# CIRCUIT DESCRIPTION

**MS4600 CPU Board Rev A**

**Covering Product Labels**

**D43014-3 (CPU Board),**
**D43016-3 (DRAM Expansion),**
**D43017-3 (Rear Connector Board),**
**D43018-3 (Front Panel Board),**
**And**
**D43020-3 (LCD Flex Cable)**

June 08,1998
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## I. ABSTRACT

The 35000 CPU board (D43014) contains most of the digital functionality of the Scorpion RF VNA, and consists of 3 major sections: Main CPU, DSP core, and Graphics core, each of which contains its own processor. The Main CPU section is an MC68040 with primary cache, and includes local system memory (16MB Fast Page Mode DRAM upgradable to 64MB, 4MB Battery Backed SRAM, 10MB Flash, 512KB Boot EPROM, 128KB NVRAM), ethernet interface, GPIB master/slave interfaces, Centronics parallel printer port, 2 serial ports, interfaces to the front panel keypad (D43018), front panel floppy disk drive, an external keyboard, and an interface to the external SCSI-2 drive. The DSP core is for calculating the sweeping S-parameter measurements and includes the TMS320C44 DSP, local system memory (2MB SRAM, 32KB Boot EPROM), global system memory (128KB SRAM) used as dual access memory to 68040 CPU, and an interface to the A/D converters located on the IF board. Finally, the Graphics core is for driving the front panel color LCD and external VGA monitor with instrument display measurements, and it includes the TMS34020 graphics processor, local system memory (1MB DRAM, 1MB Video RAM), a video palette, drivers for the VGA interface, an LCD controller, and an interface to the color LCD module through the Flex Cable (D43020).

## II. REVISION HISTORY

Rev A 6/08/98 BD Initial Issue.

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## III. BLOCK DIAGRAM

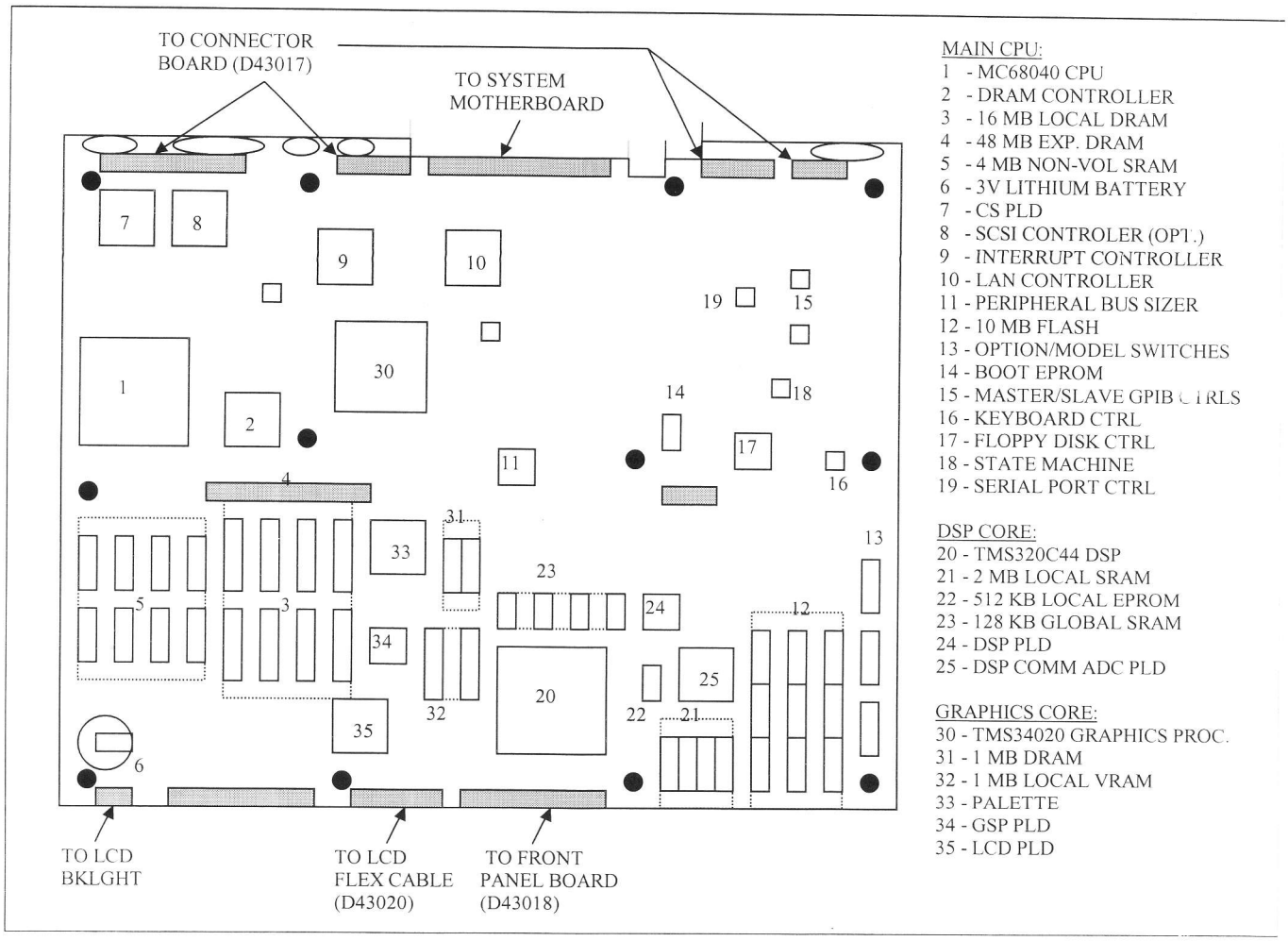



**FIGURE 1 - CPU Board Block Diagram**

## IV. EXTERNAL SPECIFICATIONS

All the signals that go on or off the board go to one of 3 destinations. They can be described as connections that go to the rear panel, the front panel, or the system motherboard. Only the rear panel connections are accessible directly by the customer. In addition, certain electrical and thermal specifications are necessary in order to guarantee observable performance within specs for all ranges of temperature and operating conditions, and these are described in this section as well.

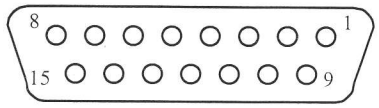
### A. CONNECTIONS TO THE REAR PANEL

Many of the connections to the rear panel go through a connector board (D43017), which brings up the height of some of the signals to couple with a second row of connectors to the outside. For each of these connectors, there will be a note in the figure indicating it belongs to the D43017 assembly. Because the functionality of the connector board is so simple, the descriptions of signals and pin numbers in this section assume the connector board is installed and are referenced to the external connector that the customer would see. All the signals can be probed directly on the CPU board although it is easier to access them from the rear panel connectors.

#### 1. ETHERNET IEEE 802.3

This connector resides on the connector board (D43017) and is used to transmit/receive ethernet signals IEEE 802.3 and carry TCP/IP protocol in order to communicate with the VNA and download new code to it. It can directly connect to a CentreCOM 210T Twisted Pair Transceiver, which is then connected to a 10 Base T cable.

J4 (ON D43017)
ETHERNET PORT



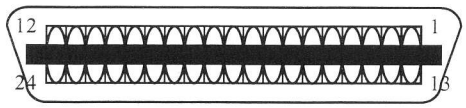

| Signal | Pin # | Signal | Pin # |
|---|---|---|---|
| LAN_T | 3 | LAN_C | 2 |
| LAN_T* | 10 | LAN_C* | 9 |
| LAN_R | 5 | LAN_12V | 13 |
| LAN_R* | 12 | GND | 1,4,6,8 |
| | | " | 11,14 |

**FIGURE 2 - Ethernet Connector Diagram**

#### 2. MASTER/SLAVE IEEE 488.2 GPIB

The two IEEE 488.2 GPIB port connectors are split up with the Master connector J8 residing on the CPU board and the Slave connector J2 residing on the connector board (D43017). Both are identical in signal layout, and differ only in the definition of slave and master.

J8
MASTER GPIB

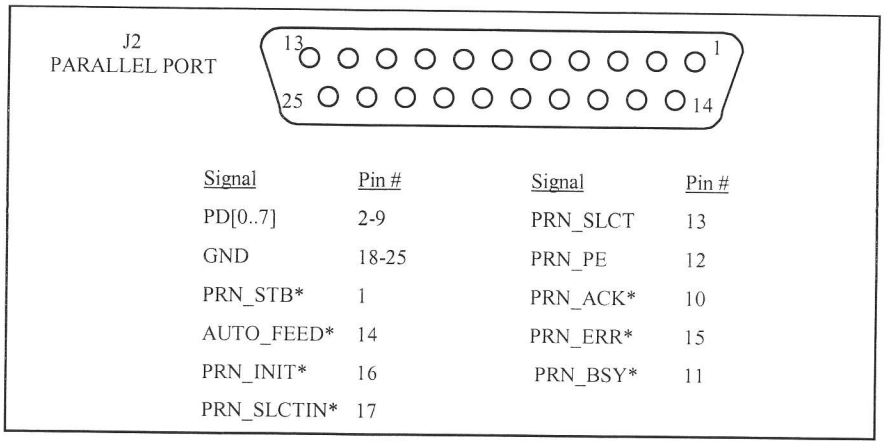



| Signal | Pin # | Signal | Pin # |
|---|---|---|---|
| DIO[1..4] | 1-4 | IFC | 9 |
| DIO[5..8] | 13-16 | SRQ | 10 |
| EOI | 5 | ATN | 11 |
| DAV | 6 | REN | 17 |
| NRF | 7 | SHIELD | 12 |
| NDA | 8 | GND | 18-24 |

**FIGURE 3 - GPIB Connector Diagram**

## 3. CENTRONICS PRINTER

The Centronics Printer port is a parallel port used for printing our hard copies of the data and waveforms from the instrument. See the following diagram for the pinout of the connector.

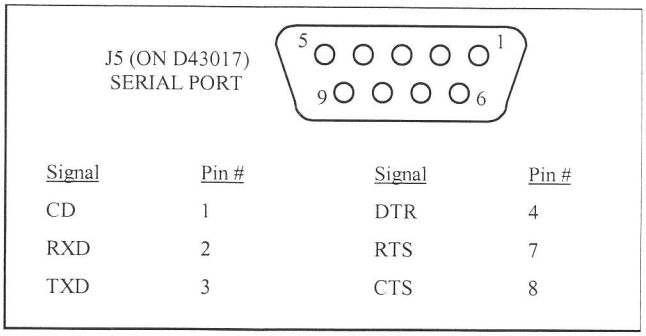



| Signal | Pin # | Signal | Pin # |
|---|---|---|---|
| PD[0..7] | 2-9 | PRN_SLCT | 13 |
| GND | 18-25 | PRN_PE | 12 |
| PRN_STB* | 1 | PRN_ACK* | 10 |
| AUTO_FEED* | 14 | PRN_ERR* | 15 |
| PRN_INIT* | 16 | PRN_BSY* | 11 |
| PRN_SLCTIN* | 17 | | |

**FIGURE 4 – Centronics Printer Connector Diagram**

## 4. SERIAL PORT

The serial port is set up to communicate at 9600bps, 8 bits, no parity, and can be connected directly to a COM port on a PC in order to use the Monitor Program, change the IP address, or see what's happening. Refer to the following diagram of a standard DB-9 interface of a male serial port connection.

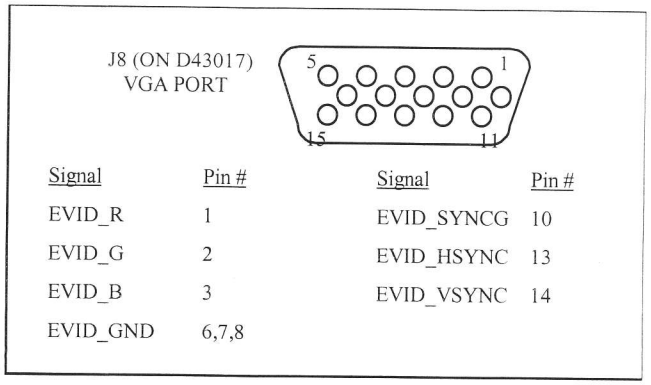



| Signal | Pin # | Signal | Pin # |
|---|---|---|---|
| CD | 1 | DTR | 4 |
| RXD | 2 | RTS | 7 |
| TXD | 3 | CTS | 8 |

**FIGURE 5 - Serial Port Connector Diagram**

## 5. VGA OUTPUT

The VGA output can be connected directly to a PC monitor, and it shows exactly the same display as what can be viewed on the color TFT LCD. It provides a way to enlarge the image by using a large size monitor, or save money by purchasing the VNA without the LCD option.

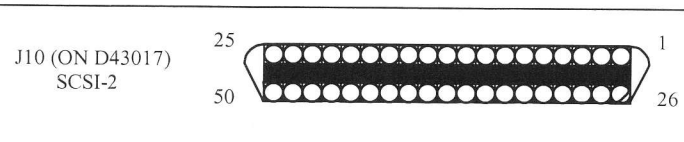



| Signal | Pin # | Signal | Pin # |
|---|---|---|---|
| EVID_R | 1 | EVID_SYNCG | 10 |
| EVID_G | 2 | EVID_HSYNC | 13 |
| EVID_B | 3 | EVID_VSYNC | 14 |
| EVID_GND | 6,7,8 | | |

**FIGURE 6 - VGA Port Connector Diagram**

## 6. SCSI-2 CONNECTOR

The purpose of the SCSI-2 connector is to connect an external SCSI-2 compatible hard drive or removable hard disk, such as an IOMEGA ZIP drive, and use it to either load new firmware into the instrument, or save files. When the unit powers up, it looks for any SCSI ID on the chain and will use it as the default hard disk if it exists; otherwise, the internal 2MB battery backed SRAM is chosen as the hard disk.

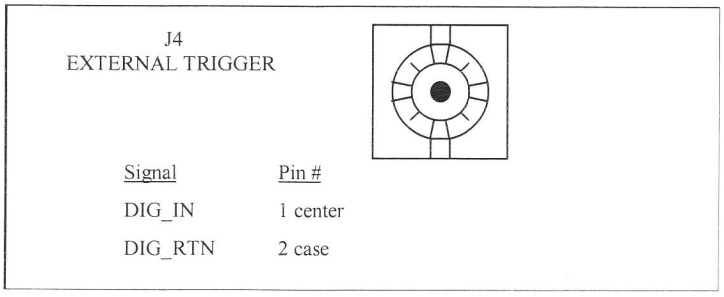



| Signal | Pin # | Signal | Pin # |
|---|---|---|---|
| DB[0..7]* | 26-33 | RST* | 45 |
| DBP* | 34 | MSG* | 46 |
| ATN* | 41 | SEL* | 47 |
| BSY* | 43 | CD* | 48 |
| SCK* | 44 | REQ* | 49 |
| TPWR | 38 | IO* | 50 |

**FIGURE 7 - Optional SCSI-2 Connector Diagram**

## 7. EXTERNAL TRIGGER IN

This is used to connect to another instrument providing a trigger source to trigger a sweep measurement. Expected signals are TTL level waveforms.




| Signal | Pin # |
|---|---|
| DIG_IN | 1 center |
| DIG_RTN | 2 case |

**FIGURE 8 – External Trigger Connector Diagram**

## 8. EXTERNAL ANALOG OUT

This is used to provide an output signal ranging from –10V to +10V and is programmable by the instrument.

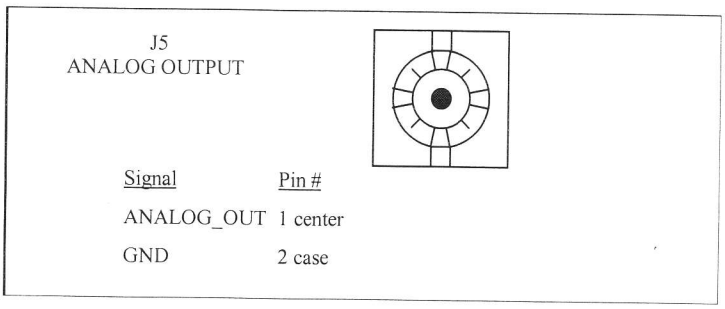



**FIGURE 9 – Analog Output Connector Diagram**

### 9. EXTERNAL I/O

This connector is used to transmit/receive TTL level signals with another instrument and display information such as channel limit fail data.

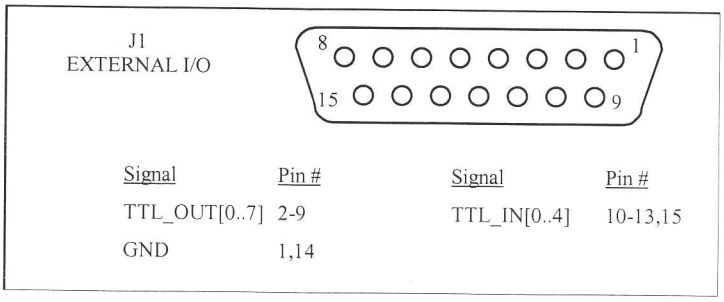


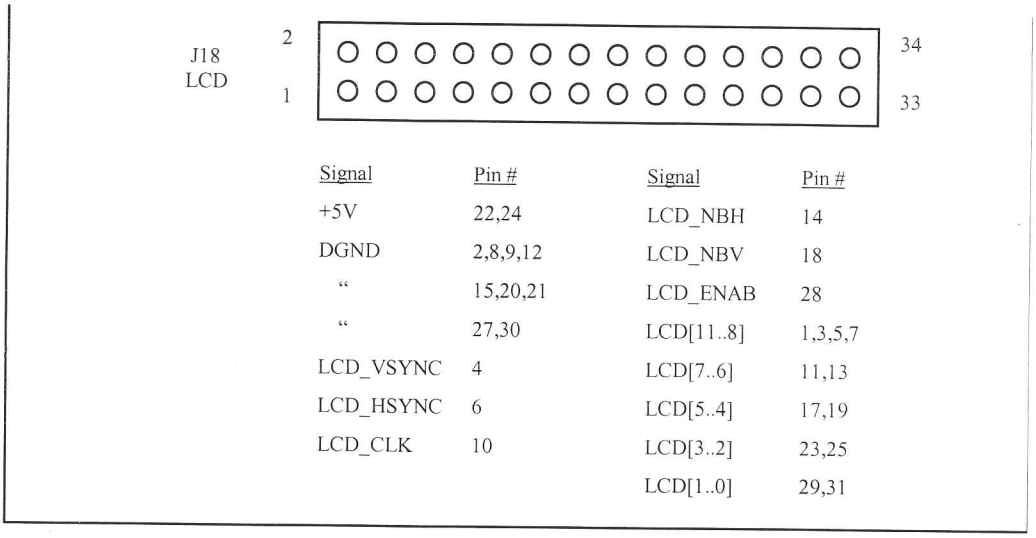

**FIGURE 10 - Ethernet Connector Diagram**

## B. CONNECTIONS TO THE FRONT PANEL

The connections to the front panel board (D43020) differ from those of the rear panel in that they all are internal to the operations of the VNA and are not directly accessible by the customer. However, if any one of these signals is operating incorrectly, then of course it will be evident to the customer. The connections are done through either flex cable (D43020) or ribbon cable and are described below.

### 1. LCD

The LCD connector (J18) shown below is used to connect to the Sharp Color TFT LCD module by using a flex cable (D43020) with a female socket on one end and a Molex connector on the other end. The cable maps the signals directly to the same pin numbers on the Sharp Color TFT LCD module for driving the data into the single panel set of latches and synchronizing the vertical and horizontal strobes.

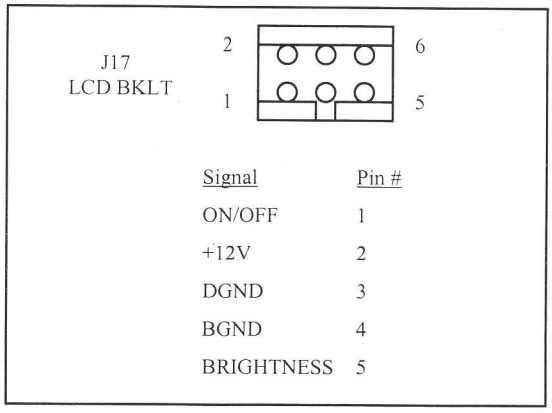



| Signal | Pin # | Signal | Pin # |
|---|---|---|---|
| +5V | 22,24 | LCD_NBH | 14 |
| DGND | 2,8,9,12 | LCD_NBV | 18 |
| " | 15,20,21 | LCD_ENAB | 28 |
| " | 27,30 | LCD[11..8] | 1,3,5,7 |
| LCD_VSYNC | 4 | LCD[7..6] | 11,13 |
| LCD_HSYNC | 6 | LCD[5..4] | 17,19 |
| LCD_CLK | 10 | LCD[3..2] | 23,25 |
| | | LCD[1..0] | 29,31 |

**FIGURE 11 - LCD Connector Diagram**

## 2. LCD BACKLIGHT INVERTER

The signals at connector J17 are for driving the Sharp Backlight AC Inverter Circuit, and are connected to it through a 5-pin ribbon cable. The AC Inverter Circuit is used to convert +12V DC into +- 200V AC for the fluorescent tube in the back of the LCD module (called a backlight). J17 is shown in the following diagram.

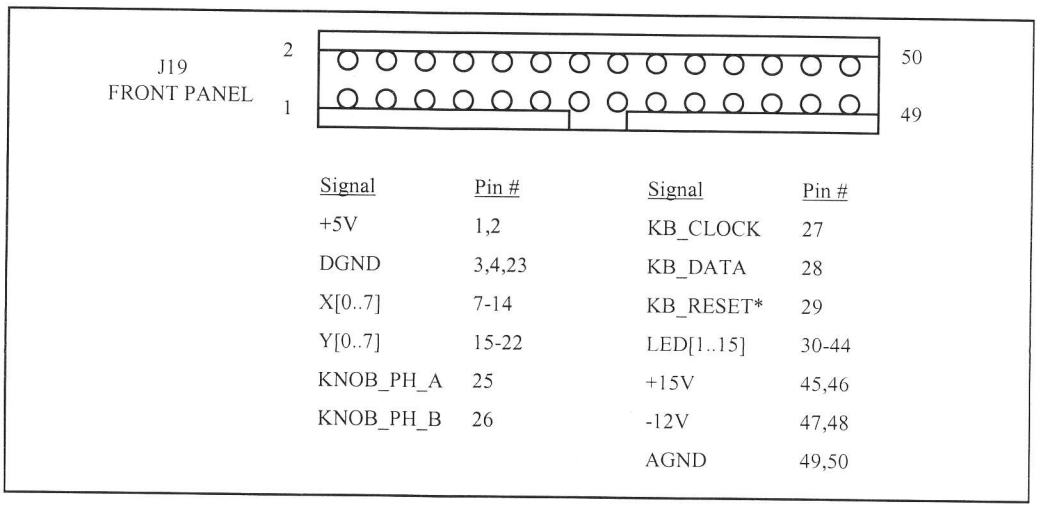



| Signal | Pin # |
|---|---|
| ON/OFF | 1 |
| +12V | 2 |
| DGND | 3 |
| BGND | 4 |
| BRIGHTNESS | 5 |

**FIGURE 12 - LCD Backlight Connector Diagram**

## 3. KEYPAD, TWIDDLE KNOB, AND KEYBOARD

The connections to the front panel board (D43018), which contains signals for the keypads, twiddle knob, LEDs, and the external keyboard, are handled through a ribbon cable connected to J19 on the CPU board. They are allocated within the connector as follows.

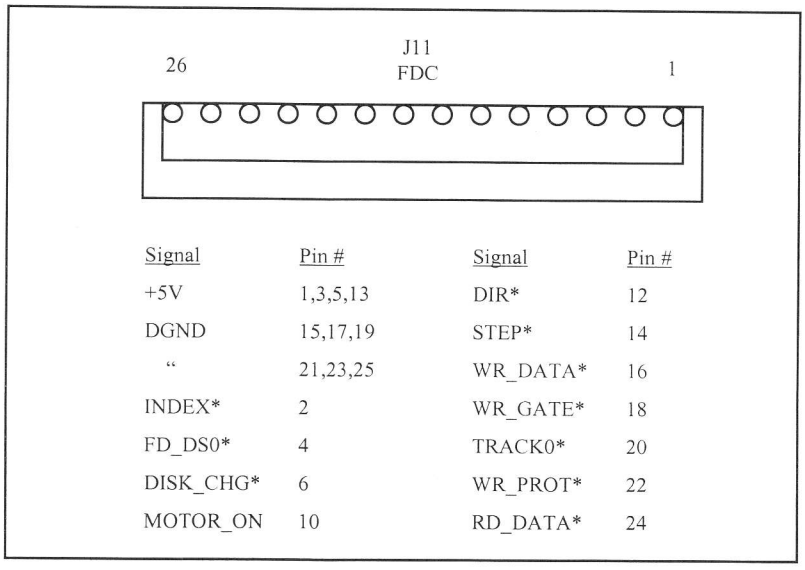



| Signal | Pin # | Signal | Pin # |
|---|---|---|---|
| +5V | 1,2 | KB_CLOCK | 27 |
| DGND | 3,4,23 | KB_DATA | 28 |
| X[0..7] | 7-14 | KB_RESET* | 29 |
| Y[0..7] | 15-22 | LED[1..15] | 30-44 |
| KNOB_PH_A | 25 | +15V | 45,46 |
| KNOB_PH_B | 26 | -12V | 47,48 |
| | | AGND | 49,50 |

**FIGURE 13 - Front Panel Connector Diagram**

### 4. FLOPPY DISK DRIVE

The connections to the Floppy Disk Drive go through a flex cable directly to the drive, which is mounted in the front of the instrument. A diagram of the connection is shown below.




| Signal | Pin # | Signal | Pin # |
|---|---|---|---|
| +5V | 1,3,5,13 | DIR* | 12 |
| DGND | 15,17,19 | STEP* | 14 |
| " | 21,23,25 | WR_DATA* | 16 |
| INDEX* | 2 | WR_GATE* | 18 |
| FD_DS0* | 4 | TRACK0* | 20 |
| DISK_CHG* | 6 | WR_PROT* | 22 |
| MOTOR_ON | 10 | RD_DATA* | 24 |

**FIGURE 14 - Floppy Disk Connector Diagram**

## C. CONNECTIONS TO THE SYSTEM MOTHERBOARD

The only connector which carries signals via the system motherboard to the I/F board, Source module, Power Distribution unit, and the Baseboard for the basic operation of the VNA is P1, and is located at the rear center of the CPU board.

### 1. P1 CONNECTOR

### 2. QUIET BUS TIMING

## D. ELECTRICAL \ THERMAL

## V. FUNCTIONAL DESCRIPTION

### A. MAIN 68040 CPU

#### 1. MEMORY MAP

**TABLE 1 - 68040 Memory Map**

| ADDRESS RANGE | DEVICE | PHYS PORT WIDTH | DECODE SIZE | ACTUAL SIZE | BURST/ CACHE INHIBIT | TRANSFER ACK | NOTE |
|---|---|---|---|---|---|---|---|
| $00000000 - 03FFFFFF | DRAM | D32 | 64 MB | 16/64 MB | N/N | DRAM PLD | 1 |
| (reserved) | | | | | | | |
| $4C000000 - 4CFFFFFF | GSP I/O regs. | D32 | 16 MB | 224 LW | Y/Y | CS PLD | 6 |
| $4D000000 - 4DFFFFFF | GSP Palette regs. | D8 | 16 MB | 256 B+ | Y/Y | CS PLD | 7 |
| $4E000000 - 4EFFFFFF | GSP VRAM | D32 | 16 MB | 1 MB | Y/Y | CS PLD | |
| $4F000000 - 4FFFFFFF | GSP DRAM | D32 | 16 MB | 1 MB | Y/Y | CS PLD | |
| (unused) | | | | | | | |
| $80000000 - 800FFFFF | DSP SRAM | D32 | 1 MB | 32/128 KB | Y/Y | DSP PLD | |
| (unused) | | | | | | | |
| $80C00000 - 80CFFFFF | New I/O Devices | (below) | 1 MB | 1 MB | Y/Y | (below) | 5 |
| (unused) | | | | | | | |
| $A0000000 - A01FFFFF | SRAM | D32 | 2 MB | 2 MB | Y/N | CS PLD | |
| (unused) | | | | | | | |
| $E0000000 - E0FFFFFF | Flash Extension | D32 | 16 MB | 10 MB | Y/N | BUS SUZER | 5,8 |
| (reserved) | | | | | | | |
| $FF800000 - FF9FFFFF | Flash/EPROM | D32 | 2 MB | 2 MB (Flash) | Y/N | BUS SIZER | 2,4,5,8 |
| $FFA00000 - FFBFFFFF | EPROM/Flash | D32 | 2 MB | 512 KB (EPROM) | Y/N | BUS SIZER | 3,5,8 |
| (unused) | | | | | | | |
| $FFD00000 - FFEFFFFF | SRAM | D32 | 2 MB | 2 MB | Y/N | CS PLD | |
| $FFF00000 - FFFEFFFF | Old I/O Devices | (below) | 960 KB | 960 KB | Y/Y | (below) | |

Notes:

1. Initially, the DRAM is disabled. To enable DRAM, control bit must be set in the DRAM Control Register at address $FFF42048, bit 24.
2. If jumper JP1 is installed, the Flash is accessed. If not, EPROM is accessed. Actual size shown for Flash.
3. If jumper JP1 is not installed, the EPROM is accessed. If so, Flash is accessed. Actual size shown for EPROM.
4. Bit 20 at $FFF42040, ROM0*, causes the boot device to be accessed at this location and at location 0 if it is cleared (default after reset). This decode at 0 must be disabled before enabling DRAM at 0.
5. Devices may be byte-wide but interface to the Bus Sizer for 8/16/32-bit accessibility.
6. Graphics I/O registers from $4C000000 - 4C0003E0 (see TMS34020 User's Guide memory map).
7. See TMS34076 data sheet.
8. Both the standard Flash ($FF...) and extended Flash ($E0...) are write enabled/disabled together.

**TABLE 2 - Old I/O Devices**

| ADDRESS RANGE | DEVICE | PHYS PORT WIDTH | DECODE SIZE | ACTUAL SIZE | TRANSFER ACK |
|---|---|---|---|---|---|
| $FFF40000 - FFF400FF | LCSR | D32 | 256 KB | $8F B | IRQ PLD |
| (unused) | | | | | |
| $FFF42000 - FFF42FFF | MC Chip | D16/D32 | 4 KB | $4F B | IRQ PLD |
| (unused) | | | | | |
| $FFF45000 - FFF45FFF | SCC (85230) | D8 | 4 KB | 4 B | BUS SIZER |
| $FFF46000 - FFF46FFF | LAN (82596CA) | D16 | 4 KB | 8 B | CS PLD |
| $FFF47000 - FFF47FFF | SCSI (53C710) | D32 | 4 KB | $40 B | SCSI |
| (unused) | | | | | |
| $FFFC0000 - FFFC7FFF | TOD clock (48T08) | D8 | 32 KB | 8 KB | BUS SIZER |
| $FFFC8000 - FFFCBFFF | Disable Flash writes | D8 | 16 KB | 8 KB | BUS SIZER |
| $FFFCC000 - FFFCFFFF | Enable Flash writes | D8 | 16 KB | 8 KB | BUS SIZER |

**TABLE 3 - New I/O Devices**

| ADDRESS RANGE | DEVICE | PHYS PORT WIDTH | DECODE SIZE | ACTUAL SIZE | TRANSFER ACK |
|---|---|---|---|---|---|
| $80C00000 - 80C00FFF | TTL I/O | D8 | 4 KB | 1 B | BS PLD |
| $80C01000 - 80C01FFF | Line Printer | D8 | 4 KB | 1 B | BS PLD |
| $80C02000 - 80C02FFF | Floppy Disk Ctrl | D8 | 4 KB | 6 B | BS PLD |
| $80C03000 - 80C03FFF | Floppy Disk Ctrl TCNT | D8 | 4 KB | (pulse) | BS PLD |
| $80C04000 - 80C04FFF | Front Panel Keypad | D8 | 4 KB | 1 B | BS PLD |
| $80C05000 - 80C05FFF | External Keyboard | D8 | 4 KB | 1 B | BS PLD |
| $80C06000 - 80C061FF | Twiddle Knob | D8 | 512 B | 1 B | BS PLD |
| $80C06200 - 80C063FF | Twiddle Knob Int Reset | D8 | 512 B | 1 B | BS PLD |
| $80C06400 - 80C065FF | Analog output (LSB) | D8 | 512 B | 1 B | BS PLD |
| $80C06600 - 80C067FF | Analog Output (MSB) | D8 | 512 B | 1 B | BS PLD |
| $80C06800 - 80C069FF | Analog Monitor | D8 | 512 B | 1 B | BS PLD |
| $80C06A00 - 80C06BFF | System ID | D8 | 512 B | 1 B | BS PLD |
| $80C06C00 - 80C06DFF | System Options | D8 | 512 B | 1 B | BS PLD |
| $80C06E00 - 80C06FFF | LCD Backlight Ctrl | D8 | 512 B | 1 B | BS PLD |
| $80C07000 - 70C07FFF | GPIB Master | D8 | 4 KB | 21 B | BS PLD |
| $80C08000 - 80C08FFF | GPIB Slave | D8 | 4 KB | 21 B | BS PLD |
| $80C09000 - 80C09FFF | Intr Ctrl (new regs.) | D32 | 4 KB | 7 LW | IRQ PLD |
| $80C0A000 - 80C0AFFF | Meas State Machine | D8 | 4 KB | (pulse) | BS PLD |
| $80C0B000 - 80C0BFFF | CPU->MSM Intr | D8 | 4 KB | (pulse) | BS PLD |
| $80C0C000 - 80C0CFFF | Miscellaneous I.O | D8 | 4 KB | 2 B | BS PLD |
| $80C0D000 - 80C0DFFF | CPU->DSP Intr | D8 | 4 KB | (pulse) | BS PLD |
| $80C0E000 - 80C0EFFF | LED Registers | D8 | 4 KB | 2 B | BS PLD |
| $80C0F000 - 80C0FFFF | spare | D8 | 4 KB | | |
| $80C10000 - 80C1FFFF | Quiet Bus | D16 | 64 KB | 1 W | BS PLD |
| $80C20000 - 80C3FFFF | NVRAM (not used) | D8 | 128 KB | 128 KB | BS PLD |

## 2. PROGRAM AND DATA CACHE

## 3. ENHANCED PAGE MODE DRAM

The DRAM is intended to provide up to 16MB of available memory (64 MB with D43016) for executing application code and storing application data optimized for speed at the 32MHz bus clock frequency. As shown in figure 15, the memory devices are split up into 2 distinct and separate data buses, even (ED[31..0]) and odd (OD[31..0]), which are selectively connected to the main 68040 CPU data bus through a set of data bus transceivers. The DRAM controller is responsible for selecting the even or odd data bus to the DRAM and setting the row (RAS/) and column (CAS/) address strobes appropriately for the DRAM to function. In addition, the DRAM controller provides all necessary refresh signals to keep the data valid while power is applied using a CAS-before-RAS method of refresh.

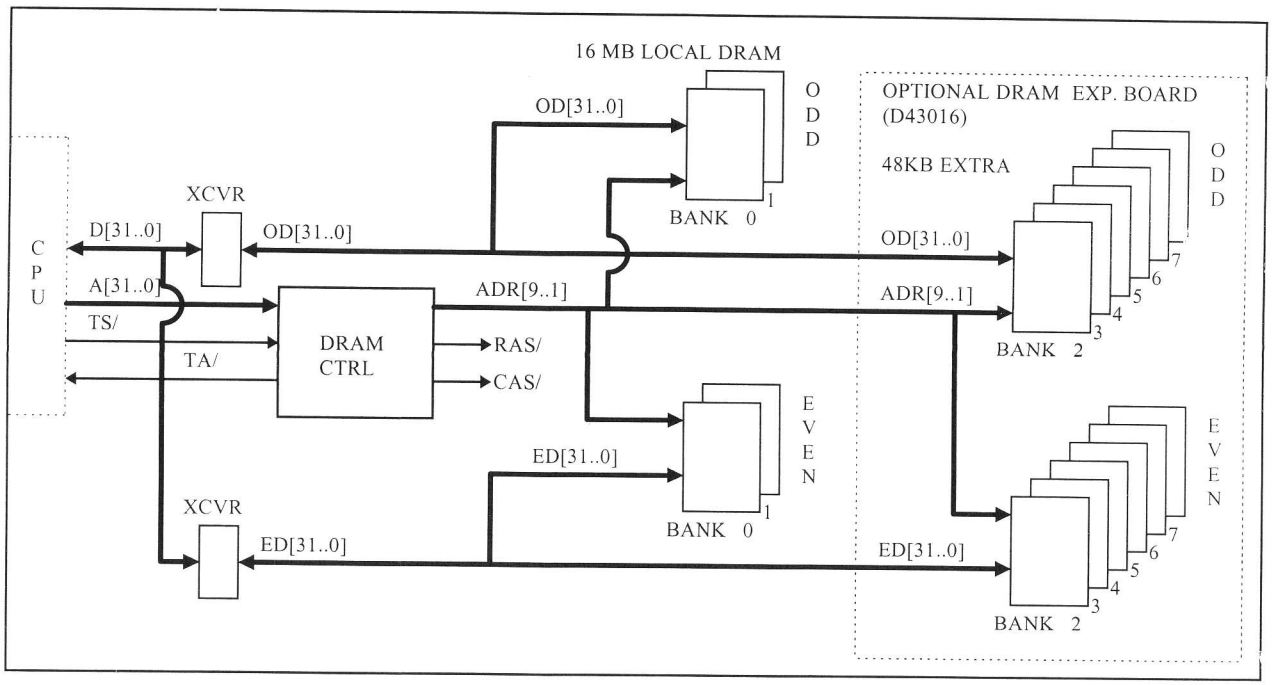



**FIGURE 15 - DRAM Memory Block Diagram**

## 4. BATTERY BACKED SRAM

The 4MB of Battery-Backed SRAM is intended for two applications. One is to emulate a hard disk drive as a way to store setups and parameter measurements, in a non-volatile way, with faster-access time than that associated with a hard drive. The other application is to provide fast access, 32-bit, non-volatile memory for the 68040 CPU. It consists of the SRAM devices and a MAXIM voltage supervisor circuit that switches between the voltage supply VCC (+5V) and a Lithium Battery VBATT (+3V) whenever there is a shutdown in the power supply line. When the power is turned back on, the MAXIM circuit switches back from the Lithium Battery VBATT to the regular VCC supply. During the period when the Lithium Battery is supplying power to the SRAM devices, all the SRAM devices are write protected through a gated chip select line (CE/). The Lithium Battery chosen provides 500 mA hours of continuous VBATT supply, which is enough to keep the data in the SRAM valid for up to 2 years in the event of a power shutdown. During normal operation, a small constant drain on the battery is expected to exhaust the battery in about 6 years.

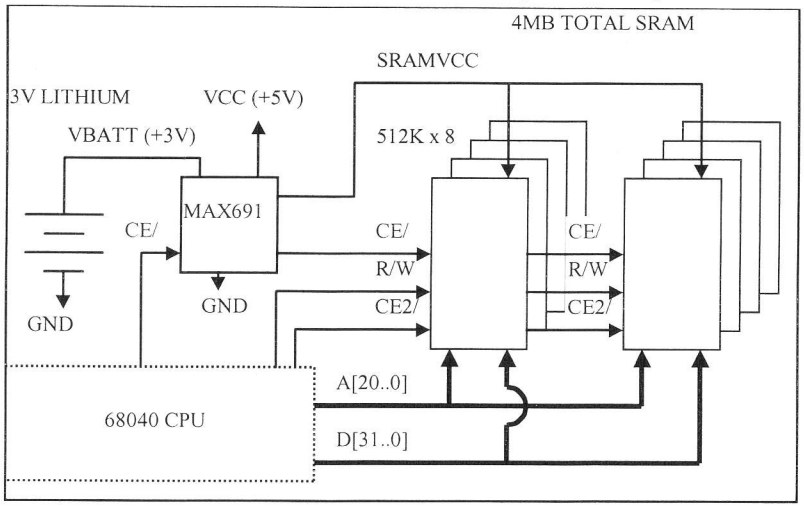



**FIGURE 16 - Battery Backed SRAM**

## 5. CHIP SELECT PLD

## 6. INTERRUPT CONTROLLER

## 7. ETHERNET CONTROLLER

The Ethernet subsystem includes Intel's 82596CA controller, 82C501AD

## 8. SCSI CONTROLLER

The SCSI subsystem includes the NCR53C710 SCSI controller and 2-50pin SCSI II connector. The 53C710 is composed of three functional blocks: the SCSI Core; the DMA Core; and the SCRIPTS Processor. The SCSI core supports synchronous transfer rates of up to 10.0 MB/S, and asynchronous transfer rates greater then 5 MB/S. The DMA core is a bus master DMA device that directly attaches to the 68040. The SCRIPTS processor is a special high-speed processor optimized for SCSI protocol. It allows both DMA and SCSI instructions to be fetched from host memory. Complex SCSI bus sequences are executed independently of the 68040.

## 9. OPTIONS AND MODEL SWITCHES

The switches and their meanings are shown in the following diagram. For the option switches, a bit set to 0 indicates that the option is installed, while a 1 indicates that the option is not avaliable.

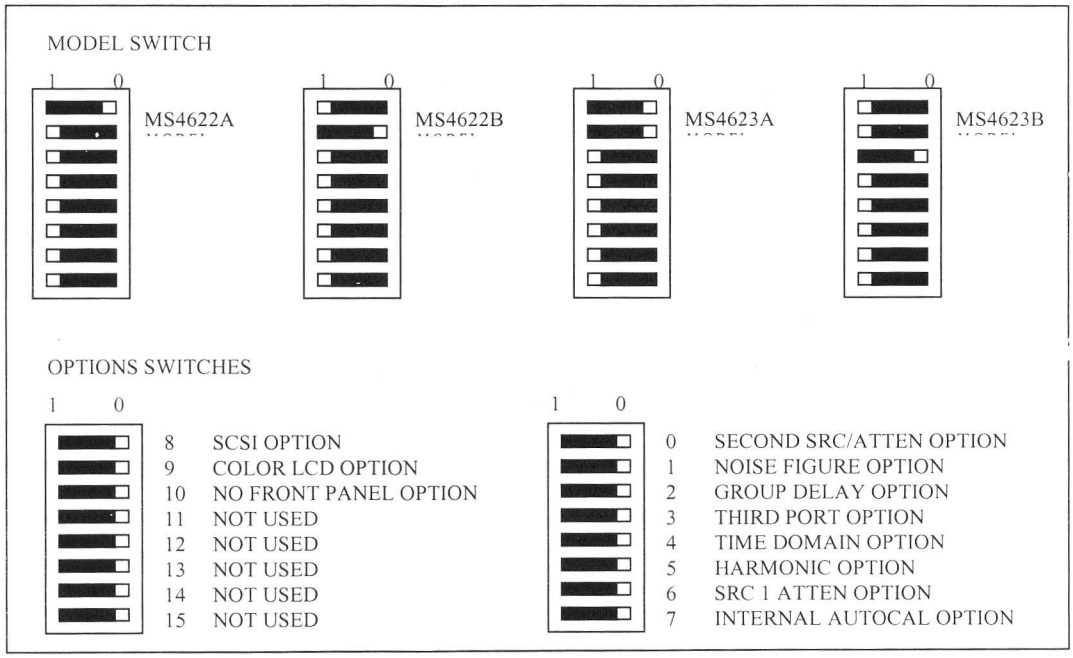



**FIGURE 17 – Model and Option Switches**

## 10. STATE MACHINE

The state machine is programmed on an Altera EPM7032LC44-15. This device controls the start conversion pulse for the A/D converters on the IF board. When measurement is requested, the state machine triggered and will begin monitoring the QB_STATUS line. If the QB_STATUS goes high, the state machine exits and a start conversion signal is pulsed. If after 400 usec the QB_STATUS remains low, the state machine exits and a state machine interrupt is issued to the DSP indicating a possible lock failure.

## 11. PERIPHERAL BUS

The peripheral bus is 16-bit wide. Most of the system's I/Os use this bus. They include: Timekeeper RAM, Floppy Disc Control, Flash memory, DUAL UART, TTL I/O, Line printer control, Boot-up EPROM, Miscellaneous I/O, External Keyboard control, Front Panel Keypad, GPIB and the Quiet bus. Most of these devices have 8-bit interfaces. So the Bus Sizer 68150-33 does the data arrangement from the 32-bit main bus to 8 or 16-bits.

### 12. TIMERS AND PSOS

There are two timers on the DSP which are configured for use by the system. The first timer is set for 10 msec and this is used as the pSOS tick timer. The tick timer is required by pSOS. The other timer on the DSP is configured for 10 usec. The main purpose of this timer is to support the sweep time functionality. This timer is used to measure the sweep time and also for inserting delay. The 10 usec timer allows the sweep time to be calculated more precisely.

## B. DSP CORE

The digital signal processor is Texas Instruments's 50 Mhz TMS320C44. It uses 2 Mbytes of SRAM for its program and data storage arrays. There is also 32 Kbytes of SRAM used for data transfers between the DSP and the 68040. The DSP has two external buses, one is used to access the global SRAM and trigger interrupts to the CPU while the other is used to access local SRAM and the dsp boot eprom. Only the global SRAM is accessible by the CPU. When the local bus is accessed, the local strobes, LSTRB0 or LSTRB1 is activated. When the global bus is accessed, GSTRB0 or GSTRB1 is activated. The strobes are used to access the memory devices. There is also a 14 pin header JTAG connector for emulation. The memory map for the DSP is as follows, this is not in the memory map for the CPU:

| ADDRESS SPACE | FUNCTION | CONTROL SIGNALS | WIDTH | SIZE | WAIT STATES |
|---|---|---|---|---|---|
| **$0000 0000 – 0000 0FFF** | On-chip ROM | Internal | Long word | N/A | N/A |
| **$0030 0000 – 003F FFFF** | EPROM | LSTRB0 | Byte | 32 Kbytes | 1 internal wait state |
| **$0040 0000 – 7FFF FFFF** | Local SRAM | LSTRB1 | Long word | 2 Mbytes | No wait states |
| **$8000 0000 – BFFF FFFF** | Global SRAM | GSTRB0 | Long word | 128 Kbytes | External |
| **$C000 0000 – FF7F FFFF with A23 = 0** | DSPIRQ | GSTRB1 | Long word | N/A | 7 internal wait states |
| **$C080 0000 – FFFF FFFF with A23 = 1** | STOP A/D | GSTRB1 | Long word | N/A | 7 internal wait states |

Note that the GSTRB1 signal has two functions. It is used with address line 23 to signal an interrupt for the 68040. If GSTRB1 is active and address line 23 is low, a dsp interrupt is generate for the 68040. If the address line 23 was high, a stop A/D pulse would be generated for the converters.

### 1. LOCAL MEMORY

The boot up eprom is an AMD 27c256-55JC in a PLCC-32 socket and is 32 Kbytes in size. This eprom is used for boot program storage. The reset line must be active for at least 400 ns to ensure proper reset of the DSP. When the reset line is released, the DSP will invoke the bootloader. The bootloader is a TI program that resides in on-chip ROMand is invoked if ROMEN is high upon reset. The bootloader simply downloads a program from a specified location. This location is identified by the IIOFx pins upon reset. For our application, this will point to the eprom. The bootup program will support the monitor program and handle the download or the main application.

The local SRAM is 2Mbytes organized as 512K X 8 bits. The speed of the memory is 20 ns, therefore no wait states are necessary to access the local SRAM. Local SRAM is used to store the application code and data arrays allocated by the application. This memory is not accesible by the 68040.

### 2. INTERFACE BETWEEN DSP AND 68040 MAIN CPU

The global SRAM is 128Kbytes organized as 32K X 8 bits. This memory is accessible by both the DSP and 68040. The shared SRAM is arbitrated btween the DSP and 68040 with the DSP having greater priority. For reads and writes by the 68040 the data is first latched in to buffers before being transferred to the DSP bus or the 68040 bus. The arbitration and communication signals between the DSP and 68040 are handled by a DSP control PLD. The PLD is an Altera EPM7064LC68-10. The PLD controls the reset operation of the dsp reset line and setting the proper values of the IIOFx pins upon reset. The PLD is also responsible to generate interrupts for the 68040 and for the DSP. The DSPIRQ and STOP_AD signals are generated from the PLD based on GSTRB1 and DSPA23. The interrupts from the state machine and 68040 are routed to the corresponding IIOFx pin for the DSP by the PLD. If there is a phase lock fail during the measurement, the status is detected by the PLD and passed to the DSP.

### 3. INTERFACE TO A/D CONVERTERS

Communication between the A/D converters and the DSP is programmed into an Altera EPM7128ELC84-20 FPGA. This controller will collect eighteen serial bits, generated from the A/D converters, most significant bit first. When eight bits are received, they are sent to the DSP communication ports, one designated for the test channel and another one for the reference channel. The communication ports were originally designed for intercommunication between DSP processors without needing external logic. Therefore to utilize the communication ports, the A/D interface controller emulates a DSP processor in terms of the communication port control signals. For each sample, there will be four byte

transfers from the controller to the DSP via an 8-bit communication port data bus. Eighteen bits will contain the data, the remaining bits will be set to zero and not be used by the DSP program. This is due to the fact that the DSP communication port must receive 32 bits of data because the FIFO's of the communication ports are 32 bits wide. Further details regarding the communication scheme for the communication ports can be found in the TMS320C4x User's Guide.

## C. GRAPHICS CORE

The graphics processor is the TI's TMS34020AGBL-40. It's acting as a slave on the system's bus and is capable of generating an interrupt back to the host processor. The standard mode of display is 640X480 resolution with 8 bits per pixel. On the graphics processor local bus side, the 34020 uses a 1-Mbyte VRAM array to hold its video frame data and a 1-Mbyte DRAM array for program and data storage. These memories are also mapped into the main address space through a set of buffers. The 34020 controls the video palette chip through its 8-bit control port. The 34020 initializes in the "load from host" mode; therefore the 34020 is incapable of running until the host processor downloads code and configuration parameters.

### 1. LOCAL VRAM MEMORY

The VRAM is 1-Megabyte organized as 256K X 32 bits. The content is accessible by the graphics controller (34020), palette chip, and the LCD controller. It stores two complete frames of display data, organized by rows and columns. Each address contains a 32-bit word, which represents 4 adjacent pixels on the display. Each pixel is 8-bits or one of 256 colors. There is the working frame, and the other is the active frame, which is the one currently being sent to the display devices (LCD and VGA). The active and working frames toggle once in awhile to allow the recently changed drawings to be seen by the user.

### 2. LOCAL DRAM MEMORY

The DRAM is 1-Megabyte organized as 256K X 32 bits. The content is accessible by the graphics controller (34020), and is used for code and variable storage. When the instrument boots up, the graphics code gets loaded here, before the graphics controller (34020) can run by itself. Internal register initialization of the 34020 is handled by the startup code.

### 3. PALETTE AND VGA SIGNALS

The video palette chip is TI's TMS34076. The standard clock input for it is 25 MHz, and 32 MHz can be optionally provided for additional video display modes by the addition of a second oscillator. The 25 MHz is required for 640X480 resolution at 8 bits per pixel. The RGB and sync outputs from the chip are buffered to used to drive the system's external monitor through a 15 pin DSUB connector (see Figure 6).

### 4. LCD CONTROLLER

The LCD controller is the Altera's EPF8452AQC160-2 FPGA. It's main function is to mimic the palette operations and convert VRAM contents from 32 bits format to 4 pixels (8-bits LCD color codes). The LCD controller uses a RAM device as the color lookup table, and can be reloaded by the software like the palette. The output of the LCD controller is all the signals needed to drive the LCD display including vertical and horizontal syncs.

## VI. PERFORMANCE VERIFICATION

There are 3 major steps to verifying the performance of the manufactured CPU assembly. The first two will be done by the manufacturer of the assembly (Altron Systems Corp. in our case), and the last will be done here at Anritsu Company.

### A. ICT TEST (TO BE DONE BY MANUFACTURER)

The first step in testing the CPU assembly is a board level ICT test. This will test every connection and component on the board, and leads to a high level of confidence the board is manufactured defect-free. After this step is completed, we proceed with the assembly level functional test. A summary of the ICT test descriptions is listed below.

1. **SHORTS AND OPENS TEST**
2. **RESISTORS, CAPACITORS, INDUCTORS, AND DIODES TEST**
3. **FUNCTIONAL AND BIST IC TEST**
4. **BOUNDARY SCAN AND JTAG IC TEST**
5. **OPEN EXPRESS IC TEST**

### B. FUNCTIONAL TEST (TO BE DONE BY MANUFACTURER)

The functional test is the second step in verifying the performance of the CPU board and its assembly into the metal tray with the rear panel connector board, D43017. This test, when applied after the ICT test, will additionally test all the connectors, which go off the CPU assembly, and confirm they will operate as expected with other boards in the system. Also, the on board configuration memory and clock will be initialized, and the firmware downloaded to Flash ROM. After this test is over, the CPU tray will be ready to slide into any Scorpion instrument, after setting the appropriate dip switches for the model number and options, and it should boot up and run code properly. Then, it will be ready to test the rest of the instrument as described in Section C.

#### 1. CONFIGURE MEMORY AND ETHERNET ADDRRESS

Insert the MONITOR PROM in U75, and connect the serial port to a PC running Windows Terminal. Configure it for 9600 Baud, no parity, 8 data bits, 1 stop bit. Power on the instrument and type the following commands.

BUG> cnfg;m

Use the following answers:

CLOCK SPEED = "32 "
ETHERNET ADDRESS = "00E0A0000XXX" where XXX is the next available address
DRAM SIZE = "16"
SRAM SIZE = "2048"
DSP SHARED MEMORY = "0128"
FLASH SIZE = "02"
EXTENDED FLASH SIZE = "08"

Read the same information back using

BUG> cnfg

All previous information should be there.

#### 2. EXTERNAL I/O TEST

Connect a cable between the external I/O connector (J1) and the test board provided (D43034). Type in the following commands and observe the output.

| | |
|---|---|
| BUG> bf 80c00000:1 a5;b | Expect to see the LEDs displaying the hex value 0xA5. |
| BUG> md 80c00000:1;b | The return result should be 0x05. |
| BUG> bf 80c00000:1 5a;b | Expect to see the LEDs displaying the hex value 0x5A. |
| BUG> md 80c00000:1;b | The return result should be 0x1A. |

### 3. EXTERNAL TRIGGER TEST

Connect a cable between the external trigger connector (J4) and the test board provided (D43035). Using an oscilloscope, monitor the signal on U98 pin 12. It should be a square wave TTL level signal.

### 4. EXTERNAL ANALOG OUTPUT TEST

Connect a cable between the external analog output connector (J5) and a Fluke Digital Voltmeter. Type in the following commands and observe the output.

BUG> bf 80c06600:1 00;b

BUG> bf 80c06400:1 00;b  Expect to see –10V.

BUG> bf 80c06600:1 0c;b

BUG> bf 80c06400:1 00;b  Expect to see +5V.

### 5. ETHERNET TEST

Power down the instrument, and insert the XRAY PROM in U75. Connect the Ethernet port (J4 of D43017) to a PC network interface card, and power p the instrument. When the instrument boots up, configure it by choosing the following answers to the questions posed.

| | |
|---|---|
| M | Choose this to modify the parameters |
| 3 | Select PROBE |
| Y | Choose to select LAN interface. |
| 172.26.21.200 | Set the new IP address |
| C/R | Hit C/R for the rest of the entries except timeout |
| 2 | Set the timeout period to 2 seconds. |
| C | Choose this to continue with operations |

Save all the above information, and then go to the PC and ping the address 172.26.21.200. It should respond to the network interface card, which sent the ping request. Go back and reset the IP address to 0.0.0.0 when done.

### 6. DOWNLOAD FIRMWARE

Power down the instrument, and insert the original 58-1638 PROM in U75. Connect the SCSI-2 connector (J10 on D43017) to the IOMEGA zip drive containing the current software diskette, and power on the instrument. The code will take approximately 5 minutes to load. Disconnect the zip drive when finished.

### 7. PRINTER TEST

Connect a cable between the parallel printer port (J2) and a printer. Go to START PRINT menu and send an output to the printer.

### 8. VGA MONITOR TEST

Connect an external monitor to the VGA connector (J8) and verify the output looks the same as the LCD display.

### 9. GPIB TEST

Connect a cable between the two GPIB connectors (J2 on D43017 and J8 on D43014), and go to UTILITY\DIAGNOSTICS\PERIPHERAL TESTS menu and select GPIB TEST. Press the ENTER key to start and the test should pass.

### 10. CLOCK SETUP

Go to UTILITY\CLOCK SETUP menu and set the current time and date.

### 11. LCD TEST

Connect the front panel LCD using the flex cable (D43020) and verify the display looks the same as the VGA output.

### 12. FRONT PANEL KEYPAD TEST

Go to UTILITY\DIAGNOSTICS\PERIPHERAL TESTS menu and select the KEYPAD TEST. Follow the directions and the test should pass.

### 13. FLOPPY DISK TEST

Connect the front panel floppy disk drive with the cable and insert a diskette into the drive. Go to SAVE\RECALL menu and select DIRECTORY. It should display the contents of the diskette correctly.

## C. SYSTEM SELF TEST (TO BE DONE BY ANRITSU)

### 1. MONITOR PROGRAM

In the user-triggered self test the monitor program tests include the following tests:

#### 1.1 LANC test

The LANC test tests the system's Ethernet controller Intel's CA82596. It includes the controller's self test and DUMP test. The self test executes the on chip self test. The DUMP executes the CA82596's DUMP command.

#### 1.2 SCC test

The SCC test tests the system's serial port controller Zilog's 85230. It runs the device/registers access test.

#### 1.3 RTC test

The RTC test tests the system's real time clock SGS Thomson's M48T18. It includes three sub-tests: clock test, ram test and address test. The clock test tests the chip's timekeeper functionality. The ram test tests the chip's "Zero Power" RAM functionality. The address test tests the chip's "Zero Power" RAM addressibility.

#### 1.4 SCSI test

The SCSI test tests the system's hard drive controller NCR 53C710. It consists of five sub-tests. The ACC1 test tests the basic accessibility to the device itself. The ACC2 test tests the accessibility to the registers. The SFIFO test tests the basic ability to write data into the SCSI FIFO and retrieve it in the same order as written. The DFIFO test tests the basic ability to write data into the DMA FIFO and retrieve it in the same order as written. The LPBK (loop back) test checks the input and output data latches and performs a selection, with the 53C710 executing initiator instructions and the 68040 implementing the target role by asserting and polling the appropriate SCSI signals.

#### 1.5 DSP test

The DSP test runs the TMS320C44 on-chip self test code to make sure the functionality.

In the troubleshooter mode the user can choose the following monitor program's memory tests, each of these test consists of code that write different patterns to the memory locations and read them back later to verify the memory is working. Some tests also contain code that copy a short execution procedure into the respective memory and run the program and verify with the output of the program.

#### 1.6 DRAM test

#### 1.7 SRAM test

#### 1.8 SRAMDISK test

#### 1.9 GVRAM test

#### 1.10 GDRAM test

#### 1.11 FLASH memory test

#### 1.12 EXTENDED FLASH memory test

## VII. RELATED DOCUMENTS


[1] Schematic drawing, D43014, Anritsu Company, Rev A, 5/5/98.

[2] MC68040 User's Guide, Motorola Company,

[3] TMS320C44 User's Guide, Texas Instruments, 1996.

[4] TMS34020 User's Guide, Texas Instruments, August 1990.

[5] BUG software documentation

[6] FPGA equations, 58-1783.ZIP, Anritsu Company, PVCS System

[7] SCSI-2 Specification, CCITT.