AUTOMATIC BOOTSTRAP LOADER

an option for the
Varian Data Machines 620/f
Computer System

Specifications Subject to Change Without Notice

varian data machines/a varian subsidiary

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FOREWORD

The 620/f Automatic Bootstrap Loader Manual defines and explains the logical, electrical, and mechanical parameters that control the interface between a Varian Data Machines 620/f computer and the automatic bootstrap loader option.

The six sections of the manual:

- Introduce the automatic bootstrap loader in relation to the system
- Describe its installation and interfacing
- Give a detailed theory of operation
- Describe testing and troubleshooting procedures for maintaining it in the field
- Reference all hardware with drawings, parts lists, and wire lists

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1.1 SYSTEM OVERVIEW

The *Model 620/f-15 Automatic Bootstrap Loader (ABL)* is a mainframe option for the Varian Data Machines 620/f computer system. The ABL loads a short bootstrap program into the 620/f core memory whenever the BOOTSTRAP switch on the computer control panel is pressed. This bootstrap program can then load the Varian binary load/dump II program (BLD II), which in turn can load and execute any other 620 programs. After pressing BOOTSTRAP, the bootstrap loading and the loading and execution of the operational program is fully automatic, thus eliminating the time and effort of manual loading and manipulation. The ABL is intended to be used only when the contents of memory are unknown.

The ABL hardware is on a portion of one standard 620/f wired-socket card in the mainframe. There is, in addition, a connection to the BOOTSTRAP switch on the computer control panel.

The ABL includes one or two read-only memory (ROM) units each capable of holding sixteen 16-bit words of the bootstrap program. The standard ABL, which is programmed either for Teletype (TTY) or for paper tape reader input, requires only one ROM unit. ABLs programmed for other I/O devices require one or two units, according to the size of the bootstrap program for the particular device.

NOTE

In this manual, numbers beginning with a digit other than zero are decimal numbers and numbers with a leading zero are octal.

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INTRODUCTION

1.2 FUNCTIONAL DESCRIPTION

The ABL is functionally divided into eight circuits: BOOTSTRAP switch control logic, bootstrap loader timing and control logic, register loading and CPU control logic, CPU control logic drivers and receivers, address counter, ROM logic, word assembly buffer, and AB bus drivers. Figure 1-1 is the ABL functional block diagram.

1.2.1 BOOTSTRAP Switch Control Logic

This circuit, located on the computer control panel, provides a pulse to the ABL whenever the BOOTSTRAP switch is pressed. This pulse initiates the loading of the bootstrap program.

The pulse is not sent if the BOOTSTRAP switch is disabled. The switch is disabled whenever the CPU is in RUN mode, or the ABL is busy executing a previous operation.

1.2.2 Bootstrap Loader Timing and Control Logic

This circuit initiates and controls the transfer of data from the ROM to the computer core memory. Specifically, this logic controls the following four functions:

It recognizes the pulse from the BOOTSTRAP switch control logic and then initiates the bootstrap program loading sequence.

It performs the bootstrap program loading sequence. This consists of reading data out of sequential addresses in the ROM and transferring these data to the computer core memory. The transfer is controlled by the 620/f direct memory access (DMA) port to memory.

It resets and advances the address counter of the ABL during the loading of the bootstrap program.

It strobes the flip-flops of the ABL word assembly buffer during the loading of the bootstrap program. This strobe controls the assembly of the ROM data bytes into 620/f computer words.

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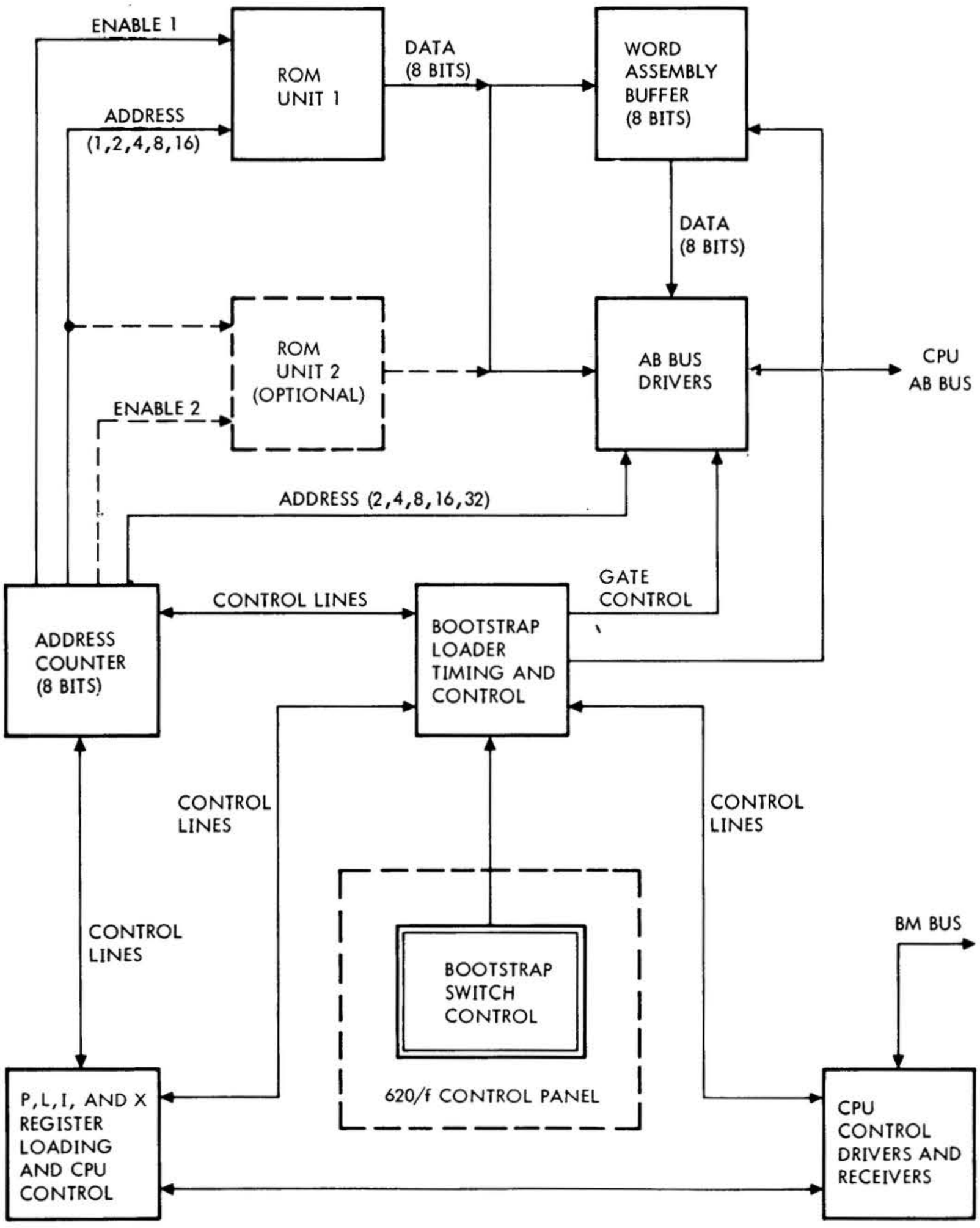

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Figure 1-1. Automatic Bootstrap Loader Block Diagram

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INTRODUCTION

1.2.3 Register Loading and CPU Control Logic

This circuit decodes the states of the address counter, thus controlling the loading of the registers and the termination of the ABL operation.

During the loading of the bootstrap program, this decoding loads the 620/f program (P), memory address (L), instruction (I), and index (X) registers with the data necessary to execute the bootstrap program. This execution occurs after the program is loaded and the CPU enters RUN mode.

When this logic detects the final state of the address counter, it generates the signal putting the 620/f in RUN mode. It also terminates the ABL operation.

1.2.4 CPU Control Logic Drivers and Receivers

This circuit is the interface between the ABL and the 620/f I/O control signals.

1.2.5 Address Counter

This circuit enables the ABL ROM and provides it with the five-bit addresses. It also provides the least significant five bits of the memory trap address.

The address counter also transmits control signals to both the bootstrap loader timing and control logic (section 1.2.2) and the register loading and CPU control logic (section 1.2.3).

1.2.6 Read-Only Memory (ROM) Logic

The ABL ROM contains the bootstrap program to be loaded into computer memory when the BOOTSTRAP switch on the 620/f control panel is actuated. Since the bootstrap program is specific to a particular input device, a separately programmed ROM for each device is required. However, only one type of device per system is accommodated by the standard ABL ROM.

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If the bootstrap program for the specified input device requires 17 to 32 computer words of 16 bits each, two ROM units are installed in the ABL. If fewer than 17 words are required, only one ROM unit is installed. The ROM configurations for the available input devices are indicated in table 1-1. In configurations requiring two ROM units, unit 1 contains the first 16 words of the bootstrap program, and unit 2 the remainder. The standard ABL has only one ROM unit.

Table 1-1. ABL ROM Configurations

Input Device	ROM Unit 1 (F2)	ROM Unit 2 (H2)
Teletype	Required	Unused
Paper Tape Reader	Required	Unused

Each ROM unit is within a 16-pin dual-in-line chip. It is a monolithic, high-speed, transistor-transistor logic (TTL) 32-byte memory. It is externally addressed by five bits from the address counter (section 1.2.5) and decodes the addresses internally. Each of the eight output transistor circuits within the chip can sink a maximum of 12 mA.

Figure 1-2 shows the formats of the ROM bytes and the 620/f computer words, and their correspondence. Table 1-2 shows the correspondence between the ROM byte addresses in each ROM unit and the 620/f bytes and words.

1.2.7 Word Assembly Buffer

This buffer stores an eight-bit byte read out of an even-numbered ROM address so that when the corresponding odd-numbered address byte is read out, the two bytes can be assembled into a 16-bit computer word for entry into the 620/f core memory.

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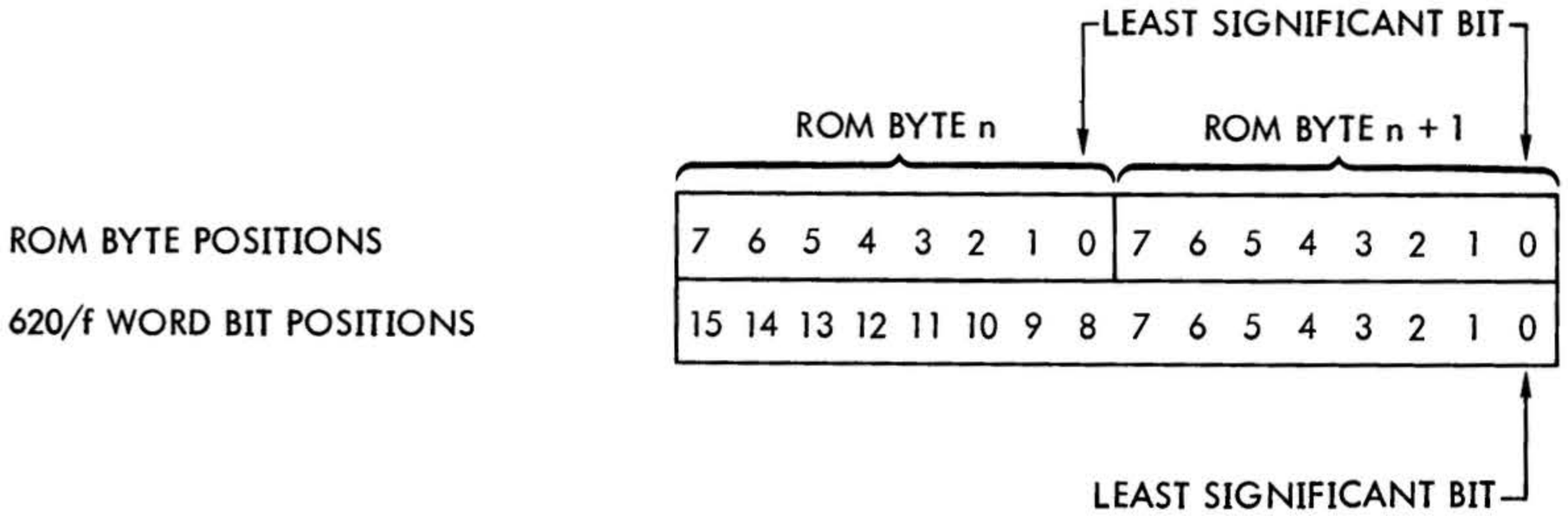

n = EVEN NUMBER (0,2,4,.....30)

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Figure 1-2. ABL ROM Byte/Computer Word Correspondence

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Table 1-2. ABL ROM Unit Byte Address/Computer Word Correspondence

ABL ROM Unit Byte Address	Computer Byte/Word		ABL ROM Unit Byte Address	Computer Byte/Word	
	Byte	Word		Byte	Word
0	1	1	16	17	9
1	2		17	18	
2	3	2	18	19	10
3	4		19	20	
4	5	3	20	21	11
5	6		21	22	
6	7	4	22	23	12
7	8		23	24	
8	9	5	24	25	13
9	10		25	26	
10	11	6	26	27	14
11	12		27	28	
12	13	7	28	29	15
13	14		29	30	
14	15	8	30	31	16
15	16		31	32	

1.2.8 AB Bus Drivers

This circuit is the interface between the ABL ROM outputs and the address counter memory trap address on one hand, and the 620/f AB bus on the other. The bootstrap loader timing and control logic (section 1.2.2) gates the ROM outputs and the trap address onto the AB bus so that the ROM data can be stored in the specified area of the 620/f core memory.

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INTRODUCTION

1.3 SPECIFICATIONS

The functional, physical, and electrical specifications of the ABL are given in table 1-3.

Table 1-3. Specifications of the ABL

Parameter	Description
Organization	BOOTSTRAP switch on the computer control panel, plus associated logic circuits. On the wired-socket card: bootstrap loader timing and control logic, register loading and CPU control logic, CPU control logic drivers and receivers, address counter, read-only memory (ROM) and associated logic, and AB bus drivers
Read-Only Memory	Specifically programmed to accommodate one type of input device. Depending on the input device, one or two ROM units, each accommodating 32 eight-bit bytes within a monolithic TTL 16-pin dual-in-line chip sinking a maximum of 12 mA
Input Devices	The ABL can accommodate only one type of input device. ABLs are presently available for the following: TTY, high-speed paper tape reader
Data Transfer	Sixteen-bit data word transfers from the ABL ROM to the computer core memory via the direct memory access (DMA) channel. Hardware insertion of instructions into CPU registers

Table 1-3. Specifications of the ABL *(continued)*

Parameter	Description
Logic Levels	Positive logic True: +2.5 to 5.0V dc False: 0.0 to +0.5V dc
Size	Twenty-four IC sockets on a 3-by-15-inch (7.7 x 38.1 cm) circuit card (If the system contains a TTY controller, it shares the card with the ABL.)
Interconnection	Plugs into 620/f CPU tray slot 13
Input Power	+5V dc ± 5 percent at 0.9 ampere maximum
Operational Environment	0 to 50 degrees C, 0 to 90 percent relative humidity without condensation

SECTION 2
INSTALLATION

It is recommended that Varian Data Machines customer service engineers install the ABL. Logic diagrams, assembly drawings, and wiring information are provided at the time of purchase.

2.1 PHYSICAL DESCRIPTION

The ABL occupies 24 socket positions on a 3-by-15-inch (7.7 x 38.1 cm) circuit card. If the system includes a TTY controller, it shares the card with the ABL. The part number of the ABL depends on the input device accommodated, and whether the card also holds a TTY controller. Table 2-1 gives the part numbers for the various combinations, and figure 2-1 shows the components on the card.

2.2 SYSTEM LAYOUT AND PLANNING

The ABL circuit card is located in slot 13 of the CPU tray. The card slots in this tray, which is mounted in the computer mainframe, are numbered 1 through 14 from rear to front as you face the 620/f control panel. Figure 2-2 shows the ABL mounted in the CPU tray.

Table 2-1. ABL Part Numbers

Input Device	TC*	ABL Part No.	Card Number	ABL ROM Unit 1**
Teletype	Yes	01P0951-000	44P0451-001	49A0113-000
	No	01P0951-001	44P0451-002	49A0113-000
Paper tape reader	Yes	01P0951-002	44P0451-001	49A0113-001
	No	01P0951-003	44P0451-002	49A0113-001

* TC = TTY controller. Yes in this column indicates that the ABL shares the card with a TC. No indicates that the ABL is alone on the card, i.e., there is no TC in the system.

** ABL ROM Unit 2 is not applicable.

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INSTALLATION

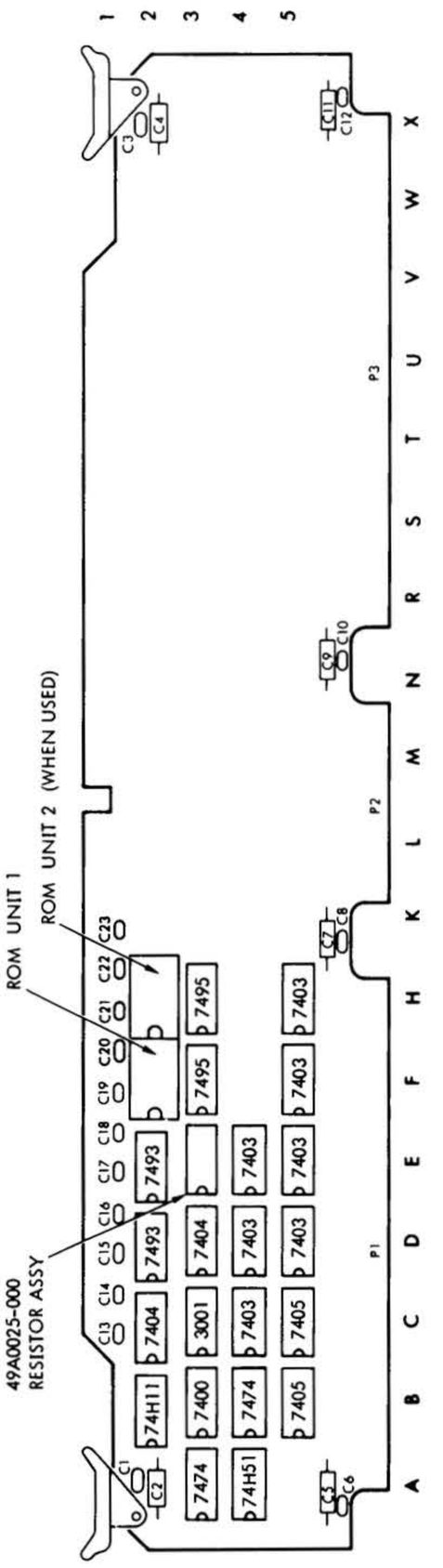

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Figure 2-1. ABL Component Layout Assembly

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INSTALLATION

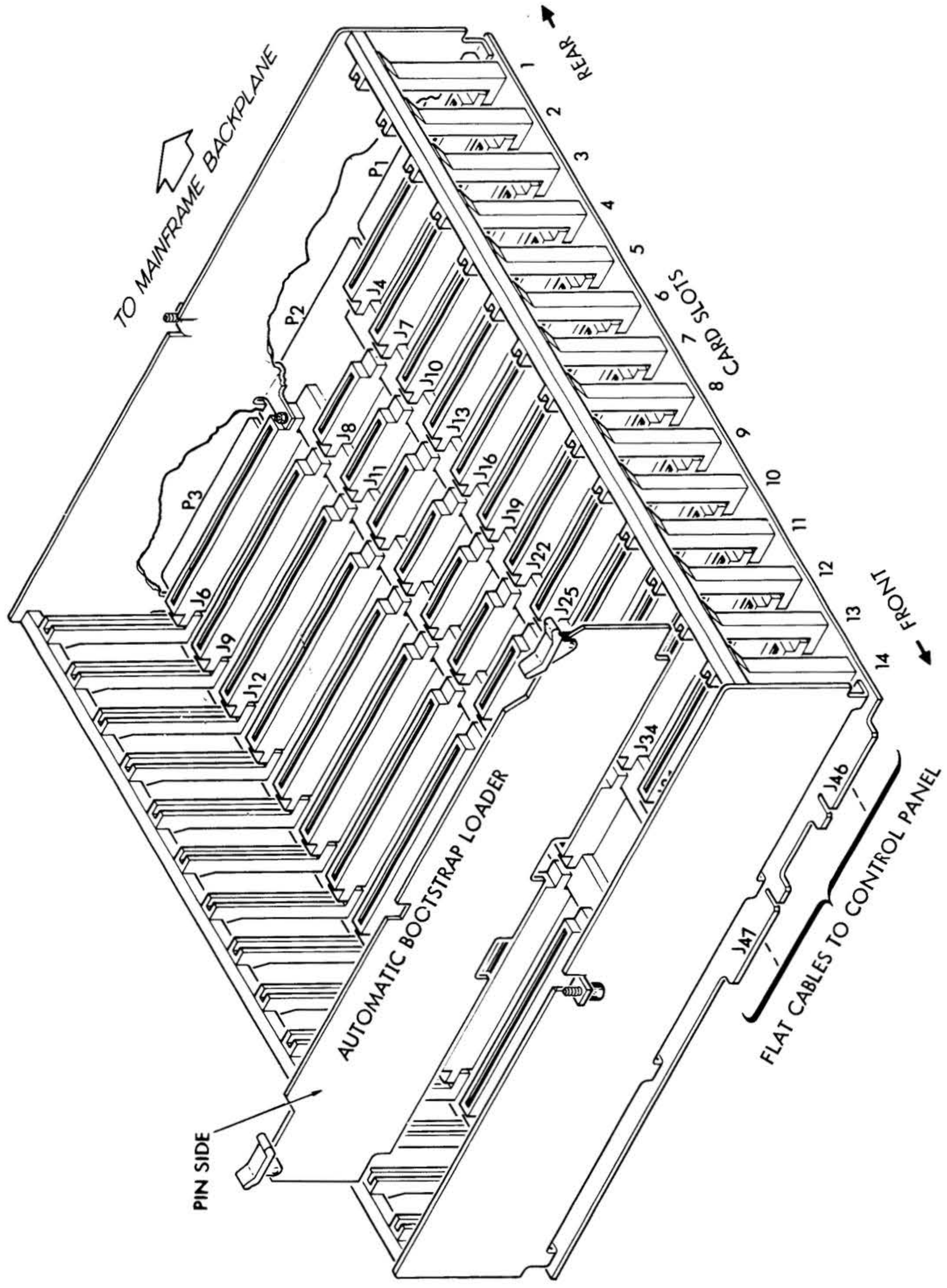

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Figure 2-2. ABL Card Location

SECTION 2
INSTALLATION

2.3 SYSTEM INTERCONNECTION

The ABL circuit card is inserted into slot 13 when the CPU tray is extended from the front of the computer mainframe and held by an extender assembly bolted to the front of the mainframe.

Insert the card into the mounting guides of slot 13 with the component side of the card toward the backplane connectors.

Apply moderate pressure to seat the card-edge connectors firmly into the mating connectors on the CPU tray. To prevent damage to the connectors or to the nylon guides, apply pressure evenly across the top of the card.

Insertion of the card also makes the required connections to the BOOTSTRAP switch on the computer control panel. No other manipulations are necessary.

The card has ejector handles for unseating it from its mating connectors. To remove the card, lift the inside edges of the ejector handles, then lift the card from the slot.

2.4 INTERFACE SIGNALS

The ABL interfaces with the CPU and with the DMA channel via control lines listed in table 2-2. A circuit card connector pin number follows each signal mnemonic. Refer to section 4 for definition of the mnemonics and explanation of the signal functions.

Table 2-2. ABL Interface Signals

Signal	Pin Number	Signal	Pin Number
ABL/CPU Interface Lines			
Input			
ABLE –	P1-25	ST1 –	P1-24
Output			
ABLST –	P1-9	BM11 –	P1-15
BM01 –	P1-7	OPECB –	P1-21
BM03 –	P1-8	OPTEI –	P1-20
BM07 –	P1-11	OPTEL –	P1-23
BM09 –	P1-13	OPTEP –	P1-21
BM10 –	P1-14	OPTEX –	P1-22
ABL/DMA Channel Interface Lines			
Input			
DRYX – C	P1-31	IUCX – C	P1-30
FRYX – C	P1-32	SYRT – C	P1-39
IUAX – C	P1-28		
Output			
TPIX – C	P1-37		
Bidirectional			
AB00 – C	P1-42	AB08 – C	P1-63
AB01 – C	P1-43	AB09 – C	P1-64
AB02 – C	P1-44	AB10 – C	P1-65
AB03 – C	P1-45	AB11 – C	P1-66
AB04 – C	P1-46	AB12 – C	P1-67
AB05 – C	P1-47	AB13 – C	P1-68
AB06 – C	P1-48	AB14 – C	P1-69
AB07 – C	P1-49	AB15 – C	P1-70

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OPERATION

The only control directly affecting the ABL is the momentary, spring-loaded BOOTSTRAP switch on the computer control panel. Pressing this switch loads the automatic bootstrap program into memory. However, the input device and CPU must first be prepared as directed below.

3.1 PREPARATION OF THE INPUT DEVICE

Prepare the input device accommodated by your ABL as directed in this section, referring also to the device manual.

3.1.1 Preparation of the Model 33B TTY

Position the binary load/dump (BLD II, appendix A) tape in the TTY reader with the first binary frame at the reading station.

Press RESET on the computer control panel.

Put the TTY reader control lever in the STOP position.

Put the TTY on-line.

3.1.2 Preparation of the Model 35B TTY

Put the TTY off-line.

Put the mode switch in position KT.

Press the following sequence of keys: CTRL, D, T, and Q.

Position the binary load/dump (BLD II, appendix A) tape in the TTY reader with the first binary frame at the reading station.

Press RESET on the computer control panel.

Put the TTY reader control lever in the STOP or LOAD position.

Put the TTY on-line.

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OPERATION

3.1.3 Preparation of the High-Speed Paper Tape Reader

Turn on the paper tape reader, ensuring that the LOAD/RUN switch is in the LOAD position.

Position the binary load/dump (BLD II, appendix A) tape in the reader with the first binary frame at the reading station.

Press RESET on the computer control panel.

Set the paper tape reader LOAD/RUN switch to RUN.

3.2 PREPARATION OF THE COMPUTER

Turn the computer on.

Put the STEP/RUN switch in the STEP position.

Then put the same switch in the RUN position.

Press and release the BOOTSTRAP switch, thus loading the bootstrap program.

If the BLD II program is being input from a TTY, set the TTY reader control lever to START or RUN.

The BLD II tape will now be read into memory automatically.

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THEORY OF OPERATION

Pressing the BOOTSTRAP switch on the computer control panel sends a starting pulse to the ABL. The ABL begins immediately to load the bootstrap program and to program the CPU registers. When this is completed, the ABL puts the CPU in run mode to execute the loaded program and then resets itself.

In the following description, ICs and components are located by their positions on the board, e.g., C3.

4.1 BOOTSTRAP SWITCH PULSE

This logic (figure 4-1) includes the BOOTSTRAP switch on the computer control panel and its connections to connector J1. Provided that the CPU is in step mode and the ABL is not busy executing a previous operation, actuating the spring-loaded BOOTSTRAP switch automatically loads the bootstrap program, using the ABL. (In systems not equipped with the ABL, the BOOTSTRAP switch is present on the computer control panel, but is not connected.)

When the switch is pressed, the connection between pins 1 and 3 produces ABLS – low, which sets a latch on CPU control card II in slot 10 (figure 4-2). The set latch produces ABLSE +, which is gated with a high ONSTP + to produce ABLE – to the ABL on card 13. ONSTP + results from the ABLSE – output of the latch being inverted to EONS + and

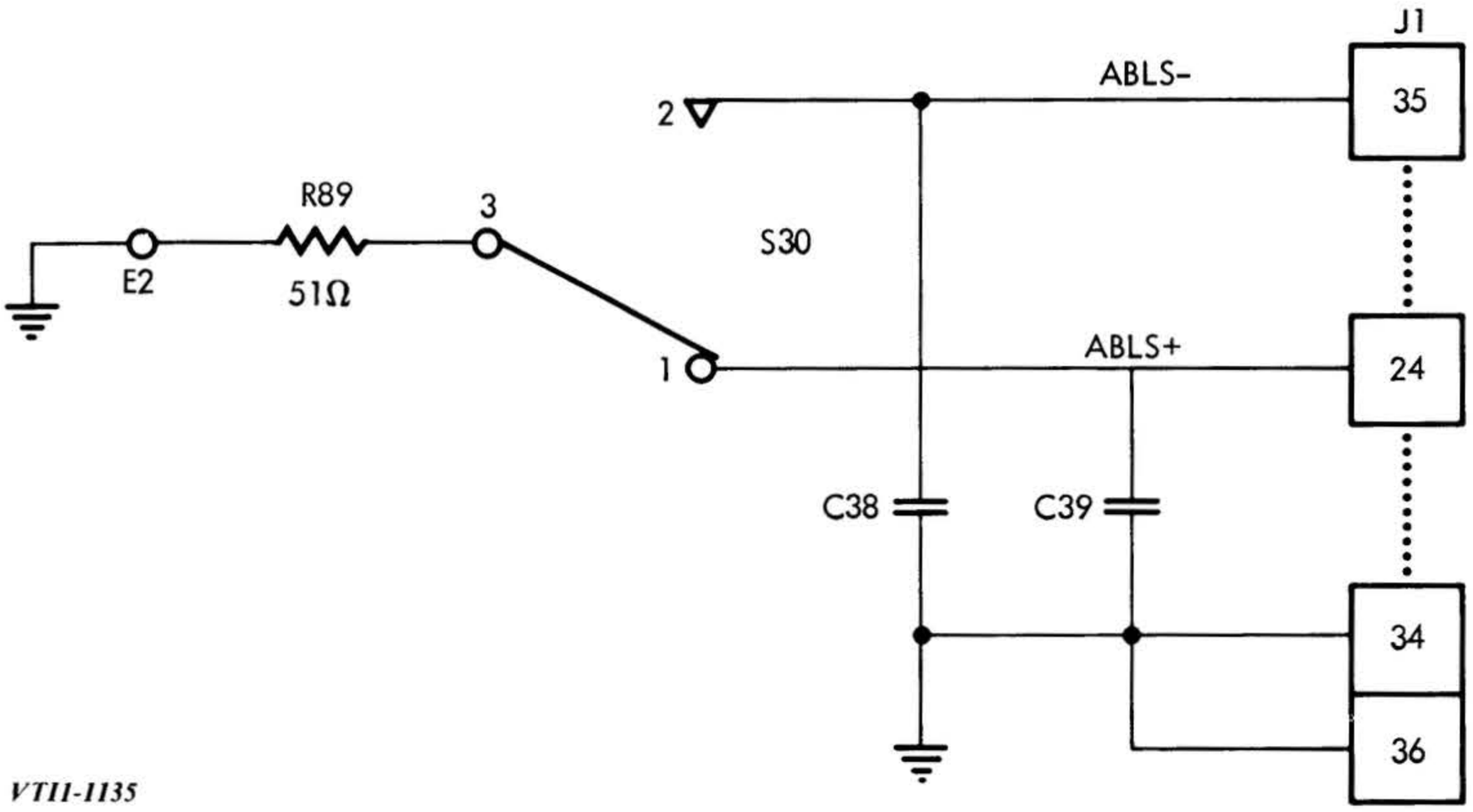

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Figure 4-1. BOOTSTRAP Switch

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THEORY OF OPERATION

input to the one-shot at C3. The width of the ONSTP+ pulse from this one-shot is 55 nanoseconds, as determined by the values of the components at C2.

ABLE– low initiates the loading of the bootstrap program by the ABL. The logic diagrams of the ABL on card 13 given in section 6 of this manual aid in understanding the following sequences.

4.2 AUTOMATIC BOOTSTRAP LOADER CONTROL SEQUENCES

The *bootstrap loading sequence (BLS)* starts with the ABLE– pulse from the BOOTSTRAP switch (section 4.1), and ends with the address counter having reached 64.

The *CPU register programming sequence (RPS)* runs parallel with the BLS.

The *CPU start/run sequence (SRS)* starts where the BLS and RPS terminate. The SRS puts the computer in run mode and resets the ABL, thus terminating the ABL hardware operation.

Figure 4-3 shows the relationships of the ABL sequences to each other, and figure 4-4 shows the correspondence of states in the CPU to those in the ABL during ABL operations. Figures 4-5 and 4-6 are the timing diagrams of the ABL sequences.

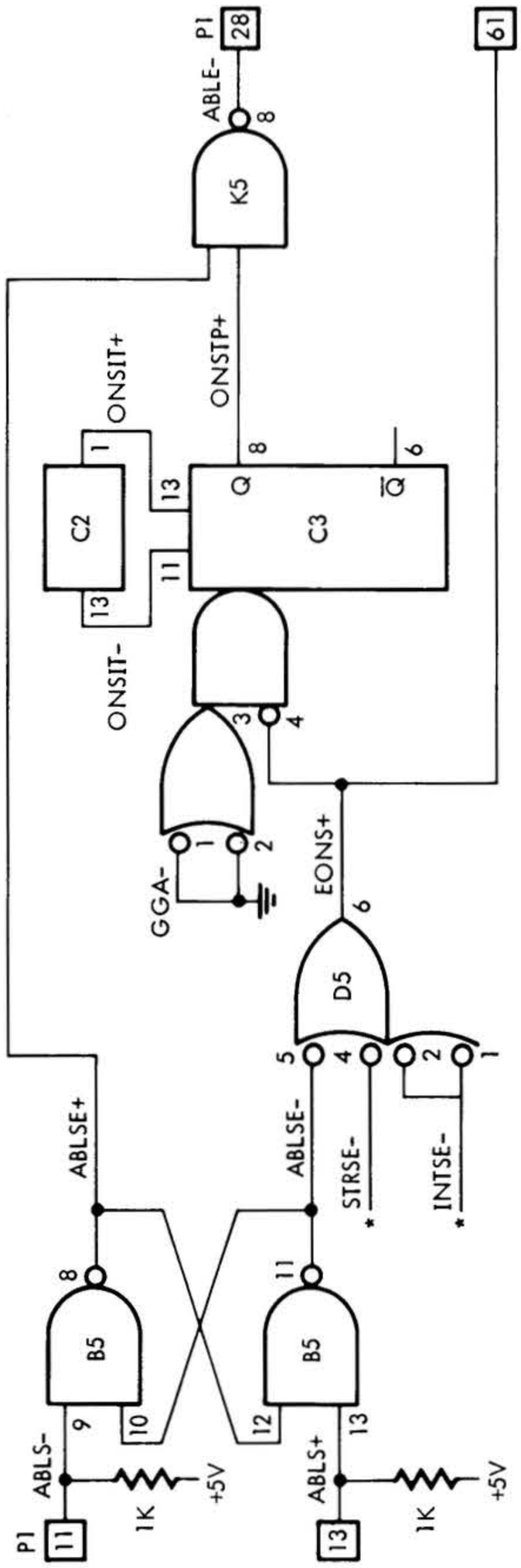

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Figure 4-2. CPU Control Board II Portion of ABL Logic

SECTION 4
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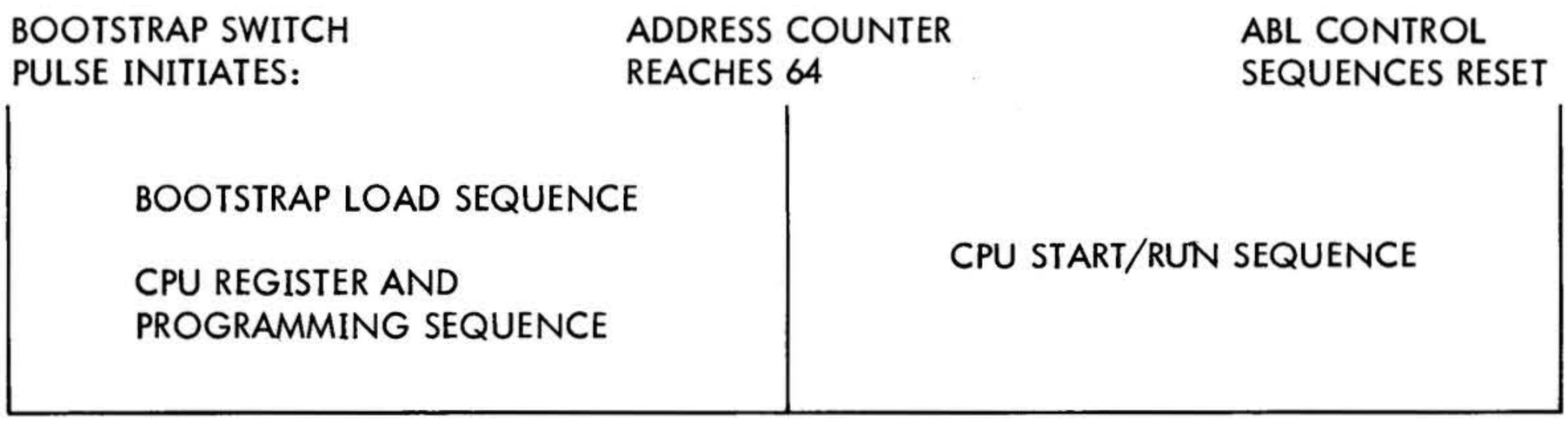

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Figure 4-3. ABL Control Sequences

4.2.1 Bootstrap Loading Sequence (BLS)

The BLS transfers the bootstrap program from the ABL ROM to the computer core memory via the DMA port. During the BLS, the address counter increments 64 times and the sequence terminates when the counter reaches this value (01000000). The counter increments twice for each data-word transfer to memory, thus providing for the assembly of the ROM bytes into computer words.

Thus, to obtain the correct ROM address and memory address, the least significant five bits of the address counter are used for the ROM address, while the memory address is determined by bits 2, 4, 8, 16, and 32. Table 4-1 shows the correspondence of address counter values to data outputs.

ABL ROM unit 1 is enabled while the value of the address counter is 0 to 31, and is then disabled. ABL ROM unit 2, if present, is enabled while the value of the address counter is 32 to 63, but is otherwise disabled. Note that the corresponding pins of each ROM unit are tied together, e.g., AD1 + enters both units at pin 10, and MO1 + leaves each ROM unit at pin 1. If ABL ROM unit 2 is not present, the value loaded into core memory will be 0177777 for each location indicated by the address counter while it has values between 32 and 63.

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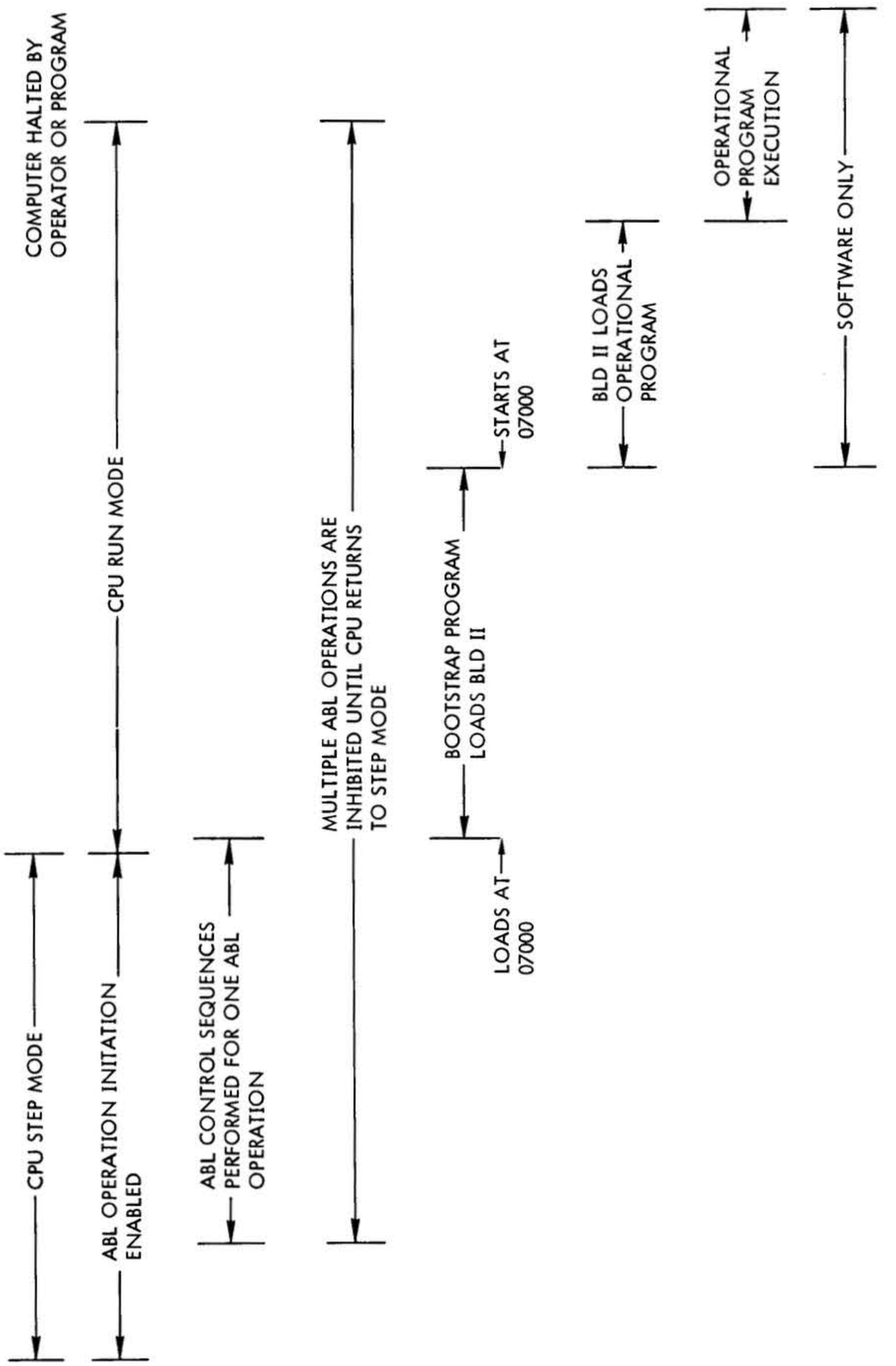

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Figure 4-4. ABL Operation and Computer States

SECTION 4
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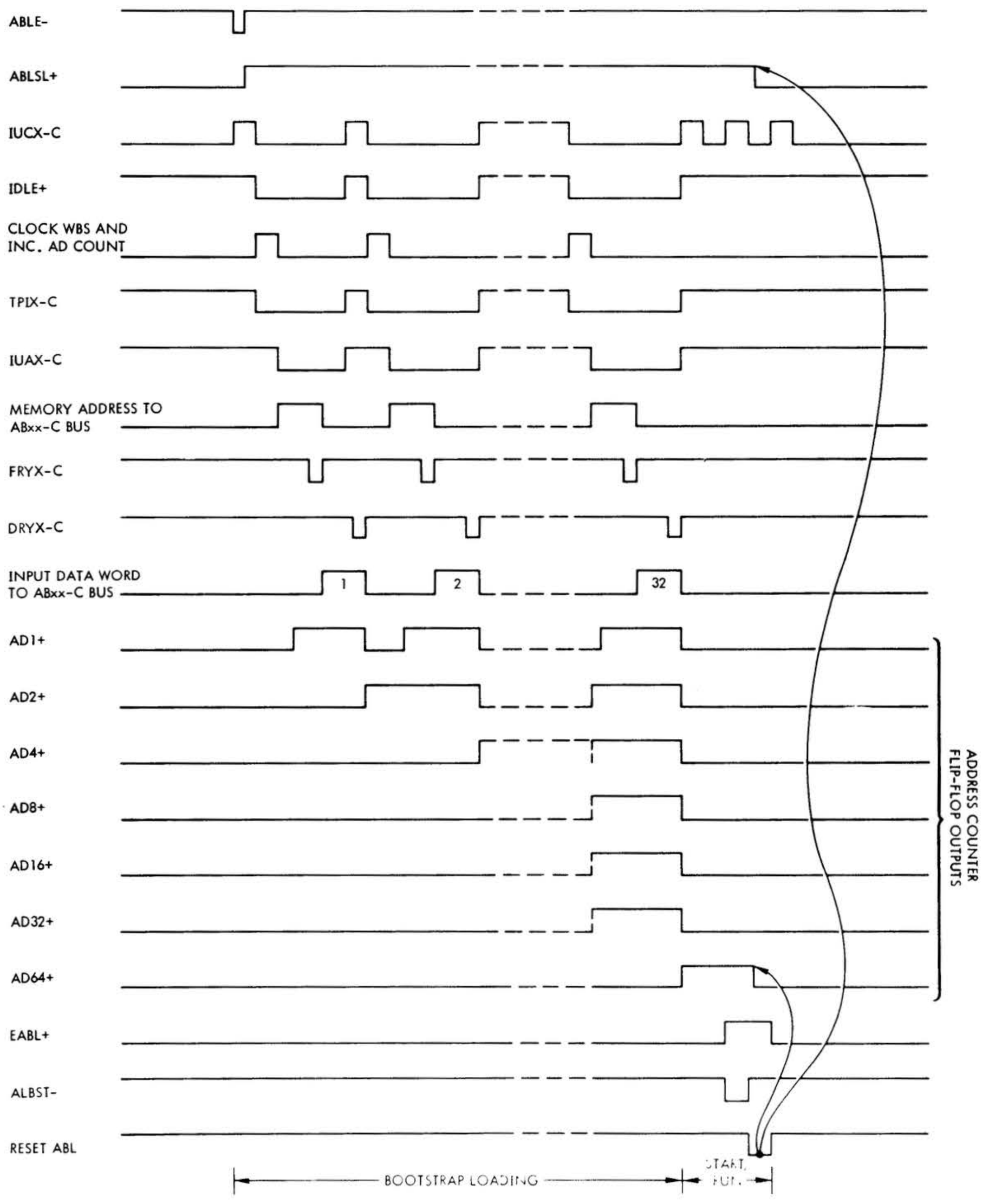

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Figure 4-5. Bootstrap Loading and Start/Run Sequence Timing

SECTION 4
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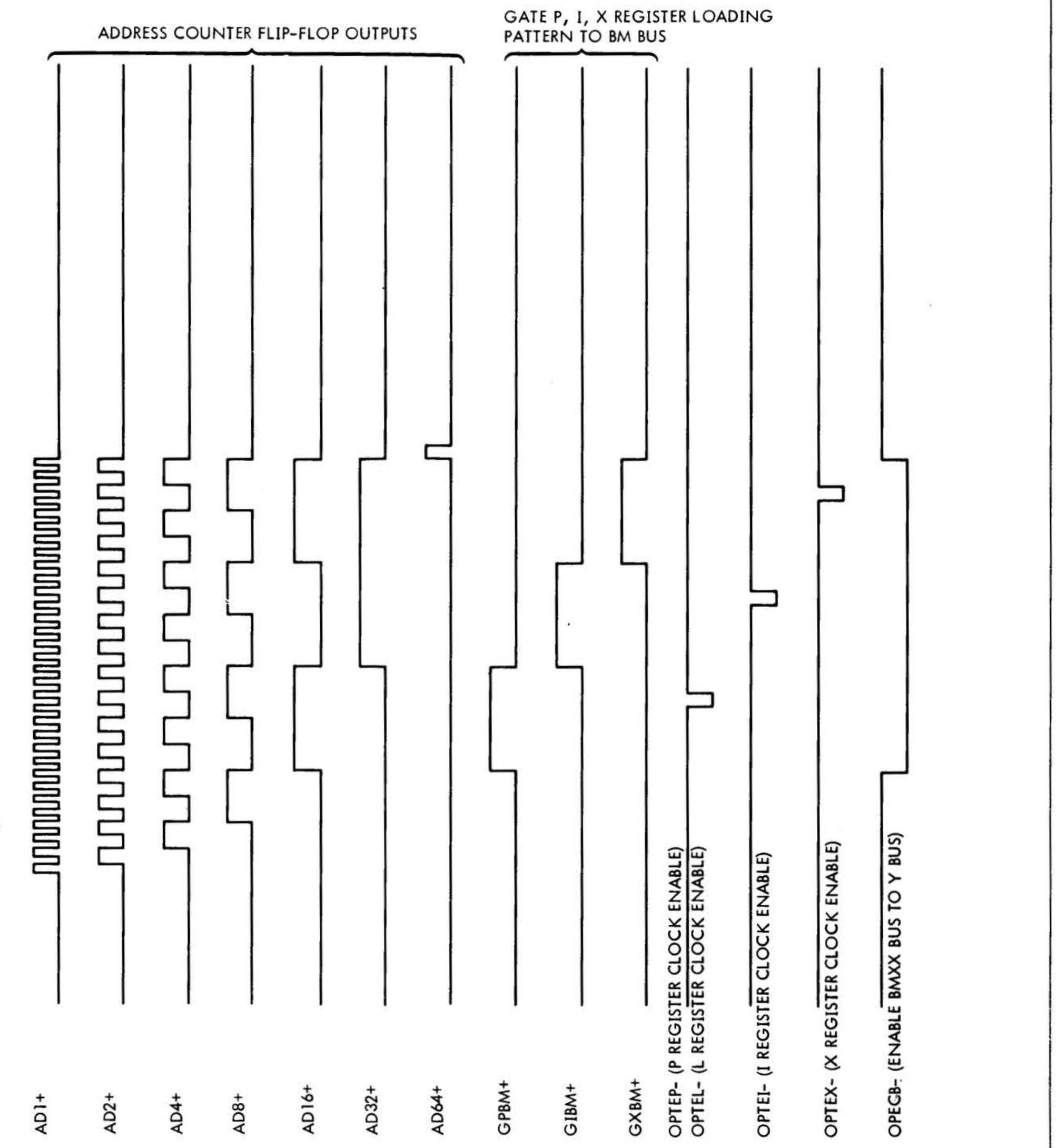

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Figure 4-6. CPU Register Programming Sequence Timing

Table 4-1. Bootstrap Loading Sequence: Address Versus Data Outputs

Address Counter Truth Table Outputs							ROM Unit 1	ROM Unit 2			
64	32	16	8	4	2	1	Byte	Byte	Data Word to Memory	ROM Unit 1	ROM Unit 2
0	0	0	0	0	0	0	1	---	---	↑	↑
0	0	0	0	0	0	1	2	---	1		
0	0	0	0	0	1	0	3	---	---		
0	0	0	0	0	1	1	4	---	2		
•	•	•	•	•	•	•	•		•	Enabled	Disabled
•	•	•	•	•	•	•	•	---	•		
•	•	•	•	•	•	•	•		•		
0	0	1	1	1	1	0	31	---	---		
0	0	1	1	1	1	1	32	---	16	↓	↓
0	1	0	0	0	0	0	---	1	---	↑	↑
0	1	0	0	0	0	1	---	2	17		
•	•	•	•	•	•	•	•		•		
•	•	•	•	•	•	•	•	---	•		
•	•	•	•	•	•	•	•		•	Disabled	Enabled
0	1	1	1	1	0	0	---	29	---		
0	1	1	1	1	0	1	---	30	31		
0	1	1	1	1	1	0	---	31	---		
0	1	1	1	1	1	1	---	32	32		
1	0	0	0	0	0	0	---	---	---	↓	↓

ROM Address
Memory Address
Initiates Start/Run Sequence

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Initially, the address counter is zero and all control flip-flops are reset. When the computer is in step mode (producing ST1 – inverted to ST1 +) and the ABLE – pulse is received by the ABL, the BLS starts. The transition at the end of the 55-nanosecond ABLE – pulse outputs ABLSL + high from flip-flop B4. ABLSL + remains high throughout the BLS and goes low only when the direct reset (RES1 –) is activated by SYRT – C and ENRS – high in the SRS (section 4.2.2).

At the start of the BLS, AD64 – and EABI – are both high, thus converting ABLSL + to STABL + at B2. STABL + goes to the bootstrap loading sequencer (components A3 and A4) to initiate the word-loading process. The word-loading process consists of 32 identical passes. The first pass starts with the address counter at 0. Since the counter increments twice for each pass, all passes start with even addresses.

One pass of the word-loading process proceeds as follows: The IUCX – C from the CPU/DMA interrupt clock is inverted to IUCX + and reinverted to IUCX – , in which form it is gated with STABL + in the sequencer at A4. This is ORed with FRYX + (inverted from FRYX – C), producing CLBS2 – , whose leading edge outputs LBS2 + high from the sequencer.

LBS2 + high and high LBS1 – from the sequencer produce LBS02 – , and thus ADCS + high input to the address counter. This strobes an ROM byte into the word assembly buffer. Address decoding is internal to the ROM.

Simultaneously, the other output of the bootstrap loading sequencer, LBS2 – low, produces TPIX + high and thence TPIX – C low, a trap-in request to the CPU DMA.

When the interrupt acknowledgment IUAX – C is received from the CPU DMA, the sequencer flip-flop outputs reverse with a delay on this transition for the LBS2 flip-flop for the enabling clock input IUCX + . TPIX – C goes high at the same time as IUAX – C. LBS1 – low from the sequencer causes the prewired sector address bits and bits 2, 4, 8, 16, and 32 of the address counter to be gated onto the AB bus (signals ABxx – C) as the memory address. The address counter increments once at this time.

When the CPU DMA transmits FRYX – C, the gated memory address is removed from the AB bus, and the outputs of both the ROM and the word assembly buffer are gated onto it. The ROM outputs form AB bus signals AB00 – C through AB07 – C, while the word assembly buffer outputs AB08 – C through AB15 – C. When the data word is stored in core memory, the CPU DMA sends DRYX – C low to the ABL. The sequencer again reverses, TPIX – C goes high, and the data are removed from the AB bus. The address counter increments a second time to complete one pass of the BLS.

The sequencer is again in the initial state, and the address counter contains a count two higher than that of the initial state for this pass. After 32 passes, the address counter contains 64 (01000000). AD64 + goes high, completing the BLS.

4.2.2 CPU Register Programming Sequence (RPS)

The RPS runs parallel with the BLS. Figure 4-6 is the timing diagram for the RPS.

The RPS loads the CPU registers with the data needed to execute the bootstrap program. First, the RPS loads the program (P) and memory address (L) registers with the entry address of the bootstrap program. It then loads the instruction (I) register with the operation code for a No Operation (NOP) instruction, enabling the computer to enter the program execution cycle. Finally, the RPS loads the index (X) register with the memory address of the beginning of the binary loader (BLD II).

Address counter outputs AD8 + high, AD4 + low (then inverted to AD4 – high), and AD2 + high produce strobe SPIX + high. The address counter outputs AD16 + and AD32 + are gated with this strobe to produce the gate signals for the P, I, and X registers, GPBM +, GIBM +, and GXBM +. These are then gated with SPIX + to output the transfer enabling signals to the registers, OPTEP –, OPTEI –, and OPTEX –. The L register enabling signal OPTEL – is produced from GPBM + and SPIX + in the same way as OPTEP – since the L and P registers are loaded with the same information.

The timing diagram makes the enabling sequence clear. When AD16 + first goes high (AD32 + is low), GPBM + goes high. On the next negative transition of AD4 +, there is an SPIX + strobe that produces OPTEP – low and OPTEL – low pulses, enabling the loading of the P and L registers with the bootstrap program entry address. This address is 000212, entered by the BM bus bits BM07 –, BM03 –, and BM01 – that are hard-wired to and inverted from GPBM +.

SECTION 4
THEORY OF OPERATION

When AD16+ then goes low (and AD32+ first goes high), GIBM+ goes high. On the next negative transition of AD4+, there is an SPIX+ strobe that produces the OPTEI− low pulse, enabling the loading of the I register with the NOP code. This code is 005000, entered by the BM bus bits BM09− and BM11− that are hard-wired to and inverted from GIBM+.

When AD16+ again goes high (AD32+ remains high), GXBM+ goes high. On the next negative transition of AD4+, there is an SPIX+ strobe that produces the OPTEX− low pulse, enabling the loading of the X register with the memory address of the beginning of the BLD II program. This address is 007000, entered by the BM bus bits BM09−, BM10−, and BM11− that are hard-wired to and inverted from GXBM+.

When AD16+ next goes low, AD32+ also goes low, and AD64+ goes high, terminating the RPS.

On each of the above transitions of AD16+, the previous high gating signal goes low as the new gating signal goes high. OPECB− which enables the transmission of BMxx− to the ABL BM bus and thence to the CPU AY bus, goes low when GPBM+ goes high (first AD16+ transition), and remains low until GXBM+ goes low (last AD16+ transition) and AD64+ goes high. Thus transmission of data on the ABL BM bus in enabled throughout the time when register loading patterns are active. The data are transmitted to the required register via the CPU adder according to the active transfer enabling signal GPBM+, GIBM+, or GXBM+. The actual data sent with each of these enabling steps depend on the bits of the BM bus that are hard-wired to these signals.

4.2.3 CPU Start/Run Sequence (SRS)

The SRS begins when AD64+ goes high, i.e., at the end of the BLS and RPS. The registers are now loaded and the ROM has been read out. The high AD64+ shows that the ABL address counter has incremented through its capacity and is now at the point of "overflow". AD64+ sets the end-ABL flip-flop on the leading edge of the next IUCX−C clock pulse following that when AD64+ went high. This flip-flop produces EABL+ high, which in turn produces ABLST− low, which puts the CPU in the RUN state. EABL+ also produces the ABL reset signal ENRS− that inputs RES1− to the direct reset of the ABL enabling flip-flop at B4. This restores the ABL to its initial state.

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THEORY OF OPERATION

4.3 MNEMONICS

The mnemonics used in the ABL (card 13) are listed alphabetically in table 4-2, with the source and definition. The source indicates the sheet number of the logic diagram (section 6) followed by the location of the IC or component, or by the pin number where the signal enters ABL card 13; e.g., ABLSL originates at IC location B4 as shown on logic diagram page 2, and ABLE enters the ABL at pin 25 of connector P1 as shown on the same page.

Following the general mnemonics list is a list of mnemonics affecting the ABL but not originating or appearing on the ABL card in slot 13 of the CPU tray. Signals designated as being shown in figure 4-2 appear in that figure, which is the logic diagram of the portion of CPU control board II (slot 10) concerning the ABL. Signals designated as being shown in figure 4-1 appear in that figure, a wiring diagram of the BOOTSTRAP switch on the computer control panel.

Table 4-2. Mnemonic Definitions

Mnemonic	Source	Definition
ABLE	2 P1-25	ABL enabler from CPU control II
ABLSL	2 B4	ABL selected
ABLST	2 C4	ABL start
AB00 – C to AB15 – C	3 D4, D5 E4, E5, F5, H5	CPU AB bus gating
ADCS	3 B3	Address counter strobe
AD1,2,4, 8,16,32,64	3 D2, E2	Address counter outputs
BMC +	3 H3, F3	Buffer mode control
BM01,03,07 09,10,11 –	2 B5, C5	ABL BM bus outputs to CPU AY bus
CLBS1, CLBS2	2 A4	Bootstrap loading sequencer clocks

Table 4-2. Mnemonic Definitions *(continued)*

Mnemonic	Source	Definition
DRYX – C	2 P1-31	Data ready signal from CPU/DMA
EABL	2 B4	End ABL
ENRS	2 D4	End reset
FRYX – C	2 P1-32	Function ready signal from CPU/DMA
GIBM	2 C3	Gate instruction to ABL BM bus
GPBM	2 B2	Gate program to ABL BM bus
GXBM	2 C3	Gate index to ABL BM bus
IUAX – C	2 P1-28	Interrupt acknowledgment from CPU/DMA
IUCX – C	2 P1-30	Interrupt clock from CPU/DMA
LBS01 to LBS03	3 B3	Decoded bootstrap loading sequencer outputs
LBS1, LBS2	2 A3	Bootstrap loading sequencer flip-flop outputs
LBS1 + A	3 D3	Inversion of LBS01 to less significant byte of the AB bus gating
LBS1 + B	3 D3	Inversion of LBS01 to more significant byte of the AB bus gating
MO1 to MO8	3 F2, H2	ROM outputs
OPCEB	2 C5	Option enabled to C bus (via BM and AY buses through the CPU arithmetic unit
OPTEI	2 C4	Option transfer enabled to I register

Table 4-2. Mnemonic Definitions *(continued)*

Mnemonic	Source	Definition
OPTEL	2 D4	Option transfer enabled to L register
OPTEP	2 C4	Option transfer enabled to P register
OPTEX	2 C4	Option transfer enabled to X register
RES1	2 C3	Reset ABL
SPIX	2 B2	Strobe P (L), I, and X registers
STABL	2 B2	Start ABL
ST1	2 P1-24	State 1 (CPU in step mode) input
SYRT – C	2 P1-39	System reset input
TPIX	2 B3	Trap-in request
TPIX – C	2 C5	ABL trap-in request output signal
WSB1 to WSB8	3 F3, H3	Word assembly buffer outputs
ABL Signals on CPU Control Panel or Control Card II		
ABLE	4-2 K5	ABL enabler
ABLS	4-1 S30	ABL control panel switch
ABLSE	4-2 B5	ABL switch latch outputs
EONS	4-2 D5	Enable one-shot
GGA	4-2 C3	Ground
INTSE	4-2 *	Interrupt switch enabler
ONSIT	4-2 C2, C3	One-shot internal timing

SECTION 4
THEORY OF OPERATION

Table 4-2. Mnemonic Definitions *(continued)*

Mnemonic	Source	Definition
ONSTP	4-2 C3	One-shot start pulse
STRSE	4-2 *	Start switch enabler

* Source is elsewhere in the CPU logic

SECTION 5
MAINTENANCE

ABL maintenance consists of running the tests described below, troubleshooting any errors detected, and making repairs as necessary. Error isolation is aided by familiarization with the ABL operation and by use of the logic diagram (section 6). The 620/f maintenance manual (document number 98 A 9908 050) provides system information useful in ABL maintenance.

5.1 EQUIPMENT

The following is a list of recommended test equipment and tools for maintaining the ABL.

a. Oscilloscope, Tektronix type 547

b. Multimeter, Triplett type 630

c. DM265 extender card, part number 44P0437

d. CPU extender cables

e. Card puller, Titchener type 1731

5.2 TESTING THE AUTOMATIC BOOTSTRAP LOADER

Perform the following tests using the ROM required by the system, and the corresponding I/O device. If more than one ABL ROM is to be used in the system or shipped with the ABL, repeat the tests for each ROM and the corresponding I/O device.

SECTION 5
MAINTENANCE

5.2.1 Bootstrap Loader Program Test

Load the AID II program (see 620/f Handbook) at address 0X6000. *

Install the required ROM in the ABL, attaching the latter to the CPU with an extender board and cables (refer to the 620/f Maintenance Manual). Connect the corresponding I/O device to the system.

Set the STEP/RUN switch on the computer control panel to STEP.

Press the REPEAT switch on the computer control panel.

Press the RESET switch on the computer control panel.

Press the BOOTSTRAP switch on the computer control panel. The CPU should remain in step mode with its registers set as follows:

a. Program (P) register: 000214

b. Index (X) register: 007000

c. Instruction (I) register: 005000

Using AID II, cause a printout of the bootstrap program just loaded by the ABL and compare it with the correct listing. Tables 5-1 and 5-2 are listings of ABL programs for the TTY and high-speed paper tape reader, respectively. Tables 5-3 and 5-4 are the corresponding ROM truth tables.

* X =	Memory Module
0	4K
1	8K
2	12K
3	16K
4	20K
5	24K
6	28K
7	32K

Table 5-1. TTY Memory Listing

Address	Octal Configuration	Symbolic Coding		
000200	102601	READ	CIB	
000201	004011		ASLB	NBIT – 7
000202	004041		LRLB	1
000203	004446		LLRL	6
000204	001020		JBZ	SEL
000205	000214			
000206	055000		STA	0, 1
000207	001010		JAZ	LHLT + 1
000210	007000			
000211	005144		IXR	
→ 000212	005101	ENTR	INCR	1
000213	102601	SEL	CIB	
000214	101201		SEN	READ
000215	000200			
000216	001000		JMP	* – 2
000217	000214			

Table 5-2. High-Speed Paper Tape Reader Memory Listing

Address	Octal Configuration	Symbolic Coding		
000200	102637	READ	CIB	
000201	004011		ASLB	NBIT – 7
000202	004041		LRLB	1
000203	004446		LLRL	6
000204	001020		JBZ	SEL
000205	000214			
000206	055000		STA	0, 1
000207	001010		JAZ	LHLT + 1
000210	007000			
000211	005144		IXR	
000212	005101	ENTR	INCR	1
000213	100537	SEL	EXC	
000214	101537		SEN	READ
000215	000200			
000216	001000		JMP	* – 2
000217	000214			

Table 5-3. TTY ROM Truth Table

Binary Input Address						MSB Outputs							LSB	Computer	
E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Byte	Word
0	0	0	0	0	0	1	0	0	0	0	1	0	1	1	1
0	0	0	0	1	0	1	0	0	0	0	0	0	1	2	
0	0	0	1	0	0	0	0	0	0	1	0	0	0	3	2
0	0	0	1	1	0	0	0	0	0	1	0	0	1	4	
0	0	1	0	0	0	0	0	0	0	1	0	0	0	5	3
0	0	1	0	1	0	0	0	1	0	0	0	0	1	6	
0	0	1	1	0	0	0	0	0	0	1	0	0	1	7	4
0	0	1	1	1	0	0	0	1	0	0	1	1	0	8	
0	1	0	0	0	0	0	0	0	0	0	0	1	0	9	5
0	1	0	0	1	0	0	0	0	1	0	0	0	0	10	
0	1	0	1	0	0	0	0	0	0	0	0	0	0	11	6
0	1	0	1	1	0	1	0	0	0	1	1	0	0	12	
0	1	1	0	0	0	0	1	0	1	1	0	1	0	13	7
0	1	1	0	1	0	0	0	0	0	0	0	0	0	14	
0	1	1	1	0	0	0	0	0	0	0	0	1	0	15	8
0	1	1	1	1	0	0	0	0	0	1	0	0	0	16	
1	0	0	0	0	0	0	0	0	0	1	1	1	0	17	9
1	0	0	0	1	0	0	0	0	0	0	0	0	0	18	
1	0	0	1	0	0	0	0	0	0	1	0	1	0	19	10
1	0	0	1	1	0	0	1	1	0	0	1	0	0	20	

Table 5-3. TTY ROM Truth Table *(continued)*

Binary Input Address						MSB Outputs							LSB	Computer	
E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Byte	Word
1	0	1	0	0	0	0	0	0	0	1	0	1	0	21	11
1	0	1	0	1	0	0	1	0	0	0	0	0	1	22	
1	0	1	1	0	0	1	0	0	0	0	1	0	1	23	12
1	0	1	1	1	0	1	0	0	0	0	0	0	1	24	
1	1	0	0	0	0	1	0	0	0	0	0	1	0	25	13
1	1	0	0	1	0	1	0	0	0	0	0	0	1	26	
1	1	0	1	0	0	0	0	0	0	0	0	0	0	27	14
1	1	0	1	1	0	1	0	0	0	0	0	0	0	28	
1	1	1	0	0	0	0	0	0	0	0	0	1	0	29	15
1	1	1	0	1	0	0	0	0	0	0	0	0	0	30	
1	1	1	1	0	0	0	0	0	0	0	0	0	0	31	16
1	1	1	1	1	0	1	0	0	0	1	1	0	0	32	
x	x	x	x	x	1	1	1	1	1	1	1	1	1		

NOTES:
1. One denotes a high voltage out.
2. Zero denotes a low voltage out.
3. x denotes the condition is irrelevant.

Table 5-4. High-Speed Paper Tape Reader ROM Truth Table

Binary Input Address						MSB Outputs							LSB	Computer	
E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Byte	Word
0	0	0	0	0	0	1	0	0	0	0	1	0	1	1	1
0	0	0	0	1	0	1	0	0	1	1	1	1	1	2	
0	0	0	1	0	0	0	0	0	0	1	0	0	0	3	2
0	0	0	1	1	0	0	0	0	0	1	0	0	1	4	
0	0	1	0	0	0	0	0	0	0	1	0	0	0	5	3
0	0	1	0	1	0	0	0	1	0	0	0	0	1	6	
0	0	1	1	0	0	0	0	0	0	1	0	0	1	7	4
0	0	1	1	1	0	0	0	1	0	0	1	1	0	8	
0	1	0	0	0	0	0	0	0	0	0	0	1	0	9	5
0	1	0	0	1	0	0	0	0	1	0	0	0	0	10	
0	1	0	1	0	0	0	0	0	0	0	0	0	0	11	6
0	1	0	1	1	0	1	0	0	0	1	1	0	0	12	
0	1	1	0	0	0	0	1	0	1	1	0	1	0	13	7
0	1	1	0	1	0	0	0	0	0	0	0	0	0	14	
0	1	1	1	0	0	0	0	0	0	0	0	1	0	15	8
0	1	1	1	1	0	0	0	0	0	1	0	0	0	16	
1	0	0	0	0	0	0	0	0	0	1	1	1	0	17	9
1	0	0	0	1	0	0	0	0	0	0	0	0	0	18	
1	0	0	1	0	0	0	0	0	0	1	0	1	0	19	10
1	0	0	1	1	0	0	1	1	0	0	1	0	0	20	

Table 5-4. High-Speed Paper Tape Reader ROM Truth Table *(continued)*

Binary Input Address						MSB			Outputs				LSB	Computer	
E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Byte	Word
1	0	1	0	0	0	0	0	0	0	1	0	1	0	21	11
1	0	1	0	1	0	0	1	0	0	0	0	0	1	22	
1	0	1	1	0	0	1	0	0	0	0	0	0	1	23	12
1	0	1	1	1	0	0	1	0	1	1	1	1	1	24	
1	1	0	0	0	0	1	0	0	0	0	0	1	1	25	13
1	1	0	0	1	0	0	1	0	1	1	1	1	1	26	
1	1	0	1	0	0	0	0	0	0	0	0	0	0	27	14
1	1	0	1	1	0	1	0	0	0	0	0	0	0	28	
1	1	1	0	0	0	0	0	0	0	0	0	1	0	29	15
1	1	1	0	1	0	0	0	0	0	0	0	0	0	30	
1	1	1	1	0	0	0	0	0	0	0	0	0	0	31	16
1	1	1	1	1	0	1	0	0	0	1	1	0	0	32	
x	x	x	x	x	1	1	1	1	1	1	1	1	1		

NOTES:
1. One denotes a high voltage out.
2. Zero denotes a low voltage out.
3. x denotes the condition is irrelevant.

5.2.2 Final Performance Test

Lcad the computer core memory with zeros as follows:

a. Clear the A register.

b. Enter 054000 in the instruction (I) register.

c. Enter 000000 in the program (P) register.

d. Press the REPEAT switch on the computer control panel.

e. Set the STEP/RUN switch on the computer control panel to RUN.

f. Press the START switch on the computer control panel.

The computer should now enter run mode and clear memory.

Load the BLD II program (appendix A) for the I/O device used by the ABL.

Using BLD II, load AID II and verify that this loading is correct. A correct loading indicates that the ABL is free of faults.

5.3 REFERENCE DOCUMENTS

In addition to this manual, the documents listed below are useful aids to understanding and maintaining the ABL.

a. 620/f Reference Handbook (98 A 9908 001)

b. 620/f Maintenance Manual (98 A 9908 050)

c. 620 Test Programs Manual (98 A 9908 960)

d. ABL Top Assembly Drawing (01A0951)

e. ABL Logic Diagram (91C0261)

f. ABL Wire List (95W0723)

g. ABL Board Assembly Drawing (44D0451)

SECTION 6
DRAWINGS AND PARTS LISTS

This section contains the logic diagram and parts information for the ABL. For the BOOTSTRAP switch on the computer control panel, refer to figure 4-1. Figure 4-2 is the logic diagram of that portion of CPU control card II (slot 10) directly affecting the ABL.

REVISIONS				
SYM	ZONE	DESCRIPTION	APPROVED	DATE
A		PRODUCTION RELEASE PER EN 5151		1/11/71

NOTES: (UNLESS OTHERWISE SPECIFIED)

REFERENCE DESIGNATIONS	
LAST USED	NOT USED

REFERENCE DRAWINGS	
44D0451	ASSEMBLY
44P0451	PARTS LIST
95W0723	WIRE LIST
40D0458	P.W. BOARD

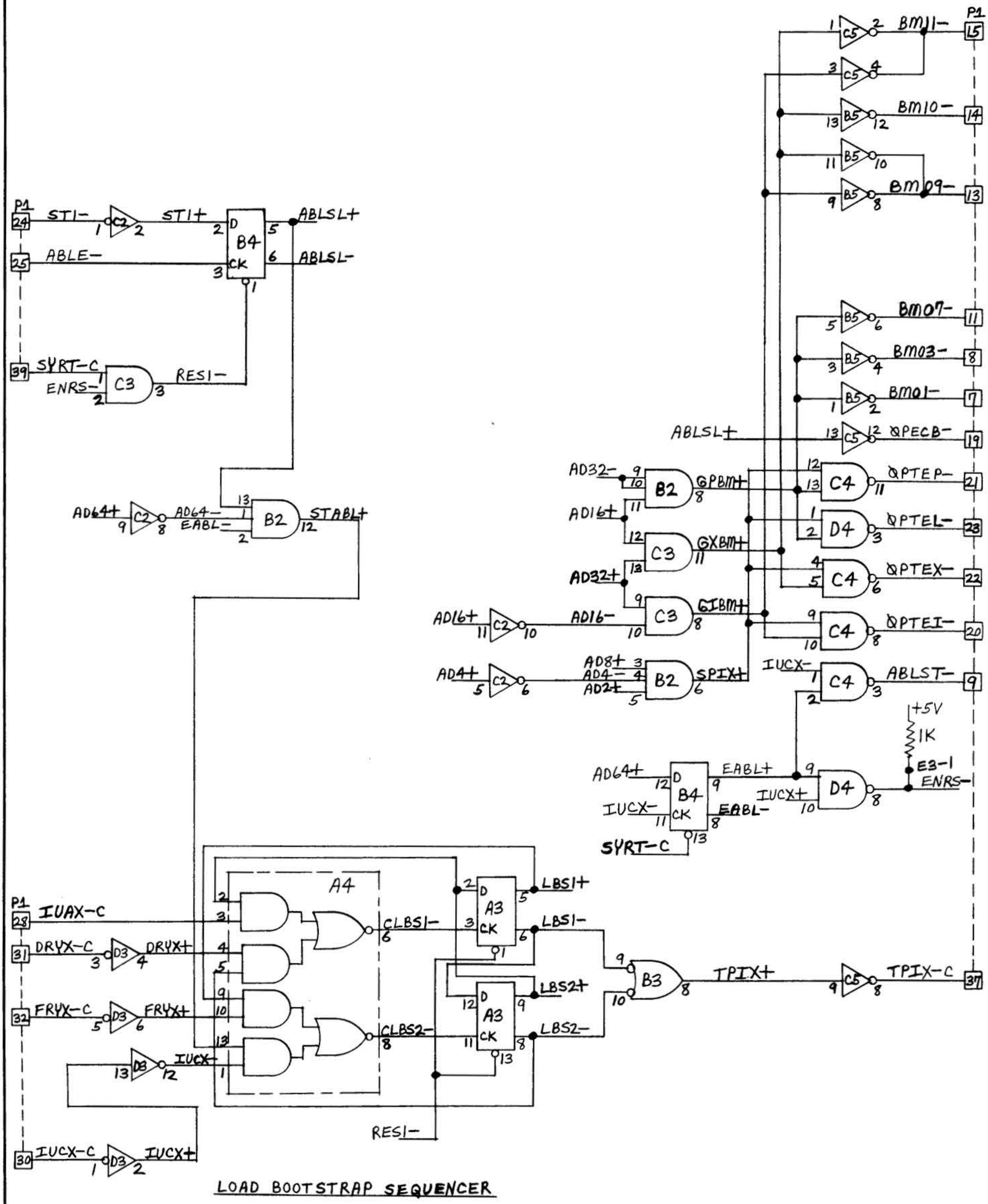
DR	DRM	12-3-70
CHK		
DSGN		12-3-70
ENGR	R. Russell	1-11-71
APPD	A. Whitcomb	1/8/71
APPD		1/9/71

varian data machines /a varian subsidiary
2722 michelson drive / irvine / california / 92664

TITLE
LOGIC DIAGRAM AUTO BOOTSTRAP LOADER

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0261	A

SCALE — | 620f-15 | SHEET 1 OF 3



LOAD BOOTSTRAP SEQUENCER

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0261	A
SCALE		SHEET 2 OF 3	

AB BUS GATING

WORD ASSEMBLY BUFFER

P1
70 AB15-C — H5 (8, 9, 10) — WSB8+
69 AB14-C — H5 (6, 4, 5) — WSB7+
68 AB13-C — H5 (11, 12, 13) — WSB6+
67 AB12-C — H5 (3, 1, 2) — WSB5+
66 AB11-C — F5 (11, 12, 13) — WSB4+
65 AB10-C — F5 (8, 9, 10) — WSB3+
64 AB09-C — F5 (6, 4, 5) — WSB2+
63 AB08-C — F5 (3, 1, 2) — WSB1+ — LBS1+B
49 AB07-C — E5 (11, 12, 13) — MQ8+
C5 (6, 5)
48 AB06-C — E5 (6, 4, 5) — MQ7+
47 AB05-C — E5 (8, 9, 10) — MQ6+
46 AB04-C — E4 (6, 4, 5) — MQ5+
E5 (3, 1, 2) — AD32+
45 AB03-C — E4 (11, 12, 13) — MQ4+
E4 (8, 9, 10) — AD16+
44 AB02-C — E4 (3, 1, 2) — MQ3+
D4 (6, 4, 5) — AD8+
43 AB01-C — D5 (8, 9, 10) — MQ2+
D5 (6, 4, 5) — AD4+
42 AB00-C — D5 (11, 12, 13) — MQ1+ — LBS1+A
D5 (3, 1, 2) — AD2+
LBS03+ — C3 (6, 4, 5) — LBS1+ LBS2+

H3 (SN7495, 8): 13, 12, 11, 10 — 2, 3, 4, 6, 5
F3 (SN7495, 8): 13, 12, 11, 10 — 2, 3, 4, 6, 5
LBS02+
D3 (8, 9): LBS01-
B3 (11, 12, 13): ADCS+, LBS02-, LBS01- — (3, 1, 2): LBS1-, LBS2+
B3 (6, 4, 5): LBS01-, LBS1+, LBS2-

MQ8+ 9, MQ7+ 7, MQ6+ 6, MQ5+ 5, MQ4+ 4, MQ3+ 3, MQ2+ 2, MQ1+ 1

ROM NO.1 F2 (15, 14, 13, 12, 11, 10): AD32+, AD16+, AD8+, AD4+, AD2+, AD1+
ROM NO.2 H2 (9, 7, 6, 5, 4, 3, 2, 1 — 15, 14, 13, 12, 11, 10): AD32-

E3-11 E3-10 E3-9 E3-8 E3-6 E3-5 E3-4 E3-3 E3-2 — 1K each — +5V

AD1+ AD2+ AD4+ AD8+ AD16+ AD32+

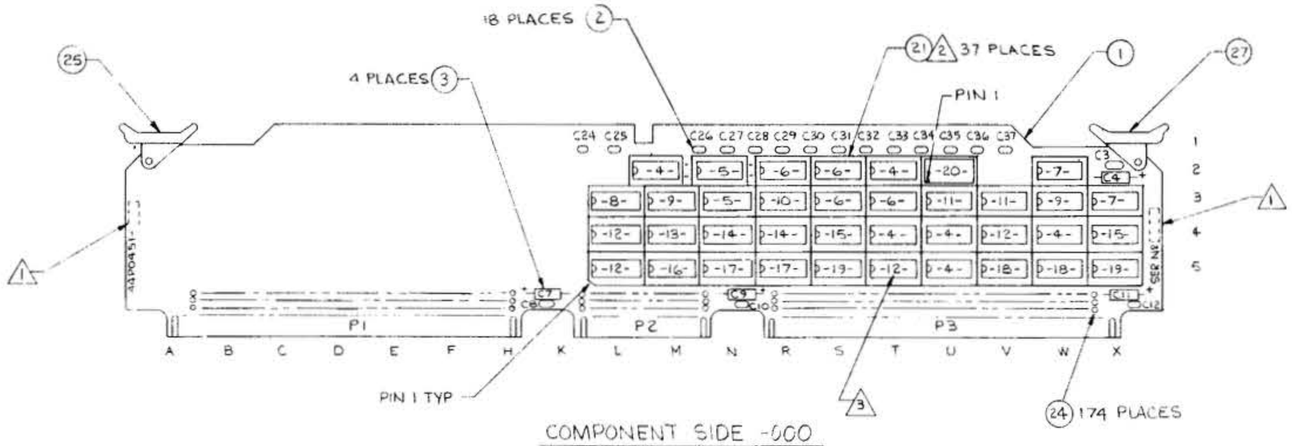
+5V — D2 (5, 12, 1, 9, 8, 11) — E2 (12, 1, 9, 8, 5)
D2: 14, 2, 3, RES1+, 10
E2: 14, 2, 3, 10, 11
ADDRESS COUNTER
AD64+

+5V — 1K — E3-12 — LBS02+ — C5 (10, 11)
RES1+ — C2 (12, 13) — RES1-
C2 (3, 4)

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9IC0261	A
SCALE			SHEET 3 OF 3

44D0451 E

REVISIONS			
SYM	ZONE	DESCRIPTION	APPROVED	DATE
A		PRODUCTION RELEASE EN 4847		9/13/72
B		REVISED PER EN 5082		1-3-73
C		REV & REDRAWN PER EN 5152		3-16-73
D		F/N 24 WAS 102 PLACES PER EN. 5246	W.B.O	4/26/73
E		REVISED NOTE 2 PER E.N 5269	W.B.O	9/19/73



COMPONENT SIDE -000

44D0451 B E

TABULATION BLOCK	
PART NO	REMARKS
44D0451-000	TTY
44D0451-001	ABL
44D0451-002	TTY/ABL

5. AT LOCATIONS D2 & E2 SOLDER SOCKET (F/N 21) AT PINS 5 & 10
4. WIRE PER WIRE LIST 95W0606 (-000 & -002) OR 95W0723 (-001 & -002)
3. NUMBERS BETWEEN DASHES ARE FIND NUMBERS.
2. SOLDER 14 PIN SOCKET (F/N 21) AT PINS 7 AND 14; SOLDER 16 PIN SOCKET (F/N 22) AT PINS 8 AND 16.
1. MARK SERIAL NO & APPLICABLE DASH NO & REV LTR OF THE P/L TO WHICH THE PART WAS MANUFACTURED APPROX WHERE SHOWN. IDENTIFICATION TO BE .12 HIGH AND PERMANENT.

NOTE: UNLESS OTHERWISE SPECIFIED

REFERENCE DRAWINGS

40D0458	PW. BOARD
95W0606	WIRE LIST (-000 & -002)
95W0723	WIRE LIST (-001 & -002)
91C0219	LOGIC DIAGRAM (-000 & -002)
91C0261	LOGIC DIAGRAM (-001 & -002)

FOR PARTS LIST SEE 44P0451

MODEL NO. 620f-15
NEXT ASSY 01A0951
MATERIAL
FINISH

DIMENSIONS ARE IN INCHES AND AFTER FINISHING
TOLERANCES (UNLESS OTHERWISE SPECIFIED)
X ±.1
XX ±.03
XXX ±.010
ANGLES ±0.5°
BREAK ALL SHARP EDGES .010 R APPROX
DO NOT SCALE DRAWING

DR ZOLL	10/4/72
CHK	10-17-72
DSGN ZOLL	10/4/72
ENGR	10/18/72
APPD	10/4/72
APPD	11/10/72

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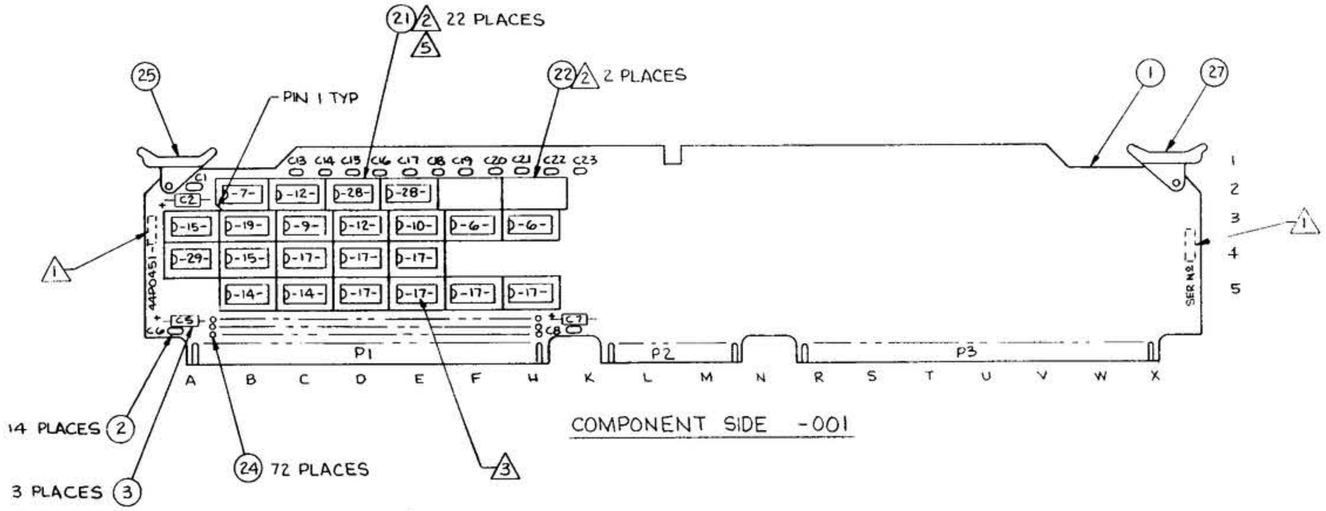
TITLE: TTY/ABL CONTROLLER ASSY

CODE IDENT NO.	SIZE	DWG NO	REV
21101	D	44D0451	E

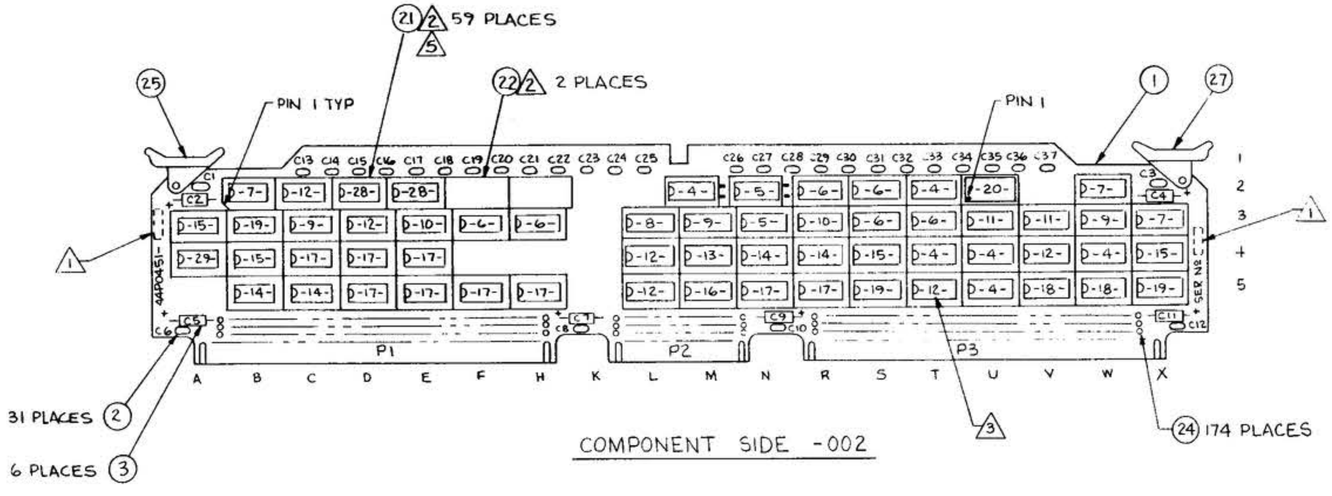
SCALE 1/1 SHEET 1 OF 2

44D0451 E

REVISIONS				
SYM	ZONE	DESCRIPTION	APPROVED	DATE
		SEE SHT 1		



COMPONENT SIDE -001



COMPONENT SIDE -002

44D0451
E

NOTE: UNLESS OTHERWISE SPECIFIED

CODE IDENT NO.	SIZE	DWG NO	REV
21101	D	44D0451	E
SCALE		SHEET 2 OF 2	

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DWG. NO. 44P0451

QUANTITY REQ'D PER DASH NO							PARTS LIST			CODE IDENT 21101	
				002	001	000	FIND NO	PART NUMBER	DESCRIPTION	REMARKS	ZONE
				REF	REF	REF	-	44D0451 E	ASSEMBLY		
				REF	-	REF	-	95W0606 E	WIRE LIST		
				REF	REF	-	-	95W0723 A	WIRE LIST		
				REF	-	REF	-	91C0219 F	LOGIC DIAGRAM		
				REF	REF	-	-	91C0261 A	LOGIC DIAGRAM		
				1	1	1	1	40D0453-000	P.W. BOARD		
				31	14	18	2	71A0009-003	CAPACITOR .1 μf		
				6	3	4	3	71N0200-225	CAPACITOR 2.2 μf		
				6	-	6	4	49A0099-000	I.C. SN74H109N		
				2	-	2	5	49A0019-000	I.C. SN74H40N		
				6	2	4	6	49A0090-001	I.C. SN7495N		
				3	1	2	7	49A0022-000	I.C. SN74H11N		
				1	-	1	8	49A0009-000	I.C. SN5862N		
				3	1	2	9	49A0104-000	I.C. MC3001P		
				2	1	1	10	49A0025-000	RESISTOR ASSY		
				2	-	2	11	49A0524-000	I.C. U6E960129		
				6	2	4	12	49A0040-000	I.C. SN7404N		
				1	-	1	13	49A0039-000	I.C. SN74H00N		

NEXT ASSY 01A0951	MODEL NO 620/f-15	APPD

REV	A	B	C	D	E	F	G	H
EN NO	4847	4913	5007	5082	5152	5246	5269	5340
DATE	[illegible]	11-23-70	1-11-71	1-11-71	1-11-71	4-21-71	4-21-71	4-21-71
DR	[illegible]	GRL	DM	D.M.	D.M.	dm	dm	dm
CHK	B.B.	RAD	RAD	[illegible]	[illegible]	WKO 4/29/71	WKO 4/29/71	WKO 4/29/71

TITLE: PARTS LIST
TTY/ABL CONTROLLER ASSY

DWG NO 44P0451 REV 4

SHEET 1 OF 2

96A0017-000B

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DWG. NO. 44P0451

QUANTITY REQ'D PER DASH NO							PARTS LIST			CODE IDENT: 21101	
				002	001	000	FIND NO	PART NUMBER	DESCRIPTION	REMARKS	ZONE
				4	2	2	14	49A0575-000	I.C. SN7405J		
				4	2	2	15	49A0012-000	I.C. SN7474N		
				1	-	1	16	49A0023-000	I.C. SN74H04N		
				9	7	2	17	49A0081-001	I.C. SN7403N		
				2	-	2	18	49A0010-000	I.C. SN6006N		
				3	1	2	19	49A0007-000	I.C. SN7400N		
				1	-	1	20	01C0995-000	COMPONENT ASSY		
				59	22	37	21	58A0060-000	SOCKET, 14 PIN		
				2	2	-	22	58A0060-001	SOCKET, 16 PIN		
							23				
				174	72	174	24	58A0062-002	POST, WIRE WRAP		
				1	1	1	25	16S1057-061	CARD HANDLE		
				0	0	0	26	53A0333-040	WIRE, KYNAR, YEL	30 AWG	
				1	1	1	27	16S1057-056	CARD HANDLE		
				2	2	-	28	49A0112-000	I.C. SN7493N		
				1	1	-	29	49A0041-000	I.C. SN74H51N		

NOTES:

DWG NO 44P0451

REV H

SHEET 2 OF 2

96A0017-001B

BINARY LOAD/DUMP (BLD II)

The ABL is intended to be used with the Varian 620 Binary Load/Dump (BLD II) program (92 A 1007-001). BLD II loads paper tape object programs produced by DAS 4A and DAS 8A assemblers. It also provides for dumping of the binary contents of memory onto paper tape in a loadable format.

Since the ABL loads the BLD II into the lowest 4K of memory starting at address 07000, BLD II, once loaded, automatically relocates the binary load/dump portions of its program to the top of memory, provided that the computer has memory wrap-around.

BLD II selects load/dump and I/O devices compatible with the ABL input device.

The BLD II program is fully discussed in document number 98 A 9908 002.

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