PRELIMINARY

VARIAN 620/f

MAINTENANCE MANUAL

Specifications Subject to Change Without Notice

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FOREWORD

This manual contains hardware maintenance information for the Varian Data Machines 620/f computer system. The manual is intended to be used in conjunction with the 620/f Reference Handbook (document number 98 A 9908 001) and the 620/f Test Programs Manual (98 A 9908 960). The reference handbook contains information on overall system capabilities and a comprehensive description of the 620/f software. The test programs manual describes the various test programs that are available for testing and maintaining the 620/f computer system.

This manual is divided into chapters. Chapter I provides an overall view of the computer system. It describes features and applications, specifications, options, and documentation.

Installation information found in chapter II consists of system layout, physical descriptions, interconnection information, and system interrupt priority data.

Chapter III provides operations information including preliminary operating procedures and control panel operation information.

Chapter IV contains theory of operations information that includes functional block and detailed circuit descriptions, and mnemonic definitions.

The maintenance information in chapter V contains general troubleshooting data and checkout procedures, and relates test program error indications to the computer hardware. Useful reference material is contained in appendixes following this chapter.

Volume 2 of this manual is assembled at the time of computer shipment to reflect a particular system configuration. It consists of engineering documents such as assembly and installation drawings, logic diagrams, and wire lists.

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CHAPTER V
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SECTION 1
FEATURES AND APPLICATIONS

The Varian Data Machines 620/f is a high-speed, general-purpose, digital computer for scientific and industrial applications. Its features include:

Fast Operation	750-nanosecond memory cycle
Large Instruction Set	142 plus 8 optional instructions
Word Length	16 bits
Modular Core Memory	Expandable to 32,768 words in 4,096- or 8,192-word increments
Read-Only Memory	Contains addressable core; 16-bit word length; provides a CPU cycle time of Less than 550 nanoseconds
Automatic Data Transfer	Direct memory access (DMA) facility provides automatic data transfers with rates to 274,000 words per second; priority memory access (PMA) for transfer rates to 1.3 million words per second
Multiple Addressing	Direct, indirect, relative, preindexed and postindexed, immediate, extended, and indirect indexed
Flexible I/O	64 devices can be placed on the I/O bus. The I/O system can easily be expanded to include features such as automatic block transfer, multilevel priority interrupt, and cycle-stealing data transfers
Extensive Software	Complete package includes a symbolic assembler, subroutine library, debugging, AID, loader, ANSI FORTRAN compiler,

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master operation system (MOS) for disc, drum, and magnetic tape, RPG IV compiler (a business-oriented language), BASIC compiler, and hardware diagnostics

SECTION 2
SPECIFICATIONS

The specifications for the 620/f computer are listed in table I-1.

Table I-1. 620/f Specifications

Parameter	Description
Type	General-purpose, parallel-operation digital computer
Memory (Read/Write)	A 3-wire/3D magnetic core memory with a 16-bit word length, 750-nanosecond full cycle time, 400-nanosecond access time, 4,096-word basic and expandable to 32,768 words in 4,096 increments, asynchronous with CPU operation
Memory (Read-Only)	A linear ferrite magnetic core ROM can be added to the memory system. The total number of words (read/write plus ROM) cannot exceed 32,768. The ROM has a 16-bit word length, addressable core memory. When operating from the ROM, the CPU cycle time is less than 550 nanoseconds, asynchronous with CPU operation
Word Length	16 bits
Machine Cycle Speed	750 nanoseconds
Operations Registers	A register: 16-bit accumulator and shift register

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Table I-1. 620/f Specifications *(continued)*

Parameter	Description	
Auxiliary Registers	B register:	16-bit accumulator and shift register (least significant half of double-length accumulator) or index register
	X register:	16-bit index register
	P register:	15-bit program counter and index register for relative addressing
	I register:	16-bit instruction register
	L register:	15-bit memory address register
	R register:	16-bit arithmetic buffer register
	D register:	16-bit input/output register
Arithmetic	Binary, two's complement notation	
Arithmetic Operation Times	Add or Subtract	1.5 microseconds
	Multiply (optional)	Variable, 5.1 microseconds average
	Divide (optional)	7.0 microseconds
	Register Change	750 nanoseconds
	Input/Output	From A or B register, 1.5 microseconds From memory, 2.25 microseconds
Logic Levels	Positive Logic: (Internal) True = +2.4V minimum, +5V maximum False = -0.5V minimum, +0.5V maximum Negative Logic: (I/O Bus) True = -0.5V minimum, +0.4V maximum False = +2.8V minimum, +3.6V maximum	

Table I-1. 620/f Specifications *(continued)*

Parameter	Description
Addressing Modes:	Direct: to 2,048 words Relative to P register: to 512 words Index with X register hardware: to 32,768 words (does not add to execution time) Index with B register hardware: to 32,768 words (does not add to execution time) Multilevel indirect: to 32,768 words immediate Indirect indexed: to 32,768 words Extended: to 32,768 words
Instructions	142 plus 8 optional instructions
Instruction Types	One-word addressing One-word nonaddressing Two-word addressing Two-word nonaddressing
Input/Output	Asynchronous
I/O Program Control Instructions	Data transfer in: One-word nonaddressing Two-word addressing Data transfer out One-word nonaddressing Two-word addressing External control One-word nonaddressing Program sense Two-word addressing
Computer Options	Memory protection (MP) Buffered interlace controller (BIC) Power failure/restart (PF/R) Real-time clock (RTC) Automatic bootstrap loader (ABL) Priority interrupt module (PIM) High-speed priority memory access (PMA)

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Table I-1. 620/f Specifications *(continued)*

Parameter	Description
	Optional instruction set: Hardware multiply/divide (M/D) Bit test (BT) Skip if register equal (SRE)
Software	SYMBOLIC ASSEMBLER: Modular two-pass symbolic assembler operating in the basic 4,096-word memory. Includes 17 basic pseudo-operations. The 8,192-word memory version includes over 30 pseudo-operations
	FORTRAN: Modular one-pass compiler; subset of ANSI FORTRAN for 8,192-word memory
	AID: Program analysis package that assists programmers in operating the machine and debugging other programs. Includes basic operational executive subroutines
	DIAGNOSTICS: Software package that provides fast off-line verification of CPU and peripheral operation and assists in isolating and correcting suspected faults
	SUBROUTINES: Complete library of basic mathematical, fixed- and floating-point, single- and double-precision, number conversion and peripheral communication subroutines plus provisions for adding application-oriented routines

Table I-1. 620/f Specifications *(continued)*

Parameter	Description
	MOS: The master operating system (MOS) provides for automatic batch processing that includes a minimum 8K core memory BASIC BASIC is an easy-to-use programming language for business and scientific applications, permitting an inexperienced operator to program the system with only a few hours training RPG IV (optional): The report program generator (RPG IV) system, a hardware/software package, produces reports, financial statements, sale records, and other commercial documents in tabular form
Dimensions	The mainframe and expansion chassis I, II, and III are 10.5 inches (26.6 cm) high, 19 inches (48.1 cm) wide, and 21 inches (53.1 cm) deep (expansion chassis III is 15 inches (37.9 cm) deep). The mainframe power supply is approximately 5.25 inches (13.3 cm) high, 19 inches (48.1 cm) wide, and 21 inches (53.1 cm) deep
Weight	The mainframe and expansion chassis each weigh approximately 65 pounds (29.3 kg). The mainframe power supply weights approximately 80 pounds (36.2 kg)
Input Voltage	105 to 125V ac or 210 to 250V ac at 50 or 60 Hz*

*For compatibility with teletype, frequency must be either 50 or 60 (+ 1/2, -0) Hz.

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Table I-1. 620/f Specifications *(continued)*

Parameter	Description
Input Current	The mainframe power supply requires approximately 15 amperes ac; each expansion frame power supply requires approximately 4 amperes ac
Temperature - Operating Storage	0 to 50 degrees C -20 to 70 degrees C
Humidity - Operating Storage	To 90 percent without condensation To 95 percent without condensation
Vibration	3 to 10 Hz at 1g force or 0.25 double amplitude, whichever is less. Exponentially raised frequency from 3 to 10 Hz and back to 3 Hz over a 10-minute period, three complete cycles. This specification applies for all three principal axes
Shock	4g for 5 to 11 milliseconds, essentially sine shock waveform (all three principal axes; both directions in each axis)

SECTION 3
COMPUTER OPTIONS

Both internal and peripheral options are available for use with the 620/f computer.

3.1 INTERNAL COMPUTER OPTIONS

Internal options increase the efficiency and versatility of the 620/f computer. These functional options are available as plug-in units that can be installed in the computer mainframe or in expansion frames.

3.1.1 620/f-5 Memory Protection

Memory protection (MP) provides a means of partitioning core memory whereby the contents of certain memory areas, designated as protected areas, are prevented from being altered by programs operating from areas that are not protected. There are no prerequisites for using MP.

3.1.2 620/f-6,-7,-8 Teletype Controller

The Teletype (TTY) controller controls the command and information transfer between the computer and one factory-modified teletype unit (33 ASR, 35 ASR, or 35 KSR). The first TTY controller, directly controlled by the CPU, is located in the CPU tray on a single 3-by-15-inch (7.7 x 38.1 cm) circuit card. Additional TTY controllers can be added if a special TTY buffer is included in the system. They can be installed in any peripheral controller slot in the mainframe and expansion chassis. Optional controllers and the TTY buffer are on 7.75-by-12-inch (19.7 x 30.3 cm) circuit cards.

3.1.3 620/f-10 Optional Instruction Set

The 620/f optional instruction set provides the required logic to implement the instructions described in the following subsections.

3.1.3.1 MULTIPLY/DIVIDE

The multiply/divide option reduces the steps required to perform a multiply or divide subroutine. The types of multiply and divide instructions available are:

a. One-word

b. Two-word addressing (preindexing and postindexing)

c. Two-word nonaddressing

During multiply, the contents of the B register are multiplied by the contents of the effective memory address. The contents of the A register are added to the product prior to execution of the instruction. The result is placed in the A and B registers, with the most significant half in the A register and the least significant half in the B register. The sign of the product is contained in the sign position of the A register. The sign position of the B register is reset to zero. If the contents of the B register and memory contain the largest possible negative number, bit 15 of the A register is set as a magnitude bit and overflow is set.

During divide, the contents of the A and B registers are divided by the contents of the effective memory address. The quotient is placed in the B register with the sign, and the remainder is placed in the A register with the sign of the dividend.

3.1.3.2 BIT TEST

The bit test (BT) instruction is a two-word instruction with a jump address in the second word. The instruction tests the condition of a selected bit in the A or B register and jumps if the condition is met.

3.1.3.3 SKIP IF REGISTER EQUAL

The skip if register equal (SRE) instruction is a two-word instruction with a skip-out address in the second word. The instruction performs a logical compare between a specified register (A, B, or X) and a memory word specified by the second word. If the result is not equal, the next instruction in sequence is executed. If the result is equal, the next two locations are skipped and the instruction in the third location is executed.

3.1.4 620/f-12 Priority Memory Access

The priority memory access (PMA) option allows external devices to directly access the 620/f memory. With four levels of priority, up to four devices can share the same data and address lines. Data can be asynchronously transferred to the CPU at rates to 1.3 million words per second.

A PMA request from an external device prevents CPU use of memory. It has the highest I/O priority in the system. A power failure suspends PMA activity until power has been

restored. A controller (designed by the user or Varian) is required for interfacing the external device and PMA circuits.

3.1.5 620/f-13 Real-Time Clock

The RTC provides flexible time orientation that can be used for time-of-day accumulation and as an interval timer. Known periods of time are generated by the RTC for program-sequencing. A free-running counter that can be read under program control is also provided.

The main program is periodically interrupted by the RTC to initiate subroutines which accomplish the desired real-time functions. The RTC can generate two types of interrupts: variable interval and memory overflow. The first interrupt is a time-base signal that increments a specific memory address when recognized by the computer. The second interrupt occurs when the incremented memory address reaches a count of 040001. The frequency of the increment interrupt is adjustable with program-controlled I/O and can range from 3 to 10,000 per second. A predelivery factory adjustment sets the RTC to initiate one increment interrupt every millisecond unless otherwise programmed. An externally generated time base can be used.

3.1.6 620/f-14 Power Failure/Restart

The PF/R provides an orderly shutdown in case of power failure or turnoff and restarts the program when power is restored.

Power input to the computer is indirectly monitored by circuits in the computer power supply. A power failure alarm voltage in the power supply is constantly sensed by the PF/R to determine power status. If the alarm voltage drops (because of power failure or power switch turn-off), the PF/R causes an interrupt. The CPU then executes a user-programmed subroutine that places the contents of volatile registers in memory and halts, after which the CPU and memory are disabled. The power-down service routine cannot be interrupted by lower-priority options or controllers.

When power is restored, the PF/R enables the memory. The CPU executes a user-programmed subroutine that restores the contents of the volatile registers, and the system resumes service of the program in progress at the time of the interrupt.

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3.1.7 620/f-15 Automatic Bootstrap Loader

The automatic bootstrap loader (ABL) is a hardware option that automatically loads the 620/f bootstrap program into core memory from an integrated-circuit ROM. This option saves the time and effort involved in manually loading the bootstrap program.

3.1.8 620/f-16 Priority Interrupt Module

The PIM establishes eight levels of interrupt priority for selected peripheral device controllers and stores and processes, in the order of their priority, interrupt requests from these controllers.

The PIM automatically scans the interrupt lines every 900 nanoseconds. If signals occur on more than one interrupt line, the highest-priority signal is acknowledged. The remaining interrupt requests are stored until each has been acknowledged. The PIM permits any or all of the eight interrupt lines to be enabled or disabled.

Acknowledgement of an interrupt by the CPU causes the instruction located at the memory address specified by the PIM to be executed. The instruction may be any of the computer repertoire with the exception of I/O commands. This technique permits an interrupt to be serviced in one instruction period.

3.2 PERIPHERAL OPTIONS

This section describes a sampling of various peripheral options that are available with the 620/f computer. The 620/f computer is I/O-compatible with the Varian Data Machines 620/i computer. For this reason (with the exception of the first teletype controller), the peripheral controllers described in this section are the 620/i type. The circuits of the 620/i peripheral controllers are contained on 7.75-by-12-inch (19.7 x 30.3 cm) circuit cards that can be installed in any peripheral controller slots in the 620/f mainframe or expansion chassis.

3.2.1 Teletypes

The optional TTY controllers (620/f-6,-7,-8) can be controlled through the I/O bus or through the BIC. Up to eight TTY units and controllers can be installed in a computer system. One TTY buffer board is required for TTY units and controllers 2 through 8 to be indirectly controlled by the CPU through the I/O bus. If the BIC is installed, the CPU is free to perform other program functions during data transfers.

The factory-modified Teletype unit that is controlled by the TTY controller can be a model

33 ASR, 35 ASR, or 35 KSR. The ASR models include paper tape reader and punch facilities; the KSR model uses only keyboard-entered instructions and data.

3.2.2 Punched Card Equipment

3.2.2.1 PUNCHED CARD READER

The model 620/f-23,-24 card reader systems (CRS) are peripheral options that read data from 80-column (51-column optional) punched cards and transfer the data to a 620/f computer. The CRS consists of either a Soroban model ERD (620/f-23) or a Data Products model SR-300 (620/f-24) card reader and a card reader controller.

The controller is constructed with 28 integrated circuit chips and discrete component assemblies mounted on a standard wired-socket card. The controller can be mounted in any peripheral controller slot of an expansion chassis.

The card reader reads the information from punched cards and provides the data to the controller. The card reader controller provides a nonbuffered interface between the card reader and the CPU. It also provides the timing and logic circuits to effect the transfers. The controller can transfer data to the CPU under direct program control or under supervision of a BIC.

3.2.2.2 CARD PUNCH

The model 620/f-26 card punch controller controls data transfer from the computer to the card punch. The controller permits punch operation under CPU control and, optionally, BIC control.

The data buffer register in the controller stores the 12-bit data words from the CPU. The control section synchronizes and controls punch operation. A data present strobe to the punch indicates that correct data are on the data lines.

Under program control, the controller senses the punch (ready or not busy) and transfers data to it. Under BIC control, the controller requests data and the BIC controls the transfer from the specified memory addresses. Transfer continues until terminated by the BIC.

3.2.3 Nine-Track Magnetic Tape Equipment

The nine-track magnetic tape system consists of up to four model 620/f-30 Peripheral Equipment Corporation Series 6000 tape transports and one magnetic tape controller (MTC) for processing IBM 2400-compatible tapes.

The MTC provides a buffered interface between the 620/f I/O bus and the tape transport. The MTC accommodates up to four tape transports, but only one of these is in use at any given time.

The MTC is on two wire-wrapped socket cards which can be installed in an expansion chassis. It contains all read/write registers and logic circuitry for the tape transport control.

Computer control of the magnetic tape system is accomplished through the I/O bus. The controller can also be operated under direction of the BIC.

If the system contains more than one tape transport, the transports are connected to the MTC in party-line configuration. The program controls the selection of the one transport that can operate at any given time.

3.2.4 Seven-Track Magnetic Tape Equipment

The seven-track magnetic tape system consists of up to four magnetic tape transports and a magnetic tape controller. The system can read and record a magnetic tape that is IBM 2400-compatible for seven- track systems.

The magnetic tape controller provides a buffered interface between the 620/f I/O bus and a seven-track magnetic tape transport. The controller accommodates up to four transports of the Peripheral Equipment Corporation 6000 series. However, only one tape transport can be selected for use at any one time.

The tape controller comprises two circuit cards and contains all read/write data registers and timing and control logic required to control one tape transport.

Computer control of the magnetic tape system is accomplished through the I/O bus. The controller can also be operated under direction of the BIC.

When more than one tape transport is used with the controller, the transports are connected to the controller in party-line configuration. However, only one transport may be operated at a time. Transport selection is program-controllable.

3.2.5 Disc Memories

The disc memory options consist of models 620/f-38 through -43 rotating memories. Only the 620/f-42 and -43 specifications are described herein.

The disc memory options offer bulk storage for data and library software routines. Data can be stored and retrieved at maximum data transfer rates of up to 59K words per second. the 620/f-42A is a hardware expansion option used to increase the basic data storage of the -42 disc memory to a maximum capacity.

The -42 disc memory option offers a basic storage capacity of 131,072 words. This basic capacity can be expanded to a maximum of 262,144 words by incorporating the -42A expansion option. This expansion feature requires the addition of 128 track head assemblies mounted within the disc memory unit. The -43 disc memory option provides a maximum storage capacity of 262,144 words.

The hardware components comprising a complete operating system for both disc memory options are:

a. Rack-mounted disc memory unit containing a built-in operating dc power supply.

b. Interconnecting system cable.

c. Plug-in interface and disc controller logic.

3.2.6 Drum Memories

The drum memory system (models 620/f-44 through -49) consists of a drum controller circuit card, a drum memory unit, and a dc power supply.

The drum memory system is field-expandable to accommodate increased system storage requirements. The smaller of the two drums is expandable in increments of 16 tracks up to a maximum of 128 tracks. The larger model is expandable in increments of 64 tracks up to a maximum of 512 tracks. Each track has 1,920 words (16 bits of storage). This provides a maximum storage capacity of 983,040 16-bit words in a 512 data track system. For a 128 data track system, the storage is 245,760 sixteen-bit words. A computer word stored on the drum unit consists of 16 data bits and one parity bit.

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The controller circuit card contains all data registers and timing and control logic required to control one drum memory unit. The drum memory unit contains a single rotating drum, mechanical drive assemblies, and read/write control logic. The dc power supply provides required operating voltages.

Control of the drum memory system by the 620/f computer is accomplished under direction of the BIC. The BIC is a prerequisite of the drum memory system. Data transfer between the drum controller and drum memory unit is accomplished via the drum cable.

The drum controller performs the following functions:

a. Controls bit serial data transfer between the controller and drum memory unit.

b. Monitors and detects parity errors during read-from-drum operations.

c. Controls mode of operation and provides all interface control between the computer and the drum memory unit.

3.2.7 High-Speed Paper Tape Equipment

The model 620/f-52 high-speed paper tape system is composed of a controller card, a paper tape perforator, and a paper tape reader. A paper tape spooler is also available for use with the reader.

The controller card contains a data register which buffers the data words being transferred, a decoder section which interprets instructions received from the computer, a timing and control section which synchronizes operation of the peripheral equipment with the computer and necessary interface hardware.

The paper tape controller can transfer data from the tape reader to the computer; it can also transfer data to the tape perforator from the computer, or it can be used to reproduce paper tapes. The controller can transfer data into the computer in a continuous read mode, which places the tape reader in continuous slew until a stop command is received, or it can operate in a step read mode, requiring a new instruction from the computer for each transmitted data word.

Computer control of the paper tape system is accomplished through the I/O bus. The controller can also be operated under direction of the BIC.

Each controller is capable of operating one perforator and one reader on a time-shared basis.

3.2.8 Data Communications Equipment

3.2.8.1 DATA COMMUNICATIONS CONTROLLER

The model 620/f-60 data communications controller system (DCC-1) provides a data communications link between the 620/f computer and remote teletype terminals.

Using telephone lines as the communications media, bidirectional transmission of binary serial data is accomplished by means of dataset modems and 33/35 ASR TTY terminals. The dataset modems must be located within 50 feet (15m) of their associated interface units.

The DCC-1 system offers an economical and efficient means of providing on-line computer services to many remote users. Some typical applications include: on-line program debugging, on-line computation and execution, information storage and retrieval data, inquiry services, computer aid for 'hands-on' use in classroom instruction, and scientific hybrid simulation. In addition, these remote terminals can also be used in an off-line mode for general-purpose utility program routines.

The overall DCC-1 system consists of the power supply (620/f-95-5), dataset, TTY coupler, 33/35 ASR TTY, a line controller card, and a multiplexer card.

The multiplexer circuit board (DM171) is used to select and control the operation of all the enabled data channels. The line controller circuit board (DM135) provides the logic for four data communication channels.

3.2.8.2 DATASET CONTROLLER

Dataset controllers interface with the computer and modems that are compatible with standard datasets. These controllers can operate in half- or full-duplex mode. They detect and establish input synchronization and switch to word mode for data transfers.

Data are transferred in one of three ways:

a. The controller can be connected to the BIC for operations requiring minimum program intervention. BIC can be connected for half-duplex operation to input or output data. In full-duplex operation, I/O functions can be connected to the BIC and data flow can be controlled by the program.

b. Full- or half-duplex operation can be completely controlled by the program.

c. Inputting data to the PIM provides interrupt-controlled transfers.

The controller functions are:

a. Receive. The controller receives data from the modem and transfers it to the computer.

b. Transmit. The controller receives data from the computer and outputs it to the modem.

c. Receive/Transmit. The controller simultaneously transfers data in both directions.

3.2.9 Digital Plotter

The model 620/f-72 digital plotter system consists of a Calcomp 565 digital plotter and plotter controller card. The plotter produces high-quality, ink-on-paper graphic presentations of computer output.

The plotter controller provides a fully buffered interface to permit operation of the plotter under program control or under the direction of BIC.

The plotter uses digital commands from the computer to produce the plot or drawing on a 12-inch wide roll of paper. These commands actuate step motors to produce incremental movement of the pen with respect to the paper. One step motor controls movement in two directions along the X axis, and a separate motor controls movement on the Y axis. X-axis movement is accomplished by rotating the paper drum in either the +X or -X direction. The pen is moved to the left or right to effect movement on the Y axis. Composite commands can be given to move the pen on two axes simultaneously. This results in commands to move the plotter pen in any of eight directions. Model 565 operates at up to 300 increments per second, with three optional increment sizes: 0.005 inches, 0.010 inches, and 0.1 millimeters. The increment size is specified when ordering.

3.2.10 Line Printer Equipment

The model 620/f-76 buffered line printer represents an operational, self-contained subsystem consisting of a high-speed line printer and an interface controller.

This option offers high performance and printing quality to meet user requirements in a wide range of on-line applications. The line printer can also be used for off-line activities by incorporating the required interface control logic.

Significant features and characteristics of the line printer are:

a. Fully buffered line storage of up to a 132 six-bit character capacity.

b. Programmed line space control using standard TTY paper tape format.

c. Up to 600-line-per-minute printing speeds providing 63 graphic and one blank (ASCII) character codes.

d. High reliability and printout quality as a result of friction-free, one-piece hammer construction.

3.2.11 A/D and D/A Converters

The model 620/f-85 A/D converter, or analog input system (AIS), converts multiplexed analog input signals to equivalent digit values. The model 620/f-87 D/A converter, or analog output system (AOS), converts digit values to equivalent multiplexed output signals.

The converters consist of a controller, multiplexer, and power supply. The basic multiplexer configuration has 32 channels connected in a single-ended mode or 16 channels connected in a differential mode. The multiplexer channels can be expanded in increments of 32 single-ended channels or 16 differential channels. The maximum number of channels is 128 single-ended or 64 differential.

3.2.12 Oscilloscope Display System

The model 620/f-73 oscilloscope display system provides visual display of 620 computer output. The system includes a Tektronix model 602 oscilloscope with a 5-inch (8.7 cm) rectangular cathode ray tube (CRT), a controller, reference power supply, and interconnecting cables.

The oscilloscope controller converts digital data to analog values which drive the horizontal

and vertical deflection plates of the oscilloscope. The oscilloscope is specially designed for X-Y presentation. One of the D/A converters in the controller drives the oscilloscope X axis; the other, the Y axis. The Z channel input turns the CRT beam on and off.

The display system is directly under program control. The display is programmed by outputting data to one of the two A/D converters. Portions of the display can be inhibited by the program.

3.2.13 Buffered I/O Controller

The model 620/f-80 buffered I/O controller provides a self-contained, programmable hardware interface for general-purpose data-handling.

The input and output buffer registers provide parallel word data communications between the computer I/O bus and an external device. In addition to data handling, the output buffer register can be programmed to output discrete control bits to an external device.

The buffered I/O controller uses a customer-fabricated U cable, up to 20 feet (6m) long, for communication with external devices.

3.2.14 Digital I/O Controller

The model 620/f-81 digital I/O controller (DIOC) provides a programmed link between an external device and the computer. There are eight separate control and sensing lines to permit the user to initialize, implement iterative control sequences, synchronize otherwise asynchronous external devices, and monitor the operational state of an external device.

The DIOC operates entirely under program control. The function code defines one of eight individual control or sensing lines. The DIOC responds to an EXC command by placing a pulse on the selected output control line. Similarly, it responds to a SEN command by testing the operational state of an external device via the true or false level applied to the selected sense-response line.

The DIOC uses a customer-fabricated U cable, up to 20 feet (6m) long, for communication to external devices.

3.2.15 Buffer Interlace Controller

The model 620/f-20 BIC frees the CPU to perform other functions during block word transfers. The BIC transfers 16-bit words to and from memory and peripheral controllers connected to the I/O bus. These transfers occur at a maximum rate of 274,000 words per second.

3.2.16 Relay I/O Module

The model 620/f-83 relay I/O option provides a general-purpose, relay-buffered data link between special peripherals and the 620/f. This option has the capability of 16 relay-buffered inputs (620/f-83-2), 16 mercury-wetted relay contact outputs (620/f-83-1), or combined input/output (620/f-83-3). The relay input and output options are each packaged on one 7.75-by-12-inch (19.7 x 30.3 cm) socket board. Printed circuit etch is used for the relay portion of the board.

3.2.16.1 RELAY INPUTS

In the model 620/f-83-2, input relay contacts are activated by voltages from the user's equipment through the 12V dc input relay coil (10 volts at 6.5 mA minimum). Series resistors for coil input voltages greater than 12 volts can be installed. An energized input relay coil closes a contact that is gated into a flip-flop. This 16-bit flip-flop register can be accessed by the 620/f with one of five data input commands. The flip-flop register can be cleared with an external control command or by system reset. The flip-flops remain set after an initial relay input until they are cleared.

3.2.16.2 RELAY OUTPUTS

This option allows isolated parallel data transfer of a 16-bit word from the 620/f via mercury-wetted relay contacts to the user's equipment. A 16-bit word is clocked into a flip-flop register by any of three data transfer out commands. The register drives 16 discrete circuits that, in turn, drive the 12-volt relay coils closing the contacts.

The relays can be cleared by an external control instruction, transferring all-zeros data out, or by system reset. The relay contacts remain closed until the flip-flops are cleared.

3.2.17 Priority Data Channel

The model 620/f-12A priority data channel (PDC) performs block data transfers between memory and a high-speed peripheral device. The PDC operates in the 620/f system that includes the PMA, PIM, device controller and up to eight high-speed peripherals. One PMA priority level is assigned to each PDC.

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The device controller contains logic to control the high-speed peripherals; it must be specially designed for the requirements of the particular device.

The PDC is a standard unit and can interface with any device controller. It is contained on one 7.75-by-12-inch (19.7 x 30.3 cm) wired-socket card and is installed adjacent to the device controller in expansion chassis 1. One PDC is required for each controller.

SECTION 4
DOCUMENTATION

To ensure full utilization of the 620/f computer system, technical manuals (of which this manual is a part) are provided with each computer. The manuals, along with their part numbers, are listed below.

Title	Document No.
620/f Reference Handbook	98 A 9908 001
620/f Maintenance Manual	98 A 9908 050
620/f Test Programs	98 A 9908 960
620/f-5 Memory Protection	98 A 9908 490
620/f-6,-7,-8 Teletype Controller	98 A 9908 160
620/f-10 Optional Instruction Set	98 A 9908 430
620/f-12 Priority Memory Access	98 A 9908 420
620/f-13 Real-Time Clock	98 A 9908 450
620/f-14 Power Failure/Restart	98 A 9908 440
620/f-15 Automatic Bootstrap Loader	98 A 9908 300

SECTION 1
SYSTEM LAYOUT AND PLANNING

1.1 COMPUTER CHASSIS

The three types of chassis available with the 620/f computer system are:

a. Mainframe

b. Expansion chassis I

c. Expansion chassis II

1.1.1 Mainframe

The basic computer hardware consists of central processing unit (CPU) and memory circuit cards and is contained in the mainframe. Memory size can be either 8,192 words (8K) or 4,096 words (4K).

The mainframe can also accommodate internal computer options and two peripheral controller cards.

The internal computer options that can be installed in the mainframe are:

a. Priority memory access (PMA)

b. Optional instruction set

c. Memory protection (MP)

d. Automatic bootstrap loader (ABL)

e. First Teletype (TTY) controller

f. Real-time clock (RTC)

g. Power failure/restart (PF/R)

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h. Priority interrupt module (PIM)

i. Buffer interlace controller (BIC)

A peripheral controller interfaces the computer and an external device (i.e., line printer, card reader, magnetic tape transport, etc.) One edge of the controller card plugs into the computer I/O groundplane, and the other edge, into cables that connect to the peripheral device. A peripheral controller can be contained on one 7.75-by-12-inch (19.7 x 30.3 cm) circuit card; however, some controllers require more than one card (refer to the 620/f reference manual, document number 98 A 9908 001).

If the PIM and BIC are included in the system, they must be installed in the mainframe peripheral controller card slots. The first TTY controller card is installed in the mainframe CPU tray (with the CPU and internal option cards). Additional peripheral controller cards must be installed in an expansion chassis.

1.1.2 Expansion Chassis

With expansion chassis, the system can contain up to 32K of memory and up to ten peripheral controllers.

Expansion chassis I can accommodate six peripheral controller cards and 8K (or 4K) of memory.

Expansion chassis II can contain up to 16K of memory and two peripheral controller cards.

With the maximum ten peripheral devices included in the system, a second chassis I may be required because some peripheral devices connect to controllers that consist of two or more circuit cards.

1.2 POWER AND ENVIRONMENTAL REQUIREMENTS

One mainframe power supply provides power for the mainframe, one expansion chassis I, and an expansion chassis II. A second expansion chassis I requires an expansion power supply.

The mainframe and expansion power supplies are in individual chassis. They connect to a standard 115-volt, 60-Hertz power source. Also available, for European installations, are power supplies for use with 230-volt, 50-Hertz sources.

These power supplies need not be regulated under normal commerical power conditions. With maximum loads, the mainframe power supply draws approximately 15 amperes of ac power, and the expansion power supply, approximately 4 amperes.

Ambient temperature at the installation site can vary between 0 and 50 degrees C with no adverse effects on computer operations. To extend the life expectancy of the computer, however, it is recommended that ambient temperature be maintained between 15 and 30 degrees C.

Relative humidity can be up to 90 percent (without condensation).

1.3 SPACE REQUIREMENTS

The mainframe, expansion chassis, and power supplies are in individual cabinets suitable for rack-mounted or table-top installation. Both the mainframe and the expansion chassis are 10.5 inches (26.6 cm) high, 21 inches (53.1 cm) deep, and 19 inches (48.1 cm) wide. The mainframe power supply is 5.2 inches (13.3 cm) high, 20 inches (50.6 cm) deep, and 19 inches (48.1 cm) wide. The expansion power supply dimensions are identical to the mainframe power supply, except that it is 18 inches (45.5 cm) deep. The standard 33 ASR TTY unit with stand is approximately 33 inches (83.5 cm) high, 19 inches (48.1 cm) deep, and 22 inches (55.7 cm) wide.

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SECTION 2
PHYSICAL DESCRIPTION

2.1 GENERAL

The mainframe and expansion chassis are fabricated from cold-rolled steel with spot-welded construction. The steel is cadmium-plated per military specification QQ-P-416, type II, class 2, for corrosion protection.

The mainframe and expansion chassis each contain six fans mounted on the right side (when viewed from the front) to provide cooling for the electronic components.

2.2 MAINFRAME

The mainframe (assembly drawing 01E0902, volume 2 of this manual) contains:

a. The control panel

b. CPU tray

c. Memory tray

d. Backplane

e. I/O groundplane

2.2.1 Control Panel

The molded-plastic control panel contains all the necessary controls and indicators to operate the computer. The printed-circuit DM254 display card is mounted behind the panel. This card holds the lamps and switches, and associated circuits. The lamps can be replaced without soldering.

The control panel is hinged to the front of the mainframe. To unlatch the panel, press the pushbutton fastener on the left side. The front panel can then be opened (figure II-1) to expose the CPU and memory trays and the I/O groundplane.

The control panel can also be installed up to 25 feet (7.5m) from the mainframe. In this case, the mainframe front panel is blank.

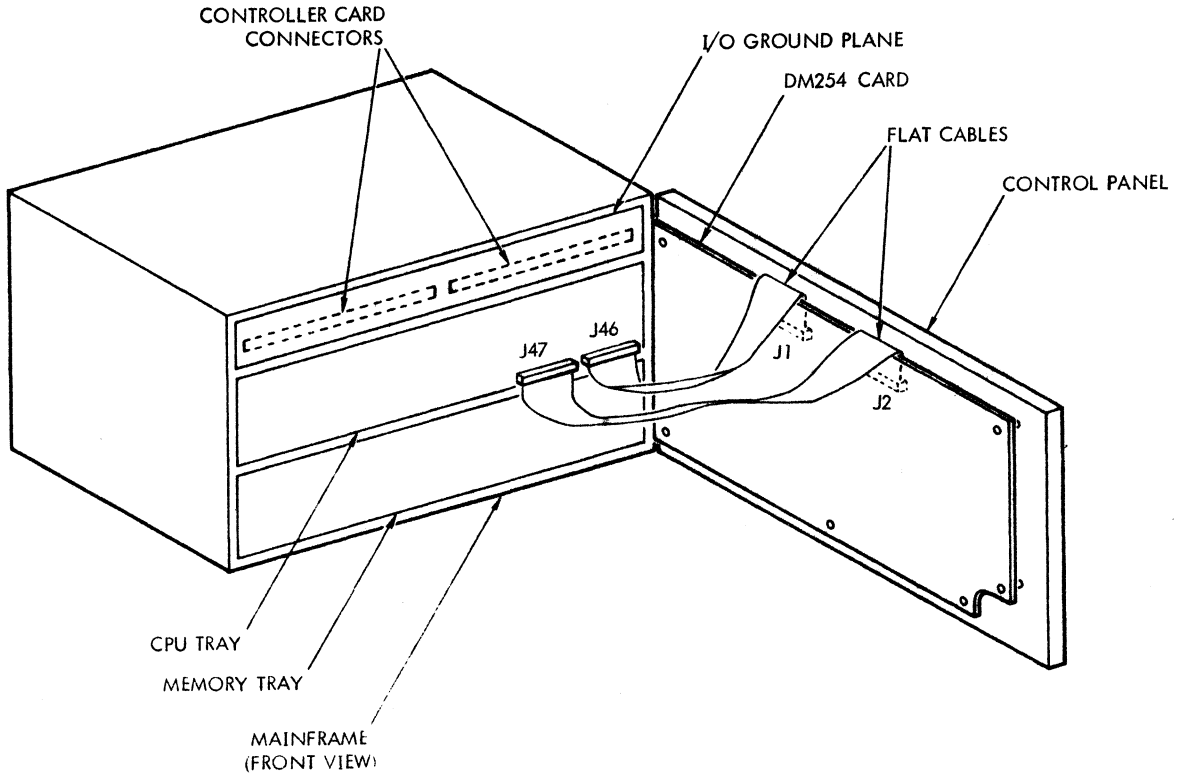

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Figure II-1. Mainframe With Open Control Panel

2.2.2 CPU Tray

As illustrated in figure II-2 the CPU tray (part number 01P0850) has 14 card slots to accommodate CPU and optional circuit cards Table II 1 lists the names and slot locations of the circuit cards in the CPU tray

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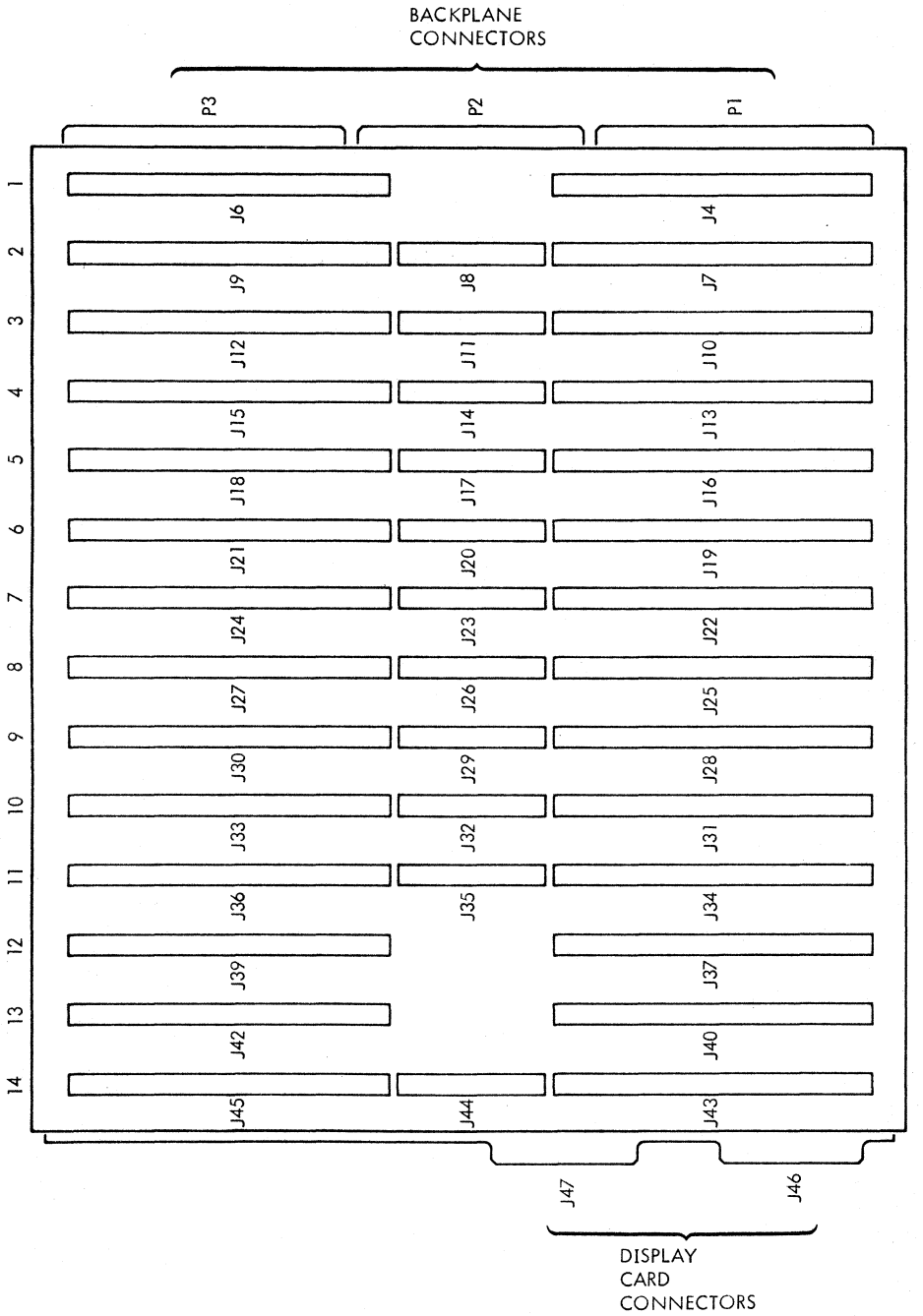

VTII-0968

Figure II-2. Top View of CPU Tray

Table II-1. Card Locations in CPU Tray

Slot	Description	Part No.
1	I/O Control	44P0442
2*	Priority memory access	01A0948
3	I/O data	44P0443
4*	Optional instruction set	44P0444
5	Data loop 12-15	44P0448
6	Data loop 8-11	44P0447
7	Data loop 4-7	44P0446
8	Data loop 0-3	44P0445
9	Control I	44P0449
10	Control II	44P0450
11	Clock (DM253)	44P0440
12*	Memory protection	01A0984
13*	TTY controller and automatic bootstrap loader	
14*	Real-time clock and power failure/restart	

* Card slot for optional circuit card

CPU tray connectors P1, P2, and P3 mate with connectors J8, J9, and J10, respectively, on the mainframe backplane (part number 44P0430) CPU tray connectors J46 and J47 connect to the DM254 display card via flat cables.

To remove the CPU tray from the mainframe:

a. Turn off computer power

b. Open the control panel (section 2.2.1).

c. Disconnect the flat cables from J46 and J47

d Pull out the CPU tray.

For maintenance, an extender cable connects P1, P2, and P3 to backplane connectors J8, J9, and J10. The CPU tray can then be extended forward through and firmly attached to the front of the mainframe with a tray extender assembly that is bolted to the front of the mainframe. Remove the card retainer bar and install the circuit card to be accessed on a

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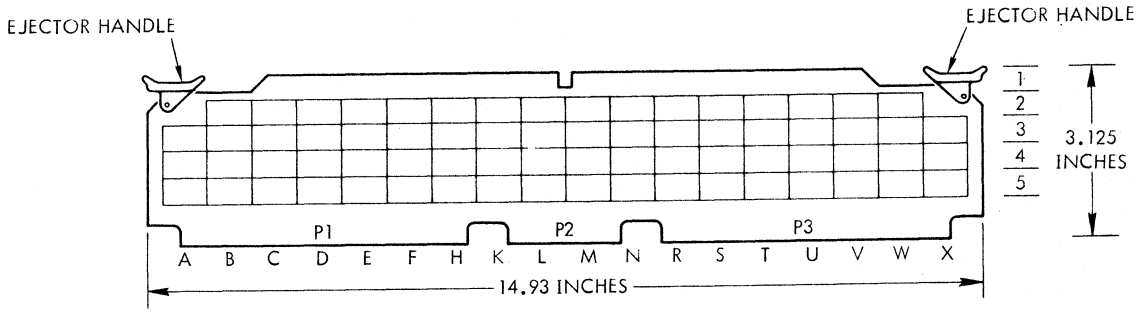
DM265 extender card (part number 44P0437). With the CPU tray and the circuit card in this configuration, the computer can be turned on to begin troubleshooting.

The type of circuit card in the CPU tray is illustrated in figure II-3. Component locations are identified by alphanumeric coordinates. To install a card, insert it into the mounting guides of the designated slot with the component side of the card toward the backplane connectors. Apply moderate pressure to the card, forcing the three card-edge connectors to seat firmly in their mating connectors in the CPU tray. To remove a card, lift the inside edge of the ejector handles to unseat the card from the mating connectors; then lift the card from that slot.

2.2.3 Memory Tray

The mainframe memory tray contains a master memory module (part number 01P0779). As illustrated in figure II-4, the memory module consists of four circuit cards that are approximately 18 inches (45.5 cm) long and 15.6 inches (39.5 cm) wide. An 8K module requires no more space than a 4K module; both consists of four circuit cards. The memory circuit cards (figure II-4) are:



VTII-0969

Figure II-3. Typical Circuit Card in CPU Tray

a. Card 1 - Timing control and register, DM261 (part number 44P0417)

b. Card 2 - Driver and switch, DM257 (part number 44P0411)

c. Card 3 - Inhibit/sense, DM256 (part number 44P0410-000 for 4K, 44P0410-001 for 8K)

d. Card 4 - Memory stack (part number 50S0008-000 for 4K, 50S0008-002 for 8K)

The memory module interconnects with the computer through the mainframe backplane. Memory tray connectors P4, P5, and P6 mate with connectors J16, J17, and J18, respectively, on the backplane. Figure II-5 illustrates the layout of the memory module connectors.

The DM261 card attaches to a rigid frame that rides on the mainframe chassis slides, so that the memory tray can be installed and removed. P4, P5, and P6, which connect to the backplane, are on the DM261 card. This card also contains two right-angle connectors (P8 and P9), which serve as receptacles for a short printed-circuit (PC) card. The PC card terminates wires that connect to the card-edge connectors on the three remaining memory circuit cards. This interconnected wiring allows each circuit card to be disconnected from the memory module without unsoldering wires.

To remove the memory circuit cards:

a. Detach the hinged pins.

b. Unscrew the interconnect-cable connector holddown screws.

c. Unplug the card from the interconnect-cable connector.

The four memory circuit cards are tied together during operation by five through bolts on the forward end (opposite the connector end). In addition, standoff spacers are located between modules for vibration suppression

The memory tray can be removed and attached to the front of the mainframe in the same manner as the CPU tray (section 2.2.2). The memory cards are mounted with hinges so that they can be opened. For troubleshooting, open a card to a convenient position and hold it firmly with a support brace.

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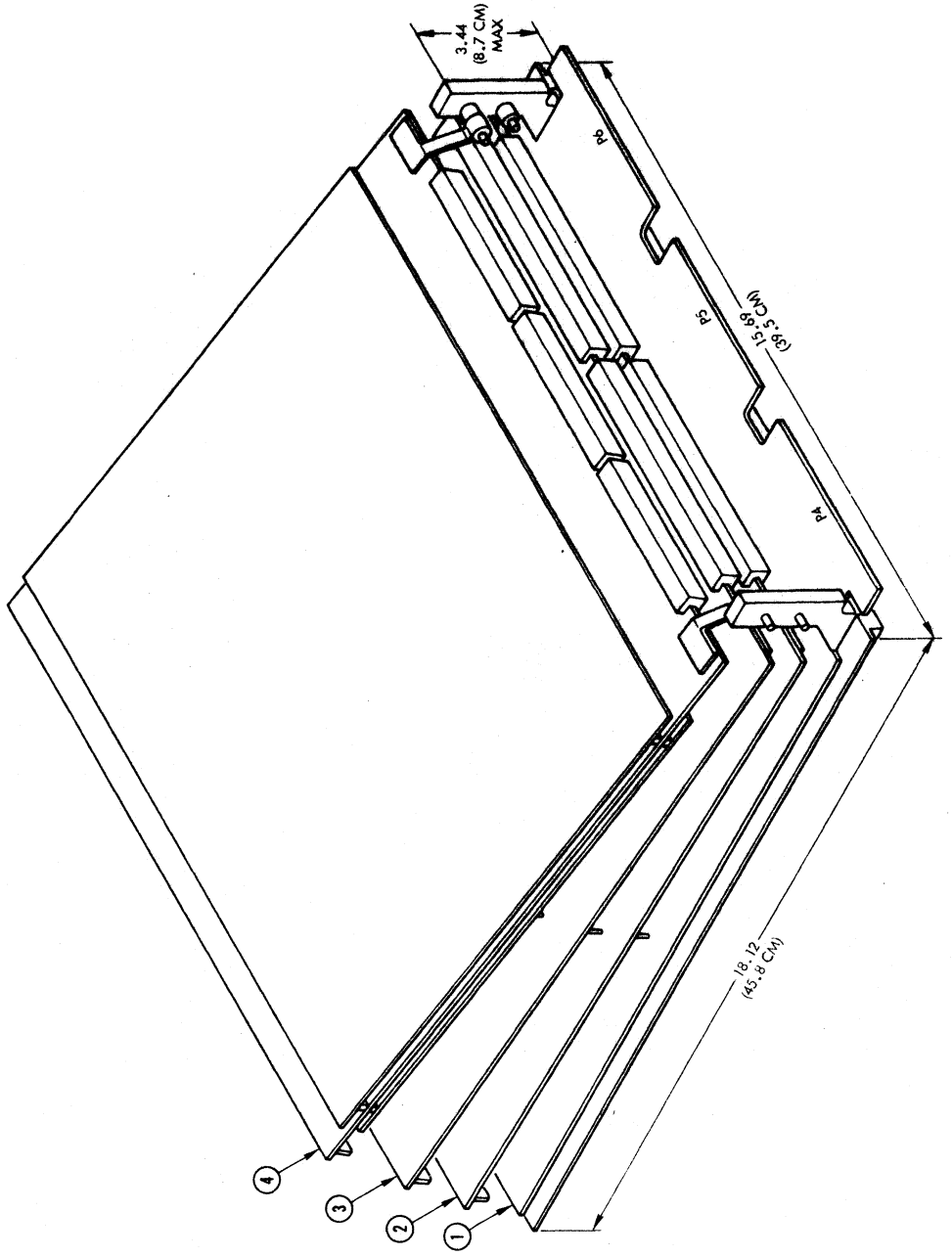

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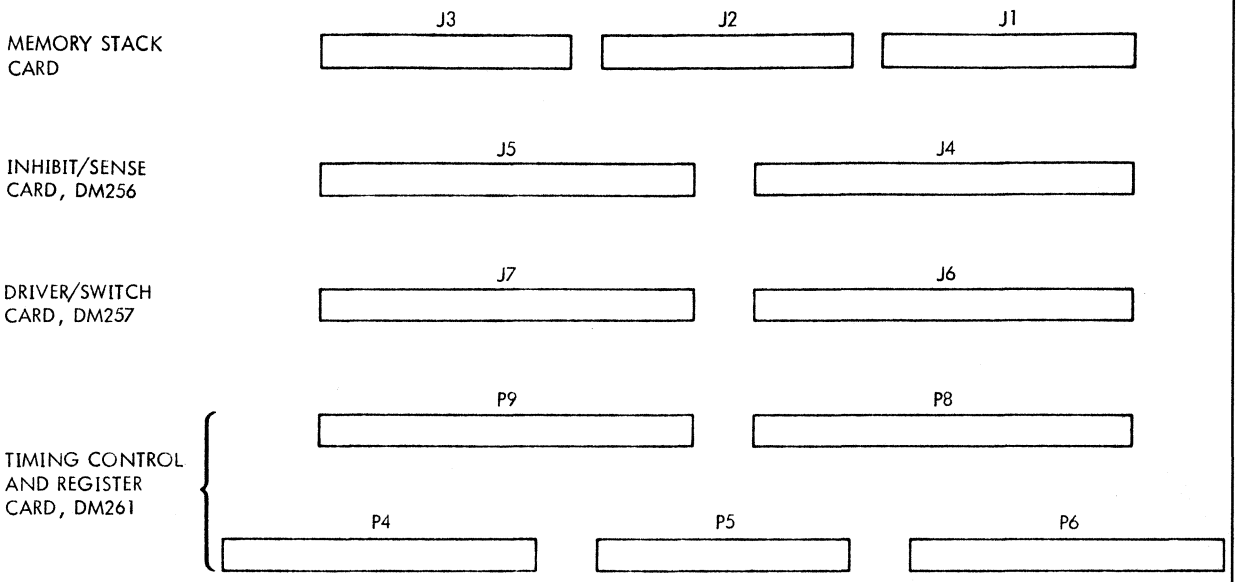
Figure II-4. Master Memory Module



NOTE: THE CONNECTOR DESIGNATIONS IN THIS ILLUSTRATION ARE REFERENCED AT THE MEMORY MODULE LEVEL; THE INDIVIDUAL CIRCUIT CARD ASSEMBLIES HAVE DIFFERENT CONNECTOR DESIGNATIONS.

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Figure II-5. Master Memory Module Connector Layout

2.2.4 Backplane

The DM260 backplane (part number 44P0430) is a PC board at the rear of the mainframe. As illustrated in figure II-6, the backplane contains connectors that interconnect the mainframe with external chassis and equipment. The backplane connectors are listed in table II-2.

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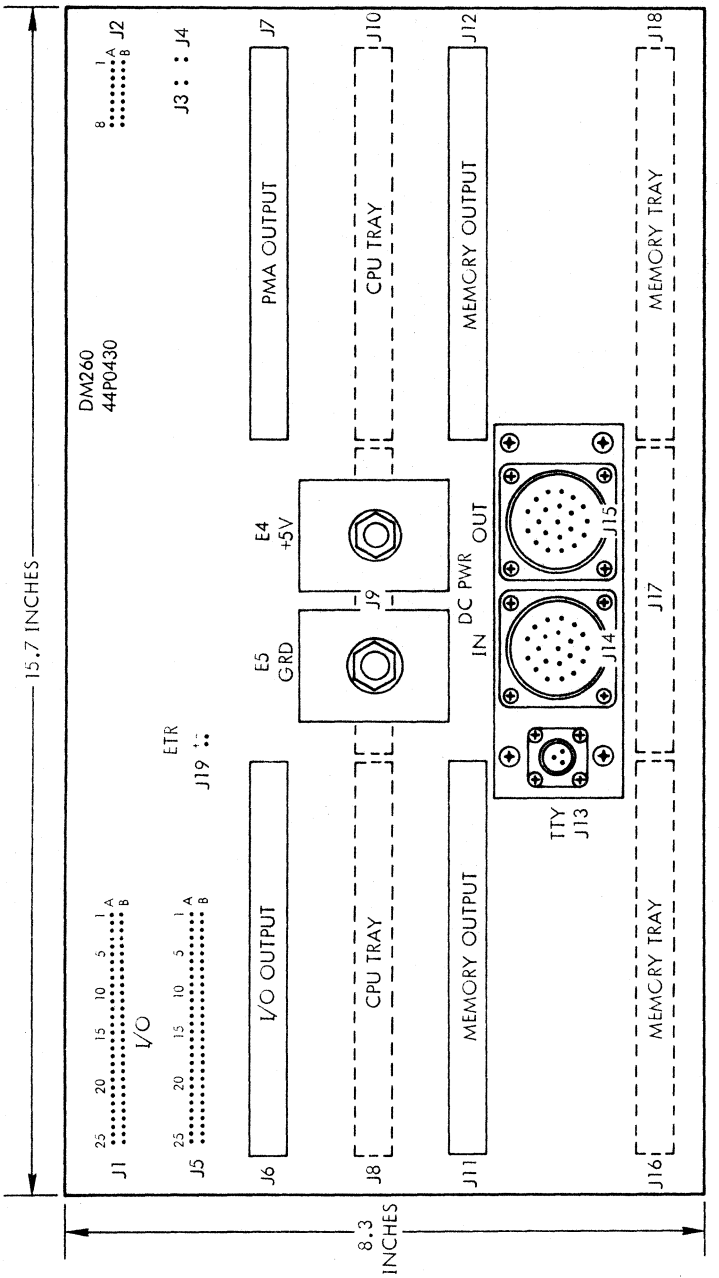

NOTE: CONNECTORS J8, J9, J10, J16, J17, AND J18 ARE MOUNTED ON THE OTHER SIDE OF BACKPLANE.

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Figure II-6. Mainframe Backplane (DM260)

Table II-2. DM260 Backplane Connectors

Connector	Name	Description
J1	I/O	Contains two rows of 25 pins. Connects to flat I/O cable that routes I/O signals and interrupt (PIM) lines to the I/O groundplane of the mainframe.
J2	I/O Power	Contains two rows of eight pins. Connects to flat I/O power cable that routes the required power to the I/O groundplane of the mainframe.
J3	Ext +12V	Contains two pins. Allows an external 12 volt source to be connected to the mainframe.
J4	Ext -12V	Contains two pins. Allows an external -12 volt source to be connected to the mainframe.
J5	I/O	Contains two rows of 25 pins. Connects to flat I/O cable that routes I/O signals to the I/O groundplane of the mainframe.
J6	I/O Output	Contains two rows of 50 pins. Connects to an I/O termination shoe (44P0489) or an I/O expansion cable (53P0494) that routes I/O signals to an expansion chassis.
J7	PMA Output	Contains two rows of 50 pins. Connects to a PMA cable (53P0513) that routes signals from the PMA circuit in the mainframe to the I/O groundplane in expansion chassis I.
J8	CPU Tray	Contains two rows of 50 pins. Connects to P1 of CPU tray.
J9	CPU Tray	Contains two rows of 40 pins. Connects to P2 of CPU tray.
J10	CPU Tray	Contains two rows of 50 pins. Connects to P3 of CPU tray.

Table II-2. DM260 Backplane Connectors *(continued)*

Connector	Name	Description
J11	Memory Output (left)	Contains two rows of 50 pins. Connects to a left-hand memory termination shoe (44P0485) or a memory expansion cable (53P0471) that routes memory signals to an expansion chassis.
J12	Memory Output (right)	Contains two rows of 50 pins. Connects to a right-hand memory termination shoe (44P0486) or a memory expansion cable (53P0464) that routes memory signals to an expansion chassis.
J13	TTY	Contains three pins. Connects to teletype cable that routes transmit, receive, and return signals to the teletype unit. The part number for the cable used with a model 33 ASR is 53P0157; for the cable used with models 35 ASR and 33 KSR, 53P0266).
J14	DC Power In	Contains 21 pins. Connects to power supply cable (53P0479) that routes all voltages, except +5 volts, from the power supply to the mainframe.
J15	DC Power Out	Contains 21 pins. Connects to expansion power cable (53P0466) that routes all voltages, except +5 volts, to an expansion chassis.
J16	Memory Tray	Contains two rows of 50 pins. Connects to P4 of memory tray.
J17	Memory Tray	Contains two rows of 40 pins. Connects to P5 of memory tray.
J18	Memory Tray	Contains two rows of 50 pins. Connects to P6 of memory tray.
J19	ETR	Allows an external time reference to be connected to the mainframe.

Table II-2. DM260 Backplane Connectors *(continued)*

Connector	Name	Description
E1, E2, and E3	Jumper Terminals	These terminals are jumpered for the routing of internal or external ± 12 volts in the mainframe.
E4	Grd	Provides a return for the +5 volts. Connects to a 6-gage battery cable (53P0478-000) that routes the return between the power supply and mainframe.
E5	+5V	Terminal for +5 volts. Connects to a 6-gage battery cable (53P0478-001) that routes +5 volts between the power supply and mainframe.

2.2.5 I/O Groundplane

The I/O groundplane (part number 01P0904) is in the mainframe (figure II-7). Two 7-3/4-by-12-inch peripheral controller cards or PIM and BIC cards can be installed in 122-pin connectors J16 and J17 of the I/O groundplane.

Install the circuit cards by inserting them through the rear of the mainframe into the mounting guides with the component side of the card facing up. Apply moderate pressure to the card, forcing the 122-terminal card-edge connector to seat firmly in its mating connector on the I/O groundplane. The pressure applied to the card during insertion should be equally distributed to prevent damage to the I/O connector or to the nylon guides.

Two flat I/O cables and a flat I/O power cable (part number 53S1080-002) are routed from the DM260 backplane to the front side (opposite the side containing 122-pin connectors) of the I/O groundplane. The cables are fanned out at the I/O groundplane and connect to Berg terminals. I/O groundplane connectors J18 and J19 contain two rows of 8 pins; they route BIC and PIM signals, respectively.

2.3 EXPANSION CHASSIS I

Expansion chassis I contains a front panel, memory tray, backplane, and I/O groundplane (drawing 01E0927, volume 2).

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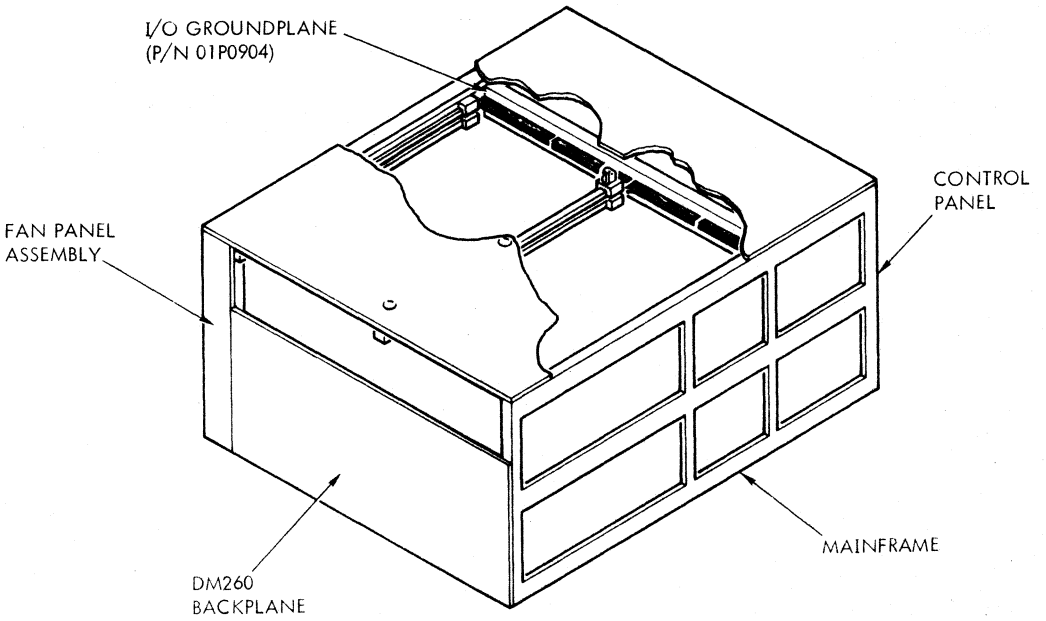
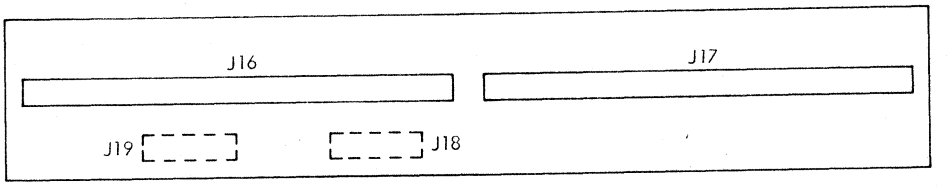


(a) LOCATION OF I/O GROUNDPLANE IN MAINFRAME



(b) CONNECTOR LAYOUT OF I/O GROUNDPLANE

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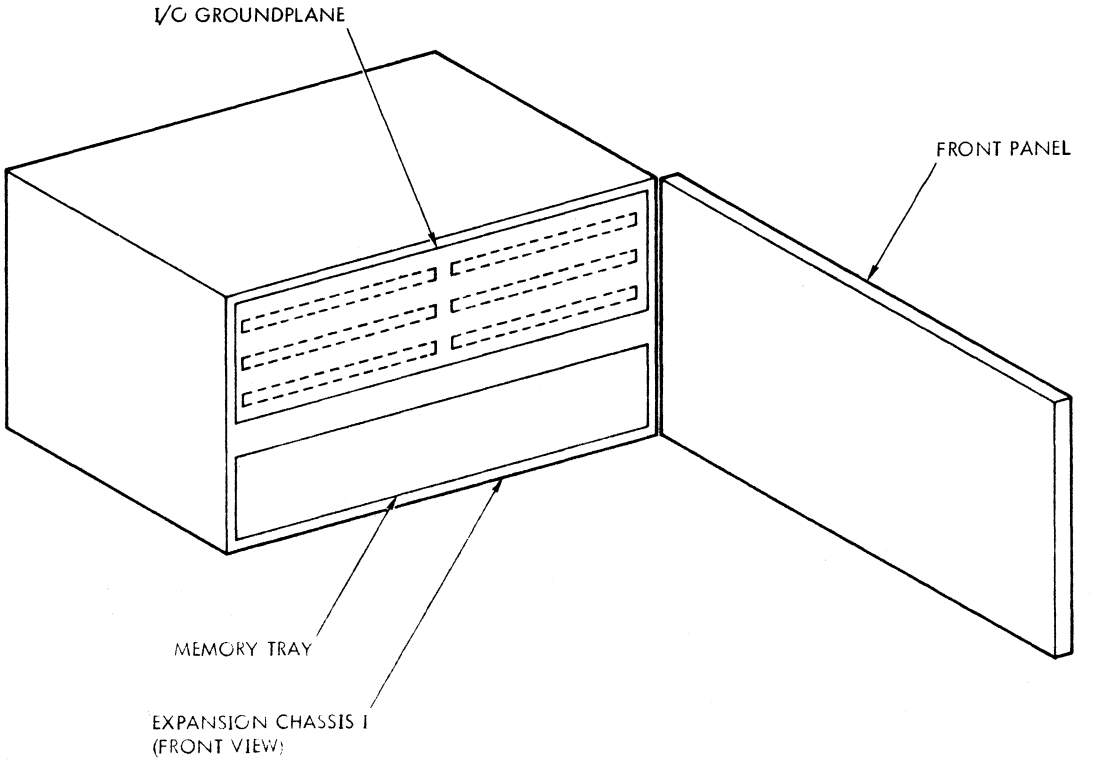
Figure II-7. Mainframe I/O Groundplane



VTII-0975

Figure II-8. Expansion Chassis I With Front Panel Open

2.3.1 Front Panel

The front panel is blank and mounted on hinges. To unlatch the front panel, press the pushbutton fastener on the left side. The panel swings open (figure II-8) to expose the memory tray and the I/O groundplane.

2.3.2 Memory Tray

The memory tray of expansion chassis I contains a slave memory module (part number 01P0926). This memory module is the same as the master module except it does not contain a DM261 timing control and register card. Replacing the DM261 card is a short PC card containing card-edge connectors P4, P5, and P6, which interconnect the slave memory module to backplane connectors J19, J20, and J21 (figure II-9). Installation and circuit card accessibility is identical to that of the master memory module.

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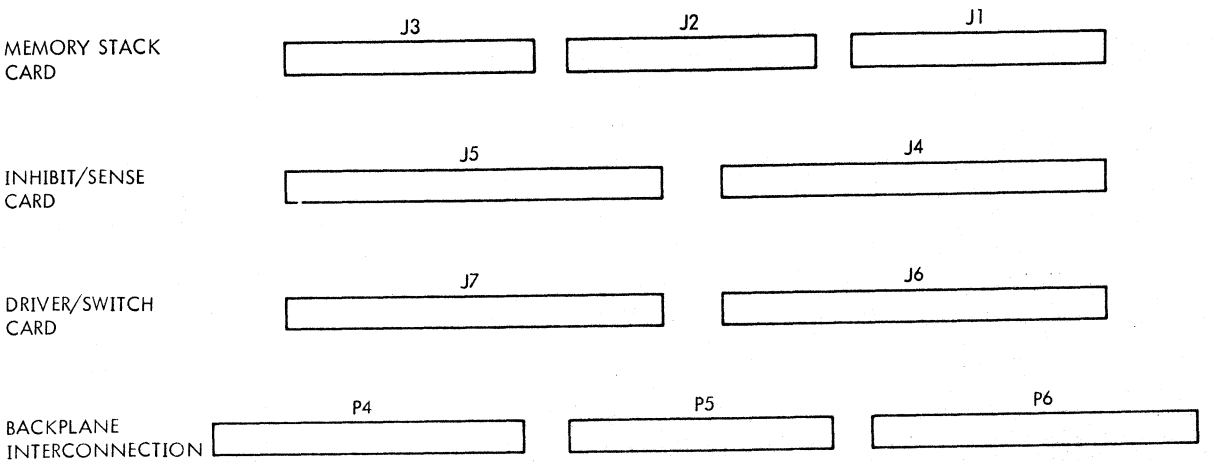
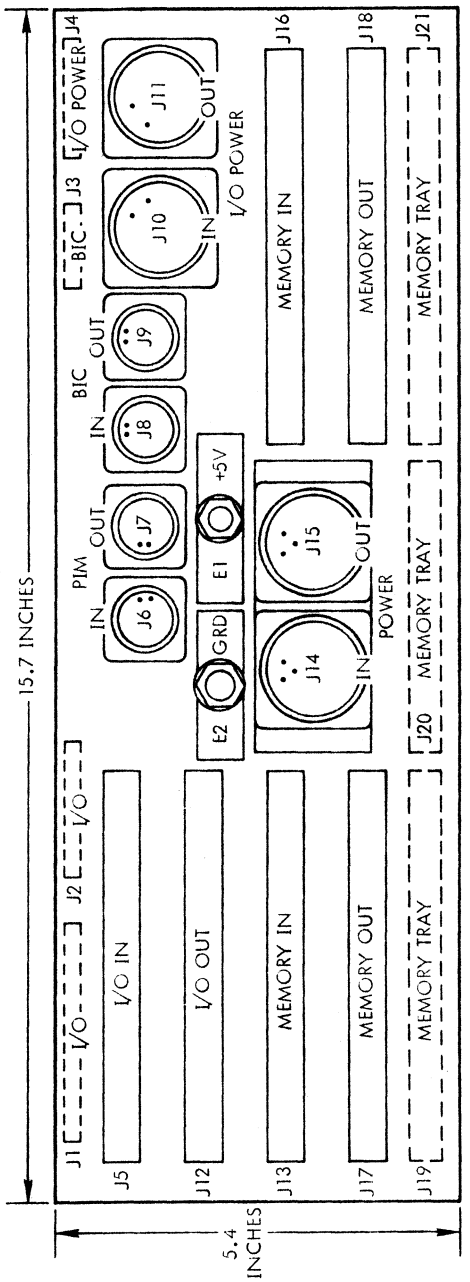


VTII-0976

Figure II-9. Connector Layout of Slave Memory Module

2.3.3 Backplane

The DM276 PC backplane board (part number 44P0476) is located at the rear of expansion chassis I. The backplane contains connectors for interconnecting expansion chassis I with external chassis and equipment (figure II-10). The backplane connectors are listed in table II-3.



NOTE: CONNECTORS J1, J2, J3, J4, J19, J20, AND J21 ARE MOUNTED ON THE OTHER SIDE OF BACKPLANE.

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Figure II-10. Expansion Chassis I Backplane

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Table II-3. DM276 Backplane Connectors

Connector	Designation	Description
J1	I/O	Contains two rows of 25 pins and connects to the flat I/O cable that routes I/O signals to the I/O groundplane.
J2	I/O	Contains two rows of 25 pins and connects to the flat I/O cable that routes I/O signals and PIM lines to the I/O groundplane.
J3	BIC	Contains two rows of eight pins and connects to the flat BIC cable that routes BIC signals to the I/O groundplane.
J4	I/O Power	Contains two rows of 16 pins and connects to the flat I/O power cable that routes dc power to the I/O groundplane.
J5	I/O In	Contains two rows of 50 pins and connects to the I/O expansion cable (53P0494) that routes I/O signals from the mainframe or another expansion chassis.
J6	PIM In	Contains 18 pins and connects to either the PIM 1 cable (53P0514) or PIM 2 cable (53P0515) that routes PIM interrupt lines from a PIM card or another expansion chassis.
J7	PIM Out	Contains 18 pins and connects to the PIM 2 cable (53P0515) that routes PIM interrupt lines to another expansion chassis.

Table II-3. DM276 Backplane Connectors *(continued)*

Connector	Designation	Description
J8	BIC In	Contains 18 pins and connects to either the BIC 1 cable (53P0516) or BIC 2 cable (53P0517) that routes BIC/peripheral interface signals from a BIC card or another expansion chassis.
J9	BIC Out	Contains 18 pins and connects to either a BIC termination shoe or the BIC 2 cable (53P0517) that routes BIC/peripheral interface signals to another expansion chassis.
J10	I/O Power In	Contains 21 pins and connects to the dc power cable for peripheral controllers. The cable comes from power-out connectors on this or another expansion chassis.
J11	I/O Power Out	Contains 21 pins and connects to the cable (53P0479) that routes dc voltages to peripheral controllers in another expansion chassis.
J12	I/O Out	Contains two rows of 50 pins and connects to the I/O expansion cable (53P0494) that routes I/O signals to another expansion chassis.
J13	Memory In (left)	Contains two rows of 50 pins and connects to the left-hand memory expansion cable (53P0471) that routes memory signals from the mainframe or another expansion chassis.
J14	Power In	Contains 21 pins and connects to the expansion power cable (53P0466) that routes dc memory voltages (except +5 volts) from the mainframe or another expansion frame.

Table II-3. DM276 Backplane Connectors *(continued)*

Connector	Designation	Description
J15	Power Out	Contains 21 pins and connects to the expansion power cable (53P0466) that routes dc memory voltages (except +5 volts) to another expansion chassis. It can also connect to a cable that routes dc voltages to I/O power-in connector J10.
J16	Memory In (right)	Contains two rows of 50 pins and connects to the right-hand memory expansion cable (53P0464) that routes memory signals from the mainframe or another expansion chassis.
J17	Memory Out (left)	Contains two rows of 50 pins and connects to either a left-hand memory termination shoe (44P0485) or the memory expansion cable (53P0471) that routes memory signals to another expansion chassis.
J18	Memory Out (right)	Contains two rows of 50 pins and connects to either a right-hand memory termination shoe (44P0486) or the memory expansion cable (53P0464) that routes memory signals to another expansion chassis.
J19	Memory Tray	Contains two rows of 50 pins and connects to P4 on the memory tray.
J20	Memory Tray	Contains two rows of 40 pins and connects to P5 on the memory tray.
J21	Memory Tray	Contains two rows of 50 pins and connects to P6 on the memory tray.

Table II-3. DM276 Backplane Connectors *(continued)*

Connector	Designation	Description
E1	+5 Volts	Terminal for +5 volts; connects to one or two 6-gage battery cables (53P0478-001) that route +5 volts from the mainframe or expansion chassis.
E2	Grd	Ground terminal that connects to or two 6-gage battery cables (53P0478-000) that provide a return for +5 volts.

2.3.4 I/O Groundplane

Figure II-11 illustrates the location of the I/O groundplane (part number 01P0975) in expansion chassis I. Six 7.75-by-12-inch (19.7 x 30 cm) peripheral controller cards can be installed in the 122-pin connectors (J25 through J30) of the I/O groundplane. Installation procedures are the same as described in section 2.2.5.

Two flat I/O cables and a flat I/O power cable (part number 53S1080-002) go from the DM276 backplane to the front side (the side opposite the 122-pin connectors) of the I/O groundplane. The cables fan out at the I/O groundplane and connect to Berg terminals. I/O groundplane connectors J31 and J32 contain two rows of eight pins and route BIC and PIM signals, respectively.

2.4 EXPANSION CHASSIS II

Expansion chassis II contains a front panel, two memory trays, a backplane, and I/O groundplane (drawing 01E0929, volume 2).

The front panel and memory trays of expansion chassis II are identical to those of expansion chassis I, and the I/O groundplane is identical to that of the mainframe. The memory trays and groundplane are exposed when the front panel is open (figure II-12).

The DM269 backplane (part number 44P0460) PC board is located at the rear of expansion chassis II. The backplane connectors interconnect expansion chassis II with external chassis and equipment (figure II-13).

Table II-4 lists the backplane connectors.

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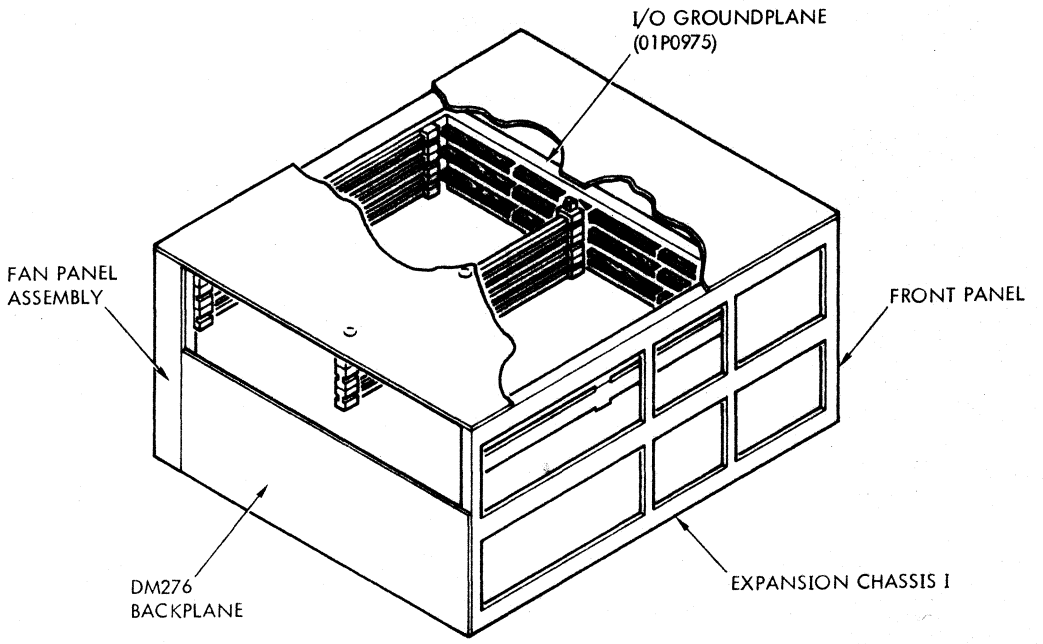
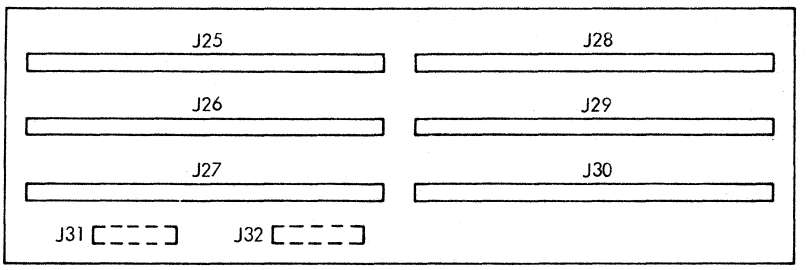


(a) LOCATION OF I/O GROUNDPLANE IN EXPANSION CHASSIS I



(b) CONNECTOR LAYOUT OF I/O GROUNDPLANE

VTI-0978

Figure II-11. Expansion Chassis I Groundplane

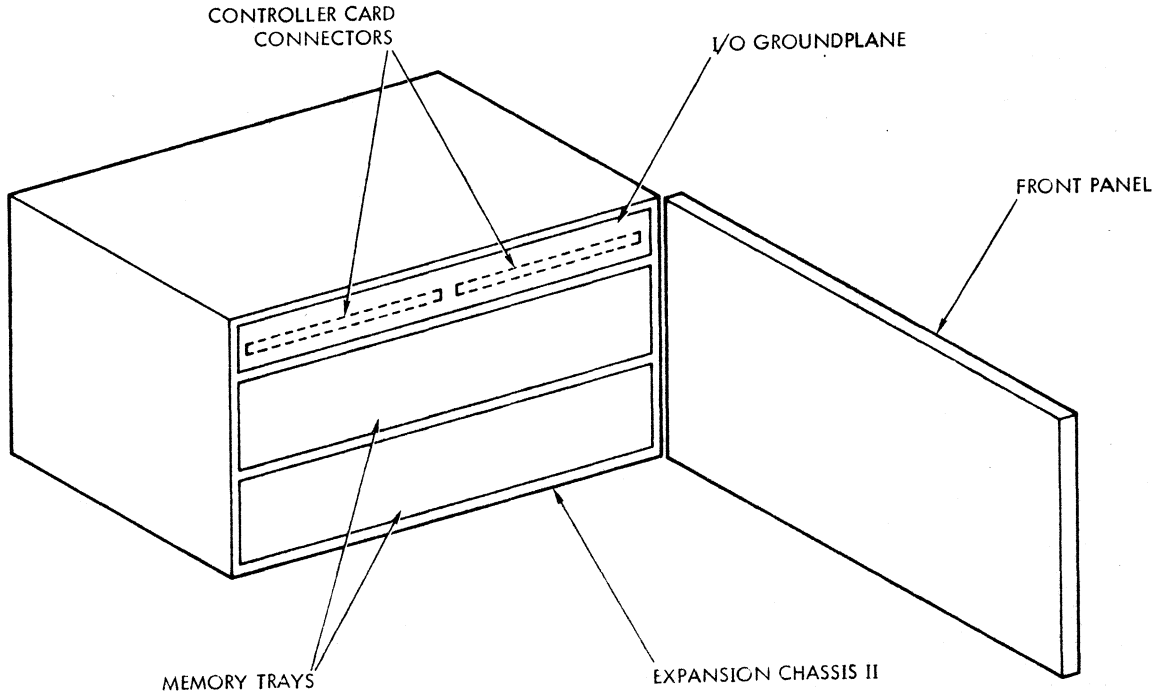


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Figure II-12. Expansion Chassis II With Front Panel Open

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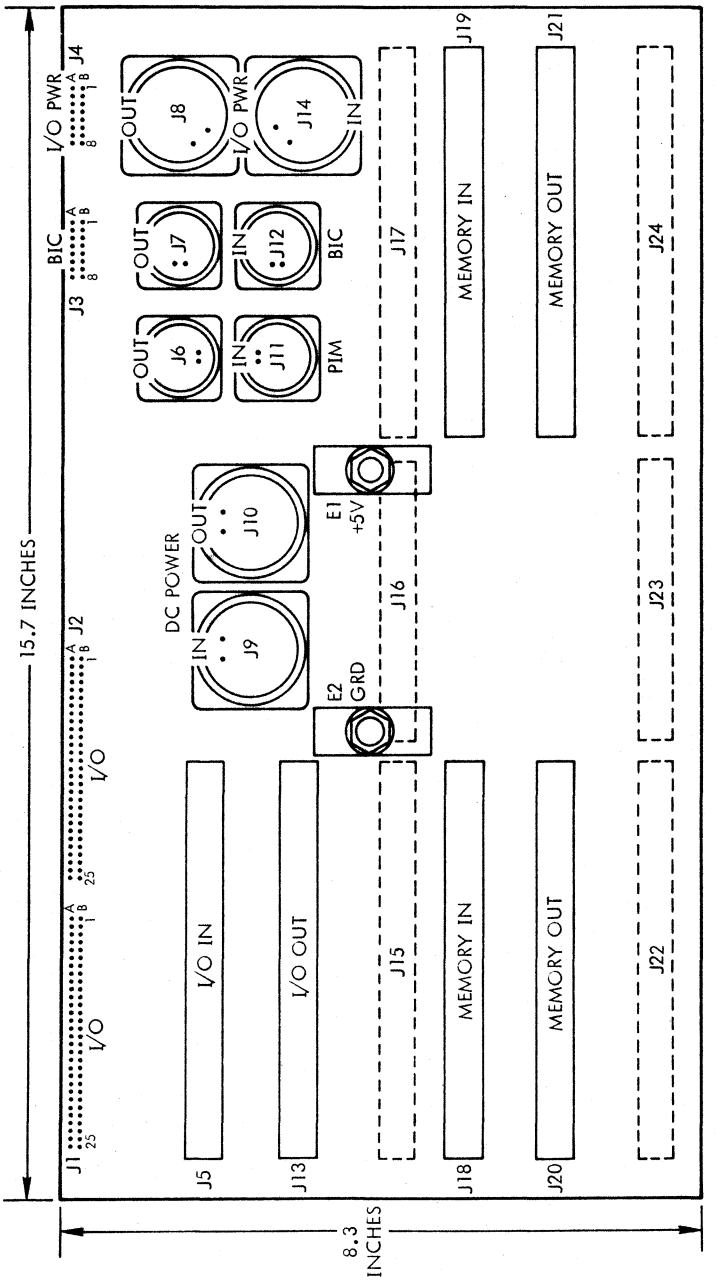

NOTE: CONNECTORS J15, J16, J17, J22, J23, AND J24 ARE MOUNTED ON THE OTHER SIDE OF BACKPLANE.

VTI1-0980

Figure II-13. Expansion Chassis II Backplane

Table II-4. DM269 Backplane Connectors

Connector	Designation	Description
J1	I/O	Contains two rows of 25 pins and connects to the flat I/O cable that routes I/O signals to the I/O groundplane.
J2	I/O	Contains two rows of 25 pins and connects to the flat I/O cable that routes I/O signals and PIM lines to the I/O groundplane.
J3	BIC	Contains two rows of eight pins and connects to the flat BIC cable that routes BIC signals to the I/O groundplane.
J4	I/O Power	Contains two rows of eight pins and connects to the flat I/O power cable that routes dc power to the I/O groundplane.
J5	I/O In	Contains two rows of 50 pins and connects to the I/O expansion cable (53P0494) that routes I/O signals from the mainframe or another expansion chassis.
J6	PIM Out	Contains 18 pins and connects to the PIM 2 cable (53P0515) that routes PIM interrupt lines to another expansion chassis.
J7	BIC Out	Contains 18 pins and connects to either a BIC termination shoe or the BIC 2 cable (53P0517) that routes BIC/peripheral interface signals to another expansion chassis.

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Table II-4. DM269 Backplane Connectors *(continued)*

Connector	Designation	Description
J8	I/O Power Out	Contains 21 pins and connects to the cable (53P0479) that routes dc voltages to peripheral controllers in another expansion chassis.
J9	Power In	Contains 21 pins and connects to the expansion power cable (53P0466) that routes all dc memory voltages (except +5 volts) from the mainframe or another expansion chassis.
J10	Power Out	Contains 21 pins and connects to the expansion power cable (53P0466) that routes all dc memory voltages (except +5 volts) to another expansion chassis. It can also connect to the cable that routes dc voltages to I/O power-in connector J14.
J11	PIM In	Contains 18 pins and connects to either the PIM 1 cable (53P0514) or the PIM 2 cable (53P0515) that routes PIM interrupt lines from a PIM card or another expansion chassis.
J12	BIC In	Contains 18 pins and connects to either the BIC 1 cable (53P0516) or the BIC 2 cable (53P0517) that routes BIC/peripheral interface signals from a BIC card or another expansion chassis.
J13	I/O Out	Contains two rows of 50 pins and connects to the I/O expansion cable (53P0494) that routes I/O signals to another expansion chassis.
J14	I/O Power In	Contains 21 pins and connects to the cable that contains dc voltages for

Table II-4. DM269 Backplane Connectors *(continued)*

Connector	Designation	Description
		peripheral controllers. The cables come from power-out connectors on this or another expansion chassis.
J15	Memory Tray	Contains two rows of 50 pins and connects to P4 of top memory tray.
J16	Memory Tray	Contains two rows of 40 pins and connects to P5 of top memory tray.
J17	Memory Tray	Contains two rows of 50 pins and connects to P6 of top memory tray.
J18	Memory In (left)	Contains two rows of 50 pins and connects to the left-hand memory expansion cable (53P0471) that routes memory signals from the main-frame or another expansion chassis.
J19	Memory In (right)	Contains two rows of 50 pins and connects to the right-hand memory expansion cable (53P0464) that routes memory signals from the main-frame or another expansion chassis.
J20	Memory Out (left)	Contains two rows of 50 pins and connects to the left-hand memory termination shoe (44P0485) or the memory expansion cable (53P0471) that routes memory signals to an-other expansion chassis.
J21	Memory Out (right)	Contains two rows of 50 pins and connects to either a right-hand memory termination shoe (44P0486) or the memory expansion cable (53P0464) that routes memory sig-nals to another expansion chassis.
J22	Memory Tray	Contains two rows of 50 pins and

Table II-4. DM269 Backplane Connectors *(continued)*

Connector	Designation	Description
		connects to P4 on the bottom memory tray.
J23	Memory Tray	Contains two rows of 40 pins and connects to P5 on the bottom memory tray.
J24	Memory Tray	Contains two rows of 50 pins and connects to P6 on the bottom memory tray.
E1	+5 Volts	Terminal for +5 volts; connects to one or two 6-gage battery cables (53P0478-001) that route +5 volts from the mainframe or expansion chassis.
E2	Grd	Ground terminal that connects to one or two 6-gage battery cables (53P0478-000) that provide a return for the +5 volts.

2.5 MAINFRAME POWER SUPPLY

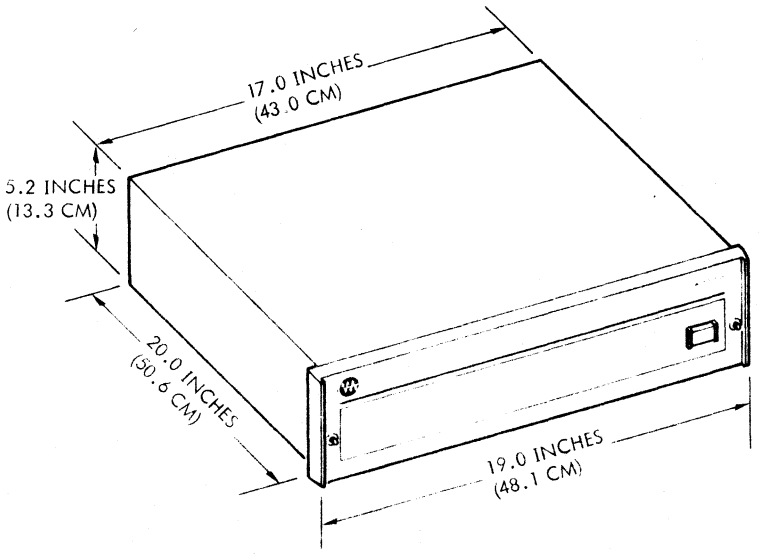
The mainframe power supply provides total power required by the mainframe and expansion chassis I and II. The power supply (figure II-14) is contained in a standard rack-mountable chassis which is 19 inches (48.1 cm) wide, 20.0 inches (50.6 cm) deep, and 5.2 inches (13.3 cm) high. A fan in the rear of the chassis provides cooling for the electronic components of the power supply. The power supply contains a front panel and a connector panel.

2.5.1 Front Panel

The mainframe front panel contains two pushbutton fasteners and a power-on indicator.

Removal of the front panel is accomplished by pressing the pushbutton fasteners on each side of the panel and lifting.

The power-on indicator illuminates when the on/off switch (located on the connector panel) is turned on.



VTII-0993

Figure II-14. 620/f Mainframe Power Supply

2.5.2 Connector Panel

The connector panel is located at the rear of the mainframe power supply, and contains various controls, cables, and connectors (figure II-15). These connectors and cables are described in table II-5.

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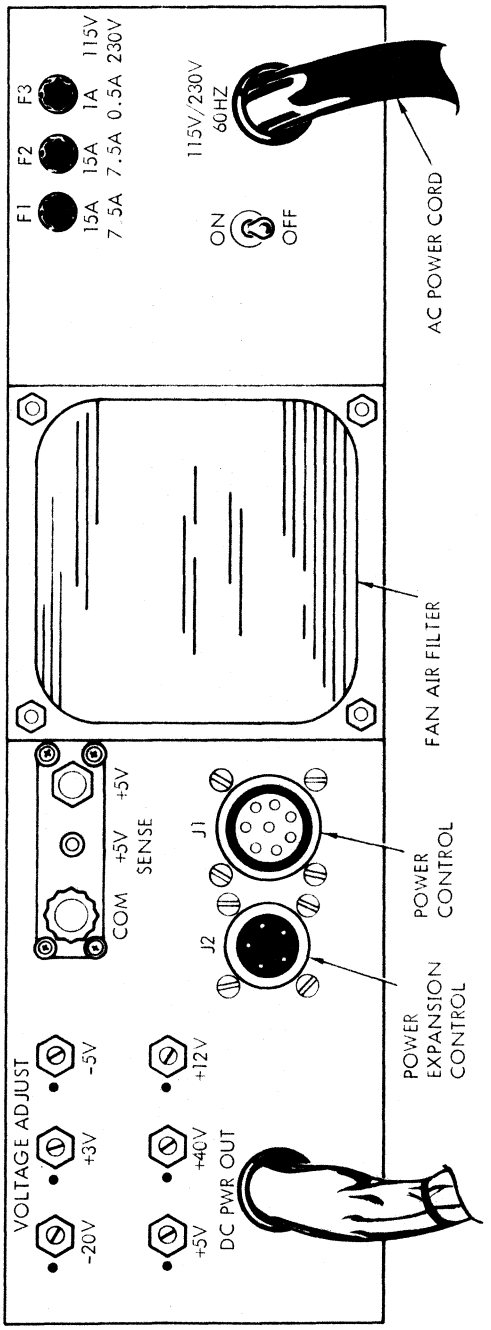

VTII-0994

Figure II-15. Mainframe Power Supply Connector Panel

Table II-5. Mainframe Power Supply Connector Panel

Connector	Description
+5V	The +5V terminal connects to a 6-gage battery cable (53P0478-001) that routes the +5 volts to the mainframe.
+5V Sense	The +5V sense input terminal provides a remote sensing capability when connected to a remote sense cable (53P0462). If remote sensing is not used, the +5V sense terminal is jumpered to the +5V terminal.
Com	The common terminal provides a return for the +5 volts. It connects to a 6-gage battery cable (53P0478-000) that is routed to the ground terminal (E4) on the mainframe.
DC Pwr Out	The dc output cable (P2) routes -20V, +12V, -5V, +40V, +3V, thermistor programming, power failure output and feedback input, and common sense return signals to the mainframe. The dc output cable (53P0479) is hardwired at the power supply end and connects to J14 on the mainframe backplane.
J1	The power control connector is an eight-pin connector that mates with an ac power cable. The ac power cable routes the 24-volt ac and 115-volt ac lines to connector J1 on the mainframe fan panel assembly (01P0903). The 24-volt line provides computer power on/off control and the 115-volt line operates the fans.
J2	The power expansion control connector connects to a cable that routes power on/off control signals to the expansion power supply.
ON/OFF	The on/off switch controls the application of ac input to the power supply.

Table II-5. Mainframe Power Supply Connector Panel *(continued)*

Connector	Description
Power Cord	A standard three-conductor power cable that routes ac voltage to the power supply.

2.6 EXPANSION POWER SUPPLY

To be supplied (not available for preliminary edition).

SECTION 3
SYSTEM INTERCONNECTION

3.1 INTRODUCTION

The system is interconnected by cables that mate with connectors at the rear of the mainframe and expansion chassis. Figure II-16 identifies external connectors on the mainframe and expansion chassis backplanes. A typical system interconnection is illustrated in figure II-17.

3.2 MEMORY EXPANSION INTERCONNECTION

Two memory expansion cables, left-hand cable (53P0471) and right-hand (53P0464), are required for each expansion chassis containing memory. The left-hand memory cable connects J11 on the mainframe to either J18 on the expansion chassis II (model 620/f-011) or J13 on the expansion chassis I (model 620/f-010). The right-hand memory cable connects J12 on the mainframe to either J19 on the expansion chassis II (model 620/f-011) or J16 on the expansion chassis I (model 620/f-010). Memory expansion cables also interconnect two expansion chassis (memory-out connector to memory-in connector).

The maximum length of memory expansion cable in a system is 3 feet (94.1 cm). In a system consisting of a mainframe and two expansion chassis containing memory, the length of the memory expansion cables between chassis is 1.5 feet (47.0 cm). The connector at each end of the memory expansion cables consists of a 100-pin printed-circuit (PC) card. The same type of memory expansion cable is used for both the read/write memory and the read-only memory. Memory termination shoes are installed on the memory-out connectors (J20 and J21 or J17 and J18) of the last expansion chassis of the system. The left-hand memory termination shoe is part number 44P0485, and the right-hand, 44P0486.

3.3 I/O EXPANSION INTERCONNECTION

One I/O expansion cable (53P0494) is required for the interconnection of each expansion chassis containing I/O controller cards. The I/O expansion cable connects I/O connector J6 on the mainframe to I/O-in connector J5 on expansion chassis I or II. The same type of I/O expansion cable also connects any two expansion chassis (I/O-out connector to I/O-in connector). Total length of I/O expansion cables can be up to 20 feet (6m). Each I/O cable contains a 100-pin PC card connector at each end. An I/O termination shoe (44P0489) goes on the I/O-out connector of the last expansion chassis of the system.

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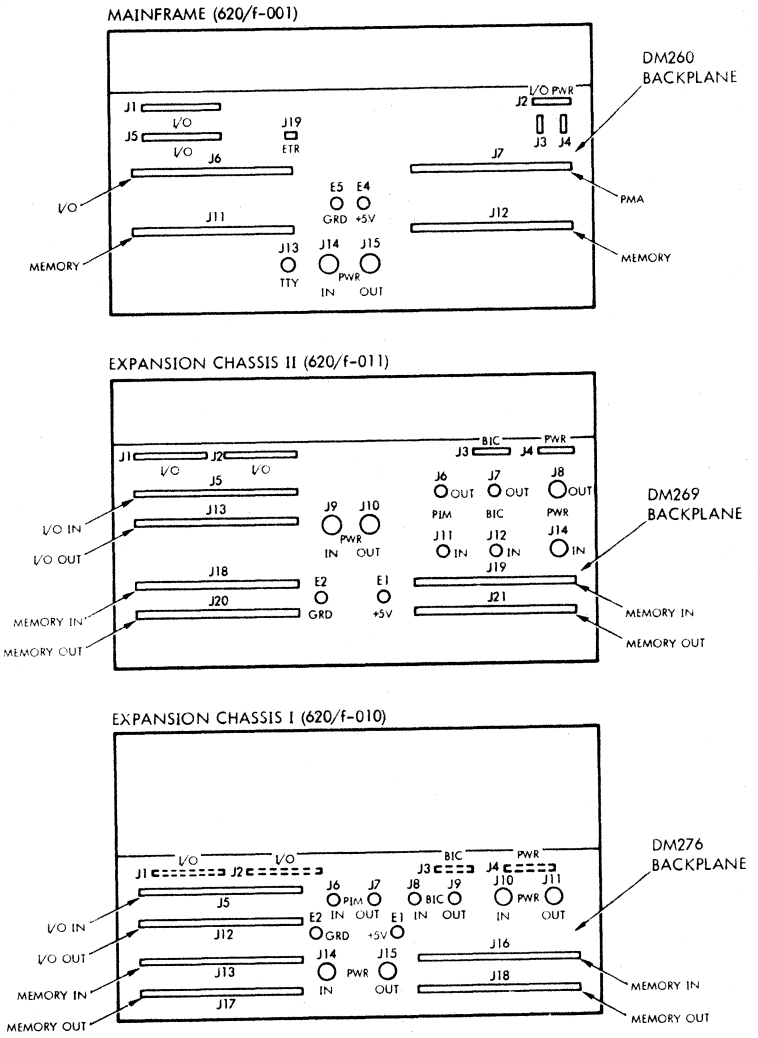

VTI2-0204

Figure II-16. Mainframe and Expansion Chassis Backplane Connectors

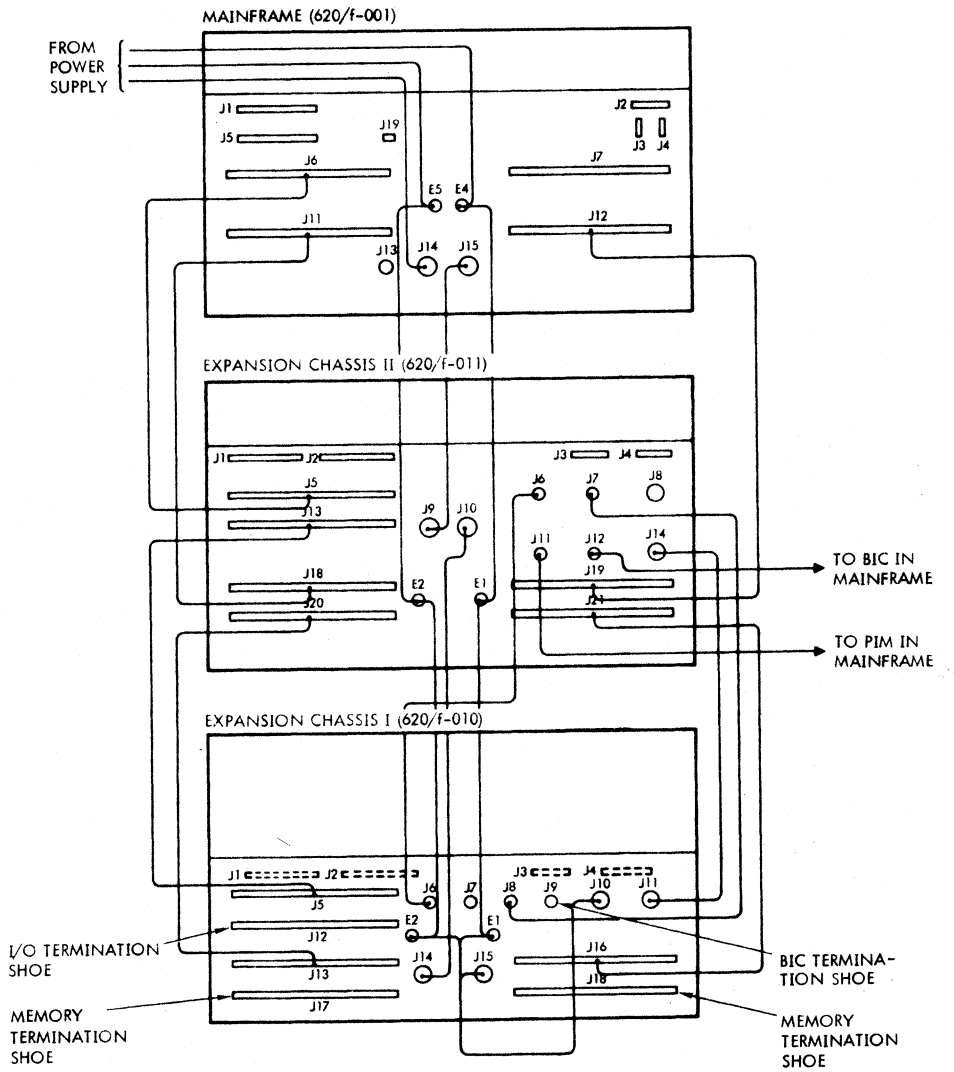

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Figure II-17. Typical System Interconnection

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At the mainframe, the I/O lines routed through connector J6 connect, via etched conductors, to connectors J1 and J5. J1 and J5 (50-pin Berg connectors) connect to two flat I/O cables. As illustrated in figure II-18, the flat I/O cables routed in the mainframe to the front of the I/O ground plane are fanned out and connected with Berg pins to E bus pins. The other side of the I/O ground plane contains two circuit-card connectors that accommodate I/O controller cards.

At expansion chassis II, the I/O lines routed through connector J5 connect, via etched conductors, to connectors J1 and J2. J1 and J2 (50-pin Berg connectors) connect to two flat I/O cables. As illustrated in figure II-19, the flat I/O cables routed in expansion chassis II to the front of the I/O ground plane are fanned out and connected with Berg terminals to E bus pins. The other side of the I/O ground plane contains two circuit-card connectors that accommodate I/O controller cards.

At expansion chassis I, the I/O lines routed through connector J5 connect, via etched conductors, to connectors J1 and J2 (mounted on the other side of the DM276 backplane). J1 and J2 (50-pin Berg connectors) connect inside the expansion chassis I to two flat I/O cables. As illustrated in figure II-20, the flat I/O cables routed in expansion chassis I to the front of the I/O ground plane are fanned out and connected with Berg

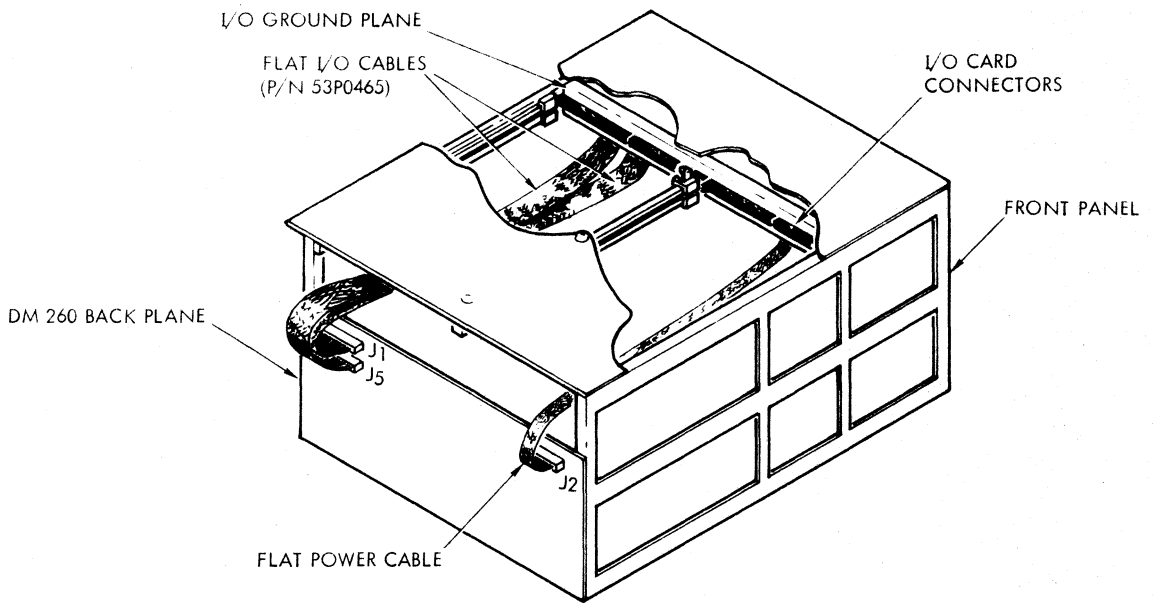

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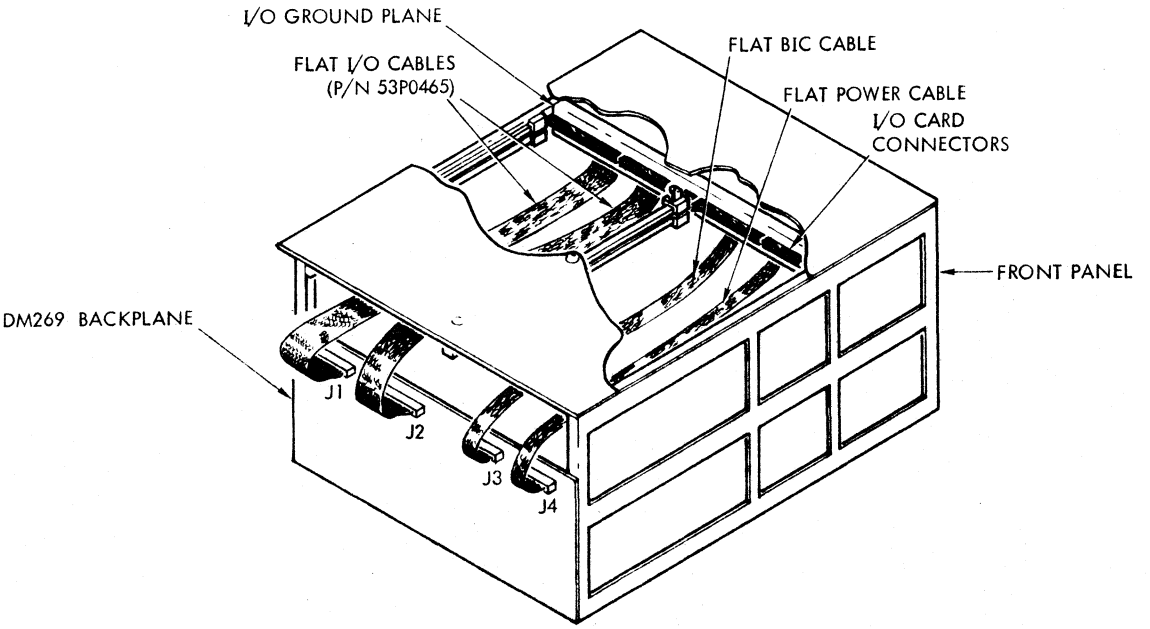
Figure II-18. Internal Cables in Mainframe (620/f-001)



VTII-0914

Figure II-19. Internal Cables in Expansion Chassis II (620/f-011)

terminals to E bus pins. The other side of the I/O ground plane contains six circuit-card connectors that accommodate I/O controller cards.

3.4 POWER SUPPLY INTERCONNECTION

Power for the CPU tray, 32K memory, and ten peripheral controller cards can be supplied by one mainframe power supply. As illustrated in figure II-17, three cables connect the power supply and the mainframe. One cable (53P0479) routes all voltages, except +5 volts, to the mainframe. This cable is 2.5 feet (65.9 cm) long and mates with a 21-pin connector (J14) on the mainframe. Two 6-gage battery cables, 2 feet (60.5 cm) long each, supply +5 volts and ground to the mainframe. The +5-volt cable (53P0478-001) and ground cable (53P0478-000) connect to the mainframe at terminal studs E4 and E5, respectively.

To route power to expansion memories (figure II-17), expansion power cables connect from mainframe power connectors E4, E5, and J15 to expansion chassis connectors E1, E2, and J9 (or J14), respectively. The expansion power cable (53P0466), which provides all voltages except +5 volts, is 2.5 feet (65.9 cm) long with a 21-pin connector at each end. This cable connects the power-out connector (J15) on the mainframe to power-in connectors (J9 or J14) on expansion chassis. The expansion power cable can also connect the power-out connector (J10 or J15) of an expansion chassis to the power-in connector

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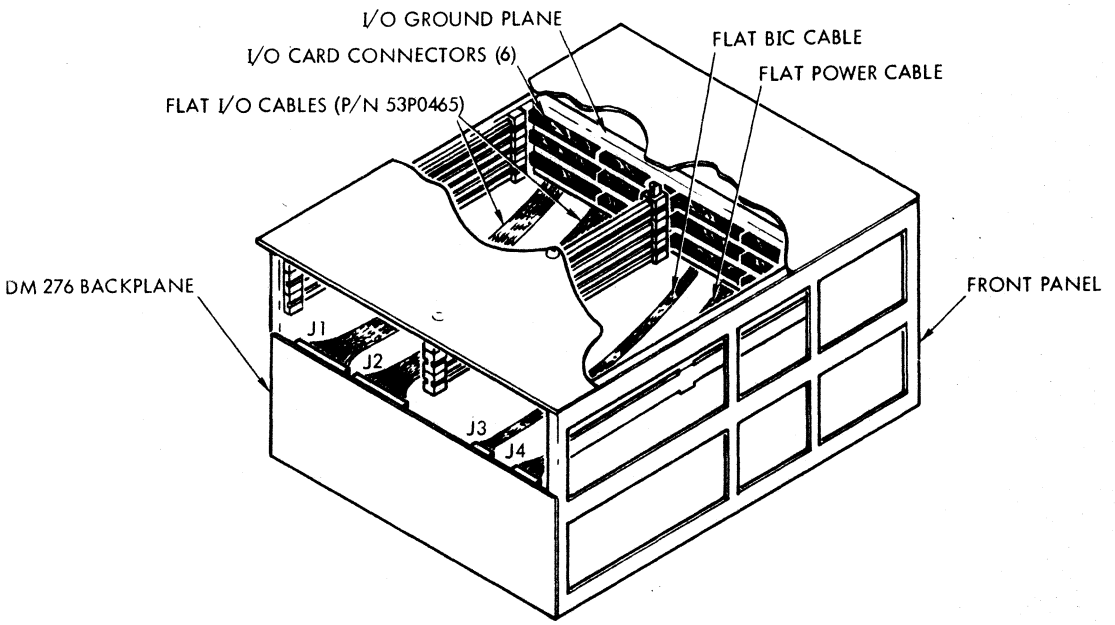

VTII-0915

Figure II-20. Internal Cables in Expansion Chassis I (620/f-010)

(J9 or J15) of a second expansion chassis. The expansion power cables for +5 volts (53P0478-001) and ground (53P0478-000) are 6-gage battery cables, 2 feet (60.5 cm) long, with terminal lugs at each end. These cables connect mainframe terminals E4 and E5 to expansion chassis terminals E1 and E2, respectively; they can also route +5 volts and ground between two expansion chassis.

Power for peripheral controller cards in the mainframe is routed to the I/O ground plane in a flat power cable that connects to a 16-pin Berg connector J2 (figure II-18). The voltages are routed to connector J2 via etched conductors from J15, E4, and E5.

Power for peripheral controller cards in the expansion chassis is routed through one cable that connects from the three power connectors (E1, E2, and J15 or J10) to I/O-power-in connector J10 on expansion chassis I or J14 on expansion chassis II (figures II-16 and II-17). The dc power lines routed through I/O-power-in connectors J14 and J10 are connected via etched conductors to power-out connectors J8 and J11, respectively (figure II-16). To supply dc power to I/O controller cards in the second expansion chassis, a 2.5-foot (65.9 cm) I/O power cable (53P0479) connects the I/O-power-out connector of one expansion chassis to the power-in connector of the second expansion chassis (figure II-17). All power-in and power-out connectors contain 21 pins. In each expansion chassis backplane, the dc power lines are routed to Berg connector J4 via etched conductors (in

expansion chassis I, J4 is mounted on the other side of backplane). As illustrated in figures II-19 and II-20, J4 connects to a flat power cable that routes dc power to the expansion chassis I/O ground plane.

Figure II-21 illustrates a mainframe power supply connected to a computer system with 32K of memory. An ac power cable connects power supply connector J1 and connector J1 on the fan panel assemblies of the mainframe and expansion chassis. For 32K and 28K computer systems, the ac power cable (53P0521-024) is a single cable containing four connectors 2 feet apart. For computer systems with less than 28K of memory, two other ac power cables are required and are listed as follows:

a. Systems with 4K or 8K of memory use ac power cable 53P0502-024.

b. Systems with 12K, 16K, 20K, or 24K of memory use ac power cable 53P0503-024.

The ac power cable contains the computer power on/off control signal and 115 volts to operate the fans.

An expansion control cable is connected to J2 of the mainframe power supply when an expansion power supply is required. The expansion control cable routes on/off control signals to the expansion power supply.

More that ten peripheral controller cards in a system require an additional expansion chassis I and an expansion power supply. A typical computer system containing more than ten peripheral controller cards is illustrated in figure II-22. In this example, the second expansion chassis I is interconnected with an I/O expansion cable (connects to I/O-in connector J5) and a cable from an expansion power supply (connects to I/O power-in connector J10).

3.5 PIM INTERCONNECTION

The optional priority interrupt module (PIM) has eight interrupt lines (IL00 through IL07) for connection with up to eight peripheral controllers. PIM interconnection consists of connecting these interrupt lines to selected peripheral controller cards thus providing them with interrupt capabilities on a priority basis. For peripheral controllers that are located in the same computer chassis as the PIM, the interrupt lines are connected on the I/O ground plane. For peripheral controllers located in a different chassis, the interrupt line connections are routed through external interrupt cables.

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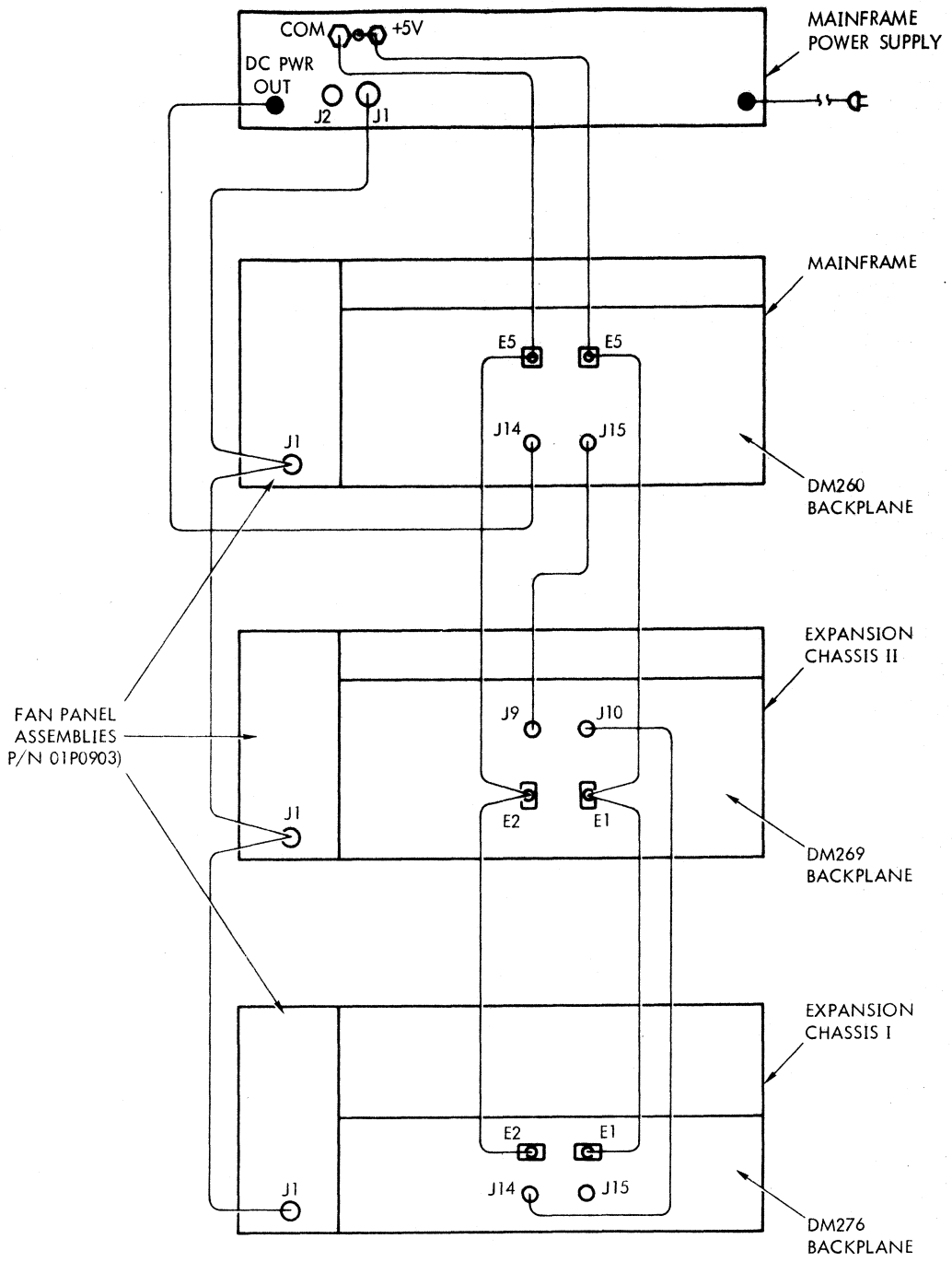
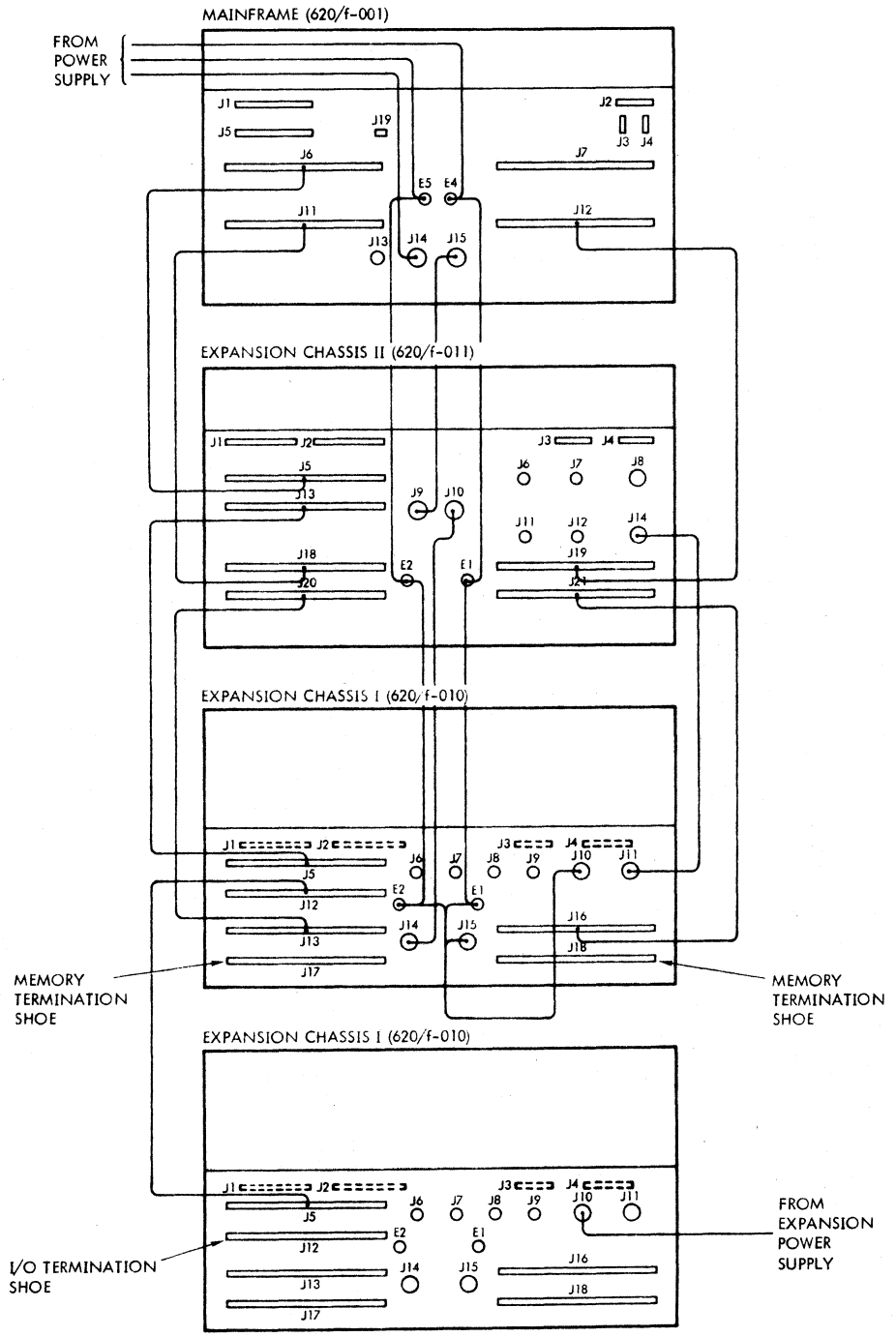


VTII-0995

Figure II-21. Power Connections for 32K Systems



VTI2-0206

Figure II-22. Typical Interconnection Using Expansion Power Supply

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The PIM card is normally installed in one of the I/O card slots of the mainframe. The interrupt lines are routed to the peripheral controller cards in expansion chassis as follows (figure II-17): A PIM 1 cable (53P0514) connects to one of 44-pin card-edge connectors J1 or J2 (parallel-wired) of the PIM card. The other end of the cable connects to PIM-in connector J11 on the expansion chassis II or J6 on the expansion chassis I. Interrupt lines are routed between two expansion chassis via a PIM 2 cable (53P0515) with an 18-pin connector at each end. This cable connects a PIM-out connector (J6 or J7) of one expansion chassis to a PIM-in connector (J11 or J6) of a second expansion chassis. All expansion chassis PIM connectors are 18-pin connectors. Total length of interrupt cables can be 20 feet (6m).

In the mainframe and expansion chassis, the interrupt lines are routed from the backplane to the I/O ground planes via the flat I/O cable. In the mainframe, the interrupt lines are in the flat cable that connects to Berg connector J1 (figure II-18); in the expansion chassis, they are in the flat cable that connects to Berg connector J2 (figures II-19 and II-20).

3.6 BIC INTERCONNECTION

Control signal routing for the optional buffer interlace controller (BIC) is divided into two parts. One part consists of BIC/computer interface signals; the other, BIC/peripheral interface signals (B cable signals). For a BIC in the mainframe, the BIC/computer interface signals are routed via the I/O ground plane in the mainframe. For a BIC in an expansion chassis, the BIC/computer interface signals are routed to the mainframe via the I/O expansion cable. For a BIC connected to a peripheral controller (or controllers) in the same computer chassis, the B cable signals are routed via the I/O ground plane; if the BIC is in another chassis, the B cable signals are routed via an external B cable.

Up to four BICs can be installed in a system. When two or more BICs are located in the same chassis, the B cable lines are only connected to the peripheral controller (or controllers) with which each BIC is communicating. B cable lines are not installed between two BICs.

A typical BIC interconnection is illustrated in figure II-17. In this example, the BIC card (which is installed in one of the I/O card slots of the mainframe) is connected to peripheral controllers located in the two expansion chassis. A BIC 1 cable (53P0516) connects to one of the 44-pin card-edge connectors J1 and J2 (parallel-wired) of the BIC card. The other end of the BIC 1 cable connects to BIC-in connector J12 on the expansion chassis II. The B cable signals are routed to peripheral controllers in the expansion chassis I via a BIC 2 cable (53P0517) with an 18-pin connector at each end. The BIC 2 cable

connects BIC-out connector J7 on the expansion chassis II to BIC-in connector J8 on the expansion chassis I. BIC-out connector J9 on the expansion chassis I is terminated with a BIC termination shoe because it is the last BIC connector in the illustrated system.

Except for Berg connector J3, the expansion chassis BIC connectors contain 18 pins. The BIC cables contain eight twisted pairs and are as short as the system configuration permits. The B cable signals are routed to the I/O ground plane of the expansion chassis in a flat cable that connects Berg connector J2 (figures II-19 and II-20). The signals are routed to the J3 connectors via etched conductors from the BIC-out connectors.

3.7 PMA INTERCONNECTION

The optional priority memory access (PMA) allows up to eight peripheral devices direct access to the 620/f memory. The controllers for the peripheral devices can only be installed in the I/O card slots of the expansion chassis I (model 620/f-010). PMA interconnection consists of routing signals from the PMA circuit in the mainframe to the I/O ground plane in the expansion chassis I.

As illustrated in figure II-23, a PMA cable (53P0513) connects 100-pin card-edge connector J7 on the mainframe to circuit card connectors on the I/O ground plane of the expansion chassis I. The PMA lines on the I/O ground plane must also be terminated with a PMA termination shoe. The PMA cable is 2.5 feet (67.9 cm) long if the expansion chassis I is located directly under the mainframe; however, the cable can be up to 20 feet (6m) long if required (approximately 2 feet (60.5 cm) of cable are used inside the expansion chassis I).

3.8 CABLE PIN ASSIGNMENTS

To be supplied (not available for preliminary edition).

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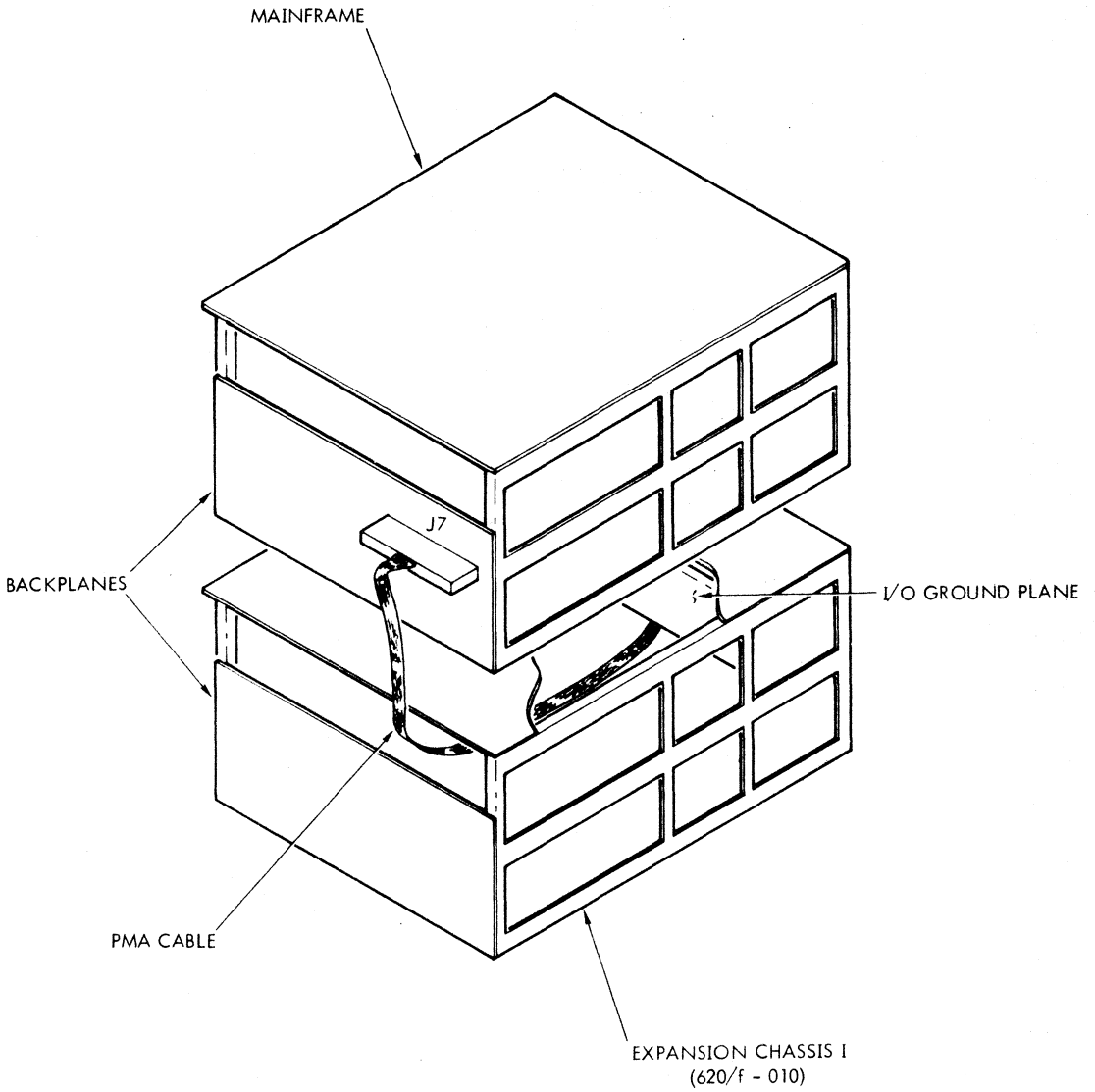

VTII-0916

Figure II-23. PMA Interconnection

SECTION 4
SYSTEM INTERRUPT PRIORITY

To be supplied (not available for preliminary edition).

SECTION 1
OPERATING PROCEDURES

This section describes the procedures that prepare the computer system for use. These procedures include power on, bootstrap loader program, and the binary load/dump program.

When a new system is being initialized, or when the contents of memory are unknown, make a cold start:

a. Turn the power switch key to PWR ON.

b. Load the bootstrap loader program, either manually (see below and sections 2.2.6.2 and 3.3) or, if the system contains an automatic bootstrap, automatically (section 2.2.3).

c. Load the paper tape binary load/dump program provided. Use a 33/35 ASR Teletype reader or a Remex RS0302RB high-speed reader.

To load the bootstrap loader manually:

a. Load instruction 054000 in the I register.

b. Place REPEAT in the up position, and set STEP/RUN to STEP.

c. Load the starting memory address (0x7756) of the bootstrap loader into the P register.

NOTE

The letter x in the memory address of the bootstrap loader represents any digit 0 through 7, depending on the size of the computer memory, for example, 0 for 4K, 1 for 8K, 2 for 12K, 3 for 16K, 4 for 20K, 5 for 24K, 6 for 28K, and 7 for 32K.

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SYSTEM OPERATION

d. Load the following instruction codes in the A register manually (sections 2.2.6.2 and 3.3), pressing START after loading each instruction. The computer loads the A register contents into the address specified by the P register, which is incremented by one after each instruction is loaded.

Address	Paper Tape Reader Code	TTY Code	Mnemonic
0x7756	102637	102601	CIB
0x7757	004011	004011	ASLB
0x7760	004041	004041	LRLB
0x7761	004446	004446	LLRL
0x7762	001020	001029	JBZ
0x7763	0x7772	0x7772	Memory address
0x7764	055000	055000	STA
0x7765	001010	001010	JAZ
0x7766	0x7600	0x7600	Memory address
0x7767	005144	005144	IXR
0x7770	005101	005101	INCR
0x7771	100537	102601	CIB
0x7772	101537	101201	SEN
0x7773	0x7756	0x7756	Memory address
0x7774	001000	001000	JMP
0x7775	0x7772	0x7772	Memory address

To determine that the bootstrap loader has been correctly loaded, perform the following steps.

a. Initialize the CPU by pressing RESET.

b. Clear all registers by momentarily pressing each register switch, pressing RESET each time.

c. Load instruction 014000 (load A relative to P) in the I register.

d. Load the starting memory address (0x7756) in the P register. Keep REPEAT in the up position.

e. Select the A register and press STEP. The contents of each memory address is sequentially displayed each time STEP is pressed.

f. If an error is found, reload the erroneous instruction codes into memory.

NOTE

The P register error address is always the error address plus one.

The 620/f is now ready for use. The next section explains the switches and indicators on the control console, and the following section gives the manual loading procedure.

Appendix A is an alphabetical index of the 620/f internal instructions, and appendix B lists the I/O instructions.

CHAPTER III
SYSTEM OPERATION

SECTION 2
SWITCHES AND INDICATORS

2.1 GENERAL

Figure III-1 shows the switches and indicators on the control panel of the 620/f computer. Their uses are discussed individually in the following subsections.

The front panel of the power supply has an AC PWR ON indicator light.

2.2 CONTROL PANEL

Used with a teletypewriter and peripheral devices, the control panel contains all controls necessary to operate the 620/f computer system.

2.2.1 Power Switch

The key-operated power switch controls the ac input to the 620/f power supply.

In the PWR OFF position, ac input to the power supply primary is disabled.

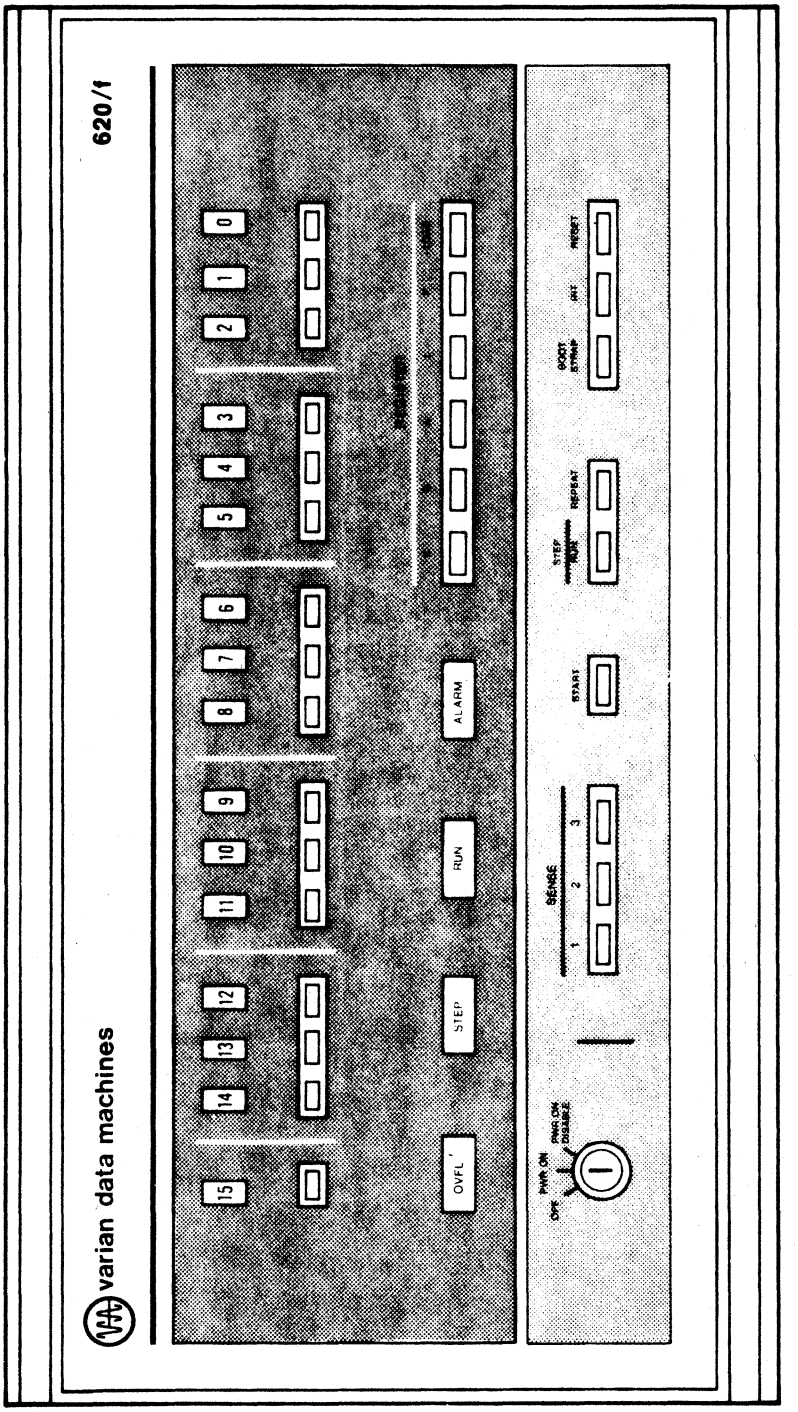
In the PWR ON position, there is ac power to the power supply primary and the system should be fully operational.

In the PWR ON DISABLE position, there is ac power to the power supply primary and the computer is operational. However, all control console switches are disabled except the power switch itself. pressing any other switch while the POWER switch is in PWR ON DISABLE has no effect.

The control panel and power supply indicator lights are functional when the POWER switch is in PWR ON or PWR ON DISABLE.

The key can be removed from the power switch in any of the three positions. To turn off the computer, place the power switch in the PWR ON position, lift the STEP/RUN switch (section 2.2.2), then turn the power switch to PWR OFF.

CHAPTER III
SYSTEM OPERATION



VTII-0703

Figure III-1. 620/f Computer Control Panel

CHAPTER III
SYSTEM OPERATION

2.2.2 STEP/RUN Switch and STEP and RUN Indicators

When the STEP/RUN switch is up, the 620/f is in step mode and the STEP indicator is lit. When the switch is down, the computer is in run mode and the RUN indicator is lit.

If the computer is in step mode:

a. Pressing the STEP/RUN switch to RUN position puts the computer in run mode.

b. Pressing the START switch (section 2.2.4) executes the instruction in the I register, and fetches the next instruction from the address specified by the contents of the P register and places it in the I register.
If the computer is in run mode:

a. Lifting the STEP/RUN switch to STEP position halts the 620/f after completing the execution of the current instruction and fetches the next instruction and sets it in the I register. The RUN indicator goes out and the STEP indicator lights.

b. Pressing the START switch (section 2.2.4) starts the program at the address specified by the P register after executing the instruction in the I register.

Place the STEP/RUN switch in the RUN position for loading the automatic bootstrap (section 2.2.3), and in the STEP position for manual loading of the bootstrap (section 1) and for manual data entry or register display (section 2.2.6).

2.2.3 BOOTSTRAP Switch

BOOTSTRAP is a momentary, spring-loaded switch that is functional in 620/f systems containing the optional automatic bootstrap. In other 620/f systems, this switch is present on the control panel, but it is not connected.

The bootstrap program enables the binary load/dump program to be loaded into memory. Before the automatic bootstrap is loaded into memory, the binary load/dump tape should be inserted into the paper tape reader with the first binary frame at the read station.

To load the automatic bootstrap program:

a. Set the power switch to PWR ON.

b. Set the STEP/RUN switch to RUN.

c. Press and release BOOTSTRAP.

If the system does not contain an automatic bootstrap, load the provided bootstrap program manually (section 1).

2.2.4 START Switch

START is a momentary, spring-loaded switch. Pressing it when the 620/f is in the run mode starts the program. Pressing the START switch when the computer is in the step mode executes the instruction in the I register (except HLT), and fetches the next instruction from the address specified by the contents of the P register and places it in the I register.

2.2.5 REGISTER Switches

Pressing one of the five REGISTER switches selects the designated register (X, B, A, I, or P) for display or entry (section 2.2.6).

Only one register can be selected at a time. Simultaneously pressing two or more REGISTER switches disables the selection logic and front panel register display.

2.2.6 Register Entry Switches and Display Indicators

The 16 indicators across the top of the 620/f control panel display the contents of a selected register. Data are entered into registers on the corresponding register entry switches located under the indicators. The indicators and switches are read from left to right, bits 15 to 0. An illuminated indicator shows that that bit contains a one. For negative data, the sign bit (bit 15) is a one. The indicators and switches are divided into groups of three for ease in reading octal configurations.

2.2.6.1 REGISTER DISPLAY

To display the contents of a register, switch the STEP/RUN switch to STEP and press the REGISTER switch for the desired register (section 2.2.5).

The display indicators light when they correspond to register bits that contain ones. To remove the display, pull up on the REGISTER switch and the indicators go out.

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2.2.6.2 DATA OR INSTRUCTION ENTRY

To enter data or instructions in a register:

a. Display the contents of the register (section 2.2.6.1).

b. Enter ones by pressing down on the register entry switches corresponding to the bits to be set.

c. Enter zeros in the other bits by pulling up on all other register entry switches. The indicator lights do not change when the register entry switches are manipulated. They still display the contents of the register.

d. When the desired configuration is entered on the register entry switches, press LOAD (section 2.2.7). This loads the register with the configuration entered on the switches, and the indicators change to display this new configuration in the register.

To enter data into core memory:

a. Load into the I register a storage instruction (STA, etc.).

b. Select the register specified by the storage instruction in step a.

c. Load the selected register using the data entry switches.

d. Press START to execute the instruction in the I register. This stores the contents of the specified register at the effective memory address.

The TSA instruction can also transfer data entered on the control panel switches to the A register.

2.2.7 LOAD Switch

LOAD is a momentary, spring-loaded switch. When the 620/f is in step mode and a register has been selected (section 2.2.6), pressing this switch loads the register with the bit configuration entered on the register entry switches.

2.2.8 REPEAT Switch

REPEAT is a toggle switch that is operative in both step and run modes. To repeat an instruction contained in the I register, press REPEAT, and then press START. The instruction is executed again and the program counter advances. However, the contents of the I register remain unchanged.

To run a program, REPEAT must be off.

2.2.9 SENSE Switches

The three SENSE switches are toggle switches permitting program modification by the operator. When the program contains instructions dependent on the setting of these switches, jumps and executions occur when the switch condition is met and do not occur when the switch condition is not met.

To set a SENSE switch, press down. To reset it, lift. Operations dependent on the position of this switch will be executed if the switch is in the position indicated by the instruction.

EXAMPLE

A program can be written so that the operator can obtain a partial total of a column of figures being added by use of the JSS1 (jump if SENSE switch 1 is set) instruction. The program writes individual entries as long as SENSE switch 1 is not set. When the operator wants a partial total, he sets the switch. The program then jumps to an instruction sequence that prints the desired information.

2.2.10 INT (Interrupt) Switch

INT is a momentary, spring-loaded switch used to interrupt the 620/f computer. It is functional only when the 620/f is in the run mode.

In systems that do not contain the optional priorty interrupt module (PIM), pressing INT interrupts to memory address 0.

In systems containing a PIM, pressing INT interrupts to an even-numbered memory address specified by the PIM.

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2.2.11 RESET Switch

RESET is a momentary, spring-loaded switch used for initialization control and for stopping I/O operations. Pressing this switch halts the 620/f and initializes the computer and peripherals. This switch is electrically interlocked with the STEP/RUN switch and is disabled when the latter is in RUN.

Note that this switch is not a display reset.

2.2.12 OVFL (Overflow) Indicator

OVFL lights whenever an overflow condition exists. Refer to Part III of this handbook for descriptions of overflow conditions.

2.2.13 ALARM Indicator

ALARM lights to signal an overheated system. If the POWER switch key is accessible, turn the power switch to PWR OFF and call the Varian customer service engineer.

If the power switch key is not accessible, turn off the power switch located on the back of the power supply, or pull the main plug, and call the Varian customer service engineer.

SECTION 3
MANUAL OPERATIONS

3.1 GENERAL

With the 620/f in step mode, data or instructions can be manually transferred to or from memory or stored programs can be manually executed.

Note that the I register contains the instruction being executed, while the P register points to the address of the following instruction.

3.2 LOADING, DISPLAYING, AND ALTERING MEMORY

To load data or instructions into memory, to display the contents of memory, or to alter the contents of memory, follow the procedures in section 2.2.6.

3.3 LOADING SEQUENTIAL MEMORY ADDRESSES

To load a sequential group of memory addresses:

a. Set STEP/RUN to STEP and press REPEAT.

b. Load the P register with the base address.

c. Load into the I register a storage instruction (STA, etc.) with 100 in the M field (relative addressing), and zero in the A field.

d. Select the register specified by the storage instruction in step c.

e. Load the selected register using the data entry switches.

f. Press START to execute the instruction in the I register.

g. Repeat steps e and f until all instructions are loaded. The next cell to be loaded can be observed by displaying the P register.

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3.4 DISPLAYING SEQUENTIAL MEMORY ADDRESSES

To display the contents of a group of sequential memory addresses:

a. Place STEP/RUN in STEP, and press REPEAT.

b. Load the P register with the base address.

c. Load into the I register a loading instruction (LDA, etc.) with 100 in the M field (relative addressing), and zero in the A field.

d. Select the register specified by the loading instruction in step c.

e. Press START once for each memory location to be displayed.

3.5 MANUAL EXECUTION OF A STORED PROGRAM

To execute a stored program manually:

a. Select step mode.

b. Set the P register to the first address of the program.

c. Clear the I register.

d. Press START.

e. Press START again to execute the instruction and to load the next instruction into the I register.

f. Repeat step e once for each instruction.

3.6 MANUAL REPETITION OF INSTRUCTIONS

To repeat an instruction manually:

a. Press the REPEAT switch down.

b. Press START. This advances the P register but inhibits loading the I register. Thus, pressing START again executes the same instruction.

SECTION 1
SYSTEM ORGANIZATION

The main functional sections of the computer (figure IV-1) are:

a. Central processing unit (CPU)

b. Memory

c. Input/output (I/O)

The circuit cards comprising these three sections are:

a. CPU cards:
   (1) Data loop 0 through 3 (part number 44P0445)
   (2) Data loop 4 through 7 (part number 44P0446)
   (3) Data loop 8 through 11 (part number 44P0447)
   (4) Data loop 12 through 15 (part number 44P0448)
   (5) Control I (part number 44P0449)
   (6) Control II (part number 44P0450)
   (7) Clock, DM253 (part number 44P0440)
   (8) Display, DM254 (part number 44P0409)

b. Memory cards:
   (1) Memory stack (part number 50S0068)
   (2) Inhibit/sense, DM256 (part number 44P0410)
   (3) Driver and switch, DM257 (part number 44P0411)
   (4) Timing control and register, DM261 (part number 44P0417)

c. I/O cards:
   (1) I/O control (part number 44P0442)
   (2) I/O data (part number 44P0443)

A transmission bus technique is employed throughout the computer. The term bus, as used in this manual, is any group of parallel signal paths. It may be any part or combination of the following:

CHAPTER IV
THEORY OF OPERATION

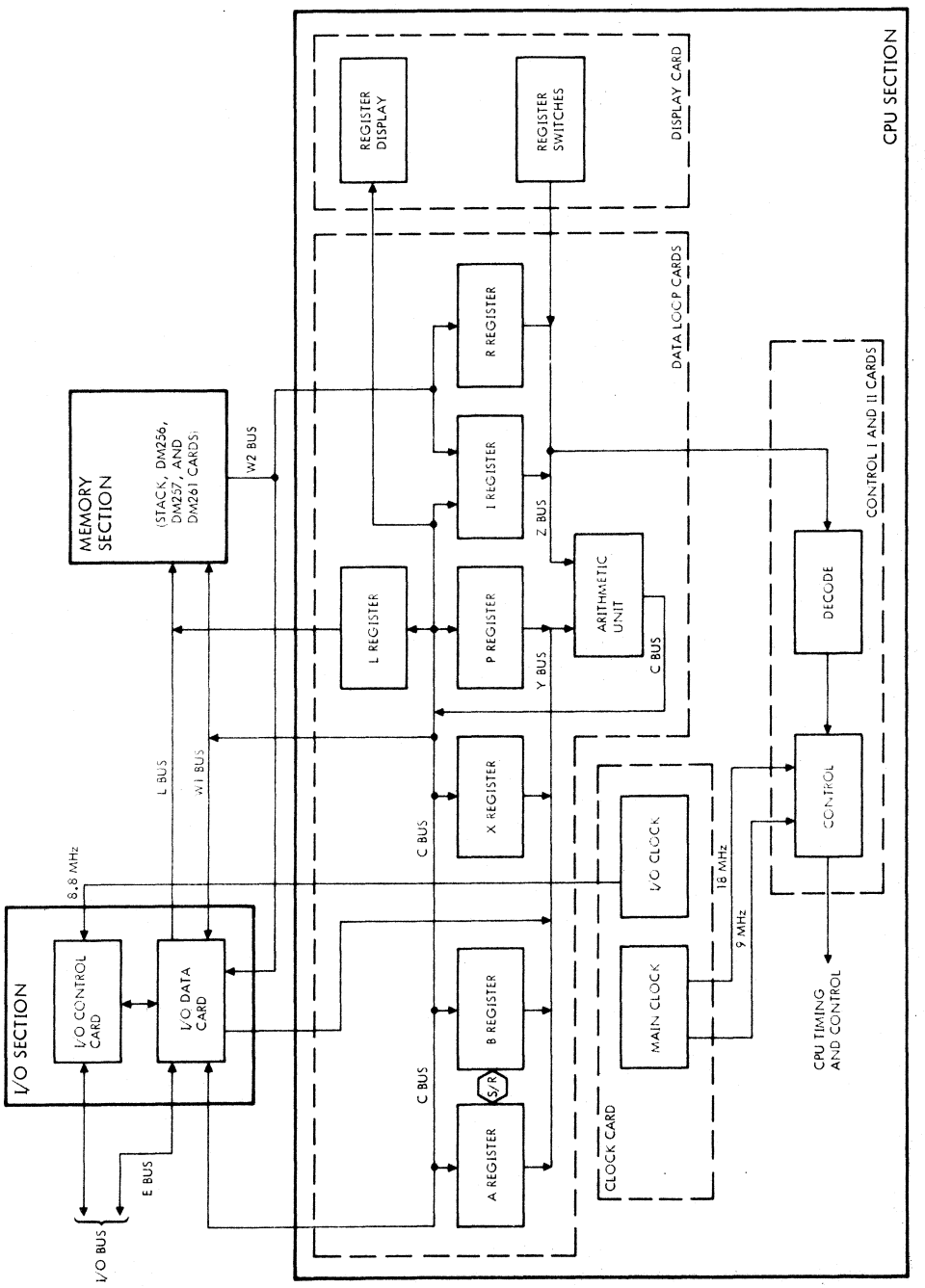

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Figure IV-1. 620/f Functional Block Diagram

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THEORY OF OPERATION

a. Circuit paths on a printed circuit board or group of boards which carry the same parallel bits of data words or related control signals.

b. An entire wire harness assembly or a group of wires in such an assembly which carries parallel bits of data words or related control signals.

c. An entire cable or a group of wires in a cable which carries parallel bits of data words or related control signals. A group of jumper wires or patch cords which carry parallel bits of data words or related control signals.

The following subsections briefly describe the CPU, memory, and I/O sections of the computer. Detailed circuit descriptions are sections 2, 3, and 4.

1.1 CPU SECTION

The CPU section consists of clock circuits, operations and auxiliary registers, arithmetic unit, control and decoding circuits, and register display and switch circuits.

The bit slice technique is used in structuring the arithmetic unit and CPU registers. Each of the four data loop cards contains four bits of all registers (and arithmetic unit) with their respective input and output gates.

1.1.1 Clock Circuits

Two crystal-controlled clock circuits on the DM253 card provide basic timing signals. The main clock circuit generates an 18-MHz master clock to the CPU control circuits for memory interface. The main clock circuit also divides the 18-MHz clock by two and applies the resulting 9-MHz clock to the control circuits for state control.

The I/O clock circuit generates an 8.8-MHz master clock for the I/O section.

1.1.2 Operations Registers

The A, B, X, and P registers comprise the 620/f operations registers. The A, B, and X registers can be directly accessed. The P register is indirectly accessed through the use of jump instructions that modify the program sequence. The outputs of the operations registers (figure IV-1) are connected to the Y bus and routed to the Y inputs of the arithmetic unit. The inputs to the operations registers come from the C bus, which contains output data from the arithmetic unit.

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1.1.2.1 A REGISTER

This 16-bit register is the upper half of the accumulator. It is used for:

a. Accumulating the result of logical operations

b. Accumulating the result of addition or subtraction

c. Accumulating the more significant half of the product in multiplication (optional)

d. Accumulating the remainder in division (optional)

e. Program-controlled I/O transfers

A shift/rotate (S/R) circuit provides a special data path to implement A and B register shift and rotate operations.

1.1.2.2 B REGISTER

This 16-bit register is the lower half of the accumulator. It is used for:

a. Accumulating the less significant half of the product in multiplication (optional)

b. Accumulating the quotient in division (optional)

c. Program-controlled I/O transfers

d. Indexing (as a second index register)

1.1.2.3 X REGISTER

This 16-bit register permits the indexing of operand addresses without adding time to the execution of indexed instructions.

1.1.2.4 P REGISTER

This 15-bit register contains the address of the current instruction. It is incremented before each new instruction is fetched.

1.1.3 Auxiliary Registers

The I, R, L, and D registers comprise the auxiliary registers. The D register is in the I/O section (section 1.2). The outputs of the I and L registers (figure IV-1) are connected to the Z bus and routed to the Z inputs of the arithmetic unit. The inputs to the I and L registers come from the W2 bus, which contains memory output data.

1.1.3.1 I REGISTER

This 16-bit instruction register receives each instruction from memory and holds it during execution. In the case of two-word instructions, the I register holds the first word, i.e., the instruction portion.

1.1.3.2 R REGISTER

This 16-bit buffer register buffers the arithmetic unit from memory to permit interlaced I/O operations to steal memory cycles. The R register holds the second word of a two-word instruction, the multiplicand in multiplication (optional), and the divisor in division (optional).

1.1.3.3 L REGISTER

This 16-bit register contains the address of the currently accessed memory address.

1.1.4 Arithmetic Unit

This section contains the adder and gating for all operations except shifting. Under the control of the CPU control circuits, the arithmetic unit processes data from the Y and Z buses and sets the result on the C bus.

1.1.5 Control Circuits

This section generates timing and control signals using the information received from the I register. The control circuits are contained on the control I and II cards.

1.1.6 Decoding Circuits

This section decodes the bits of the word in the I register used to determine control signal levels generated by the control circuits. The decoding circuits are contained on the control I and II cards.

CHAPTER IV
THEORY OF OPERATION

1.1.7 Register Display and Switch Circuits

This section displays the contents of and loads registers or memory on the 620/f control panel (chapter III). The register display and switch circuits are contained on the DM254 display card.

1.2 MEMORY SECTION

The expandable, random-access, three-wire/three-dimensional magnetic core memory is used for program and data storage. It operates asynchronously with the CPU and I/O sections.

Instructions from memory are transferred to the control section for execution. Under program control, words can be transferred from memory to the arithmetic unit, operations register, or I/O bus and, conversely, to memory from the operations registers or the I/O bus.

Words written into memory are transferred on the W1 bus; words read out, on the W2 bus. Memory addresses are transferred to memory on the unidirectional L bus.

A modular master/slave configuration permits economical memory expansion. The slave module (or modules) uses the timing and control circuits of the master, and requires no DM261 card.

1.3 I/O SECTION

Peripheral devices communicate with the computer on the I/O bus. The 16-bit, party-line, bidirectional I/O bus transfers programmed data between peripheral devices and the computer. The I/O bus also permits plug-in expansion of existing 620/f peripherals. Part of the I/O bus is an E bus for bidirectional data transfer.

Information exchanges with peripheral devices are synchronized by peripheral controllers, which can control one or more similar devices. Each controller and the device (or devices) it controls comprise a peripheral device option.

The I/O section is on two circuit cards. The I/O data card contains the 16-bit D register, which stores E bus I/O information. The I/O control card contains timing and control circuits for program-controlled I/O, direct memory access (DMA), and interrupt operations.

1.3.1 Program-Controlled I/O

Under program control, the I/O system communicates directly with peripheral device options. The computer can initiate operation of a peripheral device by transmitting an external control code and device address to the selected controller via the I/O bus. The computer can determine when a device is ready to send or receive information by interrogating its associated sense line. A device can be requested to place a word of data on the I/O bus during a computer input transfer or to accept a word of data placed on the bus by the computer during an output transfer.

1.3.2 Direct Memory Access

DMA trapping consists of automatic data transfers between memory and peripheral controllers. A peripheral device can request the transfer of a data word while temporarily halting the processing of the stored program.

To implement DMA, the buffer interlace controller (BIC) must be installed to generate the required trap-out and trap-in requests. To prevent several peripheral devices from requesting data transfers simultaneously, the priority interrupt module (PIM) determines the order (priority) of the requests.

The period that the stored program halts for DMA operation is:

Trap Out:	1.250 microseconds (minimum)
	1.675 microseconds (average)
	2.100 microseconds (maximum)
Trap In:	1.025 microseconds (minimum)
	1.465 microseconds (average)
	1.900 microseconds (maximum)

This cycle-stealing does not disturb the contents of the operations and auxiliary registers. The program can, therefore, proceed normally at the conclusion of the transfer.

The data transfer rate of the DMA trap function is:

220,000 words per second (minimum)
244,000 words per second (average)
275,000 words per second (maximum)

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To determine the minimum transfer rate, add the trapping sequence time (2.73 microseconds) and the priority settling time (0.91 microsecond) to the full synchronization time (0.91 microsecond) required by the external device. To determine the average transfer rate, add the trapping sequence time (2.73 microseconds) and the priority settling time (0.91 microsecond) to one-half the synchronization time (0.45 microsecond) required by the external device. The maximum transfer rate assumes that no synchronization time is required by the external device; it is determined by adding the trapping sequence time (2.73 microseconds) to the priority settling time (0.91 microsecond).

1.3.3 I/O Interrupts

The interrupt circuits allow internal computer options, on a priority basis, to request the computer to execute an instruction independent of the stored program. The options are:

a. Memory protection (MP)

b. Power failure/restart (PF/R)

c. Real-time clock (RTC)

d. PIM

e. BIC

During the interrupt, the computer is directed to the memory address specified by the interrupting device and executes the instruction at that address.

The execution of all but I/O instructions can be requested. Normally, it is a jump-and-mark instruction that results in the processing of an I/O subroutine. In this event, the interrupt system is automatically inhibited until program-controlled termination of the inhibit.

SECTION 2
CPU

To be supplied.

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THEORY OF OPERATION

SECTION 3
MEMORY

The 620/f memory is an expandable, random-access, three-wire/three-dimensional, magnetic core memory for storing instructions and data. The memory system can be expanded to 32,768 (32K) words in 8,192- and 4,096-word increments (modules). Memory words are 16 bits long. Memory is expanded by connecting 8,192-word (8K) or 4,096-word (4K) slave modules to the 8K or 4K master module.

3.1 MEMORY CYCLE

During a memory cycle, the memory performs a reading sequence followed by a writing sequence. When a word is transferred from the CPU to memory, the memory cycle is a clear/write operation. When a word is transferred from memory to the CPU, the memory cycle is a read/restore operation.

3.1.1 Clear/Write

A clear/write operation loads the memory. The clear portion of the operation resets the addressed cores to zero; the write sequence then loads data in the addressed cores.

During the clear sequence, the X and Y drive wires of an addressed word are activated (read current) to magnetize the cores to zero. Addressed cores already at zero are not changed.

During writing, the X and Y drive wires of an address word are activated (write current) to magnetize the cores to one. If a core must be zero, the associated inhibit wire generates an inhibit current that cancels Y drive current, preventing the core from switching. The word, with correct bit configuration, is thus loaded into memory.

3.1.2 Read/Restore

A read/restore operation reads information from memory. The read portion of the operation unloads the addressed word from memory; the restore immediately reloads (writes) the word in the same core location.

During reading, the X and Y drive wires of an addressed word are activated (read current) to magnetize the cores to zero. Addressed cores already at zero are not changed. If an addressed core is one, a voltage is induced in the associated sense wire when the core

switches to zero. The sense voltage is then interrogated and amplified to provide a memory read bit.

During the restore sequence, the X and Y drive wires of an addressed word are activated (write current) to magnetize the cores to one. If a core must be zero, the associated inhibit wire generates an inhibiting current that cancels Y drive current, preventing the core from switching. The word, with correct bit configuration, is thus loaded into the same core location.

3.2 MEMORY CIRCUIT CARDS

An 8K master memory module consists of four circuit cards:

a. *Memory Stack Card* -- contains a diode-decoding matrix, a magnetic core array, and two sensistors.

b. *Driver and Switch Card (DM257)* -- contains 32 pairs of drivers and switches.

c. *Inhibit/Sense Card (DM256)* -- contains 32 inhibit drivers and 32 sense amplifiers.

d. *Timing Control and Register Card (DM261)* -- contains timing control circuits, address register, address decoder, data register, and current sources.

Figure IV-2 illustrates the functional circuit blocks of the memory in relation to the four circuit cards.

3.2.1 Memory Stack Card

The upper and lower surfaces of the memory stack card contain a printed-circuit (PC) diode matrix and a planar magnetic core array. For an 8K module, the core array consists of thirty-two 4K mats, each mat comprising one bit of the 16-bit word. A 4K mat contains 63 rows (X lines) and 64 columns (Y lines) of magnetic cores (figure IV-3). To reduce the number of drivers and switches (on the DM257 card) required to operate an 8K stack, sixteen 4K mats are wired for coincident-current storage, and 16, for anticoincident-current storage (anticoincident core-driving method). For addressing, the 16 mats wired for coincident-current storage comprise the first half of the 8K stack, designated 4K-A. The 16 anticoincident-current storage mats comprise the second half of the 8K stack, designated 4K-B.

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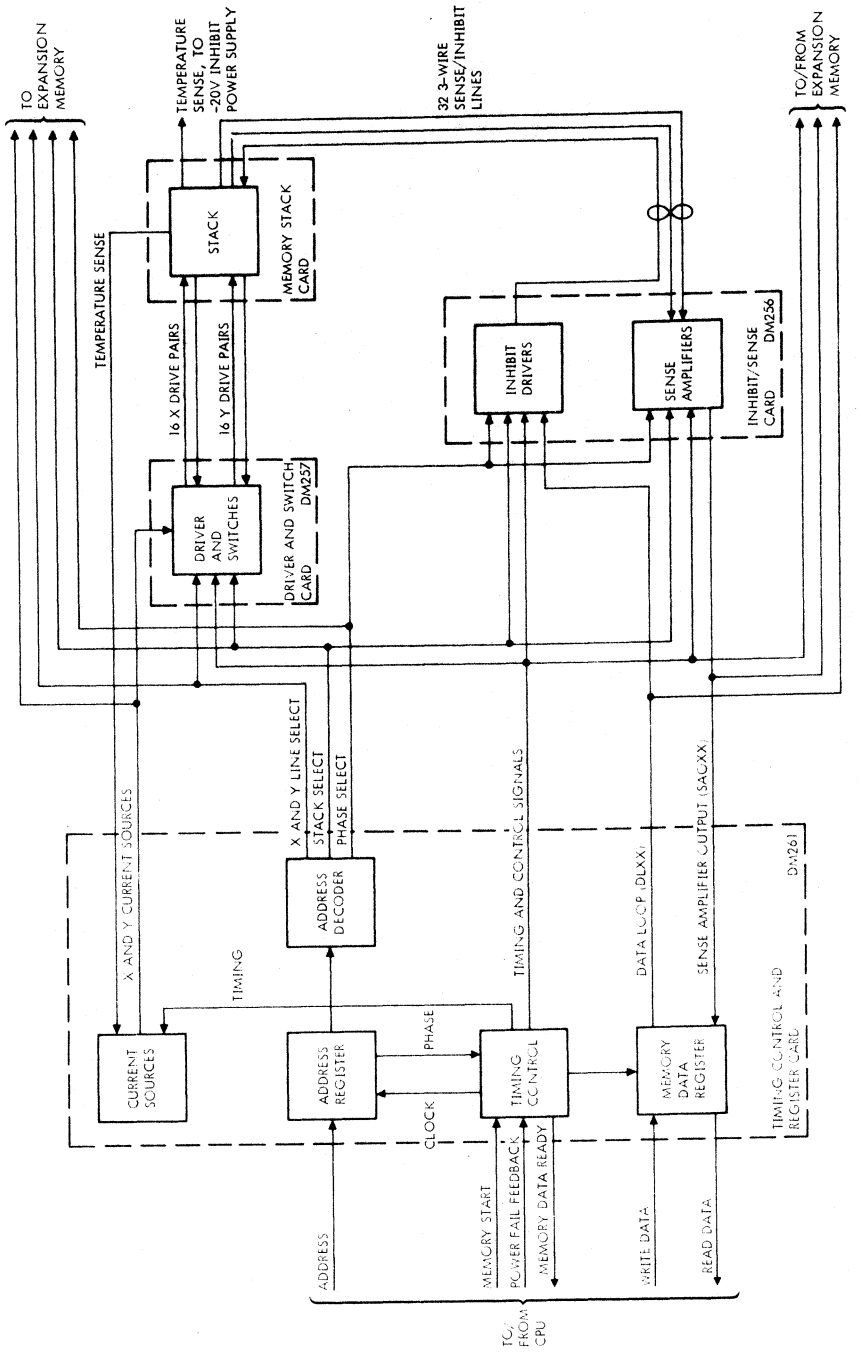

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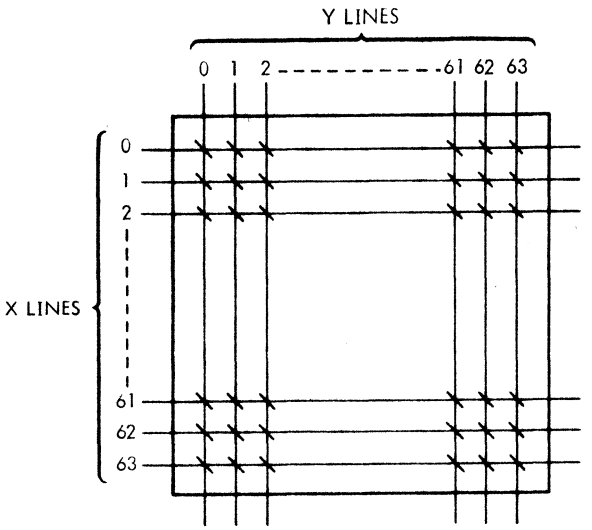
Figure IV-2. 620/f Memory Block Diagram



NOTE: A SENSE/INHIBIT LINE, NOT SHOWN ABOVE, ALSO PASSES THROUGH ALL CORES OF A 4K MAT PARALLEL TO THE Y LINES.

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Figure IV-3. 4K Core Mat

3.2.1.1 CONTROL LINES

Three control lines (X, Y, and sense/inhibit) pass through each magnetic core.

a. **X Lines.** Each X line passes through the same row of core in all thirty-two 4K mats (16 for a 4K memory module). The current in the X line can be either zero or one-half the current required to change the magnetized state of a core. The direction of the current depends on whether memory is being written into or read from. It also depends on whether the memory operation is a positive- or negative-phase cycle. A positive phase indicates that the addressed cores are in the 4K-A section of the stack; a negative phase indicates that the cores are in 4K-B.

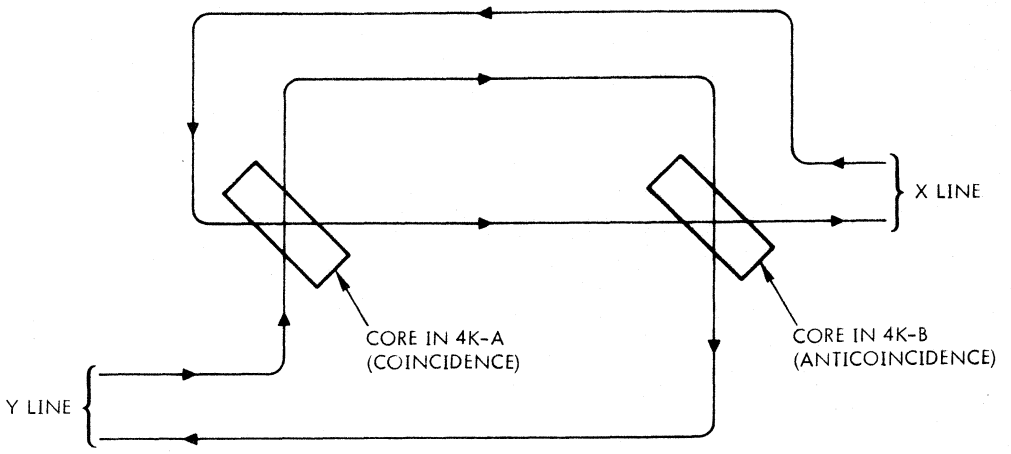
b. **Y lines.** Each Y line passes through the same column of cores in all thirty-two 4K mats (16 for a 4K memory module). The current in the Y line can be either zero or one-half the current required to change the magnetized state of a core. The direction of the current depends only on whether a read or write operation is occurring in memory. The memory cycle phase (positive or negative) does not affect currect direction. The Y line is routed so that the current enters 4K-A cores in one direction and the 4K-B cores in the other (figure IV-4). In figure IV-4, the X and Y currents enter the same side of the 4K-A cores (additive); the

currents enter opposite sides of 4K-B, canceling each other. This indicates a positive-phase memory cycle and 4K-A changes state (coincidence) and 4K-B does not (anticoincidence).

c. **Sense/Inhibit Lines.** A sense/inhibit line passes through all cores of a 4K mat parallel to the Y lines and perpendicular to the X lines. Each mat has an individual sense/inhibit line.

The sense/inhibit line senses the state of the cores. If a core is one, an induced voltage is applied to the associated sense amplifier; otherwise, no voltage is induced. During reading, the sense amplifier outputs are strobed into the memory data register.

The sense/inhibit line also routes an inhibiting current through an addressed core into which a zero is to be written. During writing, half-current signals are applied to the selected X and Y lines to set the addressed cores to one. For zero cores, the inhibiting current cancels the Y line current, preventing the addressed core from switching to one. Thus, a zero bit from the memory data register generates inhibiting current, and a one does not.



NOTE: THE CURRENT DIRECTIONS IN THIS EXAMPLE INDICATE A POSITIVE PHASE MEMORY CYCLE.

VTII-0974

Figure IV-4. Routing of X and Y Lines

3.2.1.2 SENSISTORS

The memory stack card also contains two temperature-sensing silicon resistors (sensistors). The sensistors monitor stack temperature and produce temperature-sensing signals that control the amount of current in the X and Y and the inhibit lines. Stack temperature can, thus, follow a significant change in amibient temperature and maintain reliable memory operation.

One sensistor provides an input reference voltage for the X and Y current source circuits on the DM261 card. The other sensistor provides a signal to control the -20 volts from the power supply, which, in turn, regulates the current flow in the memory inhibit lines.

3.2.2 Driver and Switch Card

The driver and switch card (DM257) contains 32 pairs of drivers and switches, four predriver circuits, and read/write and phase-selection gates.

Driver and switch inputs are connected to 32 address decoding lines from the DM261 card. Their outputs are connected in an 8 x 8 X driver/switch matrix and an 8 x 8 Y driver/switch matrix. The decoded address from the DM261 card activates one of the 64 X and one of the 64 Y driver/switch combinations to route the X and Y drive currents through the appropriate X and Y lines.

The read/write and phase-selection gates receive read or write signals from the DM261 card that determine the direction of current in the X and Y lines.

3.2.3 Inhibit/Sense Card

The inhibit/sense card (DM256) contains 32 inhibit drivers and 32 sense amplifiers, sense amplifier strobe and inhibit timing gates, and a threshold voltage regulator. Each inhibit driver and sense amplifier is connected to the sense/inhibit line associated with an individual 4K core mat. For 4K stacks, the DM256 card contains only 16 inhibit drivers and 16 sense amplifiers.

The inhibit driver inputs are connected to the 16 output data lines of the memory data register on the DM261 card. During writing and under control of the inhibit timing, the inhibit drivers produce inhibiting current for zero data bits and none for ones.

The differential input of a sense amplifier is connected to a corresponding sense/inhibit line. The output is connected to a corresponding input data line of the memory data

register. The states of addressed cores are sensed by the sense amplifiers, and, during reading, the amplifiers are strobed to set data register flip-flops for all sensed one bits.

The threshold voltage regulator provides a voltage reference for the sense amplifiers.

3.2.4 Timing Control and Register Card

The timing control and register card (DM261) contains timing control circuits, address register and decoder, memory data register, and current sources.

The timing control circuits, which consist of two tapped delay lines in series and transistor-transistor logic gates, provide timing and control signals for memory operation. A memory start pulse sends a signal to one of the delay lines. At precise intervals along the delay lines, signals are tapped off. Selected tapped signals combine with control signals to generate internal memory timing and an interface signal to the CPU. The internal memory timing signals are:

a. Address register clock

b. Data register load and reset

c. X and Y read/write timing

d. Inhibit driver timing

e. Sense amplifier strobes

f. X and Y current source timing

The CPU interface signal is: memory data ready.

The 15-bit address register accepts address information from the CPU at the beginning of each memory cycle. The register outputs are decoded by the address decoder. Address bits 0-5 select one of 64 Y lines; bits 6-11, one of 64 X lines; bit 12, a positive or negative phase; and bits 13-14, the stack. The X and Y line selection information goes to the driver and switch card; phase selection, to the inhibit/sense card; and stack selection, to both the inhibit/sense and driver and switch cards. The decoded address information goes to all memory modules in the computer system; however, only the module enabled by the stack selection signal is activated.

The 16-bit memory data register accepts write data from the CPU and read data from the memory sense amplifiers. During a clear/write operation, a data register loading signal loads the CPU data in the memory data register where it is routed through buffer gates to the memory inhibit drivers. During a read/restore operation, a data enable signal transfers sense amplifier data stored in the memory address register through line drivers to the CPU.

The current source circuits consist of two current regulators that provide drive currents for the X and Y lines. A temperature sensing signal from a sensistor on the memory stack card comprises the input reference voltage for both regulators. The regulators are enabled during reading and writing sequences with X and Y timing pulses from the timing control circuits.

3.3 MEMORY CIRCUIT OPERATION

To be supplied.

3.4 DATA LOOP OPERATION

To be supplied.

3.5 MNEMONICS

Mnemonics that appear on the 620/f memory logic diagrams are alphabetically listed in table IV-1, with a description and source information (i.e., card number-logic diagram page number). The memory circuit cards and corresponding logic diagrams are:

Card	Description	Drawing No.
DM256	Inhibit Sense	91C0186 (8K)
DM257	Driver Switch	91C0252
DM261	Timing Control and Register	91C0220

Table IV-1. 620/f Memory Mnemonics

Mnemonic	Source	Description
ABS00-14	DM261-9,10,11	Address bus bits 0-14. These signals come from the CPU; bits 0-5 select one of 64 Y lines, bits 6-11 select one of 64 X lines, bit 12 selects positive or negative phase, and bits 13-14 select the stack.

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A0	DM261-13,15	Input pulse to delay line DL1
ARB12	DM261-11	Address register bit 12; output of memory address register. Provides phase selection information for the sense/inhibit card.
ARCLK	DM261-15	Address register clock signal for memory address register.
A1-A25	DM261-13	Output terminals of delay line DL1.
B0	DM261-13	Input terminal of delay line DL2.
B1-B25	DM261-13	Output terminals of delay line DL2.
CSGRD	DM261-12	Current source ground.
CW	DM261-14	Clear/write. This signal is generated in the memory timing and control circuit; it is a 120-nanosecond sample of RW-.
DATA EN1	DM261-13	Data enable 1; transfers data bits 0-6 from the memory data register to the CPU.
DATA EN2	DM261-13	Data enable 2; transfers data bits 7-15 from the memory data register to the CPU.
DL0-15	DM261-6,7,8	Data loop bits 0-15; transferred from the memory data register to the memory inhibit drivers during a write memory sequence.
DRL1	DM261-14	Data register load 1. During a clear/write operation, this signal loads data bits 0-8 from the CPU into the memory data register.

DRL2	DM261-14	Data register load 2. During a clear/write operation, this signal loads data bits 9-15 from the CPU into the memory data register.
DRR	DM261-14	Data register reset; clears the memory data register approximately 120 nanoseconds after the start of each memory cycle.
D0A-D15A	DM256-6,7,8,9	Output data bits 0-15 of inhibit drivers A. During a write memory sequence, these signals produce inhibit current in the 4K-A cores if the corresponding data bit is zero.
D0B-D16B	DM256-6,7,8,9	Output data bits 0-15 of inhibit drivers B. During a write memory sequence, these signals produce inhibit current in the 4K-B cores if the corresponding data bit is zero.
GINH	DM256-3	Inhibit ground for the inhibit circuits on the inhibit/sense card. The inhibit ground is isolated from the signal ground used throughout the remainder of the memory.
GSIG	DM256-3	Signal ground; used throughout the memory except for the inhibit circuits on the inhibit/sense card.

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INHT	DM261-13	Inhibit timing. At the beginning of a write memory sequence, this signal goes to the inhibit/sense card to produce INHTA or INHTB.
INHTA	DM256-4	Inhibit timing A; input timing signal for inhibit drivers A.
INHTB	DM256-4	Inhibit timing B; input timing signal for inhibit drivers B.
MB00-15	DM261-6,7,8	Memory bus bits 0-15. These signals represent data from the CPU that are to be written into memory.
MBZY	DM261-15	Memory busy; indicates when a memory cycle is in progress.
MDR	DM261-15	Memory data ready; generated during a read/restore or a clear/write operation to signal the CPU that data are on the W bus.
MD00-15	DM261-6,7,8	Memory data bits 0-15. These signals are transferred from the memory data register to the CPU during a read memory sequence.

MST	DM261-15	Memory start; generated in the CPU (control II card) to initiate a memory cycle (clear/write or read/restore).
PFF	DM261-15	Power failure feedback. During a power failure, PFF from the CPU disables the memory by resetting the memory timing and control circuits.
PHASE A	DM256-4	Originates from signal ARB12- on the DM261 card; determines whether sense/inhibit lines A or B are to be activated.
PXRT	DM261-14	Positive phase X read time; activates driver/switch circuits at the appropriate times to cause read current to flow in the selected X line. PXRT occurs during a read memory sequence when a positive phase (addressing of 4K-A cores) is selected and during a write memory sequence when a negative phase (addressing of 4K-B cores) is selected.
PXWT	DM261-14	Positive phase X write time; activates driver/switch circuits at the appropriate times to cause write current to flow in the selected X line. PXWT occurs during a write memory sequence when a positive

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		phase (addressing of 4K-A cores) is selected and during a read memory sequence when a negative phase (addressing of 4K-B cores) is selected.
R	DM261-15	Read half cycle; generated by the memory timing and control circuit during a read memory sequence.
RW	DM261-14	Read/write; generated by the CPU; a low level causes a read memory sequence, and a high level, a write memory sequence.
SASA	DM256-4	Sense amplifier strobe A; enables sense amplifier circuits that produce SAO10-15.
SASA (9-15)	DM256-4	Sense amplifier strobe A1; enables sense amplifier circuits that produce SAO0-9.
SASB	DM256-4	Sense amplifier strobe B; enables sense amplifier circuits that produce SAO10-15.
SASB1	DM256-4	Sense amplifier strobe B1; enables sense amplifier circuits that produce SAO0-09.
SAS1	DM261-14	Sense amplifier strobe 1; generated by the memory timing and control circuit during a memory read sequence. It goes to the inhibit/sense card to produce SASA1 or SASB1.

SAS2	DM261-14	Sense amplifier strobe 2; generated by the memory timing and control circuit during a memory read sequence. It goes to the inhibit/sense card to produce SASA or SASB.
SAO0-15	DM256-6,7,8,8	Sense amplifier output bits 0-15. The sense amplifiers monitor the states of the addressed cores and route the information to the memory data registers during a read sequence.
SH0A-SH15A	DM256-6,7,8,9	Sense high A bits 0-15; the high lines to the differential inputs of the 16 sense amplifiers associated with the 4K-A cores.
SH0B-SH15B	DM256-6,7,8,9	Sense high B bits 0-15; the high lines to the differential inputs of the 16 sense amplifiers associated with the 4K-B cores.
SL0A-SL15A	DM256-6,7,8,9	Sense low A bits 0-15; the low lines to the differential inputs of the 16 sense amplifiers associated with the 4K-A cores.

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SL0B-SL15B	DM256-6,7,8,9	Sense low B bits 0-15; the low lines to the differential inputs of the 16 sense amplifiers associated with the 4K-B cores.
SS0-3	DM256-11	Stack select 0-3. SS0 selects the first 8K (or 4K) memory module; SS1, the second; SS2, the third; and SS3, the fourth.
TSCH	Memory stack card (see DM261-12)	Temperature sense current source high; the high side of a temperature sense signal generated by a sensistor on the memory stack card. TSCH goes to the input of the X and Y current sources on the DM261 card.
TSCL	Memory stack card (see DM261-12)	Temperature sense current ource low; the low side of a temperature sense signal generated by a sensistor on the memory stack card. TSCL goes to the input of the X and Y current sources on the DM261 card.
TSZH	Memory stack card (see DM261-16)	Temperature sense inhibit high; the high side of a temperature sense signal generated by a sensistor on the memory stack card. TSZH controls the -20 volts from the computer power

		supply, which, in turn, regulates the current flow in the memory inhibit lines.
TSZL	Memory stack card	Temperature sense inhibit low; the low side of a temperature sense signal generated by a sensitor on the memory stack card. TSZL controls the -20 volts from the computer power supply, which, in turn, regulates the current flow in the memory inhibit lines.
+VREF	DM256-4	Voltage reference; a threshold voltage reference for the sense amplifiers.
W	DM261-15	Write half cycle; generated by the memory timing and control circuit during a write memory sequence.
XA0-7	DM261-10	X select A signals 0-7; result of the decoding of address bits 6, 7, and 8.
XA0D-XA7D	DM257-7	XA driver output lines 0-7. During a positive phase read or a negative phase write sequence, one of these lines routes the X current source through the addressed cores.

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XA0S-XA7S	DM257-7	XA switch output lines 0-7. During a positive phase write or a negative phase read sequence, one of these lines provides a return (sink) for routing the X current source through the addressed cores.
XB0-7	DM261-10	X select B signals 0-7; result of the decoding of address bits 9, 10, and 11.
XB0D-XB7D	DM257-7	XB driver output lines 0-7. During a positive phase write or a negative phase read sequence, one of these lines routes the X current source through the addressed cores.
XB0S-XB7S	DM257-7	XB switch output lines 0-7. During a positive phase read or a negative phase write sequence, one of these lines provides a return (sink) for routing the X current source through the addressed cores.
XCS	DM261-12	X current source; drives the memory X lines and is nominally 420 mA.
XCSR	DM261-12	X current source return.

XCST	DM261-13	X current source time; generated by the memory timing control circuits to turn on the X current source circuits at the appropriate times during read and write sequences.
YA0-YA7	DM261-9	Y select A signals 0-7; result of the decoding of address bits 0, 1, and 2.
YA0D-YA7D	DM257-6	YA driver output lines 0-7. During a positive or negative phase read sequence, one of these lines routes the Y current source through the addressed core.
YA0S-YA7S	DM257-6	YA switch output lines 0-7. During a positive or negative phase write sequence, one of these lines provides a return (sink) for routing the Y current source through the addressed cores.
YB0-YB7	DM261-9	Y select B signals 0-7; result of the decoding of address bits 3, 4, and 5.
YB0D-YB7D	DM257-6	YB driver output lines 0-7. During a positive or negative phase write sequence, one of these lines routes the Y current source through the addressed cores.

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YB0S-YB7S	DM257-6	YB switch output lines 0-7. During a positive or negative phase read sequence, one of these lines provides a return (sink) for routing the Y current source through the addressed cores.
YCS	DM261-12	Y current source; drives the memory Y lines and is nominally 420 mA.
YCSR	DM261-12	Y current source return.
YCST	DM261-13	Y current source time; generated by the memory timing control circuits to turn on the Y current source circuit at the appropriate times during read and write sequences.
YRT	DM261-14	Y read time; activates driver/switch circuits at the appropriate times to cause read current to flow in the selected Y line.
YWT	DM261-14	Y write time; activates driver/switch circuits at the appropriate times to cause write current to flow in the selected Y line.

SECTION 4
INPUT/OUTPUT

To be supplied.

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THEORY OF OPERATION

SECTION 5
CPU AND I/O MNEMONICS

To be supplied.

CHAPTER V
MAINTENANCE

SECTION 1
INTRODUCTION

Integrated-circuit design reduces the occurrence of malfunctions in 620/f systems. Overheating is signaled by the ALARM indicator on the 620/f control panel. The power failure/restart (PF/R) option provides an orderly shutdown in case of power failure or turn-off and restarts the program when power is restored. To prevent accidental setting of control panel controls during computer operation, all switches can be disabled with the power switch.

To ensure effective maintenance of the 620/f:

a. Study the documentation furnished with the equipment.

b. Assess system performance with adequate test equipment.

c. Implement the available maintenance aids.

d. Apply orderly and logical troubleshooting techniques.

1.1 TEST EQUIPMENT

The following test equipment is recommended for 620/f maintenance:

Equipment	Description
Oscilloscope	Tektronix type 547 or equivalent with dual-trace plug-in unit
Multimeter	Simpson 260 or equivalent
Card Extenders	DM265 for cards in CPU tray; DM115 for peripheral controllers
Extension Cable	Required for CPU and memory trays
Card Puller	Titchener 1731

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Equipment	Description
Wire-Wrap Gun	Gardener-Denver 14R2 or equivalent
Soldering Iron	39-watt pencil type

1.2 CIRCUIT CARD ACCESSIBILITY

All computer circuits are on three types of plug-in circuit cards:

a. Cards in the CPU tray, 3 by 15 inches (7.7 x 38.1 cm)

b. Cards in the memory tray, 15 by 18 inches (38.1 x 45.5 cm)

c. Peripheral controller cards, 7.75 by 12 inches (19.7 x 30.3 cm)

1.2.1 Cards in CPU Tray

When the computer is turned off and the control panel opened on its hinges, the CPU tray can be disconnected from the motherboard. A flexible extender cable is connected between the motherboard and the CPU tray, allowing the tray to extend forward through the front of the mainframe. The CPU tray is then firmly attached to a bracket mounted on the front of the mainframe. A card can be made accessible for troubleshooting by installing it on an extender card. With the CPU tray and the circuit card in this configuration, the computer can be turned on to begin troubleshooting.

1.2.2 Cards in Memory Tray

The memory trays can be extended through the front of the mainframe or expansion frames in the same manner as the CPU tray. The memory cards are mounted with hinges that allow them to be opened. A card is made accessible for troubleshooting by opening it to a convenient position where it can be held firmly with a support brace.

1.2.3 Peripheral Controller Cards

Any peripheral controller card is accessible for troubleshooting when it is installed on a DM115 extender card. This allows the peripheral controller card to extend outside the rear of the computer frame. In this configuration, the controller interfaces with the CPU through the extender card and with the peripheral device through the two-44-pin card-edge connectors.

1.3 MAINTENANCE AIDS

The 620/f maintenance aids include test programs, logic diagrams and assembly drawings, connector pin assignment lists, and the control panel. Tables V-1, V-2, and V-3 provide a reference to lists, drawings, and assemblies.

Table V-1. Computer Reference Drawings

Computer/Function	Assembly	Wire List	Logics
CPU	01P0902	95W0696	
Control I	44P0449	95W0649	91C0217
Control II	44P0450	95W0648	91C0218
Data Loop 0-3	44P0445	95W0608	91C0213
Data Loop 4-7	44P0446	95W0609	91C0214
Data Loop 8-11	44P0447	95W0610	91C0215
Data Loop 12-15	44P0448	95W0611	91C0216
I/O Control	44P0442	95W0646	91C0210
I/O Data	44P0443	95W0636	91C0211
TTY Control	44P0451	95W0606	91C0219
Clock	44P0440		91C0209
Front Panel	01P0905		
Power Supply	01P0921		
Memory	01P0779		

Table V-2. Option Reference Drawings

Component/Function	Assembly	Wire List	Logics
Optional Instruction Set	44P0444	95W0647	91C0217
Memory Protection	44D0480	95W0719	91B0257
Priority Memory Access	44D0481	95W0720	91B0258
Real-Time Clock	44D0482	95W0721	91B0259
Power Failure/Restart	44D0483	95W0722	91C0260
Automatic Bootstrap Loader	44D0484	95W0723	91B0261

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Table V-3. Other Documents

Title	Document No.
620/f Reference Handbook	98 A 9908 001
620/f Test Programs Manual	98 A 9908 960
620 Master Operating System Reference Manual	98 A 9952 090

1.3.1 MAINTAIN II

The MAINTAIN II test program system verifies correct system operation, including internal instructions, memory, internal options, and peripherals and their controllers. Malfunctions can be isolated to a specific area of the system and corrected.

MAINTAIN II is described in detail in the 620 test programs manual (document number 98 A 9908 960). Table V-4 lists the MAINTAIN II test program.

Table V-4. MAINTAIN II Test Programs

Program	Part Number
Test Executive	92A0107-001
Instructions Test	92A0107-002
Memory Test	92A0107-004
Teletype Test	92A0107-005
Power Failure/Restart Test	92A0107-008
Priority Interrupt Module Test	92A0107-009
Priority Memory Access Test	81A0107-001
Memory Protection Test	
Real-Time Clock Test	
Buffered I/O Test	92A0107-010

1.3.2 Integrated-Circuit Terminals

Observing electrical waveforms is essential for locating specific malfunctioning components. Using the DM115 extender card, integrated-circuit terminals on the circuit cards can be accessed and waveforms monitored. Integrated-circuit locations are shown on the circuit card assembly drawings, and terminal locations are shown on the circuit card logic diagrams. These drawings and diagrams are in volume 2 of this manual.

1.3.3 Control Panel

The control panel contains the switches and indicators required for operating the 620/f computer. Refer to the 620/f reference handbook (document number 98 A 9908 001) for detailed descriptions of the switches and indicators and operating procedures. The switches described below are particularly useful for maintenance and troubleshooting:

a. STEP/RUN. When the STEP/RUN switch is up, the 620/f is in step mode and a program sequence can be executed one instruction at a time. In step mode, pressing the START switch executes the instruction in the I register, and fetches the next instruction from the address specified by the contents of the P register and places it in the I register. The computer halts after executing each instruction, and the results can be observed using the register display indicators.

b. REPEAT. The REPEAT toggle switch is operative in both step and run modes. To repeat an instruction contained in the I register, press REPEAT, and then press START. The instruction is executed again and the contents of the I register remain unchanged.

c. Register Entry Switches and Display Indicators. The 16 indicators across the top of the 620/f control panel display the contents of a selected register. Data are entered into registers on the corresponding register entry switches located under the indicators. The indicators and switches are read from left to right (bits 15 to 0). A lighted indicator shows that that bit is a one. The indicators and switches are divided into groups of three for ease in reading octal configurations.

1.4 TROUBLESHOOTING TECHNIQUES

The time required to correct system malfunctions depends on the efficiency of the procedures used. Although various specific techniques can be applied, there is no substitute for an ordered, logical analysis of the problem and isolation of the cause to the level of the faulty component. Such an analysis can be based only on knowledge of the equipment design.

General troubleshooting steps are illustrated in figure V-1.

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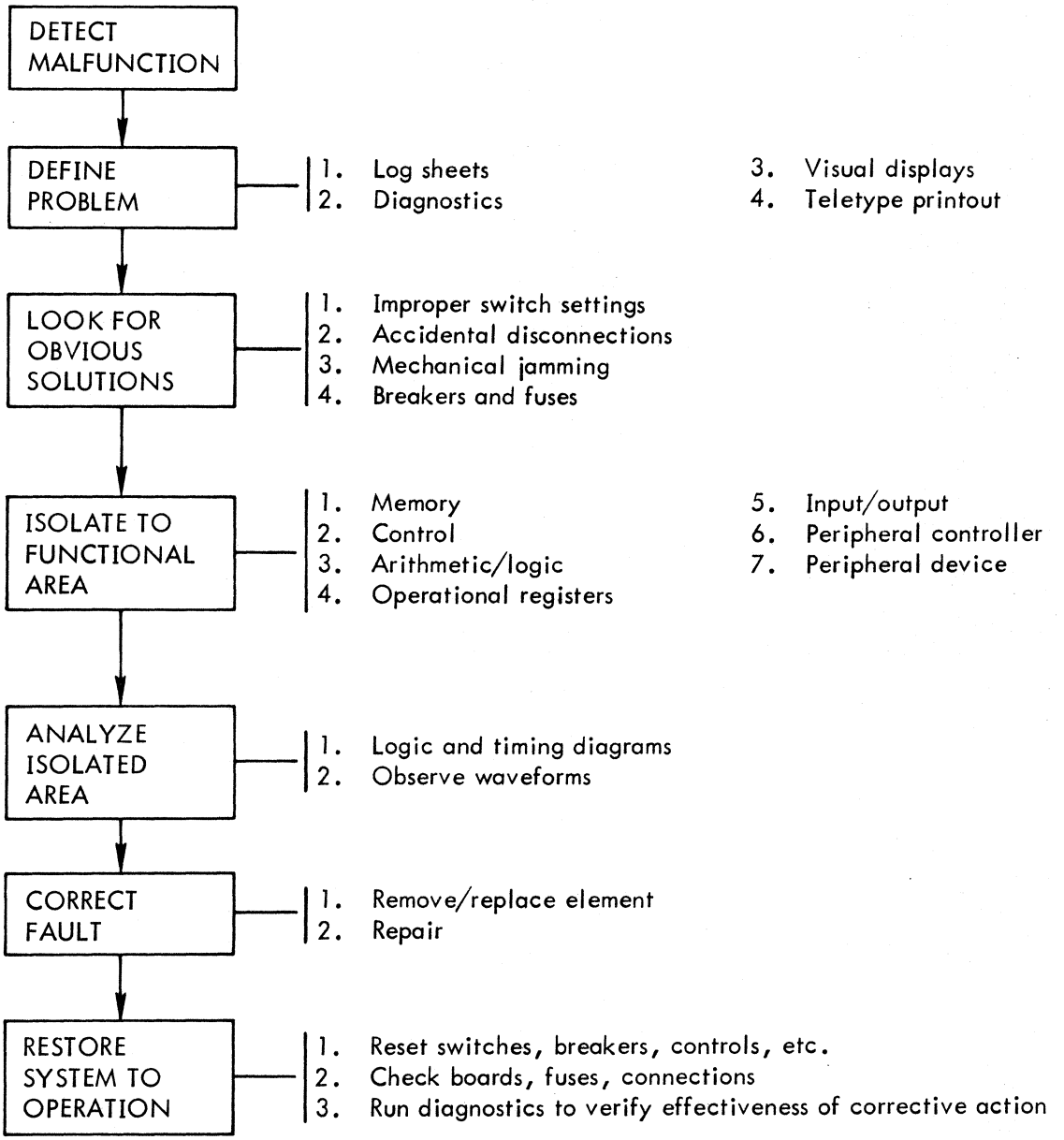

VTII-0519A

Figure V-1. General Troubleshooting Steps

1.4.1 Define the Problem

Define the problem thoroughly. For example, if the ADD instruction does not produce the correct results, is the fault a function of the sign (plus or minus), of the carries, or of some other element Are the operations registers being loaded properly Use the displays, connector pins, and integrated-circuit terminals for gathering the necessary data.

1.4.2 Look for Obvious Solutions

Make sure that a malfunction has actually occurred. Relate problems to recent events, such as cleaning or servicing. Look for improperly set controls or test equipment and accidental disconnections of plugs, etc. Consider miscellaneous temporary failure, such as mechanical jamming of peripheral equipment.

1.4.3 Isolate to a Functional Area

Isolate the fault to a functional area, such as memory, control, arithmetic logic, operations register, I/O, peripheral controller, or peripheral device. The process of isolating the malfunctioning area is generally a straightforward process of eliminating areas that are operating properly.

1.4.4 Analyze the Area

When the fault has been isolated to a functional area, use the logic and timing diagrams, and observe circuit waveforms to isolate the problem to an individual replaceable element. Put the computer in step mode (STEP indicator on) before removing input power.

1.4.5 Correct the Fault

Replace the faulty card or component. Before restoring power, take any necessary measures to prevent recurrence of the failure.

1.4.6 Restore the System to Normal Operation

When the system appears to be operating properly, return it to normal operating conditions. If circuit cards have been unseated, be sure all are properly reseated in the connectors. Set all controls and place the power switch in the PWR ON position. Finally, verify proper operation by running the test programs.

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1.5 SPECIFIC TROUBLESHOOTING PROCEDURES

When it has been determined that the computer is not operating properly, the general characteristics of the failure will, in most cases, immediately indicate the faulty section of the system.

If the failure is catastrophic and all instructions fail, the cause is usually in the timing, decoding, and control section.

Incorrect arithmetic operations or incorrect incrementing of the P register indicates the the failure is in the arithmetic and registers section.

Memory failures may be evidenced by repeated halts or by completely random instruction sequencing.

I/O failures are restricted to I/O instructions and are associated only with the logic of the I/O device. An I/O failure can be easily diagnosed if failure occurs in I/O routines and not in internal routines.

If reliable test programs indicate that the computer is not operating properly, apply the specific troubleshooting procedures outlined in sections 2, 3, and 4.

1.6 PRELIMINARY CPU CHECKS

In cases where no test programs will operate, the following procedures can be used to isolate failures.

1.6.1 Voltage Check

With the power supply disconnected, check for isolation between +5 volts and ground on all cards and on the motherboard. Check for isolation between +3 volts and ground, +3 volts and +5 volts on the motherboard, I/O control, I/O data, and the four data loop boards. If a ground condition exists, clear the ground before continuing.

With the power supply connected, check for the presence of +5 and +3 volts to ground at the proper pins on the motherboard.

Voltage tolerances are:

5.00 ± 0.25V dc
3.00 ± 0.15V dc

1.6.2 CPU Clock

Verify the proper operation of the CPU clock by measuring the following:

IOC-	Clock Board	P3-76	55-nanosecond period
ALC-	Clock Board	P3-72	110-nanosecond period (within scope accuracy of ± 3 percent)

In each case, check the pulsewidth at the 1.5V dc level for continuous variability (variable resistor R28 on the clock board) between 15 and 28 nanoseconds. Upon completion of test, adjust the pulsewidth to 24 nanoseconds (nominal).

1.6.3 Control Switches

Verify the proper operation of the following switches at the appropriate J46 or J47 connector pin on the motherboard.

RESET	RSS- RSS +	START	STRS- STRS +
INT (interrupt)	INTS- INTS +	SENSE 1	SENS1- SENS1 +
BOOTSTRAP	ABLS- ABLS +	SENSE 2	SENS2- SENS2 +
REPEAT	REPTS-	SENSE 3	SENS3- SENS3 +
STEP/RUN	STSW- RUNSW-		

The voltage limits are:

High: 3.3 ± 0.9V Low: 0.27 ± 0.13V

In each case, the first signal is low when the switch is down; the second, when the switch is up.

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1.6.4 Register Entry Switches and Display Indicators

Check the register entry switches (SW00-SW15) for proper operation at the appropriate J46 or J47 connector pin on the motherboard.

a. Set the switches (bits 15 through 0) to 0125252.

b. Press the X register switch.

c. Press LOAD.

d. Lift the X register switch. The pattern should be displayed.

e. Repeat steps a through d for the pattern 052525.

f. Repeat steps a through e for the B, A, I, and P registers. Since the P register has only 15 bits, the patterns for it are 025252 and 052525.

g. While checking the patterns in the P register, verify with an oscilloscope that the same patterns are stored in the L register. For reference, ABSxx- high equals zero; ABSxx- low, one.

ABS00-	ABS04-	ABS08-	ABS12-
ABS01-	ABS05-	ABS09-	ABS13-
ABS02-	ABS06-	ABS10-	ABS14-
ABS03-	ABS07-	ASB11-	ABS15-

Jumper P1-25 on control II to ground.

h. Press REPEAT and RUN; the I register should contain 005111; press START; the overflow (OVFL) indicator should light.

i. Press RESET; OVFL should go off.

The voltage levels for the register entry switches are the same as for the control switches (section 1.6.3).

1.6.5 CPU Internal Operations

The following sequences of instructions verify the data paths from the X, B, and A registers to the adder, the data paths from the adder to the X, B, and A registers, and the increment, decrement, and transfer input functions of the adder.

SEQUENCE 1

X Register	B Register	A Register	I Register	Instruction
000000	000000	125252	005014	TAX
000000	000000	052525	005012	TAB
000000	000000	000001	005016	TABX
000000	000000	000002	005016	TABX
000000	000000	000004	005016	TABX

Result:

X Register	B Register	A Register
125252	000000	125252
000000	052525	052525
000001	000001	000001
000002	000002	000002
000004	000004	000004

Note that, for TABX, bits 0-2 of the source A register are one. In the same manner, shift the one in the A register to bits 3-15 and verify that it is correctly transferred to the B and X registers by TABX (005016).

SEQUENCE 2

X Register	B Register	A Register	I Register	Instruction
000000	125252	000000	005021	TBA
000000	052525	000000	005024	TBX
000000	177776	000000	005125	IAXR
000000	177775	000000	005125	IAXR
000000	177773	000000	005125	IAXR

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Result

X Register	B Register	A Register
000000	125252	125252
052525	052525	000000
177777	177776	177777
177776	177775	177776
177774	177773	177774

Note that, for IAXR, bits 0-2 of the source B register are zero. In the same manner, shift the zero in the B register to bits 3-15 and verify that the value, incremented by one, is correctly transferred to the A and X registers by IAXR (005125).

SEQUENCE 3

X Register	B Register	A Register	I Register	Instruction
125252	000000	000000	005041	TXA
052525	000000	000000	005042	TXB
000001	000001	000000	005343	DXBAR
000002	000000	000000	005343	DXBAR
000004	000000	000000	005343	DXBAR

Result

X Register	B Register	A Register
125252	000000	125252
052525	052525	000000
000001	000000	000000
000002	000001	000001
000004	000003	000003

Note that, for DXBAR, bits 0-2 of the source X register are one. In the same manner, shift the one in the X register to bits 3-15 and verify the value, decremented by one, is transferred to the A and B registers by DXBAR (005343).

SEQUENCE 4

Check the control circuits for the remaining register operations and the complement

function of the adder. The register functions include transfer zeros, complement, and add and subtract overflow and the previous register operations contingent on the state of the OVFL flip-flop.

X Register	B Register	A Register	I Register	Instruction
000000	000000	125252	005211	CPA
000000	052525	000000	005222	CPB
177776	000000	000000	005244	CPX
000000	000000	100000	005311	DAR
177777	177777	177777	005007	TZABX
000007	000077	000777	005577	AOFABX*
000007	000077	000777	005577	AOFABX**
000001	000010	000100	005577	SOFABX*
000001	000010	000100	005577	SOFABX**
000000	000000	101010	005412	TAB/OVFL*
000000	010101	000000	005622	CPB/OVFL*
000050	000000	000000	005744	DXR/OVFL*
000000	000000	101010	005412	TAB/OVFL*
000000	010101	000000	005622	CPB/OVFL*
000050	000000	000000	005744	DXR/OVFL*

* OVFL = one.
** OVFL = zero.

Result

X Register	B Register	A Register
000000	000000	052525
000000	125252	000000
000001	000000	000000
000000	000000	077777
000000	000000	000000
000010	000100	001000
000007	000077	000777

X Register	B Register	A Register
000000	000007	000077
000001	000010	000100
000000	101010	101010
000000	101010	000000
000040	000000	000000
000000	000000	101010
000000	010101	000000
000050	000000	000000

1.6.6 Shift/Rotate Instructions

Check long logical rotate left, double-word end-around connections, and all shift counts.

A Register	B Register	Instruction
100000	000001	004441
100000	000001	004442
100000	000001	004443
100000	000001	004444
100000	000001	004445
100000	000001	004446
100000	000001	004447
100000	000001	004450
100000	000001	004451
100000	000001	004452
100000	000001	004453
100000	000001	004454
100000	000001	004455
100000	000001	004456
100000	000001	004457
100000	000001	004460
100000	000001	004461
100000	000001	004462
100000	000001	004463
100000	000001	004464
100000	000001	004465

A Register	B Register	Instruction
100000	000001	004466
100000	000001	004467
100000	000001	004470
100000	000001	004471
100000	000001	004472
100000	000001	004473
100000	000001	004474
100000	000001	004475
100000	000001	004476
100000	000001	004477
100000	000001	004440

Result

A Register	B Register
000000	000003
000000	000006
000000	000014
000000	000030
000000	000060
000000	000140
000000	000300
000000	000600
000000	001400
000000	003000
000000	006000
000000	014000
000000	030000
000000	060000
000000	140000
000001	100000
000003	000000
000006	000000
000014	000000
000030	000000
000060	000000
000140	000000
000300	000000
000600	000000

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A Register	B Register
001400	000000
003000	000000
006000	000000
014000	000000
030000	000000
060000	000000
140000	000000
100000	000001

Check the remainder of the shift/rotate instructions for connections and accuracy.

A Register	B Register	I Register	Instruction
177747	052525	004342	LSRA
177747	052525	004142	LSRB
177747	052525	004242	LRLA
177747	052525	004043	LRLB
177747	052525	004542	LLSR
177747	052525	004302	ASRA
177747	052525	004202	ASLA
177747	052525	004102	ASRB
177747	052525	004002	ASLB
177747	052525	004502	LASR
177747	052525	004402	LASL

Result

A Register	B Register
037771	052525
177747	012525
177637	052525
177747	125252
037771	152525
177771	052525
177634	052525
177747	012525
177747	052524
177771	072525
177636	052524

1.6.7 Memory Operand Instructions

Check the indexing and indirect capabilities of one- and two-word addressing arithmetic and logic instructions:

a. Store the A register (one-word), indexed by the X, B, and P registers and indirect.

P Reg.	A Reg.	B Reg.	X Reg.	I Reg.	Memory
000050	125252	000070	000000	056333	
000050	052525	000000	000070	055333	
000050	125252	000000	000000	054333	
000050	177777	000000	000000	057333	(000333) = 000423

Result

P Register*	Memory
000051	(000423) = 125252
000051	(000423) = 052525
000051	(000423) = 052525
	(000403) = 125252
000051	(000423) = 177777

* Registers unchanged except P.

b. Store the A register (two-word), postindexed by the X, B, and P registers and indirect.

P Reg.	A Reg.	B Reg.	X Reg.	I Reg.	Memory
000777	125252	000070	000000	006056	(001000) = 001001
000777	125252	000000	000070	006055	(001000) = 001011
000777	125252	000000	000000	006054	(001000) = 001001
000777	177777	000000	000000	006057	(001000) = 100200
					(000200) = 001001

Result

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P Register*	Memory
001001	(001070) = 125252
001001	(001101) = 125252
001001	(002000) = 125252
001001	(001001) = 177777

* Registers unchanged except P.

c. Indirect and preindexed by the B register (OPA denotes operand address).

Sequence	Result
P = P	P = P + 2
A = 107070	(OPA2) = 107070
B = 000050	
X = 000000	
I = 006256	
(P + 1) = OPA1	
(OPA1 + 50) = OPA2	

d. Indirect and postindexed by the X register.

Sequence	Result
P = P	P = P + 2
A = 070707	(OPA2 + 1) = 070707
B = 000000	
X = 000001	
I = 006055	
(P + 1) = OPA1	
(OPA1) = OPA2 = 1xxxxx	

Check the control circuits for the remaining memory operand instructions and the logical and arithmetic functions of the adder.

a. One-word addressing control and adder functions.

(OPA1) = 052525
(OPA2) = 125252

A Register	I Register	Instruction	Result, A Register
052525	12OPA1	ADD	125252
125252	12OPA2		052524
125252	12OPA1		177777
052525	12OPA2		177777
052525	14OPA1	SUB	000000
215252	14OPA2		000000
125252	14OPA1		052525
052525	14OPA2		125253
052525	11OPA1	ORA	052525
125252	11OPA2		125252
125252	11OPA1		177777
052525	11OPA2		177777
052525	13OPA1	ERA	000000
125252	13OPA2		000000
125252	13OPA1		177777
052525	13OPA2		177777
052525	15OPA1	ANA	052525
125252	15OPA2		125252
125252	15OPA1		000000
052525	15OPA2		000000

A Register	B Register	X Register	I register	Instruction
000000	000000	000000	01OPA1	LDA
000000	000000	000000	02OPA2	LDB
000000	000000	000000	03OPA2	LDX
000000	000000	000000	04OPA1	INR
000000	060000	000000	06OPA1	STB
000000	000000	070000	07OPA2	STX

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Result

A Register	B Register	X Register
052525	000000	000000
000000	125252	000000
000000	000000	125252
000000	000000	000000
	(OPA1) = 052526	
000000	060000	000000
	(OPA1) = 060000	
000000	000000	070000
	(OPA2) = 070000	

b. Two-word extended control circuits and adder functions. All registers and memory addresses remain unchanged except as noted in result column.

Sequence	Instruction	Result
P = P A = 111111 B = 000000 X = 000000 I = 006057 (P + 1) = OPA1 direct	STAE	P = P + 2 (OPA1) = 111111
P = P A = 000000 B = 022222 X = 000000 I = 006067 (P + 1) = OPA2 direct	STBE	P = P + 2 (OPA2) = 022222
P = P A = 000000 B = 000000 X = 044444 I = 006077 (P + 1) = OPA3 direct	STXE	P = P + 2 (OPA3) = 044444
P = P A = 000000 B = 000000 X = 000000	LDAE	P = P + 2 A = 044444

Sequence	Instruction	Result
I = 006017 (P + 1) = OPA3		
P = P A = 000000 B = 000000 X = 000000 I = 006027 (P + 1) = OPA1 direct	LDBE	P = P + 2 B = 111111
P = P A = 000000 B = 000000 X = 000000 I = 006027 (P + 1) = OPA2 direct	LDXE	P = P + 2 X = 022222
P = P A = 000000 B = 000000 X = 000000 I = 006047 (P + 1) = OPA1	INRE	P = P + 2 (OPA1) = 111112
P = P A = 060606 B = 000000 X = 000000 I = 006127 (P + 1) = OPA2	ADDE	P = P + 2 A = 103030
P = P A = 111111 B = 000000 X = 000000 I = 006147 (P + 1) = OPA1	SUBE	P = P + 2 A = 177777
P = P A = 066665	ORAE	P = P + 2 A = 177777

Sequence	Instruction	Result
B = 000000 X = 000000 I = 006317 (P + 1) = OPA1		
P = P A = 177000 B = 000000 X = 000000 I = 006337 (P + 1) = OPA2	ERAE	P = P + 2 A = 155222
P = P A = 177000 B = 000000 X = 000000 I = 006357 (P + 1) = OPA3	ANAE	P = P + 2 A = 044000
P = P A = 101010 B = 000000 X = 000000 I = 006050 (P + 1) = 000000	STAI	P = P + 2 (P + 1) = 101010
P = P A = 000000 B = 000000 X = 000000 I = 006033 (P + 1) = 123456	LDXI	P = P + 2 X = 123456

1.6.8 Conditional Instructions

Check the test condition logic, and the control circuits for the jump instruction. In the following sequence, the instruction in the I register is:

Instruction	Description
001006	Jump if A register positive and negative. Test must fail.
001775	Jump if SENSE switches set; X, B, and A registers equal zero; overflow set; and A register negative. Test must fail.
001773	Jump if SENSE switches set; X, B, and A registers equal zero; overflow set; and A register positive. Test is successful when conditions are met. In the last seven tests, one of the conditions is not met and the test fails.
001777	Jump if SENSE switches not set; X, B, and A registers equal nonzero; and overflow set. Test is successful when conditions are met. In the last seven tests, one of the conditions is not met and the test fails.
001776	Jump if SENSE switches not set; and X, B, and A registers nonzero. Test is successful when conditions are met.

SS3	SS2	SS1	X Reg.	B Reg.	A Reg.	OVFL	I Reg.
0	0	0	xxxxxx	xxxxxx	xxxxxx	x	001006
1	1	1	000000	000000	000000	1	001775
1	1	1	000000	000000	000000	1	001773
0	1	1	000000	000000	000000	1	001773
1	0	1	000000	000000	000000	1	001773
1	1	0	000000	000000	000000	1	001773
1	1	1	000000	000000	000000	1	001773
1	1	1	000000	000001	000000	1	001773
1	1	1	000000	000000	000010	1	001773
1	1	1	000000	000000	000000	0	001773
0	0	0	000010	000100	001000	0	001777
1	0	0	000010	000100	001000	0	001777
0	1	0	000010	000100	001000	0	001777
0	0	1	000010	000100	001000	0	001777

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SS3	SS2	SS1	X Reg.	B Reg.	A Reg.	OVFL	I Reg.
0	0	0	000000	000100	001000	0	001777
0	0	0	000010	000000	001000	0	001777
0	0	0	000010	000100	000000	0	001777
0	0	0	000010	000100	001000	1	001777
0	0	0	000010	000100	001000	0	001776
0	0	0	000010	000100	001000	1	001776

To completely check the zero detect logic:

a. Set all SENSE switches.

b. Set OVFL to zero.

c. Set the I register to 001777.

d. Set the X, B, and A registers to zero, except one bit each.

e. Repeatedly execute the instruction, moving the one from bit 0 to bit 15 in each register. In each case, the jump address (P + 1) must be transferred to the P register.

Check control for the jump-and-mark instructions. JMPAD denotes the jump address.

Sequence	Instruction	Result
I = 002002 A = 000000 P = P (P + 1) = JMPAD (JMPAD) = 000000	JAPM	P = JMPAD1 (JMPAD) = P + 2
I = 002002 A = 100000 P = P (P + 1) = JMPAD (JMPAD) = 000000	JAPM	P = P + 2

Check control for the execute instructions.

Sequence	Instruction	Result
I = 003010 A = 111111 P = P (P + 1) = EXAD (EXAD1) = OPA (OPA) = 000000	EXAZ	P = P + 2
I = 003010 A = 000000 P = P (P + 1) = EXAD (EXAD) = STAE direct (EXAD1) = OPA (OPA) = 177777	EXAZ	P = P + 2 (OPA) = 000000

1.6.9 Miscellaneous Instructions

Halt:

Sequence	Result
P = ADD1 A = 000000 I = 000000 (ADD1) = 005111 (ADD2) = 000777 Set run mode and press START	P = ADD2 + 1 A = 000001 I = 000777

Set/Reset Overflow:

OVFL	Instruction	I Reg.	Result
0	SOF	007401	OVFL = 1
1	ROF	007400	OVFL = 0
1	JOF	001001	OVFL = 0
1	JOFN	001007	OVFL = 0

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Increment Memory and Replace:

Sequence	Result
P = P I = 006040 (P + 1) = 077777 OVFL = 0	P = P + 2 (P + 1) = 077777
P = P I = 006040 (P + 1) = 077777 OVFL = 0	P = P + 2 (P + 1) = 100000

Increment Registers:

OVFL	P Reg.	A Reg.	I Reg.	Instruction
0	P	077776	005111	IAR
0	P	077777	005111	IAR
		B Reg.		
0	P	077776	005122	IBR
0	P	077777	005122	IBR
		X Reg.		
0	P	077776	005144	IXR
0	P	077777	005144	IXR

	Result	
P Reg.	**OVFL**	**A Reg.**
P + 1	0	077777
P + 1	1	100000
P + 1	0	077777
P + 1	1	100000
P + 1	0	077777
P + 1	1	100000

Decrement Registers:

OVFL	P Reg.	A Reg.	I Reg.	Instruction
0	P	100001	005311	DAR
0	P	100000	005311	DAR
		B Reg.		
0	P	100001	005322	DBR
0	P	100000	005322	DBR
		X Reg.		
0	P	100001	005344	DXR
0	P	100000	005344	DXR

Result

P Reg.	OVFL	A Reg.
P + 1	0	100000
P + 1	1	077777
P + 1	0	100000
P + 1	1	077777
P + 1	0	000000
P + 1	1	177777

Arithmetic Instructions:

Sequence	Instruction	Result
P = P I = 12OPA A = 077666 (OPA) = 000111 OVFL = 0	ADD	P = P + 2 A = 077777 OVFL = 0
P = P I = 12OPA A = 077777 OVFL = 0 (OPA) = 000001	ADD	P = P + 1 A = 100000 OVFL = 1

Sequence	Instruction	Result
P = P I = 14OPA A = 100001 OVFL = 0 (OPA) = 000001	SUB	P = P + 1 A = 100000 OVFL = 1
P = P I = 14OPA A = 100000 OVFL = 0 (OPA) = 000001	SUB	P = P + 1 A = 177777 OVFL = 0

1.6.10 I/O Instructions

Verify that device address and function codes for each I/O instruction, if applicable, are generated on the internal (ABxx-I) and external (EBxx-1) E bus in both logic states when FRYX is active.

Verify that for each I/O data transfer instruction a data line is also generated in both logic states when DRYX is active.

The instructions to be verified are:

EXC	INA	IME	CIAB	OBR
EXCA	INB	CIA	OME	OAB
SEN	INAB	CIB	OAR	

The TTY can be used to check most of the programmed-I/O instructions.

1.6.11 Interrupt Operation

Verify that interrupts do not occur immediately after an I/O, halt, or shift instruction; any two-word addressing instruction; multiply or divide instruction; or while the CPU is in step mode.

The control panel INT switch can be used to check the interrupt function. INT should be wired to be lowest in priority. Ground PRMX-I when no other I/O controllers are being used. Interrupt addresses are 000000 and 000001.

The following sequences verify that the interrupt function is operating properly:

```
000000      SOF
000001      HLT

000004      NOP         Start here
000005      JMP
000006      000004
```

In run mode, start the program at 000004. Press INT; the overflow indicator should light and the CPU remain running in the NOP-JMP loop. Press RESET to turn off the overflow indicator.

```
000000      JMPM
000001      000010
000002      HLT 1

000004      NOP         Start here
000005      JMP
000006      000004
000007      000000
000010      (000000)    LOC 5
000011      SOF
000012      HLT 2
```

In the run mode, start the program at 000004. Press INT; the overflow indicator should light and the I register should contain HLT 2. Memory address 000010 should contain 000005 (interrupt address plus one).

The timing of IUJX should be checked with respect to IUAX. The JMPM interrupt test can cycle IUJX; change 000011 and 000012 to jump indirect to 000010.

1.6.12 Direct Memory Access (DMA)

Verify that data can be stored and read from memory via DMA in both step and run modes.

Verify that other memory addresses are not disturbed.

Verify that the computer remains in the same mode during and after the DMA transfers.

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Verify the operation of each address line (FRYX active) and data line (DRYX active) in both logic states.

Verify that DMA seuqneces can be extended by priority memory access without losing DMA data.

1.6.13 Optional Instruction Set

With the board installed, repeat the tests described in sections 1.6.5 and 1.6.9 to verify that the CPU operates correctly with this option.

1.6.14 Memory Protection (MP)

With the MP installed, repeat the tests described in sections 1.6.5 and 1.6.9 to verify that the CPU continues to operate correctly.

1.6.15 Priority Memory Access (PMA)

With the PMA installed, repeat the tests described in sections 1.6.5 and 1.6.9 to verify that the CPU continues to operate correctly.

1.6.16 Real-Time Clock (RTC)

With the RTC installed, repeat the tests described in sections 1.6.5 and 1.6.9 to verify that the CPU continues to operate correctly.

1.6.17 Automatic Bootstrap Loader (ABL)

With the ABL installed, repeat the tests described in sections 1.6.5 and 1.6.9 to verify that the CPU continues to operate correctly.

1.6.18 Power Failure/Restart (PF/R)

With the PF/R installed, repeat the tests described in sections 1.6.5 and 1.6.9 to verify that the CPU continues to operate correctly.

1.7 MARGIN TESTS

1.7.1 CPU Power Margins

Run the instructions test program of MAINTAIN II, checking that it operates correctly with the +5-volt supply varied between +5.25 and +4.75 (1 minute at each extreme of the range).

1.7.2 Clock Period Margins

Verify that the instructions test operates correctly for 1 minute with a 20-MHz crystal (or equivalent 100-nanosecond clock period) installed on the clock board (44P0440); +5 volts at +5.00 ± 0.05V.

1.7.3 Pulsewidth Margins

Verify that the instructions test operates correctly for 1 minute while the pulsewidth (IOC- at P3-76 of clock board) is varied between 15 and 18 nanoseconds at the 1.5V dc level (R28 on clock board).

1.7.4 Maximum Clock Frequency

Check for maximum clock frequency at which the instructions test operates correctly. Vary +5 volts between +5.00 and +4.75 volts, as needed. Note the maximum frequency and the voltage range over which it operates correctly; pulsewidth nominal. Run 1 minute at each extreme of the voltage range.

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MAINTENANCE

SECTION 2
CENTRAL PROCESSING UNIT

To be supplied.

SECTION 3
MEMORY

To be supplied.

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SECTION 4
INPUT/OUTPUT

To be supplied.

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APPENDIX A

INDEX OF INTERNAL INSTRUCTIONS

Mnemonic	Instruction	Group	Format
*	Asterisks denote optional instructions		
ADD	Add memory to A register	6	1
ADDE	Add extended	6	3
ADDI	Add immediate	6	2
ANA	AND memory and A register	4	1
ANAE	AND extended	4	3
ANAI	AND immediate	4	2
AOFA	Add overflow to A register	5	1
AOFB	Add overflow to B register	5	1
AOFX	Add overflow to X register	5	1
ASLA	Arithmetic shift left A register	5	1
ASLB	Arithmetic shift left B register	5	1
ASRA	Arithmetic shift right A register	5	1
ASRB	Arithmetic shift right B register	5	1
*BT	Bit test	7	4b
CPA	Complement A register	5	1
CPB	Complement B register	5	1
CPX	Complement X register	5	1
DAR	Decrement A register	5	1
DBR	Decrement B register	5	1
*DIV	Divide	6	1
*DIVE	Divide extended	6	3
*DIVI	Divide immediate	6	2
DXR	Decrement X register	5	1
ERA	Exclusive-OR memory and A register	4	1
ERAE	Exclusive-OR extended	4	3

APPENDIX A

INDEX OF INTERNAL INSTRUCTIONS *(continued)*

Mnemonic	Instruction	Group	Format
ERAI	Exclusive-OR immediate	4	2
HLT	Halt	1	1
IAR	Increment A register	5	1
IBR	Increment B register	5	1
IJMP	Jump indexed	7	4a
INR	Increment memory and replace	6	1
INRE	Increment memory and replace extended	6	3
INRI	Increment memory and replace immediate	6	3
IXR	Increment X register	5	1
JAN	Jump if A register negative	7	4
JANM	Jump and mark if A register negative	8	4
JANZ	Jump if A register not zero	7	4
JANZM	Jump and mark if A register not zero	8	4
JAP	Jump if A register positive	7	4
JAPM	Jump and mark if A register positive	8	4
JAZ	Jump if A register zero	7	4
JAZM	Jump and mark if A register zero	8	4
JBNZ	Jump if B register not zero	7	4
JBNZM	Jump and mark if B register not zero	8	4
JBZ	Jump if B register zero	7	4
JBZM	Jump and mark if B register zero	8	4
JIF	Jump if (general)	7	4
JMIF	Jump and mark if (general)	8	4
JMP	Jump (unconditional)	7	4
JMPM	Jump and mark (unconditional)	8	4
JOF	Jump if overflow indicator	7	4

APPENDIX A

INDEX OF INTERNAL INSTRUCTIONS *(continued)*

Mnemonic	Instruction	Group	Format
	set		
JOFM	Jump and mark if overflow indicator set	8	4
JOFN	Jump if overflow indicator not set	7	4
JOFNM	Jump and mark if overflow indicator not set	8	4
JS1M	Jump and mark if SENSE switch 1 set	8	4
JS2M	Jump and mark if SENSE switch 2 set	8	4
JS3M	Jump and mark if SENSE switch 3 set	8	4
JSR	Jump and set return in index register	7	4a
JSS1	Jump if SENSE switch 1 set	7	4
JSS2	Jump if SENSE switch 2 set	7	4
JSS3	Jump if SENSE switch 3 set	7	4
JS1N	Jump if SENSE switch 1 not set	7	4
JS2N	Jump if SENSE switch 2 not set	7	4
JS3N	Jump if SENSE switch 3 not set	7	4
JS1NM	Jump and mark if SENSE switch 1 not set	8	4
JS2NM	Jump and mark if SENSE switch 2 not set	8	4
JS3NM	Jump and mark if SENSE switch 3 not set	8	4
JXNZ	Jump if X register not zero	7	4
JXNZM	Jump and mark if X register not zero	8	4
JXZ	Jump if X register zero	7	4
JXZM	Jump and mark if X register zero	8	4
LASL	Long arithmetic shift left	5	1
LASR	Long arithmetic shift right	5	1
LDA	Load A register	2	1a
LDAE	Load A regiseter extended	2	3

APPENDIX A

INDEX OF INTERNAL INSTRUCTIONS *(continued)*

Mnemonic	Instruction	Group	Format
LDAI	Load A register immediate	2	2
LDB	Load B register	2	1a
LDBE	Load B register extended	2	3
LDBI	Load B register immediate	2	2
LDX	Load X register	2	1a
LDXE	Load X register extended	2	3
LDXI	Load X register immediate	2	2
LLRL	Long logical rotation left	5	1
LLSR	Long logical rotation right	5	1
LRLA	Logical rotation left A register	5	1
LRLB	Logical rotation left B register	5	1
LSRA	Logical shift right A register	5	1
LSRB	Logical shift right B register	5	1
*MUL	Multiply	6	1a
*MULE	Multiply extended	6	3
*MULI	Multiply immediate	6	2
NOP	No operation	1	1b
ORA	Inclusive-OR memory and A register	4	1a
ORAE	Inclusive-OR extended	4	3
ORAI	Inclusive-OR immediate	4	2
ROF	Reset overflow indicator	1	1
SOF	Set overflow indicator	1	1
SOFA	Subtract overflow from A register	5	1b
SOFB	Subtract overflow from B register	5	1b
SOFX	Subtract overflow from X register	5	1b
*SRE	Skip if register equal to memory	4	3a
STA	Store A register	2	1a
STAE	Store A register extended	2	3
STAI	Store A register immediate	2	2
STB	Store B register	2	1a
STBE	Store B register extended	2	3

APPENDIX A

INDEX OF INTERNAL INSTRUCTIONS *(continued)*

Mnemonic	Instruction	Group	Format
STBI	Store B register immediate	2	2
STX	Store X register	2	1a
STXE	Store X register extended	2	3
STXI	Store X register immediate	2	2
SUB	Subtract memory from A register	6	1a
SUBE	Subtract extended	6	3
SUBI	Subtract immediate	6	2
TAB	Transfer A register to B register	3	1b
TAX	Transfer A register to X register	3	1b
TBA	Transfer B register to A register	3	1b
TBX	Transfer B register to X X register	3	1b
*TSA	Load A register with switches	3	1
TXA	Transfer X register to A register	3	1b
TXB	Transfer X register to B register	3	1b
TZA	Transfer zero to A register	3	1b
TZB	Transfer zero to B register	3	1b
TZX	Transfer zero to X register	3	1b
XAN	Execute if A register negative	9	5
XANZ	Execute if A register not zero	9	5
XAP	Execute if A register positive	9	5
XAZ	Execute if A register zero	9	5
XBNZ	Execute if B register not zero	9	5
XBZ	Execute if B register zero	9	5
XEC	Execute (unconditional)	9	5
XIF	Execute if (general)	9	5
XOF	Execute if overflow indicator set	9	5
XOFN	Execute if overflow indicator	9	5

APPENDIX A

INDEX OF INTERNAL INSTRUCTIONS *(continued)*

Mnemonic	Instruction	Group	Format
	not set		
XS1	Execute if SENSE switch 1 set	9	5
XS2	Execute if SENSE switch 2 set	9	5
XS3	Execute if SENSE switch 3 set	9	5
XS1N	Execute if SENSE switch 1 not set	9	5
XS2N	Execute if SENSE switch 2 not set	9	5
XS3N	Execute if SENSE switch 3 not set	9	5
XXNZ	Execute if X register not zero	9	5
XXZ	Execute if X register zero	9	5

APPENDIX B

INDEX OF INPUT/OUTPUT INSTRUCTIONS

Mnemonic	Instruction
CIA	Clear and input to A register
CIB	Clear and input to B register
EXC	External control
IME	Input to memory
INA	Input to A register
INB	Input to B register
OAR	Output from A register
OBR	Output from B register
OME	Output from memory
SEN	Program sense

APPENDIX C

POWERS OF TWO

2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0.000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0.000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0.000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0.000 000 000 001 818 989 403 545 856 475 830 078 125

APPENDIX D

OCTAL-DECIMAL INTEGER CONVERSIONS

0000 to 0777 (Octal)	0000 to 0511 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
0000	0000	0001	0002	0003	0004	0005	0006	0007
0010	0008	0009	0010	0011	0012	0013	0014	0015
0020	0016	0017	0018	0019	0020	0021	0022	0023
0030	0024	0025	0026	0027	0028	0029	0030	0031
0040	0032	0033	0034	0035	0036	0037	0038	0039
0050	0040	0041	0042	0043	0044	0045	0046	0047
0060	0048	0049	0050	0051	0052	0053	0054	0055
0070	0056	0057	0058	0059	0060	0061	0062	0063
0100	0064	0065	0066	0067	0068	0069	0070	0071
0110	0072	0073	0074	0075	0076	0077	0078	0079
0120	0080	0081	0082	0083	0084	0085	0086	0087
0130	0088	0089	0090	0091	0092	0093	0094	0095
0140	0096	0097	0098	0099	0100	0101	0102	0103
0150	0104	0105	0106	0107	0108	0109	0110	0111
0160	0112	0113	0114	0115	0116	0117	0118	0119
0170	0120	0121	0122	0123	0124	0125	0126	0127
0200	0128	0129	0130	0131	0132	0133	0134	0135
0210	0136	0137	0138	0139	0140	0141	0142	0143
0220	0144	0145	0146	0147	0148	0149	0150	0151
0230	0152	0153	0154	0155	0156	0157	0158	0159
0240	0160	0161	0162	0163	0164	0165	0166	0167
0250	0168	0169	0170	0171	0172	0173	0174	0175
0260	0176	0177	0178	0179	0180	0181	0182	0183
0270	0184	0185	0186	0187	0188	0189	0190	0191
0300	0192	0193	0194	0195	0196	0197	0198	0199
0310	0200	0201	0202	0203	0204	0205	0206	0207
0320	0208	0209	0210	0211	0212	0213	0214	0215
0330	0216	0217	0218	0219	0220	0221	0222	0223
0340	0224	0225	0226	0227	0228	0229	0230	0231
0350	0232	0233	0234	0235	0236	0237	0238	0239
0360	0240	0241	0242	0243	0244	0245	0246	0247
0370	0248	0249	0250	0251	0252	0253	0254	0255

	0	1	2	3	4	5	6	7
0400	0256	0257	0258	0259	0260	0261	0262	0263
0410	0264	0265	0266	0267	0268	0269	0270	0271
0420	0272	0273	0274	0275	0276	0277	0278	0279
0430	0280	0281	0282	0283	0284	0285	0286	0287
0440	0288	0289	0290	0291	0292	0293	0294	0295
0450	0296	0297	0298	0299	0300	0301	0302	0303
0460	0304	0305	0306	0307	0308	0309	0310	0311
0470	0312	0313	0314	0315	0316	0317	0318	0319
0500	0320	0321	0322	0323	0324	0325	0326	0327
0510	0328	0329	0330	0331	0332	0333	0334	0335
0520	0336	0337	0338	0339	0340	0341	0342	0343
0530	0344	0345	0346	0347	0348	0349	0350	0351
0540	0352	0353	0354	0355	0356	0357	0358	0359
0550	0360	0361	0362	0363	0364	0365	0366	0367
0560	0368	0369	0370	0371	0372	0373	0374	0375
0570	0376	0377	0378	0379	0380	0381	0382	0383
0600	0384	0385	0386	0387	0388	0389	0390	0391
0610	0392	0393	0394	0395	0396	0397	0398	0399
0620	0400	0401	0402	0403	0404	0405	0406	0407
0630	0408	0409	0410	0411	0412	0413	0414	0415
0640	0416	0417	0418	0419	0420	0421	0422	0423
0650	0424	0425	0426	0427	0428	0429	0430	0431
0660	0432	0433	0434	0435	0436	0437	0438	0439
0670	0440	0441	0442	0443	0444	0445	0446	0447
0700	0448	0449	0450	0451	0452	0453	0454	0455
0710	0456	0457	0458	0459	0460	0461	0462	0463
0720	0464	0465	0466	0467	0468	0469	0470	0471
0730	0472	0473	0474	0475	0476	0477	0478	0479
0740	0480	0481	0482	0483	0484	0485	0486	0487
0750	0488	0489	0490	0491	0492	0493	0494	0495
0760	0496	0497	0498	0499	0500	0501	0502	0503
0770	0504	0505	0506	0507	0508	0509	0510	0511

1000 to 1777 (Octal)	0512 to 1023 (Decimal)

	0	1	2	3	4	5	6	7
1000	0512	0513	0514	0515	0516	0517	0518	0519
1010	0520	0521	0522	0523	0524	0525	0526	0527
1020	0528	0529	0530	0531	0532	0533	0534	0535
1030	0536	0537	0538	0539	0540	0541	0542	0543
1040	0544	0545	0546	0547	0548	0549	0550	0551
1050	0552	0553	0554	0555	0556	0557	0558	0559
1060	0560	0561	0562	0563	0564	0565	0566	0567
1070	0568	0569	0570	0571	0572	0573	0574	0575
1100	0576	0577	0578	0579	0580	0581	0582	0583
1110	0584	0585	0586	0587	0588	0589	0590	0591
1120	0592	0593	0594	0595	0596	0597	0598	0599
1130	0600	0601	0602	0603	0604	0605	0606	0607
1140	0608	0609	0610	0611	0612	0613	0614	0615
1150	0616	0617	0618	0619	0620	0621	0622	0623
1160	0624	0625	0626	0627	0628	0629	0630	0631
1170	0632	0633	0634	0635	0636	0637	0638	0639
1200	0640	0641	0642	0643	0644	0645	0646	0647
1210	0648	0649	0650	0651	0652	0653	0654	0655
1220	0656	0657	0658	0659	0660	0661	0662	0663
1230	0664	0665	0666	0667	0668	0669	0670	0671
1240	0672	0673	0674	0675	0676	0677	0678	0679
1250	0680	0681	0682	0683	0684	0685	0686	0687
1260	0688	0689	0690	0691	0692	0693	0694	0695
1270	0696	0697	0698	0699	0700	0701	0702	0703
1300	0704	0705	0706	0707	0708	0709	0710	0711
1310	0712	0713	0714	0715	0716	0717	0718	0719
1320	0720	0721	0722	0723	0724	0725	0726	0727
1330	0728	0729	0730	0731	0732	0733	0734	0735
1340	0736	0737	0738	0739	0740	0741	0742	0743
1350	0744	0745	0746	0747	0748	0749	0750	0751
1360	0752	0753	0754	0755	0756	0757	0758	0759
1370	0760	0761	0762	0763	0764	0765	0766	0767

	0	1	2	3	4	5	6	7
1400	0768	0769	0770	0771	0772	0773	0774	0775
1410	0776	0777	0778	0779	0780	0781	0782	0783
1420	0784	0785	0786	0787	0788	0789	0790	0791
1430	0792	0793	0794	0795	0796	0797	0798	0799
1440	0800	0801	0802	0803	0804	0805	0806	0807
1450	0808	0809	0810	0811	0812	0813	0814	0815
1460	0816	0817	0818	0819	0820	0821	0822	0823
1470	0824	0825	0826	0827	0828	0829	0830	0831
1500	0832	0833	0834	0835	0836	0837	0838	0839
1510	0840	0841	0842	0843	0844	0845	0846	0847
1520	0848	0849	0850	0851	0852	0853	0854	0855
1530	0856	0857	0858	0859	0860	0861	0862	0863
1540	0864	0865	0866	0867	0868	0869	0870	0871
1550	0872	0873	0874	0875	0876	0877	0878	0879
1560	0880	0881	0882	0883	0884	0885	0886	0887
1570	0888	0889	0890	0891	0892	0893	0894	0895
1600	0896	0897	0898	0899	0900	0901	0902	0903
1610	0904	0905	0906	0907	0908	0909	0910	0911
1620	0912	0913	0914	0915	0916	0917	0918	0919
1630	0920	0921	0922	0923	0924	0925	0926	0927
1640	0928	0929	0930	0931	0932	0933	0934	0935
1650	0936	0937	0938	0939	0940	0941	0942	0943
1660	0944	0945	0946	0947	0948	0949	0950	0951
1670	0952	0953	0954	0955	0956	0957	0958	0959
1700	0960	0961	0962	0963	0964	0965	0966	0967
1710	0968	0969	0970	0971	0972	0973	0974	0975
1720	0976	0977	0978	0979	0980	0981	0982	0983
1730	0984	0985	0986	0987	0988	0989	0990	0991
1740	0992	0993	0994	0995	0996	0997	0998	0999
1750	1000	1001	1002	1003	1004	1005	1006	1007
1760	1008	1009	1010	1011	1012	1013	1014	1015
1770	1016	1017	1018	1019	1020	1021	1022	1023

APPENDIX D

OCTAL-DECIMAL INTEGER CONVERSIONS *(continued)*

	0	1	2	3	4	5	6	7
2000	1024	1025	1026	1027	1028	1029	1030	1031
2010	1032	1033	1034	1035	1036	1037	1038	1039
2020	1040	1041	1042	1043	1044	1045	1046	1047
2030	1048	1049	1050	1051	1052	1053	1054	1055
2040	1056	1057	1058	1059	1060	1061	1062	1063
2050	1064	1065	1066	1067	1068	1069	1070	1071
2060	1072	1073	1074	1075	1076	1077	1078	1079
2070	1080	1081	1082	1083	1084	1085	1086	1087
2100	1088	1089	1090	1091	1092	1093	1094	1095
2110	1096	1097	1098	1099	1100	1101	1102	1103
2120	1104	1105	1106	1107	1108	1109	1110	1111
2130	1112	1113	1114	1115	1116	1117	1118	1119
2140	1120	1121	1122	1123	1124	1125	1126	1127
2150	1128	1129	1130	1131	1132	1133	1134	1135
2160	1136	1137	1138	1139	1140	1141	1142	1143
2170	1144	1145	1146	1147	1148	1149	1150	1151
2200	1152	1153	1154	1155	1156	1157	1158	1159
2210	1160	1161	1162	1163	1164	1165	1166	1167
2220	1168	1169	1170	1171	1172	1173	1174	1175
2230	1176	1177	1178	1179	1180	1181	1182	1183
2240	1184	1185	1186	1187	1188	1189	1190	1191
2250	1192	1193	1194	1195	1196	1197	1198	1199
2260	1200	1201	1202	1203	1204	1205	1206	1207
2270	1208	1209	1210	1211	1212	1213	1214	1215
2300	1216	1217	1218	1219	1220	1221	1222	1223
2310	1224	1225	1226	1227	1228	1229	1230	1231
2320	1232	1233	1234	1235	1236	1237	1238	1239
2330	1240	1241	1242	1243	1244	1245	1246	1247
2340	1248	1249	1250	1251	1252	1253	1254	1255
2350	1256	1257	1258	1259	1260	1261	1262	1263
2360	1264	1265	1266	1267	1268	1269	1270	1271
2370	1272	1273	1274	1275	1276	1277	1278	1279

	0	1	2	3	4	5	6	7
2400	1280	1281	1282	1283	1284	1285	1286	1287
2410	1288	1289	1290	1291	1292	1293	1294	1295
2420	1296	1297	1298	1299	1300	1301	1302	1303
2430	1304	1305	1306	1307	1308	1309	1310	1311
2440	1312	1313	1314	1315	1316	1317	1318	1319
2450	1320	1321	1322	1323	1324	1325	1326	1327
2460	1328	1329	1330	1331	1332	1333	1334	1335
2470	1336	1337	1338	1339	1340	1341	1342	1343
2500	1344	1345	1346	1347	1348	1349	1350	1351
2510	1352	1353	1354	1355	1356	1357	1358	1359
2520	1360	1361	1362	1363	1364	1365	1366	1367
2530	1368	1369	1370	1371	1372	1373	1374	1375
2540	1376	1377	1378	1379	1380	1381	1382	1383
2550	1384	1385	1386	1387	1388	1389	1390	1391
2560	1392	1393	1394	1395	1396	1397	1398	1399
2570	1400	1401	1402	1403	1404	1405	1406	1407
2600	1408	1409	1410	1411	1412	1413	1414	1415
2610	1416	1417	1418	1419	1420	1421	1422	1423
2620	1424	1425	1426	1427	1428	1429	1430	1431
2630	1432	1433	1434	1435	1436	1437	1438	1439
2640	1440	1441	1442	1443	1444	1445	1446	1447
2650	1448	1449	1450	1451	1452	1453	1454	1455
2660	1456	1457	1458	1459	1460	1461	1462	1463
2670	1464	1465	1466	1467	1468	1469	1470	1471
2700	1472	1473	1474	1475	1476	1477	1478	1479
2710	1480	1481	1482	1483	1484	1485	1486	1487
2720	1488	1489	1490	1491	1492	1493	1494	1495
2730	1496	1497	1498	1499	1500	1501	1502	1503
2740	1504	1505	1506	1507	1508	1509	1510	1511
2750	1512	1513	1514	1515	1516	1517	1518	1519
2760	1520	1521	1522	1523	1524	1525	1526	1527
2770	1528	1529	1530	1531	1532	1533	1534	1535

2000 to 2777 (Octal)	1024 to 1535 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
3000	1536	1537	1538	1539	1540	1541	1542	1543
3010	1544	1545	1546	1547	1548	1549	1550	1551
3020	1552	1553	1554	1555	1556	1557	1558	1559
3030	1560	1561	1562	1563	1564	1565	1566	1567
3040	1568	1569	1570	1571	1572	1573	1574	1575
3050	1576	1577	1578	1579	1580	1581	1582	1583
3060	1584	1585	1586	1587	1588	1589	1590	1591
3070	1592	1593	1594	1595	1596	1597	1598	1599
3100	1600	1601	1602	1603	1604	1605	1606	1607
3110	1608	1609	1610	1611	1612	1613	1614	1615
3120	1616	1617	1618	1619	1620	1621	1622	1623
3130	1624	1625	1626	1627	1628	1629	1630	1631
3140	1632	1633	1634	1635	1636	1637	1638	1639
3150	1640	1641	1642	1643	1644	1645	1646	1647
3160	1648	1649	1650	1651	1652	1653	1654	1655
3170	1656	1657	1658	1659	1660	1661	1662	1663
3200	1664	1665	1666	1667	1668	1669	1670	1671
3210	1672	1673	1674	1675	1676	1677	1678	1679
3220	1680	1681	1682	1683	1684	1685	1686	1687
3230	1688	1689	1690	1691	1692	1693	1694	1695
3240	1696	1697	1698	1699	1700	1701	1702	1703
3250	1704	1705	1706	1707	1708	1709	1710	1711
3260	1712	1713	1714	1715	1716	1717	1718	1719
3270	1720	1721	1722	1723	1724	1725	1726	1727
3300	1728	1729	1730	1731	1732	1733	1734	1735
3310	1736	1737	1738	1739	1740	1741	1742	1743
3320	1744	1745	1746	1747	1748	1749	1750	1751
3330	1752	1753	1754	1755	1756	1757	1758	1759
3340	1760	1761	1762	1763	1764	1765	1766	1767
3350	1768	1769	1770	1771	1772	1773	1774	1775
3360	1776	1777	1778	1779	1780	1781	1782	1783
3370	1784	1785	1786	1787	1788	1789	1790	1791

	0	1	2	3	4	5	6	7
3400	1792	1793	1794	1795	1796	1797	1798	1799
3410	1800	1801	1802	1803	1804	1805	1806	1807
3420	1808	1809	1810	1811	1812	1813	1814	1815
3430	1816	1817	1818	1819	1820	1821	1822	1823
3440	1824	1825	1826	1827	1828	1829	1830	1831
3450	1832	1833	1834	1835	1836	1837	1838	1839
3460	1840	1841	1842	1843	1844	1845	1846	1847
3470	1848	1849	1850	1851	1852	1853	1854	1855
3500	1856	1857	1858	1859	1860	1861	1862	1863
3510	1864	1865	1866	1867	1868	1869	1870	1871
3520	1872	1873	1874	1875	1876	1877	1878	1879
3530	1880	1881	1882	1883	1884	1885	1886	1887
3540	1888	1889	1890	1891	1892	1893	1894	1895
3550	1896	1897	1898	1899	1900	1901	1902	1903
3560	1904	1905	1906	1907	1908	1909	1910	1911
3570	1912	1913	1914	1915	1916	1917	1918	1919
3600	1920	1921	1922	1923	1924	1925	1926	1927
3610	1928	1929	1930	1931	1932	1933	1934	1935
3620	1936	1937	1938	1939	1940	1941	1942	1943
3630	1944	1945	1946	1947	1948	1949	1950	1951
3640	1952	1953	1954	1955	1956	1957	1958	1959
3650	1960	1961	1962	1963	1964	1965	1966	1967
3660	1968	1969	1970	1971	1972	1973	1974	1975
3670	1976	1977	1978	1979	1980	1981	1982	1983
3700	1984	1985	1986	1987	1988	1989	1990	1991
3710	1992	1993	1994	1995	1996	1997	1998	1999
3720	2000	2001	2002	2003	2004	2005	2006	2007
3730	2008	2009	2010	2011	2012	2013	2014	2015
3740	2016	2017	2018	2019	2020	2021	2022	2023
3750	2024	2025	2026	2027	2028	2029	2030	2031
3760	2032	2033	2034	2035	2036	2037	2038	2039
3770	2040	2041	2042	2043	2044	2045	2046	2047

3000 to 3777 (Octal)	1536 to 2047 (Decimal)

APPENDIX D

OCTAL-DECIMAL INTEGER CONVERSIONS *(continued)*

4000 to 4777 (Octal)	2048 to 2559 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
4000	2048	2049	2050	2051	2052	2053	2054	2055
4010	2056	2057	2058	2059	2060	2061	2062	2063
4020	2064	2065	2066	2067	2068	2069	2070	2071
4030	2072	2073	2074	2075	2076	2077	2078	2079
4040	2080	2081	2082	2083	2084	2085	2086	2087
4050	2088	2089	2090	2091	2092	2093	2094	2095
4060	2096	2097	2098	2099	2100	2101	2102	2103
4070	2104	2105	2106	2107	2108	2109	2110	2111
4100	2112	2113	2114	2115	2116	2117	2118	2119
4110	2120	2121	2122	2123	2124	2125	2126	2127
4120	2128	2129	2130	2131	2132	2133	2134	2135
4130	2136	2137	2138	2139	2140	2141	2142	2143
4140	2144	2145	2146	2147	2148	2149	2150	2151
4150	2152	2153	2154	2155	2156	2157	2158	2159
4160	2160	2161	2162	2163	2164	2165	2166	2167
4170	2168	2169	2170	2171	2172	2173	2174	2175
4200	2176	2177	2178	2179	2180	2181	2182	2183
4210	2184	2185	2186	2187	2188	2189	2190	2191
4220	2192	2193	2194	2195	2196	2197	2198	2199
4230	2200	2201	2202	2203	2204	2205	2206	2207
4240	2208	2209	2210	2211	2212	2213	2214	2215
4250	2216	2217	2218	2219	2220	2221	2222	2223
4260	2224	2225	2226	2227	2228	2229	2230	2231
4270	2232	2233	2234	2235	2236	2237	2238	2239
4300	2240	2241	2242	2243	2244	2245	2246	2247
4310	2248	2249	2250	2251	2252	2253	2254	2255
4320	2256	2257	2258	2259	2260	2261	2262	2263
4330	2264	2265	2266	2267	2268	2269	2270	2271
4340	2272	2273	2274	2275	2276	2277	2278	2279
4350	2280	2281	2282	2283	2284	2285	2286	2287
4360	2288	2289	2290	2291	2292	2293	2294	2295
4370	2296	2297	2298	2299	2300	2301	2302	2303

	0	1	2	3	4	5	6	7
4400	2304	2305	2306	2307	2308	2309	2310	2311
4410	2312	2313	2314	2315	2316	2317	2318	2319
4420	2320	2321	2322	2323	2324	2325	2326	2327
4430	2328	2329	2330	2331	2332	2333	2334	2335
4440	2336	2337	2338	2339	2340	2341	2342	2343
4450	2344	2345	2346	2347	2348	2349	2350	2351
4460	2352	2353	2354	2355	2356	2357	2358	2359
4470	2360	2361	2362	2363	2364	2365	2366	2367
4500	2368	2369	2370	2371	2372	2373	2374	2375
4510	2376	2377	2378	2379	2380	2381	2382	2383
4520	2384	2385	2386	2387	2388	2389	2390	2391
4530	2392	2393	2394	2395	2396	2397	2398	2399
4540	2400	2401	2402	2403	2404	2405	2406	2407
4550	2408	2409	2410	2411	2412	2413	2414	2415
4560	2416	2417	2418	2419	2420	2421	2422	2423
4570	2424	2425	2426	2427	2428	2429	2430	2431
4600	2432	2433	2434	2435	2436	2437	2438	2439
4610	2440	2441	2442	2443	2444	2445	2446	2447
4620	2448	2449	2450	2451	2452	2453	2454	2455
4630	2456	2457	2458	2459	2460	2461	2462	2463
4640	2464	2465	2466	2467	2468	2469	2470	2471
4650	2472	2473	2474	2475	2476	2477	2478	2479
4660	2480	2481	2482	2483	2484	2485	2486	2487
4670	2488	2489	2490	2491	2492	2493	2494	2495
4700	2496	2497	2498	2499	2500	2501	2502	2503
4710	2504	2505	2506	2507	2508	2509	2510	2511
4720	2512	2513	2514	2515	2516	2517	2518	2519
4730	2520	2521	2522	2523	2524	2525	2526	2527
4740	2528	2529	2530	2531	2532	2533	2534	2535
4750	2536	2537	2538	2539	2540	2541	2542	2543
4760	2544	2545	2546	2547	2548	2549	2550	2551
4770	2552	2553	2554	2555	2556	2557	2558	2559

5000 to 5777 Octal)	2560 to 3071 (Decimal)

	0	1	2	3	4	5	6	7
5000	2560	2561	2562	2563	2564	2565	2566	2567
5010	2568	2569	2570	2571	2572	2573	2574	2575
5020	2576	2577	2578	2579	2580	2581	2582	2583
5030	2584	2585	2586	2587	2588	2589	2590	2591
5040	2592	2593	2594	2595	2596	2597	2598	2599
5050	2600	2601	2602	2603	2604	2605	2606	2607
5060	2608	2609	2610	2611	2612	2613	2614	2615
5070	2616	2617	2618	2619	2620	2621	2622	2623
5100	2624	2625	2626	2627	2628	2629	2630	2631
5110	2632	2633	2634	2635	2636	2637	2638	2639
5120	2640	2641	2642	2643	2644	2645	2646	2647
5130	2648	2649	2650	2651	2652	2653	2654	2655
5140	2656	2657	2658	2659	2660	2661	2662	2663
5150	2664	2665	2666	2667	2668	2669	2670	2671
5160	2672	2673	2674	2675	2676	2677	2678	2679
5170	2680	2681	2682	2683	2684	2685	2686	2687
5200	2688	2689	2690	2691	2692	2693	2694	2695
5210	2696	2697	2698	2699	2700	2701	2702	2703
5220	2704	2705	2706	2707	2708	2709	2710	2711
5230	2712	2713	2714	2715	2716	2717	2718	2719
5240	2720	2721	2722	2723	2724	2725	2726	2727
5250	2728	2729	2730	2731	2732	2733	2734	2735
5260	2736	2737	2738	2739	2740	2741	2742	2743
5270	2744	2745	2746	2747	2748	2749	2750	2751
5300	2752	2753	2754	2755	2756	2757	2758	2759
5310	2760	2761	2762	2763	2764	2765	2766	2767
5320	2768	2769	2770	2771	2772	2773	2774	2775
5330	2776	2777	2778	2779	2780	2781	2782	2783
5340	2784	2785	2786	2787	2788	2789	2790	2791
5350	2792	2793	2794	2795	2796	2797	2798	2799
5360	2800	2801	2802	2803	2804	2805	2806	2807
5370	2808	2809	2810	2811	2812	2813	2814	2815

	0	1	2	3	4	5	6	7
5400	2816	2817	2818	2819	2820	2821	2822	2823
5410	2824	2825	2826	2827	2828	2829	2830	2831
5420	2832	2833	2834	2835	2836	2837	2838	2839
5430	2840	2841	2842	2843	2844	2845	2846	2847
5440	2848	2849	2850	2851	2852	2853	2854	2855
5450	2856	2857	2858	2859	2860	2861	2862	2863
5460	2864	2865	2866	2867	2868	2869	2870	2871
5470	2872	2873	2874	2875	2876	2877	2878	2879
5500	2880	2881	2882	2883	2884	2885	2886	2887
5510	2888	2889	2890	2891	2892	2893	2894	2895
5520	2896	2897	2898	2899	2900	2901	2902	2903
5530	2904	2905	2906	2907	2908	2909	2910	2911
5540	2912	2913	2914	2915	2916	2917	2918	2919
5550	2920	2921	2922	2923	2924	2925	2926	2927
5560	2928	2929	2930	2931	2932	2933	2934	2935
5570	2936	2937	2938	2939	2940	2941	2942	2943
5600	2944	2945	2946	2947	2948	2949	2950	2951
5610	2952	2953	2954	2955	2956	2957	2958	2959
5620	2960	2961	2962	2963	2964	2965	2966	2967
5630	2968	2969	2970	2971	2972	2973	2974	2975
5640	2976	2977	2978	2979	2980	2981	2982	2983
5650	2984	2985	2986	2987	2988	2989	2990	2991
5660	2992	2993	2994	2995	2996	2997	2998	2999
5670	3000	3001	3002	3003	3004	3005	3006	3007
5700	3008	3009	3010	3011	3012	3013	3014	3015
5710	3016	3017	3018	3019	3020	3021	3022	3023
5720	3024	3025	3026	3027	3028	3029	3030	3031
5730	3032	3033	3034	3035	3036	3037	3038	3039
5740	3040	3041	3042	3043	3044	3045	3046	3047
5750	3048	3049	3050	3051	3052	3053	3054	3055
5760	3056	3057	3058	3059	3060	3061	3062	3063
5770	3064	3065	3066	3067	3068	3069	3070	3071

APPENDIX D

OCTAL-DECIMAL INTEGER CONVERSIONS *(continued)*

	0	1	2	3	4	5	6	7
6000	3072	3073	3074	3075	3076	3077	3078	3079
6010	3080	3081	3082	3083	3084	3085	3086	3087
6020	3088	3089	3090	3091	3092	3093	3094	3095
6030	3096	3097	3098	3099	3100	3101	3102	3103
6040	3104	3105	3106	3107	3108	3109	3110	3111
6050	3112	3113	3114	3115	3116	3117	3118	3119
6060	3120	3121	3122	3123	3124	3125	3126	3127
6070	3128	3129	3130	3131	3132	3133	3134	3135
6100	3136	3137	3138	3139	3140	3141	3142	3143
6110	3144	3145	3146	3147	3148	3149	3150	3151
6120	3152	3153	3154	3155	3156	3157	3158	3159
6130	3160	3161	3162	3163	3164	3165	3166	3167
6140	3168	3169	3170	3171	3172	3173	3174	3175
6150	3176	3177	3178	3179	3180	3181	3182	3183
6160	3184	3185	3186	3187	3188	3189	3190	3191
6170	3192	3193	3194	3195	3196	3197	3198	3199
6200	3200	3201	3202	3203	3204	3205	3206	3207
6210	3208	3209	3210	3211	3212	3213	3214	3215
6220	3216	3217	3218	3219	3220	3221	3222	3223
6230	3224	3225	3226	3227	3228	3229	3230	3231
6240	3232	3233	3234	3235	3236	3237	3238	3239
6250	3240	3241	3242	3243	3244	3245	3246	3247
6260	3248	3249	3250	3251	3252	3253	3254	3255
6270	3256	3257	3258	3259	3260	3261	3262	3263
6300	3264	3265	3266	3267	3268	3269	3270	3271
6310	3272	3273	3274	3275	3276	3277	3278	3279
6320	3280	3281	3282	3283	3284	3285	3286	3287
6330	3288	3289	3290	3291	3292	3293	3294	3295
6340	3296	3297	3298	3299	3300	3301	3302	3303
6350	3304	3305	3306	3307	3308	3309	3310	3311
6360	3312	3313	3314	3315	3316	3317	3318	3319
6370	3320	3321	3322	3323	3324	3325	3326	3327

	0	1	2	3	4	5	6	7
6400	3328	3329	3330	3331	3332	3333	3334	3335
6410	3336	3337	3338	3339	3340	3341	3342	3343
6420	3344	3345	3346	3347	3348	3349	3350	3351
6430	3352	3353	3354	3355	3356	3357	3358	3359
6440	3360	3361	3362	3363	3364	3365	3366	3367
6450	3368	3369	3370	3371	3372	3373	3374	3375
6460	3376	3377	3378	3379	3380	3381	3382	3383
6470	3384	3385	3386	3387	3388	3389	3390	3391
6500	3392	3393	3394	3395	3396	3397	3398	3399
6510	3400	3401	3402	3403	3404	3405	3406	3407
6520	3408	3409	3410	3411	3412	3413	3414	3415
6530	3416	3417	3418	3419	3420	3421	3422	3423
6540	3424	3425	3426	3427	3428	3429	3430	3431
6550	3432	3433	3434	3435	3436	3437	3438	3439
6560	3440	3441	3442	3443	3444	3445	3446	3447
6570	3448	3449	3450	3451	3452	3453	3454	3455
6600	3456	3457	3458	3459	3460	3461	3462	3463
6610	3464	3465	3466	3467	3468	3469	3470	3471
6620	3472	3473	3474	3475	3476	3477	3478	3479
6630	3480	3481	3482	3483	3484	3485	3486	3487
6640	3488	3489	3490	3491	3492	3493	3494	3495
6650	3496	3497	3498	3499	3500	3501	3502	3503
6660	3504	3505	3506	3507	3508	3509	3510	3511
6670	3512	3513	3514	3515	3516	3517	3518	3519
6700	3520	3521	3522	3523	3524	3525	3526	3527
6710	3528	3529	3530	3531	3532	3533	3534	3535
6720	3536	3537	3538	3539	3540	3541	3542	3543
6730	3544	3545	3546	3547	3548	3549	3550	3551
6740	3552	3553	3554	3555	3556	3557	3558	3559
6750	3560	3561	3562	3563	3564	3565	3566	3567
6760	3568	3569	3570	3571	3572	3573	3574	3575
6770	3576	3577	3578	3579	3580	3581	3582	3583

6000	3072
to	to
6777	3583
(Octal)	(Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
7000	3584	3585	3586	3587	3588	3589	3590	3591
7010	3592	3593	3594	3595	3596	3597	3598	3599
7020	3600	3601	3602	3603	3604	3605	3606	3607
7030	3608	3609	3610	3611	3612	3613	3614	3615
7040	3616	3617	3618	3619	3620	3621	3622	3623
7050	3624	3625	3626	3627	3628	3629	3630	3631
7060	3632	3633	3634	3635	3636	3637	3638	3639
7070	3640	3641	3642	3643	3644	3645	3646	3647
7100	3648	3649	3650	3651	3652	3653	3654	3655
7110	3656	3657	3658	3659	3660	3661	3662	3663
7120	3664	3665	3666	3667	3668	3669	3670	3671
7130	3672	3673	3674	3675	3676	3677	3678	3679
7140	3680	3681	3682	3683	3684	3685	3686	3687
7150	3688	3689	3690	3691	3692	3693	3694	3695
7160	3696	3697	3698	3699	3700	3701	3702	3703
7170	3704	3705	3706	3707	3708	3709	3710	3711
7200	3712	3713	3714	3715	3716	3717	3718	3719
7210	3720	3721	3722	3723	3724	3725	3726	3727
7220	3728	3729	3730	3731	3732	3733	3734	3735
7230	3736	3737	3738	3739	3740	3741	3742	3743
7240	3744	3745	3746	3747	3748	3749	3750	3751
7250	3752	3753	3754	3755	3756	3757	3758	3759
7260	3760	3761	3762	3763	3764	3765	3766	3767
7270	3768	3769	3770	3771	3772	3773	3774	3775
7300	3776	3777	3778	3779	3780	3781	3782	3783
7310	3784	3785	3786	3787	3788	3789	3790	3791
7320	3792	3793	3794	3795	3796	3797	3798	3799
7330	3800	3801	3802	3803	3804	3805	3806	3807
7340	3808	3809	3810	3811	3812	3813	3814	3815
7350	3816	3817	3818	3819	3820	3821	3822	3823
7360	3824	3825	3826	3827	3828	3829	3830	3831
7370	3832	3833	3834	3835	3836	3837	3838	3839

	0	1	2	3	4	5	6	7
7400	3840	3841	3842	3843	3844	3845	3846	3847
7410	3848	3849	3850	3851	3852	3853	3854	3855
7420	3856	3857	3858	3859	3860	3861	3862	3863
7430	3864	3865	3866	3867	3868	3869	3870	3871
7440	3872	3873	3874	3875	3876	3877	3878	3879
7450	3880	3881	3882	3883	3884	3885	3886	3887
7460	3888	3889	3890	3891	3892	3893	3894	3895
7470	3896	3897	3898	3899	3900	3901	3902	3903
7500	3904	3905	3906	3907	3908	3909	3910	3911
7510	3912	3913	3914	3915	3916	3917	3918	3919
7520	3920	3921	3922	3923	3924	3925	3926	3927
7530	3928	3929	3930	3931	3932	3933	3934	3935
7540	3936	3937	3938	3939	3940	3941	3942	3943
7550	3944	3945	3946	3947	3948	3949	3950	3951
7560	3952	3953	3954	3955	3956	3957	3958	3959
7570	3960	3961	3962	3963	3964	3965	3966	3967
7600	3968	3969	3970	3971	3972	3973	3974	3975
7610	3976	3977	3978	3979	3980	3981	3982	3983
7620	3984	3985	3986	3987	3988	3989	3990	3991
7630	3992	3993	3994	3995	3996	3997	3998	3999
7640	4000	4001	4002	4003	4004	4005	4006	4007
7650	4008	4009	4010	4011	4012	4013	4014	4015
7660	4016	4017	4018	4019	4020	4021	4022	4023
7670	4024	4025	4026	4027	4028	4029	4030	4031
7700	4032	4033	4034	4035	4036	4037	4038	4039
7710	4040	4041	4042	4043	4044	4045	4046	4047
7720	4048	4049	4050	4051	4052	4053	4054	4055
7730	4056	4057	4058	4059	4060	4061	4062	4063
7740	4064	4065	4066	4067	4068	4069	4070	4071
7750	4072	4073	4074	4075	4076	4077	4078	4079
7760	4080	4081	4082	4083	4084	4085	4086	4087
7770	4088	4089	4090	4091	4092	4093	4094	4095

7000	3584
to	to
7777	4095
(Octal)	(Decimal)

APPENDIX E

OCTAL-DECIMAL FRACTION CONVERSIONS

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000	.000000	.100	.125000	.200	.250000	.300	.375000
.001	.001953	.101	.126953	.201	.251953	.301	.376953
.002	.003906	.102	.128906	.202	.253906	.302	.378906
.003	.005859	.103	.130859	.203	.255859	.303	.380859
.004	.007812	.104	.132812	.204	.257812	.304	.382812
.005	.009765	.105	.134765	.205	.259765	.305	.384765
.006	.011718	.106	.136718	.206	.261718	.306	.386718
.007	.013671	.107	.138671	.207	.263671	.307	.388671
.010	.015625	.110	.140625	.210	.265625	.310	.390625
.011	.017578	.111	.142578	.211	.267578	.311	.392578
.012	.019531	.112	.144531	.212	.269531	.312	.394531
.013	.021484	.113	.146484	.213	.271484	.313	.396484
.014	.023437	.114	.148437	.214	.273437	.314	.398437
.015	.025390	.115	.150390	.215	.275390	.315	.400390
.016	.027343	.116	.152343	.216	.277343	.316	.402343
.017	.029296	.117	.154296	.217	.279296	.317	.404296
.020	.031250	.120	.156250	.220	.281250	.320	.406250
.021	.033203	.121	.158203	.221	.283203	.321	.408203
.022	.035156	.122	.160156	.222	.285156	.322	.410156
.023	.037109	.123	.162109	.223	.287109	.323	.412109
.024	.039062	.124	.164062	.224	.289062	.324	.414062
.025	.041015	.125	.166015	.225	.291015	.325	.416015
.026	.042968	.126	.167968	.226	.292968	.326	.417968
.027	.044921	.127	.169921	.227	.294921	.327	.419921
.030	.046875	.130	.171875	.230	.296875	.330	.421875
.031	.048828	.131	.173828	.231	.298828	.331	.423828
.032	.050781	.132	.175781	.232	.300781	.332	.426781
.033	.052734	.133	.177734	.233	.302734	.333	.427734
.034	.054687	.134	.179687	.234	.304687	.334	.429687
.035	.056640	.135	.181640	.235	.306640	.335	.431640
.036	.058593	.136	.183593	.236	.308593	.336	.433593
.037	.060546	.137	.185546	.237	.310546	.337	.435546
.040	.062500	.140	.187500	.240	.312500	.340	.437500
.041	.064453	.141	.189453	.241	.314453	.341	.439453
.042	.066406	.142	.191406	.242	.316406	.342	.441406
.043	.068359	.143	.193359	.243	.318359	.343	.443359
.044	.070312	.144	.195312	.244	.320312	.344	.445312
.045	.072265	.145	.197265	.245	.322265	.345	.447265
.046	.074218	.146	.199218	.246	.324218	.346	.449218
.047	.076171	.147	.201171	.247	.326171	.347	.451171
.050	.078125	.150	.203125	.250	.328125	.350	.453125
.051	.080078	.151	.205078	.251	.330078	.351	.455078
.052	.082031	.152	.207031	.252	.332031	.352	.457031
.053	.083984	.153	.208984	.253	.333984	.353	.458984
.054	.085937	.154	.210937	.254	.335937	.354	.460937
.055	.087890	.155	.212890	.255	.337890	.355	.462890
.056	.089843	.156	.214843	.256	.339843	.356	.464843
.057	.091796	.157	.216796	.257	.341796	.357	.466796
.060	.093750	.160	.218750	.260	.343750	.360	.468750
.061	.095703	.161	.220703	.261	.345703	.361	.470703
.062	.097656	.162	.222656	.262	.347656	.362	.472656
.063	.099609	.163	.224609	.263	.349609	.363	.474609
.064	.101562	.164	.226562	.264	.351562	.364	.476562
.065	.103515	.165	.228515	.265	.353515	.365	.478515
.066	.105468	.166	.230468	.266	.355468	.366	.480468
.067	.107421	.167	.232421	.267	.357421	.367	.482421
.070	.109375	.170	.234375	.270	.359375	.370	.484375
.071	.111328	.171	.236328	.271	.361328	.371	.486328
.072	.113281	.172	.238281	.272	.363281	.372	.488281
.073	.115234	.173	.240234	.273	.365234	.373	.490234
.074	.117187	.174	.242187	.274	.367187	.374	.492187
.075	.119140	.175	.244140	.275	.369140	.375	.494140
.076	.121093	.176	.246093	.276	.371093	.376	.496093
.077	.123046	.177	.248046	.277	.373046	.377	.498046

APPENDIX E

OCTAL-DECIMAL FRACTION CONVERSIONS *(continued)*

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000000	.000000	.000100	.000244	.000200	.000488	.000300	.000732
.000001	.000003	.000101	.000247	.000201	.000492	.000301	.000736
.000002	.000007	.000102	.000251	.000202	.000495	.000302	.000740
.000003	.000011	.000103	.000255	.000203	.000499	.000303	.000743
.000004	.000015	.000104	.000259	.000204	.000503	.000304	.000747
.000005	.000019	.000105	.000263	.000205	.000507	.000305	.000751
.000006	.000022	.000106	.000267	.000206	.000511	.000306	.000755
.000007	.000026	.000107	.000270	.000207	.000514	.000307	.000759
.000010	.000030	.000110	.000274	.000210	.000518	.000310	.000762
.000011	.000034	.000111	.000278	.000211	.000522	.000311	.000766
.000012	.000038	.000112	.000282	.000212	.000526	.000312	.000770
.000013	.000041	.000113	.000286	.000213	.000530	.000313	.000774
.000014	.000045	.000114	.000289	.000214	.000534	.000314	.000778
.000015	.000049	.000115	.000293	.000215	.000537	.000315	.000782
.000016	.000053	.000116	.000297	.000216	.000541	.000316	.000785
.000017	.000057	.000117	.000301	.000217	.000545	.000317	.000789
.000020	.000061	.000120	.000305	.000220	.000549	.000320	.000793
.000021	.000064	.000121	.000308	.000221	.000553	.000321	.000797
.000022	.000068	.000122	.000312	.000222	.000556	.000322	.000801
.000023	.000072	.000123	.000316	.000223	.000560	.000323	.000805
.000024	.000076	.000124	.000320	.000224	.000564	.000324	.000808
.000025	.000080	.000125	.000324	.000225	.000568	.000325	.000812
.000026	.000083	.000126	.000328	.000226	.000572	.000326	.000816
.000027	.000087	.000127	.000331	.000227	.000576	.000327	.000820
.000030	.000091	.000130	.000335	.000230	.000579	.000330	.000823
.000031	.000095	.000131	.000339	.000231	.000583	.000331	.000827
.000032	.000099	.000132	.000343	.000232	.000587	.000332	.000831
.000033	.000102	.000133	.000347	.000233	.000591	.000333	.000835
.000034	.000106	.000134	.000350	.000234	.000595	.000334	.000839
.000035	.000110	.000135	.000354	.000235	.000598	.000335	.000843
.000036	.000114	.000136	.000358	.000236	.000602	.000336	.000846
.000037	.000118	.000137	.000362	.000237	.000606	.000337	.000850
.000040	.000122	.000140	.000366	.000240	.000610	.000340	.000854
.000041	.000125	.000141	.000370	.000241	.000614	.000341	.000858
.000042	.000129	.000142	.000373	.000242	.000617	.000342	.000862
.000043	.000133	.000143	.000377	.000243	.000621	.000343	.000865
.000044	.000137	.000144	.000381	.000244	.000625	.000344	.000869
.000045	.000141	.000145	.000385	.000245	.000629	.000345	.000873
.000046	.000144	.000146	.000389	.000246	.000633	.000346	.000877
.000047	.000148	.000147	.000392	.000247	.000637	.000347	.000881
.000050	.000152	.000150	.000396	.000250	.000640	.000350	.000885
.000051	.000156	.000151	.000400	.000251	.000644	.000351	.000888
.000052	.000160	.000152	.000404	.000252	.000648	.000352	.000892
.000053	.000164	.000153	.000408	.000253	.000652	.000353	.000896
.000054	.000167	.000154	.000411	.000254	.000656	.000354	.000900
.000055	.000171	.000155	.000415	.000255	.000659	.000355	.000904
.000056	.000175	.000156	.000419	.000256	.000663	.000356	.000907
.000057	.000179	.000157	.000423	.000257	.000667	.000357	.000911
.000060	.000183	.000160	.000427	.000260	.000671	.000360	.000915
.000061	.000186	.000161	.000431	.000261	.000675	.000361	.000919
.000062	.000190	.000162	.000434	.000262	.000679	.000362	.000923
.000063	.000194	.000163	.000438	.000263	.000682	.000363	.000926
.000064	.000198	.000164	.000442	.000264	.000686	.000364	.000930
.000065	.000202	.000165	.000446	.000265	.000690	.000365	.000934
.000066	.000205	.000166	.000450	.000266	.000694	.000366	.000938
.000067	.000209	.000167	.000453	.000267	.000698	.000367	.000942
.000070	.000213	.000170	.000457	.000270	.000701	.000370	.000946
.000071	.000217	.000171	.000461	.000271	.000705	.000371	.000949
.000072	.000221	.000172	.000465	.000272	.000709	.000372	.000953
.000073	.000225	.000173	.000469	.000273	.000713	.000373	.000957
.000074	.000228	.000174	.000473	.000274	.000717	.000374	.000961
.000075	.000232	.000175	.000476	.000275	.000720	.000375	.000965
.000076	.000236	.000176	.000480	.000276	.000724	.000376	.000968
.000077	.000240	.000177	.000484	.000277	.000728	.000377	.000972

APPENDIX E

OCTAL-DECIMAL FRACTION CONVERSIONS *(continued)*

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000400	.000976	.000500	.001220	.000600	.001464	.000700	.001708
.000401	.000980	.000501	.001224	.000601	.001468	.000701	.001712
.000402	.000984	.000502	.001228	.000602	.001472	.000702	.001716
.000403	.000988	.000503	.001232	.000603	.001476	.000703	.001720
.000404	.000991	.000504	.001235	.000604	.001480	.000704	.001724
.000405	.000995	.000505	.001239	.000605	.001483	.000705	.001728
.000406	.000999	.000506	.001243	.000606	.001487	.000706	.001731
.000407	.001003	.000507	.001247	.000607	.001491	.000707	.001735
.000410	.001007	.000510	.001251	.000610	.001495	.000710	.001739
.000411	.001010	.000511	.001255	.000611	.001499	.000711	.001743
.000412	.001014	.000512	.001258	.000612	.001502	.000712	.001747
.000413	.001018	.000513	.001262	.000613	.001506	.000713	.001750
.000414	.001022	.000514	.001266	.000614	.001510	.000714	.001754
.000415	.001026	.000515	.001270	.000615	.001514	.000715	.001758
.000416	.001029	.000516	.001274	.000616	.001518	.000716	.001762
.000417	.001033	.000517	.001277	.000617	.001522	.000717	.001766
.000420	.001037	.000520	.001281	.000620	.001525	.000720	.001770
.000421	.001041	.000521	.001285	.000621	.001529	.000721	.001773
.000422	.001045	.000522	.001289	.000622	.001533	.000722	.001777
.000423	.001049	.000523	.001293	.000623	.001537	.000723	.001781
.000424	.001052	.000524	.001296	.000624	.001541	.000724	.001785
.000425	.001056	.000525	.001300	.000625	.001544	.000725	.001789
.000426	.001060	.000526	.001304	.000626	.001548	.000726	.001792
.000427	.001064	.000527	.001308	.000627	.001552	.000727	.001796
.000430	.001068	.000530	.001312	.000630	.001556	.000730	.001800
.000431	.001071	.000531	.001316	.000631	.001560	.000731	.001804
.000432	.001075	.000532	.001319	.000632	.001564	.000732	.001808
.000433	.001079	.000533	.001323	.000633	.001567	.000733	.001811
.000434	.001083	.000534	.001327	.000634	.001571	.000734	.001815
.000435	.001087	.000535	.001331	.000635	.001575	.000735	.001819
.000436	.001091	.000536	.001335	.000636	.001579	.000736	.001823
.000437	.001094	.000537	.001338	.000637	.001583	.000737	.001827
.000440	.001098	.000540	.001342	.000640	.001586	.000740	.001831
.000441	.001102	.000541	.001346	.000641	.001590	.000741	.001834
.000442	.001106	.000542	.001350	.000642	.001594	.000742	.001838
.000443	.001110	.000543	.001354	.000643	.001598	.000743	.001842
.000444	.001113	.000544	.001358	.000644	.001602	.000744	.001846
.000445	.001117	.000545	.001361	.000645	.001605	.000745	.001850
.000446	.001121	.000546	.001365	.000646	.001609	.000746	.001853
.000447	.001125	.000547	.001369	.000647	.001613	.000747	.001857
.000450	.001129	.000550	.001373	.000650	.001617	.000750	.001861
.000451	.001132	.000551	.001377	.000651	.001621	.000751	.001865
.000452	.001136	.000552	.001380	.000652	.001625	.000752	.001869
.000453	.001140	.000553	.001384	.000653	.001628	.000753	.001873
.000454	.001144	.000554	.001388	.000654	.001632	.000754	.001876
.000455	.001148	.000555	.001392	.000655	.001636	.000755	.001880
.000456	.001152	.000556	.001396	.000656	.001640	.000756	.001884
.000457	.001155	.000557	.001399	.000657	.001644	.000757	.001888
.000460	.001159	.000560	.001403	.000660	.001647	.000760	.001892
.000461	.001163	.000561	.001407	.000661	.001651	.000761	.001895
.000462	.001167	.000562	.001411	.000662	.001655	.000762	.001899
.000463	.001171	.000563	.001415	.000663	.001659	.000763	.001903
.000464	.001174	.000564	.001419	.000664	.001663	.000764	.001907
.000465	.001178	.000565	.001422	.000665	.001667	.000765	.001911
.000466	.001182	.000566	.001426	.000666	.001670	.000766	.001914
.000467	.001186	.000567	.001430	.000667	.001674	.000767	.001918
.000470	.001190	.000570	.001434	.000670	.001678	.000770	.001922
.000471	.001194	.000571	.001438	.000671	.001682	.000771	.001926
.000472	.001197	.000572	.001441	.000672	.001686	.000772	.001930
.000473	.001201	.000573	.001445	.000673	.001689	.000773	.001934
.000474	.001205	.000574	.001449	.000674	.001693	.000774	.001937
.000475	.001209	.000575	.001453	.000675	.001697	.000775	.001941
.000476	.001213	.000576	.001457	.000676	.001701	.000776	.001945
.000477	.001216	.000577	.001461	.000677	.001705	.000777	.001949

APPENDIX F

STANDARD CHARACTER CODES

Symbol	ASCII	Printer	Mag Tape	Hollerith	FORTRAN
@	300	00	32	0-2-8	77
A	301	01	61	12-1	13
B	302	02	62	12-2	14
C	303	03	63	12-3	15
D	304	04	64	12-4	16
E	305	05	65	12-5	17
F	306	06	66	12-6	20
G	307	07	67	12-7	21
H	310	10	70	12-8	22
I	311	11	71	12-9	23
J	312	12	41	11-1	24
K	313	13	42	11-2	25
L	314	14	43	11-3	26
M	315	15	44	11-4	27
N	316	16	45	11-5	30
O	317	17	46	11-6	31
P	320	20	47	11-7	32
Q	321	21	50	11-8	33
R	322	22	51	11-9	34
S	323	23	22	0-2	35
T	324	24	23	0-3	36
U	325	25	24	0-4	37
V	326	26	25	0-5	40
W	327	27	26	0-6	41

APPENDIX F

STANDARD CHARACTER CODES *(continued)*

Symbol	ASCII	Printer	Mag Tape	Hollerith	FORTRAN
X	330	30	27	0-7	42
Y	331	31	30	0-8	43
Z	332	32	31	0-9	44
[	333	33	75	12-5-8	76*
\	334	34	36	0-6-8	76*
]	335	35	55	11-5-8	76*
↑	336	36	17 (Note)	7-8	76*
←	337	37	20	2-8	75[1]
blank	240	40	20	No Punch	00
!	241	41	52	11-2-8	51
"	242	42	35	0-5-8	62
#	243	43	37	0-7-8	63
$	244	44	53	11-3-8	60
%	245	45	57	11-7-8	64
&	246	46	77	12-7-8	65
'	247	47	14	4-8	66
(	250	50	34	0-4-8	52
)	251	51	74	12-4-8	53
*	252	52	54	11-4-8	47
+	253	53	60	12	45
,	254	54	33	0-3-8	54
-	255	55	40	11	46
.	256	56	73	12-3-8	51
/	257	57	21	0-1	50

APPENDIX F

STANDARD CHARACTER CODES *(continued)*

Symbol	ASCII	Printer	Mag Tape	Hollerith	FORTRAN
0	260	60	12	0	01
1	261	61	01	1	02
2	262	62	02	2	03
3	263	63	03	3	04
4	264	64	04	4	05
5	265	65	05	5	06
6	266	66	06	6	07
7	267	67	07	7	10
8	270	70	10	8	11
9	271	71	11	9	12
:	272	72	15	5-8	67
;	273	73	56	11-6-8	70
<	274	74	76	12-6-8	76*
=	275	75	13	3-8	55
>	276	76	16	6-8	76^2
?	277	77	72	12-2-8	76

Note: End-of-file for mag tape.
*: Undefined character.
1: Form control: Return to col 1.
2: Tab control: Skip to col 7.

} FORTRAN System only

APPENDIX G

TELETYPEWRITER CHARACTER CODES

Teletype Character	DATA 620/i Internal Code	Teletype Character	DATA 620/i Internal Code
0	260	Y	331
1	261	Z	332
2	262	blank	240
3	263	!	241
4	264	'	242
5	265	#	243
6	266	$	244
7	267	%	245
8	270	&	246
9	271	'	247
A	301	(	250
B	302	)	251
C	303	*	252
D	304	+	253
E	305	,	254
F	306	—	255
G	307	.	256
H	310	/	257
I	311	:	272
J	312	;	273
K	313		274
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V	326	NUL	200
W	327	SOM	201
X	330	EOA	202

APPENDIX G

TELETYPEWRITER CHARACTER CODES *(continued)*

Teletype Character	DATA 620/i Internal Code	Teletype Character	DATA 620/i Internal Code
EOM	203	X-OFF	223
EOT	204	TAPE OFF	
WRU	205	AUX	224
RU	206	ERROR	225
BEL	207	SYNC	226
FE	210	LEM	227
H TAB	211	SO	230
LINE FEED	212	S1	231
V TAB	213	S2	232
FORM	214	S3	233
RETURN	215	S4	234
SO	216	S5	235
SI	217	S6	236
DCO	220	S7	237
X-ON	221		
TAPE AUX ON	222		

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