The

144-A SERIES

CORE

BUFFER

MEMORIES

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TELEMETER MAGNETICS, INC.
2245 Pontius Avenue, Los Angeles 64, California

THE

144-BQ-8A, 144-BQ-4A, 144-BA-8A

and

144-BA-4A

CORE BUFFER MEMORIES

TELEMETER MAGNETICS, INC.
2245 Pontius Avenue
Los Angeles 64, California

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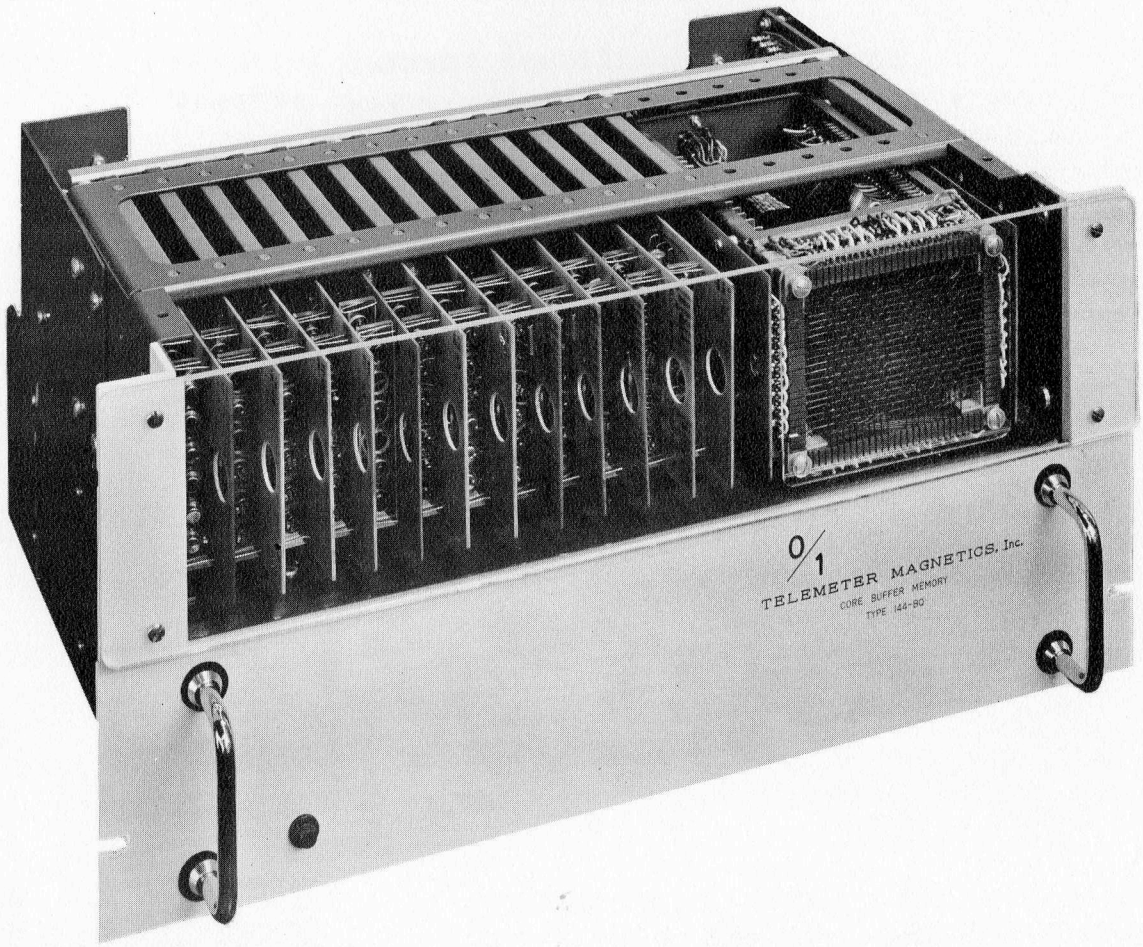


Figure 1-1. 144-A Core Buffer Memory

SECTION I

GENERAL DESCRIPTION

1-1. INTRODUCTION.

1-2. SCOPE. This manual contains information necessary for installation, operation and maintenance of the core buffer memories which comprise the 144-A series. The 144-A series contains the following buffers: 144-BA-4A, 144-BA-8A, 144-BQ-4A and 144-BQ-8A.

1-3. MODEL DESIGNATIONS. The model designation explains the storage capcity, character-bit length and operating mode of the particular buffer as follows:

Character Capacity		Operating Mode		Character Length (bits)
144	-	BA	-	4
144	-	BA	-	8
144	-	BQ	-	4
144	-	BQ	-	8

1-4. The designation BQ indicates that loading and unloading of characters may be interlaced in any sequence, as long as the 144 character capacity is not exceeded. Clearing of the BQ models is required only at the start of operations.

1-5. The designation BA indicates the following:

(a) Addressing circuits must be cleared after a load operation, prior to the unloading of information.

(b) Address and storage circuits must be cleared after an unload operation prior to the loading of additional information.

1-6. PURPOSE AND BASIC PRINCIPLES.

1-7. PURPOSE. The purpose of the buffers is to accomodate differences in rates of information flow in data handling systems. Digital information is loaded into a buffer at a time and rate convenient to one data system component and unloaded at a time and rate convenient to another. One or more buffers may be operated in parallel to obtain character lengths in excess of eight bits.

1-8. The buffers are used between non-synchronized components in data processing, computing, automatic machine control instrumentation and on-line data handling systems.

1-9. BASIC PRINCIPLES. The buffers are coincident-current ferrite core storage systems driven by magnetic stepping switches through logical control circuits in response to externally applied synchronization pulses. These pulses time the coincident currents which determine the state of the bi-stable ferrite cores and regulate the flow of digital information through the buffer. A load pulse causes information on the parallel input lines to be stored in the system. An unload pulse produces one character on the parallel output lines. Each operation takes 10 microseconds.

1-10. The load control circuits consist of blocking oscillators, flip-flops and delay circuits used to write information into the storage system by determining the state of storage cores selected by the switches. Similar unload circuitry reads the state of each core and gates the information out of the system through read amplifiers. Information in the form of d-c levels on the input (load or write) lines may be regulated into the buffer at a rate as high as 100 kc. Positive pulses are produced at the buffer output lines. These pulses may be ONEs or ZEROs depending on the coding.

1-11. COMPONENTS.

1-12. GENERAL. (See Figure 1-1). The buffer is a compact unit consisting of the storage system and magnetic stepping switches (top right), printed circuit cards (right to left) and the power supply (bottom section) shown in Figure 1-1. The entirely transistorized buffer is 8-3/4 inches high, 14 inches deep and fits into a standard 19 inch relay rack. Mechanical retainers are provided on all external plugs and sockets. Table 1-1 lists all components and gives the TMI part number for each.

TABLE 1-1. COMPONENTS.

Component	Abbreviation (Figure 6-1)	TMI Part Number	Number Per Buffer	
			BA	BQ
Input Sync Amplifier		10780	1	1
Two Phase Driver	2ØD	10605	1	2
34-Way Magnetic Switch	MS-34	10620	1	2
Positive Current Stabilizer	PCS	10793	1	1
Digit Driver	DD-G	10787	1 in BA-4 2 in BA-8	1 in BQ-4 2 in BQ-8
Read Amplifier	RA-J	10803	1 in BA-4 2 in BA-8	1 in BQ-4 2 in BQ-8
Strobe Generator		10960	1	1
Electronic Clear		10785	1	1
Coincident Current Detector (optional)	CD-B	10782	1	1
Dummy Board		P-10816	1	0
Magnetic Assembly (includes MS-34)		10679 (BA) 10621 (BQ)	1	1
Power Supply	PS	10904	1	1

1-13. **INPUT SYNC AMPLIFIER.** The input sync amplifier printed circuit card accepts load and unload sync pulses from the external equipment and produces pulses which control the load two phase driver, the unload two phase driver, the digit drivers and the strobe generator circuits.

1-14. TWO PHASE DRIVER. The 144-BA buffers contain one two phase driver and the 144-BQ buffers contain two of them. In each case, the two phase driver is used to advance a magnetic stepping switch. Delayed sync pulses from the input sync amplifier are fed to the two phase driver. Successive sync pulses at the sync input of the driver result in alternate current pulses at driver output lines. The alternate current pulses cause the magnetic switch to select successive storage cores within the storage matrix in a predetermined sequence.

1-15. MAGNETIC STEPPING SWITCH. The 144-BA buffers contain one 34-way magnetic stepping switch and the 144-BQ buffers contain two. Current pulses from the two phase driver advance the magnetic switch so that it selects predetermined storage cores within the storage matrix in a predetermined sequence. In 144-BQ buffers, one magnetic switch is used when information is loaded into the buffer and the second magnetic switch is used when information is unloaded from the buffer. The 144-BA buffers employ one magnetic switch for both load and unload operations.

1-16. STORAGE SYSTEM. The storage system (matrix) contains the ferrite storage cores which store the digital information bits. The cores are arranged on rectangular matrix frames. Each frame contains 288 storage cores which constitute two matrix planes. The 144-BA-4 and 144-BQ-4 buffers contain four matrix planes. These buffers each have a storage capacity of 572 information bits (4 x 144). The 144-BA-8 and 144-BQ-8 buffers contain eight matrix planes. These buffers each have a storage capacity of 1152 information bits (8 x 144).

1-17. Each time that the magnetic switch is stepped (paragraph 1-15), one core in each matrix plane is selected. In the 144-BA-4 and 144-BQ-4 buffers the magnetic switch selects four cores at a time (four planes). In the 144-BA-8 and 144-BQ-8 buffers the magnetic switch selects eight cores at a time (eight planes). Each group of four or eight cores is called an address. There are 144 addresses in each buffer and each address corresponds to a particular setting of the magnetic switch.

1-18. POSITIVE CURRENT STABILIZER. The positive current stabilizer is connected between the power supply and the two phase drivers. It stabilizes current which is steered by the magnetic switches through the storage system. Current flows from the positive current stabilizer, through the two phase driver, the magnetic switch, and the storage system to ground.

1-19. DIGIT DRIVER. The purpose of the digit driver is twofold:

(a) It prevents current flow through the inhibit winding of a matrix plane so that the magnetic state of a storage core may be switched by drive currents from the magnetic switch. It does this by presenting a high impedance to the inhibit current source at the proper time.

(b) It permits current flow through the inhibit winding of a matrix plane to prevent a core from being switched. It does this by presenting a low impedance to the inhibit current source at the proper time.

1-20. The timing of the digit driver currents is controlled by gating levels from the input sync amplifier. Each digit driver printed circuit card contains four information inputs, four gate inputs and four outputs.

1-21. READ AMPLIFIER. The read amplifier receives a signal pulse from the storage system during the time that information is being unloaded from the buffer. At this time the read amplifier is enabled by a strobe pulse from the strobe generator. The strobe pulse permits the read amplifier to produce information bits at the output lines of the buffer only at the proper time. Each read amplifier printed circuit card contains four read amplifier circuits. Each amplifier circuit contains an information input, a strobe input and an information output.

1-22. STROBE GENERATOR. The strobe generator receives a pulse from the input sync amplifier whenever the ferrite core switching currents flow in the matrix. Gating levels from the input sync amplifier control the operation of the strobe generator so that it produces a load strobe output pulse during each load operation and an unload strobe output pulse during each unload operation. The load strobe pulse is used to gate the load coincident current detector. The unload strobe pulse gates the unload coincident current detector and the read amplifiers.

1-23. COINCIDENT CURRENT DETECTOR. The coincident current detector printed circuit card is optional equipment. Its purpose is to produce a marker output pulse in synchronization with the loading or unloading of a character at predetermined addresses. The printed circuit card contains two detector circuits. These two circuits may be connected to the magnetics assemblies of the buffer so as to produce any of the following marker outputs:

(a) One load marker and one unload marker.

(b) Two load markers.

(c) Two unload markers.

(d) One load marker may be obtained when one detector circuit is unused.

(e) One unload marker may be obtained when one detector circuit is unused.

1-24. The load or unload markers may be synchronized with any of the 144 addresses. Wiring between the coincident current detector and the storage circuits is performed at the factory in accordance with the requirements of the user.

1-25. POWER SUPPLY. The power supply operates on 115 volts, 60 cps and delivers d-c operating voltages to all circuits of the buffer. The input a-c voltage is regulated within the power supply. In addition, several of the output voltages are regulated. Several output adjustment controls are located at the rear of the power supply.

1-26. REFERENCE DATA.

Dimensions	19 x 8-3/4 x 14 inches
Weight	38 pounds
Operating Power.	115 $\pm$15 volts, 48 to 62 cps at 2 amperes
Environmental Limits	0^{o} to 70^{o} C. (continuous operation).

Information Signal Polarity	The buffer can operate so that either the positive level or the negative level of the information signal represents a binary ONE.
Input Information Levels	Between -12 and +12 volts. Swing from ZERO to ONE may be from 3 to 10 volts in amplitude.
Input Information Timing	The information level must reach the 50% level of its voltage swing within 1.0 microsecond after zero time.
Zero Time.	Zero time is defined as the time when a load or unload sync pulse crosses the reference level.
Information Level Duration	Information level must remain settled for 9 us after zero time during a load cycle.

Note

The buffer is wired at the factory to utilize the information levels specified by the user. It is adjusted at the factory to accomodate the information voltage swing specified by the user.

Character Capacity	144 characters
Character Length	
144-BA-4 and 144-BQ-4 . . .	four bits
144-BA-8 and 144-BQ-8 . . .	eight bits

Operating Mode

144-BA Buffers	Continuous loading of any number of characters up to 144. Continuous unloading of characters. Address clearing required after loading. Master clearing (address and storage) required prior to reloading.
144-BQ Buffers	Characters may be loaded or unloaded continuously in any interlaced pattern. Address and storage circuits must be cleared at the start of operations.
Cycle Time	10 microseconds
Rate of Operation	100 kc maximum

Sync Pulse Requirements

Polarity	either positive or negative
Pulse Amplitude	3 to 10 volts
Peak Limits	-12 and +12 volts
Leading Edge	0.1 to 0.7 us (10% to 90%)
Duration.	1.0 to 3.0 us between points of 90% amplitude
Trailing Edge	0.1 to 3.0 us (90% to 10%)

Clear Pulse Requirements . . . . . Same as for sync pulses

Settling Intervals Required (leading edge to leading edge)

From	To	Interval
Sync Pulse	Clear Pulse	10 us
Switch Clear Pulse	Sync Pulse	20 us
Master Clear Pulse	Sync Pulse	10 us
Switch Clear Pulse	Clear Pulse	100 us
Master Clear Pulse	Clear Pulse	200 us

NOTE

The buffer is wired at the factory to accomodate the sync and clear pulse levels specified by the user.

Input Capacitance . . . . . 0.001 microfarad max.

Output Pulse Characteristics

Polarity . . . . . positive

Amplitude . . . . . 10.0 $\pm$1.0 volts

Reference Level . . . . . -5.0 $\pm$ 0.5 volts

Rise Time . . . . . 1.0 us maximum

Duration . . . . . 0.5 to 1.5 us between points of 90% amplitude

Fall Time . . . . . 3.0 us maximum

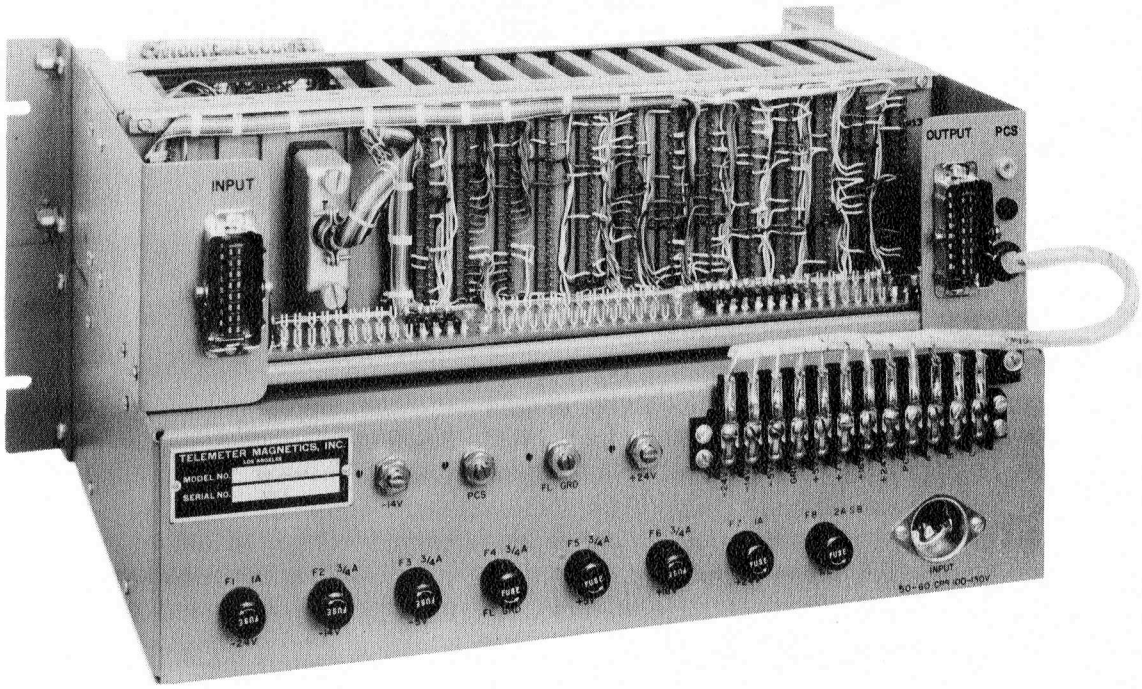


Figure 1-2. Type 144-A Core Buffer Memory, Rear View.

SECTION II

INSTALLATION

2-1. GENERAL.

2-2. This section contains instructions for installing the buffers.

2-3. UNPACKING.

2-4. EQUIPMENT SUPPLIED. Each shipping crate contains two Amphenol Blue Ribbon connectors in addition to the buffer.

2-5. REMOVAL FROM SHIPPING CRATE. Each buffer is shipped in a wooden box and the box strapped with metal bands. During shipment, the buffer is protected by rubberized hair and fiberboard packing materials. The packing materials should be saved for future shipment of the buffer.

2-6. Use cutters to remove the metal bands from the crate. Pry the crate apart with a crowbar.

CAUTION

Exercise extreme care to avoid damaging the buffer while opening the crate. Do not disturb the setting of any adjustment control.

2-7. INSPECTION. Examine the equipment after it has been unpacked. If any part of the buffer has been received in a damaged condition, report the damage at once to the shipper.

2-8. CABLING INSTRUCTIONS.

2-9. FOR ALL 144-A BUFFERS. The two Amphenol connectors used to connect the buffer to the external equipment must be wired as shown in Figure 2-1 or Figure 2-2. Use No. 22 wire to connect the load and unload information lines, the load and unload sync lines and the clear lines. Use No. 16 wire for the interconnection

between the buffer and the external equipment ground. Make all lines between the buffer and the external equipment as short as possible. Route the signal lines (sync, clear and information) as far as possible from noise sources.

2-10. FOR 144-BA-4 AND 144-BA-8 BUFFERS. Wire the INPUT and OUTPUT connectors as shown in Figure 2-1.

2-11. FOR 144-BQ-4 AND 144-BQ-8 BUFFERS. Wire the INPUT and OUTPUT connectors as shown in Figure 2-2.

2-12. PRELIMINARY CHECKS.

2-13. TEST EQUIPMENT REQUIRED. The following checks require a Tektronix Type 531 oscilloscope and a Simpson Model 260 multimeter or their equivalents.

2-14. INPUT SIGNALS. Check that the load sync pulses, unload sync pulses, clear pulses, information levels and power sources conform with the specifications of Paragraph 1-27.

NOTE

Do not attach the INPUT or OUTPUT connector at this time.

2-15. APPLICATION OF POWER. Connect the power source and turn the power on. The pilot indicator at the front of the power supply must light.

2-16. POWER SUPPLY OUTPUTS. Check all power supply output voltages in accordance with Paragraphs 5-14 through 5-17.

2-17. PCS OUTPUT. Check the output of the positive current stabilizer in accordance with Paragraph 5-18.

2-18. OPERATIONAL CHECKS. Perform the operational checks outlined in Paragraphs 5-9 through 5-13. If the buffer meets the requirements of the operational checks, perform the final installation.

2-19. INSTALLATION. The buffer may be installed in a standard

19-inch relay rack or notched for either Western Electric or Amateur racks. Other equipment may be mounted immediately below the buffer, but a space of at least 3/8 inch is required between the buffer and the equipment which is immediately above it. Ambient airflow provides sufficient cooling.

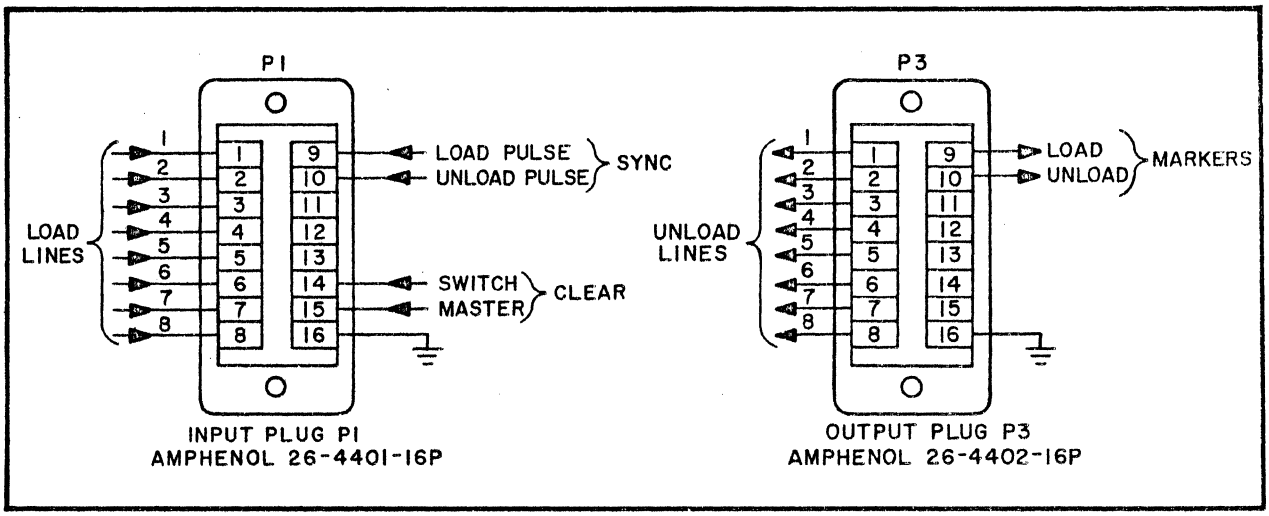


Figure 2-1. Input and Output Connector Wiring For 144-BA-4A, 144-BA-8A, 144-BQ-4A, and 144-BQ-8A Buffers.

NOTE

The 144-BQ-4A and 144-BQ-8A buffers do not use the switch clear input lead shown at Pin 14, Figure 2-1.

SECTION III

OPERATION

3-1. GENERAL.

3-2. This section contains the operating instructions required for the 144-A Core Buffer Memories. Before operating the buffer, check that all the installation instructions of Section II have been carried out.

3-3. INDICATORS AND CONTROLS.

3-4. The red indicator lamp on the front panel of the power supply will be lit if the buffer is receiving power. Screwdriver adjustment controls are located at the rear of the power supply. These control the power supply output voltages and the PCS output current which should be checked monthly.

3-5. INPUT AND OUTPUT TERMINALS.

3-6. All inputs and outputs of the 144-A buffers are illustrated in Figure 2-1.

3-7. OPERATING MODES.

3-8. DATA TRANSFER. This is the method of operation by which the buffer is used as a converter between two data systems which operate at different data processing rates. The buffer stores excess characters from the input equipment and unloads these characters at the operating rate of the output equipment.

3-9. 144-BQ-4A AND 144-BQ-8A BUFFERS. When these buffers are used for data transfer, a number of characters are loaded into the storage system, a portion of these are unloaded, and the load and unload commands continue alternating.

3-10. 144-BA-4A AND 144-BA-8A BUFFERS. When these buffers are used for data transfer, a number of characters are first loaded into the buffer. The buffer address circuits (magnetic switch) are then cleared. Next, any desired number of characters is unloaded. The address circuits and the storage system are then cleared. The loading and unloading process is continued as above.

NOTE

If the buffer is not completely emptied of information during the unloading process, the remaining characters will be destroyed by the following master clear pulse.

3-11. CIRCULATING REGISTER (BQ BUFFERS ONLY). During this mode of operation, a block of characters is first loaded into the buffer and the buffer is put through a program of loading and unloading. In this case, each character unloaded is returned to the buffer during the following load operation and the length of the information loop is determined by the length of the original block of characters. The register length is therefore equal to the number of characters stored in the buffer and may be changed by loading or unloading characters as required.

3-12. PARALLEL OPERATION. Two or more buffers may be connected for parallel operation in either the data transfer or the circulating register mode. The two buffers then operate as a single unit with the same 144-character capacity but with a larger character bit length.

3-13. SERIES OPERATION. Two or more buffers may be connected in series to increase the character storage capacity by multiples of 144.

3-14. OPERATING PROCEDURES.

3-15. PRELIMINARY CHECKS. Before operating a buffer, check that the input and output connectors are firmly attached and locked with their retainers. Check that the buffer is receiving power (the pilot lamp is lit).

3-16. 144-BA-4A AND 144-BA-8A BUFFERS. After performing the checks of paragraph 3-14, operate the buffer as follows:

(a) Clear both the address and the storage circuits by means of a master clear pulse.

(b) Load any number of characters up to 144.

(c) Clear the address circuits by means of a switch clear pulse.

(d) Unload any desired number of characters.

(e) Repeat step (a).

(f) Continue to load and unload characters as instructed in steps (a) through (e).

3-17. 144-BQ-4A AND 144-BQ-8A BUFFERS. After performing the checks of Paragraph 3-14, operate the buffer as follows:

(a) Clear the buffer by means of a master clear pulse.

(b) Load any number of characters up to 144.

(c) Unload any desired number of characters.

(d) Load as many characters as desired but do not exceed a total of 144 stored characters.

(e) Repeat steps C and D as many times as desired.

3-18. INPUT AND OUTPUT INFORMATION. Information is presented to a buffer in the form of d-c levels on the parallel input lines. A load sync pulse causes this information to be loaded. An unload sync pulse causes the unloading of one character. Refer to Paragraph 1-27 for input pulse levels, input pulse characteristics, timing requirements and output characteristics.

NOTE

Information stored in the buffer will be destroyed if power is removed. Always clear the buffer after power is applied.

3-19. If the buffer does not operate correctly, refer to Section V for troubleshooting information.

SECTION IV

THEORY OF OPERATION

4-1. GENERAL THEORY.

4-2. BLOCK DIAGRAM. (See Figure 4-1). The 144-A Core Buffer memories are core storage units designed to connect non-synchronized data systems. Each buffer consists basically of the control circuits, magnetic switches, digit drivers, storage system and read amplifiers shown in the block diagram. Figure 4-2, the timing chart, shows the timing relationships of signals from the above circuits.

4-3. CONTROL CIRCUITS. The input sync amplifier, the two phase drivers and strobe generator constitute the control circuits. Paragraphs 4-4 through 4-7 explain the interrelationship of these circuits in the 144-BQ buffers. The circuits have similar functions in the 144-BA buffers but the 144-BA buffers have only one two phase driver which is used for both loading and unloading information.

4-4. The input sync amplifier produces the following outputs on receipt of a load sync pulse from the external equipment:

(a) A delayed load sync pulse which is used to trigger the load two phase driver and the strobe generator. The load two phase driver, in turn, turns on the load magnetic switch.

(b) A gating level ($\overline{LU}$) which enables the digit drivers to supply information to the storage cores and enables the strobe generator to produce a load strobe pulse.

(c) A gating level (LU) which enables the strobe generator to produce a load marker strobe pulse during the load operation.

4-5. The input sync amplifier produces the following outputs on receipt of a unload sync pulse from the external equipment:

(a) A delayed unload sync pulse which is used to trigger the unload two phase driver and the strobe generator.

(b) A gating level (LU) which enables the unload strobe generator during the unload operation.

(c) A gating level ($\overline{LU}$) which prevents the strobe generator from producing a load strobe pulse during the unload operation.

4-6. The two phase drivers control the counting sequence of the magnetic switches. Successive delayed sync pulses at the input to a two phase driver result in current pulses at two outputs of the two phase driver in alternation. These current pulses step the magnetic switch through a predetermined counting sequence. Storage cores within the matrix are driven by currents from the magnetic switch.

4-7. The strobe generator produces strobe pulses which control the timing of the coincident current detectors and the read amplifiers. When the LU level is at the proper voltage, a delayed load sync pulse from the input sync amplifier causes the strobe generator to produce the load strobe pulse. This pulse controls the timing of the load coincident current detector. When the $\overline{LU}$ gating level is at the proper voltage, and the strobe generator receives a delayed unload sync pulse from the input sync amplifier, the strobe generator produces an unload strobe pulse. This pulse controls the timing of the unload coincident current detector and the read amplifiers.

4-8. MAGNETIC SWITCHES. In the 144-BQ buffers, the load magnetic switch selects the cores which are to store information when a character is being loaded and the unload magnetic switch selects those cores from which information is to be unloaded during the unloading of a character. The 144-BA buffer contains only one magnetic switch which is used for both loading and unloading. Each magnetic switch contains eighteen X output lines and eight Y output lines. At each step of its counting sequence, the magnetic switch drives a current pulse through one X matrix drive line and one Y matrix drive line in coincidence. Since there are 144 possible combinations of X and Y drive (18 x 8 = 144), the magnetic switch can select 144 distinct matrix addresses. The coincident currents from the magnetic switch are sufficient to turn over a core which is at the selected X and Y lines of the matrix.

4-9. DIGIT DRIVERS. The digit drivers present information to the storage cores which are selected by the load magnetic switch during the loading of a character. When the $\overline{LU}$ level from the input sync amplifier is at the proper voltage and the information input line is at the proper level, the digit driver drives an

inhibit current through one of the cores selected by the magnetic switch. This inhibit current opposes the coincident currents from the magnetic switch and prevents turnover of the core. A core which is allowed to turn over stores either a binary ONE or a binary ZERO, depending on whether the system is BA or BQ. (Refer to Paragraph 4-64).

4-10. STORAGE SYSTEM. The ferrite cores which store digital information bits are strung on the wires which constitute the X and Y drive lines. The storage matrix contains either four or eight digit planes, each plane contains 144 storage cores (18 x 8 drive lines). Each digit plane contains an inhibit line which is threaded through all 144 cores and an output line which is threaded through all 144 cores. A magnetic switch addresses one core of each plane during the load operation and during the unload operation. During the load operation, the digit drivers prevent certain cores from turning over by means of the inhibit current. During the unload operation, each core which is turned over supplies an information output from its read widning to one of the read amplifiers.

4-11. READ AMPLIFIERS. A read amplifier receives a pulse from a storage core when the core is turned over during an unload or load operation. In both the 144-BA and 144-BQ buffers, this pulse signifies a binary ONE information bit. The unload strobe pulse from the strobe generator permits a read amplifier to amplify a turnover signal only during the time of the core turnover signal. A read amplifier therefore cannot amplify a core turnover signal which may be produced by a sense winding during a load operation. The binary ONE pulses are fed from the read amplifiers to the external equipment on either four or eight output lines. The absence of a pulse at any information output indicates a binary ZERO information bit during the unloading operation.

4-12. COINCIDENT CURRENT DETECTORS. The coincident current detectors are optional equipment and their purpose is to produce an output marker pulse in synchronization with either the loading of a character or the unloading of a character at a particular address. Each coincident current detector is connected to an X drive line and a Y drive line of a magnetic switch. Since the particular X and Y drive lines are pulsed at only one address, the detector circuit receives coincident input signals only at this address. A strobe pulse(load or unload) from the strobe generator controls the timing of the marker output pulse.

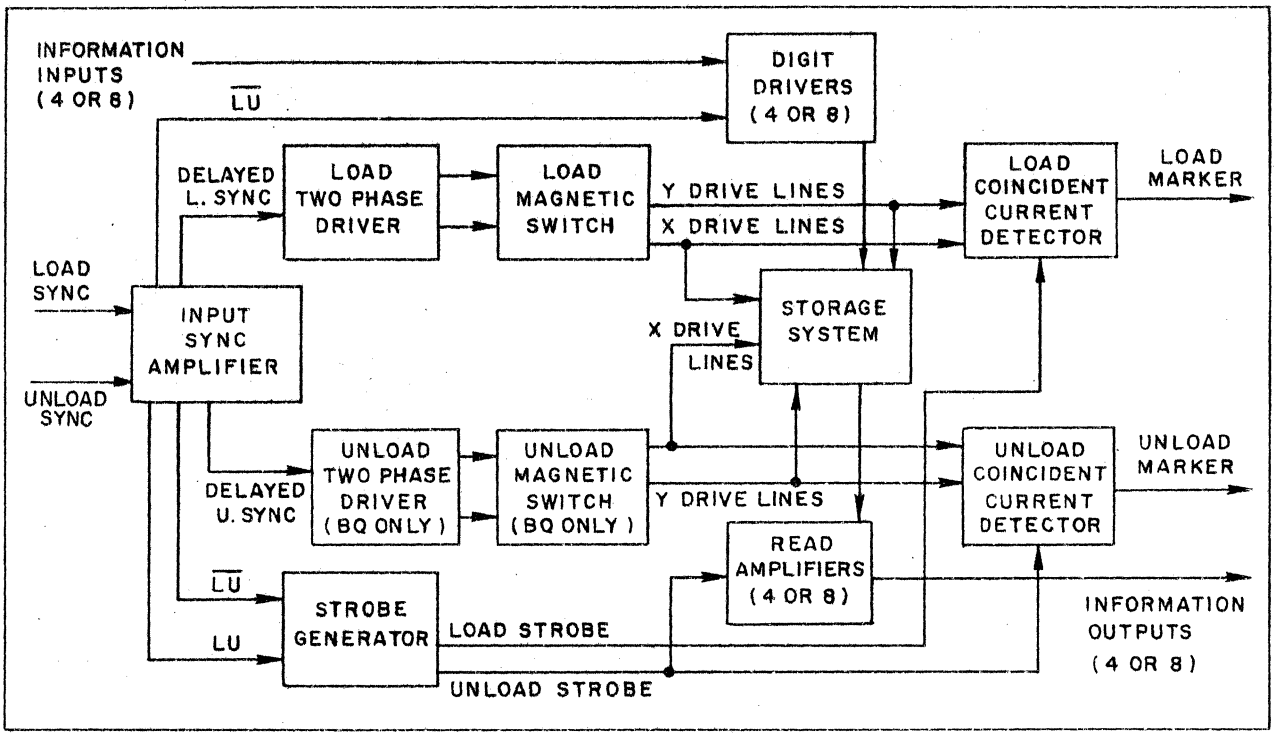


Figure 4-1. 144-A Core Buffer Memory, Block Diagram

4-13. DETAILED THEORY.

4-14. GENERAL. The following paragraphs explain the detailed theory of operation of the buffer circuits. The first drawing in Section VI of the manual (Figure 6-1) is a complete block diagram of the buffer. Figure 6-1 and the schematic diagrams of Section VI should be consulted while the detailed theory is being read.

4-15. INPUT SYNC AMPLIFIER.

4-16. See Figure 4-3 and 6-2. The input sync amplifier receives load sync pulses and unload sync pulses from the external equipment and delays these pulses for the purpose of triggering load and unload control circuits of the buffer. A flip-flop in the load sync amplifier produces gating levels which are used to gate the digit drivers and the strobe generator. Descriptions of the various input sync amplifier circuits follow.

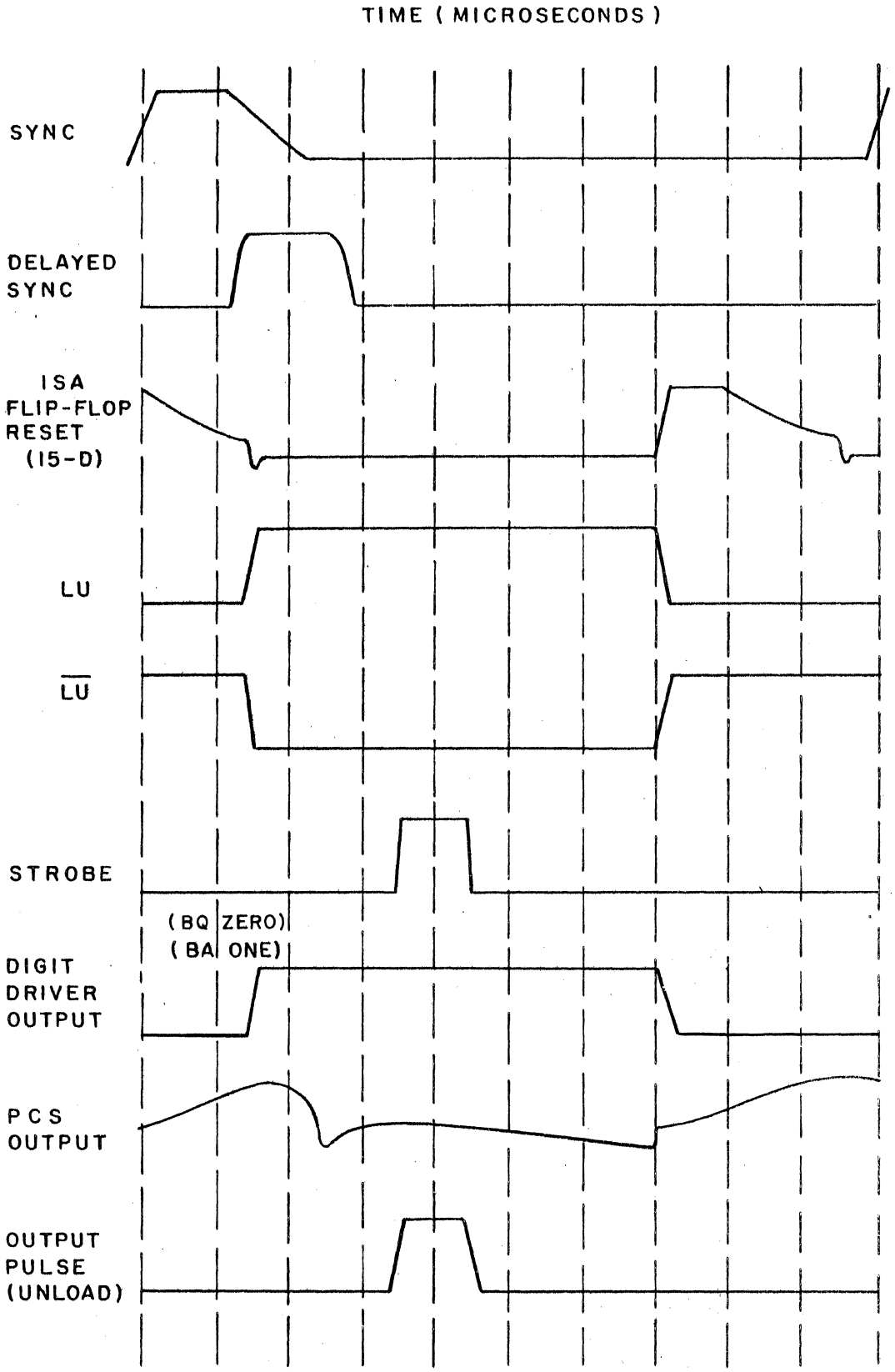


Figure 4-2. Timing Chart

4-17. LOAD SYNC AMPLIFIER. The input sync amplifier may be manufactured to utilize either positive or negative going input sync pulses. When only jumpers W2 and W4 are disconnected, the input circuits are wired to accomodate positive-going load and unload sync pulses. When only jumpers W1 and W3 are disconnected, the inputs are wired for negative going sync pulses.

4-18. In either case, Q1 amplifies the load sync pulse at input A-1 or A-2 and a negative pulse from the Q1 collector is coupled through C2 and CR7 to load sync blocking oscillator Q2.

4-19. LOAD SYNC BLOCKING OSCILLATOR. A negative pulse from the collector of Q1 triggers blocking oscillator Q2. Transistor Q2 is normally cut off and the negative pulse at its base drives it into conduction. As the transistor conducts through the primary winding of T1, feedback current flows in the Q2 base circuit through R33 and the feedback winding of T1. This causes the transistor to saturate for the duration of the pulse. On saturation, the field about the transformer collapses and an inductive kick from the feedback winding turns Q2 off. The entire cycle takes place during a period of approximately 1.5 microseconds. Resistor R14 and transformer T1 comprise the resistance-inductance elements which determine the cycle time.

4-20. LOAD DELAY AMPLIFIER. During the time that the blocking oscillator conducts, a positive pulse is coupled from terminal 6 of T1 to the base of load delay amplifier Q3, which is normally cut-off. A negative excursion at the trailing edge of the positive pulse drives Q3 into conduction and a positive pulse appears at output A-1. Since Q3 is turned on by the trailing edge of the blocking oscillator pulse, the A-1 output pulse is delayed 1.0 microsecond in relation to the load sync pulse.

4-21. UNLOAD SYNC AMPLIFIER. The operation of unload sync amplifier Q6 is similar to that of the load sync amplifier (Paragraph 4-17).

4-22. UNLOAD SYNC BLOCKING OSCILLATOR. The operation of unload sync blocking oscillator Q7 is identical to that of the load sync blocking oscillator (Paragraph 4-19).

4-23. UNLOAD DELAY AMPLIFIER. The operation of unload delay amplifier Q8 is identical to that of the load delay amplifier (Paragraph 4-20). Its output (B-1) is delayed 1.0 microsecond with respect to the unload sync pulse.

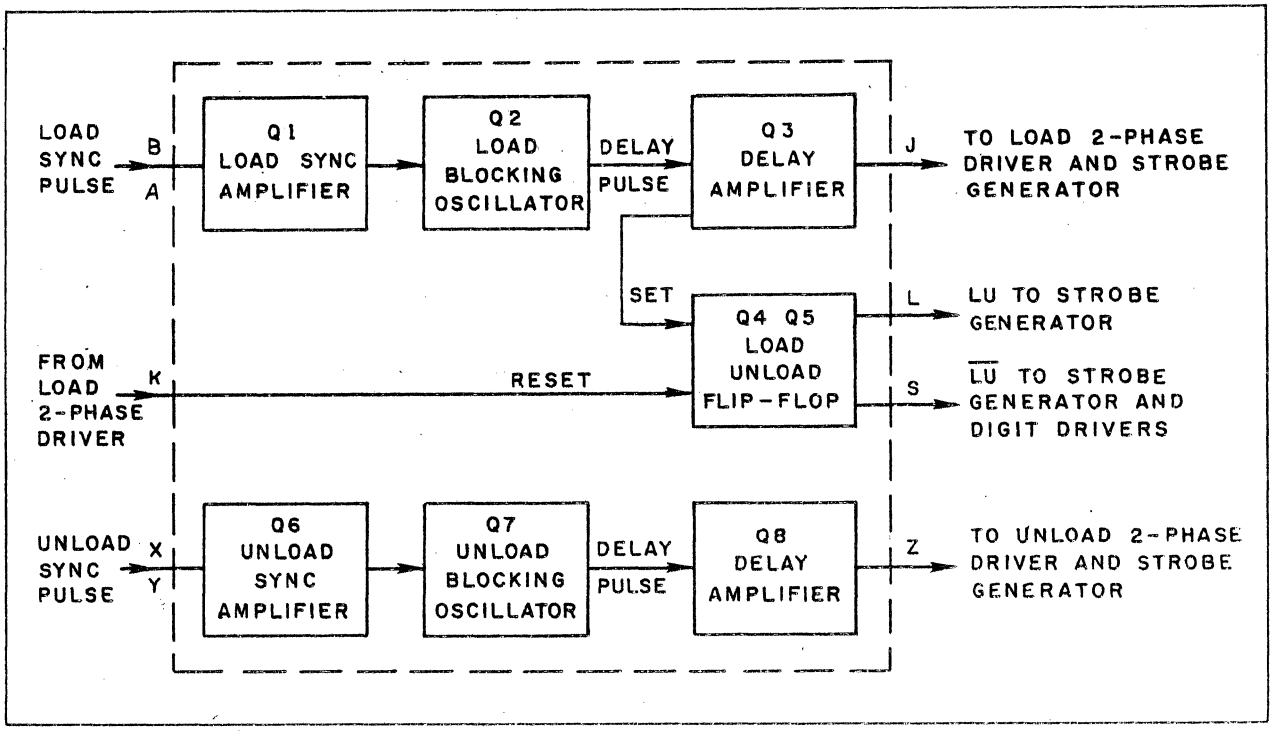


Figure 4-3. Input Sync Amplifier, Block Diagram

4-24. LOAD-UNLOAD FLIP-FLOP. Transistors Q4 and Q5 and associated components comprise the load-unload flip-flop. The flip-flop provides two gating levels which are designated LU and $\overline{LU}$. These levels are used to gate various load and unload circuits of the buffer. The LU level is obtained from the collector of Q5 and the $\overline{LU}$ level from the collector of Q4. When power is first turned on, either Q4 or Q5 may conduct. When a character is being loaded into the buffer, the LU level must be at +5 volts (high) and the $\overline{LU}$ level must be at -5 volts (low). This is called the LOAD state of the flip-flop. Should Q4 conduct when power is first turned on (UNLOAD state with LU low and $\overline{LU}$ high), a delayed pulse from delay amplifier Q3 is coupled through C4 and CR13, cutting off Q4 and switching the flip-flop. This occurs as a result of the first load sync pulse from the external equipment, so that the LU and $\overline{LU}$ levels are correct when the first character is loaded into the buffer. Should Q5 conduct when power is first turned on, the LU and $\overline{LU}$ levels are correct and the pulse from Q2 has no effect on the flip-flop.

4-25. Each subsequent load sync pulse results in a delayed load sync pulse output and switches the flip-flop. Approximately 6 microseconds

after zero time (Paragraph 1-27), a reset pulse from the load two phase driver resets the flip-flop to the UNLOAD state.

4-26. Since the load-unload flip-flop is automatically reset to the UNLOAD state, a short time after it is switched to the LOAD state, the LU and $\overline{LU}$ levels are always correct for unloading a character when an unload sync pulse is received by the buffer. However, sufficient time must be allowed between a load sync pulse and an unload sync pulse for resetting the flip-flop.

4-27. TWO PHASE DRIVERS. (See Figures 4-4 and 6-3).

4-28. BA BUFFERS. The 144-BA-4A and 144-BA-8A buffers contain one two phase driver circuit card (load-unload) which is used to step the load-unload magnetic switch. At the start of operations, the driver is set to its initial state by a clear pulse from the electronic clear circuit. After it has been cleared, the two phase driver feeds current pulses to the load-unload magnetic switch on two output lines in alternation. The load-unload two phase driver is triggered by delayed load sync pulses from the input sync amplifier and delayed unload sync pulses through the dummy circuit card (Paragraph 4-48).

4-29. BQ BUFFERS. The 144-BQ-4A and 144-BQ-8A buffers contain two identical two phase driver circuit cards (load and unload). The load two phase driver advances the load magnetic switch and the unload two phase driver advances the unload magnetic switch. At the start of operations, both drivers are cleared to their initial states by a pulse from the electronic clear circuit. The load two phase driver is triggered by delayed load sync pulses from the input sync amplifier and the unload two phase driver by delayed unload sync pulses from the input sync amplifier. Successive load sync pulses result in current pulses from the load two phase driver to the load magnetic switch on two output lines in alternation. Successive unload sync pulses result in current pulses from the unload two phase driver to the unload magnetic switch on two output lines in alternation.

4-30. CIRCUITS. The two phase drivers of the BA and BQ buffers are identical. Each driver contains an inverter, a flip-flop, two blocking oscillators and two transistor switches. Delayed sync pulses (load or unload) trigger the blocking oscillators in alternation. The operation of the flip-flop is similar to that of the input sync amplifier and it gates the blocking oscillators

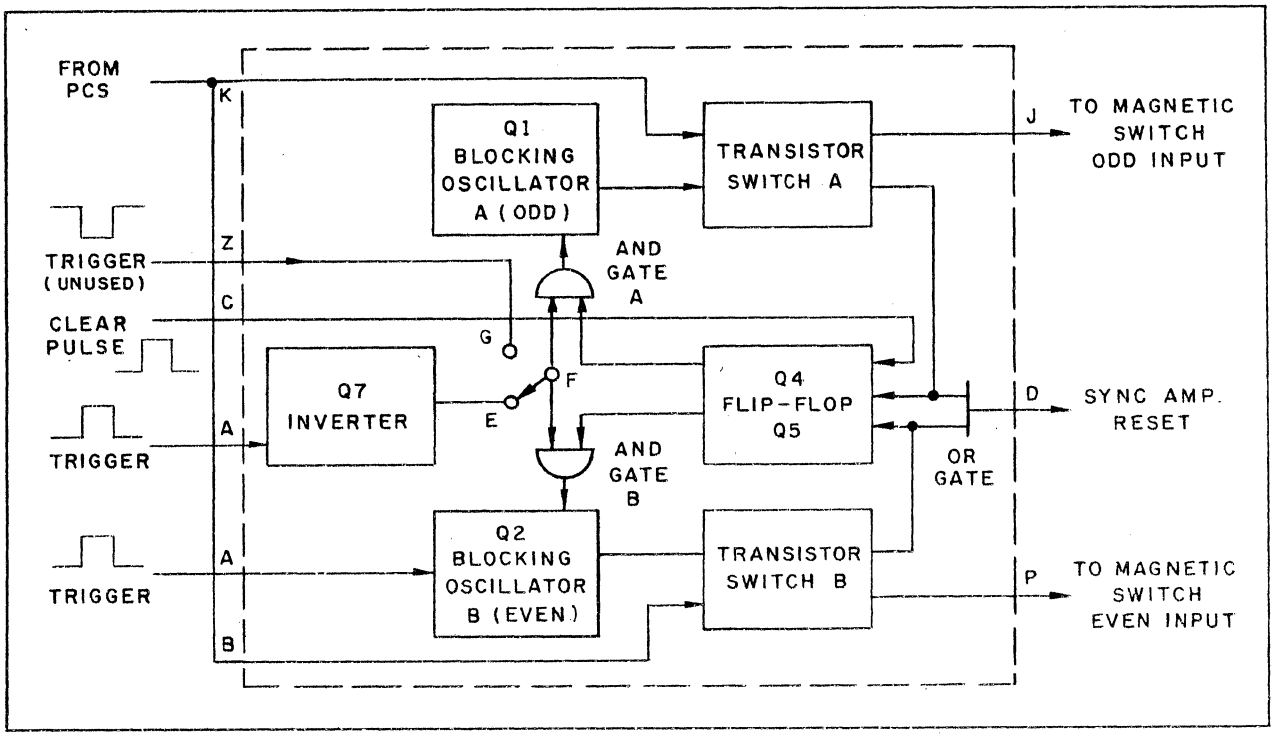


Figure 4-4. Two Phase Driver, Block Diagram

so that they are triggered in the proper sequence. Each of the transistor switches is connected between the positive current stabilizer and one drive line of the magnetic switch. The blocking oscillators turn on the magnetic switches in alternation, permitting current flow through the magnetic switch drive lines.

4-31. At the start of operations, the ODD input of the magnetic switch must be driven first so that the magnetic switch will select matrix address No. 1 for the loading of the first character. For this reason, a positive clear pulse is used to cut off Q5 if it should happen to conduct after the power is first turned on. This switches the flip-flop to the ODD state so that blocking oscillator A is the first to be triggered. In the 144-BA-4A and 144-BA-8A buffers, the same two phase driver is used for loading and unloading operations. In these buffers it is necessary to clear the two phase driver to the ODD state prior to the loading or unloading of any characters. This so so because the BA buffers have only one magnetic switch which must return to the first address prior to unloading one or more characters. The two phase drivers of the BQ buffers need not be cleared prior to the unloading of information.

4-32. INPUT CIRCUITRY. Positive trigger pulses from the input sync amplifier are inverted by transistor Q7 and applied as negative pulses to diodes CR17 and CR19 in parallel. The printed circuit card contains a provision for bypassing the inverter to permit the use of negative-going input pulses.

4-33. NEGATIVE AND GATES. (See Figure 4-5). Diodes CR17 and CR18 comprise AND gate A at the input to blocking oscillator A. The collector of Q4 may be at either -5 or +5 volts, depending on the state of flip-flop Q4-Q5. When the collector of Q4 is at +5 volts, CR8 conducts through R8 so that the AND gate output is clamped to the +5 volt level. Diode CR17 is therefore biased in reverse and a negative going sync pulse cannot cause CR17 to conduct. When the Q4 collector is at -5 volts and no sync pulse exists at the sync input, CR17 clamps the output of the AND gate to the +5 volt level of the Q7 collector and CR8 is reverse biased. On arrival of the sync pulse, CR17 conducts so that the AND gate output drops to -5 volts. AND gate A thus passes a sync pulse only when the flip-flop is in the even state and the collector of Q4 is at a -5 volt level.

4-34. Diodes CR13 and CR19 and resistor R19 comprise AND gate B at the input to blocking oscillator B (See Figure 6-3). AND gate B allows blocking oscillator B to be triggered only when the flip-flop is in the odd state and the collector of Q5 is at a -5 volt level.

4-35. BLOCKING OSCILLATORS. (See Figure 4-5). The negative going pulse at the output of AND gate A causes CR7 to conduct and the voltage at terminal 4 of transformer T1 drops from +5 to -5 volts. The resulting current change through winding 1-4 induces a current in 3-6 to drive the base of Q3 negative while feedback drives Q1 into conduction through 2-5. When Q1 saturates the transformer field collapses to turn off both transistors. Resistor R1 and T1 comprise the resistance-inductance circuit which determine the blocking oscillator cycle time. The transistor junction resistance is negligible in this respect.

4-36. The collector circuit of Q1 may be wired in three configurations as shown on Figure 6-3.

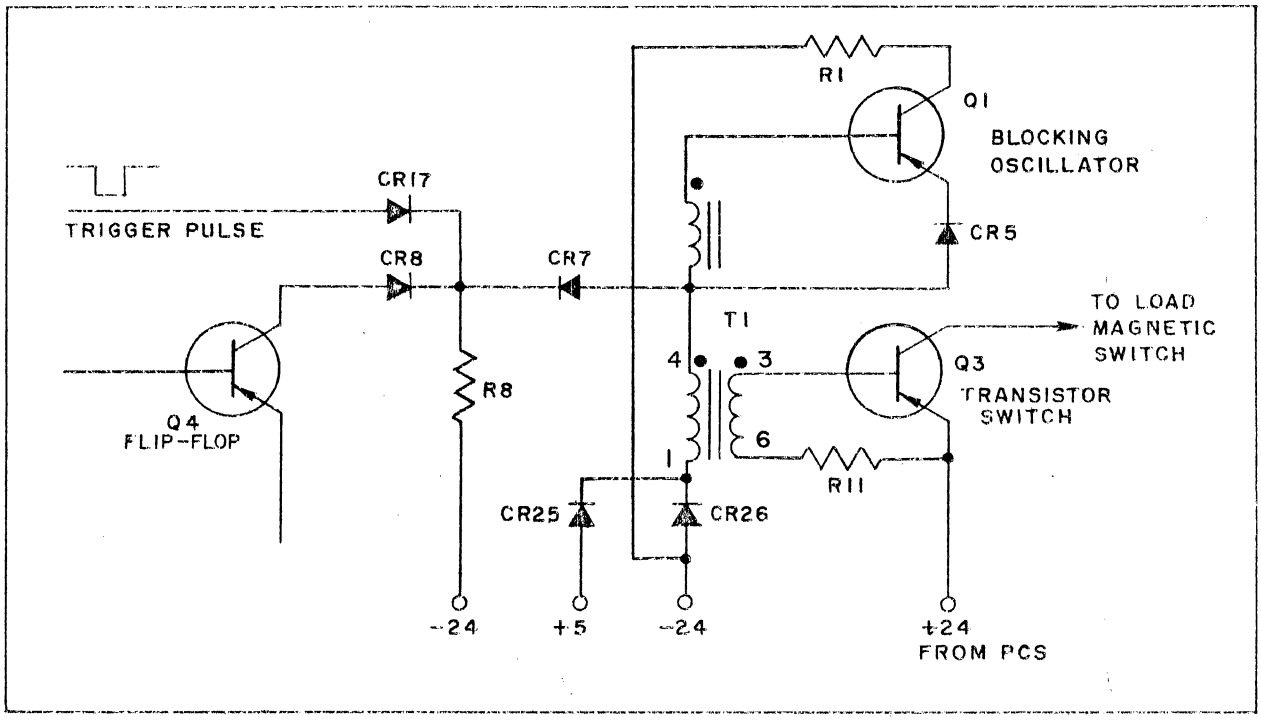


Figure 4-5. AND Gate and Blocking Oscillator, Simplified Schematic Diagram

Resistor R1 is temperature sensitive and maintains a constant ratio of L/R, thus maintaining a constant pulse duration with varying temperature.

4-37. The operation of blocking oscillator B is identical to that of blocking oscillator A.

4-38. TRANSISTOR SWITCHES. Transistor switch A and transistor switch B are identical. During the time that Q1 conducts, a current is induced in winding 3-6 of T1. This currents turns on transistor switch Q3 during the blocking oscillator cycle. Transistor Q3 is in series with the positive current stabilizer (PCS) and the even drive line of the magnetic stepping switch.

During the time that Q1 conducts, current flows from the PCS through Q3 to the drive line of the magnetic switch. The duration of the current pulses through the transistor switch is dependent on the cycle time of the blocking oscillator.

4-39. DIODE NETWORK. (See Figure 6-3). Diodes CR25 and CR26 and capacitor C4 form a network which maintains a constant operating voltage across the blocking oscillators. Zener diode CR26 maintains a constant voltage across resistor R1 and terminal 1 of the transformer. Diode CR25 maintains a voltage-drop of approximately .6 volts, and applies a +4.4 volt level to the base of Q1. This keeps Q1 cut off between trigger pulses.

4-40. LOAD-UNLOAD SYNC OUTPUT. (See Figure 6-3). When the field about the blocking oscillator transformer collapses at the end of the cycle, the inductive kickback of the transformer causes a positive excursion at the trailing edge of the negative pulse. This positive pulse (at terminal 5 of either T1 or T2) causes diode CR15 or diode CR21 to conduct through resistor R20 and the reset input circuit of the load-unload flip-flop in the input sync amplifier.

4-41. MAGNETIC STEPPING SWITCH. (See Figure 4-6).

4-42. The magnetic stepping switch is driven by constant current pulses from a two phase driver. Drive currents appearing at the two inputs of the magnetic switch in alternation enable the switch to steer current through successive lines of the storage matrix. The magnetic switches of the BA buffers and the BQ buffers are identical. Different methods are employed for the loading and unloading of information in BA and BQ buffers (Paragraph 4-14). The different techniques used in storage core switching involve the operation of the digit drivers and the coding of information in the matrix. Magnetic switches of the BA and BQ buffers operate in exactly the same manner.

4-43. Each switch core has four windings (clear, set, drive, and output). The clear winding starts the counting operation by setting all the cores except T25 and T34 to ZERO. Since the reset winding is wound oppositely on these two cores they are initially set to ONE.

4-44. The first input pulse on line 1 then sees a low impedance path through all the core windings in its row except T25 and T34. These cores are turned to ZERO by the input pulse. As they turn from ONE

to ZERO a voltage is induced in their output windings.

4-45. The T34 output current passes through the T9 set winding, turning T9 to ONE, through the first matrix X line, and through the X ODD wire to the output winding of T25. The current from T25 now sets up T1 and passes through the first matrix Y lines to ground. All cores except T1 and T9 are now set to ZERO, and one core in each of the matrices (1,1) has been driven with a full current.

4-46. The first input 2 pulse turns T1 and T9 to ZERO. These cores now energize the T18 and T26 set windings and apply current through CR2 and CR18 to Y line 1 and X line 2 of the matrices.

4-47. The next input 1 pulse turns cores T18 and T26 to drive Y line 2 and X line 3 in exactly the same way. Notice that the switches steer stabilized current from step to step because the ferrite switch cores store information as to the next switch position address. The cores are able to act as counters in this manner because they have two stable states. This is further discussed in connection with the storage system explained in Paragraph 4-60.

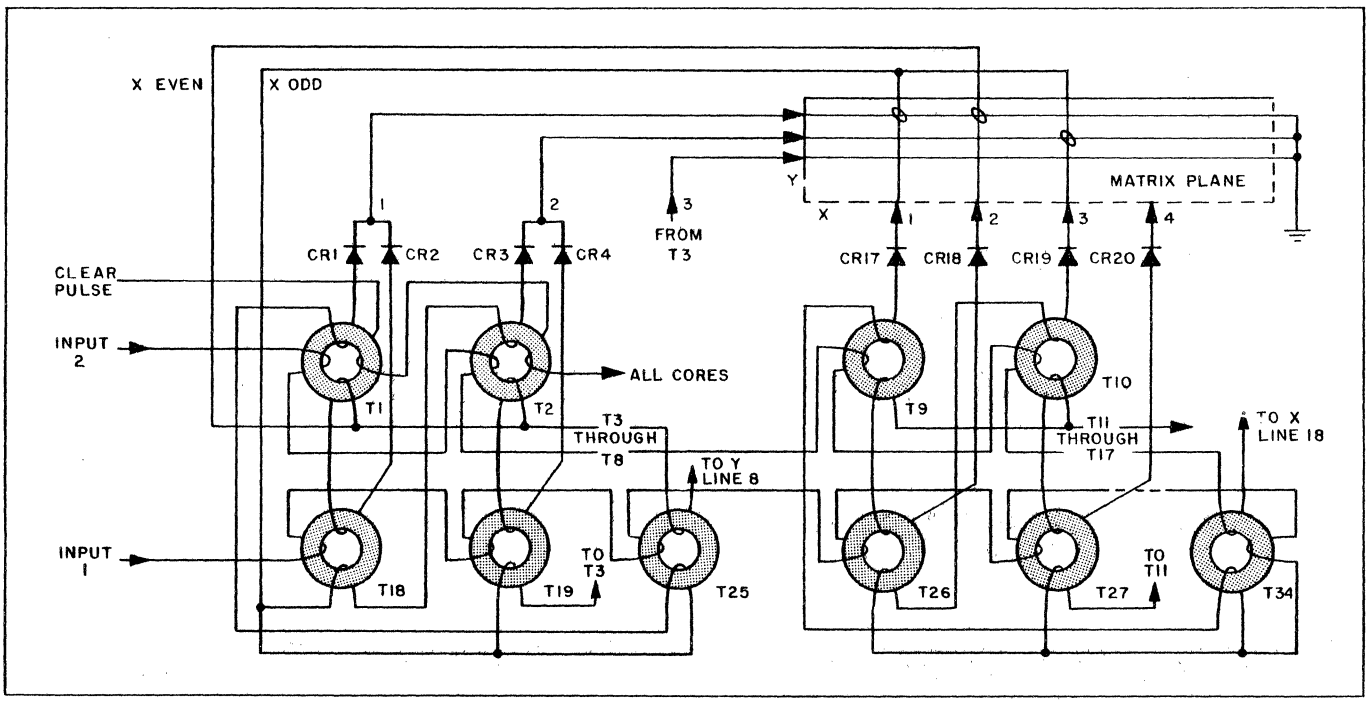


Figure 4-6. Magnetic Stepping Switches, Simplified Schematic Diagram

4-48. DUMMY CIRCUIT CARD (BA ONLY). (See Figure 6-5). The wiring of card cage connector No. 7 is identical in both the BQ and BA buffers. In the BQ buffers, the unload magnetic switch is installed in this position. The BA buffers contain a dummy circuit card in place of the unload magnetic switch to provide continuity for the following signals. (Refer also to Paragraph 4-64):

(a) The switch clear pulse.

(b) The delayed unload sync pulse which triggers the load-unload two phase driver during an unload operation.

4-49. POSITIVE CURRENT STABILIZER. (See Figure 6-6).

4-50. The positive current stabilizer (PCS) is connected between the power supply and the two phase driver transistor switches to maintain the current which flows through the storage system at a value which is independent of load changes. The current from the PCS is adjusted to approximately 150 milliamperes by means of a 50 ohm potentiometer which is located in the power supply (R15).

4-51. Transistors Q1 and Q4 are the linear current stabilizers which operate in parallel to maintain a constant current output at pin H of the PCS. The linear current stabilizers receive an error signal from operational amplifier Q3 in order to compensate the output current for changes in temperature. An increase in the environmental temperature results in a decrease in the output current and a decrease in temperature results in an increase in the output current.

4-52. Transistor Q3 maintains a constant reference potential at the junction of R9 and R12. Resistor R13 is a sensistor (temperature sensitive resistor) with a positive temperature coefficient. With an increase in temperature, the current flow through R13, R12 and R9 decreases. Because of the constant potential at the junction of R9 and R12, this results in a decrease of the current flow through the base circuits of Q1 and Q4 and a resultant decrease in the output current of the PCS.

4-53. Diodes CR5 through CR9 maintain a constant reference potential at the base of current amplifier Q2. Transistor Q2 maintains a constant reference potential at the emitter of Q3, matching the high impedance of the diode network to the low impedance input of the operational amplifier.

4-54. Diodes CR1 through CR4 provide a current path for the output of Q1 and Q4 under no-load conditions. These diodes conduct when the output potential of the PCS rises above +16 volts.

4-55. DIGIT DRIVER. (See Figure 4-7).

4-56. The digit drivers control the switching of storage cores within the storage matrix. They do this by permitting an inhibit current to flow through the digit plane windings of a selected matrix plane as a character is being loaded into the buffer. The inhibit current prevents the switching of a storage core. Each digit driver circuit card contains four identical digit driver circuits. Each circuit contains an information input, a gate input and an information (current) output.

4-57. INPUT CIRCUITRY. In the 144-BA-4A and 144-BA-8A buffers, a binary ONE signal at the information input results in the flow of inhibit current. This signal may be either a positive voltage level or a negative voltage level, depending on how the digit input is wired. The digit driver of Figure 4-7 is wired so that a positive level at input A-2 constitutes the binary ONE signal for a BA buffer. In the 144-BQ-4A and 144-BQ-8A buffers, a binary ZERO signal at the information input results in the flow of inhibit current. This signal may be either a positive or a negative level, depending on how the digit driver input is wired. The digit driver of Figure 4-7 is wired so that a positive level at input A-2 constitutes the binary ZERO signal for a BQ buffer.

4-58. Normally, transistor Q1 is conducting and the input binary ONE signal cuts it off, causing its collector voltage to become more negative. Diodes CR1 and CR6 and resistor R10 comprise a negative AND gate at the input to Q2. This AND gate is similar to those of the two phase driver (Paragraph 4-33) and its output level is either at -5 volts or +5 volts. When the signal pulse and the gating level are present in coincidence, the AND gate output is at -5 volts and Q2 is driven into conduction. Transistor Q2 drives Q3 which, in turn, drives output transistor Q4 into conduction. Current flows from ground through Q4 and the inhibit winding to the -14 volt supply when the signal pulse and the gating level are present in coincidence.

4-59. STORAGE SYSTEM.

4-60. CORE PROPERTIES. (See Figure 4-8). The storage property of the ferrite core lies in the fact that it will remain

magnetized indefinitely in one of two possible states. These states are the directions of magnetization shown by the hysteresis loop of Figure 4-8. Current from one direction (P) drives the core into one state of magnetization. Pulses of the opposite direction (N) drive the core into the opposite state of magnetization. The core will remain in either state until it is subjected to a magnetomotive force of sufficient strength and of the correct polarity to reverse the magnetization of the core.

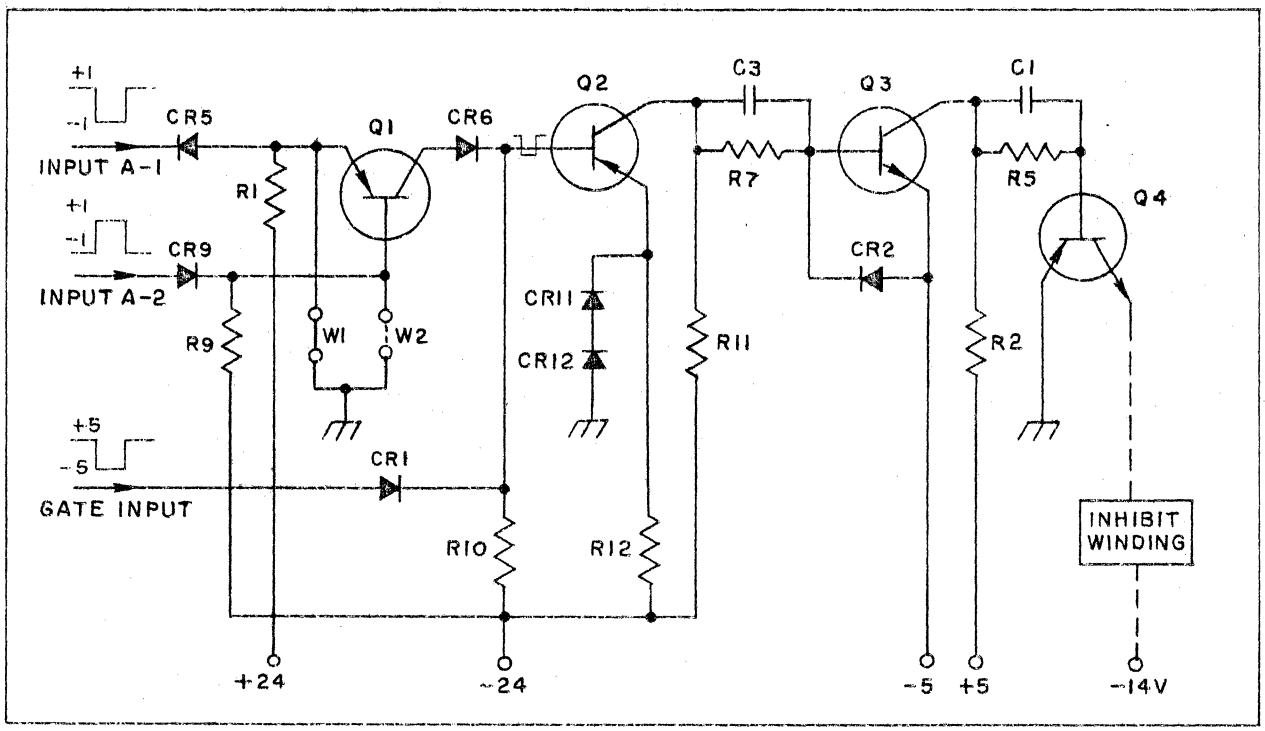


Figure 4-7. Digit Driver, Simplified Schematic Diagram

4-61. The cores are dynamic storage devices. That is, their state is only sensed during the time that the magnetic state of a core is changing from one state to another. This is called "destructive readout".

4-62. CORE WINDINGS. (See Figure 4-8). Several windings pass through each core. The X and Y windings are driven by the magnetic stepping switches to provide coincident currents at selected cores. The clear winding carries the full switching current in a direction which switches all the cores to the ZERO

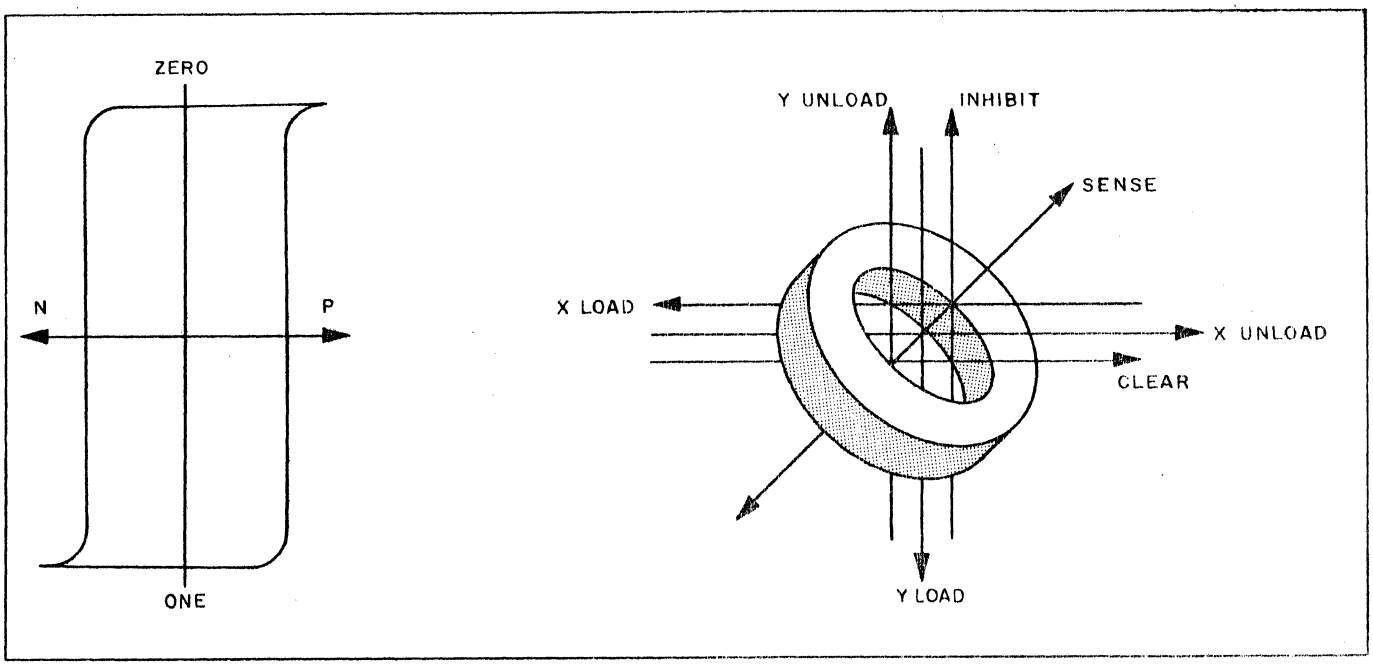


Figure 4-8. Storage Core Hysteresis Loop and Core Windings

state. The inhibit winding is energized by the digit drivers so as to cancel the effect of the load X and Y windings in order to prevent turnover of a core. The sense windings are coupled to the read amplifier inputs and carry current which is induced by the change in flux when a core changes its state (turns over).

4-63. The X and Y windings carry only half the current required to turn over a core. The inhibit winding also carries a half current, but in a direction opposite to that of the Y load windings. The inhibit current thus acts to reduce what would otherwise be the full coincident current by approximately one-half.

4-64. LOADING AND UNLOADING. The loading and unloading sequences differ in the 144-BA and the 144-BQ buffers. Different techniques are used because the BQ buffers contain two magnetic switches whereas the BA buffers contain only one. In the BA buffers, the unload switch is replaced by a dummy circuit card. The dummy card provides continuity for circuits of the load magnetic switch which are in series with the unload magnetic switch in the 144-BQ buffers. In the 144-BQ buffers, the load magnetic switch drives currents

through the selected core windings in the directions which tend to switch the cores to the ONE state during the loading of a character. During the unloading of a character, the unload magnetic switch of the 144-BQ buffer drives currents through the selected switch core windings in directions which tend to switch the cores to their ZERO states. Since the 144-BA buffers have only one magnetic switch, both the load and unload drive currents must be driven in the same direction in these buffers. Therefore, in the BA buffers, inhibit currents are applied to each core which is to load a binary ONE during the loading of a character (the opposite is true of the BQ buffers). All the selected cores which do not receive inhibit currents are switched. Those cores which have been switched are in the ZERO state and those that have not are in the ONE state. In unloading a character from a 144-BA buffer, drive currents are driven through the selected core windings so as to switch all cores to the ZERO state. Those cores which were not switched during the loading of the character are now turned over and produce signal pulses which signify a binary ONE.

4-65. LOADING OF 144-BQ-4A AND 144-BQ-8A BUFFERS.

(a) The clear winding is energized, setting the switches to the first address and all matrix cores which are in the ONE state to the ZERO state. Cores which are in the ZERO state prior to the clearing pulse are not turned over.

(b) A load sync pulse triggers the load blocking oscillator of the input sync amplifier. The oscillator, in turn, switches the load-unload flip-flop and feeds a delayed load sync pulse to the load two phase driver. The flip-flop gates the digit drivers and the two phase driver steps the magnetic switch to address No. 2. As the magnetic switch is being stepped, it feeds a drive current through the X and Y windings of all cores in the first address.

(c) A binary ZERO information input to any digit driver causes that driver to energize the inhibit winding of the matrix plane to which it is connected. This prevents turn over of the selected core in that matrix plane.

(d) Those information input lines with binary ONE voltage levels do not allow the digit drivers to conduct and the load magnetic switch drives the associated storage cores to the ONE state.

(e) The result is a stored character. Each of the cores which were switched to the ONE state during the above sequence contains a binary ONE information bit. Each core which was prevented from being switched contains a binary ZERO information bit.

(f) The above process may be repeated as many as 144 times without unloading or clearing.

4-66. UNLOADING OF 144-BQ-4A and 144-BQ-8A BUFFERS.

(a) An unload sync pulse triggers the unload blocking oscillator of the input sync amplifier card and a delayed sync pulse is fed from the blocking oscillator to the unload two phase driver. The two phase driver, in turn, drives the unload magnetic switch. The unload magnetic switch, in turn, drives coincident currents through each of the selected cores in the reverse (unload) direction.

(b) Those cores which are in the binary ONE state turn over when subjected to the unload currents from the magnetic switch. As a core turns over, it induces a current in its sense winding which drives the associated read amplifier. Only those cores which are in the ONE state turn over, so that the current which is induced in the sense winding constitutes a binary ONE signal.

(c) The above unloading process may be initiated at any time as long as a sufficient delay is allowed between the previous load sync pulse and the unload sync pulse. The process may be repeated as many times as is desired, after which the load process may be resumed, without clearing.

4-67. LOADING OF 144-BA-4A AND 144-BA-8A BUFFERS.

(a) The magnetic switch and the matrix clear windings are energized. This sets the magnetic switch to address No. 1 and sets all cores of the matrix which are in the ZERO state to the ONE state.

NOTE

This and following steps differ from corresponding steps of paragraph 4-65.

(b) A load sync pulse triggers the load blocking oscillator of the input sync amplifier. The oscillator, in turn, triggers the load-unload flip-flop and feeds a delayed pulse to the two phase driver. The flip-flop gates the digit drivers and the two phase driver steps the magnetic switch to address No. 2. As the switch is being stepped, it feeds drive current through all cores of the first address.

(c) A binary ONE information input to any of the digit drivers causes that driver to energize the inhibit winding of the matrix plane to which it is connected. This prevents turn over of the selected cores in that plane.

(d) Those information input lines with binary ZERO information levels do not cause the digit drivers to conduct and the magnetic switch drives the associated storage cores to the ZERO state.

(e) The result is a stored character. Each of the cores which were switched to the ZERO state during the loading of the character contains a binary ZERO information bit. The remainder of the selected cores contain binary ONE information bits.

(f) The above process may be repeated as many as 144 times without clearing.

4-68. UNLOADING OF 144-BA-4A AND 144-BA-8A BUFFERS.

(a) A switch clear pulse resets the magnetic switch to address No. 1.

(b) An unload sync pulse triggers the unload blocking oscillator in the input sync amplifier and a delayed sync pulse is fed from the blocking oscillator to the load-unload two phase driver. The two phase driver, in turn, drives the magnetic switch. The magnetic switch drives coincident currents through each of the selected cores in the same direction as during step (b) of Paragraph 4-67.

(c) Those cores which are now in the binary ONE state turn over when subjected to the coincident currents from the magnetic switch. As a core turns over, it induces a current in its sense winding which drives the associated read amplifier.

Only those cores which are now in the ONE state turn over, so that the current which is induced in the sense winding constitutes a binary ONE signal.

(d) The above unloading process may be repeated until the buffer is empty. Both the matrix and the magnetic switch must be cleared prior to the loading of additional characters.

4-69. PHYSICAL CONSTRUCTION OF STORAGE SYSTEM. During manufacture of the storage matrices, two additional lines of cores are strung on each frame to facilitate assembly. This results in an actual total of 180 ferrite cores in each plane, of which only 144 cores are used.

4-70. Although coincident half select currents from the X and Y windings are required to change the state of a core, the cores on the selected X and Y wires are affected to some extent by the half excitation X and Y pulses. The sense winding is therefore interlaced through the cores in such a manner as to cancel these spurous signals from half selected cores. The winding is arranged so that cancellation occurs in pairs.

4-71. The sense winding produces a full turnover signal when a core is turned over during the loading of a character as well as during the unloading of a character. The strobe generator produces the unload strobe pulse only during an unload cycle to gate the read amplifiers. Since the read amplifiers are disabled during the load cycle, turnover signals which are produced during the loading of a character are blocked by the read amplifiers.

4-72. READ AMPLIFIERS (See Figure 4-9).

4-72a. Each read amplifier printed circuit card contains four read amplifier circuits. Each read amplifier circuit presents a binary ONE signal on a buffer unload line on receipt of a sense winding turn-over signal from the matrix in coincidence with a strobe pulse from the strobe generator.

4-73. Both ends of the matrix plane sense winding are connected to input transformer T1. Since the sense windings are laced through the cores in opposing directions (paragraph 4-70), the signal to the read amplifier may be of either polarity.

4-74. Between signal pulses, transistors Q1 and Q3 conduct slightly. On receipt of a pulse from the matrix, one of the transistors saturates and the other becomes cut off. The polarity of the signal pulse determines which of the transistors will conduct. There is a 10 microfarad capacitor between the emitter of each transistor and ground. Because of the capacitors, the transistor which conducts operates as a grounded emitter amplifier when the signal is present.

4-75. Any signal will be amplified by Q1 or Q3. When the signal is present, the conduction of Q1 or Q3 through resistor R3 produces a negative pulse at the base of Q2. The strobe input line which is in series with Q2 is normally at a -5 volt level. The strobe pulse raises the Q2 emitter voltage from -5 to +5 volts so that the transistor can conduct when a signal is present at its base. Potentiometer R14 of the strobe generator circuit card is adjusted so that the strobe pulse occurs at the correct time (Paragraph 4-72).

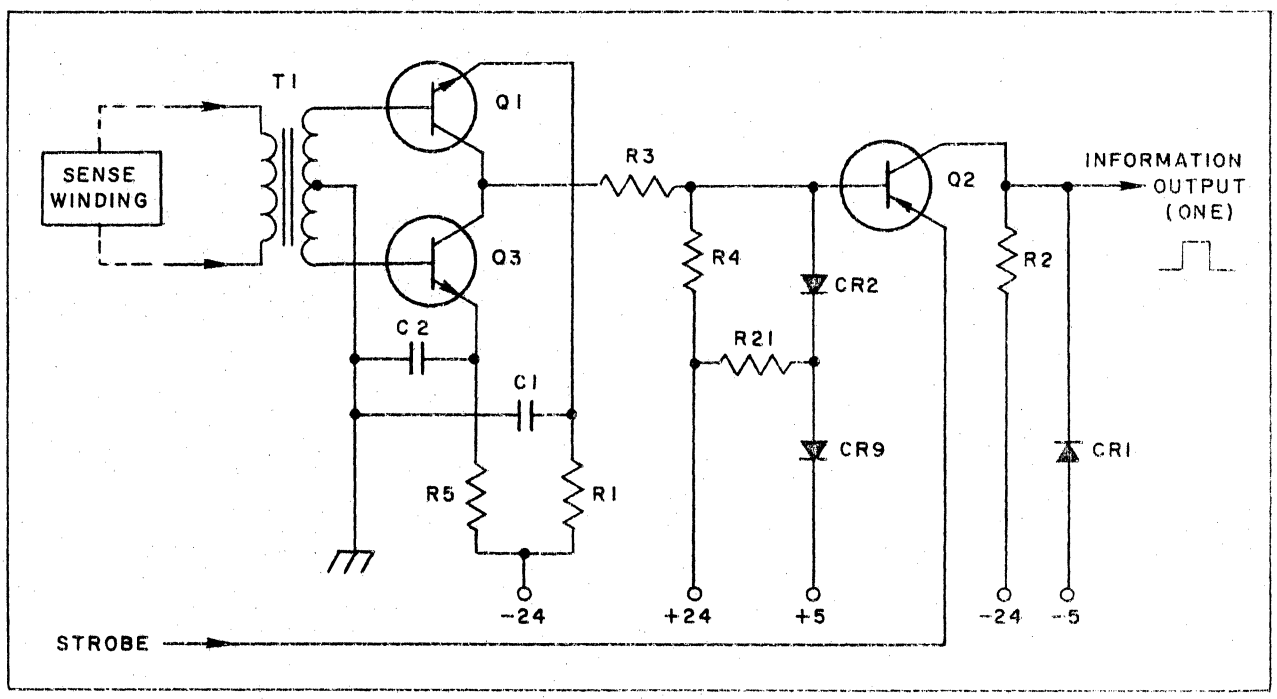


Figure 4-9. Read Amplifier, Simplified Schematic Diagram

4-76. STROBE GENERATOR. (See Figures 4-10 and 6-9).

4-77. GENERAL. The strobe generator produces strobe pulses which enable the load coincident current detector, the unload

coincident current detector and the read amplifiers at the proper times. It contains the following circuits: delay blocking oscillator, delay amplifier, load strobe blocking oscillator, unload strobe blocking oscillator, load strobe amplifier and unload strobe amplifier.

4-78. Diodes CR12, CR13 and resistor R17 at the sync inputs of the strobe generator comprise a positive OR gate. The output of the OR gate is either at -5 volts or +5 volts, depending on the input levels. When there is no load or unload sync pulse, the OR gate output is at -5 volts. A positive pulse at either input raises the output level to +5 volts, triggering delay blocking oscillator Q4 through C6 and CR11. Operation of the delay blocking oscillator is similar to that of the blocking oscillators of the two phase driver (Paragraph 4-27). Resistor R9 is a temperature sensitive sensistor with a positive coefficient. It keeps the pulse width of the delay blocking oscillator pulse constant in spite of temperature changes by maintaining a constant L/R ratio. Zener diode CR1 maintains a constant voltage drop from terminal 3 of T1 to ground. Potentiometer R14 is used to adjust the delay pulse width.

4-79. A positive pulse is produced at the collector of Q4 during the delay blocking oscillator cycle. The trailing edge of this pulse has a steep negative excursion which is caused by the collapsing magnetic field about T1 at the end of the cycle. The negative spike causes CR7 to conduct and a negative pulse is coupled through R12 and C2 to the base of delay amplifier Q1. Transistor Q1 conducts for a short time and a positive pulse is coupled from the Q1 collector to C3 and C10 in parallel.

4-80. Capacitor C3, resistor R11 and diode CR8 comprise a pulse gate at the input to load strobe blocking oscillator Q2. Operation of the pulse gate is such that a positive pulse appears at the pulse gate output only when a pulse is applied to its input and the LU input is at +5 volts. When a character is being loaded into the buffer, the load-unload flip-flop of the input sync amplifier is switched to the load state so that the LU input is at +5 volts. This results in a positive pulse at the emitter of load strobe blocking oscillator Q2 when the pulse from Q1 is applied to pulse gate C3-R11-CR8. Blocking oscillator Q2 is thus triggered during the load operation. When it is triggered, a negative pulse at terminal 4 of T2 is inverted by load strobe amplifier Q3 and used to gate the load coincident current detector. Load strobe blocking oscillator Q2 cannot be triggered

during an unload operation because the load-unload flip-flop level is low at this time.

4-81. Capacitor C10, resistor R22 and diode CR15 comprise a similar pulse gate at the input to unload strobe blocking oscillator Q5. When a character is being unloaded from the buffer, the $\overline{LU}$ input to this pulse gate is high and a pulse from Q1 results in the triggering of unload strobe blocking oscillator Q5. Unload strobe amplifier Q6 inverts and amplifies the pulse from Q5. The unload strobe pulse from Q6 is used to gate the unload coincident current detector and the read amplifiers. Unload strobe blocking oscillator Q5 cannot be triggered during a load operation because the $\overline{LU}$ input level is at -5 volts only during a load cycle.

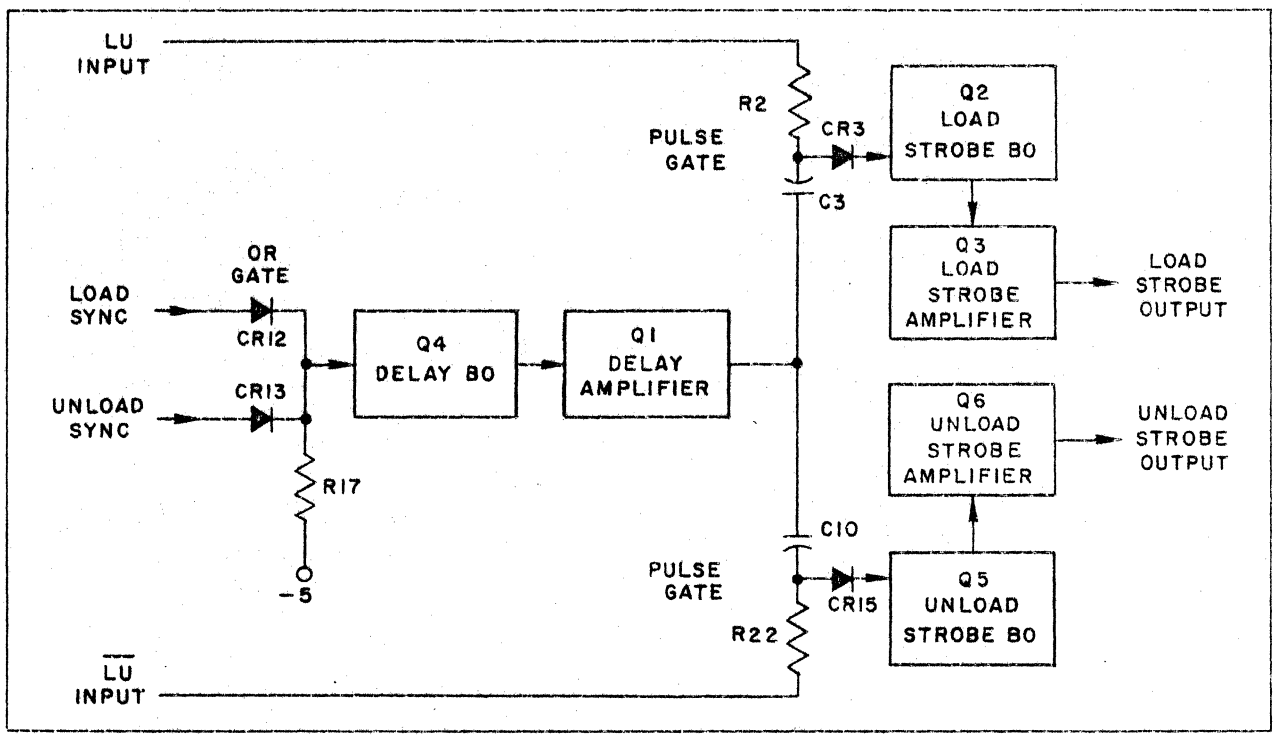


Figure 4-10. Strobe Generator, Functional Block Diagram

4-82. ELECTRONIC CLEAR CIRCUITS. (See Figure 4-11).

4-83. GENERAL. The electronic clear circuit card contains a magnetic switch clear blocking oscillator and a matrix clear blocking oscillator. The circuit card contains two inputs;

switch clear and master clear.

4-84. In the BA buffers, a switch clear input pulse triggers the switch clear blocking oscillator and results in an output pulse which clears the magnetic switch to its initial state. A master clear input pulse triggers both blocking oscillators and results in two simultaneous output pulses which reset both the magnetic switch and the matrix.

4-85. In the 144-BQ-4A and 144-BQ-8A buffers, only the master clear input is used. The master clear pulse resets the matrix and both magnetic switches.

4-86. MAGNETIC SWITCH CLEAR. (See Figure 6-10). The magnetic switch clear circuits consist of input amplifier Q5, blocking oscillator Q1 and output pulse amplifier Q4. Amplifier Q5 is normally conducting but is cut off by either a positive pulse at input B-1 or a negative pulse at input B-2. The amplifier accomodates either positive or negative clear pulses depending on whether jumper W3 or jumper W4 is connected (refer to Paragraph 1-27). When Q5 is cut off, a positive pulse is coupled from the Q5 collector through C7 and CR9 to the emitter of magnetic switch clear blocking oscillator Q1. The operation of this blocking oscillator is similar to that of the two phase driver blocking oscillators (Paragraph 4-27). Diode CR4 normally conducts through R2 and R14, maintaining a base bias which keeps Q1 conducting near cutoff. When Q1 is triggered by the positive pulse from CR9, CR4 becomes reverse biased and the Q1 base is maintained at a +1.5 volt potential while a positive pulse is produced at the Q1 emitter. Resistor R9 and potentiometer R8 in series with the feedback winding of T1 determine the width of the Q1 blocking oscillator pulse.

4-87. A negative pulse is coupled through C4 to the base of magnetic switch clear amplifier Q4. The pulse turns Q4 on so that current flows through Q4 and the magnetic switch clear windings in series. A pulse from the Q4 collector is used to reset the load-unload flip-flop of the input sync amplifier.

4-88. MASTER CLEAR. A master clear pulse from the external equipment is amplified by transistors Q2 and Q3 and utilized to trigger blocking oscillators Q1 and Q6 simultaneously. When the blocking oscillators are triggered, Q1 clears the magnetic switch circuitry (as in Paragraph 4-80) while Q6 clears the storage matrix. Jumpers are incorporated in the Q2 input circuits to

permit the use of positive or negative master clear pulses (as in the case of Q5, Paragraph 4-86).

4-89. The amplified master clear pulse is coupled from the collector of Q3 through C3 to CR5 and CR16 in parallel. Diodes CR5 and CR16 conduct simultaneously on receipt of the positive pulse, triggering both blocking oscillators. The Q6 blocking oscillator pulse turns on transistor Q7 which conducts through the matrix clear windings. Potentiometer R26 is used to adjust the width of the pulse from blocking oscillator Q6.

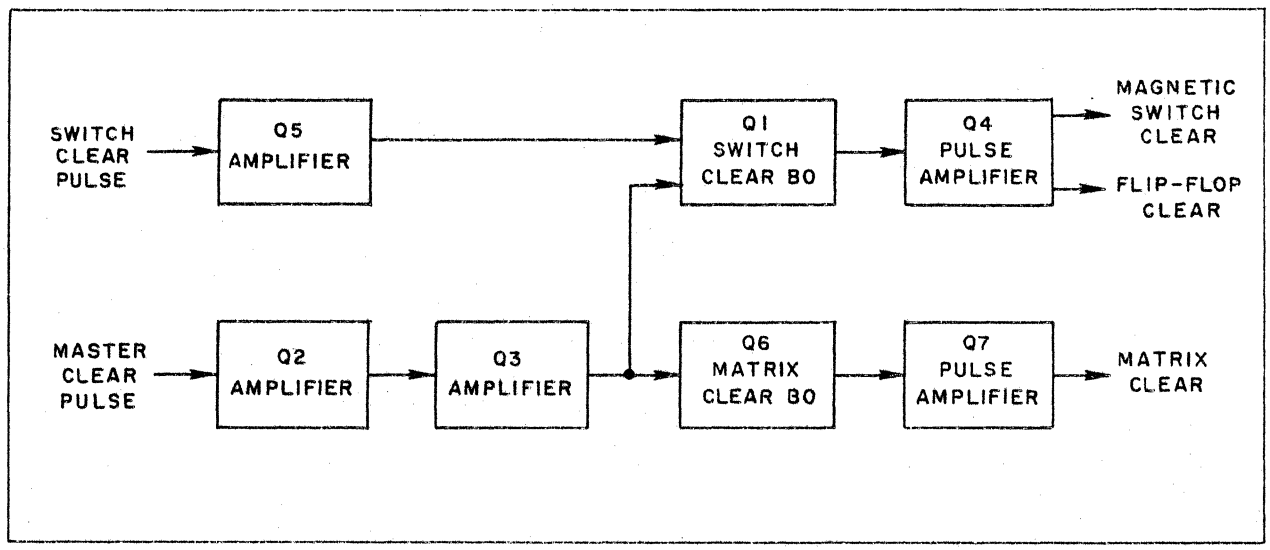


Figure 4-11. Electronic Clear Circuits, Block Diagram

4-90. COINCIDENT CURRENT DETECTORS. (See Figure 6-11).

4-91. The coincident current detector printed circuit card contains two coincident current detectors. Each of the detectors operates to produce a marker pulse in synchronization with either the loading of a character or the unloading of a character at a particular address.

4-92. In 144-BQ buffers the load coincident current detector utilizes signals from the load magnetic switch to produce a load address marker and the unload coincident current detector utilizes signals from the unload magnetic switch to produce an unload address marker. In the 144-BA buffers both coincident current detectors utilize signals from the same magnetic switch.

4-93. Transistors Q1, Q2 and Q3 comprise one coincident current detector and transistors Q4, Q5 and Q6 comprise the other. The primary winding of transformer T1 is connected across a one-ohm resistor which is in series with an X output drive line of the magnetic switch. The primary winding of T2 is connected across one-ohm resistor which is in series with a Y drive line. Whenever the two drive lines to which T1 and T2 are connected are pulsed simultaneously, Q1 and Q2 are driven into saturation and a negative pulse is coupled from the Q2 emitter to the base of Q3. Transistor Q3 can only conduct when the negative signal pulse is present at its base and the positive strobe pulse is present at its emitter. When these two pulses are present at Q3 in coincidence, the strobe pulse is produced at the Q3 collector.

4-94. If Q1, Q2 and Q3 are being used to produce a load marker pulse, the load strobe pulse is applied to the emitter of Q3. If they are being used to produce an unload strobe pulse, the unload strobe is applied to the Q3 emitter. The strobe pulse thus permits the marker pulse to be produced at the proper time.

4-95. The operation of coincident current detector Q4-Q5-Q6 is identical to that of coincident current detector Q1-Q2-Q3.

4-96. POWER SUPPLY. (See Figure 6-12).

4-97. GENERAL. The 100 to 130 volt a-c input is applied through filter FL1 and magnetic amplifier M/A1 to power transformer T1. The series magnetic amplifier regulates the input to T1. Two secondaries of T1 apply the regulated a-c to rectifiers which produce outputs of +24, +16, +7, -5, -14, -24, the PCS supply and an adjustable 7 volt supply to the circuit ground.

4-98. MAGNETIC AMPLIFIER. Since diodes CR6 and CR7 conduct on alternate half-cycles a d-c bias flows through gate windings 1-4 and 5-8. This current tends to saturate the magnetic amplifier cores. A down bias current developed by CR1 flows through down bias winding 2-3; this bias opposes the gate bias, preventing saturation. Thus when the line input is increased the down bias is also increased to limit the a-c in the T1 primary. When the line input decreases the down bias follows the drop allowing more a-c in the primary because the magnetic amplifier core is less saturated. An increase in load current is followed by an increase in gate bias current through the magnetic amplifier gate windings 1-4 and 5-8. This gate current moves the amplifier cores closer to saturation, and lowers the IR drop across the gate windings, to offset losses imposed by increased power supply loading.

4-99. DIFFERENCE AMPLIFIER. The difference amplifier consists of PNP transistors Q4 and Q5, and Zener diode CR12. The amplifier provides precision regulation and fine manual adjustment of the power supply +24 volt output. Positive 24 volts applied across CR12 and resistor R16 enables CR12 to hold the base of Q4 at a pre-determined voltage. Positive 24 volts is also applied across voltage divider R28, R21, R19 and a sample picked off and fed to the base of Q5 as a sense voltage. If the reference voltage at Q4 base and the sense voltage at Q5 base are equal, the two collector currents are equal and the difference amplifier does not provide correcting current to the 6-7 control winding. An increase in sense voltage at Q5 base will increase conduction thru Q5 collector and force a decrease in Q4 collector current, since the sum of these currents through the common emitter circuit must remain constant. Temperature compensation is achieved by the matched characteristics and common emitter circuit of Q4 and Q5.

4-100. D-C SUPPLIES. Rectifier CR8 developes the +5 and -5 volt outputs. Rectifier CR9 develops the -14, -24, +14, +16, +24 volt outputs and the PCS output. The -14 volt output is regulated by difference amplifier Q7-Q8 and series regulator Q6. The operation of the difference amplifier Q7-Q8 is similar to that of Q4-Q5 (Paragraph 4-99). A control current from Q8 varies the base current of Q6, regulating the current through Q6 and Q9 and maintaining a constant -14 volt output. Diodes CR10, CR11, CR13, CR14 and CR15 stabilize the potential at the Q7 base. Potentiometer R26 supplies the sample voltage to Q8 and is used to set the -14 volt output level. Sensistor R31 (temperature sensitive resistor) has a positive coefficient of temperature. It varies the Q8 bias with variations in temperature so that the -14 volt output becomes less negative with an increase in temperature. The -14 volt output is compensated in order to obtain optimum inhibit current from the digit drivers and optimum clear current from the electronic clear circuits under various temperatures. CR16, Zener diode regulates the +16v output.

4-101. Rectifier CR2 develops the adjustable d-c output which is used to vary the potential of the circuit ground (Paragraph 4-102). The 7-volt d-c output is regulated by difference amplifier Q2-Q3 and series regulator Q1. Operation of these regulator circuits is similar to that of the -14 volt

regulator (Paragraph 4-100), but the seven volt supply does not vary with the ambient temperature.

4-102. CIRCUIT GROUND. (See Figure 4-12). Terminal A of TB5 is the circuit ground terminal. Either the positive output terminal, B, or the negative output terminal, C, of the adjustable supply is connected to terminal A. The ground line of the external equipment is connected to the other output terminal of the adjustable supply. Terminal A is therefore shifted to either +7 volts or -7 volts with respect to the ground line of the external equipment when the 7 volt supply produces its full 7 volt output. Potentiometer R4 is used to vary the output from 0.5 to 7 volts. The circuit ground (terminal A) can therefore be set to any level within ±7 volts with respect to the chassis ground, depending on the setting of R4 and on how the 7 volt output is connected.

4-103. All operating voltages of the buffer are returned to the circuit ground, and signal levels within the buffer are referenced to the circuit ground. A signal level which is at a voltage E with respect to the chassis ground is at a level E + V with respect to the circuit ground, when the output of the adjustable supply is equal to V. Since either the positive or negative output can be connected to the chassis ground and since the adjustable output can be varied from 0.5 to 7 volts, E + V may be made to equal to any level from E + 7 to E - 7. This means that a signal level from the external equipment may be shifted to any level within ±7 volts of the buffer ground.

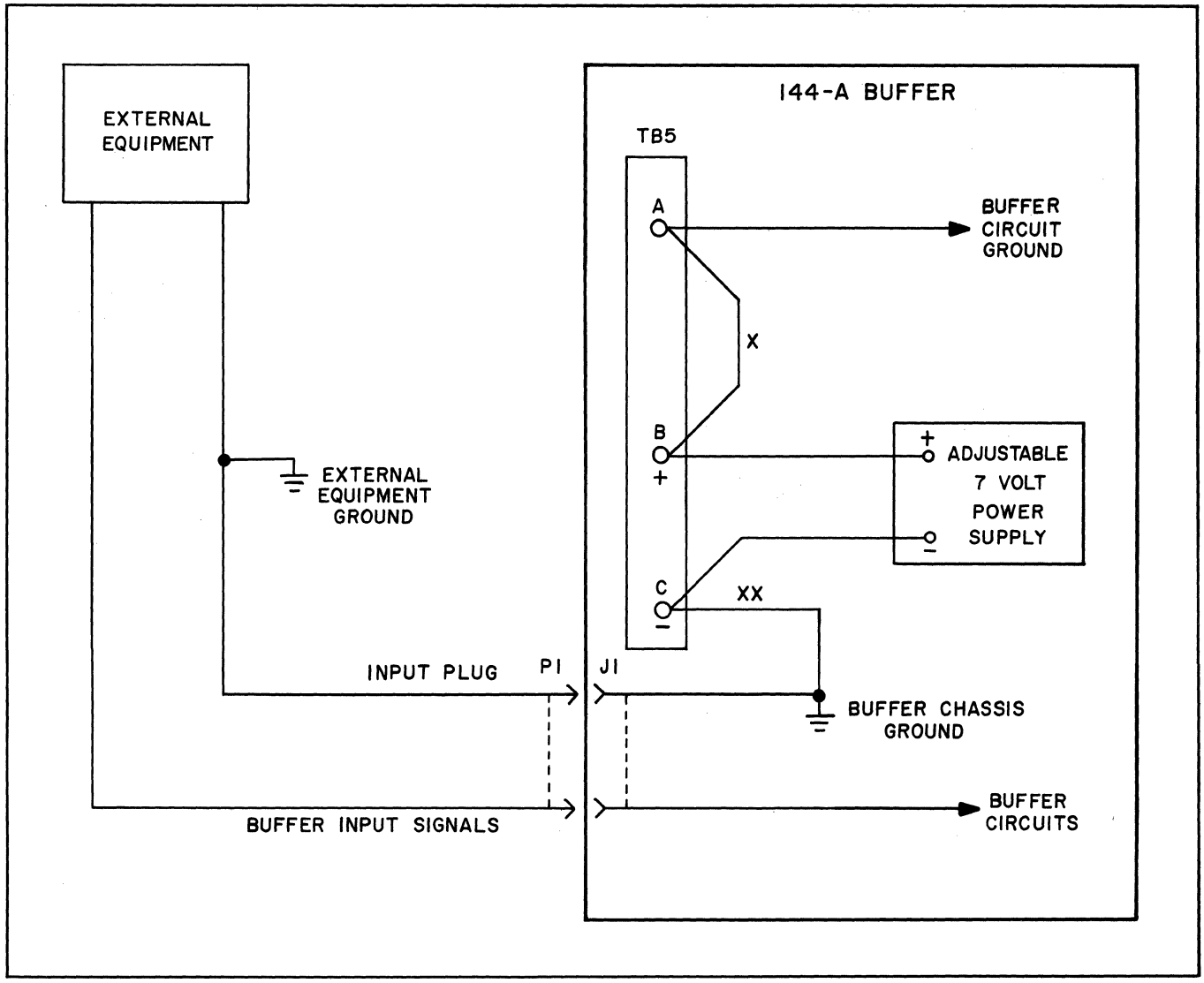


Figure 4-12. Level Shifting By Means of the Circuit Ground

NOTE

TB5 shown wired for a positive midpoint on the information signal swing. For a negative midpoint on the information signal swing; remove wire X from A to B, remove wire XX from C to chassis ground, install wire X from A to C, install wire XX from B chassis ground.

SECTION V

MAINTENANCE

5-1. GENERAL.

5-2. This section contains maintenance instructions for the 144-A Core Buffer Memories. Test equipment required, testing, trouble shooting techniques and repair procedures are included.

5-3. TEST EQUIPMENT.

5-4. Table 5-1 lists the test equipment required to service the buffer.

TABLE 5-1. TEST EQUIPMENT REQUIRED

Item	Characteristics
1. Oscilloscope	Tektronix Inc. Type 531, 541 or equivalent
2. Multimeter	Simpson 260 or equivalent
3. Information Source	Refer to Paragraph 5-9.
4. Sync Pulse Source	Refer to Paragraphs 5-8, 5-10 & 5-11.
5. Clear Pulse Source	Refer to Paragraphs 5-8, 5-10 & 5-11.
6. Variable a-c Power Source	A variac or equivalent
7. Breaker Key	To be used in series with the variac to break up the a-c power to the buffer
8. Alligator Clips	Mueller Electric Co. Mini-Gator No. 30 with No. 32 sleeve or equivalent; to be used with meters and scope at printed circuit card terminals
9. Thermometer	Centigrade Scale
10. Extender Card	TM Part No. 8002-5-128

5-5. MECHANICAL INTEGRITY.

5-6. Make certain that mechanical connections are secure before employing more advanced trouble shooting procedures. Check that the nuts and bolts which secure the connectors are not loose, that the unit is not physically damaged and that no wires have been accidentally torn from the buffer. Make sure that all printed circuit cards are firmly inserted in the card cage connectors.

5-7. TESTING.

5-8. TEST SETUP. (See Figure 5-1). Figure 5-1 shows how the clear pulse, sync pulse and information sources mentioned in Table 5-1 are used. The sync and clear pulse sources must be capable of producing the sync and clear pulses specified in Paragraph 1-27. The switch clear pulse output of the clear pulse source is needed only for the 144-BA buffers. The test setup shown in Figure 5-1 will permit the maintenance of one buffer while a replacement is on the line.

CAUTION

The buffer contains an external equipment (chassis) ground and a floating (buffer circuit) ground as described in Paragraph 4-102. Do not short the two ground terminals. The circuit ground adjustable power supply will be short circuited if this is done.

5-9. INFORMATION LEVELS. Either the +1.5 volt or the -1.5 volt level shown in Figure 5-1 may signify a binary ONE, depending on the coding of the information inputs for the buffer under test. To determine which level signifies a binary ONE, consider the information coding of the data processing equipment which feeds information to the buffer. If the high level from the external equipment signifies a binary ONE, then the +1.5 volt level of Figure 5-1 is the binary ONE. If the low level from the external equipment signifies a ONE, then the -1.5 volt level of Figure 5-1 is the binary ONE.

NOTE

The +1.5 volt and the -1.5 volt information levels of Figure 5-1 are with respect to the buffer circuit ground. The clear pulse and the sync pulse levels of the test set-up are also referenced to the circuit ground. Be sure to connect the ground line of the information source, the sync pulse source and the clear pulse source to the circuit ground which is located at terminal A of the power supply terminal board.

5-10. PULSE SOURCES. It is suggested that both the load sync pulses and the unload sync pulses from the sync pulse source be spaced 40 microseconds apart and that they be 180 degress out of phase. For both the 144-BQ-4A and the 144-BQ-8A buffers, the master clear pulse should be timed so as to occur twenty microseconds after the 144th load sync pulse. With this arrangement, a trouble at any of the 144 addresses can be observed.

5-11. In the case of the 144-BA-4A and 144-BA-8A buffers, the magnetic switch clear pulse should occur twenty microseconds after the 144th load sync pulse. The master clear pulse should occur twenty microseconds after the 144th unload sync pulse.

5-12. FUNCTIONAL TEST (BQ BUFFERS). Test the operation of the 144-BQ-4A and 144-BQ-8A buffers as follows:

(a) Place Switch S3 in the position which supplies a binary ONE information level to the buffer inputs.

(b) Apply the clear and sync pulses to the buffer as instructed in Paragraph 5-10.

(c) Feed information to each input by means of S4 and observe each buffer output on the oscilloscope. Each output should produce a continuous train of binary ONE pulses.

(d) Place switch S3 in the other position. The buffer outputs should now be all ZEROs.

(e) Check the clearing of the buffer by applying a (200 us min period)train of master clear pulses to the buffer. Oscilloscope checks at the electronic clear outputs (19-B, 19-E,19-X) should show the waveforms of Table 5-3, Steps 5, 6 and 7.

5-13. FUNCTIONAL TEST. (BA BUFFERS). Test the operation of the 144-A Buffers as follows:

(a) Place switch S3 in the position which supplies a binary ONE information level to the buffer inputs.

(b) Apply the clear and sync pulses to the buffer as described in Paragraph 5-12.

(c) Feed information to each buffer input by means of S4 and observe each output on the oscilloscope. Each output should produce a continuous train of binary ONE pulses.

(d) Place switch S3 in the other position. The buffer outputs should now be all ZEROs.

(e) Check the clearing of the magnetic switch by applying a continuous train of magnetic switch clear pulses to the buffer (100us min. Pulse Period). Electronic clear output (19-B) should indicate the waveform shown in Table 5-3, Step 5.

(f) Check the master clear operation by applying a continuous train of master clear pulses to the buffer. The electronic clear output (19-B, 19-E, 19-X) should conform to Table 5-3, Steps 5 , 6 and 7.

5-14. VOLTAGE AND CURRENT CHECKS. (See Figure 5-2). Power supply output voltages should be measured every thirty days. With the exception of the -14 volt output, all voltages should be within 5% of the rated values which are shown on the rear of the power supply. Use a voltmeter which has been calibrated to an accuracy of 1% for the voltage measurements. If necessary, adjust the power supply outputs by means of the adjustment controls which are located at the rear of the power supply.

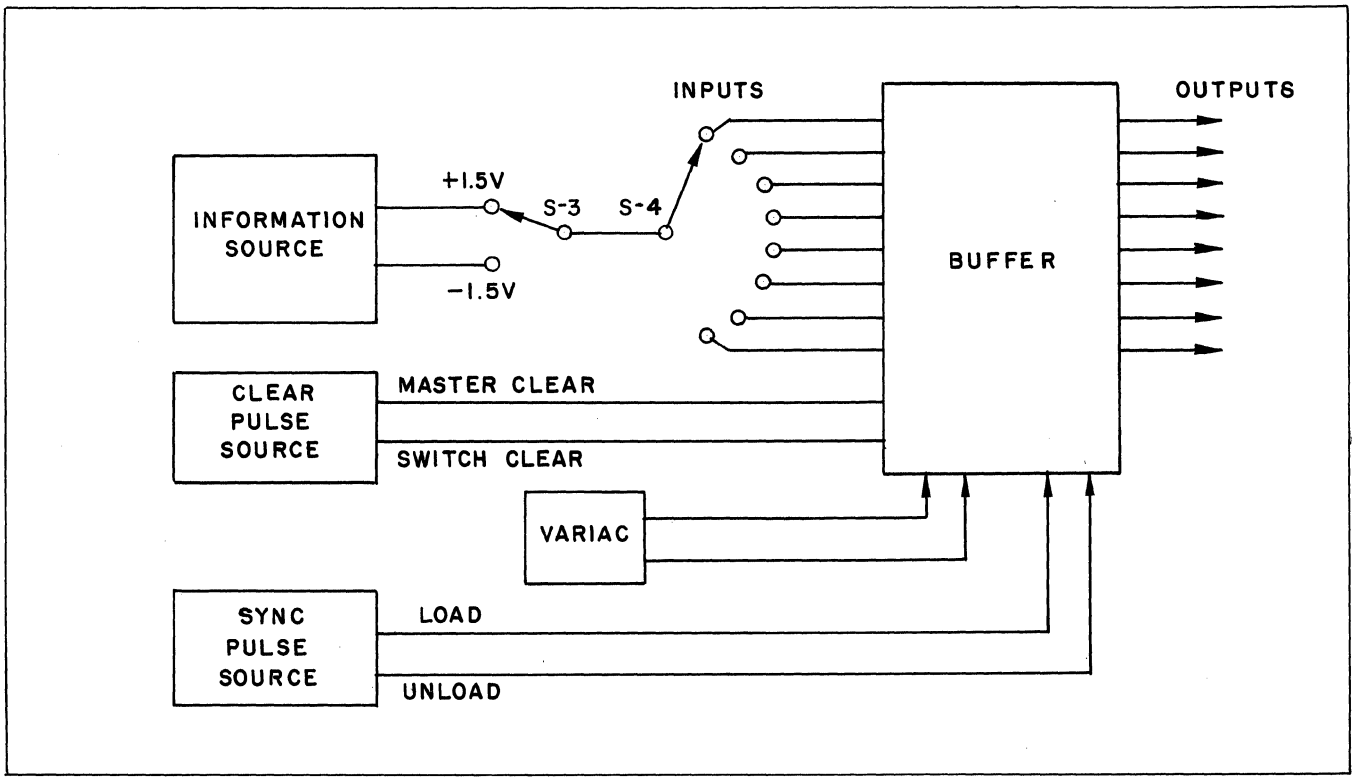


Figure 5-1. Test Setup

NOTE

Do not measure the power supply outputs with respect to the chassis ground. Measure them with respect to terminal A of the power supply output terminal board (buffer circuit ground). The PCS, +5 volt, -5 volt, +24 volt, and -24 volt outputs are affected if any output control is adjusted. Always check all voltages after adjustments.

5-15. MINUS 14 VOLT OUTPUT. The -14 volt output varies automatically with the ambient temperature of the buffer. Determine the proper output level by means of the -14 volt calibration chart, Figure 5-3. The -14 volt supply is used to drive the inhibit windings and is in direct opposition to, and precisely one half the intensity of the PCS current.

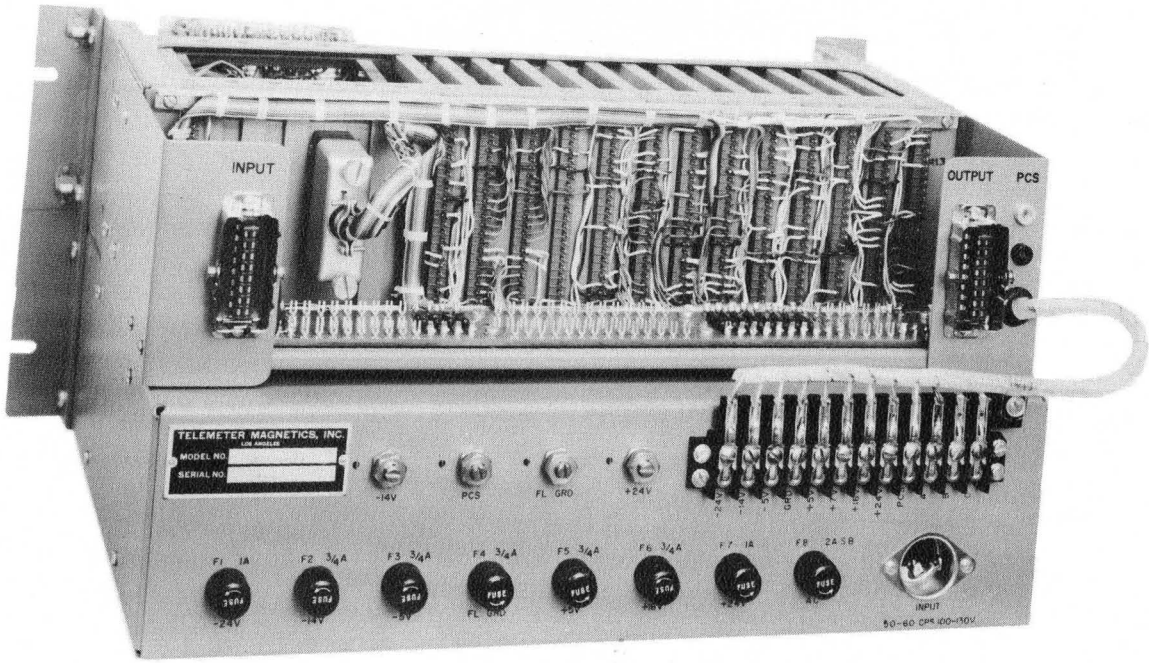


Figure 5-2. Power Supply Controls

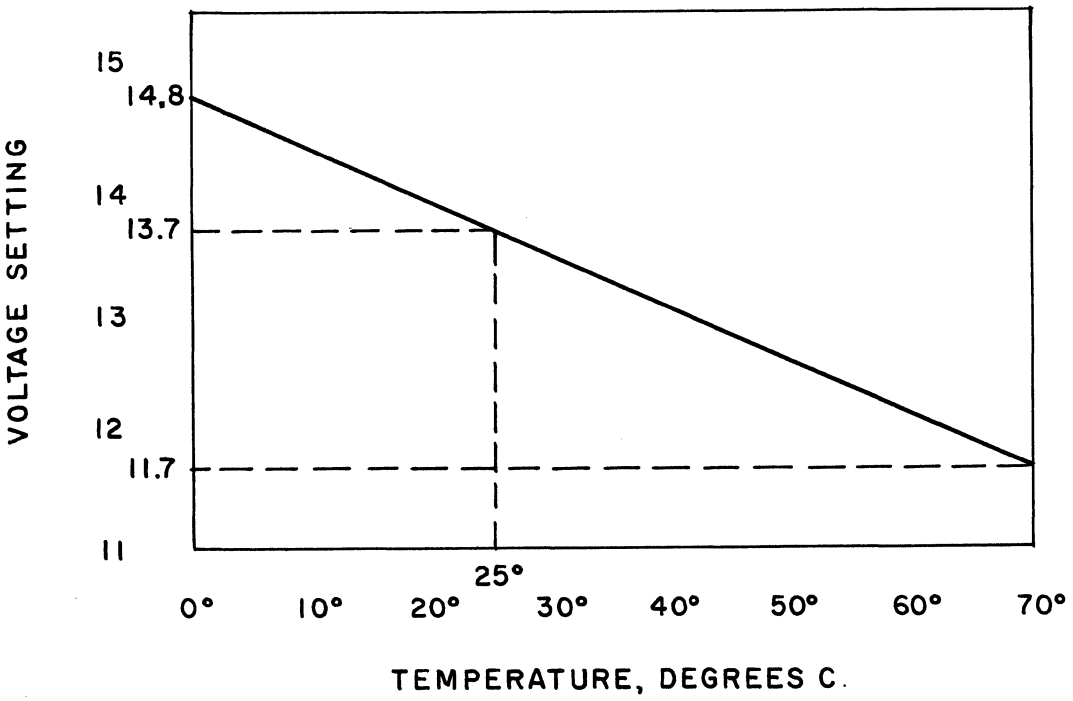


Figure 5-3. Calibration Chart For -14 Volt Output

5-16. BUFFER CIRCUIT GROUND. (Refer to Paragraph 4-102 and Figures 4-12 and 5-2). The buffer circuit ground (terminal A of the power supply terminal board TB5) may be at either a positive or a negative potential with respect to the chassis ground. The circuit ground connections are factory wired to meet the requirements specified by the user.

5-17. The difference in potential between the buffer circuit ground and the chassis ground may be any voltage between 0.5 and 7.0 volts. Determine the proper setting of the CKT GRD SHIFT VOLTAGE (also called FL GRD on some early models) adjustment control as follows:

(a) Consider the coding of the information inputs to the buffer under test as the buffer is used with the data processing equipment. Ascertain the two information levels (ZERO and ONE).

(b) Determine the voltage level which is equivalent to the midpoint of the information voltage swing.

(c) If the midpoint voltage is a positive level, connect the voltmeter negative test lead to chassis ground and the positive test lead to terminal B of TB5, power supply terminal board. If the midpoint voltage is a negative level, connect the voltmeter positive test lead to chassis ground and the negative test lead to terminal C of TB5.

(d) Adjust the CKT GRD SHIFT VOLTAGE control at the rear of the power supply so that the voltmeter indicates a voltage which is equal to the midpoint of the voltage swing.

5-18. For example, if the buffer is used in an application where a zero volt level signifies a binary ZERO and a puls six volt level signifies a ONE, the proper setting of the floating ground potential is determined as follows:

(a) The midpoint of the information voltage swing is +3 volts.

(b) The negative test lead of the voltmeter is connected to the chassis ground and the positive test lead to terminal B of the terminal board.

(c) The CKT GRD SHIFT VOLTAGE control is adjusted so that +3 volts is indicated on the voltmeter.

5-19. PCS CURRENT. Check the output current of the positive current stabilizer at the PCS test jacks which are located at the rear of the buffer. Connect the positive lead of the milliammeter to the orange jack and the negative load to the black one. The PCS current varies automatically with the ambient temperature. Determine the proper PCS current by means of the chart shown in Figure 5-4.

5-20. A-C INPUT TESTS.

5-21. A-C VOLTAGE TEST. Check that the buffer operates with the proper a-c input voltage range as follows:

(a) Set the variac to an output of ZERO volts.

(b) Slowly increase the output voltage of the variac. The buffer must begin to operate normally by the time that the variac output reaches 100 volts.

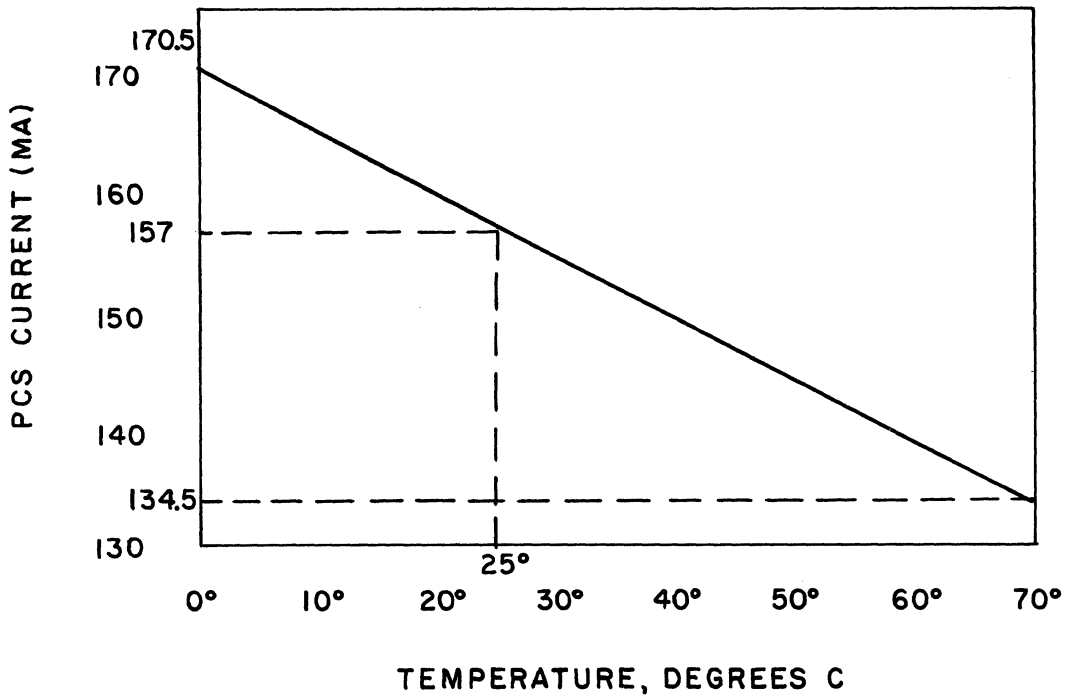


Figure 5-4. Calibration Chart For PCS Adjustment

(c) Continue to raise the a-c output of the variac. The buffer must operate normally within the range from 100 to 130 volts.

CAUTION

Do not raise the buffer input voltage higher than 130 volts.

5-22. TROUBLE SHOOTING.

5-23. GENERAL. Table 5-2 isolates troubles to general areas of the buffer and table 5-3 isolates troubles to specific circuits. Paragraphs 5-24 through 5-28 contain general trouble-shooting instructions.

5-24. When trouble occurs, first check that the a-c power input to the buffer is correct. Next, check that the power supply outputs and the PCS output are correct. Thirdly, check that

the printed circuit cards are all firmly inserted in the card cage connectors. If trouble occurs frequently, or if the buffer has not been used for a long time, remove the printed circuit cards, one at a time, and check the circuit card and the card cage connector terminals for dirt, corrosion and damage. If necessary, clean the printed circuit card terminals as instructed in Paragraph 5-35.

CAUTION

1. Turn off the a-c power to the buffer before removing or inserting printed circuit cards. Failure to do this may result in damage to the circuit card, the power supply, or both.

2. When removing or inserting a card, rock the card up and down gently to facilitate the removal or insertion.

3. The printed circuit card and the card cage connectors are not keyed. Always insert the card so that the components are on the left hand side (as viewed from the front of the buffer). Be sure to insert cards in the proper positions.

5-25. LOCATION OF PRINTED CIRCUIT CARDS. Printed circuit cards are located in the card cage connector at positions which are designated with the numbers 1 through 19. In determining the numerical designation of a card cage connector, count from right to left while facing the front of the buffer. Figure 6-1, the functional block diagram, shows the location of each circuit in the right hand corner of each block. For example; the input sync amplifier bears the designation 18 in Figure 6-1 and it is located in position 18 of the card cage.

5-26. PRINTED CIRCUIT CARD PIN CONNECTIONS. The terminal designations of the printed circuit cards correspond with the terminals of the card-cage connector with which they make contact. Terminal designations are visible at both the receptacle and the wiring side of the card cage connectors.

5-27. PRELIMINARY TROUBLE SHOOTING. If the buffer continues to malfunction after the instructions of Paragraphs 5-1 through 5-26 have been carried out and the power supply outputs

are normal, use the extender card and check that all operating voltages are present at the printed circuit cards (Refer to Table 5-3). If all voltages are present, replace suspected cards with spares.

CAUTION

Use the alligator clips specified in Table 5-1 when measuring voltages or observing waveforms at the card cage connectors. Avoid shorting adjacent connector terminals. Shorting the terminals may damage the circuit card or the power supply

5-28. SIGNAL TRACING. Table 5-3 shows signal waveforms at the inputs and outputs of the buffer and of each printed circuit card. With the exception of the clear pulses, all waveform photographs were taken with the buffer operating at the rate of 10 kc. In general, the waveform checks apply to all 144-A Core Buffer Memories. Where the waveform differs for applicable buffers of the series, the applicable buffer is specified.

CAUTION

The oscilloscope signal ground lead and the oscilloscope sync ground lead must be connected to the circuit ground when observing waveforms. Dissimilar sync and signal grounds will short out the adjustable 7 volt power supply (See Figure 4-12).

5-29. NOISE PROBLEMS.

5-30. Isolate the noise source by first loading and unloading the buffer in the data system with which it is used and then in the test setup of Figure 5-1. Noise is indicated by the presence of random spikes or intermittant grass on the oscilloscope patterns. The most frequent causes of noise are inductive and capacitive pickup from an external source adjacent to the buffer load lines.

5-31. When the noise is definitely traced to the buffer, the noise source may be a loose buffer connection or an intermittent component. Observe the oscilloscope patterns while gently tapping connections and components with a light rubber hammer or pencil eraser. If the noise indication is effected either favorably or adversely by tapping a particular component, replace that component and check for dirty terminal contacts. Examine suspect cards for dirty contacts. To isolate the noise source, substitute one printed circuit card at a time until the trouble disappears. Repair defective card in accordance with Paragraphs 5-34 thru 5-40.

5-32. PRINTED CIRCUIT CARD REPLACEMENT.

5-33a. With three noted exceptions, replacement printed circuit cards may be installed in the buffer without re-adjusting circuit parameters. The electronic clear card, the two phase driver card, and the strobe generator card must be adjusted when installed as a replacement for a defective unit.

5-33b. STROBE GENERATOR. (Refer to Table 5-3 and Figure 6-9). The strobe generator must be timed with potentiometer R14 so that the strobe pulse will enable the read amplifier during the exact peak of the core turnover signal. Table 5-3, Step 24 indicates waveform and test point.

5-33c. TWO PHASE DRIVER. (Refer to Table 5-3 and Figure 6-3). Each two phase driver card contains two blocking oscillators, Q1 and Q2; each BO should be adjusted for a 5.5 us pulse period, i.e., the leading edge of a negative pulse must occur precisely 5.5 us after the leading edge of a positive pulse. Table 5-3, Steps 13-15, indicates the proper waveform and test points for this adjustment. To modify the Q1 output on Pin J, resistor R1 may be shunted, C to D, to lengthen the pulse period. An added resistor, A to B, in series with R1 will shorten the pulse period. The Q2 output on Pin P may be similarly modified by adding to, or decreasing, the resistance of resistor R2. Sixty ohms is representative of the series resistance required to shorten the pulse period.

5-33d. ELECTRONIC CLEAR. (Refer to Table 5-3 and Figure 6-10). Potentiometer R8 should be used to adjust the switch clear output for 8 us pulse width at Pin X. Potentiometer R26 should be used to adjust the matrix clear output for a 15 us pulse width at Pin B.

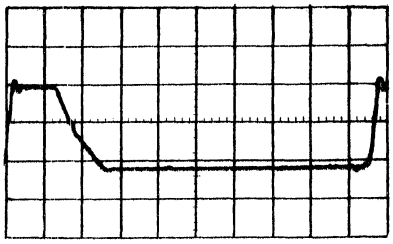
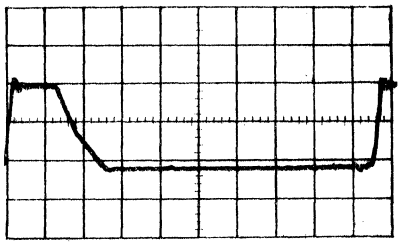
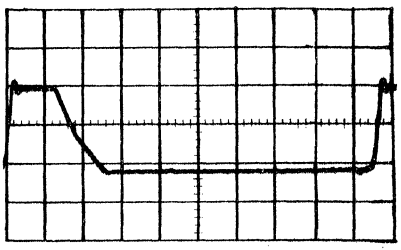
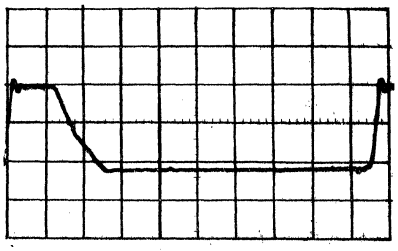
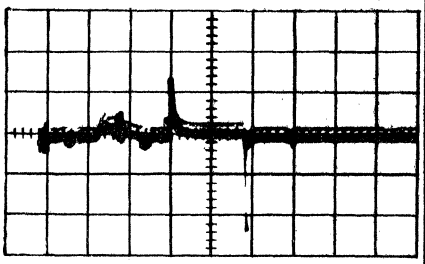
TABLE 5-2. GENERAL TROUBLE SHOOTING

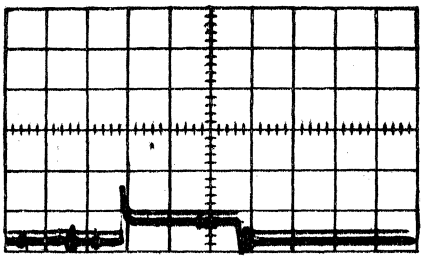
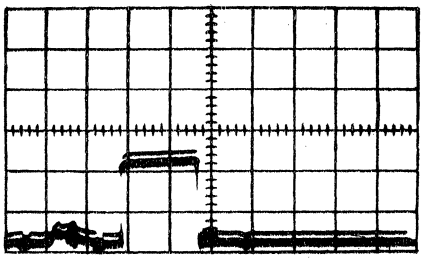
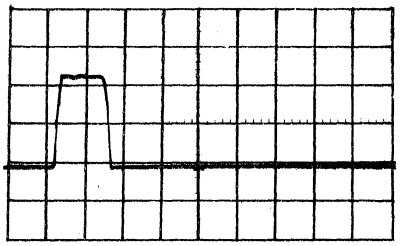
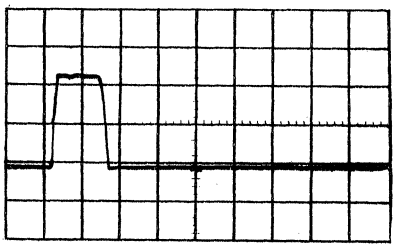
Trouble	Probable Cause	Remedy
1. Equipment does not turn on	a. Input fuse F4 blown	a. Replace Fuse
	b. Faulty power connection	b. Check connection at J1
2. Equipment turns on but does not operate	a. Incorrect operating power	a. Check that buffer is receiving 115 ±15 volts a-c at 60 cps.
	b. Blown power supply fuse or fuses	b. Replace necessary fuses.
		c. (Refer to Figure 6-12.)
3. Erratic information outputs.	a. Sync pulses do not meet the requirements of Paragraph 1-27.	a. Repair sync pulse source
	b. Noise trouble	b. Refer to Paragraph 5-29.
4. Incorrect outputs		
a. All ZEROs	a1. No unload strobe at read amplifiers	a1. Check strobe generator (Table 5-3, Step 16).
	a2. No unload matrix drive current.	a2. Check operation of load & unload 2 phase drivers (Table 5-3, steps 13-15)
	a3. No inhibit current (BA only)	a3. Check PCS current, Check input sync amplifier (Table 5-3 & Paragraph 5-18)

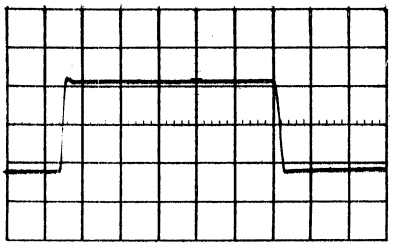
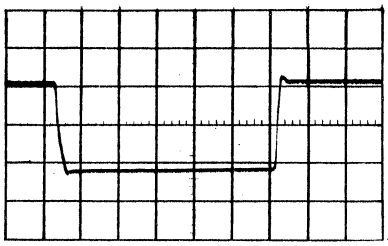
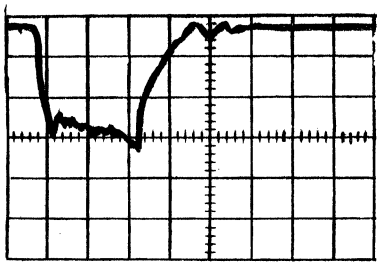
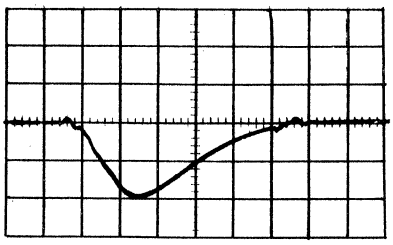
Trouble	Probable Cause	Remedy
	a4. Wrong $\overline{LU}$ level at digit drivers (BQ only)	a4. Check input sync amplifier (Table 5-3, Step 11).
b. All ONEs.	b1. Incorrect LU level at digit drivers (BA only)	b1. Check input sync amplifier (Table 5-3, Step 10).
	b2. Overflow of unload sync pulses; buffer is empty (BQ only)	
c. Garbled information	c1. Matrix is not being cleared	c1. Check electronic clear circuit (Table 5-3, Steps 5 and 6).
	c2. Magnetic switches not being cleared.	c2. Check electronic clear circuit.(Table 5-3, Steps 5 and 6. Check PCS current (Paragraph 5-18).
	c3. Load 2 phase driver or unload 2 phase driver not operating correctly.	c3. Check 2 phase driver output (Table 5-3, Steps 13 thru 15).

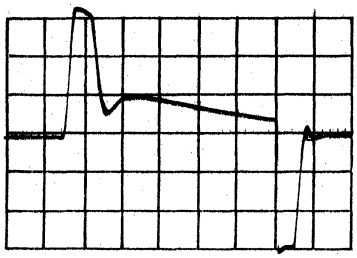
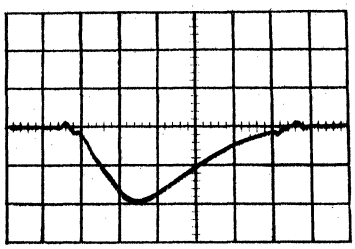
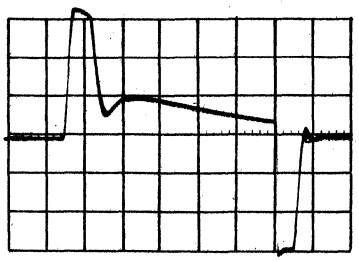
NOTE

Always begin troubleshooting procedures by checking power supply voltages.

Step	Description	Waveform	If Waveform is Abnormal
1.	Magnetic switch clear input. (BA only). EC-B at 19-A or 19-L; 5 volts/cm, 2 us/cm. Positive pulse at L or negative pulse at A.		Check switch clear pulse source.
2.	Master clear input. EC-B at 19-P or 19-Y; 5 volts/cm, 2 us/cm. Positive pulse at P or negative pulse at Y.		Check master clear pulse source.
3.	Load sync input. ISA at 18-A or 18-B; 5 volts/cm, 2 us/cm. Positive pulse at A, negative pulse at B.		Check load sync pulse source.
4.	Unload sync input. ISA at 18-X or 18-Y; 5 volts/cm, 2 us/cm. Positive pulse at Y or negative pulse at X.		Check unload sync pulse source.
5.	Magnetic switch clear output. Continues clearing at 100 us min. pulse period. Adjust R8 for a 8 us pulse width between spikes.		Replace or repair EC-B card.

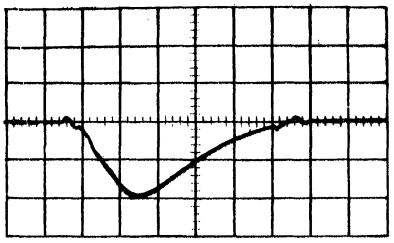
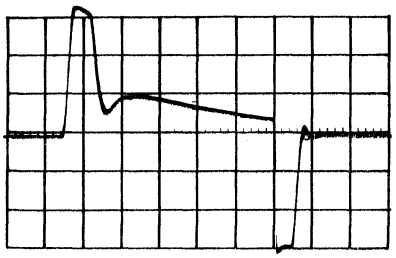
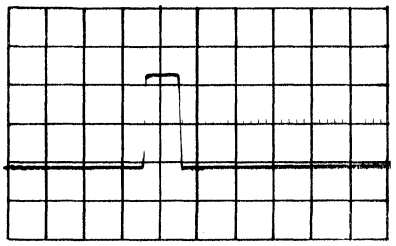
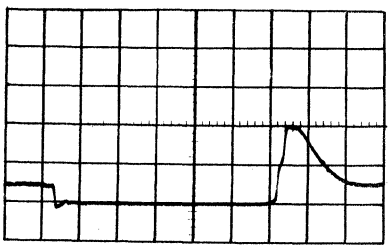
Step	Description	Waveform	If Waveform is Abnormal
6.	Matrix clear output. Continuous Clearing at 200 us min. pulse period. EC-B at 19-B; 5V/cm, 5 us/cm. Leading and trailing edges show positive & negative overshoot. Adjust R26 for a 15 us pulse width.		Replace or repair EC-B card.
7.	Clear output for 2 phase driver. EC-B at 19-E; 5 V/cm, 5 us/cm.		Replace or repair EC-B card.
8.	Delayed load sync. ISA at 18-M; 5V/cm, 1 us/cm.		Replace or repair input sync amplifier.
9.	Delayed Unload sync. ISA at 18-R; 5V/cm, 1 us/cm.		Replace or repair input sync amplifier.

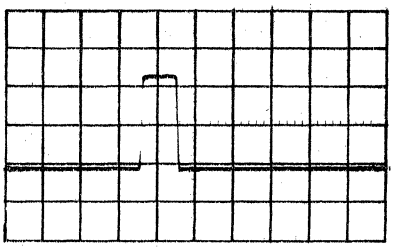
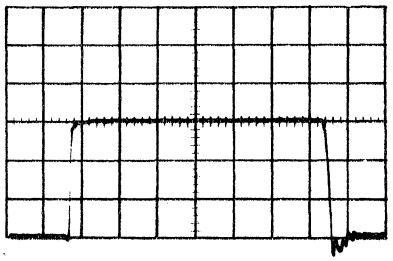
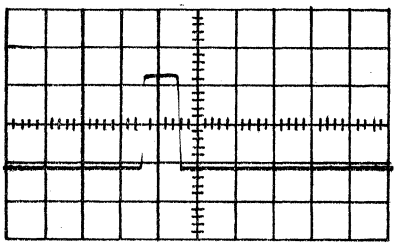
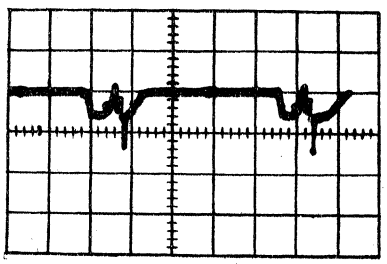
Step	Description	Waveform	If Waveform is Abnormal
10.	Load-Unload Flip-Flop output (LU level) during load cycle. ISA at 18-L; 5 volts/cm, 1 us/cm		Replace or repair input sync amplifier
11.	Load-Unload Flip-Flop output (LU level) during load cycle. ISA at 18-S; 5 volts/cm, 1 us/cm		Replace or repair input sync amplifier
12.	PCS output during load or unload cycle. PCS at 17-H; 5 volts /cm, 2 us/cm.		Replace or repair PCS.
13.	Load 2 phase driver output during load cycle. Load 2 phase driver at 15-P; 5v/cm 1 us/cm. Waveforms at 15-P and 15-J may trade positions or appear simultaneously, depending on type of scope sync (odd or even).		Replace or repair load 2 phase driver

Step	Description	Waveform	If Waveform is Abnormal
13. (Cont.)	Load 2 phase driver output during load cycle. Load 2 phase driver at 15-J; 5 V/cm, 1 us/cm. Waveforms at 15-J & 15-P may trade positions or appear simultaneously, depending on type of scope sync (odd or even).		Replace or repair PCS.
14.	(BA Buffers only) Load 2 phase driver output during unload cycle. Load 2 phase driver at 15-J; 5v/cm, 1 us/cm. Waveforms at 15-J & 15-P may trade positions appear simultaneously depending on type of scope sync (odd or even).		Replace or repair load 2 phase driver
	Load 2 phase driver output during unload cycle. Load 2 phase driver at 15-P; 5v/cm, 1 us/cm. Waveforms at 15-P & 15-J may trade positions or appear simultaneously.		Replace or repair load 2 phase driver

NOTE

The hump at the trailing edge of the positive pulse in Steps 13-15 is due to feedback from core turnover signals. Absence of hump on an otherwise normal drive pulse indicates X or Y lines shorted or open.

Step	Description	Waveform	If Waveform is Abnormal
15.	(BQ Buffers only) Unload 2 phase driver output during unload cycle. Unload 2 phase driver at 16-J; 5V/cm, 1 us/cm. Waveforms at 16-J and 16-P may trade positions or appear simultaneously.		Replace or repair unload 2 phase driver.
	Unload 2 phase driver output during unload cycle. Unload 2 phase driver at 16-P; 5V/cm, 1 us/cm. Waveforms at 16-P and 16-J may trade positions or appear simultaneously, depending on type of scope sync (odd or even).		Replace or repair unload 2 phase driver.
16.	Unload strobe during unload cycle. Strobe generator at 11-J; 5 volts/cm, 1 us/cm.		Repair or replace strobe generator.
17.	Load-Unload flip-flop reset pulse. 2 phase driver at 15-D; 5 V/cm, 1 us/cm.		Replace or repair load 2 phase driver.

Step	Description	Waveform	If Waveform is Abnormal
18.	Information pulses at read amplifier outputs during unload cycle. Read amplifiers at pins 8-V, 8-W, 8-X 8-Y; pins 9-V, 9-W, 9-X, 9-Y. Scope at 5V/cm, 1 us/cm. Buffer load will vary pulse shape slightly.		Replace or repair read amplifiers.
19.	Digit driver output. All digit drivers at pins 13-A, 13-K, 13-P, 13-Z; pins 14-A, 14-K, 14-P, 14-Z. Scope at 5V/cm, 1us/cm.		Replace or repair digit driver.
20.	Load strobe during load cycle. Strobe generator at 11-E; 5V/cm, 1 us/cm. Pulse used only to drive coincident current detector (optional equipment).		Replace or repair strobe generator.
21.	Core turnover signal coincident with strobe pulse during unload cycle. All read amplifiers at base of Q3, Q5, Q8, Q11; 5V/cm, 1 us/cm. Strobe rises thru center of negative core signal.		Replace or repair read amplifier. Check strobe generator & adjust strobe timing for center of turnover signal if necessary.

5-34. HANDLING AND REPAIR OF PRINTED CIRCUIT CARDS.

5-35. HANDLING PROCEDURES. The printed circuit cards are designed to operate on very low power levels. As a result, the card contacts are sensitive to dirt, dust, moisture and corrosion. The cards should never be inserted into the buffer without cleaning. Cleaning the cards is accomplished as follows:

(a) Wipe each contact with a cloth moistened with tri-cloroethylene, or equivalent.

(b) Erase the thin film left by the cleaning fluid from each contact with a rubber eraser.

(c) Wipe the rubber particles left by the eraser from the contact with a dry, lint-free cloth.

(d) Remove any loose surface metal between contacts.

5-36. REPAIR PROCEDURES. The printed card circuits can be serviced easily using conventional shop practices. The most logical procedure is to check resistances on the cards with the aid of the schematics. Voltages normally applied to the cards through the back of the card cage can be found listed in Table

5-37. TRANSISTORS. There is usually more than one transistor of a given type on each printed circuit card. The transistors may therefore be checked by substitution or resistance comparison. The latter must be done carefully to avoid damaging the transistor with an ohmeter. Proceed as follows:

(a) Turn off the equipment and remove the questionable card.

(b) Check the emitter-collector resistance of the transistor in both directions (alternate ohmeter polarity) using the meter scale which will apply the least amount of current to the transistor and still provide a reading.

(c) Replace the transistor in accordance with Paragraph 5-40 when the readings differ by more than 15% of the values obtained for other transistors of the same type.

5-38. DIODES. Check diodes by comparing forward and back resistance of diodes suspected of faulty operation to that of one known to be good.

5-39. RESISTORS AND CAPACITORS. Check resistor and capacitor components by freeing one end of the component from the circuit and using an ohmeter in a conventional manner. A VTVM is required to check most of the small capacitors for opens by inducing a needle "kick".

CAUTION

Never apply VTVM probes to a circuit if the meter current may flow through a transistor.

5-40. COMPONENT REPLACEMENT. Replacing components on printed circuit cards presents problems not normally encountered in conventional electronic repair work. The following basic rules must always be observed:

(a) Use only top quality rosin core 60/40 solder equivalent to that required by Federal Specification QQ-S-571, Sn-60.

(b) Use a small, hot soldering iron and a heat sink to conduct heat away from other components while soldering. A large pair of pliers clamped to the wire being soldered will satisfy the heat sink requirement.

(c) Replace spaghetti which may have been removed from any wire during soldering.

(d) Clean the solder grommets thoroughly by shaking the printed card over a cloth immediately after the hot iron is removed.

(e) Insert leads of new components into and through the grommets, then solder from the printed circuit side of the card-never from the component side.

(f) Clip off excessive wire and examine the card carefully for excess solder and possible strings of spilled solder. Check for rosin deposits. Wipe the card clean with a dry lint-free cloth.

(g) Clean the terminals as instructed in Paragraph 5-35.

5-41. MAGNETIC STEPPING SWITCHES.

5-42. REPAIR PROCEDURES. When trouble is definitely traced to the magnetic stepping switches, remove, then check with the aid of Figures 5-5 and 6-4. If ohmeter continuity checks reveal no shorted or open wires, the trouble may be in the clamp card components shown in Figure 5-5. If the card components are not defective, trouble may be a defective solder joint.

5-43. Solder joints which have been opened may normally be repaired by holding an iron under the switch cards on the joint. In other circumstances, the cards may be bent gently back to uncover a hidden joint or defective component.

CAUTION

Bend the card slowly and no oftener than necessary.

5-44. Remember that identical magnetic switches are used in all 144-A Core Buffer memories. The operational differences depend on the directions of the matrix drive currents during the unload cycle. The directions of the drive currents, in turn, depend on the directions of the core windings within the matrix.

5-45. If the substitution procedure fails to disclose a bad switch, check for broken wires or parted connectors.

5-46. The switches are attached through split leaf connectors to the storage system. Occasionally, these connectors part to create an open circuit. Should this occur, bend the connectors gently together with a pair of pliers. After any work is done on the split leaf connectors, clean them carefully as explained for the printed circuit card contacts in Paragraph 5-35.

5-47. STORAGE SYSTEM.

5-48. CONTINUITY CHECKS. (See Figures 5-6 and 5-7). The storage system consists of small ferrite cores laced into four matrix planes by wires. Failures of the storage system are rare. However, the correct procedures for continuity checks are given below to enable maintenance personnel to logically eliminate the matrices as sources of trouble.

CAUTION

The matrices may be damaged by improper test procedures. Never move or touch a matrix wire during the following tests. Apply test probes only to the indicated terminals.

5-49. PREPARING THE MATRICES FOR CHECKS. Carefully remove the magnetic stepping switches from the matrices. Tag one switch corresponding to one set of split leaf connectors. Although the switches are interchangeable, the process of elimination is best accomplished with only one variable at a time.

5-50. Place the matrix frame face-down on a cloth so that plug P2 is located at the top of the magnetics assembly. (See Figure 5-5).

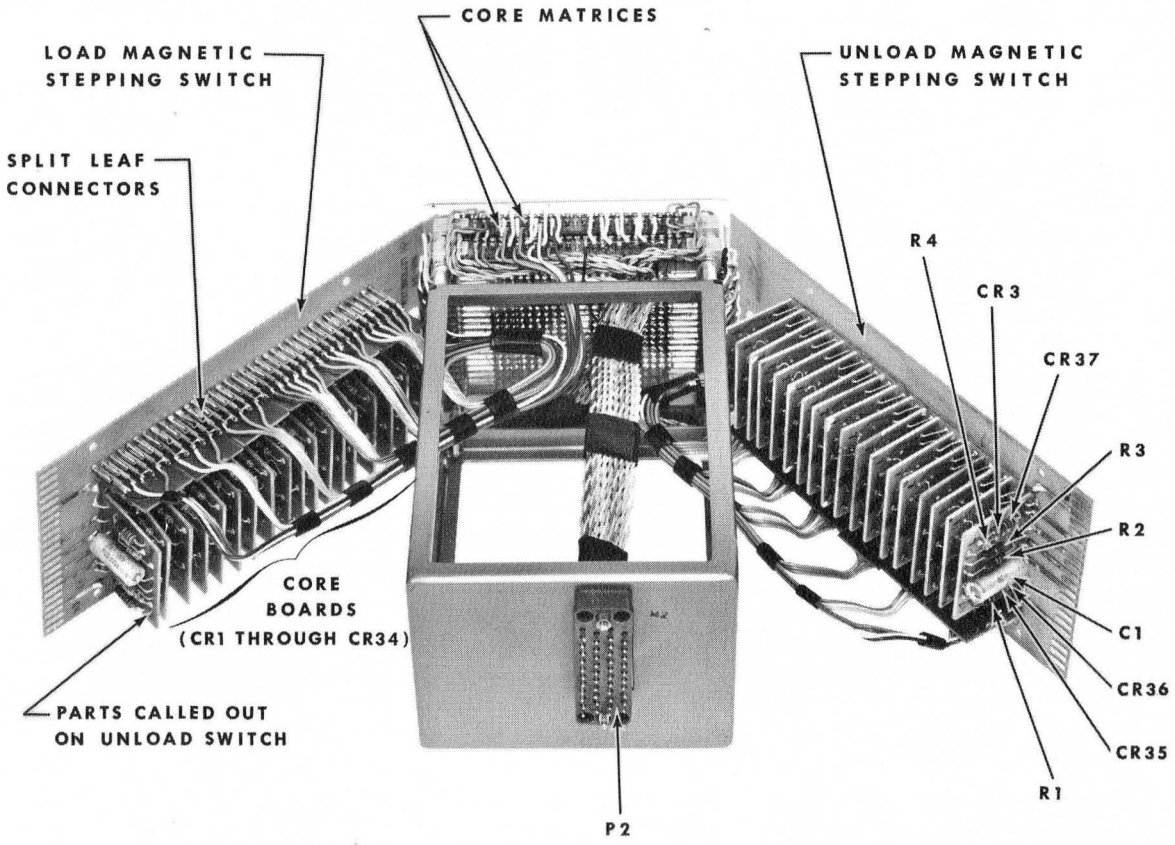


Figure 5-5. Storage System and Magnetic Stepping Switches For 144-BQ-8A Buffer, Parts Identification

5-51. MATRIX CONTINUITY CHECKS. (See Figures 5-5 and 5-6). Figure 5-5, a pictorial diagram of the storage system, and Figure 5-6, a wiring diagram of a portion of the storage system harness provide the necessary identification for a complete check of the matrix wiring. Figure 5-6 shows the 144 BA wiring which connects only one magnetic stepping switch assembly. The 144 BQ wiring is identical but will contain two identical harnesses, one for each magnetic stepping switch assembly. Continuity for the matrix X and Y drive lines, inhibit windings, sense windings, and clear windings may be checked against Tables 5-4 and 5-5. Resistance values are of a very low magnitude and careful ohmeter alignment is required if significant readings are to be obtained. The resistance of the clear, sense, and inhibit windings may be checked through connector P-2 by reading across the pin numbers indicated in Table 5-4.

Table 5-4. Resistance of Matrix Windings.

Inhibit Windings, 2.7 ohms each.

Pin NN to	Pin NN to
SS	VV
RR	WW
TT	XX
UU	PP

Sense Windings, 1.5 ohms each.

Pin E to H	Pin F to J
Pin P to S	Pin A to C
Pin M to K	Pin T to R
Pin D to B	Pin L to N

Clear windings, 12 ohms (BQ-8, BA-8). Pin U to W.

Clear Windings, 6 ohms (BQ-4, BA-4). Pin U to W.

5-52. MATRIX DRIVE LINE CONTINUITY. A rapid and reliable check on proper drive line operation may be obtained from Table 5-3, Step 13. If the X or Y drive lines are suspected of being shorted or open, Table 5-5 should be employed for continuity readings. Storage matrix continuity through eight separate Y lines to a

common return bus, through nine separate odd X lines to a common return bus, and through nine separate even X lines to a common return bus can be checked by referring to Figure 5-6 for pin and wire identification.

5-53. The eight Y drive lines are shown near the bottom of the magnetic switch split leaf connector harness. Each Y line is connected to two split leaf connectors and, beginning with the third wire off the harness bottom, the lines count consecutively up the harness. The first Y line is the first brown wire, number three from the bottom. The eight Y line is the first gray wire, number ten from the bottom.

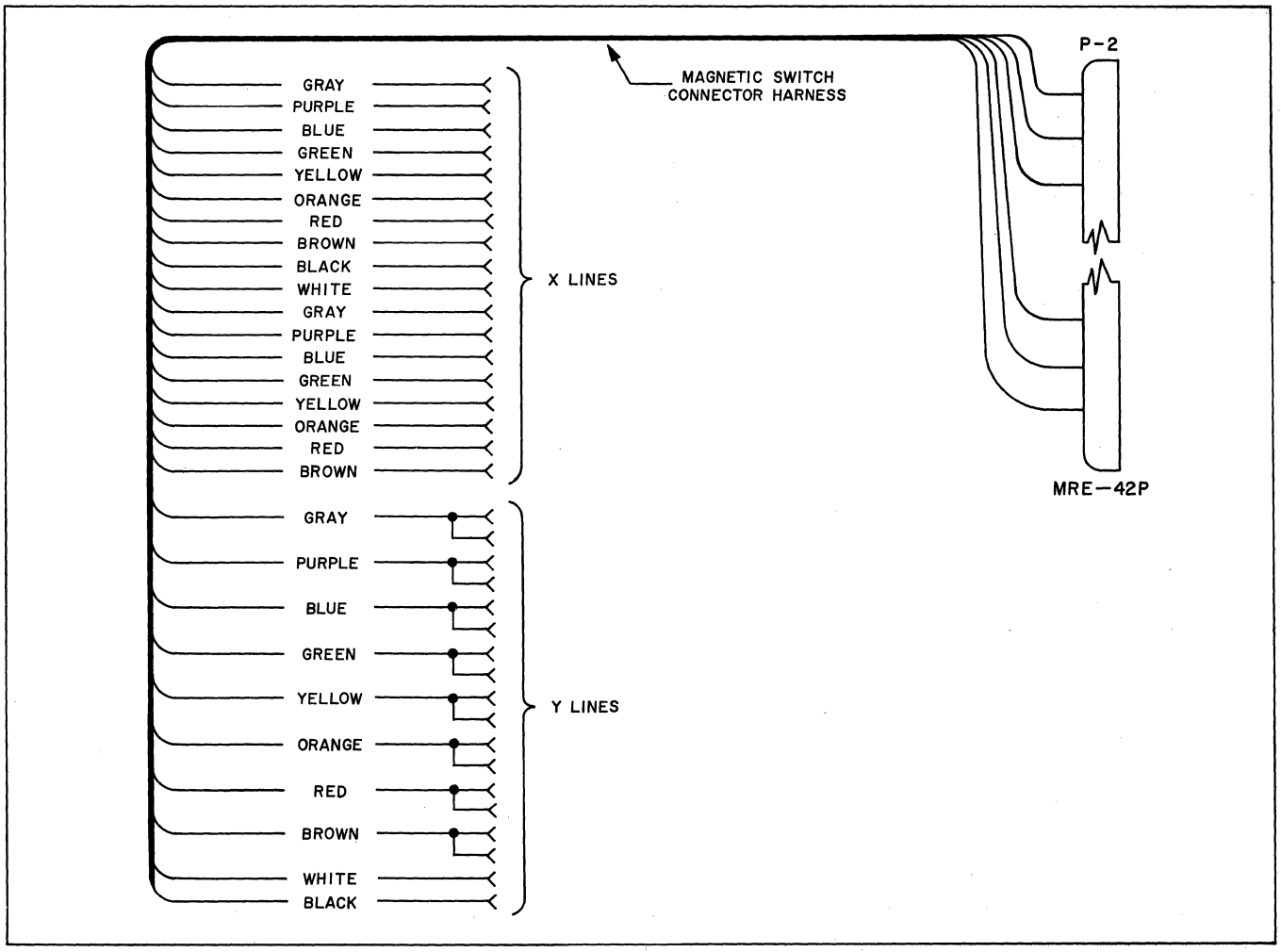


Figure 5-6. Matrix Wiring From Plug P-2 to Magnetic Switch Connectors

5-54. Continuity of the Y lines through the matrix can be checked between Plug P-2, Pin MM and the magnetic switch split leaf connectors. Pin MM locates the common return bus; the color coded wires terminating at paired split leaf connectors locate the individual drive lines. Table 5-5 will identify the color coded wires and present resistance values.

NOTE

For buffers equipped with load-unload marker card CD-B, Plug P-2 must be jumpered BB to DD and X to Z to check X drive and Y drive line continuity through the storage matrix.

Table 5-5. Matrix Drive Line Continuity.

Y Drive Lines, 1.2 Ohms Each.

Plug P-2, Pin MM to	Plug P-2, Pin MM to
Brown Wire	Green Wire
Red Wire	Blue Wire
Orange Wire	Purple Wire
Yellow Wire	Gray Wire

Odd X Drive Lines, 0.7 Ohms Each.

Black Wire, Common, to	Black Wire, Common, to
Brown Wire.... 1st X line	Brown Wire.... 11th X line
Orange Wire... 3rd X line	Orange Wire... 13th X line
Green Wire.... 5th X line	Green Wire.... 15th X line
Purple Wire... 7th X line	Purple Wire... 17th X line
White Wire.... 9th X line	

Even X Drive Lines, 0.7 Ohms Each.

White Wire, Common, to	White Wire, Common, to
Red Wire..... 2nd X line	Red Wire..... 12th X line
Yellow Wire... 4th X line	Yellow Wire... 14th X line
Gray Wire..... 6th X line	Blue Wire..... 16th X line
Blue Wire..... 8th X line	Gray Wire..... 18th X line
Black Wire.... 10th X line	

5-55. The eighteen X drive lines are shown in the harness section immediately above the Y lines. They may be counted up the harness commencing with a brown wire, number eleven from the

harness bottom. Every other X wire, i.e., the odd number wires. counting the brown wire eleven from the bottom as the first X wire, will return on a common bus. All of the even number X lines will return on a different common bus.

5-56. The two return busses are located at the very bottom of the split leaf connector harness. The black wire is the common return for all of the odd X drive lines; the white wire is the common return for all of the even X drive lines. Table 5-5 presents resistance readings between each X drive line and its common return.

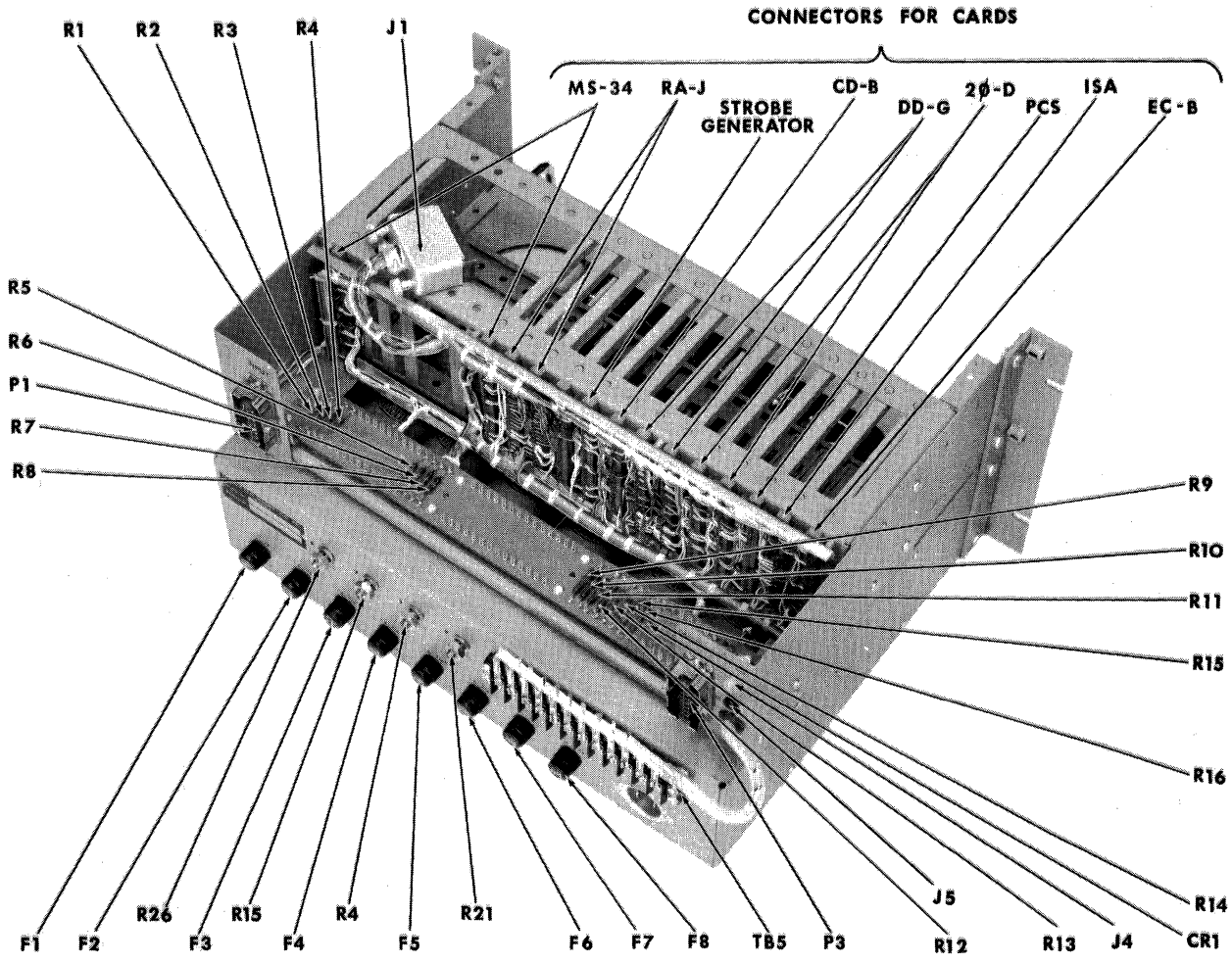


Figure 5-7. Buffer Parts Identification, Storage System, Magnetic Stepping Switches and Printed Circuit Cards Removed

TABLE 5-6. CARD CAGE WIRING

Location	Color	Terminals	Purpose
Top	Black	1P,7L,8F,9F,10F, 11Y,12L,13S,14S, 17T,17S,18H,19R	Ground
Top	Green	8K,9K,10K,11Z, 13N,14N,15F,16F, 18N,19V	+5 volt
Top	White & Green	8D,9D,10D,11B, 12E,13X,14X,15H, 16H,18P	-5 volt
Top	Purple	19T	+7 volt
Top	Orange	17E	+16 volt
Top	None	7V,7U,7T	-14 volt
Top	Red	8A,9A,10A,11H, 12M,13R,14R,15T, 16T,17Z,18C,19Z	+24 volt
Top	White & Red	1S,7J,8Z,9Z,10Z, 11P,12F,13Y,14Y, 15U,16U,18D,19M	-24 volt
Bottom	White	1U,15P	Signal
Bottom	White	1M,15J	Signal
Bottom	White	1F,7C	Signal
Bottom	White	1X, 19X	Signal
Top	White	7Z,11X,16A,18R	Signal

Location	Color	Terminals	Purpose
Top	White	7Y, 11W, 15A	Signal
Bottom	White	7F, 16P	Signal
Bottom	White	7N, 16J	Signal
Bottom	White	8T,8U,9U,9T, 11J, 12A	Signal
Bottom	White	11E, 12T	Signal
Top	White	11A, 18L	Signal
Top	White	11F,13D,13F, 13U,13W,14W, 14U,14F,14F, 18S	Signal
Bottom	White	15C,16C,19E	Signal
Bottom	White	15K,15R,16R, 16K,17H	Signal
Top	White	15D, 18K	Signal
Top	White	17Y	Signal
Top	Clear	8J	MRE 42S Pin A
Top	Brown	8H	MRE 42S Pin C
Top	Clear	8N	MRE 42S Pin B
Top	Red	8P	MRE 42S Pin D
Top	Clear	8S	MRE 42S Pin H
Top	Orange	8R	MRE 42S Pin E
Top	Clear	8M	MRE 42S Pin J
Top	Yellow	8L	MRE 42S Pin F

Location	Color	Terminals	Purpose
Top	Clear	9J	MRE 42S Pin M
Top	Green	9H	MRE 42S Pin K
Top	Clear	9N	MRE 42S Pin N
Top	Blue	9P	MRE 42S Pin L
Top	Clear	9S	MRE 42S Pin S
Top	Purple	9R	MRE 42S Pin P
Top	Clear	9M	MRE 42S Pin T
Top	Grey	9L	MRE 42S Pin R
Bottom	White	19B	MRE 42S Pin U
Top	White & Orange	7T	MRE 42S Pin W
Bottom	Brown	Terminal Board	MRE 42S Pin X
Bottom	Clear	Terminal Board	MRE 42S Pin Z
Bottom	Red	Terminal Board	MRE 42S Pin BB
Bottom	Clear	Terminal Board	MRE 42S Pin DD
Bottom	Orange	Terminal Board	MRE 42S Pin Y
Bottom	Clear	Terminal Board	MRE 42S Pin AA
Bottom	Yellow	Terminal Board	MRE 42S Pin CC
Bottom	Clear	Terminal Board	MRE 42S Pin EE
Bottom	Brown	Terminal Board	MRE 42S Pin XX
Bottom	Red	Terminal Board	MRE 42S Pin WW
Bottom	Orange	Terminal Board	MRE 42S Pin VV

Location	Color	Terminals	Purpose
Bottom	Yellow	Terminal Board	MRE 42S Pin UU
Bottom	Green	Terminal Board	MRE 42S Pin TT
Bottom	Blue	Terminal Board	MRE 42S Pin SS
Bottom	Purple	Terminal Board	MRE 42S Pin RR
Bottom	Grey	Terminal Board	MRE 42S Pin PP
Top	Black	Terminal Board	MRE 42S Pin MM
Top	White	7U	MRE 42S Pin NN

5-57. A rapid check of all power supply voltages at their card cage terminations may be accomplished with Table 5-6. Color coding and harness run (top or bottom) are listed to facilitate wire identification. Additional card cage and terminal board wiring information is also presented.

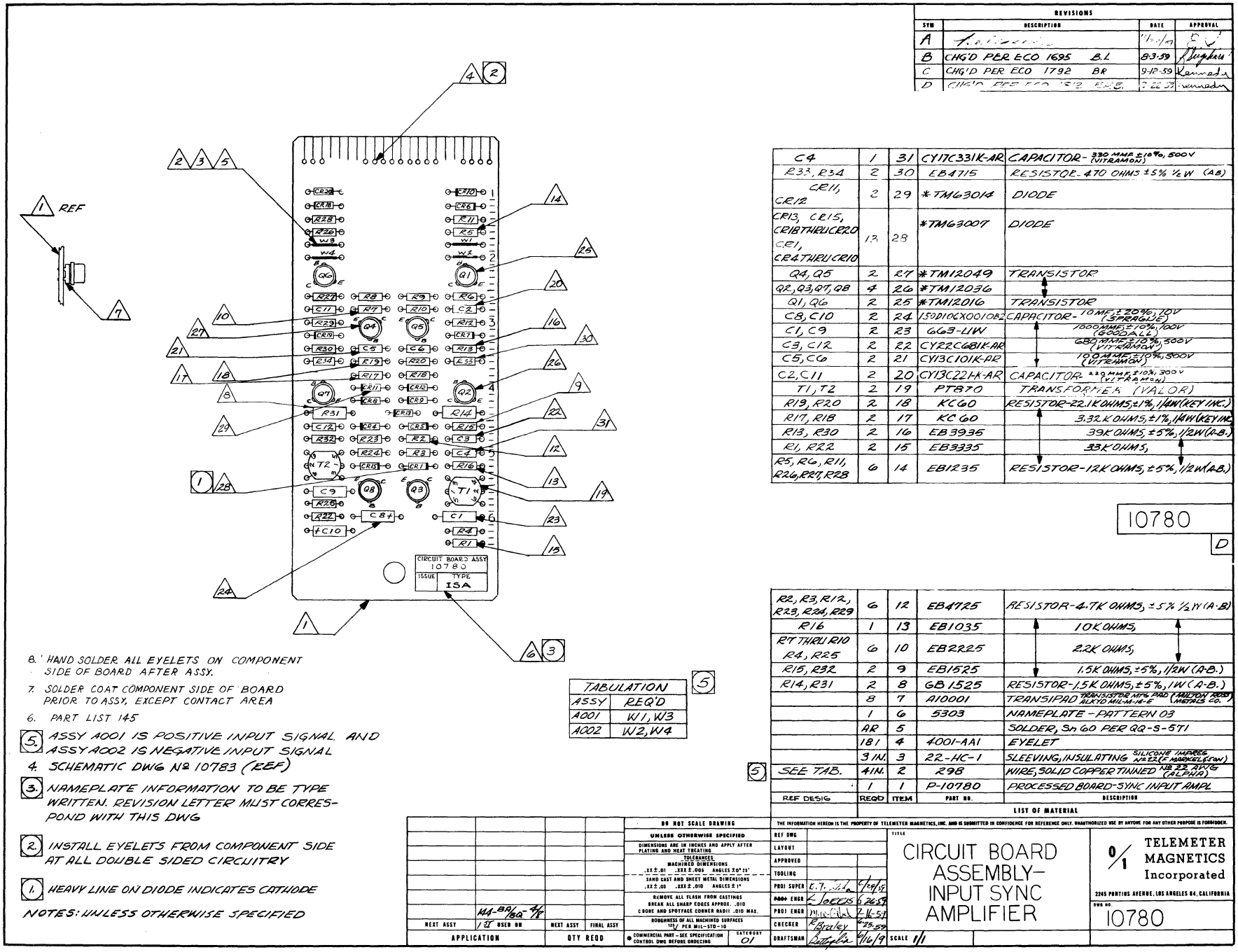
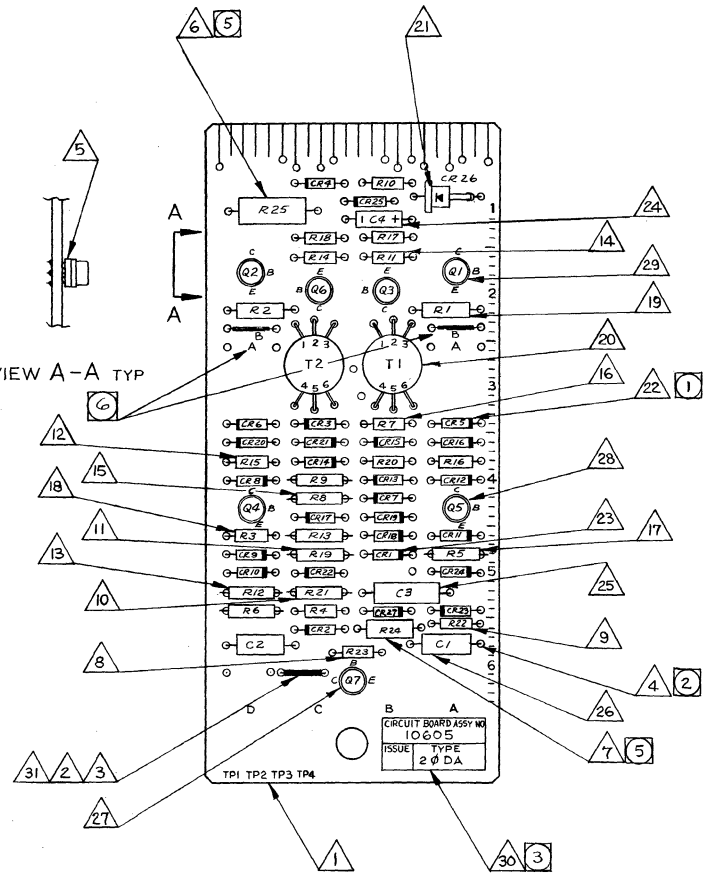


Figure 5-8. Input Sync Amplifier, Parts Identification



REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	Released	4/1/57	E.L.
B	CHANGED PER ECO 1729 AR	8/21/57	Mattson
C	CHANGED PER ECO 1792 BR	9/12/58	Kennedy
D	CHANGED PER ECO's 1847 & 1854 E.Z.	9/22/59	Mattson Kennedy

REF. DESIG FOR ASSY 10605	REQD	ITEM	PART NO.	DESCRIPTION
	AR	31		SOLDER - Sn60 PER QQ-S-571
	1	30	5303	NAMEPLATE - PATTERN 03
Q1,Q2,Q3,Q6	4	29	*TM 12041	TRANSISTOR
Q4,Q5	2	28	*TM 12001	TRANSISTOR
Q7	1	27	*TM 12004	TRANSISTOR
C1, C2	2	26	GP1K-101	CAPACITOR-100 UUF ±10%, 600V (ERIE)
C3	1	25	GP2L-102	CAPACITOR-1000 UUF ±10%, 600V (ERIE)
C4	1	24	150D106X0020B2	CAPACITOR- 10 UF, ±20% 20V (SPRAGUE)
CR1, CR2, CR3, CR4 CR7, CR8, CR9, CR12 CR13, CR14, CR15, CR16 CR17, CR18, CR19, CR20 CR21, CR22, CR23, CR27	20	23	*TM 63015	DIODE
CR5, CR6, CR10, CR11, CR24, CR25	6	22	*TM 63014	DIODE
CR26	1	21	IN 1524	DIODE (I.R.C.)
T1, T2	2	20	CP5CA	TRANSFORMER (TECHNITROL)
R1, R2	2	19	TM 1/4	SENSISTOR, 120 OHM (TEXAS INSTRUMENTS)
R3, R4	2	18	EB 1825	RESISTOR-1.8 K OHM, ±5%, 1/2W (A.B)
R5, R6	2	17	CPSE 1/2 ±1% 162 K KEL-F INSULATION	RESISTOR-1.62 K OHM, ±1%, 1/2 W (AEROVOX)
R7, R10, R17, R18	4	16	EB 4725	4.7 K OHM, ±5%, 1/2W (A.B)
R8, R9	2	15	CPSE 1/2 ±1% 4.70K KEL-F INSULATION	4.70 K OHM, ±1%, 1/2W (AEROVOX)
R11, R14	2	14	EB 5605	56 OHM, ±5%, 1/2 W (A.B)
R12, R13	2	13	CPSE 1/2 ±1% 10.0K KEL-F INSULATION	10.0 K OHM, ±1%, 1/2 W (AEROVOX)
R15, R16, R20	3	12	EB 3325	3.3 K OHM, ±5%, 1/2 W (A.B.)
R19	1	11	CPSE 1/2 ±1% 2.20K KEL-F INSULATION	2.20 K OHM, ±1%, 1/2 W (AEROVOX)
R21	1	10	CPSE 1/2 ±1% 2.61 K KEL-F INSULATION	2.61 K OHM, ±1%, 1/2W (AEROVOX)
R22	1	9	EB 2225	2.2 K OHM, ±5%, 1/2 W (A.B.)
R23	1	8	EB 1035	10 K OHM, ±5%, 1/2 W (A.B)
R24	1	7	GB 1225	RESISTOR-1.2 K OHM, ±5%, 1W (A.B.)
R25	1	6	HB 3315	RESISTOR-330 OHM, ±5% 2W (A.B)
	7	5	A-10001	TRANSIPAD - ALKYD. MIL-M-14-E (M. ROSS METALS)
	169	4	4001-AA1	EYELET
	1 IN.	3	22 HC-1	INSULATING SLEEVING SILICONE IMPREG NO. 22 (F. MARKEL & SONS)
	1 IN.	2	298	WIRE - SOLID COPPER TINNED NO. 22 AWG (ALPHA)
	1	1	P-10605	PROCESSED BOARD-2 PHASE DRIVER 'A'

LIST OF MATERIAL

10605

D

9. PARTS LIST NO. 127.
8. HAND SOLDER ALL EYELETS ON COMPONENT SIDE OF BOARD AFTER ASSY.
7. SOLDER COAT COMPONENT SIDE OF BOARD PRIOR TO ASSY, EXCEPT CONTACT AREA.
6. REFER TO TPS 10605 FOR SELECTION OF COMPONENTS AT POSITIONS A & B
5. NO EYELETS USED WITH RESISTORS R24 AND R25
4. FOR SCHEMATIC SEE DWG NO. 10604.
3. INFORMATION ON NAMEPLATE TO BE TYPEWRITTEN. ISSUE LETTER TO AGREE WITH ISSUE OF THIS DRAWING.
2. EYELETS TO BE INSTALLED FROM COMPONENT SIDE.
1. HEAVY LINE ON DIODE INDICATES CATHODE.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY	1ST USED ON	NEXT ASSY	FINAL ASSY
APPLICATION	144-BQ-8A	QTY REQD	

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING AND HEAT TREATING
TOLERANCES: MACHINED DIMENSIONS .XX ±.01 .XXX ±.005 ANGLES ±0° 25'; SAND CAST AND SHEET METAL DIMENSIONS .XX ±.03 .XXX ±.010 ANGLES ±1°
REMOVE ALL FLASH FROM CASTINGS BREAK ALL SHARP EDGES APPROX. .010 C'BORE AND SPOTFACE CORNER RADII .010 MAX.
ROUGHNESS OF ALL MACHINED SURFACES 125 PER MIL-STD-10
COMMERCIAL PART - SEE SPECIFICATION CONTROL DWG BEFORE ORDERING
CATEGORY 04

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REF DWG		
LAYOUT		
APPROVED		
STDS	B. Mattson	6/24/57
PROJ SUPER	L. T. Lee	4/1/57
PROJ ENGR	[illegible]	[illegible]
PROJ ENGR	L. Lee	6/5/59
CHECKER	R. Kennedy	6/3/59
DRAFTSMAN	E. Fung	21-MAY 59

TITLE: CIRCUIT BOARD ASSY- 2 PHASE DRIVER 'A'

SCALE 1/1

0/1 TELEMETER MAGNETICS Incorporated
2245 PONTIUS AVENUE, LOS ANGELES 64, CALIFORNIA

DWG NO. 10605

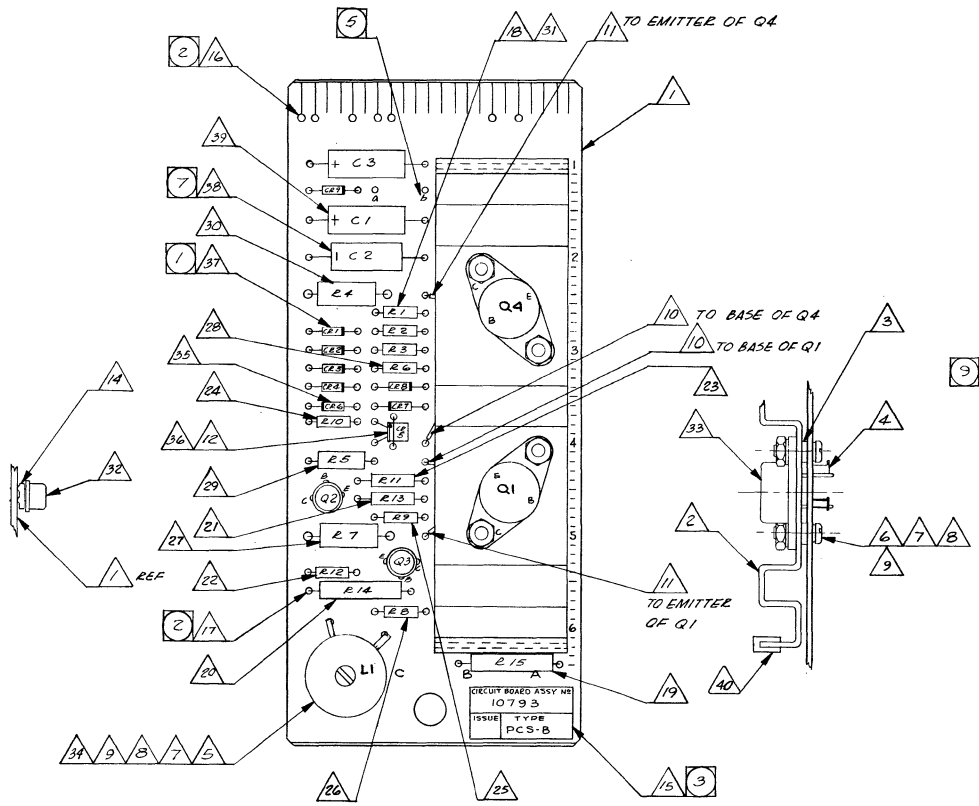
Figure 5-9. Two Phase Driver, Parts Identification

NOTES CONTINUED:

10. SOLDER COAT COMPONENT SIDE OF BOARD PRIOR TO ASSY, EXCEPT CONTACT AREA.

11. HAND SOLDER ALL EYELETS ON COMPONENT SIDE OF BOARD AFTER ASSY.

REVISIONS				
SYM	DESCRIPTION		DATE	APPROVAL
A	Released		9/16/59	E.K.
B	CHANGED PER ECO 1644	J.MC.	7-7-59	MC 7-16-59
C	CHG'D PER ECO 1700	RHC	8-13-59	R. Leyhaus
D	CHANGED PER ECO 1718	R.P.	8-20-59	Morton
E	CHANGED PER ECO 1751	J.MC	8-31-59	Mathna
F	CHANGED PER ECO 1792	B.R.	9-12-59	Kennedy



	REQD	ITEM	PART NO.	DESCRIPTION
	2	40	1335	RUBBER EXTRUSION 1.625 LG (RUBBERCRAFT)
C1, C3	2	39	150D156X0035R2	CAPACITOR - 15 UF, 35 V (SPRAGUE)
C2	1	38	XGS-2709-10	CAPACITOR - .022 UF ±10% 100 V (GUDEMAN)
CR1, CR2, CR3, CR4	4	37	*TM 63005	DIODE
CR5	1	36	*TM 64009	DIODE
CR6, CR7, CR8, CR9	4	35	*TM 63014	DIODE
L1	1	34	C279	CHOKE - 5 OHMS D.C. MAX, 10 MHY (DEECO)
Q1, Q4	2	33	*TM 12030	TRANSISTOR
Q2, Q3	2	32	*TM 12036	TRANSISTOR
R1, R2, R3	3	31	EB 1005	RESISTOR - 10 OHMS ±5% ½ W (A.B.)
R4	1	30	HB 2215	220 OHMS ±5% 2W (A.B.)
R5	1	29	GB 1021	1K OHMS ±5% 1W (A.B.)
R6	1	28	EB 1515	150 OHMS ±5% ½ W (A.B.)
R7	1	27	HB 6815	680 OHMS ±5% 2W (A.B.)
R8	1	26	EB 1525	1.5K OHMS ±5% ½ W (A.B.)
R9	1	25	TYPE RC 60 180Ω ±1% ¼W	180 OHMS ±1% ¼ W (KEY)
R10	1	24	EB 8215	820 OHMS ±5% ½ W (A.B.)
R11	1	23	EB 1515	150 OHMS ±5%, ½ W (AB)
R12	1	22	TYPE RC 60 82Ω ±1% ¼ W	RESISTOR - 82 OHMS ±1%, ¼ W (KEY)
R13	1	21	TM 14-100Ω 10% ¼W	SENSISTOR - 100 OHMS ±10%, ¼ W (SPRAGUE) (TEXAS INSTR.)
R14	1	20	TYPE RC 75 68Ω ±1% 1W	RESISTOR - 68 OHMS ±1%, 1W (KEY)
R15	1	19	TYPE RC 75 56Ω ±1% 1W	RESISTOR - 56 OHMS ±1%, 1W (KEY)
	AR	18		SOLDER - Sn 60 PER QQ-S-571
	10	17	3E 23E	EYELET - GOLDFLASHED (UNITED SHOE)
	67	16	4001-AA1	EYELET
	1	15	5303	NAMEPLATE - PATTERN 03
	2	14	A 10001	TRANSIPAD TRANSISTOR MTG PAD (MILTON BOSS) ALKYD MIL-M-14-E (METALS CO.)
		13		
	1 IN	12	298	WIRE - SOLID COPPER, TINNED Nº 22 AWG (ALPHA)
	3 IN	11	1000-22-(19) 1	WIRE - INSULATED PER MIL-W-16878 (SEQUOIA) BROWN
	4 IN.	10	1000-22-(19) 5	WIRE - INSULATED PER MIL-W-16878 (SEQUOIA) GREEN
	5	9	MS 35649-62	NUT - HEXAGON CAD PLATE 6-32
	5	8	MS 35333-37	WASHER - LOCK Nº 6
	5	7	MS 15795-205	WASHER - FLAT Nº 6 CAD PLATE
	4	6	MS 35223-30	SCREW Nº 6-32 x 1/2 LONG
	1	5	MS 35223-32	SCREW Nº 6-32 x 3/4 LONG
	2	4	210-6400	TRANSISTOR SIDE LEAD SOCKET (AMP)
	4	3	3911AA04-152-02	SPACER
	1	2	1037-3-2022	HEAT SINK
	1	1	P-10793	PROC BD-POSITIVE CURRENT STABILIZER-B

REFERENCE DESIGNATION — LIST OF MATERIAL

10793 F

9. IF KEY RESISTORS ARE NOT AVAILABLE SUBSTITUTE DALOHM DC-1, 56 OHMS ±1%, 1W.
8. PARTS LIST Nº 142
7. DASH (-) INDICATES LEAD COMMON TO CASE
6. TO CONNECT PINS "T" & "S" TOGETHER JUMPER POINTS "a" & "b"
5. RUBBER STAMP LETTERS "a" & "b" APPROX. AS SHOWN
4. SCHEMATIC DWG Nº 10874
3. NAMEPLATE INFO TO BE TYPEWRITTEN. REVISION LETTER MUST COINCIDE WITH THIS DWG.
2. INSTALL EYELETS FROM COMPONENT SIDE AT ALL DOUBLE SIDED CIRCUITRY
1. HEAVY LINE ON DIODE INDICATES CATHODE.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY	1ST USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING AND HEAT TREATING
TOLERANCES
MACHINED DIMENSIONS
.XX ±.01 .XXX ±.005 ANGLES ±0°15'
SAND CAST AND SHEET METAL DIMENSIONS
.XX ±.03 .XXX ±.010 ANGLES ±1°
REMOVE ALL FLASH FROM CASTINGS
BREAK ALL SHARP EDGES APPROX. .010
C BORE AND SPOTFACE CORNER RADII .010 MAX.
ROUGHNESS OF ALL MACHINED SURFACES 125 PER MIL-STD-10
* COMMERCIAL PART - SEE SPECIFICATION CONTROL DWG BEFORE ORDERING — CATEGORY 04

REF DWG		
LAYOUT		
APPROVED		
STDS	E. Hathaway	9/16/59
PROJ SUPER	G.T. Davis	9/11/59
~~PROJ~~ ENGR	L. Ferris	9/16/59
PROJ ENGR	M. Arellano	
CHECKER	R. Leyhaus	9/16/59
DRAFTSMAN	Nishimura	9-11-59

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TITLE: CIRCUIT BOARD ASSEMBLY- POSITIVE CURRENT STABILIZER-B

SCALE 1/1

0/1 TELEMETER MAGNETICS Incorporated
2345 PONTIUS AVENUE, LOS ANGELES 64, CALIFORNIA

DWG NO. 10793

Figure 5-10. Positive Current Stabilizer, Parts Identification

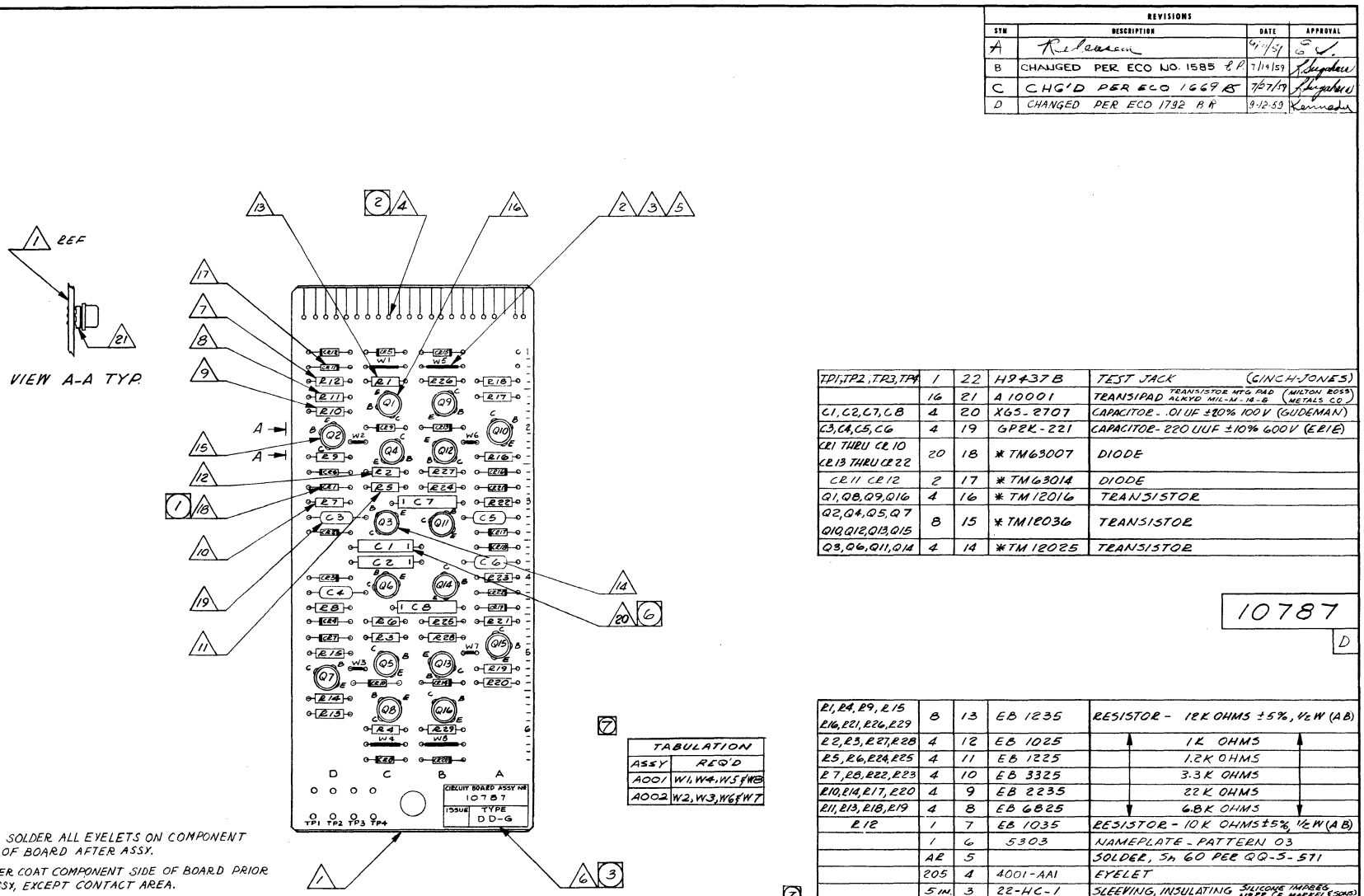
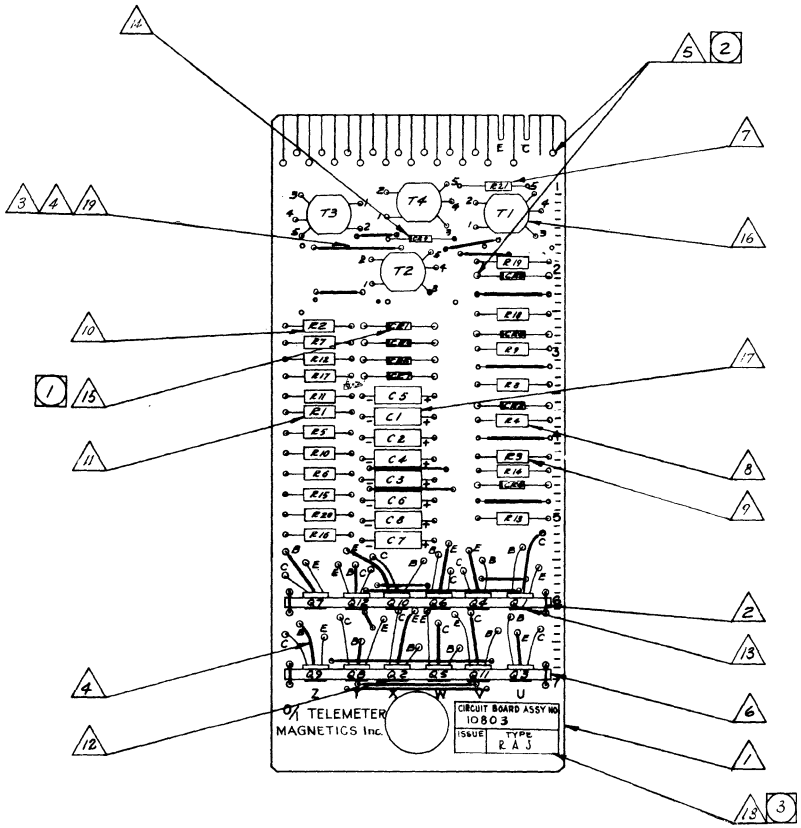


Figure 5-11. Digit Driver, Parts Identification



REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A			
B	CHG'D PER ECO NO 1727 B R	8-25-59	
C	CHG'D PER ECO # 1742 REVISED	9/31/59	
D	CHG'D PER ECO # 1792 B R	9-12-59	

REF. DESIGNATION	REQD	ITEM	PART NO.	DESCRIPTION
	AR	19		SOLDER Sn 60 PER QQ-S-571
	1	18	5303	NAMEPLATE PATTERN 03
C1, C2, C3, C4, C5, C6, C7, C8	8	17	150 D 106X002 CB2	CAPACITOR 10μF 20% 20VDC (SPRAGUE)
T1, T2, T3, T4	4	16	PT 860	TRANSFORMER (VALOR)
				10803 D
CR1, CR2, CR3, CR4, CR5, CR6, CR7, CR8	8	15	* TM 630-5	DIODE
CR9	1	14	* TM 630-4	DIODE
Q1, Q3, Q4, Q6, Q7, Q9, Q10, Q12	8	13	* TM 12048	TRANSISTOR
Q2, Q5, Q8, Q11	4	12	* TM 2647	TRANSISTOR
R1, R5, R6, R10, R11, R15, R16, R20	8	11	CPSF ½ 1% 33.2K REG. F-INSULATION	RESISTOR 33.2K 1% ½W (AEROVOX)
R2, R7, R12, R17	4	10	EB 4725	RESISTOR 4.7K 5% ½W (A B)
R3, R8, R13, R18	4	9	EB 4715	RESISTOR 470Ω 5% ½W (A B)
R4, R9, R14, R19	4	8	CPSF ½ 1% 332K REG. F-INSULATION	RESISTOR 8.25K 1% ½W (AEROVOX)
R21	1	7	EB 8225	RESISTOR 8.2K 5% 1/2W (A B)
	2	6	4903 A1	BRACKET - PATTERN 03
	71	5	4001-AA1	EYELET
	.36 IN	4	22 HC-1	INSULATION SLEEVING SILICONE IMPREG NO 22 (FRANK MAKELL)
	24 IN	3	298	WIRE COPPER SOLID TINNED (NO 22 AWG)
	4	2	297	WIRE COPPER SOLID TINNED (NO 20 AWG) E.IN. LONG (ALPHA)
	1	1	P 10803	PROC BD-ETCH CKT READ AMPL J

LIST OF MATERIAL

7. PARTS LIST NO. 134
6. HAND SOLDER ALL EYELETS ON COMPONENT SIDE OF BOARD AFTER ASSY.
5. SOLDER COAT COMPONENT SIDE OF BOARD PRIOR TO ASSY, EXCEPT CONTACT AREA.
4. FOR SCHEMATIC SEE DWG. NO. 10805
3. INFORMATION ON NAMEPLATE TO BE TYPEWRITTEN ISSUE LETTER TO AGREE WITH ISSUE OF THIS DRAWING
2. EYELETS TO BE INSTALLED FROM COMPONENT SIDE AT ALL DOUBLE SIDED CIRCUITRY & SEMI CONDUCTOR TERMINALS
1. HEAVY LINES ON DIODES INDICATES CATHODES

NOTES: UNLESS OTHERWISE SPECIFIED

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING AND HEAT TREATING
TOLERANCES
MACHINED DIMENSIONS
.XX ± .01 .XXX ± .005 ANGLES ± 0° 15'
SAND CAST AND SHEET METAL DIMENSIONS
.XX ± .03 .XXX ± .010 ANGLES ± 1°
REMOVE ALL FLASH FROM CASTINGS
BREAK ALL SHARP EDGES APPROX. .010
RADII AND SPOTFACE CORNES RADII .010 MAX.
ROUGHNESS OF ALL MACHINED SURFACES 125 PER MIL-STD-10
COMMERCIAL PART - SEE SPECIFICATION CONTROL DWG BEFORE ORDERING
FACTORY 84

REF DWG
LAYOUT
APPROVED
STDS
PROJ SUPER
PROJ ENGR
PROJ ENGR
CHECKED
DRAFTSMAN

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TITLE
CIRCUIT BOARD ASSY-READ AMPLIFIER-J

0/1 TELEMETER MAGNETICS Incorporated
2340 PONTIUS AVENUE, LOS ANGELES 64, CALIFORNIA

DWG NO. 10803

SCALE 1/1

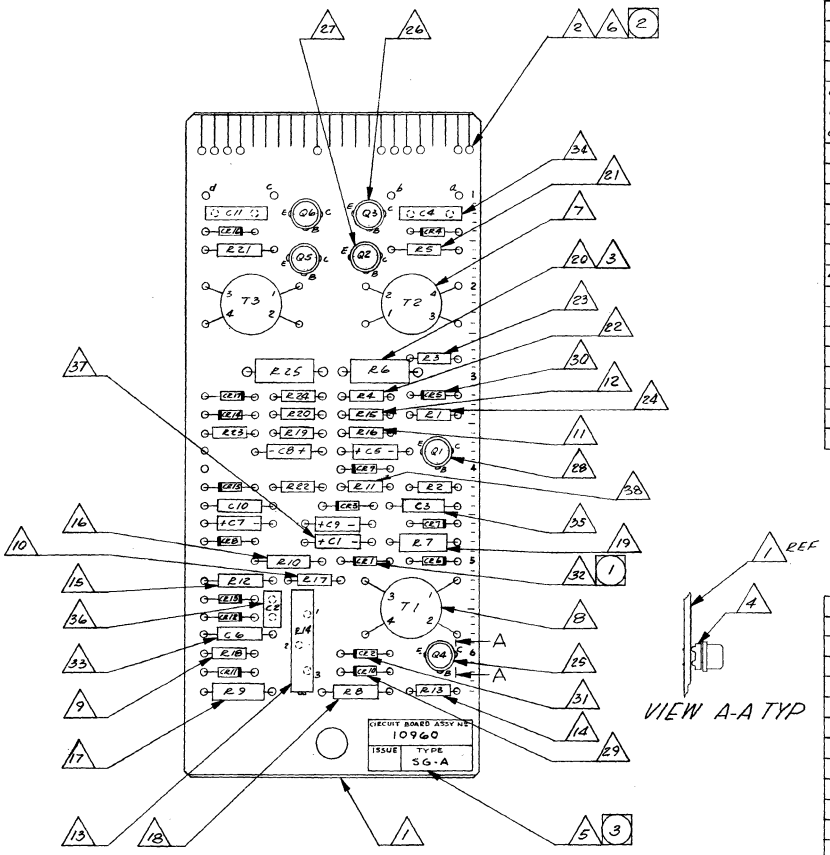
NEXT ASSY	1ST USED ON	NEXT ASSY	FINAL ASSY
APPLICATION	144 89/84 4/8	QTY REQD	

Figure 5-12. Read Amplifier, Parts Identification

NOTES CONTINUED

7. SOLDER COAT COMPONENT SIDE OF BOARD PRIOR TO ASSY. EXCEPT CONTACT AREA.
8. SOLDER ALL EYELETS TO CIRCUITRY ON COMPONENT SIDE OF BOARD AT ASSY.

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
F	F		F
B	CHANGED PER ECO 1745 GW	25 JULY 59	
C	[illegible] 1792 SR	9-12-59	Kennedy
D	CHANGED PER E.C.O. NO. 1849 C.S.	9-25-59	



REF. DESIG.	REQD	ITEM	PART NO.	DESCRIPTION
R11	1	38	EB 3935	RESISTOR - 39K ±5% ½W (AB)
C1,C5,C7,C8,C9	5	37	150D106X0020 B2	CAPACITOR - 10 UF ±20% 20V (SPRAGUE)
C2	1	36	DM 15-331-J	330 UUF ±5% 500V DUR-MICA (ARCO)
C3, C10	2	35	DM-15-151-J	150 UUF ±5% DUR-MICA (ARCO)
C4, C11	2	34	DM 20-502-J	5000 UUF ±5% 300V DUR-MICA (ARCO)
C6	1	33	DM-15-221-J	CAPACITOR 220 UUF ±5% DUR-MICA (ARCO)
CR1	1	32	PS 6468	DIODE (PSI)
CR2, CR3, CR4 CR7, CR8, CR9 CR11 THRU CR16	12	31	*TMG3007	
CR5, CR6, CR17	3	30	*TMG3006	
CR10	1	29	*TMG3014	DIODE
Q1	1	28	*TM 12047	TRANSISTOR
Q2, Q5	2	27	*TM 12016	
Q3, Q6	2	26	2N417	(RAYTHEON)
Q4	1	25	*TM 12041	TRANSISTOR
R1, R2 , R22	3	24	EB 1025	RESISTOR - 1K ±5% ½W (AB)
R3, R23	2	23	EB 2215	220 OHMS ±5% ½W (AB)
R4, R24	2	22	EB 4725	4.7K ±5% ½W (AB)
R5, R21	2	21	CPSE ½ 221 ±1%	221 OHMS ±1% ½W REL-F INSUL (AEROVOX)
R6, R25	2	20	HB 6815	680 OHMS ±5% 2W (AB)
R7	1	19	GB 1225	1.2K ±5% 1W (AB)
R8	1	18	CPSE ½ 100 ±1%	RESISTOR - 100 OHMS ±1% ½W REL-F INSUL (AEROVOX)
R 9	1	17	TI 913-TM ¼	SENSISTOR 100 OHMS ±10% ¼W (TEXAS INST.)
R10	1	16	CPSE ½ 1.00K ±1%	RESISTOR - 1.00K ±1% ½W REL-F INSUL (AEROVOX)
R12	1	15	CPSE ½ 562 ±1%	RESISTOR - 562 OHMS ±1% ½W REL-F INSUL (AEROVOX)
R13	1	14	EB 3325	RESISTOR - 3.3K ±5% ½W (AB)
R14	1	13	275-1-201	VARIABLE RESISTOR - 200 OHMS (BOURNS)
R15, R20	2	12	EB 2705	RESISTOR - 27 OHMS ±5% ½W (AB)
R16, R19	2	11	EB 5605	56 OHMS ±5% ½W (AB)
R17	1	10	EB 8225	8.2K ±5% ½W (AB)
R18	1	9	EB 1225	RESISTOR - 1.2K ±5% ½W (AB)
T1	1	8	C02HA	TRANSFORMER, PULSE (TECHNITROL)
T2, T3	2	7	C52HA	TRANSFORMER, PULSE (TECHNITROL)
	AR	6	4001-AA1	SOLDER - Sn 60 PER QQ-S-571
	1	5	5303	NAMEPLATE - PATTERN 03
	6	4	A10001	TRANSIPAD TRANSISTOR MTG PAD (H BOSS METALS CO) ALKYD MIL-M-14-E
	4	3	SE-23F	EYELET - GOLD FLASHED (UNITED-CAROE)
	151	2	4001-AA1	EYELET
	1	1	P-10960	PROC BD - STROBE GENERATOR-A

LIST OF MATERIAL

10960 D

6. PARTS LIST Nº 168 (REF)
5. SPACES BETWEEN POINTS a & b AND c & d PROVIDED FOR ADDITIONAL RESISTORS
4. SCHEMATIC DRAWING Nº 10961
3. NAMEPLATE INFORMATION TO BE TYPEWRITTEN. REVISION LETTER MUST CORRESPOND WITH THIS DRAWING.
2. INSTALL EYELETS FROM COMPONENT SIDE
1. HEAVY LINE ON DIODE INDICATES CATHODE

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING AND HEAT TREATING
TOLERANCES
MACHINED DIMENSIONS .XX ±.01 .XXX ±.005 ANGLES ±0°25'
SAND CAST AND SHEET METAL DIMENSIONS .XX ±.03 .XXX ±.010 ANGLES ±1°
REMOVE ALL FLASH FROM CASTINGS
BREAK ALL SHARP EDGES APPROX. .010 C'BORE AND SPOTFACE CORNER RADII .010 MAX.
ROUGHNESS OF ALL MACHINED SURFACES 125 PER MIL-STD-10
COMMERCIAL PART - SEE SPECIFICATION CONTROL DWG BEFORE ORDERING
CATEGORY 04

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REF DWG	
LAYOUT	
APPROVED	
TOOLING	
PROJ SUPER	L.T. 9/17/59
PROJ ENGR	L. Jones 9/17/59
CHECKER	R. Braley 9/18/59
DRAFTSMAN	Kirkman 9/10/59

TITLE: CIRCUIT BOARD ASSEMBLY- STROBE GENERATOR-A

SCALE 1/1

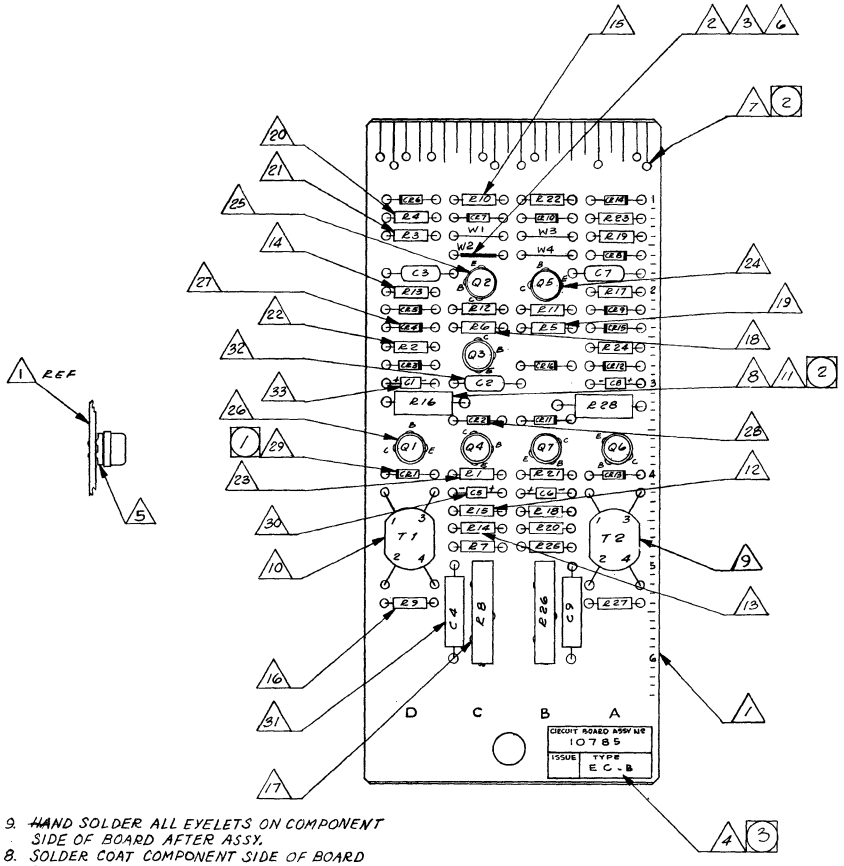
0/1 TELEMETER MAGNETICS Incorporated
2245 PONTIUS AVENUE, LOS ANGELES 64, CALIFORNIA

DWG NO. 10960

Figure 5-13. Strobe Generator, Parts Identification

REVISIONS				
SYM	DESCRIPTION		DATE	APPROVAL
A	Released		4/16/59	E.K.
B	CHG'D PER ECO NO 1668	RHC	7-24-59	Hughes
C	CHG'D PER ECO 1714	RS	8-12-59	Hughes
D	CHG'D PER ECO NO 1727	B.R	8-25-59	Ewing
E	CHG'D PER ECO NO 1778 & 1848	I.M. R.P.B.	9-21-59	Kennedy Sullivan
F	CHG'D PER ECO 1792	B.R.	9-12-59	Kennedy

6 TABULATION	
ASSY	REQ'D
A001	W1 & W4
A002	W2 & W3



REFERENCE DESIGNATION	REQD	ITEM	PART NO.	DESCRIPTION
C1, C8	2	33	150D225X0006A2	CAPACITOR, 2.2 UF ± 20% 6V (SPRAGUE)
C2, C3, C7	3	32	GP2K-471	470 UUF ±10% 600V (ERIE)
C4, C9	2	31	GP2L-102	1000 UUF ±10% 600V (ERIE)
C5, C6	2	30	150D224X0035A2	CAPACITOR, .22 UF ± 20% 35V (SPRAGUE)
CR1, CR5 THRU CR10, CR13, CR14, CR16	10	29	*TM63015	DIODE
CR2, CR3, CR11, CR12	4	28	*TM63014	DIODE
CR4, CR15	2	27	IN625	DIODE (HUGHES)
Q1, Q4, Q6, Q7	4	26	*TM12041	TRANSISTOR
Q2, Q3	2	25	*TM12001	TRANSISTOR
Q5	1	24	*TM12004	TRANSISTOR
R1, R7, R21, R25	4	23	EB 6815	RESISTOR, 680 OHMS ±5% ½W (A.B)
R2, R12, R24	3	22	EB 3925	3.9K OHMS
R3	1	21	EB 3935	39K OHMS
R4, R11, R19, R22	4	20	EB 1235	12K OHMS
R5	1	19	EB 4725	4.7K OHMS
R6	1	18	EB 2725	RESISTOR 2.7K OHMS ±5% ½W (A.B)
R8, R26	2	17	TYPE-R, PIN TYPE	RESISTOR, VARIABLE 250 OHMS ±10% ½W (A.B)
R9, R27	2	16	EB 1015	RESISTOR, 100 OHMS ±5%, ½ W (A.B)
R10, R23	2	15	EB 4735	RESISTOR, 47K OHMS ±5%, ½ W (A.B)
R13, R17	2	14	EB 1035	10K OHMS
R14, R20	2	13	EB 2735	27K OHMS
R15, R18	2	12	EB 5605	RESISTOR, 56 OHMS ±5% ½W (A.B)
R16, R28	2	11	HB 3305	RESISTOR, 33 OHMS ±5% 2W (A.B)
T1	1	10	20F821	TRANSFORMER (VALOR)
T2	1	9	40F821	TRANSFORMER (VALOR)
	4	8	5E-23F	EYELET, GOLD FLASHED (UNITED SNAP)
	151	7	4001-AA1	EYELET
	AR	6		SOLDER, Sn 60 PER QQ-S-571
	7	5	A10001	TRANSIPAD TRANSISTOR MTG PAD (MILTON ROY) ALKYD MIL-M-14-E (METALS CO.)
	1	4	5303	NAMEPLATE, PATTERN 03
	1 IN	3	22-HC-1	SLEEVING, INSULATING Nº22 SILICONE IMPREG (J. MARREL & SONS)
SEE TAB	3 IN	2	298	WIRE, SOLID COPPER TINNED Nº22 AWG (ALPHA)
	1	1	P-10785	PROCESSED BD-ELECTRONIC CLEAR-B

LIST OF MATERIAL

10785 F

9. ~~HAND~~ SOLDER ALL EYELETS ON COMPONENT SIDE OF BOARD AFTER ASSY.
8. SOLDER COAT COMPONENT SIDE OF BOARD PRIOR TO ASSY, EXCEPT CONTACT AREA.
7. PARTS LIST Nº 141
6. ASSY A001 IS FOR POSITIVE SIGNAL & ASSY A002 IS FOR NEGATIVE SIGNAL
5. ~~INSTALL TRANSFORMER 20F821 ON BA SYSTEM~~ ~~INSTALL TRANSFORMER 40F821 ON BB SYSTEM~~
4. SCHEMATIC DWG Nº 10853
3. NAMEPLATE INFORMATION TO BE TYPEWRITTEN. REVISION LETTER MUST COINCIDE WITH THIS DWG.
2. INSTALL EYELETS FROM COMPONENT SIDE AT ALL DOUBLE SIDED CIRCUITRY.
1. HEAVY LINE ON DIODE INDICATES CATHODE

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

144-BA/BB-4/B

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING, AND HEAT TREATING

TOLERANCES
MACHINED DIMENSIONS
.XX ±.01 .XXX ±.005 ANGLES 30' 15'
SAND CAST AND SHEET METAL DIMENSIONS
.XX ±.05 .XXX ±.010 ANGLES 2.1°

REMOVE ALL FLASH FROM CASTINGS
BREAK ALL SHARP EDGES APPROX. .010
C'BORE AND SPOTFACE CORNER RADII .010 MAX.

ROUGHNESS OF ALL MACHINED SURFACES
125/ PER MIL-STD-10

● COMMERCIAL PART - SEE SPECIFICATION CONTROL DWG BEFORE ORDERING

CATEGORY 04

REF DWG			
LAYOUT			
APPROVED			
STDS	[illegible]	6/2/59	
PROJ SUPER	D.T. Bell	11/4/59	
PROJ ENGR	L. Harris	6/15/59	
PROJ ENGR	H. Abel	6/15/59	
CHECKER	[illegible]	6/15/59	
DRAFTSMAN	Nishimura	6/8/59	

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TITLE
CIRCUIT BOARD ASSEMBLY - ELECTRONIC CLEAR-B

SCALE 1/1

0/1

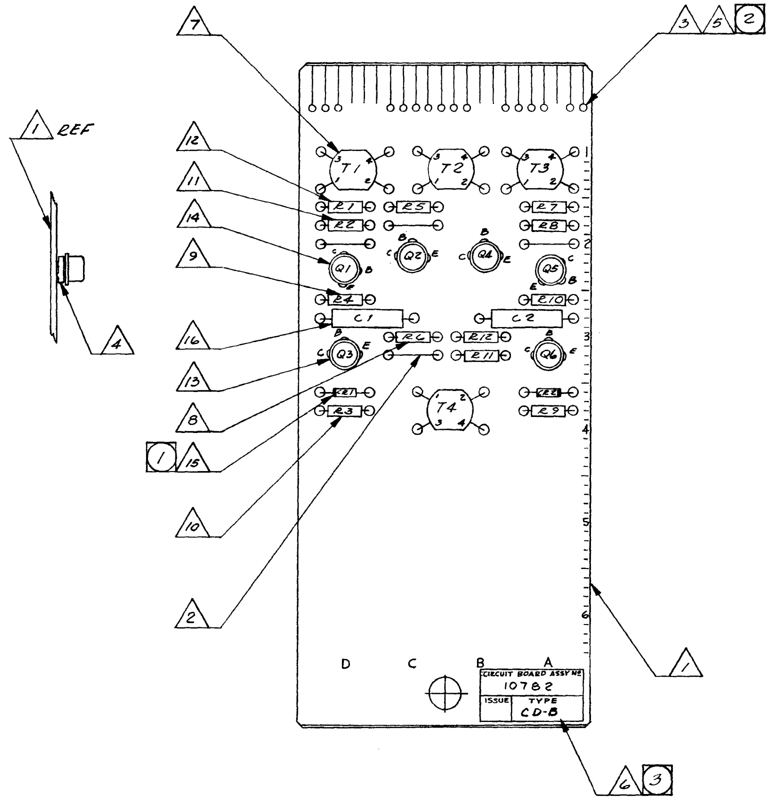
TELEMETER MAGNETICS Incorporated
2245 PORTIUS AVENUE, LOS ANGELES 64, CALIFORNIA

DWG NO. 10785

Figure 5-14. Electronic Clear (EC-B), Parts Identification

REVISIONS

SYM	DESCRIPTION	DATE	APPROVAL
A	Released	6/17/59	
B	CHANGED PER ECO 01630 J.Mc	7-7-9	7-16-9
C	CHANGED PER ECO 1745 C.P.		



10782

C

REFERENCE DESIGNATION	REQD	ITEM	PART NO.	DESCRIPTION
C1, C2	2	16	663-UW (.001UF)	CAPACITOR-1000UUF ±20% 100V (GOOD ALL)
CR1, CR2	2	15	*TM 63015	DIODE
Q1, Q2, Q4, Q5	4	14	*TM 12041	TRANSISTOR
Q3, Q6	2	13	*TM 12016	TRANSISTOR
R1, R5, R7, R11	4	12	EB5605	RESISTOR - 56 OHMS ±5%, ½W (A.B)
R2, R8	2	11	CPSE ½ 3.82K 1% ½W KEL-F INSULATION	3.82K OHMS ±1%, ½W KEL-F INSULATION (AEROVOX)
R3, R9	2	10	EB 4725	4.7 K OHMS ±5%, ½W (A.B)
R4, R10	2	9	EB 1025	1 K OHMS ±5%, ½W (A.B)
R6, R12	2	8	CPSE ½ 8.25K 1% ½W KEL-F INSULATION	RESISTOR - 8.25K OHMS ±1% ½W KEL-F INSULATION (AEROVOX)
T1, T2, T3, T4	4	7	PT 808	TRANSFORMER (VALOR)
	1	6	5303	NAMEPLATE - PATTERN 03
	AR	5		SOLDER, Sn 60 PER QQ-S-571
	6	4	A10001	TRANSIPAD TRANSISTOR MTG PAD ALKYD MIL-M-14-E (MILTON ROSS METALS CO.)
	90	3	10687	EYELET
	6IN	2	298	WIRE, SOLID COPPER, TINNED Nº 22 AWG (ALPHA)
	1	1	P-10782	PROC BD - COINCIDENCE DETECTOR B

LIST OF MATERIAL

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5 PARTS LIST Nº 143
4. SCHEMATIC DWG Nº 10812
3 NAMEPLATE INFORMATION TO BE TYPEWRITTEN. REVISION LETTER MUST COINCIDE WITH THIS DWG.
2 INSTALL EYELETS FROM COMPONENT SIDE AT ALL DOUBLE SIDED CIRCUITRY.
1 HEAVY LINE ON DIODE INDICATES CATHODE
NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
144-BA/BQ-4/8	1ST		
APPLICATION		QTY REQD	

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING AND HEAT TREATING
TOLERANCES
MACHINED DIMENSIONS
.XX ± .01 .XXX ± .005 ANGLES ± 0° 25'
SAND CAST AND SHEET METAL DIMENSIONS
.XX ± .03 .XXX ± .010 ANGLES ± 1°
REMOVE ALL FLASH FROM CASTINGS
BREAK ALL SHARP EDGES APPROX. .010
C BORE AND SPOTFACE CORNER RADII .010 MAX.
ROUGHNESS OF ALL MACHINED SURFACES 125 PER MIL-STD-10
* COMMERCIAL PART - SEE SPECIFICATION CONTROL DWG BEFORE ORDERING
CATEGORY 04

REF DWG		
LAYOUT		
APPROVED		
STDS	E. Hathaway	6/15/59
PROJ SUPER	D.T. Jude	6/17/59
~~PROJ ENGR~~	L. Soreis	6/15/59
PROJ ENGR	H. ADEL BTG	6/17/59
CHECKER		6/15/59
DRAFTSMAN	Nishimura	6-13-59

TITLE: CIRCUIT BOARD ASSEMBLY-COINCIDENCE DETECTOR B

SCALE 1/1

TELEMETER MAGNETICS Incorporated
2245 PONTIUS AVENUE, LOS ANGELES 64, CALIFORNIA

DWG NO. 10782

Figure 5-15. Coincident Current Detector, Parts Identification

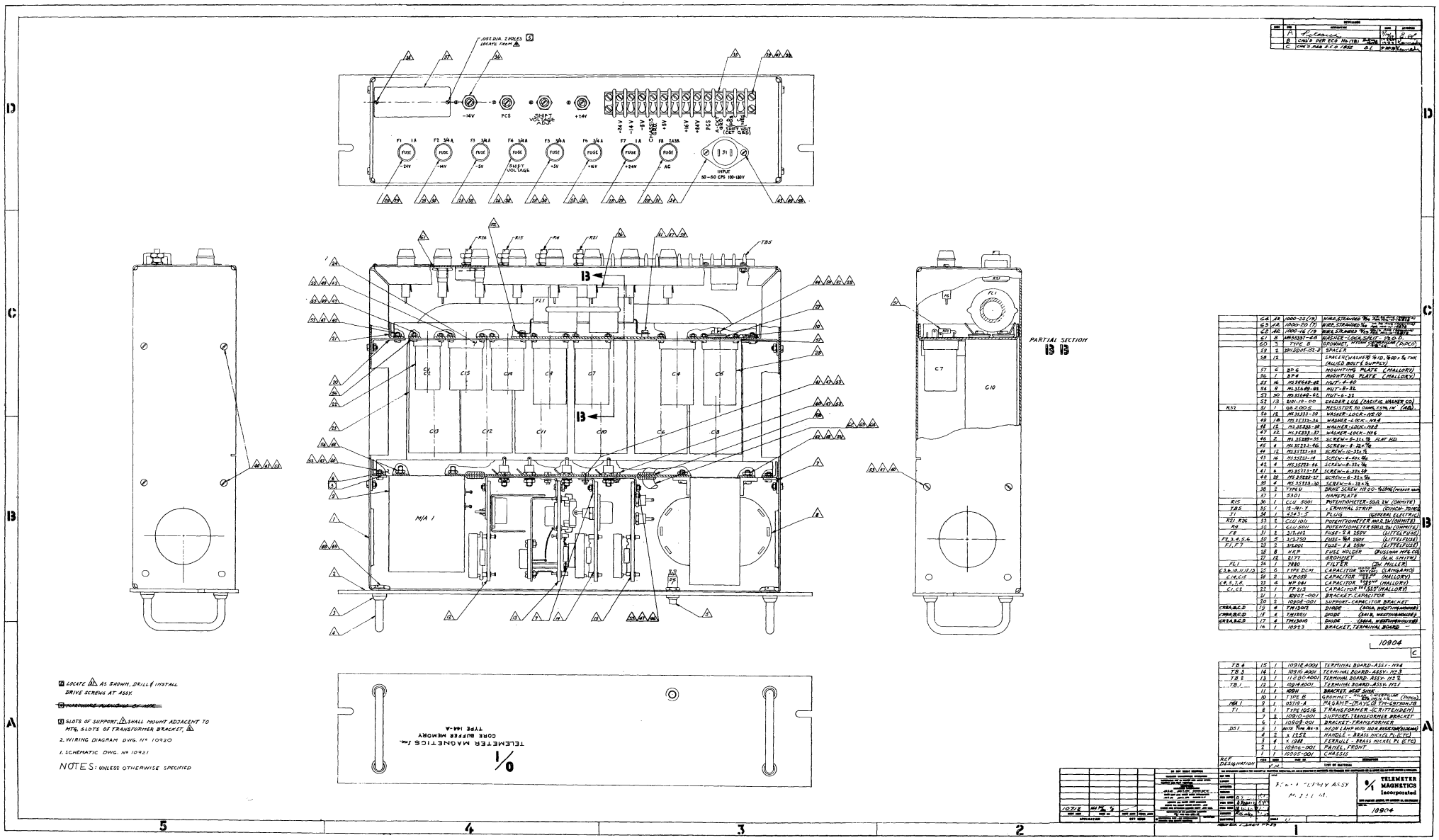


Figure 5-16. Power Supply, Parts Identification

SECTION VI

DRAWINGS

6-1. GENERAL.

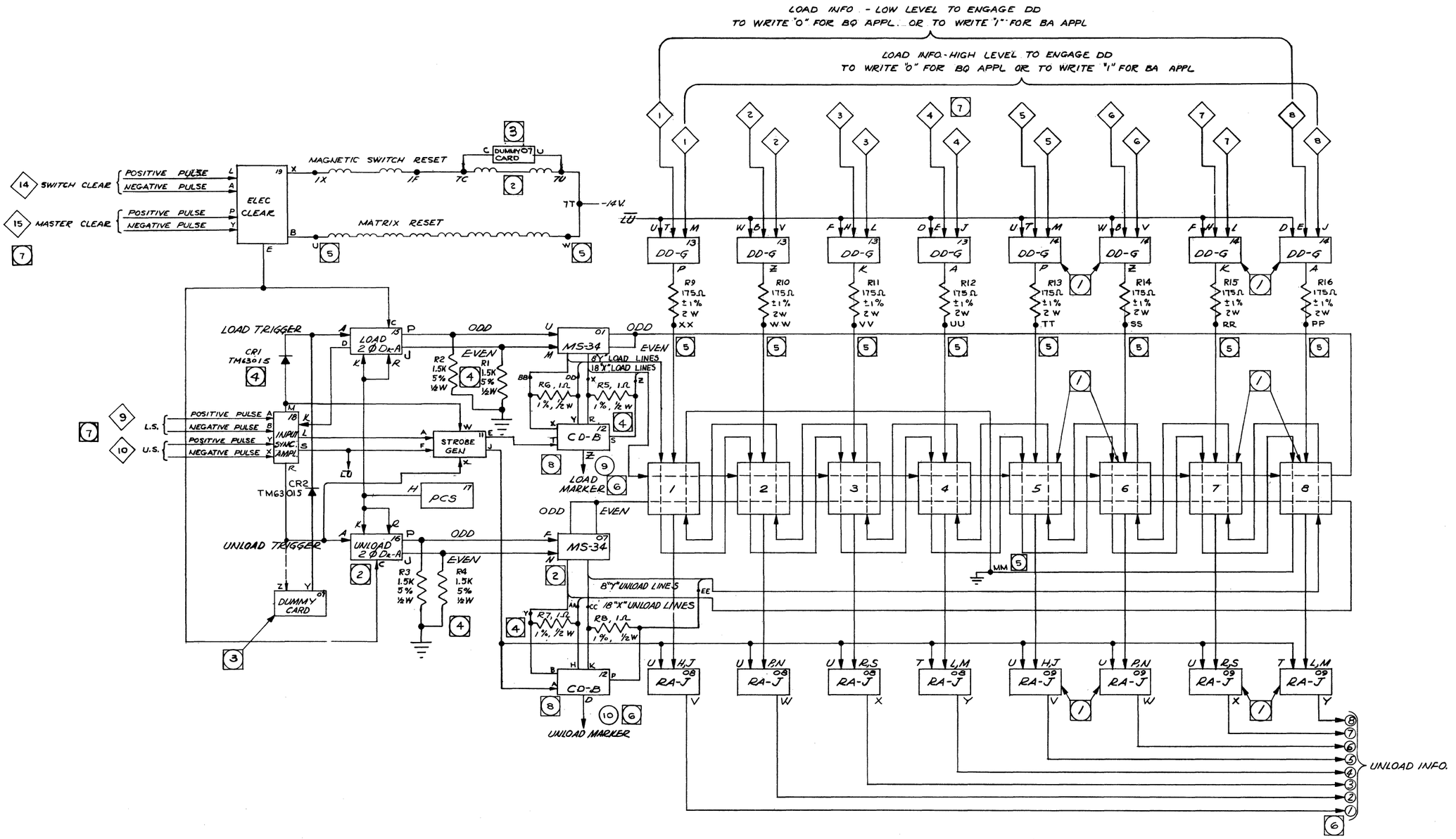
6-2. This section contains a functional block diagram and schematic diagrams for all circuits of the 144-A buffers. The block diagram covers all four buffers of the 144-A series with notations which show the basic differences between models.

6-3. The numerical designations in the blocks of Figure 6-1 indicate the physical location of the circuit within the buffer. Point-to-point wiring is shown for all signal lines by card designations at the line terminations.

6-4. Several of the schematic diagrams, Figures 6-2 through 6-13, show circuit wiring with respect to the buffer circuit (common) ground. This ground is located at terminal A of the power supply terminal strip, as well as at the ground terminals shown in Figures 6-1 through 6-13. Figure 6-12, the Power Supply Schematic Diagram, shows both the chassis and the circuit ground. Do not confuse these ground potentials while making voltage or oscilloscope checks.

6-5. Limited cross referencing between the separate schematic diagrams is achieved by the functional block diagram, Figure 6-1. The functional block diagram provides continuity for the schematic diagram signal inputs and outputs by identifying each functional block with its printed card name and number and placing a connector designation on each input and output.

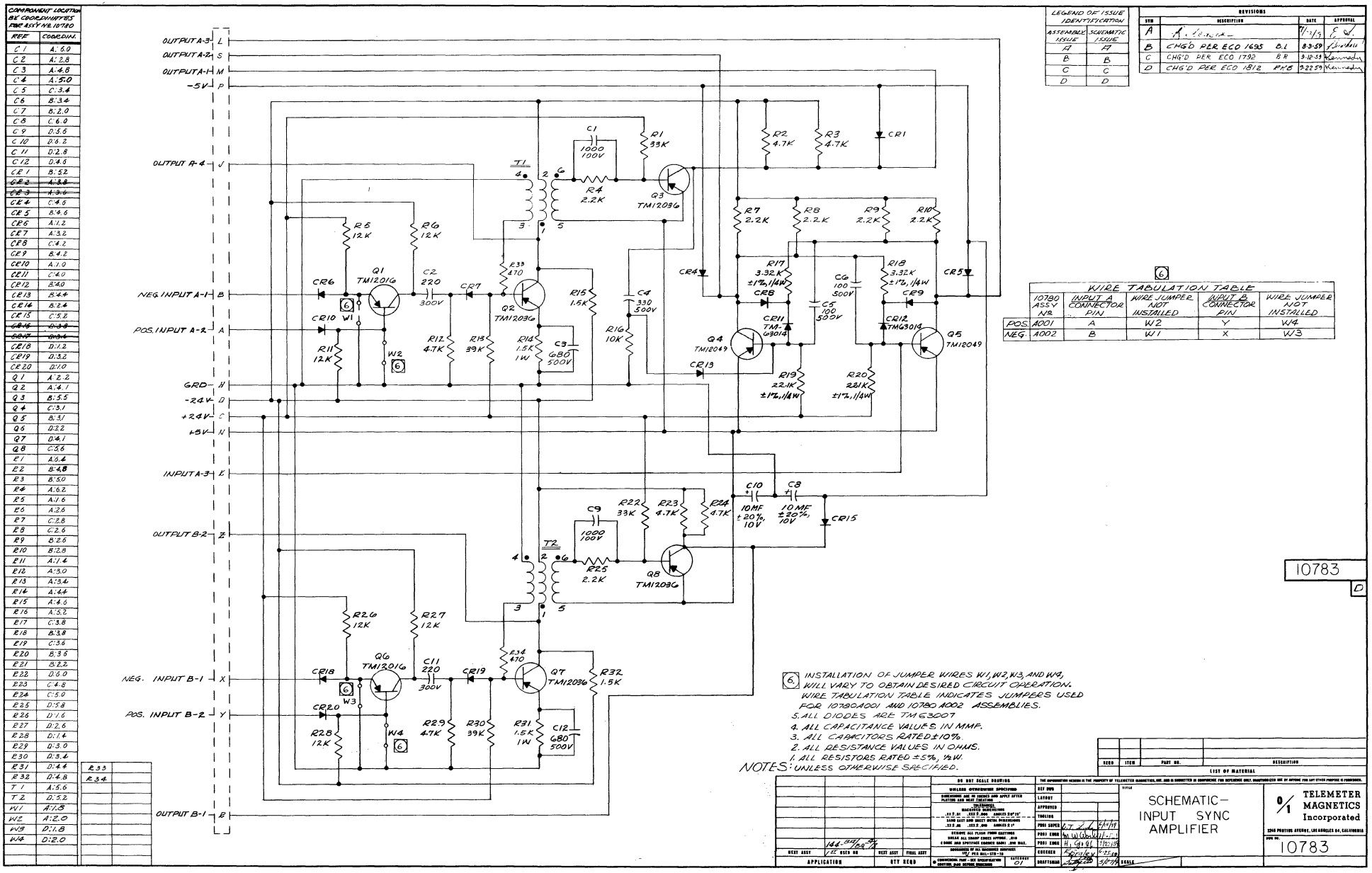
6-6. The following example will illustrate schematic cross-referencing. Figure 6-2, input sync amplifier schematic, shows the delayed sync signal output terminated at Pin M. Figure 6-1, functional block diagram, identifies the input sync amplifier as a functional block and shows the Pin M output connected to the load two phase driver, Pin A.



6 THIS CARD EXISTS ONLY WHEN MARKER IS REQUIRED
7 ◇ REFER TO INPUT PLUG PIN NOS.
6 ① REFER TO OUTPUT PLUG PIN NOS.
5 TERMINALS ON MAGNETICS ASSY MRE 425 CONNECTOR
4 ON TERMINAL BOARD.
3 THIS CARD EXISTS ONLY IN 144BA-4A AND 144 BA-8A BUT WIRING EXISTS IN ALL SYSTEMS.
2 THIS CARD EXISTS ONLY IN 144BQ-4A AND 144BQ-8A BUT WIRING EXISTS IN ALL SYSTEMS.
1 CIRCUITS WIRED BUT MATRIX PLANE AND PCB NOT INSTALLED IN 144 BQ-4A AND 144 BA-4A.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 6-1. Type 144-A Buffer, Block Diagram



COMPONENT LOCATION BY COORDINATES FOR ASSY NR. 10780	
REF	COORDIN.
C 1	A: 6.0
C 2	A: 2.8
C 3	A: 4.8
C 4	A: 5.0
C 5	C: 3.4
C 6	B: 3.4
C 7	B: 2.0
C 8	C: 6.0
C 9	D: 5.6
C 10	D: 6.2
C 11	D: 2.8
C 12	D: 4.6
CR 1	B: 5.2
~~CR 2~~	~~A: 3.8~~
~~CR 3~~	~~A: 3.6~~
CR 4	C: 4.5
CR 5	B: 4.6
CR 6	A: 1.2
CR 7	A: 3.2
CR 8	C: 4.2
CR 9	B: 4.2
CR 10	A: 1.0
CR 11	C: 4.0
CR 12	B: 4.0
CR 13	B: 4.4
CR 14	B: 2.4
CR 15	C: 5.2
~~CR 16~~	~~D: 3.8~~
~~CR 17~~	~~D: 3.6~~
CR 18	D: 1.2
CR 19	D: 3.2
CR 20	D: 1.0
Q 1	A: 2.2
Q 2	A: 4.1
Q 3	B: 5.5
Q 4	C: 3.1
Q 5	B: 3.1
Q 6	D: 2.2
Q 7	D: 4.1
Q 8	C: 5.6
R 1	A: 0.4
R 2	B: 4.8
R 3	B: 5.0
R 4	A: 6.2
R 5	A: 1.6
R 6	A: 2.6
R 7	C: 2.8
R 8	C: 2.6
R 9	B: 2.6
R 10	B: 2.8
R 11	A: 1.4
R 12	A: 3.0
R 13	A: 3.4
R 14	A: 4.4
R 15	A: 4.6
R 16	A: 5.2
R 17	C: 3.8
R 18	B: 3.8
R 19	C: 3.6
R 20	B: 3.6
R 21	B: 2.2
R 22	D: 6.0
R 23	C: 4.8
R 24	C: 5.0
R 25	D: 5.8
R 26	D: 1.6
R 27	D: 2.6
R 28	D: 1.4
R 29	D: 3.0
R 30	D: 3.4
R 31	D: 4.4
R 32	D: 4.8
T 1	A: 5.6
T 2	D: 5.2
W 1	A: 1.8
W 2	A: 2.0
W 3	D: 1.8
W 4	D: 2.0

R 33	
R 34	

LEGEND OF ISSUE IDENTIFICATION	
ASSEMBLY ISSUE	SCHEMATIC ISSUE
A	A
B	B
C	C
D	D

REVISIONS				
SYM	DESCRIPTION		DATE	APPROVAL
A	A. Release		7-23-59	E. W.
B	CHG'D PER ECO 1695	D.L	8-3-59	Kendall
C	CHG'D PER ECO 1792	B.R	9-12-59	Kennedy
D	CHG'D PER ECO 1812	R.K.S	9-22-59	Kennedy

6

WIRE TABULATION TABLE

10780 ASSY NR.	INPUT A CONNECTOR PIN	WIRE JUMPER NOT INSTALLED	INPUT B CONNECTOR PIN	WIRE JUMPER NOT INSTALLED
POS. A001	A	W2	Y	W4
NEG. A002	B	W1	X	W3

6. INSTALLATION OF JUMPER WIRES W1, W2, W3, AND W4, WILL VARY TO OBTAIN DESIRED CIRCUIT OPERATION. WIRE TABULATION TABLE INDICATES JUMPERS USED FOR 10780A001 AND 10780 A002 ASSEMBLIES.

NOTES:
5. ALL DIODES ARE TMG3007.
4. ALL CAPACITANCE VALUES IN MMF.
3. ALL CAPACITORS RATED ±10%.
2. ALL RESISTANCE VALUES IN OHMS.
1. ALL RESISTORS RATED ±5%, ½W.
UNLESS OTHERWISE SPECIFIED.

10783 D

REQD	ITEM	PART NR.	DESCRIPTION

LIST OF MATERIAL

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED

DEF ENG		
LAYOUT		
APPROVED		
TOOLING		
PROJ SUPER	D.T.	9/9/59
PROJ ENGR	W. Wilcox	9-11-59
PROJ ENGR	H. Gross	11-13-59
CHECKED	R. Spilker	9-23-59
DRAFTSMAN		9/9/59

SCALE

TITLE: SCHEMATIC— INPUT SYNC AMPLIFIER

0/1 TELEMETER MAGNETICS Incorporated
2248 PROTON AVENUE, LOS ANGELES 64, CALIFORNIA

DWG NR. 10783

NEXT ASSY | USED ON | NEXT ASSY | FINAL ASSY
APPLICATION | QTY REQD

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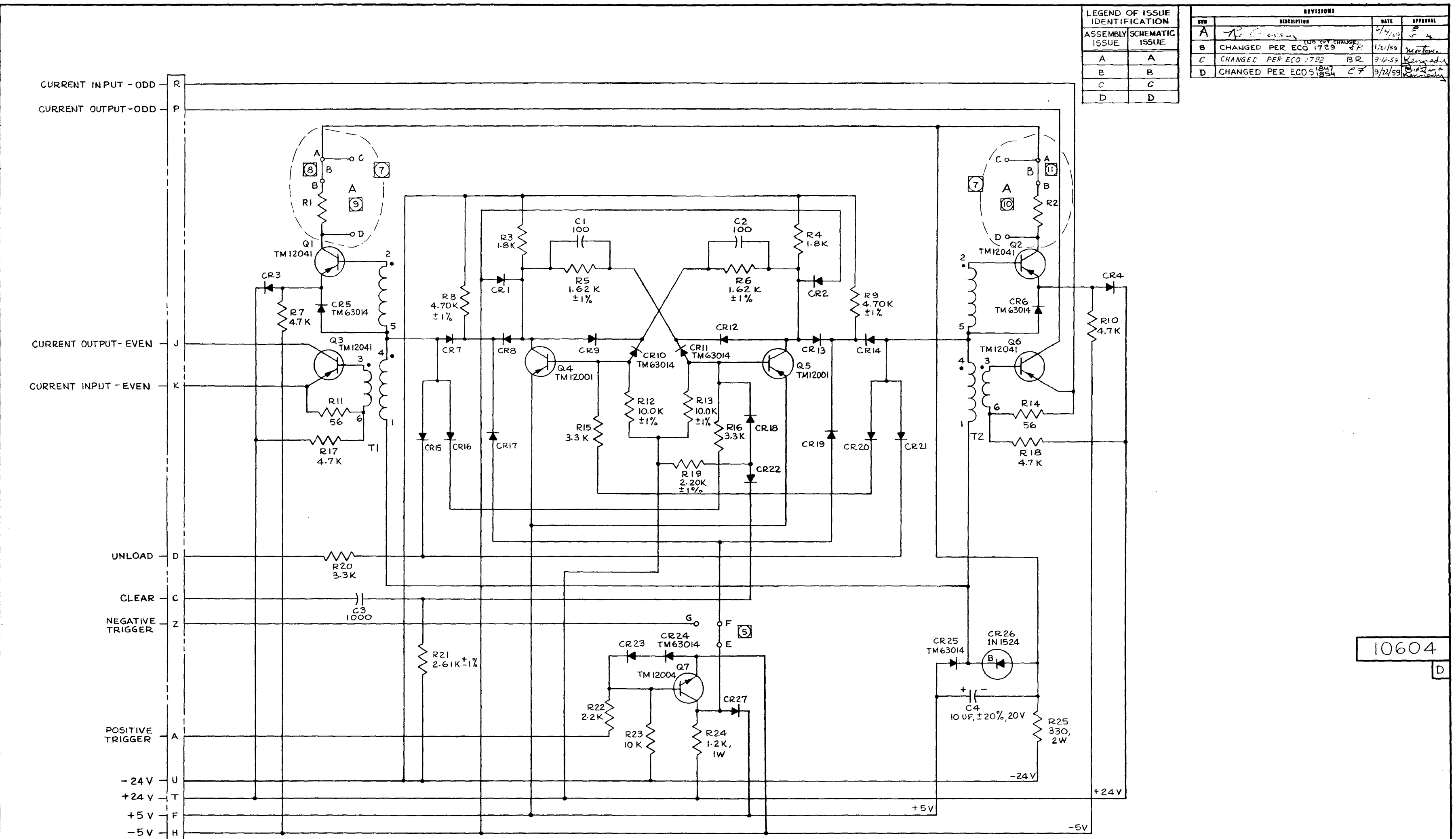
Figure 6-2. Input Sync Amplifier, Schematic Diagram

COMPONENT LOCATION BY COORDINATES FOR ASSY 10605

REF	COORDINATES
C1	A:5.8
C2	D:5.8
C3	B:5.2
C4	B:1.2
CR1	B:4.8
CR2	C:5.6
CR3	C:3.4
CR4	C:1.0
CR5	A:3.4
CR6	D:3.4
CR7	B:4.2
CR8	D:4.0
CR9	D:4.8
CR10	D:5.0
CR11	A:4.6
CR12	A:4.0
CR13	B:4.0
CR14	C:3.8
CR15	B:3.6
CR16	A:3.6
CR17	C:4.4
CR18	B:4.6
CR19	B:4.4
CR20	D:3.6
CR21	C:3.6
CR22	C:5.0
CR23	A:5.4
CR24	A:5.0
CR25	B:1.0
CR26	A:1.0
CR27	B:5.4
Q1	A:1.8
Q2	D:1.8
Q3	B:1.9
Q4	D:4.3
Q5	A:4.3
Q6	C:1.9
Q7	BC:6.2
R1	A:2.2
R2	D:2.2
R3	D:4.6
R4	C:5.4
R5	A:4.8
R6	D:5.4
R7	B:3.4
R8	C:4.2
R9	C:4.0
R10	B:1.0
R11	B:1.6
R12	D:5.2
R13	C:4.6
R14	C:1.6
R15	D:3.8
R16	A:3.8
R17	B:1.4
R18	C:1.4
R19	C:4.8
R20	B:3.8
R21	C:5.2
R22	A:5.6
R23	BC:5.9
R24	B:5.6
R25	D:1.1
8	A:2.4
9	A:2.6
10	D:2.6
11	D:2.4
T1	B:2.8
T2	C:2.8



6. ALL CAPACITORS RATED ±10%, 600 VDC.

5 FOR NEGATIVE TRIGGER, CONNECT POINTS 'F' & 'G' AND BREAK CONNECTION BETWEEN POINTS 'E' & 'F'.

4. FOR ASSY SEE DWG NO. 10605

3 ALL DIODES TYPE TM 63015

2. ALL RESISTORS RATED ±5%, ½W.

1. ALL RESISTANCE VALUES IN OHMS; ALL CAPACITANCE VALUES IN MICRO MICROFARADS.

NOTES: UNLESS OTHERWISE SPECIFIED.

7 POSSIBLE CONDITIONS AT CONNECTION POINTS 'A' & 'B' AND 'C' & 'D'.

(a) SPACE A CONTAINS A RESISTOR WHEN SPACE B CONTAINS A JUMPER.

(b) SPACE A EMPTY WHEN SPACE B CONTAINS A JUMPER.

(c) SPACE A EMPTY WHEN SPACE B CONTAINS A RESISTOR. RESISTOR VALUES DETERMINED AT ASSY.

144-BQ-8A

APPLICATION | QTY REQD

LIST OF MATERIAL

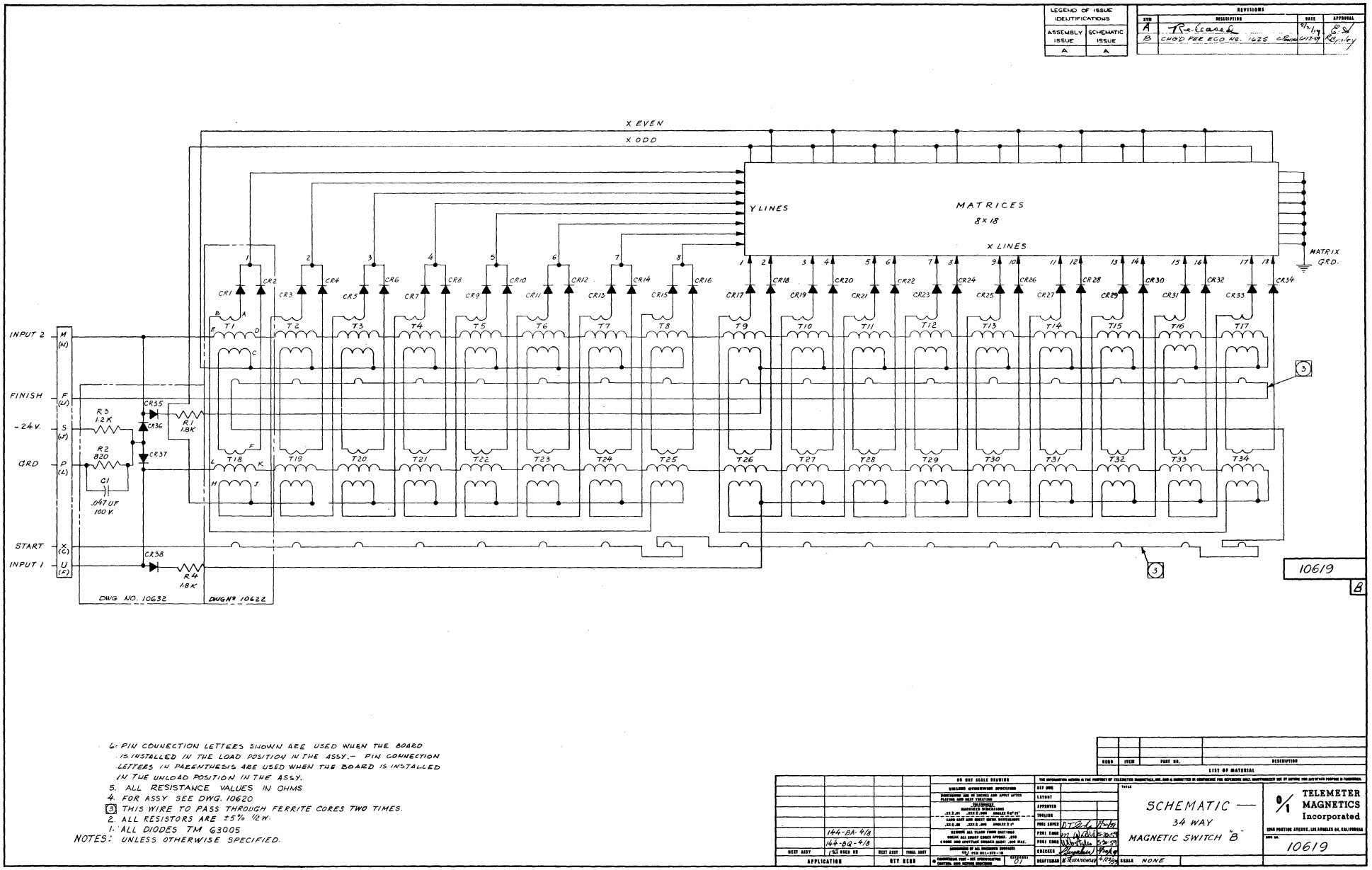
SCHEMATIC - 2 PHASE DRIVER 'A'

TELEMETER MAGNETICS Incorporated

10604

SCALE NONE

Figure 6-3. Two Phase Driver "A", Schematic Diagram



6. PIN CONNECTION LETTERS SHOWN ARE USED WHEN THE BOARD IS INSTALLED IN THE LOAD POSITION IN THE ASSY.- PIN CONNECTION LETTERS IN PARENTHESIS ARE USED WHEN THE BOARD IS INSTALLED IN THE UNLOAD POSITION IN THE ASSY.
5. ALL RESISTANCE VALUES IN OHMS
4. FOR ASSY SEE DWG. 10620
3. THIS WIRE TO PASS THROUGH FERRITE CORES TWO TIMES.
2. ALL RESISTORS ARE ±5% 1/2 W.
1. ALL DIODES TM G3005

NOTES: UNLESS OTHERWISE SPECIFIED.

LEGEND OF ISSUE IDENTIFICATIONS	
ASSEMBLY ISSUE	SCHEMATIC ISSUE
A	A

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	TR-Learch	8/24/67	
B	CHGD PER ECO NR. 1625	6/12/69	

LIST OF MATERIAL			
BOARD	ITEM	PART NO.	DESCRIPTION

TITLE	SCHEMATIC — 34 WAY MAGNETIC SWITCH "B"
SCALE	NONE
	0/1 TELEMETER MAGNETICS Incorporated
	10619

Figure 6-4. Magnetic Stepping Switch, Schematic Diagram

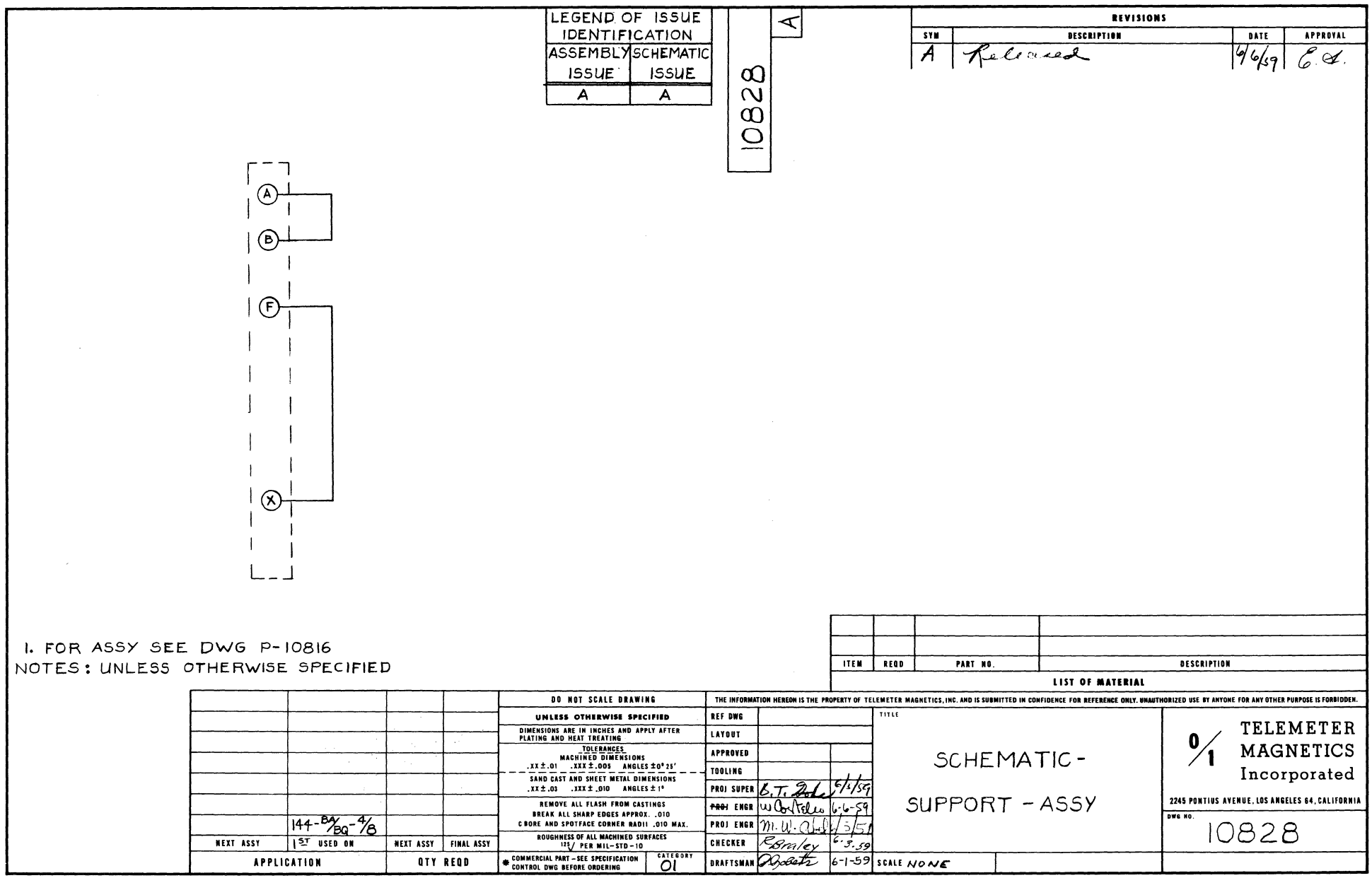


Figure 6-5. Dummy Circuit Card, Schematic Diagram

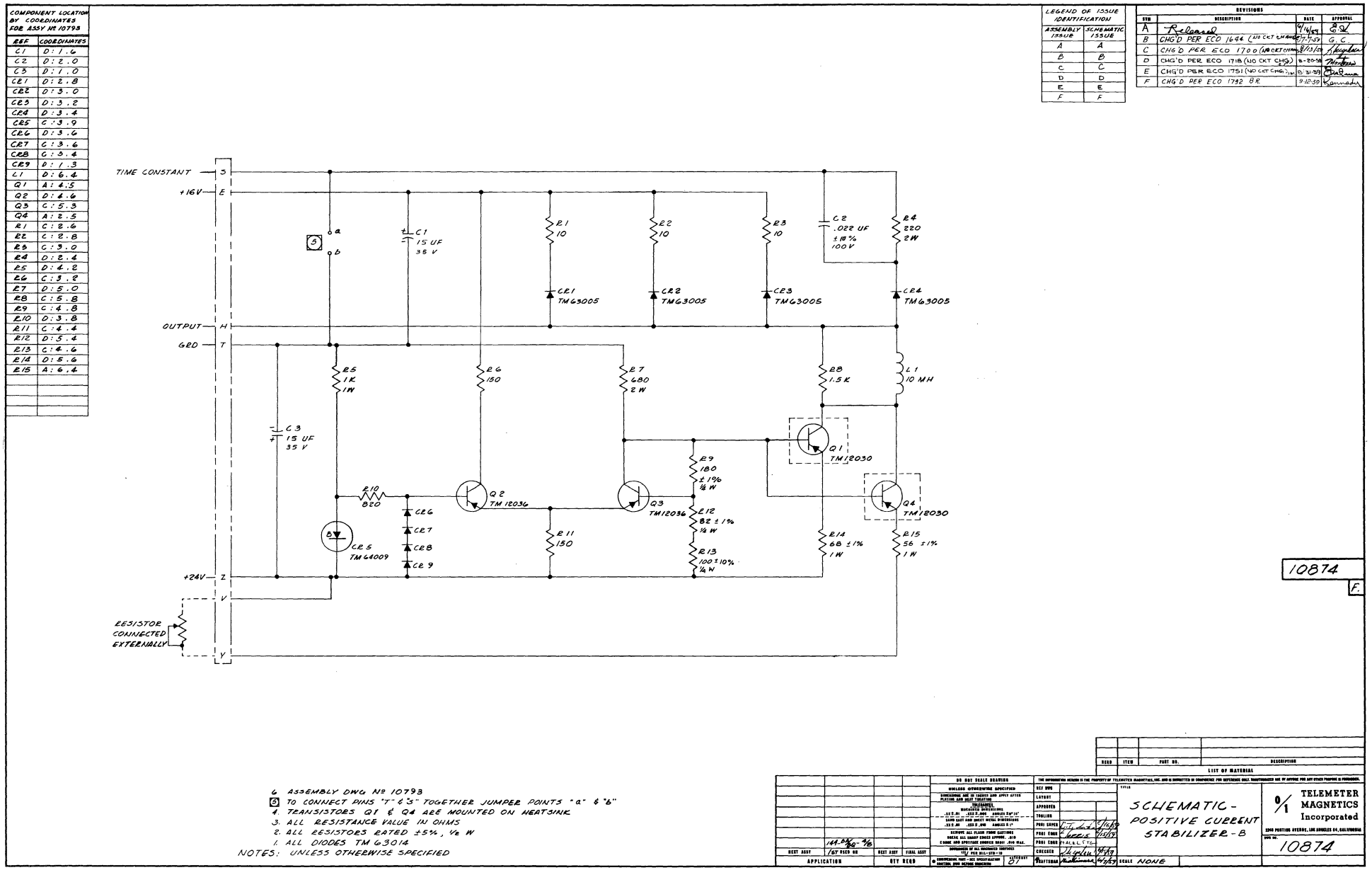


Figure 6-6. Positive Current Stabilizer, Schematic Diagram

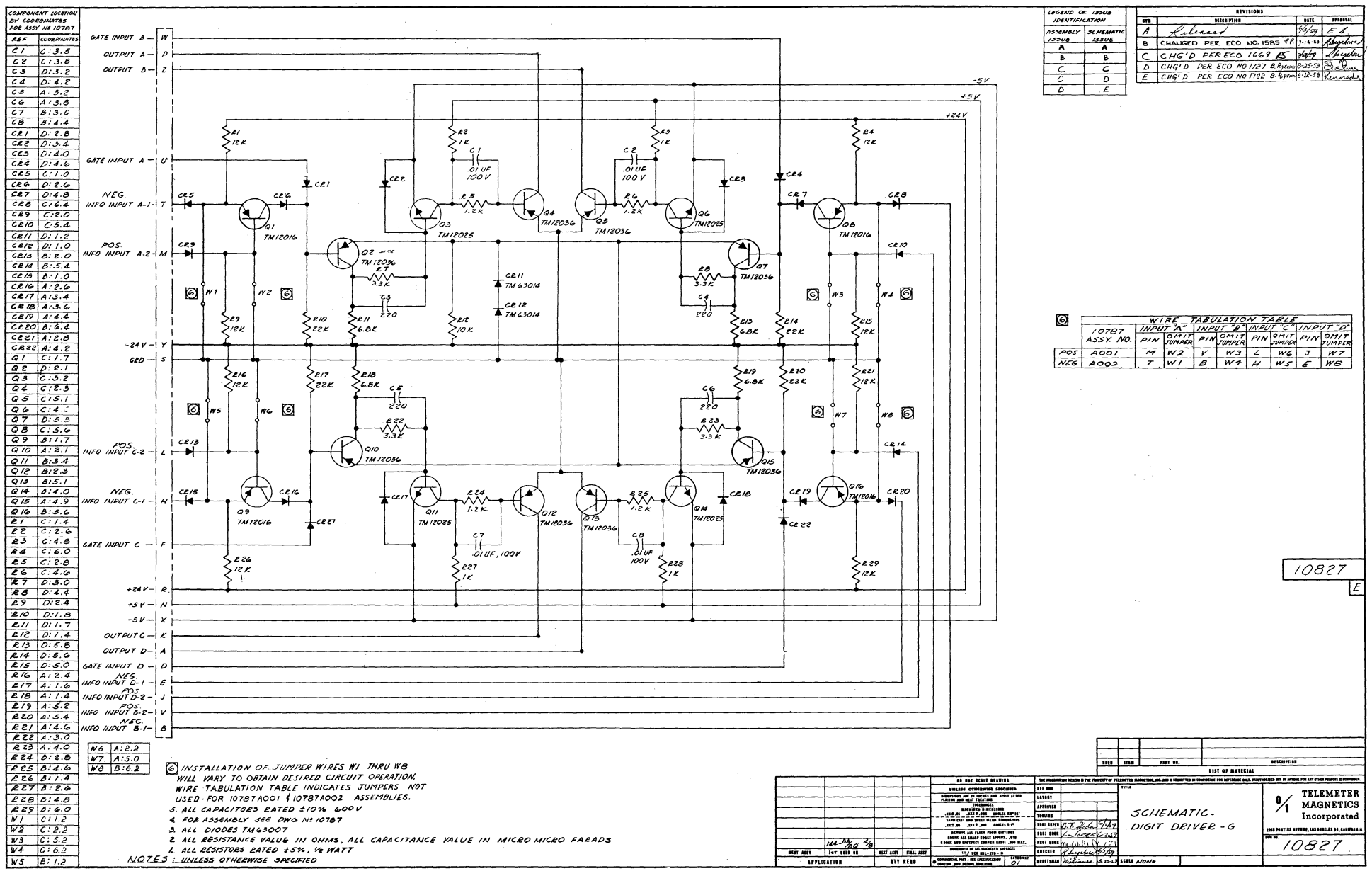


Figure 6-7. Digit Driver "G", Schematic Diagram

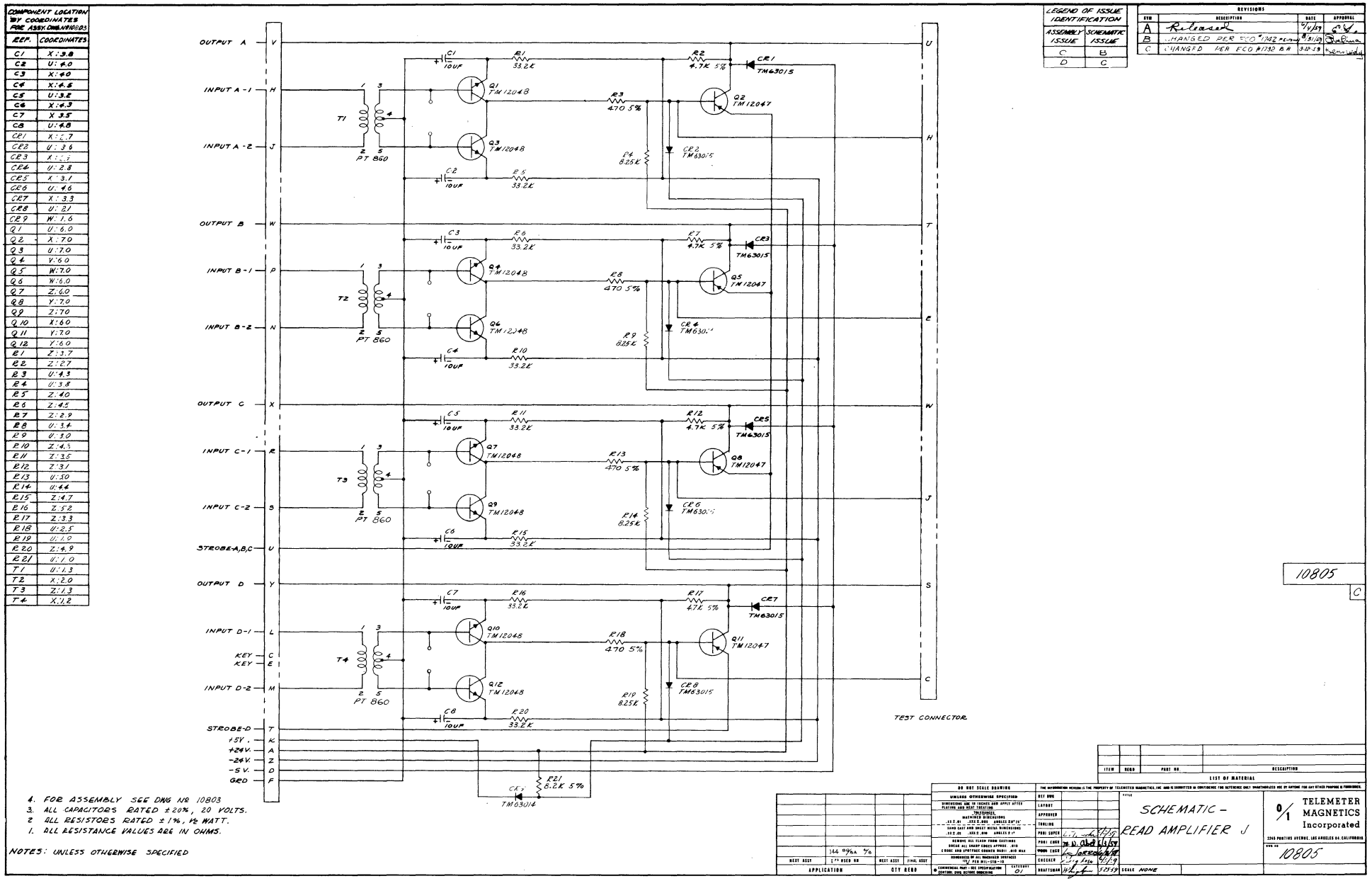


Figure 6-8. Read Amplifier "J", Schematic Diagram

COMPONENT LOCATION BY COORDINATES FOR ASSY NO 10960	
REF	COORDINATES
C-1	BC:4.8
2	C:5.5
3	A:4.4
4	A:1.2
5	B:3.8
6	D:5.8
7	D:4.6
8	C:3.8
9	BC:4.6
10	D:4.4
11	D:1.2
CR 1	B:5.0
2	B:6.0
3	B:4.4
4	A:1.4
5	A:3.2
6	A:5.0
7	A:4.6
8	D:4.8
9	B:4.0
10	B:6.2
11	D:6.2
12	D:5.6
13	D:5.4
14	D:3.4
15	D:4.2
16	D:1.4
17	D:3.2
Q 1	A:3.8
2	B:1.7
3	B:1.2
4	A:6.0
5	C:1.7
6	C:1.2
R 1	A:3.4
2	A:4.2
3	A:2.8
4	B:3.2
5	A:1.6
6	B:2.9
7	A:4.8
8	B:6.4
9	D:6.4
10	C:5.0
11	B:4.2
12	D:5.2
13	A:6.4
14	C:5.9
15	B:3.4
16	B:3.6
17	C:5.2
18	D:6.0
19	C:3.6
20	C:3.4
21	D:1.6
22	C:4.2
23	D:3.6
24	C:3.2
25	C:2.9
T 1	A:5.5
2	A:2.2
3	D:2.2

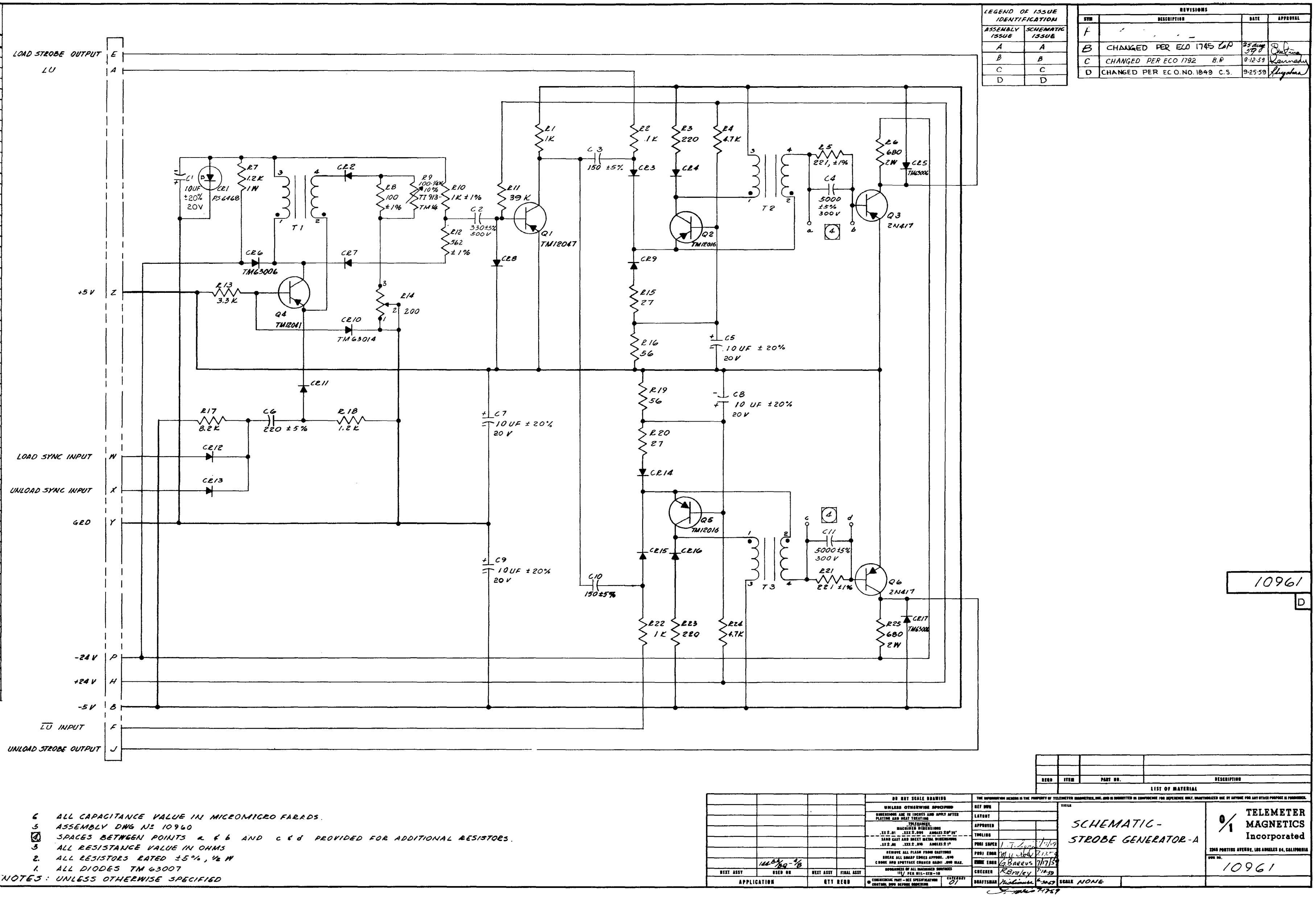


Figure 6-9. Strobe Generator "A", Schematic Diagram

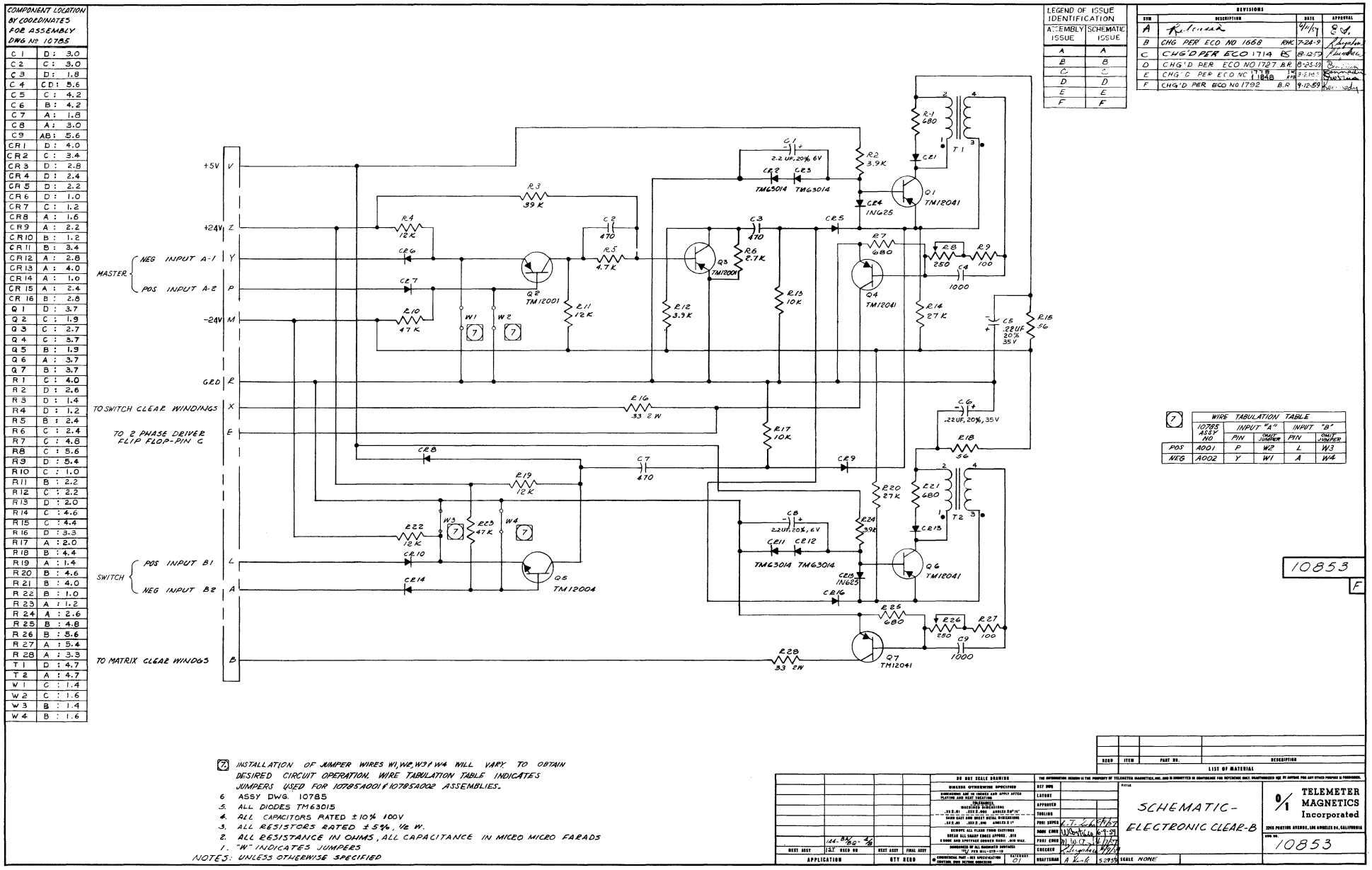


Figure 6-10. Electronic Clear "B", Schematic Diagram

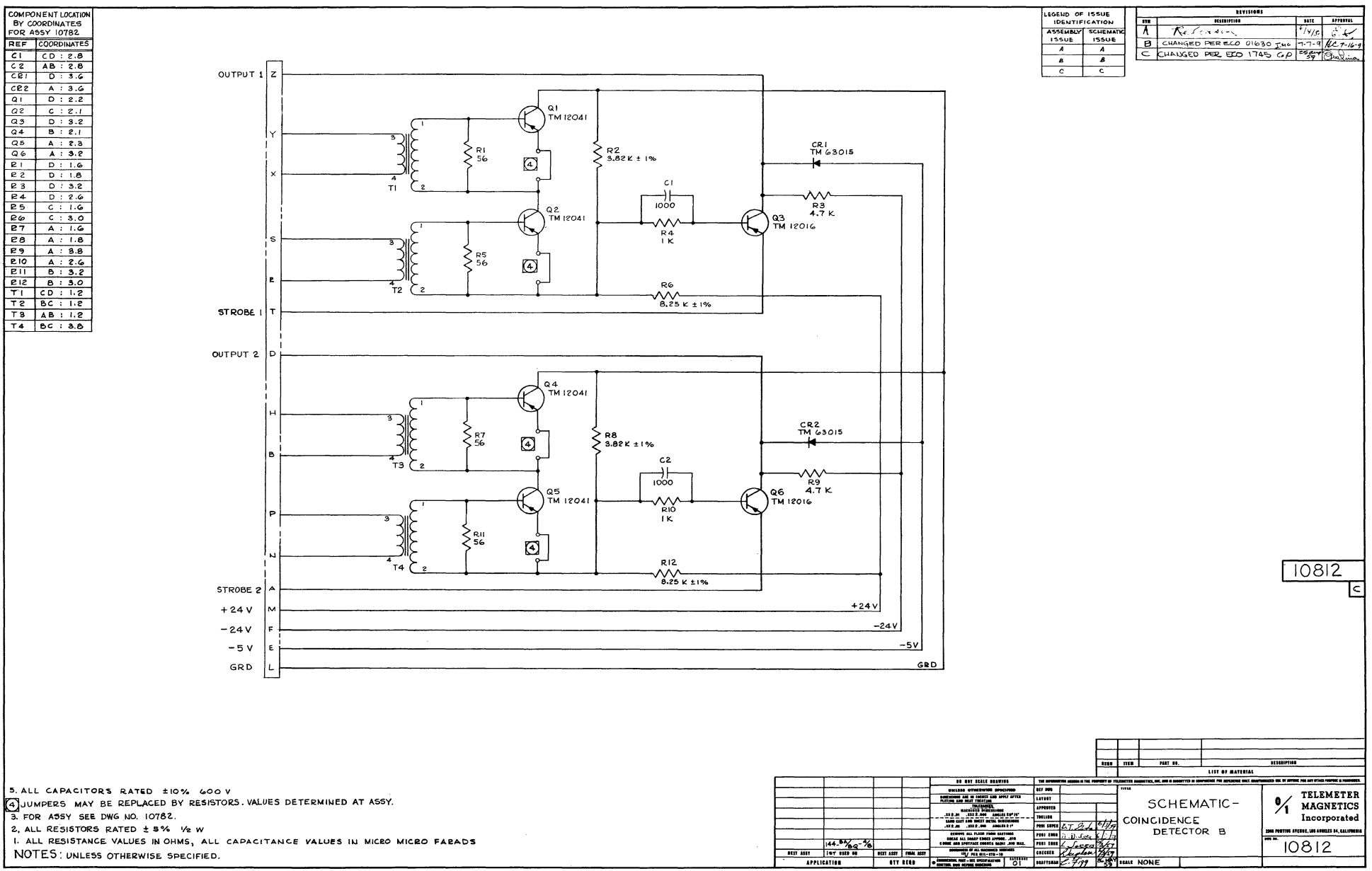
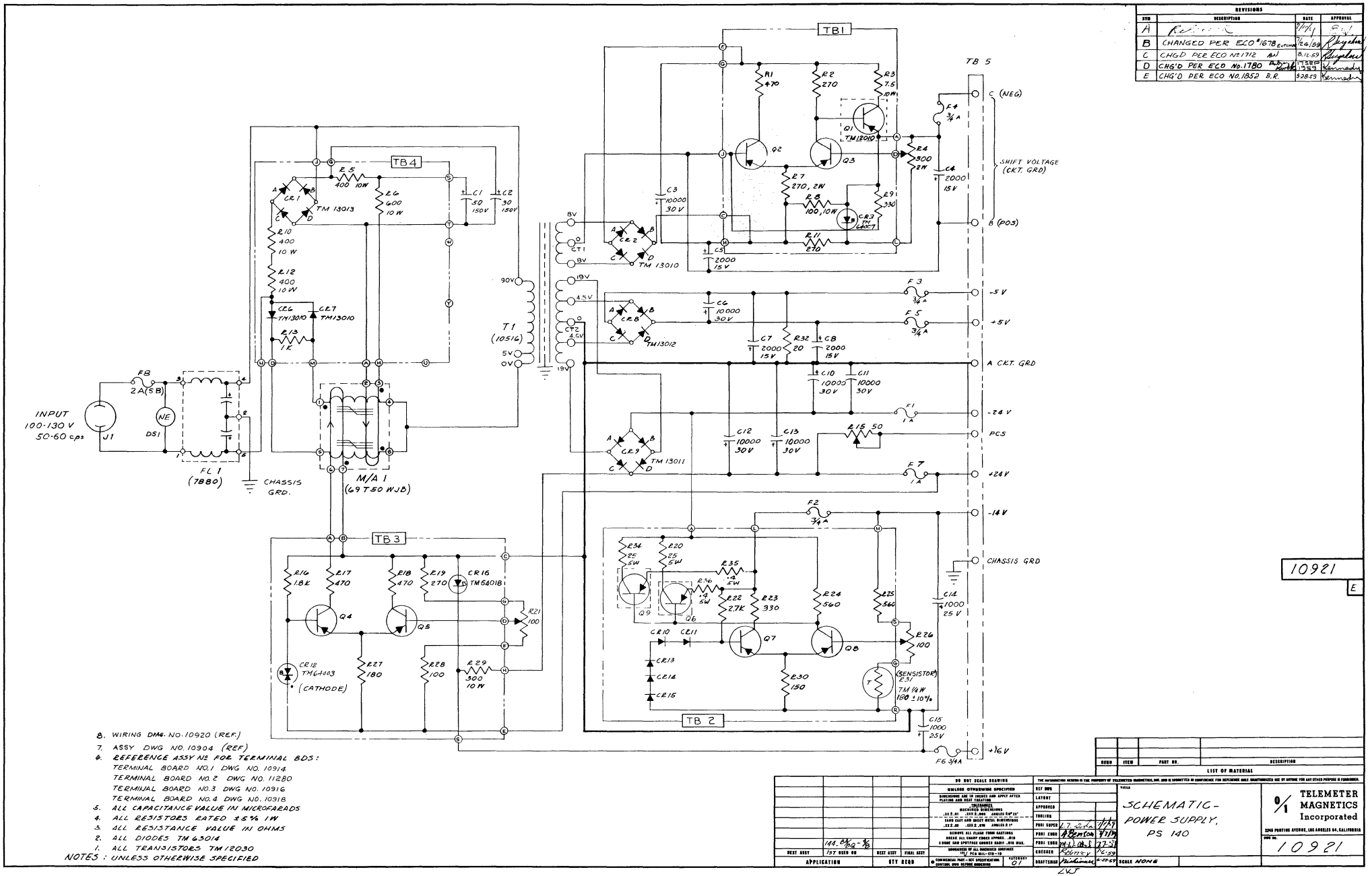


Figure 6-11. Coincidence Detector "B", Schematic Diagram



REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	Rel	7/7/61	
B	CHANGED PER ECO #1678	7/24/68	Ringelstein
C	CHG'D PER ECO NO 1712	8.16.69	Ringelstein
D	CHG'D PER ECO NO.1780	11-28-68 1-3-69	Kennedy
E	CHG'D PER ECO NO.1852 B.R.	9.28-69	Kennedy

8. WIRING DIAG. NO. 10920 (REF.)
7. ASSY DWG NO. 10904 (REF)
6. REFERENCE ASSY Nº FOR TERMINAL BDS:
   TERMINAL BOARD NO.1 DWG NO. 10914
   TERMINAL BOARD NO.2 DWG NO. 11280
   TERMINAL BOARD NO.3 DWG NO. 10916
   TERMINAL BOARD NO.4 DWG NO. 10918
5. ALL CAPACITANCE VALUE IN MICROFARADS
4. ALL RESISTORS RATED ±5% 1W
3. ALL RESISTANCE VALUE IN OHMS
2. ALL DIODES TM 63014
1. ALL TRANSISTORS TM 12030

NOTES : UNLESS OTHERWISE SPECIFIED

ITEM	PART NO.	DESCRIPTION
		LIST OF MATERIAL

DO NOT SCALE DRAWING

NEXT ASSY	137 USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

REF DES	
LAYOUT	
APPROVED	
TOOLING	
PROJ SUPER	
PROJ ENGR	
PROJ ENGR	
CHECKED	
DRAFTSMAN	

CATEGORY 01

SCHEMATIC - POWER SUPPLY, PS 140

SCALE NONE

0/1 TELEMETER MAGNETICS Incorporated

10921

Figure 6-12. Power Supply PS140, Schematic Diagram