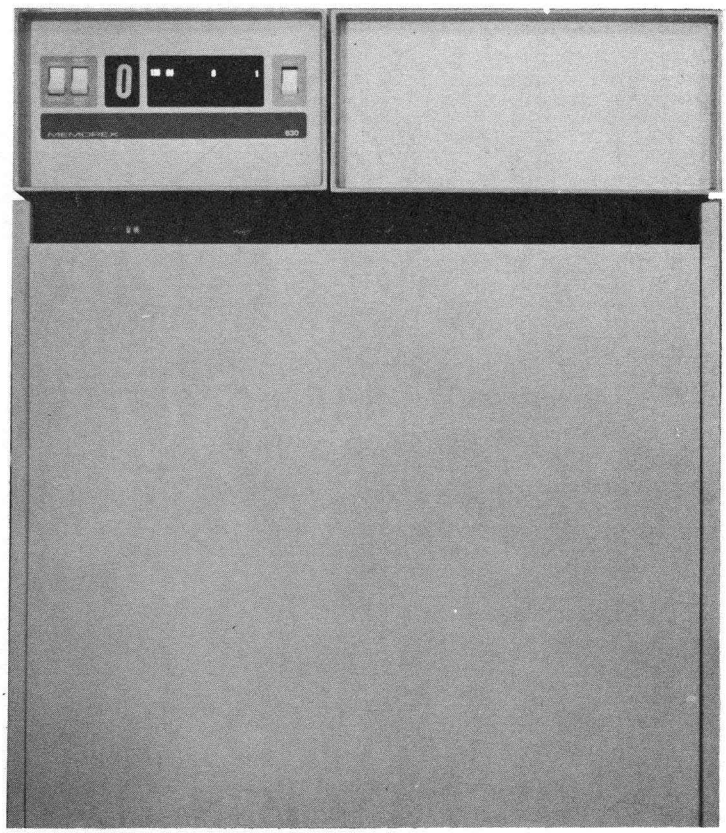

PRELIMINARY

Maintenance Manual

for

MEMOREX MODEL 630

DISC DRIVE

PREFACE

The purpose of this manual is to instruct customer engineers in the proper field maintenance of Memorex Model 630 disc pack drives. Procedures for installing one or more Model 630 drives are also included.

This manual contains a detailed description of the machine to aid in trouble-shooting as well as in performing periodic maintenance routines. Necessary tools for performing tests and making adjustments are also described.

If it becomes necessary to replace an assembly or part, refer to the spare parts list for the part number and instructions for ordering a replacement.

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Requests for additional copies of this manual should be sent to the attention of Technical Publications, MEMOREX Equipment Group, San Tomas at Central Expressway, Santa Clara, California 95052

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ILLUSTRATIONS

ILLUSTRATIONS (continued)

SECTION 1.0
INTRODUCTION

1.1 GENERAL

Peripheral Systems Corporation's Model 630 Series Disc Drive is a direct access disc pack storage unit. It reads and writes information on Memorex Mark I, IBM 1316 or equivalent disc packs.

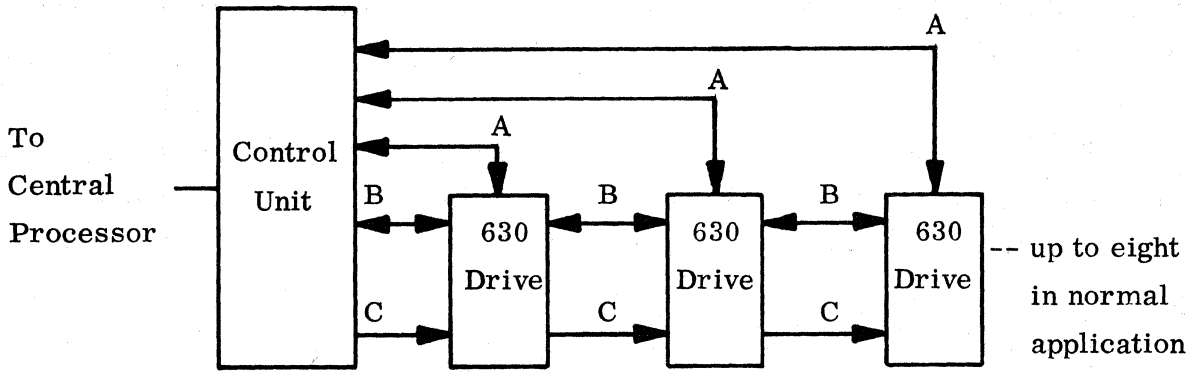
These disc packs serve as permanent or temporary information storage media which can be written on by one drive, removed and stored, and then installed on another drive with no loss of compatibility.

To record (write) and recover (read) information, a disc pack is installed on a Model 630 disc pack drive. The drive is responsible for performing the three basic operations: seek, read and write. To do this it must rotate the disc pack at the required speed (2400 rpm $\pm$ 2%), select one of 10 read/write heads for an operation and position it to the prescribed track on the disc surface (all 10 heads position to the same cylinder simultaneously, but only one head is selected to read or write at a time). The drive allows the controller to synchronize read/write operations by referencing to an index on the disc pack.

Model 630 drives receive commands and data from the central processing unit through a controller. Up to eight drives can communicate with the same controller. Figure 1-1 is a simple block diagram showing the system configuration when more than one drive is connected to a single controller.

AC power is supplied externally and, in the typical installation, also comes from the controller (as shown in Figure 1-1). There are two configurations of the Model 630 drive (A and B) to accommodate either 60- or 50-Hz power supplies. Details of ac power requirements are given in Section 2.3.2.

Standard Model 630 drives are completely compatible with the IBM 2841 controller. These drives employ the second level of a two-level interface concept which has been incorporated into the Model 630 interface design. All cables and connectors necessary to communicate with an IBM 2841 are available in second-level drives.



A - DC, data and select lines
B - SIGNAL lines
C - AC and sequence lines

System Configuration

Figure 1-1

However, Model 630 drives include self-contained dc power supplies and do not depend on the controller for dc power.* For this reason, certain pins are not used. These pins and the dc power supply are described in more detail in Sections 2.3.2 and 2.3.5.

First-level interfaces are custom designed to meet the special requirements of non-2841 controllers. Standard voltage levels on first-level interface connectors are +5 volts for logical one and 0 volts for logical zero. Exceptions to this are identified in the appropriate pin connection lists in Section 2.3.2.

---

* Except for special terminator power which is supplied by the dc line from the controller.

1.2 STORAGE MEDIA

Memorex Mark I, IBM 1316 or equivalent disc packs serve as the storage media for the Model 630. Figure 1-2 shows the recording discs, slotted index/sector disc on the bottom of the pack and top and bottom protective pack covers.

Each pack consists of six aluminum discs coated with a magnetic oxide and mounted one-half inch apart on a common hub. Information is recorded on the 10 inner disc surfaces in the form of polarized magnetic particles called bits. The bits are recorded on 203 concentric circles (track 000 to track 202) on each disc surface. Corresponding tracks on all 10 surfaces are considered information cylinders; there are 203 cylinders per pack. Cylinders 200, 201 and 202 are ordinarily reserved as spares under the control of initialization routines.

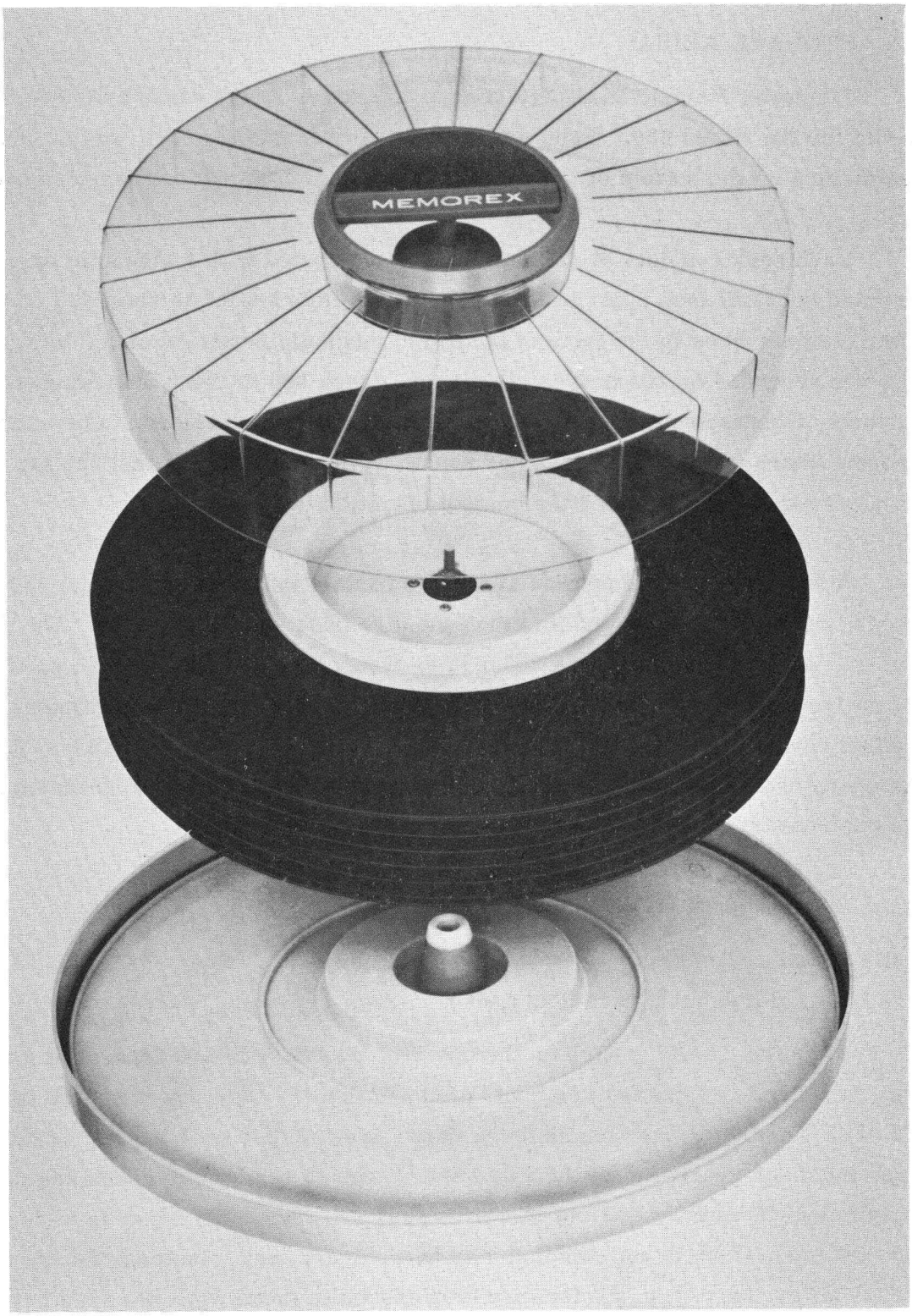
A Memorex Mark I or IBM 1316 disc pack is installed on a Model 630 by raising the cabinet cover and lowering the disc pack onto the spindle. The discs are secured to the spindle with 206 $\pm$32 lb of force by twisting the disc pack handle clockwise. Once the discs are secured, the disc pack cover can be removed, the cabinet cover closed and the machine started by depressing the START switch on the operator control panel. Interlocks prevent the drive motor from starting until the pack cover has been removed and the cabinet cover closed.

1.3 BASIC DRIVE OPERATIONS

1.3.1 Seek

1.3.1.1 First Seek (to cylinder 000)

When the START switch on the operator control panel is depressed (assuming that the drive is connected to a controller and that its main power switch is closed), power is supplied to the spindle drive motor and the disc pack begins rotating. Once the discs reach 70% of the rated speed, the 10 read/write heads are positioned to cylinder 000 (home position) in a first seek sequence. This begins with a forced forward seek which is not completed as in a normal seek. Instead, the carriage moves all the way out to the forward stop and waits there while the simulated seek command continues for 800 ms. When the delay times out, a reverse seek of 204 cylinders is initiated which detents the carriage at cylinder 000. At 2.5 ms after



Memorex Mark I Disc Pack
Figure 1-2

the detent engages, the drive signals the controller that it is ready for further instructions, Ordinarily, this would mean a seek command to some cylinder where one head would be selected to read or write information.

1.3.1.2 Seeks Other Than First Seek

The controller initiates a seek by sending the address of the cylinder scheduled for the next seek to the drive where that address is compared with the address of the cylinder at which the heads are presently positioned. The computed difference between the two addresses represents the number of cylinders the heads must travel. Comparison logic also determines which direction the heads must move. Once the cylinder scheduled for the next seek has been selected, the controller selects one of the 10 heads by diode switching.

Meanwhile, the difference count is converted by the drive into an analog voltage which powers the linear positioning motor. Before the difference count voltage reaches the linear positioning motor, however, it is compared with a speed sense voltage supplied by a tachometer located in the positioning motor. This comparison is made by a servo amplifier to control the voltage supplied to the positioning motor so that the access speed of the heads is controlled.

The detent is then pulled, a 300-ms delay is started, and the linear positioning motor moves the heads to the new cylinder. The purpose of the delay is to provide a time check on the positioning system. If the carriage does not reach the new cylinder and detent within the 300 ms, a seek incomplete signal is sent to the controller. See Sections 2.3.5 and 3.0 for details.

During a normal seek, access control circuitry monitors the position of the heads constantly by a cylinder transducer which sends a pulse to the present address register each time a new cylinder is reached by the heads. Each pulse increases or decreases (depending on direction of travel) the present address by one which causes the difference count to decrease. When the difference count reaches zero, the detent engages and the heads stop at the prescribed cylinder.

After a 2-1/2-ms damping delay times out, the drive signals the controller that it is ready for a read or write operation.

1.3.2 Write Operation

Writing is performed by a magnetic recording head which flies close to the surface of the disc while the disc rotates rapidly under it.

The controller sends data to the drive using the double-frequency nonreturn-to-zero technique. Clock pulses supplied by the controller synchronize recording of the data pulses. Every 800 ns (called a bit cell time) a clock pulse is recorded. If no other pulse is recorded between two clock pulses, that bit cell time represents a logical zero. Two pulses recorded during a bit cell time (every 400 ns) represent a logical one.

The pulses are recorded as magnetic flux reversals in a track 0.008-inch wide. An erase gap, which follows the write gap by 0.045 inch, erases the edges of the written track and narrows it to a width of 0.005 inch. This process, called tunnel erasing, prevents track-to-track smearing.

The data track will now remain on the disc surface until erased and can be read at any time.

1.3.3 Read Operation

The same head poles used to write the data track are used to read it. The magnetic flux changes recorded on the disc surface cause current reversals in the two center-tapped read coils. The current reversals are converted to an output signal which is transmitted to the controller. The recorded clock pulses serve as a built-in clock for the transmitted data.

SECTION 2.0
MACHINE DESCRIPTION

This section is devoted to a description of the Model 630 disc pack drive from three viewpoints.

A. Machine parameters

B. Machine assemblies and parts

C. Functional areas

2.1 MACHINE PARAMETERS

TABLE 2-I
BASIC MACHINE PARAMETERS

Capacity	
Maximum disc pack capacity, 8-bit bytes	7.25 million
Bits available to a single access	Over 288,000
Data Retrieval Times	
Rotational time, ms	25 (2400 rpm ± 2%)
Track-to-track position time, ms	20, maximum*
Average access time **, ms	50
Maximum access time, ms	80
Readback data cell time, ns	800, nominal
	1060, maximum
	550, minimum
Read data pulse width, ns	150, nominal
	200, maximum
	75, minimum

* This figure does not include average latency time of 12.5 ms due to rotation.

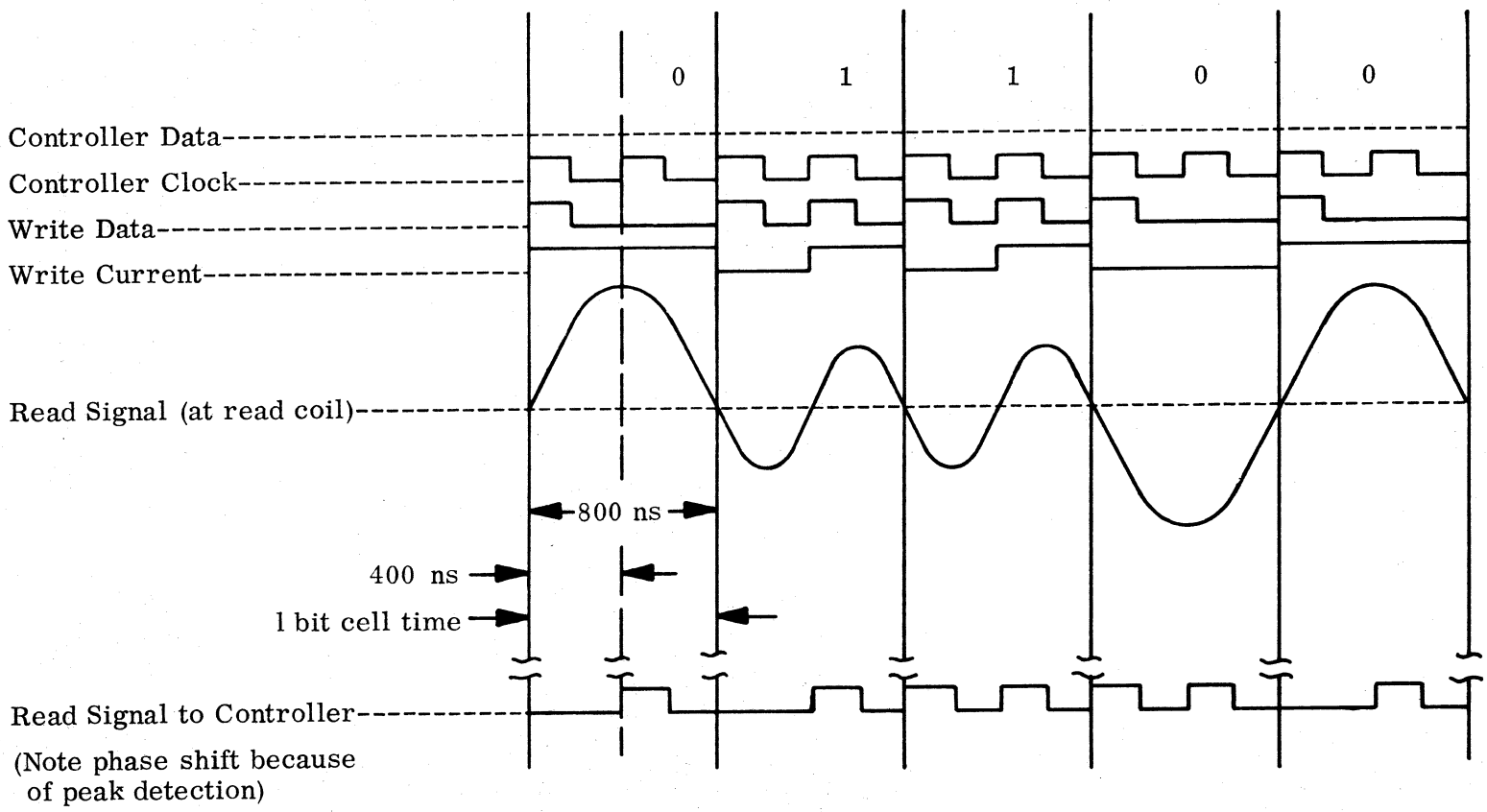
** Average access time = $\frac{\text{time to do all seeks}}{\text{number of seeks possible}}$

TABLE 2-I (continued)

BASIC MACHINE PARAMETERS (continued)

Write Operation	
Technique	Double-frequency, nonreturn to zero
Density, track 000, bits/inch (zero's rate)	765 (nominal)
Density, track 202, bits/inch (zero's rate)	1114 (nominal)
Logical 1 (write pulse frequency regulated by controller), MHz	2.5 * $\pm$0.3%
Logical 0 (clock pulse at beginning of bit cell time only), MHz	1.25 *
Data transfer rate, megabits/sec	1.25 (nominal)
Read Operation	
Double-frequency recording technique provides self-clocking read data	
Data is sent to controller as stream of binary bits	
Disc Pack Characteristics	
Number of recording discs	6
Number of recording surfaces	10
Tracks per surface	200 plus 3 spares
Recording discs' outside diameter, inches	14.030 +0.000 -0.010
Diameter of track 000, inches	13.012, nominal
Diameter of track 202, inches	8.928, nominal
Disc pack cover outside diameter, inches	14.55, maximum
Radial dimension of track 202 to reference, inches	4.464, nominal
Radial dimension of track 000 to reference, inches	6.506, nominal
Disc pack weight, lb	10 (approximate)
Coating material	Magnetic oxide

* See Figure 2-1



Summary of Basic Machine Parameters

Figure 2-1

TABLE 2-I (continued)

BASIC MACHINE PARAMETERS (continued)

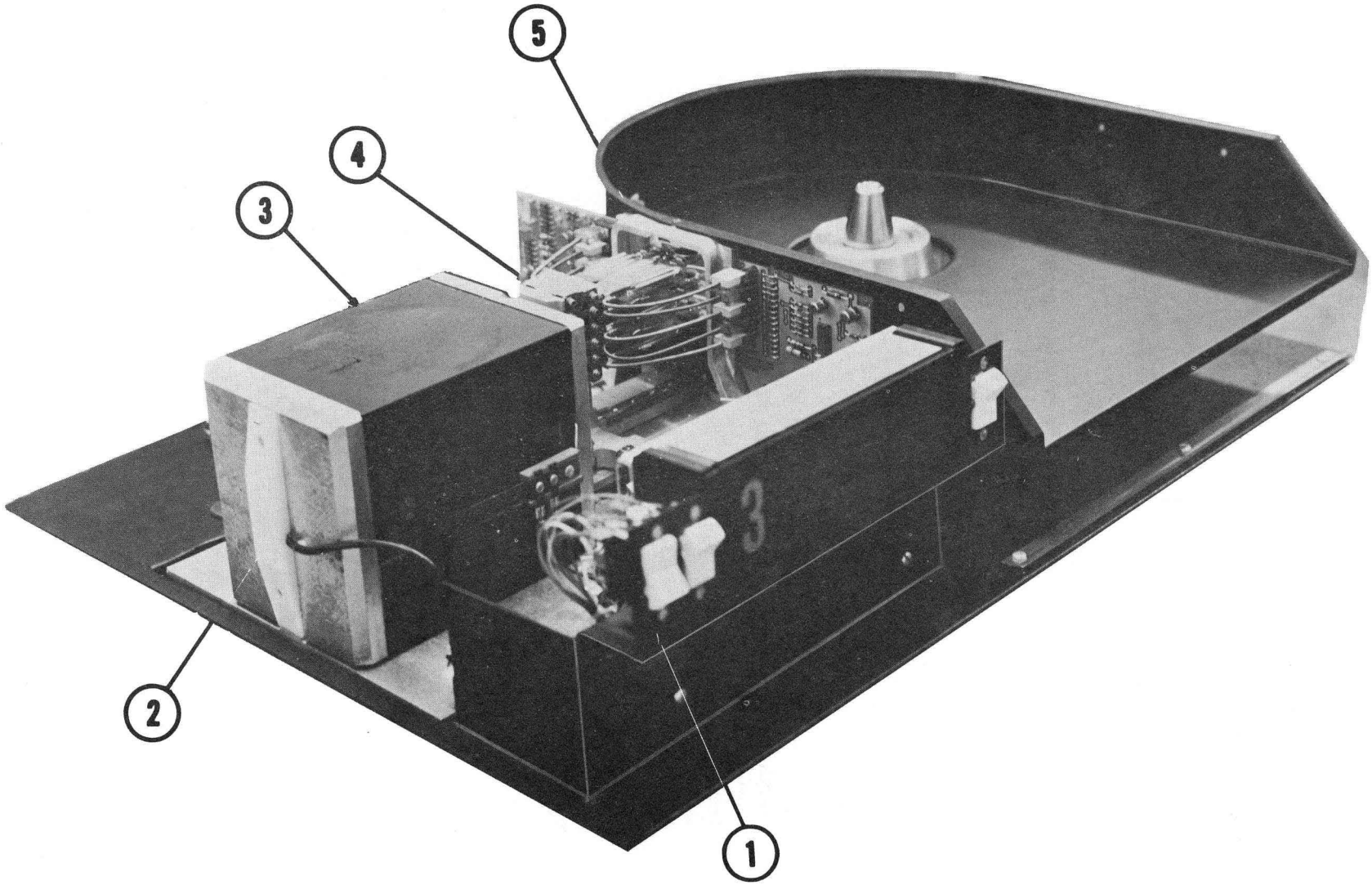
Heads	
Number of heads	10
Width of track as written, inches	0.008
Width of track when erased, inches	0.005
Track spacing center-to-center, inches	0.010
Operator Controls	ENABLE-DISABLE
	READ/WRITE - READ ONLY
	START - STOP
Overall Dimensions	
Width, inches	30
Depth, inches	24
Height, inches	38
Weight, lb	295
Environment	
Temperature range, ^{o}F *	60 to 90
Relative humidity range, %	8 to 80
Heat dissipation, BTU/hr	3500
Electrical Requirements (see Section 2.3.2)	
Model A ac power, vac, Hz	208/230, 60
Model B ac power, vac, Hz	220/380, 50
Phase	Receive 3-phase, use single-phase
DC power supply	Self-contained, except for special termination requirements
Maximum start current, amp	25
Maximum run current, amp	4.5

* Temperature changes less than 15^{o} per hour are acceptable.

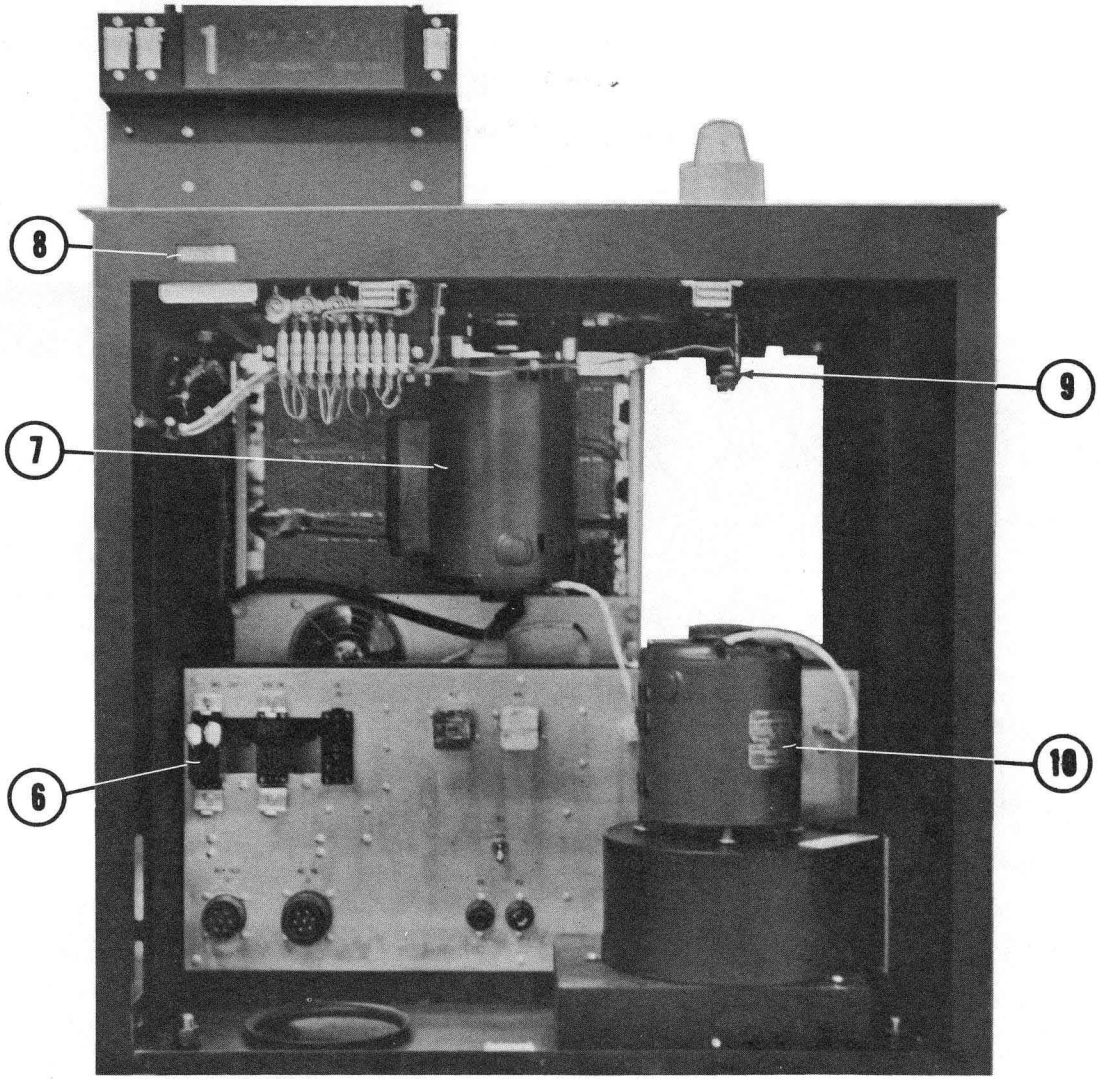
2.2 MACHINE ASSEMBLIES AND PARTS

Figures 2-2A through 2-2D illustrate a Model 630 without covers. The circled numbers call out assemblies and subassemblies which are cross referenced to the following lists:

A.	1.	Operator control panel
	2.	Tachometer (in armature behind nylon cap)
	3.	Linear positioning motor (armature within permanent magnet)
	4.	Carriage, carriage way and head-arm assembly
	5.	Cam tower and read/write amplifier cards
B.	6.	Interior control panel (connector side)
	7.	Spindle drive motor, pulley and motor mount
	8.	Running-time meter (or usage meter)
	9.	Pack-on switch
	10.	Cabinet blower
C.	11.	Interior control panel (access panel for maintenance)
	12.	Spindle pulley, belt and mechanical spindle lock
	13.	Logic card file (connector side)
	14.	Logic card file plenum (including pass-transistor regulator and logic card file fan)
	15.	DC power supply
D.	16.	Spindle (disc pack mounting surface)
	17.	Detent mechanism and cylinder transducer
	18.	Servo amplifier
	19.	Heads retracted/extended switch
	20.	Index transducer

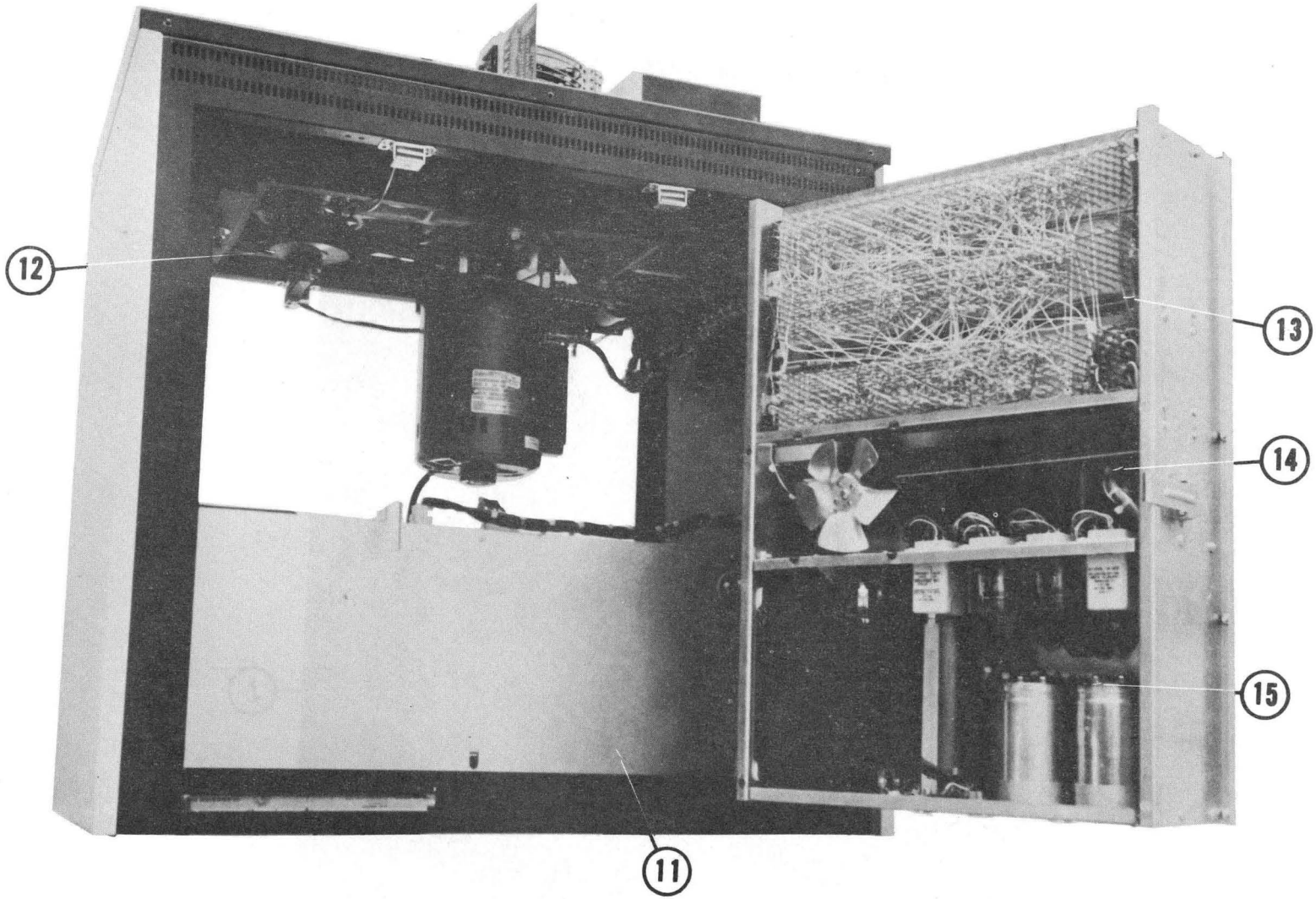


A
Machine Assemblies and Parts
Figure 2-2 (sheet 1 of 4)

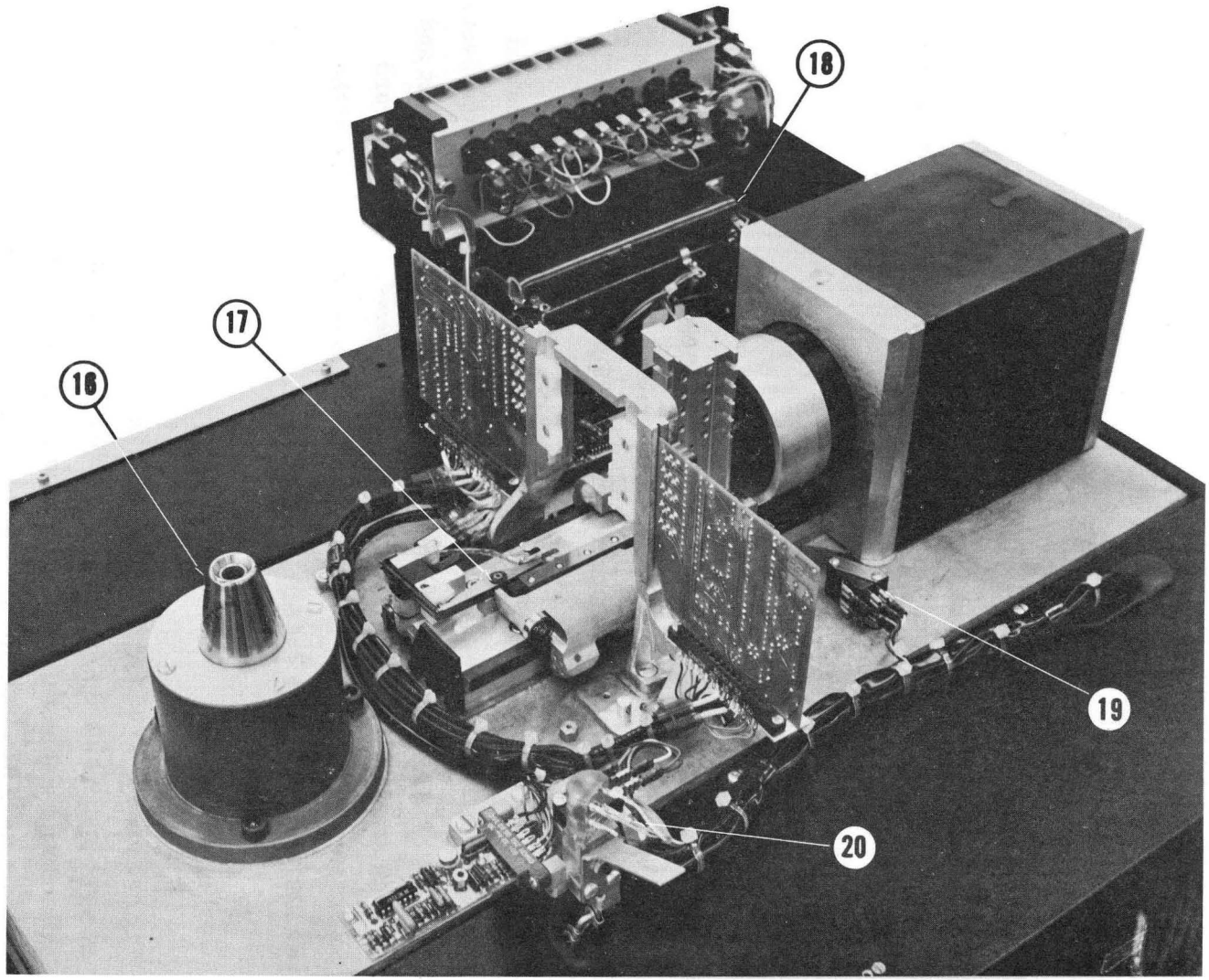


B
Machine Assemblies and Parts

Figure 2-2 (sheet 2 of 4)



C
Machine Assemblies and Parts
Figure 2-2 (sheet 3 of 4)



D
Machine Assemblies and Parts

Figure 2-2 (sheet 4 of 4)

2.3 FUNCTIONAL AREAS

The various assemblies and parts identified in Section 2.2 can be classified into five major functional areas of the Model 630.

A. Cabinet and cooling system
B. I/O interface
C. Operator control panel
D. Positioning and spindle drive mechanisms
E. Control circuitry

The disc pack, which is not an integral part of the drive, was described in Section 1.2.

2.3.1 Cabinet and Cooling System

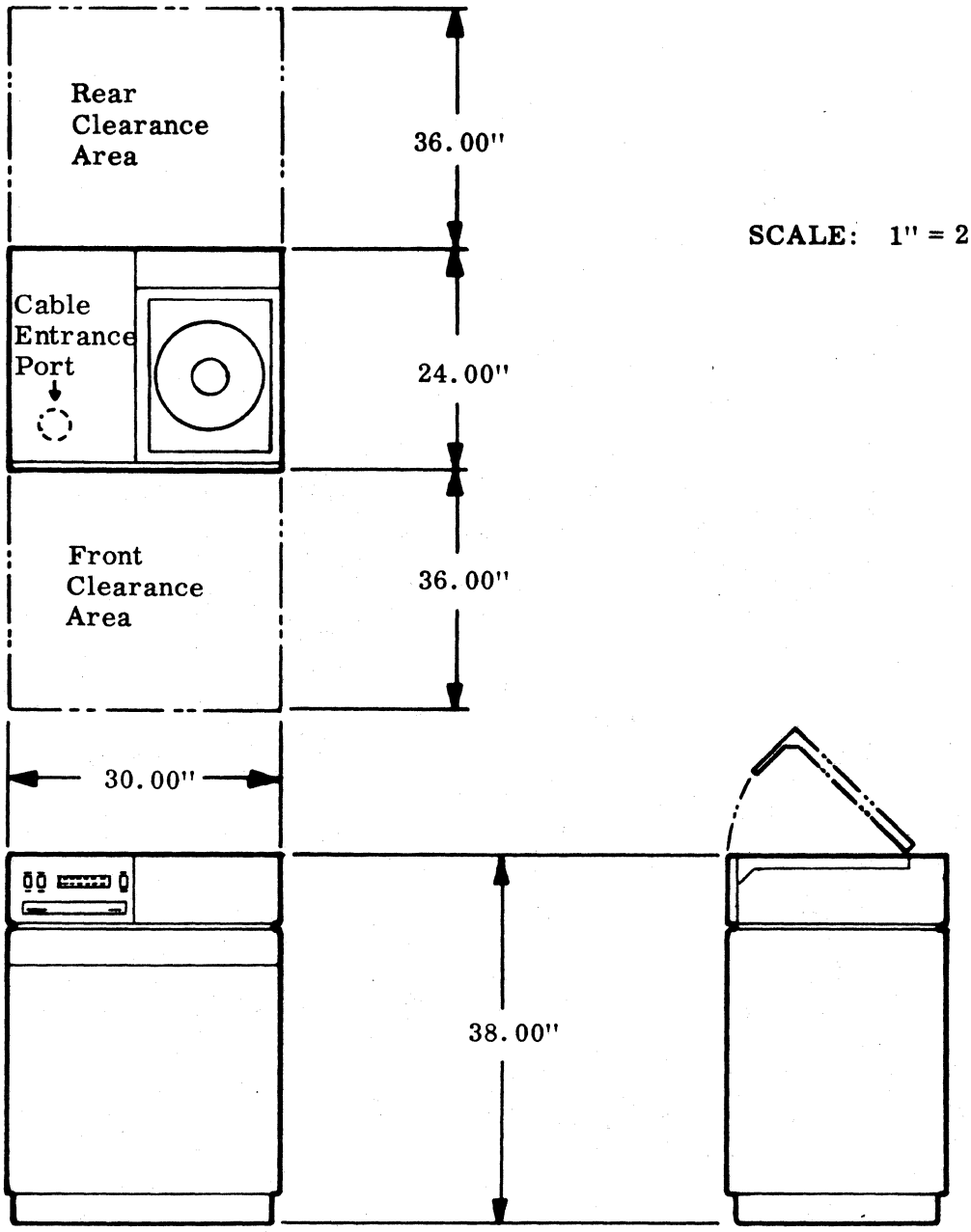
2.3.1.1 Cabinet

The cabinet housing the unit is 30 inches wide, 24 inches deep and 38 inches high. Figure 2-3 is a diagram showing cabinet dimensions and floor space needed for maintenance. A Model 630 weighs approximately 295 pounds.

Front and back covers are attached to the mainframe by magnetic strips and pull off for easy access to the cabinet's interior. The side panels and two top covers are also attached by magnetic strips. The kick panel on the front of the cabinet and the one on the back are each attached by two sheetmetal screws. The logic card file and dc power supply are housed in a door which swings out of the back of the cabinet on two hinges (see Figure 2-4).

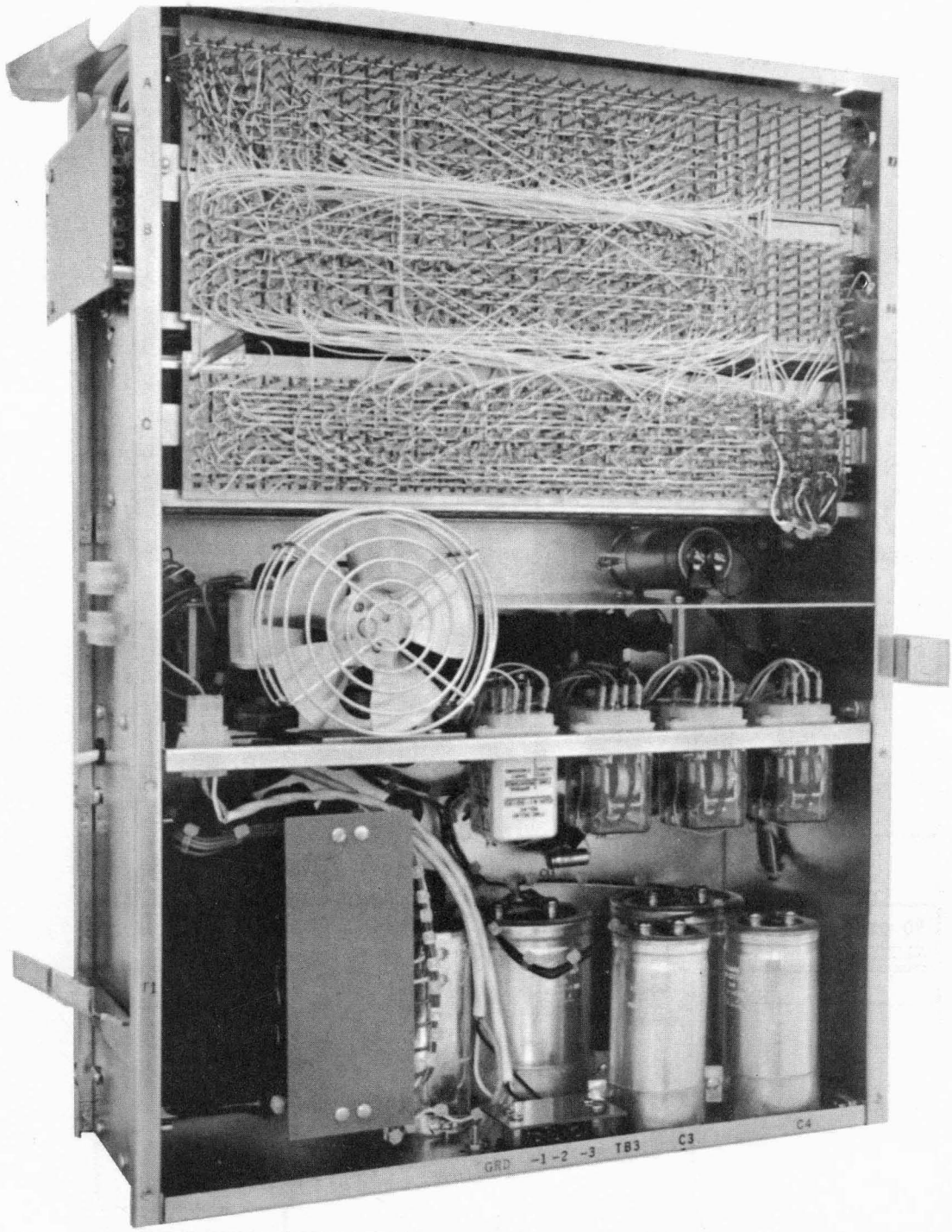
2.3.1.2 Cooling System

Two fans are used for cooling the cabinet. The main blower is located on the floor of the cabinet just inside the front panel. Driven by a 1/8-horsepower motor, it pulls cool air into the cabinet through a filter at a rate of 200 cfm (static pressure at blower is 0.25 inches of water). The air is deflected by a piece of sheetmetal into two columns of air. One column is forced through a duct up the side of the cabinet and into the shroud area. No air is forced into the disc pack itself. Disc rotation generates its own air circulation. From there, the air flows into the positioning motor area, past the servo amplifier/heat sink and back down into the



Cabinet Dimensions 00015

Figure 2-3



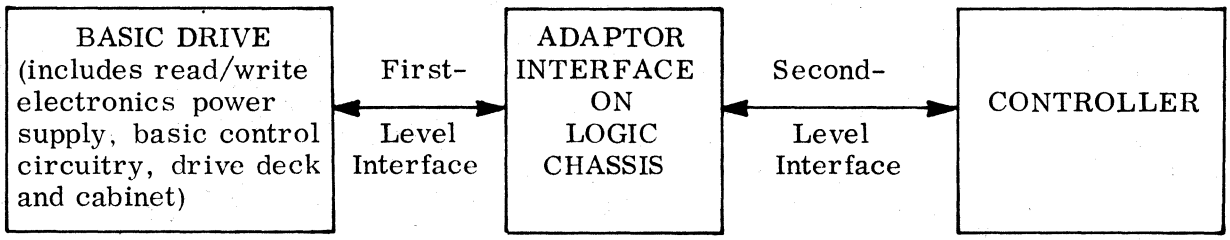
Logic File and DC Power Supply
Figure 2-4

interior of the cabinet. This flow of air then leaves the cabinet through ports in the back of the unit.

The other column moves into the box containing the interior control panel and then out through a hood directly into the card file door. A small fan assists some of the air into the regulator section and down into the power supply area. The rest of the air flows through slits in the card file, past the cards and out holes in the back panel. See Figure 2-5 for an air flow diagram.

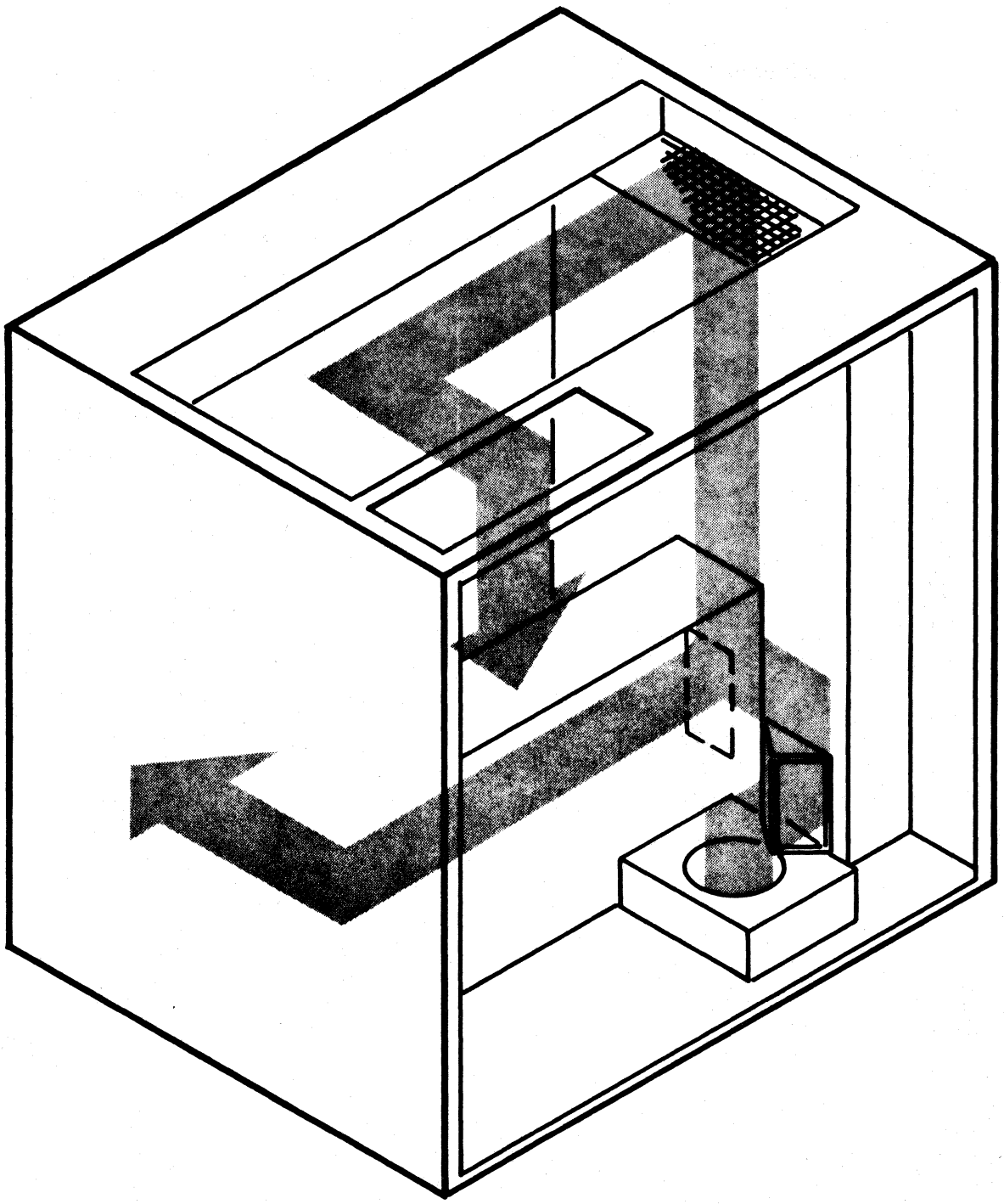
2.3.2 I/O Interface

A two-level interface option has been incorporated in the Model 630. Model 630 drives which are plug-compatible with IBM 2841 controllers employ the second-level interface. Model 630 interfaces may also be designed to communicate with non-2841 controllers. These custom interfaces are at the first level. The two levels are illustrated in Figure 2-6.



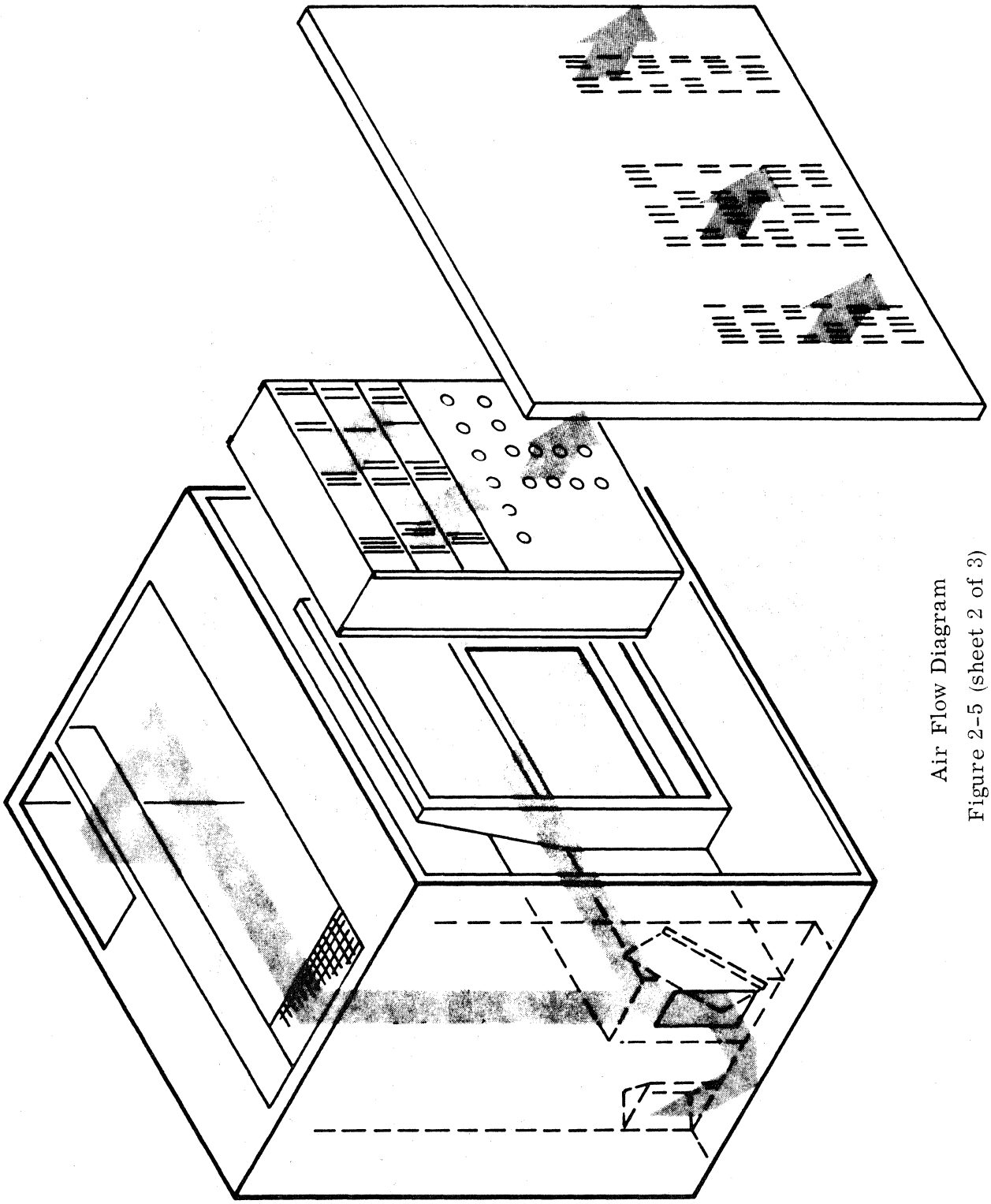
Two-Level Interface Concept

Figure 2-6



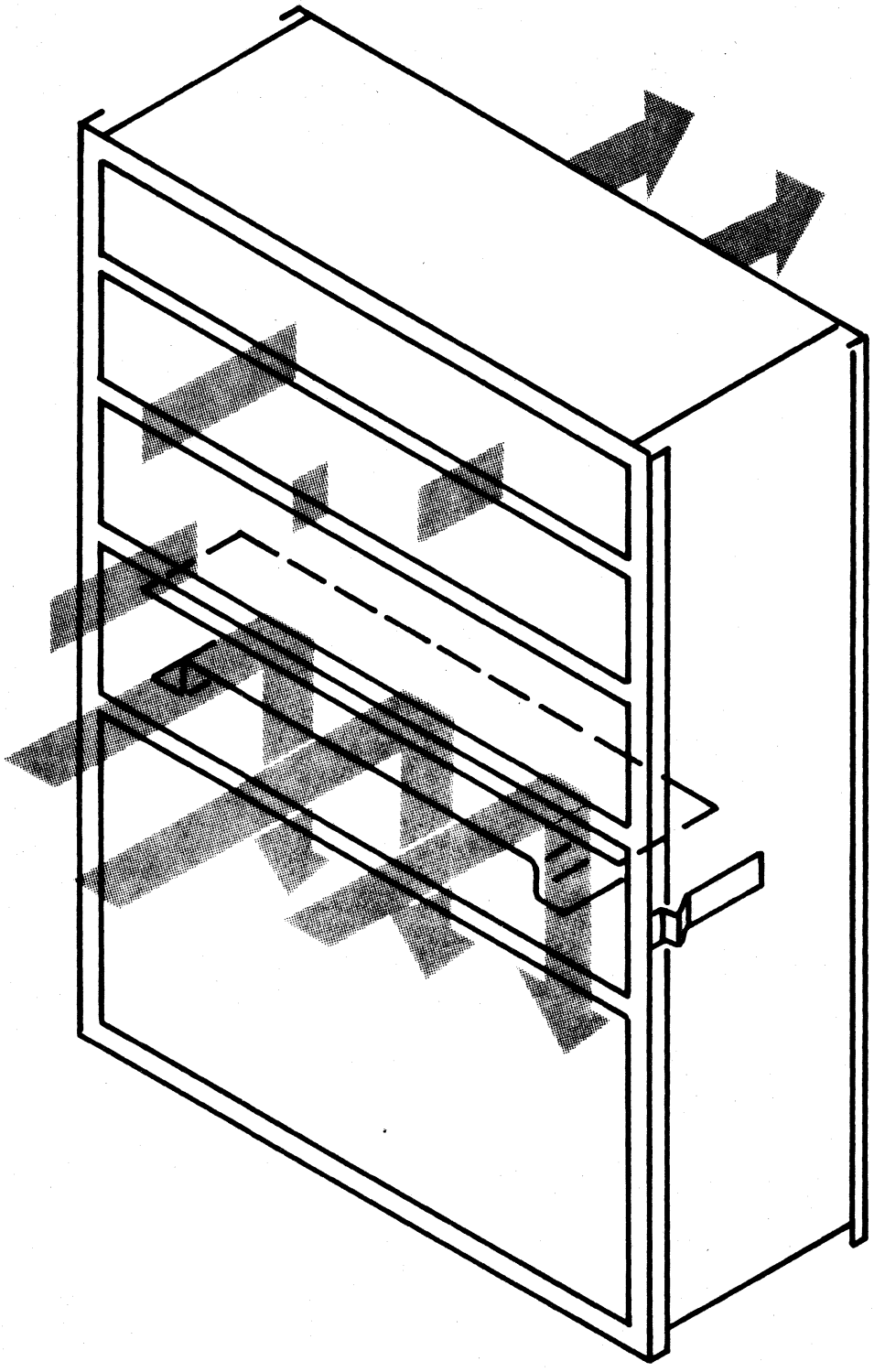
Air Flow Diagram

Figure 2-5 (sheet 1 of 3)



Air Flow Diagram

Figure 2-5 (sheet 2 of 3)



Air Flow Diagram

Figure 2-5 (sheet 3 of 3)

2.3.2.1 Power Requirements (AC and DC)

AC power requirements are the same for drives using either interface level. The following list defines these requirements for the two basic Model 630 configurations (Model 630 A and Model 630 B).

Model	Voltage (vac)	Current (amp)	Frequency (Hz)
A	208/230 ± 10%	25 (start); 4.5 (run)	60 ± 1/2
B	220/380 ± 10% *	25 (start); 4.5 (run)	50 ± 1/2

Both configurations receive power via six-wire cables. The sixth wire (neutral) is not used except in areas where only 380-vac, 50-Hz Wye-connected power is available. When neutral is used, a terminal board change is required so that power is received from line-to-neutral (in a four-wire, 380 vac system, line-to-neutral is 220 vac). Neutral is normally not used in 60-Hz configurations.

AC power is supplied as three-phase, but the individual units draw current from only one phase. The phases are rotated (between in and out connectors) in a multiunit system to provide a balanced load.

Either 208 or 230 vac is required but not both; a tap is available on the power transformer to allow use of 208 vac instead of 230 vac.

DC power for the logic and control functions is provided by the unit itself. A self-contained dc power supply is located in the card file door at the back of the cabinet. The dc power supply and control and logic circuitry are discussed in detail in Section 2.3.5.

---

* Wire change in Model 630 required when 380 vac is used.

Cable lengths should conform to the following specifications (refer to Figure 1-1).

Cable A -- Separate run for each drive	50 ft. (maximum)
Cable B -- Jumper connection from drive to drive	100 ft. (maximum accumulated)
Cable C -- Jumper connection from drive to drive	100 ft. (maximum accumulated)

To satisfy electrical requirements in most areas of the United States, a maximum ac power cable length of 14 ft. is recommended. (UL and local codes must be checked for each installation.)

2.3.2.2 Communication Lines

The communication lines illustrated in Figure 1-1 are identified in more detail in Figure 2-7. These lines can be listed in two basic categories, input and output.

Input (to Model 630 from controller)

- 8 - Time-shared bus lines
- 4 - Tag lines
- 1 - Select unit line
- 1 - Write data coaxial line
- 1 - +36 vdc to controller (for first drive in chain sequence control)
- 1 - +36 vdc in
- 1 - Controlled ground

Output (from Model 630 to controller)

- 8 - Selected unit cylinder address lines
- 1 - Attention
- 1 - Unit selected
- 1 - Selected unit ready
- 1 - Selected unit on line
- 1 - Selected unit index pulse
- 1 - Selected file unsafe
- 1 - Selected unit seek incomplete
- 1 - Selected unit end of cylinder
- 1 - Read data coaxial line

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- 1 - Selected unit end of cylinder
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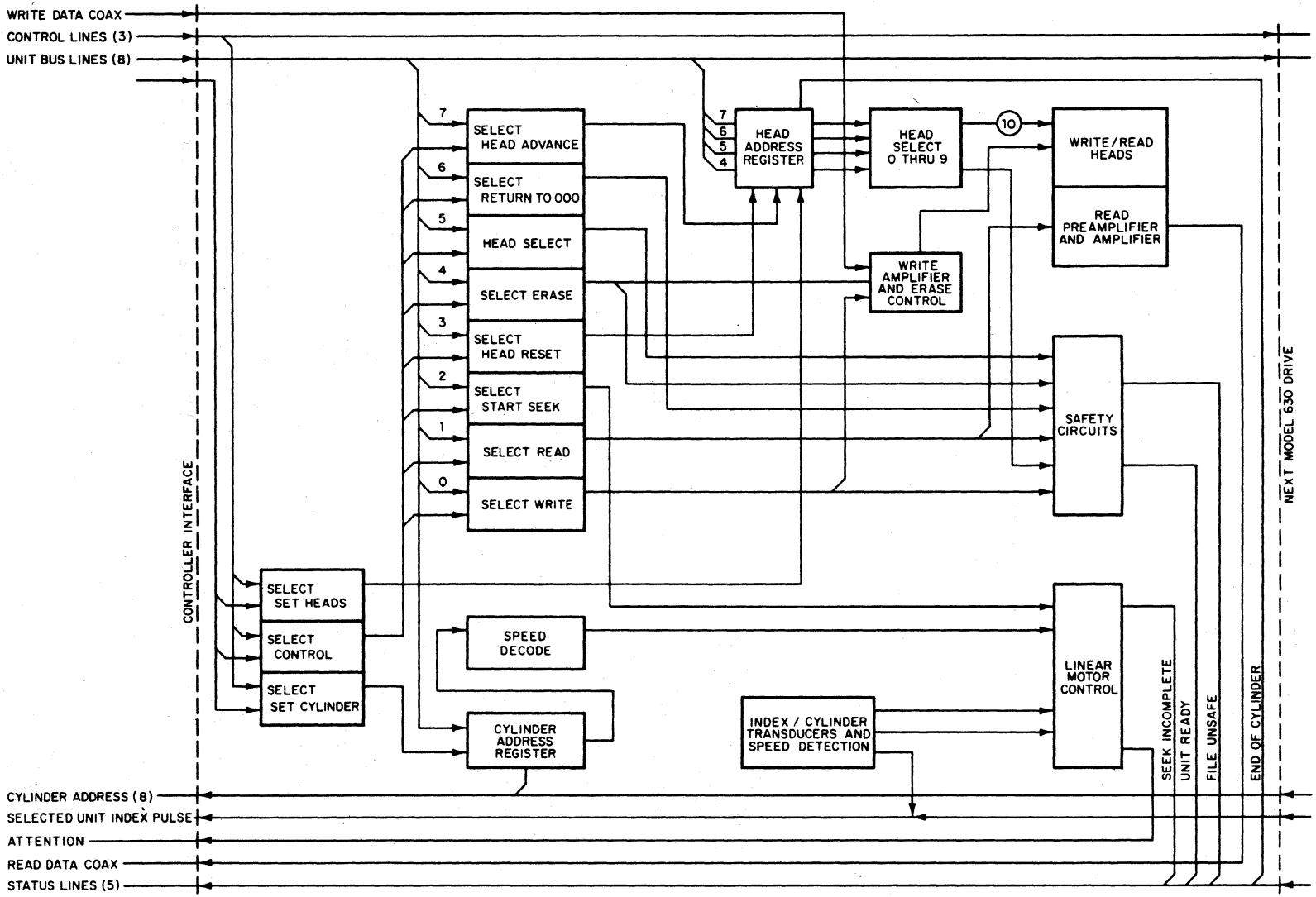


Model 630 Communication Lines
Figure 2-7

1 - Selected unit read only

1 - Selected unit write current sense

1 - Heads extended line (common to all drives)

1 - Sequencing voltage out

INPUT LINES

A. Write Data Coaxial

Information is received from the controller on this line in binary form. A -L level signal (nominal 0 vdc) represents a bit and +L level signal (nominal +3 vdc) represents absence of a bit. A bit is sent at the beginning of each 800 ns bit cell time for a "zero" and a bit is sent at the beginning of each 800 ns bit cell time plus a data bit in the center of the cell time (400 ns interval) for "ones". Pulse width is 100 ±25 ns with fall time less than 30 ns.

B. Select Unit

A separate line exists for each unit in a multidrive system via dc cables. This line must remain at -Q (nominal -3 vdc) during read, write and control operations. When the 630 drive is not selected, this line is at +Q (nominal +3 vdc).

C. Tag Lines

There are four lines used to perform setup and control functions by acting as strobe pulses (pulse duration 800 ns) for the time-shared bus lines. They are:

1. Control

When this line is pulsed (assuming select unit and file safe conditions) with a -Q level, the 630 looks at the bus line selected by the control tag line and performs the indicated control function.

2. Set Cylinder

When this line is pulsed (assuming select unit and file safe conditions) with a -Q level, the 630 looks at all eight bus lines for the new cylinder address and sets the CAR (cylinder address register) with the new address.

3. Set Head and Direction *

When this line is pulsed with a -Q level, the 630 looks at unit bus lines 4, 5, 6 and 7 and sets the head address register with the new head address. The head address register requires a "reset head register" control command prior to "set head" commands.

4. Set Difference

This line is not used in the Model 630 drive. It is used by the IBM 2311 to set the difference count into difference counter. The 630 calculates this difference itself, using one's complement arithmetic and does not depend on the controller for a difference count.

D. Controlled Ground

This line provides ground input to the K1 sequence relay. The controller normally uses the line to power up and down a string of 630 drives.

E. +36 vdc Sequencing Voltage In

This line receives +36 vdc from the previous drive or controller to pick sequence control relay K1.

F. Unit Bus Lines (Eight)

These time-shared lines are used under control of the tag lines to perform control functions in the 630 drive. These functions are listed below (Table 2-II). The lines are pulsed (-Q level).

G. CPU Halt

This line brings in a signal generated by the central processing unit which notifies the controller when the CPU is in a wait state (e.g., a programmed halt instruction). The active signal is at the -Q level and is used only in conjunction with the revenue meter option on the 630 drive.

---

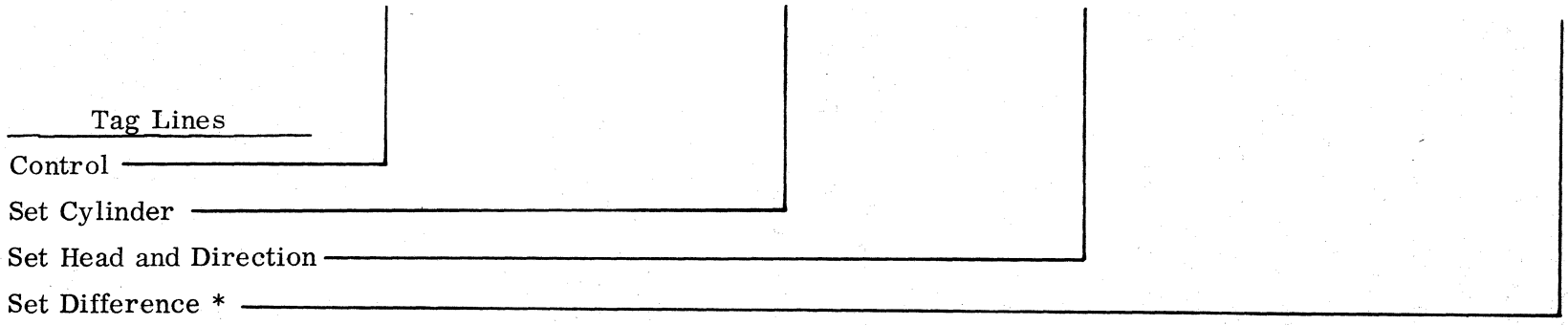
* When a Model 630 communicates with an IBM 2841, it receives a direction of travel bit on the 0 bus line. This bit is ignored because direction is derived as part of the difference count operation performed by the 630.

Table 2-II

UNIT BUS LINE FUNCTIONS

Function During Various Cycles

Line Name	I. Control Cycle	II. Set Cylinder	III. Set Head and Direction	IV. Set Difference *
Bus 0	Set Write	Cylinder 128	Set Forward *	128
Bus 1	Set Read	Cylinder 64		64
Bus 2	Seek Start (0.8 us≤t≤2 us)	Cylinder 32		32
Bus 3	Reset head register	Cylinder 16		16
Bus 4	Set erase	Cylinder 8	Head 8	8
Bus 5	Select head	Cylinder 4	Head 4	4
Bus 6	Restore (15 ms≤t≤50 ms)	Cylinder 2	Head 2	2
Bus 7	Set head advance (0.8 us≤t≤2 us)	Cylinder 1	Head 1	1



* Shown but not needed in 630 drive.

OUTPUT LINES

A. Attention

When this line goes to the -Q level (nominal -3 vdc), one of two conditions exists:

1. A normal seek is completed.
2. 300 ms have expired since a seek command was given and detenting did not occur. This is an abnormal condition which is sent to the controller on the seek incomplete line.

This line is not conditional upon select unit line and is reset (+Q level, +3 vdc) when set read is selected. A separate attention line for each 630 drive is provided via dc cable.

B. Selected Unit Seek Incomplete

This line goes to -Q as a signal to the controller that the access mechanism failed to reach a normal detent position in 300 ms or less. The select unit line must be at -Q for this line to be active.

C. Unit Selected

This line goes to -Q, as a signal to the controller that the 630 is selected. A separate line exists for each drive via the dc cable. The select unit line must be at -Q for this line to be active.

D. Selected Unit Ready

This line goes to -Q when the drive has satisfactorily completed a seek. The select unit line must be at -Q for this line to be active.

E. Selected Unit On Line

This line goes to -Q when cables are connected, heads have been loaded, and the unit is ready to read or write. The select unit line must be at -Q for this line to be active.

F. Selected Unit Index Pulse

This line goes to -Q when an index pulse is detected. The select unit line must be at -Q for this line to be active.

G. Selected File Unsafe

This line goes to -Q when the 630 drive (which has been selected with select unit line) is unsafe for operation. Conditions that cause the file to go unsafe are described in the Control Translation logic diagram writeup in Section 2.3.5.

H. Selected Unit End of Cylinder

This line goes to -Q when the selected 630 head counter has reached the end of present cylinder. This condition is determined by the contents of the head select register. When bit 8 and bit 2 are set (head select change from 9 to 0) an end-of-cylinder indication is given to the controller. The select unit line must be at -Q for this line to be active.

I. Read Data Coax

Information is sent to the controller on this line as binary pulses. A pulse (150 $\pm$ 50 ns) is sent at the beginning of each 800-ns bit cell time; this pattern is the zero's representation. When one's are detected, two pulses are sent during bit cell time (one every 400 ns). A +L (nominal +3 vdc) level represents a bit and a -L (nominal ground) represents absence of bit.

J. Selected Unit Cylinder Address (Eight Lines)

These eight lines indicate the present cylinder address by going to -Q level when the select unit line is at -Q. At set cylinder time (see tag lines) the contents of the CAR changes.

K. Selected Unit Read Only

This line goes to -Q when the READ ONLY/READ-WRITE switch on the operator control panel is in READ ONLY position. The select unit line must be at -Q for this line to be active.

L. Selected Unit Write Current Sense

This line goes to -Q when write is selected and write drive current is sensed.

M. Heads Extended

This line is used in the IBM 2841 as an indication that the heads are retracted. Since the 2841 provides dc voltages to IBM 2311's, it needs to know that heads are retracted before power down.

N. +36 vdc Sequencing Voltage Out

When the 630 reaches 70% of full speed, a relay contact closes which provides +36 vdc to the sequence relay in the next drive in the chain.

O. Clock Out

This line is used in the 630 Drive to inhibit changing the state of the READ-WRITE/READ ONLY and ENABLE-DISABLE latches when the unit is selected, and in the revenue meter option to indicate that the CPU is running. This line is active at a +Q level from the controller.

2.3.2.3 Interface Connections

The Model 630 drive is designed so that multiple units can be connected in chain fashion (see Figure 1-1). Power control circuitry is provided to allow the controller to start the units - one at a time. As soon as the first unit reaches 70% of its full speed, transfer contacts close, enabling the second unit to start. This sequence continues until all units in the chain are running. In-and-out phase connection of power is used to balance phase current in a multiple drive system.

POWER

DC, Data and Select Connector (IN Connection Only)

In Pin Connection	Description	Level	IBM Terminology (if different)
1	+6 vdc		
2	+6 vdc		
3	dc ground		
4	dc ground		
5	Write data coax	-L	
6 through 9	Spares		
10	dc ground		
11	dc ground		
12	Read data coax	+L	
13	+3 vdc (used as termination power source on 630)		
14	+3 vdc		
15	-36 vdc		
16 through 18 and G	Not used		
19	-3 vdc		
20	-3 vdc		
21	Attention	-Q	Gated Attention
22	Unit is selected	-Q	Selected Module
23	Select unit	-Q	Module Select
24	Not used		

POWER (continued)

DC, Data and Select Connector (IN Connection Only) (continued)

In Pin Connection	Description	Level	IBM Terminology (if different)
25	Shield ground		
26	Common for 21		
27	Common for 22		
28	Common for 23		

NOTE: All pin connections are shown as IBM-compatible connections. Since the Model 630 drive supplies its own power, pins 1, 2, 4, 11, 14, 15, 19 and 20 are not used.

AC and Sequence Control Connector

In Pin Connection	Description	Out Pin Connection
A	208/230 vac, phase A	B
B	208/230 vac, phase B	C
C	208/230 vac, phase C	A
D	Neutral (when required)	D
E	110 vac convenience outlet	E
F	110 vac convenience outlet	F
G	Frame ground (cable shield)	G

SIGNAL *

SIGNAL CONNECTOR

In Pin Connection	Line Description	Out Pin Connection	Level	IBM Terminology (if different)
1	Unit bus 0	1	-Q	File bus 0
2	Twisted pairs ground	2		
3	Unit bus 1	3	-Q	File bus 1
4	Unit bus 2	4	-Q	File bus 2
5	Twisted pairs ground	5		
7	Unit bus 3	7	-Q	File bus 3
8	Unit bus 4	8	-Q	File bus 4
10	Twisted pairs ground	10		
11	Unit bus 5	11	-Q	File bus 5
12	Unit bus 6	12	-Q	File bus 6
13	Twisted pairs ground	13		
14	Unit bus 7	14	-Q	File bus 7
15	Set difference (not used in 630 drive)	15	-Q	
16	Twisted pairs ground	16		
17	Set cylinder (tag line)	17	-Q	
18	Set head and direction (tag line)	18	-Q	
20	Twisted pairs ground	20		

* Five control/signal lines have already been defined on the dc connector (see page 2-26.

SIGNAL CONNECTOR (continued)

In Pin Connection	Line Description	Out Pin Connection	Level	IBM Terminology (if different)
21	Control (tag line)	21	-Q	
22	CPU halt (for IBM Type Usage Meter Control) *	22	-Q	
23	Twisted pairs ground	23		
24	SCU Metering On (for IBM Type Usage Meter Control) *	24	+Q	
25 through 39	Spares			
40	Cylinder address register 1	40	-Q	
41	Twisted pairs ground	41		
42	Cylinder address register 2	42	-Q	
43	Cylinder address register 4	43	-Q	
44	Twisted pairs ground	44		
45	Cylinder address register 8	45	-Q	
46	Cylinder address register 16	46	-Q	
47	Twisted pairs ground	47		
48	Cylinder address register 32	48	-Q	
49	Cylinder address register 64	49	-Q	
50	Twisted pairs ground	50		
51	Cylinder address register 128	51	-Q	

* Initial 630 drives have running time meters which are activated whenever the drive is up to 70% of full speed and heads are loaded.

SIGNAL CONNECTOR (continued)

In Pin Connection	Line Description	Out Pin Connection	Level	IBM Terminology (if different)
52	Selected unit ready	52	-Q	Selected ready
53	Twisted pairs ground	53		
54	Selected unit on line	54	-Q	Selected on line
55	Selected unit index pulse	55	-Q	
56	Twisted pairs ground	56		
57	Selected file unsafe	57	-Q	
58	Selected unit seek incomplete	58	-Q	Selected seek incomplete
59	Twisted pairs ground	59		
60	Selected unit end of cylinder	60	-Q	Selected end of cylinder
62	Selected unit sector pulse (not used in 630 A or 630 B)	62		Selected sector
63	Twisted pairs ground	63		
64	Selected unit write current sense	64	-Q	Selected write current sense
65	Heads extended	65	-W	
66	Twisted pairs ground			
67	Selected unit read only	67	-Q	Not applicable
70 through 75	Spares	70 - 75		
76	Controlled ground			
77	+36 vdc sequence pick in			
	+36 vdc sequence pick out	77		

SIGNAL CONNECTOR (continued)

In Pin Connection	Line Description	Out Pin Connection	Level	IBM Terminology (if different)
78	+36 vdc to controller (for first drive in chain sequence control)			
	+3 vdc to termination plug	79		
80	Shield ground	80		
82	Shield ground	82		

Pins 6, 9, 19, 61, 68, 69 and 81 do not exist on the Signal Connector.

The voltage levels identified by the letters Q, L and W in the right-hand column are defined as follows:

-Q = -0.5 to -3.5 volts

+Q = +3.5 to +0.65 volts

-W = +1.3 to 0 volts

+W = +38.9 to +28.4 volts (+36 volts, nominal)

-L = +0.3 to 0 volts

+L = +6.28 to +2.0 volts (+3 volts, nominal)

2.3.3 Operator Control Panel

Figure 2-8 shows how the keys and lights are displayed on the operator control panel. The functions of operator control switches and indicators are as follows:

A. ENABLE-DISABLE Switch

ENABLE Position - The switch enables the logical connection between the controller and the Model 630 drive.

DISABLE Position - The switch disables the logical connection between the controller and the Model 630 drive.

If the Model 630 drive is performing an operation under the command of the controller, changing the state of the switch will give an off-line indication to the controller.

B. READ/WRITE - READ ONLY Switch

READ/WRITE Position - The switch enables read and write circuitry.

READ ONLY Position - The switch disables the write and erase circuitry to allow a READ ONLY operation. A line is available in the I/O interface to indicate that the READ ONLY mode has been selected. The controller designer must incorporate this signal in system status if the central processor is to recognize the condition (a standard IBM 2841 does not recognize this condition).

C. UNIT NUMBER/READY Indicator (Green)

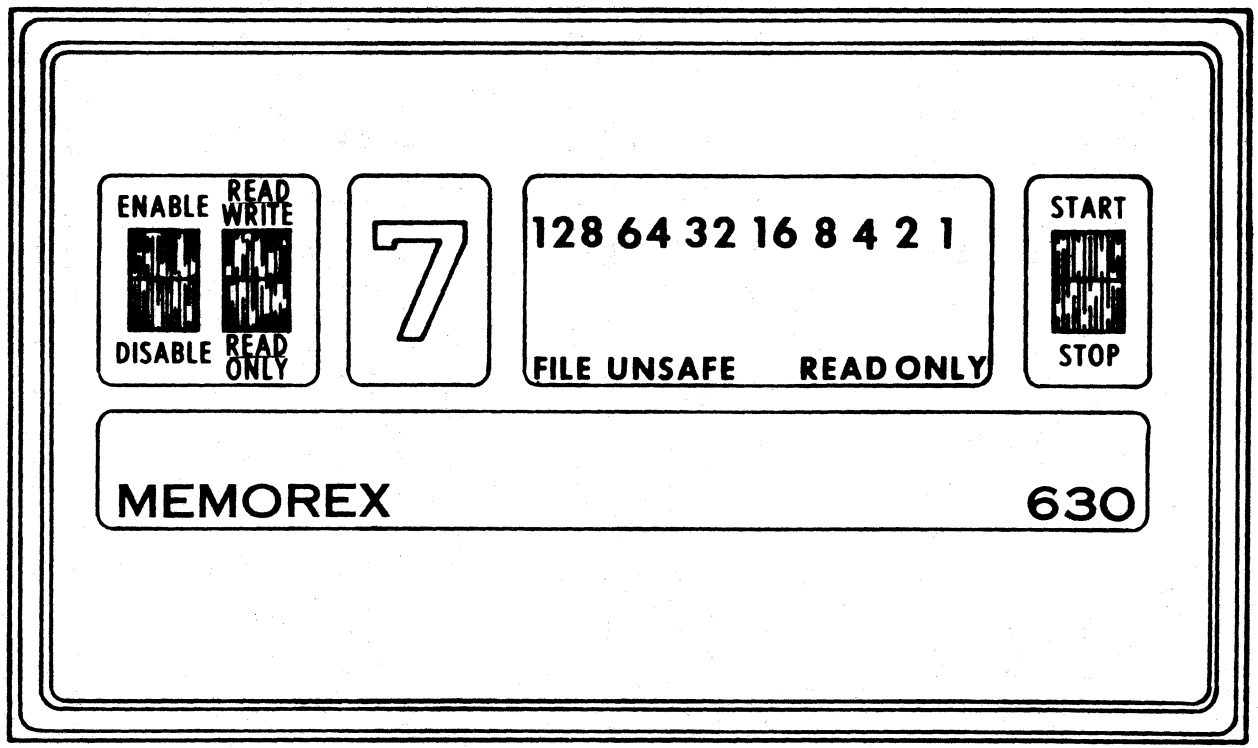
The number legend associated with this indicator can be changed easily to reflect the logical unit number of the drive in the system. This indicator lights up when the drive has reached operational speed and the heads are positioned to track 000 on the initial load operation. This green light signifies that the drive is ready for instructions. The indicator goes off when the STOP switch is depressed or when system power is dropped. The indicator also goes off if the detent remains unseated for 300 ms or longer.

D. File Monitor Indicators

This indicator cluster calls out the cylinder position (weighted, binary number readout) and indicates a FILE UNSAFE condition (red light) and READ ONLY mode (white light).

The access position indicator continuously identifies the cylinder to which the heads have been positioned.

The FILE UNSAFE indicator lights when the safety circuits determine that the file is unusable.



Operator Control Panel
Figure 2-8

The READ ONLY indicator lights when the write and erase circuits are disabled by the READ ONLY switch.

E. START-STOP Switch

START Position - This switch is operable when the main power switch to the unit is on, a pack has been loaded and the cover closed. Depressing this switch powers the drive motor and, when the disc pack speed is greater than 1700 rpm, and pack stabilization delay of 45 seconds has expired, loads the heads and positions them to cylinder 000.

STOP Position - With the switch in this position, power to the motor cuts off and the carriage is retracted, which unloads the heads. Dynamic braking stops the spindle within 10 seconds.

2.3.4 Positioning and Spindle Drive Mechanisms

2.3.4.1 Positioning Motor

The linear positioning motor consists of a stationary permanent magnet surrounding a moveable, bobbin-wound armature. The armature is free to slide in and out of the permanent magnet through a hole in one of the magnet's faceplates. See Figure 2-9.

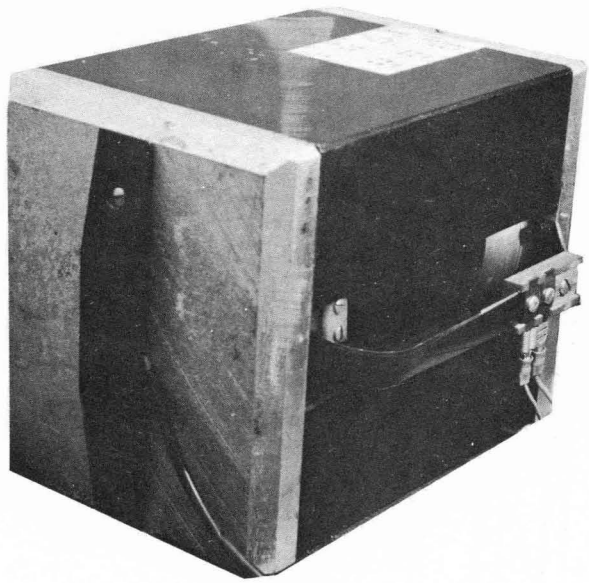
Fastened to the armature by three screws is a T-bar tower which holds the 10 head-arm assemblies. The T-bar is mounted on a carriage that moves freely along a carriage way on three pair of opposed ball bearing rollers. Movement of the armature in and out of the permanent magnet moves the carriage forward and back. This linear travel positions the heads over or under their respective disc surfaces or pulls them out and away from the disc pack.

Power for this movement is provided by a direct current which is fed to the armature over a current range of 0 to 6 amp. The magnetic field built up around the armature by this current reacts with the permanent magnetic field. The reaction either forces the armature out away from the permanent magnet or pulls it into the field. Direction depends on the polarity of current; speed depends on the current level. Refer to Section 2.3.5 for a description of the source and control of this power. Two beryllium strips serve as flexible connectors between the armature coil and the dc power supply leads.

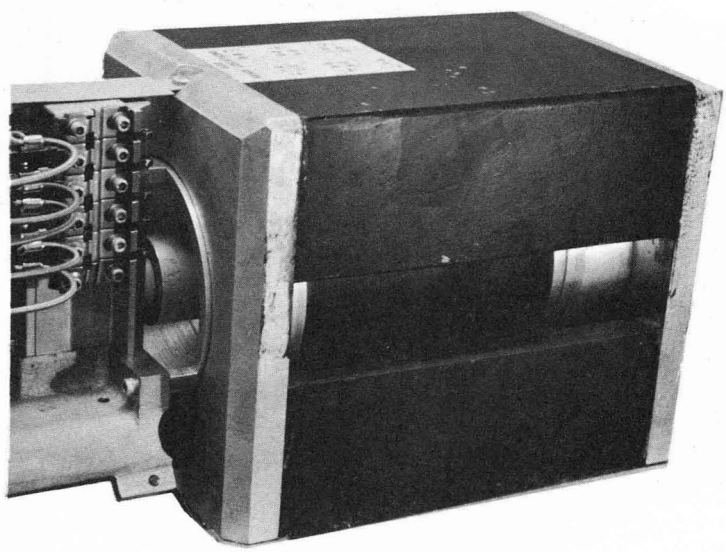
2.3.4.2 Head-Arm Assembly

The head-arm assembly consists of 10 read/write heads attached to the ends of 10 support arms. These arms are mounted on a moveable T-bar carriage in two banks of five each; half of the head-arm assemblies face up and half face down. See Figure 2-10.

The read/write heads contain the read/write and erase poles. As can be seen in Figure 2-11, the read/write gap precedes the erase gap by 0.045 inch. The coils



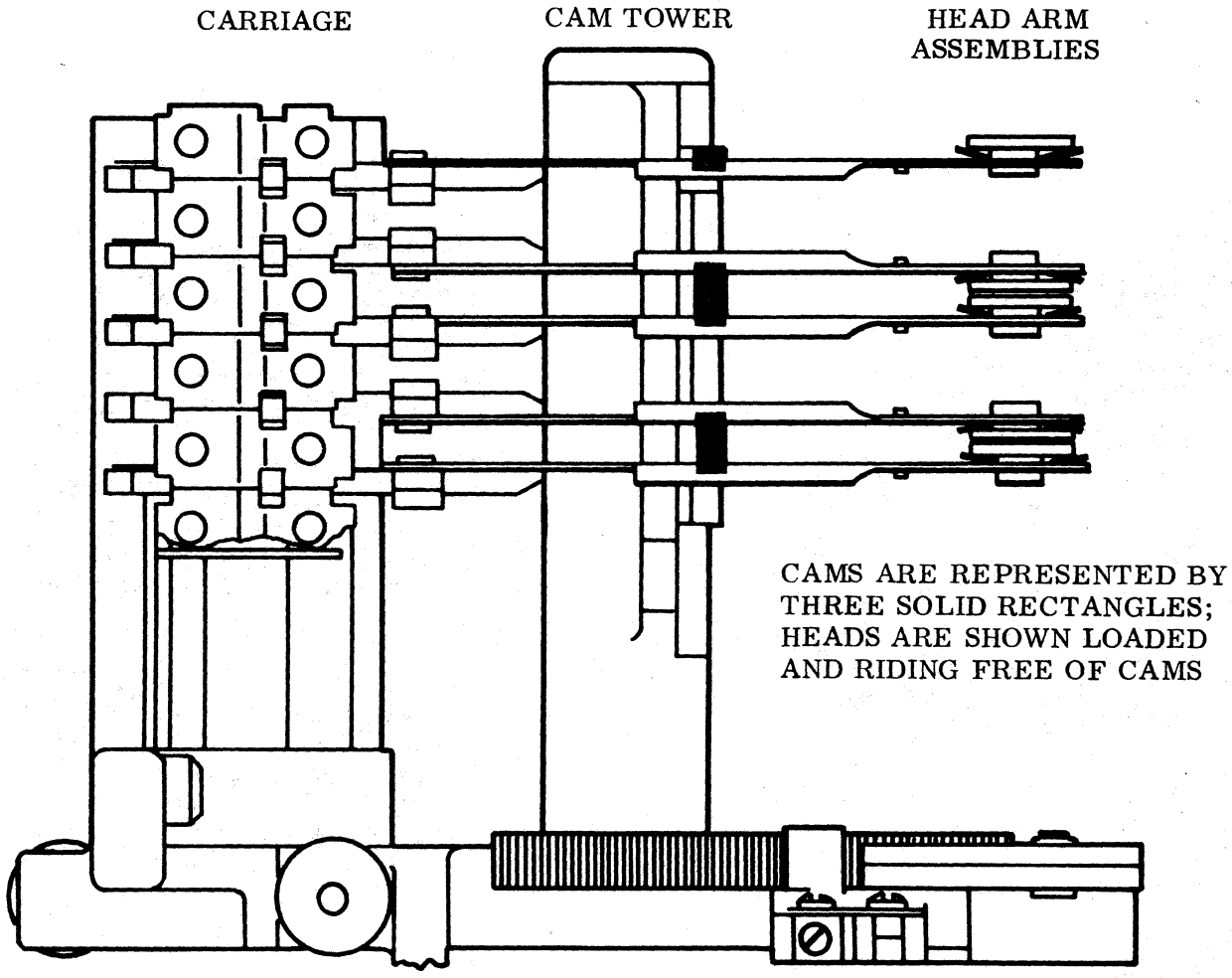
A



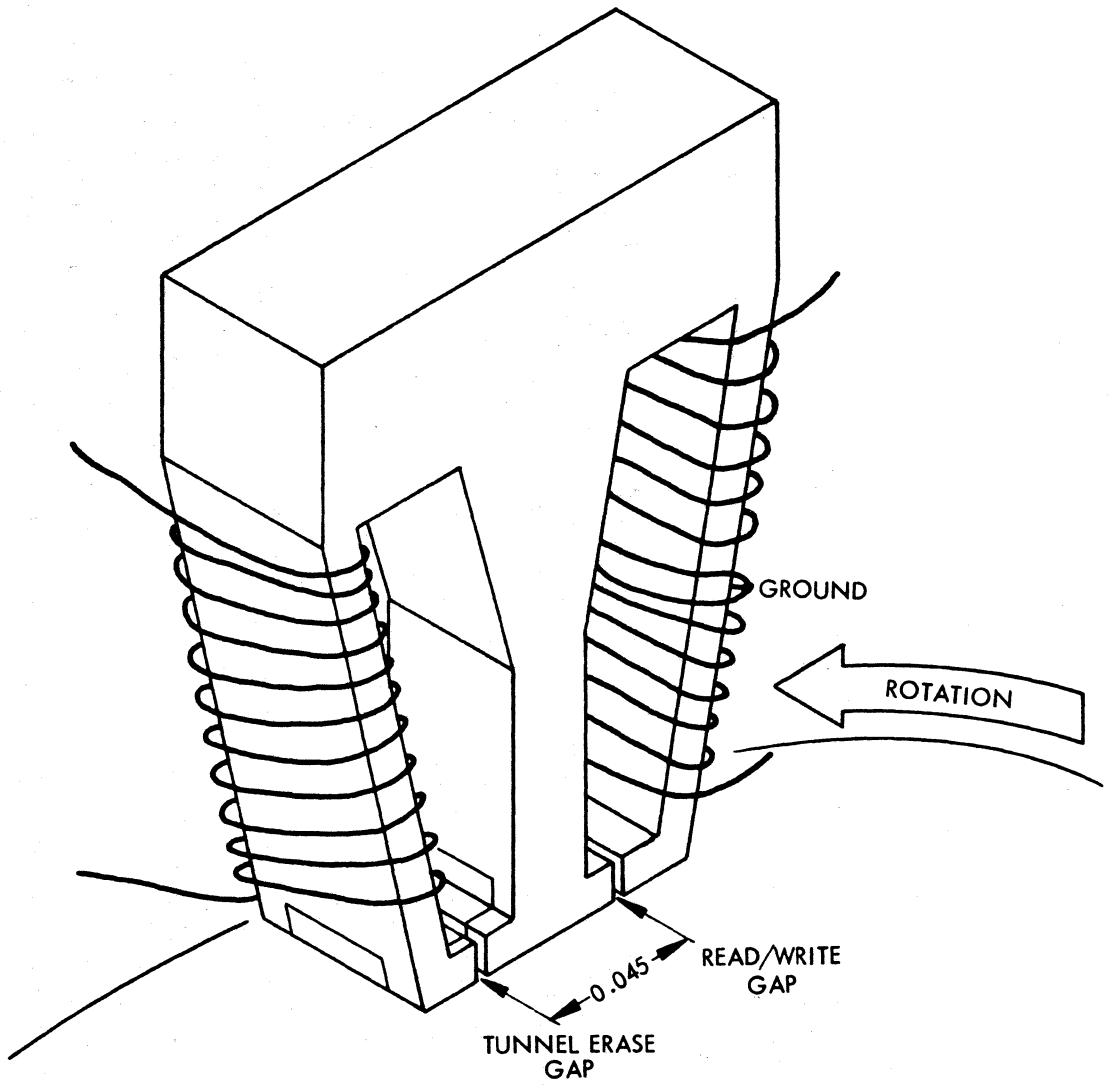
B

Linear Positioning Motor

Figure 2-9

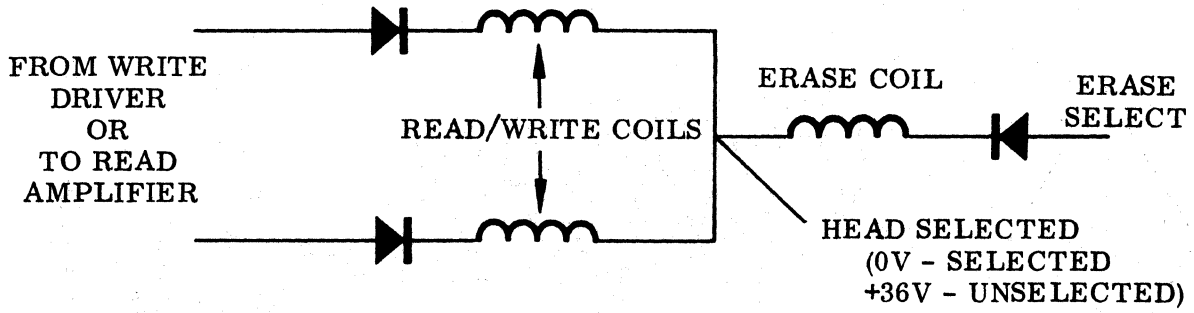


Head Mounting Concept
Figure 2-10



Read/Write and Erase Poles
Figure 2-11

which carry the read/write and erase currents are also illustrated in Figure 2-11. Two coils are connected in series (center tapped) on the read/write pole and a single coil is used on the erase pole. Head selection (using diode switching) places ground on the center tap of the selected head as shown in the sketch below.



Each head shoe is gimbal-mounted to allow pivoting on any horizontal axis. Vertical mobility is provided by a leaf spring built into the arm. This freedom of movement allows the head to maintain the correct altitude over the disc surface.

The leads connected to the read/write and erase coils are encased in a stainless steel spring. This spring supports and shields the leads and acts as a ground connection between the head arm and read/write circuitry.

The leaf spring is designed to maintain a constant loading force on the heads (350 grams, nominal). When the heads are in the retracted position, Delrin * unload pins bear against a ramp surface (also an integral part of the head arm). They counter the loading force and hold the heads in the unload position. The purpose of the pins is to keep the heads separated enough to clear the discs during load and unload operations. The pins are attached to an aluminum tower which arches over the arms.

The load/unload ramp rides off its pin as the head moves into the pack. When the ramp is clear of the pin, spring tension from the leaf spring forces the head toward the disc surface. An air bearing between the head and disc surface created by the rotating disc counters the spring loading force and keeps the head at the required flying height (125 microinches, nominal).

As the arm is retracted, the ramp rides back onto its pin and the head is lifted clear of the disc surface. Just as loading the heads is an inseparable part of initial seek, unloading is integrated with the retract operation.

2.3.4.3 Detent Mechanism

A rack of teeth, called the detent rack, is mounted on the carriage directly under the array of arms. As the carriage moves along the track during positioning, the rack moves with it. Spacing of the rack teeth is 0.020 inch.

A double detent pawl is mounted on the carriage way opposite the rack. Each pawl has a set of four teeth with the same pitch as the rack teeth. The two pawls are offset from one another by half their pitch (0.010 inch). See Figure 2-12. This offset spacing allows the pawl to engage the rack in twice as many positions as there are teeth. When one pawl is engaged, the other rests on top of the adjacent rack tooth. This is commonly referred to as odd/even detenting. One detent pawl engages at all odd cylinder positions while the other engages at all even cylinder positions.

The two pawls are spring loaded and held in the detent-out position by a detent actuator. See Figure 2-13.

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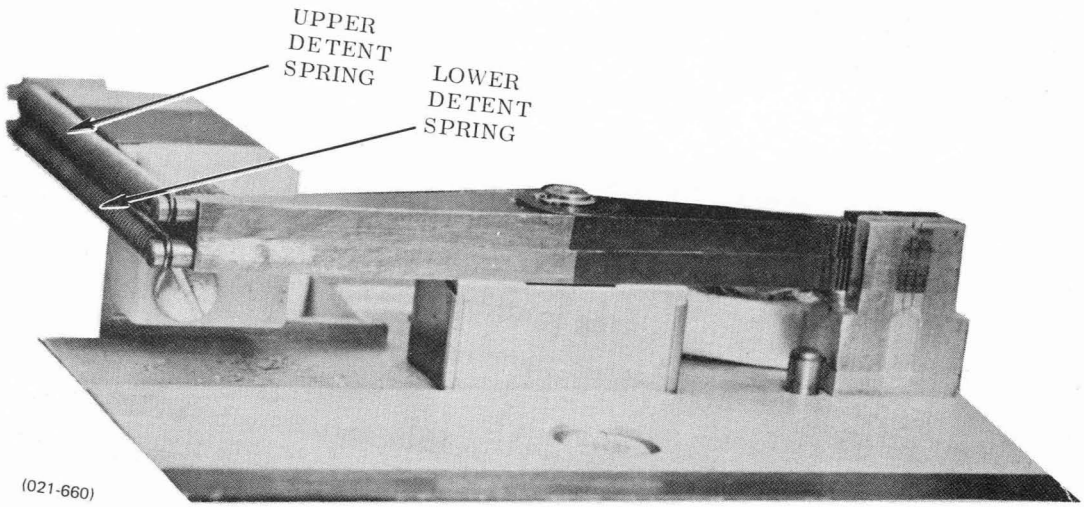
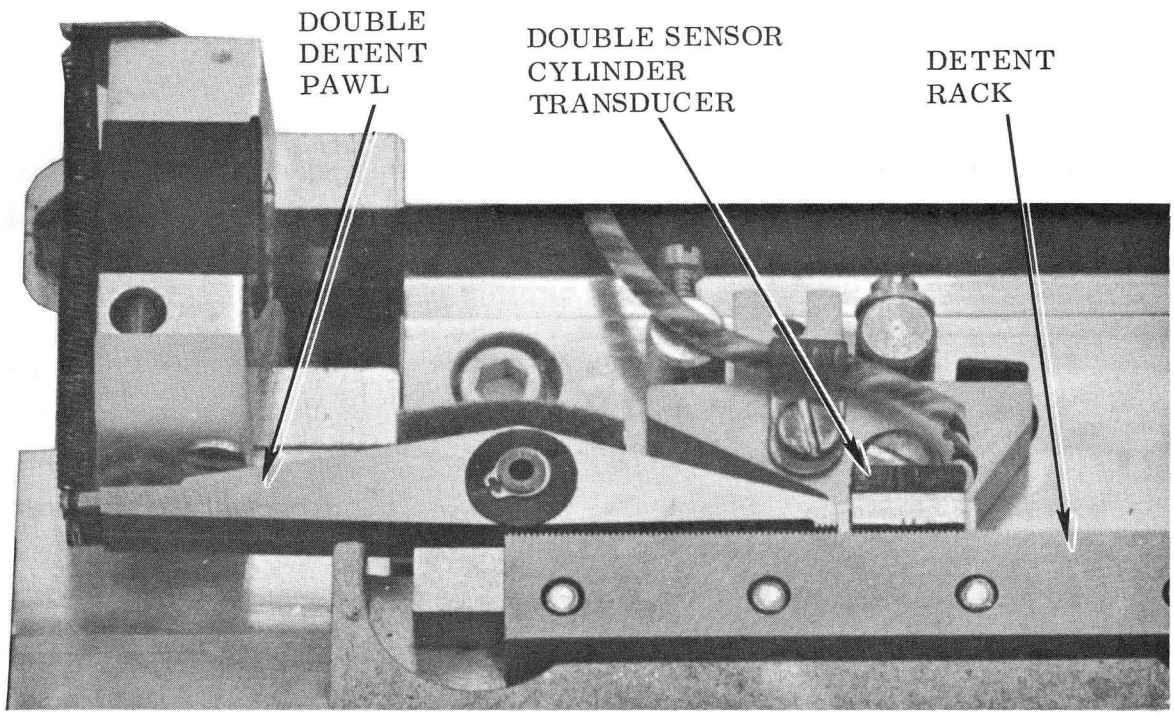
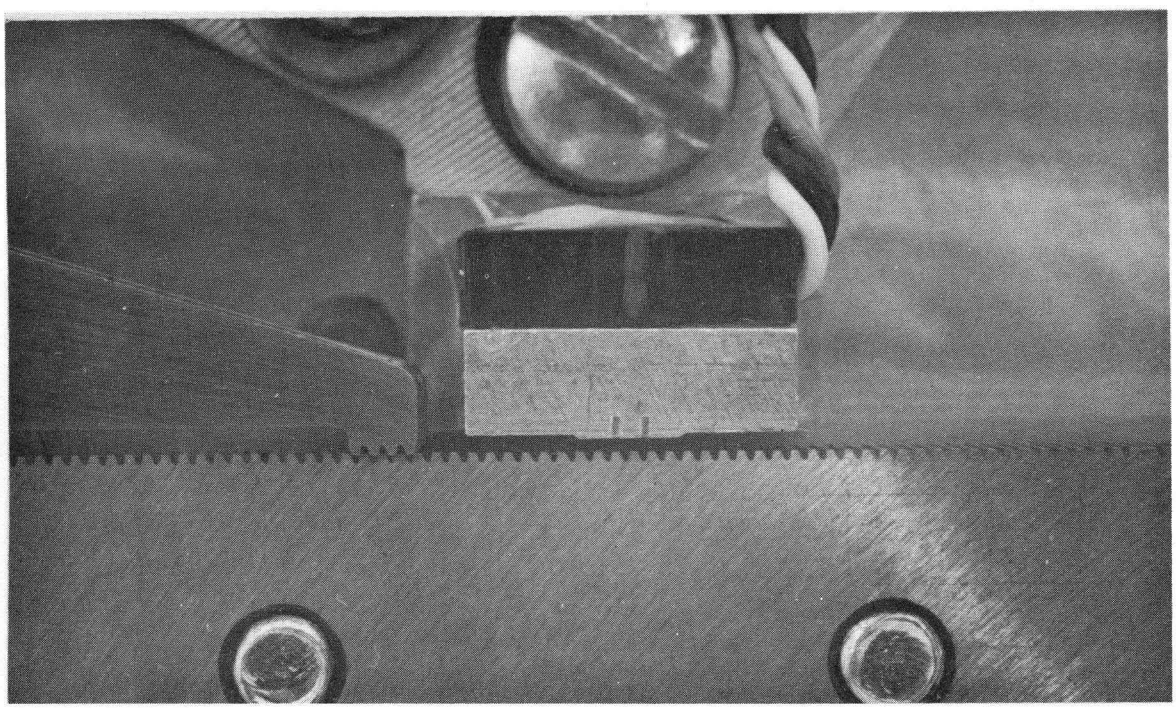
* du Pont trade name for an acetyl resin



Double Detent Pawl and Cylinder Transducer

Figure 2-12





Spring Loaded Detent Pawls and Detent Actuator

Figure 2-13

2.3.4.4 Motion and Position Detectors

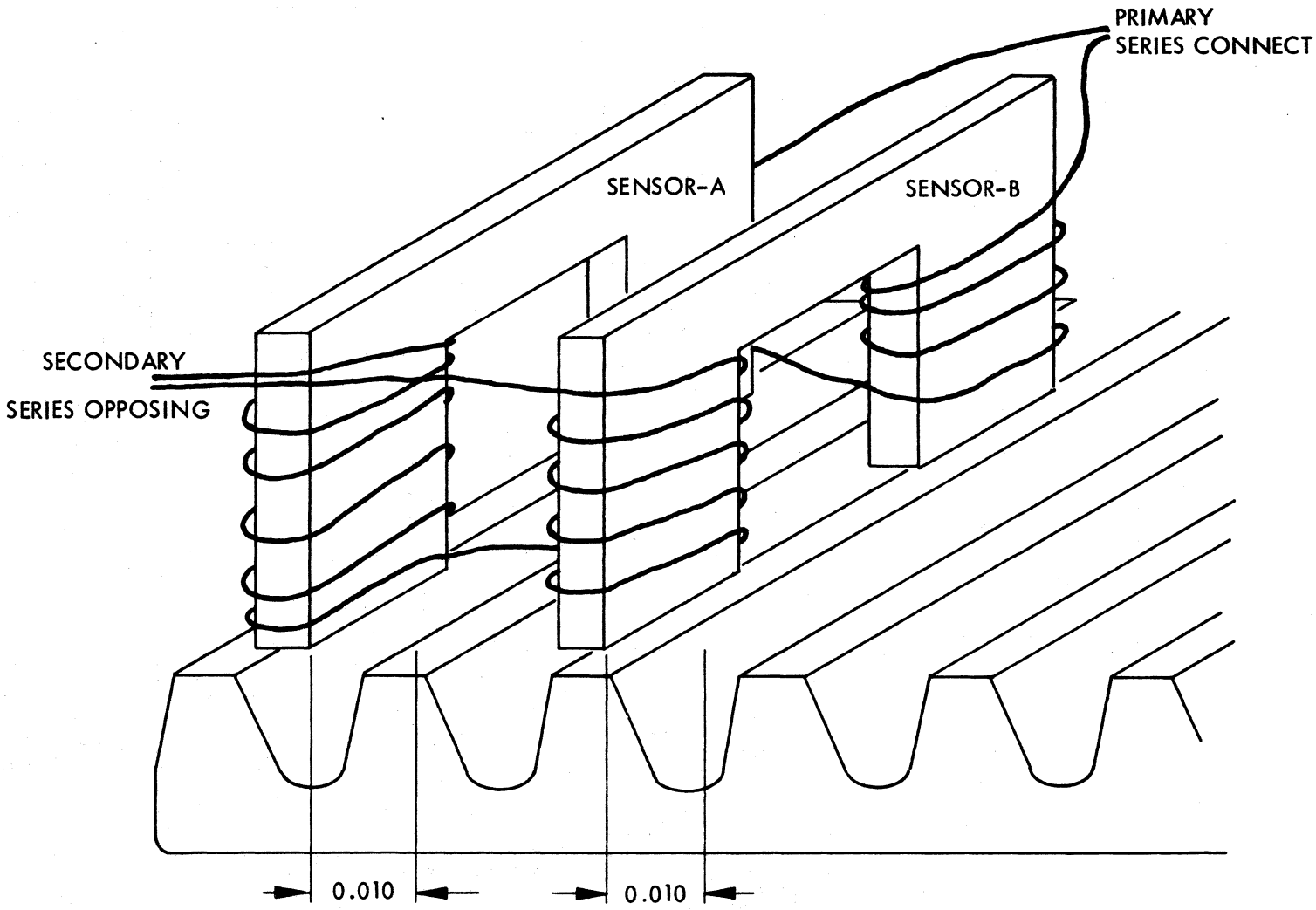
There are two basic movements in the Model 630 which must be monitored: (1) the linear travel of the carriage along its way and (2) the rotary motion of the disc pack on its spindle.

As the heads are positioned from one cylinder to another within the disc pack, it is necessary to keep an accurate count of the number of cylinders passed. This is accomplished by a variable reluctance transducer mounted on the carriage way at one end of the detent pawls facing the detent rack. See Figures 2-12 and 2-13.

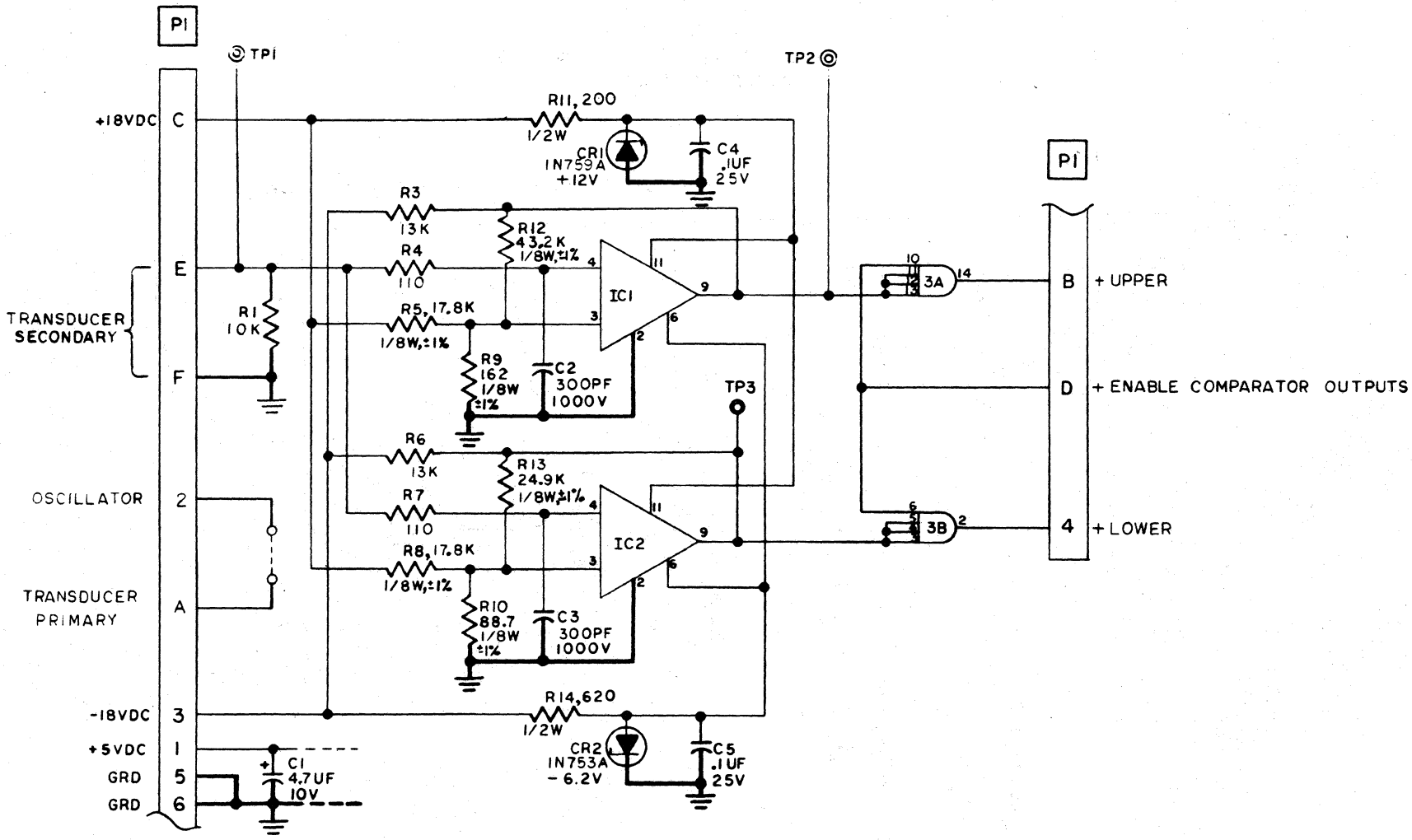
This cylinder transducer contains two sets of paired primary and secondary coils. See Figure 2-14. The two sets are separated from one another so that while one is opposite a rack tooth, the other is opposite a valley. The primaries are wired in series and excited at 145 kc at about 5 volts. Each time a rack tooth passes a primary-secondary pair, it couples them. The coupling indicates to an up-down counter in the logic that another cylinder has been reached by the read/write heads. The peak-to-valley spacing allows each rack tooth to be counted twice to give a 0.010-inch cylinder spacing indication. Figure 2-15 is a schematic of the cylinder transducer circuit and Figure 2-16 shows the sequence of pulse shapes as seen on a scope when rack teeth pass the cylinder transducer.

Home position (cylinder 000) is detected using the forward carriage stop as a starting point. Whenever the heads must be positioned to home from a location without a known address, they are first sent to the forward stop, which is assigned an address of 204. A reverse seek of 204 cylinders is initiated; when zero difference count (compare) condition is reached, the carriage is detented. This is home position.

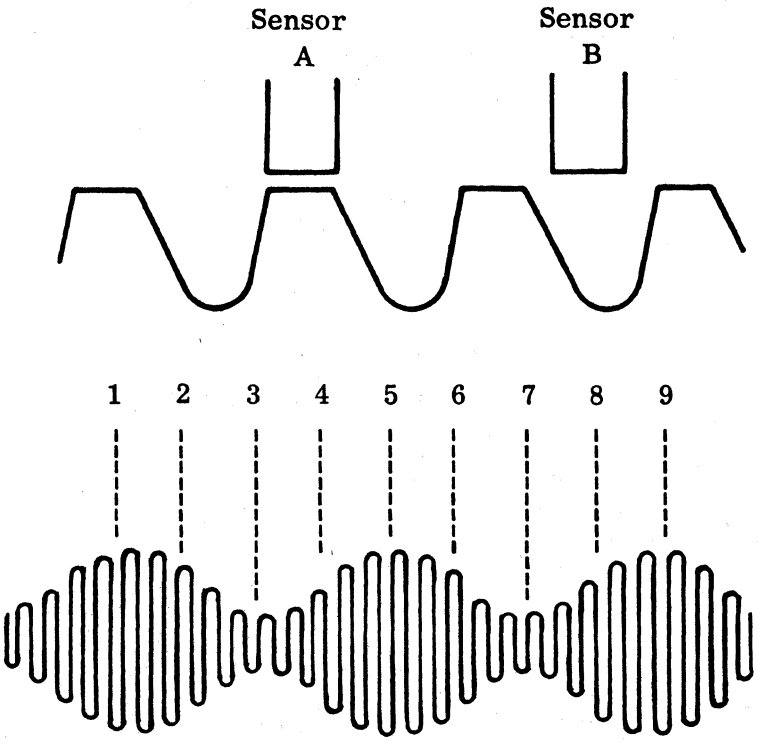
Certain safety circuits need to know whether the heads are extended or retracted. A double microswitch mounted on the carriage way near the positioning motor is switched off when the heads are retracted and on when they are extended. See Figure 2-17.



Cylinder Transducer
Primary and Secondary Pairs
Figure 2-14

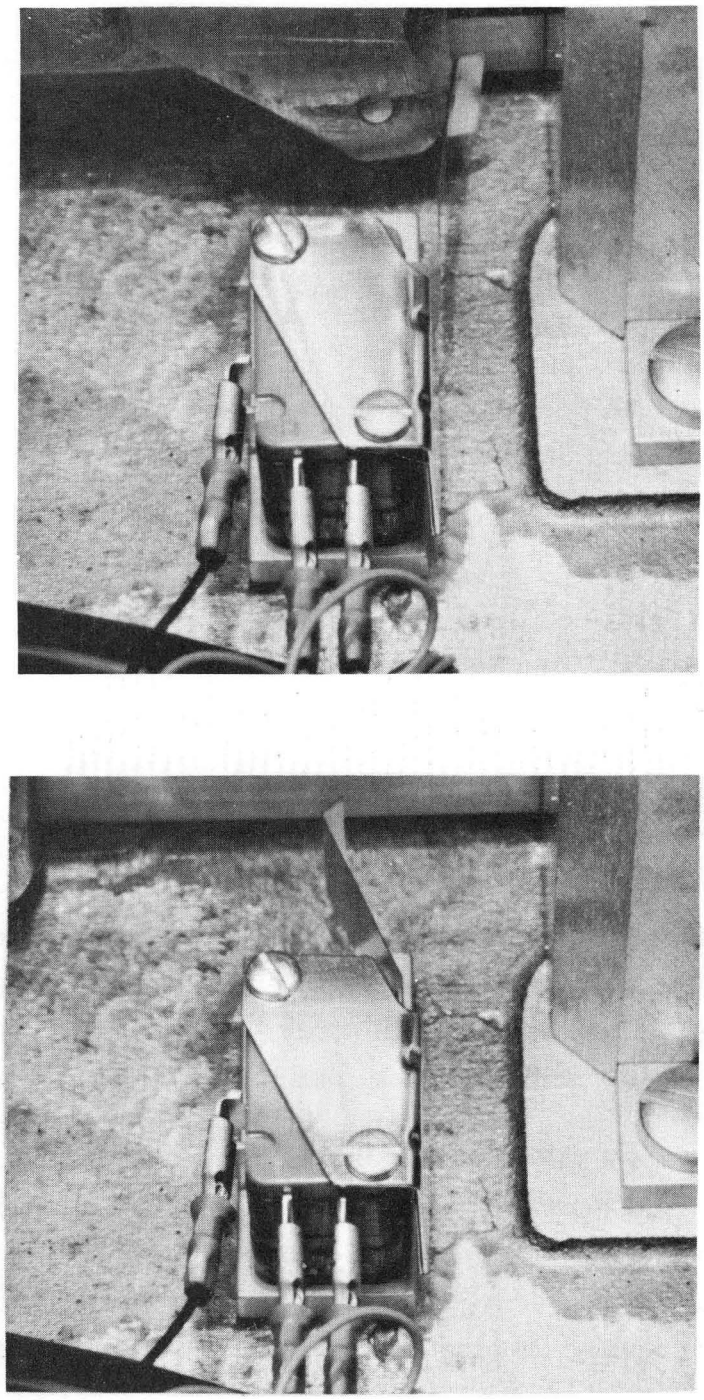


Cylinder Transducer
Circuit Schematic
Figure 2-15



1. Sensor A is fully coupled by a tooth; sensor B is opposite a valley.
2. Tooth moving away from A; another tooth approaching B; trigger point.
3. Equal coupling of both sensors; null point.
4. Coupling of A approaching minimum; coupling of B approaching maximum; trigger point.
5. Sensor A opposite a valley; sensor B fully coupled by a tooth.
6. Tooth approaching sensor A; tooth moving away from B; trigger point.
7. Equal coupling of both sensors; null point.
8. Tooth approaching sensor A; tooth moving away from B; trigger point.
9. Sensor A fully coupled by a tooth; sensor B is opposite a valley.

Cylinder Transducer Output When Counting
Figure 2-16



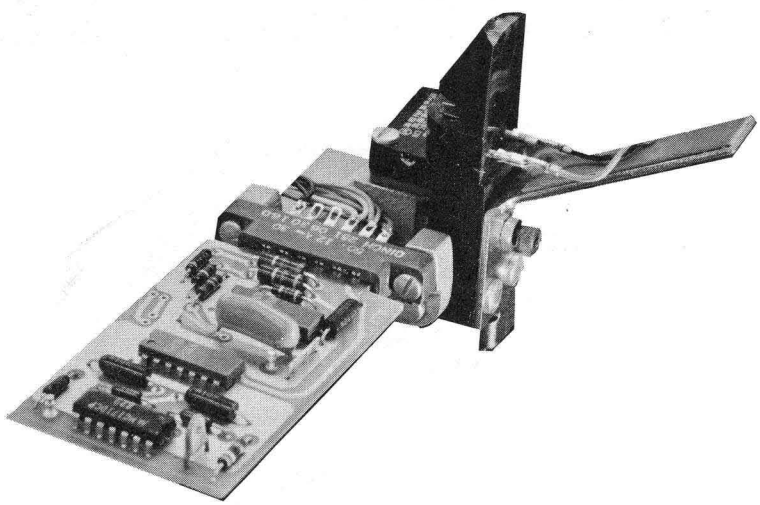
(024-660)

Heads Retracted/Extended Switch

Figure 2-17

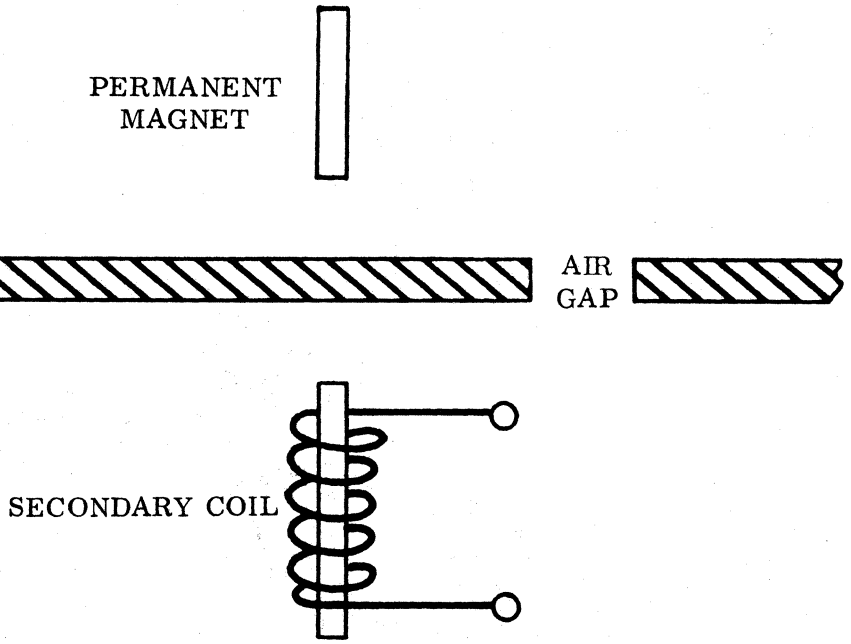
Rotational speed of the disc pack and location of index are monitored by the index transducer (Figure 2-18), which is mounted facing the spindle. When a disc pack is installed, the edge of the slotted disc on the bottom of the pack separates a permanent magnet from a single coil (Figure 2-19). As the pack rotates, the slots pass between the magnet and coil. Since the disc is aluminum, there is minimum coupling when the air gap between the magnet and coil is blocked by the disc and maximum coupling when the slots appear

The edge of the disc contains 20 evenly spaced single slots (sector slots). Close to one of the sector slots is another slot which marks index for the disc pack. See Figure 2-20. As the disc pack rotates and each sector slot is detected, a pulse from the index transducer comparator sets a flip-flop in the index/sector logic. The flip-flop resets itself following a delay. The relationship between the length of the delay and the sector slot spacing is such that the delay times out before the next sector slot reaches an AND gate in the index/sector logic. Output of the reset flip-flop ANDs with the sector slot pulse to generate a sector signal. The pulse generated by the index pulse reaches another AND gate before the flip-flop can time out so that the output of the set flip-flop ANDS with the index slot pulse to generate an index signal. The sector signals and index signals are used by the controller to synchronize read/write operations. Figure 2-21 illustrates coupling output during index detection.



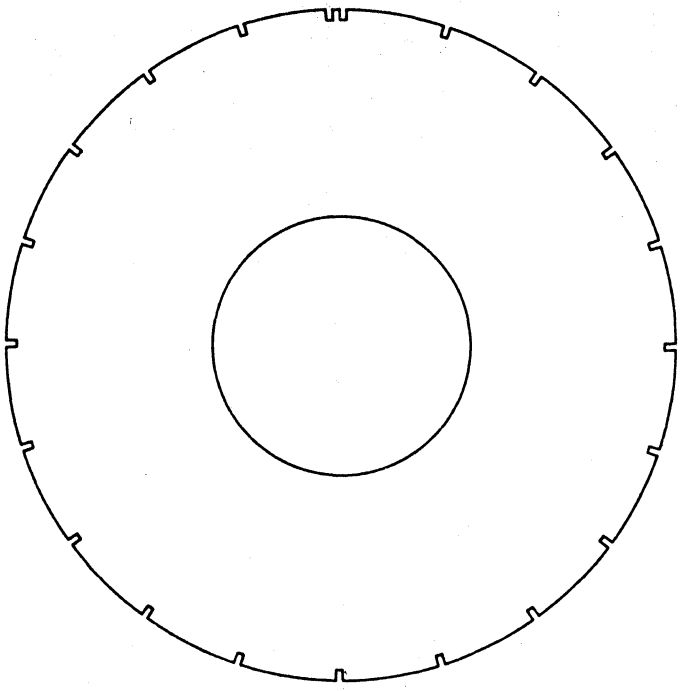
Index Transducer
Figure 2-18

The logic that determines whether or not the disc pack has reached minimum operating speed relies on two delays. Each delay is initiated by the arrival of alternate index pulses. As the disc pack accelerates from rest, the interval between the arrival of index pulses at the logic decreases until one of the delays does not have time to time out. This causes a flip-flop to set. The next index pulse arrives before the other delay times out, causing its flip-flop to set. The output of the two set flip-flops is ANDed to produce a signal which indicates that the disc pack has reached minimum operating speed. Figure 2-22 illustrates the timing relationships in the up speed detection logic. Refer to the logic description for logic diagram 200616 for a more detailed explanation of the timing diagram.



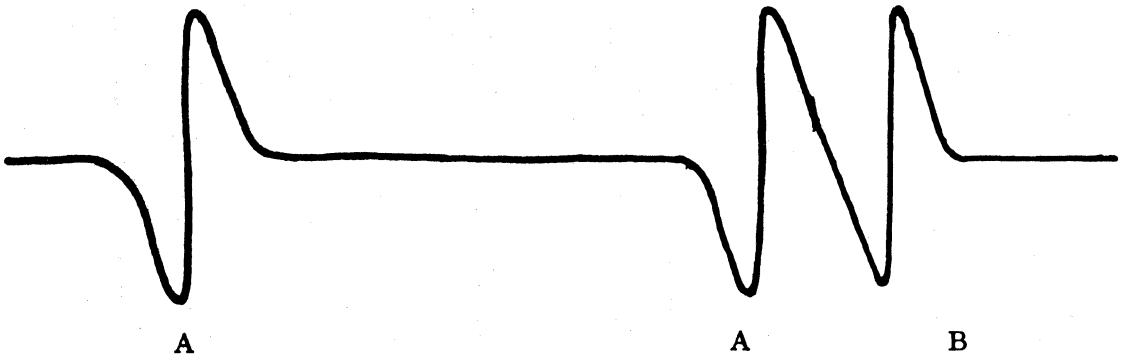
Coil and Slot Relationship

Figure 2-19



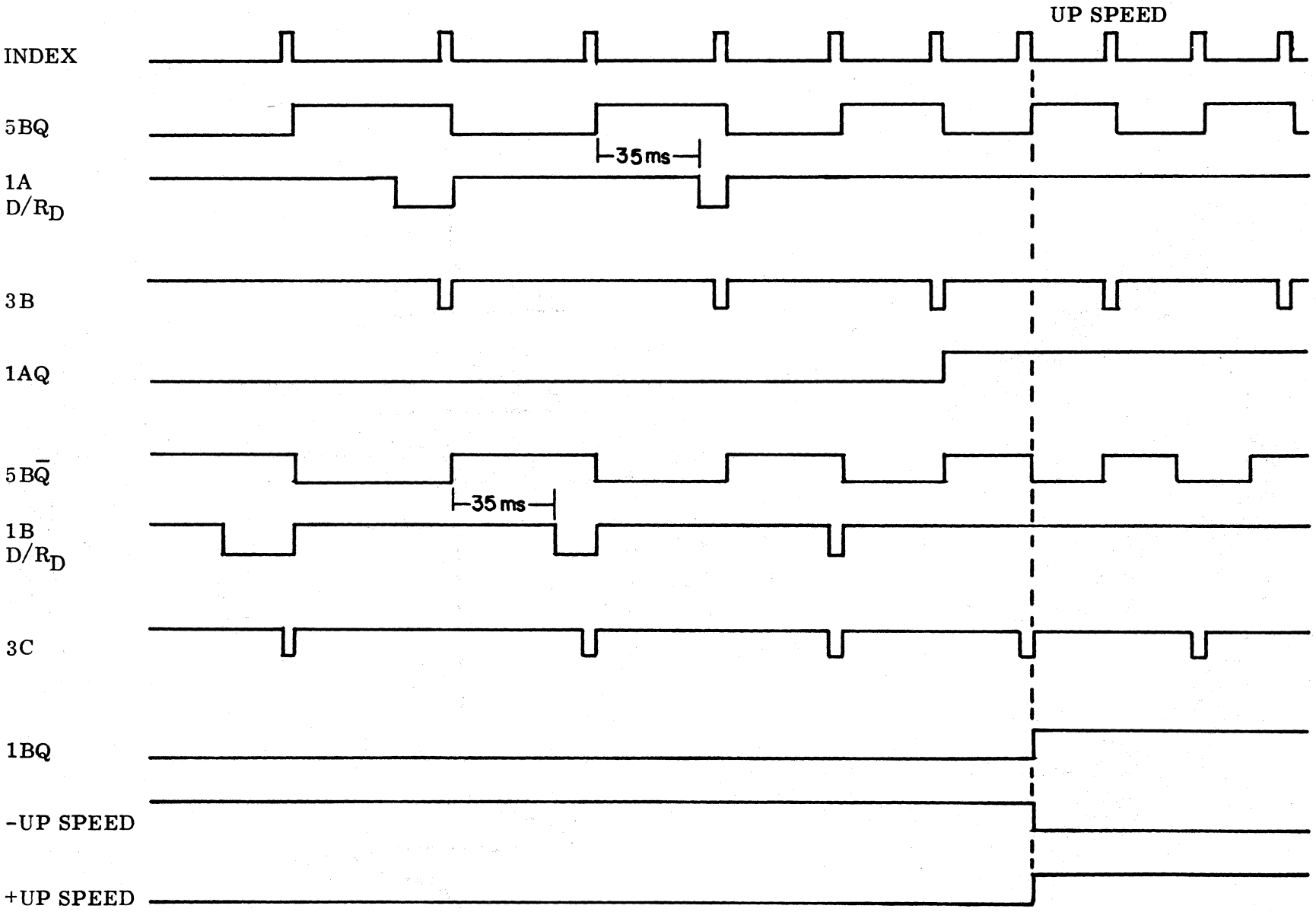
Index/Sector Disc
Figure 2-20

Index/Sector Disc
Figure 2-20



A - Sector pulses
A and B - Index

Index Detection Output
Figure 2-21



Up-Speed Detection

Figure 2-22

2.3.4.5 Spindle Drive System

Rotation of the disc packs is provided by the spindle drive system which includes the disc pack drive motor, spindle and drive belt. See Figure 2-23.

The disc pack drive system is powered by a one-half horsepower, 60- or 50-Hz, single-phase ac motor. As shown in Figure 2-24, the motor transfers torque to the spindle drive pulley by a simple belt loop. Tension on the belt is maintained by a special motor shock mounting; no idler pulley is used.

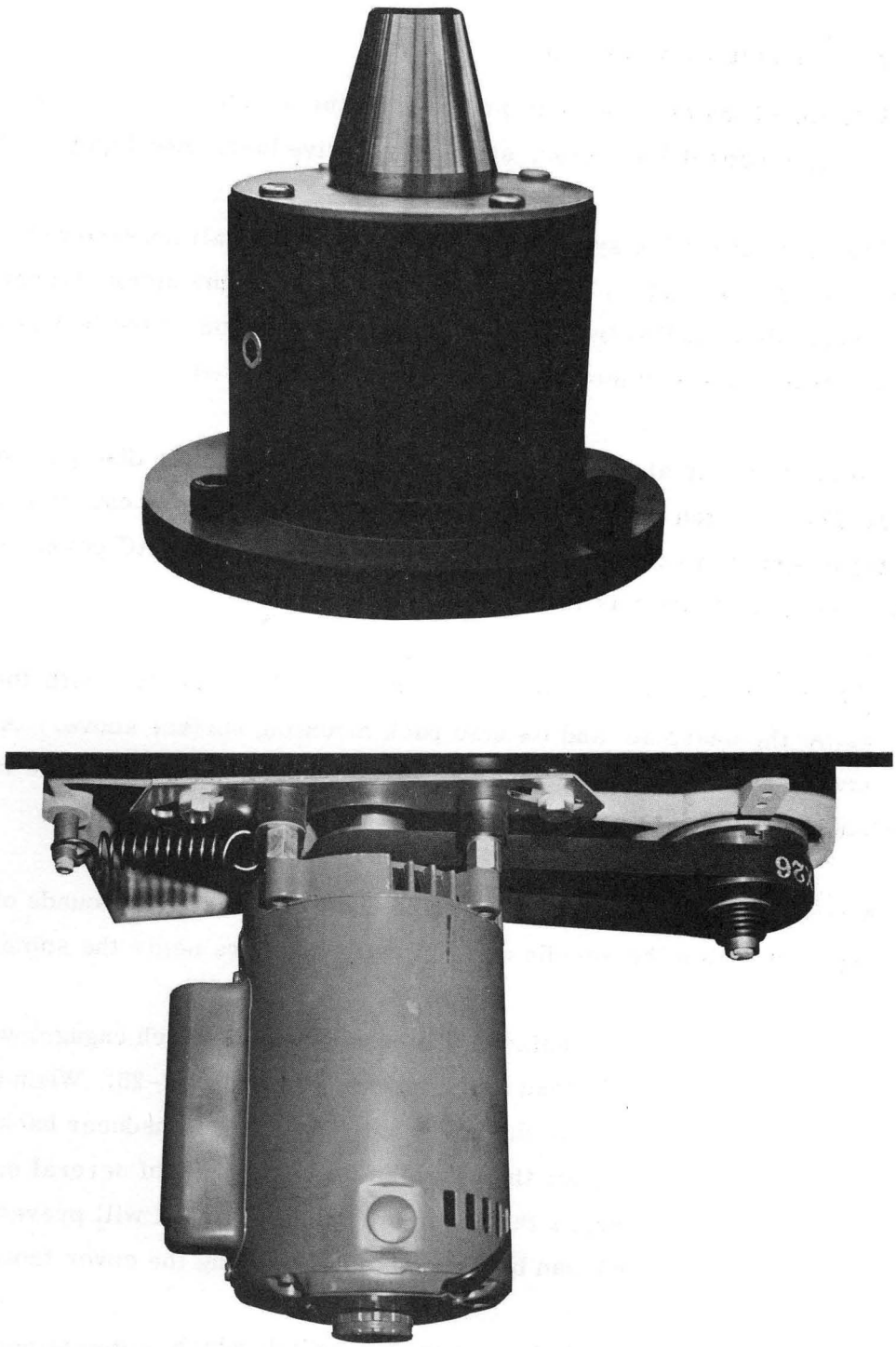
The drive motor also serves as a dynamic brake for the disc pack drive. When the STOP switch is depressed, ac power to the motor is cut off and dc power (36 volts) is applied to the motor coil for about 10 seconds. AC power is also cut off when the cabinet cover is lifted.

The disc pack spindle is bolted into a hole in the baseplate with the spindle pulley below the baseplate and its disc pack mounting surface above. A speed ratio between the motor pulley and the spindle pulley reduces spindle rotation to a maximum of 2400 $\pm$ 48 rpm.

A disc pack is secured to the spindle cone with 206 $\pm$ 32 pounds of force by a locking shaft within the spindle and Belleville washers below the spindle pulley.

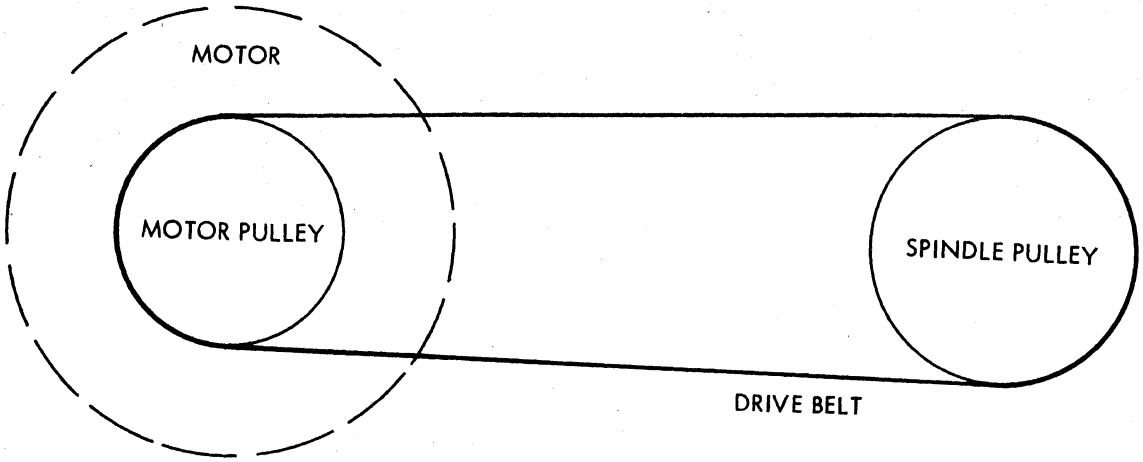
The spindle assembly includes a mechanical lock which engages when the top cover is raised to load or unload a disc pack. See Figure 2-25. When the cabinet cover is lifted, a nylon arm on the cover tilts the index transducer back. This movement causes a pawl under the baseplate to engage one of several notches in the spindle pulley. As long as the cover is raised, the pawl will prevent the spindle from turning. This lock can be bypassed by removing the cover from the machine.

The assembly also includes a pack-on switch which automatically closes when a disc pack is installed (see Figure 2-26). The pack-on switch is a safety feature and must be closed for the drive motor to operate.

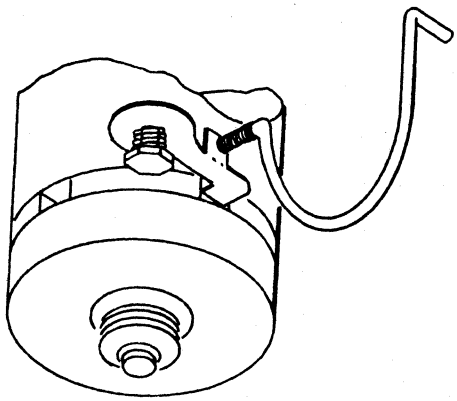


Spindle Drive System

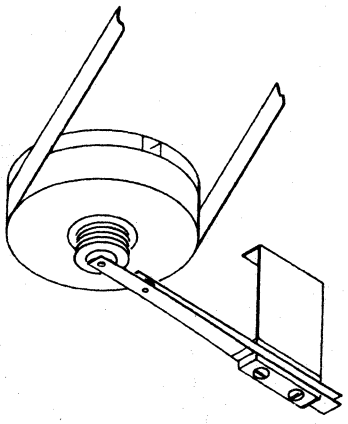
Figure 2-23



Simple Belt Drive
Figure 2-24



Mechanical Spindle Lock
Figure 2-25



Pack-On Switch
Figure 2-26

2.3.5 Logic Standards and Symbols

Output of the AND function, as it is used in Model 630 logic, is "active" when all its inputs are "active". Any "nonactive" AND inputs will cause a "nonactive" output. Output of the OR function is "active" when any one or more input(s) are "active". All "nonactive" OR inputs will cause a "nonactive" output.

Note that the above activity definitions do not refer to logical one, logical zero or electrical reference states.

The level required (high or low) for the active state of an input or output of any particular logic element is indicated by an active state symbol attached to the logic element symbol.

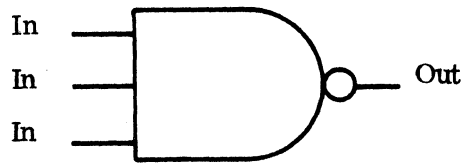
A small circle at the input(s) indicates that a relatively low input signal activates the function. Conversely, the absence of a small circle indicates that a relatively high input signal activates the function. A small circle at the output indicates that the output of the activated function is relatively low. Absence of a small circle at the output indicates that the output of the activated function is relatively high.

The presence of an indicated active output does not necessarily provide a useful input to other elements. It may prevent the operation of some and enable others. Conversely, the absence of the indicated output signal state may provide a useful input to elements in the logical net and prevent the operation of others.

Voltage levels for the two states are:

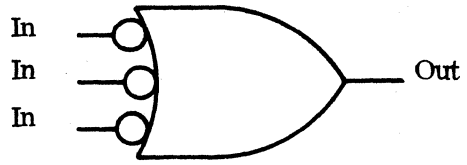
High	Logical 1	+5v
Low	Logical 0	0v (ground)

The following logic symbols and definitions outline the rules governing symbology for the Model 630 logic diagrams.



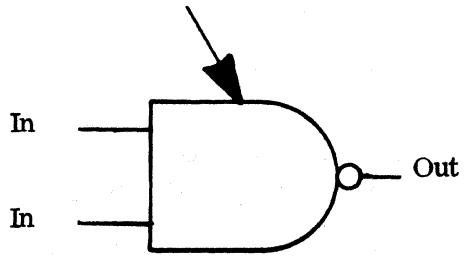
AND Function (NAND Gate)

Output is low only if all inputs are high.



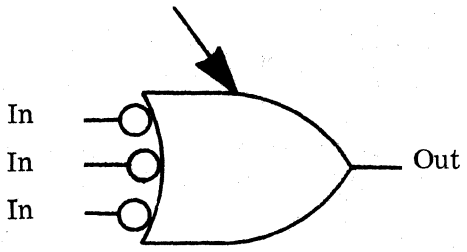
OR Function (NOR Gate)

Output is high if any input is low.

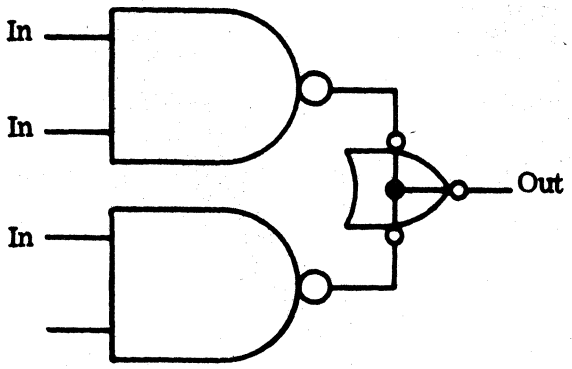


AND Function (with Expander Input)

The expander input does not alter the function of the gate. Its purpose is to provide a greater number of inputs.

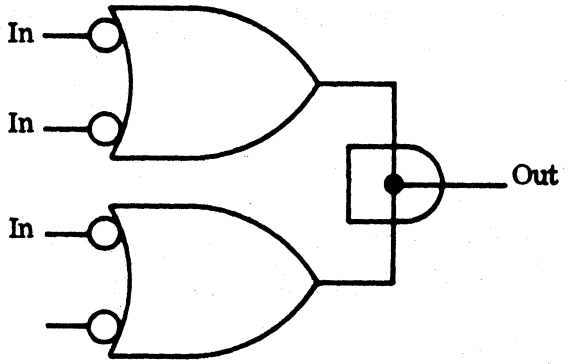


OR Function (with Expander Input)



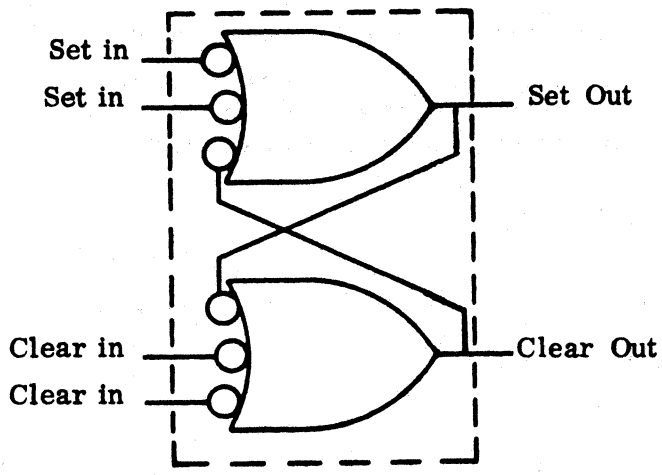
Collector OR* (DOT OR)

The output is active (low) if either or both inputs are low.



Collector AND* (DOT AND)

The output is active (high) only if both inputs are high.



FLIP-FLOP (Latch)

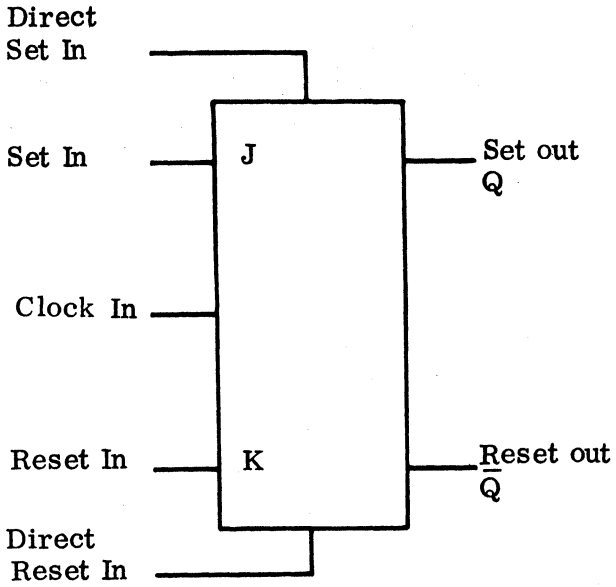
This device stores a single bit. It has two sets of inputs: SET and RESET. It has two possible outputs: SET and RESET.

If any SET input is low and all RESET inputs are high, SET out will be high.

If any RESET input is low and all SET inputs are high, RESET out will be high.

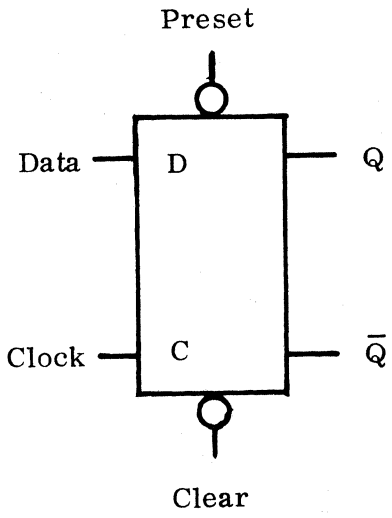
If all inputs are high (SET and RESET), the latch will maintain its last state.

* Collector gates are tie points. The symbols represent a meeting of two logic outputs.



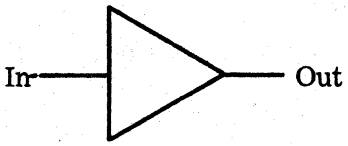
JK FLIP FLOP

- If J input is high while all others (Direct Set, Direct Reset and Reset) are low, Q will go high with the trailing edge of the next clock pulse.
- If K input is high while all others are low, $\overline{Q}$ will go high with the trailing edge of the next clock pulse.
- If both J and K are high, the output will alternate between Q and $\overline{Q}$ with the trailing edge of each clock pulse.
- If Direct Set is high, J and K are not both high, the clock is low and Direct Reset is low, Q out will be high.
- If Direct Reset is high, J and K are not both high, the clock is low and Direct Set is low, $\overline{Q}$ out will be high.
- If J, K, Direct Set and Direct Reset are all low, the latch will ignore any clock pulses and remain in its last state.



D-Type edge triggered F. F.

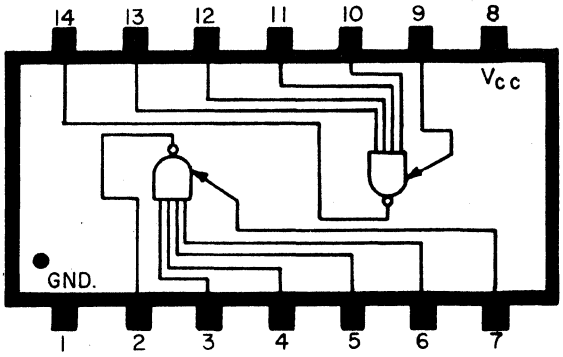
- If D input is high, PRESET is high and CLEAR high, Q will go high on leading edge of clock.
- If D input is low, PRESET is high and CLEAR is high, $\overline{Q}$ will go high on leading edge of clock.
- PRESET and CLEAR are independent of D and C inputs.



Amplifier. The amplifier may have one or more stages, and may or may not produce gain or inversion.

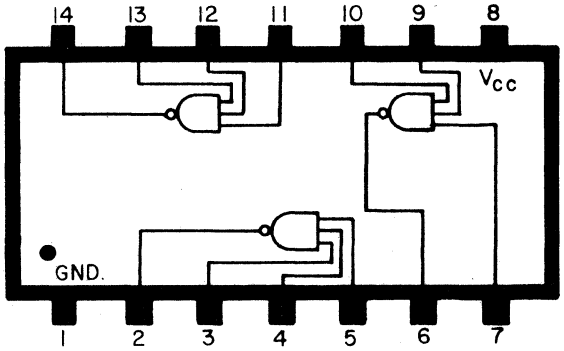
General Logic symbol, for functions not specified. Symbol must be labeled so as to define the function performed.

The IC components used in the Model 630 are defined below.

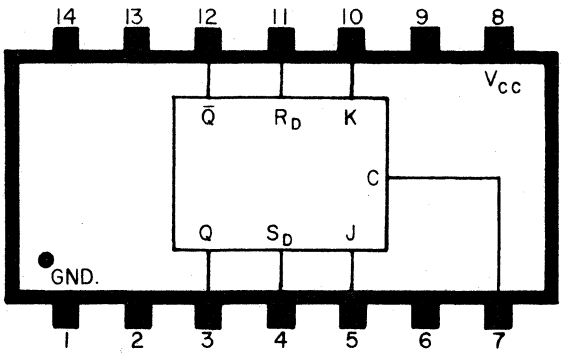


616A

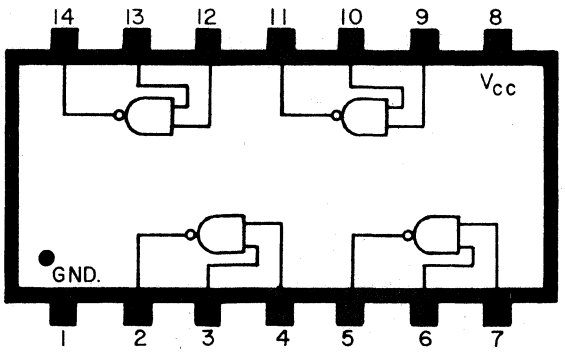
659A



670A



620A



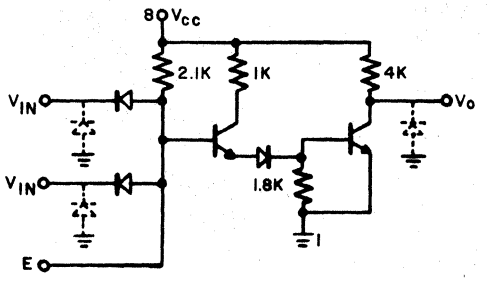
680A

BASIC GATE CIRCUIT

616A

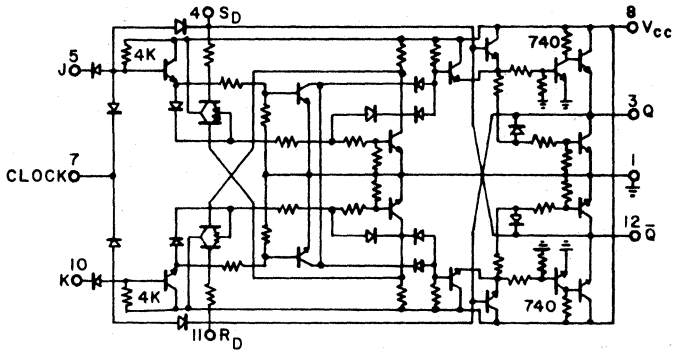
670A

680A



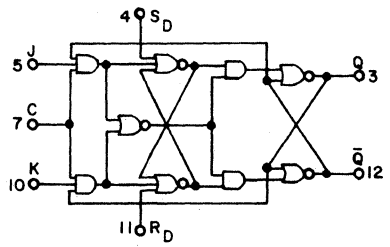
Component values shown are typical.

620A



Component values shown are typical

620A

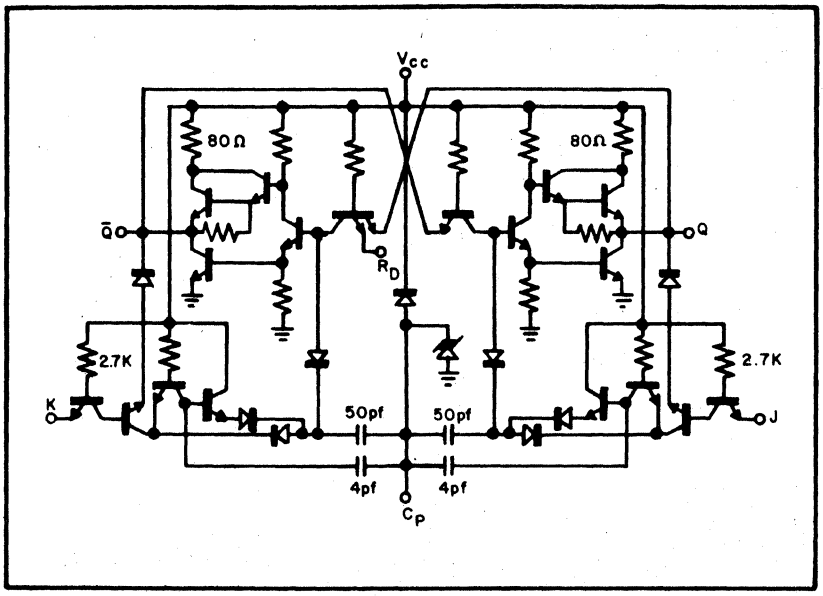


TRUTH TABLE

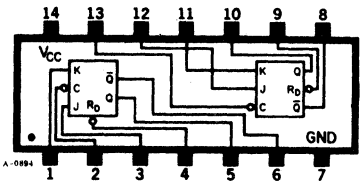
J	K	Q
0	0	Q
0	1	0
1	0	1
1	1	$\bar{Q}$

Synchronous Inputs at clock time

S_D	R_D	Q
0	0	Q
0	1	0
1	0	1
1	1	NO Change



8826A PACKAGE



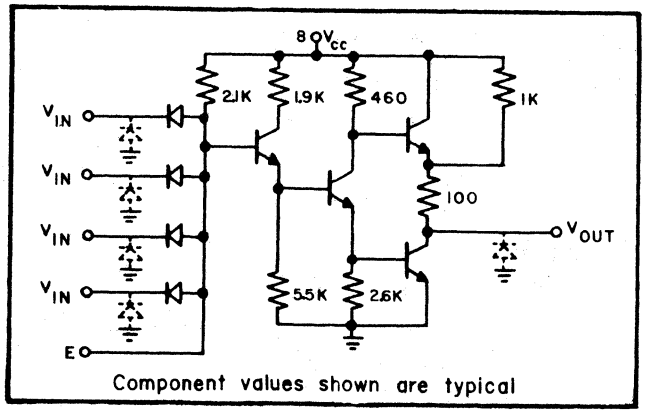
TRUTH TABLE

J_n	K_n	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\bar{Q}_n$

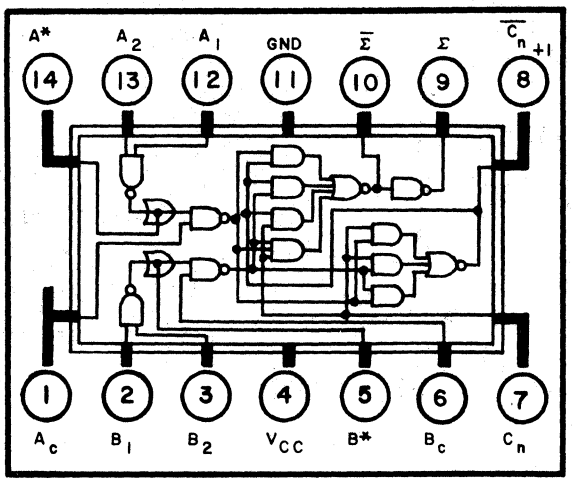
$R_D = 0 \Rightarrow Q = 0$

n is time prior to clock
n+1 is time following clock

8826A



Buffer/Driver
Element - 659A



ADDER

SN7480

TRUTH TABLE (See Notes 1, 2, and 3)

C_n	B	A	$\overline{C_{n+1}}$	$\overline{\Sigma}$	Σ
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

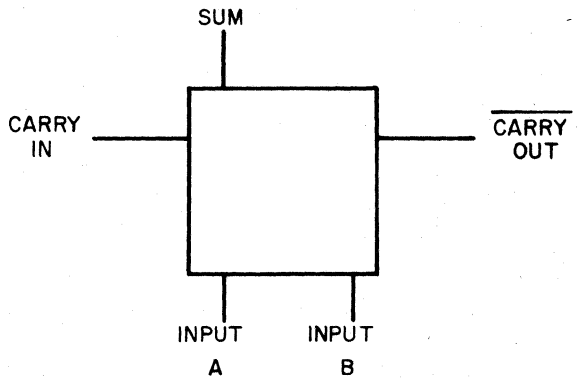
SN7480

NOTES: 1. $A = \overline{A\bigstar \bullet A_C}$, $B = \overline{B\bigstar \bullet B_C}$

Where $A\bigstar = \overline{A_1 \bullet A_2}$, $B\bigstar = \overline{B_1 \bullet B_2}$

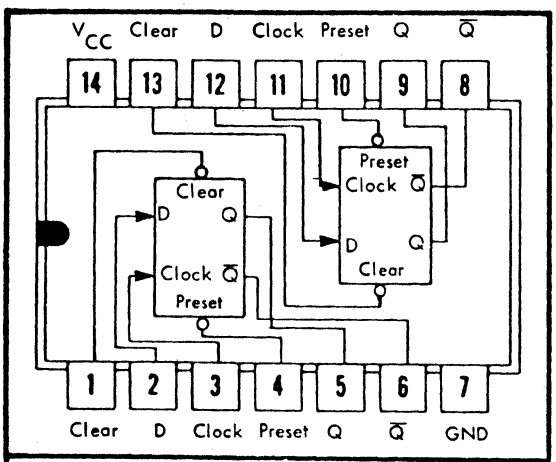
2. When A★ or B★ are used as inputs, A_1 and A_2 or B_1 and B_2 respectively must be connected to GND.

3. When A_1 and A_2 or B_1 and B_2 are used as inputs, A★ or B★ respectively must be open or used to perform Det-OR logic.



SN7480

SN7474N
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP



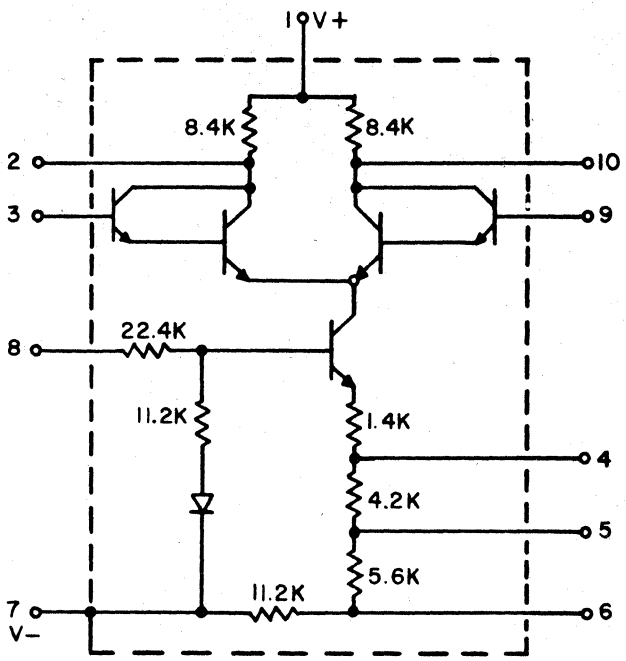
positive logic

a. Low input to clear sets Q to logical 0.
b. Low input to preset sets Q to logical 1.
c. Clear or preset inputs dominate regardless of clock and D inputs

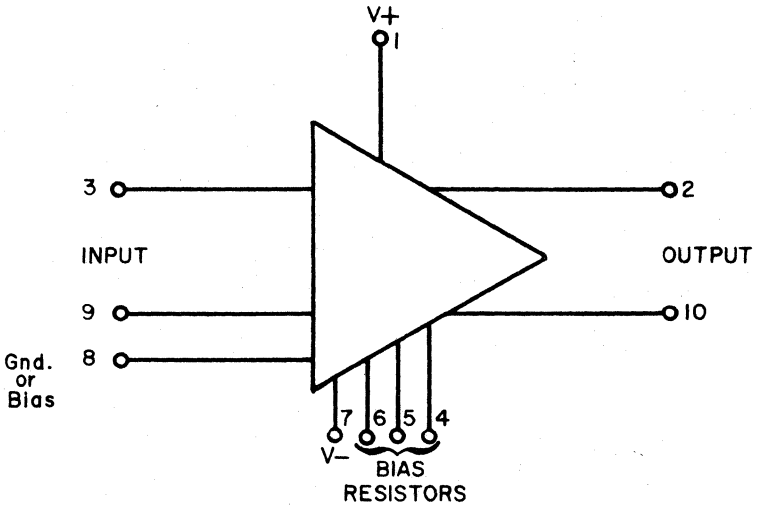
TRUTH TABLE (Each Flip-Flop)

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\overline{Q}$
0	0	1
1	1	0

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

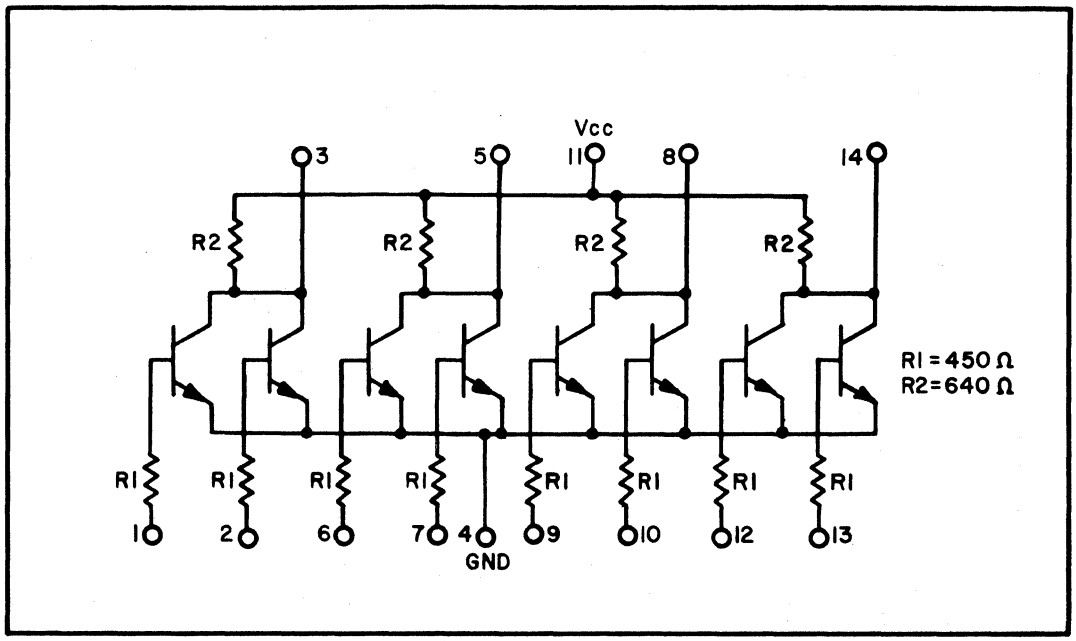


MC1429G



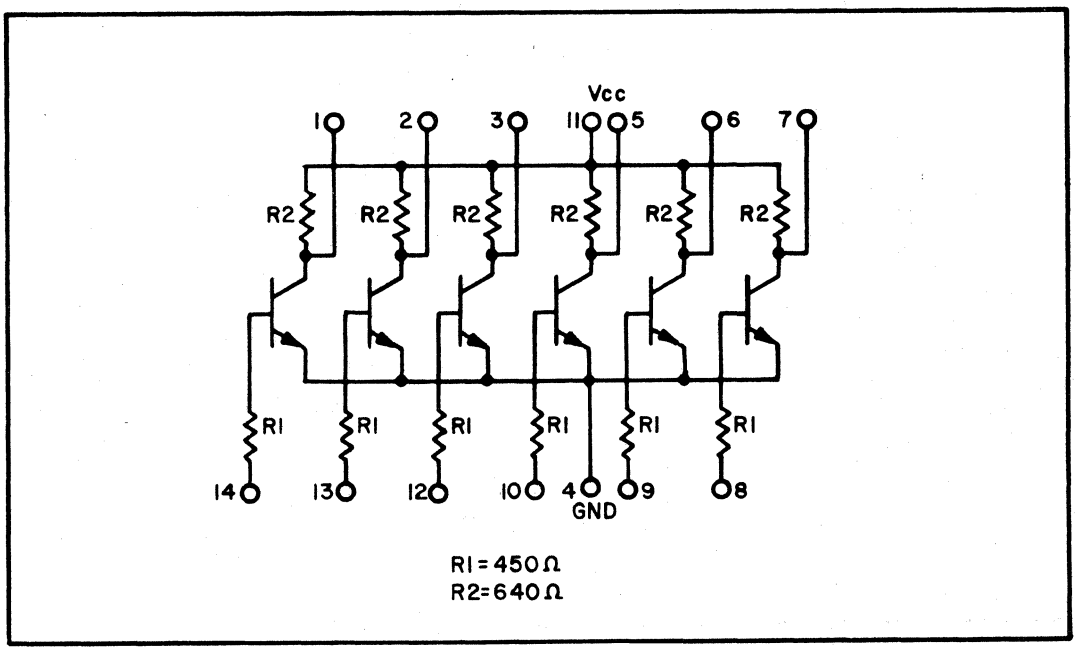
MC1429G

EQUIVALENT CIRCUIT

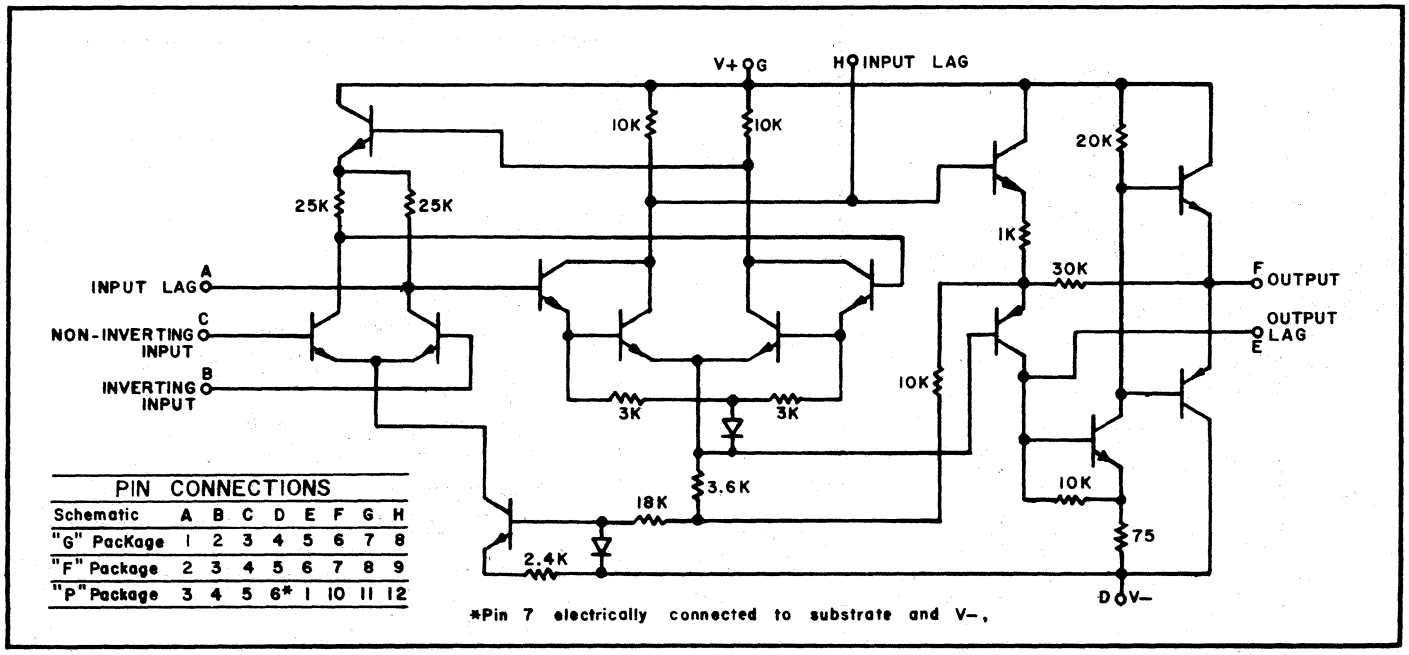


RESISTOR VALUES ARE TYPICAL

SERVO AMPLIFIER
MC724P

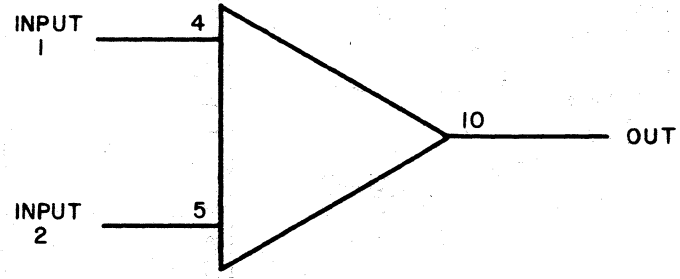


LINE RECEIVER
MC789P



PIN CONNECTIONS								
Schematic	A	B	C	D	E	F	G	H
"G" Package	1	2	3	4	5	6	7	8
"F" Package	2	3	4	5	6	7	8	9
"P" Package	3	4	5	6*	1	10	11	12

MC1709C



SECTION 3.0

THEORY OF OPERATION

The theory of operation for a Model 630 is defined by a set of operational flow charts and pertinent timing diagrams. These flow charts include:

A. Power up, power sequencing

B. First seek

C. Programmed seek (three sheets)

D. Restore-retract

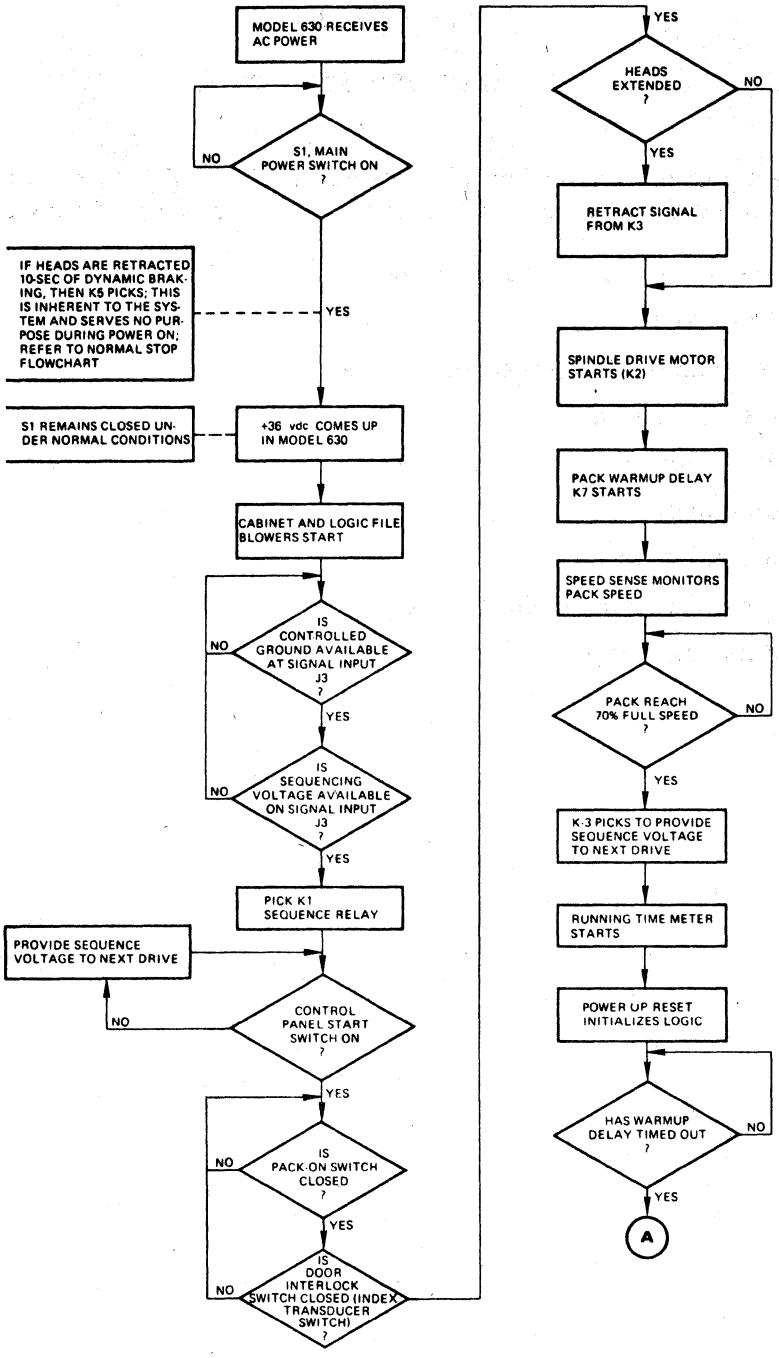
E. Write operation

F. Read operation

G. Normal stop

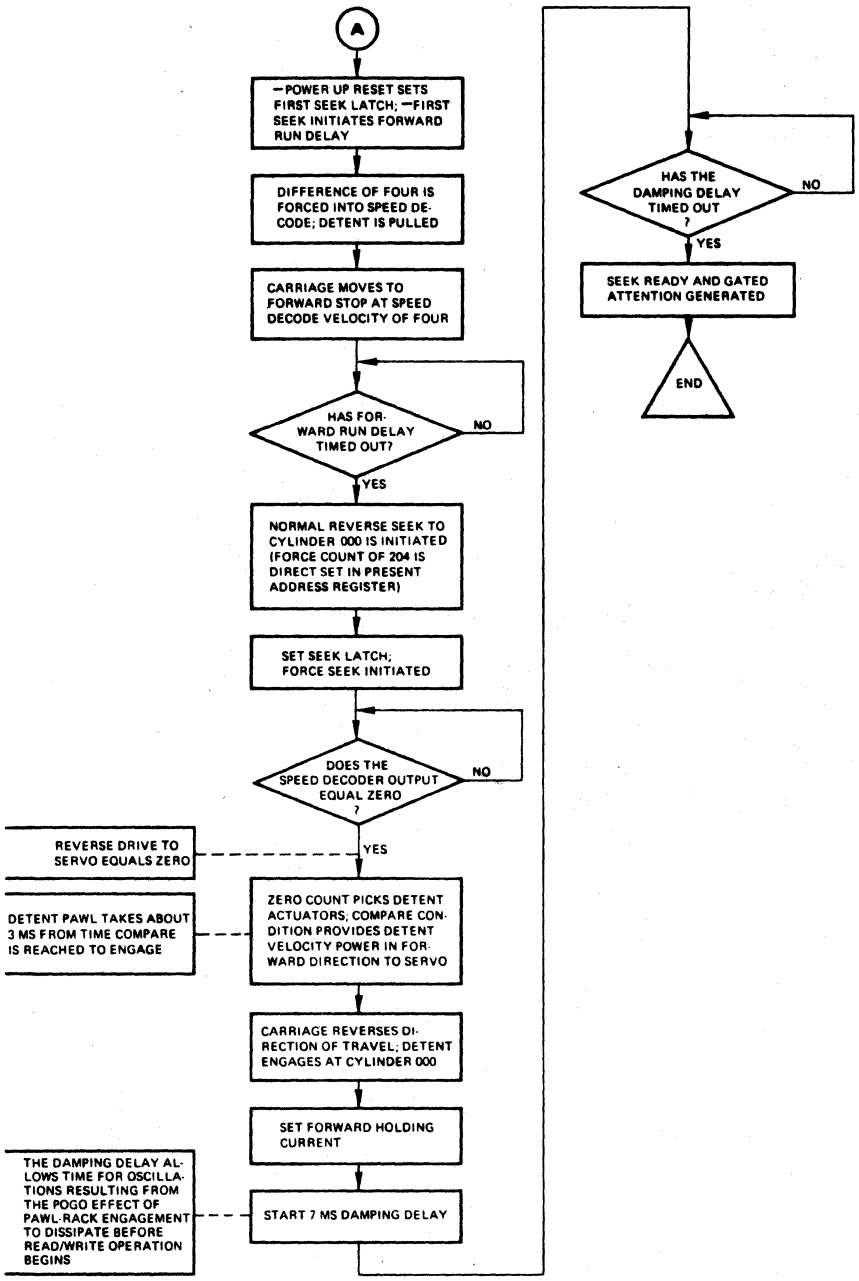
H. Controlled power down

I. Abnormal stop



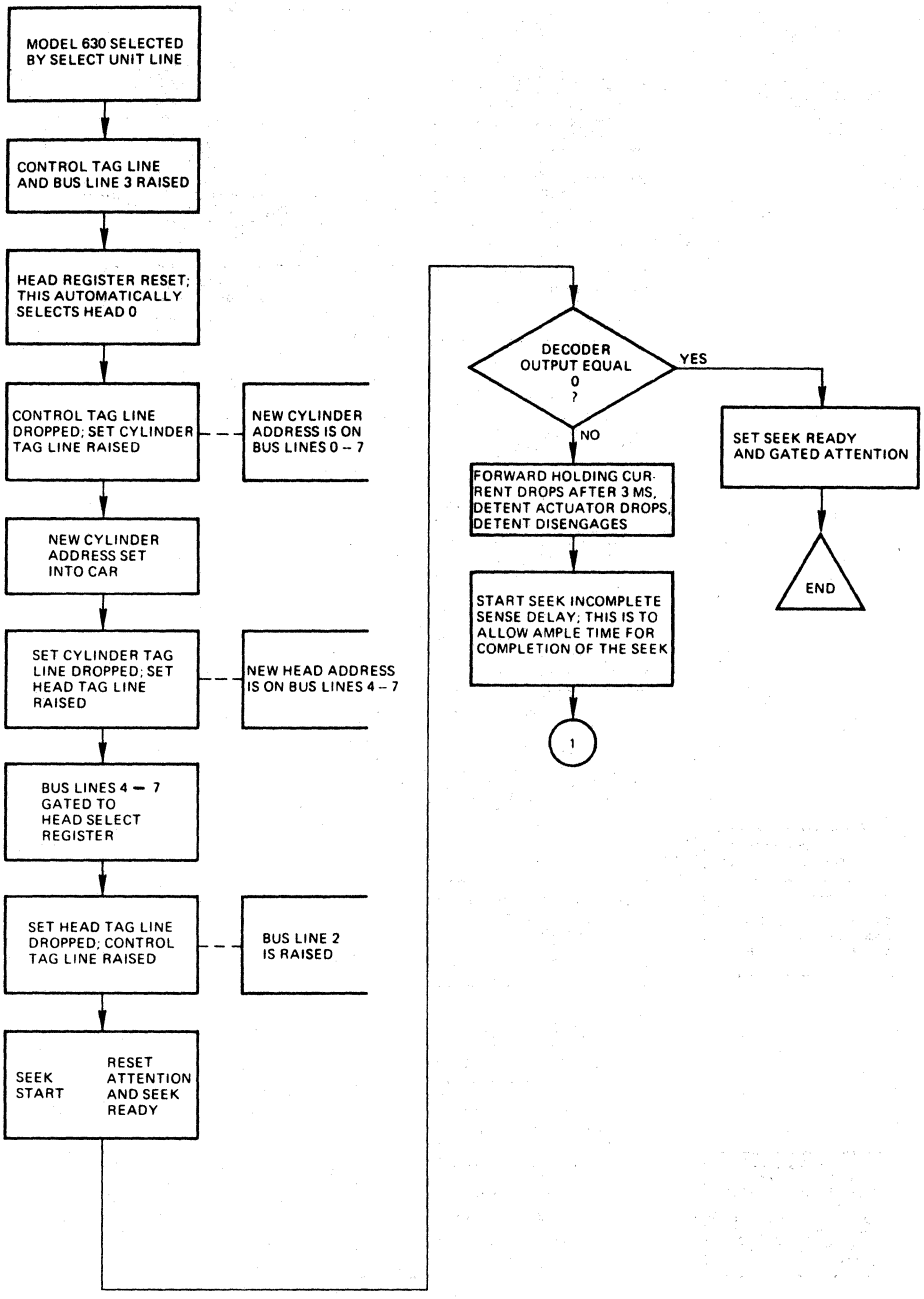
Power Up, Power Sequencing

Figure 3-1



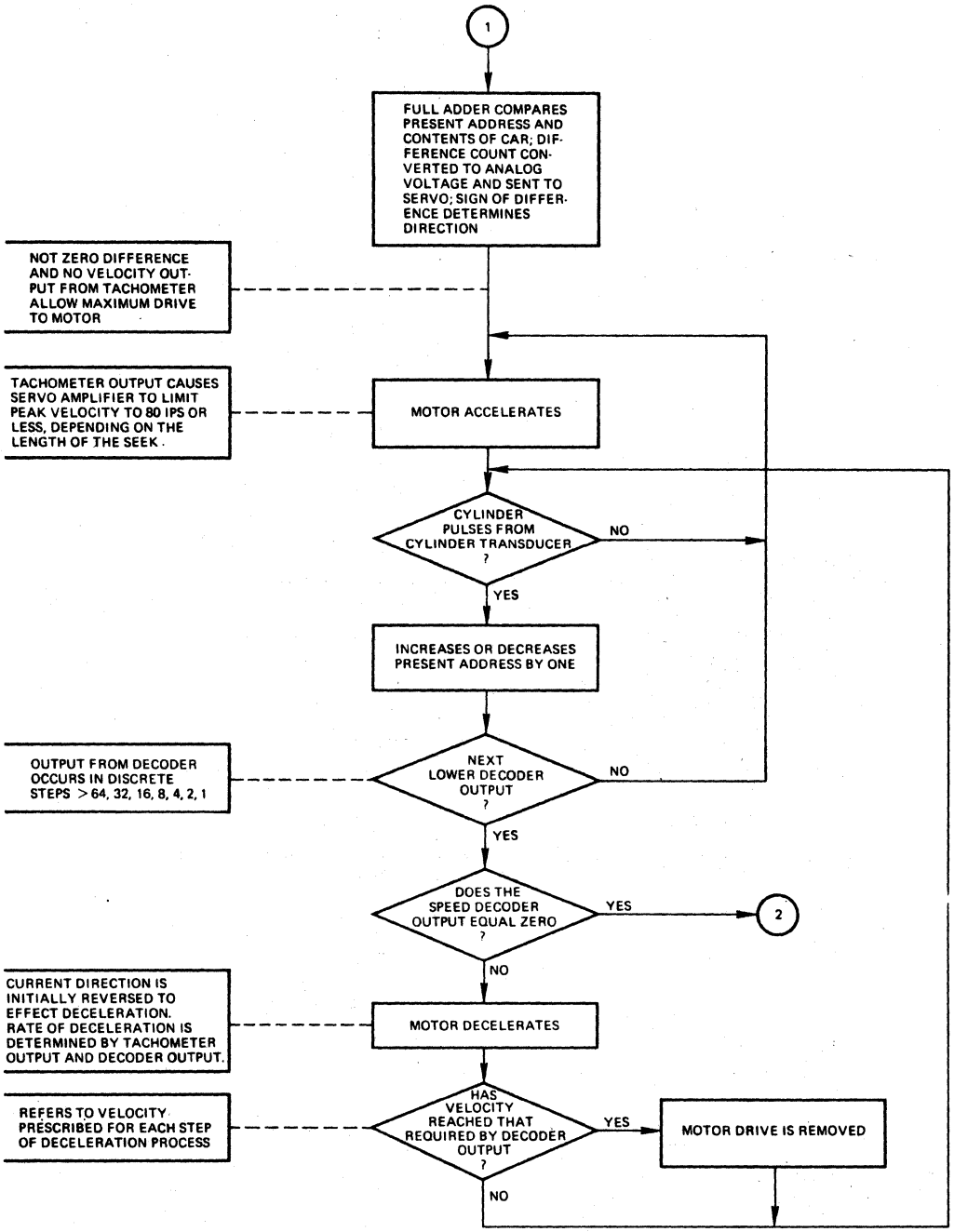
First Seek

Figure 3-2



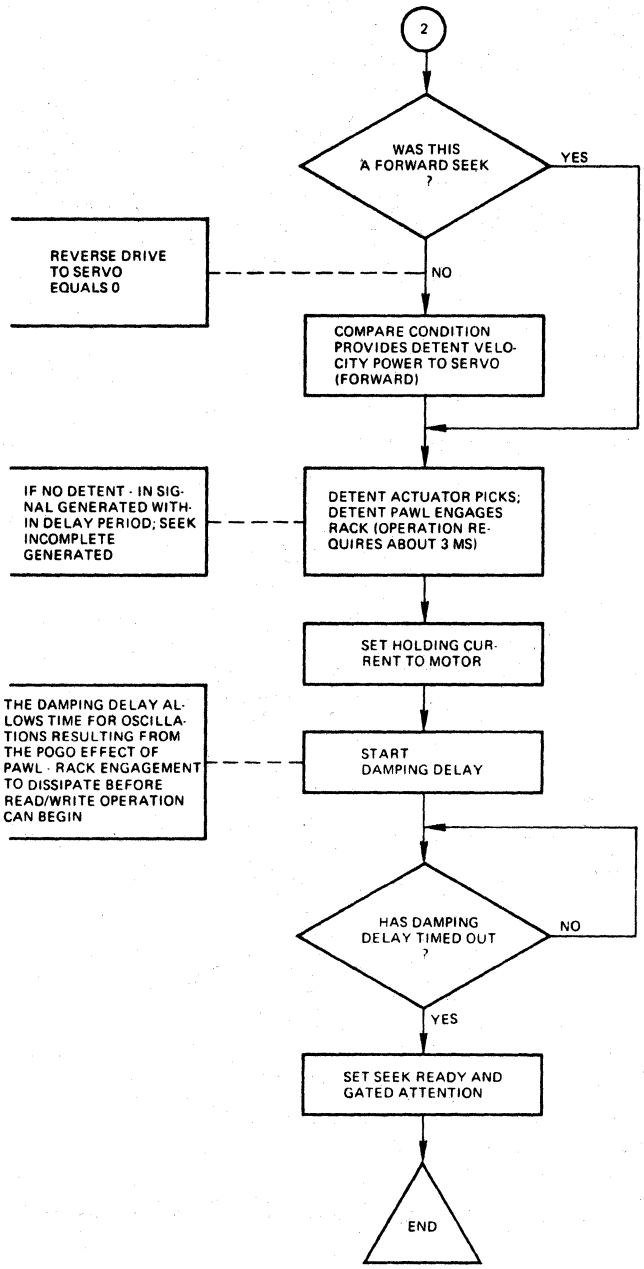
Programmed Seek (Sheet 1 of 3)

Figure 3-3

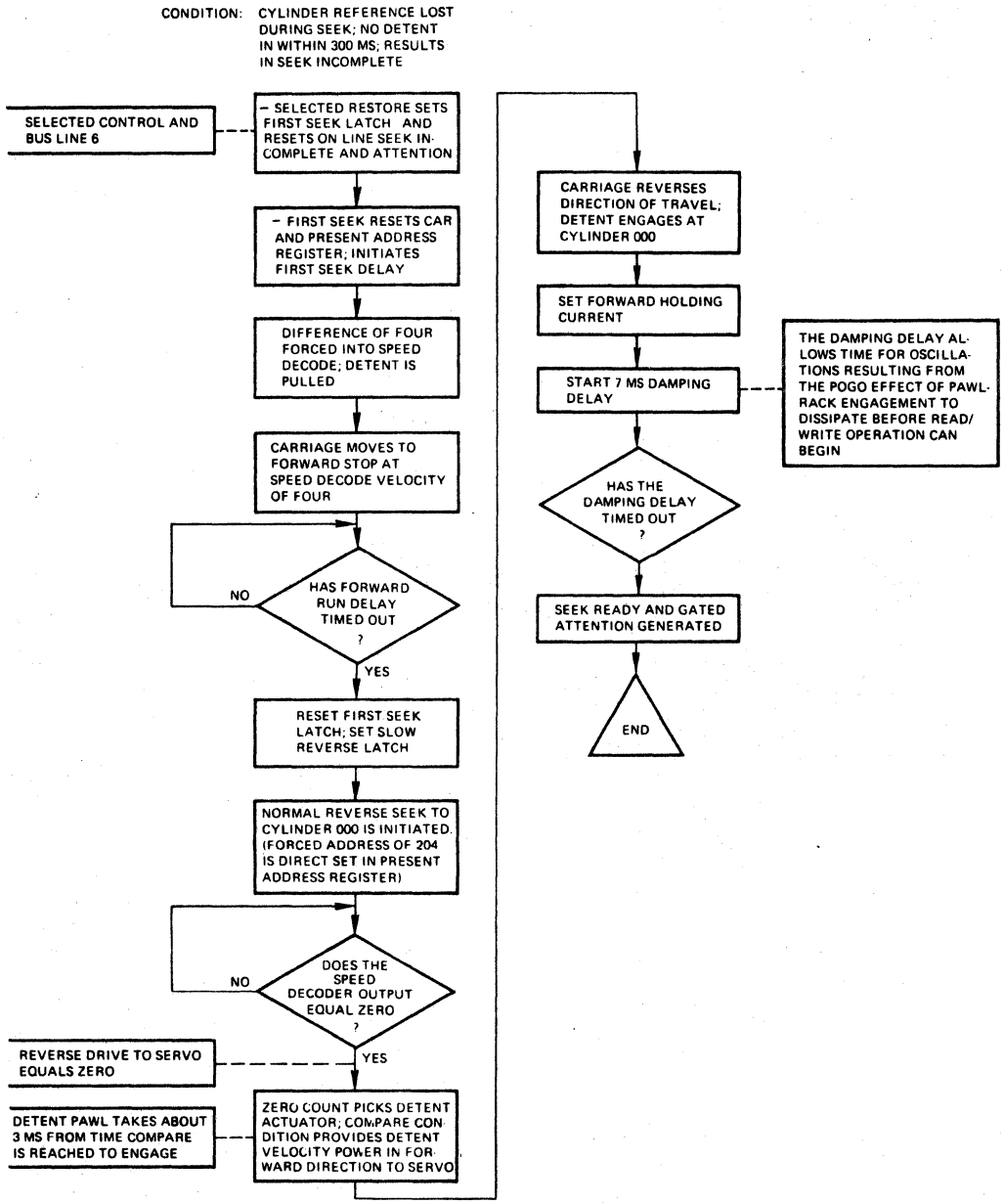


Programmed Seek (Sheet 2 of 3)

Figure 3-3

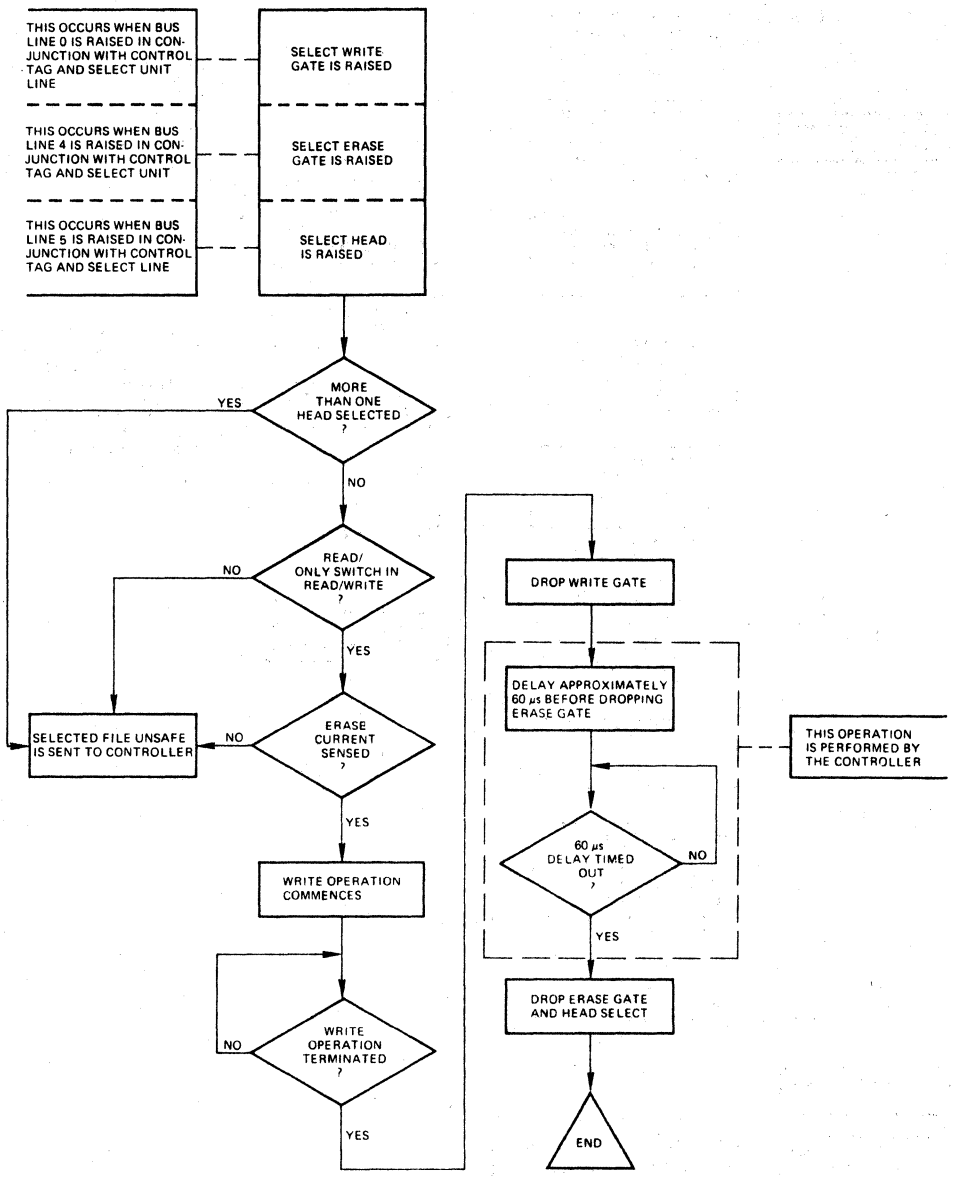


Programmed Seek (Sheet 3 of 3)
Figure 3-3



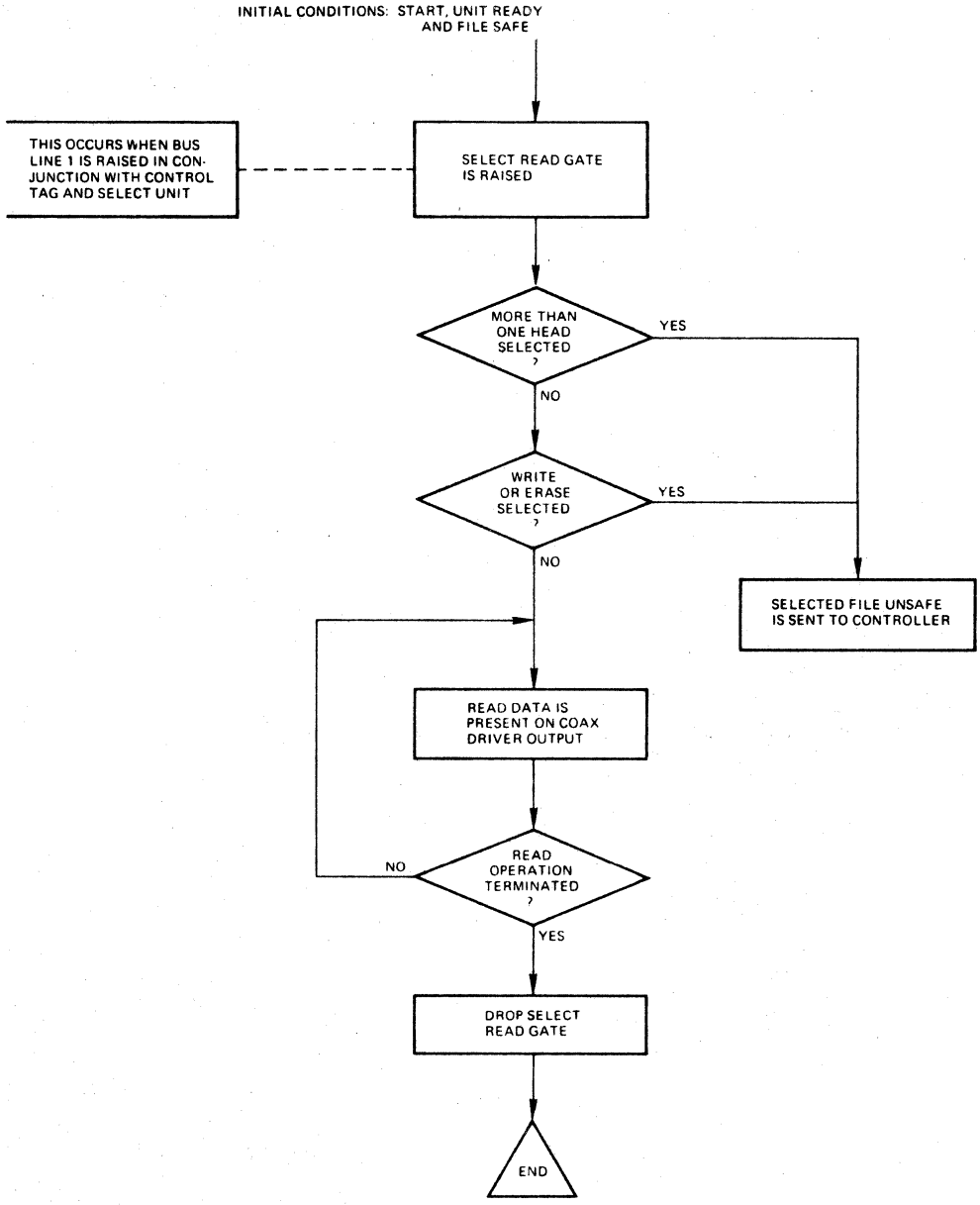
Restore Retract

Figure 3-4



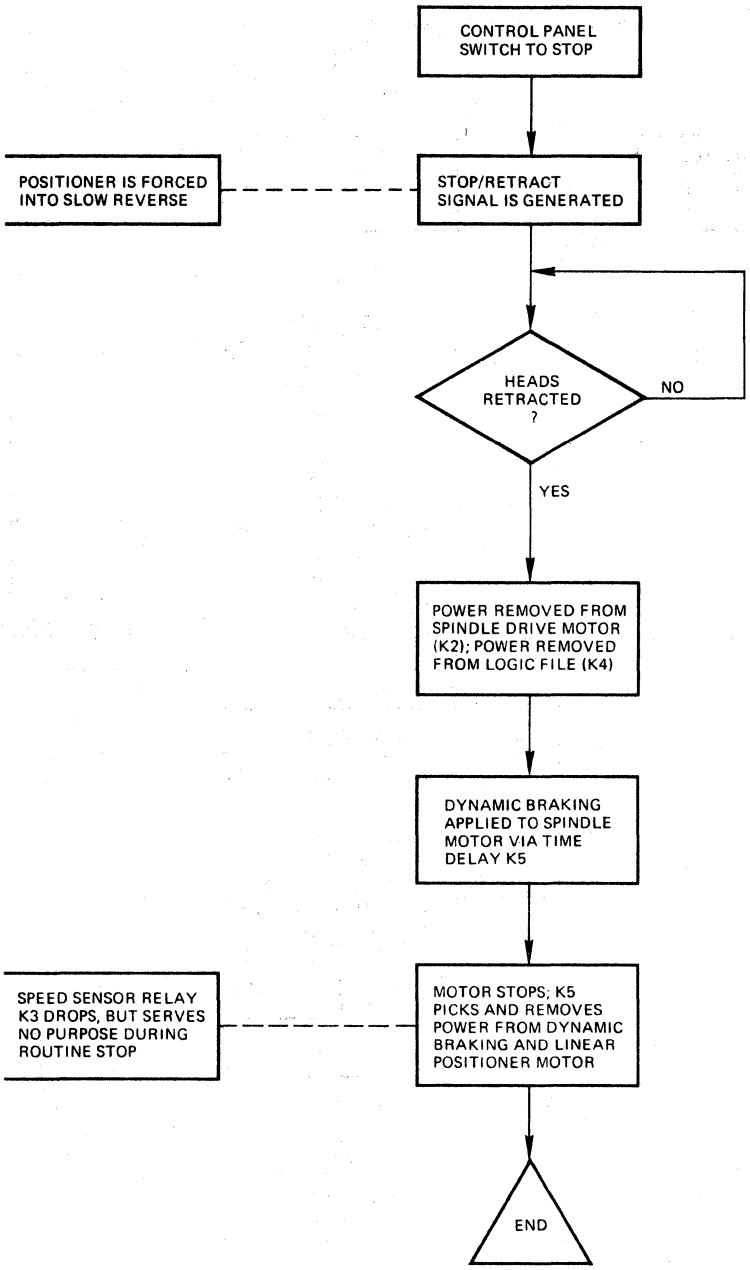
Write Operation

Figure 3-5



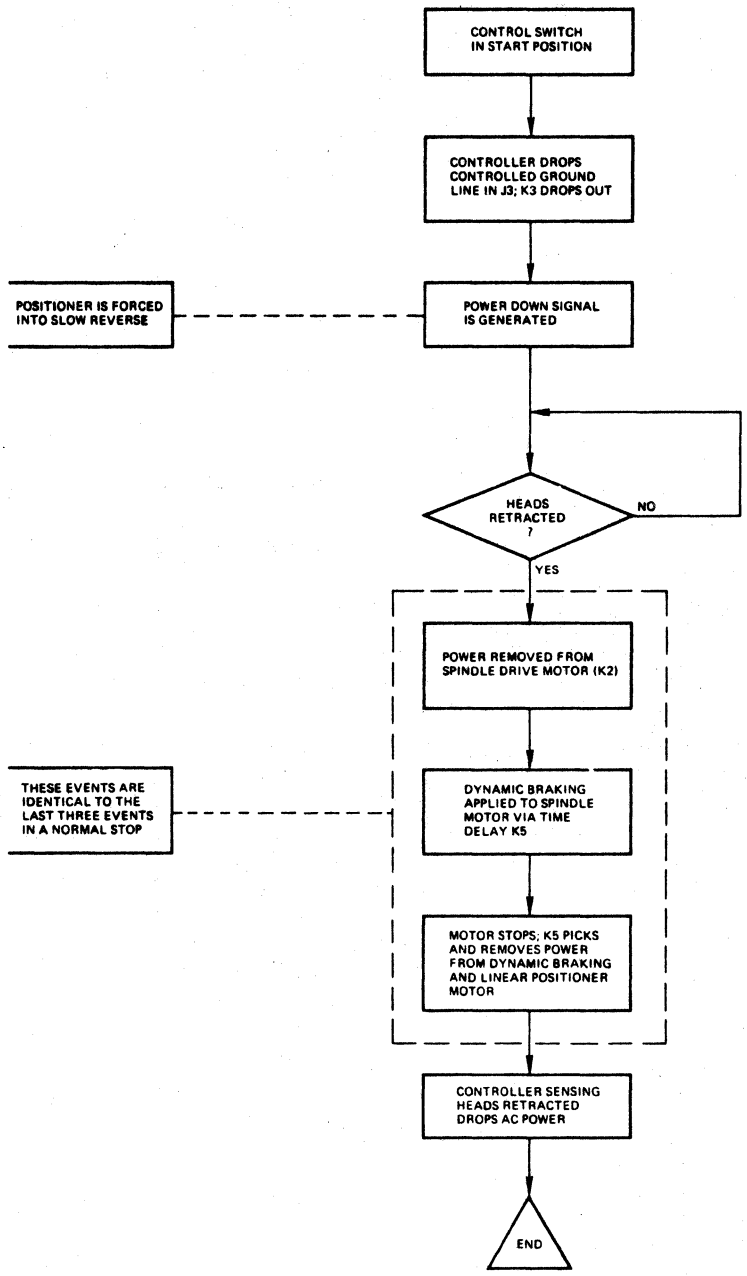
Read Operation

Figure 3-6



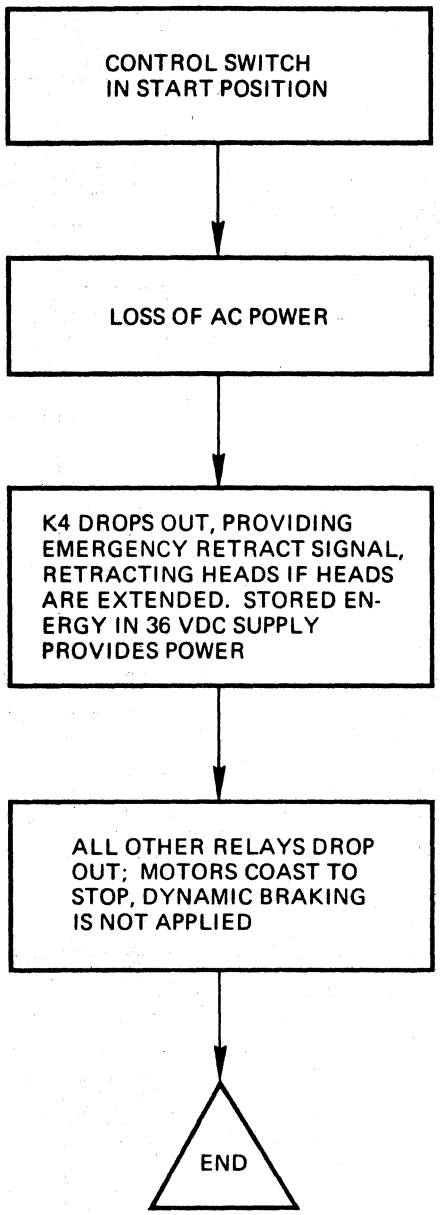
Normal Stop

Figure 3-7



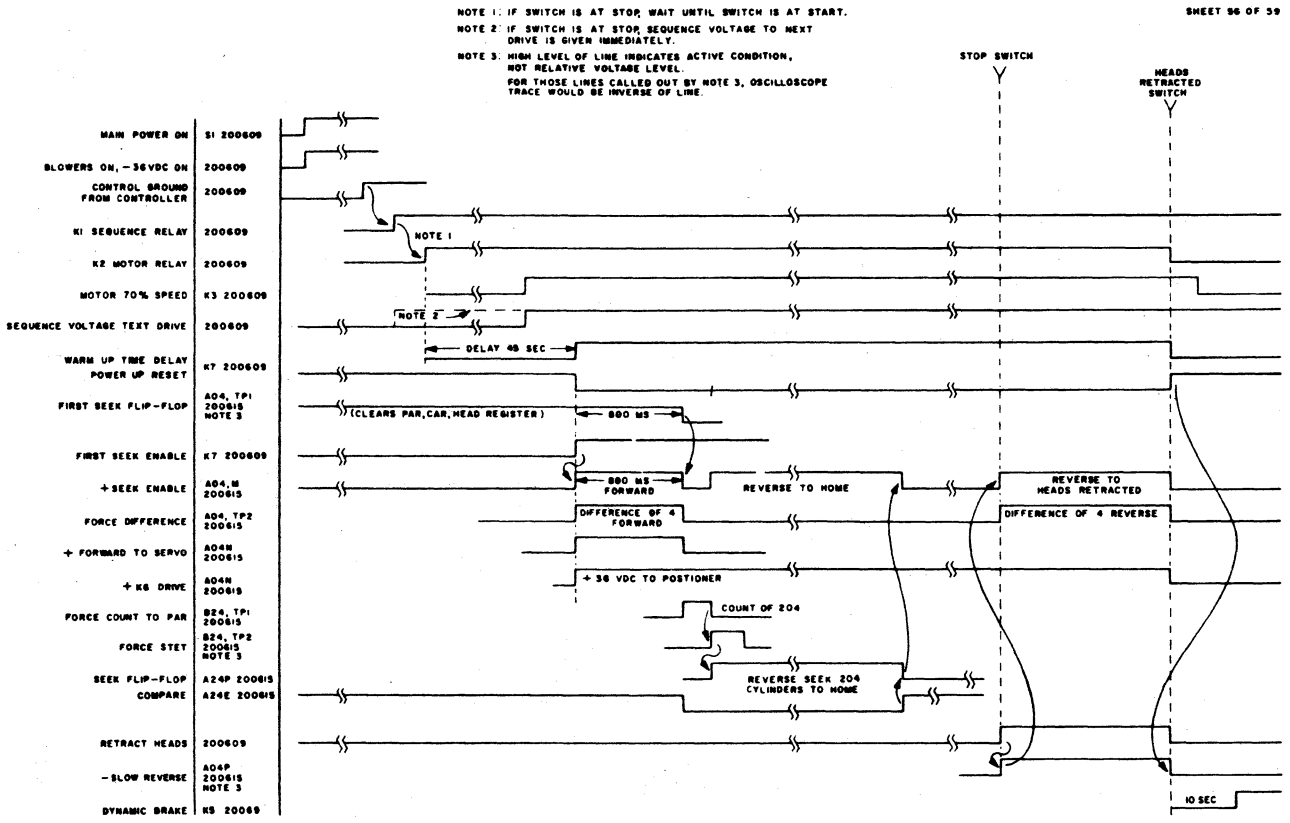
Controlled Power Down

Figure 3-8



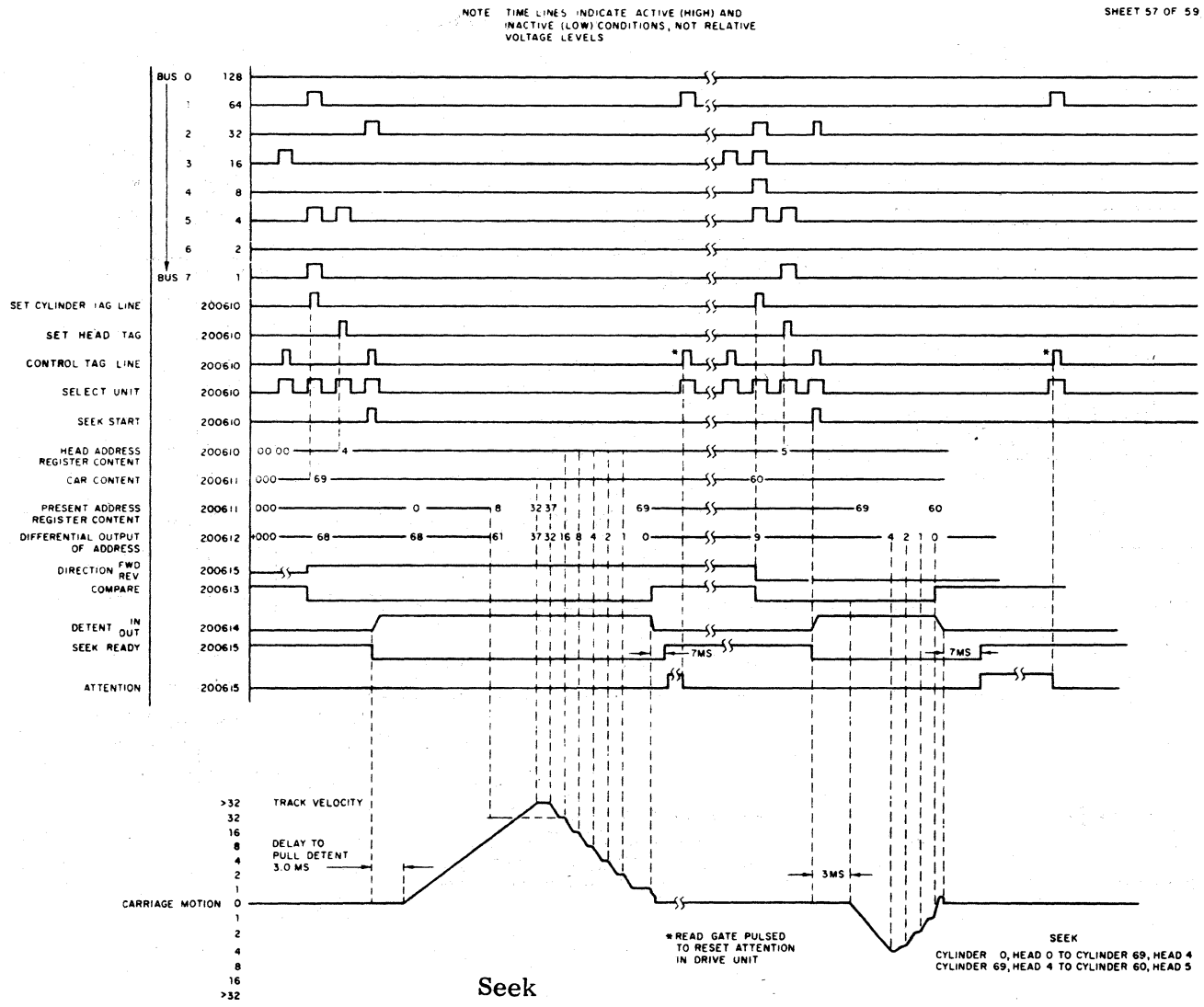
Abnormal Stop

Figure 3-9



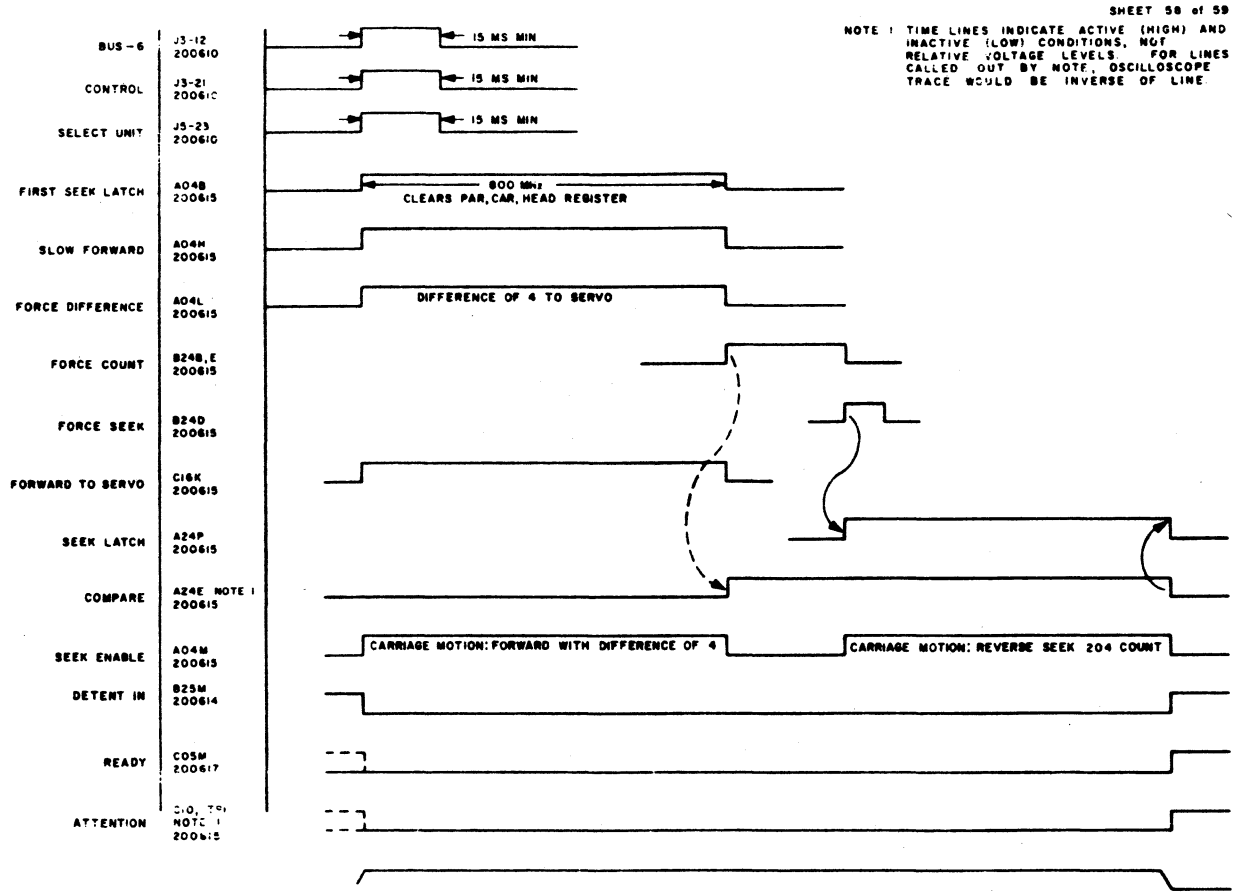
Power Sequence

Figure 3-10



Seek

Figure 3-11



Restore/Recalibrate

Figure 3-12

SECTION 4.0

ADJUSTMENT PROCEDURES

4.1 SERVO ADJUSTMENTS

4.1.1 General

The three printed circuit boards which make up the servo system are listed below:

Board Name	Assembly No.	Location
Fwd/Rev Speed Decode	001476 (schematic 001477)	A/B15
Tach Amplifier	001436 (schematic 001437)	A22
Servo Amplifier	001426 (schematic 001427)	B23

Use a calibrated oscilloscope with two one-to-one attenuation probes.

4.1.2 Machine Preparation

If the drive is capable of performing a normal first seek, it is not necessary to pull the Forward/Reverse Speed Decode board A/B15; otherwise, remove A/B15 and set it away from the linear motor.

4.1.3 Oscilloscope Preparation

A. Set the amplitude scale to 50 mv/cm. Select ground and the chopped mode.

B. Connect one probe to TP2 on the Tachometer Amplifier board A22 and the other probe to TP3 on the same board.

C. Balance the traces and then switch from ground to dc.

4.1.4 Preliminary Servo Calibration

The adjustments described in this section are static preparations. While they do compensate for voltage deviations, final adjustments must be made during actual seek operations.

A. Adjust the top pot (zero pot) on A22 so that the output from TP2 is 50 mv more negative than the TP3 trace.

NOTE

It is possible to cause the opposite result so note carefully which trace goes relatively more negative.

This adjustment assures that when carriage velocity, as decoded by the tachometer amplifier, falls below 50 mv, a zero velocity output is generated.

B. Move the probes to TP2 and TP4, both on the Servo Amplifier Board B23.

C. Change the vertical scale on the oscilloscope to 1 v/cm and switch back to ground. Adjust the two traces until they are balanced; then switch to dc.

D. Adjust the center pot (servo balance pot) on A22 until the two traces are balanced.

E. Adjust the top pot (dc level pot) on B23 so that the output is -2 volts.

NOTE

If step E. unbalances the traces, readjust the center pot on A22. It is necessary that both conditions (balanced traces and -2 volt output) be met.

F. Return A/B15 to its slot in the logic file.

4.1.5 Final Servo Calibration

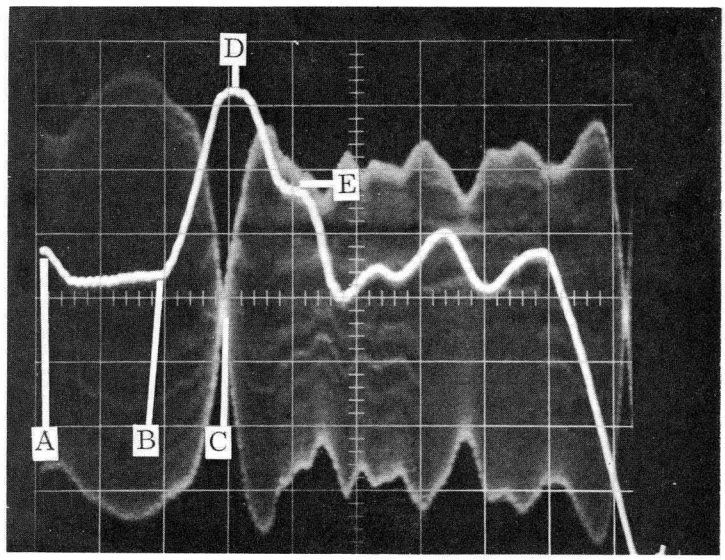
A. Connect one scope probe to TP2 on A22 and the other probe to TP1 on the Transducer Comparator board. Use A24-N (-Forward Up Count Enable) for the external sync.

B. Set the vertical scale to 100 mv/cm and the sweepspeed to 2 ms/cm. Select ground and balance the traces. Switch to ac.

C. Initiate alternate one track seeks between cylinder 000 and 001. The resulting trace should resemble the one shown in Figure 4-1.

D. Point A (sync point) represents the time -Forward Up Count Enable goes low. At point B, forward motion begins. From that time until the null is detected at point C should be about 2 ms. The amplitude of the output at point D should be about 300 mv.

E. Adjust the bottom pot (gain pot) on B23 until the amplitude of the step at point E is 150 mv. This adjustment establishes proper detenting velocity.

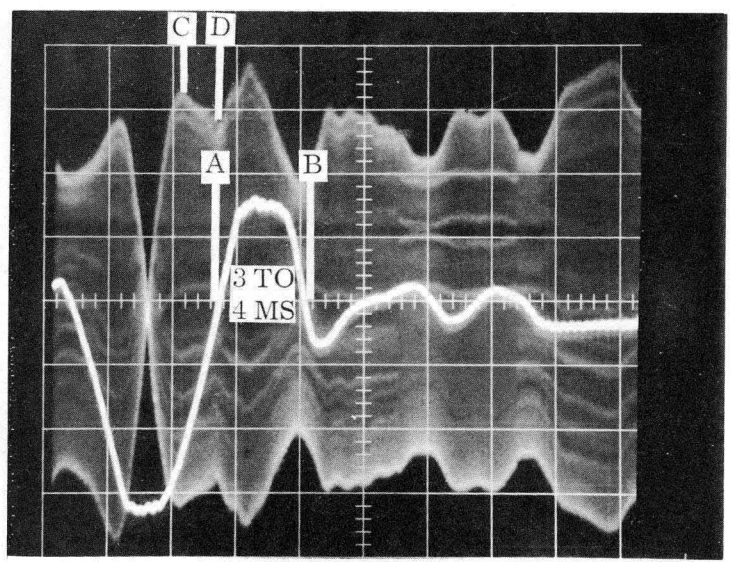


Alternate One Track Seek (Forward Trace)

Figure 4-1

F. Change the sync to A24-L (-Reverse Down Count Enable).

G. Initiate alternate one track seeks between cylinders 000 and 001. The resulting trace should resemble the one shown in Figure 4-2.



Alternate One Track Seeks (Reverse Trace)

Figure 4-2

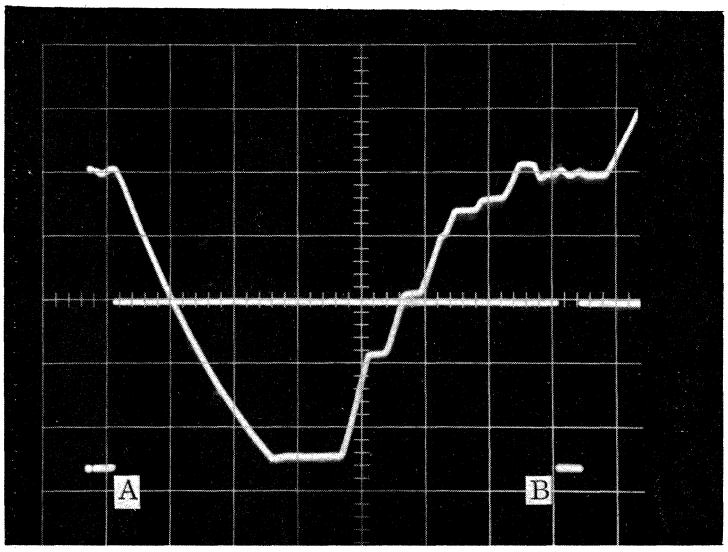
H. Adjust the single pot (reverse run pot) on A/B15 so that period from point A to point B is about 3 to 4 ms. This is not an absolute range. The ideal turnaround time on any particular drive may fall slightly oustide this range. However, generally speaking, a carriage which is allowed over 4 ms of turnaround time will occasionally detent one cylinder lower than its intended cylinder and a carriage which is allowed less than 3 ms will occasionally detent one cylinder higher than its intended cylinder.

NOTE

Another clue to proper adjustment of the reverse run pot is the point on the ghost trace identified as point D. This indentation should be about 10% lower than the peak identified as C. If the reverse turnaround time is too long, the indentation will pull in toward the base line. If the turnaround time is too short, the indentation will tend to fill out away from the base line.

I. Connect one probe to TP4 on C09, the Seek Gating board and the other to TP2 on A22. Change the sync to A24-L, -Reverse Down Count Enable. Set the vertical scale for the C09 trace (Seek Ready) at 2 v/cm and vertical seek for the A22 trace at 1 v/cm. Select 10 ms/cm for the sweepspeed.

J. Initiate alternate 200 track seeks between cylinders 000 and 200. The resulting trace should resemble the one shown in Figure 4-3.



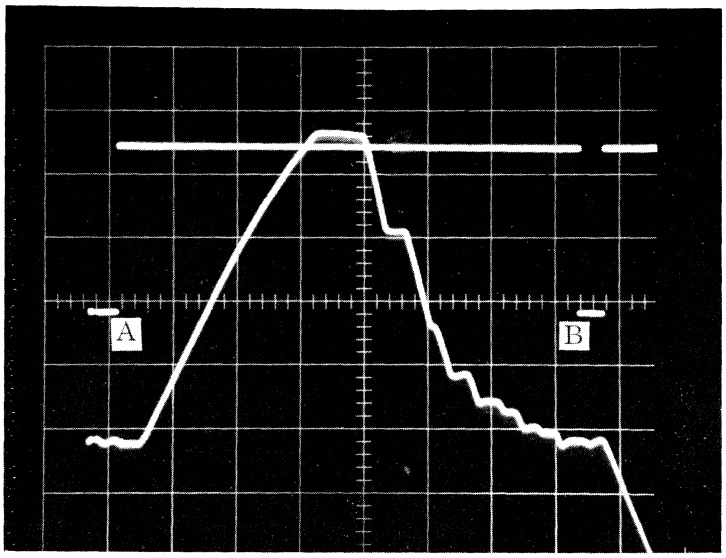
200 Track Seek (Reverse)

Figure 4-3

K. Adjust the bottom pot (velocity pot) on A22 so that the period from the time -Seek Ready goes high to the time it goes low again (point A to point B) is about 72 ms.

L. Connect one probe to TP4 on C09, the Seek Gating board, and the other to TP2 on A22. Change the sync to A24-N, -Forward Up Count Enable. Do not change the vertical scale or sweepspeed settings. Initiate alternate 200 track seeks between cylinders 000 and 200. The resulting trace should resemble the one in Figure 4-4.

M. The period from the time -Seek Ready goes high to the time it goes low again (point A to point B) should be about 74 to 76 ms.



200 Track Seek (Forward)

Figure 4-4

N. After all the steps through step M. have been performed, the entire procedure should be repeated. This is to ensure that no intermediate adjustment has altered an earlier calibration. At each appropriate point, compare the scope trace with the corresponding illustration.

4.2 VOLTAGE ADJUSTMENTS

For the following checks, use either a calibrated scope or a dc meter with at least 2% accuracy.

4.2.1 Minus 18 vdc

A. With the machine running and warmed up, check for -18 ±0.5 vdc on the regulator card, slot C01 at TP2 (ground) and TP1 (hot).

B. If the voltage is outside limits, adjust the 5-K potentiometer (R10) as necessary.

4.2.2 Plus 18 vdc

A. With the machine running and warmed up, check for +18 ±0.5 vdc on the regulator card, slot C02 at TP1 (ground) and TP2 (hot).

B. If the voltage is outside limits, adjust the lower 5-K potentiometer (R10) as necessary.

4.2.3 Plus 5 vdc - Overvoltage Sense

A. The absolute value of the +5 vdc supply is not adjustable, but the setting of the overvoltage protection sensing point is. The actual +5 vdc supply has a tolerance of ±2%, and the overvoltage trip point is set about 0.5 volts above the existing normal value.

B. If it is necessary to adjust the sensing point, check at pin A of C02 for +5 vdc; confirm that it is within the tolerances listed above. Adjust the upper 5-K potentiometer (R13) clockwise until the voltage at pin A suddenly goes to zero. Then turn the main power switch off.

C. Adjust R13 counterclockwise two turns. Select START on the START-STOP switch and allow the machine to warm up (approximately 45 seconds). Check to see if the +5 vdc returns to its original value. The overvoltage sensing point is thus set to about 0.5 volts above the existing 5-vdc level.

4.3 OFF-LINE HEAD REPLACEMENT AND ALIGNMENT

4.3.1 Equipment

Head replacement and alignment while the drive is off line requires:

A. PSC portable off-line tester (PSC P/N 200557)

B. Head alignment plug (PSC P/N 200517)

C. Head alignment tool (PSC P/N 200515)

D. CE disc pack (yellow shield, IBM P/N 2200018)

E. Calibrated scope with two one-to-one attenuation probes:

4.3.2 Head-Arm Assembly Replacement

When replacing a head-arm assembly, be sure the drive meets these conditions: (1) DISABLE is selected with the ENABLE-DISABLE* switch, (2) both top covers are removed and (3) the shroud is removed.

A. While holding the detent out by hand, carefully move the carriage forward as far as possible (about 3/8-inch) without loading the ramps off the unload pins. Engage the detent.

B. Disconnect the head plug from its board (select/read preamplifier or select/write amplifier and coax receiver).

C. Remove the two side clamps which hold the assembly in the T-bar slot (one above and one below the head arm). See Figure 4-5.

D. Take the T-bar end of the head-arm assembly between the thumb and a finger of one hand. Use a finger or thumb to act as a brace behind the bend of the leaf spring (see Figure 4-6, point A).

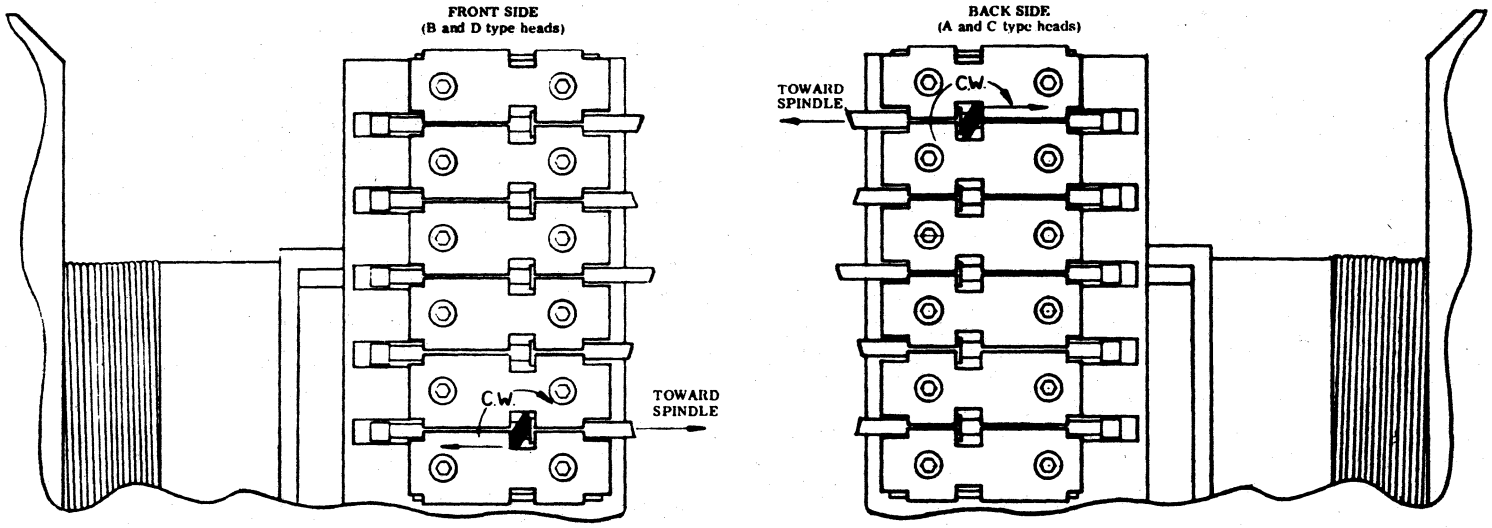
E. Take a corner of the leaf spring at the head shoe end between the thumb and finger of the other hand.

CAUTION

Do not touch the head shoe face or press against the flexure. Refer to Figure 4-6, points B and C . Even slight pressure against the flexure could bend it and impair the head's flying attitude.

Bend the leaf spring back just enough to clear the cam supporting it. Excessive bending may exceed the yield point of the leaf spring.

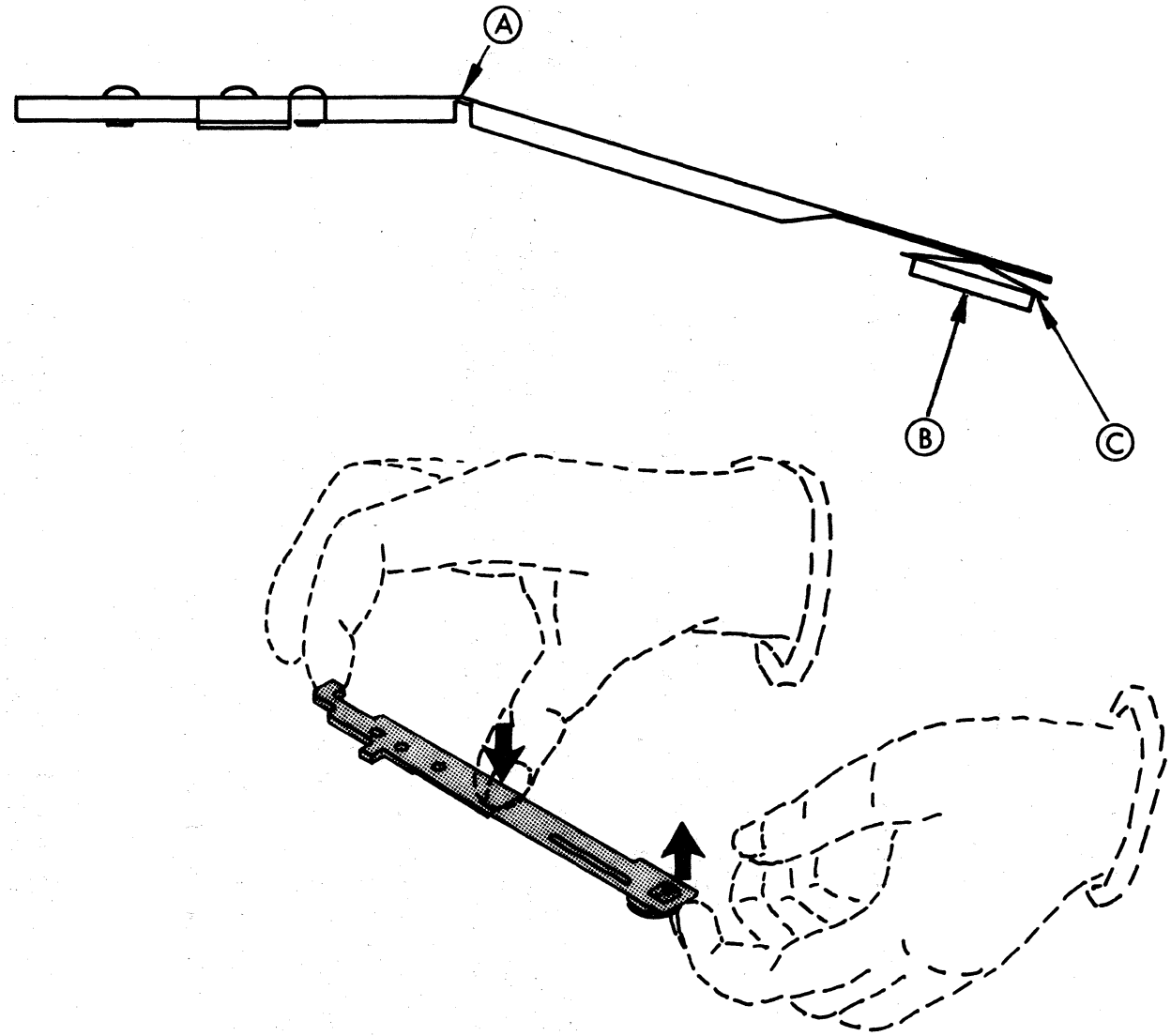
* The drive should not be disabled at this point if an off-line tester will not be used. See Section 4.3.3.2.



A B

Head-Arm Mounting Clips and Alignment Slots

Figure 4-5



Handling the Head-Arm Assembly

Figure 4-6

F. While holding the assembly clear of the cam with one hand, work the other end free of the T-bar slot. Keep the leaf spring straight until the head shoe is completely clear of the other head-arm assemblies.

CAUTION

Maintain a secure hold on both ends of the assembly. As soon as the arm is out of the T-bar slot and off the cam, the leaf spring will suddenly attempt to unflex. If this is allowed to happen, the head shoe will slap against another head-arm assembly.

G. To install a head-arm assembly, reverse steps A through F.

NOTE

The head must be mounted so that the bleed holes relative to disc pack rotation are located in the leading half of the head shoe. The disc pack rotates counterclockwise.

Whenever a read/write head is replaced, an alignment check must be made on it and the two adjacent heads (one adjacent head if the replaced head is at the top or bottom of the T-bar). This is advisable because the adjacent head-arm assemblies may move slightly when the clips they share with the replaced head are removed.

4.3.3 Head Alignment Check

4.3.3.1 Preliminary Steps

The following preparations must be made before head alignment can be analyzed.

A. See that the shroud is in place.

B. Install a CE disc pack (yellow shield; IBM P/N 2200018).

CAUTION

Be certain the carriage and heads are fully retracted before installing or removing a disc pack.

C. Preparation of Off-Line Tester

To substitute a PSC off-line tester for the controller, perform the following steps (ignore step C and move to step D if an off-line tester is not available).

1. Select DISABLE with the ENABLE-DISABLE switch on the Model 630 operator control panel. This puts the drive off line.
2. Check to be certain all switches on the off-line tester are in the OFF position.
3. Remove paddle boards C26, C27 and C28 from the card file. This prevents communication with the controller on the signal in, signal out and dc lines.
4. Insert the appropriate off-line tester paddle boards into card file locations C26, C27 and C28.

D. Head and Pack Thermal Equilibrium

The temperature stabilization cycle, which assures standard operating temperature during head alignment, consists of two phases:

1. Run the drive, with a CE pack installed and all covers on for 1 hour and 15 minutes.
2. Run the drive, with a CE pack installed and the two top covers off, for 20 minutes.

E. Scope Connection

Use a scope with direct probes (1:1 attenuation). Set its display to A+B so the two test points are read differentially. Set the vertical scale at 5 mv/cm and the sweeprate to 3 ms/cm (or enough to observe one revolution).

Connect one probe to TP-1 on the read amplifier card (located in A/B16). Connect the other probe to TP-2 on the same card. The scope should be in an external sync mode with the sync point on -index (located at TP-6 on card A23 in the logic file).

F. Remove the transducer oscillator board from slot B26.

Once these preparations have been completed, the off-line head alignment check can be performed.

4.3.3.2 Head Alignment Check

Perform steps A through H if an off-line tester is being used and bypass step I. If an off-line tester is not available, substitute step I for A through H.

A. Position the heads to cylinder 73 with the off-line tester.

1. Rotate the SELECT OPERATION dial to ALTERNATE CYLINDER.
2. Throw toggle switches 1, 8 and 64 to ON and throw the LOAD ADDRESS toggle (momentary switch). This loads the binary equivalent of 73 into the cylinder address register.

3. Throw the SINGLE CYCLE momentary switch. This positions the heads to cylinder 73.

4. Return all off-line tester switches to OFF.

CAUTION

Before going further, be certain that the head about to be checked is deselected. If the next step is performed while the head is selected, the track will be erased.

B. Disconnect the head plug from its board (select/read preamplifier or select/write amplifier and coax receiver).

C. Insert the head plug into a head alignment plug; insert the head alignment plug into the socket from which the head plug has just been removed.

D. Throw the RESET HEAD switch and SINGLE CYCLE momentary switch. Return the RESET HEAD switch to OFF.

E. Select the head by throwing the appropriate toggle switches and the SET HEAD momentary switch to ON. Sum of switch values equals the head number; e.g., head 3 is selected by switches 1 and 2. This loads the numbers (e.g., 1 and 2) into the head register. Return switches to OFF. The WRITE and READ switches (128 and 64) must be OFF.

NOTE

To select head 0, throw the RESET HEAD switch and single cycle momentary switch; this fills the head register with zeros.

F. Throw toggle switch 4 to ON. This brings up the enabling line called head select. Return switch 4 to OFF.

G. Rotate the SELECT OPERATION dial to READ.

H. Throw toggle switch 64 to ON. This enables the selected head to read. The read operation causes a signal to appear on the scope. When the head is aligned, the trace will resemble the curve in Figure 4-7.

I. The following steps must be performed if an off-line tester is not available.

1. Position the heads to cylinder 73 via the controller.

2. Select DISABLE with the ENABLE-DISABLE switch.

CAUTION

Before going further, be certain that the head about to be checked is deselected. If the next step is performed while the head is selected, the track will be erased.

3. Disconnect the head plug from its board (select/read preamplifier or select/write amplifier and coax receiver).

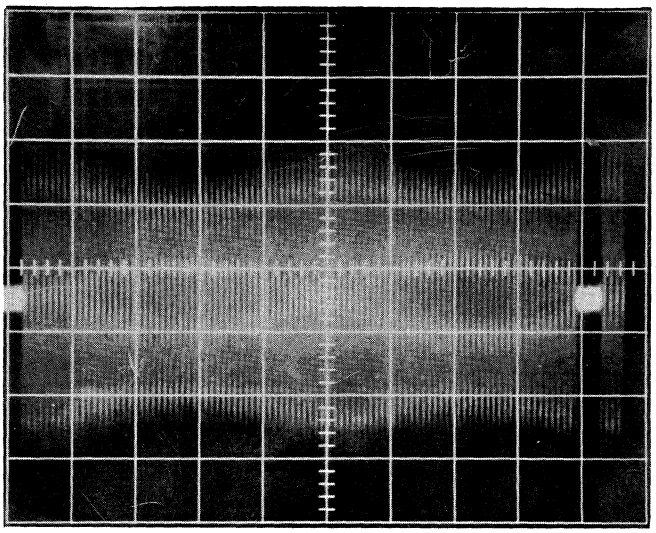
4. Insert the head plug into a head alignment plug; insert the head alignment plug into the socket from which the head plug has just been removed.

5. Select the head by jumpering it to ground.

NOTE

If other heads in the same bank are to be aligned, their head plugs can be inserted in the alignment plug in its present location. This makes it unnecessary to move the alignment plug and jumper lead from socket to socket.

6. A read signal should appear on the scope. When the head is aligned, the trace will resemble the curve in Figure 4-7.



Vertical: 5 mv/div

Sweep Rate: 2 ms/div

Head Alignment Read Signal at One Revolution

Figure 4-7

4.3.4 Head Alignment

The following alignment procedure assumes that the conditions necessary for performing a head alingment check (described in Section 4.3.3.1) are satisfied. In addition, check to be certain that the DISABLE switch on the Model 630 is depressed, all switches on the off-line tester are OFF and the three off-line tester paddle boards are plugged into slots C26, C27 and C28 in the logic file. Finally, position the heads to cylinder 73 of the CE disc pack if they are not already there.

CAUTION

Before going further, be certain the head about to be aligned is deselected. If the next step is performed while the head is selected, the track will be erased.

A. Remove the head plug of the head to be aligned from its socket in the select/read preamplifier or select/write amplifier and coax receiver card.

NOTE

- If all the heads on the front side of the T-bar (B and D type heads) are to be aligned, start with the bottom assembly and work up.
- If all the heads on the back side of the T-bar (A and C type heads) are to be aligned, start with the top assembly and work down.

B. Insert the head plug into the head alignment plug and insert the head alignment plug into the socket from which the head plug was just removed.

C. Throw the RESET HEAD switch and SINGLE CYCLE momentary switch. Return the RESET HEAD switch to OFF.

D. Select the head with the off-line tester by throwing the appropriate toggle switches and SET HEAD momentary switch to ON (the sum of the switch values equals the head number; e.g., to select head 3, throw switches 1 and 2). This sets the head number in the head register. Return the switches to OFF. The WRITE and READ switches (128 and 64) must be OFF.

NOTE

To select head 0, throw the RESET HEAD switch and SINGLE CYCLE momentary switch; this fills the head register with zeros. Return the RESET HEAD switch to OFF.

E. Throw toggle switch 4 to ON. This raises the enabling line called head select. Return switch 4 to OFF.

F. Rotate the SELECT OPERATION dial to READ.

G. Throw toggle switch 64 to ON. This enables the head to read. The read operation causes a signal to appear on the scope. When the head is aligned, the scope trace will resemble the curve in Figure 4-7.

H. Loosen the four screws of the two clamps which hold the head-arm assembly in place just enough to allow the assembly to move when forced with a moderate pressure.

I. Push lightly against the tab on the head-arm assembly with a head alignment tool so that the assembly moves all the way back in its slot against the T-bar.

J. Tighten one of the clips (bottom clip for a B or D type head; top clip for an A or C type head) with a torque wrench set at 6-8 inch-pounds. Refer to Figure 4-5.

NOTE

The alignment tool should always push back against the clip that is tightened down. Since the tool twists clockwise, the bottom clip must be tightened on the front side of the T-bar and the top clip on the back side.

K. While observing the trace on the scope, carefully twist the alignment tool clockwise so the assembly moves forward (toward the spindle). Stop twisting as soon as a trace resembling the curve in Figure 4-7 appears on the scope.

L. If the head goes too far forward, return to step I.

NOTE

Do not try to align the head while pushing the assembly back. Always align the head while adjusting it in the forward direction.

M. Before tightening the other clip, check the alignment of the adjacent head(s). To do this, it will be necessary to deselect the head just aligned and select an adjacent head.

1. See that all switches on the tester are OFF.

CAUTION

Before going further, be certain the head just aligned and the head about to be checked are both deselected.

2. Remove the head alignment plug from its present head plug and install it on the head plug about to be checked. Return the head plug of the head just aligned to its socket and insert the head alignment plug in its socket.

3. Throw the RESET HEAD switch and SINGLE CYCLE momentary switch. Return the RESET HEAD switch to OFF.

4. Select the head by throwing the appropriate toggle switches and the SET HEAD momentary switch to ON. Return switches to OFF.

5. Observe the scope trace and align the head if necessary, using the technique described in steps A through K.

N. When the adjacent heads are aligned, check to be certain all clips are tight.

4.4 INDEX TRANSDUCER BLOCK ALIGNMENT

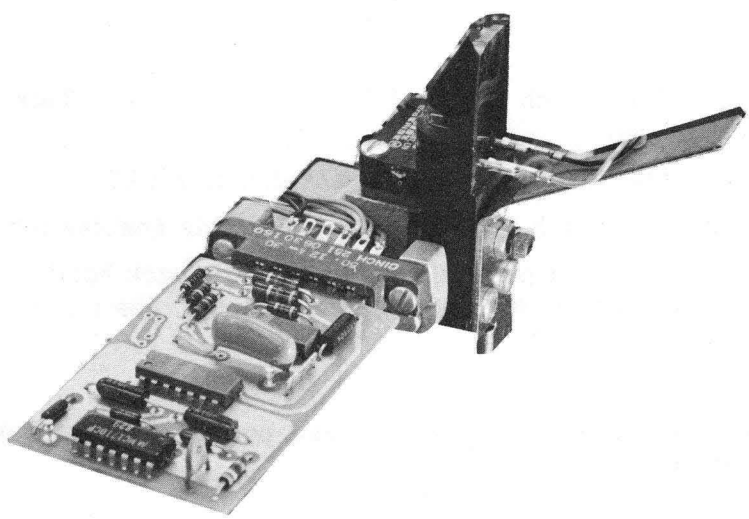
Accuracy of carriage tracking and alignment of the index transducer block are checked using the burst track located at cylinder 003 of the CE disc pack (yellow shield; IBM P/N 2200018). The following alignment check and adjustment procedures assume that the preparations described in Section 4.3.3 have been completed.

4.4.1 Transducer Output Amplitude

Amplitude of the index transducer output should be 0 between slots and 400 mv at the slots. Refer back to Figure 2-21 for an illustration of index transducer output. If the trace observed on the scope does not meet these amplitude requirements, the following adjustment should be made.

A. Slowly turn the adjustment nut located on the back of the transducer block (see Figure 4-8) counterclockwise until the trace on the scope meets the 0 to 400 mv standards. If this does not happen after one full turn, go on to step B.

B. Slowly turn the adjustment nut clockwise until the trace is satisfactory. Be prepared to reverse direction with the wrench. Clockwise adjustment moves the transducer toward the disc and the disc may begin to rub against the back face of the channel in the index transducer. If this happens, back the nut off 3/4 of a full turn. This will set the transducer for optimum output.



Index Transducer

Figure 4-8

4.4.2 Index Transducer Block Alignment Check

A. Position the heads to cylinder 003. *

1. Rotate the SELECT OPERATION dial to ALTERNATE CYLINDER.
2. Throw toggle switches 1 and 2 to ON and throw the LOAD ADDRESS momentary switch. This loads the binary equivalent of 003 into the cylinder address register.
3. Throw the SINGLE CYCLE toggle switch. This positions the heads to cylinder 003.
4. Return all switches to OFF.

CAUTION

Before going further, be certain that all heads are deselected. Bit switch 8, SELECT HEAD must be down (OFF).

B. Throw the RESET HEAD switch and SINGLE CYCLE momentary switch. This loads the head register with zeros. Return the RESET HEAD switch to OFF.

C. Select a head by throwing the appropriate bit switches and the SET HEAD momentary switch to ON (head 0 was selected by step B). The sum of the bit switch values equals the head number. This operation loads the number into the head register.

NOTE

Bit switches 16, 32, 64 and 128 must be OFF during head selection.

D. Throw bit switch 4 (SELECT HEAD) to ON. This enables the head select line.

E. Rotate the SELECT OPERATION dial to READ.

F. Throw bit switch 64 (READ) to ON. This enables the selected head to read.

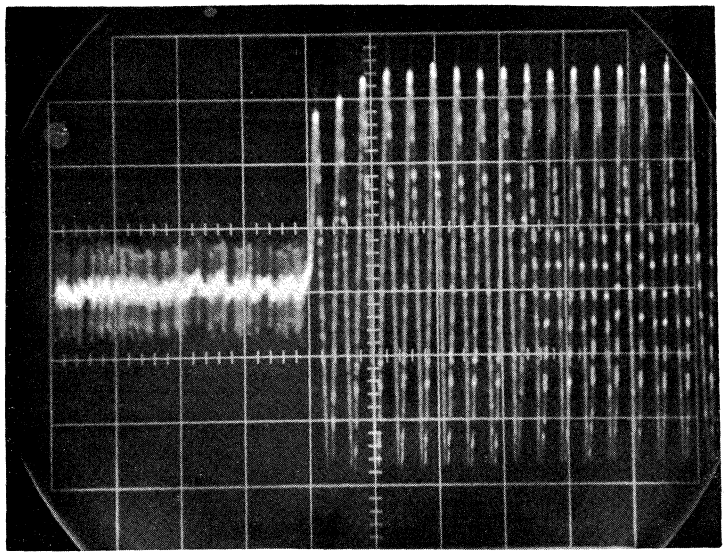
G. Check the burst pulse timing as read by each head. If all heads seem to be off by approximately the same amount, the index transducer block must be adjusted.

---

* Refer to Section 4.3.3.2, Step I for head positioning and selection without an off-line tester.

4.4.3 Index Transducer Block Adjustment

While observing the burst track display on the scope, tighten the adjustment nut slightly (see Figure 4-8). If tightening the nut causes the read pulses to appear closer to the 20 $\pm$ 4 μs range after index, continue tightening until they fall within that range. If not, loosen the nut until the read pulses occur after the optimum interval. See Figure 4-9.



Vertical: 50 mv/div

Sweep Rate: 5 μs/div

Index Transducer Alignment Output

Figure 4-9

4.5 CYLINDER TRANSDUCER

4.5.1 Drive Preparation

The cylinder transducer installation and adjustment procedures require the following:

A. Both top covers and the shroud removed from the Model 630.

B. Turn power off at main power switch, S1.

C. Remove 36V from servo drive, sixth wire from left (red) on the terminal board of the servo amplifier plate (as shown in Figure 4-10).

D. Unplug the spindle drive motor to prevent continuous dynamic braking, which would result in overheating.

E. Remove the Actuator Logic Driver board, A26, from the logic file. This allows manual operation of the detent pawls.

F. Close the main power switch S1 (on).

G. Select STOP on the START-STOP switch.

4.5.2 Transducer Installation

A. Insert the leaf spring in the round hole in carriage way (A in Figure 4-11).

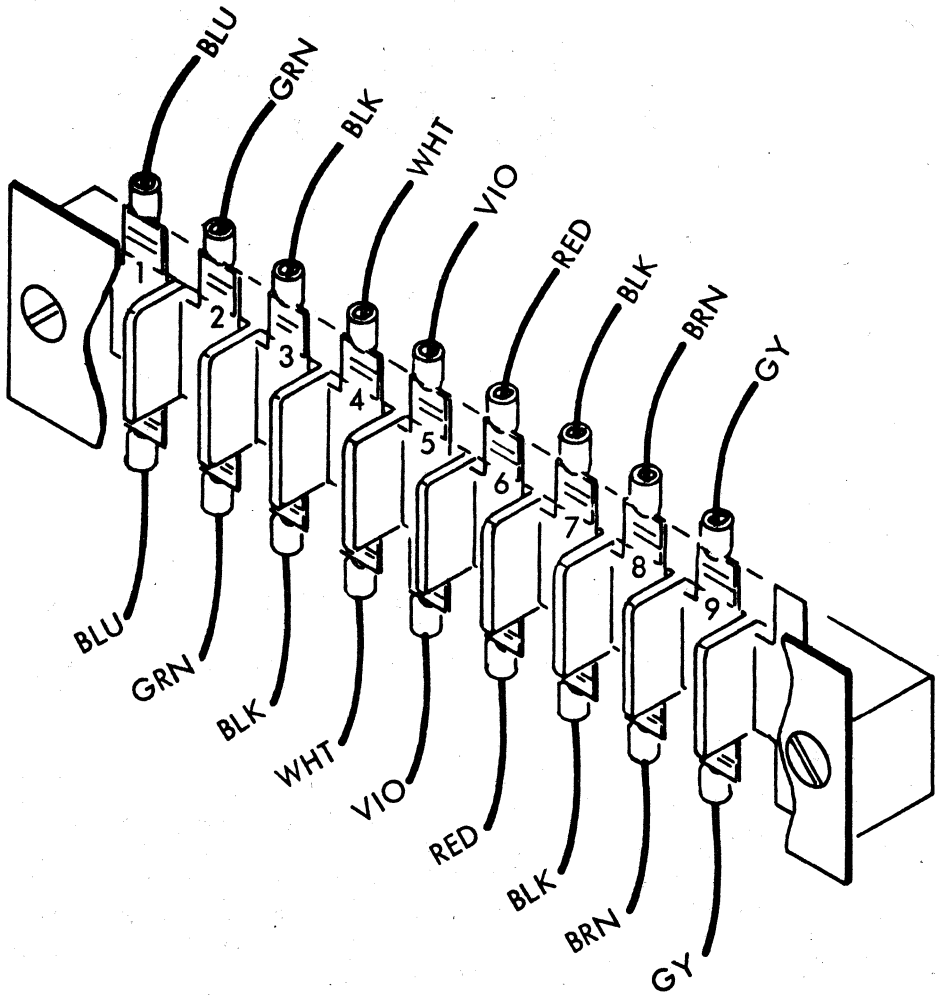
B. Place transducer on way so that the back of base is up against the leaf spring and the right side of the base rests against the locating pin (B in Figure 4-11).

C. Turn the pivoting screw counterclockwise to draw it back away from the transducer base (C in Figure 4-11).

D. Push draw-back screw through the hole in its post and start its thread in the threaded hole in the back of the transducer base (D in Figure 4-11). Turning this screw clockwise will pull it into the transducer base until the washer reaches the post. After that, more turning will pull the transducer back away from the rack.

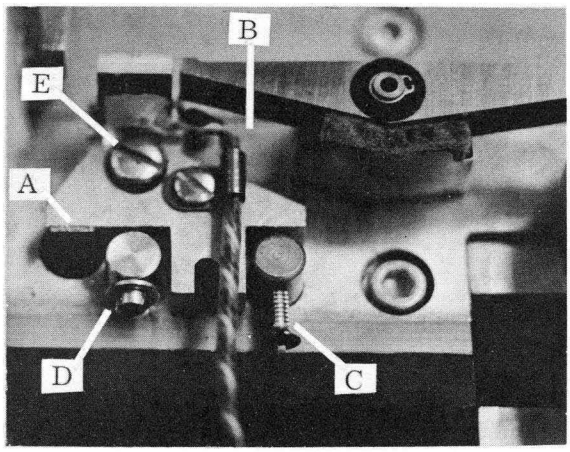
E. Screw in hold-down screw until it is snug (E in Figure 4-11).

F. Turn the draw-back screw (D) clockwise while moving the carriage forward. Draw the transducer back just enough to allow the carriage to slide past the transducer.



Servo Amplifier Terminal Board

Figure 4-10



Cylinder Transducer

Figure 4-11

4.5.3 Prepare Oscilloscope

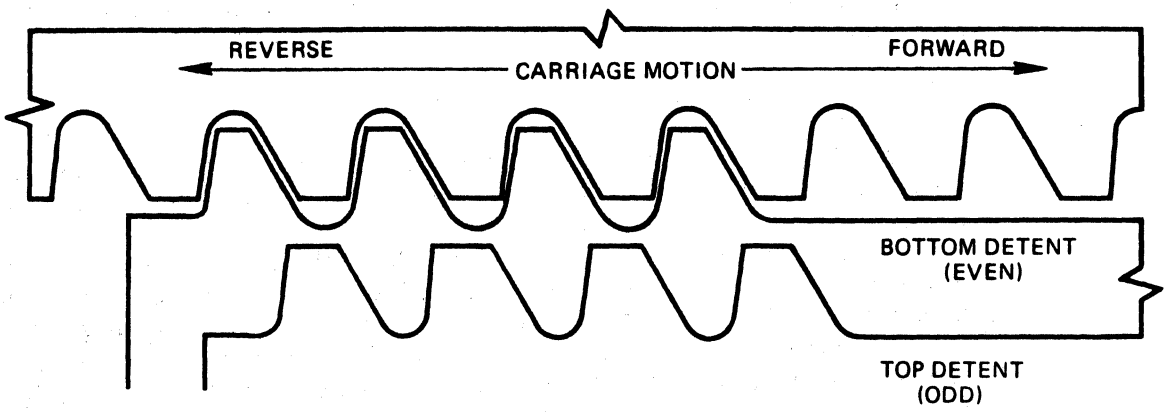
A. Set the amplitude scale at 100 mv/cm and the sweep speed at 5 ms/cm.

B. Connect the scope probe to TP1 on the Transducer Comparator board.

4.5.4 Preliminary Alignment

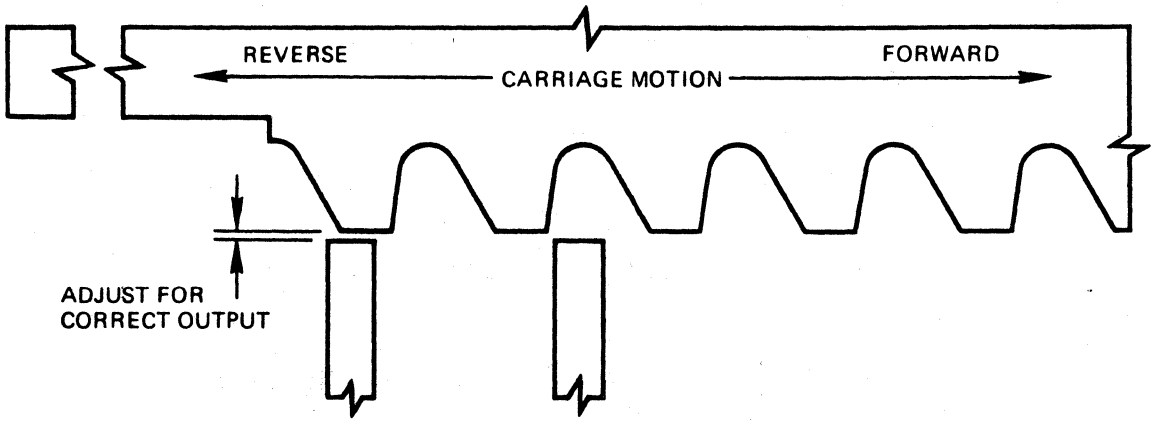
A. Move the carriage by hand to the home position (cylinder 000). Although the scale on top of the T-bar identifies home position, its accuracy should be checked by examining the position of the detent pawls with respect to the rack (refer to Figure 4-12). When the carriage is in the home position, the bottom pawl is engaged and there are two rack teeth in back of the top pawl.

B. Move the carriage to cylinder 200 as identified by the scale. From 200, the carriage can be moved to cylinder 202 by steps. Since the bottom pawl is engaged at 200, disengaging the bottom pawl while keeping a slight forward pressure against the carriage will cause the top pawl to engage at 201. Next, disengage the top pawl and allow the bottom pawl to engage at cylinder 202.



Rack and Pawls at Cylinder 000

Figure 4-12



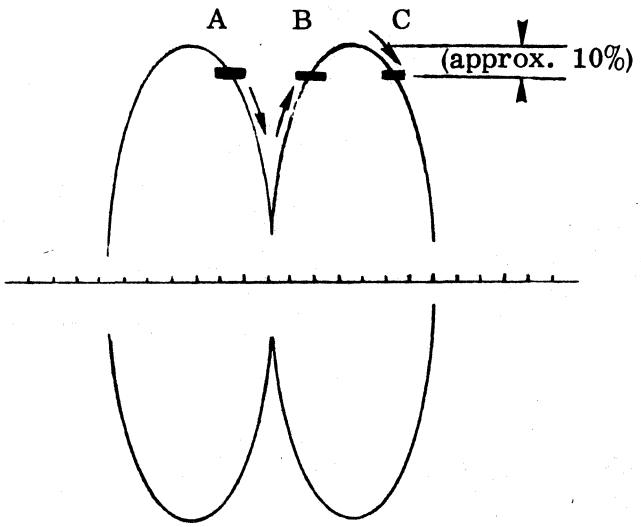
Rack and Cylinder Transducer at Cylinder 202

Figure 4-13

C. The left transducer coil (the slot closest to the linear motor) should be just to the left of the last rack tooth. If it is directly in front of it or to the right, the transducer must be pivoted counterclockwise. To do this, turn the pivot screw clockwise until the coil is in the proper position. See Figure 4-13.

4.5.5 Final Transducer Alignment

A. Observe the scope trace while turning the pivot screw clockwise (this operation pivots the transducer counterclockwise and causes the left transducer coil to line up with the last tooth on the rack). As the transducer begins to pivot, the amplitude of the trace will either begin to decrease or increase, depending on the initial position of the transducer coil with respect to the null. If it is at the position represented by A in Figure 4-14, it will decrease until it reaches the null and then begin to increase. If it is at the position represented by B, it will increase first. Shortly after the coil passes position B, the trace will reach its maximum amplitude and begin to decrease. As soon as the amplitude decreases about 10% stop turning the pivot screw. The coil will be in the position represented by C. As a final check, push lightly back against the carriage. The amplitude should increase slightly.



Reference Points for Final Transducer Alignment

Figure 4-14

B. Disengage the detent pawl and try to move the carriage. If there is resistance to movement, it means the transducer is too close to the rack. There are two methods for correcting this condition. Method 1 should be applied first. If it does not succeed, use method 2. If there is no resistance, go on to section 4.5.6.

1. With a beryllium screwdriver, push the front end of the carriage sideways across the carriage way. The best approach for this is to push against the side of the carriage with the screwdriver blade inserted under the detent pawls. This will open a gap between the rack and transducer. Slip a piece of sandpaper (#600 emery cloth) between the rack and transducer with the abrasive side toward the transducer. Leave enough sandpaper above the rack and transducer to hold with your fingers. Gently allow the carriage to move back into position. Bend the sandpaper back over the rack and crease it so that the rack becomes, in effect, a sanding block. Now roll the carriage back and forth several times, sanding the face of the transducer. After the first two or three passes, remove the sandpaper and check the carriage's freedom of movement. If the first sanding did not free the carriage, repeat the process one more time. If the second attempt does not succeed, go on to method 2.

2. Turn the pivot screw counterclockwise to relieve pressure on that end of the transducer base. Then turn the draw-back screw slowly clockwise. This will pull the transducer assembly back away from the rack. Be sure to bring it back only far enough to free the carriage. The larger the gap is between the transducer and rack the lower the amplitude will be of the transducer comparator output.

C. Move the carriage back to cylinder 202 and reexamine the position of the left transducer coil to be sure the transducer is still aligned.

4.5.6 Amplitude Adjustment

A. Check the amplitude of the trace when detented at cylinder 000. It should be at least 450 mv. It can be any value above that but should not be less than 450 mv. Simulate forward holding current during this check by pushing lightly against the T-bar.

B. Check the amplitude of the next few cylinder positions until you are satisfied that the worst-case amplitude is not less than 450 mv. It is probably not necessary to check amplitude at all cylinder positions since the lowest amplitudes typically appear at or near cylinder 000. However, it is best to test adjacent (odd and even) cylinder positions.

C. If amplitudes less than 450 mv are found at one or more cylinder positions, detent the carriage at the cylinder showing the lowest amplitude. With the blade of a beryllium screwdriver set against the back of the leaf spring, tap the handle of the screwdriver lightly until the amplitude goes above 450 mv. This technique is capable of increasing the amplitude by about 50 mv. If the deficiency is greater than that, turn the draw-back screw counterclockwise a quarter turn. If necessary, tap the leaf spring again. Check for clearance between the transducer and rack by pushing against the back of the transducer (where the coils are, not at the base). If there is clearance, comparator output amplitude will increase. If it stays the same or

decreases, the transducer is too close to the rack. In that case, the sandpaper should be used again. Push the carriage back slightly; the amplitude should increase about 10% indicating that the transducer is still properly aligned (as described in section 4.5.5 A). If the amplitude decreases or increases significantly more than 10%, repeat the procedure described in section 4.5.5 A.

D. Return to the other cylinder positions which showed insufficient amplitude and check the comparator output again as well as clearance between the transducer and rack.

E. As a final check, move the carriage back to cylinder 202. The left coil of the transducer should be centered on the last tooth.

4.5.7 Unusual Conditions

A. Occasionally, you may find a transducer whose adjacent peak outputs are unequal. This is most likely caused by an uneven surface on the transducer face. In such a case, sand the transducer face using the technique described in section 4.5.5 B. It may take more than the few passes mentioned in that description to resurface the transducer face and balance the coil outputs. However, if two dozen or so passes do not solve the problem, replace the transducer.

B. There should be no nulls along the rack higher than about 70 mv. High nulls can be decreased by sanding the transducer face. Since this process decreases both peak and null amplitude, check to see what effect the sanding has on the peak amplitude. If that is below 450 mv when the carriage is detented, the transducer must be moved closer to the rack. See section 4.5.6. Figure 4-15 shows a correct cylinder transducer output waveform.

4.5.8 General Transducer Characteristics

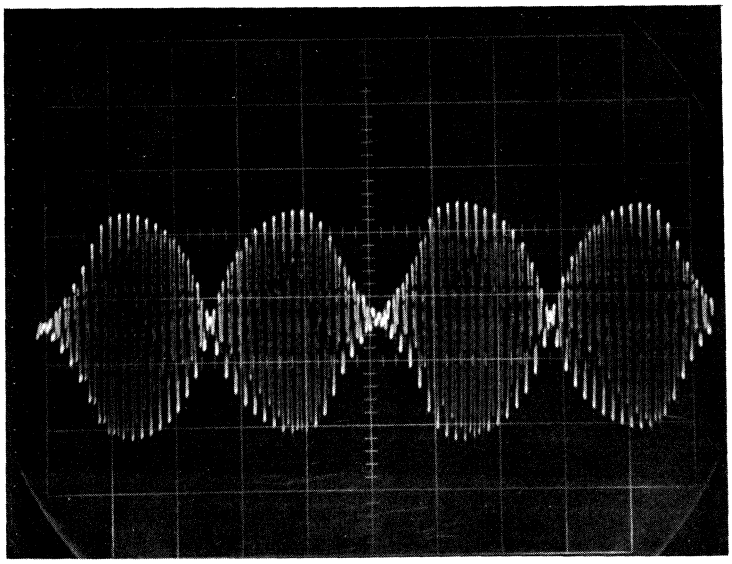
The following list defines the factory specifications used in checking cylinder transducers.

A. Minimum peak amplitude when the carriage is not detented is 580* mv.

B. Minimum peak amplitude when the carriage is detented is 450 mv.

C. Maximum null amplitude is 70 mv.

*Beginning with S/N 455 transducer oscillator voltage may be set anywhere within the range of 4 volts peak-to-peak to 7 volts peak-to-peak to raise the secondary coil peak output above the required minimum of 580 mv. This adjustment can be substituted for, or used in conjunction with, the physical adjustment of the cylinder transducer. This new voltage level will not affect the 70 mv maximum null level.



Vertical: 100 mv/div

Sweep Rate: 2 ms/div

Cylinder Transducer Output

Figure 4-15

While these values specify maximum and minimum levels, levels above the minimum or below the maximum specifications are acceptable. Nor do output levels need to be consistent for all cylinder positions. It is only required that no peak fall below the minimum specifications and no null go about the maximum specification.

4.5.9 Returning the Drive to Service

A. Turn power off at Main Power switch, S1.

B. Return the 36v to the servo drive, sixth wire from left (red) on the terminal board of the servo amplifier plate (see Figure 4-10).

C. Return the Actuator Logic Driver board, A26, to the logic file.

D. Close the Main Power switch, S1 (on).

E. Select START on the START-STOP switch.

4.6 SPINDLE DRIVE MOTOR REPLACEMENT

4.6.1 Motor Plate Assembly Removal

A. Turn power off at the main power switch S1 and disconnect the drive motor power plug from the interior control panel.

B. Remove the spindle drive belt (see Section 4.7 for removal procedure).

C. Place a support block (approximately 2.38 inches high) on the cross member of the interior control panel under the drive motor.

D. Break the lock-tite adhesive bond holding the three shoulder screws (see Figure 4-16) and loosen the screws.

E. Pivot the motor plate assembly slightly to extend the belt tension spring. Remove the two shoulder screws and plastic washers in the slotted area.

F. Allow the motor plate assembly to pivot back, releasing tension on the spring, and remove the remaining shoulder screw and washer.

G. Lift the motor plate assembly from the drive.

H. Remove the four sets of nuts and lock washers, offset bracket, vibration mount - hex standoff assembly and pulley.

4.6.2 Motor Plate Assembly Installation

A. Install the vibration mount - hex standoff assembly, offset bracket and four sets of nuts and lockwashers.

NOTE

Be certain the spring bracket orientation corresponds to Figure 4-16.

B. Install the motor plate to the vibration mount studs and secure with the four nuts and lock washers.

C. Install the motor pulley and position it on the motor shaft so that the distance from the top face of the pulley to the top surface of the motor plate is 0.240 ± 0.015 inches.

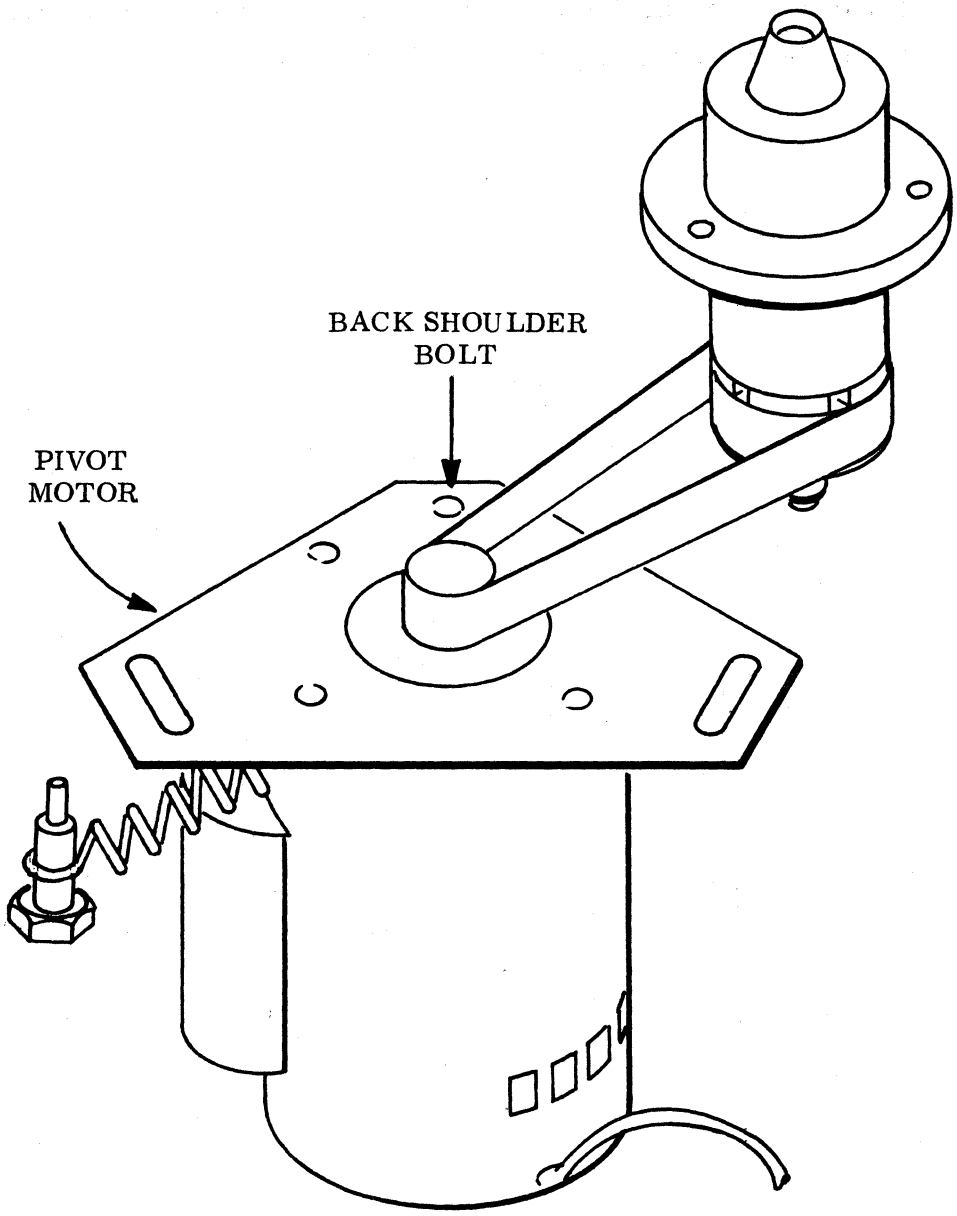
D. Apply lock-tite adhesive (PSC P/N 110877) to the shoulder screw threads.

E. With the motor supported by the 2.38 inch high block, insert the shoulder screw and washer in the pivot hole located in the deck plate. Snug down the screw (finger tight).

F. Fit the free end of the belt tension spring into the groove on the post and pivot the motor plate assembly slightly to extend the spring.

G. Install the two shoulder screws and washers in the slotted holes.

H. Allow the motor plate assembly to pivot back, releasing tension on the spring.



Drive Motor and Mount Assembly

Figure 4-16

I. Tighten all three shoulder screws to approximately 10 inch-lb of torque. Excessive tightening will indent the aluminum base plate.

J. Install the drive belt (see Section 4.7 for installation procedure).

K. Insert the drive motor power plug in its socket.

4.7 SPINDLE DRIVE BELT REPLACEMENT

A. Remove front panel, turn off main power switch, S1, on interior control panel and unplug the spindle drive motor.

B. Pivot the drive motor on its back shoulder bolt (see Figure 4-16): this will allow enough slack in the belt for it to drop off the pulleys.

C. Slip the belt between the pack-on switch and the bottom of the spindle; now the belt can be removed from the drive.

D. If the pulleys are not clean, clean them with isopropyl alcohol, P/N 110939.

E. Install a new belt.

NOTES

1. Be sure the replacement belt is the right length for the drive: 60 Hz drives use P/N 200230; 50 Hz drives use P/N 200253.
2. The smooth side of the belt should be inside against the pulley faces.
3. The belt should be centered on the flat of the motor pulley.

F. Check pack-on switch clearance: see Section 4.8 for details.

4.8 SPINDLE ASSEMBLY REPLACEMENT

A. With the main power switch, S1, off, remove the shroud area top cover, shroud, filter, filter mount and spindle drive belt (refer to Section 4.7 for belt removal procedure).

B. Remove all four spindle flange bolts.

C. Lift the spindle out of the baseplate.

D. Install new spindle assembly, P/N 200003, and tighten the flange bolts securely.

NOTE

Be sure the new spindle pulley is clean; if it isn't, clean it with isopropyl alcohol (P/N 110939).

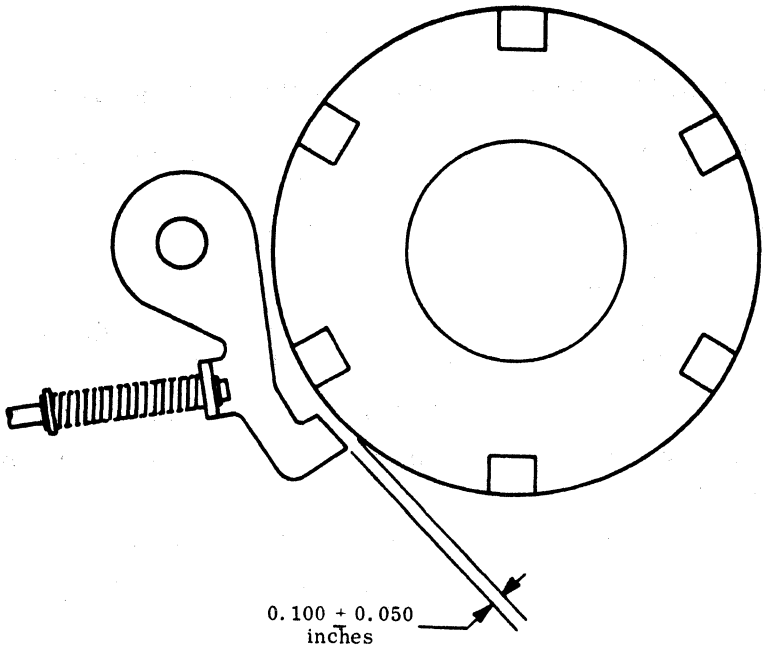
E. Replace the spindle drive belt.

F. Check brake pawl-to-pulley clearance. If necessary, deform the linkage rod to provide the necessary clearance (0.100 $\pm$0.050 inches). See Figure 4-17.

G. Install a disc pack on the spindle and check clearance between the bottom of the spindle and the lower contact arm of the pack-on switch (see Figure 4-18). If necessary, deform the upper contact arm of the switch to allow 0.025 $\pm$0.010 inches of clearance.

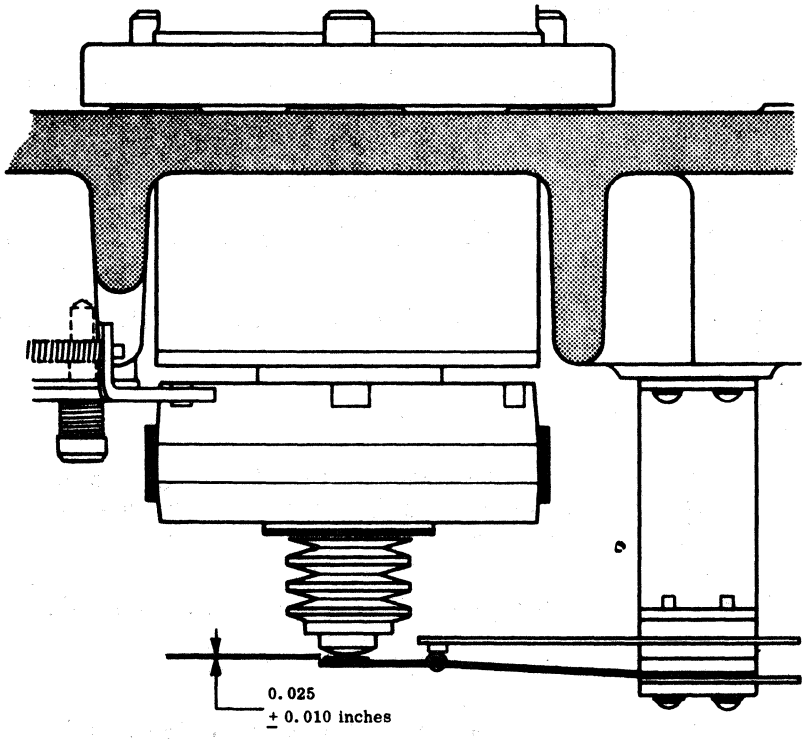
H. Remove disc pack and replace the filter mount, filter and shroud.

I. Check head alignment. See Section 4.3 for head alignment procedure.



Brake Pawl-to-Spindle Pulley Clearance

Figure 4-17



Pack On Switch to Spindle Clearance

Figure 4-18

4.9 TORSION ROD REPLACEMENT (located in shroud area cover)

A. Turn off the main power switch, which is located on the interior control panel.

B. Remove the disc pack, if one is installed.

C. Remove the shroud area cover:

(1) release the two latches located at the back of the machine where the top cover meets the main frame

(2) tilt the rear of the cover assembly up to approximately 5^{o}

(3) pull the assembly toward the front of the drive approximately 3/4 inch

(4) lift the cover straight up and off the machine.

CAUTION

- Do not hit the index transducer or the PC board mounted on the cam tower.

- Hold the cover with both hands in a way that will keep the door closed no matter how the cover assembly is tilted. This is important for the next step.

D. Stand the top cover assembly on a clean, flat surface in a vertical position (90^{o} from normal on its rear surface).

E. Allow the door to lie back gently into a fully open position. This releases tension on the torsion bars.

F. Remove the two plastic clamps which bundle the four torsion bars (each clamp holds three bars).

G. Lift the torsion bars out of their respective slots in the two plastic bearing blocks.

NOTE

Rods which miss contact with the hinge (when the the door is fully open) by more than 0.03 inch should be replaced.

H. Install torsion rods by reversing steps A through G.

NOTE

The first two rods installed should always be on the same side (i.e., install the upper rod and the lower rod on one side; then install the upper and lower rods on the other side).

I. Lubricate the rods sparingly at points of friction with a silicone grease (PSC P/N 110875) or a similar nonbleeding grease.

4.10 DOOR STABILITY ADJUSTMENT

The door normally requires 3 lb $\pm$1 lb of lifting force initially to open it. The spring loaded roller arm, which is responsible for maintaining stability in the door in both closed and open positions, can be adjusted to vary the lifting ease of the door.

A. Remove the roller arm torsion rod from its slots; remove the stationary end first.

B. Remove the three screws which hold the roller arm assembly to release tension on the arm.

C. To increase hold-down force, move the roller forward in the slots provided in the arm. To decrease the force, move the roller back.

D. Replace the roller arm assembly and torsion rod.

The initial opening should raise the door to 10^{o} to 20^{o}, where it should stabilize itself. It should require 1 to 2 pounds of lifting force to raise the door any further. All positions from 20^{o} to fully open should also be stable. If the door is unstable or if excessive force is required to open it beyond 20^{o}, two friction washer screw nuts can be adjusted to correct the condition.

A. Loosen the two screw nuts if the door resists opening.

B. Tighten the two screw nuts if the door is unstable.

C. If instability cannot be corrected by tightening the screw nuts, the problem may be caused by a defective torsion rod or worn friction washers. Replace either or both of these if such is the case.

4.11 LINKAGE LEVER - INDEX PADDLE ADJUSTMENT

The linkage lever forces the index paddle down whenever the door is opened. This retracts the index transducer from the shroud and engages the mechanical spindle lock. There should be a clearance of about 0.100 inch between the lever and the paddle. This means that the index transducer assembly first begins to move when the door is raised 1-1/4 to 3 inches. The transducer will be fully retracted when the door reaches about 19-1/2 inches. Deform the index paddle to achieve the correct clearance.

CAUTION

Support the transducer block when bending the paddle upward to prevent indentation of the radial adjustment ramp.

4.12 DETENT PAWL REPLACEMENT

Whenever either detent pawl requires replacement, all of the following items must be replaced:

A. Pivot block assembly (P/N 200330)

B. Lower detent pawl (P/N 200243)

C. Upper detent pawl (P/N 200242)

D. Bowed detent washer (P/N 200331)

E. Retaining clip (P/N 110814)

NOTE

These items are considered a single assembly and must be replaced as an assembly.

4.12.1 Detent Assembly Removal

A. Turn main power switch S1, located on interior control panel, off.

B. Remove both top covers, disc pack (if any) and shroud.

C. Remove both detent extension springs from the detent pawls.

D. Press down on the center of the retaining clip and slip it off. Then lift off the bowed washer, both detent pawls and the pivot block assembly.

E. Clean the rack and pivot block area with isopropyl alcohol (P/N 110939). Be sure all magnetized particles are removed from the rack teeth. Relubricate the rack teeth sparingly with a light grease.

4.12.2 Detent Assembly Installation

A. Install a new pivot block assembly; tighten cap screws securely.

B. Lubricate sparingly the top surface of the block, the entire pivot pin, and the sliding surfaces of both detent pawls (lower and upper) with a light grease.

C. Install the lower detent pawl on the pivot block first, then the upper pawl.

NOTE

The lower pawl is distinguished by the two raised surfaces near the pivot pin hole. This area is not raised on the upper pawl.

D. Insert the detent guide pin tool (P/N 200541) into the pivot block pin.

E. Slide the bowed washer over the guide pin with the bowed center of the washer up.

F. Place the retaining ring over the guide pin.

G. Secure the detent pawls by placing the detent cover tool (P/N 200542) over the guide pin with the recessed side down. Then force the retaining ring over the pivot pin.

H. When the retaining ring is securely clipped to the pivot pin, remove the cover tool and the guide pin tool.

I. Wipe any excess grease from the detent pawl assembly.

J. Attach the two extension springs to the two pawls.

NOTE

If there is not enough clearance between the groove ends of the detent pawls for the springs, the upper and lower pawls are reversed. See NOTE following step 4.10.2C.

K. Check cylinder transducer alignment (section 4.5) and head alignment (section 4.3).

4.13 CARRIAGE REPLACEMENT

A. Disconnect the tachometer leads at the connector located behind the operator control panel and the leads connected to the flex strips on the bobbin.

B. Remove the shroud and heads.

C. Remove the three screws which hold the T-bar to the bobbin.

D. Unscrew the tachometer rod from the back of the T-bar.

E. Remove the cap from the rear of the linear motor and pull the tachometer assembly (coil and rod) out of the motor by gently pulling on the tachometer leads. Set the tachometer assembly away from the linear motor.

F. Remove the left side panel from the drive to expose one of the screws which hold the linear motor in place.

G. Remove that screw and the two other screws located under the base plate and lift the motor off the drive.

H. Slide the carriage and T-bar back off the carriage way. When the carriage leaves the way, the spring-loaded bearing will drop off the spring.

I. Hold the bearing in place on the new carriage and slide that carriage onto the way.

J. Set the linear motor back on the base plate and slide it up against the back of the carriage way. See that the motor also fits firmly against the side alignment bar fixed to the base plate.

K. When the motor is securely positioned against the back of the way and the side alignment bar, it is properly aligned with the spindle. Replace the three screws which fasten the motor to the base plate. Use caution so that the motor does not move out of alignment.

L. Replace the tachometer assembly and cap.

M. Slide the T-bar back against the bobbin to align the carriage and screw the tachometer rod into the back of the T-bar.

N. Insert your fingers into the motor and press against the side of the bobbin in various places. The bobbin should give, indicating that it is not up against the core.

O. Check the alignment and clearance of the cylinder transducer and adjust it if necessary.

4.14 PREVENTIVE MAINTENANCE

The following maintenance operations should be performed at the indicated intervals to assure reliable operation of the drive. Preventive maintenance should be limited to these routines as long as the drive is functioning normally.

Period	Procedure
30 days	• Clean the face of the detent rack with a soft bristle brush dampened with 90% isopropyl alcohol.
30 days	• Apply a small dab of grease on the flat surface of both detent pawls where the actuator push rod makes contact.
30 days	• Inspect head shoe and disc surfaces for damage or contamination. These should only be cleaned when contamination (such as oxide deposit on the head shoe) is likely to cause read or write errors or the heads to crash. The cleaning procedure is described below.
30 days	• Inspect pack filter and main blower filters and replace when dirty.
30 days	• Apply a drop of No. 10 oil in the top of the spindle to ensure easy removal of disc packs.
	-----
60 days	• Apply two drops of No. 10 oil between the detent pawls.
60 days	• Place a drop of No. 10 oil between the washer and pawl of the mechanial spindle brake. Compress the spring on the brake spindle to separate the washer and pawl.
6 months	• Clean the carriage way with a Kimwipe dampened with 90% isopropyl alcohol and wipe dry. Then apply a light coat of No. 10 (PSC Part No. 200824) oil on the carriage way (under the rollers).

If head shoe and disc surfaces need cleaning, the following routine should be performed.

A. Remove the shroud area top cover, the disc pack, and the shroud. Turn the main power switch (located on the Interior Control Panel) to the off position.

B. Move the carriage out by hand until the load/unload ramp is just at the point of riding off the cam. Do not load the heads, or serious damage will result to the bearing surfaces of the read/write elements.

C. Wrap a Kimwipe tissue around a head paddle (a wooden tongue depressor will do) and dampen (do not soak) one end of it with 91% isopropyl alcohol (9% distilled water). Wipe the bearing surface of each head thoroughly with the dampened end of the paddle, push the paddle further into the assembly and use the dry portion of the Kimwipe to dry the surface of the head. Remove the paddle by pushing it toward the center of the carriage until it is clear of the cleaned head and then pull it out. This technique will prevent the dampened portion of the Kimwipe from contacting the cleaned surface of the head.

   It is extremely important that the surface of the head be dried immediately after cleaning with alcohol to prevent evaporation which will result in a residue on the bearing surface.

D. After all contaminated heads have been cleaned, check the flexures and arm assemblies for loose pieces of Kimwipe tissue.

E. Return the carriage to the retracted position and inspect the gimbal flexures and arms for broken welds. Replace any defective assemblies.

F. Replace the shroud and disc pack.

SECTION 5.0

INSTALLATION PROCEDURES

5.1 GENERAL

The following information is provided as a guide to personnel responsible for installing a Model 630 drive. It outlines some basic procedures which should bring the drive on line in as short a time as is practical. These procedures are not intended as a substitute for whatever standard practice the customer may have for equipment installation.

5.2 UNCRATING AND INSPECTION

A. Examine the packing crate. If there is any damage to the crate, note the damage on the freight bill before releasing the unit from the carrier.

B. Remove the steel bands from around the top and bottom of the cardboard packing crate.

CAUTION

Be careful when cutting these bands; they can spring back and cause injury to anyone standing near the crate.

C. Remove the top and side cardboard covers.

D. Cut the nylon bands around the machine.

E. Remove the floater (cardboard box on top of the machine). The instruction manuals and kick panels are inside this box.

F. Remove the plastic cover and packing material from around the machine.

G. Pull off the front and rear panels from the machine. Pull each panel toward you from the top; they are held by magnetic clips.

H. Remove the machine from the bottom packing cover. Exercise care, as the weight of the equipment is between 295 and 325 pounds; depending on the model.

I. Install the two rear caster locks. To do this, turn the rear casters so that they face front to rear (rollers positioned nearest to the outside of the cabinet), and use the screws provided to secure the locks to the bottom of the main frame from inside the cabinet.

J. Remove the cardboard supporting block from beneath the power supply chassis (left-hand door in the back of the machine).

K. Remove the two top covers. Lift them from the front; the clips holding the backs will automatically release.

L. Remove the tape that straps the carriage to the linear motor.

M. Remove the wooden blocks from around the deck plate.

N. Remove the sheet metal cable entrance cover so that the cables can be routed through the cable hole (in the bottom of the machine) to the cable connectors.

O. Examine the interior and top deck plate of the machine. If any damage is discovered, notify the carrier.

P. Check to be certain that all printed circuit boards are secure in their connectors.

Q. Check to be certain that the head plugs are connected to the connectors on the Read/Write Amplifier boards.

R. Clean the heads (some dirt might have accumulated during shipment). Refer to Section 4.14 of this manual for instructions on cleaning heads.

5.3 ENVIRONMENT

The disc pack drive should be placed so that there is a 3 foot clearance at both the front and rear of the machine. This allows room to remove the front and rear panels for maintenance. Refer to Figure 2-3. The room temperature range should be between 60° F and 90° F with temperature changes less than 15° F per hour.

5.4 INSTALLATION

A Memorex Model 120 Off-Line Tester and a CE alignment pack (yellow shield, IBM P/N 2200018) are needed to properly perform the necessary operational checks on the drive. To prepare the drive for operation, proceed as follows:

A. Check to be certain the power switch, S1, on the interior control panel, is in the OFF (down) position. Then connect the primary ac power cable (all cables are shipped in a separate carton) between the AC IN connector, J1 on the interior control panel and the controller.

NOTE

Because the disc drive has ground currents in excess of 5.0 milliamperes, the controller, or control unit to which these drives are connected, must have electrical grounding that contains the following:

a. An insulated grounding conductor that is identical to the grounded and ungrounded branch-circuit supply conductors except that it is finished to show a green color or green with a yellow stripe is to be installed as part of the branch circuit that supplies the unit or system.

b. The grounding conductor mentioned in item a is to be grounded at the service equipment.

c. The attachment-plug receptacles in the vicinity of the unit or system are all to be of a grounding type, and the grounding conductors serving these receptacles are to be connected to the grounding conductor that serves the unit or system.

If the drive is part of a string of drives, the second and subsequent drives in the string receive their power via the AC OUT connector, J2, on the previous drive. All cables which are connected to the drive must enter the machine through the cable hole in the bottom of the machine.

NOTE

The maximum three phase current which may be fed through the ac connections on any drive to power it and succeeding drives in the string is 26.0 amps per phase.

B. Check to be certain that the switches on the operator control panel are all down.

C. Install the CE pack on the drive. Move the carriage out by hand a short distance to check that the heads will not hit the edges of the discs.

NOTE

This procedure is included as a precaution against attempting to perform a first seek with heads which might be out of line as a result of damage during shipment.

D. Connect the Model 120 Off-Line Tester to the drive as instructed in the Model 120 instruction manual.

E. Turn the main power switch, S1, ON. The main blower and the power supply cooling fan will come on. Examine the machine for any signs of component overheating.

F. Select START with the START-STOP switch on the operator control panel. The disc pack will begin rotating. Following a pack temperature stabilization delay of 60 seconds, the heads will move out to the forward stop and then perform a reverse seek to cylinder 000. If any head chattering (the sound the heads make when they come in contact with the disc) occurs, power down immediately by selecting STOP. Head chattering means that

either a head(s) or disc pack is damaged. If no head chattering occurs, proceed with the installation check out.

G. Check head alignment as described in Section 4.3

H. Check the index transducer circumferential alignment. The procedure for this check can be found in Section 4.4.

I. Use the off-line tester to perform random seeks in the AUTOCYCLE mode for 10 minutes. Then seek to cylinder 000. Verify that the carriage is at cylinder 000 by checking the cylinder scale on top of the Tee-block.

J. Select STOP with the START-STOP switch. Make certain that the disc pack comes to a complete stop in 10 to 15 seconds after STOP has been selected. This verifies that dynamic braking is working properly.

K. Attach the kick panels to the bottom of the machine with the clips which are already mounted. Replace the two top covers. Be sure the disc pack cover (right hand) is closed while installing it. Otherwise, the door-open interlock arm may not properly engage the paddle on the index transducer.

L. Select START with the START-STOP switch. When the disc pack motor comes up to speed, open the disc pack cover door. When it is open about 1 inch, the heads should retract and the motor should shut off. Dynamic braking is not applied in this case, so the disc pack will coast slowly to a stop. Close the disc pack cover door.

M. Use the off-line tester to make a quick write/read check.

1. Select READ/WRITE with the READ/WRITE-READ ONLY switch.
2. Write all ONEs with any head on cylinders 000 and 128.

CAUTION

Use only these cylinders for this operation. Valuable information is permanently stored on other cylinders of the CE pack.

3. Select the READ mode. Monitor the output of the Read Amplifier, A10, by connecting an oscilloscope to pin 4 of A10.
4. The double frequency (2F) pulses observed on the oscilloscope should be at a 2.5 MHz rate.

5. Write all ZEROs with the same head on cylinders 000 and 128. The single frequency pulses (1F) should be at a 1.25 MHz rate.

6. Disconnect the oscilloscope.

N. Select STOP with the START-STOP switch, turn the main power switch, S1, OFF and disconnect the Model 120 off-line tester.

O. Connect the controller's Bus cable to the BUS IN connector J3 on the interior control panel of the drive. If the drive is not the first drive in a string of drives, connect the cable that comes from the Bus Out connector, J4, of the previous drive to the Bus In connector, J3.

P. If the drive is the only drive or the last drive in a string of drives, plug a line terminator assembly into the Bus Out connector, J4.

Q. Connect the proper Unit cable from the controller to the Unit connector, J5, on the interior control panel. The controller has a separate Unit cable for each drive.

R. When all cables are connected, replace the sheet metal cable entrance cover.

S. Turn the main power switch, S1, ON and then replace the front and rear panels.

T. If the drive is part of a string of drives (but not the last drive) it should be checked for proper power up sequencing. To do this, first make certain a disc pack is on the drive and the disc pack cover is closed. Leave the drive's START-STOP switch in the STOP position. Place the next drive's START-STOP switch in the START position. In a power up sequence from the controller, the drive under test will not come on; it will be bypassed and the next drive in the string will turn on.

U. To make certain that the next drive turns on when the drive being installed comes up to speed, place the START-STOP switch on both drives in the START position. Power up from the controller and observe the first drive come up to speed (70% of spindle drive motor speed). At this time, the spindle drive motor on the second drive should begin rotating.

V. As the last step in the installation check, select STOP with the START-STOP switch.

LOGIC DESCRIPTIONS

AND

DIAGRAMS

POWER UP SEQUENCE AND INTERLOCKS

POWER SEQUENCING

The purpose of a power sequencing scheme is to prevent simultaneous starting of all the drives in a multiple drive system. This could happen if all START-STOP switches on the drives were in the START position and no sequencing control were provided. In starting, the controller would attempt to power up all the drives at once and the lines would be overloaded. (The drives draw approximately six times as much startup current as running current.) Power sequencing avoids overloading by requiring that a drive reach approximately 70% of full speed before the next drive in line can receive its power.

In a normal startup of a string of drives, each drive will have its main power switch (S1) on and its START-STOP switch in the START position. When the controller powers up, it supplies ac power to each drive, turning on the main cooling blower, logic card file fan and dc power supply via a ferro-resonant transformer.

This dc power supply provides +26 vdc, -26 vdc, +24 vrac (volts rectified ac) and +36 vdc. Electronic regulators convert the +26 vdc to +18 and +5 vdc and the -26 vdc to -18 and -3 vdc for use by the drive's logic. The +24 vrac is supplied by the same rectifier as the +26 vdc but is isolated from it and has very little filtering; it contains a high degree of ripple. The unregulated +36 vdc is used for powering the positioning motor, providing dynamic braking power to the drive motor, energizing the detent actuator and energizing K1, the sequencing relay.

In a typical power-up operation, the +36 vdc in the first drive in the chain will leave the drive on J3, pin 78, go through a jumper in the controller and reenter the drive on J3, pin 77. From there it passes through an isolation diode (CR8) and a resistor (R8) and enters the coil of K1. If a ground return is available through the controller via J3, pin 76, K1 will energize and the +36 vdc contributed by the dc power supply through contacts 9-6 will hold K1 energized. This self-holding feature of K1 makes each drive independent of the previous drives once K1 has picked.

As soon as K1 in the first drive has picked, contacts 8-5 provide a ground return for the motor relay K2. Then, if the door switch is closed, if the heads are retracted and if the START-STOP switch is in the START position, the spindle drive motor will start (the interlock system is described in detail in the INTERLOCKS section below). When the disc pack reaches approximately 70% of full speed, a speed sensing system provides a ground return for the speed relay (K3), causing it to energize. This sends +36 vdc to the next unit via K3 contacts 8-5, K1 contacts 7-4 and the signal out connector J4, pin 77. This sequencing voltage causes K1 in that drive to pick.

If the START-STOP switch is in the STOP position, the drive's interlock system will be bypassed. Since the spindle drive motor does not start, sequencing to the next drive does not wait for the speed sense relay (which would never pick). Instead, as soon as K1 picks, +36 vdc is sent to the next drive through the STOP contacts of switch S2-A and K1 contacts 7-4.

INTERLOCKS

A safety interlock system is incorporated in the drive which prevents the disc drive motor from starting unless certain conditions are met.

A. K1 must be energized.

B. The door switch must be closed; i.e., the drive's top cover is closed.

C. The START-STOP switch must be in the START position.

D. The heads extended-retracted switch must be in the retracted position.

If these five conditions are satisfied, a ground return is provided for motor relay K2 and the warmup delay relay K7, which are connected in parallel. The motor starts. At 70% of full speed, speed relay K3 energizes and removes a ground from the -retract heads circuit by breaking contacts 7-1. The -retract heads line is also interlocked with the open contacts of door switch S5, the STOP contacts of S2-B, and the deenergized contacts 8-2 of K1. However, if the interlock conditions listed above are met, K3 removes the last ground from the -retract heads line.

The warmup delay relay K7 requires approximately 45 seconds of voltage to its coil before it energizes. During this interval, contacts 7-1 provide a ground for the -power up reset line, which resets all system logic. After the warmup period, K7 energizes, and contacts 7-4 make, providing a ground for the -first seek enable line. This initiates a first seek. +36 vdc are supplied to the servo power amplifier via servo power relay K6, contacts 7-4 to launch the heads. K6 will be provided a ground return via a relay driver on card CO7 when the electronic logic is complete (see below).

Once the heads are launched, one of the original interlock requirements (-heads retracted) is lost; however, S3-B is shunted in parallel by the energized contacts of K3. As long as K3 is energized, it is presumed to be safe to launch heads; however, if the speed relay deenergizes during routine operation, contacts 7-1 of K3 would provide a -retract heads signal, causing the heads to retract at a slow speed. This situation could be caused by a broken drive belt, a faulty spindle drive motor or some similar circumstance. Should any of the other interlocks fail while the heads are extended, (START-STOP switch, door switch, or sequence relay) the same -heads extended line would be provided with a ground. Each of these interlock failures would cause the heads to retract and, as soon as the heads were retracted, would remove ground from K6, deenergizing the servo power relay. This keeps the heads in the retracted position until the interlock sequence has been reinstated. In addition, if the door switch or START-STOP switch are involved, motor relay K2 and warmup relay K7 deenergize, causing the whole system to come to a halt. If the interruption in the interlock is restored (such as opening and closing the cover door) the system will go through a normal start-up, including the warmup delay, will launch the heads again and will initiate a first seek.

The controller initiates a power-down sequence by dropping the controlled ground for all the K1 relays. This opens the basic interlock, but the by-pass around the original system via the energized contacts 9-6 of K7 keeps the disc motor turning until the heads have been retracted. Once the controller confirms that the -heads extended line is clear (indicating that all drives have retracted their heads) it shuts off ac power.

POWER FAILURE

Power failure in the drive, which may be caused by loss of ac power from the controller, a blown main fuse in the drive or defective wiring, requires that the heads be retracted from the disc pack as rapidly as possible. Power failure relay K4 is responsible for this safety feature. Within a few milliseconds after power is first available at the main power switch, K4 is energized by the +24 vrac. The relay remains energized until there is a power failure, or power is turned off at the main switch.

When K4 deenergizes and contacts 9-3 make, a -emergency retract signal is applied to the servo power amplifier, overriding any normal command signals present at the servo power amplifier inputs. In effect, it calls for full speed retract of the positioner motor. However, since the servo power relay, K6, is also being deenergized by the loss of +24 vrac, the breaking of contacts 7-4 removes the +36 vdc to the power amplifier. K4 contacts 7-1 make in the deenergized position, supplying the power amplifier with the stored energy in the +36 vdc system. This causes the heads to retract at maximum speed.

Power failure is the only reason for head retraction at maximum speed; any other power down or interlock interruption causes the heads to retract at a relatively slow speed. When turning a drive off, it is advisable to select STOP on the START-STOP switch before switching off the main power switch.

DYNAMIC BRAKING

Dynamic braking of the spindle drive motor is used to bring the disc pack to a quick, smooth stop. It is accomplished by applying +36 vdc to the field windings of the motor; this induces heavy current flow in the shorted armature windings in a direction and magnitude which opposes the dc field. The opposing fields brake the motor to a halt in about 7 seconds. The +36 vdc is applied to the motor only when the START-STOP switch is in the STOP position; under any other condition, there is no dynamic braking available.

When STOP is selected, +36 vdc is supplied to the motor via the back contacts of S2-A, the deenergized contacts 9-3 of time delay relay K5 and the deenergized contacts of motor relay K2. A ground return is provided by the second set of deenergized contacts on K2. Ten seconds after the heads have retracted, K5 energizes and cuts off dynamic braking. If the heads are already retracted when STOP is selected, the 10-second delay begins immediately.

Since the disc drive motor represents a highly inductive load, opening of contacts 9-3 of K5 would cause a voltage surge that would tend to arc over these contacts. Capacitor C1, which is connected across the motor, dampens this voltage surge to an acceptable value (refer to schematic 008027). If K5 ever fails to deenergize for some reason, the dynamic braking current (about 8 amp at 36 vdc) will not overload the power supply. Extended application of the current would probably create enough heat in the motor windings to activate the thermal-overload cutout in the motor. This would interrupt the current flow (refer to schematic 008022).

SIGNAL CONDITIONER (refer to schematic 001567)

Four of the signal lines originating in the relay switching and control system share a common problem. They indicate some degree of noise, even when grounding the circuit; the signal lines are often open (i.e., not grounded). In order to provide solid switching of the associated logic circuits, the signal conditioner assures that some of the noise is suppressed, and that both the grounded and ungrounded line conditions result in solid output logic signals. This is accomplished by a positive dc voltage on the gate inputs when the line is not grounded, and a negative voltage on the gate inputs when the lines are grounded. Small by-pass capacitors render the system insensitive to short-duration noise pulses.

CONTROL TRANSLATION

The controller selects one unit out of a series by activating the select unit line to a particular unit. This line, which enters on J5, pin 23, is combined with a file safe condition to partially enable the control translation network of a selected unit.

The control translation network input consists of eight unit bus lines, which all come in on J3, and three tag lines (a fourth tag line, set difference, comes into J3, pin 15 but is not used by the unit). Functions of the three tag lines, set cylinder, J3, pin 17; set head and direction, J3, pin 18 and control, J3 pin 21, are defined in detail in Section 2.3.2.2, Communication Lines. The unit bus lines are also defined in Section 2.3.2.2. Depending on which tag line is activated, one or more bus lines will be used.

The control tag line is used to partially enable the eight unit bus lines; one of these eight is selected by the controller to initiate a particular function (i.e., select write, select read, seek start, select reset head register, select erase, head select, select restore/retract and select head advance).

The set cylinder tag line gates all eight bus lines, which contain the address of the cylinder about to be selected, into the cylinder address register (CAR).

The set head and direction tag line gates bus lines 4 through 7, which contain the address of the head about to be selected, into the head address register. Before the head address can be gated into the head address register, however, the register must be reset. This is done by selecting the control tag line and bus line 3, select reset head register or as part of a first seek or restore operation.

Inputs from the bus lines go only to the direct set side of the register flip-flops; this provides for a transfer of one's only rather than a forced transfer. Output of the head address register flip-flops goes through the head switch decoder to the head switch drivers. These are shown in the Read/Write logic diagram.

CAR AND PRESENT ADDRESS REGISTER

CYLINDER ADDRESS REGISTER

The set outputs of this eight-bit register go to the controller through the CAR line drivers. The reset outputs go to the adder. Input to the CAR is by forced transfer directly from the unit bus lines.

PRESENT ADDRESS REGISTER/COUNTER

The eight-bit present address register/counter consists of eight JK flip-flops, four of which have their direct set inputs tied down. The four not tied down allow the register to be force set to 204. Other inputs to the register are: preset to zero, cylinder count pulses from the cylinder transducer amplifier, and either a forward up count enable or a reverse down count enable. The register may be reset as part of a power-up sequence or a restore operation.

When the forward direction gating is enabled, the reverse down count enable line into inverter B06-2B is high. The low output from 2B goes into OR gates A/B10-2D, 4D, 6D and 8D and A/B11-2D, 4D, 6D and 8D. This clamps the output of each OR gate trying to go high. At the same time, the forward up count enable line is low into AND gate B06-1B and OR gate B06-3A. A high out of B06-3A enables the J and K inputs to the first counter flip-flop and partially enables AND gate A/B10-2B on the set output line. The first cylinder pulse coming to the block input of that flip-flop will set it. All other flip-flops in the counter have low inputs. With the first flip-flop set, the AND gate A/B10-2B from the set output is satisfied, providing a low into OR gate A/B10-2A. Since each of the two OR gates feeding the second flip-flop has a low input, the collector AND on their outputs is enabled; its high output sets the J and K inputs to the second flip-flop. The next cylinder pulse into the clock inputs will reset the first flip-flop and set the second one. Resetting the first flip-flop disables the AND gate on its set output. This disables J and K inputs to the second flip-flop so that the next cylinder pulse will set the first flip-flop. Again the AND gate on its set output is completed. The OR gates and collector AND for the J and K inputs to the second flip-flop are high. This flip-flop is set and the AND gate on its set output provides a low to OR gate A/B10-2A. High outputs from OR gates 2A and 2D satisfy the collector AND which sets the next flip-flop (No. 4). The fourth cylinder pulse resets the first two flip-flops and sets the third. This process continues, increasing the present address register's contents; a reverse direction enable causes a similar sequence.

Power up and restore sequences first preset the present address register/counter to zero. This is maintained during the 800 ms forward travel. Following this delay, a count of 204 is loaded into the register. A power down sequence clears the counter. Refer to the Access Control logic diagram (200615) description for power up and restore details.

ADDER

The adder is made up of eight full-add IC modules. Each module combines two bits and a carry and gives an inverted carry out and sum out. The inverted carry is supplied by the adder module. To get a complete sum, inputs to every other adder module must be inverted. Since each module sends out an inverted carry, different pins are used on each module for inverting signals. For clarification, refer to the adder schematic (001197). This shows the pin configuration on each adder module.

All inputs, with the exception of -force difference (sent from home seek logic) and +forward (sent from seek forward/reverse logic), come from the cylinder address register and present address register/counter. In a compare (detent condition), each adder module has for one input a logical zero and for the other a logical one.

The carry line is called an end around carry; it is connected back from bit 128 to the carry input of bit 1. It also goes out to seek gating as the direction carry. When the carry line is high, a reverse seek is indicated.

The output of each adder is sent to two AND gates; it goes to one directly and to the other through an inverter. The one set of AND gates is enabled by the +reverse line which comes from the carry output of bit 128 adder module. The other set of AND gates is enabled by +forward which comes from seek gating.

Forward and reverse gate outputs are brought to an OR gate. The output of the OR gate goes to an output pin on the adder board and through an inverter to another output pin. In each case, the two outputs are labeled true and not. The true outputs (1, 2, 4, 8, etc.) are not used. The not outputs ($\overline{1}$, $\overline{2}$, $\overline{4}$, $\overline{8}$, etc.) go to the speed decode network. With a forward gate enable, the true output of each adder module goes to the speed decode; with a reverse gate enable, the inverted output of the adder modules goes to the speed decode.

The input +forward is high during controller-instructed seeks as dictated by the logic in the carry line in A24. This input is low at all other times (except during the reverse portion of the power up or restore sequences).

During forward travel in a power up or restore sequence and during reverse travel in power down, a collector OR tied to A/B12-EE forces $\overline{4}$ of the adder low, while all other outputs are high. This low output forces a difference count of 4 into the speed decode network. At this time, +reverse into A/B12-KK is high.

SPEED DECODE NETWORK

The Speed Decode Network is responsible for converting the output of the adder (i.e., the number of cylinders required for positioning the heads during a seek) into a drive current input to the servo amplifier. Input lines from the adder to the speed decode network are gated by a forward or reverse enable. Refer to the Adder logic diagram, 200612.

Forward and reverse operations are performed by separate decode sections. This is necessary because the motor has more force in the reverse direction. The same eight input lines from the adder feed both sections. Forward and reverse speed decode enable lines (one each) select which section will use the input. The eight inputs from the adder also go to an OR gate with expander inputs. Its output is labeled -compare.

At the beginning of a seek, when the detent is engaged and when the contents of the CAR and the present address register/counter agree (no output from the adder), the following two conditions exist:

A. The forward and reverse gating lines to the adder output are both low.

B. Inputs to the speed decode network are all high.

With all inputs to the speed decode OR gates high, these OR gates will supply low inputs to their AND gates. The AND gates, in turn, will produce a high output (+5 volts) which provides zero drive to the servo amplifier. The high condition of the eight adder output lines does satisfy the requirements of the compare OR gate, however. Its output is low and is labeled -compare. The -compare line is connected to pin P on the speed decode board and enables inverter A/B 15-4B. The high output of 4B partially enables AND gate 3A. The output of 3A does not go low when the detent is engaged, however, because the other input line, labeled +detent speed enable is not high. If AND gate 3A were enabled and its output did go low it would provide detent velocity to the servo amplifier.

When a seek is initiated by gating a new address into the CAR, some of the adder output lines will go low, indicating the number of cylinders required for positioning. Assuming that the positioning requires a forward seek of greater than 64 cylinders, the true output of the adder is gated to the speed decode network. A +forward speed decode enable is generated by the detent logic and partially enables the AND gates of the forward section of the speed decode network (9D through 3C). Because the seek is greater than 64 cylinders, at least one input from the adder to the first two OR gates, 9C and 2A, is low. This low input forces the output of the gates to go high. The high outputs complete AND gates 9D and 1D so that their outputs go low. The low outputs of gates 9D and 1D turn on their diodes, supplying current to the servo amplifier. This low out of 1D also serves as the input to OR gate 2C. The low input to 2C forces a high output, satisfying the third AND gate, 1C. Its low output forces the output of OR gate 2B to go high, satisfying AND gate 1B. This continues down the line until all seven pairs of OR gates and AND gates in the forward section of the speed decode logic are activated. In each case, the active outputs of the AND gates cause the diodes on their output lines to be biased on and conducting. The current on all seven output lines is summed and provides maximum current to the servo amplifier.

As soon as the output from the adder indicates that there are fewer than 64 cylinders left for positioning, all inputs to gates 9C and 2A go high, causing their outputs to go low. The lows into AND gates 9D and 1D drive their outputs high and turn off their diodes. The current supplied to the servo amplifier is reduced by the amount contributed by the outputs of 9D and 1D. At each succeeding decode difference level, that is 32, 16, 8, 4, 2 and 1 cylinders, the respective OR and AND gate pairs will turn off, one pair at a time, reducing the total current input to the servo amplifier by discrete amounts.

When the adder output reaches zero, the forward section of the speed decode network stops supplying current to the servo amplifier. At this point, all input from the adder is high and the OR gate which provides the -compare signal is satisfied. This -compare signal goes high at inverter 4B and partially enables 3A. Since the +detent speed enable line is also active at this point, AND gate 3A is satisfied, providing a low output. The low output from 3A supplies detent velocity current to the servo amplifier. When the detent engages and velocity decreases to zero, this AND gate is disabled and removes drive from the servo amplifier.

The decode logic for a reverse seek is effectively the same as for a forward seek with these three exceptions:

A. Resistor values on the output lines of the AND gates are different for the two sections.

B. Current values supplied to the servo amplifier are different for the two sections.

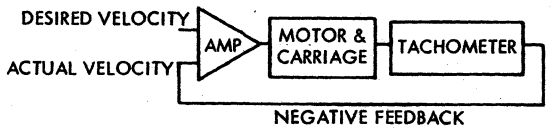
C. The +detent speed enable line is only connected to the forward section. When compare occurs on a reverse seek, reverse drive to the servo is removed. At this time the two lines (-compare and +detent speed enable) are active and provide forward detent velocity. This causes the carriage to turn around so the detent falls while the carriage is moving in the forward direction. As in a forward seek, 0 velocity will remove the forward drive detent velocity signal to the servo.

SERVO CONTROL SYSTEM

The servo amplifier used in the Model 630 is a velocity servo; it consists of a tachometer and amplifier, a servo amplifier and a power amplifier (see simplified block diagram below). Output from the amplifier is used to control the speed and direction of travel of the linear positioning motor. A tachometer is attached to the motor to monitor its velocity.

The basic inputs to the servo amplifier are: a negative feedback voltage from the tachometer and two inputs from the speed decode network which specify the velocity requirements imposed by the number of cylinders required for the seek. Two inputs are used because this is a differential amplifier and a forward or reverse direction must be determined.

When a desired velocity arrives at the servo amplifier and the carriage is standing still, the amplifier algebraically sums the desired velocity (as represented by the speed decode output) and the actual velocity. Because the carriage is not moving, an algebraic sum of the desired velocity and a zero velocity from the tachometer provides maximum input to the servo amplifier. The servo amplifier turns on the motor and tries to cause the current to jump to its maximum value. Resistors in series with the motor and power amplifier limit this current to about 5 amp.



Inductance in the motor and back emf prevent the current from jumping instantaneously to 5 amp. Back emf increases in amplitude from zero as the armature begins to move and accelerates. There is a theoretical velocity (about 100 ips) at which back emf would equal the power supply voltage so that current flow would cease.

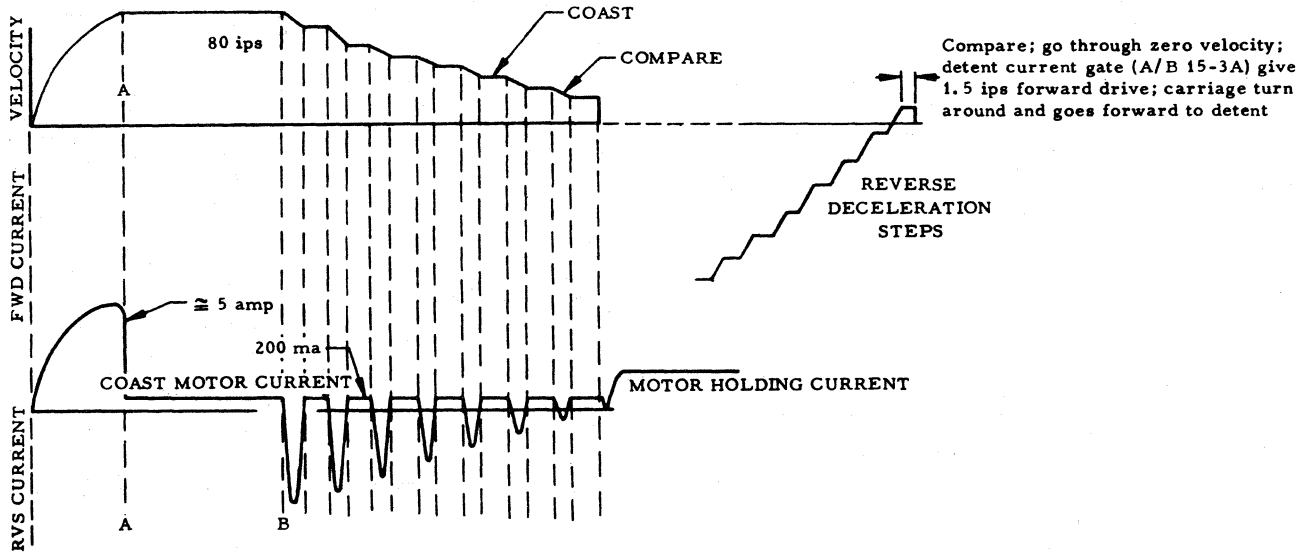
At some velocity below this (represented by A in the following sketch), the negative feedback essentially cancels the desired velocity output. This is the maximum desired velocity (approximately 80 ips) for seeks of 64 cylinders or longer. Only about 200 ma are required by the motor armature to overcome mechanical friction and wind resistance to maintain that velocity. Negative feedback from the tachometer will compensate for minor fluctuations in velocity.

When the speed decode network determines that there are fewer than 64 cylinders to go, the desired velocity becomes less than the actual velocity. Excess negative feedback provides the amplifier with reverse voltage input. Motor current builds up in the reverse direction at a sharper rate than in the forward direction because back emf is now assisting the power supply (see B on the current level curve in the following sketch). As the current increases, the armature and carriage decelerate sharply; negative feedback drops off.

At some point in the deceleration, the negative feedback (actual velocity) will again equal desired velocity. This is represented on the velocity and current curves by the short, horizontal segments. Again, the motor current will be briefly held at about 200 ma. The coast period has been greatly exaggerated in the sketches.

The next lower decoder output (32 cylinders) causes another reverse pulse of current; actual velocity is again greater than desired velocity. This sequence of deceleration steps continues. As velocity decreases, the successive peaks of the reverse current waveform also decrease. Five amp of reverse current are no longer needed before the desired velocity is reached.

The last velocity step occurs when compare is reached. The speed decoder output becomes zero since there is no difference count from the adder; however, the detent velocity gate 3A is activated by an inverted -compare and a +detent speed enable signal so that enough forward current is supplied to the motor to maintain a 1.5 ips forward velocity. This is the carriage velocity at which the detent pawl engages with the detent rack. Detent velocity current lasts for approximately 3 ms. When the detent drops in, velocity drops on a straight line to zero.



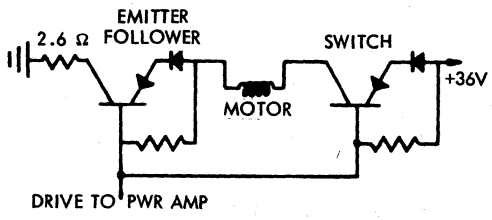
The preceding curve also shows the deceleration portion of carriage velocity during a reverse seek. The most significant difference between reverse and forward seek velocity curves is that the reverse curve includes a turnaround segment. When compare is reached in a reverse seek, output of the reverse decode network goes to zero; there is no reverse drive to the servo. Inertia of the carriage keeps the carriage moving at about 3 ips. Since there is a +detent speed enable and an inverted -compare into detent velocity gate 3A, this servo is supplied with forward detent velocity current which causes the carriage to coast through zero velocity, turn around and proceed forward while the detent drops in.

The following sketch shows a pair of transistors of the power amplifier in the motor winding. One transistor (tied to +36 volts), acts simply as a switch. When this transistor is turned on, it is driven into saturation and will pass or conduct all of the current the power supply is capable of delivering through the motor and the 2.6-ohm resistor. The other transistor acts as an emitter follower which controls the amount of current through the motor.

As shown in the schematic portion of the logic diagram, the output of the tachometer is tied across a 50-K pot and 6.8-K resistor. This pot is adjusted to change motor speed. It, in turn, feeds a differential amplifier. By feeding the tachometer output into the differential amplifier, amplitude of the signal out of the tachometer is doubled. This is desirable since the tachometer output is relatively low.

This signal enters the servo amplifier board on pins B and D. There is a 10-K resistor on each of the negative feedback input lines to the servo amplifier just before the lines join the forward and reverse input lines from the speed decode network. The forward and reverse speed decode input lines each include 2.21-K resistors. On the pair of lines formed by the junctions of the negative feedback and speed decode input lines are two 46.7-K resistors referenced to +18 volts (one resistor per line). Negative feedback and speed decoder output current is summed through these resistors; the algebraic sum of actual velocity and desired velocity becomes the differential inputs to the servo amplifier. Each input to the servo amplifier has a 0.0068 μf capacitor tied to ground. This serves as a high-frequency filter to the input signal. High-frequency oscillations are shorted to ground through the capacitors.

Inputs to the servo amplifier on pins 3 and 9 have a +18-volt reference. Outputs on pins 2 and 10 are referenced to about +13 volts; this is merely a characteristic of the amplifier IC used.



The Darlington-connected transistors (the 2N3568's and 2N3054's) need a reference signal of -2 volts. Between the Darlingtons and the servo amplifier are a pair of 2N3906 transistors which change the reference from the servo amplifier from +13 volts to -2 volts to drive the Darlingtons in the power amplifier. This also provides additional gain and the 10-K pot provides system gain control.

A negative voltage on the base of the Darlington-connected transistors will turn them off. When they are turned off there is an open circuit to the base of the power transistors. Any leakage current through the power transistors goes through the diode in series with each emitter. The voltage drop across this diode assures that the power transistors are turned off or are not conducting with this zero input signal. A zero voltage on the base of the Darlingtons causes them to turn on and a ground is placed on the input of either the forward or reverse power amplifier drive. If it is forward, a ground at TB2, the power amplifier, will drive the base negative with respect to the emitter; the power transistors will turn on. When they turn on, there is a complete circuit from ground through the motor and the power transistors to +36 vdc. The power transistors are germanium PNP units and tend to have a fairly high current leakage with an increase in temperature. To compensate for this, silicon diodes are put in series with each emitter. There is about a 0.5-volt drop across each diode. Then leakage current through the germanium develops a voltage across that diode which keeps the power transistors turned off with zero signal in, even if the temperature does rise.

DETENT AND ACTUATOR CONTROL

DETENT LOGIC

There are seven output lines from the detent logic board B25. The following list defines each line and identifies the logic level, when the detent is engaged and before a seek is initiated.

A. Forward Servo Bypass and Holding Current (Both Active)

These two lines work together to perform a single function. The forward servo bypass line bypasses the servo amplifier and provides a forward signal to the motor power amplifier. The holding current line enables holding current, which limits the current through the motor. This causes the carriage to maintain a positive force against the reference surfaces of the detent pawl teeth when the detent is engaged so that the carriage will not waver during a read/write operation.

B. -Active Detent Out (High)

When this line is active its signal enables the actuator logic to pull the detent out.

C. +Forward Speed Decode Enable and +Reverse Speed Decode Enable (Both Low)

Each of these two lines serve to partially enable the AND gates in their respective sections of the speed decode network.

D. +Detent In (High)

When this line is active its high output indicates to the seek gating logic that the detent is in.

E. -Detent In (Low)

When this line is active, it prevents AND gate A25-3C (in the clock generator) from sending a -detent speed enable to the speed decode network.

In addition to the seven output lines, the detent logic board has five input lines. Static state logic levels are identified for these lines also.

A. -Forward Velocity (High)

This line, coming from the tachometer amplifier, partially enables the set input to the detent latch and provides a high into the reset input of the reverse hold latch when there is no carriage velocity, or when the carriage is moving forward.

B. +K6 Drive (High)

When this line is high (indicating that there is power applied to the positioning motor), it partially enables the set input to the detent latch, partially enables the AND gate which generates the -active detent out signal and feeds a high into the reset input of the detent latch.

C. +Seek Enable (Low)

This line, coming from the home logic, partially enables the AND gate which resets the detent latch and generates the -active detent out signal.

D. -Reverse (High)

A low on this line is inverted to become the +reverse speed decode enable. It also serves as the single set input to the reverse hold latch.

E. +Forward to Servo (Low)

Either a -slow forward signal from the home logic or a -forward up count enable from the seek forward/reverse card will be inverted by an OR gate to become +forward to servo. The detent logic delays this signal long enough for the detent to be disengaged and then converts it to a +forward speed decode enable which partially enables the forward half of the speed decode network.

Before a seek is initiated, the detent pawl is engaged, the carriage is not moving, +K6 drive is high, +seek enable is low, -forward velocity is high and the detent latch is set. At that time, +detent in is high, -detent in is low and -active detent out is high.

When a seek is initiated by the controller, or during sequence 2 of power up or restore, the +seek enable line goes high. Since +K6 drive is also high (indicating that power is supplied to the motor), AND gate B25-1D will make, causing -active detent out to go low. If it is a forward seek, -active detent out will reset the detent latch as soon as the carriage begins to move and tachometer output (greater than 50 mv) causes -forward velocity to go low. The latch will remain reset until the detent engages and stops forward motion of the carriage.

On a reverse seek, -reverse is low, which sets the reverse hold latch (reverse hold latch is reset at all other times). The reset output of this latch disables AND gate B25-4B, allowing -active detent out to reset the detent latch. When compare is reached on a reverse seek, -reverse goes high. The reverse hold latch is ready to be reset as soon as -forward velocity goes low. Compare also causes +seek enable to go low. This causes -active detent out to go high so that the detent latch can be set when B25-4B is enabled again after being disabled by -forward velocity going low. Minus forward velocity goes low after the carriage passes through zero velocity during turnaround and begins to move forward. When it goes low, it resets the reverse hold latch which provides a partial enable to B25-4B. However, the low on -forward velocity keeps this gate disabled until the detent engages and forward motion of the carriage stops. Then -forward velocity goes high, completes the AND gate and sets the detent latch. When the detent latch sets, +detent in goes high, indicating that the detent is engaged.

The active detent out signal is also collector ORed with -force count to set the transducer enable latch (refer to the Index and Cylinder Pulse Detection logic diagram). The low on -active detent out also goes to the actuator logic and driver board, A26. Refer to the Detent Actuator Logic section below for a discussion of the effect -active detent out has on the detent actuator.

DETENT ACTUATOR LOGIC

The -active detent out, entering the actuator logic board A25 on pin B, goes low when a seek is initiated and is inverted to a high signal by A25-1C. This high output turns on the holding current transistor which provides holding current for the detent actuator. The purpose of this holding current is to keep the detent pawl out away from the rack during a seek operation. This high output from 1C also goes to inverter 2C. The output of 2C goes low into inverter 2B, whose output starts going high. However, the capacitor on 2B's output line delays this high-going signal for approximately 3 ms. For this 3-ms period the input to inverter 2A is low and its output attempts to go high. The output of inverter 2A is collector ANDed with the output of inverter 2D. The input to inverter 2D comes from inverter 2C and is at this point low. Since both inverters have low inputs, the collector AND is satisfied and the line goes high. This turns on the transistor which provides pick current for the detent actuator; the detent pawl is pulled out from the rack and held in that position. After the 3-ms delay times out, the input to inverter 2A goes high and its output goes low. The collector AND is broken so there is a low signal into the pick transistor. This turns off the pick current transistor.

When the -seek enable line goes high, indicating that a seek is not in progress, the output of 1C will go low. This turns off holding current and goes to inverter 1D. Its output attempts to go high but is collector ANDed with 1A. The input to 1A is from another 3-ms delay and will be low for that period. During this time, the collector AND is satisfied and provides a 3-ms long actuator drive signal to drop the detent into the rack. Holding current is not necessary for this period because the detent spring provides the necessary holding force.

POWER UP SEQUENCE

When START is selected with the START-STOP switch, -power up reset from C04-B (at K7) is tied to ground for 45 seconds. During this period, -power up reset sets the first seek latch and provides a low at A04-E (which clears the CAR, present address register/ counter and head address register via C10-K, C10-H and C10-P).

Following the 45-second delay, -power up reset goes high and -first seek enable goes, and remains, low. This low provides drive to K6 via A04-N. K6, in turn, relays power to the positioner motor.

When -first seek enable goes low, it enables A04-4B, which initiates Sequence 1.

Sequence 1

- Enabling of A04-4B initiates an 800-msec delay during which +seek enable (A04-M) goes high and -slow forward (A04-H) and -force difference (A04-L) go low.
- A high +seek enable to B25-F (shown in the Speed Decode and Servo logic diagram) actuates the detent.
- The low -slow forward provides a forward enable to the servo via C16-K.
- The -force difference is collector ORed with the adder output from B12-EE. This supplies a low to A15-K of the speed decode network which interprets it as a difference count of four. This simulated difference count is maintained throughout the 800-ms delay. This causes the carriage to travel forward until it comes to rest against the forward stop.
- Following the 800-ms delay, -slow forward goes high, causing a 2-ms (approximate) pulse at B24-B (high) and B24-E (low). The high signal goes to the up-down counter as a forced 204-cylinder count. The low from B24-E is collector ORed with B25-H and is sent to A26-B to prevent the detent from dropping during this period.

Sequence 2

- Following the 2 ms pulse, a 1.5 μs pulse (approximate) at B24-D sets the seek latch (A24-F). This initiates a normal 204-cylinder reverse seek.

RESTORE SEQUENCE

When the controller generates a restore command, control translation causes a -restore to set the first seek latch in A04. A high out of the first seek latch initiates sequence 1, which is followed by sequence 2. These sequences are identical to those in the power up description.

SEEK INCOMPLETE

The seek incomplete latch, as shown in the Access Control logic diagram, is normally set. When a seek other than first seek or restore is initiated, there is a high on -first seek or restore. When the detent is pulled, +detent goes low. The low is inverted and combines with the high -first seek or restore to enable AND gate C09-1C. The low out of 1C is prevented for 300 ms from resetting the seek incomplete latch. If the detent engages before the delay times out, the latch will not be reset. If the +detent line is still low after 300 ms, the latch is reset. Its reset output, +seek incomplete, causes a selected unit seek incomplete signal to be sent to the controller and the seek incomplete indicator on the operator control panel to light. The set output, -seek incomplete, disables the detent speed enable logic and causes attention to be sent to the controller.

The seek incomplete latch is set again by a low on the -first seek/restore line. This will occur if the controller initiates a restore operation or if the operator selects STOP and then START on the START-STOP switch. This procedure would cause the drive to go through a first seek sequence, setting the seek incomplete latch.

If an invalid address (greater than 202) is entered into the cylinder address register, the cylinder transducer will run out of rack teeth to detect before the invalid address can be reached. This means a compare condition will not be reached; consequently, the detent will not engage. When the seek incomplete delay times out, a seek incomplete condition is generated.

A line labeled -seek ready goes to the controller via the status logic and indicates a ready condition, implies that a seek has been completed and that the drive is ready to perform another seek, read or write operation. If the detent is in (+detent is high) and if a seek start condition has not been selected by the controller (-select seek start is high), -seek ready will be low.

A -seek ready, inverted by OR gate C09-3A is one of three conditions which will cause a -attention signal to be generated. A -seek incomplete from the set output of the seek incomplete latch also provides a -attention signal to the status logic. This would indicate either an incomplete seek or an invalid address.

ATTENTION, DELTA ATTENTION AND ON LINE LATCHES

During the pack warm up period of the power up sequence, the low on +K6 drive holds the on line latch reset. At that time, the set output, +gated on line, will be low and will set the delta attention latch. The high out of delta attention can then partially enable AND gate C10-1C. However, the low on +gated on line disables C10-1C. The high from C10-1C and the high on -select seek start to the set input of the attention latch and the low on -power up reset into the reset input hold the attention latch reset.

After the warm up period, -power up reset and +K6 drive go high, removing the reset inputs to the on line and attention latches. A first seek is then initiated. At the beginning of the first seek, +K6 drive has no effect on the on line latch, which remains reset since -seek ready is still high. The high on -power up reset has no effect on the attention latch since +gated on line is still low and -select seek start is still high.

When the first seek is completed, the detent engages (+detent into C09-C goes high) and -seek ready goes low (following 2-1/2 ms damping delay). This sets the on line latch. Now +gated on line is high. It is collector ANDed with an inverted -enable latch on and completes

AND gate C10-1C (set output of the delta attention latch is still high). The low out of C10-1C sets the attention latch. This partially enables AND gate C10-2C. Since +detent and -select seek start are high at this time, C10-2C is satisfied and a -attention signal is sent to the controller via a status network line driver.

Whenever the read mode is selected by the controller, bus line 1, the control tag line and the select unit line combine to generate a -reset attention signal (see the Control Translation logic diagram). This signal resets the delta attention and attention latches.

SEEK ENABLE AND COUNT LOGIC

The purpose of this logic is to convert output from the null detector to forward and reverse count enables to the counter, a forward gating enable to the adder, a forward enable to the servo and count pulses to the counter.

A low from the reset side of the seek latch will combine with the signal on the +carry line. If the +carry line is low, a +forward is generated; if the +carry line is high, a +reverse is generated. The high +forward is inverted to provide a -forward up count enable to the counter and the high +reverse is inverted to provide a -reverse down count enable to the counter.

The uninverted +forward partially enables a pair of AND gates. One of the gates is responsible for generating a forward count pulse to be sent to the counter logic. The other three inputs to this AND gate require a high on the +strobe line, a low (to be inverted) on the -null line and a high on the -delayed null line. Refer to the Index and Cylinder Pulse Detection logic diagram for a discussion of the strobe, null and delayed null lines. The other AND gate fed by the +forward line supplies a compare pulse to reset the seek latch. This occurs at the time compare is reached and a strobe pulse is received from the clock generator during a forward seek.

The uninverted +reverse partially enables a similar pair of AND gates. A high +reverse will combine with a high on the +strobe and -null lines and a low (to be inverted) on the -delayed null line to generate a reverse count pulse to the counter logic. The other AND gate fed by the +reverse line supplies a compare pulse to reset the seek latch. This occurs at the time compare is reached and a strobe pulse is received from the clock generator at the end of a reverse seek.

UP SPEED DETECTION

With the disc pack installed and the cabinet cover closed, the aluminum sector disc separates the permanent magnet and coil of the index/sector transducer. Before the disc begins moving, there is no current in the coil and the aluminum disc interrupts the magnet's flux field. When the disc is rotating, slots will periodically pass between the magnet and coil. Each time this happens, the flux field will expand through the slot and surround the coil, inducing a current in the coil. When the slot passes by, the flux field collapses, reversing the current in the coil. Output from the coil appears as a single dipulse for each slot. There are 20 evenly spaced slots (sector slots) around the periphery of the disc. Another slot, close to one of the sector slots, marks index for the disc pack.

The transducer comparator card converts the induced coil waveform output to positive-going sector and index pulses. Each revolution of the disc produces 20 sector pulses and 1 index pulse. These pulses are then transferred directly to input pin B on the up speed detector card A23.

The logic on A23 has two primary responsibilities: (1) to discriminate between sector and index pulses, (2) to determine whether disc pack rotation is above or below minimum operating speed (70% ±10% of 2400 rpm).

A. Index/Sector Separation

A23 discriminates between sector and index pulses so that they may be sent to the controller on separate lines. These signals are used by the controller for synchronizing data transmission between the drive and itself. Pulses identified as sector pulses leave card A23 on pin K as -sector signals. They occur whenever AND gate A23-4A receives a pulse from +sector/index line while JK flip-flop 5A is reset. Since the Q output of 5A is tied back through a delay to its own direct reset input, setting 5A will cause the flip-flop to reset itself following a 300 μs delay. 5A will always be in the reset state from the time the delay ends until the trailing edge of the next clock pulse (a high signal on the + sector/index line) sets the flip-flop. Distinguishing index pulses from sector pulses relies on the spacing of the slots on the sector disc and the duration of the 5A delay. The sector slots are spaced far enough apart that the 300 μs delay always times out before the next sector slot reaches the index transducer regardless of disc pack speed. However, the index slot follows one of the sector slots so closely that it always generates a pulse in the transducer before the 300 μs delay can time out, regardless of disc pack speed.

Since 5A is in the reset state as each sector pulse reaches AND gate 4A, that gate is enabled, generating a -sector signal to pin K. The index slot does not enable 4A because the $\overline{Q}$ line from 5A is low when the index pulse reaches gate 4A. Instead, the pulse from the index/sector line is ANDed with the Q output of 5A at gate 4B. The output of 4B leaves the board at pin C as -index. This signal is also inverted by 4D to become +index. The signal +index leaves the board on pin D. It is also used by the up speed portion of the A23 logic.

B. Up Speed Detection (see Timing Diagram in Section 2.3.4)

A23 logic determines whether disc pack speed has reached minimum operating speed (70% ±10% of 2400 rpm). This is based on how much time there is between the arrival of +index pulses. During disc pack acceleration, the interval between the +index pulses decreases until it is less than a time constant provided by the up-speed timing logic. This constant, or up speed reference, is derived from two 35 ms delays, which are used in conjunction with two AND gates (3B and 3C), one JK flip-flop (5B) and two D-type flip-flops (1A and 1B).

The +index pulse is used as the clock pulse for JK flip-flop 5B to partially enable AND gates 3B and 3C. The Q and $\overline{Q}$ outputs of 5B are the other inputs to 3B and 3C, respectively. The outputs of AND gates 3B and 3C are used to clock their respective flip-flops (1A and 1B). The Q and $\overline{Q}$ outputs of 5B also go to inverters 3A and 3D, respectively. The outputs of inverters 3A and 3D are each sent through separate 35 ms delays. The two delays generate signals which are used as the D and R_D inputs of D-type flip-flops 1A and 1B. Since the Q output of 5B is tied back to its K input and the $\overline{Q}$ output is tied back to the J input, 5B toggles with each clock pulse (+index).

The signal -up speed is generated when flip-flops 1A and 1B are in the set state together, providing two high inputs to AND gate 2B. When the disc pack begins rotating, the trailing edge of each +index pulse causes 5B to change state. If 5B sets, its Q output partially enables 3B. That gate is not completed however, because 5B did not set until the trailing edge of the pulse. Consequently, the Q output lagged behind the + index input to 3B. Instead, AND gate 3C is enabled because +index arrived while 5B was still reset. $\overline{Q}$ and +index enabled 3C, providing a clock input to 1B. This clock pulse has no effect on 1B because the R_D input to 1B is low at this time, which holds 1B reset. The next +index pulse enables 3B before it resets 5B, providing a clock pulse to flip-flop 1A. The clock pulse does not set 1A, however, because the R_D input to 1A is low as a result of 5B being set by the last +index pulse. When 5B resets on the trailing edge of +index, the R_D input to 1A goes high. 35 ms after 5B resets and $\overline{Q}$ goes high, the R_D input to 1B goes low, resetting that flip-flop. Flip-flop 5B continues to toggle with each +index pulse without setting either 1A or 1B; the 35 ms delays time out and allow the R_D inputs to each flip-flop to go low before the next +index pulse is able to provide a clock pulse. The first time the interval between +index pulses is less than 35 ms, one of the flip-flops (1A or 1B) is set. If the next +index pulse arrives less than 35 ms later, the other flip-flop is set in the same manner. With 1A and 1B set at the same time, their Q outputs enable AND gate 2B, providing the signal -up speed.

CYLINDER TRANSDUCER

Output from a 150 KHz oscillator induces voltage in the transducer's secondary coils through the rack teeth closest to the two coils. This induced voltage is modulated as the level of coupling between the primary coil and secondary coils varies with the movement of rack teeth past the coils during a seek.

The secondary frequency envelope is fed into a dual comparator circuit which has two thresholds, 100 and 175 mv from ground. The lower threshold represents the maximum voltage acceptable for a null condition and the upper threshold is the minimum voltage allowable for a peak. The 75 mv difference between the two levels provides a clear distinction between peaks and nulls.

The amplified dc reference and transducer output voltages are then fed into a pair of AND gates (one for lower and one for upper reference levels). These gates convert both reference levels to ground (low standard logic level) and shape the reference transducer outputs to nearly rectangular waves with peaks of +5 volts (high standard logic level). A transducer enable line is high and enables both gates when the -active detent line is low and -gated attention is high. This condition exists from the time a seek starts until attention is signaled to the controller.

Both upper and lower (peak and null)pulses are sent to their respective logic sections of the null detector card, B22. There, they are ANDed with negative going strobe pulses which are sent from the clock generator card, A25.

These strobe pulses, are produced by a clock generator which is fed by the same oscillator that supplies the cylinder transducer. The clock generator amplifies and shapes its input to negative going pulses 1 μs wide at the standard logic levels of 0 (low) and +5v (high).

The primary responsibility of the null detector logic is to synchronize count pulses so that the carriage is in the same position when the count pulse is generated whether the carriage is moving forward or reverse. Consider the transducer output represented in the curve below. Each cycle on the curve is analogous to a rack tooth. Since the same side of a tooth must always serve as the reference surface for the cylinder counts for both forward and reverse seeks, the same slope of each cycle on the curve must initiate count pulses, both forward and reverse.

The count pulse logic on A24 takes advantage of the fact that the reference slope is approached from one direction during a forward seek and from the other direction during a reverse seek by requiring that a pair of latches in the null detector logic be set and reset during a forward seek and reset and set (respectively) during a reverse seek. The forward relationship between the latches is caused by a peak-to-null approach to the slope. The reverse relationship is caused by a null-to-peak approach. During forward travel, the

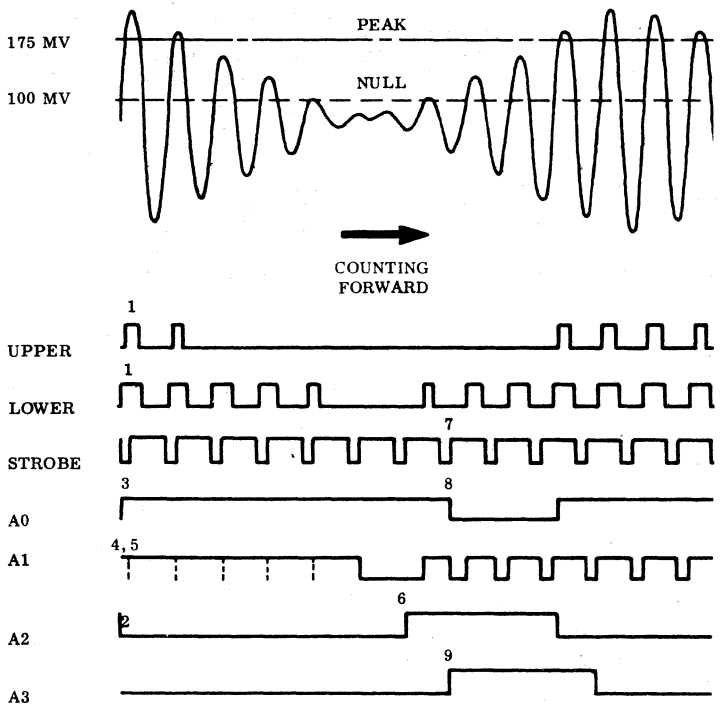
carriage must travel through a peak condition in the transducer and then transfer to a null condition; a forward count pulse is generated with the trailing edge of the next strobe pulse. Conversely, during reverse travel, the carriage must travel through a null condition and then transfer to a peak condition; a reverse count pulse is generated with the trailing edge of the next strobe pulse.

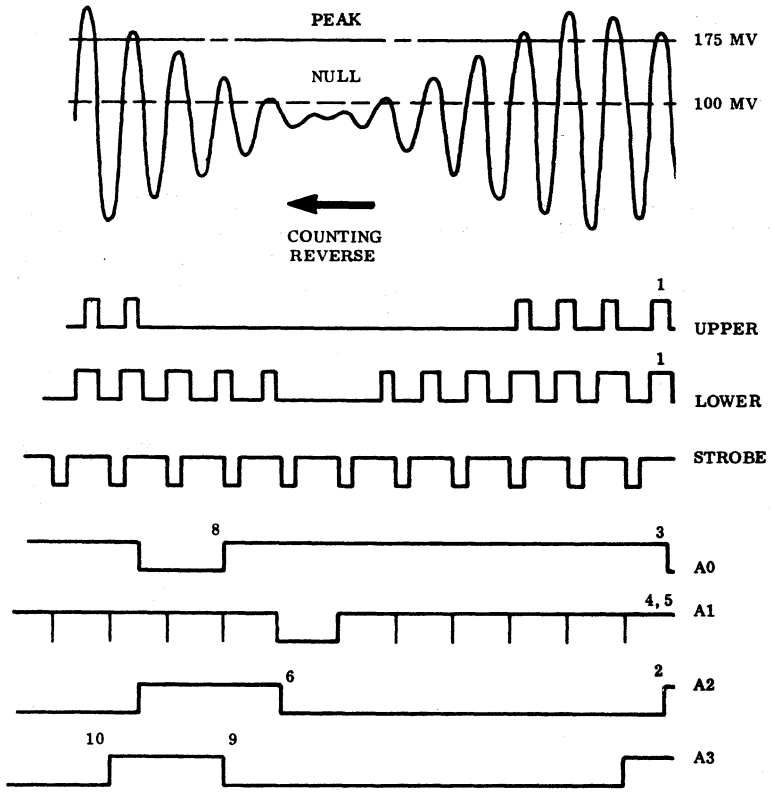
When the rack begins to move at the start of a seek, a peak will be sensed by the comparator (i.e., an induced voltage whose peak-to-peak amplitude exceeds 350 mv; this is twice the upper threshold of 175 mv). As a result, both the line labeled lower and the line labeled upper will be high (Note 1 in the timing diagram below). While these are high and there is no strobe pulse (-strobe is high), AND gate B22-4B makes. Its low output is inverted to a high which ANDs with the high on upper to make B22-4A. The low out of 4A is inverted by B22-3A and resets A2, the null latch (Note 2). There is no clock pulse into A2 at this time because the clock input for all the JK's is an inverted -strobe pulse; the -strobe line is high. The high out of the reset A2 ANDs with the high out of 3B and the high on the upper line at B22-5A. Output of 5A is inverted by B22-3A and sets A0, the peak latch (Note 3).

A1, the sample latch, is set and remains set during the period the lower line is active (high) and the -strobe line is high (producing a high out of B22-3B; Note 4). It will reset momentarily at those times when the clock pulses happen to arrive when the lower line is low. It will set again if the lower line goes high before the next clock pulse (Note 5). When the lower line goes, and remains low, A1 will stay reset. This initiates a sequence of events that will set the null latch and reset the peak latch.

When A1 is reset, its reset output is high. This ANDs with the high out of the set peak latch to provide a high into the set input of A2 (via B22-4C and 3D). The trailing edge of the next clock pulse sets A2 (Note 6). The low out of the reset side of A2 goes to board A24 and partially enables the forward count logic (refer to the Access Control logic diagram). If the carriage is performing a forward seek, the count logic will be enabled and a count pulse will be generated with the next strobe (Note 7). The high out of the set side of A2 goes to the reset input of the peak latch so that the next clock pulse resets A0 (Note 8). A0 remains reset until the next time both the upper and lower lines go high.

If the carriage is performing a reverse seek, the forward count pulse logic will not be enabled. A high on the +carry line (this line is high during reverse seeks) disables the forward count pulse logic while partiallv enabling the reverse count pulse logic. This logic is waiting for the transition from a null to a peak. This is represented by A3 being set and A2 reset. The next clock pulse will set A3 with direct input from A2 (Note 9). Some time later, a peak will be detected (lower and upper lines will be high) which will reset A2 (Note 10). The high out of the reset side of A2 and the low out of the reset side of A3 complete the reverse count logic on A24, generating a reverse count. Since the count logic had to wait for the transition from null to peak, the rack and carriage were in the same position they would have been in for a forward count to be generated during a forward seek.





READ/WRITE ENABLE AND READY LAMP DRIVERS

The primary purpose of the read/write enable synchronizer card, B04, is to prevent switching of read/write and on line states while the CPU is running.

If ENABLE is selected on the ENABLE-DISABLE switch while the CPU is not running (-clock out is high) and the unit is not selected (-unit select is high), the enable latch will set. When -clock out goes low again, the enable latch will be unaffected by the ENABLE-DISABLE switch. By the same logic, the latch cannot be switched from reset to set while -clock out is high.

A low -unit select line will also prevent resetting a set latch; however, it will not prevent the latch from setting.

The read only latch is restricted by -clock out in the same way as the enable latch. It cannot be toggled whenever -clock out is low. It is also true that the read only state cannot be deselected while the unit is selected (-unit select is low). This assures that a write operation will not be terminated prematurely.

The standard Model 630 is equipped with a running time meter. That is, the meter records operating time whenever the spindle is up to speed. If the revenue meter option has been installed, the meter will operate only while the CPU is running, +gated on line is high (refer to the Access Control logic diagram) and there is no file unsafe condition present. During that time, AND gate B04-2B will be complete. Its low out is inverted to a +revenue meter. This serves as the enabling line to the meter relay, B01.

The READY lamps behind the operator control panel will only light when there is drive to the positioning motor (+K6 drive is high), a first seek is not in progress (-first seek is high) and a seek incomplete condition does not exist (-seek incomplete is high).

READ/WRITE

The head switch drivers, which are on the double board A/B 18, receive their inputs from the head switch decode network shown in the Control Translation logic diagram. A low on any one of these lines selects the head switch driver on that line. There should be only one line low at a time. Another input to each driver comes from A/B 14, the read/write enable. When the common line from A/B 14-L, labeled -head deselected is high, it is considered an enable line to the drivers. In a file unsafe condition, this line goes low and clamps all of the head switch drivers so that no head can be enabled.

Outputs of the drivers go to a cable run to the top deck via a paddle board. There they are connected to the read and write amplifier boards. Head wires plug into connectors on the read and write boards.

The select write gate output is received by A06-1A (pin Q). It goes to the paddle board B28 and through the cable run to the top deck to the direct reset input of the write JK flip-flop. When write gate is selected, this line goes low and removes the direct reset from the flip-flop. Write data comes through the line terminator and coax receiver into the clock input in this flip-flop. The flip-flop is toggled by each write data pulse; its outputs feed the write amplifier. The select write gate enable also goes through inverter A06-1A into the write enable and current driver. The write driver enable goes through the cable run into the write amplifier. Another output goes to the read amplifier and disables the read preamp during a write operation. The controller must also select erase to provide tunnel erase current during the write operation. Isolation diodes are in series with each head lead so that only the selected head will have a complete pass for write and erase current flow.

Isolation diodes in the read amplifier block write or erase current flow through it. The output of the read amplifier goes to a read shaper coax drive board and out of the drive on the read data coax to the controller. No decoding or clock sensing is performed since the data was written to be self-clocking. Read data is simply amplified and shaped and fed serially to the controller.

STATUS AND SIGNAL OUTPUT LINES

LINE DRIVERS

The line drivers send the contents of the CAR and control signals to the controller. These drivers require a high logic level input (+5 vdc); their output, when active, is low. Contents of the CAR remain on the lines when the unit is selected. The line drivers are gated by inverters C11-1B and C11-1A via a collector AND gate. A -unit selected partially enables this collector AND; the other input is from the initial seek latch. This latch is set by a first seek operation during the power-up sequence or any restore operation from the controller. Either of these conditions will disable the line drivers and remove the CAR contents from the lines until the first select set cylinder command comes from the controller. Select set cylinder resets the initial seek latch and enables the line drivers.

STATUS LINES

The selected unit file unsafe line, shown leaving the unit at J3, pin 57, is enabled by a file unsafe condition and select unit. The unit selected line, which leaves the unit at J5, pin 21, receives its input from select unit; this is shown as line 1 in the Control Translation logic diagram. The -selected unit seek incomplete line is generated by a collector AND from inverters C12-3B and 3C. The 3C input is from select unit; 3B input from -seek incomplete. The selected unit read only, selected unit on-line, selected unit index pulse and selected unit write current sense lines are all generated in the same manner, that is, by combining select unit with the individual function line. Three of the status lines: selected unit end of cylinder, attention and selected unit ready are not combined with select unit at this point but earlier in the logic.

UNSAFE SENSING

Inverters B05-1A and 1B supply a -heads unsafe signal to the heads unsafe latch. One resistor and one isolation diode are connected to the output of each head select driver. This makes a current summing network similar to that used in the speed decode. Selection of one head will not generate enough current and voltage to pass the threshold of the first inverter, B05-1A. However, any two or more heads selected simultaneously or one head selected with a condition of seek not ready will generate enough voltage to activate B05-1A. Its output will go high, causing a low output from 1B, labeled -heads unsafe. This low output is fed back to the current summing network assuring that both inverters stay locked in the heads unsafe condition. The -heads unsafe line goes to the heads unsafe latch, C15-2B and 2A.

The reset output of this latch serves as one of five inputs to OR gate C15-3B. The other four inputs include: -selected unsafe, -write and/or erase unsafe, -dc voltage unsafe (in on pin N) and -ac voltage unsafe (in on pin M and through a diode). Any one of these inputs going low will generate a high out of OR gate 3B labeled +file unsafe. The +file unsafe signal is inverted by C15-3A to -file unsafe. This goes to the FILE UNSAFE light on the operator control panel through a lamp driver. It also goes to inverter C13-2B. Output of this inverter is collecter ORed with the inverted states of the -head select and ac unsafe lines. If this collector OR is satisfied, it means that one head has been selected, the file is safe and the ac circuitry is safe. If any of the inputs to the collector OR go low, the head(s) will be deselected. The -head deselect output of the collector OR goes directly to head switch drivers.

AC and dc unsafe sensing is done by voltage divider networks and inverters.

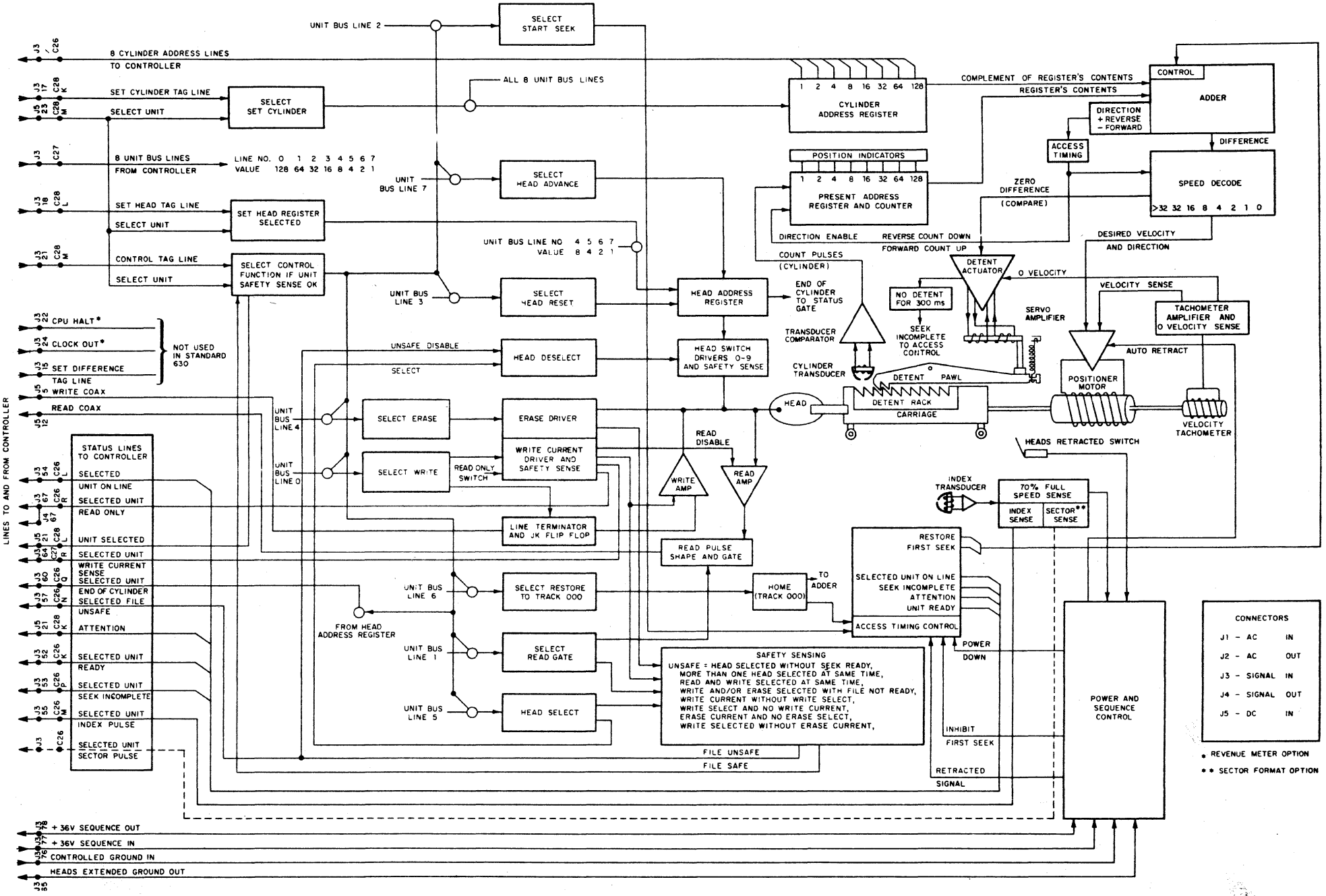
Write/erase unsafe is done with a combination of three AND gates. A fourth AND gate included in this group, C13-1D, is effectively not used since one input (pin B) is grounded. That AND gate does not take part in unsafe sensing. Inverter C13-1C combines -selected write gate and +write current. This AND is satisfied when write current is present without write gate selected. Inverter 1B combines -selected erase gate and erase current; its active output indicates the presence of erase current without the erase gate being selected. Inverter C13-1A combines selected write gate and -erase current; it indicates that write coils were selected without erase current. Outputs of these gates are combined in a collector OR. Any output going low would cause the collector OR to go low. A low into the write unsafe latch, C15-4B, would set it. Its low reset output to OR gate C15-3B would give the file unsafe condition.

The fifth input to OR gate C15-3B, -select unsafe, comes from a latch composed of three OR gates. The outputs of two OR gates are collector ANDed and tied back into the reset input of the latch. Output of this latch, -select unsafe, is active when read is selected along with either write or erase or when write or erase is selected while the unit is not ready. Input to the set side of the select unsafe latch comes from AND gates C08-1C and C08-2A through a collector OR. Input to 1C is from the -select unit line and input to 2A is -seek ready. When either 1C output or 2A output is active (low), the collector OR is satisfied and a low input is supplied to one of the six set inputs of the select unsafe latch. However, the input alone will not set the latch; outputs of OR gates C15-1A and 1B are collector ANDed. To set the latch, a low input to each of these gates is necessary.

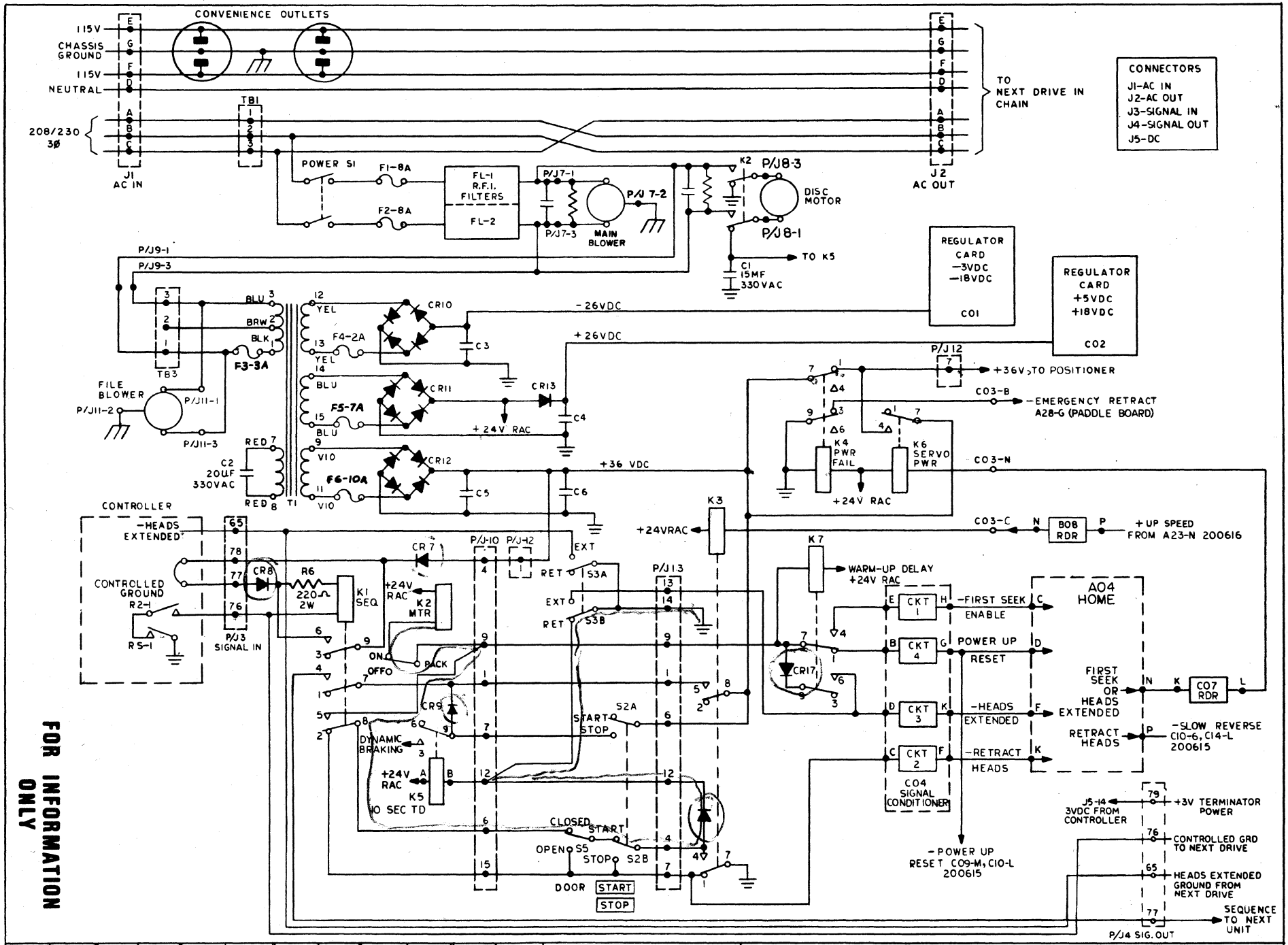
The collector logic of inverters C08-1C and 2A also goes to A06-2C on the status line labeled +unit ready. The +unit ready line regards the collector logic for those two inverters as a collector AND. Since a high level is required for this condition, both inverters must have low input. This is true when the unit is selected and a seek ready condition exists. A unit selected condition along with seek ready indicates that the unit is ready. This line is sent to status gating as +unit ready. However, if this line should go low, as it does when a seek is initiated, and at the same time either selected write gate or selected erase gate lines go low, each set term of the select unsafe latch would have a low input. The collector AND of inverters 1A and 1B would be satisfied and that line would go high. This would cause one of the three inputs to C15-1C to go high. The other two inputs are reset inputs. Their normal state can be considered high. Since that would mean all inputs to C15-1C would be high, the reset output of the select unsafe latch would be low. This output goes to C15-3B. The low output of 1C is the select unsafe condition. This latch, the select heads unsafe latch and the write/erase unsafe latch may be reset by either of two conditions:

A. -CE Reset Select Lock
This is put in as a convenience for customer engineer. If the unsafe condition exists, a customer engineer can reset or clear this unsafe condition by jumpering a ground to C15, pin B.

B. Nonintervention
Under normal operating conditions, these latches could be reset only by the output of AND gate C15-2C. Its inputs are from reset present address counter and up-speed. Up-speed indicates that a pack is on the drive, the drive is up to normal speed and the heads are loaded. The present address counter must be reset by a first seek condition, which is a consequence of a power up sequence. The first seek resulting from a power up sequence is a means of resetting the unsafe condition by operator intervention (press STOP, then START switch on operator control panel).

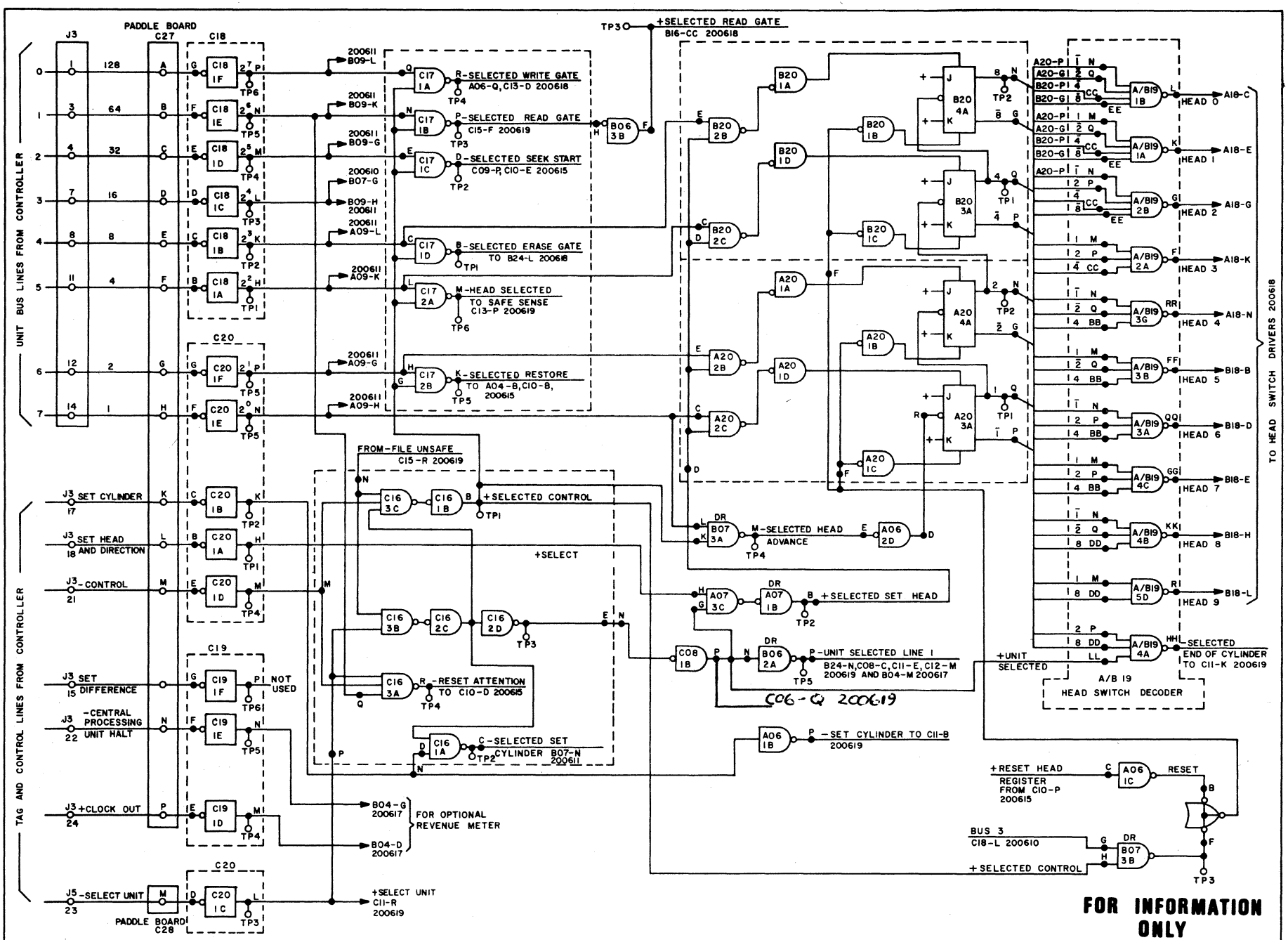


Functional Block Diagram

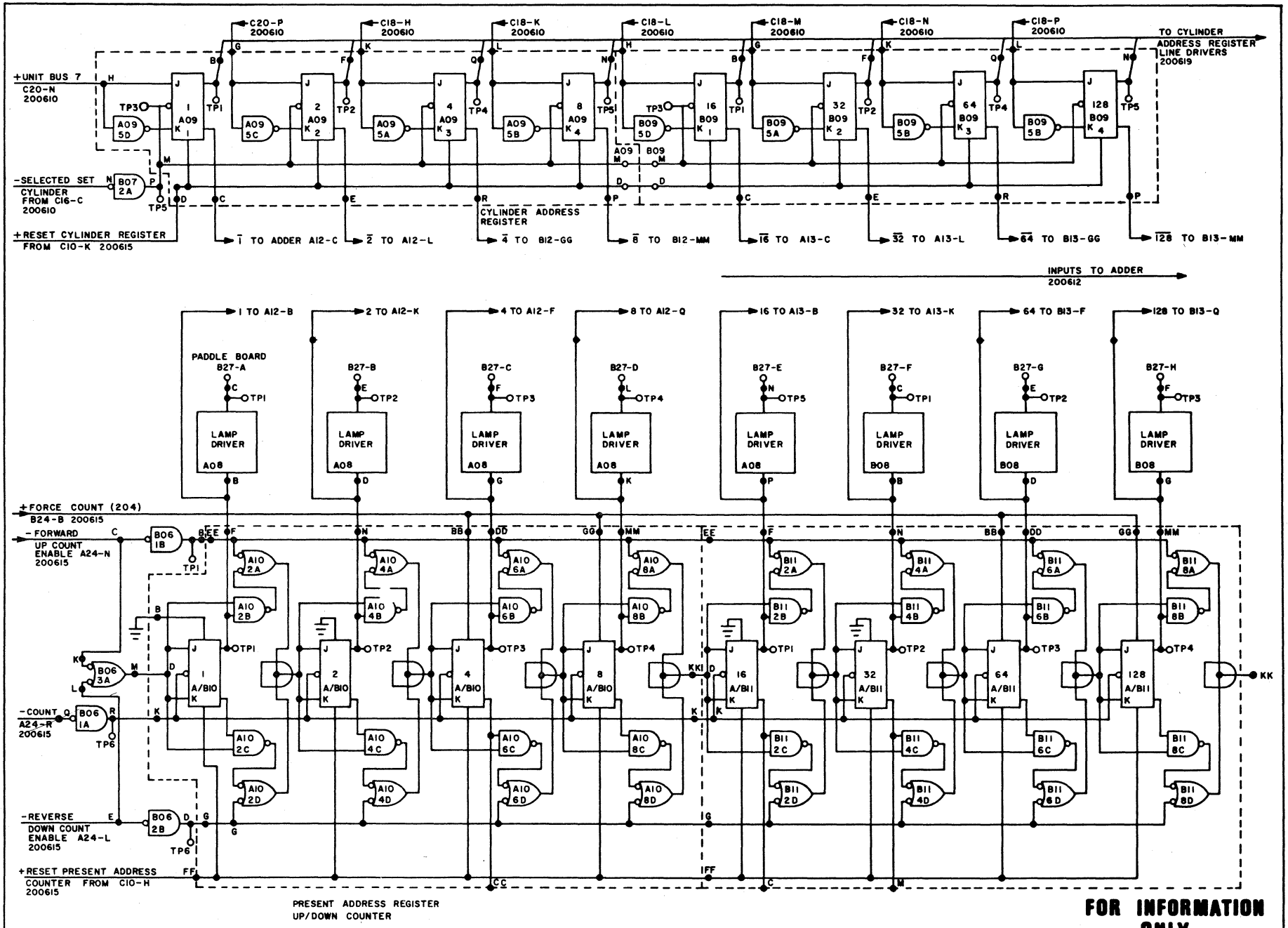


FOR INFORMATION ONLY

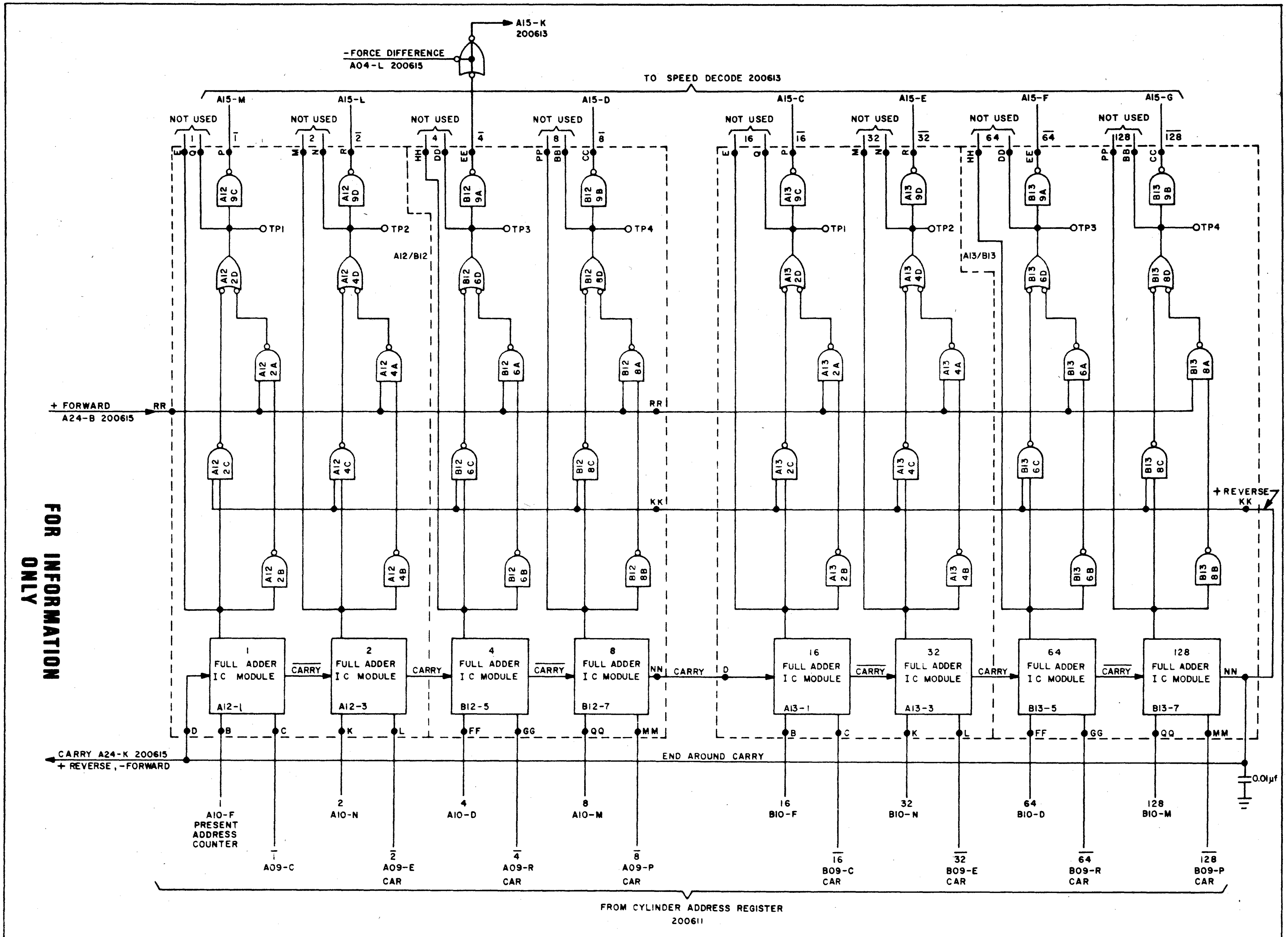
200609 | POWER UP SEQUENCE AND INTERLOCKS



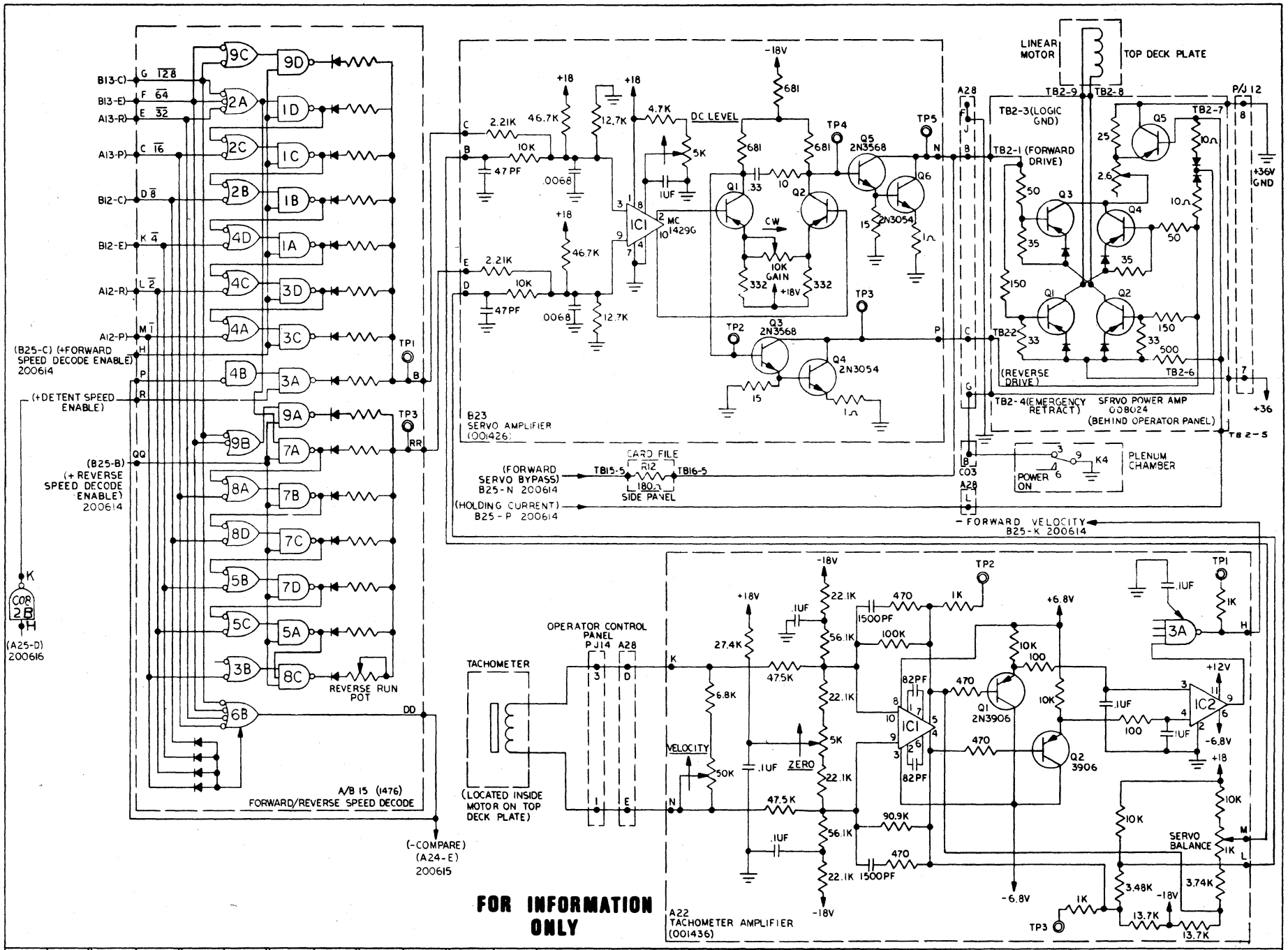
CORRECTED 04-07-69		200610	CONTROL TRANSLATION



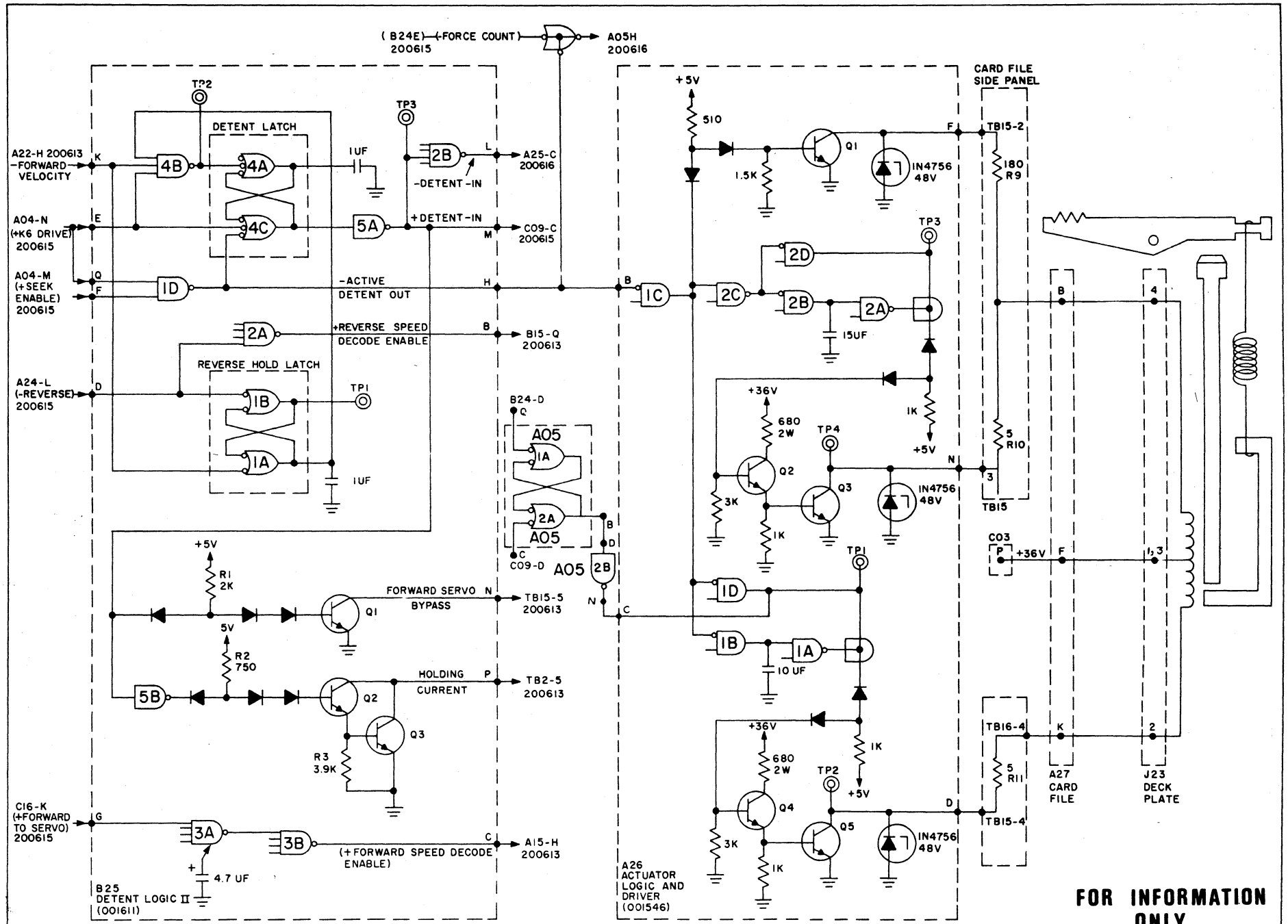
ECN 190 03-10-69 DDC	CORRECTED 04-01-69	200611	CAR & PRESENT ADDRESS REGISTER/COUNTER



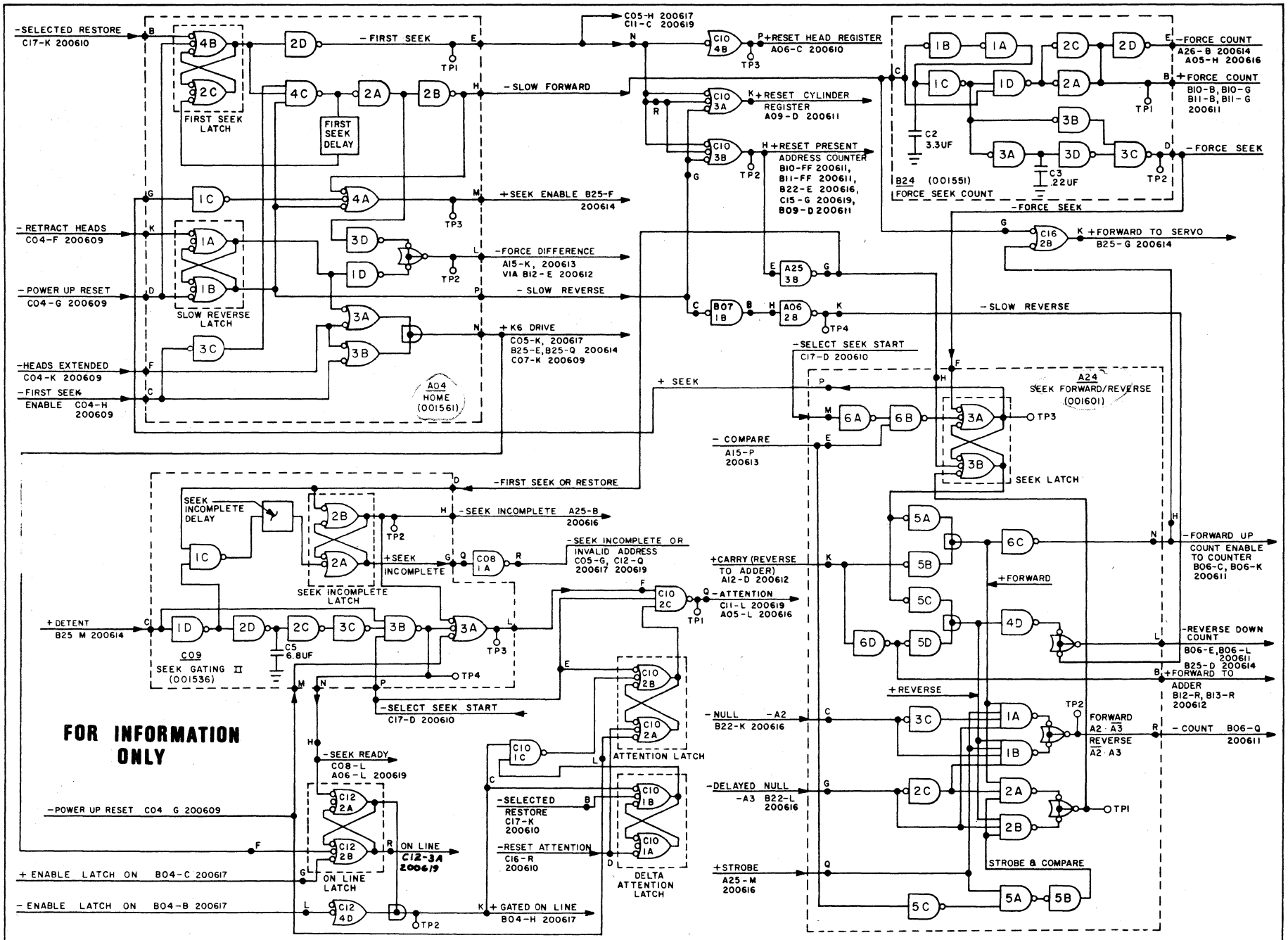
200612 ADDER



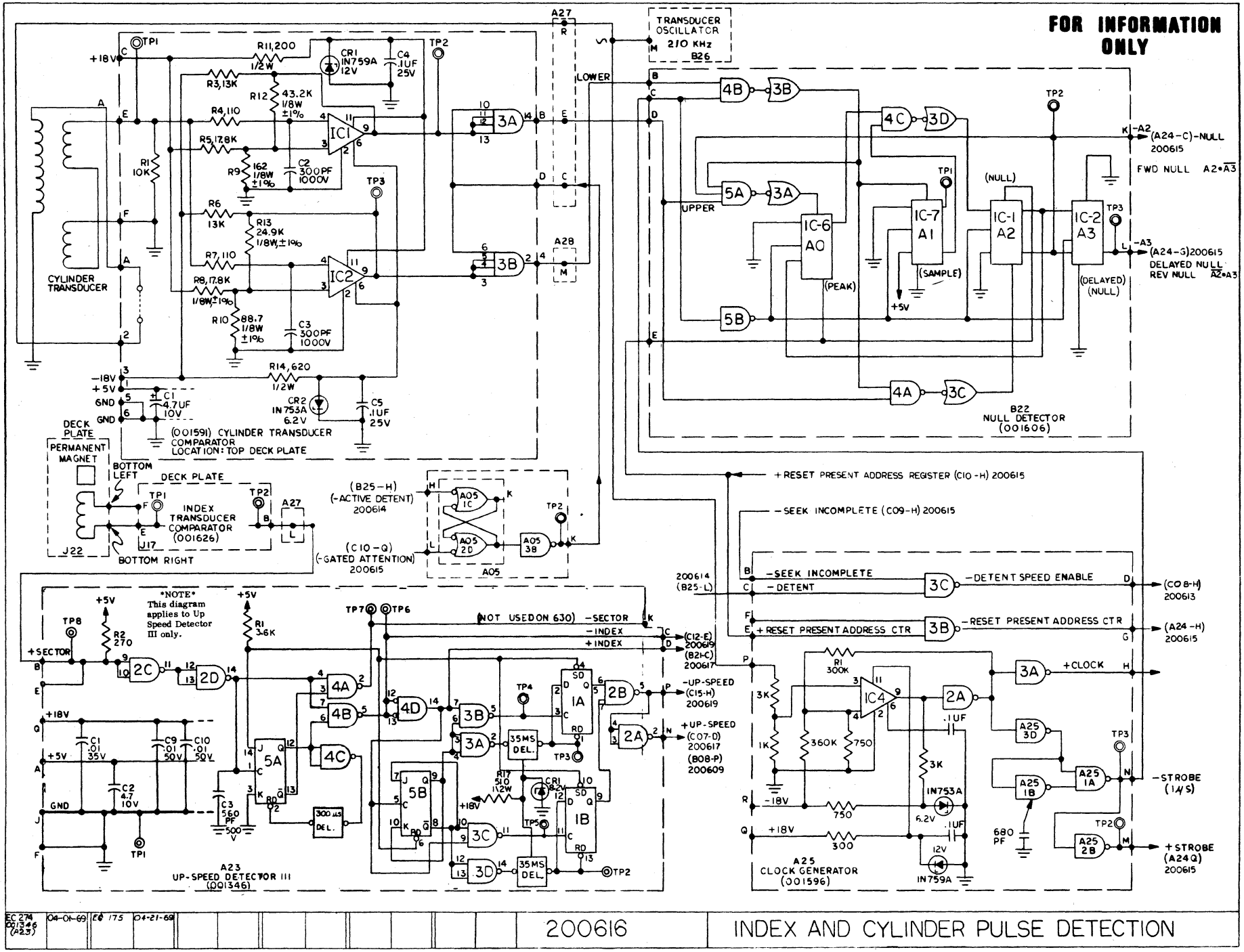
E.C.172 #1476	07-14-68	E.C.151 #1436	07-31-68	E.C.190 #1246 a&c									200613	FORWARD/REVERSE SPEED DECODE AND SERVO



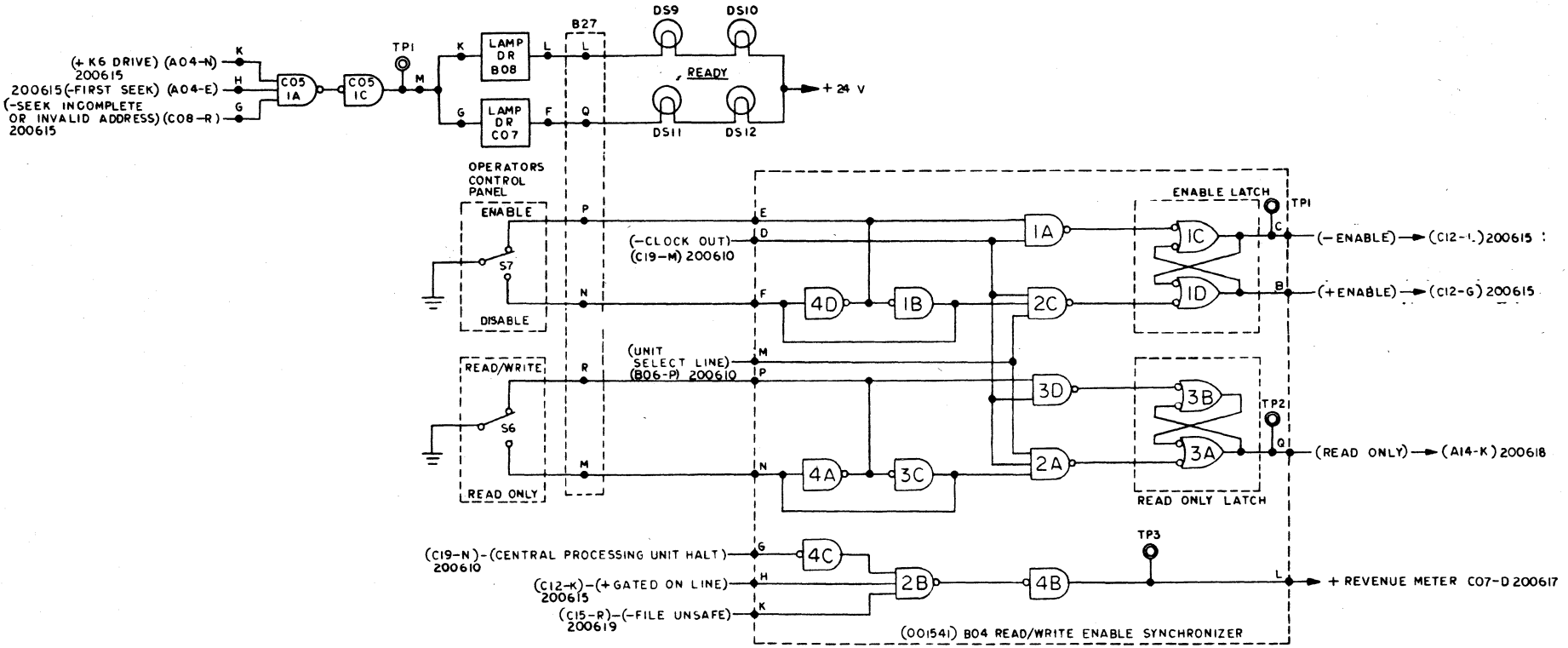
200614 | DETENT AND ACTUATOR CONTROL



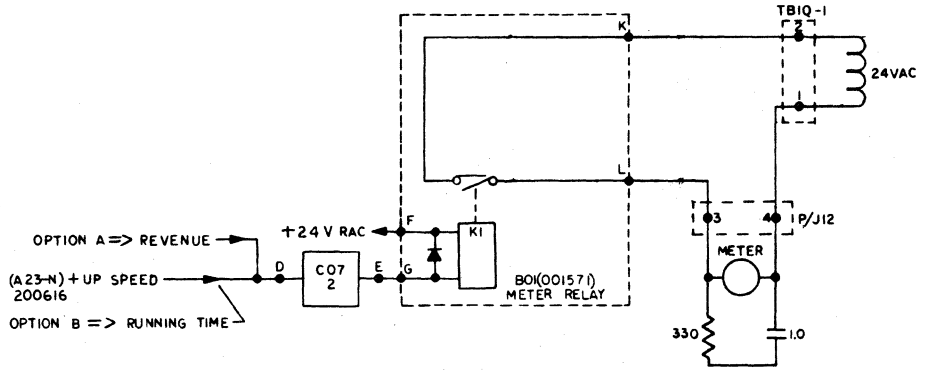
200615 ACCESS CONTROL



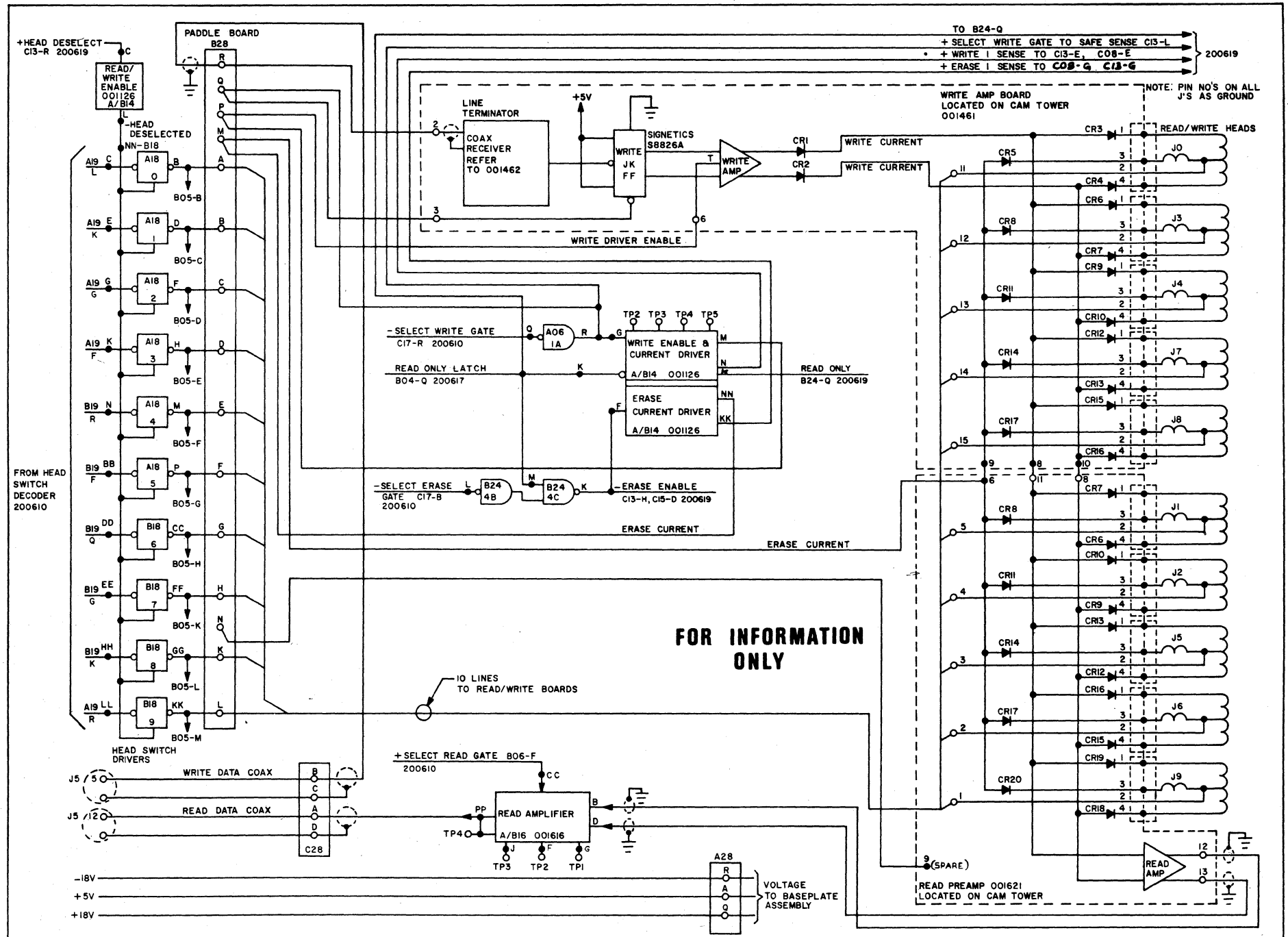
EC 274	04-01-69	EC 175	04-21-69	200616	INDEX AND CYLINDER PULSE DETECTION
001346 (A23)					



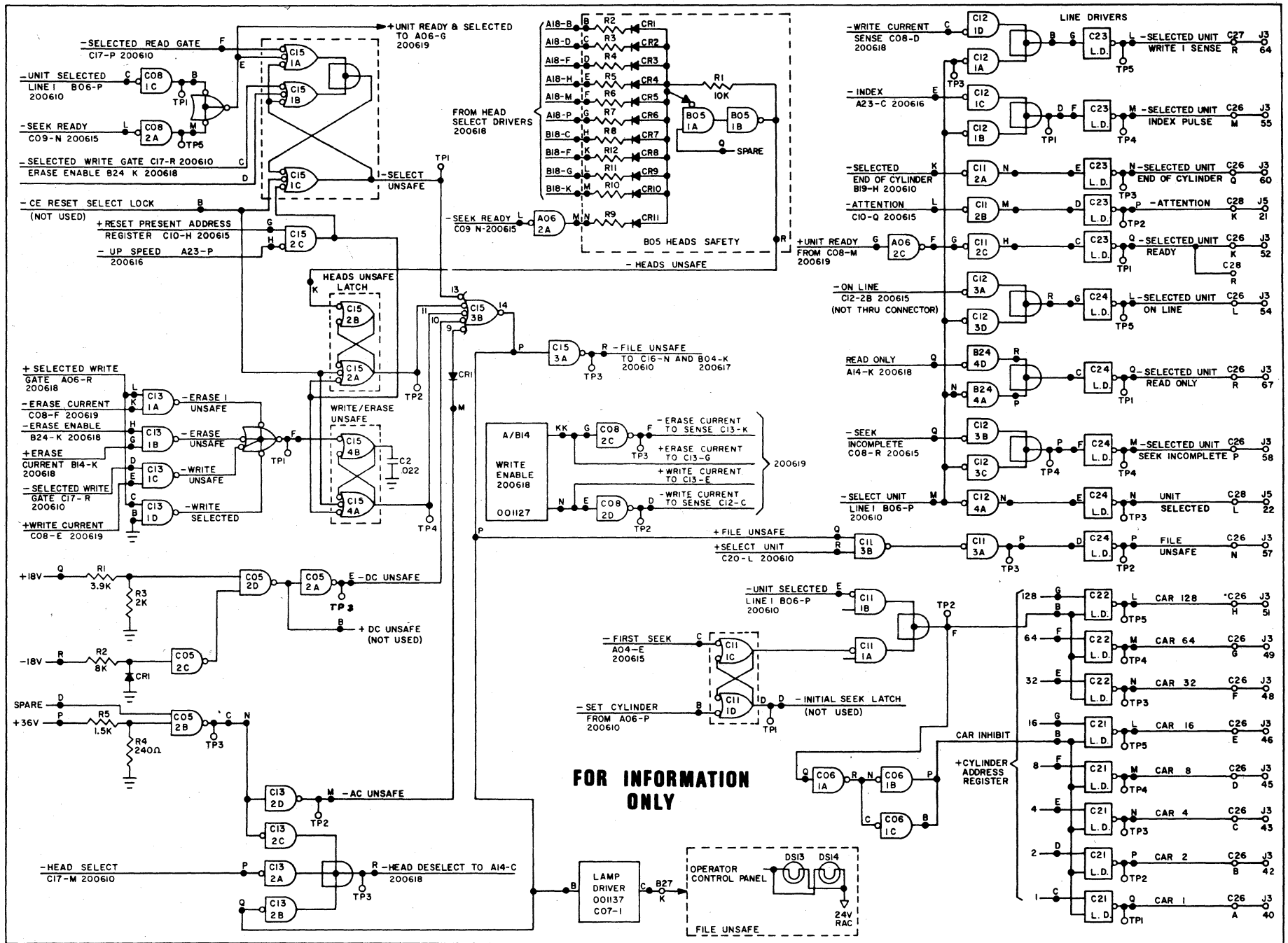
FOR INFORMATION ONLY



200617	READ WRITE ENABLE AND READY LAMP DRIVERS



E.C. 190	03-10-69											200618	READ/WRITE



200619 | STATUS AND UNSAFE SENSE

008031

BOARDS LOCATED OUTSIDE OF FILE (REFERENCE)

READ PREAMPLIFIER 001621 [1]	WRITE AMP/COAX/REC/ SELECT 001461 [1]	CYL TRANSDUCER COMP 001591 [1]
		INDEX TRANSDUCER COMP 001626 [1]

[1] FOR REFERENCE ONLY

FILE A	FILE B	FILE C	
PADDLE BOARD, SIGNAL (DRIVE CONTROL) 001371 [1]	PADDLE BOARD, SIGNAL (DRIVE HEADS) 001371 [1]	PADDLE BOARD, D.C. (DC SIGNAL OUT) 001376 [1]	28
PADDLE BOARD, SIGNAL (DRIVE CONTROL) 001371 [1]	PADDLE BOARD, SIGNAL (CYL. ADD. LAMPS) 001371 [1]	PADDLE BOARD, SIGNAL (SIGNAL IN) 001371 [1]	27
ACTUATOR LOGIC & DRIVER II 001681	TRANSDUCER OSCILLATOR 001341	PADDLE BOARD, SIGNAL (SIGNAL OUT) 001371 [1]	26
CLOCK GENERATOR 001596	DETENT LOGIC II 001611		25
SEEK FORWARD/REVERSE 001601	FORCE SEEK COUNT 001551	LINE DRIVER II 001641	24
UP-SPEED DETECTOR III 001346	SERVO AMPLIFIER 001426	LINE DRIVER II 001641	23
TACHOMETER AMPLIFIER 001436	NULL DETECTOR 001606	LINE DRIVER II 001641	22
		LINE DRIVER II 001641	21
HEAD REGISTER 001331	HEAD REGISTER 001331	TERMINATED LINE RECEIVER 001506	20
HEAD SWITCH DECODER 001191		LINE RECEIVER 001351	19
HEAD SWITCH DRIVER 001131		LINE RECEIVER 001351	18
		CONTROL GATING 001401	17
READ AMPLIFIER 001616		SELECT GATING 001411	16
FWD/REV SPEED DECODER 001476		CONTROL SAFETY 001386	15
READ/WRITE ENABLE 001126			14
ADDER 001196		WRITE/ERASE SAFETY 001381	13
ADDER 001196		STATUS GATING II 001556	12
UP-DOWN COUNTER 001186		CYLINDER ADDRESS REG GATING 001391	11
UP-DOWN COUNTER 001186		FIRST SEEK GATING 001421	10
4 BIT J-K REGISTER 001156	4 BIT J-K REGISTER 001156	SEEK GATING II 001536	9
RELAY LAMP DRIVERS 001136	RELAY/LAMP DRIVERS 001136	INVERTERS 001246	8
4 BIT DRIVER 001166	DRIVERS (6) 001206	RELAY/LAMP DRIVERS 001136	7
INVERTERS 001246	DRIVERS (6) 001206	INVERTERS 001246	6
LATCHES 001631	HEADS SAFETY III 001726	AC/DC SAFETY 001441	5
HOME 001561	READ WRITE ENABLE SYNC 001541	SIGNAL CONDITIONER 001566	4
			3
		REGULATOR+18,+5VDC 001366	2
	METER RELAY 001571	REGULATOR-18,-3VDC 001361	1

008031

008031

008031

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
630 A	200629 60 Hz	4-18-69	304		
630 B	200635 50 Hz	JUL 70	891		

008031

MATERIAL	SEE B/M 008031	NO.	
HARDNESS			
CASE DEPTH			
SURFACE TREATMENT			
TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	3 PLACE DEC ±	ANGLES ±
CORNERS AND/OR EDGES BROKEN	OUTSIDE		INSIDE
	MAX		MAX

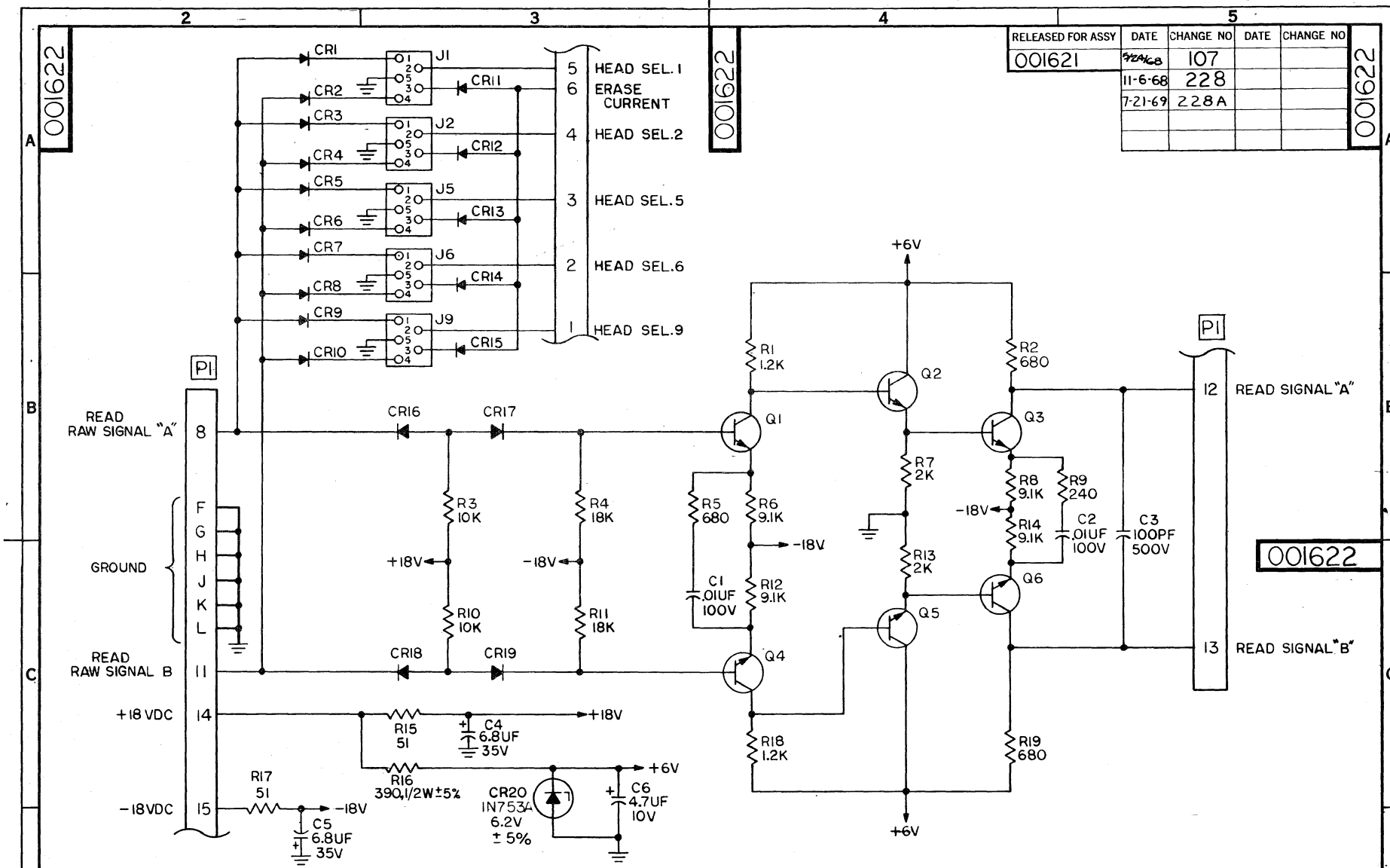
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

	NAME	DATE
DESIGN		
DETAIL		
CHECK		

MODEL 630
P.C. CARD LOCATION ASSY

DRAW	SCALE	TYPE	
E.S. 6-4-68	NONE		

008031



RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001621	5/24/68	107		
	11-6-68	228		
	7-21-69	228A		

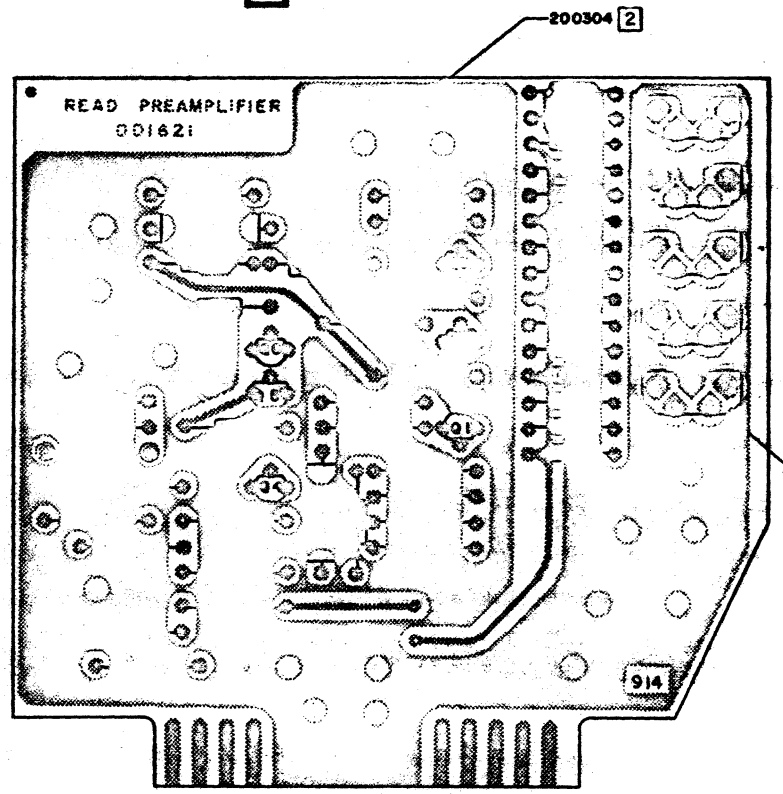
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCES ARE IN OHMS, 1/4W, 5%
2. ALL DIODES ARE IN4148
3. ALL TRANSISTORS ARE 2N3904

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION
			3 PLACE DEC ±	NAME SCHEMATIC DIAGRAM READ PREAMPLIFIER
CASE DEPTH			ANGLES ±	DESIGN apw 6-11-68 TYPE
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DETAIL SCALE NONE
SURFACE TREATMENT			INSIDE MAX	CHECK DRAW K.B. 5-24-68
001622	C	RADII UNLESS OTHERWISE NOTED		APPRO apw 6-11-68 CHECK R.S. 5-27-68

K.K.H. 6-11-68

REF DESIG	DESCRIPTION	P S C PART NO
———	PRINTED CIRCUIT BOARD	001624
C1,2	CAPACITOR, .01UF, 100V, ± 10%	151063
C3	CAPACITOR, 100PF, 500V, ± 5%	151222
C4,5	CAPACITOR, 6.8UF, 35V, ±10%	151129
C6	CAPACITOR, 4.7UF, 10V, ±10%	151124
CR1—19	DIODE, IN4148	150834
CR20	DIODE, Z, IN753A 6 2V ±5%	150840
R1,18	RESISTOR, 1.2K, 1/4W, ±5%	151485
R2,5,19	RESISTOR, 680 OHM, 1/4W, ±5%	151479
R3,10	RESISTOR, 10K, 1/4W, ±5%	151507
R4,11	RESISTOR, 18K, 1/4W, ±5%	151513
R6,8,12,14	RESISTOR, 9.1K, 1/4W, ±5%	151506
R7,13	RESISTOR, 2K, 1/4W, ±5%	151490
R9	RESISTOR, 240 OHM, 1/4W, ±5%	151468
R15,17	RESISTOR, 51 OHM, 1/4W, ±5%	151452
R16	RESISTOR, 390 OHM, 1/2W, ±5%	151617
Q1—6	TRANSISTOR, 2N3904	150735
J1,2,5,6,9	RECEPTACLE	200155
———	TAG, ENGINEERING CHANGE	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200628-60 ~	5 28 68	107	11 13 69	869
200634-50 ~	7 16 68	145	12-23-69	631
	8 6 68	228	JAN 9,70	914
	7 21 68	228A	NOV'70	1579
	9 15 69	471		



001621

NOTES: UNLESS OTHERWISE SPECIFIED.

1. INSERT MALE PLUG NO.200143 (ASSY TOOL) INTO RECEPTACLE NO.200155 PRIOR TO SOLDERING TO BOARD. PRESS RECEPTACLE PINS INTO THE RECEPTACLE BODY AFTER THE MALE PLUG IS INSERTED.
2. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
3. COMPONENT HEIGHT NOT TO EXCEED .350
4. RECPTACLE NO.200155 MUST BE SPACED FROM THE SURFACE OF THE P.C. BOARD FROM .020" TO .025"; THE AREA UNDER THE RECEPTACLE MUST BE LEFT OPEN FOR INSPECTION.

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001622	228
ARTMASTER	001623	914
FABRICATION	001624	914

MATERIAL	SEE B/M NO 001621
CASE DEPTH	
HARDNESS	
SURFACE TREATMENT	

001621 C

TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
	3 PLACE DEC ±
	ANGLES ±
CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
	INSIDE MAY
RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	P.C. BOARD ASSEMBLY			
READ PREAMPLIFIER				
DESIGN			TYPE	
DETAIL			SCALE	2/1
CHECK			DRAW	
APPRO			CHECK	

001621

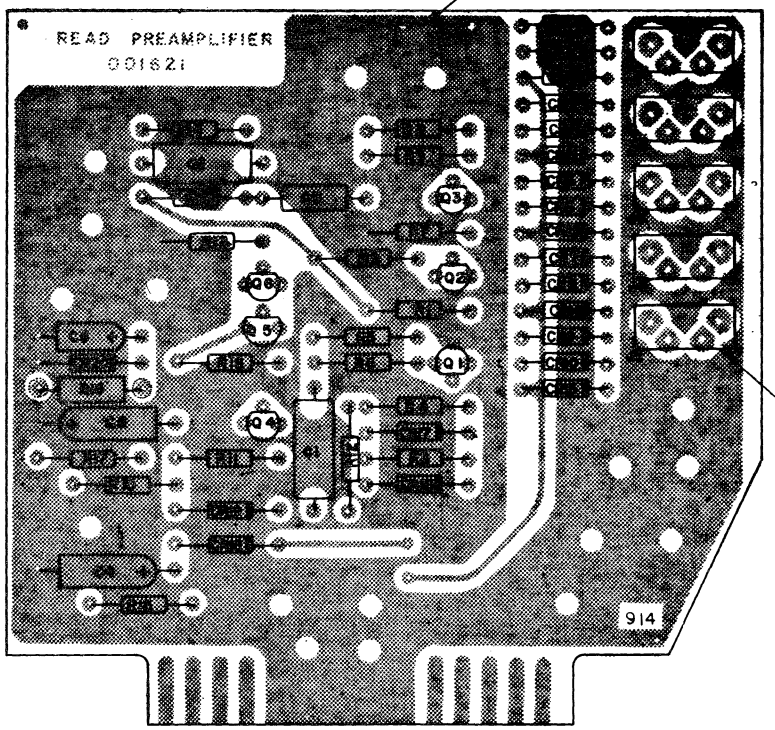
001621

REF DESIG	DESCRIPTION	P.S.C. PART NO.
———	PRINTED CIRCUIT BOARD	001624
C1,2	CAPACITOR, .01UF, 100V, ± 10%	151063
C3	CAPACITOR, 100PF, 500V, ±5%	151222
C4,5	CAPACITOR, 6.8UF, 35V, ±10%	151129
C6	CAPACITOR, 4.7UF, 10V, ±10%	151124
CR1—19	DIODE, IN4148	150834
CR20	DIODE, Z, IN753A 6.2V ±5%	150840
R1,18	RESISTOR, 1.2K, 1/4W, ±5%	151485
R2,5,19	RESISTOR, 680 OHM, 1/4W, ±5%	151479
R3,10	RESISTOR, 10K, 1/4W, ±5%	151507
R4,11	RESISTOR, 18K, 1/4W, ±5%	151513
R6,8,12,14	RESISTOR, 9.1K, 1/4W, ±5%	151506
R7,13	RESISTOR, 2K, 1/4W, ±5%	151490
R9	RESISTOR, 240 OHM, 1/4W, ±5%	151468
R15,17	RESISTOR, 51 OHM, 1/4W, ±5%	151452
R16	RESISTOR, 390 OHM, 1/2W, ±5%	151617
Q1—6	TRANSISTOR, 2N3904	150735
J1,2,5,6,9	RECEPTACLE	200155
———	TAG, ENGINEERING CHANGE	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200628-60 ~	5 28 68	107	11 13 69	569
200634-50 ~	7 16 68	145	12-23-69	631
	11 6 68	228	APR 9,70	914
	7 21 68	228 A		
	9 15 69	471		

001621

200304 [2]



[4] [1] 5 PLACES

001621

NOTES: UNLESS OTHERWISE SPECIFIED.

[1] INSERT MALE PLUG NO.200143 (ASSY TOOL) INTO RECEPTACLE NO.200155 PRIOR TO SOLDERING TO BOARD. PRESS RECEPTACLE PINS INTO THE RECEPTACLE BODY AFTER THE MALE PLUG IS INSERTED.

[2] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER

3. COMPONENT HEIGHT NOT TO EXCEED .350

[4] RECPTACLE NO. 200155 MUST BE SPACED FROM THE SURFACE OF THE P.C. BOARD FROM .020" TO .025"; THE AREA UNDER THE RECEPTACLE MUST BE LEFT OPEN FOR INSPECTION.

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001622	228
ARTMASTER	001623	914
FABRICATION	001624	914

MATERIAL SEE B/M	NO 001621	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001621	C	RADII UNLESS OTHERWISE NOTED	

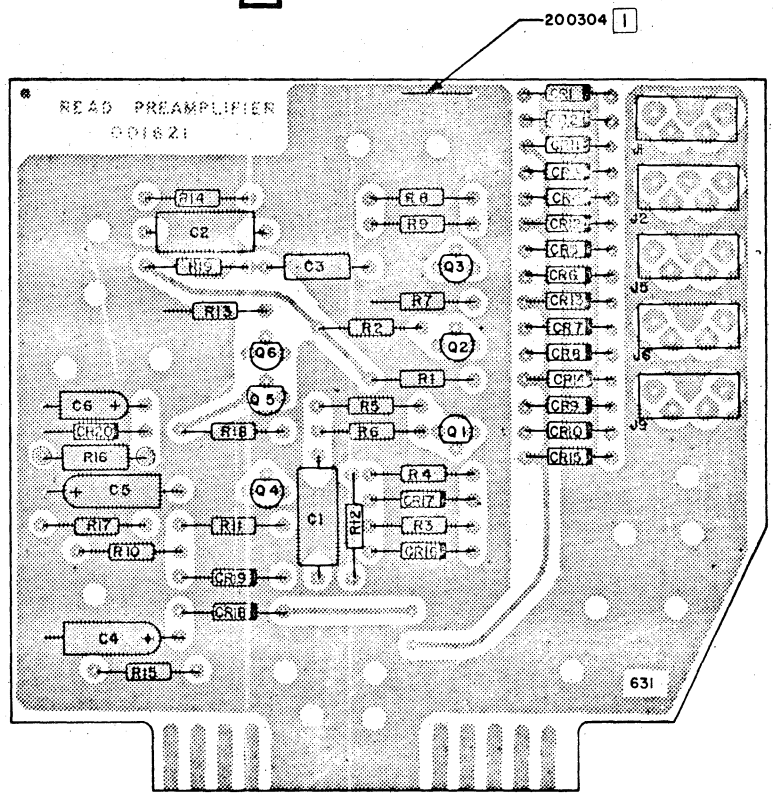
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	P.C. BOARD ASSEMBLY				
READ PREAMPLIFIER					
DESIGN	W W	6-11-68	TYPE		
DETAIL			SCALE	2/1	
CHECK			DRAW	JIM	5/28/68
APPRO	W W K E	6-11-68 6-11-68	CHECK	R.D.E.	6/10/68

001621

REF DESIG	DESCRIPTION	P S C PART NO
———	PRINTED CIRCUIT BOARD	001624
C1,2	CAPACITOR, .01UF, 100V, ± 10%	151063
C3	CAPACITOR, 100PF, 500V, ± 5%	151222
C4,5	CAPACITOR, 6.8UF, 35V, ±10%	151129
C6	CAPACITOR, 4.7UF, 10V, ±10%	151124
CR1—19	DIODE, IN4148	150834
CR20	DIODE, Z, IN753A 6.2V ±5%	150840
R1,18	RESISTOR, 1.2K, 1/4W, ±5%	151485
R2,5,19	RESISTOR, 680 OHM, 1/4W, ±5%	151479
R3,10	RESISTOR, 10K, 1/4W, ±5%	151507
R4,11	RESISTOR, 18K, 1/4W, ± 5%	151513
R6,8,12,14	RESISTOR, 9.1K, 1/4W, ± 5%	151506
R7,13	RESISTOR, 2K, 1/4W, ±5%	151490
R9	RESISTOR, 240 OHM, 1/4W, ± 5%	151468
R15,17	RESISTOR, 51 OHM, 1/4W, ±5%	151452
R16	RESISTOR, 390 OHM, 1/2W, ± 5%	151617
Q1—6	TRANSISTOR, 2N3904	150735
J1,2,5,6,9	RECEPTACLE	200155
———	TAG, ENGINEERING CHANGE	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200628-60 ~	5 28 68	107	11 15 69	569
200634-50 ~	7 16 68	145	12-23-69	631
	11 6 68	228		
	7 21 68	228A		
	9 15 69	471		



REFERENCE DOCUMENTS		EC LEVEL
SCH DIAG.	001622	228
ART MASTER	001623	631
FABRICATION	001624	631

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M NO 001621

CASE DEPTH

HARDNESS

SURFACE TREATMENT

001621 C

TOLERANCE UNLESS OTHERWISE NOTED: 2 PLACE DEC ±; 3 PLACE DEC ±; ANGLES ±

CORNERS AND/OR EDGES BROKEN: OUTSIDE MAX; INSIDE MAX

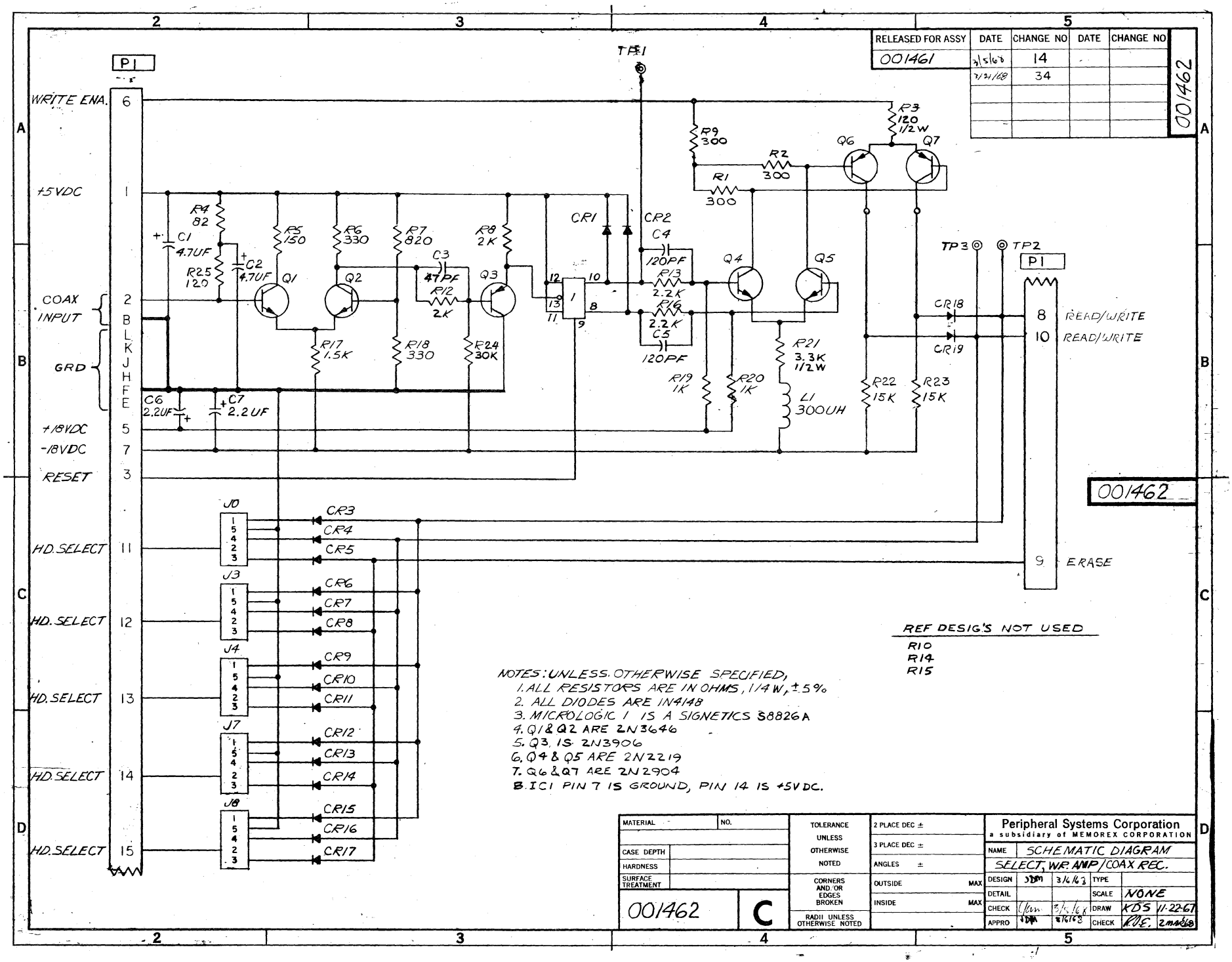
RADII UNLESS OTHERWISE NOTED

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME P.C. BOARD ASSEMBLY
READ PREAMPLIFIER

DESIGN	W W	6-11-68	TYPE		
DETAIL			SCALE	2/1	
CHECK			DRAW	JIM	5/29/68
APPRO	W W E	6-11-68	CHECK	R.D.E.	6/11/68

001621



RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001461	2/5/68	14		
	2/21/68	34		

001462

001462

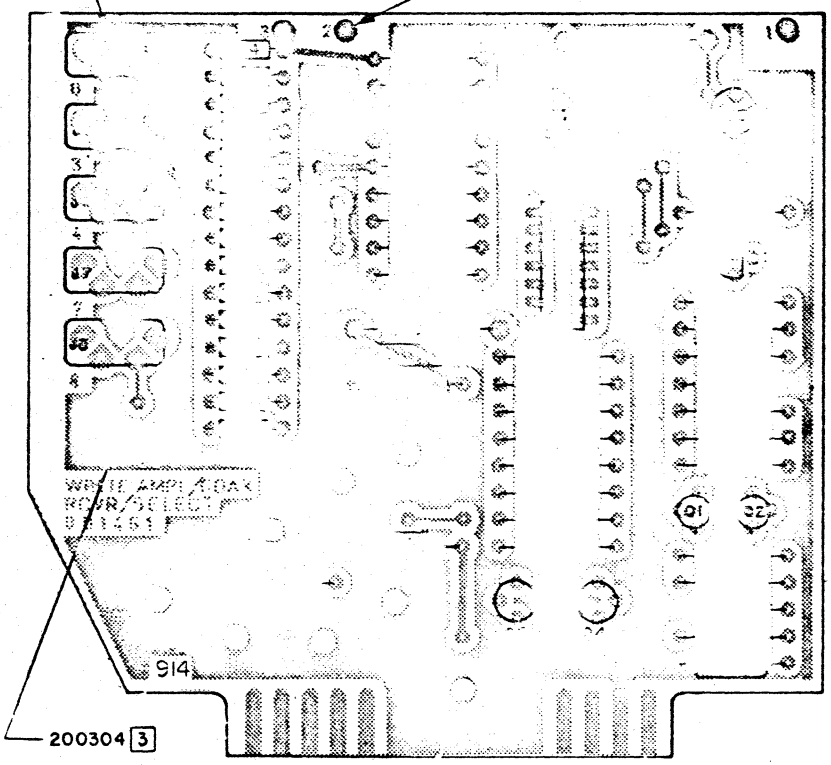
REF DESIG'S NOT USED

R10
R14
R15

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTORS ARE IN OHMS, 1/4 W, ±5%
2. ALL DIODES ARE IN4148
3. MICROLOGIC 1 IS A SIGNETICS S8826A
4. Q1 & Q2 ARE 2N3646
5. Q3 IS 2N3906
6. Q4 & Q5 ARE 2N2219
7. Q6 & Q7 ARE 2N2904
8. IC1 PIN 7 IS GROUND, PIN 14 IS +5V DC.

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
CASE DEPTH			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM SELECT, WR. AMP/COAX REC.
HARDNESS			ANGLES ±	DESIGN	3/4/68 TYPE
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DETAIL	SCALE NONE
001462	C		INSIDE MAX	CHECK	3/5/68 DRAW KDS 11-22-67
		RADII UNLESS OTHERWISE NOTED		APPRO	3/6/68 CHECK RE. 2mar68

REF DESIG	DESCRIPTION	M. E. G. PART NO.
———	PRINTED CIRCUIT BOARD	001464
C1,2	CAPACITOR, .47 μF, 0V, ± 0%	51124
C4,5	120 PF 500V ± 5%	5224
C6,7	2.2 UF 35V, ± 0%	151127
C3	CAPACITOR, 47PF, 500V, ± 5%	151215
CR1-19	DIODE (IN4148)	150854
L1	NDUCTOR, 300UH	151397
IC1	INTEGRATED CIRCUIT (SE8264)	150663
Q1,2	TRANSISTOR (2N3646)	150734
Q3	(2N3906)	150736
Q4,5	(2N2219)	150741
Q6,7	TRANSISTOR (2N2904)	150742
R1,29	RESISTOR, 300Ω, 1/4W, ± 5%	51470
R4	82Ω,	151457
R6,18	330Ω,	151471
R7	820Ω,	151481
R8,12	2K,	151490
R13,16	2.2K,	151491
R17	1.5K,	151487
R19,20	1K,	151483
R22,23	15K,	151511
R24	30K,	151518
R25	120Ω,	151461
R5	150Ω, 1/4W,	151463
R3	120Ω, 1/2W,	151605
R21	RESISTOR, 3.3K, 1/2W, ± 5%	151639
J0,3,4,7,8	RECEPTACLE	200155
———	TAG, ENGINEERING CHANGE	200304
———	TERMINAL, TEST POINT	150374



NOTES: UNLESS OTHERWISE SPECIFIED

1. RECEPTACLE NO 200155 MUST BE SPACED FROM THE SURFACE OF THE P.C BOARD FROM .020" TO .025" THE RECEPTACLE MUST BE LEFT OPEN FOR INSPECTION.
2. INSERT MALE PLUG NO.200143 (ASSY TOOL) INTO RECEPTACLE NO.200155 PRIOR TO SOLDERING TO BOARD. PRESS RECEPTACLE PINS INTO THE RECEPTACLE BODY AFTER THE MALE PLUG IS INSERTED.
3. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
4. COMPONENT HEIGHT NOT TO EXCEED .350"

REFERENCE DOCUMENTS		EC LEVEL
SCH DIAG	[illegible]	[illegible]
ARTMASTER	[illegible]	914
FABRICATION	[illegible]	914

MATERIAL SEE B/M NO C01461
CASE DEPTH
HARDNESS
SURFACE TREATMENT
C01461 C

TOLERANCE UNLESS OTHERWISE NOTED: 2 PLACE DEC ±; 3 PLACE DEC; ANGLES; OUTSIDE MAY; INSIDE MAY; CORNERS AND OR EDGES BROKEN; RADII UNLESS OTHERWISE NOTED

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

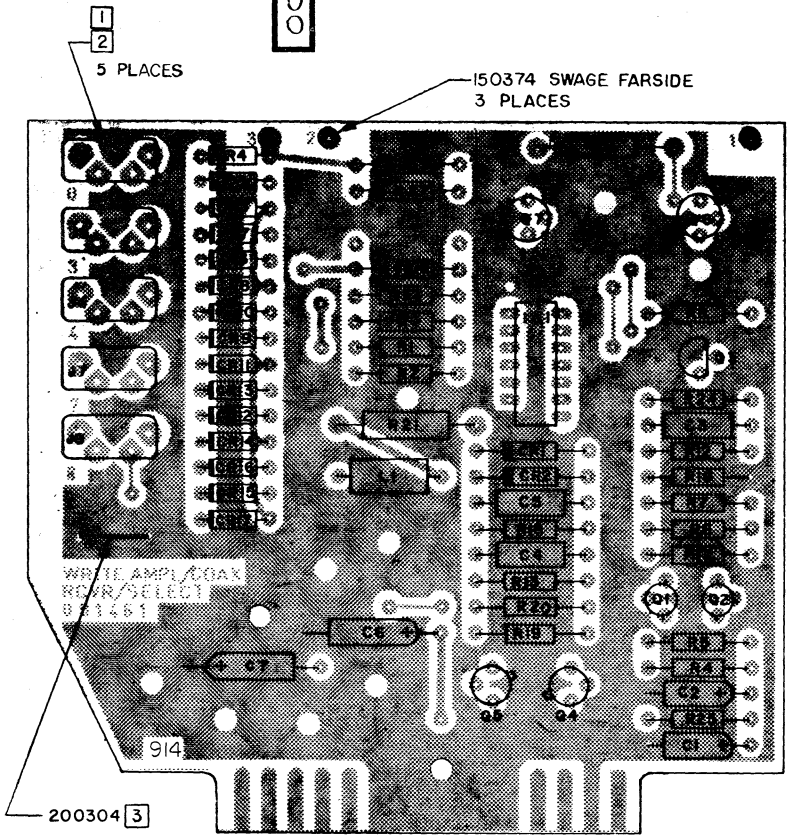
NAME P.C. BOARD ASSEMBLY
ARTE AMPL/COAX RCVR/SEL
DESIGN TYPE
DETAIL SCALE 2/1
CHECK DRAW
APPRO CHECK

C01461

2 3 4 5

REF DESIG	DESCRIPTION	M. E. G. PART NO.
———	PRINTED CIRCUIT BOARD	001464
C1, 2	CAPACITOR, .47 UF, 10V, ± 10%	151124
C4, 5	120 PF, 500V, ±5%	151224
C6, 7	2.2 UF, 35V, ±10%	151127
C3	CAPACITOR, 47PF, 500V, ±5%	151215
CR1-19	DIODE (IN4148)	150834
L1	INDUCTOR, 300UH	151397
IC1	INTEGRATED CIRCUIT(S88264)	150663
Q1, 2	TRANSISTOR (2N3646)	150734
Q3	(2N3906)	150736
Q4, 5	(2N2219)	150741
Q6, 7	TRANSISTOR (2N2904)	150742
R1, 2, 9	RESISTOR, 300Ω, 1/4W, ±5%	151470
R4	82Ω,	151457
R6, 18	330Ω,	151471
R7	820Ω,	151481
R8, 12	2K,	151490
R13, 16	2.2K,	151491
R17	1.5K,	151487
R19, 20	1K,	151483
R22, 23	15K,	151511
R24	30K,	151518
R25	120Ω,	151461
R5	150Ω, 1/4W,	151463
R3	120Ω, 1/2W,	151605
R21	RESISTOR, 3.3K, 1/2W, ±5%	151639
J0, 3, 4, 7, 8	RECEPTACLE	200155
———	TAG, ENGINEERING CHANGE	200304
———	TERMINAL, TEST POINT	150374

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200628-60	3/5/68	14	11/14/69	569
200634-50	3/21/68	34	APR 9, 70	914
	5/27/68	64		
	7/16/68	156		
	9/20/69	470		



001461

NOTES: UNLESS OTHERWISE SPECIFIED

1. RECEPTACLE NO. 200155 MUST BE SPACED FROM THE SURFACE OF THE P.C. BOARD FROM .020" TO .025". THE RECEPTACLE MUST BE LEFT OPEN FOR INSPECTION.
2. INSERT MALE PLUG NO. 200143 (ASSY TOOL) INTO RECEPTACLE NO. 200155 PRIOR TO SOLDERING TO BOARD. PRESS RECEPTACLE PINS INTO THE RECEPTACLE BODY AFTER THE MALE PLUG IS INSERTED.

3 **ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER**

4. **COMPONENT HEIGHT NOT TO EXCEED .350"**

REFERENCE	DOCUMENTS	EC LEVEL
SCH. DIAG.	001462	34
ARTMASTER	001463	914
FABRICATION	001464	914

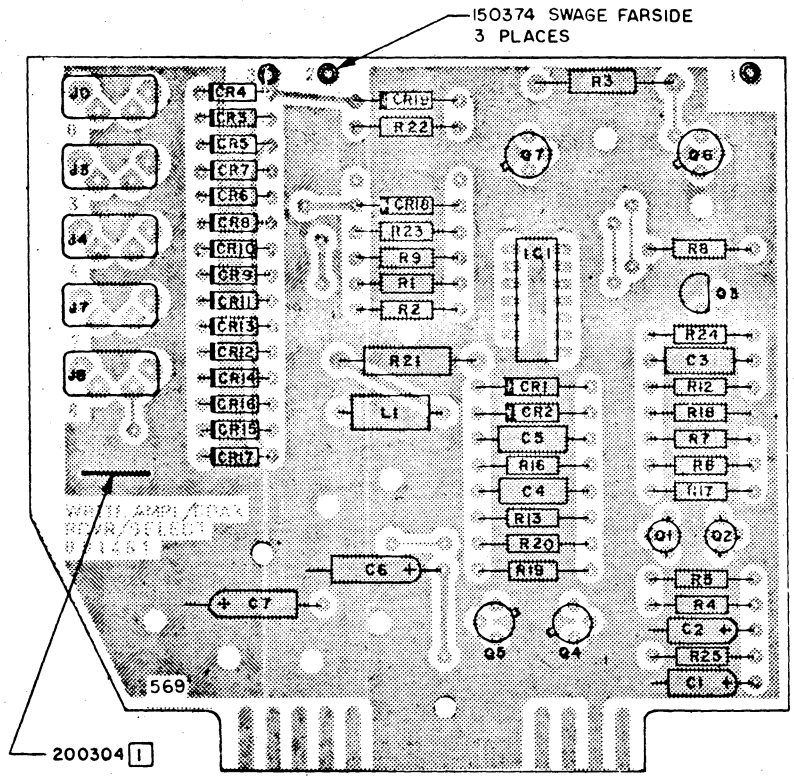
MATERIAL SEE B/M NO 001461		TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001461	C	RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	P.C. BOARD ASSEMBLY			
	WRITE AMPL./COAX RECVR/SEL			
DESIGN		TYPE		
DETAIL		SCALE	2/1	
CHECK		DRAW	RE	2-16-68
APPRO		CHECK	RE	3/2/68

001461

REF DESIG	DESCRIPTION	M. E. G PART NO.
———	PRINTED CIRCUIT BOARD	001464
C1, 2	CAPACITOR, .47 UF, 10V, ±10%	151124
C4, 5	120 PF, 500V, ±5%	151224
C6, 7	2.2 UF, 35V, ±10%	151127
C3	CAPACITOR, 47PF, 500V, ±5%	151215
CR1-19	DIODE (IN4148)	150854
L1	INDUCTOR, 300UH	151397
IC1	INTEGRATED CIRCUIT(S88264)	150663
Q1, 2	TRANSISTOR (2N3646)	150734
Q3	(2N3906)	150736
Q4, 5	(2N2219)	150741
Q6, 7	TRANSISTOR (2N2904)	150742
R1, 2, 9	RESISTOR, 300Ω, 1/4W, ±5%	151470
R4	82Ω,	151457
R6, 18	330Ω,	151471
R7	820Ω,	151481
R8, 12	2K,	151490
R13, 16	2.2K,	151491
R17	1.5K,	151487
R19, 20	1K,	151483
R22, 23	15K,	151511
R24	30K,	151518
R25	120Ω,	151461
R5	150Ω, 1/4W,	151463
R3	120Ω, 1/2W,	151605
R21	RESISTOR, 3.3K, 1/2W, ±5%	151639
J0, 3, 4, 7, 8	RECEPTACLE	200155
———	TAG, ENGINEERING CHANGE	200304
———	TERMINAL, TEST POINT	150374



RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200628-60	3/5/69	14	11/14/69	569
200634-50	3/24/69	34		
	5/21/69	64		
	7/16/69	156		
	9/20/69	470		

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG	001462	34
ARTMASTER	001463	569
FABRICATION	001464	569

NOTES: UNLESS OTHERWISE SPECIFIED

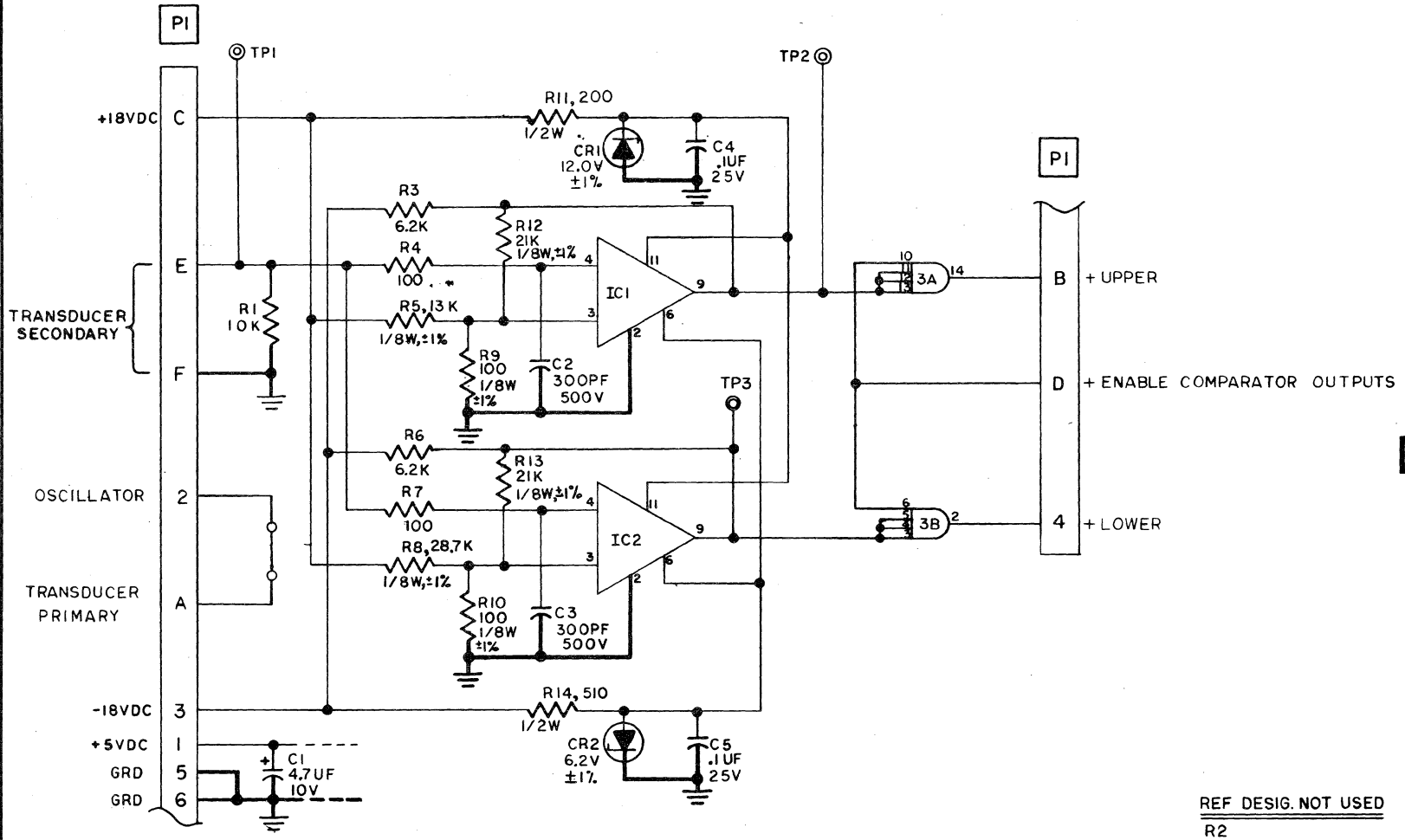
1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M NO 001461	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation, a subsidiary of MEMOREX CORPORATION
CASE DEPTH		3 PLACE DEC	NAME P.C. BOARD ASSEMBLY
HARDNESS		ANGLES	WRITE AMPL./COAX RECVR/SEL
SURFACE TREATMENT	CORNERS AND OR EDGES BROKEN	OUTSIDE MAX	DESIGN — TYPE
001461 C	RADII UNLESS OTHERWISE NOTED	INSIDE MAY	DETAIL — SCALE 2/1
			CHECK — DRAW RE 2-16-68
			APPRO — CHECK RE 3/2/68

001461

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001591	5-28-8	104		
	12/1/67	493		

001592



001592

REF DESIG. NOT USED

R2

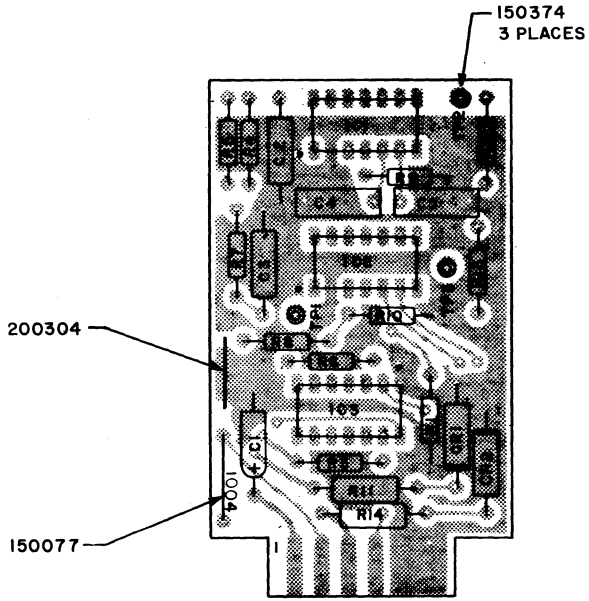
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1/4W, ±5%
2. CONNECT PIN 1 OF IC3 TO GRD, PIN 8 TO +5VDC
3. IC3 IS SP659A
4. IC1 AND IC2 ARE MOTOROLA MC1710CL

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION
			3 PLACE DEC ±	
CASE DEPTH			ANGLES ±	NAME SCHEMATIC DIAGRAM CYL TRANSDUCER COMP
HARDNESS			OUTSIDE MAX	DESIGN TYPE
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	INSIDE MAX	DETAIL SCALE
001592	C	RADII UNLESS OTHERWISE NOTED		CHECK M.C.L. 6/20/68 DRAW 9/20/68
				APPRO 6/24/68 CHECK 9/20/68

001592

REF DESIG	DESCRIPTION	M. E. G. PART NO.
———	PRINTED CIRCUIT BOARD	001594
C1	CAPACITOR, T, 4.7UF, 10V, ±10%	151124
C2,3	CAPACITOR, P, 300PF, 500V, ±5%	151233
C4,5	CAPACITOR, C, 0.1UF, 25V, ±20%	150980
CR1	DIODE Z, SZ 12.0, 1%	150907
CR2	DIODE Z, SZ 6.2, 1%	150900
R3,6	RESISTOR, COMP, 6.2K, ¼W, 5%	151502
R4,7	COMP, 100 Ω, ¼W, 5%	151459
R5	MF, 13K, ⅛W, 1%	153070
R8	28.7K, ⅛W, 1%	153103
R9,10	100 Ω, ⅛W, 1%	152963
R12,13	MF, 21K, ⅛W, 1%	153090
R1	COMP, 10K, ¼W, 5%	151507
R11	COMP, 200 Ω, ½W, 5%	151610
R14	RESISTOR, COMP, 510 Ω, ½W, 5%	151620
IC1,2	INTEGRATED CIRCUIT, MC1710CL	150664
IC3	INTEGRATED CIRCUIT, SP659A	150654
———	WIRE, 22 GAGE, SOLID, BARE	150077
TP1-3	TERMINALS, TEST POINTS, USECO 2030B	150374
———	TAG, ENGINEERING CHANGE	200304

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
630 A	200628-60∩	5.25.68	104		
630 B	200634-50∩	9.5.69	439		
	MULTI-USE	12.11.69	493		
		MAY 6, 70	1004		



NOTES: UNLESS OTHERWISE SPECIFIED
1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

REFERENCE DOCUMENTS		E.C. LEVEL
SCH. DIAG.	001592	493
ARTMASTER	001593	1004
FABRICATION	001594	1004
TEST SPEC.		

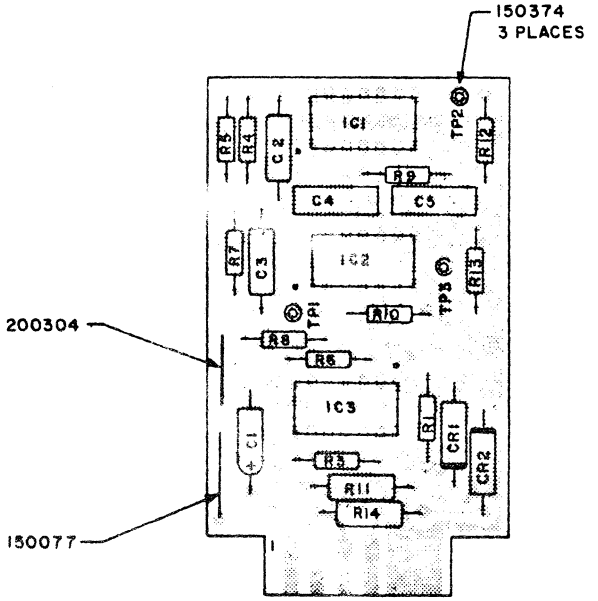
MATERIAL SEE B/M	NO. 001591	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
CASE DEPTH			3 PLACE DEC ±	NAME	P.C. BOARD ASSEMBLY
HARDNESS			ANGLES ±		CYL TRANSDUCER COMPARATOR
SURFACE TREATMENT		CORNERS AND OR EDGES BROKEN	OUTSIDE MAX	DESIGN	TYPE
001591	C		INSIDE MAX	DETAIL	SCALE 2/1
		RADII UNLESS OTHERWISE NOTED		CHECK M·C·L 6 17 68	DRAW 11 Dec '69
				APPRO JOK 6 24 68	CHECK P L E 6 17 68

001591

USED ON	RELEASED FOR ASSY
630 A	200628-60~
630 B	200634-50~
620 A	202020
620 B	202021

DATE	CHANGE NO.	DATE	CHANGE NO.
8-25-67	104		
9-3-67	439		
12-11-67	493		

REF DESIG	DESCRIPTION	M E G PART NO
———	PRINTED CIRCUIT BOARD	001594
C1	CAPACITOR, T, 4.7UF, 10V, ± 10%	151124
C2,3	CAPACITOR, P, 300 PF, 500V, ± 5%	151233
C4,5	CAPACITOR, C, 0.1 UF, 25V, ± 20%	150980
CR1	DIODE Z, SZ 12.0, 1%	150907
CR2	DIODE Z, SZ 6.2, 1%	150930
R3,6	RESISTOR, COMP, 6.2K, 1/4W, 5%	51502
R4,7	COMP, 100 Ω, 1/4W, 5%	51459
R5	MF, 13K, 1/8W, 1%	153070
R8	28.7K, 1/8W, 1%	153107
R9,10	100 Ω, 1/8W, 1%	152963
R12,13	MF, 21K, 1/8W, 1%	153090
R1	COMP, 10K, 1/4W, 5%	151507
R11	COMP, 200 Ω, 1/2W, 5%	151610
R14	RESISTOR, COMP, 510Ω, 1/2W, 5%	151620
IC1,2	INTEGRATED CIRCUIT, MC1710CL	150664
IC3	INTEGRATED CIRCUIT, SP659A	50654
———	WIRE, 22 GAGE, SOLID, BARE	150077
TP1-3	TERMINALS, TEST POINTS, ISECO 7030B	50374
———	TAG, ENGINEERING CHANGE	200304



NOTES: UNLESS OTHERWISE SPECIFIED
1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

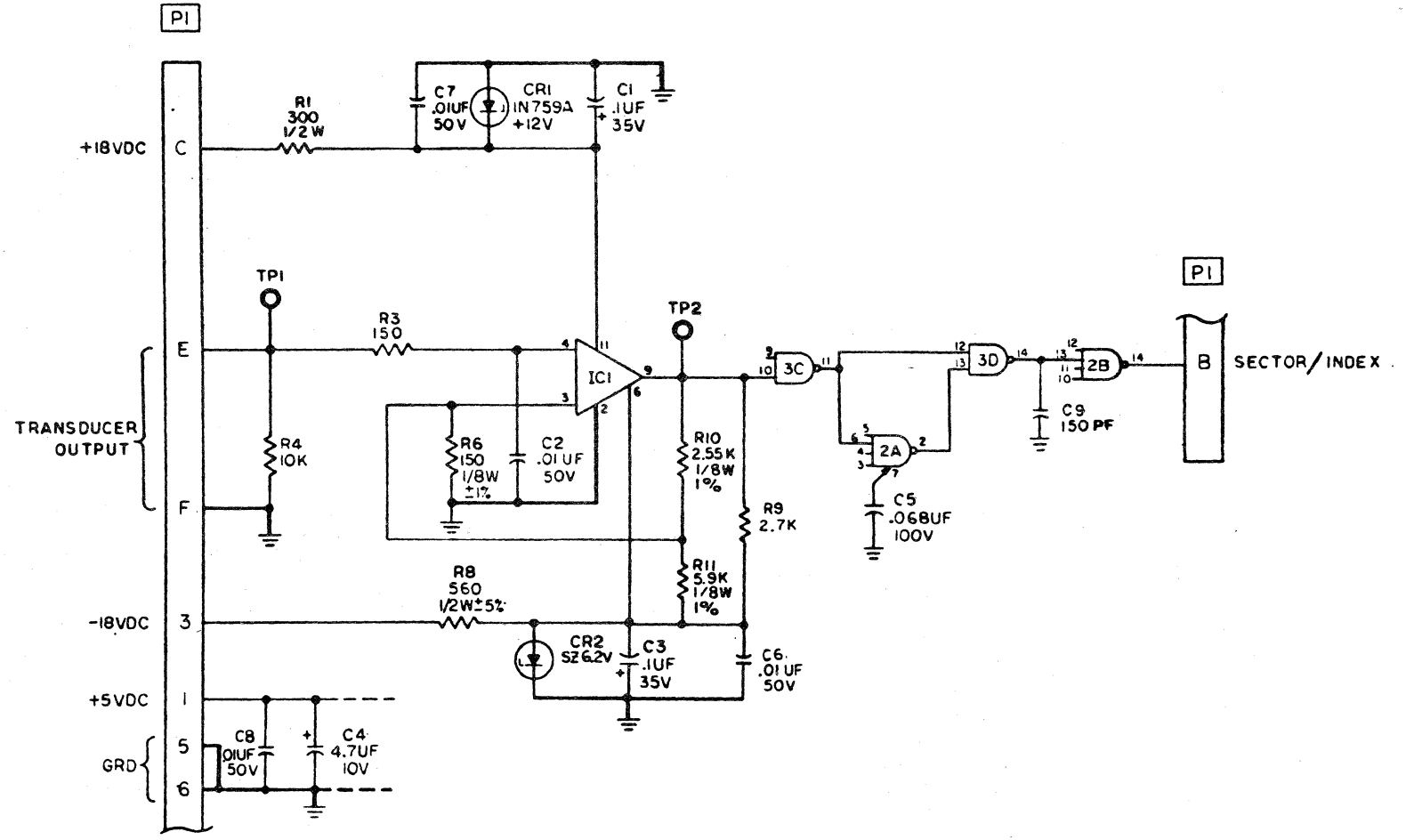
REFERENCE DOCUMENTS		E C LEVEL
SCH. DIAG	001592	493
ARTMASTER	001593	493
FABRICATION	001594	493
TEST SPEC		

MATERIAL: SEE B/M 001591 | TOLERANCE UNLESS OTHERWISE NOTED: | FINISH: | BREAK CORNERS AND EDGES | DRAWING NO. 001591 | SIZE C

Peripheral Systems Corporation
PC BOARD ASSEMBLY
CYL TRANSDUCER COMPARATOR
SCALE 2/1
DRAWN M.C.L. 6/17/68
CHECKED J.O.K. 6/24/68
APPROVED R.L.E. 6/17/68

001591

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001626	5-29-68	104		
	7/29/68	175		
	1-6-70	519		



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS. 1/4W ±5%
2. IC1 IS A MOTOROLA MC1710CL
3. IC2 IS A SP659A
4. CONNECT PIN 1 OF IC2 & 3 TO GRD, PIN 8 TO +5VDC
5. IC3 IS A SP680A

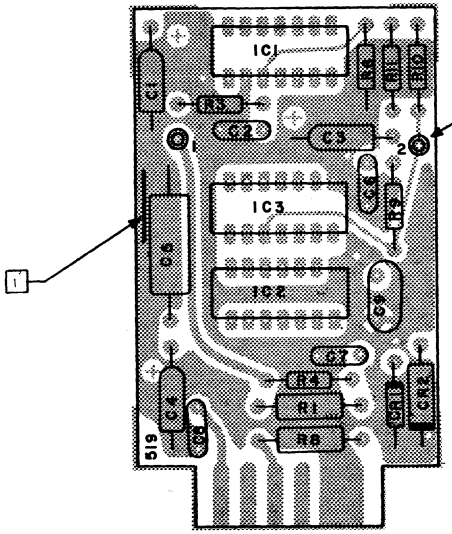
MATERIAL / NO	TOLERANCE	PLACE DEC.	Peripheral Systems Corporation	
CASE DEPTH / HARDNESS / SURFACE TREATMENT		PLACE DEC. / ANGLES	NAME: SCHEMATIC DIAGRAM INDEX TRANSDUCER COMP	
001627 C		D. TITLE / NOTE	DESIGN / DETAIL / CHECK / APPD	TYPE: NONE

001627

001626

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200628-60Ω	6-17-68	104		
200634-50Ω	7-30-68	175		
	9-13-68	205		
	1-7-70	519		

REF DESIG	DESCRIPTION	M. E. G. PART NO.
———	PRINTED CIRCUIT BOARD	001629
C2,6-8	CAPACITOR, C, .01 UF, 50V, ±20%	150991
C1,3	T, .1UF, 35V, ±10%	151096
C9	S/M, 150PF, 500V, ±5%	153720
C4	T, 4.7UF, 10V, ±10%	151124
C5	CAPACITOR, M, .068 UF, 100V, ±10%	151074
CR1	DIODE Z, SZ IN759A, 12V	150841
CR2	DIODE Z, SZ 6.2V, 1%	150900
R10	RESISTOR, 2.55K, 1/8 W, ±1%	153050
R1	300Ω, 1/2 W, ±5%	151614
R3	150Ω, 1/4 W, ±5%	151463
R4	10K, 1/4W, ±5%	151507
R6	150Ω, 1/8W, ±1%	152980
R8	560Ω, 1/2 W, ±5%	151621
R9	2.7K, 1/4W, ±5%	151493
R11	RESISTOR, 5.9K, 1/8W, ±1%	153229
IC1	INTEGRATED CIRCUIT, MC1710CL	150664
IC2	INTEGRATED CIRCUIT, SP659A	150654
IC3	INTEGRATED CIRCUIT, SP680A	150656
TP1,2	TERMINAL, TEST POINT, USECO 2030B	150374
	TAG, ENGINEERING CHANGE	200304



150374 SWAGE (FARSIDE)
2 PLACES

001626

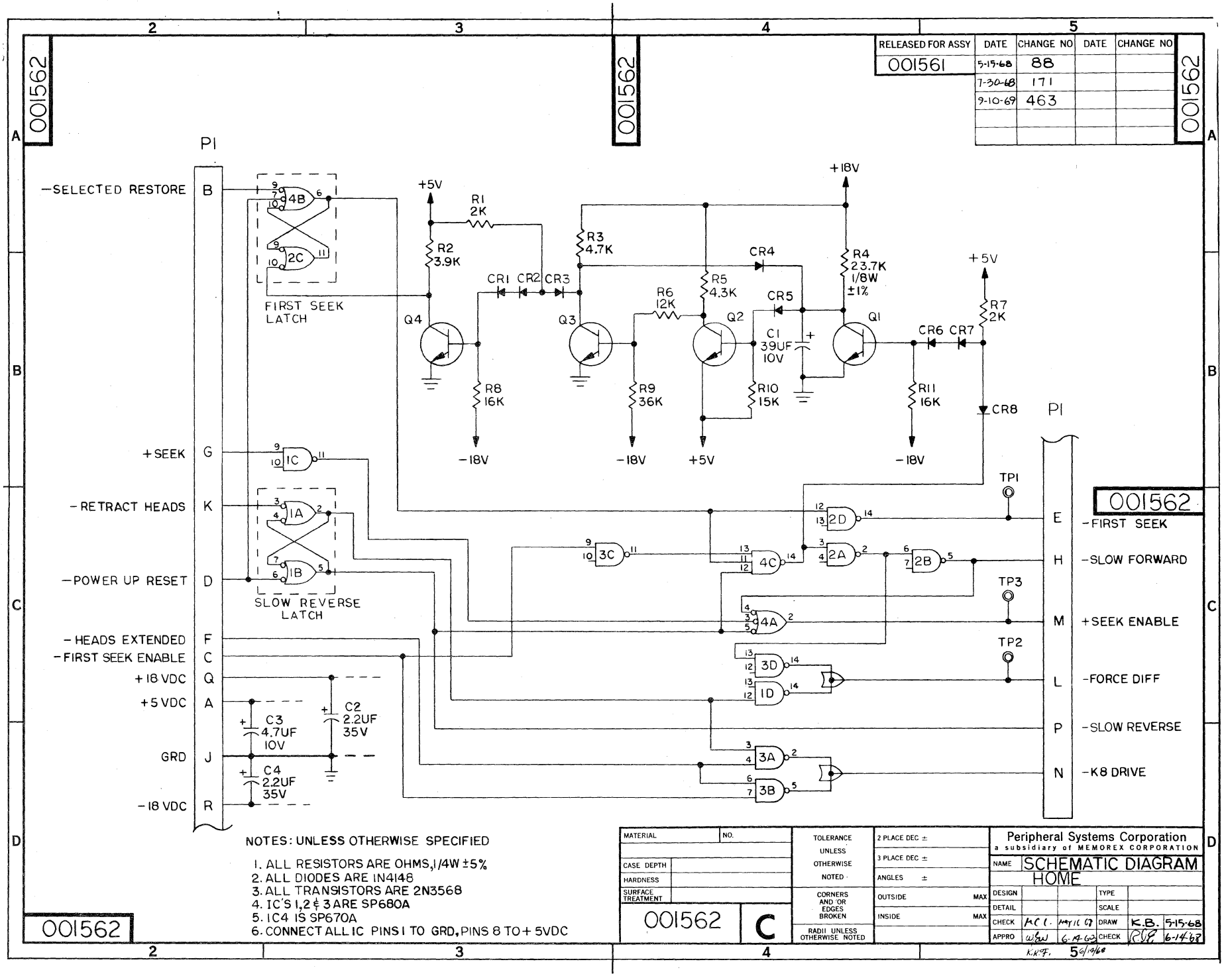
NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

REFERENCE DOCUMENTS		E.C. LEVEL
SCH. DIAG.	001627	519
ARTMASTER	001628	519
FABRICATION	001629	519
TEST SPEC.		

MATERIAL SEE B/M NO. 001626	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION
CASE DEPTH		3 PLACE DEC ±	NAME P.C. BOARD ASSEMBLY
HARDNESS		ANGLES ±	INDEX TRANSDUCER COMP
SURFACE TREATMENT	CORNERS AND OR EDGES BROKEN	OUTSIDE MAX	DESIGN TYPE
001626 C	RADII UNLESS OTHERWISE NOTED	INSIDE MAX	DETAIL SCALE 2/1
			CHECK MCB 7-30-68 DRAW 1-8-70
			APPRO CHECK 1-15-70

001626

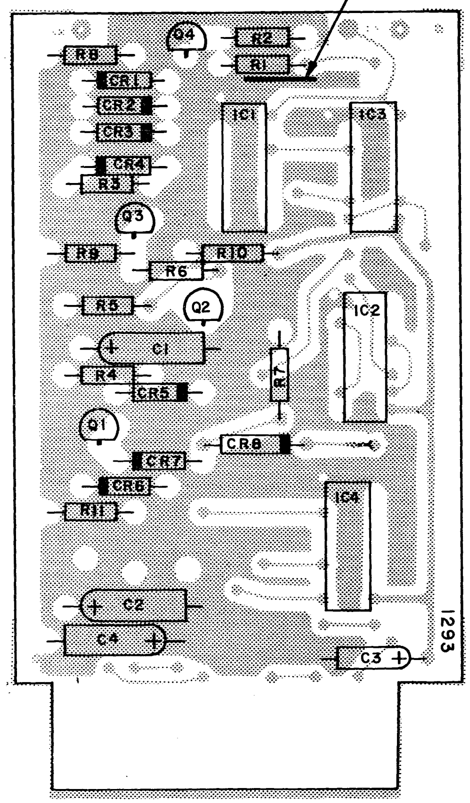

001562
RELEASED FOR ASSY
001561
DATE
CHANGE NO
5-15-68 88
7-30-68 171
9-10-69 463
P1
-SELECTED RESTORE B
+SEEK G
-RETRACT HEADS K
-POWER UP RESET D
-HEADS EXTENDED F
-FIRST SEEK ENABLE C
+18 VDC Q
+5 VDC A
GRD J
-18 VDC R
4B
2C
FIRST SEEK LATCH
1C
1A
1B
SLOW REVERSE LATCH
+5V
+18V
-18V
R1 2K
R2 3.9K
R3 4.7K
R4 23.7K 1/8W ±1%
R5 4.3K
R6 12K
R7 2K
R8 16K
R9 36K
R10 15K
R11 16K
CR1 CR2 CR3
CR4
CR5
CR6 CR7
CR8
Q1
Q2
Q3
Q4
C1 39UF 10V
C2 2.2UF 35V
C3 4.7UF 10V
C4 2.2UF 35V
2D
3C
4C
2A
2B
4A
3D
1D
3A
3B
TP1
TP3
TP2
E -FIRST SEEK
H -SLOW FORWARD
M +SEEK ENABLE
L -FORCE DIFF
P -SLOW REVERSE
N -K8 DRIVE
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE OHMS, 1/4W ±5%
2. ALL DIODES ARE IN4148
3. ALL TRANSISTORS ARE 2N3568
4. IC'S 1, 2 & 3 ARE SP680A
5. IC4 IS SP670A
6. CONNECT ALL IC PINS 1 TO GRD, PINS 8 TO +5VDC
MATERIAL
NO.
CASE DEPTH
HARDNESS
SURFACE TREATMENT
001562
C
TOLERANCE UNLESS OTHERWISE NOTED
2 PLACE DEC ±
3 PLACE DEC ±
ANGLES ±
CORNERS AND 'OR EDGES BROKEN
OUTSIDE MAX
INSIDE MAX
RADII UNLESS OTHERWISE NOTED
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION
NAME SCHEMATIC DIAGRAM HOME
DESIGN
DETAIL
CHECK MCC. MAGIC G
APPRO WSW 6-4-69
TYPE
SCALE
DRAW K.B. 5-15-68
CHECK RDB 6-14-68
K.K.F. 5/19/68
001562

REF DESIG	DESCRIPTION	P. S. C. PART NO.
———	PRINTED CIRCUIT BOARD	001564
C1	CAPACITOR, 39UF, 10V ±10%	151139
C2,4	CAPACITOR, 2.2UF, 35V ±10%	151127
C3	CAPACITOR, 4.7UF, 10V ±10%	151124
CR1-8	DIODE, 1N4148	150834
IC1,2,3	INTEGRATED CIRCUIT, SP680A	150656
IC4	INTEGRATED CIRCUIT, SP670A	150655
R1,7	RESISTOR, 2K, 1/4W ±5%	151490
R2	3.9K, 1/4W ±5%	151497
R3,5	4.7K, 1/4W ±5%	151499
R4	23.7K, 1/8W ±1%	153075
R6	12K, 1/4W ±5%	151509
R8,11	16K, 1/4W ±5%	151512
R9	36K, 1/4W ±5%	151520
R10	RESISTOR, 15K, 1/4W ±5%	151511
Q1,2,3,4	TRANSISTOR, 2N3568	150730
———	TAG, ENGINEERING CHANGE	200304

RELEASED	DATE	CHANGE	DATE	CHANGE
200490-60	14MAY68	88	1-2-70	580
200495-50	7-30-68	171	JULY'70	1293
	11-19-68	219		
	7-21-69	219A		
	10-69	463		

001561

200304 [1]



001561

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001562	463
ARTMASTER	001563	1293
FABRICATION	001564	1293

NOTES: UNLESS OTHERWISE SPECIFIED

[1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER

2 COMPONENT HEIGHT NOT TO EXCEED .4

B/M 001561

Peripheral Systems Corporation

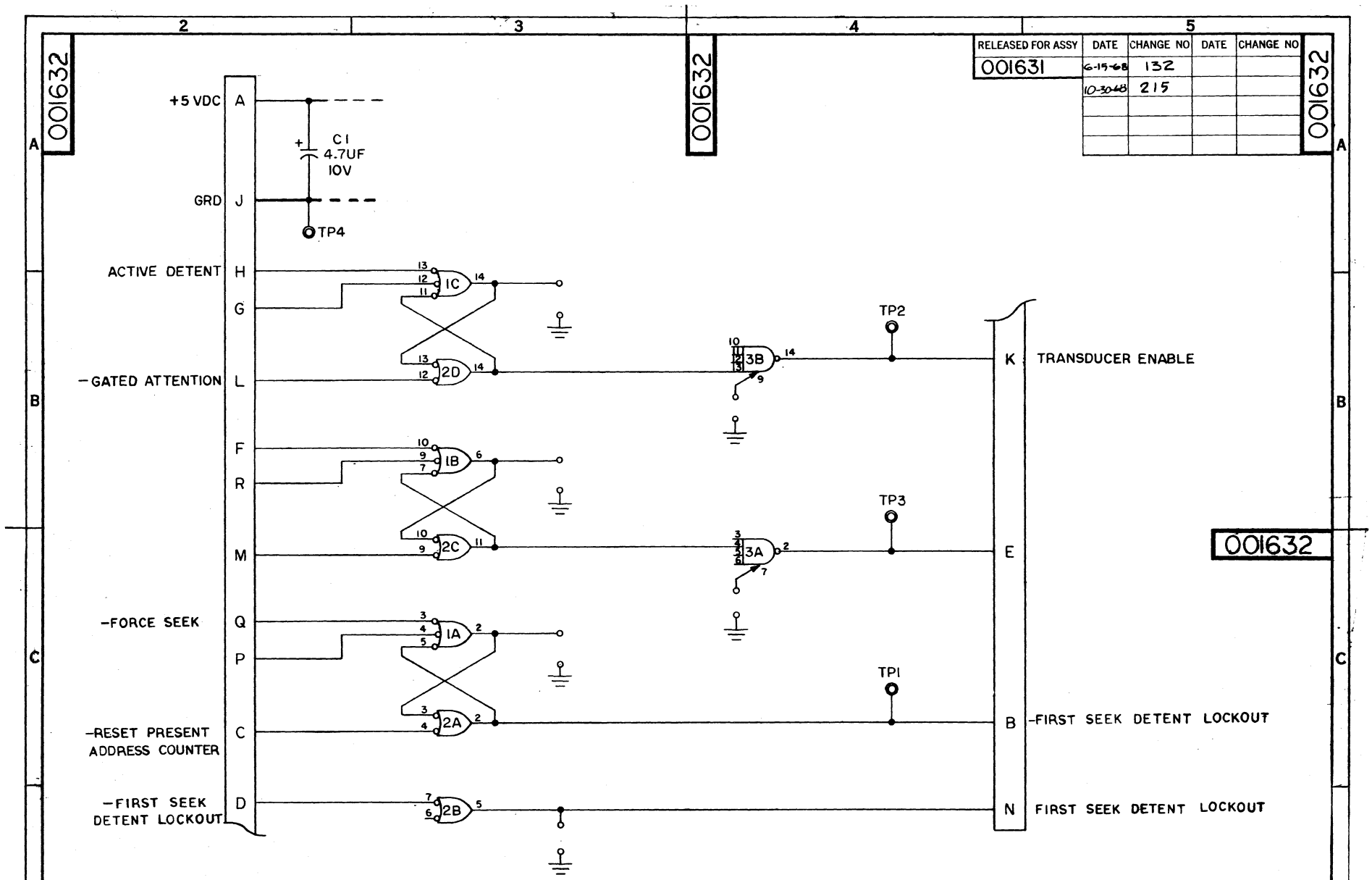
P.C. BOARD ASSEMBLY
HOME

2/1

MCL 5-17-68 RDE 14MAY68

001561 C

001561


001632
001632
001632
001632
001632
001632
RELEASED FOR ASSY
001631
DATE
6-15-68
10-30-68
CHANGE NO
132
215
+5 VDC
A
C1
4.7UF
10V
GRD
J
TP4
ACTIVE DETENT
H
G
-GATED ATTENTION
L
F
R
M
-FORCE SEEK
Q
P
-RESET PRESENT ADDRESS COUNTER
C
-FIRST SEEK DETENT LOCKOUT
D
1C
2D
1B
2C
1A
2A
2B
3B
3A
TP2
TP3
TP1
K
TRANSDUCER ENABLE
E
B
-FIRST SEEK DETENT LOCKOUT
N
FIRST SEEK DETENT LOCKOUT
NOTES:UNLESS OTHERWISE SPECIFIED
1. IC1 IS SP670A
2. IC2 IS SP680A
3. IC3 IS SP659A
4. CONNECT ALL IC'S PIN TO GRD, PIN 8 TO + 5V
MATERIAL
NO.
CASE DEPTH
HARDNESS
SURFACE TREATMENT
001632
C
TOLERANCE UNLESS OTHERWISE NOTED
2 PLACE DEC ±
3 PLACE DEC ±
ANGLES ±
CORNERS AND/OR EDGES BROKEN
OUTSIDE MAX
INSIDE MAX
RADII UNLESS OTHERWISE NOTED
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION
NAME
SCHEMATIC DIAGRAM
LATCHES
DESIGN
DETAIL
CHECK
APPRO
TYPE
SCALE
NONE
DRAW
K.B.
6-15-68
CHECK
R.R.S.
25 Jun 68
K.R.S. 5/14/68
001632

001631

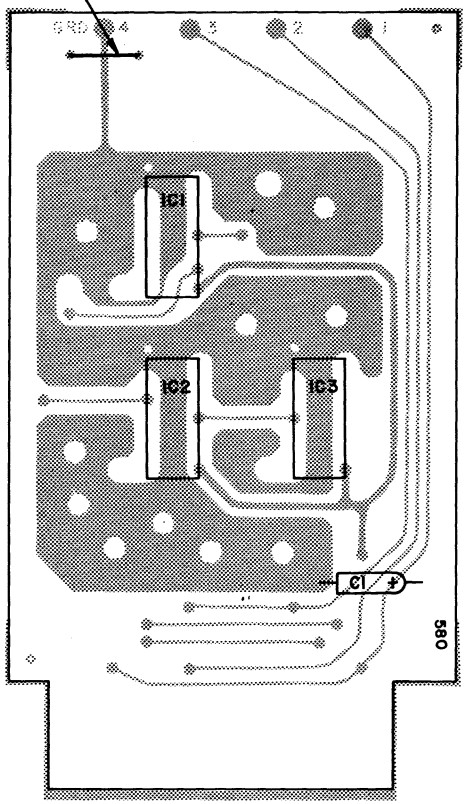
REF DESIG	DESCRIPTION	P.S.C. PART NO.
———	PRINTED CIRCUIT BOARD	001634
C1	CAPACITOR, 4.7UF, 10V ± 10%	151124
IC1	INTEG CIRCUIT, SP670A	150655
IC2	INTEG CIRCUIT, SP680A	150656
IC3	INTEG CIRCUIT, SP659A	150654
———	TAG, ENGINEERING CHG	200304

001631

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490-60 ~	6-15-68	132		
200495-50 ~	11-18-68	219		
	1-2-70	580		

001631

200304 [1]



001631

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001632	215
ARTMASTER	001633	580
FABRICATION	001634	580

NOTES: UNLESS OTHERWISE SPECIFIED

[1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER

2 COMPONENT HEIGHT NOT TO EXCEED .450

SEE B/M 001631

001631 C

Peripheral Systems Corporation

P.C. BOARD ASSEMBLY
LATCHES

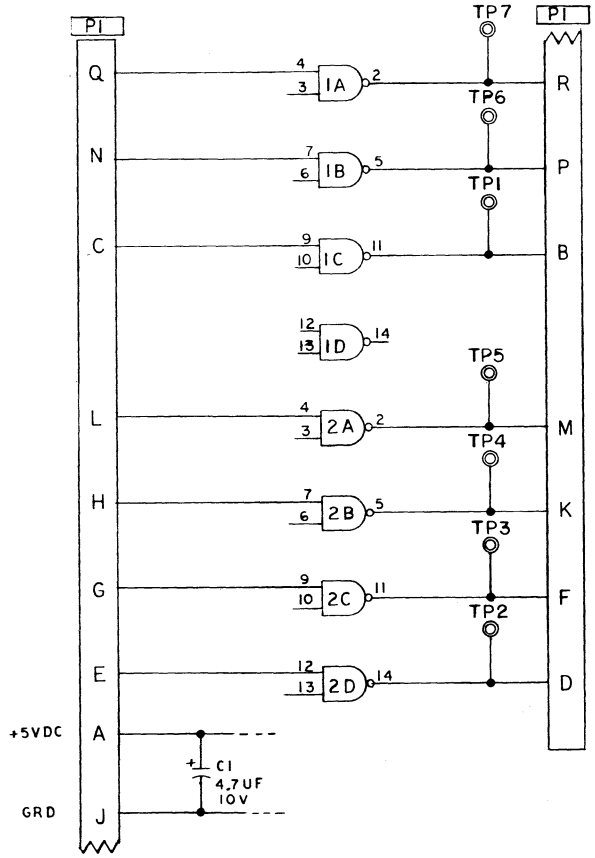
2 / 1

MCL 6/14/68 K.B. 6-15-68

001631

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001246	3/13/68	14		
	3/21/68	34		

001247



001247

NOTES; UNLESS OTHERWISE SPECIFIED
1. CONNECT PIN 1 OF ALL IC'S TO GRD
2. CONNECT PIN 8 OF ALL IC'S TO +5VDC
3. IC1 AND 2 ARE SP680A

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
CASE DEPTH			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM INVERTERS
HARDNESS			ANGLES ±	DESIGN	TYPE
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DETAIL	SCALE NONE
001247	C		INSIDE MAX	CHECK	DRAW EGG 12-18-67
		RADII UNLESS OTHERWISE NOTED		APPRO	CHECK VVE 12-20-67

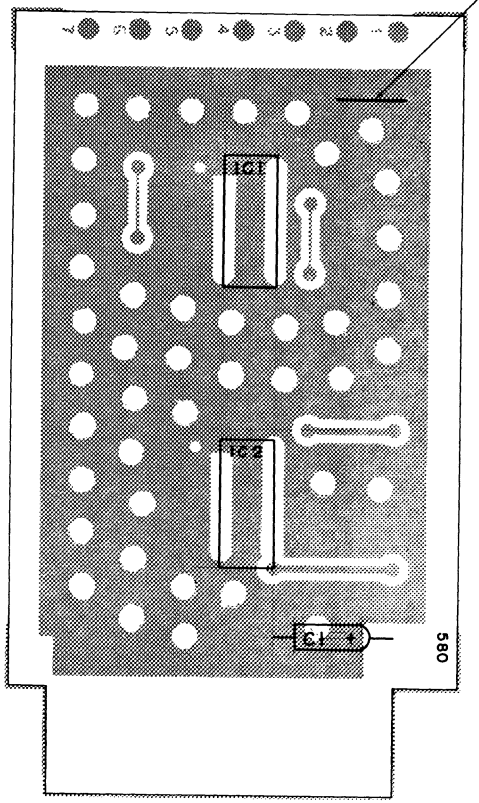
001247

001246

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200244	13 MAR 68	14		
	3/21/68	34		
	11-19-68	219		
	12-16-69	580		

REF DESIG	DESCRIPTION	P.S.C. PART NO.
———	PRINTED CIRCUIT BOARD	001249
C1	CAPACITOR-4.7 UF, 10V; ±10%	151124
IC1 & IC2	INTEGRATED CIRCUITS (SP680A)	150656
———	TAG - ENGINEERING CHANGE	200304

200304 [1]



001246

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001247	54
ARTMASTER	001248	550
FABRICATION	001249	580

NOTES: UNLESS OTHERWISE SPECIFIED:

1. [1] ENG. CHANGE TAG (200304) MUST REFLECT THE LATEST ENG. CHANGE NUMBER.
2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M	NO. 001246	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001246	C	RADII UNLESS OTHERWISE NOTED	

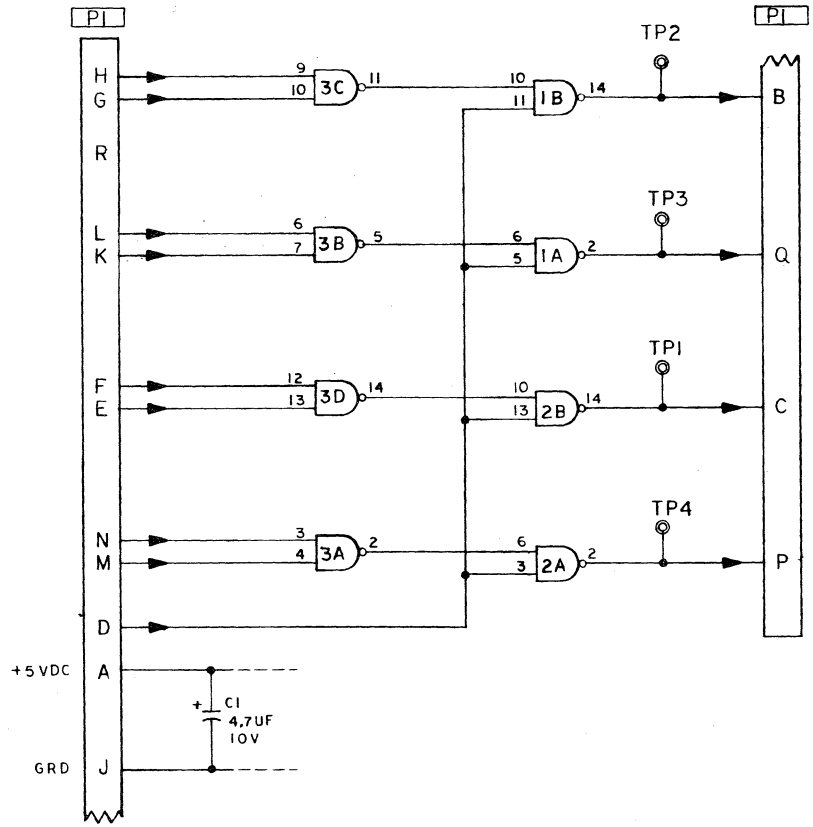
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME ASSEMBLY DRAWING
INVERTERS

DESIGN			TYPE	———	
DETAIL			SCALE	2/1	
CHECK	[illegible]	13 MAR 68	DRAW	HAB	1-22-68
APPRO	[illegible]	3-27-68	CHECK	R.J.E	1-25-68

001246

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001166	3/13/68	14		
	3/21/68	34		



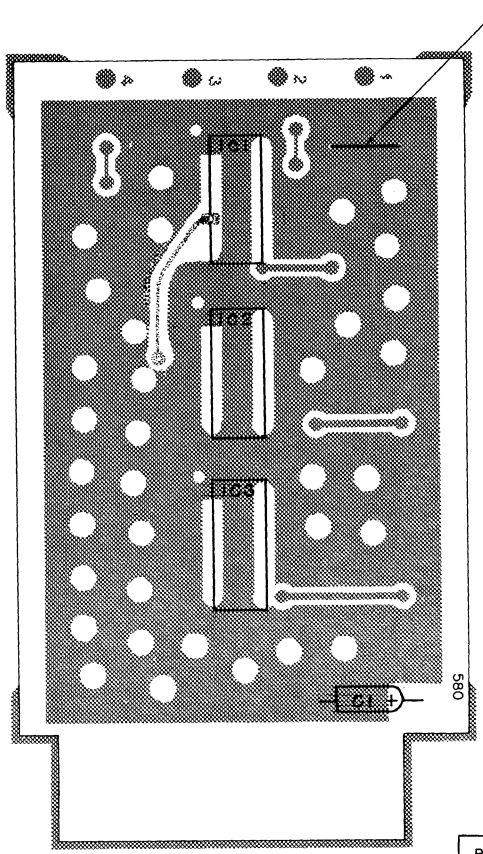
NOTES: UNLESS OTHERWISE SPECIFIED
1. CONNECT PIN 1 OF ALL IC'S TO GRD
2. CONNECT PIN 8 OF ALL IC'S TO +5VDC
3. IC1 AND 2 ARE SP659A
4. IC3 IS SP680A

001167

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
CASE DEPTH			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM
HARDNESS			ANGLES ±		4 BIT DRIVER
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN	TYPE
001167	C		INSIDE MAX	DETAIL	SCALE NONE
		RADII UNLESS OTHERWISE NOTED		CHECK	DRAW EGG 12/15/67
				APPRO	CHECK

REF DESIG	DESCRIPTION	P.S.C. PART NO.
———	PRINTED CIRCUIT BOARD	001169
C1	CAPACITOR - 4.7 UF, 10V; ±10%	151124
IC1 & IC2	INTEGRATED CIRCUITS (SP6594)	150654
IC3	INTEGRATED CIRCUIT (SP680A)	150656
———	ENGINEERING CHANGE TAG	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200244	13MAR68	14		
	5/21/68	34		
	11-19-68	219		
	12-16-69	580		



001166

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001167	54
ARTMASTER	001168	580
FABRICATION	001169	5-

NOTES: UNLESS OTHERWISE SPECIFIED:

/. ENG. CHANGE TAG (200304) MUST REFLECT THE LATEST ENG. CHANGE NUMBER.

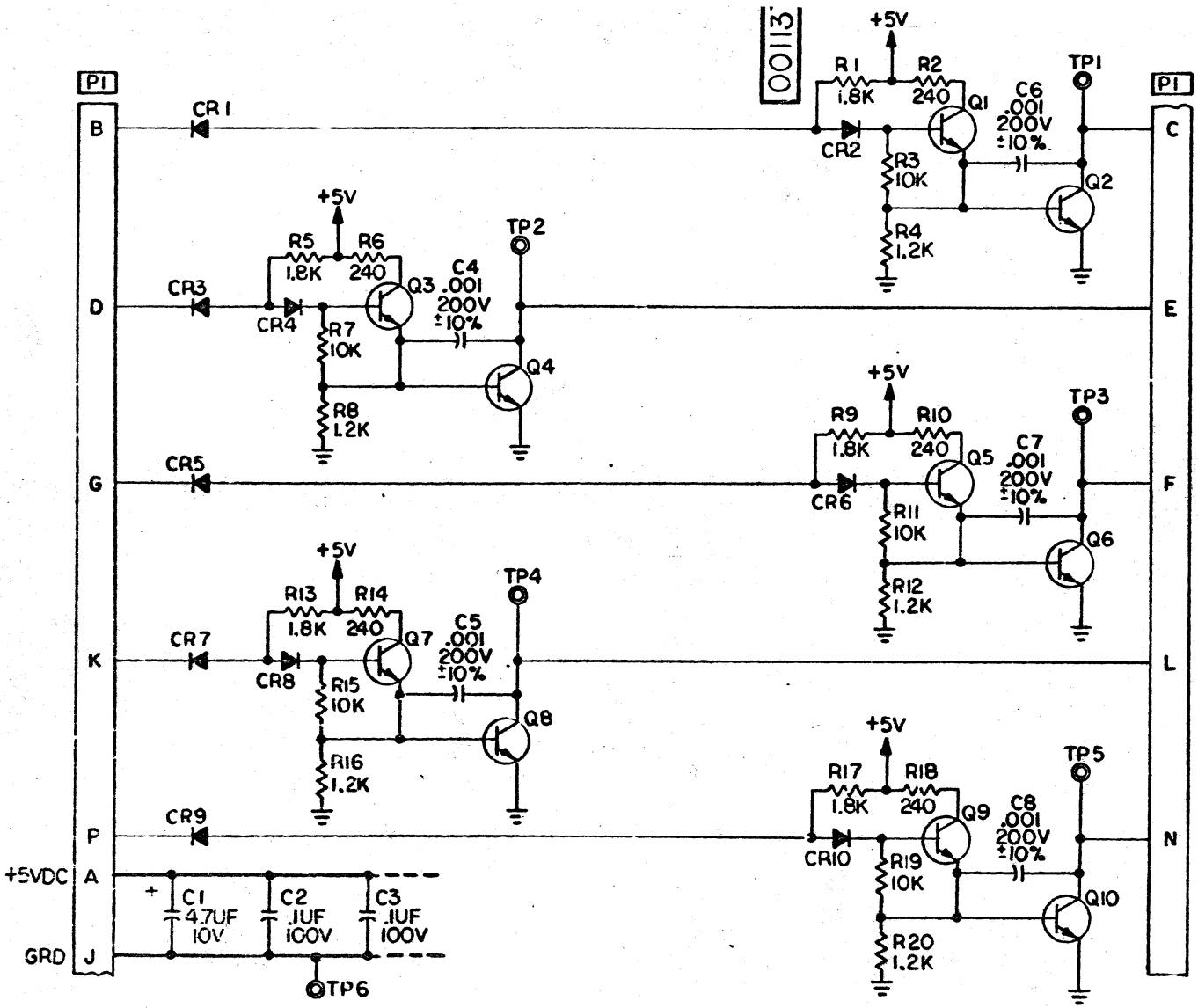
2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M	NO. 001166	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001166	C	RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	ASSEMBLY DRAWING 4 BIT DRIVER				
DESIGN			TYPE	———	
DETAIL			SCALE	2/1	
CHECK	RDX	13 MAR 68	DRAW	HAB	1-22-68
APPRO	RDX RJW	13 MAR 68 5-27-68	CHECK	R.D.E	1-25-68

001166



001137

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1/4W, ±5%
2. ALL DIODES ARE IN4148
3. ALL TRANSISTORS ARE 2N2222A
4. ALL CAPACITORS ARE IN MICROFARADS.

DATE	CHANGE NO.	DATE	CHANGE NO.	TECHNICAL APPROVAL
3-11-68	14			
8-26-68	34			
OCT, 70	1384			
JAN 70	1772			

MEMOREX EQUIPMENT GROUP

NAME: SCHEMATIC DIAGRAM
RELAY / LAMP DRIVER

DESIGN
DETAIL: 10-6-70
CHECK: OCT 70
APPRO: TEG 10/26/70

001137

001137

C

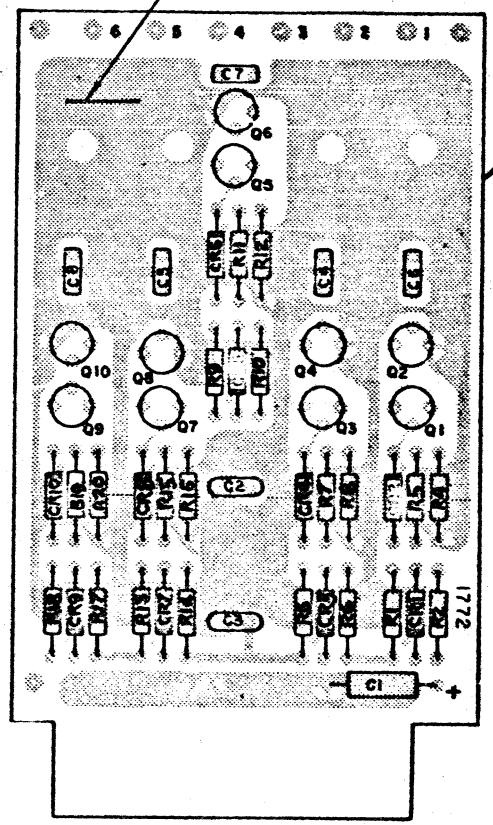
4 3 2 1

REF DESIG	DESCRIPTION	M. E. G. PART NO.
C1	CAPACITOR, T, 4.7MF, 10V, ± 10 %	151124
C2, 3	CAPACITOR, C, .1MF, 100V, ± 10 %	154151
C4,5,6,7,8	CAPACITOR, C, .001 MF, 200V, ± 10 %	154184
CR1 – 10	DIODE, IN4148	150834
R3,7,11, 15,19	RESISTOR, COMP, 10K, 1/4W, ±5%	151507
R1,5,9,13, 17	1.8K,	151489
R4,8,12, 16,20	1.2K,	151485
R2,6,10,14, 18	RESISTOR, COMP, 240Ω, 1/4W, ±5%	151468
Q1 – 10	TRANSISTOR, 2N2222A	150768
	TAG, ENGINEERING CHG	200304

001112

[1] 200304

[3] 001139



001136

REFERENCE DOCUMENTS		E.C. LEVEL
SCH DIAG	001137	1772
ARTMASTER	001138	1772

NOTES:

[1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER

2. COMPONENT HE 3HT NOT TO EXCEED .350

[3] P.C. BOARD 001139 MUST BE AT EC LEVEL 1772 .

4. MUST CONFORM TO ENG. SPEC. 001140 AT E.C. LEVEL 1384

001136

SEE B/M NO. 001136

C

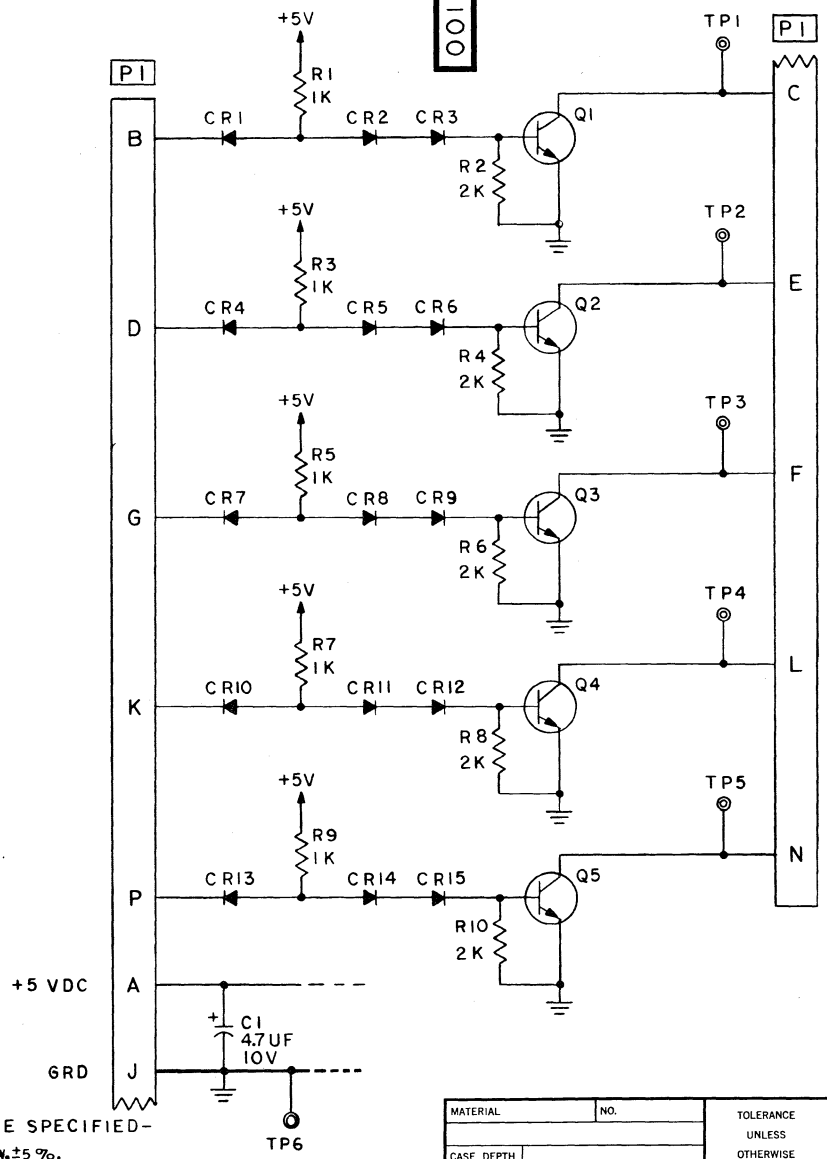
MEGATEK EQUIPMENT GROUP

P.C. BOARD ASSEMBLY
RELAY / LAMP DRIVER

2/1

001136

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001136	3/11/68	14		
	3-26-68	34		



NOTES: UNLESS OTHERWISE SPECIFIED-

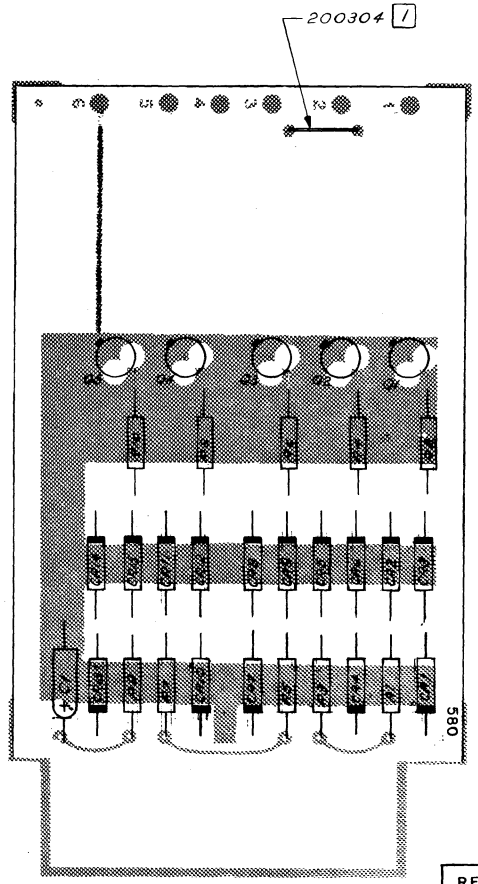
1. ALL RESISTORS IN OHMS, 1/4W, ±5%.
2. ALL DIODES ARE IN4148.
3. ALL TRANSISTORS ARE 2N3568.

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
CASE DEPTH			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM
HARDNESS			ANGLES ±		RELAY/LAMP DRIVERS
SURFACE TREATMENT		CORNERS AND OR EDGES BROKEN	OUTSIDE MAX	DESIGN JDM 3/12/68	TYPE
001137	C		INSIDE MAX	DETAIL	SCALE NONE
		RADII UNLESS OTHERWISE NOTED		CHECK 3/11/68	DRAW WGR 6 MAR 68
				APPRO	CHECK

001137

REF DESIG	DESCRIPTION	P.S.C. PART NO.
——	PRINT CIRCUIT BOARD	001139
C1	CAPACITOR, 4.7 UF 10V, ±10%	151124
CR1-CR15	DIODES, (IN4148)	150834
Q1-Q5	TRANSISTORS (2N3568)	150730
R1,R3, R5, R7 R9	RESISTOR, COMP, 1K 1/4W, ±5%	151483
R2,R4,R6, R8, R10	RESISTOR, COMP, 2K 1/4W, ±5%	151490
——	TAG, ENG. CHANGE	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200244	2/MAR/68	14		
	3/21/68	34		
	11-19-68	219		
	12/16/69	580		



001136

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001137	34
ARTMASTER	001138	580
FABRICATION	001139	580

NOTES: UNLESS OTHERWISE SPECIFIED:

/1 ENG. CHANGE TAG (200304) MUST REFLECT THE LATEST ENG. CHANGE NUMBER.

2 COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M	NO. 001136	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC
CASE DEPTH			ANGLES
HARDNESS		CORNERS AND OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001136	C	RADII UNLESS OTHERWISE NOTED	

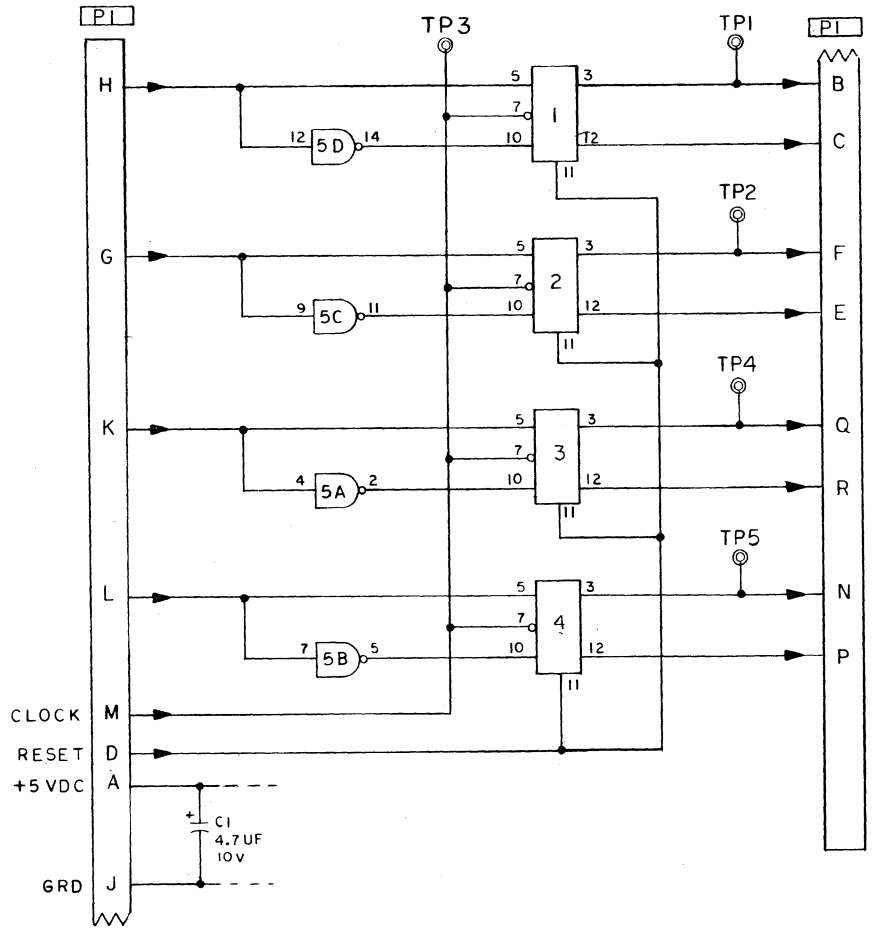
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	ASSEMBLY DRAWING			
	RELAY LAMP DRIVERS			
DESIGN	JDM	3/12/68	TYPE	
DETAIL			SCALE	2/1
CHECK			DRAW	TCM 1-22-68
APPRO	JDM W/W	3/12/68 5-27-68	CHECK	R.D.E 1-24-68

001136

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001156	3/14/68	14		
	3/21/68	34		

001157



001157

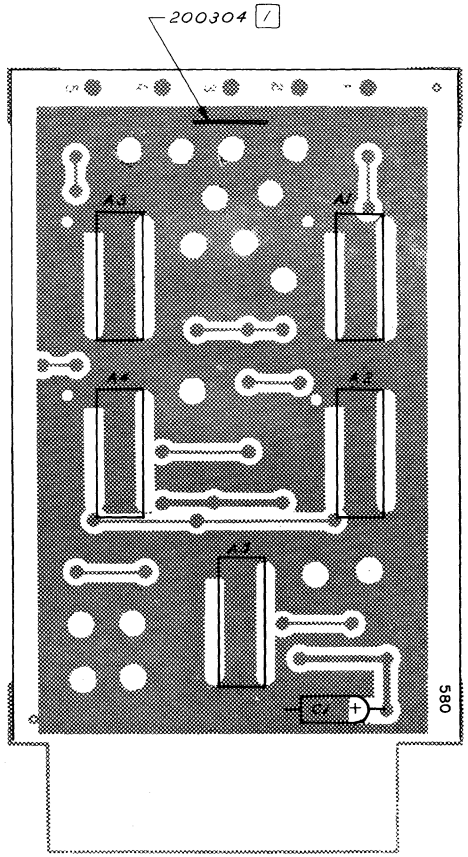
NOTES: UNLESS OTHERWISE SPECIFIED
1. CONNECT PIN 1 OF ALL IC'S TO GRD
2. CONNECT PIN 8 OF ALL IC'S TO +5VDC
3. IC1, 2, 3 AND 4 ARE SP620A
4. IC5 IS SP680A

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION
			3 PLACE DEC ±	NAME SCHEMATIC DIAGRAM
CASE DEPTH			ANGLES ±	J-K REGISTER, 4 BIT
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN TYPE
SURFACE TREATMENT			INSIDE MAX	DETAIL SCALE NONE
001157	C	RADII UNLESS OTHERWISE NOTED		CHECK DRAW EGG 12/15/67
				APPRO 3/14/68 CHECK P.D.E. 14 MAR 68

001157

REF DESIG	DESCRIPTION	P.S.C. PART NO.
——	PRINTED CIRCUIT BOARD	001159
C1	CAPACITOR, 4.7 UF, 10V, ± 10%	151124
IC1 - IC4	INTEGRATED CIRCUIT(SP620A)	150651
IC5	INTEGRATED CIRCUIT(SP680A)	150656
——	TAG, ENG CHANGE	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200244	1/4/68	14		
	3/21/68	34		
	11-19-68	219		
	12/10/69	580		



001156

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001157	34
ARTMASTER	001158	580
FABRICATION	001159	580

NOTES: UNLESS OTHERWISE SPECIFIED:

1. ENG. CHANGE TAG(200304) MUST REFLECT THE LATEST ENG. CHANGE NUMBER.
2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M	NO. 001156	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES °
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001156	C	RADII UNLESS OTHERWISE NOTED	

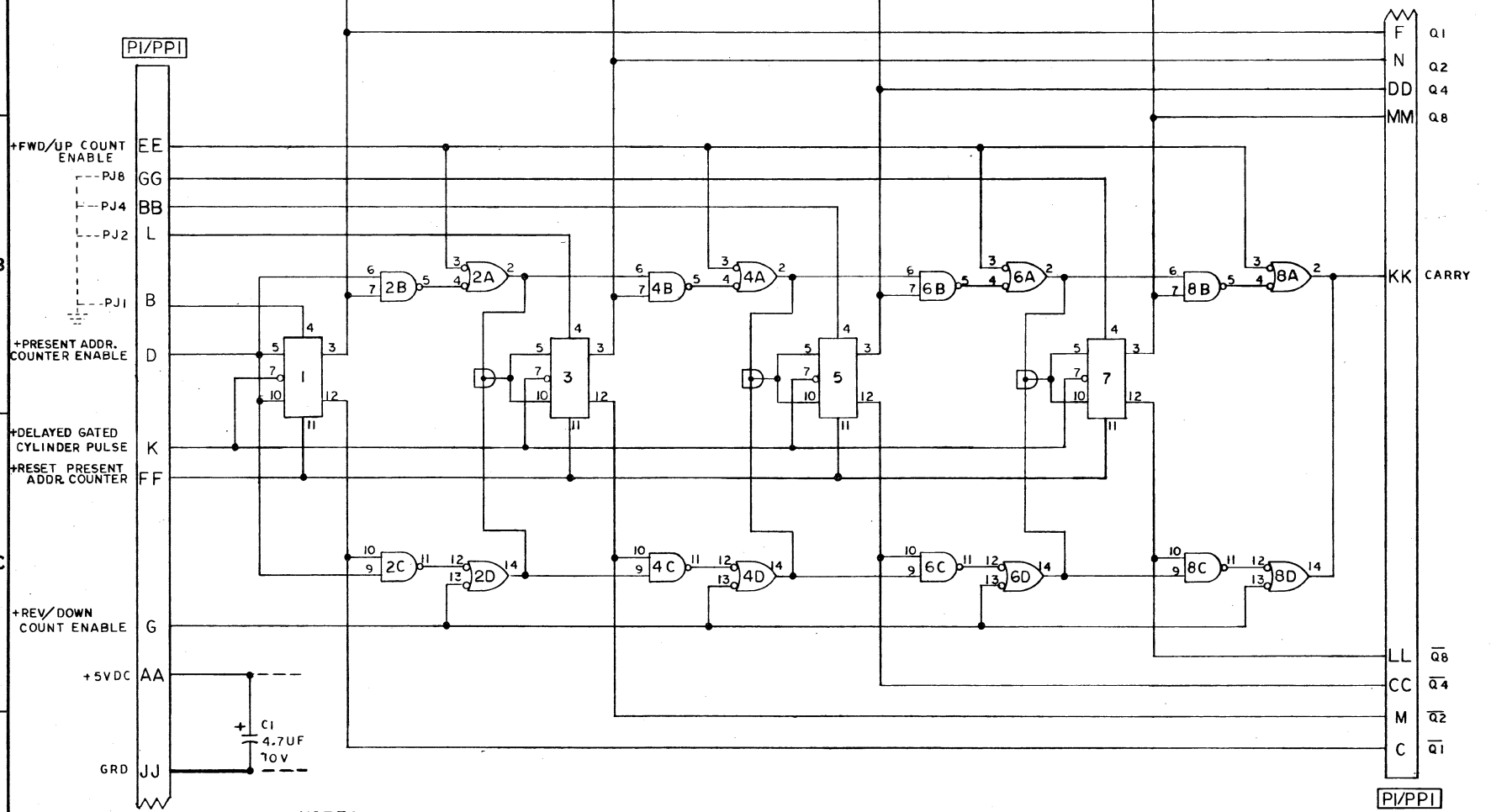
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	ASSEMBLY DRAWING				
	J-K REGISTER, 4 BIT				
DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK	TDK	14 JAN 68	DRAW	TCM	1-22-68
APPRO	TDK WJW	14 JAN 68 3-27-68	CHECK	RBE	1-24-68

001156

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001186	3/19/68	14		
	3-21-68	34		
	6-18-68	86		

001187



NOTES: UNLESS OTHERWISE SPECIFIED
1. CONNECT PIN 1 OF ALL IC'S TO GRD
2. CONNECT PIN 8 OF ALL IC'S TO +5VDC
3. IC1, 3, 5 AND 7 ARE SP620A
4. IC2, 4, 6 AND 8 ARE SP680A

MATERIAL	NO.
CASE DEPTH	
HARDNESS	
SURFACE TREATMENT	

001187 C

TOLERANCE UNLESS OTHERWISE NOTED
CORNERS AND/OR EDGES BROKEN
RADII UNLESS OTHERWISE NOTED

2 PLACE DEC ±	
3 PLACE DEC ±	
ANGLES ±	
OUTSIDE MAX	
INSIDE MAX	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

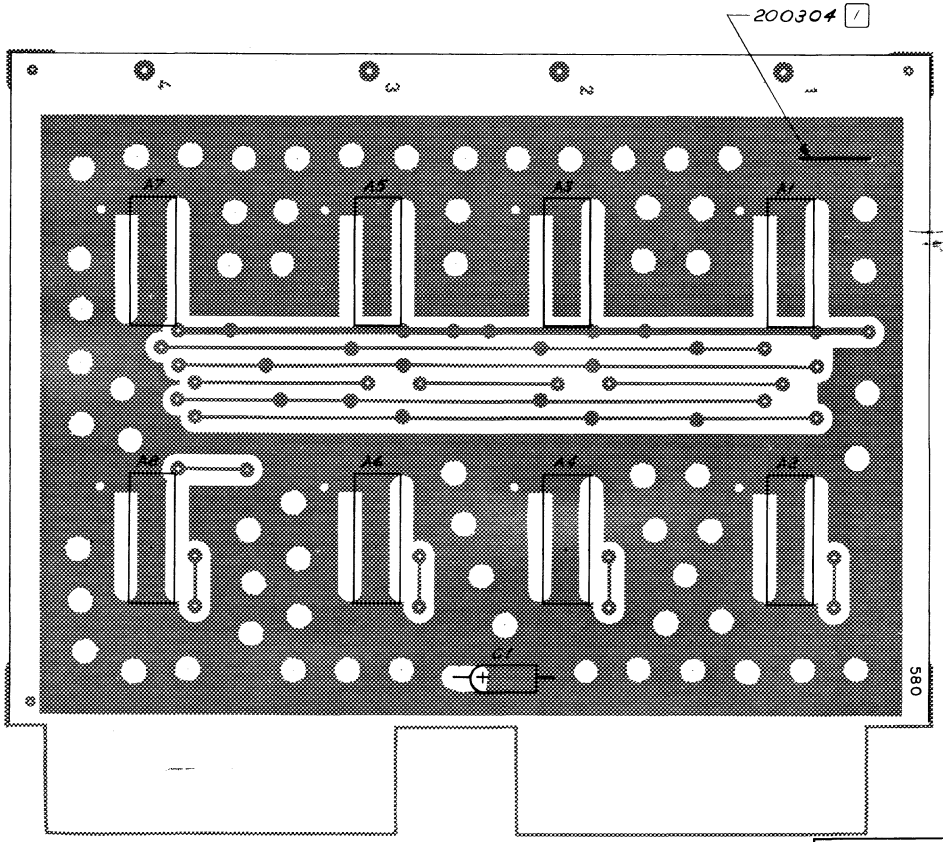
NAME SCHEMATIC DIAGRAM
UP/DOWN COUNTER

DESIGN			TYPE		
DETAIL			SCALE	NONE	
CHECK	[illegible]	3/19/68	DRAW	EGG	12/20/67
APPRO	[illegible]	3/28/68	CHECK		

001187

REF DESIG	DESCRIPTION	P.S.C. PART NO.
——	PRINTED CIRCUIT BOARD	001189
C1	CAPACITOR, 4.7 UF, 10V, ±10%	151124
IC2, IC4 IC6, IC8	INTEGRATED CIRCUIT (SP680A)	150656
IC1, IC3, IC5, IC7	INTEGRATED CIRCUIT (SP620A)	150651
——	TAG, ENG. CHANGE	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490-60	19 MARCH 68	14		
200495-50	3/21/68	34		
	6-18-68	86		
	11-19-68	219		
	12-16-69	580		



001186

NOTES: UNLESS OTHERWISE SPECIFIED:
1. / ENG CHANGE TAG (200304) MUST REFLECT THE LATEST ENG. CHANGE NUMBER.
2. COMPONENT HEIGHT NOT TO EXCEED .350

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001187	86
ARTMASTER	001188	580
FABRICATION	001189	580

MATERIAL SEE B/M	NO. 001186	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001186	C	RADII UNLESS OTHERWISE NOTED	

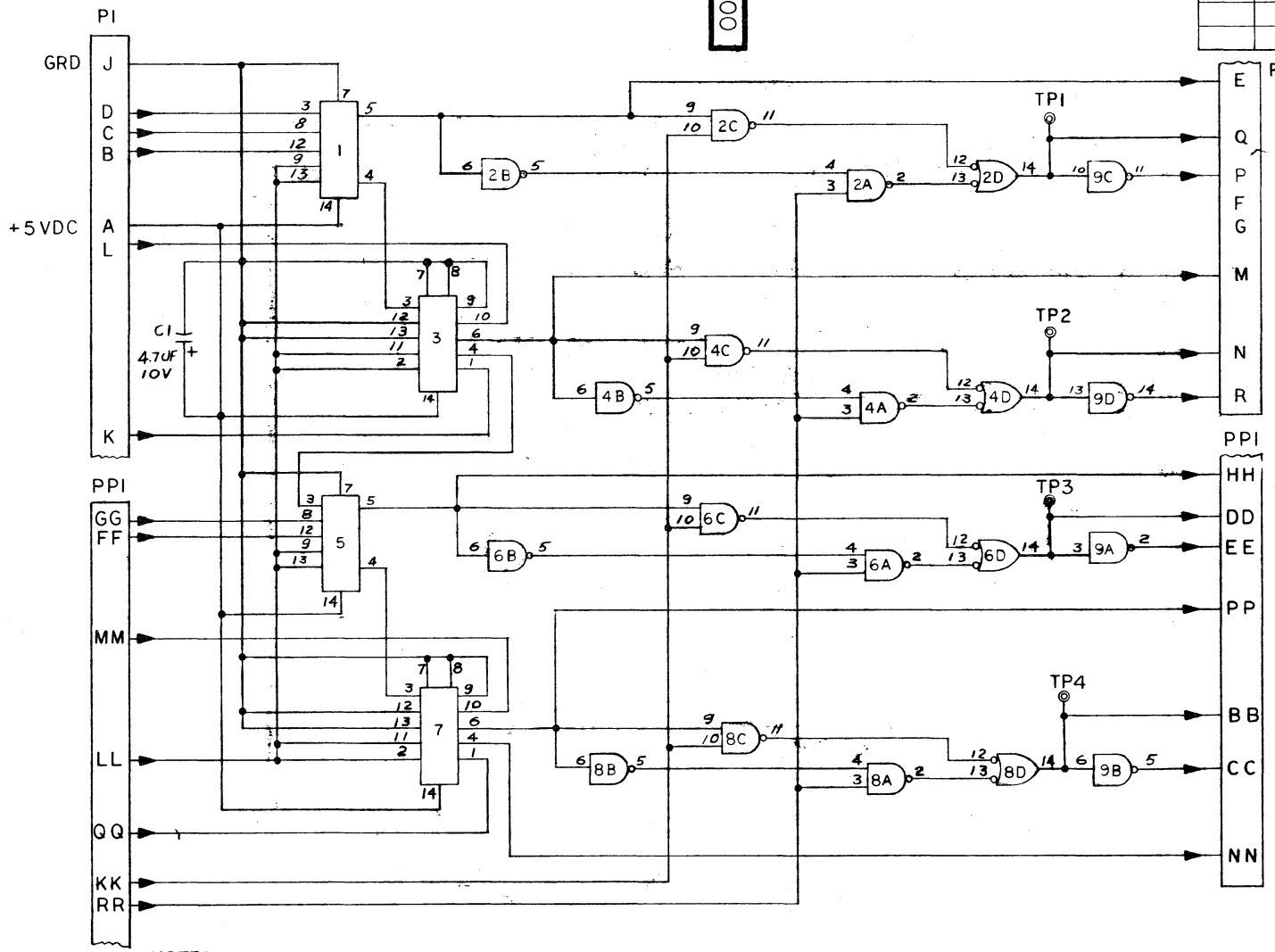
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME ASSEMBLY DRAWING
UP-DOWN COUNTER

DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK	[illegible]	20 DEC 68	DRAW	TCM	1-24-68
APPRO	[illegible]	20 DEC 68 5-27-68	CHECK	[illegible]	1-25-68

001186

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001196	2/15/68	14		
	3/20/68	34		



NOTES: UNLESS OTHERWISE SPECIFIED
1. IC2, 4, 6, 8 AND 9 CONNECT PIN 1 TO GRD
2. IC2, 4, 6, 8 AND 9 CONNECT PIN 8 TO +5VDC
3. IC1, 3, 5 AND 7 ARE SN7480N
4. IC2, 4, 6, 8 AND 9 ARE SP680A

001197

001197

001197

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM ADDER
CASE DEPTH			ANGLES ±	DESIGN	TYPE
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DETAIL	SCALE NONE
SURFACE TREATMENT			INSIDE MAX	CHECK	DRAW EGG 12-6-67
001197	C	RADII UNLESS OTHERWISE NOTED		APPRO	CHECK

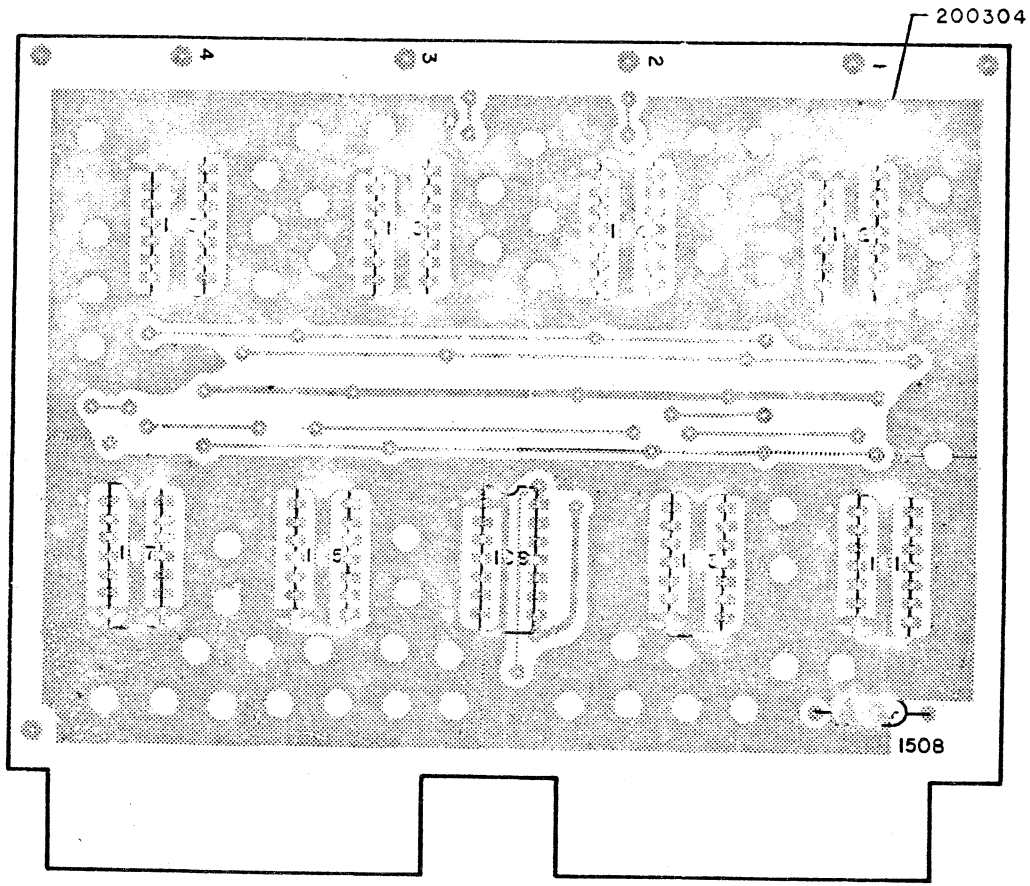
001196

	14	Oct 70	1508
	34		
	219		
	580		

001196
RELEASED FOR ASSEMBLY
200244

001100

REF DESIG	DESCRIPTION	M E G PART NO.
———	PRINTED CIRCUIT BOARD	001199
C1	CAPACITOR,T,4.7UF,10V,±10%	151124
IC1,IC3, IC5,IC7	INTEGRATED CIRCUIT,SN7480N	150661
IC2,IC4 IC6,IC8, IC9	INTEGRATED CIRCUIT,SP680A	150656
——	TAG ENGRG. CHANGE	200304



001196

NOTES:

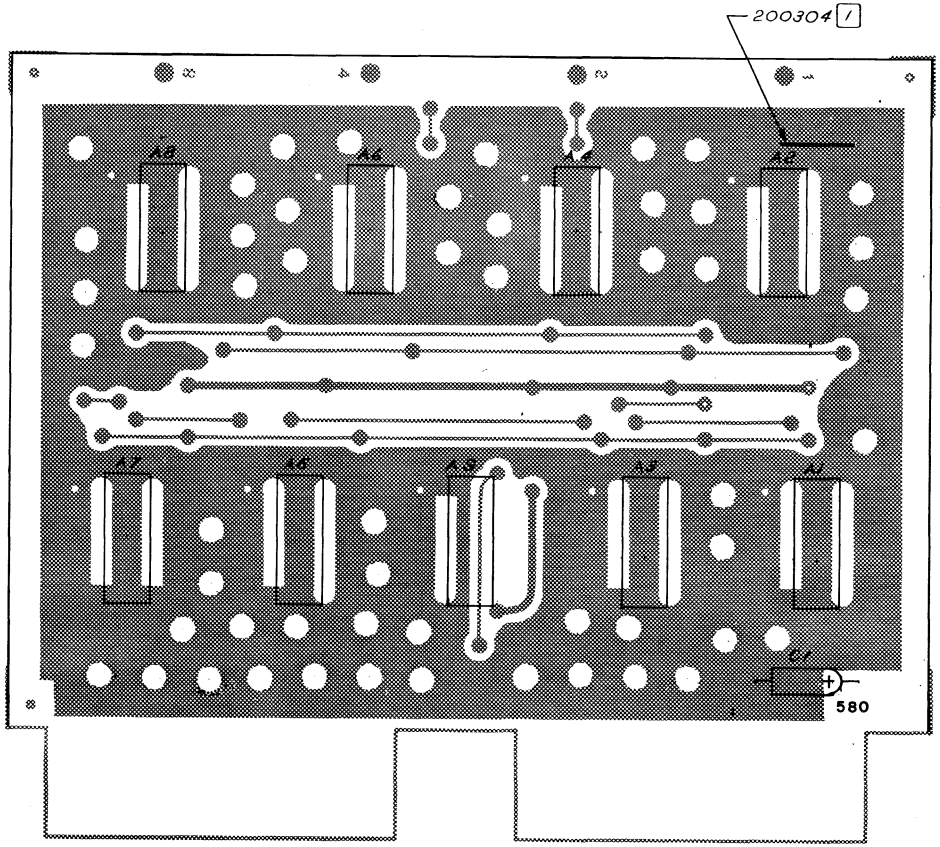
[1] ENGRG CHANGE TAG (200304) MUST REFLECT THE LATEST ENGRG CHANGE NUMBER.
2. COMPONENT HEIGHT NOT TO EXCEED .350.

REFERENCE	DOCUMENTS	E.C. LEVEL
SCH. DIAG.	001197	34
ART. MASTER	001198	1508
FABRICATION	001199	1508
ENGRG SPEC	———	———

MATERIAL NO SEE E/M 001196	MUST CONFORM TO ENG. SPEC 880000	TOLERANCE UNLESS OTHERWISE NOTED	MEMOREX EQUIPMENT GROUP
CASE DEPTH	TECHNICAL APPROVAL	LINEAR ±	NAME P.C. BOARD ASSEMBLY ADDER
HARDNESS		ANGULAR ±	
SURFACE TREATMENT		CORNERS AND OR EDGES BROKEN	DESIGN
STD CODE C		ONTSIDE MAX	DETAIL A.O. Oct 70 SCALE 2/1
		INSIDE MAX	CHECK
			APPRO 001196

REF DESIG	DESCRIPTION	P.S.C. PART NO.
—	PRINTED CIRCUIT BOARD	001199
C1	CAPACITOR, 4.7UF, 10V, ±10%	151124
IC1, IC3,	INTEGRATED CURCUIT(SN7480N)	150661
IC5, IC7		
IC2, IC4, IC6,	INTEGRATED CIRCUIT(SP680A)	150656
IC8, IC9		
—	TAG, ENG. CHANGE	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200244	15MAR68	14		
	3/21/68	34		
	11-19-68	219		
	1-2-70	580		



001196

NOTES: UNLESS OTHERWISE SPECIFIED:

/ ENG. CHANGE TAG (200304) MUST REFLECT THE LATEST ENG. CHANGE NUMBER.

2. COMPONENT HEIGHT NOT TO EXCEED .350

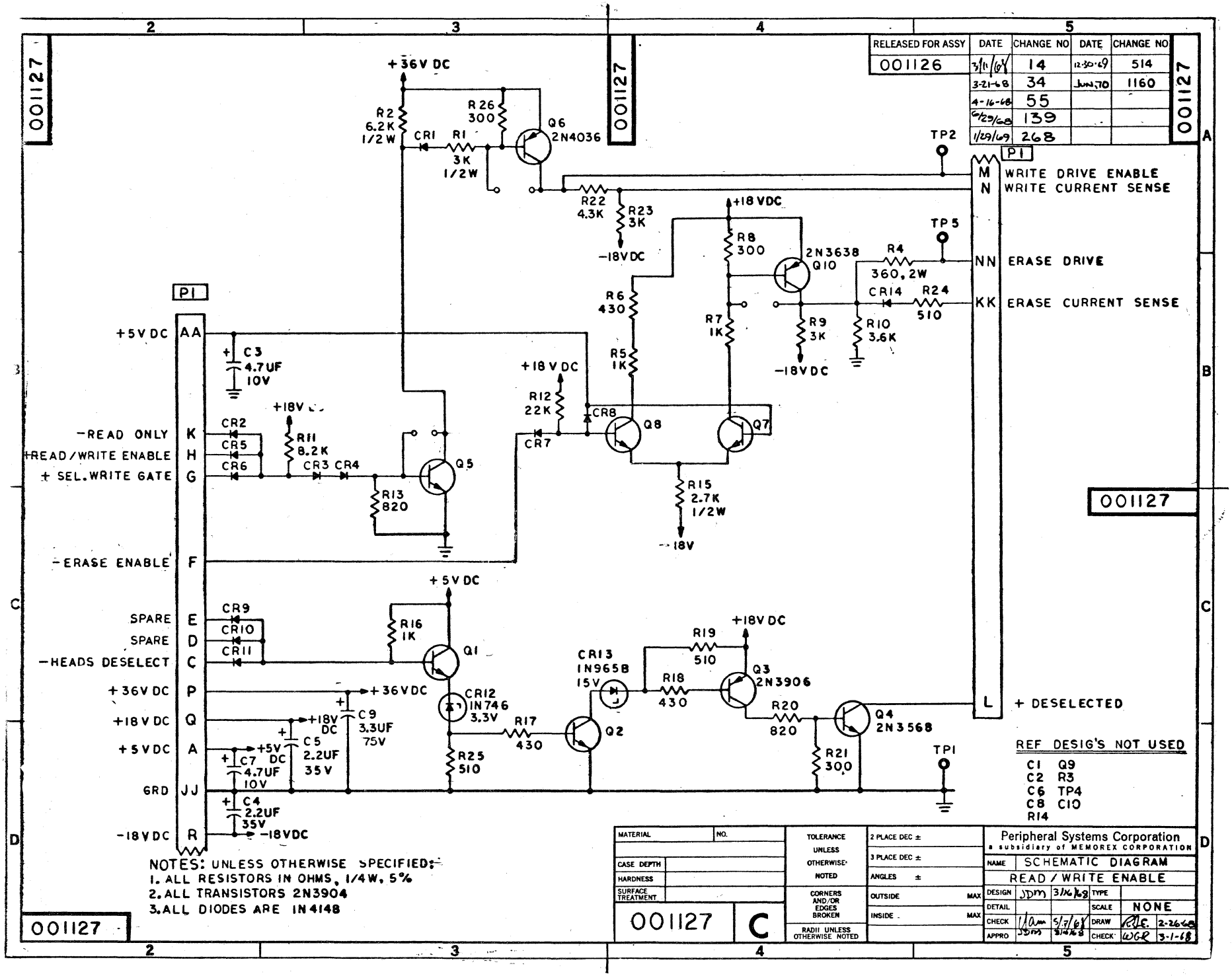
REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001197	34
ARTMASTER	001198	580
FABRICATION	001199	580

MATERIAL SEE B/M	NO. 001196	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001196	C	RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	ASSEMBLY DRAWING		
	ADDER		
DESIGN		TYPE	
DETAIL		SCALE	2/1.
CHECK	DOK 15MAR68	DRAW	TCM 1-22-68
APPRO	DOK 15MAR68 3-27-68	CHECK	RJC 15MAR68

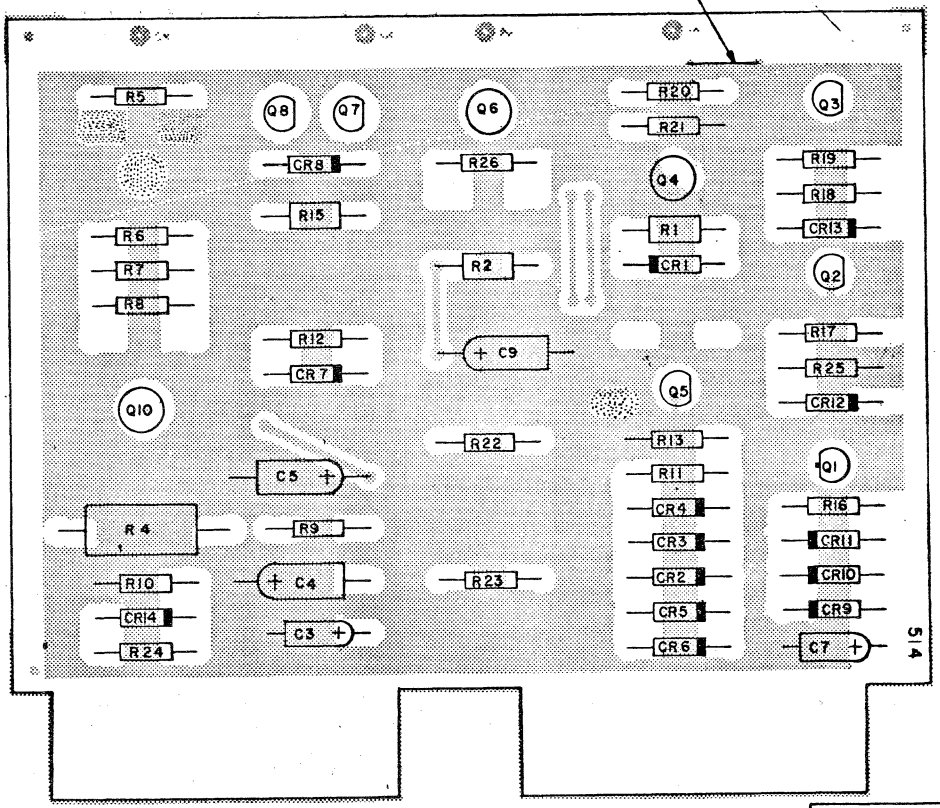
001196


001127
RELEASED FOR ASSY
001126
DATE
CHANGE NO
3/11/68 14
3-21-68 34
4-16-68 55
6/29/68 139
1/29/69 268
12-30-69 514
Jun 70 1160
+36V DC
R2 6.2K 1/2W
CR1
R1 3K 1/2W
R26 300
Q6 2N4036
TP2
P1
M WRITE DRIVE ENABLE
N WRITE CURRENT SENSE
R22 4.3K
R23 3K
-18VDC
+18VDC
R8 300
2N3638 Q10
TP5
R4 360, 2W
NN ERASE DRIVE
CR14
R24 510
KK ERASE CURRENT SENSE
R6 430
R7 1K
R9 3K
R10 3.6K
R5 1K
+5V DC AA
C3 4.7UF 10V
+18V DC
R12 22K
CR8
Q8
Q7
CR7
-READ ONLY K
+READ/WRITE ENABLE H
± SEL. WRITE GATE G
CR2
CR5
CR6
R11 8.2K
CR3 CR4
Q5
R13 820
R15 2.7K 1/2W
-18V
-ERASE ENABLE F
+5V DC
SPARE E
SPARE D
-HEADS DESELECT C
CR9
CR10
CR11
R16 1K
Q1
+36V DC P
+18V DC Q
+5V DC A
GRD JJ
-18VDC R
CR12 IN746 3.3V
C9 3.3UF 75V
C5 2.2UF 35V
C7 4.7UF 10V
C4 2.2UF 35V
R17 430
R25 510
CR13 IN965B 15V
R19 510
+18V DC
Q3 2N3906
R18 430
R20 820
Q4 2N3568
R21 300
TPI
L + DESELECTED
REF DESIG'S NOT USED
C1 Q9
C2 R3
C6 TP4
C8 C10
R14
NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS IN OHMS, 1/4W, 5%
2. ALL TRANSISTORS 2N3904
3. ALL DIODES ARE IN4148
MATERIAL
NO.
CASE DEPTH
HARDNESS
SURFACE TREATMENT
001127
C
TOLERANCE UNLESS OTHERWISE NOTED
2 PLACE DEC ±
3 PLACE DEC ±
ANGLES ±
CORNERS AND/OR EDGES BROKEN
OUTSIDE MAX
INSIDE MAX
RADII UNLESS OTHERWISE NOTED
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION
NAME SCHEMATIC DIAGRAM
READ / WRITE ENABLE
DESIGN JDM 3/16/68
DETAIL
CHECK 1/10am 5/7/68
APPRO
TYPE
SCALE NONE
DRAW R.L.E. 2-26-68
CHECK WGR 3-1-68

REF DESIG	DESCRIPTION	P.S.C. PART NO.
——	PRINTED CIRCUIT BOARD	001129
C3, C7	CAPACITOR, 4.7UF, 10V, ±10%	151124
C4, C5	CAPACITOR, 2.2UF, 35V, ±10%	151127
C9	CAPACITOR, 3.3UF, 75V. ±20%	51152
CR1 - CR11,	DIODES, (IN4148)	150834
CR14		
CR12	DIODES, (ZENER IN746)	150827
CR13	DIODES, (ZENER IN965B)	150833
Q1, Q2, Q5	TRANSISTOR (2N3904)	150735
Q7, Q8		
Q3,	TRANSISTOR (2N3906)	150736
Q4	TRANSISTOR (2N3568)	150730
Q6	TRANSISTOR (2N4036)	150737
Q10	TRANSISTOR (2N3638)	150731
R1	RESISTOR, 3K, 1/2W, ±5%	151638
R2	RESISTOR, 6.2K, 1/2W, ±5%	151646
R4	RESISTOR, 360Ω, 2W, ±5%	151880
R5, R7, R16	RESISTOR, 1K, 1/4W, ±5%	151483
R6, R17, R18	RESISTOR, 430Ω, 1/4W, ±5%	151474
R8, R21, R26	RESISTOR, 300Ω, 1/4W, ±5%	151470
R10	RESISTOR, 3.6K, 1/4W, ±5%	151496
R11	RESISTOR, 8.2K, 1/4W, ±5%	151505
R12	RESISTOR, 22K, 1/4W, ±5%	151515
R13, R20	RESISTOR, 820Ω, 1/4W, ±5%	151481
R15	RESISTOR, 2.7K, 1/2W, ±5%	151637
R19, R24	RESISTOR, 510Ω, 1/4W, ±5%	151476
R25		
R22	RESISTOR, 4.3K, 1/4W, ±5%	151498
R9, R23	RESISTOR, 3K, 1/4W, ±5%	151434
——	ENG. CHANGE TAG	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490-60~	3-15-68	14	1-29-69	268
200495-50~	3/14/68	34	11-18-68	219
	4-16-68	55	2-31-69	514
	6/29/68	139	JUN.70	1160
	9/13/68	196		

200304 [1.]



001126

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001127	1160
ARTMASTER	001128	514.
FABRICATION	001129	514

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350
3. Q6 HEIGHT NOT TO EXCEED .310

MATERIAL SEE B/M	NO. 001126	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001126	C	RADII UNLESS OTHERWISE NOTED	

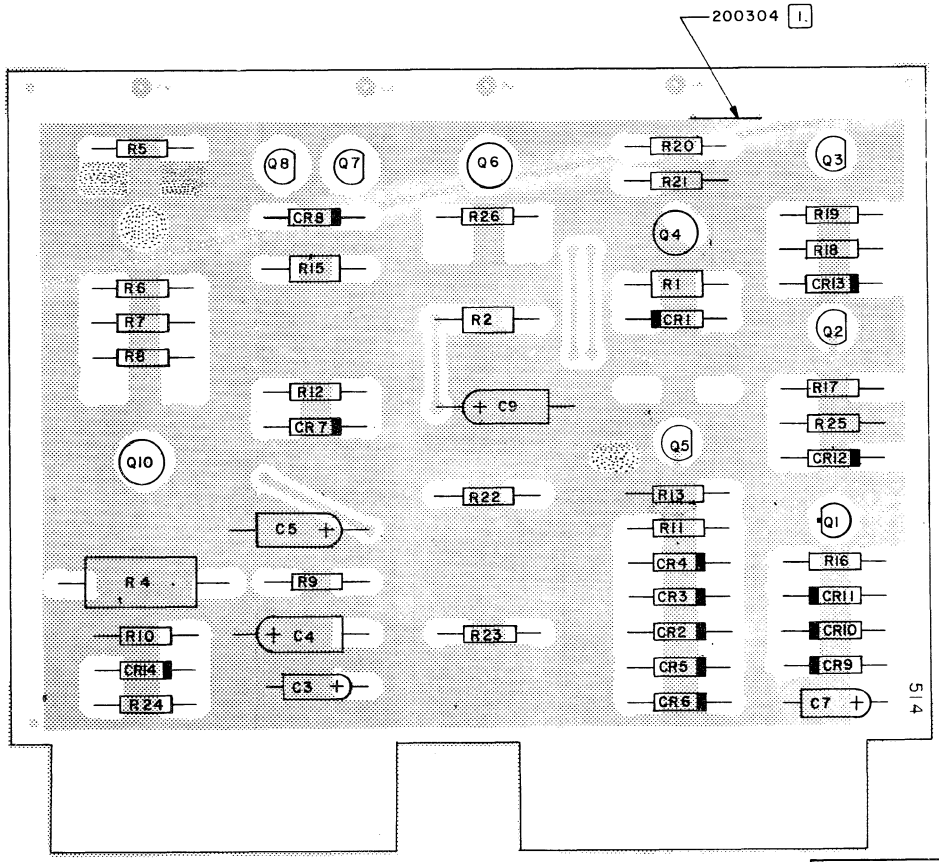
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	ASSEMBLY DRAWING				
	READ/WRITE ENABLE				
DESIGN	JDM	3/14/68	TYPE		
DETAIL			SCALE	2/1	
CHECK	[illegible]	5/7/68	DRAW	T.C.M.	3-12-68
APPRO	JDM w/pd	3/14/68 3-27-68	CHECK	[illegible]	15 MAY 68

001126

REF DESIG	DESCRIPTION	P.S.C. PART NO.
——	PRINTED CIRCUIT BOARD	001129
C3,C7	CAPACITOR, 4.7UF, 10V, ±10%	151124
C4, C5	CAPACITOR, 2.2UF, 35V, ±10%	151127
C9	CAPACITOR, 3.3UF. 75V. ± 20%	151132
CR1 - CR11,	DIODES, (IN4148)	150834
CR14		
CR12	DIODES, (ZENER IN746)	150827
CR13	DIODES, (ZENER IN965B)	150833
Q1, Q2, Q5	TRANSISTOR (2N3904)	150735
Q7, Q8		
Q3,	TRANSISTOR (2N3906)	150736
Q4	TRANSISTOR (2N3568)	150730
Q6	TRANSISTOR (2N4036)	150737
Q10	TRANSISTOR (2N3638)	150731
R1	RESISTOR, 3K, 1/2W, ±5%	151638
R2	RESISTOR, 6.2K, 1/2W, ±5%	151646
R4	RESISTOR, 360Ω 2W, ±5%	151380
R5 R7, R1	RESISTOR, 1K, 1/4W, ±5%	151483
R6, R17, R18	RESISTOR, 430Ω, 1/4W, ±5%	151474
R8, R21, R26	RESISTOR, 300Ω, 1/4W, ±5%	151470
R10	RESISTOR, 3.6K, 1/4W, ±5%	151496
R11	RESISTOR, 8.2K, 1/4W, ±5%	151505
R12	RESISTOR, 22K, 1/4W, ±5%	151515
R13, R20	RESISTOR, 820Ω, 1/4W, ±5%	151481
R15	RESISTOR, 2.7K, 1/2W, ±5%	151637
R19, R24	RESISTOR, 510Ω 1/4W, ±5%	151476
R25		
R22	RESISTOR, 4.3K, 1/4W, ±5%	151498
R9, R23	RESISTOR, 3K, 1/4W, ±5%	151494
——	ENG. CHANGE TAG	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490-60~	3-15-68	14	1-29-69	268
200495-50~	3/22/68	34	11-18-68	219
	4-16-68	55	2-31-69	514
	6/29/68	139		
	5/13/68	196		



001126

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001127	514
ARTMASTER	001128	514
FABRICATION	001129	514

NOTES: UNLESS OTHERWISE SPECIFIED

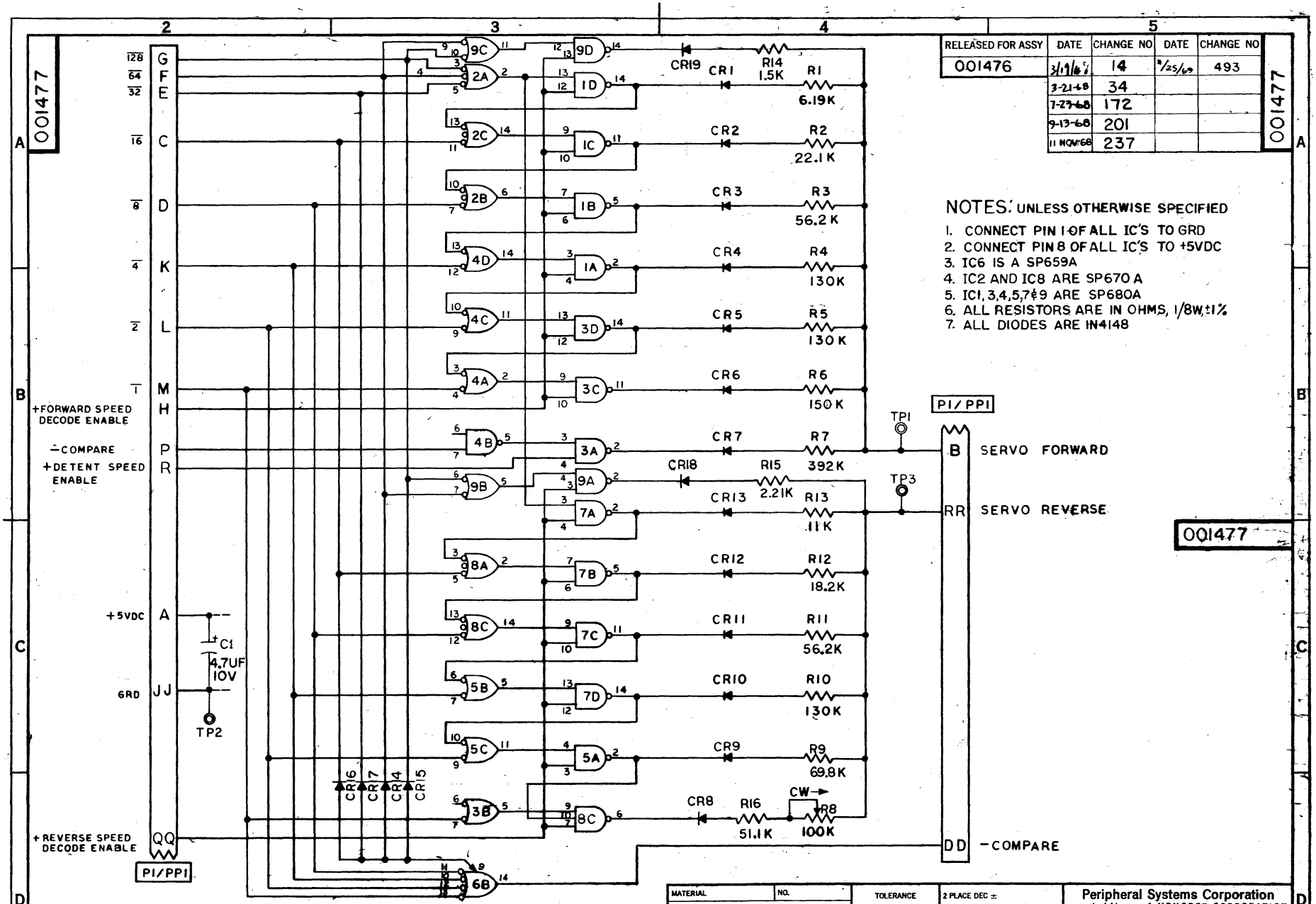
1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M	NO. 001126	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS			OUTSIDE MAX
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	INSIDE MAX
001126	C	RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	ASSEMBLY DRAWING			
	READ/WRITE ENABLE			
DESIGN	JDM	3/16/68	TYPE	
DETAIL			SCALE	2/1
CHECK	[illegible]	5/7/68	DRAW	T.C.M. 3-12-68
APPRO	JDM W/AW	3/16/68 3-27-68	CHECK	R.O.E. 15MAR68

001126



NOTES: UNLESS OTHERWISE SPECIFIED

1. CONNECT PIN 1 OF ALL IC'S TO GRD
2. CONNECT PIN 8 OF ALL IC'S TO +5VDC
3. IC6 IS A SP659A
4. IC2 AND IC8 ARE SP670A
5. IC1, 3, 4, 5, 7 & 9 ARE SP680A
6. ALL RESISTORS ARE IN OHMS, 1/8W, ±1%
7. ALL DIODES ARE IN4148

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001476	3/1/68	14	8/25/69	493
	3-21-68	34		
	7-27-68	172		
	9-13-68	201		
	11 NOV 68	237		

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
CASE DEPTH			3 PLACE DEC ±
HARDNESS			ANGLES ±
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
001477	C	RADII UNLESS OTHERWISE NOTED	INSIDE MAX

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	SCHMATIC DIAGRAM				
	FWD/REV SPEED DECODER				
DESIGN			TYPE		
DETAIL			SCALE	NONE	
CHECK		3/19/68	DRAW	R.D.E.	
APPRO			CHECK		

001477

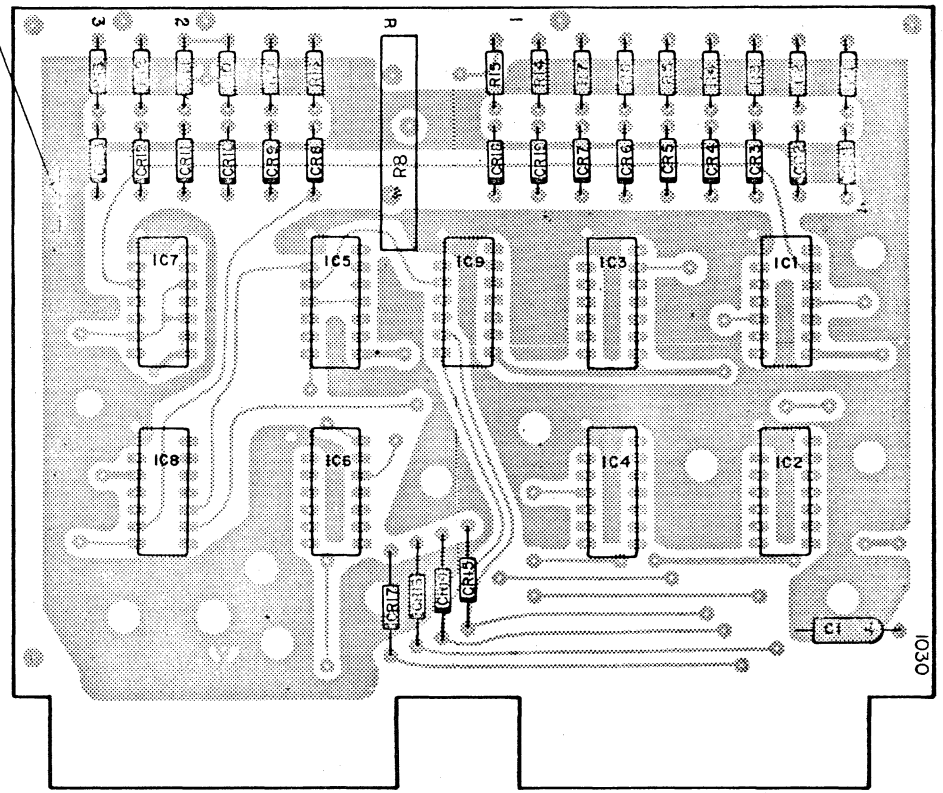
001476

USED ON	RELEASED FOR ASSY
630 A	200490
630B	200495
620	202032

DATE	CHANGE NO.	DATE	CHANGE NO.
Mar 19,68	14	Nov 25,69	493
Mar 21,68	34	Jun 1,70	1030
Jul 25,68	172	SEPT.70	1244
Sept. 13,68	201		
Nov 11,68	237		

REF DESIG	DESCRIPTION	M. E. G. PART NO.
———	PRINTED CIRCUIT BOARD	001479
C1	CAPACITOR, T, 4.7UF, 10V, ±10%	151124
CR1-19	DIODE, IN4148	150834
IC1,3,4,	INTEGRATED CIRCUIT, SP680A	150656
5,7,9		
IC2,8	INTEGRATED CIRCUIT, SP670A	150655
IC6	INTEGRATED CIRCUIT, SP659A	150654
P8	POTENTIOMETER, 100K, 3/4W, ±20%	153413
R13	RESISTOR, MF, 11K, 1/8W, ±1%	153063
R1	6.19K, 1/8W, ±1%	153231
R2	22.1K, 1/8W, ±1%	153092
R3,11	56.2K, 1/8W, ±1%	153275
R4,5,10	130K, 1/8W, ±1%	153310
R6	150K, 1/8W, ±1%	153316
R7	392K, 1/8W, ±1%	153351
R9	69.8K, 1/8W, ±1%	153284
R12	18.2K, 1/8W, ±1%	153084
R14	1.5K, 1/8W, ±1%	153028
R16	51.1K, 1/8W, ±1%	153271
R15	RESISTOR, MF, 2.21K, 1/8W, ±1%	153044
———	TAG, ENGINEERING CHANGE	200304

1 200304



001476

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

REFERENCE DOCUMENTS		E.C. LEVEL
SCH. DIAG.	001477	493
ARTMASTER	001478	1030
FABRICATION	001479	1030
TEST SPEC.	001480	1244

MATERIAL SEE B/M NO. 001476

CASE DEPTH

HARDNESS

SURFACE TREATMENT

001476 C

TOLERANCE UNLESS OTHERWISE NOTED

CORNERS AND OR EDGES BROKEN

RADII UNLESS OTHERWISE NOTED

2 PLACE DEC ±

3 PLACE DEC ±

ANGLES ±

OUTSIDE MAX

INSIDE MAX

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME PC. BOARD ASSEMBLY

FWD / REV SPEED DECODE

DESIGN TYPE

DETAIL SCALE 2/1

CHECK J.C.B. Jul 26,68 DRAW

APPRO CHECK

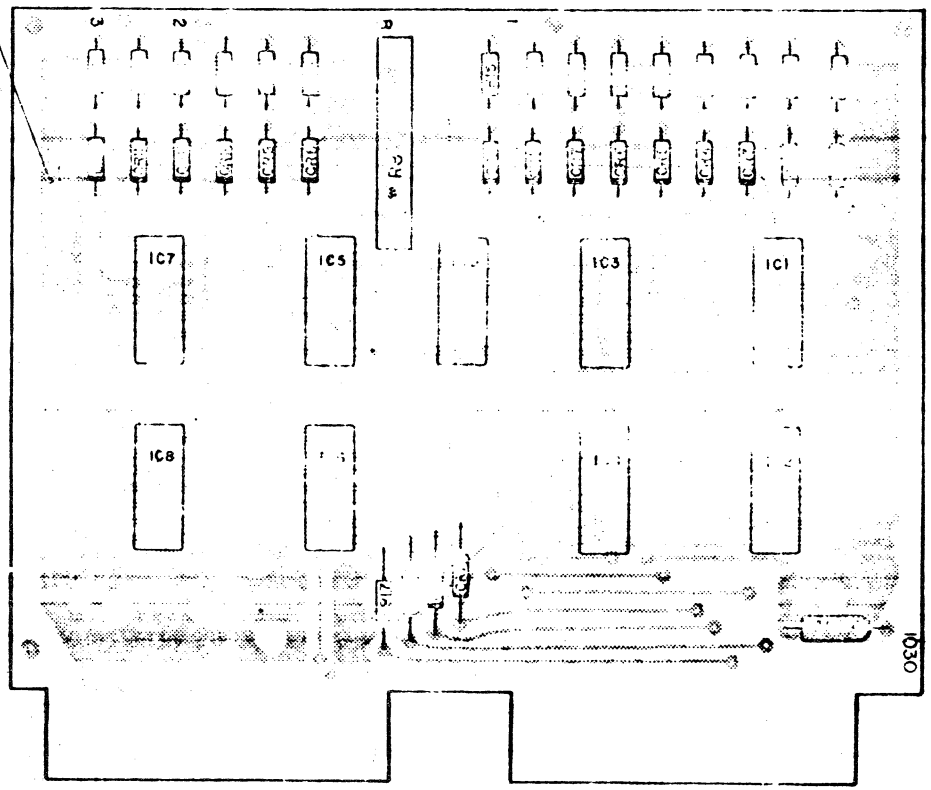
001476

001476

USED ON	PART NO.	CHANGE NO	DATE CHANGED
630 A	200430	14	Nov25,69 493
630B	200435	34	Jan1,70 1030
820	200832	172	
		201	
		237	

REF DESIG	DESCRIPTION	M. E. G PART NO.
—	PRINTED CIRCUIT BOARD	001479
C1	CAPACITOR, T. A. 7UF, 10V. ±10%	151124
CR1-19	DIODE, 1N4148	150834
IC1,3,4, 6,7,9	INTEGRATED CIRCUIT, SP680A	150656
IC2, 8	INTEGRATED CIRCUIT, SP670 A	150655
IC5	INTEGRATED CIRCUIT, SP659A	150654
R3	POTENTIOMETER, 20K, ¾W, ±20%	153314
R13	RESISTOR, F. M.R., ¼W, ±1%	153063
R	2K, ¼W, ±1%	153231
R2	33.2K, ¼W, ±1%	153092
R3, 11	56.2K, ¼W, ±1%	153275
R4, 5, 10	130K, ¼W, ±1%	153310
R6	150K, ¼W, ±1%	153316
R7	392K, ¼W, ±1%	153357
R9	59.8K, ¼W, ±1%	153264
R12	18.2K, ¼W, ±1%	153264
R14	1.5K, ¼W, ±1%	153228
R16	51.1K, ¼W, ±1%	153311
R15	RESISTIVE, 2.21K, ¼W, ±1%	153241
—	ENGINEERING CHANGE	200304

1 200304



NOTES: UNLESS OTHERWISE SPECIFIED
1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001477	493
ART MASTER	001479	1030
FABRICATION	001479	1030
TEST SPEC.		

SEE B/M 001476

TOLERANCE UNLESS OTHERWISE NOTED	
MATERIAL	
FINISH	

Peripheral Systems Corporation
A SUBSIDIARY OF MEMOREX CORPORATION

PC BOARD ASSEMBLY
FLD / REV SPEED DECODE

SIZE C | DWG NO 001476 | REV

SCALE 2/1

SHEET

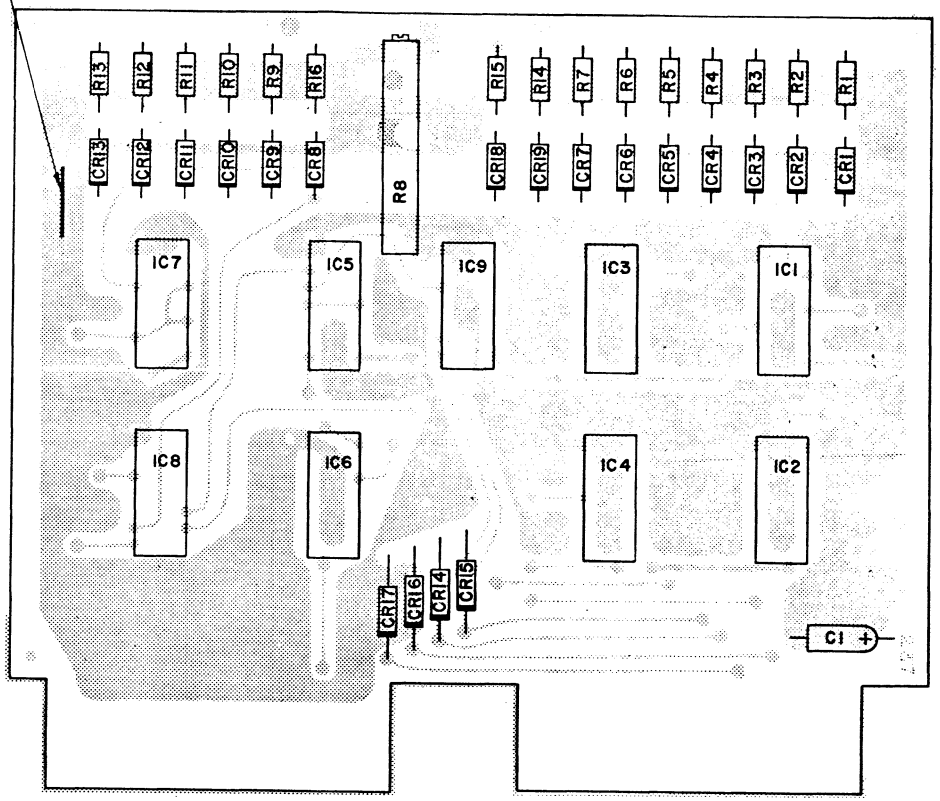
001476

001476

REF DESIG	DESCRIPTION	P.S.C. PART NO.
———	PRINTED CIRCUIT BOARD	001479
C1	CAPACITOR, 4.7UF, 10V ±10%	151124
CR1-19	DIODE, IN4148	150834
IC1,3,4,5,7,9	INTEG. CIRCUIT, SP680A	150656
IC2,8	INTEG. CIRCUIT, SP670A	150655
IC6	INTEG. CIRCUIT, SP659A	150654
R8	POT., 100K, 3/4W ±20%	153314
R13	RESISTOR, 11K, 1/8W ± 1%	153063
R1	6.19K	153231
R2	22.1K	153092
R3,11	36.2K	153275
R4,5,10	130K	153310
R6	150K	153316
R7	392K	153357
R9	62.3K	153284
R12	18.2K	153084
R14	1.5K	153028
R16	51.1K,	153271
R15	RESISTOR, 2.21K, 1/8W ± 1%	153044
———	TAG, ENGINEERING CHANGE	200304

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
630A	200490-60Hz	3-19-68	14	11 NOV 68	493
630B	200495-50Hz	3-21-68	34		
620	202032	7-25-68	172		
		8-13-68	201		
		11NOV68	237		

200304



001476

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001477	493
ARTMASTER	001478	237
FABRICATION	001479	493

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

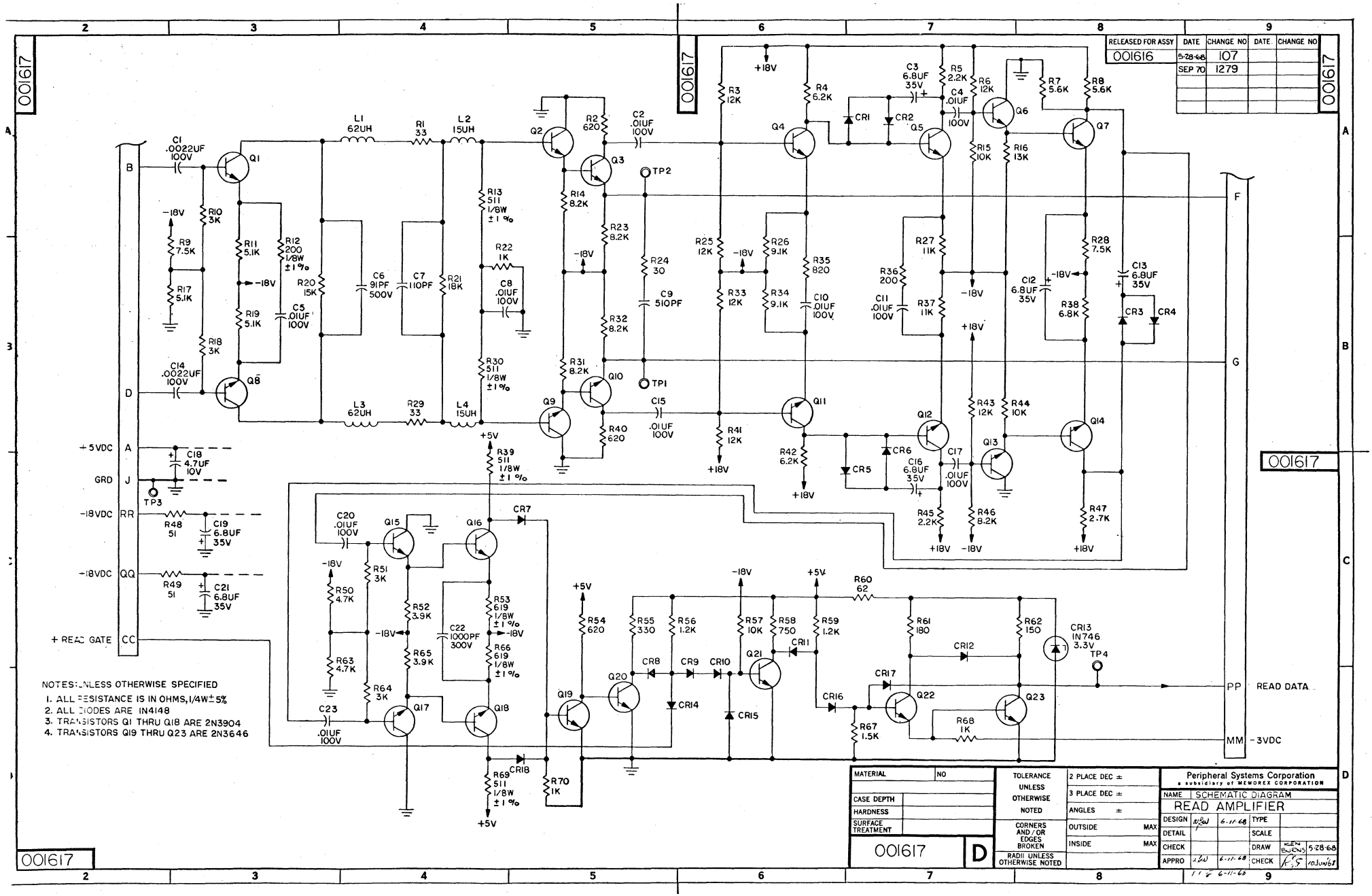
MATERIAL SEE B/M	NO. 001476
CASE DEPTH	
HARDNESS	
SURFACE TREATMENT	
001476	C

TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
	3 PLACE DEC
	ANGLES
CORNERS AND OR EDGES BROKEN	OUTSIDE MAX
	INSIDE MAX
RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	P.C. BOARD ASSEMBLY				
FWD/REV SPEED DECODER					
DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK	WCB	7-26-68	DRAW	K.B.	7-25-68
APPRO			CHECK	R.W.F	27 Nov 68

001476


001617
001617
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001617
001617
RELEASED FOR ASSY
001616
DATE
5-28-68
CHANGE NO
107
DATE
SEP 70
CHANGE NO
1279
C1 .0022UF 100V
L1 62UH
R1 33
L2 15UH
Q1
Q2
R2 620
C2 .01UF 100V
Q3
TP2
R3 12K
+18V
R4 6.2K
C3 6.8UF 35V
R5 2.2K
R6 12K
R7 5.6K
R8 5.6K
CR1
CR2
Q4
Q5
Q6
Q7
R10 3K
R9 7.5K
R11 5.1K
R12 200 1/8W ±1%
R13 511 1/8W ±1%
R14 8.2K
R15 10K
R16 13K
-18V
R17 5.1K
R18 3K
R19 5.1K
R20 15K
C6 91PF 500V
C7 110PF
R21 18K
R22 1K
C8 .01UF 100V
C5 .01UF 100V
R23 8.2K
R24 30
C9 510PF
R25 12K
R26 9.1K
R27 11K
R28 7.5K
R32 8.2K
R33 12K
R34 9.1K
R35 820
C10 .01UF 100V
R36 200
C11 .01UF 100V
R37 11K
C12 6.8UF 35V
R38 6.8K
C13 6.8UF 35V
CR3
CR4
C14 .0022UF 100V
Q8
R30 511 1/8W ±1%
R31 8.2K
Q10
TP1
Q9
C15 .01UF 100V
R40 620
L3 62UH
R29 33
L4 15UH
R41 12K
Q11
R42 6.2K
Q12
Q13
Q14
R43 12K
R44 10K
CR5
CR6
C16 6.8UF 35V
C17 .01UF 100V
R45 2.2K
R46 8.2K
R47 2.7K
+5V
R39 511 1/8W ±1%
+5VDC
C18 4.7UF 10V
GRD
TP3
-18VDC
R48 51
C19 6.8UF 35V
-18VDC
R49 51
C21 6.8UF 35V
+ READ GATE
C20 .01UF 100V
Q15
Q16
CR7
R51 3K
R50 4.7K
R52 3.9K
R53 619 1/8W ±1%
C22 1000PF 300V
R63 4.7K
R65 3.9K
R66 619 1/8W ±1%
R64 3K
Q17
Q18
C23 .01UF 100V
R69 511 1/8W ±1%
CR18
R70 1K
R54 620
Q19
Q20
R55 330
R56 1.2K
CR8
CR9
CR10
CR14
CR15
R57 10K
R58 750
R59 1.2K
Q21
CR11
CR16
R67 1.5K
R60 62
R61 180
CR12
CR17
Q22
Q23
R62 150
CR13 IN746 3.3V
TP4
R68 1K
F
G
PP
READ DATA
MM
-3VDC
001617
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE IS IN OHMS, 1/4W ±5%
2. ALL DIODES ARE IN4148
3. TRANSISTORS Q1 THRU Q18 ARE 2N3904
4. TRANSISTORS Q19 THRU Q23 ARE 2N3646
MATERIAL
NO
CASE DEPTH
HARDNESS
SURFACE TREATMENT
001617
D
TOLERANCE UNLESS OTHERWISE NOTED
2 PLACE DEC ±
3 PLACE DEC ±
ANGLES ±
CORNERS AND/OR EDGES BROKEN
OUTSIDE MAX
INSIDE MAX
RADII UNLESS OTHERWISE NOTED
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION
NAME SCHEMATIC DIAGRAM
READ AMPLIFIER
DESIGN
DETAIL
CHECK
APPRO
TYPE
SCALE
DRAW
CHECK
5-28-68
10JUN68
6-11-68

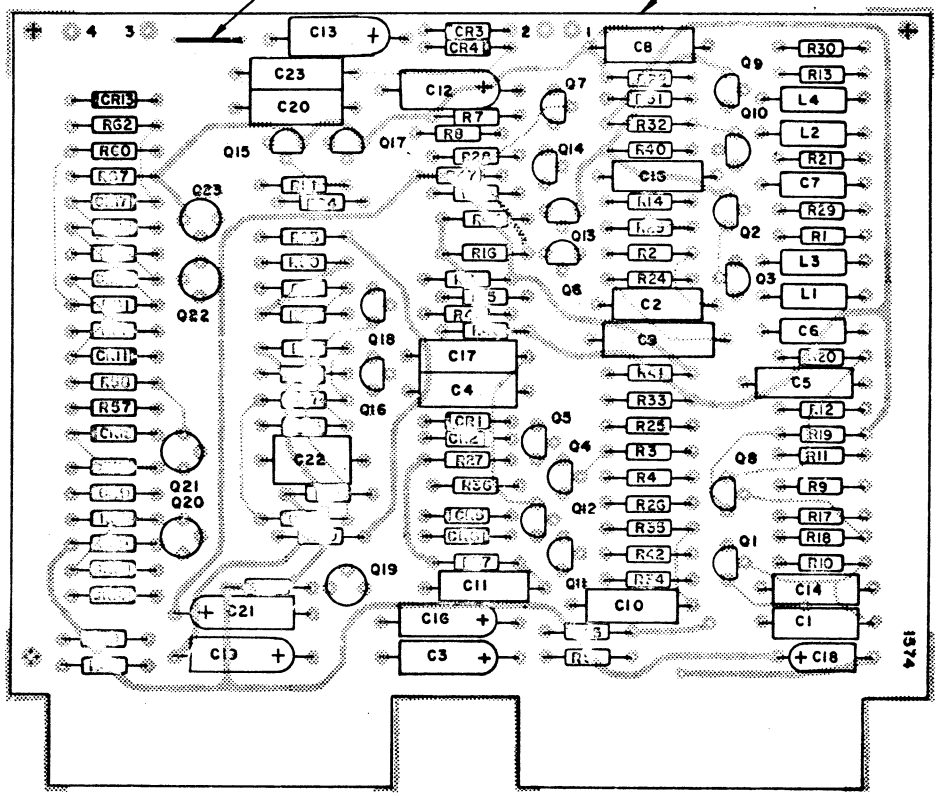
REF DESIG	DESCRIPTION	M E G PART NO.
C1,14	CAPACITOR, .0022uF, COV, ± 5%	15.054
C2,4,5,8,10, 11,15,17,20,23	.01 UF, 100V, ±10%	51063
C3,12,13, 16,19,21	6.8uF, 35V, ±10%	151129
C6	91 PF, 500V ±5%	151221
C7	110PF, 500V, ±5%	151223
C9	510PF, 500V, ±5%	151239
C22	1000PF, 300V, ±5%	151246
C18	CAPACITOR, 4.7uF, 10V, ±10%	151124
CR1-12,14-18	DIODE, IN4148	150834
CR13	DIODE, IN746, 3.3V ±10%	150827
R1,229	RESISTOR 33Ω, 1/4W, ±5%	151447
R2,40,54	620Ω	151478
R3,6,25, 33,41,43	12K	151509
R4,42	6.2K	151502
R5,45	2.2K	151491
R7,8	5.6K	151501
R9,28	7.5K	151504
R10,18,51,64	3K	151494
R11,17,19	5.1K	151500
R36	200Ω	151466
R14,23,31	8.2K	151505
R32,46		
R15,44,57	10K	151507
R16	13K	151510
R22,68,70	1K	151483
R21	18K	151513
R24	30Ω	151446
R27,37	11K	151508
R26,34	9.1K	151506
R35	820Ω	151481
R38	6.8K	151503
R47	2.7K	151493
R48,49	51Ω	151452
R56,59	1.2K	151485
R55	330Ω	151471
R58	750Ω	151480
R60	62Ω	151454
R61	180Ω	151465
R62	150Ω	151463
R67	1.5K	151487
R70	15K	151511
R50,63	4.7K	151499
R52,65	RESISTOR, 3.9K, 1/4W, ±5%	151497
R13,53,66	RESISTOR, 511Ω, 1/8W, ±1%	153175
R53,66	RESISTOR, 619Ω, 1/8W, ±1%	153183
R12	RESISTOR, 200Ω, 1/8W, ±1%	152992
L1,3	INDUCTOR, 62uH, ±5%	151381
L2,4	INDUCTOR, 15uH, ±10%	151366
Q1-18	TRANSISTOR, 2N3904	150735
Q19-23	TRANSISTOR, 2N3646	150734
——	TAG ENGINEERING CHANGE	200304

001616

DATE	CHANGE NO	DATE	CHANGE NO	001616
6-8-68	107	SEPT.70	1279	
16 JULY 68	153	NOV. 70	1574	RELEASED FOR ASSEMBLY
11-19-68	219	NOV'70	1579	200490-60~
1-2-70	580			200495-50~

200304 [1]

001619 [3]



001616

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001617	1279
ARTMASTER	001618	1574

NOTES:

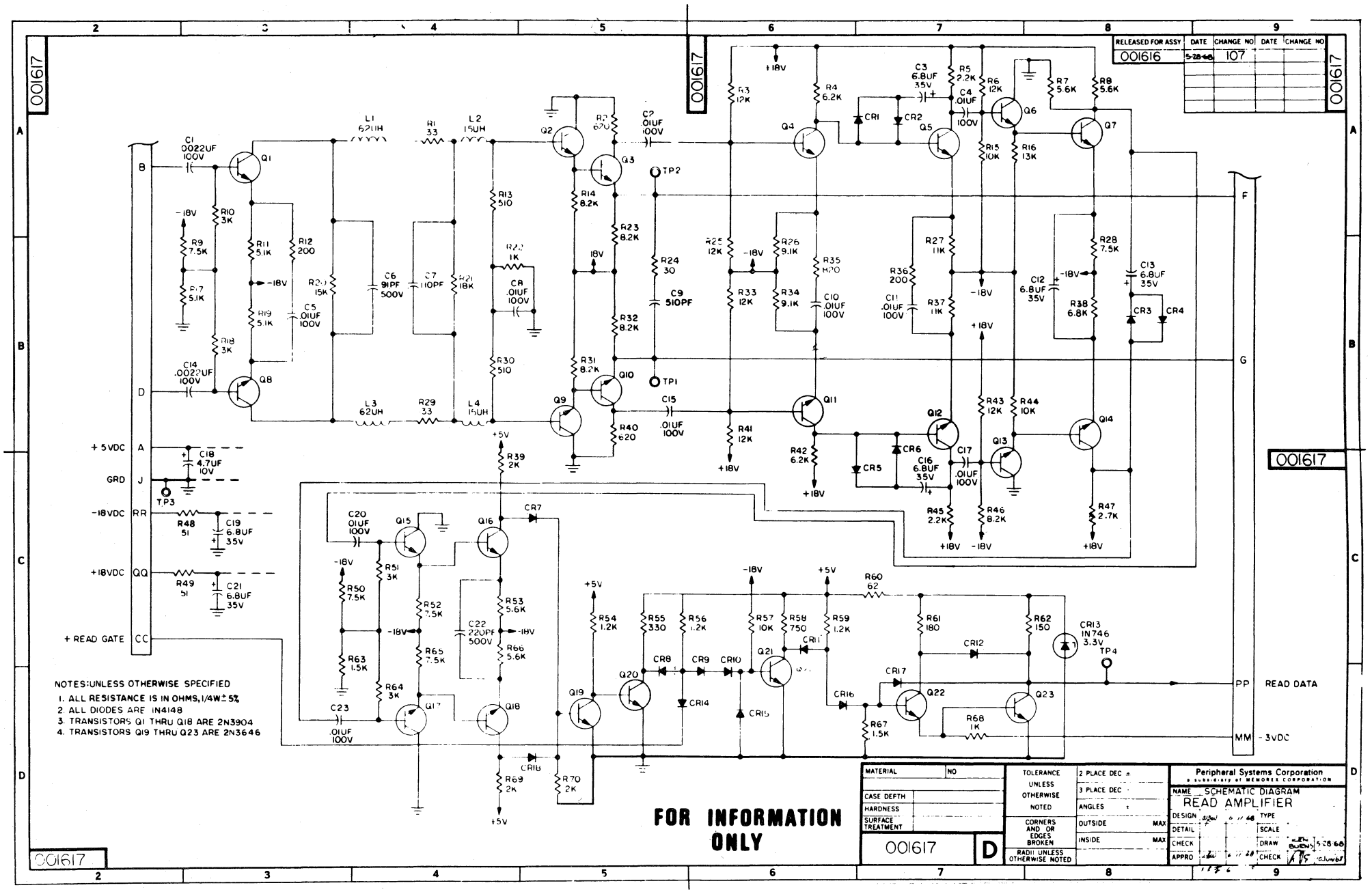
[1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER

2. COMPONENT HEIGHT NOT TO EXCEED .350.

[3] P.C. BOARD 001619 MUST BE AT EC LEVEL 1574 .

4. MUST CONFORM TO ENG. SPECIFICATION 801185 AT EC LEVEL 1279 .

MATERIAL NO SEE B/M 001616	MUST CONFORM TO ENG SPEC 88000C	TOLERANCE UNLESS OTHERWISE NOTED	MEMOREX EQUIPMENT GROUP
CASE DEPTH		LINEAR	NAME PC BOARD ASSEMBLY READ AMPLIFIER
HARDNESS	TECHNICAL APPROVAL	ANG. LAP	
SURFACE TREATMENT		CORNERS AND OR EDGES BROKEN	DESIGN SCALE 2/1
STD CODE C		OUTSIDE WAS / WILL	DETAIL OCT 70 CHECK OCT 70 APPRO 001616


001617
RELEASED FOR ASSY
DATE
CHANGE NO
001616
5-28-68
107
+18V
-18V
+5V
+5VDC
GRD
-18VDC
+18VDC
+READ GATE
TP1
TP2
TP3
TP4
READ DATA
-3VDC
NOTES:UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE IS IN OHMS, 1/4W ± 5%
2. ALL DIODES ARE IN4148
3. TRANSISTORS Q1 THRU Q18 ARE 2N3904
4. TRANSISTORS Q19 THRU Q23 ARE 2N3646
FOR INFORMATION ONLY
MATERIAL
NO
CASE DEPTH
HARDNESS
SURFACE TREATMENT
TOLERANCE UNLESS OTHERWISE NOTED
2 PLACE DEC ±
3 PLACE DEC ±
ANGLES °
CORNERS AND OR EDGES BROKEN
RADII UNLESS OTHERWISE NOTED
OUTSIDE MAX
INSIDE MAX
Peripheral Systems Corporation
A SUBSIDIARY OF MEMOREX CORPORATION
NAME SCHEMATIC DIAGRAM
READ AMPLIFIER
DESIGN
DETAIL
CHECK
APPRO
TYPE
SCALE
DRAW
CHECK
5-28-68
001617
D

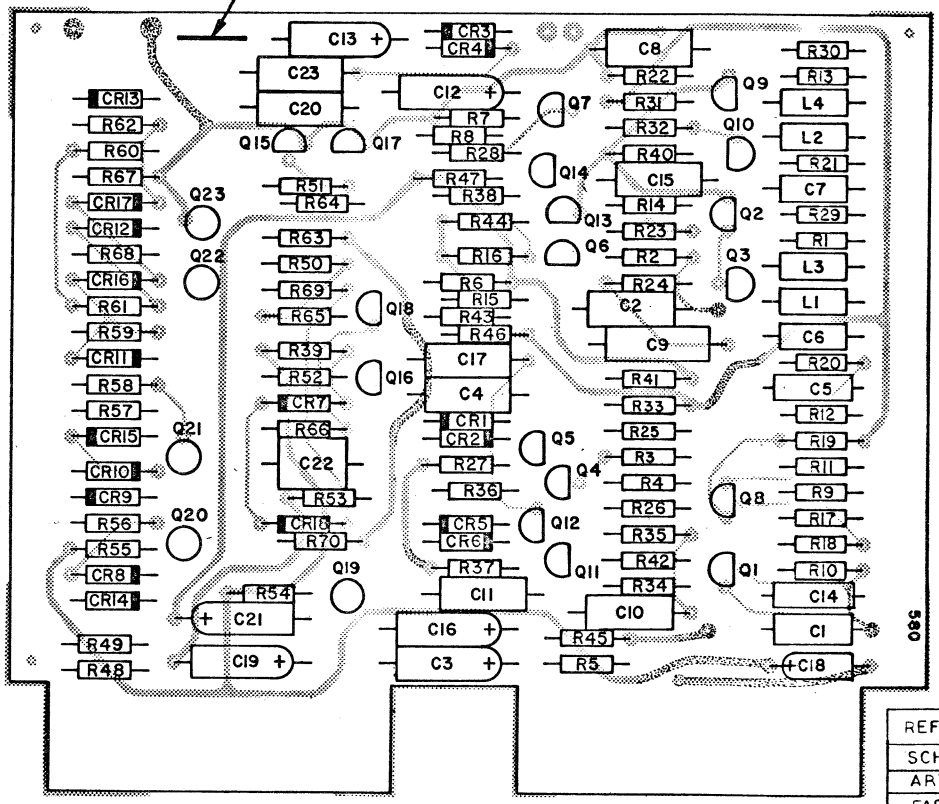
001616

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490-60~	6-8-68	107		
200495-50~	11-14-68	153		
	11-19-68	219		
	1-2-70	580		
	SEP 70	1279		

001616

REF DESIG	DESCRIPTION	P.S.C. PART NO.
——	PRINTED CIRCUIT BOARD	001619
C1,14	CAPACITOR, .0022UF, 100V ±10%	151054
	CAPACITOR, .01 UF, 100V ±10%	151063
	C2,4,5,8,10,11,15,17,20,23	
C3,9,12,13,16,19,21	CAPACITOR, 6.8UF, 35V ±10%	151129
C6	91 PF, 500V ±5%	151221
C7	110 PF, 500V ±5%	151223
C9	510 PF, 500V ±5%	151239
C22	1000 PF, 300V ±5%	151246
C18	CAPACITOR, 4.7UF, 10V ±10%	151124
CR1-12, 14-18	DIODE, IN4148	150834
CR13	DIODE, IN746 (ZENER)	150827
R1,29	RESISTOR, 33Ω, 1/4W ±5%	151447
R2,40,54	620Ω	151478
R3,6,25,33,41,43	12K	151509
R4 42	6.2K	151502
R5,45	2.2K	51491
R7,8	5.6K	151501
R9,28	7.5K	151504
R10,18,51,64	3K	151494
R11,17,19	5.1K	151500
R36	200Ω, 1/4W, ±5%	151466
R38,50,39,69	511Ω, 1/8W, ±1%	153175
R4,23,31,53,66	8.2K, 1/4W, ±5%	151505
R15,44,57	10K	151507
R16	13K	151510
R22,68,70	1K	151483
R21	18K	151513
R24	30Ω	151446
R27,37	11K	151508
R26,34	9.1K	151506
R35	820Ω	151481
R38	6.8K	151503
R47	2.7K	151433
R48,49	51Ω	151452
R56,59	1.2K	151485
R55	330Ω	151477
R58	750Ω	151480
R60	62Ω	151454
R61	180Ω	151465
R62	150Ω	151463
R67	1.5K	151487
R20	RESISTOR, 15K, 1/4W, ±5%	151511
R50,63	RESISTOR, 4.7K, 1/4W, ±5%	151499
R52,65	RESISTOR, 3.9K, 1/4W, ±5%	151497
R53,66	RESISTOR, 619Ω, 1/8W, ±1%	153163
R12	RESISTOR, 200Ω, 1/8W, ±1%	152992
L1,L3	INDUCTOR, 62 uH, ±5%	51381
L2,4	INDUCTOR, 15 uH, ±10%	151366
Q1-18	TRANSISTOR 2N3904	150735
Q19-23	TRANSISTOR, 2N3646	150734
——	TAG, ENGINEERING CHG	200304

200304 [1]



001616

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001617	1279
ARTMASTER	001618	580
FABRICATION	001618	580
ENGRG SPEC	881185	1279

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M	NO. 001616	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC
CASE DEPTH			ANGLES
HARDNESS			OUTSIDE MAX
SURFACE TREATMENT		CORNERS AND OR EDGES BROKEN	INSIDE MAX
001616	C	RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

P.C. BOARD ASSEMBLY
READ AMPLIFIER

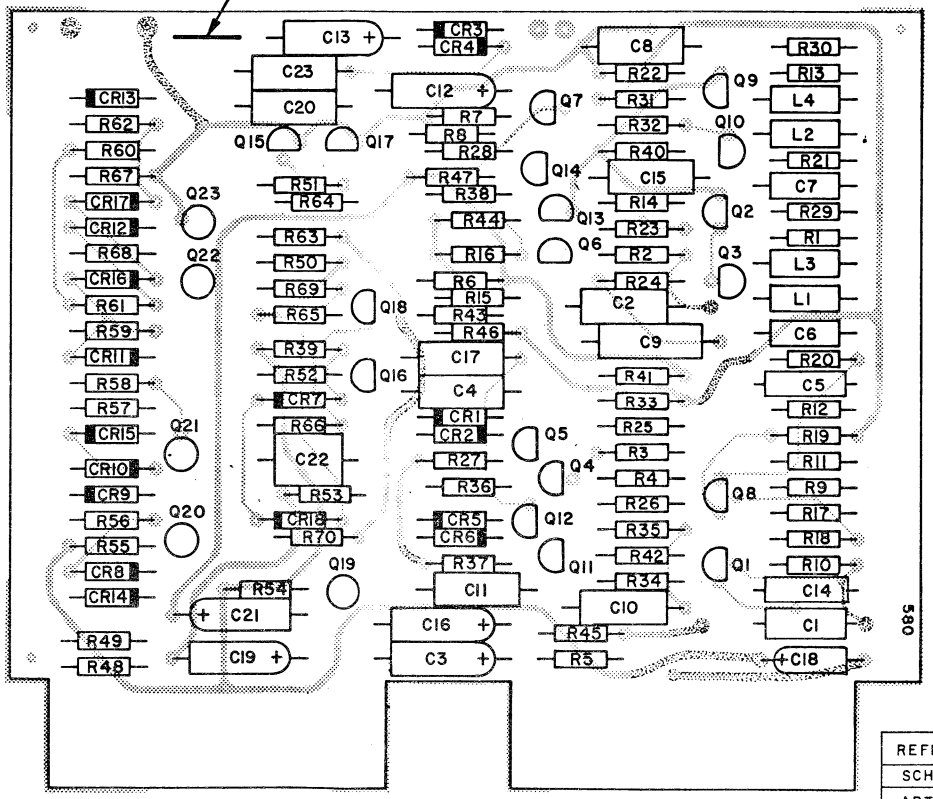
DESIGN	[illegible]	6-11-68	TYPE		
DETAIL			SCALE	2/1	
CHECK			DRAW	K.B.	5-29-68
APPRO	[illegible]	6-11-68 7-11-68	CHECK	[illegible]	10 Jan '68

001616

REF DESIG	DESCRIPTION	P.S.C. PART NO.
———	PRINTED CIRCUIT BOARD	001619
C1,14	CAPACITOR, .0022UF, 100V ±10%	151054
	CAPACITOR, .01 UF, 100V ±10%	151063
	C2,4,5,8,10,11,15,17,20,23	
C3,12,13,16, 19,21	CAPACITOR, 6.8UF, 35V ±10%	151129
C6	91 PF, 500V ±5%	151221
C7	110PF, 500V ±5%	151223
C9	510PF, 500V ±5%	151239
C22	220PF, 500V ±5%	151230
C18	CAPACITOR, 4.7UF, 10V ±10%	151124
CR1-12, 14-18	DIODE, IN4148	150834
CR13	DIODE, IN746 (ZENER)	150827
R1,29	RESISTOR, 33Ω, 1/4W ±5%	151447
R2,40	620Ω	151478
R3,6,25, 33,41,43	12K	151509
R4,42	6.2K	151502
R5,45	2.2K	151491
R7,8,53,66	5.6K	151501
R9,28,50, 52,69	7.5K	151504
R10,18,51,64	3K	151494
R11,17,19	5.1K	151500
R12,36	200Ω	151466
R13,30	510Ω	151476
R14,23,31, 32,46	8.2K	151505
R15,44,57	10K	151507
R16	13K	151510
R22,68	1K	151483
R21	18K	151513
R24	30Ω	151446
R27,37	11K	151508
R26,34	9.1K	151506
R35	820Ω	151481
R38	6.8K	151503
R39,63,70	2K	151450
R47	2.7K	151453
R48,49	51Ω	151452
R54,56,59	1.2K	151485
R55	330Ω	151471
R58	750Ω	151480
R60	62Ω	151454
R61	180Ω	151465
R62	150Ω	151463
R63,67	1.5K	151487
R20	RESISTOR, 15K, 1/4W, ±5%	151511
Q1-18	TRANSISTOR, 2N3904	150735
Q19-23	TRANSISTOR, 2N3646	150734
L1,3	INDUCTOR, 62UH ±5%	151381
L2,4	INDUCTOR, 15UH ±10%	151366
———	TAG, ENGINEERING CHG	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490-60~	6-8-68	107		
200495-50~	11-4-68	153		
	11-19-68	219		
	1-2-70	580		

200304 [1]



001616

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001617	107
ARTMASTER	001618	580
FABRICATION	001619	580

NOTES: UNLESS OTHERWISE SPECIFIED

[1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER

2. COMPONENT HEIGHT NOT TO EXCEED .350

SEE B/M 001616

001616 C

Peripheral Systems Corporation

P.C. BOARD ASSEMBLY

READ AMPLIFIER

LSW 6-11-68 TYPE

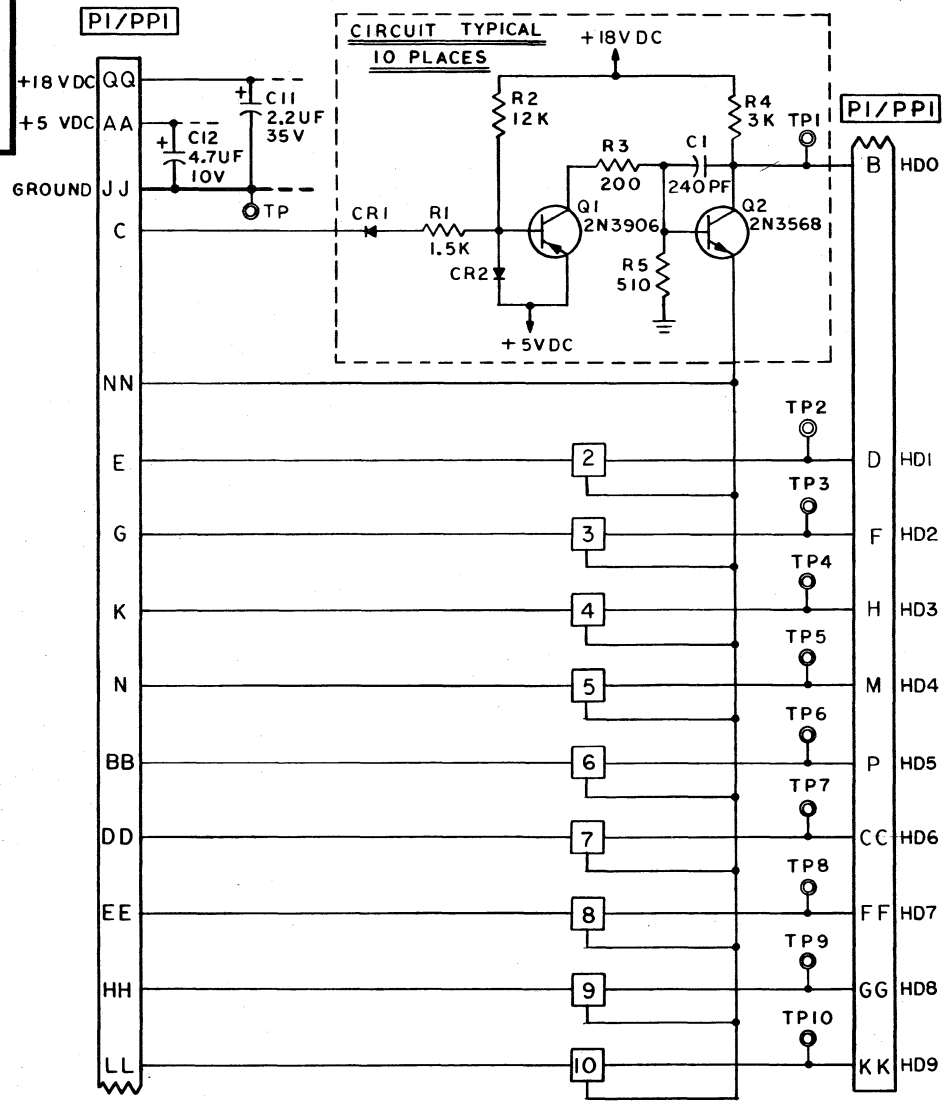
SCALE 2/1

K.B. 5-20-68

LSW 6-11-68 10 Jun 68

001616

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001131	3/21/68	14		
	3-21-68	34		



001132

CIRCUIT	REFERENCE DESIGNATIONS									
1	C1	CR1	CR2	Q1	Q2	R1	R2	R3	R4	R5
2	C2	CR3	CR4	Q3	Q4	R6	R7	R8	R9	R10
3	C3	CR5	CR6	Q5	Q6	R11	R12	R13	R14	R15
4	C4	CR7	CR8	Q7	Q8	R16	R17	R18	R19	R20
5	C5	CR9	CR10	Q9	Q10	R21	R22	R23	R24	R25
6	C6	CR11	CR12	Q11	Q12	R26	R27	R28	R29	R30
7	C7	CR13	CR14	Q13	Q14	R31	R32	R33	R34	R35
8	C8	CR15	CR16	Q15	Q16	R36	R37	R38	R39	R40
9	C9	CR17	CR18	Q17	Q18	R41	R42	R43	R44	R45
10	C10	CR19	CR20	Q19	Q20	R46	R47	R48	R49	R50

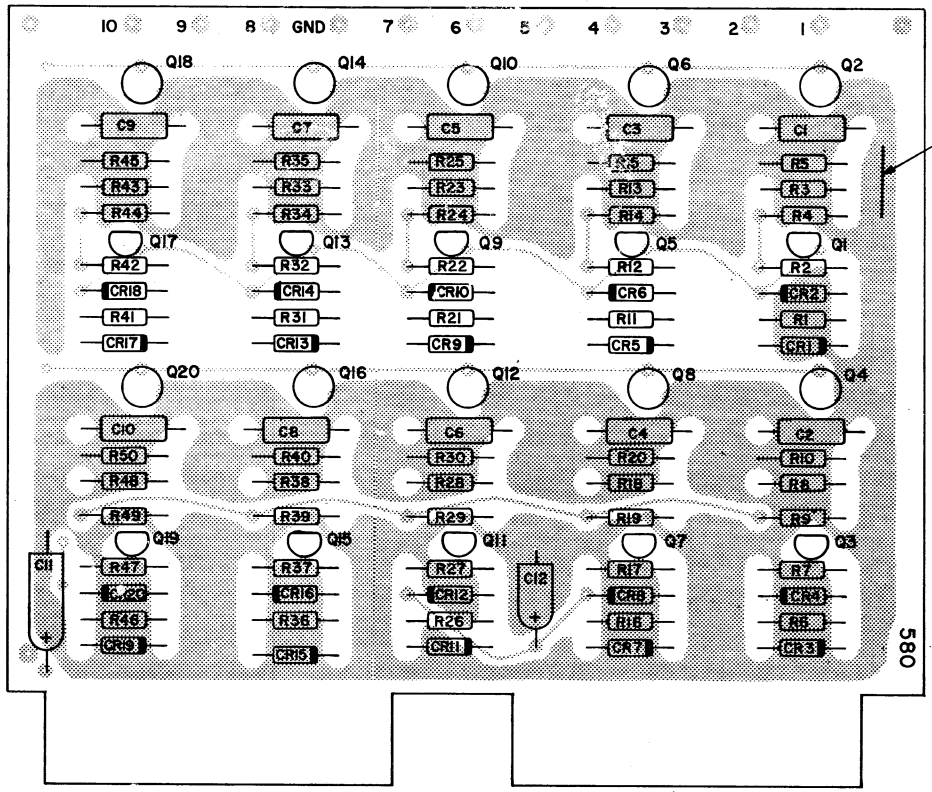
NOTES: UNLESS OTHERWISE SPECIFIED –

1. ALL RESISTORS IN OHMS, 1/4W, ±5%
2. ALL DIODES ARE IN4148

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION
CASE DEPTH			3 PLACE DEC ±	NAME SCHEMATIC DIAGRAM
HARDNESS			ANGLES ±	HEAD SWITCH DRIVERS
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN TYPE
001132	C	RADII UNLESS OTHERWISE NOTED	INSIDE MAX	DETAIL SCALE NONE
				CHECK 3/21/68 DRAW R.D.E. 20 MAR 68
				APPRO CHECK R.D.E. 21 MAR 68

REF. DESIG	DESCRIPTION	M. E. G. PART NO.
———	PRINTED CIRCUIT BOARD	001134
R1, 6, 11, 16, 21, 26, 31, 36, 41, 46	RESISTOR, COMP, 1.5K, 1/4W, ±5%	151487
R2, 7, 12, 17, 22, 27, 32, 37, 42, 47	RESISTOR, COMP, 12K, 1/4W, ±5%	151509
R3, 8, 13, 18, 23, 28, 33, 38, 43, 48	RESISTOR, COMP, 200 OHM, 1/4W, ±5%	151466
R4, 9, 14, 19, 24, 29, 34, 39, 44, 49	RESISTOR, COMP, 3K, 1/4W, ±5%	151494
R5, 10, 15, 20, 25, 30, 35, 40, 45, 50	RESISTOR, COMP, 510 OHM, 1/4W, ±5%	151476
C1-10	CAPACITOR P, 240PF, 500V, ±5%	151231
C11	" " T, 2.2UF, 35V, ±10%	151127
C12	CAPACITOR T, 4.7 UF, 10V, ±10%	151124
CR1-20	DIODES, IN4148	150834
Q1, 3, 5, 7, 9, 11, 13, 15, 17, 19	TRANSISTORS, (2N 3906)	150736
Q2, 4, 6, 8, 10, 12, 14, 16, 18, 20	TRANSISTORS, (2N 3568)	150730
	TAG, ENGINEERING CHANGE	200304

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
630A	200490	3/24/69	288A		
630B	200495	12/10/68	580		
620	202032				



[1] 200304

001131

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001132	34
ARTMASTER	001133	580
FABRICATION	001134	580

NOTES: UNLESS OTHERWISE SPECIFIED

[1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER

2. COMPONENT HEIGHT NOT TO EXCEED .350

001131

MATERIAL SEE B/M NO 001131		TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001131	C	RADII UNLESS OTHERWISE NOTED	

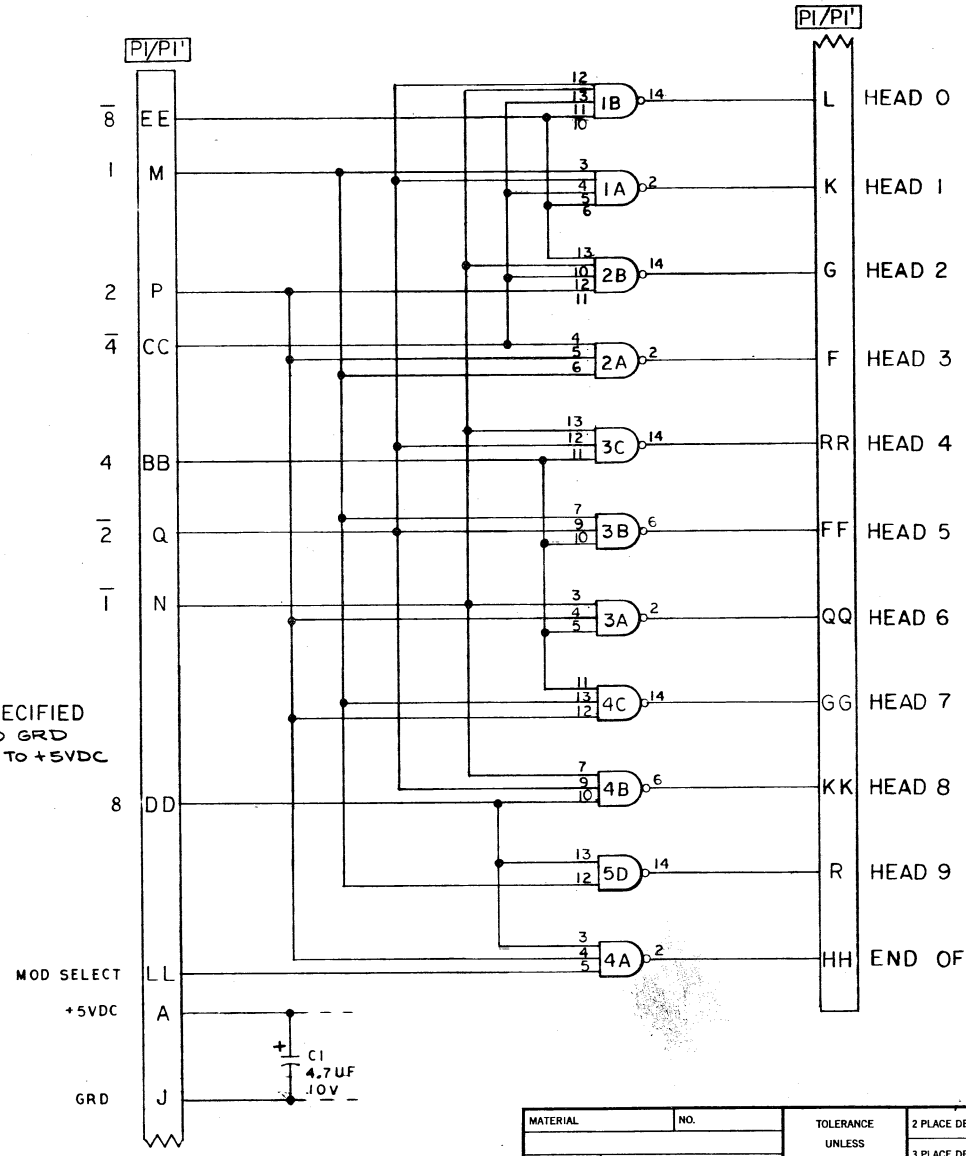
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME P.C. BOARD ASSEMBLY
HEAD SWITCH DRIVERS

DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK			DRAW	J.C.W.	3/24/69
APPRO	H.R.T.	4/1/69	CHECK	R. Thomas	4.4.69

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001191	3/14/68	14		
	3/21/68	34		

001192



001192

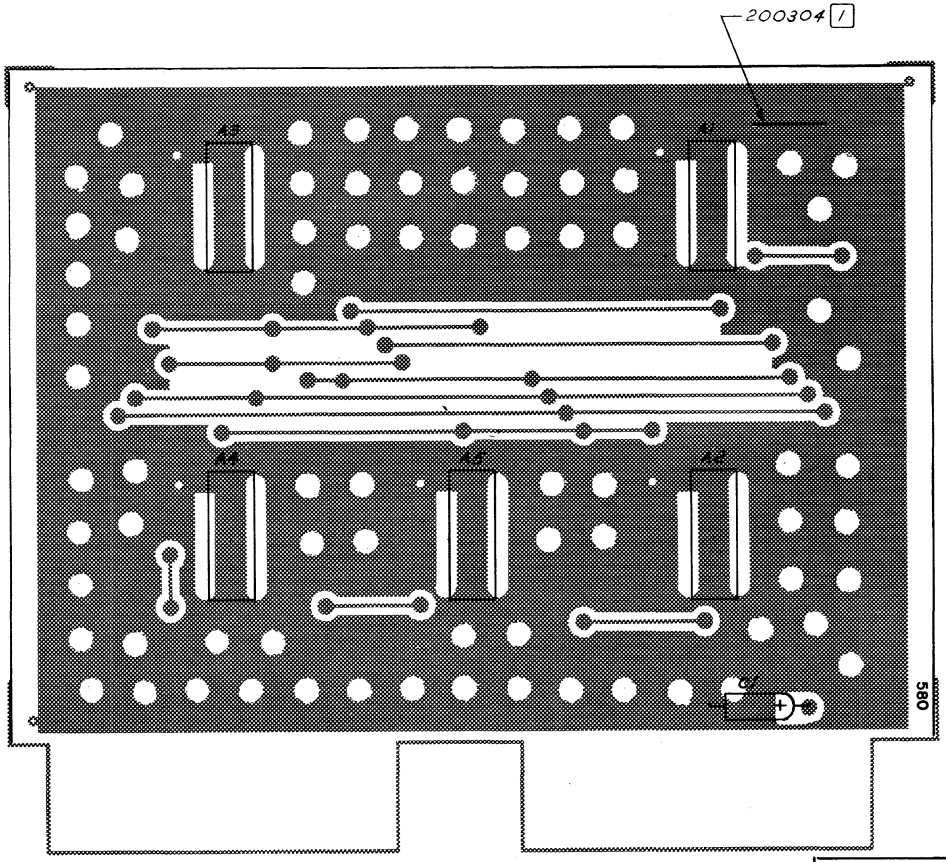
NOTES: UNLESS OTHERWISE SPECIFIED
1. CONNECT PIN 1 OF ALL IC'S TO GRD
2. CONNECT PIN 8 OF ALL IC'S TO +5VDC
3. IC'S 1 AND 2 ARE SP616A
4. IC'S 3 AND 4 ARE SP670A
5. IC5 IS SP680A

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM HEAD SWITCHING DECODER
CASE DEPTH			ANGLES ±	DESIGN	TYPE
HARDNESS			OUTSIDE MAX	DETAIL	SCALE NONE
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	INSIDE MAX	CHECK JAM 3/14/68	DRAW EGG 12/11/67
001192	C	RADII UNLESS OTHERWISE NOTED		APPRO JSK 3/15/68	CHECK [illegible] 3/14/68

001192

REF DESIG	DESCRIPTION	P.S.C. PART NO.
—	PRINTED CIRCUIT BOARD	001194
C1	CAPACITOR, 4.7 UF, 10V, ±10%	151124
IC1, IC2	INTEGRATED CIRCUIT, SP616A	150650
IC3, IC4	INTEGRATED CIRCUIT, SP670A	150655
IC5	INTEGRATED CIRCUIT, SP680A	150656
—	TAG, ENG CHANGE	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490-60~	13MAR68	14		
200495-50~	3/21/68	34		
	17JUL68	158		
	11-19-68	219		
	12-16-69	580		



001191

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001192	34
ARTMASTER	001193	580
FABRICATION	001194	580

NOTES: UNLESS OTHERWISE SPECIFIED:
1. / ENG. CHANGE TAG (200304) MUST REFLECT THE LATEST ENG. CHANGE NUMBER.
2. COMPONENT HEIGHT NOT TO EXCEED .350

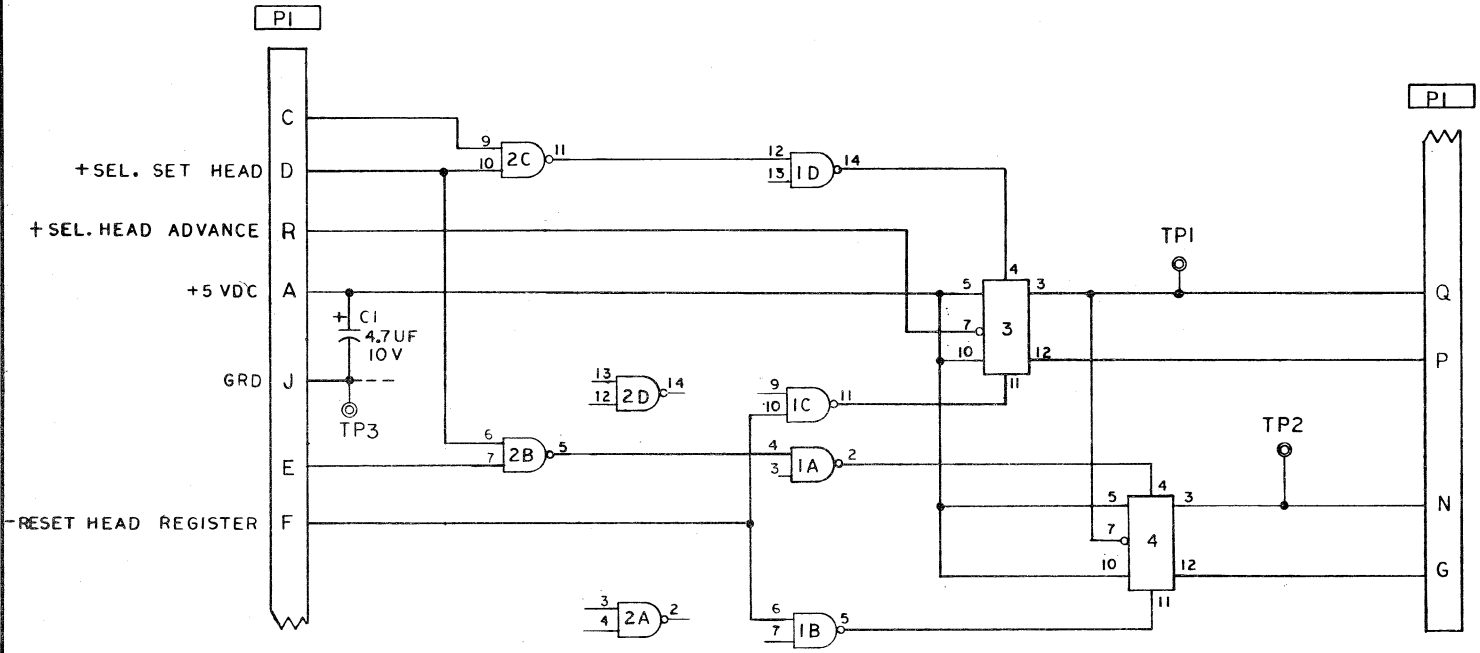
MATERIAL SEE B/M	NO. 001191	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES °
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001191	C	RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	ASSEMBLY DRAWING				
	HEAD SWITCH DECODER				
DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK	JOX	15 JUL 68	DRAW	TCM	1-22-68
APPRO	JOX dfw	15 JUL 68 3-27-68	CHECK	R.O.E.	1-24-68

001191

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001331	3/18/68	14		
	3/21/68	34		



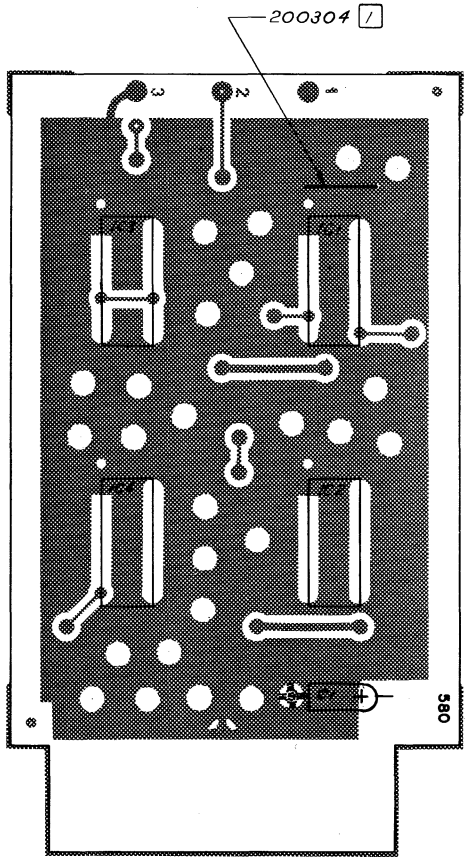
NOTES: UNLESS OTHERWISE SPECIFIED,
1. CONNECT PIN 1 OF ALL IC'S TO GRD
2. CONNECT PIN 8 OF ALL IC'S TO +5VDC
3. IC1 AND 2 ARE SP680A
4. IC3 AND 4 ARE SP620A

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION
CASE DEPTH			3 PLACE DEC ±	NAME SCHEMATIC DIAGRAM HEAD REGISTER
HARDNESS			ANGLES ±	DESIGN TYPE
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DETAIL SCALE NONE
001332	C		INSIDE MAX	CHECK 3/18/68 DRAW EGG 12/24/67
		RADII UNLESS OTHERWISE NOTED		APPRO CHECK KJE 12/26/67

001332

REF DESIG	DESCRIPTION	P.S.C. PART NO.
——	PRINTED CIRCUIT BOARD	001334
C1	CAPACITOR, 4.7UF, 10V, ±10%	151124
IC1, IC2	INTEGRATED CIRCUIT (SP680A)	150656
IC3, IC4	INTEGRATED CIRCUIT (SP620A)	150651
—	ENG. CHANGE TAG	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200244	1BMAR68	14		
	5/21/68	34		
	11-19-68	219		
	12-16-69	580		



REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001332	34
ARTMASTER	001333	580
FABRICATION	001334	580

NOTES: UNLESS OTHERWISE SPECIFIED

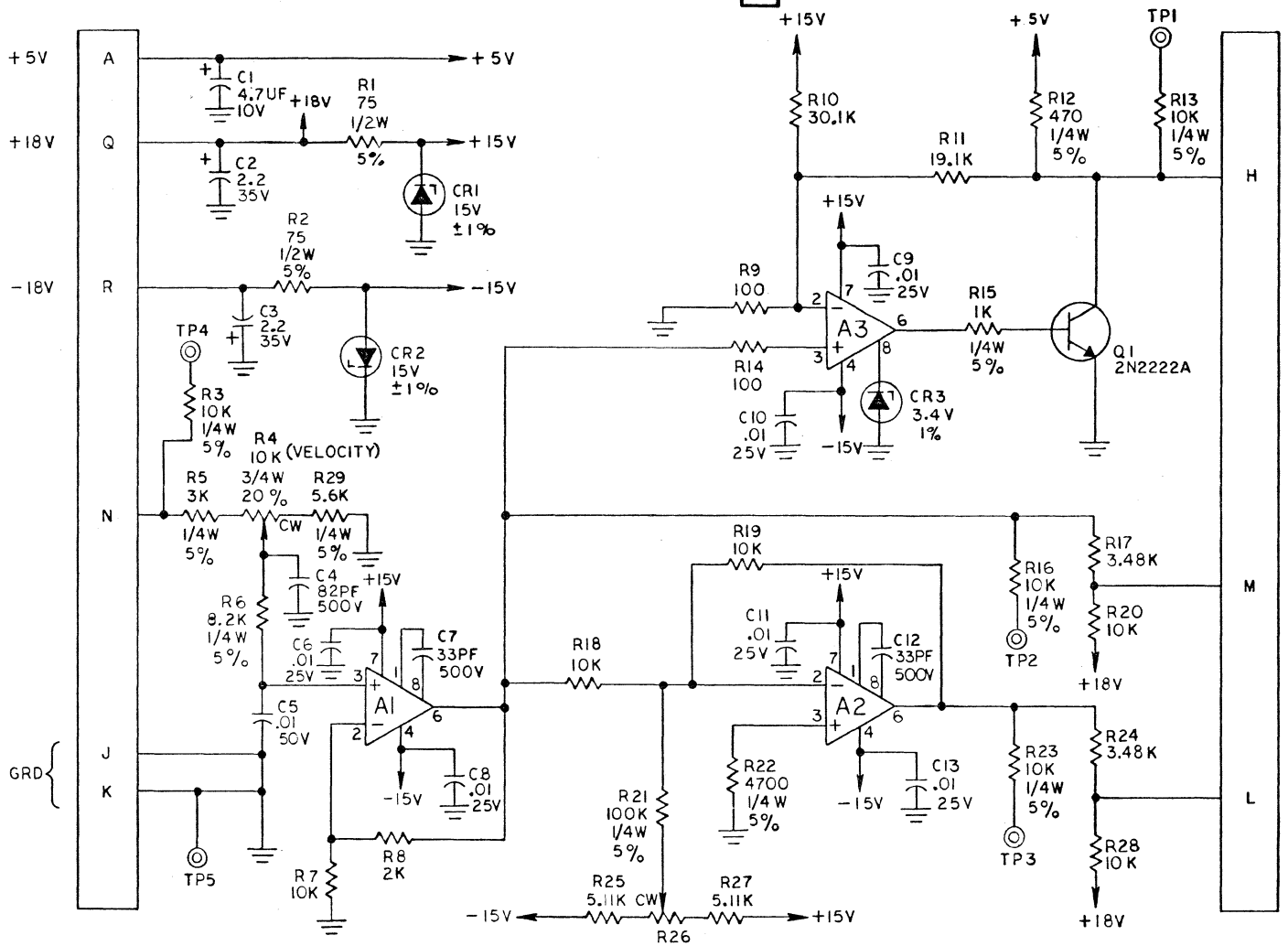
1. ENGINEERING CHANGE TAG (NO. 200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NO.
2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M	NO. 001331	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS			
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
001331	C		INSIDE MAX
		RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	ASSEMBLY DRAWING				
	HEAD REGISTER				
DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK	WGR	1-29-68	DRAW	TCM	1-27-68
APPRO	[illegible]	18 MAR 68 3-27-68	CHECK	[illegible]	1-29-68

001331



NOTES: UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE IN OHMS, 1/8W, ±1%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. IC A1,2,3 ARE LM301A.

DATE	CHANGE NO.	DATE	CHANGE NO.	TECHNICAL APPROVAL
		6-3-68	111	
		7-18-68	151	
		MAY 18,70	790	

MEMOREX EQUIPMENT GROUP

NAME SCHEMATIC DIAGRAM
TACHOMETER AMPLIFIER

DESIGN		
DETAIL	EVANS	3-12-70
CHECK		
APPRO		6/12/63

001437

001437

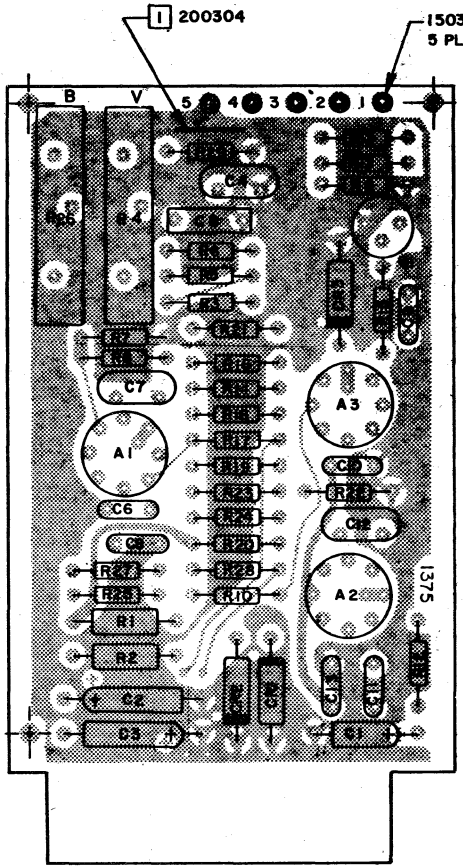
001437

C

USED ON	RELEASED FOR ASSY
630 A	200490
	MULTI-USE

DATE	CHANGE NO	DATE	CHANGE NO
3-25-68	14	9-8-69	441
3-27-68	34	11-21-69	559
6-10-68	111	1-16-69	685
7-18-68	151	MAY 18, 70	790
2-14-69	246	AUG. 70	1375

REF DESIG	DESCRIPTION	M. E. G. PART NO.
———	PRINTED CIRCUIT BOARD	001439
C1	CAPACITOR, T, 4.7UF, 10V, ±10%	151124
C2,3	T, 2.2UF, 35V, ±10%	151127
C6,8,9, 10,11,13	C, .01UF, 25V, ±20%	150971
C7,12	M, 33PF, 500V, ±5%	153711
C5	P, .01UF, 50V, ±10%	151020
C4	CAPACITOR, M, 82PF, 500V, ±5%	153717
CR3	DIODE, SZ, 3.4V, ±1%	150888
CR1,2	DIODE, SZ, 15V, ±1%	150909
A1,2,3	INTEGRATED CIRCUIT, LM301A	150645
R1, 2	RESISTOR COMP, 750HMS, 1/2W, ±5%	151600
R3,13,16, 23	10K, 1/4W, ±5%	151507
R21	100K, 1/4W, ±5%	151531
R6	8.2K, 1/4W, ±5%	151505
R22	4.7K, 1/4W, ±5%	151499
R29	5.6K, 1/4W, ±5%	151501
R5	3K, 1/4W, ±5%	151494
R15	1K, 1/4W, ± 5%	151483
R12	COMP, 470 OHMS, 1/4W, ±5%	151475
R7,18,19, 20,28	MF, 10K, 1/8W, ±1%	153059
R17,24	3.48K, 1/8W, ±1%	153207
R9,14	100 OHMS, 1/8W, ±1%	152963
R11	19.1K, 1/8W, ±1%	153086
R10	30.1K, 1/8W, ±1%	153105
R25,27	MF, 5.11K, 1/8W, ±1%	153223
R4,26	VAR, 10K, 3/4W, ±20%	153409
R8	RESISTOR, MF, 2K, 1/8W, ±1%	153040
Q1	TRANSISTOR, 2N2222A	150768
TP1-5	TERMINAL, TURRET	150374
.	TAG ENGINEERING CHANGE	200304



NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350
3. Q1, A1 THRU A3 HEIGHT NOT TO EXCEED .330.

REFERENCE DOCUMENTS		E.C. LEVEL
SCH. DIAG.	001437	790
ARTMASTER	001438	1375
FABRICATION	001439	1375
TEST SPEC.	001440	790

MATERIAL SEE B/M	NO 001436	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC. ±
CASE DEPTH			3 PLACE DEC. ±
HARDNESS			ANGLES ±
SURFACE TREATMENT		CORNERS AND OR EDGES BROKEN	OUTSIDE MAX
001436	C	RADII UNLESS OTHERWISE NOTED	INSIDE MAX

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	P.C. BOARD ASSEMBLY		
	TACHOMETER AMPLIFIER		
DESIGN		TYPE	
DETAIL		SCALE	2/1
CHECK		DRAW.	
APPRO.		CHECK	

001436

001436

REF DESIG	DESCRIPTION	M. E. G. PART NO.
———	PRINTED CIRCUIT BOARD	001439
C1	CAPACITOR, T, 4.7UF, 10V, ±10%	151124
C2,3	T, 2.2UF, 35V, ± 10%	151127
C6,8,9, 10,11,13	C, .01UF, 25V, ±20%	150971
C7,12	M, 33PF, 500V, ±5%	153711
C5	P, .01UF, 50V, ±10%	151020
C4	CAPACITOR, M, 82PF, 500V, ±5%	153717
CR3	DIODE, SZ, 3.4V, ±1%	150888
CR1,2	DIODE, SZ, 15V, ±1%	150909
A1,2,3	INTEGRATED CIRCUIT, LM301A	150645
R1, 2	RESISTOR COMP, 750HMS, 1/2W, ±5%	151600
R3,13,16, 23	10K, 1/4W, ±5%	151507
R21	100K, 1/4W, ±5%	151531
R6	8.2K, 1/4W, ±5%	151505
R22	4.7K, 1/4W, ±5%	151499
R29	5.6K, 1/4W, ±5%	151501
R5	3K, 1/4W, ±5%	151494
R15	1K, 1/4W, ± 5%	151483
R12	COMP, 470 OHMS, 1/4W ±5%	151475
R7,18,19, 20,28	MF, 10K, 1/8W, ±1%	153059
R17,24	3.48K, 1/8W, ±1%	153207
R9,14	100 OHMS, 1/8W, ±1%	152963
R11	19.1K, 1/8W, ±1%	153086
R10	30.1K, 1/8W, ± 1%	153105
R25,27	MF, 5.11K, 1/8W, ± 1%	153223
R4,26	VAR, 10K, 3/4 W, ± 20%	153409
R8	RESISTOR, MF, 2K, 1/8W, ±1%	153040
Q1	TRANSISTOR, 2N2222A	150768
TP1-5	TERMINAL, TURRET	150374
	TAG ENGINEERING CHANGE	200304

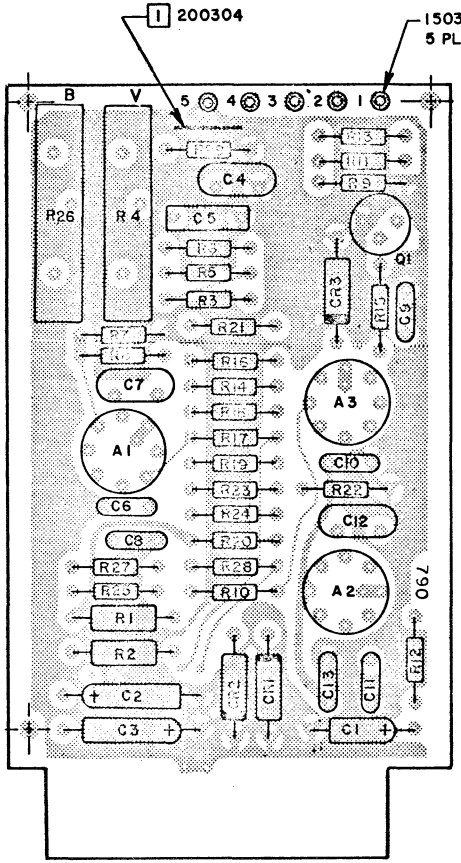
NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350
3. Q1, A1 THRU A3 HEIGHT NOT TO EXCEED .330.

001436

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
630 A	200490	3-25-68	14	9-8-69	441
	MULTI-USE	3-27-68	34	11-21-69	559
		6-10-68	111	1-16-69	685
		7-18-68	151	MAY 18, 70	790
		2-14-69	246		

001436



001436

REFERENCE DOCUMENTS		E.C. LEVEL
SCH. DIAG.	001437	790
ARTMASTER	001438	790
FABRICATION	001439	790
TEST SPEC.	001440	790

MATERIAL SEE B/M 001436	TOLERANCE UNLESS OTHERWISE NOTED	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION
FINISH		NAME P.C. BOARD ASSEMBLY
HARDNESS		TACHOMETER AMPLIFIER
HEAT TREATMENT		DESIGN TYPE
001436 C	CORNER AND EDGE BREAKS RADII UNLESS OTHERWISE NOTED	DETAIL SCALE 2/1
		CHECK DRAW
		APPRO CHECK

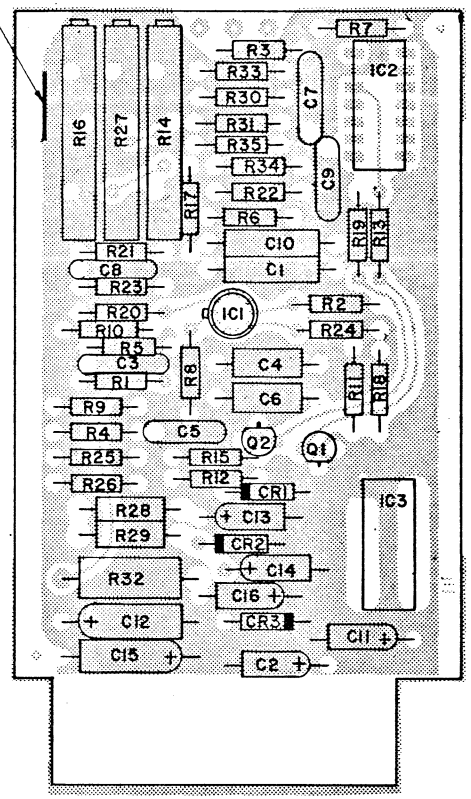
001436

001436

REF DESIG	DESCRIPTION	P.S.C. PART NO.
———	PRINTED CIRCUIT BOARD	001439
C1, 10	CAPACITOR, .0015UF, 100V ±5%	151052
C13,14,16	1UF, 35V ±10%	151116
C 3,5,7,8,9	.1UF 25V ±20%	150990
C4,6	82PF, 500V ± 5%	151220
C11	4.7UF, 10V ±10%	151124
C12, 15	2.2UF, 35V ±10%	151127
C2	CAPACITOR, .1UF, 35V, ± 10%	151096
CR1, 2	DIODE, IN 4736 , 6.8V	150847
CR2	DIODE, IN 4742 , 12V	150848
IC2	INTEG CIRCUIT, MC1710CL	150664
IC1	INTEG CIRCUIT, MC1520G	150655
IC3	INTEG CIRCUIT, SP659A	150654
R1,10,17,23	RESISTOR, 22.1K, 1/8W ±1%	153092
R2,11,18,24	470Ω, 1/4W ±5%	151475
R3,7,33	1K, 1/4W ±5%	151483
R4	27.4K, 1/8W ±1%	153101
R5,21	56.2K, 1/8W ±1%	153275
R6,22	90.9K, 1/8W ±1%	153255
R8,20	47.5K, 1/8W ±1%	153268
R25,26	10K, 1/8W ±1%	153059
R12,15	10K, 1/4 W ±5%	151507
R13,19	300Ω, 1/4W ±5%	151470
R28	680Ω, 1/2W ±5%	151623
R29	560Ω, 1/2W ±5%	151621
R30	3.48K, 1/8W ±1%	153207
R31	3.74K, 1/8W ±1%	153210
R32	330Ω, 1 W ±5%	151769
R34,35	13.7K, 1/8W ± %	153072
R9	RESISTOR, 6.8K, 1/4W, ±5%	151503
R14	POT., 5K, 3/4W ±20%	153408
R16	POT., 50K, 3/4W ±20%	153412
R27	POT., 1K, 3/4W ±20%	153406
Q1,2	TRANSISTOR, 2N3906	150736
———	TAG, ENGINEERING CHG.	200304

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
630 A	200490	3-25-68	14	9-8-69	441
630 B	200495	3-27-68	34	11-21-69	559
620	202032	6-10-68	111		
630-1 (CONV.)	200762	7-18-68	151		
630-1	200878	2-14-69	246		
630-3	200754				

200304



IN PROCESS

E/C 685

001436

REFERENCE DOCUMENTS		E.C. LEVEL
SCH. DIAG.	001437	151
ARTMASTER	001438	441
FABRICATION	001439	441
TEST SPEC.		

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL	SEE B/M
FINISH	
CASE DEPTH	
HARDNESS	
SURFACE TREATMENT	

001436 C

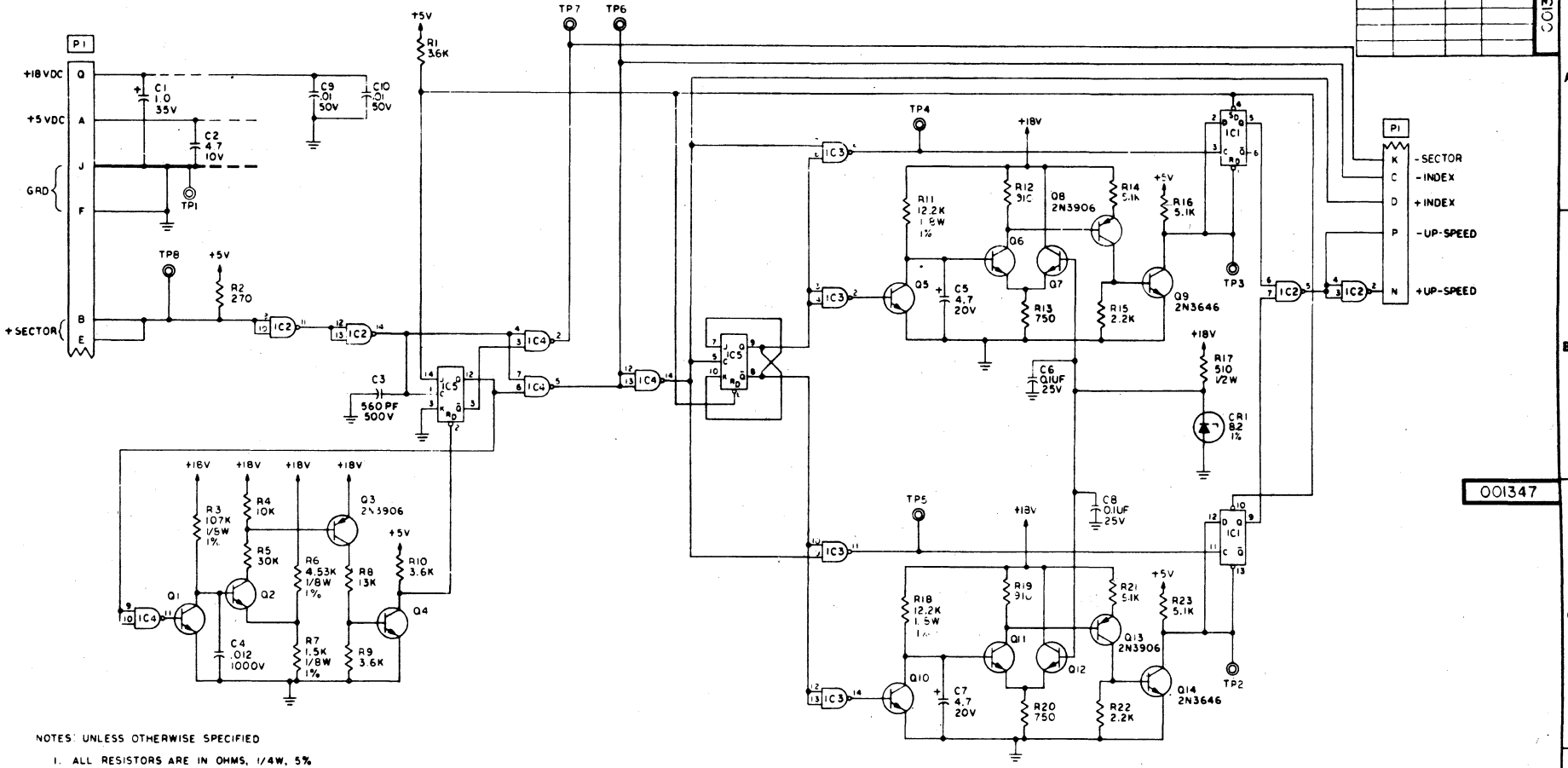
TOLERANCE UNLESS OTHERWISE NOTED
DECIMALS ± .010
FRACTIONS ±
ANGLES
OUTSIDE MAX
INSIDE MAX
CORNERS AND OR EDGES BROKEN
RADII UNLESS OTHERWISE NOTED

Peripheral Systems Corporation
A DIVISION OF MEMOREX CORPORATION

P.C. BOARD ASSEMBLY
TACHOMETER AMPLIFIER

DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK	JDM	6/11/68	DRAW	K.B.	6-10-68
APPRO	[illegible]	[illegible]	CHECK	[illegible]	11JUN68

001436



RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001346		274		

001347

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%
2. ALL CAPACITORS ARE IN MICROFARADS
3. ALL TRANSISTORS ARE 2N3904
4. CONNECT PIN 7 OF IC1 TO GRD, AND PIN 14 TO +5VDC
5. CONNECT PIN 1 OF IC2, IC3 & IC4 TO GRD, AND PIN 8 TO +5VDC
6. CONNECT PIN 11 OF IC5 TO GRD, AND PIN 4 TO +5VDC
7. IC1 IS A SN7474N
8. IC2, IC3 & IC4 ARE SP680A
9. IC5, IS A SN7473N

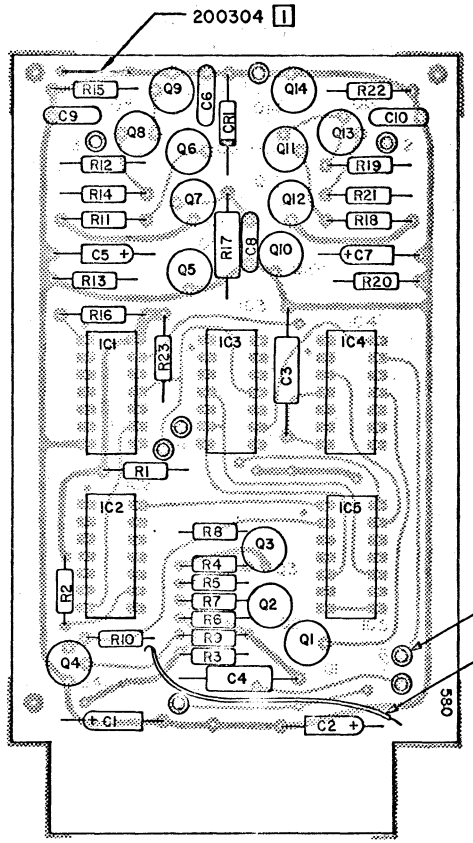
FOR INFORMATION ONLY

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation
CASE DEPTH			3 PLACE DEC	NAME SCHEMATIC DIAGRAM
HARDNESS			ANGLES	UP-SPEED DETECTOR III
SURFACE TREATMENT		CORNERS AND OR EDGES BROKEN	OUTSIDE MAX	DESIGN TYPE
001347	D	RADII UNLESS OTHERWISE NOTED	INSIDE MAX	DETAIL SCALE NONE
				CHECK TEG DRAW
				APPRO CHECK BRH 3/8/69

001347

REF DESIG	DESCRIPTION	M. E. G. PART NO.
———	PRINTED CIRCUIT BOARD	001349
C1	CAPACITOR T, 1UF, 35V, ±10%	151116
C2	T, 4.7UF, 10V, ±10%	151124
C5,7	T, 4.7UF, 20V, ±10%	151149
C3	P, 560PF 500V ±5%	151240
C4	M, .012UF, 100V, ±10%	151064
C6,8	C, .1UF, 25V, ±20%	150990
C9,10	CAPACITOR C, .01UF, 50V, ±10%	150991
CR1	DIODE, ZENER, 8.2V	150903
IC 1	INTEGRATED CIRCUIT, SN 7474 N	150673
IC 2,3,4	" " " SP 680 A	150656
IC 5	INTEGRATED CIRCUIT, SN 7473N	150672
R1, 9,10	RESISTOR, COMP, 3.6K, 1/4W, ±5%	151496
R2	COMP, 270 OHM, 1/4W, ±5%	151469
R3	MF, 107K, 1/8W, ±1%	153302
R4	COMP, 10K, 1/4W, ±5%	151507
R5	COMP. 30K, 1/4W, ±5%	151518
R6	MF, 4.53K, 1/8W, ±1%	153218
R7	MF, 1.5K, 1/8W, ±1%	153028
R8	COMP, 13K, 1/4W, ±5%	151510
R11, 18	MF, 12.7K, 1/8W, ±1%	153069
R12, 19	COMP, 910 OHM, 1/4W, ±5%	151482
R13, 20	COMP. 750 OHM, 1/4W, ±5%	151480
R15, 22	COMP, 2.2K, 1/4W, ±5%	151491
R14,16,21,23	COMP, 5.1K, 1/4W, ±5%	151500
R17	RESISTOR, COMP, 510 OHM 1/2W, ±5%	151620
Q1,2,4,5,6, Q7,10,11,12	TRANSISTOR, 2N 3904	150735
Q3, 8, 13	TRANSISTOR, 2N 3906	150736
Q9, 14	TRANSISTOR, 2N 3646	150734
———	TERMINAL, TURRET	150374
———	WIRE-WRAP, SOLID	150161
———	TAG, ENGINEERING CHANGE	200304

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
630 A	200490-60~	2-26-69	274		
630 B	200495-50~	4-14-69	289		
630-1	200762	12-16-69	580		
		Jan 70	1146		



150374 (SWAGE FARSIDE) 8 PLACES

150161

001346

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001347	274
ARTMASTER	001348	580
FABRICATION	001349	580

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350
3. AFTER SOLDERING TRIMMED LEAD HEIGHT NOT TO EXCEED .063.

MATERIAL SEE B/M NO 001346		TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001346	C	RADII UNLESS OTHERWISE NOTED	—

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME P.C. BOARD ASSEMBLY

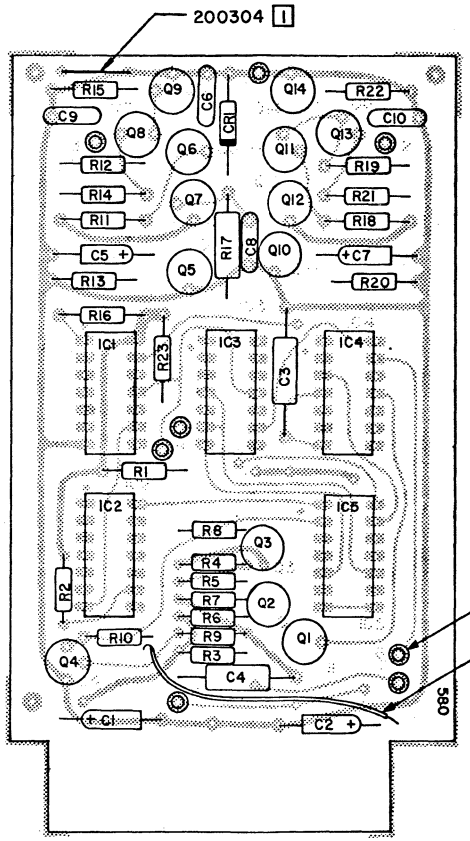
UP-SPEED DETECTOR III

DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK	TZG	3/10/69	DRAW	C.ONO	2-26-69
APPRO	K.R.C.	3/15/69 Plant	CHECK	DRH	3/8/69

001346

REF DESIG	DESCRIPTION	M. E. G. PART NO.
———	PRINTED CIRCUIT BOARD	001349
C1	CAPACITOR T, 1UF, 35V, ±10%	151116
C2	T, 4.7UF, 10V, ±10%	151124
C5, 7	T, 4.7UF, 20V, ±10%	151149
C3	P, 560PF 500V ±5%	151240
C4	M, .012UF, 100V, ±10%	151064
C6, 8	C, .1UF, 25V, ±20%	150990
C9, 10	CAPACITOR C, .01UF, 50V, ±10%	150991
CR1	DIODE, ZENER, 8.2V	150903
IC 1	INTEGRATED CIRCUIT, SN 7474 N	150673
IC 2,3,4	" " " SP 680 A	150656
IC 5	INTEGRATED CIRCUIT, SN 7473N	150672
R1, 9, 10	RESISTOR, COMP, 3.6K, 1/4W, ±5%	151496
R2	COMP, 270 OHM, 1/4W, ±5%	151469
R3	MF, 107K, 1/8W, ±1%	153302
R4	COMP, 10K, 1/4W, ±5%	151507
R5	COMP, 30K, 1/4W, ±5%	151518
R6	MF, 4.53K, 1/8W, ±1%	153218
R7	MF, 1.5K, 1/8W, ±1%	153028
R8	COMP, 13K, 1/4W, ±5%	151510
R11, 18	MF, 12.7K, 1/8W, ±1%	153069
R12, 19	COMP, 910 OHM, 1/4W, ±5%	151482
R13, 20	COMP, 750 OHM, 1/4W, ±5%	151480
R15, 22	COMP, 2.2K, 1/4W, ±5%	151491
R14,16,21,23	COMP, 5.1K, 1/4W, ±5%	151500
R17	RESISTOR, COMP, 510 OHM 1/2W, ±5%	151620
Q1,2,4,5,6, Q7,10,11,12	TRANSISTOR, 2N 3904	150735
Q3, 8, 13	TRANSISTOR, 2N 3906	150736
Q9, 14	TRANSISTOR, 2N 3646	150734
———	TERMINAL, TURRET	150374
———	WIRE-WRAP, SOLID	150161
———	TAG, ENGINEERING CHANGE	200304

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
630A	200490-60~	2-26-69	274		
630B	200495-50~	4-14-69	289		
630-1	200762	12-16-69	580		



001346

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001347	274
ARTMASTER	001348	580
FABRICATION	001349	580

NOTES: UNLESS OTHERWISE SPECIFIED

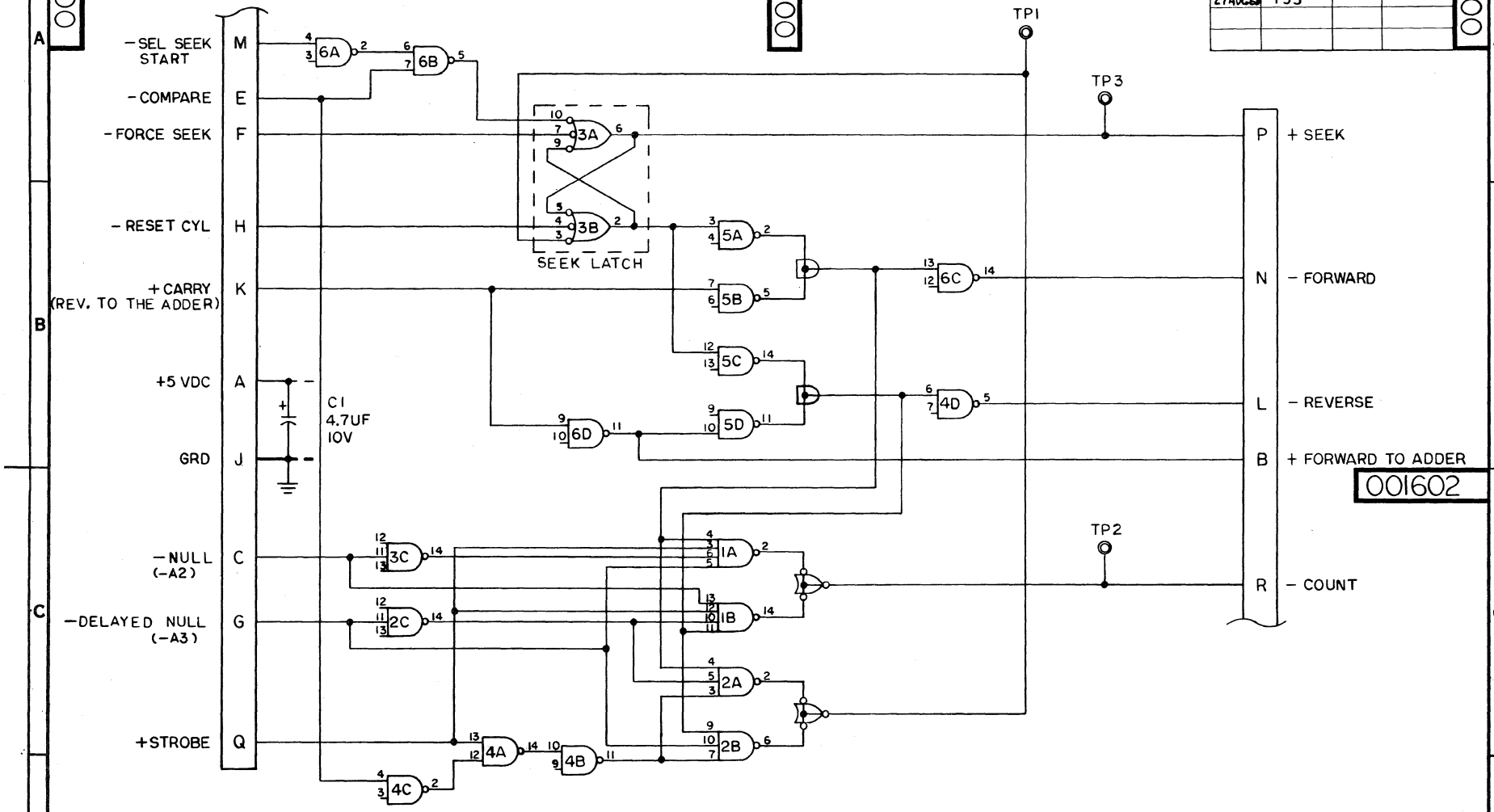
1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

001346

MATERIAL SEE B/M NO 001346		TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX.
SURFACE TREATMENT			INSIDE MAX.
001346	C	RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	P.C. BOARD ASSEMBLY				
	UP-SPEED DETECTOR III				
DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK	TEG	3/10/69	DRAW	C.ONO	2-26-69
APPRO			CHECK	SRH	3/8/69



RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001601	5/27/68	104		
	7-30-68	171		
	27AUG68	195		

NOTES UNLESS OTHERWISE SPECIFIED

1. IC1 IS SP616A
2. IC'S 2&3 ARE SP670A
3. IC'S 4,5&6 ARE SP680A
4. CONNECT ALL IC S PIN 1 TO GRD, PIN 8 TO +5VDC

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
CASE DEPTH			3 PLACE DEC ±
HARDNESS			ANGLES ±
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
001602	C	RADII UNLESS OTHERWISE NOTED	INSIDE MAX

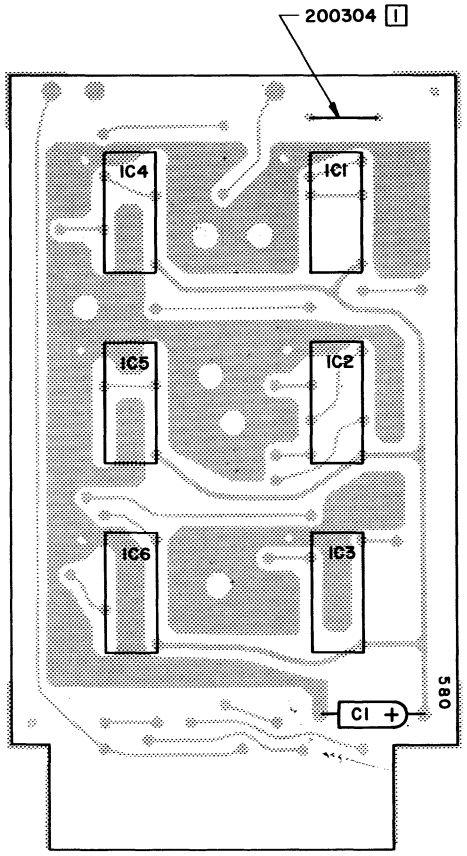
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	SCHEMATIC DIAGRAM SEEK FORWARD/REVERSE				
DESIGN			TYPE		
DETAIL			SCALE	NONE	
CHECK	MC C	6/10/68	DRAW	K.B.	5-27-68
APPRO			CHECK	R.V.P.	P.J.W.

001602

REF DESIG	DESCRIPTION	P.S.C. PART NO.
———	PRINTED CIRCUIT BOARD	001604
C1	CAPACITOR, 4.7UF, 10V ±10%	151124
IC1	INTEG. CIRCUIT, SP616A	150650
IC2,3	INTEG. CIRCUIT, SP670A	150655
IC4,5,6	INTEG. CIRCUIT, SP680A	150656
———	TAG, ENGINEERING CHG.	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490-60~	6-7-68	104		
200495-50~	7-30-68	171		
	27AUG68	193		
	11-19-68	219		
	1-2-70	580		



REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001602	195
ARTMASTER	001603	580
FABRICATION	001604	580

NOTES: UNLESS OTHERWISE SPECIFIED

[1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER

2 COMPONENT HEIGHT NOT TO EXCEED .350

SEE B/M 001601

001601 C

Peripheral Systems Corporation

P.C. BOARD ASSEMBLY

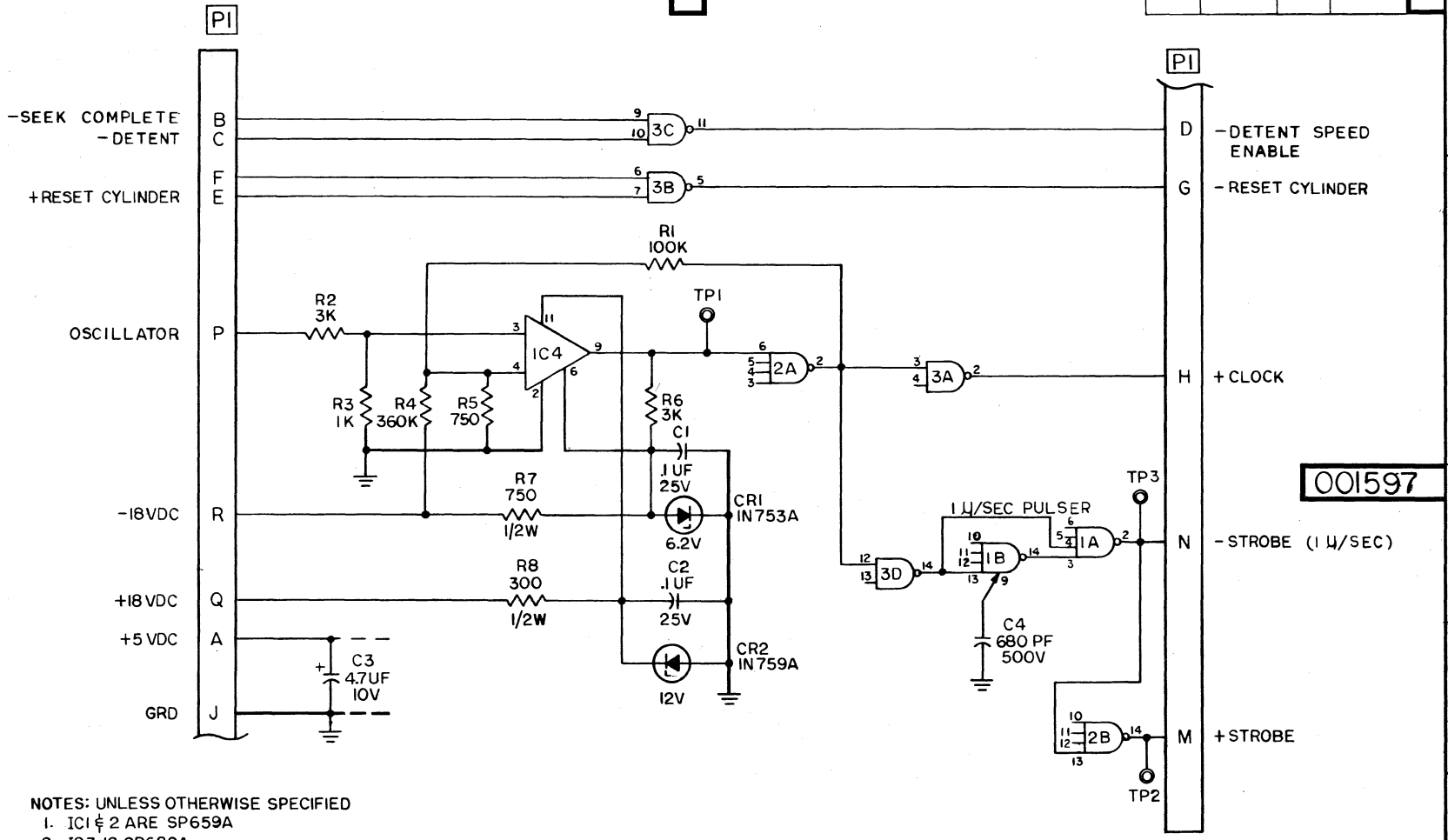
SEEK FORWARD / REVERSE

SIZE			TYPE	
DETAIL			SCALE	2 / 1
MFG.	MCL	6/19/68	DRAW	K.B. 6-7-68
APPRO		6-12-68	CHECK	6Jun68

001601

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	C.
001596	5-22-68	104		
	7-30-68	171		

001597



001597

NOTES: UNLESS OTHERWISE SPECIFIED
1. IC1 & 2 ARE SP659A
2. IC3 IS SP680A
3. IC4 IS 1710CP, MOTOROLA
4. ALL RESISTORS ARE OHMS, 1/4W ±5%
5. CONNECT ALL IC PINS 1 TO GRD, PINS 8 TO +5V EXCEPT IC4

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
			3 PLACE DEC ±		
CASE DEPTH			ANGLES ±	NAME	SCHEMATIC DIAGRAM
HARDNESS					CLOCK GENERATOR
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN	TYPE
001597	C		INSIDE MAX	DETAIL	SCALE NONE
		RADII UNLESS OTHERWISE NOTED		CHECK MC 6/9/68	DRAW K.B. 5-22-68
				APPRO K.K.T. 6/10/68	CHECK R.L.E. 27 may 68

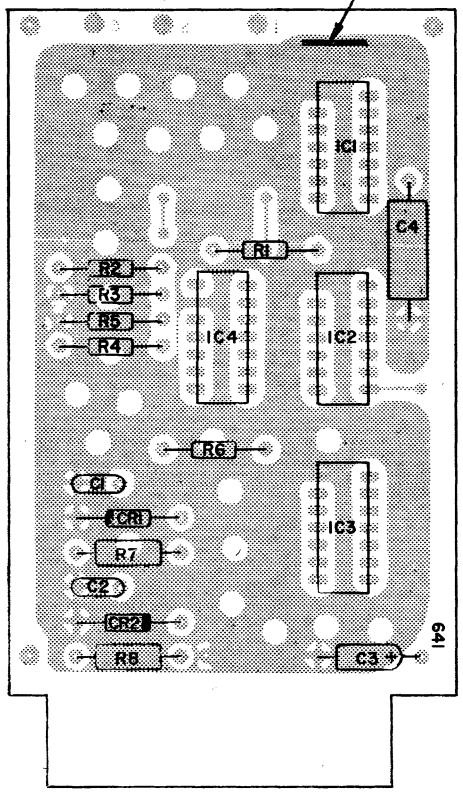
001597

001596 001596 001596

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490	6-10-68	104	Aug 6, 70	641
200495	7-30-68	171		
	2-14-69	246		
	3-3-69	219		
	1-2-70	580		

REF DESIG	DESCRIPTION	M. E. G. PART NO.
———	PRINTED CIRCUIT BOARD	001599
C1,C2	CAPACITOR, .1UF, 25V ± 20%	150990
C3	CAPACITOR, 4.7UF, 10V ± 10%	151124
C4	CAPACITOR, 680PF, 500V ± 5%	151242
CR1	DIODE, Z, IN753A, 6.2V	150840
CR2	DIODE, Z, IN759A, 12V	150841
R1	RESISTOR, COMP, 100K, 1/4W, ±5%	151531
R2, R6	3K, 1/4W, ± 5%	151494
R3	1K, 1/4W, ± 5%	151483
R4	360K, 1/4W, ± 5%	151544
R5	750Ω, 1/4W, ± 5%	151480
R7	750Ω, 1/2W, ± 5%	151624
R8	RESISTOR, COMP, 300Ω, 1/2W, ±5%	151614
IC1, IC2	INTEGRATED CIRCUIT, SP659A	150654
IC3	INTEGRATED CIRCUIT, SP680A	150656
IC4	INTEGRATED CIRCUIT, MC1710CP	150664
———	TAG, ENGINEERING CHANGE	200304

200304 [1]



001596

NOTES: UNLESS OTHERWISE SPECIFIED
[1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

REFERENCE DOCUMENTS		E.C. LEVEL
SCH. DIAG.	001597	171
ARTMASTER	001598	641
FABRICATION	001599	641
TEST SPEC.		

MATERIAL SEE B/M NO. 001596	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION
CASE DEPTH		3 PLACE DEC ±	NAME PC. BOARD ASSEMBLY
HARDNESS		ANGLES ±	CLOCK GENERATOR
SURFACE TREATMENT	CORNERS AND OR EDGES BROKEN	OUTSIDE MAX	DESIGN TYPE
001596 C		INSIDE MAX	DETAIL SCALE 2/1
	RADII UNLESS OTHERWISE NOTED		CHECK HCL 6/10/68 DRAW K.B. 6-10-68
			APPRO K.E.M. 6/12/68 CHECK R.P.E. 10 JUN 68

001596

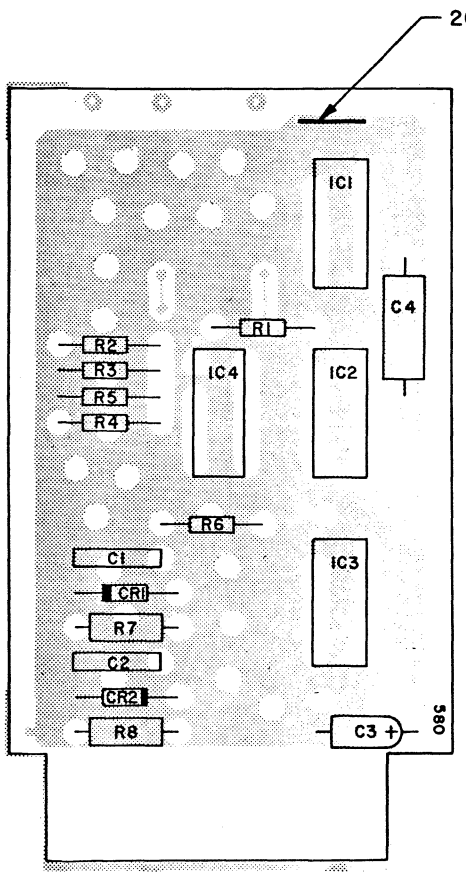
001596

REF DESIG	DESCRIPTION	P.S.C. PART NO.
———	PRINTED CIRCUIT BOARD	001599
C1,2	CAPACITOR, .1UF, 25V ±20%	150990
C3	CAPACITOR, 4.7UF, 10V ±10%	151124
C4	CAPACITOR, 680PF, 500V ±5%	151242
CR1	DIODE, Z, IN753A, 6.2V	150840
CR2	DIODE, Z, IN759A, 12V	150841
R1	RESISTOR, 100K, 1/4W ±5%	151531
R2,6	3K, 1/4W ±5%	151494
R3	1K, 1/4W ±5%	151483
R4	360K, 1/4W ±5%	151544
R5	750Ω, 1/4W ±5%	151480
R7	750Ω, 1/2W ±5%	151624
R8	RESISTOR, 300Ω, 1/2W ±5%	151614
IC1,2	INTEG CIRCUIT, SP659A	150654
IC3	INTEG. CIRCUIT, SP680A	150656
IC4	INTEG. CIRCUIT, MC1710CP	150664
———	TAG, ENGINEERING CHANGE	200304

001596

RELEASED FOR A	DATE	CHANGE NO	DATE	CHANGE
200490-60	6-10-68	104		
200495-50	7-30-68	171		
	2-14-69	246		
	3-3-69	219		
	1-2-70	580		

001596



001596

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001597	171
ARTMASTER	001598	580
FABRICATION	001599	580

NOTES: UNLESS OTHERWISE SPECIFIED

[1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER

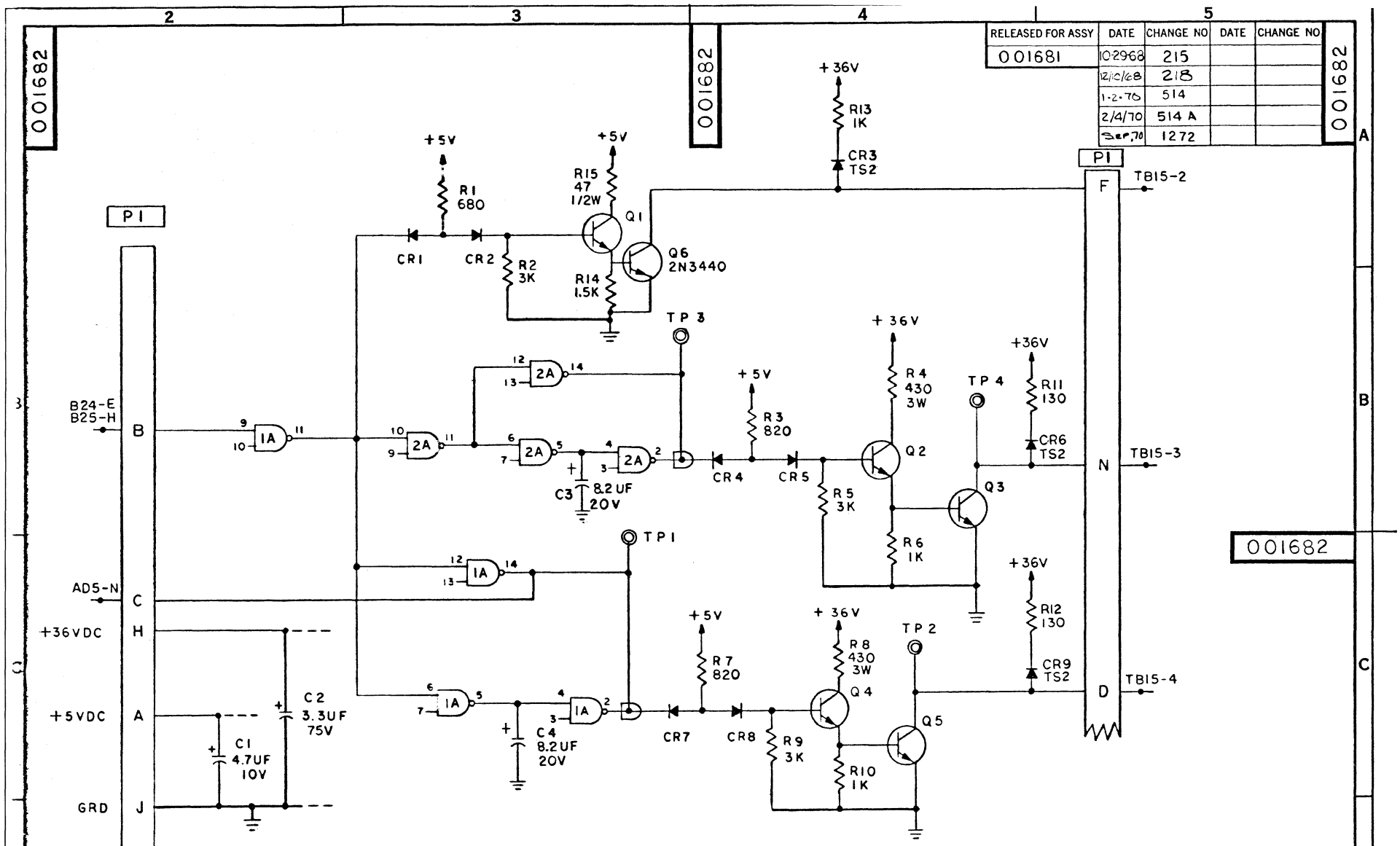
2 COMPONENT HEIGHT NOT TO EXCEED .750

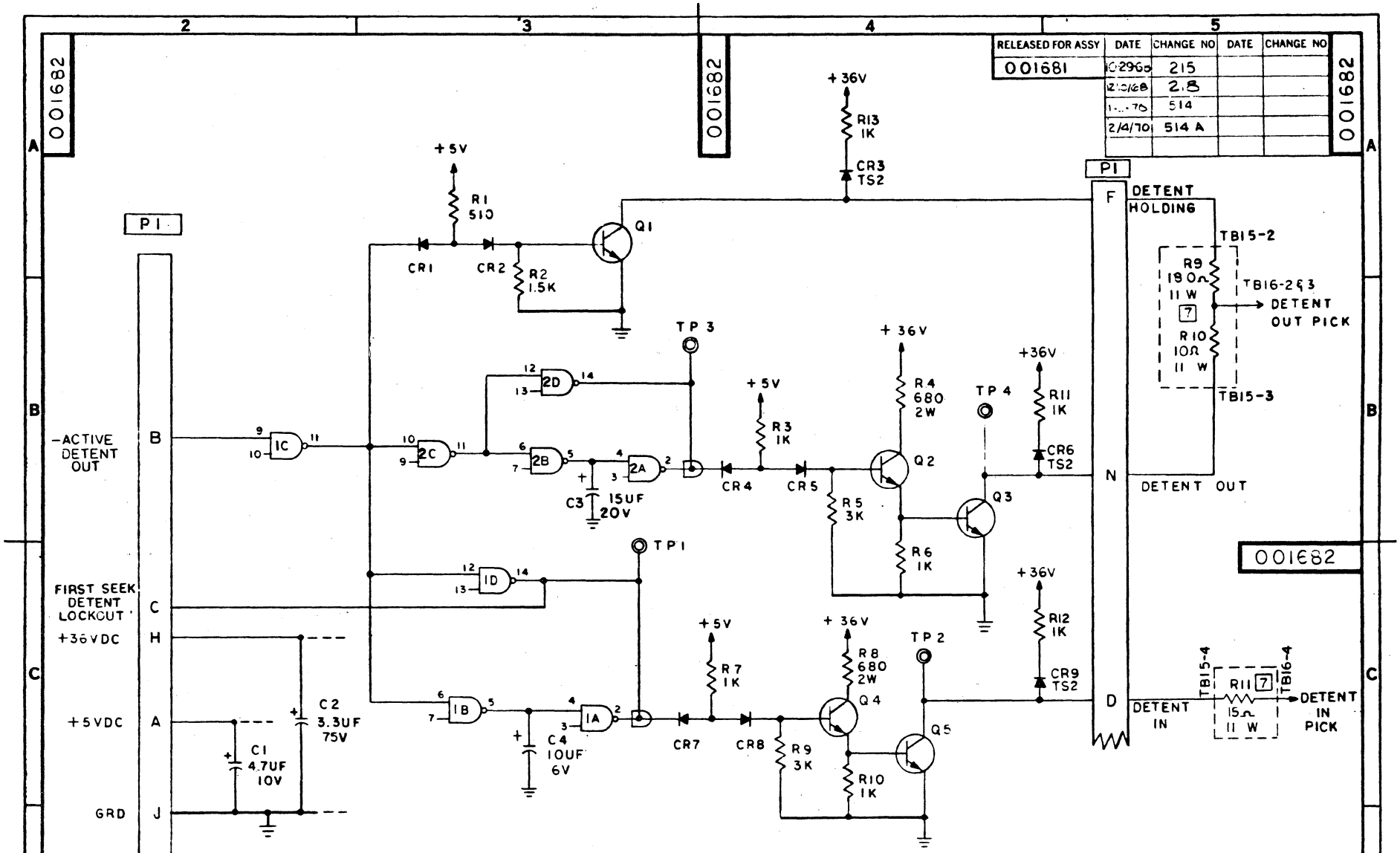
SIZE	B/M	001596
001596	C	

Peripheral Systems Corporation

P.C. BOARD ASSEMBLY
CLOCK GENERATOR

		TYPE	2 / 1
DRAWN	MC L.	6/10/68	K.B. 6-18-68
CHECKED	[illegible]	6-12-68	R.V.E. 6/18/68
ENGR			
MFG			

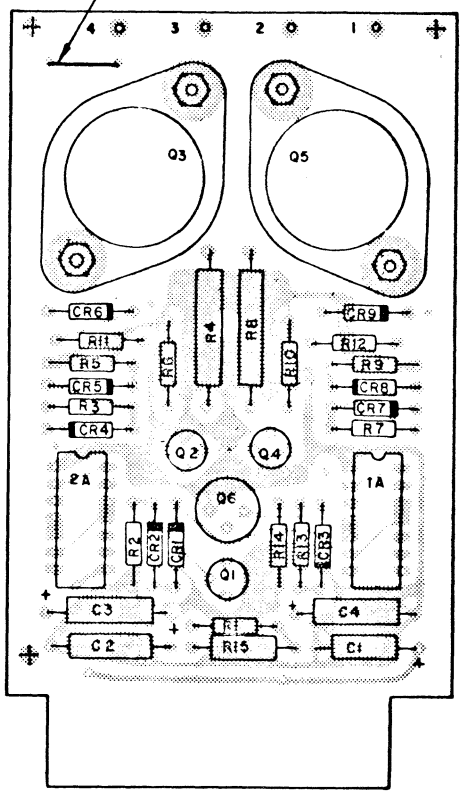

001682
001682
001682
001682
001682
001682
001682
001682
RELEASED FOR ASSY
001681
DATE
CHANGE NO
DATE
CHANGE NO
10-29-68
215
12/10/68
218
1-2-70
514
2/4/70
514 A
Sept 70
1272
P1
P1
+36V
R13
1K
CR3
TS2
+5V
R1
680
+5V
R15
47
1/2W
Q1
Q6
2N3440
CR1
CR2
R2
3K
R14
1.5K
TP 3
+36V
R4
430
3W
+36V
R11
130
TP 4
+5V
R3
820
CR6
TS2
TBI5-2
TBI5-3
TBI5-4
F
N
D
B24-E
B25-H
B
AD5-N
C
+36VDC
H
+5VDC
A
GRD
J
1A
2A
C3
8.2 UF
20V
CR4
CR5
Q2
Q3
R5
3K
R6
1K
TP 1
+36V
R12
130
CR9
TS2
+5V
R7
820
+36V
R8
430
3W
TP 2
Q4
Q5
CR7
CR8
R9
3K
R10
1K
C1
4.7UF
10V
C2
3.3UF
75V
C4
8.2UF
20V
NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTORS ARE IN OHMS, 1/4W, ± 5%.
2. IC1 & IC2 ARE SP680A.
3. CONNECT ALL IC PIN 1 TO GRD, PIN 8 TO +5V.
4. ALL DIODES ARE IN4148.
5. Q1 Q2 AND Q4 ARE 2N2222A
6. Q3 & Q5 ARE DTS-411.
MATERIAL
NO
CASE DEPTH
HARDNESS
SURFACE TREATMENT
001682
C
TOLERANCE UNLESS OTHERWISE NOTED
2 PLACE DEC ±
3 PLACE DEC ±
ANGLES ±
CORNERS AND/OR EDGES BROKEN
OUTSIDE MAX
INSIDE MAX
RADII UNLESS OTHERWISE NOTED
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION
NAME
SCHEMATIC DIAGRAM
ACTUATOR LOGIC & DRIVER II
DESIGN
TYPE
DETAIL
SCALE
CHECK
DRAW
10-27-68
APPRO
CHECK
SRH
10-30-68

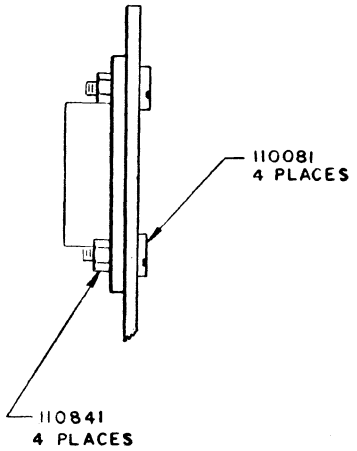

001682
RELEASED FOR ASSY
001681
DATE
CHANGE NO
215
2.8
514
514 A
+36V
R13 1K
CR3 TS2
+5V
R1 510
Q1
CR1
CR2
R2 1.5K
P1
F
DETENT HOLDING
TB15-2
R9 190Ω 11 W
7
R10 10Ω 11 W
TB16-2&3
DETENT OUT PICK
TB15-3
TP 3
TP 4
R4 680 2W
R11 1K
CR6 TS2
R3 1K
CR4
CR5
Q2
Q3
R5 3K
R6 1K
N
DETENT OUT
-ACTIVE DETENT OUT
B
1C
2C
2D
2B
2A
C3 15UF 20V
TP1
1D
FIRST SEEK DETENT LOCKOUT
C
+36VDC
H
R12 1K
CR9 TS2
TP 2
R7 1K
R8 680 2W
Q4
Q5
+5VDC
A
C2 3.3UF 75V
C1 4.7UF 10V
1B
1A
C4 10UF 6V
CR7
CR8
R9 3K
R10 1K
D
DETENT IN
TB15-4
TB16-4
R11 7 15Ω 11 W
DETENT IN PICK
GRD
J
NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTORS ARE IN OHMS, 1/4W, ±5%.
2. IC1 & IC2 ARE SP680A.
3. CONNECT ALL IC PIN 1 TO GRD, PIN 8 TO +5V.
4. ALL DIODES ARE IN4148.
5. Q2 & Q4 ARE 2N3568
6. Q3 & Q5 ARE 2N4240
7. POWER RESISTORS SEE DWG. 200490
8. Q1 IS A 2N3440
MATERIAL
NO
CASE DEPTH
HARDNESS
SURFACE TREATMENT
001682
C
TOLERANCE UNLESS OTHERWISE NOTED
2 PLACE DEC ±
3 PLACE DEC ±
ANGLES ±
CORNERS AND/OR EDGES BROKEN
OUTSIDE MAX
INSIDE MAX
RADII UNLESS OTHERWISE NOTED
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION
NAME SCHEMATIC DIAGRAM
ACTUATOR LOGIC & DRIVER II
DESIGN
DETAIL
CHECK
APPRO
TYPE
SCALE
DRAW
CHECK
10-30-68

REF DESIG	DESCRIPTION	M. E. G. PART NO.
———	PRINTED CIRCUIT BOARD	001684
C1	CAPACITOR,T,4.7UF,10V,±10%	151124
C2	CAPACITOR,T,3.3UF,75V,±20%	151152
C3,4	CAPACITOR,T,8.2UF,20V,±10%	151131
CR1,2,4,5,7,8	DIODE, IN4148	150834
CR3,6,9	DIODE, TS-2	150826
1A,2A	INTEGRATED CIRCUIT,SP680A	150656
R11,12	RESISTOR,COMP,130Ω,1/4W,±5%	151462
R1	680Ω	151479
R3,7	820Ω	151481
R6,10,13	1K	151483
R14	1.5K	151487
R2,5,9	3K, 1/4W, ±5%	151494
R15	RESISTOR,COMP,47Ω,1/2W,±5%	151595
R4,8	RESISTOR,WW,430Ω,3W,±5%	153439
Q3,5	TRANSISTOR, DTS411	201449
Q6	TRANSISTOR, 2N3440	150744
Q1,2,4	TRANSISTOR, 2N2222A	150768
	SCREW BIND HD,6-32x.375	110081
	NUT, KEP 6-32	110841
	TAG,ENGINEERING CHANGE	200304

001681

200304 [1]





001681

NOTES: UNLESS OTHERWISE SPECIFIED

[1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER.

2. COMPONENT HEIGHT NOT TO EXCEED .350.

3. Q1, Q2, Q4, Q6 HEIGHT NOT TO EXCEED .310

REFERENCE DOCUMENTS		E.C. LEVEL
SCH. DIAG.	001682	1272
ARTMASTER	001683	1272
FABRICATION	001684	1272
TEST SPEC	001685	1272

DATE	CHANGE NO.	DATE	CHANGE NO.
10-30-68	215		
12-10-68	218		
1-2-70	514		
SEP. 70	1272		

001681

RELEASED FOR ASSEMBLY
200490-60
200495-50

MATERIAL NO.	SEE B/M NO. 001681	MUST CONFORM TO ENG. SPEC 880000	TOLERANCE UNLESS OTHERWISE NOTED
CASE DEPTH		TECHNICAL APPROVAL	LINEAR ± .XX ± .XXX
HARDNESS			ANGULAR ±
SURFACE TREATMENT NO.			CORNERS EDGES BROKEN
STD CODE	C		OUTSIDE MAX
			INSIDE MAX

MEMOREX EQUIPMENT GROUP

NAME P.C. BOARD ASSEMBLY
ACTUATOR LOGIC & DRIVER II

DESIGN
DETAIL SCK SEP 70
CHECK Tal SEP 23,70
APPRO [illegible] 9/23/70

SCALE 2/1

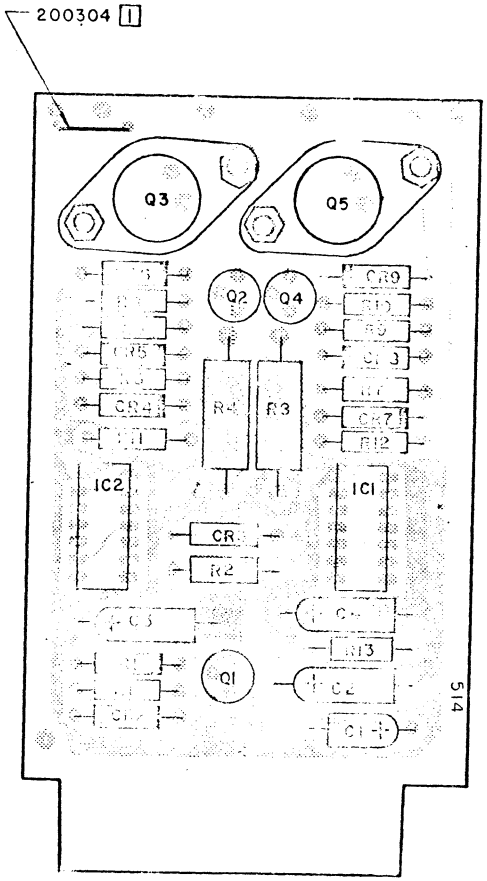
001681

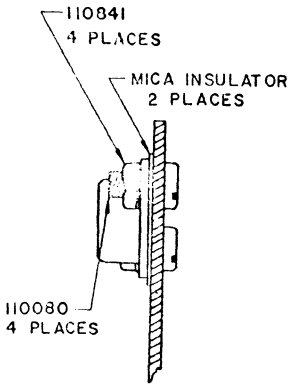
001681

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200499-00	10-30-68	215		
200405-50	12-10-68	218		
	1-2-70	514		
	June 70	1146		

001681

REF DESIG	DESCRIPTION	M. E. G PART NO.
———	PRINTED CIRCUIT BOARD	001684
C1	CAPACITOR, T, 4.7UF, 10V. ±10%	151124
C2	T, 3.3 UF, 75V. ± 20%	151152
C3	T, 15UF, 20V. ± 10%	151134
C4	CAPACITOR, T, 10UF, 6V. ±10%	151143
CR1,2,4,5,7,8	DIODE, IN4148	150838
CR3,6,9	DIODE, TS-2	150826
IC1,2	INTEGRATED CIRCUIT, SP680A	150656
R1	RESISTOR, COMP, 510Ω 1/4W ±5%	151476
R2	1.5K, 1/4W, ±5%	151487
R3,6,7,10,13	1K, 1/4 W, ±5%	151483
R4,8	680Ω, 2W, ±5%	151887
R5,9	RESISTOR, COMP, 3K, 1/4W, ±5%	151494
Q2,4	TRANSISTOR, 2N3568	150730
Q3,5	TRANSISTOR, 2N4240	150743
Q1	TRANSISTOR, 2N3440	150744
	SCREW, BIND. HD, 6-32 X 5/16 LG	110080
	NUT, KEP 6-32	110841
	TAG, ENGINEERING CHANGE	200304





001681

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350
3. Q1 HEIGHT NOT TO EXCEED .310

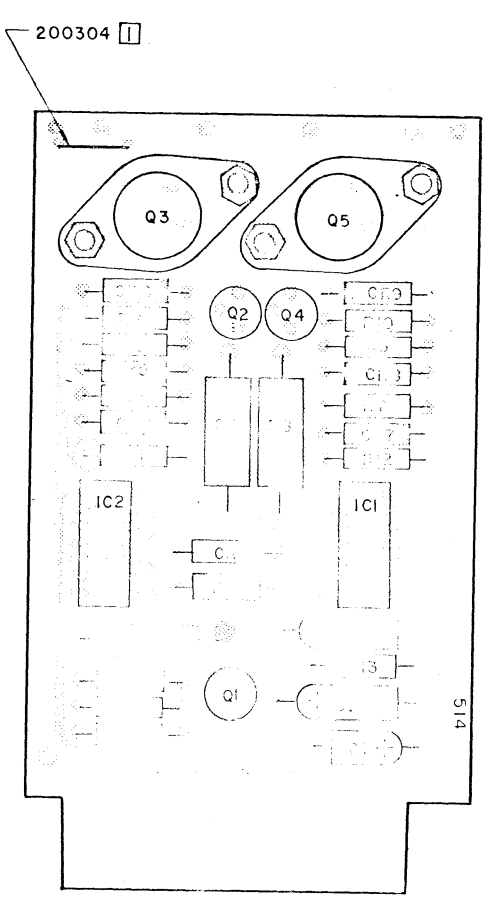
REFERENCE DOCUMENTS		E.C. LEVEL
SCH. DIAG.	001682	514
ARTMASTER	001683	514
FABRICATION	001684	514
TEST SPEC.		

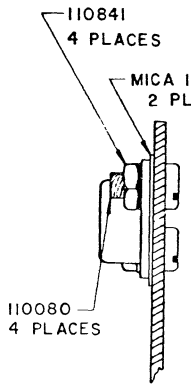
MATERIAL SEE B/M NO 001681	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION
CASE DEPTH		3 PLACE DEC ±	NAME PC BOARD ASSEMBLY
HARDNESS		ANGLES ±	ACTUATOR LOGIC & DRIVER II
SURFACE TREATMENT	CORNERS AND OR EDGES BROKEN	OUTSIDE MAX	DESIGN TYPE
001681 C		INSIDE MAX	DETAIL SCALE 2/1
	RADII UNLESS OTHERWISE NOTED		CHK'K HCL 10 31 68 DRAW 11-2 70
			APPRO KEP 11-1-68 WAW 11-1-68 ICHECK -5-70

001681

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490-60	10-20-68	215		
200495-50	12-10-68	218		
	1-2-70	514		

REF DESIG	DESCRIPTION	M. E. G. PART NO.
———	PRINTED CIRCUIT BOARD	001684
C1	CAPACITOR, T, 4.7UF, 20V, ±10%	151124
C2	" T, 3.3UF, 35V, ± 20%	151152
C3	" T, 15UF, 20V, ± 10%	151134
C4	CAPACITOR, T, 10UF 6V, ±10%	151143
CR1,2,4,5,7,8	DIODE, IN4148	150834
CR3,6,9	DIODE, TS-2	150826
IC1,2	INTEGRATED CIRCUIT, SP650A	150656
R1	RESISTOR, COMP, 510Ω, 1/4W, ±5%	151476
R2	" 1.5K, 1/4W, ±5%	151487
R3,6,7,10,13	" 1K, 1/4W, ±5%	151483
R4,8	" 680Ω, 2W, ±5%	151887
R5,9	RESISTOR, COMP, 3K, 1/4W, ±5%	151494
Q2,4	TRANSISTOR, 2N3546	150730
Q3,5	TRANSISTOR, 2N4240	150743
Q1	TRANSISTOR, 2N3440	150744
	SCREW, BIND, HD, 6-32 X 5/16 LG	110080
	NUT, KEP 6-32	110841
	TAG, ENGINEERING CHANGE	200304





001681

NOTES: UNLESS OTHERWISE SPECIFIED

[1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER

2. COMPONENT HEIGHT NOT TO EXCEED .350

REFERENCE DOCUMENTS		E.C. LEVEL
SCH. DIAG.	001682	514
ARTMASTER	001683	514
FABRICATION	001684	514
TEST SPEC.		

MATERIAL SEE B/M | DWG NO 001681

FINISH

NEXT ASSY

USED ON

001681 | C

TOLERANCE UNLESS OTHERWISE NOTED: DECIMALS ± PLACE DEC ± PLACE DEC ± ANGLES ±

CORNERS AND/OR EDGES BROKEN SHARP UNLESS OTHERWISE SPECIFIED

OUTSIDE MAX

INSIDE MAX

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME PC. BOARD ASSEMBLY
ACTUATOR LOGIC & DRIVER II

DESIGN | TYPE

DETAIL | SCALE 2/1

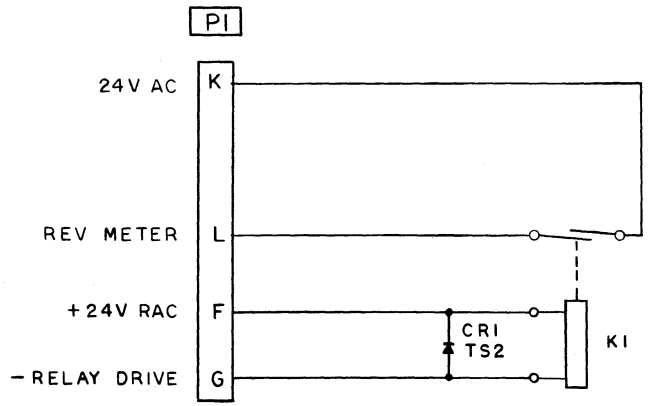
CHECK M.C.L. 10-31-68 | DRAW

APPRO KEF 11-1-68 | CHECK

001681

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001571	8MAY'68	88		
	10JUL'68	133		

001572



001572

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM
CASE DEPTH			ANGLES ±		METER RELAY
HARDNESS				DESIGN	TYPE
SURFACE TREATMENT		CORNERS AND OR EDGES BROKEN	OUTSIDE MAX	DETAIL	SCALE NONE
001572	C		INSIDE MAX	CHECK	DRAW
		RADII UNLESS OTHERWISE NOTED		APPR	CHECK

001572

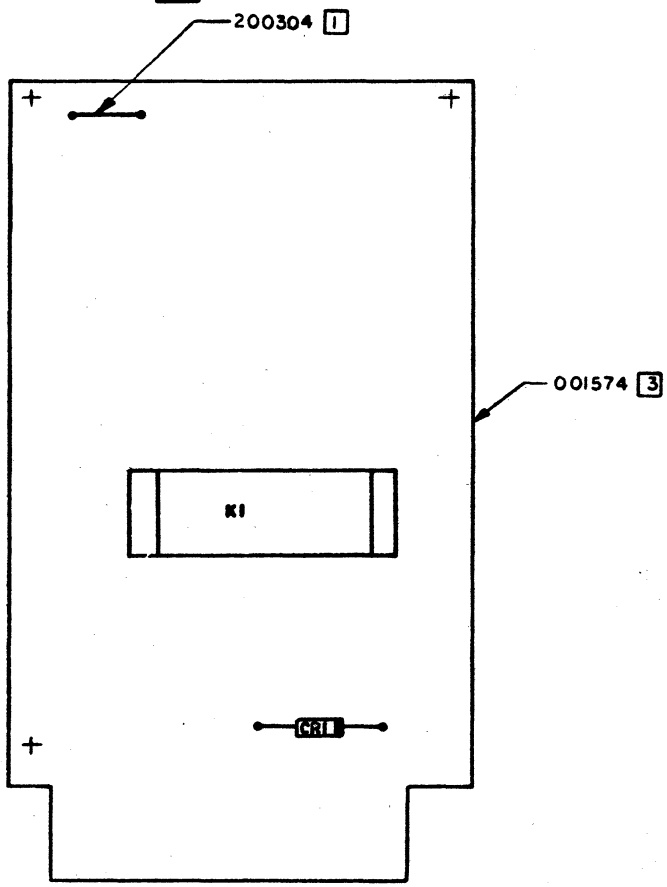
DATE	CHANGE NO	DATE	CHANGE NO
MAY 68	88	NOV. 70	1585
JUNE 68	133		
11-19-68	219		
1-2-70	580		

001571

RELEASED FOR ASSEMBLY
200490-60~
200495-50~

REF DESIG	DESCRIPTION	M. E. G. PART NO.
CR1	DIODE, TS2	50826
K1	RELAY, REED, 3PNO-24VAC	005076
—	TAG, ENGINEERING CHANGE	200304

001571



001571

REFERENCE DOCUMENTS		E.C. LEVEL
SCH. DIAG.	001572	133
ARTMASTER	001574	580

NOTES:

[1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER.

2. COMPONENT HEIGHT NOT TO EXCEED .400.

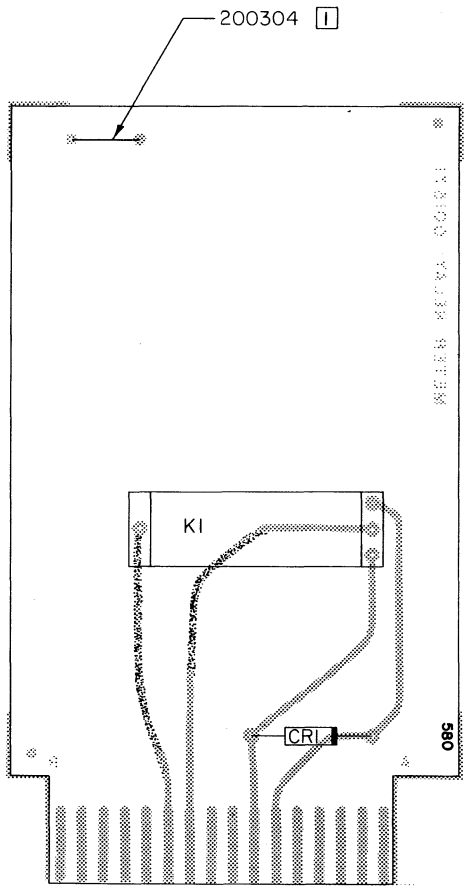
[3] P.C. BOARD 001574 MUST BE AT EC LEVEL 580.

001571

MATERIAL NO. SEE B/M NO. 001571	MUST CONFORM TO ENG. SPEC 88000L	TOLERANCE UNLESS OTHERWISE NOTED	MEMOREX EQUIPMENT GROUP
CASE DEPTH	TECHNICAL APPROVAL	LINEAR ± .XX / .XXX	NAME P.C. BOARD ASSEMBLY METER RELAY
HARDNESS		ANGULAR ±	DESIGN SCALE 2/1
SURFACE TREATMENT		CORNERS/EDGES BROKEN	DETAIL TRG 11/5/70
STD CODE C		OUTSIDE MAX	CHECK 11/5/70
		INSIDE MAX	APPRO TRG 11/7/70 001571

REF DESIG	DESCRIPTION	P.S.C. PART NO.
——	PRINTED CIRCUIT BOARD	C01574
CR1	DIODE, TS2	150826
K1	RELAY, REED, S.P.N.O., 24VAC	005076
——	TAG, ENGINEERING CHANGE	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490-60~	8MAY68	88		
200495-50~	10JUL'68	133		
	11-19-68	219		
	1-2-70	580		



REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001572	133
ARTMASTER	001573	580
FABRICATION	001574	580

NOTES: UNLESS OTHERWISE SPECIFIED

[1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER

2 COMPONENT HEIGHT NOT TO EXCEED .750

3. CIRCUITRY SHOWN FARSIDE

SEE B/M 001571

001571 C

Peripheral Systems Corporation

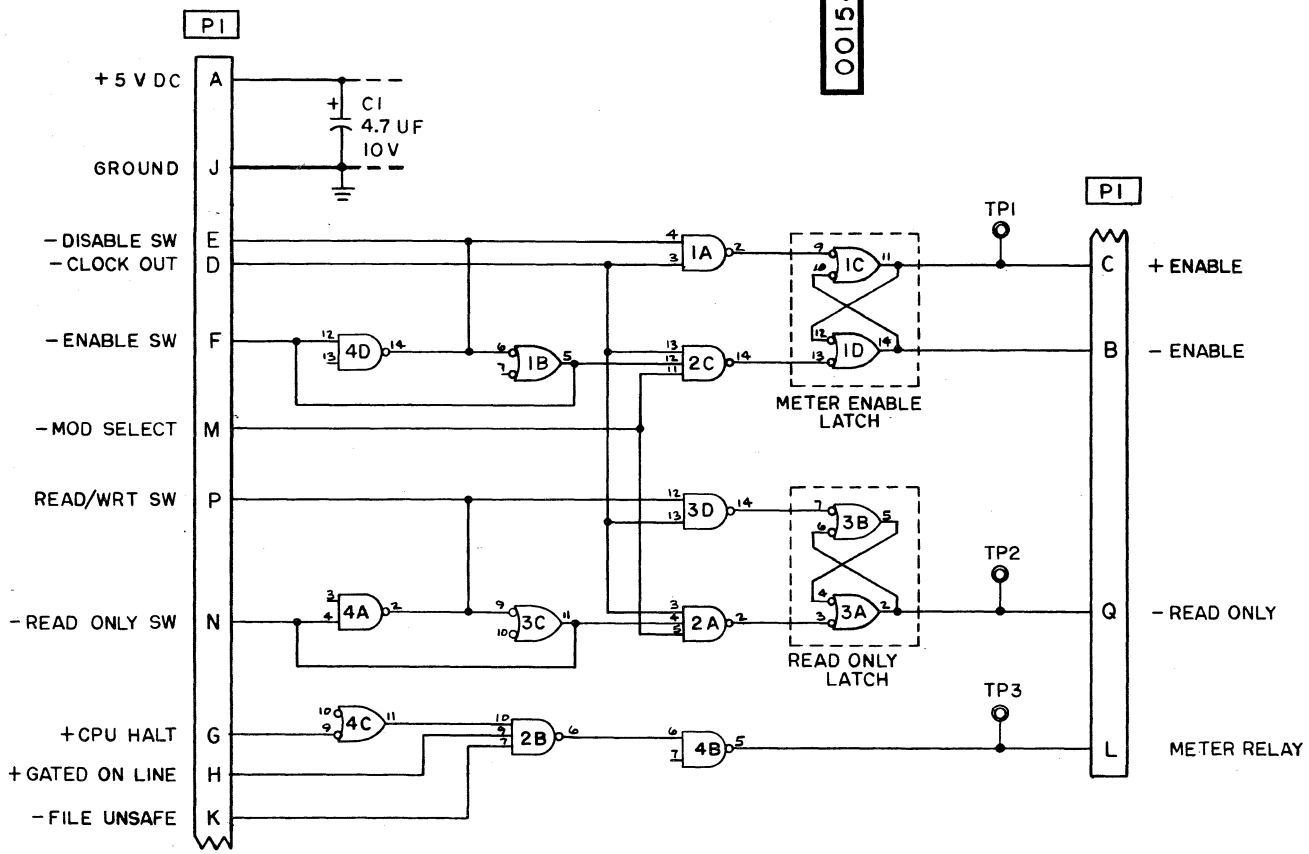
ASSEMBLY DRAWING

METER RELAY

DRAWN	Esu	5/7/68	TYPE	
ENGR			SCALE	2/1
MFG	Esu	5/7/68	DRAW	K.B. 8MAY68
APPR		7/7/68	CHECK	KDE 8may68

001571

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001541	1MAY68	79		
	6-11-68	127		



001542

NOTES: UNLESS OTHERWISE SPECIFIED -

1. IC1, 3 AND 4 ARE SP680A
2. IC2 IS SP670A
3. CONNECT PIN 1 OF ALL I/C'S TO GROUND
4. CONNECT PIN 8 OF ALL I/C'S TO +5VDC

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM
CASE DEPTH			ANGLES ±	RD/WRT-ENABLE SYNC	
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN	TYPE
SURFACE TREATMENT			INSIDE MAX	DETAIL	SCALE NONE
001542	C	RADII UNLESS OTHERWISE NOTED		CHECK K.R.F. 5/1/68	DRAW R.D.S. 1MAY68
				APPRO K.R.F. 5/7/68	CHECK R.D.S. 6-11-68

001542

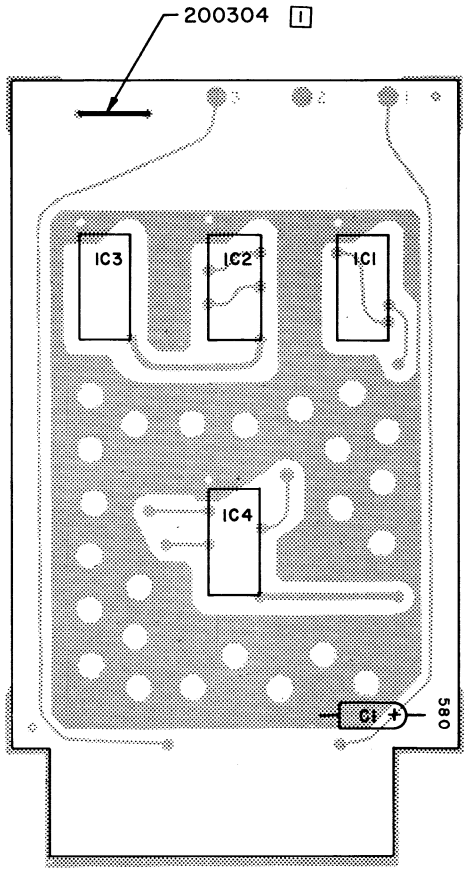
001541

REF DESIG	DESCRIPTION	P.S.C. PART NO.
——	PRINTED CIRCUIT BOARD	C01544
C1	CAPACITOR, 4.7UF, 10V ±10%	151124
IC1,3,4	INTEG CIRCUIT, SP680A	150656
IC2	INTEG. CIRCUIT, SP670A	150655
——	TAG, ENGINEERING CHANGE	200304

001541

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490-60~	5-3-68	79		
200495-50~	6-11-68	127		
	11-19-68	219		
	1-2-70	580		

001541



001541

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001542	127
ARTMASTER	001543	580
FABRICATION	001544	580

NOTES: UNLESS OTHERWISE SPECIFIED

[1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER

2 COMPONENT HEIGHT NOT TO EXCEED .350

001541

SEE B/M 001541

001541 C

Peripheral Systems Corporation

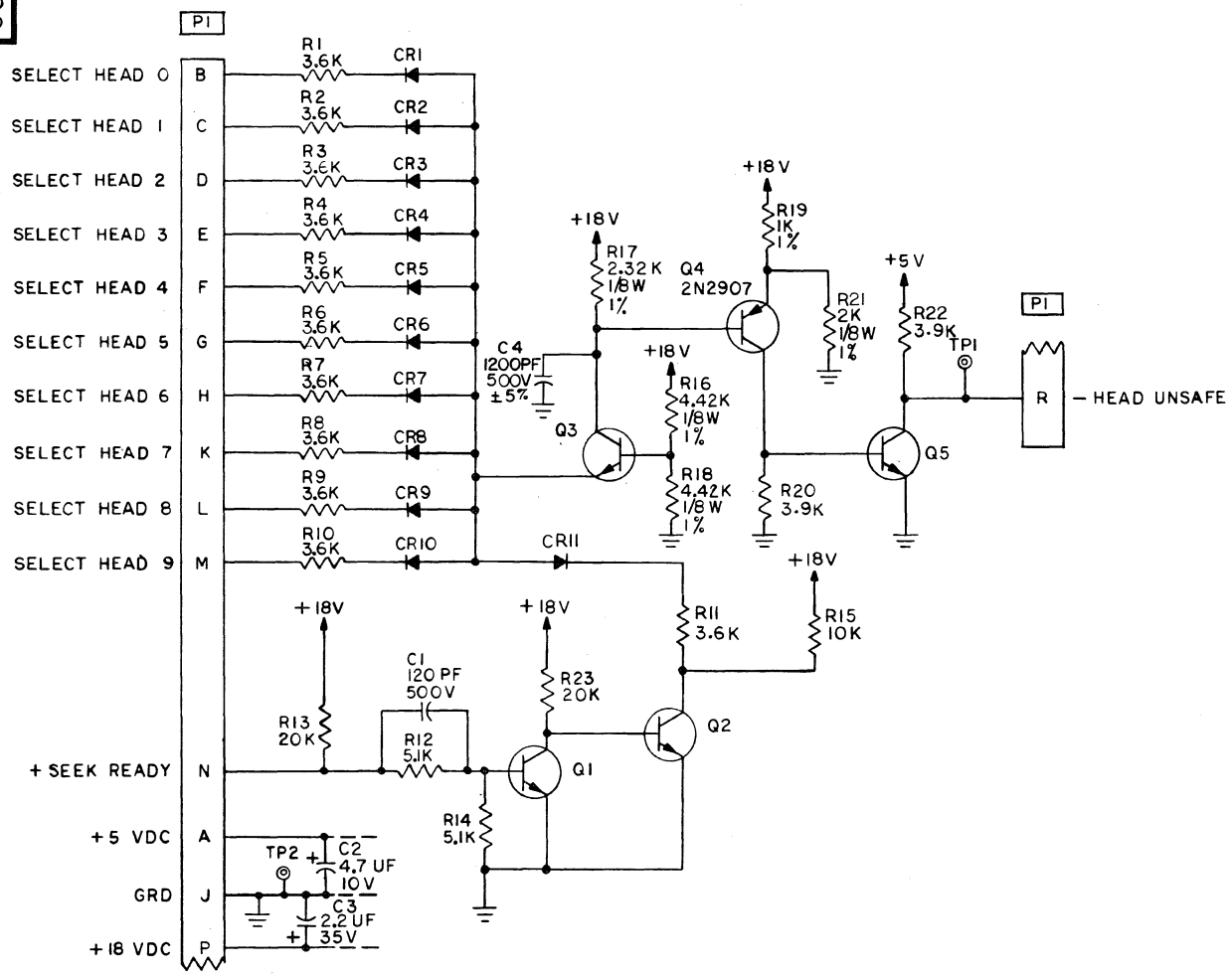
P.C. BOARD ASSEMBLY

READ/WRITE ENABLE SYNC

DRAWN	MCL	6/14/68	TYPE	
TRACED			SCALE	2/1
CHECKED	MCL	6/14/68	PROJ.	K.B. 6-11-68
APPROVED	[illegible]	[illegible]	MFG.	P.O.S. 13 Jun 68

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001726	10-30-68	225		
	11/8/69	536		
	MAY 6,70	1004		

001727



001727

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1/4 W, 5%.
2. ALL DIODES ARE IN4148.
3. ALL TRANSISTORS ARE 2N2222A.

MATERIAL	NO
CASE DEPTH	
HARDNESS	
SURFACE TREATMENT	

001727 C

TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	
	3 PLACE DEC ±	
	ANGLES ±	
CORNERS AND/OR EDGES BROKEN	OUTSIDE	MAX
	INSIDE	MAX
RADII UNLESS OTHERWISE NOTED		

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

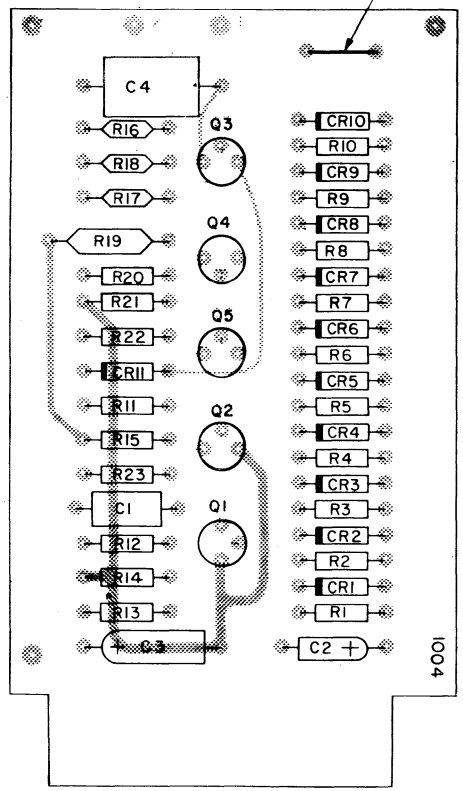
NAME	SCHEMATIC DIAGRAM				
	HEADS SAFETY III				
DESIGN			TYPE		
DETAIL			SCALE	NONE	
CHECK	04/21/68	A.C.L.	DRAW	M.H.	10-30-68
APPRO	K.L.P.	11/68	CHECK	DFH	10-30-68

001727

REF DESIG	DESCRIPTION	M. E. G. PART NO.
———	PRINTED CIRCUIT BOARD	001729
C1	CAPACITOR P, 120PF, 500V, ±5%	151224
C2	CAPACITOR T, 4.7UF, 10V, ±10%	151124
C3	CAPACITOR T, 2.2UF, 35V, ±10%	151127
C4	CAPACITOR P, 1200PF, 500V, ±5%	151248
CR1-11	DIODES, IN4148	150834
R1-11	RESISTOR, 3.6K, 1/4W, ±5%	151496
R12,14	RESISTOR, 5.1K, 1/4W, ±5%	151500
R13,23	RESISTOR, 20K, 1/4W, ±5%	151514
R15	RESISTOR, 10K, 1/4W, ±5%	151507
R16,18	RESISTOR, 9.42K, 1/8W, ±1%	153217
R17	RESISTOR, 2.32K, 1/8W, ±1%	153046
R19	RESISTOR, 1K, 1/4W, ±1%	152066
R21	RESISTOR, 2K, 1/8W, ±1%	153090
R20,22	RESISTOR, 3.9K, 1/4W, ±5%	151497
Q1,2,3,5	TRANSISTOR, 2N2222A	150768
Q4	TRANSISTOR, 2N2907	150765
	TAG, ENGINEERING CHANGE	200304

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
630A	200490	9/6/68	225		
630B	200495	11/8/69	536		
	MULTI-USE	MAY 6,70	1004		

200304 [1]



001726

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001727	1004
ARTMASTER	001728	1004
FABRICATION	001729	1004

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

001726

MATERIAL SEE B/M NO 001726	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
		3 PLACE DEC ±
CASE DEPTH		ANGLES ±
HARDNESS	CORNERS AND OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT		INSIDE MAX
001726 C	RADII UNLESS OTHERWISE NOTED	

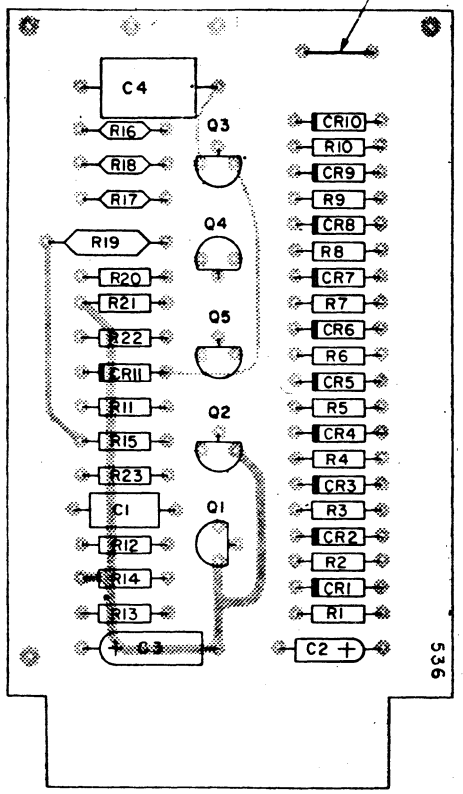
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	P.C. BOARD ASSEMBLY				
	HEADS SAFETY III				
DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK	MC		DRAW		10-30-69
APPRO			CHECK		10-30-69

REF DESIG	DESCRIPTION	M. E. G. PART NO.
———	PRINTED CIRCUIT BOARD	001729
C1	CAPACITOR P, 120PF, 500V, ±5%	151224
C2	CAPACITOR T, 4.7UF, 10V, ±10%	151129
C3	CAPACITOR T, 2.2UF, 35V, ±10%	151127
C4	CAPACITOR P, 1200PF, 500V, ±5%	151248
CR1-11	DIODES, IN4148	150834
R1-11	RESISTOR, 3.6K, 1/4W, ±5%	151496
R12,14	RESISTOR, 5.1K, 1/4W, ±5%	151500
R13,23	RESISTOR, 20K, 1/4W, ±5%	151514
R15	RESISTOR, 10K, 1/4W, ±5%	151507
R16,18	RESISTOR, 4.42K, 1/8W, ±1%	153217
R17	RESISTOR, 2.32K, 1/8W, ±1%	153046
R19	RESISTOR, 1K, 1/4W, ±1%	152066
R21	RESISTOR, 2K, 1/8W, ±1%	153090
R20,22	RESISTOR, 3.9K, 1/4W, ±5%	151497
Q1,2,3,5	TRANSISTOR, 2N3904	150735
Q4	TRANSISTOR, 2N3906	150736
	TAG, ENGINEERING CHANGE	200304

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
630A	200490	11/1/78	225		
630B	200495	11/8/79	536		
630-IKIT	200762				
620	202032				

200304 [1]



001726

REFERENCE DOCUMENTS		EC LEVEL
SCH DIAG	001727	536
ARTMASTER	001728	536
FABRICATION	001729	536

NOTES: UNLESS OTHERWISE SPECIFIED

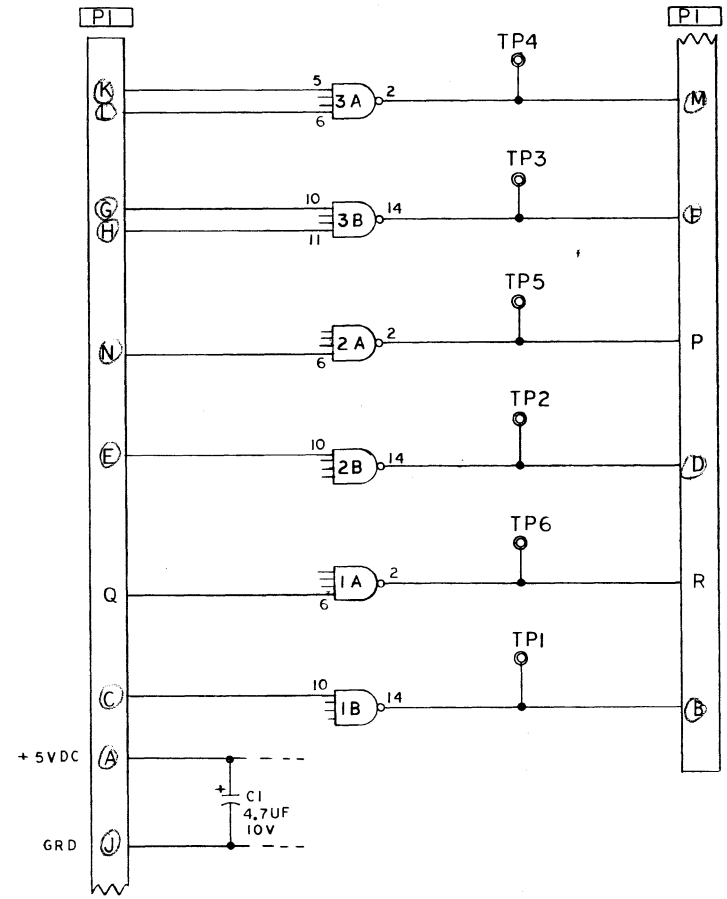
1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

001726

MATERIAL SEE B/M 001726	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation, a subsidiary of MEMOREX CORPORATION
		3 PLACE DEC ±	NAME P.C. BOARD ASSEMBLY
CASE DEPTH		ANGLES ±	HEADS SAFETY III
HARDNESS	CORNERS AND OR EDGES BROKEN	OUTSIDE MAX	DESIGN — TYPE
SURFACE TREATMENT		INSIDE MAX	DETAIL — SCALE 2/1
001726 C	RADII UNLESS OTHERWISE NOTED		CHECK MCC — DRAW
			APPRO — CHECK

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001206	3/13/68	14		
	3/21/68	34		

001207



001207

NOTES: UNLESS OTHERWISE SPECIFIED
1. CONNECT PIN 1 OF ALL IC'S TO GRD
2. CONNECT PIN 8 OF ALL IC'S TO +5VDC
3. IC1, 2 AND 3 ARE SP659A

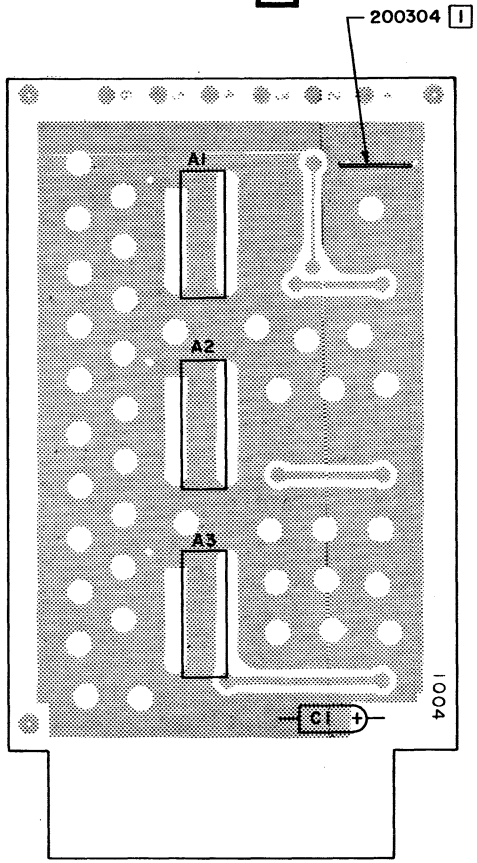
MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION
			3 PLACE DEC ±	NAME SCHEMATIC DIAGRAM DRIVERS (6)
CASE DEPTH			ANGLES ±	DESIGN — TYPE
HARDNESS			CORNERS AND/OR EDGES BROKEN	DETAIL — SCALE NONE
SURFACE TREATMENT			OUTSIDE MAX	CHECK 3/13/68 DRAW EGG 12/15/67
001207	C		INSIDE MAX	APPRO CHECK R.J.E.
			RADII UNLESS OTHERWISE NOTED	

001207

001206

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
630 A	200490-60 ~	3-13-68	14	MAY 6,70	1004
630 B	200495-50 ~	3-21-68	34		
	MULTI-USE	7-17-68	158		
		11-18-68	219		
		11-18-69	540		

REF DESIG	DESCRIPTION	P. S. C. PART NO.
—	PRINTED CIRCUIT BOARD	001209
C1	CAPACITOR, T, 4.7UF, 10V ± 10%	151124
IC1, IC2, IC3	INTEGRATED CIRCUIT, SP659A	150654
—	TAG, ENG. CHANGE	200304



001206

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001207	34
ARTMASTER	001208	1004
FABRICATION	001209	1004

NOTES: UNLESS OTHERWISE SPECIFIED

[1.] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER

2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M	NO 001206
CASE DEPTH	
HARDNESS	
SURFACE TREATMENT	
001206	C

TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	
	3 PLACE DEC ±	
	ANGLES ±	
CORNERS AND/OR EDGES BROKEN	OUTSIDE	MAX
	INSIDE	MAX
RADII UNLESS OTHERWISE NOTED		

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

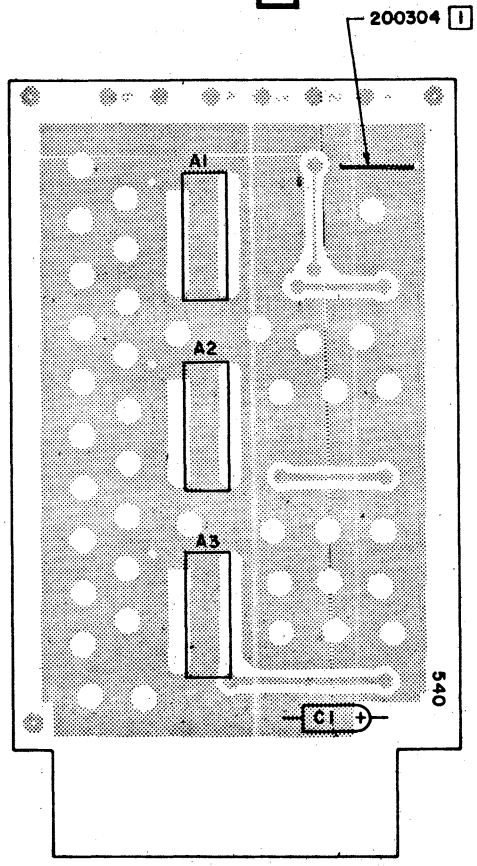
NAME	P.C. BOARD ASSEMBLY DRIVERS (6)			
DESIGN			TYPE	
DETAIL			SCALE	2/1
CHECK	JDX	3 MAR 68	DRAW	TCM 1-22-68
APPRO	JDX JPW	3 MAR 68 3-27-68	CHECK	1-24-68

001206

001206

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
630 A	200490-60 ~	3-13-68	14		
630B	200495-50 ~	3-21-68	34		
630-1	200762	7-17-68	158		
620	202032	11-18-68	219		
		11-18-68	540		

REF DESIG	DESCRIPTION	P. S. C. PART NO.
—	PRINTED CIRCUIT BOARD	001209
C1	CAPACITOR, T, 4.7UF, 10V ± 10%	151124
IC1, IC2, IC3	INTEGRATED CIRCUIT, SP659A	150654
—	TAG, ENG. CHANGE	200304



001206

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001207	34
ARTMASTER	001208	540
FABRICATION	001209	540

NOTES: UNLESS OTHERWISE SPECIFIED

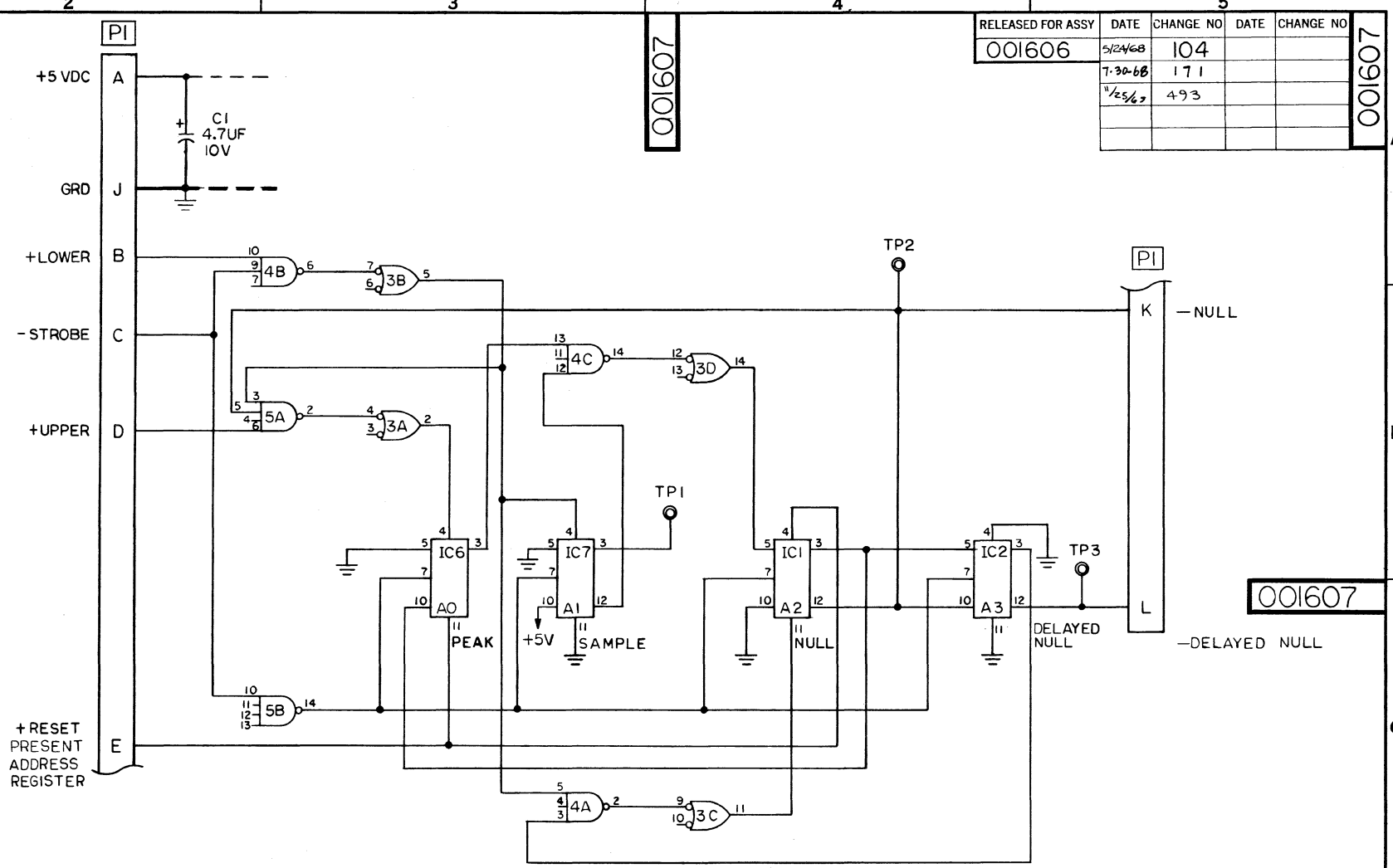
1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M	NO 001206	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001206	C	RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	P.C. BOARD ASSEMBLY DRIVERS (6)				
DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK	DX	3 MAR 68	DRAW	TCM	1-22-68
APPRO	DX MJ	3 MAR 68 3-27-68	CHECK	RPE	1-24-68

001206



RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001606	5/24/68	104		
	7-30-68	171		
	11/25/68	493		

001607

NOTES: UNLESS OTHERWISE SPECIFIED
1. IC'S 1,2,6 & 7 ARE SP620A
2. IC3 IS SP680A
3. IC4 IS SP670A
4. IC5 IS SP659A
5. CONNECT ALL IC PINS 1 TO GRD, PINS 8 TO +5V

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001607	C	RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME: SCHEMATIC DIAGRAM
NULL DETECTOR

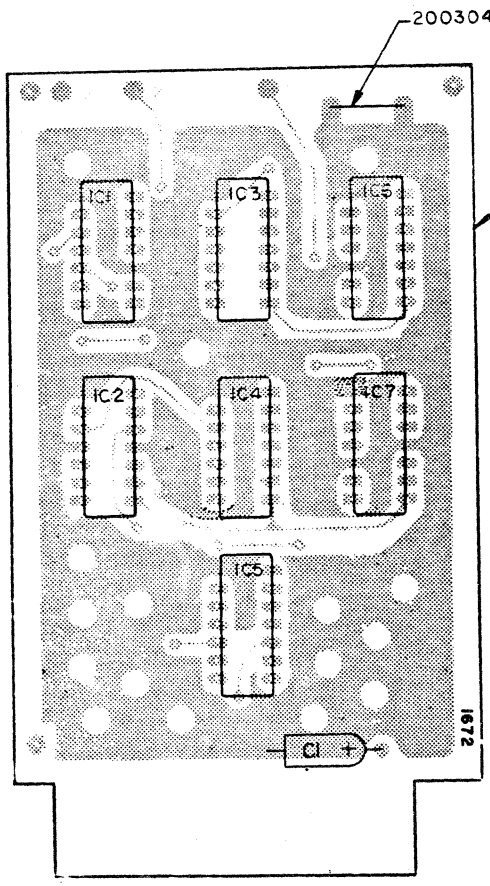
DESIGN			TYPE		
DETAIL			SCALE	NONE	
CHECK	M.C.L.	6/10/68	DRAW	K.B.	5-24-68
APPRO	K.E. Gow	6/10/68	CHECK	R.E.	27 MAY 68

001607

REF DESIG	DESCRIPTION	M. E. G. PART NO.
C1	CAPACITOR 4.7 UF C1 ± 0%	511124
IC2,6,7	INTEGRATED CIRCUIT SP620A	150651
IC3	INTEGRATED CIRCUIT SP630A	500556
IC4	INTEGRATED CIRCUIT SP670A	150655
IC5	INTERATED CIRCUIT SP655A	150654
——	TAG ENGINEERING CHANGE	200304

USED ON	RELEASED FOR ASSY
630A	200490-60
630B	200495-50
	MULTI-USE

DATE	CHANGE NO	DATE	CHANGE NO
1/8/68	104	DEC. '70	1672
7/30/68	171		
11/19/68	219		
11/25/69	493		
MAY 6, 70	1004		



001606

NOTES:
1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350
3. PC BOARD 001609 MUST BE AT E.C LEVEL 1672

REFERENCE DOCUMENTS		E.C LEVEL
SCH. DIAG.	001607	J03
ARTMASTER	001608	1672

MATERIAL SEE B/M NO 001606
CASE DEPTH
HARDNESS
SURFACE TREATMENT
001606 C

TOLERANCE UNLESS OTHERWISE NOTED
FRACTIONS
DECIMALS
ANGLES
BREAK SHARP EDGES
RADII UNLESS OTHERWISE NOTED

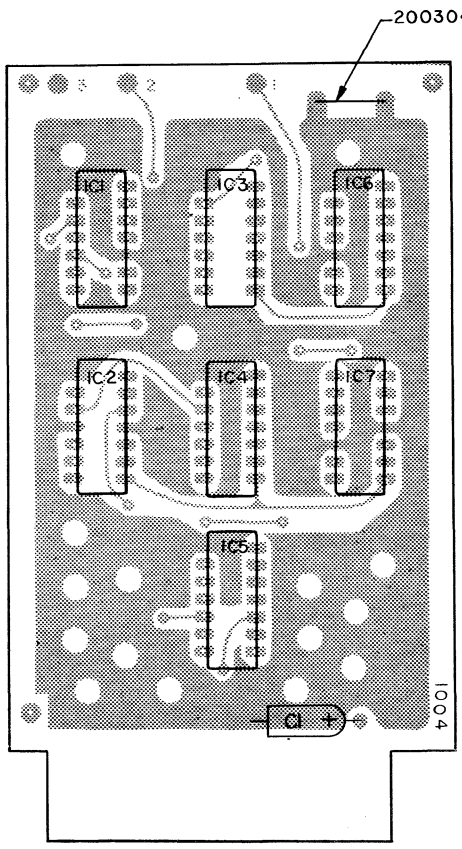
Peripheral Systems Corporation
A SUBSIDIARY OF MEMOREX CORPORATION
NAME PC BOARD ASSEMBLY
NULL DETECTOR
DESIGN TYPE
DETAIL SIZE 2/1
CHK MCL 6-10-68 PAW DA 12-15-69
APPR WGW 6-12-68 REV RJE 6-10-68

001606

001606

REF DESIG	DESCRIPTION	M. E. G. PART NO.
——	PRINTED CIRCUIT BOARD	001609
C1	CAPACITOR, 4.7 UF, 10V, ±10%	151124
IC1,2,6,7	INTEGRATED CIRCUIT, SP620A	150651
IC3	INTEGRATED CIRCUIT, SP680A	150656
IC4	INTEGRATED CIRCUIT, SP670A	150655
IC5	INTERATED CIRCUIT, SP659A	150654
——	TAG, ENGINEERING CHANGE	200304

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
630A	200490-60	6/8/68	104		
630B	200495-50	7/30/68	171		
	MULTI-USE	11/19/68	219		
		11/25/69	493		
		MAY 6, 70	1004		



001606

NOTES: UNLESS OTHERWISE SPECIFIED

[1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER

2. COMPONENT HEIGHT NOT TO EXCEED .350

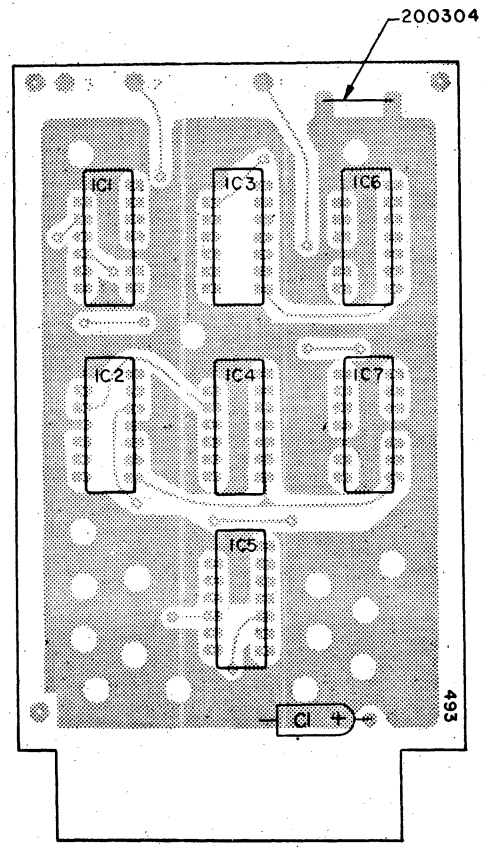
REFERENCE DOCUMENTS		E.C. LEVEL
SCH. DIAG.	001607	493
ARTMASTER	001608	1004
FABRICATION	001609	1004
TEST SPEC.	——	——

MATERIAL SEE B/M NO. 001606		TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
CASE DEPTH			3 PLACE DEC ±	NAME	P.C. BOARD ASSEMBLY
HARDNESS			ANGLES ±		NULL DETECTOR
SURFACE TREATMENT		CORNERS AND OR EDGES BROKEN	OUTSIDE MAX	DESIGN	TYPE
001606	C		INSIDE MAX	DETAIL	SCALE 2/1
		RADII UNLESS OTHERWISE NOTED		CHECK M.C.L. 6-10-68	DRAW D.A. 12-18-69
				APPRO K.R.F. W.G.Y. 6-10-68 6-12-68	CHECK R.J.E. 6 10 68

001606

REF DESIG	DESCRIPTION	M. E. G. PART NO.
——	PRINTED CIRCUIT BOARD	001609
C1	CAPACITOR, 4.7 UF, 10V, ±10%	151124
IC1,2,6,7	INTEGRATED CIRCUIT, SP620A	150651
IC3	INTEGRATED CIRCUIT, SP680A	150656
IC4	INTEGRATED CIRCUIT, SP670A	150655
IC5	INTERATED CIRCUIT, SP659A	150654
——	TAG, ENGINEERING CHANGE	200304

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
630A	200490-60	5/8/68	104		
630B	200495-50	7/30/68	171		
620	202032	11/19/68	219		
		11/25/69	493		



001606

NOTES: UNLESS OTHERWISE SPECIFIED
1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

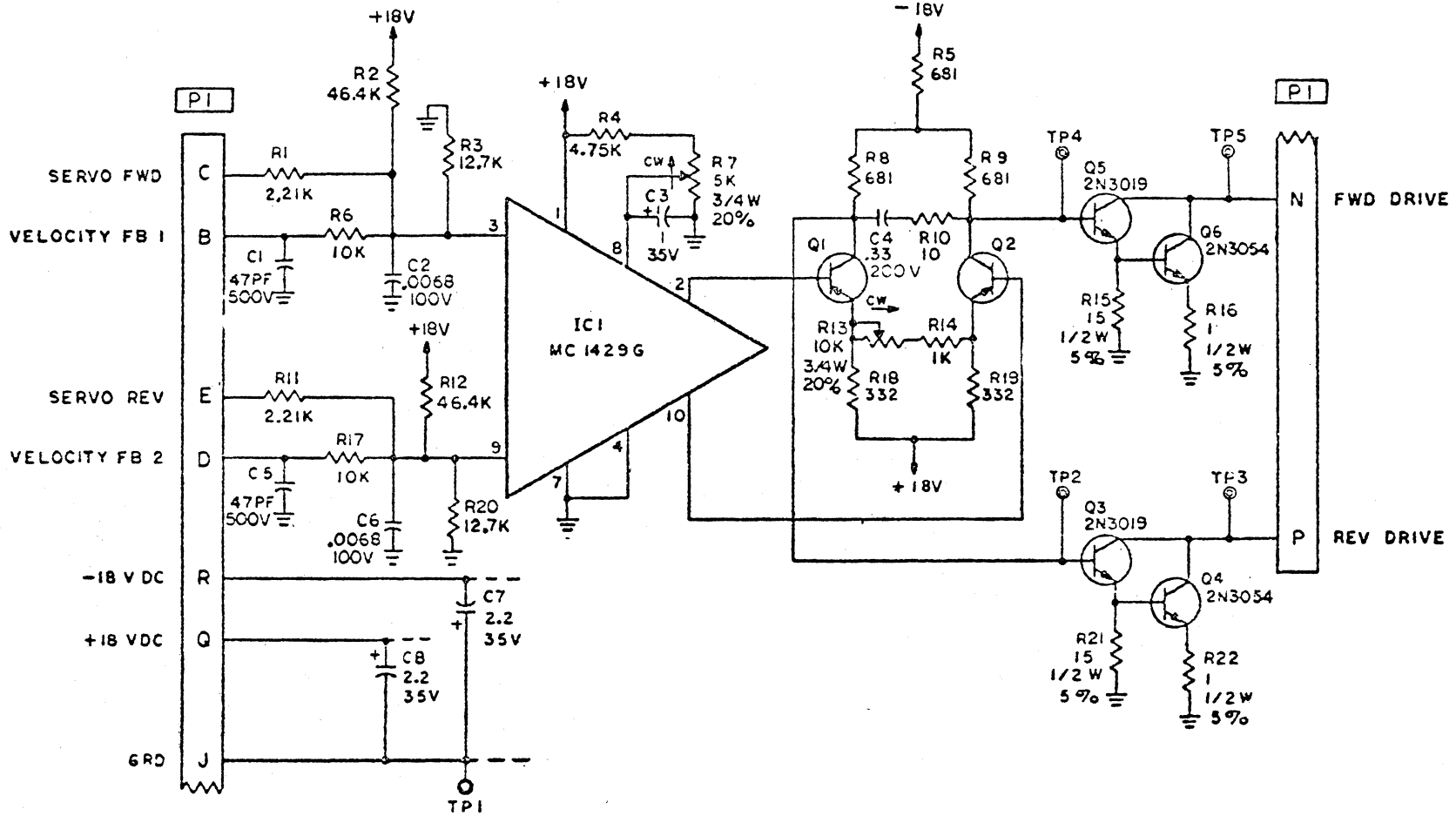
REFERENCE DOCUMENTS		E.C. LEVEL
SCH. DIAG.	001607	493
ARTMASTER	001608	493
FABRICATION	001609	493
TEST SPEC.	——	——

MATERIAL SEE B/M NO. 001606	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation subsidiary of MEMOREX CORPORATION
		3 PLACE DEC ±	NAME P.C. BOARD ASSEMBLY
CASE DEPTH		ANGLES ±	NULL DETECTOR
HARDNESS		OUTSIDE MAX	DESIGN TYPE
SURFACE TREATMENT	CORNERS AND OR EDGES BROKEN	INSIDE MAX	DETAIL SCALE 2/1
001606 C	RADII UNLESS OTHERWISE NOTED		CHECK M.C.L. 6-10-68 DRAW D.A. 12-18-69
			APPRO. K.R.W. W.G.W. 6-10-68 6-12-68 CHECK R.J.E. 6-10-68

001606

001427

RELEASED FOR	DATE	CHANGE NO	DATE	CHANGE NO
001426	2-14-68	14	12-30-70	1265
	3-21-68	34		
	6-19-68	126		
	8-29-68	442		
	9-4-68	509		



001427

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1/8W, ± 1%
2. ALL CAPACITORS ARE IN MICROFARADS
3. Q1 AND Q2 ARE 2N2907A.

MATERIAL	NO
CASE DEPTH	
HARDNESS	
SURFACE TREATMENT	

001427 C

TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	
	3 PLACE DEC ±	
	ANGLES ±	
CORNERS AND/OR EDGES BROKEN	OUTSIDE	MAX
	INSIDE	MAX
RADII UNLESS OTHERWISE NOTED		

Peripheral Systems Corporation
A SUBSIDIARY OF MEMOREX CORPORATION

NAME SCHEMATIC DIAGRAM
SERVO AMPLIFIER

DESIGN	JDM	3/21/68	TYPE	
DETAIL			SCALE	NONE
CHECK			DRAW	2-3-68
APPRO			CHECK	

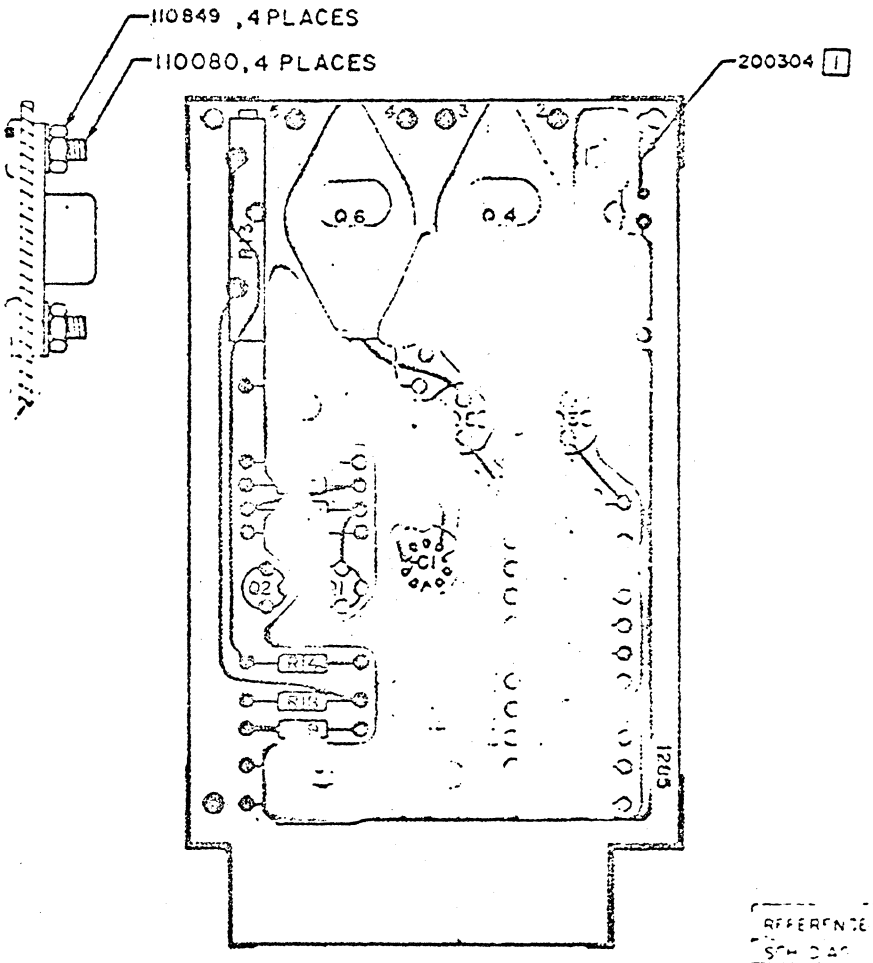
001427

2 3 4 5

001426

REF DES	DESCRIPTION	M E G PART NO
— —	PRINTED CIRCUIT BOARD	001429
C1, 5	CAPACITOR P, 47PF, 500V, ± 10%	151215
C2, 6	" M, .0068UF, 100V, ± 10%	151061
C3	" T, 1UF, 35V, ± 10%	151116
C4	" M, .33UF, 200V, ± 5%	151200
C7, 8	CAPACITOR T, 2.2UF, 35V, ± 10%	151127
IC1	INTEG CIRCUIT, MC1429G	150660
Q1, 2	TRANSISTOR, 2N2907A	150771
Q3, 5	TRANSISTOR, 2N3019	150796
Q4, 6	TRANSISTOR, 2N3054	150739
R7	POTENTIOMETER, 5K, 3/4W, ± 20%	153408
R13	POTENTIOMETER, 10K, 3/4W, ± 20%	153409
R1, 11	RESISTOR, MF, 2.21K, 1/8W, ± 1%	153044
R2, 12	" MF, 46.4K, 1/8W, ± 1%	153267
R3, 20	" MF, 12.7K, 1/8W, ± 1%	153069
R4	" MF, 4.75K, 1/8W, ± 1%	153220
R5, 8, 9	" MF, 681 OHM, 1/8W, ± 1%	153187
R6, 17	" MF, 10K, 1/8W, ± 1%	153059
R10	" MF, 10 OHM, 1/8W, ± 1%	152915
R14	" MF, 1K, 1/8W, ± 1%	153011
R15, 21	" COMP, 15 OHM, 1/2W, ± 5%	151583
R16, 22	" COMP, 1 OHM, 1/2W, ± 5%	152898
R18, 19	RESISTOR, MF, 332 OHM, 1/8W, ± 1%	153157
	SCREW, BINDER HD # 6-32 x 3/8 Lg	110080
	NUT, KEP # 6-32 (SMALL PATTERN)	110849
	TAG, ENGINEERING CHANGE	200304

630 A	200480-60	5 13 68	14	12 4 68	248
630 B	200495-50	5 21 68	34	1 8 68	2.9
620	202032	5 13 68	126	5 26 68	442
		7 12 68	144	10 3 68	503
		8 30 68	154	2 3 69	580
				4 1 69	1.46
				6 4 70	1285



001426

NOTES

1. ENGINEERING CHANGE TAG 200304 MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350
3. IC1, Q1 & Q2 HEIGHT NOT TO EXCEED .330.
4. Q3 & Q5 HEIGHT NOT TO EXCEED .310.
5. AFTER SOLDERING, TRIMMED LEAD HEIGHT NOT TO EXCEED .063.

REFERENCE DOCUMENTS		E C LEVEL
SCHEMATIC	001427	1285
ARTMASTER	001428	1285
FABRICATION	001429	1285
ENGRG SPEC	001430	1285

SEE B/M 001426

001426 C

PC BOARD ASSEMBLY
SERVO AMPLIFIER
jd
2/1

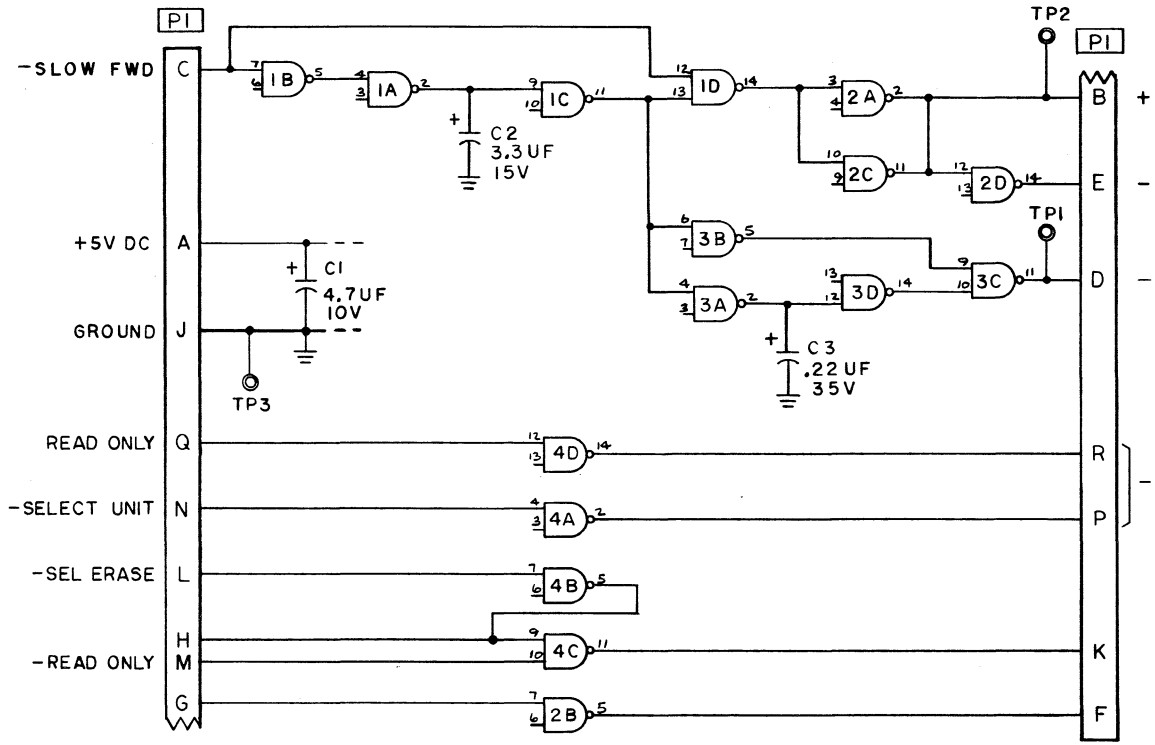
jdm 6 14 68 KB 6 13 68
RDE 6 14 68

001426

2 3 4 5

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001551	29 APR 68	88		

001552



001552

NOTES: UNLESS OTHERWISE SPECIFIED –

1. ALL I/C'S ARE SP680A
2. CONNECT PIN 1 OF ALL I/C'S TO GROUND
3. CONNECT PIN 8 OF ALL I/C'S TO +5V DC

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM
CASE DEPTH			ANGLES ±	FORCE SEEK COUNT	
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN	TYPE
SURFACE TREATMENT			INSIDE MAX	DETAIL	SCALE NONE
001552	C	RADII UNLESS OTHERWISE NOTED		CHECK H.C.L. 4-29-68	DRAW R.G.F. 29 APR 68
				APPRO [illegible] 4-30-68	CHECK R.S. 17 JUN 68

001551

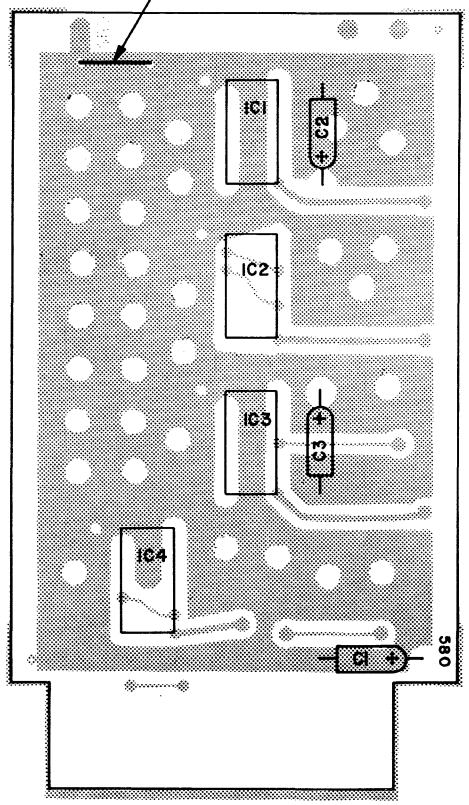
REF DESIG	DESCRIPTION	P.S.C. PART NO.
———	PRINTED CIRCUIT BOARD	001554
C1	CAPACITOR, 4.7UF, 10V ±10%	151124
C2	CAPACITOR, 3.3UF, 15V ±10%	151122
C3	CAPACITOR, .22UF, 35V ±10%	151098
IC1,2,3,4	INTEG CIRCUIT, SP680A	150656
	TAG, ENGINEERING CHANGE	200304

001551

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490-60~	6-17-68	88		
200495-50~	6/14/68	158		
	11-19-68	219		
	1-2-70	580		
	JUN,70	1146		

001551

200304 [1]



001551

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001552	88
ARTMASTER	001553	580
FABRICATION	001554	580

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350
3. AFTER SOLDERING TRIMMED LEAD HEIGHT NOT TO EXCEED .063

001551

SEE B/M 001551

001551 C

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME P.C. BOARD ASSEMBLY
FORCE SEEK COUNT

DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK	M.C.L.	6/14/68	DRAW	K.B.	6-17-68
APPRO	K.R.H.	6/19/68	CHECK	R.C.S.	17JUN68

001551

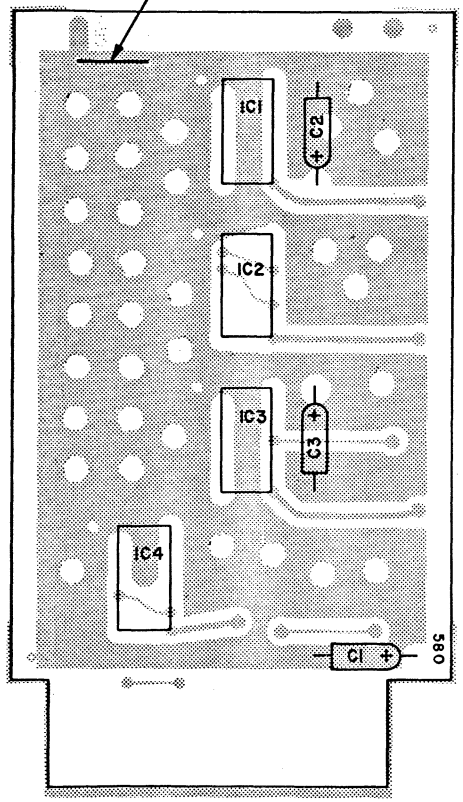
REF DESIG	DESCRIPTION	P.S.C. PART NO.
———	PRINTED CIRCUIT BOARD	001554
C1	CAPACITOR, 4.7UF, 10V ±10%	151124
C2	CAPACITOR, 3.3UF, 15V ±10%	151122
C3	CAPACITOR, .22UF, 35V ±10%	151098
IC1,2,3,4	INTEG CIRCUIT, SP680A	150656
	TAG, ENGINEERING CHANGE	200304

001551

RELEASED FOR ASSY	DATE	CHANGE NO	DATE,	CHANGE NO
200490-60~	6-17-68	88		
200495-50~	6/14/68	158		
	11-19-68	219		
	1-2-70	580		

001551

200304 [1]



001551

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001552	88
ARTMASTER	001553	580
FABRICATION	001554	580

NOTES: UNLESS OTHERWISE SPECIFIED

[1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER

2. COMPONENT HEIGHT NOT TO EXCEED .350

SEE B/M 001551

001551 C

Peripheral Systems Corporation
A SUBSIDIARY OF MEMOREX CORPORATION

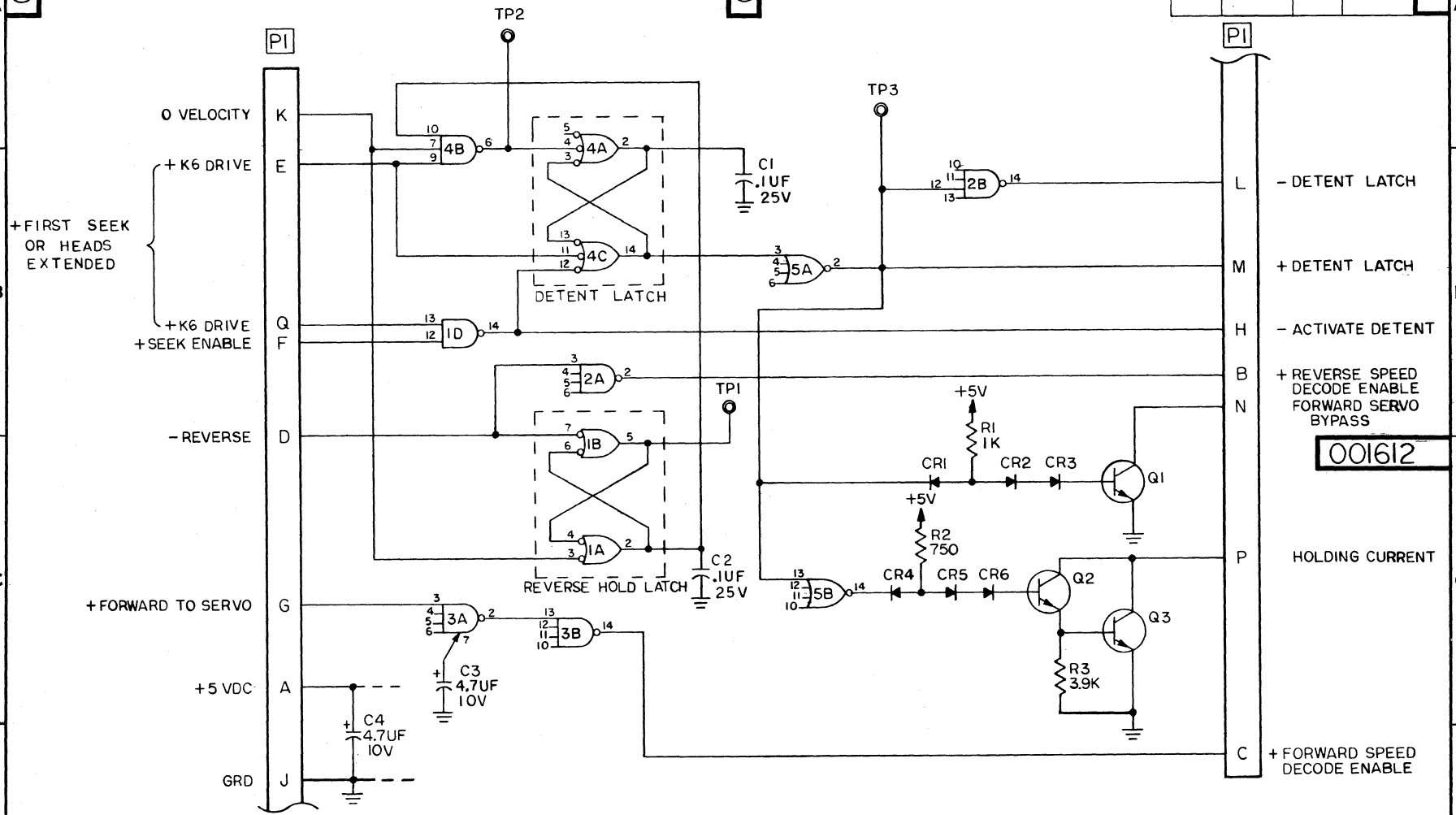
P.C. BOARD ASSEMBLY
FORCE SEEK COUNT

DESIGN			TYPE	
DETAIL			SCALE	2 / 1
CHECK	M.C.L	6/14/68	DRAW	K.B. 6-17-68
APPRO	CRF	6/19/68	CHECK	R.C.E 17Jun68

001551

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001611	5/23/68	104		
	6AUG68	161		

001612



001612

NOTES: UNLESS OTHERWISE SPECIFIED

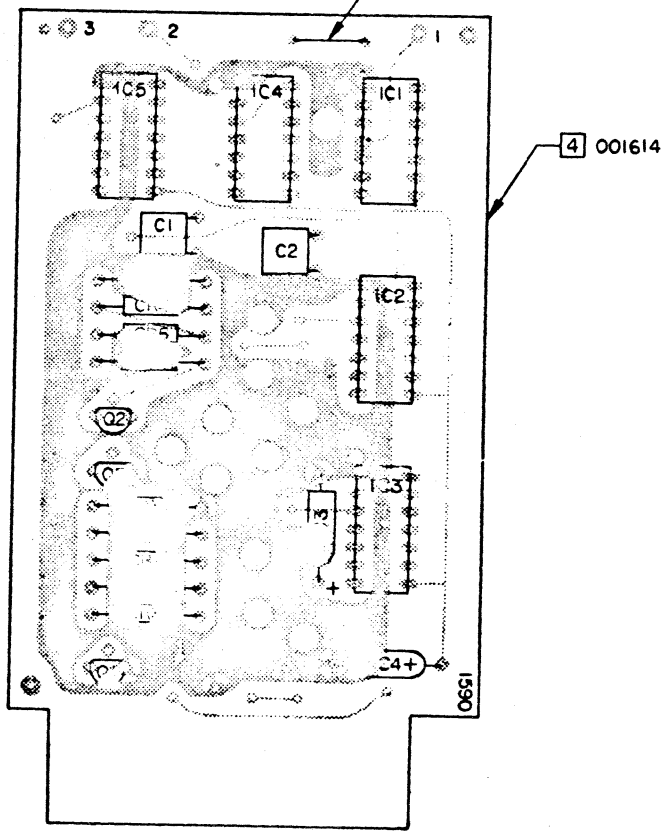
1. ALL RESISTORS ARE IN OHMS, 1/4W ±5%
2. ALL DIODES ARE IN4148
3. ALL TRANSISTORS ARE 2N3568
4. IC1 IS SP680A
5. IC'S 2,3 & 5 ARE SP659A
6. IC4 IS SP670A
7. CONNECT ALL IC PINS 1 TO GRD, PINS 8 TO +5V

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001612	C	RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	SCHEMATIC DIAGRAM				
	DETENT LOGIC II				
DESIGN				TYPE	
DETAIL				SCALE	NONE
CHECK	M.C.L.	6/10/68	DRAW	KB	5/23/68
APPRO	[illegible]	6/10/68	CHECK	[illegible]	27MAY68

C1,C2	CAPACITOR, .1 UF, 100V, ±10%	154151
C3,C4	CAPACITOR, 4.7 UF, 10V, ±10%	151124
CR1,2,3, 4,5,6	DIODE, 1N4148	150834
R1	RESISTOR, 1K, 1/4W, ±5%	151483
R2	RESISTOR, 750Ω, 1/4W, ±5%	151480
R3	RESISTOR, 3.9K, 1/4W, ±5%	151497
Q1, 2, 3	TRANSISTOR, 2N3568	150730
IC1	INTEGRATED CIRCUIT, SP680A	150656
IC2,3,5	INTEGRATED CIRCUIT, SP659A	150654
IC4	INTEGRATED CIRCUIT, SP670A	150655
——	TAG, ENGINEERING CHANGE	200304



001611

REFERENCE DOCUMENTS		EC LEVEL
SCHEM DIAGRAM	001612	161
APTMASTER	001613	1590

NOTES:

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER.
2. COMPONENT HEIGHT NOT TO EXCEED .350.
3. C1 & C2 MAY BE MOUNTED WITH BODY PARALLEL TO BOARD IF NECESSARY TO MEET NOTE 2 REQUIREMENT, OTHERWISE USE .050 MAX SPACER UNDER CAPACITOR BODY DURING SOLDERING.
4. P.C. BOARD 001614 MUST BE AT E.C. LEVEL 1590

MEMOREX EQUIPMENT GROUP

NAME: P.C. BOARD ASSEMBLY
DETENT LOGIC II

SCALE: 2/1

DRAWN: P.W. Jones 11-23-70
CHECK: NOV 70
APPRO: 12-7-70 12-7-70

001611

001611

REF DESIG	DESCRIPTION	P.S.C. PART NO.
———	PRINTED CIRCUIT BOARD	001614
C1,2	CAPACITOR, .1UF, 25V, ±10%	150980
C3,4	CAPACITOR, 4.7UF, 10V, ±10%	151124
CR1,2,3, 4,5,6	DIODE, IN4148	150834
R1	RESISTOR, 1K, 1/4W ±5%	151483
R2	RESISTOR, 750Ω, 1/4W ±5%	151480
R3	RESISTOR, 3.9K, 1/4W ±5%	151497
Q1,2,3	TRANSISTOR, 2N3568	150730
IC1	INTEG CIRCUIT, SP680A	150656
IC2,3,5	INTEG. CIRCUIT, SP659A	150654
IC4	INTEG. CIRCUIT, SP670A	150655
———	TAG, ENGINEERING CHG	200304

001611

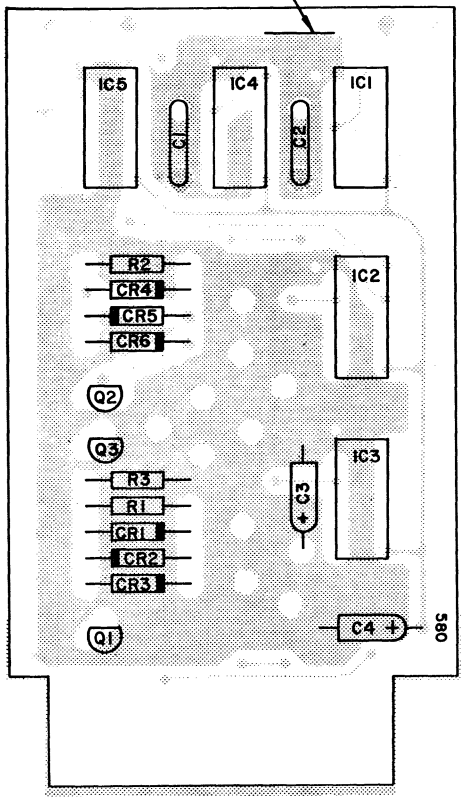
001611

001611

RELEASED FOR ASY	DATE	CHANGE NO.	DATE	CHANGE NO.
200490-60~	6-7-68	104		
200495-50~	8/10/68	161		
	11-19-68	219		
	1-2-70	580		

001611

200304 [1]



001611

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001612	161
ARTMASTER	001613	580
FABRICATION	001614	580

NOTES: UNLESS OTHERWISE SPECIFIED

[1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER

2 COMPONENT HEIGHT NOT TO EXCEED .350

SEE B/M 001611

001611 C

Peripheral Systems Corporation

P.C. BOARD ASSEMBLY

DETENT LOGIC II

SIZE C | SCALE 2/1

DES.			
DETAIL			
CHK	M.C.L	6/10/68	K.B. 6-7-68
APPRO			R.V.S. 8/10/68

001611

001342

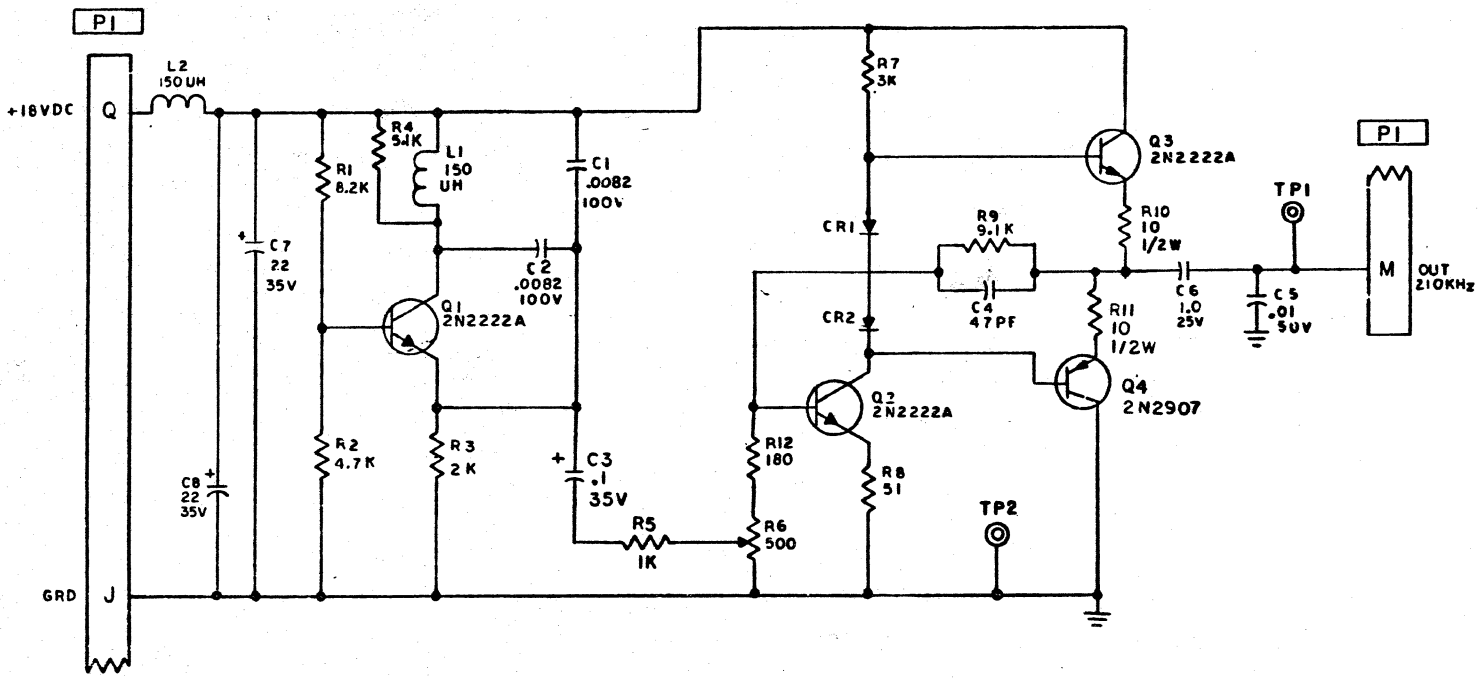
001342

001342

001342

001341			
3/11/68	14	7-17-69	249-A
3/21/68	34	Mar 7, 70	848
7/22/68	155	OCT, 70	1523
9/13/68	203		
12/5/68	249		

001342



001342

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS IN OHMS, 1/4W, ±5%
2. ALL CAPACITORS ARE IN MICROFARADS
3. ALL DIODES ARE IN4148

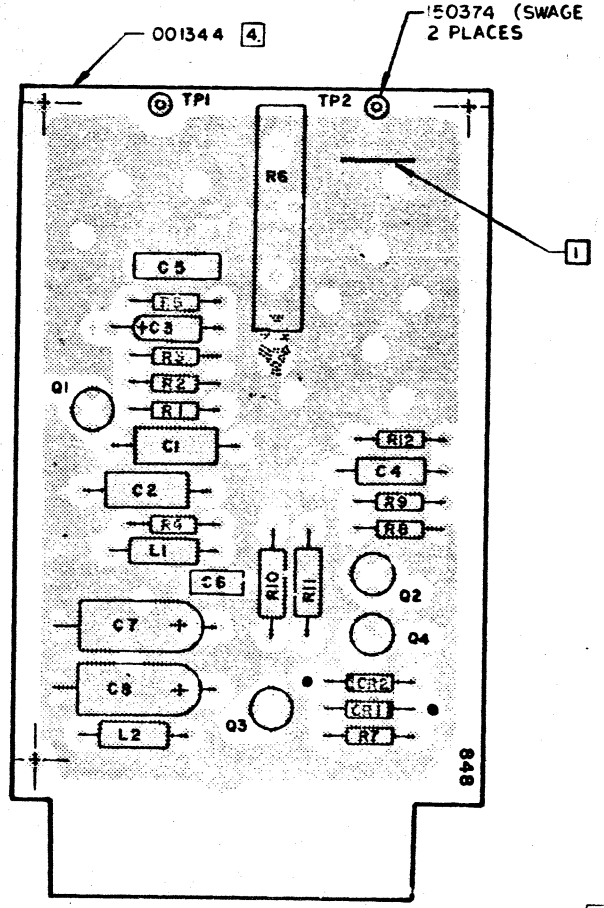
MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM TRANSDUCER OSCILLATOR
CASE DEPTH			ANGLES ±	DESIGN	JDM 3/12/68 TYPE
HARDNESS		CORNERS AND OR EDGES BROKEN	OUTSIDE MAX	DETAIL	SCALE NONE
SURFACE TREATMENT			INSIDE MAX	CHECK	DRAW EGS 12-22-67
001342	C	RADII UNLESS OTHERWISE NOTED		APPRO	CHECK

2 3 4 5

001341

REF DESIG	DESCRIPTION	M E G PART NO.
C1, 2	CAPACITOR, MM, .0082 UF/100V, ±10%	151062
C3	T, .1 UF, 50V, ±10%	151096
C4	P, 47PF, 500V, ±5%	151215
C5	PF, .01UF, 50V, ±10%	151020
C6	C, 1 UF, 25V, ±10%	150986
C7, 8	CAPACITOR, T, 22UF, 50V, ±10%	151147
CR1, 2	DIODE IN4148	150834
L1, 2	INDUCTOR, .50 UH, ±5%	151390
R6	POTENTIOMETER, 500Ω, 3/4W	153405
R1	RESISTOR, COMP, 2K, 1/4W, ±5%	151505
R2	4.7K, 1/4W, ±5%	151499
R3	2K, 1/4W, ±5%	151490
R5	1K, 1/4W, ±5%	151483
R7	3K, 1/4W, ±5%	151494
R8	51Ω, 1/4W, ±5%	151452
R9	9.1K, 1/4W, ±5%	151506
R12	160Ω, 1/4W, ±5%	151465
R4	5.1K, 1/4W, ±5%	151500
R10, 11	RESISTOR, COMP, 10Ω, 1/2W, ±5%	151579
Q1, 2, 3	TRANSISTOR, 2N2222A	150768
Q4	TRANSISTOR, 2N2907	150765
TP1, 2	TERMINAL, TURRET	150374
	ENGINEERING CHANGE TAG	200304

200490 – 60~	Mar 16,66	14	473
200495 – 50~	Mar 21,68	34	Nov 14,69 569
	Jun 22,66	155	Mar 7,70 848
	Sept 13,68	203	Jun, 70 1146
	Dec 5,66	249	Oct, 70 1523



001341

NOTES

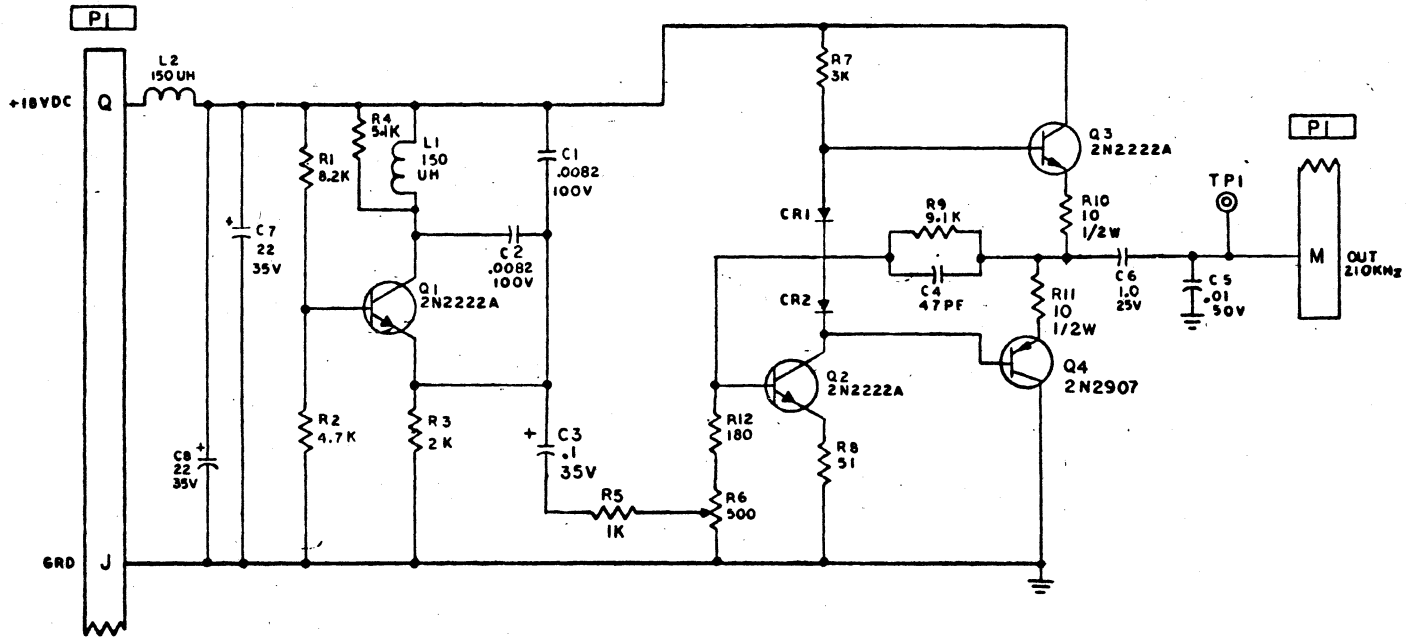
1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350
3. Q1,Q2,Q3,Q4 HEIGHT NOT TO EXCEED .330.
4. P.C. BOARD 001344 MUST BE AT EC LEVEL 848.
5. MUST CONFORM TO ENG SPECIFICATION 1345 AT EC LEVEL 848.

REFERENCE DOCUMENTS		EC LEVEL
SCH DIAG	001342	523
ARTMASTER	001343	848

SEE B/M			Peripheral Systems Corporation
			PC BOARD ASSEMBLY TRANSDUCER OSCILLATOR
001341	C		2/1

001341

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001341	2/7/68	14	7-17-69	249-A
	2/14/68	34	MAY 7, 70	848'
	7/22/68	155		
	9/13/68	203		
	12/5/68	249		



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS IN OHMS, 1/4W, ± 5%
2. ALL CAPACITORS ARE IN MICROFARADS
3. ALL DIODES ARE IN414B

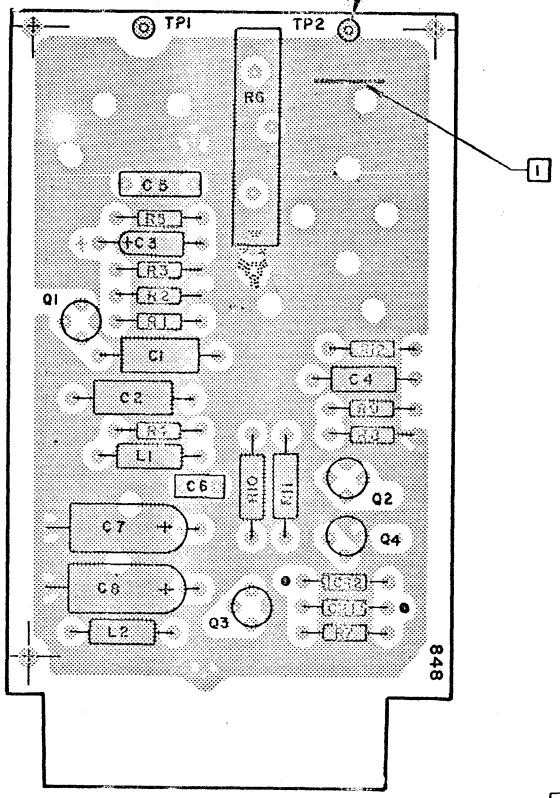
MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
CASE DEPTH			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM
HARDNESS			ANGLES ±		TRANSDUCER OSCILLATOR
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN JDM 3/2/68	TYPE
001342	C		INSIDE MAX	DETAIL	SCALE NONE
		RADII UNLESS OTHERWISE NOTED		CHECK 3/7/68	DRAW EGE 12-22-67
				APPRO JDM 3/7/68	CHECK RWP 7-22-68

001342

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490 – 60~	MAR 18,68	14	SEPT.15,69	473
200495 – 50~	MAR 21,68	34	NOV.14,69	569
	JUN 22,68	155	MAY 7,70	848
	SEPT. 13,68	203	JUN, 70	1146
	DEC. 5, 68	249		

REF DESIG	DESCRIPTION	M. E. G. PART NO.
———	PRINTED CIRCUIT BOARD	001344
C1, 2	CAPACITOR, M, .0082 UF/100V ±10%	151062
C3	T, .1 UF, 35V, ±10%	151096
C4	P, 47PF, 500V ±5%	151215
C5	PF, .01UF, 50V, ±10%	151020
C6	C, 1 UF, 50V, ±20%	150997
C7, 8	CAPACITOR, T, 22UF, 35V, ±10%	151147
CR1, 2	DIODE, IN4148	150834
L1, 2	INDUCTOR, 150 UH, ±5%	151390
R6	POTENTIOMETER, 500Ω, 3/4W	153405
R1	RESISTOR, COMP, 8.2K, 1/4W, ±5%	151505
R2	4.7K, 1/4W, ±5%	151499
R3	2K, 1/4W, ±5%	151490
R5	1K, 1/4W, ±5%	151483
R7	3K, 1/4W, ±5%	151494
R8	51Ω, 1/4W, ±5%	151462
R9	9.1K, 1/4W, ±5%	151506
R12	160Ω, 1/4W, ±5%	151465
R4	5.1K, 1/4W, ±5%	151500
R10, 11	RESISTOR, COMP, 10Ω, 1/2W, ±5%	151579
Q1, 2, 3	TRANSISTOR, 2N2222A	150768
Q4	TRANSISTOR, 2N2907	150765
TP1, 2	TERMINAL, TURRET	150374
	ENGINEERING CHANGE TAG	200304

150374 (SWAGE FARSIDE)
2 PLACES



NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350
3. Q1,Q2,Q3,Q4 HEIGHT NOT TO EXCEED .330.

REFERENCE DOCUMENTS		E.C. LEVEL
SCH. DIAG.	001342	848
ARTMASTER	001343	848
FABRICATION	001344	848
TEST SPEC.	001345	848

MATERIAL SEE B/M NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation, a subsidiary of MEMOREX CORPORATION
CASE DEPTH		3 PLACE DEC ±	NAME PC. BOARD ASSEMBLY
HARDNESS		ANGLES ±	TRANSDUCER OSCILLATOR
SURFACE TREATMENT	CORNERS AND OR EDGES BROKEN	OUTSIDE MAX	DESIGN — TYPE
001341 C		INSIDE MAX	DETAIL — SCALE 2/1
	RADII UNLESS OTHERWISE NOTED		CHECK — DRAW MAY 6,70
			APPRO — CHECK MAY 6,70

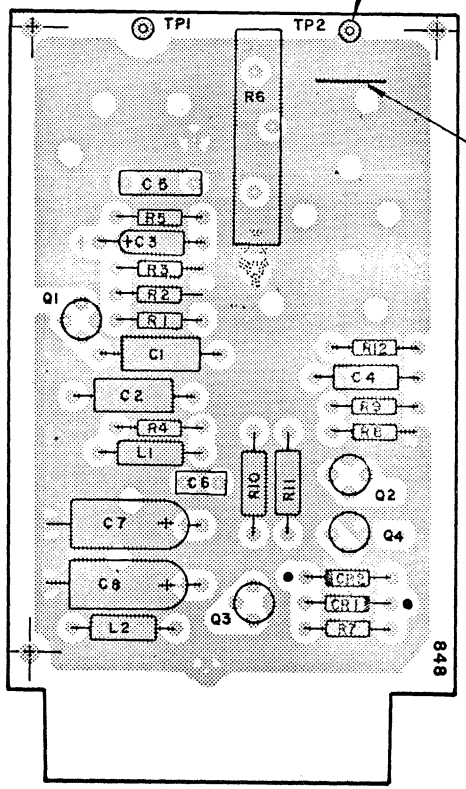
001341

001341

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490 – 60~	MAR 18,68	14	SEPT.15,69	473
200495 – 50~	MAR 21,68	34	NOV.14,69	569
	JUN 22,68	155	MAY 7,70	848
	SEPT. 13,68	203		
	DEC. 5,68	249		

REF DESIG	DESCRIPTION	M. E. G. PART NO.
———	PRINTED CIRCUIT BOARD	001344
C1, 2	CAPACITOR, M., .0082 UF/100V ±10%	151062
C3	T, .1 UF, 35V, ±10%	151096
C4	P, 47 PF, 500V ±5%	151215
C5	PF, .01 UF, 50V, ±10%	151020
C6	C, 1 UF, 50V, ±20%	150997
C7, 8	CAPACITOR, T, 22 UF, 35V, ±10%	151147
CR1, 2	DIODE, 1N4148	150834
L1, 2	INDUCTOR, 150 UH, ±5%	151390
R6	POTENTIOMETER, 500Ω, 3/4W	153405
R1	RESISTOR, COMP, 8.2K, 1/4W, ±5%	151505
R2	4.7K, 1/4W, ±5%	151499
R3	2K, 1/4W, ±5%	151490
R5	1K, 1/4W, ±5%	151483
R7	3K, 1/4W, ±5%	151494
R8	51Ω, 1/4W, ±5%	151452
R9	9.1K, 1/4W, ±5%	151506
R12	180Ω, 1/4W, ±5%	151465
R4	5.1K, 1/4W, ±5%	151500
R10, 11	RESISTOR, COMP, 10Ω, 1/2W, ±5%	151579
Q1, 2, 3	TRANSISTOR, 2N2222A	150768
Q4	TRANSISTOR, 2N2907	150765
TP1, 2	TERMINAL, TURRET	150374
	ENGINEERING CHANGE TAG	200304

150374 (SWAGE FARSIDE)
2 PLACES



001341

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

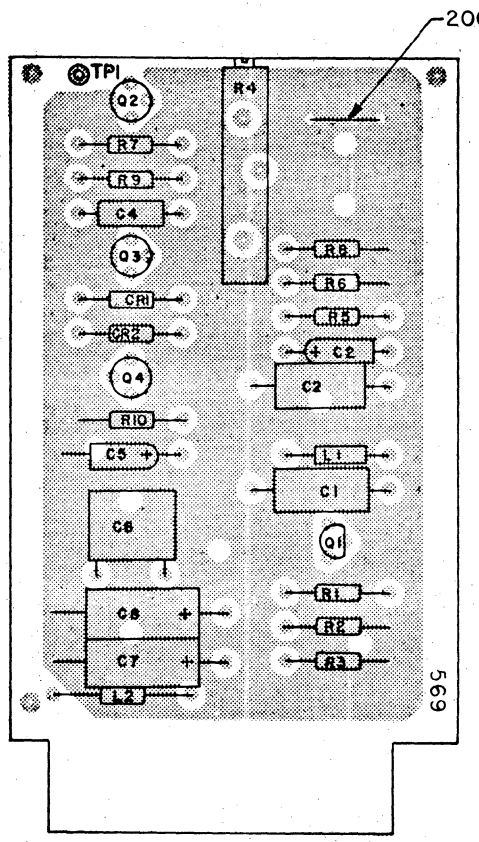
REFERENCE DOCUMENTS		E.C. LEVEL
SCH. DIAG.	001342	848
ARTMASTER	001343	848
FABRICATION	001344	848
TEST SPEC.	001345	848

MATERIAL SEE B/M NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION
CASE DEPTH		3 PLACE DEC ±	NAME P.C. BOARD ASSEMBLY TRANSDUCER OSCILLATOR
HARDNESS		ANGLES ±	
SURFACE TREATMENT	CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN TYPE
001341 C	RADII UNLESS OTHERWISE NOTED	INSIDE MAX	DETAIL SCALE 2/1
			CHECK DRAW G.S. MAY 6 70
			APPRO CHECK

001341

001341

REF DESIG	DESCRIPTION	M. E. G. PART NO
———	PRINTED CIRCUIT BOARD	001344
C1,2	CAPACITOR, .01 UF, 100V ± 10%	151063
C3	.1UF, 35V ± 10%	151096
C4	47PF, 500V, ± 5%	151215
C5	3.3UF, 50V ± 10%	151140
C6	1UF, 25V ± 20%	150986
C7,8	CAPACITOR, 22UF, 35V ± 10%	151147
CR1,2	DIODE, IN4148	150834
L1,2	INDUCTOR, 150UH ± 5%	151390
R4	POTENTIOMETER, 5K, 3/4W ± 20%	153408
R1	RESISTOR, 8.2K 1/4W ± 5%	151505
R2	4.7K	151499
R3	2K	151490
R5	1K	151483
R6	680Ω	151479
R7	3K	151494
R8	51Ω	151452
R9	9.1K	151506
R10	RESISTOR, 150Ω 1/4W ± 5%	151463
Q1	TRANSISTOR, 2N3904	150735
Q2,3	TRANSISTOR, 2N3568	150730
Q4	TRANSISTOR, 2N3638	150731
	TAG, ENGINEERING CHG	200304



001341

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490-60 ~	3/15/68	14	9/13/68	473
200495-50 ~	4/21/68	34	11/4/68	569
	7/23/68	155		
	7/17/68	203		
	12/5/68	249		

001341

001341

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001342	249
ARTMASTER	001343	569
FABRICATION	001344	569

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST - ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL	SEE B/M NO 001341
CASE DEPTH	
HARDNESS	
SURFACE TREATMENT	

001341 C

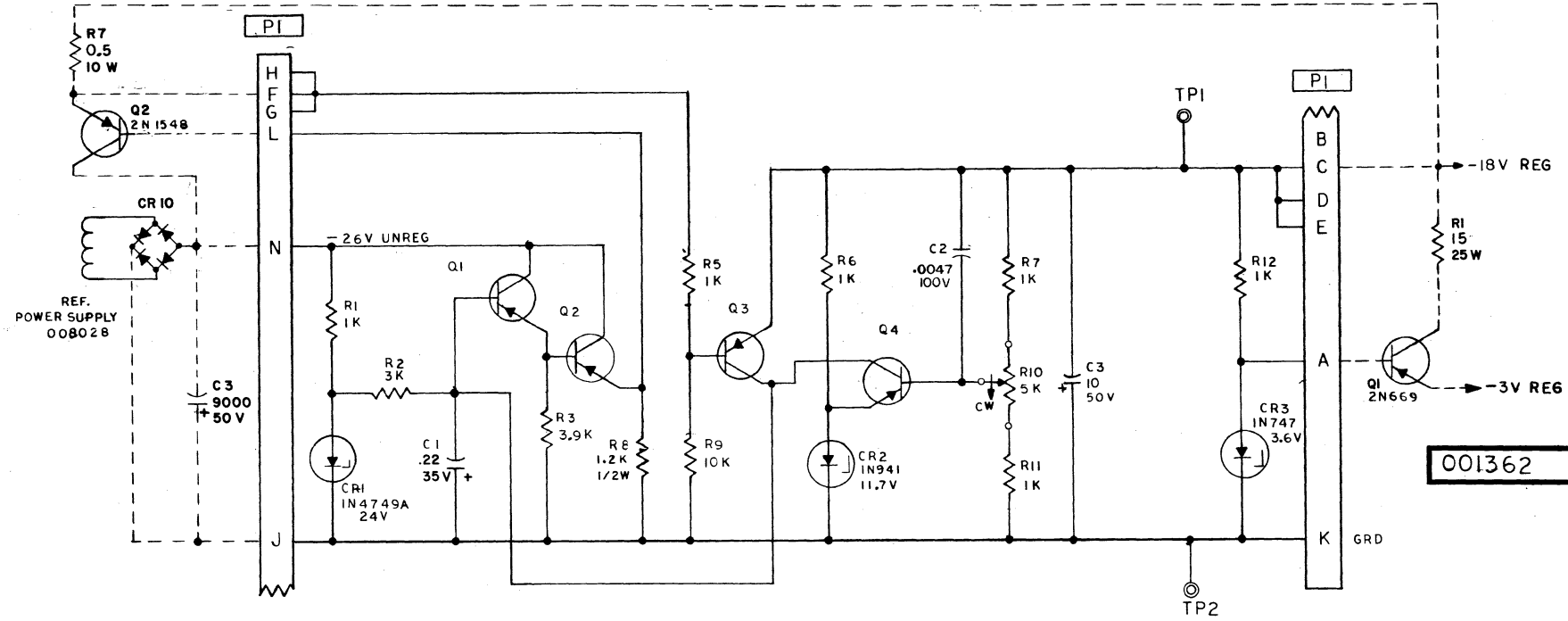
TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
	3 PLACE DEC ±
	ANGLES ±
CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
	INSIDE MAX
RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	P.C. BOARD ASSEMBLY				
	TRANSDUCER OSCILLATOR				
DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK	LLP	7/26/68	DRAW	KB	7/22/68
APPRO	[illegible]	7/24/68 7/29/68	CHECK	EDE	7/23/68

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001361	3/9/68	14	JUN 20	1146
	3/21/68	34		
	19JUN68	114		
	27AUG68	183		
	1-22-70	561		

001362



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS 1/4 W, ±5%
2. ALL CAPACITORS ARE IN MICROFARADS
3. **ALL TRANSISTORS ARE 2N4037**
4. **COMPONENTS SHOWN IN DOTTED LINES ARE FOR REFERENCE ONLY.**

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation, a subsidiary of MEMOREX CORPORATION
			3 PLACE DEC ±	NAME: SCHEMATIC DIAGRAM
CASE DEPTH			ANGLES ±	REGULATOR -18 &-3VDC
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN / TYPE
SURFACE TREATMENT			INSIDE MAX	DETAIL / SCALE: NONE
001362	C	RADII UNLESS OTHERWISE NOTED		CHECK / DRAW: EGG 1-2-68
				APPRO / CHECK

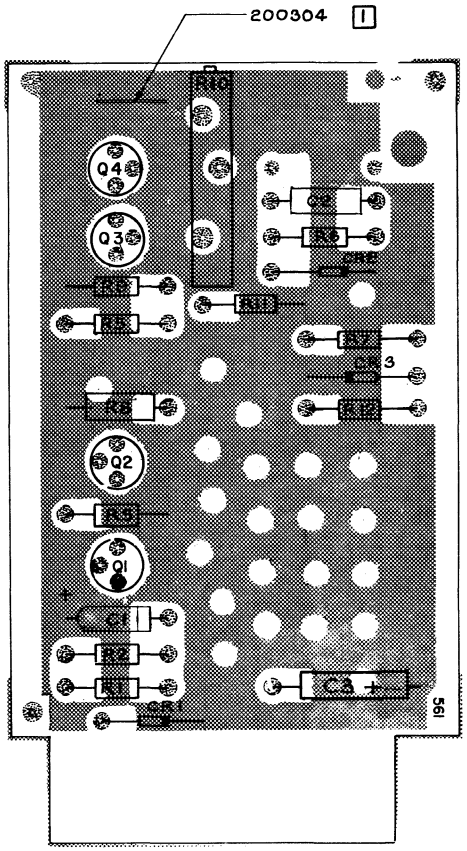
001361

REF DESIG	DESCRIPTION	P.S.C. PART NO.
—	PRINTED CIRCUIT BOARD	001364
C1	CAPACITOR, T, .22 UF, 35 V, ± 10%	151098
C2	CAPACITOR, M, .0047 UF, 100V, ± 10%	151058
C3	CAPACITOR, 10 UF, 50V;	150939
CR1	DIODE (IN4749A) 24V ZENER	150836
CR2	DIODE (IN941) 11.7V ZENER	150842
CR3	DIODE (IN 747) 3.6V ZENER	150828
Q1,2,3,4	TRANSISTORS, 2N 1037	150745
R1,5,6,7	RESISTORS - 1K, 1/4W, ±5%	151483
R11,12		
R2	RESISTOR - 3K, 1/4W, ±5%	151494
R9	RESISTOR - 10K, 1/4W, ±5%	151507
R10	POTENTIOMETER - 5K, 3/4W, ±20%	153408
R3	RESISTORS - 3.9K, 1/4W, ±5%	151497
R8	RESISTOR, 1.2 K, 1/2W, ± 5%	151629
—	TAG, ENGINEERING CHANGE	200304

001361

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
630 A	200490	17MAR68	14	1-21-70	561
630 B	200495	3/21/68	34	JAN 70	1146
620	202032	12JUN68	114		
		27AUG68	183		
		11-19-68	219		

001361



001361

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001362	1146
ARTMASTER	001363	561
FABRICATION	001364	561

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350.
3. Q1,Q2,Q3,Q4 HEIGHT NOT TO EXCEED .310

001361

MATERIAL SEE B/M	NO. 001361	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001361	C	RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME ASSEMBLY DRAWING
-18 -3 VDC REGULATOR

DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK			DRAW	HAB	1-26-68
APPRO	JDF	20 MAR 68 3-27-68	CHECK	RJE	19MAR68

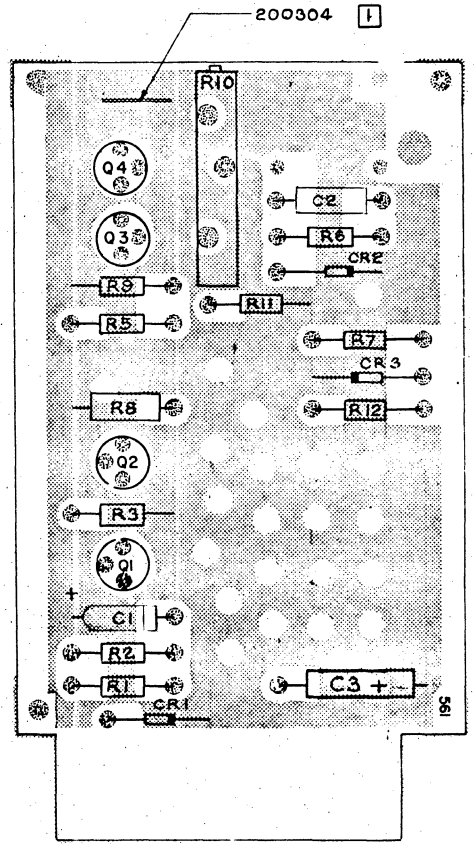
001361

REF DESIG	DESCRIPTION	P.S.C. PART NO.
—	PRINTED CIRCUIT BOARD	001364
C1	CAPACITOR, T, .22 UF, 35 V, ± 10%	151098
C2	CAPACITOR, M, .0047 UF, 100V, ± 10%	151058
C3	CAPACITOR, 10 UF, 50V,	150939
CR1	DIODE (1N4749A) 24V ZENER	150836
CR2	DIODE (1N941) 11.7V ZENER	150842
CR3	DIODE (1N747) 3.6V ZENER	150828
Q1,2,3,4	TRANSISTORS, [illegible]	[illegible]
R1,5,6,7	RESISTORS - 1K, 1/4W, ±5%	151483
R11,12		
R2	RESISTOR - 3K, 1/4W, ±5%	151494
R9	RESISTOR - 10K, 1/4W, ±5%	151507
R10	POTENTIOMETER - 5K, 3/4W, ±20%	153408
R3	RESISTORS - 3.9K, 1/4W, ±5%	151497
R8	RESISTOR, 1.2 K, 1/2W, ± 5%	151629
—	TAG, ENGINEERING CHANGE	200304

001361

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
630 A	200490	[illegible]	14	1-21-70	561
630 B	200495	[illegible]	34		
620	202032	[illegible]	114		
		[illegible]	183		
		11-19-68	219		

001361



001361

REFERENCE DOCUMENTS		E.C. LEVEL
SCH. DIAG.	001362	561
ARTMASTER	001363	561
FABRICATION	001364	561

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350.

001361

MATERIAL SEE B/M	NO. 001361		
CASE DEPTH			
HARDNESS			
SURFACE TREATMENT			
001361	C		

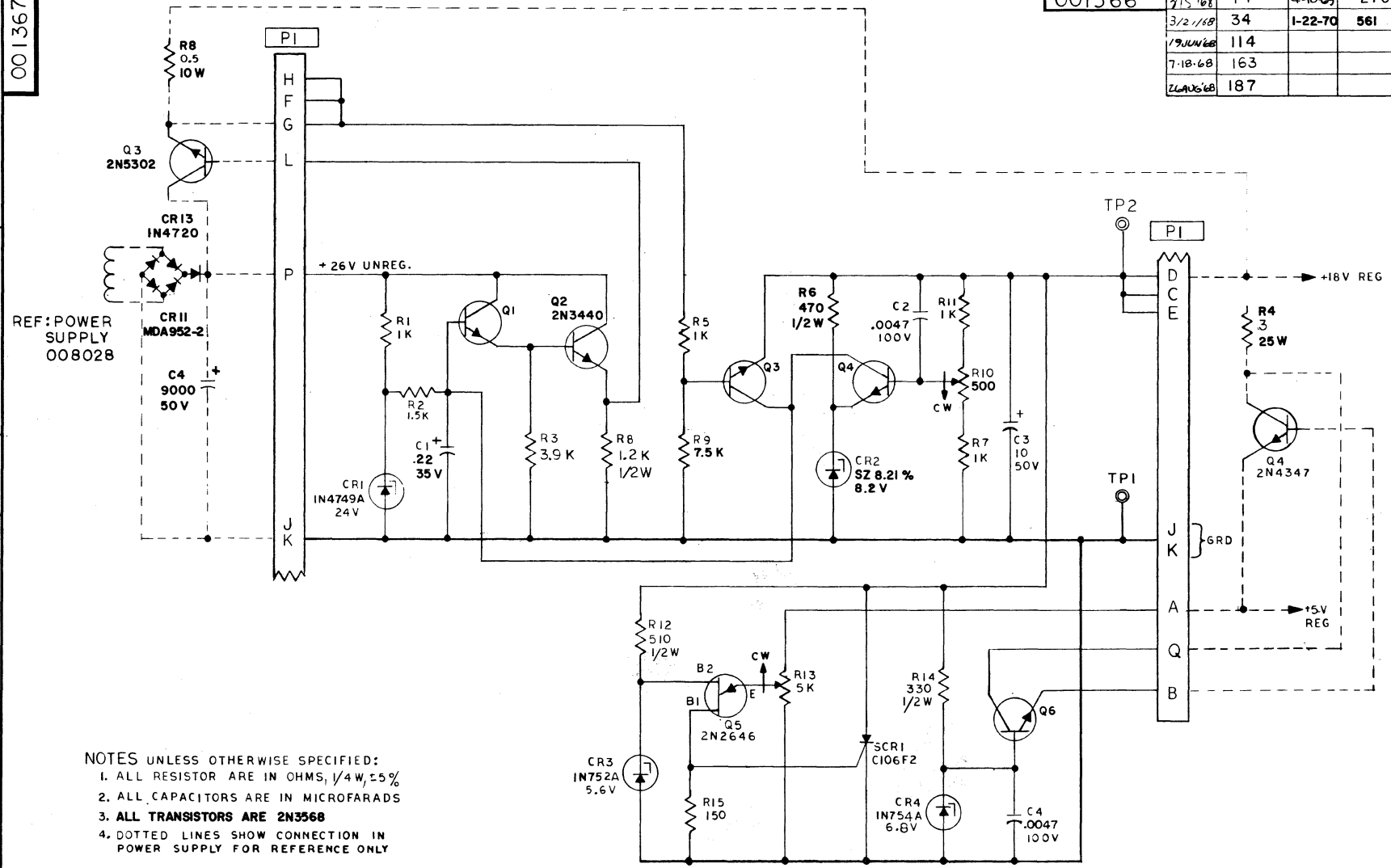
TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	
	3 PLACE DEC ±	
	ANGLES	
CORNERS AND OR EDGES BROKEN	OUTSIDE	MAX
	INSIDE	MAX
RADII UNLESS OTHERWISE NOTED		

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	ASSEMBLY DRAWING				
	-18 -3 VDC REGULATOR				
DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK			DRAW	HAB	1-26-68
APPRO	[illegible]	[illegible]	CHECK	[illegible]	19 MAR 68

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001366	3/5/68	14	4-10-69	276
	3/21/68	34	1-22-70	561
	19JUN'68	114		
	7-18-68	163		
	12AUG'68	187		

001367



NOTES UNLESS OTHERWISE SPECIFIED:

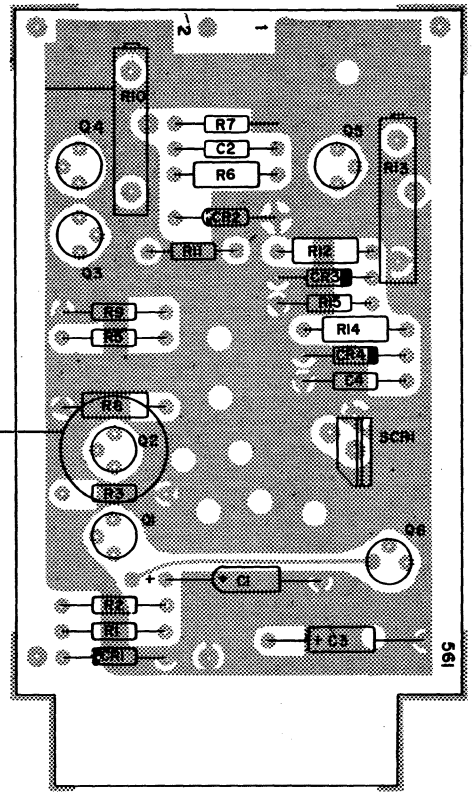
1. ALL RESISTOR ARE IN OHMS, 1/4W, ±5%
2. ALL CAPACITORS ARE IN MICROFARADS
3. **ALL TRANSISTORS ARE 2N3568**
4. DOTTED LINES SHOW CONNECTION IN POWER SUPPLY FOR REFERENCE ONLY

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM
CASE DEPTH			ANGLES ±		REGULATOR +18 & +5VDC
HARDNESS			OUTSIDE MAX	DESIGN CM 3/6/68	TYPE
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	INSIDE MAX	DETAIL	SCALE NONE
001367	C	RADII UNLESS OTHERWISE NOTED		CHECK Uam 3/5/68	DRAW EGG 1/4/68
				APPRO JDM 3/6/68	CHECK RJS 4-9-68

001367

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
630-A	200490	3-4-68	14	11-19-68	219
630-B	200495	3-21-68	34	4-10-69	276
620	202032	6-19-68	114	7-21-69	276A
		7-18-68	163	9-2-69	438
		8-26-68	187	1-22-70	561

REF DESIG	DESCRIPTION	M. E. G. PART NO.
———	PRINTED CIRCUIT BOARD	001369
C1	CAPACITOR,T, .22UF,35 V, ± 10%	151098
C3	CAPACITOR,E, 10 UF, 50V, +70%,-10%	150939
C2,4	CAPACITOR,M, .0047UF, 100V, ± 10%	151058
CR1	DIODE,IN4749A,24 V	150836
CR2	DIODE, SZ8 21%, 8.2 V	150903
CR4	DIODE, IN754A, 6.8V	150846
CR3	DIODE, IN752A, 5.6V	150830
R6	RESISTOR, 470 OHM, 1/2 W, ± 5%	151619
R1,5,7,11	1K, 1/4 W, ± 5%	151483
R2	1.5K, 1/4 W, ± 5%	151487
R3	3.9K, 1/4 W, ± 5%	151497
R4	NOT ASSIGNED	
R9	7.5K, 1/4 W, ± 5%	151504
R12	510 OHM, 1/2W, ± 5%	151620
R14	330 OHM, 1/2W, ± 5%	151615
R15	150 OHM, 1/4W, ± 5%	151463
R8	RESISTOR, 1.2K, 1/2W, ± 5%	151605
R13	POTENTIOMETER, 5K, 3/4W, ± 20%	153408
R10	POTENTIOMETER, 500 OHM, 3/4W, ± 20%	153405
Q1,3,4,6,	TRANSISTOR, 2N 3568	150730
Q5	TRANSISTOR, 2N 2646	150729
Q2	TRANSISTOR, 2N 3440	150744
SCR1	SILICON CONTROLLED RECTIFIER	150630
———	PAD, TRANSISTOR MOUNTING	200718
———	HEAT SINK, TRANSISTOR	200719
———	ENGINEERING CHANGE TAG	200304



NOTES: UNLESS OTHERWISE SPECIFIED
1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

REFERENCE DOCUMENTS		E.C. LEVEL
SCH. DIAG.	001367	561
ARTMASTER	001368	561
FABRICATION	001369	561
TEST SPEC.		

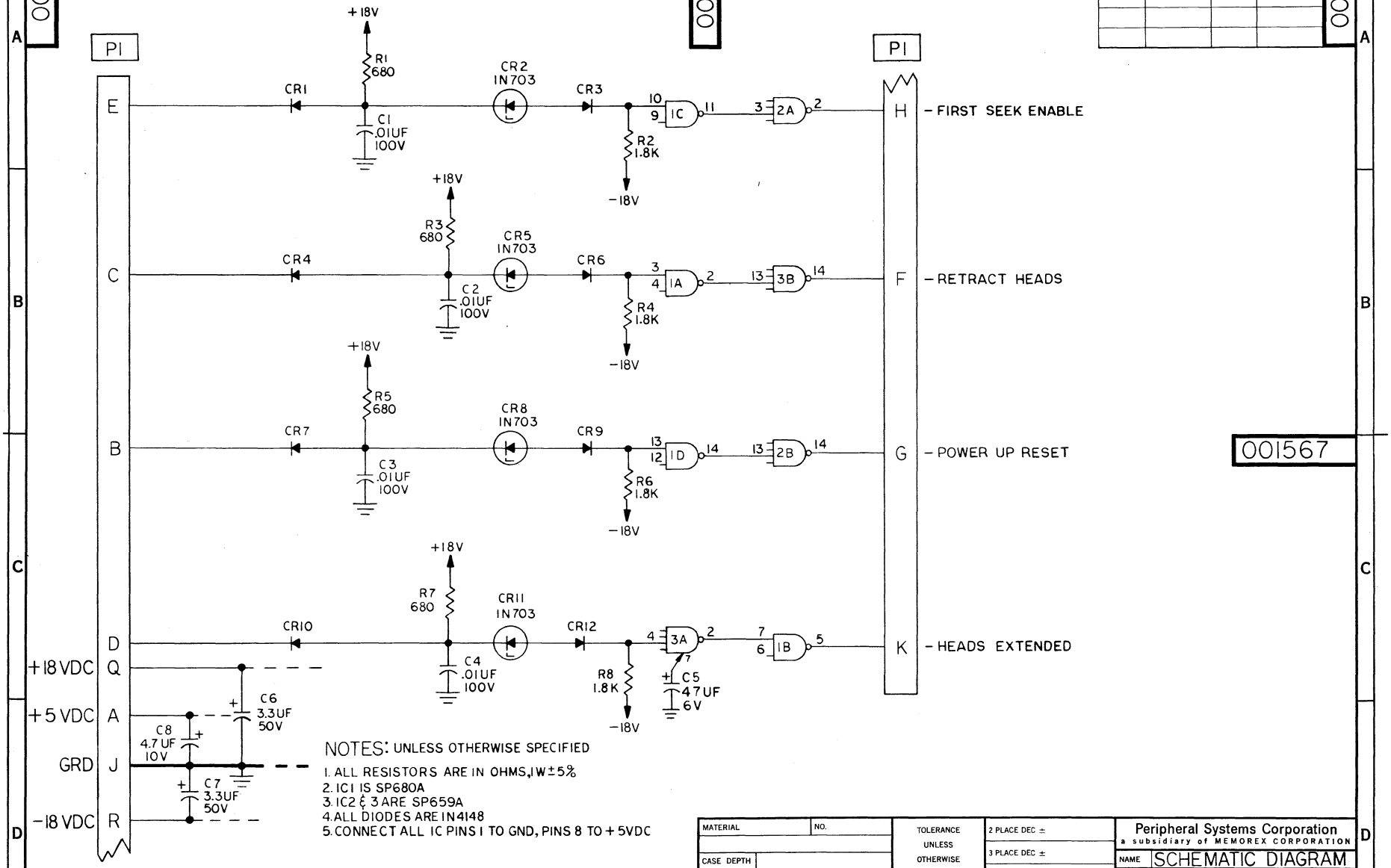
MATERIAL SEE B/M	NO. 001366	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
CASE DEPTH			3 PLACE DEC ±
HARDNESS			ANGLES ±
SURFACE TREATMENT		CORNERS AND OR EDGES BROKEN	OUTSIDE MAX
001366	C		INSIDE MAX
		RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME P.C. BOARD ASSEMBLY
+18, +5 VDC REGULATOR

DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK			DRAW	[illegible]	1-23-70
APPRO	JDM WBW	3-6-68 3-27-68	CHECK	RdE.	4 mar 68

001366


001567
001567
001567
001567
001567
001567
RELEASED FOR ASSY
DATE
CHANGE NO
DATE
CHANGE NO
001566
5-9-68
88
P1
P1
+18V
R1 680
CR1
CR2 IN703
CR3
C1 .01UF 100V
R2 1.8K
-18V
1C
2A
E
H
- FIRST SEEK ENABLE
+18V
R3 680
CR4
CR5 IN703
CR6
C2 .01UF 100V
R4 1.8K
-18V
1A
3B
C
F
- RETRACT HEADS
+18V
R5 680
CR7
CR8 IN703
CR9
C3 .01UF 100V
R6 1.8K
-18V
1D
2B
B
G
- POWER UP RESET
+18V
R7 680
CR10
CR11 IN703
CR12
C4 .01UF 100V
R8 1.8K
-18V
3A
1B
C5 47UF 6V
D
K
- HEADS EXTENDED
+18 VDC
Q
+5 VDC
A
GRD
J
-18 VDC
R
C6 3.3UF 50V
C8 4.7UF 10V
C7 3.3UF 50V
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1W ±5%
2. IC1 IS SP680A
3. IC2 & 3 ARE SP659A
4. ALL DIODES ARE IN4148
5. CONNECT ALL IC PINS 1 TO GND, PINS 8 TO +5VDC
001567
001567
C
MATERIAL
NO.
CASE DEPTH
HARDNESS
SURFACE TREATMENT
TOLERANCE UNLESS OTHERWISE NOTED
2 PLACE DEC ±
3 PLACE DEC ±
ANGLES ±
CORNERS AND/OR EDGES BROKEN
OUTSIDE MAX
INSIDE MAX
RADII UNLESS OTHERWISE NOTED
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION
NAME SCHEMATIC DIAGRAM
SIGNAL CONDITIONER
DESIGN
TYPE
DETAIL
SCALE
CHECK
5-10-68
DRAW K.B. 5-9-68
APPRO
CHECK R.L.E. 10 Jun 68

001566

REF DESIG	DESCRIPTION	P.S.C. PART NO.
———	PRINTED CIRCUIT BOARD	001569
C1,2,3,4	CAPACITOR .01UF, 100V, ±10%	151063
C5	CAPACITOR, 27 UF, [illegible] V, ±10%	[illegible]
C6,7	CAPACITOR, 3.3UF, 50V, ±10%	151140
C8	CAPACITOR, 4.7UF, 10V ±10%	151124
CR1,3,4,6, 9,10,12	DIODE, IN4148	150834
CR2,5,8,11	DIODE Z, IN703 3.4V, ±10%	150839
R1,3,5,7	RESISTOR 680Ω, 1W ±5%	151767
R2,4,6,8	RESISTOR 1.8K, 1W ±5%	151777
IC1	INTEGRATED CIRCUIT, SP680A	150656
IC2,3	INTEGRATED CIRCUIT, SP659A	150654
———	TAG, ENG. CHANGE	200304

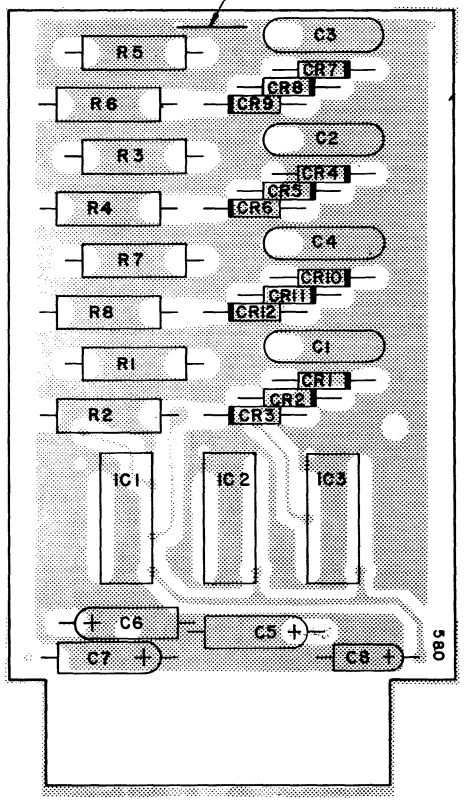
001566

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490-60~	9 MAY 68	88		
200495-50~	16 MAY 68	154		
	11-19-68	219		
	7-21-69	219 A		
	1-2-70	580		

001566

001566

200304 [1]



001566

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001567	88
ARTMASTER	001568	580
FABRICATION	001569	580

NOTES: UNLESS OTHERWISE SPECIFIED

[1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER

2 COMPONENT HEIGHT NOT TO EXCEED 350

SEE B/M	001566

001566 C

Peripheral Systems Corporation

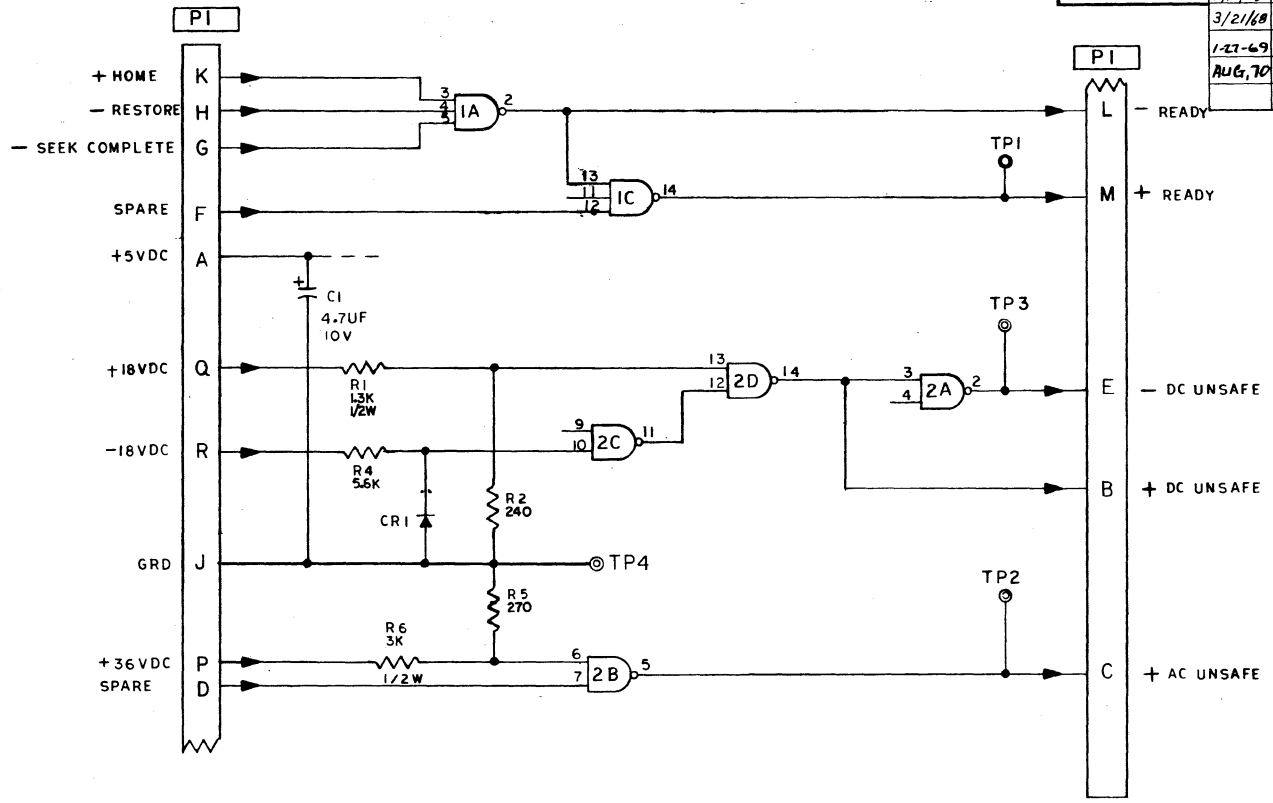
ASSEMBLY DRAWING

SIGNAL CONDITIONER

DES'D			TYPE	
DETAIL			SCALE	2/1
CHECK	MC L.	5-17-68	DRAW.	K.B. 5-9-68
APPRO	[illegible]	6-11-68	CHECK	R.D.E. 10 Jun 68

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001441	1/18/68	14		
	3/21/68	34		
	1-27-69	254		
	AUG, 70	1263		

001442



001442

NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTORS ARE IN OHMS, 1/4W, ±5%
2. ALL DIODES ARE IN4148
3. IC1 IS SP670A
4. IC2 IS SP680A
5. CONNECT PIN 1 OF ALL IC'S TO GRD
6. CONNECT PIN 8 OF ALL IC'S TO +5VDC

REF DESIG NOT USED
R3

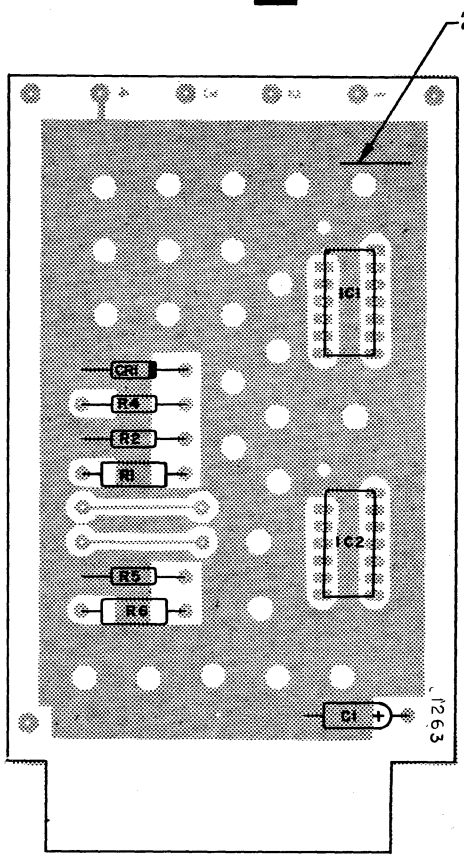
MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION
CASE DEPTH			3 PLACE DEC ±	NAME SCHEMATIC DIAGRAM AC/DC SAFETY
HARDNESS			ANGLES ±	
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN TYPE
001442	C		INSIDE MAX	DETAIL SCALE NONE
		RADII UNLESS OTHERWISE NOTED		CHECK 3/18/68 DRAW EGG 12-15-67
				APPRO 3/18/68 CHECK

001442

001441

REF DESIG	DESCRIPTION	P.S.C. PART NO.
–	PRINTED CIRCUIT BOARD	001444
C1	CAPACITOR-4.7UF, 10V, ± 10%	151124
CR1	DIODE (IN4148)	150834
R1	RESISTOR, 1.3K, 1/2W, ±5%	151630
R2	,240 OHMS, 1/4W, ±5%	151468
R4	,5.6K, 1/4W, ±5%	151501
R5	,270 OHMS, 1/4W, ±5%	151469
R6	RESISTOR, 3K, 1/2W, ±5%	151638
IC1	INTEGRATED CIRCUIT (SP670A)	150655
IC2	INTEGRATED CIRCUIT (SP680A)	150656
–	ENGINEERING CHANGE TAG	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490 – 60HZ	3 18 68	14	AUG, 70	1263
200495 – 50HZ	3 21 68	34		
MULTI-USE	1 27 69	254		
	11 12 69	569		
	MAY 6, 70	1004		



001441

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001442	1263
ARTMASTER	001443	1263
FABRICATION	001444	1263
ENG SPEC	001445	1263

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL	SEE B/M NO 001441
CASE DEPTH	
HARDNESS	
SURFACE TREATMENT	

001441 C

TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
	3 PLACE DEC ±
	ANGLES ±
CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
	INSIDE MAX
RADII UNLESS OTHERWISE NOTED	

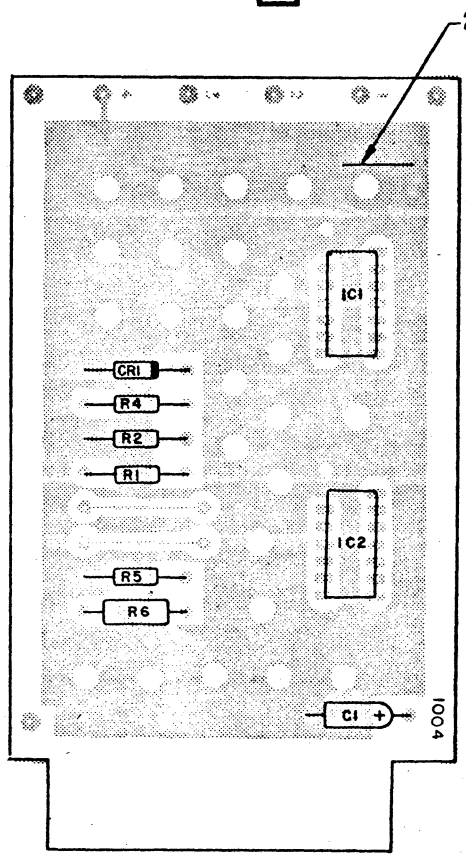
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	P.C. BOARD ASSEMBLY				
	A.C./D.C. SAFETY				
DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK	JOK	3/15/68	DRAW	HSD	1/27/68
APPRO	JOK	3/15/68	CHECK	RDE	3/18/68

001441

REF DESIG	DESCRIPTION	P.S.C. PART NO.
–	PRINTED CIRCUIT BOARD	001444
C1	CAPACITOR-4.7UF, 10V, ±10%	151124
CR1	DIODE (IN4148)	150834
R1	RESISTOR-3.9K, 1/4 W, ±5%	151497
R2	RESISTOR-2K, 1/4 W, ±5%	151490
R4	RESISTOR-8.2K, 1/4 W, ±5%	151505
R5	RESISTOR-240Ω 1/4 W, ±5%	151468
R6	RESISTOR-1.5K, 1/2 W, ±5%	151631
IC1	INTEGRATED CIRCUIT (SP670A)	150655
IC2	INTEGRATED CIRCUIT (SP680A)	150656
–	ENGINEERING CHANGE TAG	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490 - 60HZ	S 18 68	14		
200495--50HZ	S 21 68	34		
MULTI-USE	I 27 69	254		
	II 12 69	569		
	MAY 6,70	1004		



REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001442	254
ARTMASTER	001443	1004
FABRICATION	001444	1004

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M	NO 001441	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND OR EDGES BROKEN	OUTSIDE MAX.
SURFACE TREATMENT			INSIDE MAY
001441	C	RADII UNLESS OTHERWISE NOTED	

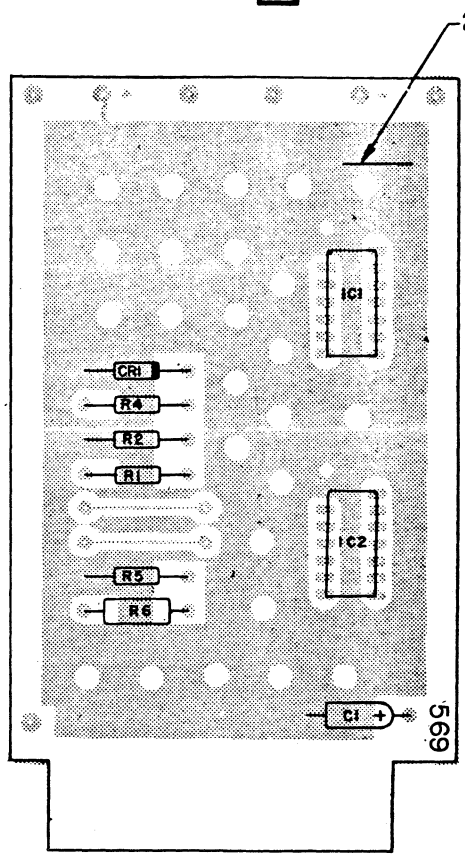
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	P.C. BOARD ASSEMBLY			
	A.C./D.C. SAFETY			
DESIGN			TYPE	
DETAIL			SCALE	2/1
CHECK	JCC	3/15/68	DRAW	HEP 1/24/68
APPRO	JCK	3/15/68	CHECK	EDE 3/15/68

C01441

REF DESIG	DESCRIPTION	P.S.C. PART NO.
–	PRINTED CIRCUIT BOARD	001444
C1	CAPACITOR 47UF, 10V, ±10%	151124
CR1	DIODE (IN4148)	150834
R1	RESISTOR 3.9K 1/4 W, ±5%	151497
R2	RESISTOR 2K 1/4 W, ±5%	151490
R4	RESISTOR 8.2K, 1/4 W, ±5%	151505
R5	RESISTOR 240Ω 1/4 W, ±5%	151462
R6	RESISTOR 1.5K, 1/2 W, ±5%	151631
IC1	INTEGRATED CIRCUIT (SP670A)	150655
IC2	INTEGRATED CIRCUIT (SP680A)	150656
–	ENGINEERING CHANGE TAG	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490 – 60HZ	3 18 68	14		
200495 – 50HZ	3 21 68	34		
	I 27 69	254		
	II 12 69	569		



REFERENCE DOCUMENTS		EC LEVEL
SCH DIAG.	001442	254
ARTMASTER	001443	569
FABRICATION	001444	569

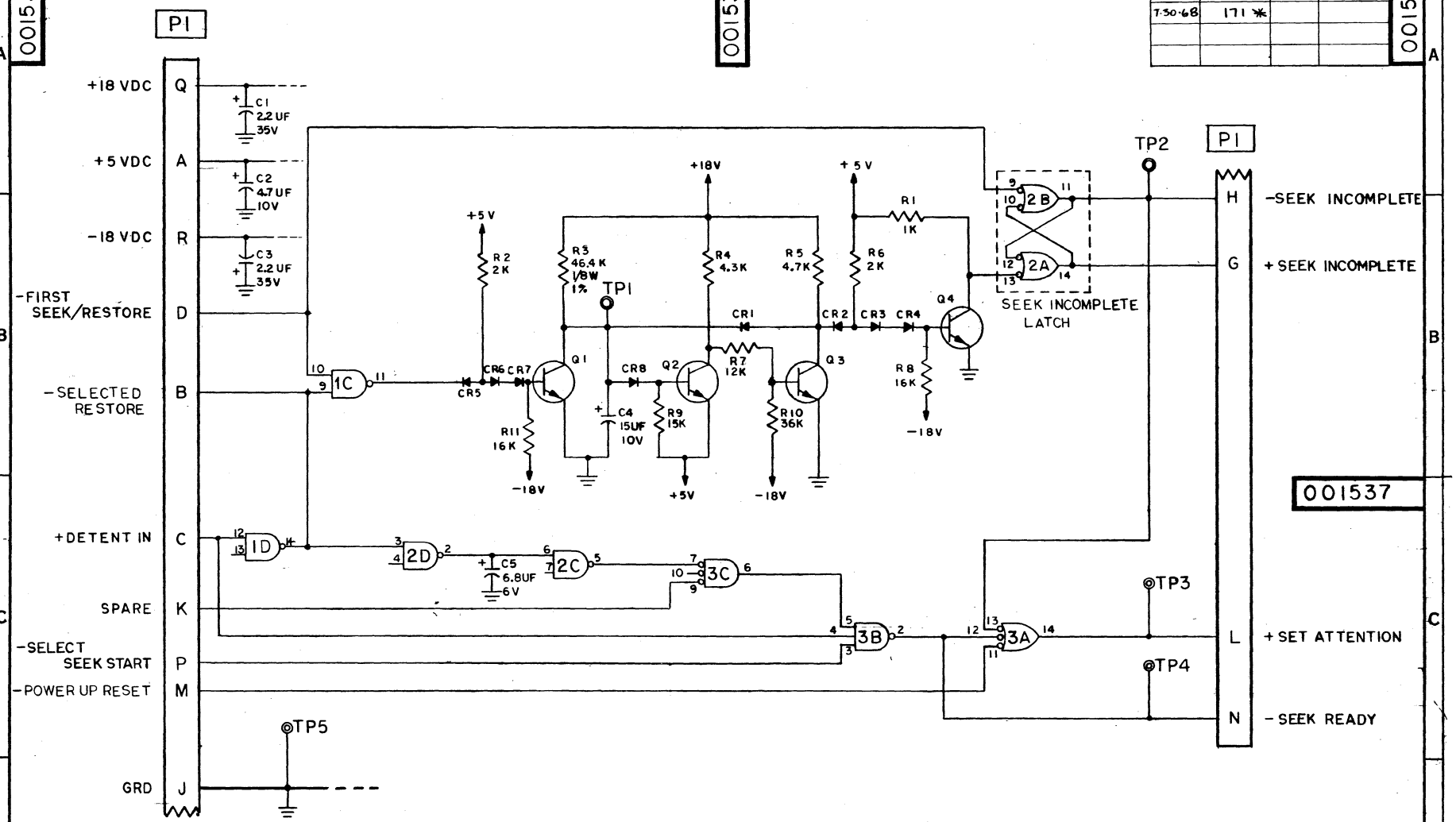
NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M NO 001441	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION
CASE DEPTH		3 PLACE DEC –	NAME P.C. BOARD ASSEMBLY
HARDNESS		ANGLES ±	A.C./D.C. SAFETY
SURFACE TREATMENT	CORNERS AND OR EDGES BROKEN	OUTSIDE MAX	DESIGN / TYPE
001441 C	RADII UNLESS OTHERWISE NOTED	INSIDE MAY	DETAIL / SCALE 2/1
			CHECK JCK 3/15/68 / DRAW HSD 1/29/68
			APPRO JCK 3/15/68 / CHECK EDE 3/15/68

001441

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001536	3MAY68	57		
	6-11-68	122		
	7-30-68	171 *		



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIODES IN4148.
2. ALL RESISTORS 1/4W, ±5%.
3. ALL TRANSISTORS 2N3568.
4. IC 1,2 ARE SP680A.
5. IC 3 IS SP670A.
6. IC'S PIN 1 IS GRD, PIN 8 IS +5VDC.

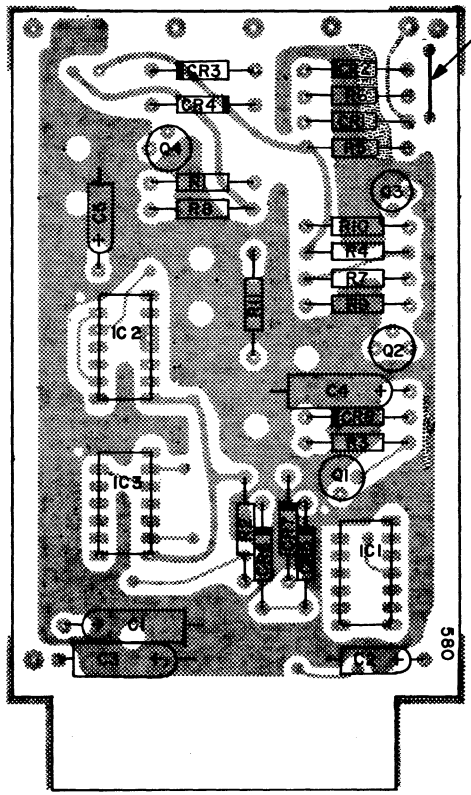
MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
CASE DEPTH			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM
HARDNESS			ANGLES ±		SEEK GATING II
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN	5/7/68 TYPE
001537	C	RADII UNLESS OTHERWISE NOTED	INSIDE MAX	DETAIL	SCALE NONE
				CHECK	5/7/68 DRAW 3MAY68
				APPRO	5/9/68 CHECK 8MAY68

001537

001536

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490-60~	6-10-68	57	12-29-69	580
200495-50~	6-11-68	122		
	7-30-68	171		
	11-19-68	219		
	9-12-69	456		

REF DESIG	DESCRIPTION	M. E. G. PART NO.
	PRINTED CIRCUIT BOARD	001539
C1, 3	CAPACITOR, T, 2.2UF, 35V, ±10%	151127
C2	T, 4.7UF, 10V, ± 10%	151124
C4	T, 15UF, 10V, ± 10%	151146
C5	CAPACITOR, T, 6.8UF, 6V, ± 10%	151126
CR1-8	DIODE, IN4148	150834
IC1, 2	INTEG. CIRCUIT, SP680A	150656
IC3	INTEG. CIRCUIT, SP670A	150655
R1,	RESISTOR, COMP, 1K, 1/4W, ±5%	151483
R2, 6	COMP 2K, 1/4W, ± 5%	151490
R3	MF, 46.4 K, 1/8W, ± 1%	153267
R4	COMP, 4.3 K, 1/4W, ± 5%	151498
R5	, 4.7 K,	151499
R7	, 12 K,	151509
R8, 11	, 16 K,	151512
R9	COMP, 15 K,	151511
R10	RESISTOR, COMP, 1/4W, ± 5%	151520
Q1-4	TRANSISTOR, 2N3568	150730
	TAG, ENGINEERING CHANGE	200304



001536

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

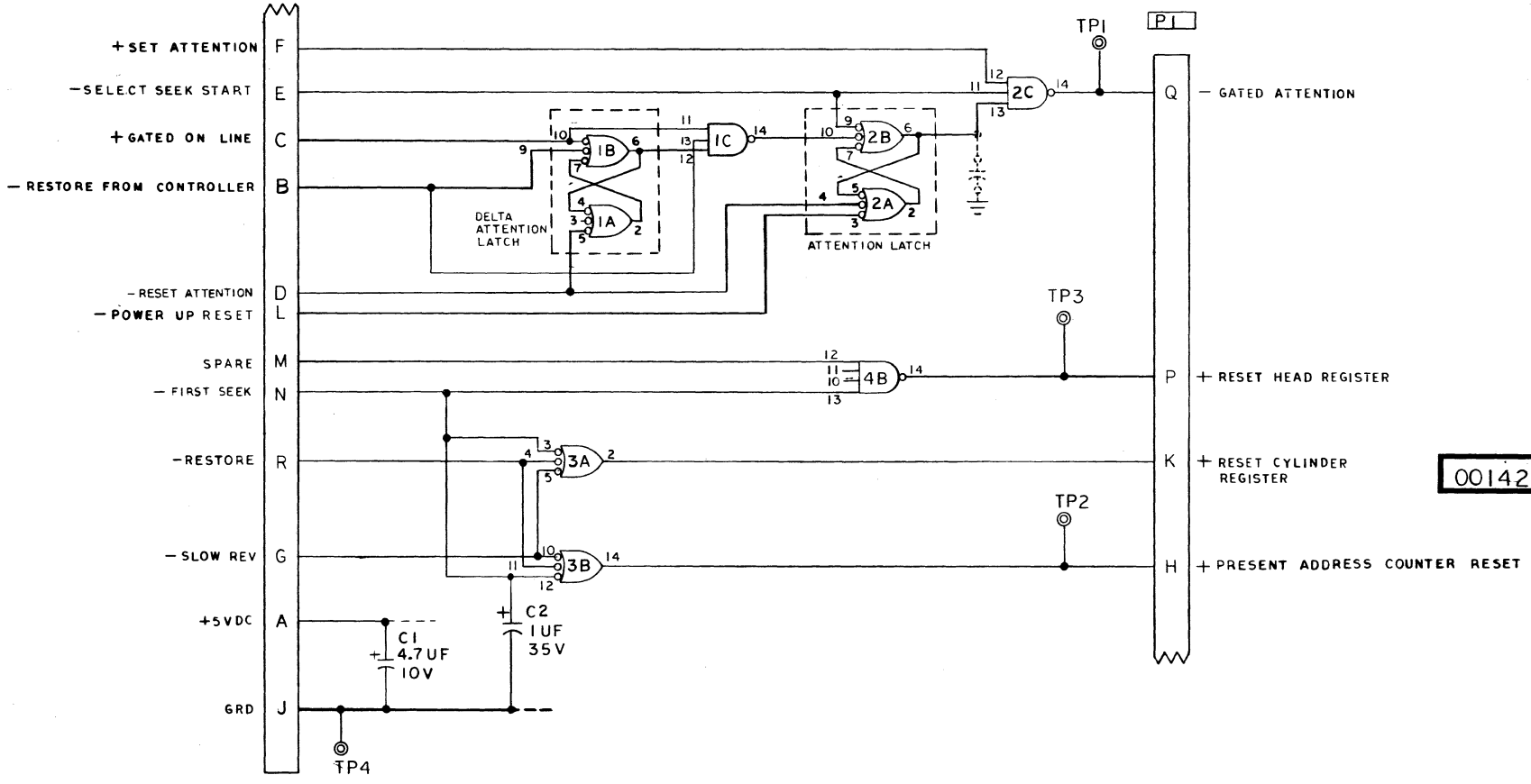
REFERENCE DOCUMENTS		E.C. LEVEL
SCH. DIAG.	001537	171
ARTMASTER	001538	580
FABRICATION	001539	580
TEST SPEC.		

MATERIAL SEE B/M NO. 001536	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION
CASE DEPTH		3 PLACE DEC ±	NAME PC. BOARD ASSEMBLY
HARDNESS		ANGLES ±	SEEK GATING II
SURFACE TREATMENT	CORNERS AND OR EDGES BROKEN	OUTSIDE MAX	DESIGN TYPE
001536 C	RADII UNLESS OTHERWISE NOTED	INSIDE MAX	DETAIL SCALE 2/1
			CHECK M.C.L. 6/11/68 DRAW K.B. 6-10-68
			APPRO KRB 6-12-68 CHECK R.L.C. 11-JUN 68

001536

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001421	2/15/68	14		
	3/20/68	34		
	7-30-68	171		
	9/12/69	435		

001422



001422

NOTES: UNLESS OTHERWISE SPECIFIED

1. CONNECT PIN 1 OF ALL IC'S TO GRD
2. CONNECT PIN 8 OF ALL IC'S TO +5VDC
3. IC 1 & 2 ARE SP670A
4. IC3 & 4 ARE SP659A

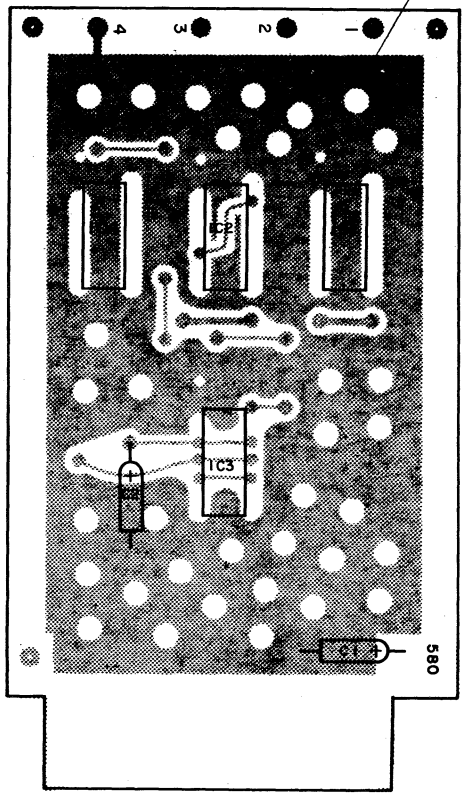
MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM
CASE DEPTH			ANGLES ±		FIRST SEEK GATING
HARDNESS			OUTSIDE MAX	DESIGN	TYPE
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	INSIDE MAX	DETAIL	SCALE NONE
001422	C	RADII UNLESS OTHERWISE NOTED		CHECK JDM 3/15/68	DRAW EGG 11/2/68
				APPRO JDK 3/18/68	CHECK 4/04/68

001422

REF DESIG	DESCRIPTION	M E G PART NO.
———	PRINTED CIRCUIT BOARD	001424
REF.	SCHEMATIC DIAGRAM	001422
C1	CAPACITOR T, 4.7 UF, 10V, ±10%	151124
C2	CAPACITOR T, 1 UF, 35V, ±10%	151116
IC1, 2	INTEGRATED CIRCUIT SP 670 A	150655
IC3, 4	INTEGRATED CIRCUIT SP 659 A	150654
———	TAG, ENGINEERING CHANGE	200304

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
630 A	200490-60~	12-11-68	14	1-2-70	580
630 B	200495-50~	3-21-68	34		
620	202032	7-30-68	171		
		11-8-68	219		
		8-8-69	435 A		

200304 [1]



001421

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001422	435
ARTMASTER	001423	580
FABRICATION	001424	580

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M	NO 001421	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001421	C	RADII UNLESS OTHERWISE NOTED	

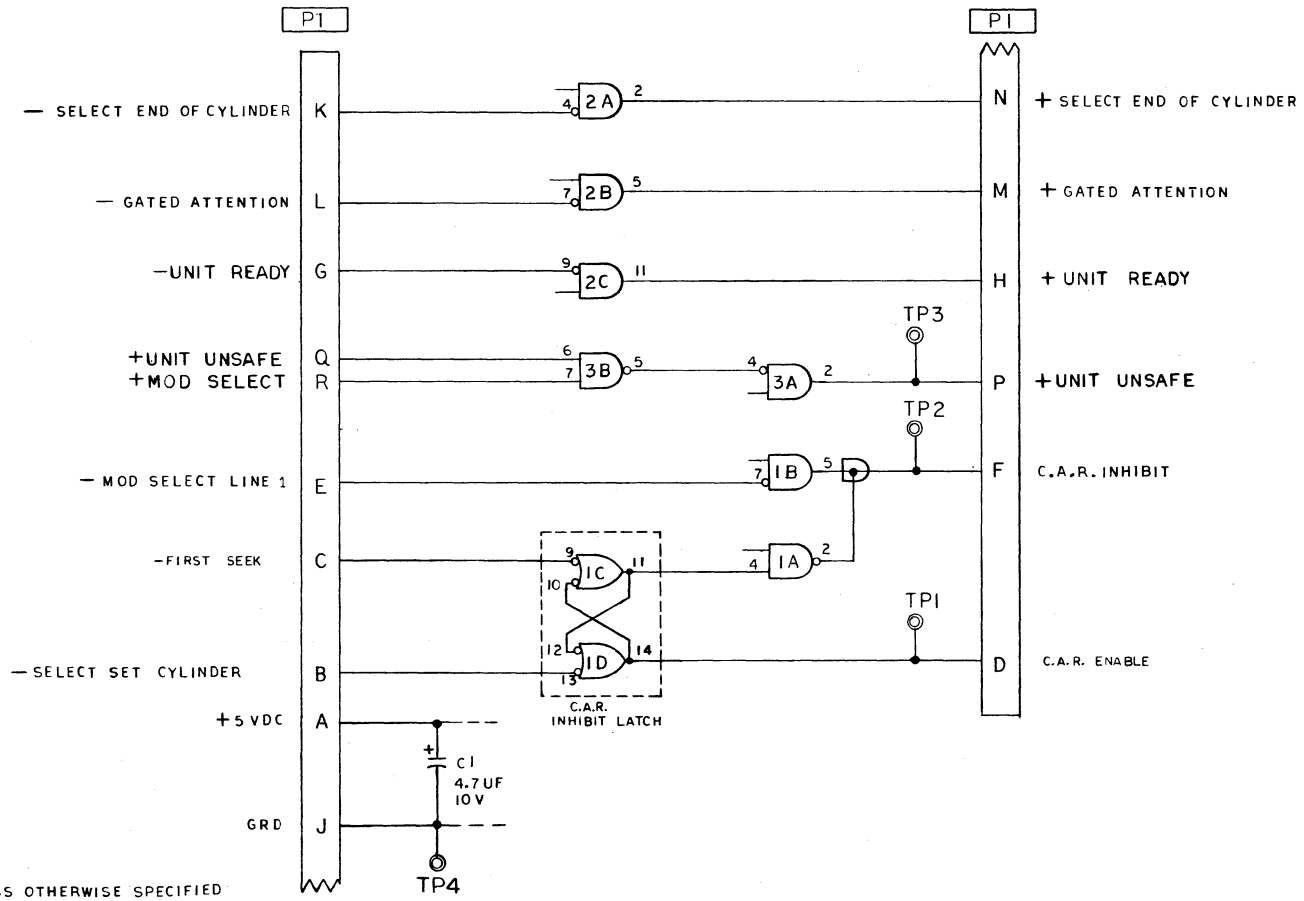
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	P.C. BOARD ASSEMBLY				
	FIRST SEEK GATING				
DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK			DRAW	[illegible]	8/11/69
APPRO	JDK WBW	18 III 68 3-27-68	CHECK	[illegible]	8/11/69

001421

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001391	2/7/68	14		
	3/21/68	34		
	7-30-68	171		

001392



001392

NOTES: UNLESS OTHERWISE SPECIFIED
1. CONNECT PIN 1 OF ALL IC'S TO GRD
2. CONNECT PIN 8 OF ALL IC'S TO +5VDC
3. IC1, 2 AND 3 ARE SP680A

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001392	C	RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

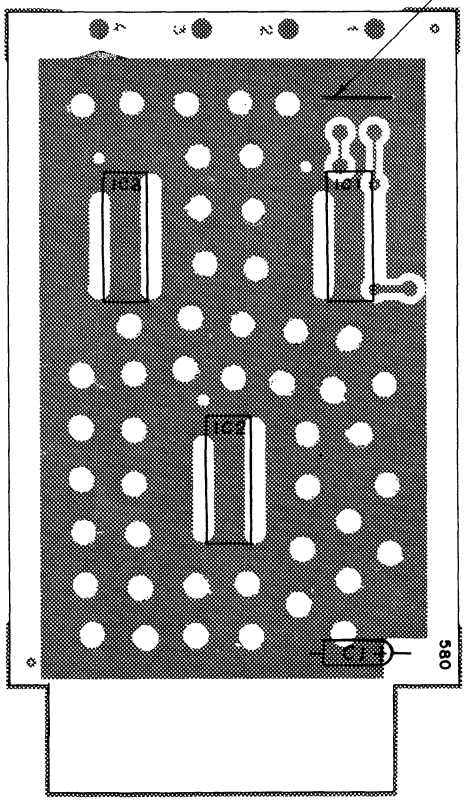
NAME	SCHEMATIC DIAGRAM C.A.R. GATING				
DESIGN	JDM	3/9/68	TYPE		
DETAIL			SCALE	NONE	
CHECK	JDM	3/7/68	DRAW	EGG	1/5/68
APPRO		3/8/68	CHECK	R.V.E.	8 MAR 68

001392

001391

REF DESIG	DESCRIPTION	P.S.C. PART NO.
–	PRINTED CIRCUIT BOARD	001394
C1	CAPACITOR-4.7 UF, 10V, ±10%	151124
IC1,2,3	INTEGRATED CIRCUITS-(SP680A)	150656
–	TAG, ENGINEERING CHANGE	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490-60~	[illegible]	14		
200495-50~	3/21/68	34		
	7-30-68	171		
	11-19-68	219		
	12-16-69	580		



001391

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001392	171
ARTMASTER	001393	580
FABRICATION	001394	580

NOTES: UNLESS OTHERWISE SPECIFIED,

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE No.
2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M	NO. 001391	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC
CASE DEPTH			ANGLES
HARDNESS			
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
001391	C		INSIDE MAX
		RADII UNLESS OTHERWISE NOTED	

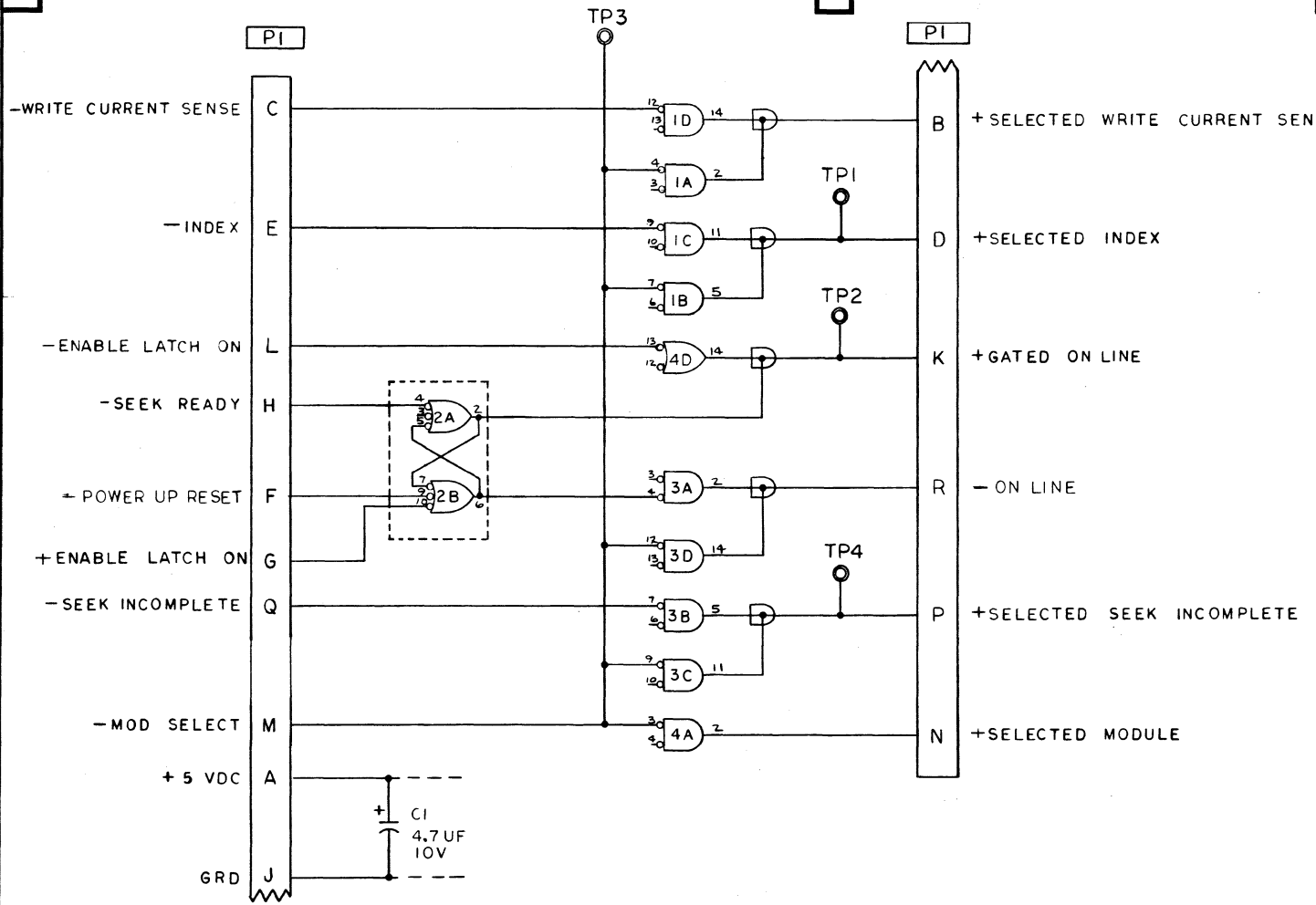
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	ASSEMBLY DRAWING				
	C.A.R. GATING				
DESIGN	[illegible]	8 MAR 68	TYPE		
DETAIL			SCALE	2/1	
CHECK	[illegible]	8 MAR 68	DRAW	MAB	1-24-68
APPRO	[illegible]	8 MAR 68 5-27-68	CHECK	R.O.S.	1-25-68

001391

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001556	4-19-68	73		
	7-30-68	171		

001557



001557

NOTES: UNLESS OTHERWISE SPECIFIED
1. IC1, 3 AND 4 ARE SP680A
2. IC2 IS SP670A
3. CONNECT PIN 1 OF ALL IC'S TO GRD
4. CONNECT PIN 8 OF ALL IC'S TO +5VDC

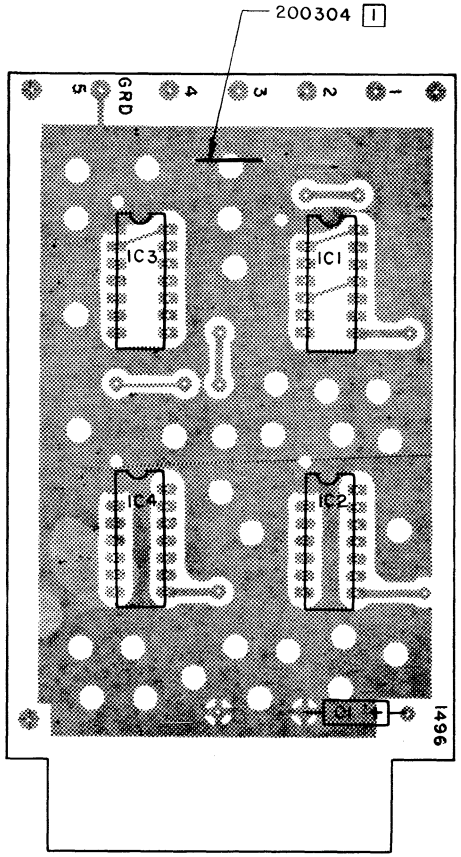
001557

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM STATUS GATING II
CASE DEPTH			ANGLES ±	DESIGN	TYPE
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DETAIL	SCALE NONE
SURFACE TREATMENT			INSIDE MAX	CHECK YCB	DRAW 1MAY68
001557	C	RADII UNLESS OTHERWISE NOTED		APPRO KRH 5/2/68	CHECK 3MAY68

DATE	CHANGE NO.	DATE	CHANGE NO.	001556
3MAY68	73	SEP70	1496	
7-30-68	171			RELEASED FOR ASSEMBLY
11-19-68	219			200490-60~
1-2-70	580			200495-50~

001556

REF DESIG	DESCRIPTION	M. E. G. PART NO.
———	PRINTED CIRCUIT BOARD	001559
C1	CAPACITOR, 4.7UF, 10V, ± 10%	151124
IC1,3,4	INTEGRATED CIRCUIT, SP680A	150656
IC2	INTEGRATED CIRCUIT, SP670A	150655
—	ENGINEERING CHANGE TAG	200304



001556

NOTES: UNLESS OTHERWISE SPECIFIED

[1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER.

2. COMPONENT HEIGHT NOT TO EXCEED .350.

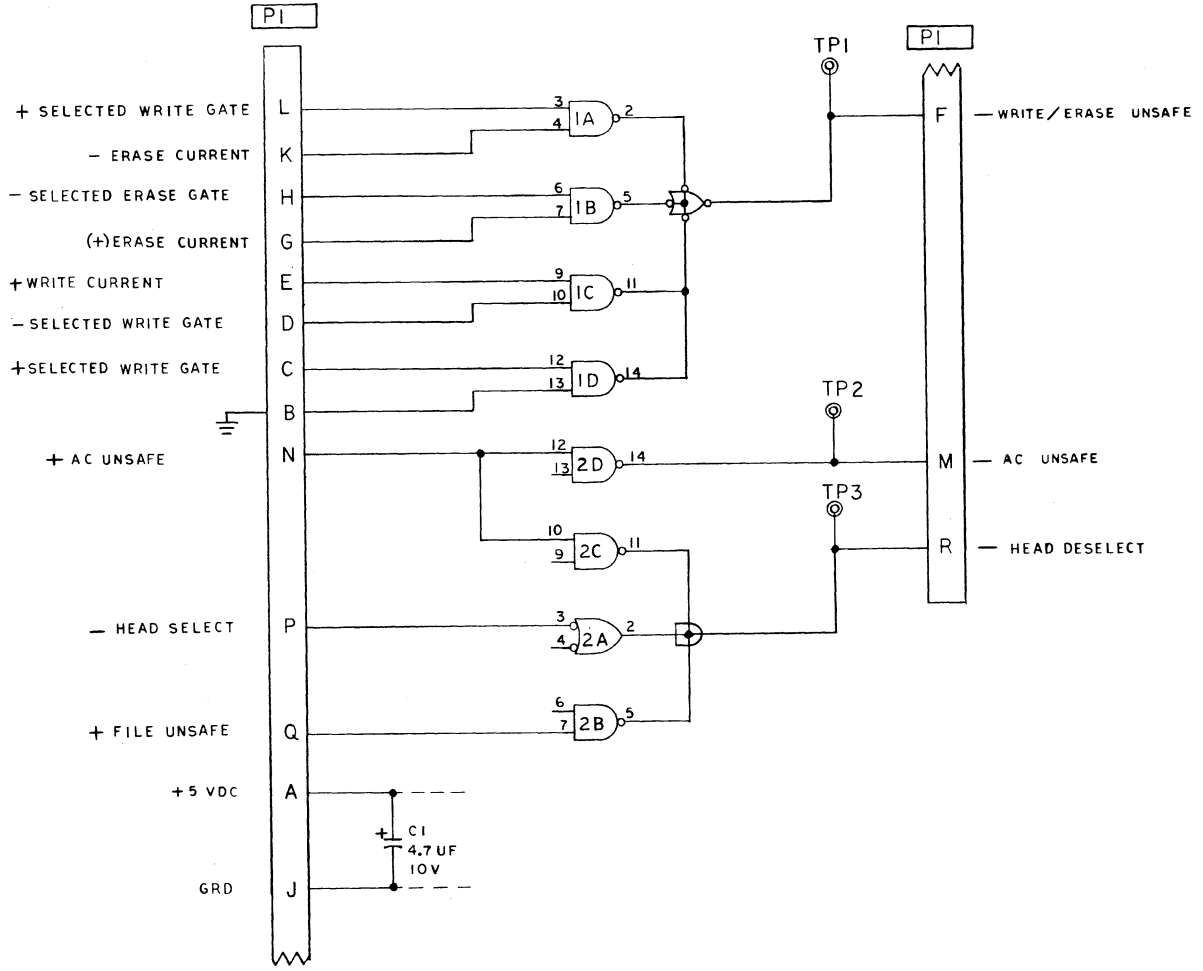
REFERENCE DOCUMENTS		E.C. LEVEL
SCH. DIAG.	001557	171
ARTMASTER	001558	1496
FABRICATION	001559	1496
TEST SPEC		

MATERIAL NO. SEE B/M NO. 001556	MUST CONFORM TO ENG. SPEC 880000	TOLERANCE UNLESS OTHERWISE NOTED	MEMOREX EQUIPMENT GROUP	
CASE DEPTH	TECHNICAL APPROVAL	LINEAR ± .XX, ± .XXX	NAME P.C. BOARD ASSEMBLY	
HARDNESS		ANGULAR ±	STATUS GATING II	
SURFACE TREATMENT NO.		CORNERS/EDGES BROKEN	DESIGN	SCALE 2/1
STD CODE C		OUTSIDE MAX	DETAIL SSK Sep70	
		INSIDE MAX	CHECK	
			APPRO M.N. 1/30 Oct 5,70 10/11/70	001556

001556

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001381	3/8/68	14		
	3/21/68	34		

001382



001382

NOTES: UNLESS OTHER SPECIFIED
1. IC1 AND 2 ARE SP680A
2. CONNECT PIN 1 OF ALL IC'S TO GRD
3. CONNECT PIN 8 OF ALL IC'S TO +5VDC

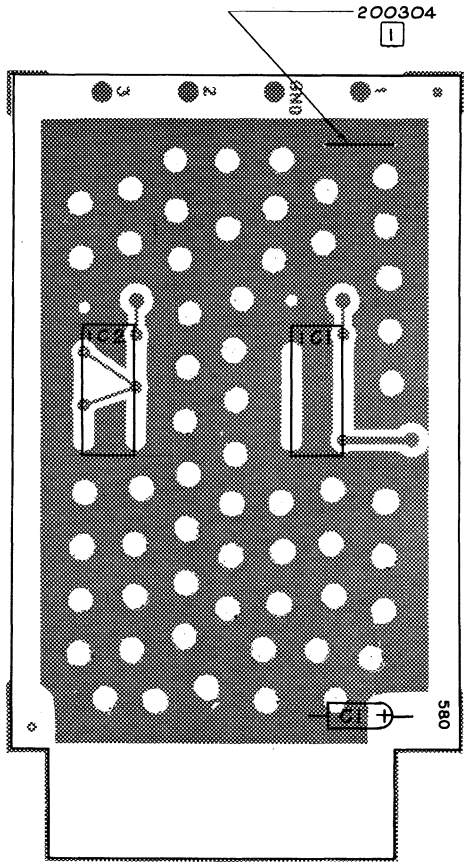
MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM WRITE/ERASE SAFETY
CASE DEPTH			ANGLES ±	DESIGN	TYPE
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DETAIL	SCALE NONE
SURFACE TREATMENT			INSIDE MAX	CHECK	DRAW EGG 12/5/67
001382	C	RADII UNLESS OTHERWISE NOTED		APPRO	CHECK

001382

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200244	8 MAR 68	14		
	3/28/67	34		
	11-19-68	219		
	12-16-69	580		

001381

REF DESIG	DESCRIPTION	P.S.C. PART NO.
—	PRINTED CIRCUIT BOARD	001384
IC1, 2	INTEGRATED CIRCUITS (SP680A)	150656
C1	CAPACITOR, 4.7 UF, 10V, ± 10%	151124
—	TAG, ENGINEERING CHANGE	200304



001381

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001382	34
ARTMASTER	001383	580
FABRICATION	001384	580

NOTES: UNLESS OTHERWISE SPECIFIED,

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE No.
2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M	NO. 001381	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001381	C	RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME ASSEMBLY DRAWING
WRITE/ERASE SAFETY

DESIGN			TYPE		
DETAIL	JDX	8 MAR 68	SCALE	2/1	
CHECK			DRAW	HAB	1-14-68
APPRO	JDX	8 MAR 68 3-27-68	CHECK	R.D.E	1-25-68

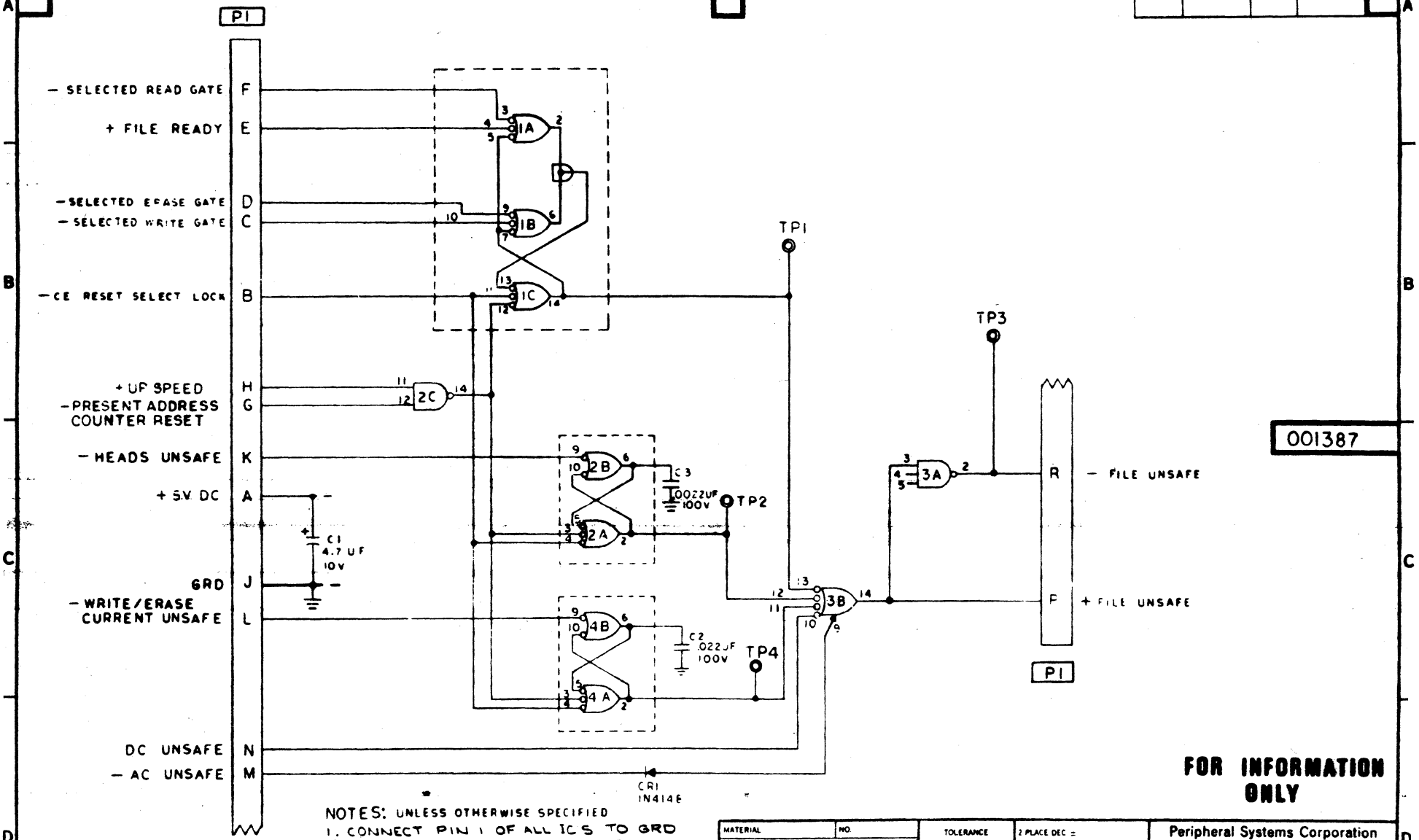
001381

001387

001387

001387

RELEASED FOR ASST	DATE	CHANGE NO.	DATE	CHANGE NO.
001386	5/14/68	14		
	7/22/68	34		
	24 JUNE	134		



NOTES: UNLESS OTHERWISE SPECIFIED
1. CONNECT PIN 1 OF ALL IC'S TO GRD
2. CONNECT PIN 8 OF ALL IC'S TO +5VDC
3. IC 1, 2 AND 4 ARE SP670A
4. IC 3 IS SP659A

FOR INFORMATION ONLY

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION
CASE DEPTH			3 PLACE DEC ±	NAME SCHEMATIC DIAGRAM
HARDNESS			ANGLES ±	CONTROL SAFETY
SURFACE TREATMENT		CORNERS AND OR EDGES BROKEN	OUTSIDE MAX	DESIGN TYPE
001387	C	RADII UNLESS OTHERWISE NOTED	INSIDE MAX	DETAIL SCALE NONE
				CHECK APPR'D

01387

2 3 4 5

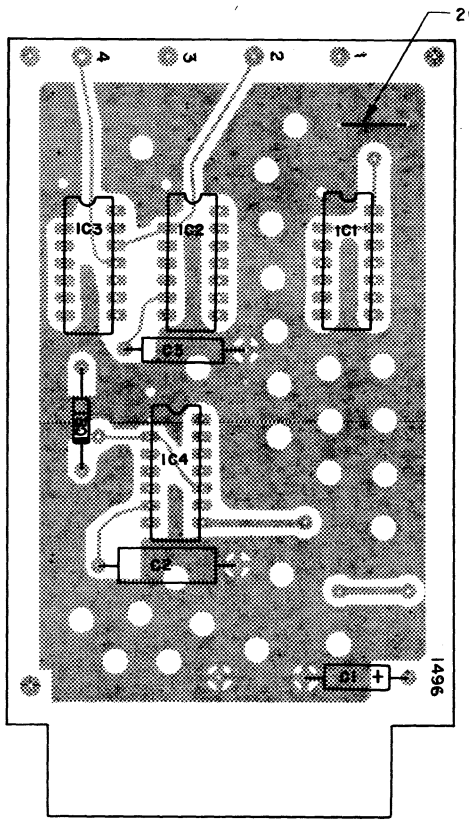
DATE	CHANGE NO.	DATE	CHANGE NO.
3-15-68	14	9-3-69	440
3-21-68	34	12-16-69	580
6-28-68	134	Sep 70	1496
11-19-68	219		

001386

RELEASED FOR ASSEMBLY
200490
200495
202032

001386

REF DESIG	DESCRIPTION	M. E. G. PART NO.
———	PRINTED CIRCUIT BOARD	001389
C1	CAPACITOR, 4.7UF, 10V, ±10%	151124
C2	CAPACITOR, .022UF, 100V, ±10%	151067
C3	CAPACITOR, .0022UF, 100V, ±10%	151054
CR1	DIODE, IN4148	150834
IC1, 2, 4	INTEGRATED CIRCUIT, SP670A	150655
IC3	INTEGRATED CIRCUIT, SP659A	150654
———	TAG, ENGINEERING CHANGE	200304



001386

NOTES: UNLESS OTHERWISE SPECIFIED

[1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER.

2. COMPONENT HEIGHT NOT TO EXCEED .350.

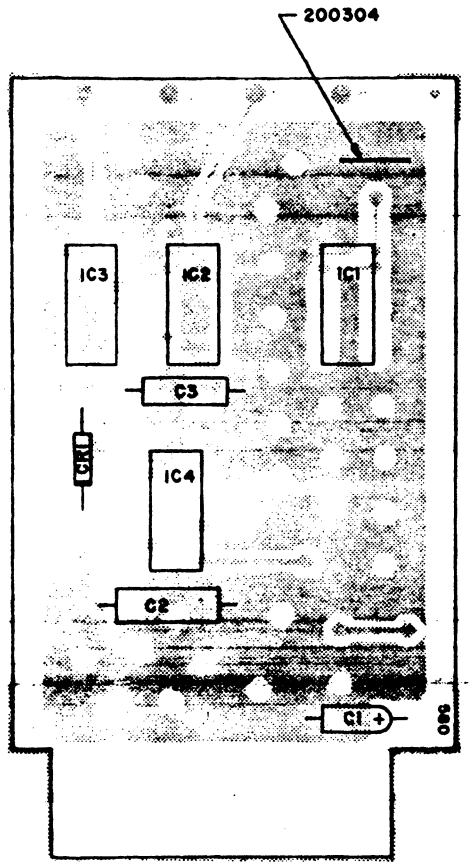
REFERENCE DOCUMENTS		E.C. LEVEL
SCH. DIAG.	001387	134
ARTMASTER	001388	1496
FABRICATION	001389	1496
TEST SPEC		

MATERIAL NO. SEE B/M NO. 001386	MUST CONFORM TO ENG. SPEC 880000	TOLERANCE UNLESS OTHERWISE NOTED	MEMOREX EQUIPMENT GROUP
CASE DEPTH	TECHNICAL APPROVAL	LINEAR ± .XX / ± .XXX	NAME P.C. BOARD ASSEMBLY CONTROL SAFETY
HARDNESS		ANGULAR ±	DESIGN / SCALE 2/1
SURFACE TREATMENT NO.		CORNERS/EDGES BROKEN	DETAIL
STD CODE C		OUTSIDE MAX / INSIDE MAX	CHECK / APPRO M.H. REG. OCT 5,70 10/16/70

001386

REF DESIG	DESCRIPTION	P.S.C. PART NO.
———	PRINTED CIRCUIT BOARD	
C1	CAPACITOR, 4.7UF 10V ±10%	151124
C2	CAPACITOR, .022UF, 50V ±10%	151067
C3	CAPACITOR, .0022UF 50V ±10%	151054
CR1	DIODE, IN4148	150834
IC1,2,4	INTEG. CIRCUIT, SP670A	150655
IC3	INTEG. CIRCUIT, SP659A	150654
———	TAG, ENGINEERING CHG	200304

USED ON	REPLACED BY ASSY	DATE	CHANGE NO	DATE	CHANGE NO
630A	200490	3-19-68	14	12-16-68	580
630B	200495	3-21-68	34		
620	202032	6-28-68	134		
		11-19-68	219		
		9-369	440		



REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001387	134
ARTMASTER	001388	580
FABRICATION	001389	580

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

SEE B/M 001386

001386 C

Peripheral Systems Corporation

P.C. BOARD ASSEMBLY
CONTROL SAFETY

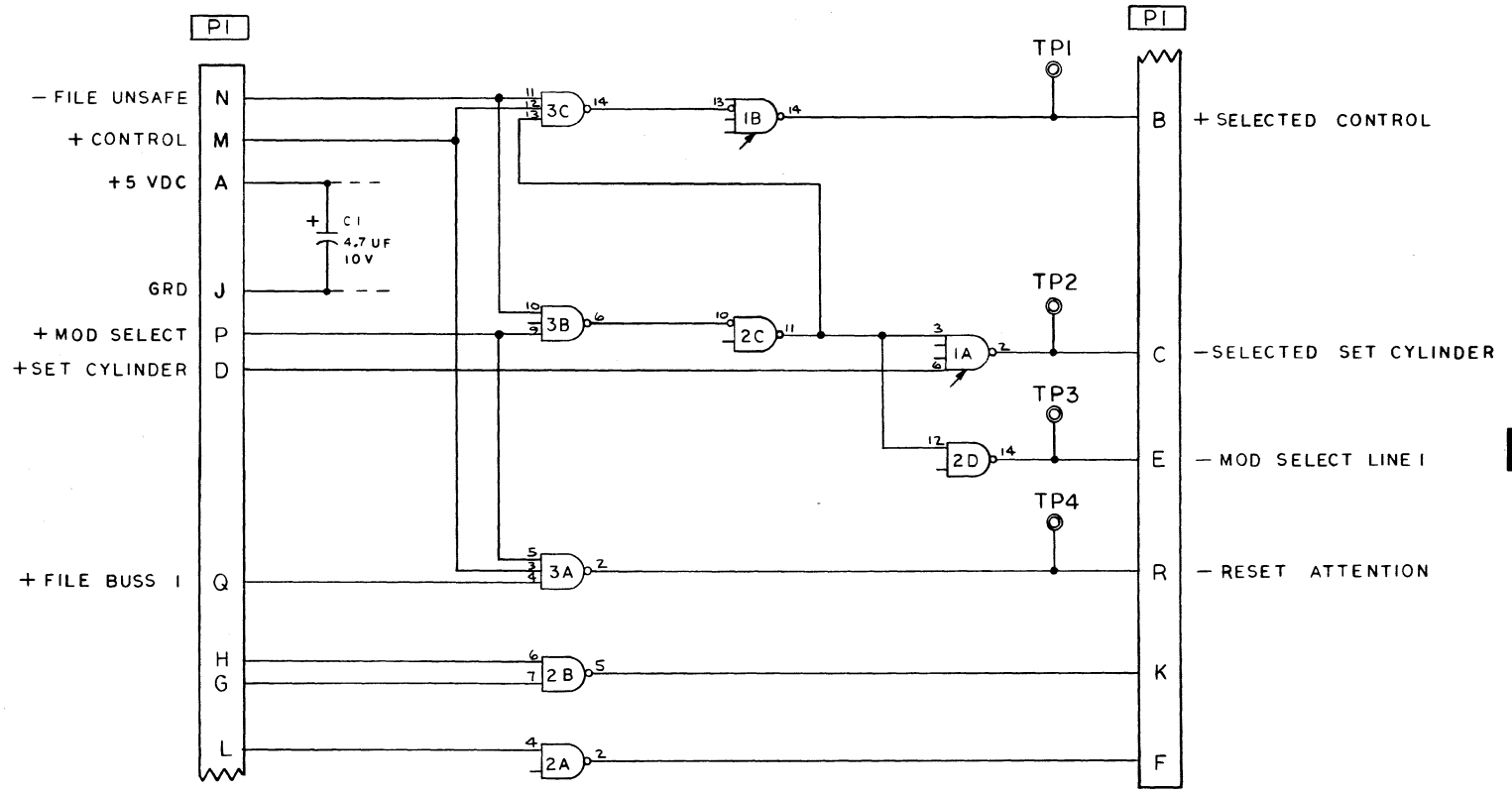
SCALE 2/1

K.B 6-28-68

001386

001386

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001411	3/8/68	14		
	3/21/68	34		



001412

NOTES: UNLESS OTHERWISE SPECIFIED
1. CONNECT PIN 1 OF ALL IC'S TO GRD
2. CONNECT PIN 8 OF ALL IC'S TO +5 VDC
3. IC1 IS SP659A
4. IC2 IS SP680A
5. IC3 IS SP670A

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001412	C	RADII UNLESS OTHERWISE NOTED	

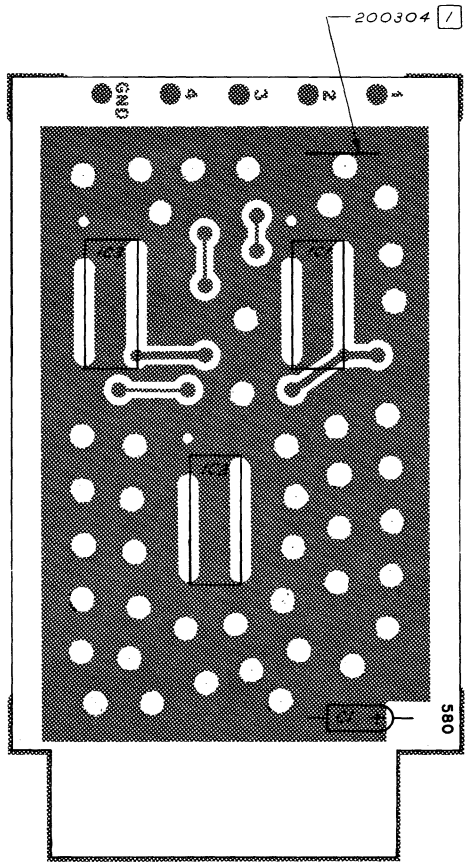
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	SCHEMATIC DIAGRAM				
	SELECT GATING				
DESIGN	JDX	8 Mar 68	TYPE		
DETAIL			SCALE	NONE	
CHECK	Jan	3/8/68	DRAW	R.V.F.	6JAN68
APPRO	JDX	8 Mar 68	CHECK	R.V.F.	8MAR68

001412

REF DESIG	DESCRIPTION	P.S.C. PART NO.
—	PRINTED CIRCUIT BOARD	001414
C1	CAPACITOR, 4.7 UF, 10V, ±10%	151124
IC1	INTEGRATED CIRCUIT (SP659A)	150654
IC2	INTEGRATED CIRCUIT (SP680A)	150656
IC3	INTEGRATED CIRCUIT (SP670A)	150655
—	ENG. CHANGE TAG.	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200244	8MAR68	14		
	3/21/68	34		
	11-19-68	219		
	1-2-70	580		



001411

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001412	34
ARTMASTER	001413	580
FABRICATION	001414	580

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (NO. 200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NO.
2. COMPONENT HEIGHT NOT TO EXCEED .350

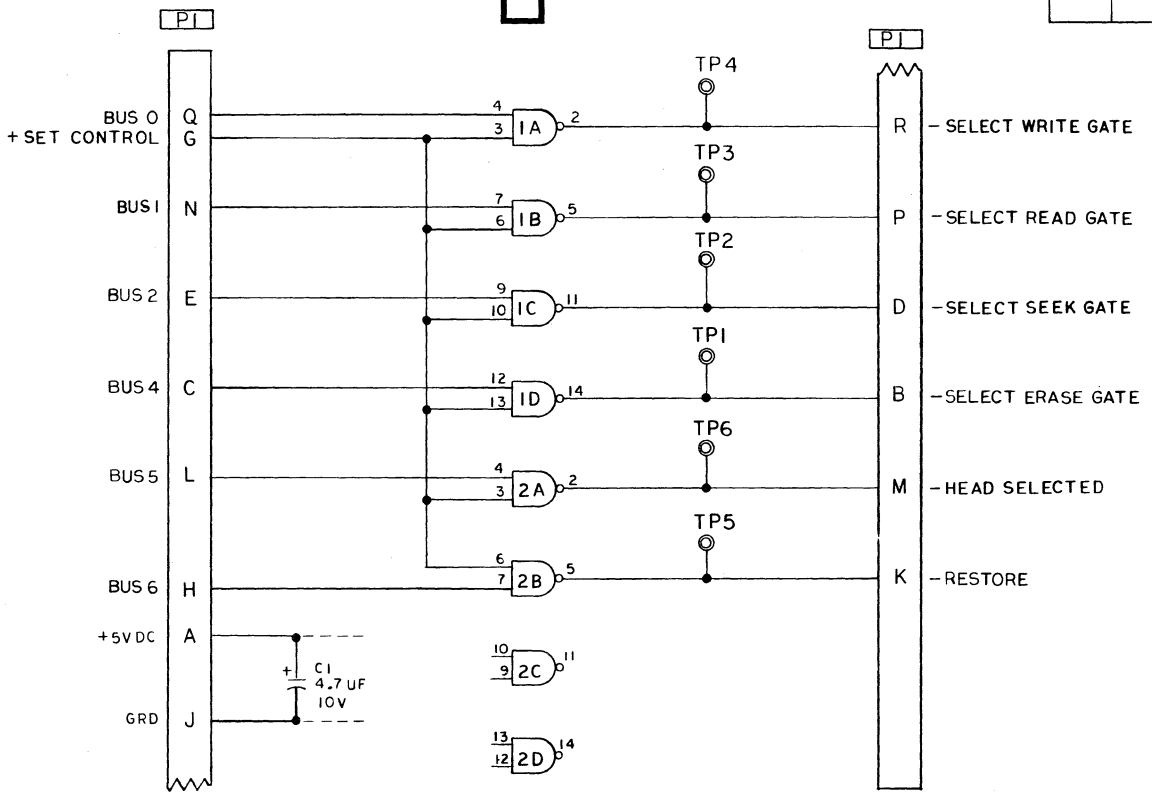
MATERIAL SEE B/M	NO. 001411	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC
CASE DEPTH			ANGLES
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001411	C	RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	ASSEMBLY DRAWING				
	SELECT GATING				
DESIGN	WGR	8 MAR 68	TYPE		
DETAIL			SCALE	2/1	
CHECK	WGR	1-29-68	DRAW	FCM	1-27-68
APPRO	WGR	8 MAR 68 3-27-68	CHECK	R.D.E.	1-29-68

001411

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001401	2/15/68	14		
	3/21/68	34		



001402

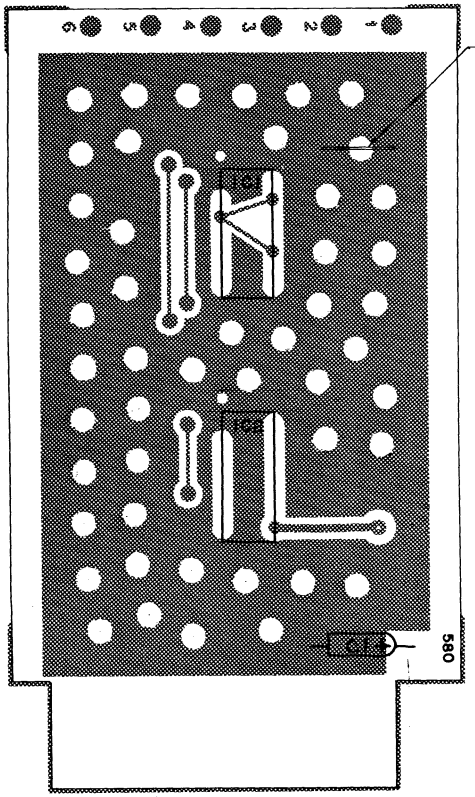
NOTES: UNLESS OTHERWISE SPECIFIED
1 IC1 & 2 ARE SP680A
2 CONNECT PIN 1 OF ALL ICS TO GRD
3 CONNECT PIN 8 OF ALL ICS TO +5VDC

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM
CASE DEPTH			ANGLES ±		CONTROL GATING
HARDNESS			CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN / TYPE
SURFACE TREATMENT				INSIDE MAX	DETAIL / SCALE NONE
001402	C	RADII UNLESS OTHERWISE NOTED			CHECK / DRAW EGG 1/16/68
					APPRO / CHECK K.W.E. 13 MAR 68

001402

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200244	12MAR68	14		
	3/2/68	34		
	11-18-68	219		
	1-2-70	580		

REF DESIG	DESCRIPTION	P.S.C. PART NO.
—	PRINTED CIRCUIT BOARD	001404
C1	CAPACITOR- 4.7UF, 10V, ±10%	151124
IC1,2	INTEGRATED CIRCUITS SP680A	150656
—	ENGINEERING CHANGE TAG	200304



001401

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001402	34
ARTMASTER	001403	580
FABRICATION	001404	580

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (NO. 200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NO.
2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M	NO. 001401	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001401	C	RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

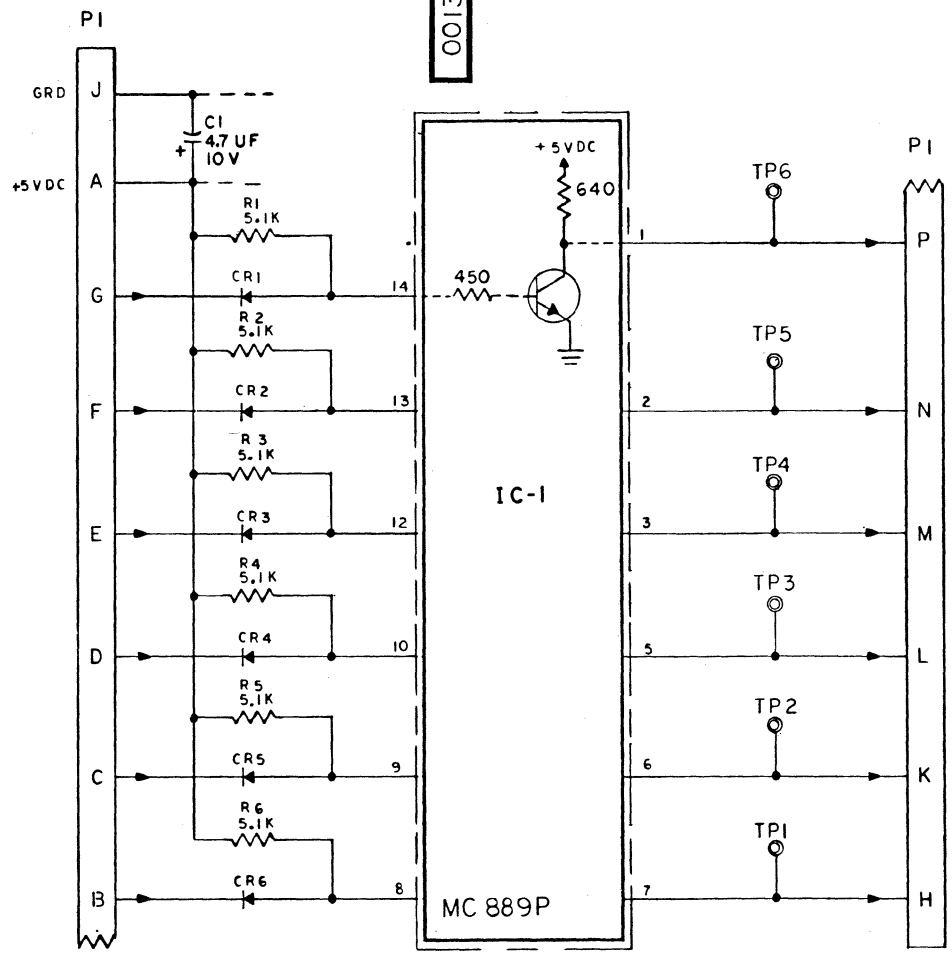
NAME ASSEMBLY DRAWING
CONTROL GATING

DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK	JDK	13 MAR 68	DRAW	HAB	1-25-68
APPRO	JDK W/W	13 MAR 68 3-27-68	CHECK	R.V.S	1-25-68

001401

001352

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001351	3/15/68	14		
	3-21-68	34		
	SEPT, 72	1244		



001352

NOTES: UNLESS OTHERWISE SPECIFIED
1. GRD ON IC1 IS ON PIN 4
2. +5VDC ON IC1 IS ON PIN 11
3. ALL DIODES ARE IN4148
4. ALL RESISTORS IN OHMS, 1/4W, ±5%

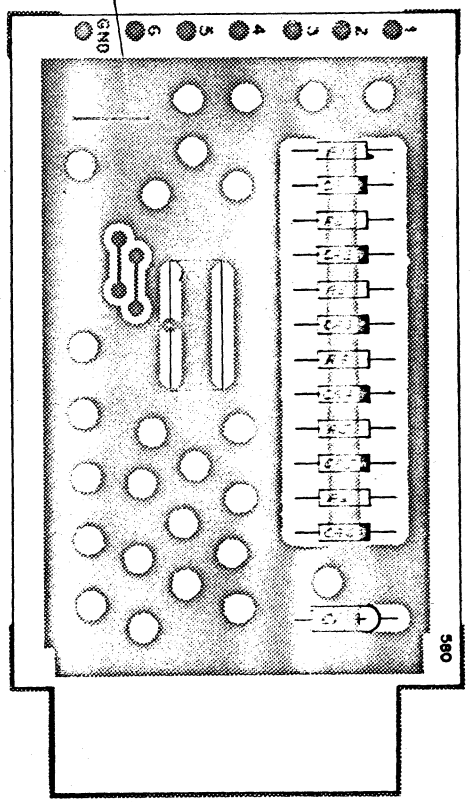
MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM LINE RECEIVER
CASE DEPTH			ANGLES ±	DESIGN	TYPE
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DETAIL	SCALE NONE
SURFACE TREATMENT			INSIDE MAX	CHECK	DRAW
001352	C	RADII UNLESS OTHERWISE NOTED		APPRO	CHECK

001352

REF DESIG	DESCRIPTION	P.S.C. PART NO.
———	PRINTED CIRCUIT BOARD	001354
C1	CAPACITOR, 4.7 UF, 10V, ±10%	151124
CR1-CR6	DIODE, (IN4148)	150834
IC1	INTEGRATED CIRCUIT (MC889P)	150659
R1-R6	RESISTOR, 5.1K, 1/4W ±5%	151500
———	ENG. CHANGE TAG	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200244	18MAR66	14		
	3/21/68	34		
	11-19-68	219		
	12-16-69	580		
	SEPT. 7.	1244		

200304 [1]



001351

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001352	1244
ARTMASTER	001353	580
FABRICATION	001354	580

NOTES: UNLESS OTHERWISE SPECIFIED

[1] ENGINEERING CHANGE TAG (NO. 200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NO.

2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M	NO. 001351	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001351	C	RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

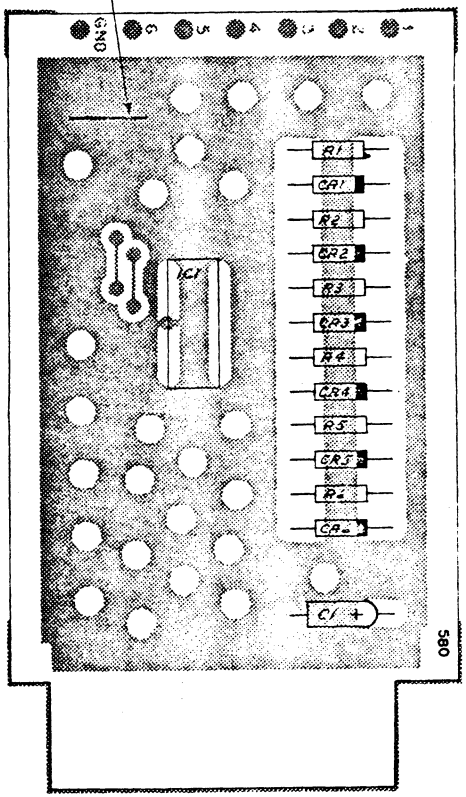
NAME	ASSEMBLY DRAWING LINE RECEIVER			
DESIGN			TYPE	
DETAIL			SCALE	2/1
CHECK	JOX	18 MAR 66	DRAW	TCM 1-25-68
APPRO	JDX (4/W)	8 MAR 68 3-27-68	CHECK	K.J.E 1-26-68

001351

REF DESIG	DESCRIPTION	P.S.C. PART NO.
———	PRINTED CIRCUIT BOARD	001354
C1	CAPACITOR, 4.7 UF, 10V, ±10%	151124
CR1-CR6	DIODE, (IN4148)	150834
IC1	INTEGRATED CIRCUIT (MC789P)	150659
R1-R6	RESISTOR, 5.1K, 1/4W ±5%	151500
———	ENG. CHANGE TAG	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200244	[illegible]	14		
	[illegible]	34		
	11-19-68	219		
	12-16-69	580		

200304 [1]



001351

REFERENCE	DOCUMENTS	EC LEVEL
SCH. DIAG.	001352	
ARTMASTER	001353	
FABRICATION	001354	

NOTES: UNLESS OTHERWISE SPECIFIED

[1] ENGINEERING CHANGE TAG (NO. 200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NO.

2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M	NO. 001351	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC
CASE DEPTH			ANGLES
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001351	C	RADII UNLESS OTHERWISE NOTED	

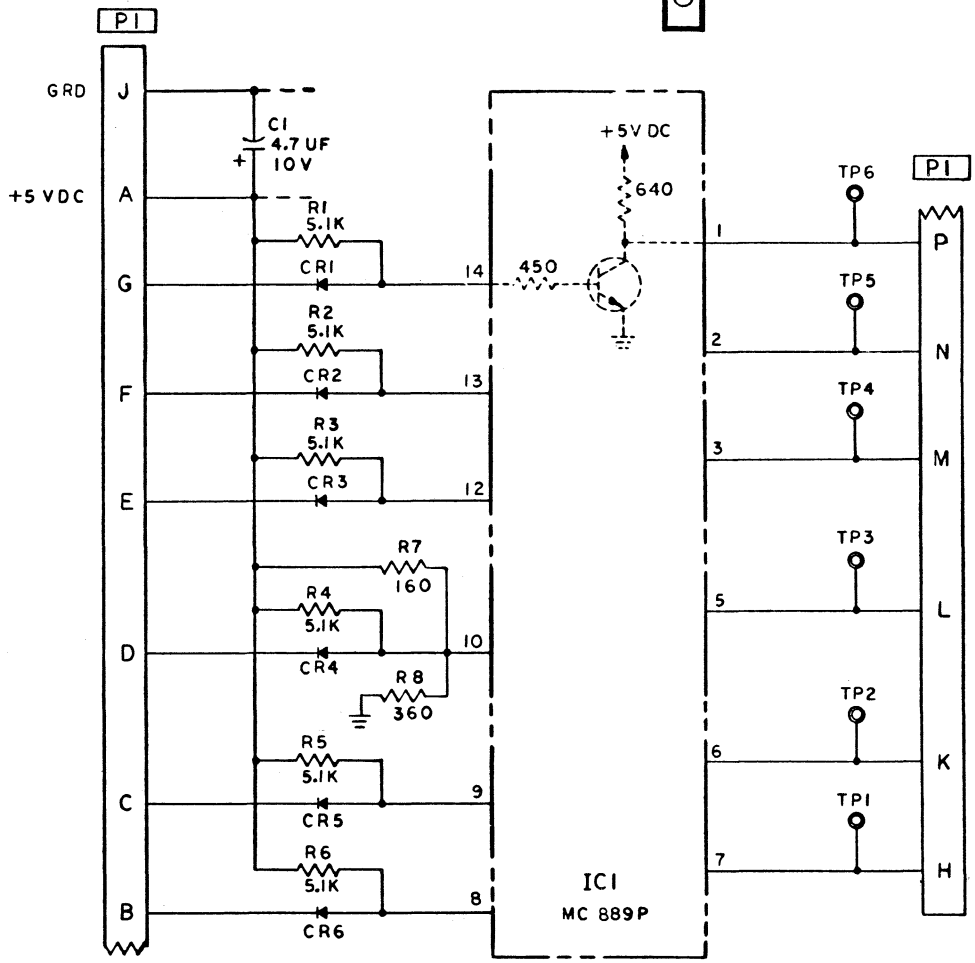
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	ASSEMBLY DRAWING LINE RECEIVER			
DESIGN		TYPE		
DETAIL		SCALE	2/1	
CHECK	[illegible]	DRAW	TCM	[illegible]
APPRO	[illegible]	CHECK	[illegible]	[illegible]

001351

001507

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001506	2/18/64	14		
	3/21/68	34		
	SEPT. 72	1244		



001507

NOTES: UNLESS OTHERWISE SPECIFIED

1. CONNECT PIN 4 OF IC1 TO GRD
2. CONNECT PIN 11 OF IC1 TO +5V DC
3. ALL RESISTORS ARE IN OHMS, 1/4W, ±5%
4. ALL DIODES ARE IN4148

MATERIAL	NO
CASE DEPTH	
HARDNESS	
SURFACE TREATMENT	

001507 C

TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
	3 PLACE DEC ±
	ANGLES ±
CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
	INSIDE MAX
RADII UNLESS OTHERWISE NOTED	

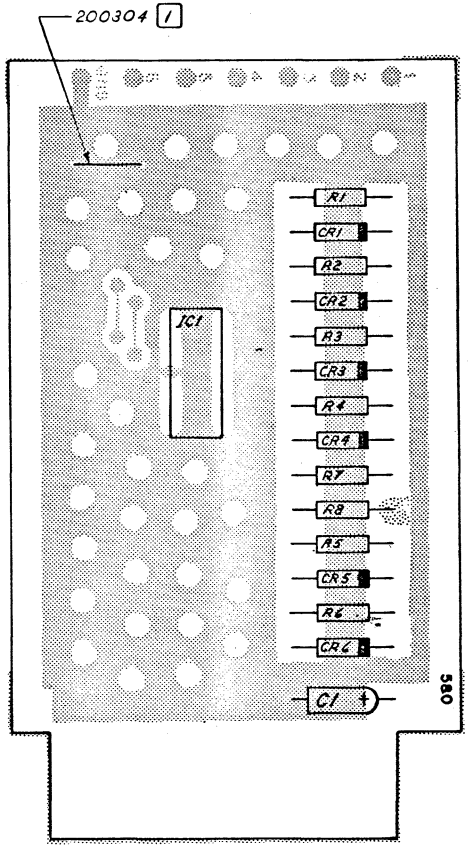
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	SCHEMATIC DIAGRAM				
TERMINATED LINE RECEIVER					
DESIGN			TYPE		
DETAIL			SCALE	NONE	
CHECK	[illegible]	3/18/68	DRAW	[illegible]	2-3-68
APPRO	[illegible]	[illegible]	CHECK	[illegible]	[illegible]

001507

REF DESIG	DESCRIPTION	P.S.C. PART NO.
—	PRINTED CIRCUIT BOARD	001509
C1	CAPACITOR, 4.7 UF, 10V, ± 10%	151124
CR1-CR6	DIODES (IN4148)	150834
IC1	INTEGRATED CIRCUIT (MC339P)	150659
R1-R6	RESISTORS, 5.1K, 1/4W, ± 5%	151500
R7	RESISTOR, 160 Ω, 1/4W, ± 5%	151464
R8	RESISTOR, 360 Ω, 1/4W, ± 5%	151472
—	ENG. CHANGE TAG	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200244	1[illegible]-3	14		
	3/21/68	34		
	11-19-68	219		
	1-2-70	580		
	SEPT-[illegible]	214		



001506

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001507	1244
ARTMASTER	001508	580
FABRICATION	001509	580

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M	NO. 001506	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ± ,
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001506	C	RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

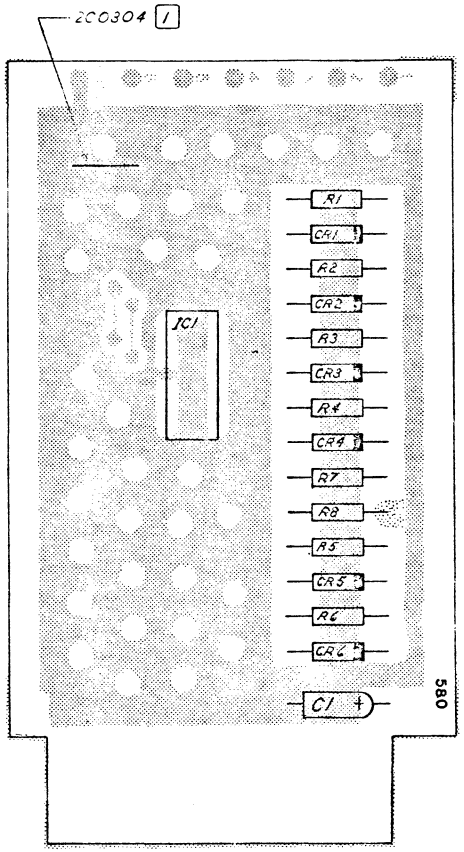
NAME	ASSEMBLY DRAWING				
TERMINATED LINE RECEIVER					
DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK	[illegible]	[illegible]	DRAW	TCM	2-15-68
APPRO	[illegible]	[illegible] 3-27-68	CHECK	[illegible]	[illegible]

001506

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200244	1-BASIC	14		
	3/21/68	34		
	11-19-68	219		
	1-2-70	580		

001506

REF DESIG	DESCRIPTION	P.S.C. PART NO.
—	PRINTED CIRCUIT BOARD	001503
C1	CAPACITOR, 4.7 UF, 10V, ±10%	151124
CR1-CR6	DIODES 1N4148	150634
IC1	INTEGRATED CIRCUIT (MC753F)	150659
R1-R6	RESISTORS, 5.1K, 1/4W, ±5%	151500
R7	RESISTOR, 150Ω, 1/4W, ±5%	151464
R8	RESISTOR, 360Ω, 1/4W, ±5%	151472
—	ENG. CHANGE TAG	200304



001506

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001507	34
ARTMASTER	001508	580
FABRICATION	001509	580

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

001506

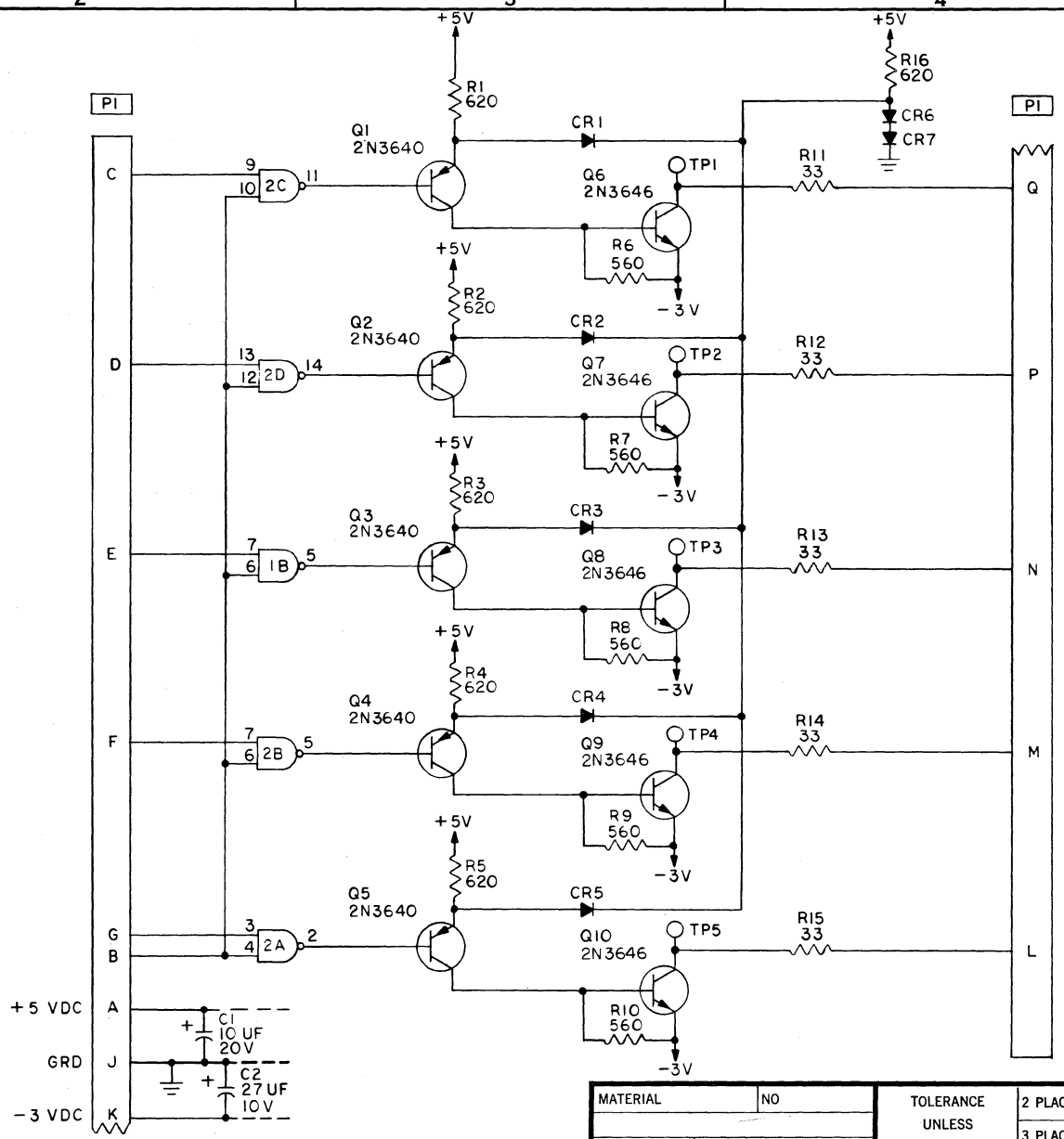
MATERIAL SEE B/M	NO. 001506	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001506	C	RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME ASSEMBLY DRAWING

TERMINATED LINE RECEIVER

DESIGN			TYPE	
DETAIL			SCALE	2/1
CHECK	[illegible]	[illegible]	DRAW	[illegible]
APPRO	[illegible]	[illegible]	CHECK	[illegible]



NOTES: UNLESS OTHERWISE SPECIFIED

1. IC1 AND IC2 ARE SP680A.
2. CONNECT PIN 1 OF ALL IC'S TO GRD.
3. CONNECT PIN 8 OF ALL IC'S TO +5VDC.
4. ALL RESISTORS ARE IN OHMS, 1/4 W, 5%.
5. ALL DIODES ARE IN4148.

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001641	8-26-68	189		

001642

MATERIAL	NO
CASE DEPTH	
HARDNESS	
SURFACE TREATMENT	

001642 C

TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
	3 PLACE DEC ±
	ANGLES ±
CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
	INSIDE MAX
RADII UNLESS OTHERWISE NOTED	

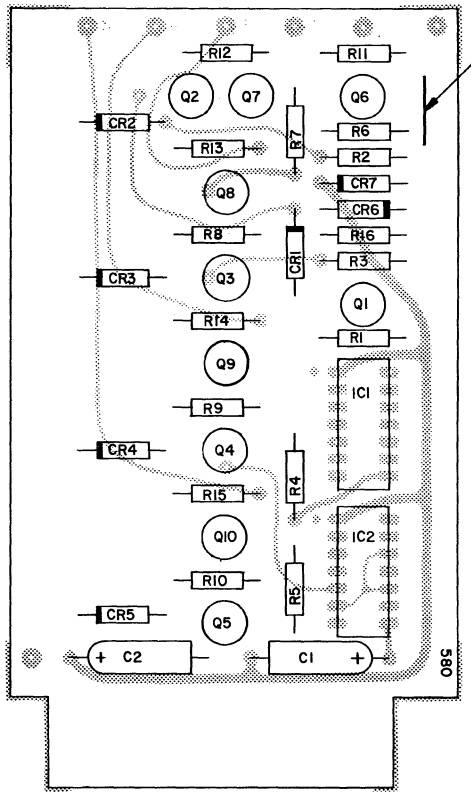
Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	SCHEMATIC DIAGRAM LINE DRIVERS II				
DESIGN			TYPE		
DETAIL			SCALE		
CHECK	JE	9-5-68	DRAW	DEH	8-26-68
APPRO	[illegible]	9/5/68 9/6/68	CHECK	DEH	9-5-68

001642

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200490-60 ~	8-29-68	189		
200495-50 ~	1-2-70	580		

REF DESIG	DESCRIPTION	P.S.C. PART NO.
———	PRINTED CIRCUIT BOARD	001644
REF	SCHEMATIC DIAGRAM	001642
C1	CAPACITOR, T, 10 UF, 20V	151132
C2	CAPACITOR, T, 27 UF, 10V	151137
CR1-7	DIODE, IN4148	150834
IC1, 2	INTEGRATED CIRCUIT, SP680A	150656
R1-5, 16	RESISTOR, 620 OHMS, 1/4W, ±5%	151478
R6-10	RESISTOR, 560 OHMS, 1/4W, ±5%	151477
R11-15	RESISTOR, 33 OHMS, 1/4W, ±5%	151447
Q1-5	TRANSISTOR, 2N3640	150732
Q6-10	TRANSISTOR, 2N3646	150734
———	TAG, ENGINEERING CHANGE	200304



001641

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001642	189
ARTMASTER	001643	580
FABRICATION	001644	580

NOTES: UNLESS OTHERWISE SPECIFIED

1. [1] ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .450

SEE B/M NO. 001641

001641 C

Peripheral Systems Corporation

P.C. BOARD ASSEMBLY

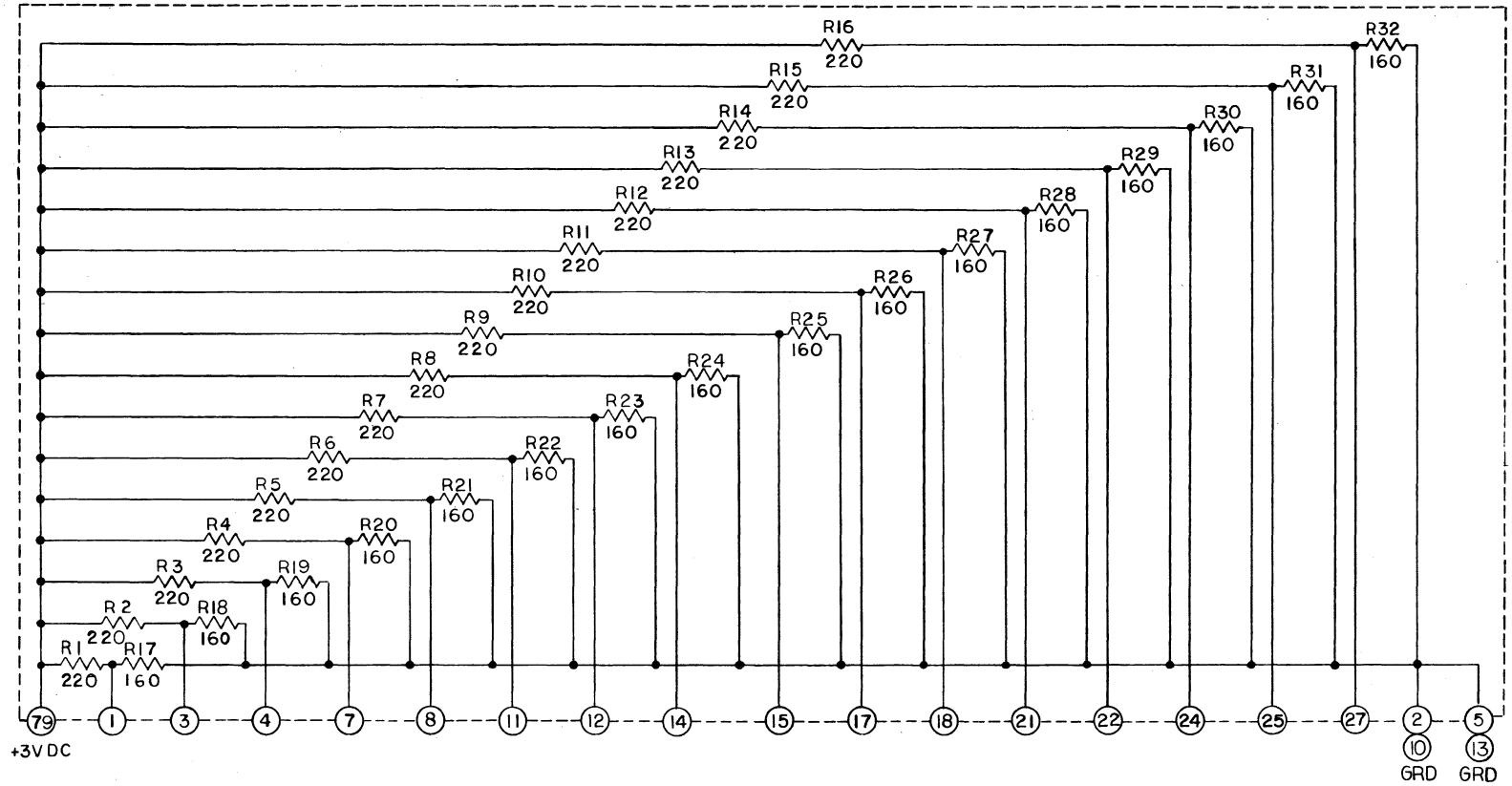
LINE DRIVERS II

DESIGN			TYPE		
DETAIL			SCALE	2/1	
CHECK	JE	9-5-68	DRAW	DRH	8-29-68
APPRO	KEJ	9-5-68	CHECK	DRH	9-5-68

001641

001517

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
001516	12 APR 68	60		



NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTORS ARE IN OHMS, 1/4W, ±5%.

MATERIAL	NO
CASE DEPTH	
HARDNESS	
SURFACE TREATMENT	

001517 C

TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	
	3 PLACE DEC ±	
	ANGLES ±	
CORNERS AND/OR EDGES BROKEN	OUTSIDE	MAX
	INSIDE	MAX
RADII UNLESS OTHERWISE NOTED		

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

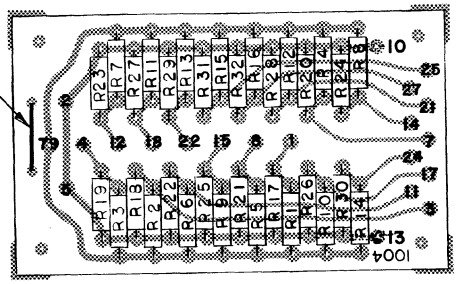
NAME	SCHEMATIC DIAGRAM			
	LINE TERMINATOR			
DESIGN			TYPE	
DETAIL			SCALE	NONE
CHECK	[illegible]	4/15/68	DRAW	TCM 4-8-68
APPRO	[illegible]	4/15/68	CHECK	[illegible] 15APR68

001517

REF DESIG	DESCRIPTION	P.S.C. PART NO.
——	PRINTED CIRCUIT BOARD	001519
R 1,2,3,4	RESISTOR,220 OHM, 1/4W,± 5%	151467
R 5,6,7, 8		
R9,10,11,12		
R13,14,15,16		
R17,18,19	RESISTOR.160 OHM, 1/4W,± 5%	151464
R 20,21,22		
R23,24,25		
R26,27,28		
R29,30,31		
R 32		
——	TAG, ENGINEERING CHANGE	200304

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
244465	12-APR-68	60		
MULTI-USE	MAY6,70	1004		

200304 [1]



001516

REFERENCE DOCUMENTS		EC LEVEL
SCH. DIAG.	001517	60
ARTMASTER	001518	1004
FABRICATION	001519	1004

NOTES: UNLESS OTHERWISE SPECIFIED

1. ENGINEERING CHANGE TAG (200304) MUST REFLECT THE LATEST ENGINEERING CHANGE NUMBER
2. COMPONENT HEIGHT NOT TO EXCEED .350

MATERIAL SEE B/M	NO. 001516	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
			3 PLACE DEC ±
CASE DEPTH			ANGLES ±
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
SURFACE TREATMENT			INSIDE MAX
001516	C	RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME	P.C. BOARD ASSEMBLY		
	LINE TERMINATOR-P.C. BRD. ASSY.		
DESIGN		TYPE	
DETAIL		SCALE	2/1
CHECK	E.G.M. 4/15/68	DRAW	R.D. 12APR68
APPRO	E.G.M. 4/15/68	CHECK	R.J.S. 15APR68

001516

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200877	2-14-68	14		
008041	7-18-68	167		
	2-13-70	604		

008017

J3 SIGNAL IN	J4 SIGNAL OUT	WIRE	PB-C27	FUNCTION
1	1	RED/BLK	A	FILE BUS Ø
2	2	RED	J	COMMON
3	3	ORG	B	FILE BUS 1
4	4	RED/GRN	C	FILE BUS 2
5	5	GRN	J	COMMON
7	7	BLU	D	FILE BUS 3
8	8	RED/WHT	E	FILE BUS 4
10	10	WHT/BLK	J	COMMON
11	11	WHT	F	FILE BUS 5
12	12	BLK	G	FILE BUS 6
13	13	BLK/WHT	J	COMMON
14	14	WHT/RED	H	FILE BUS 7
15	15	YEL		NOT USED (SET DIFFERENCE)
16	16	ORG/BLK	J	COMMON
17	17	ORG/GRN	K	SET CYLINDER (TAG LINE)
18	18	BLU/BLK	L	SET HEAD AND DIRECTION (TAG LINE)
20	20	BLU/RED	J	COMMON
21	21	BLU/WHT	M	CONTROL (TAG LINE)
22	22	GRN/WHT	N	CPU HALT (METER)
23	23	GRN/BLK	J	COMMON
24	24	BLK/RED	P	STORAGE CONTROL UNIT METERING ON
62	62	ORG/RED	Q	SELECTED SECTOR PULSE (NOT USED ON 630)
63	63	RED/WHT/BLK	J	COMMON
64	64	BLK/WHT/RED	R	SELECT WRITE CURRENT SENSE
	79	ORG	J5-13 (DC IN)	DC FOR TERMINATION PLUG (+3V FOR 630, +5V FOR 630-1 & 630-3)

008017

SHEET 1 OF 2

NOTES: SEE SHEET 2

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION
			3 PLACE DEC ±	NAME SCHEMATIC DIAGRAM
CASE DEPTH			ANGLES ±	SIGNAL IN / OUT
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN 7/8/68 TYPE
SURFACE TREATMENT			INSIDE MAX	DETAIL SCALE NONE
008017	C	RADII UNLESS OTHERWISE NOTED		CHECK DRAW R.D.E. 2-14-68
				APPRO 4-3-68 CHECK

008017

008017

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200877	2-14-68	14		
008041	7-18-68	167		
	2-13-70	604		

J3 — SIGNAL IN	J4 - SIGNAL OUT	WIRE	PB-C26	FUNCTION
40	40	RED/BLK	A	CAR 1
41	41	RED	J	COMMON
42	42	ORG	B	CAR 2
43	43	RED/GRN	C	CAR 4
44	44	GRN	J	COMMON
45	45	BLU	D	CAR 8
46	46	RED/WHT	E	CAR 16
47	47	WHT/BLK	J	COMMON
48	48	WHT	F	CAR 32
49	49	BLK	G	CAR 64
50	50	BLK/WHT	J	COMMON
51	51	WHT/RED	H	CAR 128
52	52	ORG/GRN	K	SELECTED DRIVE READY
53	53	ORG/BLK	J	COMMON
54	54	BLU/BLK	L	SELECTED DRIVE ON LINE
55	55	BLU/WHT	M	SELECT INDEX
56	56	BLU/RED	J	COMMON
57	57	GRN/WHT	N	SELECTED FILE UNSAFE
58	58	BLK/RED	P	SELECTED SEEK INCOMPLETE
59	59	GRN/BLK	J	COMMON
60	60	ORG/RED	Q	SELECTED DRIVE END OF CYLINDER
67		RED/WHT/BLK	J	SPARE
	67	BLK/WHT/RED	R	SELECTED READ ONLY

008017

SHEET 2 OF 2

NOTES: UNLESS OTHERWISE SPECIFIED—

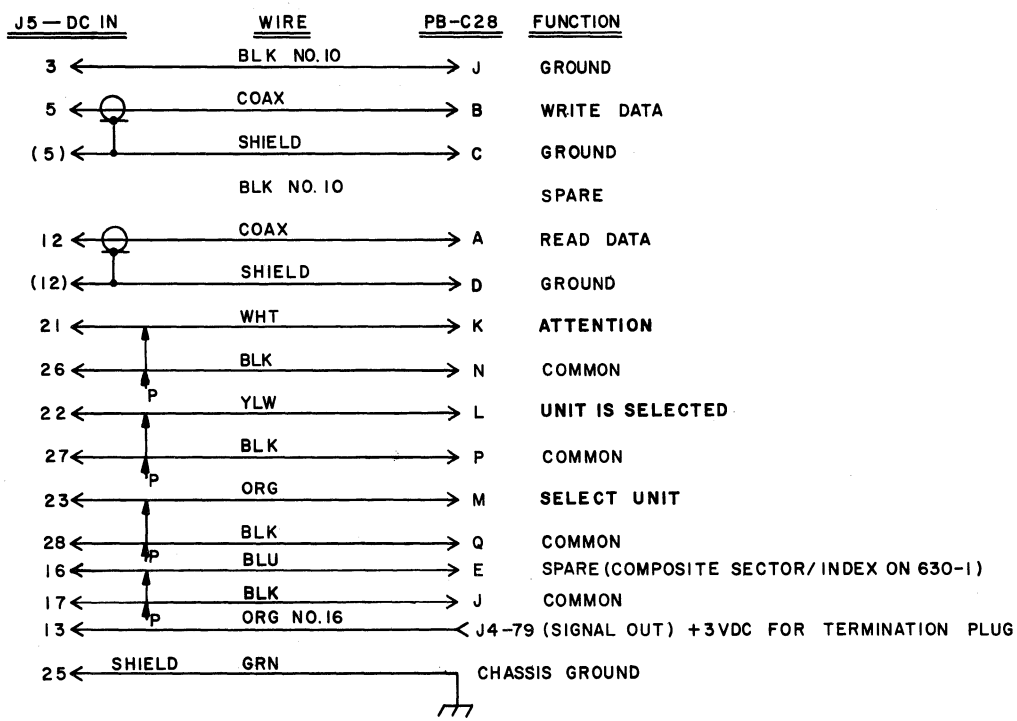
1. PINS 70 THRU 75 AND PINS 25 THRU 39 ARE SPARES.
2. FOR CIRCUITRY ASSOCIATED WITH PINS 65,66,76,77,78 80 AND 82 SEE DRAWING 008021
3. PINS 6, 9, 19, 61, 68, 69 AND 81 ARE NON-EXISTENT

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION
CASE DEPTH			3 PLACE DEC ±	NAME: SCHEMATIC DIAGRAM
HARDNESS			ANGLES ±	SIGNAL IN/OUT
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN: ESH 2/15/69 TYPE:
008017	C		INSIDE MAX	DETAIL: SCALE: NONE
		RADII UNLESS OTHERWISE NOTED		CHECK: DRAW: RVF 2-14-68
				APPRO: ESH 2-26 CHECK:

008017

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200101	2-15-68	14		
	19APR68	59		
	7-18-68	167		
	2-8-69	257		

008018



008018

NOTES: UNLESS OTHERWISE SPECIFIED —

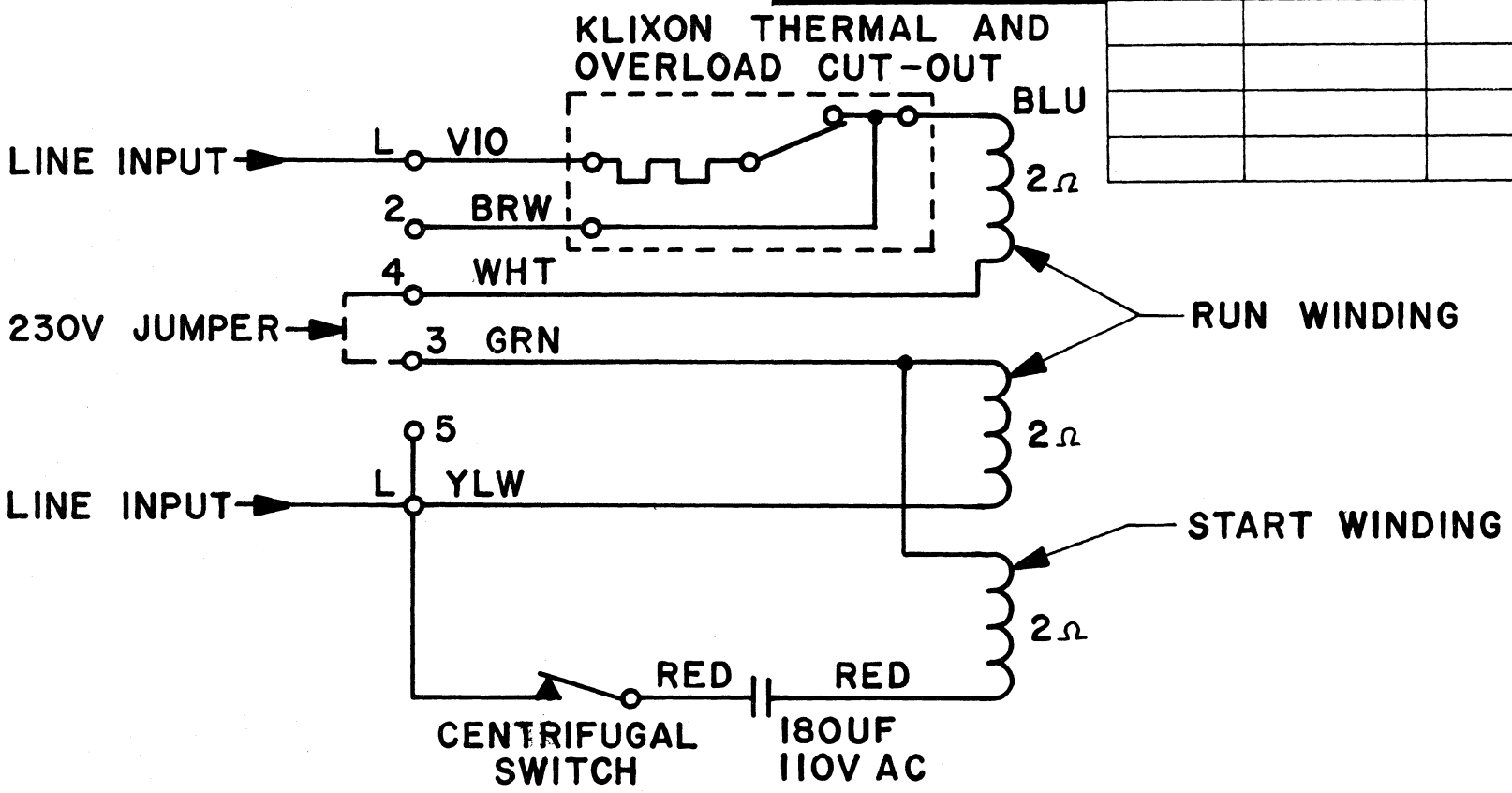
1. ALL OTHER PINS IN J5 ARE NOT USED, INCLUDING PIN G.

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION
			3 PLACE DEC ±	
CASE DEPTH			ANGLES ±	NAME SCHEMATIC DIAGRAM
HARDNESS				DC INPUT
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN EGM 3/1/68 TYPE
008018	C		INSIDE MAX	DETAIL SCALE
		RADII UNLESS OTHERWISE NOTED		CHECK DRAW RDS 2-15-68
				APPRO EGM 4-3-68 CHECK

008018

	2-15-68	14		

00802

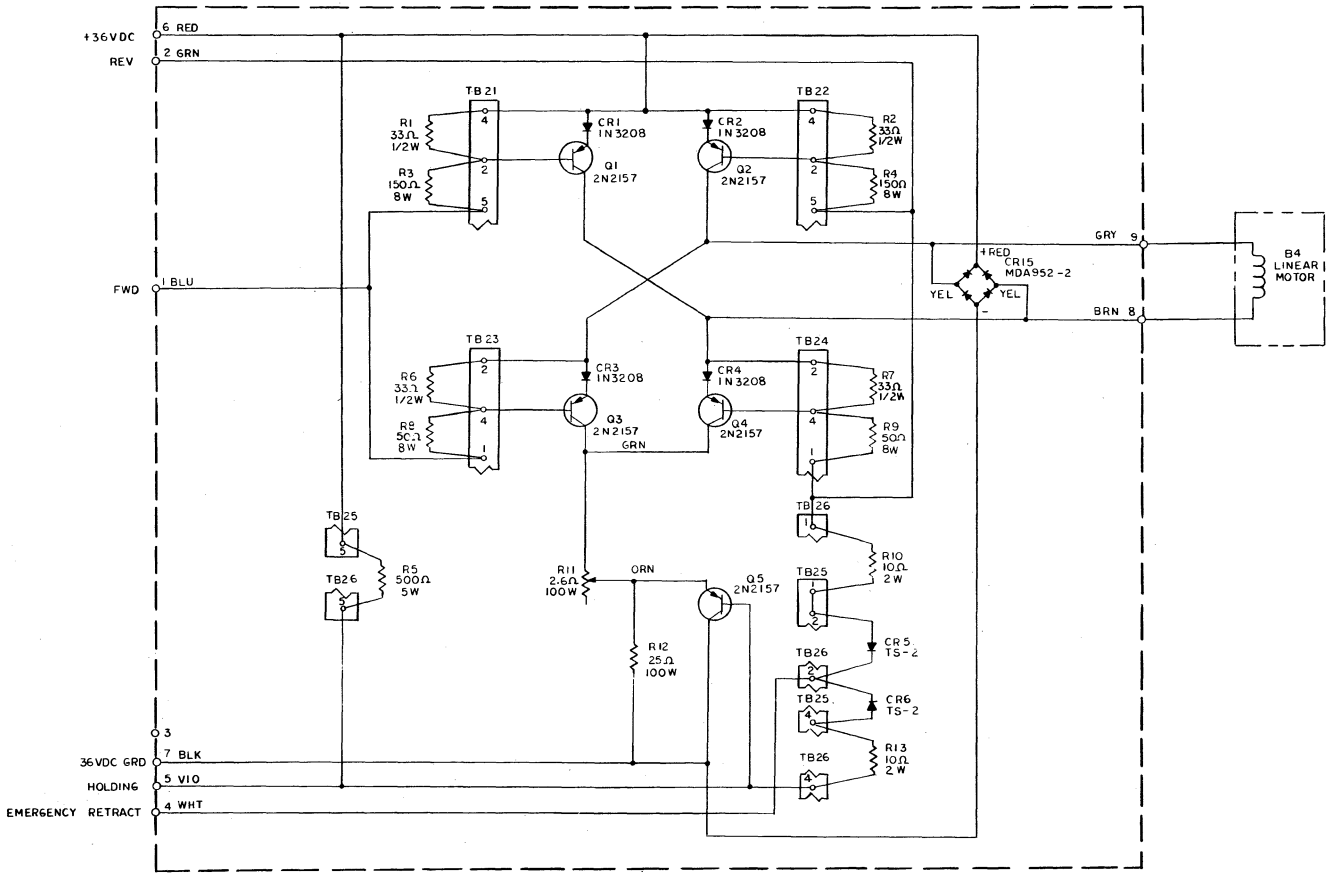


G.E. MOTOR TYPE 5KC37GI55X

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION				
			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM DISC DRIVE MOTOR			
CASE DEPTH			ANGLES ±					
HARDNESS				DESIGN	E Shn	2/15/68	TYPE	
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DETAIL			SCALE	NONE
008022	A		INSIDE MAX	CHECK			DRAW	K.B. 7-26-68
		RADII UNLESS OTHERWISE NOTED		APPRO	E Shn	4/3/68	CHECK	

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200462	3-21-68	36		
	8-20-68	170		
	10-8-69	455		

008024

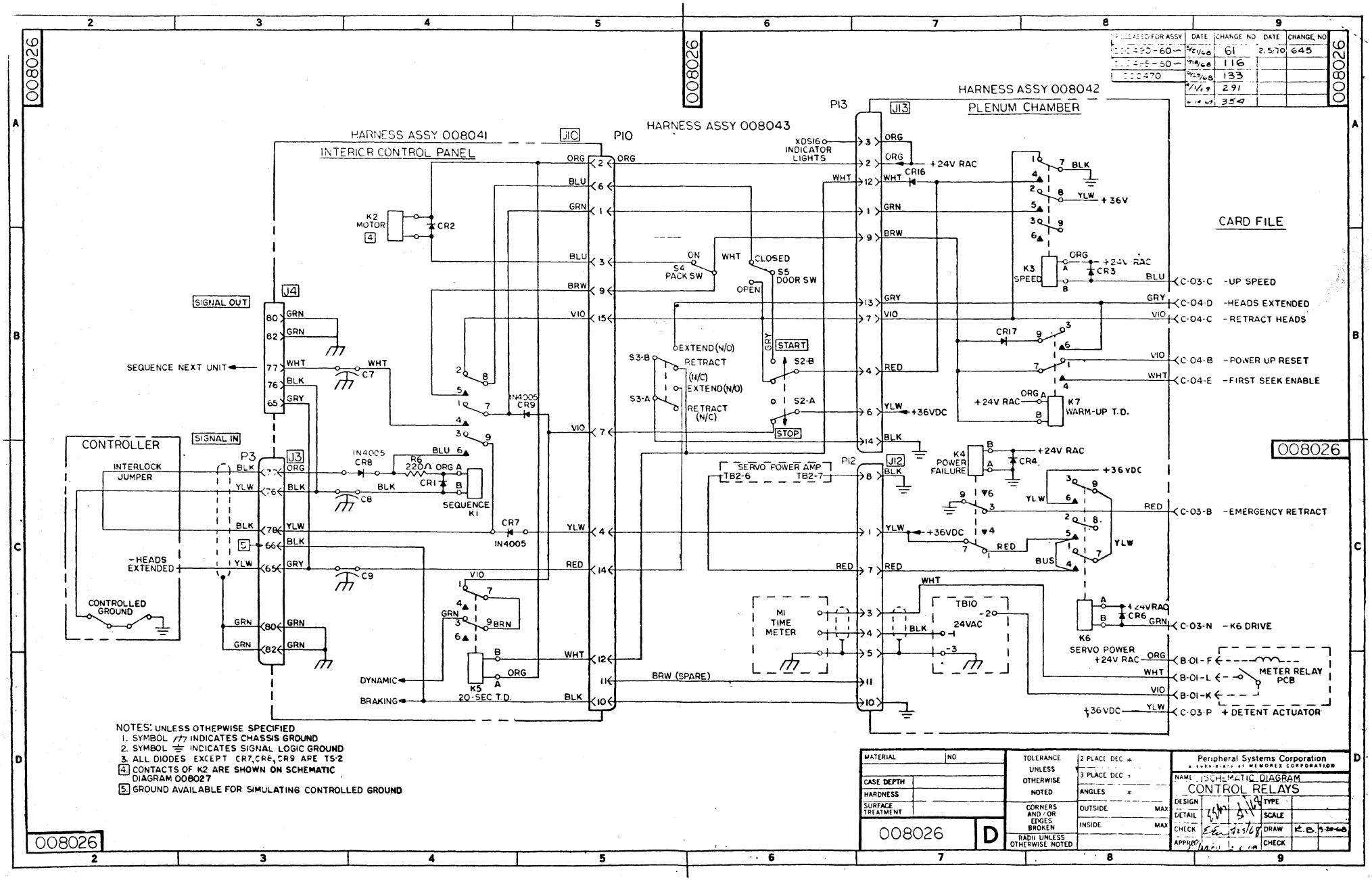


008024

NOTES: UNLESS OTHERWISE SPECIFIED,
1. O INDICATES TB2 TERMINALS.

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM
CASE DEPTH			ANGLES ±	SERVO PWR AMPLIFIER	
HARDNESS		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN EEL 2-15-68	TYPE
SURFACE TREATMENT			INSIDE MAX	DETAIL	SCALE
008024	D	RADII UNLESS OTHERWISE NOTED		CHECK Jam 2-11-68	DRAW 10-9-69
				APPRO EEL 3-11-68	CHECK 10-9-69

008024



NOTES: UNLESS OTHERWISE SPECIFIED
1. SYMBOL ⏚ INDICATES CHASSIS GROUND
2. SYMBOL ⏚ INDICATES SIGNAL LOGIC GROUND
3. ALL DIODES EXCEPT CR7, CR8, CR9 ARE TS-2
4. CONTACTS OF K2 ARE SHOWN ON SCHEMATIC DIAGRAM 008027
5. GROUND AVAILABLE FOR SIMULATING CONTROLLED GROUND

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
008480-60	9/1/68	61	2.5.70	645
008485-50	7/8/68	116		
008470	9/23/68	133		
	9/11/69	291		
	6/4/69	354		

MATERIAL	NO
CASE DEPTH	
HARDNESS	
SURFACE TREATMENT	
008026	D

TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±
	3 PLACE DEC ±
	ANGLES ±
CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX
	INSIDE MAX
RADII UNLESS OTHERWISE NOTED	

Peripheral Systems Corporation
A SUBSIDIARY OF MEMOREX CORPORATION

NAME: SCHEMATIC DIAGRAM CONTROL RELAYS

DESIGN		TYPE	
DETAIL	7/11/68	SCALE	
CHECK	7/15/68	DRAW	K.B. 9-20-68
APPROV		CHECK	

008026

RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
630A	4/9/68	61	SEPT. 70	1065
630-1A	5/2/68	90		
620-A	12/3/68	240		
	1 MAR 69	278		
	2/13/70	604		

008027

AC IN

AC OUT

INTERIOR CONTROL PANEL

P1 J1 TB1 J2

115 VAC 1Ø

FRAME GROUND

208–230 VAC 3Ø

E BLK 5 BLK E

G GRN GRN G

F WHT 6 WHT F

D GRN 4 GRN D

A BLK 1 BLK B

B WHT 2 WHT C

C RED 3 RED A

J6-A J6-B

WHT YEL F1 8A WHT FL 1

RED VIO F2 8A BLU FL 2

S1 POWER

P9 J9 J7 P7

TO POWER SUPPLY

WHT 1 WHT — WHT 1 WHT

BLK 3 BLU — R2 68 C11 .5 UF — GRN 2 GRN — BLU 3 BLU — BLK — B2 BLOWER

2 GRN

J8 P8

K5 5 9 6 GRN C1 15UF 330V AC BLK

DYNAMIC BRAKING 3

L1 50UH 5A — WHT 3 WHT — R3 68 C12 .5UF — GRN 2 GRN — BLU 1 BLU — BLK — B1 DISC MOTOR

L2 50UH 5A

K2 MOTOR COIL 3

008027

NOTES: UNLESS OTHERWISE SPECIFIED

1. REF SCHEMATIC 201941 FOR 50HZ POWER.
2. SYMBOL ⏚ INDICATES FRAME GROUND
3. REF SCHEMATIC 008026 (630 & 620) AND 200773 (630-1).

MATERIAL	NO.
CASE DEPTH	
HARDNESS	
SURFACE TREATMENT	
008027	C

TOLERANCE UNLESS OTHERWISE NOTED: 2 PLACE DEC ±; 3 PLACE DEC ±; ANGLES ±

CORNERS AND OR EDGES BROKEN: OUTSIDE MAX; INSIDE MAX

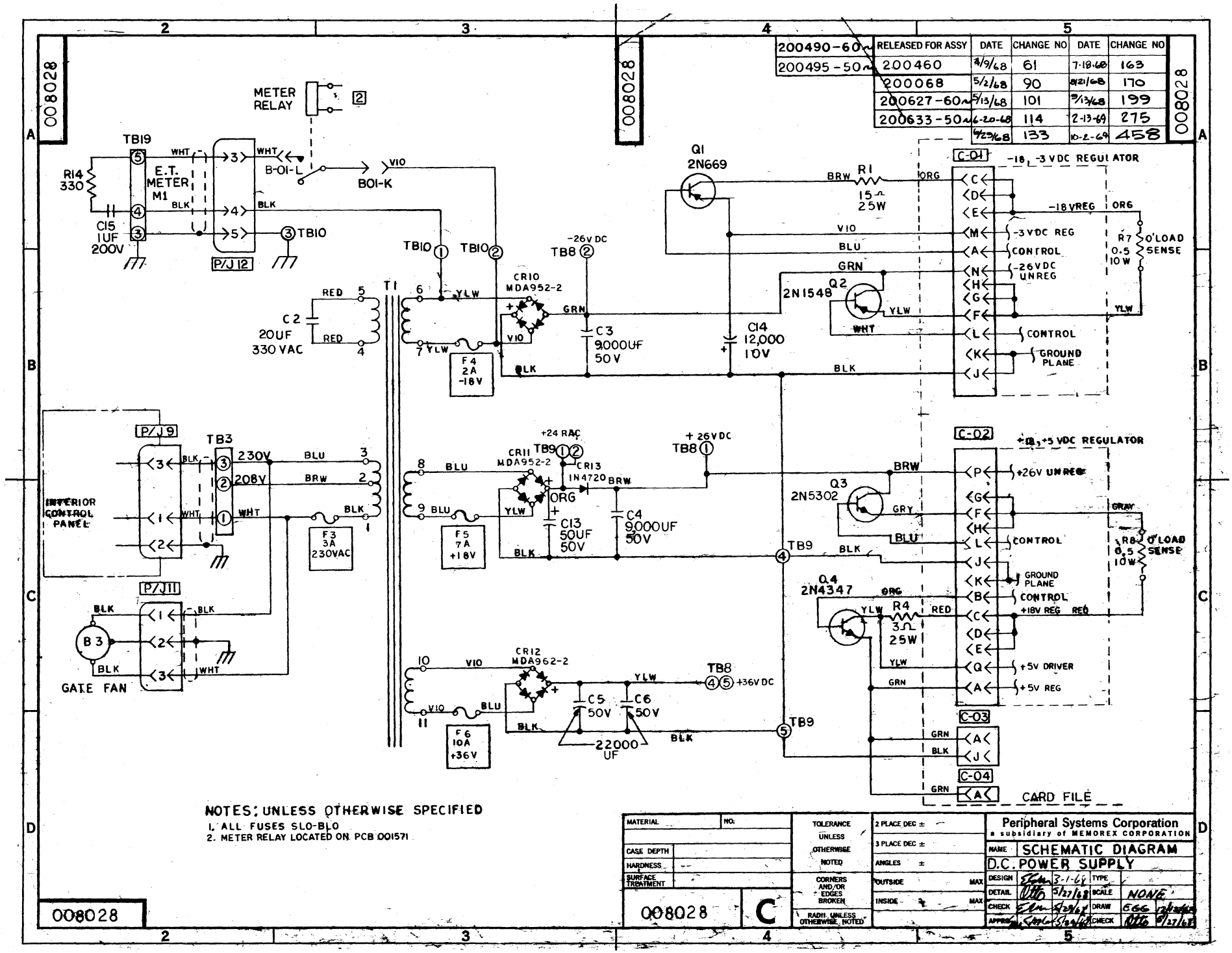
RADII UNLESS OTHERWISE NOTED

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

NAME: SCHEMATIC DIAGRAM
AC POWER 60HZ

DESIGN		TYPE	
DETAIL		SCALE	NONE
CHECK	3-12-68	DRAW	2-12-68
APPRO		CHECK	

008027

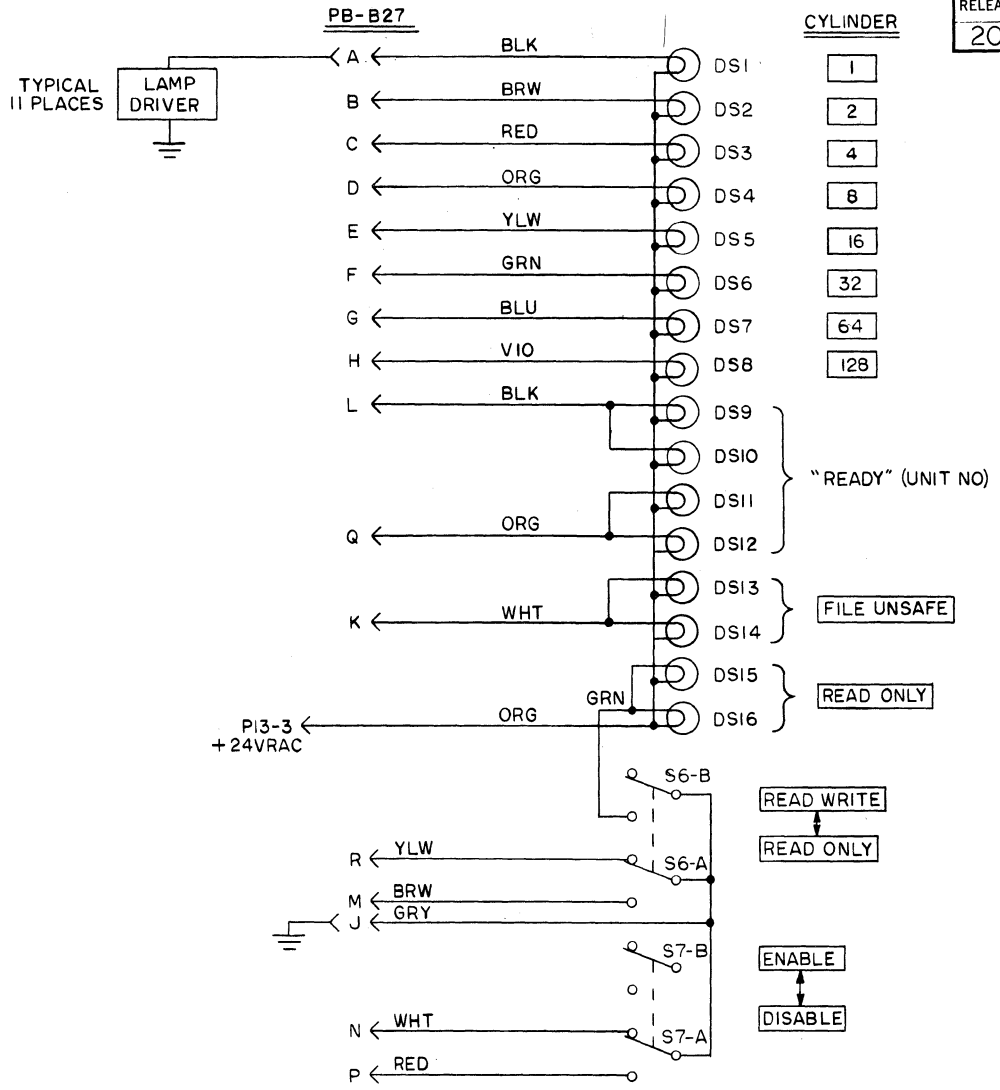


200490-60	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200495-50	200460	4/9/68	61	7-18-68	163
	200068	5/2/68	90	8/21/68	170
	200627-60	5/13/68	101	9/13/68	199
	200633-50	6-20-68	114	12-13-68	275
		6/25/68	133	10-2-69	458

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL FUSES SLO-BLO
2. METER RELAY LOCATED ON PCB 001571

MATERIAL	NO:	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
CASE DEPTH			3 PLACE DEC ±	NAME	SCHEMATIC DIAGRAM D.C. POWER SUPPLY
HARDNESS			ANGLES ±	DESIGN	3-1-68 TYPE
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN RADII UNLESS OTHERWISE NOTED	OUTSIDE MAX	DETAIL	5/27/68 SCALE NONE
008028	C		INSIDE MAX	CHECK	DRAW EGG
				APPRO	CHECK 9/27/68

008028



RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
200030	5-21-68	61		
	7-30-68	171		

NOTES:
1. FOR START-STOP SWITCH SEE SCHEMATIC 008026

008030

MATERIAL	NO.	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION
CASE DEPTH			3 PLACE DEC ±	NAME SCHEMATIC DIAGRAM
HARDNESS			ANGLES ±	OPERATOR CONTROL PANEL
SURFACE TREATMENT		CORNERS AND OR EDGES BROKEN	OUTSIDE MAX	DESIGN TYPE
008030	C	RADII UNLESS OTHERWISE NOTED	INSIDE MAX	DETAIL SCALE
				CHECK DRAW K.B. 5-21-68
				APPRO W&W 6-3-68 CHECK

008030

WIRE TABULATIONS

RELEASED FOR ASM
200485

DWG NO. 008048
SHEET 0 OF 86

MEMOREX EQUIPMENT GROUP

TITLE WIRE TAB BACK PANEL

SHEET	EC	EC	EC	EC	EC	EC
0	89	1188				
1	248	1188				
2	89	1188				
3	89	1188				
4	89	135	190	1188		
5	89	215	1188			
6	89	190	1188			
7	89	1188				
8	190	1188				
9	89	1188				
10	89	1188				
11	89	190	1188			
12	89	100	1188			
13	89	1188				
14	89	100	1188			
15	89	100	190	1188		
16	89	124	1188			
17	89	1188				
18	89	1188				
19	89	1188				
20	89	1188				
21	89	1188				
22	89	1188				
23	89	100	135	1188		
24	89	215	1188			
25	89	190	215	1188		
26	89	215	1188			
27	89	100	124	1188		
28	89	100	124	1188		
29	89	133	1188			
30	89	1188				
31	89	1188				
32	89	1188				
33	89	1188				
34	89	1188				
35	89	1188				
36	89	190	1188			
37	89	1188				
38	89	100	1188			
39	89	100	1188			
40	89	100	1188			
41	89	100	1188			
42	89	190	1188			
43	89	100	1188			
44	89	1188				
45	89	1188				
46	89	1188				
47	89	1188				
48	89	1188				

SHEET	EC	EC	EC	EC	EC	EC
49	89	1188				
50	89	1188				
51	89	1188				
52	89	215	1188			
53	89	100	124	1188		
54	89	100	1188			
55	89	1188				
56	89	190	1188			
57	89	1188				
58	89	1188				
59	89	133	135	1188		
60	89	1188				
61	89	100	124	135	1188	
62	89	190	1188			
63	89	190	1188			
64	89	190	1188			
65	89	190	1188			
66	89	100	124	1188		
67	89	124	1188			
68	89	194	1188			
69	89	1188				
70	89	190	1188			
71	89	100	1188			
72	89	1188				
73	89	1188				
74	89	1188				
75	89	1188				
76	89	1188				
77	89	124	1188			
78	89	124	1188			
79	89	100	1188			
80	89	1188				
81	89	1188				
82	89	1188				
83	89	1188				
84	89	229	1188			
85	89	1188				
86	89	190	225	1188		

WIRE TABULATIONS

RELEASED FOR ASSY 200485

DWG NO. 008048

SHEET 1 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A01

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0001		A	01	A									+5 VOLTS
0002				B									
0003				C									
0004				D									
0005				E									
0006				F									
0007				G									
0008				H									
0009				J									GROUND
0010				K									
0011				L									
0012				M									
0013				N									
0014				P									
0015				Q									
0016		A	01	R									

ENG. CHANGE NO.	248	1188									
DATE	12/06/68	7/30/70									

PSC 030 1-69

A01

WIRE TABULATIONS

RELEASED FOR ASSY 200485

DWG NO. 008048

SHEET 2 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A02

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0017		A	02	A									+5 VOLTS
0018				B									
0019				C									
0020				D									
0021				E									
0022				F									
0023				G									
0024				H									
0025				J									GROUND
0026				K									
0027				L									
0028				M									
0029				N									
0030				P									
0031				Q									
0032		A	02	R									

ENG. CHANGE NO.	89	1188									
DATE	5-21-68	7/30/70									

PSC 030 1-69

A02

WIRE TABULATIONS

RELEASED FOR ASSY 200485

DWG NO. 008048

SHEET 3 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A03

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0033		A	03	A									+5 VOLTS
0034				B									
0035				C									
0036				D									
0037				E									
0038				F									
0039				G									
0040				H									
0041				J									GROUND
0042				K									
0043				L									
0044				M									
0045				N									
0046				P									
0047				Q									
0048		A	03	R									

ENG. CHANGE NO.	89	1188									
DATE	5-21-68	7/30/70									

PSC 030 1-69

A03

WIRE TABULATIONS

RELEASED FOR ASSY 200485

DWG NO. 006018

SHEET 4 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

FROM						WIRE LENGTH	TO					LOC/NAME: A04-HOME SECTION:	
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
0049		A	04	A									+5 VOLTS
0050				B					C	10	B		
									C	17	K		
0051				C					C	04	H		
0052				D					C	04	G		
									C	09	M		
									C	10	L		
0053				E					C	05	H		
									C	10	N		
									C	10	R		
									C	11	C		
0054				F					C	04	K		
0055				G					A	24	P		
0056				H					B	24	C		
									C	16	G		
0057				J									GROUND
0058				K					C	04	F		
0059				L					A	15	K		
									B	12	E		
0060				M					B	25	F		
0061				N					B	25	E		
									B	25	Q		
									C	05	K		
									C	07	K		
									C	12	F		
0062				P					B	07	C		
									C	10	G		
0063				Q									+18 VOLTS
0064				R									-18 VOLTS

ENG. CHANGE NO.	89	135	190	1188							
DATE	5/21/68	6/19/68	10/7/68	7/30/70							

WIRE TABULATIONS

RELEASED FOR ASSY 200485

DWG NO. 006048

SHEET 5 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A05-LATCHES

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0065		A	05	A									+5 VOLTS
0066				B					A	05	D		
0067				C					A	24	H		
									A	25	G		
									C	09	D		
0068				D			0066						
0069				E									
0070				F									
0071				G									
0072				H					A	26	B		
									B	24	E		
									B	25	H		
0073				J									GROUND
0074				K					A	27	C		
0075				L			1054						
0076				M									
0077				N					A	26	C		
0078				P									
0079				Q					A	24	F		
									B	24	D		
0080				R									

ENG. CHANGE NO.	89	215	1188								
DATE	~~5/22/68~~	10/2/68	7/30/70								

PSC 030 1-69

A05

WIRE TABULATIONS

RELEASED FOR ASSY 200485

DWG NO. 008048

SHEET 6 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A06-INVERTERS

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0081		A	06	A									+5 VOLTS
0082				B					A	20	F		
									B	07	F		
									B	20	F		
0083				C					C	10	P		
0084				D					A	20	R		
0085				E					B	07	M		
0086				F					C	11	G		
0087				G					C	08	B		
									C	08	M		
									C	15	E		
0088				H					B	07	B		
0089				J									GROUND
0090				K					A	24	L		
									B	06	E		
									B	06	L		
									B	25	D		
0091				L					C	08	L		
									C	09	N		
									C	12	H		
0092				M					B	05	N		
0093				N					C	16	D		
									C	20	K		
0094				P					C	11	B		
0095				Q					C	13	D		
									C	15	C		
									C	17	R		
0096				R					A	14	G		
									B	28	Q		
									C	13	C		
									C	13	L		

ENG. CHANGE NO.	89	190	1188								
DATE	5/21/68	10/7/68	7/30/70								

PSC 030 1-69

A06

WIRE TABULATIONS

RELEASED FOR ASSY 200485

DWG NO. 008048

SHEET 7 OF 86

Peripheral Systems Corporation.
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A07- 4 BIT DRIVERS

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0097		A	07	A									+5 VOLTS
0098				B					A	20	D		
									B	20	D		
0099				C									
0100				D									
0101				E									
0102				F									
0103				G					B	06	N		
									B	19	L		
									C	08	P		
0104				H					C	20	H		
0105				J									GROUND
0106				K									
0107				L									
0108				M									
0109				N									
0110				P									
0111				Q									
0112				R									

ENG. CHANGE NO.	89	1188									
DATE	5-21-68	7/30/70									

PSC 030 1-69

A07

WIRE TABULATIONS

RELEASED FOR ASSY 200485

DWG NO. 008048

SHEET 8 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A08-LAMP DRIVERS

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0113		A	08	A									+5 VOLTS
0114				B					A	10	F		
									A	12	B		
0115				C					B	27	A		
0116				D					A	10	N		
									A	12	K		
0117				E					B	27	B		
0118				F					B	27	C		
0119				G					B	10	D		
									B	12	F		
0120				H									
0121				J									GROUND
0122				K					B	10	M		
									B	12	Q		
0123				L					B	27	D		
0124				M									
0125				N					B	27	E		
0126				P					A	11	F		
									A	13	B		
0127				Q									
0128				R									

ENG. CHANGE NO.	190	1188									
DATE	10/7/68	7/30/70									

PSC 030 1-69

A08

WIRE TABULATIONS

RELEASED FOR ASSY 200485

DWG NO. 006048

SHEET 9 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A09-J-K REGISTER

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0129		A	09	A									+5 VOLTS
0130				B					C	21	C		
0131				C					A	12	C		
0132				D					B	09	D		
									C	10	K		
0133				E					A	12	L		
0134				F					C	21	D		
0135				G					A	20	E		
									C	17	H		
									C	20	P		
0136				H					A	20	C		
									B	07	L		
									C	20	N		
0137				J									GROUND
0138				K					B	20	C		
									C	17	L		
									C	18	H		
0139				L					B	20	E		
									C	17	C		
									C	18	K		
0140				M					B	07	P		
									B	09	M		
0141				N					C	21	F		
0142				P					B	12	M		
0143				Q					C	21	E		
0144				R					B	12	G		

ENG. CHANGE NO.	89	1188									
DATE	5-21-68	7/30/70									

PSC 030 1-69

A09

WIRE TABULATIONS

RELEASED FOR ASSY 200485

DWG NO. 008048

SHEET 10 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A10-UP/DOWN COUNTER

SECTION:

FROM						WIRE LENGTH	TO						
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
0145		A	10	A									+5 VOLTS
0146				B					A	10	J		
									A	10	L		
0147				C									
0148				D					B	06	M		
0149				E									
0150				F			0114						
0151				G					A	11	G		
									B	06	D		
0152				H									
0153				J			0146						GROUND
0154				K					A	11	K		
									B	06	R		
0155				L			0146						
0156				M									
0157				N			0116						
0158				P									
0159				Q									
0160				R									

ENG. CHANGE NO.	89	1188									
DATE	5/21/68	7/30/70									

PSC 030 1-69

A10

WIRE TABULATIONS

RELEASED FOR ASSY 200485

DWG NO. 008048
SHEET 11 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A11- UP-DOWN COUNTER
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0161		A	11	A									+5 VOLTS
0162				B					A	11	L		
									A	11	J		
0163				C									
0164				D					B	10	K		
0165				E									
0166				F			0126						
0167				G			0151						
0168				H									
0169				J			0162						GROUND
0170				K			0154						
0171				L			0162						
0172				M									
0173				N					A	13	K		
									B	08	B		
0174				P									
0175				Q									
0176				R									

ENG. CHANGE NO.	89	190	1188								
DATE	5/21/68	10/7/68	7/30/70								

WIRE TABULATIONS

RELEASED FOR ASSY 200485

DWG NO. 008048

SHEET 12 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

FROM						WIRE LENGTH	TO					LOC/NAME: A12-ADDER SECTION:	
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
0177		A	12	A									+5 VOLTS
0178				B			0114						
0179				C			0131						
0180				D					A	24	K		
									B	07	Q		
									B	12	K		
									B	13	K		
									B	13	N		
0181				E									
0182				F									.01 CAP
0183				G									
0184				H									
0185				J									
0186				K			0116						
0187				L			0133						
0188				M									
0189				N									
0190				P					A	15	M		
0191				Q									
0192				R					A	15	L		

ENG. CHANGE NO.	89	100	1188								
DATE	5-21-68	6-7-68	7/30/70								

PSC 030 1-69

A12

WIRE TABULATIONS

RELEASED FOR ASSY 200485

DWG NO. 008048

SHEET 13 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A13-ADDER

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0193		A	13	A									+5 VOLTS
0194				B			0126						
0195				C					B	09	C		
0196				D					B	12	N		
0197				E									
0198				F									
0199				G									
0200				H									
0201				J									GROUND
0202				K			0173						
0203				L					B	09	E		
0204				M									
0205				N									
0206				P					A	15	C		
0207				Q									
0208				R					A	15	E		

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SHEET 14 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A14-READ/WRITE ENABLE

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0209		A	14	A									+5 VOLTS
0210				B									
0211				C					C	13	R		
0212				D									
0213				E									
0214				F					B	24	K		
									C	13	H		
									C	15	D		
0215				G			0096						
0216				H									
0217				J									GRO UND
0218				K					B	04	Q		
									B	24	Q		
									B	24	M		
0219				L					B	18	N		
0220				M					B	28	P		
0221				N					C	08	E		
									C	13	E		
0222				P					A	26	H		
									A	27	F		
									C	03	P		
									C	05	P		
0223				Q									+ 18 VOLTS
0224				R									

ENG. CHANGE NO.	89	100	1188								
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WIRE TABULATIONS

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DWG NO. 008048

SHEET 15 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

FROM						WIRE LENGTH	TO					LOC/NAME: A15-FWD/REV SPEED DECOD SECTION:	
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
0225		A	15	A									+5 VOLTS
0226				B					B	23	C		
0227				C			0206						
0228				D					B	12	C		
0229				E			0208						
0230				F					B	13	E		
0231				G					B	13	C		
0232				H					B	25	C		
0233				J									GROUND
0234				K			0059						
0235				L			0192						
0236				M			0190						
0237				N									
0238				P					A	24	E		
									B	15	D		
0239				Q									
0240				R					C	08	K		

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WIRE TABULATIONS

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DWG NO. 008048

SHEET 16 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A16-READ AMPLIFIER

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0241		A	16	A									+5 VOLTS
0242				B					A	28	H	(COAX)	GROUND SHIELD AT A17J
0243				C									
0244				D					A	28	N	(COAX)	GROUND SHIELD AT A15J
0245				E									
0246				F									
0247				G									
0248				H									
0249				J									GROUND
0250				K									
0251				L									
0252				M									
0253				N									
0254				P									
0255				Q									+ 18 VOLTS
0256				R									

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A17

SECTION:

FROM SEQUENCE	FILE	ROW	COLUMN	PIN		WIRE LENGTH	TO REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
0257		A	17	A									+5 VOLTS
0258				B									
0259				C									
0260				D									
0261				E									
0262				F									
0263				G									
0264				H									
0265				J									GROUND
0266				K									
0267				L									
0268				M									
0269				N									
0270				P									
0271				Q									
0272				R									

ENG. CHANGE NO.	89	1188									
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SHEET 18 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A18-HEAD SWITCH DRIVER

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0273		A	18	A									+5 VOLTS
0274				B					B	05	B		
									B	28	A		
0275				C					A	19	L		
0276				D					B	05	C		
									B	28	B		
0277				E					A	19	K		
0278				F					B	05	D		
									B	28	C		
0279				G					A	19	G		
0280				H					B	05	E		
									B	28	D		
0281				J									GROUND
0282				K					A	19	F		
0283				L									
0284				M					B	05	F		
									B	28	E		
0285				N					B	19	R		
0286				P					B	05	G		
									B	28	F		
0287				Q									
0288				R									

ENG. CHANGE NO.	89	1188									
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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

FROM						WIRE LENGTH	TO					LOC/NAME: A19-HEAD SWITCH DECODE SECTION:	
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
0289		A	19	A									+5 VOLTS
0290				B									
0291				C									
0292				D									
0293				E									
0294				F			0282						
0295				G			0279						
0296				H									
0297				J									GROUND
0298				K			0277						
0299				L			0275						
0300				M					A	20	Q		
0301				N					A	20	P		
0302				P					A	20	N		
									B	20	R		
0303				Q					A	20	G		
0304				R					B	18	L		

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SHEET 20 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A20-HEAD REGISTER

SECTION:

FROM SEQUENCE	FROM FILE	FROM ROW	FROM COLUMN	FROM PIN		WIRE LENGTH	TO REFERENCE	TO FILE	TO ROW	TO COLUMN	TO PIN	LINE LABEL	REMARKS
0305		A	20	A									+5 VOLTS
0306				B									
0307				C			0136						
0308				D			0098						
0309				E			0135						
0310				F			0082						
0311				G			0303						
0312				H									
0313				J									GROUND
0314				K									
0315				L									
0316				M									
0317				N			0302						
0318				P			0301						
0319				Q			0300						
0320				R			0084						

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A21
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0321		A	21	A									+5 VOLTS
0322				B									
0323				C									
0324				D									
0325				E									
0326				F									
0327				G									
0328				H									
0329				J									GROUND
0330				K									
0331				L									
0332				M									
0333				N									
0334				P									
0335				Q									
0336				R									

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WIRE TABULATIONS

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SHEET 22 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A22-TACH AMP-ZERO VEL

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0337		A	22	A									+5 VOLTS
0338				B									
0339				C									
0340				D									
0341				E									
0342				F									
0343				G									
0344				H					B	25	K		
0345				J									GROUND
0346				K					A	28	D		
0347				L					B	23	D		
0348				M					B	23	B		
0349				N					A	28	E		
0350				P									
0351				Q									
				R									

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A23-UP SPEED DETECTOR
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0352		A	23	A									+5 VOLTS
0353				B					A	27	L		
0354				C					C	12	E		
0355				D									
0356				E									
0357				F									
0358				G									
0359				H									
0360				J									GROUND
0361				K									
0362				L									
0363				M									
0364				N					B	08	P		
									C	07	D		
0365				P					C	15	H		
0366				Q									+18 VOLTS
0367				R									

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A24-SEEK FWD/REV

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0368		A	24	A									+5 VOLTS
0369				B					B	12	R		
									B	13	R		
0370				C					B	22	K		
0371				D									
0372				E			0238						
0373				F			0079						
0374				G					B	22	L		
0375				H			0067						
0376				J									GROUND
0377				K			0180						
0378				L			0090						
0379				M					C	09	P		
									C	10	E		
									C	17	D		
0380				N					B	06	C		
									B	06	K		
									C	16	H		
0381				P			0055						
0382				Q					A	25	M		
0383				R					B	06	Q		

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SHEET 25 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: A25-CLOCK GENERATOR
SECTION:

FROM SEQUENCE	FILE	ROW	COLUMN	PIN		WIRE LENGTH	TO REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
0384		A	25	A									+5 VOLTS
0385				B					C	09	H		
0386				C					B	25	L		
0387				D					C	08	H		
0388				E					B	10	F		
									B	11	F		
									B	22	E		
									C	10	H		
									C	15	G		
0389				F									
0390				G			0067						
0391				H									
0392				J									GROUND
0393				K									
0394				L									
0395				M			0382						
0396				N					B	22	C		
0397				P					A	27	R		
									B	26	M		
0398				Q									
0399				R									

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME A26-ACTUATOR LOGIC & DRIVER
SECTION

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0400		A	26	A									+5 VOLTS
0401				B			0072						
0402				C			0077						
0403				D					TB-15 -		4		#24 AWG (YEL)
0404				E									
0405				F					TB-15-2				#24 AWG (VIO)
0406				G									
0407				H			0222						
0408				J									GROUND
0409				K									
0410				L									
0411				M									
0412				N					TB-15-3				#24 AWG (BLU)
0413				P									
0414				Q									
0415				R									

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

FROM						WIRE LENGTH	TO					LOC/NAME: A27-SIGNAL PADDLE BOARD SECTION:	
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
0416		A	27	A									
0417				B					TB-16-3				#24 AWG (GRN)
0418				C			0074						
0419				D									
0420				E					B	22	D		
0421				F			0222						
0422				G									
0423				H									
0424				J									GROUND
0425				K					TB-16-4				#24 AWG (GRY)
0426				L			0353						
0427				M									
0428				N									
0429				P									
0430				Q									+ 18 VOLTS
0431				R			0397						

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME A28-SIGNAL PADDLE BOARD
SECTION

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0432		A	28	A									+ 5 VOLTS
0433				B					TB-16	-	5		#24 AWG (ORG)
									B	23	N		
0434				C					B	23	P		
0435				D			0346						
0436				E			0349						
0437				F					A	28	J		
0438				G					C	03	B		
0439				H			0242						
0440				J			0437						GROUND
0441				K					COAX SHIELD			FROM A28H	
0442				L					B	25	P		
0443				M					B	22	B		
0444				N			0244						
0445				P					COAX SHIELD FROM A28N				
0446				Q			0430						+18 VOLTS
0447				R									

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WIRE TABULATIONS

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: B01-METER RELAY
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0448		B	01	A									+5 VOLTS
0449				B									
0450				C									
0451				D									
0452				E									
0453				F					C	03	F		
0454				G					C	07	E		
0455				H									
0456				J									GROUND
0457				K					C	03	K		
0458				L					C	03	L		
0459				M									
0460				N									
0461				P									
0462				Q									
0463				R									

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WIRE TABULATIONS

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: B02
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0464		B	02	A									+5 VOLTS
0465				B									
0466				C									
0467				D									
0468				E									
0469				F									
0470				G									
0471				H									
0472				J									GROUND
0473				K									
0474				L									
0475				M									
0476				N									
0477				P									
0478				Q									
0479				R									

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: B03

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0480		B	03	A									+5 VOLTS
0481				B									
0482				C									
0483				D									
0484				E									
0485				F									
0486				G									
0487				H									
0488				J									GROUND
0489				K									
0490				L									
0491				M									
0492				N									
0493				P									
0494				Q									
0495				R									

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME B04 READ/WRITE ENABLE SYNC

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0496		B	04	A									+5 VOLTS
0497				B					C	12	L		
0498				C					C	12	G		
0499				D					C	19	M		
0500				E					B	27	P		
0501				F					B	27	N		
0502				G					C	19	N		
0503				H					C	10	C		
									C	12	K		
0504				J									GROUND
0505				K					C	15	R		
									C	16	N		
0506				L									
0507				M					B	06	P		
									B	24	N		
									C	08	C		
									C	11	E		
									C	12	M		
0508				N					B	27	M		
0509				P					B	27	R		
0510				Q			0218						
0511				R									

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: B05-HEADS SAFETY

SECTION:

FROM						WIRE LENGTH	TO						
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
0512		B	05	A									+5 VOLTS
0513				B			0274						
0514				C			0276						
0515				D			0278						
0516				E			0280						
0517				F			0284						
0518				G			0286						
0519				H					B	18	C		
									B	28	G		
0520				J									GROUND
0521				K					B	18	F		
									B	28	H		
0522				L					B	18	G		
									B	28	K		
0523				M					B	18	K		
									B	28	L		
0524				N			0092						
0525				P									
0526				Q									+18 V
0527				R					C	15	K		

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: B06-DRIVERS

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0528		B	06	A									+5 VOLTS
0529				B					B	10	E		
									B	11	E		
0530				C			0380						
0531				D			0151						
0532				E			0090						
0533				F					B	16	C		
0534				G									
0535				H					C	15	F		
									C	17	P		
0536				J									GROUND
0537				K			0380						
0538				L			0090						
0539				M			0148						
0540				N			0103						
0541				P			0507						
0542				Q			0383						
0543				R			0154						

ENG. CHANGE NO.	89	100	1188								
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WIRE TABULATIONS

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200485

DWG NO. 008048
SHEET 35 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: B07-DRIVERS (6)
SECTION:

FROM						WIRE LENGTH	TO						
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
0544		B	07	A									+5 VOLTS
0545				B			0088						
0546				C			0062						
0547				D									
0548				E									
0549				F			0082						
0550				G					B	09	H		
									C	18	L		
0551				H					B	07	K		
									C	16	B		
									C	17	G		
0552				J									GROUND
0553				K			0551						
0554				L			0136						
0555				M			0085						
0556				N					C	16	C		
0557				P			0140						
0558				Q			0180						
0559				R									

ENG. CHANGE NO.	89	190	1188								
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WIRE TABULATIONS

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DWG NO. 008048

SHEET 36 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: B08-LAMP DRIVERS

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0560		B	08	A									+5 VOLTS
0561				B			0173						
0562				C					B	27	F		
0563				D					B	11	D		
									B	13	F		
0564				E					B	27	G		
0565				F					B	27	H		
0566				G					B	11	M		
									B	13	Q		
0567				H									
0568				J									GROUND
0569				K					C	05	M		
									C	07	G		
0570				L					B	27	L		
0571				M									
0572				N					C	03	C		
0573				P			0364						
0574				Q									
0575				R									

ENG. CHANGE NO.	89	190	1188								
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WIRE TABULATIONS

RELEASED FOR ASSY 200485

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: B09-J-K REGISTER

SECTION:

FROM						WIRE LENGTH	TO						
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
0576		B	09	A									+5 VOLTS
0577				B					C	21	G		
0578				C			0195						
0579				D			0132						
0580				E			0203						
0581				F					C	22	E		
0582				G					C	17	E		
									C	18	M		
0583				H			0550						
0584				J									GROUND
0585				K					C	16	Q		
									C	17	N		
									C	18	N		
0586				L					C	17	Q		
									C	18	P		
0587				M			0140						
0588				N					C	22	G		
0589				P					B	13	M		
0590				Q					C	22	F		
0591				R					B	13	G		

ENG. CHANGE NO.	89	1188									
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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: B10-UP/DOWN COUNTER
SECTION:

FROM						WIRE LENGTH	TO						
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
0592		B	10	A									+5 VOLTS
0593				B					B	10	G		
									B	11	B		
									B	11	G		
									B	24	B		
0594				C									
0595				D			0119						
0596				E			0529						
0597				F			0388						
0598				G			0593						
0599				H									
0600				J									GROUND
0601				K			0164						
0602				L									
0603				M			0122						
0604				N									
0605				P									
0606				Q									
0607				R									

ENG. CHANGE NO.	89	100	1188								
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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME B11-UP/DOWN COUNTER
SECTION:

FROM						WIRE LENGTH	TO						
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
0608		B	11	A									+5 VOLTS
0609				B			0593						
0610				C									
0611				D			0563						
0612				E			0529						
0613				F			0388						
0614				G			0593						
0615				H									
0616				J									GROUND
0617				K									
0618				L									
0619				M			0566						
0620				N									
0621				P									
0622				Q									
0623				R									

ENG. CHANGE NO.	89	100	1188								
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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: B12-ADDER
SECTION:

FROM						WIRE LENGTH	TO						
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
0624		B	12	A									+5 VOLTS
0625				B									
0626				C			0228						
0627				D									
0628				E			0059						
0629				F			0119						
0630				G			0144						
0631				H									
0632				J									GROUND
0633				K			0180						
0634				L									
0635				M			0142						
0636				N			0196						
0637				P									
0638				Q			0122						
0639				R			0369						

ENG. CHANGE NO.	89	100	1188								
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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: B13-ADDER

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0640		B	13	A									+5 VOLTS
0641				B									
0642				C			0231						
0643				D									
0644				E			0230						
0645				F			0563						
0646				G			0591						
0647				H									
0648				J									GROUND
0649				K			0180						
0650				L									
0651				M			0589						
0652				N			0180						
0653				P									
0654				Q			0566						
0655				R			0369						

ENG. CHANGE NO.	89	100	1188								
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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME B14-READ/WRITE ENABLE
SECTION

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0656		B	14	A									+5 VOLTS
0657				B									
0658				C									
0659				D									
0660				E									
0661				F									
0662				G									
0663				H									
0664				J									GROUND
0665				K					C	08	G		
									C	13	G		
0666				L									
0667				M									
0668				N					B	28	M		
0669				P									
0670				Q									
0671				R									

ENG. CHANGE NO.	89	190	1188								
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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

FROM						WIRE LENGTH	TO					LOC/NAME: B15-FWD/REV SPEED DECODE SECTION:	
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
0672		B	15	A									+5 VOLTS
0673				B									
0674				C									
0675				D			0238						
0676				E									
0677				F									
0678				G									
0679				H									
0680				J									GROUND
0681				K									
0682				L									
0683				M									
0684				N									
0685				P									
0686				Q					B	25	B		
0687				R					B	23	E		

ENG. CHANGE NO.	89	100	1188								
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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME B16 READ DECODE/COAX DRIVER
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0688		B	16	A									+5 VOLTS
0689				B									
0690				C			0533						
0691				D									
0692				E									
0693				F									
0694				G									
0695				H									
0696				J									GROUND
0697				K									
0698				L									
0699				M									
0700				N									
0701				P									COAX SHIELD TO B16J
0702				Q									+18 VOLTS
0703				R									-18 VOLTS

ENG. CHANGE NO.	89	1188										
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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

FROM						WIRE LENGTH	TO					LOC/NAME: B17 SECTION:	
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
0704		B	17	A									+5 VOLTS
0705				B									
0706				C									
0707				D									
0708				E									
0709				F									
0710				G									
0711				H									
0712				J									GROUND
0713				K									
0714				L									
0715				M									
0716				N									
0717				P									
0718				Q									
0719				R									

ENG. CHANGE NO.	89	1188									
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WIRE TABULATIONS

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME B18-HEAD SWITCH DRIVER
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0720		B	18	A									+5 VOLTS
0721				B					B	19	F		
0722				C			0519						
0723				D					B	19	Q		
0724				E					B	19	G		
0725				F			0521						
0726				G			0522						
0727				H					B	19	K		
0728				J									GROUND
0729				K			0523						
0730				L			0304						
0731				M									
0732				N			0219						
0733				P									
0734				Q									
0735				R									

ENG. CHANGE NO.	89	1188										
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WIRE TABULATIONS

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: B19-HEAD SWITCH DECODER
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0736		B	19	A									+5 VOLTS
0737				B					B	20	Q		
0738				C					B	20	P		
0739				D					B	20	N		
0740				E					B	20	G		
0741				F			0721						
0742				G			0724						
0743				H					C	11	K		
0744				J									GROUND
0745				K			0727						
0746				L			0103						
0747				M									
0748				N									
0749				P									
0750				Q			0723						
0751				R			0285						

ENG. CHANGE NO.	89	1188									
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WIRE TABULATIONS

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: B20-HEAD REGISTER
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0752		B	20	A									+5 VOLTS
0753				B									
0754				C			0138						
0755				D			0098						
0756				E			0139						
0757				F			0082						
0758				G			0740						
0759				H									
0760				J									GROUND
0761				K									
0762				L									
0763				M									
0764				N			0739						
0765				P			0738						
0766				Q			0737						
0767				R			0302						

ENG. CHANGE NO.	89	1188									
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WIRE TABULATIONS

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200485

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: B21
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0768		B	21	A									+5 VOLTS
0769				B									
0770				C									
0771				D									
0772				E									
0773				F									
0774				G									
0775				H									
0776				J									GROUND
0777				K									
0778				L									
0779				M									
0780				N									
0781				P									
0782				Q									
0783				R									

ENG. CHANGE NO.	89	1188									
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WIRE TABULATIONS

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200485

DWG NO. 008048
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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: B22-NULL DETECTOR
SECTION:

FROM						WIRE LENGTH	TO						
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
0784		B	22	A									+5 VOLTS
0785				B			0443						
0786				C			0396						
0787				D			0420						
0788				E			0388						
0789				F									
0790				G									
0791				H									
0792				J									GROUND
0793				K			0370						
0794				L			0374						
0795				M									
0796				N									
0797				P									
0798				Q									
0799				R									

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WIRE TABULATIONS

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: B23-SERVO AMP

SECTION:

FROM SEQUENCE	FROM FILE	FROM ROW	FROM COLUMN	FROM PIN		WIRE LENGTH	TO REFERENCE	TO FILE	TO ROW	TO COLUMN	TO PIN	LINE LABEL	REMARKS
0800		B	23	A									+5 VOLTS
0801				B			0348						
0802				C			0226						
0803				D			0347						
0804				E			0687						
0805				F									
0806				G									
0807				H									
0808				J									GROUND
0809				K									
0810				L									
0811				M									
0812				N			0433						
0813				P			0434						
0814				Q									
0815				R									

ENG. CHANGE NO.	89	1188									
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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: B24-FORCE SEEK COUNT
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0816		B	24	A									+5 VOLTS
0817				B			0593						
0818				C			0056						
0819				D			0079						
0820				E			0072						
0821				F									
0822				G									
0823				H									
0824				J									GROUND
0825				K			0214						
0826				L					C	17	B		
0827				M			0218						
0828				N			0507						
0829				P					B	24	R		
									C	24	C		
0830				Q			0218						
0831				R			0829						

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: B25-DETENT LOGIC II
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0832		B	25	A									+5 VOLTS
0833				B			0686						
0834				C			0232						
0835				D			0090						
0836				E			0061						
0837				F			0060						
0838				G					C	16	K		
0839				H			0072						
0840				J									GROUND
0841				K			0344						
0842				L			0386						
0843				M					C	09	C		
0844				N					TB - 15 - 5				#24 AWG (BRN)
0845				P			0442						
0846				Q			0061						
0847				R									

ENG. CHANGE NO.	89	100	124	1188							
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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: B26-TRANSDUCER OSC.
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0848		B	26	A									+5 VOLTS
0849				B									
0850				C									
0851				D									
0852				E									
0853				F									
0854				G									
0855				H									
0856				J									GROUND
0857				K									
0858				L									
0859				M			0397						
0860				N									
0861				P									
0862				Q									+18 VOLTS
0863				R									

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Peripheral Systems Corporation
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TITLE WIRE TAB BACK PANEL

LOC/NAME: B27-SIGNAL PADDLE BOARD

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0864		B	27	A			0115						
0865				B			0117						
0866				C			0118						
0867				D			0123						
0868				E			0125						
0869				F			0562						
0870				G			0564						
0871				H			0565						
0872				J									GROUND
0873				K					C	07	C		
0874				L			0570						
0875				M			0508						
0876				N			0501						
0877				P			0500						
0878				Q					C	07	F		
0879				R			0509						

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: B28-SIGNAL PADDLE BOARD

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0880		B	28	A			0274						
0881				B			0276						
0882				C			0278						
0883				D			0280						
0884				E			0284						
0885				F			0286						
0886				G			0519						
0887				H			0521						
0888				J									GROUND
0889				K			0522						
0890				L			0523						
0891				M			0668						
0892				N									
0893				P			0220						
0894				Q			0096						
0895				R									WRT COAX SHIELD TO C28B

ENG. CHANGE NO.	89	190	1188								
DATE	5-21-68	9-5-68	7/30/70								

WIRE TABULATIONS

RELEASED FOR ASSY 200485

DWG NO. 008048

SHEET 57 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C01-18/-3 VOLT REGULATOR

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0896		C	01	A									
0897				B									
0898				C									
0899				D									
0900				E					R7-LOCATED ON SIDE OF CARD FILE (#20 AWG)				
0901				F					R7-LOCATED ON SIDE OF CARD FILE (#20 AWG)				
0902				G									
0903				H									
0904				J									GROUND
0905				K									
0906				L									
0907				M									
0908				N									
0909				P									
0910				Q									
0911				R									

ENG. CHANGE NO.	89	1188									
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C01

WIRE TABULATIONS

RELEASED FOR ASSY 200485

DWG NO. 008048

SHEET 58 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C02-+18/+5 VOLT REGULATOR

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0912		C	02	A									+5 VOLTS
0913				B									
0914				C									+18 VOLTS
0915				D					R8	LOCATED ON SIDE OF CARD FILE (#20 AWG)			+18 VOLTS
0916				E									
0917				F					R8	LOCATED ON SIDE OF CARD FILE (#20 AWG)			
0918				G									
0919				H									
0920				J									GROUND
0921				K									
0922				L									
0923				M									
0924				N									
0925				P									
0926				Q									
0927				R									

ENG. CHANGE NO.	89	1188										
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WIRE TABULATIONS

RELEASED FOR ASSY
200485

DWG NO. 008048
SHEET 59 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C03-TIE POINTS FOR FILE
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0928		C	03	A									+5 VOLTS
0929				B			0438						
0930				C			0572						
0931				D									
0932				E									
0933				F			0453						
0934				G									
0935				H									
0936				J									GROUND
0937				K			0457						
0938				L			0458						
0939				M									
0940				N					C	07	L		
0941				P			0222						
0942				Q									
0943				R									

ENG. CHANGE NO.	89	133	135	1188							
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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C04-SIGNAL CONDITIONER

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0944		C	04	A									+5 VOLTS
0945				B									
0946				C									
0947				D									
0948				E									
0949				F			0058						
0950				G			0052						
0951				H			0051						
0952				J									GROUND
0953				K			0054						
0954				L									
0955				M									
0956				N									
0957				P									
0958				Q									+18 VOLTS
0959				R									-18 VOLTS

ENG. CHANGE NO.	89	1188										
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WIRE TABULATIONS

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

FROM						WIRE LENGTH	TO					LOC/NAME: C05-AC/DC SAFETY SECTION:	
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
0960		C	05	A									+5 VOLTS
0961				B									
0962				C					C	13	N		
0963				D									
0964				E					C	15	N		
0965				F									
0966				G					C	08	R		
									C	12	Q		
0967				H			0053						
0968				J									GROUND
0969				K			0061						
0970				L									
0971				M			0569						
0972				N									
0973				P			0222						
0974				Q									
0975				R									

ENG. CHANGE NO.	89	100	124	135	1188						
DATE	5-21-68	6-7-68	6-25-68	6-19-68	7/30/70						

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WIRE TABULATIONS

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200485

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SHEET 62 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C06-INVERTERS
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
0976		C	06	A									+5 VOLTS
0977				B					C	06	P		
									C	21	B		
0978				C					C	06	N		
									C	06	R		
0979				D									
0980				E									
0981				F									
0982				G									
0983				H									
0984				J									GROUND
0985				K									
0986				L									
0987				M									
0988				N			0978						
0989				P			0977						
0990				Q					C	11	F		
									C	22	B		
0991				R			0978						

ENG. CHANGE NO.	89	190	1188								
DATE	5-21-68	10-2-68	7/30/70								

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WIRE TABULATIONS

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260485

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SHEET 63 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

FROM						WIRE LENGTH	TO					LOC/NAME: C07-LAMP DRIVERS SECTION:	
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
0992		C	07	A									+5 VOLTS
0993				B					C	11	Q		
									C	13	Q		
									C	15	P		
0994				C			0873						
0995				D			0364						
0996				E			0454						
0997				F			0878						
0998				G			0569						
0999				H									
1000				J									GROUND
1001				K			0061						
1002				L			0940						
1003				M									
1004				N									
1005				P									
1006				Q									
1007				R									

ENG. CHANGE NO.	89	190	1188								
DATE	5-21-68	9-5-68	7/30/70								

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WIRE TABULATIONS

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C08-INVERTERS

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
1008		C	08	A									+5 VOLTS
1009				B			0087						
1010				C			0507						
1011				D					C	12	C		
1012				E			0221						
1013				F					C	13	K		
1014				G			0665						
1015				H			0387						
1016				J									GROUND
1017				K			0240						
1018				L			0091						
1019				M			0087						
1020				N					C	16	E		
1021				P			0103						
1022				Q					C	09	G		
1023				R			0966						

ENG. CHANGE NO.	89	190	1188								
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WIRE TABULATIONS

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C09-SEEK GATING II

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
1024		C	09	A									+5 VOLTS
1025				B									
1026				C			0843						
1027				D			0067						
1028				E									
1029				F									
1030				G			1022						
1031				H			0385						
1032				J									GROUND
1033				K									
1034				L					C	10	F		
1035				M			0052						
1036				N			0091						
1037				P			0379						
1038				Q									
1039				R									

ENG. CHANGE NO.	89	190	1188								
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Peripheral Systems Corporation
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TITLE WIRE TAB BACK PANEL

LOC/NAME: C10-FIRST SEEK GATING
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
1040		C	10	A									+5 VOLTS
1041				B			0050						
1042				C			0503						
1043				D					C	16	R		
1044				E			0379						
1045				F			1034						
1046				G			0062						
1047				H			0388						
1048				J									GROUND
1049				K			0132						
1050				L			0052						
1051				M									
1052				N			0053						
1053				P			0083						
1054				Q					A	05	L		
									C	11	L		
1055				R			0053						

ENG. CHANGE NO.	89	100	124	1188							
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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C11-CYLINDER ADDRESS REG.

SECTION: GATING

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
1056		C	11	A									+5 VOLTS
1057				B			0094						
1058				C			0053						
1059				D									
1060				E			0507						
1061				F			0990						
1062				G			0086						
1063				H					C	23	C		
1064				J									GROUND
1065				K			0743						
1066				L			1054						
1067				M					C	23	D		
1068				N					C	23	E		
1069				P					C	24	D		
1070				Q			0993						
1071				R					C	16	P		
									C	20	L		

ENG. CHANGE NO.	89	124	1188								
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WIRE TABULATIONS

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C12-STATUS GATING

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
1072		C	12	A									+5 VOLTS
1073				B					C	23	G		
1074				C			1011						
1075				D					C	23	F		
1076				E			0354						
1077				F			00611						
1078				G			0498						
1079				H			0091						
1080				J									GROUND
1081				K			0503						
1082				L			0497						
1083				M			0507						
1084				N					C	24	E		
1085				P					C	24	F		
1086				Q			0966						
1087				R					C	24	G		

ENG. CHANGE NO.	89	194	1188								
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WIRE TABULATIONS

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C13-WRITE/ERASE CURRENT

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
1088		C	13	A									+5 VOLTS
1089				B					C	13	J		
1090				C			0096						
1091				D			0095						
1092				E			0221						
1093				F					C	15	L		
1094				G			0665						
1095				H			0214						
1096				J			1089						GROUND
1097				K			1013						
1098				L			0096						
1099				M					C	15	M		
1100				N			0962						
1101				P					C	17	M		
1102				Q			0993						
1103				R			0211						

ENG. CHANGE NO.	89	1188									
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WIRE TABULATIONS

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C14
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
1104		C	14	A									+5 VOLTS
1105				B									
1106				C									
1107				D									
1108				E									
1109				F									
1110				G									
1111				H									
1112				J									GROUND
1113				K									
1114				L									
1115				M									
1116				N									
1117				P									
1118				Q									
1119				R									

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WIRE TABULATIONS

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SHEET 71 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C15-CONTROL SAFETY
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
1120		C	15	A									+5 VOLTS
1121				B					C	28	F		
1122				C			0095						
1123				D			0214						
1124				E			0087						
1125				F			0535						
1126				G			0388						
1127				H			0365						
1128				J									GROUND
1129				K			0527						
1130				L			1093						
1131				M			1099						
1132				N			0964						
1133				P			0993						
1134				Q									
1135				R			0505						

ENG. CHANGE NO.	89	100	1188								
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WIRE TABULATIONS

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DWG NO. 006048

SHEET 72 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C16-SELECT GATING

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
1136		C	16	A									+6 VOLTS
1137				B			0551						
1138				C			0556						
1139				D			0093						
1140				E			1020						
1141				F									
1142				G			0056						
1143				H			0380						
1144				J									GROUND
1145				K			0838						
1146				L									
1147				M		3			C	20	M		
1148				N			0505						
1149				P			1071						
1150				Q			0585						
1151				R			1043						

ENG. CHANGE NO.	89	1188									
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WIRE TABULATIONS

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C17-CONTROL GATING
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
1152		C	17	A									
1153				B			0826						
1154				C			0139						
1155				D			0379						
1156				E			0582						
1157				F									
1158				G			0551						
1159				H			0135						
1160				J									GROUND
1161				K			0050						
1162				L			0138						
1163				M			1101						
1164				N			0585						
1165				P			0535						
1166				Q			0586						
1167				R			0095						

ENG. CHANGE NO.	89	1188									
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WIRE TABULATIONS

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SHEET 74 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C18-LINE RECEIVER

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
1168		C	18	A									+5 VOLTS
1169				B					C	27	F		
1170				C					C	27	E		
1171				D					C	27	D		
1172				E					C	27	C		
1173				F					C	27	B		
1174				G					C	27	A		
1175				H			0138						
1176				J									GROUND
1177				K			0139						
1178				L			0550						
1179				M			0582						
1180				N			0585						
1181				P			0586						
1182				Q									
1183				R									

ENG. CHANGE NO.	89	1188									
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WIRE TABULATIONS

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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C19-LINE RECEIVER

SECTION:

FROM						WIRE LENGTH	TO						
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
1184		C	19	A									+5 VOLTS
1185				B									
1186				C									
1187				D									
1188				E					C	27	P		
1189				F					C	27	N		
1190				G									
1191				H									
1192				J									GROUND
1193				K									
1194				L									
1195				M			0499						
1196				N			0502						
1197				P									
1198				Q									
1199				R									

ENG. CHANGE NO.	89	1188									
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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME C20-TERMINATED LINE

SECTION RECEIVER

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
1200		C	20	A									+5 VOLTS
1201				B					C	27	L		
1202				C					C	27	K		
1203				D					C	28	M		
1204				E					C	27	M		
1205				F					C	27	H		
1206				G					C	27	G		
1207				H			0104						
1208				J									GROUND
1209				K			0093						
1210				L			1071						
1211				M			1147						
1212				N			0136						
1213				P			0135						
1214				Q									
1215				R									

ENG. CHANGE NO.	89	1188									
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Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C21-LINE DRIVER
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
1216		C	21	A									+5 VOLTS
1217				B			0977						
1218				C			0130						
1219				D			0134						
1220				E			0143						
1221				F			0141						
1222				G			0577						
1223				H									
1224				J									GROUND
1225				K									
1226				L					C	26	E		
1227				M					C	26	D		
1228				N					C	26	C		
1229				P					C	26	B		
1230				Q					C	26	A		
1231				R									

ENG. CHANGE NO.	89	124	1188								
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RELEASED FOR ASSY
220485

DWG NO. 008048
SHEET 78 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C22-LINE DRIVER
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
1232		C	22	A									+5 VOLTS
1233				B			0990						
1234				C									
1235				D									
1236				E			0581						
1237				F			0590						
1238				G			0588						
1239				H									
1240				J									GROUND
1241				K									
1242				L					C	26	H		
1243				M					C	26	G		
1244				N					C	26	F		
1245				P									
1246				Q									
1247				R									

ENG. CHANGE NO.	89	124	1188								
DATE	5-21-68	6-25-68	7/30/70								

PSC 030 1-69

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WIRE TABULATIONS

RELEASED FOR ASSY 200485

DWG NO. 008048

SHEET 79 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C23-LINE DRIVER

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
1248		C	23	A									+5 VOLTS
1249				B									
1250				C			1063						
1251				D			1067						
1252				E			1068						
1253				F			1075						
1254				G			1073						
1255				H									
1256				J									GROUND
1257				K									
1258				L					C	27	R		
1259				M					C	26	M		
1260				N					C	26	Q		
1261				P					C	28	K		
1262				Q					C	26	K		
									C	28	R		
1263				R									

ENG. CHANGE NO.	89	100	1188								
DATE	5-21-68	6-7-68	7/30/70								

PSC 030 1-69

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WIRE TABULATIONS

RELEASED FOR ASSY
200485

DWG NO. 006048
SHEET 80 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

FROM						WIRE LENGTH	TO					LOC/NAME: C24-LINE DRIVER SECTION:	
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
1264		C	24	A									+5 VOLTS
1265				B									
1266				C			0829						
1267				D			1069						
1268				E			1084						
1269				F			1085						
1270				G			1087						
1271				H									
1272				J									GROUND
1273				K									
1274				L					C	26	L		
1275				M					C	26	P		
1276				N					C	28	L		
1277				P					C	26	N		
1278				Q					C	26	R		
1279													

ENG. CHANGE NO.	89	1188									
DATE	5-21-68	7/30/70									

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WIRE TABULATIONS

RELEASED FOR ASSY
200485

DWG NO. 008048
SHEET 81 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C25
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
1280		C	25	A									+5 VOLTS
1281				B									
1282				C									
1283				D									
1284				E									
1285				F									
1286				G									
1287				H									
1288				J									GROUND
1289				K									
1290				L									
1291				M									
1292				N									
1293				P									
1294				Q									
1295				R									

ENG. CHANGE NO.	89	1188									
DATE	5-21-68	7/30/70									

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WIRE TABULATIONS

RELEASED FOR ASSY
200485

DWG NO. 008048
SHEET 82 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C26-SIGNAL PADDLE BOARD
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
1296		C	26	A			1230						
1297				B			1229						
1298				C			1228						
1299				D			1227						
1300				E			1226						
1301				F			1244						
1302				G			1243						
1303				H			1242						
1304				J									GROUND
1305				K			1262						
1306				L			1274						
1307				M			1259						
1308				N			1277						
1309				P			1275						
1310				Q			1260						
1311				R			1278						

ENG. CHANGE NO.	89	1188									
DATE	5-21-68	7/30/70									

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WIRE TABULATIONS

RELEASED FOR ASSY 200485

DWG NO. 008048

SHEET 83 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

FROM						WIRE LENGTH	TO					LOC/NAME: C27-SIGNAL PADDLE BOARD SECTION:	
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN	LINE LABEL	REMARKS
1312		C	27	A			1174						
1313				B			1173						
1314				C			1172						
1315				D			1171						
1316				E			1170						
1317				F			1169						
1318				G			1206						
1319				H			1205						
1320				J									GROUND
1321				K			1202						
1322				L			1201						
1323				M			1204						
1324				N			1189						
1325				P			1188						
1326				Q									
1327				R			1258						

ENG. CHANGE NO.	89	1188									
DATE	5-21-68	7/30/70									

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WIRE TABULATIONS

RELEASED FOR ASSY 200485

DWG NO. 008048

SHEET 84 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: C28D.C. PADDLE BOARD
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
1328		C	28	A									RD COAX SHIELD TO C28C
1329				B			0895						WRT COAX SHIELD TO C28D
1330				C					C	28	D		
									C	28	G		
									C	28	H		
									C	28	J		
									C	28	N		
									C	28	P		
									C	28	Q		
1331				D			01330						
1332				E									
1333				F			1121						
1334				G			1330						
1335				H			1330						
1336				J			1330						GROUND
1337				K			1261						
1338				L			1276						
1339				M			1203						
1340				N			1330						
1341				P			1330						
1342				Q			1330						
1343				R			1262						

ENG. CHANGE NO.	89	229	1188								
DATE	6-21-68	10-14-68	7/30/70								

PSC 030 1-69

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WIRE TABULATIONS

RELEASED FOR ASSY 200485

DWG NO. 008048

SHEET 85 OF 86

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: BACK PANEL VOLTAGE WIRING

SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
1344		A	01	A					A	28	A		SOLID BUSS JUMPER
1345		B	01	A					B	26	A		
1346		C	02	A					C	24	A		
1347		A	16	R					A	18	R		
1348		A	16	Q					A	18	A		
1349		B	16	R					B	18	R		
1350		B	16	Q					B	18	Q		
1351		C	21	R					C	24	R		
1352		C	21	K					C	24	K		SOLID BUSS JUMPER
1353		C	01	D					A	14	R		NO. 24 SOLID
									A	16	R		
1354		C	01	C					B	14	R		
									B	16	R		
1355		C	01	E					C	21	R		
1356		C	02	A									
1357		C	01	C					C	01	D		
									C	01	E		
1358		C	01	F					C	01	G		
									C	01	H		
1359		C	01	J					C	01	K		
1360		C	02	C					C	02	D		
									C	02	E		
									C	04	Q		
									C	05	Q		
									C	07	Q		
									C	09	Q		
									B	08	Q		
									A	04	Q		
									A	08	Q		
									A	14	Q		
									A	16	Q		
									A	17	Q		
									A	22	Q		
									A	23	Q		NO. 24 SOLID

ENG. CHANGE NO.	89	1188									
DATE	5-21-68	7/30/70									

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WIRE TABULATIONS

RELEASED FOR ASSY
200485

DWG NO. 008048
SHEET 86 OF 83

Peripheral Systems Corporation
a subsidiary of MEMOREX CORPORATION

TITLE WIRE TAB BACK PANEL

LOC/NAME: BACK PANEL VOLTAGE WIRING
SECTION:

FROM						WIRE LENGTH	TO					LINE LABEL	REMARKS
SEQUENCE	FILE	ROW	COLUMN	PIN			REFERENCE	FILE	ROW	COLUMN	PIN		
									A	25	Q		NO. 24 SOLID
									A	27	Q		
									A	28	Q		
									B	26	Q		
									B	23	Q		
									B	16	Q		
									B	14	Q		
									B	05	P		
1361		C	02	F					C	02	G		
									C	02	H		
1362		C	02	J					C	02	K		
1363		A	04	R					A	28	R		
									A	27	P		
									A	25	R		
									A	22	R		
									A	17	R		
									B	23	R		
									C	04	R		
									C	05	R		
									C	09	R		
1364		C	05	A					B	05	A		
									A	05	A		
1365		C	06	A					B	06	A		
									A	06	A		
1366		C	07	A					B	07	A		NO. 24 SOLID

ENG. CHANGE NO.	89	190	225	1188							
DATE	5-21-68	10-2-68	10-14-68	7/30/70							

PSC 030 1-69