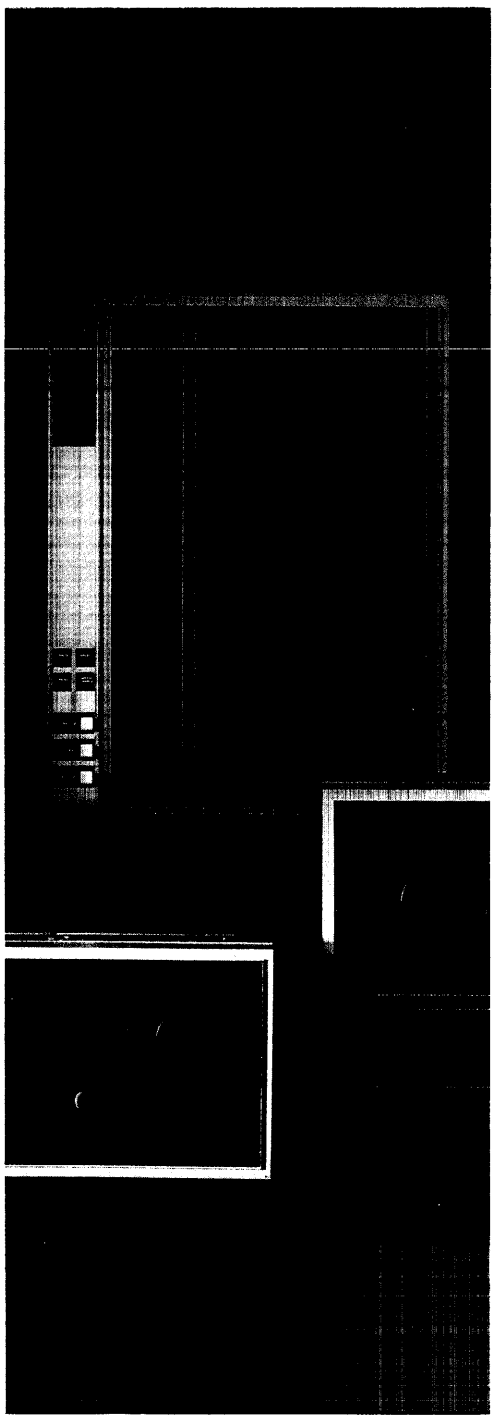
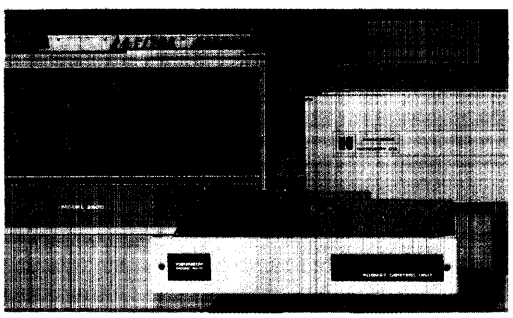
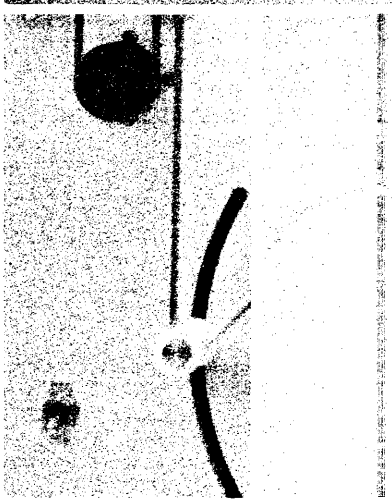
Operation and maintenance manual

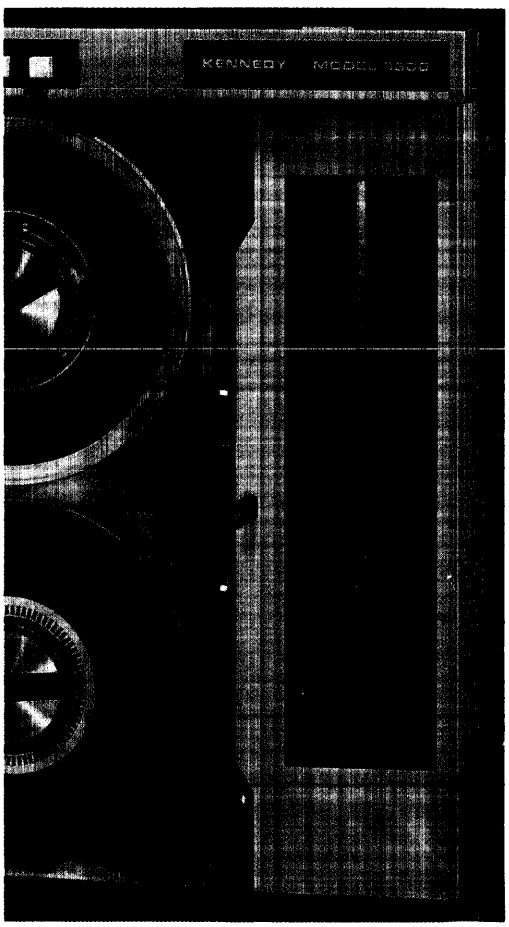
KENNEDY CO.

Model 1600/360
Magnetic Tape Recorder









SECTION I

GENERAL INFORMATION

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GENERAL INFORMATION

PRINCIPLES OF OPERATION

Kennedy Incremental Recorders prepare IBM compatible tape from sources of data operating at random or non-standard rates. This means that tapes recorded can be mounted on standard computer tape drives and read as though they had been written by the computer itself.

All the characteristics of computer written tape are duplicated. Data characters are evenly spaced as required by the computer, parity bits are generated internally and properly placed on tape and gaps of standard lengths are inserted on command.

Incremental recorders are capable of producing evenly spaced data even though the data source may be operating in a sporadic or random manner. Continuous, or start-stop tape drives, cannot do this without use of a large and costly memory.

As an example, consider the problem of recording the output of an electric typewriter operated manually. Keys are struck with variable rapidity and if the recording tape were in smooth motion, the variability would result in uneven spacing on the tape. Even if the operator were capable of absolutely consistent typing, time for carriage return would differ from key stroke time.

In an incremental recorder, each character is recorded upon command. The tape then steps one increment--which may be 0.005" for 200 BPI; 0.0018" for 556 BPI; or 0.0012" for 800 BPI--then stops and awaits the next step command, thus the data is evenly recorded assuming that the maximum asynchronous stepping rate of the recorder has not been exceeded. The incremental recorder has numerous advantages over other methods of performing this function:

1. The recorder is an inexpensive device because tape speeds are very low.

2. No expensive memory is required.

3. The recorder is mechanically simple with almost no moving parts to fail--highly reliable.

4. Tapes produced are immediately usable on computers without conversion.

Stepping Mechanism

The heart of the incremental recorder is its stepping mechanism which must be accurate and reliable. Not only must its step size be accurate, but there must be no possibility that the step is not accurately transmitted to the tape itself. When the drive is stationary, as

it may be for long periods of time, there must be no possibility that the tape may creep or otherwise move.

All these requirements together with the obvious requirement for high asynchronous stepping rates are met by the stepper motor drive used in Kennedy Incremental Recorders. The stepping motor itself is a special ultra-high speed, variable reluctance motor which moves 15^{o} per step. Each position of the motor is strongly detented magnetically. This 15^{o} step motion is reduced through precision gearing to the proper angular motion to advance the tape the required increment.

Tape is driven by a capstan and pinch roller in such a way as to make slippage a virtual impossibility at any speed.

The drive mechanisms on all standard Kennedy Incremental Recorders are identical--the only variation being in step size as determined by gear ratio and capstan diameter.

Electronics

Ease of application has been the primary consideration in design of the recorder interface. Internally, recorder electronics are all solid state, silicon. Integrated circuits are used in all appropriate applications.

INCREMENTAL RECORDING SYSTEMS

A block diagram is shown in Figure 1-1 of a typical Kennedy Incremental Recorder illustrating its principal components. It will be noted that electronics may be divided into sections having inter-related but separate functions.

1. Parity-Write Amplifier section produces the actual recording on tape.

2. Gap generation system develops the drive signals necessary to insert gaps.

3. Control section provides circuits operable by pushbuttons and remote signals to control tape motion.

4. Stepper drive system receives step commands and produces signals which cause the stepper motor to increment.

Each of these sections will be shown in detail in this book.

In addition to the basic system shown, there are other functions which may be added for special purposes. They do not basically alter the system but add to its complexity.

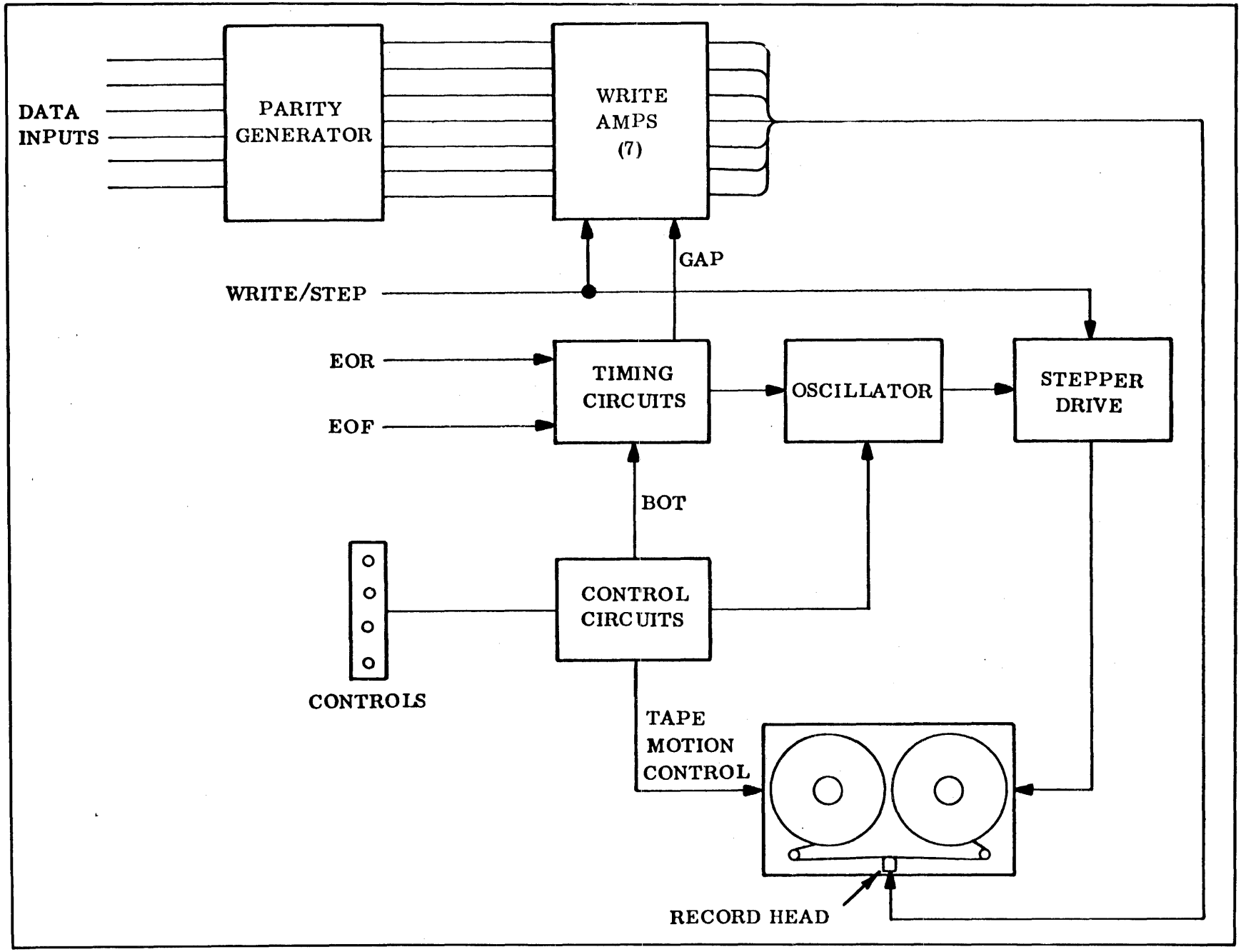


Figure 1-1. Incremental Recording System

DIGITAL MAGNETIC RECORDING

To record digital data on magnetic tape it is necessary, in some way, to magnetize the tape discretely to indicate binary ones and zeros. Of several different schemes, the IBM NRZI system has been most widely adopted. As shown in Figure 1-2, ones are represented by transitions between saturation magnetism (+ and -) on the tape.

Since magnetic heads respond to the rate of change of flux but not to steady flux, when tape is read output waveforms, such as those shown in Figure 1-2, are produced. No change in flux represents a binary zero and no voltage is recovered from the head.

In order to be usable as a recording scheme, the NRZI system requires at least one bit to be recorded for all characters; otherwise, in an all zero character there would be no indication that a character was supposed to be in that location.

NRZI recording is implemented by driving current through the head winding in a direction determined by a flip-flop which toggles for each one to be recorded.

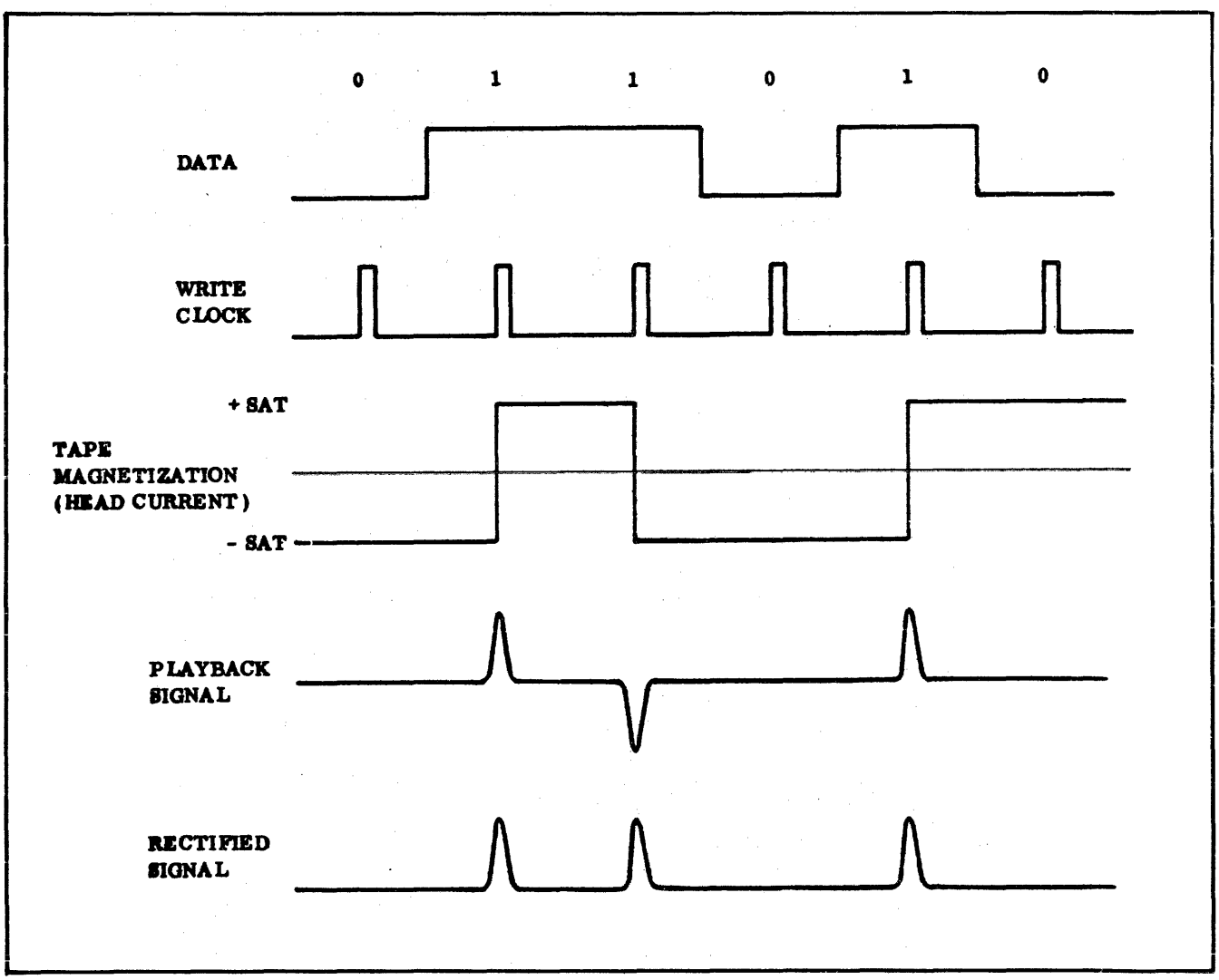
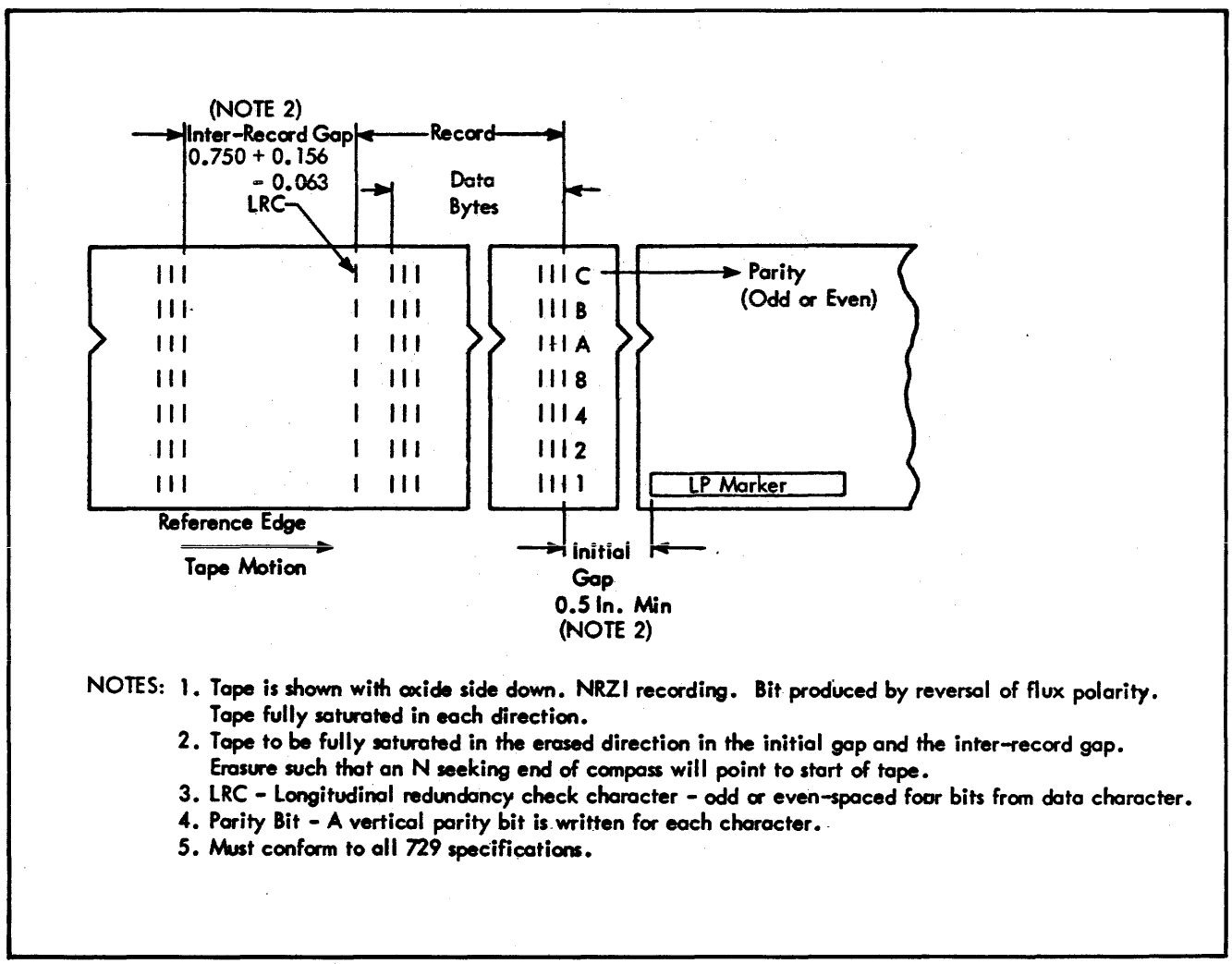


Figure 1-2. NRZ Waveforms

In a seven-track system, as shown in Figure 1-3, six of the tracks are data channels while the seventh is the parity channel. Parity may be either odd or even which is to say that bits may be added in the C track to make the sum of the bits in the character either odd or even. Even parity is used with BCD coding while odd parity is used when operating in the binary mode.



NOTES:
1. Tape is shown with oxide side down. NRZI recording. Bit produced by reversal of flux polarity. Tape fully saturated in each direction.
2. Tape to be fully saturated in the erased direction in the initial gap and the inter-record gap. Erasure such that an N seeking end of compass will point to start of tape.
3. LRC - Longitudinal redundancy check character - odd or even-spaced four bits from data character.
4. Parity Bit - A vertical parity bit is written for each character.
5. Must conform to all 729 specifications.

Figure 1-3. Data Format - Seven Track

BCD

IBM seven-channel BCD code is shown in Figure 1-4. It will be noted that there are 63 combinations of the 6-data bits available to stand for numerics, letters, and special symbols. Actually, a somewhat larger variety of symbols may be used, depending upon the print chain, by leaving out some unused symbols and substituting others.

Collating Sequence	Graphics		Eight - Bit Code								BCD					
	8 Bit	BCD	0	1	2	3	4	5	6	7	B	A	8	4	2	1
00	blank	blank	0	1	0	0	0	0	0	0	0	0	0	0	0	0
01	.	.	0	1	0	0	1	0	1	1	1	1	1	0	1	1
02	←	¤)	0	1	0	0	1	1	0	0	1	1	1	1	0	0
03	(	[	0	1	0	0	1	1	0	1	1	1	1	1	0	1
04	+	<	0	1	0	0	1	1	1	0	1	1	1	1	1	0
05	GM	GM	0	1	0	0	1	1	1	1	1	1	1	1	1	1
06	&	& +	0	1	0	1	0	0	0	0	1	1	0	0	0	0
07	$	$	0	1	0	1	1	0	1	1	1	0	1	0	1	1
08	*	*	0	1	0	1	1	1	0	0	1	0	1	1	0	0
09	)	]	0	1	0	1	1	1	0	1	1	0	1	1	0	1
10	;	;	0	1	0	1	1	1	1	0	1	0	1	1	1	0
11	MC	MC	0	1	0	1	1	1	1	1	1	0	1	1	1	1
12	-	-	0	1	1	0	0	0	0	0	1	0	0	0	0	0
13	/	/	0	1	1	0	0	0	0	1	0	1	0	0	0	1
14	,	,	0	1	1	0	1	0	1	1	0	1	1	0	1	1
15	%	% (	0	1	1	0	1	1	0	0	0	1	1	1	0	0
16	WS	WS	0	1	1	0	1	1	0	1	0	1	1	1	0	1
17	↓	\	0	1	1	0	1	1	1	0	0	1	1	1	1	0
18	SM	SM	0	1	1	0	1	1	1	1	0	1	1	1	1	1
19	↻	↻	0	1	1	1	1	0	1	0	0	1	0	0	0	0
20	↑	↑ =	0	1	1	1	1	0	1	1	0	0	1	0	1	1
21	@	@ '	0	1	1	1	1	1	0	0	0	0	1	1	0	0
22	▽	:	0	1	1	1	1	1	0	1	0	0	1	1	0	1
23	=	>	0	1	1	1	1	1	1	0	0	0	1	1	1	0
24	TM	TM	0	1	1	1	1	1	1	1	0	0	1	1	1	1
25	ð	ð	1	1	0	0	0	0	0	0	1	1	1	0	1	0
26	A	A	1	1	0	0	0	0	0	1	1	1	0	0	0	1
27	B	B	1	1	0	0	0	0	1	0	1	1	0	0	1	0
28	C	C	1	1	0	0	0	0	1	1	1	1	0	0	1	1
29	D	D	1	1	0	0	0	1	0	0	1	1	0	1	0	0
30	E	E	1	1	0	0	0	1	0	1	1	1	0	1	0	1
31	F	F	1	1	0	0	0	1	1	0	1	1	0	1	1	0
32	G	G	1	1	0	0	0	1	1	1	1	1	0	1	1	1
33	H	H	1	1	0	0	1	0	0	0	1	1	1	0	0	0
34	I	I	1	1	0	0	1	0	0	1	1	1	1	0	0	1
35	ð	ð	1	1	0	1	0	0	0	0	1	0	1	0	1	0
36	J	J	1	1	0	1	0	0	0	1	1	0	0	0	0	1
37	K	K	1	1	0	1	0	0	1	0	1	0	0	0	1	0
38	L	L	1	1	0	1	0	0	1	1	1	0	0	0	1	1
39	M	M	1	1	0	1	0	1	0	0	1	0	0	1	0	0
40	N	N	1	1	0	1	0	1	0	1	1	0	0	1	0	1
41	O	O	1	1	0	1	0	1	1	0	1	0	0	1	1	0
42	P	P	1	1	0	1	0	1	1	1	1	0	0	1	1	1
43	Q	Q	1	1	0	1	1	0	0	0	1	0	1	0	0	0
44	R	R	1	1	0	1	1	0	0	1	1	0	1	0	0	1
45	RM	RM	1	1	1	0	0	0	0	0	0	1	1	0	1	0
46	S	S	1	1	1	0	0	0	1	0	0	1	0	0	1	0
47	T	T	1	1	1	0	0	0	1	1	0	1	0	0	1	1
48	U	U	1	1	1	0	0	1	0	0	0	1	0	1	0	0
49	V	V	1	1	1	0	0	1	0	1	0	1	0	1	0	1
50	W	W	1	1	1	0	0	1	1	0	0	1	0	1	1	0
51	X	X	1	1	1	0	0	1	1	1	0	1	0	1	1	1
52	Y	Y	1	1	1	0	1	0	0	0	0	1	1	0	0	0
53	Z	Z	1	1	1	0	1	0	0	1	0	1	1	0	0	1
54	0	0	1	1	1	1	0	0	0	0	0	0	1	0	1	0
55	1	1	1	1	1	1	0	0	0	1	0	0	0	0	0	1
56	2	2	1	1	1	1	0	0	1	0	0	0	0	0	1	0
57	3	3	1	1	1	1	0	0	1	1	0	0	0	0	1	1
58	4	4	1	1	1	1	0	1	0	0	0	0	0	1	0	0
59	5	5	1	1	1	1	0	1	0	1	0	0	0	1	0	1
60	6	6	1	1	1	1	0	1	1	0	0	0	0	1	1	0
61	7	7	1	1	1	1	0	1	1	1	0	0	0	1	1	1
62	8	8	1	1	1	1	1	0	0	0	0	0	1	0	0	0
63	9	9	1	1	1	1	1	0	0	1	0	0	1	0	0	1

Figure 1-4. Eight Bit Code - BCD Relations

Binary Mode

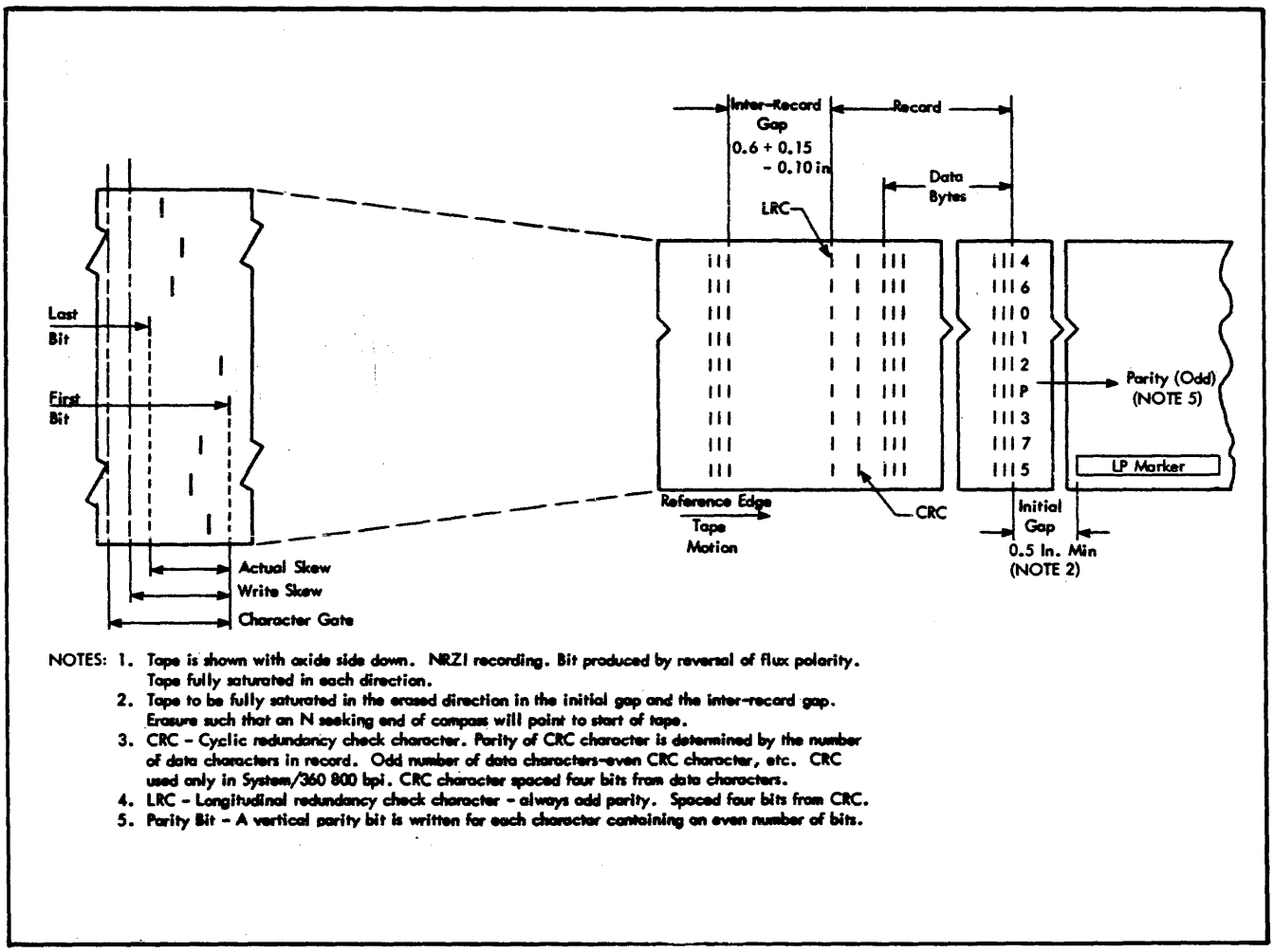
In the binary mode, the computer is programmed to accept tape characters as binary numbers. This mode obviously is useful only with straight numeric input.

Thus, a six-bit character can represent a six-digit binary number, or 0-63. By using more than one character, larger numbers may be represented. In some cases this results in considerable saving in space on the tape and in computer time. For example, the number 56 would require two character spaces in BCD but only one in binary. Obviously, odd parity must be used because six zeros can be a perfectly valid portion of a binary number.

Nine-track Coding

Nine-track tape, as used in IBM System/360, uses a modified ASCII code also shown in Figure 1-5. Parity in the nine-track 800 BPI system is always odd.

Operation in binary mode is possible with proper programming. An interesting possibility is recording two 4-bit numerics per byte with consequent doubling of effective data rate.



NOTES:
1. Tape is shown with oxide side down. NRZI recording. Bit produced by reversal of flux polarity. Tape fully saturated in each direction.
2. Tape to be fully saturated in the erased direction in the initial gap and the inter-record gap. Erasure such that an N seeking end of compass will point to start of tape.
3. CRC - Cyclic redundancy check character. Parity of CRC character is determined by the number of data characters in record. Odd number of data characters-even CRC character, etc. CRC used only in System/360 800 bpi. CRC character spaced four bits from data characters.
4. LRC - Longitudinal redundancy check character - always odd parity. Spaced four bits from CRC.
5. Parity Bit - A vertical parity bit is written for each character containing an even number of bits.

Figure 1-5. Data Format - Nine Track

Longitudinal Parity

In writing blocks on tape, it is necessary to return to the reference magnetic condition in the gaps if records are to be rewritten at any future time. Otherwise, the direction for any track would not be known and spurious characters would result. In returning to reference state those tracks which are in the opposite state, spurious characters are also generated. This difficulty has been cleverly converted to an asset in the NRZI system by accurately locating the "spurious" character and using it as a check.

Since it started and returned to reference level, each track must have had an even number of transitions. The number of transitions are counted and if the result is odd, an error is indicated.

The Longitudinal Check Character, as it is called, is spaced four or five character spaces from the end of the block so that it will not be interpreted as data.

Other Checks

In the newer IBM transports built for 800 BPI, nine-track recording, another check, called "Cyclic Redundancy Check", is included. This check has the ability to direct correction of a certain limited class of errors. Kennedy Incremental Recorders built for System 360 compatibility include circuits for generation of the CRC.

Additionally, in the nine-track system there is a "Lost Character Check" which implements the error correction routine. In this check a character is expected to have been read within 15 clock times of the last. If it has not been read in 17 clock times, an error is flagged.

This requirement places fairly stringent criteria on character spacing accuracy. While not used in the seven-track 2400 series transport, lost character detection circuits are retained placing the same restrictions on spacing as in the nine-track system.

FLUX CHECK™

Flux Check™ is a system of checking data as it is written on tape. A true read-after-write check, it uses only one gap for both operations. If a character is incorrectly written for any reason, including tape flaws, an error signal is produced before another character is due to be written.

Available as an option on nearly all Kennedy Incremental Recorders, Flux Check™ is the ultimate safeguard against lost data.

While it may be argued with perfect logic that good tape operating in a good machine will not have any errors recorded on it, the human factor cannot be entirely eliminated, and once precious data is lost it may be impossible to replace.

Basic principles of Flux Check™ recording are shown in Figure 1-6. Magnetically neutral tape is passed over the head which is built with a 0.006" gap--wider than the widest increment, 0.005" at 200 BPI. The head has two windings, a write winding and a read winding. Short pulses of current in the head magnetize a portion of the tape as wide as the gap. Polarity of the pulses is controlled by a flip-flop in the Flux Check™ Write Amplifier.

If zeros are being recorded, pulses are all in the same direction. This produces smooth magnetism on the tape as required for zeros. Polarity of write pulses reverses for ones. After writing, the tape moves, pulling the recorded section out of the gap and inducing a signal in the read windings.

Write pulses are suppressed by the Flux Check™ read amplifiers; but the read signal is amplified and compared on a bit-by-bit basis with the input data. If disagreement is found, an error is signalled.

Time to signal an error does not exceed 1.9 ms. This allows for a maximum operating speed of 500 steps per second, still retaining the ability to locate an erroneous character before the next is recorded.

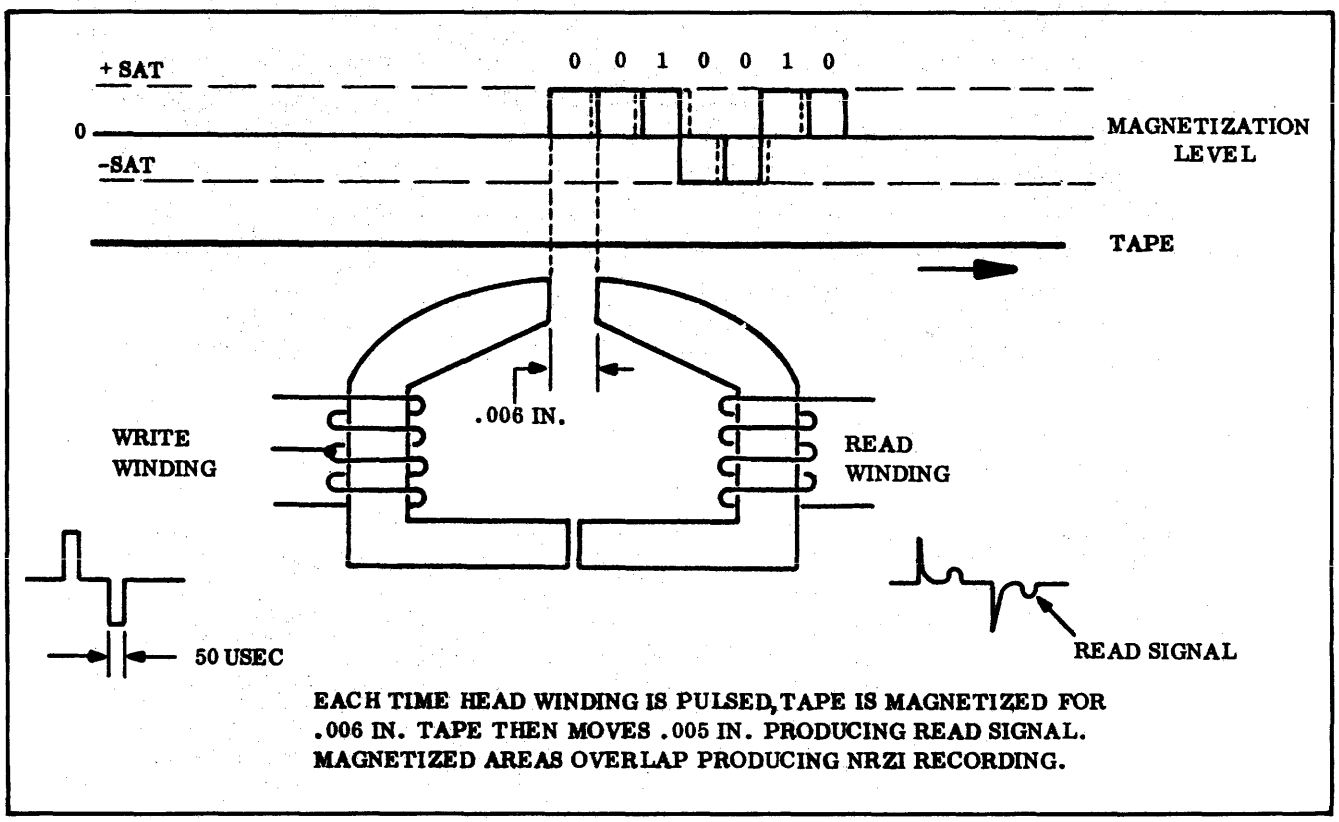


Figure 1-6. Flux Check Recording

READERS

Kennedy Company Incremental Magnetic Recorders may also be equipped for reading as well as writing tape. Model numbers are suffixed by designation as shown in the following examples:

1600R	Incremental Record/Continuous Read
1600IR	Incremental Record/Incremental Read
2059RO	Continuous Read Only

Principles and equipment requirements for the various models are identical or similar and, in many cases, the read portion of the machine is modular to simplify interfacing and construction.

The description in this section is general in nature. Specifics for a particular model may be found in the Performance Specifications section and in the circuit descriptions of the circuit cards used.

File Protect Switch

Kennedy recorders equipped for both reading and writing are also equipped with a File Protect Switch and Indicator Light. This switch detects the presence of the File Protect Ring in the reel of tape mounted on the supply side of the machine. If this flexible ring is removed from the reel, it indicates that the tape must not be written on under any circumstances. This treatment is often reserved for library and program tapes or, in some instances, the ring may be removed immediately after the tape is written to prevent erasure of a tape.

On a machine so equipped it is impossible to select the Write mode in the machine or to write or erase data on tape when the File Protect Ring has been removed from the reel. If an attempt is made to write on a tape which does not have the File Protect Ring in place, the red FILE PROTECT Light will glow either immediately or when the machine goes into Ready, depending on the model, to indicate to the operator that he has made a procedural error. An indication of this is also provided to the interface plug so that external equipment may sense this condition. Machines which are Write Only or Read Only do not have a File Protect Switch.

Controls and Loading Procedure

The controls and loading procedure for a Read machine are identical to those of a Write Only machine. However, when the tape is loaded, no Beginning of Tape gap is inserted. The read head will come to a stop at a point prior to the place where recording began. In other words, it will stop immediately when the Load Point sensor is under the photo cell instead of the customary 3-1/2" after this point.

Interface Connector

On all recent Kennedy Incremental Recorders a separate interface connector is provided for the functions associated with reading. This enables a machine equipped for reading to be directly substituted for a Write Only machine using the same wiring. The read signals do not compromise or affect the normal signals on the connector associated with writing.

Skew Delay

In writing a tape certain tolerances with regard to the gap scatter in the heads, the skew of the head (that is, the failure of the gaps to be absolutely perpendicular to the tape), and other causes can accumulate in tolerances which make it necessary to provide electronic circuitry to compensate for these variables and to assure that the output data is timed correctly. These conditions are aggravated when a tape is written on one machine and read on another which is a normal circumstance. The common method for achieving this is to read each track independently and sense the first "one" that is detected on any track. This is done by connecting the outputs of all of the data tracks into an "OR" gate. The first "one" then triggers a delay which is usually set to be approximately 45% of the prescribed time for one character.

At this time the data in the output register is changed to reflect the new character, and a few microseconds later a Clock pulse is provided to enable strobing this data into the external system. This assures that data is transferred at a time when it is valid and correct and eases the interfacing of the machine to an external system. (On old machines the output register was not provided, and Data pulses and Clock pulses were coincident with each other.)

Gap Detector

Another output provided at the interface connector is the Gap Detector output. In either Incremental Read or Continuous Read machines a Clock pulse should be detected within a prescribed time after a Read/Step or Read command is given. Internal circuitry has been provided to detect whether or not this clock is available within approximately two or three time intervals. If no clock is received within this time, then it follows that the read head must be passing through a gap. This output is called the Gap Detect output and may be used to control stopping of a Continuous machine in the gap.

Longitudinal Check Character

This Gap Detect output is also used internally to inhibit the Clock pulse for the Longitudinal Check Character. The Longitudinal Check Character will appear at the data output terminals and will remain there during the gap until the first character of the succeeding block is detected. However, the Clock pulse for it is deliberately inhibited since, in most simplified systems where a reader of this type is employed, the character is not desired. Where it is required, it may be reconstituted by a simple modification to one of the circuit cards. The factory should be consulted regarding this if it is required.

Error Rates

Maximum error rates are difficult to define. Many variables, such as tape condition, environment, etc., enter the picture. Continuous reading with error rates of less than one error in 10^6 characters is reasonable to expect under ordinary conditions and may be improved several orders of magnitude with reasonable precautions. Incremental reading is much more difficult to implement and is less tolerant of tape imperfections. Therefore, typical error rates may be expected to be slightly higher.

CONTINUOUS READING

On machines equipped for Continuous reading, the tape is run at a fixed speed and should be stopped only in Inter-Record gaps. In most recorders this is done by running the stepper motor at a slewing rate fast enough so that the steps blend together into a smooth continuous motion. This speed is usually 1000 steps per second.

On some machines, such as the 3700 Series, an auxiliary capstan motor is employed to run the tape at a pre-selected speed of up to 30 inches per second. Other machines, such as the 2059 Series, use a servo controlled dc motor system which allows pre-selected tape speeds of 1.5 inches to 6 inches per second. All of these systems have in common the fact that:

1. the tape is running at a pre-selected fixed speed,

2. a data register is filled at a synchronous rate,

3. a Read Clock output is provided to enable strobing out the register into memory or other external devices.

The control of these recorders is relatively simple. A Read Select level is applied followed by a Slew level which will cause the tape to accelerate rapidly to the prescribed speed and run continuously at that speed emitting Data and Clock pulses. When a gap is detected, a signal is available which may be used to control the slew level which should be removed to enable the tape to stop in the desired gap.

INCREMENTAL READING

The Incremental Read feature permits reading of 200 BPI NRZI tapes one character at a time. Standard computer tapes may be read into such low speed devices as typewriters, data sets, plotters, etc. without the necessity of buffering. In operation the machine is given a Read/Step command. The tape advances to the next character (read search) and stops upon having read that character. Output information is held in storage until the next Read/Step command. Read commands may be repeated at rates up to 150 characters per second.

In order to read incrementally, a means must be provided to assure orientation with the information on the tape. The motion of the tape must be such that the head gap falls between characters when the tape comes to a stop. A step size equal to the character spacing cannot be used since density and step size variations will eventually accumulate to a point where information could be lost.

Kennedy Incremental Recorders use a unique method of correcting tape position. The step size, instead of being 0.005" as it is in Incremental Write Only machines, is set at 0.0025". Thus, two steps will be required to move the tape one character space under ideal conditions. However, since magnetic tape does not have sprockets or other mechanical means to assure that the tape is between characters over the recorder gap, a technique is required which will assure that the tape always stops between characters and that it takes the correct number of steps to assure this. While two steps are usually required, one may be adequate or perhaps

three may be necessary. To achieve this an internal oscillator is started when the Read/Step pulse is applied at the interface. The stepper motor then advances the tape. As soon as a character is sensed, the oscillator is cut off and no more pulses are produced and the motor stops. In this way a closed loop system is produced which keeps the tape properly oriented.

Upon entering a blank region of tape, that is, an Inter-Record gap or End of File gap, the stepper drive will advance as many steps as may be required to reach the next character. A Read/Stop input is provided at the interface to allow stopping this action at the end of data on the tape.

Since the stepper motor and gear box must be arranged to provide two steps per character in the Incremental Read mode, it follows that the same unit being used in the Write mode requires that two steps be taken for each character written. This is automatically provided for internally so that each Write/Step results in a character on the tape with the proper 0.005" spacing. However, this does restrict the upper speed of the writing to 300 characters per second, and the high speed option is thus not available on machines equipped to incrementally read.

SECTION II

PERFORMANCE SPECIFICATIONS

SECTION II

MODEL 1600/360

PERFORMANCE SPECIFICATIONS

GENERAL SPECIFICATIONS

TAPE USED	0.5" wide, 1.5 mil thick computer tape
TAPE FORMAT	Nine-track NRZ1
TAPE REELS	Up to 8.5" diameter, IBM compatible
TAPE COMPATIBLE WITH	IBM 2400 series tape transports
WRITE MODE	
Recording Speed	0-500 characters per second
Density	800 bpi
RECORD GAP TIME	550 milliseconds (maximum)
SLEW RATE	1000 characters per second (nominal) (1.25 ips)
REWIND TIME	Less than 2 minutes

OPERATOR CONTROLS AND INDICATORS

All front panel controls (except AC POWER switch) are duplicated by logic inputs at Write Interface connector P1.

AC POWER Switch

Applies power to the tape unit, presets the control circuits, and places dc braking voltage across the reel motors.

LOAD FORWARD Pushbutton With Indicator

Automatically advances the tape to the Load Point marker during a loading operation and generates a Beginning of Tape (BOT) Gap (see below) when the Load Point marker is sensed.

After the loading operation, pressing this button causes tape to be advanced at 1000 characters per second. Indicator illuminates when the button is first pressed and remains lit until the automatic stop following a Rewind operation. The indicator also goes out if Broken Tape is sensed.

READY Indicator With Pushbutton

Indicator illuminates whenever the tape unit is in READY (ready to accept data). The push-button may be used to place the tape unit in READY by pressing it simultaneously with the LOAD FORWARD Pushbutton. This is an interlock to guard against inadvertently pushing this button. Since the tape unit automatically enters READY when the Load Point marker passes under the sensor assembly, this feature should be used only in the rare instances where no Load Point marker is present.

Note

Use of this feature will not result in a BOT Gap (see below).

FILE GAP Pushbutton Only

Manually inserts the IBM File Gap (see below), File Mark, and IRG.

REWIND Pushbutton With Indicator

Drops the tape unit from READY and rewinds tape at high speed until the Load Point marker is sensed or until tape winds off the reel. In either case, stop is automatic.

INTERNAL CONTROLS AND FEATURES (Also See Figure 1-5, Data Format - Nine Track)

Parity Generator

Lateral Parity is generated and written on Channel P. Odd parity is supplied as required by IBM standards.

The Cyclic Redundancy Check Character (CRCC), required in the 9-track format in addition to Lateral Parity and the LCC, is written four character spaces after the last data character in a block. Its generation is part of the Inter-Record Gap and File Gap sequences.

Longitudinal Parity (the Longitudinal Check Character, or LCC) is written eight character spaces after the last data character in a block and four character spaces after the CRCC. Its generation is part of the Inter-Record Gap and File Gap sequences.

Continuous (Slew) Operation

For applications requiring a higher data input rate, continuous writing at 1000 characters per second may be achieved with this recorder. In this mode, data is recorded in bursts, and all starts and stops take place in the IRG (see below).

The high speed is achieved by accelerating the motor beyond its normal asynchronous rate. Internally generated motor clock pulses are brought out to the interface for use as a system data clock. Thus, stepping and writing are exactly synchronized.

Gaps and Marks

Inter-Record Gaps and File Gaps which are compatible with IBM format are generated automatically on command from the interface. File Gaps may also be automatically generated with a front panel control.

Inter-Record Gap (IRG)	Also called End of Record Gap (EOR). A 0.6" IRG generated upon command from the interface. A properly spaced CRCC and LCC are inserted as part of the gap timing sequence.
File Gap (EOF)	Standard 3-3/4" File Gap generated upon command from the interface or with a front panel control.
File Mark	Also called Tape Mark. A "one" in Channels 3, 6, and 7 written automatically upon completion of the File Gap. The File Mark is followed automatically by a properly spaced File Mark Check Character (another 3, 6, 7) and an additional 0.6" IRG. A CRCC is not written at this time.
Beginning of Tape Gap (BOT)	Also called Initial Gap. A 1/2" (minimum) BOT Gap is automatically inserted when the Load Point marker is sensed during a loading operation.

Tape Sensors

Load Point, End of Tape, and Broken Tape sensors are provided. Signals generated by the first two of these sensors are amplified and brought out to the interface connector. The Load Point sensor is used during a loading operation to generate a BOT Gap. It is also used to halt a Rewind operation.

The End of Tape sensor has no internal function. It provides a control signal to the external equipment when the End of Tape marker is under the sensor assembly.

The Broken Tape sensor halts all machine operations in the event of broken or missing tape at the sensor assembly.

INTERFACE CHARACTERISTICS

Model 1600/360 Standard Write interface is compatible with current sinking positive logic having a "one" level of +4V to +6V and a "zero" level of 0V ±0.5V. "Zero" levels should be capable of sinking 5 ma. All input functions except remote controls are initiated by "one" levels. Remote

control inputs require closures to ground to be activated. Maximum current through the closure is 5 ma; open circuit voltage is +10V. This may be loaded or clamped to +5V (minimum) for use with IC logic.

Note

Because of the nature of DTL logic used in the tape unit, the following inputs must be tied to Signal Ground if they are not used: COUNT ENABLE, CONTROL COMMON, SLEW, EOF COMMAND, and EOR COMMAND. All P1 pins not assigned are reserved by Kennedy Company for future use and should not be used as tie points.

The P1 connector is Part No. 121-5004-036 (Amphenol 57-40360 or equivalent). The mating connector (supplied) is Part No. 121-5003-036 (Amphenol 57-30360 or equivalent).

Modified interfaces are available. Consult the factory.

Inputs

PULSES are to be a minimum of 20 usec long and a maximum of 100 usec long.

LEVELS are to be static at the time of the leading edge of the pulse which clocks them in. They must remain static for at least 50 usec thereafter.

CLOSURES TO GROUND are to be a minimum of 20 usec long and a maximum of 100 ms long.

DATA LINES	LEVEL	Channel 7	P1-18
		6	P1-19
		5	P1-17
		4	P1-20
		3	P1-21
		2	P1-16
		1	P1-22
		0	P1-23
WRITE/STEP Command	PULSE		P1-14
Clocks in information on data lines.			
EOR Command	PULSE		P1-30
Starts IRG sequence. Must be applied no sooner than 2 ms after the trailing edge of the last Write/Step Command in the block.			

EOF Command PULSE P1-29

Starts File Gap sequence. Must be applied no sooner than 2 ms after the trailing edge of the last Write/Step command. This function is duplicated by the File Gap front panel control.

WRITE SELECT LEVEL P1-1

Enables Write mode when True and the tape unit is READY. Disables Write mode when False. In normal Write-Only operation this input should be tied directly to +5V.

REMOTE LOAD FORWARD CLOSURE TO GROUND P1-2

Prepares tape unit for writing after tape has been loaded. Causes tape to feed at 1000 characters per second until Load Point marker is reached. BOT Gap is automatically generated at this point. This function is duplicated by the Load Forward front panel control.

REMOTE READY CLOSURE TO GROUND P1-3

Not normally used. Places machine in READY. This input should be used only in the rare instances where no Load Point marker is present on tape.

REMOTE REWIND CLOSURE TO GROUND P1-4

Drops READY and rewinds tape at high speed until the Load Point marker is sensed. To further rewind the tape off the reel for unloading, the tape unit must be placed in the Load Forward mode after the tape has stopped. Rewind may then be activated again to remove tape completely from the take-up reel. Rewind stops automatically when tape is completely wound on to the supply reel. This function is duplicated by the front panel Rewind control.

COUNT ENABLE P1-6

This input is not used in nine-channel tape units and must be tied to Signal Ground to avoid erroneous operation.

CONTROL COMMON P1-7

Connect to Signal Ground to enable front panel pushbuttons. Buttons are disabled if this connection is not made.

SLEW LEVEL P1-8

Used during Continuous Writing operation only. A True level activates an oscillator which gradually accelerates the stepping motor to 1000 steps per second. Outputs from this oscillator are brought to the interface (see below) for use in synchronizing the data inputs to the stepper motor pulses.

FORWARD SELECT LEVEL P1-10

Used in Read/Write models to control the direction of the stepper motor.

A True Forward Select level causes the stepper motor to run forward. A False level causes the stepper motor to run backward.

CAUTION

In Write-Only models the Forward Select input should be tied directly to +5V or +6V to avoid driving tape backward and erasing it.

+5V P1-12

The internal +5V supply is brought to this pin for use as an external reference. Maximum external loading is 100 ma.

SIGNAL GROUND P1-11

CHASSIS (FRAME) GROUND P1-36

Signal Ground and Chassis Ground are not connected together within the tape unit. For best results, run these two lines separately to the Main System Ground and connect them together only at that point.

Outputs

P1 signal outputs are terminated in the tape unit through a source impedance of 1.5K (nominal), and are capable of sinking up to 10 ma of external load current. Levels are +5V ±1V True and 0V ±0.5V False. Outputs may be loaded or clamped to +3V (minimum).

READY LEVEL P1-27

Indicates that the loading process is complete and head current is flowing. Data may be recorded whenever this output is True and the Gap in Process output is False. This output is duplicated by the READY Indicator on the front panel.

GAP IN PROCESS LEVEL P1-28

Indicates that the tape unit is under the control of the gapping electronics and is inserting an IRG, End of File, or BOT Gap. The output includes a delay at the end of each gap for the tape unit to come to a stop. Writing should not be attempted while this level is True.

END OF TAPE LEVEL P1-5

Indicates that the End of Tape marker is under the sensor assembly. This function is not used internally.

WRITE ERROR LEVEL P1-24

Indicates that the Echo Check circuits have detected an error in the write electronics. Level will go True a maximum of 1.95 ms after the Write/Step Command has been given and will remain True until the next Write/Step Command is given.

OSCILLATOR OUT PULSE P1-26

Pulse duration 10 usec (minimum). Pulses from an internal oscillator, used primarily to drive the stepper motor at high speed during gapping operations, are brought out to this pin for use as a system clock in the Continuous Writing mode. Pulses are produced whenever the Slew input is applied or whenever the tape unit is inserting a gap. Nominal rate is 1000 pulses per second; however, the motor must accelerate to this speed over a number of steps.

Note

These pulses are used internally to drive the stepper motor during loading and gapping operations in either the Incremental or the Continuous Writing mode. Therefore, they must be properly gated externally to avoid system errors when a loading or gapping operation is in progress.

LOAD POINT LEVEL P1-31

Indicates that the Load Point marker is under the sensor assembly. This function is used internally to generate a BOT Gap during a loading operation and to halt tape during a Rewind operation.

POWER REQUIREMENTS	115V/230V ±10%, 50/60 Hz is standard. Power consumption: 150VA.
PHYSICAL CHARACTERISTICS	Panel 19 inches x 12-1/4 inches, fits standard rack. Depth behind panel: 10 inches. Added 8-inch depth clearance required to open auxiliary card cage. Weight: 45 lbs.

ENVIRONMENTAL

Operating Temperature	+2°C to +50°C (+35°F to +122°F)
Storage Temperature	-40°C to +75°C (-40°F to +167°F)
Storage Altitude	20,000 feet (maximum)
Relative Humidity	15% to 95%

Note

No condensation is allowed on any portion of the tape unit during operation. Any condensation accumulated during shipping and/or storage must be thoroughly removed before tape unit is operated. Tape manufacturers' specifications may impose more stringent environmental limitations than those given above. Consult tape supplier.

SECTION III

CHECKOUT AND INSTALLATION

SECTION III

CHECKOUT AND INSTALLATION

INTRODUCTION

This section contains information on unpacking, inspection, repacking, storage, and installation.

UNPACKING AND INSPECTION

If the shipping carton is damaged, ask that the carrier's agent be present when the recorder is unpacked. Inspect the recorder for damage (scratches, dents, broken knobs, etc.). If the recorder is damaged or fails to meet specifications, notify the carrier and Kennedy Company immediately. Retain the shipping carton and the padding material for the carrier's inspection. Kennedy Company will arrange for the repair or replacement of your recorder without waiting for the claim against the carrier to be settled.

STORAGE AND SHIPMENT

Packaging

To protect valuable electronic equipment during storage or shipment always use the best packaging methods available. Kennedy Company can provide packing material such as that used for original factory packaging. Contract packaging companies in many cities can provide dependable custom packaging on short notice. Here are a few recommended packaging methods:

Rubberized Hair: Cover painted surfaces of recorder with protective wrapping paper. Pack recorder securely in strong corrugated container (350 lbs./sq. in. bursting test) with 2-inch rubberized hair pads placed along all surfaces of the recorder. Insert fillers between pads and container to ensure a snug fit.

Excelsior: Cover painted surfaces of recorder with protective wrapping paper. Pack recorder in strong corrugated container (350 lbs./sq. in. bursting test) with a layer of excelsior about 6 inches thick packed firmly against all surfaces of the recorder.

Environment

Conditions during storage and shipment should normally be limited as follows:

a. Maximum altitude: 20,000 feet
b. Minimum temperature: $-40^{\circ}F$ ($-40^{\circ}C$)
c. Maximum temperature: $167^{\circ}F$ ($75^{\circ}C$)

Shipping Frame

Some Kennedy Company recorders are shipped in steel frames for protection. This frame fits snugly inside the shipping carton. Remove unit and frame from box. The frame is suitable for holding the machine in an upright position during initial handling and checkout.

RACK MOUNTING

Rack mounting slots are accessible with the recorder door open. If desired for greater ease of access, the door may be removed during mounting and replaced when the machine is in place.

Appropriate washers under mounting screw heads will prevent damage to painted surfaces of the panel.

POWER CONNECTION

A 3-wire detachable power cable is supplied with each machine. Exposed portions of the machine are grounded for safety. When only a 2-blade outlet is available, use connector adapter and ground the short wire from the side of the adapter.

Before plugging in to a 230V main, be sure the machine is wired for 230V operation. 230V wiring will be indicated by a prominent stamp near the power connector, or some models have a switch to select 115V/230V operation.

SECTION IV

OPERATION

SECTION IV

OPERATION

INTRODUCTION

In order to operate the recorder properly it is necessary to have it connected to a suitable interface. This is particularly true in the case of machines with DTL logic; they will not operate unless inputs specified to be zero are connected to ground.

It is assumed in the following that suitable preparations have been made and the machine is in an operable condition.

TAPE LOADING

1. With power off, place a full reel on the supply hub as shown in Figure 4-1.
2. Thread tape along tape path as shown in Figure 4-1 to the take-up reel.
3. Holding end of tape with a finger, wrap a few turns around the take-up reel.
4. Turn power on.

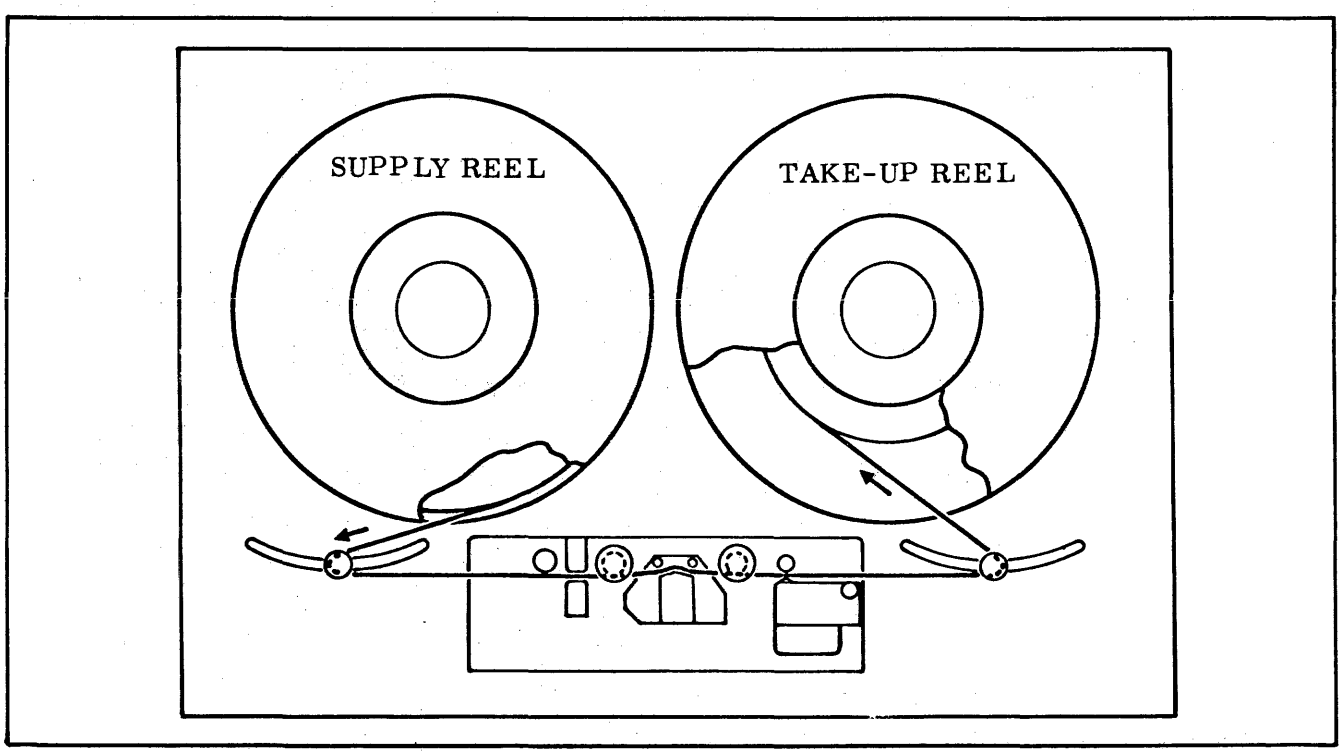


Figure 4-1. Tape Threading Diagram

5. Press LOAD FORWARD Pushbutton. Servos will energize and pinch roller will engage. Tape now advances automatically to the Load Point marker and in Write mode will insert Beginning of Tape Gap and stop.

6. READY light comes on and machine is now prepared to accept data.

INCREMENTAL WRITING

1. Feed a series of data inputs and Write/Step Commands to the interface connector, observing the proper relative timing requirements for these inputs. Input rate must not exceed that shown in the Performance Specifications.

2. At intervals, determined solely by system requirements, an IRG must be inserted. At these times, apply an EOR Command to the interface. Be sure to observe the timing requirements with respect to the final Write/Step Command of the record.

3. At the end of a job, or at other times determined by system requirements, an EOF Gap must be inserted. This can be done by applying the appropriate command to the interface or by pressing the FILE MARK Pushbutton on the front panel.

Note

In the case of systems that apply an IRG at the end of each record, no improper formatting results from following the last IRG of a job with an EOF Command; however, the separate EOR Command is not required.

REWIND

1. Press REWIND Pushbutton. Tape will rewind until Load Point marker is sensed and then stop. Rewind cannot be stopped (except by turning off power) once initiated. This is to prevent partial rewinding and subsequent possible destruction of data.

2. After tape has stopped it may be removed by manually completing the rewind with power off or by pressing LOAD FORWARD quickly, followed by pressing REWIND. Tape will then wind completely out of the machine and the reels will stop.

CAUTION

To avoid tape damage, always wait at least one second after the Load Point marker is sensed before activating any machine function. This allows the tape to stop completely.

SECTION V

MAINTENANCE

SECTION V

MAINTENANCE

ROUTINE MAINTENANCE

Primarily, routine maintenance consists of keeping mechanical parts clean. At regular intervals, depending in length upon use of machine and cleanliness of machine environment, the following steps should be taken:

1. Clean head surface and entire guide plate area with soft cloth and a mild organic solvent such as IBM head cleaner.

2. Clean surface of pinch roller to remove accumulation of oxide with a similar solvent.

3. Remove any accumulation of dust within the main cover and on the panel.

It should be kept in mind that while incremental recorders are very reliable devices and can operate under conditions more adverse than high speed computer tape transports, dirt is always a major source of difficulty and potential error. The tape path must be kept as clean as possible.

All bearings in the machine are lubricated for life. No further lubrication should be attempted since ball bearing lubrication can be destroyed by oil.

CHECKOUT AND ADJUSTMENT PROCEDURE

Relatively few adjustments are required on Kennedy Incremental Recorders. These can be divided into two classes, mechanical adjustments and electrical adjustments. Electrical adjustments, if any, will be found in Sections VI and VII. Mechanical adjustment procedures are given below.

Mechanical Adjustments

Tension Arm Adjustment: Two tape tension arms are provided for sensing tape tension and providing a buffer loop to allow free tape motion. Tension arms are coupled to potentiometers which control reel motor torque to maintain tension constant. Adjustments required are:

1. Tension Arm Return Force (Ref. Figure 5-1)

   Tension arms are spring loaded to provide proper tape tension. To set tape tension:

a. Swing arm to approximate center of arc.

b. Measure return force at the end of the arm with a spring scale.

c. Adjust anchor lug position for a spring scale reading of 4 oz (113 gm). This setting will establish 2 oz of tape tension.

2. Servo Potentiometer Angular Position (see Figure 5-1)

Tension arm is coupled to servo potentiometer by a shaft clamp. Potentiometer shaft extends through the panel and is slotted to accept a screwdriver. Servo potentiometer must be positioned to give proper motor torque.

a. Loosen shaft clamp lock screw until potentiometer shaft may be rotated with a screwdriver but still is snug enough to be rotated by tension arm. Press LOAD FORWARD pushbutton.

b. Hold tension arm in approximate center of arc. Turn potentiometer shaft until torque produced by reel servo drops to zero.

c. Tighten clamp lock screw.

d. With tape in place energize servos. Note position assumed by tension arm. If not close to center of arc, readjust potentiometer shaft to correct.

Note

Potentiometer shafts are accessible only with reels removed.

3. Tape Path Location

Tension arm rollers establish approximate tape path. To assure that no skew is introduced this path must conform closely to guide path. To adjust:

a. Loosen locking setscrew (Figure 5-1).

b. Measure height of rear edge of tape (closest to panel) at the guide plate. Tape should clear guide plate surface by 0.437 inch (1.72 cm) ±0.005 inch (0.127 mm), and be parallel to guide plate surface throughout its length.

c. When proper tape height is obtained lock roller in plate by tightening locking setscrew.

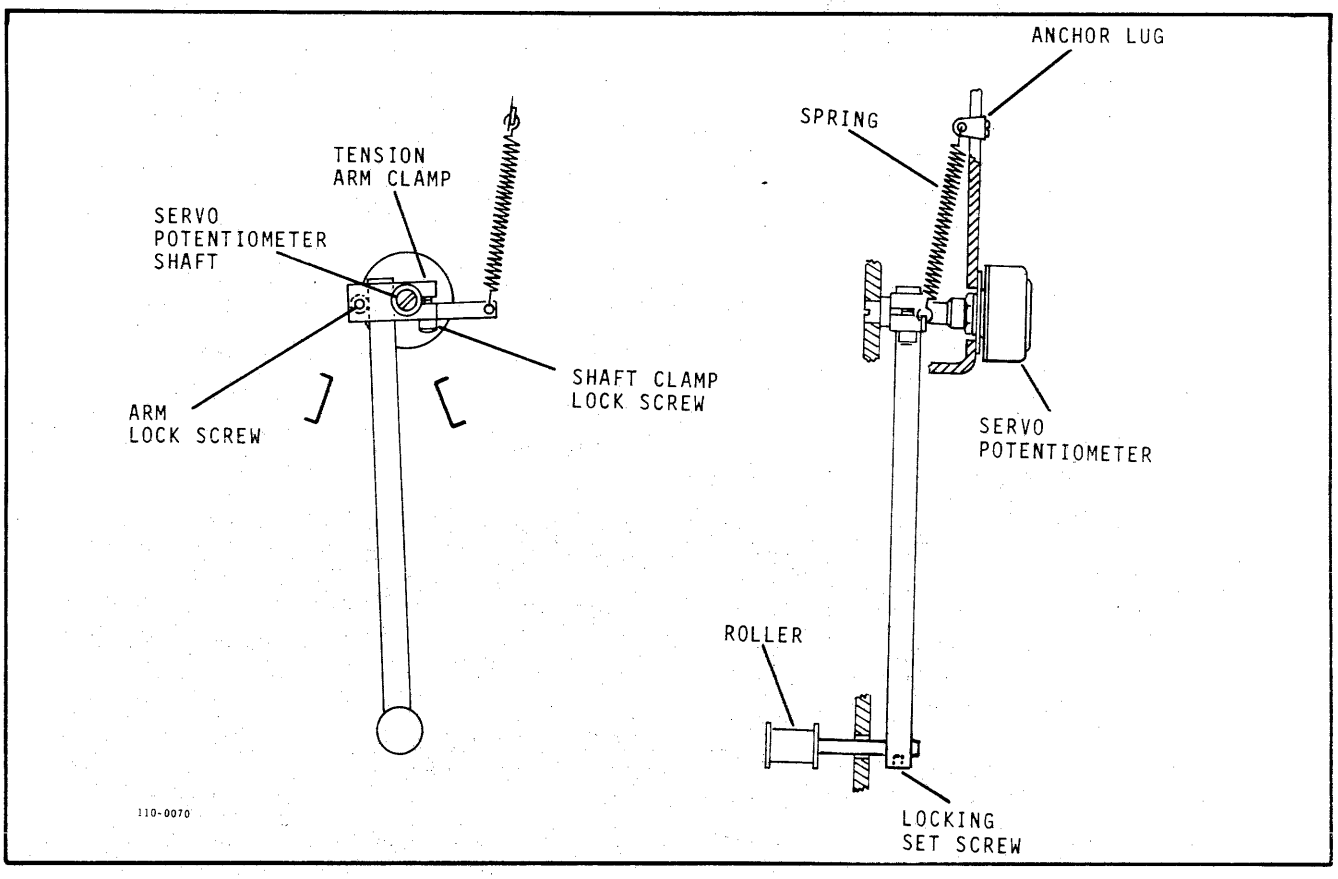


Figure 5-1. Tension Arm Adjustments

4. Capstan Drive Gear Mesh

Adjustment of Capstan Drive Gear Mesh is accomplished by rotating the stepper motor in its eccentric mounting. This adjustment should not be attempted unless there is strong reason to believe it is required. Gears are properly meshed when units leave the factory and should not require re-adjustment over long periods.

Mesh adjustment cannot be measured directly; it must be accomplished by feel. With power off:

a. Loosen three clamp screws holding motor in place.

b. Rotate motor clockwise (from rear) to tighten mesh.

c. Rotate capstan shaft as motor is rotated to detect zero backlash setting.

d. Lock motor in place and check again for zero backlash and free rotation. It should be possible to rotate motor from the capstan without difficulty.

e. If necessary, repeat procedure until zero backlash with free rotation is achieved. In the proper setting a slight "toothy" feel will be noticed.

5. Pinch Roller Adjustment (Figure 5-2)

The standard pinch roller should be adjusted to supply sufficient frictional force to drive the tape properly. To adjust the pinch-roller pressure proceed as follows:

a. Clean pinch roller well before making any adjustments.

b. With power applied to pinch roller, or holding solenoid in energized position, adjust roller height adjusting screw until roller does not touch capstan.

c. Turn screw an additional quarter turn.

d. Feed about 2 feet of tape through guides and over head, through pinch roller capstan.

e. Attach a spring scale to tape and press LOAD FORWARD button. Hold tape back until it slips at the drive.

f. Spring scale should read at least 6 oz (170 gm). If not, rotate the height adjusting screw slightly and remeasure.

g. Lock the height adjusting screw with Loctite grade H.

Tape recorders with the fast gap feature require an additional parallelism adjustment not required by the standard decks. To adjust the parallelism proceed as follows:

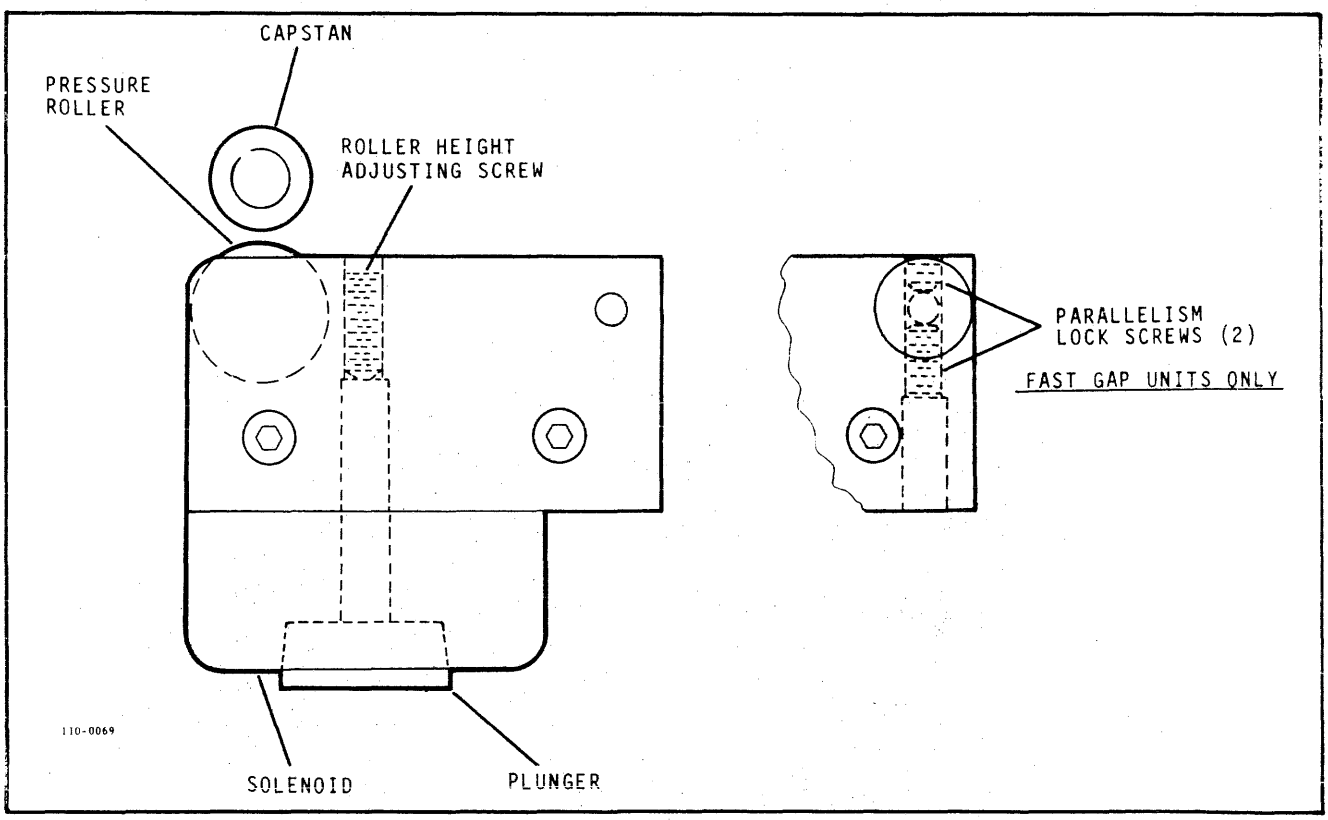


Figure 5-2. Pinch Roller Adjustments

a. Using a length of tape, say, 3 feet long (about 1 meter), feed through machine as above.

b. Press LOAD FORWARD and observe tape motion. Tape should pull evenly through pinch roller/capstan with no tendency to skew either in or out.

c. If tape does not pull straight, readjust parallelism screws (Figure 5-2) until straight motion is obtained. Tape will tend to move toward the tight side of engagement.

d. Lock screws in place and apply Loctite grade H.

e. Recheck as above after locking.

PHOTO SHUTTER ADJUSTMENT PROCEDURE

The photo shutter setting is preadjusted, and should not be changed during normal use and maintenance. Should readjustment become necessary, proceed as follows:

CAUTION

Do NOT touch the shutter disc while making the photo shutter adjustment; its knifelike edge may cause injury.

a. Remove the three retaining screws of the shutter cover, and then remove the cover itself, exposing the shutter mechanism.

b. Loosen the two retaining screws of the shutter horseshoe holder, as shown in Figure 5-3.

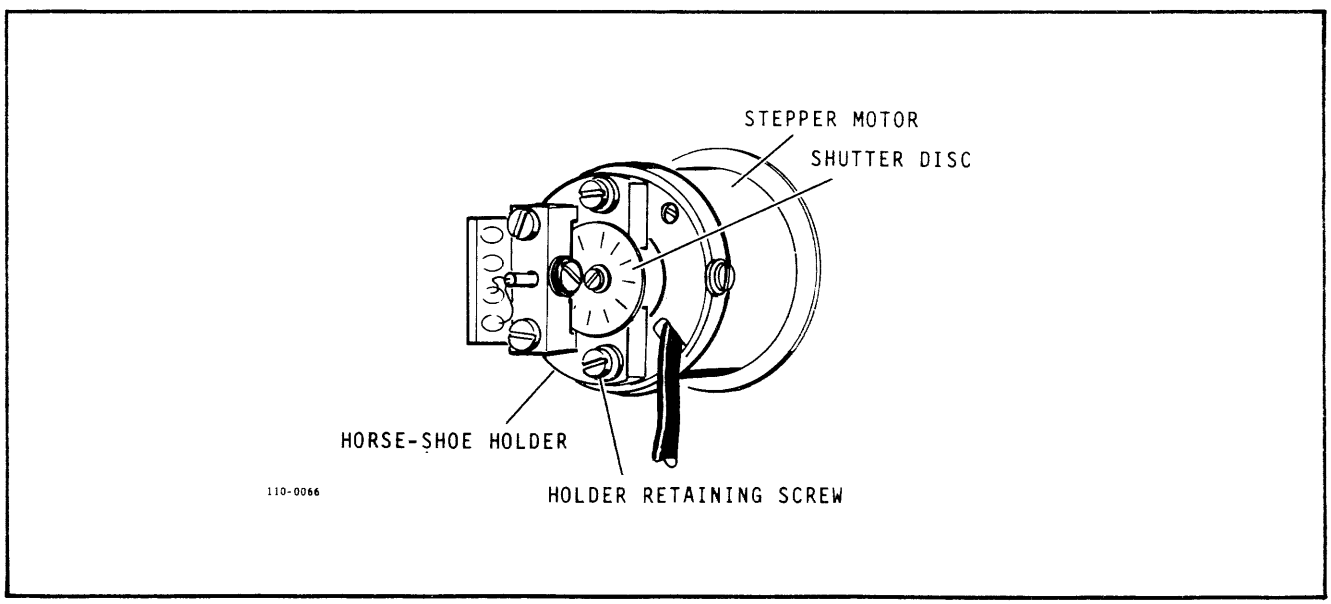


Figure 5-3. Photo Shutter Adjustment

c. Attach an oscilloscope probe to the OPTICAL PICKUP output at either test point B of the write control module in the Model 1600/360 or test point C of the interface module in the Model 1600.

d. Thread a tape on the reels and place the recorder in the LOAD FORWARD mode.

e. Rotate the horseshoe shutter holder until 1,000 pulses per second are shown by the oscilloscope.

f. To prevent the recorder from switching to 500 steps per second during slewing, tape off the BOT and BROKEN TAPE sensors from their respective light sources, disabling the BROKEN TAPE detection. Remove the reels from the hubs, and place the recorder in the LOAD FORWARD mode again. Load the capstan by pressing the capstan roller with the thumb and index fingers, and rotate the shutter holder until the 1,000 steps per second rate is recovered immediately after the capstan roller is released.

g. Supply write step commands to the recorder covering the possible writing range. The shutter pulses displayed by the oscilloscope should be free of extraneous peaks. If extraneous peaks are detected, rotate the shutter holder slightly until the peaks just disappear.

h. For a final check trigger the oscilloscope probe (attached the OPTICAL PICKUP) off the WRITE/STEP command and locate the resonance stepping frequency. The resonance frequency is the point at which the interval between the shutter pulse and the WRITE/STEP command is at a maximum. Ascertain that at this point the shutter pulse trails the WRITE/STEP command by a maximum of 1.2 milliseconds.

i. When the adjustment is complete, lock the shutter holder retaining screws and apply Loctite grade H (supplied with the K-21 maintenance kit). Replace the shutter cover.

REPLACEMENT OF PARTS

In the event of damage to the machine, parts not normally expected to be replaced might require maintenance. The following discussion describes procedures for maintenance under these circumstances.

1. Servo Potentiometer Replacement

   a. Remove potentiometer by removing two screws holding potentiometer mounting plate. Remember to loosen shaft clamp screw in tension arm clamp.

   b. Mount new potentiometer with lugs in same approximate location of old nut.

   c. Return potentiometer and mounting plate to assembly replacing tension arm.

d. Return mounting screws. Be sure potentiometer shaft rotates freely after screws are tightened.

e. Go through adjustment procedure as outlined above.

2. Tension Roller

Under extreme circumstances shaft of tension arm roller may be bent. In this case it requires replacement.

a. Remove old roller together with shaft.

b. Install new roller and shaft.

c. Adjust as previously described in step 3.

3. Pinch Roller

After long service the pinch roller may become worn and require replacement. To replace pinch roller:

a. Remove assembly from mounting surface by removing screws (item 1, Figure 5-4).

b. Remove pin (item 2) by means of a small hook formed from stiff wire.

c. Lift pinch roller yoke (item 3) clear of housing (item 4).

d. Remove retaining ring (item 5) from front of shaft.

e. Remove shaft (item 6) from rear of assembly, freeing pinch roller (item 7).

f. Replace pinch roller and reassemble.

g. Readjust pinch roller as previously described in step 5.

4. Capstan Assembly

In the event that through wear or other cause the capstan assembly needs replacement:

a. Remove old assembly by removing wires from terminal block and removing two mounting screws from front side of panel.

b. Replace with new assembly. Bearing must seat in counterbore on reverse side of mounting plate.

c. Readjust pinch roller (as previously described in step 5). Repair of capstan assemblies in the field is not advised. Return used assembly together with complete information to factory for credit.

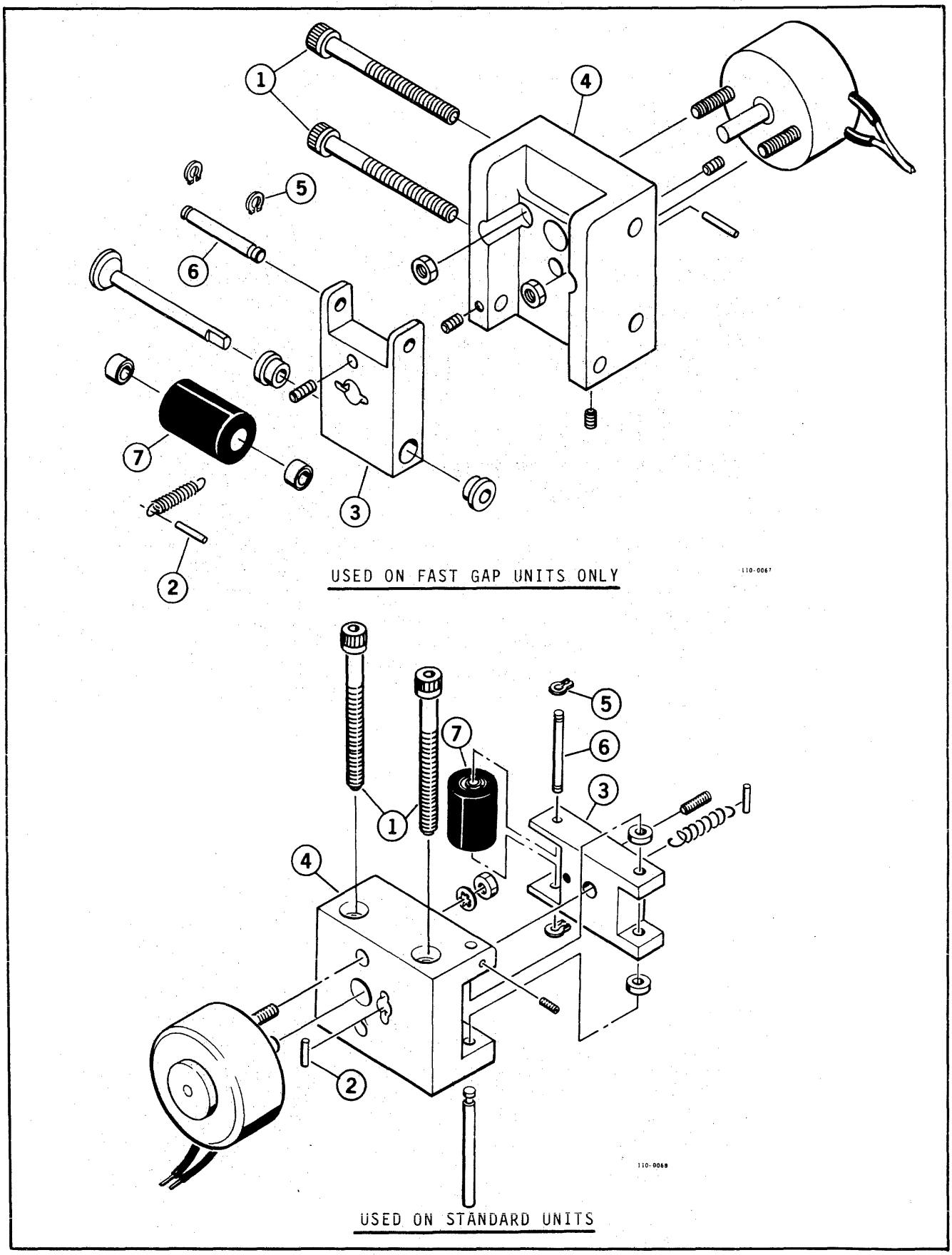


Figure 5-4. Pinch Roller Replacement

5. Reel Hub Grip Ring (Figure 5-4)

   A rubber ring is used as an expansion ring to hold the tape reel in place. If it should require replacement, simply pry old ring off without disassembling hub and snap new ring in its place.

6. Guides

   If a guide becomes worn, it is usually adequate to simply loosen its mounting screw, turn the guide a few degrees, and retighten.

   If complete replacement is desired, remove screw and guide. Replace with new guide; no adjustment is required.

7. Magnetic Head

   Heads have very long life at speeds encountered in incremental recorders. If replacement is required:

   a. Unplug head.

   b. Remove two mounting screws.

   c. Pass connector through hole in panel and remove head.

   d. Replace with new head.

   No adjustment of heads is possible or required. Return head to factory with complete details of cause for replacement.

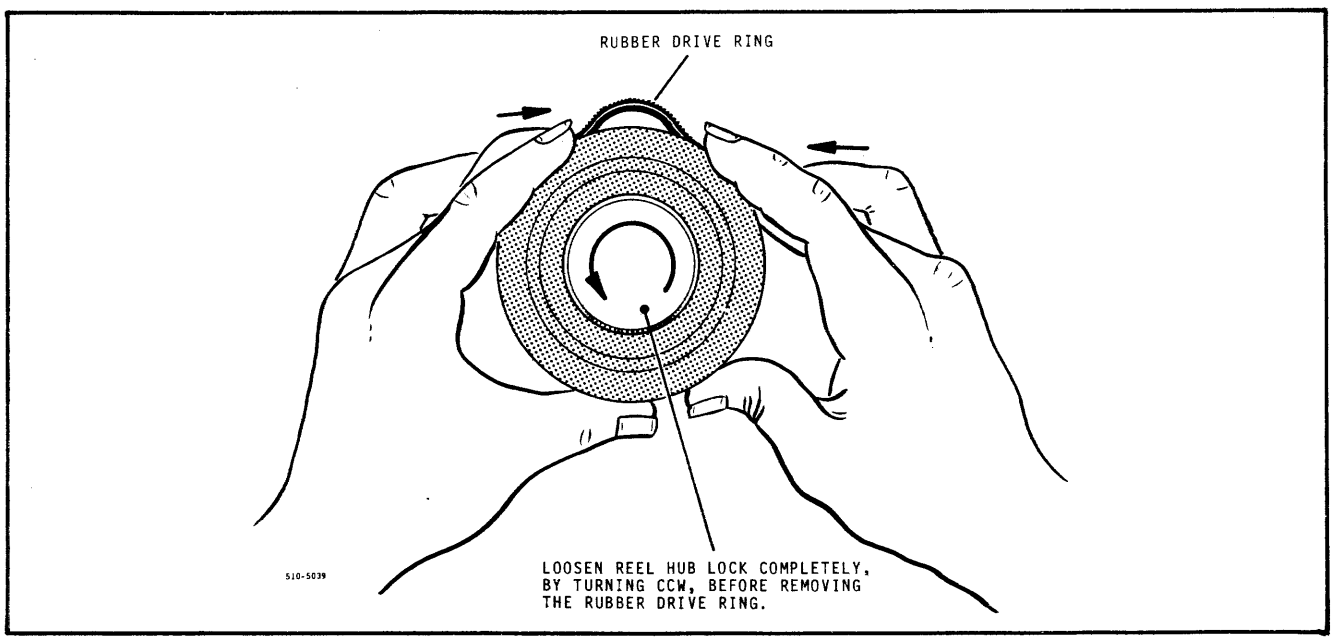
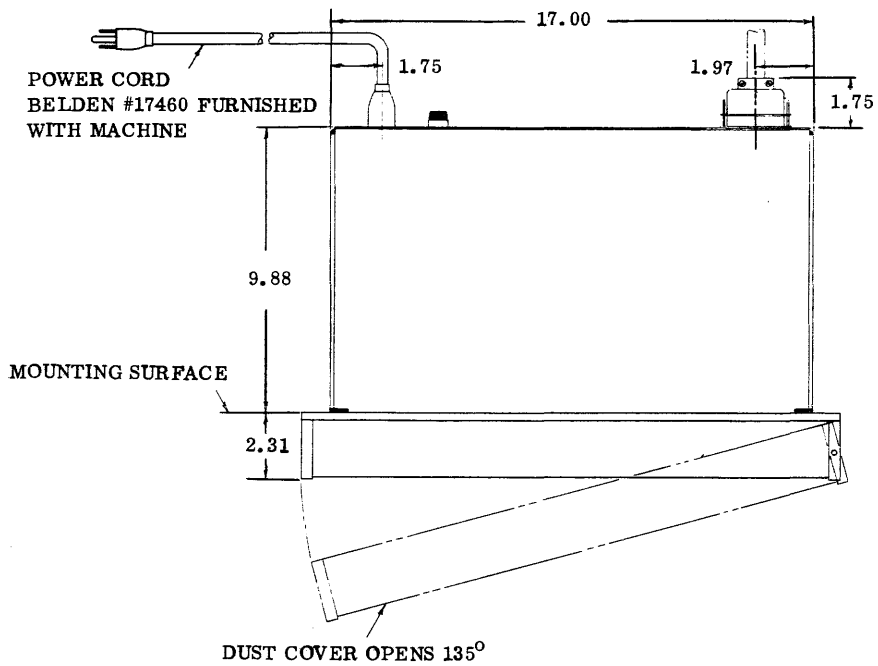
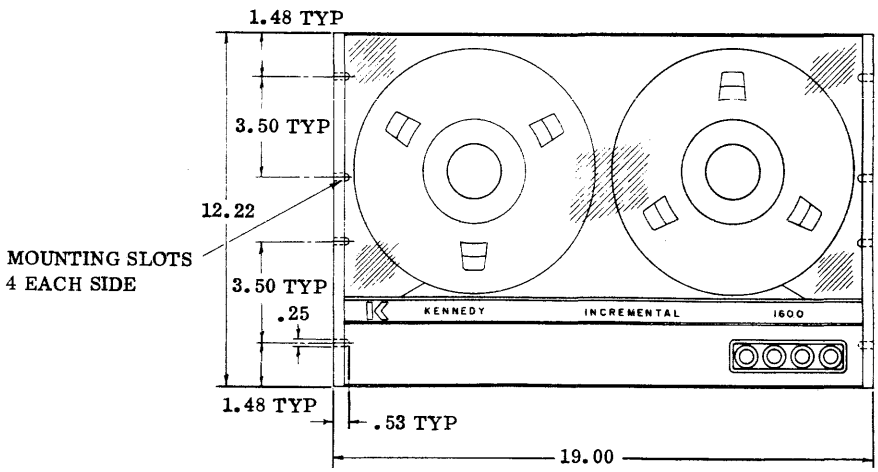


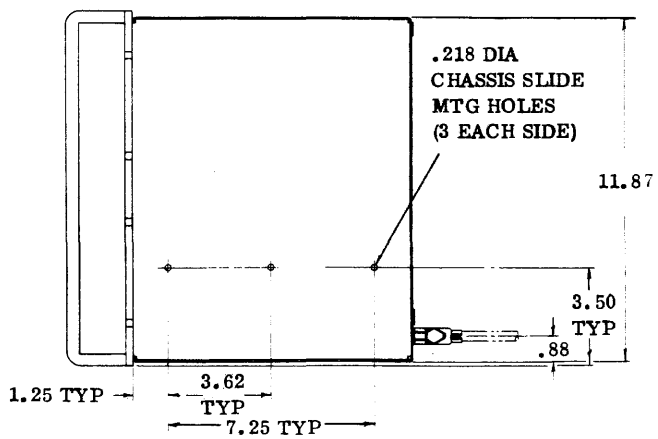
Figure 5-5 Rubber Ring Drive Replacement

SECTION VI

MECHANICAL



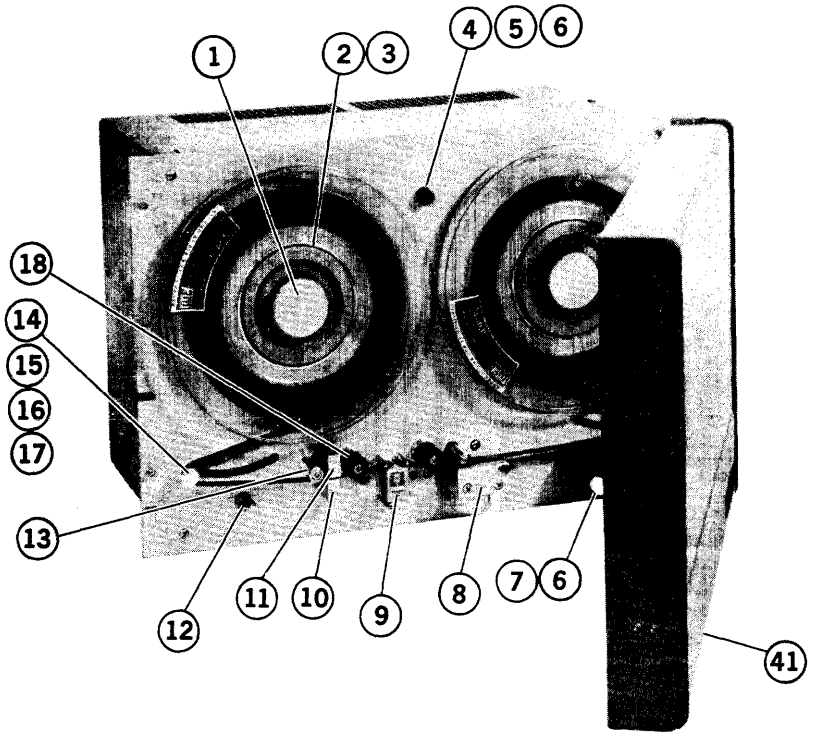


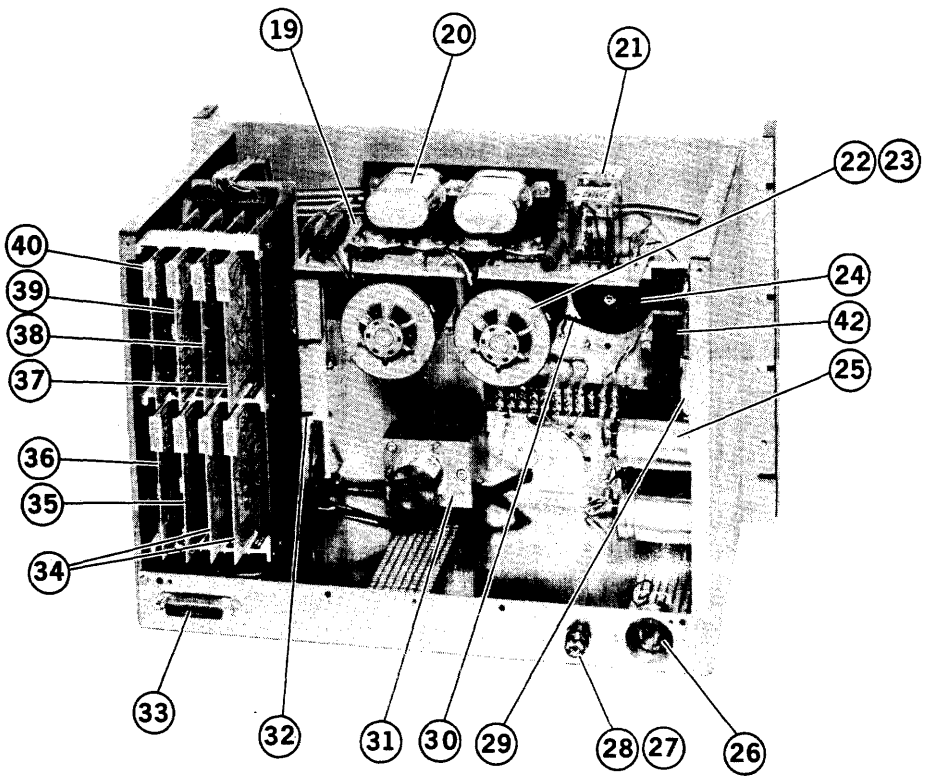


Model 1600 Outline and Installation Drawing

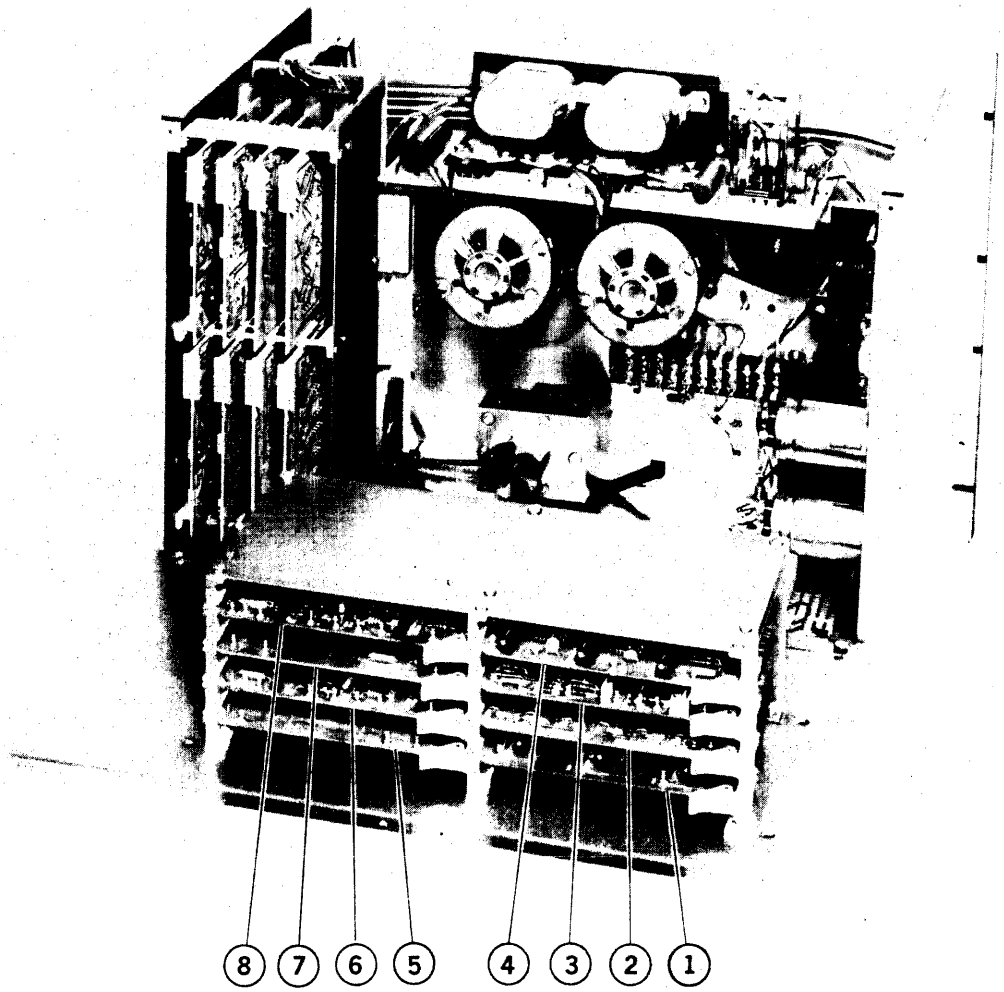
ITEM NO.	PART NO.	DESCRIPTION	QTY PER MACHINE
1	190-1141-001	ASSEMBLY, hub handle	2
2	190-1140-001	ASSEMBLY, reel hub	2
3	191-0574-001	RING, hub drive	2
4	139-2900-001	HOLDER, lamp	1
5	139-1900-501	COVER, lamp, green	1
6	139-0214-001	LAMP, no. 330	4
7	151-1005-101	SWITCH	4
8	190-1995-000	ASSEMBLY, pressure roller actuator	1
9	190-2451-001	ASSEMBLY, magnetic head	1
10	190-1139-001	ASSEMBLY, sensor, broken tape	1
11	190-1139-001	ASSEMBLY, sensor, end of tape	1
12	151-2001-101	SWITCH, toggle, spst	1
13	191-0549-001	POST, brake	1
14	190-0637-000	ASSEMBLY, roller, tension	2
15	191-0766-005	ARM, tension	2
16	125-0036-001	SPRING, extension 251A	2
17	191-0635-002	POTENTIOMETER	2
18	190-1509-001	ASSEMBLY, guide, split tape	2
19	190-2273-001	ASSEMBLY, control board, deck power	1
20	115-3625-798	CAPACITOR	2
21	145-0005-001	RELAY, 3pdt	2
22	135-0001-001	MOTOR	2
23	191-2353-001	PULLEY, motor	2
24	191-2354-001	PULLEY, reel drive	2
25	115-7049-405	CAPACITOR, 4 uf, 330v	2
26	121-9001-003	RECEPTACLE, ac power	1
27	151-0802-001	HOLDER, fuse	1
28	151-0132-001	FUSE, 2 amp, slo-blo	1
29	190-2307-001	ASSEMBLY, power supply regulator	1
30	125-0004-002	BELT, timing	2
31	190-2204-003	ASSEMBLY, capstan drive	1
32	190-2413-001	ASSEMBLY, master board	1
33	121-5004-036	CONNECTOR, 36 pin (P1)	1
34			OMIT
35			OMIT
36			OMIT
37	190-2528- *	ASSEMBLY, printed circuit board, stepper power ampl	1
38	190-2677- *	ASSEMBLY, printed circuit board, stepper logic	1
39	190-2655- *	ASSEMBLY, printed circuit board, gap timing	1
40	190-2654- *	ASSEMBLY, printed circuit board, control	1
41	190-2445-001	ASSEMBLY, dust cover	1
42	156-3385-001	TRANSFORMER	1
		*Suffix P/N with dash number reflected on card I.D. chart	

12-08-01





Model 1600 Parts Identification



Auxiliary Card Cage Parts Identification

ITEM NO.	PART NO.	DESCRIPTION	QTY PER MACHINE
1, 2, 3	190-2436-005	ASSEMBLY, printed circuit board, write amplifier	3
4	190-2567-001*	ASSEMBLY, printed circuit board, write control	1
5	190-2252-011	ASSEMBLY, printed circuit board, parity generator	1
6	190-2551-001	ASSEMBLY, printed circuit board, CRCC generator	1
7	190-2555-001	ASSEMBLY, printed circuit board, CRCC logic	1
8	190-2236-001**	ASSEMBLY, printed circuit board, CRCC control	1

*Replaced by 190-3454-001 in some units

**Replaced by 190-3620-001 in some units

Model 1600/360 Auxiliary Card Cage Parts Identification

SECTION VII

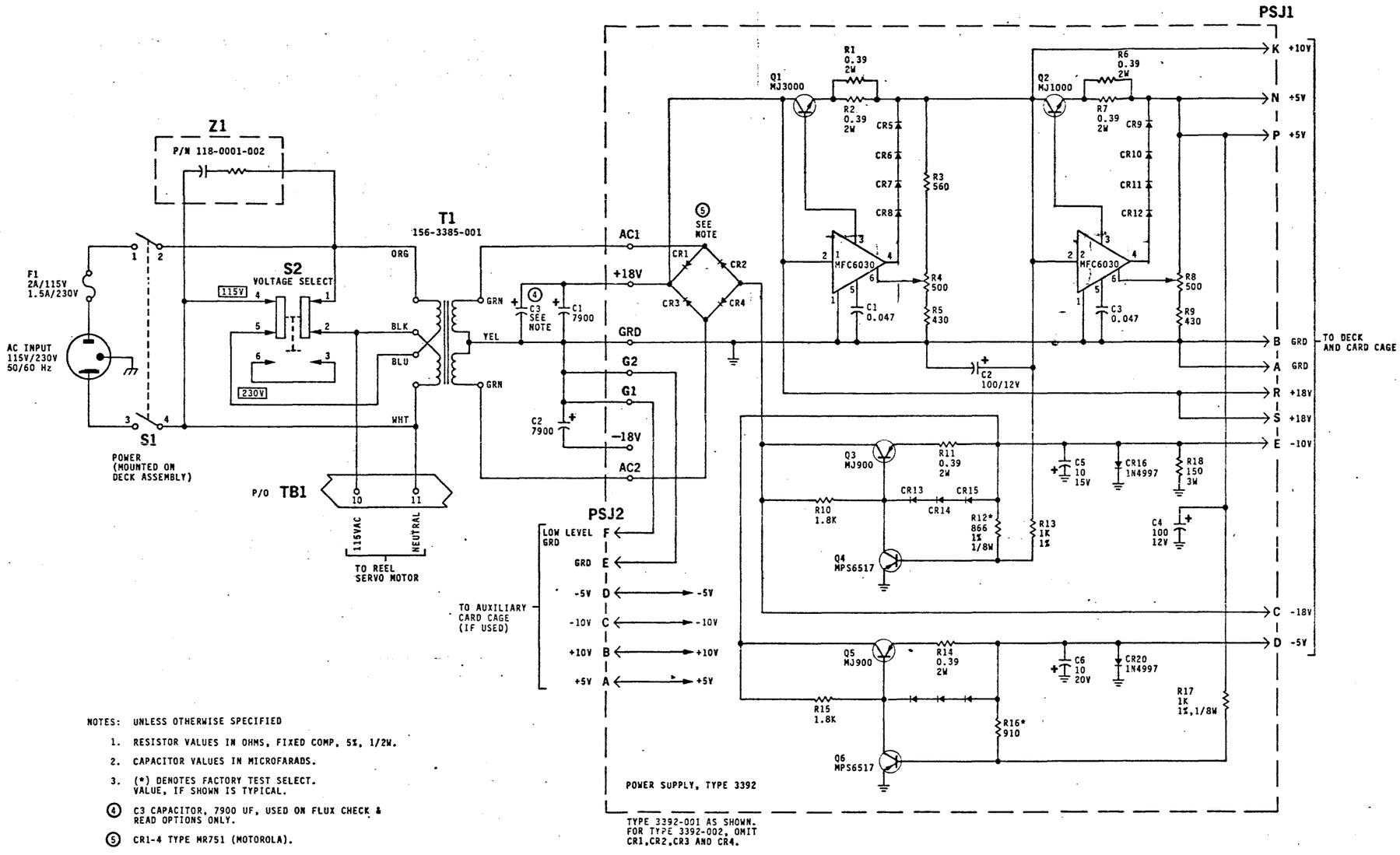
ELECTRICAL

VOLTAGE REGULATOR TYPE 3392

Voltage regulator type 3392 consists of four regulators, used to generate +10, -10, +5, and -5 voltage levels. The +10 volts regulator consists of Darlington transistor Q1, current regulator IC1, and associated components. Resistors R3, R4, and R5 supply the reference voltage to IC1, while IC1-3 supplies current to the base of Q1 as required to maintain the voltage level at +10 volts. Resistors R1 and R2 and diodes CR5, CR6, CR7, and CR8 form a current limiting network, while capacitor C2 eliminates any short spikes at the output.

The -10 volt regulator consists of a base regulated emitter follower using transistors Q3, Q4, and associated components. Resistors R12 and R13 form a voltage divider to supply a reference voltage to the base of Q4. The collector of Q4 regulates the base current of Q3, maintaining a level output voltage. Resistors R11 and diodes CR13, CR14, and CR15 form a current limiting network. Diode CR16 limits any positive voltage that may be shorted to the -10 volt output.

The +5 and -5 volt regulators are identical to the +10 and -10 volt regulators. The regulated outputs of the +10 and -10 regulators are used as the inputs of the +5 and -5 voltage regulators, thus providing a doubly regulated output.



NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2W.
2. CAPACITOR VALUES IN MICROFARADS.
3. (*) DENOTES FACTORY TEST SELECT. VALUE, IF SHOWN IS TYPICAL.
4. C3 CAPACITOR, 7900 UF, USED ON FLUX CHECK & READ OPTIONS ONLY.
5. CR1-4 TYPE MR751 (MOTOROLA).
6. THIS CARD FUNCTIONALLY INTERCHANGEABLE WITH 2563 POWER SUPPLY REGULATOR HAVING SAME DASH NO.
7. ALL DIODES ARE TYPE 1N914.

Power Supply Regulator,
Type 3392-001
Schematic Diagram

TYPE 2273 REEL MOTOR SERVO CONTROL

CARD PURPOSE

Servos and control circuits for both reel motors are contained on the Type 2273 card.

DESCRIPTION

Circuitry for the supply motor will be described. Circuitry for the take-up motor is similar.

Reel Braking

When power is first turned on, dc dynamic braking holds the tape reels in position. The same condition is obtained following a Rewind operation and brings the tape to a stop quickly and smoothly.

In the braking condition, both relays KF and KR are de-energized. Braking current then flows from +18V through KF1-NC, R5 (a current limiting resistor), CR3, the line winding of the supply motor, and KF3-NC to -18V.

Servo Operation

The reel servos control motor torque output to achieve constant tape tension. Tension is sensed by passing the tape over spring loaded buffer arms connected to potentiometers in the servo circuit.

WARNING

The servos are powered entirely from line voltage. Consequently, the components in these circuits are at line potential and can be dangerous unless handled carefully.

KF is energized by grounding Terminal 3. This occurs when the LOAD FORWARD Pushbutton is pressed. The control logic holds KF energized until the conclusion of a Rewind operation. During this time, the dc voltage is disconnected from the reel motors and replaced by controlled ac voltage.

Ac power is connected to the supply reel motor through KF2-NO, control bridge rectifier CR8, the motor windings, and KF3-NO. The bridge conducts ac current to the extent that it is loaded at its dc terminals.

Transistor Q4 is connected as a dc load to CR8. Its conduction is controlled by servo potentiometer R7 and transistor Q2. Part of the voltage appearing across Q4 is applied to the potentiometer. When the slider voltage exceeds the total of the forward-biased diode drops of Q2, Q4, and CR2, then Q4 begins to conduct. As it conducts, ac current flows through the supply reel motor and produces torque.

Rectifiers CR3 and CR4 isolate the controlled ac supplies of the two reel motors from each other. During dc braking they are both forward-biased and provide braking current to their respective reel motors.

A dc path is completed to the pinch roller solenoid whenever KF is energized and KR is de-energized, as in normal operation. Current flows from +18V through KF1-NO and KR2-NC to the solenoid.

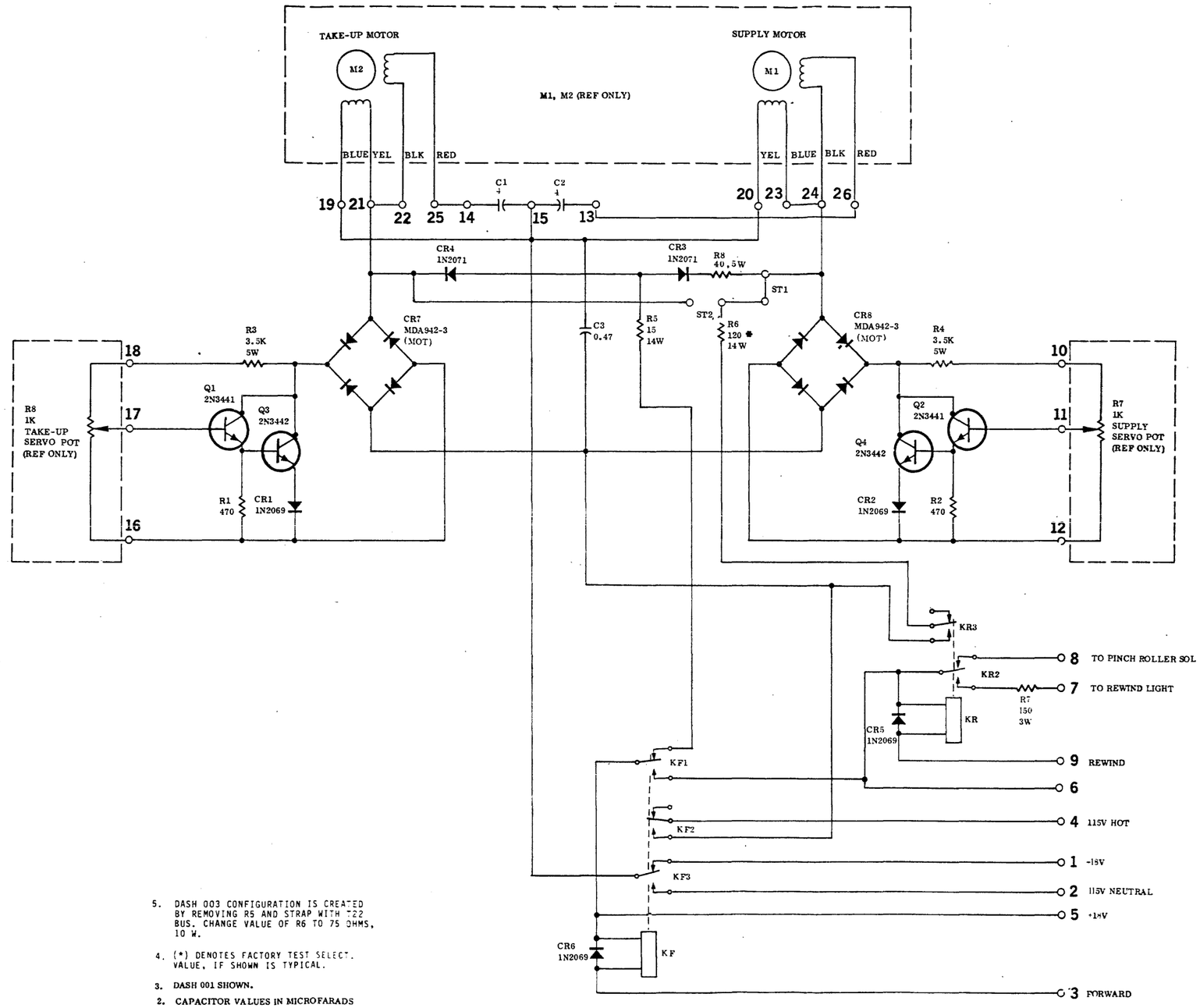
Another dc path is completed to the File Protect solenoid (in Write/Read units only) whenever KF is energized. Current flows from +18V through KF1-NO to Terminal 6 and the File Protect solenoid. This allows tape reels to be changed in the dc condition without switching power off, yet still provides full file protection by de-energizing the File Protect solenoid while the reels are being changed.

Rewind

Relay KR is interlocked with KF1-NO and cannot be energized unless KF is also energized. KR is energized by grounding Terminal 9. This occurs when the REWIND Pushbutton is pressed. A holding circuit is provided in the control logic. In the rewind condition the pinch roller solenoid is de-energized, current being switched instead to the REWIND Indicator on the front panel. KR3-NO connects the ac line directly to the supply motor through R6 (thus bypassing CR8), causing the supply motor to run independently of the condition of the supply tension arm and potentiometer R7.

Note

Resistor R6 and relay connection KR3 are not duplicated on the take-up motor.



5. DASH 003 CONFIGURATION IS CREATED BY REMOVING R5 AND STRAP WITH #22 BUS. CHANGE VALUE OF R6 TO 75 OHMS, 10 W.
4. (*) DENOTES FACTORY TEST SELECT. VALUE, IF SHOWN IS TYPICAL.
3. DASH 001 SHOWN.
2. CAPACITOR VALUES IN MICROFARADS
1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2 W

NOTES: UNLESS OTHERWISE SPECIFIED

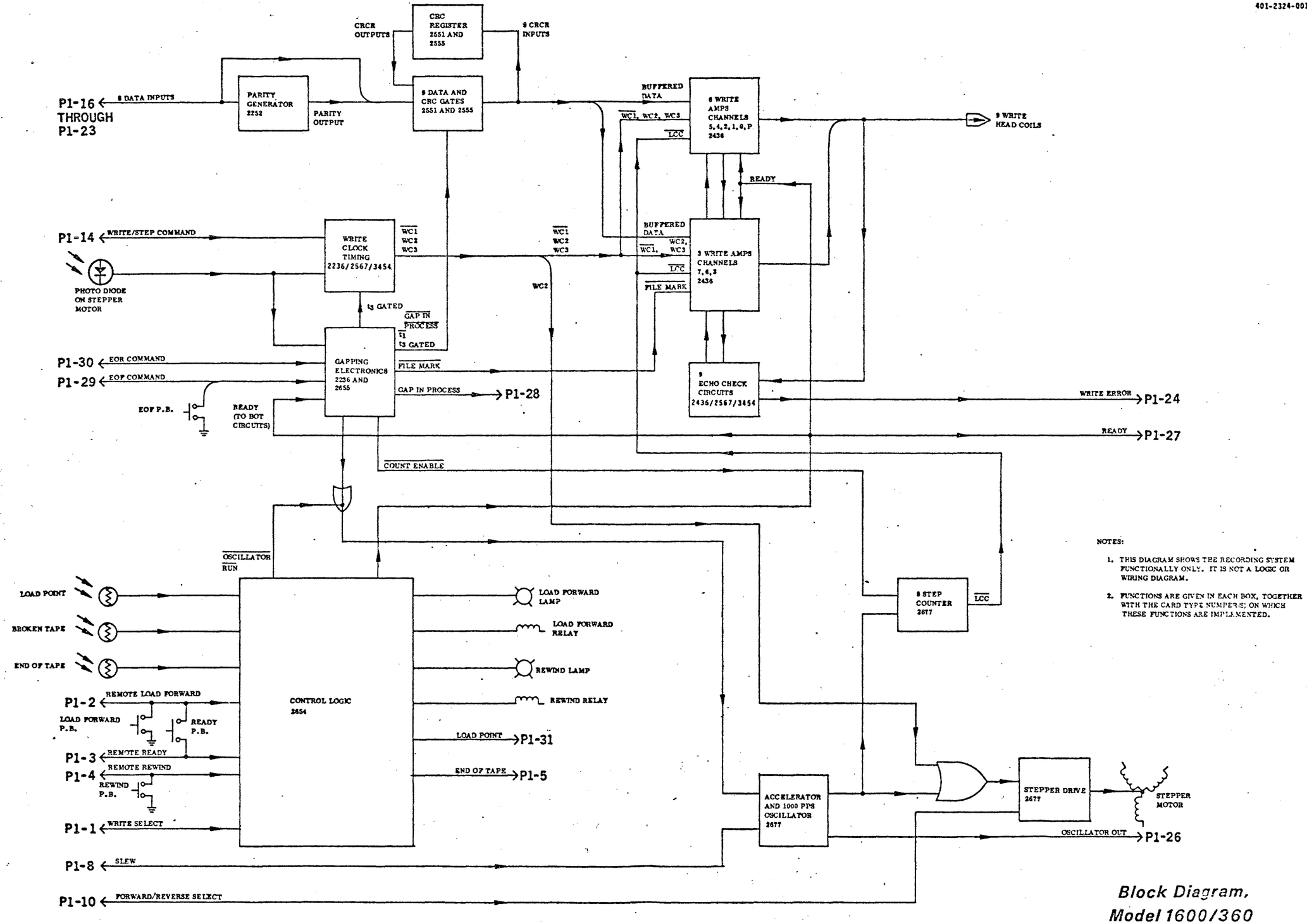
Reel Motor Servo Control, Type 2273, Schematic Diagram

SECTION VIII

PLUG-IN MODULES

ARRANGEMENT OF SCHEMATICS AND WIRING DIAGRAMS FOR MODEL 1600/360

Functional Group	Schematic Name and Type
Wiring and Block Diagrams	Block Diagram Model 1600/360
	Model 1600/360 Logic Section Wiring Diagram
	1600/360 Auxiliary Card Cage Wiring Diagram
Control and Timing Circuits	Control Type 2654
	Gap Timing Type 2655
	Stepper Logic Type 2677
	Stepper Power Amplifier Type 2528
	Interface Type 2569
Write Data Circuits	1600/360 Write Control Type 3454
	Write Amplifier Type 2436
	Parity Logic Type 2252
	CRC Functional Logic Diagram
	CRC Control Type 3620
	CRC Logic Type 2551
	CRC Logic Type 2555



NOTES:

1. THIS DIAGRAM SHOWS THE RECORDING SYSTEM FUNCTIONALLY ONLY. IT IS NOT A LOGIC OR WIRING DIAGRAM.
2. FUNCTIONS ARE GIVEN IN EACH BOX, TOGETHER WITH THE CARD TYPE NUMBERS; ON WHICH THESE FUNCTIONS ARE IMPLEMENTED.

Block Diagram, Model 1600/360

401-2325-001C

P1

INTERFACE CARD (SEE SEPARATE SCHEMATIC)

WRITE ERROR 24 ← 16 T

WRITE/STEP COMMAND 14 ← 6 F

NOT USED 13 ← 5 E

SPARE 15 ← 7 H

DATA
- CHAN 2 16 ← 8 J
- CHAN 5 17 ← 9 K
- CHAN 7 18 ← 10 L
- CHAN 6 19 ← 11 M
- CHAN 4 20 ← 12 N
- CHAN 3 21 ← 13 P
- CHAN 1 22 ← 14
- CHAN 0 23 ← 15

NOT USED ON 1600/360
SEE 401-2347-001

PARITY GEN. TYPE 2894 CHAN C

MASTER BOARD

WC1

WC2

WC3

S

R

TYPE 2895 CHAN 1 WRITE AMPL/ECHO CHECK

CHAN B

CHAN 8

TYPE 2895 CHAN 2 WRITE AMPL/ECHO CHECK

CHAN A

CHAN 4

FILE MARK

LCC

SPARE 25 ← 17 U

FRAME GRD 36

OSCILLATOR OUT 26 ← 18 V

SLEW 8

COUNT ENABLE 6

END OF RECORD COMMAND 30 ← W 19

END OF FILE COMMAND 29 ← X 20

FORWARD SELECT 10

READY

NOT USED 9

GAP IN PROCESS 28 ← Y 21

RB

CC

WRITE SELECT 1

REMOTE LOAD FORWARD 2

READY LEVEL 27 ← Z 22

REMOTE READY 3

REMOTE REWIND 4

END OF TAPE 5

LOAD POINT 31

+5V 12 → A11

GRD 11 → A10

CONTROL COMMON 7 → J C13

CONTROL TYPE 2654

SWITCHED +18V

KF COIL

KB COIL

BKN

LP

EOT

+10V

READY

L. FWD.

RWD

LOAD FWD.

READY

RWD

FILE GAP

OSCILLATOR RUN

GAP TIMING TYPE 2655

A14

+18V

-18V

OSC/ STEPPER LOGIC TYPE 2677

STEPPER DRIVE TYPE 2528

STEPPER MOTOR

25 OHMS 10W (3)

TO ALL CARDS

TO STEPPER DRIVE

FROM POWER SUPPLIES

-10V

+10V

GRD

+5V

+18V

-18V

MASTER BOARD LAYOUT

1. CONNECTOR "A"
2. 2654
3. 2655
4. 2677
5. 2528
6. INTERFACE.
10. RA
11. RB
12. RC
13. CONNECTOR "B"
14. CONNECTOR "C"

PENDANT CABLE TO PUSHBUTTONS

PLUG M TO HEAD

J4

5

6

7

TO AUX. CARD CAGE

NOTE 1 ● INDICATES CLOSED PAD NOT NORMALLY USED. PROVISION FOR EXTRA CONNECTIONS IN SOME OPTIONS.

[A] INDICATES NORMALLY USED PAD ON MASTER BOARD.

M-J INDICATES PRINTED CONNECTOR FINGER "J" ON MASTER BOARD.

A2 INDICATES PIN 2 OF P.C. CONNECTOR "A" ON MASTER BOARD.

Model 1600/360 Logic Section, Wiring Diagram

401-2347-00182

TO J4(ADJACENT TO MOTHER BOARD)

P4 5 6 7

SHUTTER

P6 B D A C

SHUTTER SIGNAL

SHUTTER OUTPUT

LCC

CH P

GIP (DELAYED)

-10V

+10V

GRD

+6V

2N5067

+5V

5

+18V

CH 7

CH 3

FILE MARK

CH 4

CH 1

WRITE READY

CH 0

WRITE STEP IN

t_3 GATED

ECHO CHECK

WC1

LCC

WC2

WC3

CH P

WC2

GIP

ECHO CHECK OUT

PARITY TO CH P

CH 0 IN

CH 1 IN

CH 6

CH 7

CH 6 IN

CH 7 IN

CH P

CH 0

CH 1

CH 2

CH 5

7-2 OUT

5-1 OUT

CH 5

CH 4

GIP DELAYED

CH 3

C_D

CRC CLOCK

CH 2

1-1 OUT

FILE MARK

GIP DELAYED

t_3 GATED

GAP CLOCK

CC-INT

CH-LBT

CH 5-2

CH 5-1

CH 6-2

CH 6-1

CH 7-2

CH 7-1

CH 2-2

CH 2-1

CH 3-2

CH 3-1

CH 4-2

CH 4-1

CH P-2

CH P-1

CH 0-2

CH 0-1

CH 1-2

CH 1-1

WRITE READY

WRITE READY

OSC OUT

CH 2 IN

CH 5 IN

CH 4 IN

CH 3 IN

TYPE 2436 WRITE AMP

TYPE 2436 WRITE AMP

TYPE 2436 WRITE AMP

TYPE 2567/3454 WRITE CONTROL

TYPE 2252 PARITY GENERATOR

TYPE 2551 CRCC GENERATOR

TYPE 2555 CRC LOGIC

TYPE 2236/3620 CRC CONTROL

P3 18 17 4 3 2 1 — 10 9 8 7 6 5 — 14 13 16 15 12 11

CHAN 5 CHAN 6 CHAN 7 — CHAN 2 CHAN 3 CHAN 4 WRITE HEAD CONNECTOR — CHAN P CHAN 0 CHAN 1

TO READ INTERFACE PIN V

PM4 INTERFACE TO P1

6 R 21 16 18 14 15 9 12 13 8 11 10

CH 1 CH 0 CH 5 CH 4 CH 3 CH 2 CH 6 CH7

DATA IN

1600/360 Auxiliary Card Cage, Wiring Diagram

CONTROL TYPE 2654

This module performs the following control functions:

a. Controls forward loading.

b. Controls the rewind operation.

c. Amplifies the LOAD POINT, END OF TAPE, and BROKEN TAPE sensors' outputs.

The functions are discussed in detail below.

Forward Loading

When the power is initially turned on, the FORWARD, READY, and REWIND flip-flops are reset. Initially silicon unilateral switch Q1 does not conduct; consequently IC4E is activated by the +10 volts through R4; IC4E-10 goes low (test point B) and clears the FORWARD flip-flop IC2B/IC3D. The 0 output of the flip-flop goes high (test point A), is inverted by IC6D and clears the REWIND and READY flip-flops; thus all three flip-flops are placed in a known state before any commands are received. Once C3 charges to +8 volts through R6, Q1 conducts and the clear input of the FORWARD flip-flop, IC2B-9, goes high, enabling the flip-flop to respond to a forward command. A $\overline{\text{LOAD FORWARD}}$ command, given either by the LOAD pushbutton or through the interface, sets the FORWARD flip-flop; the 0 output of the flip-flop (test point A) goes low, is inverted by IC5B, and turns on transistor Q3; the collector of the transistor is grounded and the FORWARD RELAY COIL is activated through output pin H. In addition IC6D-11 goes high, is inverted by IC7B, and generates a low output at pin F to drive the FORWARD LAMP. IC6D-11 high also disables OR gate IC6B-4, causing IC6B-6 to go low, since IC6B-5 is held high by the 0 output of the cleared READY flip-flop. IC6B-6 low disables NAND gate IC5C, IC5C-8 going high and charging C12 up until the firing point of SUS Q8 is reached, at which point Q8 conducts, causing IC5F-12 to go high. This disables OR gate IC1B, since IC1B-4 is kept high by the cleared REWIND flip-flop, and IC1B-3 is kept high by the collector of Q6 (unless broken tape has been detected). The output of IC1B-6 goes low (test point E), and $\overline{\text{OSC RUN}}$ becomes true (low) at output pin R. $\overline{\text{OSC RUN}}$ true accelerates the oscillator on the stepper logic module, driving the stepper motor forward at 1000 steps per second. The tape is loaded until the BOT sensor detects beginning of tape, at which point input pin Y goes high and turns on transistor Q2; the collector of Q2 is grounded, setting the READY flip-flop at IC1A-2. The 0 output of the flip-flop goes low, activating OR gate IC6B. If the $\overline{\text{LOAD FORWARD}}$ input at pin P has returned to a high state, meaning that the command has been terminated, NAND gate IC5C is activated, IC5C-8 going low; SUS Q8 stops conducting, IC4-13 is activated, IC4F-12 going low and activating IC1B-5; IC1B-6 goes high (test point E) and $\overline{\text{OSC RUN}}$ command is terminated at output pin R. However, the gap timing module holds $\overline{\text{OSC RUN}}$ low until the BOT gap is completed. When the READY flip-flop is set, its 0 output goes low, is inverted by IC6C, and enables NAND gate IC6A-1. If WRITE SELECT (input pin M) is true, IC6A is activated, IC6A-3 goes low, and

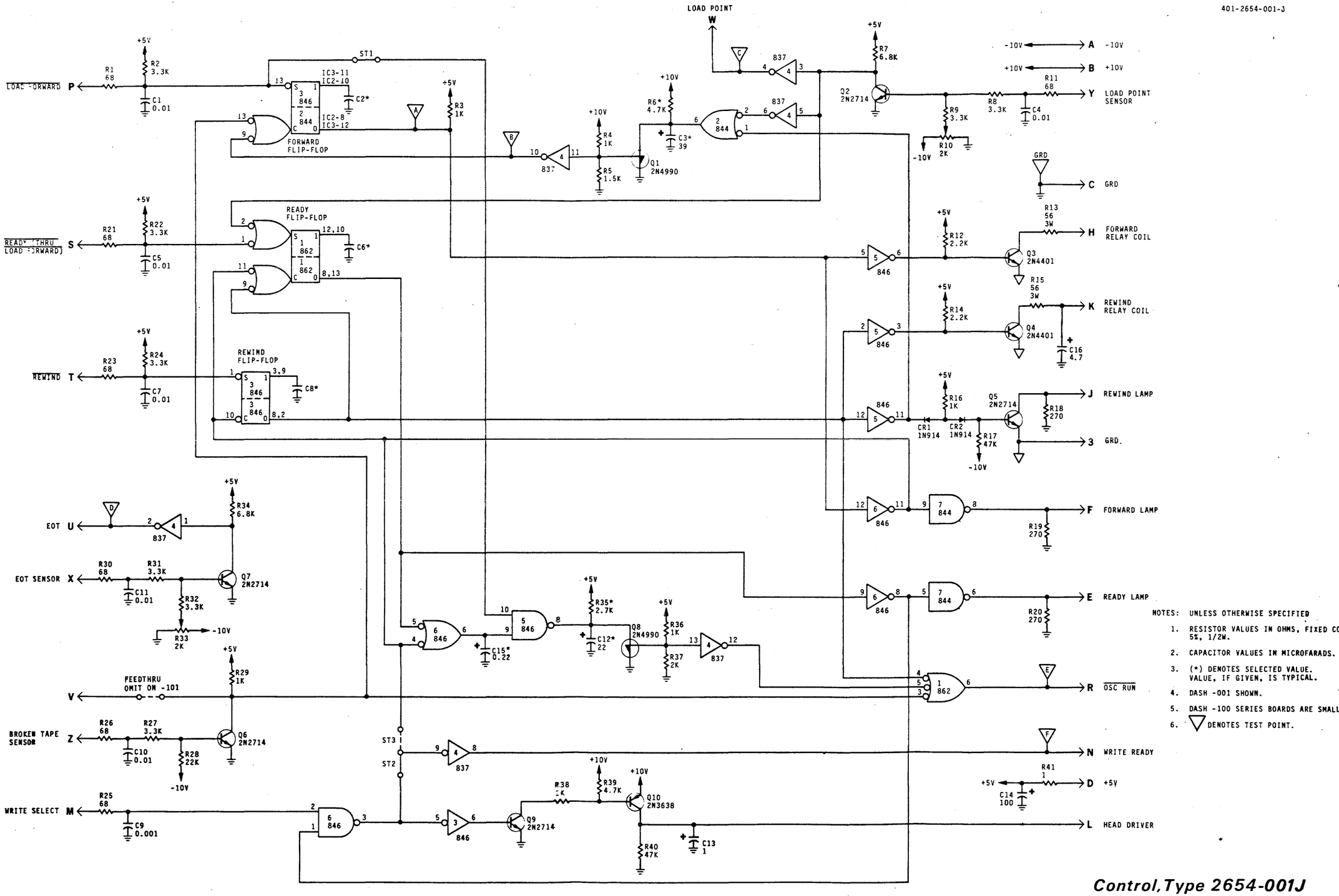
is inverted by IC3B and IC4D. IC4D generates WRITE READY true (high) at pin N, test point F. IC3B-6 turns on transistor Q9, whose collector turns on transistor Q10; the collector of Q10 supplies +10 volts HEAD DRIVE voltage at output pin L. The head drive is the center tap voltage on the write head.

If the tape is broken, or is rewound completely off the takeup reel, the BROKEN TAPE SENSOR input at pin Z goes high, turning on transistor Q6; the collector of Q6 is grounded, generating a low output at pin V, and resetting the FORWARD flip-flop, which in turn resets the READY and the REWIND flip-flops. In addition, OR gate IC1B-6 is activated, setting $\overline{\text{OSC RUN}}$ false at output pin R.

Rewinding

When a REWIND command is given, either by the front panel pushbutton or through the interface, input pin T goes low and the REWIND flip-flop is set. The 0 output of the flip-flop clears the READY flip-flop, disabling the HEAD DRIVE and WRITE READY outputs. In addition, the 0 output of the REWIND flip-flop is inverted by IC5A and IC5D. IC5A-3 high turns on transistor Q4, grounding output pin R, which activates the REWIND RELAY COIL. IC5D-11 high turns on transistor Q5; the grounded Q5 collector drives the rewind lamp through output pin J. At the same time OR gate IC1B-6 is kept high, and $\overline{\text{OSC RUN}}$ is kept false. Rewinding is terminated when the FORWARD flip-flop is cleared by either a broken tape input or by the BOT input. Note that during rewinding the 0 output of the REWIND flip-flop keeps IC5D-11 high, therefore OR gate input IC2A-1 is high as well. When BOT is detected, input pin Y goes high, transistor Q2 is turned on, and its collector is grounded; IC4C-6 then goes high, OR gate IC2A is disabled, IC2A-6 going low. This prevents SUS Q1 from conducting, IC4E-11 is activated, IC4E-10 (test point B) goes low and resets the FORWARD flip-flop. The FORWARD flip-flop in turn resets the REWIND flip-flop, and rewinding is terminated. When the collector of Q2 is grounded IC4B-4 also goes high, generating LOAD POINT true (high) at output pin W (test point C).

401-2654-001-J



NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2W.
2. CAPACITOR VALUES IN MICROFARADS.
3. (*) DENOTES SELECTED VALUE. VALUE, IF GIVEN, IS TYPICAL.
4. DASH -001 SHOWN.
5. DASH -100 SERIES BOARDS ARE SMALLER.
6. ▽ DENOTES TEST POINT.

Control, Type 2654-001J
Schematic Diagram

GAP TIMING TYPE 2655

This module performs the following timing functions:

a. Provides the timing circuit for the interrecord gap (IRG).

b. Provides the timing for the end of file gap (EOF).

c. Provides the timing for the beginning of tape gap (BOT).

The interrecord gap incorporates the timing delays supplied by the IRG one-shot and the Delay one-shot. The longer gaps, namely the EOF and BOT gaps, incorporate the delays supplied by the EOF one-shot, as well as those supplied by the IRG and Delay one-shots. Each delay circuit will be described only once; for details of the subcomponents refer to the appropriate paragraphs.

Interrecord Gap and Delay Circuitry

An IRG command at input pin U is routed through IC7B to set the IRG flip-flop IC2C-9, 10. The 1 output of the flip-flop goes high, is inverted by IC8C, IC8C-8 goes low and fires the IRG one-shot. The IRG one-shot consists of Darlington transistors Q4, Q5, silicon unilateral switch Q6, and associated components. When IC8C-8 goes low, it grounds the base of Q5. As Q5 is turning off, its collector charges up through R36, supplying current to the base of Q4; the emitter of Q4 supplies current back to the base of Q5, causing it to turn off linearly. Consequently the collector of Q5 charges up linearly until it reaches approximately 6.2 volts, at which point SUS Q3 fires and clears the IRG flip-flop at IC2A-13. The interrecord gap duration can be controlled by adjusting R41, to compensate for different character densities and step lengths in the various recorders. When the IRG flip-flop is set, its 0 output (test point B) goes low, is inverted by IC3A and IC3B; IC3B-6 goes low, generating COUNT INHIBIT low at output pin Z (test point H). COUNT INHIBIT is supplied to the stepper logic module where it presets the $\overline{\text{LCC}}$ position counter during the BOT gap, and later either enables or inhibits the $\overline{\text{LCC}}$ counter as required. In addition, the 0 output of the IRG flip-flop low sets flip-flop IC2B/IC6D.

The 1 output (IC2B-6, 13) of the flip-flop goes high and activates NAND gate IC6C-10, provided that WRITE READY is true at input pin E; IC6C-8 goes low, setting $\overline{\text{OSC RUN}}$ true (low) at output pins F and M. $\overline{\text{OSC RUN}}$ is supplied to the stepper logic module where it accelerates the oscillator to 1000 steps per second in order to drive the stepper motor during the gap. $\overline{\text{OSC RUN}}$ low is also routed to NAND gate IC4C-9, causing IC4C-8 to go high and $\overline{\text{GAP IN PROCESS}}$ ($\overline{\text{GIP}}$) to go true (low) at output pin Y, and GIP to go true at output pins J, N, and R. When the IRG one-shot clears the IRG flip-flop, the 0 output of the flip-flop goes high, is inverted by IC3A-3, and generates a negative-going pulse through C14 to OR gate IC3D-13; this fires the Delay one-shot. The purpose of the delay one-shot is to hold $\overline{\text{GIP}}$ low, after the IRG flip-flop has been cleared, inhibiting any step commands while

$\overline{\text{OSC RUN}}$ goes false. This allows the oscillator to decelerate from the gap rate of 1000 counts per second to the normal stepping rate. The delay one-shot functions as follows: The negative pulse into IC3D is inverted twice by IC3D and IC4D, and clears flip-flop IC2B/IC6D, setting $\overline{\text{OSC RUN}}$ false. IC4D-11 false keeps NAND gate IC4C disabled after $\overline{\text{OSC RUN}}$ has gone high until capacitor C15 charges up and activates IC4C-10. This keeps $\overline{\text{GIP}}$ true until the stepper motor has had time to recover.

End of File Circuitry

END OF FILE command, given either by the pushbutton at input pin W or by the interface at input pin T, sets the EOF flip-flop at IC1B-5. The 1 output of the flip-flop goes high, is inverted by IC1C and fires the EOF one-shot. The EOF one-shot operation is identical to that of the IRG one-shot described above. When the EOF flip-flop is set, its 0 output (test point A) goes low and sets flip-flop IC2B/IC6D, which in turn sets $\overline{\text{OSC RUN}}$ true at input pins F and M, advancing the stepper motor during the EOF gap. Following the delay, the EOF one-shot clears the EOF flip-flop. The 0 output of the flip-flop (test point A) goes high, is inverted by IC6B-6, and generates a negative-going pulse through C9. This pulse is inverted by IC5D-11 and activates NAND gate IC5C-8, provided that the BOT flip-flop is cleared, indicating that this is not a BOT sequence. In that case IC5C-8 goes low, generating the $\overline{\text{FILE MARK}}$ pulse at pin A, test point C. The negative-going pulse generated by C9 is also supplied to IC7B-5, activates the OR gate, and sets the IRG flip-flop, initiating the IRG sequence after the file mark is written. Thus an IRG gap is generated after the EOF gap, and the end of file sequence is complete.

BOT Circuitry

When the tape is at load point and the transport is in the WRITE READY state, input pins K and E go high and activate NAND gate IC6A; IC6A-3 goes low, generating a negative-going pulse through C11 which sets both the BOT flip-flop IC5A-1, and the EOF flip-flop IC1B-4. This initiates the End-of-File gap sequence, as described above. In addition, when the BOT flip-flop is set, its 0 output goes low and generates a pulse through C13 which sets the IRG flip-flop, thus initiating the IRG sequence. Since the EOF gap is much longer, the initial IRG sequence has no effect. At the end of the EOF sequence, the IRG sequence is initiated again; this time the IRG is stepped following the EOF gap, and is followed by the Delay one-shot delay. Note that when the EOF flip-flop is reset during the BOT sequence, the $\overline{\text{FILE MARK}}$ pulse at output pin H is inhibited, since the 0 output of the BOT flip-flop disables NAND gate IC5C.

401-2655-001-K

IRG CMD (RECORD GAP) U
GRD C
+5V D
GIP Y
GIP (GAP IN PROCESS) J
N
R
EOF PUSH BUTTON W
EOF CMD (END OF FILE) T
-10V A
+10V B
LOAD POINT K
WRITE READY E
FILE PROTECT COMMON L

R2 68, C2 0.001, IC7A 846, IC7B 846, IC7C 846, IC7D 846, IC8C 846, IC8B 846, IC8A 846, IC8D 846
R1 1, C1 100
R42 680, C7 0.001 *, R8 3.3K, C8 0.01, R9 6.8K
R31 470, R32 470, R33 8.2K, R37 SEE TABLE, CR5 1N914, CR6 1N914, R34 1K, Q4 2N2714, R38 27K
R36 2.2K, CR7 1N270, CR8 1N270, C16 *3.3, R35 100, Q5 2N2714, Q6 2N4990
R39 2.7K, R41 IRG TIMING 2K ADJUSTMENT, R40 3.3K
R46 68, C18 0.001, R47 1K, IC3C 846
P COUNT ENABLE
Z COUNT INHIBIT
PRESET
IC2C 862, IC2A 862, IRG (S 1, C 0, 8,1 9,10 12,11), IRG ONE SHOT
ST1, ST2
R30 47*, C15 *4.7, DELAY ONE SHOT, IC4D 849, IC4C 849, IC4A 849, IC4B 849
R28, R29 6.8K, IC3D 846, R26 3.3K, R27 6.8K
IC28 862, IC6D 846
R14 1K, IC3A 846, IC3B 846, C14 0.0033
CR11 1N270
IC6C 846, CR9 STRAP, R15 68, C12 0.001
F OSC RUN
M OSC RUN
ST3
R4 2.2K, R3 68, C3 0.1
R5 68, C4 0.001
R44 3.3K, R43 6.8K
IC1B 862, IC1A 862, EOF (S 1, C 0, 6,2 12,3), IC1C 862
R21 2.2K, *C17 39, R20 100, CR3 1N270, CR4 1N270, R24 2K, R25 2K *
R16 470, R17 470, R18 8.2K, CR1 1N914, CR2 1N914, R19 1K, Q1 2N2714, R22 SEE TABLE, R23 27K, Q2 2N2714, Q3 2N4990
EOF ONE SHOT
R6 68, C5 0.001, IC6A 846, C11 0.01, R12 3.3K, R13 6.8K
R7 68, C6 0.001
CR10 OMIT
IC5A 846, IC5B 846, BOT, C13 0.047, R45 680
IC6B 846, C9 0.01, R10 3.3K, R11 6.8K, IC5D 846, IC5C 846
H FILE MARK

8. DASH 300 SERIES BOARDS ARE SAME AS DASH NUMBERS SHOWN EXCEPT R37 IS CHANGED TO 33K FOR FAST GAP OPERATION.

7. DASH 200 SERIES BOARDS ARE SMALLER VERSIONS OF DASH NUMBERS SHOWN AND R37 IS CHANGED TO 33K.

DASH NO.	-001D	-002F	-003D	-004D	-007A	
FIRST USED ON	1510	1510	1510/360	1510IR	1600V	
SPEED	500	500	500	300	1500	
DENSITY	200BPI	556BPI	800BPI	200BPI	556BPI	
R37	100K	270K	300K	180K	120K	
R22	33K	91K	120K	68K	47K	

6. DASH 001 SHOWN.

5. DASH-100 SERIES BOARDS ARE SMALLER VERSIONS OF DASH NO.S SHOWN. NO OTHER CHANGES

4. (*) DENOTES SELECTED VALUE (VALUE GIVEN TYPICAL)

3. ▽ DENOTES TEST POINT

2. CAPACITOR VALUES IN MICROFARADS

1. RESISTOR VALUES IN OHMS 5%, 1/2W.

NOTES: UNLESS OTHERWISE SPECIFIED

Gap Timing, Type 2655, Schematic Diagram

STEPPER LOGIC TYPE 2677

This module contains the following components:

a. An oscillator used to advance the stepper motor during gaps or during slewing operations.

b. A longitudinal check character position counter, used to generate the $\overline{\text{LCC}}$ position pulse.

c. Stepper logic circuitry used to advance the stepper motor.

Oscillator

$\overline{\text{OSC RUN}}$ low (input pin J) or SLEW INPUT high (input pin H) activates OR gate IC10-11, causing inverter IC1-8 to go low and ground the base of transistor Q1. The collector of Q1 is then charged through R6 until it is clamped at +10 volts by zener diode CR4. Resistor R5 and capacitor C3 provide a feedback loop from the collector to the base of Q1, providing for a linear acceleration of the oscillator to 1000 counts per second over a time period determined by R5, R6, R7, and C3. Once the collector of Q1 goes positive, capacitor C4 starts charging up until it reaches +8 volts, at which point silicon unilateral switch Q2 conducts, causing SUS Q3 to stop conducting and simultaneously discharging capacitor C4. Once C4 is discharged, Q3, which has been charged through R11, conducts, generating a negative going pulse through capacitors C6, C7, and C8 into the base of transistor Q4, which is normally biased on through R13. The collector of Q4 then transmits a positive pulse to IC2-3; after being inverted through IC2-8, the pulse is output at pin P as the oscillator output, and is supplied to the interface connector. On this module the oscillator pulses are used in the stepper logic circuitry and the $\overline{\text{LCC}}$ counter, as discussed below. The external oscillator input at pin F is used only in the incremental read recorders. In those recorders the external oscillator input high at pin F causes IC1-3 to go low, setting IC3-6 (test point H) low as well. The stepping proceeds as for the internal oscillator.

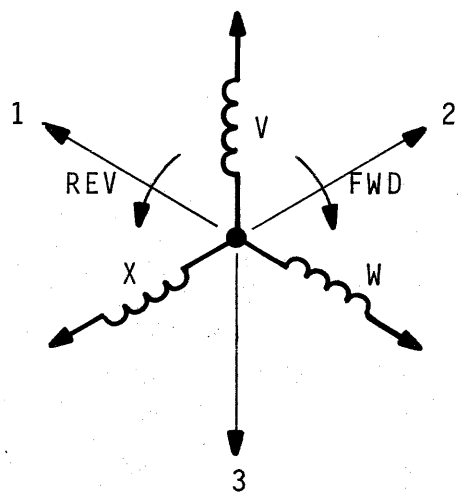
$\overline{\text{LCC}}$ Counter

Divide-by-16 counter IC12 is used to generate the Longitudinal Character Check position pulse $\overline{\text{LCC}}$. During the data block, COUNT INHIBIT from the gap timing module is true at input pin K, and holds the $\overline{\text{LCC}}$ counter cleared. When a gap is detected, COUNT INHIBIT goes false, enabling the $\overline{\text{LCC}}$ counter. In shutterless transports the counter is advanced by the oscillator pulse, fed from IC2-8 through strap 5 to the clock input of IC12; strap 4 is omitted in this case. On transports with shutters, the counter is advanced through strap 4 by flip-flop IC5/IC3, which in turn is toggled by the shutter pulses, as described in the stepper logic paragraph below; in this case strap 5 is omitted. The outputs of the counter, as well as the clock, are supplied to NAND gate IC13. On seven-track transports IC11-8 is activated on the fourth count of the gap, supplying $\overline{\text{LCC}}$ pulse low through output pin Z to the parity module. On nine-track transports, the $\overline{\text{LCC}}$ pulse is generated on the eighth character count of the gap.

Stepper Logic Circuitry

Two modes of forward stepping are employed in the incremental recorders. Shutterless transports employ the two-coil stepping, while transports with shutters employ the single-two-coil stepping. Note that in the reverse direction all incremental transports employ the two-coil stepping mode. The two stepping modes can best be explained with the aid of the diagram and truth tables given below. The diagram is a position reference of the motor with the three coils labeled for the pin numbers which energize them: V, W, and X. A clockwise direction on the diagram is equivalent to forward stepping by the motor, while counterclockwise direction is equivalent to reverse stepping. In the two-coil mode of stepping, the motor moves from position 1 to position 2 by turning off coil X and turning on coil W. In the single-two-coil mode of stepping the motor ends up in the two-coil position at the end of each step, namely positions 1, 2, and 3, but it takes two half-steps to accomplish it. Each step starts from the two-coil position by turning off one of the coils, which causes the motor to take a half step; the shutter output at pin Y clears flip-flop IC5/IC3 when the half-step position is reached, and the state of the counter is changed according to the truth tables shown below. This causes the motor to move a second half-step to the two-coil position and ends the step. Thus if the motor is at position 1 at the beginning of the step, coil X is turned off, leaving only coil V on, causing the motor to move to position V. When that position is reached, coil W is turned on, moving the motor to position 2. The single two-coil stepping accelerates the motor, allowing for an increased and smoother stepping rate.

A step starts when WRITE CLOCK 2 (WC2) input pin N from the write control module goes high; test point H goes low, and flip-flop IC5/IC3 is set. The 0 output of the flip-flop goes low, disabling NAND gate IC3-13, while enabling IC3-10. The flip-flop is reset in shutterless recorders through strap 2 when WRITE CLOCK 2 goes low; in recorders with shutters the flip-flop is reset by the shutter pulse (input pin Y) after it is amplified by Q5, and is supplied to the clear input of the flip-flop through strap 3; strap 5 is omitted in this case. If forward stepping is selected, input pin M goes high, enabling NAND gate IC3-12 while IC3-9 is disabled. When the flip-flop is reset, IC3-11 is activated, test point D going low, J-K flip-flop IC8 is toggled, and according to the truth tables the motor takes a step. When the



STEPPING MODES

FORWARD SINGLE/TWO COIL STEPPING

(ST2, CR10, CR11 omitted, ST3 installed)

	IC3-3	IC8		IC9		Stepper Drive I	Stepper Drive II	Stepper Drive III	
		Q	$\overline{Q}$	Q	$\overline{Q}$	Pin W	Pin V	Pin X	Position
Start	1	1	0	0	1	1	0	0	1
Step 1	0	1	0	0	1	1	0	1	V
	1	0	1	1	0	0	0	1	Z
Step 2	0	0	1	1	0	0	1	1	W
	1	1	0	1	0	0	1	0	3
Step 3	0	1	0	1	0	1	1	0	X
	1	1	0	0	1	1	0	0	1
Numbers are two-coil positions, letters are single-coil positions.									

TWO COIL STEPPING

(ST2, CR10, CR11 installed, ST3 omitted)

	Forward	IC8		IC9		Stepper Drive I	Stepper Drive II	Stepper Drive III	
	Pin M	Q	$\overline{Q}$	Q	$\overline{Q}$	Pin W	Pin V	Pin X	Position
Forward	1	1	0	0	1	1	0	0	1
	1	0	1	1	0	0	0	1	2
	1	1	0	1	0	0	1	0	3
Reverse	0	1	0	0	1	1	0	0	1
	0	0	1	1	0	0	1	0	3
	0	1	0	1	0	0	0	1	2

reverse direction is selected, IC3-12 is disabled while IC3-9 is enabled by pin L high; in this case the stepping is controlled by the 1 output of flip-flop IC3/IC5; when the flip-flop is set IC3-8 is activated, test point D going low, and flip-flop IC8 is toggled again, causing the motor to take a step backward.

Note that when the REVERSE input is high, it is inverted by IC4-11, and is supplied to the clear input of flip-flop IC3/IC5, holding the flip-flop cleared as long as REVERSE is true. Consequently the 0 output is held high while the 1 output still responds to the set inputs at IC5-1 or IC5-13; thus both outputs of the flip-flop can go high simultaneously and the flip-flop action is not used when reverse direction is selected.

J-K flip-flops IC8 and IC9 are connected as a divide-by-3 counter with one of the states suppressed, namely the state in which both flip-flops are cleared. This is accomplished by supplying the $\overline{Q}$ outputs of both flip-flops to NAND gate IC4-4, 5, thus causing flip-flop IC8 to be direct set when both flip-flops are cleared. The counter enables NAND gates IC5, IC6, IC7, IC10, and IC11 in order to generate STEPPER DRIVE pulses I, II, and III, as shown in the truth tables. During forward two-coil stepping, gates IC7-12, IC7-6, IC5-6, IC10-6, IC6-3, and IC11-3 are activated. When reverse two-coil stepping gates IC7-12, IC5-8, IC7-6, IC10-3, IC6-3, and IC11-3 are activated. When forward single-two-coil stepping gates IC7-12, IC7-6, IC5-6, IC11-8, IC6-11, and IC11-3 are all activated. As shown in the truth tables, a corrective step is required in two-coil stepping when selecting FORWARD direction.

401-2677-007D

DASH NO.	007D	012A
FIRST USED ON SPEED	1600/360	1510/360
DENSITY		
C11	AS	OMIT
C17	AS	STRAP
R20	AS	STRAP
R21	AS	OMIT
R22	AS	OMIT
R23	AS	OMIT
R28	AS	STRAP
R29	AS	OMIT
R30	AS	OMIT
R31	AS	OMIT
R35	AS	OMIT
ST1	AS	STRAP
Q5	AS	OMIT

AS=AS SHOWN

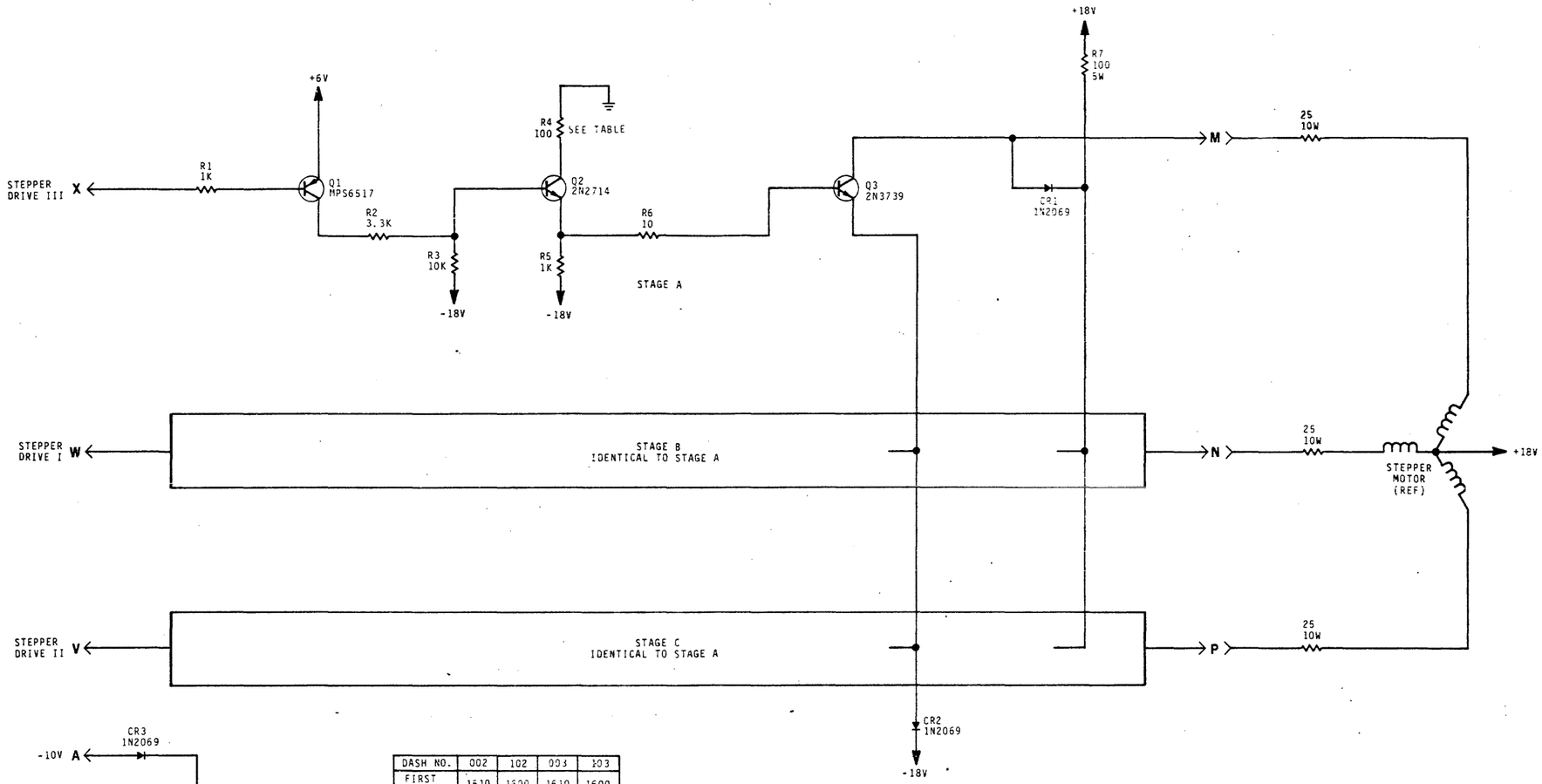
NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/4W
2. CAPACITOR VALUES IN MICROFARADS
3. ▽ DENOTES TEST POINT
4. (*) DENOTES SELECTED VALUE (VALUE IF GIVEN IS TYPICAL)
5. DASH 100 SERIES BOARDS ARE SMALLER VERSIONS OF DASH NUMBERS SHOWN
6. UNUSED IC INPUTS MAY BE TIED TOGETHER OR TO +5V

Stepper Logic, Type 2677
Schematic Diagram

STEPPER POWER AMPLIFIER TYPE 2528

This module consists of three stages of a noninverting power amplifier, one for each winding of the stepper motor. Each stage consists of three transistors, as shown for stage A. When STEPPER DRIVE III (input pin X), supplied from the stepper logic module, goes high, it biases the base of transistor Q1 off; the collector of Q1, in turn, turns transistor Q2 off, causing Q3 to be turned off as well. Consequently, the corresponding motor winding is de-energized. When STEPPER DRIVE III goes low, transistor Q1 is turned on, and its collector supplies current to the base of Q2. Q2 then turns on Q3, grounding its collector and energizing the corresponding motor winding. Stages B and C on this module operate similarly.



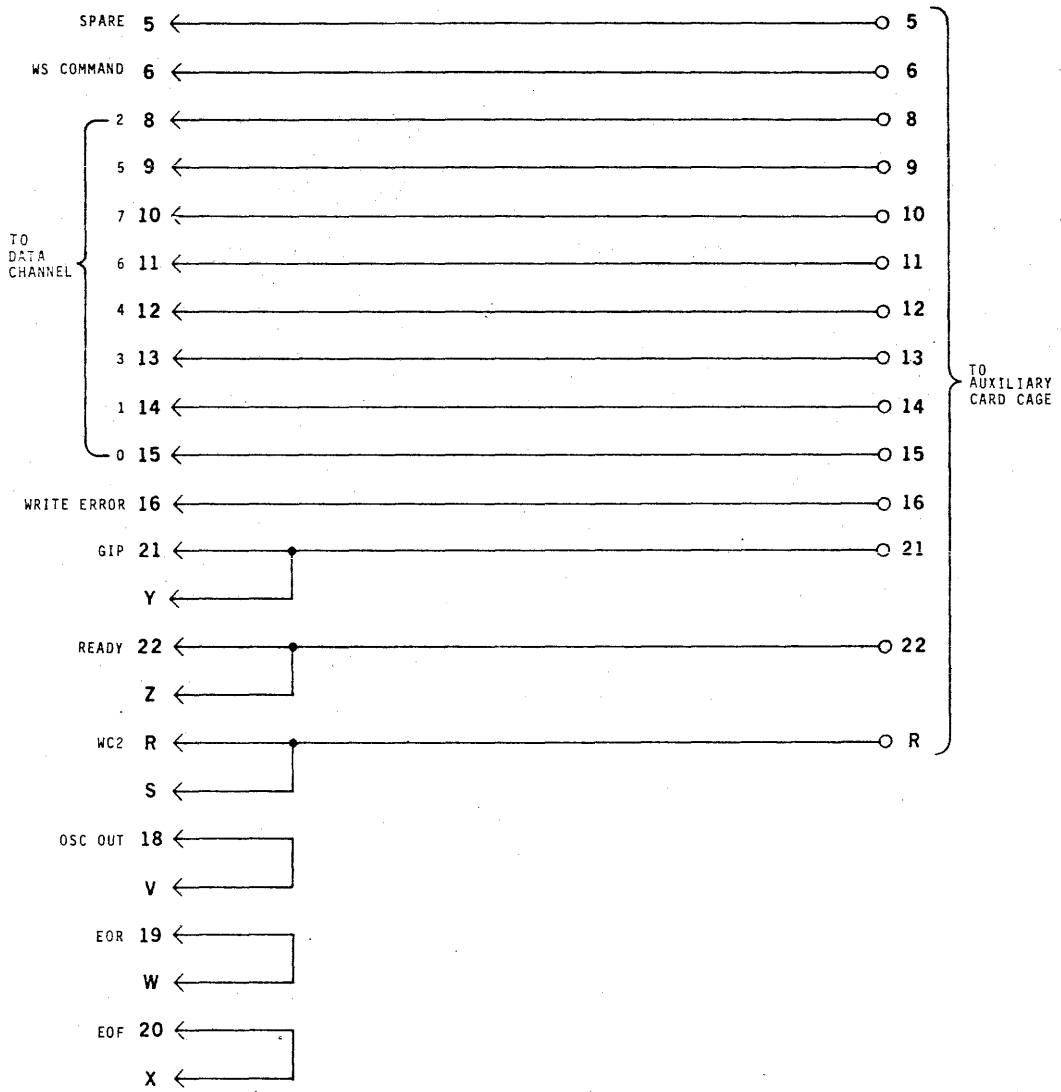
DASH NO.	002	102	003	103
FIRST USED ON	1510	1600	1610	1600
SPEED				
DENSITY				
R4	AS	AS	270/2W	270/2W

AS=AS SHOWN

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2W.
2. CAPACITOR VALUES IN MICROFARADS.
3. ▽ DENOTES TEST POINT.
4. UNUSED IC INPUTS MAY BE TIED TOGETHER OR TO +5V.
5. (*) DENOTES FACTORY TEST SELECT. VALUE, IF SHOWN, IS TYPICAL.
6. DASH 100 SERIES BOARDS ARE NARROW VERSIONS OF DASH NO.S SHOWN.

Stepper Power Amplifier, Type 2528, Schematic Diagram



Interface, Type 2569-001A, Schematic Diagram

1600/360 WRITE CONTROL TYPE 3454

This module performs the following write control functions:

a. Detects the shutter output peaks, supplying SHUTTER OUTPUT and SHUTTER TRAILING EDGE outputs.

b. Generates WRITE CLOCK 1 and WRITE CLOCK 2.

c. Provides the WRITE ERROR OUTPUT.

These functions are discussed in detail below.

Shutter Pulse Detection Circuitry

The shutter optical pickup is supplied from the stepper motor at input pin F. When a shutter peak is detected, the output of operational amplifier IC12 swings from +10 to -10 volts, supplying a negative pulse through capacitor C16 into the base of transistor Q1, which is normally biased on by R16. The collector of Q1 then swings positive. When Q1 collector goes positive the two pulse-forming circuits (consisting of IC8-8, C11, IC9-11, and IC8-6, C9, IC7-8) generate 15 μsec negative going pulses. The pulse output by IC9-11 is inverted by IC9-4 and is output at pin 7 (test point D) as the SHUTTER TRAILING EDGE PULSE. IC7-8 is activated following a delay of approximately 1.5 μsec determined by C10, provided WRITE/STEP flip-flop IC4 has been set. The output of IC7-8 is inverted by IC9-10 and is supplied to output pin 8 (test point C) as SHUTTER OUTPUT. In addition, the pulse output by IC7-8 is supplied to another pulse-forming circuit consisting of IC10-6, C7, IC10-8, C6; this circuit generates a delayed pulse on the trailing edge of the shutter pulse; the output of IC10-8 is used to clear the WRITE/STEP flip-flop IC4, at the end of the step. The delay is provided to allow the $\overline{\text{ERROR}}$ input at pin 9 to high before flip-flop IC4 is cleared.

Generation of WRITE CLOCKS 1 and 2

The WRITE/STEP COMMAND (input pin K, test point A, from interface II module) is supplied to a pulse-forming circuit consisting of IC5-8, C2, IC5-6 and C3. When WRITE/STEP COMMAND goes high, IC5-6 generates a 5 μsec negative-going pulse, provided that WRITE READY (input pin E) is true at IC5-2, and $\overline{\text{GAP IN PROCESS}}$ is false (high) at IC5-1. The pulse is delayed approximately 5 μsec by C3 on extender IC5-3. The delayed pulse sets the WRITE/STEP flip-flop IC4-13; the 0 output of the flip-flop goes low and is inverted by IC3-6, setting test point H high and activating the pulse-forming circuit consisting of IC11-6, C4 and IC6-11. IC6-11 outputs a negative-going, 5 μsec pulse (test point J) supplied to the output at pin 13 as $\overline{\text{WRITE CLOCK 1}}$ ($\overline{\text{WC1}}$). $\overline{\text{WC1}}$ is also supplied to another pulse-forming circuit consisting of IC11-8, C5 and IC2-8; this circuit generates a 5 μsec negative-going pulse on the trailing edge of WC1, provided that $\overline{\text{WRITE READY}}$ is true (input pin E), $\overline{\text{GAP IN PROCESS}}$ is false (test point E high), and WRITE/STEP flip-flop IC4 has not been reset (test point H high). The pulse output by IC2-8 is supplied to output pin 4 as $\overline{\text{WRITE CLOCK 2}}$

($\overline{WC2}$); in addition, the pulse is inverted by NOR gate IC2-6 and is output at pin 12, test point K, as WRITE CLOCK 2 (WC2). Alternatively T3 GATED at input pin H from the CRC control module is gated through IC2-6 as WC2.

WRITE READY false clears the WRITE/STEP flip-flop IC4, and the WRITE/STEP COMMAND pulses are inhibited. In addition, the WRITE/STEP flip-flop is cleared at the end of each step by the delayed shutter output pulse supplied from IC10-8, as discussed in the shutter circuitry paragraph above. Once flip-flop IC4 is cleared and a gap is detected, GAP IN PROCESS high at pin 10 and the 0 output of IC4 high activate NAND gate IC6-4, generating a low level (test point E) which is output at pin 11 as $\overline{\text{GAP IN PROCESS}}$. $\overline{\text{GIP}}$ is supplied to the CRC control module where it initiates the CRC generation. In addition, $\overline{\text{GIP}}$ true (low) inhibits IC5-1, preventing flip-flop IC4 from being set by any following WRITE/STEP pulses; $\overline{\text{GIP}}$ low also disables NAND gates IC2-10 and IC7-2, inhibiting WRITE CLOCK 2 and the WRITE ERROR OUTPUT.

WRITE ERROR OUTPUT

$\overline{\text{ERROR}}$ input true (low) at pin 9, supplied from the write amplifier modules, is inverted by IC9-3 and enables the error NAND gate IC7-5. The gate is activated provided that WRITE READY is true at IC7-4, $\overline{\text{GAP IN PROCESS}}$ is false at IC7-2, and the WRITE/STEP flip-flop IC4 has been cleared at the end of the step; in this case IC7-6 generates a negative-going pulse, which is inverted by IC6-3, and is output at pin 6 (test point F) as ERROR OUTPUT true.

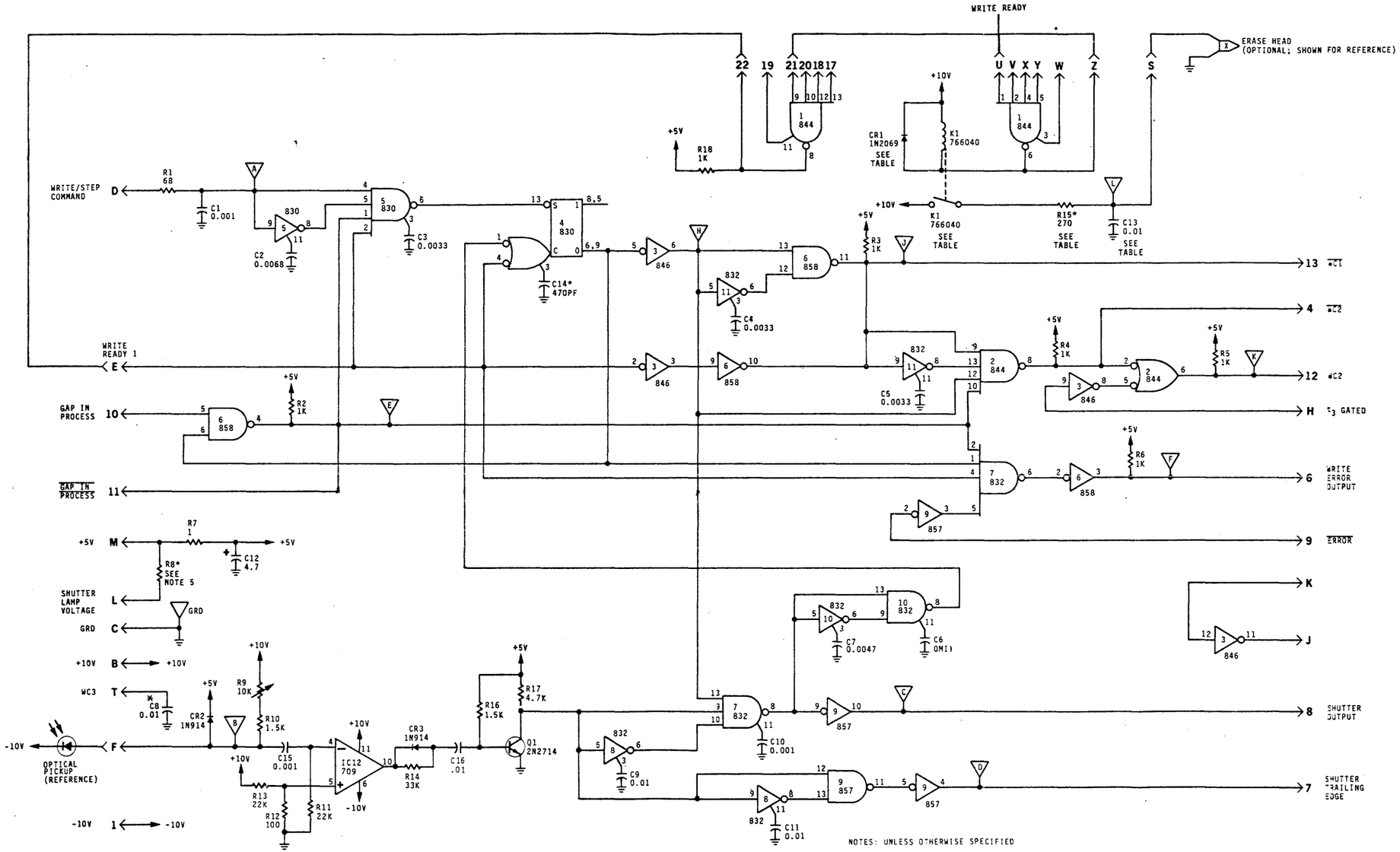
Miscellaneous Functions

The circuitry consisting of IC1, relay K1 and diode CR1 is used when an erase head is installed. WRITE READY is supplied to pin U of IC1, enabling the gate; IC1-6 goes low and activates relay K1, closing the relay contacts and feeding +10 volts to the erase head through R15, test point L, with capacitor C13 used as a filter.

NAND gates IC1 and IC3 are two spare gates which are used in certain incremental configurations.

Resistors R7 and R8, and capacitor C12 are used to control the voltage of the shutter lamp, located behind the shutter in recorders with shutters.

401-3454-001-H



DASH NO.	-001K	-002H	-003F
C13	OMIT	OMIT	AS
CR1	OMIT	OMIT	AS
K1	OMIT	OMIT	AS
R15	OMIT	OMIT	AS

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2W.
2. CAPACITOR VALUES IN MICROFARADS.
3. ▽ DENOTES TEST POINT.
4. (*) DENOTES FACTORY TEST SELECT. VALUE, IF SHOWN, IS TYPICAL.
5. R8 IS 22 OHMS ON RECORDERS WHICH HAVE +6V SUPPLY, AND IS 10 OHM ON RECORDERS WHICH HAVE +5V SUPPLY.
6. R9 ADJUSTED TO OPTICAL PICKUP SO THAT TEST POINT 8 SHUTTER PULSES GO TO GROUND WHEN STEPPER MOTOR IS SLEWING.

1600/360 Write Control
Type 3454
Schematic Diagram

TYPE 2436 WRITE AMPLIFIER

CARD PURPOSE

Type 2436 Write Amplifier is a standard general purpose Write Amplifier which can be readily adapted to write in the normal NRZI fashion or to pulse the write head, and may include the Echo Check or Flux Check error checking techniques. (See Sheet 2 of the schematic diagram.)

CIRCUIT DESCRIPTION

NRZI Recording

Stages A, B, and C on this card are identical, and the signal logic described for Stage A also applies to Stages B and C. The main objective of each stage is to cause current in the write head to reverse polarity each time a binary one (high level) signal appears in the data flow. This is accomplished in the following manner.

A positive (high data level) pulse appears at Pin 4. $\overline{WC1}$ (Pin 13) clears storage flip-flop IC1B/IC1C. WC2 appears at IC1A producing a negative (low) signal at the set input of IC1B/IC1C. This produces a positive level gate at S1 and C1 of flip-flop IC2. When Clock Pulse WC3 (Pin 16) arrives, its trailing edge causes IC2 to transfer, reversing state. Since WC4 is held high in the normal usage of this card, this causes the head driving chains of IC3A, IC3B, Q1, and IC3D, IC3C, Q2 to be alternated from the state they were in for the previous positive bit. The current flows in the other coil of the write head and produces a flux change in the head gap, resulting in the recording of a signal on tape which is interpreted as a "1" in that position.

When a 0-bit appears at Data I terminal 4, the output of IC1A will not set flip-flop IC1B/C. Since no changes can occur in the driving chains, current in the head remains static resulting in no flux change in the head gap, which is interpreted as a "0" in that position.

Inputs are provided to the SD and CD connections of IC2. SD is used for returning IC2 to reference condition for the Longitudinal Check Character to be written.

CD is brought out for each channel to allow writing the File Mark.

Pulse timings given are nominal values. Timing is not critical, allowing circuit operation without adjustment. Because of component tolerances, actual times may vary somewhat.

Signal	Nominal
WC1	10 usec
WC2, 3	10 usec
WC4	+6V Level

Echo Check

When this option is used, a negative level $\overline{\text{Error}}$ signal appearing at Pin 12, at the appropriate time, causes an error to be registered in an external circuit. Refer to the following diagram which illustrates three consecutive "1's" the middle one of which results in an error. In this description, it is presumed that the preceding "1" left the following static conditions:

Pins 6, 9 of IC1B/IC1C are Low.

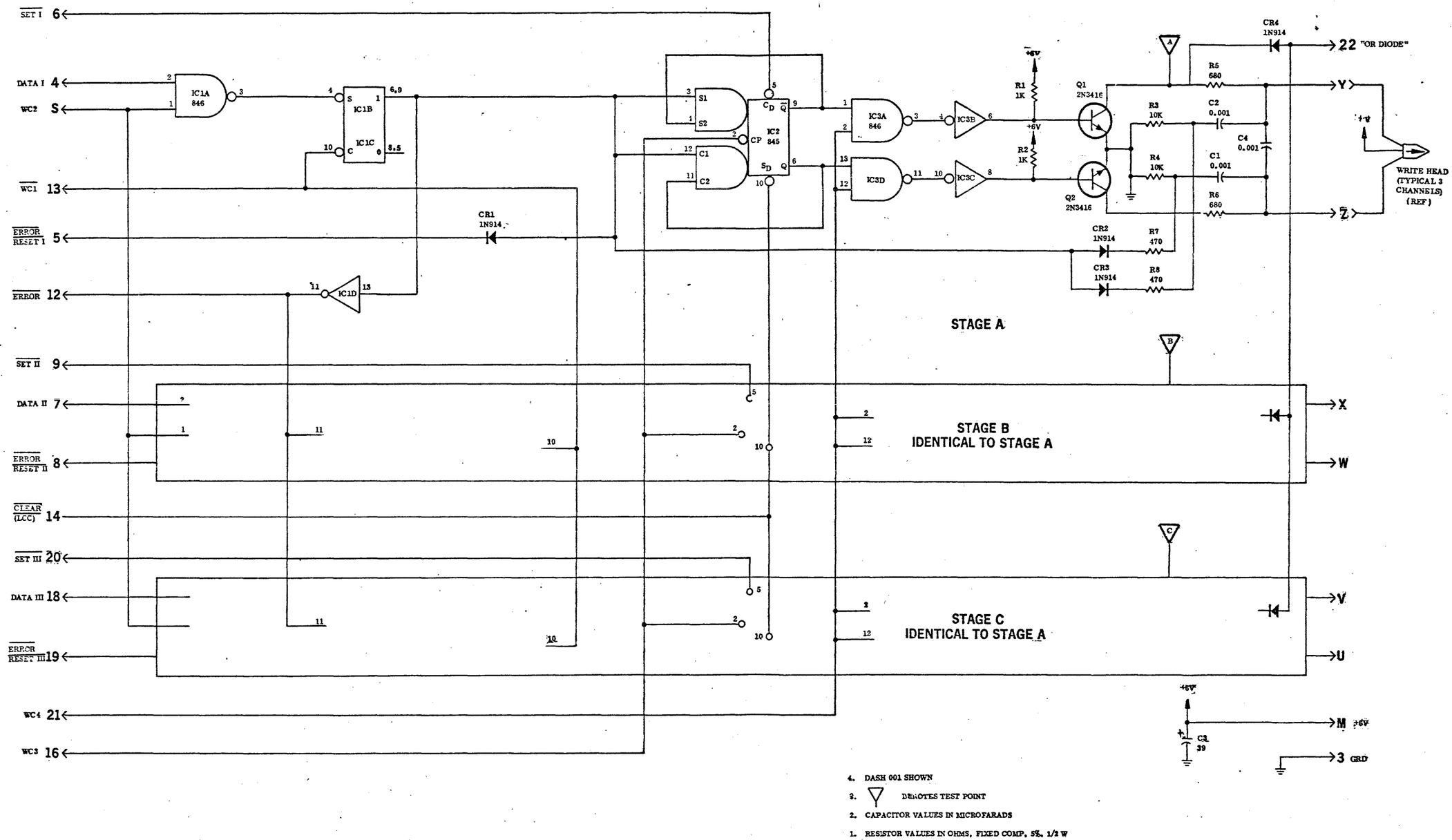
Pins 9, 4 of IC2 are High.

Write Head Y-Side is saturated.

When the next "1" is received, flip-flop IC1B/C sets and a positive gate is produced through S1-S2 of IC2 at trailing edge time of WC3. This produces a negative level at $\overline{Q}$ and a positive level at Q (this state remains until the next data "1" causes reversal). IC3A then cuts off and IC3D conducts. This reverses polarity through the Write head, causing the Z-Side to conduct heavily. At the reversal, the negative inductive spike produced at Pin Y is fed back through diode CR3 to IC1B/IC1C causing it to reset and the Echo Check $\overline{\text{Error}}$ level to go high (through inverter IC1D).

At the second Write/Step command the logic flow proceeds normally, except flip-flop IC1B/IC1C is not reset by the inductive flyback from the Write head. The EC $\overline{\text{Error}}$ thus remains low and an error is registered. The $\overline{\text{Error}}$ line is gated appropriately so that no spurious outputs will occur on the Error Output line to the interface plug.

At the third Write/Step command $\overline{\text{WC1}}$ clears IC1B/IC1C so that IC1A may set flip-flop IC1B/C at WC2 time and circuit operation returns to normal.



4. DASH 001 SHOWN
3. ▽ DENOTES TEST POINT
2. CAPACITOR VALUES IN MICROFARADS
1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2 W

NOTES: UNLESS OTHERWISE SPECIFIED

Write Amplifier, Type 2436,
Schematic Diagram
Sheet 1 of 2

DASH NO.	-001	-002	-003	-004	-005	-006	-007	-008	-009	-010
FIRST USED ON	1400 EC	1400 FC	3710 -001	3710 -002	1600 360	1814 EC				
SPEED	300	300	43.16IPS	5.4IPS	500	300				
DENSITY	200	200	556	556	800	200				
C1		OMIT	OMIT	AS	AS	AS				
C2		OMIT	OMIT	AS	AS	AS				
C4		AS	OMIT	OMIT	AS	OMIT				
CR1		AS	OMIT	BUS	STRAP	AS				
CR2		OMIT	OMIT	AS	AS	AS				
CR3		OMIT	OMIT	AS	AS	AS				
R3	AS SHOWN	OMIT	OMIT	AS	AS	AS				
R4		OMIT	OMIT	AS	AS	AS				
R5		220/2W	1.2K	1.2K	470	AS				
R6		220/2W	1.2K	1.2K	470	AS				
R7		OMIT	OMIT	AS	AS	AS				
R8		OMIT	OMIT	AS	AS	AS				
IC1		AS	AS	AS	AS	946				
IC2		AS	AS	AS	AS	945				
IC3		AS	AS	AS	AS	946				
Q1		AS	AS	AS	AS	2N2222				
Q2		AS	AS	AS	AS	2N2222				
CR4	OMIT	OMIT	OMIT	OMIT	OMIT	AS				

REV - REVERSED
AS - AS SHOWN

Write Amplifier, Type 2436 Schematic Diagram

Sheet 2 of 2

CYCLIC REDUNDANCY CHECK CHARACTER GENERATOR
TYPES 2551-001, 2555-001, AND 2236-001

CARD PURPOSE

This package is used in 9-track, 800 characters per inch recorders to generate the IBM Cyclic Redundancy Check Character (CRCC) required in IBM System 360 installations. The CRCC is located four character spaces after the final data character in a tape record. The traditional Longitudinal Check Character (LCC) is located four character spaces after the CRCC. Both characters precede the 0.6 inch (minimum) End of Record Gap.

The CRCC is used, in conjunction with circuits in the computer tape unit, to detect almost all the errors which may occur in transmission of the character from the tape to the data output interface. These circuits assume that no errors occurred during the writing operation which produced the tape. Detected errors can be electronically corrected (the tape is not altered) if they all occur in the same track of a given record. If errors occur in more than one track per record, they cannot be corrected; but an error signal is generated.

The circuits which generate the CRCC are based on a complex equation that reduces the mathematical probability of an undetected error almost to zero. The formula itself is beyond the scope of this description and is not required for an understanding of the circuits or for trouble shooting.

Functional Description

Refer to CRC Functional Logic, Drawing No. 301-2245-001. The Cyclic Redundancy Check Register (CRCR) is basically a nine-bit shift register connected as a ring counter. Data is shifted from Bit P toward Bit 0, 0 toward 1, and so on, with Bit 7 returning toward Bit P. The subsequent state of each bit is determined by the present state of the previous bit in the register, the present state of the data input to the given bit, and (in Bits 2 through 5 only) the present state of Bit 7.

In Tracks P, 0, 1, 6, and 7 the data input to the CRCR bit is compared with the present output of the previous stage in the CRCR. The comparison takes place in the first of two Exclusive OR circuits. Functionally, the Exclusive OR produces a one (high) output if its inputs are different from each other. It produces a zero (low) output if the inputs are the same (either high or low).

The output of the first Exclusive OR gate becomes one input to the second Exclusive OR. The other input is the present state of the CRCR stage under consideration. The output of the second Exclusive OR is gated by a clock pulse to the Trigger (or toggle) input of a binary-connected flip-flop. A pulse on the Trigger input causes the flip-flop to change state.

Functionally, the second Exclusive OR makes it possible to operate a Trigger (T type) flip-flop as a Set-Reset (R-S) flip-flop. For all four combinations of inputs to the second

Exclusive OR, the output of the flip-flop after the clock pulse will be a one if the output of the first Exclusive OR is a one, and a zero if the output of the first Exclusive OR is a zero.

Tracks, 2, 3, 4, and 5 are similar to the others, except that the first Exclusive OR has three inputs. The third input samples the present state of CRCR Bit 7. The output of the Exclusive OR is high if any one input or all three inputs are high. It is zero otherwise. The second stage Exclusive OR and the flip-flop are identical to those of the other tracks.

During the tape loading operation and in each End of Record or End of File Gap, the CRCR is reset to all zeros in preparation for operating on the data in the next record. Because of this and the other properties of the CRCR, the first character of a new record will pass unchanged into the CRCR. Subsequent data inputs will not, of course, reproduce themselves in the CRCR except by chance.

The CRCC written on tape is not the same as that contained in the CRCR after the last data character is written. The latter character is first shifted by an additional clock pulse (with the data inputs held at zero). The CRCR logic is such that if Bit 7 contains a zero prior to this shift, data in the CRCR will be shifted one bit in the register (that is, the contents of Bit P become the contents of Bit 0, those of Bit 0 become those of Bit 1, etc.). If Bit 7 contains a one, then the contents of Bits 1, 2, 3, and 4 will be complemented before being shifted to Bits 2, 3, 4, and 5 respectively. The remaining five bits are shifted unchanged into the succeeding bit position.

Following the extra shift, all bits except those in Positions 2 and 4 are complemented. It is this final result which is written on the tape as the CRCC.

According to IBM specifications for nine-track equipment, bits of a character are assigned the following order on tape (starting from the outside edge, the edge to which the Load Point marker is applied): 5, 7, 3, P, 2, 1, 0, 6, 4. The CRCC as written on tape will also conform to this specification.

Circuit Description

Refer to CRCC Generator Schematic Type 2551, CRC Logic Schematic Type 2555, and CRC Control Schematic Type 2236. The logic for Track 4 will be described. Logic for other tracks is similar. The control logic is also described. Integrated circuit logic (930 series DTL) is shown functionally only.

Data for Track 4 is applied at Pin N of the Type 2555 board. During normal writing (that is, not during gaps), Pin 4 of IC5B is high and Pin 2 of IC5A is low. This allows data to enable IC5B while IC5A, which gates the output of the CRCR, is inhibited. Data is passed unchanged through IC5B and IC5C to Pin K, which feeds the write amplifier data input elsewhere in the recorder. It also feeds the data input to the CRCR logic for Track 4.

The combination of IC5D, IC6B, IC6C, and the "wired AND" form a COMPARE circuit. That is, for any two inputs A and B, the logical output $C = A\,B + \overline{A}\,\overline{B}$. In other words, C is high whenever A and B are the same, whether high or low. The COMPARE circuit forms the

complement of the Exclusive OR in which a logical output $D = E \overline{F} + \overline{E} F$. In this situation, D is high whenever E and F are different. Thus, we may obtain the Exclusive OR of two inputs by inverting the output of the COMPARE circuit. The COMPARE circuit can also be made into an Exclusive OR by complementing either input A or B. That is, if $C = A B + \overline{A} \overline{B}$, then $\overline{C} = \overline{A} B + \overline{\overline{A}} \overline{B} = \overline{A} B + A \overline{B}$ when A is complemented.

By cascading two COMPARE circuits, the three-way Exclusive OR described in the Functional Description is performed. The data input for Track 4 and the state of Bit 7 are compared in the first circuit, and the output of this circuit is compared with the state of Bit 3 in the second COMPARE circuit. The output of the first COMPARE circuit is the complement of an Exclusive OR, but since it is also the (inverted) input of the second COMPARE circuit, the output of the two circuits in cascade is a true three-way Exclusive OR.

The second level Exclusive OR, described functionally in earlier paragraphs, is performed in the third COMPARE circuit (IC7D, IC7A, and IC7C). So that this circuit produces the desired Exclusive OR output to the Register IC8, the complement (or 0 output) of IC8 is fed back as the second input to this COMPARE circuit.

Data is gated into Register IC8 by a clock pulse generated during the step-and-write cycle and applied (inverted) to Pin 13 of the Type 2555 board. In Models 1400/360 and 1500/360 this pulse is derived from the output of an optical shutter assembly located on the stepper motor. In Model 1600/360, $\overline{WC2}$, derived from the input Write-Step command, is used.

The output of the shutter assembly is passed unchanged (except during gaps) through IC2B and IC1A of the Type 2236 board to the Write Amplifier Clock line (WC3). Thus, data is written on tape with the stepper motor in a known position.

Writing proceeds from character to character with each new character in the register being determined by the previous contents of the register and by the data inputs. This continues until the final character of a record has been written and a gap command (either End of Record or End of File) has been issued.

At that time, the character in the CRCR is shifted and read out to be written on the tape. The complementing of all bits except 2 and 4 is accomplished by simply reading out the zero outputs of the CRCR except for Bits 2 and 4. After readout, the CRCR must be cleared in preparation for the next data block. The remainder of the logic in the CRCC generator package is concerned with these operations.

This logic consists of a two-stage binary counter (IC19 and IC20), a decoder (IC18) which decodes counts of 0, 1, and 3, and various gating circuits. IC19 and IC20 are connected so that, once they have counted to 0, they will remain at 0 unless IC3 (on the Type 2236 board) is set. IC3 is set at the beginning of a gap and when a File Mark is written during an End of File Gap.

All timing in the gap logic is controlled by Gap Clock pulses obtained by amplifying the output of the optical shutter assembly (located on the stepper motor) during gaps. During normal writing these outputs are inhibited from this circuit by the $\overline{\text{Gap in Process}}$ level.

At the beginning of a gap, Pin L ($\overline{\text{Gap in Process}}$) of all boards goes to zero, enabling the Gap Clock circuit (described more fully below), and inhibiting the data input lines and WC3 to the write amplifiers. The zero level on Pin L also sets IC3 (on the Type 2236 board) through C2.

Setting IC3 primes the counter IC19 and IC20 (on the Type 2555 board) so that it will count when Gap Clock pulses are generated. IC3 is reset by the first Gap Clock pulse, so that IC19 and IC20 will only count to four once at the beginning of the gap.

As the count progresses, the stages of IC18 (on the Type 2555 board) decode various counts to perform specific functions. IC18A decodes t_1, which is used to perform the extra shift required of the CRCR at the end of a record. (Since the count started at 0, t_1 actually occurs on the second Gap Clock pulse.) All data inputs are inhibited by the zero level on Pin L; therefore, the outputs to the write amplifiers are at zero. These outputs are also the inputs to the CRCR logic; hence, the shift at t_1 is performed with zero on the data inputs as required.

IC18B decodes t_3 (which actually occurs on the fourth Gap Clock pulse). This pulse is gated in IC4B and IC1A of the Type 2236 board to create a clock pulse to the write amplifiers and enable all the gates controlling the readout of the CRCR (t_3 GATED). Thus at t_3, the write amplifiers see the appropriate data on their input lines and a clock pulse on the clock line. Therefore, they treat the CRCC as an ordinary data input. Thus, the CRCC is written four steps after the final data character, as required.

After the CRCC has been written, the CRCR must be reset. IC18C accomplishes this by decoding the zero, or reset, state of IC19 and IC20. This level is gated by the Gap Clock in IC1B of the Type 2236 board and applied to the Direct Clear inputs of the CRCR as $\overline{t_0}$. Subsequent Gap Clock pulses will continue to "reset" the register, but these pulses cease before any new data is entered, so no harm is done.

The $\overline{t_0}$ pulse also sets flip-flop IC4C-IC4D. This flip-flop, once set, prevents t_3 pulses from passing through IC4B to the CRCC readout gates and the write amplifier clock line. Thus, no CRCC will be written while this flip-flop is set. Since t_0 follows t_3, the desired CRCC will be written, but no others.

IC4C-IC4D is reset by the first Shutter Clock pulse to be generated after a gap. This pulse results only from external application of a Write-Step input, signifying that data is to be recorded. If another End of Record or End of File Gap input is applied instead, IC4C-IC4D remains set and inhibits the t_3 pulse generated at the beginning of the second (or subsequent) gaps.

The t_3 pulse must be inhibited because the CRCC for no input data is not a zero character. (It is ones in all tracks except 2 and 4.) The computer would interpret this lone character (and its LCC) as noise in the gap, causing (in some cases) an undesirable program termination. Since t_3 is inhibited, no LCC is generated because no write amplifiers have been set by a CRCC.

IC19 and IC20 start from 0 at the beginning of a gap. To keep this condition from being interpreted as a signal to reset the CRCR (quite prematurely), the condition of primer flip-flop IC3 is included in the decoding of the reset pulse. If IC3 is set, as at the beginning of a gap, IC18C is inhibited and no reset pulse is generated.

The output of IC17A is zero during the first four Gap Clock pulses. As such, it may be used to inhibit the "4-shot" circuits (located on another card) which write the LCC. The LCC, normally separated by four character spaces from the data on seven-channel recorders, must be moved out to the eighth character space to allow the CRCC to be written in the fourth space. The output of IC17A thus allows the LCC logic to ignore the first four Gap Clock pulses, and so proper spacing of the LCC is assured.

During an End of File Gap, a second count-of-eight sequence is produced in addition to the one at the beginning of the gap. This occurs when the File Mark is written.

The $\overline{\text{File Mark}}$ signal on Pin H (from the timing circuits) may occur at any time during the step cycle, and so it is buffered in flip-flop IC6C-IC6D. The next Gap Clock pulse sets IC3 through IC5D and IC2D. Setting IC3 primes IC19 and IC20 (the binary counter). When IC3 is set, the t_0 level is removed which inhibits further inputs to IC5D.

IC6C-IC6D is reset by the resulting t_3 pulse (before the inhibiting gate), which removes that input to IC5D before the t_0 level reappears. Thus, IC3 is set only once at this time.

IC4C-IC4D is also set during this time, having been set by the first $\overline{t_0}$ pulse of the End of File Gap. Thus, the CRCC due to the File Mark is inhibited, as described above. Since the count-of-eight sequence is otherwise normal, the File Mark Check Character will be written eight character spaces after the File Mark, as required.

IC2A, IC2C, Q5, Q6, IC6A, and IC6B on the Type 2236 board generate the Gap Clock pulses directly from the optical shutter assembly during gaps. When $\overline{\text{Gap in Process}}$ (Pin L) goes to zero during gaps, IC6A is enabled and passes outputs from Q6. The first 30 microseconds (approximately) of the shutter output are used as Gap Clock pulses. During normal writing, Pin L is high, and the output of IC2A inhibits IC6A.

The combination of R14 and C6 on the Type 2236 board form a 100 microsecond time constant filter to eliminate high frequency noise on the +5V supply line. R1 and C1 on the Type 2551 and Type 2555 boards perform a similar function.

401-2236-001-H-1

PART OF TYPE 2555.
CIRCUITS WITHIN DASHED
LINE SHOWN FOR REFERENCE
ONLY.

-10V A → -10V
+10V B → +10V
GRD C
R14 1K
+6V Z → +6V
C6 100

GAP CLOCK T

IC3 845 · IC5A 846 · IC20 845 · IC19 845 · IC18A 862 · IC18B 862 · IC18C 862 · IC17A 832 · IC17B 832 · IC6C IC6D 846 · IC5D 846 · IC2D 845

X 20 · T 16 · W 19 · V 18 · U 17 · Y 21 (NOT GATED)

TO PIN 2 OF IC4, IC8, IC12, & IC16

CRCR CLOCK S

FILE MARK H

13 WC2 (MODEL 1600/360)

4-SHOT INHIBIT

AD 13 GATED

R10 6.8K · R11 3.9K · R12 6.8K · R9 10K · Q5 2N2714 · Q6 2N2714 · IC2C 846 · C3 0.01 · IC6A 846 · IC6B 846 · C4 0.001 · IC1B 832

PHOTO-SENSITIVE ELEMENT (REF) · -10V

R13 6.8K · C5 0.001 · IC2A 846 · C2 0.01 · R8 6.8K · R7 27K

CR1 1N914 · GAP IN PROCESS L

IC4C IC4D 846 · IC2B 846 · IC4A 846 · IC4B · IC1A 832 · IC5B 846 · IC5C 846

GATED 13 M

S WC3

N SHUTTER CLOCK

R

(6) TYPE 2236 PIN P CONNECTS TO TYPE 2555 PIN 13 IN MODELS 1400/360 AND 1500/360

5. DASH -001 SHOWN
4. (*) DENOTES SELECTED VALUE (VALUE GIVEN TYPICAL)
3. ▽ DENOTES TEST POINT
2. CAPACITOR VALUES IN MICROFARADS
1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2W

NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO.	-001	-002
FIRST USED ON	1400/360	1600/360 RFC
SPEED		
DENSITY		
C3	AS	STRAP
C4	AS	OMIT

APPLIES TO	
PART NO.	REV
190-2235-001	F
190-2236-002	-

CRC Control, Type 2236

TYPE 2252 PARITY LOGIC

OPERATIONAL DESCRIPTION

The Type 2252 Parity Logic card is a general purpose modulo-2 generator which can be used with up to nine inputs. The flexible (discrete) input stages allow the card to be used for a variety of applications, while the remainder of the logic is implemented by DTL integrated circuits.

Typical seven- and nine-channel applications of the Type 2252 Parity Logic include:

1. Vertical parity generation based on data inputs for input to a parity channel. Positive or negative logic inputs may be used.

2. Parity checking of current in the write head (echo check).

3. Parity checking of read amplifier outputs in machines equipped to read tape as well as write.

4. Vertical parity generation with power applied to the card only during the write-step cycle, used in low power applications.

An additional input allows the user his choice of odd or even parity. (In odd parity systems, the total number of bits in a data character is always odd, etc.)

THEORY OF OPERATION

The modulo-2 section consists of eight groups of three two-input gates. Each of their outputs is tied together in a "wired AND" section. The logic of each group of gates is such that it produces a COMPARE output, that is, its output will be high (+5V) if both its inputs are identical (0V or +5V), and its output will be low (0V) if the two inputs are different.

The outputs of two of these groups can be used to drive a third group in a similar fashion. And so a parity tree is formed, with each input to the card ultimately contributing to the parity output of the tree seven groups later.

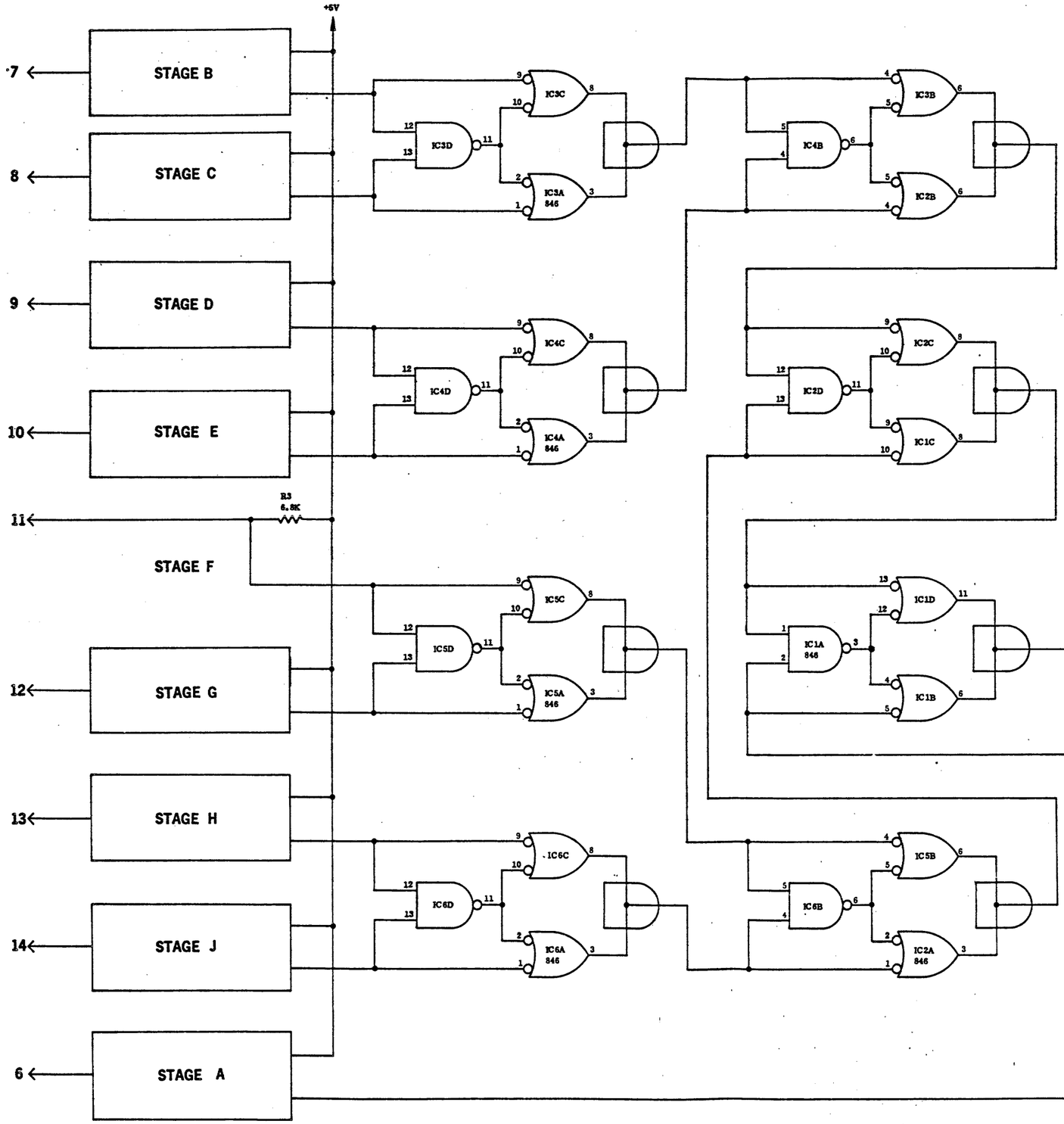
An eighth group (IC1, Pins 1-6 and 11-13) is added to provide the parity selection feature in parity generating configurations. When the output of Stage A is high, the eighth group acts as a non-inverting amplifier to the output of the seventh group. When the output of Stage A is low, the eighth group inverts the seventh group's output. Stage A is designed so that an open-circuited input will always produce odd parity.

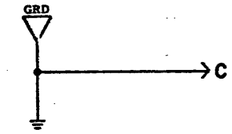
In parity checking applications, Stage A is used to input the parity channel to the card. The eighth group then compares the contents of the parity channel with the parity output of the data channels.

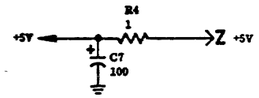
When inputs to the card have the proper voltage and impedance levels to drive the IC logic directly, the input stages are omitted (except for pull-up resistor R3), and inputs are made directly to Pins 6 through 14 of the card (6 through 12 in seven channel applications). Inputs which do not match the IC levels are buffered in the input stages. Examples of such inputs are positive levels exceeding +7V when high and/or +0.3V when low, all negative logic levels, inductive spikes from the write head in echo check configurations, and so on.

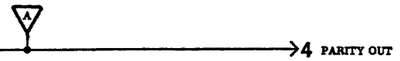
Outputs from the card will vary, depending on the card's application. The parity output is always present. IC10 and IC11 are included to generate the Write Clock for the write amplifiers when required. IC7 through IC9 are used in echo check applications to strobe the parity output. In read parity check applications, only IC7 is used. The necessary delays are generated in the deskewing logic elsewhere in the system. In both echo check and read parity check systems, an output is produced for incorrect parity if the strap corresponds to the type of parity used in the system. If the strap and the actual parity are different, an output will be produced for each correct character and no output will be produced for incorrect characters.

401-2252-011









4. NINE IDENTICAL STAGES, STAGE F SHOWN
3. ▽ DENOTES TEST POINT
2. CAPACITOR VALUES IN MICROFARADS
1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2 W

NOTES: UNLESS OTHERWISE SPECIFIED

Parity Logic, Type 2252-011, Schematic Diagram

CYCLIC REDUNDANCY CHECK CHARACTER GENERATOR
TYPES 2551-001, 2555-001, AND 3620-001

CARD PURPOSE

This package is used in 9-track, 800 characters per inch recorders to generate the IBM Cyclic Redundancy Check Character (CRCC) required in IBM System 360 installations. The CRCC is located four character spaces after the final data character in a tape record. The traditional Longitudinal Check Character (LCC) is located four character spaces after the CRCC. Both characters precede the 0.6 inch (minimum) End of Record Gap.

The CRCC is used, in conjunction with circuits in the computer tape unit, to detect almost all the errors which may occur in transmission of the character from the tape to the data output interface. These circuits assume that no errors occurred during the writing operation which produced the tape. Detected errors can be electronically corrected (the tape is not altered) if they all occur in the same track of a given record. If errors occur in more than one track per record, they cannot be corrected; but an error signal is generated.

The circuits which generate the CRCC are based on a complex equation that reduces the mathematical probability of an undetected error almost to zero. The formula itself is beyond the scope of this description and is not required for an understanding of the circuits or for trouble shooting.

Functional Description

Refer to CRC Functional Logic, Drawing No. 301-2245-001. The Cyclic Redundancy Check Register (CRCR) is basically a nine-bit shift register connected as a ring counter. Data is shifted from Bit P toward Bit 0, 0 toward 1, and so on, with Bit 7 returning toward Bit P. The subsequent state of each bit is determined by the present state of the previous bit in the register, the present state of the data input to the given bit, and (in Bits 2 through 5 only) the present state of Bit 7.

In Tracks P, 0, 1, 6, and 7 the data input to the CRCR bit is compared with the present output of the previous stage in the CRCR. The comparison takes place in the first of two Exclusive OR circuits. Functionally, the Exclusive OR produces a one (high) output if its inputs are different from each other. It produces a zero (low) output if the inputs are the same (either high or low).

The output of the first Exclusive OR gate becomes one input to the second Exclusive OR. The other input is the present state of the CRCR stage under consideration. The output of the second Exclusive OR is gated by a clock pulse to the Trigger (or toggle) input of a binary-connected flip-flop. A pulse on the Trigger input causes the flip-flop to change state.

Functionally, the second Exclusive OR makes it possible to operate a Trigger (T type) flip-flop as a Set-Reset (R-S) flip-flop. For all four combinations of inputs to the second

Exclusive OR, the output of the flip-flop after the clock pulse will be a one if the output of the first Exclusive OR is a one, and a zero if the output of the first Exclusive OR is a zero.

Tracks, 2, 3, 4, and 5 are similar to the others, except that the first Exclusive OR has three inputs. The third input samples the present state of CRCR Bit 7. The output of the Exclusive OR is high if any one input or all three inputs are high. It is zero otherwise. The second stage Exclusive OR and the flip-flop are identical to those of the other tracks.

During the tape loading operation and in each End of Record or End of File Gap, the CRCR is reset to all zeros in preparation for operating on the data in the next record. Because of this and the other properties of the CRCR, the first character of a new record will pass unchanged into the CRCR. Subsequent data inputs will not, of course, reproduce themselves in the CRCR except by chance.

The CRCC written on tape is not the same as that contained in the CRCR after the last data character is written. The latter character is first shifted by an additional clock pulse (with the data inputs held at zero). The CRCR logic is such that if Bit 7 contains a zero prior to this shift, data in the CRCR will be shifted one bit in the register (that is, the contents of Bit P become the contents of Bit 0, those of Bit 0 become those of Bit 1, etc.). If Bit 7 contains a one, then the contents of Bits 1, 2, 3, and 4 will be complemented before being shifted to Bits 2, 3, 4, and 5 respectively. The remaining five bits are shifted unchanged into the succeeding bit position.

Following the extra shift, all bits except those in Positions 2 and 4 are complemented. It is this final result which is written on the tape as the CRCC.

According to IBM specifications for nine-track equipment, bits of a character are assigned the following order on tape (starting from the outside edge, the edge to which the Load Point marker is applied): 5, 7, 3, P, 2, 1, 0, 6, 4. The CRCC as written on tape will also conform to this specification.

Circuit Description

Refer to CRCC Generator Schematic Type 2551, CRC Logic Schematic Type 2555, and CRC Control Schematic Type 3620. The logic for Track 4 will be described. Logic for other tracks is similar. The control logic is also described. Integrated circuit logic (930 series DTL) is shown functionally only.

Data for Track 4 is applied at Pin N of the Type 2555 board. During normal writing (that is, not during gaps), Pin 4 of IC5B is high and Pin 2 of IC5A is low. This allows data to enable IC5B while IC5A, which gates the output of the CRCR, is inhibited. Data is passed unchanged through IC5B and IC5C to Pin K, which feeds the write amplifier data input elsewhere in the recorder. It also feeds the data input to the CRCR logic for Track 4.

The combination of IC5D, IC6B, IC6C, and the "wired AND" form a COMPARE circuit. That is, for any two inputs A and B, the logical output $C = A\,B + \overline{A}\,\overline{B}$. In other words, C is high whenever A and B are the same, whether high or low. The COMPARE circuit forms the

complement of the Exclusive OR in which a logical output D = E $\overline{F}$ + $\overline{E}$ F. In this situation, D is high whenever E and F are different. Thus, we may obtain the Exclusive OR of two inputs by inverting the output of the COMPARE circuit. The COMPARE circuit can also be made into an Exclusive OR by complementing either input A or B. That is, if C = A B + $\overline{A}$ $\overline{B}$, then $\overline{C}$ = $\overline{A}$ B + $\overline{\overline{A}}$ $\overline{B}$ = $\overline{A}$ B + A $\overline{B}$ when A is complemented.

By cascading two COMPARE circuits, the three-way Exclusive OR described in the Functional Description is performed. The data input for Track 4 and the state of Bit 7 are compared in the first circuit, and the output of this circuit is compared with the state of Bit 3 in the second COMPARE circuit. The output of the first COMPARE circuit is the complement of an Exclusive OR, but since it is also the (inverted) input of the second COMPARE circuit, the output of the two circuits in cascade is a true three-way Exclusive OR.

The second level Exclusive OR, described functionally in earlier paragraphs, is performed in the third COMPARE circuit (IC7D, IC7A, and IC7C). So that this circuit produces the desired Exclusive OR output to the Register IC8, the complement (or 0 output) of IC8 is fed back as the second input to this COMPARE circuit.

Data is gated into Register IC8 by a clock pulse generated during the step-and-write cycle and applied (inverted) to Pin 13 of the Type 2555 board. In Models 1400/360 and 1500/360 this pulse is derived from the output of an optical shutter assembly located on the stepper motor. In Model 1600/360, $\overline{WC2}$, derived from the input Write-Step command, is used.

The output of the shutter assembly is passed unchanged (except during gaps) through IC2B and IC1A of the Type 3620 board to the Write Amplifier Clock line (WC3). Thus, data is written on tape with the stepper motor in a known position.

Writing proceeds from character to character with each new character in the register being determined by the previous contents of the register and by the data inputs. This continues until the final character of a record has been written and a gap command (either End of Record or End of File) has been issued.

At that time, the character in the CRCR is shifted and read out to be written on the tape. The complementing of all bits except 2 and 4 is accomplished by simply reading out the zero outputs of the CRCR except for Bits 2 and 4. After readout, the CRCR must be cleared in preparation for the next data block. The remainder of the logic in the CRCC generator package is concerned with these operations.

This logic consists of a two-stage binary counter (IC19 and IC20), a decoder (IC18) which decodes counts of 0, 1, and 3, and various gating circuits. IC19 and IC20 are connected so that, once they have counted to 0, they will remain at 0 unless IC3 (on the Type 3620 board) is set. IC3 is set at the beginning of a gap and when a File Mark is written during an End of File Gap.

All timing in the gap logic is controlled by Gap Clock pulses obtained by amplifying the output of the optical shutter assembly (located on the stepper motor) during gaps. During normal writing these outputs are inhibited from this circuit by the $\overline{\text{Gap in Process}}$ level.

At the beginning of a gap, Pin L ($\overline{\text{Gap in Process}}$) of all boards goes to zero, enabling the Gap Clock circuit (described more fully below), and inhibiting the data input lines and WC3 to the write amplifiers. The zero level on Pin L also sets IC3 (on the Type 3620 board) through C2.

Setting IC3 primes the counter IC19 and IC20 (on the Type 2555 board) so that it will count when Gap Clock pulses are generated. IC3 is reset by the first Gap Clock pulse, so that IC19 and IC20 will only count to four once at the beginning of the gap.

As the count progresses, the stages of IC18 (on the Type 2555 board) decode various counts to perform specific functions. IC18A decodes t_1, which is used to perform the extra shift required of the CRCR at the end of a record. (Since the count started at 0, t_1 actually occurs on the second Gap Clock pulse.) All data inputs are inhibited by the zero level on Pin L; therefore, the outputs to the write amplifiers are at zero. These outputs are also the inputs to the CRCR logic; hence, the shift at t_1 is performed with zero on the data inputs as required.

IC18B decodes t_3 (which actually occurs on the fourth Gap Clock pulse). This pulse is gated in IC4B and IC1A of the Type 3620 board to create a clock pulse to the write amplifiers and enable all the gates controlling the readout of the CRCR (t_3 GATED). Thus at t_3, the write amplifiers see the appropriate data on their input lines and a clock pulse on the clock line. Therefore, they treat the CRCC as an ordinary data input. Thus, the CRCC is written four steps after the final data character, as required.

After the CRCC has been written, the CRCR must be reset. IC18C accomplishes this by decoding the zero, or reset, state of IC19 and IC20. This level is gated by the Gap Clock in IC1B of the Type 3620 board and applied to the Direct Clear inputs of the CRCR as $\overline{t_0}$. Subsequent Gap Clock pulses will continue to "reset" the register, but these pulses cease before any new data is entered, so no harm is done.

The $\overline{t_0}$ pulse also sets flip-flop IC4C-IC4D. This flip-flop, once set, prevents t_3 pulses from passing through IC4B to the CRCC readout gates and the write amplifier clock line. Thus, no CRCC will be written while this flip-flop is set. Since t_0 follows t_3, the desired CRCC will be written, but no others.

IC4C-IC4D is reset by the first Shutter Clock pulse to be generated after a gap. This pulse results only from external application of a Write-Step input, signifying that data is to be recorded. If another End of Record or End of File Gap input is applied instead, IC4C-IC4D remains set and inhibits the t_3 pulse generated at the beginning of the second (or subsequent) gaps.

The t_3 pulse must be inhibited because the CRCC for no input data is not a zero character. (It is ones in all tracks except 2 and 4.) The computer would interpret this lone character (and its LCC) as noise in the gap, causing (in some cases) an undesirable program termination. Since t_3 is inhibited, no LCC is generated because no write amplifiers have been set by a CRCC.

IC19 and IC20 start from 0 at the beginning of a gap. To keep this condition from being interpreted as a signal to reset the CRCR (quite prematurely), the condition of primer flip-flop IC3 is included in the decoding of the reset pulse. If IC3 is set, as at the beginning of a gap, IC18C is inhibited and no reset pulse is generated.

The output of IC17A is zero during the first four Gap Clock pulses. As such, it may be used to inhibit the "4-shot" circuits (located on another card) which write the LCC. The LCC, normally separated by four character spaces from the data on seven-channel recorders, must be moved out to the eighth character space to allow the CRCC to be written in the fourth space. The output of IC17A thus allows the LCC logic to ignore the first four Gap Clock pulses, and so proper spacing of the LCC is assured.

During an End of File Gap, a second count-of-eight sequence is produced in addition to the one at the beginning of the gap. This occurs when the File Mark is written.

The $\overline{\text{File Mark}}$ signal on pin H (from the timing circuits) may occur at any time during the step cycle, and so it is buffered in flip-flop IC6C-IC6D. The next Gap Clock pulse sets IC3 through IC5D and IC2D. Setting IC3 primes IC19 and IC20 (the binary counter). When IC3 is set, the t_0 level is removed which inhibits further inputs to IC5D.

IC6C-IC6D is reset by the resulting t_3 pulse (before the inhibiting gate), which removes that input to IC5D before the t_0 level reappears. Thus, IC3 is set only once at this time.

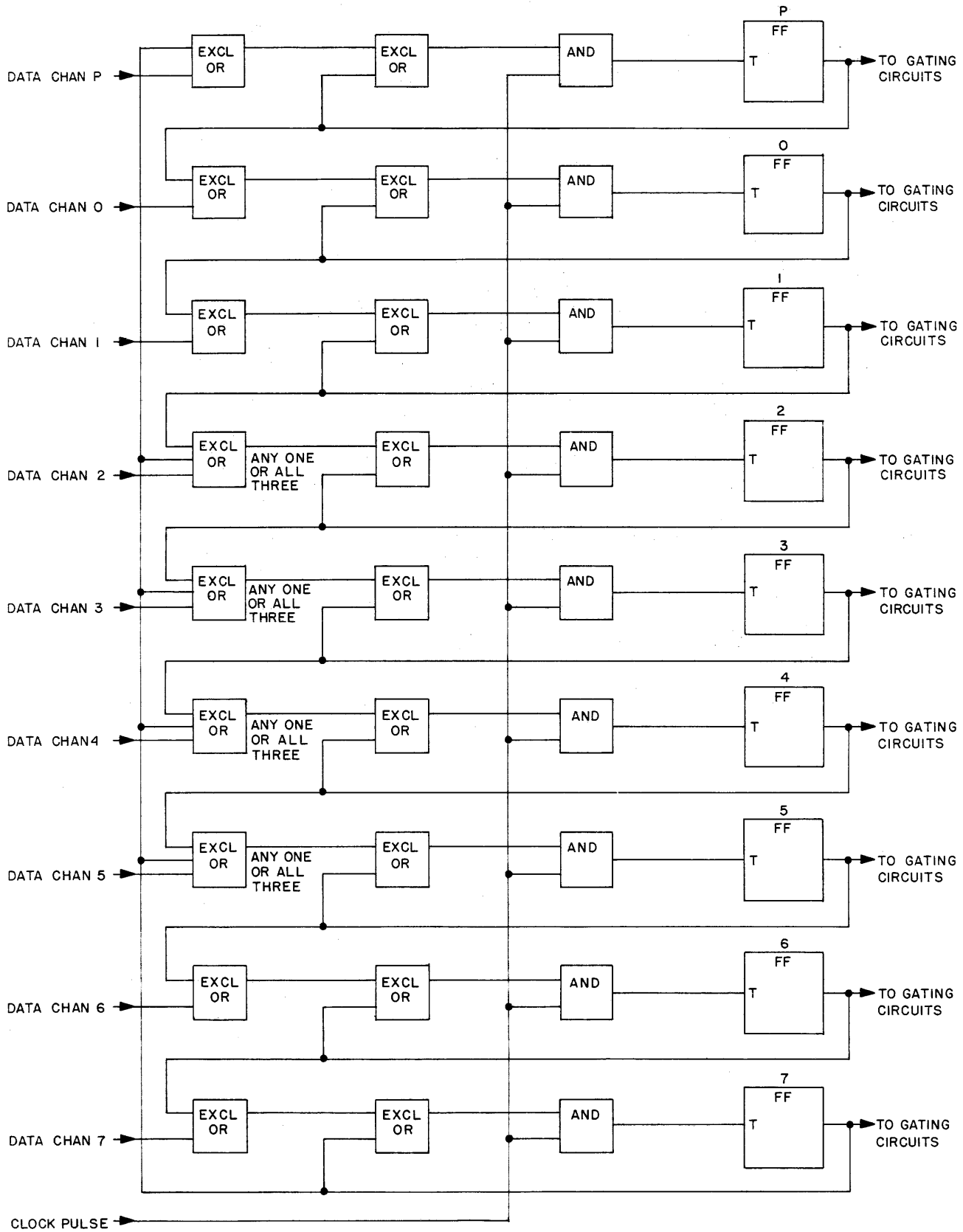
IC4C-IC4D is also set during this time, having been set by the first $\overline{t_0}$ pulse of the End of File Gap. Thus, the CRCC due to the File Mark is inhibited, as described above. Since the count-of-eight sequence is otherwise normal, the File Mark Check Character will be written eight character spaces after the File Mark, as required.

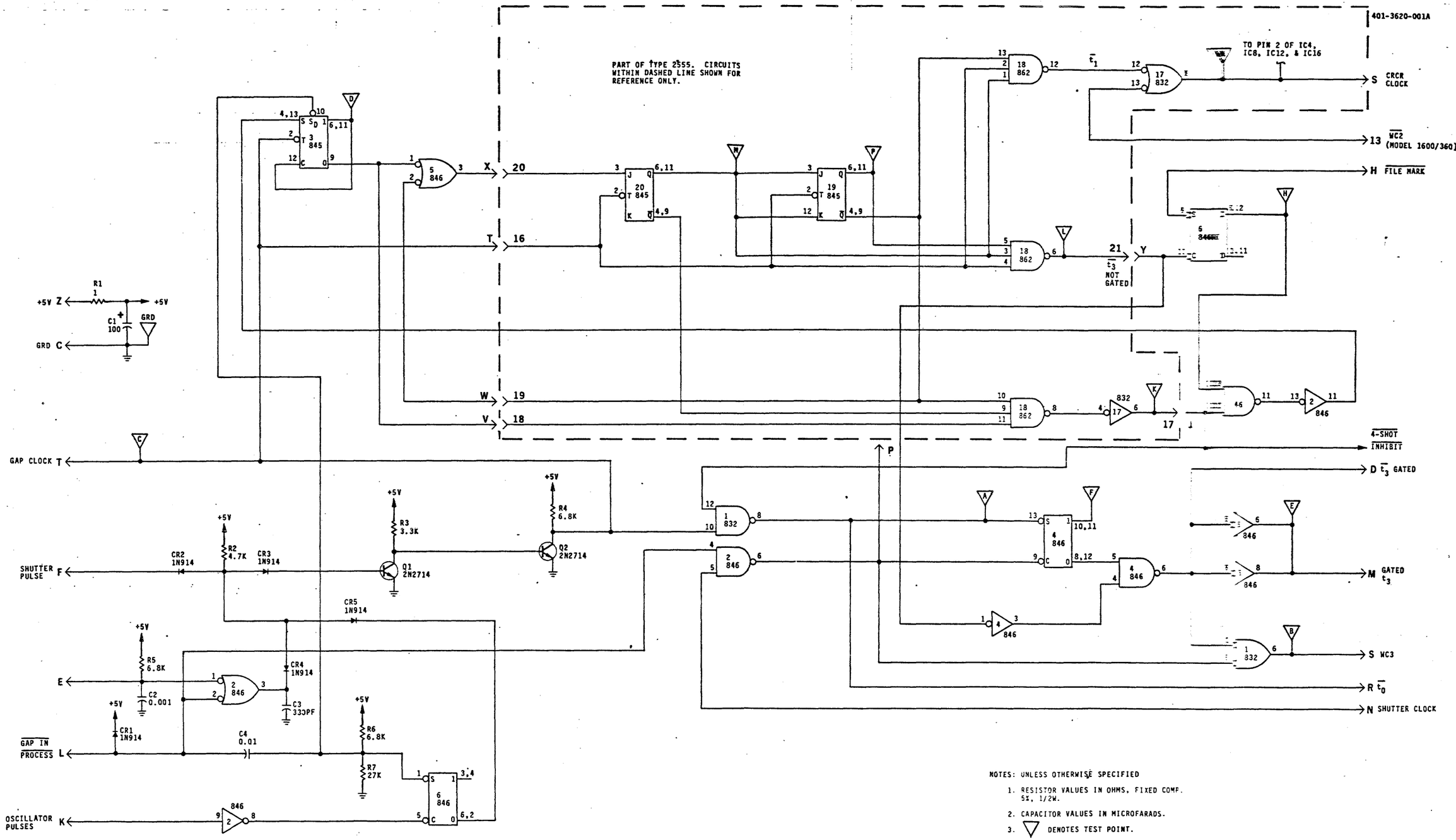
The shutter output which comes in at pin F (3620) is gated by $\overline{\text{GAP IN PROCESS}}$. When a gap is entered the shutter output is still gated out until the first oscillator pulse is detected. At this time a flip-flop is cleared and the shutter pulse circuitry is enabled. During normal writing the shutter output is disabled by $\overline{\text{GAP IN PROCESS}}$.

The combination of R14 and C6 on the Type 3620 board forms a 100 microsecond time constant filter to eliminate high frequency noise on the +5V supply line. R1 and C1 on the Type 2551 and Type 2555 boards perform a similar function.

TITLE CRC FUNCTIONAL LOGIC

DWG NO. 301-2245-001 REV

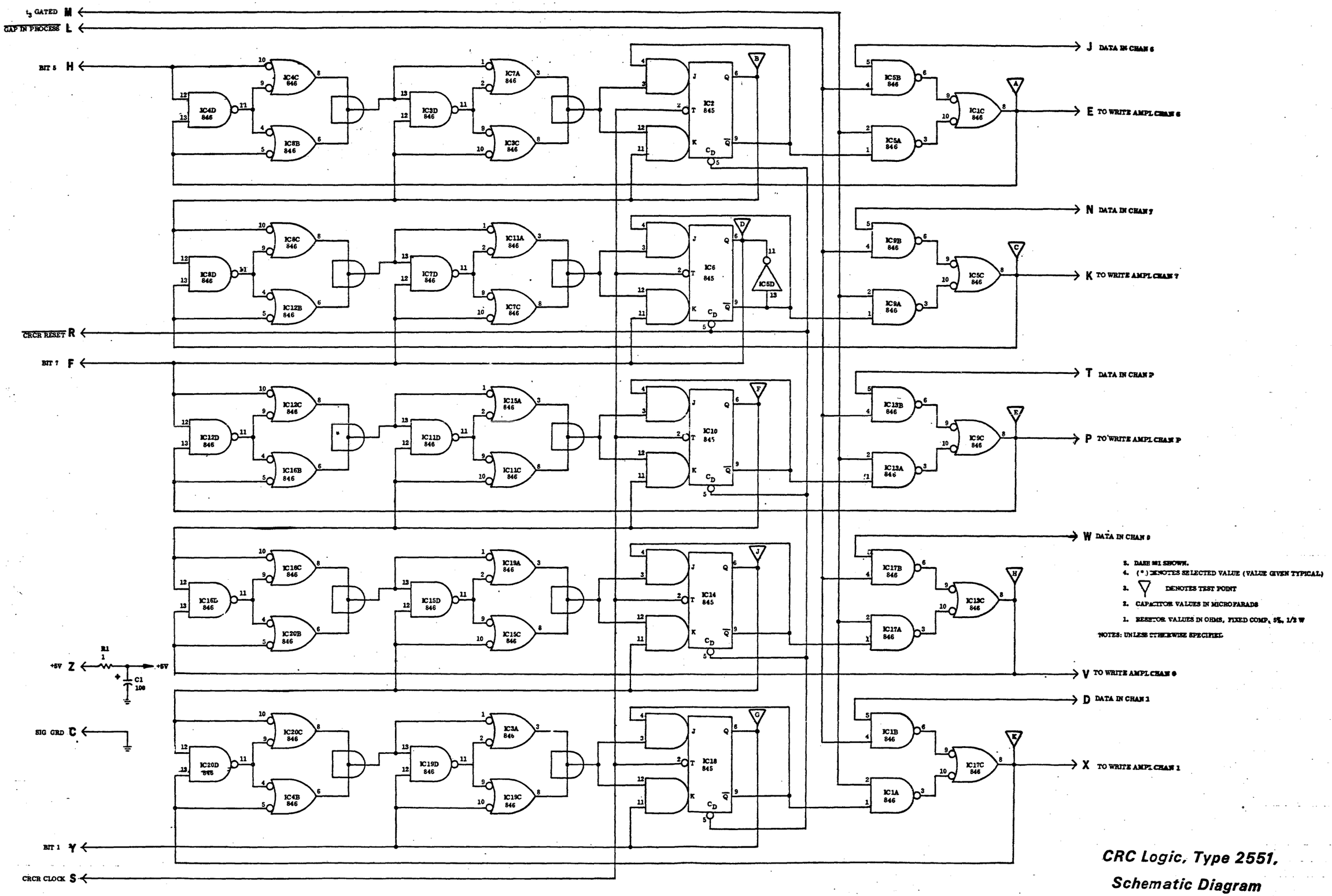




NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP. 5%, 1/2W.
2. CAPACITOR VALUES IN MICROFARADS.
3. ▽ DENOTES TEST POINT.
4. UNUSED IC INPUTS MAY BE TIED TOGETHER OR TO +5V.

CRC Control Type 3620-001A, Schematic Diagram



CRC Logic, Type 2551, Schematic Diagram

401-2555-001-E

H BIT 5

L $\overline{\text{GAP IN PROCESS}}$

J DATA IN CHAN 5

E TO WRITE AMPL CHAN 5

N DATA IN CHAN 4

K TO WRITE AMPL CHAN 4

F BIT 7

T DATA IN CHAN 3

P TO WRITE AMPL CHAN 3

R $\overline{\text{CRCR RESET}}$

Y BIT 1

S CRCR CLOCK

D DATA IN CHAN 2

V TO WRITE AMPL CHAN 2

17 t_0

Z +5V

C

13 $\overline{WC2}$

M, 11 t_3 GATED

21 $\overline{t_2}$

18

COUNTER 19

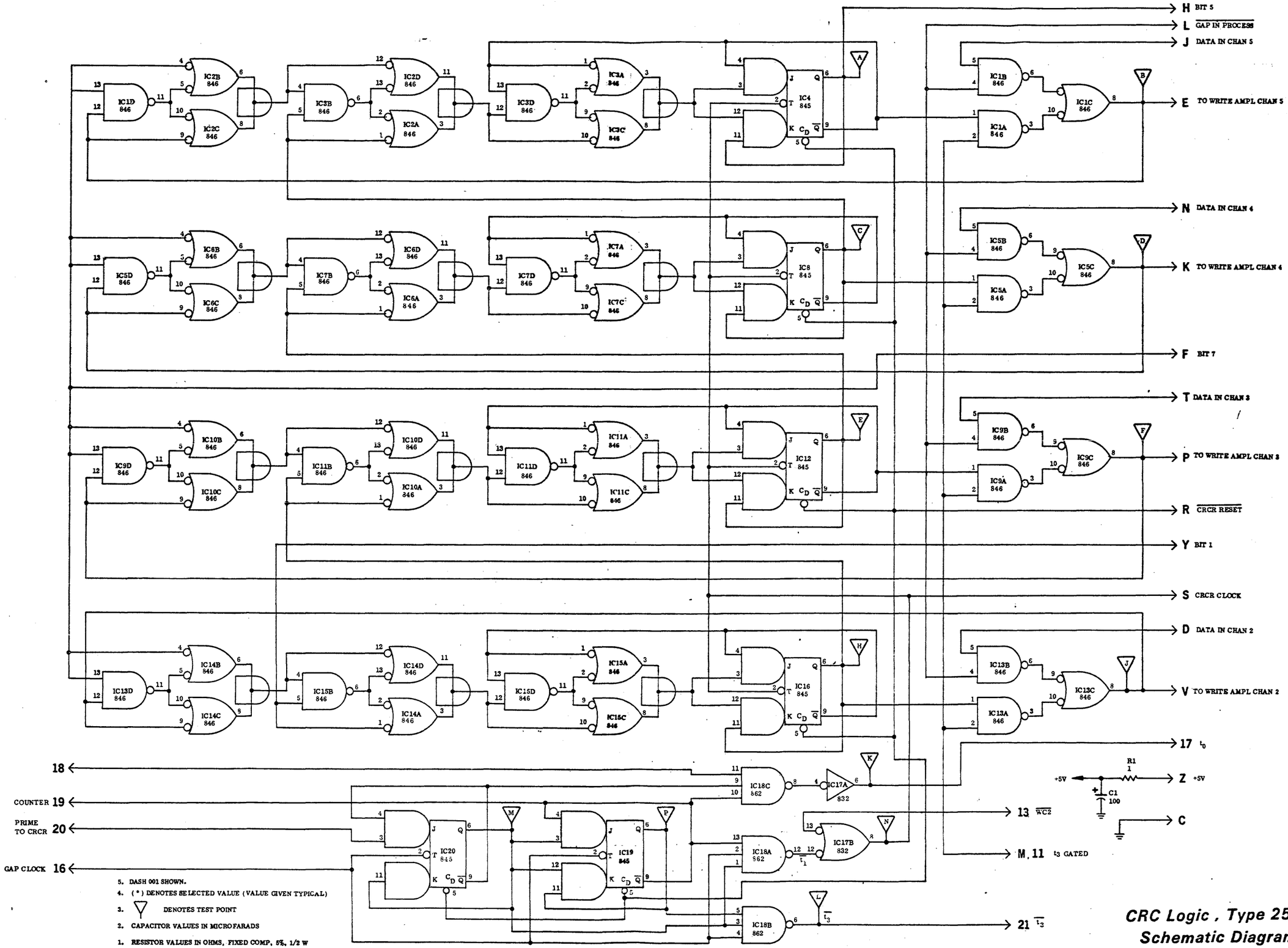
PRIME TO CRCR 20

GAP CLOCK 16

5. DASH 001 SHOWN.
4. (*) DENOTES SELECTED VALUE (VALUE GIVEN TYPICAL)
3. ▽ DENOTES TEST POINT
2. CAPACITOR VALUES IN MICROFARADS
1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2 W

CRC Logic , Type 2555, Schematic Diagram

401-2555-001-E



5. DASH 001 SHOWN.
4. (*) DENOTES SELECTED VALUE (VALUE GIVEN TYPICAL)
3. ▽ DENOTES TEST POINT
2. CAPACITOR VALUES IN MICROFARADS
1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2 W

NOTES: UNLESS OTHERWISE SPECIFIED

CRC Logic , Type 2555, Schematic Diagram

SECTION IX

SPARE PARTS

SECTION IX

SPARE PARTS

RECOMMENDED SPARE PARTS KITS

In applications where the recorder is to be operated in locations remote from the factory, the Kennedy Company recommends Spare Parts Kits.

ORDERING SPARE PARTS AND/OR KITS

When ordering parts and/or kits, it is important to include model number, serial number, density, logic, and special modifications.

MODIFICATIONS

When ordering parts, it is important to include the modification number(s) along with the model number.

If the recorder is equipped with modifications, the necessary information can be obtained in the Modifications Section of the manual.

EXCHANGE OF CAPSTAN ASSEMBLY

If capstan assembly becomes inoperative, it can be rebuilt or exchanged for a rebuilt capstan assembly (the cost is approximately one-half that of a new capstan).

K-21 MAINTENANCE KIT

To assist in the routine maintenance of Kennedy Magnetic Tape Recorders, it is recommended that Maintenance Kit K-21 be used. The kit contains all the necessary items required to clean and adjust all tape recorders during scheduled routine maintenance. Each kit contains: one can head cleaner, tape guide line block, cleaning cloths, reflective strips, special tools, tape developer, and a small tube of Loctite(tm).

SPARE PARTS LIST

A Spare Parts List with minimum and long term kits is shown on the following page.

PART NUMBER	DESCRIPTION
	MINIMUM KIT
151-0132-001	FUSE, 2 amp, slo-blo
139-0214-001	LAMP, no. 330
190-2607-002	ASSEMBLY, tension roller
190-2528-103*	ASSEMBLY, printed circuit board, stepper power ampl.
190-2677-112*	ASSEMBLY, printed circuit board, stepper logic
190-2655-103*	ASSEMBLY, printed circuit board, gap timing
190-2654-101*	ASSEMBLY, printed circuit board, control
190-3392-001	ASSEMBLY, power supply regulator
190-2273-001	ASSEMBLY, control board, deck power
190-2224-002	ASSEMBLY, card extender
190-2436-005	ASSEMBLY, printed circuit board, write amplifier
190-3454-001	ASSEMBLY, printed circuit board, write control
190-2252-011	ASSEMBLY, printed circuit board, parity generator
190-2551-001	ASSEMBLY, printed circuit board, CRCC generator
190-2555-001	ASSEMBLY, printed circuit board, CRCC logic
190-2236-001/3620-001	ASSEMBLY, printed circuit board, CRCC control
190-2224-001	ASSEMBLY, card extender
190-2324-001	K-21 Maintenance Kit
	*Suffix P/N with dash number reflected on card I.D. chart
	LONG TERM KIT (the above plus the following)
191-0574-001	RING hub drive
151-0037-001	SWITCH
190-1995-000	ASSEMBLY, pressure roller actuator
190-2183-003	ASSEMBLY, magnetic head
190-1139-001	ASSEMBLY, sensor broken tape
190-1138-001	ASSEMBLY, sensor LP-EOT
125-0036-001	SPRING
191-0635-002	POTENTIOMETER
190-1509-001	ASSEMBLY, guide
115-3625-798	CAPACITOR
115-7049-405	CAPACITOR
145-0005-001	RELAY
135-0001-001	MOTOR
125-0004-002	BELT
190-2204-003	**ASSEMBLY, capstan drive & shutter
156-2292-001 or 156-3385-001	TRANSFORMER (determine type used or give machine serial number when ordering spare parts)
	** Capstans are available on exchange basis.

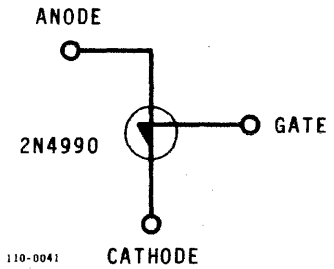
3-69-02

CIRCUIT EXPLANATIONS

Utilized in certain areas throughout the machine are circuits with which the user may be unfamiliar. Characteristics of these are given below.

Silicon Unilateral Switch 2N4990

The SUS is similar to a four-layer diode but with a gate terminal brought out.

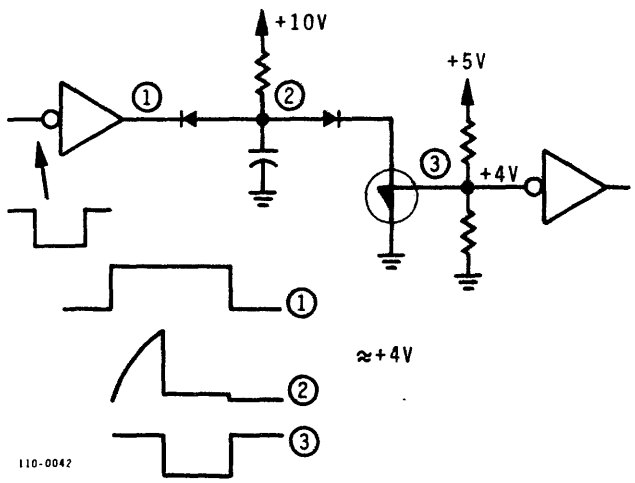


The SUS conducts at an anode voltage of about 7 volts if the gate terminal is open. Once fired the device continues to conduct until current drops below a threshold value.

During conduction the anode drops to about 1.0 volt but the gate goes nearly to ground.

Firing voltage may be set at any desired point less than 7 volts by setting the gate at a lower voltage. The device then fires at the gate voltage value.

Typical Circuit



Logic Convention

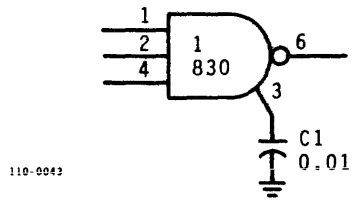
All circuits internal to the machine are shown with positive true logic.

Unused Inputs

Unused inputs may be connected to used inputs or to +5 volts. These connections are not necessarily indicated on the schematics.

Extender Connections

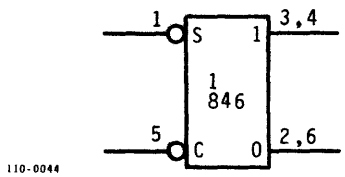
The extender connection is used in some gates to provide time delays. This is shown as:



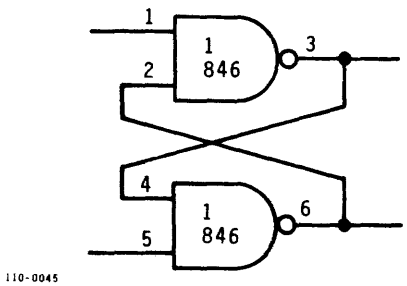
The output is delayed in going to ground by an amount proportional to capacitor size. Positive going output is not appreciably affected.

R-S Flip-Flop

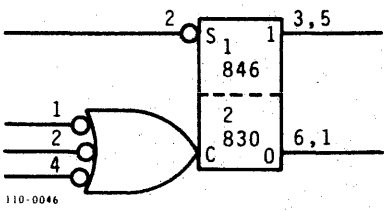
In logic circuits two gates are often connected as flip-flops and shown as below.



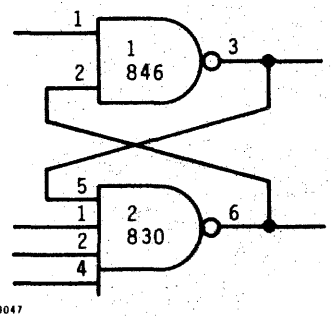
Drawn as gates this would be



If multiple input gates are connected in this fashion they are shown as:

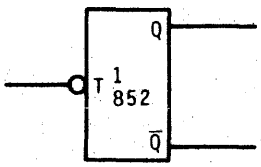


As gates this would be

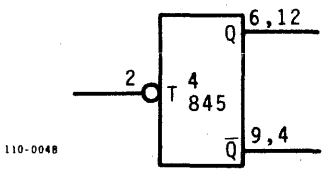


J-K Flip-Flops

Cross connections internal to J-K flip-flops are not shown.

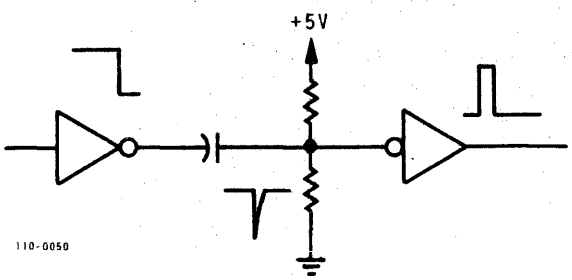


When R-S flip-flops are J-K connected the cross connection is indicated but not drawn:

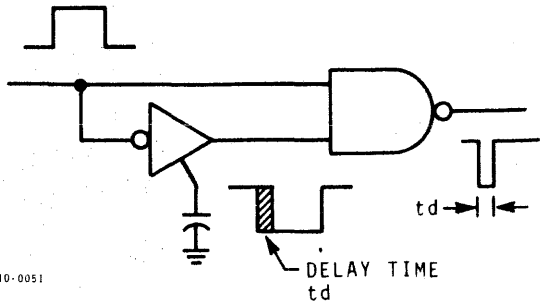


Edge Circuits

To take an edge to produce a pulse either of two circuits may be used:



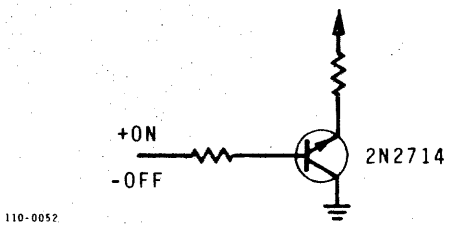
Conventional differentiator:



Delay Edge Circuit

Inverted Transistor

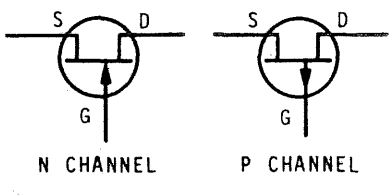
Inverted transistors are used as analog switches in servo amplifiers and read amplifiers.



In this connection the transistor gain is less than unity — base drive must be greater than current switched. The advantage is that (nominally) emitter and collector assume identical voltages. In other words, there is zero collector-emitter drop.

FET Switches

For analog switching FET switches are used in some circuits.



The N channel FET is conducting when 0 volts is applied to the gate and cuts off with negative gate signal (like a vacuum tube). No gate current flows.

P channel FETs are the inverse of the N channel. They cut off with positive gate voltage.

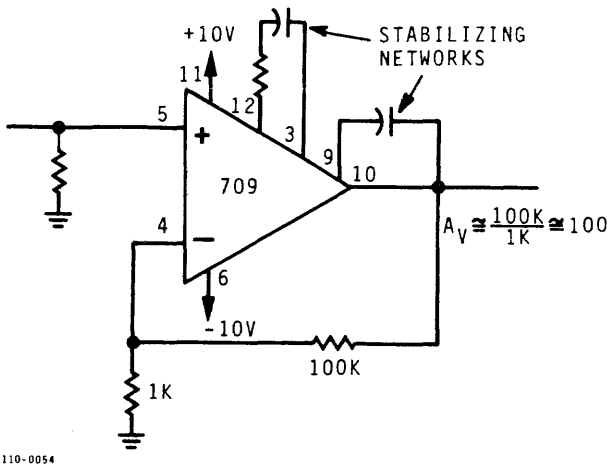
Operational Amplifiers

Analog circuits make considerable use of operational amplifiers. Type 709 is standard.

An operational amplifier is a high gain dc coupled amplifier having a pair of inputs — inverting (-) and non-inverting (+). Gain and dc offset are controlled by feedback — in most circuits negative. With positive feedback the amplifier becomes a switch with a controllable threshold and various characteristics determined by the feedback network.

With negative feedback a linear amplifier results again with gain and response characteristics dictated by the feedback network.

Typical circuit:



Notes

Warranty

Kennedy Company products are warranted to be free from defects in materials and workmanship for a period of one year.

Kennedy Company reserves the right to inspect any defective parts or material to determine damage and cause of failure.

This warranty does not apply to any Kennedy equipment that has been subject to neglect, misuse, improper installation and maintenance, or accident.

Liability under warranty is limited to no charge repair of defective units when equipment is shipped prepaid to factory or authorized service center after authorization from Kennedy Company to make such return.

Kennedy Company is continually striving to provide improved performance, value and reliability in their products, and reserves the right to make these improvements without being obligated to retrofit delivered equipment.

KENNEDY CO.

KENNEDY CO.

540 WEST WOODBURY ROAD, ALTADENA, CALIFORNIA