CONTENTS

INTRODUCTION	Wait (WAIT)	40
APPLICATIONS 1		40
Process Control 1		41
High Speed Data Acquisition 2		42
Data Collection and Plant Communications 3		44
Other Acquisition and Control		
SYSTEM DESCRIPTION	INTERVAL TIMERS	47
Processor-Controller (P-C)	INTERIOR INTERIOR IN THE INTERIOR I	
Process Input/Output Features	STORAGE PROTECTION	48
Data Processing I/O Units4	brounds inorderion p.,	10
Communications Devices	PARITY	49
Communications Services	PARITY	40
System Data Flow 4	OPERATIONS MONITOR	50
1800 SYSTEM UNITS AND FEATURES		50
PROCESSOR-CONTROLLERS	POWER FAILURE PROTECT	3(
Data Representation	PROGREGOR GOVERNOLLER GOVERNE	E 1
Core Storage	PROCESSOR-CONTROLLER CONSOLE	51
Arithmetic	Push-Button Switches and Lights	51
Indirect Addressing		53
Index Registers	Toggle Switches	55
Data Channels	Console Indicators	56
Interrupt	Data Flow Displays	57
Instruction Formats	Display Procedures	58
	Program Failure — Restart	58
P-C Registers		
P-C Data Flow	I/O CONTROL	60
Data Flow Examples	On-Line Maintenance Considerations	60
INSTRUCTION SET	Direct Program Control Operation	63
LOAD AND STORE INSTRUCTIONS 17	Data Channel (DC)	64
Load Accumulator (LD) 17	Data Channel Operation	66
Double Load (LDD)	•	
Store Accumulator (STO)		
Double Store (STD)	INTERRUPT	70
Load Index (LDX) 20	Interrupt Levels	70
Store Index (STX)	Status Words	72
Store Status (STS)	Programmed Operation	74
() () () () () () () () () ()		
Load Status (LDS)	DATA PROCESSING INPUT/OUTPUT AND	
	COMMUNICATIONS DEVICES	78
1144 (12)	Input/Output Devices and Control Units	78
	Input/Output Interface	78
Subtract (S)		78
Double Subtract (SD)	I/O Control	79
Multiply (M)	Input/Output Instruction (XIO)	81
Divide (D)	Input/Output Termination	
Logical And (AND)	Input/Output Interrupts	81
Logical Or (OR)	Device Status Word (DSW)	81
Logical Exclusive Or (EOR) 30		
SHIFT INSTRUCTIONS	IBM 1816 PRINTER-KEYBOARD AND	
Shift Left Logical A (SLA)	IBM 1053 PRINTER	82
Shift Left Logical A & Q (SLT)	Printer Functional Description	82
Shift Left and Count A (SLCA)	Printer Programming	84
Shift Left and Count A & Q (SLC) 33	Keyboard Functional Description	86
Shift Right Logical A (SRA)		8'
Shift Right A & Q (SRT)	Programming	0
Rotate Right A & Q (RTE)		
BRANCH INSTRUCTIONS	IBM 1442 CARD READ PUNCH	90
Branch or Skip on Condition (BSC or BOSC) 36	Functional Description	90
Branch and Store Instruction Register (BSI) 37	Programming	92
Modify Index and Skip (MDX)	Read and Punch Operations	9

IBM 1443 PRINTER	98	COMMUNICATIONS ADAPTER 161
Functional Description	98	General Description
Programming	101	Communication Facilities
		CA Code
IBM 1054 PAPER TAPE READER AND IBM 1055		Functional Description 166
PAPER TAPE PUNCH	104	Timeout Controls
Functional Description		CA Programming
Description of Operation		Implementation of BSC
Programming		Examples of Transmit and Receive Sequences 177
IBM 1627 PLOTTER	108 S	SELECTOR CHANNEL 180
Operation		Introduction
1627 Operating Controls	109	Programming
Programming		Channel Command Word
		Channel Status Word
IBM 2401 AND 2402 MAGNETIC TAPE UNITS	112	Initiation of Selector Channel Operations 191
Functional Description		Termination of Selector Channel Operations 192
Programming		SYSTEM/360 ADAPTER
		Commands
IBM 1810 DISK STORAGE		Device Status
Functional Description		PROGRAMMED OPERATION
Programming	122	
ANALOG INPUT	196	Control (System/360)
Analog Input Units and Features		
1851 Multiplexer Terminal	120	Read or Read Backward (System/360)
Multiplexer/R	120	Write (System/360)
Multiplexer/S (HLSE)	129	Test I/O (System/360)
Signal Conditioning Elements	129 190	No-Operation (System/360)
Differential Amplifier	190	Halt I/O (System/360)
Analog-Digital Converter (ADC)	101	Sense (1800)
Comparator	131 190	Initialize Read (1800)
Analog Input Expander	100	Initialize Write (1800)
Programmed Operation	133 199	Control (1800)
I/O CONTROL COMMANDS — ANALOG INPUT	$\frac{133}{196}$ 2	790 ADAPTER
Direct Program Control	190	FUNCTIONAL AREAS 202.2
Data Channel	130	Loop Output
ANALOG INPUT EXECUTION TIMES	136	Loop Input
		Frame Processing
Direct Program Control Operations Data Channel Operations	139	Cycle Steal Controls
Thermosouple Operation	139	1800 I/O Channel Interface 202.4
Thermocouple Operation		Repeater Interfaces and Bypass Controls 202.4
DIGITAL INPUT	146	2790 Adapter Diagnostic Controls 202.4
DIGITAL INPUT UNITS AND FEATURES	148	OPERATION
Digital Input Data Channel Adapter	148	Loop Channels
Digital Input		Data Transmission Arrangement 202.6
Pulse Counter		Commands and Responses
Th	149	PROGRAM CONTROL 202.11
Digital Input Addressing		Loop Channel Control Block (LCCB) 202.12
Programmed Operation		Loop Channel Interrupt Block (LCIB) 202.16
7/0 00370000 000000000000000000000000000	151	Input/Output Control Commands
was a second of the second of	151	Sense Diagnostic DSW Usage
Data Channel		Channel Sequence Handling
		- · · · · · · · · · · · · · · · · · · ·
DIGITAL AND ANALOG OUTPUT	154	—
	L56	
	l56 A	DDRESS ASSIGNMENT 203
Digital-To-Analog Conversion	156	Fixed Assignment 203
	157	Additional Assignments 205
I/O CONTROL COMMANDS — DIGITAL AND		
	¹⁵⁷ A	PPENDIX A. 1800 INSTRUCTION SET 211
	157 A	PPENDIX B. INSTRUCTION EXECUTION TIMES 214
Data Channel		PPENDIX C. I/O DEVICE ADDRESSING
	= 0	PPENDIX D. DEVICE STATUS WORDS 224
Data Table Layouts		NDEX

The ever increasing pace of technology, industry, and business continues to demand more and more reliable, up to date information. History is a good teacher, true, but its compression within the past few decades of progress has taught us that today's problems require real-time answers, not a history of past performances. Data of almost every conceivable nature—available from a myriad of sources—must be collected, analyzed, and translated into terms that can be used to optimize today's performance.

IBM's answer to the demand for real-time data acquisition, analysis, and control is the IBM 1800 Data Acquisition and Control System. The 1800 System is designed to handle a wide variety of real-time applications, process control, and high-speed data acquisition. Each system is individually tailored with modular building blocks that are easily integrated to meet specific system requirements.

The 1800 System provides a large variety of features and devices as follows:

- A family of real-time process input/output (I/O) devices such as analog input, analog output, digital input, and digital output.
- A variety of data processing I/O devices such as magnetic tape, disk storage, line printer, graph plotter, card I/O and paper tape I/O.
- Several other features and adapters which include System/360 Adapter, Communications Adapters, Selector Channel, and 2790 Adapters.

Real-time process I/O devices enable the 1800 System to accept either analog or digital input signals and provide analog or digital output signals for control or display purposes.

Data processing I/O devices enable the 1800 System to perform the necessary data processing for data analysis, editing, and control purposes. These devices are also used to provide instructions for process and control room operators as well as reports for management review.

The System/360 Adapter provides a control and data path for direct attachment of an IBM System/360 in applications where more powerful supervision is required. For example, the System/360 may be used to integrate the commercial aspects of an application with the controlling operations exercised by the 1800 System.

A Communications Adapter (maximum of four) provides one or two communication paths (Line Adapters) for connection, over voice grade lines, to remote System/360's, IBM 1130 Systems, IBM 2780 Data Transmission Terminals, or other 1800's. This allows the 1800 System to be integrated into large scale control systems without consideration of the physical location of control systems above or below the 1800 in the control hierarchy.

The Selector Channel provides the facilities for attaching an IBM 2841 Storage Control with up to eight 2311 Disk Storage Drives. Through the use of shared files on the 2311's, the 1800 can exchange data with System/360 or another 1800.

The 2790 Adapter (maximum of 2) provides the interface facilities for attaching an IBM 2790 Data Communication System to the 1800 Processor-Controller. This 1800/2790 combination provides real-time data collection or plant communication capabilities with the 1800 being the system controller for the 2790 System.

APPLICATIONS

The 1800 is capable of accepting electrical signals, both analog and digital, from such devices as thermocouples, pressure and temperature transducers, flow meters, analytical instruments, and contacts. It provides electrical on/off and analog control signals for the customer's controlling devices. With these capabilities and remote communication facilities, the 1800 System can be integrated into large multiprocessor systems with varied real-time applications. Typical applications exist in the area of process control, high speed data acquisition, and data collection or plant communications.

PROCESS CONTROL

Industrial processing applications are wide and varied, as are the degrees of control that individual processes may require. Some general process control application areas are:

Primary Metals Production Primary Metals Finishing Power Generation Power Dispatching Pipeline Transmission Paper Production Glass Production Cement Production Environmental Control Pilot Plants Chemical Processes Petroleum Refining

The IBM 1800 Data Acquisition and Control System provides maximum flexibility in the types of process data that it can accept and the variety of output signals and data format that it can produce. Some of the degrees of control that an 1800 may exercise follow in order of increasing complexity:

Data Gathering: Process data is gathered by the 1800 System, converted into digital information, and printed to provide: (a) operating records for accounting and supervisory purposes; or (b) a record of experimental data in process research.

Data Collection and Analysis: Process data is collected by the 1800 Processor-Controller (P-C) for mathematical analysis. Current performance figures are compared with those obtained in the past, and the results are printed for process operator and management evaluation.

Data Evaluation and Operator Guidance: Process data is collected, analyzed, and evaluated with respect to previously stored guidance charts. Control instructions are then typed out for the process and control room operator, and messages and log sheets are provided for management review.

Process Study: The P-C rapidly collects the process data that is necessary for the development of a model of the process. The model is developed by using a combination of empirical techniques and observing past methods of running the process. When a more complete and more precise description of the process is required, a model is constructed by using such mathematical techniques as correlation analysis and regression analysis. The process control program is then tested on the mathematical model prior to its use on the process. Extensive operator guide information is obtained. In addition, the model represents considerable progress toward complete supervisory control.

Process Optimization: An extensive P-C program, based on the model of the process, directs the 1800 System. Process data is continuously collected and analyzed for computation of optimum operating instructions. These instructions are given to the process operator via an on-line printer.

Supervisory Control: The P-C communicates messages and commands to the operator and, if desired,

directly to the process equipment and instrumentation. The sensors that measure process conditions are continuously monitored by the P-C. The P-C program analyzes this information and then generates the required output information.

Messages from the P-C to the operator may be displayed by several methods in the operator's working area. These messages guide the operator in adjusting the status of instruments located at the point of control. Data messages based upon visual observation of the process and its instrumentation are sent back to the P-C or the process operator. These messages are evaluated by the P-C to provide additional output, if required, for continued process operator guidance. Communication between the control room operator and the process is maintained through the P-C.

When the P-C supervisory program computes new set point values, it may—at the discretion of the operator—automatically adjust the set points of the controlling instrumentation to the new values.

HIGH SPEED DATA ACQUISITION

A High Speed Data Acquisition (HSDA) System may be thought of as a monitoring and controlling facility that is used to acquire, evaluate, and record data developed during the testing of a system (or assembly, subassembly, or component). The system here refers to anything from an anesthetized rodent in the research laboratory to a Saturn V booster on its test stand.

Many types of HSDA Systems are used. Some merely stream data directly from instrumentation to magnetic tape with a minimum of "quick look" information and data editing or checking. However, as experimental work on large systems has become more complex and time consuming, a trend has been observed toward HSDA Systems with more sophisticated data reduction and real-time display requirements. HSDA Systems most readily meet these requirements when the system design is based on a digital computer.

Many aerospace applications, for example, now require control signals to modify the test as a result of out-of-limit conditions or evaluation of sample test data. Thus we find a direct parallel with the historical development of process control systems. They began with data gatherings; progressed to operator guide control; and where the applications required it, automatically applied system output commands directly to the process equipment.

The following are typical HSDA application areas for the 1800 System:

Missile Check Out
Wind Tunnels
Static Test Stands
Missile Telemetry
Nuclear Reactor Research
Particle Physics Control and Acquisition
Environmental Chambers
Flight Simulators
Hybrid Systems
Medical Research
Medical Analysis—Clinical

DATA COLLECTION AND PLANT COMMUNICATIONS

The 1800/2790 Data Communications System combines, within a single powerful system, the sensor based capabilities of the 1800 System and the manmachine interface of the 2790 System. This system features a high speed two-way data communications network specifically designed to accommodate a large volume of short messages from many in-house locations to a central processing area.

Data communications systems have applications in many types of installations. Among these are installations involved in manufacturing or assembly line processes. In this type of installation, each step in the manufacturing or assembly process is usually dependent on completion of a previous step. These installations are usually susceptible to work stoppages due to failure of one or more steps in the assembly process. Through remote data entry units or area stations located throughout the installation, data concerning the progress of each phase or station along the line can be entered by the workers. Since data entry is in real-time, the over-all status of the complete installation is always available from the 1800 System. This real-time reporting capability can be used to ensure smooth and continuous operation of the entire installation.

OTHER ACQUISITION AND CONTROL

The 1800 System has been designed to handle widely divergent applications which involve real-time processing abilities. Inputs may include signals from only digital sources or from both digital and analog sources. If desired, the results of analyzing the required data may be displayed in analog or digital form, or used to cause direct functions.

These applications cover a wide range, including the following areas:

General Research Traffic Control (vehicle, railways, etc.) Engine Testing Component Testing
Quality Control
Information Display
Material Dispatching
Marine Operating Systems

SYSTEM DESCRIPTION

Components of the IBM 1800 Data Acquisition and Control System can be used in three basic configurations:

- 1. The 1800 System process I/O equipment attached to the Processor-Controller, with any necessary data-processing I/O units. The minimum system will satisfy initial control and analysis needs and can be expanded to support medium-scale applications.
- 2. The 1800 System process I/O equipment attached directly to an IBM System/360 Model 30, 40, 44, or 50. This configuration is well suited to medium-scale, real-time applications involving substantial data processing loads.
- 3. One or more 1800 Systems (Processor-Controllers, each with appropriate process I/O equipment) communicating with System/360 via Communications Adapter (CA), System/360 Adapter, or through use of shared files on the 2311 Disk Storage Drives. These multiprocessor configurations are suited to large-scale real-time applications, and can be expanded to supply almost any combination of data processing capability and real-time input/output channel capacity.

PROCESSOR-CONTROLLER (P-C)

- Central Processing Unit provides arithmetic, logic, and control functions for the 1800
 System.
- Stored program controls input/output and processing.
- Standard features include three Index Registers, 12 levels of Priority Interrupt, three Data Channels, three Interval Timers, an Operations Monitor, and an Operator's Console.
- Design includes basic circuitry and controls for attachment of process input/output equipment.

The Processor-Controller contains a binary stored-program Central Processing Unit (CPU). Within its

basic design, it has interrupt and cycle-stealing capabilities which are used in controlling the various I/O devices to be attached to the using system. Index Registers and Indirect Addressing are provided to facilitate address modification and programming.

A complete instruction set with powerful options gives the computer very high performance for tasks normally encountered in data acquisition and control applications.

Two Processor-Controllers are available: the IBM 1801 and the IBM 1802. Each has ten models based on speed and size of core storage. (Core storage size may be expanded with the addition of an IBM 1803 Core Storage Unit as described under "Core Storage.") The 1801 has no provision for magnetic tape, while the 1802 includes the Tape Control Unit for the IBM 2401/2402 Magnetic Tape Units.

PROCESS INPUT/OUTPUT FEATURES

- Modular features are available to match the 1800 System with the process requirements.
- Analog Input converts bipolar voltage or current signals to digital values for use by the computer.
- Digital Input accepts binary information represented by contact closures or voltage levels.
- Analog Output converts digital values to precise voltage levels for operating process devices.
- Digital Output provides binary data to the process in the form of "contact" closures or voltage levels.

Analog Input features include analog-to-digital converters, multiplexers, amplifiers, and signal conditioning equipment to handle all types of process analog and input signals. System conversion rates to 20,000 samples per second are provided, with program selectable resolution and external synchronization. Analog input capacities are 1,024 relay multiplexer points and 256 solid-state (high-speed) multiplexer points. A second analog-to-digital converter can be added to double the system analog input performance and capacity.

The Digital Input features provide up to 384 process interrupt points; up to 1,024 bits of contact sense, digital input, high-speed parallel register input; or 128 high-speed pulse counters.

Analog Output features provide up to 128 analog output points for individual or simultaneous operation of a wide range of customer devices.

The Digital Output features provide up to 2,048 bits of pulse output, electronic "contact" operate, and high-speed register output.

DATA PROCESSING I/O UNITS

Adapters and controls are available for attaching a wide variety of data processing I/O units.

Data processing I/O units function with an external document such as a punched card or a reel of magnetic tape. To provide the logical and buffering capabilities necessary for operation on the 1800 system, a control (adapter) feature is available for each I/O Unit.

The following I/O units can be attached to the 1800 System via the data processing I/O attachment features:

1053 Printer

1054 Paper Tape Reader

1055 Paper Tape Punch

1442 Card Read Punch

1443 Printer

1627 Plotter

1810 Disk Storage

1816 Printer-Keyboard

2311 Disk Storage Drive (attached via a Selector Channel and IBM 2841 Storage Control)

2401/2402 Magnetic Tape Unit

COMMUNICATIONS DEVICES

These devices and adapters enable expansion of the 1800 System's capabilities so that it can be utilized in applications requiring multiprocessor systems, remote telecommunication or direct communication capabilities, or multipoint real-time data collection or plant communications. These devices include:

- Communications Adapters
- System/360 Adapter
- 2790 Adapters

SYSTEM DATA FLOW

- Data is stored and processed in fixed-length 18bit words for fast parallel manipulation of data.
- The I/O devices are linked to the Processor-Controller via a standard I/O interface.

- Adapter circuitry at each I/O device performs the necessary conversion, buffering, and control functions.
- Cycle-stealing capability permits high-speed transfer of data.

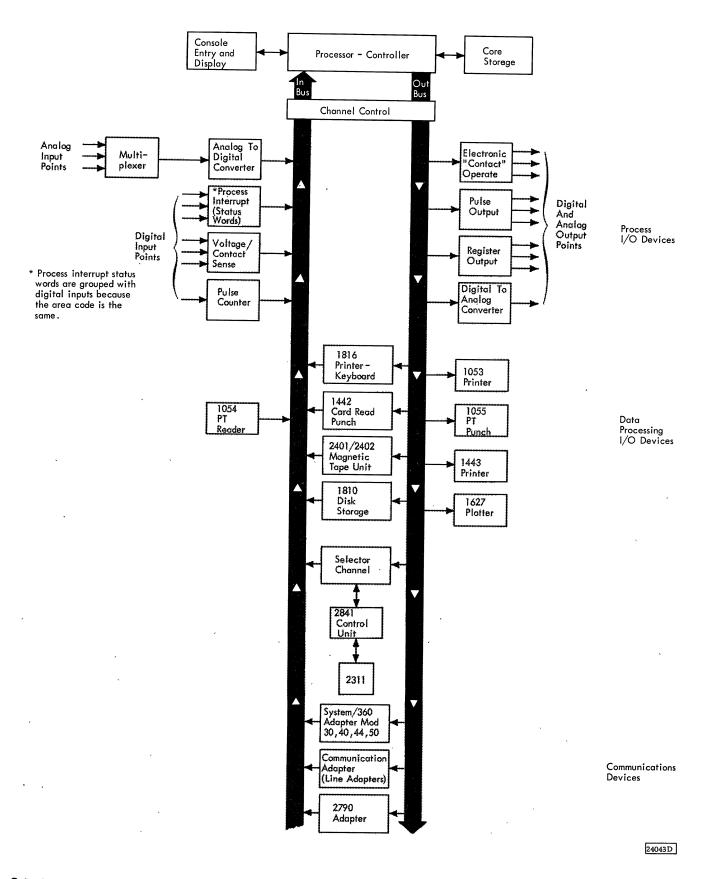
A standard I/O interface is used between the Processor-Controller (P-C) and all input/output devices. Adapter circuitry to accommodate each type of I/O device is installed in the 1800 System as required. The adapters provide the necessary buffer registers and controls to permit operation on the system.

Configuration 1 shows the data flow between the P-C and the various I/O devices. In a closed-loop system, process conditions are monitored and analyzed continuously, and controlling signals are sent to the devices that control the process. Input data is obtained directly from measuring devices in the process area without the need for off-line conversion equipment. Electrical signals are accepted in analog or digital form from such devices as thermocouples, pressure transducers, digital voltmeters, and contacts. Signal conditioning, multiplexing, and conversion functions are performed by the input circuits. The input data, in 1800 System format, is held in registers until called for entry into core storage.

After the input data has been read and analyzed by the Processor-Controller, the program may

select a process control function. Both digital and analog output data can be generated for controlling equipment such as set-point positioners, displays, and telemetry systems. Data processing information can be entered and retrieved in a variety of forms through the DP I/O units and their adapter circuitry.

When a device is ready to send or receive data, it can notify the Processor-Controller by issuing an interrupt request. The program identifies the source of the interrupt by sensing the status of indicators associated with each I/O device. The program responds to the interrupt by sending the appropriate I/O command to the device. Each I/O command always places a control word on the Out-Bus to specify the input/output device and the function to be performed. Depending on the intrinsic data rate of the I/O device receiving the control word, the transfer of data between core storage and the device can take place under direct program control, or on a Data Channel operation. A Data Channel transfers data on a high-speed cycle-steal basis, using a data table in core storage for flexibility of scanning rates and patterns. The cycle-stealing capability makes it possible to delay the program for one machine cycle and to use this cycle to transfer the data word between P-C storage and the I/O device. Cycle-stealing and interrupt servicing are conducted by the P-C on a priority basis. This makes it possible to simultaneously control combinations of real-time input/output devices.



Configuration 1. IBM 1800 Data Acquisition and Control System

A brief description of 1800 features and units follows. This description will facilitate an understanding of the P-C instruction set. More detailed descriptions are provided at appropriate sections of the manual.

PROCESSOR-CONTROLLERS

The Processor-Controllers (1801 and 1802), are fixed-word-length, binary computers. Five core storage sizes (4,096; 8,192; 16,384; 24,576; or 32,768 words of 18 bits each) with core storage cycle times of 2 or 4 microseconds (μ sec) are available. With the addition of an IBM 1803 Core Storage Unit, four additional system core storage sizes (40,960; 49,152; 57,344; and 65,536 words of 18 bits each) with core storage cycle time of 2.25 μ sec are also available. One of the 18 bits in a core storage word is used for storage protection and one bit is used for parity checking. The remaining 16 bits in each core storage word are data bits.

The instruction set (many of which serve multiple functions) includes arithmetic instructions that manipulate both 16-bit and 32-bit words (16 data bits are handled in parallel). The 2 μ sec system can perform high-speed I/O operations during cycle steal operations via Data Channels at rates up to 500,000 words (or 8,000,000 bits) per second in burst mode. Both indirect addressing and index registers (3) are provided for address modification.

Other Processor-Controller (P-C) features include a multi-level interrupt system, three high-resolution interval timers, storage protection, Customer Engineering (CE) storage for limited on-line DP I/O maintenance, operations monitor and an operator's console.

DATA REPRESENTATION

The standard or single precision data word is 16 bits in length.



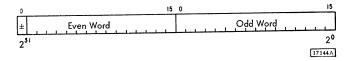
Positive numbers are always in true binary form, whereas negative numbers are in 2's complement form. The sign bit (position 0) is always 0 for positive numbers and 1 for negative numbers. The 2's complement of a binary number is defined as its 1's complement increased by one. The 1's complement of a binary number is that number that results by replacing each 1 in the number with a 0 and each 0 with a 1. Some decimal numbers are shown in Figure 1 with their binary equivalents and 1's and 2's complements.

Decimal	Binary	1's Comp	2's Comp
15	01111	10000	10001
9	01001	10110	10111
3	00011	11100	11101
			17 143

Figure 1. Binary 1's and 2's Complement

Bit positions 1 through 15 represent decimal values of 2^{14} through 2^0 respectively. Thus the largest single precision positive number that can be represented is 2^{15} -1 or 32,767 (a sign bit of 0 and 1's in all other bit positions). The largest negative number is -2^{15} or -32,768 (a sign bit of 1 and 0's in all bit positions) The number zero is represented by all bits being zero. There is no negative zero.

A double precision number of 32 bits can be used to give a number range from +2,147,483,647 to -2,147,483,648 (2^{31} -1 to -2^{31}) Two adjacent words must be used in core storage with the leftmost word at an even address and the right-most word at the next higher odd address.



CORE STORAGE

Five core storage sizes are available in the 1801/1802 P-C. The IBM 1803 Core Storage Unit provides facilities for an additional four core storage sizes for the system, bringing the total number of sizes to

nine. System core storage sizes and cycle times—that is, the time required to transfer a word to or from a core storage address—are as follows:

Storage Size (18-bit words)	Storage Cycle Time
4,096	2 or 4 μsec
8,192	$2 \text{ or } 4 \mu \text{sec}$
16,384	$2 \text{ or } 4 \mu \text{sec}$
24,576	$2 \text{ or } 4 \mu \text{sec}$
32,768	$2 \text{ or } 4 \mu \text{sec}$
40,960	$2.25~\mu\mathrm{sec}$
49,152	$2.25~\mu\mathrm{sec}$
57,344	$2.25~\mu\mathrm{sec}$
65,536	$2.25~\mu\mathrm{sec}$

In systems with core storage capacities above 32,768 words, the P-C contains 24,576 words of core storage and an 1803 adapter. The 1803 contains either 16,384; 24,576; 32,768; or 40,960 words of core storage depending on which 1803 model is ordered.

Each core storage word consists of 18 bits: 16 are data bits which can be either data or instructions; one bit is used for the Storage Protect feature; one bit is used to maintain odd parity. Parity includes the 16 data bits and the storage protect bit. The parity bit cannot be affected by the program. Detection of a parity check causes an interrupt to the internal interrupt level. See "Interrupt" section.

Core storage addresses 00001 and 00002 are reserved for CE Interrupt; addresses 00004, 00005, and 00006 are reserved for the Interval Timers; addresses 00008 through 00034 are reserved for interrupt addresses.

Addressing

Although core storage addresses have been expressed in decimal (base 10) form up to now, the 1800 P-C uses a binary (base 2) form. Internal addressing and console displays are in 16-bit binary form. However, greater ease of operation is realized when hexadecimal (base 16) notation is used. Programming Systems for the 1800 make use of hexadecimal notation.

The different notations are shown in the following illustration.

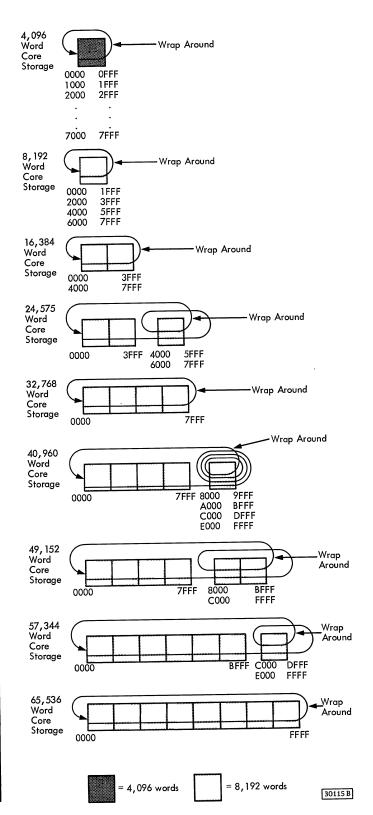
Core Storage Address Notation		
Base 10	Base 2	Base 16
4095	0000 1111 1111 1111	OFFF
8191	0001 1111 1111 1111	1FFF
16,383	0011 1111 1111 1111	3FFF
24,575	0101 1111 1111 1111	5FFF
32,767	0111 1111 1111 1111	7FFF
40,959	1001 1111 1111 1111	9FFF
49,151	1011 1111 1111 1111	BFFF
57,343	1101 1111 1111 1111	DFFF
65,535	1111 1111 1111 1111	FFFF

17811

A wrap around addressing scheme for core storage is provided in the 1800 System. Core storage addresses begin at zero (000016). The ending addresses depend on the core storage size and are shown in the preceding illustration. However, the address register increments or decrements through the full spectrum of addresses. That is, 000016 through 7FFF₁₆ for core storage sizes of 32,768 words or less, or 0000_{16} through FFFF₁₆ for core storage sizes above 32,768 words. Depending on core storage size, this may produce multiple excursions through portions of core storage or cause wrap around to occur more than once with one pass through the address spectrum. The programmer should be aware that storage is addressed even if the address register contains an address above actual core storage size.

The following examples illustrate how wrap around occurs for each core storage size. Note the unique differences in the 24,576; 40,960; 49,152; and 57,344 word models.

Note: When an instruction is executed, the instruction register (I) contains the address of the next sequential instruction.



ARITHMETIC

The arithmetic operations of the P-C include add, subtract, multiply, and divide. Negative data is always stored and operated upon in 2's complement form. Addition and subtraction can be done in single or double precision. Multiplication operates on two single precision words to provide a double precision product. Division allows the dividend to be double length and uses a single precision divisor to provide a single precision quotient and a single precision remainder.

Overflow and Carry Indicators

The two indicators associated with the Accumulator are Overflow and Carry. The Overflow indicator can be turned on by add, subtract, or divide, and indicates a result larger than can be represented in the Accumulator. The Overflow indicator can also be turned ON by a Load Status instruction. Once Overflow is on, it will not be changed except by testing the indicator, or by a Load Status or Store Status instruction. The Carry indicator provides the information that a carry (or borrow) from the high order position of the Accumulator has occurred. The Carry indicator is dynamic and changes with each add or subtract operation. The Carry indicator is also affected by Shift Left, Load Status, Store Status, and Compare instructions.

INDIRECT ADDRESSING

Indirect addressing is a standard feature of the 1800. One level of indirect addressing is provided. Indirect addressing cannot be used with one word instructions. The instructions that can be modified by indirect addressing are indicated in the Instruction Set section. The recognition in the instruction of an Indirect Address control bit (position 8, two-word instruction only) causes the address portion to be treated as an indirect address. The address after indexing (if specified) gives the location of the effective address. An additional core storage cycle is required for indirect addressing.

INDEX REGISTERS

Three index registers (XR) are standard features. The XRs are addressed by the TAG (positions 6 and 7 in the instruction) as follows:

Bits 6 & 7	_XR_
01	1
10	2
11	3

Operations on the XR, such as load, store, modify and skip, are accomplished through instructions in the basic instruction set. The contents of an Index Register or the Instruction Register are usually used to perform address arithmetic.

DATA CHANNELS

Data Channels give the P-C the ability to delay the execution of a program while an I/O device communicates with core storage. For example, if an input unit requires a core storage cycle to store data that it has collected, the data channel with its "cycle stealing" capability makes it possible to delay the program during execution of an instruction and store the data word without changing the logical condition of the P-C. After the data is stored, the P-C continues executing the program which was delayed by the "cycle-stealing". This capability should not be confused with interrupt which changes the contents of the Instruction Register.

Cycle stealing by the Data Channels can occur at the end of any core storage cycle. Maximum delay before cycle stealing can occur is 2.25 μs for the 2 μs system, 2.50 μs for the 2.25 μs system, and 4.5 μs for the 4 μs system, assuming no higher level cycle steal is active.

A Wait instruction, which halts the P-C, will not stop the operations of Data Channels.

INTERRUPT

The interrupt facility provides an automatic branch in the normal program sequence based upon external conditions (those in the process) or internal conditions (those within the 1800). Examples of such conditions are:

- The detection of an external process condition that requires immediate attention.
- A P-C Interval Timer has concluded the recording of a preset time interval.
- A magnetic tape drive has completed a data transfer previously requested and is ready for another request.

 An operator has initiated an interrupt from the P-C console.

These devices and conditions are assigned priority levels by the user. An interrupt request is not honored while the level of the request itself or any higher level is being serviced or if the level requested is masked. A request is honored if the level is not masked and no interrupt is being serviced or if any level lower than that of the request is being serviced. A Wait instruction does not prevent interrupts from being serviced.

INSTRUCTION FORMATS

Two basic instruction word formats are used (Figures 2 and 3). The bits within the instruction words are used in the following manner:

OP	These five bits define which opera-
F	tion is to be performed by the P-C. This format bit controls the instruction format. A "zero" indicates a single word instruction and a "one" indicates a two word instruction.
Т	These two Index Tag bits specify the base register (XR, I or AD- DRESS) used in address modifica- tion or the location (XR or DISP) of the shift count.
DISP	These eight bits are called the displacement and, with one word instructions only, are usually added to the Instruction Register or the index register specified by T. The modified address is defined as the effective address (EA). If T is 00, the displacement is added to the Instruction Register (then EA=I+DISP). The displacement is in 2's complement form if negative, with the sign in bit 8. The bit in position 8 is automatically extended to the higher ordered bits (0-7) when the displacement is used in EA generation, or as an add to core storage operand.
IA	The Indirect Addressing bit is used in the two word instruction format. If "zero", addressing will be direct. If a "one", addressing will be indirect. See the Load Index and Modify Index and Skip

Instructions for exceptions.

во This bit is used to specify that the Branch or Skip on Condition (BSC) instruction is to be interpreted as a "Branch Out" (BOSC) when used in an interrupt routine. Specifies the condition of indicators COND

that are interrogated on a BSC or BSI instruction.

ADDRESS These 16 bits usually specify a core storage address in a two word instruction. The address can be modified by the contents of an index register or used as an indirect address if the IA bit

is on.

Effective Address Generation

The effective address (EA) is developed as shown in Table 1 for most instructions. (Exceptions are noted in the Instructions section.)

P-C REGISTERS

The following registers are used in the manipulation of data within the P-C and may be displayed on the P-C console.

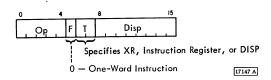


Figure 2. One-Word Instruction Format

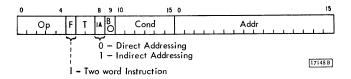


Figure 3. Two-Word Instruction Format

Storage Address Register (SAR)

All P-C program references to storage are under direct control of this 16-bit register. Data Channel (DC) references to storage use the Channel Address Register (CAR) of the active DC. See "Data Channel" section.

Table 1. Determining Effective Addresses

	F = 0	F = 1, IA = 0	F = 1, IA = 1
	(Direct Addressing)	(Direct Addressing)	(Indirect Addressing)
T = 00 T = 01 T = 10 T = 11	EA = I+Disp EA = XR1+Disp EA = XR2+Disp EA = XR3+Disp	EA = Address EA = Address+XR1 EA = Address+XR2 EA = Address +XR3	(3) EA = C (Address) EA = C (Address+XR1) EA = C (Address+XR2) EA = C (Address+XR3)

- Contents of instruction register or index register.
- May be true positive quantity or negative 2's complement quantity.
- C specifies "Contents" at location specified by address or address +XR1,2, or 3.

17149

Instruction Register (I)

This 16-bit counter register holds the address of the next sequential instruction. It is automatically incremented for sequential operation of instructions.

Storage Buffer Register (B)

This 16-bit register is used for buffering all word transfers with core storage.

Arithmetic Factor Register (D)

This 16-bit register is used to hold one operand for arithmetic and logical operations. The Accumulator provides the other factor.

Accumulator (A)

This 16-bit register contains the results of any arithmetic operation. It can be loaded from or stored into core storage, shifted right or left, and otherwise manipulated by specific arithmetic and logical instructions.

Accumulator Extension (Q)

This register is a 16-bit low order extension of the Accumulator. It is used during multiply, divide, shifting, and double precision arithmetic.

Shift Control Counter (SC)

This six-bit counter is used primarily to control shift operations.

OP Register (OP)

This five-bit register is used to hold the operation code portion of an instruction.

<u>Note</u>: The above registers are also used uniquely in specific operations described later.

P-C DATA FLOW

As shown in the simplified P-C data flow block diagram (Figure 4), all instructions and data entering and leaving core storage do so via the B-register. Input devices send data and instructions to the B-register via the In-Bus. Output devices receive data from the B-register via the Out-Bus. As each stored program instruction is selected, its various parts (op code, format bit, etc.) are directed to the control registers via the B-register and the Out-Bus. The control registers decode and interpret each instruction before the instruction is executed.

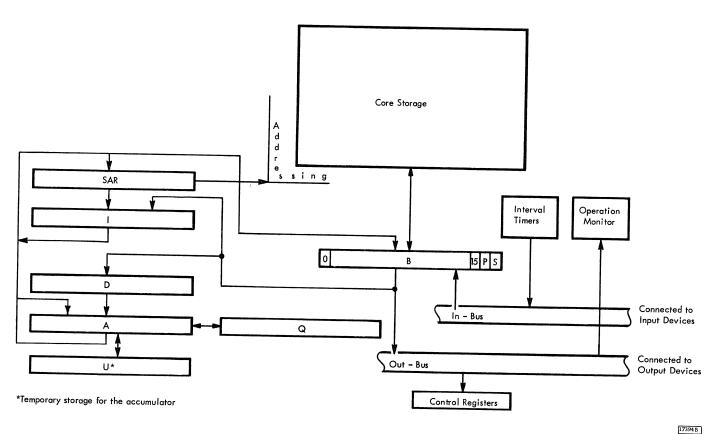


Figure 4. 1800 P-C Data Flow

Except for Data Channel operations (see "I/O Control" section), all instructions and data must first be addressed by the Storage Address Register (SAR) before leaving core storage. SAR obtains the core storage address from the I-register or the A-register. The contents of the I-register are developed by one of the following means, depending on the P-C operation:

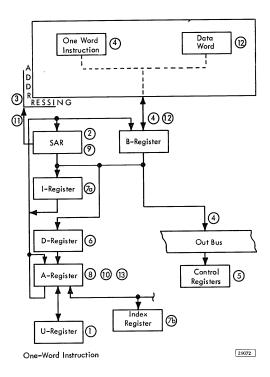
- The I-register is incremented for each instruction during sequential operation of the stored program instructions.
- 2. The effective address of each instruction is developed in the accumulator (A-register) and then transferred to SAR. The contents of the accumulator are saved in an auxiliary (U) register during effective address computation. If the instruction was a branch, the contents of SAR is transferred to the I-register.

Data Transfer, 18 Bits

Each word in core storage comprises 18 bits: 16 data bits, a parity bit (P), and a storage protect bit (S). During P-C operation, the P bit is automatically added or removed to maintain odd parity. The S bit is added or removed by the Store Status instruction, depending on whether a "read only" condition is desired. The 16 data bits enter or leave core storage via the B-register. The P and S bits do so via individual latches. The latches and the B-register together enable the transfer of 18 bits to and from core storage. The In-Bus and the Out-Bus contain 16 data lines and 2 parity lines. Thus, 18 bits can be transferred between the P-C and the magnetic tape units. (See "Data Formats" in the magnetic tape units section.)

DATA FLOW EXAMPLES

The following three examples illustrate the data flow for the Load Accumulator (LD) instruction including an example for each type of addressing (one-word format; two-word format, Direct and Indirect addressing). Circled numbers in each illustration correspond to the numbered items included for that illustration.



One-Word Instruction

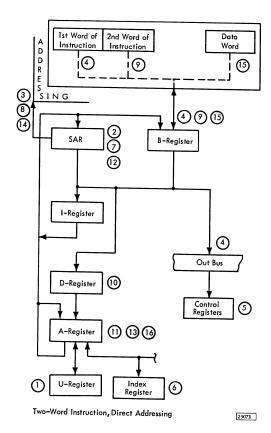
Instruction Cycle

- 1. A-register transfers to U-register.
- 2. I-register transfers to SAR (I-register is then incremented).
- 3. SAR addresses the core-storage location containing the instruction.
- 4. Core-storage location transfers to the B-register and out-bus.
- 5. Control registers store various parts of the instruction (op-code, format, and tag).
- 6. Displacement is stored in the D-register.
- 7. a. If tag = 00, I register transfers to A-register.
 - b. If $tag \neq 00$, the specified XR transfers to A-register.
- 8. Displacement (D-register) is added to A-register.

Execute Cycle

- 9. A-register transfers to SAR (effective address).
- 10. U-register transfers to A-register.

- 11. SAR addresses data word.
- 12. Data word transfers to B-register.
- 13. B-register loads into A-register (through D-register).



Two-Word Instruction, Direct Addressing

Instruction Cycle 1

- 1. A-register transfers to U-register.
- 2. I-register transfers to SAR (I-register is then incremented)
- 3. SAR addresses the core-storage location containing the instruction (1st word)
- 4. Core-storage location transfers to B-register and out-bus.
- 5. Control registers store various parts of the instruction (op code, format, and tag).
- 6. If tag ≠ 00, the specified XR transfers to A-register.

Instruction Cycle 2

- 7. I-register transfers to SAR (I-register is then incremented).
- 8. SAR addresses second word of instruction.
- 9. Second word of instruction (address) is read into B-register.
- 10. Address (from B-register) is stored in D-register.
- 11. a. If tag = 00, D-register transfers to A-register.
 - b. If $tag \neq 00$, D-register is added to A-register (A-register contains contents of XR).

Execute Cycle

- 12. A-register transfers to SAR (effective address).
- 13. U-register transfers to A-register.
- 14. SAR addresses core-storage at effective address (data word).
- 15. Data word transfers to B-register.
- 16. B-register loads into A-register (through D-register.)

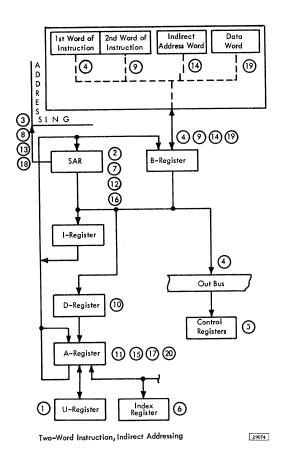
Two-Word Instruction, Indirect Addressing

Instruction Cycle 1

- 1. A-register transfers to U-register.
- 2. I-register transfers to SAR (I-register is then incremented).
- 3. SAR addresses core-storage location containing the instruction (1st word).
- Core-storage location transfers to B-register and out-bus.
- 5. Control registers store the various parts of the instruction (op-code, format, and tag).
- 6. If tag ≠ 00, the specified XR transfers to A-register.

Instruction Cycle 2

- 7. I-register transfers to SAR (I-register is then incremented).
- 8. SAR addresses second word of the instruction.
- 9. Second word of the instruction (address) is read into B-register.



- 10. Address (from B-register) is stored in D-register.
- 11. a. If tag = 00, D-register transfers to A-register.
 - b. If $tag \neq 00$, D-register is added to A-register. (A-register contains contents of XR).

Indirect Addressing Cycle

- 12. A-register transfers to SAR.
- 13. SAR addresses core-storage location at address (or address + XR).
- 14. Core-storage location transfers to B-register.
- 15. B-register transfers to A-register (through D-register).

Execute Cycle

- 16. A-register transfers to SAR.
- 17. U-register transfers to A-register.
- 18. SAR addresses core storage at effective address (data word).
- 19. Data word transfers to B-register.
- 20. B-register loads into A-register (through D-register).

The 1800 instruction set is shown in Table 2. An invalid code (such as 0000) enables the programmer to detect an inadvertent branch to noninstruction area of core storage. Each instruction falls into one of five classes. Note that the instructions which may be used with indirect addressing are indicated in the Indirect Addressing column. Some instructions perform multiple uses, as specified by their control bits. A more complete breakdown of instructions, including hexadecimal representations, is found in sections for each instruction and in Appendix A. Execution times are provided in Appendix B.

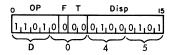
Table 2. Instruction Set

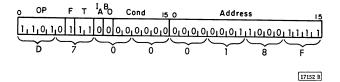
Class	Instruction	Indirect Addressing	Mnemonic
Load and Store	Load Accumulator Double Load Store Accumulator Double Store Load Index Store Index Load Status Store Status	Yes Yes Yes Yes Yes No Yes	LD LDD STO STD LDX STX LDS STS
Arithmetic		Yes	A AD S SD M D AND OR EOR
Shift	Shift Left Instructions Shift Left Logical (A) * Shift Left Logical (AQ)* Shift Left and Count (AQ)* Shift' Left and Count (A) *	2 0 0 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	SLA SLT SLC SLCA
Branch	Shift Right Instructions Shift Right Logical (A)* Shift Right Arithmetically (AQ)* Rotate Right (AQ)* Branch and Store I Branch or Skip on Condition Modify Index and Skip Wait Compare Double Compare	No No No Yes Yes ** No Yes Yes	SRA SRT RTE BSI BSC (BOSC) MDX WAIT CMP DCM
1/0	Execute I/O	Yes	XIO

^{*} Letters in parentheses indicate registers involved in shift operations.

17151 D

Hexadecimal Representation





The hexadecimal version(s) of each instruction is provided with its description. The hexadecimal number is derived by dividing each word into groups of four bits each and assigning a hexadecimal value corresponding to the decimal (BCD) value of each group.

Instruction Format and Operation Symbology

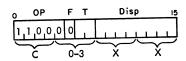
The following descriptions of 1800 P-C instructions include the instruction format(s) that can be used with each instruction, the effect of the instruction on the carry and overflow indicators, and the hexadecimal representations of each instruction. Symbols are used to describe the objective of each hexadecimal representation of instructions. The symbols and their meanings are:

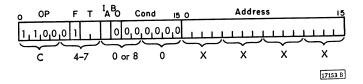
$\underline{\text{Symbol}}$	Meaning
A	Accumulator
Q	Accumulator Extension
ADDRESS	Contents of the Address
or	portion of a two-word
Addr	instruction.
CSL :	Core Storage Location
DISP	Contents of the Displacement
	portion of a one-word instruction.
$\mathbf{E}\mathbf{A}$	Effective Address (see Table 1)
EA +1	Next higher address from the
	Effective Address
I	Contents of the Instruction Register
V	Value
XR1	Contents of Index Register 1
XR2	Contents of Index Register 2
XR3	Contents of Index Register 3
X	Hexadecimal value (can be 0-F).
*	Used for hexadecimal values that
	have limits. The limits are given
	below each group of hexadecimal
	instructions.

^{**} See the section for the individual instruction (MDX and LDX)

LOAD AND STORE INSTRUCTIONS

LOAD ACCUMULATOR (LD)





Description: The contents of the core storage location specified by the effective address (EA) of the instruction replace the contents of the Accumulator (A). The contents of the core storage location are unchanged.

<u>Indicators</u>: The Carry and Overflow indicators are not changed by this instruction.

Hexadecimal Representation

One-Word Instruction

C0XX	Contents of CSL at EA (I+DISP) are
	loaded into A
C1XX	Contents of CSL at EA (XR1+DISP)
	are loaded into A
C2XX	Contents of CSL at EA (XR2+DISP)
	are loaded into A
C3XX	Contents of CSL at EA (XR3+DISP)
	are loaded into A

Two-Word Instruction, Direct Addressing

C400XXXX	Contents of CSL at EA (Addr) are
	loaded into A (See example.)*
C500XXXX	Contents of CSL at EA (Addr +XR1)
	are loaded into A
C600XXXX	Contents of CSL at EA (Addr +XR2)
	are loaded into A
C700XXXX	Contents of CSL at EA (Addr +XR3)
	are loaded into A

Two-Word Instruction, Indirect Addressing

C480XXXX Contents of CSL at EA (V in CSL at Addr) are loaded into A

C580XXXX Contents of CSL at EA (V in CSL at "Addr +XR1") are loaded into A

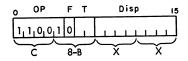
C680XXXX Contents of CSL at EA (V in CSL at "Addr +XR2") are loaded into A

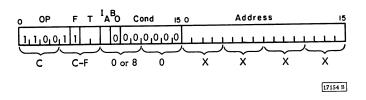
C780XXXX Contents of CSL at EA (V in CSL at "Addr +XR3") are loaded into A



In the preceding example the accumulator is loaded with the contents of DATA.

DOUBLE LOAD (LDD)





<u>Description</u>: The contents of the core storage location specified by the instruction (EA) and the next higher core storage location (EA+1) are loaded into the Accumulator (A) and its extension (Q), respectively. This provides double precision load for use with the double precision arithmetic. The EA of the instruction must be an even address for correct operation. If the EA is odd, the contents of that location are entered into both the Accumulator and its extension. The contents of core storage remain unchanged.

<u>Indicators</u>: The Carry and Overflow indicators are not changed by this instruction.

Hexadecimal Representation

One-Word Instruction

C8XX Contents of CSL at EA (I+DISP) and EA+1 are loaded into A and Q

^{*}Throughout the instruction section are Assembler Language examples; the particular form illustrated is followed by a (See example) note.

C9XX	Contents of CSL at EA (XR1 + DISP)
	and EA+1 are loaded into A and Q
CAXX	Contents of CSL at EA (XR2 + DISP)
	and EA+1 are loaded into A and Q
CBXX	Contents of CSL at EA (XR3 + DISP)
	and EA+1 are loaded into A and Q

Two-Word Instruction, Direct Addressing

CC00XXXX	Contents of CSL at EA (Addr) and
	EA+1 are loaded into A and Q
	(See example.)
CD00XXXX	
	+XR1) and EA+1 are loaded into
	A and Q
CE00XXXX	Contents of CSL at EA (Addr
	+XR2) and EA+1 are loaded into
	A and Q
CF00XXXX	Contents of CSL at EA (Addr
	+XR3) and EA+1 are loaded into
	A and Q

Two-Word Instruction, Indirect Addressing

CC80XXXX	CSL at EA (V in CSL at Addr) and
CD80XXXX	EA+1 are loaded into A and Q CSL at EA (V in CSL at "Addr +XR1") and EA+1 are loaded into
CE80XXXX	A and Q
OLOUAAAA	CSL at EA (V in CSL at "Addr +XR2") and EA+1 are loaded into
CF80XXXX	A and Q
OI OUXAAA	CSL at EA (V in CSL at "Addr +XR3") and EA+1 are loaded into A and Q

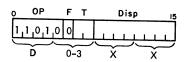
Labe	ı	Operation	Π	F	т				
21	25	 27 30	<u> </u>	32	33	L	35	40	45
		$L_iD_iD_i$		L			D,A,T,A,		

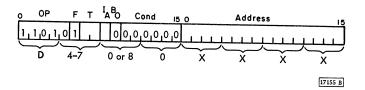
Note: Data must be an even address.

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In the preceding example the Accumulator and Extension are loaded with the contents of DATA and DATA +1. To receive the desired results DATA must be an even address.

STORE ACCUMULATOR (STO)





Description: The contents of the Accumulator replace the contents of the core storage location specified by the effective address. The contents of the Accumulator are unchanged.

<u>Indicators:</u> The Carry and Overflow indicators are not changed by this instruction.

Hexadecimal Representations

One-Word Instruction

D0XX	Contents of A are stored in CSL at EA (I+DISP)
D1XX	,
DIAA	Contents of A are stored in CSL
	at EA (XR1+DISP)
D2XX	Contents of A are stored in CSL
	at EA (XR2+DISP)
D3XX	·
DOAA	Contents of A are stored in CSL
	at EA (XR3+DISP)
20111	at EA (XR3+DISP)

Two-Word Instruction, Direct Addressing

D400XXXX	Contents of A are stored in CSL
	at EA (Addr)
D500XXXX	Contents of A are stored in CSL
	at EA (Addr +XR1)
D600XXXX	Contents of A are stored in CSL
	at EA (Addr +XR2)
D700XXXX	Contents of A are stored in CSL
	at EA (Addr +XR3)

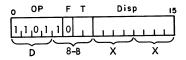
Two-Word Instruction, Indirect Addressing

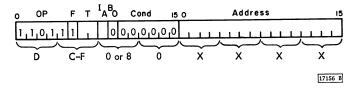
D480XXXX	Contents of A are stored in CSL
	at EA (V in CSL at Addr) (See .
	example.)
D580XXXX	Contents of A are stored in CSL
	at EA (V in CSL at "Addr +XR1")
D680XXXX	Contents of A are stored in CSL
	at EA (V in CSL at "Addr +XR2")
D780XXXX	Contents of A are stored in CSL
	at EA (V in CSL at "Addr +XR3")

Labe	1	Opera	tion	F	т						
21	25	27	30	32	33		35	40		45	
		SIT	٥	I		ľ	$W_iO_iR_iD_i$		لــــــــــــــــــــــــــــــــــــــ	 . 1	1 1 1
			_								
											30132

In the preceding example the accumulator is stored at the location whose address is stored at WORD.

DOUBLE STORE (STD)





Description: The contents of the Accumulator (A) and its extension (Q) are stored at the core storage locations specified by the effective address (EA) and the EA+1. This provides double precision store for use with the double precision arithmetic. The EA of the instruction must be an even address for correct operation. If the EA is odd, the contents of the Accumulator are stored at the EA and the contents of the Accumulator Extension (Q) will not appear in core storage. The contents of A and Q remain unchanged.

<u>Indicators:</u> The Carry and Overflow indicators are not changed by this instruction.

Hexadecimal Representation

One-Word Instruction

D8XX	Contents of A and Q are stored in
DOXX	
	CSL at EA (I+DISP) and EA+1
D9XX	Contents of A and Q are stored in
	CSL at EA (XR1 +DISP) and EA+1
DAXX	Contents of A and Q are stored in
	CSL at EA (XR2 +DISP) and EA+1
DBXX	Contents of A and Q are stored in
	CSL at EA (XR3 +DISP) and EA+1

Two-Word Instruction, Direct Addressing

DC00XXXX	Contents of A and Q are stored in
	CSL at EA (Addr) and EA+1
DD00XXXX	Contents of A and Q are stored in
	CSL at EA (Addr +XR1) and EA+1
DE00XXXX	Contents of A and Q are stored in
	CSL at EA (Addr +XR2) and EA+1
	(See example.)
DF00XXXX	Contents of A and Q are stored in
	CSL at EA (Addr +XR3) and EA+1

Two-Word Instruction, Indirect Addressing

DC80XXXX	Contents of A and Q are stored in
20001111111	CSL at EA (V in CSL at Addr) and
	EA+1
DD80XXXX	Contents of A and Q are stored in
	CSL at EA (V in CSL at "Addr
	+XR1") and EA+1
DE80XXXX	Contents of A and Q are stored in
	CSL at EA (V in CSL at "Addr
	+XR2") and EA+1
DF80XXXX	Contents of A and Q are stored in
	CSL at EA (V in CSL at "Addr
	+XR3") and EA+1

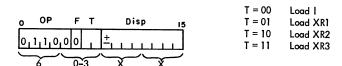
1 1 1	S,T,D,	L	2	W,O,R	', , , , , , , , , , , , , , , , , , ,	
Label	Operation	F 32	T 33	35	40	45

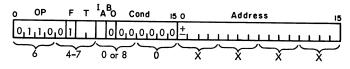
Note: Word + XR2 must be an even address.

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In the preceding example the accumulator and extension are stored at EA and EA + 1. The EA is determined by adding the address of WORD to index register 2. The EA must be an even address.

LOAD INDEX (LDX)





IA = 0 - Load Immediate
IA = 1 - Load Direct

17157 B

<u>Description</u>: An Index Register (XR) or the Instruction Register (I) is loaded by the DISPLACEMENT, the ADDRESS, or the contents of the location specified by the ADDRESS. The T bits indicate which Register is loaded and the F and IA (2-word instruction only) bits determine the source of data.

If the F bit is 0, the register specified by T is loaded with the DISPLACEMENT. The eight high-order positions of the specified register are filled with the value of the sign bit (bit position 8 of instruction) to complete the 16-bit word.

If, however, the F bit is 1, the loading of the register is dependent on the IA bit of the instruction. If the IA bit is 1, the register is loaded with the contents of the word specified by the ADDRESS; if 0, the register is loaded with the ADDRESS portion of the instruction.

<u>Indicators</u>: The Carry and Overflow indicators are not changed by this instruction.

Hexadecimal Representation

One-Word Instructions

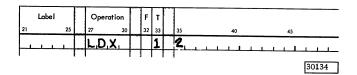
60XX	Load DISP into the Instruction
	Register
61XX	Load DISP into Index Register 1
	(See example.)
62XX	Load DISP into Index Register 2
63XX	Load DISP into Index Register 3

Two-Word Instruction, Direct Addressing

6400XXXX	Load Addr into the Instruction
	Register
6500XXXX	Load Addr into Index Register 1
6600XXXX	Load Addr into Index Register 2
6700XXXX	Load Addr into Index Register 3

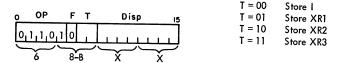
Two-Word Instruction, Indirect Addressing

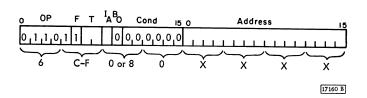
6480XXXX	Load contents of CSL at Addr into
	Instruction Register
6580XXXX	Load contents of CSL at Addr into
	Index Register 1
6680XXXX	Load contents of CSL at Addr into
	Index Register 2
6780XXXX	Load contents of CSL at Addr into
	Index Register 3
6780XXXX	



In the preceding example index register 1 is loaded with the value 2.

STORE INDEX (STX)





Description: An Index Register, or the Instruction Register, is stored in core storage at the Effective Address (EA). The T bits specify which register is stored and bits 5 (F bit) and 8 (IA) govern the generation of the Effective Address.

<u>Indicators:</u> The Carry and Overflow indicators are not affected.

6

Hexadecimal Representation

One-Word Instruction

68XX	Store I in CSL at EA (I+DISP)
69XX	Store XR1 in CSL at EA (I+DISP)
6AXX	Store XR2 in CSL at EA (I+DISP)
6BXX	Store XR3 in CSL at EA (I+DISP)

Two-Word Instruction, Direct Addressing

6C00XXXX	Store I in CSL at EA (Addr)
6D00XXXX	Store XR1 in CSL at EA (Addr)
6E00XXXX	Store XR2 in CSL at EA (Addr)
6F00XXXX	Store XR3 in CSL at EA (Addr)
	(See example.)

Two-Word Instruction, Indirect Addressing

6C80XXXX	Store I in CSL at EA (value in CSL
	at Addr)
6D80XXXX	Store XR1 in CSL at EA (value in
	CSL at Addr)
6E80XXXX	Store XR2 in CSL at EA (value in
	CSL at Addr)
6F80XXXX	Store XR3 in CSL at EA (value in
	CSL at Addr)

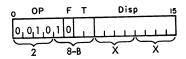
Label		Оре	eration	F	т		
21	25	27	30	32	33	 35 40	45
		S,1	۲,۲,	L	3	P.L.A.C.E.	
	T			Į	1		30135

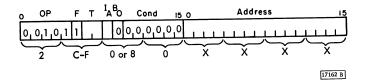
In the preceding example the contents of index register 3 is stored at location PLACE.

STORE STATUS (STS)

<u>Description:</u> Depending on bit 9 (BO), the Store Status instruction is used in either of two operations:

1. Store the status of the Carry and Overflow indicators.

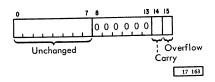




Bit 9 (BO) in the two word instruction must equal zero. The conditions of the Carry and Overflow indicators are stored in the low-order bits of the word

specified by the effective address: Carry indicator at bit 14 and the Overflow indicator at bit 15.

Bits 0 through 7 of the word at the effective address remain unchanged and bits 8 through 13 are reset to zero. The indicators are reset. An ON status stores a one bit; and OFF status a zero bit.



<u>Indicators</u>: The Carry and Overflow indicators are reset as they are stored.

Hexadecimal Representation

One-Word Instruction

$28\mathrm{XX}$	Store status of indicators in CSL
	at EA (I+DISP) (See example.)
29XX	Store status of indicators in CSL
	at EA (XR1+DISP)
2AXX	Store status of indicators in CSL
	at EA (XR2+DISP)
2BXX	Store status of indicators in CSL
	at EA (XR3+DISP)

Two-Word Instruction, Direct Addressing

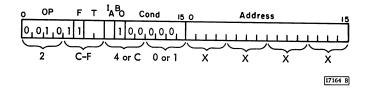
2C00XXXX	Store status of indicators in	CSL	at
	EA (Addr)		
2D00XXXX	Store status of indicators in	CSL	at
	EA (Addr+XR1)		
2E00XXXX	Store status of indicators in	CSL	at
	EA (Addr+XR2)		
2F00XXXX	Store status of indicators in	ı CSL	at

Two-Word Instruction, Indirect Addressing

EA (Addr+XR3)

2C80XXXX	Store status of indicators in CSL at
	EA (V in CSL at Addr)
2D80XXXX	Store status of indicators in CSL at
	EA (V in CSL at "Addr +XR1")
2E80XXXX	Store status of indicators in CSL at
	EA (V in CSL at "Addr +XR2")
2F80XXXX	Store status of indicators in CSL at
	EA (V in CSL at "Addr +XR3")

Write or clear the storage protect bit from the core storage address specified by the instruction.



The following conditions must exist:

- A two word instruction (F bit equals 1) must be used.
- 2. Bit 9 (BO) must equal 1.
- 3. The Write Storage Protection Bit switch must be on to change storage protection bits.

Bit 15 determines whether the storage protect bit for the word specified by the effective address of the instruction is written or cleared:

B15 is zero -- Storage protect bit is cleared. B15 is one -- Storage protect bit is written.

As long as the Write Storage Protection Bit switch remains in the on position the program continues to have the ability to write or clear storage protection bits. If the switch is off this instruction performs as a NO-OP (No-Operation).

Hexadecimal Representation

Two-Word Instruction, Direct Addressing

2C40XXXX	Clear storage protect bit in CSL at
	EA (Addr)
2C41XXXX	Write storage protect bit in CSL at
	EA (Addr)
2D40XXXX	Clear storage protect bit in CSL at
	EA (Addr +XR1)
2D41XXXX	Write storage protect bit in CSL at
	EA (Addr +XR1)
2E40XXXX	Clear storage protect bit in CSL at
	EA (Addr +XR2)
2E41XXXX	Write storage protect bit in CSL at
	EA (Addr +XR2)
2F40XXXX	Clear storage protect bit in CSL at
	EA (Addr +XR3)
2F41XXXX	Write storage protect bit in CSL at
	EA (Addr +XR3)

Two-Word Instruction, Indirect Addressing

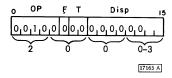
2CC0XXXX Clear storage protect bit in CSL at EA (V in CSL at Addr)

2CC1XXXX Write storage protect bit in CSL at EA (V in CSL at Addr) 2DC0XXXX Clear storage protect bit in CSL at EA (V in CSL at "Addr +XR1") 2DC1XXXX Write storage protect bit in CSL at EA (V in CSL at "Addr +XR1") 2EC0XXXX Clear storage protect bit in CSL at EA (V in CSL at "Addr +XR2") 2EC1XXXX Write storage protect bit in CSL at EA (V in CSL at "Addr +XR2") 2FC0XXXX Clear storage protect bit in CSL at EA (V in CSL at "Addr +XR3") 2FC1XXXX Write storage protect bit in CSL at EA (V in CSL at "Addr +XR3")

Label	Operation	F	Т	Г	
21 25	27 30	32	33	L	35 40 45
	S,T,S,			Γ	H.E.R.E.
1 1		П			
					30136

In the preceding example the status of the Carry and Overflow indicators is stored in position 14 and 15, respectively, of the word located at address HERE. A 1-bit is stored if the indicator is on; a 0-bit is stored if the indicator is off.

LOAD STATUS (LDS)



Description: This instruction applies to the single word format only. The Carry and Overflow indicators are loaded with the status of the bits in positions 14 (Carry) and 15 (Overflow) of the instruction. Normally this status was stored into this instruction by a previous Store Status instruction. Core storage remains unchanged. A one bit causes an indicator ON condition and a zero bit an indicator OFF condition.

<u>Indicators</u>: The Carry and Overflow indicators are set according to the bits at positions 14 and 15.

Hexadecimal Representation

One-Word Instruction (only)

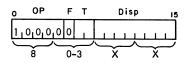
2000	Set CARRY and OVERFLOW
	indicators OFF
2001	Set OVERFLOW ON and
	CARRY OFF
2002	Set OVERFLOW OFF and
	CARRY ON
2003	Set CARRY and OVERFLOW
	indicator ON

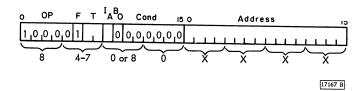
Label		Oper	ation	F	т										
21	25	27	30	32	33		35		40			45			
H,E,R,E	_	L,D,	s _.					1_	 	 	 	_			
				1		1	1						3	013	7

In the preceding example the status of the Carry and Overflow indicators is set according to bits 14 and 15 of the instruction. These bits are usually determined by a previous Store Status.

ARITHMETIC INSTRUCTIONS

ADD (A)





Description: The contents of the core storage location specified by the instruction are added to the contents of the accumulator. Two's complement arithmetic is used; that is, both negative operands and sums are in two's complement form. Core storage remains unchanged. See Appendix C for details of "data addition."

Indicators: The Overflow indicator is turned ON if the magnitude of the sum is too large to be represented in the Accumulator; that is, greater than $+2^{15}-1$ or less than -2^{15} (this is detected by a resultant carry out of one and only one of the two high-order bit positions of the accumulator). If overflow was previously ON, it is not changed. (Overflow can be reset by testing, or by a Load Status or Store Status instruction. See Branch or Skip on Condition instruction.) The Carry indicator is set by a carry out of the high-order bit position of the accumulator.

Hexadecimal Representation

One-Word Instruction

80XX	Add contents of CSL at EA (I+DISP)
81XX	to A Add contents of CSL at EA (XR1
82XX	+DISP) to A Add contents of CSL at EA (XR2
83XX	+DISP) to A Add contents of CSL at EA (XR3 +DISP) to A

Two-Word Instruction, Direct Addressing

8400XXXX	Add contents of CSL at EA (Addr)
8500XXXX	to A (See example.) Add contents of CSL at EA (Addr+XR1) to A

8600XXXX Add contents of CSL at EA

(Addr+XR2) to A

8700XXXX Add contents of CSL at EA

(Addr+XR3) to A

Two-Word Instruction, Indirect Addressing

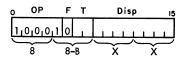
8480XXXX	Add contents of CSL at EA (V in
	CSL at Addr) to A
8580XXXX	Add contents of CSL at EA (V in
	CSL at "Addr+XR1") to A
8680XXXX	Add contents of CSL at EA (V in
	CSL at "Addr+XR2") to A
8780XXXX	Add contents of CSI at EA (X) :-

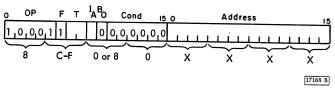
XXX Add contents of CSL at EA (V in CSL at "Addr+XR3") to A

Lai	bel	Oper	ation	F	т			
21	25	27	30	32	33	35	40	45
		A,		L		SUI	1	
ı	ı	i	1	1	ı	1		
								30138

In the preceding example the contents of SUM is added to the accumulator.

DOUBLE ADD (AD)





Description: The contents of the core storage location specified by the instruction and the next higher addressed location are added to the contents of the Accumulator (A) and its extension (Q). This provides double precision addition where the Accumulator and its extension are considered as one 32 bit Accumulator. The sum replaces the contents of A and Q. Core storage remains unchanged.

The effective address formed by the instruction must be an even address for correct operation. If the effective address is odd, the contents of the location are added to both the Accumulator and its extension, and may be added incorrectly into the Accumulator.

Indicators: When the instruction is completed, the Carry indicator represents the results of this instruction – not previous instructions. The Carry indicator

0

is set ON by detection of a Carry out of the high-order position of the Accumulator.

The Overflow indicator is turned ON by this instruction if the magnitude of the sum is greater than $+2^{31}-1$ or less then -2^{31} . If this indicator was ON before the instruction, no change occurs. If OFF, it is turned ON when the magnitude of the number is too large to be represented (this is detected by a carry out of one and only one of the two high-order bits of the Accumulator).

Hexadecimal Representation

One-Word Instruction

88XX	Add contents of CSL at EA
	(I+DISP) and EA+1 to A and Q
89XX	Add contents of CSL at EA (XR1
	+DISP) and EA+1 to A and Q
8AXX	Add contents of CSL at EA (XR2
	+DISP) and EA+1 to A and ${f Q}$
8BXX	Add contents of CSL at EA (XR3
	+DISP) and EA+1 to A and Q

Two-Word Instruction, Direct Addressing

8C00XXXX	Add contents of CSL at EA (Addr)
	and EA+1 to A and Q
8D00XXXX	Add contents of CSL at EA
	(Addr+XR1) and EA+1 to A and Q
8E00XXXX	Add contents of CSL at EA
	(Addr+XR2) and EA+1 to A and Q
8F00XXXX	Add contents of CSL at EA
	(Addr+XR3) and EA+1 to A and Q

Two-Word Instruction, Indirect Addressing

8C80XXXX	Add contents of CSL at EA (V in
	CSL at Addr) and EA+1 to A and Q
8D80XXXX	Add contents of CSL at EA (V in
	CSL at "Addr+XR1") and EA+1 to
	A and Q
8E80XXXX	Add contents of CSL at EA (V in
	CSL at "Addr+XR2") and EA+1 to
	A and Q (See example.)
8F80XXXX	Add contents of CSL at EA (V in
	CSL at "Addr+XR3") and EA+1 to

Labe	ı		Opero	tion		F	т				
21	25		27	30	<u> </u>	32	33	L	35	40	45
			A.D.	1		I	2		SUM		
		_							1		
			CCI	. 11					'D O!! \		T

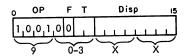
Note: EA (V in CSL at "SUM + XR2") must be even

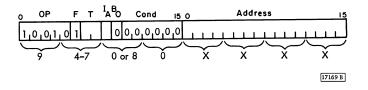
A and Q

30139 I

In the preceding example the address of SUM is added to the value in index register 2 to obtain the storage location containing the effective address. The contents of EA (EA must be an even address) and EA \pm 1 are treated as a single 32-bit word and are added to the Accumulator and extension.

SUBTRACT (S)





Description: The contents of the core storage location specified by the instruction are subtracted from the contents of the Accumulator. The result replaces the contents of the Accumulator. Two's complement arithmetic is used; that is, both negative operands and differences are in two's complement form. Core storage remains unchanged.

Indicators: The Overflow indicator is turned ON if the magnitude of the difference is too large to be represented in the Accumulator; that is, greater than $+2^{15}-1$ or less than -2^{15} . If Overflow was previously ON, it is not changed. (Overflow can be reset by testing or a Load or Store Status instruction. See Branch or Skip on Condition Instruction.) This is detected by a borrow from one and only one of the two high-order bit positions of the accumulator. The Carry indicator is set by a borrow from the high-order position.

Hexadecimal Representation

One-Word Instruction

90XX	Subtract contents of CSL at EA
	(I+DISP) from A
91XX	Subtract contents of CSL at EA
	(XR1+DISP) from A
92XX	Subtract contents of CSL at EA
	(XR2+DISP) from A
93XX	Subtract contents of CSL at EA
	(XR3+DISP) from A

Two-Word Instruction, Direct Addressing

9400XXXX Subtract contents of CSL at EA (Addr) from A (See example.)

9500XXXX Subtract contents of CSL at EA (Addr+XR1) from A
9600XXXX Subtract contents of CSL at EA (Addr+XR2) from A
9700XXXX Subtract contents of CSL at EA (Addr+XR3) from A

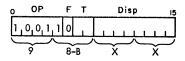
Two-Word Instruction, Indirect Addressing

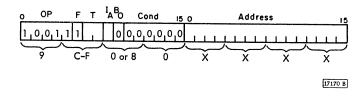
9480XXXX	Subtract contents of CSL at EA
	(V in CSL at Addr) from A
9580XXXX	Subtract contents of CSL at EA
	(V in CSL at "Addr+XR1") from A
9680XXXX	Subtract contents of CSL at EA
	(V in CSL at "Addr+XR2") from A
9780XXXX	Subtract contents of CSL at EA
	(V in CSL at "Addr+XR3") from A

	Label	Operation		F	Т		
21	25	27 30	L	32	33	35 40	45
		S, , ,		L		TIOTAL.	
							30140

In the preceding example the contents of TOTAL is subtracted from the Accumulator.

DOUBLE SUBTRACT (SD)





Description: The contents of the core storage location specified by the instruction and the next higher Core Storage location are subtracted arithmetically from the contents of the Accumulator (A) and its extension (Q). This provides double precision subtraction where the Accumulator and its extension are considered as one 32-bit accumulator. The difference replaces the contents of A and Q. Core storage remains unchanged. The effective address formed by the instruction must be an even address for correct operation. If the effective address is odd, the contents of that location are subtracted from both the Accumulator and its extension, and may be incorrect in the Accumulator.

Indicators: The Overflow indicator is turned ON if the magnitude of the difference is too large to be represented in the Accumulator (A) and its extension (Q), or more specifically, greater than $+2^{31} - 1$ or less than -2^{31} . This is detected by a borrow from one and only one of the two high-order bit positions of the Accumulator. If Overflow was previously ON, it is not changed. (Overflow can be reset by testing or by a Load or Store Status instruction.) See Branch or Skip on Condition instruction.) The Carry indicator is set by a borrow from the high-order position.

Hexadecimal Representation

One-Word Instruction

98XX	Subtract contents of CSL at EA
	(I+DISP) and EA+1 from A and Q
99XX	Subtract contents of CSL at EA
	(XR1+DISP) and EA+1 from A and Q
9AXX	Subtract contents of CSL at EA
	(XR2+DISP) and EA+1 from A and Q
9BXX	Subtract contents of CSL at EA
	(XR3+DISP) and EA+1 from A and Q

Two-Word Instruction, Direct Addressing

9C00XXXX	Subtract contents of CSL at EA
	(Addr) and EA+1 from A and Q (See
	example.)
9D00XXXX	Subtract contents of CSL at EA
	(Addr+XR1) and EA+1 from A and Q
9E00XXXX	Subtract contents of CSL at EA
	(Addr+XR2) and EA+1 from A and Q
9F00XXXX	Subtract contents of CSL at EA
	(Addr+XR3) and EA+1 from A and Q

Two-Word Instruction, Indirect Addressing

9C80XXXX	Subtract contents of CSL at EA (V in CSL at Addr) and EA+1 from
	A and Q
9D80XXXX	Subtract contents of CSL at EA
	(V in CSL at "Addr+XR1") and EA+1
	from A and Q
9E80XXXX	Subtract contents of CSL at EA
	(V in CSL at "Addr+XR2") and EA+1
	from A and Q
9F80XXXX	Subtract contents of CSL at EA
	(V in CSL at "Addr+XR3") and EA+1
	from A and Q

L	abel	Operation	Τ	F	т	Г			
21	25	27 3	0	32	33	L	35	40	45
		 S,D,	L	L			T	,O,T,A,L, ,	

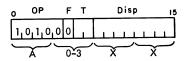
Note: Total must be an even address.

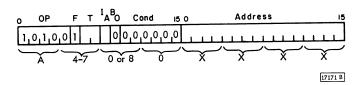
30141A

In the preceding example TOTAL and TOTAL + 1 are subtracted from the Accumulator and extension.

TOTAL must be an even address.

MULTIPLY (M)





Description: The contents of the core storage location specified by the instruction (multiplicand) are multiplied algebraically by the contents of the Accumulator (multiplier). The 32-bit product replaces the contents of the Accumulator (A) and its extension (Q). The most significant bits of the product are in the Accumulator. Core storage remains unchanged. The product is in the double precision format.

<u>Indicators:</u> Neither the Overflow nor the Carry indicators are changed.

Programming Note: The largest product that can be developed is 2^{30} . This occurs when the multiplier and multiplicand are both the largest negative numbers, -2^{15} .

Hexadecimal Representation

One-Word Instruction

A0XX	Multiply contents of CSL at EA
	(I+DISP) by A
A1XX	Multiply contents of CSL at EA
	(XR1+DISP) by A
A2XX	Multiply contents of CSL at EA
	(XR2+DISP) by A
A3XX	Multiply contents of CSL at EA
	(XR3+DISP) by A

Two-Word Instruction, Direct Addressing

A400XXXX	Multiply contents of CSL at EA
	(Addr) by A (See example.)
A500XXXX	Multiply contents of CSL at EA
	(Addr+XR1) by A

A600XXXX Multiply contents of CSL at EA

(Addr+XR2) by A

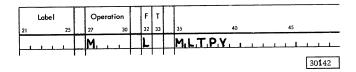
A700XXXX Multiply contents of CSL at EA

(Addr+XR3) by A

Two-Word Instruction, Indirect Addressing

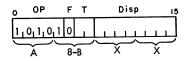
A480XXXX	Multiply contents of CSL at EA
	(V in CSL at Addr) by A
A580XXXX	Multiply contents of CSL at EA
	(V in CSL at "Addr+XR1") by A
A680XXXX	Multiply contents of CSL at EA
	(V in CSL at "Addr+XR2") by A
A780XXXX	Multiply contents of CSL at EA

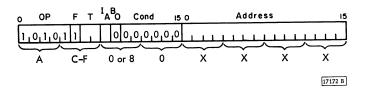
(V in CSL at "Addr+XR3") by A



In the preceding example the contents of MLTPY is multiplied by the contents of the Accumulator. The resultant product is 32 bits with the low-order bit in position 15 of the extension.

DIVIDE (D)





Description: The contents of the Accumulator and its extension (a 32-bit double precision word) are divided by the contents of the core storage location specified by the instruction. The quotient and remainder replace the contents of the Accumulator and the Accumulator extension, respectively. The "sign" of the remainder is the same as the dividend.

The largest dividend that can correctly be operated upon is $2^{30} + 2^{15} - 1$ if divided by the largest negative divisor (-2¹⁵).

<u>Indicators:</u> The Overflow indicator is turned ON when division by zero is attempted or when the quotient overflow condition exists. A quotient overflow occurs when the factors are such that the quotient would exceed the range of -2^{15} to $+2^{15}$ - 1. An overflow causes the accumulator and its extension (Q) to be left in an undefined state. Divide by zero leaves the Accumulator and its extension unchanged.

Hexadecimal Representation

One-Word Instruction

A8XX	Divide A and Q by contents of CSL
	at EA (I+DISP) (See example.)
A9XX	Divide A and Q by contents of CSL
	at EA (XR1+DISP)
AAXX	Divide A and Q by contents of CSL
	at EA (XR2+DISP)
ABXX	Divide A and Q by contents of CSL
	at EA (XR3+DISP)

Two-Word Instruction, Direct Addressing

AC00XXXX	Divide A and Q by contents of CSL
	at EA (Addr)
AD00XXXX	Divide A and Q by contents of CSL
	at EA (Addr+XR1)
AE00XXXX	Divide A and Q by contents of CSL
	at EA (Addr+XR2)
AF00XXXX	Divide A and Q by contents of CSL
	at EA (Addr+XR3)

Two-Word Instruction, Indirect Addressing

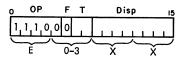
AC80XXXX	Divide A and Q by contents of CSL
	at EA (V in CSL at Addr)
AD80XXXX	Divide A and Q by contents of CSL
	at EA (V in CSL at "Addr+XR1")
AE80XXXX	Divide A and Q by contents of CSL
	at EA (V in CSL at "Addr+XR2")
AF80XXXX	Divide A and Q by contents of CSL
	at EA (V in CSL at "Addr+XR3")

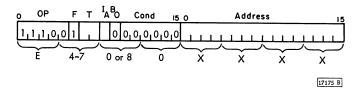
Label		Operation		F	т				
21 25		27 30		32	33	L	35	40	45
		D					*, +,6,		
	l		1			ŀ			
									201424

The contents of the Accumulator and extension are considered as a 32-bit dividend; therefore, it is generally necessary to shift the Accumulator right 16 places before dividing. In the preceding example the Accumulator and extension are divided by the contents of the EA which is determined by adding the displacement (6) to the I-register. The quotient replaces the Accumulator and the remainder is in the extension.

Note: The *+6 is an 1800 Assembler Language notation to indicate a displacement of 6 from the location following this instruction (I-register).

LOGICAL AND (AND)





<u>Description</u>: The contents of the core storage location specified by the instruction are ANDed bit by bit with the contents of the Accumulator. The following table defines the AND operation.

AND				
Storage	1	1	0	0
Accum	1	0	1	0
Result	1	0	0	0
			П	7176

The result replaces the contents of the Accumulator. Core storage remains unchanged.

<u>Indicators:</u> The Carry and Overflow indicators are not changed by this operation.

Hexadecimal Representation

One-Word Instruction

E0XX	AND contents of CSL at EA (I+DISP) with A
E1XX	AND contents of CSL at EA (XR1 +DISP) with A

E2XX

AND contents of CSL at EA

(XR2+DISP) with A

E3XX

AND contents of CSL at EA

(XR3+DISP) with A

Two-Word Instruction, Direct Addressing

E400XXXX

AND contents of CSL at EA (Addr)

with A (See example.)

E500XXXX

AND contents of CSL at EA

(Addr+XR1) with A

E600XXXX

AND contents of CSL at EA

(Addr+XR2) with A

E700XXXX

AND contents of CSL at EA

(Addr+XR3) with A

Two-Word Instruction, Indirect Addressing

E480XXXX AND contents of CSL at EA (V

in CSL at Addr) with A

E580XXXX

AND contents of CSL at EA (V

in CSL at "Addr+XR1") with A

E680XXXX

AND contents of CSL at EA (V in CSL at "Addr+XR2") with A

E780XXXX

AND contents of CSL at EA (V

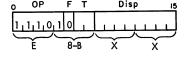
in CSL at "Addr+XR3") with A

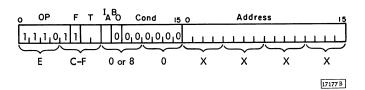
Lab	el	Орег	ation	F	Т			
21	25	27	30	32	33	3.	5 40	45
	1 1	A,N	D.	L		F	I ELD	
			I	1	1	1		20144

30144

In the preceding example the contents of FIELD is ANDed with the Accumulator. If a 1-bit appears in both words in corresponding positions, a 1-bit is placed in that position of the Accumulator, otherwise, a zero is placed there.

LOGICAL OR (OR)





Description: The contents of the core storage location specified by the instruction are ORed bit by bit with the contents of the Accumulator. The following table defines the OR operation:

OR				
Storage	1	1	0	0
Accum	1	0	1	0
Result	1	1	1	0
			[13	7178

The result replaces the contents of the Accumulator. Core storage remains unchanged.

Indicators: The Carry and Overflow indicators are not changed by this operation.

Hexadecimal Representation

One-Word Instruction

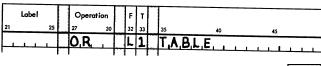
E8XX	OR contents of CSL at EA (I+DISP)
	with A
E9XX	OR contents of CSL at EA (XR1
	+DISP) with A
EAXX	OR contents of CSL at EA (XR2
	+DISP) with A
EBXX	OR contents of CSL at EA (XR3
	+DISP) with A

Two-Word Instruction, Direct Addressing

EC00XXXX	OR contents of CSL at EA (Addr)
	with A
ED00XXXX	OR contents of CSL at EA
	(Addr+XR1) with A (See example.)
EE00XXXX	OR contents of CSL at EA
	(Addr+XR2) with A
EF00XXXX	OR contents of CSL at EA
	(Addr+XR3) with A

Two-Word Instruction, Indirect Addressing

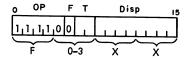
EC80XXXX	OR contents of CSL at EA (V in
	CSL at Addr) with A
ED80XXXX	OR contents of CSL at EA (V in
	CSL at "Addr+XR1") with A
EE80XXXX	OR contents of CSL at EA (V in
	CSL at "Addr+XR2") with A
EF80XXXX	OR contents of CSL at EA (V in
	CSL at "Addr+XR3") with A

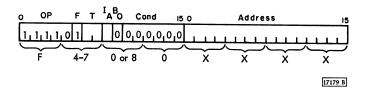


30145A

The contents of the effective address, determined by modifying the address of table by index register 1, is ORed into the Accumulator. A 1-bit appearing in either the Accumulator or the word at EA causes a 1-bit to be placed in the corresponding position of the Accumulator.

LOGICAL EXCLUSIVE OR (EOR)





<u>Description</u>: The contents of the core storage location specified by the instruction are Exclusive ORed bit by bit with the contents of the Accumulator. The following table defines the Exclusive OR operation:

Exclusive O	R			
Storage	1	7	0	0
Accum	1	0	1	0
Result	0	1	1	0
17180				

The result replaces the contents of the Accumulator. Core storage remains unchanged.

<u>Indicators</u>: The Carry and Overflow indicators are not changed by this operation.

Hexadecimal Representation

One-Word Instruction

F0XX	EOR contents of CSL at EA (I+DISP)
	with A
F1XX	EOR contents of CSL at EA
	(XR1+DISP) with A
F2XX	EOR contents of CSL at EA
	(XR2+DISP) with A
F3XX	EOR contents of CSL at EA
	(XR3+DISP) with A

Two-Word Instruction, Direct Addressing

F400XXXX	EOR contents of CSL at EA (Addr)
	with A
F500XXXX	EOR contents of CSL at EA
i	(Addr+XR1) with A
F600XXXX	EOR contents of CSL at EA
	(Addr+XR2) with A
F700XXXX	EOR contents of CSL at EA
	(Addr+XR3) with A

Two-Word Instruction, Indirect Addressing

F480XXXX	EOR contents of CSL at EA (V in
	CSL at Addr) with A (See example.)
F580XXXX	EOR contents of CSL at EA (V in
	CSL at "Addr+XR1") with A
F680XXXX	EOR contents of CSL at EA (V in
	CSL at "Addr+XR2") with A
F780XXXX	EOR contents of CSL at EA (V in
	CSL at "Addr+XR3") with A

Label	T	Operation	F	7	T			
21 2	5	27 30	32	33	ı	35	40	45
	L	E.O.R.	I		Τ	A,R,E	Α	
1	1	1	1	1	Ţ			
								30146

In the preceding example the EA is determined by the contents of AREA. The contents of the EA is exclusively ORed into the Accumulator. That is, Accumulator bits which are equal to their corresponding bits at EA are set to zero, otherwise to 1.

SHIFT INSTRUCTIONS

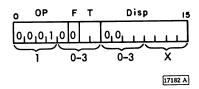
All shift instructions are single word format only (F=0). They are divided into subclasses as defined by bit positions 8 and 9. Those that have their shift count defined by the TAG bits shift as shown below:

Table 3. Shift Count

Tag	Shift Count Determined By:
00	Low-Order 6 Bits of Disp
01	Low-Order 6 Bits of XR1
10	Low-Order 6 Bits of XR2
11	Low-Order 6 Bits of XR3
	17 181

If the shift count is zero, the instruction performs a NO-OP.

SHIFT LEFT LOGICAL A (SLA)



Description: The Accumulator (A) is shifted left the number of spaces specified by the Shift Count (Table 3). Vacated bit positions are set to zero. Bits leaving the high-order (bit 0 of A) position are shifted into the Carry indicator. (See Indicators below.) The Extention (Q) is not affected. Note that bit positions 8 and 9 must be 00.

Indicators: The Carry indicator is turned on for each one and off for each zero shifted left from the high-order position of A. The Overflow indicator is unaffected.

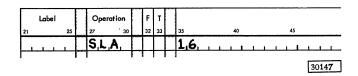
Hexadecimal Representation

One-Word Instructions (Only)

10*X	Contents of A shift left the number
	of shift counts in DISP (See exam-
	ple.)
1100	Contents of A shift left the number
	of shift counts in XR1
1200	Contents of A shift left the number
	of shift counts in XR2

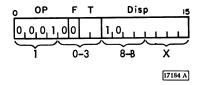
1300 Contents of A shift left the number of shift counts in XR3

*The third from the high order position can be 0, 1, 2, or 3, depending on the value of the shift count.



In the preceding example the Accumulator is shifted left 16 places. The vacated positions are set to zero. In this particular case the Accumulator is cleared (set to all zeros).

SHIFT LEFT LOGICAL A & Q (SLT)



Description: The accumulator (A) and its extension (Q) are shifted left as a 32-bit double precision register. Vacated bit positions are set to zero. Bits leaving the high-order position (bit position 0 of A) are shifted into the Carry indicator.

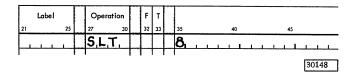
<u>Indicators</u>: The Carry indicator is turned on for each one and off for each zero shifted left from high-order position of A. The Overflow indicator is unaffected.

Hexadecimal Representation

One-Word Instructions (Only)

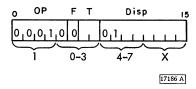
10*X	Contents of A and Q shift left the
	number of shift counts in DISP (See
	example.)
1180	Contents of A and Q shift left the
	number of shift counts in XR1
1280	Contents of A and Q shift left the
	number of shift counts in XR2
1380	Contents of A and Q shift left the
	number of shift counts in XR3

*The third from the high-order position can be 8, 9, A, or B depending on the value of the shift count.



In the preceding example both the Accumulator and extension are shifted left 8 places as one 32-bit register.

SHIFT LEFT AND COUNT A (SLCA)



<u>Description</u>: A TAG of 00 causes this instruction to be performed as a Shift Left A instruction. A TAG specifying one of the indéx registers causes the shift count to be transferred from the low-order six bits of the specified register to the shift counter. This count is decremented by one for each position that the contents of the Accumulator (A) are shifted to the left. Vacated bit positions are set to zero.

The shift terminates either when an attempt is made to shift a one from the high-order position of A (the "1" remains in the high-order position after the instruction has terminated) or when the shift count has been decremented to zero. The decremented count is then loaded back into the six low-order bit positions of the index register (bits 10-15) and bits 8 and 9 are reset to zero. Bit positions 0-7 of the index register remain unchanged at completion of the instruction. If the shift count is initially zero or if the high-order position of the Accumulator (Bit 0) is initially a one bit, the instruction performs as a NO-OP.

<u>Indicators</u>: The Carry indicator will be OFF at the end of the operation if the shift is terminated by the detection of the count reaching zero. The Carry indicator will be ON at the end of the operation if the shift is terminated by the detection of a 1 in bit 0 of the Accumulator before the shift count reaches zero. For T=0 the Carry indicator is set as in Shift Left instruction. The Overflow indicator is unaffected.

SLCA Examples: For the four examples below, assume the Index Register was previously loaded by an LDX instruction. Only the low-order bit positions (10-15) of the Index Register (XR) are shown and only the high-order bit positions (0-5) of the Accumulator (A) are shown. Those bit positions containing an X can be zero or one.

Example Number 3 XR before SLCA 000011 000100 000101 000110 XR after SLCA 000000 000000 000001 000010 A before SLCA 00001X 00001X 00001X 00001X A after SLCA 01XXXX 1XXXXX 1XXXXX 1XXXXX Carry Indicator after SLCA OFF* OFF* ON** ON**

*If no one bits were contained in the field defined by the Index Register (Examples 1 and 2), the program can determine the value of Accumulator bit 0 only by testing the Accumulator sign. (Carry Indicator is OFF and the Index Register is zero.)

**If a one bit was contained in the field defined by the Index Register (Examples 3 and 4), the SLCA instruction was terminated when an attempt was made to shift the one out of the high-order position, leaving the Carry Indicator ON and the Index Register at a non-zero condition. (The one bit remains in the high-order position.)

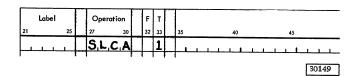
Hexadecimal Representation

One-Word Instructions (Only)

10*X	Contents of A shift left the number
	of shift counts in DISP
1140	**Contents of A shift left the number
	of shift counts in XR1 (See example.)
1240	**Contents of A shift left the number
	of shift counts in XR2
1340	**Contents of A shift left the number
	of shift counts in XR3

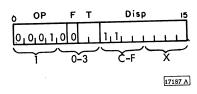
*The third from the high-order position can be 4, 5, 6, or 7, depending on the value of the shift count.

**These instructions are terminated either when an attempt is made to shift a one bit from the high-order position of the Accumulator (with a non-zero shift count remaining) or when the shift count has been decremented to zero.



In the preceding example index register 1 should be set to the number of bit positions to be shifted. As the Accumulator is shifted to the left, index register 1 is decremented by one each time a zero is shifted out. The first 1-bit in Accumulator position zero terminates the operation. By branching to a table indexed by register 1 it is possible to have a unique subroutine for each position of the Accumulator that could contain a 1-bit. This is quite helpful in determining device status and interrupt conditions.

SHIFT LEFT AND COUNT A & Q (SLC)



Description: This instruction is the same as the Shift Left and Count A except that both the Accumulator (A) and its Extension (Q) are shifted. Bit position 0 of Q is shifted into bit position 15 of A and vacated positions at the right of Q are set to zero.

<u>Indicators</u>: The Carry indicator will be OFF at the end of the operation if the shift is terminated by the detection of the count reaching zero. The Carry indicator will be ON at the end of the operation if the shift is terminated by the detection of a 1 in the bit zero position of the Accumulator before the shift count reaches zero. For T=0 the Carry indicator is set as in Shift Left instruction.

The Overflow indicator is unaffected.

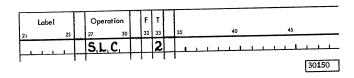
Hexadecimal Representation

One-Word Instructions (Only)

10*X	Contents of A and Q shift left the number of shift counts in DISP
11C0	**Contents of A and Q shift left the number of shift counts in XR1
12C0	**Contents of A and Q shift left the number of shift counts in XR2
13C0	(See example.) **Contents of A and Q shift left the number of shift counts in XR3

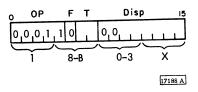
*The third from the high-order position can be C, D, E, or F, depending on the value of the shift count.

**These instructions are terminated either when an attempt is made to shift a one bit from the high-order position of the Accumulator (with a non-zero shift count remaining) or when the shift count has been decremented to zero.



In the preceding example both the Accumulator and extension are shifted left until a 1-bit appears in the high-order position of the Accumulator (or index register 2 is decremented to zero). Index register 2 is decremented by one each time a zero is shifted out of the Accumulator.

SHIFT RIGHT LOGICAL A (SRA)



Description: The Accumulator (A) is shifted right the number of places indicated by the Shift Count. Zeros are entered in all vacated spaces. The Extension (Q) is undisturbed. Low-order bits of A are lost.

<u>Indicators:</u> The Carry and Overflow indicators are not affected.

Hexadecimal Representation

One-Word Instructions (Only)

18*X	Contents of A shift right the number of shift counts in DISP (See exam-
	ple.)
1900	Contents of A shift right the number
	of shift counts in XR1
1A00	Contents of A shift right the number
	of shift counts in XR2
1B00	Contents of A shift right the number
	of shift counts in XR3

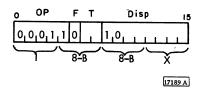
*The third from the high-order position can be 0, 1, 2, or 3, depending on the value of the shift count.

Label	Operation	F	т	Г			
21 25	27 30	32	33		35	40	45
	S,R,A,				3, ,	1 1 1 1 1	
1							20151

21 25 27 30 32 33 35	40	45
S,R,T,	1 1 1 1 1	1
		30152

In the preceding example the contents of the Accumulator is shifted right 3 places. The vacated positions of the Accumulator are set to zero, and the positions shifted out are lost.

SHIFT RIGHT A & Q (SRT)



Description: The Accumulator (A) and Extension (Q) are shifted right as a 32-bit double precision register. The value of the sign (bit position 0 of A) is entered in all vacated spaces. Low-order bits of Q are lost.

<u>Indicators</u>: The Carry and Overflow indicators are not changed.

Hexadecimal Representation

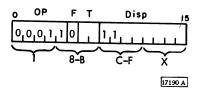
One-Word Instruction (Only)

18*X	Contents of A and Q shift right the number of shift counts in DISP (See example.)
1980	Contents of A and Q shift right the
	number of shift counts in XR1
1A80	Contents of A and Q shift right the
	number of shift counts in XR2
1B80	Contents of A and Q shift right the number of shift counts in XR3

^{*}The third from the high-order position can be 8, 9, A, or B, depending on the value of the shift count.

In the preceding example the Accumulator and extension are shifted to the right 6 places. The value of the sign bit is placed in all vacated positions of the Accumulator. The bits shifted out of the extension are lost.

ROTATE RIGHT A & Q (RTE)



Description: The Accumulator (A) and Extension (Q) are rotated to the right as a 32-bit double precision register the number of bit positions specified by the Shift Count. Bit position 15 of the Extension (Q) is linked to bit position 0 of the Accumulator (A) to form a continuous loop cycle shift so that the high-order positions of the Accumulator pick up the bits dropped from the low-order position of the Extension.

<u>Indicators</u>: The Carry and Overflow indicators are not changed.

Hexadecimal Representation

One-Word Instruction (Only)

18*X	Contents of A and Q rotate right the number of counts in DISP (See ex-
	ample.)
19C0	Contents of A and Q rotate right the
	number of counts in XR1
1AC0	Contents of A and Q rotate right the
	number of counts in XR2
1BC0	Contents of A and Q rotate right the
	number of counts in XR3

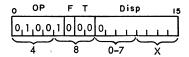
^{*}The third from the high-order position can be C, D, E, or F, depending on the value of the shift count.

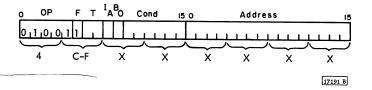
Label			Оре	ration	F	т	Ī.			
21	25		27	30	 32	33	L	35	40	45
	_		R,T	E,			L	1,0,		
		Γ	I		1	1	ľ	1		30153

In the preceding example the Accumulator and extension are rotated to the right 10 places, that is, the bits shifted out of the low-order of the extension are shifted into the high-order of the Accumulator.

BRANCH INSTRUCTIONS

BRANCH OR SKIP ON CONDITION (BSC or BOSC)





<u>Description:</u> There are six testable conditions associated with the Accumulator. These conditions may be tested by indicating the bit pattern in the DISPLACE-MENT of the instruction.

The six Accumulator conditions that can be tested are shown by bit position.

$\underline{\mathrm{Bit}}$	Condition
15	Overflow OFF
14	Carry OFF
13	Accumulator Even
12	Accumulator Plus (greater than zero)
11	Accumulator Negative
10	Accumulator Zero

When F=0, the instruction executed is a Skip on Condition when one or more of the conditions specified is true. This enables the program to skip over the next one word instruction. If none of the conditions specified are true, the next instruction in sequence is executed.

When F=1, the instruction executed is a Branch to the Effective Address (EA) when none of the condition(s) specified are true. If any one of the condition(s) specified in bit positions 10-15 is true, the next instruction in sequence is executed. Examples are shown in Figure 5.

The EA is calculated as follows:

$$F = 1 \quad IA = 0 \qquad T = 00 \qquad EA = ADDR$$

$$T = 01 \qquad EA = XR1 + ADDR$$

$$T = 10 \qquad EA = XR2 + ADDR$$

$$T = 11 \qquad EA = XR3 + ADDR$$

When the IA bit is equal to a one (IA = 1), this instruction enables the program to return to a mainline program from a program subroutine or interrupt routine. This is accomplished by making the EA of this instruction identical to the EA of a previously executed Branch and Store Instruction Register (BSI) instruction. The EA as calculated below is loaded into the Instruction Register.

*C means "Contents of"

Programming Note: When an interrupt request has been detected by a priority level, the program is directed to service the request by interrupting. During the servicing, all interrupt requests of equal or lower status are effectively constrained from interrupting while the servicing of the higher priority is in progress. However, if a request is detected for a higher priority level than is presently in progress, the program is immediately interrupted again. This is frequently called Nesting of Interrupts.

At the completion of servicing any level of interrupt, it is necessary to signal the priority hardware to reset the priority-status of the highest level that is on. This reset permits lower priority requests, that may have been temporarily constrained but recorded, to be accepted once again by the P-C. This is effected by making Bit 9 = 1 in the BSC instruction. A BSC instruction with Bit 9=1 is called a Branch Out of Interrupts (BOSC). This programmed recognition of waiting interrupts should not be confused with a normal subroutine linkage back to a mainline program in which Bit 9 should be set to zero.

The BSC is a conditional instruction. When Bit 9 = 1, the reset of the interrupt level occurs only if the Branch or Skip occurs. If the Branch or Skip does not occur, the interrupt level is not reset.

<u>Indicators</u>: The Overflow indicator is reset when <u>tested</u>. The Carry indicator is not reset by testing. The contents of the Accumulator are not changed by testing. If no conditions are specified, a Skip does not occur on the SKIP instruction (F = 0) or a branch does occur on the BRANCH instruction (F = 1).

Bit Positions: ACC Conditions:	10 Zero	11 Minus	12 Plus	13 Even	Skip (F = 0)	Branch (F=1)
	(1	1	1	0	Always	Never
	0	0	0	0	Never	Always
	0	0	1	0	Plus	Not Plus
Test	1	1	0	0	Not Plus	Plus
Conditions -	0	1	0	0	Minus	Not Minus
	1	0	1	0	Not Minus	Minus
Ī	1	0	0	0	Zero	Not Zero
	0	1	1	0	Not Zero	Zero
	0	0	0	1	Even	Odd
	0	0	1	1	Even or	Odd and
	l				Plus	Minus
	0	1	0	1	Even or	Odd and
					Minus	Plus

Notes: 1. ACC Zero is not a plus condition.

- Skip and Branch columns specify action or ACC condition required for Skip or Branch.
- 3. Skip on Odd condition, Carry ON, or Overflow ON are not possible.

Figure 5. BSC Examples

Hexadecimal Representation

One-Word Instruction

48*X

SKIP the next one-word instruction if ANY condition is sensed

*The third from the high-order position can be 0, 1, 2, or 3 (BSC) or 4, 5, 6, or 7 (BOSC), depending on which conditions are tested.

Two-Word Instruction, Direct Addressing

4C*XXXXX Branch to CSL at EA (Addr) on NO condition (See example.)

4D*XXXXX Branch to CSL at EA (Addr+XR1) on NO condition

4E*XXXXX Branch to CSL at EA (Addr+XR2) on NO condition

4F*XXXXX Branch to CSL at EA (Addr+XR3) on NO condition

*The third from the high-order position can be 0, 1, 2, or 3 (BSC) or 4, 5, 6, or 7 (BOSC). These hexadecimal values are determined by the conditions being tested.

Two-Word Instruction, Indirect Addressing

4C*XXXXX Branch to CSL at EA (V in CSL at Addr) on NO condition

4D*XXXXX Branch to CSL at EA (V in CSL at "Addr+XR1") on NO condition

4E*XXXXX Branch to CSL at EA (V in CSL at "Addr+XR2") on NO condition
4F*XXXXX Branch to CSL at EA (V in CSL at "Addr+XR3") on NO condition

*The third from the high-order position can be 8, 9, A, B (BSC) or C, D, E, or F (BOSC). These hexadecimal values are determined by the conditions being tested.

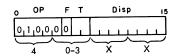


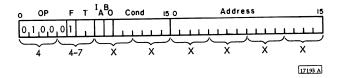
In the preceding example the program branches to THERE if the Accumulator is negative. Otherwise, the next sequential instruction is executed.



In the preceding example the program branches to the address stored at RETRN and resets the currently active interrupt level.

BRANCH AND STORE INSTRUCTION REGISTER (BSI)





<u>Description:</u> When F = 0 (one word format), the <u>contents of the Instruction Register</u> are stored in the core storage location specified by the effective

address. The stored address is that of the next instruction in the normal sequence. The Instruction Register is then set to the value of the effective address plus one, and program execution proceeds from that point.

For example, a BSI instruction located at core storage address 0500, with an effective address of 0550, would store the address 0501 at location 0550 and then branch to 0551. (See Figure 6.)

A BSC instruction with an IA bit of one and an ADDRESS of 0550 would be used to return from the subroutine.

When F=1 (two word instruction format), the above function is conditionally executed depending on the condition bits specified in the Displacement. These Accumulator condition bits are defined in the preceding BSC instruction. If <u>any one</u> of the conditions specified is true, the previously explained branch does <u>not</u> occur. Instead, the next instruction in sequence is performed. If <u>none</u> of the conditions are true, the Instruction Register is stored at the effective address (specified by the ADDRESS) and the branch is to EA + 1.

Internal, CE, and external level interrupts are suppressed for the first instruction following a BSI instruction. Therefore, the Mask Register (See Interrupt section) may be set without the possibility of an interrupt other than trace immediately following the BSI instruction.

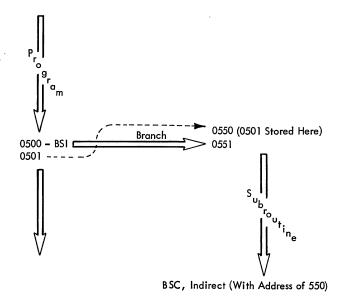


Figure 6. BSI Operation

Indicators: When F = 0, the status of the indicators is unchanged. When F = 1, the Overflow indicator is reset if tested.

Hexadecimal Representation

One-Word Instruction

40XX	Store next sequential address in
	CSL at EA (I+DISP) and Branch to
	EA+1
41XX .	Store next sequential address in
	CSL at EA (XR1+DISP) and Branch
	to EA+1
42XX	Store next sequential address in
	CSL at EA (XR2+DISP) and Branch
	to EA+1
43XX	Store next sequential address in
	CSL at EA (XR3+DISP) and Branch
	to EA+1

Two-Word Instruction, Direct Addressing

44*XXXXX	If NO condition is true, store next
	sequential address in CSL at EA
	(Addr) and Branch to EA+1
45*XXXXX	If NO condition is true, store next
	sequential address in CSL at EA
	(Addr+XR1) and Branch to EA+1
46*XXXXX	If NO condition is true, store next
	sequential address in CSL at EA
	(Addr+XR2) and Branch to EA+1
47*XXXXX	If NO condition is true, store next
	sequential address in CSL at EA
	(Addr+XR3) and Branch to EA+1

^{*}The third from the high-order position can be 0, 1, 2, or 3, depending on the conditions being tested.

Two-Word Instruction, Indirect Addressing

44*XXXXX

17194B

	(V in CSL at Addr) and Branch
	to EA+1 (See example.)
45*XXXXX	If NO condition is true, store next
	sequential address in CSL at EA
	(V in CSL at "Addr+XR1") and
	Branch to EA+1
46*XXXXX	If NO condition is true, store next
	sequential address in CSL at EA
	(V in CSL at "Addr+XR2") and
	Branch to EA+1

If NO condition is true, store next sequential address in CSL at EA

47*XXXXX

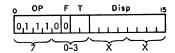
If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR3") and Branch to EA+1

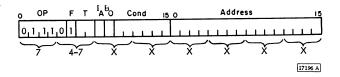
*The third from the high-order position can be 8, 9, A, or B, depending on the conditions being tested.

Label			Operation		F	T	Γ			
21	25		27 30	L	32	33	L	35	40	45
			B,S,I,		I			1,0	,0,8,0,	
		1		T	1	ı	ŀ	1		30156

In the preceding example the Instruction Address Register is stored at the effective address which is specified by the contents of storage location /0080. The program then branches to EA + 1. (Slash denotes hexadecimal.)

MODIFY INDEX AND SKIP (MDX)





Description: The Modify Index and Skip instruction has many uses. The specific operation and the registers involved depend upon the instruction format. An Index Register may be modified by a value; this value may be the expanded Displacement, the Address, or the contents of the core storage location specified by the Address. The Instruction Register or a core storage word may be modified by the expanded Displacement.

The Displacement is automatically expanded to a 16-bit value by duplicating bit position 8 (sign bit) in the left 8 positions.

In <u>no</u> case is the Accumulator (A) or its Extension (Q) modified.

If T is not zero, the Index register specified is modified. The Instruction Register is incremented an additional time to cause a skip whenever the Index Register specified is zero after the operation is complete or has changed sign during the operation. Therefore, the MDX instruction with T=non-zero should be followed by a one-word instruction.

If T is zero and the MDX instruction is short (F=0), the Instruction Register is modified by the contents of the Displacement. The Instruction Register is <u>not</u> incremented an additional time if the Instruction Register is zero after the operation is complete. Note that the Instruction Register has no sign as such, but is treated as a 16-bit logical value.

If T is zero and the MDX instruction is long (F=1), the core storage location specified by Address is modified by the expanded Displacement. The Instruction Register is incremented an additional time if the content of the specified location is zero after the operation is complete or has changed sign during the operation. Therefore the MDX instruction with T=zero and F = one should be followed by a oneword instruction.

The MDX instruction 70FF can be used as a dynamic wait instruction. This instruction will cause the instruction register to be modified so that this same instruction will be repeated continuously, allowing interrupts to be serviced and returning to the MDX instruction (dynamic wait). Unless an interrupt subroutine alters the stored return address, the program will return to the MDX instruction at the end of the interrupt subroutine. An exit from the dynamic wait condition can be made manually by the following procedure.

- 1. Change the Mode switch to Display.
- 2. Press console Start.
- 3. Change Mode switch to Run.
- 4. Press console Start.
- 5. The program starts with the instruction following the MDX instruction.

<u>Indicators</u>: The Carry and Overflow indicators are not changed by this instruction.

Hexadecimal Representation

One-Word Instructions

70XX	ADD Expanded DISP to I (no skip
	can occur)
71XX	ADD Expanded DISP to XR1
72XX	ADD Expanded DISP to XR2
73XX	ADD Expanded DISP to XR3
	(See example.)

Two-Word Instruction, Direct

74XXXXXX Add Expanded Positive DISP to CSL at Addr (Add to memory)

7500XXXX Add Addr to XR1 7600XXXX Add Addr to XR2 7700XXXX Add Addr to XR3

Two-Word Instruction, Indirect

7780XXXX

74XXXXX Add Expanded negative DISP to CSL at Addr (Add to Memory)

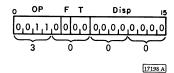
A tag must be specified.
7580XXXX Add V in CSL at Addr to XR1
7680XXXX Add V in CSL at Addr to XR2

Add V in CSL at Addr to XR3

Label Operation F T T 27 30 35 40 45 45 30157

In the preceding example index register 3 is incremented by 6. If index register 3 changes sign the I-register is incremented by one.

WAIT (WAIT)



Description: This instruction is a one word format instruction only. The P-C stops in a wait condition. It can be restarted manually or by detection of an interrupt. Following completion of an interrupt subroutine, the instruction immediately following the Wait instruction is executed if the Branch Out of Interrupt (BOSC) is the normal indirect subroutine linkage. Data channel or Timer operations continue during the wait condition.

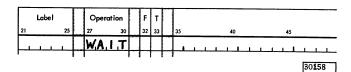
Another method of accomplishing the WAIT function is described under the heading $\underline{\text{Modify Index}}$ And Skip (MDX).

<u>Indicators</u>: The Carry and Overflow indicators are not changed by this instruction.

Hexadecimal Representation

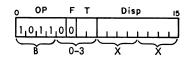
One-Word Instruction (only)

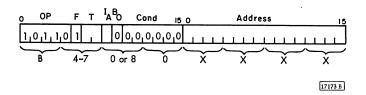
3000 WAIT until manual start or until interrupted.



In the preceding example the P-C stops. The P-C is automatically restarted if an interrupt request is detected. It may also be restarted by pressing the console start switch.

COMPARE (CMP)





<u>Description</u>: The contents of the Accumulator (A) are algebraically compared against the contents of the word at the effective address, and the Instruction Register (I) is modified according to the result of the comparison as shown below:

if A > C(EA) then I = Iif A < C(EA) then I = I + 1If A = C(EA) then I = I + 2

The contents of A and Q and core storage are unchanged at the end of the instruction execution.

<u>Indicators</u>: The Overflow indicator is unaffected by this instruction. The Carry indicator may be altered.

Hexadecimal Representation

One-Word Instruction

B0XX	Compare A with contents of CSL
	at EA (I+DISP) (See example.)
B1XX	Compare A with contents of CSL
	at EA (XR1+DISP)
B2XX	Compare A with contents of CSL
	at EA (XR2+DISP)
B3XX	Compare A with contents of CSL
	at EA (XR3+DISP)

Two-Word Instruction, Direct Addressing

B400XXXX Compare A with contents of CSL at EA (Addr)

B500XXXX $\;$ Compare A with contents of CSL

at EA (Addr+XR1)

B600XXXX Compare A with contents of CSL

at EA (Addr+XR2)

B700XXXX Compare A with contents of CSL

at EA (Addr+XR3)

Two-Word Instruction, Indirect Addressing

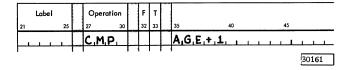
B480XXXX Compare A with contents of CSL at EA (V in CSL at Addr)

B580XXXX Compare A with contents of CSL at EA (V in CSL at "Addr+XR1")

B680XXXX Compare A with contents of CSL

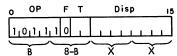
at EA (V in CSL at "Addr+XR2") B780XXXX Compare A with contents of CSL

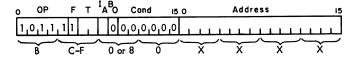
at EA (V in CSL at "Addr+XR3")



In the preceding example, AGE + 1, which must be within 127 (or -128) positions of the instruction (short instruction format), is algebraically compared against the contents of the accumulator. If the accumulator is greater, the next sequential instruction is executed; if the accumulator is less, one word is skipped and I+1 is executed; and if they are equal, two words are skipped and I+2 is executed.

DOUBLE COMPARE (DCM)





Description: The contents of the Accumulator (A) and its Extension (Q) are compared against the contents of the effective address (EA must be an even address) and the effective address plus one (odd). The Instruction Register (I) is modified as follows:

if A, Q > C(EA), C(EA + 1), then I = Iif A, Q < C(EA), C(EA + 1), then I = I + 1if A, Q = C(EA), C(EA + 1), then I = I + 2

Indicators: The Overflow indicator is unaffected by this instruction. The Carry indicator may be altered.

Hexadecimal Representation

One-Word Instruction

B8XX	Compare A and Q with contents of
	CSL at EA (I+DISP) and EA+1
B9XX	Compare A and Q with contents of
	CSL at EA (XR1+DISP) and EA+1
BAXX	Compare A and Q with contents of
	CSL at EA (XR2+DISP) and EA+1
BBXX	Compare A and Q with contents of
	CSL at EA (XR3+DISP) and EA+1

Two-Word Instruction, Direct Addressing

BC00XXXX	Compare A and Q with contents of CSL at EA (Addr) and EA+1 (See example.)
BD00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR1) and EA+1
BE00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR2) and EA+1
BF00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR3) and EA+1

Two-Word Instruction, Indirect Addressing

BC80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at Addr)
DD 00 TETELL	and EA+1
BD80XXXX	Compare A and Q with contents of
	CSL at EA (V in CSL at "Addr
	+XR1'') and EA+1
BE80XXXX	Compare A and Q with contents
	of CSL at EA (V in CSL at
	"Addr+XR2") and EA+1
BF80XXXX	Compare A and Q with contents
	of CSL at EA (V in CSL at
	"Addr+XR3") and EA+1

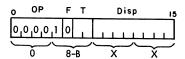
Labe	ı	Operation	F	т	Γ	Γ		
21	25	27 30	32	33	L	35	40	45
		D,C,M,	L			T,	0,T,A,L, , ,	

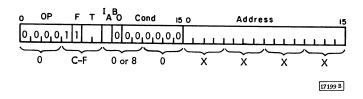
Note: Total must be an even address.

30160A

In the preceding example, TOTAL, which must be an even address, and TOTAL + 1 are algebraically compared against the accumulator and extension. If A and Q are greater, the next sequential instruction is executed; if A and Q are less, one word is skipped and I+1 is executed; and if they are equal, two words are skipped and I+2 is executed.

EXECUTE I/O (XIO)





Description: This instruction is used for all I/O operations; it may be either one or two words in length, as specified by the F-bit. In the two-word instruction, the Address is either a direct or indirect address, as specified by the IA bit. For proper operation, the Effective Address must be an even address. The Effective Address is used to select a two-word I/O Control Command (IOCC) from storage.

Internal, Trace, CE, and External interrupts are suppressed for the first instruction following an XIO instruction. Therefore, the mask register (See Interrupt section) may be set without the possibility of an interrupt.

Hexadecimal Representation

One-Word Instruction

08XX Execute IOCC in CSL at EA (I+DISP) and

09XX Execute IOCC in CSL at EA (XR1+DISP) and EA+1

0AXX Execute IOCC in CSL at EA (XR2+DISP) and EA+1

0BXX Execute IOCC in CSL at EA (XR3+DISP) and EA+1

Two-Word Instruction, Direct Addressing

OC00XXXX Execute IOCC in CSL at EA (Addr) and EA+1 (See example.)

0D00XXXX Execute IOCC in CSL at EA (Addr+XR1) and EA+1

0E00XXXX Execute IOCC in CSL at EA (Addr+XR2) and EA+1

0F00XXXX Execute IOCC in CSL at EA (Addr+XR3) and EA+1

Two-Word Instruction, Indirect Addressing

0C80XXXX Execute IOCC in CSL at EA (V in CSL at Addr) and EA+1

0D80XXXX Execute IOCC in CSL at EA (V in CSL at "Addr+XR1") and EA+1

0E80XXXX Execute IOCC in CSL at EA (V in CSL at "Addr+XR2") and EA+1

0F80XXXX Execute IOCC in CSL at EA (V in CSL at "Addr+XR3") and EA+1

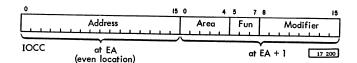
Label Operation F T | 21 25 27 30 32 33 35 40 45

Note: IOCC must be an even address.

30159A

In the preceding example, the I/O control command located at IOCC is executed.

The IOCC specifies the I/O operation, I/O device, and core storage address. The format of the two-word IOCC follows, with an explanation of the assigned fields:



Area

This 5-bit field specifies a unique segment of I/O which may be a single device (1442 Card Read-Punch, 1443 Printer, etc.) or a group of several units (mag-

netic tape drives, serial I/O units, contact sense units, etc.). (See Appendix D.)

Area 00000 is used to address such devices as the Console and the Interrupt Mask Register. (See "Area Code Zero" following XIO Data Flow.)

Function

The primary I/O functions are specified by the 3-bit function code of the IOCC:

- 000 This code is used to remove an I/O device from on-line status and place it in CE mode. It can also be used to restore the on-line status and remove the I/O device from CE mode.
- 001 Write
 This code is used to transfer a single word
 from storage to an I/O unit. The address of
 the storage location is provided by the Address
 field of the I/O Control Command.
- 010 Read

 This code is used to transfer a single word
 from an I/O unit to storage. The address of
 the storage location is provided by the Address
 field of the I/O Control Command.
- 011 Sense Interrupt Level
 This code is used to load the Accumulator
 with the Interrupt Level Status Word (ILSW)
 for the highest interrupt level pending at the
 time it is issued. This command is common
 to all I/O devices; therefore, no device code
 is needed. (See "Interrupt" section.)
- 100 Control

 This code causes the selected device to interpret the Address word or modifier of the IOCC as a specific control action. (See "Area Code Zero" following XIO Data Flow.)
- 101 Initialize Write

 This code initiates a WRITE operation on a device or unit which will subsequently make data transfers from storage via a Data Channel.
- 110 Initialize Read

 This code initiates a READ operation from a device or unit which will subsequently make data transfers to storage via a Data Channel.
- 111 Sense Device
 This code causes the selected device to make
 its current status available in the Accumulator
 as the Device Status Word or Process Interrupt Status Word (PISW).

If Area 00000 is specified, the Console status or Interval Timer status may be brought into the Accumulator as specified by a unit address code in the Modifier field.

Programming Note: The current contents of the Accumulator are destroyed by the execution of Sense Interrupt Level, Sense Device, Initialize Read, Initialize Write, Read, or Write. Therefore, it is the programmer's responsibility to save the Accumulator contents if necessary.

Modifier

This 8-bit field provides additional detail for either Function or Area. For example, if the Area specifies a Disk Storage Drive, and if the Function specifies Control (100) then a particular modifier code specifies the direction of the Seek operation. In this case, the Modifier serves to extend the Function.

If, however, the Area specifies a group of serial I/O devices, and if the Function specifies Write (001), then the particular unit address is specified by the Modifier. (See Appendix D.)

Address

The meaning prescribed for this 16-bit field is dependent upon the Function specified by this I/O Control Command:

- If Function = Initialize Write (101) or if Function = Initialize Read (110), then Address specifies the starting address of a table in storage (an I/O block). The contents of this table are data words and control information (Channel Command Words for the Selector Channel).
- 2. If Function = Control (100) and if, for example, Area specifies the 1443 Printer, the Address may specify a specific control action.
- 3. If Function = Sense (011) or (111), the Address field is ignored. Instead, an increment of time equivalent to a core storage cycle is taken, during which the selected I/O device or Interrupt Level places its status word in the Accumulator.
- 4. If Function = Write (001) or if Function = Read (010), the Address specifies the storage location of the data word.

XIO Execution Data Flow

The circled numbers in Figure 7 correlate with the data flow sequence that follows:

- 1. The EA of the XIO is developed in the Accumulator (A) and routed to the Storage Address Register (SAR) to locate the IOCC.
- 2. Bit position 15 of SAR is forced on to select the EA + 1 where the IOCC Area, Function, and Modifier are found.

43

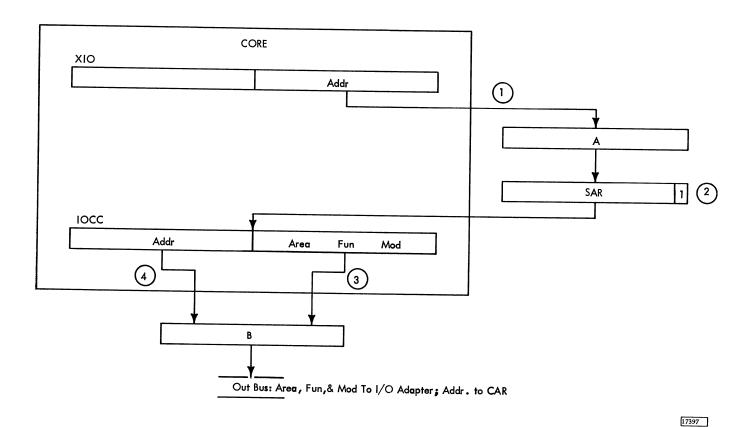


Figure 7. XIO Data Flow

- 3. The Area, Function, and Modifier are routed through the B-register to the Out-Bus to the I/O Adapter of the device specified by the Area.
- 4. Bit position 15 of SAR is turned off to allow the Address portion of the IOCC word to be transferred, from the core-storage location specified by the Effective Address (EA), to the B-register.
- 5. If the Function is an Initialize Read, Initialize Write, or Control, the Address part of the IOCC is routed through the B-register to the Out-Bus. The address part of the Initialize Read/Write IOCC goes to the Channel Address Register (CAR) of the Data Channel. If the Function is Read or Write, the Address is routed from the B-register through the A-register to the SAR. SAR addresses the storage location to or from which data is transmitted.

AREA CODE ZERO

The IOCC Area code 00000 is used with Modifier bits 8-10 to specify the particular feature or register listed below. These bits are fixed for all 1800 systems:

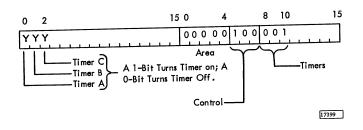
Feature/Register	Bits 8-10
Interval Timers	001
Console Data Entry Switches	010
Console Sense and Program Select Switches, and CE Switches	011
Interrupt Mask Register	100
Programmed Interrupt	101
Console Interrupt	110
Operations Monitor	111

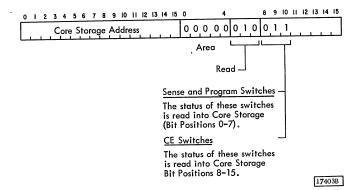
17398

The IOCC for each operation follows. Note that the Function specifies the operation. Those bit positions left blank are not used.

Interval Timers

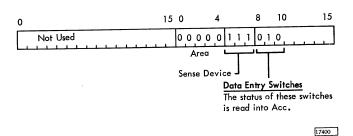
This IOCC is used to start or stop the interval timers. See 'Interval Timers' section.

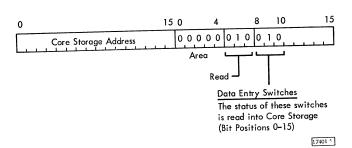


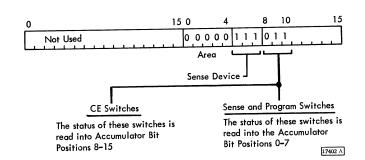


Console Data Entry Switches Console Sense and Program Switches

The following IOCC's are used to read the console switches into the accumulator or core storage.

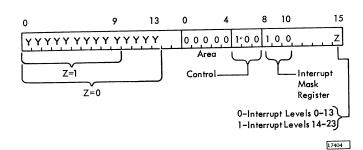






Interrupt Mask Register

This IOCC is used to mask or unmask customer interrupt levels 0-23. Internal check level, Trace, and CE interrupts cannot be masked.



Y - The status of bit positions 0-13 or 0-9, depending on Z, is copied into bit positions 0-13 or 14-23 of the 24-bit Interrupt Mask register.

A 1-bit turns the corresponding mask register bit on. This bit prevents the external interrupt on that particular level from being acknowledged until the mask is changed to unmask. A 1-bit prevents a Programmed Interrupt for its corresponding interrupt level.

A 0-bit causes the mask register bit to be set off, which enables the particular interrupt level.

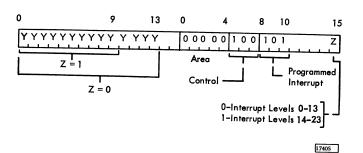
The execution of this instruction does not destroy the contents of the accumulator.

<u>Note</u>: Pressing the Console Reset key masks interrupt levels 0-23.

45

Programmed Interrupt

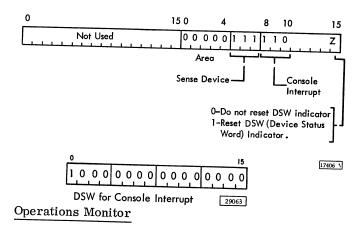
This IOCC is used to initiate an interrupt (or interrupts) from within the program. Programmed interrupts do not turn on bits in the ILSW. See 'Interrupt' section for details of programmed interrupt.



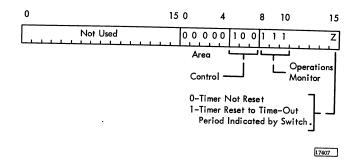
Y - A 1-bit in positions 0-13 or 0-9, depending on Z, turns on corresponding interrupt level 0-13 or 14-23 unless this level is masked or becomes masked prior to the forced BSI due to this instruction.

Console Interrupt

This IOCC is used to read the Console Interrupt Device Status Word (DSW) into the accumulator.



This IOCC is normally used to reset the Operations Monitor timer, thereby preventing its time-out and the resulting alarm that would otherwise occur. See "Operation Monitor" section for more detail.



Three timers are provided to supply real-time information to the program. They are in core storage locations 0004 (timer A), 0005 (timer B), and 0006 (timer C). Each timer has a permanent time base which can be selected by the customer (Table 4). All three timers can operate at different time periods.

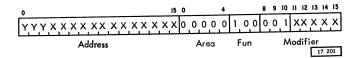
Table 4. Interval Timers

Core Storage Cycle Times	Available Time Bases (In Milliseconds)									
2 or 2.25 µsec	0.125	0.25	0.5	١	2	4	8	16	32	64
4 µsec	0.25	0.5	1	2	4	8	16	32	64	128
L										17408 A

The timers can be started or stopped under program control. Once started, they are automatically incremented one count at a time through the cycle stealing facility of the P-C. A count is added each time the assigned time base period is completed. This count is automatic and does not require a program. The count of the timers proceeds in the positive direction. When the count reaches the largest positive value (2¹⁵-1), the count continues to the most negative value and then through the negative numbers (two's complement) toward zero. When the count reaches zero, an interrupt is requested on the level assigned to the timers. (All three timers are on the same interrupt level which is assigned by the user.) The timer continues to operate after the zero value has been reached.

The timers, once operating, continue to record time correctly when the P-C is in the Run, Trace, or SIW/CS mode. Further, a WAIT instruction may also be executed by the program without affecting the timers ability to record time correctly.

The timers are started by means of the XIO instruction with the Function of <u>Control</u> referring to <u>Area zero</u>. The IOCC used to start and stop the timer has the following form.

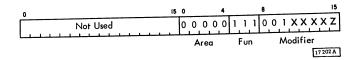


X - Unused

Y - This information is copied into the Timer Control. A one (1) causes the timer to be turned ON and a zero turns the timer OFF. Bit position 0 of the address corresponds to Timer A, Bit position 1 - Timer B, and Bit position 2 - Timer C.

Modifier 001 - Unit Address of Timers

The IOCC used to sense the DSW and reset the interrupt assigned to the timers is:



Modifier 001 - Unit address of timers

X - Unused

Z - A 1-bit resets the DSW indicators; a 0-bit does not reset them.

The DSW has the following bit significance:

B0 Timer A

B1 Timer B

B2 Timer C

B3-15 Not Used

The bit being ON indicates that the timer has initiated an interrupt.

Note: The timers continue to increment correctly even if they are protected with a storage protect bit. However, any other attempt by the P-C or an I/O device to alter the data in a protected timer will cause a storage protect violation.

STORAGE PROTECTION

The Storage Protection facility protects the contents of specified locations of core storage from change due to the erroneous storing of information during the execution of a program. This protection is achieved by providing each location in core storage with a storage protect bit. The status of each storage location is identified as "read only" or "read/write" by the condition of the storage protect bit.

"Read only" is indicated by the bit being set to one (ON). "Read only" is defined as the ability to access a protected location, read the contents into the B-register and regenerate into the storage the contents that were read out. Under program control, any location in core storage may be designated as "read only". Since each location has its own storage protect bit, each location is conditioned individually by means of the Store Status instruction.

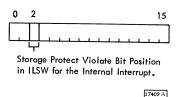
The Store Status instruction, with bit nine equal 1, is used to Write or Clear storage protect bits. See Instruction Set section for Store Status. The execution of this instruction is under control of the Write Storage Protect Bits switch on the P-C Console. When this switch is ON, the Store Status instruction can change the storage protect bits. When the Write Storage Protect Bits switch is OFF, this instruction (Store Status with bit nine equal 1) performs as a NO-OP.

Although the storage protect bit, the parity bit, and the 16 data bits result in an 18 bit word, only the 16-bit data word need be considered for instruction and data flow purposes. The odd parity bit covers the 16 data bits and the storage protect bit. Loss of any one of the 18 bits in a location is detected by a Parity Check.

Any attempt by the program to write into a "read only" protected location results in a storage protect

violation which causes an Internal Interrupt (highest priority interrupt). A 2-bit is placed in the Interrupt Level Status Word (ILSW) of the Internal Interrupt. The data in the protected location is not changed.

By storage protecting the word following the last word in input data tables, the storage protect bit can be employed to detect word count program errors. This can be especially beneficial during the check out of new programs. A word count in excess of the number of words available in the input table can cause the loss of data in words following the table.



If an XIO or cycle steal operation attempts to write into a protected location, the protected data remains intact and the Storage Protect Violation indicator is set in a bit position of the Device Status Word (DSW) associated with the device operating on the Data Channel. No internal level interrupt occurs.

The Check Stop switch being ON causes the P-C to stop at the end of the core-storage cycle in which any storage protect violation is detected. If the Check Stop switch is on the OFF position, a storage protect violation causes the P-C to initiate an internal interrupt or set the storage protect violation indicator in the appropriate DSW as described above.

The Disable Interrupt toggle switch on the P-C Console being ON prevents an Internal Interrupt.

Any attempt by the program to read from a core storage location having incorrect (even) parity or to write a word having incorrect parity will result in an Internal Interrupt. This includes initialization cycles (and loading CAR) of an XIO instruction. Reading from core storage takes place as an instruction is read out to be executed, as an address is read out, etc. In these circumstances a parity error will not prevent instruction execution. Therefore, programmed recovery may not be possible.

If a parity error causes an I/O device to reject the XIO command (Initialize Read or Write only) during the XIO control cycle, a CAR check will also occur since CAR is not selected to be loaded. If a parity error is detected during a data cycle (cycle steal) the Device Status Word of the device will have the parity error indicator set. The core storage word in error can be found by using a routine such as the following that loads data (from core) into the A register and detects the error at the time the internal interrupt occurs. A parity error during a data cycle resulting from an XIO instruction, does not cause an Internal interrupt. This parity error results in setting the parity indicator in the Device Status Word (DSW) for the I/O device being used. It is the responsibility of the program operating that

	•		•	
	•		•	
	•		•	
	LDX	L1	INTRP	Setup Interrupt Branch Address
	STX	Ll	8	
	LDX	L1	+32,767	XR1=Core Storage Size
LOOP	LD	1	0	
	MDX	1	-1	
	MDX		LOOP	
	•		•	
	•		•	
	•		•	
INTRP	DC		0	Internal Interrupt Branch
	•		•	
	•		•	XR1=Address of Error Word
	•		•	
	BOSC	I	INTRP	Check Next Word
				23413

device to initiate retries or other error recovery procedures.

The Check Stop switch being ON causes the P-C to stop at the end of the core-storage cycle in which any parity error is detected. If the Check Stop switch is in the OFF position, a parity error causes the P-C to initiate an internal interrupt or set the parity indicator in the appropriate DSW as described above.

The Disable Interrupt toggle switch being ON prevents an Internal Interrupt.

OPERATIONS MONITOR

This basic feature of the 1800 System can be used to check program operation. If the 1800 P-C fails to execute a predetermined sequence of instructions, within a pre-selected time interval, an alarm circuit is activated. The alarm may be audible and/or visual (an indicator light is located at the 1800 console). Both the alarming device and the power required to operate it must be furnished by the customer. (Customer power is limited to 30 volts and 1 ampere.)

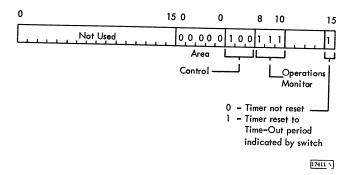
The Operations Monitor includes an internal timer and manual controls on the 1800 console. The operator may select any one of six time intervals: 5, 10, 15, 20, 25, or 30 seconds. (The selection switch is located on the CE panel underneath the console.) Once the Operations Monitor has been activated by the operator, a reset monitor timer command must be executed during program operation at intervals frequent enough to prevent the timer from timing out. If the reset command is not given during the selected time interval, the timer runs out and the alarm circuit is activated. Once the Operations Monitor alarm is on, it cannot be reset off by the P-C program executing a XIO control instruction; reset can only be accomplished by manually turning the Operations Monitor toggle switch off. The cause of the timeout should be identified before the switch is turned back on. Timeout can also be caused by a power failure, computer hang-up, computer looping, or any departure from the predicted instruction sequence in the program.

Programming Note

The use of the Operations Monitor depends on the positions of two switches:

- 1. The time interval selection switch on the CE panel.
- 2. The Operations Monitor on-off toggle switch on the P-C console. The first time interval is initiated when this switch is turned on.

With these two switches correctly positioned and the P-C in programmed operation, the Operations Monitor timer must be reset at intervals frequent enough to prevent it from timing out and causing an alarm. An XIO instruction with the IOCC described below is used to reset the timer:



POWER FAILURE PROTECT

In the event of an emergency power failure, circuitry is provided which permits the P-C to complete execution of the instruction in progress prior to termination of program control. The program is automatically terminated and the system is reset at the completion of the cycle in progress.

The P-C console (Figure 8) provides the means for manual control of the Processor-Controller during debugging or operating phases.

The basic operating features and controls provide the facility to:

- 1. Start or stop instruction execution.
- 2. Address core storage.
- 3. Set-up and store data or instructions.
- Communicate with the program via Sense or Program Select switches.
- 5. Control the cycling rate in the Run, Single Storage Cycle, Single Instruction, or Single Step modes.
- 6. Interrupt the program manually.
- 7. Trace each instruction.
- 8. Reset all control circuitry and storage.
- 9. Turn power on and off.
- 10. Indicate basic machine conditions and status.
- 11. Display storage words and register data.
- 12. Write or clear storage protect bits.
- 13. Clear core storage.

PUSH-BUTTON SWITCHES AND LIGHTS

There are two rows of push-button switches and lights. One row is at the top of the console (Figure 9) and one row is at the bottom (Figure 10). Descriptions of their functions follow:

Clear Storage

This push-button (P.B.) switch has four functions (Table 5). None of the four functions can be executed, however, until Clear Storage is first held pressed and then Start is pressed. This dual action requirement prevents the accidental clearing of storage. Note in Table 5 that each clear storage function is dependent on the positions of two console switches, the rotary Mode switch and the Write Storage Protect Bits (WSPB) toggle switch.

The P-C cycles completely through all core storage addresses during the execution of each clear storage function.

Program Load

The Program Load push-button switch (Figure 8) is used to load the first 1442 card or 1054 tape record

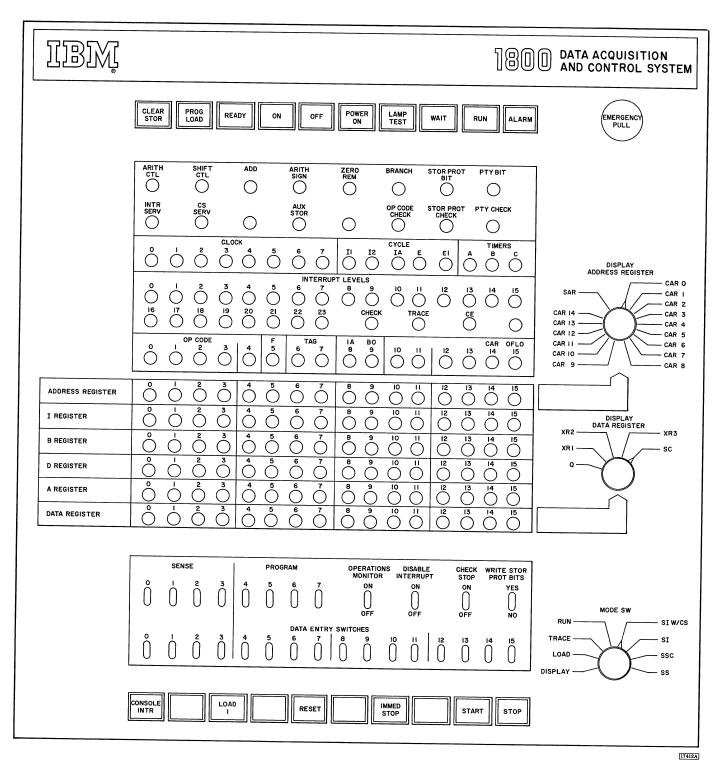
into core storage. The Reset push-button switch must be pressed prior to pressing the program load switch. The input device must be in a "ready" condition. The first card or tape record loaded must contain instructions that will initiate loading the remainder of the cards or tape records. (P-C must be in Run Mode for program operation.) Only one input device can be used for Initial Program Load. The first 1442 on the system will be used for Initial Program Load (IPL). The 1054 is used for IPL when there is no 1442 on the system.

The program load operation does not alter the status of the interrupt mask register.

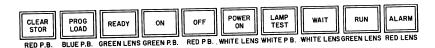
When the 1442 is used for Initial Program Load, it operates in Packed Mode, reading the 80 columns of the first card into core-storage locations 0000- $0039 (0000_{16} - 0027_{16})$. Each core-storage location stores the binary data from two card columns. For example, binary data from card column 1 (Rows 12-5) is read into core-storage location 0000 (bit positions 8-15) and binary data from card column 2 (rows 12-5) is read into the same core-storage location (bit positions 0-7). Rows 6-9 of the card are not read into core storage. The remainder of the first card is entered in the same manner, entering all odd numbered card columns in bit positions 8-15 of their respective core-storage location, and entering all even numbered card columns in bit positions 0-7 of their respective core-storage location.

After the first card is read into core storage, the P-C begins (at 0000) executing the instructions that were stored in core storage from the first card. The first card must contain instructions to load the remainder of the program cards.

When the 1054 Paper Tape Reader is used for Initial Program Load, tape data is loaded into core storage, starting at location 0000 and loading succesively higher core-storage locations until an end-ofrecord punch is sensed in the tape. Each core-storage location stores the binary data from four tape characters. For example, binary data from the first tape character (channels 1-4) is stored in core-storage location 0000 (bit positions 0-3),..., binary data from the fourth tape character (channels 1-4) is stored in core-storage location 0000 (bit positions 12-15). The remainder of the tape data is entered in the same manner (four characters per word) until a channel 5 punch is sensed. (Any channel 5 punch except when it is in a delete character.) The channel 5 punch is the endof-record character and is not read into core storage.



• Figure 8. P-C Console



EMERGENCY

7413

Figure 9. Console Lights and Switches, Top Row

The 1054 interrupt requests are suppressed while in IPL mode.

Delete characters are characters containing punches in channels 1-7 and are not read into core storage while in IPL mode.

Channels 5-8 of the paper tape are not loaded into core storage during Initial Program Load.

The P-C then begins (at 0000) executing the instructions stored in core storage from the first tape record. If the entire program was not included in the first tape record, the first record must contain instructions for loading the remainder of the tape records (program).

Ready

This light is \underline{on} when the P-C is in an operative condition.

Off

This push-button switch is used to shut down the power supplies within the P-C.

On

This push-button switch is used to turn on the power supplies within the P-C.

Power On

This light is used to indicate that the P-C power supplies are operative.

Lamp Test

This push-button switch is pressed to apply lamp voltage to all console lamps. Its use is to verify operation of all console lamps.

Wait

This light is used to indicate that the P-C: is in either Load or Display Mode; has been halted by a Wait Instruction; has been halted by the operator pushing the Stop or Immediate Stop switch.

Run

This light is used to indicate that the P-C is operating under program control.

Alarm

This light is used to indicate that the Operation Monitor has timed out. The customer may install an audible alarm to operate in conjunction with the Alarm light. See "Operation Monitor" section.

EMERGENCY PULL SWITCH

This pull-switch is for emergency use only. If pulled out, all electrical power within the 1801/1802 is turned off, including power to the blowers that cool the electronic circuitry. Turning the blowers off in this manner may damage some of the circuitry. This switch must be reset by an IBM Customer Engineer.

Console Interrupt

This push-button switch enables the operator to interrupt P-C operation. The console interrupt level is assigned by the customer. The Program toggle switches may be used in conjunction with Console Interrupt to specify the console interrupt routine. However, this relationship between the Program switches and Console Interrupt would exist only by virtue of the program. There is no internal relationship between the two.

The Console Interrupt IOCC is provided in the "Area Code Zero" section of the description for the Execute I/O instruction.

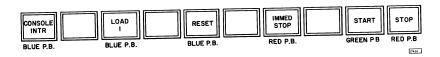


Figure 10. Console Lights and Switches, Bottom Row

Table 5. Clear Storage Functions

Function	Mode Switch	WSPB Switch
1. Store Contents of Data Entry Switches in all Core Storage Locations. Storage-Protect Bits are Removed and Parity is Corrected as Required Because of Bit Removal. If All Data Entry Switches Are Off, Only Parity Bits are Left in Storage.	Run	On
Store Contents of Data Entry Switches in Each Core Storage Location that is Unprotected. Locations having Protect Bits are Unchanged.	Run	Off
Clear Storage Protect Bits. All Other Data Remains Unchanged. Parity is Automatically Corrected in Each Word in Storage.	Display	On
Search for Parity Errors. The P-C Cycles Through Storage Until Stopped by the Stop Key or a Parity Error. The Check Stop Switch Must be on for a Parity Error to Cause a Stop.	Display	Off

17415

Load I

This push-button switch is used with the rotary Mode switch in the Load position to transfer the contents of the Data Entry toggle switches into the I-register of the P-C. The P-C is in the stopped condition when it terminates the Load I operation.

Reset

This push-button switch is used to reset all basic timing, controls, registers (except Index Registers and Address Registers), and I/O devices. The interrupt mask register is reset with all bits "on". The Digital Input and Digital-Analog Output registers are not reset.

Immediate Stop

This push-button switch stops the P-C at the end of the core-storage cycle in operation when the Immediate Stop contacts close.

All basic timing, controls, registers (except Index Registers and Address Registers), and I/O devices are reset. The Immediate Stop switch can also be used to stop data channel (cycle stealing) operations that are no longer under program control.

Stop

This push-button switch stops the P-C without resetting the P-C registers or I/O devices, at the end of the instruction in operation when the Stop contacts

close. Data channel operations can be stopped only by pressing Immediate Stop.

If, at the same time the Stop key is pressed, an interrupt occurs that can force a BSI (i.e., on an unmasked level higher than any in progress), the Stop key must be pressed again to be effective. Pressing the Start key causes the program to resume operation.

Start

This push-button switch initiates P-C operations, if the Ready light is on, as specified by the Rotary Mode switch.

Mode Switch

This eight-position rotary switch (Figure 11) is used with the Start switch to extend operator control of the P-C.

Single Instruction with Cycle Steal (SI W/CS): A Start switch depression with the Mode switch on SI W/CS causes the execution of one instruction. Data channel operations can occur during execution of the instruction.

Single Instruction (SI): A Start switch depression with the Mode switch on SI causes the execution of one instruction. Data Channel operations are prevented.

Single Storage Cycle (SSC): A Start switch depression with the Mode switch on SSC causes one storage cycle (2, 2.25, or 4 μ sec). Single Storage Cycle operations (usually called Single Cycle operations) can be used in conjunction with the console Cycle lights to step through instructions and analyze P-C operation.

Single Step (SS): A Start switch depression with the Mode switch on SS causes one basic P-C clock cycle. (See console Clock Lights.)

Run: A Start switch depression with the Mode switch on Run initiates normal program operation of the P-C.

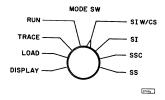


Figure 11. Console Mode Switch

Trace: This position of the Mode switch causes a Trace interrupt after the execution of each instruction. The Trace interrupt is a unique interrupt. It has no device status word, no interrupt level status word, and cannot be masked. The Trace interrupt is the lowest priority customer interrupt. Once initiated, it is delayed by the occurrence of any other interrupt. It cannot occur while other interrupts are being serviced. When the Trace interrupt occurs, the P-C executes the forced BSI and branches to the routine whose address is stored at 009. (See "Interrupt" section).

<u>Load:</u> A Start switch depression with the Mode switch on Load causes the contents of the Data Entry Switches to be stored at the address specified by the I-register. (The P-C must be in a stopped condition.) The I-register is incremented following each Load operation caused by pressing Start.

A Load I switch depression with the Mode Switch on Load causes the contents of the Data Entry switches to be stored in the I-register of the P-C.

Display: A Start switch depression with the Mode switch on Display causes the data at the I-register address to be displayed in the console B-register lights. The I-register is incremented after each display. Successive words are displayed with successive depressions of Start.

TOGGLE SWITCHES

See Figure 12.

Sense and Program

The contents of these eight switches may be stored in bit positions 0-7 of the A-register or a core storage location. An XIO instruction with an IOCC function of Read stores the contents of the Sense and Program switches at the core storage address specified by the IOCC. (See "Area Code Zero" in the description of the XIO instruction.) A function of Sense Device stores the switch data in the A-register.

Operations Monitor

This switch is used to start the Operations Monitor. The $\underbrace{\text{off}}$ position disables the Monitor.

Disable Interrupt

This switch is used to mask all interrupt levels, including Internal errors. It is especially useful during program analysis when the operator wants to choose the time at which the program may be interrupted. The highest level interrupt on and unmasked is serviced when the switch is turned off.

Check Stop

The switch is used to stop the P-C when one of the following errors occurs: invalid operation, parity error or storage protect error. The stop occurs at the end of the core-storage cycle in which the error is detected. The appropriate error light will be on. Start must be pressed to restart the system.

An internal error initiates an Internal Interrupt when Check Stop is OFF.

The Channel Address Register (CAR) Check internal level error is an exception to the above description of the Check Stop operation. A CAR Check error will initiate an internal level interrupt regardless of the position (ON or OFF) of the Check Stop switch.

A clear storage function is stopped when Check Stop is on and a parity error is detected (Table 5).

Write Storage Protect Bits

This switch enables the writing or clearing of storage protect bits. (See "Store Status" instruction and "Clear Storage" functions, Table 5). A parity error may occur if the position of this switch is changed while the P-C is running.

Data Entry Switches

The contents of these 16 toggle switches can be stored by either manual or program control. See "Area Code Zero" in the description of the XIO instruction for program control. The description of the Load position under "Mode Switch" describes manual control.

	SEN	SE.			PROG	RAM		OPERATIONS MONITOR	DISABLE INTERRUPT	CHECK	WRITE STOR PROT BITS
Ö	Ó	2)	3	Ô	5	6	Ö	ON OFF	ON OFF	OFF	YES
Ů	Ó	Č	Š	Ô	5	6 G	7 8	TCHES 9	0 11 12	13	14 15

Figure 12. Console Toggle Switches

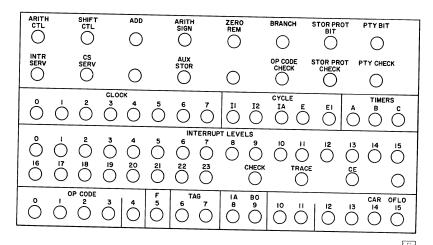


Figure 13. Console Indicators

CONSOLE INDICATORS

These indicators (Figure 13) show the status of various P-C functions and operations.

Arithmetic Control: On during arithmetic operations.

Shift Control: On during shift operations.

Add: On during add operations.

Arithmetic Sign: On when bit position zero in the Aregister (accumulator) does not initially equal bit position zero in the B-register.

Storage Protect Check: Turned on when an attempt is made to write into a "read-only" location.

The Storage Protect Check Console indicator is turned off and the Check Console indicator is turned on (internal interrupt) at the end of the cycle in which the error is sensed, allowing the storage protect indicator to indicate any subsequent storage protect error. (See "Storage Protect" section.)

Parity Check: Turned on when a parity error (even number of bits) is detected in the 18-bit word transfer between the B-register and core storage. The presence or absence of storage protect and parity bits in each word is indicated by their respective console indicators.

The Parity Check console indicator is turned off and the Check Console indicator is turned on (internal interrupt) at the end of the cycle in which the error is sensed, allowing the parity-check indicator to indicate any subsequent parity error. (See Parity section.)

Zero Remainder: On when the A-register contains a zero balance during a divide instruction.

Branch: On during branch instructions.

<u>Interrupt Service:</u> Turned on when the hardware BSI instruction is being executed for the highest level interrupt that is on and not masked.

<u>Cycle Steal Service:</u> On during cycle steal operations for the highest priority data channel requiring service.

Op Code Check: On when an invalid Op code is placed in the Op register. The Op Code Check console indicator is turned off and the check console indicator is turned on (internal interrupt) at the end of the cycle in which the error is sensed, allowing the the Op Code Check indicator to indicate any subsequent error.

The Op Code Check error causes an internal interrupt if the Disable Interrupt switch is off and causes a check stop if the Check Stop switch is on.

Auxiliary Storage: Core storage (CE Storage) is provided for Customer Engineering (CE) use. The indicator is on when CE storage is being used.

Storage Protect Bit: On when a storage protect bit is transferred with the 16 data bits between the B-register and core storage.

Parity Bit: On when a parity bit is transferred with the 16 data bits between the B-register and core storage.

Clock

These eight indicators (0-7) show the advance of the basic P-C clock during Start key depressions when the rotary Mode switch is on Single Step (SS). Normally, eight Start key depressions with the Mode switch on SS is equivalent to one Start key depression with the Mode switch on Single Storage Cycle (SSC).

Cycle

These five indicators (I1, I2, IA, E, and E1) show the progress of an instruction that is being <u>Single Stepped</u> or <u>Single Storage Cycled</u>; that is, advanced by successive Start key depressions with the rotary Mode switch on SSC or SS.

- shows that a new instruction is being set up for execution. It is turned on at the beginning of all single word instructions and for the first word of all double word instructions.
- shows that the second word of a double word instruction is being set up for execution.
- shows that the instruction being set up is a double word instruction that has an indirect address.
 The indicator is on while the indirectly addressed word is being read out of storage.
- E shows that the instruction set up during I-time has been defined by the Op code and is now being executed.
- E1 is turned on with the E indicator. Its on condition shows that instruction execution control circuitry has progressed to the E1 cycle point. E1 is turned off at the next clock zero (0) time. Instruction can then progress through E2 and E3 time.

 (There are no E2 and E3 console indicators.)

Timers

These three indicators (A, B, and C) show the status of their respective interval timers. An \underline{on} condition indicates that the timer is in operation.

Interrupt Levels: An Interrupt Level indicator is on for each interrupt level requesting service or being serviced. Once on, an Interrupt Level indicator can be reset by either of two instructions:

- A mask instruction that is executed before servicing of the interrupt begins. (The interrupt request is not lost but merely detained until the interrupt level is unmasked, at which time the indicator is turned back on.)
- 2. A branch-out-of-interrupt (BOSC) instruction is executed to complete servicing of the interrupt.

Both of the above instructions are quasi instructions; that is, variations of the XIO and BSC instructions.

The last three interrupt level indicators—Customer Engineering, Trace, and Check (Internal Interrupt) — cannot be masked. The CE interrupt can be initiated only from the CE panel or from a device operating in CE mode.

Operation Code

These five indicators (0-4) display the Op code of each instruction.

Format (F)

This indicator is \underline{on} when a two-word instruction is specified.

Tag

The status of these two indicators reflect the instruction register or index register modification of the instruction address (the <u>on</u> condition of the indicators is shown by a 1):

Indic	ators	Register
6	7	Register
0	0	I-Reg
0	1	XR-1
1	0	XR-2
1	1	XR-3

17419

Indirect Addressing

The IA (Bit 8) indicator is on when the instruction contains this bit, which usually indicates indirect addressing.

Branch Out

The BO (Bit 9) indicator is <u>on</u> when there is a bit in position 9 of an instruction. When on in a BSC instruction, a branch-out-of-interrupt (BOSC) <u>is</u> specified.

Carry and Overflow

These two indicators are turned on individually when their respective conditions occur in the accumulator (A-register).

DATA FLOW DISPLAYS

Six rows of indicators and two rotary switches (Figure 14) facilitate the display of data flow in the P-C. A review of the P-C Data Flow section and the Data Channel section is recommended at this point.

Address Register

These 16 indicators display the data in the Storage Address Register (SAR) or the selected Channel Address Register (CAR), depending on the position of the Display Address Register rotary switch. The selected register is displayed each time the P-C comes to a stop or wait condition. (The clock will be at 7.)

Display Address Register Switch

The 16-position rotary switch is used to select a CAR or SAR for display in the Address Register.

Permanent Register Displays: I, B, D, and A

The contents of these four registers are always displayed.

Data Register

These 16 indicators display the contents of the Q-register, which is the accumulator or A-register extension, the index registers (XR1, XR2, or XR3), or the shift counter (SC), depending on the position of the Display Data Register rotary switch. The selected register is displayed each time the P-C comes to a stop or wait condition. (The clock will be at 7.)

Display Data Register Switch

This 5-position rotary switch is used to select the Q-register, an index register, or the shift counter for display in the Data Register.

DISPLAY PROCEDURES

The following procedure may be used to display core storage data between the execution of single instructions:

1. With the P-C in a stop condition, position the rotary Mode switch to SI (Single Instruction).

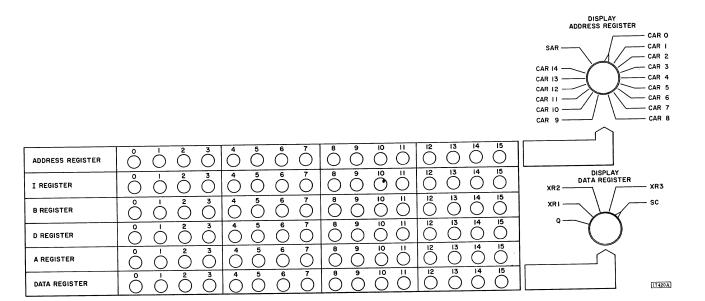
- 2. Start switch depressions may now be used for single instruction operations to get the program to the desired point for data display.
- 3. Record the address in the I-register. (The I-register is used in Display mode and this recorded address is needed to return the P-C to the next instruction.)
- 4. Set the address of the core storage word to be displayed in the Data Entry Switches.
- 5. Position the Mode switch to LOAD.
- 6. Press Load I switch.
- 7. Position Mode switch to DISPLAY.
- .8. Press START. The selected word is now displayed in the B-register indicators.
- 9. To display other core storage words, repeat steps 4 through 8.
- 10. To continue the program:
 - a. Set Data Entry Switches to address recorded in step 3.
 - b. Position Mode switch to LOAD.
 - c. Press Load I switch.
 - d. Position Mode switch to RUN.
 - e. Press START.

To display core storage data between single core storage cycle operations:

- 1. With the P-C in a stop condition, position the Mode Switch to SSC (Single Storage Cycle).
- 2. Press START repeatedly until the desired cycle the execution of the instruction is reached.
- 3. Perform steps 3 through 10 of the preceding Single Instruction execution procedure.

PROGRAM FAILURE—RESTART

Program restart points should be written into programs to allow recovery of the system or a complete restart of the system. This recovery procedure must consider the nature of the process and the operational philosophy of the customer.



• Figure 14. Data Display Lights and Switches

I/O CONTROL

There are two basic methods of transmitting and/or receiving data to or from the P-C. First, specific low speed devices are controlled directly by the program. In this Direct Program Control operation, each character or word of data is transmitted to or from the P-C core storage by means of separate Execute I/O (XIO) instructions. The program continues transmission, character by character, or word by word, by responding to "Service Request" interrupts. Devices operating under Direct Program Control (DPC) include:

1053 Printer
1054 Paper Tape Reader
1055 Paper Tape Punch
1627 Plotter
1816 Printer Keyboard
Process I/O Devices such as analog-to-digital
converters, contact sense, voltage level
sense, pulse counters, etc.

The second method of transferring data is transfer via the Data Channels. Data channel (DC) operations are initialized by a single XIO instruction. The transfer of data words then proceeds under control of the specified DC, completely asynchronous to program operation.

The Data Channel method of accessing core storage provides a powerful means of I/O communication with the core storage. Whenever the DC requires core storage access, the P-C operation is suspended for one core storage cycle time. During this cycle, the data is taken from or placed into core storage. Access by the DC can occur at the end of any storage cycle. It does not require that an instruction be completed. As soon as the DC has been satisfied, which normally takes one cycle, the stored program execution proceeds. The logical state of the P-C is not changed by the DC's access to core storage. This method of access is sometimes referred to as "cycle stealing" since a cycle is taken from the stored program execution cycles at any time.

Devices operating under DC control include:

1442 Card Read Punch 1443 Printer 1810 Disk Storage 2401/2402 Magnetic Tape 2790 Adapter CA (Line Adapter) Selector Channel System/360 Adapter

Some devices operate under DC or DPC control, depending on their characteristics and the configuration of the 1800 system. These devices include:

Analog Input Analog Output

Digital Input Digital Output

ON-LINE MAINTENANCE CONSIDERATIONS

The 1800 System is designed to provide a means for limited On-Line maintenance of most DP and Communications I/O features without interrupting the customer operations. Such on-line maintenance is limited to cases where it will not affect user operations. In any case, the user will be notified when any on-line maintenance is performed.

The feature which makes this service approach possible is CE Core Storage which provides the Customer Engineer (CE) with storage for the necessary programs and data.

CE Storage is designed to prohibit the possibility of alterations of the main core storage during service operations. CE Storage cannot read or write in main storage, but main storage can read or write in CE Storage.

To assist Customer Engineers in maintenance of complex I/O devices such as the Communications Adapters (CA), 2790 Adapters, and Selector Channel, the Multiprogramming Executive (MPX) Operating System provides the following error information:

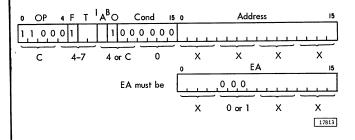
- 1. Error logs for CA, 2790 Adapters, and Selector Channel.
- 2. Error Statistics table for each CA line adapter.
- 3. A CA trace buffer.

This information is stored in CE Storage and is maintained on a real-time basis.

Seven modified instructions are used by MPX to maintain the error information in CE storage. These instructions utilize CE storage addresses shown in the following illustration to address CE storage. The instructions are described in the following paragraphs.

		System Storage in 8K Increments						
	lst	2nd	3rd	4th	5th	6th	7th	8th
	0000	2000	4000	6000	8000	A000	C000	E000
CE Storage Addresses in Hex	00FF	20FF	40FF	60FF	80FF	AOFF	C0FF	EOFF
	1100	3100	5100	7100	9100	B100	D100	F100
	11FF	31FF	51FF	71FF	91FF	BIFF	DIFF	FIFF
								17812

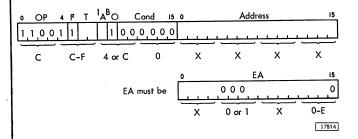
Load Accumulator (LD)



Description: The contents of the CE storage location specified by the effective address (EA) of the instruction replace the contents of the Accumulator (A). The contents of the CE storage location are unchanged. Indexing and Indirect Addressing are performed in the same manner as with normal instructions. (Indirect addressing uses main storage addresses.)

<u>Indicators</u>: The Carry and Overflow indicators are not changed by the instruction.

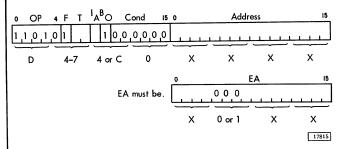
Double Load (LDD)



Description: The contents of the CE storage location specified by the instruction (EA) and the next higher CE storage location (EA+1) are loaded into the Accumulator (A) and its extension (Q), respectively. The EA of the instruction must be an even address for correct operation. If the EA is odd, the contents of that location are entered into both A and Q. The contents of the CE storage location are unchanged. Indexing and indirect addressing are performed in the same manner as with normal instructions. (Indirect addressing uses main storage addresses.)

<u>Indicators</u>: The Carry and Overflow indicators are not changed by this instruction.

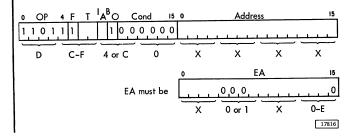
Store Accumulator (STO)



Description: The contents of the Accumulator replace the contents of the CE storage location specified by the effective address. The contents of the Accumulator are unchanged. Indexing and indirect addressing are performed in the same manner as with normal instructions. (Indirect addressing uses main storage addresses.)

<u>Indicators</u>: The Carry and Overflow indicators are not changed by this instruction.

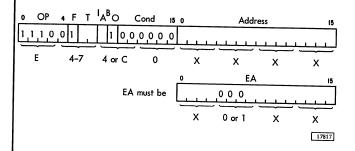
Double Store (STD)



Description: The contents of the Accumulator (A) and its extension (Q) are stored at the CE storage location specified by the EA and EA+1. The EA of the instruction must be an even address. If the EA is odd, the contents of the Accumulator are stored at the EA and the contents of Q will not appear in storage. The contents of A and Q remain unchanged. Indexing and indirect addressing are performed in the same manner as with normal instructions. (Indirect addressing uses main storage addresses.)

<u>Indicators</u>: The Carry and Overflow indicators are not changed by this instruction.

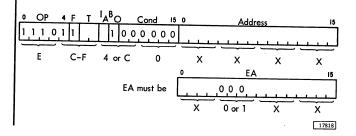
Logical AND (AND)



Description: The contents of the CE storage location specified by the EA are ANDed bit by bit with the contents of the Accumulator. The result replaces the contents of the Accumulator and the CE storage location remains unchanged. Indexing and indirect addressing are performed in the same manner as with normal instructions. (Indirect addressing uses main storage addresses.)

<u>Indicators</u>: The Carry and Overflow indicators are not changed by this operation.

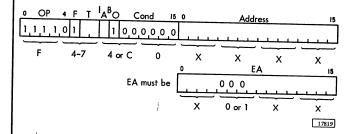
Logical OR (OR)



Description: The contents of the CE storage location specified by the EA are ORed bit by bit with the contents of the Accumulator. The result replaces the contents of the Accumulator, and CE storage location remains unchanged.

<u>Indicators</u>: The Carry and Overflow indicators are not changed by this operation.

Logical Exclusive OR (EOR)



<u>Description</u>: The contents of the CE storage location specified by the EA are Exclusive ORed bit by bit with the contents of the Accumulator. The result replaces the contents of the Accumulator, and the CE storage location remains unchanged.

<u>Indicators</u>: The Carry and Overflow indicator are not changed by this operation.

Customer Engineering Mode

Customer Engineering mode is enabled or disabled by a CE diagnostic program with the execution of an XIO instruction. The IOCC of the XIO must contain the area code of the device to be placed in CE mode and a function code of 000. CE mode is enabled with Bit 15 on and disabled with Bit 15 off.

When an I/O device is in CE mode and is being exercised by a CE program, the main storage program is impacted only by the execution time of the CE instruction. Because the CE mode operates on the lowest interrupt priority, service programs will execute only when the main storage programs are not operating on interrupt routines.

To permit this service approach, it is necessary to reserve words 1, 2, and A₁₆ in main storage. It is also necessary for main storage programs to have the ability to program disconnect any I/O device that requires servicing.

Once the CE mode is operating in CE storage, all subsequent interrupts (except internal interrupts) are masked until a BOSC is executed by the CE program. However, if an internal interrupt occurs while in CE storage, the CE interrupt level is reset and the program branches to the main storage internal interrupt routine. Upon completion of the routine instead of returning to CE storage, the program returns to the corresponding main storage address. Thus, any program that branches out of an internal interrupt routine returns to an address undefined by the program if the interrupt routine was entered from CE storage. However, most programming systems provide a restart procedure for internal interrupts.

CE programs can utilize the Arithmetic and Index registers. All service programs restore these registers to their original state before branching out.

It is necessary for the customer to realize that a CE service program can possibly interrupt from a Wait instruction in main storage. When this occurs, the branch out from this CE program will be to the instruction at the address following the Wait instruction.

When in CE mode, the device status word of the device is altered to make the device appear to be not ready and not busy, which is off line status. The true status of ready and/or busy is located elsewhere in the device status word and is used for diagnosis. The action initiated in the CE diagnostic program interrupts on the CE level and not on the normal assigned level of the device. The CE mode uses the assigned core-storage addresses (0001, 0002, and 000 A_{16}). The interrupt on CE level stores the instruction register at location 000A₁₆ in main storage (even if this location is storage protected) and branches to execute location 0001 in main storage or to location 0001 in CE storage depending on the position of the aux/ main storage switch on the CE panel. The Branch out of CE interrupt branches indirectly to location $000A_{16}$ for return to the main program.

DIRECT PROGRAM CONTROL OPERATION

DPC operation of I/O devices proceeds on a one for one basis; that is, an XIO instruction is executed for each data word transferred to or from core storage. The XIO instruction for DPC specifies an I/O Control Command (IOCC) with a <u>function</u> of Control, Sense Interrupt Level, Sense Device, Read or Write. (See description of XIO instructions.)

Control: An IOCC with a <u>function</u> of Control uses the IOCC <u>address</u> and <u>modifier</u> to specify the particular device and the operation to be executed. Examples of Control operations are Feed Card, and Load Interrupt Mask Register.

Sense: An IOCC with a <u>function</u> of Sense Interrupt Level or Sense Device is used to read the "status words" associated with the device: the Device Status Word (DSW), the Process Interrupt Status Word (PISW), and the Interrupt Level Status Word (ILSW). These status words are explained in detail in the "Interrupt" section.

Read or Write: An IOCC with a function of Read or Write uses the IOCC $\underline{address}$ to determine the core storage address receiving or providing the single data word. Immediately following the one word transfer to or from storage, the XIO instruction is terminated and the next sequential instruction is executed. Normally, several data words must be transferred to complete the message transfer. This is accomplished by P-C recognition of a device interrupt each time the device is ready to send or receive a data word. P-C recognition of the interrupt causes a branch to a program subroutine associated with the device interrupt. The interrupt subroutine includes the XIO instruction to read or write the next data word. This subroutine must also modify the address portion of the IOCC for the next data word, provide "table look up" for translation of the device character if required, and maintain a program word count to indicate the end of message if necessary.

The exit from the interrupt subroutine must be accomplished with a BSC instruction that has a one in its Bit 9 position. This Branch-Out-of-Interrupt (BOSC) operation restores the interrupt hardware so that future interrupt requests at the same or lower priority levels can be acknowledged.

Device Busy

It is possible for the program sequence to execute an XIO instruction to a device that is busy responding to a previous XIO instruction. Each device that can have this condition will provide a Busy indicator in the DSW. This indicator signals that the device cannot accept data or control information, and that should it be sent it will be lost. It is up to the program to ensure, by testing the Busy indicator, that data will not be lost. Usually no hardware indication is given to signal incorrect use of the device.

Data Overrun

It is possible for a device operating asynchronously to the program to request a data word transfer before the program sequence is ready to service the request. This can be true for both input and output. Devices with this potential provide a "program check" indicator that will enable the P-C to know if a data overrun occurs.

DATA CHANNEL (DC)

Data channels are used to transfer data between P-C core storage and high-speed I/O devices. The P-C initializes each DC with a single XIO instruction. The DC then takes control of the data transfer while the P-C continues program operation. The DC has priority to the extent that when the I/O device is ready to send or receive a data word, the P-C is stopped while the word transfers to or from core storage. This transfer takes 2, 2.25, or 4 $\mu \rm sec$, depending on the core storage cycle time, and is referred to as a cycle steal. P-C data and conditions are undisturbed except for the core storage locations that receive data from an input device.

Three DC's are standard on the 1800 system; twelve more are available on an individual basis. Thus, it is possible to have more than one I/O device requesting core storage cycles at the same time. When this occurs, the DC control circuitry stops the P-C and services the requesting devices according to their DC priority. This DC priority is an assigned hardware priority and is not related in any way to the Interrupt feature.

The maximum time before service of the highest priority DC (level zero) is 2.25, 2.50, or $4.5~\mu \rm sec$, depending on the cycle time of core storage. After all requesting devices have been serviced, the P-C continues with the program.

I/O devices that are to be operated concurrently must be on separate DC's. Within configuration restrictions, those devices that do not require concurrent operation can be on the same DC. When multiple devices are assigned to the same data channel, the Busy indicator of all these devices must be tested before an operation can be given to any of these devices.

The XIO instruction for DC specifies an I/O control command (IOCC) with a function of Initialize Read or Initialize Write. However, even though a device operates on a data channel, XIO instructions for DPC can be used to sense device status and for control. (See description of XIO instructions.)

Programming Note: All devices attached to a data channel will treat an XIO instruction as a no-op if the addressed device is busy or not ready.

Data Channel Functional Components

Channel Address Register

A Channel Address Register (CAR) is a 16 bit register used to store the core-storage address of the next word that will be addressed (by the Channel Address Buffer) for an operation with its associated Data Channel. Each Data Channel is assigned to a particular I/O device and has its own Channel Address Register.

A Data Channel and its associated CAR are selected when their assigned I/O device is selected by the Area Code and Modifier of an IOCC word. CAR is incremented by one after each transfer of its contents to the Channel Address Buffer.

Channel Address Buffer

One Channel Address Buffer (CAB) is used by all Channel Address Registers to address core storage. When a cycle steal request occurs, the CAR for the requesting I/O device is transferred into the Channel Address Buffer.

Channel Address Register Check

Channel Address Register (CAR) checking is provided to ensure that the first word addressed by a selected CAR is the first word of the correct data table. The CAR check will be performed in one of two ways, depending on the type of I/O device (chaining or non-chaining).

Non-chaining devices are the

1442

1443

1810

2790 Adapter

Selector Channel*

Chaining devices are the

2401/2402

Analog Input

CA Line Adapter

Digital-Analog Output

Digital Input

System/360 Adapter

^{*}Data chaining with the Selector Channel is accomplished through use of Channel Command Words as described in the Selector Channel section of this manual.

A CAR check is made for all devices after the Address from the IOCC word is transferred to the selected CAR. A bit by bit comparison is made between the contents of the selected CAR and the contents of the B-register. If any of the corresponding bits are not equal, a CAR check error occurs. This CAR check error terminates subsequent cycle steal requests for the assigned I/O device and initiates an internal interrupt. The I/O device cannot request a cycle steal until the Interrupt Level Status Word for the internal interrupt is sensed and the I/O device is reinitialized by another XIO instruction.

Another CAR check is made for chaining devices each time the I/O device chains to a different data table. The CAR check at the beginning of the second data table and all subsequent data tables in the chain is accomplished as follows: The first word of the data table (second data table, third data table, etc.) must contain its own address. After the first word of the data table is addressed, a bit by bit comparison is made between the contents of the selected CAR and the contents of the B-register. If any of the corresponding bits are not equal, a CAR check error has occurred. Subsequent cycle steal requests are terminated and a bit is set in the DSW for the device.

I/O Device Functional Components

Word or Byte Count Register

A Word Count Register is provided in each of the following I/O devices assigned to a Data Channel:

1443 1810 2401/2402 Analog Input Digital-Analog Output Digital Input System/360 Adapter

The Word Count Register is loaded with the contents of the word count portion (bit positions 2 - 15) of the data table and is decremented each time a data word is transferred from or to the data table. For I/O devices without chaining ability, the word count must be stored in the first word of the data table. For devices with chaining ability, the word count must be stored in the first word of the first data table and in the second word of all subsequent data tables in the chain.

A Byte Count Register is provided for each of the following devices:

CA (Line Adapter) Selector Channel

The Byte Count Register for the CA (Line Adapter) is analogous with the Word Count Register, except the count represents the number of character locations supplied by the data table (two characters per word.) The Selector Channel Byte Count Register contains the number of eight bit bytes in the input or output area. It is loaded from the Byte Count Word of a Channel Command Word (CCW), and decremented each time a byte is transferred from or to core storage. (See Selector Channel.)

The following is the word or byte count capacities for the devices:

Device	Number of Bits Available	Word <u>Cou</u> nt Bit Positions	Max Count Accepted by Device
1443	7	9-15	60 or 72
1810	9	<i>7</i> -15	321
2401/2402	14	2-15	16,383
Al	14	2-15	16,383
CA (Line Adapter)	12	4-15	4,095
DAO	8	8-15	255
DI	8	8-15	255
Selector Channel	16	0-15	65,535
System/360 Adapter	14	2-15	16,383

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Scan Control Register

A Scan Control Register is provided in each device that has chaining ability. Scan control bits must be stored in the first word of the first data table (bit positions 0 and 1) and in the second word (bit positions 0 and 1) of the second data table and all subsequent data tables in a chain. The following is a list of the devices that have a Scan Control register.

2401/2402 Analog Input CA (Line Adapter) Digital-Analog Output Digital or Pulse Counter Input System/360 Adapter The Scan Control register controls the I/O device and the Data Channel operation at the end of the data table as follows:

Bit 0	Bit 1	
0	0	Single scan of data table and stop with an interrupt
0	1	Single scan of data table and stop (no interrupt)
1	. 0	Continuous scan of this data table or a different data table with an interrupt at the end of this table.
1	1	Continuous scan of this data table or a different data table with no interrupt.

DATA CHANNEL OPERATION

The numbered steps that follow correlate with the circled numbers in Figures 15 and 16. These steps apply to either non-chaining devices or the first data table of a chaining device.

- 1. XIO references the IOCC word.
- 2. The Area Code and Modifier select the I/O device. Function specifies the type of operation (Initialize Read or Initialize Write, etc.)
- 3a. The Address portion of the IOCC word is stored in CAR for the selected Data Channel (I/O device).
- 3b. CAR Check made between selected CAR and B-register.
- 4. Cycle steal requested. CAR transfers to CAB.

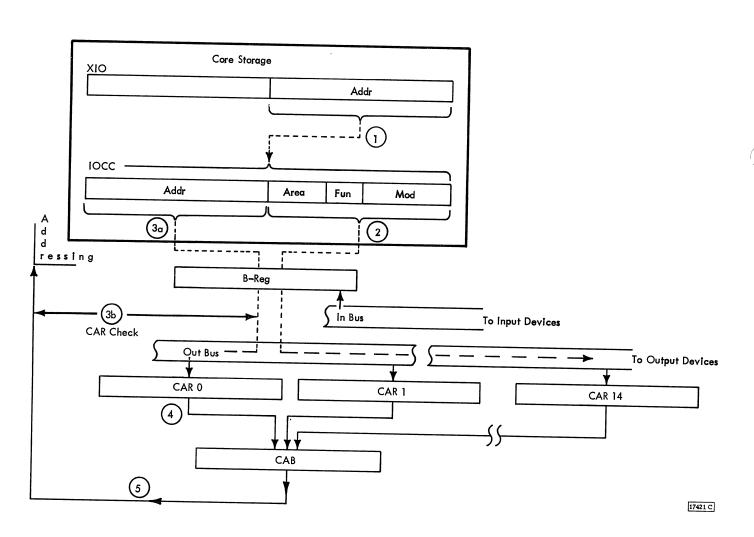


Figure 15. Data Channel Operation

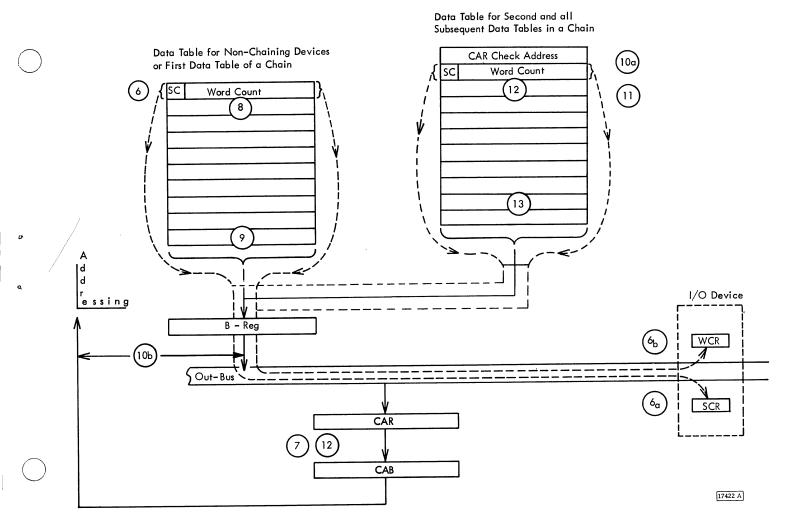


Figure 16. Data Channel Operation

- 5. CAB addresses core storage for the first word of data table while CAR is being incremented by one.
- 6. The first word of the data table contains

 a. Scan control bits (bit position 0 and 1)
 b. Word Count (bit position 2-15)
 These are transferred to their respective registers in the I/O device. This is the end of the first cycle steal cycle.
- 7. When another cycle steal request occurs, CAR, which was incremented in step 5, now transfers the next higher address to CAB. CAB then addresses core storage while CAR is being incremented.
- 8. The first <u>data</u> word is transferred to or from the I/O device via the B-register and Data

Channel. The Word Count register in the I/O device is decremented by one. This is the end of the second cycle steal cycle.

Steps 7 and 8 now continue on a cycle steal basis; that is, they occur as the I/O device requests data transfers. Between cycle steals, the P-C continues program operation. The CAR is incremented with each data transfer and the WCR is decremented. This sequence continues until the last data word of the data table is transferred. The last word transfer is sensed by the WCR reaching zero or through some indicator in the device. If the device does not have chaining ability, no more demands for data transfer are made until the device is reinitialized with another XIO instruction.

Data Chaining

When a continuous scan is indicated by the Scan Control Register (SCR) in a device having chaining ability, the DC takes three cycles after the WCR has reached zero at the end of the data table. The first cycle is used to transfer the word following the data table to the CAR. The address in this word is the address of the next table of data. The second cycle addresses the first word of the data table and performs the CAR check. The first word of the data table must contain its own address. The third cycle addresses the second word of the data table and transfers its contents (Word Count and Scan Control) to their respective registers. The I/O device is then ready for independent Data Channel operation. In this manner, the DC can operate in a scatter read-write mode. This method of using the DC in a continuous mode is called "data chaining" because the data tables are essentially connected together. The length of time between data transfer cycles on a data chaining operation is a maximum of three corestorage cycles on a device connected to the highest priority DC. It may be greater than this for devices of lower cycle steal priorities, depending on whether they must wait for higher DC priorities to be serviced.

Data Channel Operation (Chaining)

If the Scan Control register contains the bits for a continuous scan, the following numbered steps correlate to the circled numbers in Figure 16. These steps are for the second and all subsequent data tables. See section "Data Channel Control" for steps 1 through 8 (first data table).

- 9. The contents of the word following the last data word in the first data table are transferred to CAR. This word must contain the address of the next data table.
- 10a. When the next cycle is requested, CAR is transferred to CAB to address core storage. The contents of the first word of the next data table are transferred to the B-register. This word must contain the address of itself.
 - b. CAR Check is performed and CAR is incremented by one.
- 11. When the next cycle steal is requested, CAR is transferred to CAB and CAB addresses core storage. The Scan Control bits and Word Count bits are transferred from the second word of the data table to their respective registers. CAR is incremented by one.
- 12. Data is transferred to (from) the I/O device on a cycle steal basis via the B-register and the Data Channel. CAB addresses core storage to transfer a data word to the B-register. Each time CAB addresses core storage, CAR is incremented by one. When the next cycle steal request occurs, CAR is transferred to CAB. The Word Count register is decremented for each word transferred.
- 13. When the last data character is transferred (Word Count is decremented to zero), operation will continue as specified by the Scan Control register. See section for "Scan Control Register."

Data Table

Figure 17 is an illustration of two data tables with Scan control (SC) bits to initiate chaining from the first data table to the second data table.

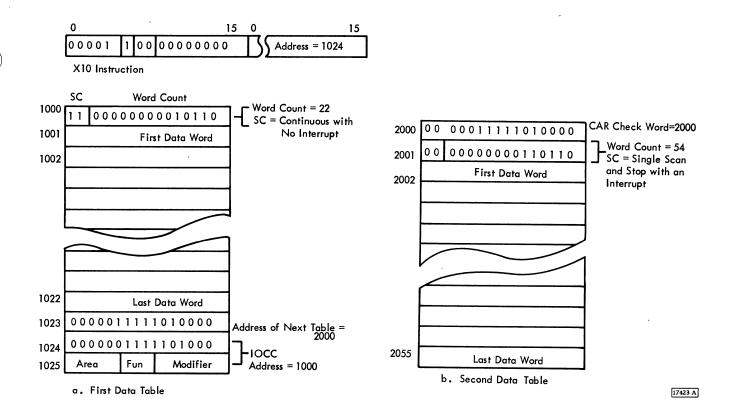


Figure 17. Data Tables for Chaining

To allow for coordination of overlapped I/O operations and provide for a smooth flow of productive processing, it is necessary to provide a means of switching from one program routine to another. In the 1800, an interrupt system is provided for this purpose.

The Interrupt feature provides an automatic branch from the normal program sequence. The branch is based upon an external condition. Examples of conditions which would normally be used to cause interrupts follow: (1) The Interval Timer has concluded the recording of a preset time interval. (2) The Magnetic Tape drive initialized and selected on a Data Channel has completed the required data transfer and signals the P-C with a Scan Complete. (3) An undefined operation code has been detected during the P-C instruction readout and therefore cannot be executed. (4) A device, such as the Printer Keyboard, has completed the transfer of the previous character and requests a subsequent character. (5) An external process condition has been detected which requires an immediate change in the program execution.

Interrupt Philosophy

Because of the large number and widely varying types of interrupt requests, it is often not desirable to cause a branch to a unique address for each condition. For the same reasons, it is frequently not desirable to cause one branch for all interrupt requests and to require the program to determine the individual request(s) requiring service. Therefore, it is expedient to group the many individual request lines into a lesser number of priority levels. This accomplishes two very important functions: First, it allows all interrupt requests common to a specific interrupt level to have the privilege of interrupting immediately if the only requests present are of a lower priority level. Conversely, it permits interrupt requests connected to a higher priority level to temporarily terminate the servicing on a lower level and to immediately interrupt to the higher priority. Service is returned to the initial request only after all higher level requests have been serviced. Second, since a unique branch can be defined for each interrupt priority level, it is possible to combine many interrupt requests on a common priority level and therefore use a common interrupt subroutine to service many requests.

There are two important operating characteristics of the interrupt system. (1) When more than one request line is connected to any priority level, it is necessary by programming means to identify the individual request(s) causing the priority level to be energized. (2) The first request that is recognized on a given priority level prevents future requests on that or lower priority levels from interrupting until the completion of servicing the first interrupt is signaled by a Branch Out Operation (see Branch or Skip on Condition-BSC). However, interrupts that occur on the same level for which an interrupt is being serviced can be interrogated and serviced by programming if the Interrupt Level Status Word (ILSW) is interrogated again before the "Branch Out" is executed. The ILSW is explained in detail towards the end of this section.

INTERRUPT LEVELS

As shown in Table 6, a maximum of 24 external interrupt levels are available. Twelve external interrupt levels are standard, as are the Internal, Trace, and CE interrupt levels. Note that the priority level of each interrupt, as well as its unique core storage address is listed in decimal form. Note also that all but the Trace and CE interrupts have an Interrupt Level Status Word (ILSW). The ILSW, which is explained in detail later, is used to identify the specific condition causing its interrupt level to request service. No external interrupt can occur at the end of an XIO or BSI instruction (until another instruction is taken).

Internal Interrupt

The Internal Interrupt is a P-C interrupt that occurs when any one of four error conditions occur in the P-C:

- 1. An invalid Op code is detected.
- 2. A parity error (even number of bits) is detected in the B-register during data transfer to or from core storage.
- 3. A storage protect violation occurs from an attempt to write into a "read-only" core storage position.
- 4. CAR Check error occurs either as a CAR Check or as the result of a parity error having caused a command reject.

Table 6. Interrupts

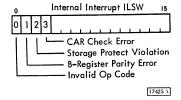
	Priority	Core Storag	e Location		.SW
Interrupt	Level	Decimal	Hex.		
Internal	1	8	8	Yes)	
Trace	26	9	9	No	
** CE	27	10	Α	No	
*External 0		11	В	Yes	
1	2 3 4 5 6 7	12	С	Yes	
2	4	13	D	Yes	
2 3	5	14	E	Yes	
4	6	15	F	Yes }	Basic
4 5		16	10	Yes	
6	8	17	11	Yes	:
6 7	9	18	12	Yes	
8	10	19	13	Yes	
9	11	20	14	Yes	
10	12	21	15	Yes	
11	13	22	16	Yes J	
12	14	23	17	Yes)	
13	15	24	18	Yes	
14	16	25	19	Yes	Special
15	17	26	1A	Yes	Feature
16	18	27	18	Yes	Group 1
17	19	28	1C	Yes)	
18	20	29	1D	Yes)	
19	21	30	1E	Yes	Special
20	22	31	1F	Yes }	Feature
21	23	32	20	Yes	Group 2
22	24	33	21	Yes	ż
23	25	34	22	Yes /	

- * External Interrupt cannot occur at the end of an XIO or BSI instruction.
- ** A CE Interrupt Stores the return link in core location 10 (decimal) and starts execution at core location 0001.

 Interrupts are prevented in the same manner as for the standard forced BSI.

17424 B

The Internal interrupt cannot be masked. However, an XIO or BSI instruction prevents the internal interrupt for one instruction. Its ILSW is reset when it is sensed to determine the interrupting condition. The four error conditions are assigned to the ILSW as follows:



Trace Interrupt

The Trace interrupt occurs after every instruction if the P-C is in program operation with the console mode switch on Trace. The Trace interrupt cannot be masked and does not have an ILSW. However, an XIO instruction prevents a Trace interrupt for one instruction.

CE Interrupt

The CE interrupt can be initiated from the CE panel or from a device operating in CE mode. It cannot be masked and does not have an ILSW. The CE level is not polled on an XIO or BSI instruction

Interrupt Level Masking

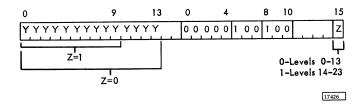
A mask register exists for the masking and unmasking of external interrupt levels. An interrupt level that is masked cannot initiate a request for service until it has been unmasked.

Programmed interrupts will not occur if the corresponding interrupt is masked prior to the time the XIO command for programmed interrupt is executed or before the forced BSI occurs.

Device status words and PISWs are not affected by the mask operation.

The XIO Control instruction is used to simultaneously mask and unmask external interrupt levels 0-13 or 14-23, depending on Modifier bit 15 of the IOCC. Two XIO Control instructions are required to mask/unmask the maximum of 24 external interrupts (All external interrupts are automatically masked when electrical power is first applied to the P-C.) The execution of this instruction does not affect the contents of the A-register.

The IOCC for the Mask instruction is shown below:



Note that the Area is 00000 and that Modifier bits 8-10 must be 100.

The status of Address bit positions 0-13, or 0-9, depending on Modifier bit 15 (Z), determine whether external interrupt levels 0-13 or 14-23 are masked or unmasked:

A 1-bit masks the corresponding interrupt level. A 0-bit unmasks the corresponding interrupt level.

External Interrupt Polling

Two polling cycles are required to sample all 24 interrupt level requests. Interrupt levels 0 through 13 are polled as a group and interrupt levels 14 through 23 are polled as another group. The group that is polled on any given cycle is not readily predictable because the first

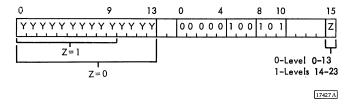
71

group polled after an interrupt will be the group that was being polled when the interrupt occurred. During any core-storage cycle, other than the first core-storage cycle of an instruction, both groups of interrupt levels are polled. Therefore, unmasking an interrupt level for an instruction that takes only one core-storage cycle (MDX, LDX, LDS, etc.), would not poll all 24 interrupt level requests. This one core-storage cycle instruction would poll only one group, and the group could be either 0-13 or 14-23. Polling is inhibited during:

- XIO and BSI instructions.
- Load, display, or IPL modes.
- Clear storage operations.

Programmed Interrupts

External interrupt levels can be programmed. An XIO Control instruction is used to turn on individual external interrupt levels within either of two groups (0-13 or 14-23) depending on the status of Modifier bit position 15 of the IOCC. Two instructions must be executed to turn on interrupt levels in both of these groups. The IOCC is shown below:



Note that the Area is 00000 and that Modifier bits 8-10 must be 101.

The status of Address bits 0-9 or 0-13, depending on Modifier bit 15 (Z), determine whether individual interrupts within priority levels 0-13 and 14-23 will be turned on:

- A 1-bit turns on the corresponding external interrupt level.
- A 0-bit does not turn on the corresponding external interrupt level.

Programmed interrupts will not occur if the corresponding interrupt level is masked prior to the time the XIO command is executed.

If a programmed interrupt level is turned on but the hardware forced BSI instruction has not occurred, an XIO instruction to mask the programmed interrupt level will turn the programmed interrupt level off. Another Programmed Interrupt XIO instruction would be needed to reinitiate the programmed interrupt after the specified level is unmasked.

Programming Note

A BOSC instruction following an XIO instruction which turns on a programmed interrupt for a level as high or higher than the level currently being serviced will reset the programmed interrupt just turned on. For example, while in a routine servicing interrupt level 4 an XIO instruction to set program interrupt to level 2, followed by a BOSC instruction would reset interrupt level 2 and not reset level 4. To prevent this condition the following technique can be used for program set interrupts.

OIX OIX		MSK1 }	Prevent All Interrupts
BOSC		+ -Z	Clear Current Interrupt Level
NOP			,
XIO		UMSKI (Restore Interrupt Mask Register
XIO		UMSK2 }	kestore interrupt Mask Register
XIO		PROGI	Set Program Interrupt
BSC	I	EXIT	Exit Current Level 23412

STATUS WORDS

The I/O devices of the 1800 System and some of the system features contain "status" indicators. The on/off condition of each status indicator reveals to the operating program an operational status or condition of the device in which the indicator is located. Status indicators are also contained in the process being monitored and/or controlled by the 1800 System. These indicators, both system and process oriented, project their individual conditions into the system via the In-Bus. Those process and system indicators assigned to interrupt levels initiate interrupt requests when they are turned on.

The status words used in the 1800 are:

- 1. Device Status Word (DSW) (includes Selector Channel Status Words)
- 2. Process Interrupt Status Word (PISW)
- 3. Interrupt Level Status Word (ILSW)

Device Status Word Indicators

DSW indicators (including Selector Channel Status indicators) usually fall into three general categories:

- 1. Error or exception interrupt conditions.
- 2. Normal data or service required interrupts.
- 3. Routine status conditions.

The DSW indicators are always read into the A-register with a Sense Device instruction. A unique DSW exists for each device, and consists of one or more words. The second word of a Sense Device IOCC specifies the device whose DSW is to be sensed. If the device has more than one word in the DSW, the modifier bits are used to specify the desired word of the DSW.

(See Appendix C.)

Bit 15, of the second word of the IOCC, being 1 specifies reset of the resettable indicators in the word being sensed. A list of the DSWs is in Appendix D.

Process Interrupt Status Word Indicators

The PISW indicators, which are physically located in the 1800 System, are turned on by the closing of a contact or the shifting of a voltage from a customer process.

When an XIO Sense or XIO Read instruction reads a specified PISW, the indicators are unconditionally reset. The difference between the two instructions is where the PISW is stored. A read instruction stores the PISW at the core storage location specified by the first word of the IOCC; the sense instruction stores it in the A-register.

Assignment of PISW Bit Positions

Process interrupts are terminated on 16-position terminal blocks within the 1800 System. The terminating circuitry restricts the assignment of process interrupts to the bit positions within each PISW:

- 1. Terminal block positions 0 through 15 must be assigned to corresponding PISW bit positions 0 through 15. There can be no cross assignment, such as position 0 of the terminal block to position 1 of the PISW. Position 0 must be assigned to position 0, 1 to 1, . . . 15 to 15.
- 2. Terminal block positions can be separated in groups of four and assigned to one, two, three, or four PISW's.

For example, as shown in Figure 18, terminal block positions 0-3 may be assigned to bit positions 0-3 of one PISW; terminal block positions 4-7 may be assigned to positions 4-7 of a second PISW; terminal block positions 8-11 to 8-11 of a third PISW; and terminal block positions 12-15 to 12-15 of a fourth PISW. In like manner, terminal block positions 0-7 could be assigned to 0-7 of one PISW, and terminal block positions 8-15 to 8-15 of a second PISW.

Twenty-four PISW's exist in the 1800. They are addressed individually by the modifier of the XIO Sense Device instruction. PISW decimal addresses in the modifier are 2 through 25.

Interrupt Level Status Word

The Interrupt facility includes one 16-position Interrupt Level Status Word (ILSW) for each interrupt level. (The Trace and CE interrupts are exceptions; they are unique interrupts and require no ILSW.)

The ILSW is always read into the A-register. Each of its bits is assigned to a specific device or PISW on the interrupt level associated with the ILSW. See Figure 19.

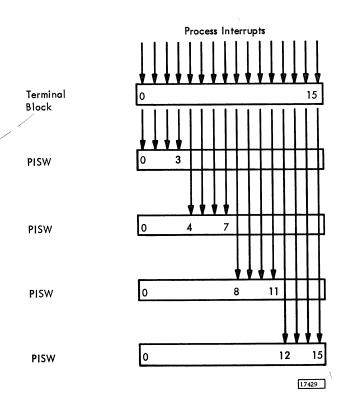


Figure 18. Bit Positions Assignment of PISW's (typical)

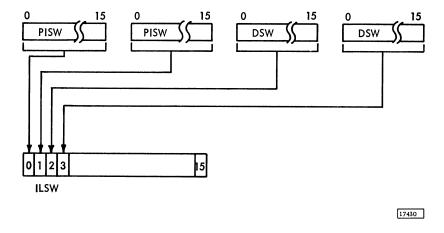


Figure 19. Relationship of Status Words

Each interrupt level requests service when any one of the 16 bits in its ILSW is turned on. When the P-C program recognizes the interrupt request, it executes an XIO Sense Interrupt Level instruction to read the ILSW of the requesting interrupt level into the A-register. The P-C program then determines which bit position in the ILSW caused the interrupt. This bit position identifies the DSW or PISW that has the interrupt initiating indicator. The DSW or PISW is then analyzed by the P-C program to determine which indicator in the DSW or PISW caused the interrupt.

The programmer does not specify the ILSW in the XIO Sense Interrupt Level instruction used to read the ILSW into the A-register. This specification is fixed; that is, each ILSW is hardware assigned to its interrupt level. The Sense Interrupt operation provides the ILSW of the highest priority level requesting service. Except for the P-C Internal interrupts, none of the DSW and/or PISW interrupt indicators ORed into ILSW bit positions are reset when the ILSW is read into the A-register. The indicators are not reset until their respective DSW or PISW is read into the A-register with an XIO Sense Device instruction with reset.

Figure 19 also shows that each PISW may be assigned to one bit position of an ILSW. If this practice were carried to its extreme, all 24 PISW's could be assigned to only two ILSW's, which would restrict all process interrupts to two interrupt levels. Conversely, only one PISW could be assigned to each ILSW, which would provide the maximum number of interrupt levels for process interrupts. Interrupt level assignments for any one Process Interrupt Adapter must be to interrupt levels 0-11 or 12-23.

PROGRAMMED OPERATION

The 1800 System may be programmed to service interrupt requests in several alternative manners:

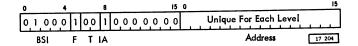
- 1. Process and other interrupts are intermixed on the same level. The ILSW is interrogated first and the PISW is interrogated subsequently.
- 2. Process and other interrupts are intermixed on the same level, but process interrupt is given priority on that level so that the PISW's (typically one) are sensed directly and checked before the ILSW is sensed and checked.
- 3. An interrupt level is completely reserved for process interrupts and interrogation of the ILSW determines which PISW contains the actual interrupt.
- 4. An interrupt level is completely reserved for process interrupts and the number of PISW's on that level is restricted to one. In this case, the program can go directly to the PISW containing the interrupting condition.

In general, an interrupt request is recognized at the completion of the instruction being executed when the interrupt request occurs. Exceptions to this practically instantaneous recognition occur when:

1. The instruction being executed when the interrupt request occurs is either an interrupt forced or normal Branch and Store Instruction Register (BSI) instruction or an XIO instruction. These instructions effectively mask all interrupts during

- their execution and the execution of the next instruction.
- 2. The interrupt request level is masked. The request will be retained by the device adapter in the 1800 System for recognition when the interrupt level is unmasked. (Programmed interrupts are not retained if masked prior to their execution.)
- 3. The interrupt request is of the same or a lower priority level than an interrupt level being serviced.

When an interrupt request is recognized, the P-C inhibits the normal access to core storage and generates into the B-register a BSI Indirect Addressing instruction. The format of this forced hardware instruction is:



Programming Details

The Address of the forced BSI Indirect instruction is unique for each interrupt level, as specified in Table 6. Program operation from this point is shown in Figure 20 and described below. The circled numbers in Figure 20 correspond to the numbered descriptions below:

- 1. The interrupt request occurs during operation of the main line program.
- 2. The forced BSI Indirect instruction stores the contents of the I-register at the Effective Address (EA) of the instruction. The EA is the

- address that the user stores at the interrupt vector. The forced BSI Indirect instruction then branches to the address of the interrupt subroutine (EA + 1).
- 3. The interrupt subroutine stores all data and/or index registers that it will use and then prior to subroutine completion restores the same data and/or index registers.
- 4. The last instruction of the interrupt subroutine is a Branch or Skip on Condition (BOSC) instruction (Bit 9 = 1) that returns the program to the address previously stored at the EA (step 2). This address is the location of the next instruction in the main line program. The BOSC instruction also resets the interrupt level so that other lower priority levels can be recognized.

If a Wait instruction is operative when the interrupt request occurs, the Wait instruction is considered complete when the interrupt request is recognized. Following completion of the interrupt subroutine, the instruction immediately following the Wait instruction will be executed.

Because a number of interrupt requests can be assigned to any one priority level, program analysis of the requesting interrupt level's ILSW is necessary to determine the source of the interrupt request signal. This analysis is accomplished within the interrupt subroutine in the following manner (the numbered descriptions that follow relate to the circled numbers in Figure 20):

5. An XIO Sense Interrupt Level instruction causes the ILSW for the interrupt level being serviced (the highest priority level on) to be read into the A-register. Only the Function of the IOCC need be specified. No other parts

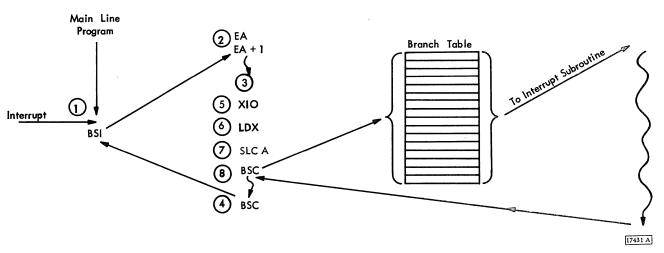


Figure 20. Program Identification of Interrupts

of the IOCC are used. The status of the indicators in the devices assigned to the ILSW are not reset.

- 6. A Load Index Register (LDX) instruction loads an index register with the number of interrupt signals assigned to the ILSW.
- 7. A Shift Left and Count (SLCA) instruction is executed. The resulting count in the index register corresponds to the first non-zero bit of the ILSW in the A-register.
- 8. A BSC instruction is executed. This instruction is both <u>indirect</u> and <u>indexed</u> with the index register containing the count corresponding to the first non-zero bit in the A-register. The Address of the BSC instruction is related to the top word of the Branch Table (Figure 21).

The Branch Table is a table of addresses. Each address is the location of an interrupt subroutine that is related to an interrupt request assignment in the ILSW. Thus, if bit position zero of the ILSW is on, the last word of the table is used, and the BSC branch is to the address stored in the last word of the table.

If bit position one of the ILSW is on, the BSC branch is to the address stored in the second to last word of the Branch Table, etc.

Thus, the above sequence of instructions locates the interrupt subroutine for the ILSW bit that initiated the interrupt. Each time the A-register is shifted, the shift count is decreased by one. As the shift

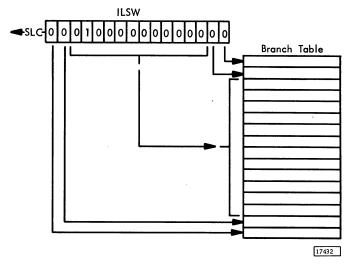
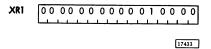


Figure 21. ILSW Branch Table

count is decreased, the indexed address for the BSC instruction is decreased. Effectively, the branch address of the BSC instruction begins at the bottom of the Branch Table and progresses up the Branch Table as the A-register is shifted. For example:

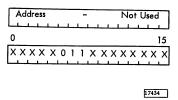
1. Load Index Register

Index Register one (XR1) is loaded with sixteen or the maximum number of interrupt request lines connected to the level which caused the interrupt. (In this example, assume sixteen request lines are connected to the interrupting level.)



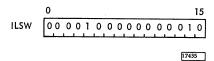
2. Execute I/O (Sense Interrupt Level) An XIO instruction is executed which senses the ILSW of the interrupting level into the Arregister.

3. I/O Control Command



X - Unused bits

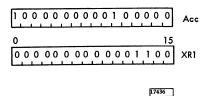
In this example, the ILSW appears in the Aregister as follows:



4. Shift Left and Count

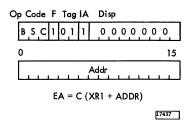
A Shift Left and Count normalizes the A-register and leaves a remainder count in the index register. Note that four shifts have reduced

the value in XR1 from 16 to 12. Also, regardless of the status of bit positions 8 and 9 in the index register, they are set to zero and bit positions 0-7 will be unchanged.



5. Branch or Skip on Condition

An indexed branch instruction with an indirect bit permits a unique branch to a table of addresses which contains an entry for each bit of the accumulator.



Indicator Identification

If the device requesting service is assigned to a DSW or PISW, it is necessary to determine which indicator

in the DSW or PISW is responsible for the interrupt request. This identification can be made in an almost identical manner to the previously described program steps 1 through 8 of Figure 20:

- 1. An XIO Sense Device instruction is executed in step 5 instead of an XIO Sense Interrupt Level instruction. The area and/or modifier must specify the device or the status word.
- 2. The LDX instruction (step 6) loads the index register with the maximum number of indicators assigned to the DSW or the PISW instead of the number of interrupt request signals assigned to the ILSW.
- 3. SLCA and BSC (in steps 7 and 8) should be programmed in such a manner that all possible interrupting conditions are checked; i.e., even if one condition is on, the other conditions are not assumed to be off.

Programming Note

If a subroutine can be called from two or more priority levels there can be a significant problem in the loss of data (return addresses and intermediate subroutine results) unless care in programming is exercised.

Note: If only one device (one interrupt) is on an interrupt level, the program can be written so that only the DSW is sensed into the A-register and its indicators are interrogated. Since only one interrupt is on the interrupt level, the ILSW need not be interrogated.

DATA PROCESSING INPUT/OUTPUT AND COMMUNICATIONS DEVICES

IBM 1053 Printer

IBY 1816 Printer-Keyboard

The IBM 1800 Data Acquisition and Control System offers a wide variety of highly flexible input/output devices:

IBM 1054 Paper Tape Reader
IBM 1055 Paper Tape Punch
IBM 1442 Card Read Punch
IBM 1443 Printer
IBM 1627 Plotter
IBM 1810 Disk Storage

IBM 2311 Disk Storage Drives (attached via a Selector Channel and 2841 Storage Control) IBM 2401/2402 Magnetic Tape Units

In addition, communications devices such as System/360 Adapters, Communications Adapters and 2790 Adapters are available.

INPUT/OUTPUT DEVICES AND CONTROL UNITS

Input/output operations involve the transfer of information to or from main storage and an I/O device. Input/output devices include such equipment as card read punches, magnetic tape units, disk storage, printer-keyboard devices, printers, incremental plotters, communications devices, and process-control equipment.

Many I/O devices function with an external document, such as a punched card or a reel of magnetic tape. Other I/O devices handle only electrical signals, such as communications devices and those devices found in process-control networks. In either case, I/O device operation is regulated by a control (adapter) function. All I/O devices, except 1810, require an adapter and/or controls. Adapters and/or controls for all DP I/O devices, except 2311, are located in the 1801 or 1802. A Selector Channel provides the control functions for a 2841 Storage Control which in turn controls the 2311's. The Selector Channel is located in an 1826 Data Adapter Unit along with adapters and/or controls for System/360 Adapter, Communications Adapters (CA), and 2790 Adapters.

In all cases, the control function provides the logical and buffering capabilities necessary to

operate the associated I/O devices. From the programming point of view, most control functions merge with I/O device functions.

Each control function operates only with the I/O device for which it is designed, but each control function has standard signal connections with regard to the channel to which it is attached which allows it to be attached to a shared channel.

INPUT/OUTPUT INTERFACE

So that the Processor-Controller (P-C) may control a wide variety of I/O devices, all control functions are designed to respond to a standard set of signals. This "I/O unit to P-C" connection is called the I/O interface. It enables the P-C to handle all I/O operations with a common set of instructions.

I/O CONTROL

The IBM 1800 uses two methods to control I/O devices:

Data Channel Control (cycle steal)
Direct Program Control

Data Channel Control

The IBM 1800 Data Channel transfers blocks of data between P-C core storage and the I/O device at a rate controlled by the I/O device. While this transfer is underway, the P-C can continue with the program. The P-C program is delayed one core storage cycle for each word the I/O device reads or writes into or out of core storage. (See Data Channel for Data Channel operations.)

The following devices are under Data Channel Control:

IBM 1442 Card Read Punch IBM 1443 Printer IBM 1810 Disk Storage IBM 2401/2402 Magnetic Tape Units 2790 Adapters CA Line Adapters Selector Channel System/360 Adapter

Direct Program Control

IBM 1800 Direct Program Control transfers individual words of data between P-C core storage and the I/O device at a rate controlled by the program and the I/O device's maximum speed. The P-C program is interrupted for each word transfer. The following steps are performed when the interrupt occurs.

- 1. Branch to an I/O routine where the next word transfer instruction to the I/O device is executed.
- 2. Turn off the interrupt request, and
- 3. Branch back to the normal P-C program.

The following devices are under Direct Program Control:

IBM 1053	Printer
IBM 1054	Paper Tape Reader
IBM 1055	Paper Tape Punch
IBM 1627	Plotter
IBM 1816	Printer-Keyboard

INPUT/OUTPUT INSTRUCTION (XIO)

The IBM 1800 uses only one I/O instruction: Execute I/O. This instruction initiates all I/O operations.

<u>Programming Note:</u> All devices attached to a data channel will treat the XIO instruction as a no-op if the addressed device is busy or not ready.

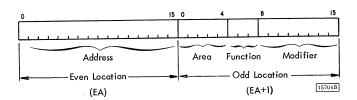
I/O Control Commands

The address portion of the Execute I/O instruction (XIO) specifies the core storage location of a two-word I/O Control command.

Eight I/O Control command functions are provided for the IBM 1800:

Read
Write
Initialize Read
Initialize Write
Control
Sense Device Status Word (DSW)
Sense Interrupt Level Status Word (ILSW)
Set CE Mode

All I/O Control commands have four parts: Address, area, function, and modifier.



Address

The meaning of this 16-bit field is dependent upon the function of the I/O Control command:

- 1. If the function is Initialize Write (101) or Initialize Read (110), the address field specifies the starting address of a table in storage (an I/O Block). This table contains data words and control information (Channel Command Words for the Selector Channel). Initialize Write and Initialize Read functions are used only with data channel control.
- 2. If the function is Control (100), for example, and the area field specifies a disk storage device, the address field may indicate the number of cylinders the actuator must be moved. The function of the address is variable, depending upon the I/O device used.
- 3. If the function is Sense DSW (111) or Sense Interrupt Level (011), the address field is ignored. Instead, an increment of time, equivalent to a core storage cycle, is taken during which the selected I/O device or interrupt level places its status code into the P-C accumulator.
- 4. If the function is Write (001) or Read (010), the address field specifies the core storage location of the data word. These functions are used only with direct program control.

Area

This 5-bit field specifies a unique segment of I/O, which may be a single device (1442 Card Read Punch, 1443 Printer, etc.) or a group of several units (magnetic tape units, printer-keyboard unit, etc.).

Area codes are preassigned by IBM to each type of I/O device that can be ordered for the system. The following is a list of those devices and their codes.

I/O Device	Are	ea Code	
1/ O Device	Decimal	Binary	Hex
Console Operations	0	(00000)	0
1816/1053 Printers (first 4)	1	(00001)	1
1442 Card Read Punch (first)	2	(00010)	2
1054/1055 Paper Tape Units	3	(00011)	3
1810 Disk Storage (first drive)	4	(00100)	4
1627 Plotter	5	(00101)	5
1443 Printer	6	(00110)	6
2790 Adapter (first)	7	(00111)	7
1810 Disk Storage (second drive)	8	(01000)	8
1810 Disk Storage (third drive)	9	(01001)	9
Analog Input	10	(01010)	Α
Digital Input (Digital and Pulse Count)	11	(01011)	В
Digital and Analog Output (DO, ECO, RO, AO)	12	(01100)	U
System/360 Adapter	13	(01101)	D
2401/2402 Magnetic Tape Units	14	(01110)	Е
1816/1053 Printers (second 4)	15	(01111)	F
Analog Input Expander	16	(10000)	10
1442 Card Read Punch (second)	1 <i>7</i>	(10001)	11
Selector Channel	18	(10010)	12
2790 Adapter (second)	19	(10011)	13
Comm Adapter (fourth)	20	(10100)	14
Comm Adapter (first)	21	(10101)	15
Comm Adapter (second)	22	(10110)	16
Comm Adapter (third)	23	(10111)	17

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Function

The eight primary I/O functions are specified by the 3-bit function code:

000 Customer Engineering Mode

> This code is used to place a device in CE mode or to remove a device from CE mode.

001 Write

> This code is used to transfer a single word from core storage to an I/O unit. The address of the core storage location is provided by the address field of the I/O Control command.

010 Read

> This code is used to transfer a single word from an I/O unit to core storage. The address of the core storage location is provided by the address field of the I/O Control command.

011 Sense Interrupt Level This code is used to load the Accumulator with the Interrupt Level Status Word (ILSW) for the highest interrupt level pending at the time it is issued. This command is common to all I/O devices; therefore, no device code is needed. 100 Control

This code causes the selected device to interpret the modifier and/or the address field as a specific control action.

101 Initialize Write

> This code initiates a write operation to a device or unit which will subsequently request data transfers from core storage via a data channel.

110 Initialize Read

> This code initiates a read operation from a device or unit which will subsequently request data transfers to core storage via a data channel.

111 Sense Device Status Word (DSW)

> This code directs the selected device to make its current indicator status available for automatic placement into the P-C accumulator. If area 00000 is specified, the console status or interval timer status may be brought into the P-C accumulator as specified by a unit address code in the modifier field.

Note: The current contents of the P-C accumulator are destroyed by the execution of the following six functions: Read, Initialize Read, Write, Initialize Write, Sense DSW, Sense Interrupt Level. Therefore, it is the programmer's responsibility to save the P-C accumulator contents, if necessary.

Modifier

This 8-bit field provides additional definition for either function or area. For example, if the area field specifies a 1443 Printer, and the function field specifies Initialize Write (101), a particular modifier code specifies the suppress-space operation. In this case, the modifier extends the function. If, however, the area field specifies a group of serial

I/O devices (for example, magnetic tape), and the function specifies Write (001), the particular unit address is specified by the modifier field. In this case, the modifier extends the area.

INPUT/OUTPUT TERMINATION

Input/output operations using devices under direct program control are terminated when the device has completed the single function requested by the program.

Data channel I/O operations are terminated when the end of the last core storage data table has been reached.

INPUT/OUTPUT INTERRUPTS

Input/output interrupts are caused by termination of an I/O operation, by certain error conditions, or by operator intervention at the I/O device. Input/output interrupts enable the P-C to provide appropriate programmed responses to conditions that occur in I/O devices.

Input/output interrupts are assigned priority sequences to allow the most efficient use of all I/O devices.

Conditions responsible for I/O interrupt requests are preserved in the Device Status Word of the I/O devices until they are reset by the P-C executing a Sense DSW instruction with modifier bit 15 set to 1.

Note: The interrupting conditions for each device are listed under each device in the manual.

DEVICE STATUS WORD (DSW)

The 16-bit Device Status Word consists of bit indicators that define the status of the I/O device and its control. The indicators vary from device to device. However, each indicator falls into one of two groups: interrupt indicators and non-interrupt indicators.

As the name implies, interrupt indicators are associated with conditions that interrupt the stored program execution; for example, "operation complete". Non-interrupt indicators are associated with conditions that do not interrupt the P-C program; for example, "Busy" and "Not-Ready."

Programming Note: Since the P-C is much faster than the I/O devices, it is necessary that they operate asynchronously. It is therefore possible to sense the status of a device during the short period of time that the status is being changed.

The following technique should be used to assure that the final status of the device is sensed. The DSW should be sensed with the resetting modifier bit off. When the bit state changes, the sense should be done once more with the resetting modifier bit on; the data from the last DSW sensed should be used as the valid machine condition.

The IBM 1816 Printer-Keyboard (Figure 22) provides a console-keyboard entry and a console-printer output for the Processor-Controller (P-C) of the IBM 1800.

The IBM 1053 Printer (Figure 23) provides additional output typewriter printers for the IBM 1800.

The printer portion of the 1816 is physically and functionally the same as the 1053. Therefore, the printer description and programming are the same for these two units.

A maximum of two 1816's and six 1053's can be attached to the 1800 System, or one 1816 and seven 1053's, or eight 1053's.

All 1053 printers can operate in the overlapped mode; that is, each can print a different message at the same time. The 1816 can be installed up to 50 feet from the P-C. Each 1053 can be installed up to 2000 feet from the P-C.

PRINTER FUNCTIONAL DESCRIPTION

IBM 1053 printers provide output at a maximum rate of 14.8 characters per second. Data to be printed is transferred from core storage to the 1053 by direct program control.

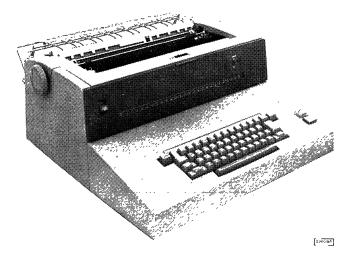


Figure 22. IBM 1816 Printer-Keyboard

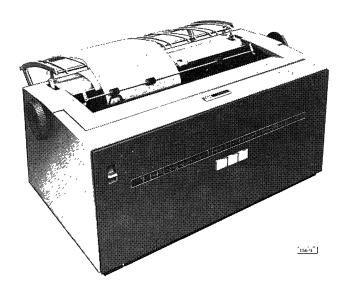
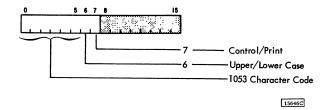


Figure 23. IBM 1053 Printer

Data and control characters (space, tabulate, etc.), are sent to the 1053 by means of the Write command. Because control characters and data characters are sent in the same manner, the message to be printed contains a mixture of data characters and control characters in the sequence necessary to give the desired formatted output.

The character format within a core storage word to be transmitted to the 1053 printer is:



Each word transmitted to the 1053 Printer contains one data character or one control character. Line formatting is programmed by use of the control characters. For example, the carrier return control characters are used at the end of the line in order to return the carriage. If a carrier return control is not given, in some instances data will be over printed in the last column until a carrier

return is given. To prevent this from occurring a carrier return command should be given at the end of each line of print.

The 1053 and 1816 output printer should have a pinfeed platen for continuous forms.

Data Coding

The character coding for input data is shown in Figure 24. The right side of each half of the Figure

shows the binary coding assigned to each input character.

Data to be printed by the 1053 printer is coded by the program into the 1053 code. Figure 25 shows the characters which can be printed by the standard print element for IBM 1053 printers.

The data-character codes also contain (in bit 6) the information as to whether the character is an upper-case (UC) shift or lower-case (LC) shift

Key IBM C	ard Code	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Key IBM Co	ard Code	0	l	2	3	4	5	6	7	8	9	10	11	12 1	3 1	4 1	5
*	11,8,4		1	П				1			Ī	1		Г				J	11,1		1		1									\Box	ight ceil	\rfloor	
/	0,1			1	1													К	11,2		1			1											
0	0		\vdash	1	H									Г	T		П	L	11,3		1				1										
1	1			П	1												Π	М	11,4		1					1	<u> </u>	L				\Box		\perp	
2	2					1								Г			Γ	Ν	11,5		1						1	L							
3	3						1							Γ				0	11,6		1							1				Ц	\perp	\perp	_
4	4					Г		1						Г				Р	11,7		1			L				L	1			Ц	\perp		_
5	5			T					1					Г	Τ			Q	11,8		1									1		Ш			
6	6	T		T	Г	Г				1				Ī				R	11,9		1										1	Ш			
- 7	7	\vdash	T	t	T	T				Г	1			Γ	T	T	T	S	0,2			1		1											_
8	8	Г		T								1		Γ		T	1	Т	0,3			1			1										
9	9		T	T	Γ					T			1	Γ		T		U	0,4	Γ		1				1									
\$	11,8,3		1	T	T	m	1	T				1		T	T	T		٧	0,5			1				Γ	1	I				П			
• (Period)	12,8,3	ī	T	T	T	Г	1			T		1	-	T	Ť	T	1	W	0,6	Ī		1			П		Γ	1				П			
, (Comma)	0,8,3	H	t	1	\vdash	T	1	\vdash		r		1		T	T	T	1	Х	0,7			1						L	1						L
EOF	None	T	\dagger	t	Γ	T	T	1						Ī		I	T	Υ	0,8	L		1		L			L	L		1					_
ER CHR	None	Γ				Γ				Γ					1			Z	0,9			1		L				L			1	Ш			L
ER	None	╁╴	+	T	T	T	r	T	r	T	Г			t	T	Ī		Space	Blank		L							L				Ш	\Box		L
FLD		L	lacksquare	╀	-	Ļ	<u> </u>	ļ	L	_	L	L		L	+	F	4-	¢	12,8,2	1				1				L		1	L				L
=	6,8	L	1	\perp	L	L			L	1	Ļ	1	L	L	1	-	-	<	12,8,4	1						1		L		1					Ĺ
' (Apostrophe)	5,8						L		1		L	1	L	L			_	1	12,8,7	1								L	1	1					L
(12,5,8	1				L	L		1			1		L				&	12	1								L							L
)	11,5,8		1	L		L		L	1	L	L	1	L	L	\perp	1	\perp	!	11,8,2		1			1				L		1					L
+	12,8,6	1	\perp	L	L	L	<u> </u>	_	L	1		1	L	L	\perp	ļ	_	; (Semi-colon)	11,8,6		1			l				1		1					L
– (Dash)	11		1			L	L			L	L	L	L	L		1			11,8,7		1							L	1	1					L
Α	12,1	1			1	L	L		L	L	L	L	L	L	\perp	1	\perp	%	0,8,4			1		Γ		1				1					
В	12,2	1				1			L	L			L	L	L	1	1	(Underscore)	0,8,5		T	1	T	T	T	T	1	T	T	1	Τ	П	П		Γ
С	12,3	1		L	L	L	1	L	L	L	L		L	L	\perp	1	\perp	>	0,8,6	Τ	T	1	Τ	T				1	I	1					
D	12,4	1						1			L		L	l	╧	\downarrow	\perp	?	0,8,7	I	I	1		Ι				I	1	1					[
E	12,5	1						L	1	_	L	L		L			\perp	: (Colon)	8,2					1						1					
F	12,6	1								1		L	L			\perp	\perp	#	8,3	T	T			Ī	1					1					Γ
G	12,7	1		T	Ι						1		L					@	8,4	T		T	T	T	T	1		T		1	Ι	Γ			
Н	12,8	1			I							1			$oldsymbol{oldsymbol{oldsymbol{oldsymbol{\Box}}}$	I		п	8,7					I				I	1	1		\Box			L
1	12,9	1	Τ	T									1					0-8-2	0,8,2			1		Ī	Τ	Ι				1	L	L			L

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Figure 24. IBM 1816 Keyboard Character Coding

ı								wer Case			,
1	во	В1	В2	В3	В4	В5	B6=0	Hexadecimal	B6=1	pper Case Hexadecimal	B7
-	0	0	1	1	1	1	Á		+		
-	0	0	Ö	i	1	0	B	3C 18	A B	3E 1A	0
- 1	ō	ō	ō	i	i	ì	c	1C	c	1E	0
١	0	0	1	i	Ö	Ö	Ď	30	Ď	32	ő
-	0	0	1	1	0	1	E	34	E	36	ō
-	0	0	0	1	0	0	F	10	F	12	0
-	0	0	0	1	0	1	G	14	G	16	0
1	0	0	1	0	0	1	Н	24	Н	26	o'
-	0	0 1	1	0	0	0	ı.	20	1	22	0
		-	1	1	1	1	J	7C	J	7E	0
1	0	1	0	1	1	0	K	58	K	5A	0
1	0	1	0 1	1 1	1 0	1	L	5C 70	L	5E	0
١	0	i	i	i	0	1	N	70 74	N	72 76	0
١	0	i	ò	i	Ö	ö	Ö	50	Ö	52	0
1	0	1	0	1	0	- 1	Р	54	P	56	0
١	0	i	1	Ō	0	i	Q	64	Q	66	0
1	0	1	1	0	0	0	R	60	R	62	ō
١	1	0	0	1	1	0	S	98	S	9A	0
ı	1	0	0	1	1	1	T	9C	Т	9E	0
١	1	0	1	1	0	0	U	во	U	B2	0
1	1	0	1 0	1	0	1 0	<u></u>	B4	V	B6	0
1	i	Ö	Ö	i	0	ĭ	W X	90 94	W X	92 96	0
١	i	ō	ì	ò	ŏ	- i	Ŷ	A4	Ŷ	A6	0
1	1	0	1	0	0	0	z	Α0	z	A2	ō
	1	1	1	1	1	1	ı	F.C	,		
ı	i	i	Ö	i	i	6	2	FC D8	(FE DA	0
١	1	1	Ō	i	i	i	3	DC	<	DE	0
1	1	1	1	1	0	0	4	F0	-	F2	ō
	1	1	1 0	1	0	1	5	F4	7	F6	0
						0	6	D0	;	D2	0
1	1	1 1	0	1	0	1	7	D4	*	D6	0
1	1	1	i	0	0	1 0	8	E4	′.	E6	0
١	i	i	0	0	0	ĭ	9	E0 C4	ï	E2 C6	0
l	1	i	Ō	ō	Ö	o l	0	co	=	C2	0
	1	0	1	1	1	1	1	BC	_	BE	ŏ
1	1	0	0	0	0	1	-	84	?	86	0
	1	0	0	0	0	0	,	80		82	ŏ
	0	1	0	0	0	1	&	44	: > ! %	46	0
	0	1 0	0	0	0	0	\$ @	40	!	42	0
	0	0	0	0	0	6		04 00		06 02	0
1		-	-	-	-		.	••	¢	V2	۱ ۲
_											

Figure 25. IBM 1816/1053 Printer-Character Coding

character. The printer shifts automatically as required for each data character.

A 1053 Printer Write command is modified by the bit 7 position of the output character word. If bit 7 equals 1, the Write command is interpreted as a control function. If bit 7 equals 0, the Write command is interpreted as a print function.

The codes for 1053 Printer control functions are shown in Figure 26.

Note: When alphameric data is the output, programs should be written using LC mode alpha characters since any shifting adds from 60 to 70 ms to the print time.

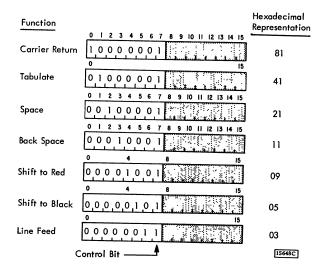


Figure 26. Printer Function Codes

PRINTER PROGRAMMING

The 1053 Printers operate on the IBM 1800 under direct program control.

I/O Control Commands (IOCC)

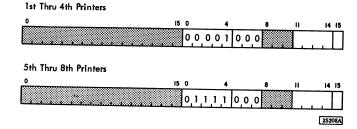
The first four printers are addressed by the 5-digit area code of 1 (00001). The second four printers are addressed by the 5-digit area code of 15 (01111). The modifier bits 11-14 address specific printers in a write, CE mode, or sense DSW operation.

B14 - 1st or 5th printer B13 - 2nd or 6th printer B12 - 3rd or 7th printer B11 - 4th or 8th printer

Note: Printers 1 and 5 may be either 1816 Printer-Keyboards or 1053 Printers. Typewriters 2-4, 6-8 are 1053 printers.

CE Mode (000)

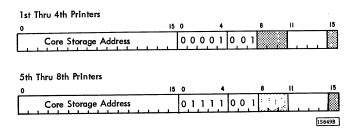
25198



This command places the specified 1053 printers (and keyboard if 1816 is specified) in CE mode if

modifier bit 15 is on, or removes them from CE mode if bit 15 is off.

Write (001)

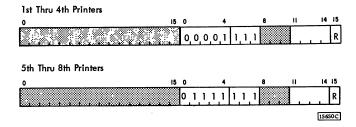


This command causes the P-C word at the core storage location specified by the address field to be sent to the specified 1053 printers for printing or control.

If two or more printers are addressed all those addressed will print the same data simultaneously. At least one 1053 printer must be addressed.

Note: A console-printer (1816) can only be addressed by modifier bit 14; a type-writer-printer (1053) can be addressed by any of the modifier bits B11 to B14.

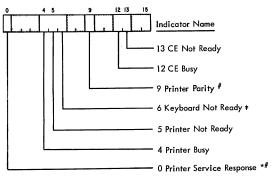
Sense DSW (111)



This command causes the Device Status Words of the selected printers to be ORed together and then placed in the PC accumulator. This command also resets the indicators on the selected printers if bit 15 is set to 1. There is one Device Status Word for each 1053 Printer (Figure 27), and one for the 1816 (Figure 29).

R=1 Resets indicators.

R=0 Does not reset indicators.



* Interrupt .

Indicator reset by a sense DSW.

(Other indicators are reset by their status turnoff).

Always on when first or fifth printer is a 1053.

15651 D

Figure 27. Device Status Word (1053)

Note: If the 1816 Printer-keyboard is specified, the indicator bits for the console-keyboard are also ORed into the DSW. If bit 15 of the DSW is a 1, the indicators will be reset.

Interrupt Indicator

There is only one interrupt associated with each 1053 Printer.

All typewriters within a group of four(1-4 or 5-8) must be assigned to the same priority level of interrupt and each typewriter within that group must have its interrupting DSW bits assigned to a unique ILSW bit associated with that interrupt level.

Printer Service Response: This interrupt occurs each time a printer has completed printing the data or the control operation specified by the last Write command.

Non-Interrupt Indicators (DSW)

The following indicators are associated with each 1053.

<u>Printer Busy</u>: When on, this indicates that the printer is in the process of typing a character or executing a control and therefore should not be given a Write command. The busy line is active from the time data is sent to the 1053 printer until the printer has completed the action required.

Note: The Printer Not Ready indicator will always be on when the Busy indicator is on.

Printer Not Ready: When off, this indicates that the printer is properly loaded with forms, has de power, is not in CE mode, and is not busy. It is necessary that the program always determine that the Printer Not Ready (or CE Not Ready) indicator is off before a write command is given. If a Write command is given while the Not Ready indicator is on, loss of information will probably occur. No indication is given of this loss.

If the Not Ready indicator is tested and found to be on, Busy should then be tested. If Busy is off, operator intervention is required unless the 1053 is in CE mode. However, the Not Ready indicator on and Busy on, indicates that the printer has not finished execution of the previous Write command.

Printer Parity Error: This indicator is turned on when a parity error is detected in the character transmitted from the P-C.

CE Busy: In the CE mode (000), this indicator is used in place of the Printer Busy indicator. All conditions defined in the Printer Busy status are applicable to this indicator in the CE mode only. Programs utilizing the CE mode use this indicator instead of the Busy indicator.

CE Not Ready: In the CE mode (000), this indicator is used in place of both the Keyboard Not Ready and the Printer Not Ready indicators. All conditions defined for both the Not Ready indicators are applicable to this indicator in the CE mode only. Programs utilizing the CE mode use this indicator instead of Printer Not Ready or Keyboard Not Ready.

KEYBOARD FUNCTIONAL DESCRIPTION

The input speed of the IBM 1816 Printer-Keyboard is 20 characters per second but is usually limited by the speed of the operator. Keyboard entries are not automatically printed. The P-C must be programmed to provide an output of the Keyboard entry on the printer. The keyboard emits a coded character for each key struck by the operator. These characters are related to IBM card coding. Striking the A character key places bits in positions 0 and 3 of the P-C word; striking the I character key places bits in positions 0 and 11 of the word; striking the 9 character key places a bit in position 11 of the word; etc. The input code for each character is shown in Figure 24.

The position and arrangement of the various keys are shown in the keyboard layout (Figure 28).

The Power On switch on the 1816 front panel must be left on for printer operation.

Keyboard Function Keys

KBD REQ (Keyboard Request): This key causes an interrupt in the P-C and turns the Proceed light off.

EOF (End of Field): When the P-C reads in response to this key, a word containing a 12-bit only is placed in memory. Analysis of this word allows the program to determine that no further characters are to be sent in this message.

ER CHR (Erase Character): When the P-C reads in response to this key, a word containing a 13-bit only is placed in memory. Analysis of this word allows the program to determine that the last character received is to be replaced by the next character to be entered.

ER FLD (Erase Field): When the P-C reads in response to this key, a word containing a 14-bit only is placed in memory. Analysis of this word allows the program to determine that the message being entered is to be deleted and replaced by a corrected message.

Mode: There are two mode keys: Numeric (NUM) (upper case shift) and Alphabetic (ALPHA) (lower case shift). These keys place the keyboard in the indicated mode. The keyboard remains in the selected mode until changed. If the numbers or symbols which appear on the top portion of the keys are desired, the keyboard must be placed in Numeric mode.

REST KBD (Restore Keyboard): This key allows the operator to restore the keys if they should become locked. System Reset from the P-C console also unlocks the keyboard.

Keyboard Lights

<u>Proceed</u>: This light comes on when the P-C has performed a Control command. This light goes off when a Read command is performed or 25 ms after a key is pressed (when keyboard service response interrupt is given).

ALPHA: When ALPHA is illuminated, it indicates that the keyboard is in the Alphabetic mode (lower case shift).

NUM: When NUM is illuminated, it indicates that the keyboard is in the Numeric mode (upper case shift).

Operating Procedure

The following procedure describes a typical use of the keyboard.

- 1. Unlock keyboard by pressing Restore key.
 The program initializes by issuing an XIO
 read to turn Proceed light off (DSW keyboard
 not ready off).
- 2. Press KBD REQ key. Key locks down. Keyboard is locked. After 25 ms, request interrupt is set.
- 3. The program is interrupted and Sense DSW notes that request bit is on. (Sense DSW uses bit 15 to turn off request).
- 4. The program does XIO control. Proceed light turns on (DSW goes keyboard not ready).
- 5. At the end of 25 ms keyboard is unlocked and restored and the Proceed light is turned on (DSW goes keyboard not ready).

- 6. Operator presses any character keyboard key. Key locks down and keyboard is locked. After 25 ms the Proceed light is turned off (DSW keyboard not ready is off) and a Service Interrupt is set.
- 7. One key is now down, the keyboard is locked, and Proceed light is off (DSW keyboard not ready is off).
- 8. The program is interrupted and sense DSW notes that service bit is on. (Sense DSW uses bit 15 to turn off service interrupt).
- 9. The program does XIO read. If parity error is detected, program reads again.
- 10. Return to step 4. (Replace "KBD REQ" with "Character").

PROGRAMMING

The keyboard operates under direct program control of the IBM 1800.

I/O Control Commands (IOCC)

The Printer-Keyboard is addressed by the same area code used by the IBM 1053 printers, modified by a 1 in the bit 14 position of the IOCC.

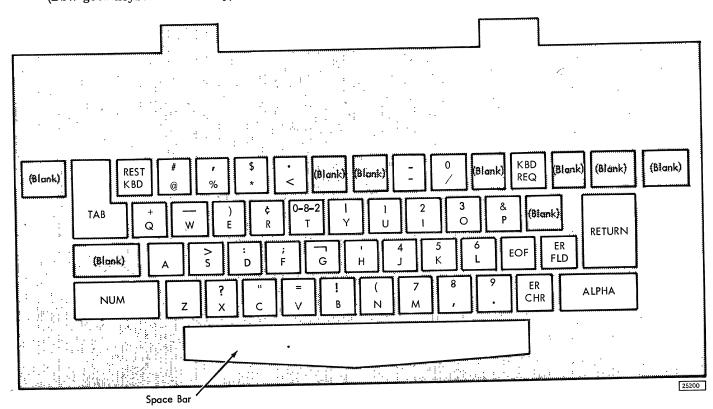
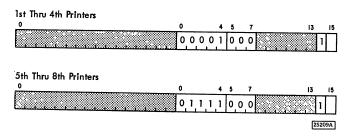


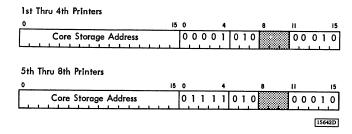
Figure 28. Keyboard Layout

CE Mode (000)



This command places the 1816 printer-keyboard in the CE mode if modifier bits 14 and 15 are on or removes it from CE mode if bit 14 is on and 15 is off.

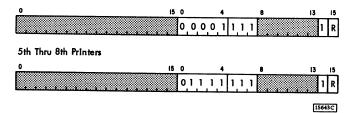
Read (010)



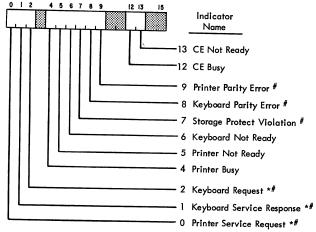
This command enters a single input character from the keyboard into the P-C storage location specified by the address of the IOCC and turns off the Proceed light. The character can be re-read if desired.

Sense DSW (111)

1st Thru 4th Printers



This command reads the Device Status Word (Figure 29) associated with the 1816 keyboard-printer into the Processor-Controller. Modifier bit 14 must be a 1 to select the keyboard.



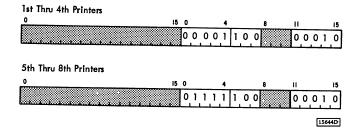
- * Interrupt
- Indicator reset by a sense DSW (Other indicators are reset by their status turnoff)

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Figure 29. Device Status Word (1816)

Modifier bit 15 specifies whether the indicator bits are to be reset: no reset if 0; reset if 1. Any console printer indicators which are on, will be reset at the same time.

Control (100)



This command places the keyboard in a proceed status so that a character can be entered. This command also turns on the Proceed light and unlocks the keyboard.

Interrupt Indicators

The two interrupts associated with the keyboard are internally ORed together with the 1816 printer interrupt as a single interrupt to be assigned to a priority level of external interrupt and to a unique ILSW bit.

Printer Service Response: This interrupt occurs each time a printer has completed printing the data or the control operation specified by the last Write command transmitted.

Keyboard Service Response: This interrupt signals that a character key has been pressed and that a character is ready to be entered into core storage.

<u>Keyboard Request</u>: This interrupt is initiated by the Request key located on the keyboard.

Non-Interrupt Indicators (DSW)

Printer Busy: When on, this indicates that the printer is in the process of typing a character or executing a control and therefore should not be given a Write command. The busy line is active from the time data is sent to the printer until the printer has completed the action required.

<u>Note</u>: The Printer Not Ready indicator will always be on when the Busy indicator is on.

Printer Not Ready: When off, this indicates that the printer is properly loaded with forms, has do power, is not in CE mode, and is not busy. It is necessary that the program always determine that the printer not ready (or CE not ready) indicator is off before a write command is given. If a write command is given while the Printer Not Ready indicator is on, loss of information will probably occur. No indication is given of this loss.

If the Printer Not Ready indicator is tested and found to be on, Busy should then be tested. If Busy is off, operator intervention is required unless the 1053 is in CE mode. However, the Printer Not Ready indicator on and Busy on indicates that the printer has not finished execution of the previous Write command.

Keyboard Not-Ready: When off, this indicates that the keyboard is attached, has do power, is not in CE mode, and is not busy. The keyboard is normally not ready from the time a keyboard control is given until the keyboard service interrupt is issued, which is 25 milliseconds after a character key has been pressed. This indicator is always on if there is no 1816 attached in the first or fifth position.

It is necessary that the program always determine that the Printer Not Ready indicator is off before a Control or Read command is given. Otherwise, loss of information may occur. No indication is given of this loss.

Storage Protect Violation: This indicator is turned on if there is an attempt to read data from the keyboard into a storage-protected core location.

Keyboard Parity Error: This indicator is turned on if a parity error is detected by the P-C in the received character during an XIO Read instruction.

Printer Parity Error: This indicator is turned on when a parity error is detected in the character transmitted from the P-C.

<u>CE Busy</u>: In the CE mode (000), this indicator is used in place of the Printer Busy indicator. All conditions defined in the Printer Busy status are applicable to this indicator in the CE mode only. Programs utilizing the CE mode use this indicator instead of the Printer Busy indicator.

CE Not Ready: In the CE mode (000), this indicator is used in place of both the Keyboard Not Ready and the Printer Not Ready indicators. All conditions defined for both the Not Ready indicators are applicable to this indicator in the CE mode only. Programs utilizing the CE mode use this indicator instead of Printer Not Ready or Keyboard Not Ready.

The IBM 1442 Card Read Punch (Model 6 or 7) provides card input/output for the IBM 1800. One or two 1442s can be connected to the 1800 system.

Reading and punching of the card by the Card Read Punch are under Data Channel control.

FUNCTIONAL DESCRIPTION

The IBM 1442 Card Read Punch (Figure 30) is a single unit that processes cards serially, column-by-column from a single supply hopper. All cards first pass the read station, then pass the punch station.

Maximum machine speeds are:

Operation	Model	Speed
Read	6	300 cards per minute
_	7	400 cards per minute
Punch	6	80 columns per second
	7	160 columns per second

Maximum reading rates are attained only when successive initialize Read commands arrive early

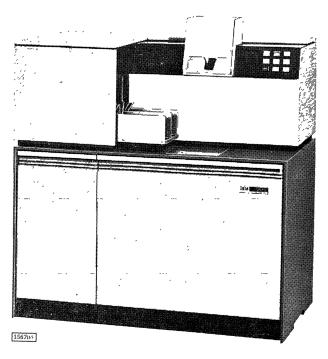


Figure 30. IBM 1442 Card Read Punch

enough to re-energize the read clutch before the clutch latch point is reached. To accomplish this, successive Initialize read commands must arrive within 35 milliseconds (25 ms Model 7) after the operation complete interrupt is given by the Card Read Punch. If an initialize read command does not arrive within this time, the maximum reading rate becomes 285 cards per minute (cpm) for Model 6 and 375 cpm for Model 7.

Punching rates depend on the position of the card when the last column is punched. The punching speed ranges are:

Model 6 - 49 cpm to 262 cpm Model 7 - 91 cpm to 355 cpm

The approximate time required to process a single card is:

Model 6 - 216 ms + 12.5 ms for each card column spaced or punched.

Model 7 - 163 ms + 6.25 ms for each card column spaced or punched.

Last Column Punched	Punch Tir	me (ms)	Total Pur Cycle Ti		Cards per Minute				
	Model 6	Model 7	Model 6	Model 7	Model 6	Model 7			
1	13	6	229	169	262	355			
10	125	63	341	226	176	265			
20	250	125	466	288	127	208			
30	375	188	591	351	102	171			
40	500	250	<i>7</i> 16	413	84	145			
50	625	313	841	476	71	126			
60	750	375	966	538	62	112			
70	875	438	1091	601	55	100			
80	1000	500	1216	663	49	.91			

23095A

Data Channel Assignment

If two 1442s are attached to the system, they should be connected to different Data Channels for simultaneous operation.

Data Coding

The Card Read Punch reads in either card image or packed mode and punches in card image only. Any combination of bits may be read or punched; therefore any code translation required must be done by the stored program.

Card Image Mode: The twelve rows (12-9) in a card column correspond to the bits 0-11 respectively in core storage (Figure 31). Bits 12-15 are set to zero.

Packed Mode: Rows 12-5 of the odd-numbered columns are stored in core storage as bits 8-15 (rows 6-9 are ignored); rows 12-5 of the even-numbered columns are stored in core storage as bits 0-7 (Figure 32).

Initial Program Load Mode (IPL): A special mode is initiated by pressing the Program Load Key on the Processor-Controller console. In the initial program load mode, 40 words of data enter core storage in the packed mode starting at location 000. Following this load action, the P-C branches to location 000 and begins program execution. The Mode switch should be in RUN or SI W/CS mode. The first 1442 is wired for IPL.

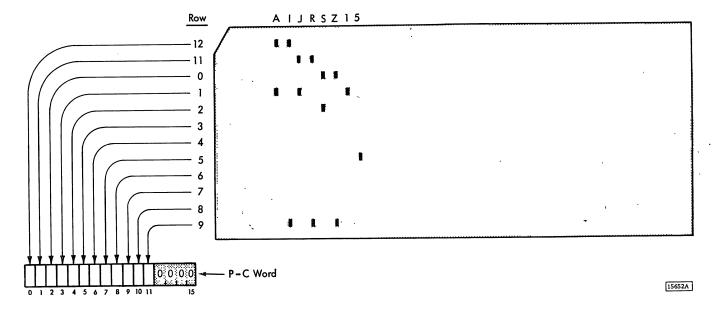


Figure 31. Card Image, Read or Punch (1442)

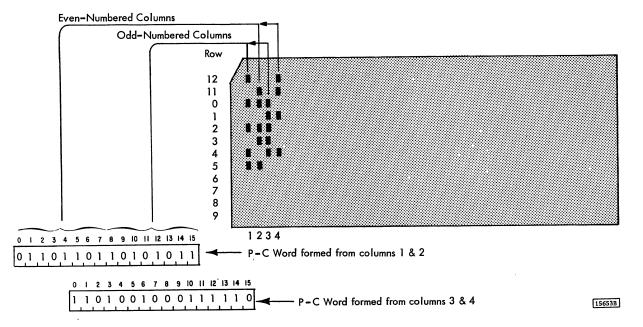


Figure 32. Packed Mode Read (1442)

Functional Keys

Start Key:

- 1. When initially loading the Card Read Punch, pressing the Start key causes the bottom card in the hopper to move to the read station (run in) and restores ready status.
- 2. After manually stopping the Card Read Punch, or when initiating a last-card routine, the Start key restores the ready status.

Stop Key: This key removes the Card Read Punch from the ready status. If card I/O is in process, it is necessary to hold the key down until the Operation Complete interrupt is given; otherwise the 1442 will not recognize that the Stop key has been pressed.

Non-Process Runout Key: This key is used to eject cards from the serial path without processing them and also resets the error conditions. The key is effective only if the hopper is empty. However, if the key is held depressed when the hopper goes empty during card operations, the operation complete interrupt for the card being processed is not given.

Indicator Lights

Power On Light: This light indicates that ac power is supplied to the card punch.

Chip Box Light: This light indicates that the punch chip box is either full or has been removed. This condition removes the 1442 from the ready status.

Ready Light: This light indicates that the Card Read Punch is prepared to accept instructions from the processor. The following conditions are required:

- 1. Power on.
- 2. Card properly registered at the read station.
- 3. Either cards in the hopper or Card Read Punch in the last-card routine.
- 4. Stacker not full.
- 5. Check light off.
- 6. Chip box light off.

Check Light: Indicates that one of the eight error conditions exists. These are displayed on the backlighted panel of the 1442 and are listed below. Any of these error conditions removes the 1442 from the ready status and can be reset only by pressing the Non-Process Runout key with the hopper empty.

<u>Data Overrun</u>: Indicates that data was lost because the channel failed to transfer the data to or from core storage within the time the 1442 required service. Read Registration Check: Indicates that a read error has occurred due to incorrect registration of the card or failure of the first and second reading of a column to compare equally.

<u>Punch Check:</u> Indicates that a punching error has been detected. Punching into prepunched columns does not cause a punch check.

<u>Hopper:</u> Indicates that a card failed to pass properly from the hopper to the read station.

Transport: Indicates a jam in the stacker.

<u>Feed Check – Read Station</u>: Indicates a card improperly positioned at the read station.

<u>Feed Check</u> - Punch Station: Indicates a card improperly positioned at the punch station.

<u>Feed Clutch</u>: Indicates that a feed cycle was taken that was not requested.

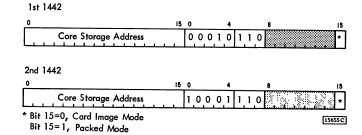
Power Down

If a card is under the punches when the 1442 is powered down, it may be punched in one column. To prevent this, the cards should run out and the unit made not ready prior to powering down.

PROGRAMMING

The IBM 1442 Card Read Punch operates on the IBM 1800 under Data Channel control. The Initialize Read, Initialize Write, Control, and Sense operations are initiated by an XIO instruction that specifies one of the following IOCC control words:

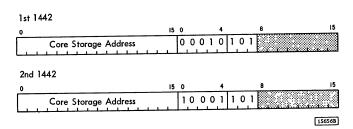
Initialize Read Command (110)



This command causes 80 columns of data to enter core storage, through cycle stealing, starting at the

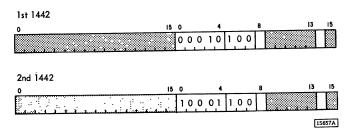
specified core-storage address. If bit 15 is a zero, the data enters core storage at a specified address and the next 79 locations. If bit 15 is a 1, data is entered in the packed mode into the specified corestorage location and the next 39 locations.

Initialize Write Command (101)



This command causes the data starting in the core storage location, specified by the Address of the IOCC, to be transmitted and punched as card column images in the card. The last data word to be punched is indicated by a 1 bit in bit 12 of that data word.

Control Command (100)



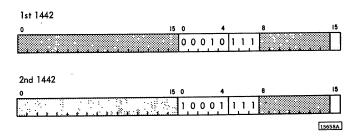
The control command causes the Card Read Punch to accomplish the function specified by the modifier.

Modifier bits that have significance are:

- B14 Feed cycle causes the card to move through the read station without reading, ejects any card in the punch station, and moves a card from the hopper to the read station. There are no cycle-steal requests.
- B8 <u>Stacker Select</u> causes the card leaving the punch area to enter the

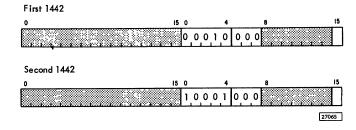
alternate stacker. This control applies only to the next card leaving the punch station. It does not turn on the Busy indicator or cause an interrupt.

Sense DSW (111)



This command directs the Card Read Punch to place its Device Status Word (Figure 33) into the P-C accumulator. Modifier bit 15 specifies whether the DSW indicators are to be reset: 0 if no reset, 1 if reset.

CE Mode (000)



This command places the Card Read Punch in CE mode if modifier bit 15 is on or removes it from CE mode if modifier bit 15 is off.

Interrupt Indicator

There is one interrupt associated with the 1442.

Operation Complete: This interrupt occurs after a card has been read or fed. It indicates that column 80 of the card has passed the read station. This interrupt occurs 20.6 ms after column 80 for the Model 6 and 15.4 ms after column 80 for the Model 7.

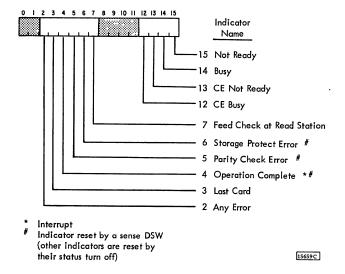


Figure 33. Device Status (1442)

This interrupt also occurs after the last column to be punched has been punched and checked with the punch drive stopped. This will occur 12.5 ms after the last column punched for the Model 6 and 6.25 ms for the Model 7.

The Operation Complete interrupt also occurs if a new XIO command is given after the operation complete for the previous operation but before one of the following errors is detected: transport, hopper misfeed, feed check-punch station, and feed clutch.

Non-Interrupt Indicators (DSW)

Any Error: Indicates that one or more of the following error conditions exist:

- 1. Parity Check Error (described below).
- 2. Storage Protect Error (described below).
- 3. Feed Check at Read Station (described below).
- 4. Data Overrun indicates that data was lost because the channel failed to transfer the data to or from core storage within the time the 1442 required service.
- 5. Read Registration Check indicates that a read error has occurred. This can result from incorrect registration of the card or failure of

- the first and second reading of the column to compare equal.
- 6. Punch Check indicates that a punching error has been detected. Punching into prepunched columns does not cause a punch check.
- 7. Hopper* indicates card failed to pass properly from the hopper to the read station.
- 8. Transport* indicates a jam in the stacker.
- 9. Feed Check at Punch Station* indicates a card improperly positioned at the punch station.
- 10. Feed Clutch* indicates the 1442 took a feed cycle which was not called for.

<u>Last Card</u>: This indicator shows that column 80 of the last card has passed the read station and that the hopper and read station are empty.

Parity Check Error: This indicator is turned on when a transfer to or from the B-register has resulted in a word not having correct odd bit parity. The parity check error does not remove the 1442 from the ready status and is reset by a sense DSW function with modifier bit 15 on.

Storage Protect Error: This indicator is turned on when the 1442 attempts to read into a storage location previously defined as a storage-protected area. The storage protect error does not remove the 1442 from the ready status and is reset by a sense DSW function with modifier bit 15 on.

Feed Check at Read Station: Indicates that a card is improperly positioned at the read station.

CE Busy: In CE mode this indicator is used in place of the 1442 card reader busy indicator.

CE Not Ready: In CE mode this indicator is used in place of the 1442 card reader not ready indicator.

Busy: The Busy indicator indicates that any command other than sense cannot be initiated because an Initialize Read, Initialize Punch, or Feed operation is already in progress.

Not Ready: This indicator shows that the 1442 is not ready, is busy, or is in CE mode. If not ready, manual intervention is required to ensure that these conditions are met:

^{*}Error indicator is not turned on until after the operation complete interrupt, unless the operation was an Initialize Write requiring an automatic feed cycle. If another operation is initiated before the error indicator is turned on, these errors force an Operation Complete although no reading or punching has taken place.

CE Not Ready: In CE mode this indicator is used in place of the 1442 card reader not ready indicator.

Busy: The Busy indicator indicates that any command other than sense cannot be initiated because an Initialize Read, Initialize Punch, or Feed operation is already in progress.

Not Ready: This indicator shows that the 1442 is not ready, is busy, or is in CE mode. If not ready, manual intervention is required to ensure that these conditions are met:

- 1. Power on.
- 2. Card registered at read station (initially).
- 3. Cards in hopper or last-card sequence in progress.
- 4. Stacker not full.
- 5. Check light off.
- 6. If the Stop key has been pressed, the Start key must have been subsequently pressed.
- 7. Chip box not full or removed.

READ AND PUNCH OPERATIONS

Before any operation can begin, the Card Read Punch must be placed in the ready condition. With power on and cards in the hopper, the Start key is pressed; this feeds the first card into position at the read station (Figure 34).

Card Feeding

After the initial feed cycle (run in), card reading or punching may begin. A constant-speed drive moves the cards through the serial path during a feed cycle.

A feed cycle is initiated by a Control command (Feed Card), by an Initialize Read command, or by an Initialize Punch command (if there is no card at the punch station). The feed cycle does three things:

- 1. It moves a card from the punch station to the stacker.
- 2. It moves a card through the read station and places it in the punch station with column 1 under the punches.
- 3. It moves a card from the hopper to the read station.

An incremental drive moves the card through the punch station for punching without moving cards in the hopper or read station. An empty hopper leaves the machine in such a status that the operator can

either reload the hopper and continue operations or he can initiate a last-card sequence.

Card Read (Card Image Mode)

Card reading is initiated by an Initialize Read command with bit 15 equal to 0. This causes columns 1-80 of the card to be read in one continuous motion. Each column of data is read, placed in the data register, and checked. A cycle-steal request is sent to the P-C to request a data transfer. An Operation Complete interrupt is sent to the P-C after all 80 columns have been read.

Card Read (Packed Mode)

Card reading is initiated by an Initialize Read command with bit 15 equal to 1. This causes punch positions 12-5 of the odd-numbered columns to be read and transferred to P-C data word bits 8 through 15. Punch positions 12-5 of even-numbered columns are read and transferred to P-C data word bits 0 through 7. A cycle-steal request is sent to the P-C after every even-numbered column is read. An operation Compete interrupt is sent to the P-C after column 80 has been read.

Initial Program Load (IPL)

The Initial Program Load reads, stores, and initiates a program. The IPL reads each column as packed mode into core storage locations 0000-0039. After the load-card has been stored, beginning at core storage location 0000, the P-C begins execution of the instruction at 0000.

Card Punch

Card punching is initiated by an Initialize Write command. A card is fed to the punch station only if no card is at the punch station or if the card at the punch station has been previously punched. A cyclesteal request is then sent to the P-C to request data transfer. As the data is punched, it is checked and another cycle-steal request is initiated to get the data for the next column. The Operation Complete interrupt is initiated when a data word to be punched contains a 1 bit in bit 12. If a 12 bit is not detected, more than 80 characters may be punched, and no interrupt will occur.

To eject a punched card to the stacker, a Control (Feed Card), an Initialize Read, or another Initialize Write command must be given. These commands advance all the cards in the serial path.

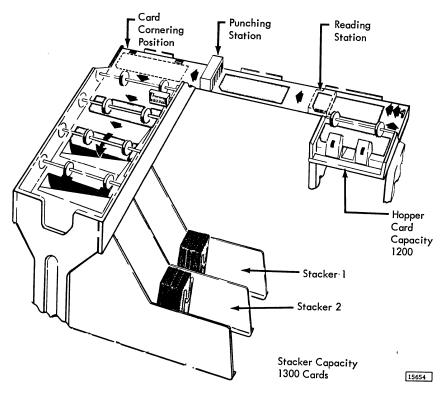


Figure 34. 1442 Card Path

Last-Card Sequence

When the hopper becomes empty during a feed cycle, the Card Read Punch is taken out of ready status.

The operator may continue processing cards by loading more cards into the hopper and pressing the Start key, or he may initiate a last-card sequence by pressing the Start key without loading more cards in the hopper. When the Start key is pressed without cards in the hopper but with a card in the read station, the 1442 is placed in the ready condition and allows two more feed cycles to be taken. No Operation Complete is given at the end of the second feed cycle.

If the last-card sequence has been entered, the program determines this through the Last Card indicator in the Device Status Word. This indicator is turned on after the last card has passed the read station (first feed cycle) and remains on until a second feed cycle has been taken.

Error Recovery

Error recovery requires the cooperation of the operator and the programmer as indicated in the following examples:

- 1. If the error is parity or storage protect, the 1442 does not drop out of ready, does not turn on an error light, and does not stop transmission of data. Therefore the program will have to inform the operator of the error before the cards can be repositioned and the operation reinitiated.
- 2. If the error is hopper, the card at the punch station has not been punched and the card in the hopper has not been read or fed. If the command was Initialize Punch, the card at the punch station can be placed in the hopper and the I/O command given again. If the command was a Feed (to eject the card at the punch station before giving a Punch command), the card at the punch station should not be placed in the hopper unless the program is prepared to give two Feed commands before giving a Punch command.

Therefore the program may need to detect the difference between an I/O operation completed incorrectly (example 1) and an I/O operation not even initiated (example 2).

 If the command given was a feed-cycle Control, the operation was completed incorrectly if the

- feed-check at read station indicator is on in the DSW; otherwise the operation was not initiated.

 If the command given was an Initialize Read,
- 2. If the command given was an Initialize Read, the operation was completed incorrectly if the parity, storage protect, or feed-check at read station indicator is on in the DSW. Otherwise, the core locations read into must be examined: If a column was read, the operation was completed incorrectly because of an overrun or read registration check; if no column was read, the operation was not initiated because of a hopper, transport, feed check at punch station, or feed clutch error.
- 3. If the command given was an Initialize Punch, the card was incorrectly punched if the overrun or punch check occurred. If the feed-check at read station indicator is on, punching was not initiated although the automatic feed cycles did

eject the card that was at the punch station. The program cannot detect the difference between a punch check (card punched incorrectly) or one of the other four feed checks (card not punched).

1442 Usage Meter

This meter runs when the following conditions are present:

- 1. The unit is selected for operation by the program.
- 2. The processor is running.

Once the unit has been selected, the meter continues to run until a programmed control stop occurs, a manual non-process runout is performed, or the last card has been processed.

The IBM 1443 Printer (Model 1 or Model 2) provides high-speed on-line printing capabilities for the IBM 1800. One 1443 can be connected to the system.

FUNCTIONAL DESCRIPTION

The IBM 1443 Printer (Figure 35) is buffered and operates on an IBM 1800 data channel. This combination provides on-line printing with a minimum amount of Processor-Controller time and attention.

The data to be printed must be edited and arranged in core storage in exactly the form to be printed. The data format in core storage is two characters per word as shown in Figure 36.

An Initialize Write command causes the data to be transferred from core storage to the print buffer two characters at a time. The number of characters at a time. The number of characters transferred is determined by the word count (n). (A word count of n will cause 2n characters to be transferred. The word count must not be greater than one-half the number of print positions). Once the data is transferred and the remaining positions of the print buffer have been filled automatically with blanks, the printer prints the line.

The total time demand from the P-C during the loading of the buffer via the data channel depends on the core storage cycle time (approximately 4(n+1)

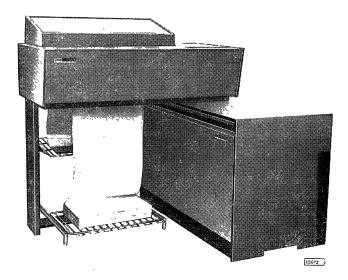


Figure 35. IBM 1443 Printer

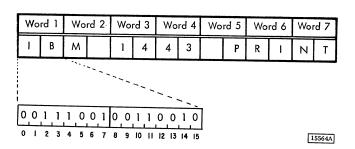


Figure 36. Core Storage Word Format

usec for 4-usec core storage, 2(n+1) usec for 2-usec core storage).

Spacing and skipping of the carriage are under direct program control. Control commands are used to indicate the spacing or skipping desired before or after printing the line. The Control command can be executed at any point in the program prior to the Initialize Write command. All skip immediate and space immediate controls are executed by the printer when the Control command has been completed. The most recent skip-after-print or space-after-print control is executed immediately after the printing of the next line, unless printing with spacing suppressed was requested by the Initialize Write command.

Printing Speeds

The 1443 takes approximately 2 ms to load its buffer. The actual line-printing speed depends upon the character set in use (Figure 37). The time to print one line varies from 100 to 500 milliseconds, depending on 1443 Model and type-bar character set.

Character	Lines per Minute								
Set	1443 - 1	1443 - 2							
13	430	600							
39	190	300							
52	150	240 .							
63	120	200							
	I	15565C							

Figure 37. Printing Speeds (1443)

Print Positions

The standard printer has 120 print positions horizontally spaced at 10 per inch. Vertical line spacing is 6 or 8 lines per inch and is selected by a belt pully adjustment located on the carriage.

The 1443 option of 24 additional print positions is available.

Character Codes and Typebar Arrangements

IBM 1800: Figure 38 shows the character coding required in the core storage for the corresponding printed character.

IBM 1443: The 52-character bar (Figure 39 is standard. Typebars with 13, 39, and 63 characters are also available.

Forms

Continuous forms with marginal punching on both sides must be used. For more detail on forms

specifications refer to "IBM 1403 and 1443 Printers: Form Design Considerations" (Form A24-3041).

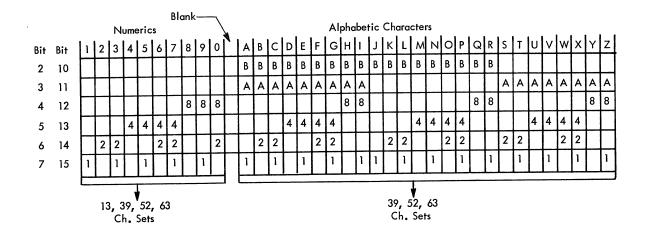
Carriage

The carriage is tape controlled and advances the form as directed by the P-C program. The carriage control characters and their meanings are shown in Figure 40.

The carriage Control command can be used to initiate an immediate or a delayed start for a line space or forms skip. An immediate skip or immediate space is executed at the time the Control command is given.

A delayed skip or delayed space is executed at the end of the next print cycle and supersedes the automatic single space after print that occurs if there is no programmed carriage control.

The skipping speed is about 15 inches per second. The carriage can be single, double, or triple spaced on an immediate or delayed basis. An immediate skip or immediate space requires



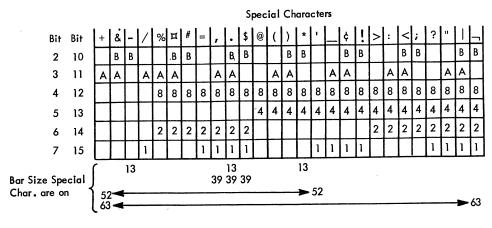


Figure 38. Character Coding (1443)

25202B

&-|1/AJ2|SBK3|TCL|4|UDM5|VEN6WFO7XGP8YHQ9|Z||R|0%||#|=|,|.\$@(|)|*|+

13 Character Set - Optional

39 Character Set - Optional

63 Character Set - Optional

25203B

Figure 39. Character Sets (1443)

45 ms for the first line and 10 ms for each additional line. A delayed space or delayed skip of one or two lines is executed as part of the 1443 print cycle. The third line adds approximately 1 ms to the print time and each additional line of a skip adds 10 ms. Sensing a punch in either tape channel 9 or 12 during spacing sets indicators in the Device Status Word. These indicators can be entered into the P-C accumulator by a Sense Device command.

The channel 9 indicator is reset by the carriage sensing a channel 12 punch in the tape. The channel 12 indicator is reset by the carriage sensing a channel 1 punch in the tape.

The carriage is equipped with an adjustable paper brake that also functions as a forms-stop contact. The distance between the platen and the type bar is adjustable to permit optimum printing impressions with forms of different thickness.

The forms tractor on the 1443 can be positioned to approximate locations and locked to the guide.

Final adjustment is accomplished with the Lateral Print Vernier, which is capable of moving the forms tractor a maximum of 1/2 inch.

Printer Keys and Lights

<u>Power ON:</u> This light indicates that power is applied to the printer control circuits.

Ready: This light indicates that the printer is ready to complete a Print or Carriage Control operation.

The light is turned off when the Stop key or Carriage Stop key is pressed, the printer runs out of forms, or the Typebar Motor switch is turned off. "Not Ready" in the DSW will come on immediately however a print or control operation in process will be completed.

Parity Check: This light is turned on when a parity error is detected in the printer check circuits. It is turned off when the IBM 1800 Reset key is pressed or when the Printer Check indicator is reset by a Sense Device command.

Immediate Skip to	Hex	Bit 0 1 2 3 4 5 6 7	Skip after Print to	Hex	Bit 0 1 2 3 4 5 6 7
Channel 1 Channel 2 Channel 3 Channel 4 Channel 5 Channel 6 Channel 7 Channel 8 Channel 9 Channel 10 Channel 11 Channel 12	01 02 03 04 05 06 07 08 09 0A 0B	00000001 00000010 00000010 00000101 00000101 00000111 00001000 00001001	Channel 1 Channel 2 Channel 3 Channel 4 Channel 5 Channel 6 Channel 7 Channel 8 Channel 9 Channel 10 Channel 11 Channel 12	31 32 33 34 35 36 37 38 39 3A 3B 3C	00110001 00110010 00110010 00110010 001101010 0011011
Immediate Space			Space after Print		
1 Space 2 Spaces 3 Spaces	21 22 23	00100001 00100010 00100011	1 Space 2 Spaces 3 Spaces	11 12 13	00010001 00010010 00010011

23484

Figure 40. Carriage Control Characters (1443)

<u>SYNC Check</u>: This light is turned on when the type bar is not properly synchronized. When this occurs the Error indicator in the DSW is turned on. Pressing the Printer Reset Key turns the light off and resets the Error indicator.

End of Form: This light is turned on when the end of the last form passes the End-of-Form switch lever. Printing will continue until a hole is sensed in control tape channel 1 setting the End-of-Forms latch; at this time the Ready light is turned off. Pressing the Start key places the Printer in a ready status, resets the End-of-Forms latch and allows printing to continue until another hole is sensed in control tape channel 1 with the same results as before.

<u>Form Check</u>: This light is turned on whenever the form guides are raised.

Carriage Interlock: This light is turned on if the typebar motor is on and the carriage tape brush is raised or the space-adjust mechanism is not seated properly.

<u>Start</u>: Pressing this key with power on, paper forms in position, and typebar motor on places the printer in a ready status.

Stop: Pressing this key turns off the Ready light. If a Print or control operation is already in progress, it is completed. If a print or control is not in progress further operations are prevented until the Start key has been pressed.

Reset: Pressing this key causes all printer check circuit indicators to be reset.

Typebar Motor: This switch is turned on for normal printer operation. In the OFF position the typebar motor and the Ready light are turned off; however, ribbon and typebar control circuits are still active. In the TYPEBAR REMOVAL position, the typebar motor is off and the ribbon and typebar controls are turned off to permit the typebar to be removed.

Carriage Restore: Pressing this key when the Ready light is off, positions the carriage at the next channel 1 punch of the control tape. If the carriage clutch is disengaged, the form does not move. When the clutch is engaged, the form moves in synchronization with the control tape.

<u>Carriage Space:</u> Pressing this key when the Ready light is off causes the form to advance one space.

<u>Carriage Stop:</u> Pressing this key stops carriage operation and turns off the Ready light.

<u>Carriage Clutch Knob</u>: The carriage clutch is used to control the carriage drive and the form feed mechanism. When the Carriage Clutch knob is set at Out, automatic form feeding cannot take place.

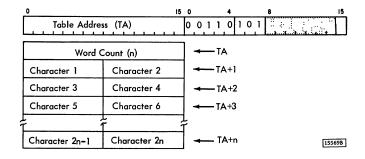
PROGRAMMING

The following I/O control commands provide for the operation and control of the 1443 printer.

I/O Control Commands

The 1443 is addressed by the five-digit area code 00110.

Initialize Write (101)



This command causes data in the table at the location specified by the address portion of the IOCC to be transmitted to the 1443 buffer provided the 1443 is ready and not busy.

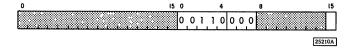
The word count (n) defines the number of words in the message. This results in 2n characters being sent to the buffer (two characters per word).

When the Initialize Write is given, the following process occurs under data channel control. The word count is transmitted to the word-count register of the data channel, and then the data transmission proceeds one core storage word at a time. Each transmission sends a word to a serial buffer. The 1443 stores both characters from the first word in its core buffer before requesting another word. As each word is read from the P-C, the word count is

decremented by one. When the word count reaches zero, the Transfer Complete interrupt occurs and the remainder of the printer buffer is loaded with blanks without accessing the P-C storage. When the last position of the printer buffer is loaded, the 1443 automatically takes a print cycle. If the Space Suppress latch was set on the Initialize Write instruction, the carriage will not automatically take a line space or any after-print control after printing a line.

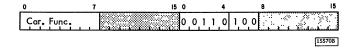
Modifier bit 15 suppresses spacing or any afterprint controls on the line to be printed.

CE Mode (000)



This command places the 1443 in CE mode if modifier bit 15 is on or removes it from CE mode if modifier bit 15 is off.

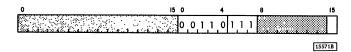
Control (100)



This command is used to initiate carriage control. The carriage control character (Figure 40) indicating the desired motion is located in bit 0 to bit 7 of the address word of the IOCC.

The Control command must be given while the Printer Not Ready and Carriage Busy indicators are off. Completion of a Carriage Control causes a printer complete interrupt.

Sense DSW (111)



This command is used to enter the Device Status Word (Figure 41) into the P-C accumulator.

Modifier bit 15 indicates whether the indicators associated with the 1443 are to be reset: 0 if no reset, 1 if reset.

Interrupt Indicators

There are two Interrupts associated with the 1443.

Transfer Complete: This interrupt occurs when the word count (n) has been reduced to zero by the channel controls. This indicates that 2n data characters have been transmitted to the printer buffer. Once this interrupt occurs, the P-C program can start setting the next line of print into the message area. This indicator is turned off by the Sense Device command with bit 15 on.

<u>Print Complete</u>: This interrupt occurs when the printer has completed a control or initialize write operation. It signals that the next operation can be transmitted to the 1443. This indicator is turned off by the Sense Device command with bit 15 on.

Non-Interrupt Indicators (DSW)

Error: This indicator is turned on whenever a parity check or sync check occurs in the printer, or a parity error occurs on the channel data bus during a data transfer cycle-steal cycle. (These errors can occur randomly during program execution since the printer is buffered as well as cycle-steal ori-

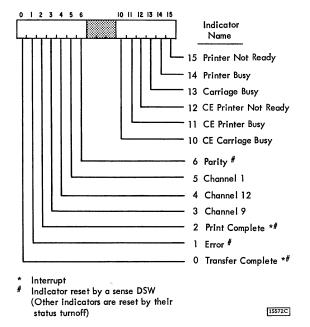


Figure 41. Device Status Word (1443)

ented). When Sense DSW with bit 15 on is executed, the error indicator is reset if a printer parity error or a parity error on the channel data bus turned it on. If a sync check turned the indicator on, the XIO instruction does not reset it. The IBM 1801/1802 Reset key resets the error indicator if a parity check in the printer or a parity check on the channel data bus was the cause. The 1443 Reset resets the indicator if a parity or sync check in the 1443 was the cause. A 1443 sync check removes the 1443 from a ready condition.

<u>Channel 9</u>: This indicator is turned on when a punched hole is detected in channel 9 of the carriage control tape. This indicator is turned off by detection of a hole in channel 12 of the carriage tape.

<u>Channel 12</u>: This indicator is turned on when a punched hole is detected in channel 12 of the carriage control tape. This indicator is turned off by detection of a hole in channel 1 of the carriage tape.

<u>Channel 1</u>: This indicator is on whenever a punched hole is detected in channel 1 of the carriage control tape.

Parity: This indicator is turned on when a parity error is detected on the channel data bus during a cycle-steal operation when data is being transferred from core storage to the 1443 buffer. This indicator is turned off by the XIO (Sense DSW) instruction with bit 15 on.

CE Carriage Busy: This indicator is on when the 1443 is in CE mode and printing is in progress or the carriage is in motion. Sensing this indicator does not cause it to be reset. This indicator should be tested prior to execution of an XIO instruction to the 1443 with the 1443 in CE mode.

CE Printer Busy: This indicator is on when the 1443 is in CE mode and printing is in progress or the carriage is in motion. Sensing this indicator does not cause it to be reset. This indicator should be tested prior to execution of an XIO instruction to the 1443 with the 1443 in CE mode.

CE Printer Not Ready: This indicator is turned on by any of the following conditions: (No print or

carriage control command should be executed for the 1443 when this indicator is on.)

- 1. When the 1443 is in CE mode and if CE Printer Busy is on as indicated above.
- 2. When the 1443 is physically unable to accept an instruction.
- 3. When the End-of-Forms indicator in the 1443 is on.

Carriage Busy: This indicator will be on when the 1443 is not in CE mode and when printing is in progress or the carriage is in motion. Sensing this indicator does not cause it to be reset. This indicator should be tested prior to execution of an XIO to the 1443.

Printer Busy: This indicator will be on when the 1443 is not in CE mode and when printing is in progress or the carriage is in motion. Sensing this indicator does not cause it to be reset. This indicator should be tested prior to execution of an XIO to the 1443.

Printer Not Ready: This indicator is turned on by any of the following conditions: (No print or carriage control command should be executed for the 1443 when this indicator is on.)

- 1. When the Printer Busy indicator is on as defined above.
- 2. When the 1443 is physically unable to accept an instruction.
- 3. When the End-of-Forms light is on.
- 4. When the 1443 is in CE mode.

1443 Usage Meter

This meter runs when the following conditions are present:

- 1. The printer is selected for operation by the program.
- 2. The processor is running.

Once the printer has been selected, the meter continues to run until the printer is manually stopped by the operator, an out of forms condition exists, or a programmed stop occurs.

The IBM 1054 Paper Tape Reader (Figure 42) and the IBM 1055 Paper Tape Punch (Figure 43) provide paper tape input/output for the IBM 1800. One of each unit can be connected to the system.

FUNCTIONAL DESCRIPTION

The 1054 and 1055 operate on the IBM 1800 under direct program control.

The 1054 Paper Tape Reader reads one-inch, eight-track paper tape at a maximum rate of 14.8 characters per second (cps).

The 1055 Paper Tape Punch punches one-inch, eight-track paper tape at a maximum punching rate of 14.8 cps.

Character Code

The 1054 Paper Tape Reader reads input data into the core storage as an image of the holes in the tape. One paper tape character is read into each addressed core storage location. Any code translation must be made by programming.

Figure 44 indicates which bits of the word correspond to the respective holes in the paper tape read by the 1054.

The 1055 Paper Tape Punch punches data as an image of the data contained in the core storage word on a character-to-character basis as shown in Figure 44.

Special data-character and control-character coding (feed code, etc.) and recognition must be handled by the stored program.

DESCRIPTION OF OPERATION

Paper Tape Reader

The reading of paper tape from the 1054 is initiated by a Control command with the 1054/1055 addressed. This command loads a character into an input buffer and then moves the paper tape one character position. When the buffer has been loaded with data, an interrupt is initiated that signals the program that information is available for reading into the core storage position specified by the address word of a subsequent Read command.

The elapsed time from the execution of the Control command until the interrupt is initiated is approximately 15 ms. To maintain the 14.8 cps operating speed of the 1054, the Read command must be given within 60 ms after the interrupt so that

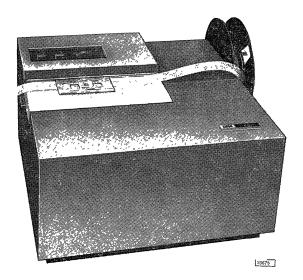


Figure 42. IBM 1054 Paper Tape Reader

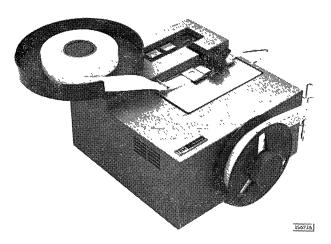


Figure 43. IBM 1055 Paper Tape Punch

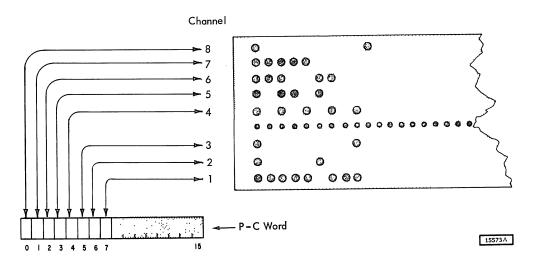


Figure 44. Word Format (1054/1055)

another Control command can be executed to energize the reader clutch preparatory to reading the next character.

Paper Tape Punch

The punching of data by the IBM 1055 Paper Tape Punch is initiated through execution of a Write command with the 1054/1055 addressed. The execution of the Write command starts the punch, and the data in the core storage position specified by the address word is punched into the tape. Each core storage word contains one paper tape character to be punched in the tape.

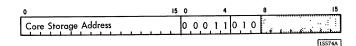
PROGRAMMING

The IBM 1054 Paper Tape Reader and the IBM 1055 Paper Tape Punch operate on the IBM 1800, under direct program control.

I/O Control Commands (IOCC)

The 1054 and 1055 are addressed by the same five-digit area code and may operate simultaneously.

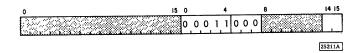
Read (010)



This command reads one character from paper tape into P-C core storage into bits 0-7 and clears bits 8-15 to zero.

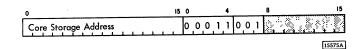
The address word specifies the location in P-C core storage where the tape character is to be stored.

CE Mode (000)



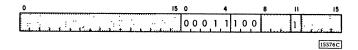
This command sets CE mode according to modifier bit 15. With modifier bit 15 on, the 1054/1055 is placed in CE mode; with bit 15 off, 1054/1055 is removed from CE mode.

Write (001)



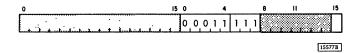
This command writes one character from bits 0-7 in P-C core storage to the paper tape punch. The address word specifies the location in P-C core storage where the tape character is stored.

Control (100)



This command is valid only if the bit 11 modifier bit (Start Paper Tape Reader) is on. This command must be given prior to each character to be read from the 1054. Execution of this command causes one character to enter the paper tape reader buffer, the tape to be advanced one column, and a Reader Service Response interrupt to be initiated to indicate that a character from paper tape can be read into the core storage location specified by a subsequent Read command.

Sense DSW (111)



This command is used to enter the Device Status Word (Figure 45) into the P-C accumulator. Modifier bit 15 indicates if the indicators associated with the 1054/1055 are to be reset.

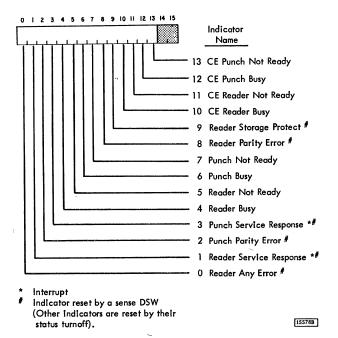


Figure 45. Device Status Word (1054/1055)

Note: The DSW word is shared by the 1054/1055, therefore, under simultaneous operation of both devices, care must be used in Reset Sense Device to avoid loss of indicators for one of the devices.

Interrupt Indicators

There are two interrupts associated with the 1054/1055. These two interrupts are internally wired to the same interrupt level.

Reader Service Response: This interrupt occurs when the reader has completed the execution of a Control command. This interrupt indicates to the P-C that a character is available to be entered into core storage.

Punch Service Response: This interrupt occurs when the punch has completed punching as directed by the execution of a Write command, and indicates that the punch can accept the next command.

Non-Interrupt Indicators (DSW)

These indicators are associated with the 1054/1055:

Reader Any Error: This indicator is turned on when the P-C detects a parity error or a reader storage protect error occuring on an IPL or read operation.

Punch Parity Error: This indicator is on if a P-C Parity Check error is detected in any character being sent to the Paper Tape Punch as the result of a write command.

Reader Busy: This indicator is on from the time a Control command (Start Paper Tape Reader) is given until data is available (approximately 15 ms). Availability of data is signalled through issuance of a Reader Service Response interrupt.

Reader Not Ready: This indicator is on when the Tape Extension switch is open. This condition exists when the paper tape is broken or not feeding freely. Manual intervention is required to clear these conditions. This indicator is also on if the reader is "busy" (See Reader Busy indicator) or if the reader is in CE mode.

This indicator should be tested by the program before a Read or Control command is given. If a Read command is given while this indicator is on, erroneous data can be read into core storage. No indication can be given as to whether the data read is correct or incorrect. This indicator is always on if there is no 1054 Paper Tape Reader attached.

Punch Busy: This indicator is on for the total time the punch is mechanically engaged and punching a character (68 ms). During this time the punch is not able to accept another Write command.

Punch Not Ready: This indicator is on when tape is not feeding freely from the tape spool, when the tape pressure roll holder is not down and holding the tape against the feed wheel, or when tape is not present. Manual intervention is required to clear these conditions. The indicator is also on if the punch is "busy" (see Punch Busy indicator) or if the punch is in CE mode.

This indicator should always be tested by the program before a Write command is given. If a Write command is given while this indicator is on, loss of information will probably occur. No indication is given of this loss. This indicator is always on if there is no 1055 Paper Tape Punch attached.

Reader Parity Error: This indicator is on if a P-C parity check error is detected in any character being read as the result of a read command from the Paper Tape Reader.

Reader Storage Protect: This indicator is turned on if an attempt is made to store data in a storage-protected core location.

<u>CE Reader Busy</u>: In CE mode this indicator is used in place of the Reader Busy indicator.

CE Reader Not Ready: In CE mode this indicator is used in place of the Reader Not Ready indicator.

CE Punch Busy: In the CE mode this indicator is used in place of the Punch Busy indicator.

CE Punch Not Ready: In CE mode this indicator is used in place of the punch Not Ready Indicator.

Paper Tape Initial Program Load

If there is no 1442 on the System, the 1054 will be wired for initial program load (IPL). During IPL, the 1054 Paper Tape Reader is forced into a run condition as a result of the IPL line on the channel interface. The 1054 operates at its maximum operating speed of 14.8 characters per second. Data words are read into core storage, starting at location 0000.

Paper-tape channels 1 through 4, inclusive, of each tape character are used as data bits for assembly into a 16-bit word during the IPL mode. These four channel bits are assembled into a 16-bit word for transmission to core storage. Four paper-tape characters are required to load one 16-bit word.

Upon assembly of the word within the reader, the channel is signalled and the word is transferred to core storage. The Instruction counter is incremented plus one, and the P-C awaits the channel signal that another word has been assembled for transfer to the P-C.

The operation continues in this manner until a channel 5 punch in other than a delete (0111 1111) character is detected in the paper tape. Upon detection of the channel 5 punch, the channel receives a signal that the IPL mode has been terminated. The IPL line is then deconditioned, stopping the tape reader; the P-C Instruction counter is reset to zero and the P-C commences execution of the loaded program. The paper tape character with a channel 5 punch is not read into core storage.

<u>Note</u>: The paper tape reader is busy and not ready for several milliseconds after IPL mode is terminated.

During program load, delete characters are recognized by the reader. These characters are not loaded into the assembly buffer in IPL mode. Delete characters will not be recognized nor handled in any special manner by the reader except in the IPL mode. This allows the customer to punch a leader of delete characters to facilitate loading the tape.

Data characters from tape are loaded to the channel read bus as follows (in the IPL mode):

First tape character:

Tape Channel 4 - B0

Tape Channel 3 - B1

Tape Channel 2 - B2

Tape Channel 1 - B3

Second tape character:

Tape Channel 4 - B4

Tape Channel 3 - B5

Tape Channel 2 - B6

Tape Channel 1 - B7

Third tape character:

Tape Channel 4 - B8

Tape Channel 3 - B9

Tape Channel 2 - B10

Tape Channel 1 - B11

Fourth tape character:

Tape channel 4 - B12

Tape channel 3 - B13

Tape channel 2 - B14

Tape channel 1 - B15

Definition

Delete character: Tape channels 7654321

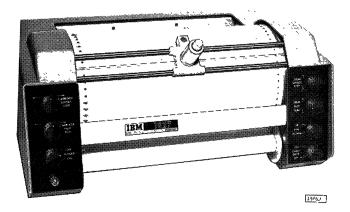


Figure 46. IBM 1627 Plotter (Model 1)

The IBM 1627 Plotter provides an exceptionally versatile, reliable, and easy-to-operate plotting system for the IBM 1800. The plotter converts tabulated digital information into graphic form. Bar charts, flow charts, organization charts, engineering drawings, and maps are among the many graphic forms of of data which can be plotted on the 1627 Plotter.

Two models of the 1627 are available and the major characteristics are as follows:

Model 1 - Plotting area: 11 inches by 120 feet; incremental-step size: 1/100 inch; speed: up to 18,000 steps/minute.

Model 2 - Plotting area: 29-1/2 inches by 120 feet; incremental-step size: 1/100 inch; speed: up to 12,000 steps/minute.

Speed	X, Y Increments Pen Status Change	Model 1 18,000 Steps/Min 600 Operations/Min	Model 2 12,000 Steps/Min 600 Operations/Min
Increment Size		1/100 Inch	1/100 Inch
Chart Paper	Width Plotting Width Length Sprocket Hole Dimensions	12 Inches 11 Inches 120 Feet .130 Inch Dia on 3/8 Inch Centers	31 Inches 29 1/2 Inches 120 Feet .188 Inch Dia on 1 Inch Centers
			15667

Figure 47. Operating Characteristics (1627)

More information on both models is given in Figure 47.

The IBM 1800, with the 1627, can be used for trend recording and for presenting real-time graphic representation of computed variables relative to the process under control.

OPERATION

Data from the IBM 1801 or 1802 Processor-Controller core storage is transferred serially (under direct program control) to the 1627, where it is translated into 1627 actuating signals. These signals are then converted into drawing movements by the 1627 Plotter.

The actual recording is produced by incremental movement of the pen on the paper surface (y-axis) and/or the paper under the pen (x-axis). The pen is mounted in a carriage that travels horizontally across the paper. The vertical plotting motion is achieved by rotation of the pin-feed drum, which also acts as a platen (Figure 48).

The drum and the pen carriage are bidirectional; that is, the paper moves up or down, and the pen moves right or left. Control is also provided to raise or lower the pen from or to the paper surface. The pen remains in the "raised" or "lowered" position until directed to change to the opposite status.

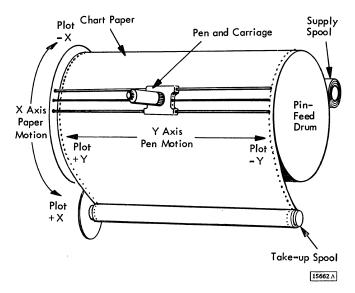


Figure 48. Paper and Pen Motions (1627)

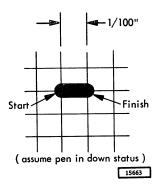


Figure 49. Plotter Result for One Horizontal (Y-Axis) Movement (1627)

The drum and pen-carriage movements and the pen status are controlled by digits transferred to the 1627. Each output word is decoded into a directional signal which causes a 1/100-inch incremental movement of the pen carriage (Figure 49) and/or paper, or a raise-pen or a lower-pen movement. The motion or action resulting from each word in the output record is shown in Figure 50. As shown in Figure 50, a valid combination of bits 1 through 4 (1/4, 1/3, 2/4, 2/3) causes a diagonal line.

Opposing command bit combinations (1/2) and 3/4 are invalid, and should not be used.

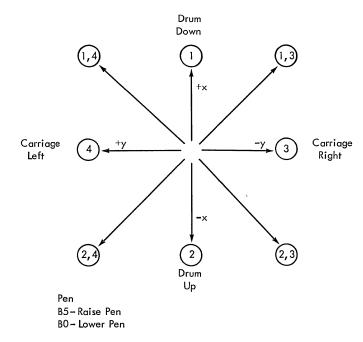
The time required for execution of raise-pen and lower-pen commands is 100 ms. The time to plot a point is approximately 5 ms (3.3 ms for 300 steps/sec). In order to keep the plotter operating at full speed, the next control character must be sent to the plotter 0.5 ms after the Service Complete interrupt.

1627 OPERATING CONTROLS

Seven operating controls and one Power On light are mounted on the front panels of the 1627 (Figures 51 and 52). A description of the function of each control follows.

Power: This switch connects power from the 1800 to the 1627. There is no power-on delay involved with the 1627 Power switch; that is, the plotter can operate as soon as the switch is turned on. A Power On Light, associated with this switch, indicates when power is on.

Carriage Fast Run: This switch allows the pen carriage to be stepped rapidly to the left or right at the



Note: The encircled numerical figures are the P-C word bit positions that correspond to the indicated direction of plotting movement as viewed from the front of the plotter. Normally, graphs are plotted so that their horizontal axes are, in reality the X axis as shown above.

25205

Figure 50. Output Record Control (1627)

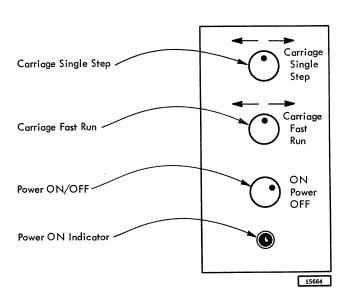


Figure 51. Left Console Controls (1627)

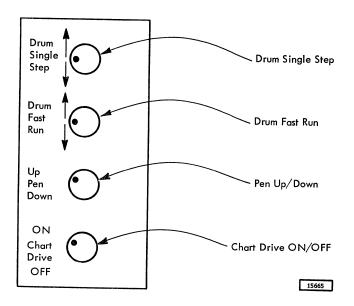


Figure 52. Right Console Controls (1627)

rate of 120 steps a second. The Carriage Fast Run switch is used to move the carriage to any desired area of the graph.

Carriage Single Step: This switch allows the pen carriage to be moved in singlestep increments (1/100 inch) either left or right. The Carriage Single Step switch permits the operator to accurately align the carriage along the y-axis of the chart.

<u>Drum Fast Run:</u> This switch allows the drum to move the paper rapidly up or down at the rate of 120 steps a second. The Drum Fast Run switch is used in conjunction with the Carriage Fast Run switch to position the pen to any desired area of the graph.

Drum Single Step: This switch allows the drum to be rotated in single-step increments (1/100 inch) in either direction. The Drum Single Step switch is used in conjunction with the Carriage Single Step switch to permit the operator to accurately align the pen on a point or fixed coordinate on the graph.

<u>Pen:</u> This switch provides a means for manually raising the pen from the surface of the drum or lowering the pen to the drum.

<u>Chart Drive</u>: This switch allows the front and rear chart drives to be disabled. When recording on single sheets of graph paper, the Chart Drive switch should be in the Off position. When recording on roll paper, this switch should be in the On position.

Vernier Control: Large-size chart paper may vary in width due to high or low humidity; therefore a vernier control is provided on the 1627, Model 2, to vary the size of the pen carriage increments. In this way, the pen movement is adjusted to match the printed scale of the chart paper. The vernier control knob is located at the left end of the drum above the switch panel. For work with non-scale paper, the control should be centered at the zero position.

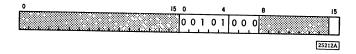
PROGRAMMING

The IBM 1627 Plotter operates under direct program control of the IBM 1800.

I/O Control Commands (IOCC)

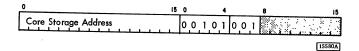
The 1627 is addressed by the five-digit area code of the IOCC.

CE Mode (000)



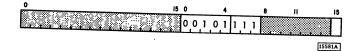
This command places the 1627 in CE mode if modifier bit 15 is on and removes the 1627 from CE mode if modifier bit 15 is off.

Write (001)



This command causes the word in the core storage location specified by the address to be sent to the 1627 to control the movement of the pen or drum.

Sense DSW (111)



This command causes the 1627 Device Status Word (Figure 53) to be placed in the P-C accumulator. Modifier bit 15 specifies if the interrupt is to be cleared: 1-bit if it is to be reset, 0-bit if it is not.

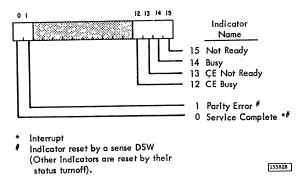


Figure 53. Device Status Word

Interrupt Indicator

There is only one interrupt associated with the 1627: Service Complete. This interrupt occurs when the 1627 has completed the action specified by the last character transmitted by the Write command.

Note: If conflicting P-C word bits are placed in the command, no definite statement can be made about what action (if any) will occur. Examples of conflicting commands: Raise Pen (B5) and Lower Pen (B0); Carriage Left (B4) and Carriage Right (B3); Drum Up (B1) and Drum Down (B2).

Non-Interrupt Indicators (DSW)

Parity Error: This indicator is turned on when a parity error is detected in a control character transferred to the 1627 from the P-C.

CE Busy: In the CE mode this indicator is used in place of the Busy indicator. All conditions defined in the Busy status are applicable to this indicator in the CE mode only. Programs utilizing the CE mode use this indicator instead of the Busy indicator.

CE Not Ready: In CE mode this indicator is used in $\overline{\text{place of the Not}}$ Ready indicator. All conditions defined in the Not Ready status are applicable to this indicator in the CE mode only.

Busy: The 1627 is in a Busy status and cannot accept a character when this indicator is on. The program should always determine that the Busy indicator is off before a Write command is given. If a Write command is given while Busy is on, loss of information will probably occur. No indication is given of this loss.

Not Ready: The 1627 has power on when this indicator is off.

The IBM 1802 Processor-Controller provides a means of connecting IBM 2401 and 2402 Magnetic Tape Units to the 1800 System (Figure 54).

The following IBM magnetic tape units are available for the 1800 System.

- The 2401 Model 1, a single 9-track 30-kc tape drive.
- The 2401 Model 2, a single 9-track 60-kc tape drive.
- The 2401 Model 3, a single 9-track 90-kc tape drive.
- The 2402 Model 1, a double 9-track 30-ke tape drive.
- The 2402 Model 2, a double 9-track 60-kc tape drive.
- The 2402 Model 3, a double 9-track 90-kc tape drive.

One or two tape drives (7- and 9-track intermixed) can be attached to the 1802 in any of these configurations:

- One 2401.
- Two 2401's (models and heads can be intermixed).
- One 2402 (7- and 9-track heads can be intermixed).

The magnetic tape unit operation requires a data channel.

Note: A 7-track read-write head feature is available for 2401 and 2402 Magnetic Tape Units.

FUNCTIONAL DESCRIPTION

The 2401 and 2402 Magnetic Tape Units are described in more detail in the IBM 2401 and 2402 Magnetic Tape Units Principles of Operation, Form A22-6866.

Registers

The following 1802 registers are associated with control of the magnetic tape units:

Data Input/Output Register: This register assembles magnetic tape characters into 16-bit words for the Processor-Controller, and distributes words from the P-C into character formats for magnetic tape.

Read/Write Buffer Register: This buffer register permits the overlapping of cycle-steal requests with tape drive data transfers and permits more time for cycle steals to be honored.

Data Formats

A tape record is defined as information on tape between two inter-record gaps. This information is made up of characters (known as bytes) with possible

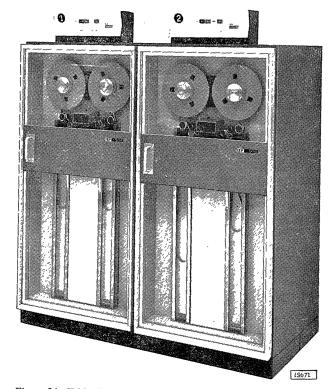


Figure 54. IBM 2401 Magnetic Tape Unit, 2402 Magnetic Tape Unit

bits in each track of each character. One track is always reserved for parity.

The minimum length of a record to be written should be 8 P-C words or 16 bytes long. Each word transmitted to or from the P-C data channel contains 16 data bits when using a 9-track tape drive. For 7-track operation each word transmitted may contain 12 or 16 data bits, as specified by the I/O Control command.

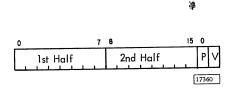
When reading or writing in 9-track mode, each P-C word contains two 8-bit tape bytes. The first byte is in bit positions 0 through 7; the second byte is in bit positions 8 through 15.

When reading or writing two bytes per word in 7-track mode, the first byte is in bit positions 2 through 7; the second byte is in bit positions 10 through 15; bit positions 0, 1, 8, and 9 are not used.

When reading or writing in 7-track packed format mode, each P-C word contains two 6-bit tape bytes and one 4-bit tape byte. The first byte is in bit positions 0 through 5; the second byte is in bit positions 6 through 11; and the third byte is in bit positions 12 through 15 (Figure 55).

Seven-track packed format is designed for use on 1800 systems only. Data written on other systems, such as the IBM 7090, cannot be read into the 1800 in 7-track packed format unless care is taken to generate correct P and V check bits. Reading data containing incorrect P and V check bits generates internal level interrupts which must be serviced and stores an incorrect character.

Each P-C word transmitted to or from the $\underline{P-C}$ $\underline{I/O\ Channel}$ consists of 16 data bits plus two parity bits, P and V, which maintain an odd-bit count for each half of the word. P is the parity bit for data bits 0-7, and V is the parity bit for data bits 8-15.



In 7-track packed format, these bits are recorded on magnetic tape as three characters and are in the same manner directly read off tape and placed on the P-C I/O Channel (including the P & V bits, which are not corrected).

Additional bits (check bits) are generated by the tape control for each byte as required to maintain the parity condition specified by the IOCC Modifier. On reading, these check bits are first checked to indicate any errors, and after that they are reset.

Error Check Registers

Skew Registers (High and Low Clips): These registers receive and de-skew bit pulses from tape track amplifiers. The high-clip register assists in the 9-track error correction scheme. The low-clip register has a Vertical Redundancy Check (VRC) error.

LRCR (Longitudinal Redundancy Check Register): This register checks the LRC error of every tape record including the LRC character itself. All bit triggers have to be off to have no LRC error.

CRCR (Cyclic Redundancy Check Register): This register computes the CRC character to be written preceding every LRC character and is used to determine the track in error (9 track only).

EPR (Error Pattern Register): This register creates a high-clip VRC error pattern, which in comparison with the CRCR specifies the track in error for error correction (9 track only).

Timings

The following timings are valid for a 2- μ sec, 2.25- μ sec, or 4- μ sec P-C core storage and include storage times in the tape buffer registers.

7–Track Tape Bit Positions	First Character	Second Character	Third Character
С	С	С	С
-	-	-	-
-	-	-	-
В	0	6	12
Α	1	7	13
8	2	8	14
4	3	9	15
2	4	10	Р
1	5	11	٧

25206A

Figure 55. Data Format (7 Track Packed)

Cycle steals for magnetic tape must be honored within an average of 16 μ sec to permit operation of 2400 series tape drives at a 90-kHz rate.

The tape control unit should be assigned a high data channel priority (cycle steal) to insure that no data is lost.

When a tape drive is selected by a Sense Device command, a second Sense command must be issued after a minimum interval of 5 μ sec to receive a valid indication of any of the following conditions (See Non-Interrupt Indicators section): (1) tape at load point, (2) tape channel busy or rewinding, (3) tape channel busy or not ready, (4) End-of-Tape indicator or tape mark.

Scan Control

Magnetic tape operations can use the IBM 1800 Scan Control facility. This facility allows data tables to be "chained" and operated on as if they were only one table.

Parity

The 1800 can read or write 7-track magnetic tape in either even-parity or odd-parity mode. Bit 15 of the Initialize Read or Initialize Write modifier specifies the mode: 1 = even parity; 0 = odd parity. Nine-track operations are performed in odd parity only, and bit position 15 is ignored.

When reading or writing 7-track magnetic tape in even parity, the following should be considered with respect to all-0 tape characters.

- 1. A 0 character from main storage is written on tape as an A-bit and a C-bit.
- 2. A character that contains only an A-bit and a C-bit which is read from tape is placed in main storage as a 0 character.
- 3. Data characters containing only a tape A-bit (@) are written on tape as an A-bit and a C-bit. Therefore, if these characters are read back, they are placed in main storage as 0 characters.
- 4. No Tape Data Error indication occurs if the A-bit and C-bit are transferred properly.

Tape Mark

A 9-track tape mark sets bits 3, 6, and 7 and has odd parity.

A 7-track tape mark sets bits 4, 5, 6, and 7 if read in 2-byte mode, or bits 2, 3, 4, and 5 if used in packed format mode. Seven-track tape marks always have even parity.

Error Correction (9-Track)

An Initialize Read command can recover automatically any number of errors (pick-ups or dropouts) on any one track, if modifier field bit 14 is programmed. However, for this automatic error correction to work, a read re-try procedure is required that intermixes a number of read re-trys on the same record with moving tape to another record (which is usually backward past the tape cleaner) and back to the desired record to continue more read re-trys. The standard recovery procedure is to first read a record; then, if errors exist, backspace and readcorrect (read with modifier bit 14) each record up to ten times. Finally, if errors still exist, perform five backspaces (equal to 3" with minimum records) to ensure that the tape record desired has moved past the tape cleaner and to insure that the errorcorrection circuitry has been reset (requires two backspaces).

Note: For the first record on tape (where backspacing two records is not possible), this tape record movement has to be replaced by temporarily selecting the opposite tape drive through a Sense Device command for the error correction to function. This may be done even when there is only one drive attached.

Then move tape forward by reading records with word count of zero to reach the beginning of the desired record and continue the standard recovery procedure with read-correct until tape record movement past the cleaner is required again. Repeat this procedure up to 9 times for a total of 100 read-correct operations before concluding that a record is not correctible.

In some cases, the 10 read-corrects on the same record can be reduced, but not reduced to less than 3. The 10 record movements past the tape cleaner can also be reduced, but not reduced to less than 2.

PROGRAMMING

Magnetic tape operates on an IBM 1800 Data Channel. Four I/O Control Commands are used for tape operations.

<u>Initialize Read:</u> Reads data from magnetic tape into core storage.

<u>Initialize Write:</u> Writes data from core storage onto magnetic tape.

Control: Initiates tape control functions such as backspace, rewind, etc.

Sense Device: Selects the specific tape unit to "ready" it for operation, or reads the Device Status Word into the accumulator, or reads the channel word count into the accumulator, or performs the operation stop to clear the data channel for other use.

Note: The DSW should be sensed and checked for any error conditions after a read or write since the tape errors do not cause an interrupt.

Command Rejections

See Interrupt Indicators.

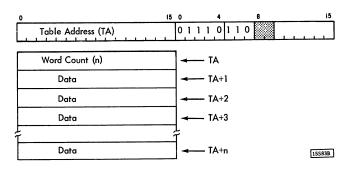
Tape Unit Selection

Before a tape unit may be used, it must be placed in a selected mode. Tape unit zero is automatically placed in this mode when the P-C Reset key is pressed. To change the selection from unit 0 to unit 1, the execution of a Sense Device command is required while the tape control unit is not busy. When a unit is selected, it remains selected until another Sense Device command selects the other unit. While a unit is selected, it may be read from or be written to, or Control commands may be executed, without any additional selection.

I/O Control Commands (IOCC)

The five-digit area code (01110) designates Tape Control Unit (TCU).

Initialize Read (110)



If accepted, this command resets the Device Status Word indicators marked with an X in Figure 56 and reads a specific number of words (n) from magnetic tape to the P-C via a data channel. (For resetting of Tape Mark indicator, see the description of that indicator.)

Modifier bits that have significance are:

B10 (bit 10) = 0 - Specifies tape unit 0.

B10 (bit 10) = 1 - Specifies tape unit 1.

B11 and B12 - Specify the density (7-track tape only; ignored for 9-track, which is always 800 bits/inch).

<u>11</u> <u>12</u>

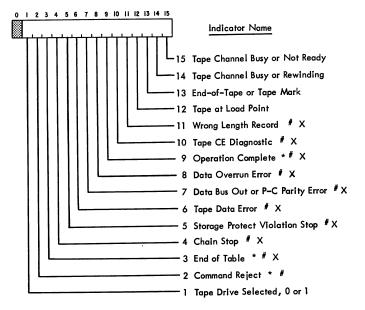
0 = 800 bits/inch

0 1 = 200 bits/inch

 $1 \quad 0 = 556 \text{ bits/inch}$

- B13 Specifies packed format for 7-track tape (ignored on 9-track).
- B14 Requests a Read-While Correcting operation on 9-track mode (ignored on 7-track or initial 9-track mode). Should always be used, unless error correction is to be eliminated.
- B15 Specifies the parity mode: 1 = even parity; 0 = odd parity (ignored on 9-track).

The address word specifies the location in core storage of the table area where the data is to be stored.

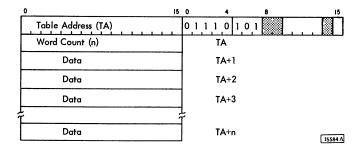


- * Interrupt
- Indicator reset by a sense DSW (other indicators are reset by their status turn off.)
- X Reset by a read or write command

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Figure 56. Device Status Word (2401/2402)

Initialize Write (101)



If accepted, this command resets the Device Status Word indicators marked with an X in Figure 56 and writes a specific number of words (n) from the P-C to magnetic tape via the data channel. (For resetting of Tape Mark indicator, see the description of that indicator.)

Modifier bits that have significance are:

B10 = 0 - Specifies tape unit 0.

B10 = 1 - Specifies tape unit 1.

B11 and B12 - Specify the density (7-track tape only; ignored for 9-track which is always 800 bits/inch).

<u>11</u> <u>12</u>

0 = 800 bits/inch

0 1 = 200 bits/inch

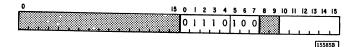
1 0 = 556 bits/inch

Bit 13 - Specifies packed format for 7-track tape (ignored on 9-track).

B15 - Specifies the parity mode; 1 = even parity; 0 = odd parity (ignored on 9-track).

The address word specifies the location in core storage of the table area that contains data to be put onto magnetic tape.

Control (100)



If accepted, this command causes the tape drive to perform the control function specified by B13, B14, and B15 of the modifier field, and resets the Device Status Word indicators marked with an X in Figure 56. (For resetting of Tape Mark indicator, see the description of that indicator.)

Modifier bits that have significance are:

B10 - Specifies tape unit 0 or 1.

B11 and B12 - Specifies density (7-track only): if function is backspace, 200 bits/inch should be programmed.

11 12

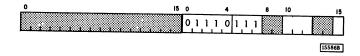
0 = 800 bits/inch

0 1 = 200 bits/inch

 $1 \quad 0 = 556 \text{ bits/inch}$

B13 through B15 - Specify control function (Figure 57)

Sense Device (111)



This command may be used to:

- 1. Sense the Device Status Word.
- 2. Place a tape unit in the selected mode.
- 3. Reset the Device Status Word indicators.
- 4. Sense the channel word count.
- 5. Perform the operation stop to clear the data channel.

Bit position 10 of the modifier field specifies the tape unit (0 or 1) to be selected. If an attempt is

Bit	Posit	ions	C			
13	14	15	Control Function			
0	0	0	Rewind and Unload			
0	0	1	Write Tape Mark			
0	1	0	Erase			
0	1	1	Backspace			
1	0	0	Rewind			

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Figure 57. Tape Control Functions

made to change the selection from one tape unit to the other while the first unit is busy, the busy unit remains selected. Interrogation of bit position 1 of the Device Status Word which has been read into the accumulator will show that the selection is unchanged.

If bit position 11 of the modifier field is 0, the Sense DSW reads the Device Status Word and selects a tape unit. The Device Status Word of the tape unit selected is read into the accumulator.

When bit position 11 of the modifier field is 0, the Sense Device command may also be used to reset the Device Status Word indicators shown in Figure 56. If bit position 15 of the modifier field is 0, no indicators are reset. If bit position 15 of the modifier field contains a 1, those indicators marked with a # in Figure 56 are reset after being loaded into the accumulator. (See the description of Tape Mark and Command Reject.)

If bit position 11 of the modifier field contains a 1, the Sense Device command reads the channel word count. In this case, bit positions 10 and 15 of the modifier field are ignored. The channel word count gives the word count difference if the number of data words on magnetic tape did not equal the word count in the P-C. When the tape record is longer than the programmed word count, the channel word count is in true form. When the tape record is shorter than the programmed word count, the channel word count is in 1's complement form. Bit positions 0 and 1 of the channel word count indicate:

Bit Positions

0 1

0 0 = true binary number

1 1 = 1's complement number

Bit positions 2 through 15 contain the word count. If bit position 12 of the modifier field contains a 1, an operation stop is performed by setting the word count to zero in addition to the other Sense Device or Sense Channel Word Count command present. Modifier bits that have significance are:

B10 - Specifies tape unit.

B11 - Specifies channel word count.

B12 - Specifies program stop operation.

B15 - Specifies indicator reset.

The indicators identified by the Device Status Word bits 12, 13, 14, and 15 require 5 μ s from the selection of the tape unit before their status can be

accurately placed in the Device Status Word. Therefore, if the status of these indicators is desired, the Sense Device command to select the tape unit must precede the Sense DSW command to read the DSW indicators by at least 5 μ s.

Interrupt Indicators

Three interrupts are associated with tape control operation. These indicators generate interrupts on the same interrupt level.

Command Reject: This indicator comes on if an Initialize Read, Initialize Write, or Control command is rejected for one of the following reasons:

- 1. Addressed unit busy or not ready.
- 2. Attempt to write on file protected unit (includes Tape Mark or Erase).
- 3. Backspace or rewind when already at load point.
- 4. Parity Error (P-C or busy out) while initiating commands.
- 5. Command given for unselected unit.

This indicator can be reset by a Sense DSW command. If a command is rejected, that rejected command will not set the Operation Complete indicator, although any previous operation still in progress will set the Operation Complete indicator in the normal manner.

End of Table: This interrupt occurs if requested by the scan control bits, when the specified word count on a magnetic tape I/O operation becomes equal to zero. The indicator associated with this interrupt is reset by an accepted Initialize Read, Initialize Write, or Control command. It can also be reset by a Sense DSW command.

Note: When chaining, with an interrupt after each table, and using short tables and a long interrupt subroutine, a subsequent interrupt may be lost if it occurs before the DSW bit is reset.

Operation Complete: This interrupt occurs at the completion of a Write Tape Mark, Initialize Read, Initialize Write, Erase, or Backspace operation. This interrupt also occurs immediately after the initiation of a Rewind or Rewind Unload operation. The indicator associated with this interrupt is reset by an accepted Initialize Read, Initialize Write, or Control command. It can also be reset by a Sense DSW command.

Non-Interrupt Indicators (DSW)

Twelve non-interrupt indicators are associated with tape control operations. The indicator bit positions in the Device Status Word are shown in Figure 56.

Tape Drive Selected Indicator: This indicator specifies which of two possible tape drives is currently selected by the tape control, 0 or 1.

Chain Stop: This indicator comes on if a control parity error occurs while chaining and not while initializing. Initialize Write operation is terminated at this point and an operation complete interrupt occurs. Any transfer of data for an initialize read operation will be terminated although the operation complete interrupt does not occur until an inter-record gap is encountered. This indicator is reset by an accepted Initialize Read, Initialize Write, or Control command. It can also be reset by a Sense DSW command.

Storage Protect Violation (SPV) Stop: This indicator is set if an attempt is made to store data (tape read operation) into a storage-protected location. The transfer of data is terminated although the tape proceeds to the inter-record gap. This indicator is reset by an accepted Initialize Read, Initialize Write, or Control command. It can also be reset by a Sense DSW command.

Tape Data Error: This indicator comes on if any of the following read or write checks is detected:

- 1. R-W register VRC error.
- 2. Write high-clip VRC error.
- 3. Write no-echo error or read lost character.
- 4. Write skew error.
- 5. R-W LRCR error.
- 6. Read CRCR error.

When reading 7-track tape in packed format, a tape error can cause bad parity in core storage. If this occurs and the check stop switch is on Stop, the P-C will come to a check stop. This indicator is reset by an accepted Initialize Read, Initialize Write, or Control command. It can also be reset by a Sense DSW command.

Data Bus Out or P-C Parity Error: This indicator is set during cycle-steal data-transfer memory cycles if a P-C parity error is detected on bus out or bus in or if a bus out parity error is detected in the tape control unit. This indicator is reset by an accepted Initialize Read, Initialize Write, or Control command. It can also be reset by a Sense DSW command.

<u>Data Overrun Error:</u> This indicator is set if a cyclesteal acknowledge did not arrive in time for a valid data transfer. This indicator is reset by an accepted Initialize Read, Initialize Write, or Control command. It can also be reset by a Sense DSW command.

Tape CE Diagnostic: This indicator, for IBM Field Engineering use as a modifier of Tape Data Error Indicators, comes on if any one of the following tape-control checks is detected:

- 1. Read high-clip VRC check.
- 2. Read-clock VRC check.
- 3. Write-clock VRC check.
- 4. Delay-counter VRC check.

This indicator is reset by an accepted Initialize Read, Initialize Write, or Control command. It can also be reset by a Sense DSW command.

Wrong Length Record: This indicator is on if the number of words of data on magnetic tape in an Initialize Read operation is not identical to the word count in the P-C or if a tape mark is encountered during an Initialize Read operation. This indicator also comes on if a record does not contain byte multiples exactly matching the whole total of P-C words. In this case, one or more extra bytes are added to fill up the last P-C word, and this complete word is transferred to core storage with the word counter counting this last word. This indicator is reset by an accepted Initialize Read, Initialize Write, or Control command. It can also be reset by a Sense DSW command.

Tape at Load Point: This indicator is turned on if the tape is physically at load point. Since the first record written on a tape has an extra-long record gap preceding it, this indicator will not be on after a backspace has positioned the tape at the beginning of the first record. This indicator is reset only by tape motion as the tape physically leaves the load point. This indicator is not turned off by an XIO operation. Care must be taken to ensure that the tape drive sensed is the tape drive desired by the programmer.

End-of-Tape Indicator or Tape Mark: This indicator is on if an End-of-Tape indicator is sensed during Initialize Read, Initialize Write, Write Tape Mark, or Erase, or if a tape mark has been read during an Initialize Read operation. This indicator is not set by tape marks encountered during an Initialize Write, Write Tape Mark, Erase, or Backspace Operation.

If a tape mark only was sensed, this indicator is reset by an accepted Initialize Read, Initialize Write,

or Control command. It can also be reset by a Sense DSW command. To reset the indicator if an End-of-Tape indicator is sensed, it is necessary to perform either a backspace (even if the backspace does not encounter the End-of-Tape indicator), Rewind or Rewind Unload tape operation.

Reading a tape mark always causes the Wrong Length Record indicator to be set. Sensing an Endof-Tape indicator does not stop the transfer of data and does not therefore cause the Wrong Length Record indicator to be set unless a short or long record condition also exists.

Tape Channel Busy or Rewinding: This indicator is on during Initialize Read, Initialize Write, Write Tape Mark, Erase, and backspace operations. The indicator is also on during Rewind and Rewind Unload operations after initialization of these operations. This indicator is not reset by an XIO operation. Care must be taken to ensure that the tape drive sensed is the tape drive desired by the programmer.

Tape Channel Busy or Not Ready: During Initialize Read, Initialize Write, Write Tape Mark, Erase,

and backspace operations, the tape drive is considered to be ready and busy. During Rewind and Rewind Unload operations, the tape drive is considered to be not ready and not busy. Accordingly, the tape channel busy or not ready indicator is on during all of the above listed operations. This indicator is also on if the tape drive is not physically ready. This indicator is not reset by an XIO operation. Care must be taken to ensure that the tape drive sensed is the tape drive desired by the programmer.

Programming Note: On systems with a Selector Channel and a 2401/2402 Model 3, 2401/2402 operations can not overlap Selector Channel operations.

2401 and 2402 Usage Meters

These meters run when the following conditions are present:

- 1. The unit is selected for operation by the program
- 2. The CPU is running.

The IBM 1810 Disk Storage (Figure 58) provides random-access storage capabilities for the IBM 1800. Only one 1810 (containing up to three Disk Storage Drives) can be attached to an IBM 1800. The 1810 Models A1 and B1 consist of a housing that contains a single Disk Storage Drive, and additional fittings and space for two additional Disk Storage Drives. The 1810 Models A2 and B2 contain two Disk Storage Drives; the 1810 Models A3 and B3 contain three Disk Storage Drives.

All three Disk Storage Drives can be attached to a single data channel. However, more flexible operation can be achieved by using a separate data channel for each drive.

FUNCTIONAL DESCRIPTION

The Disk Storage Drive is a small, low-cost storage device that has both random-and sequential-access

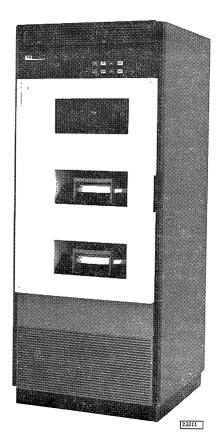


Figure 58. IBM 1810 Disk Storage

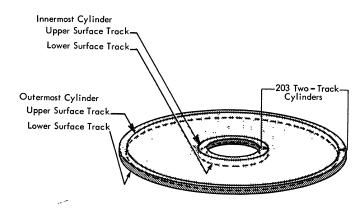
capabilities. It is designed to satisfy the IBM 1800 requirements for low-cost bulk storage.

The disk storage recording medium is an oxide coated disk in an interchangeable 2315 Disk Cartridge (one cartridge for each disk drive).

The access mechanism consists of two parallel horizontal arms that straddle the disk. Each arm has a magnetic read/write head, and each head is positioned to read or write on the corresponding disk surface. The entire assembly moves horizontally allowing the heads to have access to the entire recording area (two surfaces).

Disk Organization and Capacity

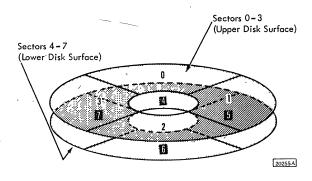
The access mechanism is moved back and forth by program instructions and can be placed in any one of 203 positions, from a point near the periphery of the disk to a point near the center of the disk. As the disk revolves, one of the heads can read or write in a circular pattern on one of the disk surfaces. The circular patterns of data are called tracks. The track of the upper surface of the disk and the corresponding track on the lower surface of the disk are called a cylinder. The total number of cylinders is 203; three cylinders are used as spares to insure that 200 cylinders are available for customer use. The following illustration shows the innermost and outermost cylinders of two tracks each. To complete the picture, visualize that the intermediate cylinders (pairs of tracks) have been omitted for the sake of clarity.



NOTE: The thickness of the disk has been greatly exaggerated in order to show the relative positions of the upper and lower surface tracks.

20254 A

Each track is divided into four equal segments called sectors. Sectors are numbered from 0 through 7. Sectors 0-3 divide the upper surface tracks; sectors 4-7 divide the lower surface tracks. A sector contains 321 data words and is the largest segment of data that can be read or written with a single instruction.



The sector is the basic addressable unit for reading and writing. Each Read or Write command must address one of the eight sectors available to the heads in each cylinder.

Although the capacity of the sector is 321 words, it is recommended that one word be written as a sector address, leaving 320 data words. A command may specify any number of words equal to or less than 321. A zero word count will force an operation complete interrupt with no reading or writing occurring. The 321-word capacity, then, refers only to a maximum number of words that may be transferred with one command and still guarantee at least 235 microseconds before the next sector starts. This allows sufficient time for the issuance of the next XIO. There is no hardware in the 1810 to limit reading or writing to 321 words. Therefore, the program must limit the word count. A 1810 word is composed of 16 data bits, 3 check bits, and one space bit. (The check and space bits do not appear on the P-C Data Channel.) The following illustration shows the organizational components of disk storage. Note that the capacities are based upon the 320-word sector.

No of Per	Word	Sector	Track	Cylinder	Disk
Bits	16	5, 120	20,480	40,960	8,192,000
Data Words		320	1,280	2,560	512,000
Sectors			4	8	1,600
Tracks				2	400
Cylinders					200
3,11110013					29145

Timing

The magnetic disk revolves at 1500 rpm, making the revolution time 40 ms. The word rate is 36 kHz.

There is no timing consideration for switching read/write heads. The shortest time available between the end of a 321 word sector and the beginning of the next sector is approximately 235 μ sec. For every word not used, 27.8 μ sec may be added.

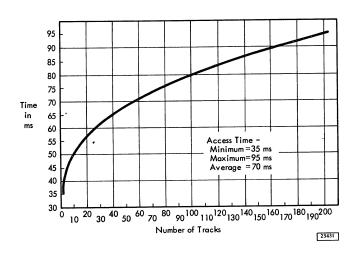
Access Time - Models A1, A2, and A3

The access mechanism, used with the "A" models of the 1810, moves in increments of two cylinders at the rate of 15 ms per increment. Thus, in the formula that follows, the number of cylinders (N) must be even. (The next higher even number is used if an odd number of cylinders is specified.) In addition to the time required to move from one cylinder to another, 20-25 ms must be allowed for carriage stabilization at the addressed cylinder before reading or writing can begin. This delay is handled automatically; an Initialize Read or Initialize Write command issued during this period is executed immediately after the 20-25 ms period. However, 20-25 ms is required between accesses; this is usually accounted for by a Read between each access.

access time (ms) = 7.5 (N) + (22.5 ± 2.5)

Access Time - Models B1, B2, and B3

The access mechanism, used with the "B" models of the 1810, moves in one continuous motion to the cylinder address. Access time including carriage stabilization:



Data Transfer Checking

Data that is transferred between core storage and disk storage is monitored for four conditions that ensure data transfer accuracy.

14 19,0

Parity

All words that pass into or out of the IBM 1800 core storage are checked for odd parity; that is, each word must have an odd number of bits turned on.

Storage Protect

Each core storage address is checked for a storage-protect bit before a new word is placed there. If an attempt is made to transfer data to a protected area, an indicator is set in the 1810 Device Status Word but the operation is not terminated. Data is written from core on the disk storage without this check. The storage-protect bit prevents data transfer from disk to core storage only.

Data Overrun

If a disk drive is not assigned a high enough data channel priority, it is possible for data to be lost. Data overrum checks that the previous word had been transferred to or from core storage before the next word on the disk requires service.

Modulo 4

The disk storage adapter generates up to three additional check bits for each word written. These bits are written at the end of each word so that the total number of bits in each disk storage word is divisible by 4. This divisible-by-4 (Modulo 4) condition is checked as the word is written on the disk and as it is read from the disk.

PROGRAMMING

The IBM 1810 Disk Storage uses one, two, or three 1800 Data Channels.

I/O Control Command (IOCC)

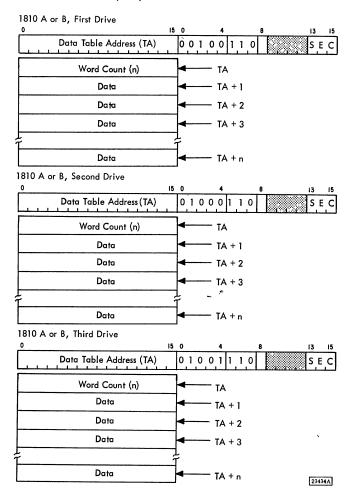
The five-digit area code designates a specific disk storage drive. A different area code is assigned to each disk storage drive.

CE Mode (000)

This command places the disk storage drive in CE mode if modifier bit 15 is on, or removes it from CE mode if modifier bit 15 is off.

23433A

Initialize Read (110)



This command reads a specific number of words (up to 321) from disk storage to the P-C via the Data Channel.

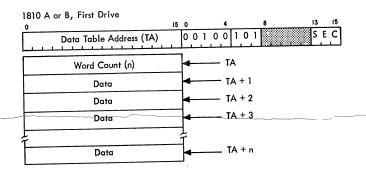
To read more than one sector, a separate Initialize Read command must be given for each sector or portion of a sector to be read.

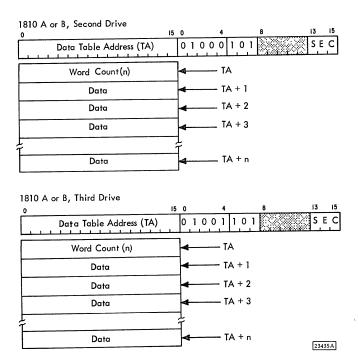
An Operation Complete interrupt occurs when the word count has been reduced to zero. A Device Status Word indicator is set if an error is encountered. The program should provide for repeating Initialize Read commands that show a data transfer error. These errors are often due to temporary conditions that are not present in subsequent tries.

Modifier bit 8 is decoded to determine the specific operation. If B8 equals 0, a Read-into-Memory operation is performed; if B8 equals 1, a Read-Check operation is performed. The difference between Read-into-Memory and Read-Check is that Read-into-Memory causes the read data to be stored in the specified table area, whereas Read-Check simply passes the data through the disk-storage-adapter data register and checks it for modulo 4 errors.

Modifier bits B13, B14, and B15 contain a three-bit binary code that addresses the disk sector to be read. The address word specifies the location, in core storage, of the data table. The data table contains one word for the sector word count plus one word (in ascending sequence) for as many words as are indicated by the sector word count. For example, if the command address word contains 1000, and the sector word count found at that core storage location is 50, then the data will occupy locations 1001 through 1050.

Initialize Write (101)





This command writes a specific number of words (up to 321) from the Processor-Controller to disk storage via a data channel. To write more than one sector, a separate Initialize Write command must be given for each sector or portion of a sector to be written. An Operation Complete interrupt occurs when the word count has been reduced to zero.

Modifier bits B13, B14, and B15 contain the 3-bit binary address of the disk sector to be written.

The address word specifies the core storage location of the data table. The data table contains a word count (n) and n data words. After the word count has gone to zero, zeros are written in the remainder of the sector.

Write Checking: To achieve the maximum level of performance the program should provide for repeating Initialize Write commands that indicate any data transfer error. These errors are often due to temporary conditions that are not present in subsequent tries.

An Initialize Write that does not write correctly because because of temporary or intermittent conditions can be detected immediately by performing a Read-Check operation so that "soft" write errors can be corrected while the data is still available.

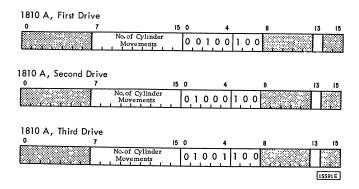
In IBM programming systems, use of Read-Check is optional. The programmer should weigh

the time consumed by error recovery procedures against the time consumed in read-checking.

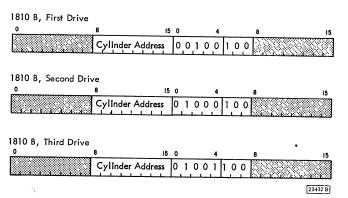
Control (100)

This command causes the carriage to move forward (toward the center) or backward (toward the outer edge or home position). At the end of the Seek Operation an Operation Complete interrupt occurs and the associated bit of the Device Status Word is turned on.

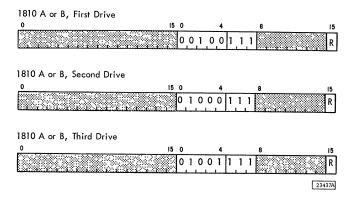
"A" Models: The address word specifies the number of cylinders to be skipped. The range of the address word is 1-202. The modifier specifies the direction of the movement. If bit 13 of the modifier is off, the actuator moves forward, if bit 13 of the modifier is on, the actuator moves backward. If two seek controls are given without a 22.5 millisecond delay between them, an error may occur on the next Read/Write attempted.



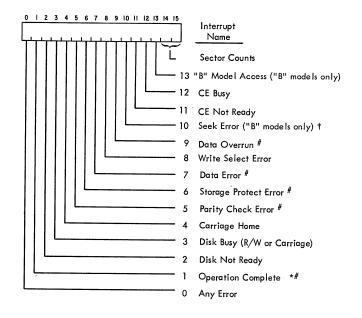
"B" Models: The address word specifies the absolute cylinder address. The range of the address word is 0 to 202. An address greater than 202 will cause a Seek Error and an Operation Complete interrupt.



Sense Device (111)



This command causes the Device Status Word (Figure 59) of the addressed disk storage to be read into the accumulator. All indicators are reset if bit 15 is present in the modifier. The Operation Complete indicator must be reset before a new 1810 Initialize Read, Initialize Write, or Control command is given.



- * Interrup
- # Indicator is reset by a sense DSW (Other indicators reset by their status turnoff).
- † Indicator is reset by a sense DSW if cause was invalid cylinder address. Indicator is reset by next valid seek command if cause was improper termination.

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Figure 59. Device Status Word (1810)

Interrupt Indicator

There is only one interrupt associated with each drive of the 1810: Operation Complete. This interrupt occurs after the last word of the data table has been read, read-checked, or written. This interrupt also occurs at the time the carriage has moved the number of cylinders requested by the XIO Control. It is turned off by a Sense DSW command which has modifier bit 15 on. This indicator must be reset before a new 1810 Initialize Read, Initialize Write, or Control command is given.

Non-Interrupt Indicators (DSW)

Data Error: This bit indicates that either a modulo-4 error was detected or there was a failure to complete reading or writing before the next sector pulse was detected. It is turned off by a Sense DSW command with modifier bit 15 on, if the operation complete indicator is on.

Any Error: This indicator is on if any of the following are on: Data Error, Parity Check Error, Storage Protect Error, Write Select Error, or Data Overrun. (Indicator also on for "B" model Seek Error.) It is turned off when all the individual error conditions are reset.

Parity Check Error: This indicator is turned on when a transfer to or from the B-Register has resulted in a word not having correct odd parity. It is turned off by a Sense DSW command with modifier bit 15 on.

Storage Protect Error: This indicator is turned on when the disk storage attempts to read into a core storage location previously defined as a storage protected area. It is turned off by a Sense DSW command with modifier bit 15 on.

<u>Disk Not Ready</u>: This indicator is on whenever the adapter is not ready to receive a command. When

on it indicates that either the disk is busy, that a 1810 interlock has not been properly satisfied, or that the disk is in CE mode.

Disk Busy (R/W or Carriage): This indicator is on whenever the adapter is executing a 1810 XIO and is not in CE mode.

CE Not Ready: Same as Disk Not Ready but active only while 1810 is in CE mode.

CE Busy: Same as Disk Busy but active only while in CE mode.

Carriage Home: This indicator is on if the carriage is in the home position (cylinder zero).

Sector Counts: These bits identify the pair of sectors which are next available for reading or writing.

<u>Data Overrun:</u> This indicator is turned on when a word on the disk requires service and the transfer of the previous word is not completed. It is turned off by a Sense DSW command with modifier bit 15 on.

Write Select Error: Failure in write selection circuitry which could result in loss of data turns this indicator on. It can be turned off only by stopping the disk drive motor.

Seek Error (1810 "B" Models): This indicator turns on when an access operation is not terminated within 200 ms (turned off by next valid Seek command) or when a cylinder address greater than 202 is specified (turned off by a Sense DSW command with modifier bit 15 on). The Seek Error causes an Operation Complete interrupt.

"B" Model Access (1810 "B" Models): This bit identifies the disk storage as a "B" model. The 1810 B1, B2, and B3 require absolute cylinder addresses for accessing operations.

Industry, science, research, government — all are faced with the need for collecting increasing amounts of data within decreasing time scales. Physical measurements must be monitored and quantified with greater speed and accuracy than ever before. The collection of analog data and its conversion for presentation to the digital Processor-Controller is the function of the Analog Input features.

A physical phenomenon is first sensed and converted to an analog electrical signal by sensors or transducers, such as thermocouples or strain gages. Electrical signals from sensors or transducers may be in the millivolt, volt, or milliampere range. Low voltage signals (less than 1 volt) must be amplified to a level acceptable for conversion to digital form. All customer lines from transducers are terminated at the control system on screw-down terminals. The signals are also conditioned at the terminals, including the filtering of extraneous signals, known as noise.

Conversion of analog signals from a voltage level to digital information is accomplished by an Analog-to-Digital Converter (ADC). Such converters, however, are complex enough so that if multiple sources of analog signals are to be converted, they share the use of one ADC. The switching is accomplished by a multiplexer. The data path from sensor or transducer to processor is shown in Figure 60.

ANALOG INPUT UNITS AND FEATURES

The Analog Input Units and features provide modular packaged equipment used to convert voltage or current signals to digital values. The modules used

to accomplish the conversions include analog-todigital converters, multiplexers, amplifiers, and other signal conditioning equipment.

The units and features that accomplish the analog input function are briefly introduced below, followed by more detailed descriptions. A description of the operation of analog input and its relation to the P-C is given later in the Programmed Operation section.

As shown in Figure 61, customer input signals are routed through termination, signal conditioning elements, multiplexer switches, an amplifier (low level signals only), and into the analog-to-digital converter (ADC). The output of the ADC is presented to the P-C via the I/O control or the Data Channel from the ADC output register.

1851 Multiplexer Terminal — Model 1: A modular chassis which mounts in an 1828 enclosure; up to 64 analog input multiplexer points (2 wire), signal conditioning elements for each point. This chassis houses either solid state multiplexers or relay multiplexers. When relay multiplexers are installed, up to two differential amplifiers can be mounted in each terminal.

1851 Multiplexer Terminal — Model 2: Similar to Model 1: However, thermocouples can also be directly connected and 62 multiplexer points are the maximum. A cold-junction temperature indicator device (RBT) is included in the terminal.

Multiplexer (Relay): The relay multiplexer provides switching for both high-level differential inputs and low-level differential inputs, allowing all Mpx/R inputs to use a common Analog-Digital Converter

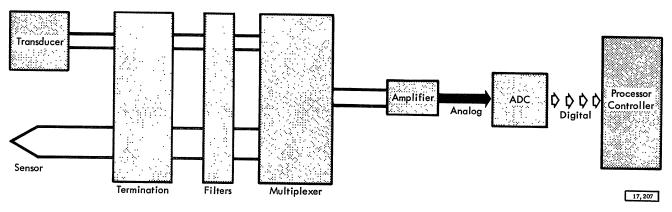


Figure 60. Data Path From Signal Source to P-C

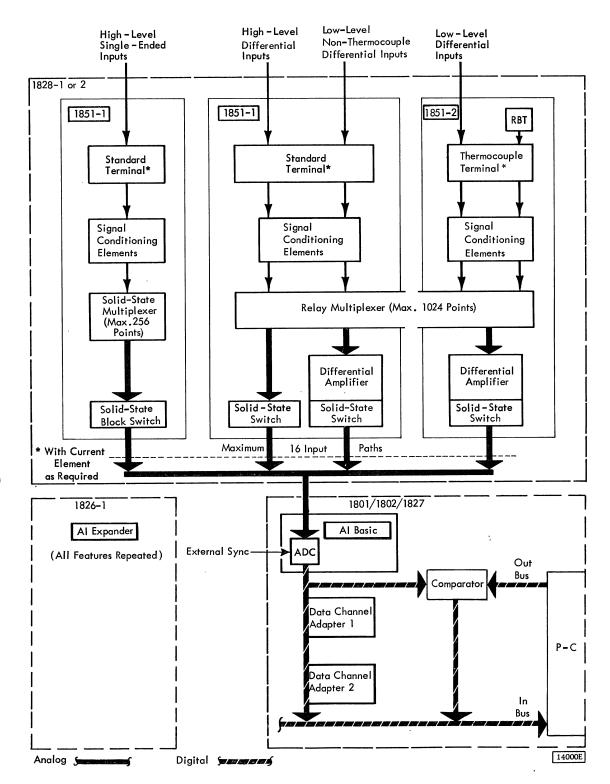


Figure 61. Interconnection of Analog Input Features

127

(ADC). Up to 100 points per second switching rate can be attained.

Multiplexer/S (HLSE): A solid state, high-level single-ended (HLSE) multiplexer to provide high-speed switching of analog input signals to allow use of a common analog-to-digital converter.

Multiplexer Overlap: This feature allows overlap of solid state and relay multiplexing.

Multiplexer/R Control and Multiplexer/R Control Additional: These features provide the necessary control circuitry to operate the Multiplexer/R points. Each feature can control up to 256 points.

Multiplexer/S Control: Control circuitry to operate the Multiplexer/S points is provided by this feature.

<u>Differential Amplifier</u>: A time shared amplifier to raise each low level signal to the 5 volt level of the ADC. Up to 256 Multiplexer/R points can use the same amplifier. It has one range setting: ±10 mv, ±20 mv, ±50 mv, ±100 mv, ±200 mv, or ±500 mv.

ADC - Model 1: Converts analog signals (±5 volt range) to digital values (8, 11, or 14 bits plus sign). This model provides a nominal 10 kc system conversion rate.

ADC - Model 2: Similar to ADC Model 1 but includes a Sample and Hold Amplifier for increased system conversion rates. The nominal system conversion rate is 20 kc for this model.

AI Data Channel Adapter - 1: Allows sequential reading of input points with one initialize read instruction via cycle steal cycles using one channel address register.

AI Data Channel Adapter - 2: Allows random reading of input points with one set of initialize read and write random instructions via cycle steal cycles using two channel address registers.

Comparator: Performs range checking on digital values developed by the ADC. The high and low limits are selectively obtained from the Processor-Controller for those values to be checked. When values are determined to be out-of-limit, then an interrupt informs the P-C. Only one P-C cycle is required for each value to be limit checked.

Analog Input Expander. Allows a complete analog input system to be configured around the 1826 Data Adapter Unit. Thus, a second ADC or simply a separated ADC may be added to any 1800 System.

 $\frac{\text{Multiplexer/R and Multiplexer/S Maximums and}}{\text{Ranges:}} \text{ Although the maximum number of Multiplexer/R points and Multiplexer/S points are 1024}$

and 256, respectively, both maximums cannot be installed within the same system. The simultaneous maximums for each system are dependent upon the number of analog input ranges.

Number of	Mpx/R *	Number of	Number of Low
Mpx/S *	Points	Differential	Level Ranges
Groups	(Maximum)	Amplifiers	(Maximum)
0.00	(**************************************	(Maximum)	,
0	256 HL +768 LL	15	6
	No HL +1024 LL	16	6
1	256 HL +768 LL	14	6
	No HL +1024 LL	15	6
2	256 HL +768 LL	13	6
	No HL +1024 LL	14	6
3	256 HL + 768 LL	12	6
	No HL +1024 LL	13	6
4	256 HL +768 LL	11	6
	No HL +1024 LL	12	6
5	256 HL +768 LL	10	6
	No HL +1024 LL	11	6
6	256 HL +768 LL	9	6
	No HL +1024 LL	10	6
7	256 HL +768 LL	8	6
	No HL +1024 LL	9	6
8	256 HL +768 LL	7	6
	No HL +1024 LL	8	6
9	256 HL +768 LL	6	6
	No HL +1024 LL	7	6
10	256 HL +768 LL	5	5
	No HL +1024 LL	6	6
11	256 HL +768 LL	4	4
	No HL +1024 LL	5	5
12	256 HL +768 LL	3	3
	No HL +1024 LL	4	4
13	256 HL +512 LL	2	2
	No HL +768 LL	3	3
14	256 HL +256 LL	1	1
	No HL +512 LL	2	2
15	256 HL + No LL	0	0
	No HL +256 LL	1	1
16	No HL + No LL	0	0

Multiplexer/R input ranges are \pm 10, \pm 20, \pm 50, \pm 100, \pm 200, and \pm 500 millivolts for input to a differential amplifier, and \pm 5.0 volts for direct input to the ADC. The only Multiplexer/S input range is \pm 5.0 volts for direct input to the ADC.

1851 MULTIPLEXER TERMINAL

The 1851 Multiplexer Terminal is a modular chassis in which multiplexing and signal conditioning features can be mounted. The 1851 terminals are mounted in an 1828 enclosure. Up to 19 terminals can be included.

for any one ADC in a system. Multiplexer/R and Multiplexer/S cannot be installed in the same 1851 terminal unit.

There are two models of the Multiplexer Terminal. The Model 1 provides for the insertion of up to 64 multiplexer points in groups of 16 points. Customer wires are terminated on screw down terminals. The Matching Elements are available for each Multiplexer Terminal. Up to two Differential Amplifiers can also be mounted in each terminal.

The Model 2 is a modified terminal to allow for thermocouple termination, cold junction thermal stabilization, and a Resistance Bulb Thermometer (RBT) circuit. These elements are used to determine coldjunction temperature. Thus, thermocouple wires can be connected directly to the terminals and the coldjunction temperature can be computed by the P-C. The maximum capacity of the Model 2 is 62 multiplexer points. Two multiplexer addresses are used for the cold-junction temperature signal measurement (00 is RBT reference; 01 is RBT bridge output voltage).

These are the first two addresses that are installed in any 1851 Model 2. The first Multiplexer/R group has only 14 analog input multiplexer points available for external source signals. The ranges for this group must be ± 10 , ± 20 , or ± 50 millivolt.

It is important that both readings be taken at intervals which are small compared with significant ambient temperature change intervals. Separate readings are required for each Model 2 Multiplexer Terminal.

All other functions of the Model 2 Terminal are the same as the Model 1 Terminal. Thus nonthermocouple signals may be terminated in the Model 2 (if required by the System configuration).

MULTIPLEXER/R

The Multiplexer/R feature provides for relay multiplexing of high or low level analog inputs at a maximum speed of 100 points per second. The equipment is card-mounted and plugs into the Multiplexer Terminal in groups of 16. Up to 16 groups can be combined to form the input to one differential amplifier providing up to 256 input points per amplifier. Each amplifier has a fixed range. The full scale input range for any group of Multiplexer/R points depends on the range of the amplifier to which it is connected. Ranges available are: ±10 mv, ±20 mv, ±50 mv,

 ± 100 mv, ± 200 mv, and ± 500 mv. High level inputs (-0.5 to +5.0 volts) do not require an amplifier.

The Multiplexer/R can operate with a maximum of 200 volts common mode (DC or peak to peak AC).

MULTIPLEXER/S (HLSE)

The Multiplexer/S feature provides for solid-state multiplexing of high-level, single-ended (HLSE) analog inputs. System speeds are dependent upon the ADC, amplifier, etc., used in any particular system. The Multiplexer Overlap feature allows the overlapping of Multiplexer/R and Multiplexer/S associated with any single ADC on a system. Groups of Multiplexer/S are mounted in the Multiplexer Terminal-Model 1 and cannot be intermixed with Multiplexer/R points within a terminal.

The input voltage range is ± 5 volts full scale. When used with the ADC Model 1, conversion rates can be as high as 10,000 conversions per second with about 50 microseconds sample time.

A Sample and Hold Amplifier in the ADC Model 2 permits conversion rates to be increased to as much as 20,000 conversions per second with about 12 microseconds sample time.

Multiplexer Overlap

Several methods of overlapping Multiplexer/R and Multiplexer/S are possible.

Overlap Without Special Feature

There are two conditions by which overlapping can occur without the overlap special feature.

 Using the direct programmed control mode of operation, the selection of a point in the relay multiplexer may be started and then a series of conversions of solid state points may be performed while the relay point is being selected.

When the relay multiplexing is complete, it obtains use of the ADC for conversion of the relay point. When the conversion of the signal at the point is completed and the resultant data in the ADC register is available, an interrupt is activated. Solid state and relay point interrupts are differentiated by programmed interrogations of the Analog Input, Device Status Word (DSW).

An interrupt resulting from the completion of an input point conversion (either relay or solid-state point) suspends selection of another point until the converted value has been read into core storage.

If a discrete conversion of a relay point is started under programmed control, a sequence of conversions of solid state points can be started on Data Channels. When the relay multiplexing is complete, it obtains use of the ADC for conversion of the relay point. When the resultant converted data is available in the ADC register, an interrupt is activated. This is the normal "DPC conversion complete" interrupt utilized for discrete conversions under programmed control. If the solid state conversions have not been completed when the relay multiplexer control captures the ADC, then the solid state conversions are continued as soon as the ADC Register has been cleared. No further discrete conversion may be started until the solid state conversions are complete.

Overlap With Special Feature

With the Multiplexer Overlap special feature another means of overlapping is possible. Under two-Data-Channel operation, relay addresses can be interleaved with solid-state multiplexer addresses.

These addresses do not have corresponding ADC values placed in the ADC converted data table. The relay point addresses are latched by the relay multiplexer control, and the interface control requests a further cycle to obtain the next solid-state multiplexer address from P-C memory. Random conversions proceed asynchronously until the relay multiplexer is ready. When the relay multiplexer is ready, the relay multiplexer takes control. The next point converted will be a relay point and an Interrupt will allow the P-C to transfer the value in the ADC Register to core storage under XIO-Read control, after which conversions are continued under Data Channel control. If another relay address is recognized before the first relay point has been converted, an interrupt occurs. This interrupt informs the P-C that a relay point was mislocated in the address table. The mislocated relay point will not be converted. A relay point cannot be the last word in a data table when the overlap special feature is installed.

Efficient use of overlapping of relay and solid state multiplexing depends upon correct placement of addresses in the Multiplexer Address Data Table. Enough solid state multiplexer addresses must be included between relay addresses to ensure that

sufficient time is always taken so that the first relay point is converted and relay multiplexer control is ready. Approximately 100 Mpx/S points can be converted with ADC Mod 1 and 200 Mpx/S points with ADC Mod 2 while one Mpx/R point is being selected.

SIGNAL CONDITIONING ELEMENTS

Signal Conditioning Elements listed below provide passive signal conditioning of each analog input signal at the terminal. For specifications and characteristics of each element, see 1800 Data Acquisition and Control System Installation Manual, Physical-Planning, Form A26-5922.

- 1. Current Element. 4 20 ma current input signals are converted into either 0.1 to 0.5 volt or 1 to 5 volts. Current elements can be installed with Multiplexer/S or Multiplexer/R. A current element cannot be used with a voltage element.
- 2. Filter Element (Multiplexer/R only). A low-pass passive filter to reject normal mode ac noise. Filter elements cannot be installed for use with Multiplexer/S.
- 3. a. Voltage Element (Multiplexer/S). Provides 2:1 voltage attenuation. This element provides for intermixing 10 volt and 5 volt signals within the same Multiplexer/S group.
 - b. Voltage Element (Multiplexer/R). Provides 2:1 voltage attenuation. For example, this allows intermixing of 100 millivolt signals and 50 millivolt signals in the same Multiplexer/R group. Voltage elements for Multiplexer/R provide the filtering function described under Filter Element. A Filter Element cannot be installed on points for which a Voltage Element is ordered.
- Connector Element. Is wired for straight through connection with no signal conditioning.
- 5. <u>Custom Element</u>. Is available for customer mounting of special conditioning circuits to meet a particular requirement.

DIFFERENTIAL AMPLIFIER

This is a time-shared amplifier used in conjunction with the Multiplexer/R, to raise analog signals to the ADC input level of ± 5 volts.

Gains available are: 500, 250, 100, 50, 25, and 10. These allow input voltage ranges of Multiplexer/R points to be specified for: ± 10 , ± 20 , ± 50 , ± 100 , ± 200 and ± 500 millivolts.

A single amplifier can service up to 256 input points (16 blocks of 16 multiplexer relays). Up to two amplifiers can be mounted in one Multiplexer Terminal. Thus, multiple amplifiers can be used for voltage range changing in place of passive Voltage Elements.

ANALOG-DIGITAL CONVERTER (ADC)

The ADC provides the 1800 with the ability to convert bipolar analog signals (±5 volt signal range) to digital values. Two models are available: Mod 1 includes a buffer amplifier and has program selectable resolutions of 8, 11, and 14 bits. Mod 2 is similar to the Mod 1 except that it includes a sample and hold amplifier which provides for increased system speed of conversion.

The ADC conversion time depends only upon the number of bits of output that are to be developed. Conversion times are as follows: 8 bits, 29 μ sec; 11 bits, 36 μ sec; and 14 bits, 44 μ sec. The input impedances of the ADC Mod 1 and Mod 2 are 10 megohms and 0.1 megohms, respectively.

The 1800 System conversion rates will vary from 9,000 to 24,000 samples per second (dependent upon equipment installed and mode of operation).

Analog Input Calibration

The analog input calibration facility is housed in the 1828 Enclosure that is abutted to the 1801, 1802, or 1826 containing the Analog Basic.

Power is supplied to the calibration facility through the power switch on the front left side of the 1828.

The calibration facility provides the following dc reference voltages for calibration of AI features when the calibration facility is connected directly to an appropriate 1851 input terminal pair:

+5 volts	100 mv
-5 volts	50 mv
500 mv	20 mv
200 mv	10 mv

Exact voltages are measured at the factory and are recorded (to five significant digits) on the reference unit. Note that connections for +5 volt and -5 volt ranges are different.

A special high-level input point is selected by multiplexer address 13E8₁₆ (which is outside the normal range of Mpx/S addresses) for ADC calibration only. The multiplexed calibration point can be addressed at any time by the customer program or diagnostic program for an operational check of the ADC. The reference voltage to be addressed is selected by changing connections on a terminal strip. An IBM Customer Engineer changes the connections on the terminal strip.

Data Word

The data word developed in the ADC Register is compatible with 1800 word format as shown below. The data word allows for sign plus 14 bits resolution. Conversion by the stored program of the value presented by the ADC should assume a position for the binary point. This position of the binary point does not change when the format (14, 11, or 8 bit) is changed. Only the number of significant bits in the ADC converted value changes. Negative numbers are in 2's complement form.

	0	ĺ	2	3	4	5	6	7	8	9	10	11	12	13	14	15
14-Bit Format	±	Х	X	Х	Х	Х	Х	Х	Х	Х	Х	X	X	Х	X	I
11-Bit Format	±	X	Х	Х	Х	Х	Х	Х	Х	Х	Х	х	1	0	0	I
8-Bit Format	±	х	х	х	х	Х	х	х	х	1	0	0	0	0	0	I

NOTES:

- 1. \pm is the sign of the data: a zero bit is positive, and a one bit is negative.
- The X's indicate that a one or zero bit may appear to represent the converted value. In the 11 and 8-bit formats, the 0's indicate that only a zero will appear in these positions.
- 3. I is the overload indication bit. The presence of a one bit indicates an overload condition; that is, the signal was outside the ±5 volt range. Bit 15 is a one when a positive value has all one bits in bit positions 1–8 (11 or 14) or when a negative value has all zero bits in bit positions 1–8 (11 or 14).
- 4. The one bit in bit position 9 of the eight bit format and bit position 12 of the 11-bit format are provided for half-adjust of the quantizing error. Half-adjust of the 14-bit format quantizing error is accomplished by the ADC circuitry.

29128

14-BIT RESOLUTION		Bit Positions
	EXAMPLE	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
	Normal Positive Binary Value	0,0,0,0,0,0,0,1,0,1,1,1,0,1,1,0
	Decimal Equivalent	+187
	Maximum Positive Value without Overload	0, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1,
	Decimal Equivalent	+16382
ļ	Normal Negative Binary Value	1,1,1,1,1,1,1,0,1,0,0,0,1,0,1,0
ļ	Decimal Equivalent	-187
	Maximum Negative Value without Overload	1,0,0,0,0,0,0,0,0,0,0,0,0,1,0
	Decimal Equivalent	-16383
	Positive Overload Condition	0, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1,
	Negative Overload Condition	1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,

Note:

Decimal equivalents assume that the binary point is between bits 14 and 15.

Buffer Amplifier

The Buffer Amplifier is a single-ended operational amplifier and is an integral part of the Mod 1 ADC. The amplifier provides high-input-impedance (10 megohms) buffering of the ADC on a time-shared basis for those applications where it is unnecessary to provide a time-shared sample-and-hold input characteristic.

Sample-and-Hold Amplifier

The Sample-and-Hold Amplifier is an integral part of the Mod 2 ADC; it is a single-ended amplifier capable of providing a short aperture time in the sampling of high-level analog signals and of providing a high accuracy hold function. The amplifier has an input impedance of 100K ohms. The P-C program must consider the reversed polarities obtained from sample-and-hold input points.

External Sync

The operation of the ADC can be controlled by an external timing (sync) pulse. When the Relay Multiplexer is used, a "ready" condition is transmitted to the external timing device after the Relay Multiplexer and relay block switches have settled. When the Solid-State Multiplexer is used, a "ready" condition is transmitted before the solid-state switches are actuated. The external device provides a sync start pulse which allows the solid-state switches in either type multiplexer to be actuated and then conversion of the selected signal begins.

An "8" bit in the modifier of an IOCC, either "Write" or "Initialize Read," sets up the external sync mode. The absence of an "8" bit in the modifier of either a "Write" or "Initialize Read" command terminates the external sync mode.

External sync cannot be used during overlap (special feature) operations.

COMPARATOR

The Comparator performs selective checking on the digital values converted by the ADC. A range type check is made to confirm that the converted values are within specified limits. The limits are obtained from the Multiplexer Address Table (one P-C cycle delay allows both limits to be acquired) whenever a check is required. The P-C is informed of an out-of-limits condition by interrupt. The two Analog Input Data channel adapter features are a prerequisite to this feature.

Operational Description

In order that a range comparison can be made, both a high limit and a low limit must be set. In converting many analog input source signals, it may be necessary to monitor each signal to assure that the signal remains within specified bounds. Normally, a number of these signals are redundant and other signals need only be checked occasionally. To allow for flexibility of checking input signals, a separate control (in Multiplexer Address word) is added to instruct the Comparator to perform checking when required.

It should be noted that limit words need not remain static. For example, when a particular high limit is exceeded, then a single change will permit

recognition of the return of the signal within the former limits. The high limit is substituted for the low limit and the maximum value is set for the high limit. If the interval timer is read after each limit is exceeded, then the time interval that the signal was out-of-limits is known.

Limit Words

The high and low limits are stored in P-C storage within the Multiplexer Address Table (See Figure 62). These limit values are expressed in eight bits (seven bits plus sign) with negative numbers represented in two's complement form. The Comparator is only used under the Random Mode of Operation (see Programmed Operation section). A limit word follows each Multiplexer Address entry that is to be checked. The Multiplexer Address entry contains two control bits in addition to the analog input point address. These bits are stored in bit positions one and two of the multiplexer address word. The L-bit, stored in bit position one, indicates the presence of a limit word as the next word in core storage. The K-bit, stored in bit position two, indicates whether or not a comparison is to be performed.

Figure 62 shows a sample Multiplexer Address table. The word count and scan control bits are obtained from the data table that receives the converted values. The chain address from this table is used to provide unique chaining. If the Multiplexer Overlap feature is installed, a limit word cannot follow Multiplexer/R addresses.

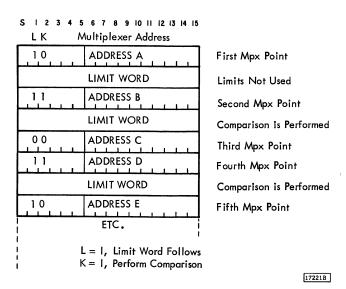


Figure 62. Multiplexer Address Table with Limit Words

Comparison Cycle (L = 1, K = 1)

When the ADC register is filled with the value to be limit checked (7 high-order bits plus sign during conversion), the limit word is acquired from storage and the limit comparison is performed.

Out-of-Limits Conditions

When the comparator determines that an out-of-limits condition exists, then bits identifying the multiplexer point and the type of condition involved are saved in the comparator. An interrupt unique to the comparator is activated to alert the processor-controller, and further comparisons are suppressed. This suppression has an identical effect to the recognition of zero K-bit in the multiplexer address.

Comparison to limits in step with multiplexing is automatically restarted when the Comparator Status Word has been sensed by the processor-controller. The Comparator Status Word enters the accumulator upon execution of a sense instruction.

The out-of-limit conditions are

- High out-of-limit when ADC value is equal to or greater than the high limit.
- Low out-of-limit when ADC value is less than the low limit.

ANALOG INPUT EXPANDER

This feature provides two prinicpal advantages:

- 1. It doubles the capacity of the analog input features.
- 2. It allows the analog input features to be structured separate from the Processor-Controller.

The Analog Input Expander is a feature of the 1826 Data Adapter Unit, which provides the basic capability for attachment of an ADC, Comparator, Multiplexer Terminals, etc. This second analog input system attaches to I/O Control and Data Channels in a manner similar to the first analog input system. Thus the system conversion rates can be doubled, neglecting I/O interaction.

PROGRAMMED OPERATION

This section describes the control modes that are available for the selection of analog input points, conversion of the selected analog signal to a digital

value, and the transfer of the digital value to the P-C.

There are three basic control modes for the input of analog data: (1) Direct Program Control (DPC), (2) Data Channel Sequential (DCS), and (3) Data Channel Random (DCR). They are described in detail below. Essentially the <u>DPC</u> mode requires the execution of at least one XIO instruction (see <u>I/O Control</u>) for each value that is read into the P-C. The <u>DCS</u> mode uses one Data Channel and allows any number of groups of sequentially addressed values to be read into the P-C with the execution of one instruction (XIO). Sequentially addressed values are those which are developed from multiplexer addresses in sequence. That is, values with multiplexer addresses 23, 24, ... 46 would constitute a sequential group of 24 points.

The <u>DCR</u> mode uses two Data Channels and allows each point to be addressed uniquely. Any number of groups of points may be addressed, converted, and read into the P-C with the execution of two XIO instructions.

Direct Program Control

Using the Direct Program Control mode of operation, two Execute Input/Output (XIO) instructions are used. The first instruction, an XIO Write, addresses the multiplexer and selects the analog input point which is to be converted. Upon completion of multiplexing, an internal signal is sent to the ADC to start the point conversion. When the ADC has completed the conversion, an interrupt signal is sent from the ADC to the P-C. The P-C initiates a subroutine (for interrupt description, see Interrupt section) to determine the cause of interrupt, if necessary, and provides the second instruction, an XIO Read, to transfer the data to storage. This mode of converting data from analog signal to digital value in storage is a discrete addressing method; that is, two instructions result in the acquisition of data from one input point.

Direct Programmed Control Sequential: A special mode of DPC can be used if the analog points are to be converted in sequence. This mode requires only one write followed by a series of reads - one for each point. A bit in position 8 of the IOCC addressed by the XIO Read instructs the multiplexer to increment by one the address previously converted and then to perform the next cycle. A cycle here is composed of selecting the analog input point, converting the selected analog signal, and initiating an interrupt to inform the P-C that the converted value is in the

ADC register ready to be read into P-C storage. The absence of a bit in position 8 of a Read IOCC terminates the operation.

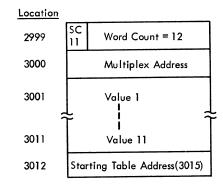
Data Channel Sequential Control

Using a single Data Channel, a sequence of analog inputs can be scanned, converted, and stored in core storage with one XIO Initialize Read instruction to initiate the action. The two word IOCC contains the core storage address where the Scan Control bits and the Word Count are stored for the operation. The Word Count is one greater than the number of input signals to be converted in the sequence. The Scan Control bits determine if an interrupt is given and whether or not chaining or termination of the operation is effected when the Word Count reaches zero.

The Word Count is in the first word of the first Data Table (Figure 63). Note that the Word Count precedes the multiplexer address word which is at location 3000 in this example. The Data Channel "writes" this multiplexer address word to the Analog Multiplexer Address Register (AMAR) which initiates the selection of analog points and conversion to digital values. At the completion of each conversion, the converted data is read into sequential storage locations. After each transfer of data, the Word Count is decremented by one and the previous address in the AMAR is incremented by one. The new address causes the next sequential point to be selected. This operation continues until the word count reaches zero.

Figure 63 illustrates two data tables which are in core storage and could be used for Chained Sequential Operation. The IOCC word that initiates this analog input function is located in storage locations 3042 and 3043 (Figure 63). The IOCC initializes the multiplexer and the ADC and then places the address of the Word Count (the first word in the table) in the Channel Address Register (CAR) of the Data Channel. In this example, the Word Count is located in storage location 2999.

The ADC now requests a cycle to place the word count into the Word Count Register (WCR). In this example, the word count is 12. CAR is incremented by one so that now CAR contains the address 3000. On the next cycle, the initial multiplexer address is transferred from location 3000 to the AMAR. When multiplexing is complete, a signal is sent to the ADC to start conversion. At the completion of conversion, the ADC register contains a digital value and a cycle steal request is made. CAR (now containing address 3001) addresses core storage and the digital value in the ADC output register is transmitted to location 3001.



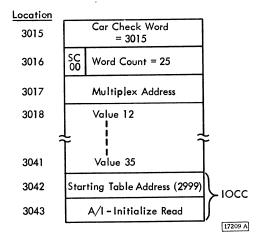


Figure 63. Data Table, Chained Sequential Control

The above procedure is repeated and continues until the WCR reaches zero. At this time, the Scan Control bits are monitored and it is discovered that they indicate continued scanning (11). When continuous scan is indicated by the Scan Control Register, the Data Channel takes four cycles to initialize the I/O device for the next data table. The first cycle transfers the word following the first data table to CAR (this word contains the core-storage location of the next table). The second cycle addresses core storage and transfers the contents of the first word to the B-register. A CAR check is then made (see section Channel Address Register Check). The third cycle transfers the Word Count and Scan Control bits from the second word of this data table to their respective registers in the I/O device. The fourth cycle transfers the Multiplexer address from the third word of the data table to the analog Multiplexer Address Register (AMAR). Data transfers then resume on a cycle steal basis.

When the Word Count Register again reaches zero, the Scan Control bits indicate that the operation will be terminated (00 also indicates an

interrupt). The operation is terminated and a new XIO instruction is required to initiate further operation.

Data Channel Random

In this mode of operation, the multiplexer addresses are transmitted on one Data Channel and the ADC data is transmitted on a second Data Channel. The operation is initiated with two XIO instructions. The first instruction sets up the controls for transferring converted data from the ADC to storage on one channel and loads the Scan Control Register (SCR) and the Word Count Register (WCR) for the operation. The Word Count is equal to the number of converted values to be stored.

The second instruction initiates the transfer of the multiplexer addresses from core storage to the Analog Multiplexer Address Register (AMAR) on the other Data Channel.

When the first analog input point has been selected, a start impulse is given to the ADC. At the completion of the first conversion, a storage cycle transfers the converted data to the set-up Data Table in the P-C. Alternate P-C cycle requests bring in the multiplexer addresses on one channel and transfer the converted data to storage on the other channel. This operation continues until the WCR is decremented to zero. When the WCR reaches zero, the Scan Control bits are interrogated to determine if an interrupt is to be given and whether the operation is to continue or terminate.

Figures 64 and 65 illustrate the multiplexer address and ADC storage tables which are to perform a random addressing operation. An XIO instruction referencing location 3524 initiates ADC action. Another XIO instruction referencing location 3122 initiates multiplexing.

In this example (Figures 64 and 65), 119 points are being read and converted in a random sequence. The two ADC tables are chained together while the multiplexer table is chained to itself. The Scan Control bits cause an interruption at the end of each ADC table. The number of multiplexing addresses set up in the Multiplexer Address table must equal the word count set up in the ADC table. Comparator limit words are not included in the word count.

Systems with two Data Channels may convert values using any mode. The mode is selected by appropriate bits in the Function or Modifier of the IOCC. In the Chained Sequential Mode (with two Data Channels), the Data Channel used by the Multiplexer is not used, and the operation is the same as that previously described under Chained Sequential Order.

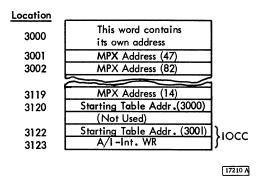
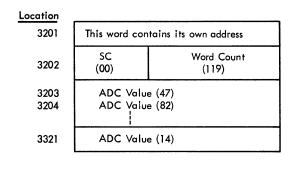
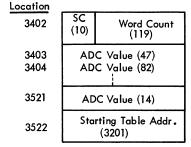


Figure 64. Multiplexer Address Table, Random Addressing





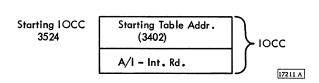


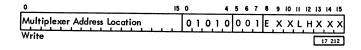
Figure 65. ADC Storage Tables, Random Addressing

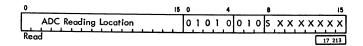
A one in bit position 10 of the Initialize Read IOCC specifies random mode, and a zero in bit position 10 of the IOCC specifies sequential mode.

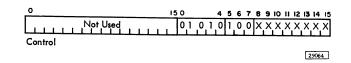
If the overlap feature is used, the ADC word count is equal to the number of solid state points. Since relay points are read by Direct Program Control, they are not stored in the ADC Storage table.

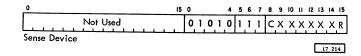
I/O CONTROL COMMANDS - ANALOG INPUT

DIRECT PROGRAM CONTROL

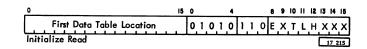


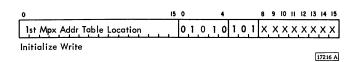






DATA CHANNEL





where:

01010 is the assigned Area for Analog Input. XX is not used.

C a one bit specifies Comparator status word; no bit specifies Analog Input status word.

E a one bit means External Synchronized.

L a one bit specifies Low Resolution - 8 bit plus sign.

H a one bit specifies High Resolution – 14 bit plus sign.

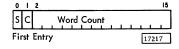
R a one bit resets indicators.

S a one bit specifies Sequential Programmed

T a one bit specifies Two Data Channel Operation, Random Mode.

Notes: 1. No L or H-bit specifies 11-bit resolution. 2. The Area Code (01010) is replaced by Area Code (10000) when AI Expander is used.

Data Table Formats



where SC are the Scan Control Bits

S One bit causes chaining to occur.

C No bit causes interrupt at end of Table.



where:

S Sign bit.

O One bit indicates Overload.



where:

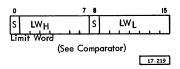
X Means not used.

K a one bit means Perform Comparison (see Comparator).

L a one bit means Limit Word follows (see Comparator).

Q a one bit signifies Solid State Multiplexer; No bit, Relay Multiplexer.

M-M Multiplexer Address.

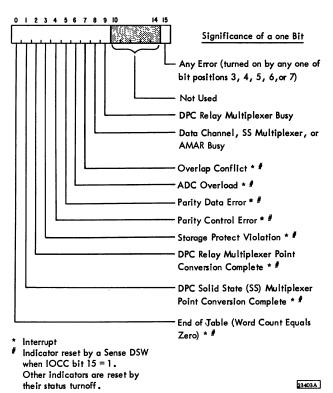


where:

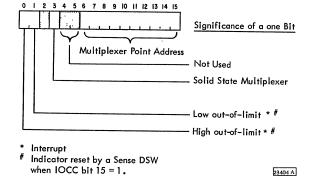
н

Device Status Format

The execution of an XIO Sense Device instruction with the area code specifying Analog Input (01010) or AI Expander (10000), when C (bit 8 of the modifier) is a zero bit, will cause the Device Status Word to be read into the accumulator. The bits of the Device Status Word are:



With a Comparator, an additional Device Status Word is addressed by an XIO instruction (IOCC) with C (bit 8 of the modifier) as a one bit:



Note: All Analog Input Basic interrupts are combined into one interrupt signal assigned to an interrupt level and ILSW bit; all Analog Input Expander interrupts are combined into one interrupt signal assigned to the same interrupt level as AI Basic but to a different ILSW bit. All Comparator (AI Basic) interrupts are combined into one signal assigned to an interrupt level and ILSW bit; all Comparator (AI Expander) interrupts are combined into one interrupt signal assigned to the same interrupt level as AI Basic Comparator but to a different ILSW bit. Analog Input and Comparator interrupts can be assigned to the same or different interrupt levels.

Analog Input Indicators

End of Table: Turned on and causes an interrupt when: 1) the end of a table is reached during a Data Channel operation, and 2) the Scan Control bits have specified an interrupt at the end of table.

<u>DPC SS Conversion Complete:</u> Turned on and causes an interrupt in a Direct Program Control (DPC) operation when a Solid State (SS) Multiplexer point conversion is complete and the converted data is ready to be transferred to core storage.

DPC Relay Conversion Complete: Turned on and causes an interrupt in a DPC operation when a Relay Multiplexer point conversion is complete and the converted data is ready to be transferred to core storage.

Storage Protect Violation: Turned on and causes an interrupt when the program tries to store converted ADC data into a "read only" core storage location. Analog input operations are halted.

Parity Control Error: Turned on and causes an interrupt when a transmission parity error is detected during a control cycle. It is also turned on when a transmission or P-C parity error is detected during loading of the word counter or loading the AMAR or during loading or checking of CAR during a cycle stealing operation. Analog input operations are halted.

Parity Data Error: Turned on and causes an interrupt if a parity error is detected when multiplexer

address or converted data are transmitted between the P-C and analog input interface.

ADC Overload: Turned on and causes an interrupt when input to the ADC exceeds the range of the ADC.

Overlap Conflict: Turned on and causes an interrupt when a second relay point is addressed before the first relay point has been converted during a two data channel overlap operation.

Data Channel SS, Mpx, or AMAR Busy: Turned on when the SS Multiplexer is addressed, or during a DC operation (relay or SS), or when the analog multiplexer address register (AMAR) is busy. The indicator is turned off when the word count equals zero with no chaining, or a DPC solid-state conversion is completed, or AMAR is no longer busy. No new instruction can be initiated except Sense Interrupt Level, Sense Device, or Control when this indicator is on.

DPC Relay Busy: Turned on when a Relay Multiplexer is addressed by a Write function, or when a Relay Multiplexer is sequenced by the sequence bit in the modifier of a Read function. The indicator is turned off 800 microseconds after the relay conversion is complete unless another relay conversion is initiated before the end of the 800 microsecond period. A new relay point can be initiated after the DPC Relay Conversion Complete interrupt has been serviced. The SS Multiplexer can be used in Overlap mode when this indicator is on.

Comparator Indicators

High Out-of-Limit: Turned on and causes an interrupt when the Comparator indicates an ADC reading equal or above limits.

Low Out-of-Limit: Turned on and causes an interrupt when the Comparator indicates an ADC reading below limits.

Indicator Reset

Device Status Word indicators are reset when they are sensed by a Sense Device XIO instruction, if bit 15 of the Sense Device IOCC is a one.

Blast Instruction

Analog Input Operations can be halted by executing a control function. This control function XIO instruction resets all ADC basic controls and registers, the ADC, Multiplexer and Comparator. If an XIO instruction was not completed, it is terminated, releasing the AI subsystem for the next XIO instruction.

ANALOG INPUT EXECUTION TIMES

The following are typical times required for reading a series of analog input points. Note that times are shown for the three core storage cycle times. ADC conversion time is for 14-bit resolution. Eleven or 8-bit resolution is 8 and 15 $\mu{\rm sec}$ per point faster, respectively. The Comparator has no appreciable effect (one core storage cycle) on these times unless an out-of-limit occurs. No time is included for whatever program housekeeping may be necessary.

DIRECT PROGRAM CONTROL OPERATIONS

Multiplexer/R - ADC Model 1

Per Point	2 μsec	$2.25~\mu \text{sec}$	$\frac{4 \ \mu \text{sec}}{}$
XIO Write	.010 ms	.01125 ms	.020 ms
MPLX Relay	9.947	9.94700	9.947
ADC Conversion	on . 043	.043	.043
Interrupt	.110	.12375	.220
XIO Read	.010	.01125	.020
	10.120 ms	10.13625 ms	10.240 ms

Multiplexer/S (HLSE) - ADC Model 1

Per Point	2 μsec	2.25 μsec	$\frac{4 \ \mu \text{sec}}{}$
XIO Write	10 μsec	$11.25~\mu\mathrm{sec}$	$20~\mu{ m sec}$
SS MPLX and Buffer Amp	. 10	10.00	10
ADC Conver-	43	43.00	43
Interrupt	110	123.75	220
XIO Read	10	11.25	20
	183 μsec	$199.25 \mu\mathrm{sec}$	313 μsec

Multiplexer/S (HLSE) - ADC Model 2

Per Point	$\frac{2 \mu \text{sec}}{}$	$2.25~\mu \mathrm{sec}$	$\frac{4 \ \mu \text{sec}}{}$
XIO Write	$10~\mu{ m sec}$	$11.25~\mu\mathrm{sec}$	$20~\mu { m sec}$
SS MPLX and			
S & H Amp.	10	10.00	10
ADC Conver-			
sion	43	43.00	43
Interrupt	110	123.75	220
XIO Read	10	11.25	20
	$\overline{183~\mu\mathrm{sec}}$	$\overline{199.25~\mu\mathrm{sec}}$	313 μsec

DATA CHANNEL OPERATIONS

One DC - MPLX/S - ADC Model 1

Initialize	2 μsec	$\frac{2.25~\mu \mathrm{sec}}{}$	4 μsec
XIO Initialize Read Cycle Steal (C	8 μsec	$9.00~\mu { m sec}$	16 μsec
Word Count	4	4.50	8
CS Initialize MPLX ADDR	. 2	2.25	4
	14 μsec	15.75 μsec	28 μsec
Per Point			
SS MPLX and Buffer Amp.	10.0 μsec	10.00 μsec	$10.0~\mu\mathrm{sec}$
ADC Conversion	43.0	43.00	43.0
Wait	50.0	50.00	50.0
CS Read Data		3.13	5.0
-	$105.5 \mu sec$	$\overline{106.13~\mu\mathrm{sec}}$	108.0 μsec
Chaining			
CS New ADDR	•	$4.50~\mu\mathrm{sec}$	8 μsec
CS CAR Check	x 4	4.50	8
CS Word Count	4	4.50	8
CS MPLX AD	DR		
	4	4.50	8
	16 μsec	18.00 μsec	32 μsec

One DC - MPLX/S - ADC Model 2

Initialize and Chaining times are the same as those for the preceding $\underline{\text{One DC} - \text{MPLX/S} - \text{ADC Model 1}}$ times.

Per Point	$\frac{2~\mu { m sec}}{}$	$\frac{2.25~\mu \text{sec}}{}$	$\frac{4 \mu \text{sec}}{}$
SS MPLX and S & H Amp. ADC Conver-	10.0 μsec	10.00 μsec	10 μsec
sion	43.0	43.00	43
CS Read Data	2.5	3.13	5
	${55.5 \mu \text{sec}}$	$56.13 \mu \text{sec}$	58 μsec

Two DC's - MP	LX/S - ADC	C Model 1	
Initialize	2 μsec	$2.25~\mu\mathrm{sec}$	4 μsec
XIO Initialize			
Read	$8~\mu sec$	$9.00~\mu\mathrm{sec}$	$16~\mu sec$
XIO Initialize		•	•
Write	8	9.00	16
CS Word			
Count	4	4.50	8
CS MPLX			
ADDR		2.25	4
	$22~\mu { m sec}$	$24.75~\mu\mathrm{sec}$	$44~\mu{ m sec}$
Per Point			
SS MPLX and			
Buffer Amp.	10. 0 usec	10, 00 usec	10 usec
ADC Conversion		43.00	43
Wait	50.0	50.00	50
CS Read Data	2.5	3.13	5
	105.5 μsec	106. 13 μsec	108 μsec
Chaining			
CS New ADDR	$2~\mu { m sec}$	$2.25~\mu\mathrm{sec}$	$4~\mu { m sec}$
CS CAR Check	4	4.50	8
CS New ADDR	4	4.50	8
CS CAR Check	4	4.50	8
CS Word Count	4	4.50	8
CS MPLX ADDR	4	4.50	_8
	$22~\mu { m sec}$	$24.75~\mu\mathrm{sec}$	$44~\mu { m sec}$

Two DC's - MPLX/S - ADC Model 2

Initialize and Chaining times are the same as those for the preceding Two DC's - MPLX/S - ADC Model 1 times.

Per Point	2 μsec	$2.25~\mu { m sec}$	4 μsec
SS MPLX/S & S & H Amp. ADC Conversion CS Read Data	10.0 μsec 43.0 2.5	10.00 μsec 43.00 3.13	10 μsec 43 5
	$55.5~\mu\mathrm{sec}$	56.13 $\mu \mathrm{sec}$	$58~\mu sec$

THERMOCOUPLE OPERATION

A thermocouple is a device used for measuring temperatures. A thermocouple produces a voltage which is almost directly proportional to the difference in temperature between the measuring junction (hot junction) and the reference junction (cold junction).

Several thermocouple types, employing different combinations of metal, are available. With an appropriate choice of thermocouple, temperatures as high as 9000 degrees Fahrenheit or as low as minus 450 degrees Fahrenheit can be measured.

Measuring Thermocouple Signals

The conversion of a thermocouple signal to a meaningful and accurate temperature value is performed as a part of the 1800 program. The following factors are used by the 1800 program to accomplish thermocouple signal conversion.

- Thermocouple calibration data.
- Resistance bulb thermometer (RBT) bridge output.
- RBT reference voltage output.
- RBT operating characteristics.
- Thermocouple signal.

Because of the interrelationship of these factors, care must be taken in correlating the measured signal to the actual temperature it represents.

Each process thermocouple is connected to the 1800 via an 1851 Model 2 Multiplexer Terminal. The thermocouple measuring (hot) junction is located in the process area (tank, furnace, etc.) where temperature sensing is desired, and the thermocouple reference (cold) junction is located in the 1851 Model 2 Multiplexer Terminal. Likewise, the resistance bulb thermometer (RBT) and the reference voltage are located in the 1851 Model 2. Thus, the 1851 Model 2 provides thermal stability to the reference junctions, a means of determining the temperature of the reference junction, and terminations for thermocouple signals. The reference junction terminations are extended to signal conditioning elements in the 1851. From this point, the multiplexer selectively connects these signals to the ADC to be converted to a digital value (See Thermocouple Conversion Example).

Thermocouple Calibration Data

Figure 66 illustrates the operating curve of an iron-constantan (type J) thermocouple. A manufacturer's thermocouple calibration graph normally shows only one curve at a stated reference (cold junction) temperature. However, Figure 66 includes two curves to show the relative influence of the cold junction temperature. For complete and more accurate data about a specific thermocouple, refer to the calibration data available from the thermocouple manufacturer, or refer to calibration data available from a testing laboratory.

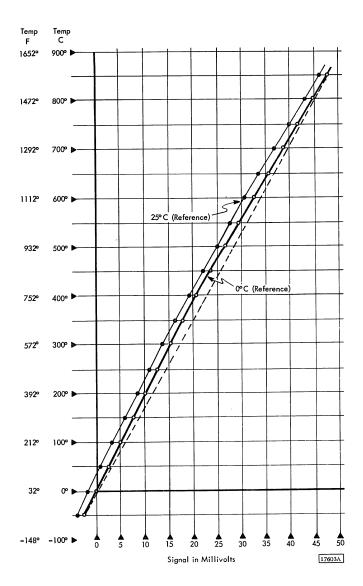


Figure 66. Iron-Constantan Thermocouple Chart

Resistance Bulb Thermometer

The RBT supplied with the 1851 model 2 provides a means of determining the reference junction temperature within the 1851 model 2.

Essentially, an RBT is a wire-wound resistor whose electrical resistance varies with temperature. The RBT resistor is electrically connected to a precision reference voltage and a Wheatstone bridge (balanced circuit). A temperature variation causes a change in resistance and a consequent imbalance of the bridge circuit. The RBT circuits provide two signals for 1800 program evaluation; the voltage produced by the imbalance of the bridge circuit (RBT)

bridge output) and the reference voltage. Thus, thermocouple signals are compensated for reference junction temperature changes, and the reference voltage value itself is read by the computer to permit temperature compensation for the RBT supply voltage variations that occur because of these temperature changes.

The RBT circiut outputs are made available at the first and second address terminals within the 1851 model 2. See Figure 87 for the Mpx/R address that will select points 00 and 01 (within the 1851 model 2 being used). When point 01 (within an 1851 model 2) is selected by the multiplexer, the RBT bridge output is converted by the ADC to a digital value. When point 00 (within an 1851 model 2) is selected, the reference voltage is converted by the ADC to a digital value.

RBT Operating Characteristics

The RBT circuit supplied with the 1851 model 2 has the following characteristics.

Range		Reference Output		RBT Bridge Output		
	65°C	25°C	5°C	65°C	25°C	5°C
Maximum Minimum						
Maximum Minimum		9.10 mv 7.33 mv	9.01 mv 7.21 mv	20.00 mv 16.05 mv	6.63 mv 4.90 mv	0.24 mv -0.19 mv
Maximum Minimum	24.03 mv 18.94 mv	23.16 mv 18.71 mv	23.02 mv 18.79 mv	50.01 mv 39.58 mv	16.87 mv 12.52 mv	0.61 mv -0.50 mv
	Maximum Minimum Maximum Minimum	65°C Maximum 4.90 mv Minimum 3.78 mv Maximum 9.58 mv Minimum 7.47 mv Maximum 24.03 mv	65°C 25°C	Maximum 4.90 mv 3.78 mv 3.70 mv 3.64 mv	Maximum 4.90 mv 4.63 mv 3.78 mv 3.70 mv 3.64 mv 7.91 mv	Maximum Minimum 4.90 mv Minimum 4.63 mv 3.70 mv 4.58 mv 7.91 mv 10.00 mv 7.91 mv 3.37 mv 2.48 mv Maximum Minimum 9.58 mv 7.47 mv 7.33 mv 7.21 mv 16.05 mv 4.63 mv 7.91 mv 4.63 mv Maximum Minimum 7.47 mv 7.33 mv 7.21 mv 16.05 mv 4.90 mv Maximum 24.03 mv 23.16 mv 23.02 mv 50.01 mv 16.57 mv

The preceding millivolt values are converted to a digital value by the ADC, and they are converted to the corresponding temperature by one of the following formulas.

$$T_{rbt}$$
 (°F) = 51 .876 $\frac{V_{rbt}}{V_r}$ + 41 .0

$$T_{rbt} (^{\circ}C) = 28.82 \frac{V_{rbt}}{V_r} + 5.0$$

Where:

 $T_{rbt} = RBT$ Temperature

V_{rbt} = ADC reading ("Q" value) for the RBT bridge output

 $V_r = ADC$ reading ("Q" value) for the reference output

The values 51.876 and 41.0 (Fahrenheit) and 28.82 and 5.0 (Centigrade) are constants for the RBT supplied with the thermocouple block. T_{rbt} can be computed in degrees Centigrade and converted to degrees Fahrenheit with the following formula.

$$T_{rbt}$$
 (°F) = $\frac{9}{5}$ (T_{rbt} in °C) +32

Thermocouple signals of up to \pm 50 mv can be terminated in the first MPX/R group of an 1851 model 2. However, when the multiplexer, under control of the 1800 program, connects a thermocouple signal to the ADC, the millivolt signal is converted to a digital value between 00000 and \pm 16383. The 1800 program must compute a temperature that corresponds to the ADC value.

Thermocouple Conversion Accuracy

Accuracy of thermocouple signal conversion depends on many factors. Some of these factors are described:

1. Accuracy of measurement of the reference (cold) junction temperature.

The resistance bulb thermometer (RBT) circuit supplied with an 1851 model 2 provides two outputs (RBT reference and RBT bridge output). These two outputs, when converted by the ADC to a digital value and used in the proper formula (see RBT Operating Characteristics), indicate the temperature of the reference (cold) junction within plus or minus two degrees Fahrenheit.

- 2. Accuracy of thermocouples may vary from plus or minus one and one half degrees Fahrenheit to plus or minus ten degrees Fahrenheit, depending on the type of thermocouple used. For more specific information, refer to the manufacturer's specifications for the thermocouple being used.
- 3. Thermocouple measurement accuracy is largely dependent on the proper installation of the thermocouple.
- 4. Heat distribution within the medium being measured is another factor that affects the accuracy of the temperature measurement.

Thermocouple Conversion Example

The remainder of this section shows an example of thermocouple conversion. Three points should be stressed about the conversion procedure which follows:

- 1. It is recognized that there are other means, such as curve fitting, to convert thermocouple signals.
- 2. The following example is valid only when the RBT supplied with the 1851 model 2 is used.

3. Each thermocouple type must be separately correlated, i.e., their curves and operating ranges are different.

The following assumptions are made for the thermocouple conversion example.

- The thermocouple signal range is plus or minus 50 mv (amplifier gain of 100).
- The thermocouple is installed (hot junction) in a process area with a temperature region of 800 degrees Centigrade.
- RBT temperature is 24.6 degrees Centigrade (room temperature).
- Thermocouple calibration data is based on a zero degree Centigrade reference curve (Zero degree curve in Figure 66).
- ADC value when reading the thermocouple signal is 15132.
- ADC value when reading RBT bridge output is 5182.
- ADC value when reading reference output is 7620.
- All numeric values in the example use a base of 10.
- The sample problem is presented immediately after each formula.

Converting Thermocouple Characteristics

For a computer conversion procedure, the thermocouple operating curve is considered as being formed of a series of short straight line segments. This segmentation is necessary because the millivolt output is not completely linear in relation to measured temperatures. This non-linear relationship is most pronounced at the upper end of the thermocouple temperature range. Smaller segments provide a closer approximation within each segment.

Study the manufacturer's calibration data (curve or table) to determine the number of segments or divisions that must be made to obtain the desired degree of accuracy. For example, the iron-constantan (type J) thermocouple curve shown in Figure 66 covers a temperature range of minus 50 degrees Centigrade to plus 850 degrees Centigrade. This range may be divided into nine segments as follows:

In order to correlate this operational curve to an actual temperature by a computer program, several intermediate values must be determined. Determination of these intermediate values (steps 1 through 5 of the following procedure) must be done once for each thermocouple type in the system.

1. The size of signal (in millivolts) required to produce an ADC digital value of one bit.

$$K_{adc} = 0.3051758 \,\text{mv}$$

Where:

Kadc = Value of one ADC register bit

29166

29167

2. Determine the ADC reading (Q value) that will be developed in the ADC register for each point used in the segmentation of the manufacturer's calibration curve. (See the zero-degree reference curve in Figure 66.)

$$Q = \frac{V_t \times G}{K_{adc}}$$

Where:

Q = ADC digital value

V_t = Voltage in the thermocouple circuit (each point used is calculated separately)

G = Gain of the differential amplifier

Kadc = Determined previously

For example:

Q (-50° C) =
$$\frac{-2.42 \times 100}{0.3051758}$$
 = -793
Q (+50° C) = $\frac{2.58 \times 100}{0.3051758}$ = 845

Q (+750°C) =
$$\frac{42.32 \times 100}{0.3051758}$$
 = 13,867

Q (+850°C) =
$$\frac{48.73 \times 100}{0.3051758}$$
 = 15,968

3. Determine the slope (A) of each segment of the calibration curve.

$$A = \frac{\triangle \text{ degrees}}{\triangle Q}$$

Where:

Both Δ degrees and $\Delta\,Q$ are the difference in the extremes of each segment.

"Q" values were obtained in a previous step
"A" has a dimension of "degrees per digit"

For example:

A (-50° C to +50° C Segment) =
$$\frac{100}{1638}$$
 = 0.0610
A (+750° C to +850° C Segment) = $\frac{100}{2101}$ = 0.0476

29168

4. Determine the temperature axis (Y-axis) intercept point (B) for each segment. This is the point where a line extended from the segment at the same slope would cross the Y-axis.

$$T = A \times Q + B$$
or
$$B = T - A \times Q$$

Where:

"A" and "Q" values were obtained previously "B" has a dimension of "degrees"

"T" is temperature in degrees corresponding to the same end point of the segment as the lower of the Q values

For example:

B (-50° C to +50° C Segment) = -50 -(0.0610
$$\times$$
 -793) = -50 -(-48.37) = -1.63
B (+750° C to +850° C Segment) = 750 -(0.0476 \times 13,867) = 750 -(660) = 90

5. Determine constants "C" and "D" for the segment that includes 25 degrees centigrade (the segment that includes the approximate RBT temperature).

$$C = \frac{1}{A}$$

$$D = -\frac{B}{A}$$

Where:

Constants "C" and "D" define this segment (-50° C to $+50^{\circ}$ C) relative to the signal axis (x - axis)

"C" has a dimension of "digits per degree"
"D" has a dimension of "digits"

For example:

$$C = \frac{1}{0.0610} = 16.4$$

$$D = -\frac{-1.63}{0.0610} = 26.7$$
29170

The "A", "B", "C", "D", and "Q" values can now be stored in the 1800 core storage to be used by the program when the thermocouple signal is read. The preceding steps provide a "program image" of the thermocouple curve. Each thermocouple type used in a system must be similarly defined and correlated.

Determining Cold Junction Temperature

The cold-junction temperature must be determined as often as indicated by (1) 1851 model 2 ambient air temperature changes and (2) the accuracy of the measurement desired. The following steps (6-8) are required to determine the RBT temperature and adjust it for the effects of the calibration curve at the RBT temperature.

- 6. The 1800 program must read the RBT bridge output and the reference output as described in the section for resistance bulb thermometer.
- 7. Using the ADC readings for the RBT bridge output and reference voltage, compute the temperature indicated by the RBT. (See RBT Operating Characteristics.)

$$T_{rbt}$$
 (°C) = 28.82 $\frac{V_{rbt}}{V_r}$ +5.0

Where:

 T_{rbt} = RBT temperature V_{rbt} = ADC reading for RBT bridge output V_r = ADC reading for reference voltage 28.82 and 5.0 are constants

For example:

$$T_{\text{rbt}}$$
 (°C) = 28.82 $(\frac{5182}{7620})$ + 5.0
= 28.82 (0.68) +5.0
= 24.6° C

8. Adjust the RBT temperature for the effects of the calibration curve slope at the RBT temperature

$$R_{rbt} = C (T_{rbt}) + D$$

Where:

R_{rbt} = Adjusted "Q" value of T_{rbt}
"C" and "D" were obtained previously
T_{rbt} was obtained previously

For example:

$$R_{rbt}$$
 = 16.4 (24.6) +26.7
= 403.4 +26.7
= 430

Determining Thermocouple Temperature

The following steps are performed for each thermocouple signal selected by the multiplexer.

9. The multiplexer, under control of the 1800 program connects the thermocouple signal to the ADC for conversion to a digital value (Q value). To adjust the Q value for the effects of the coldjunction temperature, use the following formula.

$$R_{tc} = V_{tc} + R_{rbt}$$

Where:

R_{tc} = Adjusted "Q" value for the thermocouple signal
V_{tc} = ADC reading ("Q" value) for the thermocouple signal
R_{rbt} was obtained previously

For example:

10. The previous step establishes the correct segment of the calibration curve to be used in the determination of thermocouple temperature. The 1800 program must use the adjusted "Q" value for the thermocouple signal to determine

which of the "A" and "B" values (previously stored in core storage) are to be used in the final step to determine actual thermocouple measuring junction temperature. Use the following formula to complete the computation of thermocouple temperature.

$$T_{tc} = A (R_{tc}) + B$$

Where:

 T_{tc} = Thermocouple measuring (hot) junction temperature "A" and "B" = The values corresponding to the segment (750° to 850°) that includes the "Q" value from the previous step . R_{tc} was obtained previously

For example:

29174

DIGITAL INPUT

These features enable the Processor-Controller of the 1800 to accept real-time digital information in a digital format. The modular design of the feature permits individual system tailoring as to type and quantity of digital input data, such as:

Contact Sense Voltage Level Sense Contact Interrupt Voltage Level Interrupt Digital Voltmeters Special Analog-to-Digital Converters Turbine Flowmeters Shaft Encoders Electronic Register Vibration Detectors e.g., Telemetry Weighing Devices

Mechanical Counters Electronic Counters Rotary Switches from operator Sense Switches from operator Pulse Tachometers Frequency Meters Watt-Hour Meters

Digital Input is brought into the system in 16-bit groups. The format may be in any form. For example:

Unrelated bits from Contact or Voltage levels Binary numbers Binary-coded-decimal digits Decimal digits Gray code digits

Any mixture of digital formats can be handled. Conversion from one base to another can be easily and quickly implemented by the P-C. Data input is via Direct Program Control or a Data Channel. One instruction is used in Direct Program Control to bring 16 bits of data into core storage. Where a Data Channel is used, one instruction initiates a cycle stealing operation that brings many 16-bit

groups of data into core storage (one group per core storage cycle). The number of groups read sequentially, randomly, or single address - as well as synchronization of the P-C to the input data is handled automatically.

Interrupt conditions from the process are a type of digital input. These Process Interrupts are brought into the P-C in 16-bit groups, with up to four priority levels of interrupt and four interrupt conditions per level for each 16-bit group.

High-speed 8-bit or 16-bit binary electronic pulse counters are available as special features. Counters are read into core storage as digital input groups, 16 bits at a time (two 8-bit counters or one 16-bit counter).

As shown in Figure 67 the combined capacity of the Digital Input and Pulse Counter features is 1024 bits, as follows:

Digital Input

8 adapters x 8 Digital Input groups x 16 bits per group = 1024.

Pulse Counter

8 adapters x 128 Pulse Counter bits per adapter (Pulse counters can be 8-bit or 16-bit counters) = 1024.

Any combination of the above may be used within the capacity of 1024 bits.

The capacity of the Process Interrupt feature is 24 priority levels or 384 bits, as follows:

> 8 adapters x 3 Process Interrupt groups (24 levels) x 16 bits per group = 384

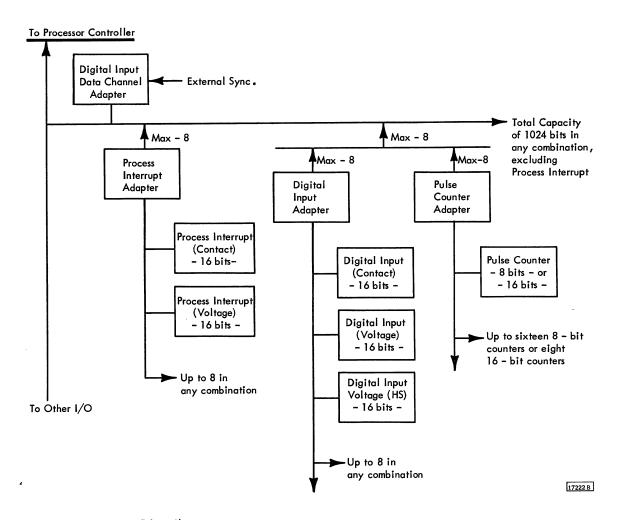


Figure 67. Digital Input Schematic

DIGITAL INPUT UNITS AND FEATURES

The 1826 Data Adapter Unit provides housing expansion of Digital Input and Digital Output points. The following units and features may be added to the system to provide Digital Input functions: For specifications, see 1800 Data Acquisition and Control System Installation Manual—Physical Planning, Form A26-5922.

DIGITAL INPUT DATA CHANNEL ADAPTER

This feature adapts digital input to a P-C Data Channel to enable digital input in the cycle stealing mode of operation.

Operation With External Sync

The Digital Input Data Channel Adapter provides the external sync function. An XIO instruction (Initialize Read-Synchronized) is executed to develop an external sync ready signal. When the external device senses the ready signal, it must transfer data to the addressed digital input group and then send an external sync signal to the Digital Input Data Channel Adapter. The external sync signal initiates a core-storage cycle to read the data into a corestorage word and turns off External Sync Ready.

An 8-bit in the modifier of an IOCC sets up the external sync mode.

The Digital Input feature will be interlocked under external sync until word count equal to zero for last external sync is obtained; however the P-C can execute instructions while the Digital Input feature is interlocked.

Operation Without External Sync

This mode of operation is initiated by execution of an XIO Initialize Read instruction when modifier bit 8 of the IOCC is zero. The speed of the digital input read operation is that of core storage, therefore the input operation will be completed prior to execution of the next instruction in the P-C.

DIGITAL INPUT

Digital input in the form of 16-bit groups can be handled by the Digital Input Adapter. Any logical

grouping of 16 bits can constitute a Digital Input group. For example:

- 16 bits of status information
- 4 4-bit BCD digits
- 1 10-bit coded decimal digit and 6 bits of status
- 1 16-bit binary number

Two types of Digital Input bits can be terminated in groups of 16. One type operates in conjunction with a customer supplied process contact. The second type senses the level of a voltage supplied from the customer's equipment.

Screw-down type terminations are provided to terminate the customer's input wires. Input groups of 16 bits are available up to a total of 64 groups. Data comes in on two wires per bit. An input channel 16 bits wide for special consoles and other low speed devices can be made by selection of devices onto the channel via the Digital Output features.

An XIO command (IOCC) received by the Digital Input feature contains the address (Modifier) of a Digital Input group and selects the group to be read into core storage or the Accumulator. If a process contact is closed or the voltage level is positive, a one-bit is placed in the designated bit position of that word. An open contact or negative level results in a 0 bit being sent. The first sense bit is located in bit position zero, the second sense bit in bit position one. This continues through the 16th bit which is in bit position 15 of the word. The Read function of the XIO instruction brings the addressed group into a core storage word and the Sense function brings the addressed group into the A-register (Accumulator). The Sense function is also used to read the digital input status word into the Accumulator. The status word contains the indicators for Digital Input.

Digital Input Adapter

The Digital Input Adapter is a prerequisite feature for Digital Input (Contact), Digital Input (Voltage) and High-Speed Digital Input. Each Digital Input Adapter provides for 128 bits of digital input. Each system can have a maximum of eight Digital Input Adapters.

Digital Input (Contact)

Digital Input (Contact) is available in groups of 16 two-wire contact input terminations. Read speeds up to 500,000 words per second are possible in burst mode when a Data Channel is used and a two microsecond core storage cycle is present. When an XIO instruction initiates reading a group of contacts, each closed contact reads a one bit into its respective bit position and each open contact reads a zero into its respective bit positive bit position.

Digital Input (Voltage)

Digital Input (Voltage) is available in groups of 16 two-wire voltage input terminations. Read speeds of up to 500,000 words per second are possible in burst mode when a Data Channel is used and a two microsecond core storage cycle is present. When an XIO instruction initiates reading a group of voltage inputs, each positive input reads a one bit into its respective bit position and each negative reads a zero into its respective bit position.

An optional high speed feature provides high repetitive reading speed for Digital registers. For example, telemetry registers may be coupled to the system using one or more modified voltage level groups, depending on register size and the number coding of the register. Conversion of the various number bases is accomplished via programming.

High-speed Telemetry Receiver registers may be read using the program mode of control (DPC) and an external interrupt for synchronization. Registers may be read by using a Data Channel synchronized by an external customer supplied sync signal.

Repetitive reading of the same group can proceed at rates up to 100,000 words per second.

Digital Input Channel

Process Operator Console (POC) input devices, such as decade switches and sense switches, and other low-speed inputs can be brought into the system by the formation of a Digital Input Channel using Electronic Contact Operate to select various groups of 16 bits over a single Digital Input Group. POC input devices and cabling are handled via RPQ.

PULSE COUNTER

Pulse Counter Adapter

The Pulse Counter Adapter is a prerequisite for adaptation of pulse counters. This feature provides for a maximum of sixteen 8-bit or eight 16-bit Pulse Counter features. A maximum of 8 adapters is available for each system.

A maximum of 128 eight bit (or 64 sixteen bit) Pulse Counters per system is available.

Pulse Counter

The Pulse Counter accepts discrete pulses as input information and advances by one per received pulse. The customer pulse is terminated by two-wire screw down termination at the individual counter terminal. These counters are read into the P-C in the same manner as a Digital Input group. Two 8-bit counters (or one 16-bit) are read from one address. (See section for Address Assignment for individual address assignments.) Either 8-bit or 16-bit binary counters are available. The counters are reset when they are read out.

PROCESS INTERRUPT

Process Interrupt Adapter

The Process Interrupt Adapter (see Interrupt section of manual) is a prerequisite for adaption of Process Interrupts (Contact) and Process Interrupts (Voltage). Each Process Interrupt Adapter provides for 48 interrupt points (Maximum - 8 Adapters per system).

<u>Process Interrupt (Contact)</u>: Termination and sensing of 16 customer contacts associated with up to 4 levels of interrupt (Maximum - 24 groups per system).

<u>Process Interrupt (Voltage)</u>: Termination and sensing of 16 customer voltage levels associated with up to 4 levels of interrupt latches (Maximum 24 groups per system).

Process inputs may exist in the form of isolated dry contact closures, [called Process Interrupt (Contact)], whereby IBM provides the sensing voltage for the contact, or if the form of a voltage level, [called Process Interrupt (Voltage)]. An interrupt is initiated by a contact closing, or a voltage level changing from negative to positive (0 bit to 1 bit). See Interrupt section of this manual.

DIGITAL INPUT ADDRESSING

An Address (IOCC Modifier) is assigned to each digital input group (16 points) and to each pulse counter (2 consecutive counters are assigned to each address) when the system is manufactured. Addresses assigned to Digital Input and Pulse Counters are 64-127. See the section for Address Assignment for the individual addresses assigned to digital input and pulse counter groups.

Digital Input

Digital input groups are assigned an address (IOCC Modifier) starting with address 64 for group 0 (16 points of the first Digital Input Adapter (DIA). Address 65 is assigned to group 1. This sequence of assignment continues through address 127 which is assigned to group 7 of the eighth Digital Input Adapter. Since Digital Input and Pulse Counters share the same group of addresses (IOCC Modifier), the total number (8 Adapters) of the two features is defined by the available addressing capacity (64 addresses): If 4 DIAs are ordered, a maximum of 4 Pulse Counter Adapters can be ordered.

Pulse Counter

Pulse Counters are assigned an address (IOCC Modifier) starting with address 127 being assigned to counters 0 and 1 (8-bit counters) or counter 0 (16-bit counter) of the first Pulse Counter Adapter.

Address 126 is assigned to counters 2 and 3 (8-bit counters) or counter 2 (16-bit counter) of the first Pulse Counter Adapter. This sequence of assignment continues through address 64 for counters 14 and 15 (8-bit) or counter 14 (16-bit) of the eighth Pulse Counter Adapter. See the section Digital Input for maximum Pulse Counter Adapters.

Process Interrupt

Digital input from process interrupt occurs via the Process Interrupt Status Word (PISW) as described in the section for Interrupts. An address (IOCC Modifier) is assigned to each PISW when the system is manufactured. When ordering the system, the customer must specify (on the Process Interrupt Status Word Assignment Form) which 16 Process interrupt points (4 groups of 4 each) will be used with each PISW. See section Fixed Assignment for address assignment.

PROGRAMMED OPERATION

Digital input is processed by Direct Program Control (DPC) and/or the Data Channel (DC). When both operations exist, DPC may be used when the DC has completed its scan of the data table. The Digital Input Busy indicator is used to determine the status of the DC. DPC operation requires one XIO instruction for each Digital Input group (16 bits) to be transmitted to the Accumulator or core storage location. If a pulse counter is specified, the counter is reset.

When Digital Input is under DC one XIO function can be used. This function performs the following operation:

INITIALIZE READ

The Digital Input group(s), addressed by address word(s), in the data table(s) is read into core storage. If a Process Interrupt group is addressed, the data read in for that group will be blank.

When Digital Input is under DPC, three XIO functions can be used. These functions perform the following operations:

READ

The Digital Input group (or Process Interrupt Status word) addressed by the Modifier field is read into core storage.

SENSE

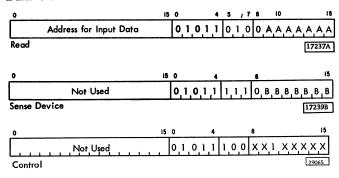
The Digital Input group (or Process Interrupt Status word) or the Device Status Word addressed by the Modifier field is placed in the Accumulator.

BLAST INSTRUCTION

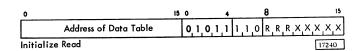
DI operations can be halted by executing a control function. This XIO Control resets all basic controls. If any operation is not completed, that operation is terminated, releasing the DI Subsystem and Data Channel for the next XIO instruction.

I/O CONTROL COMMANDS - DIGITAL INPUT

DIRECT PROGRAM CONTROL



DATA CHANNEL



where:

01011

is the assigned Area code for Digital Input

 \mathbf{X}

is not used.

AA...A

is the address of the Digital Input Group or PISW. These addresses range from 64_{10} through 127_{10} for Digital Input groups and 2_{10} through 25_{10} for Process Interrupt Status words. See the section Address Assignment.

BB...B 0000000 and 0000001 are the addresses of the Digital Input Device Status Word. The indicators are reset by 0000001. Addresses 2₁₀ through 25₁₀ are assigned to the Process Interrupt Status Words.

Addresses 64₁₀ through 127₁₀ are assigned to Digital Input and Pulse Counter groups. See the section Address Assignment.

RRR

These bits have the following meaning:

000 Read Random

001 Read Sequential

010 Read Single Address

100 Read Random and External Sync

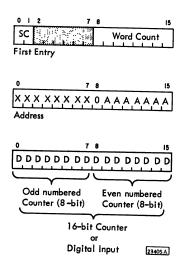
101 Read Sequential with External Sync

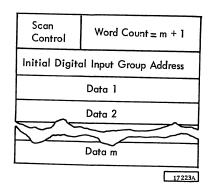
110 Read Single Address with External Sync

Overlap of operations can be done in that Process Interrupts and status indicators (modifier addresses 0_{10} through 25_{10}) may be read or sensed via DPC during a DC operation on Digital Input groups. Note that this overlap can occur only during Data Channel operations with external sync since otherwise the Data Channel operation will be completed before any P-C instructions can be executed. The following points should be considered when programming such an overlap.

- An Initialize Read will terminate the Data Channel operation in progress and set the Command
 Reject indicator.
- A Read (DI-modifier address 64 through 127) will set the Command Reject indicator and will not be executed.
- A Read (PI-modifier address 2 through 25) will set the Command Reject indicator but will be executed correctly.
- A Parity error which causes an internal level interrupt as an XIO is being executed will terminate the Data Channel operation in progress.

Data Table Formats





where:

SC are the Scan Control bits. X

is not used.

AA...Ais the address of the Digital Input group. The first group has an

address of 64_{10} , the 64th group has an address of 127_{10} .

D is data. For pulse counters: odd numbered counters bits 0 through

7 (8-bit counter); even numbered counters bits 8 through 15 (8-bit counter) or bits 0 through 15

(16-bit counter).

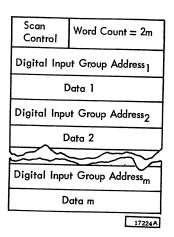
Data Table Layouts

The Address field of the IOCC used with the Data Channel operation specifies the location of the first word of the table. There are several table layouts which are described below. The first word in the table contains the word count and the chaining control.

When operating in the Sequential or Single Address mode, the second word in the table contains the initial Digital Input group to be read into core storage, and the succeeding table locations receive the data read over a Data Channel as shown in the following table.

When READ Single Address is specified, the Initial Digital Input group is read over and over and placed in succeeding words of the table, until the word count reaches zero. When External Sync is specified, the cycle steal is initiated based on the External Sync pulse.

When operating in the Random mode, succeeding alternate words supply digital input addresses and receive data as shown in the following table.



When the word count reaches zero, normal Scan Control applies as described in the I/O Control section of the manual. If chaining is used, a chain address (address of next table) word must follow the table. The first word of the next table must contain its own address to satisfy the CAR check as described in the Section for Data Channel Operation. An interrupt may be generated at the completion of the scan. The interrupt is called Digital Input Scan Complete.

TIMING: Digital Input groups will be read at the maximum rate of the channel unless a higher priority Data Channel request is honored. But timing restrictions due to filtering and customer load should be observed.

Caution

A digital input operation without external sync, locks out the P-C until the operation is complete. Chaining data tables increases the amount of data that can be transferred by a single DI operation; therefore it can increase the amount of time the P-C is locked out.

Device Status Word

An XIO Sense, specifying the Digital Input Area code (01011) and modifier address (00000 or 00001) will cause the Device Status word to be read into the Accumulator. The DSW bits are

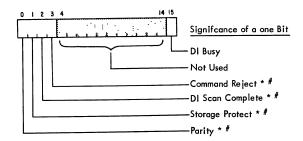
Parity - turned on if even parity is encountered during data transfers to and from core storage or if a P-C parity error is detected during a

chaining operation for any Digital Input instruction (Pulse Counter, Digital Input, Process Interrupt). This error terminates the operation. Storage Protect — turned on if an attempt is made to write into a "read only" location. This error terminates the operation.

DI Scan Complete – turned on and causes an interrupt when the word count goes to zero in a DC operation and the Scan Control bits specify an interrupt.

DI Busy - Turned on when DI is in use on a DC as the result of an XIO Initialize Read instruction. Turned off when the DC is not busy. An XIO (Read or Initialize Read) executed when this indication (DI Busy) is on causes a command reject interrupt. If the XIO Read addressed a PI group, that group was read even though the command reject indicator was on.

Digital Input (DI) Device Status Word Format:



* Interrupt

Indicator reset by a Sense DSW when IOCC bit 15 = 1. Other indicators are reset by their status turnoff.

23406

The Digital and Analog Output (DAO) feature provides versatile control capability for the 1800 System. DAO features enable computer control over the many types of auxiliary devices required in a data acquisition or control system. Equipment that can be controlled includes set point positioners, displays, trend recorders, motor operated valves, and telemetry systems. The control outputs available with the DAO include the following:

- 1. Pulse Output (PO)
- 2. Electronic "Contact" Operate (ECO)
- 3. High-Speed Digital Register Output (RO)
- 4. High-Speed Analog Voltage Output (AO)

Pulse chaining and pulse-duration outputs are accomplished by programming.

The DAO features can communicate with the 1800 system via Direct Program Control (DPC) or a Data Channel (DC). A customer "external sync" pulse can be used to initiate DC operation.

Organization

The DAO features are organized as shown in Figure 68 and as described below:

- 1. The 1800 Processor-Controller (P-C) provides the basic control for the DAO features.
- The DAO Data Channel Adapter enables communication between the P-C and DAO devices via a Data Channel (maximum of one Data Channel Adapter per system).
- 3. The Digital Output Control and the Analog Output Control provide the interface between the P-C and the output registers. A maximum of eight Controls, in any combination, can be attached:
 - a. Each Digital Output Control can accommodate 16 output registers. Note in Figure 68 that a Digital Output Adapter is required for each 4 output registers. (The Digital Output features may be installed in either the P-C or the 1826 Data Adapter Unit.)
 - b. Each Analog Output Control can accommodate 8 Digital-to-Analog Converters. (The Analog Output features are connected to the Processor-Controller through 1856 Analog Output Terminals.)

External Sync (Electronic)

This function is provided by the DAO Data Channel Adapter feature. An XIO instruction (initialize write-synchronized) is executed to load the addressed group with the data word. When the data word has been loaded, the External Sync Ready signal is turned on, signaling the external device that data is available.

The external device reads the data and then sends an External Sync signal to the DAO adapter, resetting the External Sync Ready signal and signaling that the external device is ready for another data word. This initiates a cycle steal request. At the completion of the cycle steal operation, the ready signal is turned "on" again.

When the last data word of a data table has been loaded (determined by the Word Count register in the DAO Adapter), an end of table interrupt is received with the DAO busy indicator remaining on.

The DAO busy indicator is on during the last data word until the last External Sync signals the adapter that the last word has been read.

An "8-bit" in the modifier of an IOCC sets up the external sync mode. The absence of an "8-bit" in the modifier terminates the external sync mode.

For specifications, see IBM 1800 Data Acquisition and Control System Installation Manual-Physical Planning.

System Capacity

The system capacity of DAO points depends on the combination of Digital Output (DO) and Analog Output (AO) points installed. Selection begins with the DO and AO Controls, maximum of eight:

- If the maximum number of DO points are desired, seven DO Controls are installed. Each DO Control interfaces a maximum of four DO Adapters (2 adapters in 1801), providing a maximum of 26 DO Adapters. Each DO Adapter accommodates a maximum of four 16-bit registers, which is 104 registers, or 1664 bits. Installation of the DO maximum eliminates the possibility of AO points.
- 2. If the maximum number of AO points is desired, eight AO Controls are installed. Each AO Control interfaces eight Digital-to-Analog

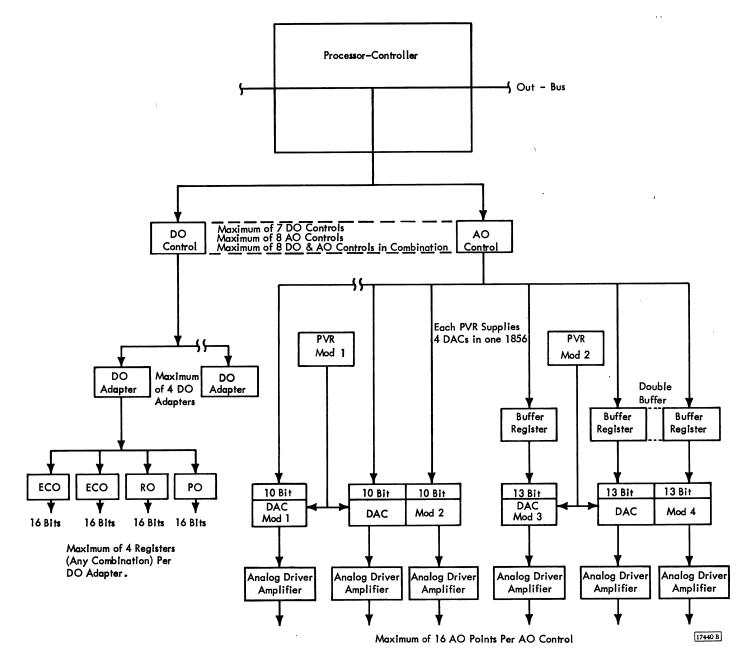


Figure 68. Schematic of Digital and Analog Output Features

Converters (DAC's), with a maximum of 16 AO points. Each DAC provides one or two AO points, depending on the DAC mod. Thus, a maximum number of 128 AO points can be installed. Installation of the maximum number of AO points eliminates the possibility of DO points.

Note that one AO point equals one 16-bit digital output register and that a total system limit of 128 (AO points plus DO registers) exists.

Installation of single point DACs reduces the maximum of 128. Each DAC Mod 1 and each DAC Mod 3 provides only one AO point, reducing the 128 maximum by one for each mod 1 and 3 installed.

DIGITAL OUTPUT

Three types of digital output are available: Electronic "Contact" Operate, Pulse Output, and Register Output. For specifications see IBM 1800 Data Acquisition and Control System Installation Manual-Physical Planning.

Electronic "Contact" Operate

ECO is used to operate alarms, console indicator lights and displays; and operating process equipment such as relays, solenoid valves, and DC motors. ECOs are provided in groups of 16 points (maximum 104 groups). The 16 points are set by a data transfer to the 16-bit register and remain latched until changed by another data transfer to the 16 bit register. A data bit of 1 corresponds to closed (conducting) and a data bit of 0 corresponds to open (nonconducting).

Process Operator Console (POC) output devices such as lights, digital displays, and other low speed outputs can be operated by the formation of a "Digital Output Channel" using Electronic "Contact" Operate to select various groups of 16 bits over a single group of Electronic "Contact" Operate. POC Output devices and cabling are handled via RPQ.*

Pulse Output

The primary use of this output is to provide for pulse trains to operate such devices as latches, set point positioners, and other stepping motor devices. Pulse Outputs are provided in groups of 16 points (maximum 104 groups) and these are driven from each 16-bit register. The 16 points are set by a data transfer to the 16-bit registers. A data bit of 1 corresponds to closed (conducting) and data of "0" corresponds to open (nonconducting).

The outputs (with a data bit of 1) are "closed" immediately when the registers are loaded, and all are "opened" by the timing out of a 3-ms timer. The timer is started by using a separate XIO Control Function. In this manner pulse chains are accomplished by programming.

Specifications for Pulse Output are similar to ECO except for the duration of switch closure. The effective duration of switch closure can be increased or decreased by loading a 16-bit register before (increase duration) or after (decrease duration) the 3-ms timer is started. All pulse output points are "opened" simultaneously.

Register Output

Digital data is transferred from core storage to the Register Output feature. The Register Output feature has a maximum of 104 sixteen bit groups. The content of each output register is then transmitted to customer-owned devices, such as telemeter registers, for a register to register transfer.

The output of this register remains latched until changed by another data transfer. $\,$

ANALOG OUTPUT

There are two basic types of analog voltage outputs. The first type, DAC Mods 1 and 2 (10 bit), is a fast response unipolar DAC utilizing digital storage of a single level. The second type, DAC Mods 3 and 4 (13 bit), is a bipolar high speed, high accuracy DAC utilizing digital storage with a standard single level of buffering, and an option of double register buffering. Both types have the option of an Analog Output Driver Amplifier to provide low output impedance to match a wider variety of loads than the standard feature.

For both the 10-bit and 13-bit types, the Output Channel Register is force loaded to minimize DAC switching transients. This force loading means that the register goes directly from the previous value to the new value without being reset to zero in between.

DIGITAL-TO-ANALOG CONVERSION

There are four DAC Mods:

- Mod 1 Provides 10-bit digital-to-analog conversion for one analog output point.
- 2. Mod 2 Provides two 10-bit converters for two analog output points.
- 3. Mod 3 Provides 13-bit + sign conversion for one analog output point.
- 4. Mod 4 Provides two 13-bit + sign converters for two analog output points.

A Precision Voltage Reference, Mod 1 or 2, is required to supply the DAC reference voltage.

^{*}Request Price Quotation from IBM

DAC Mods 1 and 2

Installed in 1856 Terminals, DAC Mods 1 and 2 provide unipolar analog output from 10-bit resolution, suitable for operating analog controllers, strip chart recorders, and other displays. Mod 1 provides one analog output point for a maximum of 64 points. Mod 2 provides two separate Digital to Analog Converters in one housing with separate output points for each converter (maximum 128 output points).

DAC Mods 3 and 4

Installed in 1856 Terminals, DAC Mods 3 and 4 provide bipolar analog output from a resolution of 13 bits plus sign, suitable for hybrid systems. Negative numbers are handled in two's complement form. Mod 3 provides one output point, for a maximum of 64 points. Mod 4 provides two separate Digital to Analog Converters in one housing, with separate output points for each converter (maximum 128 output points). It is frequently a requirement in hybrid computing and often an advantage in other applications to operate with several new values simultaneously. The Buffer Registers (one per analog output point) are loaded as the data is received from the P-C. An XIO Control instruction with a 9 bit is then executed to transfer the contents of all buffer registers to their respective analog output registers simultaneously.

Precision Voltage Reference (PVR)

The PVR feature is required to provide the precision voltage reference to the DAC. It is installed in the 1856 Analog Output Terminal.

Each Precision Voltage Reference supplies eight analog output channels in the 1856. The PVR Mod 2 may be used with eight 10- or 13-bit resolution analog outputs when it is desired to mix the two kinds of outputs in a single terminal. It is more economical, however, to use the 10-bit resolution PVR Mod 1 for each full group of eight 10-bit output points.

Analog Output Driver Amplifier

The AO Driver Amplifiers provide a ±10 volt analog output and permit operation of AO points with a wide range of load impedances. The output impedance of the DAC's is 10K ohms. To match loads differing greatly from this value, an output driver amplifier having an output impedance of less than 0.6 ohm may be used. This driver amplifier is applied on a per point basis to provide load impedance matching and voltage amplification. The driver amplifier is also used to increase the DAC analog output voltage from its normal 5 volts to 10 volts.

1856 Analog Output Terminals

There are two models of the 1856:

Model 1 provides power and housing for four DAC's. It provides as many as eight AO points if only DAC Mods 2 and 4 are installed; and as few as four AO points if only DAC Mods 1 and 3 are installed.

The 1856 Model 1 provides control circuitry for eight DAC's, any mod. Thus, an 1856 Model 1 is required for each multiple of eight DAC's.

The 1856 Model 2 provides power and housing for four DAC's, any mod. One 1856 Model 2 can be installed for each 1856 Model 1 when the additional AO points are required. An 1856 Model 2 cannot be installed without an 1856 Model 1.

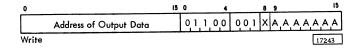
A maximum of sixteen 1856s can be installed in an 1800 system.

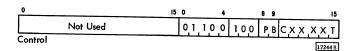
DAO PROGRAMMED OPERATION

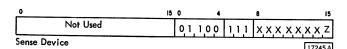
Digital and Analog Output (DAO) data are handled either by Direct Program Control (DPC) or Data Channel (DC) control. For DPC operation one Output Register is selected, and the digital data is transferred from core storage to the register of the output device using an XIO Write instruction. For DC operation a series of points are selected and data is transferred on a cycle steal basis using one XIO Initialize Write instruction to initiate the operation.

I/O CONTROL COMMANDS - DIGITAL AND ANALOG OUTPUT

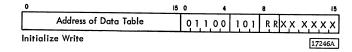
DIRECT PROGRAM CONTROL







DATA CHANNEL

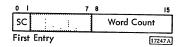


where:

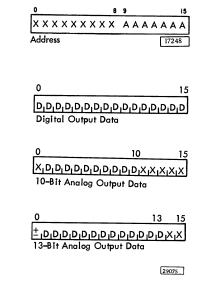
01100

01100	is the assigned Area code for
	Digital and Analog Output.
X	is not used.
AAA	is the address of the digital or
	analog output register. (See
	Address Assignment section).
P	a one bit means initiate reset
	timer for all Pulse Output
	points.
В	a one bit means initiate
	simultaneous transfer from
	Buffer Registers to all analog
	output points operating with
	the Buffer Register feature.
RR	these bits have the following
	meaning:
	00 - Write Random
	01 – Write Single Address
	10 - Write Random with
	External Sync
	11 - Write Single Address
	with External Sync
\mathbf{C}	A one bit means reset all basic
	DAO controls, terminating
	any DAO operation in progress
	and releasing the Data Channel.
${f Z}$	A one bit means reset interrupt
	indicators.
T	Test latch for Customer Engineer
	(diagnostic)

DATA TABLE FORMATS



where SC are the Scan Control bits.



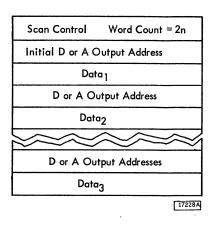
where X is not used, D is Data, and AA...A is the address of the digital or analog output register.

DATA TABLE LAYOUTS

The Address field of the IOCC used with Data Channel operation specifies the location of the first word of the table. There are several table layouts which are described below.

Write Random

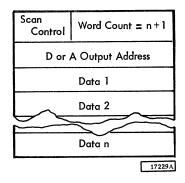
When Write Random is specified, the first word in the table contains the word count (equal to two times the number of data words to be written) and the Scanning Control. The second word in the table contains the starting Digital or Analog Output address of the sequence of addresses to be scanned. The succeeding table locations contain the data to be converted and the DAO address, alternately, as shown in the following table:



The total number of data and addresses transferred is specified by the word count. Data and Output Addresses are interleaved in the Table.

Write Single Address

When Write Single Address is specified, the word count equals the number of data words to be written plus one. The Output point is written over and over with succeeding words of data from the table until the word count reaches zero as shown in the following table:



When external sync is specified, the cycle steal is initiated based on the external sync pulse.

When the word count reaches zero, the normal Scan Control chaining applies as described in the I/O Control section of this manual. An interrupt can be generated at the completion of the scan, depending on the scan control bits. The interrupt is called DAO Complete.

TIMING: Digital Output words can be written up to the maximum rate of the channel. The actual output data rate to customer devices is limited by the device characteristics and the repetition rate to the same outputs or to single outputs.

The rate can be controlled either by external synchronization or by programming, as specified by the output feature.

NOTE: Chaining can lock out the P-C.

Device Status Word

An XIO Sense, specifying the Area code of the DAO, will cause the Device Status word to be read into the Accumulator. The DSW indicators are:

Parity - Indicator is on if even parity is encountered during data transfers to and from core storage or if a P-C parity error is detected during a chaining operation. Causes an interrupt and terminates the DAO operation.

Pulse Output Timer - indicator is on whenever the pulse output timer is on.

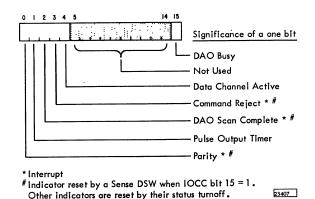
DAO Scan Complete - turned on and causes an interrupt when the word count goes to zero in a Data Channel operation and the scan control bits specify an interrupt; turned off by XIO Sense Device instruction.

Command Reject - turned on if any XIO Write or Initialize Write instruction is issued while the DAO Busy indicator is on.

Data Channel Active - Indicator is active only with external sync operation. Turned on when DAO is in use on a Data Channel. Turned off (Data Channel is released) when the last word of the last data table has been transferred (prior to receipt of external sync).

DAO Busy - Turned on when DAO is in use on a Data Channel. Turned off when the last word of the last data table has been transferred and receipt of data is acknowledged if external sync is used.

Note: DAO Busy and Data channel active indicators turn off at same time unless external sync mode is specified.



Blast Instruction

Digital and Analog output operations can be halted by executing a Control Function, XIO instruction. This instruction resets all basic controls (DO and AO output registers are not reset). If any Digital or Analog output external sync operation is not complete, that operation is terminated and the Digital-Analog subsystem, including the Data Channel, is released. Another XIO instruction can then reinitialize the Digital or Analog output operation.

GENERAL DESCRIPTION

The Communications Adapter (CA) is designed to extend the capabilities of the 1800 System by making possible communication with other systems, which have appropriate communication attachments. The functional characteristic of the CA feature is a subset of the Binary Synchronous Communication System (BSCS) and complies with the conventions established for binary synchronous communications. This makes the CA compatible with the following:

- System/360 with Synchronous Data Adapter II of the 2701 Data Adapter Unit.
- System/360 with 2703 Transmission Control Unit.
- 1130 System with Synchronous Communications Adapter.
- Other 1800 Systems with the CA feature.
- 2780 Data Transmission Terminal and other BSC devices.

For the user not familiar with data communications, the following manuals are referenced:

IBM Data Communications Primer, Form C20-1668

IBM Binary Synchronous Communications, Form A27-3004

The CA provides half-duplex, synchronous (by bit and by character) data transmission. The CA may also operate in full-duplex, thus reducing line turn-around delays, but message transmission is half-duplex only (transmission in one direction at a time). In dial-up network operation, the CA will automatically answer calls originated by a remote station (Auto Answer function).

Selectable Features

Number of Lines: Up to four (4) CA basic units may be attached to an 1800 System. Either one or two communication lines (line adapters) can be attached to the CA basic unit, thus giving a maximum of eight

(8) communication lines, all of which may be operated simultaneously.

Transmission Code: Either United States of America Standard Code for Information Interchange (USASCII) normal or Extended Binary-Coded-Decimal Interchange Code (EBCDIC) normal and transparent may be selected as the transmission code. Both lines of the CA must select the same code.

Clocking: Either business machine or data set clocking may be specified. Choice of clocking is dependent on the data set. However, the clocking (business machine or data set) must be identical in all stations on a communications link.

In addition the following options are available to the user:

<u>Line Speed</u>: Either line may select a speed of 600 (World Trade Corp. only), 1200, 2000, 2400 or 4800 (domestic only) baud. Choice of speed is dependent on the data set and quality of lines used.

<u>Transmission Mode:</u> Either line may select transmit controlled carrier or continuous carrier operation. Continuous carrier operation is permitted on 4-wire communication links only.

Primary or Secondary Station: Either station may select either option. The receive timeout for the primary station occurs at 2.7 seconds while the timeout at the secondary occurs at 3 seconds. This option assists in breaking hardware contention, which could occur when two stations attempt to transmit simultaneously.

Number of Pre-SYN Pads (Hex 55): Either 1 or 3

Pre-SYN pads may be selected for either line. Three pads are required when business machine clocking is used.

<u>Interrupt Options:</u> Both lines, if installed, are on the same selectable interrupt level. ILSW bits for each line are also selectable.

Cycle Steal (CS): Each line may be on a separate selectable data channel, which provides a separate cycle-steal control for each line.

CA Ready: This option may be installed in either line to prevent disconnecting a dial-up data set when the line is de-initialized. This is an aid to program debug and may be left in if program disconnect is not required.

Area Code

Each installed CA (maximum of 4) is assigned a different area code. The area code assigned relates to both lines of each CA if both are installed. The area code for the first CA is 21 (10110). Additional CA's are assigned as follows:

CA	Code
2	22 (10110)
3	23 (10111)
4	20 (10100)

COMMUNICATION FACILITIES

The common carrier may be either private or leased voice-grade lines, or switched telephone networks. Either two-wire or four-wire connections may be used. The network may consist of point-to-point and multipoint links.

The CA-to-data set interface conforms to the Electronic Industries Association (EIA) RS-232B Standard.

Auto-Answer Function

This function, providing the controls necessary to give "off-hook" and "hang-up" indications, allows the CA to automatically answer incoming calls on switched networks.

Outgoing calls are initiated manually. No provision for automatic calling is available.

CA CODE

The CA uses either EBCDIC or USASCII as the transmission line code. All characters (Figures 69 and

70) are transmitted low order bit first. The first bit on the transmission line is bus out bit 7 or 15 of the 1800 system. The following chart illustrates the bit positions.

Bit Significance	Hi							Low
1800 Bit Position	0	1	2	3	4	5	6	7
1800 Bit Position	8	9	10	11	12	13	14	15
EBCDIC Bit Position	0	1	2	3	4	5	6	7
USASCII Bit P∞ition	P 0	7 b ₇	6 6	5 b ₅	4 6 ₄	3 b ₃	2 b ₂	1
			Fir	st Bit	to L	ine_		

11730

Control Characters and Sequences

Ten communications control characters provide the control character set to implement the control functions. In addition, the code extension sequences are defined for representing additional control functions not included in the defined usage of the single-character control signals. Certain control functions which are optional extensions of the control procedures are defined and represented by this means of code extension.

The communication control characters and sequences defined for the BSC system are listed in Figure 71.

SYN — Synchronous Idle

Used by the CA to establish and maintain synchronism in the absence of any other character.

SOH - Start of Heading

Precedes a block of heading data. A heading consists of auxiliary information necessary to process the text portion of the message.

			1800 Core Storage Byte Positions 0, 1, 2, 3														
Byte Posi 4,5,6,7	itions	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
	Hex	0	1	2	3	4	5	6	7	8	9	A	В	С	D	E	F
0000	0	NUL	DLE	DS		SP	&	-									0
0001	1	SOH	DCI	sos						а	j			Α	J		1
0010	2	STX	DC2	FS	SYN					Ь	k	s		В	К	s	2
0011	3	ETX	DC3							С	1	t		С	L	Т	3
0100	4	PF	RES	BYP	PN.					d	m	U		D	М	υ	4
0101	5	нт	NL	LF	RS					е	f	٧		E	N	٧	5
0110	6	LC	BS	EOB ETB	UC					f	٥	w		F	0	w	6
0111	7	DEL	IL	PRE/ ESC	EOT					g	Р	×		G	Р	x	7
1000	8		CAN							h	9	у		Н	Q	Υ	8
1001	9		EM							i	r	z		ı	R	z	9
1010	A	smm	СС	SM		¢	!		•								
1011	В	VT					\$	0	#								
1100	С	FF	IFS		DC4	<	*	%	@								
1101	D	CR	IGS	ENQ	NAK	()	9	•								
1110	E	so	IRS	ACK		+	;	•	=								
1111	F	SI	IUS	BEL	SUB	ı	7	?	ıı								
									`								
0	1	2 3	3	4	5	6	7	1800 B ₃	/te					Pad	Charac	ter	
0	1	2	3	4	5	6 7	7	EBCDIO	Struc	ture				Dup	licate	Assignm	nent
0	1	2 3 4 5 6 7 Transmitted and received Control Characters															
Notes:		charact	مr is ما	afinad a	ne the o	dd pari	tv char	acters !	(anlv):	n colu	nns 6.2	. 7			k chard ceded b	acters w	/hen
 The stick character is defined as the odd parity characters (only) in columns 6 & 7 (except for 7F) and prefixed with a DLE. Bit configuration (1F) performs the Intermediate Block Check (ITB) function. 																	
2. Bit	config	uration	(It) pe	ertorms	the Inte	ermedic	ite Bloc	k Chec	:к (IIB)	tuncti	on.						117

Figure 69. Extended Binary Coded Decimal Interchange Code (as used in Binary Synchronous Communication)

						1800 (Core Sto	orage By	/te Pos	itions P	,7,6,5	(0, b ₇	, ₆ , t	₅)			
Byte Positions		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
4,3,2,1 (b ₄ ,b ₃ ,b ₂ ,b ₁)	Hex	0	1	2	3	4	5	6	7	8	9	А	В	С	D	E	F
0000	0	NUL	DLE	SP	0	@	Р	\	р								
0001	1	S OH	DC1	1	1	Α	Q	а	q								
0010	2	STX	DC2	"	2	В	R	Ь	r								
0011	3	ETX	DC3	#	3	С	S	С	s								
0100	4	EOT	DC4	\$	4	D	Т	d	t								
0101	5	ENQ	NAK	%	5	E	U	е	U								
0110	6	ACK	SYN	&	6	F	٧	f	٧							:	
0111	7	BEL	ЕТВ	-	7	G	w	g	w								
1000	8	BS	CAN	(8	Н	х	h	x								
1001	9	НТ	EM)	9	ı	Υ	i	у								
1010	A	LF	SUB	*	:	J	z	j	z								
1011	В	VT	ESC	+	;	K	[k	{								
1100	С	FF	FS	,	<	L	_	1	٦								
1101	D	CR	GS	-	=	М]	m	}								
× 1110	Е	so	RS		>	Ν	^	n	~				,				
1111	F	SI	US	1	?	0	-	•	DEL								
															٠		
0 1	2 3	3 4	. 5	6	7	_] ו	800 Byt	е							Pad C	hara c te	г
															Contro	ol Char	acters
0 b ₇ b	6 b	5 b	4 b	3 b ₂	. b		SASCII s appec								Stick	Charac	ters w
st bit					First on li							-				ded by	
otes:																•	

11732

2. Bit configuration (1F) performs the Intermediate Block Check (ITB) function.

Figure 70. Code Structure—USASCII (as used in Binary Synchronous Communication)

Name of Function	Functional	Code Realization				
	Mnemonic	EBCDIC	USASCII			
Start of Heading	SOH	SOH	SOH			
Start of Text	STX	STX	STX			
End of Transmission Block	ETB	ETB	ETB			
End of Text	ETX	ETX	ETX			
End of Transmission	EOT	EOT PAD ⁴	EOT PAD ⁴			
Enquiry	ENQ	ENQ	ENQ			
Negative Acknowledge	NAK	nak pad ⁴	NAK PAD ⁴			
Synchronous Idle	SYN	SYN	SYN			
Data Link Escape	DLE	DLE	DLE			
End of Intermediate Transmission Block	ITB	IUS	us			
Even Acknowledge	ACK0 ²	DLE (70) 1	DLE0			
Odd Acknowledge	ACK1 ²	DLE/	DLE1			
Wait Before Transmit-positive Acknowledge		DLE,	DLE;			
Mandatory Disconnect ³	DISC ²	DLE EOT ^{4,5}	DLE EOT ^{4,5}			
Reverse Interrupt	RVI ²	DLE @	DLE <			
Temporary Text Delay	TTD	STX ENQ	STX ENQ			
Transparent Start of Text	XSTX	DLE STX				
Transparent Intermediate Block	XITB	DLE IUS				
Transparent End of Text	XETX	DLE ETX				
Transparent End of Trans. Block	XETB	DLE ETB				
Transparent Synchronous Idle	XSYN	DLE SYN				
Transparent Block Cancel	XENQ	DLE ENQ				
Transparent TTD	XTTD	XSTX XENQ				
Data DLE in Transparent Mode	XDLE	DLE DLE				
	1 1		I			

- Notes: 1. Hexadecimal representation (no control or graphic assignment).
 - 2. DLE STICK Sequences
 - 3. For switched data link only.
 - The 4 low-order bits of the trailing pad character (all "1" bits) are required for reliability considerations. This is hardware checked.
 - 5. CA hardware ignores the DLE and acts on the EOT alone.

11733

Figure 71. Control Characters and Sequences

STX - Start of Text

Precedes a block of text characters. Text is that portion of the message treated as an entity to be transmitted to the remote station without change. STX also terminates a heading.

ITB - Intermediate Transmission Block

Blocks data by indicating end of intermediate text or heading block. Block check character immediately follows ITB. Blocks of data ending with ITB do not call for replies and follow each other without changing direction of transmission.

ETB - End of Transmission Block

Indicates the end of a group (block) of characters started with SOH or STX. The blocking structure is not necessarily related to the processing format. The block check characters are sent following ETB. The receive station should reply to ETB with its status (Positive or Negative Acknowledgment).

ETX - End of Text

Terminates a block of characters started with STX. The block check characters are sent following ETX. A reply is required from the receive station indicating its status.

EOT - End of Transmission

Indicates the conclusion of a message transmission, which may contain one or more blocks of text and associated headings. For multipoint networks, it causes a reset of the stations on the link.

ENQ - Enquiry

Used as a request for a response, to obtain an indication of remote station status.

NAK - Negative Acknowledgment

Indicates the previous block received was unacceptable and that the receiver is ready to accept a retransmission of the erroneous block. It is also the not ready reply to a station selection.

DLE - Data Link Escape

A control character used to provide supplementary line-control signals for transparent text. The DLE STX initiates transparent text and the DLE followed by ETX, ETB, ITB or ENQ terminates transparent text (see Figure 71).

PAD Character

Two PAD characters are used by the CA, the Pre-SYN and the ending PAD.

<u>Pre-SYN</u>: This PAD character is provided by the hardware and has a bit configuration: 01010101 (55 Hex.). The Pre-SYN PAD precedes the synchronization pattern at the start of a transmission.

PAD (End): This PAD character must be placed in the transmit data table. It has the following bit configuration: 11111111 (FF Hex.). This PAD character follows any turnaround character or sequence.

Extended Control Sequences Causing Line Turnaround

DLE-Stick Characters

The stick characters are double sequence characters. The first character is always DLE and the second character is defined as follows:

- 1. <u>EBCDIC</u>: The odd parity characters (only) that appear in columns 6 and 7 of the EBCDIC chart (Figure 69), except for 7F (Hex).
- 2. <u>USASCII</u>: Those characters that appear in column 3 of the USASCII code chart (Figure 70), except for 3F (Hex).

Character codes 7F in EBCDIC and 3F in USASCII are not used because they might be confused with the PAD character.

The DLE Stick sequences provide a sequential checking control for a series of transmissions. Thus it is possible to maintain a running check to ensure that each reply corresponds to the immediately preceding message block. Figure 71 shows other functions that the stick characters are used for.

Transparent Mode Control

Transparent mode makes the full 256 character codes in EBCDIC available for transmission. A special character, DLE, must precede any control characters in the message otherwise all characters are accepted as text. There is no provision for transparent mode in USASCII. These controls are used when binary information or external codes are to be sent or received. The CA enters transparent mode following a DLE STX sequence. A single DLE followed by an ETB, ITB, ETX or ENQ control character while in receive mode causes the line adapter to leave transparent mode. Exit from transparent mode during transmission is done by inserting DLE END character sequence in the third and second character position from the end of each core table. (END is defined as any of the characters ETB/ITB/ETX/ ENQ.)

In transparency, the transmitting adapter inserts a second DLE after each data DLE from core, and the receiving adapter deletes the first DLE from the data sent to core. DLE SYN are used to maintain synchronization in transparent mode in place of the SYN SYN characters used in normal mode. Frequency of insertion is dependent on line speed. DLE SYN cannot be placed in transparent text by the program as time-fills.

FUNCTIONAL DESCRIPTION

The CA functions as an I/O control between the 1800 system core storage and the transmission line. The CA is fully controlled by 1800 I/O control commands (IOCC), chaining, and the recognition of data link control characters it receives via communications networks or the I/O channel.

The CA can only start transmitting or receiving when the proper XIO Initialize has been programmed. Then the CA monitors data received from the remote station or the I/O channel for control characters and takes the proper action when they are detected.

Data transfers to and from core (on a cycle-steal basis), begin following the generation and recognition of a sync pattern, and end following recognition of an end control character or following a program reset. The data to be transmitted is stored 2 bytes (16 bits) to a location and as many as 4095 bytes are used to comprise a data table. Data transfers end after the end of the table is reached and no chaining is taking place.

For EBCDIC code use, the CA provides automatic checking on the data by generating a 16-bit Cyclic Redundancy Check (CRC-16). These 16 bits constitute two block check characters (BCC) and are hardware generated while transmitting or receiving data. For USASCII code use, the CA parity checks each character and accumulates a Longitudinal Redundancy Check (LRC) character which is one 8-bit BCC

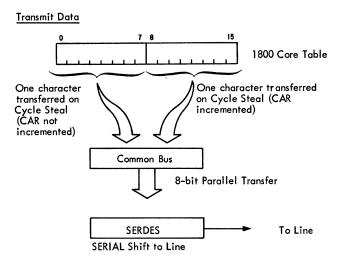
During transmit, the accumulated BCC's are inserted in the data stream at the proper location and during receive, the incoming BCC's are compared with the accumulated BCC's. The received BCC's are not sent to core storage.

The P-C and its program, control and initiate all operations within the CA and are responsible for:

- Proper sequencing of commands.
- Translation to and from data codes.
- Interpreting sense and status information.
- Initiating and terminating operations.
- Proper message and control format.
- Recognizing control characters.
- Generating, in the proper sequence, all control characters except sync patterns and additions/deletions of DLE's during a data transfer.

Data Flow via Common Bus

In transmit mode, data flow is from core to the 8-bit common bus, to the 9-bit Serializer/Deserializer (SERDES), to the data set, to the communication line (see Figure 72). Each 16-bit core word constitutes two 8-bit characters. When the byte counter contains



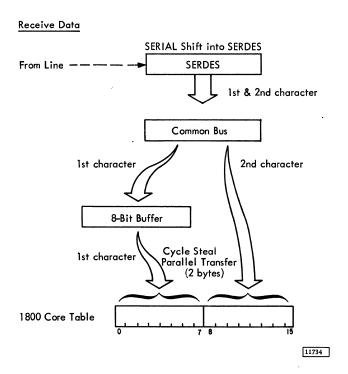


Figure 72. Data Flow - Transmit/Receive

an even count, a non-increment Channel Address Register (CAR) cycle steal is taken and the high order character (core bits 0-7) is transferred to the common bus. When the byte counter contains an odd count, the low order character (core bits 8-15) is transferred to the common bus and the CAR is incremented.

In receive mode, data flow is from communication line to the data set, to SERDES, to the common bus, to the 8-bit buffer register to core. The 8-bit

buffer is used to pack two 8-bit characters into one 16-bit core word. When the byte counter contains an even count, a non-increment CAR cycle steal is taken and the buffer is loaded from SERDES via the common bus. When the byte counter contains an odd count, characters in the buffer and on the common bus are transferred to core word bits 0-15 respectively and the CAR is incremented.

Data transfer between core and SERDES is parallel by byte and serial by character. Data transfer between SERDES and the communication line is serial by bit.

BCC Generation and Error Detection

For EBCDIC code transmission, cyclic redundancy checking (CRC-16) is used for error detection. The cyclic redundancy check uses an arithmetic accumulation of the message bits; this is accomplished by CA hardware. The receiving station performs the same accumulation with the receive data and determines whether the locally generated BCC's are equivalent to the received BCC's.

For USASCII code transmission, the following checks are made:

Vertical Redundancy Check (VRC): The USASCII character structure defines an eighth bit to provide odd parity count for each character. A vertical redundancy check is made on each character for USASCII code transmission in normal transmission mode only. This check is effective on all transmissions such as responses, control sequence and heading/text.

Longitudinal Redundancy Checking (LRC): LRC is defined as follows:

The LRC is generated by taking an exclusive OR independently on each of the individual levels of the transmitted code excluding the parity bit. The correct value of the parity bit for the LRC character is defined so as to maintain odd parity (VRC) for the LRC character.

In each code level, the total number of "one" bits (including any in the LRC) is caused to be even. Thus, the sense of longitudinal parity is said to be even.

Following initialization, the Block Check Character Register (BCCR) is reset until the first STX or SOH character is decoded. Accumulation starts with the character following SOH/STX. All subsequent SOH/STX characters before a line turnaround are included in the accumulation of the remainder. The BCCR is again reset following the ETB, ETX or ITB BCC sequence. In normal text SYN characters are

not accumulated. Within blocks of transparent text, the first DLE character in all two-character DLE sequences (DLE DLE, DLE ETX, DLE SYN) is excluded from accumulation. A SYN character following an excluded DLE is also excluded.

During transmit, the accumulated block check characters are transferred to the line following ETB, ETX or ITB.

During receive, the accumulated block check characters are compared by hardware with the received BCC's following detection of ETB, ETX or ITB. Equal comparison indicates accurate reception. The received BCC's are not transferred to core.

TIMEOUT CONTROLS

Timeouts are used to insure efficient utilization of the communication line and to prevent tie-ups due to false sequences or missed turnaround characters.

Some timeout conditions cause an interrupt, but the program has the option to suppress the time-out interrupt.

Transmit Timeout (No Interrupt)

This timeout is used to automatically insert the synchronous idle sequence in the output data stream.

- 1. Normal mode and transparent mode with external clocking a SYN SYN or DLE SYN sequence is inserted every 1.00 (±0.15) sec.
- 2. Transparent mode with business machine clocking a DLE SYN sequence is inserted at intervals depending on the line speed:

600 baud - 900 (+100) milliseconds (WTC only)

1200 baud - 475 (+50) milliseconds

2000 or

2400 baud - 255 (+25) milliseconds

4800 baud - 106 (+12) milliseconds (domestic only)

The timeout period used in transparent mode is preset by jumper. In either case, insertion of the synchronous idle sequence is delayed when insertion would occur between:

- A DLE and its following control character.
- An END character and the following BCC's.
- The Block Check Characters.
- In the case of all non-ITB ending sequences, insertion is abandoned.

The timeout is restarted when the synchronous idle sequence (SYN SYN or DLE SYN) is detected in the message stream.

Timeout (Interrupt)

This timeout has the following purposes:

- 1. Limits the waiting time allowed for a transmitting station to receive a reply (3 seconds).
- 2. Monitors incoming or outgoing data for SYN patterns. A timeout interrupt will occur in 3 seconds if either of the following occurs in the data stream:
 - A double SYN (SYN SYN) sequence is not decoded in normal mode.
 - Continuous SYN characters are decoded in normal mode.
 - A DLE SYN sequence is not decoded in transparent mode.
 - Continuous DLE SYN sequences are decoded in transparent mode.

A timeout interrupt occurs in 3 seconds if the data set fails to respond to a Request-to-Send with a Clear-to-Send.

A continue timer (nominal 2 seconds) is implemented by using a modifier bit in an Initialize or Sense command.

The timeout interrupt can be suppressed if a 1 is inserted in bit 3 of the cycle-steal byte count word.

Actual time periods are as follows:

Time Period	Secondary Station	Primary Station			
3 second timer	3.0 seconds	2.7 seconds			
2 second continue timer	2.0 seconds	1.9 seconds			
all times ± 100 milliseconds					

11735 A

CA PROGRAMMING

Each line adapter requires a separate Data Channel (DC) to transfer information to and from core if overlapping is desired. In overlap operation, sharing of a DC by both lines is not possible. If overlapping is

not desired, then the DC can be shared by the line adapters.

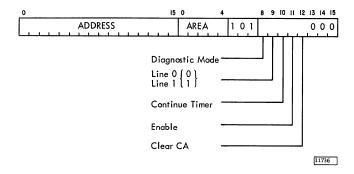
Information to be transmitted must be arranged in consecutive core locations, two eight-bit characters per word and a maximum of 4095 characters per table. This area of core constitutes a transmit data table and includes control characters as well as text characters. The characters must be coded in the transmission code selected for the CA.

If more than 4095 characters are to be transmitted, several transmit data tables can be chained together and sent as one message. When the CA is in receive mode, areas of core must be reserved as received data tables for expected messages.

A complete message can be transmitted or received using one Execute I/O instruction that specifies an I/O control command (IOCC) of Initialize CA to start the operation. Each communication line in use must be programmed with separate Execute I/O instructions. The format and significance for each of the IOCC's for the CA follows.

Initialize CA

This command initializes the CA and causes the cycle-steal byte count word to be fetched from a location determined by the Address Word. The cycle-steal byte count word is decoded for further definition of the Initialize CA command. After completing a hardware synchronization procedure, the Serializer-Deserializer (SERDES) transfers information to or from the line at speeds determined by the line baud. SERDES transfers information to or from core storage on a cycle-steal basis at the character rate which is 1/8 baud.



Address: This field, located at an even core location, contains the core storage address of the first word of the data table, which is the cycle-steal byte count word.

Area: The area code specifies which CA is to respond. The area codes are assigned as follows:

CA	Code
1	21 (10101)
2	22 (10110)
3	23 (10111)
4	20 (10100)

 $\underline{\text{Function}}$: 101 - Three-bit field that designates an initialize operation.

Modifier: The modifier bits expand the Initialize CA command as follows:

- Bit 8 Diagnostic Mode: When bit 8 is a 1, the operation of the CA is changed as follows:
 - 1. The send data line to the data set is also looped back to the input of SERDES in transmit mode.
 - All characters are read from or stored in the low order core bits 8-15.
 - 3. After each character while transmitting, and before each character while receiving, the diagnostic DSW word is stored. This is accomplished automatically by the adapter on a cycle-steal basis.

Figure 73 illustrates the setup of diagnostic transmit and receive data tables.

- Bit 9 When bit 9 is a 0, line 0 is designated. When bit 9 is a 1, line 1 is designated.
- Bit 10 Continue Timer: When bit 10 is a 1, the 3-second timeout is changed to 2 seconds and the timer is started. This new timeout period remains effective until:
 - 1. A timeout interrupt occurs.
 - 2. A change from receive to transmit, or vice versa, occurs.
 - 3. A Clear CA is given.

Note: A cold start Initialize CA command or an Initialize CA command that changes modes resets the continue timer.

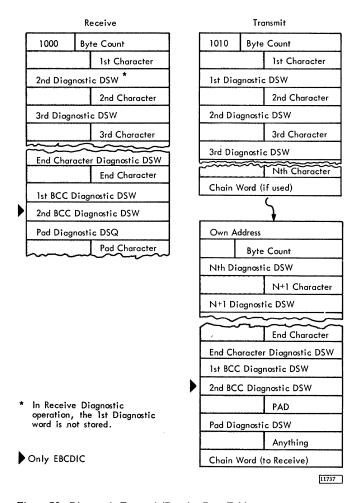


Figure 73. Diagnostic Transmit/Receive Data Tables

Continue Timer is used when the program is not ready to send or receive the next record. In the case of a transmit, as a master station, the program should send TTD after the timeout. In case of a receive, as a slave station, WACK should be sent.

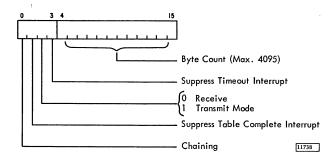
Bit 11 - Enable: The action of this bit is covered under the Sense Device command.

Bit 12 - Clear CA; When on (1), this bit resets selected triggers and latches in the addressed line adapter to enable a restart from a known condition. The SERDES triggers, which are readable by a Sense Device command, are not reset by this command.

Note: Two XIO Initialize CA commands, which both specify receive mode, may be programmed providing an intervening XIO Sense-Clear CA command is given.

Cycle-Steal Byte Count Word

The format and significance of the cycle-steal byte count word is shown below.



Chaining - Bit 0: When this bit is a 1, an automatic chain to a new table occurs when the end of table is reached. The last word of the table must contain the address of the next table. The first word of the next table must contain its own address. A hardware check is made on this first word. If it is not its own address, a CAR check occurs. The second word of the new table is a new byte count word. The chain rules are contained in the following table:

From Table	To Table	Chaining
Transmit with XITB Transmit w/o XITB Transmit with XITB Transmit w/o XITB Receive Receive	Transmit Transmit Receive Receive Receive Transmit	Mandatory Optional (1) Illegal Mandatory (2) Optional (3) Illegal
1) 10	. 1.1	

1) If message transmission not completed.

11739

Suppress Table Complete Interrupt - Bit 1: When this bit is a 1, the table complete interrupt will not occur when the byte count goes to zero.

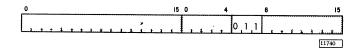
If message transmission completed and response is expected.
 Chaining two receive tables may present programming problem in determining the location of end character.
 See description of bits 3 and 4 of operating DSW.

Receive/Transmit - Bit 2: When this bit is a 1, the CA is conditioned for transmit mode and characters are sent to the data set. When this bit is a 0, the CA is conditioned for receive mode and characters are received from the data set.

Suppress Timeout Interrupt - Bit 3: When this bit is a 1, a timeout interrupt will not occur for this table.

Byte Count - Bits 4-15: The byte count should contain the number of 8-bit characters in the table. All characters including the PAD and "anything" characters should be counted. If an odd byte count is specified, the first character (bits 0-7) after the byte count word is not used or counted and may be anything. Maximum byte count is 4095₁₀.

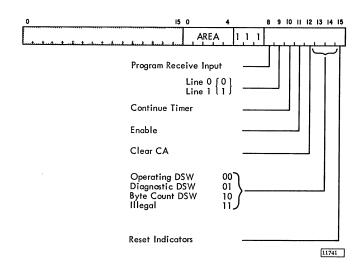
Sense Interrupt Level



This command loads the ILSW of the highest priority interrupt pending into the accumulator. The interrupt levels of a given CA are on the same level and are assigned by the customer. The interrupt level status bit for each line is also assigned by the customer. When the interrupt for the CA is the highest priority pending, the assigned bit appears in the P-C accumulator for the line which is interrupting.

Sense Device

This command is used to load one of the three DSW's into the P-C accumulator. In addition, other functions can be conditioned by use of the modifier bits.



Address: Not used.

Area: The area code designates one of the CA's.

<u>Function:</u> 111 - This bit code specifies a Sense Device command.

<u>Modifiers</u>: The modifiers expand the Sense Device command as follows:

Bit 8 - Program Receive Input: This bit is used to complement the program receive input for the line addressed. It is used when the line adapter is in receive mode to cause a space (0-bit) on the receive data input to SERDES. A subsequent command with this bit on (1) resets the receive data line to a mark (1-bit). Thus the receive input data can be controlled with a series of commands appropriately timed.

Note: The data set cable switch must be in the test position if interference with real input data is to be avoided.

- Bit 9 Performs line select function: 0= line 0: 1= line 1.
- Bit 10 Continue Timer: Action of this bit is identical to its use in the Initialize CA command. This bit can also be used to start the timer.
- Bit 11 Enable: When bit 11 is a 1, two latches are set on for the addressed line adapter. The functions of the latches are as follows:
 - 1. The first latch enables the line adapter to allow an End-Character-Decoded or Ringing interrupt when the data set indicates a ringing condition and the CA is not initialized. This latch is reset by issuing another command with bit 11 off (0).

Note: If the line adapter is initialized, a ringing interrupt cannot occur. This function is therefore negated when attempted with the Initialize CA command.

- 2. The second latch is used for World Trade data sets in those applications where the "Data Terminal Ready" option is used. When the option is selected, this latch directly controls the data terminal line. The latch requires a Clear CA or DC reset to clear.
- Bit 12 This bit performs the same function as it does when given during the Initialize CA command. In addition, the data set will go "on Hook" (data set ready reset) when switched network is being used. The actual reset of the data set ready line is dependent on the delay encountered with the type of data set used.

Bits 13

& 14 - <u>DSW Selection</u>: These bits determine which DSW is loaded into the P-C accumulator as follows:

<u>13</u>	14	$\overline{\mathrm{DSW}}$
0	0	Operating
0	1	Diagnostic
1	0	Byte Count
1	1	Illegal

Bit 15 - Reset Indicators: If this bit is a 1 when the sense operating DSW is given, the latches associated with bits 0 through 7 and bit 9 are reset.

Interrupt

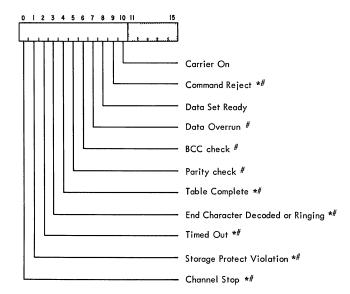
The CA has several conditions that cause interrupts to the P-C. These interrupts are defined in the operating DSW.

It is possible that CA operation could be suspended by an interrupt on a higher level. This could cause data overrun. The following is a recommended procedure for servicing CA interrupt:

- 1. Sense the operating DSW without reset.
- 2. Service the interrupt reflected in the DSW. If servicing requires a Clear CA (due to channel stop or a need to do a second receive operation, etc.), the clear should be delayed until the next XIO (to transmit or receive) is performed. At that time the following series of XIO's are done:
 - Clear CA
 - Enable CA
 - Initialize CA

The Clear CA will (1) reset the DSW and (2) prevent dropping the line by the following enable and/or initialize XIO's. (The XIO's effectively mask all interrupts during their execution and the execution of the next instruction.)

Operating DSW



^{*} Causes Interrupt.

11743 A

[#] Indicator reset by a sense DSW (Other indicators are reset by their status turnoff).

Channel Stop - Bit 0: This indicator is turned on and causes an interrupt when a P-C or Bus Out parity error or a CAR check error is detected during load CAR, Check-CAR, and XIO control cycles of the Initialize and Sense commands.

It is also turned on when a storage protect violation (bit 1) occurs.

When this error occurs in the CA, the line adapter is inhibited from taking any more cyclesteal cycles. The indicator is turned off with an IOCC Sense Operating DSW with bit 15 in the modifier on.

Storage Protect Violation - Bit 1: This indicator is turned on and causes a channel stop (bit 0) interrupt when the CA tries to store received data into a storage protected word of core.

The indicator is turned off with an IOCC Sense Operating DSW which has bit 15 in the modifier on.

Timeout - Bit 2: This indicator is turned on and causes an interrupt if a double SYN or DLE SYN is not detected for 3 seconds after CA initialization, or SYN's or DLE SYN's have been on a line continuously for over 3 seconds, in normal mode or transparent mode respectively.

A timeout also occurs in 3 seconds in transmit mode if the Clear-to-Send line is not activated by the data set in response to the Request-to-Send signal. If continue timer was previously specified, the timeout occurs in 2 seconds. The timeout also occurs if a table complete with no chaining condition exists in transmit mode, and a receive table has not been initiated.

The indicator is turned off with an IOCC Sense Operating DSW which has bit 15 on in the modifier. The program also has the option to suppress the timeout interrupt.

End-Character-Decoded or Ringing - Bit 3: This bit is turned on and causes an interrupt upon detection of a turnaround character during receive. The interrupt is delayed until after the PAD character is stored. Turnaround characters are defined as: ENQ, NAK, DLE STICK, EOT, ETX and ETB. For EOT and NAK, at least four 1-bits of the following PAD character must be received for the character to be recognized as a turnaround.

DLE STICK, EOT and NAK will not cause an interrupt if they appear in text after SOH/STX is received.

This bit, when set, stops all cycle stealing on this line. Therefore, the byte counter can be sensed before resetting the DSW bit to find the turnaround character. To find the exact location of the turnaround character, the following may be done:

- 1. Complement the sensed byte count (e.g., complement of 0111 = 1000).
- 2. Subtract the complemented byte count from the original byte count.
- 3. If the original byte count was odd, add 1 to the remainder.
- 4. Divide the result by 2.
- 5. Add the quotient to the address of the byte count word for this table. This new address points to the turnaround character.
- 6. If a remainder is obtained from step 4, the turnaround character is in bits 8-15, otherwise it is in bits 0-7.

Note: The preceding procedure assumes the PAD character is the next byte in the table and no chaining has occurred.

This indicator is also turned on by the "Ring Indicator" in the data set interface if the CA is enabled and not initialized. If the CA is initialized, an incoming ring will not set this indicator. The End-Character-Decoded and Ringing conditions must be distinguished by program retention of the initialization state.

<u>Note:</u> The CA (line adapter) must be initialized or disabled before a ringing interrupt is reset by the Sense Device command. (This inhibits the ring indicator from causing another interrupt.)

Table Complete - Bit 4: Unless suppressed by bit 1 of the byte count word, this indicator is turned on and causes an interrupt at the end of a table (byte count = 0).

In receive, this interrupt occurs simultaneously with an End-Character-Decoded if the table ends with the PAD character as the last byte. Since bits 3 and 4 may occur simultaneously, determining the location of the end character may be difficult when chaining receive tables.

This indicator is turned off with an IOCC Sense Operating DSW which has bit 15 in the modifier on.

Data Parity Check - Bit 5: This indicator is turned on when a parity error is detected during core storage data transfers or when a VRC error is detected in USASCII mode.

In USASCII mode, a transmit or receive VRC error sets this bit on. The detection of the VRC error blocks the loading of the accumulated BCC to the line during a transmit. Transmission continues, but the BCC sent contains all 1's which the receiving station detects as an error.

The indicator is turned off with an IOCC Sense Operating DSW which has bit 15 in the modifier on.

Data BCC Check - Bit 6: This indicator is turned on if a BCC error is detected when the accumulated BCC's are compared with the incoming (received) BCC's. For EBCDIC, the BCC's are 2 CRC characters (16 bits). For USASCII, the BCC is an LRC character (8 bits).

The indicator is turned off with an IOCC Sense Operating DSW which has bit 15 in the modifier on.

Data Overrun - Bit 7: This bit is turned on if a cycle steal request for a character transfer is not acknowledged before an overrun condition occurs. An overrun occurs if the one bit time of buffering is exceeded.

This error blocks the loading of the accumulated BCC to the line during transmit. Transmission continues, but the BCC sent contains all 1's which the receiving station detects as an error.

The indicator is turned off with an IOCC Sense Operating DSW which has bit 15 in the modifier on.

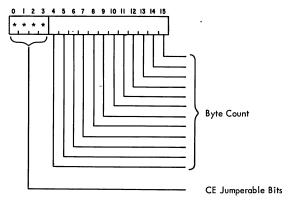
Data Set Ready - Bit 8: This bit is a 1 whenever the "Data Set Ready" line in the interface is on.

Command Reject - Bit 9: This bit is set to 1 and causes an interrupt when the CA is given an Initialize CA command with the clear CA bit (bit 12) off while the line addressed is either in transmit or receive mode and has received two SYN characters without receiving a turnaround character.

The indicator is reset with an IOCC Sense Operating DSW which has bit 15 in the modifier on.

Carrier On - Bit 10: This bit is on (1) when the carrier detect line from the data set indicates a carrier is being detected. For 4-wire networks, the bit is always on. For 2-wire switched networks, the bit is on only when a carrier is being received from a transmitting station.

Byte Count DSW



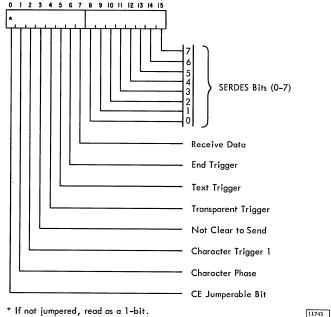
* If not jumpered, these bits read as 1's.

11744

CE Jumperable Bits - Bits 0-3: These bits are available to the CE for diagnostic purposes. If they are unjumpered, they are read as 1's.

Byte Count - Bits 4-15: These bits reflect the status of the entire byte count register in 1's complement at the time the IOCC Sense Byte Count DSW is given.

Diagnostic DSW & Diagnostic Cycle Steal



CE Jumperable Bit - Bit 0: This bit is available to the CE for diagnostic purposes. If not jumpered, it is read as a 1-bit.

Character Phase - Bit 1: This indicator is off for the duration required to transmit the initial Pre-SYN PAD and SYN characters used for bit and character synchronization, and while receiving the two SYN characters used for character synchronization.

Character Trigger 1 - Bit 2: This indicator reflects the status of the first bit in the character counter. This counter is held reset except when receiving or transmitting the following:

- 1. The initial Pre-SYN PAD and SYN characters.
- 2. SYN characters in the data stream.
- Characters following an end character.

At these times, character trigger 1 alternates on and off for each character time.

Not Clear to Send - Bit 3: This indicator is the inverted "Clear-to-Send" line from the data set interface. It is on at all times except when the data set is in the transmitting state.

Transparent Trigger - Bit 4: This indicator is turned on by a DLE STX sequence. It is turned off by the DLE END sequence, where END is defined as ETB, ITB, ETX or ENQ.

Clear CA line also resets this trigger.

Text Trigger - Bit 5: This indicator is turned on by the first character after SOH or STX in a message.

It is reset when the mode is changed (changing from a transmit to a receive mode).

Clear CA line also resets this trigger.

End Trigger - Bit 6: This indicator is turned on when any one of the following end characters are recognized: ETB, ETX, ITB or ENQ and any of the following if not preceded by SOH or STX: NAK, EOT or DLE Stick. In transparent mode, only the first four characters are recognized but they must be preceded by a DLE character and be at the proper table location.

Reset occurs at End-Character-Decoded time. Clear CA line also resets this trigger.

Receive Data - Bit 7: This indicator reflects the status of the receive data line. It is on when a mark (1-bit) is present. When the receive data is marking, the program receive input trigger may be used to cause a space (0-bit) condition.

Serializer-Deserializer (SERDES) - Bits 8-15: The right half of the Diagnostic DSW is assigned to the Serializer-Deserializer.

These 8 bits (triggers) of SERDES are the bits transferred to and from core storage and the communication line.

The 9th trigger (line trigger) of the S/D acts as a line bit buffer while the transfers are taking place. This trigger is not readable.

Data from the data set enters the 1st SERDES trigger, and data to the data set is transferred from the line trigger on every bit sampling time during normal receive or transmit operations.

Note that in a two-wire system, the transmitted data is seen back at the input to SERDES delayed by the time it takes to pass through the modulator and demodulator of the data set. Also note that with the switch on the cable to the data set in "Test" mode, the transmitted data is seen back at the input to SERDES delayed by one bit time.

IMPLEMENTATION OF BSC

Transmit Mode

During transmit mode the CA implements the BSC control characters as follows:

SYN

To enable the receiving station to establish and maintain character phase (synchronization), the CA:

- 1. Generates a SYN SYN sequence for transmission prior to the first character in the transmit data table.
- Generates a SYN SYN sequence for insertion in the data stream every second in normal mode.
- 3. In transparent mode, generates a DLE SYN sequence for insertion in the data stream at intervals depending on the line speed.

The program can insert SYN characters for time-fills in normal mode (up to 2.5 seconds only). DLE SYN sequences cannot be inserted by program as time-fills in transparent text.

SYN characters are not included in the BCC accumulation except when appearing as data in transparent text.

SOH and STX

These two control characters initiate block check transfer accumulation. The initial SOH or STX is not included in the accumulation; but any subsequent SOH and/or STX in a data table are included in the BCC accumulation.

Use of an SOH or STX after an ITB sequence is optional and when used will be accumulated.

The initial SOH, STX or DLE STX character(s) should be placed in the transmit data table in a position which ensures that the END character appears in the low order byte (bits 8-15).

When an odd byte count is used, the first character transmitted is the right-hand byte of the first data word. The left-hand byte is not transmitted and can be anything.

ETB, ETX, ITB, ENQ

ETB, ETX and ENQ are used for end characters to signify the end of a transmission. After an end character is sent (ENQ excluded), the CA sends the accumulated BCC's which are then followed by the PAD

character. For an ENQ ending, just the PAD character follows the ENQ character.

The ITB is used to end intermediate data blocks within a transmit data table and does not result in line turnaround. After the ITB character is sent, the CA sends the accumulated BCC's which are then followed by the remainder of the transmit data table.

A normal (non-transparent) ITB sequence is not restricted to location within a transmit data table. An XITB (transparent ITB) must appear at the end of a transmit data table, if it is not the last table of a chain of transmit data tables. The XITB requires chaining.

DLE

A DLE control character followed by STX places the CA in transparent text mode.

While in transparent mode, the CA inserts a DLE character into the data stream whenever a DLE is received from core storage (except when byte count = 3 or less). This enables the receiver to differentiate between data DLE's and control DLE's. Only one DLE in the DLE DLE sequence is included in the BCC accumulation.

The DLE SYN sequence, hardware generated, is the sync idle sequence used in transparent mode and it is not included in the BCC accumulations.

DLE followed by ETX, ETB, ITB, or ENQ and at the correct transmit table location in core, causes the adapter to leave transparent mode and proceed as in normal transmission ending. The DLE in this ending sequence is not included in the BCC accumulation.

PAD Character

To ensure that the last bit of the last character is properly transmitted by the data set, a PAD character must follow each turnaround character (EOT, DLE-Stick, NAK and ENQ). In the case of ETB and ETX, the PAD character is transmitted following the BCC's. In either case, it is placed in core storage by the program and it consists of all 1's (FF Hex).

Receive Mode

During receive mode the CA monitors the communication line for data and responds accordingly when the following control characters are detected.

SYN

After being set to receive mode the CA establishes character phase with the transmitter when it detects two consecutive SYN characters. If character phase is not established in 3 seconds, an interrupt is generated and the timed out indicator is set on.

All SYN characters appearing in the data stream are stripped from the data going to core storage. SYN characters are not accumulated in the BCC except when they appear in transparent text.

SOH and STX

These two control characters initiate BCC accumulation. The initial SOH or STX is not included in the accumulation, but any subsequent SOH or STX in a data table are included in the BCC accumulation.

ETB, ITB and ETX

Detection of the ETB, ITB or ETX indicates that the BCC's are to follow immediately. The incoming BCC's are hardware compared with the accumulated BCC's and equal comparison indicates no transmission error. For non-ITB ending sequences, the CA remains in receive mode, but generates an End-Character-Decoded interrupt after the BCC's have been tested and the PAD character stored.

If a non-ITB ending is received, cycle stealing halts, and the program may sense the byte count to locate the end of the received message block.

If an ITB ending is received, cycle stealing will not halt and no End-Character-Decoded interrupt is given. The BCC's are checked however, and any error is maintained until a Sense DSW command is given.

ENQ, NAK, EOT, DLE-STICK

These characters will be recognized and cause an End-Character-Decoded interrupt after the PAD character has been transferred to core.

A hardware format check is made on the NAK and EOT characters. If four 1-bits (low order portion of PAD) do not follow immediately, an interrupt does not occur. NAK, EOT or DLE-STICK do not cause interrupts if they appear in text following the SOH or STX character.

The DLE STX sequence sets the adapter to transparent text mode (both transferred to core). A DLE DLE sequence is interpreted as a data character, and the first DLE is stripped from the data sent to core. The DLE SYN sequence is also detected and deleted from the data going to core.

None of the deleted characters are included in the BCC accumulation.

A DLE followed by an ETB, ITB, ETX or ENQ causes the CA to leave transparent mode. The DLE character preceding the block ending character is stripped from the data going to core and is not part of the BCC accumulation.

The rest of the ending sequence is handled as in normal mode (ETB, ITB and ETX description).

Note: If DLE ITB is used when transparent text data is transmitted, then each subsequent intermediate block of transparent text data must start with DLE STX.

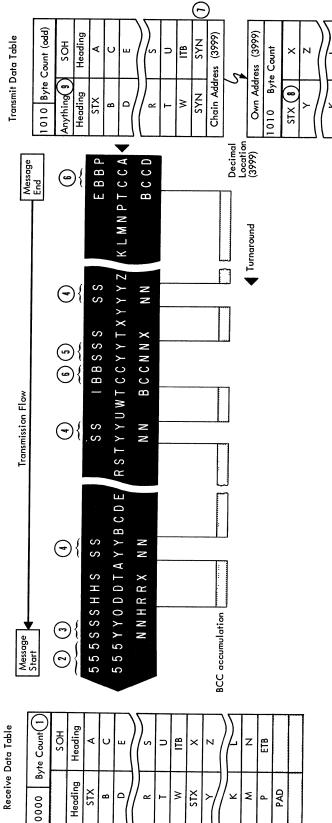
EXAMPLES OF TRANSMIT AND RECEIVE SEQUENCES

Normal Mode

Figure 74 illustrates a sample transmission between two stations. The code used can be either EBCDIC or USASCII.

Transparent Mode

Figure 75 illustrates a sample transparent mode transmission between two stations. Transparent mode is only possible for EBCDIC code transmission.



Pre-SYN pad characters hardware generated and stripped at receive station. Three pre-SYN pads are required for business machine clocking, one for data set clocking.

Byte Count must be long enough to accomodate longest transmitted message. Chaining can also be used.

Notes:

- Initial double SYN sequence used to establish Character Phase between stations. Hardware generated.
 - (4) Synchronous Idle characters inserted and stripped by hardware. Not accumulated in BCC or sent to core. Used to maintain synchronization.
- (5) Double SYN characters from core treated as a synchronous idle sequence.
- (6) BCC's automatically inserted in message stream. Only one BCC is used in USASCII code.

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Figure 74. Transmit/Receive Sequence — Normal Mode

Double SYN characters from core treated as Synchronous Idle.

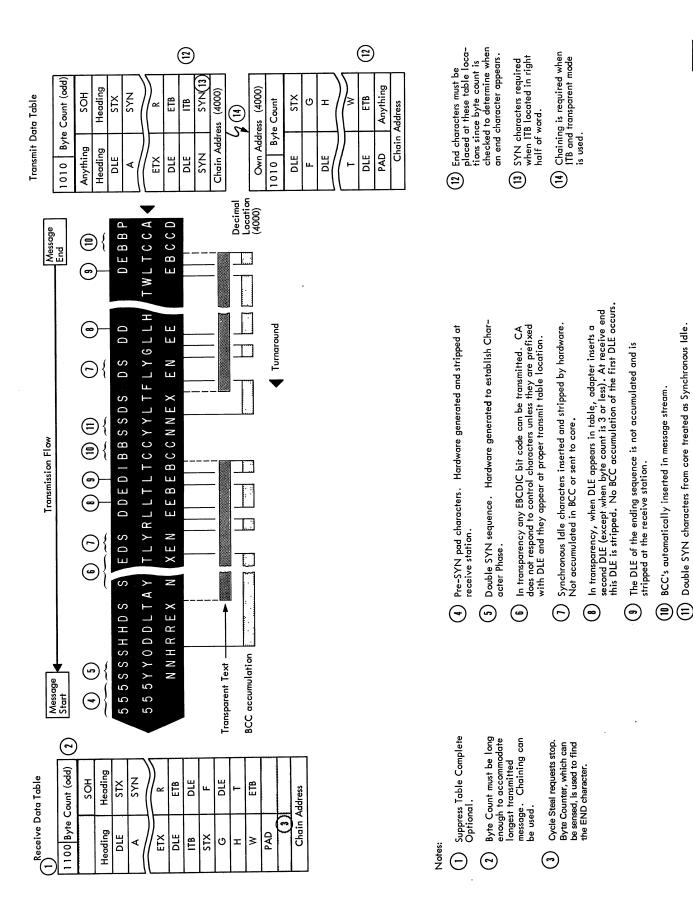


Figure 75. Transmit/Receive Sequence - Transparent Mode

SELECTOR CHANNEL

INTRODUCTION

The selector channel provides a means for attaching the IBM 2841 Storage Control Unit (see <u>2841 Storage Control-Component Description</u>, A26-5988) with up to eight IBM 2311 Disk Storage Drives to the 1801/1802 Processor-Controller. The selector channel adapter is located in the 1826 Data Adapter Unit, Model 2 or Model 3. The Model 2 must be abutted to the 1801/1802.

Mode of Operation

The selector channel operates in burst mode only using the cycle-stealing facilities of the processor-controller (P-C).

The maximum instantaneous data rate that can be handled by the selector channel is 333 kilobytes per second. Up to three microseconds may be required for the channel to respond to a service request by the control unit after a data transfer has been started.

PROGRAMMING

Modified 1800-commands are used to control the selector channel. The concepts of I/O control are the same as for System/360 channel; that is, a channel command word (CCW), a channel status word (CSW), and a Start and Halt I/O command are used.

However, programming for I/O devices is not compatible with System/360 programming for the same devices.

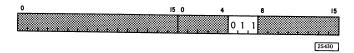
The Initialize Write command is used to effectively produce a Start I/O command. It selects the control unit and device, and contains the address of the CCW. The CCW specifies the I/O command to be executed, and designates the storage area associated with the operation. The CCW also specifies the length count in data transfer operations. Data is transferred using the 1800 data channel.

Execute I/O

The Execute I/O (XIO) instruction initiates all input/output channel operations. The selector channel responds to four different functions as specified by the Input/Output Control command (IOCC).

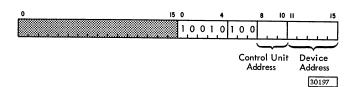
- 1. Sense Interrupt Used to indicate when the channel is requesting service.
- 2. Control (Halt I/O) Used to prematurely terminate the current I/O operation.
- 3. Sense Device (Channel Status) Used to indicate the status of the channel.
- 4. Initialize Write (Start I/O) Used to initiate I/O operations.

Sense Interrupt (011)



This command directs the selector channel to place its interrupt bit into the accumulator. The selector channel ILSW bit is assigned by the customer.

Control (Halt I/O - 100)



This command causes the execution of the current I/O operation to be terminated. If the channel is not busy, modifier bits 8-15 identify the 2311 to which the Halt I/O applies.

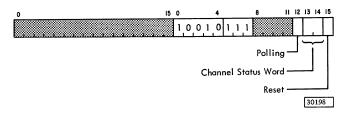
When the channel is available (not busy), and the 2841 is busy, the addressed 2311 is selected and signaled to terminate the current operation. Halt I/O does not affect the state of the control unit when both the channel and control unit are available.

If a Halt I/O is issued when the channel is executing a data transfer, the data transfer is terminated and the device performing the operation is immediately disconnected from the channel. In this case, the address in modifier bits 8-15 is ignored. A

channel end/device end interrupt is signaled by the channel.

When a program check occurs, a Halt I/O should be issued to reset the selector channel.

Sense Device (Sense Channel Status - 111)



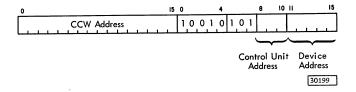
This command directs the selector channel to make its current indicator status available in the accumulator. Modifier bits 13 and 14 specify which of the four words comprising the channel status word (see "Channel Status Word") is to be interrogated.

Modifier bit 12 on (1) suppresses polling. Polling is restarted following the completion of a Start I/O operation or after another Sense Channel Status with modifier bit 12 set to 0.

Polling is the ability of the selector channel to acknowledge a request for service from the control unit. The service request is usually the result of a device end or attention bit in the unit status byte from the control unit. If the suppress polling bit is off, the channel places the 2841's address and unit status in the CA/CB registers and interrupts the P-C. The selector channel automatically suppresses polling to prevent other 2311's from superimposing status before the program has stored the former status.

Modifier bit 15 on (1) resets the selector channel status with exception of the status pending bit which is reset when the unit address-status is interrogated.

Initialize Write (Start I/O - 101)



This command initiates I/O operations. The Address word of the IOCC contain the address of a channel

command word (CCW) which instructs the control unit to perform a specific operation.

Modifier bits 8 to 15 contain the device addresses, which are assigned by the user at installation time.

Initiation of the IOCC is under program control. The selector channel continues the I/O operation in cycle-steal mode. The channel fetches the first CCW. If chaining is specified by the CCW, then the channel fetches the next CCW by stealing three cycles when the first CCW operation is complete.

CHANNEL COMMAND WORD

The channel command word contains information that directs the control unit and I/O devices to perform specific operations. The CCW consists of three 16-bit words that are located in three adjacent main storage locations. The three words are designated as follows:

- 1. Byte Count
- 2. Flags and Command Codes
- 3. Data Address

Byte Count

The byte count (Figure 76) specifies the length of the input or output data field. The maximum length (number of eight-bit bytes) which may be specified is 65,535 bytes.

All CCW's including immediate commands must have a non-zero byte count, (excluding transfer-in-channel).

Flags and Command Codes

The second word of the CCW (Figure 77) consists of flags and command codes. The flag bits (0 to 4) indicate certain conditions to the program and control chaining of commands and data. The command codes (bits 8-15) specify the operation to be performed by the control unit and I/O devices.

Flags

Chain Data (CD): Bit 0 on (1) specifies chaining of data. When data chaining is specified, the selector channel automatically fetches the next CCW when the byte count defined by the current CCW goes to zero. The new CCW located at the next higher core storage address designates a new data address.

The command code in the new CCW is ignored unless it specifies transfer-in-channel.

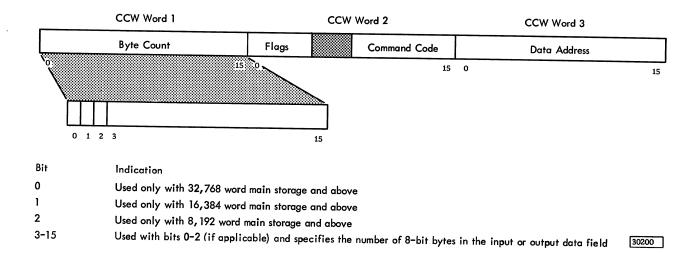


Figure 76. Byte Count (CCW Word 1)

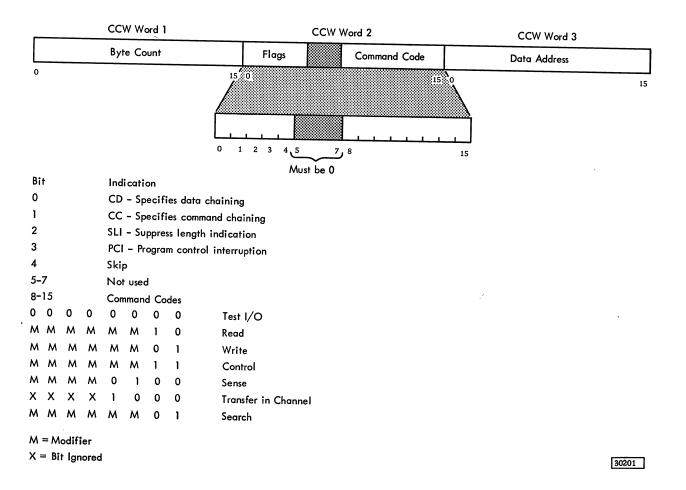


Figure 77. Flags and Command Code (CCW Word 2)

Data chaining continues until a CCW is found that does not specify chaining or the device terminates the operation by presenting ending status.

Chain Command (CC): Bit 1 on (1) specifies command chaining. When command chaining is specified, the selector channel fetches a new CCW and initiates a new I/O operation upon completion of the current CCW. The new CCW is automatically executed when the I/O device completes the current operation and signals device end. If CD and CC bits are both on, CD will take precedence.

Suppress Length Indication (SLI): Bit 2 determines whether an incorrect length condition is to be indicated. When this bit is on (1) and the CD bit is 0 in the last CCW used, the incorrect length indication is suppressed. When both the CC and SLI bits are on (1), command chaining takes place regardless of the presence of an incorrect length indication. Absence of the SLI bit or the presence of the CD bit causes the program to be notified if an incorrect length indication occurs.

The SLI bit must be on when performing a write function to a control unit or an incorrect length indication will occur.

When a CCW contains an immediate command code, incorrect length is not posted even though the byte count must be non-zero.

Program Control Interruption (PCI): Bit 3 on (1) causes the channel to generate an interrupt condition upon fetching the CCW.

Skip: Bit 4 on (1) specifies suppression of data transfer to main storage during a read or sense operation. Skip is used only in conjunction with data chaining.

Command Code

The command code in the CCW specifies to the channel and I/O devices the operation to be performed. The two low-order bits (14 and 15) of the command code identify the operation of the selector channel. If these bits are 00, the four low-order bits (12-15) identify the operation. The high-order bits contain modifiers which specify to the device how the operation is to be executed.

The bit configurations for commands are shown in Figure 78.

Test I/O: This command causes the 2841 to present its current unit status to the selector channel. The channel interrupts the program when this status is available. A Test I/O command should not be included within a chain of CCW's that specify command chaining. The Test I/O command causes command chaining to terminate, even if the CC bit is on (1).

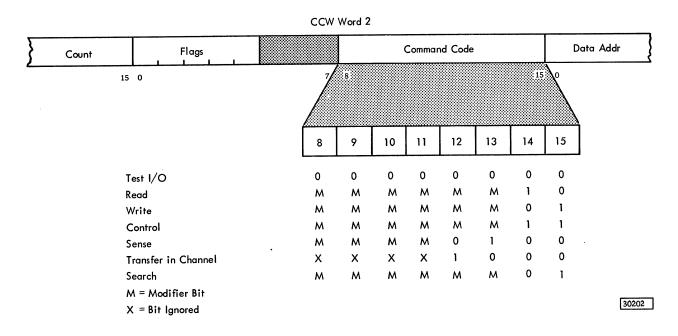


Figure 78. Command Code Assignment

It is not necessary to issue a Test I/O command prior to initiating an I/O operation with a specific unit. The channel checks the unit status while initiating the I/O operation. If the status is unacceptable, it is presented to the program with an interrupt.

Read: This command causes data to be transferred from a 2311 to main storage. The 2311 is specified in the modifier field of the IOCC.

The data address of the CCW specifies the leftmost main storage location of the field where the data is to be stored. Data is placed in main storage in an ascending order of addresses, two bytes per storage location.

The length of the data field is specified in the byte count of the CCW. Data transfer continues until the specified number of bytes have been transferred or until the 2841 terminates the operation. If the byte count is odd, the last byte is placed in bits 0-7 of the last word and bits 8-15 are set to 0's.

<u>Write</u>: This command causes data to be transferred from main storage to a 2311. The data is transferred to the 2311 specified by the device address in the modifier field of the IOCC.

The data address of the CCW specifies the leftmost main storage location from which the data is transferred. The data must be in ascending order in main storage, two bytes per word.

The length of the output record is specified by the byte count of the CCW. Data transfer continues until the specified number of bytes has been transferred or until the 2841 terminates the operation. If the byte count is odd, the last byte is transferred from bits 0-7 of the last storage location addressed.

A write command must be accompanied by the SLI flag bit on in the CCW to avoid a wrong length indication.

Control: This command generally initiates mechanical action at the specified 2311 and does not involve transfer of data. Therefore, the 2841 sends channel end as soon as the control command is received. The 2311 sends device end after it has completed the operation specified by the command (Seek, Recalibrate, etc.). The two low-order bits of the command code (11) identify the operations as a control. The modifier bits received by the 2841 are decoded to determine which of several possible functions are to be performed.

<u>Sense</u>: This command provides the system with information regarding unusual conditions detected in the last I/O operation performed by the selector

channel. The current status of the device that executed the operation is also presented.

The Sense command operates similar to a Read command. The data address of the CCW specifies the leftmost core storage location of the field where the data is to be stored. Two bytes of sense data are placed in each main storage word in ascending order until the byte count has been satisfied.

The following sense bytes are provided; they contain more detailed information than does the unit-status byte.

Sense Byte 0	Sense Byte 1	Sense Byte 2	Sense Byte 3	
Command Reject	Data Check in Count Area	Unsafe	Ready	
Intervention Required	Track Overrun	not used	On Line	
Bus-Out Parity	End of Cylinder	Serializer Check	Unsafe	
Equipment Check	Invalid Sequence	not used	not used	
Data Check	No Record Found	ALU Check	On Line	
Overrun	File Protected	Unselected File Status	End of Cylinder	
Track Condi- tion Check	Missing Add- ress Marker	not used	not used	
Seek Check	Overflow Incomplete	not used	Seek Incomplete	

30203

Transfer-in-Channel: This command causes the next CCW to be fetched from the location specified by the address field of the current CCW. TIC does not initiate any I/O operation and the 2841 is not aware of the operation.

This command provides chaining between CCW's not located in adjacent three word areas; it is considered as an unconditional branch regardless of the status of the chaining flag bit.

Search: This command is used to locate and identify information or areas previously written on the disk pack. During the search operation the channel operates in a write mode, sending data from main storage to the 2841, while the 2841 operates in a read mode, accepting data from the storage device. The 2841 compares the two sets of data. Both the channel and the control unit are busy during the operation.

If the search condition is satisfied, a status modifier indication is sent to the channel. The

channel then fetches the next CCW in the command chain from a location six addresses higher than the current (search) CCW. That is, one CCW, usually a Transfer-in-Channel, is skipped. This allows for modification of the command chain as a result of the data recorded on the track.

Data Address

For read or write operations, bits 0 to 15 of the data address (Figure 79) specify the address of the first byte in an input or output data field. If the command code specifies a Transfer-in-Channel command, the data address contains the address of a new CCW.

Command Chaining

Facilities are provided for the program to start a chain of operations with a single Start I/O command. This method of operation is called command chaining and is initiated by turning on the chain command bit (bit 1 of the second CCW word). If command chaining is specified, the selector channel fetches a new CCW, specifying a new I/O operation upon receipt of the device end signal for the current operation.

Chaining takes place only between CCW's located in successive three-word locations in main storage. It proceeds in an ascending order of addresses; that is, the address of the new CCW is obtained by adding 3 to the address of the current CCW.

Two chains of CCW's located in noncontiguous main storage areas can be coupled for chaining purposes by a Transfer-in-Channel command.

All CCW's in a chain apply to the 2311 specified by the modifier bits of the original Start I/O command.

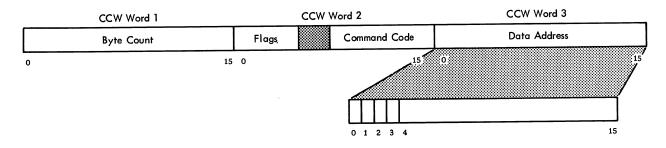
Command chaining takes place and the new operation is initiated only if no unusual conditions have been detected in the current operation. Occurrence of a unit check, unit exception, control unit end, busy, or incorrect length (when the SLI bit is 0) cause the chain of operations to be terminated. The new CCW in this case is not fetched and the status associated with the current operation causes the CSW to be stored via program interruption.

An exception to sequential chaining of CCW's occurs when the I/O device presents the status modifier condition with the device end signal. The combination of status modifier and device end bits causes the channel to fetch and chain to a CCW whose main storage location is six addresses higher than that of the current CCW.

Programming Note: Command chaining makes it possible for the program to transfer multiple blocks of data by means of a single Start I/O. In conjunction with the status modifier condition, command chaining also permits the channel to modify the normal sequence of operations in response to signals provided by the 2311.

The time required to perform command chaining is 12 microseconds on a 2 μ sec System. This speed is based on worst-case conditions and assumes that no higher priority cycle-steal request is pending.

During the execution of a chain of operations, the channel status word pertains to the last operation executed or attempted.



Bit	Indication
0	Used only with 65,536 word main storage
1	Used with 24,576 word main storage and above
2	Used with 16,384 word main storage and above
3	Used with 8, 192 word main storage and above
4-15	Used with bits 0-3 (if applicable) and specify the address of the first byte of data in an input or output data field. For Transfer in Channel commands, contains the address of a new CCW

Figure 79. Data Address (CCW Word 3)

Command chaining cannot be used in conjunction with data chaining as the latter takes precedence.

Data Chaining

Data transfers between main storage and the 2311's may be chained. Data chaining permits blocks of data to be transferred to or from noncontiguous areas of main storage. When data chaining is specified (bit 0 of the second CCW word on), the selector channel fetches a new CCW upon completion of data transfer for the current CCW. Unless the command code specifies Transfer-in-Channel, the contents of the command code field of the new CCW are ignored.

Data chaining may be used to rearrange data as it is transferred. It may also be used in conjunction with the skipping function to enable the program to place selected portions of a block of data into main storage.

Programming Note: If the device sends channel end after exhausting the count of the current CCW, but before transferring any data to or from the storage area designated by the new CCW, the CSW associated with the termination identifies the new CCW.

If programming errors are detected in the new CCW or during its fetching, a program check condition is generated and the channel terminates the operation, which results in an overrun condition from the 2841 and requires a Halt I/O condition to clear.

If the device signals channel end before transferring any data designated by the new CCW, incorrect length is indicated in the CSW.

Unless the address of the new CCW is invalid or programming errors are detected in an intervening Transfer-in-Channel command, the contents of the CSW pertains to the new CCW.

Attempting to read into a protected area is detected upon fetching the CCW and indicated with a program check bit and a channel data check bit in the CSW.

Self-Describing Blocks

When a channel program data-chains to a CCW placed in main storage by the CCW specifying data chaining, the input block is said to be self-describing. A self-describing block contains one or more CCW's that specify storage locations and counts for subsequent data in the same input block.

Use of self-describing blocks is equivalent to use of unchecked data. An I/O data transfer malfunction that affects the validity of a block of data is not signaled until the completion of the transfer. The error condition normally does not prematurely terminate or otherwise affect the execution of the

operation. Thus, there is no assurance that a CCW read as valid data is valid until the operation is complete.

If a CCW in error is read, placement of data into wrong locations in main storage could result in destruction of data. If the error in the CCW is such as to cause subsequent command chaining, it may be possible to chain to a write command; the result could be destruction of information on the 2311.

Skip

Skipping suppresses transfer of data to main storage during read and sense operations. Skipping is initiated by setting the skip flag (bit 4 of the second CCW word) to 1.

The skip function is used only in conjunction with data chaining and affects only the handling of data by the channel. The operation at the 2311 proceeds normally, and data is transferred to the channel. The channel keeps updating the count but does not place the data in main storage. If the chain data flag is on, a new CCW is fetched when the count reaches 0. In the case of data chaining, normal operation is resumed if the skip flag in the new CCW is 0.

Programming Note: Skipping, when combined with data chaining, permits the program to place selected portions of a block of data into main storage from the 2311. Skipping should only be used in conjunction with data chaining.

CHANNEL STATUS WORD

All I/O operations using the selector channel are initiated by a Start I/O command. The operation specified by the Start I/O is initiated only when the selector channel, control unit, and I/O device are available. Conditions indicating availability are contained in the channel status word (CSW). The CSW is formed, or parts of it replaced, in the process of I/O interruptions and during the execution of IOCC's.

The CSW consists of four 16-bit words.

1st Selector Channel Status

2nd Unit Address - Status

3rd Command Address

4th Count

An IOCC Sense Device command is used to transfer each word into the accumulator. Which word of the CSW that is transferred is determined by the setting of modifier bits 13 and 14 of the IOCC.

Selector Channel Status (CSW Word 1)

A Sense Device command with modifier bits 13 and 14 set to 00 causes the selector channel status portion of the CSW to be placed into the accumulator. The significance of each bit of this word is shown in Figure 80.

Channel status is updated as it occurs and may be sensed by the program at any time. Whether a bit will be on (1) or off (0) is determined by conditions existing at the channel, control unit, or device as a result of processing an I/O instruction.

Not Operational, Bit 0: Not operational occurs when a control unit fails to recognize a unit address specified by an IOCC. This bit is turned on (1) when the addressed control unit is not attached to the system or the device portion of the unit address exceeds the number that the control unit is designed to handle. This condition causes an interrupt when it is detected by the channel. This bit is reset by modifier bit 15 of the Sense Device IOCC on (1).

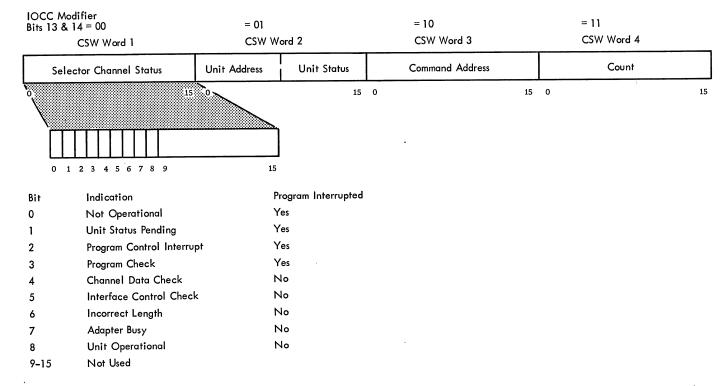
Unit Status Pending, Bit 1: Unit status pending occurs when a control unit or an I/O device has presented its ending status, stacked status, busy status, or unusual condition status to the channel. The channel is waiting for a sense device operation to interrogate this status and end the unit-statuspending condition. This condition causes an interrupt when it is detected by the channel and can only be reset by a Sense Device command with modifier bit 15 on.

Program Control Interrupt, Bit 2: Program control interrupt is on when the channel has fetched a CCW containing a PCI flag. This bit is reset by modifier bit 15 on in the Sense Device IOCC.

Program Check, Bit 3: A program check is caused by either of the following conditions:

- Invalid function code in the IOCC. When area code 18 (selector channel) is used, only the following function codes are correct: 011, 100, 101, and 111
- 2. A parity error occurred while fetching the IOCC or CCW.
- 3. The channel attempted to read data into protected storage.

The program check condition inhibits cycle stealing and causes a program interrupt. The



Note: Bits 0, 2, and 3 will only be reset if modifier bit 15 of the Sense Device IOCC is on (1). Bit 1 can only be reset if a Sense Device with modifier bits 13, 14, and 15 set to 011 is executed. (Sense Device specifying CSW word 2 with the reset bit on)

Figure 80. Selector Channel Status (CSW Word 1)

program check bit is reset by modifier bit 15 on in the Sense Device IOCC.

Channel Data Check, Bit 4: Channel data check indicates that the channel has detected a parity error in the information transferred, or a read or sense operation attempted to transfer data to a protected storage area designated by the CCW. If storage is unprotected, the byte of data causing the data check is stored in main storage and the channel places 0's in the remaining storage locations. Data protected by the storage protect bit is not changed. The current operation continues until the count as specified in the CCW is exhausted. If command chaining is in effect at the time of the data check, the following command is not executed. The program is interrupted when the device presents channel end.

Interface Control Check, Bit 5: This bit on indicates the channel has detected an invalid signal on the I/O interface. This check indicates a malfunction in the I/O device caused by either of the following conditions:

- 1. A device responded with an address other than the address specified by the channel during initiation of the operation.
- 2. An "in" tag signal from a device occurred simultaneously with another "in" tag signal.

Detection of an interface control check by the channel causes the current operation to be terminated immediately.

Incorrect Length, Bit 6: Incorrect length occurs when the number of bytes, as designated by the byte count in the CCW, is not equal to the number of bytes requested or offered by the I/O device. Incorrect length is indicated for one of the following reasons:

- 1. Long block on input: During a read or sense operation, the I/O device attempted to transfer one or more bytes to main storage after the byte count reduced to zero.
- 2. Short block on input: The number of bytes transferred during a read or sense operation is insufficient to reduce the byte count to zero.
- 3. Short block on output: The I/O device terminated a write or control operation without the byte count being reduced to zero.
- 4. Long block on output: During a write or control operation, the I/O device requested another byte from the channel after the CCW count went to zero.

Presence of the incorrect length condition suppresses chaining unless the SLI flag is on.

Adapter Busy, Bit 7: Adapter busy occurs when the selector channel is executing a previous IOCC instruction or servicing a control unit or device request. A Start I/O is ignored, however, a Halt I/O or Sense Device is executed.

Unit Operational, Bit 8: Unit operational occurs when the channel is executing a Start I/O and the data transfer portion of the command has commenced. This bit is set only by commands requiring data transfer.

Test I/O and immediate commands do not set this bit.

Unit Address - Status (CSW Word 2)

An IOCC Sense Device instruction with modifier bits 13 and 14 set to 01 places the unit address-status portion of the CSW into the accumulator. The significance of the bits in this word is shown in Figure 81.

Unit address-status is only valid when the unit status pending bit (bit 1 on the first CSW word) is on.

The first eight bits of the second word of the CSW identify the control unit and I/O device specified in the last I/O operation executed or rejected.

The last eight bits (unit status) of the second word of the CSW identify the conditions detected in the control unit and the I/O device. The unit status conditions are sent over the I/O interface from the control unit or I/O device. The channel does not modify these bits, and they appear in the CSW as received from the interface.

Attention, Bit 8: Not used by 2841.

Status Modifier, Bit 9: Status modifier is generated by the I/O device when the normal sequence of commands has to be modified or when the control unit, during initial selection sequence, detects that it cannot execute the command or instructions as specified.

When the status modifier bit appears in the CSW with the busy bit, it indicates that the busy condition pertains to the control unit associated with the addressed I/O device. The control unit appears busy when it is executing a type of operation, or is in a state, that precludes the acceptance of any command. A typical example is the Seek command, which causes the control unit to remain busy after it has signaled device end.

Once the execution of a command has started, the status modifier indication can occur only with device end. If command chaining is specified in the

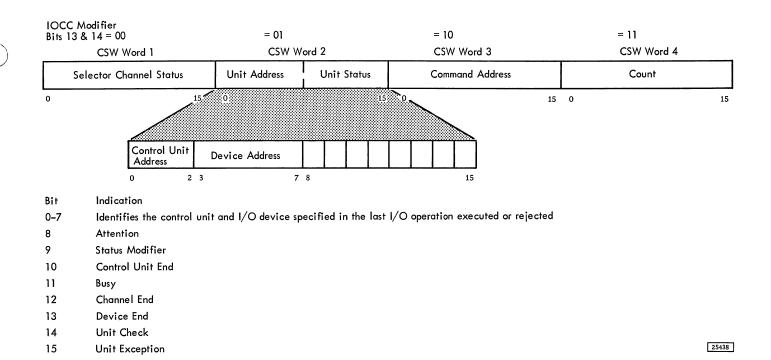


Figure 81. Unit Address - Status (CSW Word 2)

current CCW when device end and status modifier are indicated, the channel will fetch and chain to the CCW whose main storage location is six higher than that of the current CCW. Since the next CCW in a chain is normally taken from a storage location three storage locations higher than the current CCW, the status modifier condition effectively provides a branching capability for the program.

Control Unit End, Bit 10: The control unit end condition is provided only by control units shared by I/O devices, and only when one or both of the following conditions occur:

- 1. The control unit was interrogated while executing an operation. The control unit is considered to be interrogated when, during a previous initial selection sequence, the control unit responded with busy and status modifier in the status byte.
- 2. The control unit detected an unusual condition while busy and after channel end was accepted by the channel.

If the control unit remains busy executing an operation after signaling channel end, but is not interrogated by the program and does not detect any unusual conditions, control unit end is not generated.

When the busy state of the control unit is temporary, control unit end is included with busy and status modifier in response to interrogation, even though the control unit is not yet free. The busy condition is considered temporary if its duration is less than two milliseconds.

The I/O device address associated with the control unit end is determined as follows:

- 1. If control unit end is to be presented with channel end and/or device end, the address of the selected device is used.
- 2. If control unit end is generated without channel end or device end, and the status is presented during a control-unit-initiated selection sequence, the I/O device address may be any legitimate address associated with the control unit. (A legitimate address is any address the control unit is

- capable of recognizing, regardless of whether the I/O device is actually attached.)
- 3. If control unit end is to be presented during an initial selection sequence, the device address is the same as the device address specified for the operation.

A pending control unit end causes the control unit to appear busy, and new instructions or commands are not initiated.

Busy, Bit 11: Busy can occur only during an initial selection sequence. It indicates that the I/O device or the control unit cannot execute the command because a previously initiated operation is being executed or because status conditions exist. (An operation is being executed from the time initial status is accepted until device end is accepted.) Status conditions, if any, accompany the busy condition.

If the busy condition applies to the control unit, the busy bit is accompanied by status modifier.

Channel End, Bit 12: Channel end is caused by the completion of the portion of an I/O operation involving transfer of data, if any, or control information, between the I/O device and the channel.

The exact time during an I/O operation when channel end is generated depends on the operation and the type of device. Channel end is usually generated after the control information is transferred to the control unit. For data transfer operations, such as writing, channel end is generated when the block of data has been written. Operations that do not involve data transfer can provide channel end during the initial selection sequence.

When command chaining is specified, only the channel end following the last operation of the chain is made available to the program. Channel end is not made available to the program when a chain of commands is prematurely terminated because of an unusual condition indicated with control unit end or device end.

Each I/O operation causes one channel end signal to be generated. The channel end condition is not generated unless the operation is initiated.

Device End, Bit 13: Device end is caused by the completion of an I/O operation at the device or by manually changing the device from a not ready state to a ready state. The device end condition indicates that the I/O device has completed the current operation.

The device end condition associated with I/O operations can occur simultaneously with channel end or later. In case of data transfer operations,

the device terminates the operation at the time channel end is generated, and both device end and channel end appear together. For control operations, device end is generated at the completion of the operation.

When command chaining is specified, the receipt of device end without unusual conditions causes the channel to initiate a new I/O operation.

Each I/O operation causes only one device end condition. Device end is not generated unless the operation is initiated.

Unit Check, Bit 14: Unit check indicates that the I/O device or control unit requires programming or manual intervention. Unit check does not necessarily indicate an error condition. The conditions causing a unit check are detailed by data available to a sense command, which would normally follow the acceptance of unit check status. The unit check bit provides a summary indication of the conditions identified by sense data.

The unit check condition is generated when an error is detected during execution of a command, or during some activity associated with an I/O operation. Unless the error condition pertains to the activities initiated by a command and is of immediate significance to the program, the condition does not cause the program to be altered after device end is cleared.

When the device is not executing an operation and does not have a pending interrupt condition, equipment malfunction may cause the I/O device to become not ready. In this event, unit check is signaled to the program the next time the device is selected.

If, during the initial selection sequence, the I/O device detects that the command cannot be executed, unit check is presented to the channel without channel end, control unit end, or device end. This condition indicates that no action has been taken at the device in response to the command. If the condition precluding proper execution of the operation occurs after execution has begun, unit check is accompanied by channel end, control unit end, or device end, depending on when the condition is detected.

Invalid command codes or errors in command code parity do not cause unit check if the I/O device is busy or holding status at the time of selection. Under these circumstances, the device responds by providing the busy bit and indicating the pending status. Command code validity is ignored.

Termination of an operation with the unit check indication causes command chaining to be suppressed.

Unit Exception, Bit 15: Unit exception is caused when the I/O device detects an end of file condition. It results from a data length of zero being detected in the count area of a record.

Termination of an operation with a unit exception condition causes command chaining to be suppressed.

Command Address (CSW Word 3)

An IOCC Sense Device command with modifier bits 13 and 14 set to 10 places the command address portion of the CSW into the accumulator. The significance of the bits in this word is shown in Figure 82.

The command address can be sensed by the program at any time. The command address is an address three higher than the address of the CCW being executed or just completed.

Count (CSW Word 4)

An IOCC Sense Device command with modifier bits 13 and 14 set to 11 places the count portion of the CSW into the accumulator. The significance of the bits in this word is shown in Figure 83.

The count may only be sensed when the adapter busy bit (bit 7 of the 1st word) is on, or when no channel-initiated operation is in progress. If the count is sensed at any other time, the information contained in the count is unpredictable.

The count is expressed in 2's complement form plus 1. For example, a byte count of 0007 hexadecimal is expressed as FFFA.

The count is not reset by modifier bit 15 of the Sense Device IOCC.

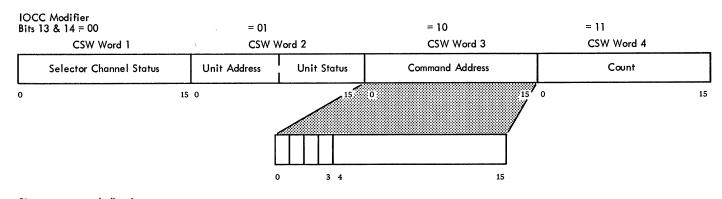
INITIATION OF SELECTOR CHANNEL OPERATIONS

The operation specified by a Start I/O is initiated only when the channel, control unit, and device are in the available state. The P-C program must interrogate the channel status to determine that the channel is not busy before initiating a Start I/O operation. If a Start I/O is attempted while the channel is busy, it is ignored. No indication is given to the program that the command was ignored. If the channel is available, the Start I/O is accepted by the channel and the status of the control unit and I/O device are examined.

If the channel is available and either the control unit or I/O device is busy, the control unit presents the busy status to the channel, and the command is not executed. The channel interrupts the program with the unit status pending bit in the CSW. The program must then execute a Sense Device with modifier bits 13 and 14 set to 01 to obtain the unit status. The status pending bit is not reset until the unit status is sensed with IOCC modifier, bit 15 on.

If the channel is available, and either the control unit or the device addressed is not operational, the address is not recognized during the initial selection. In this case, the channel interrupts the program with the not operational bit in the CSW.

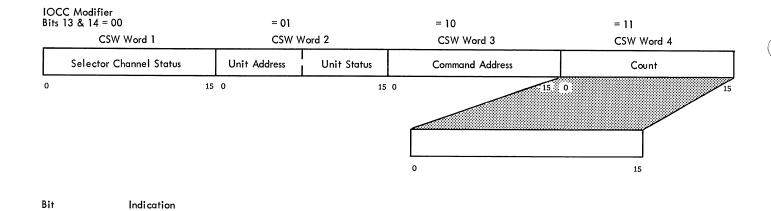
If the channel, control unit, and device are available, the operation specified by the Start I/O is executed.



Bit	Indication
0	Used only with 65,536 word main storage
1	Used with 24,576 word main storage and above
2	Used with 16,384 word main storage and above
3	Used with 8, 192 word main storage and above
4-15	Used with bits 0–3 (if applicable) and specifies an address three higher than the address of the last CCW used

30207

Figure 82. Command Address (CSW Word 3)



Forms the residual count for the last CCW used. The count is expressed in two's complement form plus one

Figure 83. Count (CSW Word 4)

0-15

TERMINATION OF SELECTOR CHANNEL OPERATIONS

Normally, an I/O operation at the channel lasts until the device signals channel end. The channel end condition can be signaled during the sequence initiating the operation or later. When the channel detects equipment malfunctioning or a system reset is performed, the channel disconnects the device without receiving channel end.

Termination at Operation Initiation

A data transfer operation is initiated at the I/O device only when no programming or equipment errors are detected by the channel, and the device responds with zero status during the initiation of the command. When the channel detects, or the device signals any unusual condition during the initiation of an operation, and channel end is off, the command is rejected.

If a command is rejected during the execution of a Start I/O, the device is not started, no interrupt conditions are generated, and the channel is not tied up beyond the initiation sequence. The conditions that precluded the initiation are detailed in the channel status and unit address-status portion of the CSW.

Unless the command was rejected because the I/O device was not operational or busy, the device is immediately available for the initiation of another operation.

When an unusual condition causes a command to be rejected during initiation of an I/O operation by command chaining, an interruption condition is generated and the device is not available until the condition is cleared. The unusual conditions are indicated

to the program by means of the corresponding status bits in the CSW. The new operation of the I/O device is not started.

25440

Termination Without Data Transfer

Immediate Operations

Instead of accepting or rejecting a command, the I/O device can signal the channel end condition immediately upon receipt of the command code. An I/O operation causing the channel end to be signaled during the initiation sequence is called an "immediate operation."

If command chaining is not specified, receipt of channel end causes the unit status pending bit to be set in the CSW. (The CSW also contains the channel end bit and any other indications provided by the channel or I/O device.) Unit status pending causes the channel to interrupt the program. The I/O operation, however, is initiated and the channel immediately made available to the program. If channel end is not accompanied by device end the device remains busy. Device end, when subsequently provided by the device, causes an interruption condition to be generated.

When command chaining is specified after an immediate operation and no unusual conditions have been detected during the execution of the command, no interruption condition is generated. The subsequent commands in the chain are handled normally, and the channel end condition for the last operation in the chain causes the program to be interrupted.

Program check or incorrect length is not set, and command chaining is not suppressed because of the contents of the CCW byte count field for immediate command operations.

Pending Interruption

When a Start I/O operation addresses an I/O device containing a pending interruption due to device end or attention, or a control unit containing a pending channel end or control unit end for the device, the channel status and unit address-status portions of the CSW are set. The unit status field contains the busy bit, identifies the interruption, and may contain other bits provided by the control unit or I/O device. The interruption condition in the unit status is cleared and the unit status pending bit is set in the channel status field. The remainder of the channel status field contains 0's. The unit status pending bit on causes the channel to interrupt the program.

The operation is not initiated and the channel is not tied up beyond the initiation sequence. The channel and device are immediately available for the initiation of another operation.

Device or Control Unit Busy

When a Start I/O operation addresses an I/O device or control unit that is busy, or a control unit which has a pending channel end or control unit end for a device other than the one addressed, the channel status and unit address-status portion of the CSW are set. The CSW unit status field contains the busy bit, or if the control unit is busy, the busy and status modifier bits. The channel status field contains 0's, except for the unit status pending bit, which will cause a program interruption.

The operation is not initiated and the channel is not tied up beyond the initiation sequence after unit status is sensed.

Termination with Data Transfer

For operations involving data transfer, either the channel or I/O device can control the timing of the channel end condition. If command chaining is not specified or chaining is suppressed because of unusual conditions, the channel end condition causes operation at the channel to be terminated. The status bits in the associated CSW indicate channel end and unusual conditions, if any.

The I/O device can signal channel end any time after the initiation of the operation. Channel end may occur prior to any actual data transfer.

The channel signals the device to terminate data transfer whenever any of the following conditions occur:

 The storage areas specified for the operation are exhausted or filled. This condition occurs

- when the channel has stepped the count in the last CCW associated with the operation to 0. A count of 0 indicates that the channel has transferred all information specified by the program.
- 2. A program or unit check condition is detected.

 This condition is due to errors and causes premature termination of the operation.
- 3. An IOCC with a function code specifying Halt I/O is executed by the program. Execution of Halt I/O automatically disconnects the device from the channel.

The channel suppresses initiation of an I/O operation when the data address of the first CCW associated with the operation exceeds the addressing capacity of main storage. When the initial data address is invalid, no data is transferred during the operation, and the device is signaled to terminate the operation. If the initial data address is invalid, the operation is terminated before the recording medium has been advanced. However, since the operation has been initiated, the device provides channel end.

If command chaining is specified, the device executing the operation remains connected to the channel until the last command of the chain has been executed. Any unusual conditions cause command chaining to be suppressed and a terminating condition generated. The unusual conditions can be detected by the channel or the I/O device. When the channel is aware of the unusual conditions by the time the channel end signal for the operation is received, the chain is terminated as if the operation in which the unusual condition occurred were the last operation in the chain.

Termination with Halt I/O

Initiation of a Halt I/O instruction terminates the current I/O operation at the addressed selector channel, control unit, or I/O device. If the channel is not busy, modifier bits 8 to 15 of the IOCC identify the control unit and I/O device to which the Halt I/O applies.

When the channel is available, and the control unit is busy, the addressed device is signaled to terminate the current operation. Halt I/O does not affect the state of the control unit when both channel and control unit are available.

If Halt I/O is issued when the channel is executing a data transfer, the data transfer is terminated and the device performing the operation is immediately disconnected from the channel. In this case, modifier bits 8 to 15 of the IOCC are ignored.

The termination of an operation as a result of a Halt I/O causes the channel and control unit to be

placed in the interruption pending state. When the channel is in the interruption pending state or available, and the control unit is in the interruption pending state, execution of Halt I/O does not affect the state of either the channel or control unit.

The CSW set during Halt I/O pertains only to the execution of Halt I/O. It does not describe under what conditions the I/O operation at the addressed device is terminated. If the addressed device has been selected and signaled to terminate the current operation, the CSW contains 0's in the unit status field unless an equipment error is detected. If an equipment error is detected, the status bits in the CSW identify the error condition. The state of the channel and the progress of the I/O operation are unpredictable.

When Halt I/O causes a data transfer operation to be terminated, the control unit associated with the operation remains busy until the data handling portion of the operation in the control unit is terminated. Termination of data handling in the control unit is signaled by channel end. Channel end may occur at the normal time or earlier or later, depending upon the operation and type of device.

If the control unit is shared, all devices attached to the control unit appear busy until the channel end is accepted by the P-C. The I/O device executing the terminated operation remains busy until termination of the operation. At this time the device signals the channel with device end.

The System/360 Adapter (located within the 1826) permits communication between the 1800 P-C and the System/360. Each system regards the other as an I/O device capable of requesting service on a random basis. The System/360 Adapter is functionally equivalent to the corresponding System/360 device, the channel-to-channel adapter.

The channel provides the ability to transfer blocks of data and/or programs at rates up to 250 kb (kilobytes) between the System/360 and the 1800 system.

Exercise caution when powering the 1800 system up or down to ensure that the System/360 Channel adapter is off-line and that the off-line switch is in the bypass/gated position. Failure to do so before the power transition will force channel failures.

Addressing

The System/360 Adapter has two device addresses, one of which responds to the System/360 and one which responds to the 1800. The System/360 address is assigned at installation time. The 1800 address is fixed, area code of 01101. Each assignment conforms to the requirements of the two systems' channels.

Mode of Operation

The System/360 Adapter acts as a burst mode control unit on the System/360 channel and operates on a Data Channel with the 1800.

Data is transferred to or from the 1800, two 8-bit bytes at a time; data transfer to or from the System/360 channel occurs one 8-bit byte at a time. An 18-bit (16 data bits plus 2 parity bits) buffer register is provided for serializing and deserializing the data bytes. The left-hand byte of the buffer, corresponding to the more significant byte of the 1800 word, is loaded or transferred first over the System/360 channel.

The priority of the System/360 Adapter is selected for the 1800 by assigning a particular interrupt level and a particular Data Channel priority to the device. Control unit priority for the System/360 is governed by its position on the channel as defined in the System Reference Library publication, IBM System/360 Principles of Operation, Form A22-6821.

COMMANDS

The System/360 Adapter decodes and responds to seven System/360 commands and five 1800 commands. (See Table 7.)

The Read, Read Backward, Write, and Control command bytes, including modifier bits, of the System/360 and the Initialize Read or Initialize Write control words of the 1800, after being presented to the idle Adapter, are available to the programmer of the other system by use of their respective Sense commands.

The M-bit being on in the System/360 Read or Write commands (Table 7) will suppress the 1800 interrupt normally caused by a System/360 command when loaded into the buffer. For example, the program for a System/360 initiated transfer may involve first, a Control command which identifies the desired operation via the modifier bits, then a Read or Write to complete the operation. These may or may not be chained. Both commands could be accepted by the Adapter buffer, and hence cause two interrupts in the 1800 system. The second interrupt (from the accepted Read or Write command) would be caused if the 1800 system response to the indicated operation (coded in the Control modifier bits) were delayed, either by the interrupt being masked, or perhaps a required intervening disk storage Seek operation. Thus, at the time the command byte following the Control arrives at the Adapter from the System/360, the Adapter would be in an idle condition and would latch the second command in the Adapter buffer. This operation normally causes an 1800 system interrupt to establish the presence of a command byte. The M-bit modifier then, is provided to suppress the interrupt for a Read or Write which could cause unnecessary interrupts in an exchange sequence such as described above.

The R-bit being on in the 1800 Sense DSW command (Table 7), will reset the interrupting DSW bit.

Table 7. Commands

1800 Sy	stem Commands	,	System/360	Commands
Func	Mod.			
101 110 111 111 011 100	XXXXXXX XXXXXXX 0 XXXXXXR 1 XXXXXXX XXXXXXXX XXXXXXXX	Initialize Write Initialize Read Sense DSW Sense Word Count *Sense Interrupt Level Control (Reset)	Test I/O Write Read Control Sense Read Backward No Operation	XXXX0000 XXXXXM01 XXXXXX111 XXXX0100 XXXX1100 XXXXX011

Area Code not required to execute

17230B

Note: The interrupt due to the Read Backward command cannot be suppressed.

DEVICE STATUS

System/360 Status Byte

The System/360 Adapter presents the following device status information to the System/360:

Status Condition	System/360 Status Byte Bit Position
A	
Attention	0
Busy	3
Channel End	4
Device End	5

In addition, the System/360 channel develops a status byte. The definition of these channel status bits are as defined in the Systems Reference Library publication, IBM System/360 Principles of Operation, Form A22-6821.

Attention: Indicates the condition, if on, that a prior Read or Write command function has been issued from the 1800 but that the System/360 has not issued the required complementary command.

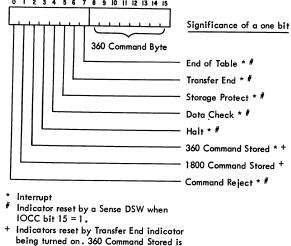
Busy: The busy indication is off when the System/ 360 Adapter is idle. Busy on indicates that the device has been selected by the System/360 and an operation is pending, a transfer is in progress, or ending status has not been accepted.

Channel End: Presented to the System/360 during initial selection sequence for Control or No Op. or with Device End during the ending sequence for all other Start I/O (SIO) commands.

Device End: Presented to the System/360 during the initial selection sequence for No Op, after an 1800 Sense DSW (with bit 15 on) command response to Control, or at the end of the data transfer for all other SIO commands.

1800 Device Status Word

The System/360 Adapter presents the following status information to a Sense DSW command from the 1800:



being turned on . 360 Command Stored is reset by Sense DSW (IOCC bit 15 = 1) only when command stored is a Control command.

23408

Command Reject: This bit on indicates that the System/360 Adapter refused an 1800 command for one of the following reasons:

- Invalid Op Code.
- An Initialize Read or Initialize Write was issued before a previous Initialize Read or Initialize Write had been cleared.
- An Initialize Read was issued after the System/ 360 had issued a Read, Read Backward, or Control command.
- An Initialize Write was sent after the System/ 360 had issued a Write or Control command.

This bit causes an 1800 interrupt and is reset after an 1800 Sense DSW with bit 15 on. If a Command Reject occurs when no 1800 command is stored, the word count register is reset to its maximum value. Such a reset can occur when Transfer End has been issued but not yet accepted.

1800 Command Stored: This bit is on whenever the System/360 Adapter has accepted an Initialize Read or Initialize Write from the 1800. It is reset when Transfer End occurs.

360 Command Stored: This bit on indicates that the System/360 has issued a Read, Read Backward, Write, or Control Command to the Adapter.

If the command is Read or Write, this bit will cause an interrupt in the 1800 unless suppressed by the System/360 command M-bit being on or by a complementary 1800 command waiting in the Adapter. An 1800 Sense DSW with bit 15 on will reset the interrupt. Transfer End resets the indicator bit.

If the command is Read Backward the response is identical to Read, as described above, except that the interrupt cannot be suppressed with the command M bit.

If the command is Control, this bit forces an interrupt in the 1800. An 1800 Sense DSW with bit 15 on will reset the interrupt and the indicator bit.

The 360 Command Stored indicator can be on at the same time as Transfer End, indicating that a new operation has been initiated by the System/360.

Halt: This bit causes an interrupt if the System/360 stops data transfer either with a normal stop or an interface disconnect sequence. Bit 6 (Transfer End) will also be on. This bit is reset after an 1800 Sense DSW with bit 15 is on.

<u>Data Check:</u> This bit on indicates that the 1800 detected a parity error during a cycle steal or the Adapter detected a System/360 bus out parity error. The Data Check causes an interrupt in the 1800 and is reset by an 1800 Sense DSW with bit 15 on.

If the error is detected during the first cycle steal of the operation (load word count cycle) and there is no complementary System/360 command stored, the Adapter is reset and the 1800 can reinitialize the data transfer operation.

If a parity error is detected during the first cycle steal operation (load word count cycle) and there is a complementary System/360 command stored or the parity error is detected during any subsequent cycle of the operation, an immediate ending procedure is initiated. The Adapter issues Device End and Channel End to the System/360, and Data Check and Transfer End to the 1800.

If the 1800 detects incorrect parity during the execution of the XIO command, the Adapter ignores the command and initiates no interrupts to either the 1800 or the System/360. This error causes an 1800 internal interrupt.

Storage Protect: This bit on indicates that the System/360 attempted to store data in a protected area in 1800 core storage on a 360 Write/1800 Read data cycle. This causes the System/360 Adapter to initiate an ending procedure, sending Channel End and Device End to the System/360, and Storage Protect

and Transfer End to the 1800. An interrupt is given to the 1800. This bit is reset by an 1800 Sense DSW with bit 15 on.

<u>Transfer End:</u> This bit on indicates that no additional data is to be transferred. This condition can be caused by any of the following conditions:

- The 1800 Word Count goes to zero and no chaining is indicated.
- 2. The System/360 byte count has gone to zero.
- 3. The System/360 issues a Halt I/O instruction or executes an interface disconnect sequence.
- 4. Parity error is detected.
- 5. A storage protect violation has occurred.

This bit is reset by an 1800 Sense DSW with bit 15 on. (An 1800 Initialize Read or Write is rejected if the Transfer End status is on.)

End of Table: This bit will be turned on (if requested by the Scan Control bits) causing an interrupt, when the 1800 word count in the System/360 Adapter goes to zero. This bit is reset by an 1800 Sense DSW with bit 15 on.

360 Command Byte: If Bit 2 is on (360 Command stored) and Bit 1 is off (no 1800 command stored), bits 8 - 15 contain the issued 360 command byte. (See Table 8.) Note: These bits can be assumed to be zero only after a reset.

PROGRAMMED OPERATION

The System/360 Adapter performs with respect to the System/360 channel as described in the System Reference Library publication <u>IBM System/360</u> <u>Principles of Operation</u> with the exception described below.

The System/360 Sense command stores in core storage at the address specified in the CCW up to two bytes of sense data under control of the byte count. The first byte contains the area and function of the 1800 I/O control word from the high order byte of the System/360 Adapter buffer. The next byte, from the low order buffer byte, contains the modifier bits of the I/O control word. All valid command codes from the System/360 are acceptable to the System/360 Adapter. The System/360 adapter rejects undefined command functions from the 1800 and identifies this occurrence by the Command Reject status bit presented in the device status word.

The following descriptions of System/360 I/O commands include statements regarding the resulting condition code. For the definition and application of these condition codes refer to the System Reference Library publication IBM System/360 Principles of Operation.

CONTROL (SYSTEM/360)

Control as used in the System/360 Adapter is always an immediate command. This means that Channel End status is sent to the System/360 in response to the initial selection (if the command is accepted), thus freeing the channel if a chain flag is not present. A Control from the System/360 may be rejected because the 1800 had previously commanded the System/360 Adapter with an Initialize Read or Write.

The modifier bits in the Control command byte may be used to communicate the particular type of transfer requested by the System/360. The Control command is normally chained to a subsequent Read or Write command, depending on the operation necessary to complete the transfer.

Control to Idle Adapter: The System/360 initiated the Control command. The complete command byte, including modifiers, is latched in the Adapter. The Adapter responds to initial selection with Channel End status, thus freeing the System/360 channel, and initiates an interrupt in the 1800. The condition code in the System/360 resulting from the command is status stored (1). The 1800, when interrupted, can accept the request by executing an XIO Sense DSW command to the Adapter. The XIO Sense DSW command loads into the 1800 accumulator the Device Status Word (DSW) containing the System/360 command byte from the buffer. A Device End status is then sent to the System/360.

Control to a Busy Adapter: A Control from the System/360 may be Busy rejected by one of three conditions:

- 1. The Control could be issued by the System/360 before a previous Control from the System/360 had been cleared. The Adapter response would be Busy status causing a condition code of busy (2) for the SIO Control.
- 2. The Control could be issued by the System/360 after a previous Control had been cleared but before the Device End had been accepted by the System/360. The response would be Busy and Device End status causing a condition code of status stored (1) for the SIO Control. This would clear the Device End from the Adapter and leave it idle.
- 3. The Control might be issued by the System/360 after the 1800 had issued an Initialize Read or Initialize Write command to the Adapter. The Adapter would respond with Busy and Attention

status to the System/360 causing a condition code of status stored (1) for the SIO Control. The Attention, after being accepted in this way, would no longer attempt to interrupt the System/360. If another command, such as Control, were issued from the System/360, the response would still be Busy and Attention.

SENSE (SYSTEM/360)

The Sense command is the normal response to Attention status (an 1800 initiated transfer). The initial status will be zero and ending status will be Device End and Channel End. If the Adapter contains an uncomplemented 1800 command, the ending status will also contain Attention. When a Sense command is received by the Adapter, one or two 8-bit bytes are transmitted to the System/360. The sense bytes consist of the contents of the System/360 Adapter buffer latches.

The Sense command data presented under alternative conditions is:

	High-Order Buffer	Low-Order Buffer
Condition	BYTE 1	BYTE 2
Adapter Idle	Undefined	Undefined
1800 Previously		
Initialize Read	Area/Function	Modifier
Initialize Write	Area/Function	Modifier
Control	Zero	Zero

17446 A

The only exception to the above is encountered when the System/360 issues a Sense command to the Adapter before a previous Control from the System/360 had been cleared. If the Control had not been answered by a Sense from the 1800, then the SIO Sense command would receive Busy status, condition code 2. If the Control had been answered, but the Device End had not been taken, or had been stacked, the Sense command would receive Busy and Device End status causing a condition code 1, status stored. This would clear the Device End from the Adapter and leave it idle.

READ OR READ BACKWARD (SYSTEM/360)

The Adapter recognizes no difference between Read and Read Backward from the System/360. In both

cases, the primary function of the Adapter is the transmission of data bytes to the System/360 from the 1800.

Read to an Idle Adapter: When the Read command is issued to an idle Adapter, the System/360 receives zero status response (condition code 0, operation initiated) and is then held up until the 1800 responds with an Initialize Write command. Unless suppressed with the M bit, a interrupt is set up to signal the 1800 that an operation is waiting. The complete Read command byte is latched in the Adapter buffer and is available to a Sense DSW command from the 1800.

Read to a Waiting Initialize Write: If a Read, issued by the System/360, encounters a previously issued Initialize Write from the 1800, both operations are performed. The System/360 receives zero initial status (condition code 0, operation initiated) whether the Attention is accepted or not. The operation continues until the System/360 byte count is zeroed, the Adapter word count is zeroed, or an error condition is detected. If neither channel is data chaining, status containing Channel End and Device End is issued to the System/360. The acceptance of the status by the System/360 frees the Adapter and returns it to idle.

Read to a Busy Adapter: There are three Busy responses to a Read command:

- Busy status alone responds to the Read command if the System/360 had previously issued a Control command that was still in the Adapter. Condition code 2, busy.
- 2. Busy and Device End status is the response to a Read command if a previously issued Control command was cleared but the Device End had not been accepted. This clears the Device End and leaves the Adapter idle. Condition code 1, status stored.
- 3. Busy and Attention status is the response to a Read command from the System/360 if the 1800 had previously issued an Initialize Read. If the Attention was not previously accepted by the System/360, this clears it as an interrupting condition, although it would still appear as a response to another Read until the previously issued command from the 1800 is satisfied. Condition code 1, status stored.

WRITE (SYSTEM/360)

The function of the Write command is the transmission of data from the System/360 to the 1800.

Write to an Idle Adapter: When the Write command is issued to an idle Adapter, the System/360 will receive zero status response (condition Code 0, operation initiated) and will then be held up until the 1800 responds with Initialize Read.

Unless suppressed by the M-bit, an interrupt is generated to signal the 1800 that an operation is waiting. The Write command is latched in the Adapter and is available to a Sense DSW command from the 1800.

Write to a Waiting Initialize Read: If a Write command issued by the System/360 encounters a previously issued Initialize Read from the 1800, both operations are performed. System/360 receives Zero status (condition code 0, operation initiated) in response to its command. The operation continues until the System/360 byte count is zeroed, the Adapter word count is zeroed, or an error condition is detected. If neither channel is data chaining, ending status containing Channel End and Device End is issued to the System/360.

The acceptance of the status by the System/360 frees the Adapter and returns it to idle.

<u>Write to a Busy Adapter:</u> There are three Busy responses to a Write issued by the System/360.

- 1. Busy status alone responds to the Write command if a previously issued Control command is still in the Adapter. Condition code 2, busy.
- 2. Busy and Device End status are the response to a Write command if a previously issued Control command was cleared but the Device End had not been accepted. This clears the Device End and leaves the Adapter idle. Condition code 1, status stored.
- 3. Busy and Attention status are the response to a Write command from the System/360 if the 1800 previously issued an Initialize Write. If the Attention had not been previously accepted by the System/360, this clears it as an interrupt condition, although it still appears as a response to another Write until the previously issued command from the 1800 is satisfied. Condition code 1, status stored.

TEST I/O (SYSTEM/360)

A Test I/O may be used by the programmer to determine the status of the System/360 Adapter any time the channel is free. The status received indicates the condition of the Adapter as follows:

- A Zero status indicates that the Adapter is idle at the time of response. Condition code 0, available.
- 2. A Busy status indicates to the System/360 that a Control previously issued had not been accepted. Condition code 2, busy.
- 3. An Attention status indicates to the System/360 that the 1800 previously issued an Initialize Read or Initialize Write. Condition code 1, status stored.
- 4. A Device End status indicates that a previously issued Control was accepted, but that the final interrupting condition had not been accepted by the channel. This clears the Device End status and leaves the Adapter idle. Condition code 1, status stored.
- 5. Channel End and Device End status indicates that a data transfer has been terminated but that the final interrupting condition had not been accepted. This clears the status and leaves the Adapter idle. Condition code 1, status stored.

NO-OPERATION (SYSTEM/360)

The No-Operation command as used with the System/360 Adapter does not affect the contents of the Adapter latches. It is always handled as an immediate command.

No-Operation to an Idle Adapter: If a No-Operation is issued to an idle Adapter, the System/360 will receive a status response containing Channel End and Device End. No interrupt will occur in the 1800. Condition code 1, status stored.

No-Operation to a Busy Adapter: A No-Operation from the System/360 may be Busy rejected by one of the following three conditions:

1. A No-Operation could be issued by the System/360 before a previous Control is cleared. The Adapter response is Busy status (condition code 2, busy).

- 2. A No-Operation could be issued by the System/
 360 after a previous Control is cleared, but
 before Device End is accepted. The response
 is Busy and Device End. This clears the Device
 End and leaves the Adapter idle. Condition
 code 1, status stored.
- 3. The No-Operation might be issued by the System/360 after the 1800 had issued an Initialize Read or Initialize Write command to the Adapter. The adapter responds with Busy and Attention status to the System/360 (condition code 1, status stored).

HALT I/O (SYSTEM/360)

If Halt I/O is issued while a System/360 Read, Read Backward, Write, or Sense command is latched in the Adapter, the response is immediate. It terminates the operation, (condition code 2, burst operation terminated) sets Channel End and Device End in its status, and waits for a chance to send the status to the System/360. If the 1800 is operating with the Adapter, it receives Halt and Transfer End status via interrupt and a Sense DSW command.

If Halt I/O is issued while an unserviced System/360 Control is latched in the Adapter it will be Busy rejected (condition code 1, status stored).

If Halt I/O is issued to an idle Adapter, zero status is developed (condition code 1, status stored).

Status Summary (System/360)

The following chart summarizes the status information presented to the System/360 during initial selection.

	Initial Status Presented					
360 Issues	Idle 360 Control 1800 Read 1800 Wri					
Read or Read Backward	Zero		Busy and Attention	Zero		
Write	Zero	D	Zero	Busy and Attention		
Control	Channel End	Busy and Device End*	Busy and Attention	Busy and Attention		
No-Operation	Channel End and Device End		Busy and Attention	Busy and Attention		
Sense	Zero		Zero	Zero		
Test I/O	Zero	Busy or Device End*	Attention	Attention		

^{*} Device End is conditional, refer to text.

23411

SENSE (1800)

Three Sense commands are recognized by the Adapter when issued by the 1800 system. A Sense function executed by the 1800 always presents 16 bits of information which are placed in the accumulator.

Sense Device Status Word (DSW): When the I/O control word bit 8 is equal to zero, the 1800 Device Status Word is presented. The various conditions and the corresponding information appearing in the 1800 accumulator in response to the unmodified Sense function are:

Condition	High-Order Accumulator	Low-Order Accumulator
Adapter Idle System/360 has previously issued:	Device Status	Undefined
Control Read Backward Read Write	Device Status	Command Byte
HALT I/O	Device Status	Zero
Transfer of Data	Device Status	Data Byte from Low – Order Buffer Byte
1800 has previously issued:		
Initialize Read Initialize Write	Device Status	IOCC Modifier

17447 A

The 1800 always responds to the Adapter interrupt by executing a Sense DSW command to identify the specific interrupt condition. Command bytes from the System/360 appear as follows in the eight low-order bits of the accumulator. This command resets all status bits except 1 and 2 if IOCC bit 15 is on.

Low Order Bits							
8	9	10	11	12	13	14	15

System/360 has previously issued:

Control	X	хх	X	X	1	1	1
Read Backward	X	хх	X	1	1	0	0
Read	X	хх	X	\mathbf{x}	M	1	0
Write	X	хх	X	X	M	0	1

Sense Word Count: A modified Sense command ("one" in bit position 8 of the control word) is provided to present the current word count of the 1800 Data Channel. The word count will be in true binary format. Following a reset, the word counter will contain maximum value, i.e., bits 2 through 15 on.

Sense Interrupt Level: Identification of a particular interrupt on any level is accomplished with a Sense Interrupt Level command.

INITIALIZE READ (1800)

This command, issued in conjunction with a Write command from the System/360, initiates data transfer from the System/360 to the 1800.

Initialize Read to Idle Adapter: Execution of this function latches the 16-bit portion of the IOCC containing the Area/Function/Modifier into the Adapter buffer, loads the Adapter word count, and raises Attention status to notify the System/360 that an operation is waiting.

Initialize Read to a Waiting Write: If an Initialize Read issued by the 1800 encounters a previously issued Write from the System/360, both operations are performed. The operation continues until either the System/360 byte count is zeroed, the Adapter word count is zeroed, or an error condition is detected. Terminating status will be Transfer End. The terminating status will also contain Halt if the System/360 terminated the data transfer.

Initialize Read to a Busy Adapter: There are two Busy responses to an Initialize Read command issued by the 1800:

- Busy rejection is caused by issuing the command to a previously issued uncompleted command from the 1800. The resulting DSW condition is Command Reject and 1800 Command Stored; 360 Command Stored will also be on if a data transfer is in progress.
- 2. An Initialize Read to the Adapter, which contains a previously issued System/360 command other than Write is rejected. A sense DSW indicates Command Reject and 360 Command Stored.

INITIALIZE WRITE (1800)

Issued to a System/360 Read command, Initialize Write initiates data transfer. If the Adapter is idle, the buffer is loaded with the I/O control word, the word counter is loaded, and Attention is raised to System/360. Busy and DSW response are the same as those indicated under Initialize Read with the Read/Write relationships reversed.

CONTROL (1800)

An 1800 Control command performs a reset of the Adapter. The Adapter is not avail-

able to either system for the duration of the reset.

Note: If the System/360 is using the Adapter at the time of the reset, this command may cause an Interface Control Check in the System/360.

Programming Note: Programming the System/360 Adapter under OS and/or DOS requires special consideration. Please consult your IBM Sales Representative.

The 2790 Adapter is an interface mounted in an IBM 1826 (Model 2 or Model 3) which allows an IBM 1801/1802 Processor-Controller to act as a "system controller" for an IBM 2790 Data Communication System. This combination 1800/2790 system may thus serve as a real time data collection system, or as a "Plant Communication System". This communication system is designed to operate in a multiprogramming environment and utilizes the capabilities of the IBM 1800 Multiprogramming Executive (MPX) Operating System. The system provides concurrent transmission capability to and from the processorcontroller, which controls the overall operation.

A maximum of two 2790 adapters may be installed on a single 1800 System. The terminals provided for the 2790 System are the 2791 Area Station and 2793 Area Station. Each 2790 adapter allows as many as 100 Area Stations to be connected to the Processor-Controller (P-C) by means of a two-wire high speed communication line operating at approximately 500,000 bits per second. The Area Stations (AS) are connected serially, starting and ending at the 2790 adapter, in a loop configuration. Because of this loop configuration, the 2790 adapter has become known as the "Loop Adapter". The 2795 and 2796 Data Entry Units attach to the 2791 and 2793 Area Stations via two-wire communication line.

The 2790 System provides data entry by means of card, badge, or key entry with visual display and attachment of OEM digital devices at the area station level, with time-of-day display and printer output. To extend data entry capability to individual work locations, unique Data Entry Units are provided, allowing entry of numeric data by card, badge, and dial selection.

The 1800/2790 MPX Communications System supports two loop adapters each with a maximum of 100 IBM 2791 or IBM 2793 Area Stations, and all capabilities presently existing in MPX. However, each 2790 adapter requires one cycle steal data channel. The transmission loop is divided into four segments (also called "lobes"); each of the four segments has its own connections to the adapter. Data from each segment is normally fed to the next segment in the loop. However, any combination of segments may be bypassed under program control. When a segment is bypassed, the area stations on that segment receive data from the adapter, but the adapter will not accept data from the segment. This

transmission line segmentation permits access to an Area Station on one segment even though another segment becomes inoperable.

The transmission loop is also time multiplexed into nine different channels; the ninth channel is subdivided into five channels with only one being selected for use during any one complete loop cycle. Eight input devices are normally associated with the first eight channels; whereas, four output devices and a time display update feature are normally associated with the subdivided ninth channel.

Features

The 2790 adapter and its 1800/2790 MPX Communications System provide the following features and functions:

- 1. Frame serializer/deserializer.
- 2. Transmission system control procedures for normal messages as well as messages with errors.
- 3. Automatic error recovery.
- 4. Circuits and programs to localize and isolate faults on the transmission system.
- 5. Message check based on transaction code via MPX Subroutines as user desires.
- 6. Error statistics for area stations on the loop.
- 7. Ability to concurrently receive messages from as many as eight input devices on the loop and write messages to four output devices on the loop.
- 8. A real time clock function is provided by the MPX time-of-day support feature. This feature provides automatic time-of-day display at the digital readout of 2791 area stations.

Configuration

The 2790 adapter is physically mounted in an IBM 1826 Data Adapter Unit (Model 2 or Model 3) and receives its power from the 1826; if two adapters are to be installed in the same system, the two adapters may be mounted in two 1826 Model 2's, or in a single 1826 Model 3, if room exists. The adapter interfaces the 1801/1802 via the 1800 I/O channel. To obtain full capabilities of the 1800/2790 MPX Communication System, the machine configuration shall be at least:

One IBM 1801/1802 Processor-Controller with a minimum of 24K words of core storage. One IBM 1053 Printer or IBM 1816 Printer-Keyboard.

One IBM 1442 Card Read Punch One 1810 Disk Storage Unit (Model A2 or B2), or one 2311 Disk Storage Unit.

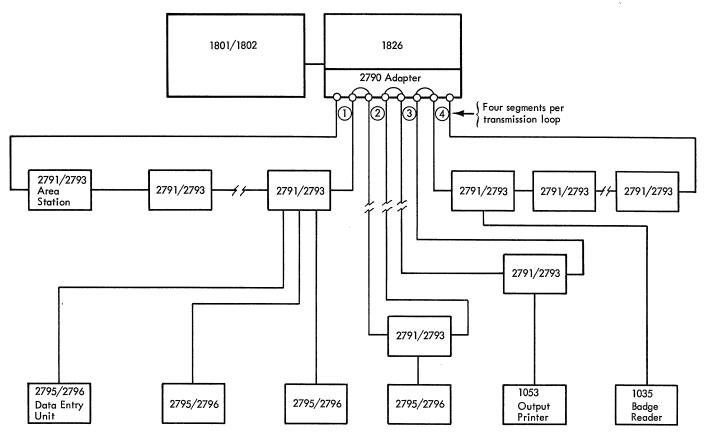
Each of the IBM 2791 or IBM 2793 Area Stations may have as many as 32 IBM 2795 or IBM 2796 Data Entry Units attached to it; however, the adapter may service, via the area stations, a maximum of 1024 Data Entry Units (Figure 83.1). Thus, one must realize that a single 2790 adapter is not capable of servicing the maximum 32 Data Entry Units on all

100 possible area stations. No two area station configurations are necessarily identical in function or operation.

FUNCTIONAL AREAS

The 2790 adapter consists of the seven following functions:

- 1. Loop Output
- 2. Loop Input
- 3. Frame Processing Controls
- 4. Cycle Steal Controls



Note:

Maximum 100 area stations per adapter.

Maximum 1,024 data entry units per adapter.

Maximum 32 data entry units per area station.

Maximum 3 1035 Badge Readers per 2791 Area Station.

Maximum one 1053 Printer per area station.

Maximum 1,000 foot two-wire communications line between data entry units and area stations.

Maximum 1,000 foot two-wire communications line between area stations, and between area stations and the adapter.

Figure 83.1. 1800/2790 Configuration for One Adapter

17827

- 5. 1800 I/O Channel Interface
- 6. Repeater Interface and Bypass Controls
- 7. Diagnostic Controls

LOOP OUTPUT

When a loop channel is active, the output area takes data from the four output registers, and serializes the data sequentially onto the loop. The four bytes of data from the Output Registers are transmitted in a frame which consists of five bytes. The first byte is a Start character generated by the loop output area. The four bytes of data follow the Start character. An entire frame cycle consists of 30 bytes. The remaining 25 bytes are Sync characters, which are also generated by the loop output circuitry.

When the output registers have been emptied, the output area causes cycle stealing to fetch the next output frame and put it in the empty registers. If the output registers are not filled when the frame byte count reaches 30, the contents of the registers are ignored, and Sync characters are placed onto the loop. Thus, if for any reason the data channel is unable to service the output area, a frame, consisting of one Start character and 29 Sync characters, is sent out. When the loop is non-operational, i.e., an XIO Start Loop has not been issued, Sync characters are continuously sent out on the loop. Normally, the only time there are no bits on the loop is when the 2790 adapter has no power.

LOOP INPUT

The input area circuitry assembles each byte of an incoming frame of a loop into its shift register to allow the frame process area to process that byte. In order to perform this function, the input area contains a bit counter, a byte counter, a shift register, synchronization controls, and a channel counter. The input area also contains some diagnostic circuitry.

The loop input data is shifted serially by bit into the shift register. Bit synchronization occurs when a Sync character is found. The Sync-Start sequence of characters is used to reset the byte counter. If a character other than Sync or Start is found between bytes 6 and 30, the input area assumes that it is out of bit sync and starts hunting for a Sync character every bit time. When a Sync character is found, the bit counter is reset and a return to normal mode takes place. The channel counter keeps track of which frame is being processed and is effectively stepped each time the byte counter

reaches count 6. The input area also decodes the Skip character between bytes 6 and 30 and uses it to inhibit the advancement of the byte counter. The Skip character is generated by an area station when it comes on-line either voluntarily or by command. An area station has a byte delay through it when it is on-line. When it comes on-line, it adds a byte to that frame. The extra byte is the Skip character and is not counted by the circuitry.

FRAME PROCESSING

These controls analyze the data transmission frame and either generate the next frame to go out in that channel, or cause an interrupt to the 1800 program. The frame processing controls are enabled by the process frame bit being on in Word 2 of the Loop Channel Control Block (refer to "Program Control"). Normally, the presence of the Start character is used to signify the beginning of a new frame. If the Process Frame bit is on at byte 1 time, the next four bytes will be processed. Before the incoming frame arrives, the cycle steal controls must have fetched the corresponding frame from core storage and loaded it into the input registers. When the incoming active frame arrives, the frame process circuits generate a new active frame, byte by byte, depending upon the contents of the corresponding bytes of the incoming frame as seen in the shift register. The new frame is stored in four one-byte Input registers. If the incoming frame is the last of a sequence or an error is detected, a channel interrupt is set and a new frame is not generated. If an error is detected, the incoming frame is still stored in the four input registers.

An input overrun condition can occur if the input registers are not loaded by input byte 2 time as a result of higher priority cycle steals. This condition causes the incoming frame not to be processed; it will cause the same frame to be sent a second time. If an error is created by an overrun condition, the error is detected the next time the frame from this channel is processed. The 1800/2790 MPX Communication System will initiate appropriate error recovery procedures.

The frame process circuits indicate to the cycle steal controls when it has a data byte to be stored into a buffer, or when it requires a data byte to be sent out on the loop.

CYCLE STEAL CONTROLS

The cycle steal controls perform the following functions:

- 1. Fetch a frame from the Loop Channel Control Block (LCCB) in core storage for the output section to transmit to the loop.
- 2. Fetch a frame from the LCCB for the input section to process with the incoming frame.
- 3. Store a processed frame in the LCCB.
- 4. Store the interrupting channel number in the Loop Channel Interrupt Block (LCIB).
- 5. Store the Channel Sense Word (CSW) or the CSW and Error Frame in the LCCB.
- 6. Store data into core storage buffers.
- 7. Fetch data from core storage buffers.

The cycle steal control circuits use inputs from the frame process circuits and output circuits to tell it what functions are required of it. The cycle steal controls then analyze the priorities to determine who gets service first.

The 2790 adapter never uses machine cycles consecutively. The adapter normally uses every other one while stepping through a cycle steal sequence, unless a higher priority device prevents it. Under normal operating conditions, the maximum number of cycles that the adapter can use in any 540 μ s period is 16; however, the worst case greatest number of cycle steals that the 2790 adapter can use in any 540 μ s period is 25 and occurs when storing data in a buffer or fetching data from a buffer, and an error is detected. The minimum number of cycles within a 540 μ s period is six, and occurs when a channel is inactive.

1800 I/O CHANNEL INTERFACE

This section takes the channel lines and uses them to transfer relevant data to and from the 2790 adapter. The interface provides the In Bus generating circuitry, interrupt controls, adapter status latches, and decodes for commands which the adapter can recognize.

REPEATER INTERFACES AND BYPASS CONTROLS

Because the transmission loop is divided into four segments, there are signal "repeaters" between each segment. Each repeater has a bypass line to allow coupling the segments together. Bypass controls allow any segment to be eliminated from the loop under program control by selectively gating the data to a given segment driver of the loop input section from any of the previous segment terminators or from the loop output section. This gating is under control of the adapter bypass register. There is a bit in this register for each of the four loop segments. A bit being set indicates that its

associated segment is to be bypassed. There are 16 possible combinations of segment bypassing; one of these, "no segments bypassed", is the normal mode of operation. When all segments are bypassed the output section data is directly gated to the input section without going through any segment repeaters. This "all segment bypass" operation is used to check the 2790 adapter circuits and gate the adapter diagnostic controls.

When any segment is bypassed, area stations on the bypassed segment still receive valid data; however, data <u>from</u> the bypassed segment is ignored. The bypass register bits are loaded with the contents of modifier bits 12 through 15 on the XIO Stop Loop control cycle. The setting of these bits can be sensed by the program using the XIO Sense Device instruction.

2790 ADAPTER DIAGNOSTIC CONTROLS

Special diagnostic controls have been built into the 2790 adapter to be used in conjunction with the "2790 Adapter Diagnostic" to aid the Customer Engineer in circuit failure isolation. A diagnostic register of 7 bits has been provided to store modifier bits 9 thru 15 of the XIO Start Loop Command. Bits 9, 10, and 11 of the diagnostic register is referred to as the Diagnostic Mode Register (DMR). The output of the DMR is decoded into various diagnostic functions for specific hardware malfunction isolation. Bits 12, 13, 14, and 15 of the diagnostic register is referred to as the Diagnostic Response Register (DRR). The DRR bits are used for simulating AS responses when all segments are bypassed thus providing a capability to exercise the frame processing circuits of the 2790 adapter.

Diagnostic circuits also provide two special diagnostic DSW's. See Sense Diagnostic DSW Usage.

OPERATION

A "select out" type of operation is used to determine the devices that require service. A frame associated with an unused channel is transmitted with "any address" code in the Area Station Address field. (Figure 83.2). An AS requiring service looks for the "any address" code and captures the frame by replacing the code with its address. This not only identifies the AS, but also prevents any other AS from seizing the frame. The AS then inserts the address of the device that will be serviced in the

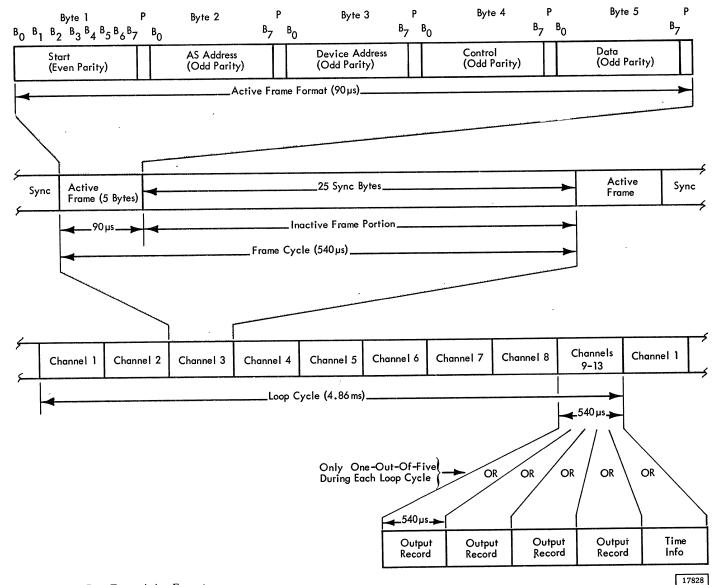


Figure 83.2. Data Transmission Format

Device Address field and inserts a read request code in the Control field. For the duration of the operation, this channel will always be addressed to this AS.

Area Stations attach to the transmission loop by inserting a one-byte shift register in series with the line. This shift register (Figure 83.3) enables the AS to examine and modify a full byte of information before passing it on.

Synchronization is maintained by always looking for either a Sync or a Start code every byte time while between frames. If neither code is seen, checking for Sync every bit time is initiated. When a Sync is found, the unit returns to the mode of looking for a Sync or a Start every byte time.

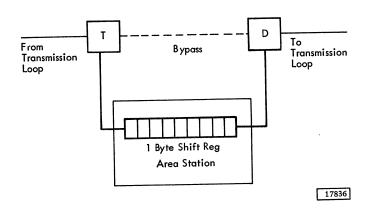


Figure 83.3. One-Byte Shift Register

LOOP CHANNELS

The transmission loop has been artificially divided into nine basic channels by the 2790 adapter. A frame is associated with each of the nine channels and is sent out in a fixed sequence. The first eight channels are frequently referred to as "high speed" with a data transmission rate of approximately 206 frames per second for each of the channels. However, because each active frame contains one data character and each data character is always transmitted twice, the effective data rate for each of these eight "high speed" channels is approximately 103 characters per second. These "high speed" channels are most often used and referred to as the "read" channels.

The ninth channel is further subdivided into five "low speed" channels and designated as "Channel 9-13" because only one of the five channels is selected each loop cycle. This one-out-of-five selection means that five complete loop cycles are required to accommodate all five of the channels using the ninth channel location. The five "low speed" channels each operate at approximately 41 frames per second (i.e., 206 frames per second divided by five subdivisions is approximately 41 frames per second), or at approximately 20 characters per second for data transfer. Because of the lower transmission rate, the "low speed" channels are most often used and referred to as the "write channels", as this rate corresponds closely with the output printer speed.

Eight independent records may be read and five independent records may be written on the eighth high speed and five low speed loop channels respectively. Generally, four low speed channels are used for write operations and the fifth low speed channel is used for broadcasting time.

DATA TRANSMISSION ARRANGEMENT

Bits of information are transmitted over the loop as bipolar pulses at approximately 500 kHz as long as the 2790 adapter in the 1826 has power. The nature of bipolar pulse transmission makes bit synchronization an inherent characteristic of transmission. All communication between the processor-controller and the area stations is achieved through the use of a sequence of information bytes called a frame. The active frame portion is 90 μ s long and is composed of five bytes (Figure 83.2):

Start AS Address Device Address

Control Data

The Start byte has even parity; the other four bytes contain odd parity. Active frames are transmitted by the loop adapter at $540~\mu s$ intervals and are separated by a series of 25 odd parity Sync bytes (referred to as the inactive frame portion). This separation is primarily used to provide time for processing of input frames and preparation of outgoing frames. The Sync bytes in conjunction with the Start byte continuously provide byte synchronization information.

Start

The Start code (Hex 39) is used to indicate the start of a frame. The end of a frame is determined by a byte count of five in the selected area station. Start is used in conjunction with the Sync code (Hex 47) to determine byte synchronization. This Start byte is the only byte which must use even parity; all other codes must use odd parity. Frame field code structures are shown in Figure 83.4.

Field	Byte	Hex	Bit Pattern 0 1 2 3 4 5 6 7 P
Start	1	39	0011 10010
AS Address	2		
Discrete AS		80-FF	1 A A A A A A -
All AS		09	0 0 0 0 1 0 0 1 1
Any AS		11	0001 0001 1
Device Address	3		Select Adapter
Diagnostics		00	0000000-
Data Entry Unit			11044444-
Local Output		40	0 1 0 0 0 0 0 0 0
Local Input		, ,	1 0 0 0 A A 0 0 -
Badge		80	1 0 0 0 0 0 0 0 0
Card Reader		84	100001001
Keyboard		88	1 0 0 0 1 0 0 0 1
OEM		8C	1 0 0 0 1 1 0 0 0
1035 Badge Reader			1 0 0 0 0 0 A A -
Remote X		81	1000 0001 1
Remote Y		82	1000001011
Remote Z		83	100000110
Control	4		AS P-C Response Digit Command Digit UVWWYYZZ
(Refer to Figure 83.5 for			TTTT Cop Code
All Command/Response			Modifier
Bit Patterns)			AS Defined
			Status Bit
			Data Mode
			Restore Ack
Data, Status or Guidance	5		D D D D D D -
Sync	6-30	47	0 1 0 0¦0 1 1 1¦1

17829

Figure 83.4. Frame Field Code Structure

Area Station Address

Three types of codes are to be found in this AS Address field: (1) a discrete AS Address, (2) an "Any Address" code, and (3) an "All Address" code. There are 128 possible discrete AS Addresses, however, only 100 area stations may be attached to the transmission loop. Only addresses within the area of Hex 80 and Hex FF are valid for these discrete AS Addresses.

Note: Because of MPX system characteristics, it is recommended that AS addresses be assigned sequentially starting with Hex 80. This address assignment does not restrict the physical placement of Area Stations on the loop.

Every frame transmitted to a specific AS has its address in this field. Any time an area station receives a frame with its address or captures an "Any Address" frame, it inserts its address in this field. This insertion provides the ability to diagnose an AS that is misusing frames.

"Any Address" is designated by Hex 11; this code is used to achieve the "select out" type operation. Whenever an AS requires service, it hunts for frames with this code and then inserts its address in its place. This address insertion captures the frame for the AS.

"All Address" is designated by Hex 09; this code is used to provide broadcast capability to the system. When it is in the AS Address field, it is not modified by an AS, but every AS carries out the instruction found in the control field, if it is able. This code is primarily used for diagnostics and to broadcast time.

Device Address

When a frame is addressed to an AS, it is also addressed to a particular device on a specific adapter. The two high-order bits of this byte identify the particular adapter on the AS, or determine that this byte is a part of diagnostic controls. The remaining six bits identify the device attached to that adapter. The diagnostic controls are normally addressed as Hex 00. However, a diagnostic command is executed regardless of the contents of this byte. If an AS adapter is selected, or an AS captures an "Any Address" frame, the AS inserts its address and that of the particular device into the frame.

Control

The Control byte has been divided into two Hex digits. The low-order digit contains the processor-controller (P-C) command. The high-order hex digit contains the AS response. The AS always responds to a command that is valid for it. The command digit is divided into a two-bit operation code and a two-bit modifier. This structure provides four types of commands for a given operation: Read, Write, Control, and Diagnostic.

The Response digit is composed of four bits/ the high-order bit is the Restore Acknowledge bit, the next bit is a data mode bit, and two low-order bits are the status bits. The data mode bit is always set when the addressed adapter decodes a valid operation code and is in Data mode. The status bits are encoded to reflect the stage of the operation of the AS adapter. The data mode bit is always set by the AS when it decodes one of the diagnostic commands. Codes in the control fields have been set up to provide the ability to communicate back and forth between the AS and the 2790 adapter at every step through the various operations.

Data Field

This field contains either a data byte or status information depending upon the contents of the control field. If the control field indicates that the content is data, this byte is transmitted along the loop without being analyzed. If the control field contains a read end or write end operation, then the data byte contains status, except when a read end command is sent to an AS Local I/O Adapter. In this case the data byte contains a guidance character (Hex 80 is the Error Guidance Character). Except for read end commands sent to a local adapter, an all zero status byte indicates normal status. A status byte of Hex 80 indicates an error to all adapters.

Data transfer resulting from a read instruction always involves sending the byte twice, once in each of two frames. This provides data checking without special check hardware in the AS as well as providing interlocks to guarantee transfer. Data transfer resulting from a write instruction is also checked by comparing the returning byte with the transmitted one. Two frames are again required to transfer a byte of data, one for the request and one for the transfer. Because two frames are required for any data transfer, this implies that each of the eight high-speed channels can operate at approximately 103

character cycles per second; whereas, the five low-speed loop channels can each operate at approximately 20 characters per second.

COMMANDS AND RESPONSES

Coding for all commands and responses to these commands is found in the Control byte of each transmission frame. All commands are sent from the 2790 adapter to an Area Station (commands can be generated by the program or the 2790 adapter); whereas, all responses are returned from an Area Station back to the 2790 adapter. Each command and response is also represented by two Hex digits corresponding to the coding within the 8-bit Control byte. The first Hex digit (four high-order bits of the Control byte) is called the AS Response digit. The second Hex digit (four low-order bits of the Control byte) is called the P-C command digit. This command digit is further divided into a 2-bit Modifier and a 2-bit Op code as shown in Figure 83.4.

Commands are readily distinguished from responses by recognizing that the AS Response digit is a zero for all commands; whereas, the AS Response digit is non-zero for all responses (Figure 83.5). There are several commands in each of the three major command categories — Read, Write, and Control. In addition, there is one or more valid responses for each of the commands.

Read Commands

Read — This command code (Hex 06) is generated by the 2790 adapter and sent after an AS has captured an Any Address frame and the AS has generated a Read Request. The code puts the AS adapter in Data mode. The only valid response is Read Command Acknowledge.

Read Null — This code (Hex 02) specifies that the frame is available for any read type request. The code is generated by the program or the 2790 adapter in the read channel frame when no other command is waiting to be transmitted. Four valid responses are: Read Null Acknowledge, Read Request, Read Data Request, and Read End Request.

Read Data — This code (Hex 0A) is generated by the 2790 adapter when a Read Data Request is received. The code causes the AS adapter to send the data byte again, so that a validity check can be performed and also releases the AS adapter to prepare for the next character. The only valid response is Read Data Acknowledge.

Read End — This code (Hex 0E) is generated by the program either as a result of receiving a Read End Request from the AS adapter or as a result of detecting an error that requires the operation to be terminated. This command removes the AS adapter from data mode, thus causing the operation in progress to be terminated in the AS adapter. The AS refers to the data byte to determine which guidance light to turn on. The only valid response to this command is Read End Acknowledge. When the

		Bit F	Pattern	
Code Name	Hex	Response 0123	<u>Command</u> 4567	
Read Commands Read Read Null Read Data Read End	06 02 0A 0E	0000 0000 0000 0000	0110 0010 1010 1110	
Read Responses Read Request Read Cmd Acknowledge Read Data Request Read Data Acknowledge Read End Request Read End Acknowledge Read End Acknowledge Read Null Acknowledge	12 46 62 6A 72 3E 42	0001 0100 0110 0110 0111 0011	0010 0110 0010 1010 0010 1110	
Write Commands Write Write Null Write Data Write End	05 01 09 0D	0000 0000 0000 0000	0101 0001 1001 1101	
Write Responses Write Data Request Write Data Acknowledge Write End Request Write End Acknowledge Write Null Acknowledge Write Cmd Acknowledge	51 69 71 3D 41 45	0101 0110 0111 0011 0010 0100	0001 1001 0001 1101 0001 0101	
Control Commands Bypass Restore Send Sync Begin Diagnostic End Diagnostic	0B 03 04 08 0C	0000 0000 0000 0000	1011 0011 0100 1000 1100	
Control Responses Bypass Acknowledge Restore Acknowledge (Response to Send Sync Cmd) Begin Diagnostic Acknowledge End Diagnostic Acknowledge	6B B3 47 68 4C	0110 1011 0100 0110 0100	1011 0011 0111 1000 1100	
RESPONSE	COMMAND 4 5 6 7 Send Sync, or 0 0 Begin/End Diag 0 1 Write 1 0 Read 1 1 Control 0 0 Null 0 1 1 0 Data 1 1 End 1 1 Command			

17830

Figure 83.5. Command/Response Codes

command is sent to the AS Local I/O Adapter, the data byte contains the Operator Guidance Character. (Refer to IBM 2790 Data Communication System, Component Description, Form A27-3015, for Operator Guidance Codes.)

Read Responses

All read responses are generated by the AS and sent back to the 2790 adapter.

Read Request — This response code (Hex 12) is sent as a response to Read Null when the AS captures an Any Address frame to initiate a read operation. The code indicates that the AS wants that loop channel to transfer information to the 2790 adapter.

Read Command Acknowledge — This code (Hex 46) is sent as a response to a Read command. The response indicates that the AS has received the command and will start to read its media.

Read Data Request — This code (Hex 62) is sent as a response to Read Null if the AS adapter has a data byte to send to the 2790 adapter.

Read Data Acknowledge — This code (Hex 6A) is sent as a response to Read Data command. The response indicates that the AS has executed the command. The AS response digit is the same as in Read Data Request. The 2790 adapter checks the received data byte against the one received with the Read Data Request for validity.

Read End Request — This code (Hex 72) is sent in response to Read Null if the AS adapter has determined either that the data transfer has come to a normal completion or that an error has been detected. The status of the operation is transmitted in the data byte. An all zero status designates a normal end.

Read End Acknowledge — This code (Hex 3E) is sent in response to Read End command. The response indicates that the AS adapter will terminate the operation according to the status in the data byte. The transaction is completed when the code is received by the 2790 adapter. The loop channel can then be made available to other devices when a new data buffer is assigned by the program. The 2790 adapter also checks the received data byte (ending status) against the one transmitted with the Read End Command for validity.

Read Null Acknowledge — This code (Hex 42) is sent in response to Read Null if no action is presently required by the AS adapter and the AS is in data mode. This response causes the 2790 adapter to increment the Channel Timer Count. Refer to Word 8 (Channel Timer Count) under "Loop Channel Control Block".

Write Commands

Write — This command code (Hex 05) is generated by the program to initiate a write operation. The command puts the AS adapter in a data mode. If the AS adapter cannot execute this command, then it will make an end request when it receives the next command, a Write Null Command. The only valid response is Write Command Acknowledge. If the command is sent to the AS Local I/O Adapter and it is busy, the AS will return a non-zero data byte of Hex 80. This will cause the 2790 adapter to repeat sending the command until a proper response is received.

Write Null — This code (Hex 01) is generated by the 2790 adapter and specifies that the frame is available for any write type request from the device that is addressed. This command is transmitted in a write channel frame when no other code is required and the channel is being used. There are three valid responses: Write Null Acknowledge, Write Data Request, and Write End Request.

Write Data — This code (Hex 09) is generated by the 2790 adapter when a Write Data Request is received. It is accompanied by a data byte and the only valid response is Write Data Acknowledge.

Write End — This code (Hex 0D) is normally generated by the 2790 adapter in response to a Write Data Request and there is no data left to be transmitted. The command can also be generated by the program as a result of a program detected error, or as a result of Write End Request by the AS adapter after detecting an abnormal condition. The data byte with the Write End Command is again used as a status field with all zeros representing normal end. The only valid response is a Write End Acknowledge.

Write Responses

All write responses are generated by the AS and sent back to the 2790 adapter.

Write Data Request — This response code (Hex 51) is sent as a response to a Write Null if the AS adapter is ready to receive a data byte.

Write Data Acknowledge — This code (Hex 69) is sent as a response to a Write Data Command, and indicates that it has received the data byte. The 2790 adapter will check the returning data byte against the transmitted one for validity.

Write End Request — This code (Hex 71) is sent as a response to Write Null if the AS adapter has detected an error, or other unusual condition. The status is also sent in the data byte.

Write End Acknowledge — This code (Hex 3D) is sent in response to Write End command. The response indicates that the AS adapter will terminate the operation according to the status in the data byte as modified by the AS adapter. An all zero status represents normal end and the channel can be made available for new operations by the program. If the status is not normal, a channel interrupt is set. The received status byte is checked by the 2790 adapter against the transmitted one for validity.

Write Null Acknowledge — This code (Hex 41) is sent in response to Write Null if no action is presently required by the AS adapter and the adapter is in the data mode. When received by the 2790 adapter, this response increments the Channel Timer Count.

Refer to Word 8 (Channel Timer Count) under Loop Channel Control Block.

Write Command Acknowledge — This code (Hex 45) is sent as a response to a Write command. The response indicates that the AS adapter has received the command and that the adapter has inserted its status in the data byte. An all zero status indicates that the operation will be executed. A non-zero status indicates busy (this can only be returned by the AS Local I/O Adapter). When the status is non-zero, the 2790 adapter will increment the Channel Timer Count. Refer to Word 8 (Channel Timer Count) under Loop Channel Control Block.

Control Commands

Bypass — This command code (Hex 0B) can be initiated by the program as part of its diagnostic procedures. The command causes the AS to bypass its shift register after the frame in which the bypass command is located has passed. This bypass results in the elimination of one of the Sync bytes of this frame, since there is a one-byte delay in the

shift register. While in a bypassed state, the AS can monitor the line, but it cannot insert information. Since the AS takes the data byte out of the frame in which it bypasses, the 2790 adapter byte counter comes up short. However, the Start character resets the byte counter on the next frame. The only valid response is Bypass Acknowledge.

Restore - This code (Hex 03) is initiated by the program as part of its diagnostic procedures. The command causes the bypassed AS to insert its shift register in series with the loop after the control byte has been received. This insertion results in a repeat of the Control byte (Restore command) to become a new data byte. A skip character (all zeros) is also substituted for the old data byte. This substitution results in the byte counter within the 2790 adapter skipping a count. If a command is sent to an AS that is not bypassed, the AS will respond with Restore Acknowledge. This response enables the program to determine whether or not the command has been executed. The active frame returning to the 2790 adapter has six bytes. Bytes four and five contain the Restore command and byte six contains the skip character. The only valid response is the Restore command itself followed by a repeat in the data byte.

Send Sync — This command code (Hex 04) may be initiated by the program after an AS has been placed in diagnostic mode. When received by an AS in diagnostic mode the AS will send a continuous stream of Sync characters until it receives at least two Hex FF characters in succession. This can be achieved by sending a frame with Hex FF in all byte positions. There is no response to this command other than the fact that all Sync characters will be generated by the AS.

This command provides the ability to isolate a link (connecting two successive area stations) that is failing intermittently and causing the system's maximum error rate count to be exceeded.

The command allows predetermined data (Sync characters) to be constantly transmitted by a selected area station without that area station transmitting what it is receiving.

All incoming frames are checked for Sync by using the Unconditional Interrupt bit with all channels; the sync fail check is used for checking all data between frames.

Begin Diagnostic — This code (Hex 08) can be initiated by the program as part of the AS diagnostic procedure. The AS enters diagnostic mode when this command is received. In diagnostic mode, the AS

only responds to commands addressed to it. The only valid response is Begin Diagnostic Acknowledge.

End Diagnostic — This code (Hex 0C) is initiated by the program as an end to the AS diagnostic procedure. The AS is removed from diagnostic mode and returns to normal operation when this command is received. The only valid response is End Diagnostic Acknowledge.

Control Responses

All control responses are generated by the AS and sent back to the 2790 adapter.

Bypass Acknowledge — This control response code (Hex 6B) is sent as a response to Bypass command and indicates that the AS has executed the command.

Restore Acknowledge — This code (Hex B3) is sent by the AS as a response to the Restore Command if the AS is already on line (not bypassed) when the command is received.

Begin Diagnostic Acknowledge — This code (Hex 68) is sent as a response to Begin Diagnostic command, and indicates that the AS has entered diagnostic mode.

End Diagnostic Acknowledge — This code (Hex 4C) is sent as a response to End Diagnostic command, and indicates that the AS has returned to normal mode.

PROGRAM CONTROL

Operation of the 2790 system via the 2790 adapter is under programming control. The program must set up a table of 224 words located on a 256 word boundary; this table must be set up prior to issuing an XIO Start Loop command to begin sending and processing frames of information. The first 16 words of the table are for the Loop Channel Interrupt Block (LCIB); each succeeding set of 16 words is for one Loop Channel Control Block (LCCB). Figure 83.6 shows format and assignments for this 224 word table which contains the LCIB and 13 LCCB's.

The first eight LCCB's are associated with 206 frame-per-second channels that are normally used for read operations; the next four LCCB's are associated with 41 frame-per-second channels normally

used for Write operations; and, the last LCCB is associated with a time broadcast channel. When setting up this table, the program must ensure that the Channel Active bit is <u>not</u> set in each LCCB prior to issuing the XIO Start Loop command. While the 2790 adapter is inactive, no interrupts or cycle steal operations occur.

			Core Address In Hex *
LCIB		(16 words)	XX00 0F
LCCB	Channel 1	(16 words)	10
LCCB	Channel 2	(16 words)	20
LCCB	Channel 3	(16 words)	30
LCCB	Channel 4	(16 words)	40
LCCB	Channel 5	(16 words)	50
LCCB	Channel 6	(16 words)	60
LCCB	Channel 7	(16 words)	70
LCCB	Channel 8	(16 words)	80
LCCB	Channel 9	(16 words)	90
LCCB	Channel 10	(16 words)	Α0
LCCB	Channel 11	(16 words)	ВО
LCCB	Channel 12	(16 words)	C0
LCCB	Channel 13	(16 words)	D0 XXDF
*Hex XX00 is loaded into Table Address Register to set the 2790 Adapter on a 256 word boundary XX = any valid Hex character			

17831

Figure 83.6. 2790 Adapter Table Format

LOOP CHANNEL CONTROL BLOCK (LCCB)

Each loop channel has a 16 word block associated with it that is located in a table associated with the loop. This block is known as the Loop Channel Control Block or simply as LCCB, it contains the status of the channel as well as the frame information that is used to send a frame to the loop and to process a frame. The LCCB is also the means by which communication relative to a given channel is passed between the 2790 adapter circuits and the program. The LCCB format is shown in Figure 83.7; all fields contained in the LCCB are described in subsequent paragraphs.

The 16 words of each LCCB are designated as follows:

Word 1 — Address (Active Frame)

Word 2 - Control (Active Frame)

Word 3 — Byte Count

Word 4 - Buffer Address

Word 5 — Channel Sense (CSW)

Word 6 — Address (Error Frame)

Word 7 — Control (Error Frame)

Word 8 - Channel Timer Count

Word 9 — Not Used by the Adapter*

.

Word 16-Not Used by the Adapter*

LCCB Address Word 1 (Active Frame)

AS Address (bits 0-7) — This 8-bit byte contains the AS Address field that can be put in the frame sent to the loop for this channel. If the process frame bit is set, the 2790 adapter input section uses this byte as an address check on the incoming frame, except if this byte is decoded as the "Any AS" code (Hex 11). In this case, the input section attempts to determine if the frame was seized. If it was, it stores the incoming AS Address in this byte.

Device Address (bits 8-15) — This 8-bit byte contains the Device Address field that can be put in the frame sent to the loop for this channel. This byte is used by the Frame Processing section to check the Device Address of the incoming frame. If an "Any Address" frame was seized, it stores the incoming Device Address in this field.

LCCB Control Word 2 (Active Frame)

Channel Control bits 0-3, are used by the adapter to determine the action to be taken on the channel as follows:

Buffer Available (bit 0) — This bit is set by the program when a read channel is being activated at the end of a read sequence. It is set with a Read End command when a new buffer address and byte count has been inserted in the LCCB. This causes the Frame Process section to set up the "Any Address" frame if the proper response is received from the AS. If this bit 0 is not set and a normal response is received, the normal sequence end bit in the CSW is set and an interrupt is generated.

Unconditional Interrupt (bit 1) — When a frame associated with this channel arrives and the Process Frame bit is set, this Unconditional Interrupt (UI) bit causes the Frame Processing section to store the incoming frame in the Error Frame field instead of the Active Frame field, and set an interrupt. This UI bit is set by the program primarily for diagnostic use.

Process Frame (bit 2) — When a frame for this channel arrives, this bit conditions the Frame Processing section to set up the response if it can, and set a Channel Interrupt if it cannot. This bit is set by the loop output section when it sends out the first frame for the channel after the Channel Active bit is set. Setting this bit ensures that a frame is transmitted after a channel is activated, but before any processing is attempted. If the Process Frame bit is not set, the incoming frame is ignored. This bit is reset by the Frame Processing section when an interrupt is generated.

Channel Active (bit 3) — This bit is set by the program, and determines whether or not a loop channel is active. Setting this bit after setting up the first frame (AS Address, Device Address, Channel Control Command, and Data field) in the Read, Write, or Control sequence to be performed is equivalent to

^{*}These words are used by the 1800/2790 MPX Communication System.

Word Number Low Order & Core Word Function Address Bits* Word Contents 15 78 Device Address Address 0000 AS Address (Active Frame) Channel Active Data/Ending Status Control 0001 CC Command (Active Frame) Byte Count Unused 0010 Byte Count Data Buffer Address 0011 Buffer Address 5 Channel Sense Reserved For CE 0100 (CSW) Device Address 0101 AS Address Address Error Frame Data/Ending Status 0110 CC Command Control AS Response Error Frame Channel Timer Count Channel Timer 0111 Count Not Used by the 2790 Adapter (These Words are Used by the 1800/2790 MPX Communication System) 9 1000 10 1001 11 1010 12 1011 13 1100 14 1101 15 1110 16 1111

Address Bits 8–11 are to be determined by either the Input Channel Counter or the Output Channel Counter Holl Cook

Figure 83.7. Loop Channel Control Block Format

^{*}Address Bits 0–7 are for Table Address on a 256 Word Boundary:
Address Bits 8–11 are to be determined by either the Input Channel Counter or the Output Channel Counter from 0001 through 1101

issuing an XIO to the loop channel. This bit conditions the loop output section to transmit the contents of the AS Address, Device Address, CC Command, and Data fields in the frame that is sent to the loop for this loop channel. If the bit is not set, a frame containing all Sync bytes is sent to the loop for this loop channel. This bit also conditions the output section to set the Process Frame bit if it is not already set. This bit is reset by the Frame Processing section when an interrupt is generated. The Byte Count, Buffer Address, and Channel Timer Count should also be set up before setting the Channel Active bit.

CC Command (bits 4-7) — If the Channel Active bit is set, the Channel Control (CC) command field is placed in the four low order bits of the Control byte of the frame transmitted by the loop output section. This field, in conjunction with the incoming AS Response field and an "Any AS" decode of the AS Address field, is used by the frame processing section to perform three functions: (1) determine if it can, what the CC command in the next frame to the loop should be, (2) set an interrupt if it cannot determine what the CC command in the next frame to the loop should be, and (3) determine whether to check or process the data byte that will be coming.

Data (bits 8-15) — This field contains the data byte or ending status that is placed in the frame sent to the loop for this channel if the Channel Active bit is set. This field is used by the Frame Processing section to store a data byte if a Null command had been sent and one of the following conditions exist (1) a data byte is received for the first time in a read operation, or (2) the next data byte to be sent has been fetched from the data buffer during a write operation.

This field is also used for comparison with (1) the data byte received the second time in a read operation to determine whether it should be stored in the data buffer or (2) the returning data byte received during a write operation to determine if it has been correctly transmitted. This field is also used to store the ending status from the AS.

LCCB Byte Count Word 3

Byte Count (bits 8-15) - This 8-bit field is used by the Frame Processing section to determine whether the low or high order byte of a word in core storage is to be stored or fetched. The byte count is also used to determine when a buffer has been emptied on a write operation, or when a buffer has been filled on a read operation. This field is initially set by

the program before activating a channel. The adapter then decrements the byte count by one each time a byte of data is stored or fetched. Only the low order byte of the word (bits 8-15) can be used.

LCCB Buffer Address Word 4

Data Buffer Address (bits 0-15) — This 16-bit field is used by the Frame Processing section to address the word in which the next data byte will be stored or from which the next data byte will be fetched. This field is initially set by the program before activating a channel. The circuits then increment the address by one each time a word (two bytes) is stored or fetched.

LCCB Channel Sense Word 5

The CSW is used to relate the reason for an interrupt occurring for this Loop Channel to the program. The appropriate bit is set by the Frame Processing section prior to setting an interrupt. If more than one bit is set, the left most (high order) is the most significant. The use of individual CSW bits are described in the following paragraphs.

Sequence Normal End (bit 0) — This bit is set when the sequence initiated by the program reaches its normal ending point as determined from the incoming frame and the stored frame. For data operations, this would imply that a message has either been received or transferred.

Sequence Unusual End (bit 1) — This bit is set when the sequence initiated by the program is prematurely terminated due to AS request. The reason for the action can be obtained from the Data Byte (Word 2, bits 8-15), which contains the AS status.

AS Address Check (bit 2) — This bit is set when an error is detected in the AS address byte of the incoming frame. The presence of this bit also indicates that the incoming frame has been stored in the Error Frame field (Words 6 and 7). This information is to be used to determine the appropriate action to take, via the Error Recovery Procedure (ERP).

Device Address Check (bit 3) — This bit is set when an error is detected in the device address byte in the incoming frame. The presence of this bit also indicates that the incoming frame has been stored in the Error Frame field. This information is to be used to determine the appropriate ERP action to take.

Frame Control Check (bit 4) — This bit is set when an error is detected in the control byte of the incoming frame. The presence of this bit also indicates that the incoming frame has been stored in the Error Frame field. This information is to be used to determine the appropriate ERP action to take.

Data Check (bit 5) — This bit is set when an error is detected in the data byte of the incoming frame. The presence of this bit also indicates that the incoming data byte has been stored in the Error Frame field. The contents of all 2790 adapter input registers have been stored in the Error Frame of this LCCB but only the data byte is significant. This information is to be used to determine the appropriate ERP action to take.

Byte Count Exceeded (bit 6) — This bit is set if the byte count field is zero when an attempt is being made to store a data byte during a read operation. It indicates that additional buffer is required to store the incoming message.

Unconditional Interrupt (bit 7) — This bit is set if the Unconditional Interrupt (UI) bit in the Channel Control field (Word 2, bit 1) is on. The presence of this bit also indicates that the incoming frame has been stored in the Error Frame field.

Data Storage Protect (bit 8) — This bit is set before generating an interrupt if a storage protect error occurs while attempting to store a Data byte in the data buffer. It either indicates that an improper buffer address has been assigned, or that a circuit error has occurred.

Channel Timed Out (bit 9) — This bit is set when a device has been locked to a channel in excess of the time which the program has allotted. (Refer to description of Word 8, Channel Timer Count.)

Sync Frame Check (bit 10) — This bit is set if all the following conditions exist:

- 1. The loop is in operation,
- 2. The loop channel (i.e., a particular frame cycle) is inactive,
- 3. Byte 2 does not have a Sync character,
- 4. Byte 4 does not have a Sync character or special character.

This condition exists because of AS hardware failure or noise on the line. The presence of this bit also indicates that the incoming frame has been stored in the Error Frame field.

CE Diagnostic Bits (bits 12, 13, 14, 15) — These four bits are reserved for Customer Engineering use. They are set from the status of the CE diagnostic circuits. These circuits are set by conditions wired in by the CE to dynamically trap signals as an aid in diagnosing intermittent errors on-line. The CSW cannot be stored with these CE bits alone, one of the other CSW bits 0 to 10 must be conditioned to store the CSW.

LCCB Address and Control Words (Error Frame)

The incoming frame is stored in these two words if either an error is detected in any portion of it, or if the UI bit was set in the Channel Control field (Word 2, bit 1). Individual field locations for this frame are described in subsequent paragraphs.

Address Word 6 (Error Frame)

 $\frac{\text{AS Address (bits 0--7)}}{\text{AS Address byte.}}$ — This contains the incoming

Device Address (bits 8-15) — This contains the Device Address byte.

Control Word 7 (Error Frame)

AS Response (bits 0-3) — This contains the AS Response digit. It indicates the AS mode if no transmission errors have occurred. This field is not valid on a Data Check.

CC Command (bits 4-7) — This contains the incoming CC Command digit. It should be identical to the transmitted CC Command (found in Word 2, bits 4-7) unless a transmission error has occurred. This field is not valid on a Data Check.

Data (bits 8-15) — This contains the incoming data byte or AS status.

LCCB Channel Timer Count Word 8

Channel Timer Count (bits 0-15) — This count is incremented from an initial value to 32,768, at which time it sets the Channel Timed Out bit as previously described. The count is incremented when a Read Null Acknowledge, a Write Null Acknowledge, or a Write Busy is received by the 2790 adapter. The channel timer count should be set up by the program before activating the channel.

LCCB Words 9 through 16

These words are not used by the 2790 adapter. These words are used by the 1800/2790 MPX Communications System.

LOOP CHANNEL INTERRUPT BLOCK (LCIB)

The LCIB is a 16-word block used by the 2790 adapter for internal interrupt stacking, and to convey interrupt status to the program. The LCIB format is shown in Figure 83.8, and all fields of the LCIB are described in subsequent paragraphs.

Interrupt Status Hold Word (ISHW, Word 1)

The ISHW is used by the 2790 adapter to stack and store the identification of all channels that set interrupts while the program is handling other interrupts.

Bits are set in positions 1 through 13 for interrupts set by channels 1 through 13 respectively. After bits from the ISHW have been transferred to the Interrupt Status Word, all former bits in the ISHW are reset by the frame processing section the first time a new bit is set into this field.

Interrupt Status Word (ISW, Word 2)

The ISW is used to relate to the program the identification of the channels that had interrupts outstanding at the time the interrupt to the 1800 was set.

Once the interrupt is set, the contents of this word

	Low Order Core Address Bits*		Word Content														
	12 15	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ISHW	0000		CHNL 1	CHNL 2	CHNL 3	CHNL 4	CHNL 5	CHNL 6	CHNL 7	CHNL 8	CHNL 9	CHNL 10	CHNL 11	CHNL 12	CHNL 13		
ISW	0001		CHNL 1	CHNL 2	CHNL 3	CHNL 4	CHNL 5	CHNL 6	CHNL 7	CHNL 8	CHNL 9	CHNL 10	CHNL 11	CHNL 12	CHNL 13		
3	0010			(The:	se word	s are us	Not u sed by t	sed by he 180	the 279 0/2790	O Adap MPX C	oter Commun	ication					
4	0011								1								
5	0100															***************************************	
6	0101																
7	0110		·														
8	0111																
9	1000																
10	1001																
11	1010																
12	1011																
13	1100																
14	1101																
15	1110																
16	1111								†								

^{*}Address bits 0-7 are for table address on a 256 word boundry: Address bits 8-11 are to be "0000".

Figure 83.8. Loop Channel Interrupt Block Format

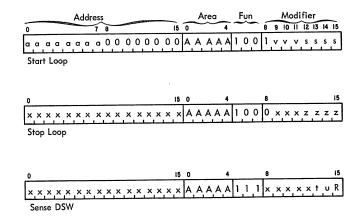
are not changed until the adapter receives an XIO Sense Device with reset. A bit set in positions 1 through 13 indicates an interrupt from loop channels 1 through 13 respectively. When a bit or group of bits are set in this field by the Frame Processing section, all other bits are reset. Bits 0, 14, and 15 are not used.

Words 3 through 16

These words are not used by the 2790 adapter. These words are used by the 1800/2790 MPX Communications System.

INPUT/OUTPUT CONTROL COMMANDS

Two types of IOCC's are valid for the 2790 adapter and will be executed by it; they are the Control and Sense Device IOCC's. All other IOCC's cause a command reject sense bit and an interrupt to be set. Two separate control functions can be performed depending on the condition of modifier bit 8 in the Control IOCC. Start Loop and Stop Loop are the two functions controlled by this modifier bit 8. The various IOCC formats are shown in Figure 83.9.



```
Where:
     AAAAA -- 00111 is the assigned area code for the first
                  2790 Adapter
                 10011 is the assigned area code for the second
     AAAAA --
                  2790 Adapter
                 is not used (ignored)
     XXX
                 are the high order address bits of Table
                  Address Register (TAR)
                  Diagnostic Mode Register (DMR) if all segments
     VVV
                   are bypassed
                  Diagnostic bits for simulating AS Response,
     ssss
                  if all segments are bypassed
                 Bypass bits
     ZZZZ
                 Diagnostic DSW (DDSW-3) of data on In Bus for
                  next cycle steal cycle
Diagnostic DSW (DDSW-2) for cycle steal controls
     u
R
                  This bit determines reset of interrupt indicators
                                                                     17834
```

Figure 83.9. IOCC Formats

Stop Loop

This operation is selected by an IOCC with a Control function code and modifier bit 8 off; the address word is not used. When this IOCC is received and the loop is not in an active status, the adapter sets modifier bits 12 through 15 into a register to be used for segment bypass control. Bit 12, when set, causes segment 1 of the loop to be bypassed. Similarly, bits 13 through 15, when set, cause segments 2 through 4 respectively to be bypassed. The result of this command is to put the loop into an inactive status and prevent any further interrupts or core storage usage. This command should not be issued during normal loop shut down procedures without first waiting for all transactions that are currently in progress to come to their normal conclusion, and second, deactivating all read channels that are not currently in use and not activating any channel after a transaction is completed. This procedure is not required for Error Recovery Procedures when it is determined that the loop is down.

Start Loop

This operation is selected by an IOCC with a control function code and modifier bit 8 set. This coding causes a Blast Reset to the adapter and then causes the adapter to begin sending and processing frames of information. During the data cycle of the IOCC, Out-Bus positions 0 through 7 will be set into the loop adapter Table Address Register (TAR). The contents of TAR will be used in all succeeding 2790 adapter cycle steal sequences as the high order byte of the address word used to select the LCIB or any LCCB.

If all segments are bypassed (as used for diagnostic purposes) then modifier bits 9 through 15 of the XIO Start Loop are used as follows: Bits 9, 10, and 11 are set in the high order position of the diagnostic register which decodes 1 of 7 diagnostic functions; bits 12, 13, 14, and 15 will be stored in low order position of the diagnostic register and placed on the loop to simulate a response from the AS for a command from the 2790 adapter.

Sense Device

This Sense Device is used to load the 2790 adapter status into the 1800's accumulator register for analysis by the program. Modifier bits 13 and 14 of the second IOCC word (Figure 83.9) are used to specify which of the three DSW's (DSW1, DDSW2, or DDSW3) will be loaded into the A-register. Modifier bit 15 of the second IOCC word is used with DSW1 to reset

the interrupting condition in the adapter and transfer interrupts presently stacked in the Interrupt Status Hold Word (ISHW) to the Interrupt Status Word (ISW). If any bits are transferred from the ISHW to the ISW, a new interrupt is initiated. Bits 13, 14 and 15 of the second IOCC word are used for the following DSW selection:

000 - Sense DSW1 without reset

001 - Sense DSW1 with reset

010 - Sense DDSW2

100 - Sense DDSW3

Two diagnostic DSW's are designated DDSW2 and DDSW3. In order to avoid possible confusion with the normal DSW1, there is no DDSW1. Individual bit functions of the three DSW's are shown in Figure 83.10; bit functions for DSW1 are described in subsequent paragraphs.

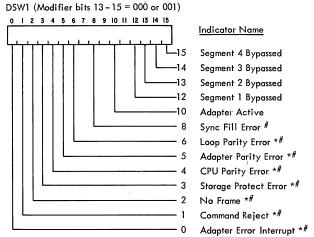
Loop Adapter Error Interrupt (Bit 0) — This bit is active when any error interrupt is set. This bit remains active until all error interrupting circuits are reset with a Sense DSW1 with reset (Bit 15 on).

Command Reject (Bit 1) — This bit is set by issuing an invalid XIO instruction to the adapter. It is also set if an XIO Start Loop is issued while the 2790 adapter is already active and all segments are not bypassed. When this bit is turned on, DSW1 bit 0 is also turned on to cause an interrupt. A Sense DSW1 with reset is required to reset this bit.

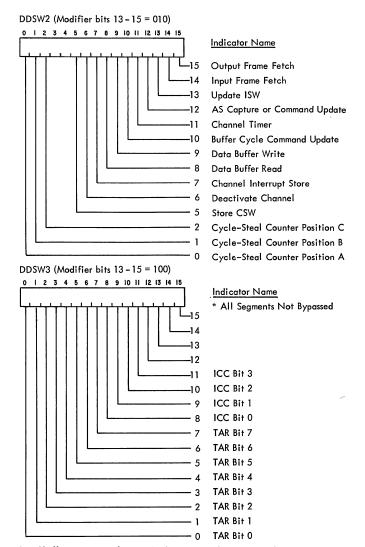
No Frame (Bit 2) — This bit is set to indicate when the 2790 adapter input section fails to receive Start or Sync bytes from the loop for a period of 100 ms or longer. Possible causes for this failure may be an open segment path, malfunctioning Area Station, or malfunctioning adapter output section. When this bit is turned on, DSW1 bit 0 is also turned on to cause an interrupt and remove the adapter from active status. A Sense DSW1 with reset is required to reset this bit.

Storage Protect Error (Bit 3) — This bit is set if a storage protect error occurred when the adapter was storing information into the LCIB or any of the LCCB's. When this bit is turned on, DSW1 bit 0 is also turned on to cause an interrupt and remove the adapter from active status. A Sense DSW1 with reset is required to reset this bit.

CPU Parity Error (Bit 4) — This bit is set if a parity error was detected by the P-C when reading into core storage or fetching out of core storage. This



- * Interrun
- # Indicator reset by Sense DSW1 with reset. (Other indicators are reset by their status turnoff.)



* If all segments are bypassed, then DDSW3 bits 0-15 reflect status of In Bus bits 0-15 respectively.

17835

Figure 83.10. 2790 DSW Bit Designations

bit being turned on also turns on DSW1 bit 0 to cause an interrupt and remove the adapter from active status. A Sense DSW1 with reset is required to reset this bit.

Adapter Parity Error (Bit 5) — This bit is set if the parity bit generated by the adapter for transmission on the loop fails to compare with the corresponding bit sent to the adapter by the 1800 channel interface. When this bit is turned on, DSW1 bit 0 is also turned on to cause an interrupt and remove the adapter from active status. A Sense DSW1 with reset is required to reset this bit.

Loop Parity Error (Bit 6) — This bit is set if the 2790 adapter In Bus generated parity does not check with the parity received from the loop. Data will always be stored with the 2790 adapter In Bus generated parity. This error bit being on turns on Bit 0 of DSW1 to cause an interrupt, but this error alone will not de-activate the 2790 adapter.

Sync Fill Error (Bit 8) — This bit is set if a sync byte is lost during the inactive portion of a frame. This bit does not set DSW1 bit 0 nor does it initiate an interrupt. The bit's purpose is to provide a method of analyzing intermittent loop transmission failures. By checking this bit while sending a Send Sync Command to successive Area Stations, the failure may be narrowed down to a link connecting two Area Stations. A Sense DSW1 with reset is required to reset this bit.

Loop Adapter Active (Bit 10) — This bit is present when the loop is in an active state. The bit is turned on with an XIO Start Loop and is turned off with a Stop Loop IOCC.

Segment 1 Bypassed (Bit 12) — This bit is present when Segment 1 is in a bypassed state as the result of an XIO Stop Loop with modifier bit 12 set; thus, DSW1 bit 12 follows the status of the Stop Loop IOCC modifier bit 12.

Segment 2 Bypassed (Bit 13) — This bit is present when Segment 2 is in a bypassed state as the result of an XIO Stop Loop with modifier bit 13 set; thus, DSW1 bit 13 follows the status of the Stop Loop IOCC modifier bit 13.

Segment 3 Bypassed (Bit 14) — This bit is present when Segment 3 is in a bypassed state as the result of an XIO Stop Loop with modifier bit 14 set; thus, DSW1 bit 14 follows the status of the Stop Loop IOCC modifier bit 14.

Segment 4 Bypassed (Bit 15) — This bit is present when Segment 4 is in a bypassed state as the result of an XIO Stop Loop with modifier bit 15 set; thus, DSW1 bit 15 follows the status of the Stop Loop IOCC modifier bit 15.

SENSE DIAGNOSTIC DSW USAGE

Two diagnostic DSW's are used by the 2790 adapter and are designated as DDSW2 and DDSW3 (Figure 83.10). DDSW2 is sensed with an XIO Sense Device with modifiers bit 13 off and bit 14 on; whereas, DDSW3 is sensed with modifier bit 13 on and bit 14 off. DDSW2 contains control status of the 2790 adapter and DDSW3 contains the data that would be gated to the P-C In Bus when the next cycle steal is taken by the adapter. If all segments are not bypassed, then DDSW3 will reflect TAR and ICC as shown in Figure 83.10; if all segments are bypassed, then DDSW3 reflects the In Bus bit status. Sensing DDSW3 is also used in conjunction with the Diagnostic Mode Register (DMR) to allow single-step operation of the cycle steal controls. When this command is issued, and the DMR is in a prescribed state, one cycle steal can be taken after each Sense DDSW3. These DSW's cannot be used to reset the 2790 adapter; reset can only be accomplished by issuing a Sense DSW1 with reset instruction.

Both DDSW2 and DDSW3 are generally examined when the 2790 adapter is in diagnostic mode (that is, All Segments Bypassed). However, DDSW2 and DDSW3 may be sensed while the 2790 adapter is in normal mode (All Segments Not Bypassed). Sensing DDSW3 while the 2790 adapter is in normal mode provides the means of identifying the LCCB which the 2790 adapter is communicating with at the time DDSW3 is sensed.

CHANNEL SEQUENCE HANDLING

When one of the 13 loop channels is to be activated and caused to step through a sequence of communications with an AS, the program must set up the first frame of the sequence in the LCCB according to acceptable formats and codes, and then set the channel active bit. If the sequence causes data to be transferred, the buffer address, byte count, and Channel Timer Count must be set in the LCCB before setting the channel active bit. Setting the channel active bit is equivalent to issuing an XIO instruction to the loop channel.

The control circuits step through three multiframe sequences without creating an interrupt; these sequences are the read, write, and time sequences. Any of the sequences can be executed by any channel; however, because of the variation in channel speeds and system through-put requirements, the read sequence is normally associated with channels 1-8, the write sequence is associated with channels 9-12, and the time sequence is associated with channel 13.

Note: Even though both the "Read" and "Write" loop channels can be used for either input or output operations, the 1053 Printer Adapter on the 2791/2793 must always operate on the slower speed "Write" channel.

Either the "Read" or the "Write" loop channel can be used to write to the 2791 Digital Display.

Read Sequence

The program can start a read sequence for a channel at any point in the sequence by setting up the frame in the LCCB that is associated with that point and set the channel active bit. The control circuits then transmit that frame and step itself through the remainder of the sequence. There are two normal starting points for a read sequence; specifically, the program may activate a channel with a Read End command frame in the LCCB or the program may activate a channel with an "Any Address" in the LCCB. The sequence is normally started with an "Any Address" frame the first time a channel is activated after the loop is started. The channel remains active until (1) an AS that has seized the channel generates an end request either after sending its data or after it has detected an unusual condition or (2) the 2790 adapter detects an error. In either case an interrupt is set, and the condition that caused it is stored in the CSW field of the LCCB. The channel then becomes inactive.

After a normal sequence end (AS has finished sending its data), the channel is normally activated by the program at the point in the sequence where an End command frame is sent to the AS along with either a normal ending or error ending status. The ending status is the next Guidance Code for the AS Local I/O Adapter. (Refer to IBM 2790 Data Communication System, Component Description, Form A27-3015, for Operator Guidance Codes.) This End command frame removes the AS from data mode and provides an indication to the AS operator as to whether the message was accepted or an error has been detected. If a new buffer is available when this frame is set up, the program should set up the associated Byte Count, Buffer Address, and Channel Timer Count in the LCCB, and also set the buffer available bit before activating the channel; this causes the control circuits to set up the "Any Address" frame unless an error is detected, and an

interrupt is not set until one of the conditions previously described occurs. If the buffer available bit is not set, an interrupt is set when the returning frame is received. Normal sequence end is set in the CSW unless an error is detected. If an error is detected, one of the error bits is set in the CSW.

Write Sequence

The program can start a write sequence for a loop channel at any point in the sequence by setting up the frame in the LCCB that is associated with that point and set the loop's Channel Active bit. The control circuits then transmit that frame and step itself through the remainder of the sequence. The sequence is normally started with a Write Command to an AS once a message has been set up for that AS. Once the channel has been activated, it stays active until one of the following conditions occurs:

- (1) the message has been transmitted to the area station and it has been released, or
- (2) the AS does not accept the command, or
- (3) the AS has been released at its request as the result of its detecting an abnormal condition (such as being out of paper), or
- (4) an error has been detected by the 2790 adapter.

After any of these terminating conditions, an interrupt is set and the condition that caused it is identified in the CSW field of the LCCB. The loop channel then becomes inactive.

Broadcast Time Sequence

The time interval for updating Time Broadcast is to be user defined. The Time Broadcast sequence results in six bytes of data being transmitted to the Local I/O Adapter of all 2791 Area Stations. These six characters will be displayed at the six position digital readout of each 2791 AS if the readout is not being used.

The sequence is started by setting the frame in the LCCB with a Write Command in the CC Command field, "All Address" as the AS address, the Local I/O address as the Device Address, and Hex 00 in the data byte of the LCCB. The byte count is set at 6 and the buffer address is set to the address of the time field in core storage. The time field in core storage consists of three words. The first word contains two bytes which will display a blank in the first two positions of the digital readout (Hex 4040). The next two words (four bytes) make up the loop time in hours and minutes. Each of these four bytes always contains a numeric EBCDIC code.

After the loop Channel Active bit is set, the channel remains active until all six bytes have been transmitted or an error has occurred. An interrupt is then set and the condition that caused it is identified in the CSW. The channel then becomes inactive.

Other Sequences

If any of the control type frames are to be set up and transmitted to the loop, the Unconditional Interrupt bit should be set before activating the loop channel. The incoming frame is then stored in the LCCB and must be checked by the program. The control circuits are not capable of processing frames other than those associated with the sequences previously described.

INTERRUPT HANDLING

Two types of interrupts are generated or processed by the 2790 adapter; they are either interrupts associated with a given loop channel or with the 2790 adapter as a whole. Interrupt conditions detected by the frame processing circuitry are associated with the loop channel whose frame is currently being processed as determined by the input channel counter. Interrupt conditions associated with the basic adapter are error conditions such as loop failure, channel interface errors, and the detection of invalid IOCC's.

When a condition which warrants an interrupt is detected and when the proper interrupt polling signal is issued by the 1800, then the 2790 adapter causes an interrupt to be set on a preassigned level.

When the interrupt routine performs a Sense ILSW instruction, the bit position which is preassigned to the 2790 adapter is turned on to indicate that this device is requesting service. The program should issue a Sense DSW1 instruction without reset to determine the cause of the interrupt. Bit 0 being on indicates that bits 1-6 of the DSW1 word contains error conditions, and appropriate recovery procedures should be initiated. If bit 0 is off, then loop channels are requesting service and the ISW word of the LCIB will indicate just which loop channels to service. A "one" in positions 1 through 13 of this ISW indicates an interrupt from loop channels 1 through 13 respectively. The Channel Sense Words (CSW) in the LCCB's for these channels should be checked and appropriate action should be taken. Any interrupts on other channels which occur while the channel interrupt is set cause the loop channel identification to be stored in the Interrupt Status Hold Word (ISHW).

After a Sense DSW1 with reset is executed by the 2790 adapter, all interrupting conditions are

reset. If any interrupts had been stored in the ISHW, the adapter uses three non-consecutive machine cycles to transfer the contents of the ISHW to the ISW and set the channel interrupt again if the loop is active (running). A Sense DSW1 with reset must be performed before exiting from the interrupt level. If either bits are detected in the ISW (loop channels waiting for service), or errors are indicated in the DSW, the program should service them and repeat the procedure.

When the initial bit is set in either the ISW or ISHW, the remaining bits are reset. When a bit is set in the CSW of any LCCB, the remaining bits are reset. It is, therefore, not necessary that the program clear these fields when it is through using them.

ERROR RECOVERY PROCEDURE (ERP)

When an error occurs on a loop channel, consideration must be given to the effect it has on the area stations on the loop. The errors of greatest importance are the frame transmission errors: AS Address Check, Device Address Check, Frame Control Check, Data Check, and Sync Frame Check. The ERP for these five errors is described in subsequent paragraphs.

Other loop channel errors detected by the 2790 adapter include: Byte Count Exceeded (BCE), Data Storage Protect (DSP), Channel Time Out (CTO), and Sequence Unusual End (SUE). BCE and DSP can both be caused by program errors or by 2790 adapter circuit malfunction, i.e., an input device gets tied up in a read operation. CTO will generally be caused by an AS malfunction, and results in tying up a loop channel to a specific device longer than the normal allowed time. It can also occur as a result of a program error or a 2790 adapter malfunction.

The Error Recovery Procedure for BCE, DSP, and CTO errors is to send an end command with error status (Hex 80) to the AS that was using the loop channel on which the error occurred. One other condition that requires ERP is Sequence Unusual End (SUE). An SUE bit indicates an error condition that is detected by the AS and sent to the 2790 adapter. If SUE occurs on a write operation, it indicates that the operation has been stopped without being completed. The program must send a Write End command to the AS to release it from the write operation. If SUE is associated with a read operation, it indicates that the AS is still waiting to be released. Thus, the program must send a Read End command with error status to the AS to release it. If the AS is in diagnostic mode, the SUE bit will always be set.

The following five frame field errors are more complex to analyze than the errors previously described: AS Address Check, Device Address Check, Frame Control Check, Data Check, and Sync Frame Check. These five errors are described briefly below. It should be noted that the occurrence of any one of these five errors will automatically cause the incoming frame to be stored in the Error Frame field of the LCCB involved.

AS Address Check

This check indicates (except for an "Any Address" frame) that the AS address which is received does not compare with the AS address sent out on that loop channel. This error could be caused by a bit error arising after the frame was processed by the addressed AS, or by a bit error arising before the frame was processed by the addressed AS. In both cases the incorrect address could change to that of an AS farther down the loop, and be processed by that new AS (called the "wrong address" AS). ERP will analyze possible problems created in both area stations and send proper commands to the two area stations to release them.

Device Address Check

These checks are usually caused either by transmission noise or a new device of an AS being selected erroneously. ERP will analyze for possible loss of a message and send end commands to the devices involved to release them.

Control Check

This check can occur as the result of noise on the loop or in the AS, or as a result of the effects of

other ERP's. For example, the "wrong address" AS from an AS Address Check could have turned out to be the address of a nonexistent AS. When the End command is sent to the nonexistent AS, there will be no response to this command and a Control Check will result. A Control Check occurs any time a nonvalid response is received for a particular command which has been sent. ERP will analyze the cause and effect by examination of commands sent with responses received, and then take corrective steps to bring the affected one or more area stations back to the desired status.

Data Check

This check usually results from transmission errors. In most cases, except on an End command, the ERP will send an End command with error status to end the operation presently in progress. The ERP for an End command is dependent on the End command sent.

0

Sync Frame Check

This check indicates noise on the loop has affected the Sync bytes in byte positions two and four of an inactive loop channel. If the returning frame for an inactive loop channel does not have a Sync in the AS Address byte (input byte 2) and a Sync or Special character in the Control byte (input byte 4), then the Sync Frame Check is posted. If input byte 2 is a Sync or input byte 4 is a Sync or Special character, this condition will not be posted. When this check condition is posted, the ERP sends an End command to terminate selection of the AS whose address is found in the Error Frame.

The wide variety of I/O devices that can be ordered with the 1800 System makes I/O device assignment an important part of ordering the system. This section provides information about assignments that are fixed (preassigned by IBM) and assignments that are to be made by the customer. The assignment forms listed below must be completed before an 1800 System can be manufactured.

- Process Interrupt Status Word Assignment Form
- Interrupt Level Status Word Assignment Form

In the sections that follow, address assignment is given for the maximum of each type I/O device.

FIXED ASSIGNMENT

Area Codes are preassigned by IBM to each type of I/O device that can be ordered for the system. The following is a list of those devices and their area codes.

1/0.5	Are	a Code	
I/O Device	Decimal	Binary	Hex
Console Operations	0	(00000)	0
1816/1053 Printers (first 4)	1	(00001)	1
1442 Card Read Punch (first)	2	(00010)	2
1054/1055 Paper Tape Units	3	(00011)	3
1810 Disk Storage (first drive)	4	(00100)	4
1627 Plotter	5	(00101)	5
1443 Printer	6	(00110)	6
2790 Adapter (first)	7	(00111)	7
1810 Disk Storage (second drive)	8	(01000)	8
1810 Disk Storage (third drive)	9	(01001)	9
Analog Input	10	(01010)	Α
Digital Input (Digital and Pulse Count)	11	(01011)	В
Digital and Analog Output (DO, ECO, RO, AO)	12	(01100)	С
System/360 Adapter	13	(01101)	D
2401/2402 Magnetic Tape Units	14	(01110)	Е
1816/1053 Printers (second 4)	15	(01111)	F
Analog Input Expander	16	(10000)	10
1442 Card Read Punch (second)	17	(10001)	11
Selector Channel	18	(10010)	12
2790 Adapter (second)	19	(10011)	13
Comm Adapter (fourth)	20	(10100)	14
Comm Adapter (first)	21	(10101)	15
Comm Adapter (second)	22	(10110)	16
Comm Adapter (third)	23	(10111)	17

Interrupt Levels are assigned a fixed core-storage location. Each interrupt level has its own unique core-storage location which is used as the indirect address of a hardware forced BSI instruction. All interrupt levels except the Trace and CE interrupts have their own Interrupt Level Status Word:

Interrupt Level	Priority	Core Storage Location (decimal)
Internal	1	0008
Trace	26	0009
CE	27	0010
0	2	0011
1	3	0012
2	4	0013
3	5	0014
4	6	0015
5	7	0016
6	8	0017
7	9	0018
8	10	0019
9	11	0020
10	12	0021
11	13	0022
12	14	0023
13	15	0024
14	16	0025
15	17	0026
16	18	0027
17	19	0028
18	20	0029
19	21	0030
20	22	0031
21	23	0032
22	24	0033
23	25	0034

27067 D

Interval Timers are assigned a fixed location in core storage. The core storage locations are:

- 0004 Interval Timer A
- 0005 Interval Timer B
- 0006 Interval Timer C

Digital Input devices (Digital Input and Pulse Counters) use a preassigned group of addresses (IOCC Modifiers). The decimal value of these addresses ranges from 64 through 127. This group of addresses is shared by both Digital Input and Pulse Counters (Figure 84).

Address 64 is assigned to the first Digital Input group of the first Digital Input adapter. Address 65 is assigned to the second Digital Input group of the first Digital Input adapter. This sequence of assignment continues through address 127 which is assigned to the last Digital Input group of the eighth Digital adapter.

If Pulse Counters are ordered, Address 127 is assigned to counters 0 and 1 (8-bit counters) or to counter 0 (16-bit counter) in the first Pulse Counter adapter. Address 126 is assigned to counters 2 and 3 (8-bit counters) or to counter 2 (16-bit counter) in the first Pulse Counter adapter. (Eight-bit counters use two numbers per address; sixteen-bit counters use only one, even-numbered, counter per address.) This sequence of assignment continues through address 64 which is assigned to counters 14 and 15 (8-bit counters) or to counter 14 (16-bit counter) in the eighth Pulse Counter Adapter.

Each adapter ordered is assigned eight addresses in the manner given above. If an adapter is ordered but is not completely populated (for example, only four groups of points are ordered for an adapter), the remainder of the eight addresses for that adapter are not available to be used in another adapter.

Process Interrupt Status Words (PISWs) are digital inputs but have their own group of addresses (IOCC Modifiers). 24 PISWs (16 points per PISW) are available. Address 2 is assigned to PISW 1. Address 3 is assigned to PISW 2. This sequence continues through address 25 which is assigned to PISW 24. Process interrupt points are assigned to a PISW on the Process Interrupt Status Word assignment form. See the section Additional Assignments.

Digital and Analog Output devices share a group of addresses (IOCC Modifiers). The decimal value of

	Decir	nal- Ad	dress	
Digit	al Inputs	↓	Pulse (Counters
Adapter	Group No. (16 pts. ea.)		Counter No. (2/Addr.) *	Adapter
First	0 1 2 3 4 5 6 7	64 65 66 67 68 69 70 71	15-14 13-12 11-10 9-8 7-6 5-4 3-2 1-0	Eighth
Second	0 1 2 3 4 5 6	72 73 74 75 76 77 78 79	15-14 13-12 11-10 9-8 7-6 5-4 3-2 1-0	Seventh
Third	0 1 2 3 4 5 6 7	80 81 82 83 84 85 86 87	15-14 13-12 11-10 9-8 7-6 5-4 3-2 1-0	Sixth
Fourth	0 1 2 3 4 5 6	88 89 90 91 92 93 94 95	15-14 13-12 11-10 9-8 7-6 5-4 3-2 1-0	Fifth
Fifth	0 1 2 3 4 5 6 7	96 97 98 99 100 101 102 103	15-14 13-12 11-10 9-8 7-6 5-4 3-2 1-0	Fourth
Sixth	0 1 2 3 4 5 6	104 105 106 107 108 109 110	15-14 13-12 11-10 9-8 7-6 5-4 3-2 1-0	Third
Seventh	0 1 2 3 4 5 6 7	112 113 114 115 116 117 118 119	15-14 13-12 11-10 9-8 7-6 5-4 3-2- 1-0	Second
Eighth	0 1 2 3 4 5 6	120 121 122 123 124 125 126 127	15-14 13-12 11-10 9-8 7-6 5-4 3-2 1-0	First

^{*}Sixteen-bit counters use even numbers (one counter number per address).

29066 B

Figure 84. IOCC Modifiers for DIAs and PCAs

these addresses is 00 through 127. Each Digital Output Control ordered is assigned 16 addresses starting with address 127 for the first group of 16 points and address 126 for the second group of 16 points. This sequence of assignment continues through address 16 assigned to the last group of 16 points (in the seventh control). See Figure 85 for addresses.

The first and all odd numbered 1856s ordered must be Model 1. The second and all even numbered 1856s must be Model 2. Each 1856 Model 1 supplies controls to the next higher numbered 1856 Model 2. Address assignment is made for each 1856 Model 1. Sixteen addresses are assigned for each 1856 Model 1 ordered. Eight addresses are assigned to the 1856 Model 1 and eight addresses are assigned to the next higher numbered 1856 Model 2. If a Model 2 is not ordered, the addresses that would be assigned to the Model 2 are not available to be used by Digital Output. Addresses 00 through 15 are assigned to the first 1856 Model 1 and the first 1856 Model 2. Addresses 16 through 31 are assigned to the second 1856 model 1 and the second 1856 model 2. This sequence of assignment continues through Addresses 112 through 127 which are assigned to the eighth 1856 Model 1 and the eighth 1856 Model 2 (Figure 85).

ADDITIONAL ASSIGNMENTS

Initial Program Load

(IPL) is assigned to one of two input devices:

First 1442 Card Read Punch 1054 Paper Tape Reader (if 1442 is not on system)

Interval Timers

Interval Timers each must be assigned a time increment when the system is ordered (all three timers). Table 4 of this manual lists time increments that can be designated.

Data Channel Assignment

Data Channels are assigned specific priorities. Data Channel 1 has the highest priority and the order of the priority follows the numeric sequence of the Data Channel numbers, with Data Channel 15 being the lowest priority.

When a system is ordered by the customer, the devices and features ordered are automatically assigned to Data Channels according to the intrinsic

data rates and operational characteristics of the devices ordered. The following is a listing of the devices and features in the sequence that they are assigned to Data Channels. The first device encountered in the list that also appears in the system is assigned to Data Channel 1. Each subsequent device in the system configuration is normally assigned to the next sequential Data Channel.

Selector Channel 2401 Model 3 2401 Model 2 1810 - 11810 - 21810 - 32401 Model 1 1442 (First) 1442 (Second) 2790 Adapter 1 2790 Adapter 2 Analog Input Basic Data Channel Adapter 2 (1810/2)Analog Input Basic Data Channel Adapter 1 (1801/2)Analog Input Exp. Data Channel Adapter 2 (1826) Analog Input Exp. Data Channel Adapter 1 (1826) CA Line Adapter 1 CA Line Adapter 2 CA Line Adapter 3 CA Line Adapter 4 CA Line Adapter 5 CA Line Adapter 6 CA Line Adapter 7 CA Line Adapter 8 System/360 Adapter Digital - Analog Output Digital Input

A different set of Data Channel assignments can be obtained upon customer request.

Two or more devices can share a Data Channel if desired, but concurrent operation of two devices sharing a Data Channel is not possible. In changing Data Channel assignments or sharing Data Channels, programming considerations and physical wiring limitations should be considered. The physical wiring limitations are presented in the IBM 1800 Data Acquisition and Control System Configurator, Form A26-5919. The programming considerations are as follows:

1. IBM systems programs assume that no devices share Data Channels.

		Decimal - /	Addre	ss (Modif	iers)			Decimal - Address (Modifiers)												
	Digital				Analog (Digital Output Analog Output												
DO Control	DO Adapter	Group No. (16 points each.)	¥	DAC 2 or 4 Output	Mod 1 or 3 Output	DAC No. within 1856	1856	DO Control	DO Adapter	Group No. (16 points each.)	¥	DAC A 2 or 4 Output	Mod 1 or 3 Output	DAC No. within 1856	1856					
	1		00 01 02	1st 2nd	lst	1			16	3 2	64 65	1st 2nd	lst	1						
	Addresses		03 04	1st 2nd 1st	lst	2	lst (Model 1)			1 0 3	66 67	1st 2nd	lst	2	9th (Model					
	00 - 15		05 06	2nd 1st	lst	3	(Woder 1)		15	2	68 69 70	1st 2nd	lst	3	(Mode)					
_	not availa	LI-	07 08	2nd 1st	lst	4		4		0 3	71 72	1st 2nd 1st	lst lst	4						
		bie	09 10	2nd 1st	lst	1			14	2	73 74	2nd 1st	lst	1						
	for DO		11 12	2nd 1st	lst	2	2nd (Model 2)			0	75 76	2nd 1st	lst	2	10th (Model					
			13 14	2nd 1st	lst	3	-		13	2	77 78	2nd 1st	lst	3	(,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,					
			15	2nd		4				0	79	2nd		4	ļ					
	28	3 2	16 17	1st 2nd	lst	1			12	3 2	80 81	1st 2nd	lst	1						
		0	18 19	1st 2nd	lst	2	3rd			0	82 83	1st 2nd	lst	2	11th					
27	27	3 2	20 21	1st 2nd	lst	3	(Model 1)		11	3 2	84 85	1st 2nd	lst	3	(Model 1)					
7		0	22 23 24	1st 2nd	lst	4		3		0	86 87	1st 2nd	lst	4						
	26	3 2 1	25 26	1st 2nd 1st	lst	1	_		10	3 2	88 89	1st 2nd	lst	1						
		0 3	27 28	2nd 1st	lst lst	2	4th (Model 2)			1 0 3	90 91 92	1st 2nd	lst	2	12th (Mode					
	25	2	29 30	2nd 1st	lst	3	(Model 2)			9	2	93 94	1st 2nd 1st	lst	3	(Mode)				
		0	31	2nd		4				0	95	2nd	lst	4						
	24	3 2	32 33	1st 2nd	lst	1			8	3 2	96 97	1st 2nd	lst	1						
		0	34 35	1st 2nd	lst	2	5th			0	98 99	1st 2nd	lst	2	13th					
	23	3 2 1	36 37	1st 2nd	lst	3	(Model 1)		7		100 101	1st 2nd	lst	3	(Model					
6		0 3	38 39 40	1st 2nd	lst	4		2	•	0	102	1st 2nd	lst	. 4						
	22	2	41 42	1st 2nd 1st	lst	1			6		104 105	1st 2nd	lst	1						
		0 3	43 44	2nd 1st	lst lst	2	6th (Model 2)			0	106 107 108	1st 2nd	lst	2	14th					
	21	2	45 46	2nd 1st	lst	3	(ITRUE! Z)		5	2	108 109 110	lst 2nd lst	lst lst	3	(Model					
		3	47	2nd		4				0	111	2nd		4						
	20	2	48 49	1st 2nd	lst	1			** 4	2	112 113	1st 2nd	lst	1						
`		1 0 3	50 51 52	1st 2nd	lst	2	7th			0	114 115	1st 2nd	lst	2	15th					
	19	2	52 53 54	1st 2nd 1st	lst	3	(Model 1)		**3	2	116 117	1st 2nd	1st	3	(Model 1)					
5		3	55 56	2nd 1st	lst lst	4		1		0	118 119	1st 2nd	lst	4						
	18	2	57 58	2nd 1st	lst	1			2	2	120 121 122	1st 2nd	lst	1						
	-	0 3	59 60	2nd 1st	lst	2	8th (Model 2)			0	122 123 124	1st 2nd	lst	2	16th					
	1 <i>7</i>	2	61 62	2nd 1st	lst	3	(Model 2)	(Model 2)	(Model 2)	(Model 2)	(Model 2)	(Model 2)		1	2	124 125 126	1st 2nd	1st	3	(Model
		Ö	63	2nd	131	4					126	1st 2nd	lst	4						

^{*} Not available when the first DO Control is in 1826. **Not available when the first DO Control is in 1801.

Figure 85. IOCC Modifiers for DOCs and 1856s

- Assigning high intrinsic data rate devices such as the Selector Channel, 2401/2402, and 1810 to Data Channels with lower priorities than specified in the preceding listing may affect optimum performance in overlapped operations.
- 3. If two Data Channels are assigned to one Analogto-Digital Converter (Random or Comparator), Analog Input Data Channel Adapter 2 must have a higher priority than Analog Input Data Channel Adapter 1.
- 4. Devices assigned to Data Channels with lower priorities than the ones assigned to Digital Input, or Digital Output may be locked out during Data Channel operations with large data tables. This can be partially alleviated by utilizing smaller data tables.

The following I/O devices can be ordered with or without Data Channel assignment:

- Analog Input
- Digital Analog Output
- Digital Input

The following I/O devices do not use a Data Channel:

- 1053 Printer
- 1054 Paper Tape Reader
- 1055 Paper Tape Punch
- 1627 Plotter
- 1816 Printer-Keyboard

Process Interrupt Status Word Assignment

Process Interrupt points are assigned, in sets of four, to a Process Interrupt Status Word (PISW). Twenty-four groups (16 points each) of Process Interrupt are available. Each of these 16 point groups is divided into four sets of four points each for PISW assignment (0-3, 4-7, 8-11, and 12-15). Each set of four can be assigned to the same or to a different PISW. Each PISW can have 16 points assigned (4 sets of 4 each), and the positions of the PISW will correspond to the positions of the points assigned. For example: If the first four points (0-3) of a Process Interrupt group are assigned to PISW 1, they are assigned to positions 0-3 of the PISW 1. Once these four positions are assigned

from one Process Interrupt group, they cannot be assigned to PISW 1 again from any other Process Interrupt group. Other groups of four points (4-7, 8-11, or 12-15) from the same or different Process Interrupt group(s) can be assigned PISW 1. Each PISW has its own address (IOCC Modifier) which is preassigned. See the sections Fixed Assignments and Interrupt.

Interrupt Level Status Word

Each external interrupt level has its own Interrupt Level Status Word (ILSW). An interrupt level requests service when one of the 16 positions of its ILSW contains a one bit. Since each interrupt level has a fixed priority (see the section Fixed Assignment), the customer can assign interrupt priority when he assigns devices to ILSW bit positions.

Devices are assigned to ILSW bit positions on the Interrupt Level Status Word assignment form. When a device is assigned to an ILSW bit, all of the interrupt conditions in the device's Device Status Word (DSW) are ORed into that ILSW bit. Thus, any interrupt condition in the DSW will change the assigned ILSW bit to a one. This is true for Process Interrupt Status Words (PISWs) also. Each PISW is assigned to an ILSW bit position, and an interrupt condition in any of the 16 PISW bits will set its ILSW bit to one.

A PISW or DSW must be assigned to one and only one ILSW bit position. For example, in the first group of four 1816/1053s, each device must be assigned to a different ILSW bit position of the same interrupt level and in the second group of four 1816/1053s each device must be assigned to a different ILSW bit position of the same interrupt level (can be the same level as the first group).

All IBM subroutines (except subroutines under the Time-Sharing Executive System) require that like devices be assigned to the same interrupt level. If the process interrupt routine in the Time-Sharing Executive program is used, each PISW must be assigned to its corresponding ILSW. For example, PISW 1 assigned to ILSW 0, PISW 2 assigned to ILSW 1, . . . and PISW 24 assigned to ILSW 23. The PISWs for any one Process Interrupt Adapter must be assigned within Interrupt level grouping of either 0-11 or 12-23. In addition, no more than one area code may be assigned to any one ILSW bit.

Console interrupt can be assigned any unused ILSW bit position on any available interrupt level.

The following interrupts must be assigned for all systems:

TI Timer interrupt (combined interrupt signal from three interval timers)

```
Typ-1 First 1816 or 1053 (circuitry is basic in P-C)
2401/2 1802 only
CI Console interrupt
```

The following interrupts must be assigned if any of the associated features are ordered for the system:

```
Typ-2
           1053s
Typ-3
Typ-4
Typ-5
           1816 or 1053
Typ-6
                             Output Printer
Typ-7
           1053s
                             Expander
Typ-8
1054/5
           1054/1055
1442 - 1
           First 1442 Adapter
1442 - 2
           Second 1442 Adapter
1443
           1443 Controls
1627
           1627 Controls
1810-1
           1810 (first drive) Model A1, A2,
             A3, B1, B2, or B3
1810-2
           1810 (second drive) Model A2, A3,
             B2, or B3
           1810 (third drive) Model A3 or B3
1810-3
2790-1
           First 2790 Adapter
2790-2
           Second 2790 Adapter
360/CA
           System/360 Adapter
AIB
           Analog Input Basic (any ADC in
             1801/2)
AIBC
           Analog Input Basic with Comparator
             (in 1801/2)
AIE
           Analog Input Expander (in 1826)
AEC
           Analog Input Expander with Com-
            parator (in 1826)
CA-LA1
           First CA (Line Adapter 0)
           First CA (Line Adapter 1)
CA-LA2
CA-LA3
           Second CA (Line Adapter 0)
           Second CA (Line Adapter 1)
CA-LA4
CA-LA5
           Third CA (Line Adapter 0)
CA-LA6
           Third CA (Line Adapter 1)
CA-LA7
           Fourth CA (Line Adapter 0)
CA-LA8
           Fourth CA (Line Adapter 1)
DAO
           Digital-Analog Output
\mathbf{DI}
           Digital Input (DI, PC, or PI)
SC
           Selector Channel
```

Assignment of devices to ILSWs should begin with the leftmost bit position (bit 0) and progress to the next higher bit position for each device assigned to the ILSW.

Analog Input (1851)

There are 1024 (0-1023) decimal addresses (Multiplexer Addresses) available for use with Analog Input. The first 256 addresses (0-255) are used by

both Multiplexer/S and Multiplexer/R. Since these 256 addresses have a dual use, bit 3 of each Multiplexer Address Word is used to specify which multiplexer is being addressed (Multiplexer/S or Multiplexer/R). When bit 3 is a zero, Multiplexer/R is addressed. When bit 3 is a one, Multiplexer/S is addressed.

All Multiplexer/S groups are installed in the lowest numbered 1851s (1851s 1-4). Multiplexer/S will be followed by Multiplexer/R in the sequence listed below.

- 1. High Level
- 2. ±10 mv range
- 3. ±20 mv range
- 4. ±50 mv range
- 5. ±100 mv range
- 6. ±200 mv range
- 7. ±500 mv range

Addresses for each point within an 1851 are shown in Figure 86 for Multiplexer/S and Figure 87 for Multiplexer/R. Each 1851 ordered is assigned the 64 addresses shown in these two illustrations.

Multiplexer/S groups are installed in an 1851 in the following sequence: Group 0, group 1, group 2, and group 3. For example, if two groups of Multiplexer/S are ordered, they are installed in group 0 and group 1. Addresses are assigned to each 1851, so that in the above example, 32 addresses are assigned to group 0 and 1, and 32 addresses are reserved for groups 2 and 3.

Addresses for 1851s containing Multiplexer/R (Multiplexer/S and Multiplexer/R are not installed in the same 1851) are assigned as shown in Figure 87.

Multiplexer/R groups are installed in an 1851 in one of the following sequences, depending on the system configuration.

- 1. 1851s containing all high-level inputs or all the same low level range are installed in the following sequence: Group 0, group 1, group 2, and group 3.
- 2. 1851s containing high-level inputs and one low-level input range (maximum two ranges per 1851) are installed in the following sequence: High-level starting with group 0 and ascending, low-level starting with group 3 and descending. For example, if one group of high-level and three groups of ±10 mv range are ordered for the same 1851, the one group of high level is installed in group 0 and the three groups of ±10 mv range are installed in groups 3, 2, and 1. An exception to this sequence occurs when the groups of high-level inputs are installed in an

	mbering nin 1851		1851s With Multiplexer/S							
Group Number	Point Number	1st 1851	2nd 1851	3rd 1851	4th 1851					
0	00 01 02 03 04 05 06 07 08 09 10 11 12 13 14	00 01 02 03 04 05 06 07 08 09 10 11 12 13 14	64 65 66 67 68 69 70 71 72 73 74 75 76 77 78	128 129 130 131 132 133 134 135 136 137 138 139 140 141 141	192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 207					
1	16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31	116 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31	80 81 82 83 84 85 86 87 88 89 90 91 92 93 94	144 145 146 147 148 149 150 151 152 153 154 155 156 157 158	208 209 210 211 212 213 214 215 216 217 218 219 220 221 222 223					
2	32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47	32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47	96 97 98 99 100 101 102 103 104 105 106 107 108 109 110	160 161 162 163 164 165 166 167 168 169 170 171 172 173 174	224 225 226 227 228 229 230 231 232 233 234 235 236 237 238 239					
3	48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63	48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63	112 113 114 115 116 117 118 119 120 121 122 123 124 125 126	176 177 178 179 180 181 182 183 184 185 186 187 188 189 190	240 241 242 243 244 245 246 247 248 249 250 251 252 253 254 255					

Figure 86. Multiplexer/S Addresses

- 1851 Model 2. Since points 00 and 01 are reserved for reference voltage and RBT respectively in an 1851 Model 2, high-level groups are installed starting with group 3 and descending, and the thermocouple inputs are installed starting with group 0 and ascending (opposite of the above example). An 1851 Model 2 must have ±10 mv, ±20 mv, or ±50 mv range specified for group 0.
- 3. 1851s containing two ranges of low-level inputs have the first range installed in ascending order starting with group 0. The second range is installed in descending order starting with group 3. For example, if two groups of ±10 mv range and two groups of ±20 mv range are ordered, the two groups of the ±10 mv range are installed in groups 0 and 1, and the two groups of ±20 mv range are installed in groups 3 and 2.

Numbe Within																	
Group Number	Point Number	1st 1851	2nd 1851	3rd 1851	4th 1851 -	5†h 1851	6th 1851	<i>7</i> th 1851	8th 1851	9th 1851	10th 1851	11th 1851	12th 1851	13th 1851	14th 1851	15th 1851	16th 1851
	00	00	64	128	192	256	320	384	448	512	576	640	704	768	832	896	960
	01	01	65	129	193	257	321	385	449	513	577	641	705	769	833	897	961
	02 03	02 03	66 67	130 131	194 195	258 259	322 323	386 387	450 451	514 515	578 579	642 643	706 707	<i>77</i> 0 <i>77</i> 1	834 835	898 899	962 963
	03	03	68	132	196	260	324	388	452	516	580	644	708	772	836	900	964
	05	05	69	133	197	261	325	389	453	517	581	645	709	773	837	901	965
	06	06	70	134	198	262	326	390	454	518	582	646	<i>7</i> 10	774	838	902	966
0	07	07	71	135	199	263	327	391	455	519	583	647	711	775	839	903	967
	08	08	72	136	200	264	328	392	456	520	584	648	712	776	840	904	968
	09 10	09 10	73 74	137 138	201 202	265 266	329 330	393 394	457 458	521 522	585 586	649 650	713 714	<i>777</i> <i>77</i> 8	841 842	905 906	969 970
	11	11	75	139	203	267	331	395	459	523	587	651	715	779	843	907	971
	12	12	76	140	204	268	332	396	460	524	588	652	716	780	844	908	972
	13	13	77	141	205	269	333	397	461	525	589	653	717	781	845	909	973
	14	14	78	142	206	270	334	398	462	526	590	654	718	782	846	910	974
	15	15	79	143	207	271	335	399	463	527	591	655	719	783	847	911	975
	16	16	80	144	208	272	336	400	464 465	528 529	592	656	720 721	784 705	848	912	976
	17 18	1 <i>7</i> 18	81 82	145 146	209 210	273 274	337 338	401 402	466	530	593 594	657 658	721 722	785 786	849 850	913 914	977 978
	19	19	83	147	211	275	339	403	467	531	595	659	723	787	851	915	979
	20	20	84	148	212	276	340	404	468	532	596	660	724	788	852	916	980
	21	21	85	149	213	277	341	405	469	533	597	661	725	789	853	917	981
	22	22	86	150	214	278	342	406	470	534	598	662	726	790	854	918	982
1	23 24	23 24	87 88	151 152	215 216	279 280	343 344	407 408	471 472	535 536	599 600	663 664	727 728	791 792	855 856	919 920	983 984
'	24 25	25	89	153	217	281	345	409	473	537	601	665	729	793	857	921	985
	26	26	90	154	218	282	346	410	474	538	602	666	730	794	858	922	986
	27	27	91	155	219	283	347	411	475	539	603	667	<i>7</i> 31	<i>7</i> 95	859	.923	987
	28	28	92	156	220	284	348	412	476	540	604	668	732	796	860	924	988
	29 30	29 30	93 94	157 158	221 222	285 286	349 350	413 414	477 478	541 542	605 606	669 670	733 734	797 798	861 862	925 926	989 990
	30	31	95	159	223	287	351	415	479	543	607	671	735	799	863	927	990
	32	32	96	160	224	288	352	416	480	544	608	672	736	800	864	928	992
	33	33	97	161	225	289	353	417	481	545	609	673	737	801	865	929	993
	34	34	98	162	226	290	354	418	482	546	610	674	738	802	866	930	994
	35	35	99	163	227	291	355	419	483	547	611	675	739	803	867	931	995
	36	36	100	164	228 229	292 293	356 357	420 421	484 485	548	612	676	740	804	868	932	996
	37 38	3 <i>7</i> 38	101 102	165 166	230	293 294	358	422	486	549 550	613 614	677 678	741 742	805 806	869 870	933 934	997 998
	39	39	103	167	231	295 .	359	423	487	551	615	679	743	807	871	935	999
2	40	40	104	168	232	296	360	424	488	552	616	680	744	808	872	936	1000
	41	41	105	169	233	297	361	425	489	553	617	681	745	809	873	937	1001
	42	42	106	170	234	298	362	426	490	554	618	682	746	810	874	938	1002
	43 44	43 44	107 108	171 172	235 236	299 300	363 364	427 428	491 492	555 556	619 620	683 684	747 748	811 812	875 876	939 940	1003 1004
	45	45	109	173	237	301	365	429	493	557	621	685	749	813	877	941	1004
	46	46	110	174	238	302	366	430	494	558	622	686	750	814	878	942	1006
	47	47	111	175	239	303	367	431	495	559	623	687	<i>7</i> 51	815	879	943	1007
	48	48	112	176	240	304	368	432	496	560	624	688	752	816	880	944	1008
	49	49	113	177	241	305	369	433	497	561	625	689	753 754	817	881	945	1009
	50 51	50 51	114 115	1 <i>7</i> 8 1 <i>7</i> 9	242 243	306 307	370 371	434 435	498 499	562 563	626 627	690 691	754 755	818 819	882 883	946 947	1010 1011
	52	52	116	180	244	308	372	436	500	564	628	692	756	820	884	948	1011
	53	53	117	181	245	309	373	437	501	565	629	693	757	821	885	949	1013
	54	54	118	182	246	310	374	438	502	566	630	694	758	822	886	950	1014
3	55	55	119	183	247	311	375	439	503	567	631	695	759	823	887	951	1015
ا ،	56 57	56 57	120	184	248 249	312	376	440	504 505	568	632	696	760 741	824 825	888 889	952	1016
	57 58	<i>57</i> 58	121 122	185 186	250	313 314	377 378	441 442	505	569 570	633 634	697	761 762	825	889	953 954	101 <i>7</i> 1018
1	59	59	123	187	251	315	379	443	507	571	635	698 699	763	827	891	955	1018
	60	60	124	188	252	316	380	444	508	572	636	700	764	828	892	956	1020
İ	61	61	125	189	253	317	381	445	509	573	637	701	765	829	893	957	1021
l	62	62	126	190	254	318	382	446	510	574	638	702	766	830	894	958	1022
- 1	63	63	127	191	255	319	383	447	511	575	639	703	767	831	895	959	1023

Figure 87. Multiplexer/R Addresses

	Land and Stare Instructions
Hexadecimal	Load and Store Instructions Load Accumulator (LD)
C0XX C1XX C2XX	Contents of CSL at EA (I+DISP) are loaded into A Contents of CSL at EA (XRI+DISP) are loaded into A Contents of CSL at EA (XR2+DISP) are loaded into A
C3XX C400XXXX C500XXXX C600XXXX C700XXXX	Contents of CSL at EA (XR3+DISP) are loaded into A Contents of CSL at EA (Addr) are loaded into A Contents of CSL at EA (Addr +XR1) are loaded into A Contents of CSL at EA (Addr +XR2) are loaded into A Contents of CSL at EA (Addr +XR3) are loaded into A
C480XXXX C580XXXX C680XXXX C780XXXX	Contents of CSL at EA (V in CSL at Addr) are loaded into A Contents of CSL at EA (V in CSL at "Addr +XR1") are loaded into A Contents of CSL at EA (V in CSL at "Addr +XR2") are loaded into A Contents of CSL at EA (V in CSL at "Addr +XR2") are loaded into A
	Double Load (LDD)
C8XX C9XX CAXX CBXX CC00XXX CC00XXX CD00XXX CF00XXX CF00XXX CF00XXX CF00XXX CC80XXX CD80XXXX CD80XXXX	Contents of CSL at EA (I + DISP) and EA+1 are loaded into A and Q Contents of CSL at EA(XR1 + DISP) and EA+1 are loaded into A and Q Contents of CSL at EA (XR2 + DISP) and EA+1 are loaded into A and Q Contents of CSL at EA (XR3 + DISP) and EA+1 are loaded into A and Q Contents of CSL at EA (Addr) and EA+1 are loaded into A and Q Contents of CSL at EA (Addr +XR1) and EA+1 are loaded into A and Q Contents of CSL at EA (Addr +XR2) and EA+1 are loaded into A and Q Contents of CSL at EA (Addr +XR2) and EA+1 are loaded into A and Q Contents of CSL at EA (V in CSL at Addr) and EA+1 are loaded into A and Q Contents of CSL at EA (V in CSL at "Addr +XR1") and EA+1 are loaded into A and Q Contents of CSL at EA (V in CSL at "Addr +XR1") and EA+1 are loaded into A and Q Contents of CSL at EA (V in CSL at "ADDR +XR2") and EA+1 are loaded into A and Q Contents of CSL at EA (V in CSL at "ADDR +XR2") and EA+1 are loaded into A and Q Contents of CSL at EA (V in CSL at "ADDR +XR2") and EA+1 are loaded into A contents of CSL at EA (V in CSL at "Addr +XR3") and EA+1 are loaded
CF80XXX	into A and Q
	Store Accumulator (STO)
D0XX D1XX D2XX D3XX D400XXX D500XXX D600XXX D700XXX D400XXX D480XXX D680XXX D680XXX D780XXX	Contents of A are stored in CSL at EA (I+DISP) Contents of A are stored in CSL at EA (XR1+DISP) Contents of A are stored in CSL at EA (XR2+DISP) Contents of A are stored in CSL at EA (XR3+DISP) Contents of A are stored in CSL at EA (Addr) Contents of A are stored in CSL at EA (Addr +XR1) Contents of A are stored in CSL at EA (Addr +XR2) Contents of A are stored in CSL at EA (Addr +XR2) Contents of A are stored in CSL at EA (Addr +XR3) Contents of A are stored in CSL at EA (V in CSL at Addr) Contents of A are stored in CSL at EA (V in CSL at "Addr +XR1") Contents of A are stored in CSL at EA (V in CSL at "Addr +XR2") Contents of A are stored in CSL at EA (V in CSL at "Addr +XR2")
	Double Store (STD)
D8XX D9XX DAXX DBXX DC00XXXX DC00XXXX DE00XXXX DF00XXXX DF00XXXX	Contents of A and Q are stored in CSL at EA (I+DISP) and EA+1 Contents of A and Q are stored in CSL at EA (XR1 +DISP) and EA+1 Contents of A and Q are stored in CSL at EA (XR2 +DISP) and EA+1 Contents of A and Q are stored in CSL at EA (XR3 +DISP) and EA+1 Contents of A and Q are stored in CSL at EA (Addr) and EA+1 Contents of A and Q are stored in CSL at EA (Addr +XR1) and EA+1 Contents of A and Q are stored in CSL at EA (Addr +XR2) and EA+1 Contents of A and Q are stored in CSL at EA (Addr +XR3) and EA+1 Contents of A and Q are stored in CSL at EA (V in CSL at Addr) and EA+1 Contents of A and Q are stored in CSL at EA (V in CSL at Addr) and EA+1 Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR1")
DD80XXXX	and EA+1
DE80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR2") and EA+1 Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR3") and EA+1
	Load Index (LDX)
60XX 61XX 62XX 63XX 6400XXXX 6500XXXX 6500XXXX 6700XXXX 6480XXXX 6580XXXX 6680XXXX	Load DISP into the Instruction Register Load DISP into Index Register 1 Load DISP into Index Register 2 Load DISP into Index Register 3 Load Addr into the Instruction Register Load Addr into Index Register 1 Load Addr into Index Register 2 Load Addr into Index Register 3 Load contents of CSL at Addr into the Instruction Register Load contents of CSL at Addr into Index Register 1 Load contents of CSL at Addr into Index Register 1 Load contents of CSL at Addr into Index Register 2
6780XXXX	Load contents of CSL at Addr into Index Register 3

Hovedoeimal	Load and Store Instructions
Hexadecimal	Store Index (STX)
68XX 69XX	Store I in CSL at EA (I+DISP) Store XRI in CSL at EA (I+DISP)
6AXX	Store XR2 in CSL at EA (I+DISP)
6BXX 6C00XXXX	Store XR3 in CSL at EA (I+DISP) Store I in CSL at EA (Addr)
6D00XXXX	Store XR1 in CSL at EA (Addr)
6E00XXXX	Store XR2 in CSL at EA (Addr)
6F00XXXX	Store XR3 in CSL at EA (Addr) Store I in CSL at EA (V in CSL at Addr)
6D80XXXX	Store XR1 in CSL at EA (V in CSL at Addr)
6E80XXXX 6F80XXXX	Store XR2 in CSL at EA (V in CSL at Addr) Store XR3 in CSL at EA (V in CSL at Addr)
0.000000	Store Status (STS)
2000	Store status of indicators in CSL at EA (I+DISP)
28XX 29XX	Store status of indicators in CSL at EA (XR1+DISP)
2AXX	Store status of indicators in CSL at EA (XR2+DISP)
2BXX 2C00XXXX	Store status of indicators in CSL at EA (XR3+DISP) Store status of indicators in CSL at EA (Addr)
2D00XXXX	Store status of indicators in CSL at EA (Addr+XR1)
2E00XXXX 2F00XXXX	Store status of indicators in CSL at EA (Addr+XR2) Store status of indicators in CSL at EA (Addr+XR3)
2C80XXXX	Store status of indicators in CSL at EA (V in CSL at Addr)
2D80XXXX 2E80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr +XR1") Store status of indicators in CSL at EA (V in CSL at "Addr +XR2")
2F80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr +XR3")
2C40XXXX	Clear storage protect bit in CSL at EA (Addr)
2C41XXXX 2D40XXXX	Write storage protect bit in CSL at EA (Addr) Clear storage protect bit in CSL at EA (Addr +XR1)
2D41XXXX	Write storage protect bit in CSL at EA (Addr +XR1)
2E40XXXX 2E41XXXX	Clear storage protect bit in CSL at EA (Addr +XR2) Write storage protect bit in CSL at EA (Addr +XR2)
2F40XXXX	Clear storage protect bit in CSL at EA (Addr +XR3)
2F41XXXX 2CC0XXXX	Write storage protect bit in CSL at EA (Addr +XR3) Clear storage protect bit in CSL at EA (V in CSL at Addr)
2CC1XXXX	Write storage protect bit in CSL at EA (V in CSL at Addr)
2DC0XXXX 2DC1XXXX	Clear storage protect bit in CSL at EA (V in CSL at "Addr +XR1") Write storage protect bit in CSL at EA (V in CSL at "Addr +XR1")
2EC0XXXX	Clear storage protect bit in CSL at EA (V in CSL at "Addr +XR2")
2EC1XXXX	Write storage protect bit in CSL at EA (V in CSL at "Addr +XR2") Clear storage protect bit in CSL at EA (V in CSL at "Addr +XR3")
2FC0XXXX 2FC1XXXX	Write storage protect bit in CSL at EA (V in CSL at "Addr +XR3")
	Load Status (LDS)
2000	Set CARRY and OVERFLOW indicators OFF
2001	Set OVERFLOW ON and CARRY OFF
2002	Set OVERFLOW OFF and CARRY ON Set CARRY and OVERFLOW indicator ON
	Arithmetic Instructions
	Add (A)
80XX	Add contents of CSL at EA (I+DISP) to A
81XX	Add contents of CSL at EA (XR1+DISP) to A
82XX 83XX	Add contents of CSL at EA (XR2+DISP) to A Add contents of CSL at EA (XR3+DISP) to A
8400XXXX	Add contents of CSL at EA (Addr) to A
8500XXXX 8600XXXX	Add contents of CSL at EA (Addr +XR1) to A Add contents of CSL at EA (Addr +XR2) to A
8700XXXX	Add contents of CSL at EA (Addr +XR3) to A
8480XXXX 8580XXXX	Add contents of CSL at EA (V in CSL at Addr) to A Add contents of CSL at EA (V in CSL at "Addr+XR1") to A
8680XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR2") to A
8780XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR3") to A
	Double Add (AD)
88XX 89XX	Add contents of CSL at EA (I+DISP) and EA+1 to A and Q Add contents of CSL at EA (XR1+DISP) and EA+1 to A and Q
8AXX	Add contents of CSL at EA (XR2+DISP) and EA+1 to A and Q
8BXX 8C00XXXX	Add contents of CSL at EA (XR3+DISP) and EA+1 to A and Q Add contents of CSL at EA (Addr) and EA+1 to A and Q
8D00XXXX	Add contents of CSL at EA (Addr+XR1) and EA+1 to A and Q
8E00XXXX 8F00XXXX	Add contents of CSL at EA (Addr+XR2) and EA+1 to A and Q Add contents of CSL at EA (Addr+XR3) and EA+1 to A and Q
8C80XXXX	Add contents of CSL at EA (V in CSL at Addr) and EA+1 to A and Q
8D80XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1
8E80XXXX	to A and Q Add contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1
	to A and Q

8F80XXXX	Arithmetic Instructions
	Add contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1 to A and Q
	Subtract (S)
90XX	Subtract contents of CSL at EA (I+DISP) from A
91XX 92XX	Subtract contents of CSL at EA (XR1+DISP) from A
93XX	Subtract contents of CSL at EA (XR2+DISP) from A Subtract contents of CSL at EA (XR3+DISP) from A
9400XXXX	Subtract contents of CSL at EA (Addr) from A
9500XXXX 9600XXXX	Subtract contents of CSL at EA (Addr+XR1) from A
9700XXXX	Subtract contents of CSL at EA (Addr+XR2) from A Subtract contents of CSL at EA (Addr+XR3) from A
9480XXXX	Subtract contents of CSL at EA (V in CSL at Addr) from A
9580XXXX 9680XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR1") from A
9780XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR2") from A Subtract contents of CSL at EA (V in CSL at "Addr+XR3") from A
	Double Subtract (SD)
98XX 99XX	Subtract contents of CSL at EA (I+DISP) and EA+1 from A and Q
9AXX 9AXX	Subtract contents of CSL at EA (XR1+DISP) and EA+1 from A and Q Subtract contents of CSL at EA (XR2+DISP) and EA+1 from A and Q
9BXX	Subtract contents of CSL at EA (XR3+DISP) and EA+1 from A and Q
9C00XXXX 9D00XXXX	Subtract contents of CSL at EA (Addr) and EA+1 from A and Q
9E00XXXX	Subtract contents of CSL at EA (Addr+XR1) and EA+1 from A and Q Subtract contents of CSL at EA (Addr+XR2) and EA+1 from A and Q
9F00XXXX	Subtract contents of CSL at EA (Addr+XR3) and EA+1 from A and Q
9C80XXXX	Subtract contents of CSL at EA (V in CSL at Addr) and EA+1 from A and Q
9D80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1 from A and Q
9E80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1 from A and Q
9F80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1 from A and Q
	Multiply (M)
A0XX	Multiply contents of CSL at EA (I+DISP) by A
AIXX	Multiply contents of CSL at EA (XR1+DISP) by A
A2XX A3XX	Multiply contents of CSL at EA (XR2+DISP) by A Multiply contents of CSL at EA (XR3+DISP) by A
A400XXXX	Multiply contents of CSL at EA (Addr) by A
A500XXXX A600XXXX	Multiply contents of CSL at EA (Addr+XR1) by A
A700XXXX	Multiply contents of CSL at EA (Addr+XR2) by A Multiply contents of CSL at EA (Addr+XR3) by A
A480XXXX	Multiply contents of CSL at EA (V in CSL at Addr) by A
A580XXXX A680XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR1") by A
A780XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR2") by A Multiply contents of CSL at EA (V in CSL at "Addr+XR3") by A
İ	Divide (D)
A8XX A9XX	Divide A and Q by contents of CSL at EA (I+DISP)
AAXX	Divide A and Q by contents of CSL at EA (XR1+DISP) Divide A and Q by contents of CSL at EA (XR2+DISP)
ABXX	Divide A and Q by contents of CSL at EA (XR3+DISP)
AC00XXXX AD00XXXX	Divide A and Q by contents of CSL at EA (Addr) Divide A and Q by contents of CSL at EA (Addr)
AE00XXXX	Divide A and Q by contents of CSL at EA (Addr+XRI) Divide A and Q by contents of CSL at EA (Addr+XR2)
AF00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR3)
AC80XXXX AD80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at Addr) Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR1")
AE80XXXX AF80XXXX	Divide A and Q by contents of CSL at EA(V in CSL at "Addr+XR2") Divide A and Q by contents of CSL at EA(V in CSL at "Addr+XR2")
	Logical And (AND)
0XX	AND contents of CSL at EA (I+DISP) with A
1XX 2XX	AND contents of CSL at EA (XR1+DISP) with A
3XX	AND contents of CSL at EA (XR2+DISP) with A AND contents of CSL at EA (XR3+DISP) with A
400XXXX	AND contents of CSL at EA (Addr) with A
500XXXX 600XXXX	AND contents of CSL at EA (Addr+XR1) with A AND contents of CSL at EA (Addr+XR2) with A
700XXXX	AND contents of CSL at EA (Addr+XR3) with A
480XXXX	AND contents of CSL at EA (V in CSL at Addr) with A
EONVVVV I	
580XXXX 680XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR1") with A
580XXXX 680XXXX 780XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR1") with A AND contents of CSL at EA (V in CSL at "Addr+XR2") with A AND contents of CSL at EA (V in CSL at "Addr+XR2") with A

Logical Or (OR) EBXX EPXX EPXX CPXX CPXX CPXX CPXX CPXX CP	
E9XX EAXX EAXX CAR contents of CSL at EA (XR1+D1SP) with A OR contents of CSL at EA (XR2+D1SP) with A OR contents of CSL at EA (XR3+D1SP) with A OR contents of CSL at EA (XR3+D1SP) with A OR contents of CSL at EA (XR3+D1SP) with A OR contents of CSL at EA (Addr+XR1) with A OR contents of CSL at EA (Addr+XR2) with A OR contents of CSL at EA (Addr+XR2) with A OR contents of CSL at EA (Addr+XR2) with A OR contents of CSL at EA (V in CSL at Addr) with EBBOXXXX CR contents of CSL at EA (V in CSL at "Addr+XR OR contents of CSL at EA (V in CSL at "Addr+XR OR contents of CSL at EA (V in CSL at "Addr+XR OR contents of CSL at EA (V in CSL at "Addr+XR OR contents of CSL at EA (XR1+D1SP) with A EOR contents of CSL at EA (XR2+D1SP) with A EOR contents of CSL at EA (XR2+D1SP) with A EOR contents of CSL at EA (XR2+D1SP) with A EOR contents of CSL at EA (Addr+XR1) with A EOR contents of CSL at EA (Addr+XR1) with A EOR contents of CSL at EA (Addr+XR2) with A EOR contents of CSL at EA (Addr+XR2) with A EOR contents of CSL at EA (Addr+XR2) with A EOR contents of CSL at EA (V in CSL at "Addr+XF1000XXXX EOR contents of CSL at EA (V in CSL at "Addr+XF1000XXXX EOR contents of CSL at EA (V in CSL at "Addr+XF1000XXXX EOR contents of CSL at EA (V in CSL at "Addr+XF1000XXXX EOR contents of CSL at EA (V in CSL at "Addr+XF1000XXXX EOR contents of CSL at EA (V in CSL at "Addr+XF1000XXXX EOR contents of CSL at EA (V in CSL at "Addr+XF1000XXXX EOR contents of CSL at EA (V in CSL at "Addr+XF1000XXXX EOR contents of CSL at EA (V in CSL at "Addr+XF1000XXXX EOR contents of CSL at EA (V in CSL at "Addr+XF1000XXXX EOR contents of CSL at EA (V in CSL at "Addr+XF1000XXXX EOR contents of CSL at EA (V in CSL at "Addr+XF1000XXXX EOR contents of CSL at EA (V in CSL at "Addr+XF1000XXXX EOR contents of CSL at EA (V in CSL at "Addr+XF1000XXXX EOR contents of CSL at EA (V in CSL at "Addr+XF1000XXXX EOR contents of CSL at EA (V in CSL at "Addr+XF1000XXXX EOR contents of A shift left the number of shift counts of Contents of A and Q shift left the number of sh	
FOXX FIXX FIXX EOR contents of CSL at EA (I+DISP) with A EOR contents of CSL at EA (XR1+DISP) with A EOR contents of CSL at EA (XR2+DISP) with A EOR contents of CSL at EA (XR2+DISP) with A EOR contents of CSL at EA (XR3+DISP) with A EOR contents of CSL at EA (Addr) with A EOR contents of CSL at EA (Addr) with A EOR contents of CSL at EA (Addr+XR1) with A EOR contents of CSL at EA (Addr+XR2) with A EOR contents of CSL at EA (Addr+XR3) with A EOR contents of CSL at EA (Addr+XR3) with A EOR contents of CSL at EA (V in CSL at Addr+XR50) EOR contents of CSL at EA (V in CSL at Addr+XR50) EOR contents of CSL at EA (V in CSL at Addr+XR50) EOR contents of CSL at EA (V in CSL at Addr+XR50) EOR contents of CSL at EA (V in CSL at Addr+XR50) EOR contents of CSL at EA (V in CSL at Addr+XR50) EOR contents of CSL at EA (V in CSL at Addr+XR50) EOR contents of CSL at EA (V in CSL at Addr+XR50) EOR contents of CSL at EA (V in CSL at Addr+XR50) EOR contents of CSL at EA (V in CSL at Addr+XR50) EOR contents of CSL at EA (V in CSL at Addr+XR50) EOR contents of CSL at EA (V in CSL at Addr+XR50) EOR contents of CSL at EA (V in CSL at Addr+XR50) EOR contents of CSL at EA (V in CSL at Addr+XR50) EOR contents of A shift left the number of shift counts Contents of A shift left the number of shift counts Contents of A shift left the number of shift counts Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A shift left the number of shift Contents of A shift left the number of shift Contents of A shift left the number of shift counts Contents of A shift left the number of shift counts Contents of A shift left the number of shift counts Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number o	I") with A 2") with A
F1XX F2XX F2XX F2XX EOR contents of CSL at EA (XR1+D1SP) with A EOR contents of CSL at EA (XR2+D1SP) with A EOR contents of CSL at EA (XR2+D1SP) with A EOR contents of CSL at EA (Addr) with A EOR contents of CSL at EA (Addr) with A EOR contents of CSL at EA (Addr) with A EOR contents of CSL at EA (Addr+XR1) with A EOR contents of CSL at EA (Addr+XR2) with A EOR contents of CSL at EA (Addr+XR2) with A EOR contents of CSL at EA (V in CSL at Addr) with EOR contents of CSL at EA (V in CSL at Addr) with EOR contents of CSL at EA (V in CSL at Addr+XR) EOR contents of CSL at EA (V in CSL at "Addr+XR") EOR contents of CSL at EA (V in CSL at "Addr+XR") EOR contents of CSL at EA (V in CSL at "Addr+XR") EOR contents of CSL at EA (V in CSL at "Addr+XR") EOR contents of A shift left the number of shift counts Contents of A shift left the number of shift counts Contents of A shift left the number of shift counts Contents of A shift left the number of shift counts Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A shift left the number of shift Contents of A shift left the number of shift Contents of A shift left the number of shift Contents of A shift left the number of shift Contents of A shift left the number of shift Contents of A shift left the number of shift Contents of A shift left the number of shift counts Contents of A shift left the number of shift counts Contents of A shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift	
Shift Left Logical A (SLA) Contents of A shift left the number of shift counts (Contents of A shift left the number of shift counts (Contents of A shift left the number of shift counts (Contents of A shift left the number of shift counts (Contents of A shift left the number of shift counts (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A shift left the number of shift (Contents of A shift left the number of shift (Contents of A shift left the number of shift (Contents of A shift left the number of shift (Contents of A shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A and Q shift left the number of shift (Contents of A a	R1") with A R2") with A
10°X 1100 1200 1300 1300 1300 1300 1300 1300	
1100 1200 1200 1200 1200 1200 1200 1200	
10*X 1180 Contents of A and Q shift left the number of shift 1280 Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Shift Left And Count A (SLCA) 10*X Contents of A shift left the number of shift counts 1140 Contents of A shift left the number of shift counts Contents of A shift left the number of shift counts Contents of A shift left the number of shift counts Shift Left And Count A & Q (SLC) 10*X Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift	in XR1 in XR2
1180 Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Shift Left And Count A (SLCA) 10°X Contents of A shift left the number of shift counts Contents of A shift left the number of shift counts Contents of A shift left the number of shift counts Contents of A shift left the number of shift counts Contents of A shift left the number of shift counts Shift Left And Count A & Q (SLC) 10°X Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift	
10*X 1140 1240 1240 1340 1340 10 10 10 10 10 10 10 10 10 10 10 10 10	counts in XR1 counts in XR2
1140 1240 1240 1240 1240 1240 1240 1240	
10*X 11C0 12C0 13C0 Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Shift Right Logical A (SRA)	in XR1 in XR2
11C0 Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Contents of A and Q shift left the number of shift Shift Right Logical A (SRA)	
	counts in XRI
18*X Contents of A shift right the number of shift counts	
1900 Contents of A shift right the number of shift counts 1A00 Contents of A shift right the number of shift counts 1B00 Contents of A shift right the number of shift counts	in XR1 in XR2
Shift Right A & Q (SRT)	
18*X Contents of A and Q shift right the number of shif 1980 Contents of A and Q shift right the number of shif 1A80 Contents of A and Q shift right the number of shif Contents of A and Q shift right the number of shif	counts in XR1
Rotate Right A & Q (RTE)	
18*X 19C0 1AC0 1BC0 Contents of A and Q rotate right the number of col 1AC0 Contents of A and Q rotate right the number of col Contents of A and Q rotate right the number of col Contents of A and Q rotate right the number of col Contents of A and Q rotate right the number of col	unts in XR1 unts in XR2

See Instruction Set Section for Meaning of Symbols

Hexadecimal	Branch Instructions
	Branch Or Skip On Condition (BSC or BOSC)
48*X 40*XXXXX 40*XXXXX 46*XXXXX 4F*XXXXX 4C*XXXXX 4D*XXXXX 4F*XXXXX 4F*XXXXX	Skip the next one-word instruction if ANY condition is sensed Branch to CSL at EA (Addr) on NO condition Branch to CSL at EA (Addr+XRI) on NO condition Branch to CSL at EA (Addr+XR2) on NO condition Branch to CSL at EA (Addr+XR3) on NO condition Branch to CSL at EA (V in CSL at Addr) on NO condition Branch to CSL at EA (V in CSL at "Addr+XR1") on NO condition Branch to CSL at EA (V in CSL at "Addr+XR1") on NO condition Branch to CSL at EA (V in CSL at "Addr+XR2") on NO condition Branch to CSL at EA (V in CSL at "Addr+XR2") on NO condition
	Branch And Store Instruction Register (BSI)
40XX	Store next sequential address in CSL at EA (I+DISP) and Branch to EA+1
41XX	to EA+1 Store next sequential address in CSL at EA (XR1+DISP) and Branch to EA+1
42XX	Store next sequential address in CSL at EA (XR2+DISP) and Branch to EA+1
43XX	Store next sequential address in CSL at EA (XR3+DISP) and Branch to EA+1
44*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr) and Branch to EA+1
45*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR1) and Branch to EA+1
46*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR2) and Branch to EA+1
47*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR3) and Branch to EA+1
44*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at Addr) and Branch to EA+1
45*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR1") and Branch to EA+1
46*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR2") and Branch to EA+1 If NO condition is true, store next sequential address in CSL at
4/ ^^^^	EA (V in CSL at "Addr+XR3") and Branch to EA+1
	Modify Index and Skip (MDX)
70XX 71XX 72XX 73XX 74XXXXX 7500XXXX 7600XXX 7700XXXX 7780XXXX 7580XXX 7680XXX 7780XXXX	ADD expanded DISP to 1 (no skip can occur) ADD expanded DISP to XR1 ADD expanded DISP to XR2 ADD expanded DISP to XR3 Add expanded positive DISP to CSL at Addr (Add to memory) Add Addr to XR1 Add Addr to XR1 Add Addr to XR2 Add Addr to XR3 Add expanded negative DISP to CSL at Addr (Add to Memory) Add Addr to XR3 Add expanded negative DISP to CSL at Addr (Add to Memory) Add V in CSL at Addr to XR1 Add V in CSL at Addr to XR2 Add V in CSL at Addr to XR3
3000	Walt (WAIT) WAIT until manual start or until completion of an interrupt
3000	subroutine
BAVV	Compare (CMP)
B0XX B1 XX B2XX B3XX B400XXXX B500XXX B700XXX B700XXX B480XXX B480XXX B580XXXX B780XXXX	Compare A with contents of CSL at EA (I+DISP) Compare A with contents of CSL at EA (XR1+DISP) Compare A with contents of CSL at EA (XR2+DISP) Compare A with contents of CSL at EA (XR3+DISP) Compare A with contents of CSL at EA (Addr) Compare A with contents of CSL at EA (Addr+XR1) Compare A with contents of CSL at EA (Addr+XR2) Compare A with contents of CSL at EA (Addr+XR3) Compare A with contents of CSL at EA (V in CSL at Addr) Compare A with contents of CSL at EA (V in CSL at "Addr+XR1") Compare A with contents of CSL at EA (V in CSL at "Addr+XR2") Compare A with contents of CSL at EA (V in CSL at "Addr+XR2") Compare A with contents of CSL at EA (V in CSL at "Addr+XR3")
	Double Compare (DCM)
B8XX B9XX BAXX	Compare A and Q with contents of CSL at EA (I+DISP) and EA+1 Compare A and Q with contents of CSL at EA (XR1+DISP) and EA+1 Compare A and Q with contents of CSL at EA (XR2+DISP) and EA+1

See Instruction	Set	Section	for	Meaning	of	Symbols
-----------------	-----	---------	-----	---------	----	---------

Hexadecimal	Branch Instructions
ввхх	Compare A and Q with contents of CSL at EA (XR3+DISP) and EA+1
BC00XXXX	Compare A and Q with contents of CSL at EA (Addr) and EA+1
BD00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR1) and EA+1
BE00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR2) and EA+1
BF00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR3) and EA+1
BC80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at Addr) and EA+1
BD80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr +XR1") and EA+1
BE80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr +XR2") and EA+1
BF80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr +XR3") and EA+1
	I/O Instructions
	Execute I/O (XIO)
08XX	Execute IOCC in CSL at EA (I+DISP) and EA+1
09XX	Execute IOCC in CSL at EA (XR1+DISP) and EA+1
0AXX	Execute IOCC in CSL at EA (XR2+DISP) and EA+1
OBXX	Execute IOCC in CSL at EA (XR3+DISP) and EA+1
0C00XXXX	Execute IOCC in CSL at EA (Addr) and EA+1
0D00XXXX 0E00XXXX	Execute IOCC in CSL at EA (Addr+XRI) and EA+1 Execute IOCC in CSL at EA (Addr+XR2) and EA+1
0F00XXXX	Execute IOCC in CSL at EA (Addr+XR3) and EA+1
0C80XXXX	Execute IOCC in CSL at EA (V in CSL at Addr) and EA+1
OD80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR1") and EA+1
0E80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR2") and EA+1
0F80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR3") and EA+1

APPENDIX B. INSTRUCTION EXECUTION TIMES

Average Instruction Execution Times. The times below pertain to the 2 μs core storage.* Add 2 μs to Execution Times when Indirect Addressing is specified.

		F	<u>= 0</u>	F =	<u>1</u>
		T=0	T≠0	T=0	_ T≠0
	LD	4 1/4	4 1/4	6	6 1/4
	STO	4 1/4	4 1/4	6	6 1/4
	LDD	6 1/4	6 1/4	8	8 1/4
	STD	6 1/4	6 1/4	8	8 1/4
	Α	4 1/2	4 1/2	6 1/4	6 1/2
	S	4 1/2	4 1/2	6 1/4	6 1/2
_	AD	6 3/4	6 3/4	8 1/2	8 3/4
(I)	SD	6 3/4	6 3/4	8 1/2	8 3/4
	M	15 1/4	15 1/4	1 <i>7</i>	17 1/4
	LD	42 3/4	42 3/4	44	44 1/2
	AND	4 1/4	4 1/4	6	6 1/4
	OR	4 1/4	4 1/4	6	6 1/4
	EOR	4 1/4	4 1/4	6	6 1/4
(2)-	BSI	2-4 1/4	2-4 1/4	2-6	2-6 1/4
9	LBSC	2	2	2-4	2-4 1/4
3)-	SLA	2 + N/4	2 + N/4	-	-
•	LSLT	2 + N/4	2 + N/4	-	-
4)	SLCA	2 + N/4	21/2 + N/4	-	-
_	LSLCAG		2 1/2 + N/4	-	-
③	SRA	2 + N/4	2 + N/4	-	-
	SRT	2 + N/4	2 + N/4	-	-
(3)	RTE	2 + N/4	2 + N/4	_	_
_	WAIT	2 ′	2	2	2
6	XIO	6 1/4 - 8 1/4	6 1/4 - 8 1/4	8-10	8 1/4 - 10 1/4
Ŭ	LDX	2 1/4	2 1/4	4 1/4	4 1/4
	STX	4 1/4	4 1/4	6	6
	MDX	2 1/2	2 1/2	10 1/4	4 3/4
	LDS	2	2	-	- ′
	STS	4 1/4	4 1/4	6	6 1/4
\bigcirc	CMP	4 1/2	4 1/2	6 1/4	61/2
Ψ.	DCM	6 3/4	6 3/4	8 1/2	8 3/4
	_	~		·	•

- \bigcirc Execution times include an average add time of 2 1/4 μs .
- \bigodot If a skip or branch is not executed, the instruction performs as a NOP with an execution time of 2.0 μs . If the skip or branch is executed, the second execution time is applicable.
- $\begin{tabular}{ll} \hline \end{tabular} N = P-4, \mbox{ where } P \mbox{ is the number of positions shifted, and } N \mbox{ must be positive or zero.} \\ \hline \end{tabular}$
- (4) If T \neq 0 and more than four (4) shifts occur, then 1/2 μ s is added to the execution time as shown to restore the specified index register from the shift counter.
- (5) A shift of 1,2,3, or 4 positions requires 2 μs, with 1/4 μs added for each additional shift position up to 15. Therefore, a shift of 5 positions takes 2.25 μs, a shift of 6 positions takes 2.5 μs, etc., up to 15 positions which takes 4.75 μs.

A shift of 16, 17, 18, or 19 positions requires 2.25 μs , with $1/4~\mu s$ added for each additional shift position up to 31. Therefore, a shift of 21 positions takes 2.5 μs , a shift of 22 positions takes 2.75 μs , etc., up to 31 positions which takes 5 μs .

- (6) The longer times apply to the Read and Write functions, the shorter times to all other functions.
- * Add 12.5% for 2.25 μs core storage or 100% for 4 μs core storage.

17439D

Internal Add Operation

The arithmetic section of the 1801/1802 P-C performs additions in successive machine cycles that are $1/4~\mu sec$ (2 or 2.25 μsec core storage) or $1/2~\mu sec$ (4 μsec core storage) in duration. The number of machine cycles required to complete the addition depends on the numbers being added and the resulting carries. As shown in Figure B-1, the augend

Machine		AUG	E١	10)	(A	-r	e g) a	nd	I	DI	DEN	1D	(D-	reg)	Со	ntents
Cycles			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	Αo		0	1	1	0	1	1	1	0	0	0	1	1	1	0	1	0
	Do		1	1	1	1	0	0	1	1	0	0	0	1	1	1	0	1
*First	Αı		1	0	0	1	1	1	0	1	0	0	1	0	0	1	1	1
	D		1	1	0	0	0	1	0	0	0	0	1	1	0	0	0	0
*Second	A ₂		0	1	0	1	1	0	0	1	0	0	0	1	0	1	1	1
	D_2		0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0
*Third	Аз		0	1	0	1	0	0	0	1	0	1	0	1	0	1	1	1
	D_3		0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
*Fourth	Α4		0	1	0	0	0	0	0	1	0	1	0	1	0	1	1	1
	D_4		0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
**Fifth	A ₅		0	1	1	0	0	0	0	1	0	1	0	1	0	1	1	1
	D ₅		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
* Occurs during the 2, 2.25, or 4 µs core storage cycle required to read the addend from core storage.																		

** Extra 1/4 or 1/2 µs machine cycle.

Figure B-1. Data Addition Example

(A register) and addend (D register) are exclusive ORed and ANDed each machine cycle. The Exclusive OR and AND functions are explained in the Arithmetic Instructions section of the manual.) The results of the Exclusive OR function are placed in the A register. The results of the AND function are ignored except for any carries that may occur. The carries are shifted one position to the left and placed in the D register. (These bits represent carries that would result from a normal binary add operation.) Each time a carry occurs, another machine cycle is initiated in which the A and D registers are Exclusive ORed and ANDed again. This process continues until

17443 A

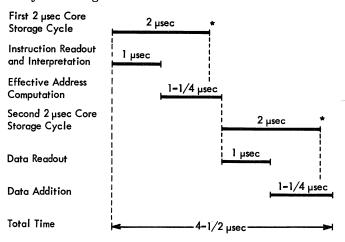
The length of each carry chain depends on the numbers involved and varies from 0 to 15. In Figure B-1, a carry chain of four (bit positions 2 through 5) caused five machine cycles. The first four of these cycles were included in the core storage cycle that read the addend from core storage. Only carry chain lengths of four and greater cause extra 1/4 or 1/2 μ sec machine cycles.

there are no further carries, at which time the cor-

rect sum exists in the A register.

Total Execution Time

Two core storage cycles are required in the execution of an Add instruction: one for instruction readout and effective address computation, and one for data readout and data addition. Figure B-2 is a sequence chart for the "average" add operation in which $F=0,\ T\neq 0$, and the carry chain length does not exceed four.



^{*}Cycle steals can occur here without stopping effective address computation or data addition.

17444

Figure B-2. Add Instruction Sequence Chart

Time Probabilities for the Addition of Data to the Accumulator

Table B-1 shows a mathematical analysis of all possible number pairs that can be added with the A and D registers:

Table B-1. Mathematical Analysis of Addition of all Possible Number Pairs

Carry Chain Length	Probability (%)	Cumulative (%)	Time (µsec)
0	1.3363	1.3363	2.00
1 1	9.8892	11.2255	2.00
2	27.0115	38.2370	2.00
3	27.71 <i>7</i> 8	65 .9 548	2.00
4	17.3 <i>7</i> 02	83.3250	2.25
5	8.9237	92.2487	2.50
6	4.2404	96.4891	2.75
7	1.9485	98.4376	3.00
8	0.8789	99.3165	3.25
9	0.3906	99. <i>7</i> 071	3.50
10	0.1709	99.8780	3. <i>7</i> 5
111	0.0732	99.9512	4.00
12	0.0305	99.9817	4.25
13	0.0122	99.9939	4.50
14	0.0046	99.9985	4.75
15	0.0015	100.0000	5.00

17445

The Carry Chain Length column lists all possible carry chain lengths up to the maximum of 15.

The <u>Probability</u> column contains percentage figures which are related to the Carry Chain Length. For example, a carry chain length of four occurs during 17.37% of all add operations.

The <u>Cumulative</u> column is merely a progressive summation of the Probability percentages. For

example, 83.32% of all add operations involve carry chain lengths of four or less; which, incidentally, is the basis for the Average Execution Time given in this appendix for Add instructions.

The <u>Time</u> column shows the time required for Data Readout and Data Addition (see Figure B-2) with a 2 μ sec core storage. The average Data Readout and Data Addition time for adding all possible numbers at random is 2.16 μ sec.

The Area, Function, and Modifier codes listed below are required for 1800 I/O operations (x indicates an unused bit position):

	AREA	FUN	MODIFIER
Console Data Entry Switches			
Sense Device - switch data to A-reg.	0 0 0 0 0	111	0 1 0 x x x x x
Read - switch data to core.	00000	0 1 0	$0\ 1\ 0\ x\ x\ x\ x$
Console Sense, Program Switches and CE Switches			
Sense Device - switch data to A-reg.	0 0 0 0 0	111	0 1 1 x x x x x
Read - switch data to core.	0 0 0 0 0	0 1 0	0 1 1 x x x x x
Console Interrupt			
Sense Device - console DSW to A-reg; indicators not reset - console DSW to A-reg; reset indicators	0 0 0 0 0	111 111	1 1 0 x x x x 0 1 1 0 x x x x 1
Operations Monitor			
Control - timer not reset - reset timer	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	1 0 0 1 0 0	1 1 1 x x x x x 0 1 1 1 x x x x 1
Interval Timers			
Control - timers started or stopped according to bits 0-2 of IOCC Address word.	0 0 0 0 0	100	0 0 1 x x x x x
Interrupt Mask Register			
Control - mask or unmask interrupt levels 0-13, depending on IOCC Address word bit positions 0-13. - mask or unmask interrupt levels 14-23,	00000	100	100xxxx0
depending on IOCC Address word bit positions 0-9.	0 0 0 0 0	100	100xxxx1
Program Interrupt			
 Control - turn on interrupt levels 0-13, depending on IOCC Address word bit positions 0-13. turn on interrupt levels 14-23, depending on IOCC Address word bit positions 0-9. 	0 0 0 0 0	1 0 0 1 0 0	1 0 1 x x x x 0 1 0 1 x x x x 1
ILSW			
Sense	0 0 0 0 0	0 1 1	$0\ 0\ 0\ 0\ 0\ 0\ 0$

NOTE: For Process Interrupt see Digital Input.

	AREA	<u>FUN</u>	MODIFIER
1053 Printer:			
First four 1053's: Write - individual 1053 specified by IOCC			
modifier bits 11-14 (y's).	$0\ 0\ 0\ 0\ 1$	0 0 1	хххуууух
Sense Device - 1816/1053 DSWs to A-reg. Individual units specified by IOCC bits 11-14 (y's), bit 15 (R)			
determines reset of indicators.	00001	111	хххуууу R
Second four 1053's: Area code is 01111.			
1816 Printer - Keyboard			
Read - single character to core storage.	00001	0 1 0	x x x x 0 0 1 0
Sense Device - 1816/1053 DSWs to Accumulator. Individual units specified by IOCC bits 11-14 (y's); bit 15 (R) determines			
reset of indicators.	0 0 0 0 1	111	$x \times x y y y y \cdot R$
Control - places keyboard in Ready status	00001	100	x x x x 0 0 1 0
1442 Card Read - Punch			
First 1442:			
Initialize Read - card columns to core storage. Where P is Packed Mode.	00010	110	x x x x x x x P
<u>Initialize Write</u> - core storage to card			
columns.	0 0 0 1 0	101	x x x x x x x x x
Control - IOCC bits 8 (S) and 14 (F) specify function. Where S is Stacker Select F is Feed Cycle.	00010	100	SxxxxxFx
Sense Device - DSW to Accumulator; bit 15 (R)			
determines reset of indicators.	0 0 0 1 0	111	$x \times x \times x \times R$
Second 1442: Area code is 10001.			
1054 and 1055 Paper Tape			
Read - one character from tape buffer to core			
storage.	0 0 0 1 1	0 1 0	x x x x x x x x x
<u>Write</u> - core storage to tape.	0 0 0 1 1	0 0 1	x x x x x x x x x
Control - One character from tape to tape buffer.	0 0 0 1 1	100	x x x 1 x x x x
Sense Device - DSW to Accumulator; bit 15 (R) determines reset of indicator.	00011	111	x x x x x x x R

		AREA	<u>FUN</u>	MODIFIER
1810 Disk Storage Drive	<u>e</u>			
<u>First 1810:</u>				
Initialize Read	-into-memory	00100	1 1 0	0 x x x x y y y
<u>Initialize</u> Read	-check	00100	1 1 0	1 x x x x y y y
Initialize Write	<u>e</u> -	0 0 1 0 0	101	$x \times x \times x y y y$
(ууу s	specify disk sector)			
	<u>Model)</u> - seek as specified by and modifier bit 13 (S).	00100	1 0 0	x
	fodel) - restore carriage to (Z) on; seek specified address off.	00100	100	x
	DSW to A-reg; bit 15 (R) set of indicators.	00100	111	x
$\frac{\text{Second and Third}}{\text{01000 and 01001, r}} \frac{1}{\text{r}}$	810's require Area codes of espectively.			
1627 Plotter				
<u>Write</u> - core s	torage to plotter.	00101	0 0 1	x x x x x x x x
<u> </u>	DSW to A-reg; bit 15 (R) set of indicators.	00101	111	x
1443 Printer				
<u>Initialize</u> Write	e - bit 15 (y) is used for			
space suppress	5.	00110	101	x x x x x x x y
<u>Control</u> - carr	iage control	0 0 1 1 0	100	$x \times x \times x \times x \times x$
	DSW to A-reg; bit 15 (R) set of indicators.	0 0 1 1 0	111	x x x x x x x R
2790 Adapter				
First Adapter	,			
(ZZZ	Loop - where -bits 12-15 (Z) specify segments to be ssed.	0 0 1 1 1	1 0 0	$0 \times \times \times Z \times Z \times Z$
Control - Start	*	0 0 1 1 1	1 0 0	1 x x x x x x x
- bits s	previously bypassed, then 9-11 (VVV) specify the nostic mode.	0 0 1 1 1	1 0 0	1 V V V S S S S
	12-15 (SSSS) simulate Area on response.			
word	where 13–15 (WWR) specify status as follows: 0 0 equals Adapter Status (DSW1) without reset.	0 0 1 1 1	1 1 1	xxxxWWR

	AREA	<u>FUN</u>	MODIFIER
0 0 1 equals Adapter Status (DSW1) with reset.		<i>i</i>	
0 1 0 equals DDSW2.			
1 0 0 equals DDSW3.			
Second Adapter: Area code is	1 0 0 1 1.		
Analog Input			
Direct Program Control:			
Write - AI point to ADC; Address word of IOCC specifies the core-storage location of the multiplexer address; where E is External Sync.	01010	0 0 i	ExxLHxxx
L is 8-bit resolution. H is 14-bit resolution.			
Read - ADC to core storage; Address word of IOCC is core-storage location specifying where the ADC reading will be stored; where S is Sequential	01010	010	S x x x x x x x
Program mode. <u>Sense Device</u> - DSW to A-reg;	0 1 0 1 0	111	CxxxxxxR
where C specifies Comparator or AI status word R bit resets indicators.			
Control (Blast Instruction)	0 1 0 1 0	1 0 0	x
Data Channel Control: Initialize Read - ADC readings to core storage where - E is External Sync. - T is Two DC operation. - L is 8-bit resolution. - H is 14-bit resolution.	0 1 0 1 0	1 1 0	ЕхТ L Нххх
Initialize Write - Address from core storage to multiplexer	0 1 0 1 0	1 0 1	x
The AI Expander Area code is 10000.			
Digital Input			
Direct Program Control:			
Read - DI or PI group to core storage; Bits 9-15 (A's) are DI addresses 64_{10} through 127_{10} or PI addresses 2_{10} through 25_{10} .	0 1 0 1 1	0 1 0	x
Sense Device - DSW, DI, or PISW to A-register. Bits 11-15 (B's) are DSW addresses 00000 or 00001 (reset indicators), PISW addresses 2 through 25 10 or DI addresses 64 10)		
through 127 ₁₀ . 10	0 1 0 1 1	1 1 1	хВВВВВВВ
Control (Blast Instruction)	0 1 0 1 1	1 0 0	x x 1 x x x x x

	AREA	<u>FUN</u>	MODIFIER
Data Channel Control: Initialize Read - where bits 8-10 (R's) specify the read mode.	0 1 0 1 1	1 1 0	RRRxxxx
Digital and Analog Output			
$\frac{\text{Direct Program Control:}}{\frac{\text{Write}}{\text{bits 9-15 (A's) are device addresses}}}$	0 1 1 0 0	0 0 1	x
Control - where bit 9 (B) initiates simultaneous transfer from buffer registers, bit 8 (P) initiates timing pulse for Pulse Output, and bit 10 (R) resets all DAO controls (Blast Instruction).	0 1 1 0 0	1 0 0	PBRxxxx
Sense Device - DSW to A-reg; bit 15 (R) determines reset of the indicators	0 1 1 0 0	1 1 1	x x x x x x x R
<u>Data Channel Control:</u> <u>Initialize Write</u> - core storage to DAO registers. Bits 8-10 (R's) specify write mode.	0 1 1 0 0	1 0 1	RRRxxxx
System/360 Adapter			
Initialize Write	0 1 1 0 1	1 0 1	x x x x x x x x
Initialize Read	0 1 1 0 1	1 1 0	x x x x x x x x
Sense Status - where bit 15 (R) determines reset of indicators.	0 1 1 0 1	1 1 1	0 x x x x x x R
Sense Word Count	0 1 1 0 1	1 1 1	1 x x x x x x x
Control (Reset	0 1 1 0 1	1 0 0	x x x x x x x x
Initialize Write - where -bit 10 (T) equals Tape Unit address 0 or 1bits 11 and 12 (D's) determine bit density for 7-track (ignored for 8-track): 00 for 800 BPI. 01 for 200 BPI. 10 for 556 BPIbit 13 (F) equals packed format for 7-track	0 1 1 1 0	1 0 1	XXTDDFxP
(ignored for 9-track)bit 15 (P) specifies even parity for 7-track (ignored for 9-track)			
Initialize Read - where -bit 10 (T) equals Tape Unit address 0 or 1bits 11 and 12 (D's) determine bit density for 7-track (ignored for 9-track): 00 for 800 BPI. 01 for 200 BPI. 10 for 556 BPI.	0 1 1 1 0	1 1 0	xxTDDFCP

	AREA	$\underline{\mathbf{FUN}}$	MODIFIER
 -bit 13 (F) equals packed format for 7-track (ignored for 9-track) -bit 14 (C) specifies read-while-correcting (ignored for 7-track or for initial 9-track record read). -bit 15 (P) specifies even parity for 7-track (ignored for 9-track). 			
Control - where bit 10 (T) equals Tape Unit address and bits 11 and 12 (D's) determine bit density for 7-track (ignored for 9-track).			
Rewind and unload	0 1 1 1 0	1 0 0	x x T x x 0 0 0
Write Tape Mark	0 1 1 1 0	1 0 0	x x T D D 0 0 1
Erase	0 1 1 1 0	1 0 0	x x T D D 0 1 0
Backspace	0 1 1 1 0	1 0 0	x x T 0 1 0 1 1
Rewind	0 1 1 1 0	1 0 0	x x T x x 1 0 0
Sense Device			
(1) Select Tape Unit specified by bit 10 (T),			
and Read DSW into A-register.	0 1 1 1 0	111	
(2) Select Tape Unit specified by bit 10 (T), Read	0 1 1 1 0	1 1 1	$x \times T 0 0 x \times 0$
DSW into A-register, and reset indicators.	0 1 1 1 0	1 1 1	
(3) Read Tape Channel work count into A-	0 1 1 1 0	1 1 1	$x \times T \times 0 \times x \times 1$
register.	0 1 1 1 0	1 1 1	** ** * 1 O
(4) Operation Stop (free tape channel) with bits		1 1 1	x x x 1 0 x x x
T, R, and y also performing functions 1, 2,			
and 3.	0 1 1 1 0	1 1 1	ххТу1ххR
			AAIYIXXN
Selector Channel			
Initialize Write (Start I/O) - where -bits 8 through 10 (C's) equal control unit addressbits 11 through 15 (D's) equal device	1 0 0 1 0	1 0 1	CCCDDDDD
address.			
Sense Status - where -bit 12 (S) specifies to suppress pollingbits 13 and 14) (W's) determine which status word to sense as follows: 00 for channel status.	1 0 0 1 0	1 1 1	xxxxSWWR
01 for unit address and status.			
10 for command address.			
11 for byte count.			
-bit 15 (R) determines the reset of indicators.			
Control (Halt I/O) - where -bits 8 through 10 (C's) equal control unit addressbits 11 through 15 (D's) equal device	1 0 0 1 0	1 0 0	СССDDDDD
address.			

	AREA	$\underline{ t FUN}$	$\underline{ ext{MODIFIER}}$
Communications Adapter (CA)			
First Communications Adapter			
Initialize Write - where -bit 8 (D) specifies diagnostic mode. -bit 9 (L) specifies the line adapter as follows: 0 for line adapter 0. 1 for line adapter 1. -bit 10 (C) specifies continue timer. -bit 11 (E) enables data terminal ready for World Trade applications. -bit 12 (T) specifies clear CA.	1 0 1 0 1	1 0 1	DLCETxxx
Sense Device - where -bit 8 (P) specifies program receive input. -bit 9 (L) specifies the line adapter as follows: 0 for line adapter 0. 1 for line adapter 1. -bit 10 (C) specifies continue timer. -bit 11 (E) enables END-character-or- ringing interrupt, and for World Trade application data terminal ready. -bit 12 (T) specifies clear CA. -bits 13 and 14 (W's) determine which status word is sensed as follows: 00 for status. 01 for diagnostic. 10 for byte count. -bit 15 (R) determines reset of indicators.	1 0 1 0 1	1 1 1	PLCETWWR
Second Communications Adapter: Area code is	1 0 1 1 0.		
Third Communications Adapter: Area code is	1 0 1 1 1.		
Fourth Communications Adapter: Area code is	1 0 1 0 0.		

APPENDIX D. DEVICE STATUS WORDS

Γ			\top	T	_			T						T	Τ	-		
	15	_	-	2	15		Į į		Sector Count	Sector Count Low	Not Ready	Printer	Segment 4 Bypass	Output Frame Fetch		3 reflects and ICC.	Any Error	AMAR 1
	4		:	4	14		Busy		Sector Count High	Sector Count High	Busy	Printer Busy	Segment 3 Bypass	Input Frame Fetch		ssed, DDSW and of TAR		AMAR 2
	2		2	2	13	†CE Not Ready	2 2 2 2 3 4	CE PT Punch Not Ready		"B" Model Access	₽ Z Z Z	Carriage Busy	Segment 2 Bypass	Update ISW		If all segments bypassed, DDSW3 reflects status of In-Bus instead of TAR and ICC.		AMAR 4
	71		5	71	12 I	† CE Busy	† P.C.E.	†CE PT Punch Busy	↑ CE Busy	† CE Busy	† CE Busy	+ CE Printer	Segment 1 Bypass	Area Station Capture or Command Update	, atom	If all se status of		AMAR 8
:			=	1] =			CE PT Reader Not Ready	† CE Not Ready	↑ CE Not Ready		+ CE Printer	(cor	Channe l Timer	1	ю		AMAR 16
2	2		2	2	10			CE PT Reader Busy		Seek Error		+ CE Carriage	Adapter Active	Buffer Cycle Command Update	Counter Bits	7		AMAR 32
٥			٥		6	Printer Parity Error		PT Reader Storage Protect	Data	Data				Data Buffer Write	Input Channel Counter Bits		DPC Relay Busy	AMAR 64
α			8		- 80	Keyboard Parity Error (1816)		PT Reader Parity Error		Write Select Error			Sync Fill Error	Data Buffer Read	— <u>i</u>	•	Cyc Steal, I SS, AMAR Busy	AMAR 128
7			7	1	7	Storage Protect Violation (1816)	Feed Check Read Station	PT Punch Not Ready	Data Error	Data Error				Channe I Interrupt Store	†		Overlap Conflict	AMAR 256
9			9		6	Keyboard Not Ready	Storage Protect Violation	PT Punch Busy	Storage Protect Error	Storage Protect Error		Parity	Loop Parity Error	Deactivate Channel		9	Overload	AMAR 512
2			5	Program	5	Printer Not Ready	Parity Error	PT Reader Not Ready	Parity Error	Parity Error		Channel 1	• Adapter Parity Error	Store		5	Parity Data Error	
4			4	ļ	4	Printer Busy	Operation Complete		Carriage Home	Carriage Home		Channel 12	• CPU Parity Error		I Table Address Register Bits	4	Parity Control Error	-
8			8	1	3		Last Card	• pt Punch Service Request	Disk Busy (R/W or Ctrl)	Disk Busy (R/W or Ctrl)		Channel 9	Storage Protect Error		l able Address	ო	Storage Protect Violation	AMAR SS MPX
2		Timer	2	Sense	2	Keyboard Request (1816)	Error	PT Punch Parity Error	Disk Not Ready	Disk Not Ready		• Printer Complete	No Frame	Position		2	DPC Rly Conv Complete	
-		Timer B	-	-	-	Keyboard Service Response (1816)		• PT Reader Service Request	Operation Complete	Operation Complete	Parity Error	Error	Command Reject	DC Cycle Steal Counter osition Position C C C C C C C C C C C C C C C C C C C		-	Conv Smplete	Low Out of Limit
0	Interrupt Request	Timer A	0	Ų.	•	• Printer Service Response		PT Reader Any Error	Any Error		Service Response	Transfer Complete		Position A		0	End of Table	High Out of Limit
FEATURE	Console Interrupt	Interval Timers	Data Entry Switches	Sense Switches		1810 Frinter-Keyboard 1053 Printer In First Group In Second Group	1442 Card Read Punch -First -Second	1054/1055 Paper Tape Reader/Punch	1810 Disk Storage "A" First Drive Second Drive Third Drive	1810 Disk Storage "B" First Drive Second Drive Third Drive	1627 Plotter		2790 Adapters -First -Second Status (DSW1)	Diagnostic (DDSW2)	Janostic	(DDSW3)	Analog Input -Basic -Expander	Comparator -Al Basic -Al Expander
AREA						15-	2- -71	ю	486	4 % 9	5	9	<u> </u>				01 - 61 - 61	<u></u>

15	DI Busy		D/AO Busy			Tape Busy or Not Ready			Unit Exception						
14						Tape Busy or Rewind			Unit Check						ä
13						Tape Indicator or Mark			Device End						ŧä
12				d Byte		At Load Point			Channel End						ializer Bit
11				360 Command Byte		Wrong Length Record			Busy						Serializer-Deserializer
01						CE Diagnostic Indicator			Control Unit End				Carrier On	mplement) —	Seric Bit
6		ned Groups).				• Operation Complete	Count		Status Modifier			- -	• Command Reject	 Byte Count (1's Complement)	ŧis
8		Process Interrupt Points (Customer Assigned Groups)		•	Complement)	Data Overrun Error	Word	Unit Operation- al	Attention	+ 3	.	Complement	Data Set Ready	Byte (tig.
7		pt Points (Cu		● End of Table	Count (1's	Data Bus Out or P-C Parity Error		Adapter Busy				Count (2's	Data Overrun		Receive Data Mark
9		rocess Interru		• Transfer End	Word	Tape Data Error		Incorrect Length	SS:	100	1607	Residual Byte	Data BCC Error		End Trigger
5				Storage Protect Violation		Storage Protect Violation Stop		Interface Control Check	Device Address				Parity Data Error		Text Trigger
4			Data Channel Active	• Data Check		Chain Stop		Channel Data Check					• End of Table		Trans- parent
3	• Command Reject		Command Reject	• Halt		End of Table		Program Check					END Character Decoded or Ringing		Clear to Send
2	• DI Scan Complete		• D & A Out Scan Complete	360 Command Stored	ļ	• Command Reject	1	Program Control Interrupt					Timed Out	ostic Bits -	Character Trigger
-	Storage Protect Violation		Pulse Output Timer	1800 Command Stored		Tape Unit 1 Select	Count	• Unit Status Pendina	Control Unit Address-				Storage Protect Violation	†† — CE Diagnostic Bit	Character Phase
0	• Parity Error	↓	• Parity Error	• Command Reject			00 = True Count 11 = 1's Complement	Not Operation-	▼ Cont				• Channel Stop		†† CE Diagnostic
FEATURE	Digital Input	PISW	Digital and Analog Output	S/360 Adapter	Adapter Word Counter	Tape Control Unit	TCU Word Counter	Se lector Channel Status	Unit Address and Status		SC COMEMBINA Address	SC Byte Count	CA Line Adapter(s) -First CA -Second CA -Third CA -Fourth CA	Adapter Byte Counter	Adapter Diagnostic
AREA	=		12	13		41		-81					22- 23- 20-		

Appendix D 225

Accumulator (A) 12	Analog Output (continued)
Accumulator Extension (Q) 12	Precision Voltage Reference (PVR) 157
ADC (See Analog-Digital Converter)	Analog-Digital Converter (ADC)
Add (A) 24	
Address Assignment	ADG G
Analog Input (1851) 208	
Area Codes 203	Buffer Amplifier 132 Data Word 131
Data Channel Assignment 205	
Digital and Analog Output 204	External Sync 132
Digital Input 204	Sample-and-Hold Amplifier 132
Initial Program Load (IPL) 205	Applications
Interrupt Level Status Word (ILSW) 207	Data Acquisition 2
Interrupt Levels 203	Data Collection and Plant Communications 3
Interval Timers 204, 205	Other Acquisition and Control 3
IOCC Modifiers for DIA's and PCA's 204	Process Control 1
IOCC Modifiers for DOC's and 1856's 206	Area Code Zero, (IOCC)
Multiplexer/R Address Table 210	Console Data Entry Switches 45
Multiplexer/S Address Table 209	Console Interrupt 46
Process Interrupt Status Word Assignment 207	Console Sense and Program Switches 45
Process Interrupt Status Words 204	Interrupt Mask Register 45
Analog Input (AI)	Interval Timers 44
Address Assignment 208	Operations Monitor 46
Analog Input Indicators 138	Programmed Interrupt 46
Analog-Digital Converter (ADC)	Area Codes 203
Analog Input Calibration 131	Arithmetic Factor Register (D) 12
Buffer Amplifier 132	Arithmetic Instructions
Data Word 131	Add (A) 24
External Sync 132	Divide (D) 27
Sample-and-Hold Amplifier 132	Double Add (AD) 24
Blast Instruction 138	Double Subtract (SD) 26
Comparator	Logical AND (AND) 28
	Logical Exclusive OR (EOR) 30
Comparison Cycle 133 Limit Words 133	Logical OR (OR) 29
	Subtract (S) 25
	Arithmetic Operations 9
~	AS (Area Station) 202.1
	Auto-Answer Function (CA) 162
75 1 61 1 6	
	Block Check Character (BCC) 166
	Block Check Character Register (BCCR) 167
Data Table Formats 137 Device Status Word 137	Branch Instructions
	Branch and Store Instruction Register (BSI) 37
Direct Program Control (DPC) 134	Branch or Skip On Condition (BSC or BOSC) 36
Execution Times 139	Compare (CMP) 40
Expander 133 I/O Control Commands 136	Double Compare (DCM) 41
	Modify Index and Skip (MDX) 39
	Wait (WAIT) 40
Interconnection of Analog Input Features 127	Bypass Controls (2790) 202.4
Multiplexer Overlap 129	Byte Count Register (BCR) 65
Thermocouple Operation 140	BCC Generation and Error Detection
Units and Features 126	Block Check Character Register (BCCR) 167
1851 Multiplexer Terminal	Cyclic Redundancy Checking (CRC-L6) 167
Differential Amplifier 130 Multiplexer/R 129	Longitudinal Redundancy Checking (LRC) 167
•	Vertical Redundancy Check (VRC) 167
Multiplexer/S 129 Signal Conditioning Florants 120	
Signal Conditioning Elements 130	CA (See Communications Adapter)
Analog Output (AO) Analog Output Driver Applifica 157	Card Feeding 95
Analog Output Driver Amplifier 157	Card Punch 95
Digital-to-Analog Conversion (DAC) 156	Card Read 95

CC (Channel Control, 2790) 202.14	Command Code (CCW)
Channel Address Buffer (CAB) 64	Control 184
Channel Address Register (CAR) 64	Read 184
Channel Address Register Check 64	Search 184
Channel Command Word (CCW)	Sense 184
Byte Count 181, 182	Test I/O 183
Command Chaining 185	Transfer-In-Channel (TIC) 184
Command Code	Write 184
Control 184	Commands and Responses (2790)
Read 184	AS Response Digit 202.8
Search 184	Control Commands 202.10
Sense 184	Control Responses 202.11
Test I/O 183	P-C Command Digit 202.8
Transfer-In-Channel (TIC) 184	Read Commands 202.8
Write 184	Read Responses 202.9
Command Code Assignment (CCW) 183	Table of 202.8
Data Address 185	Write Commands 202.9
Data Chaining 186	Write Responses 202.9
5	Commands, System/360 Adapter
	Control (System/360) 198
Flags	Control (1800) 202
Chain Command (CC) 183	Defined 195
Chain Data (CD) 181	Halt I/O (System/360) 200
Program Control Interruption (PCI) 183	Initialize Read (1800) 201
Skip 183	Initialize Write (1800) 202
Suppress Length Indication (SLI) 183	No-Operation (System/360) 200
Channel Sequence Handling (2790)	Read or Read Backward (System/360) 198
Broadcast Time Sequence 202.20	Sense (System/360) 198
Other Sequences 202.21	Sense (1800) 201
Read Sequence 202.20	· ·
Write Sequence 202.20	Table Of 195 Test I/O (System/360) 200
Channel Status Word (CSW)	, · · · /
Command Address 191	Write (System/360) 199
Count 191	Communications Adapter
Defined 180	Auto-Answer Function 162
Selector Channel Status	Block Check Character (BCC) 166
Adapter Busy 188	Block Check Character Register (BCCR) 167
Channel Data Check 188	BCC Generation and Error Detection 167
Incorrect Length 188	Clear (CA) 170
Interface Control Check 188	Code Structure-USASCII 164
Not Operational 187	Communication Facilities 162
Program Check 187	Continue Timer 169
Unit Operational 188	Control Characters and Sequences 162, 165
Unit Status Pending 187	Cycle-Steal Byte Count Word 170
Unit Address-Status	CA Code 162
Attention 188	Data Flow 166
Busy 190	Data Sets 162
Channel End 190	Description 161
Control Unit End 189	Device Status Words
	Byte Count 174
	Diagnostic 174
	Operating 172
Unit Check 190	Diagnostic Mode 169
Unit Exception 190	Diagnostic Transmit/Receive Data Tables 170
Character Coding	Enable 170
Communications Adapter 162	Extended Binary Coded Decimal Interchange Code 163
1054 Paper Tape Reader 104	Functional Description 166
1055 Paper Tape Punch 104	I/O Control Commands 169
1442 Card Read Punch 90	Interrupt 172
1443 Printer 99	Line Turnaround 165
1816 Keyboard 83	Receive Mode 176
1816/1053 Printer 84	Selectable Features 161
2401 and 2402 Magnetic Tape Units 112	Serializer/Deserializer (SERDES) 166
Command Chaining (CCW) 185	perializer/ Deperializer (periods) 100

Time and (Tabanasa A) 100	Control Characters and Sequences (CA) (Continued)
Timeout (Interrupt) 168	SOH (Start of Heading) 162
Transmit and Receive Sequences 177	STX (Start of Text) 165
Transmit Mode 175	SYN (Synchronous Idle) 162
Transmit Timeout (No Interrupt) 168	Control Commands (2790)
Transmit/Receive Sequence-Normal Mode 178	Begin Diagnostic 202.10
Transmit/Receive Sequence-Transparent Mode 179	Bypass 202.10
Transparent Mode Control 166	End Diagnostic 202.11
Communications Devices 4, 78	Restore 202.10
Comparator	Send Sync 202.10
Comparator Indicators 138	Table of 202.8
Comparison Cycle 133	Control Responses (2790)
Device Status Word 138	Begin Diagnostic Acknowledge 202.11
Limit Words 133	Bypass Acknowledge 202.11
Operational Description 132	End Diagnostic Acknowledge 202.11
Out-of-Limits Conditions 133	Restore Acknowledge 202.11
Compare (CMP) 40	Table of 202.8
Configuration, Illustration 6	Core Storage
Console	Addressing 8
Console Indicators 56	Hexadecimal Notation 8
Data Flow Displays 57	Index Registers (XR) 9
Display Procedures 58	Indirect Addressing 9
Emergency Pull Switch 53	Sizes and Cycle Times 8
Illustration 52	Wrap Around Addressing 8
Mode Switch 54	1803 Core Storage Unit 7
Program Failure-Restart 58	Customer Engineering Mode 62
Push-Button Switches and Lights 51	Cycle Steal 10
Toggle Switches 55	CA Trace Buffer 60
Console Indicators	CE Core Storage
Add 56	Addresses 60
Arithmetic Control 56	MPX Instructions 60
Arithmetic Sign 56	
Auxiliary Storage 56	CE Interrupt 71
Branch 56	DAC (See Digital Analan Gameratan)
Branch Out 57	DAC (See Digital-Analog Converter)
Carry and Overflow 57	Data Acquisition 1
Clock 50	Data Chaining 68
Cycle 56	Data Chaining (SC) 186
Cycle Steal Service 56	Data Channel Adapter
Format 57	Digital Input Group 148
Indirect Addressing 57	Operation With External Sync 148
Interrupt Levels 57	Operation Without External Sync 148
Interrupt Service 56	Data Channels (DC)
OP Code Check 56	Assignment 205
Operation Code 57	Byte Count Register (BCR) 65
Parity Bit 56	Cycle Steal 10
Parity Check 56	Described 10, 60
Shift Control 56	Functional Components
Storage Protect Bit 56	Channel Address Buffer (CAB) 64
Storage Protect Check 56	Channel Address Register (CAR) 64
Tag 57	Channel Address Register Check 64
Timers 57	I/O Control Commands (IOCC) 64
Zero Remainder 56	Operation 64
Continue Timer (CA) 169	Operation Examples
Control Characters and Sequences (CA)	Data Chaining 68
	Data Table 68
, , ,	Priority 64
ENQ (Enquiry) 165	Programming Note 64
EOT (End of Transmission) 165	Scan Control Register (SCR) 65
ETB (End of Transmission Block) 165	Service Time 64
EXT (End of Text) 165	Sharing 206
ITB (Intermediate Transmission Block) 165	Word Count Register (WCR) 65
NAK (Negative Acknowledgment) 165	Data Flow
PAD Character 165	P-C 12

Data Flow (Continued)	Digital and Analog Output (DAO) (Continued)
System 4	Digital Output
Data Flow Displays	Electronic Contact Operate 156
Address Register 57	Pulse Output 156
Data Register 58	Register Output 156
Display Address Register Switch 58	External Sync 154
Display Data Register Switch 58	I/O Control Commands 157
Permanent Register Displays 58	Organization 154
Data Flow Examples (P-C)	Schematic of 155
One-Word Instruction 13	System Capacity 154
Two-Word Instruction, Direct Addressing 14	Digital Input (DI)
Two-Word Instruction, Indirect Addressing 14	Address Assignment 204
Data Processing Devices 4, 78	Addressing
Data Representation 7	Digital Input 150
Data Sets (CA) 162	Process Interrupt 150
Data Table 68	Pulse Counter 150
Data Transmission Arrangement (2790)	Blast Instruction 151
Area Station Address 202.7	Contact 149
Control 202.7	Data Channel Adapter 148
Data Field 202.7	Data Table Formats 152
Device Address 202.7	Data Table Layouts 152
Frame Field Code Structure 202.6	Device Status Word 153
Start 202.6	Digital Input Adapter 148
Data Transmission Format (2790) 202.5	Digital Input Channel 149
Device Status Word (DSW)	I/O Control Commands 151
Analog Input 137	Process Interrupt 149
Byte Count (CA) 174	Pulse Counter 146, 149
Command Address (Selector Channel) 191	Schematic 147
Count (Selector Channel) 191	Voltage 149
DDSW2 (2790) 202.18	Digital Output (DO)
DDSW3 (2790) 202.18	Electronic Contact Operate 156
Diagnostic (CA) 174	Pulse Output 156
Digital and Analog Output 159	Register Output 156
Digital Input 153	Direct Program Control (DPC)
DSW1 (2790) 202.18	Data Overrun 64
Operating (CA) 172	Described 60
Programming Note 81	Device Busy 63
Selector Channel Status 187	I/O Control Commands (IOCC) 63
System/360 Adapter 196	Operation 63
Table of 224	Display Procedures 58
Unit Address-Status (Selector Channel) 188	Divide (D) 27
1053 Printer 85	DLE (Data Link Escape) 165
1054 Paper Tape Reader 106	DMR (Diagnostic Mode Register, 2790) 202.4
1055 Paper Tape Punch 106	Double Add (AD) 24
1442 Card Read Punch 94	Double Compare (DCM) 41
1443 Printer 102	Double Load (LDD) 17
1627 Plotter 111	Double Store (STD) 19
1810 Disk Storage 124	Double Subtract (SD) 26
1816 Keyboard-Printer 88	DRR (Diagnostic Response Register, 2790) 202.4
2401 and 2402 Magnetic Tape Units 115	DSW (See Device Status Word)
Diagnostic Controls (2790) 202.4	
Digital-Analog Converter (DAC) 156	Effective Address Generation (EA) 11
Digital and Analog Output (DAO) 154	Emergency Pull Switch 53
Address Assignment 204	ENQ (Enquiry) 165
Analog Output	EOT (End of Transmission) 165
Analog Output Driver Amplifier 157	Error Logs 60
Digital-to-Analog Conversion 156	Error Recovery Procedure (ERP, 2790)
Precision Voltage Reference (PVR) 157	AS Address Check 202.22
Blast Instruction 160	Control Check 202.22
Data Table Formats 158	Data Check 202.22
Data Table Layouts 158	Device Address Check 202.22
Davida Status Ward 150	General 202.21

Error Recovery Procedure (ERP, 2790) (Continued)	I/O Control Command (IOCC) (Continued)
Sync Frame Check 202.22	1443 Printer 101
Error Statistics 60	1627 Plotter 110
ETB (End of Transmission Block) 165	
ETX (End of Text) 165	1810 Disk Storage 122
Execute I/O (XIO)	1816 Printer-Keyboard 84, 87
	2401 and 2402 Magnetic Tape Units 115
Area Code Zero (IOCC) 44	2790 Adapter 202.17
I/O Control Command (IOCC) 42	
XIO Execution Data Flow 43	I/O Device Addressing 217
External Interrupt Polling 71	ILSW (See Interrupt Level Status Word)
External Sync	Implementation of BSC
Analog Input 132	Receive Mode
Digital and Analog Output 154	DLE 177
Digital Input 148	ENQ, NAK, EOT, DLE-STICK 176
	ETB, ITB and ETX 176
Frame Processing (2790) 202.3	•
Function Description	SOH and STX 176
	SYN 176
Communications Adapter (CA) 166	Transmit Mode
Digital and Analog Output (DAO) 154	$\rm DLE = 176$
Digital Input (DI) 146	ETB, ETX, ITB, ENQ 175
P-C Console 51	PAD Character 176
Selector Channel 180	SOH and STX 175
1053 Printer 82	SYN 175
1054 Paper Tape Reader 104	Index Registers (XR) 9
1055 Paper Tape Punch 105	Indirect Addressing 9
1442 Card Read Punch 90	Initial Program Load (IPL)
1443 Printer 98	Assignment 205
1627 Plotter 108	Described 51
1810 Disk Storage 120	
	1054 Paper Tape Reader 107
· ·	1442 Card Read Punch 91, 95
2401 Magnetic Tape Unit 112	Initialize (CA)
2790 Adapter 202.2	Clear (CA) 170
	Continue Timer 169
ICC (Input Channel Counter, 2790) 202.3	Diagnostic Mode 169
I/O Control	Enable 170
Customer Engineering Mode 62	Initiation of Operations (Selector Channel) 191
Data Channel (DC) 60	Input/Output
Device Addressing 217	Communications Devices 78
Direct Program Control (DPC) 60	Control
On-Line Maintenance 60	Data Channel 78
I/O Control Command (IOCC)	
Address Field 43, 79	Direct Program 79
	Data Processing Devices 78
Analog Input 136	Device Status Word (DSW) 81
Area Field 42, 79	Devices and Control Units 78
Communications Adapter 169	Instruction (XIO) 79
Control 80	Interface 78
Customer Engineering Mode 80	Interrupts 81
Digital and Analog Output 157	Termination 81
Digital Input 151	Instruction Execution Times
Format 42	Internal Add Operation 215
Function Field 43, 80	Time Probabilities 215
Initialize Read 80	Total Execution Time 215
Initialize Write 80	
	Instruction Formats
•	Illustrations 10
Read 80	Symbology 10, 16
Selector Channel 180	Instruction Register (I) 12
Sense Device Status Word (DSW) 80	Instruction Set
Sense Interrupt Level 80	Add (A) 24
Write 80	Branch and Store Instruction Register (BSI) 37
1053 Printers 84	Branch or Skip on Condition (BSC or BOSC) 36
1054 Paper Tape Reader 105	Compare (CMP) 40
1055 Paper Tape Punch 105	Divide (D) 27
1442 Card Read Punch 92	Double Add (AD) 24

Instruction Set (Continued)	Keyboard Functional Description 86
Double Compare (DCM) 41	Keys (See Switches and Lights)
Double Load (LDD) 17	
Double Store (STD) 19	Last Card Sequence (1442) 96
Double Subtract (SD) 26	LCCB (Loop Channel Control Block, 2790)
Execute I/O (XIO) 42	Defined 202.12
Load Accumulator (LD) 17	Format Illustration 202.13
Load Index (LDX) 20	Address and Control Words (Error Frame) 202.15
,	Address Word (Active Frame)
	AS Address (Bits 0-7) 202.12
Logical AND (AND) 28	Device Address (Bits 8-15) 202.12
Logical Exclusive OR (EOR) 30	Buffer Address Word 202.14
Logical OR (OR) 29	Byte Count Word 202.14
Modify Index and Skip (MDX) 39	Channel Sense Word
Rotate Right A & Q (RTE) 34	AS Address Check (Bit 2) 202.14
Shift Left and Count A (SLCA) 32	
Shift Left and Count A & Q (SLC) 33	2500 0000000000000000000000000000000000
Shift Left Logical A (SLA) 31	OI Diagnostic (
Shift Left Logical A & Q (SLT) 31	Channel Timed Out (Bit 9) 202.15
Shift Right A & Q (SRT) 34	Data Check (Bit 5) 202. 15
Shift Right Logical A (SRA) 33	Data Storage Protect (Bit 8) 202.15
Store Accumulator (STO) 18	Device Address Check (Bit 3) 202.14
Store Index (STX) 20	Frame Control Check (Bit 4) 202.15
Store Status (STS) 21	Sequence Normal End (Bit 0) 202.14
Subtract (S) 25	Sequence Unusual End (Bit 1) 202.14
Table of 16, 211	Synce Frame Check (Bit 10) 202.15
Wait (WAIT) 40	Unconditional Interrupt (Bit 7) 202.15
Interface, I/O 78	Channel Timer Count Word 202.15
Internal Interrupt 70	Control Word (Active Frame)
Interrupt	Buffer Available (Bit 0) 202.12
CE 71	CC Command (Bits 4-7) 202.14
Handling (2790) 202.21	Channel Active (Bit 3) 202.12
Indicator Identification 77	Data (Bits 8-15) 202.14
Internal Interrupt 70	Process Frame (Bit 2) 202.12
Interrupt Level Status Word (ILSW) 70	Unconditional Interrupt (Bit 1) 202.12
Level Assignment 203	Words 9 through 16 202.15
Level Masking 71	LCIB (Loop Channel Interrupt Block)
Levels 70	Format Illustration 202.16
Operating Characteristics 70	Interrupt Status Hold Word 202.16
- Po	Interrupt Status Word 202.16
Philosophy 70	Level Masking 71
Polling 71	Load Instructions
Program Identification of 75	Double Load (LDD) 17
Programmed 72	Load Accumulator (LD) 17
Programmed Operation 74	Load Index (LDX) 20
Programming Details 75	Load Status (LDS) 22
Recognition 74	Logical AND (AND) 28
Status Words 72	Logical Exclusive OR (EOR) 30
Table 71	
Trace 71	
Interrupt Level Status Word (ILSW)	Loop Channels (2790) 202.6
Address Assignment 207	· · · · · · · · · · · · · · · · · · ·
Branch Table 76	input 2 time to the
Defined 70, 73	Operation (2790) 202.4
Interval Timers	Output Functions (2790) 202.3
Assignment 204, 205	Segments 202.1
DSW Indicators 47	
IOCC Format 47	Maintenance, On-Line
Locations 47	Customer Engineering Mode 62
Time Base 47	CA Trace, Buffer 60
ISHW (Interrupt Status Hold Word, 2790) 202.16	CE Core Storage 60
ISW (Interrupt Status Word, 2790) 202.16	CE Core Storage Addresses 63
ITB (Intermediate Transmission Block) 165	CE Interrupt 63

Maintenance, On-Line (Continued)	Read Responses (2790)
Error Logs 60	Read Command Acknowledge 202.9
Error Statistics 60	Read Data Acknowledge 202.9
Mode Switch	Read Data Request 202.9
Display 55	Read End Acknowledge 202.9
Load 55	Read End Request 202.9
Run 54	Read Null Acknowledge 202.9
Single Instruction 54	Read Request 202.9
Single Instruction With Cycle Steal 54	Table of 202.8
Single Step 54	Registers, (P-C)
Single Storage Cycle 54	Accumulator (A) 12
Trace 55	Accumulator Extension (Q) 12
Modify Index and Skip (MDX) 39	Arithmetic Factor Register (D) 12
F (= ==,	Instruction Register (I) 12
NAK (Negative Acknowledgment) 165	OP Register (OP) 12
(2.5 Barrier - 1 and 11	C1 10 C
Operations Monitor	G(
IOCC 50	C1
Programming Note 50	
Other Acquisition and Control 3	
Overflow and Carry Indicators 9	Resistance Bulb Thermometer (RBT) 141
OP Register (OP) 12	Rotate Right A & Q (RTE) 34
or negister (or) 12	SAD (See Stemans Address D
P-C Console (See Console)	SAR (See Storage Address Register)
P-C Data Flow	Scan Control Register (SCR) 65
	Segment Terminator (2790) 202.4
Data Transfer, 18 Bits 13	Selector Channel
Illustration 12 One-Word Instruction 13	Channel Command Word
	Byte Count 181
Two-Word Instruction, Direct Addressing 14	Command Code Assignment 183
Two-Word Instruction, Indirect Addressing 14	Data Address 185
P-C Registers 11	Flags and Command Codes 181
PAD Character (CA) 165	Channel Status Word
Parity 49	Command Address 191
Power Failure Protect 50	Count 191
Printer Functional Description 82	Selector Channel Status 187
Process Control 1	Unit Address-Status 188
Process I/O Features 4	Command Chaining 185
Process Interrupt	Data Chaining 186
Adapter 149	I/O Control Commands
Contact 149	Control (Halt I/O) 180
Voltage 150	Initialize Write (Start I/O) 181
Process Interrupt Status Word (PISW)	Sense Device (Sense Channel Status) 181
Address Assignment 204	Sense Interrupt 180
Assignment Points 207	Initiation of Operations 191
Bit Positions Assignment 73	Mode of Operation 180
Indicators 73	Self-Describing Blocks 186
Processor-Controller (P-C) 3, 7	Sense Bytes 184
Program Failure-Restart 58	Skip 186
Programmed Interrupts	Termination of Operations 192
IOCC 72	Selector Channel Status Word 73
Programming Note 72	Self-Describing Blocks 186
Pulse Counter	Sense Diagnostic DSW Usage (2790) 202.19
Adapter 149	Serializer/Deserializer (SERDES) 166
Defined 146	Shift Control Counter (SC) 12
Operation 149	Shift Instructions
,	Rotate Right A & Q (RTE) 34
Read Commands (2790)	Shift Left and Count A (SLCA) 32
Read 202.8	Shift Left and Count A & Q (SLC) 33
Read Data 202.8	Shift Left Logical A (SLA) 31
Read End 202.8	Shift Left Logical A & Q (SLT) 31
Read Null 202.8	Shift Right A & Q (SRT) 34
Table of 202.8	Shift Right Logical A (SRA) 33

Skip 186	Thermocouple Operation (Continued)
SOH (Start of Heading) 162	Resistance Bulb Thermometer (RBT) 141
Status Words	Thermocouple Temperature 144
Defined 72	Toggle Switches (Console)
Device Status 73	Check Stop 55
Interrupt Level Status 73	Data Entry Switches 55
Process Interrupt Status 73	Disable Interrupt 55
Relationship of 74	Operations Monitor 55
Selector Channel Status 73	Sense and Program 55
Storage Address Register (SAR) 11	Write Storage Protect Bits 55
Storage Buffer Register (B) 12	Trace Interrupt 71
Storage Protection 48	Transparent Mode Control (CA) 166
Store Instructions	
Double Store (STD) 19	Usage Meter
Store Accumulator (STO) 18	1442 Card Read Punch 97
· · · ·	1443 Printer 103
	2401 and 2402 Magnetic Tape Units 119
,	aror and aroa stagnesses cape cares
STX (Start of Text) 165	Wait (WAIT) 40
Subtract (S) 25	Word Count Register (WCR) 65
Switches and Lights Console Indicators 56	Wrap Around Addressing 8
	Write Commands (2790)
Dataflow Displays 57	Table of 202.8
Pushbutton, Console 51	Write 202.9
Toggle, Console 55	Write Data 202.9
1442 Card Read Punch 92	Write End 202.9
1443 Printer 100	Write Null 202.9
1627 Plotter 109	Write Responses (2790)
1816 Keyboard 86	Table of 202.8
SYN (Synchronous Idle) 162	Write Command Acknowledge 202.10
System Data Flow 4	Write Data Acknowledge 202.10
System Description	Write Data Request 202.10
Communications Devices 4	Write End Acknowledge 202.10
Configuration, Illustration 6	Write End Request 202.10
Data Flow 4	Write Null Acknowledge 202.10
Data Processing I/O Units 4	<u> </u>
Process 1/O reatures 4	XIO Execution Data Flow 43
Processor-Controller (P-C) 3, 7	AIO Execution Data Flow 45
System/360 Adapter	1053 Printer
Addressing 195	Character Format 82
Commands	Device Status Word 85
Defined 195	I/O Control Commands (IOCC) 84
Table of 195	Interrupt Indicator 85
Mode of Operation 195	
Programming 202	Non-Interrupt Indicators 85 Printer Functional Description 82
Status Summary (System/360) 200	-
System/360 Status Byte 196	Printer-Character Coding 84
1800 Device Status Word 196	1054 Paper Tape Reader
System/360 Status Byte 196	Character Code 104
	Device Status Word 106
Tape Mark 114	I/O Control Commands (IOCC) 105
TAR (Table Address Register, 2790) 202.17	Initial Program Load (IPL) 107
Termination of Operations (Selector Channel)	Interrupt Indicators 106
At Operation Initiation 192	Non-Interrupt Indicators 106
With Data Transfer 193	1055 Paper Tape Punch
With Halt I/O 193	Character Code 104
Without Data Transfer 192	Device Status Word 106
Thermocouple Operation	I/O Control Commands (IOCC) 105
Calibration Data 140	Interrupt Indicators 106
Cold Junction Temperature 144	Non-Interrupt Indicators 106
Conversion Accuracy 142	1442 Card Read Punch
Conversion Example 142	Card Feeding 95
Converting Thermocouple Characteristics 142	Card Image Mode 91
Measuring Thermocouple Signals 140	Card Punch 95

1442 Card Read Punch (Continued)	1816 Printer-Keyboard (Continued)
Card Read 95	Keyboard
Character Coding 90	Function Keys 86
Data Channel Assignment 90	Lights 86
Device Status Word 94	Operating Procedure 87
Error Recovery 96	Non-Interrupt Indicators 89
Functional Description 90	Printer Functional Description 82
Functional Keys 92	Printer-Character Coding 84
I/O Control Commands (IOCC) 92	1851 Multiplexer Terminal
Initial Program Load (IPL) 91, 95	Description 128
Interrupt Indicator 93	Differential Amplifier 130
Last-Card Sequence 96	Functions 129
Lights 92	Multiplexer Overlap 129
Non-Interrupt Indicators 94	Multiplexer/R 129
Packed Mode 91	Multiplexer/S 129
Power Down 92	Signal Conditioning Elements 130
Usage Meter 97	2401 and 2402 Magnetic Tape Units
1443 Printer	Data Formats 112
Carriage	Device Status Word 115
Control Characters 100	Error Check Registers 113
Operation 99	Error Correction (9-Track) 114
Character Codes 99 .	I/O Control Commands (IOCC) 115
Character Sets 100	Interrupt Indicators 117
Core Storage Word Format 98	Non-Interrupt Indicators 118
Device Status Word 102	Parity 114
Functional Description 98	Programming Note 114, 119
I/O Control Commands (IOCC) 101	Scan Control 114
Interrupt Indicators 102	Tape Control Functions 116
Keys and Lights 100	Tape Mark 114
Non-Interrupt Indicators 102	Tape Unit Selection 115
Printing Speeds 98	Timings 113
Usage Meter 103	Usage Meters 119
1627 Plotter	1802 Registers 112
Device Status Word 111	2790 Adapter
I/O Control Commands (IOCC) 110	Adapter Table Format 202.11
Interrupt Indicator 111	Area Station Address Field 202.7
Non-Interrupt Indicators 111	Bit Synchronization 202.3
Operating Characteristics 108	Bypass Controls 202.4
Operating Controls 109	Byte Synchronization 202.6
Output Record Control 109	CC (Channel Control) 202.14
Paper and Pen Motions 108	Channel Sequence Handling 202.19
1803 Core Storage Unit 7	Commands and Responses
1810 Disk Storage	Control Commands 202.10
Access Time 121	Control Responses 202.11
Data Transfer Checking	Read Commands 202.8
Data Overrun 122	Read Responses 202.9
Modulo 4 122	Write Commands 202.9
Parity 122	Write Responses 202.9
Storage Protect 122	Configuration 202.1, 202.2
Device Status Word 124	Control Field 202.7
Disk Organization and Capacity 120	Cycle Steal Controls 202.3
Functional Description 120	Data Field 202.7
I/O Control Command (IOCC) 122	Data Transmission Format 202.5
Interrupt Indicator 125	Device Address Field 202.7
Non-Interrupt Indicators 125	Device Status Word (DSW) 202.18
Timing 121	Diagnostic Controls 202.4
1816 Printer-Keyboard	Error Recovery Procedure (ERP) 202.21
Character Coding 83	Features 202.1
Character Format 82	Frame
Device Status Word 88	Cycle 202.3
I/O Control Commands (IOCC) 84, 87	Defined 202.3
Interrupt Indicators 88	MVM1 U