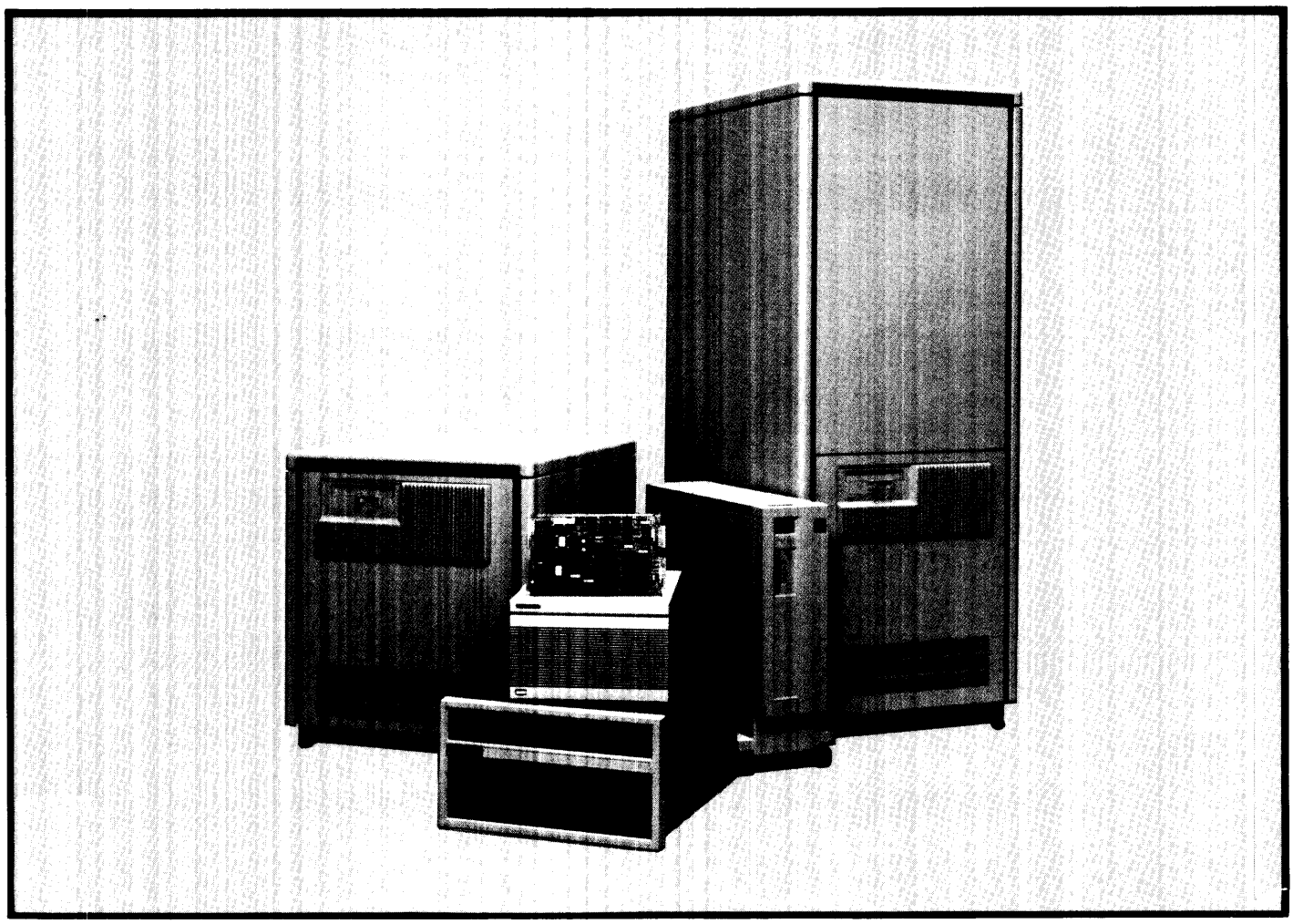
HEWLETT PACKARD

HP 1000 A400 Computer

Engineering and Reference Documentation

HP 1000 A-Series



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First Edition ..... Jul 1990 .....

Preface

This manual contains engineering and reference information for the HP 1000 A400 computer. Information is provided in this manual for each section of the A400 Board (the processor chip, the on-board memory and memory controller, and the on-board I/O), optional memory array cards, backplane, and power supply. I/O interface cards are not covered in this document since the detailed information is provided in other manuals.

This manual is organized into the following chapters:

Chapter 1 – HP 1000 A400 Computer

Chapter 2 – A400 Board General Description

Chapter 3 – Processor Chip

Chapter 4 – Memory Control

Chapter 5 – On-Board I/O

Chapter 6 – Memory Arrays

Chapter 7 – Backplane (Including I/O Requirements and Signal Timing)

Chapter 8 – Power Supply

Appendix A – Bus Control Timing Diagrams

Appendix B – Memory Control Timing Diagrams

Appendix C – Processor Memory Access Cases

Documentation Map

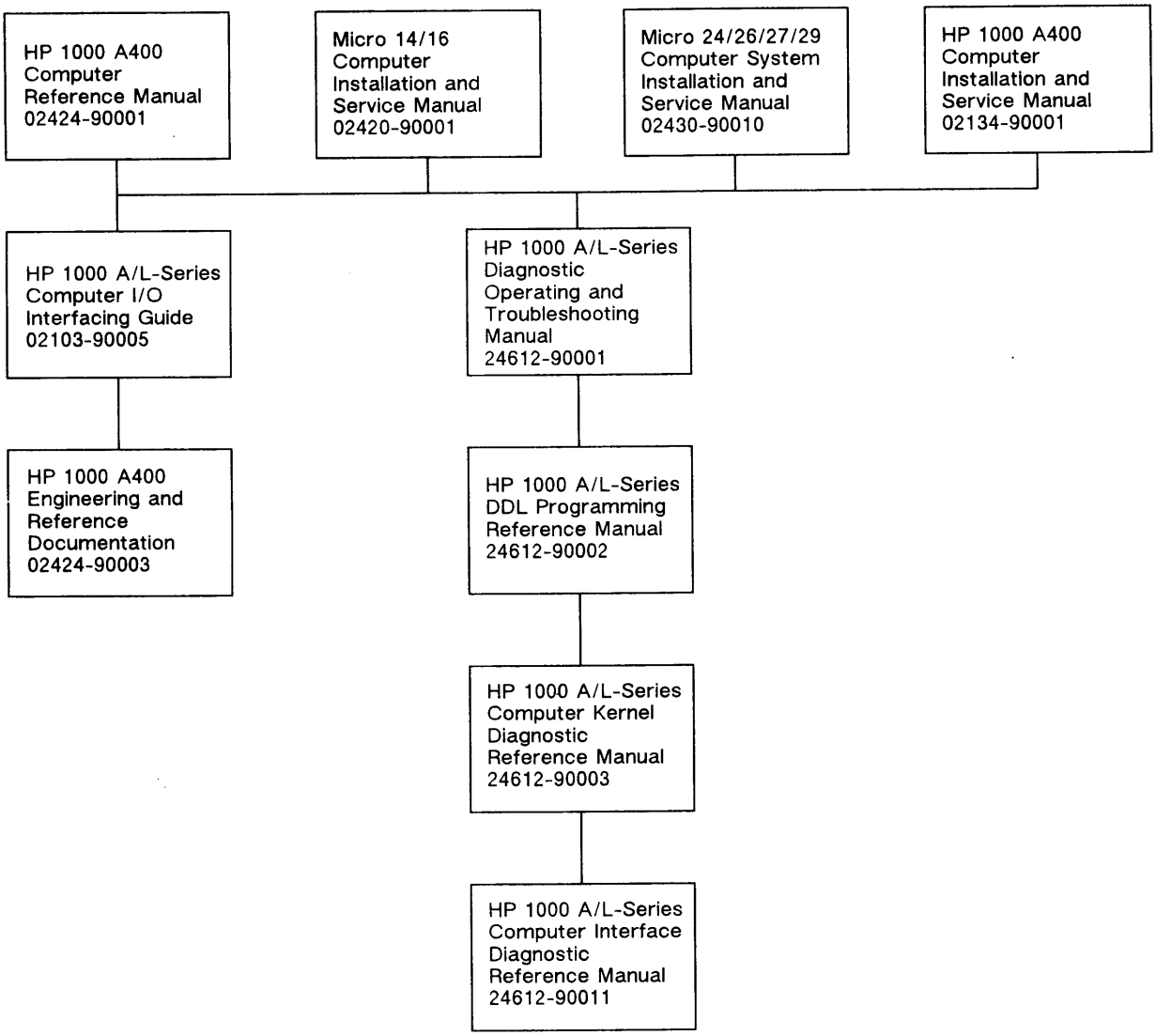


Table of Contents

Chapter 1
HP 1000 A400 Computer

Chapter 2
A400 Board Operation

Chapter 3
Processor Chip Theory of Operation

Chapter 4
A400 Memory Control

Chapter 5
On-Board I/O

Chapter 6
Memory Arrays

Chapter 7
Backplane

Chapter 8
Power Supply

Appendix A
Bus Control Timing Diagrams

Appendix B
Memory Control Timing Diagrams

Appendix C
Processor Memory Access Cases

List of Illustrations

Tables

1

HP 1000 A400 Computer

Introduction

The HP 1000 A400 Computer is a low-cost, single board computer that is fully compatible with the other A-Series Computers. Resident on the A400 board is 512k bytes of parity memory, the memory controller, and a four-port serial multiplexer.

The A400 Computer is a microprogrammed computer that offers exceptional operating flexibility. The microinstruction word is 32 bits wide which provides a larger instruction repertoire than available with lesser word widths. The microprogram memory control store of the A400 computer is 4k words. The A400 computer does not support the use of off-board control store.

Physical Description

The A400 single-board computer is built on a standard A-Series size PC board (approximately 6.75 x 11.75 inches). The board has two edge connectors for its backplane interface. There is one 50-pin edge connector on the front of the board for connection to memory arrays, with the existing memory expansion frontplane connectors, and one 36-pin edge connector for connection to the A400 on-board I/O cable with its 4-port breakout panel.

The A400 computer hardware is available as a single board, the 12100A Board Computer, which can be used as the foundation for building a customized computer system. A user-supplied computer cabinet provides the necessary backplane, power supply, and cooling fans.

The A400 computer is also available in the 20-slot box (HP 2134A), the Micro 24 16-slot box (HP 2434A or 2484A), or the Micro 14 6-slot box (HP 2424A). All A400 products are supplied with the On-Board I/O cable used specifically for the A400 on-board 4-port multiplexer. Figure 1-1 illustrates the HP 12100A, the HP 2134A, the HP 2424A, and the HP 2434A/2484A.

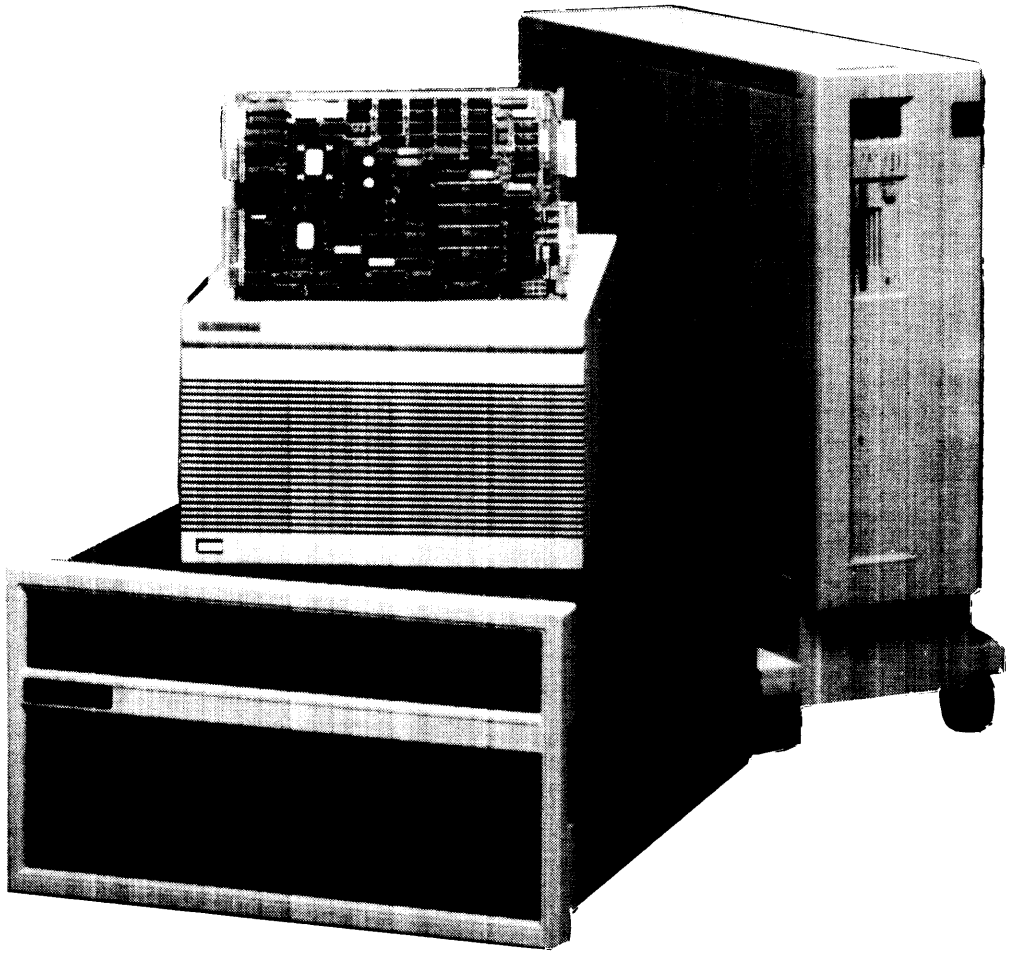


Figure 1-1. HP 1000 A400 Computers

System Environment

The A400 board plugs into a backplane which carries the logic signals, clock signals, and DC power. I/O cards and additional memory also plug into the backplane. The optional memory frontplane connector provides internal bus signal interconnections between the A400 board and the memory array cards. The 36-pin edge connector is for connection to the on-board I/O cable.

The memory array cards are located immediately above the A400 board and all I/O cards are placed below the A400 board in descending interrupt and DMA priority. The A400 on-board I/O is always the highest priority. Empty slots between cards are not permitted in order to guarantee interrupt and DMA priority chains. Refer to Chapter 7 for card slot priorities.

Description of Operation

The A400 computer is based on a micromachine architecture that is nearly identical to that of the A700 computer. The micromachine is based on a 32-bit microword with a 16k word address space. The base set is 4k words. The micromachine supports 6 microinstruction word formats and has 198 microorders. The microinstruction format is a 3 address format in that there are two ALU source addresses and a separate destination address in almost all instructions. The A400 base set microcode is identical to the A700 base set microcode except for the self-test section of the code and the addition of double precision floating point code.

The A400 processor is built around a single CMOS VLSI chip. The chip is housed in a 168-pin Pin Grid Array (PGA) package. The entire micromachine plus much of the macromachine support circuitry (for example, clock generation, memory control, interrupt control, and macro registers) is included in the VLSI processor chip.

In operation, the ALU and sequence logic of the processor carries out the commands of the microinstructions of microprograms stored in the control store. Most of the HP 1000 Computer Series instruction set are executed by microroutines of the base set.

The memory controller, other than containing external registers usable by the processor, provides memory mapping. Any main memory reference from the processor or I/O (except a boot memory access) selects one of 32 maps. Mapping expands the 32k words of logical address space to 16M words of physical memory. The microcode has access to the individual map registers on the board. The A400 supports up to the full 32M bytes of physical address space. The memory array cards configure themselves in ascending address order as they are installed in the backplane. Refer to the Memory Arrays chapter for information on available memory array cards.

An I/O read or write can occur in any cycle. When the backplane is free, an I/O handshake is performed upon a request for a handshake from the on-board I/O or an I/O card. The I/O instructions are executed by an I/O processor chip on each I/O interface; thus, each I/O interface is capable of operating independently of the A400 processor and provides efficient direct memory access (DMA) I/O transfers.

The VLSI Processor Chip

The VLSI chip is the heart of the A400 processor. It contains the intelligence and the control functions for the entire processor. The chip has approximately 19,000 gate equivalents. These consist of 14,000 standard cell gate equivalents (one gate equivalent equals one 2-input NAND gate) and three custom register files (sixteen 16-bit registers) containing 5,000 gate equivalents. The chip is packaged in a ceramic 168-pin PGA (with an extra pin for mechanical orientation). The major portions of the micromachine and macromachine of the processor reside on the chip. Chapter 3 contains a detailed description of the internals of the processor chip.

The On-Board I/O

The A400 on-board I/O consists of an I/O processor chip, the I/O master circuitry, and four serial port processors. The I/O master and the single DMA channel that it provides is shared by the four port processors. The I/O master performs all of the program functions described in the A/L-Series I/O Interfacing Guide (part no. 02103-90001).

The serial ports support RS-232 (standard), RS-422/423 (optionally), and V.24/28. Two of the four ports support modem control. Chapter 5 contains a detailed description of the on-board I/O.

System Support Features

Virtual Control Panel (VCP)

The Virtual Control Panel (VCP) is an interactive program located in a portion of the boot memory PROM. The VCP takes the place of a conventional control panel. Using the VCP, an operator can access internal and external registers, examine or change memory contents, and control execution of a program or load and initiate execution of the operating system or diagnostics.

Self-Test Capability

The A400 computer contains firmware microcode for self testing. The self-test is performed each time the power is turned on. Eight LEDs on the front edge of the A400 board are used to report operating or error status and the U1601 switches allow easy selection of boot loaders and auto-restart options.

User Microprogramming

Because the A400 computer is a microprogrammed machine, a user proficient in microprogramming techniques may add new macro instructions by adding to the A400 microcode. However, Hewlett-Packard does not support user-microprogramming of the A400 computer and therefore microprogramming tools in the form of A400 support products are not available.

Power and Cooling Requirements

For applications using the A400 circuit board, you will need to ensure that voltage, current, and ventilation provisions conform to the requirements specified in the following paragraphs.

DC Power

The DC power required for operation of the A400 board is as follows:

Voltage	Power
+5V	24 Watts
+12V	0.78 Watts
-12V	1.08 Watts

Power requirements for the memory array cards supported by the A400 are given in Table 1-1. Power requirements for I/O interface cards are provided in the individual manuals covering these cards.

Regulation Provided by the Power Supplies

DC voltages, tolerances, and periodic and random deviation (no load to full load) specifications for the power supplies used with the A400 computer are covered in Chapter 8.

Cooling Requirements

There are no external cooling requirements for the computer. Internal fans should be used to provide adequate ventilation to maintain operation within the environmental specifications given in Table 1-2.

Table 1-1. Power Specifications for Memory Array Cards

Card	Voltage	Current			Power		
		Battery Backup	Unaddressed	Addressed	Battery Backup	Unaddressed	Addressed
512k byte	+5V +5M	0.0 0.6A	1.1A 0.6A	1.1A 1.0A	0.0 3.0W 3.0W	5.5W 3.0W 8.5W	5.5W 5.0W 10.5W ← total
1M byte	+5V +5M	0.0 1.0A	1.3A 1.0A	1.3A 1.6A	0.0 5.0W 5.0W	6.5W 5.0W 11.5W	6.5W 8.0W 14.5W ← total
2M byte	+5V +5M	0.0 0.6A	0.9A 0.6A	0.9A 1.0A	0.0 3.0W 3.0W	4.5W 3.0W 7.5W	4.5W 5.0W 9.5W ← total
4M byte	+5V +5M	0.0 0.7A	0.9A 0.7A	0.9A 1.3A	0.0 3.5W 3.5W	4.5W 3.5W 8.0W	4.5W 6.5W 11.0W ← total
8M byte	+5V +5M	0.0 0.7A	0.9A 0.7A	0.9A 2.1A	0.0 3.5W 3.5W	4.5W 3.5W 8.0W	4.5W 10.5W 15.0W ← total

Note: The operating power specification is not cumulative when adding additional array cards since power consumption is proportional to access rate and only one card is accessed at any one time (only one card at a time operating). When a card is being accessed, all other cards dissipate unaddressed (standby) power.

Environmental Specifications

Environmental specifications are given in Table 1-2.

Card Cage and Backplane Assemblies

Backplane information covering items such as connector pinouts, the card cage layouts, and the card cage assembly drawings are included in Chapter 7.

Table 1-2. Electrical and Environmental Specifications

Electrical Specifications

Maximum Power Required:	32.0 Watts
Voltage:	+5Vdc +/-5% +12Vdc +/-10% -12Vdc +/-10%
Current:	5.7A at +5Vdc 0.065A at +12Vdc 0.090A at -12Vdc
DC Regulation	less than 2% periodic and random deviation

Environmental Specifications

MAXIMUM HEAT DISSIPATION	112 BTU
TEMPERATURE	
Operating in still air:	0° to 60°C (32° to 140 °F)
Operating air at 100 lineal ft/min:	0° to 65°C (32° to 145 °F)
Non-Operating:	-55 ° to 75°C (-55 ° to 167 °F)
RELATIVE HUMIDITY	5% to 95% non-condensing
ALTITUDE	
Operating:	To 4.6 km (15,000 ft.)
Non-Operating:	To 15.3 km (50,000 ft.)
SHOCK	
Operating:	3 g peak, 1/2 sine, 6 to 9 ms duration, 45 Hz crossover.
Non-Operating:	14 g peak, 1/2 sine, 6 to 9 ms duration, 45 Hz crossover.

VIBRATION

Operating Vibration:

Frequency (Hz)	Power Spectral Density (g^2/Hz)
5	0.004
5 - 15	-1.5 dB/octave
15	0.003
12 - 200	-6.0 dB/octave
200 - 350	0.00024
350 - 500	-6.0 dB/octave

g's rms = 0.86

Physical Characteristics

DIMENSIONS	
Height:	1.27 cm (0.5 in.)
Width:	17.15 cm (6.75 in.)
Depth:	29.85 cm (11.75 in.)
WEIGHT	0.682 kg (1.0 lb.)

Note: Watts = (VA) (Power Factor)
BTU/Hr = (Watts) (3.414)
KCal/Hr = (BTU/Hr) (0.252)

2

A400 Board Operation

Board Design Philosophy

One of the design goals of this computer was to minimize the cost. Since the incremental cost of adding gates to the custom VLSI chip is very small compared to adding gates to the printed circuit board (PCB), as much logic as possible was integrated into the custom chip. The PCB, therefore, contains the functions that could not be implemented on the chip, for example, buffering, large amounts of memory, speed critical circuitry, oscillators, and non-electrical interfaces (LEDs and switches).

The parts on the PCB and their organization were chosen to minimize parts count and increase manufacturability. One of the ways of decreasing the parts count was to design with the goal of 100 percent utilization, that is, use all eight bits in a latch instead of only five or six. Thus, to some extent, parts were chosen to fill the given functionality and then organized to maximize their use.

High-Level Organization

The A400 board contains an A-Series processor, memory controller, 512k bytes of memory, and four asynchronous serial channels with an associated standard A/L-Series I/O Master. This chapter gives general information on board control signals, and data and address paths. Refer to the appropriate chapter for a detailed description of the internals of the processor chip, the A400 memory control, and the I/O section of the A400 board.

The processor and memory control/array section of the board is organized around two major buses, the GIO-bus and the D-bus. These buses provide most address and data paths. Two minor buses, the PG-bus and the Map-bus, complete the address paths for the processor and memory controller. These buses, along with control signals, interact with off-board resources.

Two more buses are provided for on-board control of the micromachine, the CSA-bus (14 bits) and the CSD-bus (32 bits). They provide control store address and control store data, respectively. Figure 2-1 is a detailed block diagram of the buses on the A400 board. These buses will be described in the following sections and in the Memory Control Chapter.

Conventions

All signal names are capitalized. Bus names use brackets ([]) to identify bus bits and colons between bus bit numbers to identify a range of bus bits. For example, Address bus bits 0 through 9 would be written as AB[0:9].

References are made throughout the text to the schematics located at the end of this chapter. The integrated circuits (chips) are referenced by their U-numbers and schematic locations. For example, U405 (13C) means chip U405 on schematic sheet number 1 is located by coordinates 13 and C; where the horizontal grid on sheet number 1 is numbered 10, 11, etc. and on sheet number 2 it is numbered 20, 21, etc.

The D-Bus

The D-bus provides a data path for the backplane, the on-board user-memory, the processor chip, and the boot PROMs. It is controlled by the processor chip. Refer to the Processor Chip Chapter for a detailed description of D-bus control.

The processor chip outputs data onto the D-bus to be output onto the backplane or written to on-board memory (DRAM). Data output from the processor chip on the D-bus is driven onto the backplane even if it is to be read by the on-board DRAM.

When the processor chip reads data off of the D-bus, the buffers to the backplane drive data onto the D-bus unless the data is coming from the on-board DRAM. If the processor chip is reading the on-board DRAM or the boot PROM, the buffers between the D-bus and the backplane drive the data onto the backplane for visibility.

The DRAMs have their input and output pins tied together so that data is output onto the D-bus during a read and input off of the D-bus during a write. The write line is asserted early in a write cycle so that the DRAM outputs are not enabled during a write. Refer to the DRAM Control section in the Memory Control Chapter for a detailed description of DRAM operation.

Two 8-bit bi-directional latching buffers, U812 (44B) and U912 (45B), separate the D-bus from the backplane. D2DBE– under control of the processor chip, enables the D-bus onto the backplane when asserted. D2DBE– is asserted when the processor is handshaking with I/O, writing to memory, reading boot memory, or reading on-board DRAM. The D-bus to DB-bus latch in the buffers must be closed during the last short half-cycle (SHC) in the access when the on-board DRAM is being read to latch the data from the D-bus. The data must be latched off of the D-bus on this type of cycle because it disappears about two-thirds of the way through the last SHC as CAS deasserts and the DRAMs go tri-state. The controlling signal for the latch is RDLCH+ which is normally deasserted to pass all data through. RDLCH+ is the NOT-AND of CRD– and SECND–. SECND– is qualified against CRD– to make sure the latch is open in the long half-cycle (LHC) following the read. CRD+ is output from register U403 which is clocked on the rising edge of SC–. The D-input of the register is driven by the NAND of VALID+ and WEL– at U300. Thus CRD+ is set on the rising edge of SC– at the leading edge of the last SHC as indicated by the assertion of VALID+. CRD+ is only set during a read cycle by NANDing VALID+ and WEL–.

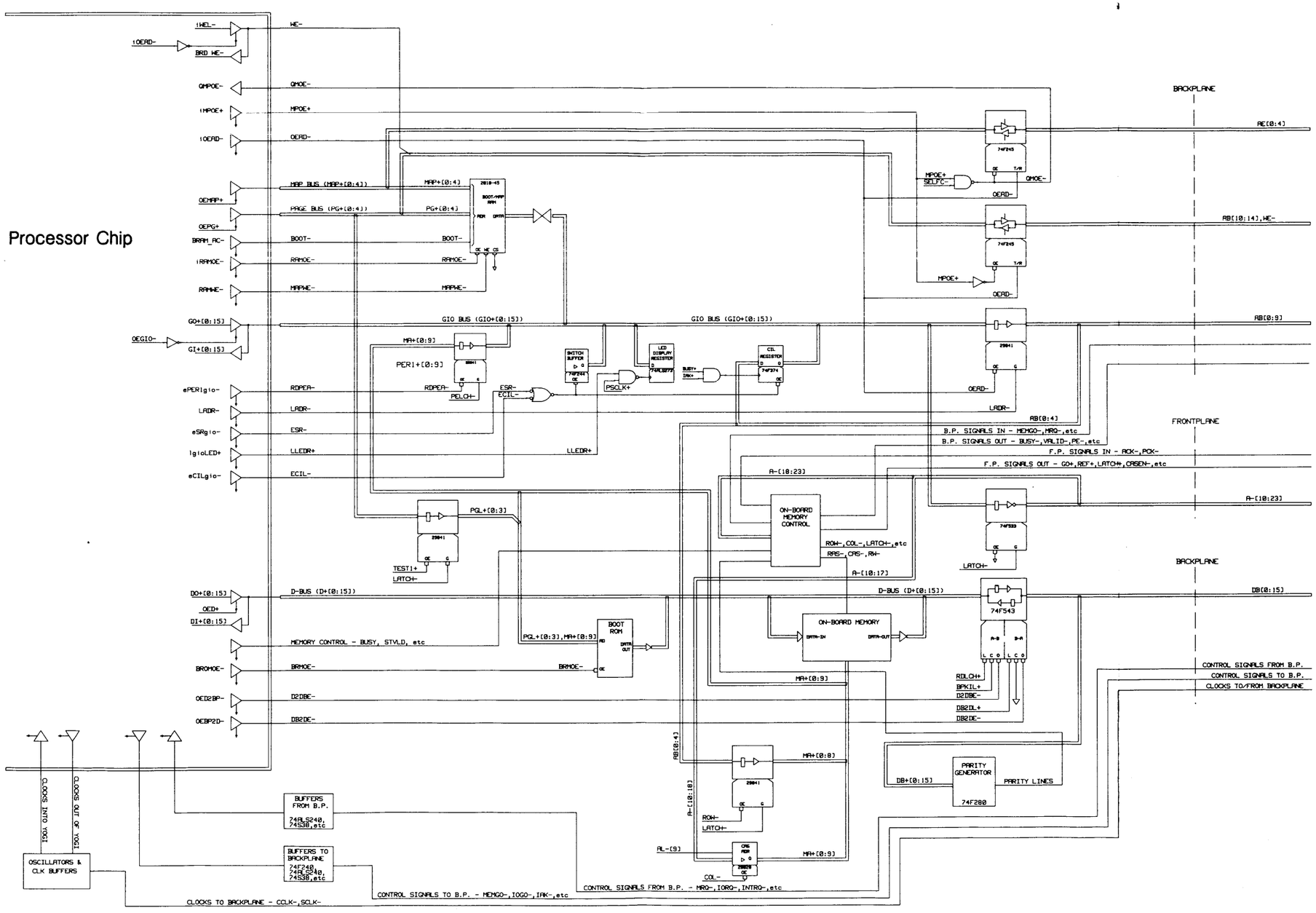


Figure 2-1. A400 Board Block Diagram

The path from the D-bus to the backplane must be turned off quickly after a read of the on-board DRAM if I/O will be requesting memory on the next SCLK cycle. I/O starts driving the backplane on the falling edge of SCLK– at the leading edge of the first LHC so the processor chip cannot be relied upon to disable U812 and U912 from driving the DB-bus. Therefore, a signal named BPKIL+ drives the chip enable pin for the D to DB direction on the buffers.

BPKIL+ is the NOT-AND of CRD–, SECND+, and MRQ– at U1104 (43B). CRD– is asserted as explained above on the last SHC of a memory read and lasts until the next SHC. CRD– thus sets up the "backplane kill". MRQ– indicates that I/O wants to do a DMA access and that the processor must get off of the bus. The deassertion of SECND+ off the trailing edge of the SHC is what starts the assertion of the BPKIL+ signal. The signal can last through the LHC because when MRQ– is asserted, I/O uses the backplane and neither the processor nor memory can use it.

Originally, SC– was used to latch the D to DB path instead of RDLCH, but BPKIL+ would always be asserted after SC– had opened the latch, thus starting to drive unknown data onto the backplane. This was changed so that the inherent backplane capacitance could hold the data valid slightly longer.

The path from the backplane DB-bus to the D-bus is enabled by the assertion of DB2DE– under control of the processor chip. The chip enable pin for this path is grounded so that DB2DE– has complete control. It is asserted when the processor is receiving control words or data from I/O, reading from off-board DRAM (disabled if reading on-board DRAM), or when I/O is accessing on-board DRAM.

DB2DL+ controls the latching function for the DB to D-bus path. DB2DL+ is normally deasserted. During the first SHC of a user memory access, the signal LATCH– is asserted to hold pertinent access information around for use throughout the cycle. LATCH– is NOT-ANDed with WEL– to produce DB2DL+. This allows the latch in the DB to D path to close only on a write cycle so that the "write" data can be captured. The deassertion of WEL– on a read access keeps the latch open so that the processor can read data from memory array cards when it was the one that requested the access. LATCH– is also not asserted when the processor handshakes with I/O for I/O instructions.

The GIO-Bus

The GIO-bus provides a data path for address and data. It connects the processor chip, the SRAM (used for the Map RAM and Boot RAM), the backplane register for the lower 14 bits of the physical address, the lower portion of the Parity Error Register (PER), the Central Interrupt Latch (CIL), the switch register, and the LED register. Logic in the processor chip controls the GIO-bus.

Map/Boot SRAM

Two 2k x 8 Static RAMs (SRAMs), U708 and U808 (34B), feed the GIO-bus. The SRAMs provide a 2k word data storage facility that is shared by Map RAM and boot RAM. The MAP+[0:4] and PG+[0:4] lines provide addressing while the BOOT- signal picks which data space (MAP or boot) the address points to. The processor controls the BOOT- signal.

Offset Address Latch and GIO-Bus Usage During a Memory Access

For a processor memory access, the GIO-bus provides a data path for the lower ten bits of data (or address bits) to their latch for the backplane. The latch at U709 (37B) drives AB+[0:9]. U709 is loaded under control of the LADR- signal from the processor chip. The OEAD- signal, from the processor chip, enables the output of the latch onto the backplane. The GIO-bus is then free for use by the SRAMs so that they can output the extended physical address and the read/write protect bits at the end of the LHC and the beginning of the SHC. The SRAMs are output enabled by RAMOE-. If the cycle is a boot RAM access, then the data from the SRAMs is boot RAM data instead of MAP information and is wrapped around to the D-bus by the processor chip. The processor chip also latches the data on a boot RAM access so that it can free the GIO-bus for use once BUSY asserts.

LATCH- is used by U906 (52A) and U601 (52B), to latch the extended physical address and the read/write protect bits from the GIO-bus during a normal DRAM access. This occurs about midway through the SHC during the assertion of MEMGO. (During a boot access the read/write protect bits are ignored). The extended physical address is driven on the A-[10:23] lines on the frontplane for use by the memory arrays. The read/write protect bits are also latched by U906 and U601 for use by the memory controller. (The output of U906 and U601 can be tri-stated for test by asserting TEST1+). The GIO-bus is then free at the end of the SHC so it can be used for micromachine off-chip register accesses. For an I/O memory access, the GIO-bus usage is the same except for the loading of the lower ten bits of address into their latch.

Parity Error Register (PER)

The Parity Error Register (PER), U806 (55D), contains the ten least significant bits of the last parity error physical address. PELCH- latches the parity error address into the PER. PELCH- is normally low. It goes high to input the parity error address during the last half of the last SHC in a user memory (DRAM) read cycle with a parity error. At the beginning of the last SHC of any access, the ROW address for the DRAMs is reasserted on the MA+[0:9] bus which is the input to the PER. PELCH- goes low at the trailing edge of the SHC to latch the parity error address.

The PER is output onto the GIO-bus by the assertion of RDPEA- under control of the processor chip.

Central Interrupt Latch (CIL)

The GIO-bus also provides a data path to read the Central Interrupt Latch (CIL). The CIL, U512 (33D), is output enabled onto the GIO-bus under control of the processor chip by asserting ECILSR-. ECILSR- is the NOT-NOR of ECIL- and ESR-. The processor chip asserts ECIL- to read the CIL and ESR- to read the switch register. These were kept as separate lines to allow for a wider switch register on future products. The enable lines are ORed together because the CIL and the switch register are each one byte wide and it is undesirable to float the inputs to the processor chip on the byte not being read.

The select code of the interrupting I/O interface is latched into the CIL by GATCI-. GATCI- is generated by NOT-NANDing IAK+ and BUSY- at U201 (32C). Thus the CIL is latched shortly after the rising edge of SCLK- when IAK+ and BUSY- are asserted during the interrupt fetch from memory of an interrupt acknowledge cycle.

Switch Register

The switch register, U1601 (41A), contains set-up information for the processor. It is implemented with a switch with internal pull-ups which is connected to a buffer, U701 (42A). The buffer is output enabled by the assertion of either ESR- or ECIL- under control of the processor chip. This allows all 16 bits of the GIO-bus to be driven so that the bus does not float when either the 8-bit switch register or the 8-bit CIL is being read by the processor chip. The switch register buffer is a fast part because this decreases the propagation delay of its data into the processor chip. Note that the switch package has pull-ups built into it. These pull-ups run off +5M.

LED Register

Eight LEDs are provided on the A400 board to indicate processor status. These LEDs are driven by U801 (44A). It is a byte wide register that can be reset. The reset line is connected to SPON+, the synchronized reset signal on the board. This makes the part turn on all the LEDs at power-up.

The data is clocked into U801 by CLEDR+ which is the AND of LLEDR+ and PSCLK+ at U1508 (43A). The processor chip controls LLEDR+. CLEDR+ clocks the LED register at the end of the LHC. PSCLK+ is an early version of SC- to give U801 more hold time before the processor chip stops driving the GIO-bus.

The Map-Bus

The Map-bus, which consists of MAP+[0:4], provides the board path for the backplane bits AE+[0:4]. AE+[0:4] are the logical address extension bits which point to the map set that the memory access will go through. MAP+[0:4] connect a bus transceiver, U412 (32B), to the processor chip and the Map RAMs. When the processor accesses memory, the extended logical address is driven onto the Map-bus by the processor chip to provide half of the address for the Map RAMs. U412, which receives the Map-bus, is turned toward the backplane and drives the backplane for visibility. This is done under control of the processor chip by asserting OEAD–. MPOE+, which is inverted at U212 (31A) to become QMOE–, turns on the transceiver. Note that U212 acts as an inverter because SELFC– is not asserted in this case.

When MRQ– is asserted to indicate that I/O wants to access memory, the processor chip gets off of the Map-bus and points the transceiver toward the board by deasserting OEAD–. The processor chip enables the transceiver by asserting MPOE+. This allows I/O to drive its AE address onto the Map-bus.

The transceiver on the Map-bus has different drive capability depending on which way it is pointing. The higher drive capability side drives the Map-bus to keep the delay to a minimum when getting an address off of the backplane.

When I/O does a DMA self-configure or acknowledges an interrupt cycle, it asserts SELFC– to indicate that the current access must go through Map 0. The board forces this by ANDing SELFC– with MPOE+ to produce the actual enable signal, QMOE–, for U412. When SELFC– is asserted, U412 is disabled, regardless of the state of MPOE+. QMOE– is also sent to the processor chip to indicate that zeroes should be driven onto the Map-bus. Thus the transceiver goes tri-state and the processor chip drives zeroes onto MAP+[0:4] to force the access to go through Map 0.

Not all of the lines are used in U412. To keep the part from oscillating, all the unused channels on side A are tied to one pull-up and all the unused channels on side B are tied to another pull-up. It is assumed that when the part turns around to drive the pull-up, there will not be contention because all the outputs will be trying to drive in the same direction.

The PG-Bus

PG+[0:4] provides the board path for backplane bits AB+[10:14]. AB+[10:14] are the upper five bits of the logical address. They point to the page register in the map set to generate the extended physical address. PG+[0:4] connect a bus transceiver, U312 (32B), to the processor chip and the Map RAMs as well as providing part of the address for the boot PROMs. When the processor accesses user memory, AB+[10:14] are driven onto the PG-bus by the processor chip to provide the second half of the address for the Map RAMs. U312, which receives the PG-bus is turned toward the backplane and drives the backplane for visibility. This is done under control of the processor chip by asserting OEAD– to point the transceiver toward the backplane and MPOE+ which is inverted to MPOE– to turn on the transceiver. (MPOE+ is inverted at U212 (31B). GPU+ which also goes into U212 is a general pull-up.)

When MRQ– is asserted to indicate that I/O wants to do a memory access, the processor chip gets off of the PG-bus and points the transceiver toward the board by deasserting OEAD–. The processor chip enables the transceiver with the assertion of MPOE+. This allows I/O to drive its upper five bits of the logical address, AB+[10:14], onto the PG-bus. The higher drive side of the transceiver is on the PG-bus to make the Map access as fast as possible.

The upper four bits of the PROM address are presented on the PG-bus for a boot access. These bits are latched through a U106 (42D) by the assertion of LATCH– so that they remain stable through the access and the processor can access the MAPs if desired.

Not all of the lines are used in U312. To keep the part from oscillating, all the unused channels on side A are tied to one pull-up and all the unused channels on side B are tied to another pull-up. It is assumed that when the part turns around to drive the pull-up, there will not be contention because all the outputs will be trying to drive in the same direction.

Clock Generation

Two oscillators on the board provide the basis for all the system clocks. The CCLK oscillator at U1509 (10A) runs at 14.7456 MHz. It is buffered by U1410 (12A) before it goes into the processor chip so that it can be disabled for testing. The disable signal is TEST2+. CCLK is used by the processor chip for the TBG interrupt and by the I/O section of the board as the basis for PPCLOCK+ which drives the four on-board serial ports. CCLK is called YCCLK- at the output of the buffer before it goes into the processor chip. The CCLK oscillator also drives another buffer in the U1410 to provide CCLK- on the backplane. TEST1+ disables this clock for testing.

The second oscillator at U1510 (11A) provides the FCLK frequency of 22 MHz. It is also buffered by U1410 before it goes into the processor chip so it can be disabled by TEST2+ for testing. To minimize skew, the processor chip receives CLOCK-, the buffered version of the oscillator output and outputs its own version of CLOCK-, it is called PFCLK+. CLOCK- is also used by the processor chip to generate PSCLK+ which runs at 4 MHz. PSCLK+ is buffered by U1410 to become SCLK- on the backplane. SCLK- goes from the output of one of the buffers in U1410 to the input of the other buffer in the U1410 as SCLKIN-. It is then output as SC+ and IOSC+. These are the clocks that the processor chip receives and uses to run its internal state machines. SC+ is inverted by U1410 to generate SC- for the board. SC+ also drives a delay line, U1408 (23B), to generate SHFTSC+ for the memory controller and the board control section of the processor chip. SHFTSC+ is skewed a nominal 42 ns from SC+. See Figure 3.1 in Chapter 3 for a block diagram of the clock generation.

U1410, which drives all these clocks, is powered off of +5M. It receives two disable signals, TEST1+ and TEST2+. TEST1+ disables SCLK-, CCLK-, FCLK-, and SC- when asserted. TEST2+ disables CLOCK-, YCCLK-, IOSC+, and SC+ when asserted.

Control Store

The control store consists of four PROMs located at U1212 (85D), U1312 (85C), U1412 (85B), and U1512 (85A). It is 4k words deep by 32 bits wide. They have a 40 ns access time but access times up to 55 ns are acceptable.

OFFBDCSA- disables the on-board control store when another card recognizes the control store address as its own. OFFBDCSA- is pulled up on the A400 board and received by a schmitt trigger NAND gate to isolate the off-board environment from the on-board control store PROMs.

Backplane Buffers

MEMGO- is driven by an open collector NAND gate, U401B (13B). Its inputs are MGO+ and MRQ-. MGO+ is asserted by the processor chip to produce MEMGO- on the backplane. MRQ- qualifies MGO+ so that when MRQ- is asserted, the board deasserts MEMGO- on the backplane as quickly as possible so it will not start a memory cycle. This always gives I/O the highest priority for the backplane.

U1112 (17C) and U306 (12B) are buffers that drive and receive miscellaneous signals to and from the backplane. These buffers were chosen for their relative high speed and low power dissipation. U1112 drives RNI-, FETCH-, CPUTURN-, CRS-, IOGO-, and IAK-. U306 receives MEMGO-, MRQ-, IORQ-, INTRQ-, SLAVE-, PFW-, and MLOST-.

Virtual Control Panel (Slave Mode) Processing

An interface card may force the processor to enter an I/O handshake by pulling down the open-collector line SLAVE-. Once the processor is in slave mode, its internal registers are accessible to external devices through certain I/O interface cards. The Asynchronous Interface card, the HDLC (DS network) Interface card, and the Parallel Interface card (PIC) are the interface cards which may request slave mode processing. In order to use the PIC as VCP, you must supply code since HP VCP code does not support the PIC interface.

Because slave mode processing involves direct interaction between the requesting device and the processor, the processor merely provides buffering, signal timing, and bus arbitration for the handshake signals and data transfers.

Slave mode processing abides by the same protocols used for the execution of I/O instructions that require interaction between the I/O processors and the central processor. Whereas an instruction causes an I/O processor to initiate an I/O handshake, slave mode processing is performed in response to some external event not related to the program flow. The I/O handshake of an I/O instruction occurs during the execution of that instruction but the I/O handshake of slave mode processing occurs between instructions. Thus, slave mode uses IORQ- and IOGO-, but operates independently of the program.

A slave mode request, BP_SLAVE-, is made over the backplane by the interface card configured for slave mode processing. Only one I/O interface card can be selected as the slave mode interface at any given time. As soon as the current instruction has been completed, the processor acknowledges the slave request and SCHOD- (slave chain output disable) is deasserted to inform the slave requesting interface card to start the I/O handshake.

Any device with input/output capabilities and connected to an interface card configured to allow slave mode processing becomes the virtual control panel (VCP). This device provides the means to access the processor registers and memory locations in a manner similar to a hardware front panel. If a terminal is the VCP device, the keyboard replaces the front panel switches for register selection and data entry, while the display replaces the hardware status and data output indicators. Unlike a hardware front panel, the VCP may be located away from the computer at a remote location. Operator interaction using a terminal is accomplished by a program located in the VCP PROMs.

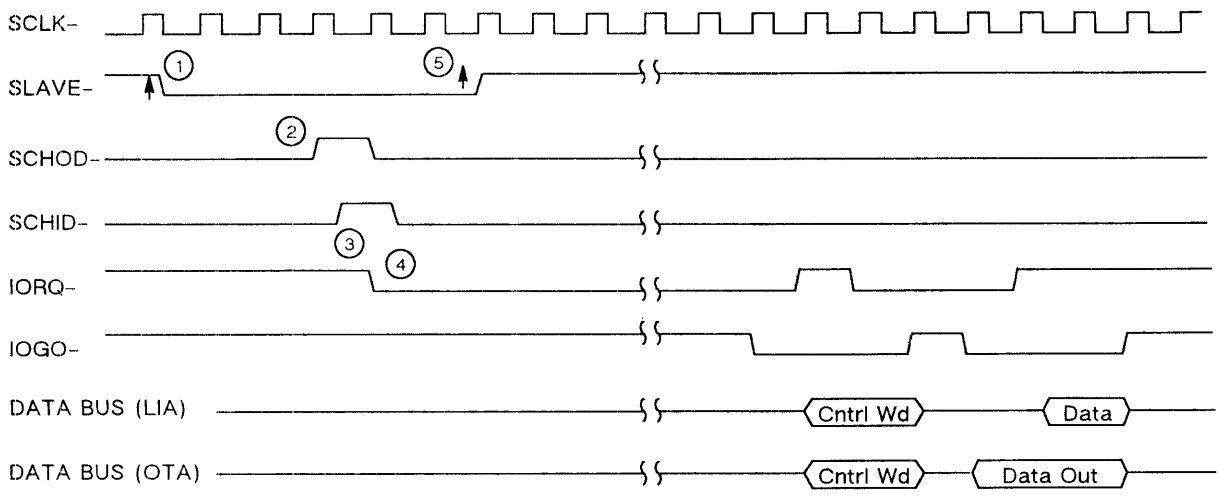
Figure 2-2 is a timing diagram of the backplane protocol for slave mode processing.

Battery Back-Up

Battery back-up is supported on the A400 board. To allow it to work, +5M must be valid. The +5M line supplies the following:

- the clock circuitry
- the processor chip (which controls refresh operations)
- the GO flip-flop
- the memory PAL (MPAL)
- the RAS and CAS drivers
- the frontplane drivers for REF+ and GO+
- the BPON synchronizing flip-flop

MLOST- is under control of the power supply. It is buffered by U306 (12B) and then received by the processor chip to determine if +5M went down when power was down (determines if user memory is valid or not). MLOST- is valid and read in a 10 ms window after BPON+ is asserted. The board provides a pull-up at U1206 (46A) on the MLOST- line.



NOTE: Same handshake protocols as an I/O Handshake. Some slave mode transfers require only one set of IORQ-/IOGO- handshakes.

① An interface card asserts SLAVE- to request the processor to enter slave mode.

② When the processor has completed executing the current instruction, it acknowledges the assertion of SLAVE- by deasserting SCHOD- for one cycle.

③ Worst case, the SCHID/SCHOD priority chain has propogated down to the lowest-priority interface card by the end of that cycle, so that the last SCHID- will go high for one cycle.

④ The interface card received the enabling signal when its SCHID- signal went high, and can now pull on IORQ- in order to initiate the I/O handshake. The rest of the I/O handshake can then proceed exactly as shown in Figure 7-8 in Chapter 7.

⑤ The interface card deasserts SLAVE- once it has asserted IORQ-.

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Figure 2-2. Slave Transfer Protocol

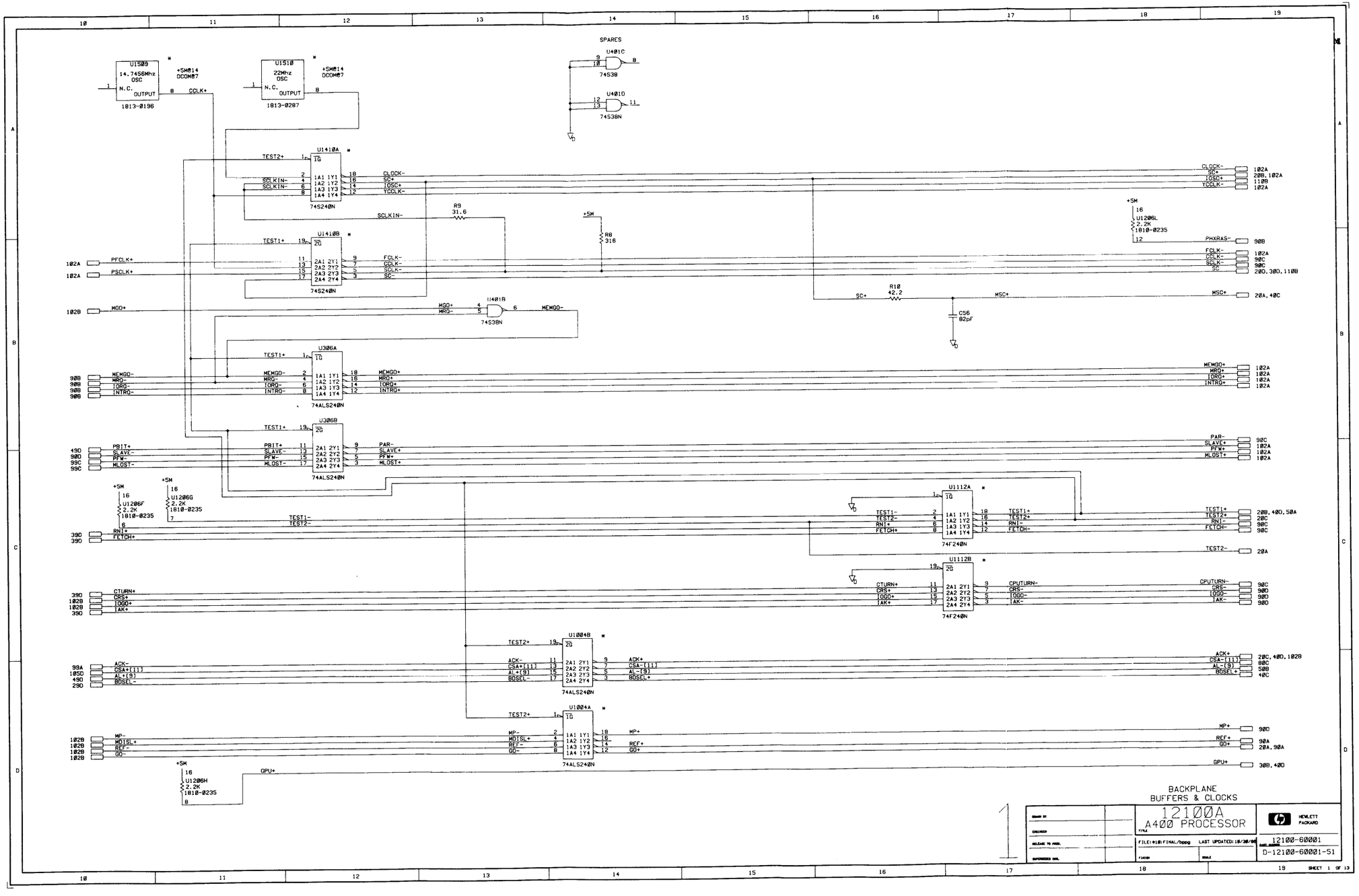


Figure 2-3. Backplane Buffers and Clocks Schematic Diagram

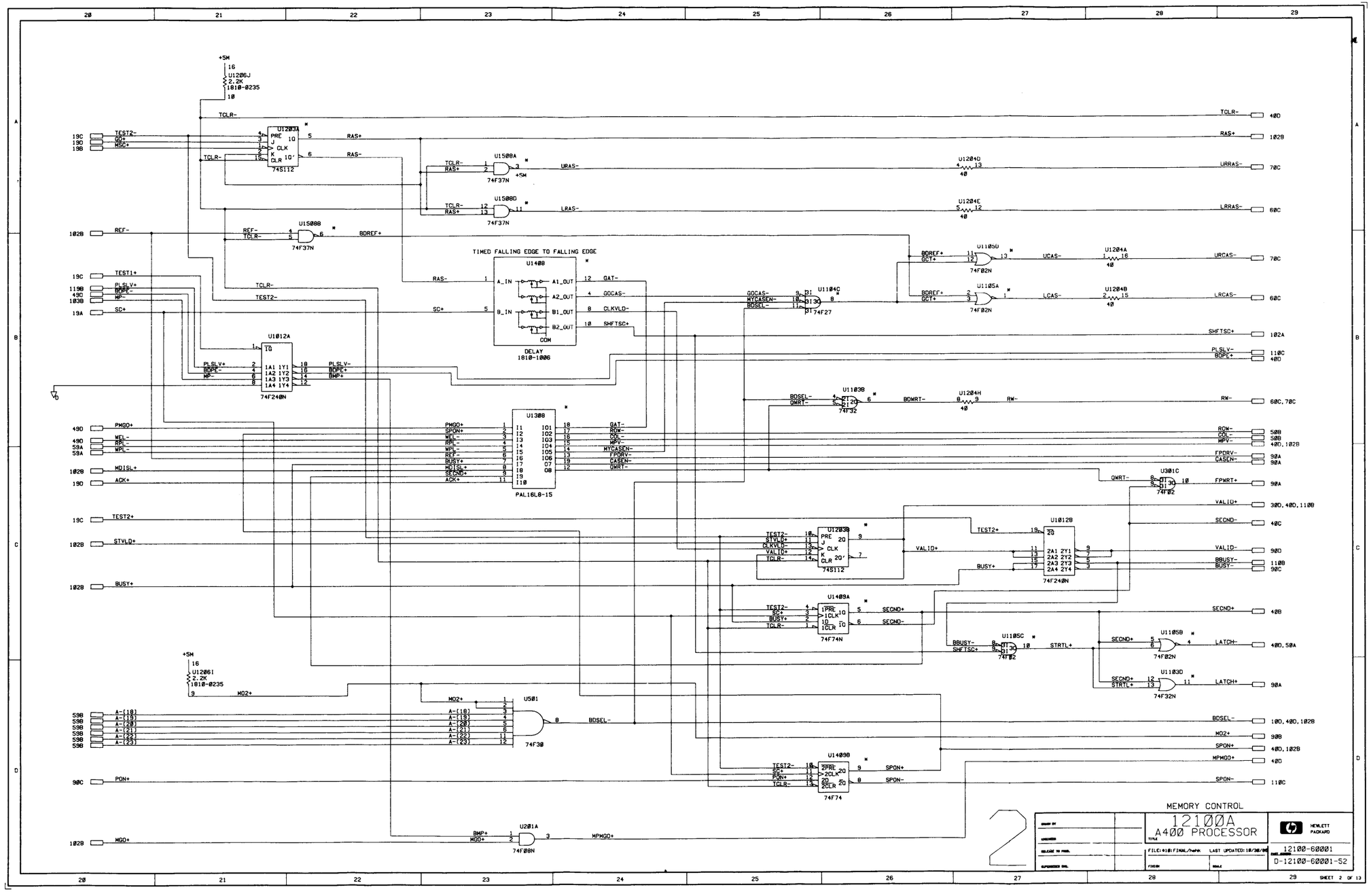


Figure 2-4. Memory Control Schematic Diagram

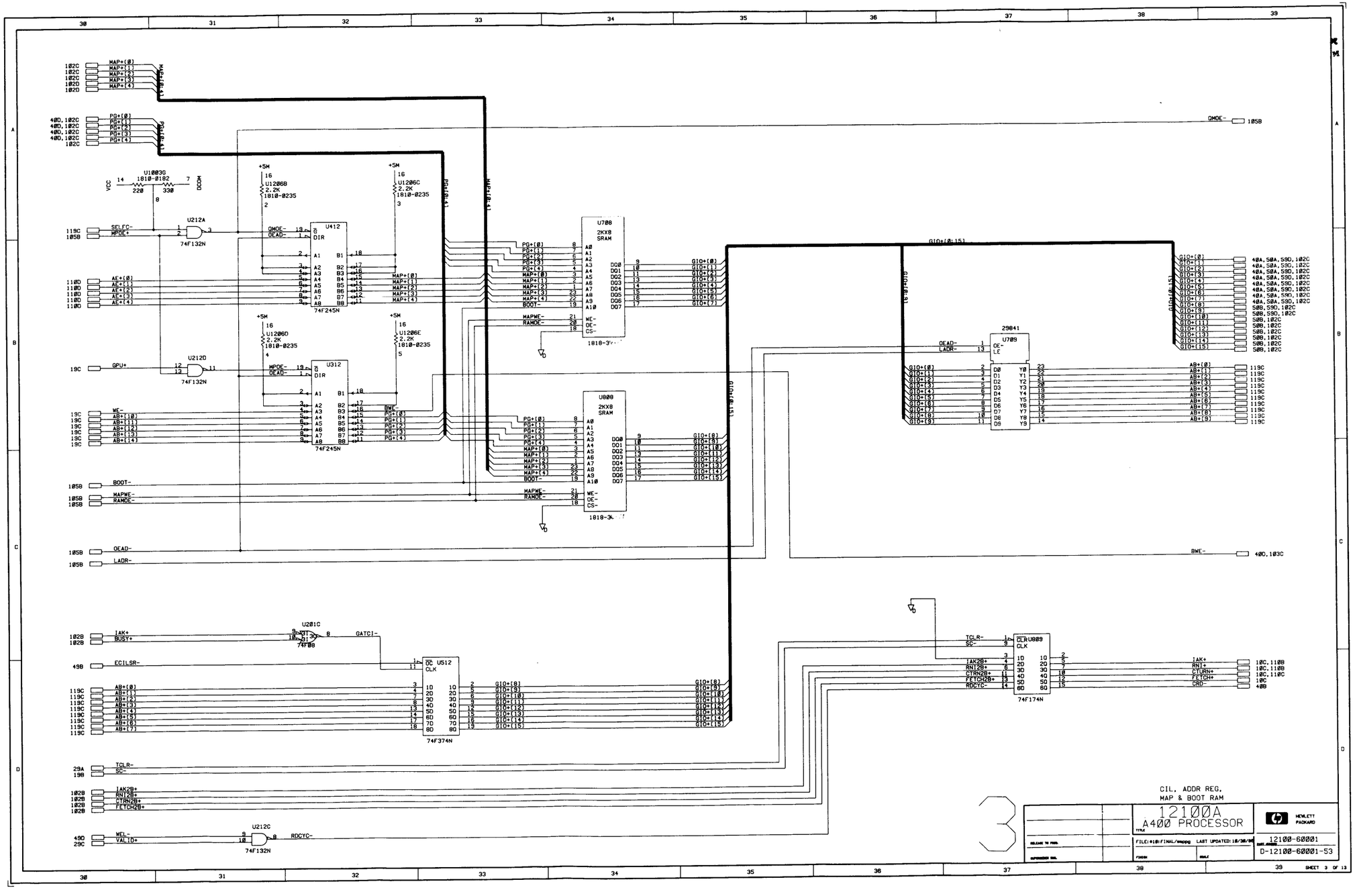


Figure 2-5. CIL, Addr Reg, Map & Boot RAM Schematic Diagram

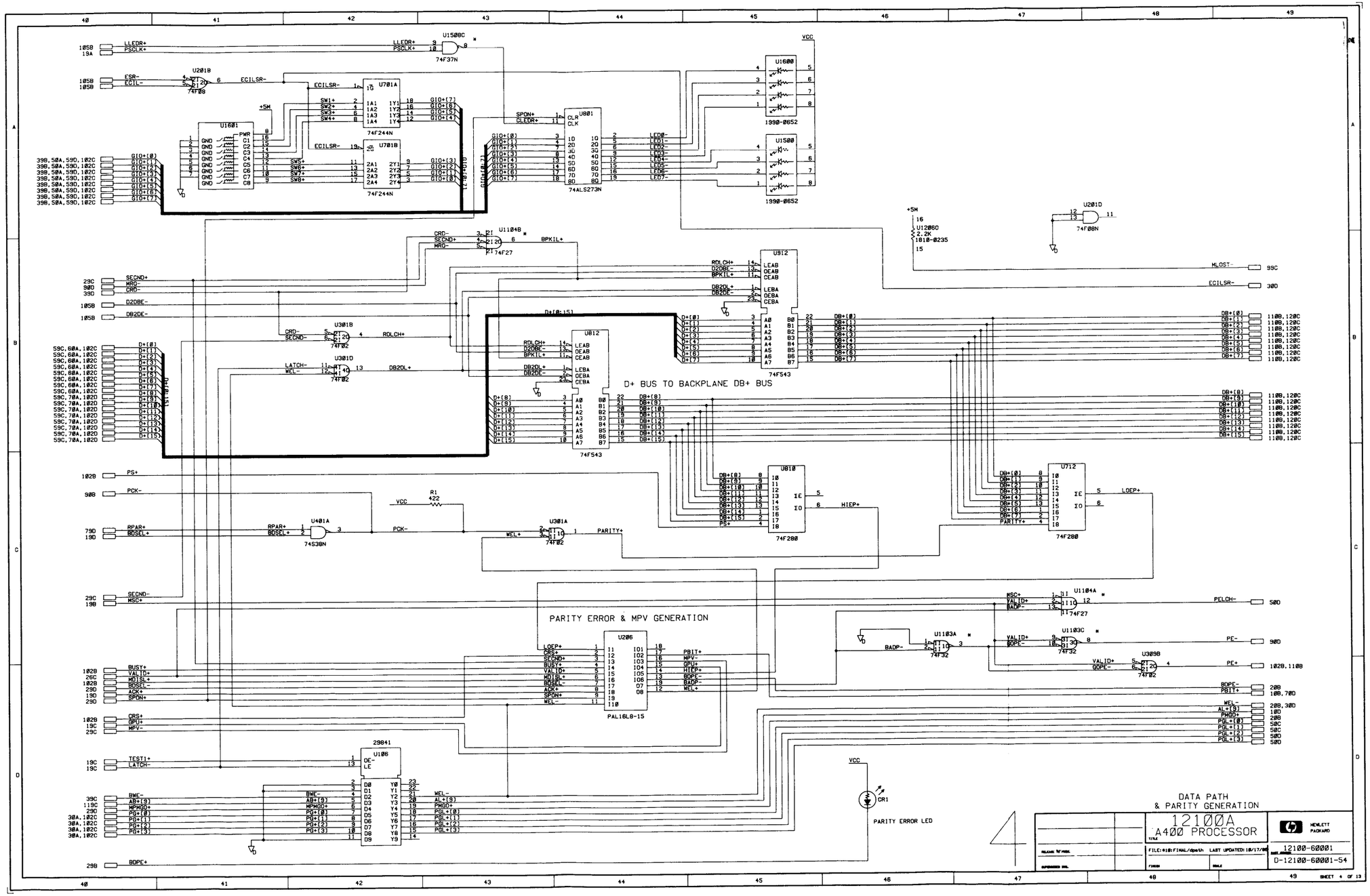


Figure 2-6. Data Path & Parity Generation Schematic Diagram

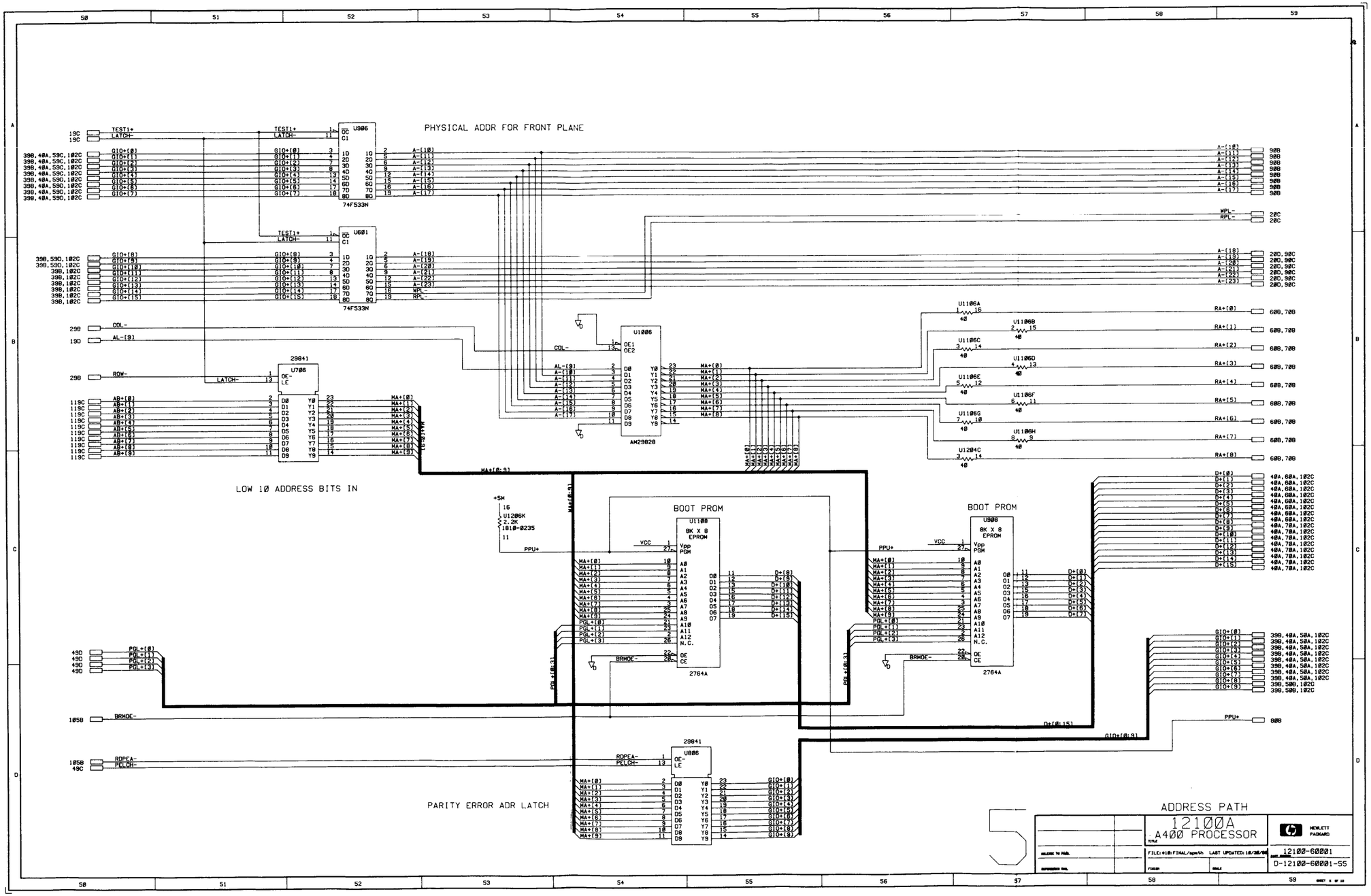


Figure 2-7. Address Path Schematic Diagram

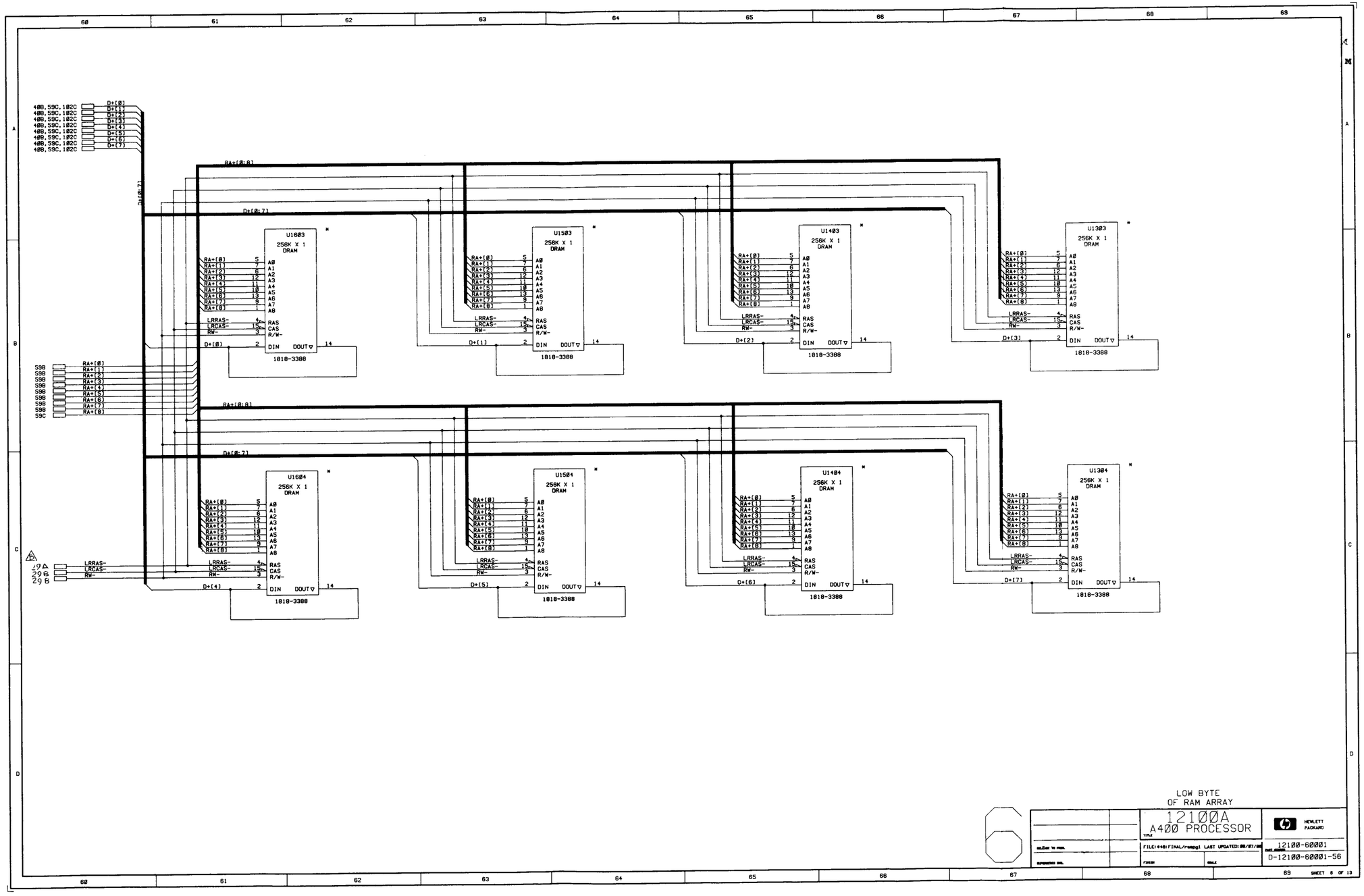


Figure 2-8. Low Byte of RAM Array Schematic Diagram

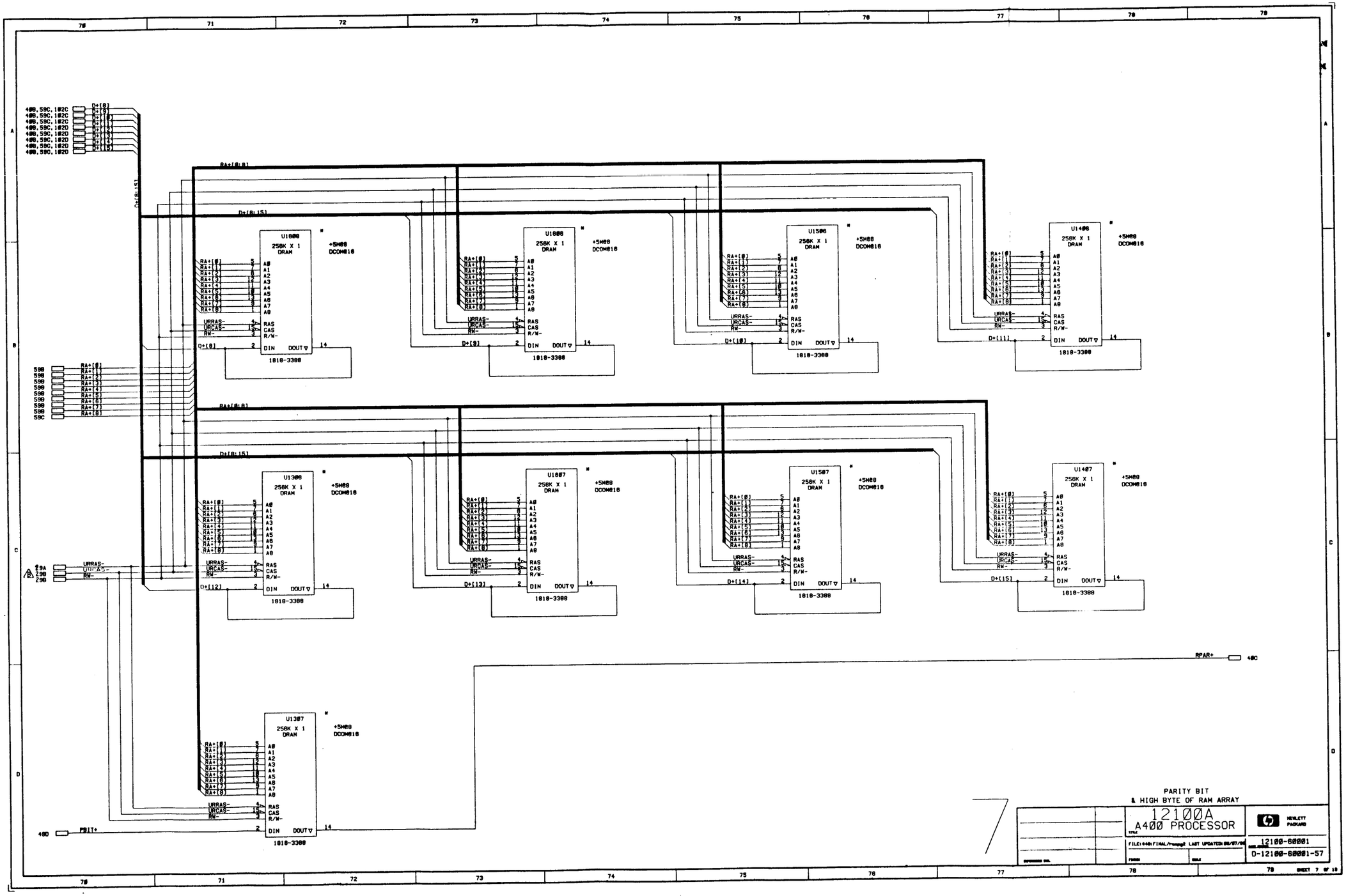


Figure 2-9. Parity Bit & High Byte of RAM Array Schematic Diagram

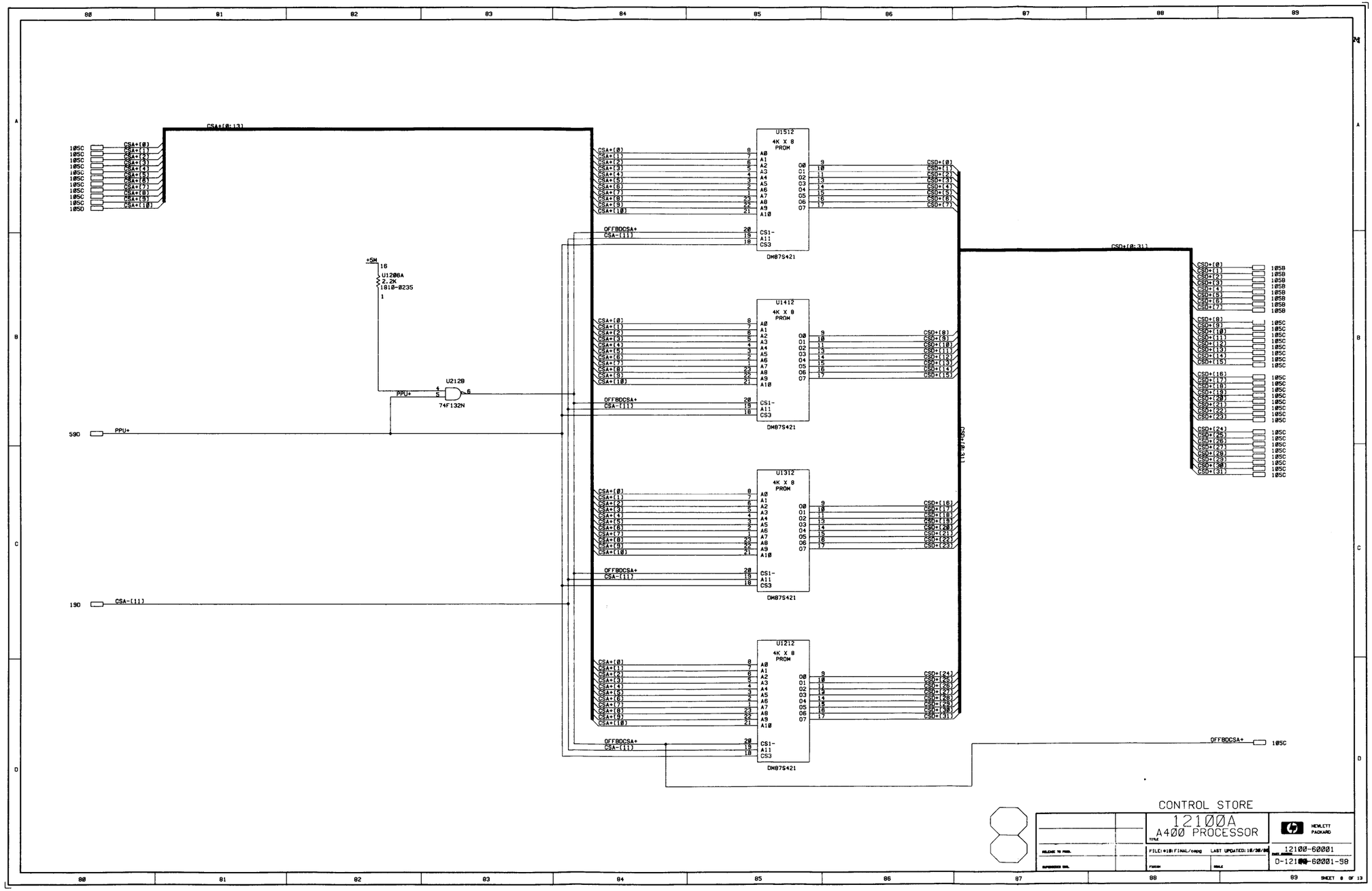


Figure 2-10. Control Store Schematic Diagram

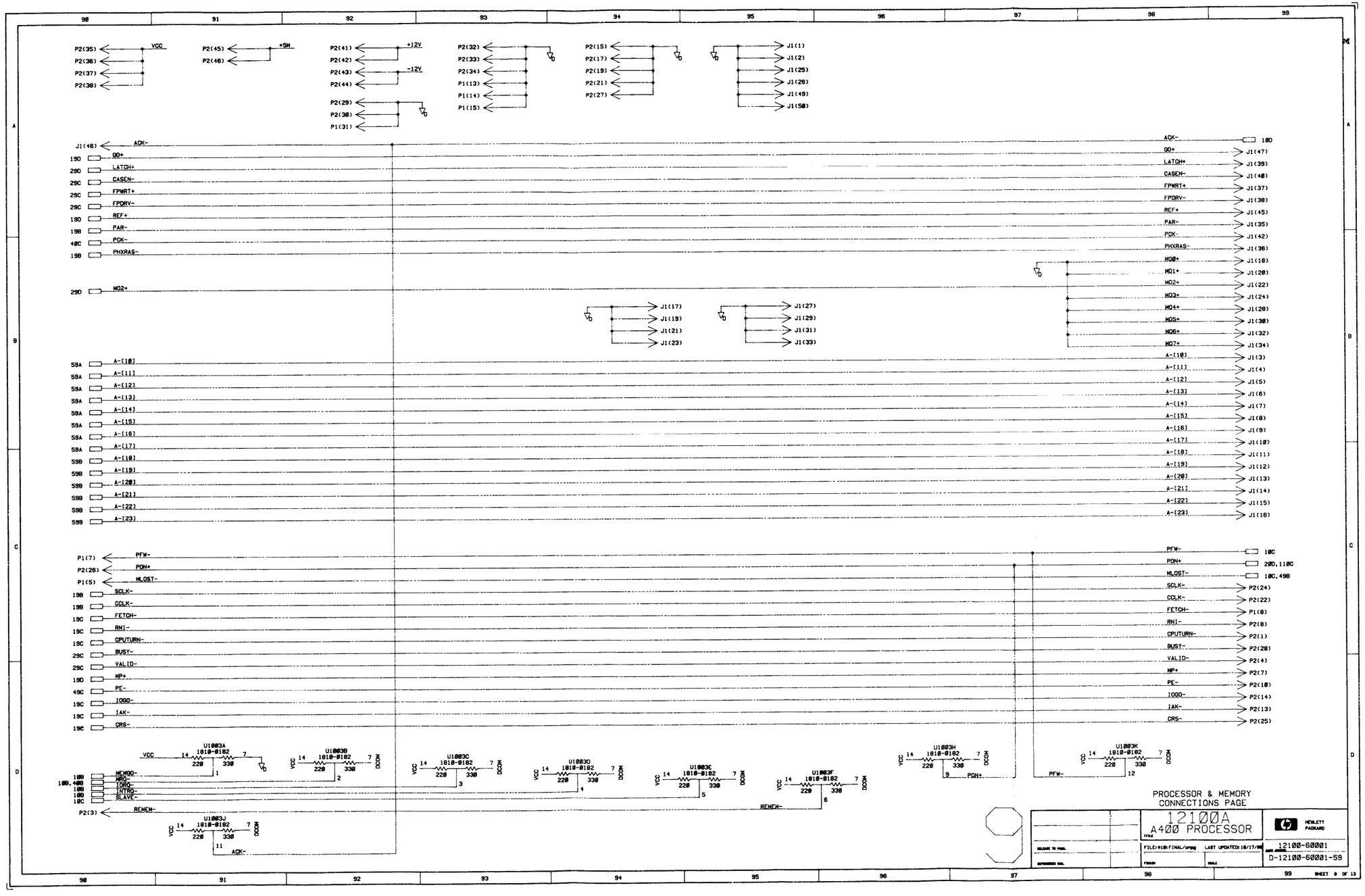


Figure 2-11. Processor & Memory Connections Page Schematic Diagram

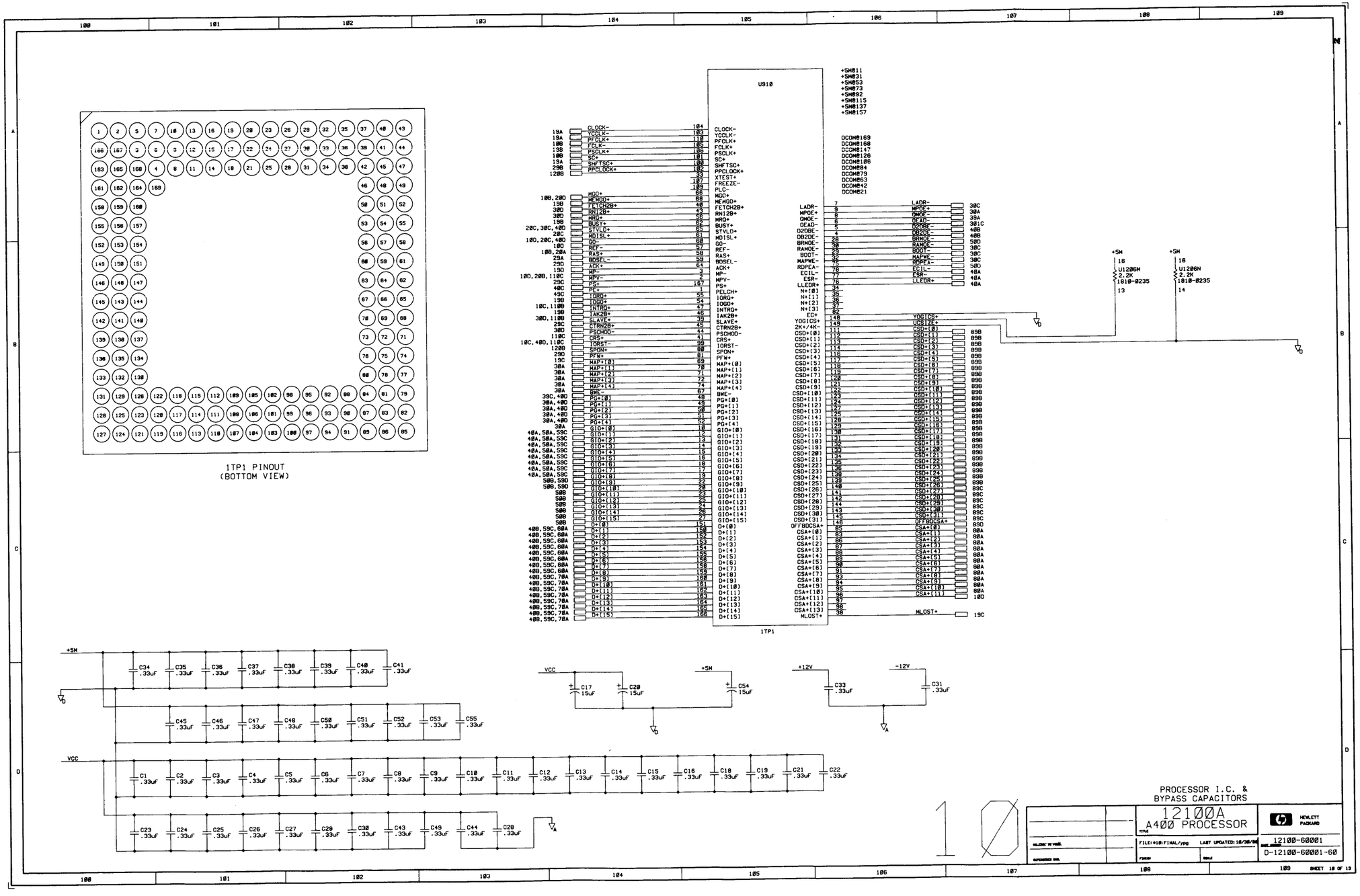


Figure 2-12. Processor I.C. & Bypass Capacitors Schematic Diagram

3

Processor Chip Theory of Operation

The VLSI chip contains the intelligence and the control functions for the entire processor. The major portions of the micromachine and macromachine of the processor reside on the chip as well as portions of the memory control logic. Figure 3-1 is a detailed block diagram of the A400 Processor Chip. It contains the following functional blocks and registers:

- Clock Generation Logic
- 32-Bit Microinstruction Register (MIR)
- Microsequencer and Look-Up Table
- Unimplemented Microcode Instruction multiplexer
- Primary ALU and Shifter
- Secondary Logical Unit (secondary LU)
- Dual-Port General Purpose Register File (GPRF)
- Address Generation Logic
- Memory and I/O State Machine Logic
- Memory Array Control Logic
- Condition Register and Selection Logic
- General and Privileged Register Files (GRIN, PRIN)
- Macro Program Counter (P)
- Memory Data In Register (T)
- Macro Instruction Register and General Purpose 16-Bit Counter (CT)
- Fetch Address Register (FA)
- Memory Address Register (MA)
- Base Register (BA)
- Interrupt Mask and Prioritizer (IMP)
- Interrupt Status Register (IST)
- Map Address Register (MPAR)
- Memory Control Register (MEMR)
- Data Out Latch (DOUT)
- Address Out Latch (AOUT)
- Extended Address Out Latch (AEOUT)
- Upper 14 Bits of the Parity Error Address Register
- Bus Control Logic
- On-Board Memory Data Latch (DO Latch)

The internal design of the A400 processor chip is based on the architecture of the A700. As an additional reference, you can read the A700 Engineering and Reference Document (part no. 02137-90005).

Conventions

This chapter makes use of some conventions for indicating logic functions and clock edges. The following symbols with their definitions are used:

SC-↑	the rising edge of the signal SC-
SC-↓	the falling edge of the signal SC-
NOT-AND	the AND-gate style DeMorgan equivalent of a NOR gate
NOT-NAND	the AND-gate style DeMorgan equivalent of an OR gate
NOT-OR	the AND-gate style DeMorgan equivalent of a NAND gate
NOT-NOR	the AND-gate style DeMorgan equivalent of an AND gate
-	can be either the NOT function or a negative true signal
+	can be either the OR function or a positive true signal
*	the AND function

All signal names are capitalized. Bus names use brackets ([]) to identify bus bits and colons between bus bit numbers to identify a range of bus bits. For example, Address bus bits 0 through 9 would be written as AB[0:9].

Error Correction Support

The A400 board does not support error-correcting memory arrays. The processor chip, however, has the necessary circuitry to support error-correction memory cycles. For example, the processor chip contains freeze logic to freeze the processor in the case of an error-correction cycle, but this type of cycle would never happen on the A400 board because the board itself does not have the circuitry necessary to support error correction.

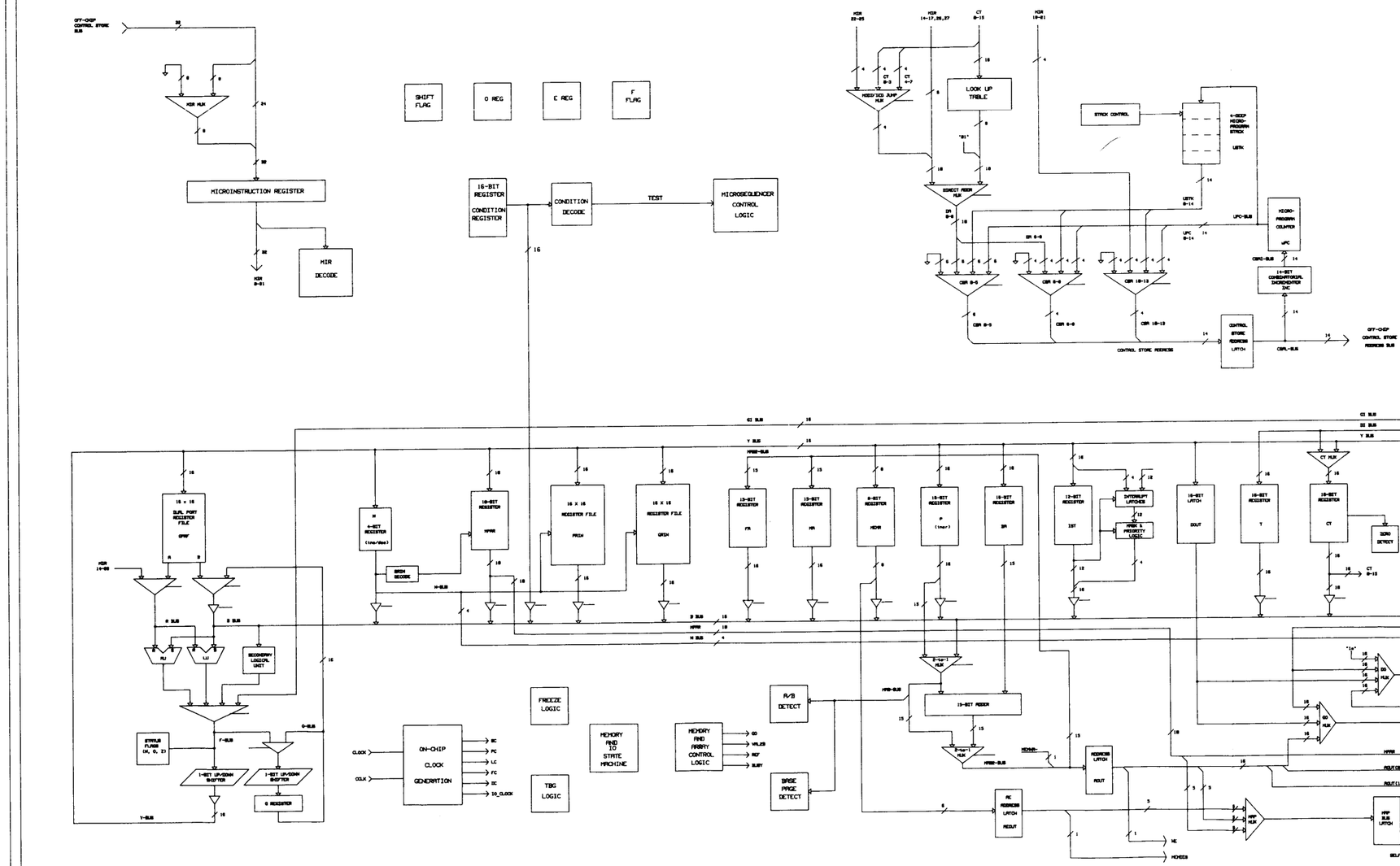


Figure 3-1. A400 Processor Chip Block Diagram

Clock Generation

General Description

The A400 board uses three main internal clocks. SC is a card version of the backplane SCLK (system clock). It has a period of 227 nanoseconds and a duty cycle of 40 percent. Processor Clock (PC) is equivalent to SC except that it may be frozen under certain conditions. A freeze is seen only by the A400 board and does not affect the backplane SCLK or any other cards. A freeze causes the short half-cycle of PC to be stretched for an integral number of SC cycles until the freezing condition goes away. Figure 3-2 is a block diagram of the clock generation logic.

A freeze is generated by the freeze logic if a microorder cannot be executed or if certain required interface logic is busy. Latch Clock (LC) is generated from PC but is asserted typically for only 75 nanoseconds (one and one-half FCLK cycles) at the end of the cycle. Since LC is generated from PC, LC is delayed accordingly if a freeze condition exists.

The Data Clock (DC–) follows SC– until there is an error-correction cycle. During an error-correction cycle, DC– toggles so that a rising edge is generated 2 FCLKs before the end of the short half-cycle. Data is clocked off of the DI-bus into the T and CT registers on DC– rising edges.

Theory of Operation

Clock generation is based on two oscillators. A 14.7456 MHz oscillator (U1509, 10A, Chapter 2) for the communications clock and a 22.0 MHz oscillator (U1510, 11A, Chapter 2) for the fast clock. The oscillators are hybrid crystal oscillators and reside on the A400 board. The output of the 22.0 MHz oscillator is brought onto the processor chip as the signal CLOCK–.

The major clock generation logic provides three J-K flip flops which comprise a divide-by-five circuit reducing CLOCK– to the pre-buffered system clock signal, PRE_SCLK+ of 227 nanoseconds. PRE_SCLK+ is then driven off of the processor chip and through a buffer on the board before becoming the backplane SCLK– with a 40 percent duty cycle. The output of the communications crystal oscillator is also driven through a buffer to become the backplane CCLK. A buffered version of CCLK is received by the processor chip and used to generate a 10 millisecond period for Time Base Generator (TBG) ticks and for refresh cycle scheduling.

The basic clocks and their relationships are given in Figure 3-3. An error correction cycle clock sequence is given in Figure 3-4.

The clock state machine is shown in Table 3-1. It has six valid states. Five states are used to generate the non-error correction cycle SCLK/SC. The sixth state is forced by the assertion of LONG_SHC–. LONG_SHC– is generated from the signal EC– (ECYC+ in the processor chip). EC– is generated by error-correction memory

arrays when they determine an error correction cycle is required during a memory read. The signal LONG_SHC- asserts during the second and third FC periods during SC's extended SHC. The state machine is not initialized at power-up, but will self-correct to a valid state sequence. There are three invalid states (100, 010, and 101) which will go to a valid sequence within three FC cycles.

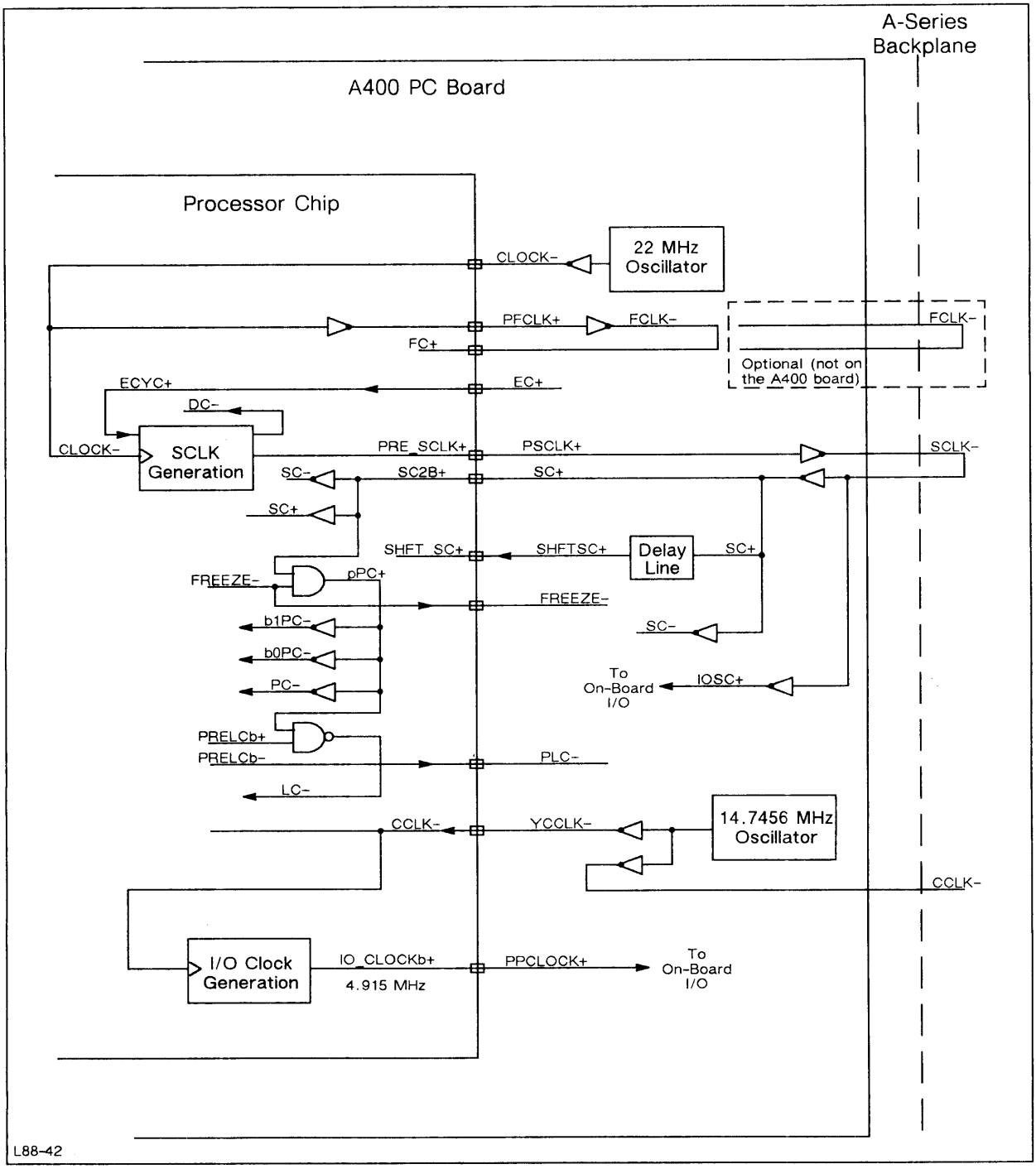


Figure 3-2. Clock Generation Logic Block Diagram

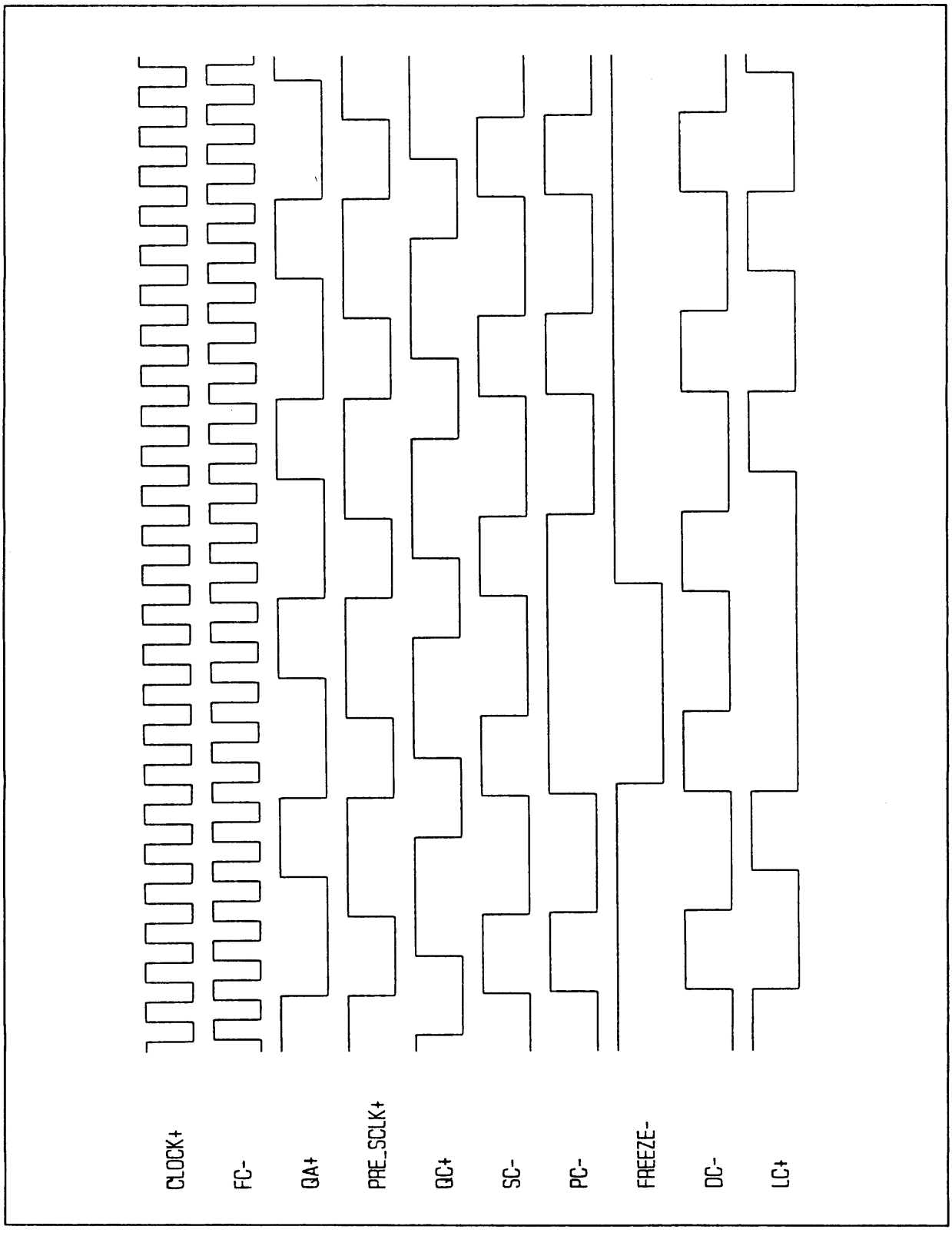


Figure 3-3. Processor Chip Clocks

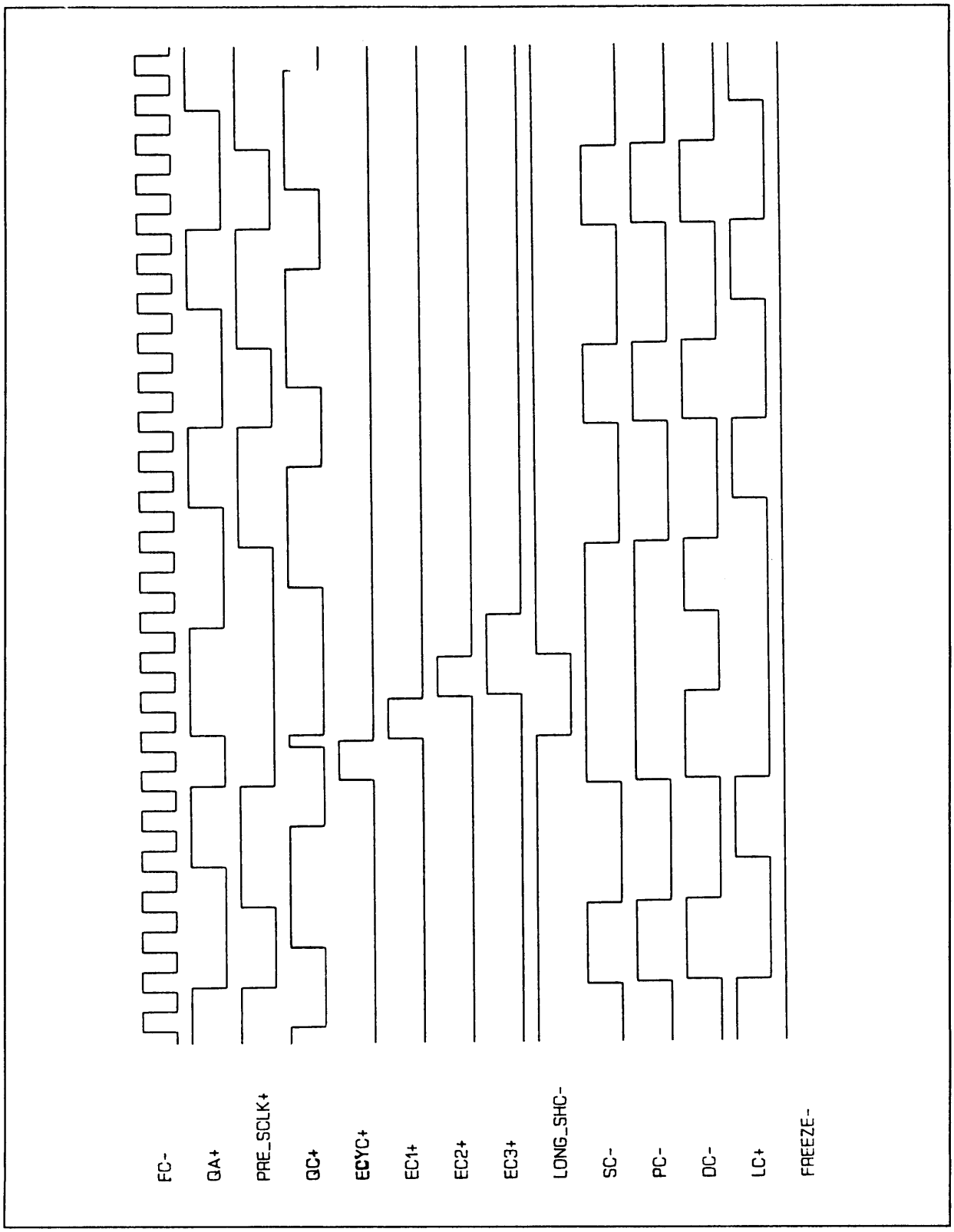


Figure 3-4. Error Correction Cycle Clocks

The state machine loops through a sequence of five states, generating the normal 40/60 SCLK. If LONG_SHC asserts, the short half-cycle of SCLK/SC will be extended by four additional FC cycles. That is, during the cycle where memory data is corrected, the short half-cycle of SCLK/SC will be 272 nanoseconds followed by a normal length long half-cycle.

SCLK/SC is generated by the following sequence of states. The state variable QB+ is PRE_SCLK+.

Non-EC SCLK/SC state sequence is as follows:
110, 000, 001, 011, 111, 110, 000, . . .

EC SCLK/SC state sequence is as follows:
110, 000, 100, 100, 100, 000, 001, 011, 111, 110, 000, . . .

A data clock (DC) is generated to be used for clocking of memory or I/O read data. DC– is used as a clock for the CT and T-Registers. It is derived by exclusive ORing SC– and EC3+. EC3+ is equivalent to LONG_SHC– but delayed one FC– cycle. DC–, effectively, provides a rising edge at every transition to state 000. This gives a rising-edge data clock pulse at every rising edge of SCLK–. If the short half-cycle is extended by an error correction, there will be an additional rising edge of DC– four FC– cycles into the short half-cycle. Thus, following the rising edge of DC– there is a full 227 nanoseconds left in the cycle. The counter, for example, will clock data in twice if an error correction occurs, the first clocked data being extraneous.

Table 3-1. Clock Generation State Machine

Present State			Flip-Flop Inputs						Next State		
QA	QB	QC	J0	K0	J1	K1	J2	K2	QA	QB	QC
0	0	0	0	1	0	1	1	0	0	0	1
0	0	1	0	0	1	0	1	1	0	1	1
0	1	0	1	1	0	1	0	1	1	0	1
0	1	1	1	0	1	0	0	0	1	1	1
1	0	0	0	1	0	1	1	0	0	0	0
1	0	1	0	0	1	0	1	1	1	1	0
1	1	0	1	1	0	1	0	1	0	0	0
1	1	1	1	0	1	0	0	0	1	1	0

The output of the 22 MHz oscillator (CLOCK–) on the A400 board is received by the processor chip. Internal to the processor chip, CLOCK– is used to generate PRE_SCLK+. PRE_SCLK+ is then driven off of the chip and onto the backplane as SCLK–. It is also driven off and back on the chip to generate FC+. This is to reduce skew between FC and SC. SC is generated for on-chip use as described in the following paragraph.

The A400 board receives SCLK– from the backplane and drives it into the processor chip as SC2B+. SC2B+ is used to generate SC+/–, PC+/–, and LC+. By using SCLK– off of the backplane to generate the board and chip timing, the entire system will be synchronized to the same clock regardless of backplane loading and the interboard skew is minimized. For other boards that might also require PC and LC, the two signals, along with SC+, used to generate them are available external to the chip. These two signals are PRELCb– and FREEZE–. By generating PC and LC external to the processor chip, the delay in generating and transmitting these clocks offsets the delay of getting SC+ onto the processor chip. This minimizes the skew on all clocks.

Internal to the processor chip, SC+/– and PC– are distributed by high-capacitive super buffers. Multiple copies of PC– are used to reduce loading and skew between the clock signals.

PC– is generated by NANDing SC+ with FREEZE–. Thus, whenever FREEZE– is asserted, PC– remains high. FREEZE– is only asserted for an integral number of SC cycles and only while SC is in its short half-cycle.

A timing diagram for the LC Generation circuit is shown in Figure 3-5. The PRELCb– signal is gated with PC– so that it will be deasserted soon after the rising edge of PC–. This also ensures that it is not asserted in a frozen cycle.

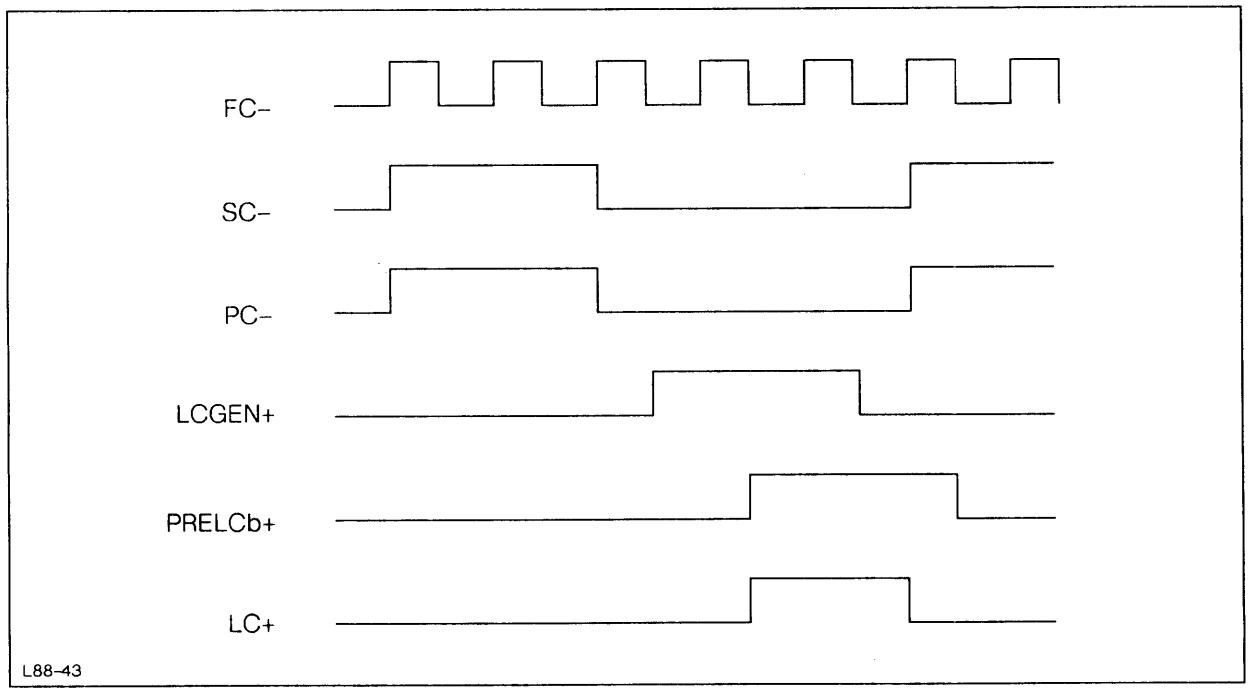


Figure 3-5. Timing Diagram of Latch Clock (LC) Generation

Microinstruction Register (MIR) and Decoders

General Description

The MIR latches the microinstruction at the beginning of the microcycle and drives the 32 bits of information during the cycle. The microinstruction format is variable depending on the operation specified in the Opcode-field. The physical format of the MIR is as follows:

Field	LSB	→	MSB
OP	MIR27	-	MIR31
ADRS (lower 6 bits)	MIR22	-	MIR27
BLOCK ADRS (upper 8 bits)	MIR14	-	MIR21
CNDX	MIR14	-	MIR17
SP2	MIR14	-	MIR17
SP1	MIR18	-	MIR22
SP0	MIR18	-	MIR21
IMMEDIATE	MIR14	-	MIR29
ALU	MIR10	-	MIR13
A-BUS	MIR23	-	MIR26
B-BUS	MIR5	-	MIR9
STORE	MIR0	-	MIR4

The Word Type and OP Decode section serves mainly to identify sets of word types used by other MIR decoders. For example, it identifies: Word Type 5 or 6 (WT_56), or Word Type 2 or 3 (WT_23) or OPs SPOT or SPOF, or the JTAB OP.

The condition encoder multiplexer receives a total of 16 signals corresponding to the conditions available in the CNDX-field. The condition multiplexer looks at the 16 condition signals and the four bits of the CNDX-field to produce CNDSPEC- which is the (negative) sense of the condition specified. In the OP-field, MIR bit 28 differentiates between the OP microorders conditional on the true or false sense. MIR bit 28 is combined with CNDSPEC- to generate the TEST+ signal to indicate that the condition sense specified in the OP-field has been met.

The SP2-field is decoded in a straightforward manner, generating a signal corresponding to each special microorder. OP-field information is used to determine if the SP2-field is present for the currently executing Word Type and to enable the decoders as needed.

The SP0/SP1-field of the MIR is used by other blocks of the processor, both before and after decoding. The SP1-field is actually the lower half of the SP0-field; that is, in terms of coding (refer to the Summary of Microorders by Field Table). The upper two bits of this field are qualified by the Word Type and other information for two purposes: 1) If the Word Type contains an SP1, the upper bit is zeroed so that it can be treated as the SP0-field; and 2) If the Word Type does not allow an SP0 or SP1, the SP0/SP1 decoders will be disabled. The SP0 decoders use these qualified signals and the MIR bus to generate a signal corresponding to most of the special microorders in the SP0/SP1-field. The decoders may be disabled if the OP is a conditional special operation (SPOC) and the condition sense is not met (TEST+). The lower three bits of the SP0/SP1-field are driven (after buffering) to the secondary ALU for execution.

The BBUS-field (not including R0 through R15 of the GPRF) is decoded in a straightforward manner directly from the MIR, generating a signal corresponding to each B-field microorder. These signals are then used to enable the contents of the appropriate register onto the B-bus.

The STOR-field (not including R0 through R15) is also decoded in a straightforward manner directly from the MIR, generating a signal corresponding to each STOR microorder. These signals are used to indicate at what destination to store the Y-bus at the end of the cycle. A STOR-field enable signal (STEN), generated from the SP0 decoders, will detect a conditional special operation (SPOT or SPOF) with STOR in the SP0-field and will disable the STOR decoders if the condition is not met.

Theory of Operation

The microinstruction register (MIR) is a 32-bit edge-triggered register. The register is composed of D flip-flops that have the true sense of the MIR bits available. The register is clocked on the rising edge of PC–, starting a microcycle. The MIR inputs are received primarily from outside the processor chip. The source of MIR bits 0 through 3 and bits 28 through 31 may be either CSD+[0:3] and bits CSD+[28:31] or the output of the UMI multiplexer. All other MIR bits are driven by the CSD-bus bits. The UMI multiplexer selects a NOP instruction to drive MIR bits 0 through 3 and 28 through 31 when either an unrecognized macroinstruction is executed or, more specifically, when no control store indicates recognition of the current microaddress. A UMI sets the Opcode field, MIR bits 31–28, to 0000 and the Store field, MIR bits 3–0, to 0100b, that is, store to the accumulator, ACC.

Refer to Tables 3-2 and 3-3 for microword formats and microorder field values.

Table 3-2. Microinstruction Word-Type Binary-Format Summary

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WORD TYPE 1	OP1					ABUS				SP0					SP2				ALU				BBUS					STOR				
WORD TYPE 2	OP2					ABUS				SP0					CNDX				ALU				BBUS					STOR				
WORD TYPE 3	OP3					ADRS							SP1		CNDX				ALU				BBUS					STOR				
WORD TYPE 4	OP4					ADRS							SP1		SP2				ALU				BBUS					STOR				
WORD TYPE 5	OP5					ADRL (LONG BRANCH ADDRESS)													ALU				BBUS					STOR				
WORD TYPE 6	OP6					DAT (IMMEDIATE DATA)													ALU				BBUS					STOR				
WORD TYPE 1S	OP1					ABUS				ALUS*					SP2				SPEC				BBUS					STOR				
WORD TYPE 2S	OP2					ABUS				ALUS*					CNDX				SPEC				BBUS					STOR				
WORD TYPE 3S	OP3					ADRS							ALUS*		CNDX				SPEC				BBUS					STOR				
WORD TYPE 4S	OP4					ADRS							ALUS*		SP2				SPEC				BBUS					STOR				
WORD TYPE 5S	OP5					ADRL (LONG JUMP TABLE ADDRESS)													SPEC				BBUS					STOR				

L8200-4

* Special microorder in ALUS field when ALU field is coded SPEC.

Table 3-3. Summary of Microorders by Field

Field										
Code	**OP**	**CNDX**	**SP0**	**SP1**	**SP2**	**ALUS**	**ALU**	**ABUS**	**BBUS**	**STOR**
00000	IMM	SF	NOP*	NOP*	NOP*	UMPY	SPEC	A	A	A
00001	IMM	F	LDQ	LDQ	CMDW	TMPY	SBAC	B	B	B
00010	IMM	ALOV	RR1	RR1	DCT	SM2C	SBBC	X	X	X
00011	IMM	CF	RL1	RL1	CLF	RMLC	ADDC	Y	Y	Y
00100	IMM	YZ	LR1	LR1	STF	DNRM	ADBC	ACC*	ACC*	ACC
00101	IMM	Y15	LL1	LL1	IP	SNRM	CMBC	HP1**	HP1**	HP1**
00110	IMM	B15	AR1	AR1	LWF	DIV	ADAC	HP2**	HP2**	HP2**
00111	IMM	INTF	AL1	AL1	LWE	DIV1	CMAC	USR**	USR**	USR**
01000	JMPL	IORQ	RDP	RDP	CMID	SWAP	ZERO*	S0	S0	S0
01001	JMPL	PON	IN	IN	RDP	SWZU	CAND	S1	S1	S1
01010	JSBL	MPEN	RDB	RDB	WRIO	SWZY	XNOR	S2	S2	S2
01011	JSBL	O	STE	STE	DN	ZUY	XOR	S3	S3	S3
01100	JMP	E	CLE	CLE	FCHP	ZLY	AND	S4	S4	S4
01101	JMP	INTP	FCIN	FCIN	RDIO	SRG	INOR	S5	S5	S5
01110	JSB	CTZ4	ACF	ACF	CT30	RL4	NAND	S6	S6	S6
01111	JSB	CTZ	IP	IP	CT74	ASG	IOR	S7	S7	S7
10000	JMPF		STOR						GRIN	GRIN
10001	JMPF		----						FA	WRP
10010	JMPT		----						SRIN	SRIN
10011	JMPT		----						P	P
10100	JSBF		----						Q	NOP*
10101	JSBF		----						T	WRB
10110	JSBT		----						IST	IST
10111	JSBT		----						N	N
11000	JTAB		IFCH						PRIN	PRIN
11001	----		BFB						MA	CWRB
11010	RTN		CK2						MEMR	MEMR
11011	NOP*		ENOE						CT	CT
11100	RTNF		STO						SR	SR
11101	SP0F		CLO						MAP	MAP
11110	RTNT		FCHB						CAB	CAB
11111	SP0T		LDBR						CXY	CXY

OP Field Divisions:

OP1 =	OP2 =	OP3=	OP4 =	OP5 =	OP6 =
JTAB	SP0T	JMPF	JMP	JMPL	IMM
NOP	SP0F	JMPT	JSB	JSBL	
RTN	RTNT	JSBF			
	RTNF	JSBT			

* Default Microorder.

** Reserved register for Hewlett-Packard (HP1 and HP2) and user (USR).

L87-76

OP-Field

MIR bits 27 through 31 are decoded by a block of combinational logic to provide information on Word Types and OP-field to the MIR decoders and other places. There are six word types. Word types 1 through 5 also have a "special" format when a SPEC instruction appears in the ALU field. Following is a summary of the logic equations used:

```
WT12_OP  = MIR31 * MIR30                      (Word Type 1 or 2)

WT56_OP  = -MIR31 * (-MIR29 + -MIR30)         (Word Type 5 or 6)

JTAB     = WT12_OP * (-MIR29 * -MIR28)        (JTAB OP)

SP0C     = WT12_OP * MIR29 * MIR27            (SP0T or SP0F OP)
```

SP0/SP1/SP2-Field Decode

The three microcode special fields (SP0, SP1, and SP2) all reside between bits 14 through 22 of the MIR. The existence of the SP0/1/2-fields is dependent on the word type. The following chart shows when each field is present. The signal SPEC is an ALU-field microorder that indicates either the need for a primary ALU special function or a secondary LU operation.

Word Type	SPEC	SP0	SP1	SP2
1	0	yes	no	yes
1	1	no	no	yes
2	0	yes	no	yes
2	1	no	no	yes
3	0	no	yes	no
3	1	no	no	no
4	0	no	yes	yes
4	1	no	no	yes
5	X	no	no	no
6	X	no	no	no

The SP2-field decoder is implemented using two 3-to-8 decoders. The inputs to the decoders are MIR14 (LSB) through MIR16 (MSB). MIR17 selects between the decoders. The decoder enable input equation is as follows:

```
ESP2D = ((MIR31 XOR MIR29) * MIR30)
```

The SP0 and SP1 fields have most of their MIR bits in common. The two fields share MIR bits 18 through 21. SP0-field microorders also include MIR22. For word type 2 microinstructions with SPOT or SPOF in the OPCODE-field, the condition specified in the CNDX field must be met to enable the SP0 decoder. It should be

specified in the CNDX field must be met to enable the SP0 decoder. It should be noted that SP0/SP1 microorders that have MIR21 = logic 1, need to be decoded for device enable signals. The SP0/SP1 microorders that have MIR21 = logic 0 are concerned with ALU shifting functions and loading the Q-Register.

The decoding of the SP0/SP1 fields is done in two parts. One part is the decoding of SP0 only microorders indicated by MIR22 = logic 1. The other decoder handles the microorders that are common between SP0 and SP1. These are microorders with MIR22 = logic 0 and MIR21 = logic 1. Both decoders are implemented with a 3-to-8 decoder using MIR18 (LSB) through MIR20 (MSB) as inputs. The two decoder enables are:

```
ESPOH = ((MIR21 * -SPEC) * (-SPOC + TEST) * (WT12_OP * MIR22))
ESPOL = ((MIR21 * -SPEC * -WT56_OP) * (-SPOC + TEST) *
        (WT12_OP * MIR22)')
```

where:

```
SPOC = WT12_OP * MIR29 * MIR27  (indicates SPOT or SPOF opcode)
SPEC = -MIR13 * -MIR12 * -MIR11 * -MIR10
```

Table 3-4. SP0/SP1-Field Decoding

MIR Bit 22	20	19	18	Field	Signal Name	Interpretation
0	0	0	0	SP0/SP1	RDP0-	preload memory read with address in P
0	0	0	1	SP0/SP1	IN-	increment N
0	0	1	0	SP0/SP1	PRDB0-	preload memory read with address on B-bus
0	0	1	1	SP0/SP1	STE-	set E flag
0	1	0	0	SP0/SP1	CLE-	clear E flag
0	1	0	1	SP0/SP1	FCIN-	force carry in
0	1	1	0	SP0/SP1	ACF-	use carry flag (CF) for ALU carry in
0	1	1	1	SP0/SP1	IP0-	increment P explicitly
1	0	0	0	SP0	IFCH-	do an interrupt instruction fetch
1	0	0	1	SP0	BFB-	memory read with B-bus address, assert RNI-
1	0	1	0	SP0	CK2-	for FPP, enable double clocking
1	0	1	1	SP0	ENOE-	enable O and E flags to be set by OVR and CF
1	1	0	0	SP0	STO-	set O flag
1	1	0	1	SP0	CLO-	clear O flag
1	1	1	0	SP0	PFCHB-	preload instruction fetch with B-bus address
1	1	1	1	SP0	LDBR-	load base register (BR) from Y-bus

ABUS-Field Decoding

The inputs for the A-bus enables of the GPRF come mostly from the A-bus field of the MIR (bits 23 through 26). For the JTAB microorder, the A-bus field address is used with the low order bit forced to zero if counter bit 11 is 0. For all word type 1 and 2 operations (except for JTAB), the A-bus field bits are used directly. For all other word types (that is, 3, 4, 5, 6), the A-bus decoder inputs defaults to 0100 which will select R04 which is the accumulator. Table 3-5 is a summary of the A-field decoding.

The equations for the input of the 4-to-16 decoder of the GPRF are as follows:

(LSB) EN_PA0+ = MIR23 * WT12_OP * (JTAB * -CT11)'

EN_PA1+ = MIR24 * WT12_OP

EN_PA2+ = MIR25 + -WT12_OP

(MSB) EN_PA3+ = MIR26 * WT12_OP

Table 3-5. A-Field Decoding

Word Type	JTAB	CT11	A-Bus Decoder Inputs
1,2	0	X	MIR23 (LSB) thru MIR26 (MSB)
1,2	1	1	MIR23 (LSB) thru MIR26 (MSB)
1,2	1	0	0 (LSB), MIR24 thru MIR26 (MSB)
3,4,5,6	X	X	0100 (R04 accumulator)

where: CT11 = counter bit 11
JTAB = WT12_OP * -MIR28 * - MIR29

BBUS-Field Decoding

The BBUS-field of the MIR (bits 5 through 9) is decoded once for the micromachine in general and separately for the GPRF. The BBUS-field determines what data is enabled onto the B-bus.

The main micromachine decoding is handled by two 3-to-8 decoders. The decoders use MIR5 (LSB) through MIR7 (MSB) as inputs and are enabled by MIR9. MIR8 is used to select between the two decoders. The signals that result are listed in Table 3-6.

When MIR9 is low (logic 0), the GPRF is being addressed. The GPRF B-bus enables are generated from the B-bus field plus information from the counter and the last memory read status register. Counter bit 11 determines an A (CT11=0) or B (CT11=1) register access for CAB microorder. Similarly, counter bit 3 determines X (CT3=0) or Y (CT3=1) register access on the CXY microorder. When a memory read is determined to be from the A- or B-Register (remember these registers are memory mapped to physical address 0 and 1), the LRMAB0- signal preserves the state of address bus bit 0. If the TAB microorder is used and the last read was from the A- or B-Registers, A or B needs to be driven onto the B-bus. The generation of the GPRF B-bus enable inputs is as follows:

```
(LSB)   EN_PB0+  = -(-MIR9 * -MIR5 + -MIR5 * -CT11
                    + MIR9 * MIR6 * MIR5 * -CT3
                    + MIR9 * -MIR6 * -LRMAB0)

        EN_PB1+  = -(-MIR6 + (MIR9 * -MIR5))

        EN_PB2+  = -(MIR9 + -MIR7)

(MSB)   EN_PB3+  = -(MIR9 + -MIR8)
```

Table 3-6. B-Field Decoding

MIR Bit		Signal Name	Interpretation
9	8765		
1	0000	eGRINb-	enable general registers indexed by N onto the B-bus
1	0001	eFAb-	enable fetch address register onto the B-bus
1	0010	eSRINb-	enable special registers indexed by N onto the B-bus
1	0011	ePb-	enable P-Reg onto the B-bus
1	0100	eNQb-	enable Q-Reg onto the B-bus
1	0101	eTABb-	enable T (memory data), A, or B-Reg onto the B-bus
1	0110	eISTb-	enable interrupt status register onto the B-bus
1	0111	eNb-	enable N-Reg onto the B-bus
1	1000	ePRINb-	enable privileged registers indexed by N onto the B-bus
1	1001	eMAb-	enable memory address register onto the B-bus
1	1010	eMEMRb-	enable memory (control) register onto the B-bus
1	1011	eCTb-	enable counter register onto the B-bus
1	1100	eLSRb-	enable light and switch register onto the B-bus
1	1101	eMAPb-	enable map address bus register onto the B-bus
1	1110	eCAb-	enable conditionally the A- or B-Reg onto the B-bus
1	1111	eCXYb-	enable conditionally the X- or Y-Reg onto the B-bus

STORE-Field Decoding

The STORE-Field of the MIR (bits 0 through 4) is decoded similarly to the B-field bits in that decoding is done once for the micromachine in general and once for the GPRF. The store field determines the dispensation of the Y-bus.

The main micromachine decoding is handled by two 3-to-8 decoders. The decoders use MIR0 (LSB) through MIR2 (MSB) as inputs and are enabled by ESTDEC+. MIR3 selects between the two decoders. Table 3-7 is a summary of the STORE-field decoding. The logic equation for ESTDEC+ is as follows:

ESTDEC+ = (MIR4 * STEN)

where:

STEN = ((MIR22 * WT12_OP)' * -MIR21 * -TEST * WT12_OP * MIR29 * MIR27)'

and

TEST is the state of condition specified in the CNDX field

The signal STEN is always asserted except for the case of the SPOT or SPOF opcodes. These opcodes, when used with the STORE microorder (in SP0-field), should permit a store to occur only when the condition being tested (as specified in the CNDX-field) is true (logic 1) or false (logic 0) accordingly. The STEN equation ensures that this is the case.

Table 3-7. STORE-Field Decoding

MIR Bit		Signal Name	Interpretation
4	3210		
1	0000	lyGRIN–	load the general registers indexed by N onto the Y-bus
1	0001	lyWRP–	write Y-bus data to memory using address in P
1	0010	lySRIN–	load the special registers indexed by N from the Y-bus
1	0011	lyP–	load the macro program counter (P) from the Y-bus
1	0100	NOP	do not store the Y-bus anywhere, i.e. do nothing
1	0101	lyWRB–	write Y-bus data to memory using address on the B-bus
1	0110	lyIST–	load the interrupt status register from the Y-bus
1	0111	lyN–	load the N-Reg from the Y-bus
1	1000	lyPRIN–	load the privileged registers indexed by N from the Y-bus
1	1001	PLYCWRB–	preload conditional memory write using B-bus address
1	1010	lyMEMR–	load the memory (control) register from the Y-bus
1	1011	lyCT–	load the counter register from the Y-bus
1	1100	lyLSR–	load the LED register from the Y-bus
1	1101	lyMAP–	load the map address bus register from the Y-bus
1	1110	lyCAB	load conditionally the A- or B-Reg from the Y-bus
1	1111	lyCXY–	load conditionally the X- or Y-Reg from the Y-bus

When MIR4 is low (logic 0), the GPRF is being addressed. The GPRF clock enables are generated from the STORE-field plus information from the counter and the last memory read status register. Counter bit 11 determines an A (CT11=0) or B (CT11=1) register write for CAB microorder. Similarly, counter bit 3 determines X (CT3=0) or Y (CT3=1) register write on the CXY microorder. When a memory write is determined to refer to the A- or B-Register (remember these registers are memory mapped to physical address 0 and 1), the MAB0+ signal identifies the state of address bus bit 0. If the WRP or WRB microorder is used and the address refers to the A- or B-Register, then a GPRF write must take place to R0 or R1. The generation of the GPRF clock enable inputs is as follows:

```
(LSB)   CLK_EN0+ = (-MIR4 * -MIR0 + MIR4 * -MIR0 * -CT11
                     + MIR4 * MIR1 * MIR0 * -CT3
                     + MIR4 * -MIR1 * -MAB0)'

        CLK_EN1+ = (-MIR1 + (MIR4 * -MIR0))

        CLK_EN2+ = (-MIR4 + MIR2)

(MSB)   CLK_EN3+ = (-MIR4 + MIR3)
```

The CLK_ENx+ signals determine to which register to write. An actual write is only enabled if a GPRF write is indicated. The GPRF is written for either an A/B register write (address 0 or 1), a CAB or CXY microorder in the store field, or when a GPRF register write is coded in the STORE-field (MIR4 = 0). The assertion of lyGPRF+ enables a GPRF register write to the register selected by the CLK_ENx+ signals.

```
lyGPRF+ = STEN * (-MIR4 + ABWR + lyCAB + lyCXY)
```

MRG Instruction Decoder

The Memory Reference Group (MRG) instructions are treated differently than the other instruction groups. Since the MRG instructions usually involve a memory reference, the CPU attempts to start this memory access concurrently with the microinstruction that contains the JTAB microorder. To accomplish this, the MRG decoder looks at counter bits 11 through 15 (CT11 through CT15) as well as JTAB to determine when to start a special "early" memory reference. The MRG decoder multiplexes the non-MRG decoded, that is, "special", memory reference signals (PFCHB- and PRDB0- from the SP0/SP1 decode and PLYCWRB- from the store decode) with the additional MRG references. The JTAB line toggles the multiplexer between passing non-MRG decoded (out of the MIR) signals and the CT-decoded signals. The equations for the logic are as follows:

```
RDB-    = JTAB * (-CT14 + -CT13 + -CT12) * (CT14 + CT13 + CT12)
            * (CT15 + CT14 + CT12 + CT11)
            * (CT15 + CT14 + CT13 + -CT11)
            + -JTAB * PRDB0-

FCHB-   = JTAB * (CT15 + CT14 + -CT13 + CT12 + -CT11) + -JTAB * PRCHB-

LYCWRB  = JTAB * (-CT14 + -CT13 + -CT12) + -JTAB * PLYCWRB-
```

Microsequencer

General Description

The microsequencer generates the 14-bit address for the control store. The 14-bit wide address allows the addressing of 16k microwords.

The microsequencer allows the selection of the 14-bit control store address from three sources or zero. The three sources are as follows:

- the microprogram counter (uPC)
- the top address in the 4-deep microprogram stack
- the direct address

On every cycle, the control store address is incremented and stored into the microprogram counter. On a jump to subroutine, the stack pointer is incremented and then the incremented control store address is pushed onto the four-deep stack. On a return from subroutine, the top of stack address is selected and then the stack pointer is decremented. The stack pointer always points to the top of the stack.

The selection of the microsequencer multiplexer and control of the stack is determined by the five OP-code bits from the OP-field of the microinstruction, TEST+, UMI–, BPON–, and MTO–. TEST+ indicates that the condition as specified in the CNDX-field of the microinstruction and the condition sense as specified in the OP-field are met. UMI– indicates that the current control store address references an unimplemented microinstruction, that is, nonexistent microcode memory. BPON– indicates a power-on/reset condition, and MTO– indicates a microcode time out. The conditions indicated by UMI–, BPON–, and MTO– force a zero onto the control store address bus.

The direct address is generated from a number of sources. A hardware look up table takes the counter data and generates a vector address which is selected when a JTAB microorder is executed. When the SP2-field contains the CT30 or CT74 microorder, counter bits 3–0 or 7–4, respectively, are selected for the lower four bits of the direct address. Counter bits 3–0 are also selected if a Word Type 5 (JMPL or JSBL) has SPEC in the ALU-field, that is, a modified jump command. For any other jump or jump to subroutine microorders, the TARGET field of the MIR is enabled onto the Direct Address bus.

The latched control store address from the sequencer is driven off-chip and directly to the control store.

Sequencer Multiplexer and Control

The sequencer provides a 14-bit microaddress. The sequencer multiplexer is a 4-to-1 multiplexer with inputs from the microprogram counter (uPC), the microprogram stack (uSTK), the Direct Address inputs (DA), and from zero (ZERO).

The programmer is allowed to specify a 14-bit jump address or a 6-bit jump address. To facilitate this the sequencer multiplexer is divided into a least significant slice (6 bits) and a most significant slice (8 bits). The most significant slice is yet divided into two 4-bit slices so that the four most significant bits, CSA[13:10], may be zeroed independently of the remainder of the control store address. Each slice receives different control signals.

The sequencer multiplexer control is determined by the OP-field bits of the microinstruction register (MIR[31:27]), the TEST+ condition, BPON–, MTO–, and UMI–.

All 14 bits of the control store address are forced to zero upon a microcode time out (MTO–), an unimplemented microcode address (UMI–), or a power on condition (BPON–). The four most significant bits (CSA[13:10]) are forced to zero on a JTAB to force a base set address (addresses 0X0100 through 0X01FF hex for a jump through the look up table).

ZERO_SEQ+ = (MTO– + ZERO_AD– + BPON–)

JTAB+ = MIR31 * MIR30 * MIR29– * MIR28– * MIR27–

where

ZERO_AD– = UMI– synchronized with PC–

There are four internal control signals for the sequencer. These are USTK_ENB+, PTR_UP+, JP_L_OP+, and RTN_OP+. These signals are combined and together with the ZERO_SEQ+ and JTAB+ signals control the sequencer multiplexer. They are generated from the OP-field bits of the microinstruction register.

USTK_ENB+ enables the microprogram stack. USTK_ENB+ is active when the micro-order is a jump to subroutine, a return from subroutine, or a jump table microorder. On conditional microorders, it is only active if the condition and the sense are met.

							Microorder
USTK_ENB+	=	MIR31 *	MIR30–	* MIR29	* TEST		JSBF,JSBT
	+	MIR31 *	MIR30	* MIR29	* MIR27–	* TEST	RTNF,RTNT
	+	MIR31–*	MIR30	* MIR28			JSBL,JSB
	+	MIR31 *	MIR30	* MIR29–	* MIR27–		JTAB,RTN

PTR_UP+ is used to indicate whether a value is to be pushed onto the microprogram stack (PTR_UP+ is asserted) or popped off the microprogram stack (PTR_UP+ is deasserted) when USTK_ENB+ is active, that is, the stack is enabled. It is also used to generate the control store signals for the low order 6-bit slice of the sequencer multiplexer (CSA[0:5]).

PTR_UP+ is active when the microorder is an unconditional jump or a jump to subroutine and on a conditional jump or a jump to subroutine when the condition and sense are met.

						Microorder
PTR_UP+ =	MIR31	* MIR30-	* TEST			JMPF,JMPT,JSBF,JSBT
	+MIR31-	* MIR30				JMPL,JSBL,JMP,JSB
	+MIR31	* MIR30	* MIR29-	* MIR28-	* MIR27-	JTAB

JP_L_OP+ is used to generate the select signals for the upper 8-bit slice of the sequencer multiplexer. JP_L_OP+ is active on long jumps or long jumps to subroutines, and on a jump table microorder.

						Microorder
JP_L_OP+ =	MIR31-	* MIR30	* MIR29-			JMPL,JSBL
	+MIR31	* MIR30	* MIR29-	* MIR28-	* MIR27-	JTAB

RTN_OP+ is used to generate the select signals for the sequencer multiplexers. RTN_OP+ is active on a return microorder or a conditional return from subroutine if the condition and sense are met.

						Microorder
RTN_OP+ =	MIR31	* MIR30	* MIR29	* MIR27-	* TEST	RTNF,RTNT
	+MIR31	* MIR30	* MIR29-	* MIR28	* MIR27-	RTN

Functionally the 14-bit sequencer multiplexer is divided into three slices. The first slice consists of CSA[5:0], the second consists of CSA[9:6], and the third consists of CSA[13:10]. Each slice has its own select signals generated from the internal control signals PTR_UP+, JP_L_OP+, RTN_OP+, ZERO_SEQ+, and JTAB+. These select signals are $\overline{S11\_SQMX}$+, $\overline{S10\_SQMX}$+, $\overline{S21\_SQMX}$+, S20_SQMX+, S31_SQMX+, S30_SQMX+ and each pair controls the generation of $\overline{CSA}$[5:0], CSA[9:6], and $\overline{CSA}$[13:10], respectively. The selection is as follows:

Sx1_SQMX	Sx0_SQMX	Selected Input
0	0	Microprogram Counter (uPC)
0	1	Zero
1	0	Microprogram Stack (uSTK)
1	1	Direct Address Bus (DA)

For CSA[5:0]:
```
S11_SQMX = (PTR_UP+ + RTN_OP+) * ZERO_SEQ-
S10_SQMX = PTR_UP+ + ZERO_SEQ+
```

For CSA[9:6]:
```
S21_SQMX = (JP_L_OP+ + RTN_OP+) * ZERO_SEQ-
S20_SQMX = JP_L_OP+ + ZERO_SEQ+
```

For CSA[13:10]:
```
S31_SQMX = (JP_L_OP+ + RTN_OP+) * (ZERO_SEQ- * JTAB-)
S30_SQMX = RTN_OP+ + ZERO_SEQ+ + JTAB
```

The only difference between the second and third slice is that a JTAB microorder results in the third slice being zero.

The output of the sequencer multiplexer is latched into the Control Store Address latch on the falling edge of PC-.

OP-Field Microorder	TEST	ZERO_SEQ	CSA[13:10]	CSA[9:6]	CSA[5:0]	FE	PUP
IMM	X	0	uPC	uPC	uPC	0	0
JMPL	X	0	DA	DA	DA	0	1
JSBL	X	0	DA	DA	DA	1	1
JMP	X	0	uPC	uPC	DA	0	1
JSB	X	0	uPC	uPC	DA	1	1
JMPF	0	0	uPC	uPC	uPC	0	0
JMPF	1	0	uPC	uPC	DA	0	1
JMPT	0	0	uPC	uPC	uPC	0	0
JMPT	1	0	uPC	uPC	DA	0	1
JSBF	0	0	uPC	uPC	uPC	0	0
JSBF	1	0	uPC	uPC	DA	1	1
JSBT	0	0	uPC	uPC	uPC	0	0
JSBT	1	0	uPC	uPC	DA	1	1
JTAB	X	0	ZERO	DA	DA	1	1
RTN	X	0	uSTK	uSTK	uSTK	1	0
NOP	X	0	uPC	uPC	uPC	0	0
RTNF	0	0	uPC	uPC	uPC	0	0
RTNF	1	0	uSTK	uSTK	uSTK	1	0
RTNT	0	0	uPC	uPC	uPC	0	0
RTNT	1	0	uSTK	uSTK	uSTK	1	0
SPOF	X	0	uPC	uPC	uPC	0	0
SPOT	X	0	uPC	uPC	uPC	0	0
X	X	1	ZERO	ZERO	ZERO	X	X

Incrementer

The incrementer is a combinatorial circuit which takes the latched control store address (CSAL[0:13]) and increments the 14-bit value. The output of the incrementer (CSAI[0:13]) is latched into the microprogram counter, uPC, on the rising edge of PC- and is pushed onto the 4-deep microprogram stack, uSTK, when one of the following occurs:

1. an unconditional jump to subroutine (JSBL or JSB)
2. a conditional jump to subroutine in which the condition and sense are met (JSBF or JSBT)
3. a JTAB is in the OP-field of the microinstruction on this cycle

The incremented value of the control store address, that is, the return address, is latched in the stack register with clock LC+.

The logic for the incrementer consists of an exclusive-OR of the current bit with the AND of all lower order bits as shown in the following equations:

$$CSAI_N = CSAL_N \text{ XOR } (CSAL_{N-1} * CSAL_{N-2} * \ldots * CSAL_0)$$
$$CSAI_0 = CSAL_0 \text{ XOR } '1'$$

Microprogram Counter (μPC)

The microprogram counter is a 14-bit register which latches the incremented control store address, CSAI[0:13], on the rising edge of PC–. The output of the microprogram counter, UPC[0:13], is used as one of the sources to the sequencer multiplexer. UPC[0:13] is the default selection.

Four-Deep Stack

The microprogram stack consists of two portions, the stack pointer and the four stack registers. The stack pointer is implemented with a 2-bit up/down counter. The counter is cleared by BPON–. The counter is enabled to count by USTK_ENB+ (that is, when there is a jump to subroutine or a return). The up/down signal is controlled by PTR_UP+. When PTR_UP+ is asserted and the stack is enabled by USTK_ENB+ (jump to subroutine microorders), the counter will increment on the rising edge of PC+, the end of the short half-cycle. When PTR_UP+ is deasserted and the stack is enabled by USTK_ENB+ (returns from a subroutine), the counter will decrement on the rising edge of PC+, the end of the short half-cycle.

The output of the stack counter, PTR0_USTK+ and PTR1_USTK+, is the 2-bit binary representation of the stack cell addressed. The output of the counter goes to a 2-to-4 decoder and a latch. The latch is gated on PC– and captures the address of the stack register selected at the start of the cycle. The address is latched so that the uSTK value seen by the sequencer multiplexer does not change when the stack counter changes. This guarantees the setup of data on the multiplexer and control store latch. The output of this latch, PTR0_L+ and PTR1_L+, are the select lines for the microsequencer stack multiplexers.

The 2-to-4 decoder is enabled by a push operation, that is, the stack is enabled (USTK_ENB+ is asserted) and it is a subroutine jump (PTR_UP+ is asserted). The output of the decoder enables the clock to the selected stack register.

Data to the four stack registers, microstack registers A through D, is the output of the microprogram counter, UPC[0:13] and is clocked into the selected stack register on the rising edge of LC+. The output of each stack register is the input into a 4-to-1 multiplexer. The select for the multiplexer comes from the latched stack pointer. The output of the stack multiplexer is the uSTK input to the sequencer multiplexer.

The stack is only four deep but can roll over without warning. It is reset upon a power-on condition, that is, BPON– resets the stack pointer to zero, microstack register A. Therefore, microsubroutines may only be nested four deep without incurring unpredictable results.

Direct Address Generation

The direct inputs for sequencer bits 0 through 9 are provided by the Direct Address Bus (DA[0:9]). The direct inputs for bits 10 through 13 come directly from the microinstruction register, MIR[21:18], since these bits are only specified by long jumps. Direct Address Bus bits 0 through 9 may come from the counter, the Look-Up Table, or from the microinstruction register. The selection of the source of these bits is generated from the microinstruction.

The Direct Address Bus is selected in the case of jumps or a JTAB. All other instances are "don't cares" for DA[0:9] generation. The selection of DA bits occurs in two stages.

The second stage selects between a JTAB or a jump microinstruction. The only jump in microinstruction word types 1 or 2 is a JTAB, so the signal indicating that the present OP-field microorder is a word type 1 or 2 instruction, WT12_OP+, is used as the select for a 16-bit wide 2-to-1 multiplexer. If WT12_OP+ is asserted, the output of the Look-Up Table (LUT[7:0]) is selected. The Look-Up Table output is placed on the low order bits DA[7:0] and DA[9,8] are set to "01". When WT12_OP+ is deasserted, that is, the microinstruction is not word type 1 or 2, the output of the first stage is selected for bits 3 through 0 and MIR27, MIR26, and MIR[17:14] are selected for DAB bits 9 through 4.

```
WT12_OP+ = MIR31 * MIR30
```

The first stage of the direct address generation is a 4-to-1 multiplexer which selects between MIR[25:22], counter bits 7 through 4 (CT[7:4]), or counter bits 3 through 0 (CT[3:0]), for DA bits 3 through 0. The select signals for the multiplexer are CT74_SP+ and SP2_CT+ (Select Counter). The select signals are as follows:

SP2_CT	CT74_SP	MUX Output
0	0	MIR[25:22]
0	1	MIR[25:22]
1	0	CT[3:0]
1	1	CT[7:4]

The signal CT74 is decoded from the SP2-field of the microinstruction (MIR[17:14]). The instruction CT30 is also decoded from the SP2-field of the microinstruction and is one of the signals used to generate SCT.

```
CT74_S      = WT14  * MIR17  * MIR16  * MIR15  * MIR14

SP2_CT      = CT74  + CT30 + WT5_MODJP

CT30        = WT14  * MIR17  * MIR16  * MIR15  * MIR14-

WT14        = MIR30 * (MIR31 XOR MIR29)              <-- word type 1 or 4

WT56_OP     = MIR31- * (MIR30- + MIR29-)             <-- word type 5 or 6

WT5_MODJP   = WT56_OP * MIR13- * MIR12- * MIR11- * MIR10-  <-- modified jump
```

One of the two sets of counter bits are selected when the microorder is a modified jump microorder (that is, Word Type 5 or 6 and SPEC is coded in the ALU-field) or CT74 or CT30 is selected in the SP2-field. If a modified jump is specified, counter bits 3 through 0 are selected. CT74 and CT30 are generated from the SP2-field when the microinstruction is of Word Type 1 or 4. DAB[13:10] are always MIR[21:18]. This is summarized in the following table:

SP2CT	CT74_SP	WT12_OP	DAB[13:10]	DAB[9,8]	DAB[7:4]	DAB[3:0]
X	X	1	MIR[21:18]	'01'	LUT[7:4]	LUT[3:0]
0	0	0	MIR[21:18]	MIR[17,16]	MIR[15,14,27,26]	MIR[25:22]
0	1	0	MIR[21:18]	MIR[17,16]	MIR[15,14,27,26]	MIR[25:22]
1	0	0	MIR[21:18]	MIR[17,16]	MIR[15,14,27,26]	CT[3:0]
1	1	0	MIR[21:18]	MIR[17,16]	MIR[15,14,27,26]	CT[7:4]

Look-Up Table

The look-up table is a block of logic which maps the Counter outputs to a value which lies between 00h and FFh hex. Table 3-8 gives the Control Store address range for the different types of microinstructions. The look-up table output is selected on a JTAB microinstruction and is therefore the first step in executing a macroinstruction. When the look-up table output is selected as the output of the sequencer multiplexer, the resulting control store address is in the range of 0100h to 01FFh. On a JTAB, the four most significant bits of the sequencer (CSA[13:10]) are zero, the next two (CSA[9,8]) are "01", and bits 7 through 0 (CSA[7:0]) are the address generated by the look-up table.

The look-up table addresses (LUT[7:0]) are generated from the Counter outputs, CT[15:0] in the following manner:

```
LUT7    =   CT15- * CT14- * CT13- * CT12-
          + CT14- * CT13- * CT12- * CT10- * CT9 * CT8 * CT6-
          + CT14- * CT13- * CT12- * CT10- * CT9 * CT8 * CT7-
          + CT14- * CT13- * CT12- * CT10- * CT9 * CT8 * CT5-
          + CT14- * CT13- * CT12- * CT11 * CT10- * CT9 * CT8-

LUT6    =   CT14- * CT13- * CT12- * CT10- * CT9- * CT8 * CT6- * CT5- * CT4-
                * CT3- * CT2- * CT1- * CT0-
          + CT14- * CT13- * CT12- * CT10- * CT9- * CT7 * CT6- * CT5- * CT4-
                * CT3- * CT2- * CT1- * CT0-
          + CT14- * CT13- * CT12- * CT10- * CT9 * CT8 * CT7 * CT6 * CT5
          + CT15- * CT14- * CT13- * CT12-

LUT5    =   CT15  * CT11 * CT9 * CT7- * CT3 * CT2 * CT1- * CT0-
          + CT14-  * CT13- * CT12- * CT10
          + CT15  * CT9 * CT8 + CT15 * CT12 + CT15 * CT13 + CT15 * CT14

LUT4    =   CT15- * CT13- * CT12- * CT10 * CT7- * CT6- * CT5- *CT4- * CT3- * CT2
                * CT1- * CT0-
          + CT15  * CT13- * CT12- * CT10- * CT9 * CT8 * CT7 * CT6 * CT5 * CT3
          + CT15- * CT13- * CT12- * CT10 * CT9 * CT7- * CT6- * CT5- * CT4-
                * CT3- * CT1- * CT0-
          + CT15  * CT13- * CT12- * CT11 * CT10- * CT9 * CT8- * CT7- * CT3-
                * CT2- * CT0-
          + CT15  * CT13- * CT12- * CT11 * CT10- * CT9 * CT8- * CT7- * CT3 * CT2
                * CT1- * CT0-
          + CT15- * CT13- * CT12- * CT10- * CT9- * CT8- * CT7- * CT6-
          + CT15- * CT13- * CT12- * CT10 * CT8 * CT7- * CT6- * CT5- * CT4-
                * CT3- * CT1- * CT0-
          + CT14

LUT3    =   CT15  * CT14- * CT12- * CT11 * CT10- * CT9 * CT7- * CT3- * CT2-
                * CT1 * CT0-
          + CT15  * CT14- * CT12- * CT10- * CT9 * CT8 * CT7-
          + CT15  * CT14- * CT12- * CT11 * CT10- * CT9 * CT8- * CT7
          + CT15- * CT14- * CT12- * CT10 * CT9- * CT8- * CT7- * CT6- * CT5-
                * CT4 * CT3- * CT2-
          + CT14- * CT12- * CT10- * CT9 * CT8 * CT6 * CT5 * CT2
          + CT15- * CT14- * CT12- * CT10- * CT5
          + CT15- * CT14- * CT12- * CT10 * CT7- * CT6- * CT5- * CT4- * CT3-
                * CT2 * CT1- * CT0-
          + CT13

LUT2    =   CT15  * CT14- * CT13- * CT10- * CT9 * CT8 * CT7 * CT5 * CT1
          + CT15- * CT14- * CT13- * CT10 * CT9- * CT8- * CT7- * CT6- * CT5-
                * CT3- * CT2- * CT1
          + CT15  * CT14- * CT13- * CT11 * CT10- * CT9 * CT8- * CT6
          + CT15  * CT14- * CT13- * CT11 * CT10- * CT9- * CT7 * CT6- * CT5-
                * CT4- * CT3- * CT2- * CT1- * CT0-
          + CT15  * CT14- * CT13- * CT11 * CT10- * CT8 * CT6- * CT5- * CT4-
                * CT3- * CT2- * CT1- * CT0-
          + CT15- * CT14- * CT13- * CT10- * CT3
          + CT15  * CT14- * CT13- * CT10- * CT9 * CT8 * CT6-
          + CT15- * CT14- * CT13- * CT10 * CT9 * CT7- * CT6- * CT5- * CT4-
                * CT3- * CT1- * CT0-
          + CT12
```

```
LUT1    =   CT15  * CT14- * CT13- * CT12- * CT10- * CT9 * CT8 * CT7 * CT6 * CT0
          + CT15  * CT14- * CT13- * CT12- * CT11- * CT8- * CT7- * CT6- * CT5
                  * CT4-
          + CT14- * CT13- * CT12- * CT10- * CT8 * CT6- * CT5- * CT4- * CT3-
                  * CT2- * CT1- * CT0-
          + CT15  * CT11 * CT10- * CT9 * CT8- * CT5
          + CT15- * CT14- * CT13- * CT12- * CT10 * CT8 * CT7- * CT6- * CT5-
                  * CT4- * CT3- * CT1- * CT0-
          + CT15 * CT14- * CT13- * CT12- * CT10- * CT9 * CT8 * CT5-
          + CT15 * CT14- * CT13- * CT12- * CT10 * CT8- * CT7- * CT6-
          + CT15- * CT14- * CT13- * CT12- * CT10- * CT4- * CT2- * CT1- * CT0-
          + CT14- * CT13- * CT12- * CT10 * CT9- * CT8- * CT7- * CT6- * CT5-
                  * CT3- * CT2- * CT0
          + CT15  * CT14- * CT13- * CT12- * CT11- * CT10- * CT8- * CT7- * CT6+
                  * CT5- * CT4-
          + CT12  * CT11 * CT13 * CT11  +  CT14 * CT11

LUT0    =   CT15  * CT14- * CT13- * CT12- * CT9- * CT7 * CT6- * CT5- * CT4-
                  * CT3- * CT2- * CT1- * CT0-
          + CT15  * CT14- * CT13- * CT12- * CT11 * CT10- * CT9 * CT4
          + CT15  * CT14- * CT13- * CT12- * CT10 * CT5- * CT4-
          + CT15  * CT14- * CT13- * CT12- * CT11- * CT8- * CT7- * CT6 * CT5-
                  * CT4-
          + CT15  * CT14- * CT13- * CT12- * CT11- * CT10- * CT8- * CT7- * CT6-
                  * CT5- * CT4
          + CT15  * CT14- * CT13- * CT12- * CT10- * CT9 * CT8 * CT4
```

Table 3-8. Control Store Jump Table Address Map

Macroinstruction	Control Store Location
Unimplemented Instruction Trap	100
ASL and ASR	101
LSL and LSR	102
RRL and RRR	103
Memory Reference Group	104 - 11F 124 - 13F
I/O Group	120 - 123
DIV,MPY,DLD,DST,JLA,JLB	141 - 14F
Extended Instruction Group	150 - 17F
1000 1010 XXXX XXXX (except FPS)	180 - 18F
Single Precision Floating Point	190 - 195
1000 X011 XXXX XXXX (except EIG)	1A0 - 1AF
Double Integer	1B0 - 1B9
Shift/Rotate Group	1C0 - 1DE
Alter/Skip Group	1E0 - 1FF

Control Store

The A400 supports addressing of 16k words of control store. Each word is 32 bits wide. The control store address latch is closed on the falling edge of PC-. The control store data must be valid at the inputs of the MIR register at the rising edge of PC-. The A400 detects accesses to nonexistent control store addresses. This is accomplished by using control store address bits 11 through 13 (CSAL[11:13]) on the

chip and the chip inputs UCSIZE+ (USIZE+ inside the chip) and OFFBDCSA+ (OFF_BRDCS+ inside the chip). UCSIZE+ indicates the size of the on-board control store as follows:

If UCSIZE+ = logic 1	then on-board control store = 2k words
If UCSIZE+ = logic 0	then on-board control store = 4k words

OFFBDCSA+ is asserted if an off-board control store recognizes the control store address and responds. Using these signals, an Unimplemented MicroInstruction (UMI) can be detected. A UMI causes a NOP to be forced on the microcode word in the MIR. It also zeros the control store address by selecting the zero input to the microsequencer multiplexer. The following equations show the implementation:

UMI- = (/OFF_BRDCS+ * ON_BRDCS-)'

where:

ON_BRDCS- = CSAL13 + CSAL12 + (CSAL11 * USIZE+)

Both A700 Control Store cards, the Writable Control Store (WCS) Card (HP 12153A) and the Prom Control Store (PCS) Card (HP 12155A) can be used to write microcode for the A400. Note that the capability is available and the description follows on how these boards are used, however, user-microprogramming on the A400 is *not* supported by Hewlett-Packard. They function in a fashion similar to the on-board control store.

The control store cards receive the Control Store Address (CSA[13:0]) generated in the processor chip and source the 32-bit wide Control Store Data word (CSD[31:0]) received by the processor chip. The WCS and PCS cards have a chained signal called OFF_BRDCS- which indicates that the logical address on the Control Store Address Bus corresponds to an address in the range of one of the Control Store Cards. The signal OFFBRDCS- when asserted by a control store card disables the on-board control store and all control store cards of lower priority. The card which asserted OFF_BRDCS- places the microcode word at the specified address onto the Control Store Data Bus.

The only difference seen by the processor chip is that the on-board control store is disabled and the exact timing of the data returned from the control store is different. The change in timing has no effect since the data is latched at the beginning of a cycle and the data from the control store cards is received in time.

ON_BDCS- is generated internal to the processor chip and indicates that the microaddress is in the on-board control store address space. If neither the OFF_BRDCS- signal nor the ON_BRDCS- signal are asserted, the signal UMI- is asserted. Upon assertion of UMI-, the microsequencer output is forced to zero and an Unimplemented Microinstruction Trap occurs.

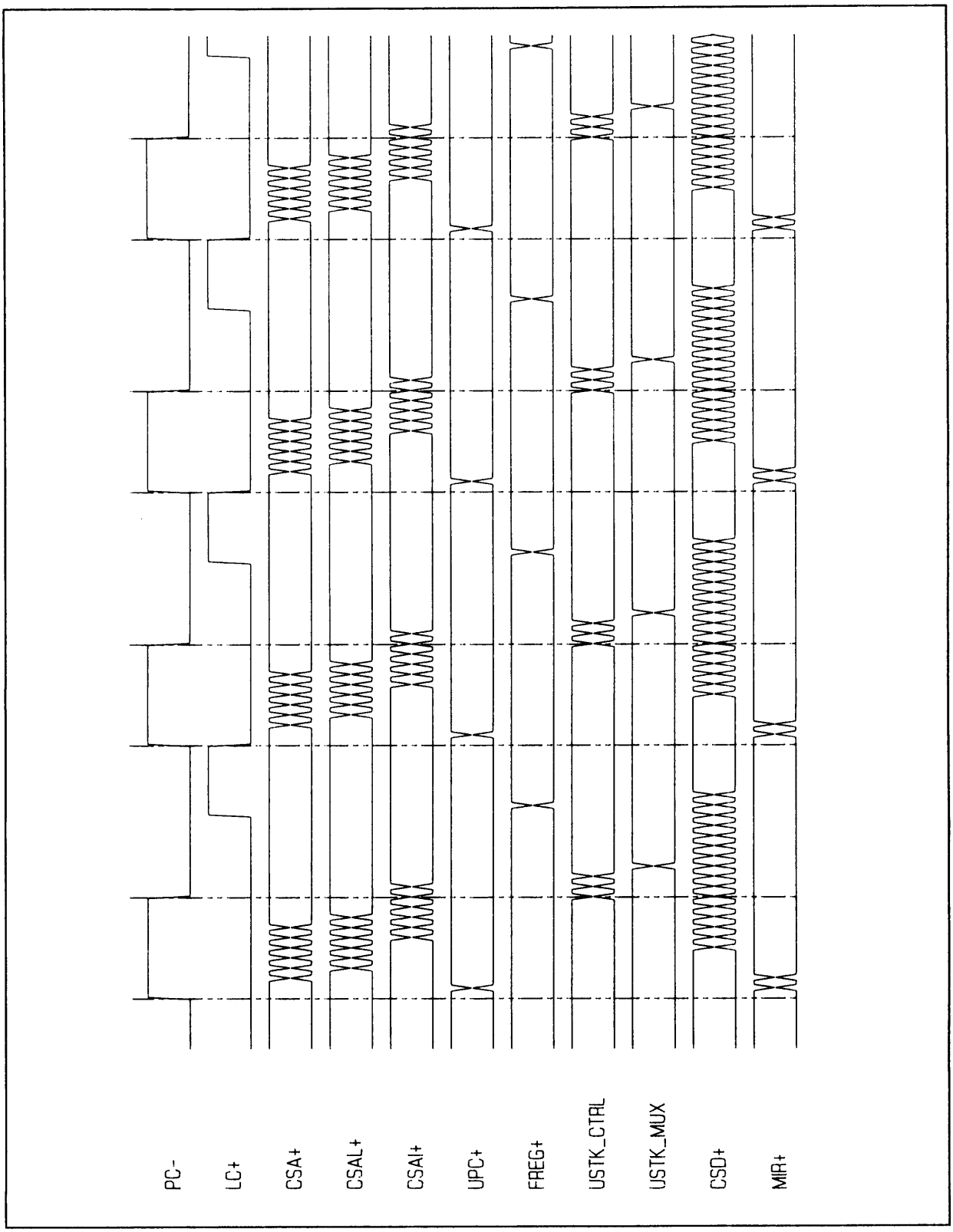


Figure 3-6. Microsequencer Timing Diagram

Condition Register

General Description

The condition register provides the processor conditions which are testable in the CNDX-field. Some of these conditions are used elsewhere in the processor.

The backplane PON+ (power-on) signal is received from the backlane and clocked on the board to obtain SPON+. It is then clocked twice in the processor chip to obtain BPON+. BPON+ is latched in the Condition Register to obtain the CNDX-field power-on (CPON). The backplane IORQ (I/O request) is latched from the backplane in the middle of the microcycle and then latched again at the end of the microcycle (CIORQ) to synchronize it.

To generate the O condition, which is also the macro-overflow (O) register, the condtion register must look at STO and CLO and ENOE from the SP0-field and the OVR output. The E condition, which is the macro-extend register, may be generated from CLE and STE in the SP0/SP1-fields and also from ENOE in the SP0-field and the COUT output. In the case of a shift function, E may be generated from LWE in the SP2-field, SHOUT (the bit shifted out) and SHEN (shift enable). The F condition or general-purpose flag is generated from STF and CLF in the SP2-field and JTAB in the OP-field. For a shift function, F may be generated from LWF in the SP2-field, SHOUT (the bit shifted out) and SHEN (shift enable). The condition SF or shift flag is generated from SHOUT (the bit shifted out) and SHEN (shift enable).

The double-word (DW) is used to indicate that shift functions will perform double word shifts. DW is generated from CMDW in the SP2-field and JTAB in the OP-field.

Theory of Operation

The condition register circuitry consists of condition capturing logic and condition selection logic. Table 3-9 defines the conditions available for the microcode to use for conditional jumps, branches, subroutine calls/returns, and stores.

The conditions CY15, CB15, YZ, ALOV, CF, and SF are clocked into the condition register at the end of all microcycles in which the ALU-field microorder is not ZERO. The FLAGN-1, CIORQ, CPON, CMP, CTZ4, and CTZ conditions are all clocked by PC-↑ regardless of the operation. The O and E conditions do not need to be stored in the condition register since their state is available at any time and does not need to be separately preserved. The INTF and INTP signals are generated by the interrupt control logic and do not need to be restored in the condition register. The condition register outputs are generated from the following inputs:

Condition Register Input		Condition Register Output
PIORQ	→	CIORQ
BPON	→	CPON
MP	→	CMP
PCTZ4	→	CTZ4
PCTZ	→	CTZ
PSF	→	SF
FLAGN	→	FLAGN-1
OVR	→	ALOV
COUT	→	CF
Z	→	CYZ
Y15	→	CY15
B15	→	CB15

The condition specified in the CNDX-field is selected by two 8-to-1 multiplexers. MIR14 (LSB) through MIR16 (MSB) are the multiplexer's select inputs while MIR17 is used to enable one or the other of the two multiplexers. The multiplexer outputs are ORed together and then selectively inverted (controlled by MIR28) to become the TEST+ signal.

TEST+ = (output of condition multiplexers) XOR MIR28

A feature included in the A400 micromachine that is not part of the A700 is the ability to read the condition register as a single 16-bit value. This is accomplished by reading SRIN register 4. The value returned has CIORQ+ as the LSB and INTF+ as the MSB.

Table 3-9. Microcode Condition Definitions

MIR Bit 7654	Condition Name	Condition Interpretation
0000	CIORQ	set if IORQ was set on the backplane on the previous cycle
0001	CPON	set if processor PON signal was set on the previous cycle
0010	CMP	set if memory protect was enabled on the previous cycle
0011	O	set if macro O-Register is set
0100	E	set if macro E-Register is set
0101	INTP	set if processor interrupt is pending
0110	CTZ4	set if lower 4 bits of the CT register are zero
0111	CTZ	set if CT register is zero
1000	SF	set if shift flag (SF) is set
1001	FLAGN-1	set if general purpose flag (F) is set
1010	ALOV	set if ALU overflow flag was set on previous cycle
1011	CF	set if carry output was set at the end of the previous cycle
1100	CYZ	set if the Y-bus is all zeros at the end of the previous cycle
1101	CY15	set if bit 15 of the Y-bus was set at the end of previous cycle
1110	CB15	set if bit 15 of the B-bus was set at the end of previous cycle
1111	INTF	set if interrupt FF is set (implies the last fetch was ignored)

The PON and IORQ Synchronizers

The two signals, BP_PON+ and IORQ–, are backplane signals that need to be synchronized to the micromachine.

The PON+ signal on the backplane is asynchronous to the processor. The A400 *board* clocks PON+ once on SC+ to create SPON+ which is input to the processor chip. In the processor chip, SPON+ is then synchronized to the micromachine and on-chip clocks. To accomplish this, SPON+ is clocked though a flip-flop (clocked on SC–↑) making preBPON+. Then, preBPON+ is clocked again on SC–↑ to generate BPON+. It is the synchronized signal, BPON+, that is input to the condition register. The output of the first stage of the synchronizer, preBPON+, is used to enable the processor chip input pads that are disabled when main +5 volt power is not present.

The timing of the IORQ– signal is such that it is valid about the falling edge of SCLK– (SC+↑). For this reason, the IORQ signal is clocked off of the backplane at SC+↑ so that it can be synchronized to the micromachine when it is clocked into the condition register.

Macro O- and E-Registers

The macro O- and E-Registers are each 1-bit registers. These registers can be selectively set and cleared, or set based on the results of an ALU or a shift operation. The two registers are implemented using JK flip-flops. When not specifically being set or cleared, these registers maintain their previous values.

The O-Register can be set or cleared by the microorder STO and CLO, respectively. If the ENOE microorder is issued, O will set if the ALU output OVR is asserted. The set (Jbar) and clear (K) equations for the O-Register are as follows:

SET_O = STO + (ENOE * OVR)

CLR_O = CLO-

The E-Register can be set or cleared by the STE or CLE microorders, respectively. The ENOE microorder causes E to set if the ALU output COUT is asserted. The LWE (link with E) microorder when used with a shift function (SHEN) will cause the E-Register to assume the state of the SHOUT signal. The set (J) and clear (K) equations for the E-Register are as follows:

SET_E = STE + (ENOE * CORBOR) + (LWE * SHEN * SHOUT)

CLR_E = CLE + (LWE * SHEN * SHOUT-)

where:

CORBOR (carry or borrow) = SUBOP XOR CYout

SUBOP = (-MIR10 + -MIR11) * -MIR12

The General Purpose Flag (F)

The general purpose flag, F, may be set or cleared, respectively, by STF or CLF. LWF, when used with a shift function (SHEN), will set or clear F according to SHOUT. JTAB will always clear F. If none of these microorders occurs, the state of F will not change. STF, CLF, and LWF are mutually exclusive. JTAB may occur with any of these, although under normal conditions it will not. No priority is defined here, but in hardware, if there are microorders for both setting and clearing, F will be set. The expressions for the general purpose flag are as follows:

FLAGN+ = (FLAG0)' + (FLAG1)' + STF

(FLAG0)' = FLAGN-1 * JTAB- * CLF- * (LWF * SHEN)

(FLAG1)' = LWF * SHEN * SHOUT

where:

FLAGN-1 = F set at the end of the previous cycle
FLAGN+ = F which will be latched at the end of the current cycle

The Shift Flag (SF)

The shift flag, SF, is set and cleared according to SHOUT when a shift function is executed (SHEN); otherwise, the state of SF is not changed. The shift flag expression is:

PSF = (SHEN+ * SHOUT+) + (SHEN- * SF)

where:

PSF = pre-shift flag to be latched at the end of the current cycle
SF = shift flag latched at the end of the previous cycle

The Double Word Flag (DW)

The double word bit, DW, is complemented by CMDW and cleared by JTAB. If both microorders occur together, then DW will be cleared. The equation is as follows:

PDW+ = (DW+ XOR CMDW-) NOR (JTAB+ OR BPON-)

where:

PDW+ = pre-double word flag to be latched at the end of the current cycle
DW+ = double word flag latched at the end of the previous cycle

The state of DW is not directly available to the microcode (though its state can be determined by doing a shift operation). The DW flag is cleared (logic 0) at power-up.

Counter

General Description

The counter register is a 16-bit parallel loadable decrementing counter. It functions as an instruction register in that it selects instructions on the backplane to pass on to the B-bus. Other sections of the counter logic are the counter multiplexer, the decrement counter logic, the zero detect logic, and the MRG execution logic.

In operation, the counter multiplexer selects either the Y-bus (Y[15:0]) or the Data bus (DI[15:0]) to pass to the counter data inputs. The multiplexer select signal is TCNT- which comes from the Memory Access logic. TCNT- indicates that the data on the Data bus is an instruction and is to be selected for loading into the counter. When TCNT- is deasserted, the data on the Y-bus is selected.

The Decrement Counter logic looks at various decoded microorders in order to generate a signal to decrement the counter. This involves the following conditions:

DCT microorder, CTZ or CTZ4 used in the CNDX-field with Word Type 2 or 3, and the processor clock FREEZE, that is, no decrement if the clock is frozen.

The Zero Detect logic looks ahead to determine if the lower four bits or all sixteen bits of the counter will be zeros on the next cycle (CTZ4 or CTZ).

When a JTAB OP is executed, the counter is used for MRG execution. This involves the initiation of one of three memory access microorders (RDB, FCHB, or CWRB) according to the instruction in the counter. A memory access is not initiated if the instruction is not an MRG instruction.

Theory of Operation

The Decrement Counter logic generates a signal, DECCT–, from a decoded microorder and FREEZE–. The counter is decremented on a non-frozen cycle by either the DCT, Decrement Counter, microorder appearing in the SP2-field of a Word Type 1 or 4 microinstruction or by a CTZ or CTZ4 microorder appearing in the CNDX-field of a Word Type 2 or 3 microinstruction. The logic equations are as follows:

```
DCT       = WT14 * MIR17- * MIR16- * MIR15 * MIR14-

WT14      = MIR30 * (MIR31  XOR  MIR29)

CTZ4_CTZ  = MIR31 * (MIR30- + MIR29) * MIR17 * MIR16 * MIR15

DECCT     = (DCT + CTZ4_CTZ) * FREEZE-
```

The counter consists of four 4-bit loadable down counters. Each counter has four data inputs, a count enable line, a ripple carry line, four tri-state outputs, four standard outputs, and a tri-state output enable. The tri-state outputs of the 16-bit Counter are tied to the B-bus. The tri-state output enable signal, ECTB–, is decoded from the B-field of the microinstruction. The signal ECTB– is asserted when the CT microorder is coded in the B-field of the microinstruction. The count enable line is DECCT– from the Decrement Counter logic for the lower four bits of the counter. The remaining 12 bits of the counter are enabled by the gating of this signal, DECCT–, with the ripple carry of the lower four bits.

The counter is clocked by the data clock, DC–. If the half-cycle of SCLK is extended due to an error correction on an instruction fetch (FCHB or FCHP), then the counter will be clocked again four FCLK cycles into the short half-cycle. This allows the counter to pick up the corrected data. Note that there is still a full cycle worth of time left in the cycle after the counter clocks in the corrected data. The counter then ends up being clocked every SCLK cycle, even when the processor is frozen. The control signals are held off on the frozen cycles so that even if the counter is clocked, the counter state will not change until the end of a non-frozen cycle. Data to be clocked into the counter from the DI-bus must be valid at the D+ pins 20.6 nanoseconds before the rising edge of a buffered DC–. Data to be clocked into the counter from the Y-bus must be valid 13.84 nanoseconds before the rising edge of a buffered DC–.

The counter is loaded during a non-frozen cycle by the signal LYCT- or on any cycle by the signal TCNT-. The signal LYCT- is generated from the decode of a CT microorder in the STOR-field of a microinstruction.

```
LYCT = MIR4 * MIR3 * MIR2- * MIR1 * MIR0 * STEN
```

The non-tristate outputs of the counter go to noninverting and inverting buffers and to the ALU address generation. The outputs of the buffers go to the look-up table, the MRG decode, and the Zero Detect logic.

The Zero Detect logic looks ahead to determine if the lower four bits or all sixteen bits of the counter will be zeros on the next cycle (CTZ4 or CTZ). To accomplish this the ripple carry outputs of the four counter slices are connected in a non-standard fashion. The ripple carry enable to the second stage (CT[7:4]) is tied low so that the ripple carry from the fourth slice, ZCTH-, indicates that CT[15:4] are all zeros. The ripple carry of the low-order slice is gated with the Decrement Counter signal, DECCT-, to enable the upper counter slices.

The signal PCTZ4 indicates that the low-order four bits of the counter (CT[3:0]) will be zero on the next cycle. This condition can occur in two cases: the lower four bits of the counter are zeros and the counter is not decremented on the next cycle (CT[3:0] = 0 and DECCT- is deasserted), or CT[3:0] = 0001b and the DECCT- signal is asserted (that is, the counter slice is to be decremented to zero from one on the next cycle). These two cases can be determined by predicting the state of CT0 for the next cycle. CT0 is exclusive ORed with DECCT- to determine NEXT_CTZ, the next CT0 state. This is then ORed with CT[3:1] to give PCTZ4. PCTZ4 is combined with the ripple carry output of the most significant nibble to give PCTZ which indicates that the counter will be zero on the next cycle. PCTZ and PCTZ4 are the unlatched versions of the CTZ and CTZ4 condition signals.

```
NEXT_CTZ = DECCT- XOR CT0

PCTZ4    = NEXT_CTZ * (CT1 + CT2 + CT3)'

PCTZ     = PCTZ4 * ZCTH
```

The conditions CTZ and CTZ4 will not be valid the cycle after a load of the counter. This occurs because it is possible to set up the conditions which assert CTZ or CTZ4 following a load and yet the counter will not actually be zero in the next cycle. The lookahead logic does not take into account that a load overrides the count function of the counter. For example, in cycle 1 the counter may be loaded and a CTZ microorder may be coded. If the data being loaded into the counter is a 0001 hex, the CTZ signal will be asserted and latched at the start of cycle 2. The counter however, will still be a 0001 hex in cycle 2 if a microorder to decrement the counter is not coded in this cycle.

Arithmetic and Logical Unit (ALU)

General Description

The ALU section of the A400 is primarily made up of the General Purpose Register File, the primary ALU, the secondary ALU, and the Q-Register and Q-Register shifter. The primary ALU is modeled after the ALU of the Advance Micro Devices 2903 bit-slice chip. Only required functions and capabilities of the 2903 ALU have been reproduced. In addition, the organization of the 2903 has been modified to enhance its performance in this application.

Figure 3-7 is a block diagram of the ALU. The ALU performs the following standard operations on 2 operands (R and S):

Arithmetic Operations	Logical Operations
S - R - 1 + Cin	$\overline{R}$ AND S
R - S - 1 + Cin	R XNOR S
R + S + Cin	R XOR S
S + Cin	R AND S
$\overline{S}$ + Cin	R NAND S
R + Cin	R OR S
$\overline{R}$ + Cin	R NOR S
output 1's	output 0's

In addition, the ALU supports some of the special functions implemented in the 2903. The special functions supported by the primary ALU are as follows:

- unsigned 16-bit multiply step
- two's complement 16-bit multiply intermediate step
- two's complement 16-bit multiply last step
- signed magnitude/two's complement conversion
- 16-bit normalize
- 32-bit normalize
- two's complement divide first step
- two's complement divide intermediate step

The organization of the primary ALU has a 2-to-1 multiplexer on the R operand input to the main ALU. The R operand is selected from either the General Purpose Register File (GPRF) or from the MIR immediate field. The S operand is always taken from the B-bus. The primary ALU is functionally separated into the primary arithmetic unit (AU) and the primary logic unit (LU). The output of both the primary AU and LU are multiplexed along with the secondary LU output and the GI-bus to form the F-bus. The F-bus then passes through a logical/arithmetic shifted to emerge as the Y-bus. The Y-bus is driven by super buffers for use throughout the processor chip.

The General Purpose Register File (GPRF) is a group of sixteen 16-bit registers that are directly addressable. The registers are dual-ported in that the A- and/or B-bus

may be selectively driven by any one or two GPRF registers at a time. The processor hardware forces the macro A- and B-Register (register numbers 0 and 1, respectively) to be in the GPRF. In addition, the macro X- and Y-Registers, the accumulator, and other scratch registers (both base set and user) are kept in this file.

The ALU also contains a single register (Q-Register) that is used for double width (32-bit) operations and for some of the special functions, that is, the Q-Register is used to hold the quotient in a divide cycle. This register can be loaded from the F-bus or from the previous value of the Q-Register via a 2-to-1 multiplexer. The Q-Register multiplexer is followed by a logical up/down 1-bit shifter. The output of the shifter is what is actually loaded into the Q-Register.

There are eight functions, not performed in the primary ALU of the processor. These are microcoded by SPEC in the ALU field and microorders SWAP, SWZU, SWZL, ZUY, ZLY, ASG, SRG, or RL4 in the ALUS field. When these functions are microcoded, the secondary ALU on the processor drives the Y-bus rather than the primary ALU.

The primary ALU generates 4 status flags that are used for various things throughout the micromachine. These flags are as follows:

Flag	General Indication
Z	Y-bus is all zeros
N	Y-bus bit 15 value
OVR	ALU overflow
CYout	ALU high-order carry out

In the case of some of the special functions, the meaning of these flags are changed to provide relevant information about the progress of the particular operation. This will be covered in later sections.

The primary ALU receives various control lines from the micromachine to determine and control its operation. The MIR ALU-field and ALUS-field identify the operation to perform. The four instruction lines (I5 through I8) are used to identify the shift operation(s) and destination of each operation. Additionally, the ALU requires a carry-in signal (Cin) for its arithmetic operations. The 2 shifters (Y-bus and Q-bus shifters) each have two shift in/out lines: SIO15, SIO0, QIO15, and QIO0. The other major control lines needed are: multiplexer select inputs (R_sel, S_sel, Q_S1–, and Q_S0–), tri-state buffer enables (OEB), and the Q-Register clock (PC–).

The sections that follow cover the construction and operation of each of the blocks. The control equations and the micromachine interface are given.

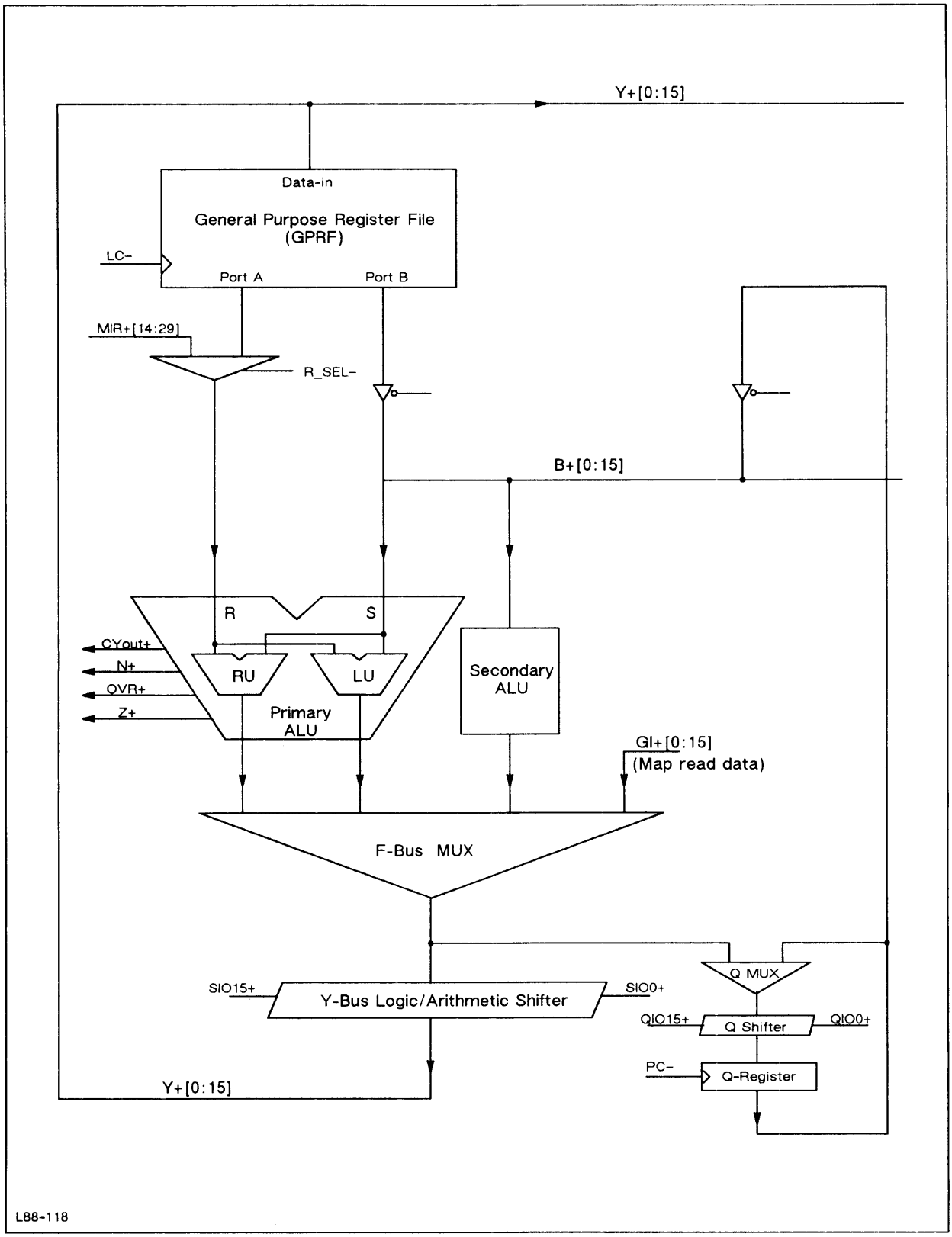


Figure 3-7. A400 ALU Block Diagram

Theory of Operation

Primary ALU R-Operand Selection

The R-operand multiplexer selects between the MIR immediate field (MIR14:31) and the GPRF. The multiplexer selects the MIR immediate data for word type 6 instructions only. The equation is as follows:

R_SEL- = MIR30 + MIR31

Primary ALU Logic

The primary ALU is divided into two parts: the Arithmetic Unit (AU) and the Logical Unit (LU). The actual ALU result is selected by a 4-to-1 multiplexer to be driven onto the F-bus. Figure 3-8 is a block diagram of the primary ALU.

The Arithmetic Unit (AU):

The Arithmetic Unit (AU) is broken down into two parts. The first part is labeled Operand Preparation. This block of logic is responsible for supplying the adder section of the AU with either the true or complement version of each operand as well as zeroing one or the other operand occasionally. Table 3-10 shows the required state of each operand depending on the operation to be performed (indicated by MIR10-12 and MIR18-22). Since the AU preparation stage is entered very early in a microcycle, the logic decodes the state of the MIR bits directly rather than first generating the 2903 instruction bits I0 – I8 and then determining what the operation calls for. This allows the logic to decide what needs to be done to the incoming data before the data actually arrives.

It should be noted that there are a few unimplemented capabilities that were present in the 2903 but are not needed in the A400 processor chip. The values of the instruction codes I5 – I8 for the 2903 unimplemented special functions are: 1H, 3H, 4H, 7H, 9H, BH, DH, EH, FH.

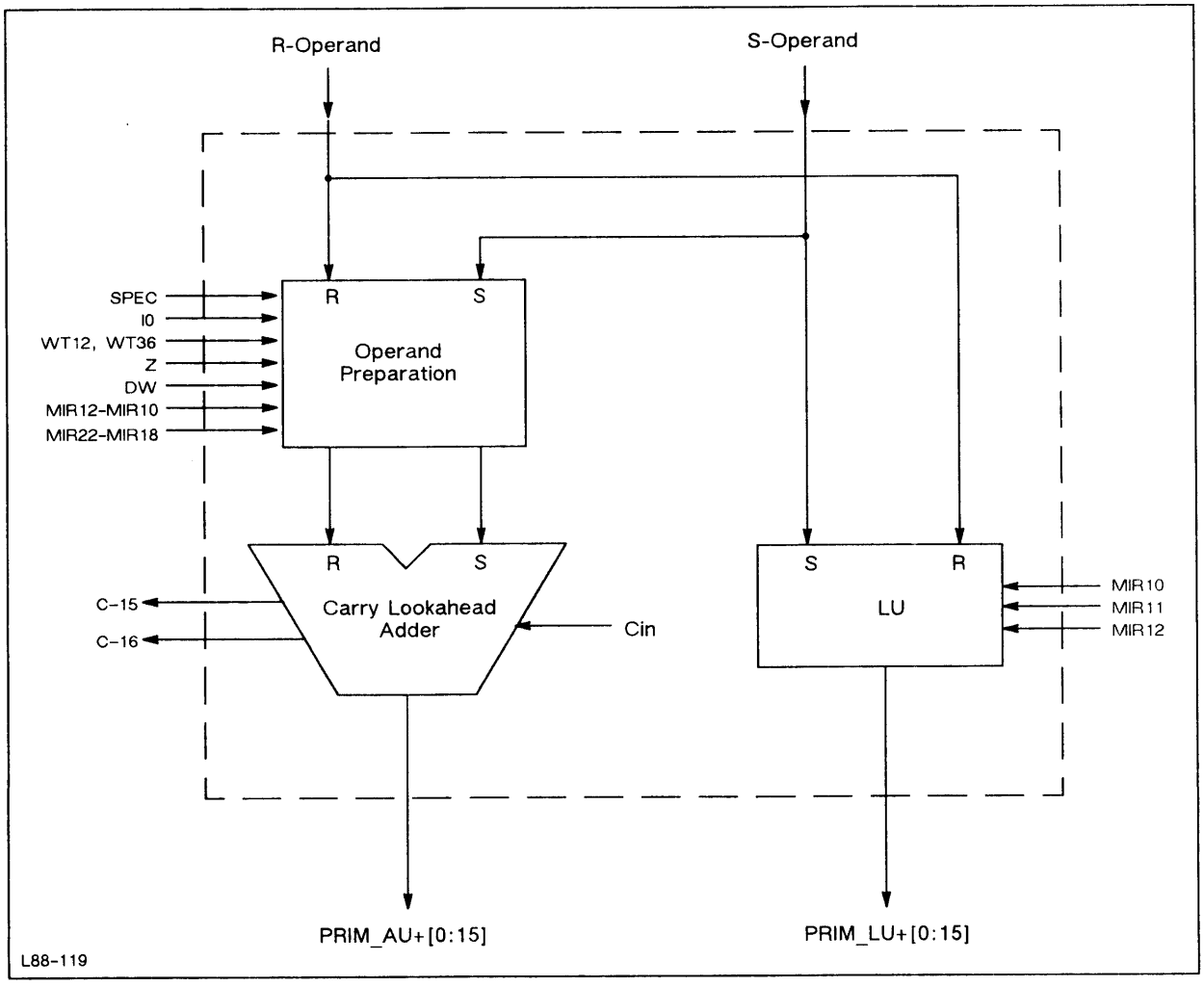


Figure 3-8. Primary ALU Block Diagram

Table 3-10. Arithmetic Unit Operand Preparation

SPCLF+	MIR Bit 22	21	20	19	18	12	11	10	I0	Z	ALU Function	Ri	Si	Comment
0	X	X	X	X	X	L	L	L	H	X	all 1's +Cin	0	1	CT modified jumps
0	X	X	X	X	X	L	L	H	X	X	S+$\overline{R}$+Cin	-(Rin)	Sin	normal ALU ops
0	X	X	X	X	X	L	H	L	X	X	R+$\overline{S}$+Cin	Rin	-(Sin)	"
0	X	X	X	X	X	L	H	H	X	X	R+S+Cin	Rin	Sin	"
0	X	X	X	X	X	H	L	L	X	X	S+Cin	0	Sin	"
0	X	X	X	X	X	H	L	H	X	X	$\overline{S}$+Cin	0	-(Sin)	"
0	X	X	X	X	X	H	H	L	X	X	R+Cin	Rin	0	"
0	X	X	X	X	X	H	H	H	X	X	$\overline{R}$+Cin	-(Rin)	0	"
1	L	L	L	L	L	L	L	L	L	0	S+Cin	0	Sin	unsigned multiply
1	L	L	L	L	L	L	L	L	L	1	R+S+Cin	Rin	Sin	
1	L	L	L	L	H	L	L	L	L	0	S+Cin	0	Sin	two's complement multiply
1	L	L	L	L	H	L	L	L	L	1	R+S+Cin	Rin	Sin	
1	L	L	L	H	L	L	L	L	L	0	S+Cin	0	Sin	sign magn./two's compl. conv.
1	L	L	L	H	L	L	L	L	L	1	$\overline{S}$+Cin	0	-(Sin)	
1	L	L	L	H	H	L	L	L	L	0	S+Cin	0	Sin	two's complement multiply
1	L	L	L	H	H	L	L	L	L	1	S+$\overline{R}$+Cin	-(Rin)	Sin	last cycle
1	L	L	H	L	L	L	L	L	L	X	S+Cin	0	Sin	32-bit normalize
1	L	L	H	L	H	L	L	L	L	X	S+Cin	0	Sin	16-bit normalize
1	L	L	H	H	L	L	L	L	L	0	R+S+Cin	Rin	Sin	two's complement divide
	L	L	H	H	L	L	L	L	L	1	S+$\overline{R}$+Cin	-(Rin)	Sin	
1	L	L	H	H	H	L	L	L	L	X	S+Cin	0	Sin	first divide cycle

where:
- Rin = operand preparation logic R-side input bit i
- Sin = operand preparation logic S-side input bit i
- Ri = operand preparation logic R-side output bit i
- Si = operand preparation logic S-side output bit i
- Z,Cin = ALU inputs
- -(xx) = one's complement of xx
- I0 = instruction bit 0 [ENQB + JMPCT30 + SCNDLUOP]
  - where JMPCT30 = WT56_OP * SPEC and SCNDLUOP = MIR21 * SPEC * -WT56_OP
- SPCLF = special ALU function [-MIR13 * -MIR12 * -MIR11 * -MIR10 * -I0]
- WT56_OP = word type 5 or 6 [MIR31 + (MIR30 * MIR29)]

The equations used for the operand preparation logic are given below. Note that these are minimized functions and might not appear to directly correspond to Table 3-10.

```
Ri   =  Rin * -MIR12 * MIR11 * -MIR10
        +  Rin * MIR12 * MIR11 * -MIR10
        +  Rin * -MIR12 * MIR11 * MIR10
        +  Rin * -Z * -MIR21 * MIR20 * MIR19 * -MIR18 * SPCLF * -WT56_OP
        +  Rin * Z * -MIR21 * -MIR20 * -MIR19 * SPCLF * -WT56_OP
        +  -Rin * -MIR12 * -MIR11 * MIR10
        +  -Rin * MIR12 * MIR11 * MIR10
        +  -Rin * Z * -MIR21 * MIR20 * MIR19 * -MIR18 * SPCLF * -WT56_OP
        +  -Rin * Z * -MIR21 * -MIR20 * MIR19 * MIR18 * SPCLF * -WT56_OP

Si   =  Sin * -MIR12 * MIR10
        +  Sin * MIR12 * -MIR11 * -MIR10
        +  Sin * -Z * -MIR21 * SPCLF * -WT56_OP
        +  Sin * -MIR21 * MIR18 * SPCLF * -WT56_OP
        +  Sin * -MIR21 * MIR20 * SPCLF * -WT56_OP
        +  Sin * -MIR21 * -MIR19 * SPCLF * -WT56_OP
        +  -Sin * MIR12 * -MIR11 * MIR10
        +  -Sin * -MIR12 * MIR11 * -MIR10
        +  -Sin * Z * -MIR21 * -MIR20 * MIR19 * -MIR18 * SPCLF * -WT56_OP
        +  -MIR12 * -MIR11 * MIR10 * I0
```

where:

```
Rin  =  operand preparation logic R-side input bit i
Ri   =  operand preparation logic R-side output bit i
Sin  =  operand preparation logic S-side input bit i
Si   =  operand preparation logic S-side output bit i
I0   =  instruction bit 0 [ENQB + JMPCT30 + SCNDLUOP]
```

where:

```
JMPCT30    = WT56_OP * SPEC   and
SCNDLUOP   = MIR21 * SPEC * -WT56_OP
WT56_OP    =  word type 5 or 6 [MIR31 + (MIR30 * MIR29)]
SPCLF      =  special ALU function  [-MIR13 * -MIR12 * -MIR11 * -MIR10 * -I0]
Z          =  ALU input
```

The second part of the AU is a standard carry lookahead 16-bit adder. The adder is implemented in 4-bit slices with a separate carry lookahead generator. The adder accepts a carry-in (Cin) and generates a carry out (C16). The carry into bit position 15 (C15) is also output for use in determining AU overflow conditions.

The Logical Unit (LU):

The other half of the primary ALU is the primary logical unit. This block of logic performs the 8 logical funtions required by the processor. The equations for this logic are:

```
LUi =  (MIR12 @ MIR11) * -MIR10 * (Rin * Sin)
     + MIR12 * MIR11 * MIR10 * (Sin)
     + MIR12 * MIR11 * -MIR10 * (-Rin + -Sin)
     + [(MIR12 * -MIR11 * MIR10) + (MIR11 * -MIR10)] * (-Rin * -Sin)
     + -MIR12 * MIR10 * (-Rin * Sin)
     + MIR11 * MIR10 * (Rin * -Sin)
```

where:

LUi	=	Logical unit output bit i
@	=	Exclusive OR
Rin	=	Logical unit R-side input bit i
Sin	=	Logical unit S-side input bit i
-xx	=	One's complement of xx

The F-Bus Multiplexer:

The F-bus multiplexer is responsible for passing the appropriate source of data onto the F-bus. The default case is to pass either the primary AU result bus (AU+[0:15]) or the primary LU result bus (PRIM_LU+[0:15]). If the current access is a map read (MAP in the BBUS-field) then the GIO input bus (GI+[0:15]) is selected. If the operation calls for the secondary LU then its result bus (SCND_LU+[0:15]) is passed onto the F-bus.

F-Bus Multiplexer

		Passed Bus			
F_S1-	F_S0-	PRIM AU	PRIM LU	SCND LU	GI BUS
0	0				X
0	1			X	
1	0		X		
1	1	X			

The F-bus multiplexer equations for the select lines F_S1- and F_S0- are as follows:

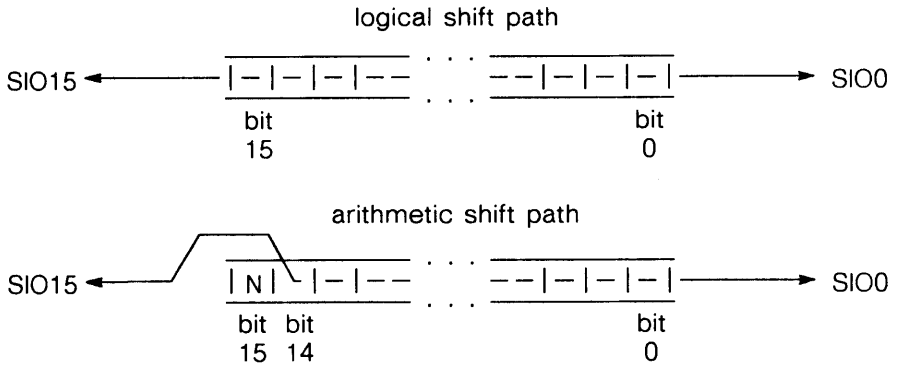
```
F_S1-  =  -(EMAPB + (MIR21 * SPEC * -WT56_OP))

F_S0-  =  -(EMAPB + MIR13)
```

where:

```
SPEC     = special in ALU field  [-MIR13 * -MIR12 * -MIR11 * -MIR10]
WT56_OP  = word type 5 or 6  [MIR31 + (MIR30 * MIR29)]
```

The Y-Bus Shifter:

The Y-bus shifter is located between the F-bus and the Y-bus. It is a one-bit left/right combinatorial shifter that performs both logical and arithmetic shifts. The shifting requirements for the Y-bus shifter are detailed in Table 3-11.



The actual multiplexers that make up the shifter consist of 15 4-to-1 multiplexers for F-bus bits 0 through 14. Bit 15 requires an 8-to-1 multiplexer. The select lines of the multiplexer are driven by the Y-bus and Q-bus shifter control logic.

For the Y-bus shifter, three separate sets of control lines are required. Bits 0 through 13 are controlled by Y_S1–/Y_S0–, bit 14 is controlled by Y14_S1+/Y14_S0+, and bit 15 is controlled by Y15_S2+/Y15_S1+/Y15_S0+. Bits 14 and 15 are treated differently than the lower order bits because of the need to shift around special functions. The third piece of logic involved in the Y-bus shifter is the shift in/shift out bit generation block. This circuitry determines the state of the shift inputs and outputs for the Y-bus shifter (SIO0+ and SIO15+) and the processor condition logic.

The Y-bus shifter control logic is responsible for selecting the appropriate source of data to pass onto the Y-bus. Table 3-12 shows the state of the select lines and the data selected.

The shifter control signals are generated by decoding the ALU instruction bits I5 through I8. The equations for generating the shifter control signals are as follows:

```
Y_S1-   = -(-SPCLF * -I8 * -I7  +  -I8 * -I7 * -I5  +  SPCLF * -I8 * I6 * -I5)

Y_S0    = -(-SPCLF * I8 * -I7 + I8 * -I7 * I6 * -I5  + SPCLF * I8 * I7 * -I6 * -I5)

Y14_S1+ = -SPCLF * (-I7 * -I5 + I8 * -I7 * I5) + SPCLF * (I8 * -I7 * I6 * -I5)
          + I8 * I7 * -I6 * -I5)

Y14_S0+ = -SPCLF * -I8 * -I7 * I5 + SPCLF * -I8 * I7 * -I6 * I5 + -I8 * -I7 * -I5

Y15_S2+ = -SPCLF * -I8 * -I7 * I5 + SPCLF * (-I8 * I7 * -I6 * I5
          +  -I8 * -I7 * -I6 * -I5)

Y15_S1+ = SPCLF * (-I8 * I6 * -I5 + -I8 * -I7 * -I6 * -I5)

Y15_S0+ = -SPCLF * I8 * -I7 * I5 + SPCLF (I8 * -I7 * I6 * -I5 + I8 * I7 * -I6 * -I5
          +  -I8 * I7 * -I6 * I5)
```

The generation of the shift lines SIO0 and SIO15 is handled by special logic. In a true 2903 implementation, these lines are bidirectional and require external shift linkage logic (like in the A700) to handle them appropriately. In the A400 implementation, there is no need for the signals to be bidirectional nor to have more than one set of logic to handle both bit generation and shift linkage. The actual generation of SIO0/SIO15 will be covered in detail in a later section.

The output of the Y-bus shifter (Y2B+[0:15]) is driven by super buffers onto the processor chip Y-bus. Note that all possible sources of Y-bus data (the primary AU, the primary LU, the secondary LU, and the GI-bus) are multiplexed onto the F-bus. Since the F-bus sources the input data of the Y-bus shifter, there is no reason to make the Y-bus a tri-state bus as on the A700.

Table 3-11. Y-Bus Shifter Functions

I8	I7	I6	I5	SPCLF	Y-Bus Shifter	SIO15	SIO0	Q-Reg & Shifter Function	QIO15	QIO0	Notes
L	L	L	L	0	arith F/2 → Y	input	F0	hold	input	Q0	
L	L	L	H	0	log F/2 → Y	input	F0	hold	input	Q0	
L	L	H	L	0	arith F/2 → Y	input	F0	log Q/2 → Q	input	Q0	
L	L	H	H	0	log F/2 → Y	input	F0	log Q/2 → Q	input	Q0	
L	H	L	L	0	F → Y	input	F0	hold	input	Q0	
L	H	L	H	0	F → Y	input	F0	log Q/2 → Q	input	Q0	
L	H	H	L	0	F → Y	input	F0	F → Q	input	Q0	
L	H	H	H	0	F → Y	input	F0	F → Q	input	Q0	
H	L	L	L	0	arith 2F → Y	F14	input	hold	Q14	input	
H	L	L	H	0	log 2F → Y	F15	input	hold	Q15	input	
H	L	H	L	0	arith 2F → Y	F14	input	log 2Q → Q	Q14	input	
H	L	H	H	0	log 2F → Y	F15	input	log 2Q → Q	Q15	input	
H	H	L	L	0	F → Y	0	input	hold	Q15	input	
H	H	L	H	0	F → Y	0	input	log 2Q → Q	Q15	input	
H	H	H	L	0	not used	--	--	--	--	--	
H	H	H	H	0	F → Y	0	input	hold	Q15	input	
L	L	L	L	1	log F/2 → Y	input	F0	log Q/2 → Q	input	Q0	Note 1
L	L	H	L	1	log F/2 → Y	input	F0	log Q/2 → Q	input	Q0	Note 2
L	H	L	H	1	F → Y	input	F0	hold	input	Q0	Note 3
L	H	H	L	1	log F/2 → Y	input	F0	log Q/2 → Q	input	Q0	Note 2
H	L	L	L	1	F → Y	F15	input	log 2Q → Q	Q15	input	
H	L	H	L	1	log F/2 → Y	R15 @ F15	input	log 2Q → Q	Q15	input	
H	H	L	L	1	log F/2 → Y	R15 % F15	input	log 2Q → Q	Q15	input	

where: SPCLF = special ALU function [-MIR13 * -MIR12 * -MIR11 * -MIR10 * -I0]
@ = exclusive OR
% = exclusive NOR

Note 1: C16 is gated to Y15

Note 2: (F15 @ OVR) is gated to Y15

Note 3: (F15 @ B15) is gated to Y15

Table 3-12. Y-Bus Shifter Control

Y Y . . S S 1 0 – –	Data	Y Y 1 1 4 4 . . 1 0 + +	Data	Y Y Y 1 1 1 5 5 5 . . . 2 1 0 + + +	Data
0 0	F[xx] (pass)	0 0	SIO15 (arith F/2)	0 0 0	C16 (SF 0)
0 1	F[xx–1] (F*2)	0 1	F[13] (F*2)	0 0 1	C16 (SF 0)
1 0	F[xx+1] (F/2)	1 0	F[15] (F/2)	0 1 0	F[15] @ B[15] (SF 5)
1 1	F[xx] (pass)	1 1	F[14] (pass)	0 1 1	SIO15 (F/2)
				1 0 0	F[15] @ OVR (SF 2&6)
				1 0 1	F[15] @ OVR (SF 2&6)
				1 1 0	F[14] (F*2)
				1 1 1	F[15] (pass)

where: F*2 = left shift
F/2 = right shift
arith F/2 = right shift around the sign bit (F[15])
pass = Y[xx] = F[xx]
SF X = AMD2903 special function X

General Purpose Register File (GPRF)

The implementation of the GPRF is based on a dual-ported 16-by-16 register file. The input for each D flip-flop in the file is from the appropriate Y-bus bit. All registers are clocked on the rising edge of PC– when enabled. Individual register enables are generated from the store field (MIR 0 through 4) of a microinstruction. The outputs of the register file are enabled onto the appropriate bus (or buses) depending on the microorders in the ABUS- and BBUS-fields.

The GPRF requires three sets of control inputs: A-bus enables 0 through 3, B-bus enables 0 through 3, and Clock enables 0 through 3. The A- and B-bus enables are each inputs to two 3-to-8 decoders which selectively enable a register(s) onto one or both buses. The clock enables are also decoded by two 3-to-8 decoders and are used to enable a specific register to be clocked. Table 3-13 lists the registers that reside in the GPRF.

The decoding logic for the GPRF bus and clock enables is covered in the MIR decoding sections for the ABUS-field, the BBUS-field, and the STOR-field.

Table 3-13. Individual Registers in the GPRF

Location	Register Mnemonic	Register Number
0000	A	R0
0001	B	R1
0010	X	R2
0011	Y	R3
0100	ACC	R4
0101	HP1	R5
0110	HP2	R6
0111	USR	R7
1000	S0	R10
1001	S1	R11
1010	S2	R12
1011	S3	R13
1100	S4	R14
1101	S5	R15
1110	S6	R16
1111	S7	R17

The Q-Register and the Q-Register Shifter

The Q-Register is an auxiliary 16-bit register whose primary use is in multiplication and division operations. It is also used for double word (32-bit) operations and for normalizations. The Q-Register is always clocked on the rising edge of PC–. The value that is clocked into the Q-Register is determined by the output of the Q-shifter (preQ+[0:15]). Note that for any bit position i, the bit loaded into the Q-Register is either Qi, Qi–1, Qi+1, or Fi. This observation has led to the implementation of the Q-shifter as simply a 4-to-1 multiplexer. The select line equations are as follows:

$$Q\_S1- = -SPCLF * (-I8 * I7 * I5 + -I8 * I6) + SPCLF * -I8 * -I7 * -I5 + -I8 * I6 * -I5$$

$$Q\_S0- = -SPCLF * (-I8 * I7 * I6 + I8 * -I7 * I6 + I8 * I7 * -I6 * I5) + SPCLF * (I8 * -I7 * - I5 + I8 * -I6 * -I5)$$

where:

Function	Q_S1–	Q_S0–	Action
Q → Q	0	0	Q[xx] → preQ[xx]
2Q → Q	0	1	Q[xx] → preQ[xx+1]
Q/2 → Q	1	1	Q[xx] → preQ[xx–1]
F → Q	1	1	F[xx] → preQ[xx]

The Q-Register can be enabled onto the B-bus whenever eNQb– asserts.

ALU Status Flags

The primary ALU provides the processor chip micromachine with four status signals. These signals have different meanings depending on the operation being performed. Table 3-14 gives the meanings of the status flags for each supported operation.

Table 3-14. ALU Status Outputs

				MIR Bit							
I8	I7	I6	I5	13	12	11	10	I0	OVR	N	Z	CYout
X	X	X	X	0	0	0	0	1	0	F15	ZEROY	0
X	X	X	X	0	0	0	1	X	C16 @ C15	F15	ZEROY	C16
X	X	X	X	0	0	1	0	X	C16 @ C15	F15	ZEROY	C16
X	X	X	X	0	0	1	1	X	C16 @ C15	F15	ZEROY	C16
X	X	X	X	0	1	0	0	X	C16 @ C15	F15	ZEROY	C16
X	X	X	X	0	1	0	1	X	C16 @ C15	F15	ZEROY	C16
X	X	X	X	0	1	1	0	X	C16 @ C15	F15	ZEROY	C16
X	X	X	X	0	1	1	1	X	C16 @ C15	F15	ZEROY	C16
X	X	X	X	1	0	0	0	X	0	F15	ZEROY	0
X	X	X	X	1	0	0	1	X	0	F15	ZEROY	0
X	X	X	X	1	0	1	0	X	0	F15	ZEROY	0
X	X	X	X	1	0	1	1	X	0	F15	ZEROY	0
X	X	X	X	1	1	0	0	X	0	F15	ZEROY	0
X	X	X	X	1	1	0	1	X	0	F15	ZEROY	0
X	X	X	X	1	1	1	0	X	0	F15	ZEROY	0
X	X	X	X	1	1	1	1	X	0	F15	ZEROY	0
0	0	0	0	0	0	0	0	0	C16 @ C15	F15	Q0	C16
0	0	1	0	0	0	0	0	0		F15	Q0	C16
0	1	0	1	0	0	0	0	0	C16 @ C15	F15 if Z=0 or F15 @ S15 if Z=1	S15	C16
0	1	1	0	0	0	0	0	0	C16 @ C15	F15	Q0	C16
1	0	0	0	0	0	0	0	0	Q14 @ Q13	Q15	ZEROQ	Q15 @ Q14
1	0	1	0	0	0	0	0	0	F14 @ F13	F15	ZEROQ * ZEROY	F15 @ F14
1	1	0	0	0	0	0	0	0	C16 @ C15	F15	SCFF	C16

where:
ZEROY = Y15 + Y14 + Y13 + . . . + Y1 + Y0)' , that is, Y-bus is all zeros
ZEROQ = Q15 + Q14 + Q13 + . . . + Q1 + Q0)' , that is, Q-Register is all zeros
@ = Exclusive OR
SCFF = Sign compare flip-flop output. This D flip-flop is clocked on the rising edge of PC-. It maintains its previous state for all operations except special functions A and C. At the conclusion (PC- ↑) of a special function A or C cycle, the state of (R15 XNOR AU15) is clocked into the SCFF flip-flop.

Table 3-14 can be summed up by the following equations which are used for generating the four status flags. In the equations below, signal substitutions have been made to take advantage of the processor's access to the entire micromachine. This increases the speed of some paths and reduces loading on others. The same function as indicated above has been preserved.

```
Z+      = ZERO_Y * -SPCLF + Q0 * (-I8 * -I5 * SPCLF) + B15 * (I7 * I5 * SPCLF)
          + ZERO_Q * (I8 * -I7 * -I6 * SPCLF) + SCFF * (I8 * I7 * SPCLF)
          + ZERO_Q * ZERO_AU * (I8 * I6 * SPCLF)

OVR+    = (C16 @ C15) * (ORI123 * -MIR13) + (C16 @ C15) * (-I8 * SPCLF)
          + (C16 @ C15) * (I7 * SPCLF) + (Q14 @ Q13) * (I8 * -I7 * -I6 * SPCLF)
          + (AU15 @ AU14) * (I8 * I6 * SPCLF)

CYout+  = (C16) * (-MIR13 * ORI123 * -SPCLF) + (C16) * (-I8 * SPCLF)
          + (C16) * (I8 * I7 * SPCLF) + (Q15 @ Q14) * (I8 * -I6 * SPCLF)
          + (AU15 @ AU14) * (I8 * I6 * SPCLF)

N+      = F15 * (-SPCLF) + F15 * (SPCLF * I5)
          + F15 * (SPCLF * (-I8 * (-I7 + -I5)))
          + F15 * (SPCLF * (I8 * (I7 + I6))) + F15 * (SPCLF * I7 * I5 * -B15)
          + Q15 * (SPCLF * I8 * -I7 * -I6)
```

where:

```
ORI123  = MIR12 + MIR11 + MIR10
SPCLF   = -MIR13 * -MIR12 * -MIR11 * -MIR10 * -I0
ZERO_Y  = (Y2B15 + Y2B14 + . . . + Y2B1 + Y2B0)'
ZERO_Q  = (Q15 + Q14 + . . . + Q1 + Q0)
ZERO_AU = (AU15 + AU14 + . . . + AU1 + AU0)
```

SCFF = Sign compare flip-flop output. This D flip-flop is clocked on the rising edge of PC−. It maintains its previous state for all operations except special functions A and C. At the conclusion (PC− ↑) of a special function A or C cycle, the state of (R15 XNOR AU15) is clocked into the SCFF flip-flop.

Carry-In Generation

The value of the ALU carry-in signal (CIN) is generated from a number of different sources depending on the particular microinstruction. CIN is required for all arithmetic (non-logical) operations. For the primary ALU logic functions and the secondary LU operations, the CIN signal represents a "don't care" situation. The value of CIN is based on the operation currently being performed. ACF and FCIN are microorders used to govern the carry-in generation. Table 3-15 defines the generation of the CIN signal.

The equation for the CIN signal is as follows:

```
CIN = (SUBOP XOR FCIN ) * -SPEC * -ACF + ACF * CF
        + MIR20 * -MIR19 * MIR18 * SPCLF
        + Z * SPEC * -MIR20 * MIR19
        + Z * SPEC * MIR19 * -MIR18
```

Table 3-15. Carry-In Generation Definition

ALU-Field	CIN		
	NO ACF NO FCIN	FCIN	ACF
ONES	0	0	-
SBAC	1	0	CF
SBBC	1	0	CF
ADDC	0	1	CF
ADBC	0	1	CF
CMBC	0	1	CF
ADAC	0	1	CF
CMAC	0	1	CF
Sec. LU specials			
UMPY	0	0	-
TMPY	0	0	-
SM2C	Z	Z	-
TMLC	Z	Z	-
DNRM	0	0	-
SNRM	1	1	-
DIV	Z	Z	-
DIV1	0	0	-

where: Z is the ALU Z status flag value during the current cycle.

Instruction Bits I5–I8 Generation

The ALU instruction bits I5 through I8 are generated from MIR18 through MIR22, plus information about the current microword type. Table 3-16 and the following equaitons detail the I5 through I8 generation.

```
I5+ = MIR21 + SPEC * WT56 + MIR22 * -SPEC * WT12 + -WT12 * WT56
      + -MIR20 * -SPEC + -MIR19 * -SPEC + -MIR20 * MIR19 * -MIR18

I6+ = MIR21 + -MIR20 * MIR18 * SPEC + DW * -SPEC
      + MIR20 * -MIR19 * -MIR18 * SPEC + MIR19 * MIR18 * SPEC
      + -MIR20 * -MIR19 * -SPEC + SPEC * WT56 +
      + MIR22 * -SPEC * WT12 + -WT12 * WT56

I7+ = MIR21 + MIR20 * MIR19 * -MIR18 * SPEC + -MIR20 * -MIR19 * -SPEC
      + -MIR20 * MIR19 * SPEC + MIR22 * -SPEC * WT12 + SPEC * WT56
      + -WT12 * WT56

I8+ = MIR21 + MIR19 * MIR18 * -SPEC + MIR20 * MIR18
      + -MIR20 * -MIR19 * -MIR18 * SPEC + MIR20 * SPEC
      + MIR22 * -SPEC * WT12 + SPEC * WT56 + -WT12 * WT56
```

Table 3-16. Instruction Bits I5 through I8 Generation Logic

Inputs						Outputs			
Function	WT12+	WT56–	MIR bits 22 thru 18	DW+	SPEC+	I8	I7	I6	I5
NOP	1	–	00000	–	0	1	1	1	1
	0	1	–0000	–	0	1	1	1	1
LDQ	1	–	00001	–	0	0	1	1	1
	0	1	–0001	–	0	0	1	1	1
single: RR1	1	–	00010	0	0	0	0	0	1
	0	1	–0010	0	0	0	0	0	1
RL1	1	–	00011	0	0	1	0	0	1
	0	1	–0011	0	0	1	0	0	1
LR1	1	–	00100	0	0	0	0	0	1
	0	1	–0100	0	0	0	0	0	1
LL1	1	–	00101	0	0	1	0	0	1
	0	1	–0101	0	0	1	0	0	1
AR1	1	–	00110	0	0	0	0	0	0
	0	1	–0110	0	0	0	0	0	0
AL1	1	–	00111	0	0	1	0	0	0
	0	1	–0111	0	0	1	0	0	0
double: RR1	1	–	00010	1	0	0	0	1	1
	0	1	–0010	1	0	0	0	1	1
RL1	1	–	00011	1	0	1	0	1	1
	0	1	–0011	1	0	1	0	1	1
LR1	1	–	00100	1	0	0	0	1	1
	0	1	–0100	1	0	0	0	1	1
LL1	1	–	00101	1	0	1	0	1	1
	0	1	–0101	1	0	1	0	1	1
AR1	1	–	00110	1	0	0	0	1	0
	0	1	–0110	1	0	0	0	1	0
AL1	1	–	00111	1	0	1	0	1	0
	0	1	–0111	1	0	1	0	1	0
other	1	–	–1---	–	0	1	1	1	1
	0	1	–1---	–	0	1	1	1	1
(SPEC): UMPY	–	1	–0000	–	1	0	0	0	0
TMPY	–	1	–0001	–	1	0	0	1	0
SM2C	–	1	–0010	–	1	0	1	0	1
TMLC	–	1	–0011	–	1	0	1	1	0
DNRM	–	1	–0100	–	1	1	0	1	0
SNRM	–	1	–0101	–	1	1	0	0	0
DIV	–	1	–0110	–	1	1	1	0	0
DIV1	–	1	–0111	–	1	1	0	1	0
other	–	1	–1---	–	1	1	1	1	1

Secondary Logical Unit

There are eight functions, not performed in the primary ALU of the processor. These are microcoded by SPEC in the ALU field and microorders SWAP, SWZU, SWZL, ZUY, ZLY, ASG, SRG, or RL4 in the ALUS field.

When these functions are microcoded, the secondary ALU on the processor drives the Y-bus rather than the primary ALU. ASG and SRG aid in the execution of the ASG and SRG microorders. RL4 does four-bit left rotate, and the other microorders do various byte swap and zero byte operations. The transformation from the B-bus to the Y-bus performed by each of the secondary LU operations is defined in Table 3-17.

Table 3-17. Transformation from the B-Bus to the Y-Bus

Microorder	SWAP	SWZU	SWZL	ZUY	ZLY	RL4	SRG0	ASG	SRG1
Y-bus gets 0	B8	B8	0	B0	0	B12	B8	B8	B0
1	B9	B9	0	B1	0	B13	B9	SKP	B1
2	B10	B10	0	B2	0	B14	B6	SETE	B2
3	B11	B11	0	B3	0	B15	B7	B9	B3
4	B12	B12	0	B4	0	B0	B0	B0	B8
5	B13	B13	0	B5	0	B1	B1	B1	B6 and (B8 OR B9)
6	B14	B14	0	B6	0	B2	B2	B2	B7
7	B15	B15	0	B7	0	B3	B4	B3	0
8	B0	0	B0	0	B8	B4	0	0	0
9	B1	0	B1	0	B9	B5	0	0	0
10	B2	0	B2	0	B10	B6	0	0	0
11	B3	0	B3	0	B11	B7	B11	B11	B11
12	B4	0	B4	0	B12	B8	0	0	0
13	B5	0	B5	0	B13	B9	0	0	0
14	B6	0	B6	0	B14	B10	B5	0	B6
15	B7	0	B7	0	B15	B11	B3	0	B9

Notes: The B bit (for example, B+[10]) is the B-bus bit to be passed.
0 means make that bit zero (undefined of the user).
SKP and SETE are conditions.

Special conditions of importance to the secondary LU operation are as follows:

SRG: The state of bit 10 (B+[10]) of the B-bus when SRG is coded provides one of the following transformations:

B+[10] is low (logic 0), SRG0 is selected (an SRG instruction)
B+[10] is high (logic 1), SRG1 is selected (an IOG instruction)

ASG: If the SETE (Set E) bit is high (logic 1), the microcode is responsible for setting the E bit. The state of SETE is based on the current E value and the CLE, CCE, CME bits (bits 6 and 7) in the macro-instruction according to the equation:

$$SETE = B+[7] * B+[6] + E' * B+[7] + E * B-[7] * B-[6]$$

The SKP bit high (logic 1) indicates that a skip will definitely occur. It does not include the effects of INA and SZA in the macroinstruction. If an INA or SZA is included in the instruction, the microcode must decide whether to skip (including the effects of RSS on SZA). SKP is a function of the B-bus bits (which have the ASG instruction to be transformed), the old E bit, and N+[0] and N+[1] which are bits of the N (index) register. Prior to executing the ASG special the microcode loads these bits with bits 0 and 15 of the A- or B-Register with microinstruction N := RL1(CAB).

The expressions for SKP are the following:

```
SKP = B0' * [B5 * E' + B4 * (B9' * B8 + N0' * B9' * B8' + N0 * B9 * B8')
                     + B3 * (B9' * B8 + N1' * B9' * B8' + N1 * B9 * B8')]
    + B0 * [B5 * E  + B4 * B3' * (B9 * B8 + N0 * B9' * B8' + N0' * B9 * B8)
                     + B4' * B3 * (B9 * B8 + N1 * B9' * B8' + N1' * B9 * B8')
                     + B4 * B3 * (B9 * B8 + N0 * N1 * B9' * B8' + N0' * N1' * B9 * B8')
                     + B5' * B4' * B3' * B1']
```

The equations to implement the secondary LU are as follows:

```
Y0  = B8 * (C1) + B0 * (C2) + B12 * (RL4)
Y1  = B9 * (C3) + B1 * (C2) + B13 * (RL4) + SKIP * (ASG)
Y2  = B10 * (C4) + B2 * (C2) + B14 * (RL4) + B6 * (SRG0) + SETE * (ASG)
Y3  = B11 * (C4) + B3 * (C2) + B15 * (RL4) + B7 * (SRG0) + B9 * (ASG)
Y4  = B12 * (C4) + B4 * (ZUY) + B0 * (C5) + B8 * (SRG1)
Y5  = B13 * (C4) + B5 * (ZUY) + B1 * (C5) + (B6 * (B8 + B9)) * (SRG1)
Y6  = B14 * (C4) + B6 * (ZUY) + B2 * (C5) + B7 * (SRG1)
Y7  = B15 * (C4) + B7 * (ZUY) + B3 * (C6) + B4 * (SRG0)
Y8  = B0 * (C7) + B8 * (ZLY) + B4 * (RL4)
Y9  = B1 * (C7) + B9 * (ZLY) + B5 * (RL4)
Y10 = B2 * (C7) + B10 * (ZLY) + B6 * (RL4)
Y11 = B3 * (C7) + B11 * (C8) + B7 * (RL4)
Y12 = B4 * (C7) + B12 * (ZLY) + B8 * (RL4)
Y13 = B5 * (C7) + B13 * (ZLY) + B9 * (RL4)
Y14 = B6 * (C9) + B14 * (ZLY) + B10 * (RL4) + B5 * (SRG0)
Y15 = B7 * (C7) + B15 * (ZLY) + B11 * (RL4) + B3 * (SRG0) + B9 * (SRG1)
```

where:

```
ZUY  = -M20 * M19 * M18
SLY  = M20 * -M19 * -M18
RL4  = M20 * M19 * -M18
ASG  = M20 * M19 * M18
SRG0 = M20 * -M19 * M18 * -B10
SRG1 = M20 * -M19 * M18 * B10
```

```
C1 = SWAP + SWZU + SRG0 + ASG
C2 = ZUY + SRG1
C3 = SWAP + SWZU + SRG0
C4 = SWAP + SWZU
C5 = RL4 + SRG0 + ASG
C6 = RL4 + ASG
C7 = SWAP + SWZL
C8 = ZLY + ASG + SRG0 + SRG1
C9 = SWAP + SWZL + SRG1
```

Shift Linkage

The primary ALU and some of the flags (E, O, SF, F) require external logic to control the shifting both in and out of the Y-bus and Q-bus shifters. SIO0+, SIO15+, QIO0+, and QIO15+ carry the shifted data bits into and out of the two shifters, respectively.

The shift linkage logic handles the SIO0, SIO15, QIO0, and QIO15 input, routing, and interpretation for the micromachine.

The shift microorders all reside in the SP0/SP1-fields. Only the low three bits of the field are needed. If no shift is needed it doesn't matter what is driven on the shift lines. The signals SPEC and DW are used to indicate the presence of the SP0/SP1 fields and for controlling the shift. The SHOUT output is used to identify the value of the actual shift output regardless of the size or direction of the shift.

The actual implementation has taken advantage of access to internal micromachine signals to speed up the shift linkage signal generation. The equations for the shift linkage logic are as follows:

```
SIO0  = -I8 * F0
        + I8 * (FLAG_N-1 * LWF * -DW * -SPCLF
           + E * LWE * -SPCLF * -DW + Q15 * DW + Q15 * SPCLF
           + F15 * -MIR20 * MIR19 * MIR18 * -LWE * -LWF * -SPCLF * -DW)

SIO15 = -I8 * (F15 * (-I7 * I5 * -SPCLF + -I7 * -I6 * SPCLF)
           + F14 * -I7 * -I5 * -SPCLF
           + (F15 @ R15) * I6 * SPCLF
           + (F15 % R15) * I7 * SPCLF)
        + I8 * (FLAG_N-1 * LWF * -SPCLF
           + E * LWE * -SPCLF
           + F0 * -MIR20 * MIR19 * -MIR18 * -LWE * -LWF * -SPCLF * -DW)
           + Q0 * -MIR20 * MIR19 * -LWE * -LWF * -SPCLF * DW)
           + N * MIR20 * MIR19 * -MIR18 * -LWE * -LWF * -SPCLF)

QIO0  = -I8 * Q0
        + I8 * (MIR20 * MIR19 * SPCLF * DW
           + FLAG_N-1 * LWF * -SPCLF * DW
           + E * LWE * -SPCLF * DW
           + F15 * -MIR20 * MIR19 * MIR18 * -LWE * -LWF * -SPCLF * DW)
           + SIO15 * MIR20 * MIR19 * SPCLF)

QIO15 = -I8 * F0  +  I8 * Q15
```

The SHOUT signal is used to indicate the value that should is considered the "shifted out" bit for all shift operations. The SHOUT signal is generated with the following equation:

```
SHOUT = SIO15 * MIR20 * MIR19 * SPEC + SIO15 * MIR20 * -MIR18 * SPEC
        + SIO15 * I8 * -SPEC + SIO0 * -I8 * -SPEC * -DW
        + QIO15 * MIR20 * -MIR19 * MIR18 * SPEC
        + QIO0 * -MIR20 * SPEC + QIO0 * -I8 * -SPEC * DW
```

Table 3-18. Shift Linkage Functions

Inputs					Outputs (X = don't card)		
Function	LWE-	LWF-	SPEC	DW-	SIO SHIFT	QIO SHIFT	SHOUT
single RR1	1	1	0	0	SIO0 → SIO15	X	SIO0
RL1	1	1	0	0	SIO15 → SIO0	X	SIO15
LR1	1	1	0	0	0 → SIO15	X	SIO0
LL1	1	1	0	0	0 → SIO0	X	SIO15
AR1	1	1	0	0	N → SIO15	X	SIO0
AL1	1	1	0	0	0 → SIO0	X	SIO15
single,link RR1	0	1	0	0	E → SIO15	X	SIO0
	1	0	0	0	F → SIO15	X	SIO0
RL1	0	1	0	0	E → SIO0	X	SIO15
	1	0	0	0	F → SIO0	X	SIO15
LR1	0	1	0	0	E → SIO15	X	SIO0
	1	0	0	0	F → SIO15	X	SIO0
LL1	0	1	0	0	E → SIO0	X	SIO15
	1	0	0	0	F → SIO0	X	SIO15
AR1	0	1	0	0	E → SIO15	X	SIO0
	1	0	0	0	F → SIO15	X	SIO0
AL1	0	1	0	0	E → SIO0	X	SIO15
	1	0	0	0	F → SIO0	X	SIO15
double RR1	1	1	0	1	QIO0 → SIO15	SIO0 → QIO15	QIO0
RL1	1	1	0	1	QIO15 → SIO0	SIO15 → QIO0	SIO15
LR1	1	1	0	1	0 → SIO15	SIO0 → QIO15	QIO0
LL1	1	1	0	1	QIO15 → SIO0	0 → QIO0	SIO15
AR1	1	1	0	1	N → SIO15	SIO0 → QIO15	QIO0
AL1	1	1	0	1	QIO15 → SIO0	0 → QIO0	SIO15
double,link RR1	0	1	0	1	E → SIO15	SIO0 → QIO15	QIO0
	1	0	0	1	F → SIO15	SIO0 → QIO15	QIO0
RL1	0	1	0	1	QIO15 → SIO0	E → QIO0	SIO15
	1	0	0	1	QIO15 → SIO0	F → QIO0	SIO15
LR1	0	1	0	1	E → SIO15	SIO0 → QIO15	QIO0
	1	0	0	1	F → SIO15	SIO0 → QIO15	QIO0
LL1	0	1	0	1	QIO15 → SIO0	E → QIO0	SIO15
	1	0	0	1	QIO15 → SIO0	F → QIO0	SIO15
AR1	0	1	0	1	E → SIO15	SIO0 → QIO15	QIO0
	1	0	0	1	F → SIO15	SIO0 → QIO15	QIO0
AL1	0	1	0	1	QIO15 → SIO0	E → QIO0	SIO15
	1	0	0	1	QIO15 → SIO0	F → QIO0	SIO15
UMPY	–	–	1	–	0 → SIO15	SIO0 → QIO15	QIO0
TMPY	–	–	1	–	0 → SIO15	SIO0 → QIO15	QIO0
SM2C	–	–	1	–	x	x	x
RMLC	–	–	1	–	0 → SIO15	SIO0 → QIO15	QIO0
DNRM	–	–	1	–	QIO15 → SIO0	0 → QIO0	SIO15
SNRM	–	–	1	–	x	0 → QIO0	QIO15
DIV	–	–	1	–	QIO15 → SIO0	SIO15 → QIO0	SIO15
DIV1	–	–	1	–	QIO15 → SIO0	SIO15 → QIO0	SIO15

Register Files

General Description

Two register files of 16 registers each are provided for microcode use. One is the general-purpose (GRIN) register and is used by the base set and user microcode for storage of temporary results. The other is the privileged register file (PRIN) which is reserved for use by the base set. Both of the register files are addressed by the N-Register.

The SRIN registers are a collection of 16 indirectly addressable registers. Unlike the GRIN and PRIN register files, the SRIN are not general purpose scratch pad registers. They all have special, predefined meanings and uses. Only five of the SRIN registers are defined in the A400 and they reside on the board (outside of the processor chip). The five board-resident registers and their index (N-reg) values are as follows:

N-Register Value	SRIN Register
0	map address register [MPAR]
1	lower word of parity error address latch [PER1]
2	upper word of parity error address latch [PER2]
3	central interrupt latch [CIL]
4	condition register
5–F	undefined

Theory of Operation

PRIN and GRIN Register Files

The GRIN and PRIN register files are loaded from the Y-bus and output to the B-bus when enabled. Each register file has a write enable and an output enable signal. The write enable signals, LYGRIN– for the GRIN register file and LYPRIN– for the PRIN register file, are generated by the STOR-field decode. The output enable signals, EGRINB– for the GRIN register file and EPRINB– for the PRIN register file, are generated by the B-field decode. The logic equations for the enable signals are as follows:

LYGRIN– = (STEN * MIR4 * MIR3– * MIR2– * MIR1– * MIR0–)'

LYPRIN– = (STEN * MIR4 * MIR3 * MIR2– * MIR1– * MIR0–)'

EGRINB– = (MIR9 * MIR8– * MIR7– * MIR6– * MIR5–)'

EPRINB– = (MIR9 * MIR8 * MIR7– * MIR6– * MIR5–)'

There are 16 data inputs from the Y-bus and each register has its own clock enable signal. There are dual ports for each register, but the PRIN and GRIN only require one port. Each of the 16 registers has an output enable. The registers in the file are clocked by PC–. The clock is enabled by a combination of the address from the N-Register and the write enable signal from the STOR-field decode. This is accomplished using two 3-to-8 decoders with an enable. The enable is the write enable signal and N+[3] to select between the two decoders. In this manner only the addressed register in the selected register file clocks in new data. The output enable signal to each register in the two register files is similarly controlled. A write to a register is signaled by LYGRIN– or LYPRIN– being asserted and occurs during the long half-cycle with data coming from the Y-bus. The data is clocked into the register by the rising edge of PC–.

The N (Index) Register

The N-Register is a 4-bit up/down counter and two 8-bit buffers to drive the B-bus. One of the buffers is shared with MEMR. MEMR is an 8-bit register. The upper eight bits of the B-bus are driven by the same buffer for both N and MEMR register reads. The shared N/MEMR byte supplies 7 bits of internal processor status when it is read.

The buffers are enabled with the eNb– signal. The buffer for the high order eight bits is also enabled with the eMEMRb– signal. The special DN (decrement N) causes the signal DN–. DN– goes directly to the UP/DN′ input and the counter is enabled if IN– or DN– is low. The counter is loaded from the Y-bus with the signal lyN–. When the N-Register is read (eNb–), the B-bus will get the following:

Bus Bit	Data Driven	
0	N+[0]	(N-Register bit 0)
1	N+[1]	(N-Register bit 1)
2	N+[2]	(N-Register bit 2)
3	N+[3]	(N-Register bit 3)
4	0	
5	0	
6	0	
7	0	
8	0	
9	SLAVEFF–	0 if slave asserted on the backplane
10	PEINT+	1 if parity error interrupt pending
11	ABFTCH–	0 if last fetch was A/B addressed
12	MTO+	1 if microcode timeout occurred
13	IMLOST+	1 if MLOST asserted on backplane
14	PFWFF–	0 if power fail warning asserted on backplane
15	TDI+	1 if interrupts held off

Map Address Register (MPAR)

The Map Address Register (MPAR) is a 10-bit incrementing register. It is used for reading and writing the map RAMs. MPAR is part of the SRIN register group and is accessed by an SRIN microorder when the N-Register contains 0. Whenever the MAP microorder is executed (on a map read or write) the map address comes from MPAR and MPAR is incremented at the end of the cycle. MPAR is implemented using three 4-bit incrementers followed by 16-bits of tristate buffers.

MPAR may be read onto the B-bus (eMPARb– asserted) and loaded from the Y-bus (lyMPAR– asserted). When read, B-bus[10:15] are driven with all zeros. The upper byte of the MPAR B-bus drivers are enabled onto the B-bus for CIL and PER2 reads also.

The Central Interrupt Latch (CIL)

The Central Interrupt Latch (CIL) is a read-only register that stores the trap cell address (lower 6-bits of the address bus) of the last I/O interrupt. The register is an 8-bit register although only 6-bits contain actual data. The CIL register is implemented on the PC board. The CIL register has its outputs on the GIO-bus on the board. When the CIL is read, GIO-bus bits 8 through 13 are driven onto the processor chip's internal B-bus.

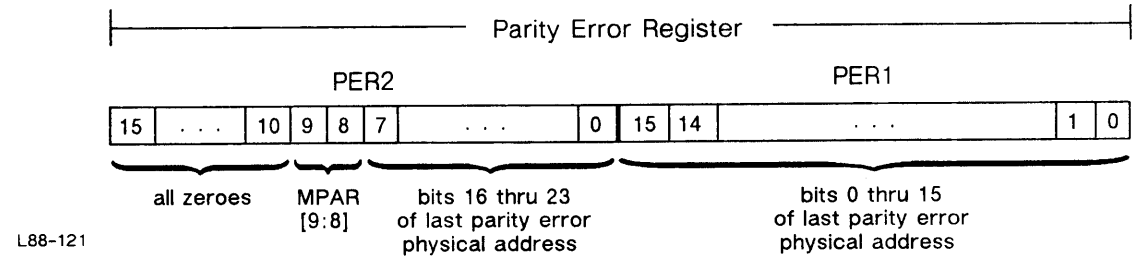
The CIL is one of the Special Registers Indexed by the N-Register (SRIN). It is selected for reading onto the B-bus by loading the N-Register with a "3" and executing an SRIN microorder in the BBUS-field. The enable signal for the CIL buffer is
eCILgio (eCILb*PC–). This signal only allows the CIL to use the GIO-bus when it is ensured that there will be no contention.

When the CIL is read, the following data is returned on the B-bus:

CIL[0:5]	→	B-bus [0:4]
0	→	B-bus [6:7]
MPAR[8:9]	→	B-bus [8:9]
0	→	B-bus [10:15]

Parity Error Register

The parity error register is actually two 16-bit registers, PER1 and PER2. The lower byte of PER2 contains the highest order 8 bits of the last parity error physical address. The upper byte of PER2 is read as all zeros in bits 15 through 10 and MPAR[9:8] in PER2 bits 9 and 8, respectively. PER1 contains the lowest order 16 bits of the last parity error physical address. The following diagram shows which bits make up the parity error register.



When a parity error occurs during a processor or I/O DMA memory access the parity error address is latched into the parity error register. The address is latched on a parity error whether parity error interrupts are enabled or not.

The actual register is implemented in two places: in the processor chip and on the PC board. The lower 10 bits of the parity error address are latched on the board while the rest are latched in the processor chip. The processor chip clocks the upper 14 physical address bits into a temporary register on every user memory access. When a parity error occurs, the contents of the temporary register are transfered to the processor chip parity error register. Refer to the GI-bus portion of the Bus Control section for more details on the implementation of the PE registers internal to the processor chip.

Memory Accessing

General Description

A memory address is required any time the processor reads or writes a word to memory. The memory referencing microorders are RDP, RDPC, RDB, FCHP, FCHB, BFB, WRB, and CWRB.

Direct Memory Access (DMA)

Direct memory access (DMA) by the I/O cards is usually given higher priority than any memory access request from the processor. If DMA is in process or pending, the next processor memory access is withheld until the current series of DMA is completed. The processor can mementarily suspend this hierarchy if it has denied access to memory for 32 consecutive DMA memory accesses. This arrangememnt grants DMA nearly the full memory access bandwidth yet permits the processor to guarantee reasonable interrupt latency in DMA intensive environments.

When there are no active or pending DMA requests, the processor initiates its memory request to the memory card. In a memory read transaction, the addressed data is returned at the end of the memory cycle. In the case of a memory write request, the data to be stored is sent to the memory card at the same time as the

address at the start of the memory cycle. A memory read request is distinguished from a write request by the sense of the write enable bit (WE–) sent to the memory card.

Address Generation Logic

A memory address consists of a 15-bit logical address, a 5-bit map number, and the MEMDIS bit which forces boot memory to be used. The entire memory address is latched at the time that the memory reference microorder is executed. When the backplane is not busy, the memory reference occurs. The map number is taken from MEMR register (bits 0–4), as is MEMDIS (bit 5). When a memory write occurs the data to be written and the address are latched at the same time.

RDP, RDPC, FCHP, and WRP specify that the logical address originates in the P-Register. Otherwise, the address originates on the B-bus. This address is then transformed by the address generation logic to form the logical address that is latched for sending over the backplane.

During a JTAB line execution, the address source is MRG resolved (the MRG instruction presented is changed to an address). If base releative mode is enabled (BASE bit 15 is a one) and the address source (after MRG resolution) is in the base page, the base register is added to the address.

If base-relative mode is enabled and the microorder is either FCHB, FCHP, BFB, or RDPC, and the address source is not in the base page, the low order bit of the map number is forced to be a one. Forcing the low-order bit of the map number to one determines that it is a code-map reference. If the low-order bit of the map number is a zero, it is a data-map reference and the microorder is either RDB, WRB, WRP, or CWRB.

The final logical address is always latched in the MA register. FCHP and FCHB cause the final logical address to be latched in the FA register also.

Data from a memory read which does not address A- or B-Registers is returned in the T-Register. The T-Register is not modified except by a processor memory read.

Theory of Operation

The T-Register

Data returned from a memory read or an I/O read is latched in the T-Register. The register is clocked by DC– so that data corrected by memory is latched. The clock is enabled by the signal ETFRZ– which is generated from TFRZ– and MEMCE–. The ETFRZ– signal indicates that a memory read or an I/O read is in progress or pending. Since it is impossible for the micromachine to read the T-Register while this signal is asserted (the processor clock would freeze), it does not matter that T

can be clocked more than once. Since valid data is always returned during the last cycle of the read, the data that ends up latched into the T-Register will be correct.

ETFRZ- = TFRZ- * MEMCE-

A memory read may reference the A- or B-Register. There is no data path to put these registers into the T-Register since they are in the general purpose register file (GPRF). The T microorder in the B-field of the microinstruction will enable either register T, A, or B to the B-bus depending on the last memory read. The signal LRAB+, which is a latched version of the signal MABAB+, indicates that the read is from register A or B. If this signal is asserted, the micromachine register file is enabled onto the B-bus when T is the microorder. The signal ETABB- indicates that the T microorder was encoded in the B-field of the microinstruction. Therefore the T-Register is enabled onto the B-bus by the signal ETABB- only if the last read was not A or B addressed. The signal LRAB- is cleared on an I/O read so that the processor may access the data returned to the T-Register even if A or B was addressed.

ETABB- = (MIR9 * MIR8- * MIR7 * MIR6- * MIR5)'

GETABB- = ETABB- + LRAB

The data to be clocked into the T-Register must be valid at the D+ pads 12.97 nsec before the rising edge of the DC- clock.

Memory Address Bus (MAB) Generation

Memory addresses originate either in the B-bus or in the P-Register as specified by the microorder. The P-Register normally holds the program counter. The P-Register consists of four 4-bit counters (P1, P2, P3, and P4).

The signal LYP- causes the P-Register to be loaded from the Y-bus, and IP- enables the counter to increment. The P-Register and B-bus address sources are multiplexed together to generate the memory address bus (MAB) by fifteen single 2-to-1 multiplexers. MRG address resolution is also accomplished by these multiplexers with some additional gates for the upper five bits.

When JTAB is executed, the data on the B-bus, if a memory reference is requested, is actually a memory reference group instruction. The ten low-order bits are address bits and B-bus bit 10 (B+[10]) selects either the base page or the current page. If B+[10] is 0, the base page is selected and the upper 5 bits are set to zero. If B+[10] is 1, the current page is selected and the upper five bits of MAB come from the P-Register. The complete address is formed as follows:

		B-Bus Source Output on MAB		R-Register Source Output on MAB
BBUS	Definition	BB[10]=0	BB[10]=1	
0–9	MRG address	BB[0:9]	BB[0:9]	P[0:9]
10	C/Z bit	0	P10	P[10]
11–14	Instruction	0	P[11:14]	P[11:14]

The AND gates trailing the high-order five bits of the MAB multiplexers, U310 through U314, zero the multiplexer outputs if B+[10] is low and JTAB– is low. The Select-S input to these high-order five MAB multiplexers is altered so that the P-Register is always selected when JTAB– is asserted.

MAB contains the memory address unmodified by the base register. MAB+[0] is sent to the MIO Support Logic to determine whether to write to the A- or B-Register if ABWR– (A/B write) is asserted.

ABWR– is the OR of MABAB– and MEMWR–. MABAB– is true if the 15-bit MAB bus has the value of zero or one. Another way of stating this is that MABAB– is true if MAB+[14:1] contain all zeros. This is the condition tested for with U320 through U322 and U324. MABAB– is further qualified by ABAB– (A/B addressability) from the MEMR Register. MEMWR+ is true if the microorder specified a write.

If MAB references the base page and not the A- or B-Registers, and the base register logic is enabled (base register bit 15 is 1), BASEPG+ is asserted.

If the upper five bits of MAB, MAB+[14:10], are zero then BASEDET+ is asserted. This means the memory reference is to the base page unless MABAB– is asserted. In the latter case, the memory reference is actually to the A- or B-Registers in the CPU. Therefore, the main memory base page reference signal BASEPG+ is the AND of BASEDET+ and MABAB–.

Base Register Logic

The base register is added to all addresses except 0 and 1 in the base page if it is enabled.

The 15 lower bits of the base register are always added to MAB by four CLA_ADD 4-bit adders (B1, B2, B3, and B4). If bit 15 of the base register is a logic 1, and the reference is to base page (BASEPG+ asserted), fifteen 2-to-1 multiplexers (U500 through U514) put the output of the adders onto the MAB2 bus. Otherwise the MAB bus is passed unchanged to the MAB2 bus.

When the base register is enabled (BR+[15] is a logic 1) the hardware distinguishes between memory references to code and to data and sends them to different maps. The low bit of the address extension bus (map number) is forced to a logic 1 indicating a code map in either one of two cases: if the memory reference is begun by an MRG instruction that does not reference the base page; or if the microorder executed is FCHB, FCHP, BFB, or RDPC.

The base register itself consists of four 4-bit registers (F3). It is loaded with the signal LDBA–. The base register bits are as follows:

Bit	Explanation
15	0 = base register disabled
14–0	don't care
15	1 = base register mode
14–0	base register value

Memory Address and Data Latches

The final resolved address on the MAB2 bus is latched in three places. The memory address register (AOUT) is the primary register for getting addresses out to main memory. It is a 16-bit transparent latch. Whenever there is not a memory request pending (MRP+), the AOUT transparent latches switch to "open" during the SHC of SHFT_SC+. This prevents the AOUT latch from opening prior to MRP+ asserting, which could destroy the address being held.

If a memory request is pending, the memory address and data latches already hold address and data waiting to be sent out to the backplane. A new memory microorder at this time will cause a clock freeze, and the MAB2 bus will not change until after there is no longer a memory request pending.

Every memory address is latched in the MA register (F1). A memory microorder is signaled by MEMRQ+ which enables MA to be clocked. This register is necessary so that the microcode can recover the resolved address to get sequential addresses for multiple word operands.

If a fetch microorder is executed (FCHP or FCHB), the signal FTCH– causes the register (F2) to be be clocked. The MAB2 bus is stored in register FA so that the microcode can recover the address of the last fetch if a violation occurs (that is, a memory protect violation).

The output of AOUT (AOUT+[0:14]) goes to the MAP multiplexer, Page Address latch, and GO MUX. These are covered in the Bus Control section.

The address extension bus latch (Z1) is gated with the same signals as the memory address latch. The map number which goes onto the address extension bus (AEOUT+[0:4]) originates in the MEMR register.

If MCD is high, the memory subsystem will never initiate any memory cycles on the backplane. This allows the microcoded self-test to test the memory addressing logic without assuming that the memory controller works.

MEMR Register:

The MEMR register contains memory related control signals which the microcode has direct access to it. The format of MEMR is as follows:

Bit	Contents	Description
0	MAEB0	Address Extension Bus Bit 0
1	MAEB1	Address Extension Bus Bit 1
2	MAEB3	Address Extension Bus Bit 3
3	MAEB4	Address Extension Bus Bit 4
4	MAEB5	Address Extension Bus Bit 5
5	ABAB	A/B Addressibilty Enable.
6	MEMDIS	Memory Disable (backplane line to enable boot memory)
7	MCD	Memory System Disable
8	0	
9	SLAVEFF-	Slave Request
10	PEINT	Parity Error Interrupt
11	ABFTCH-	A/B Fetch Interrupt
12	MTO	Microcode Time Out
13	IMLOST	Memory Lost
14	PFWFF-	Power Fail Warning
15	TDI	Temporary Disable

Bits 8 through 15 are actually part of the N-Register. However, they are enabled onto the Y-bus along with the MEMR bits.

Data Latch:

The data latch (DOUT) latches the Y-bus at the end of the processor cycle in which a WRIO- or a memory write (MEMWR-) occur. SC+ is used to generate the latch signal, which is asserted (DOUT opens), during the LHC unless there is a freeze. SPCL_WRITE- is referenced in the Bus Control section.

Data from the latch must be enabled onto the backplane data bus while the processor is driving MEMGO for a memory write and during the last two cycles of an I/O write handshake.

The output of DOUT (DOUT+ bus) is driven to the GO and DO multiplexers.

Memory and I/O State Machine and Control Logic

General Description

The Memory and I/O (MIO) state machine of the processor generates control signals for the memory address logic. One pending memory reference can be held in the address and data latches if the backplane is busy. The memory state machine determines when backplane control signals are asserted and when address and data are latched. The I/O microorders are WRIO and RDIO. The MIO state machine controls the backplane signals to perform an I/O handshake when one of these microorders is executed. The following three figures show the signal timing for memory and I/O backplane signals initiated by the MIO state machine. Figure 3-9 shows memory read, Figure 3-10 shows memory write, and Figure 3-11 shows I/O instruction broadcast.

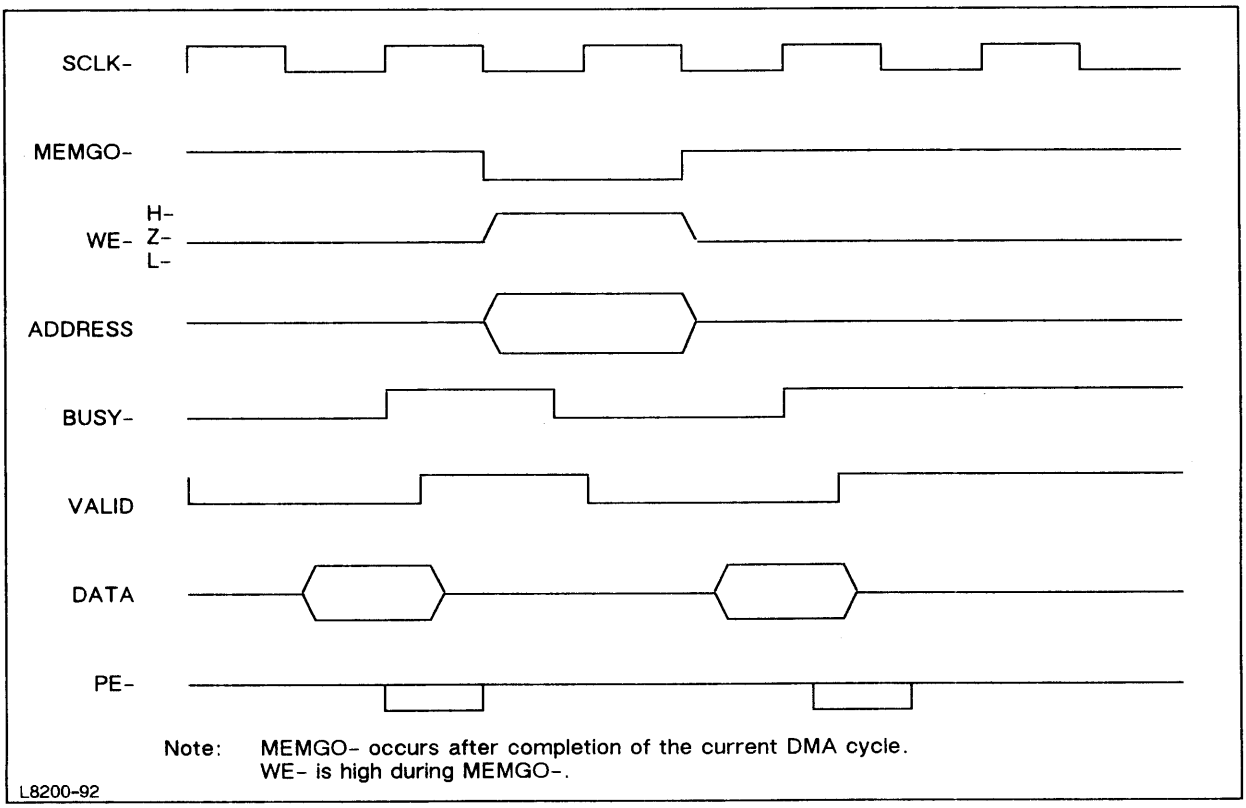


Figure 3-9. Backplane Signals for Memory Read

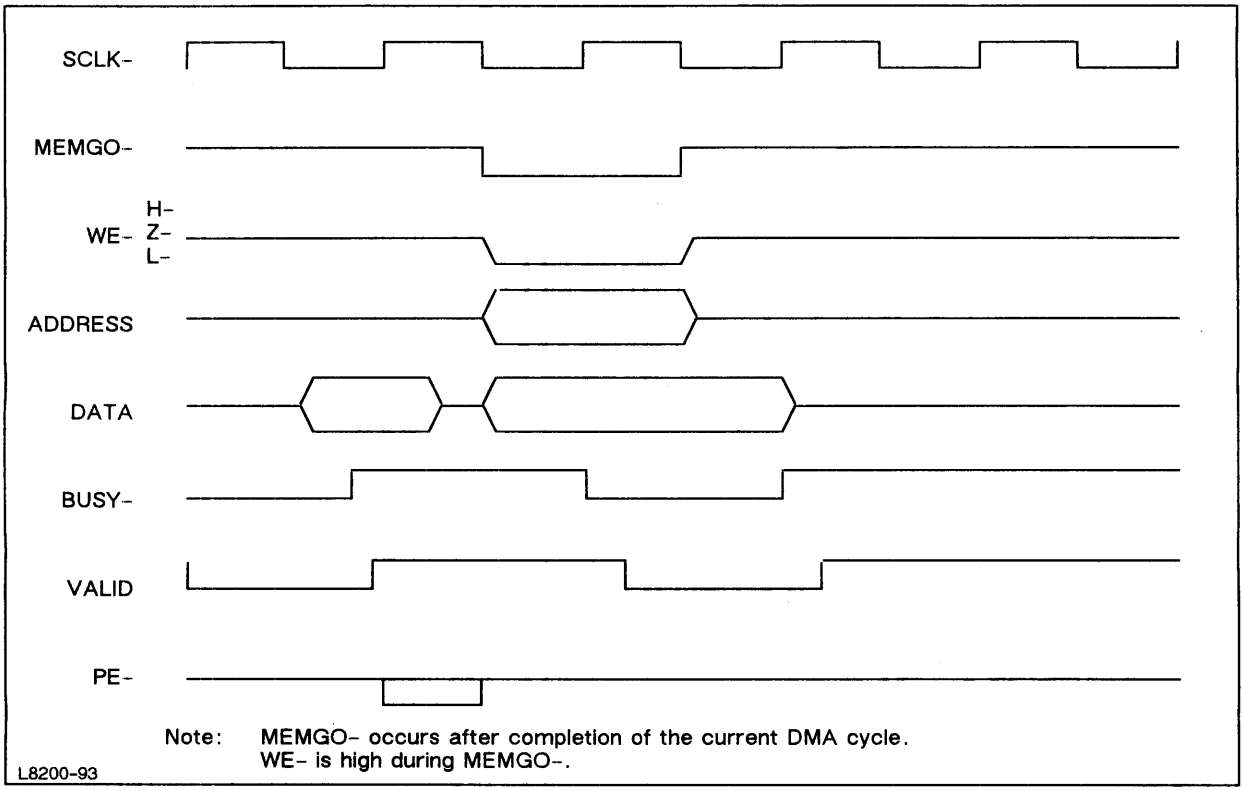


Figure 3-10. Backplane Signals for Memory Write

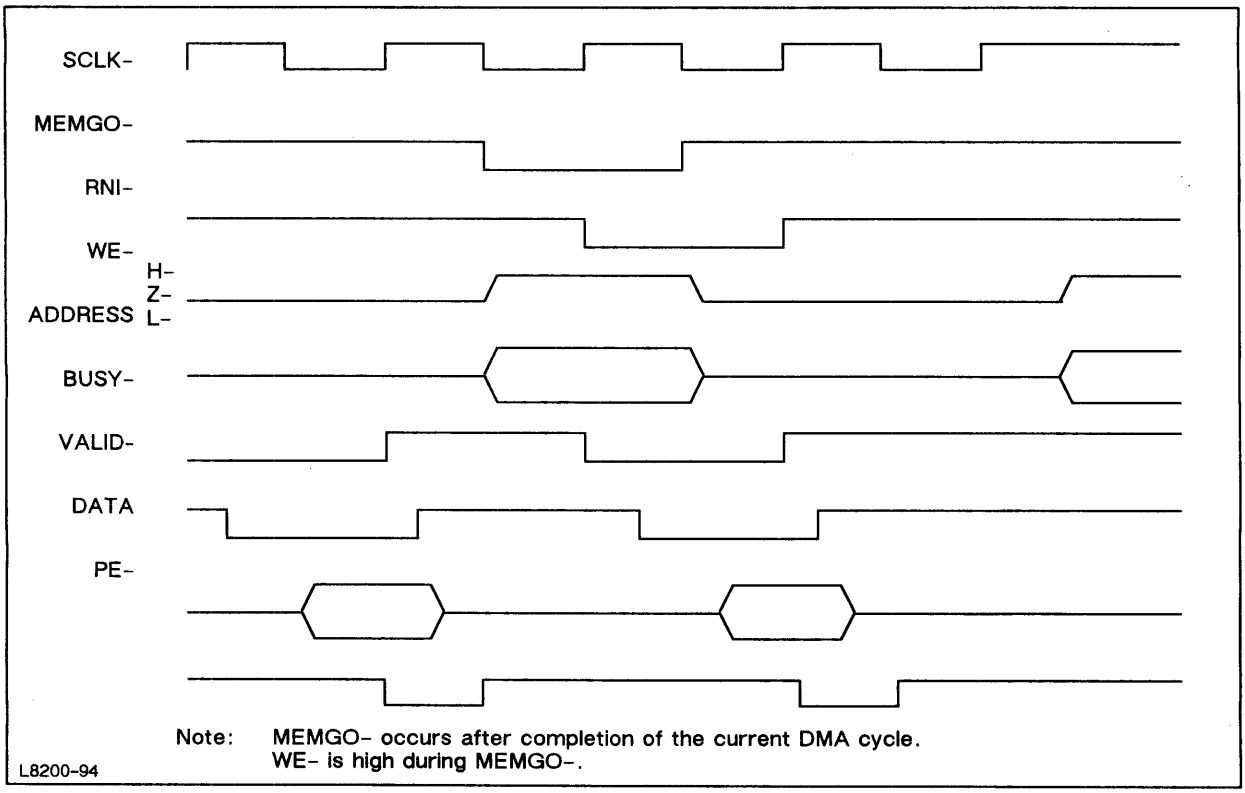


Figure 3-11. I/O Instruction Broadcast

Theory of Operation

Memory accessing microorders are as follows:

WRP Memory write with address in the P-Register. Data comes from the Y-bus.

WRB Memory write with address on B-bus. Data comes from the Y-bus.

CWRB Conditional read/write. A memory access will occur with the address on the B-bus. If B-bus bit 15 is low, a write will occur with the data on the Y-bus. If BB15 is high a read will happen. This microorder aids in the resolution of indirects which will be followed by a store.

RDP2 RDP in the SP2-field. Memory read with address from P-Register.

RDP0 RDP in the SP0-field. Memory read with address from P-Register.

RDB2 RDB generated by the JTAB logic or a RDB in the SP0-field. Memory read with address on B-bus.

FCHB Fetch with B. Fetch next instruction with address on B-bus. This microorder will not be executed if an interrupt is pending. Register FA is updated if it is executed.

FCHP Fetch with P. Fetch next instruction with address in the P-Register. This microorder will not be executed if an interrupt is pending. FA is updated if it is executed.

BFB Broadcast fetch with B. A memory read is done with the address on the B-bus. RNI is asserted during this access so that I/O masters and slave devices will pick up the instruction. FA is not updated.

IFCH Interrupt fetch. IAK is asserted on the backplane and a memory read is done. No address is driven on the backplane since IAK is asserted. RNI is not asserted, and the I/O master will provide the address. FA is not updated, and MA is updated but it will not hold the address from from where the read occurred. The read address is latched in the CIL register.

FCHP and FCHB are qualified in the interrupt logic and combined into the signal FTCH- which is asserted to cause a memory fetch.

All of the memory signals are combined in a 10-input NAND gate to form the signal MEMRQ+. This signal is asserted to request a memory access microorder.

Memory access microorders which are writes cause MEMWR+ to be asserted. The expression for generation of MEMWR+ is the following:

```
MEMWR+ = NOWRT- * (WRP + WRB + (CWRB * BB15-))
```

NOWRT- asserted means a parity error occurred in the previous cycle. Writes must be suppressed since the parity error has introduced bad data.

MABAB– is true if the address on the MAB bus is zero or one. This means that the access of this cycle is to the A- or B-Register. MABAB– and MEMWR– generate ABWR–, the signal that indicates a write to the A- or B-Register.

MEMAC+ indicates that a memory access over the backplane is being requested this cycle. It is the signal which actually fires off the MIO State Machine. The MEMAC+ circuitry is discussed in the following section.

MEMAC+ Generation

The assertion of MEMRQ– when the MAB+[0:14] address is not for the A- or B-Register (MABAB+ deasserted) is the indication that the processor is requesting a memory cycle. The MIO state machine will try to initiate a memory access when it detects the assertion of the signal MEMAC+.

```
MEMAC+ = MEMCYC_RQ+ * DO_MEMAC+
```

where:

```
MEMCYC_RQ  = MEMRQ+ * MABAB-
DO_MEMAC+ = FREEZE- + (NONGIO_FRZ- * GIO_SCND- * SPCL_WR2B-)
```

MEMAC is selectively asserted when a micromachine freeze condition exists.

When the freeze is due to a resource conflict for the GIO-bus, it is imperative to allow the memory cycle to start. The conflict will only be resolved once BUSY asserts. Only by asserting MEMAC is BUSY assured of asserting. However, if the freeze is due to either a non-GIO related freeze condition or the special memory write condition (that is, wrp := map), the memory access needs to be held off by the freeze. There is logic to handle this. The output of this logic circuit, MEMAC+, is then input to the memory and I/O state machine (MIOSM).

If the micromachine requests a memory cycle, MEMCYC_RQ+, and there is no freeze, then the request is indicated by MEMAC+ asserting. If a non-GIO freeze occurs, then MEMAC+ is held off until the freeze terminates. However, if the freeze is a GIO freeze that is not the special write/map read cycle, then MEMAC+ is asserted despite the freeze. This is provided by an AND gate.

For non-special GIO-related freezes, the assertion of MEMAC must be limited to one cycle. This is because the micromachine is frozen and the conditions that requested the memory access will persist for a minimum of two SC cycles. The signal GIO_SCND+ is used to indicate the second or subsequent cycle of a GIO freeze condition.

If the freeze is due to the special write/map read condition, then the signal SPCL_WR2B+ will prevent the assertion of MEMAC until FREEZE– deasserts when SCND_CYCLE– asserts. This will essentially prevent the MIOSM from transitioning into a state that indicates a memory access is in progress.

After the first LHC that SPCL_WR2B+ is asserted, the SCND_CYCLE signal will be set. The assertion of MEMAC will assert MGO if MRQ isn't set and at the next

SC-↑ cause the MIOSM to leave the idle state. SCND_CYCLE will only persist until the SC-↑ after BUSY asserts, clearing the SPCL_WR2B+ signal.

Since MGO is a combinatorial output it may glitch if MEMAC+ glitches. Even if MEMAC+ does glitch and eventally deasserts, MGO+ will definitely be deasserted long before the next SC-↑ so as not to mislead the MIOSM or the backplane.

Memory and I/O State Machine

The memory and I/O state machine (MIOSM) is patterned after the finite state machine of the A700. The A700 finite state machine is implemented via a programmable logic array (PLA) chip, whereas the A400 version is implemented with random logic and flip-flops in the processor chip.

The state machine keeps track of the memory and I/O accesses. It initiates the assertion of MEMGO, and it can freeze the processor when necessary. It also controls the assertion of IOGO.

The equations for the MIOSM are derived from the original PLA equations. The original PLA equations were minimized to produce the equations below:

```
ZPREMGO = -HOLD * BPON * MRP * -MAIP
          + MEMAC * -HOLD * BPON * -MRIOIP * -TFRZ * -IAIPRP * -DIST
            * -MAIP
ZPIOGO  = -HOLD * BPON * IAIPRP * -DIST * -MAIP
          + -MEMAC * -HOLD * WRIO * BPON * -TFRZ * -MRP * -DIST * -MAIP
          + -MEMAC * -HOLD * RDIO * BPON * -TFRZ * -MRP * -DIST * -MAIP
          + BPON * MRIOIP * -MAIP
ZMRIOIP = MEMAC * -HOLD * BPON * -PMEMWR * -TFRZ * -MRP * -DIST
            * -MAIP
          + BPON * MRIOIP * -DIST * -MAIP
          + IORQ * BPON * MRIOIP * IAIPRP * -MAIP
          + -VALID * BPON * MRIOIP * MAIP
          + -HOLD * BPON * TFRZ * MRP * -DIST * -MAIP
          + -HOLD * BPON * IAIPRP * -DIST * -MAIP
          + -MEMAC * -HOLD * WRIO * BPON * -TFRZ * -MRP * -DIST * -MAIP
          + -MEMAC * -HOLD * RDIO * BPON * -TFRZ * -MRP * -DIST * -MAIP
ZTFRZ   = BPON * -MRIOIP * TFRZ  +  BPON * TFRZ * DIST * MAIP
          + IORQ * BPON * TFRZ * IAIPRP * -MAIP
          + MEMAC * BPON * -PMEMWR * -IAIPRP * -MRP * -DIST
          + BPON * TFRZ * IAIPRP * -DIST * -MAIP
          + -MEMAC * RDIO * BPON * -IAIPRP * -MRP * -DIST
          + -VALID * BPON * TFRZ * MAIP
ZIAIPRP = BPON * MRIOIP * IAIPRP  +  BPON * IAIPRP * -DIST
          + -MEMAC * WRIO * BPON * -MRP * -DIST
          + -MEMAC * RDIO * BPON * -IAIPRP * -MRP * -DIST
ZMRP    = HOLD * BPON * MRP  +  MEMAC * HOLD * BPON * -IAIPRP * -DIST
ZDIST   = -VALID * BPON * MRIOIP * TFRZ * -IAIPRP * MRP * DIST
          + MEMAC * -VALID * BPON * -PMEMWR * MRIOIP * TFRZ * -IAIPRP
            * -MRP * -DIST
          + -VALID * BPON * MRIOIP * TFRZ * IAIPRP * -MRP * DIST
          + -MEMAC * -VALID * RDIO * BPON * MRIOIP * TFRZ * -IAIPRP
            * -MRP * -DIST  +  BPON*MRIOIP*-MAIP
ZMAIP   = -VALID * BPON * MAIP  +  -HOLD * BPON * MRP * -MAIP
          + MEMAC * -HOLD * BPON * -MRIOIP * -TFRZ * -IAIPRP * -DIST
            * -MAIP
```

The "Z" before the outputs denotes the next state value of the outputs.

The MIOSM state registers are cleared by BPON, so that it always powers up in state zero. For this reason, some of the BPON terms have been removed from the implementation.

Figure 3-12 shows the memory and I/O state machine diagram.

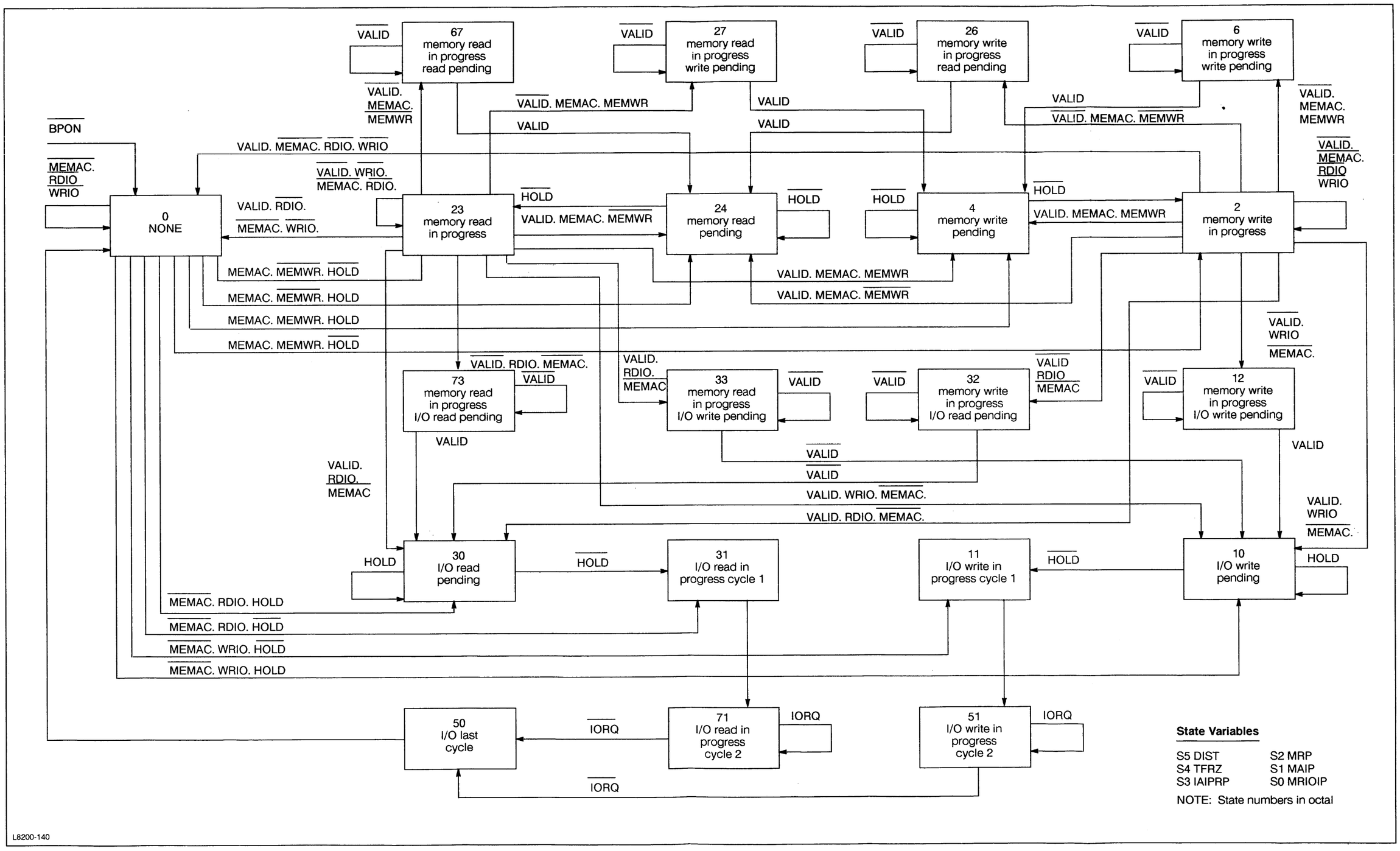


Figure 3-12. Memory and I/O State-Machine State Diagram

The memory and I/O finite state machine outputs have the following conditions:

a. MRP is asserted if a memory request is pending. The backplane was busy when the last memory microorder was executed and the address and data (for a write) were latched. The access will happen when the backplane is no longer busy.

b. MAIP is asserted if a memory request is in progress. MEMGO has been asserted and the memory circuitry is currently busy.

c. TFRZ is asserted if the T-Register is not valid, that is, read data has not yet returned. The processor will freeze if it attempts to access the T-Register while TFRZ is asserted. TFRZ is deasserted when the memory controller signals read data has returned via CHIP_VLD+.

d. MR!OIP is true if a memory read or any I/O access is in progress.

e. IAIPRP is asserted if an I/O access is in progress or pending.

f. PREMGO indicates the first cycle of a memory access and MEMGO should be asserted on the backplane if possible (no DMA in progress).

g. IOGO is true if IOGO should be asserted on the backplane.

The HOLD signal indicates that the backplane is busy. A memory cycle may not be started this cycle. HOLD is the OR of BUSY and IMRQ and SMRQ. A memory cycle cannot be started if another memory cycle is in progress (BUSY), if DMA is requesting a memory cycle (IMRQ), or is currently involved in a cycle (SMRQ). SMRQ was included to prevent the MIOSM from getting out-of-sync with the bus control circuitry after an aborted DMA cycle.

The MIOSM powers up in state 0, and MEMAC, RDIO, or WRIO must be asserted in order for it to leave state 0. If HOLD is true when MEMAC is asserted and the MIOSM is in state 0, the next state will be one with MRP asserted. Thus, the MIOSM "remembers" that a MEMAC was asserted during the HOLD condition. When HOLD becomes false a transition will be made to a state with MAIP and MRIOIP asserted.

The signal CHIP_VLD+ originates in memory controller logic of the processor chip and is asserted for one cycle during the last cycle of any memory access. CHIP_VLD+ indicates to the state machine that the memory access in progress is over.

MEMAC will never be asserted if MRP is true, since another memory access, while one is being held in the latches, will cause the processor to freeze. The freeze signal holds off MEMAC. Thus, one memory access request (while the backplane is busy) may be queued but a second memory access request results in a freeze.

The state of the MEMWR signal at the time of the memory access microorder determines whether the following states will include MRIOIP or TFRZ (state 2 or 23).

RDIO and WRIO cause entry to states with IAIPRP asserted. RDIO in addition causes TFRZ to be asserted.

MEMGO Circuitry

In order to get maximum speed out of the memory system, a memory cycle is begun during the cycle in which it is requested by the microcode, if possible (that is, MRQ is not asserted). The start of a memory cycle is signaled to the memory control logic by the assertion of both MGO+ and QMGO+. MGO+ is typically asserted for one and only one SC+ cycle (LHC then SHC). QMGO+ is a qualified version of MGO+. QMGO+ asserts with MGO but deasserts on the SHFT_SC-↑ that occurs during the SHC of SC-.

MGO+/QMGO+ are asserted on the SC-↓, while the state machine is still in state zero. The basic condition for asserting MGO+/QMGO+ is that the current state does not assert MAIP and the next state will assert MAIP. The memory cycle actually begins with the assertion of MGO+/QMGO+ one LHC before MAIP is asserted.

If an I/O device asserts MRQ- in the same cycle as the processor asserts QMGO+, the MRQ prevails and QMGO/MGO+ must be deasserted before the end of the cycle and not reasserted until the DMA cycle is over. IMRQ- becomes valid very late in the cycle. It is early enough that its assertion will cause the next state to be MRP rather than MAIP, but late enough that MAIP will not be deasserted early enough to prevent QMGO/MGO+ from being asserted. Therefore, IMRQ- bypasses the state machine and is an input to the gate which generates QMGO/MGO+.

During an interrupt fetch (IFCH) the address and MEMGO are driven by the I/O master, so IFCH- and IAKP- both hold off MGO+/QMGO+ also.

Microorders FCHB, FCHP, BFB, and IFCH need additional hardware outside of the state machine. As far as the state machine is concerned these are ordinary memory reads. They are distinguished through signals latched in the Last Read Register. These flip-flops are clocked every time there is a memory read.

Note that the logic corresponding to FCHB/FCHP, BFB, and IFCH, are actually latches. The flip-flops associated with these signals are located on the PC board. Implementing these flip-flops on the board allows the signals to meet the timing requirements of the A/L-Series backplane. Therefore, the latches need only ensure adequate set-up and hold time to the flip-flops on the board (versus the backplane).

A flip-flop is used to remember whether the last read accessed the A- or B-Register. These flip-flops must be cleared by RDIO, since I/O read data is returned only to the T-Register. However, if the last read was from either the A- or B-Register, a T microorder enables the A- or B-Register onto the B-bus and not the T-Register.

Signal ENDMRD+ is asserted during the last cycle of a processor memory read. It is generated with MRIOIP+ and CHIP_VLD+. When a fetch is executed, the signal TCNT- must be asserted during the last cycle of the read to signal to the processor to latch the instruction into the counter register.

Signal MRIP is asserted during a memory read. It is true if a memory access is in progress (MAIP) and a memory read or I/O access is in progress (MRIOIP).

Microorder BFB differs from an ordinary read in that RNI is asserted on the backplane during the memory cycle. RNI must be asserted while BUSY is asserted by the memory controller logic. IRNI+ is asserted with RNIP– and MRIP–. IRNI+ is inverted and driven onto the backplane as RNI+.

Microorder IFCH differs from an ordinary read in that IAK– is asserted on the backplane, MGO+/QMGO+ is not asserted, and the address bus is not driven. IIAK+ is asserted with MRIP– and IAKP–. IAKP– is a latched version of IFCH+. IFCH– and/or IAKP– hold off MGO+/QMGO+. On its way to the backplane, IIAK+ is used to disable the address drivers. IIAK+ is inverted and driven onto the backplane as IAK–.

A read should not be in progress when any of these four microorders (FCHB, FCHP, BFB, and IFCH) are executed or the new read will overwrite the latches and change the type of the current read being executed. It can be ensured that any previous read is finished by executing microorder T in the BBUS field in the previous cycle or the same cycle as the FTCH, BFB, or IFCH. In addition, a freeze will occur if any memory cycle is in progress and a fetch (FCHB or FCHP) is executed.

A/B Fetch

Signal ABFTCH– is true if the last memory read was a fetch and the last memory read addressed either the A- or B-Register. Both of these signals (PTCNT+ and LRAB+) are available from the Last State Register. ABFTCH– becomes an input to the interrupt prioritizer. It is also a status bit available in the N-Register. The status bit is used in I/O broadcasting, since an instruction cannot be broadcast from the A- or B-Register directly. Note that the ABFTCH– status bit is only valid until the next memory read.

A/B-Register Detect Logic

The A- and B-Registers are provided in the HP 1000 architecture as fast scratch-pad registers. To avoid special addressing modes for these registers, they are addressed as memory location 0 and 1, respectively.

While providing fast memory and ease of addressing, special hardware must monitor memory addresses to always be aware of any access to the A- or B-Register. This hardware is the A/B Detect logic.

NOR gates monitor the MAB bus for zero or one addresses. This logic must be enabled with ABAB– in order to detect A- or B-addresses. ABAB– is an output of the MEMR register.

BASEPG+ detects if the access is to the base page but not A or B. BASEPG+ is asserted if MAB+[10:14] are zero (base page access) and MAB+[1:14] are not zero (not A or B).

CPUTURN Logic

CPUTURN is a backplane signal which the processor asserts to gain access to memory. CPUTURN is only invoked by the processor when it has been locked out from accessing memory for 32 consecutive DMA memory cycles. This arrangement grants DMA nearly the full memory access bandwidth, yet permits the processor to guarantee reasonable interrupt latency in DMA intensive environments.

Two counters (Q6 and Q7) count the number of DMA memory cycles while the processor is frozen. The processor uses the signal SECOND+ from the memory controller to clock the counters. SECOND+ is a SHC-delayed version of BUSY+. By using SECOND+ there is a full cycle for ICPUTURN+ to propagate onto the backplane to set up the MRQ flip-flops on the I/O Interface.

When 32 DMA cycles have occurred, CPUT_32 asserts. This causes ICPUTURN+ to assert. It also causes the clock to the counters to lock in a high state, thus preserving ICPUTURN+ until the freeze deasserts. The deassertion of FREEZE– causes the counters to clear.

Interrupt System

General Description

There are two types of interrupt requests in the HP 1000 A400 Processor. System level interrupts may be generated by the processor to handle system level problems such as power fail and parity error. I/O interrupts may be requested by the individual I/O cards to cause processing to service the needs of that I/O channel.

System Level and I/O Interrupts

The processor receives all system level and I/O interrupt requests and determines which interrupt will be serviced. Three basic levels of importance define the relative priority of interrupt requests. A level one interrupt request has no restrictions in obtaining interrupt service. Level two and level three requests are collectively enabled/disabled by an STC/CLC 4, the interrupt inhibit flag. Level three interrupt requests may be further enabled/disabled by an STF/CLF 0, the interrupt system flag. In addition, interrupt masks are available to mask off any or all of the level three interrupt requests. A hardware signal from the processor prevents one of the level two and all level three requests from interrupting following certain instructions and slave mode transfers.

Micromachine Interrupt Level

The interrupt micromachine hardware synchronizes and qualifies the interrupt sources. The highest priority interrupt is determined and the INTP condition is generated if an interrupt is pending. The INTF condition is generated when a fetch is held off by the hardware due to a pending interrupt.

The IST register is the interface between the interrupt system and the microcode. It contains those interrupt bits which are only set by the microcode and all the interrupt mask and enable bits. It is used to read the output of the priority encoder and to set or clear the interrupt latches.

Theory of Operation

INTP indicates to the microcode that an interrupt is pending. A microroutine will check INTP if the microroutine can be interrupted. The INTF condition corresponds to the hardware signal INT+. INTF and INT+ are used interchangeably in this description.

Every microroutine must end with a fetch microorder (FCHB or FCHP). If INTP is true when the fetch microorder is executed, the fetch will not occur and the INT+ signal is set. Also, INT+ is set if INTP is false (no pending interrupt) and the fetch is A/B addressed (no path for macroinstruction in A/B to T/CT). The INTF condition is tested immediately before any microinstruction line with a JTAB on it.

If INT+ is set, the interrupt service microcode must be executed before the JTAB subroutine, since there is not a valid instruction in the counter. The masking and prioritization of the interrupt sources and the generation of INTP+ and INT+ are done by the Interrupt Mask and Priority (IMP) logic M1. This logic is based on a Field Programmable Logic Array of the A700. The equations for the IMP are shown below. The inputs to the IMP are defined in subsequent sections.

```
SETINTP+  = MIM- * (PEINT + MPINT + SLAVEFF +  FLTO)
            + TDI- * MIM- * (TBGT + TBGF + (PFWE  *  PFWFF)
            + (INTRQM * INTRQFF))

SETINT+   = PFTCH * MIM- * (PEINT + MPINT + SLAVEFF +  FLTO)
            + TDI- * PFTCH * MIM- * (TBGT + TBGF + (PFWE  *  PFWFF)
            + (INTRQM * INTRQFF)) + PFTCH * MIM- * MABAB

PPR3-     = ABFTCH

PPR2-     = ABFTCH- * PEINT  + ABFTCH- * MPINT  + ABFTCH- * SLAVEFF
            + ABFTCH- * TBGT * TDI-

PPR1-     = ABFTCH- * PEINT  + ABFTCH- * TBGT  * TDI-
            + ABFTCH- * MPINT- * SLAVEFF- * FLTO
            + ABFTCH- * MPINT- * SLAVEFF- * PFWE * PFWFF * TDI-

PPR0-     = ABFTCH- * TBGT  * TDI-  + ABFTCH- * PEINT- * MPINT
            + ABFTCH- * PEINT- * SLAVEFF- * FLTO- * TBGF  * TDI-
            + ABFTCH- * PEINT- * SLAVEFF- * PFWE  * PFWFF * TDI-
```

Interrupt Status (IST) Register

The IST is the interface between the microcode and the interrupt system. The bits of the IST register, referenced by microorder IST, are as follows:

0–3	interrupt control
4	PEE
5	PFWE
6	MRGIE
7	MIM
8	INTRQM
9	FLTO
10	TBGON
11	PS–
12	MP–
13	SCHOD–
14	CRS
15	TBGF

The upper 12 bits of the IST register are maintained in a 12-bit register. The outputs of the registers are buffered and enabled onto the B-bus when the EISTB– signal is asserted. The lower four bits of the B-bus on IST reads come from a 4-bit buffer. The buffer drives a registered version of the PPR+[0:3] outputs of the IMP. These four bits encode the highest priority interrupt pending.

When LYIST– is asserted to load the IST, the low four bits of the Y-bus are enabled through a 3-to-8 decoder, to generate set and clear signals to each of the interrupt-latch flip-flops. This path is one of the worst-case setup time paths on the Y-bus. The status bits are defined as follows:

PEE – parity enable used with the parity error interrupt source.

PFWE – the enable bit for power-fail interrupts sent directly into the IMP.

MRGIE – provided to allow base page links in a future development. It is not used currently and should always be zero.

MIM – the master interrupt mask which disables all interrupts when high.

INTRQM – the interrupt request enable; masks I/O interrupts when low.

FLTO – the floating point overflow interrupt source (not used).

TBGON – the ON/OFF bit for the time base generator.

PS–, MP–, SCHOD–, CRS – drive backplane lines via bus drivers. They are used as defined in the Backplane Chapter.

TBGF – the TBG flag interrupt source.

Interrupt Sources

The interrupt sources which the hardware recognizes in order of priority are as follows:

A/B fetch
TBG tick
Parity Error
Memory Violation (Memory Protect)
Slave
Power-Fail Warning
Floating Point Overflow
TBG Flag
I/O Interrupt

Parity error, memory protect, and TBG tick signal the interrupt system through pulses, therefore, they must be latched until the microcode can service them. This is done with JK flip-flops. Parity error interrupt source is qualified with PEE (parity error enable) status and ENDMRDP1+. This is then synchronized by a D flip-flop, before setting the parity error interrupt flip-flop. ENDMRDP1+ is true during the cycle after the end of a processor memory read. If the PE line on the backplane is asserted at any other time (for example following a DMA read) the processor will ignore it.

The three interrupt flip-flops can be set or cleared by the microcode through the lower four bits of the IST register (labelled "interrupt control" in the Interrupt Status section). A write to the IST register enables the 3-to-8 decoder if Y+[3] is low. Six of the outputs are used to set and clear the three flip-flops. One other bit is used to clear the microcode time-out flip-flop. These four flip-flops are cleared at power-on.

Slave (SLAVEFF+/–), and power fail (PFWFF+) remain asserted on the backplane until they are serviced. They need only be synchronized before being input to the IMP. This is done using D flip-flops.

Unimplemented instructions and privileged instruction interrupts are handled entirely by the microcode with no hardware assist.

The following table shows the action taken when writing to the lower four bits of the IST with the patterns shown on the Y-bus.

Y+[3:0]	Resulting Action
0000	Clears the Parity Error Interrupt Flip-Flop
0001	Sets the Parity Error Interrupt Flip-Flop
0010	Clears the Memory Protect Interrupt Flip-Flop
0011	Sets the Memory Protect Interrupt Flip-Flop
0100	Clears the TBG Tick Interrupt Flip-Flop
0101	Sets the TBG Tick Interrupt Flip-Flop
0110	Clears the Memory Time Out Interrupt Flip-Flop
0111	Not used

Any write to the IST register will clear the INT+ flip-flop. The spare output is not used because it corresponds to one of the priority values which could be read from the IST register. The interrupt flip-flops and INT+ must be cleared in the interrupt service microcode. The microcode is allowed to set these flip-flops for diagnostic purposes.

A read from the IST register provides the code (as listed below) of the highest priority interrupt pending. This code resides in the least significant four bits of the word that is read. The code is generated in the IMP and then latched in a 4-bit register.

The TDI bit indicates that certain interrupts (TBG flag, power fail, and I/O interrupts) are to be held off. If these interrupts are asserted, and TDI is true, then they will not cause an interrupt at the end of this instruction. This bit is cleared by FCHP or FCHB and is toggled by CMID–. TDI is generated by a JK flip-flop. The inputs to the IMP (interrupt sources) and the resultant priority codes are as follows:

IST Code	Interrupt Sources		Description
0111		ABFTCH–	A/B Fetch
1000		TBGT–	Time-Base Generator Tick
1001		PEINT–	Parity Error
1010		MPINT–	Memory Protect (Memory Violation)
1011		SLAVEFF	Slave
1100		PFWFF	Power-Fail Warning
1101		FLTO	Floating-Point Overflow
1110		TBGF	Time-Base Generator Flag Set
1111		IINTRQ	I/O Interrupt
	Masks and Enables	TDI–	Temporary Disable Interrupts
		PFWE	Power-Fail Enable
		INTRQM	I/O Interrupt Enable
		MIM	Master Enable
	Other	MABAB–	A/B Addressed this cycle
		PFTCH–	Fetch occurring

The outputs of the IMP are the four priority code bits (PPR+[0:3]), both senses of SETINTP, and the signal SETINT+ which sets the INT+ flip-flop.

IINTRQ is the I/O Interrupt Request from the I/O cards. It is synchronized twice since the backplane specification does not guarantee setup or hold times to the latches used.

The interrupt source and mask inputs are combined to form the INTP+ interrupt pending condition and the four priority lines, PPR+[0:3]. MABAB+ is asserted if the current memory access is A or B addressed. PFTCH+ is true if FCHB– or FCHP– is asserted. If either INTP+ or MABAB+ is true, and PFTCH is true, the SETINT+ output of the IMP is asserted to set the INT+ flip-flop. The priority lines and INTP+ are clocked at the rising edge of SC–.

The SETINTP– signal is used to hold off the fetch signal FTCH–. The output of the priority latch can be read back onto the BBUS field by IST in the B-field. If a parity

error interrupt is pending, or will be pending during the next cycle, the signal NOWRT– is asserted to change any memory write microorders to memory reads.

Freeze Logic

The Freeze logic halts the processor clock (PC) under certain conditions. These conditions occur when the processor does not have sufficient resources to finish some operation. For example, a freeze could get activated by microcode trying to access the T-Register before data is returned.

There are four basic conditions that can cause the processor clock to freeze. These freeze conditions are the following:

1. An attempt to read the T-Register before data has been returned from the last memory or I/O read.

2. An attempt to do a memory or I/O operation while there is still valid address/data in the memory address latch and memory data latch.

3. An attempt to execute an FCHB or FCHP microorder while a memory access is in progress.

4. An attempt to use the GIO-bus while it is busy. This bus is unique to the A400. This freeze condition is described more thoroughly in the GIO Freeze Condition section of the Bus Control description.

In all cases, freezes are transparent to the microcode.

Time Base Generator (TBG)

The Time Base Generator (TBG) circuitry provides a one PC cycle (Processor Clock) long pulse to the interrupt system every 10.00 milliseconds. It serves the following purposes:

- updating the real-time clocks
- timing points for task switching
- generation of microcode time-out interrupt

The time base generator can be turned on or off. After being turned on, the first TBG pulse will be generated 10 milliseconds later.

In operation, the TBG generates a pulse with a 10 millisecond pulse referred to as the "tick". The TBG tick (TICK–) sets the TBGT flip-flop which is the source of the TBGT interrupt.

If the TBGT flip-flop is already set, the tick (clock pulse) sets the MTO flip-flop instead. This indicates that a micocode time out has occurred. The tick also asserts the MTO– line to force the sequencer to execute the next instruction from location zero.

Thus, if microcode doesn't respond to the TBGT interrupt by clearing the TBGT flip-flop, microcode will be forced back to location zero when the second tick occurs.

The input to the TBG is the communications clock, CCLK–. It is divided down to the required clock frequencies. The communications clock pulses are counted by four 4-bit counters Q1, Q2, Q3, and Q4. The output is then counted by a fifth counter, Q5. The output of Q5 is a signal (TBGD5+) having a 10.00-millisecond period and a pulse width of 1.111 milliseconds.

The rising edge of TBGD5 clocks a "1" into the TBGQ6 flip-flop U1108. The output of this flip-flop is clocked twice by PC– into the TBGQ7+ and TICK– flip-flops U1109 and U1110 to synchronize it with PC–. TICK– then clears the TBGQ6 and TBGQ7 flip-flops (through the direct clear input) so that TICK becomes a pulse equalling one cycle of PC–.

When the TBG is turned off, Q1, Q2, Q3, Q4, and Q5 are held clear so that when TBG is turned back on, 10 milliseconds will go by before the first interrupt. The MTO flip-flop can be cleared with a write to the IST.

The IO_RST– signal provides special power-on timing to the on-board I/O circuitry. It is triggered immediately by either BPON– or ICRS+. IO_RST– will remain low for three ticks (30 milliseconds) after BPON– is released. For ICRS+, it remains low for three SC– clock cycles after ICRS+ is released.

At power-up, however, the TBG circuit is disabled, therefore, the TBG circuit must be explicitly enabled in order to generate the three ticks needed to deassert IO_RST–. Otherwise, the IO_RST– signal will remain asserted.

Processor Chip Portion of Memory Controller Circuitry

General Description

The processor chip portion of the memory controller can be split into four major sections and one minor section. The major sections are the GO–, BUSY+, VALID, and REF– generation circuitry. The minor section generates an on-chip LATCH signal equivalent to the off-chip signal.

Theory of Operation

GO– Generation

The GO– signal is generated by the processor chip to indicate that a RAS cycle should be initiated on the next rising edge of SCLK–. The GO– signal is asserted in response to a request from one of three sources: the processor, I/O, or the refresh counter.

A processor memory request is indicated by the assertion of MGO+. This signal is NANDed with SPON+ (synchronized PON), SECOND–, and MRQ– in U103 and U101 to produce CPU_GO–. SPON+ kills any spurious transfers when +5V is out of specification and MRQ– stops a processor request when I/O wants to access memory. SECOND+ stops MEMGO– from keeping GO– asserted on the next SCLK– rising edge when MEMGO– is slow in deasserting. MGO+ is the pre-buffered version of the processor chip signal that drives MEMGO– onto the backplane. MGO+ asserted timing is roughly SCLK– falling edge to falling edge.

When MRQ– is asserted in the same LHC as a processor generated MEMGO–, the processor deasserts MGO+ to stop driving MEMGO– on the backplane. Unfortunately, the loading on the backplane can cause the version of MEMGO– that the memory controller sees to generate GO– for an I/O access to be present late enough to cause an unwanted RAS assertion. The memory controller uses SMRQ+ to stop this incorrect assertion of GO–. MRQ– is synchronized with the processor chip by clocking it in the middle of the SHC with SHFT_SC– to provide SMRQ+. The sense of SMRQ+ is inverted from MRQ–. Since SMRQ+ is deasserted during the first LHC that MRQ– is asserted, it kills any GO– that would be created by a spurious MEMGO–. So, in this case, MRQ– stops the processor request, and SMRQ+ stops the backplane environment from creating a spurious memory request.

An I/O memory request for a DMA cycle is indicated by the assertion of MEMGO– and MRQ– on the backplane. The processor chip circuitry NANDs MEMGO+ to show that a memory request has been made, ALW_IO_GO+, SECOND– to make sure that a long deassertion of MEMGO– does not keep GO– asserted, and SPON+. ALW_IO_GO+ is the OR of SMRQ+ and SIAK+. SMRQ+ indicates that the request is past the I/O resolution cycle. SIAK+ indicates that the access is an interrupt acknowledge cycle. A valid I/O request produces IO_GO–.

A third signal, CHIP_GO-, can also produce a GO- assertion. This signal is generated to produce a RAS for refresh or a memory access if it collides with a refresh. If there is not a memory cycle in progress at the time a refresh request is generated, then bCHPREF+ will assert CHIP_GO-. If the refresh request is asserted in the same LHC as a memory access, then the memory access request posts a request for another GO- assertion (REFMGO_CLD-) when the refresh cycle is done. Alternatively, if a memory request is generated during a refresh when RAS is asserted, the system must wait one SCLK cycle for RAS to deassert. A latch captures this occurrence and generates a post-GO (RAS_POST+) request to generate a GO- assertion for the memory access after the refresh-generated RAS is deasserted. The requests are captured on the rising edge of SCLK-. The request they generate is asserted on the falling edge of SCLK- so that the request is stable during the clocking of the RAS flip-flop.

The timing of RAS_POST+ is easier than REFMGO_CLD- and so is described first. Assuming that a refresh cycle is already in progress, the RAS flip-flop had already been asserted off the leading edge of the SHC. During the next LHC MEMGO- is asserted to request a memory cycle. Unfortunately, RAS is already asserted. On the rising edge of SCLK- at the end of the LHC the memory request is captured along with the fact that RAS is asserted. This is done by ORing IO_GO+ and CPU_RM_COL+ to produce CPUIO_GO+ which is gated against SHFT_RAS+ (chosen because it is guaranteed to be stable during the rising edge of SCLK-, unlike RAS) to produce RAS2REQ-. RAS2REQ- is used to generate RAS_POST+. RAS is then deasserted on the same rising edge of SCLK- that the memory request was captured on. RAS_POST+ is ORed with REF_POST+ to produce POST_GO2B+ to set POST_GO+ on the falling edge of SCLK-. POST_GO+ is generated to initiate RAS on the next rising edge of SCLK-. All that remains is to clear the RAS_POST+ signal; this is done by feeding RAS_POST+ back to the K input to produce a one SCLK cycle duration on RAS_POST+.

When a refresh request and a MEMGO are both asserted during the same LHC, SCIOPGOR- is generated to set the REFMGO_CLD- on the rising edge of SCLK-. SCIOPGOR- is the NAND of bCHPREF+ to indicate a refresh cycle and CPUIO_GO+ to indicate that a MEMGO collided with the refresh. CPUIO_GO+ is the OR of IO_GO+ (a positive version of IO_GO-) and CPU_RM_COL+. CPU_RM_COL+ is a positive version of CPU_GO- that is further qualified against MDISL- to keep a boot cycle from being extended on a collision. Since bCHPREF+ lasts for only one SCLK cycle, SCIOPGOR- is asserted only during a refresh/MEMGO collision. The output of a flip-flop (REFMGO_CLD-) is NOT-ANDed with RAS+ to produce REF_POST+ after RAS has cycled to the deasserted state. Thus, when the refresh cycle RAS is done, REF_POST+ is asserted to produce POST_GO2B+. POST_GO2B+ is then clocked to produce POST_GO+ on the falling edge of SCLK-. The output of the flip-flop (REFMGO_CLD-) is then cleared when POST_GO+ is asserted on its K input during the next SCLK- rising edge.

Most importantly, GO- is produced by NOT-NORing IO_GO-, CPU_GO-, and CHIP_GO-.

As a final note, the assertion of MEMDISL- to indicate a boot memory cycle disables CPU_GO+ which is used for the refresh/MEMGO collision/interaction circuitry. This is because boot accesses do not need a valid RAS cycle.

BUSY- Generation

The assertion of IO_GO- or CPU_GO- generates STRT_BUSY-. Notice that CHIP_GO- is not included in the gate because it is asserted by a refresh request when there is no traffic on the backplane. Including CHIP_GO- in the gate would produce erroneous memory transfer handshakes.

STRT_BUSY- goes to the J-bar input of the BUSY flip-flop. This flip-flop is clocked by a special unloaded version of SC- on the rising edge. This allows BUSY- to be asserted a little earlier in the SHC than if we used a heavily loaded version of SC-.

The flip-flop produces BUSY_OUT+ which goes off-chip and is buffered to produce BUSY+ for on-chip use. The BUSY flip-flop also produces PREb_BUSY- which is also buffered to produce BUSY- for on-chip use.

BUSY_OUT+ is also received by a flip-flop which is clocked by SC+ at the end of the SHC to produce PREb_SECND+ and PREb_SECND-. PREb_SECND- is used to control VALID generation for boot memory accesses. Both outputs of the flip-flop are buffered to produce SECOND+ and SECOND- for on-chip use.

BUSY_OUT+ generates STRT_LTCH+ on the rising edge of SHFT_SC- which is a delayed version of SC-. STRT_LTCH+ provides the assertion of LATCH- and LATCH+. PREb_SECND+ carries the assertion of LATCH through the end of the memory access. LATCH+ and LATCH- are used on-chip to latch memory access information early in the cycle and hold it through the end.

The BUSY flip-flop is cleared by the assertion of END_BUSY+ on the K input. END_BUSY is generated when SPON has been deasserted or CHIP_VLD+ has been asserted. SPON+ is NOT-ANDed with RAS+ to produce PONCLS+. PONCLS+ is thus asserted when the supply voltages are out of specification and the board is not in the middle of a RAS cycle. PONCLS+ is clocked by SC+ to produce PON_ENDMC+. This signal is ORed with ENDMC+ to produce the magical END_BUSY+.

ENDMC+ provides for the normal deassertion of BUSY. ENDMC+ is generated on the rising edge of SC+ when CHIP_VLD+ is present. CHIP_VLD+ is asserted during the second to last SHC and lasts one SCLK cycle through the last LHC to be deasserted during the last SHC.

VALID- Generation

A memory cycle can last from two to four SCLK cycles. VALID- on the backplane is the signal that indicates the memory cycle is about to end. The generation of

VALID– is provided on the PC board under control of SET_VALID+. SET_VALID+ is generated in the processor chip. SET_VALID+ is connected to the D input of the VALID D-type flip-flop on the board.

The signals that control the assertion/deassertion of SET_VALID+ are split into four groups based on the sources of the memory accesses. The four sources of memory accesses are: I/O, the processor to main memory, the processor to boot memory, and a "Post" generated access due to a refresh/MEMGO interaction. These sources produce an assertion on IO_VLD+, CPU_VLD+, BOOT_VLD+, or POST_VLD+, respectively, to generate SET_VALID+.

IO_VLD+ is the result of NOT-ANDing SHFT_RAS+, IO_GO+, bCHPREF+, and END_BUSY+. IO_GO+ starts VALID unless a refresh cycle is in progress. bCHPREF+ stops the assertion of VALID if I/O requests memory during the LHC that bCHPREF+ is asserted. SHFT_RAS+ stops the assertion of VALID if I/O requests memory on the next LHC after bCHPREF+ was asserted. END_BUSY+ kills the SET_VALID+ signal well before the clock signal for the VALID flip-flop on the board or if PON is deasserted. END_BUSY+ provides this function for IO_VLD+ as well as CPU_VLD+, BOOT_VLD+, and POST_VLD+.

CPU_VLD+ is the result of NOT-ANDing SHFT_RAS+, CPU_GO+, bCHPREF+, MEMDISL– and END_BUSY+. CPU_GO+ starts VALID unless a refresh cycle is in progress or boot memory cycle. MEMDISL– kills CPU_VLD+ on a boot memory access while SHFT_RAS+, bCHPREF+, and END_BUSY+ provide the same functions for CPU_VLD+ as they do for IO_VLD+.

BOOT_VLD+ is the NOT-AND of END_BUSY+, BOOT_STRCH+, MEMDISL–, and PREb_SECND–. MEMDISL– starts VALID after the assertion of PREb_SECND– on a normal boot memory access. PREb_SECND– holds the assertion of SET_VALID+ until the first clock has passed the VALID flip-flop. This pushes the assertion of VALID to stretch the memory access from two cycles to three which gives more time to access the VCP PROMs in boot memory space. BOOT_STRCH+ stretches the access out to four SCLK cycles when the boot memory request is initiated on the same LHC as bCHPREF+. When this occurs, PREb_SECND+ stops the assertion of VALID on the second SCLK cycle while bCHPREF+ propagates through. SET_VALID+ is kept from being asserted on the second SHC after the assertion of MEMGO because BOOT_STRCH+ is not deasserted until the end of the second SHC so that VALID is pushed past the third LHC. SET_VALID+ is then asserted on the third SHC to produce the assertion of VALID for the fourth LHC. This allows the use of an external refresh address counter if so desired instead of CAS-before-RAS refresh because there is enough time to drive the refresh address and get off of the address lines so that the PROM address can be placed on those lines for a boot PROM access.

POST_VLD+ is the NOT-AND of POST_GO–, bCHPREF+, SHFT_RAS+, and END_BUSY+. POST_GO– generates the assertion of SET_VALID+ while the other signals provide the same functionality as described earlier.

POST_VLD+, CPU_VLD+, IO_VLD+, and BOOT_VLD+ are ORed to produce SET_VALID+. SET_VALID+ clocks CHIP_VLD+ on the rising edge of SHFT_SC–.

It also goes off-chip to control VALID- generation on the board. CHIP_VLD+ is used to generate ENDMC+ and for use by the memory and I/O state machines in the processor section.

Refresh Circuitry

The memory arrays supported by the A400 use dynamic RAM. The nature of these devices is such that every row in each memory chip must be refreshed on a regular basis or the data will be lost. Fortunately, the 256k bit memory chips used by the A400 board and the 64k bit parts used in the supported memory array cards require the same refresh rates. Both parts need to have 256 rows accessed every 4 milliseconds (note that the 256k parts only count through 256 rows even though the 9 RAS bits pick one of 512 rows). In order to ensure that each row is accessed at least once every 4 milliseconds, a refresh counter schedules a "refresh cycle" approximately every 15.6 microseconds.

In order to time the refresh cycles, the processor chip has a counter that schedules a refresh cycle every 230 CCLK cycles, or 15.598 µs. The refresh is guaranteed to occur within 4 clock cycles. The counter schedules a refresh request and then rolls over independent of when the refresh cycle actually occurs. Thus, the count value is not dependent on the refresh cycle-to-cycle time, but on the total time it takes to count through 256 requests minus 4 SCLK cycles. Each row will be accessed by a refresh cycle at least every 3.994 µs as determined by the following equation:

$$(1/(14.7456\text{MHz} - (.000025 * 14.7456\text{MHz})) * 230 * 256) + (4 * 250\text{ns}) = 3.994\ \mu\text{s}$$

Note that a refresh counter count of 230 allows SCLK to slow down to 1.7 µs before the refresh time goes out of specification, or alternatively, CCLK to drift .1% instead of .0025% of specification. The refresh rate is 5% less than it would be if timed on a refresh cycle-by-cycle basis.

The refresh counter is a synchronous counter driven by CCLK divided by two. The counter counts from 0 to 114 decimal (1110010B) to create 115 states. At 114 decimal the counter rolls over to zero. Since CCLK is divided by two before clocking the counter, the counter produces a zero every 230 CCLK cycles.

When the rollover value of 114 decimal is produced by the refresh counter it resets the counter and is clocked into a refresh request flip-flop. The refresh request flip-flop is clocked off of CCLK. To synchronize the refresh request to SCLK, it is double clocked by two flip-flops. These flip-flops have two stages which are logically connected when the clock is high and disconnected when the clock is low. A full clock cycle (which allows the clock to go low and thus disconnect the oscillations of the first stage from the second stage) between the two flip-flops will provide the greatest odds of stopping any ringing produced by hold time violations. The external refresh request signal should therefore be clean.

When there is no contention for memory, the refresh request sets up at the input to two flip-flops to be clocked on the falling edge of SC-. The output of one flip-flop is CHPREF+, a one SC- cycle refresh command which stays on the chip. The output of

the other flip-flop is REF–, a two SC– cycle signal that drives the off-chip circuitry. REF– is stretched from one cycle to two. The two flip-flops are clocked on the falling edge of SC– so that MEMGO requests for memory can reliably be over-ridden.

When there are no memory requests present, the refresh request immediately starts a refresh cycle. If a refresh request is generated and then a MEMGO request is generated in the same LHC, the MEMGO request is latched and held off while the refresh request is executed. If a refresh request occurs while a memory cycle is in progress, then the refresh request it kept from passing through by gating the request against BUSY– and RAS–. BUSY– holds off the refresh request during the access and RAS– keeps the refresh request from occuring until the RAS flip-flop has cleared.

Processor Chip I/O Control

The processor chip transfers information to and from the PC board via several buses. In addition, the processor chip controls many of the external (board resident) devices that also make use of these buses. To help in understanding the functionality and the inter-relationships of the bus control logic and the A400 board, a series of timing diagrams are supplied in Appendix C. Refer to the timing diagrams when reading the following material. The major buses and their functions that enter and exit the processor chip are described in Table 3-19.

The control store address and data bus are used exclusively in the processor chip by the microsequencer logic. Refer to the Microsequencer section for details on the usage and control of the CSAL-bus and CSD-bus.

The following sections describe in some detail the usage, control, and timing considerations of the major buses. The control of the buses and the I/O pad control logic does not constitute much circuitry but it is the heart of the processor chip's interface to the board.

The descriptions of the processor chip buses and their control relies heavily on signals that are generated outside of the specific block of logic being discussed. Therefore, a glossary of signals, their meanings, and relative timings (if relevant) is included at the end of this section.

Bus Control Functional Description

This following subsections are scenarios describing the functionality required for each type of bus cycle. These scenarios will aid in the understanding of the detailed description of the logic of the bus control that follows. The scenarios described are as follows:

- Processor Main Memory Access
- DMA Memory Access
- Interrupt Acknowledge Access
- Boot Ram Access
- Boot ROM Access
- I/O Handshake Cycle

Table 3-19. Processor Chip Major Buses

Bus Name	Mnemonic	Width	Usage
General Purpose I/O Bus (bidirectional)	GIO	16	logical address out of processor chip boot RAM data in/out of processor chip map RAM data in/out of processor chip central interrupt latch (CIL) data into processor chip switch register data into processor chip LED data out of processor chip output of map RAMs: the high 14 bits of physical address plus read and write protect bits lower 10-bits of the parity error address register into processor chip external (not in processor chip) SRIN register (SRIN[6:15]) data to/from processor chip
Data Bus (bidirectional)	D	16	main memory data to/from processor chip and to/from backplane to on-board memory boot ROM data to processor chip and to backplane boot RAM data (both read and write) from processor chip to backplane I/O read & write data to/from processor chip output of all ones for non-existent memory reads and memory protect violation reads
MAP Bus (output only)	MAP	5	AE-bus outputs from processor chip to map/boot RAM address inputs for processor main memory accesses logical address bits 5-9 to map/boot RAM address inputs for boot RAM access processor chip outputs zeros for interrupt acknowledge cycles and DMA self-configuration cycles to map/boot RAM address inputs MPAR bits 5-9 from processor chip to map/boot RAM address inputs for map reads and writes
Page Bus (output only)	PG	5	logical address bits 10-14 to map/boot RAM address inputs for main memory accesses logical address bits 0-4 to map/boot RAM address inputs for boot RAM accesses MPAR bits 0-4 from processor chip to map/boot RAM address inputs for map reads and writes
Control Store Address Bus (output only)	CSAL	14	processor chip outputs control store address for addressing control store RAM/ROM
Control Store Data Bus (input only)	CSD	32	processor chip input for microinstructions coming from control store RAM/ROM

Processor Main Memory Access

When a main memory access is requested by the micromachine, the logical address for the access is available from the AOUT latches. The memory cycle is indicated by the MEMRQ signal which is the OR of all memory accessing microorders. Since the A- and B-Registers are memory mapped, a micromachine memory request will only initiate a memory access if it is NOT an A or B address. Also, if the memory access is a write, the write data is available from the DOUT latch.

At the beginning of a processor memory cycle, the logical address from the AOUT latch is output over the GIO-bus pads to the board. The lower 10 bits of the logical address are latched and driven onto the backplane as AB+[0:9]. The upper 4 bits are not used but indicate the logical page number of the access. The fifteenth bit is also not used but indicates read/write protection. After the lower 10 bits of the logical address are latched, the GIO-bus pad outputs are tri-stated.

Concurrently with the activity on the GIO-bus, the processor chip MAP-bus and PG-bus output the map/boot RAM address. For this type of cycle the RAMs are being used to "map" logical addresses into physical ones. The value presented on the PG-bus represents the page number of the logical address, that is, AOUT+[10:14]. The value presented on the MAP-bus selects the map set being used by the processor and originates in the AEOUT latch. An additional address line is supplied by the processor chip (BOOT–) to differentiate map RAM and boot RAM accesses. In the case of a main memory access the map RAMs are selected. The output enable for the map RAMs is timed so that contention is avoided with the logical address being driven on the GIO-bus earlier in the cycle. After the processor chip's GIO-bus drivers are disabled, the RAMs are output enabled. After the RAM access time, the RAM outputs are latched for use as the upper 14 bits of the physical address. The lower 10 bits of the physical address are taken directly from the latched ten logical address bits discussed above. Once the outputs of the map RAMs have been latched, the GIO-bus is free for other uses. The MAP- and PG-bus values are driven by transceivers onto the backplane AE-bus and onto the upper bits of the backplane logical address bus (AB+[10:14]).

If the memory cycle is a write, the DOUT latch data is driven by the processor chip onto the PC board D-bus and then onto the backplane data bus by the D-bus transceivers/latches. If the write is to the on-board memory array, the processor chip will internally latch the write data so that it remains valid on the D-bus until the write cycle is complete.

If the memory cycle is a read, the data read is received by the processor chip over the D-bus and is stored in the T-Register. If the read was for an instruction fetch then the data is also stored in the CT register. For on-board memory reads, the data is placed onto the D-bus and also driven out onto the backplane. To relieve the memory RAMs from holding their outputs valid until the end of the memory cycle, the D-bus transceiver/latches internally latch the D-bus value and then drive the latched value out onto the backplane. If the read is from off-board memory (that is, from a memory array card), the D-bus transceivers drive the backplane data onto the D-bus (the latch is kept transparent).

DMA Memory Access

A DMA memory access is indicated by the assertion of MRQ on the backplane. When asserted, the processor will finish a memory access in progress but will refrain from initiating any new cycles (ignoring the use of CPUTURN). When the DMA memory cycle is initiated, I/O will drive the backplane address and address extension busses with the appropriate value for the access. The value on the address bus is equivalent to the processor's logical address. The I/O address extension bus value is used by I/O the same way the processor uses the AEOUT register value, which is to select a map set for use in the logical-to-physical address mapping.

For the DMA access, the MAP-bus and PG-bus transceivers drive the backplane addresses onto the board's MAP- and PG-buses, respectively. The MAP-bus receives the backplane AE-bus value and the PG-bus receives the page bits from the backplane logical address bus (AB+[10:14]). As was the case for the processor memory access, the map RAMs are output enabled and the map outputs latched. Again, after the physical address is captured, the GIO-bus is free for use.

If a DMA self-configuration cycle is indicated by the assertion of SELFC–, the backplane AE-bus value is ignored. In this case, the processor chip will force all zeros onto the MAP-bus to force the access to map set 0.

For all DMA writes, regardless of which array is being written, the backplane data bus is latched and driven onto the board's D-bus by the D-bus transceiver/latches. For a DMA read of on-board memory, these same devices are used to latch and drive the on-board DRAM output data onto the backplane data bus. The latch of the transceiver is used to relieve the need to maintain the DRAM outputs to the end of the cycle.

Interrupt Acknowledge Access

In response to the assertion of INTRQ by an I/O card, the processor will respond with the assertion of IAK (this is a result of the microorder IFCH). Then, I/O will do a memory cycle. As far as the bus control logic is concerned, the access is nearly identical to a self-configured DMA read access. The difference is that the micromachine considers the cycle to be a micromachine read cycle. This is the only case of the micromachine doing a memory read without providing the memory address itself. Along with the IAK address, I/O also asserts SELFC–. The bus control logic uses the assertion of SELFC to force the MAP-bus to all zeros to select map set 0. The read data is captured by the processor chip off of the board's D-bus and is stored in the T-Register.

Boot RAM Access

The boot RAM and the map RAM physically share the same RAM chips. This is possible since boot memory accesses are unmapped. Thus, the map RAM is not used during a Boot RAM access and the map RAM would otherwise be sitting idle during a boot RAM access.

A boot RAM access starts out the same as a processor memory access. The logical address is driven out onto the GIO-bus and latched. The boot RAM address must consist of the lower 10 bits of the logical address. This corresponds to an address space of 1k words. The lower 5 bits of this address (AOUT+[0:4]) are driven onto the PG-bus, and the upper 5 bits (AOUT+[5:9]) are driven onto the MAP-bus. The signal BOOT- is driven by the processor chip to select and access the boot memory portion of the map/boot RAMs. For boot RAM writes, the write data is driven from the DOUT register onto the board GIO-bus to the I/O pins of the map/boot RAMs. The write occurs soon after the write data is valid.

For boot RAM reads, the boot RAM data is read into the processor chip off of the GIO-bus. In order for boot RAM accesses to provide visibility to the read/write data and to free the GIO-bus for other uses, the following is done: On boot RAM writes, the write data is simultaneously driven onto the GIO-bus and the D-bus. The D-bus data is then driven onto the backplane. For boot RAM reads, the boot RAM output data is read off of the GIO-bus and then latched internal to the processor chip. The latched data is then driven onto the D-bus and again driven onto the backplane. However, the micromachine reads the D-bus data for storage into the T/CT registers at the end of the read cycle. This allows the boot RAM reads and writes to occur in one cycle instead of three, it frees the GIO-bus at about the same time as on a mapped access, and it allows all memory or I/O read data to be received by the processor chip over the board D-bus.

Since the PG- and MAP-bus do not contain the usual components of a logical address, the observed address on the backplane for a boot RAM address is slightly convoluted. The lower 10 bits of the backplane address bus will have the actual boot RAM address accessed. The backplane address bus bits 10:14 as well as the AE-bus values are ignored.

Boot ROM Access

Like a boot RAM access, a boot ROM access is unmapped. The ROMs reside on the D-bus and are read-only devices. Therefore, a boot ROM access is simple.

As in all processor memory accesses, the logical address is driven out early in the cycle onto the GIO-bus and latched. At this point the GIO-bus is considered free for use. The address presented to the boot ROMs is the lower 13 bits of the processor's logical address. The boot ROM address is supplied in part from the 10 bits of logical address latched from the GIO-bus. The actual address used is a version of this latched address received off of the backplane. The upper 3 bits are latched off the PG-bus. For a boot ROM access, the PG-bus contains the value of AOUT+[10:14]. The boot ROM read data is output onto the D-bus where it is driven onto the backplane and into the processor chip.

I/O Handshake Cycles

In response to the assertion of IORQ from an I/O card, the processor will execute a RDIO or WRIO microorder requesting an I/O read or I/O write handshake cycle, respectively. In response to the IORQ, the processor chip asserts IOGO on the backplane. For an I/O read, in the third cycle after IOGO is asserted (the cycle after IORQ deasserts), valid read data is on the backplane. During this cycle, the D-bus transceivers drive the backplane data onto the D-bus and into the processor chip. The data is captured in the T-Register. For an I/O write cycle, the processor will drive DOUT latch data onto the D-bus to be driven onto the backplane.

General Purpose I/O (GIO) Bus

The general purpose I/O bus (or GIO-bus) is a bidirectional bus used for several purposes. Like all bidirectional I/O signals or buses in the processor chip, the GIO-bus is composed of a separate output bus, the GO-bus, and an input bus, the GI-bus.

GO-bus

The GO-bus is responsible for providing the logical address of a processor memory accesses to the board for driving out onto the backplane. Additionally, the map/boot RAM write data, the LED display data, and the off-chip SRIN register write data are all placed on the GO-bus to be driven onto the board's GIO-bus.

The GO source is selected by 4-to-1 multiplexers. The multiplexer outputs are selected from one of three sources:

AOUT for logical address output during a boot or main memory access
Y for LED display or off-chip SRIN register writes
DOUT for boot RAM writes

The organization of the A400 board is such that both the logical and physical (mapped) address both need to appear at one time or another on the board's GIO-bus. In order for this to happen, all of the addresses must be provided when they are needed and bus contention must be avoided.

The correct GO data must be provided at the correct time. Figure C-1 in Appendix C indicates at what point in a memory access the processor chip is responsible for driving the logical address onto the GIO-bus and when the map/boot RAMs will be driving the GIO-bus. Basically, prior to the SC-↓ that would assert MEMGO, the GIO-bus is driven by the processor chip with the logical address. At SC-↓, the lower 10 bits of the logical address are latched into a 10-bit latch (AMD29841) on the board. At the subsequent falling edge of the shifted SC signal (SHFT_SC-↓), the map/boot RAMs will be enabled to drive the GIO-bus. The off-chip micromachine registers (that is, the LED display and off-chip SRIN registers) are accessed only during the LHC of PC. A freeze condition handles the case where the GIO-bus is

busy and an off-chip register must be written. By waiting until the LHC of PC, it is ensured that the freeze condition has concluded and therefore the bus must be free.

With all this in mind, the design of the GO multiplexer select circuitry can be explained. The select logic takes advantage of the fact that during the SHC of SHFT_SC the only thing ever required to be driven onto the GIO-bus by the processor chip is the logical address from the AOUT latch. For this reason SHFT_SC+ is applied to two NOR gates. This forces AOUT to be selected during the SHC of SHFT_SC+. RAMWE- is used to qualify SHFT_SC to ensure that the GIO-bus does not change state prematurely during a boot RAM write. Boot RAM writes conclude at about the same time the SHC of SHFT_SC begins. The signal, bLADR-, is included to prevent a race condition with the on-board address latch that resides on the board's GIO-bus. The signal is the LADR- signal received from the input of LADR's bidirectional I/O pad. LADR is ideally timed to occur during the SHC of SHFT_SC. By using bLADR to maintain the GIO multiplexer select lines, the GIO-bus is prevented from changing state until after the GIO-bus value is latched on the board.

The AOUT latch is a transparent latch that is latched by SHFT_SC- or MRP-. The two latch conditions allow the addresses generated by the processor chip to remain valid despite micromachine freezes and queued-up memory accesses. When a processor memory access is to begin, the address is driven directly into the address latches on the board as soon as the address becomes valid on the chip. After the SHFT_SC-↓, the select inputs of the multiplexers select the Y-bus source. If a boot RAM access is indicated by the assertion of MEMDISL along with MGO and the address is in the boot RAM range (that is, A13 NOR A14 indicated by LBRAM_AD+), then the DOUT source is selected. Boot RAM writes occur on the SHFT_SC+↓. RAM data hold time (0ns spec.) is guaranteed by the fact that the earliest that either the data, GIO multiplexer select lines, or the GIO output enables can change is a couple of gate delays from SHFT_SC-↑. SHFT_SC- is an inverted version of SHFT_SC+.

The output enable for the GO-bus output pads is called OEGIO-. The GIO-bus is output enabled under the following circumstances:

1. during the SHC of SHFT_SC when the processor is requesting a backplane cycle and the backplane is available. This implies that BUSY is not asserted and neither a DMA or IAK cycle are imminent. A processor memory request is determined by (MEMAC+ + MRP+) when RD_MAP+ is not asserted. RD_MAP eliminates enabling the GIO-bus during special map read cycles. If a processor MEMGO is intended, then the GIO-bus will get the logical address from AOUT. The timing of the output enable is governed by the SHC of SHFT_SC. The bus must be driven past the SC-↓ on which the lower 10 bits of the address will be latched (by LADR-). After being driven onto the board, LADR- is received as bLADR-. This signal is then used to ensure the GIO output enable lasts beyond LADR-↑ on the board. The standard memory access condition is identified by the signal DRIVE_LOGA+ ("drive logical address").

2. during the LHC of PC when an off-chip register will be written. An off-chip register write is indicated by the assertion of lyLSR- (an LED display register write), lyMAP- (a MAP register is to be written within the map/boot RAM), or by lyOFFC_SRIN- (a write to the SRIN register file where N indexes to a register not present in the processor chip). The timing for the output enable corresponds to the LHC of PC. Since the SHC of PC is lengthened indefinitely during a micromachine freeze, the occurrence of the LHC of PC ensures that there is no longer a freeze condition present. For the case of any microorder that requires the GIO-bus (such as an off-chip register write), a freeze is generated whenever the GIO-bus is busy with the mapping of a memory access. During this enable condition, the GO-bus contains Y-bus data. The off-chip write condition is identified by the signal OFFC_WRITE+ ("off-chip write").

3. during the period between the assertion of the processor's MEMGO (MGO-) and the assertion of LATCH on a boot RAM write. The indication of a boot RAM write is provided by the simultaneous assertions of MEMDISL-, WE-, and LBRAM_AD- (the deassertion of LBROM_AD+). The timing of the GO-bus output enable for the boot RAM write condition is that the bus enables with MGO- and disables with the assertion of LATCH. The actual boot RAM write occurs at the SHFT_SC+↓ during BUSY just before SECOND asserts. For this condition, the GO-bus contains data from the DOUT register. The boot RAM write condition is identified by the signal BRAM_WRITE+. If a DMA cycle is requested, the boot RAM write will be aborted. The GIO-bus drivers tristate when the MEMDISL- signal deasserts due to the occurrence of MRQ.

The equations for generating OEGIO- are as follows:

```
DRIVE_LOGA+   = (SIAK + SMRQ)' * (MEMAC + MRP) * SHFT_SC- * BUSY-
                    * YOGI_OE+ * RD_MAP-

OFFC_WRITE+   = (lyMAP + lyOFFC_SRIN + lyLSR) * PC- * YOGI_OE-

BRAM_WRITE+   = MEMDISL+ * LBROM_AD- * LATCH- * WE+ * MGO+
                    * YOGI_OE+

qLADR         = bLADR + preBPON- + YOGIOE-

OEGIO-        = -(RAMOE- * (DRIVE_LOGA + qLADR- + OFFC_WRITE
                    + BRAM_WRITE))
```

The upper 6 bits of the GO-bus (GO+[10:15]) are output enabled for one additional case other than those described above. The assertion of the ePER1b- signal indicates that the micromachine wants to enable the lower 16 bits of address from the last parity error onto the B-bus. The organization of the processor chip and of the board have permitted the upper 14 bits of the physical (mapped) address of a parity error to be latched on the chip. This reduces the on-board chip count by only requiring that the board maintain the lower 10 bits of the PER. When the PER low word is read, 10 bits come from the board and 6 bits come from internal to the processor chip. A problem arises in that the upper 6 bits of the GIO-bus would be floating because only a 10-bit register is being enabled onto it. By output enabling only the upper 6 bits of the GO-bus, the floating condition on the GI-bus input pads is avoided. The signal OEGIO_HI6- is the special enable for GO-bus bits 10 through 15.

The GI-bus

The GI-bus in the processor chip is the input bus from the GIO-bus on the board. The GI-bus is enabled whenever something is to be read off of the GIO-bus. The processor chip uses the GI-bus as a source for data read from the boot/map RAMs, the CIL, the switch register, the lower 10 bits of the parity error register, and for off-chip SRIN registers. It also serves to supply the upper 14 bits of physical address (map outputs) for storage into PER1[10:15] and PER2[0:7] in the event of a parity error.

The GI-bus is routed directly to any register or buffer that requires the data on the GI-bus. On boot RAM reads, the GI-bus is driven out onto the board D-bus to be output onto the backplane for observation of boot RAM activity. This is done whenever boot RAM is accessed, not just on boot RAM reads. For map reads, the GI-bus is input into the F-bus multiplexer of the ALU. This is done to avoid the time penalty of propagating the map data through the entire ALU when the desired result is to just store the map data into a micromachine register. The F-bus multiplexer is the recipient of the map data for the following reasons:

1. The major bottleneck of the ALU is avoided and map read data makes it onto the chip and becomes valid on the Y-bus with sufficient set-up time before PC–↑.
2. The Y-bus does not have to be a tristate bus. This would be the case if map data were driven directly onto the Y-bus.
3. Because bypassing the ALU implies that no ALU operation will occur when MAP is in the BBUS-field, it is safe to send the data onto the F-bus because the Y-bus shifter defaults to pass it directly. Even though it is guaranteed that no ALU operation will occur to the map data, it is possible to shift the map data if desired.

The GI-bus is fed into the 14-bit physical address register in the processor chip that is clocked by LATCH+. This register holds the mapped part of the physical address in the case that a parity error is detected. At LATCH+↑, the GIO-bus contains the map/boot RAM output. Also note that the map/boot RAMs are disabled by an internally generated version of LATCH. Calculations show the minimum set-up time provided to the physical address register is 7 nanoseconds. Hold time provided is 9.45 nanoseconds.

Worst-case analysis has the map RAM data available on the board at 35 nanoseconds after the board's SC+↓. The best-case delay of SHFT_SC+ from SC+ is 40 nanoseconds. SC+ is a buffered and inverted version of SCLK– on the backplane. The generation of the processor chip's internal LATCH+ signal requires SHFT_SC+ to propagate onto the chip, get inverted, clock a flip-flop, and be driven through a super-buffer. Best case this path takes 49.5 nanoseconds after the board's SC+↓. The map RAM output data takes approximately 7 nanoseconds to make it into the chip and to the inputs of the register. This provides for a register set-up time of 7.5 nanoseconds [(49.5–(35+7)]. The required set-up time of the register is 6.5 nanoseconds.

The hold time calculation yields the map RAM outputs tristating at a minimum of 7.15 nanoseconds after the assertion of LATCH–. LATCH– and LATCH+ (which

clocks the register) are generated in parallel and have nearly identical timing. The data does not change at the register inputs for at least 2.3 nanoseconds afterwards. This provides the 9.4-nanosecond [7.15 + 2.3] hold time. The required hold time of the register is 8.0 nanoseconds.

Both these calculations yield times that are close to the minimum required by the physical address register. In both cases, the actual circuit performance has significantly more margin because the bus hold time due to capacitance is not included and the map RAM outputs turn-off instantly. Additionally, the calculations used both best-case and worst-case numbers for gates in the processor chip. This is not likely to occur since intra-chip delays should track pretty closely since they are mainly a function of processing.

The registers for the upper 6 bits (PER1[10:15]) of PER1 and the lower 8 bits (PER2[0:7]) of PER2 sit on the outputs of the physical address register. On the rising edge of PE+, the parity error registers will clock in the stored physical address.

The GI-bus also is enabled to drive the lower 10 bits of the B-bus when SRIN is in the BBUS-field and N = 1 (a PER1 read). Likewise when SRIN is in the BBUS-field and N = 3 (a CIL read), GI+[8:12] is enabled to drive the lower 5 bits of the B-bus. When a map register or off-chip SRIN register (N > 5) is read, the GI-bus will drive the entire B-bus. The GI-bus also drives the entire B-bus for switch register reads (SR in the BBUS-field).

External GIO-bus Control

The processor chip controls all devices resident on the board which can source data onto the GIO-bus. This has been done to consolidate the bus control circuitry into one area. The processor chip controls the boot/map RAMs, the CIL register, the lower 10 bits of the PER, and the SR (switch) register.

The boot/map RAM control is provided by two signals, RAMOE– and RAMWE–. RAMOE– is the output enable for the map/boot RAMs. RAMWE– is the write enable for the map/boot RAMs. Map RAM reads and writes are discussed in the following paragraphs.

Map RAM Reads:

Differentiation between boot and map RAM access is provided by the signal BRAM_AC– which is driven onto the board as BOOT–. The default condition for the map/boot RAMs is tristate. The RAMs are output enabled whenever one of the following occurs:

1. a DMA cycle is imminent but memory is not yet busy (MRQ asserted, BUSY deasserted)
2. the processor wants to do a memory access (MGO+ asserted)
3. a map RAM access is desired (RD_MAP+ asserted)

The timing of RAMOE- is controlled by the LHC of SHFT_SC- and the assertion of LATCH in the chip. The output of the map/boot RAMs is captured into the board's physical address latches on LATCH-↓. LATCH- is generated from SHFT_SC on the board. The latches have a hold time of 3 nanoseconds. Their hold time requirement is easily satisfied since SHFT_SC+ must get on-chip, be inverted, create the chip's internal version of LATCH, be gated to become RAMOE-, and then driven back off-chip to the RAM OE- input.

Due to the timing of the map/boot RAM write enable signal, RAMWE-, it cannot be relied on to tristate the RAMs when write data must be driven onto the GIO-bus. For this reason, RAMOE- is held deasserted during a boot RAM write.

The actual signals that generate RAMOE- are shown in the following equation (the signals and their function/meaning are also listed):

RAMOE- = (OEGIO- * IO_MGO+ * SECOND- * enRAMOE+)
+ (OEGIO- * NOT_BRW * MGO+ * enRAMOE+) + (OEGIO- * RD_MAP+)

MGO+ is the processor-generated MEMGO, one cycle from SC-↓ to SC-↓. It is deasserted on the occurrence of MRQ.

NOT_BRW+ indicates that the current memory cycle cannot be a boot RAM write. The RAMWE- does not assert until the SHC when BUSY asserts. The RAM write data will be driven onto the GIO-bus starting at the SHFT_SC-↓ during MGO+ until the assertion of SECOND. This means that RAMOE- must not be asserted so as to avoid contention with the boot RAM write data and the map/boot RAM outputs. This signal ensures that RAMOE does not assert during a boot RAM write. NOT_BRW+ = (WE- + LBROM_AD+ + MEMDISL-)

IO_MGO+ (SMRQ + SIAK) indicates that a non-processor initiated MEMGO is eminent, that is, a DMA cycle or an IAK cycle.

RD_MAP+ indicates when a map read is requested.

OEGIO- is included to ensure that the processor chip GIO-bus drivers are tristate before the map/boot RAM is enabled.

SECOND- ensures that the RAMs are only output enabled for mapping during the LHC of SHFT_SC+ when MEMGO is asserted.

enRAMOE+ is a timing signal that asserts during the LHC of SHFT_SC+ and lasts until LATCH-↑.

The entire logical address (AOUT+[0:15]) is available on the board's GIO-bus during the SHC of SHFT_SC at the start of a processor memory access. The board makes use of this and latches the lower 10 bits of the address into a 29841 10-bit latch. The latched address is needed to drive the unmapped portion of the backplane address bus (AB[0:9]). The latch is normally held latched, by LADR- (DRIVE_LOGA+ * SC+). Only during the overlap of DRIVE_LOGA+ (during SHC of SHFT_SC) and the LHC of SC is the board AB+[0:9] latch opened. At the falling edge of SHFT_SC when LADR- reasserts, the logical address is latched off of the GIO-bus prior to the GIO-bus changing and the map RAMs enabling.

The latch is output enabled by the signal OEAD–. The generation of OEAD is covered in the section on External MAP-bus Control. Basically, OEAD is asserted unless I/O requires the backplane address bus as is the case for interrupt acknowledge and DMA cycles.

The signal RD_MAP is a complicated signal and requires some explanation. The reason there is a problem on map reads (MAP in the BBUS-field) is that there are cases when it is desired to read a map register and store it to memory in the same cycle. The macroinstruction STMP uses this approach. The microcode might look like: wrp := map.

Typically, all micromachine registers (that is, the map, SR, CIL, and PER1) that reside on the board's GIO-bus are read (output enabled) during the LHC of PC. There is a freeze condition that causes the SHC of PC to be extended if the GIO-bus is in use. The LHC of PC starts only when the GIO-bus is available. This eliminates GIO-bus contention when the map/boot RAMs are being used for memory address mapping. Simply gating the map/boot RAM enable with PC is not appropriate for the "wrp := map" case since the map read must occur during a micromachine freeze condition. However, the write cannot start until the map data is available and the freeze goes away.

On the other hand, if the map data is not needed for the current memory access then the memory access is free to start and the micromachine freezes until the map read is complete.

The two types of map reads are: one that needs to occur prior to a memory access and one that yields to a memory access. These are differentiated by the signal SPCL_WR2B+. This signal identifies the particular instance of a microinstruction that writes map read data to memory in which the memory write occurs the same cycle (if something does not prevent it). Note that a freeze occurs in this situation because the GIO-bus is needed at the same time a memory access needs it.

The generation of the SPCL_WR2B+ signal involves many conditions that must be satisfied to identify this special occurrence. All the input signals must be low (logic 0) in order for SPCL_WR2B+ to assert. SPCL_WR2B+ is inverted and then gated with eMAPb– and SC– to create SPCL_WRITE–. This signal is used to ensure that the DOUT register latches the map data being read during its assertion. On any standard memory write cycle, the DOUT latch "wants to" open up at the end of the PC cycle (at the assertion of LC+). This would be disastrous in the case of the special map-read/memory-write in which the DOUT latch would have just captured the map read data. To prevent this, the SCND_CYCLE signal is reclocked on SHFT_SC–↑ (to avoid a race condition with LC+) and fed to the DOUT latch gating logic as SPCLW_DIS–. This prevents the DOUT latch from opening at least through the end of the special map read microcycle. After the SC–↑ that corresponds with the end of the cycle, the memory write and its data is handled by the Memory and I/O State Machine in its normal fashion.

The actual signals that generate SPCL_WR2B+ are shown in the following equation (the signals and there function/meaning are also listed):

```
SPCL_WR2B+ = (NONGIO_FRZ- * GIO_FREEZE * IO_MGO- * MEMRQ
                          * MABAB- * MEMWR)
```

NONGIO_FRZ is the signal used to ensure that the freeze is due to the need for the GIO-bus and not one of the other freeze conditions. This signal is the OR of all other freeze conditions other than the GIO freeze.

GIO_FREEZE+ identifies that the micromachine is frozen. If GIO_FREEZE is asserted and NONGIO_FRZ is not asserted, then the freeze is due to the need for the GIO-bus.

MEMRQ+ indicates that a memory request has been identified in this microcycle.

MABAB– indicates that the request was not to the A- or B-Register so that a memory cycle is really indicated by the assertion of MEMRQ–.

MEMWR+ indicates that the cycle being requested is actually a memory write.

IO_MGO– indicates that neither MRQ or IAK is asserted. This means that a memory cycle will be initiated. It also indicates that the maps are not busy with an I/O cycle.

SPCL_WR2B+ asserts shortly into the SHC after FREEZE– asserts. It then persists for one cycle until SCND_CYCLE asserts. SCND_CYCLE–↓ causes GIO_FREEZE+ to deassert which then releases the micromachine freeze (FREEZE–↑).

RD_MAP+ is asserted for the normal and special map read cases. The assertion of RD_MAP causes the assertion of RAMOE which causes a read of the maps. NEED_MPAR+ is also asserted along with RD_MAP. This puts the MPAR register value out onto the MAP- and PG-buses. The equation for RD_MAP+ is as follows:

```
RD_MAP+ = (eMAPb+ * PC+ * SPCL_WR2B- * SCND_CYCLE-)
        + (eMAPb+ * SC+ * SPCL_WR2B+ * SCND_CYCLE-)
```

If eMAPb– is asserted without SPCL_WR2B, then a normal (non-special) map read is indicated. The timing of a normal map read is during the LHC of PC– so that PC– is gated with eMAPb– and SPCL_WR2B+. The resulting signal indicates the generic type of map read. If eMAPB– and SPCL_WR2B are asserted, then the special map read is indicated. The timing for this is during the LHC of SC (remember that PC is frozen). The signal SCND_CYCLE– is included in both cases to ensure that the map read for the special case only happens once before the memory operation. This prevents a subsequent read from occurring since the micromachine is frozen and eMAPb, MEMRQ, etc. stay asserted until the next PC–↑.

The memory cycle initiation that is associated with the special map read is covered in the discussion on MEMAC which is covered in the Memory Cycle Initiation section.

Map RAM Writes:

The signal RAMWE– is driven to the map/boot RAM write enable input(s). When write enabled, the RAM outputs go tristate. At the trailing edge of RAMWE–, the RAMs are actually written. For boot RAM writes the assertion of RAMWE occurs with BUSY and lasts until the subsequent SHFT_SC–↑. This 40-nanosecond write enable pulse easily satisfies the 25-nanosecond minimum WE pulse width of the RAMs. The assertion of RAMWE– for boot RAM writes is delayed until BUSY to ensure that no false writes occur when a processor memory cycle is preempted by a DMA or IAK cycle. The deassertion of RAMWE is sequenced with the GIO multiplexer select logic to ensure that the RAMWE–↑ occurs prior to the GIO-bus value changing.

For map writes, RAMWE– is asserted during the overlap of the LHCs of SHFT_SC and PC when lyMAP– is active (MAP is STOR-field). This ensures that the write will only occur when the GIO-bus is not in use. Recall that the LHC of PC is delayed until all freeze conditions are eliminated. A freeze would have been generated if the GIO-bus was needed for the map write and it was busy. When the PC LHC starts, GIO freeze (GIO_FREEZE+) is not asserted. Instead of using PC–, SC+ is ANDed with FREEZE– to achieve the same result. This is done so that the RAMs do not have a hold time problem. By using SC+, RAMWE– will be deasserting before the PC–↑ that will start the next microcycle. Recall that PC– is generated from SC+. By delaying RAMWE until the LHC of SHFT_SC, the map/boot RAM addresses are valid prior to the write enable input of the RAM being asserted. Map RAM write data is driven from the Y-bus onto the GIO-bus.

The boot/map RAMs have a data hold time requirement of 0 nanoseconds. It is quite reasonable that RAMWE– will deassert (at SC+↓) before the Y-bus data or the GIO-bus can be disabled and still guarantee 0 nanosecond hold time. The Y-bus data does not change until PC– can clock the MIR, its outputs are decoded, and a new set of operands can propagate through the ALU. The GIO-bus drivers are also tristated on the PC+↓.

The actual signals that generate RAMWE– are shown in the following equation (the signals and there function/meaning are also listed):

$$\text{RAMWE–} = [\,(\text{SHFT\_SC+} * \text{MEMDISL+} * \text{LBRAM\_AD+} * \text{TIMED\_MGO+}) + (\text{lyMAP+} * \text{FREEZE–} * \text{SC+} * \text{SHFT\_SC+})\,]'$$

SC+ is used along with FREEZE– to make an early version of PC+.

FREEZE– is used along with SC+ to make an early version of PC+.

lyMAP– indicates that a map write will occur this microcycle.

SHFT_SC+ is a shifted version of SC. It is used to terminate the boot RAM write at a controlled point for proper sequencing with the GIO multiplexer select logic. It delays assertion of RAMWE on map writes to ensure that the address is valid.

MEMDISL+ is a latched version of the signal MEMDIS which when asserted indicates a boot memory access. Again, there is no reason other than proper polarity to use the latched version of this signal.

LBRAM_AD+ is a latched signal that when asserted indicates the logical address falls in the address range of boot RAM (A13 NOR A14). There is no significance to the use of the latched version.

TIMED_MGO+ is a timed and qualified version of MGO. This signal is generated by QMGO+ * BUSY+ * WE+. TIMED_MGO+ provides a pulse that occurs during the SHC of SC between the assertion of BUSY and the deassertion of QMGO+. By waiting for the assertion of BUSY, it is ensured that QMGO+ will not be cancelled by MRQ.

The output enable for the lower 10 bits of the PER and the switch register (SR) are generated by gating PC with the micromachine enable signals. This ensures that the registers are not output enabled until the GIO-bus is free and there is no chance of bus contention. The enable conditions are as follows:

$$\text{ePER1gio-} = (\text{PC+} * \overbrace{(\text{eSRINb} * [\text{N=1}])}^{\text{ePER1b+}})'$$

$$\text{eSRgio-} = (\text{PC+} * \text{eLSRb})'$$

The clocking of the LED display register is accomplished by gating the store enable signal, lyLSR–, with PC. The falling edge of the resulting signal (lgioLED+ = PC– NOR lyLSR–) corresponds with the PC–↑ edge. As was already discussed, both the GIO data and the GIO-bus drivers are likely to change state at the same time. The registers that are used to hold the LED display data have a data hold time requirement of 5 nanoseconds. Circuitry is included on the board to ensure this hold time. The signal lgioLED+ is gated on the board with SCLK. Essentially, lgioLED+ is being used only as a clock enable. By clocking the LED display register using SCLK on the board, the 5 nanosecond hold time is met.

The Data Input/Output Bus (D-Bus)

The data I/O bus (or D-bus) is a bidirectional bus that is used strictly for data transfers between the processor chip, the on-board memory, boot memory, and the backplane data bus. On the processor chip, the D-bus is composed of the DI-bus, for input, and the DO-bus, for output.

The DO-Bus

The DO-bus is responsible for driving data to the board's D-bus for the purpose of writing to main memory (on-board or off-board), for writing to I/O (WRIO microorder), or for putting boot RAM data onto the backplane for observability (remember boot RAM sits on the GIO-bus and is not directly available on the backplane). The D-bus is also used to drive ones onto the backplane for memory reads of non-existent memory and for reads on which a memory protect violation occurs.

The DO-bus is a latched version of the DO2B bus. The bus is latched whenever BUSY asserts. Due to this, the processor chip provides the memory "data-in latch" function for processor writes to on-board memory. The DO2B bus source is selected by 2-to-1 multiplexers. They serve to select between passing either the DOUT register or the GI-bus value on to the DO-bus. The selection is done by the signal BRAM_AC+ (LBRAM_AD+ * QMGO+ * MEMDISL+). When asserted, the boot RAM read or write data, available on the GI-bus, is passed on to the DO2B-bus. Otherwise the output of the DOUT register is selected. The DO2B-bus is negative true and is driven to the DO-bus latches. A positive-true bus is obtained by using the Qbar output of the DO latches. The latches are kept transparent until the assertion of BUSY. They remain latched until the deassertion of LATCH at the end of the memory cycle.

For boot RAM reads, the DO-bus latches save the RAM read data until the end of the memory cycle for storing into the T-Register and maybe the CT-Register. Recall that the map/boot RAMs are only output enabled until the assertion of LATCH or the deassertion of QMGO whichever comes first. The DO latches preserve the boot RAM data so that the GIO-bus can be freed up for general micromachine use.

The signal, BRAM_AC+ is inverted to become BRAM_AC- which is driven onto the board as the signal BOOT-. This signal serves as one of the map/boot RAM address lines to "map" the 2-kbyte parts into a 1k boot RAM and a 1k map RAM.

The DO-bus is responsible for driving all ones onto the backplane during memory protect read violations (MPV * WE-) and during read accesses to non-existent memory (neither ACK, SEL, or MEMDISL asserted). These two conditions are used to generate the signal MRV_OEDAT- which will be further described in a moment. The signal MRV_OEDAT- is fed to the clear input of the DO latches. The Qbar outputs of the latches are sent to the D-bus output pads so that the D-bus is positive true.

The DO-bus is enabled on to the board's D-bus by the signal OED-. The bus needs to be enabled for any processor memory or I/O write and for any read violation (memory protect or non-existent memory access). The write enabling conditions are gathered into the signal WR_OEDAT- while the read violation conditions make up MRV_OEDAT-. Additionally, as already indicated, the D-bus also needs to be driven with boot RAM read and write data. This condition is identified by the signal BRAM_ACC-.

The WR_OEDAT signal is generated by observing outputs of the memory and I/O state machine. An I/O write is indicated by the assertion of IOGO while TFRZ is deasserted. TFRZ asserts during a read cycle with the same timing as BUSY. It is used to indicate that the T-Register is not yet valid and a freeze should occur if it is referenced. In this case TFRZ is only used to indicate that the current IOGO cycle is a write cycle. TFRZ is clocked into two flip-flops on different edges of SC-. The two clocked versions of TFRZ and TFRZ itself are ORed to generate dlydTFRZ-. This signal is used rather than just TFRZ because it lasts until the conclusion of the I/O handshake. Otherwise, the tail end of the I/O reads turn into I/O writes and cause bus contention.

A processor memory write is indicated by the assertion MGO (a processor MEMGO) while AOUT-[15] is asserted. OED- asserts at the assertion of MGO or IOGO depending on what type of write cycle is starting. For memory writes, WR_OEDAT- is maintained throughout the memory cycle until VALID deasserts. This is accomplished by the use of a latch. The latch is gated by (BUSY- * CHIP_VLD-). Whereas MGO only lasts one cycle, the latch holds WR_OEDAT- asserted until the memory write has taken place. The latch also makes the OED- enabling immune to MRQ assertions once the write is in progress. By using BUSY to initiate the latching, the OED- state is not affected by refresh lengthening the cycle. For the case of an I/O write, the assertion of WR_OEDAT- is completely controlled by the duration of IOGO.

The MRV_OEDAT- signal is generated by checking individually for the two read violation indications. The memory protect violation is indicated by the assertion MPV+ during a read cycle (WE- deasserted). MPV+ is gated against (BUSY * SECOND). SECOND ensures that the state of MPV is ignored until it is guaranteed to be valid. The signal, BUSY+, is used to remove the signal at the end of the cycle. The non-existent memory read violation is indicated by neither SEL, ACK, or MEMDIS asserting while WE- is deasserted.

The D-bus need only be driven until BUSY deasserts due to the way the backplane data drivers/latches are controlled. The latches that are directed from the D-bus to the backplane data bus are latched on the SC-↑. Since this occurs before the deassertion of BUSY on the chip, data need not be driven off-chip beyond this point.

The DI-Bus

The DI-bus receives processor main memory, boot ROM, boot RAM, and I/O read data. All incoming data is sent to the CT- and T-Registers for use by the micro-machine. The T-Register stores all D-bus read data. The CT register only stores instructions fetched.

External D-bus Control

The board D-bus is shared between on-board memory, the processor chip, and the backplane data bus bidirectional latch/driver.

The on-board main memory is controlled in such a way that the RAM outputs are never enabled unless the on-board memory is actually selected for a read access (SEL asserted). This allows the RAM inputs and outputs to be shorted together onto the D-bus. This requirement means that the RAMs don't receive CAS unless SEL is asserted. On writes, the RAMs operate using an "early write" write cycle. The write enable of the RAMs becomes active before CAS asserts. If this were not the case, the RAM outputs would enable at CAS time and conflict with the write data present on the D-bus. The memory write actually occurs at the falling edge of CAS.

When there is an on-board memory read, the RAMs are output enabled throughout the time CAS is asserted. CAS does not last through the end of the memory cycle.

It deasserts sometime after the SC-↑ edge that BUSY goes away. Memory or I/O read data is clocked into the processor chip's T/CT registers on the same SC- edge. On-board memory read data must also be driven onto the backplane for the duration of the memory cycle. Because the RAM data will disappear (RAMs go tristate after CAS-↑), the data is latched into the latch/bus driver chips used for interfacing the board with the backplane data bus. The data is latched throughout each SC- SHC and is transparent during the LHC. The latch control of the driver chips is handled the same regardless of whether the on-board memory, boot memory, or the processor chip is the intended backplane driver.

The output enable of the latches for the D-bus to backplane direction is the signal OED2BP- generated by the processor chip. There are two conditions for OED2BP-: 1) a read condition and 2) a write condition.

For on-board memory reads, the D-bus drives the backplane whenever SEL is asserted, MPV+ is asserted, or when ACK- is not asserted. This set of conditions covers boot memory reads, and non-existent memory accesses. The OED2BP- read condition is as follows:

(SEL+ + ACK- + MPV+ + MEMDISL+) * WE- * bOEBP2D-

OED2BP- is latched (READ_EN+) and held to the end of the memory cycle by SECOND-. The LATCH+ signal drives the clear line of the latch. This ensures that at the end of the cycle, the drivers get off of the backplane. Because the clocks on the processor chip lag behind the backplanes, the signal BPKIL+ is provided on the board to ensure that the backplane is not driven any longer than it should be. BPKIL+ is used to tristate the drivers without relying on OED2BP-. The signal bOEBP2D- is included in the read condition to help prevent bus contention. It is the received version of the OEBP2D- signal driven onto the board. The generation of OEBP2D- will be covered shortly.

The OED2BP write condition is provided by the WR_OEDAT- signal previously described for the OED- signal generation. The WR_OEDAT signal covers the case of any write to memory or I/O. The equation for OED2BP- is as follows:

OED2BP- = bOEBP2D- * (READ_EN + WR_OEDAT)

The bOEBP2D- signal ensures that the D-bus transceivers are never enabled in both directions at once. bOEBP2D- is the received version of the processor chip OEBP2D- output to the board. Therefore, the OED2BP- signal cannot assert until it is known that the board has been "told" to disable the D-bus transceivers in the backplane to D-bus direction.

The drivers used to drive the backplane are also used to allow the backplane to drive the D-bus. The output enable for the backplane to D-bus direction is the signal OEBP2D- which is output from the processor chip. The backplane must be enabled onto the D-bus on the board when there is a DMA write to on-board memory, during a processor off-board memory access, and during a processor I/O read. The implementation chosen does not distinguish between on- or off-board DMA writes. Any DMA write enables the backplane data onto the D-bus. The DMA write condition is latched by LATCH- to ensure that the DMA data is present at the main memory DRAMs when the write actually takes place.

The meaning and function of the signals used in determining these conditions are described below:

```
OEBP2D- = ( bOED2BP- * OED- *
                       [(MAIP+ * TRFZ+ * ACK+)
                       + (MAIP- * TFRZ+ * MRIOIP+ * DIST+ * SIORQ-)
                       + latched (SMRQ+ * WE+ * BUSY+)] )'
```

bOED2BP- is the received version of the OED2BP- output to the board. It ensures that the drivers are only enabled in one direction at a time.

MAIP+ (Memory Access In Progress) is an output of the memory and I/O state machine. This signal has the same timing as BUSY. It indicates that a processor memory access is in progress.

TFRZ+ is an output of the memory and I/O state machine. This signal is asserted when a memory read is requested. It lasts until the SC-↑ that causes BUSY-↑ for this memory access.

DIST+ is an output of the memory and I/O state machine. This signal is asserted when in the second or later cycle of an I/O handshake prior to IORQ being deasserted. The signal is both asserted and deasserted on SC-↑.

ACK+ is asserted by an off-board memory array when an address within its addressing range is detected. This signal asserts around the assertion of LATCH and lasts to the end of the memory cycle.

MRIOIP+ (Memory Read or I/O Operation In Progress) is an output of the memory and I/O state machine. This signal indicates that a memory read or an I/O operation is in progress. Along with the signal MAIP+, this signal identifies when the processor is doing an I/O access. This signal, when indicating an I/O access, has similar timing to IOGO.

SIORQ- is the output of a latch used to capture IORQ. This signal is used to indicate the last cycle of an I/O handshake. On an I/O read, this is used to enable the BP data bus onto the D-bus only when data is guaranteed to be valid.

SMRQ+ is a version of MRQ that is synchronized with SHFT_SC-↑.

WE+ (Write Enable), when asserted, indicates a memory write cycle. It becomes valid towards the end of MEMGO and is latched until the end of the memory cycle.

BUSY+ indicates that memory is busy with the current access.

A processor memory read of off-board memory is indicated by MAIP+ * TFRZ+ * ACK+. A processor I/O read is indicated by notMAIP+ * MRIOIP+ * TFRZ+. The last case of a DMA write is identified by SMRQ+ * WE+ * BUSY+. The DMA write condition is latched and gated by SC-. This enables the drivers to drive the D-bus at about the same time as BUSY asserts and to disable when BUSY deasserts. This timing ensures that there is no bus contention either at the start of the DMA write or

with any subsequent use of the D-bus. All three of the above conditions are ORed together to generate OEBP2D–.

Since the boot ROMs also reside on the D-bus, the processor chip provides for their enabling too. Whenever a boot ROM read is detected, the signal BROMOE– is asserted. The boot ROMs must be enabled from soon after BUSY asserts until BUSY deasserts. When the boot ROM data is valid past the board's SC–↑ when BUSY–↑ occurs, the drivers latch the ROM data for driving onto the backplane and the processor chip clocks it into the T/CT registers. The equation for BROMOE– is as follows:

BROMOE– = (WE– * MEMDISL+ * LBROM_AD+ BUSY+)

The signal LBROM_AD+ is a latched indication that the current address is in the address space of boot ROM as opposed to boot RAM.

The Map-Bus

The Map-bus is the input to the upper 5 bits of the map/boot RAM address inputs. When the micromachine accesses a map register (logically, there are 1024 of them in the map RAMs) the Map-bus selects one of 32 possible sets of map registers. The bus value is taken from the map address register bits 5 through 9 (MPAR+[5:9]). When used in accessing boot RAM, the Map-bus receives 5 bits of the logical address (AOUT+[5:9]). However, most common use of the Map-bus is to select the map set for all main memory accesses. For processor accesses, this is accomplished by directing the contents of the AEOUT latch (AEOUT+[0:4]) onto the Map-bus. The AEOUT latch holds the map set number that the current processor access wishes to use. The only other internal processor chip source for the Map-bus occurs in the case of an interrupt acknowledge or a DMA self-configuration cycle. The processor chip drives the Map-bus with all zeros in these two cases to force the access to use map set 0.

The Map-bus 4-to-1 multiplexers receive MPAR, the AEOUT latch, and the AOUT latch outputs. The conditions for indicating which data to pass can be summarized as follows:

MPAR must be selected on any map read or write. This condition is indicated by the signal NEED_MPAR+. This signal takes into account the special map read situation that occurs for operations such as wrp := map.

AOUT must be selected on a boot RAM access. This condition is indicated by the assertion of MEMDIS when the processor must do a memory access (IMEMDIS+ * BUSY– * (MRP+ + MEMAC+)) with the address in the range of boot RAM (or not in boot ROM).

AEOUT must be selected for any non-boot memory access. This condition is the default. If the map RAM or the boot RAM is not being accessed (mutually exclusive events), then by default the AEOUT data is passed to AEOUT.

The signal NEED_MPAR+ referred to above asserts as soon as a map access (read or write) is indicated. A map read is indicated when eMAPb– asserts (MAP in the

BBUS-field). A map write is indicated when lyMAP- asserts (MAP in the STOR-field). A map write occurs when lyMAP- asserts if neither the processor nor I/O needs the GIO-bus (not(MRP+ + MEMAC+ + SMRQ+ + SIAK+)) or if BUSY and LATCH are asserted.

Similarly, a map read occurs when eMAPb- asserts if neither the processor nor I/O need the GIO-bus or if BUSY and LATCH are asserted. The exception to this is a write cycle that needs map read data. This condition is detected by the signal SPCL_WR2B+ which is described in the External GIO-bus Control section. A special map read (one that must occur prior to the memory access) is indicated by the simultaneous assertion of SPCL_WR2B+ and eMAPb-. All these conditions are used to generate the composite signal, NEED_MPAR+.

Multiplexers are used to determine the values on the Map-bus and PG-bus. Two signals, MP_S1+ and MP_S0+, pick the source for the Map-bus and PG-bus.

Map/PG-Bus Multiplexers

MP_S1+	MP_S0+	SELFC-	Map-Bus Value	PG-Bus Value	Purpose
0	0	1	AEOUT[0:4]	AOUT[10:14]	main memory access
0	1	1	AEOUT[5:9]	AOUT[0:4]	boot RAM access
1	0	1	MPAR[5:9]	MPAR[0:4]	map access
1	1	1	n/a	n/a	-
X	X	0	0	don't care	IAK or self-config DMA

MP_S1+ = NEED_MPAR+

MP_S0+ = -NEED_MPAR+ * (MRP+ + MEMRQ_2B+)
* BUSY- * MEMDIS+ * BRAM_AD

The latches that reside on the outputs of the MAP/PG-bus multiplexers maintain the MAP/PG-bus value between the end of the microcycle (when the multiplexer inputs can change) and the time when the MAP/PG-bus has satisfied the map/boot RAM address hold time (indicated by QMGO+↓). The gate signal for the MAP- and PG-bus latches is as follows:

MP_LTCH+ = -(QMGO+ * SC-)

The outputs of the latches are gated with MAP_CLEARx+ by NOR gates. The NOR gate outputs are "zeroed" on interrupt acknowledge (IAK) and on DMA self-configuration cycles. In both of these cases, the access must be forced to map set 0. These two conditions are handled in a uniform manner by observing the backplane signal SELFC-. SELFC- is asserted on IAK cycles by the acknowledging I/O interface as well as during self-configuring DMA. The signal MPOE+, output by the processor chip, enables the MAP-bus and PG-bus bidirectional bus transceivers (74F245). SELFC- is NANDed with MPOE+ to generate the output enable for the MAP transceivers. The resulting signal, QMPOE- (Qualified Map-Page Output Enable), is input back into the processor chip. When MPOE+ is asserted but QMPOE- is not, thenSELFC- must be asserted. When this occurs the MAP-bus is forced to be all zeros. The LATCH- signal in the MAP-bus clear condition generation

only allows the MAP-bus to be forced to zero when the map outputs are being latched.

The MAP-bus is always output enabled unless MRQ is asserted without SELFC- asserted. This is the only condition in which I/O drives the MAP-bus (that is, non self-configuring DMA). The MAP-bus output enable, OEMAP-, is generated by ORing the enable conditions. The signal INT_SELFC- is only asserted during IAK or DMA self-configuration cycles. The enable condition is ORed with SECOND- so that the processor chip MAP-bus drivers are only disabled during the period of time that the MAP-bus is needed for the DMA memory access mapping.

External Map-Bus Control

In addition to the map/boot RAMs and the processor chip, a 74F245 bidirectional bus transceiver resides on the Map-bus. The direction of the transceiver is selected by the signal OEAD-, and its output enable is controlled by QMPOE-.

The signal OEAD-, when asserted, directs the transceiver toward the backplane thus driving the backplane address extension (AE) bus. This is the default state of OEAD. The AE-bus is driven by the processor chip's AEOUT latch value or the AOUT[5:9] value (on boot RAM accesses). When deasserted, OEAD- points the transceiver toward the board allowing the backplane AE-bus to drive the Map-bus on the board. OEAD is deasserted for either an IAK or DMA cycle prior to the assertion of SECOND. The extra term, preBPON, is included to keep the board from driving the backplane on power-up. YOGI_OE is also included to keep OEAD from enabling the WE- I/O pad when the processor chip is not selected. After SECOND asserts, OEAD also asserts. The assertion of SECOND corresponds to the point in a memory access when an I/O interface tristates its backplane address/data drivers during a DMA or IAK cycle.

```
OEAD+ = SECOND+ + (preBPON+ * SIAK- * SMRQ- * YOGI_OE+)
```

The processor chip signal MPOE is used as the output enable for the board PG/Map-bus backplane transceivers. The generation of MPOE is such that MPOE deasserts prior to the PG/Map-bus transceivers being directed towards the backplane. This avoids contention with the I/O interface which has been actively driving the backplane up to this point in the memory cycle. The board aids in this effort by inverting MPOE. The inversion adds delay to MPOE and further enforces the sequencing of the enable and direction selection. The equation for MPOE+ generation is as follows:

```
MPOE+ = OEAD+ + (BUSY- + LATCH-)
```

When OEAD is not asserted, the indication is that an interrupt acknowledge or a DMA cycle is imminent. After OEAD deasserts, the deassertion of MPOE will occur when LATCH asserts. This allows the map RAM access to complete before affecting the map RAM's address. MPOE stays deasserted until OEAD reasserts.

The Page-Bus (PG-bus)

The PG-bus is the input to the lower order address inputs of the map/boot RAMs. When used in accessing the map RAMs, the PG-bus selects one of the 32 map registers within the map set selected by the value on the Map-bus. The PG-bus value is taken from the map address register bits 0 through 4 (MPAR+[0:4]) for a map register read/write. When used to access the boot RAMs, the PG-bus gets the lower 5 bits of the logical address (AOUT+[0:4]). In all other cases, the PG-bus is used to access the map/boot RAMs with the intent of generating a physical address for accessing main memory. In this case, the PG-bus contains the upper 5 bits of the logical address (AOUT+[10:14]).

The PG-bus 4-to-1 multiplexers are controlled identically to the Map-bus multiplexer controls previously described. Similarly, the PG-bus output latches are also handled identically to the MAP-bus latches.

The conditions for which data are to pass are summarized below for completeness:

MPAR — must be selected on any map read or write. This condition is indicated by the signal NEED_MPAR+. This signal takes into account the special map read situation that occurs for operations such as wrp := map. The multiplexer outputs are latched by QMGO+. This provides for address hold time on the map RAMs.

AOUT[0:4] — must be selected on a boot RAM access. This condition is indicated by the assertion of MEMDIS during a processor MEMGO (QMGO+) with the address in the boot RAM address range (or not in boot ROM). The timing of the QMGO signal ensures that the multiplexer selects cannot change earlier than SHFT_SC–↑. This edge corresponds to LATCH–↓ on the board.

AOUT[10:14] — must be selected for any non-boot memory access. This condition is the default. If map RAM or boot RAM is not being accessed (mutually exclusive events), then by default AOUT+[10:14] data is passed to the PG-bus.

The PG-bus is always enabled unless INTorDMA+ (SIAK + SMRQ) is asserted. This is the only condition when I/O must drive an address to the map/boot RAMs. The INTorDMA+ signal is ANDed with SECOND– to allow the PG-bus to be disabled only during the period of time when the board's PG-bus is used by the I/O system for a map access.

External PG-bus Control

In addition to the map/boot RAMs and the processor chip, the only other device on the PG-bus is a 74F245 bidirectional bus transceiver. The direction of the transceiver is selected by OEAD– and its output enable is controlled by MPOE– (the inverted MPOE+ output of the processor chip).

As previously described, OEAD– keeps the transceiver directed toward the backplane unless there is an indication that I/O will be using the address bus.

The GIO Freeze Condition

The micromachine must freeze when a conflict occurs between its need to use the GIO-bus and the use of the GIO-bus for a memory access. In all cases but one, the micromachine yields to a memory access. When a conflict occurs the micromachine (that is, the PC) freezes and waits for the conflicting condition to be removed before continuing. Note that this section only describes the freeze condition related to the use of the GIO-bus.

The micromachine needs the GIO-bus for the following:

1) map reads (eMAPb–)
2) map writes (lyMAP–)
3) LED display register writes (lyLSR–)
4) switch register reads (eLSRb–)
5) central interrupt register reads (eSRINb– and (N=3))
6) low word parity error address register read (eSRINb– and (N=1))
7) off-chip SRIN register read/writes (lyOFFC_SRIN or eOFFC_SRINb)

These conditions are input into a NAND gate which generates the signal NEED_GIO+.

A freeze must occur if NEED_GIO asserts and a memory cycle is about to start. This freeze only needs to last until BUSY asserts. Once BUSY asserts the GIO-bus will be free during the subsequent LHC of SC or PC.

```
GIO_FREEZE+ = NEED_GIO+ * BUSY- * SCND_CYCLE- *
                          (SIAK+ + SMRQ+ + MRP+ + MEMCYC_REQ+)
```

The following is a description of some of the signals involved in a GIO freeze condition:

SIAK+ — When asserted, this signal indicates that an IAK memory cycle is about to start. This signal is actually IAK synchronized to SC–↑.

SMRQ+ — When asserted, this signal indicates that a DMA memory cycle is about to start. This signal is MRQ synchronized to SHFT_SC–↑.

MRP+ — (Memory Request Pending) indicates that the processor has a queued-up memory request that will happen when the backplane is free.

MEMRQ– — (Memory Request) indicates that a memory access has been requested during this microcycle. MEMRQ– is used to generate MEM-CYC_RQ–.

MABAB+ — (Memory Address for the A- or B-Register) if deasserted, the assertion of MEMRQ– will reference memory and not the A- or B-Register. Remember, the A- and B-Registers are memory mapped but reside internal to the micromachine. MABAB+ is used to generate MEM-CYC_RQ–.

MEMCYC_RQ– — (Memory Cycle Request) is the NAND of MEMRQ+ and MABAB–, when asserted indicates that on this microcycle there is a request for a memory cycle that is not A- or B-Register addressed.

SCND_CYCLE– is the second cycle of the special map-read/memory-write cycle. When asserted this is another indication of an impending memory cycle. In this case it is actually being used to deassert the GIO_FREEZE condition after the special map read is complete and the memory access may begin.

The GIO freeze conditions almost exclusively freeze the micromachine until an executing or requested memory cycle reaches the BUSY-asserted state. The one exception is the special map-read/memory-write situation previously discussed.

When a GIO freeze occurs whereby it is necessary to start a memory cycle in order to eliminate the freeze condition, an interesting problem can occur. There is a standard (that is, a non-GIO related) freeze condition that causes a freeze if a fetch microorder (FCHB or FCHP) is executed while BUSY is asserted. If a GIO freeze occurs during a cycle requesting a fetch, the following recurring sequence can happen:

1) MIR indicates a micromachine GIO access and a FCHP/FCHB microorder

2) GIO freeze causes PC– to freeze in the SHC

3) memory operation starts

4) BUSY asserts

   i) GIO freeze condition releases

   ii) FCHP/FCHB freeze condition asserts (that is, PC stays frozen)

5) BUSY deasserts

   i) FCHP/FCHB freeze condition releases

6) Go to 1

In order to avoid this "infinite loop", the signal GIO_SCND– is used to disable the FCHP/FCHB freeze condition when it is asserted. GIO_SCND– is generated by identifying a GIO-only freeze (GIOFREEZE+ * NONGIOFRZ–) and clocking this into a flip-flop on SC–↑. This serves to disable the FCHP/FCHB freeze long enough after the GIO freeze releases to allow the microcycle to end. As soon as a new microinstruction is read, the problem goes away.

Signal Glossary

The following descriptions of the processor chip buses and their control relies heavily on signals that are generated outside of the specific block of logic being discussed. Therefore, the following glossary of signals, their meanings, and relative timings (if relevant) is included.

Clocks

SC — is the system clock. This clock is identical to (though skewed from) the backplane SCLK–. This clock is non-freezable.

PC — is the processor clock. This clock is used by the micromachine and **not** the memory and I/O interface logic. This clock may have its SHC extended for an integral number of SC cycles due to a freeze (that is, a resource contention).

DC — is a version of SC. Only differs during error correction cycles. This clock is used to clock the T- and CT registers to capture data returned from a memory or I/O read.

SHFT_SC — is a shifted (in time) version of SC. SHFT_SC is delayed 55ns +/– 3ns from SC+ on the board. It should track SC+ on the chip with approximately the same timing as well.

Memory Handshake Signals

MEMGO — indicates a desire by either I/O or the processor to initiate a memory cycle. It is asserted ideally for one cycle between SC–↓ edges. The signal is open-collector and has long delays when changing state. A processor MEMGO may be deasserted by the assertion of MRQ. The only two cases of I/O generated MEMGO's are DMA cycles, and IAK cycles.

BUSY — indicates that memory and the backplane are busy and not available to start another transaction. Timing is from SC–↑ during MEMGO up to the SC–↑ during VALID. This is one SHC of SC before the completion of the memory cycle. The processor clocks in memory read data into the T/CT registers on the DC–↑ that corresponds to the BUSY–↑.

LATCH — is a memory controller/array timing signal that asserts on the SHFT_SC–↑ that occurs after BUSY–↓. LATCH– lasts until the SC–↓ edge after BUSY–↑.

SECOND — is a memory controller timing signal whose timing is identical to that of BUSY but is shifted one SHC to be from SC–↓ to SC–↓.

MRQ — is an open-collector signal from I/O cards that indicates the desire to do a DMA cycle on the next available backplane cycle. It is asserted on an SC– edge and lasts until the SC–↓ that also deasserts MEMGO on the last requested DMA.

SMRQ — is a synchcronized version of MRQ. This is MRQ synchronized to SHFT_SC–↑.

IAK — is a processor signal sent to I/O to allow I/O to initiate an interrupt acknowledge cycle. This clears the way for acknowledging an I/O card to do a MEMGO and supply the trap cell address for the processor memory read. The memory and I/O state machine treats an IAK cycle just like a processor read except that IAK is asserted and MGO/QMGO.

SIAK is a synchronized version of IAK. This is IAK synchronized to SC-↑.

IORQ is a signal received from I/O to indicate the need for an I/O handshake cycle. It is only asserted after an I/O instruction broadcast cycle (microorder BFB). The processor then responds with an IOGO after the execution of a WRIO or RDIO microorder.

WE indicates whether the current memory cycle is a read or write cycle. Asserted along with the address, this signal can only be considered valid after BUSY-↑. The state of WE is latched until LATCH-↑.

Memory and I/O State Machine (MIOSM) Signals

MAIP+ indicates a processor memory access is in progress. Asserted on SC-↑ during processor MEMGO. It lasts until the SC-↑ that occurs during VALID. Essentially the same timing as BUSY. Also occurs during IAK cycles but asserts on SC-↑ during IAK assertion. Deassertion still occurs on SC-↑ that occurs during VALID.

MRP+ indicates that MIOSM has a memory or I/O request from the processor pending and it is waiting for access to the backplane. Asserts on the SC-↑ that occurs after the assertion of MEMAC when the backplane is busy. Deasserted on SC-↑ after the pending access's MEMGO or IOGO is initiated.

MRIOIP indicates that a memory read or I/O access is in progress. Timing is the same as MAIP+ but just for memory reads. For I/O accesses, assertion is SC-↑ during IOGO, and deassertion is on SC-↑ 2 cycles later.

DIST is used to differentiate similar states in the MIOSM. It is used in the bus control logic to indicate cycle 2 of an I/O access. The MIOSM stays in this state until the SC-↑ after IORQ deasserts.

TFRZ indicates, when asserted, that the current memory or I/O access is a read and that the data from the read has not yet been returned to the processor. The timing is the same as MRIOIP.

MGO+ indicates that the processor wants to do a MEMGO to start a memory cycle. This is a one-cycle signal that asserts/deasserts about the SC-↓. It can assert a little late and maybe deasserted prematurely if MRQ is asserted.

QMGO+ is the same indication as MGO+ except that the normal (non-MRQ related) deassertion is in the middle of the SHC on SHFT_SC-↑.

Miscellaneous

MEMDISL indicates that the present memory cycle is a boot memory access cycle. This signal can only be considered valid after BUSY-↑. MEMDISL is latched until LATCH-↑.

MEMRQ indicates that a microorder from the micromachine that requires a memory or I/O cycle is currently being executed. Timing is from sometime into the SHC of PC for one cycle.

MEMRQ_2B is a preliminary version of MEMRQ.

FREEZE indicates that a micromachine is in effect. This holds the SHC of PC asserted for the normal 2 FC cycles plus an additional number of SC cycles. It is asserted and deasserted sometime within the SHC of SC.

NONGIO_FRZ indicates that the current FREEZE assertion is due to a non GIO-related freeze condition. The timing for this signal is the same as for FREEZE.

Processor Chip Pads

The processor chip uses several types of pads. The INPAD is an input pad with an input enable. It is used for all input only signals. The RIOPAD is a bidirectional pad with a tristate output and an enabled input. There are three types of ground pads (VSS). The V_SSPAD is used to route ground around the standard cell array. The VSSPADs supply ground to the pad bus. There are special VSSPAD cells which go into the corners of the chip. There are two types of power pads (VDD). The V_DDPAD supplies power to be routed through the standard cell array, and the VDDPAD pads supply power to the pad bus.

Input Pad Control

The CMOS-40 technology requires that chip inputs not be allowed to float for any length of time. Floating conditions on the inputs are seen during both normal and battery backup operation of the processor chip. To meet this requirement the input enable was designed into the pads. The input enable is implemented as an OR-gate with a low-true enable. Therefore, when the input is disabled, the input signal is driven high (logic 1).

The bidirectional I/O pads (RIOPAD) are used for output-only signals and have their inputs permanently disabled.

Many inputs can be enabled whenever backplane PON is asserted and can be disabled otherwise. These inputs are not needed for proper operation of the processor chip refresh or initialization circuitry. Additionally, these inputs are always driven when not in battery backup mode. The actual enable signals are buffered versions of the signal preBPON+ which asserts one cycle prior to the start-up of the micromachine at the assertion of BPON. The signals that fall into this class are as follows (using internal processor chip names):

iMPV-	IIORQ+	iPFW+	YOGI_OE+
iINTRQ+	QMPOE-	IMRQ+	USIZE+
iSLAVE	iACK+	iMLOST+	SEL-
iMEMGO+	PE+	SHFT_SC+	OFF_BRDCS+

Some inputs must always be enabled. These are signals required for battery-backup operation, or signals that go to an "undesired" state when disabled. The input disabled state of a PAD is high (logic 1). Signals that fall into the "always enabled" category are as follows:

SC2B+	ECYC+	FC+	
iRAS+	iCLOCK-	iSPON+	iCCLK-

The last class of inputs have more complex requirements for enabling and disabling. These inputs float during normal operation. Each of these inputs has an enable condition that applies only when preBPON is asserted. The signals and their input enable equations are as follows:

GI+[0:15] Note that the following signal is asserted whenever something is valid on the GIO-bus:

qienGIO- = ePER1gio + eSRgio + eSRINgio + RAMOE + OEGIO + preBPON-

DI+[0:15] Note that the following signal is asserted whenever the D-bus is driven:

qienD- = OED2BP + OEBP2D + preBPON-

BRD_WE- Note that the signal BWE- floats when the transceiver on the board that drives WE- on the backplane is tristate. This condition is covered by MPOE.

qenMPOE- = MPOE- + preBPON-

CSD+[0:31] The following signal disables the Control Store Data inputs on an unimplemented instruction cycle. The CSD+ bus goes to all ones and is then modified by the UMI multiplexer to yield a NOP.

qenUMI- = UMI+ + preBPON-

Processor Chip Signal Descriptions

Table 3-20 contains the processor chip signal names and their descriptions. Refer to this table when reading the information in Table 3-21.

Processor Chip Pin Listing

Refer to schematic 10 at the end of Chapter 2 for the location of each pin number on the processor chip. Table 3-21 contains signal name and information for each pin and Table 3-22 contains the processor chip pad listing.

Table 3-20. Processor Chip Signal Descriptions

Signal Name	Description
ACK+	Acknowledge backplane cycle
BDSEL–	On-board memory array selected
BOOT–	Selects between boot RAM and map RAM
BRMOE–	Boot ROM output enable
BUSY+	Memory busy signal
BWE–	Memory write enable signal
CLOCK–	Oscillator output
CRS+	Control Reset signal
CSA+[0:13]	Control Store Address bus (14 bits)
CSD+[0:31]	Control Store Data bus (32 bits)
CTRN2B+	CPU turn for memory access
D+[0:15]	Bidirectional Data-bus (16 bits)
DB2DE–	Control signal for Data-bus external to chip
D2DBE–	Control signal for Data-bus external to chip
EC+	Error correction signal
ECIL–	Enable Central Interrupt Latch
ESR–	Enable Switch Register
FCLK+	Fast clock
FETCH2B+	Instruction fetch signal
FREEZE–	Processor freeze signal
GIO+[0:15]	General Input/Output bus (16 bits)
GO–	Indicates the start of a memory cycle
IAK2B+	Interrupt acknowledge signal
INTRQ+	Interrupt request signal
IOGO+	Input/output handshake signal
IORQ+	Input/output request signal
IORST–	Timed reset signal for on-board I/O
LADR–	Load address register
LLEDR+	Load LED register
MAP+[0:4]	Map RAM address bus (5 bits)
MAPWE–	Map RAM write enable signal
MDISL+	Memory disable signal. Selects main or boot memory
MEMGO+	Backplane cycle handshake signal
MLOST+	Memory lost signal from powerfail
MGO+	Memory GO handshake signal
MP–	Used to enable memory protect function
MPOE–	MAP/PG-bus output enable
MPV–	Indicates a memory protect system violation
MRQ+	Memory cycle request
N+[0:3]	Indirect addressing to registers
OEAD–	Output enable address
OFFBDCSA+	Indicates microaddress is off-board
PELCH–	Parity error latch signal
PFCLK+	Pre-FCLK, output to the board
PFW+	Powerfail warning signal
PG+[0:4]	Page Address bus (5 bits)
PLC+	Pre-latch clock
PPCLOCK+	Pre-processor clock
PS+	Parity sense (odd or even parity generation)
PSCHOD+	Slave Chain Output Disable
PSCLK+	Pre-system clock

Table 3-20. Processor Chip Signal Descriptions (continued)

Signal Name	Description
QMOE–	Qualified memory output enable signal
RAMOE–	RAM output enable signal
RAS+	Row Address Strobe for RAM
RDPEA–	Read Parity Error Address
REF–	Memory refresh signal
RNI+	Read Next Instruction
SC+	System clock
SHFTSC+	Shifted system clock
SLAVE+	Places processor in slave mode
SPON+	Synchronized power-on signal
STVLD+	Valid signal for backplane access
UCSIZE+	Indicates 2k or 4k of microcode space
XTEST+	Condition test for support of floating point
YCCLK–	Yellowstone communications clock signal
YOGICS–	Processor chip select, tristates all chip outputs

Table 3-21. Processor Chip Pin Listing

Pin Number	Signal Name	Type	I_{IH} (μA)	I_{IL} (mA)	Cap. (pF)	Pin Number	Signal Name	Type	I_{IH} (μA)	I_{IL} (mA)	Cap. (pF)
1	VSS					51	PG+[3]	O	110	1.54	57
2	MPV-	I				52	PG+[4]	O	100	1.54	57
3	MP-	O	40	2.0	40	53	VDD				
4	DB2DE-	B *	40	1.2	40	54	IOGO+	O	20	1.0	35
5	D2DBE-	B *	40	1.2	40	55	IORQ+	I			
6	OEAD-	O	90	3.0	48	56	MRQ+	I			
7	LADR-	B *	50	1.0	38	57	REF-	O	60	1.4	45
8	QMOE-	I				58	RAS+	I			
9	MPOE+	O	40	1.2	40	59	BDSEL-	I			
10	GIO+[0]	B	250	3.34	57	60	GO-	O	20	1.0	35
11	VDD					61	MDISL+	O	40	1.2	40
12	GIO+[1]	B	250	3.34	57	62	BUSY+	O	110	3.4	50
13	GIO+[2]	B	250	3.34	57	63	VSS				
14	GIO+[3]	B	250	3.34	57	64	ACK+	I			
15	GIO+[4]	B	250	3.34	57	65	STVLD+	O	50	1.6	35
16	GIO+[5]	B	250	3.34	57	66	MGO+	O	40	1.2	40
17	GIO+[7]	B	250	3.34	57	67	BWE-	B	90	2.1	40
18	GIO+[6]	B	250	3.34	57	68	MEMGO+	I			
19	GIO+[8]	B	250	3.34	57	69	MAP+[0]	O	90	1.52	45
20	GIO+[10]	B	250	3.34	57	70	MAP+[1]	O	90	1.52	45
21	VSS					71	MAP+[2]	O	90	1.52	45
22	GIO+[9]	B	250	3.34	57	72	MAP+[3]	O	90	1.52	45
23	GIO+[11]	B	250	3.34	57	73	VDD				
24	GIO+[13]	B	250	3.34	57	74	MAP+[4]	O	90	1.52	45
25	GIO+[12]	B	250	3.34	57	75	RDPEA-	O	50	1.0	38
26	GIO+[14]	B	250	3.34	57	76	LLEDR+	O	20	.60	35
27	GIO+[15]	B	250	3.34	57	77	ESR-	O	20	.60	35
28	BRMOE-	O	20	.02	40	78	ECIL-	O	20	.60	35
29	BOOT-	O	20	.02	40	79	VSS				
30	RAMOE-	O	20	.02	40	80	SPON+	I			
31	VDD					81	PFW+	I			
32	MAPWE-	O	20	.02	40	82	EC+	I			
33	XTEST+	O				83	CSA+[1]	O	230	1.6	60
34	N+[0]	O	120	3.02	53	84	CSA+[0]	O	230	1.6	60
35	N+[1]	O	120	3.02	53	85	VSS				
36	N+[2]	O	120	3.02	53	86	CSA+[2]	O	230	1.6	60
37	N+[3]	O	120	3.02	53	87	CSA+[3]	O	230	1.6	60
38	MLOST+	I				88	CSA+[4]	O	230	1.6	60
39	SLAVE+	I				89	CSA+[5]	O	230	1.6	60
40	FETCH2B+	O	20	1.0	35	90	CSA+[6]	O	230	1.6	60
41	CRS+	O	90	3.02	45	91	CSA+[7]	O	230	1.6	60
42	RNI2B+	O	20	1.0	35	92	VDD				
43	VSS					93	CSA+[8]	O	230	1.6	60
44	PSCHOD+	O	100	3.6	40	94	CSA+[9]	O	230	1.6	60
45	CTRN2B+	O	70	3.0	40	95	CSA+[10]	O	230	1.6	60
46	IAK2B+	O	40	1.6	40	96	CSA+[11]	O	230	1.6	60
47	INTRQ+	I				97	CSA+[12]	O	230	1.6	60
48	PG+[0]	O	110	1.54	57	98	CSA+[13]	O	230	1.6	60
49	PG+[1]	O	110	1.54	57	99	IORST-	O	70	1.6	40
50	PG+[2]	O	110	1.54	57	100	SHFTSC+	I			

where:
B = Bidirectional
B* = Internal Feedback
O = Output
I = Input

Table 3-21. Processor Chip Pin Listing (continued)

Pin Number	Signal Name	Type	I_{IH} (μA)	I_{IL} (mA)	Cap. (pF)	Pin Number	Signal Name	Type	I_{IH} (μA)	I_{IL} (mA)	Cap. (pF)
101	SC+	I				151	D+[0]	B	90	.67	52
102	PPCLOCK+	O	80	.84	85	152	D+[2]	B	90	.67	52
103	YCCLK-	I				153	D+[3]	B	90	.67	52
104	CLOCK-	I				154	D+[4]	B	90	.67	52
105	FCLK+	I				155	D+[5]	B	90	.67	52
106	VSS					156	D+[6]	B	90	.67	52
107	FREEZE-	O	50	1.0	35	157	VDD				
108	PSCLK+	O	50	1.0	35	158	D+[7]	B	90	.67	52
109	PLC-	O	50	1.0	35	159	D+[8]	B	90	.67	52
110	PFCLK+	O	50	1.0	35	160	D+[9]	B	90	.67	52
111	CSD+[0]	I				161	D+[10]	B	90	.67	52
112	CSD+[1]	I				162	D+[11]	B	90	.67	52
113	CSD+[2]	I				163	D+[12]	B	90	.67	52
114	CSD+[3]	I				164	D+[13]	B	90	.67	52
115	VDD					165	D+[14]	B	90	.67	52
116	CSD+[4]	I				166	D+[15]	B	90	.67	52
117	CSD+[5]	I				167	PS+	O	40	.04	40
118	CSD+[6]	I				168	PELCH-	I			
119	CSD+[7]	I									
120	CSD+[8]	I									
121	CSD+[9]	I									
122	CSD+[10]	I									
123	CSD+[11]	I									
124	CSD+[12]	I									
125	CSD+[14]	I									
126	CSD+[13]	I									
127	VSS										
128	CSD+[15]	I									
129	CSD+[16]	I									
130	CSD+[17]	I									
131	CSD+[18]	I									
132	CSD+[19]	I									
133	CSD+[20]	I									
134	CSD+[21]	I									
135	CSD+[22]	I									
136	CSD+[23]	I									
137	VDD										
138	CSD+[24]	I									
139	CSD+[25]	I									
140	CSD+[26]	I									
141	CSD+[27]	I									
142	CSD+[28]	I									
143	CSD+[30]	I									
144	CSD+[29]	I									
145	CSD+[31]	I									
146	OFFBDSCA+	I									
147	VSS										
148	YOGICS+	I									
149	UCSIZE+	I									
150	D+[1]	B	90	.67	52						

where: B = Bidirectional
B* = Internal Feedback
O = Output
I = Input

Table 3-22. Processor Chip Pad Listing

Pin Number	Signal Name	Type	Input Signal Name	Output Signal Name	Tristate Signal Name	Enable Signal Name
1	VSS					
2	MPV-	I	iMPV-			b2preBPON-
3	MP-	O		iMP-	b2YOGI_OE-	disIN8+
4	DB2DE-	B *	bOEBP2D-	OEBP2D-	b3YOGI_OE-	b3YOGI_OE-
5	D2DBE-	B *	bOED2BP-	OED2BP-	b3YOGI_OE-	b3YOGI_OE-
6	OEAD-	O		iOEAD-	b3YOGI_OE-	disIN6+
7	LADR-	B *	bLADR-	iLADR-	b3YOGI_OE-	b3YOGI_OE-
8	QMOE-	I	QMPOE-			b1preBPON-
9	MPOE+	O		iMPOE+	b3YOGI_OE-	disIN6+
10	GIO+[0]	B	GI+[0]	GO+[0]	OEGIO-	qienGIO-
11	VDD					
12	GIO+[1]	B	GI+[1]	GO+[1]	OEGIO-	qienGIO-
13	GIO+[2]	B	GI+[2]	GO+[2]	OEGIO-	qienGIO-
14	GIO+[3]	B	GI+[3]	GO+[3]	OEGIO-	qienGIO-
15	GIO+[4]	B	GI+[4]	GO+[4]	OEGIO-	qienGIO-
16	GIO+[5]	B	GI+[5]	GO+[5]	OEGIO-	qienGIO-
17	GIO+[7]	B	GI+[7]	GO+[7]	OEGIO-	qienGIO-
18	GIO+[6]	B	GI+[6]	GO+[6]	OEGIO-	qienGIO-
19	GIO+[8]	B	GI+[8]	GO+[8]	OEGIO-	qienGIO-
20	GIO+[10]	B	GI+[10]	GO+[10]	OEGIO_HI6-	qienGIO-
21	VSS					
22	GIO+[9]	B	GI+[9]	GO+[9]	OEGIO-	qienGIO-
23	GIO+[11]	B	GI+[11]	GO+[11]	OEGIO_HI6-	qienGIO-
24	GIO+[13]	B	GI+[13]	GO+[13]	OEGIO_HI6-	qienGIO-
25	GIO+[12]	B	GI+[12]	GO+[12]	OEGIO_HI6-	qienGIO-
26	GIO+[14]	B	GI+[14]	GO+[14]	OEGIO_HI6-	qienGIO-
27	GIO+[15]	B	GI+[15]	GO+[15]	OEGIO_HI6-	qienGIO-
28	BRMOE-	O		BROMOE-	b3YOGI_OE-	disIN6+
29	BOOT-	O		BRAM_AC-	b3YOGI_OE-	disIN6+
30	RAMOE-	O		iRAMOE-	b3YOGI_OE-	disIN6+
31	VDD					
32	MAPWE-	O		RAMWE-	b3YOGI_OE-	disIN6+
33	XTEST+	O		TEST+	b2YOGI_OE-	disIN8+
34	N+[0]	O		iN+[0]	b3YOGI_OE-	disIN7+
35	N+[1]	O		iN+[1]	b3YOGI_OE-	disIN7+
36	N+[2]	O		iN+[2]	b3YOGI_OE-	disIN7+
37	N+[3]	O		iN+[3]	b3YOGI_OE-	disIN7+
38	MLOST+	I	iMLOST+			b2preBPON-
39	SLAVE+	I	iSLAVE+			b1preBPON-
40	FETCH2B+	O		IFTCH+	b2YOGI_OE-	disIN5+
41	CRS+	O		iCRS+	b2YOGI_OE-	disIN5+
42	RNI2B+	O		iRNI+	b2YOGI_OE-	disIN5+
43	VSS					
44	PSCHOD+	O		iSCHOD+	b2YOGI_OE-	disIN5+
45	CTRN2B+	O		iCPUTURN+	b2YOGI_OE-	disIN5+
46	IAK2B+	O		iIAK+	b2YOGI_OE-	disIN5+
47	INTRQ+	I	iINTRQ+			b1preBPON-
48	PG+[0]	O		iPG+[0]	OEPG-	disIN3+
49	PG+[1]	O		iPG+[1]	OEPG-	disIN3+
50	PG+[2]	O		iPG+[2]	OEPG-	disIN3+

where: B = Bidirectional
B* = Internal Feedback
O = Output
I = Input

dis = Input always disabled
en = Input always enabled

Table 3-22. Processor Chip Pad Listing (continued)

Pin Number	Signal Name	Type	Input Signal Name	Output Signal Name	Tristate Signal Name	Enable Signal Name
51	PG+[3]	O		iPG+[3]	OEPG-	disIN3+
52	PG+[4]	O		iPG+[4]	OEPG-	disIN3+
53	VDD					
54	IOGO+	O		iIOGO+	b2YOGI_OE-	disIN5+
55	IORQ+	I	iIORQ+			b1preBPON-
56	MRQ+	I	iMRQ+			b1preBPON-
57	REF-	O		iREF-	b1YOGI_OE-	disIN4+
58	RAS+	I	iRAS+			enRAS-
59	BDSEL-	I	SEL-			b1preBPON-
60	GO-	O		iGO-	b1YOGI_OE-	disIN4+
61	MDISL+	O		MEMDISL+	b1YOGI_OE-	disIN4+
62	BUSY+	O		BUSY_OUT+	b1YOGI_OE-	disIN4+
63	VSS					
64	ACK+	I	iACK+			b1preBPON-
65	STVLD+	O		VAL2B+	b1YOGI_OE-	disIN4+
66	MGO+	O		iMGO+	b1YOGI_OE-	disIN4+
67	BWE-	B	BRD_WE-	iWEL-	iOEAD-	qenMPOE-
68	MEMGO+	I	iMEMGO+			b1preBPON-
69	MAP+[0]	O		iMAP+[0]	OEMAP-	disIN2+
70	MAP+[1]	O		iMAP+[1]	OEMAP-	disIN2+
71	MAP+[2]	O		iMAP+[2]	OEMAP-	disIN2+
72	MAP+[3]	O		iMAP+[3]	OEMAP-	disIN2+
73	VDD					
74	MAP+[4]	O		iMAP+[4]	OEMAP-	disIN2+
75	RDPEA-	O		ePER1gio-	b2YOGI_OE-	disIN8+
76	LLEDR+	O		IgioLED+	b2YOGI_OE-	disIN8+
77	ESR-	O		eSRgio-	b2YOGI_OE-	disIN8+
78	ECIL-	O		eCILgio-	b2YOGI_OE-	disIN8+
79	VSS					
80	SPON+	I	iSPON+			enIN2-
81	PFW+	I	iPFW+			b2preBPON-
82	EC+	I	ECYC+			enIN2-
83	CSA+[1]	O		CSAL+[1]	b0YOGI_OE-	disIN0+
84	CSA+[0]	O		CSAL+[0]	b0YOGI_OE-	disIN0+
85	VSS					
86	CSA+[2]	O		CSAL+[2]	b0YOGI_OE-	disIN0+
87	CSA+[3]	O		CSAL+[3]	b0YOGI_OE-	disIN0+
88	CSA+[4]	O		CSAL+[4]	b0YOGI_OE-	disIN0+
89	CSA+[5]	O		CSAL+[5]	b0YOGI_OE-	disIN0+
90	CSA+[6]	O		CSAL+[6]	b0YOGI_OE-	disIN0+
91	CSA+[7]	O		CSAL+[7]	b0YOGI_OE-	disIN0+
92	VDD					
93	CSA+[8]	O		CSAL+[8]	b0YOGI_OE-	disIN0+
94	CSA+[9]	O		CSAL+[9]	b0YOGI_OE-	disIN0+
95	CSA+[10]	O		CSAL+[10]	b0YOGI_OE-	disIN0+
96	CSA+[11]	O		CSAL+[11]	b0YOGI_OE-	disIN0+
97	CSA+[12]	O		CSAL+[12]	b0YOGI_OE-	disIN0+
98	CSA+[13]	O		CSAL+[13]	b0YOGI_OE-	disIN0+
99	IORST-	O		IO_RST-	b1YOGI_OE-	disIN1+
100	SHFTSC+	I	SHFT_SC+			b2preBPON-

where: B = Bidirectional
B* = Internal Feedback
O = Output
I = Input
dis = Input always disabled
en = Input always enabled

Table 3-22. Processor Chip Pad Listing (continued)

Pin Number	Signal Name	Type	Input Signal Name	Output Signal Name	Tristate Signal Name	Enable Signal Name
101	SC+	I	SC2B+			enIN1-
102	PPCLOCK+	O		IO_CLOCKb+	b1YOGI_OE-	disIN1+
103	YCCLK-	I	iCCLK-			enIN1-
104	CLOCK-	I	iCLOCK-			enIN1-
105	FCLK+	I	FC+			enIN1-
106	VSS					
107	FREEZE-	O		iFREEZE-	b1YOGI_OE-	disIN1+
108	PSCLK+	O		PRE_SCLK+	b1YOGI_OE-	disIN1+
109	PLC-	O		PRELCb-	b1YOGI_OE-	disIN1+
110	PFCLK+	O		iCLOCK+	b1YOGI_OE-	disIN1+
111	CSD+[0]	I	iCSD+[0]			b1qenUMI-
112	CSD+[1]	I	iCSD+[1]			b1qenUMI-
113	CSD+[2]	I	iCSD+[2]			b1qenUMI-
114	CSD+[3]	I	iCSD+[3]			b1qenUMI-
115	VDD					
116	CSD+[4]	I	iCSD+[4]			b1qenUMI-
117	CSD+[5]	I	iCSD+[5]			b1qenUMI-
118	CSD+[6]	I	iCSD+[6]			b1qenUMI-
119	CSD+[7]	I	iCSD+[7]			b1qenUMI-
120	CSD+[8]	I	iCSD+[8]			b1qenUMI-
121	CSD+[9]	I	iCSD+[9]			b1qenUMI-
122	CSD+[10]	I	iCSD+[10]			b1qenUMI-
123	CSD+[11]	I	iCSD+[11]			b1qenUMI-
124	CSD+[12]	I	iCSD+[12]			b1qenUMI-
125	CSD+[14]	I	iCSD+[14]			b1qenUMI-
126	CSD+[13]	I	iCSD+[13]			b1qenUMI-
127	VSS					
128	CSD+[15]	I	iCSD+[15]			b1qenUMI-
129	CSD+[16]	I	iCSD+[16]			b0qenUMI-
130	CSD+[17]	I	iCSD+[17]			b0qenUMI-
131	CSD+[18]	I	iCSD+[18]			b0qenUMI-
132	CSD+[19]	I	iCSD+[19]			b0qenUMI-
133	CSD+[20]	I	iCSD+[20]			b0qenUMI-
134	CSD+[21]	I	iCSD+[21]			b0qenUMI-
135	CSD+[22]	I	iCSD+[22]			b0qenUMI-
136	CSD+[23]	I	iCSD+[23]			b0qenUMI-
137	VDD					
138	CSD+[24]	I	iCSD+[24]			b0qenUMI-
139	CSD+[25]	I	iCSD+[25]			b0qenUMI-
140	CSD+[26]	I	iCSD+[26]			b0qenUMI-
141	CSD+[27]	I	iCSD+[27]			b0qenUMI-
142	CSD+[28]	I	iCSD+[28]			b0qenUMI-
143	CSD+[30]	I	iCSD+[30]			b0qenUMI-
144	CSD+[29]	I	iCSD+[29]			b0qenUMI-
145	CSD+[31]	I	iCSD+[31]			b0qenUMI-
146	OFFBDSCA+	I				b2preBPON-
147	VSS					
148	YOGICS+	I				b2preBPON-
149	UCSIZE+	I				b2preBPON-
150	D+[1]	B				qienD-

where: B = Bidirectional
B* = Internal Feedback
O = Output
I = Input
dis = Input always disabled
en = Input always enabled

Table 3-22. Processor Chip Pad Listing (continued)

Pin Number	Signal Name	Type	Input Signal Name	Output Signal Name	Tristate Signal Name	Enable Signal Name
151	D+[0]	B	DI+[0]	DO+[0]	OED-	qienD-
152	D+[2]	B	DI+[2]	DO+[2]	OED-	qienD-
153	D+[3]	B	DI+[3]	DO+[3]	OED-	qienD-
154	D+[4]	B	DI+[4]	DO+[4]	OED-	qienD-
155	D+[5]	B	DI+[5]	DO+[5]	OED-	qienD-
156	D+[6]	B	DI+[6]	DO+[6]	OED-	qienD-
157	VDD					
158	D+[7]	B	DI+[7]	DO+[7]	OED-	qienD-
159	D+[8]	B	DI+[8]	DO+[8]	OED-	qienD-
160	D+[9]	B	DI+[9]	DO+[9]	OED-	qienD-
161	D+[10]	B	DI+[10]	DO+[10]	OED-	qienD-
162	D+[11]	B	DI+[11]	DO+[11]	OED-	qienD-
163	D+[12]	B	DI+[12]	DO+[12]	OED-	qienD-
164	D+[13]	B	DI+[13]	DO+[13]	OED-	qienD-
165	D+[14]	B	DI+[14]	DO+[14]	OED-	qienD-
166	D+[15]	B	DI+[15]	DO+[15]	OED-	qienD-
167	PS+	O		iPS+	b2YOGI_OE-	disIN8+
168	PELCH-	I	PE+			b2preBPON-

where: B = Bidirectional
B* = Internal Feedback
O = Output
I = Input
dis = Input always disabled
en = Input always enabled

4

A400 Memory Control

Introduction

The A400 board contains a memory controller and 512k bytes of user dynamic RAM (DRAM). Facilities have been included to control up to four optional array cards. The A400 board also has 2k bytes of boot RAM and 32k bytes of boot EPROM.

The memory controller supports up to 32M bytes of main memory (RAM). It supports parity memory only. Refer to the Memory Array Chapter for detailed information on the operation of the memory array cards.

System Environment

A minimum memory system consists of just the A400 board with its 512k bytes of on-board memory. The memory array cards (if any) are placed in the slots directly above (higher priority) the A400 board. A memory frontplane connector is used to connect the address bus between the A400 board and the array cards.

For the frontplane connection, the 50-pin edge-connector on the front of the A400 board is used (the smaller edge-connector on the front of the A400 board is used for the on-board I/O cable).

Memory System Functional Characteristics

Basic Operation

The memory system serves as the main memory of the A400 computer. The memory is dynamically mapped, which provides the ability to access more than 32k words of 16-bit data. Map RAMs are used to generate the physical address of data to be accessed during a memory cycle. Mapping extends the 15-bit address bus (which can access up to 32k words of memory) to a 24-bit address bus to access up to 16M words (32M bytes) of memory. The memory array cards are word addressable.

Memory accesses can be initiated by either the processor or by an I/O device using DMA. Accesses can be read or write protected by two bits which are stored in the map RAMs. Thus, a processor access to protected memory causes an interrupt to occur and the access is stopped and memory protected.

An I/O device using DMA can access protected memory, however. This is true for either a read or write access.

The detection of a parity error on a read causes the assertion of a parity error interrupt signal on the backplane. This signal is received by the processor when it initiated the access, and also by the I/O card when it initiated the access.

Data Capacity

The format of the data stored in memory is 16-bit words. When data is read, 16 bits at a time are transferred directly to the backplane from the array cards.

Memory system capacity is a function of the number of address lines available. Since there are 24 address lines, 16M words or 32M bytes of memory can be addressed. The amount of memory present in the system depends on the number and type of array cards installed. Due to physical limitations, a maximum of four array cards can be used in the memory system.

Memory Addressing

The A400 on-board DRAM exists in the physical *word* address space from 0 to 256k. Memory array cards are needed to extend memory beyond the 512k bytes.

When adding array cards to the memory system, there is no need to physically identify the array cards (that is, jumper or switch settings to set recognition of physical address space) when installing them in the system. The arrays incorporate a module self-configuring scheme which automatically designates the array card next to the memory controller (the on-board memory) as the first module and successively designates the remaining modules in ascending order going away from the memory controller. The beginning of memory is, therefore, on the A400 board and the end of memory is on the array card farthest from the A400 board. Refer to the Memory Array Chapter for a complete description of memory array configuration.

Data Transfer Rate

A typical memory access to main memory occurs within a minimum of two SCLK (clock signal) cycles. Therefore, the maximum data transfer rate is dependent on the maximum frequency of SCLK. The period of SCLK for the A400 is 227 nanoseconds. The fastest data transfer rate possible, taking into account refresh cycles, is the result of the following expression:

$$\text{Access Rate} = \frac{17{,}078 \text{ byte accesses}}{3.99305 \text{ milliseconds}} = 4.28 \text{ Mbytes/second}$$

This was calculated by determining the period between refresh requests and multiplying by 256 (15.6μs x 256 = 3.993056ms) to get the window in which 256 refresh cycles will occur. This number is divided by 227ns to get the number of SCLK cycles in that time frame (3.993056ms/227ns = 17590). 512 SCLK cycles are then subtracted from this number for 256 refresh cycles at 2 SCLK cycles each (17590 - 512 = 17078). A word is accessed every 2 SCLK cycles, so a byte is accessed every SCLK cycle. Thus the transfer rate is the number of SCLK cycles divided by the period between 256 refresh cycles.

Interface Requirements

The A400 memory controller interfaces to the processor chip, optional memory array cards, and I/O through the backplane and memory array frontplane. Interaction with I/O occurs only across the backplane.

Memory Frontplane Interface

The memory controller sends the physical address of a memory access to the memory array card frontplane connector (J1), along with various signals that control the memory access on the array card selected. Each array card is capable of driving its data onto the backplane, and the memory controller samples the frontplane signal PCK– and the backplane data bus to determine if a parity error has occurred. Table 4-1 gives the memory frontplane connector J1 pin assignments. Table 4-2 gives the memory array frontplane signal definitions.

MI/MO Chain

Each array card receives a base address over the frontplane MI chain lines which tell the array card which addresses are recognized by the cards below it in the backplane. The array card adds its size to this value and sends the new value over the MO chain lines which are tied to the MI chain lines for the next array card. Every 128k bytes on a card causes it to add one to the value of the memory chain.

The A400 memory controller sends the value four out over the MO chain to indicate the 512k bytes of memory on the board. Note that to make the memory on the A400 board transparent, that is, unused, this value can be changed to a hardwired 0.

Array Frontplane Handshakes

The array cards receive the handshake signals, for example, DRIVE, CASEN, WRITE, GO, which have the same effect as they do on the memory controller. The array card selected (if any) returns the ACK and PCK signals to the controller, to tell it that the memory exists, and to allow the controller to check the parity of the read data.

Table 4-1. Memory Frontplane Connector J1 Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	2	GND
3	A10–	4	A11–
5	A12–	6	A13–
7	A14–	8	A15–
9	A16–	10	A17–
11	A18–	12	A19–
13	A20–	14	A21–
15	A22–	16	A23–
17	MIO+	18	MO0+
19	MI1+	20	MO1+
21	MI2+	22	MO2+
23	MI3+	24	MO3+
25	GND	26	GND
27	MI4+	28	MO4+
29	MI5+	30	MO5+
31	MI6+	32	MO6+
33	MI7+	34	MO7+
35	PAR–	36	PHXRAS–
37	WRITE+	38	DRIVE–
39	LATCH+	40	CASEN–
41	SPARE	42	PCK–
43	SPARE	44	XTND–
45	REF+	46	ACK–
47	GO+	48	PHX–
49	GND	50	GND

Table 4-2. Frontplane Signal Definitions

Signal Name	Function
ACK–	Acknowledges that an array card recognizes the address. (Open collector)
A[10:23]	Physical address (mapped address)
CASEN–	Enables the array cards to do a CAS.
DRIVE–	Enables the selected array card to drive data onto the data bus.
GO+	J input to the RAS flip-flop on the array cards.
LATCH+	Latches the address and data.
MI[0:7]	Memory Chain In (not used on the memory controller).
MO[0:7]	Memory Chain Out, equal to 4 octal on the A400 board.
PAR–	Parity bit to be written into the parity RAM.
PCK–	Parity Check bit returned on a read. (Open collector)
PHX–	Asserted by the A700 memory controller, not used in A400.
PHXRAS–	Asserted by the A700 memory controller, not used in A400.
REF+	Do a refresh cycle.
WRITE–	Start a write operation.
XTND–	Extend the memory cycle; asserted by array cards, not used in A400.

Backplane Interface

The A400 memory follows the A/L-Series backplane protocols for processor and DMA memory accesses. The memory controller and each array card receive the unmapped portion of the memory address, AB[0:9], whereas only the memory controller receives the map number and page number. The memory controller and the arrays receive and drive their own data.

The A/L-Series backplane uses a 3-line handshake to access memory and status lines to identify the type of memory access taking place and the concluding results of the access. These lines are as follows:

Handshake Signals:

MEMGO– Initiates a memory cycle.
BUSY– Memory is busy and unable to accept a MEMGO–.
VALID– The rising edge of VALID– signals that data is valid on the data bus (memory read). VALID– also occurs with the same timing on a write, but the data bus is not necessarily valid.

Status Signals:

MRQ– Distinguishes between a processor or a DMA access.
MEMDIS– Boot memory accesses assert MEMDIS– along with MEMGO–.
REMEM– Indicates remote memory access, not supported by the A400.
WE– Indicates a write cycle.
MP+ Enables the memory protect function of the memory controller.
PS– Indicates parity sense to determine odd (PS– = logic 1) or even (PS– = logic 0) parity.

All memory cycles are initiated by the assertion of MEMGO on the backplane. The memory controller always responds by asserting the BUSY signal at the beginning of the following short half-cycle (SHC) of SCLK.

In the case of a two-cycle (main memory) access without a conflicting refresh cycle, BUSY is held for one SCLK cycle and is reset at the beginning of the next SHC. In the case of a three-cycle access to boot ROM or RAM without a conflicting refresh cycle, BUSY is held for two SCLK cycles and is reset at the beginning of the second SHC of SCLK.

Memory Data Transfer to I/O

All data transfers to an I/O card occur over the backplane. The memory cycle is initiated by the I/O card and the handshake occurs on the backplane. The 15-bit address sent by I/O is mapped by the memory controller so that I/O can access anywhere in the physical memory space. If a parity error occurs during a memory read access, the parity error interrupt signal is asserted on the backplane and is received by the I/O card. If I/O accesses protected memory, the memory protect interrupt is not asserted and the access is allowed to continue (both read and write). This is not true of memory accesses by the processor.

Memory System Operating Characteristics

Refresh Operations

The characteristics of the dynamic RAMs require memory refreshing for maintaining data. All the rows must be refreshed every four milliseconds for the 256k-bit dynamic RAMs. The refresh operation is transparent in the sense that no handshake signals are asserted (that is, BUSY) when a refresh is executing unless a memory cycle is requested by the assertion of MEMGO. All memory RAMs are refreshed at the same time.

Power Fail Considerations

Whenever power is removed from memory, data present in memory will be lost. Under AC power failure with battery backup operation, the +5M backplane voltage must be maintained at the memory for retention of data.

The +5M backplane voltage powers CCLK and SCLK generation logic as well as the processor chip and the PON buffer and synchronizer so that RAM refresh can continue.

Interrupt Conditions

The memory controller asserts two types of interrupts: memory protect and parity error. Whenever the processor attempts to access memory that is read-protected, the memory protect interrupt is asserted and the access is stopped. The normal handshake sequence is allowed to complete, however, with the memory system outputting all logic 1's onto the backplane data bus.

If the processor attempts a memory write to write-protected memory, the memory protect interrupt is asserted, memory is not altered, and the handshake is allowed to complete. Whenever DMA accesses memory, the access is not inhibited, whether or not it is to protected memory.

Whenever data is accessed from a memory array module and the parity of data is not correct, the parity error line will be asserted to request a parity error interrupt.

Memory System Functional Description

The two basic functions of the memory system are to provide data storage and to control data storage. Data storage is provided by the on-board DRAM and the memory array cards. Control is the function of the memory controller which resides on the A400 board. The memory controller is split between the processor chip and the on-board circuitry. The processor chip provides the control signals which are not timing-critical while the on-board circuitry provides timing-critical signals. The memory controller is responsible for the following functions:

- Generate the handshake signals for the backplane (BUSY, VALID)
- Latch data and address during memory cycles
- Generate interrupt signals (MPV, PE)
- Arbitrate memory and refresh cycles
- Generate read strobes for memory array cards
- Protect memory during illegal accesses
- Access loader and front panel firmware
- Inhibit array cards during protected accesses
- Maintain memory data during a power failure
- Verify that the physical address indeed accesses an existent array card and if not, drive all ones onto the backplane
- Determine whether the requested memory cycle should occur in two or three SCLK cycles

Mapping System

The mapping system is the means by which the memory controller provides a physical address equal to the maximum possible size of main memory. The mapping system is composed of two high-speed static RAMs which convert (or map) the logical address received from the backplane into a 24-bit address. There are 32 maps with 32 address locations per map that can address up to 32M bytes of physical memory.

In the address mapping operation, a 15-bit logical address word is divided so the lower 10 bits are used directly, where bit 0 of the backplane logical address is bit 0 of the physical address. The upper five bits of the backplane address are used in combination with five bits from the address extension bus (AE[0:4]) to select a map RAM location containing the upper 14 bits of the extended physical address of the memory location to be accessed (along with the read and write protect bits). The 14-bit mapped address is sent to the array cards over the frontplane, with the array cards receiving the lower 10 bits directly off the backplane.

Two 2k x 8 SRAMs provide 1k words of Boot RAM and 1k words for the Map RAMs. The Map RAMs are loaded from the processor chip GIO-Bus under control of the processor only. The memory accesses are timed so that the processor may access (or change) the map contents during a memory cycle.

Map Address Latch

During a memory access, the upper five bits of the logical address on the backplane access the map RAMs and the extended address (made up of the mapped upper 14 bits of the physical address and the latched lower 10 bits of the logical address) is sent to the memory arrays. The upper 14 bits are sent from the memory controller and the lower 10 bits are latched on each array card. After the assertion of MEMGO is complete, the logical address is no longer valid, but the extended address must remain valid for the remainder of the memory cycle. This is necessary to keep the appropriate array card selected for driving the requested data onto the backplane. The extended address is, thus, latched on the memory controller at the end of MEMGO so that the memory access can complete. At the same time, this frees the Map RAMs so that they can be accessed by the processor during the memory cycle if desired. In this way the processor can modify the contents of the Map RAMs during a memory cycle.

Read/Write Protect

Two bits of the Map RAMs are used to store the read/write protect status bits which control the access of protected areas of memory. These bits are written at the same time as the address bits, and are accessed in the same manner. During any protected processor access to memory, these bits, if set, prevent a memory access from occurring.

The mechanism by which this occurs is as follows: As the logical address accesses the map address RAMs, it also accesses the read/write protect bits. If the appropriate bit is set, then the requested read or write is inhibited. In the case of a write cycle, the aborted write does not cause any change of data in main memory. In the case of a read cycle, the aborted read causes the memory controller to drive all ones (octal 177777) onto the backplane data bus. However, a read can occur from write-protected memory and a write can occur to read-protected memory. In the case of a DMA access by a peripheral device, the protect bits are ignored.

Note that the map RAMs must be initialized by the processor before the main memory system can be used.

Controller RAM and PROM

The memory controller contains 1k words of static RAM (refresh not needed) and 8k words of PROM space. The RAM is used for bootstrap loading, diagnostic purposes, and for extra processor scratch pad registers. It shares 2k SRAM parts with the Map RAM. The PROM is used for storage of the VCP code, which includes boot loaders.

The 1k words of static boot RAM are accessed by the assertion of MEMDIS- on the backplane and the assertion of a base page address (0-1777, octal) on the PG-Bus and Map-Bus. The Map-Bus is the high order bus. The address is also driven on the AB-Bus on the backplane for visibility. The processor chip decodes the address and MEMDIS to assert BRMOE- which enables the boot PROMs. Reading or writing data into the RAMs is indicated by the WE signal on the backplane. The signal BOOT- is used to distinguish boot RAM from map accesses.

The boot PROMs are accessed by asserting MEMDIS- on the backplane along with an address equal to or greater than 8k (2000 octal) on the address bus.

Memory accesses to the RAM and boot PROM are the same as those to main memory with the exception of the assertion of MEMDIS- on the backplane and the access is a three-cycle access instead of two. Also, since the address may select one of the array cards in the main memory array, the controller inhibits any array card from driving the backplane data bus during a boot access. When the memory controller performs an access to either boot PROM or RAM it needs the three-cycle access because the PROMs have a slower access time than the DRAMs in main memory.

Memory Interrupt Registers

The memory interrupt registers provide information on memory protect violations and parity errors. The parity error registers (two 16-bit registers) contain the 24-bit physical address of the last parity error and are split between the processor chip and the board. The memory protect violation register contains the logical address of the instruction that caused a memory protect interrupt and resides in the processor chip. The parity error register on the board is read into the processor chip through the GIO-bus.

Parity Generation and Detection

The parity generator on the A400 monitors the data on the backplane and generates a parity bit for both read and write cycles. For a write cycle, the parity bit is generated and sent to every array card over the frontplane shortly after the data is valid on the backplane.

As the write cycle continues, the appropriate memory array card is selected and the parity bit is written into the parity RAM along with the 16-bit data word on the same array card.

Read parity detection is done using the same parity generator as used for a write. As the array card drives the requested data onto the backplane, the parity generator monitors it for correctness. At the same time, the parity bit from the array card is sent to the memory controller over the frontplane. The parity generator compares the check bit with the data on the backplane to ensure proper parity. If an error has occurred, the offending physical address is latched and the parity error signal, PE–, is asserted on the backplane after the release of VALID–. Also, the parity LED on the array card which contains the parity error is extinguished.

To summarize, the memory controller asserts the PE– signal whenever a parity error on the A400 board or one of the array cards is detected. This indicates that accessed data is in error. The faulty card will have its green parity LED extinguished.

Refresh Circuitry

Main memory is composed of dynamic RAMs which require periodic refreshing for the retention of data. The memory controller schedules and performs the refresh function on all array cards simultaneously.

Refresh accesses are interleaved between requested memory cycles. If a memory cycle is in progress when a refresh cycle becomes due, the refresh waits until the pending memory cycle completes. On the other hand, if a refresh is executing and a memory cycle is requested, the memory cycle is extended while the refresh completes. The requested memory cycle is then executed. A refresh request and a MEMGO request are kept from exactly colliding by starting the cycles on different edges of SCLK. A refresh cycle is started at the leading edge of the LHC while a MEMGO request is started at the leading edge of the SHC.

The refresh rate is determined by CCLK. The processor chip generates the refresh request signal for the memory system.

When AC power is removed from the computer system and there is a battery back–up system installed, the memory controller still refreshes memory using circuitry powered by +5M.

Memory Control Theory of Operation

References are made throughout the text to the schematics located at the end of Chapter 2. The integrated circuits (chips) are referenced by their U-numbers and schematic locations. For example, U405 (13C) means chip U405 on schematic sheet number 1 is located by coordinates 13 and C; where the horizontal grid on sheet number 1 is numbered 10, 11, etc. and on sheet number 2 it is numbered 20, 21, etc.

The A400 memory controller circuitry exists partially in the processor chip and partially on the board. When appropriate you will be referred to the Processor Chip Chapter for a detailed description of the memory control circuitry that resides in the processor chip.

Data and Address Buses

The processor and memory control/array section of the board are organized around two major buses, the GIO-bus and the D-bus. These buses provide most address and data paths. Two minor buses, the PG-bus and the MAP-bus, complete the address paths for the processor and memory controller. These buses, along with control signals, interact with off-board resources. Refer to Chapter 2 for a detailed description of the function and use of each bus.

Memory Accesses

A memory cycle can be initiated by an I/O card doing DMA, or by the processor doing an access or an IAK cycle. Processor accesses fall into two categories: normal accesses and boot memory accesses. Normal processor memory accesses are always mapped, and boot memory accesses are never mapped. Normal processor accesses can be either read protected or write protected (or both) on a page-by-page basis. Boot memory accesses and DMA accesses are not protected. The A400 memory has a 16-bit data format, with a 17th bit (parity bit) used to detect single-bit errors in RAM accesses. The memory takes two cycles to do a main memory access, and three cycles to do a boot memory access.

Two-Cycle Main Memory Access

The two-cycle main memory access to the memory array cards is shown in the timing diagram of Figure 4-1. MEMGO is asserted on the backplane during the long half-cycle (LHC) of SCLK. This signifies the start of a memory access.

The assertion of MEMGO indicates that BUSY should be asserted, which occurs during the first short half-cycle (SHC) after the assertion of MEMGO. If there is no refresh cycle in progress, VALID is also asserted. VALID is asserted one or two SCLK cycles later if a refresh cycle is in progress.

The asserted VALID allows BUSY to be reset on the next SHC of SCLK. Thus, BUSY and VALID are asserted for one SCLK cycle if the access does not collide with a refresh cycle. If the access does collide with a refresh cycle, BUSY will be extended to two or three SCLK cycles and VALID will remain asserted for just one SCLK cycle, the last one of the access. After BUSY resets, VALID is reset. This completes the two-cycle backplane handshake.

Three-Cycle Boot Memory Access

The three-cycle boot access timing is shown Figure 4-2. If an access to boot RAM or ROM is initiated, the MEMDIS signal is asserted with MEMGO. The MEMDIS signal indicates that a three-cycle access should occur instead of a two-cycle access.

During a three-cycle access, BUSY is asserted as in a two-cycle access, but extends for two SCLK cycles instead of one. VALID is held off until the second SCLK cycle of BUSY.

When VALID is set, BUSY resets on the next rising edge of SCLK– and VALID resets shortly thereafter as described in the description of the two-cycle access. Thus, BUSY is asserted for two SCLK cycles and VALID is asserted for one cycle.

A collision with refresh will extend the access to four SCLK cycles.

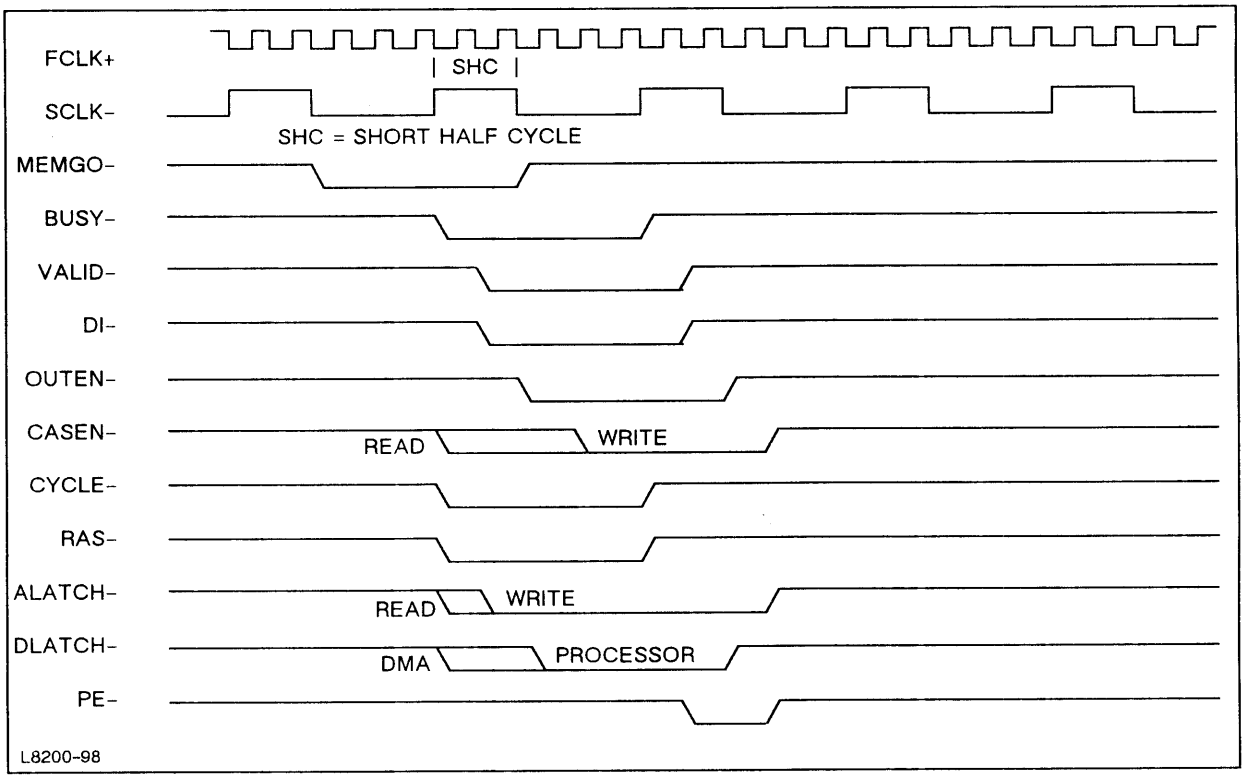


Figure 4-1. Two-Cycle Main Memory Access

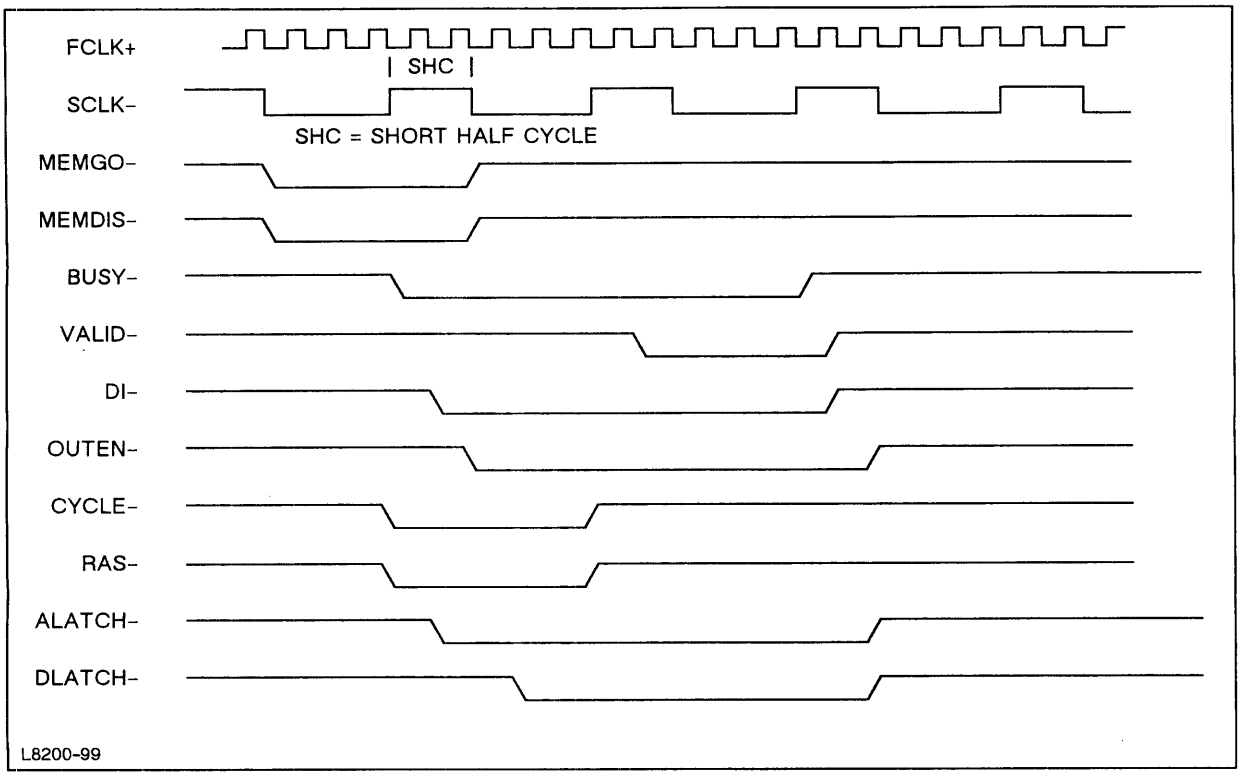


Figure 4-2. Three-Cycle Boot Memory Access

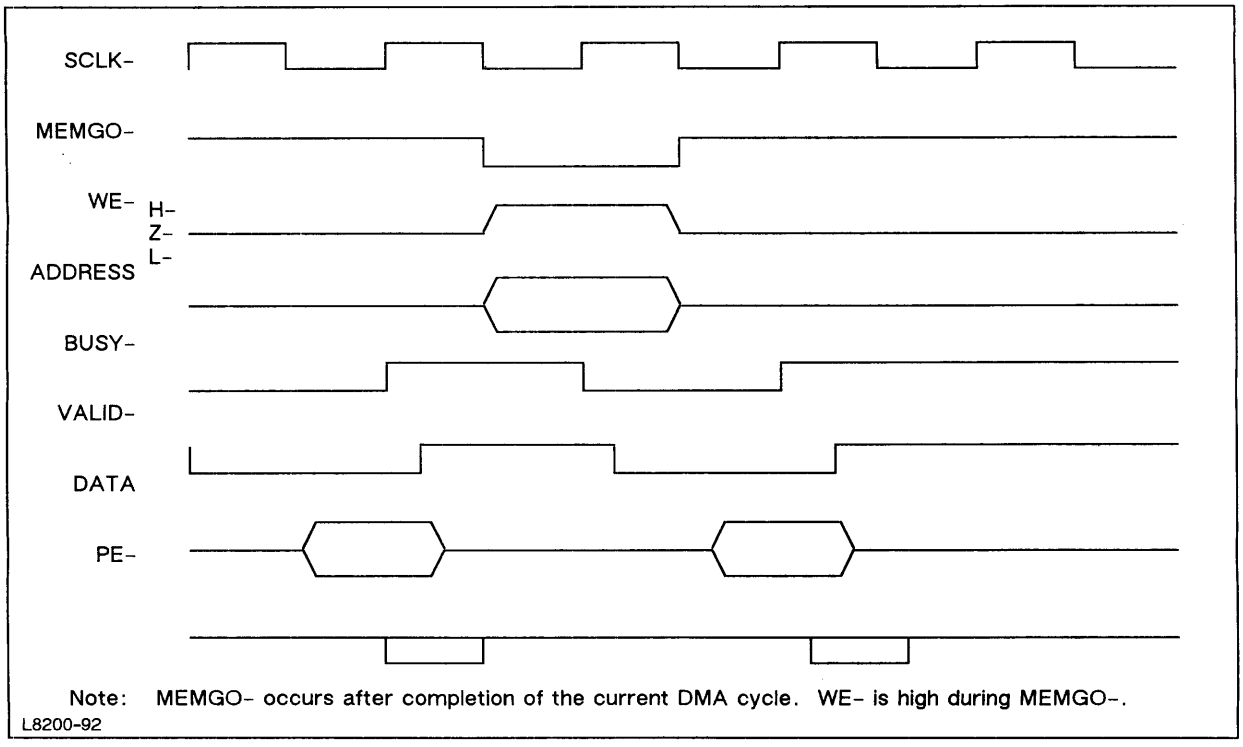


Figure 4-3. Backplane Signals for Memory Read

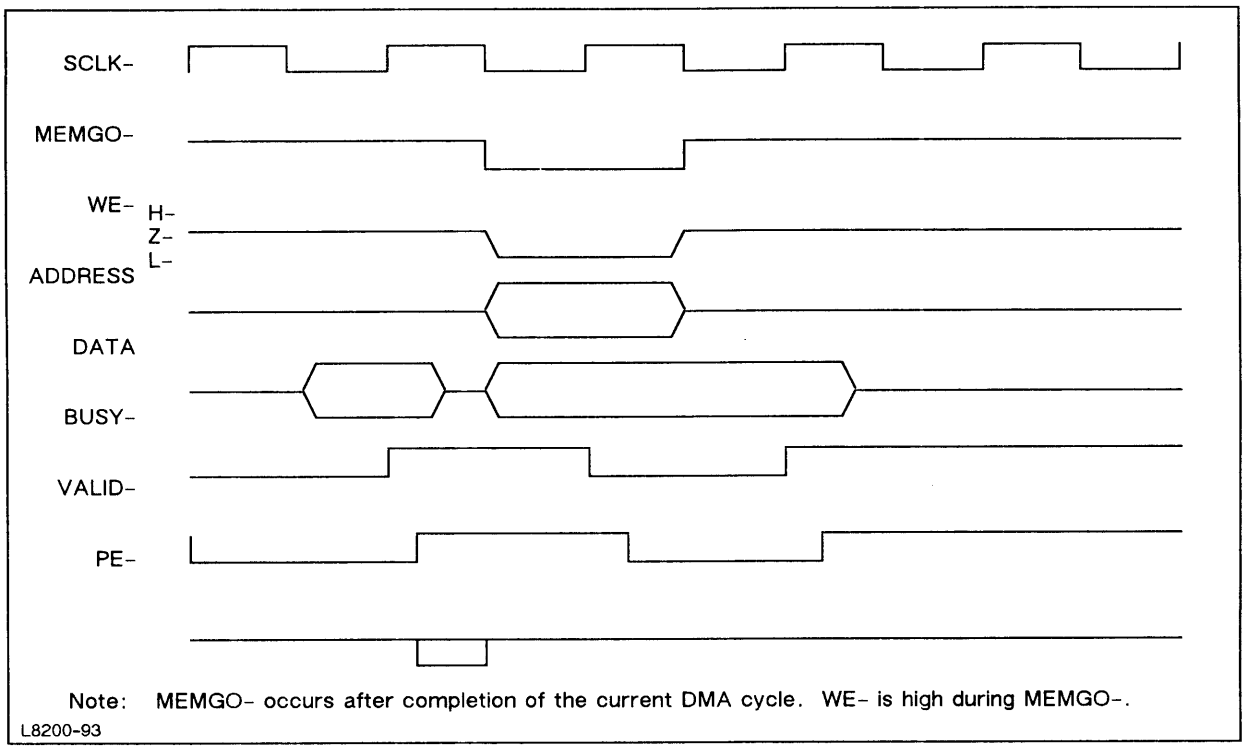


Figure 4-4. Backplane Signals For Memory Write

Offset Address Latch and GIO-Bus Usage During a Memory Access

For a processor memory access, the GIO-bus provides a data path for the lower ten bits of data (or address bits) to their latch for the backplane. The latch at U709 (37B) drives AB+[0:9]. U709 is loaded under control of the LADR- signal from the processor chip. The OEAD- signal, from the processor chip, enables the output of the latch onto the backplane. The GIO-bus is then free for use by the SRAMs so that they can output the extended physical address and the read/write protect bits at the end of the LHC and the beginning of the SHC. The SRAMs are output enabled by RAMOE-. If the cycle is a boot RAM access, then the data from the SRAMs is boot RAM data instead of MAP information and is wrapped around to the D-bus by the processor chip. The processor chip also latches the data on a boot RAM access so that it can free the GIO-bus for use once BUSY asserts.

LATCH- is used by U906 (52A) and U601 (52B), to latch the extended physical address and the read/write protect bits from the GIO-bus during a normal DRAM access. This occurs about midway through the SHC during the assertion of MEMGO. (During a boot access the read/write protect bits are ignored). The extended physical address is driven on the A-[10:23] lines on the frontplane for use by the memory arrays. The read/write protect bits are also latched by U906 and U601 for use by the memory controller. (The output of U906 and U601 can be tri-stated for test by asserting TEST1+). The GIO-bus is then free at the end of the SHC so it can be used for micromachine off-chip register accesses. For an I/O memory access, the GIO-bus usage is the same except for the loading of the lower ten bits of address into their latch.

Self-Configuration Map Select

DMA self-configurations, by definition, originate in Map 0. This is ensured by the signal SELFC–, which is asserted on the backplane during an I/O self-configuration or interrupt acknowledge cycle. The assertion of SELFC– forces the map RAMS to access Map 0.

I/O interrupt trap cell memory references are also asserted with SELFC– low, ensuring that the trap cell reference comes out of logical page 0 which should be mapped to physical page 0.

General Control Signals for Memory Access

Several signals control the general nature of a user memory access. These signals are MEMGO–, BUSY–, VALID–, and LATCH+. MEMGO– and BUSY– are generated by the processor chip. The assertion of MEMGO– requests a memory access cycle. If memory is busy with a refresh cycle, it will latch the request and execute it one to three cycles later.

BUSY– is asserted by the memory controller in response to MEMGO–. It stays asserted until the requested memory access is complete. MEMGO– is asserted during a LHC. BUSY– is asserted during the following SHC. During the SHC, LATCH+ is also asserted by the memory controller to capture all needed information to execute the request before the state changes. Information, for example the requested address, read or write cycle information, memory protect information, and data to be written (if it is a write cycle), is captured on the assertion of LATCH+.

The assertion of BUSY+ by the processor chip is inverted at U1012 (27C) to produce BBUSY–. This signal is NOT-ANDed with SHFTSC+ at U1105 (27C) to produce STRTL+. SHFTSC+ is a version of SC+ that has been shifted at U1408 a nominal 42 ns. SHFTSC+ also goes to the processor chip to be used for internal control.

SHFTSC+ sets the leading edge of STRTL+ which drives NOR (U1105, 28C) and OR (U1103, 28D) gates to produce LATCH– and LATCH+, respectively. The other input to the NOR and OR gates is SECND+. SECND+ is BUSY+ shifted one SHC at U1409 (26C). The deassertion of SECND+ determines the trailing edge of LATCH. The trailing edge of LATCH occurs off the trailing edge of the last SHC which is the end of a memory access.

VALID– is generated by U1012 (27C), with two of its outputs tied together to increase the drive. This is done to minimize the rise time at the end of a cycle when VALID– is deasserted. By minimizing the rise time, the uncertainty of where the position of the rising edge of VALID– occurs is limited. This means that the returned data on a read does not have to be valid for as long or as early.

VALID- is generated by VALID+ which is generated by a JK flip-flop, U1203 (26C), for one SCLK cycle on the last cycle of the access. The placement of VALID+ in time is controlled by CLKVLD-. This clock is produced by the delay line U1408 off of SC+ and is nominally skewed from SC+ by 35 ns. This time was picked for the placement of the rising edge of VALID-. The cycle in which VALID- is to be asserted is picked by the processor chip through the assertion of STVLD+. The processor chip has uncontrollable skew which inhibits accurate placement of VALID- in time, however, the processor chip can determine the cycle in which to assert VALID. Thus the processor chip picks the SCLK cycle, and the board determines the timing of VALID-.

On-Board Memory (DRAM) Description

The on-board memory array consists of 17 256k x 1 Dynamic RAM (DRAM) chips. They are located on schematics 6 and 7. These parts make up a 256k word (512k byte) memory space with one parity bit. The on-board DRAM is controlled by the RAS, CAS, and WRITE inputs. These lines determine the address accessed and the direction of data flow. The 256k locations in each DRAM, are accessed through 18 address bits which are multiplexed onto 9 pins. The RAS signal indicates when the "row" address is valid while the CAS signal indicates when the "column" address is valid. The WRITE input is asserted when data is to be input into the DRAM.

DRAM Control

An on-board DRAM access is started by the assertion of GO+ (buffered GO- from the processor chip) before the falling edge of SC+ (beginning of the SHC). GO+ is asserted over the memory frontplane, for a refresh cycle, or to start a refresh-delayed memory access. The asserted GO+ signal during the falling edge of SC+ clocks a JK flip-flop at U1203 (21A) to produce RAS+ and RAS-. RAS+ is buffered by two drivers, U1508 (23A), to produce URAS- and LRAS-. These signals go through line termination resistors in a resistor pack at U1204 (27A) to produce URRAS- and LRRAS-. URRAS- provides the RAS signal for the DRAMs on bits 8 through 15 and the parity bit while LRRAS- drives the DRAMs on bits 0 through 7. The RAS inputs clock the row address into the DRAM. The RAS lines are split to limit the effect of capacitive loading on the RAS drivers and to provide a more controlled delay in the assertion of RAS.

RAS– drives a delay line, U1408 (23B), to produce GAT– a nominal 23ns later and GOCAS– a nominal 63ns after the assertion of RAS–. GAT– is the timing signal to gate the address transition from the row address to the column address. GAT– is an input into the Memory PLA (MPLA) at U1308 (23C) which controls many of the memory functions. The PLA equations are listed in Table 4-3. GAT– is qualified against SECND, BUSY, MDISL, and REF to control the ROW– and COL– outputs of the MPLA . At the beginning of the SHC which starts a DRAM access, ROW– is asserted to output enable the row address driver, U706 (52B), onto MA+[0:8]. The row address driver receives the address off of the AB-bus on the backplane (AB+[0:9]). The column address is then driven where the row address had been on the MA+[0:8] bits which run through line termination resisters to become RA+[0:8] (59-B) and drive the DRAMs (60B, 70B).

Sixty-three nanoseconds after the assertion of RAS–, GOCAS– is asserted from the delay line. GOCAS– provides the leading edge of the assertion of CAS for a non-refresh access. It is NOT-ANDed with MYCASEN– and BDSEL– at U1104 (25B) to become GCT+. GCT+ drives one input of each of two CAS drivers, U1105 (27B), which produce UCAS– and LCAS–. UCAS– and LCAS– run through a termination resistor in a resistor pack to produce URCAS– and LRCAS–, respectively. These lines drive the CAS inputs to the DRAMs. Again, there are two CAS drivers to minimize the capacitive loading on the drivers. If the memory cycle was a read, data will exit the DRAMs 60 ns later. If the cycle was a write, the RW– line was asserted into the DRAMs and the DRAM output will remain tri-stated.

The two signals that GOCAS– is gated against are BDSEL– and MYCASEN–. BDSEL– is produced by NANDing A–[18:23] and MO2+ at U501 (23D). MO2+ is normally asserted and tells the next memory array card to start at word address 1000000 octal. It is possible to ground MO2+ to disable the onboard DRAM and start the next memory array card at location 0. To assert BDSEL– then, MO2+ is asserted and A–[18:23] are all deasserted to indicate the physical address is in the first 256k user memory locations.

MYCASEN– is generated by the MPLA. It is the qualification of BUSY+, SECND+, MDISL+, PMGO+, WEL–, RPL–, WPL–, and REF–. MYCASEN– indicates that it is a memory cycle (BUSY+ or SECND+), it is not a refresh cycle (REF–), it is not a boot access (MDISL+) and the access is not reading from or writing to protected memory (PMGO+, WPL–, RPL–). REF– is included to ensure that noise on BDSEL– does not toggle GCT+ during battery backup when U501 (which drives BDSEL–) is powered down. RPL– is the read protect bit, WPL– is the write protect bit, and PMGO+ indicates that the access is from the processor and memory protect is on (MP+ is asserted). PMGO+ is generated at latch U106 (42D) from MPMGO+. MPMGO+ is generated by ANDing BMP+ (board MP+) and MGO+ (the processor signal to assert MEMGO– on the backplane) at U201 (23D).

QWRT– is driven by the MPLA to determine whether the cycle is a read or a write. QWRT– is determined by the state of BUSY+, SECND+, REF–, MDISL+, PMGO+, WPL–, and WEL–. When the cycle is a refresh cycle (REF–), QWRT– cannot be asserted. The assertion of QWRT– indicates that the memory cycle (BUSY+, SECND+) is a write cycle (WEL–) and that if the processor requested the write, the memory location is not write protected (PMGO+, WPL–).

QWRT- is NOT-NANDed at U1103 (26B) with BDSEL- to produce BDWRT- which runs through a termination resistor to produce RW-. BDSEL- only allows a write when the address being accessed is on-board. RW- is the signal input to the DRAMs which controls the direction of the access. BDSEL- is qualified against QWRT- outside the MPLA to make sure that RW- is asserted before the CAS lines are asserted on a write cycle. This timing produces an "early write" cycle in which the DRAM outputs remain disabled throughout the cycle.

The MPV- output of the MPLA is asserted when there has been a memory protect violation, that is, the processor has read a read-protected location or written to a write-protected location. MPV- uses PMGO+, WEL-, RPL-, WPL-, and MDISL+ to determine if a memory access was to protected user memory. The terms that produce MPV- also show up in the equations which produce QWRT- to stop an illegal write as well as MYCASEN- and the off-board version, CASEN-, to stop a read when an illegal access occurs.

The MPV- terms also appear in the equations which determine FPDRV-. FPDRV- is sent to the memory array boards in the system to tell them to output their data on a memory read. If there is a read protect violation, FPDRV- is deasserted and the A400 board drives ones output from the processor chip onto the backplane data bus. This happens whether the access was to off-board user memory or not. If the memory protect violation was a write violation, FPDRV- is still deasserted, but the access is turned into a read with the data staying on the accessed board.

FPDRV- is only asserted in a read cycle when SECND+ is asserted and the accessed array (remember the array is off-board) returns an acknowledge signal ACK-. If ACK- is not returned, FPDRV- is not asserted. If BDSEL- on the board is also not asserted, then the processor asserts ones on the D-bus and drives them onto the backplane. This is an A-Series feature that returns 177777 octal when a non-existent memory location is accessed.

The memory array boards work much the same as the on-board memory. Their accesses are started by GO+ and they use CASEN- from the A400 board to determine whether CAS should be asserted or not. The equations for CASEN- are the same as those for MYCASEN except for: (1) REF- must not be asserted for CASEN- to be asserted and (2) MYCASEN is held off on a write to force an early write while CASEN is not. This is because the memory array boards use GO+ and REF+ to do a "RAS-only" refresh cycle which cannot have CAS assert. The A400 board does a "CAS-before-RAS" refresh cycle by NORing the refresh request BDREF+ line with GCT+ (U1105, 27B) described earlier. BDREF+ is the inverted sense of the REF- line generated by the processor. REF- is asserted at the beginning of the LHC. GO+ is also asserted to generate the assertion of RAS+ at the beginning of the following SHC. Thus CAS is asserted, then RAS. This tells the DRAMs on the board to do a refresh cycle and increment their internal refresh address counters which address the DRAM rows during a refresh cycle.

Just as QWRT- was only qualified by BDSEL- for the A400 board to produce an early write cycle, QWRT- is qualified by SECND- to create a late write cycle for the memory array boards. By NOT-ANDing QWRT- and SECND-, the resultant control line, FPWRT-, is not asserted until after CAS has been asserted on the memory array boards. This gives the arrays time to determine whether they have been selected before doing the write.

Table 4-3. Logic Equations for Memory PLA U1308

MPV- = (PMGO+ * WEL- * RPL- * REF- * MDISL+ * SPON+) + (PMGO+ * WEL- * WPL- * REF- * MDISL+ * SPON+)
CASEN- = (SECND+ * REF- * MDISL+ * PMGO+) + (SECND+ * REF- * MDISL+ * PMGO+ * RPL- * WEL-) + (SECND+ * REF- * MDISL+ * PMGO+ * WPL- * WEL-) + (BUSY+ * REF- * MDISL+ * PMGO+) + (BUSY+ * REF- * MDISL+ * PMGO+ * RPL- * WEL-) + (BUSY+ * REF- * MDISL+ * PMGO+ * WPL- * WEL-)
MYCASEN- = (SECND+ * MDISL+ * REF- * PMGO+) + (SECND+ * MDISL+ * REF- * PMGO+ * RPL- * WEL-) + (SECND+ * MDISL+ * REF- * PMGO+ * WPL- * WEL-) + (BUSY+ * MDISL+ * REF- * PMGO+ * WEL-) + (BUSY+ * MDISL+ * REF- * PMGO+ * RPL- * WEL-)
QWRT- = (BUSY+ * REF- * MDISL+ * PMGO+ * WPL- * WEL-) + (BUSY+ * REF- * MDISL+ * PMGO+ * WEL-) + (SECND+ * REF- * MDISL+ * PMGO+ * WPL- * WEL-) + (SECND+ * REF- * MDISL+ * PMGO+ * WEL-)
FPDRV- = (ACK+ * SECND+ * REF- * MDISL+ * PMGO+ * RPL- * WEL- * SPON+) + (ACK+ * SECND+ * REF- * MDISL+ * PMGO+ * WEL- * SPON+)
ROW- = GAT- + (SECND+ * BUSY+) + MDISL+ + REF-
COL- = (GAT- * REF- * MDISL+ * BUSY+) + (GAT- * REF- * MDISL+ * SECND+)

Parity Error Register (PER)

The Parity Error Register (PER), U806 (55D), contains the ten least significant bits of the last parity error physical address. PELCH- latches the parity error address into the PER. PELCH- is normally low. It goes high to input the parity error address during the last half of the last SHC in a user memory (DRAM) read cycle with a parity error. At the beginning of the last SHC of any access, the ROW address for the DRAMs is reasserted on the MA+[0:9] bus which is the input to the PER. PELCH- goes low at the trailing edge of the SHC to latch the parity error address.

The PER is output onto the GIO-bus by the assertion of RDPEA- under control of the processor chip.

Parity Generation and Checking

The parity circuitry of the A400 board consists of two parity generators, the Parity PLA (PPLA), U206 (44D), and some random logic. The parity circuitry generates the parity bit which is written with every word in user memory and checks the bit when the data is read. One control line, PS+, is received at U810 (45C) to determine the sense of parity, and two control lines, PE- and PELCH-, are generated to indicate status. The equations for the Parity PLA are listed in Table 4-4.

When data is written to user memory, the parity generation circuitry generates a parity bit to be included with the word. This is done as described in the following paragraph.

Two parity generators, U810 (45C) and U712 (47C), access the backplane DB-bus. U712 receives DB+[0:7] and PARITY+. PARITY+ is produced by NOT-ANDing PCK-and WEL+ at U301 (44C). Because WEL+ is asserted on all write cycles, PARITY+ is always forced to a deasserted state for a write. Data is presented on the backplane DB-bus at the end of the first LHC of the access and into the following SHC. The lower parity generator looks at the DB-bus and PARITY+ to produce even parity on LOEP+. U810 looks at PS+ and backplane data bits DB+[8:15] to produce HIEP+ on the odd parity output. The odd output was used instead of the even output because the sense of PS+ is positive instead of negative. PS+ is the control signal from the processor that picks the sense of parity. When PS+ is deasserted, the parity type selected is odd and the total number of ones in the word, including the parity bit, is an odd number. The HIEP+ and LOEP+ lines go to PPLA which XORs them to produce PBIT+. PBIT+ is what is written into the on-board DRAM parity bit. It is also inverted at U306 (12C) to generate PAR- to be sent to the memory array boards.

On a user memory read, the accessed array sends its parity bit onto PCK- which is wire-ORed on the frontplane. PCK- is the inverted sense of the accessed parity bit. On the board, RPAR+ is the accessed parity bit. It is NANDed with BDSEL+ at U401 (42C) to drive PCK-, and thus is only allowed to drive PCK- when the on-board memory is accessed. PCK- becomes valid at the end of the access. Since WEL+ is deasserted at that time, PCK- is inverted and allowed to pass through as PARITY+. HIEP+ and LOEP+ are then generated just as in the write cycle. If there is no parity error, the read cycle finishes as usual.

If there is a parity error, it is determined by XORing HIEP+ and LOEP+ in the PPLA and qualifying the result against the deassertion of BUSY+, MDISL+, MPV–, and WEL– to make sure that it is the end of the cycle (BUSY+), it is not a boot access (MDISL+) or a memory protect violation (MPV–), and that it is a read cycle. It is also qualified against the assertion of SECND+ (places the check at the end of the cycle) and BDSEL– or ACK– to make sure that a memory array was actually accessed. All this comes together to produce BADP– on a parity error. BADP– is further qualified against VALID+ to produce the parity error signals. This places those signals in the last half of the last SHC of the access after VALID+ deasserts. Since data is stable at least 50 ns before the deassertion of VALID+, the parity error circuitry has plenty of time to settle to a valid state. This is needed because the parity error lines cannot be allowed to glitch.

So, on a parity error, BADP– is asserted during the last SHC. BADP– is NOT-ANDed with VALID+ and MSC+ at U1104A (47C) to produce PELCH– which is used to latch the low ten bits of the parity error address off the MA-bus. BADP– and VALID+ deassert PELCH– to open the latch and the assertion of MSC+ asserts PELCH– to quickly close the latch. Since PELCH– is in effect a positive version of PE–, PELCH– is what the processor chip and the on-board I/O receive for a parity error indication.

PE– is the other parity error indication signal and it does not have to go away as fast as PELCH– but it should be asserted as soon after the VALID– rising edge as possible. BADP– is buffered at U1103A (46C) to produce GOPE– (this buffer supplies additional hold time after SC+ 4 for proper operation with the I/O Extender). GOPE– is NOT-NANDed with VALID+ at U1103C (47C) to assert/deassert PE–, the backplane indication of a parity error.

The same equations that generate BADP– are further qualified against VALID+ to produce BDPE–. BDPE–, therefore, has about the same timing as PE– except that once it is asserted it stays asserted until CRS+ is asserted or SPON+ is deasserted. This latching function is accomplished by enabling the input on the BDPE– pin so that the output drives the OR term (BDPE– * SPON– * $\overline{\text{CRS+}}$).

BDPE– runs through an inverter, U1012A (21B), to become BDPE+ which drives the cathode of the parity error LED. This green LED is normally on. A parity error sets BDPE+ which drives the cathode of the parity error LED high to turn off the LED. The LED remains off until BDPE+ is reset with SPON+ or CRS+.

The GPU+ signal on the PPLA is used for testing to disable the outputs of the PPLA.

Table 4-4. Logic Equations for Parity PLA U206

PBIT+ = (HIEP+ * LOEP+) * $\overline{\text{SECND+}}$ + ($\overline{\text{HIEP+}}$ * $\overline{\text{LOEP+}}$) * SECND+ + PBIT+ * SECND+
BDPE- = ($\overline{\text{HIEP+}}$ * $\overline{\text{LOEP+}}$ * $\overline{\text{BUSY+}}$ * SECND+ * $\overline{\text{MPV-}}$ * $\overline{\text{MDISL+}}$ * $\overline{\text{WEL-}}$ * BDSEL- * $\overline{\text{VALID+}}$) + (HIEP+ * LOEP+ * $\overline{\text{BUSY+}}$ * SECND+ * MPV- * MDISL+ * WEL- * BDSEL- + VALID+) + (BDPE- * SPON+ * $\overline{\text{CRS+}}$)
BADP- = ($\overline{\text{HIEP+}}$ * $\overline{\text{LOEP+}}$ * $\overline{\text{BUSY+}}$ * SECND+ * $\overline{\text{MPV-}}$ * $\overline{\text{MDISL+}}$ * $\overline{\text{WEL-}}$ * BDSEL-) + (HIEP+ * $\overline{\text{LOEP+}}$ * $\overline{\text{BUSY+}}$ * SECND+ * $\overline{\text{MPV-}}$ * $\overline{\text{MDISL+}}$ * $\overline{\text{WEL-}}$ * BDSEL-) + ($\overline{\text{HIEP+}}$ * LOEP+ * $\overline{\text{BUSY+}}$ * SECND+ * $\overline{\text{MPV-}}$ * $\overline{\text{MDISL+}}$ * $\overline{\text{WEL-}}$ * ACK+) + (HIEP+ * LOEP+ * BUSY+ * SECND+ * MPV- * MDISL+ * WEL- * ACK+)
WEL+ = $\overline{\text{WEL-}}$
GPU+ = tri-states all outputs

Processor Chip Portion of Memory Control

The processor chip portion of the memory controller can be split into four major sections and one minor section. The major sections are the GO-, BUSY+, VALID, and REF- generation circuitry. The minor section generates an on-chip LATCH signal equivalent to the off-chip signal.

GO- Generation

The GO- signal is generated by the processor chip to indicate that a RAS cycle should be initiated on the next rising edge of SCLK-. The GO- signal is asserted in response to a request from one of three sources: the processor, I/O, or the refresh counter. Refer to the Processor Chip Chapter for a detailed description of GO- generation.

BUSY Generation

BUSY is asserted in response to MEMGO- and stays asserted until the requested memory access is complete. Refer to the Processor Chip Chapter for a detailed description of BUSY generation.

VALID- Generation

A memory cycle can last from two to four SCLK cycles. VALID- on the backplane is the signal that indicates that the memory cycle is about to end. The generation of VALID- is provided on the PC board under control of SET_VALID+. SET_VALID+ is generated in the processor chip. SET_VALID+ is connected to the D input of the VALID D-type flip-flop on the board. Refer to the Processor Chip Chapter for a detailed description of VALID- generation.

Processor Chip Refresh Circuitry

The 256k bit memory chips used by the A400 board and the 64k bit parts used in the supported memory array cards require the same refresh rates. Both parts need to have 256 rows accessed every 4 milliseconds (note that the 256k parts only count through 256 rows even though the 9 RAS bits pick one of 512 rows). In order to ensure that each row is accessed at least once every 4 milliseconds, a refresh counter schedules a "refresh cycle" approximately every 15.6 microseconds. Refer to the Processor Chip Chapter for a detailed description of the processor chip refresh circuitry.

5

On-Board I/O

On-Board I/O Functional Description

The on-board 4-port multiplexer consists of an I/O Processor (IOP) chip and the associated I/O master circuitry, and four serial port processors. The I/O Master is shared by the four port processors. The port processors buffer data until one of the user-definable special characters is detected, a carriage return is detected, or until its buffer is full (approximately 95 characters). At that time the port processor requests a DMA transfer from the driver. The port processor also does backspace processing to minimize the interrupts that the CPU must process.

The serial ports support RS-232 (standard), RS-422 (optional), RS-423 (optional), and V.24/28. Ports B and C support modem control. Port A of the on-board I/O can be selected to operate in the Virtual Control Panel (VCP) mode. In this mode, the terminal connected to port A can access and modify CPU registers. The U1001 switches on the A400 board configure the ports for RS-232/422/423 and configure Port A for VCP.

The select code of the on-board I/O is not programmable and is hard-wired to select code 77 and has an I/O ID number of 1777 octal.

The I/O Master

The I/O Master is the standard interface circuitry for the A-Series backplane and is used on every A-Series I/O Interface. It interfaces the 4-port serial multiplexer on the A400 board to the backplane and consequently to the A400 Central Processor itself and memory. Note that most signals and buses used by the on-board I/O "talk" to the CPU section of the board over the backplane.

The I/O Master manages most of the I/O functions from the 4-port multiplexer to free the Central Processor from the detailed management of the I/O functions and to improve system performance. The I/O Master also implements the Direct Memory Access (DMA) function. This allows the on-board I/O to have access to memory and to manage its own transfers to and from memory.

The I/O Master contains the IOP chip and associated logic circuits that control all interactions between the processor, main memory, and the on-board I/O interface. This includes decoding and executing I/O instructions and DMA functions. The I/O Master portion of the on-board I/O performs all of the program functions described in the A/L-Series I/O Interfacing Guide (part no. 02103-90005).

The Port Processors

Each port processor is a Hitachi HD63701V1 8-bit single-chip microcomputer unit.[1] The HD63701V1 has 192 bytes of on-chip RAM and 4k bytes of on-chip PROM. It is used in single-chip mode (mode 7), which includes four multiplexed ports. Port 1 and Port 4 are 8-bit parallel I/O ports, Port 2 is the timer (which is not used) and Serial Communications Interface, and Port 3 is an 8-bit parallel I/O port with two control lines, Input Strobe 3 (IS3–) and Output Strobe 3 (OS3–). The input frequency is 4.9152 MHz, which is internally divided by 4 to give a Frequency of Operation of 1.2288 MHz. This provides a cycle time of 0.8138 microseconds. The A400 provides an external communications clock at 19.2k baud. This clock is derived by a 19.2k baud divider on the board. Figure 5-1 is a block diagram of the HD63701V1 microcomputer chip.

The four port processors are labeled PPA, PPB, PPC, and PPD. Each of the port processors is connected to one serial port. The serial input and output lines on each port can transfer data at 300, 1200, 9600, or 19.2k baud in RS-232, RS-422, or RS-423 electrical protocols. 76.8k baud is available with RS-422.

Port Processor A is the only port that supports VCP operation. It can detect a "BREAK" function, therefore, causing the CPU to enter VCP mode. This feature can be disabled by setting the break enable switch (U1601 SW5) of the A400 processor switch to the closed position. Port A is configured to operate as the VCP by setting the on-board I/O switch U1001 SW7 closed.

Port Processors B and C support modem control (Port Processors A and D do not support modem control). The six modem control lines are Clear To Send (CTS), Request To Send (RTS), Data Set Ready (DSR), Carrier Detect (CD), Data Terminal Ready (DTR), and Ring Indicator (RI).

The port processors are interfaced to the I/O Master by three Programmable Logic Arrays (PLAs) and three registers. The three PLAs are the Bus Control PLA, the Port Processor Handshake PLA, and the Interrupt Generation PLA. The three registers and their functions are as follows:

- Data Register (register 30) - buffers transfers of command sequences or data bytes to the port processors.
- Control Register (register 31) - directs data transfers to one of the four port processors.
- Status Register (register 32) - indicates self-test and interrupt status of the port processors.

[1] Hitachi America, ltd.
Semiconductor & IC Sales and Service Division

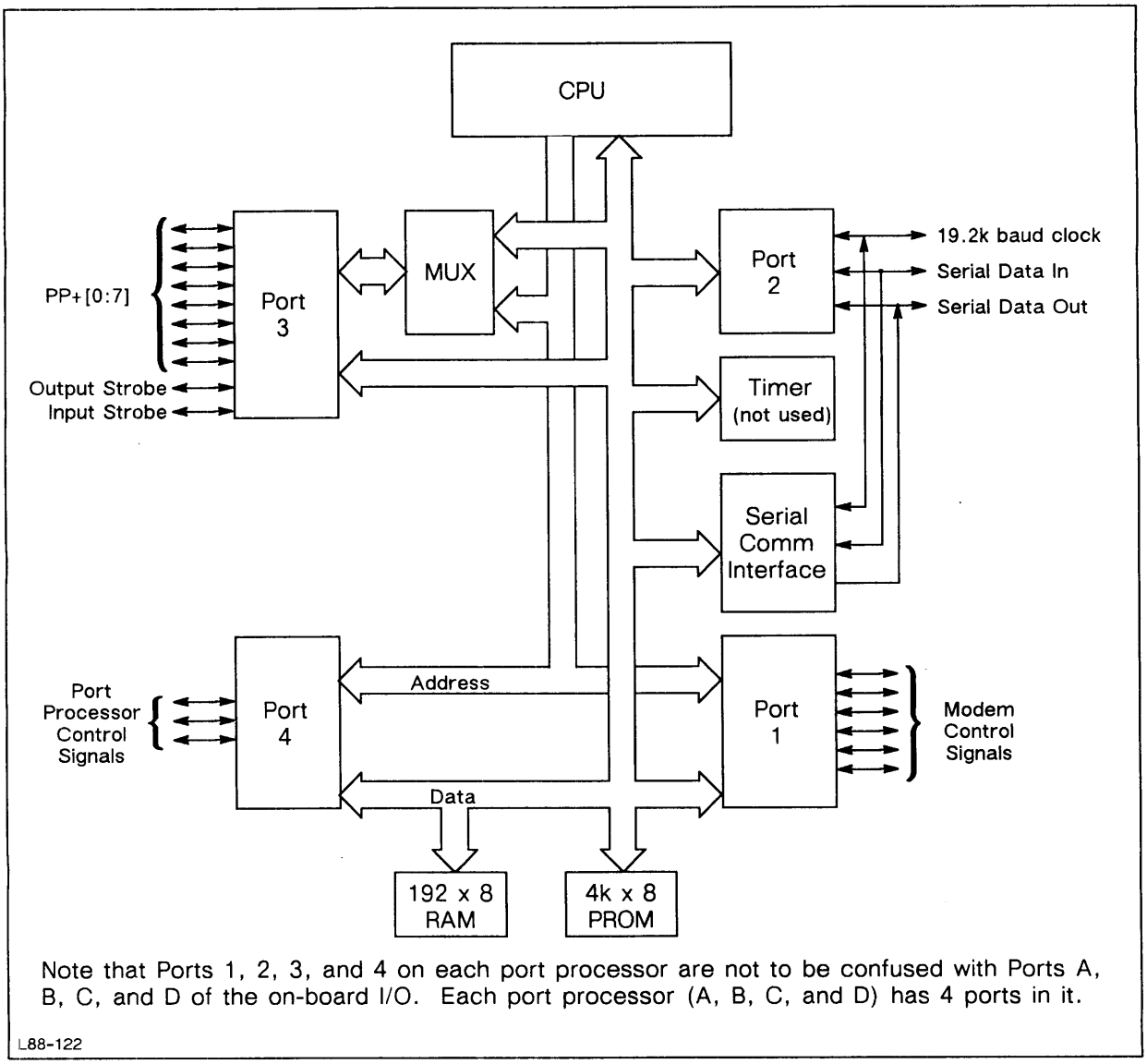


Figure 5-1. Hitachi HD63701V Port Processor Block Diagram

Port Processor Initialization and Self-Test

Upon reset, Port Processor A must be configured to a default value for VCP. Because all four port processors have the same firmware, all ports are preconfigured to this same initial value. These default values are as follows: Internal clocking of 9600 baud, and no XON/XOFF handshakes. If a carrier is detected, the port is configured as a connected modem, otherwise it is assumed that no modem is present. Unsolicited character interrupts are recognized, and all characters are echoed. The port processor performs a self-test, and upon successful completion, asserts the port processor status available interrupt request lines (PINTA–, PINTB–, PINTC–, and PINTD–), and deasserts the self-test fail bits (STFLA+, STFLB+, STFLC+, and STFLD+).

Also, on power-up, each port processor reads pins 24 and 25 to determine which port it is so that it will perform the proper functions (for example, VCP Slave functions for Port A or modem control for Ports B and C). Pins 24 and 25 are defined as follows:

Pin 24	Pin 25	Port Processor
0	0	A
0	1	B
1	0	C
1	1	D

The port processor self-test initially sets the self-test fail bit (STFLA/B/C/D+) in the Status Register. Upon successful completion of the self-test it clears the fail bit and sets the port interrupt bit (PINTA/B/C/D–) in the Status Register. A self-test failure is indicated by the fail bit being set. If the interrupt bit is also set when the self-test bit is set, additional information may be available from the port processor that failed. Refer to the On-Board I/O Chapter in the A400 Computer Reference Manual (part no. 02424-90001) for more information on the port processor firmware and self-test results. If the interrupt bit is not set when a self-test failure occurs, then the port processor self-test failed in the beginning of the self-test and it is not possible to obtain failure information from that port processor.

On-Board I/O Switches (U1001)

The U1001 switches configure the ports for RS-232 or RS-422/RS-423 (switches S1 through S4), configure modem control (switches S5 and S6), and determine if Port A will be the VCP interface (switch S7). Note that if modem control is desired, switches S2 and/or S3 (ports B and C, respectively) must be configured as RS-232 in addition to setting switches S5 and S6 for V.28 or RS-232. Refer to Table 5-1 for a definition of the switches.

Table 5-1. On-Board I/O U1001 Switch Definitions

Switch	I/O Port Controlled	Definiton
S1	A	Open = RS-422/423; Closed = RS-232.
S2	B	Open = RS-422/423; Closed = RS-232.
S3	C	Open = RS-422/423; Closed = RS-232.
S4	D	Open = RS-422/423; Closed = RS-232.
S5	C	Open = V.28; Closed = RS-232. You must also set switch S3 for RS-232 when using Port C for Modem control.
S6	B	Open = V.28; Closed = RS-232. You must also set switch S2 for RS-232 when using Port B for Modem control.
S7	A	Open = does not operate as VCP; Closed = does operate as VCP.

VCP Slave Functions

The slave feature of the I/O Processor (IOP) chip is used in conjunction with the Virtual Control Panel (VCP) program. The slave feature enable (SLRQ+ deasserted) is read into the IOP chip of the VCP interface on power-up and cannot be altered until the next power-up condition.

If the slave feature is enabled, any assertion of the slave signal (SLRQ+) causes the IOP chip to generate a slave request on the next instruction fetch. (If the slave feature is not enabled at power-up, then all future transitions of SLRQ+ are ignored.) When the request is granted, the IOP chip requests the CPU's current P-Register contents and saves these contents in a register in the IOP chip. The IOP chip then stores the starting address of the VCP program into the CPU's P-Register, instructs the CPU to enable VCP, and allows execution to start. The VCP program can be started in two ways:

1. On power-up and after the self-test the VCP program starts execution. This selection may often be used because the loaders can be invoked individually from the VCP.
2. When a HLT* (halt) instruction is executed, the IOP chip interprets it in the same manner as a change in the slave enable signal. This allows a program to have breakpoints for debugging purposes. Note that if memory protect is enabled, a HLT instruction is not executed but causes a memory protect interrupt.

During execution of the VCP program, access to the P-save register in the IOP chip is accomplished with LIA/B 3 and OTA/B 3 (without the instruction's Flag bit set). It should also be noted that the IOP chip will not execute a slave request until an STC 2 (enable break feature) instruction has been executed. This prevents re-entry of the VCP program once it has been entered.

During the self-test, the starting address of the VCP program is assigned to the break-enabled interface card by an OTA/B 3,C* instruction with the A- or B-Register set to the address. This address also can be read back with an LIA/B 3,C* instruction.

On-Board I/O Cable

The A400 Computer is equipped with a cable for the on-board 4-Channel Multiplexer. One end of the cable connects to the 36-pin edge connector (J2) on the A400 board; the other end is a 4-port breakout panel which contains four 25-pin RS-232 D-connectors labeled A through D. Refer to Figure 5-2 for a diagram of the breakout panel.

Each of the RS-232 connectors on the breakout panel support all three electrical standards, however, RS-422/423 require non-standard connections. If the RS-449 mechanical standard is required, an adaptor cable with an RS-449 connector must be fabricated by the customer. Figure 5-3 is a diagram of how the adaptor cable is used with the A400 for RS-422/423 communication. The following section describes the adaptor cable.

* If break is not enabled on any interface card, then the instruction has no effect.

The modem control lines are labeled in Figure 5-4 for Ports B and C. Modem control is not supported on Ports A and D; the control lines are wired together as shown in Figure 5-4. Note that the numbers in parenthesis next to the signal lines are the V.28 standard signal labels.

Table 5-2 gives the signal definitions for connector J2. It also indicates to which pin number on each of the ports of the breakout panel the signal goes and how the 6 pins of each of the DCE/DTE Switches is connected.

Adaptor Cable for RS-422/423 Support

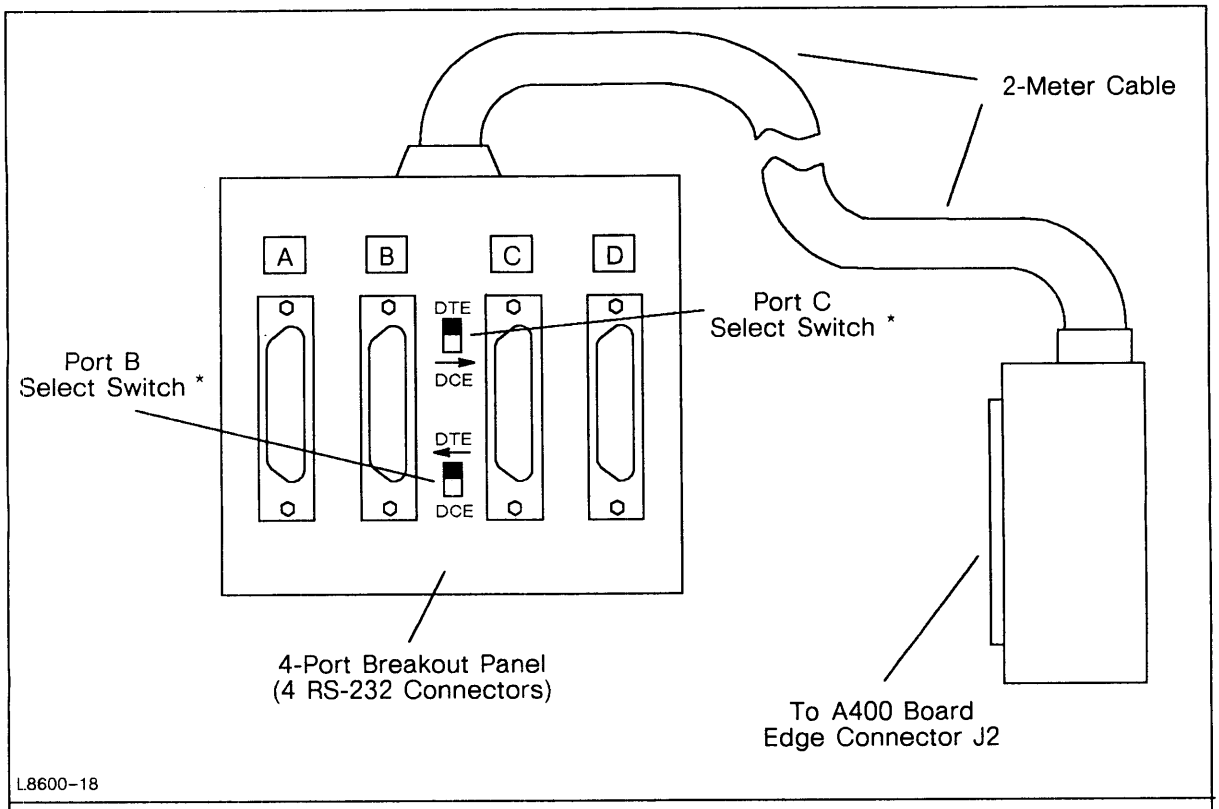
The four RS-232 connectors on the breakout panel include signals necessary for RS-422/423 protocol. If the mechanical standard, RS-449, is being used for RS-422/423 communication, an adaptor cable (fabricated by the customer) is required to connect the proper RS-422/423 signal lines from the breakout panel to an RS-449 standard connector. Figure 5-6 is a wiring diagram showing which pins from the RS-232 connector on the breakout panel connect to the proper pins on the RS-449 connector.

Breakout Panel DCE/DTE Switches

Ports A and D are wired to operate as Data Communication Equipment (DCE). Ports B and C are equipped with switches on the breakout panel allowing them to operate independently as DCE or Data Terminal Equipment (DTE). The direction of data flow on pins 2 and 3 of the 25-pin D-connectors determines DCE or DTE operation. The direction shown on pins 2 and 3 in Figure 5-4 is for DCE operation. When the port select switch for port B or C is in the DTE position, the direction of data flow shown on pins 2 and 3 is reversed. Figure 5-5 is a wiring diagram showing how the switch connects the signals from the board edge connector to the RS-232 connectors for Ports B and C.

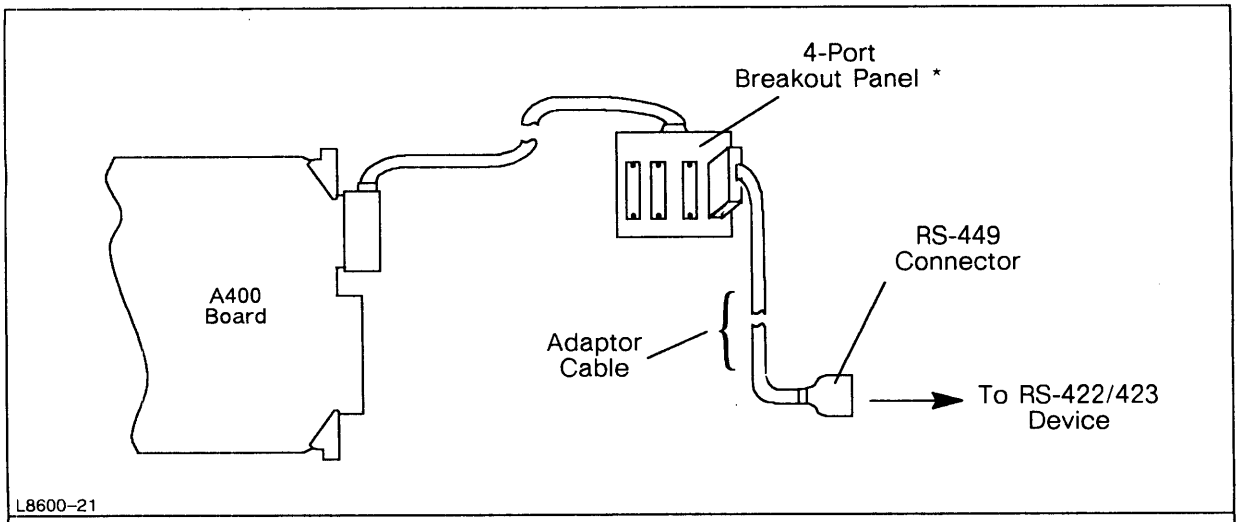
When connecting a terminal to Port B or C, the switch on the breakout panel must be in the DCE position. Note that only pins 2, 3, and 7 should be used in the cable going from the breakout panel connector to the terminal.

When connecting a modem to Port B or C, the switch must be in the DTE position.



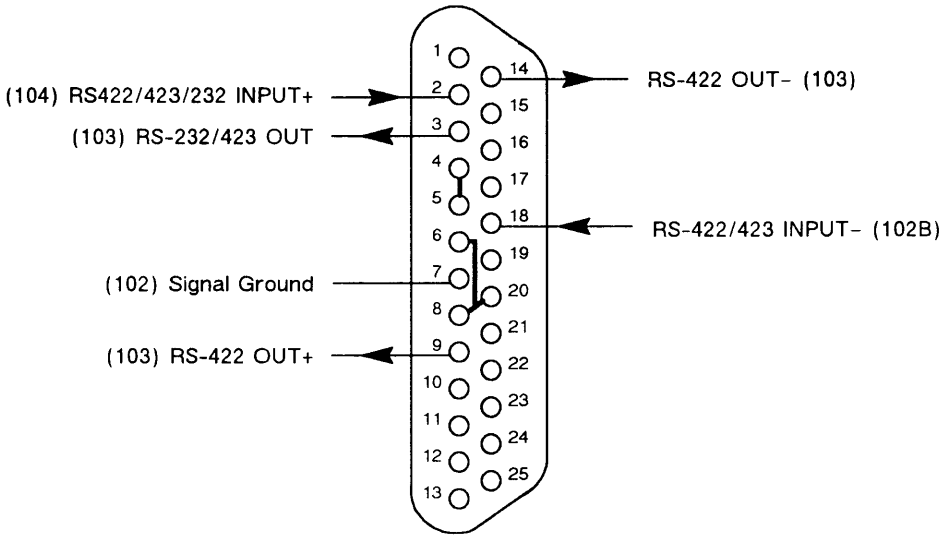
* When connecting a terminal to Port B or C, the Select Switch must be in the DCE position. When connecting a modem, the Select Switch must be in the DTE position.

Figure 5-2. A400 4-Channel Multiplexer Cable

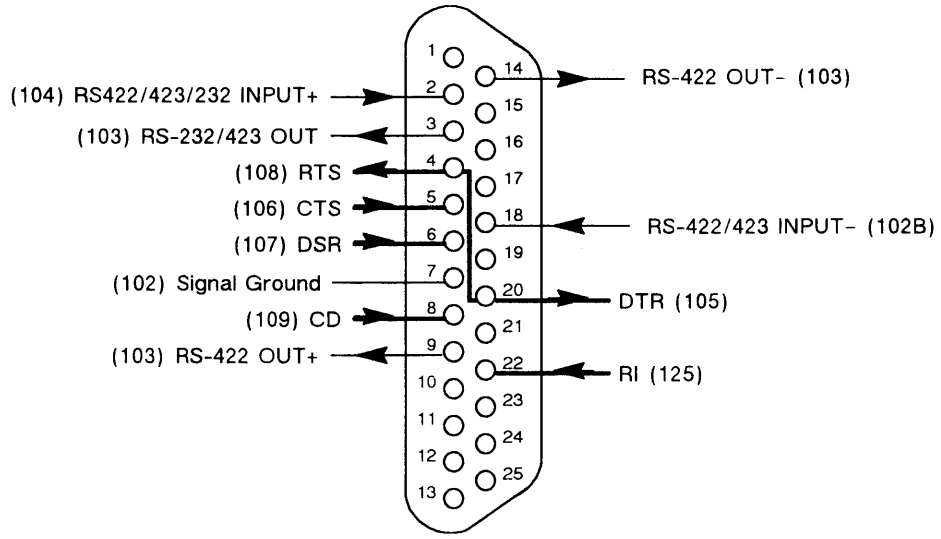


* The RS-232 connector on the adaptor cable can be connected to any of the four ports on the breakout panel.

Figure 5-3. Cabling Diagram when Using an Adaptor Cable for RS-422/423 Communication



Pin Assignments for Signals on Ports A and D



Pin Assignments for Signals on Ports B and C

L8600-19

Note the following:

1. Bold lines indicate modem control lines; all others are data lines.
2. The arrows indicate the direction of data flow.
3. Switches on the breakout panel will configure Ports B and C for either DCE or DTE. The switches reverse the direction of data flow in pins 2 and 3. The direction shown in this diagram is for DCE which is the same as the HP 12040 8-Channel Multiplexer.

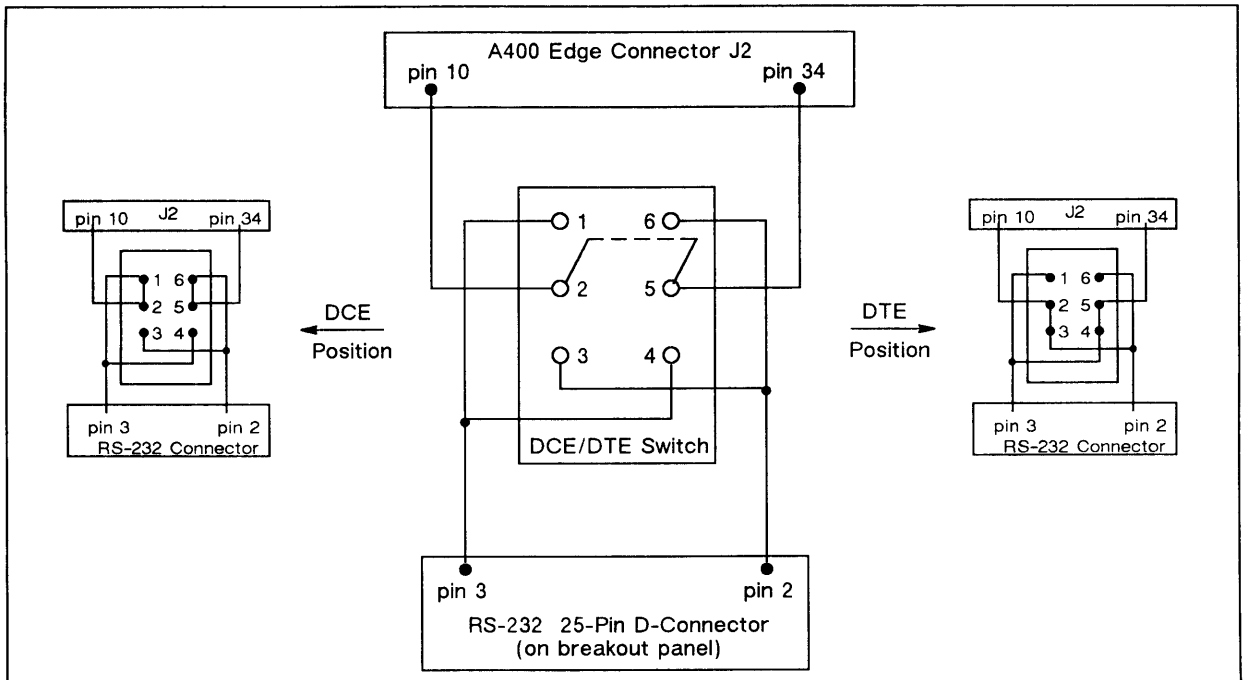
Figure 5-4. RS-232 Connector Pin Assignments on the MUX Cable Breakout Panel

Table 5-2. Connector J2 Signal Definitions

Signal Name	Connector J2 Pin Number	Breakout Panel Port Pin Number				Twisted Pair	DCE/DTE Switch Port B	DCE/DTE Switch Port C
		Port A	Port B	Port C	Port D			
OUTA+	1	9				1		
OUTA-	2	14				1		
OUTB+	3		9			2		
OUTB-	4		14			2		
OUTC+	5			9		3		
OUTC-	6			14		3		
OUTD+	7				9	4		
OUTD-	8				14	4		
OA232+	9	3				5		
OB232+	10					6	2	
OB232I+	10		2				3 & 6	
OC232+	11					7		2
OC232I+	11			2				3 & 6
OD232+	12				3	8		
RTSC+	13			4				
DTRC+	14			20				
RTSB+	15		4					
DTRB+	16		20					
SIG GND	17	7				5		
SIG GND	18		7			6		
SIG GND	19			7		7		
SIG GND	20				7	8		
CTSB+	21		5					
DSRB+	22		6					
RIB+	23		22					
CDB+	24		8					
CTSC+	25			5				
DSRC+	26			6				
RIC+	27			22				
CDC+	28			8				
RECDD-	29				18	9		
RECDD+	30				2	9		
RECDC-	31			18		10		
RECDC+	32					10		5
RECDCI+	32			3				1 & 4
RECDB-	33		18			11		
RECDB+	34					11	5	
RECDBI+	34		3			11	1 & 4	
RECDA-	35	18				12		
RECDA+	36	2				12		
JUMPER1+		8						
JUMPER1+		20						
JUMPER1+		6						
JUMPER2+		4						
JUMPER2+		5						
JUMPER3+					8			
JUMPER3+					20			
JUMPER3+					6			
JUMPER4+					4			
JUMPER4+					5			

Notes: 1. The DCE/DTE switches are double-throw 6-pin switches. Refer to Figure 5-5 for a pin connection diagram.

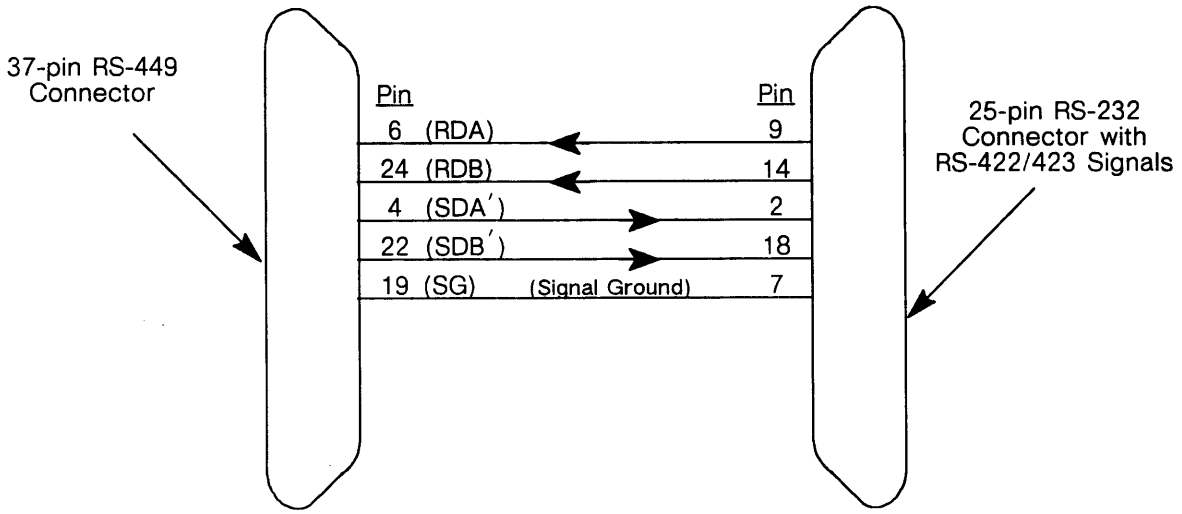
2. The JUMPER1/2/3/4+ signals interconnect the modem control signals of Ports A and D (which do not support modems) as specified in the table.



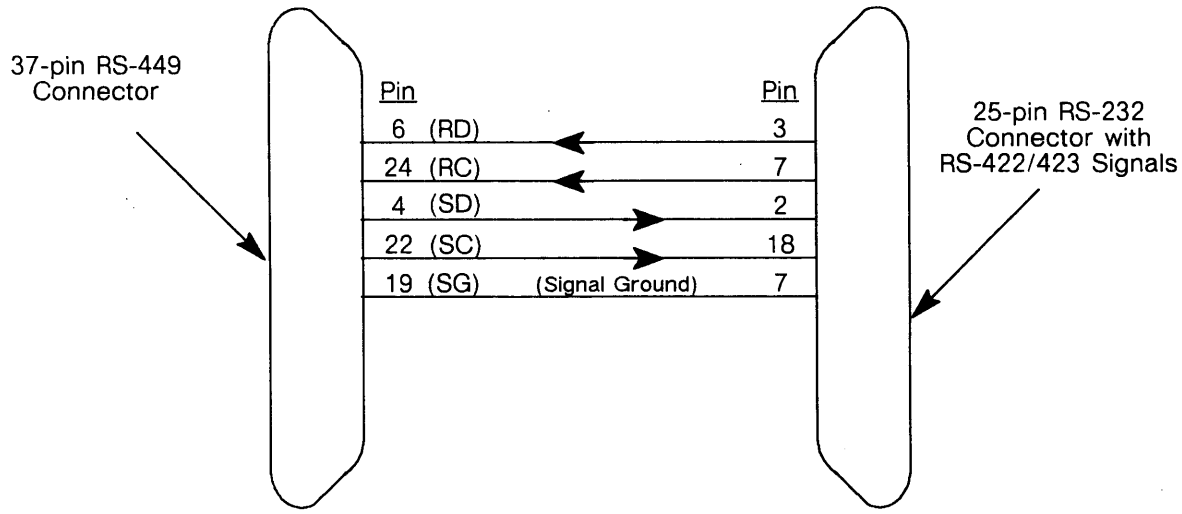
Note that this diagram is for Port B. The diagram for Port C is identical except that pins 10 and 34 on connector J2 for Port B are pins 11 and 32, respectively, for Port C.

L88-123

Figure 5-5. Port B and C DCE/DTE Switches Connection Diagram



Pin Connections for an RS-422 Adaptor Cable (Arrows indicate direction of data flow)*



Pin Connections for an RS-423 Adaptor Cable (Arrows indicate direction of data flow)*

* Note that the direction shown requires the Port Select Switch to be set to DCE if Ports B or C are used for RS-422 or RS-423.

L8600-20

Figure 5-6. Wiring Diagram of RS-232 to RS-449 Connections for Adaptor Cable

On-Board I/O Theory of Operation

This section describes the gate-level operation of the on-board I/O. Note that the on-board I/O and the CPU portion of the A400 board interact over the backplane, the same as the other I/O interfaces in the backplane. The on-board I/O and the CPU, however, share the backplane receivers (one receiver drives both I/O and CPU) on the following twelve signals:

BPON+	CRS–	PE–
BUSY–	IAK–	RNI–
CCLK–	IOGO–	SCLK–
CPUTURN–	MP+	VALID–

The I/O Master

The I/O Master portion of the I/O system is depicted on page 11 of the schematics. The standard A-Series I/O signal names SCLK– and BPON+ were changed to SC– and PON+, respectively, for the A400 on-board I/O (the standard name will be shown in the text within parenthesis).

The I/O Master is hardwired to select code 77 and I/O ID 1777. All lines of the Chip-bus, CB+[0:15], are tied high at 111B/C/D on the schematics. Therefore, at power-on, when PON+ is asserted, this word on CB+[0:15] (177777 octal) is latched into an internal register in the IOP chip.

The Port Processors

Each port processor is a Hitachi HD63701V1, an 8-bit CMOS single-chip microcomputer with 4 kbytes of PROM, 192 bytes of RAM, and 4 I/O ports. A block diagram of the 63701V is shown in Figure 5-1.

The port processors interface to the I/O Master by three registers and three PLAs. The three registers are the Data Register (register 30), the Control Register (register 31) and the Status Register (register 32). The three PLAs are the Bus Control PLA, the Port Processor Handshake PLA, and the Interrupt Generation PLA.

The function of the four ports within each port processor and the registers and PLAs that interface them to the I/O Master are described in the following sections.

The Modem Control Port (Port 1)

The Modem Control Port, port 1 (P1[0:5]), of Port Processors B and C connects to six control lines: Request to Send (CA), Clear to Send (CB), Data Set Ready (CC), Data Terminal Ready (CD), Ring Indicator (CE), and Carrier Detect (CF). Request to Send (CA) and Data Terminal Ready (CD) are outputs from the port processor and the other four signals are received by the port processor. All of these signals use RS-232 electrical standard transmitters or receivers. The signal names, J2 connector pin numbers, and RS-232 25-pin "D" pin numbers are listed in Table 5-2.

The Serial Port (Port 2)

The serial input to each port processor is driven into the Serial Port, port 2 bit 3 (P2[3]), by a receiver. The receiver can be configured for either RS-232 or RS-422/423 by setting the U1001 switches 1 through 4 (which correspond to ports A through D, respectively). If the switch is closed, the port is configured for RS-232; if the switch is open, it is configured for RS-422/423. Note that Port Processors A through D are independently configurable.

The serial output from each port processor is driven from port 2 bit 4 (P2[4]) to the 422/423 transmitters. The clock rate required to transfer data at 19.2k baud is applied to port 2 bit 2 (P2[2]) and all other baud rates are generated within the port processor. The baud rate desired is selected by the driver requesting that the firmware load the 63701V's "TRANSFER RATE/MODE CONTROL REGISTER" (address 10 hex) with one of the following codes:

Code (HEX)		Baud Rate
0C	→	19.2k
07	→	9600
06	→	1200
05	→	300

Note that VCP speed senses or defaults to a baud rate of 9600 depending on the setting of the U1601 BOOT SEL switches.

The CPU Data Port (Port 3)

All communications between the port processors and the CPU go through the CPU Data Port (port 3). Input data is applied to port 3 (P3[0:7]) and DVCMD- is asserted by an STC, 30 from the CPU. DVCMD is input to the Port Processor Handshake PLA (refer to the PLA Equations section) to generate ISA-, ISB-, ISC-, and ISD- which are applied to the IS3- input (pin 39) of each port processor.

When the port processor is ready for the next word it sets OS3- (the OSA-, OSB-, OSC-, and OSD- signal for the corresponding port processor). These signals go the the Port Processor Handshake to generate SRQ- and the sequence is repeated.

In the output mode the CPU strobes ISA-, ISB-, ISC-, and ISD- by asserting DVCMD- (STC, 30). The port processor then applies the data to port 3 and generates its output strobe signal (OSA-, OSB-, OSC-, or OSD-).

The Port Processor Control Port (Port 4)

The Status and Control registers are connected to each port processor through the Control Port (port 4). Port 4 (P4[0:7]) is an 8-bit dynamic register in which the direction of each bit can be assigned independently. The bit assignments for port 4 are as follows:

7	6	5	4	3	2	1	0
PORT INT (O)	SLAVE REQ (IO)	PORT ID 1 (I)	PORT ID 0 (I)	not used	not used	INPUT XFER (I)	CNTL XFER (I)

where (I) indicates input, (O) indicates output, and (IO) indicates both directions.

Bits 1 and 0 are inputs to the port processor and are driven by the corresponding signals in the control register, register 31.

The PORT ID bits (bits 5 and 4) are inputs and identify the port processor as PPA (00), PPB (01), PPC (10) or PPD (11).

The SLAVE REQ bit (bit 6) of PPA (not used by PPB, PPC, or PPD) generates SLRQ– for the I/O Master. This line is used to cause the CPU to enter the VCP code if the break enable switch (U1601 SW5) was closed at the time that the system was powered up.

The PORT INT bit (bit 7) is connected to the Status Register, register 32, PORT INTR bit for its port processor and is qualified with the control register, register 31, ENAB INT PORT bit by the Interrupt Generation PLA to generate IRQ– for the I/O Master.

The Status Register (LIA/B 32)

The Status Register, U108 (122B), is read when the main program executes an LIA/B 32. The I/O Master generates BCS7– which drives the EN input of the Status Register, gating the inputs onto the data bus, DB+[0:7]. The inputs to the Status Register reflect the dynamic status of the port processors. The bit assignments of the Status Register are as follows:

7	6	5	4	3	2	1	0
Self-Test ST D	Self-Test ST C	Self-Test ST B	Self-Test ST A	PORT D INTR	PORT C INTR	PORT B INTR	PORT A INTR

The PORT * INTR bits (bits 0 through 3), when asserted (logic 0), indicate that the port identified by the (*) is requesting an interrupt. More than one port can request an interrupt at one time. The port interrupt bits are deasserted (logic 1) when its port processor no longer requires service.

The self-test bits, ST * (bits 4 through 7), when asserted (logic 1) indicate that the port processor identified by the (*) failed the last execution of its self-test.

The Control Register (OTA/B 31 or LIA/B 31)

Transfers to the on-board I/O are directed to one of the four port processors by the Control Register, U406 (122A). It functions similar to the Status Register. An OTA/B 31 causes the I/O Master to assert BCS2- and CKDAT-. The Bus Control PLA, U208 (121C), ANDs BCS2- and CKDAT to generate CREGLD- which loads the backplane data into the Control Register. The Control Register can also be loaded from the second word of a DMA self-configuring quad. The signal generation is identical whether the load is DMA or OTA/B.

The Control Register can be read by the execution of an LIA/B 31. BCS6- is asserted which drives the contents of the register onto the data bus, DB+[0:7]. The bit assignments of the Control Register are as follows:

7	6	5	4	3	2	1	0
63701V CNTL XFER	PORT SEL 1	PORT SEL 0	INPUT XFER	ENAB INT PORTD	ENAB INT PORTC	ENAB INT PORTB	ENAB INT PORTA

The ENAB INT PORT* bits (bits 0 through 3) allow the port processors to generate a CPU interrupt when they need service. These bits do not affect the setting of the Status Register interrupt bits. They generate the interrupt (the jump through the trap cell) for that port processor.

The INPUT XFER bit (bit 4) indicates the direction of the transfer. If the bit is set, it indicates a transfer from the port processor to the CPU or main memory.

The PORT SEL * bits (bits 5 and 6) are used by the Port Processor Handshake PLA to generate an input strobe (ISA-, ISB-, ISC-, or ISD-) to the selected port processor. The port selection is as follows:

PORT SEL 1	PORT SEL 0	Port Processor Selected
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Port D

The 63701V CNTL XFER bit (bit 7) indicates to the port processors that the transfer will be port processor control information rather than port data. The control register can be loaded during DMA transfers by using the self-configuring DMA quad. The second word is the control register data. Under program control an OTA/B 31 loads the register and an LIA/B 31 reads the register.

The Data Register (OTA/B 30 or LIA/B 30)

The Data Register, U506 (122C) and U606 (122B), transfers command sequences or data bytes to the port processors. Transfers through this register occur in two modes, program control and DMA control.

Output Transfer:

An output transfer (from the CPU or main memory to the Port Processor) starts with loading the Control Register to indicate an output transfer (INXFR+ is deasserted) and to select the desired port processor (using PSEL1+ and PSEL0+). The Data Register is loaded when an OTA/B 30 or a DMA transfer is executed by the main program. The I/O Master generates BCS1- to indicate that the data is applied to the backplane and CKDAT- to indicate that the data on the backplane is now valid. These two signals are ANDed together by the Bus Control PLA, U208 (121C), to generate DREGLD-. DREGLD- is then applied to the CAB pin of the Data Register which clocks the 16-bit wide data from the backplane into the Data Register.

If the load is caused by an OTA/B, only the lower eight bits of the data word are available to the port processors as data. If the load was caused by a DMA transfer and the BYTE PACK bit is set in the DMA Control Word (the first word in the DMA quad), both the upper and the lower byte are passed to the port processor. The upper byte (bits 8 through 15) is the first byte to be transferred in the byte mode.

The data transfer between the Data Register and the port processors is started when an STC 30,C or a DMA transfer causes the I/O Master to generate DVCMD-. The Bus Control PLA ANDs LOBYT- and INXFR+ to generate RHIBYTE+ and RLOBYTE+. Refer to Figure 5-7 for a listing of the Bus Control PLA equations. RHIBYTE+ enables the high byte of the Data Register (if LOBYT- is high) onto the port processor bus (PP+[0:7]). RLOBYTE+ enables the low byte of the Data Register onto the PP+[0:7].

The Port Processor Handshake PAL, U204 (123D), ANDs PSEL0+, PPSEL1+, and DVCMD- to assert the appropriate input strobe (ISA-, ISB-, ISC-, or ISD-) on the port processor selected by PSEL0+ and PSEL1+. The input strobes notify the port processors that a data byte is valid on the port processor CPU Data Port 3 (P3[0:7]). When the port processor no longer needs the data it asserts its output strobe (OSA-, OSB-, OSC-, or OSD-). The Port Processor Handshake PAL then ANDs the output strobe with PSEL0+ and PSEL1+ to generate SRQ-. SRQ- is an input to the I/O Master that indicates that the transaction is complete. If the load was caused by a DMA transfer, the next byte is transferred or the transfer is terminated. In the STC 30,C mode the SRQ- sets the flag on select code 30.

Programmed Control Output Transfer (OTA/B 30):

> Under programmed control the data register is loaded by an OTA/B 30 and the data is sent to the port processor by an STC 30,C. When the port processor is ready for the next byte it sets flag 30. Note that only the lower byte of the data word (bits 0 through 7) are transferred to the port processor.

DMA Output (Memory to Device):

During a DMA output transfer through the port processor, the following conventions must be used:

a. DMA self-configuration mode must be used.

b. The Auto bit must be set (register 21, bit 8).

c. The DVCMD bit must be set (register 21, bit 14).

Input Transfer:

The Data Register input transfer (from the port processors to the CPU or main memory) starts with a load of the Control Register, U406 (122A), to indicate an input transfer (INXFR+ is asserted) and to select the desired port processor (using PSEL0+ and PSEL1+). An STC 30,C or a DMA transfer (with the AUTO bit set) causes the I/O Master to assert DVCMD- which the Port Processor Handshake PAL ANDs with PSEL0+ and PSEL1+ to generate the input strobe (ISA-, ISB-, ISC-, or ISD-) to one of the port processors.

Serial data from a device is input to the port processor through the Serial Data In line of each port processor (SDINA+, SDINB+, SDINC+, or SDIND). The port processor converts this to parallel data, applies the data to PP+[0:7] (port 3 bits 0 through 7), and asserts its output strobe (OSA-, OSB-, OSC-, or OSD-). The Port Processor Handshake PAL ANDs the output strobe, PSEL0+, and PSEL1+ to generate SRQ-.

In addition to the I/O Master using SRQ- to notify the CPU that data is available (setting the flag or triggering DMA), the Bus Control PAL ANDs SRQ- with LOBYT- and INXFER+ to generate LHIBYTE- and LLOBYTE-. These two signals clock the data (the CBA pin) into the high and low bytes of the Data Register.

When both bytes have been packed during a DMA transfer or on the execution of an LIA/B 30, the I/O Master generates BCS5- which asserts the GBA pin on the Data Register and drives the contents of the Data Register onto the Data Bus.

Programmed Control Input Transfer (LIA/B 30):

Under programmed control the data register is read by an LIA/B 30. That data is requested from the port processor by an STC 30,C. When the port processor is ready for the next byte it sets flag 30. Note that only the lower byte of the data word (bits 0 through 7) is meaningful. Bits 8 through 15 represent the last byte loaded into the high byte (meaningless).

DMA Input (Device to Memory):

During a DMA input transfer through the port processor, the following conventions must be used:

a. The input bit must be set (register 21, bit 7)

b. The Auto bit must **not** be set (register 21, bit 8)

c. The DVCMD bit must be set (register 21, bit 14)

VCP Operation

Port Processor A, U804 (126A), is capable of being the VCP port for the A400 processor. Port Processor A drives SLRQ– (port 4 bit 6) out to the Interrupt Generation PLA, U104 (124A). This PLA inverts it to produce BSLRQ+ and supplies it to the VCP enable switch, U1001 SW7 (pin 7). The other side of the switch (pin 8) is connected to the SLRQ+ input of the I/O Master.

The SLRQ– line on the port processor floats during a power-up sequence, therefore a pull-up resistor is connected to this line to ensure that the line is high during power-up. This causes BSLRQ+ (out of the Interrupt Generation PLA) to be low. If U1001 SW7 is closed during a power-up sequence (PON+ low), then the SLRQ+ input to the I/O Master is also low on the rising edge of PON+. This signals the I/O Master that it is the VCP interface. After the port processor self-test has completed, the port processor drives the SLRQ– line high (SLRQ+ input to I/O Master is low). When the port processor sees a "BREAK" transmitted over the line it drives SLRQ– low (SLRQ+ input to I/O Master is high) causing the I/O Master to initiate a VCP entry. The relationship of SLRQ+ to the IOP chip during and after power-up can be summarized as follows:

SLRQ+	During Power-Up	After Power-Up
0	I/O Master is VCP interface	Not Slave Request
1	I/O Master is **not** VCP interface	Slave Request

If U1001 SW7 is open, the pull-up resistor (U3080, 134B) on SLRQ+ keeps the line high during the power-up sequence. This indicates to the I/O Master that it is not the VCP interface and to ignore all future transitions on the SLRQ+ input.

The Port Processor Clock

All four port processors receive a 4.91520 MHz clock, PPCLK+, which is supplied by the A400 processor chip. It is a symmetrical version of CCLK+ divided by three. The E output of Port Processor A, U804 (126A), is input into a divide by 16 counter, U203 (124B). This counter divides it by 8 and connects it to the the external communications clock input, Port 2 bit 2 (pin 10), of the port processors. This external clock allows the port processors to communicate at 19.2k baud.

Power-On Reset

The port processors require that the reset line (RESET–) stay low for at least 20 milliseconds after the +5 volt supply is in regulation and at least 900 nanoseconds for an in-process reset (without the loss of +5V). To accomplish this, the A400 processor chip generates IORST– which stays low for 20 milliseconds after PON– goes high and 1 microsecond after CRS is asserted.

Interrupt Generation

Each port processor has an interrupt signal (port 4 bit 7), PINTA–, PINTB–, PINTC–, or PINTD–. This signal is gated by the Interrupt Generation PAL with that port processors enable interrupt bit from the Control Register (ENINTA+, ENINTB+, ENINTC+, or ENINTD+) to assert the IRQ– line of the I/O Master. The IRQ– line sets flag 30 and keeps it set until the port processor deasserts the PINT*+ line or the interrupt enable is disabled.

The EIA Standards

The on-board I/O is capable of communicating over RS-232, RS-422, or RS-423. Each port can be independently configured for one of these standards. If modem control is desired, that port must be configured as RS-232. Transmit and receive data for all three standards are connected to the port processors through SDIN*+ (port 2 bit 4) for input data and SDOUT*+ (port 2 bit 3) for output data.

Biasing

The same receivers are used to receive the RS-232/422/423 standards. To accomplish this, the input must be biased and have a specified input resistance. The circuit uses a 6k ohm pull-down resistor to a –2.4 volt supply. R2, CR2, and C32 generate the –2.4 volt supply at 131A on the schematics.

RS-232

The output serial data line (SDOUTA+, SDOUTB+, SDOUTC+, or SDOUTA+) from each port processor is received by the RS-232 drivers, U1502 (137B) and U1402 (137C), and sent out over connector J2. The slew rate resistors (R7 and R5, 137B/C) provide 2.08 microseconds of rise and fall time on the data drivers to comply with the RS-232 standard.

The input data receiver, U1401 (133B), drives the serial data input lines to the port processors. For RS-232 operation the positive input of the receiver must be grounded by closing its switch, U1001 (132B).

RS-422

The RS-422 output data driver, U1101 (137A), converts the serial single-ended output of each port processor to the differential outputs required by the standard. The input data path for RS-422 uses the same receiver as RS-232 but requires the grounding switch (U1001) for that port to be open. Both input lines (pins 2 and 18 on the breakout panel connector) are connected to the differential outputs of the transmitter (device end).

RS-423

The output path for RS-423 is the same as the path for RS-232. The input path for RS-423 also uses the same input receivers as RS-232 but requires the grounding switch (U1001) for that port to be open. RS-423 requires the devices to provide the signal ground on one side of the twisted pair, the SC signal line (pin 18 on the breakout panel connector).

Modem Control

Each modem control port contains two output lines and four input lines. These lines are supported under the RS-232 standard. The two output lines (RTSB/C+ and DTRB/C+) are driven from the port processor signal TDTRB/C- (port 1 bit 3 of PPB and PPC) to connector J2 by an RS-232 driver, U1302 (137C).

The input lines (CDB/C+, RIB/C+, DSRB/C+, and CTSB/C+) at 131C,D are connected to pull-up resistors to ensure state on disconnect. These lines are received by U1301 (132C) and U1201 (132D) and passed to the port processors (port 1 bits 5,4,2,1 of PPB and PPC).

PLA Equations

The logic equations used to generate the three PLAs for the on-board I/O are given in the source listings for each PLA which are shown in Figure 5-7, Figure 5-8 and Figure 5-9. The signal TSTDIS- is used to disable the PLAs for testing. When TSTDIS- is asserted, the outputs of the PLAs float.

LHIBYTE+ = SRQ- * $\overline{\text{LOBYT-}}$ * INXFER+ * $\overline{\text{SACK-}}$	(Data from PP to Data Register)
LLOBYTE+ = SRQ- * LOBYT- * INXFER+ * $\overline{\text{SACK-}}$ + SRQ- * $\overline{\text{LOBYT-}}$ * INXFER+ * $\overline{\text{SACK-}}$	(Data from PP to Data Register) (Data from PP to Data Register, odd byte pack)
RHIBYTE+ = $\overline{\text{LOBYT-}}$ * $\overline{\text{INXFER+}}$	(Data from Data Register to PP)
RLOBYTE+ = LOBYT- * $\overline{\text{INXFER+}}$	(Data from Data Register to PP)
$\overline{\text{DREGLD-}}$ = $\overline{\text{BCS1-}}$ + $\overline{\text{CKDAT-}}$	(Data bus to Data Register)
$\overline{\text{CREGLD-}}$ = $\overline{\text{BCS2-}}$ + $\overline{\text{CKDAT-}}$	(Data bus to Control Register)
TSTDIS- = disables the PLA for testing	

Figure 5-7. Bus Control PLA (U208) Equations

BSLRQ–	= $\overline{\text{SLRQ}}$–
IRQ–	= (PINTD– * ENINTD+) + (PINTC– * ENINTC+) + (PINTB– * ENINTB+) + (PINTA– * ENINTA+)
TSTDIS	= disables the PLA for testing

Figure 5-8. Interrupt Generation PLA (U104) Equations

$\overline{\text{ISA}}$– = PSEL1+ + PSEL0+ + $\overline{\text{DVCMD}}$–	(Input strobe for Port A)
$\overline{\text{ISB}}$– = PSEL1+ + $\overline{\text{PSEL0}}$+ + $\overline{\text{DVCMD}}$–	(Input strobe for Port B)
$\overline{\text{ISC}}$– = $\overline{\text{PSEL1}}$+ + PSEL0+ + $\overline{\text{DVCMD}}$–	(Input strobe for Port C)
$\overline{\text{ISD}}$– = $\overline{\text{PSEL1}}$+ + $\overline{\text{PSEL0}}$+ + $\overline{\text{DVCMD}}$–	(Input strobe for Port D)
$\overline{\text{SRQ}}$– = $\overline{\text{PSEL1}}$+ * $\overline{\text{PSEL0}}$+ * $\overline{\text{OSA}}$– * $\overline{\text{SRQ}}$– * $\overline{\text{SACK}}$–	(SRQ– for Port A)
+ $\overline{\text{PSEL1}}$+ * $\overline{\text{PSEL0}}$+ * $\overline{\text{OSB}}$– * $\overline{\text{SRQ}}$– * $\overline{\text{SACK}}$–	(SRQ– for Port B)
+ PSEL1+ * $\overline{\text{PSEL0}}$+ * $\overline{\text{OSC}}$– * $\overline{\text{SRQ}}$– * $\overline{\text{SACK}}$–	(SRQ– for Port C)
+ PSEL1+ * PSEL0+ * $\overline{\text{OSD}}$– * $\overline{\text{SRQ}}$– * $\overline{\text{SACK}}$–	(SRQ– for Port D)
+ INHIB+	(assert once per OS*)
+ SRQ– * SACK–	(assert until SACK)
INHIB+ = SACK –	(assert INHIB+)
+ INHIB+ * $\overline{\text{PSEL1}}$+ * $\overline{\text{PSEL0}}$+ * OSA–	(assert INHIB+ until $\overline{\text{OSA}}$–)
+ INHIB+ * $\overline{\text{PSEL1}}$+ * PSEL0+ * OSB–	(assert INHIB+ until $\overline{\text{OSB}}$–)
+ INHIB+ * PSEL1+ * $\overline{\text{PSEL0}}$+ * OSC–	(assert INHIB+ until $\overline{\text{OSC}}$–)
+ INHIB+ * PSEL1+ * PSEL0+ * OSD–	(assert INHIB+ until $\overline{\text{OSD}}$–)
TSTDIS– = disables the PLA for testing	
Note: The signal INHIB+ is generated by the PLA and is input back into the PLA to generate SRQ–. It does not go out onto the board.	

Figure 5-9. Port Processor Handshake PAL (U204) Equations

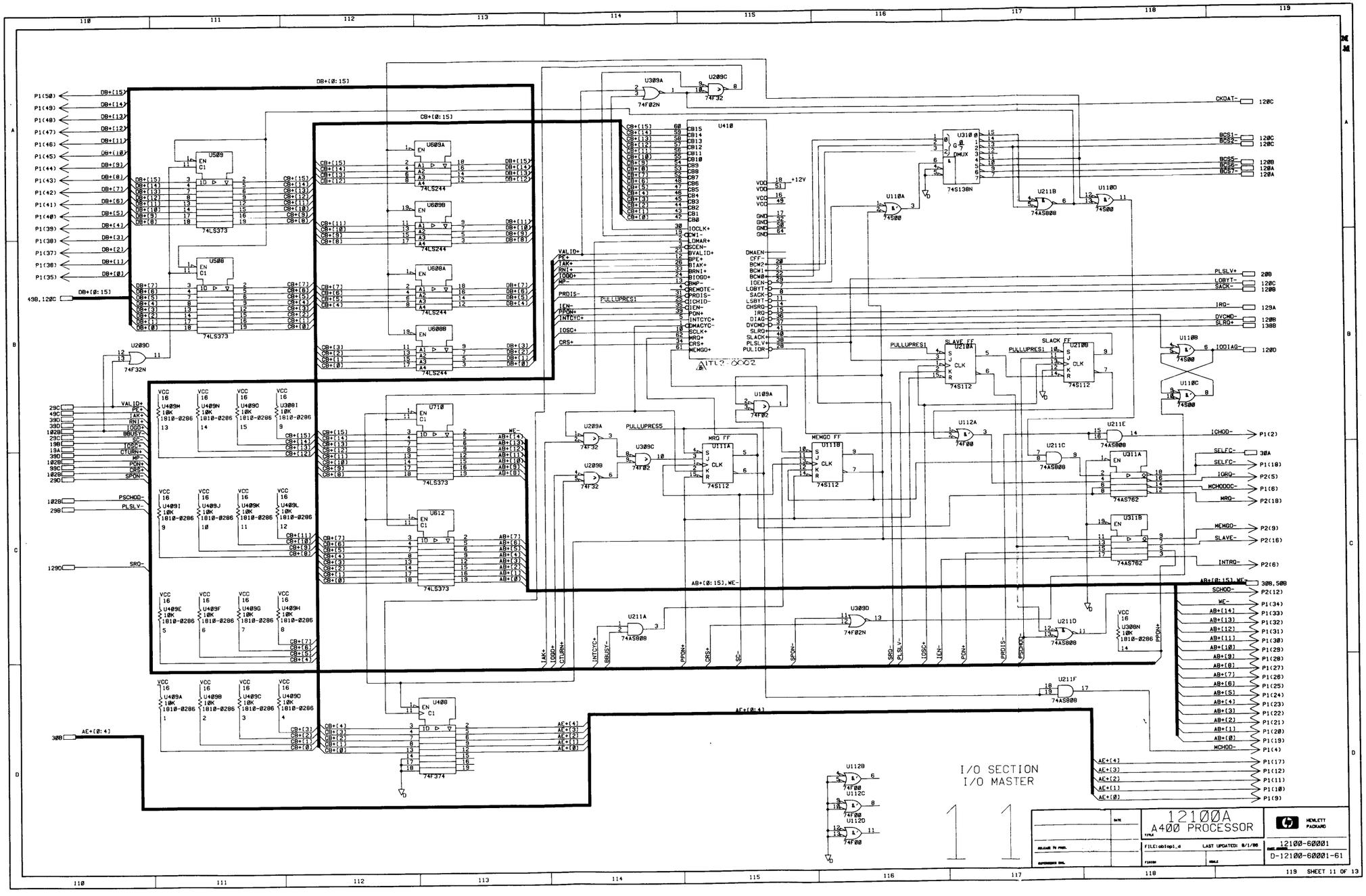


Figure 5-10. I/O Section I/O Master Schematic Diagram

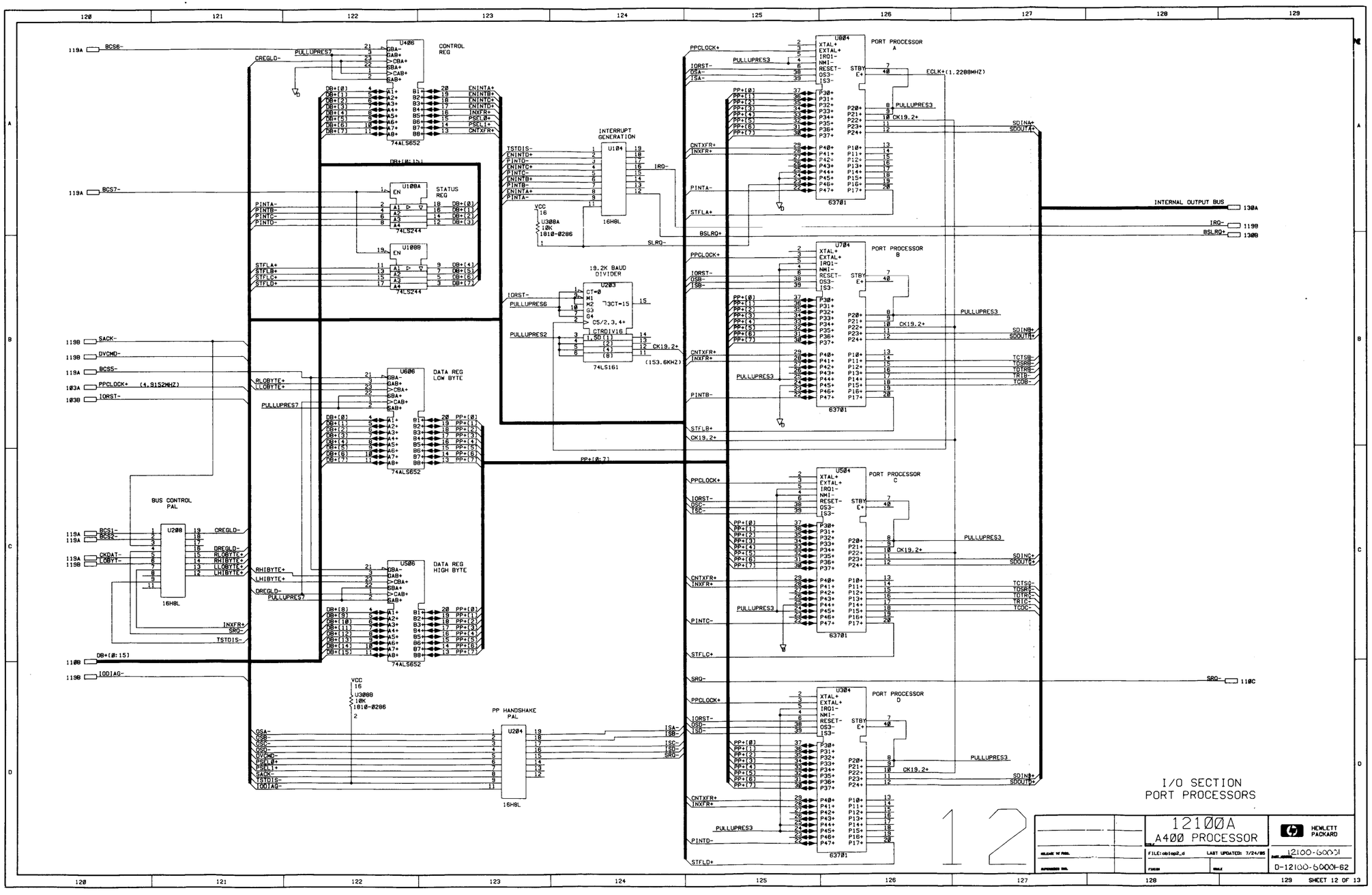


Figure 5-11. I/O Section Port Processors Schematic Diagram

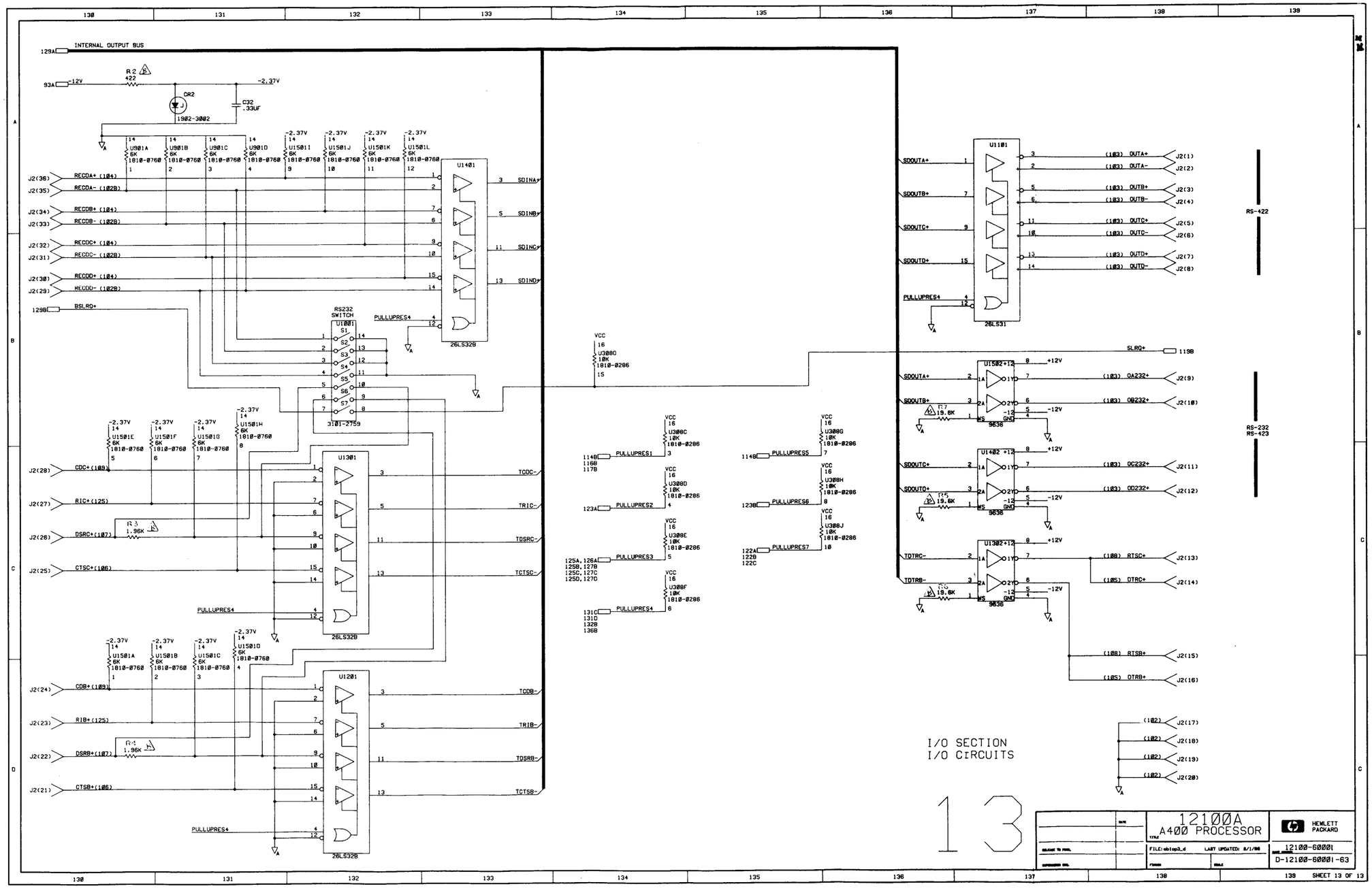


Figure 5-12. I/O Section I/O Circuits Schematic Diagram

6

Memory Arrays

Introduction

The A400 Computer allows main memory expansion beyond the 512k bytes of on-board memory by adding memory array cards. This chapter covers memory array cards supported by the A400. The A400 processor supports the following memory array cards (parity only):

HP 12103C	512k byte parity array card	(part no. 12103-60003)
HP 12103D	1M byte parity array card	(part no. 12103-60004)
HP 12103K	2M byte parity array card	(part no. 12103-66001)
HP 12103L	4M byte parity array card	(part no. 12103-66002)
HP 12103M	8M byte parity array card	(part no. 12103-66003)

A maximum of four array cards are allowed. This number may consist of four 12103K/L/M array cards or a mix of 12103K/L/M and the 12103C/D array cards. If four 12103M array cards (8-Mbyte cards) are installed in a system, then the maximum of 32 Mbytes of main memory will be present.

These memory array cards are also used in the A600+ and A700 computers. The A400 and A600+ computers access the memory array cards identically. The A700, however, uses some circuitry on the memory array cards that is not used by the A400 and A600+. The differences will be pointed out in the appropriate sections of this chapter.

The 12103B 256k byte memory array card is not supported by the A400 and A600+ computers because its addressing is not compatible with the memory controllers of those computers. The 12103D has a different parts layout to accommodate twice the number of RAMs as the 12103C array card. These memory array cards are described as though there were one basic card but the differences on them are mentioned wherever a difference exists.

The newer 12103K/L/M arrays have a slightly different design and are described in the second half of this chapter. These memory array cards use the same PC layout, the only difference being the amount of RAMs loaded and the memory configuration Programmable Logic Array (PLA) on each capacity card.

Physical Characteristics

The memory array cards are installed in the backplane above the A400 board. Additional array cards are added in successive fashion with the memory frontplane connecting each array card.

All signals and data are Schottky-TTL levels and comply with Schottky-TTL design rules. No jumper or switch settings are necessary for configuring the array cards for insertion into the system (jumpers on the cards are preset at the factory for the size of memory on the card).

The power supply specifications for the cards are covered in Chapter 1. The total operating power is not the summation of the operating power specification of each card. This results from the fact that power consumption is proportional to the access rate and only one card is accessed at any one time. Therefore, only one card at a time is operating. Meanwhile, all other array cards dissipate standby power.

The numbers listed for +5M in the Addressed column are the maximum that an array will draw at the fastest access rate. The less frequently that the memory system accesses the array, the less the current draw on +5M will be. This is due to the RAM, whose current consumption is proportional to access rate.

12103C/D Memory Array Card Operation

Array Card Configuration

The memory array cards in the A400 memory system serve as an extension of the data storage space provided by the on-board memory. Operation of the memory array cards is described below. A memory array card block diagram is shown in Figure 6-1.

Each array card, when installed, occupies a unique address space so that the controller may access it by address only. To accomplish this, each array card has an adder that takes a chained address from the previous card, adds the number of rows of RAMs on the card, and passes this incremented address over the frontplane to the next higher array card in the backplane. A value of one is added to the memory chain for every 128k bytes of memory.

These incremented addresses are essentially the starting address for each array card and, when compared to the physical address (on the frontplane), form a basis for selecting the array cards. For example, the address received by the first card above the A400 board is 0004 (octal), indicating the 512k bytes of on-board memory.

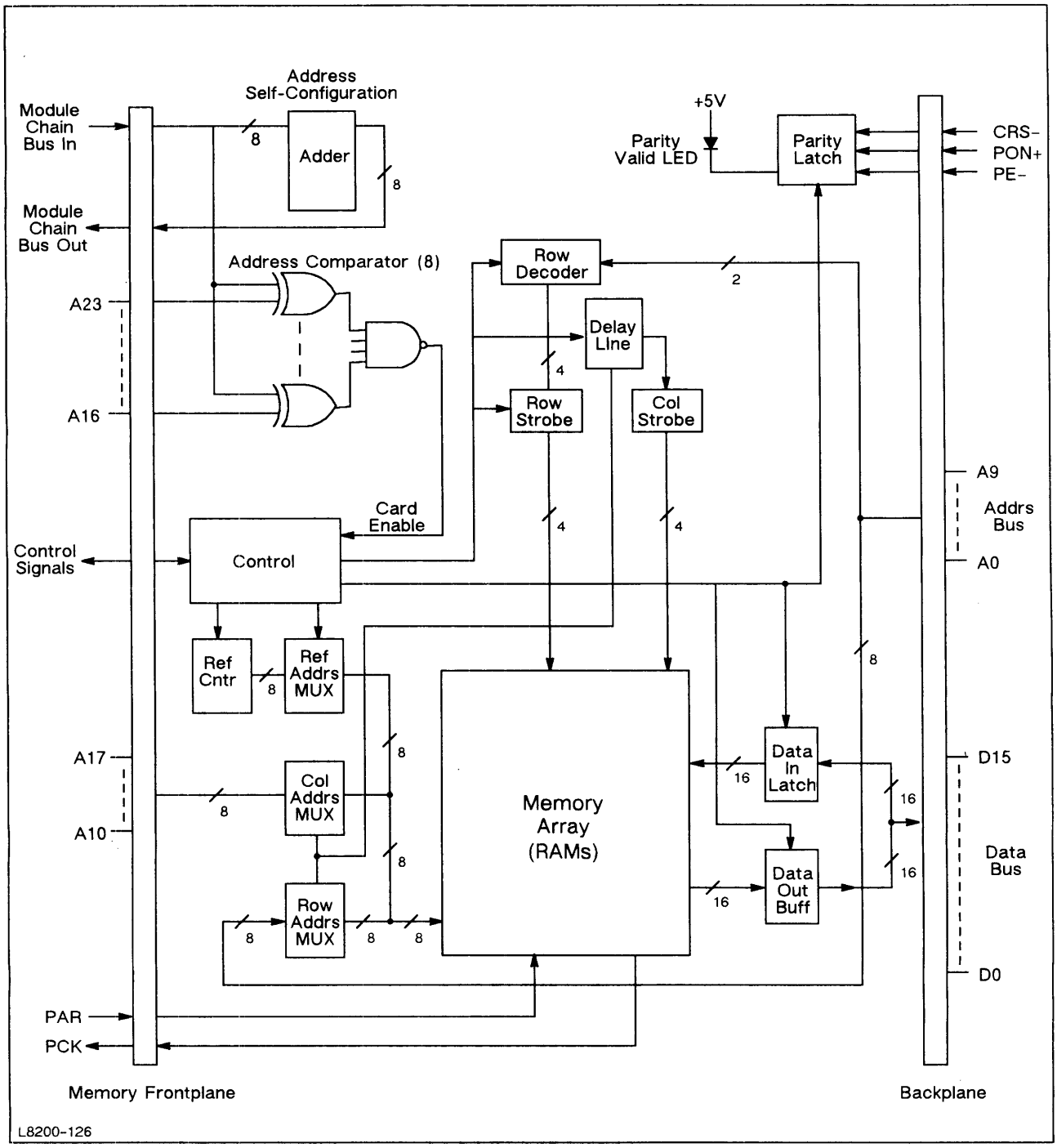


Figure 6-1. Memory Array Card Block Diagram

Since each array card sends an incremented number equal to the number of rows of RAMs on the card to the next array card, the array cards automatically configure themselves in an ascending address order. Thus, if two cards are interchanged, they automatically reconfigure themselves to form the ascending address sequence. The advantage of this scheme is that identical memory modules become unique in the address space of the computer without the aid of manually selected switch or jumper settings unique to the location or dedicated backplane locations. There is a rule, however, that must be followed when adding memory array cards to a system. This rule is explained in the Theory of Operation section.

Array Card Select

Each memory array card receives the physical address sent by the memory controller over the frontplane. Using XOR gates, the cards compare the physical address with the incremented address (see previous paragraph). When a match is encountered on a card, the outputs of all its XOR gates go high causing its card select line to go true (this can happen on only one array card at a time). When a card select line is true that card is enabled for access to the RAM array.

RAM Array

The RAM array consists of dynamic MOS memory elements in 16-pin Dual In-line Packages (DIPs) with 64k bits per package. The RAMs are arranged on the 512k byte array card in rows of 17 to provide sixteen data bits plus one parity bit. The 512k byte card has four rows of RAMs and the 1M byte card has eight rows of RAMs.

Each word of data written into memory is stored in one row of the array. Thus, during any access only one row of RAMs is activated. (This is not true of refresh cycles which access all rows of all array cards simultaneously.) One row of RAMs is accessed on every memory card in the system during every memory cycle (two rows are accessed on the 12103D).

Row Decoding

Row decoding is used to select a row of the RAM array for access. Bits 8 and 9 of the logical address from the backplane are routed to the decoder which performs a one-out-of-four decoding function. The outputs of the decoder are then fed to the row address strobe (RAS) buffers. The RAS signal to the RAMs performs the chip select function in concert with the CAS signal. On the 1M byte card, address bit 18 is used to select a bank of four rows of RAMs with bits 8 and 9 selecting a row within the bank.

Strobe Generation

The RAM elements need two strobe signals to allow access to the array. This is necessary since the RAM elements on the memory array cards are organized into a 64k x 1 matrix and thus require a 16-bit address to identify each memory cell. Since the RAM is housed in a 16-pin DIP package, there are an insufficient number of pins to allow direct addressing. Therefore, the 16-bit address is split into two groups of eight which are the lower-order address and the upper-order address (ROW and COLUMN).

The procedure for accessing the RAM cell is as follows:

1. Set up ROW address at RAM input.
2. Apply RAS strobe to RAM.
3. Set up COLUMN address at RAM input.
4. Apply CAS strobe to RAM.

The timing of these two strobes is critical for efficient memory timing. Therefore, a delay line is incorporated on each array card to ensure a tightly controlled time spacing between the RAS and CAS signals. Thus, when the RAS pulse arrives from the controller and is asserted at the RAMs, the CAS pulse occurs a precise time later at the RAMs.

Address Multiplexer

The timing of the multiplexer switching of the ROW and COLUMN addresses is just as critical as the timing of the RAS and CAS pulses. To ensure the correct timing between strobes and address switching, the same delay line is used to switch the multiplexer from ROW address to COLUMN address. This signal occurs from an intermediate tap on the delay line.

A third group of address bits is the refresh address needed for the memory refresh operation. Only seven bits of address are needed by the RAMs since refreshing is done by rows in the RAM elements. This address is switched to the RAMs during every refresh cycle. Control of the refresh multiplexer is handled from the controller by the REF+ signal over the frontplane.

Data Latch

During a write cycle, data is latched on each array card at the beginning of the memory cycle. The latch signal is generated on the controller and is routed to all array cards over the frontplane. The latching function occurs on all array cards even though the data is only being written to one particular card.

Parity Status LED

The green parity error LED is controlled by a NAND-latch circuit on each array card which monitors the PE– signal on the backplane and the card select signal. Thus, when a parity error occurs, the A400 asserts the PE– signal and the appropriate LED is turned off. Note that this parity error detection scheme does not detect multiple-bit errors.

The latch circuit can be reset by asserting a CRS (Control Reset) signal on the backplane (execution of a CLC 0 instruction). Also, the latch is initialized during system turn-on by the PON signal.

12103C/D Theory of Operation

The integrated circuit packages (chips) are referenced by their U-numbers and schematic locations. For example, U69 (13C) means chip 69 on schematic sheet no. 1 is located by coordinates 13 and C; where the horizontal grid on sheet no. 1 is numbered 10, 11, etc, and on sheet no. 2 it is numbered 20, 21, etc. In the text all chip references for the 12103A/C cards are followed by a chip reference for the 12103D in brackets [#], if it is different. The schematic locations are included in the same way (see Figures 6-5 and 6-6 and the schematics for these cards located at the end of this chapter).

Self-Configuration

The module addressing circuit is used to automatically configure the array cards into the address space of the A400 Computer. This is accomplished by using eight chained lines (the MI and MO lines) on the memory frontplane to allow the passing of unique addresses to each array card. Each array card uses the address sent to it as the starting address of its address space.

Each array card receives a base address over the frontplane MI chain lines which tells the array card the addresses that are recognized by the cards below it. The array card adds its size to this value and sends the new value over the MO chain lines. These MO lines are tied to the MI chain lines for the next array card. A one is added to the value on the memory chain for every 128k bytes of memory on a card. The memory on the A400 board, therefore, sends the value four out over the MO chain lines to the first memory array card indicating the 512k bytes of on-board memory.

The value received by each array card is used as the starting address of that array card. In this manner, each array card is located on a unique address boundary in the memory address space. Also, each array card is in sequence with the others; the beginning of memory is located on the A400 board and the end of memory is on the array card farthest from the A400 board. Figure 6-2 is a block diagram of the module addressing circuitry.

The module addressing circuit is implemented by using two 4-bit full adders U102 (23B) and U202 (23A). These adders are connected in cascade to perform full 8-bit addition. Jumpers located at W1, W4, and W7 determine the capacity of the array card by setting the number to be added to the incoming address to form the outgoing address for the next array card. The use of these jumpers allows the manufacture of three different size array cards from a single board, the only difference being the amount of RAMs loaded on the board and the jumper placement. The 12103A (128k bytes), 12103B (256k bytes), and the 12103C (512k bytes) memory array cards were all manufactured from the same board. The 12103A/B, however, are no longer manufactured. The 12103D (1M byte) adds eight to the memory chain address using just one 4-bit adder U113 (11A).

The 12103C has four rows of 17 RAMs of capacity. Since 64k RAMs are used, the capacity of each row is 64k words or 128k bytes of memory. The jumpers are set at the time of manufacture. The card will then send the correct incremented address to the next array card when installed in a system. The 12103D 1M byte card cannot be partially loaded, and therefore it has no jumper options.

In operation, the eight bits of chained address (the MI lines) are compared to the upper eight bits of physical address present on the memory frontplane. (The lower order 16 bits are used to address locations in the RAM chips themselves.) These upper eight bits are used to determine which card is to be selected when a given address is present. The card select signal is generated by the NAND gate U204 (23C) [U1402 (13B) on the 12103D].

This eight input gate receives the outputs of the XOR gates at U103 (22D) and U203 (22C) [U1202 (11B) and U1302 (12B) on the 12103D]. In operation, the outputs of all the XOR gates must be high for the card to be selected in the following way: The physical address is low true while the chained address is high true so that the comparison of these two signals is equal when one is low and the other is high. The output of each XOR gate under the equal condition is, therefore, high.

In the case of a 512k byte array, jumpers W5 and W6 are both present to allow address decoding to select all four rows of the array card. Jumpers W2 and W3 are not present and the corresponding inputs of U204 are pulled high so that the card select circuit ignores bits A16 and A17. Thus, the card remains selected while bits A16 and A17 select the desired row of RAMs. Jumper W7 is present to add a four to the chain address.

The 12103D card is selected on a match of bits A19 through A23. It uses bit A18 to select a bank of four rows of RAMs and bits A8 and A9 to select a row within that bank. The 12103D has no jumper options.

For example, A400 sends out MI[3:0]=0100 to the next array. If this next array is 512k bytes, then it has the jumpers on the two lower gates removed. Therefore, A16 and A17 are not used to select this card; they are used to select the row of RAMs on the selected card. If the address requested is between 0 and 512k bytes, only A[0:17] are required and A[18:23] are deasserted (logic 1). Because MI2=1 on this card, the XOR gate associated with A18 is disabled, thus deselecting this card (the on-board 512k bytes does the accessing for addresses 0 through 512k bytes). If an address between 512k bytes and 1M byte is required, bit A18 is asserted low. This enables the XOR gate associated to A18 (the gates for A19 through A23 are also enabled because A[19:23]=11111 and MI[3:7]=00000) and, therefore, this card is selected.

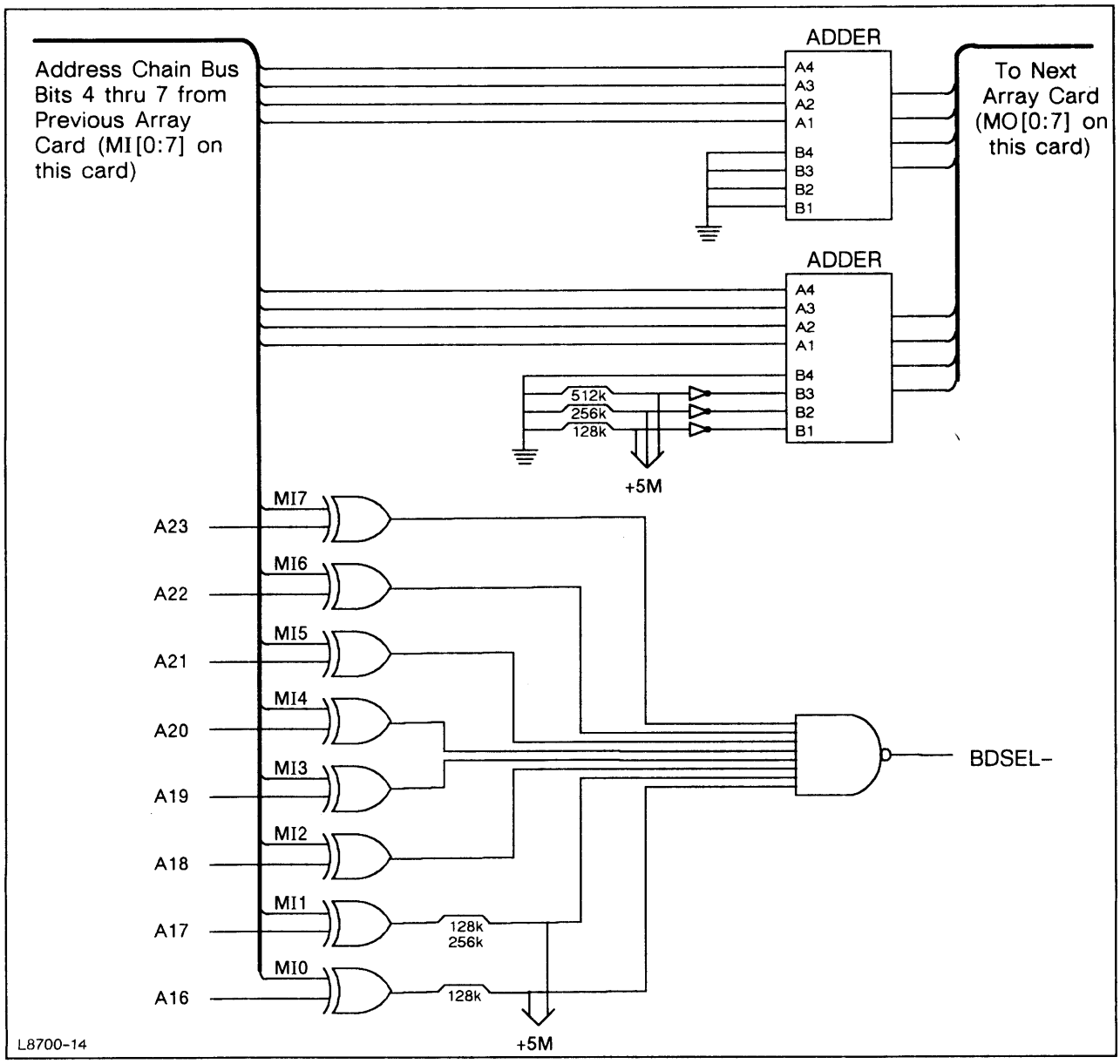


Figure 6-2. Module Addressing Circuitry Block Diagram for 12103A/B/C

An important restriction must be placed on the position of partially loaded array cards in the computer system. All cards MUST be located on an address boundary where the starting address for the card can be evenly divided by the memory capacity of the card. That is, a 512k byte card can only be installed where its starting address would be an even multiple of 512k bytes and so on. An example of an incorrect installation would be to have a 1M byte card installed as the first card next to the 512k bytes of on-board memory. The correct installation is to install a 512k byte card next to the A400 board and then install a 1M byte card next to that. Table 6-1 gives examples which illustrate the order of memory array card placement.

The reason for the restriction is that the jumper scheme assumes that row selection on a 512k byte card occurs with address bits 16 and 17 going through the sequence of 00, 01, 10, 11 with no change on address bit 18, and thus is located on a 512k byte boundary in the address space. If address bit 18 did change, the card could not remain selected.

Similarly, the 1M byte card only looks at address bits A19 through A24 for board selection, and assumes that memory chain bits MI0, MI1, and MI2 are all low, which only happens on 1M byte boundaries.

Table 6-1. Memory Array Card Configuration

Rule: Arrange memory array cards so that the size of memory (including on-board memory) installed in the backplane satisfies the following equation.

$$\frac{\textbf{Memory Size Now in Backplane}}{\textbf{Size of Array Card to be Added}} = \textbf{An Integer}$$

Examples:

Right

12100A	(512)		
12103C	(512)		
12103D	(1024)	$\frac{2048}{512}$	= 4
12103C*	(512)		

12100A	(512)		
12103C	(512)		
12103D	(1024)	$\frac{2048}{1024}$	= 2
12103D*	(1024)		

Wrong

12100A	(512)		
12103C	(512)		
12103C	(512)	$\frac{1536}{1024}$	= 1.5
12103D*	(1024)		

12100A	(512)	$\frac{512}{1024}$	= 0.5
12103D*	(1024)		

* Array card to be added

RAS Generation

The RAS (Row Access Strobe) pulse is used to initiate every access and to perform refreshes to the RAM array. It is generated on the array card by the RAS flip-flop U503 (13D) [U1212 (13C) on the 12103D] when the GO+ signal is asserted by the A400. The PHXRAS- line is pulled up (disabled) by the A400.

When the RAS pulse occurs, the proper row of RAMs to be accessed has already been determined, and the appropriate RAS driver is enabled by U303 (15D) [U307 (25B) or U407 (25C) on the 12103D]. RAS then passes through to the selected row.

Row Selection

The proper row of memory to be accessed is determined by logical address bits 8 and 9 from the backplane. These bits are routed to multiplexer U402-2 and -5 (13E) [U1213-2 and -5 (13D) for the 12103D]. The A inputs of this multiplexer are selected so that the address bits pass through to U302-3 and -2 (14E) [U207 (22D) for the 12103D] which is a one-to-four decoder. This decoder determines which row to enable from the binary code on the address lines and sets the appropriate line high to the RAS drivers of U403 [U807 and U907].

During refresh cycles, all four outputs of the multiplexer are high to enable RAS to all rows simultaneously. This occurs by asserting the BREF+ signal at U303 (15D) [U307 at 25C and U407 at 25B] high for the duration of the refresh cycle.

Card Select Control

When the correct address is present on the frontplane, the card select circuitry enables the appropriate card as described in the Module Addressing Circuit section. The card is enabled by the card select signal BDSEL (Board Select) generated at U204 (23C) [U1402 (13B) for the 12103D]. This signal enables the card for a memory access in several ways.

First, the BDSEL line is sent to NAND gate U210 (14D) [U812 (26E) for the 12103D]. At U210 pin 9 [U812 pin 12], the DRIVE signal is enabled so that the array card may drive the backplane if the present cycle is a read access. In the case of a write access, the WRITE+ signal at U501 (16D) [U107 (27E)] is enabled to the RAMs.

In the A400 and A600+, the state of BDSEL- at U303 (15D) on the 12103C and the state of BDSELL and BDSELH at U307 and U407 (25B,C) on the 12103D does not matter. This is because the LTNG- signal is asserted at U302 (14E) [U207 (22D)] which makes the A and B inputs to U303 [U307 and U407] identical. This results in a row of RAMs receiving a RAS pulse whether or not the card is selected.

In the A700, however, the BDSEL- line at U303 (15D) on the 12103C switches the multiplexer to select the proper row of RAMs as described in the previous section. On the 12103D, the BDSEL line is decoded with A18 by U812 (22E) to produce bank select signals BDSELL and BDSELH. BDSELL goes to U307 (25C) and BDSELH goes to U407 (25B), allowing the proper row of RAMs to be selected.

Therefore, in the A700 only, when the card is not selected, the multiplexer at U303 [U307 and U407] selects the B inputs. These inputs are all high since the LTNG– signal at U302 (14E) [U207 (22D)] is high in the A700. This causes the outputs of U303 [U307 and U407] to be low which disables all RAS driver inputs at U403 [U807 and U907] so that no rows are selected.

CAS Generation

The CAS (Column Access Strobe) pulse is used to strobe the second half of the address into the RAMs during a memory access. The CAS pulse to the RAMs is generated from the RAS pulse through the use of a delay line located at U601 (15C) [U1607 at 24E]. The delay inserts the minimum time required for the RAM address bus to switch from the row address to the column address.

The CAS pulse is sent to CAS drivers U603 (14B,C) [U1207 at 24D and U1307 at 27D]. Note on the schematic that the CAS pulse only appears at the RAMs if the CASEN (CAS Enable) signal is asserted. Since the delay line signal CAS occurs every time the RAS pulse occurs, the CASEN signal is used to inhibit unwanted CAS cycles during memory refreshes and memory protect violations.

Since the CAS pulse holds the accessed data valid at the output of the memory RAMs during a read cycle, CAS at the RAMs remains asserted until the memory cycle completes. This is done by extending RAS, which holds CAS (otherwise it would terminate 60 nanoseconds after the controller RAS signal terminates).

In operation, the CASEN and VALID signals are gated by U501 pins 1 and 2 (13C) [U912 pins 4 and 5 (13C)], and present an extended RAS signal to U502 (14C) [U107 (15C)]. Thus, RAS to the RAMs is extended to the end of the VALID signal and the delay line CAS is correspondingly extended. This provides sufficient extra time for the delay line CAS to hold data valid until the end of the memory cycle.

Address Multiplexer

The addresses used by the memory RAMs are controlled by the address multiplexer chips U107 (12A), U108 (12B), and U109 (12C). For the 12103D the multiplexer chips are U902 (21A), U413 (21B) and U213 (21C) for the low bank; and U901 (22A), U513 (22B), and U313 (22C) for the high bank.

The address multiplexer presents the row and column addresses as well as the refresh addresses to the RAMs. U109 [U413 and U513] is used to latch the lower-order eight bits of physical address directly from the backplane. The output of this latch is used as the row address to the RAMs. After the RAS pulse occurs and the address hold time at the RAMs is satisfied, the delay line asserts the COLEN signal at U401 pin 13 (11C) and U501 pin 9 (12C) [U512 pin 2 (23C) and U912 pin 10 (23B)] which disables the output of the row driver U109 [U413 and U513] and enables the output of the column driver U108 [U901 and 902].

After the column address has had sufficient time to settle, the CAS pulse is asserted at the RAMs.

When a refresh cycle is initiated, the REF+ signal appears at U401 pin 12 (11C) [512 pin 1 (23C)] and inverted at U501 pin 10 (12C) [U912 pin 9 (23B)]. This signal disables the outputs of both the row and column address drivers U109 and U108 [U413, U513, U901, and U902] and enables the refresh address driver U107 [U213 and U313]. This presents the refresh address to the RAMs.

Address Latch

The lower order ten bits of physical address are latched directly from the backplane. Bits 0 through 7 are latched by U109 [U413 and U513] and are presented to the RAMs as the row address. Bits 8 and 9 are latched by U214 (11E) [U1013 (12D)].

Data Latch

Data is latched directly from the backplane using U111 (18B) and U211 (18A) [U813 (38B) and U913 (38B)]. These latches are transparent so that as data becomes available on the backplane, it is sent to the RAMs before the LATCH signal freezes the latch. These latches hold the input data at the RAMs during every write cycle.

Backplane Data Drivers

Data is driven onto the backplane by two octal drivers U112 (18C) and U212 (18C) [U613 (38D) and U713 (38C)]. The outputs of these drivers are enabled by the BDRIVE signal whenever the card is selected and the memory access is a read cycle.

Parity LED Latch

Whenever the parity of data being accessed from the card is not correct, the controller asserts a parity interrupt signal to the processor and memory array. This is the PE- (Parity Error) signal line. A memory array card must be selected to monitor the PE- signal. The PE- signal is received at U220 pin 13 (18E) [U512 pin 12 (14E)] and if the BDRIVE- signal is asserted at U220 pin 11 [U512 pin 13], latch U220 [U912 and U612] will be reset, turning off the parity LED. This will identify this card as causing the parity error. The latch can be set again by issuing a CRS- (Control Reset) signal or by cycling the system power.

Refresh Counter

Refresh addresses are generated on the array card. Counter U106 (11A) [U312 (21D)] is used to count in a binary sequence to generate the 128 row addresses needed for refresh cycles. Note that eight bits are generated and sent to the RAMs but only seven are needed. The counter is clocked by the COUNT+ signal from U210 (10B) [U412 (20D)] which is a gated from of the REF signal. The counter is clocked at the end of each refresh cycle so that the refresh address is set up in time for the next refresh cycle.

Frontplane Handshake Signals

There are two signals passed over the frontplane from the standard array card to the A400 board whenever a memory access takes place. These are the ACK- (Acknowledge) and PCK- (Parity Check) signals. Both signals are sent to the A400 board by the open collector driver U206 (24,25D) [U612 (15,16B)]. The driver is enabled when the card is selected.

ACK- is sent as soon as the array card is enabled to inform the A400 board that the address on the frontplane does indeed access an existing array card. The PCK- signal is sent at the time that the parity bit has been accessed from the parity RAM. This is used in the parity checking process.

12103K/L/M Memory Array Card Operation

The 12103K/L/M Memory Array cards are compatible with the existing memory array cards and controllers without modification. These cards are standard parity arrays (that is, non error-correcting) which makes use of the most current release dynamic RAMs (1-Megabit DRAMs).

Array Card Capacity

The 12103K/L/M use 1-megabit x 1 DRAMs. The array cards have a maximum capacity of 8 Mbytes. This is implemented as four rows of 17 RAMs each (16 rows for data and 1 row for parity). Each row stores 1 megaword (16-bit words) or 2 megabytes of data. Therefore, the 12103K array card has 1 row of RAMs loaded with a capacity of 2 Mbytes, the 12103L has 2 rows loaded with a capacity of 4 Mbytes, and the 12103M has 4 rows loaded with a capacity of 8 Mbytes.

Array Card Configuration

The array cards make use of the self-configuration scheme used in the A-Series memory systems. This scheme eliminates the need to set jumpers or switches on the array card when it is installed in a system with existing array cards. It allows the system to uniquely identify the array cards in the memory address space.

The self-configuring circuit performs two functions. First, it establishes the capacity of the memory array card. This depends on how many rows of RAMs are loaded on the board. Second, it generates an address that is used as the starting address of the next (higher address) array card in the computer system.

Both functions are performed by a Programmable Logic Array (PLA). This chip is uniquely programmed for each capacity of array card. In other words, for the three capacity configurations (2, 4, and 8 Mbytes), three unique PLAs exist.

Card capacity is controlled by the PLA. For example, assuming that all four rows of RAMs are loaded, an 8 Mbyte array can be converted into any capacity simply by changing the PLA. However, disabling existent memory with PLAs will not normally be done. Array cards are loaded with the desired number of rows of DRAMs and the PLA programmed for that capacity is installed. PLAs used in this way replace the method of selecting card capacity by using wire jumpers as done in the 12103C/D arrays. Also note that the old memory configuration rules described in the previous section for the 12103C/D arrays no longer apply for the 12103K/L/M arrays.

Array Card Select

The module self-configuring circuit operates by receiving a chained address from the module preceding it, adding an address increment representing the capacity of the array card, and sending the incremented address to the next array card in the system. The address received by the next array card is the starting address of its memory address space. The incremented address sent to the next array card is the starting address for that array card.

When data is required from memory, the physical address of the memory location is sent over the frontplane by the memory controller. If this address is located on this array card, the select circuitry enables the card. Only one array card is enabled at any given time.

The select circuitry uses magnitude comparators to determine if the desired address exists on this array card. This scheme allows for detecting starting addresses with 512-kbyte resolution. This means that the array card can be installed on 512-kbyte boundaries in the memory address space in a given computer system.

Strobe Generation

The DRAMs need two strobe signals to allow access to the array. This is necessary because the DRAMs are organized into a 1-megabit x 1 matrix and require a 20-bit address to access each memory cell. Because the DRAM is housed in an 18-pin DIP package, there is an insufficient number of pins to allow direct addressing. Therefore, the 20-bit address is split up into two groups of ten, which form the lower order and upper order address (Row and Column).

The procedure for accessing the DRAM cell is as follows:

1. Set up Row address at DRAM input
2. Apply RAS strobe to DRAM
3. Set up Column address at DRAM input
4. Apply CAS strobe to DRAM

The timing of these two strobes is critical for efficient memory operation. A delay line is incorporated on each card to ensure a tightly controlled time spacing between the RAS and CAS signals.

In the A400 system, these two signals are derived from SCLK with MEMGO- as a qualifier. The Row and Column address multiplexing to the DRAMs is also controlled by the same delay line.

Row Decoding

Due to the late arrival of the mapped address from the A400 (and A600+), the array rows cannot be decoded before the RAS signal occurs. There is only enough time to select the board in which the memory access will occur. (The row selection circuitry has a longer delay path.)

In the 12103C/D array card designs, which use slower DRAMs, there is enough time for row decoding before RAS. The reason is that the 64k DRAMs need only 16 address bits for accessing a memory location (8 bits for row address and 8 bits for column address). When the RAS pulse occurs, the 8-bit row address is available at the DRAM and the row that the DRAM is in is selected.

This requires that 10 bits of address be available early in the memory cycle. These address bits are taken directly from the lower 10 bits of the physical address. This address is the displacement address for locations in a page of main memory and does not come from MAP RAMs.

The 1-Megabit DRAMs need 20 address bits to access a memory location, 10 for row and 10 for column. In this case, all 10 bits of the displacement address are used early in the memory cycle without any left for row selecting. As a result, the RAS pulse is presented to all DRAMs on the array card that is selected. The CAS pulse is used to decode which card row is to be enabled.

The effect of presenting a RAS pulse to card rows not accessed causes a "RAS-only" refresh cycle to occur in those rows. This refresh cycle is not considered one of the required refresh cycles (that is, a refresh cycle that is scheduled by the memory controller when the REF+ signal is asserted). This does not alter data there, but does increase the power consumption of the memory array.

Parity Status LED

The memory array card provides a parity status indication identical to the 12103C/D array cards. This LED is normally lit (no-fault condition). It is extinguished if a parity error occurs on a data access from this array card.

12103K/L/M Theory of Operation

The integrated circuit packages (chips) are referenced by their U-numbers and schematic locations. For example, U69 (13C) means chip 69 on schematic sheet no. 1 is located by coordinates 13 and C; where the horizontal grid on sheet no. 1 is numbered 10, 11, etc, and on sheet no. 2 it is numbered 20, 21, etc. See Figures 6-5 and 6-6 and the schematics for these cards located at the end of this chapter.

Self-Configuration

The memory arrays automatically configure themselves into the address space of the host memory system. This is accomplished by receiving a chained address from the memory frontplane, incrementing this address, and sending the incremented address along the frontplane chain to the next array card in the system.

The input address consists of 8 bits designated as MI[0:7]. These 8 bits are used as the upper-order bits of the starting address for the array card. They are compared to the 8 upper-order address bits of the memory address sent to the array card by the memory controller during a memory access. These bits are designated as FPAD-[16:23].

In effect, the MI address can be viewed as a 24-bit address whose 16 lower-order bits are always zero. Therefore, the MI address always represents an address that is a boundary between 64k words (128 kbytes) of memory.

The smallest array of memory that can be added to the system using the 12103K/L/M cards is 2 Mbytes. However, to make the installation of the arrays more flexible, the configuration circuitry can recognize 512-kbyte boundaries. This means that a 2-Mbyte array can be installed on a 512-kbyte address boundary in the computer system. This happens, for example, when a 12103K/L/M array is installed as the first array card in an A400 system.

The least significant MI address bit used by the board select circuitry is MI[2]. Also, the LSB of the frontplane address used by the board select circuitry is FPAD-[18]. This allows for the installation of the array card on any address boundary that is an increment of 512 kbytes.

The MI address is received at the inverter pack at U1101(11D). This address is inverted because it is compared to the low-true frontplane address bus. The inverted MI address is sent to the board select comparator at U501(14C). This comparator checks that the frontplane address is greater than or equal to the MI address. The MI address also goes to the addressing PLA at U1301(12C). This PLA adds the proper number to the MI address to form the MO address which is sent to the next array card as its starting address. The MO address is also used as the upper limit of addresses that will select this array card, so it is sent to the comparator at U401(14B). This comparator checks that the frontplane address is less than the MO address.

Note that the operation of the comparators is inverted because the addresses being compared are low-true instead of high-true. That is, a frontplane address that is greater than or equal to the MI address will cause the output of U501 (LOSELECT+) to be asserted. Because the addresses are inverted, the frontplane address is actually less than the MI address. This is why the P<Q output at U501 is used as the output.

The equal function is obtained by tying the P<Q input at U501 high. With this input high, the P<Q output at pin 14 is also high when the P inputs equal the Q inputs of the comparator.

When the frontplane address is less than the MO address, the output of U401 (HISELECT+) is asserted. The frontplane address is actually greater than the MO address (in a positive, numerical sense). This is why the P>>Q at U401 is used as the output.

The equal function is not normally required on the upper limit comparator at U401. Whenever the array card is installed completely within the memory space of the computer (that is, the end of the 32-Mbyte memory space is not located on this array), the equal function is not used and the P>>Q and P<Q inputs at U401 are both low. This causes the comparator output (HISELECT+) to remain low when the P inputs equal the Q inputs. For the special case where the end of memory is located on this array see the Top of Memory section.

The assertion of both HISELECT+ and LOSELECT+ signifies that the frontplane address from the memory controller is accessing a memory location on this array card. These two signals generate the BDSEL– (board select) signal at U1205(15C). This signal is used to enable the array card for the impending data transfer. (This signal is not generated when memory is being refreshed.

The HISELECT+ and LOSELECT+ signals also directly enable the RAS (Row Address Strobe) drivers. All drivers are enabled simultaneously. When the RAS pulse occurs, all rows of DRAM are strobed. The row of DRAMs which actually contains the desired address is selected later with the appropriate CAS (Column Address Strobe) signal.

The MO address is inverted at U1201(16D) and sent to the next array card as its starting address. The MO address is a high-true signal when it is on the frontplane chain lines.

Note that the MI[0:1] lines are routed straight through to the MO[0:1] lines. These lines are not used by the array card but are passed on because they may be used by a 128 or 256 kbyte array card installed down the chain.

Row Address Generation

Each row of DRAM stores 1 Megaword of data, therefore, the 20 address bits MA+[0:19] address each DRAM location. The next two address bits, MA+[20,21] (referred to as A20 and A21), select the four rows of DRAM to be enabled on a given card. Two problems were addressed in order to use A20 and A21 for row selection.

First, the array card must be installable on 1/2-Mbyte address boundaries. This means that each row of DRAM on an array may not have its starting address on a 2-Mbyte address boundary. In order for A20 and A21 to directly do row selection, the rows of DRAM must be located on 2-Mbyte address boundaries. Refer to the following table of addresses.

	512 kbyte	1.5 Mbyte	5.5 Mbyte	8 Mbyte
Address Bit	2 2 2 2 1 1 3 2 1 0 9 8	2 2 2 2 1 1 3 2 1 0 9 8	2 2 2 2 1 1 3 2 1 0 9 8	2 2 2 2 1 1 3 2 1 0 9 8
Starting Addrs.	0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 1 1 0 0 0 1 0 0	0 0 0 0 1 1 0 0 0 1 0 0 0 0 0 1 0 1 0 0 0 1 1 0	0 0 1 0 1 1 0 0 1 1 0 0 0 0 1 1 0 1 0 0 1 1 1 0	0 1 0 0 0 0 0 1 0 0 0 1 0 1 0 0 1 0 0 1 0 0 1 1
	0 0 0 1 0 1 0 0 0 1 1 0 0 0 0 1 1 1 0 0 1 0 0 0	0 0 0 1 1 1 0 0 1 0 0 0 0 0 1 0 0 1 0 0 1 0 1 0	0 0 1 1 1 1 0 1 0 0 0 0 0 1 0 0 0 1 0 1 0 0 1 0	0 1 0 1 0 0 0 1 0 1 0 1 0 1 0 1 1 0 0 1 0 1 1 1
	0 0 1 0 0 1 0 0 1 0 1 0 0 0 1 0 1 1 0 0 1 1 0 0	0 0 1 0 1 1 0 0 1 1 0 0 0 0 1 1 0 1 0 0 1 1 1 0	0 1 0 0 1 1 0 1 0 1 0 0 0 1 0 1 0 1 0 1 0 1 1 0	0 1 1 0 0 0 0 1 1 0 0 1 0 1 1 0 1 0 0 1 1 0 1 1
	0 0 1 1 0 1 0 0 1 1 1 0 0 0 1 1 1 1 0 1 0 0 0 0	0 0 1 1 1 1 0 1 0 0 0 0 0 1 0 0 0 1 0 1 0 0 1 0	0 1 0 1 1 1 0 1 1 0 0 0 0 1 1 0 0 1 0 1 1 0 1 0	0 1 1 1 0 0 0 1 1 1 0 1 0 1 1 1 1 0 0 1 1 1 1 1
	Next Card Address			
	0 1 0 0 0 1	0 1 0 0 1 1	0 1 1 0 1 1	1 0 0 0 0 0
	8.5 Mbyte	**9.5 Mbyte**	**13.5 Mbyte**	**16 Mbyte**

The above table shows four possible installation locations for the array card. In all cases, each group of four addresses must access a single row of DRAM. Note that only in the last column (8-Mbyte boundary case) do address bits 21 and 20 behave correctly to do row selection, that is, 00 for the first group, 01 for the second group, 10 for the third and 11 for the fourth. In the other three cases, the starting address is not located on an 8-Mbyte boundary, so that the needed 00 to 11 sequence of A21 and A20 is lost (actually, it has just been shifted).

Second, the memory array has all rows of DRAM loaded only in the 8-Mbyte configuration. Because there are 2 and 4 Mbyte versions, we must allow for partially loaded arrays. These empty rows produce "holes" in memory. The board select circuitry correctly enables these array cards for the existing rows, but the next array card in the system must have DRAMs loaded in the corresponding missing rows or memory gaps will exist.

For example, consider the case where two half-loaded (4-Mbyte) arrays, each with rows 0 and 1 loaded, are installed in consecutive card slots. Assume that the first array is installed on the 8-Mbyte boundary. The first array recognizes the first eight addresses in the last column of the table. Row selection is done using A21 and A20, which are 00 for the first four addresses and 01 for the second four. The starting address for the second array is the ninth address (011000). Note that A21 and A20 sequence through 10 and 11 for the eight addresses recognized by the second array. A21 and A20 would, therefore, select the two empty rows on the second array. The problem is hopelessly complicated if the first array is not installed on an 8-Mbyte boundary; A21 and A20 incorrectly select rows on both cards.

The solution is to numerically shift the window of board selected addresses to begin on an 8-Mbyte boundary. This is accomplished by subtracting the positive offset from the nearest lower 8-Mbyte boundary from the incoming frontplane address.

For example, if the starting address of a 4-Mbyte card is at the 5.5 Mbyte boundary (001011), address bits A21 and A20 would assume values of 10, 11, 00 for the eight addresses enabling the card. By subtracting 1011 from the incoming address, the enabling addresses produce an orderly progression of row addresses on A21 and A20 starting from 00.

This situation occurs on every array card simply by subtracting the offset from the nearest lower 8-Mbyte address boundary. Every array card does row selection in its address space starting at row 00. Therefore, it does not matter if partially loaded array cards exist because each array card starts selecting rows from its own 00 point.

The subtraction is performed by two cascaded F283 4-bit adders. These adders are located at U202(13A) and U302(13B). They are positive logic adders, so the frontplane address must be inverted before the offset is subtracted. This inversion is done at the frontplane address receivers at U201(11B) and U301(11B).

The offset is subtracted by adding its 2's complement to the frontplane address. The offset is equal to the number represented by MI[2:5] received by the array card. This number is also represented by bits 18 through 21 of the starting address for the array card. The offset number is inverted at U1101(11D) and is sent to the adders. The number is effectively incremented by forcing a carry input signal to the adders at U202. This line is tied high, providing the carry.

Due to the rather long path taken for the row selection process, the row select signals are not valid before the RAS strobe occurs. As a result, all rows of DRAM are enabled with RAS when the card is selected.

The outputs of the adder at U202 are the shifted A21 and A20 address bits. These bits are designated 1MSEL0+ and 1MSEL1+. These lines are decoded to select one-of-four rows by passing them through a 74F139 decoder located at U402(14B). This pack produces the four distinct row select signals for each row.

The distinct row select signals are gated and inverted by the 74AS158 data selector at U502(17B). This selector prevents the row select signals from enabling the CAS drivers when the array is not selected.

Row Selection

The capability has been provided on the 12103K/L/M memory array cards to increase the capacity beyond an 8-Mbyte card by allowing for 4-Mbit DRAMs to be used. This section describes how the row select signals are generated depending on whether 1-Mbit or 4-Mbit DRAMs are loaded.

When 1-Mbit DRAMs are loaded on the card the addressing PLA located at U1301(12C) asserts the 1MEN– line low. This enables the F139 decoder at U402(14B), allowing the 1MSEL0+ and 1MSEL1+ signals to select one-of-four row select lines. The 1MEN– line is inverted at U1001(14B) and disables the other half of the F139. This forces the output select lines for this half to go high. These lines are the 4MCE0– through 4MCE3– signals.

The row select signals for the 1-Mbit DRAM array card, 1MCE0– through 1MCE3–, are routed to the A select inputs of the AS158 data selector at U502(17B). The row select signals for the 4-Mbit DRAM card are routed to the B select inputs of the data selector.

When BDSEL– is asserted, the A data inputs on U502 appear (inverted) at the outputs. This is a result of the 1M–/4M+ line being driven low. The signals, CE0+ through CE3+, are the enable signals for the CAS drivers at U805(18C), U905(18C), U1005(18B), U1105(18B).

When the array card is not selected for access, BDSEL– is not asserted. This selects the B inputs of U502, but because the B inputs are the 4-Mbit row select lines and are driven from the now disabled section of the F139 (all are high), the B inputs are effectively pulled up. This causes the CE0+ through CE1+ outputs to be driven low, disabling the CAS drivers.

When the card is loaded with 4-Mbit DRAMs, the situation reverses. The new addressing PLA at U1301 now drives the 1MEN– line high. This signal disables the first section of the F139 decoder at U402. This signal is inverted at U1001 and enables the second section of the decoder at U402. In this case, the 1MCE0– through 1MCE3– lines act as pull-up lines and the 4MCE0– through 4MCE3– lines act as row select lines.

The sense of BDSEL– is now inverted at U1001, because 1MEN– is high. So, when the card is selected for access, the 1M–/4M+ line is high, selecting the B inputs of the data selector. When the card is not selected for access, the 1M–/4M+ line is low, selecting the A inputs of the data selector which inhibit the CAS drivers.

Therefore, when 4-Mbit DRAMs are loaded, an access to the card causes row selection with the B inputs (4MCE0- through 4MCE3+) of the data selector. When the board is not being accessed, the CAS drivers are inhibited (inputs pulled low) by the selection of the A inputs of the data selector, which are pulled high by the disabled 1MCE0- through 1MCE3- lines.

Top of Memory

It is possible to fill the entire 32-Mbyte memory space of the computer system. This can be done by installing four 8-Mbyte array cards. Although the module addressing circuit on each array card configures the card for its address location, a difficulty arises with the module addressing circuit on the array card that contains the end of memory.

Recall that the circuit provides a window of addresses which enable the array card. The array is selected when the incoming address is greater than or equal to the lower limit (MI) address and less than the upper limit (MO) address. The MI/MO chained address bus on the frontplane consists of 6 lines: MI[2:7] and MO[2:7]. The starting address for the last 512 kbytes of memory have an MI address of all ones. If the MI address is then incremented to form the MO address (as it would be on the last card) the address overflows; all chain address lines become zero. Because this MO address is used as the upper limit address for the last array card, the MI address will be greater than the MO address. The array cannot be accessed regardless of what address is sent from the memory controller.

The solution is to limit the MO address at the top of memory to all ones. The addressing PLA is programmed so that it will never create an MO address greater than all ones on the frontplane.

Another problem arises, however. The MO address of all ones is used as the upper address limit on the last array card, and the card is only selected if the incoming memory controller address is less than the MO address. Because the MO address is artificially limited to prevent overflow, it does not represent the correct upper address limit. An MO address of all ones really represents the starting address for the very last 512 kbytes of memory in the computer system. However, the array card is not enabled for the last 512 kbytes of memory because it only recognizes addresses less than the generated MO address.

The solution is to change the function of the upper address limit comparator on the array card that contains the top of memory. This requires that the function of the comparator at U401(14C) be changed from a less than condition to a less than or equal to condition. With this condition, the array card is enabled for the last 512 kbytes of memory.

This function is implemented by generating the MTOP- signal using the addressing PLA at U1301(12C). This signal is inverted and appears at U401 which is the P>>Q input of the comparator. MTOP+ is true when the end of 32 Mbytes of memory occurs on this array. It is only asserted on one array card in the computer system.

Excess Memory in Address Space

The maximum memory capacity of the A400 is 32 Mbytes. This limit is set by the computer architecture which provides 24 physical address lines to access memory. The memory configuration circuitry can determine when more than 32 Mbytes of memory is installed.

The MO address sent to the next card in the system must not be greater than the highest address of the system. The addressing PLA on each array card increments its own MI address to produce the MO address sent to the next array. When the MO address would be pushed over the top by this addition, the addressing PLA produces only the maximum address value. This value consists of all ones. This is true even if the incoming MI address is already at the maximum. The MO address sent out is this same maximum value.

With this scheme, any excess memory that is installed will be disabled. For example, if 28 Mbytes of memory already exist in a system, and an 8-Mbyte array is installed, the last 4 Mbytes of the array is never accessed. The MO address being limited to the maximum address effectively turns the 8-Mbyte array into a 4-Mbyte array.

Any further array cards that are added will become 0 Mbyte arrays. This happens because the outgoing MO address on these cards is the same as the incoming MI address. The board select circuitry is designed to select the card if the frontplane address from the memory controller is greater than or equal to the lower address limit (MI address) and less than the upper address limit (MO address). The MTOP+ signal is asserted only on the card that contains the top of memory. The upper address limit comparison always fails for any address that passes the lower comparison and the card or cards are never selected.

Note that this limiting scheme only works with the 12103K/L/M array cards. The 12103C/D arrays use adders instead of addressing PLAs and do not limit the MO address. There are four cards of concern: 128 kbyte, 256 kbyte, 512 kbyte and 1 Mbyte. If any of these cards are installed as the last card in the system, and the memory capacity of the system is exceeded by its addition, the MO address will wrap around. This results in the last card not being enabled. This is because its upper address limit is now less than its lower address limit.

If a given combination of 12103K/L/M and 12103C/D cards exceed the capacity of the system, but the elimination of any one of them results in a capacity of less than maximum, then the 12103C/D cards should be installed in the lower address space (near the A400 board). The 12103K/L/M array cards are then installed as the last cards in the system, and configure themselves correctly to fill up the address space.

Because the 128-kbyte and 256-kbyte cards cannot be installed before the 12103K/L/M array cards, they should not be installed at all if their added capacity causes main memory to exceed 32 Mbytes.

Address Multiplexing

The 1-Megabit DRAMs require a 20-bit address to access all memory cells in the device. There is an insufficient number of pin connections to allow the direct application of the 20-bit address, therefore, the address is split into two 10-bit addresses which are sequentially loaded. These addresses are designated as the row and column addresses.

The column address is derived from the 10 lower-order address bits of the frontplane address bus: FPAD–[10:19]. The row address is derived from the backplane address bus: BPAD+[0:9]. The column address is received at U201(11B) and U601(11A). These receivers are also inverters so that the column address is high-true on the array card.

The row address is received at U308(21B). This receiver latches the address and drives it onto the array as a high-true address. The address is latched for the entire memory cycle because memory cycles may be attempted by the processor or DMA when the array is undergoing a refresh cycle. When this happens, the memory access is held off by the memory controller until the refresh cycle completes. Because the backplane address is only present on the backplane during the actual request for the memory cycle, the array must save the address so that it is available when the delayed memory cycle is performed.

The row and column addresses are sent to the address multiplexer buffers at U305(26A) and U405(26A). These buffers are configured to alternately drive the two addresses to the entire DRAM array. The buffers are controlled by COLEN+, which is normally low when the array is not undergoing a memory access. This signal is routed to the row driver output enable at U405. COLEN+ is inverted at U1205(26A) and sent to the enable input of the column buffer at U305. The state of COLEN+ controls which address is driven to the array. When COLEN+ is low, the row address is driven; when COLEN+ is high, the column address is driven.

Eleventh Address Bit Multiplexing

The capability of addressing 4-Mbit DRAM chips has been built into the 12103K/L/M array cards. In this case, 22 address bits are needed to access all locations in each RAM. This amounts to increasing the row and column addresses to 11 bits each. The result is that the eleventh address bit must be multiplexed to the DRAMs in the same manner as MA+[0:19]. MA+[20,21] are sent to the data selector at U102(23A). When 4-Mbit DRAMs are installed, 1MEN– is high, which selects these two address bits to be applied to the address driver at U205(24A). This address driver is controlled by COLEN+ in the same manner as the main address multiplexer.

When COLEN+ is low, MA+[20] is driven as address 11 of the row address to each row of DRAM. Note that each row has its own separate driver for this address bit. When COLEN+ goes high, the A section of the driver is disabled and the B section is enabled. This drives MA+[21] as address 11 of the column address to the DRAM array.

When 1-Mbit DRAMs are loaded on the array card, 1MEN– is low. This selects the A inputs of the data selector at U102 which are all tied to ground. This low signal is applied to the "address 11" driver at U205. The net effect is that a low signal appears at the DRAM address 11 input whether the row or column address is presently being driven. This is necessary because, even though "address 11" is a no-connect on many 1-Mbit DRAMs, some DRAM suppliers use this pin as a test pin and require that it remain low for normal DRAM operation. Address 11 is designated as A10 on the DRAMs.

Access Strobe Sequencing

To access a memory location, the 20-bit address must be applied to the desired row of DRAM that has this location. The row address is driven by the row buffer at U405(27B) as soon as it becomes available from the backplane latch. The Row Address Strobe (RAS) signal is generated and applied to all rows of DRAM. After sufficient hold time has elapsed for the row address, COLEN+ goes high, enabling the column address to the entire DRAM array. After sufficient time has elapsed for settling of the address, the Column Address Strobe (CAS) signal occurs and is applied only to the row of DRAM that has the desired memory location.

RAS, COLEN+, and CAS are derived from a delay line at U1405(16B). This delay line takes the generated RAS+ signal and delays it until the array card selection has taken place, that is, the array card from which the memory access will take place has its BDSEL– line asserted and all other array cards are disabled. This delayed RAS signal appears at U1405 and is routed directly to the RAS drivers at U805(18C), U905(18C), U1005(18B) and U1105(18B). If this array card is selected and this is not a refresh cycle, the RAS signal is driven to all four rows of DRAM.

A fixed time-delay later, COLEN+ appears at U1405 and is routed to the address multiplexer buffers to switch from row address to column address.

After another time-delay, CAS appears at U1405. This signal is routed to the CAS drivers at U805, U905, U1005, and U1105. If this memory array is selected, only one of the CAS drivers is enabled by one of the column enable signals. CAS propagates through the enabled CAS driver and appears at the appropriate row of DRAM.

By timing the above events with a delay line, memory accesses occur as fast and repeatably as possible. The last tap of the delay line is used to provide a "late RAS" signal used during refresh cycles.

RAS Generation

The RAS signal is generated in two different ways, depending on whether the array card is installed in an A400/A600+ system or an A700 system. When installed in an A400 or an A600+ system, the RAS pulse is generated by monitoring the GO signal sent by the memory controller over the frontplane. When GO is asserted, the system clock, SCLK, sets a flip-flop whose Q output is RAS+.

When the array card is installed in an A700 system, the RAS signal is generated by the PRAS– signal sent by the memory controller over the frontplane. This signal directly drives the preset and clear inputs of the RAS flip-flop, so that the flip-flop output is essentially an inverted duplicate of the PRAS– signal.

In A400 or A600+ operation, the PHX– signal at connector J1 pin 48 floats high. This signifies that the array card is to operate in A400/A600+ mode. PHX– is received at U601(11A), buffered and inverted, then sent to the RAS reset circuit. This circuit consists of the F64 AND-OR INVERT gate at U1002(23C) plus some inverters. When PHX+ is low, LTNG+ is high. This enables the reset gate to reset the RAS signal in A400/A600+ mode.

To start the RAS signal, GO+ is sent from the memory controller and is received at U702(22C). Because LTNG+ is high at U702, GO+ appears at the J input of the RAS flip-flop at U1605(24C). GO+ also removes the reset signal from the flip-flop, because GO– appears at U1002(23C). On the next falling edge of SCLK+, the flip-flop is set, initiating RAS+. Note that PRAS– is routed to the set input of the flip-flop, but because the array card is installed in an A400/A600+ system, this line is not driven by the memory controller and is pulled high by resistor R1.

As the memory cycle progresses, VALID– is asserted on the backplane. This signal is received at U1308(21D), and is gated by BPON+ at U1205(22D). The gated VALID signal, GVLD–, is then sent to the reset circuit to also disable the reset at the RAS flip-flop. GO+ is removed by the memory controller in the middle of the memory cycle, so that GVLD– maintains the disabled reset. When VALID– is deasserted at the end of the memory cycle, the reset circuit turns off the RAS flip-flop, terminating the RAS pulse. The purpose of resetting RAS with the trailing edge of VALID is to extend RAS longer than one SCLK cycle. Because RAS generates CAS (through the delay line), CAS is extended also. This extended CAS signal is necessary to hold accessed data from the DRAMs on the backplane to satisfy data hold-time requirements.

To summarize, in A400/A600+ mode, the RAS pulse is initiated on the rising edge of SCLK– during the assertion of GO+, and is terminated on the trailing edge of VALID– at the end of the memory cycle. This sequence occurs during all normal memory cycles.

RAS generation is different during refresh cycles. GO+ is asserted in the same manner as a normal memory cycle. However, VALID– is not asserted during a refresh cycle. No memory access is taking place, therefore, no backplane handshake is carried out with the processor or I/O card. GO+ sets the RAS flip-flop, initiating the RAS pulse. Because VALID– is not available to keep the RAS flip-flop from being reset, the BREF– signal is routed to the reset gate at U1002. This disables the reset gate for the entire refresh cycle. Instead, the RAS pulse is terminated by causing the RAS flip-flop to synchronously reset. This is done by applying a reset signal to the K input of the flip-flop. For this reason, the GREF+ signal is routed to the K input of the RAS flip-flop at U1605. This causes the RAS flip-flop to reset one SCLK cycle after it was set.

When the array card is installed in an A700 system, PHX– is pulled low by the memory controller. This puts the RAS reset circuitry in A700 mode. GO+ is disabled from appearing at the RAS flip-flop; it is not used in A700 mode. PRAS– is now driven by the memory controller. This signal is routed to the preset input of the RAS flip-flop at U1605. This signal also is routed to the RAS reset circuit at U1002. When PRAS– is asserted by the memory controller, it removes the RAS reset and sets the flip-flop in one action. As the memory cycle progresses, VALID– also disables the RAS reset. When PRAS– is removed by the memory controller, the RAS flip-flop is not reset. The reset occurs when VALID– is deasserted at the end of the memory cycle. This has the action of extending CAS, for data hold-time requirements, as in the A400/A600+ case.

During refresh cycles, VALID– does not occur, and the RAS pulse is reset as soon as PRAS– deasserts. The RAS pulse, in this case, is an inverted copy of PRAS–.

Note that, VALID+ is gated with the BPON+ signal at U1205. This is necessary during standby, when GVLD– is held high by BPON+ being low. This ensures that GVLD– enables the RAS reset circuit while the array card is in battery backup mode. This is necessary because VALID–, received at U1308, is not held in a definite state during standby operation.

Memory Protection

There are certain memory cycles initiated by the processor that do not access memory. These include accesses to Boot ROM and Boot RAM. There is also the case where the processor attempts to access a protected memory location. In all three cases, access to main memory is prohibited. This is accomplished by inhibiting CAS from appearing at the DRAMs.

The above three cases are detected by the memory controller. When they occur, the memory controller disables main memory (simultaneously, on all array cards) by not asserting CASEN– on the backplane. The absence of this signal prevents the CAS strobe from appearing at the DRAMs, causing the memory cycle to complete as a "RAS-only" cycle. The effect is that no data is read or written to memory.

CASEN– is received by the array card at U601(11A). It is inverted and then gated with BREF+ at U1001(17A). The combination of these two signals forms CEN+, which is the combined CAS enable signal to the DRAMs.

For all protected memory accesses, CASEN+ is inhibited (low), which forces CEN+ low. This prevents the assertion of CAS at the DRAMs. During refresh cycles, the memory controller protects memory by inhibiting CASEN+ and performs a "RAS-only" refresh cycle. Due to the use of 1-Mbit DRAMs, which have the "CAS-before-RAS" refresh feature, CAS must be sent to the DRAMs during refresh. This is the reason for gating BREF+ with CASEN+; BREF+ asserts CEN+ during refresh cycles and allows CAS to be asserted at the DRAMs.

Therefore, for all cases that the memory controller does not assert CASEN, memory is protected.

Parity LED

As data is accessed from an array card, the memory controller performs a parity check on each 16-bit word. When an error occurs in one bit (or any odd multiple number of bits), PE– is asserted on the backplane by the memory controller and, if interrupts are enabled, causes a parity error interrupt.

When a parity error occurs, circuitry on the array card indicates if this card is the one that caused the error. This circuit monitors PE– on the backplane and BDSEL– on the array card. If the parity error occurred when this card was selected, then the error occurred on this card and the parity LED is extinguished.

The green parity LED is located at the frontplane end of the card. It is designated CR1. This LED is lit for normal operation. The LED is driven by the flip-flop at U1605(25D). When this flip-flop is cleared, the LED is lit. The flip-flop is cleared by a CLC 0 instruction or by power cycling the system. This forces PON+ to go low and then high.

The flip-flop is set (LED unlit) when PE– and BDSEL– are both asserted. The flip-flop remains off until it is cleared, regardless if additional memory cycles are made with no parity errors. An unlit parity LED means that a parity error occurred on an access from this array card at some time in the past. It does not necessarily mean on the most recent access.

Frontplane Handshake Signals

The open-collector driver at U901(27B) is used to drive the handshake signals to the memory controller when this card is being accessed. ACK– is an acknowledgement to the memory controller that the memory address presently on the frontplane is accessing a memory card. (The absence of this signal notifies the memory controller when it is attempting to access non-existent memory). This signal is driven to the memory controller whenever BDSEL– is asserted at U901.

ACK– is also unconditionally asserted whenever a refresh cycle takes place. Normally, if the CPU attempts to access an array card while a refresh cycle is in progress, ACK– is not asserted until the refresh cycle completes. The A400, however, expects an immediate response on the ACK– line and cannot tolerate a delay. If ACK– does not immediately respond to the access request, the A400 memory controller assumes there is no memory present and drives all ones onto the backplane. For this reason, ACK– is driven during every refresh cycle to prevent the A400 from assuming there is no memory.

The unconditional assertion of ACK– is done by using another NAND gate in U901. BREF+ is applied to U901. The output at pin 8 is tied to ACK– at pin 6 in a wired-OR configuration.

The parity bit is also sent from the array card to the memory controller over the frontplane. It is stored along with each data word as the 17th bit and is sent back to the memory controller via the parity check signal, PCK–. This signal is active whenever BDSEL+ is present at U901.

Undershoot Suppression Resistors

The write line (BW–), each DRAM address line (MA+[0:9]), the 11th address lines (ADR11RW+[0:3]) and each individual RAS and CAS strobe line (RAS0– through RAS3–, CAS0– through CAS3–) all have series resistors inserted between the driver outputs and the DRAM inputs. These resistors serve as series terminating resistors for each signal line.

Their purpose is to suppress transmission line effects due to reflections on the bus lines connecting these signals. Due to the incorrectly terminated transmission lines formed by the bus routing, signal reflections occur which cause voltage undershoot to appear at the DRAM inputs. This undershoot can be in excess of the minimum undershoot specification for the DRAM, which is generally about –0.5 volt. The series resistors are chosen to critically damp the falling edge of the signals so that no undershoot occurs.

Refresh Operation

Dynamic RAMs require periodic refreshing to retain their data. This is accomplished by performing CAS-before-RAS refresh cycles simultaneously to all rows on the array card. These cycles are scheduled by the memory controller every 15.6 μsec.

A refresh cycle is done by altering the normal RAS-CAS strobe sequence to the DRAMs. Instead of the RAS-before-CAS sequence of normal memory accesses, the RAS signal is delayed until after CAS has occurred. The DRAMs interpret this strobe sequence as a refresh by enabling a row of memory cells within each DRAM (this does the actual refresh for those memory cells), and by disabling any data output from the DRAM. The CAS-before-RAS sequence also increments the internal refresh counter in each DRAM to prepare it for the next refresh cycle. The next refresh cycle will be performed at the row of memory cells addressed by the incremented counter. The internal refresh counter in each DRAM eliminates the need to supply an external refresh row address to the DRAMs. The counter cycles through all the rows of the internal DRAM matrix, so that within 8 milliseconds, all 512 rows of internal memory cells of the 1-Mbit DRAMs are refreshed.

A refresh cycle is initiated by the memory controller asserting REF+. This signal puts the array card into refresh mode. REF+ is inverted and buffered at U601(11A) and is routed on the array as BREF–. It is inverted again to become BREF+ where needed.

BREF+ is gated with the refresh RAS signal at U702 to become the gated refresh signal, GREF+, at U702(25C). GREF+ is used as a more tightly controlled refresh signal. It is asserted during a refresh cycle only when the RAS pulse is present. As a result, GREF+ is contained within BREF+.

A refresh cycle can be viewed as occurring in two steps. First, BREF+ is asserted to set up the necessary conditions for the impending refresh cycle. Second, GREF+ enables the actual refresh. The sequence of events occurs as described in the following paragraphs.

First, the RAS and CAS drivers are disabled when BREF+ is asserted. This is necessary to prevent any trailing RAS pulses from a memory cycle immediately preceeding the refresh cycle from causing a premature RAS pulse to the DRAMs. (This trailing pulse would be present at U1405 on the delay line). BREF+ appears at U401(14C) and U501(14D). This causes LOSELECT+ and HISELECT+ to go low, disabling the RAS drivers.

Also, BREF+ disables the CAS drivers to prevent the assertion of a premature CAS pulse. BREF– is routed to U1205(15C) where it prevents the assertion of BDSEL–. This causes the multiplexer at U502(17B) to disable all CAS rows because the board is effectively not selected.

Next, GREF+ is asserted when the refresh RAS pulse occurs from the RAS generator at U1605(24C). This signal enables all the RAS and CAS drivers to drive the CAS-before-RAS strobe sequence. GREF+ is routed to U401 and U501 where it forces LOSELECT+ and HISELECT+ both high, enabling the RAS drivers. GREF+ is also routed to the CAS row multiplexer at U502 which drives all the CAS enable lines high, enabling the CAS drivers.

Everything is now ready for the CAS-before-RAS refresh to occur. Because RAS occurs first in a normal memory access sequence, the RAS pulse during refresh must be delayed until after the CAS pulse has occurred at the DRAMs. This is done by inhibiting the RAS pulse until a delayed RAS pulse appears at the last tap of the delay line at U1405. The early RAS pulse is inhibited by GREF+ appearing at U902(17B). The output of this gate does not go high until the delayed RAS appears. Because the early RAS pulse is already present at the RAS drivers, the late RAS pulse initiates the refresh RAS pulse to the DRAMs.

Finally, GREF+ is routed to the K input of the RAS generator flip-flop at U1605. This causes the RAS pulse to reset during A400/A600+ system refresh cycles.

Backplane Data Drivers and Receivers

Data is received by the array card from the backplane by two ALS573 octal latches, U408(27C) and U608(27D). These devices are used to latch data from the backplane during memory write cycles. Data must be latched after it is received because data is only driven on the backplane from either a processor or I/O card during the beginning of a memory write. When the actual writing of data into the DRAMs takes place, the data has already disappeared from the backplane. The outputs of the latches run directly to the DRAM data inputs. The latch outputs are tri-state capable but this function is never used because the latch outputs only go to the DRAM inputs, and no other data sources are present on this bus. As a result, the output enable pins of the latches are grounded, permanently enabling the outputs of the devices. Latching of input data is done by BLATCH– which is generated by the memory controller.

Data is driven onto the backplane by the array card during memory read cycles. Data that is output from the DRAMs is buffered by two F241 octal drivers, U508(28C) and U708(28D), which then drive the backplane data bus. The drivers are enabled only when DRIVE– is sent from the memory controller and the array card is selected for access. Each octal driver pack consists of two sections of four channels. The two sections have complementary enable signals. The first section is enabled by a low signal on pin 1 and the second section is enabled by a high signal on pin 19. As a result, both BDRIVE– and BDRIVE+ are needed to enable each backplane driver.

Addressing PLA

The addressing PLA at U1301(12C) is used to set the card capacity of the array. It also specifies what type of DRAMs are installed on the array card. (1-Mbit versus 4-Mbit DRAMs). The PLA also generates MTOP– which is used by the module self-configuration circuits to determine the end of memory.

This PLA is factory programmed for the memory capacity of the particular array card onto which it is installed.

Stand-By Operation

Standby operation refers to the state that the memory system takes when BPON+ is low. When in this state, the only operation that the memory controller performs is refreshing. No accesses are done to the memory system.

The normal +5 volts is removed, and only +5M is maintained by battery power. This voltage is routed only to the RAMs and to those components necessary for the refresh function. All components that receive +5M are designated with an asterisk (*) on the schematic. All other components do not receive any power during standby operation.

Parts Locations

The parts locations for the 12103C and 12103D memory arrays are shown in Figure 6-3 and Figure 6-4, respectively. The parts locations for the 12103K/L/M memory arrays are shown in Figure 6-5.

Parts List

The parts for the 12103C, 12103D, 12103K, 12103L, and 12103M memory arrays are listed in Tables 6-2 through 6-6. Refer to Table 6-7 for the names and addresses of the manufacturers of the parts in the Manufacturer's Code List.

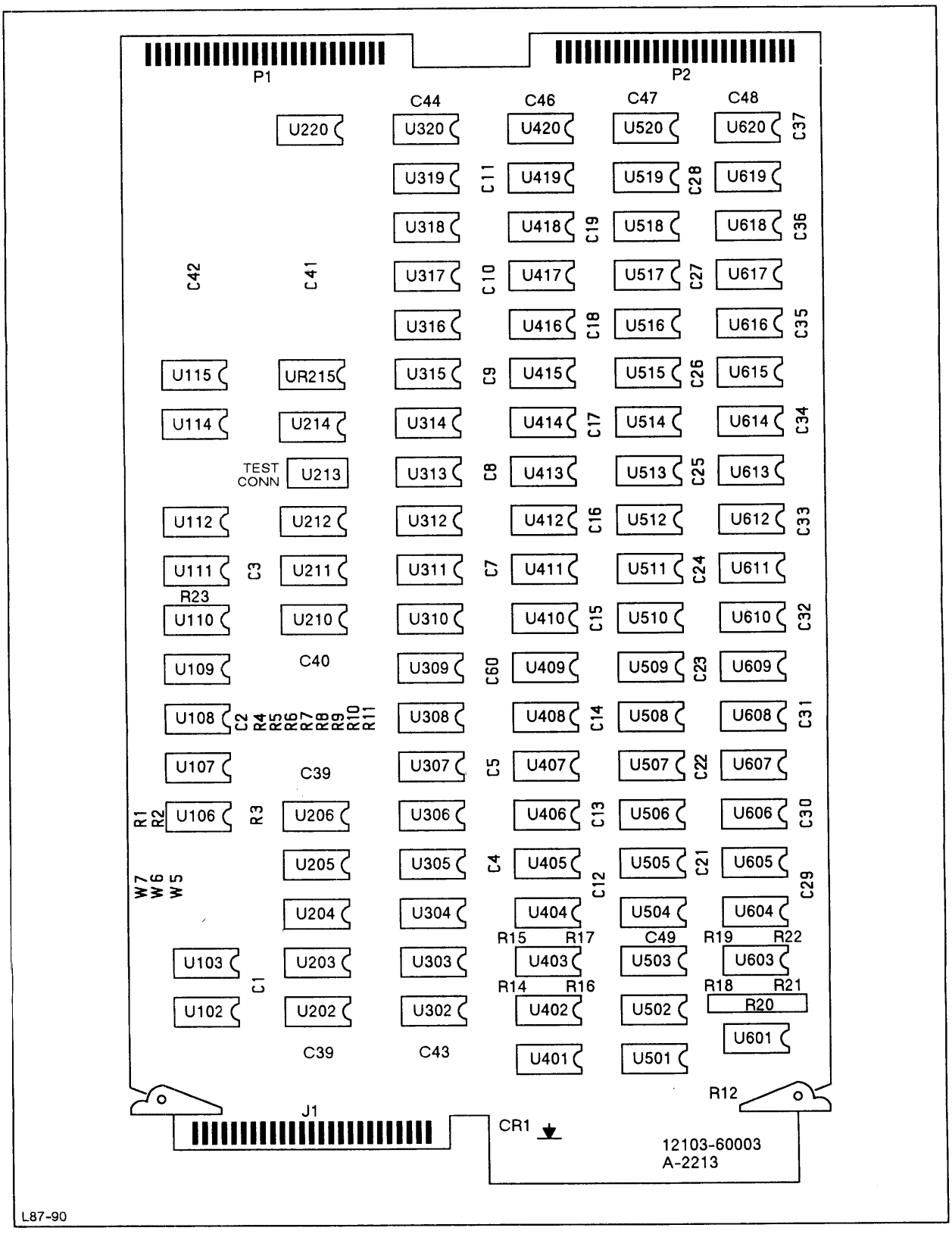


Figure 6-3. 12103C Parts Locations

Table 6-2. 12103C Parts List (sheet 1 of 3)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
	12103-60016	9	1	PCA-ARRAY CARD	28480	12103-60016
C1	0160-4842	6	37	CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C2	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C3	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C4	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C5	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C6	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C7	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C8	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C9	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C10	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C11	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C12	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C13	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C14	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C15	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C16	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C17	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C18	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C19	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C20	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C21	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C22	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C23	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C24	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C25	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C26	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C27	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C28	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C29	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C30	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C31	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C32	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C33	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C34	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C35	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C36	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C37	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C38	0180-0374	3	11	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C39	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C40	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C41	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C42	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C43	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C44	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C45	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C46	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C47	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C48	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C49	0160-4818	6	1	CAPACITOR-FXD 47PF +-10% 100VDC CER	28480	0160-4818
CR1	1990-0598	1	1	LED-LAMP LUM-INT=800UCD IF=60MA-MAX	28480	5082-4190
R1	0757-0442	9	2	RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1002-F
R2	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1002-F
R3	0698-3441	8	1	RESISTOR 215 1% .125W F TC=0+-100	24546	CT4-1/8-T0-215R-F
R4	0757-0346	2	8	RESISTOR 10 1% .125W F TC=0+-100	28480	0757-0346
R5	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	28480	0757-0346
R6	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	28480	0757-0346
R7	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	28480	0757-0346
R8	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	28480	0757-0346
R9	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	28480	0757-0346
R10	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	28480	0757-0346

Table 6-2. 12103C Parts List (sheet 2 of 3)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R11	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	28480	0757-0346
R13	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	CT4-1/8-T0-422R-F
R14	0757-0294	9	4	RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R15	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R16	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R17	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R18	0698-3430	5	4	RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R19	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R20	1810-0277	3	1	NETWORK-RES 10-SIP 2.2K OHM X 9	91637	CSC10A01-222G/MSP10A01-
R21	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R22	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R23	0698-4037	0	1	RESISTOR 46.4 1% .125W F TC=0+-100	28480	0698-4037
U102	1820-1441	6	2	IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
U103	1820-0694	9	2	IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U106	1820-1989	7	1	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U107	1820-1917	1	1	IC DRVR TTL LS LINE OCTL	01295	SN74LS240N
U108	1820-1633	8	2	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U109	1820-1676	9	1	IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U110	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U111	1820-2102	8	2	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U112	1820-2699	8	2	IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U202	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
U203	1820-0694	9		IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U204	1820-1323	3	1	IC GATE TTL S NAND 8-INP	01295	SN74S30N
U205	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
U206	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U210	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U211	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U212	1820-2699	8		IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U214	1820-2786	4	1	IC LCH TTL F INV TRANSPARENT COM CLEAR	07263	74F533PC
U215	1810-0235	3	1	NETWORK-RES 16-DIP 2.2K OHM X 15	73138	898-1-R2.2K
U220	1820-1414	3	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS12N
U302	1820-1072	9	1	IC DCDR TTL S 2-TO-4-LINE DUAL 2-INP	01295	SN74S139N
U303	1820-1015	0	2	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U304	1818-3059	1	68	IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U305	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U306	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U307	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U308	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U309	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U310	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U311	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U312	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U313	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U314	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U315	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U316	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U317	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U318	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U319	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U320	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U401	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U402	1820-1015	0		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U403	1820-1450	7	1	IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U404	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U405	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U406	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U407	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U408	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U409	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U410	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U411	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U412	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U413	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U414	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U415	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U416	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059

Table 6-2. 12103C Parts List (sheet 3 of 3)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U417	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U418	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U419	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U420	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U501	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U502	1820-0691	6	1	IC GATE TTL S AND-OR-INV	01295	SN74S64N
U503	1820-0629	0	1	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U504	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U505	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U506	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U507	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U508	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U509	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U510	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U511	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U512	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U513	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U514	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U515	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U516	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U517	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U518	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U519	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U520	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U601	1813-0199	4	1	DELAY LINE ACTIVE DELAY LINE; TTL	07910	HY-5003
U603	1820-4615	2	1	IC BFR TTL S NAND QUAD 2-INP	18324	74S37N
U604	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U605	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U606	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U607	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U608	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U609	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U610	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U611	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U612	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U613	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U614	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U615	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U616	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U617	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U618	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U619	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U620	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
W5	0811-3587	5	3	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W6	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W7	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
	0403-0289	3	2	EXTR-PC BD RED POLYC .063-BD-THKNS	28480	0403-0289
	1200-0997	1	1	SOCKET-8 PIN DIP	28480	1200-0997
	4114-1039	4	1	PLASTIC FLM POLYI AMB ADH-1-S	85480	XB-652
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
	7121-0871	8	1	LABEL-PR	28480	7121-0871
	7121-2061	2	1	LABEL-DATE CODE	28480	7121-2061
	7121-2551	5	1	LABEL-INFO	28480	7121-2551
	5180-0176	8	1	PCB-ARRAY CARD	28480	5180-0176

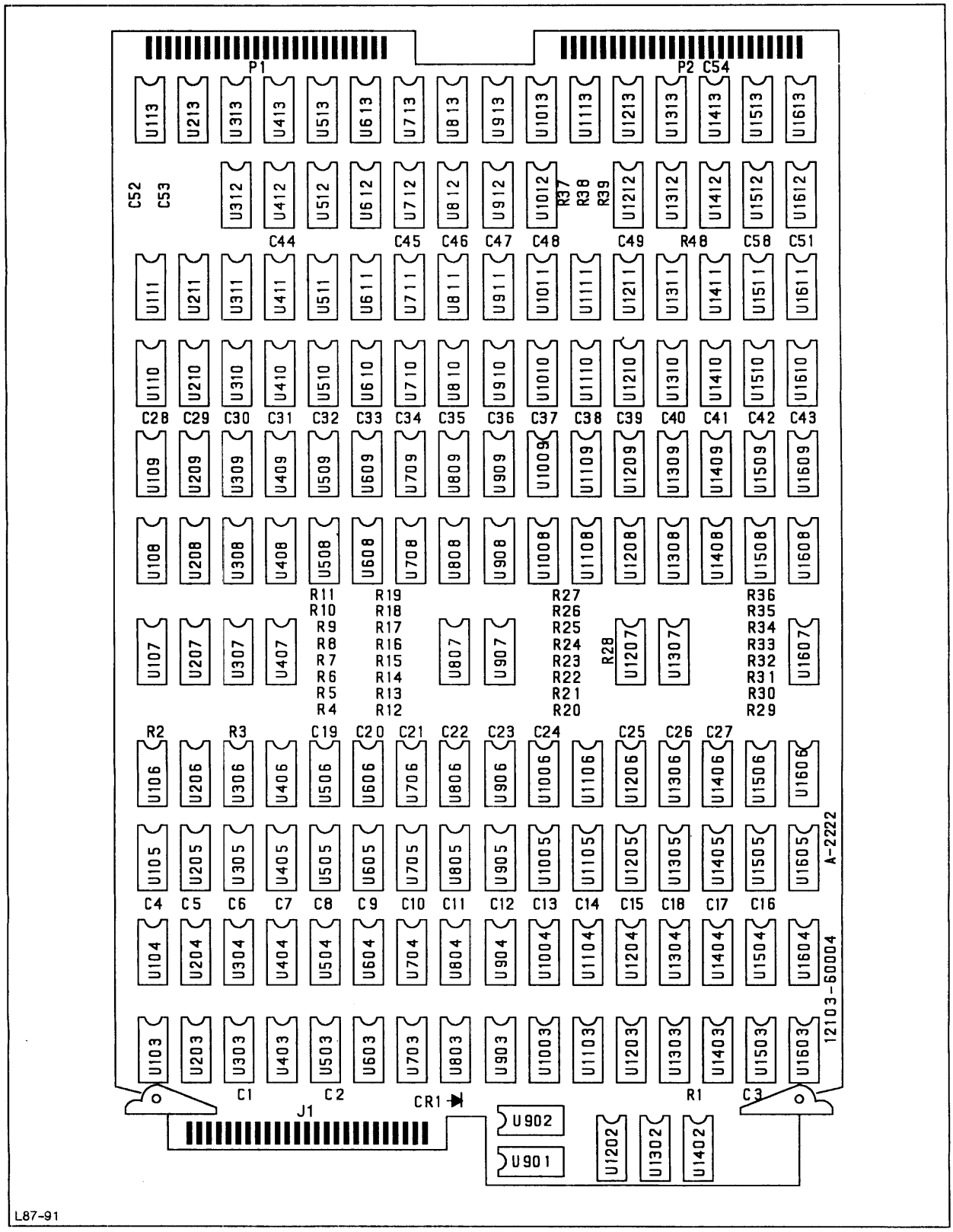


Figure 6-4. 12103D Parts Locations

Table 6-3. 12103D Parts List (sheet 1 of 4)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12103-60004	5	1	PCA-1M BYTE ARRAY	28480	12103-60004
C1	0180-0229	7	5	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C2	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C3	0160-5148	7	48	CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C4	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C5	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C6	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C7	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C8	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C9	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C10	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C11	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C12	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C13	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C14	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C15	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C16	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C17	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C18	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C19	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C20	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C21	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C22	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C23	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C24	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C25	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C26	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C27	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C28	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C29	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C30	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C31	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C32	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C33	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C34	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C35	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C36	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C37	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C38	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C39	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C40	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C41	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C42	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C43	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C44	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C45	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C46	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C47	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C48	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C49	0160-4818	6	1	CAPACITOR-FXD 47PF +-10% 100VDC CER	28480	0160-4818
C50	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C51	0160-5148	7		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-5148
C52	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C53	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C54	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
CR1	1990-0485	5	1	LED-LAMP LUM-INT=2MCD IF=30MA-MAX BVR=5V	28480	HLMP-1503
R1	0683-2215	1	1	RESISTOR 220 5% .25W CF TC=0-400	01121	CB2215
R2	0698-0084	9	4	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-2151-F
R3	0757-0294	9	17	RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R4	0698-3432	7	16	RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R5	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F

Table 6-3. 12103D Parts List (sheet 2 of 4)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R6	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R7	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R8	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R9	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R10	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R11	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R12	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R13	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R14	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R15	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R16	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R17	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R18	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R19	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R20	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R21	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R22	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R23	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R24	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R25	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R26	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R27	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R28	1810-0277	3	1	NETWORK-RES 10-SIP 2.2K OHM X 9	91637	CSC10A01-222G/MSP10A01-
R29	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R30	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R31	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R32	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R33	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R34	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R35	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R36	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	5033R-1/8-T0-17R8-F
R37	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-2151-F
R38	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-2151-F
R39	0698-4037	0	1	RESISTOR 46.4 1% .125W F TC=0+-100	28480	0698-4037
R40	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-2151-F
U103	1818-3059	1	112	IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U104	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U105	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U106	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U107	1820-0690	5	1	IC BFR TTL S NAND DUAL 4-INP	01295	SN74S40N
U108	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U109	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U110	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U111	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U113	1820-1441	6	1	IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
U203	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U204	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U205	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U206	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U207	1820-1072	9	1	IC DCDR TTL S 2-TO-4-LINE DUAL 2-INP	01295	SN74S139N
U208	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U209	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U210	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U211	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U213	1820-1917	1	2	IC DRVR TTL LS LINE OCTL	01295	SN74LS240N
U303	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U304	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U305	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U306	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U307	1820-1015	0	3	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U308	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U309	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U310	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U311	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U312	1820-1989	7	1	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC

Table 6-3. 12103D Parts List (sheet 3 of 4)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U313	1820-1917	1		IC DRVR TTL LS LINE OCTL	01295	SN74LS240N
U407	1820-1015	0		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U412	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U413	1820-1676	9	2	IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U512	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U513	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U612	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U613	1820-2699	8	2	IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U703	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U704	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U705	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U706	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U708	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U709	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U710	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U711	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U712	1820-0683	6	2	IC INV TTL S HEX 1-INP	01295	SN74S04N
U713	1820-2699	8		IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U803	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U804	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U805	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U806	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U807	1820-1450	7	2	IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U808	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U809	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U810	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U811	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U812	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U813	1820-2102	8	2	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U901	1820-1633	8	3	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U902	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U903	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U904	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U905	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U906	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U907	1820-1450	7		IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U908	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U909	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U910	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U911	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U912	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U913	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U1003	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1004	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1005	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1006	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1008	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1009	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1010	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1011	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1012	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U1013	1820-2786	4	1	IC LCH TTL F INV TRANSPARENT COM CLEAR	07263	74F533PC
U1103	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1104	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1105	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1106	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1108	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1109	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1110	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1111	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1113	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U1202	1820-0694	9	2	IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U1203	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1204	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1205	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059

Table 6-3. 12103D Parts List (sheet 4 of 4)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
U1206	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1207	1820-4615	2	2	IC BFR TTL S NAND QUAD 2-INP	18324	74S37N
U1208	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1209	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1210	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1211	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1212	1820-0629	0	1	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U1213	1820-1015	0		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U1302	1820-0694	9		IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U1303	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1304	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1305	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1306	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1307	1820-4615	2		IC BFR TTL S NAND QUAD 2-INP	18324	74S37N
U1308	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1309	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1310	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1311	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1312	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1313	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1402	1820-1323	3	1	IC GATE TTL S NAND 8-INP	01295	SN74S30N
U1403	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1404	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1405	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1406	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1408	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1409	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1410	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1411	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1412	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1413	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1503	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1504	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1505	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1506	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1508	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1509	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1510	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1511	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1512	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1513	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1603	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1604	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1605	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1606	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1607	1813-0292	8	1	DELAY LINE ACTIVE DELAY LINE; TTL	28480	1813-0292
U1608	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1609	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1610	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1611	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1612	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
U1613	1818-3059	1		IC NMOS 65536(64K) DYN RAM 150-NS 3-S	28480	1818-3059
	0403-0289	3	2	EXTR-PC BD RED POLYC .063-BD-THKNS	28480	0403-0289
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
	4114-1039	4	1	PLASTIC FLM POLYI AMB ADH-1-S	85480	XB-652
	7120-6829	6	1	LABEL-FRANCE	28480	7120-6829
	7120-6830	9	1	LABEL-USA	28480	7120-6830
	7120-8074	7	1	LABEL-JAPAN	28480	7120-8074
	7121-0871	8	1	LABEL-PR	28480	7121-0871
	7121-2061	2	1	LABEL DATE CODE	28480	7121-2061
	7121-2551	5	1	LABEL-INFO	28480	7121-2551
	9222-0763	3	1	BAG-ASTAT	28480	9222-0763
	12103-80004	7	1	PCB-1M BYTE ARRAY	28480	12103-80004

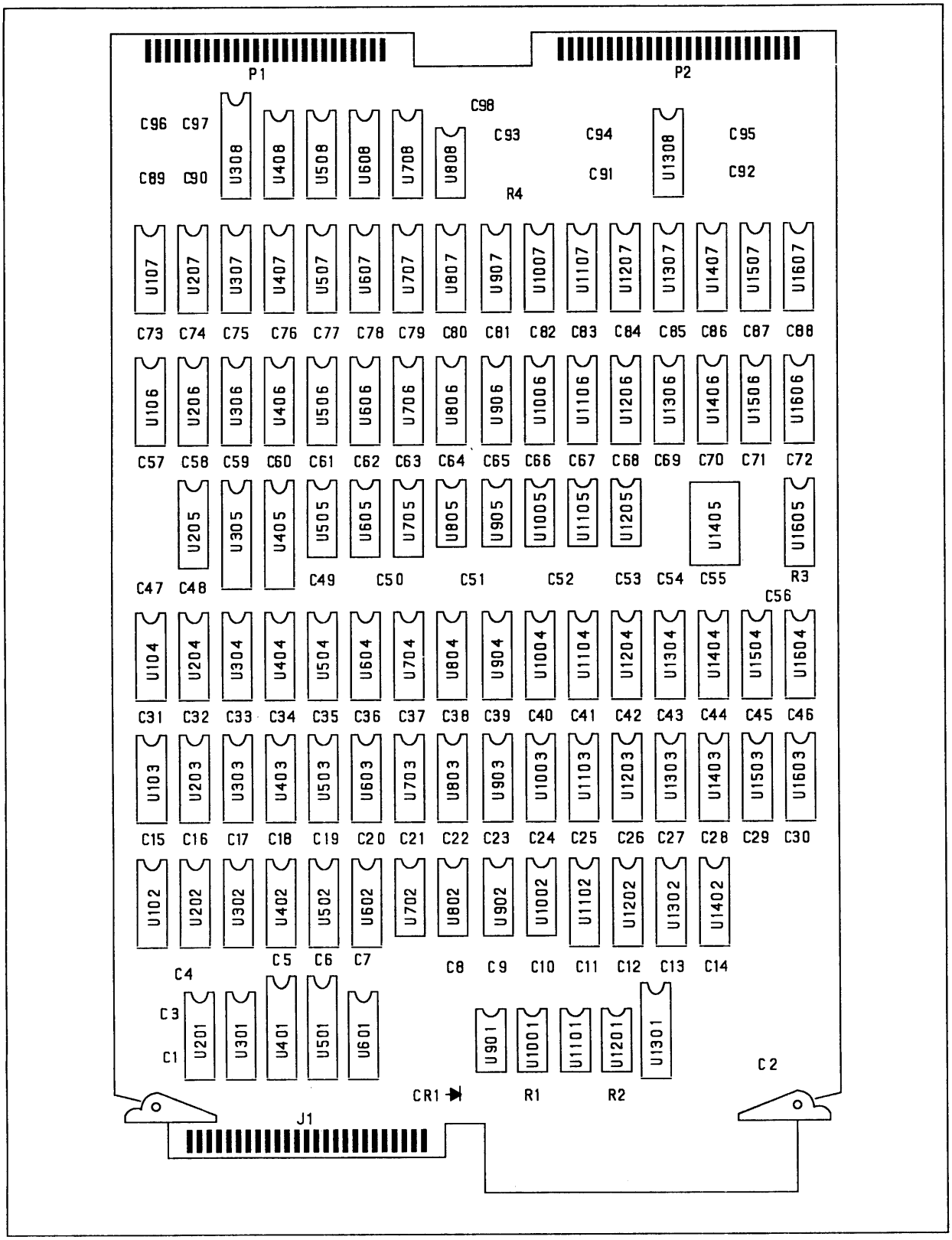


Figure 6-5. 12103K/L/M Parts Locations

Table 6-4. 12103K Replaceable Parts (sheet 1 of 2)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12103-66001	4	1	PCA-2MB MEMORY	28480	12103-66001
C1	0160-6463	1	37	CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C2	0180-0229	7	9	CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C3	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C4	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C5	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C6	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C7	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C8	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C9	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C10	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C11	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C47	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C48	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C49	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C50	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C51	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C52	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C53	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C54	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C55	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C56	0160-4805	1	1	CAP-FXD 47PF -5 +5C0G	12474	CAC02C0G470J100A
C73	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C74	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C75	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C76	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C77	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C78	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C79	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C80	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C81	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C82	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C83	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C84	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C85	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C86	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C87	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C88	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C89	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C90	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C91	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C92	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C93	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C94	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C95	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C96	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C97	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C98	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
CR1	1990-0485	5	1	LED-LAMP LUM-INT=2MCD IF=30MA-MAX BVR=5V	28480	HLMP-1503
R1	0757-0280	3	1	RESISTOR 1K +-1% .125W TF TC=0+-100	12498	CT4-1/8-T0-1001-F
R2	0698-3447	4	1	RESISTOR 422 +-1% .125W TF TC=0+-100	12498	CT4-1/8-T0-422R-F
R3	0698-4037	0	1	RESISTOR 46.4 +-1% .125W TF TC=0+-100	D8439	MK2
R4	0698-3431	6	1	RESISTOR 23.7 +-1% .125W TF TC=0+-100	D8439	MK2
U102	1820-3738	8	1	IC MUXR/DATA-SEL TTL AS 2-TO-1-LINE QUAD	01295	SN74AS157N
U107	1818-4032	2	17	DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U201	1820-3543	3	3	IC DRVR TTL AS BUS OCTL	01295	SN74AS240N
U202	1820-3133	7	2	IC ADDR TTL F BIN FULL ADDR 4-BIT	07263	74F283PC
U205	1820-3745	7	1	IC DRVR TTL AS LINE QUAD	01295	SN74AS241N
U207	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U301	1820-3543	3		IC DRVR TTL AS BUS OCTL	01295	SN74AS240N
U302	1820-3133	7		IC ADDR TTL F BIN FULL ADDR 4-BIT	07263	74F283PC
U305	1820-3440	9	2	IC DRVR TTL S BUS 10-BIT	34335	AM29827DC
U307	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10

Table 6-4. 12103K Replaceable Parts (sheet 2 of 2)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
U308	1820-4535	5	1	IC LCH TTL ALS TRANSPARENT 10-BIT	01295	SN74ALS841NT
U401	1820-2899	0	2	IC COMPTR TTL AS MAGTD 8-BIT	01295	SN74AS885NT
U402	1820-3220	3	1	IC DCDR TTL F BIN 2-TO-4-LINE DUAL	07263	74F139PC
U405	1820-3440	9		IC DRVR TTL S BUS 10-BIT	34335	AM29827DC
U407	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U408	1820-2724	0	2	IC LCH TTL ALS TRANSPARENT OCTL	01295	SN74ALS573BN
U501	1820-2899	0		IC COMPTR TTL AS MAGTD 8-BIT	01295	SN74AS885NT
U502	1820-3739	9	1	IC MUXR/DATA-SEL TTL AS 2-TO-1-LINE QUAD	01295	SN74AS158N
U505	1810-0557	2	2	NETWORK-RES 16-DIP 22.0 OHM X 8	91637	MDP1603-220G
U507	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U508	1820-2699	8	2	IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U601	1820-2951	5	1	IC DRVR TTL ALS BUS OCTL	01295	SN74ALS240AN
U602	1810-0424	2	1	NETWORK-RES 16-DIP 4.7K OHM X 15	11236	761-1-R4.7K
U605	1810-0557	2		NETWORK-RES 16-DIP 22.0 OHM X 8	91637	MDP1603-220G
U607	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U608	1820-2724	0		IC LCH TTL ALS TRANSPARENT OCTL	01295	SN74ALS573BN
U702	1820-2635	2	1	IC GATE TTL ALS AND QUAD 2-INP	01295	SN74ALS08N
U705	1810-0533	4	1	NETWORK-RES 16-DIP 33.0 OHM X 8	91637	MDP1603-330G
U707	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U708	1820-2699	8		IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U802	1820-2634	1	4	IC INV TTL ALS HEX	01295	SN74ALS04BN
U805	1820-5212	7	4	IC BFR TTL F NAND DUAL 4-INP	18324	74F40N
U807	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U808	1820-2634	1		IC INV TTL ALS HEX	01295	SN74ALS04BN
U901	1820-3349	7	1	IC BFR TTL ALS NAND QUAD 2-INP	01295	SN74ALS38AN
U902	1820-2656	7	1	IC GATE TTL ALS NAND QUAD 2-INP	01295	SN74ALS00AN
U905	1820-5212	7		IC BFR TTL F NAND DUAL 4-INP	18324	74F40N
U907	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1001	1820-2692	1	1	IC GATE TTL F EXCL-OR QUAD 2-INP	07263	74F86PC
U1002	1820-2676	1	1	IC GATE TTL F AND-OR-INV	07263	74F64PC
U1005	1820-5212	7		IC BFR TTL F NAND DUAL 4-INP	18324	74F40N
U1007	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1101	1820-2634	1		IC INV TTL ALS HEX	01295	SN74ALS04BN
U1102	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1105	1820-5212	7		IC BFR TTL F NAND DUAL 4-INP	18324	74F40N
U1107	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1201	1820-2634	1		IC INV TTL ALS HEX	01295	SN74ALS04BN
U1205	1820-3731	1	1	IC GATE TTL AS NAND TPL 3-INP	01295	SN74AS10N
U1207	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1301	12103-80019	4	1	IC-PGM	28480	12103-80019
U1307	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1308	1820-3543	3		IC DRVR TTL AS BUS OCTL	01295	SN74AS240N
U1405	1810-1092	2	1	DELAY LINE ACTIVE DEVICE W/DUAL IN-LINE	07910	HY50-073
U1407	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1507	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1605	1820-2694	3	1	IC FF TTL F J-K NEG-EDGE-TRIG	07263	74F112PC
U1607	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
	0403-0289	3	2	EXTR-PC BD RED POLYC 1.6-MM-BD-THKNS	28480	0403-0289
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	73957	GP24-063 X 250-17
	4114-1039	4	1	PLASTIC FLM POLYI AMB ADH-1-S	85480	XB-652
	5180-4275	6	1	PCB-MEMORY	28480	5180-4275
	7120-6829	6	1	LABEL-FRANCE	28480	7120-6829
	7120-6830	9	1	LBL-WARR DATE CD	28480	7120-6830
	7120-8074	7	1	LABEL-JAPAN	28480	7120-8074
	7121-0850	3	1	LBL-ANTISTAT BAG	76381	7101
	7121-0871	8	1	LBL-PR/WARRANTY	28480	7121-0871
	7121-2061	2	1	LABEL-DATE CODE	28480	7121-2061
	7121-2551	5	1	LABEL-INFO	28480	7121-2551
	7121-3054	5	1	LABEL BLANK	28480	7121-3054
	9211-5376	1	1	PACK-CONT	28480	9211-5376
	9222-0666	5	1	BAG-ANTISTATIC	76381	2100

Table 6-5. 12103L Replaceable Parts (sheet 1 of 3)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12103-66002	5	1	PCA-4MB MEMORY	28480	12103-66002
C1	0160-6463	1	54	CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C2	0180-0229	7	9	CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C3	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C4	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C5	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C6	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C7	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C8	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C9	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C10	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C11	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C12	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C47	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C48	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C49	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C50	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C51	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C52	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C53	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C54	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C55	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C56	0160-4805	1	1	CAP-FXD 47PF -5 +5C0G	12474	CAC02C0G470J100A
C57	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C58	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C59	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C60	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C61	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C62	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C63	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C64	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C65	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C66	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C67	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C68	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C69	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C70	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C71	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C72	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C73	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C74	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C75	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C76	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C77	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C78	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C79	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C80	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C81	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C82	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C83	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C84	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C85	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C86	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C87	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C88	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C89	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C90	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C91	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C92	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C93	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C94	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2

Table 6-5. 12103L Replaceable Parts (sheet 2 of 3)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
C95	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C96	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C97	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C98	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
CR1	1990-0485	5	1	LED-LAMP LUM-INT=2MCD IF=30MA-MAX BVR=5V	28480	HLMP-1503
R1	0757-0280	3	1	RESISTOR 1K +-1% .125W TF TC=0+-100	12498	CT4-1/8-T0-1001-F
R2	0698-3447	4	1	RESISTOR 422 +-1% .125W TF TC=0+-100	12498	CT4-1/8-T0-422R-F
R3	0698-4037	0	1	RESISTOR 46.4 +-1% .125W TF TC=0+-100	D8439	MK2
R4	0698-3431	6	1	RESISTOR 23.7 +-1% .125W TF TC=0+-100	D8439	MK2
U102	1820-3738	8	1	IC MUXR/DATA-SEL TTL AS 2-TO-1-LINE QUAD	01295	SN74AS157N
U106	1818-4032	2	34	DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U107	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U201	1820-3543	3	3	IC DRVR TTL AS BUS OCTL	01295	SN74AS240N
U202	1820-3133	7	2	IC ADDR TTL F BIN FULL ADDR 4-BIT	07263	74F283PC
U205	1820-3745	7	1	IC DRVR TTL AS LINE QUAD	01295	SN74AS241N
U206	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U207	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U301	1820-3543	3		IC DRVR TTL AS BUS OCTL	01295	SN74AS240N
U302	1820-3133	7		IC ADDR TTL F BIN FULL ADDR 4-BIT	07263	74F283PC
U305	1820-3440	9	2	IC DRVR TTL S BUS 10-BIT	34335	AM29827DC
U306	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U307	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U308	1820-4535	5	1	IC LCH TTL ALS TRANSPARENT 10-BIT	01295	SN74ALS841NT
U401	1820-2899	0	2	IC COMPTR TTL AS MAGTD 8-BIT	01295	SN74AS885NT
U402	1820-3220	3	1	IC DCDR TTL F BIN 2-TO-4-LINE DUAL	07263	74F139PC
U405	1820-3440	9		IC DRVR TTL S BUS 10-BIT	34335	AM29827DC
U406	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U407	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U408	1820-2724	0	2	IC LCH TTL ALS TRANSPARENT OCTL	01295	SN74ALS573BN
U501	1820-2899	0		IC COMPTR TTL AS MAGTD 8-BIT	01295	SN74AS885NT
U502	1820-3739	9	1	IC MUXR/DATA-SEL TTL AS 2-TO-1-LINE QUAD	01295	SN74AS158N
U505	1810-0557	2	2	NETWORK-RES 16-DIP 22.0 OHM X 8	91637	MDP1603-220G
U506	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U507	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U508	1820-2699	8	2	IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U601	1820-2951	5	1	IC DRVR TTL ALS BUS OCTL	01295	SN74ALS240AN
U602	1810-0424	2	1	NETWORK-RES 16-DIP 4.7K OHM X 15	11236	761-1-R4.7K
U605	1810-0557	2		NETWORK-RES 16-DIP 22.0 OHM X 8	91637	MDP1603-220G
U606	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U607	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U608	1820-2724	0		IC LCH TTL ALS TRANSPARENT OCTL	01295	SN74ALS573BN
U702	1820-2635	2	1	IC GATE TTL ALS AND QUAD 2-INP	01295	SN74ALS08N
U705	1810-0533	4	1	NETWORK-RES 16-DIP 33.0 OHM X 8	91637	MDP1603-330G
U706	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U707	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U708	1820-2699	8		IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U802	1820-2634	1	4	IC INV TTL ALS HEX	01295	SN74ALS04BN
U805	1820-5212	7	4	IC BFR TTL F NAND DUAL 4-INP	18324	74F40N
U806	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U807	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U808	1820-2634	1		IC INV TTL ALS HEX	01295	SN74ALS04BN
U901	1820-3349	7	1	IC BFR TTL ALS NAND QUAD 2-INP	01295	SN74ALS38AN
U902	1820-2656	7	1	IC GATE TTL ALS NAND QUAD 2-INP	01295	SN74ALS00AN
U905	1820-5212	7		IC BFR TTL F NAND DUAL 4-INP	18324	74F40N
U906	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U907	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1001	1820-2692	1	1	IC GATE TTL F EXCL-OR QUAD 2-INP	07263	74F86PC
U1002	1820-2676	1	1	IC GATE TTL F AND-OR-INV	07263	74F64PC
U1005	1820-5212	7		IC BFR TTL F NAND DUAL 4-INP	18324	74F40N
U1006	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1007	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1101	1820-2634	1		IC INV TTL ALS HEX	01295	SN74ALS04BN
U1102	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1105	1820-5212	7		IC BFR TTL F NAND DUAL 4-INP	18324	74F40N

Table 6-5. 12103L Replaceable Parts (sheet 3 of 3)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U1106	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1107	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1201	1820-2634	1		IC INV TTL ALS HEX	01295	SN74ALS04BN
U1202	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1205	1820-3731	1	1	IC GATE TTL AS NAND TPL 3-INP	01295	SN74AS10N
U1206	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1207	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1301	12103-80020	7	1	IC-PGM	28480	12103-80020
U1306	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1307	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1308	1820-3543	3		IC DRVR TTL AS BUS OCTL	01295	SN74AS240N
U1405	1810-1092	2	1	DELAY LINE ACTIVE DEVICE W/DUAL IN-LINE	07910	HY50-073
U1406	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1407	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1506	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1507	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1605	1820-2694	3	1	IC FF TTL F J-K NEG-EDGE-TRIG	07263	74F112PC
U1606	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1607	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
	0403-0289	3	2	EXTR-PC BD RED POLYC 1.6-MM-BD-THKNS	28480	0403-0289
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	73957	GP24-063 X 250-17
	4114-1039	4	1	PLASTIC FLM POLYI AMB ADH-1-S	85480	XB-652
	5180-4275	6	1	PCB-MEMORY	28480	5180-4275
	7120-6829	6	1	LABEL-FRANCE	28480	7120-6829
	7120-6830	9	1	LBL-WARR DATE CD	28480	7120-6830
	7120-8074	7	1	LABEL-JAPAN	28480	7120-8074
	7121-0850	3	1	LBL-ANTISTAT BAG	76381	7101
	7121-0871	8	1	LBL-PR/WARRANTY	28480	7121-0871
	7121-2061	2	1	LABEL-DATE CODE	28480	7121-2061
	7121-2551	5	1	LABEL-INFO	28480	7121-2551
	7121-3054	5	1	LABEL BLANK	28480	7121-3054
	9211-5376	1	1	PACK-CONT	28480	9211-5376
	9222-0666	5	1	BAG-ANTISTATIC	76381	2100

Table 6-6. 12103M Replaceable Parts (sheet 1 of 4)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12103-66003	6	1	PCA-8MB MEMORY	28480	12103-66003
C1	0160-6463	1	88	CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C2	0180-0229	7	9	CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C3	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C4	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C5	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C6	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C7	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C8	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C9	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C10	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C11	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C12	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C13	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C14	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C15	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C16	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C17	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C18	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C19	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C20	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C21	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C22	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C23	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C24	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C25	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C26	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C27	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C28	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C29	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C30	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C31	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C32	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C33	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C34	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C35	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C36	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C37	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C38	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C39	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C40	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C41	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C42	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C43	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C44	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C45	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C46	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C47	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C48	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C49	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C50	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C51	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C52	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C53	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C54	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C55	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C56	0160-4805	1	1	CAP-FXD 47PF -5 +5C0G	12474	CAC02C0G470J100A
C57	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C58	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C59	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C60	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA

Table 6-6. 12103M Replaceable Parts (sheet 2 of 4)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
C61	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C62	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C63	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C64	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C65	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C66	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C67	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C68	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C69	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C70	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C71	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C72	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C73	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C74	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C75	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C76	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C77	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C78	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C79	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C80	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C81	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C82	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C83	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C84	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C85	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C86	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C87	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C88	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C89	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C90	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C91	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C92	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C93	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C94	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C95	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
C96	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C97	0160-6463	1		CAP-FXD 0.33UF -20 +80Z5U	04222	SA115E334ZAA
C98	0180-0229	7		CAP-FXD 33UF -10 +10TA0 OHM	56289	150D336X9010B2
CR1	1990-0485	5	1	LED-LAMP LUM-INT=2MCD IF=30MA-MAX BVR=5V	28480	HLMP-1503
R1	0757-0280	3	1	RESISTOR 1K +-1% .125W TF TC=0+-100	12498	CT4-1/8-T0-1001-F
R2	0698-3447	4	1	RESISTOR 422 +-1% .125W TF TC=0+-100	12498	CT4-1/8-T0-422R-F
R3	0698-4037	0	1	RESISTOR 46.4 +-1% .125W TF TC=0+-100	D8439	MK2
R4	0698-3431	6	1	RESISTOR 23.7 +-1% .125W TF TC=0+-100	D8439	MK2
U102	1820-3738	8	1	IC MUXR/DATA-SEL TTL AS 2-TO-1-LINE QUAD	01295	SN74AS157N
U103	1818-4032	2	68	DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U104	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U106	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U107	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U201	1820-3543	3	3	IC DRVR TTL AS BUS OCTL	01295	SN74AS240N
U202	1820-3133	7	2	IC ADDR TTL F BIN FULL ADDR 4-BIT	07263	74F283PC
U203	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U204	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U205	1820-3745	7	1	IC DRVR TTL AS LINE QUAD	01295	SN74AS241N
U206	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U207	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U301	1820-3543	3		IC DRVR TTL AS BUS OCTL	01295	SN74AS240N
U302	1820-3133	7		IC ADDR TTL F BIN FULL ADDR 4-BIT	07263	74F283PC
U303	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U304	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U305	1820-3440	9	2	IC DRVR TTL S BUS 10-BIT	34335	AM29827DC
U306	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U307	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U308	1820-4535	5	1	IC LCH TTL ALS TRANSPARENT 10-BIT	01295	SN74ALS841NT

Table 6-6. 12103M Replaceable Parts (sheet 3 of 4)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
U401	1820-2899	0	2	IC COMPTR TTL AS MAGTD 8-BIT	01295	SN74AS885NT
U402	1820-3220	3	1	IC DCDR TTL F BIN 2-TO-4-LINE DUAL	07263	74F139PC
U403	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U404	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U405	1820-3440	9		IC DRVR TTL S BUS 10-BIT	34335	AM29827DC
U406	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U407	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U408	1820-2724	0	2	IC LCH TTL ALS TRANSPARENT OCTL	01295	SN74ALS573BN
U501	1820-2899	0		IC COMPTR TTL AS MAGTD 8-BIT	01295	SN74AS885NT
U502	1820-3739	9	1	IC MUXR/DATA-SEL TTL AS 2-TO-1-LINE QUAD	01295	SN74AS158N
U503	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U504	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U505	1810-0557	2	2	NETWORK-RES 16-DIP 22.0 OHM X 8	91637	MDP1603-220G
U506	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U507	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U508	1820-2699	8	2	IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U601	1820-2951	5	1	IC DRVR TTL ALS BUS OCTL	01295	SN74ALS240AN
U602	1810-0424	2	1	NETWORK-RES 16-DIP 4.7K OHM X 15	11236	761-1-R4.7K
U603	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U604	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U605	1810-0557	2		NETWORK-RES 16-DIP 22.0 OHM X 8	91637	MDP1603-220G
U606	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U607	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U608	1820-2724	0		IC LCH TTL ALS TRANSPARENT OCTL	01295	SN74ALS573BN
U702	1820-2635	2	1	IC GATE TTL ALS AND QUAD 2-INP	01295	SN74ALS08N
U703	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U704	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U705	1810-0533	4	1	NETWORK-RES 16-DIP 33.0 OHM X 8	91637	MDP1603-330G
U706	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U707	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U708	1820-2699	8		IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U802	1820-2634	1	4	IC INV TTL ALS HEX	01295	SN74ALS04BN
U803	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U804	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U805	1820-5212	7	4	IC BFR TTL F NAND DUAL 4-INP	18324	74F40N
U806	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U807	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U808	1820-2634	1		IC INV TTL ALS HEX	01295	SN74ALS04BN
U901	1820-3349	7	1	IC BFR TTL ALS NAND QUAD 2-INP	01295	SN74ALS38AN
U902	1820-2656	7	1	IC GATE TTL ALS NAND QUAD 2-INP	01295	SN74ALS00AN
U903	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U904	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U905	1820-5212	7		IC BFR TTL F NAND DUAL 4-INP	18324	74F40N
U906	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U907	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1001	1820-2692	1	1	IC GATE TTL F EXCL-OR QUAD 2-INP	07263	74F86PC
U1002	1820-2676	1	1	IC GATE TTL F AND-OR-INV	07263	74F64PC
U1003	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1004	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1005	1820-5212	7		IC BFR TTL F NAND DUAL 4-INP	18324	74F40N
U1006	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1007	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1101	1820-2634	1		IC INV TTL ALS HEX	01295	SN74ALS04BN
U1102	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1103	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1104	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1105	1820-5212	7		IC BFR TTL F NAND DUAL 4-INP	18324	74F40N
U1106	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1107	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1201	1820-2634	1		IC INV TTL ALS HEX	01295	SN74ALS04BN
U1202	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1203	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1204	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1205	1820-3731	1	1	IC GATE TTL AS NAND TPL 3-INP	01295	SN74AS10N
U1206	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10

Table 6-6. 12103M Replaceable Parts (sheet 4 of 4)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U1207	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1301	12103-80021	8	1	IC-PGM	28480	12103-80021
U1302	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1303	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1304	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1306	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1307	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1308	1820-3543	3		IC DRVR TTL AS BUS OCTL	01295	SN74AS240N
U1402	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1403	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1404	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1405	1810-1092	2	1	DELAY LINE ACTIVE DEVICE W/DUAL IN-LINE	07910	HY50-073
U1406	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1407	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1503	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1504	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1506	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1507	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1603	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1604	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1605	1820-2694	3	1	IC FF TTL F J-K NEG-EDGE-TRIG	07263	74F112PC
U1606	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
U1607	1818-4032	2		DRAM 1MX1 100 NS PLSTC FST-PG-M 5V	S0562	TC511000AP-10
	0403-0289	3	2	EXTR-PC BD RED POLYC 1.6-MM-BD-THKNS	28480	0403-0289
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	73957	GP24-063 X 250-17
	4114-1039	4	1	PLASTIC FLM POLYI AMB ADH-1-S	85480	XB-652
	5180-4275	6	1	PCB-MEMORY	28480	5180-4275
	7120-6829	6	1	LABEL-FRANCE	28480	7120-6829
	7120-6830	9	1	LBL-WARR DATE CD	28480	7120-6830
	7120-8074	7	1	LABEL-JAPAN	28480	7120-8074
	7121-0850	3	1	LBL-ANTISTAT BAG	76381	7101
	7121-0871	8	1	LBL-PR/WARRANTY	28480	7121-0871
	7121-2061	2	1	LABEL-DATE CODE	28480	7121-2061
	7121-2551	5	1	LABEL-INFO	28480	7121-2551
	7121-3054	5	1	LABEL BLANK	28480	7121-3054
	9211-5376	1	1	PACK-CONT	28480	9211-5376
	9222-0666	5	1	BAG-ANTISTATIC	76381	2100

Table 6-7. Manufacturer's Code List

MFR Number	Manufacturer Name	Address	Zip Code
D8439	Roederstein/Resista GMBH	Landshut, West Germany	8300
S0562	Toshiba Corp.	Tokyo, Japan	
01295	Texas Instruments Inc.	Dallas, TX	75265
04222	AVX Corp.	Great Neck, NY	11021
07263	Fairchild Semiconductor Corp.	Cupertino, CA 95014	
07910	Teledyne Semiconductor	Hawthorne, CA	90250
11236	CTS Corp.	Elkhart, IN	46514
12474	Bel-Ray Co. Inc.	Farmingdale, NJ	07727
12498	Crystalonics, Div. Teledyne	Cambridge, MA	02140
18324	Signetics Corp.	Sunnyvale, CA94086	
28480	Hewlett-Packard Co. Corp. HQ	Palo Alto, CA 94304	
34335	Advanced Micro Devices Inc.	Sunnyvale, CA94086	
56289	Sprague Electric Co.	Lexington, MA 02173	
73957	Groov-Pin Corp.	Ridgefield, NJ 07657	
76381	3M Co.	St. Paul, MN 55144	
85480	Brady W H Co.	Milwaukee, WI 53209	
91637	Dale Electronics Inc.	Columbus, NE 68601	

ROW 0 LOADED FOR 128KB (12103-60015) LOAD W1, 2, 3

ROW 0,# 1 LOADED FOR 256KB (12103-60017) LOAD W3, 4, 5 (A700 ONLY)

ROW 0 - 3 LOADED FOR 512KB (12103-60016) LOAD W5, 6, 7

RAM ARRAY

D-5955-4388-61

SYM	REVISIONS	APPROVED	DATE
B	REVISED	[illegible]	[illegible]
C	12103-60017 WAS 12103-60015 (A700 ONLY)	R. [illegible]	[illegible]
D	PCO 88-7604 ADDED NOTE	HVH	4-26-88

ENGINEERING RESPONSIBILITY: SE/A

ADDRESS MUX

DATA IN LATCH -2102 74LS373

DATA OUT DRIVER -2898 74F241

RAS SELECT

64K RAM 1818-3059

TO PIN 15 OF RAMS IN CORRESPONDING ROW

TO PIN 4 OF RAMS IN CORRESPONDING ROW

TO PIN 3 OF ALL RAMS

PULL DOWN 1

PULL DOWN 2

NOTES POWER AND GND PINS ARE NON-STANDARD ON THE RAMS
* INDICATES IC'S REQUIRING +5V VOLTAGE
UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/8W 1%
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY

NOTE : PULL DOWN 1 & 2 HAVE A PULL-UP RESISTOR ON THE 3065 TEST FIXTURE. (A) INDICATES LOW LEAKAGE PART.

DRAWN BY	Y. SUZUKI	3/8/82	A600 / A700 MEMORY ARRAY CARD
ENGINEER	MEHAFFEY	10-22-82	HEWLETT PACKARD
RELEASE TO PROD	[signature]	11/9/82	12103A & 12103C
SUPERSEDES DWG.			NEXT ASSEMBLY 12103B
			SHEET 1 OF 2
			12103-60015, -60017
			PART NUMBER -60016 (A)
			D-5955-4388-61

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	
16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43	

SYM	REVISIONS	APPROVED	DATE
B	[illegible]	[illegible]	[illegible]
C	ADD [illegible]	[illegible]	[illegible]
D	PC022-76014 U206 : DELETE [illegible]	[illegible]	4-24-85
E	PER DOC CHANGE, ADDED & ELIMINAT- ION FOR U206	[illegible]	[illegible]

D-5955-4388-2

-1441 74LS283 U202

-1441 74LS283 U102

SPARE GATES

-1449 74S32 U401

-1449 74S32 U401

-0829 74S112 U103

-0883 74S04 U205

-0884 74S86 U203

-1323 74S30 U204

-1451 74S38 U206

-1451 74S38 U206

J1-33	WI_7	(78)	
J1-31	WI_6	(79)	
J1-29	WI_5	(81)	
J1-27	WI_4	(77)	
J1-23	WI_3	(66)	
J1-21	WI_2	(70)	
J1-19	WI_1	(73)	
J1-17	WI_0	(88)	

(37) MO_7 → J1-34
(36) MO_6 → J1-32
(41) MO_5 → J1-30
(40) MO_4 → J1-28
(33) MO_3 → J1-24
(34) MO_2 → J1-22
(36) MO_1 → J1-20
(35) MO_0 → J1-18

+5M 1810-0235 UR215 2.2K

512K W7 (202) -0883 74S04 U205
256K W4 (203) -0883 74S04 U205
128K W1 (200) -0883 74S04 U205

(111) 128K+ → 10E

J1-16	A23-	WI_7	(78) (75)
J1-15	A22-	WI_6	(79) (80)
J1-14	A21-	WI_5	(81) (82)
J1-13	A20-	WI_4	(77) (78)
J1-12	A19-	WI_3	(66) (85)
J1-11	A18-	WI_2	(70) (72)
J1-10	A17-	WI_1	(73) (74)
J1-9	A16-	WI_0	(88) (89)

W3 128K 256K (71) (195)
W2 128K (67) (194)
W6 512K (74) (188)
W5 256K 512K (89) (170)

UR215 2.2K 1810-0235

R1 0757-442 10K
R2 0757-442 10K

(107) BDSEL- → 10E
(155) BDSEL+ → 10E
(115) ACK- → J1-48
(188) A17- → 10D
(170) A18- → 10D
(108) PCK- → J1-42
(104) TS_1 → 10A

19A PBIT+ (110)

19D BDRIVE+ (185)

P2 +5M
P2 +5V
J1 P1, P2 GND

0180-4842 0.22MF ONE PER 6 PACKS
0180-0374 10MF ONE PER 6 PACKS
0180-4842 0.22MF ONE PER 2 RAMS
0180-0374 10MF ONE PER ROM

E2 E1

1200-0997 TEST SOCKET U213

+5M = P2-45, 46
+5V = P2-35, 36, 37, 38
GND = J1-1, 2, 25, 26, 48, 50 / P1-13, 14, 18 / P2-2, 15, 17, 19, 21, 27, 29, 30, 31, 32, 33, 34

NOTES
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/8W 1%
ALL RESISTANCE IN OHMS
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY
# INDICATES PACKS SUPPLIED BY +5M
POWER AND GND CONNECTIONS TO EDGE CONNECTORS MUST BE DONE USING SOLID RINGS

DRAWN BY	Y. SUZUKI	DATE	3/22/82
ENGINEER	MEHAFFEY	DATE	10-22-82
RELEASE TO PROD	Vic Soulenas	DATE	11/9/82
SUPERSEDES DWG.			

TITLE: A600 / A700 MEMORY ARRAY CARD

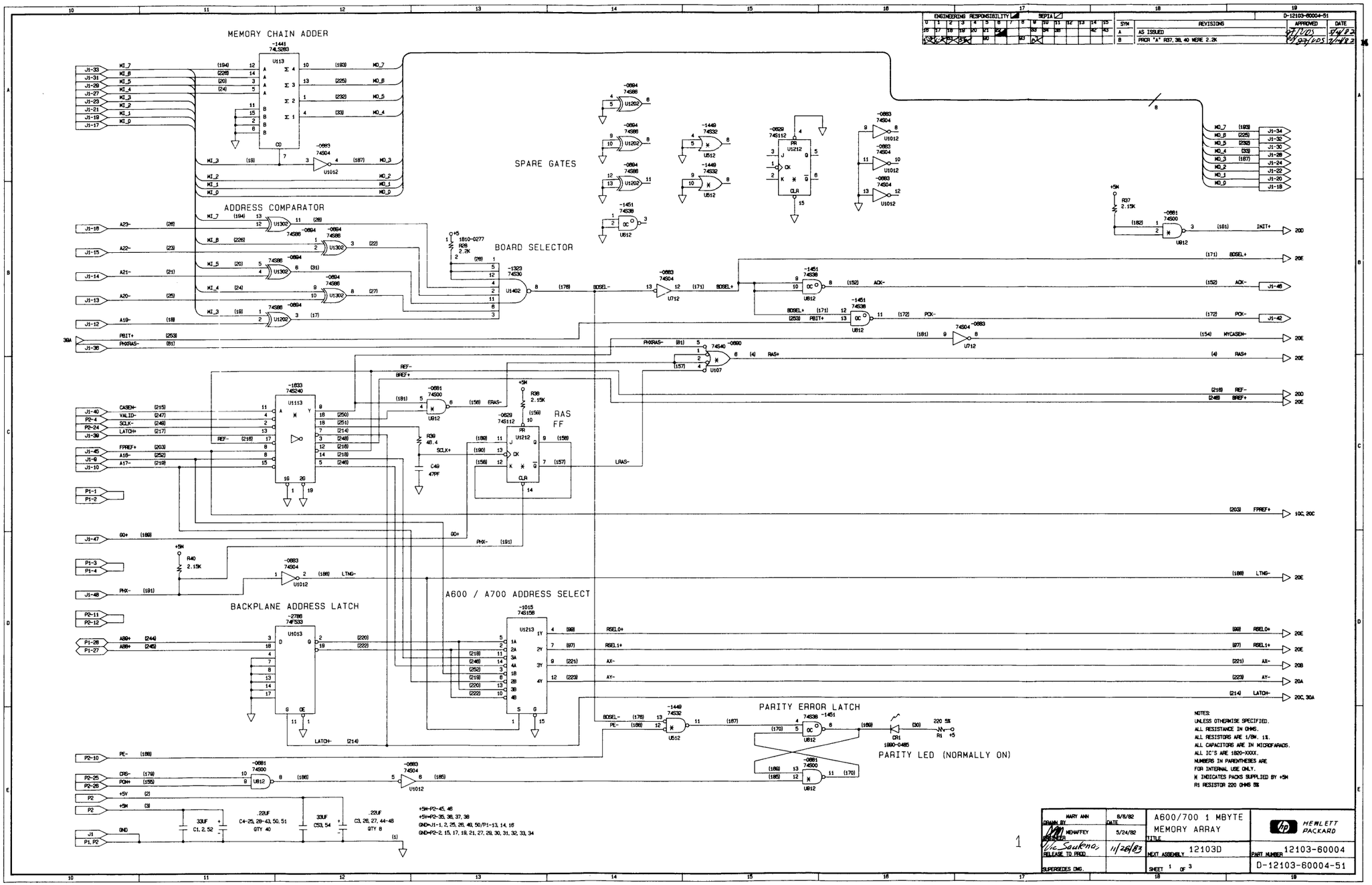
NEXT ASSEMBLY: 12103A, B, C,

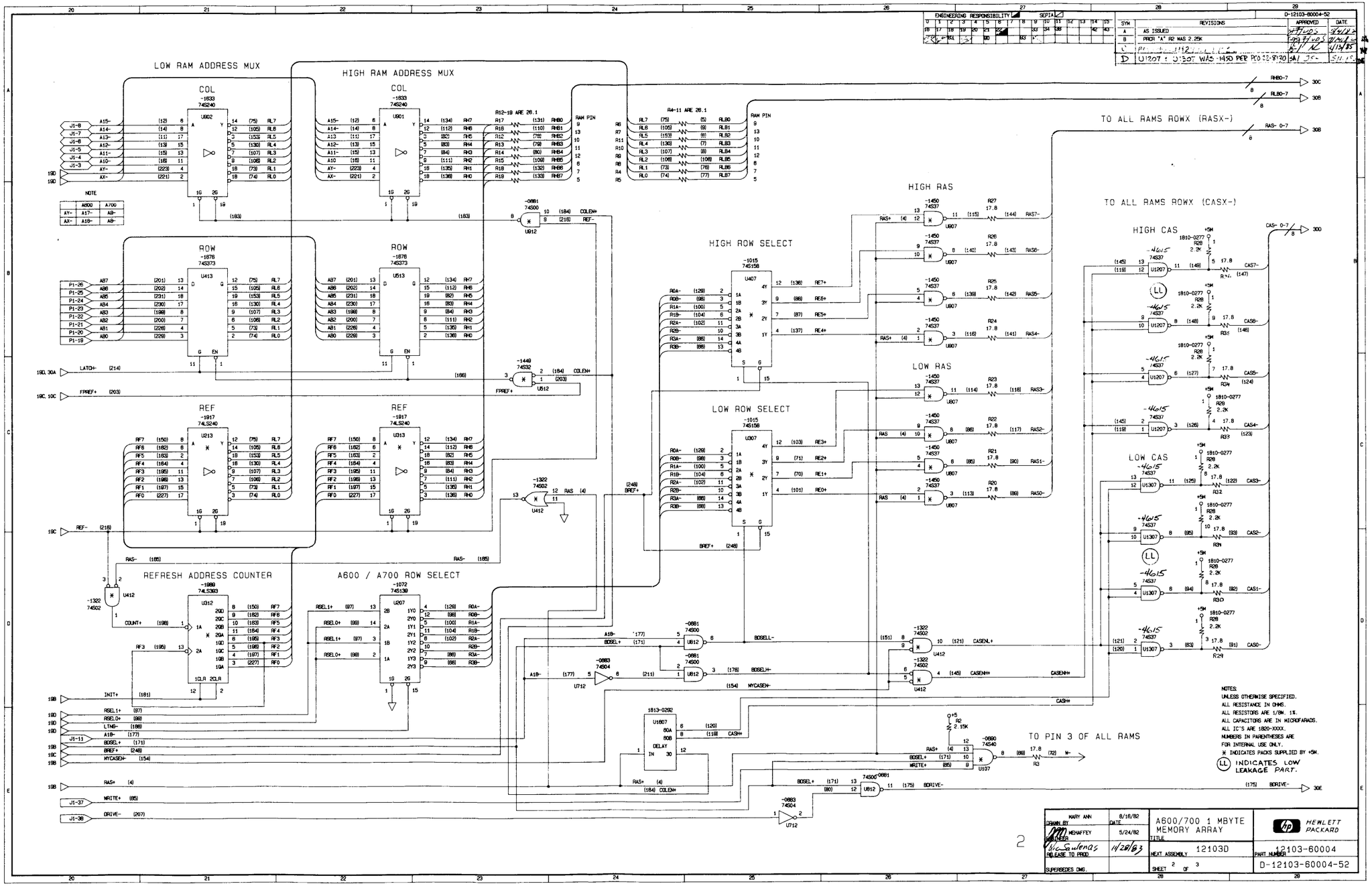
SHEET 2 OF 2

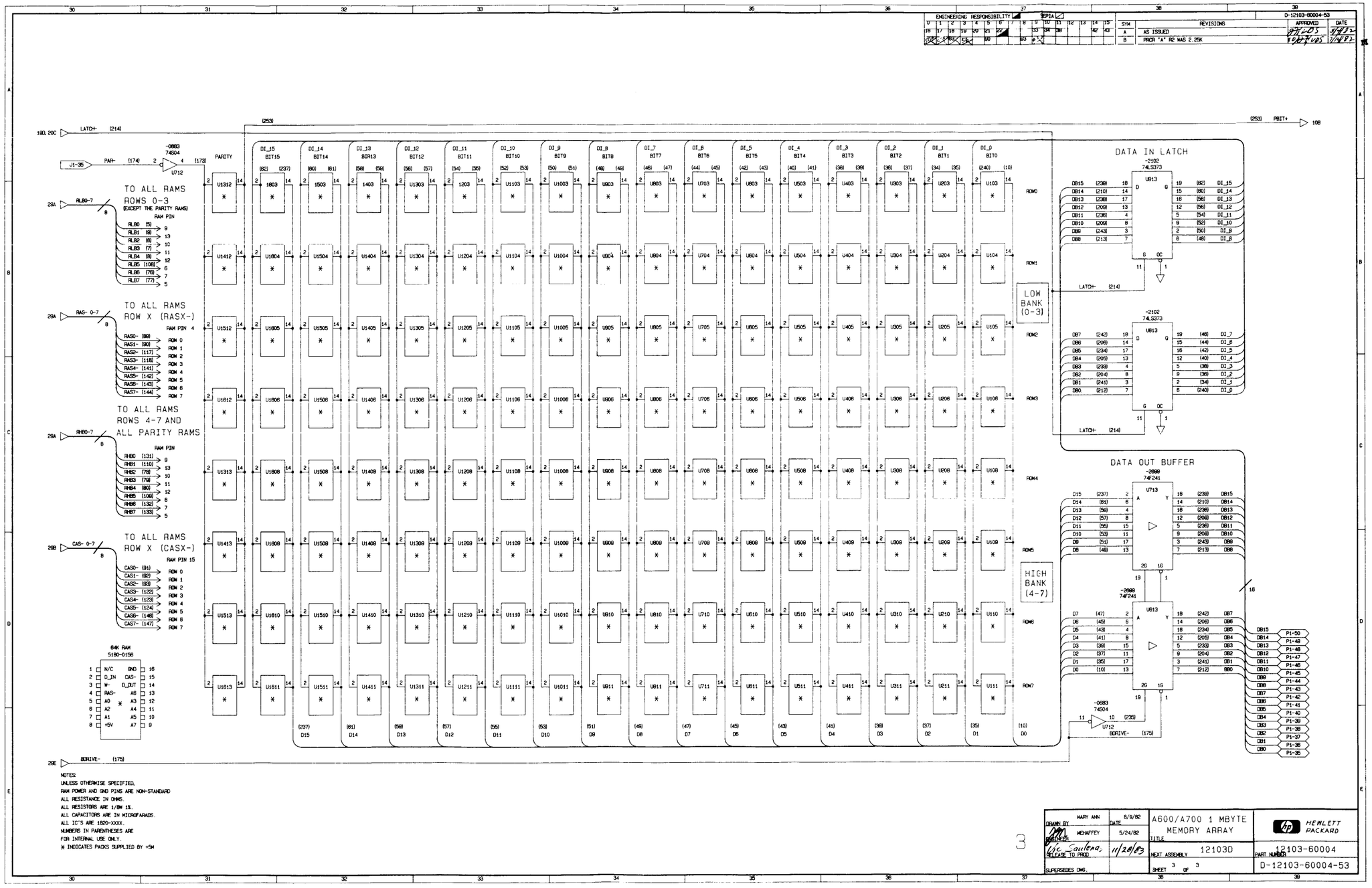
HEWLETT PACKARD

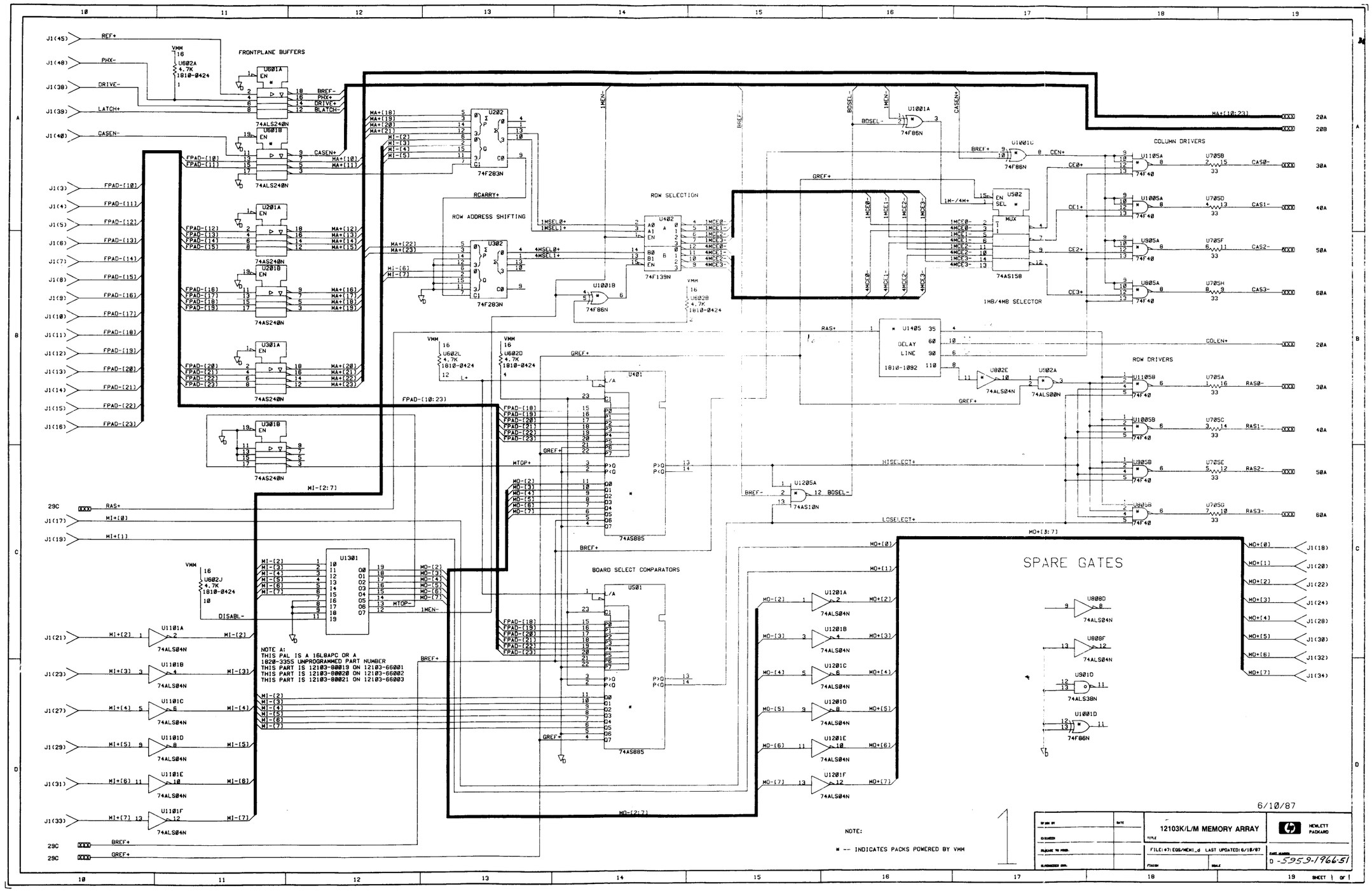
PART NUMBER 12103-60015, -60017 -60216

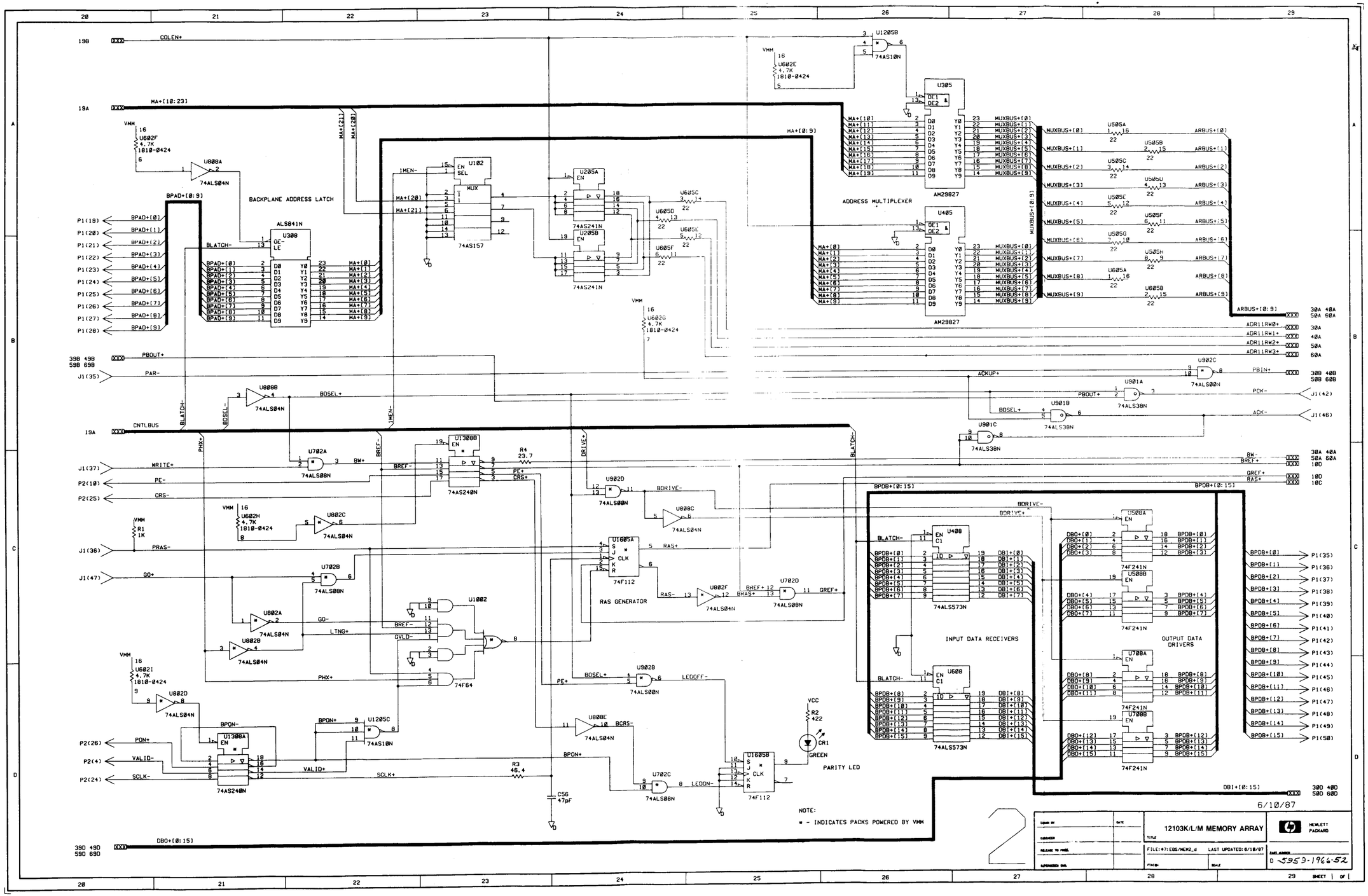
D-5955-4388-62

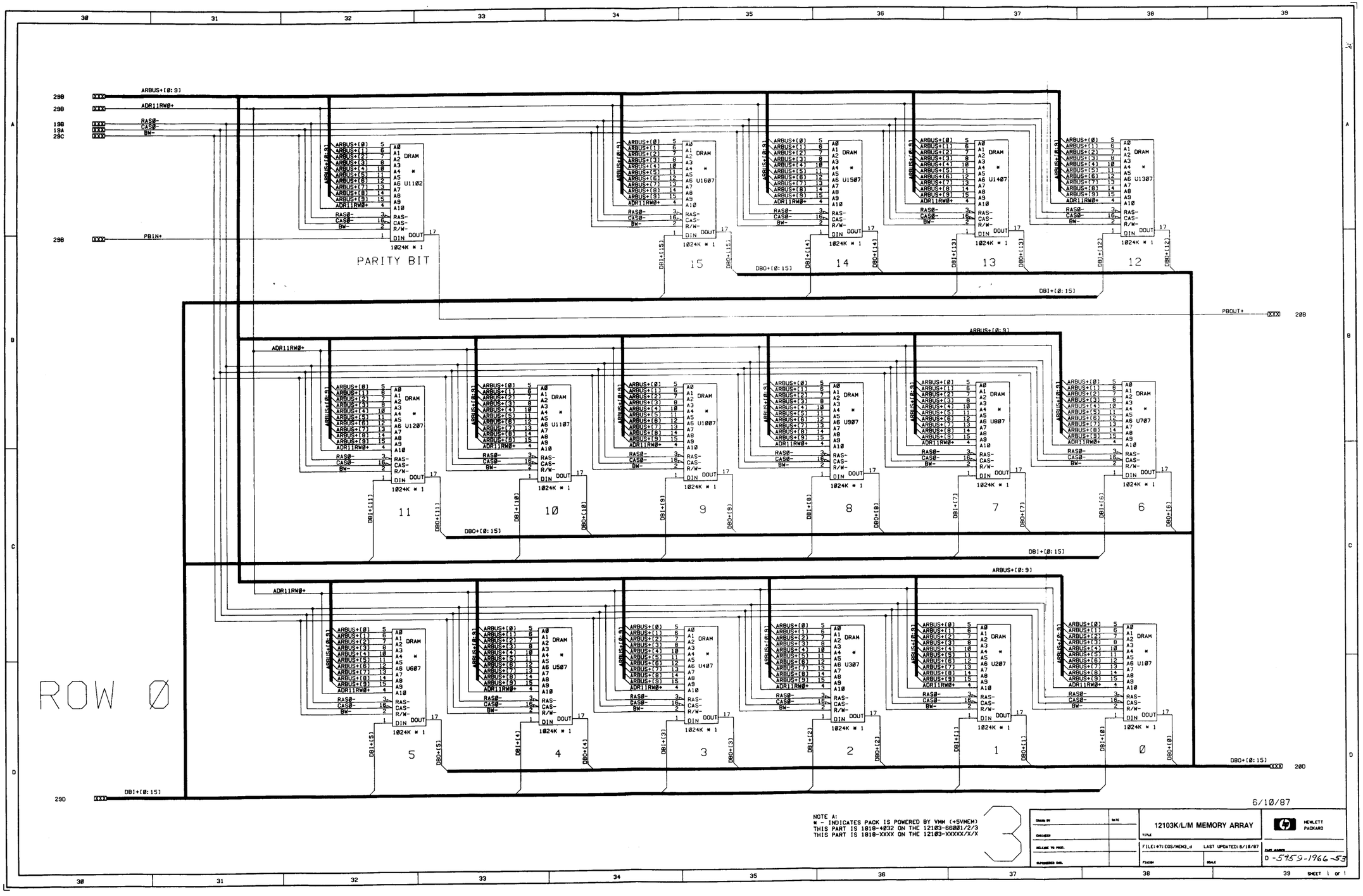

MEMORY CHAIN ADDER
SPARE GATES
ADDRESS COMPARATOR
BOARD SELECTOR
BACKPLANE ADDRESS LATCH
A600 / A700 ADDRESS SELECT
RAS FF
PARITY ERROR LATCH
PARITY LED (NORMALLY ON)
ENGINEERING RESPONSIBILITY
SEPIA
D-12103-60004-51
REVISIONS
APPROVED
DATE
A AS ISSUED
B PRDR "A" R37, 38, 40 WERE 2.2K
NOTES:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIED BY +5V
R1 RESISTOR 220 OHMS 5%
+5V-P2-45, 46
+5V=P2-35, 36, 37, 38
GND-J1-1, 2, 25, 26, 49, 50/P1-13, 14, 15
GND-P2-2, 15, 17, 19, 21, 27, 29, 30, 31, 32, 33, 34
MARY ANN
DRAWN BY
MEHAFFEY
DESIGNER
5/24/82
RELEASE TO PROD
11/26/83
SUPERSEDES DWG.
8/6/82
DATE
A600/700 1 MBYTE
MEMORY ARRAY
TITLE
12103D
NEXT ASSEMBLY
SHEET 1 OF 3
HEWLETT PACKARD
PART NUMBER 12103-60004
D-12103-60004-51

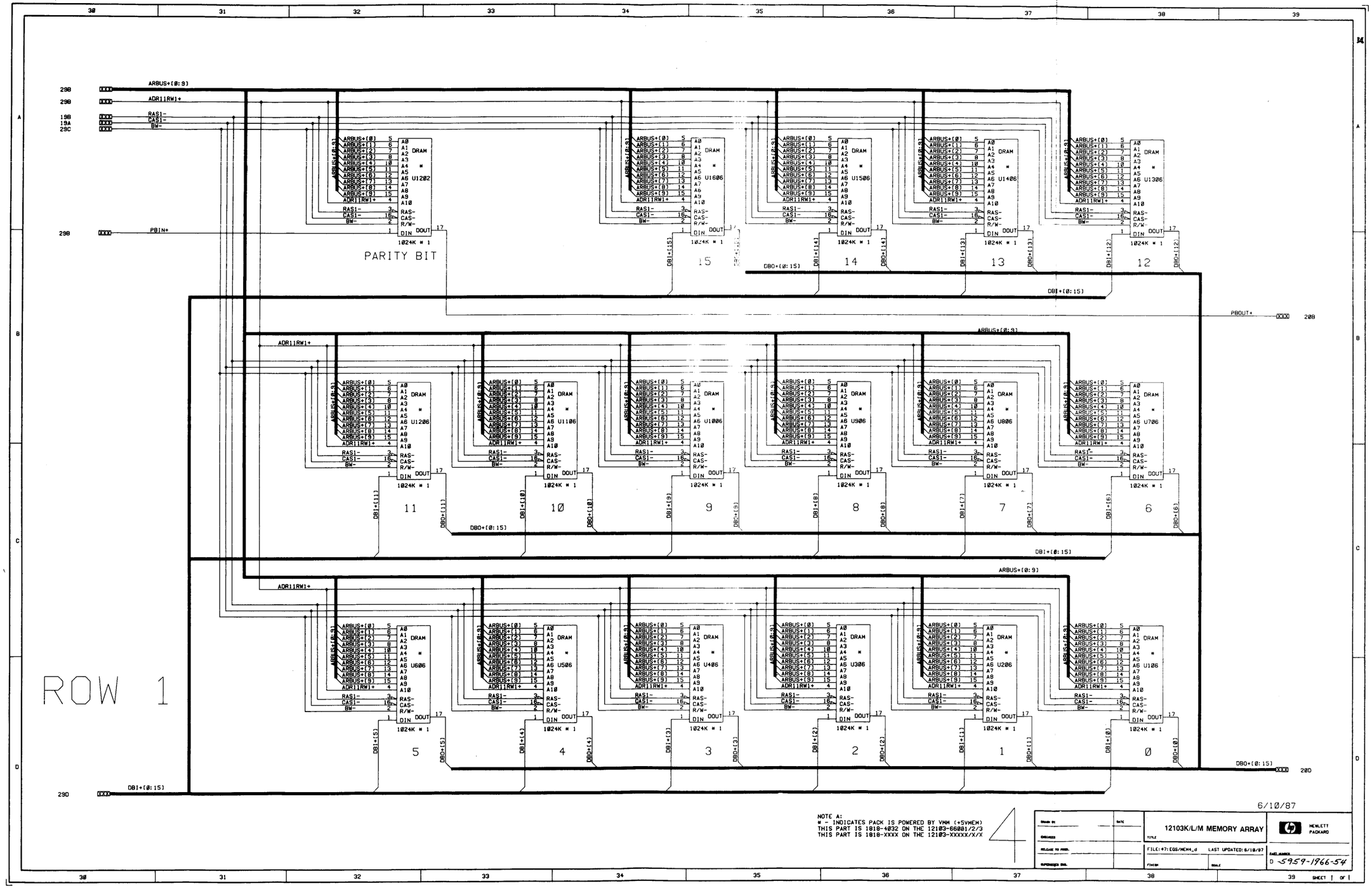

LOW RAM ADDRESS MUX
HIGH RAM ADDRESS MUX
COL
-1833
74S240
U602
U901
ROW
-1876
74S373
U413
U513
REF
-1917
74LS240
U213
U313
HIGH ROW SELECT
LOW ROW SELECT
-1015
74S156
U407
U607
HIGH RAS
LOW RAS
HIGH CAS
LOW CAS
-1450
74S37
U807
U1207
U1307
TO ALL RAMS ROWX (RASX-)
TO ALL RAMS ROWX (CASX-)
REFRESH ADDRESS COUNTER
-1989
74LS393
U312
A600 / A700 ROW SELECT
-1072
74S139
U207
TO PIN 3 OF ALL RAMS
NOTE
A600 A700
AY- A17- A8-
AX- A16- A9-
NOTES:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIED BY +5V.
(LL) INDICATES LOW LEAKAGE PART.
ENGINEERING RESPONSIBILITY
SEPIA
D-12103-60004-52
SYM REVISIONS APPROVED DATE
A AS ISSUED
B PROM "A" R2 WAS 2.25K
D U1207 : U1307 WAS -1450 PER PCO 12-8120-6A1
MARY ANN 8/16/82 DRAWN BY
MEHAFFEY 5/24/82 ENGINEER
RELEASE TO PROD
SUPERSEDES DWG.
A600/700 1 MBYTE MEMORY ARRAY TITLE
12103D NEXT ASSEMBLY
SHEET 2 OF 3
HEWLETT PACKARD
12103-60004 PART NUMBER
D-12103-60004-52

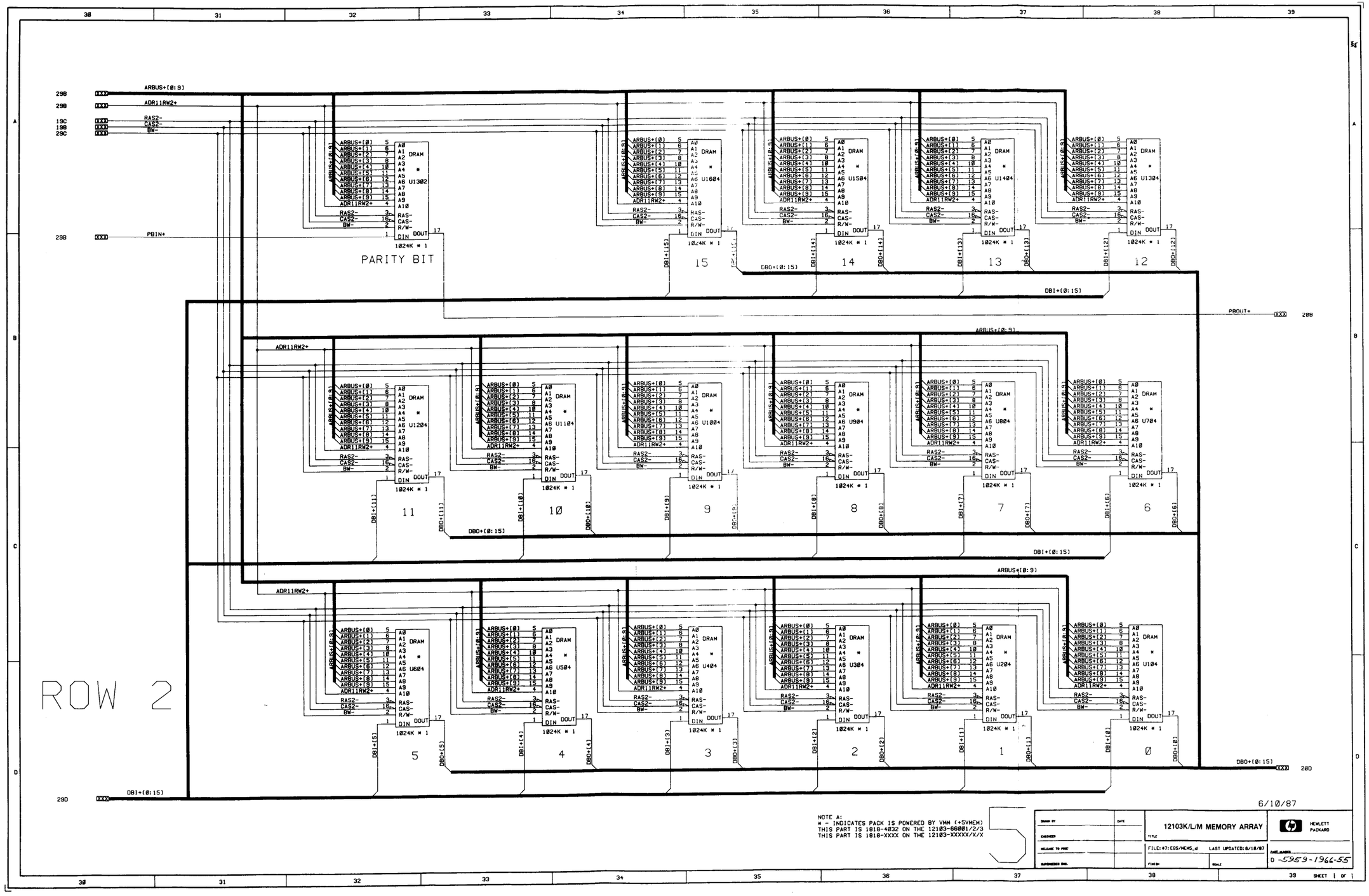

ENGINEERING RESPONSIBILITY
SEPIA
D-12103-80004-53
SYM
REVISIONS
APPROVED
DATE
A
AS ISSUED
B
PRIOR "A" R2 WAS 2.25K
LATCH+ (214)
PBIT+ 10B
PARITY
DI_15 BIT15
DI_14 BIT14
DI_13 BIT13
DI_12 BIT12
DI_11 BIT11
DI_10 BIT10
DI_9 BIT9
DI_8 BIT8
DI_7 BIT7
DI_6 BIT6
DI_5 BIT5
DI_4 BIT4
DI_3 BIT3
DI_2 BIT2
DI_1 BIT1
DI_0 BIT0
ROW0
ROW1
ROW2
ROW3
ROW4
ROW5
ROW6
ROW7
LOW BANK (0-3)
HIGH BANK (4-7)
TO ALL RAMS ROWS 0-3 (EXCEPT THE PARITY RAMS)
TO ALL RAMS ROW X (RASX-)
TO ALL RAMS ROWS 4-7 AND ALL PARITY RAMS
TO ALL RAMS ROW X (CASX-)
64K RAM 5180-0156
DATA IN LATCH
DATA OUT BUFFER
BDRIVE- (175)
NOTES:
UNLESS OTHERWISE SPECIFIED,
RAM POWER AND GND PINS ARE NON-STANDARD
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIED BY +5V
MARY ANN 8/9/82
DRAWN BY
MEHAFFEY 5/24/82
BROWNER
RELEASE TO PROD 11/20/83
SUPERSEDES DWG.
A600/A700 1 MBYTE MEMORY ARRAY
TITLE
NEXT ASSEMBLY 12103D
SHEET 3 OF 3
HEWLETT PACKARD
12103-60004
PART NUMBER
D-12103-60004-53

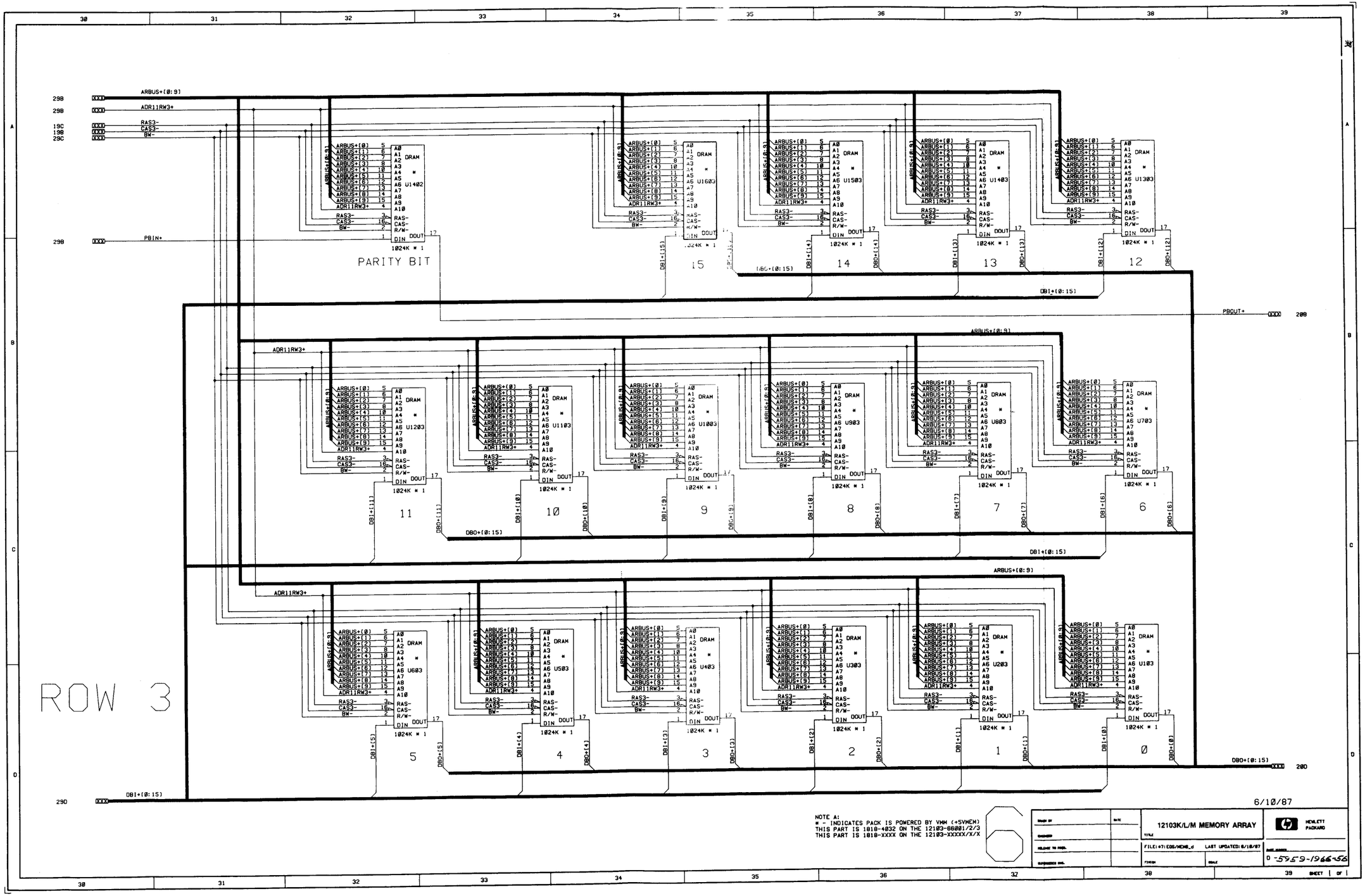

FRONTPLANE BUFFERS
ROW ADDRESS SHIFTING
ROW SELECTION
BOARD SELECT COMPARATORS
COLUMN DRIVERS
ROW DRIVERS
1MB/4MB SELECTOR
SPARE GATES
DELAY LINE 1810-1092
NOTE A:
THIS PAL IS A 16L8APC OR A
1820-3355 UNPROGRAMMED PART NUMBER
THIS PART IS 12103-80019 ON 12103-66001
THIS PART IS 12103-80020 ON 12103-66002
THIS PART IS 12103-80021 ON 12103-66003
NOTE:
* -- INDICATES PACKS POWERED BY VMM
12103K/L/M MEMORY ARRAY
D-5959-1966-51
6/10/87


BACKPLANE ADDRESS LATCH
ADDRESS MULTIPLEXER
RAS GENERATOR
INPUT DATA RECEIVERS
OUTPUT DATA DRIVERS
PARITY LED
NOTE:
* - INDICATES PACKS POWERED BY VMM
12103K/L/M MEMORY ARRAY
HEWLETT PACKARD
6/10/87

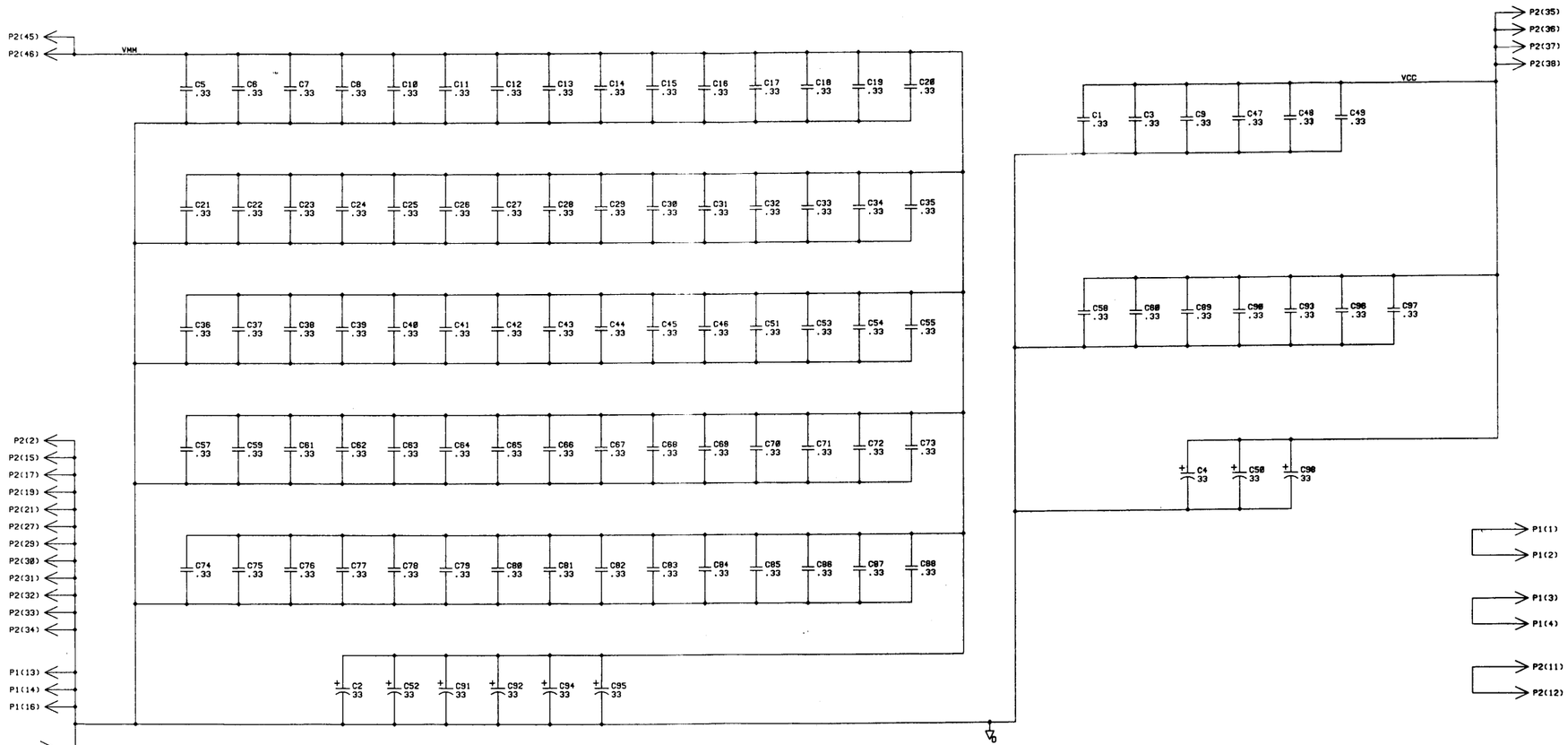

ARBUS+[0:9]
ADR11RW0+
RAS0-
CAS0-
BW-
PB1N+
PARITY BIT
DRAM
1024K * 1
DB1+[15]
DBO+[15]
DBO+[0:15]
DB1+[0:15]
PBOUT+
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
ROW 0
NOTE A:
N - INDICATES PACK IS POWERED BY VMM (+5VMEM)
THIS PART IS 1818-4032 ON THE 12103-66001/2/3
THIS PART IS 1818-XXXX ON THE 12103-XXXXX/X/X
6/10/87
12103K/L/M MEMORY ARRAY
HEWLETT PACKARD
FILE:#7:EQS/MEM3_d
LAST UPDATED:6/10/87
D-5959-1966-53
SHEET 1 OF 1


ARBUS+[0:9]
ADR11RW1+
RAS1-
CAS1-
BW-
PBIN+
PBOUT+
DBI+[0:15]
DBO+[0:15]
PARITY BIT
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
U1202
U1602
U1502
U1402
U1302
U1206
U1106
U1006
U906
U806
U706
U606
U506
U406
U306
U206
U106
U006
1024K * 1
DRAM
ROW 1
NOTE A:
* - INDICATES PACK IS POWERED BY VMM (+5VMEM)
THIS PART IS 1818-4032 ON THE 12103-66001/2/3
THIS PART IS 1818-XXXX ON THE 12103-XXXXX/X/X
6/10/87
12103K/L/M MEMORY ARRAY
HEWLETT PACKARD
FILE: 47:EOS/MEM4_d
LAST UPDATED: 6/10/87
D-5959-1966-54
SHEET 1 OF 1


ARBUS+[0:9]
ADR11RW2+
RAS2-
CAS2-
BW-
PB1N+
PARITY BIT
DBI+[0:15]
DBO+[0:15]
PROUT+
ROW 2
1024K * 1
DRAM
NOTE A:
* - INDICATES PACK IS POWERED BY VMM (+5VMEM)
THIS PART IS 1818-4032 ON THE 12103-66001/2/3
THIS PART IS 1818-XXXX ON THE 12103-XXXXX/X/X
6/10/87
12103K/L/M MEMORY ARRAY
HEWLETT PACKARD
FILE: #7:EOS/MEMS_d
LAST UPDATED: 6/10/87
D-5959-1966-55
SHEET 1 OF 1


ROW 3
ARBUS+[0:9]
ADR11RW3+
RAS3-
CAS3-
BW-
PBIN+
PBOUT+
PARITY BIT
DBI+[0:15]
DBO+[0:15]
1024K * 1
DRAM
DIN
DOUT
RAS-
CAS-
R/W-
NOTE A:
* - INDICATES PACK IS POWERED BY VMM (+5VMEM)
THIS PART IS 1818-4032 ON THE 12103-66001/2/3
THIS PART IS 1818-XXXX ON THE 12103-XXXXX/X/X
12103K/L/M MEMORY ARRAY
HEWLETT PACKARD
FILE:+7:EDS/MEMB_d
LAST UPDATED: 6/10/87
D-5959-1966-56
6/10/87

POWER SUPPLY BY-PASSING



NOTE A:
ALL CAPS UNLESS OTHERWISE SPECIFIED
ARE ALL IN MICROFARADS (uF)

6/10/87

12103K/L/M MEMORY ARRAY

HEWLETT PACKARD

FILE: 97:E88/MEM7_d LAST UPDATED: 6/10/87

D -5959-1966-5-7

SHEET 1 OF 1

7

Backplane

Introduction

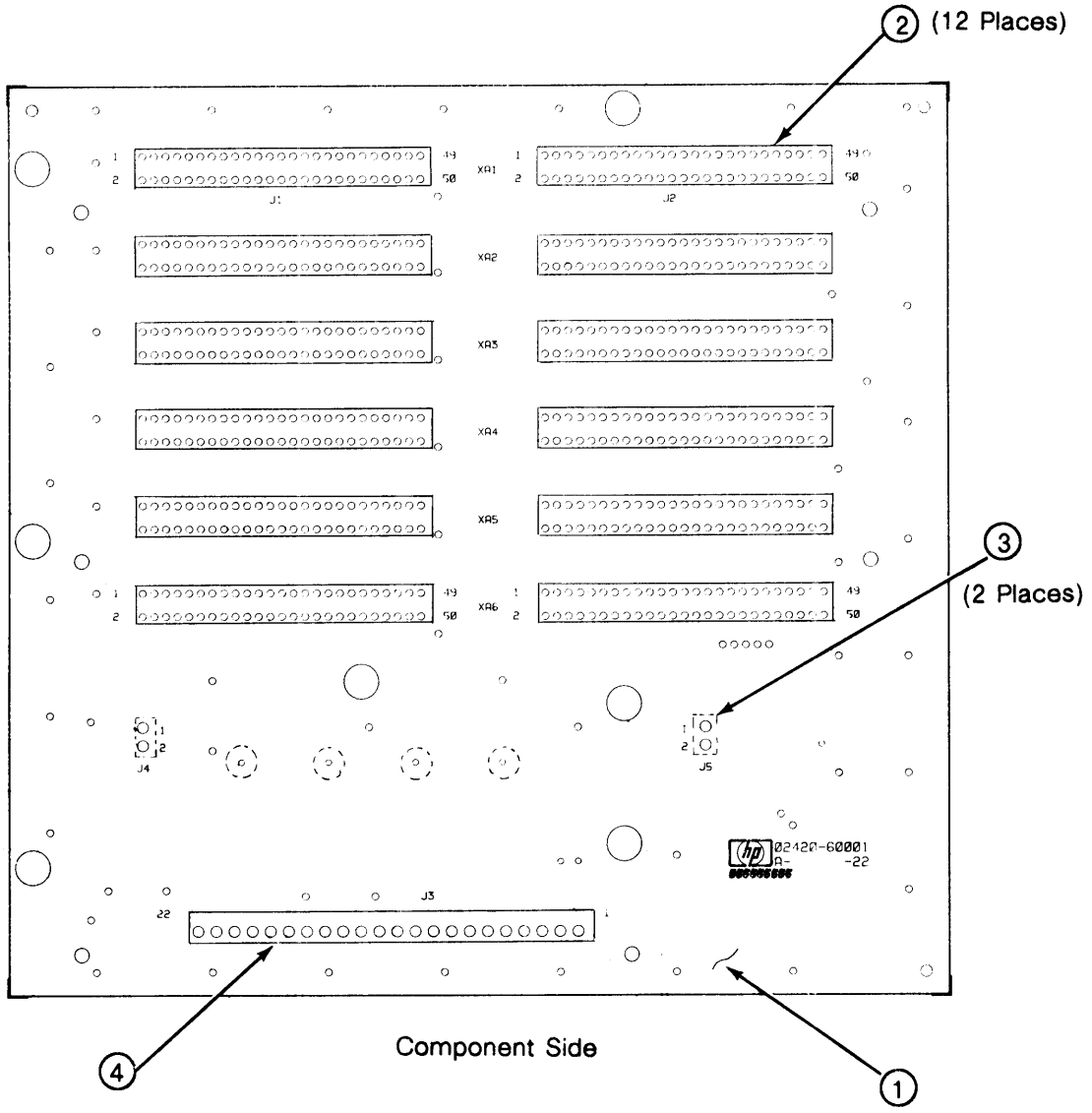
The backplane links the A400 single-board computer with other cards in the HP 1000 A-Series family such as memory arrays, I/O interface cards, and the power supply. This chapter describes the backplane from both a physical and a logical aspect.

The backplane functions as a mother board for the A400 board, additional memory cards, and interface cards. It is a printed circuit board on which traces carry the power, ground, and interconnecting signals between all the cards in the computer. Figures 7-1, 7-2, and 7-3 show the physical layout of the 6-slot, 16-slot, and 20-slot backplanes, respectively.

The logical backplane defines protocols for the communications between all of the cards in the system. The definition, function, and timing of the backplane signals, and the protocols for their interaction are all considered to be part of the logical backplane.

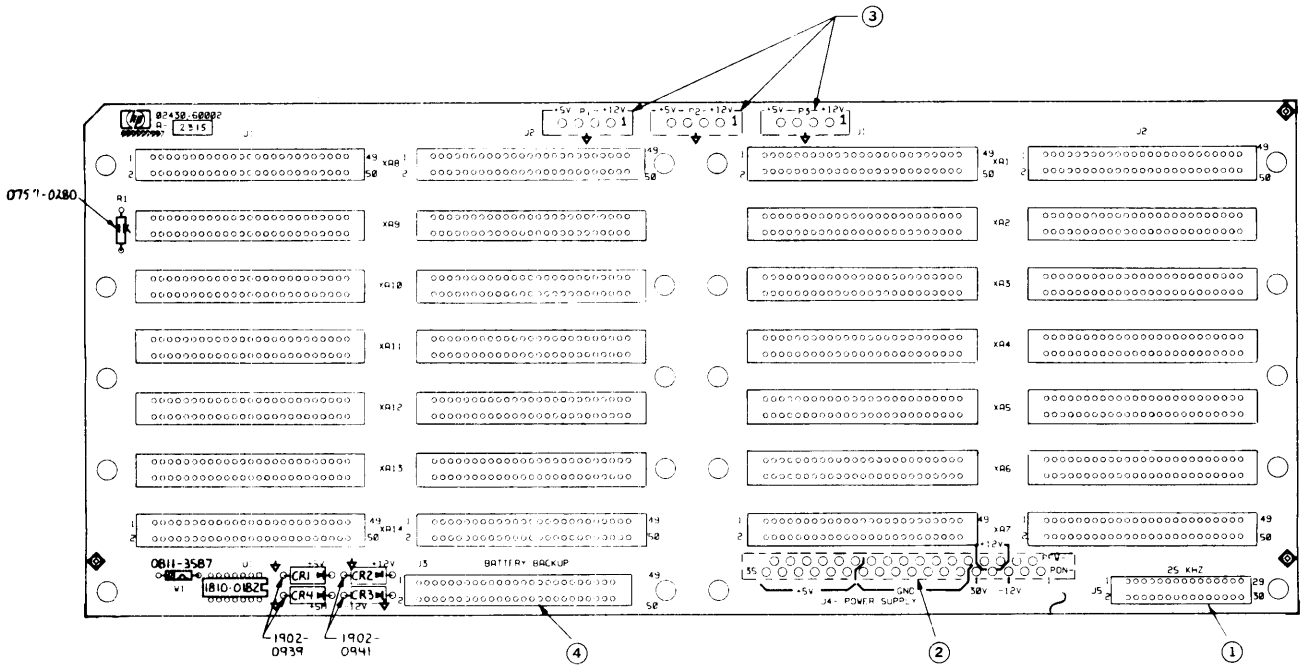
Thus, the physical backplane houses a set of communications channels, whereas the logical backplane defines protocols for that communication.

This chapter covers both aspects of the backplane, and is intended to provide all of the information needed to design a hardware interface to the backplane and thereby successfully integrate a design of arbitrary functions into the A400 Computer.



Item #	Description	Part #
1	PCB	02420-80001
2	Connector PC	1251-8053
3	Connector, 2-Pin	1252-1479
4	Connector, 22-Pin	1252-1480

Figure 7-1. HP 1000 6-Slot Backplane



ITEM	MATERIAL DESCRIPTION	PART NO.
1	CONN PC EDGE	1251-8396
2	CONN 35-PIN F	1251-8346
3	CONN 4-PIN	1251-8331
4	CONN 2 X 25	1251-8053

NOTE: Backplane 02430-60002 is replaced by 02430-60015. Parts locations of the two versions are identical.

Figure 7-2. HP 1000 16-Slot Backplane

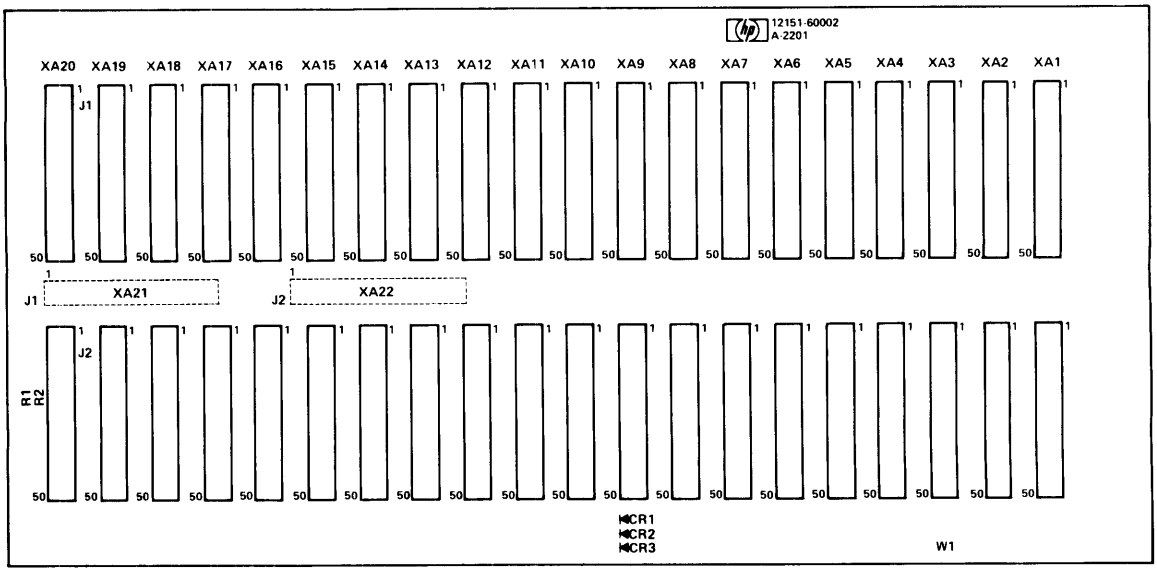


Figure 7-3. HP 1000 20-Slot Backplane

Backplane Physical Description

System Environment Overview

The backplane holds the following two sets of connectors for card edge connections:

1. Card Connector Slots

   Each card plugs into a set of dual 50-pin sockets (each set designated J1 and J2 of sockets XA1 through XA6 for the 6-slot backplane, XA1 through XA14 for the 16-slot backplane, and XA1 through XA20 for the 20-slot backplane). These pins carry signals, power, and ground connections between the cards and the backplane. The 6-slot backplane shown in Figure 7-1, used in the 2424A, has 6 sets of dual 50-pin sockets.

   The 16-slot backplane shown in Figure 7-2, used in the 2434A and 2484A, has 14 sets of dual 50-pin sockets for the CPU and I/O cards, a single 50-pin socket for the battery backup option, and a 30-pin socket for the 25 kHz card option. The 20-slot backplane shown in Figure 7-3, used in the 2134A, has 20 sets of dual 50-pin sockets.

2. Power Supply Connector Slots

   On the 6-slot backplane, DC power is connected to the backplane directly from the power supply through a 22-pin post header, designated J3, located below the connectors for slot 6. On the 16-slot backplane a single 35-pin connector, designated J4, is used for DC power.

   On the 20-slot backplane, DC power is connected to the backplane directly from the power supply through 50-pin sockets, designated J1 and J2 (sockets XA21 and XA22); that is, two power supply PC connector cards plug into the opposite side of the backplane from the A400 card side.

The A400 board can be plugged into any backplane card slot subject to the following rules:

- The first memory array card must go directly above the A400 board followed by any additional memory array cards.
- Any unused slot between two I/O cards must be filled with a priority jumper card.

The term "above" refers to a higher priority slot and "below" refers to a lower priority slot. The backplane slots are numbered from the highest priority slot XA1 in order down to XAn where n is the nth highest priority slot in the card cage.

Internal Specifications Overview

The diodes on the 16-slot and 20-slot backplane are on the +5V, +12V, and -12V lines from the power supply. They are transient voltage suppressers, with a clamping action response of one picosecond, and the capability of handling a surge current of 50 Amps. They serve to protect the components on the cards plugged into the backplane from any power supply over-voltage or transient spike. (Refer to Figures 7-2 and 7-3 for backplane parts locations.)

The physical backplane includes four different types of traces.

1. **Bus line:** This line is common to the same pin on each set of card sockets. Examples are WE- and CRS-.

2. **Power Supply line:** This line comes from the power supply and runs to the same pin on each set of card sockets. Examples are PFW- and PON+.

3. **Ground and Voltage lines:** This line comes from the power supply and typically has two or more pin assignments on each set of card sockets. Grounds and voltages are typically carried on much wider traces than other signals. Examples are +5V and +l2V.

4. **Chained lines:** This is a set of lines which connect every pair of adjacent card sockets. Each of these lines is common to exactly two sockets. Examples are ICHID-, ICHOD-, SCHID-, and SCHOD-.

The distinction between these four types of lines is important when determining backplane compatibility.

Backplane Interface Hardware

All backplane interface hardware can be grouped into one of the four categories listed below.

1. **CPU Interface**

   The signals and clocks generated by the CPU on the A400 board are carried to the other A-Series cards via the backplane. The clocks include SCLK and FCLK and the signals include such signals as RNI (Read Next Instruction) and IAK (Interrupt Acknowledge). The processor interface is described in Chapter 2.

2. **Memory Interface**

   The memory interface is also resident on the A400 board. It includes the memory controller and memory array interface circuitry. This interface is responsible for generating such signals as PE (memory Parity Error) and VALID (data bus Valid). The memory interface is described in Chapter 4.

3. **I/O Master Interface**

   The I/O master interface consists of an IOP chip and its support logic. This circuitry is located on the A400 board and on every A-Series I/O interface card. The I/O master serves to standardize the I/O interface to the backplane by performing all the functions (for example, I/O instruction recognition and execution, interrupt processing, and DMA control) common to all I/O cards.

4. **Passive Interfaces**

   Passive interfaces include those that supply, monitor, or use power lines. Signals may be monitored without ever interacting on the backplane.

General Hardware Specifications

6-Slot Backplane

The 6-slot backplane uses a four-layer, printed circuit board to provide all the required signal and power traces. The backplane consists of voltage and ground planes, signal lines, power traces to the DC fan, and traces to the power control switch. All cards mate to the backplane via twelve card-edge connectors (two per slot). The power supply connects to a 22-pin post header located below the connectors of the sixth slot.

Signal lines connect straight parallel paths between the six slots. Signal trace lengths and proximity to one another have been designed to minimize antenna loop areas and cross coupling for clean Electro-Magnetic Interference (EMI) characteristics.

16-Slot and 20-Slot Backplanes

The 16-slot and 20-slot backplanes use a six-layer, printed circuit board to provide all the required signal and power traces. One layer provides a +5V plane, and another is a ground plane to minimize signal cross-talk and to permit the traces to maintain a consistent characteristic impedance throughout their length.

The four remaining layers are mainly to carry signals and for voltage distribution. The layout provides a characteristic impedance of 47 to 51 ohms that provides a good match with the output impedances of the backplane drivers. The driver impedances are in the range of 25 to 100 ohms; that is, all impedances are matched within a 2-to-l ratio.

DC Power Routing

6-Slot Backplane

V_{cc} (+5.1V) and logic ground are distributed from the power supply to a voltage and ground plane, respectively. Fan power is routed via two dedicated traces which are located along the bottom edge of the backplane. These fan traces are spaced away from the other traces and planes to prevent electrical fan noise from coupling onto the logic lines and voltage planes.

+12V and −12V are wide power traces located on the signal layers.

The power control switch traces connect the remote enable signal on the power supply to a back-loaded Molex connector on the backplane.

Chassis ground on the backplane is connected to DC Common via a stub trace on the component side of the board. It is located below the fan connector (J4), connecting the window frame to the DC Common cross-hatch. The stub trace can be removed if necessary for experimenting with ground loops. If removed, the connection can be restored by using a wire jumper in the two holes located directly below J4. Chassis ground is also brought to the outer layer ground planes for effective EMI shielding.

16-Slot and 20-Slot Backplanes

Ground and +5V lines carry the highest currents, therefore these traces are transferred over whole planes. Currents for other voltages are carried over multiple traces.

On the 16-slot backplane, chassis ground is connected to DC Common via a 0-ohm resistor located below socket XA14.

Power Supply Interconnect

The pin assignments for the DC output connector P1 for the 6-slot and the 16-slot backplane and connectors P1 and P2 for the 20-slot backplane power supply connectors are given in Table 7-1.

Table 7-1. Power Supply Connector Pin Assignments

6-Slot Connector P1		16-Slot Connector P1	
Pin Number	**Signal Name**	**Pin Number**	**Signal Name**
1	PFW–	1	PON+
2	PON+	2	PFW–
3 thru 8	+5.1V DC	3	25 kHz ϕ1
9 thru 14	DC Common	4	25 kHz ϕ2
15, 16	+12V DC	5	–12V DC
17, 18	DC Common	6 thru 8	+12V DC
19	–12V DC	9	+28V DC
20	DC Common	10 thru 23	Common
21	Remote Enable	24 thru 35	+5.1V DC
22	Not used (spare)		

20-Slot Connectors P1 and P2

Connector P1		Connector P2	
Pin Number	**Signal Name**	**Pin Number**	**Signal Name**
1 thru 36	+5.1V DC	1 thru 28	Common
37 thru 50	Common	29 thru 32	+12V DC
		33, 34	–12V DC
		35 thru 38	+5V Mem BB
		39 thru 42	25 kHz ϕ1
		43 thru 46	25 kHz ϕ2
		47	PON+
		48	PFW–
		49	MLOST–
		50	SPARE

Card Socket Interconnects

Each card used in the A400 Computer has two 50-pin edge-connectors, Pl and P2, which plug into a set of 50 pin sockets J1 and J2 on the backplane, respectively. The card cage is constructed with card guides. The cards slide in along the card guides and then snap into place in the backplane connectors. The cards must be inserted with the component sides of the cards facing the same way as shown in Figure 7-4. The pin assignments for these l00 connections are given in Table 7-2. For signal definitions, refer to Table 7-34.

Backplane Loading Rules

Backplane loading rules were established to provide guidelines for the selection of bus drivers and backplane signal drivers, and to ensure that these drivers are not overloaded. These rules take into account the drive capabilities and loading of certain industry standard parts such as the S/LS240 and S/LS241. Each card must adhere to the rules in order to prevent possible overloading. These loading rules were established assuming a maximum system in a 20-slot box. Note that the I/O Master was designed such that all backplane lines except the data bus are buffered and cannot be used in the unbuffered form by I/O interface logic external to the I/O Master.

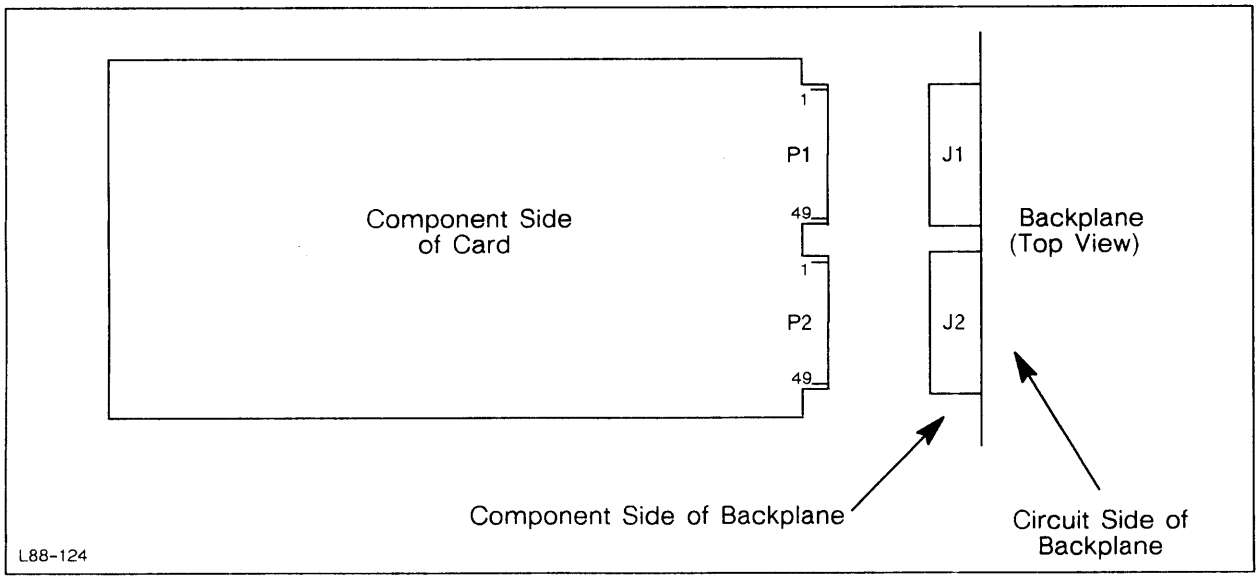


Figure 7-4. Card Socket Interconnects

Table 7-2. Pin Assignments for Backplane Sockets

Pin	XAnP1 Signals		Pin	Pin	XAnP2 Signals		Pin
1	ICHID–	* ICHOD–	2	1	CPUTURN–	ISOGND	2
3	MCHID–	MCHOD–	4	3	† REMEM–	VALID–	4
5	MLOST–	MCHODOC–	6	5	IORQ–	INTRQ–	6
7	PFW–	FETCH–	8	7	MP+	RNI–	8
9	AE0 (SC0)	AE1 (SC1)	10	9	MEMGO–	PE–	10
11	AE2 (SC2)	AE3 (SC3)	12	11	SCHID–	** SCHOD–	12
13	GND	GND	14	13	IAK–	IOGO–	14
15	EC–	GND	16	15	ISOGND	SLAVE–	16
17	AE4 (SC4)	SELFC–	18	17	ISOGND	MRQ–	18
19	AB0	AB1	20	19	ISOGND	† FCLK–	20
21	AB2	AB3	22	21	ISOGND	CCLK–	22
23	AB4	AB5	24	23	† SPRQ–	SCLK–	24
25	AB6	AB7	26	25	CRS–	PON+	26
27	AB8	AB9	28	27	ISOGND	BUSY–	28
29	AB10	AB11	30	29	GND	GND	30
31	AB12	AB13	32	31	GND	GND	32
33	AB14	WE–	34	33	GND	GND	34
35	DB0	DB1	36	35	+5V	+5V	36
37	DB2	DB3	38	37	+5V	+5V	38
39	DB4	DB5	40	39	† +12M	† –12M	40
41	DB6	DB7	42	41	+12V	+12V	42
43	DB8	DB9	44	43	–12V	–12V	44
45	DB10	DB11	46	45	+5M	+5M	46
47	DB12	DB13	48	47	25 kHz ϕ2	25 kHz ϕ2	48
49	DB14	DB15	50	49	25 kHz ϕ1	25 kHz ϕ1	50

* Above the A400 board, this signal is called PS–.

** Above the A400 board, this signal is called MEMDIS–.

† These are L-Series signals which are spares for the A-Series and are not used on the A400.

DC Loading

DC loading rules are made to ensure that a device driving any given backplane line can handle sufficient current to keep all the inputs connected to that line at the required voltage level. Low-state load on a given line is the sum of the input low-level leakage current for all receivers (I_{IL}) plus the tri-state low-level leakage current for all tri-state drivers (I_{OZL}) on the line. High-state load is the sum of the input high-level leakage current for all receivers (I_{IH}) plus the tri-state high-level leakage current for all tri-state drivers (I_{OZH}).

Actual Worst Case Loading

Actual worst case loading in a 16-slot box for the address bus (AB[0:14]), address-extension bus (AE/SC[0:4]), and the data bus (DB[0:15]) is as follows (where LS = low-state load in mAmps, and HS = high-state load in μAmps):

Maximum Memory

	AB[0:9]		AB[10:14]		(SC[0:4]) AE[0:4]		DB[0:15]	
	LS	HS	LS	HS	LS	HS	LS	HS
12103D (times 3)	1.80	300	0	0	0	0	1.35	210
12103C	0.60	50	0	0	0	0	0.45	70
12100A	3.14	290	1.22	60	1.22	60	1.00	40
I/O Master (times 9)	3.60	180	3.60	180	3.60	180	8.75	900
Total:	9.14	820	4.82	240	4.82	240	11.55	1220

Maximum I/O

12100A	3.14	290	1.22	60	1.22	60	1.0	40
I/O Master (times 13)	5.20	260	5.20	260	5.20	260	12.6	1300
Total:	8.34	550	6.42	320	6.42	320	13.6	1340
Worst case overall:	9.14	820	6.42	320	6.42	320	13.6	1340

The design rules and guidelines are shown in Table 7-3.

Table 7-3. Design Rules and Guidelines

Design Rules/Guidelines	Address Bus AE[0:4]	Data Bus	All Other Bussed Lines	Chained Lines
Maximum allowable load per card – HS	130 μA	250 μA	60 μA	400 μA
Maximum allowable load per card – LS	1.2 mA	1.2 mA	1 mA	10 mA
Minimum allowable drive capability – HS	2.6 mA	5.0 mA	1.2 mA	1 mA
Minimum allowable drive capability – LS	24 mA	24 mA	20 mA	20 mA
where: HS = High State LS = Low State				

AC Loading

Every connection made to any given line places a capacitive load on that line due to PC board trace capacitance and due to the integrated circuit input or output capacitance. Care must be taken to ensure that any given line is not capacitively overloaded as this results in a slowing down of its switching speed to below an acceptable level. Typical delays/capacitive loads are in the range of 2-nanoseconds/50-picofarads for a line driven by an LS240/241 and 4-nanoseconds/50-picofarads for an LS373/374.

The AC loading specifications, as with the DC loading rules, should be strictly adhered to for the I/O interfaces but they can be used as guidelines for processor and memory cards. Signal timing calculations are made considering actual worst case loads as shown in Table 7-3 (a 20-slot system is assumed).

Data Bus

Each card cannot exceed 60 picofarads load per line.

All Other Lines

Each card cannot exceed 25 picofarads load per line.

Backplane Logical Description

The following paragraphs pertain exclusively to the logical backplane. The protocols and conventions used by all A-Series cards to interact over the backplane are described. An important feature of an A-Series computer is its distributed intelligence. Every interface card in the system has the capability of handling its own memory accesses (DMA), of decoding its own instructions, and of forcing the central processor into slave mode processing. Each of these three capabilities and the protocols with which they are implemented are described. You may find it helpful, while working through each handshake protocol, to refer to the glossary of signal definitions in Table 7-34.

Table 7-4. Capacitance Data on 20-Slot System

Pin	Signal	C_L in pF
J1 - 1, 2	ICHID, ICHOD	40
J1 - 3, 4	MCHID, MCHOD	25
J1 - 5	MLOST	200
J1 - 6	MCHODOC	850
J1 - 7	PFW	200
J1 - 8	FETCH	250
J1 - 9,10,11,12,17	AE[0:4] (SC[0:4])	400
J1 - 18	SELFC	900
J1 - 19 thru 34	ADDRESS BUS	500
J1 - 35 thru 50	DATA BUS	1300
J2 - 1	CPUTURN	400
J2 - 3	REMEM	600
J2 - 4	VALID	550
J2 - 5	IORQ	580
J2 - 6	INTRQ	650
J2 - 7	MP	500
J2 - 8	RNI	500
J2 - 9	MEMGO	550
J2 - 10	PE	500
J2 - 11,12	SCHID, SCHOD	30
J2 - 13	IAK	500
J2 - 14	IOGO	500
J2 - 16	SLAVE	740
J2 - 18	MRQ	550
J2 - 20	FCLK	500
J2 - 22	CCLK	620
J2 - 23	SPRQ	250
J2 - 24	SCLK	500
J2 - 25	CRS	500
J2 - 26	PON	550
J2 - 28	BUSY	400

Note that all capacitances shown are worst case figures.

Memory Access Protocol

Every card that accesses memory uses the same handshake protocol. This approach greatly simplifies the operation of multichannel DMA. The DMA feature of every A-Series I/O interface allows input or output operations to proceed without processor intervention, thus significantly decreasing the processing requirements on the CPU.

The processor is the lowest-priority memory requester (the on-board I/O is the highest). If any other card pulls on the open-collector line MRQ (Memory Request), the processor is kept from doing a memory cycle. This means that the processor may be locked out by high speed interfaces using adjacent memory cycles. To prevent being locked out entirely, the processor can assert the CPUTURN- signal after waiting 32 consecutive memory cycles. CPUTURN- informs the interface cards not to reassert MRQ after their current memory request is satisfied.

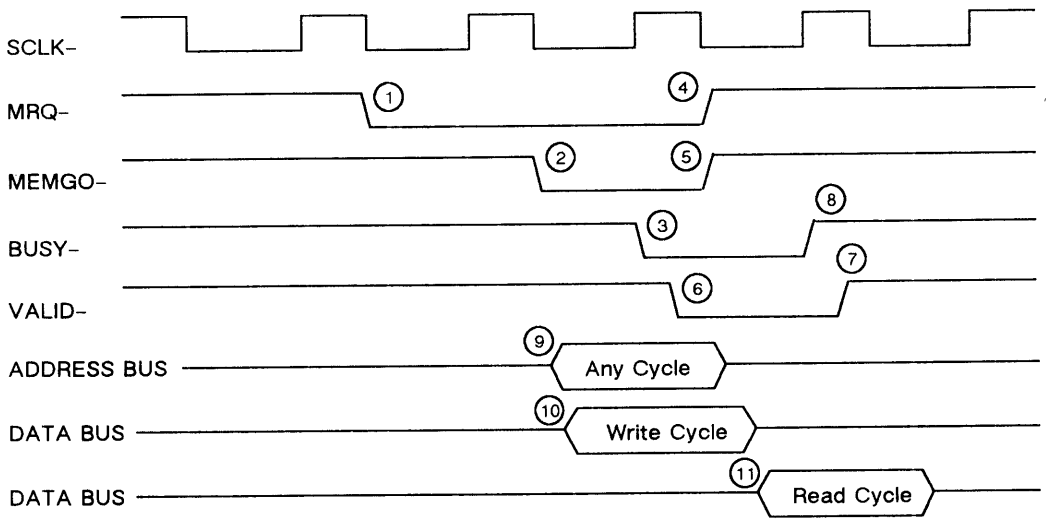
A priority scheme is used in the A-Series computers to resolve contention between interfaces wanting memory cycles. An interface determines if it is entitled to a memory cycle by monitoring certain backplane signals, like BUSY-, CPUTURN-, and MCHID-. The first signal, MRQ-, disables the processor from taking the next memory cycle. A signal called MCHOD- is part of a priority chain that ripples down, disabling all lower-priority interfaces. MCHODOC- is a look-ahead on this chain. It is used as the top of the chain for the stack of lowest-priority slots. Although MRQ- may be asserted by one or more interfaces at any given time, MEMGO- may only be asserted by the one interface that gets the memory cycle.

An interface determines if it is entitled to a memory cycle (to assert MEMGO-) by monitoring certain backplane signals. It can initiate a memory cycle on any falling edge of SCLK- when BUSY- is high, its MCHID- is high, and its MRQ- has been asserted for at least one cycle. This stipulation means that contention among I/O cards for memory always has one cycle of SCLK in which to be resolved, namely, the cycle that occurs just before the assertion of MEMGO-.

The processor card begins its access to memory by asserting MEMGO- on the falling edge of SCLK-. If an I/O interface card desiring a DMA transfer asserts MRQ- on that same edge, the processor card immediately relinquishes its claim to accessing memory by releasing MEMGO- prior to the next rising edge of SCLK-. Therefore, contention between the processor and any I/O interface for memory is resolved in favor of the I/O interface. The processor's MEMGO- signal will only be asserted after the completion of all current DMA requests. Refer to Table 7-17 for the aborted MEMGO- timing specifications.

Memory Handshake Timing

Memory handshake timing is part of the Memory and I/0 state machine operation. The memory handshake timing is shown in Figure 7-5.



① An interface card asserts MRQ- to request a memory cycle. (MCHOD- is asserted simultaneously to hold off all lower priority cards).

② An interface card asserts MEMGO-, if one cycle after the assertion of MRQ-, it still has priority; that is, its MCHID- is high. If MRQ- is not asserted, the MEMGO- is from the processor, or an interface card during an interrupt cycle.

③ Memory asserts BUSY-, once MEMGO- has been asserted, in order to hold off other memory cycles until this cycle can be completed.

④ An interface card releases MRQ- at the end of the short half cycle when MEMGO- is released.

⑤ MEMGO- is released one cycle after being asserted.

⑥ Memory asserts VALID- during the last cycle of BUSY-.

⑦ VALID- is released to signal that data is valid on the backplane.

⑧ BUSY- is released to signal that a new memory cycle can begin.

⑨ The address bus is driven by the interface card during the assertion of MEMGO-.

⑩ In the case of a memory write cycle, the interface data is valid on the backplane shortly after the address bus.

⑪ In the case of a memory read cycle, the memory guarantees valid data on the rising edge of VALID-.

* BUSY is generally asserted for one SCLK- cycle but may be asserted as long as three SCLK- cycles.
VALID is always one SCLK- cycle and is the last SCLK- cycle of the access.

L8200-132A

Figure 7-5. Memory Handshake Timing

Interrupt Protocol

In the A400, interrupt priority is determined only by physical proximity to the processor on the interrupt priority chain (the on-board I/O is therefore always the highest priority). The interrupt service routine, however, is determined by the select code of the interrupting I/O interface. This select code is independent of the physical location of the interface. The select code of the on-board I/O is hard-wired to 77 octal and cannot be changed. It is determined on each I/O card by setting six switches, one switch per select code bit.

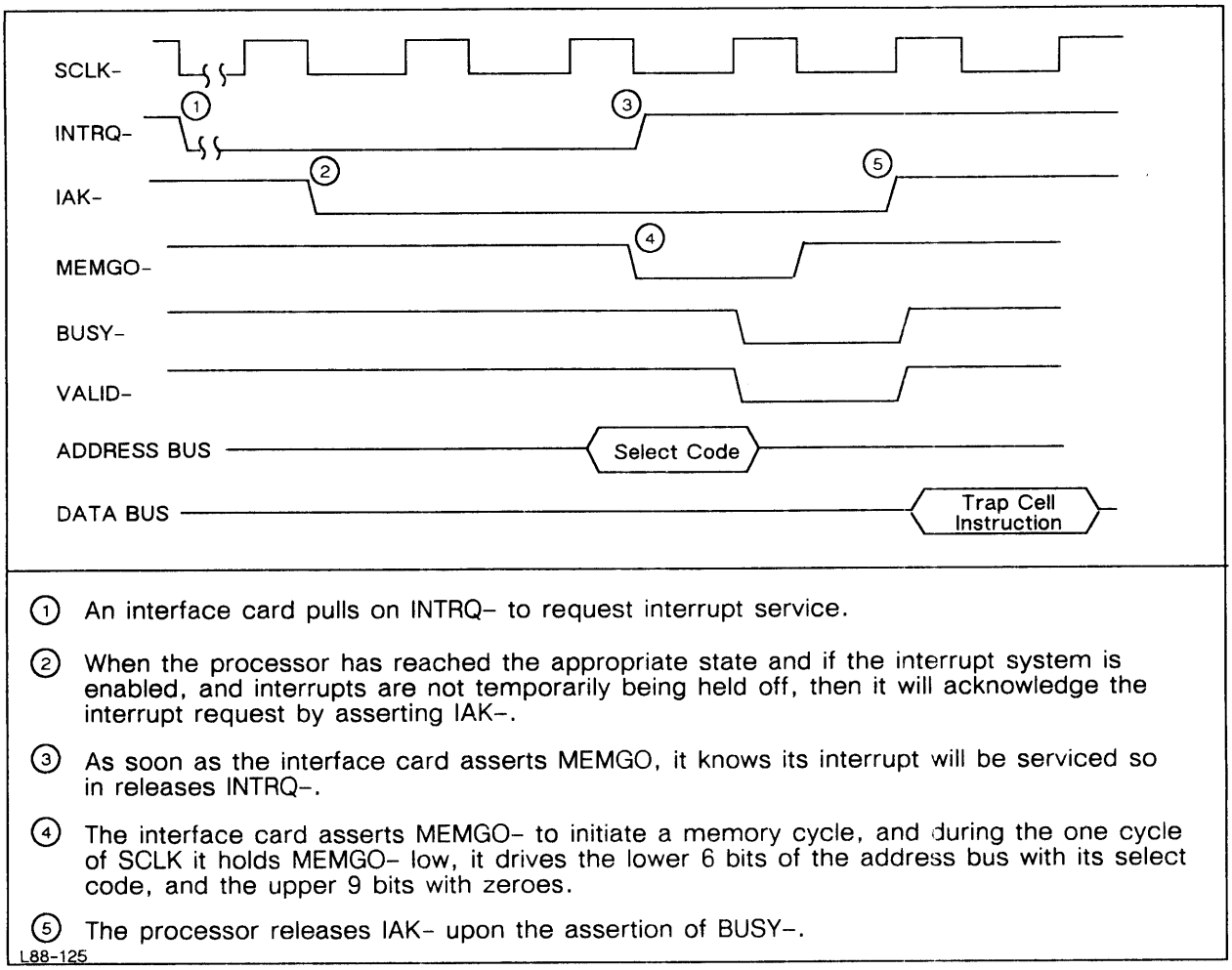
Interrupt timing is shown in Figure 7-6. An interrupt request occurs when a card's CONTROL flip-flop is set and the FLAG flip-flop gets set by either the interface itself or the execution of an STF instruction. This will cause the interface to assert the interrupt-requesting signal INTRQ- on the backplane. INTRQ- is a common signal (open collector, wired-OR) used by all interfaces to notify the processor that one of the interfaces would like an interrupt. An interrupt acknowledgment, IAK-, from the processor card, is triggered by an interrupt request from any one of the I/O interfaces. The processor asserts IAK- under the following conditions:

- the processor chip has reached the state in which it is ready to fetch the next instruction and
- the interrupt system is enabled and interrupts are not temporarily being held off and
- DMA is not occurring

Because interrupt servicing is accomplished with the help of a memory cycle, the handshake in Figure 7-5 is similar to that in Figure 7-6. Also, because interrupt servicing is transparent to the memory, neither BUSY- nor VALID- change functions from one timing diagram to the next. MEMGO- has the same function as in a normal memory cycle. During its assertion, the address bus is driven with the select code of the interface to use as the address. SELFC is also driven so that the data which is read from this location in memory is used as the next instruction executed by the processor.

This instruction will normally be a jump (JSB, I) to the location of some interrupt service routine. When an interface card asserts INTRQ-, it also pulls on ICHOD-. ICHOD- will disable all lower-priority cards from requesting interrupt service. If a high-priority card preempts the request, ICHID- will go low, disabling the requesting card. The lower-priority card should maintain its request until its ICHID- goes back up and the card can be serviced.

If any contention exists between an IAK- assertion and an MRQ- assertion, the DMA request will win. Both IAK- and MRQ- assertions may occur simultaneously on the falling edge of SCLK-, but IAK- will be deasserted prior to the next rising edge of SCLK-. The assertion of IAK will be permitted at the completion of all current DMA requests. Refer to Table 7-12 for the aborted IAK- timing specifications.



① An interface card pulls on INTRQ– to request interrupt service.

② When the processor has reached the appropriate state and if the interrupt system is enabled, and interrupts are not temporarily being held off, then it will acknowledge the interrupt request by asserting IAK–.

③ As soon as the interface card asserts MEMGO, it knows its interrupt will be serviced so in releases INTRQ–.

④ The interface card asserts MEMGO– to initiate a memory cycle, and during the one cycle of SCLK it holds MEMGO– low, it drives the lower 6 bits of the address bus with its select code, and the upper 9 bits with zeroes.

⑤ The processor releases IAK– upon the assertion of BUSY–.

L88-125

Figure 7-6. Interrupt Timing

Interrupt Latency

Interrupt latency is defined as the time from the user interrupt request to the assertion of IAK by the processor. In the best case, the interrupt can be serviced as soon as it is received, so that with the 250-nanosecond SCLK time it is 5.25 microseconds. Generally, the interrupt cannot be serviced until a DMA cycle completes or until an instruction has finished executing.

In addition, interrupts are temporarily held off for one instruction time after a JMP,I, JSB,I, or I/O instruction is executed. Therefore, worst case interrupt latency is highly dependent on the software that is running at the time of the interrupt. Assuming that no more than three channels of DMA self-configure at once, and no more than three adjacent instructions that hold off interrupts are executed back-to-back, the maximum interrupt latency is 29.75 microseconds.

Minimum	Typical	Maximum
5.25 µs	7.0 µs	30 µs

Remote Memory Access

All A-Series I/O interface cards have the capability of accessing a remote memory (that is, memory other than that plugged into the backplane). To access the remote memory, an interface card must assert REMEM– with MEMGO–. The assertion of REMEM– will signal the local memory to ignore MEMGO–. Instead, a cycle with the remote memory will be initiated. Remote memory access, however, is not supported by the A400 Computer.

Expanded Memory Access

To facilitate DMA access to expanded memory, every A-Series I/O card has a five-bit Address Extension Bus AE[0:4] (previously called SC[0:4]) that is driven onto the backplane simultaneously with the address bus during a memory access.

I/O Transfer Protocol

In the A-Series, I/O instructions are not executed by the CPU. Instead, they are decoded by the I/O interface to which they apply, then executed by that interface in conjunction with the CPU. The instruction decoding and executing capability of the interface is provided by an HP proprietary IC chip, the IOP (I/O Processor), located on each I/O interface. The I/O handshake uses the two signals IORQ–, I/O request by an interface card, and IOGO–, the "go ahead" signal from the processor.

Like processor accesses to memory, the completion of an I/O handshake is subject to DMA action on the backplane. DMA is automatically suspended for an instruction fetch but may be resumed thereafter by I/O cards unaffected by the instruction. The affected I/O card will issue an IORQ– but the processor will be unable to respond with an IOGO– until all pending DMA is completed.

I/O interface cards indicate pending DMA activity by asserting MRQ–. Both IOGO– and MRQ– are asserted on the falling edge of SCLK–. Thus the processor may come into contention with an I/O interface card if both signals occur simultaneously. The DMA activity has higher-priority than the processor so that IOGO– must be deasserted prior to the next rising edge of SCLK–. When all concurrent DMA has completed, then IOGO– may be asserted on the backplane to complete the I/O handshake.

I/O Timing Diagram

I/O Processing can be best summarized by a timing diagram. Figure 7-7 illustrates an I/O instruction being captured and executed by an I/O interface. For more information on a preempted I/O handshake and aborted IOGO–, refer to the timing specifications in Table 7-15.

I/O Instruction Execution

The I/O instructions may be broken down into three groups in terms of their execution requirements, as follows:

A. Data Transfer I/O instructions — OTA/B, LIA/B, MIA/B

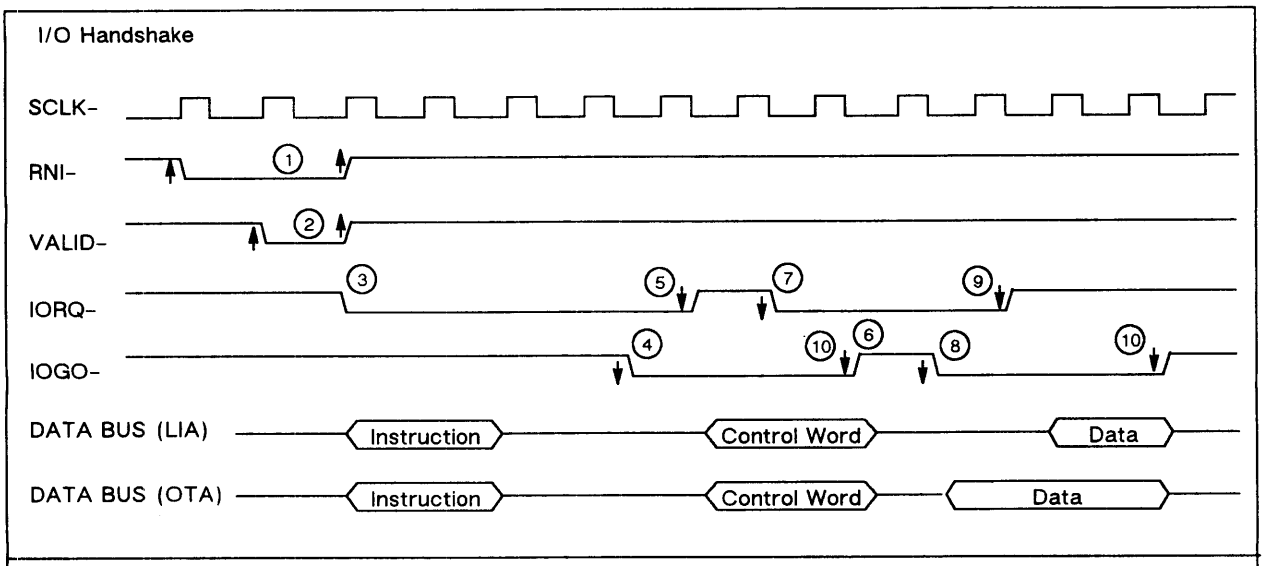
This group requires a double handshake as shown in Figure 7-7. In the first half of the handshake, a control word is transferred from the interface card to the processor. In the second half of the handshake, the data is transferred either into or out of the A- or B-Register, according to which of the six instructions above is being executed. I/O transfers over the backplane have lower priority than DMA transfers, and can be preempted. DMA transfers can occur while an I/O instruction is in the process of being executed (that is, between the two halves of the handshake).

B. Status Sensing Instructions — SFS, SFC

This group requires, at most, a single handshake during which a control word from the interface card to the processor (signaling the program counter to increment one) is transferred. If no skip is required, no handshake occurs.

C. Status Altering Instructions — STC, CLC, STF, CLF

This group requires no interaction with the CPU. The interface card executes these instructions itself, and never needs to assert IORQ–.



① Processor asserts RNI- to inform all system cards that an instruction is being fetched from memory.

② Memory asserts VALID- to inform all system cards that data on the backplane will soon be valid. Each interface should now latch the instruction off the data bus, and decode it to see if it is an I/O instruction to its select code.

③ An interface card pulls on IORQ- to signal that it recognized the I/O instruction and needs the CPU in order to execute it.

④ The processor asserts IOGO- to indicate that it is ready to receive a command from the interface card.

⑤ The interface card releases IORQ- to signal the processor that the control word will be available on the data bus on the second rising edge of SCLK-.

⑥ The processor releases IOGO- when it has clocked the command off the backplane.

⑦ The interface card reasserts IORQ- one cycle after it was released if another handshake is needed in order to transfer a data word.

⑧ The processor reasserts IOGO- in order to indicate that it is ready to receive an operand in the case of an input operation, or that data will be valid on the next falling edge in the case of an output operation.

⑨ The interface card releases IORQ- to indicate that it has latched an operand off the backplane in the case of an output operation, or that an operand will be valid on the backplane on the second rising edge in the case of an input operation.

⑩ The processor releases IOGO- to indicate that it has clocked data off the backplane in the case of an input operation, or that the handshake is complete in the case of an output operation.

L8200-148

Figure 7-7. I/O Handshake

Slave Mode Transfers

An interface card may force the processor card to enter an I/O handshake by pulling down the open-collector line SLAVE–. Once in slave mode, the interface has the capability of accessing the internal CPU registers, and does so with the use of the same handshake signals as in the I/O transfer protocol as illustrated in Figure 7-7.

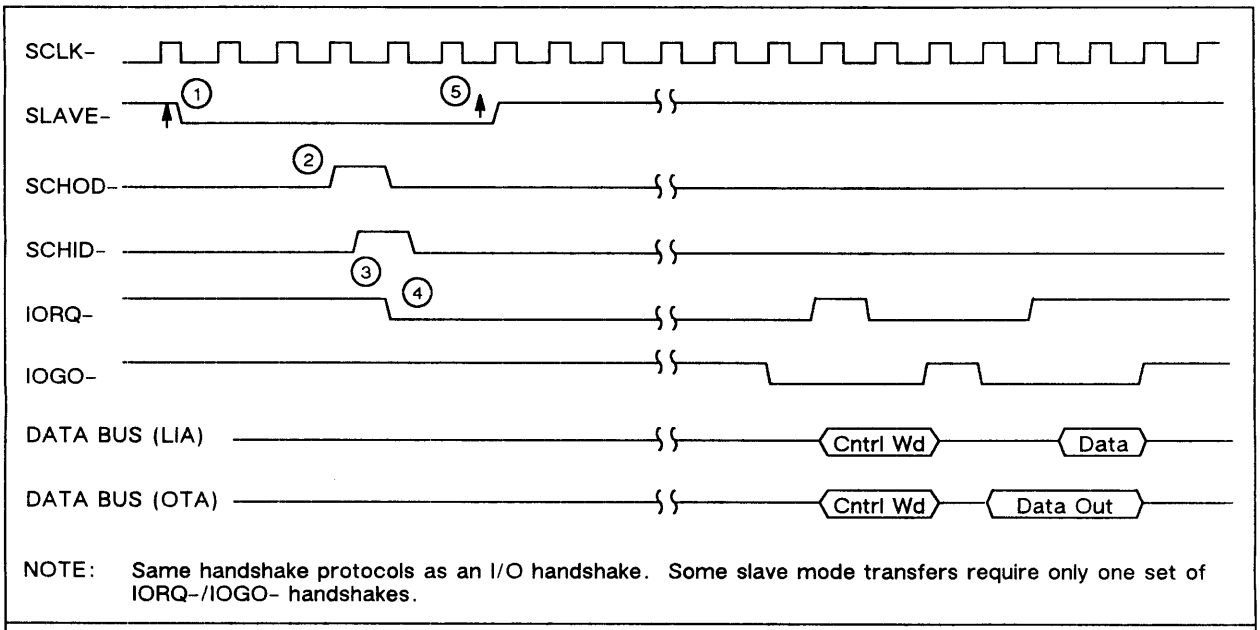
Once the slave mode has been entered, an interface card may keep the processor in that mode as long as desired by setting a bit in the control word (transferred during the first half of the handshake). This signals that another handshake (single or double) will occur. Note that the slave chain (SCHID–, SCHOD–) operates differently from the other chains in that its quiescent state is low. It is enabled only for one cycle at a time, during which the highest priority interface card pulling on SLAVE– must assert IORQ–, thereby entering slave mode. See Figure 7-8 for slave mode operation.

The control words that are sent to the CPU by an interface during an I/0 instruction (requiring a handshake) and during all slave mode processing are made up of five bits using bits 4 through 8 of the data bus. Control words for slave mode processing are defined in Table 7-5.

Table 7-5. Control Words for Slave Mode Processing

	Data Bus Bit				
	8*	7	6	5	4
NOP	X	0	0	0	0
Load Program Counter	X	0	0	0	1
Load A	X	0	0	1	0
Load B	X	0	0	1	1
Clear O	X	0	1	0	0
Set O	X	0	1	0	1
OR into A/B	X	0	1	1	0
Increment Program Counter	X	0	1	1	1
Read E and O	X	1	0	0	0
Enable ROMs	X	1	0	0	1
Read A	X	1	0	1	0
Read B	X	1	0	1	1
Clear E	X	1	1	0	0
Set E	X	1	1	0	1
Read P	X	1	1	1	0
Read and Increment P	X	1	1	1	1

* Loop for next control word if X=1; last handshake if X=0.



NOTE: Same handshake protocols as an I/O handshake. Some slave mode transfers require only one set of IORQ-/IOGO- handshakes.

① An interface card asserts SLAVE- to request the processor to enter slave mode.

② When the processor has completed executing the current instruction, it acknowledges the assertion of SLAVE- by deasserting SCHOD- for one cycle.

③ Worst case, the SCHID/SCHOD priority chain has propogated down to the lowest-priority interface card by the end of that cycle, so that the last SCHID- will go high for one cycle.

④ The interface card received the enabling signal when its SCHID- signal went high, and can now pull on IORQ- in order to initiate the I/O handshake. The rest of the I/O handshake can then proceed exactly as shown in Figure 7-7.

⑤ The interface card deasserts SLAVE- once it has asserted IORQ-.

L8200-81

Figure 7-8. Slave Mode Timing

Signal Timing Specifications

The A400 board can be divided into three sections for backplane timing: memory, processor, and I/O Master. Each of these three sections has its timing requirements for the signals it receives and its timing guarantees for the signals it generates. To ensure the basic integrity of all backplane interactions, it is necessary only to ascertain that all requirements are satisfied by the guarantees. All timing guarantees take into account the signal propagation delay due to line length and loading.

In Tables 7-6 through 7-33, timing specifications are given in terms of both requirements and guarantees. All backplane signals are listed in alphabetical order.

The definition of terms used in the timing specifications are provided below. All times are given in nanoseconds unless otherwise indicated.

Definition of terms used in timing specifications are as follows:

C = Cycle
One cycle of Slow Clock (SCLK).

f = Frequency
The number of cycles per unit time of a given signal.

I/O = I/O Master
The I/O Master consists of an I/O Processor (IOP) chip and some TTL logic which together perform all the backplane I/O interfacing functions in the A400 computer.

LHC = Long Half Cycle
The Long Half Cycle refers to the time period when SCLK- is low.

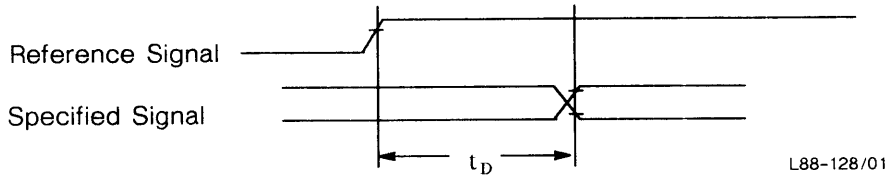
M = Memory
The A400 memory system.

P = Processor
The A400 processor.

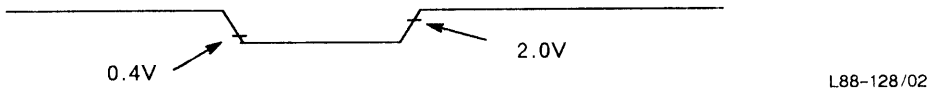
PS = Power Supply

SHC = Short Half Cycle
The Short Half Cycle is the time period when SCLK- is high.

t_D = Delay time
The time interval from a signal edge used as a reference point to the point in time when the specified signal is guaranteed to be stable on the backplane.

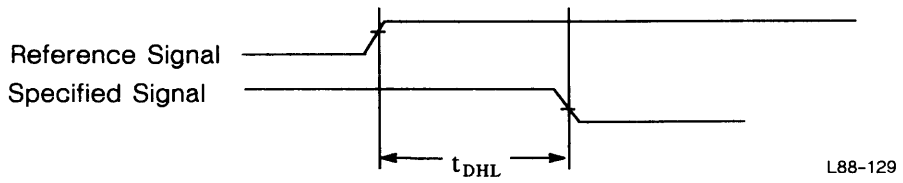


Note: In these timing diagrams, a high notch is 2.0 volts and a low notch is 0.4 volt as shown below.

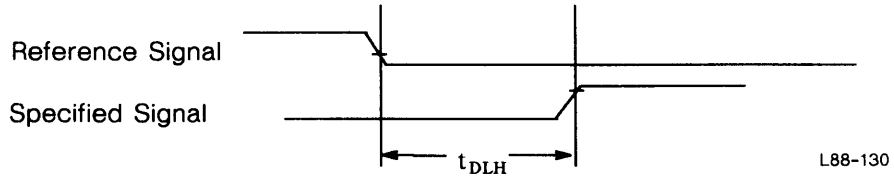


Definition of Terms Used in Timing Specifications (continued):

t_{DHL} = Delay time high to low
The time interval from a signal edge used as a reference point, to the point in time when the specified signal is guaranteed to be low if in fact it is going low.

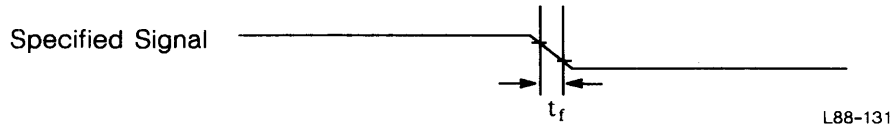


t_{DLH} = Delay time low to high
The time interval from a signal edge used as a reference time to the point in time when the specified signal is guaranteed to be high if in fact it is going high.

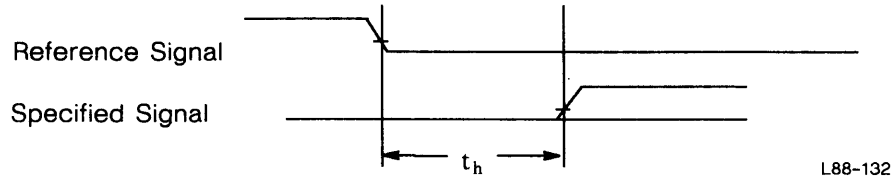


t_{DZ} = Delay time to high impedance
The time interval from a signal edge used as reference to the point in time when the specified signal will no longer be actively driven.

t_f = Fall time
The time interval during which a signal is in transition from high to low.

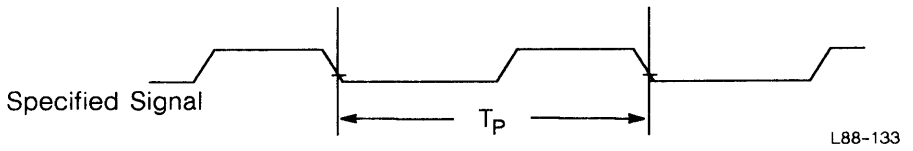


t_h = Hold time
The period of time during which a specified signal must remain stable at its logic level after a certain reference edge.

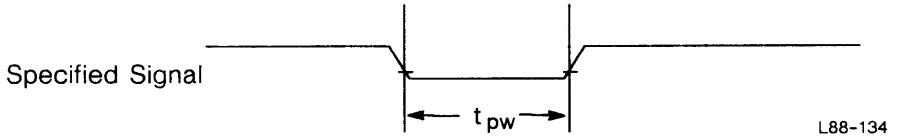


Definition of Terms Used in Timing Specifications (continued):

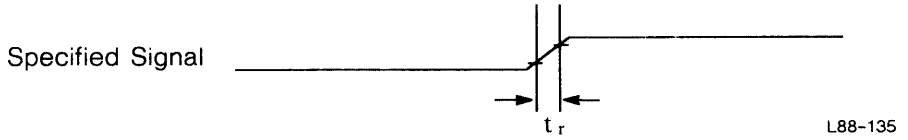
T_P = Period
The duration of one cycle of a periodic signal.



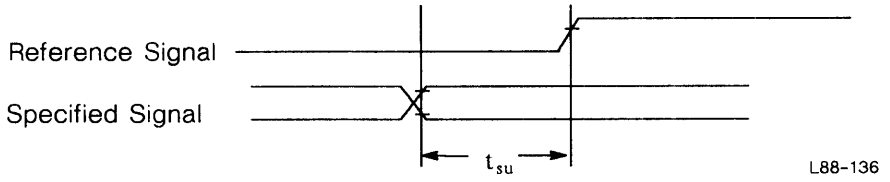
t_{pw} = Pulse width time
The time interval between the leading and trailing edge of a pulse. Specifically, for a normally high signal, t_{pw} is the time when that signal is low. For a normally low signal, t_{pw} is the time when that signal is high.



t_r = Rise time
The time interval during which a signal is in transition from low to high.

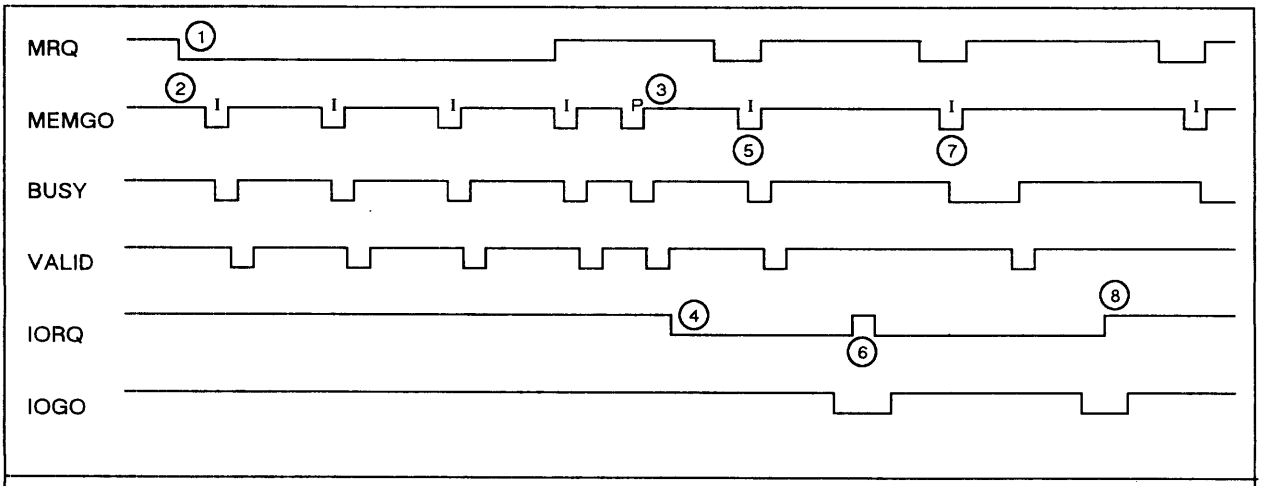


t_{su} = Set-up time
The time interval a specified signal must be at a stable logic level before a given edge of a reference signal.



Interactive Timing Examples

Previous timing examples have shown handshakes or protocols by type of interaction. During actual operation, however, transactions may start only to be preempted by other higher priority transactions and held off for an indefinite period of time. Figures 7-9 and 7-10 show various transactions over the backplane which begin, are preempted, and then later are allowed to complete.



① MRQ– is held asserted for 21C during a 4-word self-configuration.

② All assertions of MEMGO– are labeled with their source; P for Processor, I for I/O Master.

③ The processor fetches an LIA instruction.

④ The I/O Master asserts IORQ– upon recognition of the LIA, but the processor is held off from responding by ⑤ .

⑤ The first actual DMA data transfer takes place.

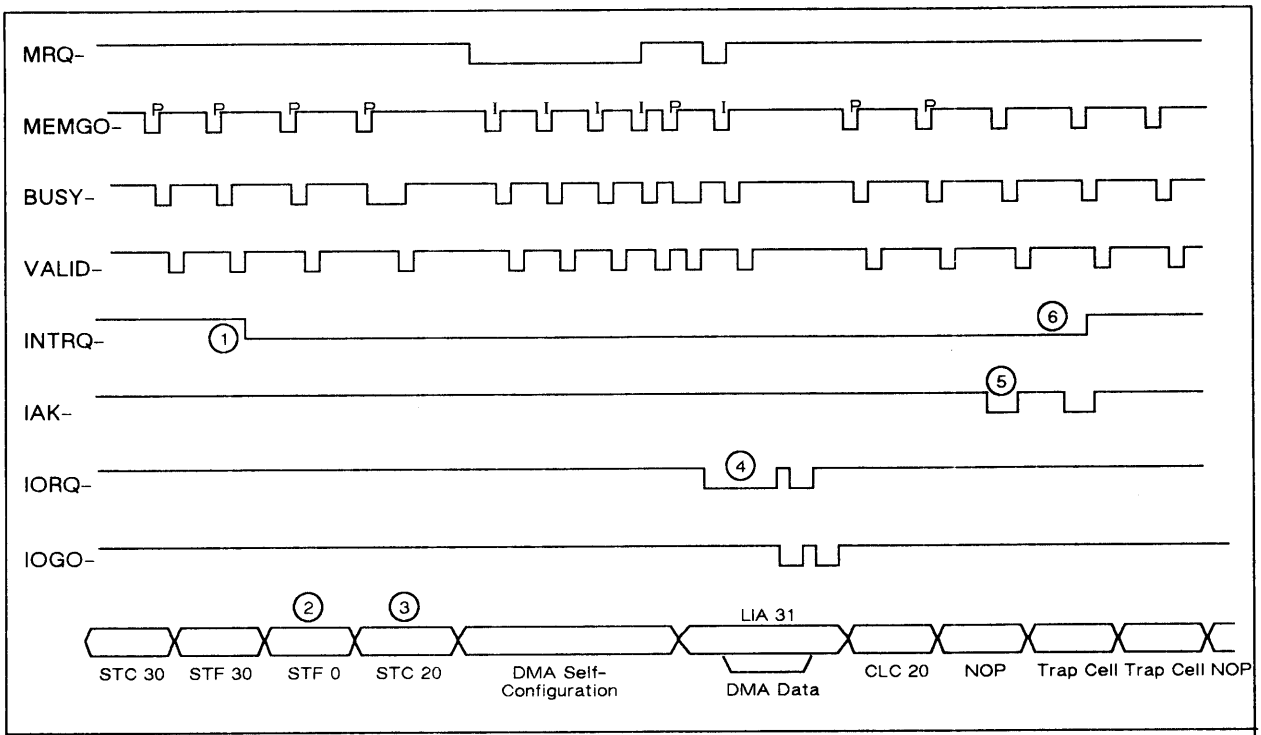
⑥ The first half of the I/O instruction handshake can now complete.

⑦ The second DMA data transfer takes place. It happened when memory was refreshing, so BUSY– is asserted for 3C (5C if it is a boot memory access) instead of the usual 2C (3C for boot memory) in order that the refresh can complete.

⑧ Now that this DMA transfer is complete, the I/O handshake can complete.

L88-126

Figure 7-9. Interactive DMA and I/O Instruction Timing



① The Flag and Control flop-flops are set so that the I/O Master attempts to interrupt.

② Interrupt system is turned on with an STF 0 but the processor must not respond until after the next instruction if the current instruction is an I/O instruction.

③ Self-configuring DMA is started, set up for a one-word transfer.

④ An LIA is executed, interleaved with DMA as in Figure 7-9.

⑤ After the NOP instruction is fetched, the processor can respond to the interrupt caused by Flag 30.

⑥ The I/O Master does not release INTRQ, because it now also has a DMA completion interrupt pending.

L8200-149

Figure 7-10. Interactive DMA, I/O Instruction, and Interrupt Timing

Table 7-6. Timing Specifications for AB[0:14]

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
t_{su}	SCLK-↑	Edges that occur during MEMGO		M	50		
t_D	SCLK-↓	Edge that causes MEMGO-↓	I/O				100
t_h	SCLK-↓	Edge that causes MEMGO-↑	I/O		0		
t_{su}	SCLK-↑	Edge that occurs during MEMGO-↓	P		60		
t_h	SCLK-↓	Edge that causes MEMGO-↑	P		20		
t_D	SCLK-↓	First edge after BUSY-↑ following MRQ-↑	P				90
t_{DZ}	MRQ-↓	CPU can be held off by MRQ- from any interfc	P		10		60
t_{DZ}	SCLK-↓	Due to MRQ-↓	P				95
t_H	SCLK-↑	Edge that causes IAK-↓	P				75

Timing Specifications for AE[0:4] (Address Extension Bus)

This bus was previously called the select code bus, SC[0:4]. Refer to Table 7-26, Timing Specifications for SC[0:4].

Table 7-7. Timing Specifications for BUSY-

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
t_{DHL}	SCLK-↑	Edge that occurs during MEMGO-	M		0		71
t_{DLH}	SCLK-↑	2C later if memory was not doing a refresh	M		0		71
t_{DLH}	SCLK-↑	3C - 5C later if memory was doing a refresh when MEMGO- occurred	M		0		71
t_{su}	SCLK-↓	In order to hold off MEMGO-		I/O	5		
t_h	SCLK-↓			I/O	5		
t_{su}	SCLK-↑	Any falling edge		P	40		
t_h	SCLK-↑	Same edge		P	-4		
t_{pw}		Longer that 1C when doing a refresh	M		1C-52	1C	3C

Table 7-8. Timing Specifications for CCLK-

Parameter	Reference	Notes	Guaranteed By	Required By	Min	Typ	Max
f	Asynchronous	To all other backplane signals	P		14.7441	14.7456 MHz	14.7471
Duty Cycle			P		30%	50%	

Table 7-9. Timing Specifications for CPUTURN-

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
t_{DHL}	SCLK-↑	That causes BUSY-↓	P				47
t_{DLH}	SCLK-↑		P				42
t_{su}	SCLK-↓	To inhibit MRQ-		I/O	25		
t_h	SCLK-↓	Same edge		I/O	-5		
t_{DHL}	RNI-↓		P				10
t_{DLH}	RNI-↑		P				10

Table 7-10. Timing Specifications for CRS–

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
t_{pw}	Asynchronous			M	1C		
t_{pw}				I/O	1C		
t_{su}	SCLK–↓			I/O	–30		
t_{DHL}	SCLK–↑	No concurrent DMA	P				35
t_{DHL}	SCLK–↑	End of DMA	P				50
t_{DLH}	Next SCLK–↑		P				35

Table 7-11. Timing Specifications for DB[0:15]

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
t_D	SCLK–↑	During MEMGO–, DMA		M			50
t_D	SCLK–↑	Processor		M			100
t_{su}	SCLK–↑	That causes VALID–↑	M		11		
t_h	SCLK–↑	That causes VALID–↑	M		97		
t_{su}, t_h	VALID–↑	All cases	M		50		
t_D	SCLK–↓	Edge that causes MEMGO–↓ (DMA)	I/O				140
t_h	SCLK–↓	Edge that causes MEMGO–↑ (DMA)	I/O		35		
t_D	SCLK–↓	First SCLK–↓ after IOGO–↓ * (I/O instruc)	I/O				315
t_h	SCLK–↑	Third SCLK–↑ during IOGO– (I/O instruction)	I/O		65		
t_{su}	VALID–↑	DMA read		I/O	50		
t_h	VALID–↑	DMA read		I/O	50		180
t_{su}	SCLK–↓	Second SCLK–↓ * during IOGO– (I/O instruction)		I/O	10		

* Provided IOGO–↓ met 10-nanosecond set-up time to previous SCLK–↑.

Table 7-11. Timing Specifications for DB[0:15] (continued)

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
t_h	SCLK-↑	Third SCLK-↑ * during IOGO- (I/O instruction)		I/O	40		227
t_{su}	SCLK-↑	Edge that causes VALID-↑ (memory read)		P	11		
t_h	SCLK-↑	Same edge (memory read)		P	9		
t_{su}	SCLK-↑	Second SCLK-↑ after SCLK-↓ which causes IORQ-↑ (I/O instruction)		P	11		
t_h	SCLK-↑	Same edge (I/O instr)		P	9		
t_D	SCLK-↑	Edge that causes MEMGO-↓ (memory write)	P				210
t_h	SCLK-↓	Edge that causes MEMGO-↑ (memory write)	P		190		
t_D	SCLK-↑	Edge that precedes SCLK-↓ which causes IOGO-↓ (I/O write)	P		30		180
t_h	SCLK-↑	Edge that precedes SCLK-↓ which causes IOGO-↑ (I/O write)	P		90		

* Provided IOGO-↓ met 10-nanosecond set-up time to previous SCLK-↑.

Timing Specifications for FETCH-

The timing specifications for FETCH- are the same as for RNI-, refer to Table 7-25, Timing Specifications for RNI- and FETCH-.

Table 7-12. Timing Specifications for IAK–

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
t_{su}	SCLK–↑			I/O	10		
t_h	SCLK–↑	Same edge		I/O	25		
t_{pw}				I/O	2C		3C
t_{su}	SCLK–↓	To inhibit MRQ		I/O	25		
t_h	SCLK–↓	Same edge		I/O	0		
t_D	SCLK–↑		P				50
t_h	SCLK–↑	First edge after VALID–↓	P		8		

Table 7-13. Timing Specifications for ICHID–/ICHOD–

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
ICHID– t_{su}	SCLK–↓	Second SCLK–↓ * during IAK–		I/O	10		
ICHID– t_h	SCLK–↓	Third SCLK–↓ * during IAK–		I/O	50		
t_D	Asynchronous	ICHID–↓ to ICHOD–↓	I/O			5	7.5
ICHOD– t_{DHL}	SCLK–↑	Edge that causes INTRQ–↓	I/O				200
ICHOD– t_h	IAK–↑	ICHOD– is held low during the entire assertion of IAK–	I/O		SHC		

Table 7-14. Timing Specifications for INTRQ–

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
t_{DHL}	SCLK–↓		I/O				200
t_{DLH}	SCLK–↓	Third SCLK– after IAK–↓ *	I/O				300
t_{su}	SCLK–↓			P	15		
t_h	IAK–↓			P	0		
* Provided IAK– met the 10-nanosecond set-up time to previous SCLK–↑.							

Table 7-15. Timing Specifications for IOGO–

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
t_{su}	SCLK–↑	During IORQ–		I/O	10		
t_h	SCLK–↑	Same edge		I/O	25		
t_{pw}		Third rising edge of SCLK–		I/O	2C+LHC		
t_{su}	SCLK–↓	To inhibit MRQ–		I/O	25		
t_h	SCLK–↓	Same edge		I/O	0		
t_{DHL}	SCLK–↓		P				63
t_{DLH}	SCLK–↓	Second SCLK–↓ after the SCLK–↓ that caused IORQ–↑	P				40
t_{DHL}	SCLK–↓	Second edge after BUSY–↑ following MRQ–↑	P				50
t_{DLH}	MRQ–↓		P				90
t_{DLH}	SCLK–↓	Due to MRQ–↓	P				85

Table 7-16. Timing Specifications for IORQ–

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
t_{DHL1}	Data bus valid during VALID– *	1 refers to first handshake request after RNI–↓	I/O				325
t_{DHL2}	SCLK–↓	2 refers to second ** SCLK–↓ after IOGO–↓ (double handshake only)	I/O				145
t_{DHL3}	SCLK–↑	SCLK–↑ following SCHID–↑ (3 refers to initial IORQ–↓ on slave cycle)	I/O				45
t_{DLH}	SCLK–↓	First SCLK–↓ after ** IOGO–↓	I/O				210
t_{su}	SCLK–↓	5C+SHC after SCLK–↑ which causes RNI–↑ or VALID–↑		P	20		
t_h	SCLK–↓	Same edge		P	15		
t_{su}	SCLK–↓	1 cycle after edge which caused second assertion of IORQ–		P	20		
t_h	SCLK–↓	Same edge		P	15		
t_{su}	SCLK–↓	Following any release of IORQ–		P	20		
t_h	SCLK–↓	Same edge		P	15		
t_{su}	SCLK–↓	First SCLK–↓ after SCHOD–↓		P	20		
t_h	SCLK–↓	Same edge		P	15		

* During VALID–, there could be false assertions of IORQ– due to the data bus being in transition. This will not affect system operation, however, because the processor does not check IORQ– until two states after RNI–↑ when IORQ– is guaranteed to be valid.

** Provided IOGO–↓ met the 10-nanosecond set-up time to previous SCLK–↑.

Table 7-17. Timing Specifications for MCHID-/MCHOD-, MCHODOC-

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
MCHID- t_{su}	SCLK-↓			I/O	5		
MCHID- t_h	SCLK-↓	Same edge		I/O	20		
t_{DHL}		MCHID-↓ to MCHOD-↓	I/O			5	7
MCHOD- t_{DHL}	SCLK-↓	Edge that causes MRQ-↓	I/O				30
MCHODOC- t_{DHL}	SCLK-↓	Edge that causes MRQ-↓	I/O				55
MCHODOC- t_{DLH}	SCLK-↓	Edge that causes MRQ-↑	I/O				165

Table 7-18. Timing Specifications for MEMGO-

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
t_{su}	SCLK-↑	For DMA MEMGO-, processor MEMGO- is for reference only		M	45		
t_h	SCLK-↑	Same edge		M	SHC		215
t_{DHL}	SCLK-↓		I/O				45
t_{DLH}	SCLK-↓	Next edge	I/O		30		110
t_{DHL}	SCLK-↓		P				121
t_{DHL}	SCLK-↑	Following an I/O handshake	P				130
t_{DLH}	SCLK-↓	First SCLK-↓ after BUSY-↓	P				124
t_{DHL}	SCLK-↓	First edge after BUSY-↑ following MRQ-↑	P				95
t_{DLH}	MRQ-↓		P				77
t_{DLH}	SCLK-↓	MEMGO- aborted by MRQ- from edge which caused MEMGO-	P				127

Table 7-19. Timing Specifications for MLOST–

Parameter	Reference	Notes	Guaranteed By	Required By	Time Min	Time Typ	Time Max
t_r, t_f			BB				50 ns
t_{su}	PON+↑		BB		500 µs		
t_h	PON+↑		BB		10 ms		1 s
t_h	PON+↑		SW*		5 ms		

* The processor does not latch MLOST–. During the pretest, the state of this line is used by the software to determine whether or not to initialize memory.

Table 7-20. Timing Specifications for MP+

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Time in ns Typ	Time in ns Max
t_{su}	VALID–↑			I/O	0		
t_h	SCLK–↑	Second SCLK–↑ after VALID–↑ (non-I/O instr). Second SCLK–↑ after last IOGO–↑ (I/O instr)		I/O	0		
t_D	SCLK–↑		P				69

Table 7-21. Timing Specifications for MRQ–

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Time in ns Typ	Time in ns Max
t_{DHL}	SCLK–↓		I/O				50
t_{DLH}	SCLK–↓	Edge that causes MEMGO–↑	I/O		30		110
t_{su}	SCLK–↑			P	85		
t_h	SCLK–↑	Edge that causes BUSY–↓		P	50		
t_{su}	SCLK–↑	Edge that occurs during the processor MEMGO–		M	51		
t_h	SCLK–↑	Edge that occurs during MEMGO–		M	45		

Table 7-22. Timing Specifications for PE–

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
t_{pw}	Asynchronous	1 cycle = 250 ns	M		50		
t_{DHL}	VALID–↑		M		–4		36
t_{pw}		Must occur during window		I/O	50		
t_{su}	Start window SCLK–↓	First edge after edge that causes RNI–↓ (instr fetch window)		I/O	0		
t_h	End window SCLK–↑	First edge after VALID–↑ (instr fetch window)		I/O	0		
t_{su}	Start window SCLK–↓	First edge after edge that causes VALID–↓ (DMA window)		I/O	0		
t_h	End window SCLK–↓	Second edge after edge that causes VALID–↑ (DMA window)		I/O	0		
t_{su}	SCLK–↓	First edge after VALID–↑		P	20		
t_{su}	End window SCLK–↓	First edge after VALID–↑		P	0		

Table 7-23. Timing Specifications for PFW–

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
t_{su}	PON+↓		PS		5 ms		
t_{su}	PON+↑		PS		10 ms		
t_r, t_f			PS				50
t_{su}	PON+↑			P	50		
t_{su}	PON+↓	Software requires time for power down routine to execute		SW	5 ms		

Table 7-24. Timing Specifications for PON+

Parameter	Reference	Notes	Guaranteed By	Required By	Time Min	Time Typ	Time Max
t_D		Supplies up and within regulation	PS		50	65	100 ms
t_r, t_f			PS				50 ms
t_{pw}		Time required to fully initialize the CPU chip		P	1C+30 ns		

Table 7-25. Timing Specifications for PS–

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Time in ns Typ	Time in ns Max
All		Same as data bus requirements for all memory writes		M			
t_D	SCLK–↑		P		0		20

Table 7-26. Timing Specifications for RNI–, FETCH–

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Time in ns Typ	Time in ns Max
t_{su}	SCLK–↓	Edge that occurs during VALID–		I/O	25		
t_h	SCLK–↓	Same edge		I/O	30		
t_{DHL}	SCLK–↑	First edge after MEMGO–↓ from CPU	P				47
t_{DLH}	SCLK–↑	Edge that causes VALID–↑	P				42
t_{pw}			P			1C	
t_{pw}				I/O	1C–t_{su}	1C	

Table 7-27. Timing Specifications for SC[0:4] (AE[0:4])

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
t_D	SCLK-↓	Edge that causes MEMGO-↓	I/O				90
t_h	SCLK-↓	Edge that causes MEMGO-↑	I/O		20		
t_{su}	SCLK-↑	Edge that occurs during MEMGO-		M	40		
t_h	SCLK-↑	Edge that occurs during MEMGO-		M	62		
t_{su}	SCLK-↑	Edge that occurs during MEMGO-↓	P		60		
t_h	SCLK-↓	Edge that causes MEMGO-↑	P		20		
t_D	SCLK-↓	First after BUSY-↑ following MRQ-↑	P				90
t_{DZ}	MRQ-↓	CPU can be held off by MRQ- from any interfc	P		10		45
t_{DZ}	SCLK-↓	Due to MRQ-↓	P				95
t_h	SCLK-↑	Edge that causes IAK-↓	P				75

Table 7-28. Timing Specifications for SCHID-/SCHOD-

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
t_D		SCHID-↓ to SCHOD-↓	I/O			5	7.5
SCHOD- t_{DHL}*	SCLK-↑	Edge that caused SCHID-↑	I/O				25
SCHID- t_{su}	SCLK-↑			I/O	0		
SCHID- t_h	SCLK-↑	Same edge		I/O	15		
t_{DLH}	SCLK-↑		P				50
t_{DHL}	SCLK-↑	Next edge	P				50

* If a low priority interface asserts SLAVE-, a higher priority interface can get the slave cycle if the higher priority interface lowers SCHOD- at any time up until 1C - 169 ns after the SCLK- which caused SCHID-.

Table 7-29. Timing Specifications for SCLK–

Parameter	Notes	Guaranteed By	Required By	Time Min	Time Typ	Time Max
f		P		–0.005%	4.40 (MHz)	+0.005%
T_P			I/O	227 ns		
t_{pw}	LHC		I/O	135 ns		
t_{pw}	SHC		I/O	90 ns		

Table 7-30. Timing Specifications for SELFC

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
t_{DHL}	SCLK–↓	Edge that causes MEMGO–↓	I/O				80
t_h	SCLK–↓	Edge that causes MEMGO–↑	I/O		40		180
t_{su}	SCLK–↑	Edge that occurs during MEMGO–		M	50		
t_h	SCLK–↑	Edge that occurs during MEMGO–		M	100		
t_{su}	SCLK–↑	Edge that occurs during MEMGO–↓	P		53		
t_h	SCLK–↓	Edge that causes MEMGO–↑	P		20		
t_D	SCLK–↓	First after BUSY–↑ following MRQ–↑	P				90
t_{DZ}	MRQ–↓	CPU can be held off by MRQ– from any interfc	P		10		45
t_{DZ}	SCLK–↓	Due to MRQ–↓	P				95
t_h	SCLK–↑	Edge that causes IAK–↓	P				75

Table 7-31. Timing Specifications for SLAVE-

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
t_{DHL}	SCLK-↑		I/O				45
t_{DLH}	SCLK-↑	First edge after SCHID-↓	I/O				130
t_{su}	SCLK-↓			P	0		
t_h	SCLK-↑	Edge that causes SCHOD-↑		P	0		

Table 7-32. Timing Specifications for VALID-

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
t_{DHL}	SCLK-↑	First SCLK-↑ before BUSY-↓, no refresh. Second to fourth SCLK-↑ after BUSY-↓ with refresh.	M		38		67
t_{DLH}	SCLK-↑	Second SCLK-↑ after BUSY-↓, no refresh. Third to fifth SCLK-↑ with refresh.	M		39		66
t_{su}	SCLK-↓			I/O	10		
t_h	SCLK-↓	Same edge		I/O	30		
t_{su}	SCLK-↑			P	60		
t_h	SCLK-↑	Same edge		P	-10		
t_{pw}				I/O	1C-t_{su}	1C	

Table 7-33. Timing Specifications for WE-

Parameter	Reference	Notes	Guaranteed By	Required By	Time in ns Min	Typ	Max
t_{su}	SCLK-↑	Edge that occurs during MEMGO-		M	20		
t_h	SCLK-↑	Same edge		M	SHC		
t_D	SCLK-↓	Edge that causes MEMGO-↓	I/O				100
t_h	SCLK-↓	Edge that causes MEMGO-↑	I/O		20		
t_D	SCLK-↓	Edge that causes MEMGO-↓	P				100
t_h	SCLK-↓	Edge that causes MEMGO-↑	P		20		
t_D	SCLK-↓	First after BUSY-↑ following MRQ-↑	P				90
t_{DZ}	MRQ-↓		P		10		45
t_{DZ}	SCLK-↓	Due to MRQ-↓	P				95
t_h	SCLK-↑	Edge that causes IAK-↓	P				75

Signal Definitions

Table 7-34 lists all of the backplane signals. The signals are listed in alphabetical order, along with their definitions, where they originated, where they go, functions, and general timing specifications. Timing values, when given, are nominal. For specific timing values, see Tables 7-6 through 7-33.

Table 7-34. Backplane Signal Definitions

AB[0:14]

Full Name: Address Bus bits 0 through 14 (Tri-state, high true)

Driven By: The processor card or the I/O Master during a DMA transfer or while receiving interrupt service. (In the case of interrupt service, the card drives AB[0:5] with its select code and AB[6:14] with zeroes.)

Received By: Memory and the processor.

Function: The address bus is used to transfer a 15-bit absolute address to the memory, of which AB[0] is the least significant bit. The processor will latch the address in case a parity error or memory protect violation occurs. (It will not check for these during DMA.)

Timing: The address bus is driven with the assertion of MEMGO- during a DMA transfer and during an interrupt cycle. In addition, the processor drives the address bus and asserts MEMGO when accessing the boot ROM.

NOTE: The default address bus driver is the processor card, which drives the address bus at all times except the following:

a. During the assertion of IAK-.

b. During the assertion of MRQ-.

c. From the first SCLK-↓ after the assertion of BUSY- until the first SCLK- ↓ after the release of BUSY-.

AE[0:4]

Full Name: Address Extension Bus. This bus was previously called the SC (Select Code) Bus. Refer to SC[0:4] for signal definition.

BUSY-

Full Name: Memory Busy (Tri-state, low true)

Driven By: The memory controller on the A400 board.

Received By: The processor and interface cards.

Function: BUSY- is asserted by the memory controller to indicate that it is unable to begin a new cycle.

Timing: BUSY- is asserted after the rising edge of SCLK-, following the assertion of MEMGO-. BUSY- is released following the rising edge of SCLK- during the assertion of VALID-.

L88-127/01

Table 7-34. Backplane Signal Definitions (continued)

CCLK-

Full Name:	Communications Clock (low true)
Driven By:	The processor
Received By:	Interface Cards
Function:	This clock provides a fixed frequency which may be used to drive a state machine, or which may be divided down for baud rate generation.
Timing:	14.7456 MHz clock with a 50 percent duty cycle.

CPUTURN-

Full Name:	Processor Turn
Driven By:	The processor
Received By:	All interface cards
Function:	Asserted during RNI- and in addition, in order to signal that the processor requests backplane priority. The assertion of CPUTURN- inhibits all interfaces from reasserting MRQ- once all current requests are satisfied.
Timing:	When the processor wants to get on the backplane for any one of three reasons (accessing memory, acknowledging an interrupt, or participating in an I/O handshake) but is held off by DMA, a counter counts 32 MEMGOs before asserting CPUTURN. CPUTURN stays asserted until the processor starts its transaction on the backplane.

CRS-

Full Name:	Control Reset (low true)
Driven By:	The processor
Received By:	All cards
Function:	The assertion of CRS- completely resets the I/O system. All of the following will occur: 1. All interface control flip-flops will be cleared. 2. All interface flag flip-flops will be cleared. 3. All pending I/O interrupts will be cleared except power fail. 4. The global register will be disabled. 5. Parity valid LED on memory card will be turned on. In addition, each I/O interface interprets CRS- to perform its own various test functions.
Timing:	CRS- is asserted for one cycle of SCLK- when a CLC 0 instruction is executed.

L88-127/02

Table 7-34. Backplane Signal Definitions (continued)

DB[0:15]+

Full Name:	Data Bus bits 0 through 15 (Tri-state, high true)
Driven By:	Any memory or I/O interface or the processor.
Received By:	Any memory or I/O interface or the processor.
Function:	DB[0:15], of which DB[0]+ is the least significant bit, are used for all system data transfers.
Timing:	An I/O interface drives the data bus during the assertion of MEMGO- on a DMA write. The RAM card drives the data bus on a read cycle for one cycle, during the assertion of VALID-. The processor drives the data bus with the assertion of MEMGO- on a memory write (STA), with IOGO- on an I/O write (OTA), and with VALID- clocked by the start of the long half-cycle on an A or B fetch or a Boot read.

FCLK-

Full Name:	Fast Clock
Driven By:	The processor
Received By:	Memory
Function:	FCLK- is exactly five times the frequency of SCLK- and is used by the processor to generate SCLK-.
Timing:	FLCK- is a 50 percent duty cycle clock with a maximum frequency of 20.0 MHz. FCLK- is in synchronization with SCLK- such that a positive edge of FCLK- accompanies every transition of SCLK-.

NOTE: FCLK- is not driven onto the backplane by the A400 board as it is in the other A-Series processors.

FETCH-

Full Name:	Fetch
Driven By:	The processor
Received By:	Logical analysis interface (not supplied by HP)
Function:	Asserted to indicate that the present memory reference is an instruction fetch.
Timing:	Same as RNI-.

L88-127/03

Table 7-34. Backplane Signal Definitions (continued)

IAK–	
Full Name:	Interrupt Acknowledge (low true)
Driven By:	The processor
Received By:	Any interrupting I/O interface
Function:	Asserted to signal that an interrupt request is about to be serviced and to freeze the interrupt priority chain.
Timing:	IAK– is asserted by the processor following the start of the short half cycle of SCLK–. It is held until after the trap cell instruction has commenced. (BUSY–↓ causes IAK–↑.)
ICHID–	
Full Name:	Interrupt Chain In Disable (low true)
Driven By:	The next higher priority I/O interface, to whom this signal is ICHOD–.
Received By:	All I/O interface cards.
Function:	See description for ICHOD–.
Timing:	See description for ICHOD–.
ICHOD–	
Full Name:	Interrupt Chain Out Disable (low true)
Driven By:	All I/O interfaces, and the processor (which is the top of the chain).
Received By:	The next lower priority I/O interface, to whom this signal is ICHID–.
Function:	Asserted to disable lower priority cards from interrupting. A high on this line keeps interrupt generation enabled. ICHOD– is part of the ICHID–/ICHOD– daisy chain, used to determine interrupt priority.
Timing:	Asserted by an I/O interface when its ICHID– line goes low, or when its Flag and Control flip-flops get set. Deasserted when ICHID– goes high, and on either a CLF, CLC, or PON+. ICHOD– is tied high on the A400 board and is passed to the on-board I/O Master.

L88-127/04

Table 7-34. Backplane Signal Definitions (continued)

INTRQ– Full Name: Interrupt Request (open-collector, low true) Driven By: All I/O interfaces Received By: The processor Function: Asserted to signal an interrupt request, and held low until the interrupt gets service, until PON+ goes low, or until a CLC 0 is executed. Timing: Asserted by an I/O interface when both its Control and Flag flip-flops are set and its ICHID– signal is high. Deasserted when the Control or Flag flip-flop is cleared, or 2 cycles after the assertion of IAK– while ICHID– is high.
IOGO– Full Name: I/O Handshake Request Acknowledge (low true) Driven By: The processor Received By: All I/O interfaces. Function: Asserted to signal that the processor is ready to receive a command or send or receive an operand from an interface. Deasserted when the transfer has been completed. Timing: Pulled low when the data bus is available for transfers and released as soon as the data has been clocked off of the backplane. NOTE: For some types of I/O transfers, this signal will participate in a double handshake (see Figure 5-6).
IORQ– Full Name: I/O Handshake Request (open collector, low true) Driven By: All I/O interfaces Received By: The processor Function: Asserted to signal that an interface requires processor service, and deasserted when being serviced. Timing: Asserted within 2 cycles after the rising edge of RNI–, or in slave mode (refer to the Slave Mode Transfers section in this chapter) on the next rising edge of SCLK– after SCHID– goes high. Deasserted to signal that data will be valid on the second rising edge of SCLK–, or during an input, to signal that data has just been latched. Refer to the I/O Transfer Protocol section in this chapter. NOTE: For some types of I/O transfers, this signal will participate in a double handshake (see Figure 5-6). L88-127/05

Table 7-34. Backplane Signal Definitions (continued)

MCHID–

Full Name: Memory Chain In Disable (low true)

Driven By: The next higher priority I/O interface, to whom this signal is MCHOD–.

Received By: All I/O interfaces

Function: Asserted to disable initiation of a memory cycle.

Timing: MCHID– is asserted a maximum of one cycle after MRQ– goes low. Released as soon as memory cycle of higher priority device is complete.

MCHOD–

Full Name: Memory Chain Out Disable (low true)

Driven By: All I/O interfaces and the processor

Received By: The next lower priority I/O interface, to whom this signal is MCHID–.

Function: Asserted to disable all lower priority interface cards from initiating a memory cycle.

Timing: An I/O interface wanting a DMA cycle asserts MCHOD– at the end of the short half cycle of SCLK–. MCHOD– is deasserted at the end of the short half cycle, following the assertion of BUSY–. The processor is the top of this priority chain. MCHOD– is tied high on the processor and passed to the on-board I/O Master.

NOTE: For some types of I/O transfers, this signal will participate in a double handshake (see Figure 5-6).

MCHODOC–

Full Name: Memory Chain Out Disable Open Collector (open collector, low true)

Driven By: All I/O interfaces

Received By: The head of the priority chain on the lower priority stack.

Function: Used as look-ahead for the memory priority chain. If any I/O interface in the higher priority stack asserts MCHODOC–, all interfaces in the lower priority stack will become disabled from initiating a memory cycle.

Timing: An I/O interface wanting a DMA cycle asserts MCHODOC– at the end of the short half cycle of SCLK–. MCHODOC– is released at the end of the short half cycle, following the assertion of BUSY–.

NOTE: As far as the output of any given interface is concerned, MCHODOC– is logically identical to MCHOD–.

The pull-up resistor on this line is located on the 16-slot backplane. The 6-slot backplane configuration is not large enough to require look-ahead in the memory priority chain, so this line is not terminated in this smaller configuration.

L88-127/06

Table 7-34. Backplane Signal Definitions (continued)

MEMGO–	
Full Name:	Memory Cycle Initiation (open collector, low true)
Driven By:	The processor and I/O interfaces
Received By:	Memory
Function:	Pulled low to signal a memory request and released once service begins.
Timing:	MEMGO– may be asserted by the card wanting to initiate a memory cycle after the falling edge of SCLK– that follows the release of BUSY–. MEMGO– is released after the assertion of BUSY–. MEMGO– is released by an interface or the processor after being held low for one cycle of SCLK–.
MLOST–	
Full Name:	Memory Lost (open collector, low true)
Driven By:	The processor, memory, and battery back-up card.
Received By:	The processor and memory controller
Function:	MLOST– is asserted by the optional battery in the power supply (or the battery backup card) to indicate that memory power was lost when system power last went down. Memory will be cleared on the next power up. Where there is no battery backup for memory, MLOST– can be grounded. Do this by setting the U1601 switch 8 closed which grounds MLOST–.
Timing:	Asserted as soon as memory power fails. Released 10 ms after the rising edge of PON+.
MP+	
Full Name:	Memory Protect (open collector, high true)
Driven By:	The processor
Received By:	All I/O interfaces and the memory controller
Function:	MP+ is asserted to indicate that the memory protect system is on. When MP+ is high, all I/O interfaces are inhibited from recognizing I/O instructions. DMA is not affected. Enables memory system protection.
Timing:	MP+ is asserted after an STC 05 instruction. It is released when IAK– is asserted, but reasserted if an I/O group instruction is in the trap cell. MP+ is always in the proper state before RNI– is asserted and does not change until the next instruction fetch is initiated.

L88-127/07

Table 7-34. Backplane Signal Definitions (continued)

MRQ-

Full Name:	Memory Request (open collector, low true)
Driven By:	All I/O interfaces
Received By:	The processor and the memory controller
Function:	Asserted to indicate that an interface performing DMA has requested a memory cycle. When MRQ- is low, the processor is inhibited from requesting a memory cycle.
Timing:	An I/O interface wanting a DMA cycle asserts MRQ- at the start of the long half cycle of SCLK-. MRQ- is deasserted on the falling edge of SCLK- after the assertion of BUSY-.

PE-

Full Name:	Parity Error (open collector)
Driven By:	The memory controller
Received By:	The processor and I/O interfaces
Function:	Asserted if the last memory read produced a parity error.
Timing:	PE- is asserted during the short half cycle after release of VALID-.

PFW-

Full Name:	Power Fail Warning (open collector, low true)
Driven By:	The power supply
Received By:	The processor
Function:	Asserted to signal an AC line voltage failure.
Timing:	Asserted at least 5 ms before the fall of PON+. Released before the rise of PON+.

NOTE: The pull-up resistor on this open collector line is located on the A400 board.

L88-127/08

Table 7-34. Backplane Signal Definitions (continued)

PON+

Full Name: Power On (open collector, high true)

Driven By: The power supply and the processor

Received By: All cards in the system

Function: PON+ is asserted by the power supply shortly after all power supply voltages are stable, to allow time for initialization on individual system cards.

Timing: Asserted 10 ms after all power supplies are stable. Deasserted if any supply falls below a tolerable level.

PS-

Full Name: Parity Sense

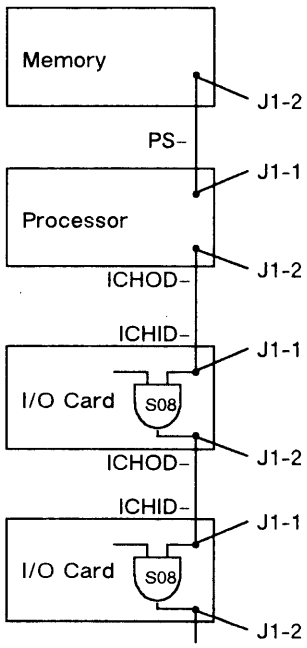
Driven By: The processor

Received By: The memory controller

Function: A high level on PS- causes memory to generate and detect odd parity. A low on PS- causes memory to generate and detect even parity.

Timing: The level of PS- is selected by flag 5. An STF 5 selects even parity and a CLF 5 selects odd parity.

NOTE: On power up, PS- is set for odd parity. Also note that PS- is not bussed up and down the backplane. Instead, it is sent by the A400 board only to the memory card located above it. See the figure below.



L88-127/09

Table 7-34. Backplane Signal Definitions (continued)

RNI–

Full Name: Read Next Instruction (low true)

Driven By: The processor

Received By: All I/O interfaces

Function: RNI– is asserted to indicate that the current memory cycle is a fetch and that an instruction will be on the data bus.

Timing: RNI– is asserted with the fetch address for I/O instructions. It is released after the start of the short half cycle of SCLK– after VALID– is asserted.

NOTE: The instruction is to be latched on the trailing (rising) edge of RNI–.

SC[0:4] (or AE[0:4])

Full Name: Address Extension Bus, bits 0 through 4

Driven By: I/O interfaces and the processor

Received By: The memory controller

Function: The SC-bus is used to select one of 32 map sets.

Timing: The SC-bus is driven simultaneously with AB[0:14].

SCHID–

Full Name: Slave Chain In Disable (low true)

Driven By: The next higher priority card, to whom this signal is SCHOD–

Received By: All I/O interfaces

Function: See SCHOD–

Timing: See SCHOD–

L88-127/10

Table 7-34. Backplane Signal Definitions (continued)

SCHOD-

Full Name: Slave Chain Out Disable (low true)

Driven By: All I/O interfaces

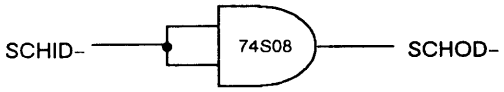
Received By: The next lower priority card, to whom this signal is SCHID-

Function: SCHOD- is asserted to disable lower priority cards from entering slave mode. SCHOD- is part of the SCHID-/SCHOD- priority chain, used to settle conflicts for slave mode processing.

Timing: SCHOD- is asserted with SLAVE-, or if a higher priority card pulls on SCHID-, and is held as long thereafter as it takes the daisy chain to ripple down. Likewise, SCHOD- is released with SLAVE- or SCHID-.

NOTE: The top of the priority chain is the processor and on-board I/O. Whenever SLAVE- is asserted by an I/O card, the processor has completed executing the current instruction, and the on-board I/O did not assert SLAVE-, SCHOD- is driven high for one cycle of SCLK-. If SLAVE- is asserted by the on-board I/O, then SCHOD- is not driven onto the backplane for the other I/O cards.

There must be exactly one non-inverting Schottky gate on each I/O card between SCHID- and SCHOD-. For example:



SCLK-

Full Name: Slow Clock

Driven By: The processor

Received By: All system cards

Function: SCLK- is used to synchronize many diverse system signal interactions.

Timing: SCLK- is a derivative of FCLK. It is generated with a divide-by-five circuit which produces a signal with a minimum of a 250-nanosecond period and a 40 percent duty cycle.

NOTE: In all timing descriptions, the term "short half-cycle" refers to the time (2/5 period) when SCLK- is high. The "long half-cycle" refers to the 3/5 period when SCLK- is low.

To minimize clock skew, all cards are required to receive SCLK- into an S240.

L88-127/11

Table 7-34. Backplane Signal Definitions (continued)

SELFC-	
Full Name:	Self Configure (open collector, low true)
Driven By:	All I/O interfaces
Received By:	The memory controller
Function:	SELFC- is asserted to indicate that DMA self-configuration is occurring. The memory controller enables MAP 0 to use during DMA self-configuration. It is also asserted during IAK- (interrupt acknowledge) cycles.
Timing:	SELFC- is driven simultaneously with AB[0:14].
SLAVE-	
Full Name:	Slave Request (open collector, low true)
Driven By:	All I/O interfaces
Received By:	The processor
Function:	SLAVE- is asserted to request the processor to enter slave mode, that is, to force the processor to enter an I/O handshake.
Timing:	SLAVE- is held asserted until the start of the long half cycle of SCLK- following the release of SCHID-.
VALID-	
Full Name:	Data Valid (Tri-state, low true)
Driven By:	The memory controller
Received By:	The processor and I/O interfaces
Function:	VALID- is asserted to signal that the data on the data bus is about to become valid during a memory read cycle or that the data has been written on a write cycle.
Timing:	On a read cycle, the memory will assert VALID- after the rising edge of SCLK- that precedes the appearance of valid data on the backplane by one cycle. VALID- will be held low for one cycle and then released after the rising edge of SCLK- right after data becomes valid. VALID- is also asserted during a write during the last SCLK- cycle of the access.
WE-	
Full Name:	Write Enable (Tri-state, low true)
Driven By:	The processor and I/O interfaces
Received By:	The memory controller
Function:	WE- is asserted to signal a memory write, and held high to signal a memory read.
Timing:	WE- is asserted and released with AB[0:14].

L88-127/12

Parts Locations

Parts locations for the backplanes are shown in Figures 7-1, 7-2, and 7-3.

Parts List

Parts lists for the backplanes are provided in Tables 7-35, 7-36, and 7-37. Refer to Table 7-38 for the names and addresses of manufacturers of the parts in the Manufacturer's Code List.

Dimensions and Assembly

The dimensions for the A400 board, memory, and I/O cards are as follows:

Length	289 mm	(11.38 inches)
Width	172 mm	(6.75 inches)
Thickness	1.6 mm	(9.063 inches)
Parts Clearance:		
Top-of-card	10.2 mm	(0.4 inch)
Beneath card	5.1 mm	(0.2 inch)

The backplane and card cage dimensions are the following:

6-Slot Backplane		
Length	206 mm	(8.13 inches)
Width	198 mm	(7.8 inches)
16-Slot Backplane		
Length	375 mm	(14.75 inches)
Width	140 mm	(5.50 inches)
20-Slot Backplane		
Length	419 mm	(16.5 inches)
Width	203mm	(8.0 inches)
2424A (6-Slot Box)		
Width	325 mm	(12.8 inches)
Height	205 mm	(8.07 inches)
Height w/feet	208 mm	(8.19 inches)
Depth	500 mm	(19.69 inches)
2434A, 2484A (16-Slot Box)		
Width	483 mm	(19 inches)
Height	178 mm	(7 inches)
Depth	648 mm	(25.5 inches)
2134A (20-Slot Box)		
Width	483 mm	(19 inches)
Height	117 mm	(10.5 inches)
Depth	6120 mm	(24 inches)

Figure 7-11 shows the assembly of the 6-slot box, Figure 7-12 shows the assembly of the rack-mounting 16-slot box, and Figure 7-13 shows the assembly of the rack-mounting 20-slot box.

Backplane Schematics

Figures 7-14 and 7-15 are the schematics for the 6-slot backplane and the 16-slot backplane, respectively.

Table 7-35. 6-Slot Backplane Replaceable Parts

Reference Designator	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02420-80001	1	Printed Circuit Board	28480	02420-80001
J1, J2	1251-8053	12	Connector, PC, 2 X 25	28480	1251-8053
J4, J5	1252-1479	2	Connector, Post, 2-pin		
J3	1252-1480	1	Connector, Post, 22-pin		

Table 7-36. 16-Slot Backplane Replaceable Parts

Reference Designator	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02430-80015	1	Printed Circuit Board	28480	02430-80015
J1, J2	1251-8053	21	Connector, PC, 2 X 25	28480	1251-8053
P1-P3	1251-8331	3	Connector, Post, 4-pin	00779	350424-2
J4	1251-8346	1	Connector, Post, 35-pin	00779	531920-1
J5	1251-8396	1	Connector, PC, 2 X 25	28480	1251-8053
CR1, CR4	1902-0939	2	Diode, IN5908	03287	IN5908
CR2, CR3	1902-0941	2	Diode, Transient Sup.	03287	GSICTE-12
R1	0757-0280	1	Resistor, 1k, 125W F TC=0+ -100	24546	C4 1/8 to 1001 F
U1	1810-0182	1	Res Net 220/330X12	04200	1810-0182
W1	0811-3587	1	Resistor 0-ohm	03123	104

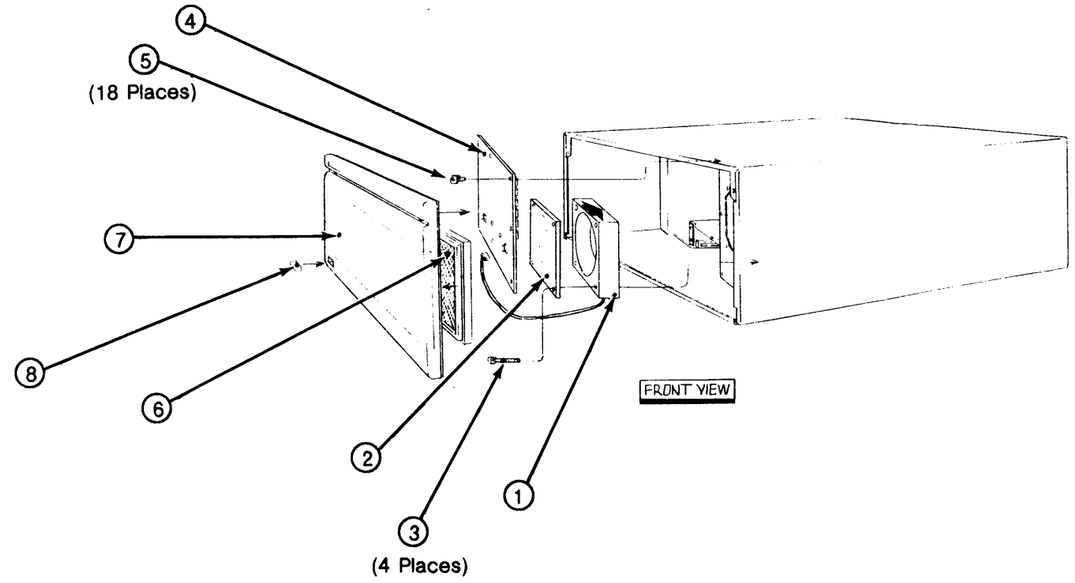
Table 7-37. 20-Slot Backplane Replaceable Parts

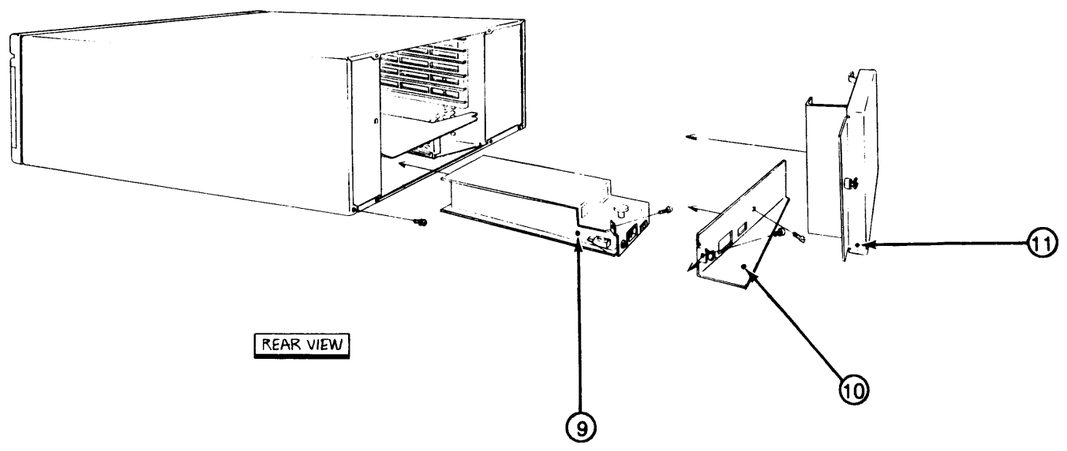
Reference Designator	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1	12151-80002	1	20-Slot Backplane	28480	12151-80002
-	1251-8053	42	Connector, PC, 2 X 25	28480	1251-8053
CR1	1902-0939	1	Diode-Zener 5.0V	03287	IN5908
CR2	1902-0941	2	Diode, Transient Sup.	03287	GSICTE-12
CR3	1902-0941		Diode, Transient Sup.	03287	GSICTE-12
R1	1810-0271	1	Res Network 9 x 200	04200	1810-0271
R2	1810-0272	1	Res Network 9 x 330	04200	1810-0272
W1	0811-3587	1	Resistor-FXD 0-ohm	03123	104

Table 7-38. Manufacturer's Code List

MFR Number	Manufacturer Name	Address	Zip Code
00779	AMP Inc	Harrisburg, PA	17105
01121	Allen-Bradley Co	Milwaukee, WI	53204
01295	Texas Instruments Inc Semicond Component Div	Dallas, TX	75222
03123	Micro Ohm	El Monte, CA	91734
03287	General Semiconductor	Tempe, AZ	85282
03888	K D I Pyrofilm Corporation	Whippany, NJ	07981
04200	Sprague Electric	North Adams, MA	01247
04713	Motorola Semiconductor Products	Phoenix, AZ	85008
07263	Fairchild Semiconductor Division	Mountain View, CA	94042
07910	Teledyne Semiconductor	Hawthorne, CA	90250
18324	Signetics Corporation	Sunnyvale, CA	94086
19701	Mepco/Electra Corporation	Mineral Wells, TX	76067
24546	Corning Glass Works (Bradford)	Bradford, PA	16701
27014	National Semiconductor Corporation	Santa Clara, CA	95051
28480	Hewlett-Packard Co. Corporate Headquarters	Palo Alto, CA	94304
31585	RCA Corporation Solid State Division	Somerville, NJ	08876
34335	Advanced Micro Devices Inc	Sunnyvale, CA	94086
34344	Motorola Inc	Franklin Park, IL	60131
56289	Sprague Electric Company	North Adams, MA	01247

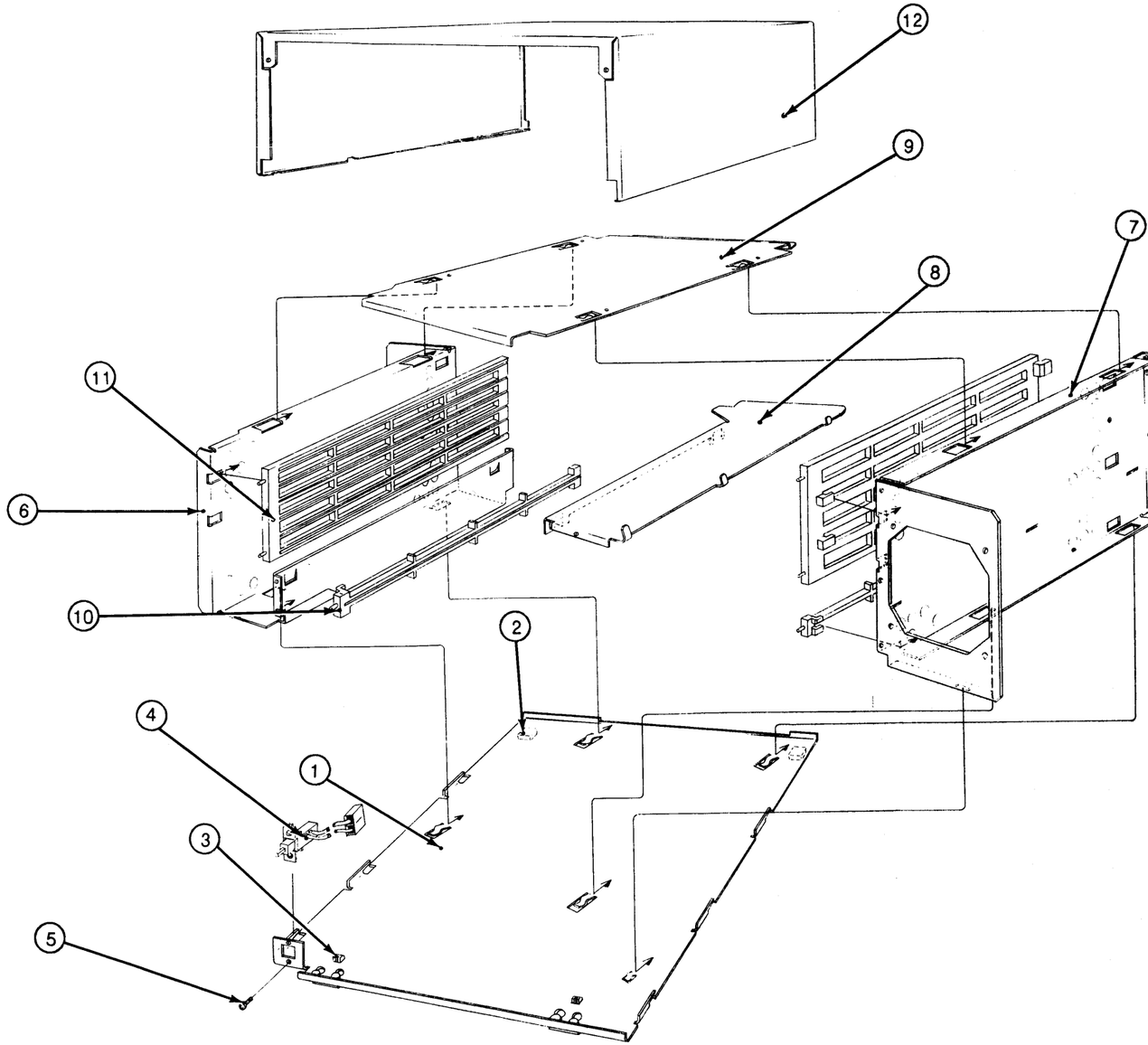
Code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and their supplements.





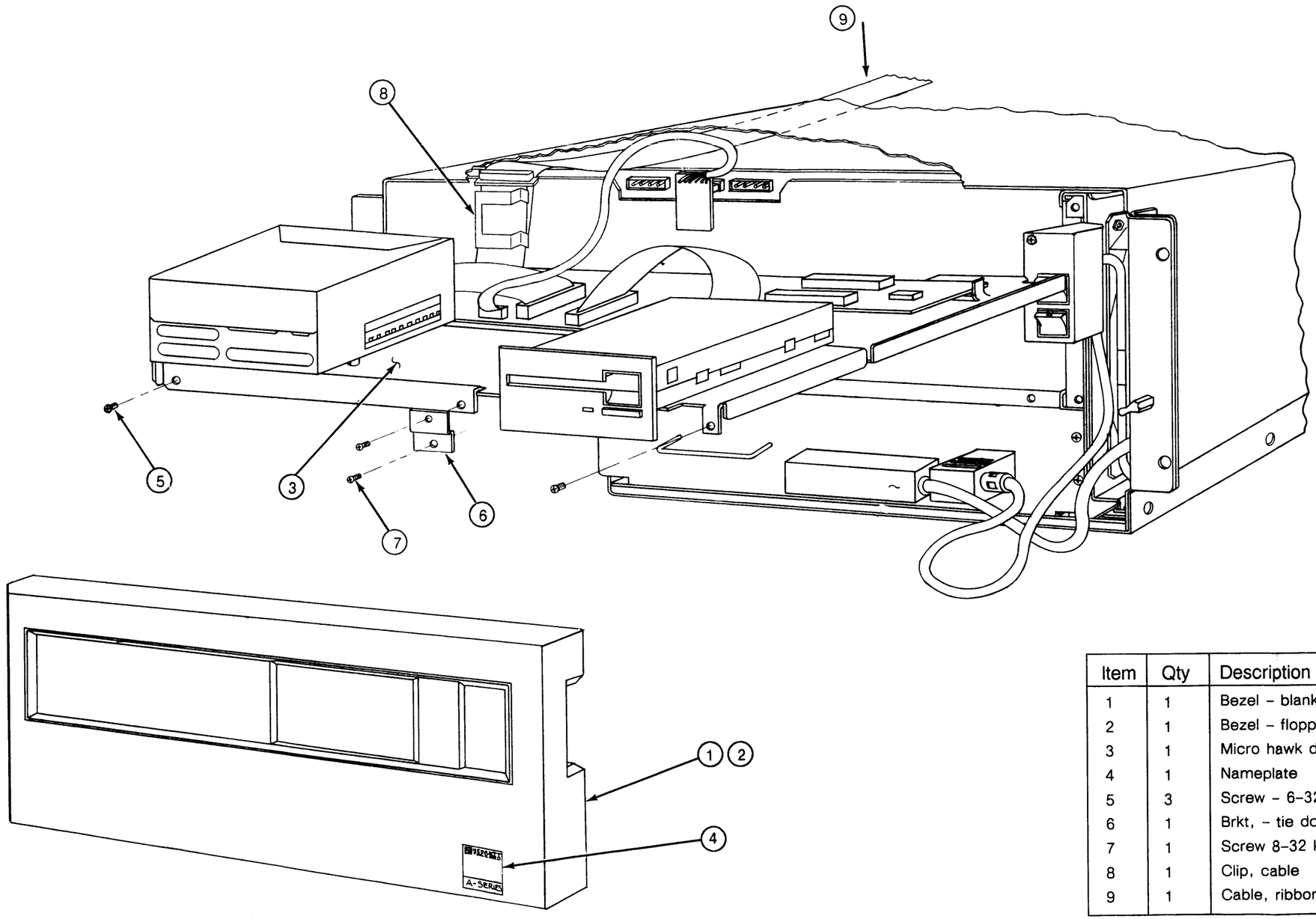
Item #	Description	Part #
1	Fan	3160-0493
2	Finger guard	3160-0463
3	Scr-Mach M3x.5	0515-1431
4	PCA – Backplane	02420-60001
5	Scr-Machine	0515-0866
6	Air filter	3150-0511
7	Bezel	02420-60002
8	Plas push button	5041-1203
9	Power supply	0950-1822
10	Cover power supply	02420-00007
11	Door – rear	02420-00008

Figure 7-11. 6-Slot Box Exploded View, Front (Sheet 1 of 2)



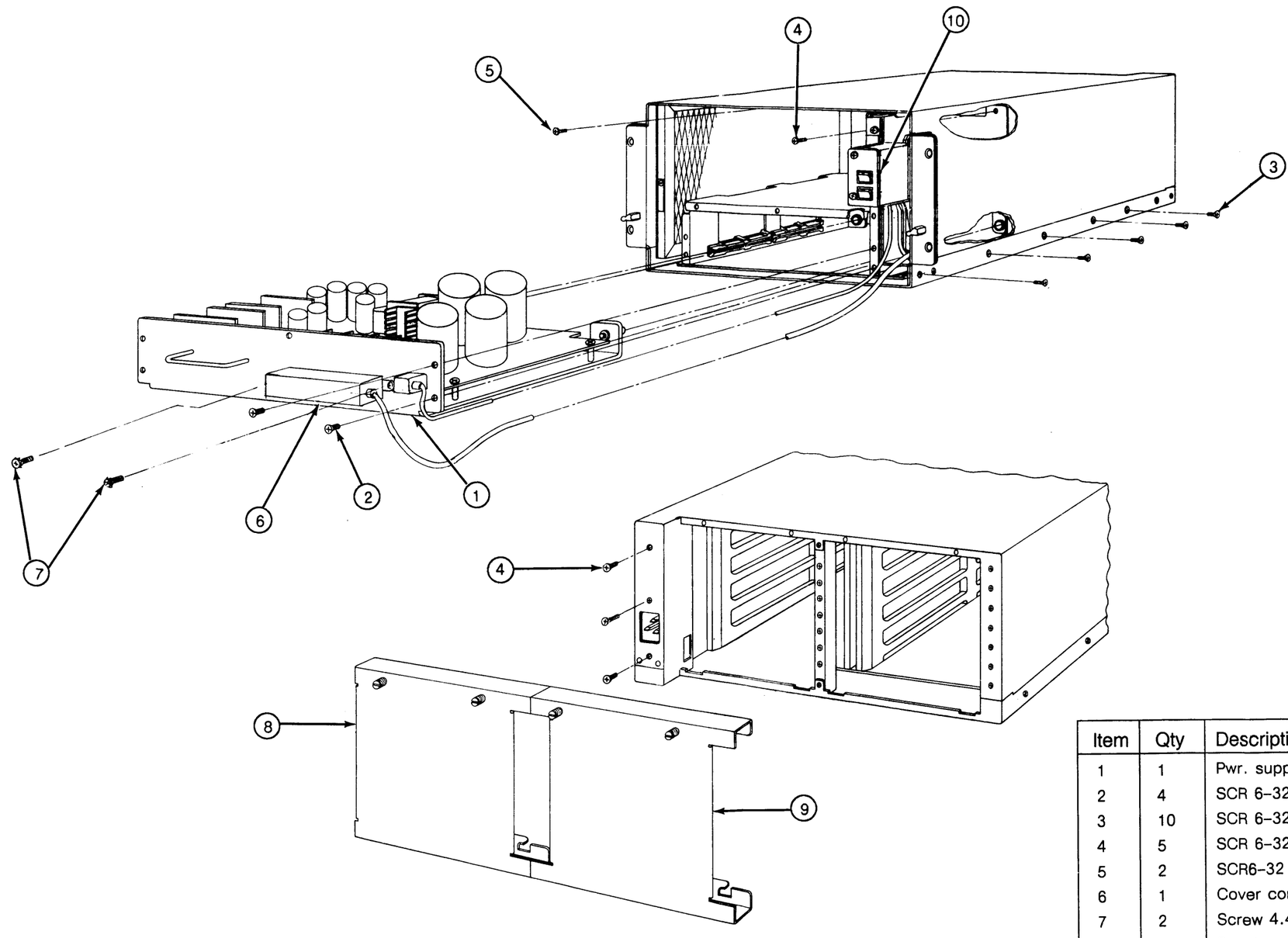
Item	Qty	Description	Part #
1	1	Pan base	02420-00001
2	2	BMPR FT-ADH MTS	0403-0427
3	2	Mounting foot	09121-48303
4	1	Assy-switch	3101-2881
5	18	SCR-machine	0515-0866
6	1	Card cage –L side	02420-00003
7	1	Card cage –R side	02420-00002
8	1	Shield – PWR sup	02420-00004
9	1	Card cage Top CV	02420-00005
10	2	P–S card guide	02420-40003
11	2	Card guide	02420-40002
12	1	Cover top	02420-00006

Figure 7-11. 6-Slot Box Exploded View, Back (Sheet 2 of 2)



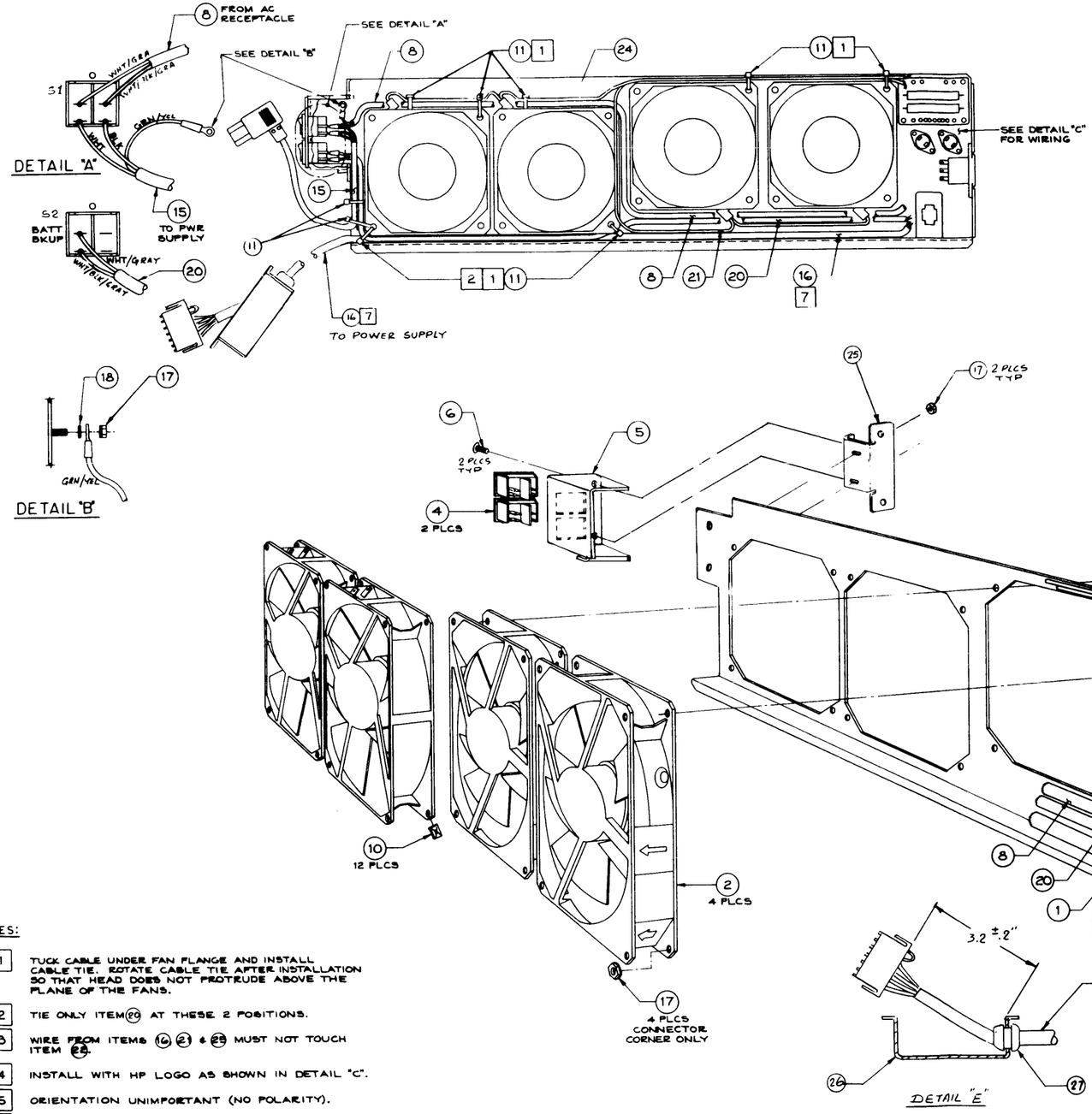
Item	Qty	Description	Part #
1	1	Bezel – blank	02430-40001
2	1	Bezel – floppy	02430-40002
3	1	Micro hawk disc S/S	97596 K
4	1	Nameplate	5180-4242
5	3	Screw – 6–32 k.312	2360-0115
6	1	Brkt, – tie down	02430-00025
7	1	Screw 8–32 k.375	2510-0045
8	1	Clip, cable	1400-1365
9	1	Cable, ribbon	97596-61602

Figure 7-12. 16-Slot Box Exploded View, Front (Sheet 1 of 3)



Item	Qty	Description	Part #
1	1	Pwr. supply - 300W	0950-1788
2	4	SCR 6-32 x. 375L	2360-0117
3	10	SCR 6-32 x .250L FH	2360-0192
4	5	SCR 6-32 x .250 PH	2360-0113
5	2	SCR6-32	2360-0429
6	1	Cover conn.	02430-00028
7	2	Screw 4.40 x 250 W/LK	2200-0103
8	1	Panel rear left	02430-00030
9	1	Panel rear right	02430-00029
10		PDU fan assy	02430-60026

Figure 7-12. 16-Slot Box Exploded View, Back (Sheet 2 of 3)

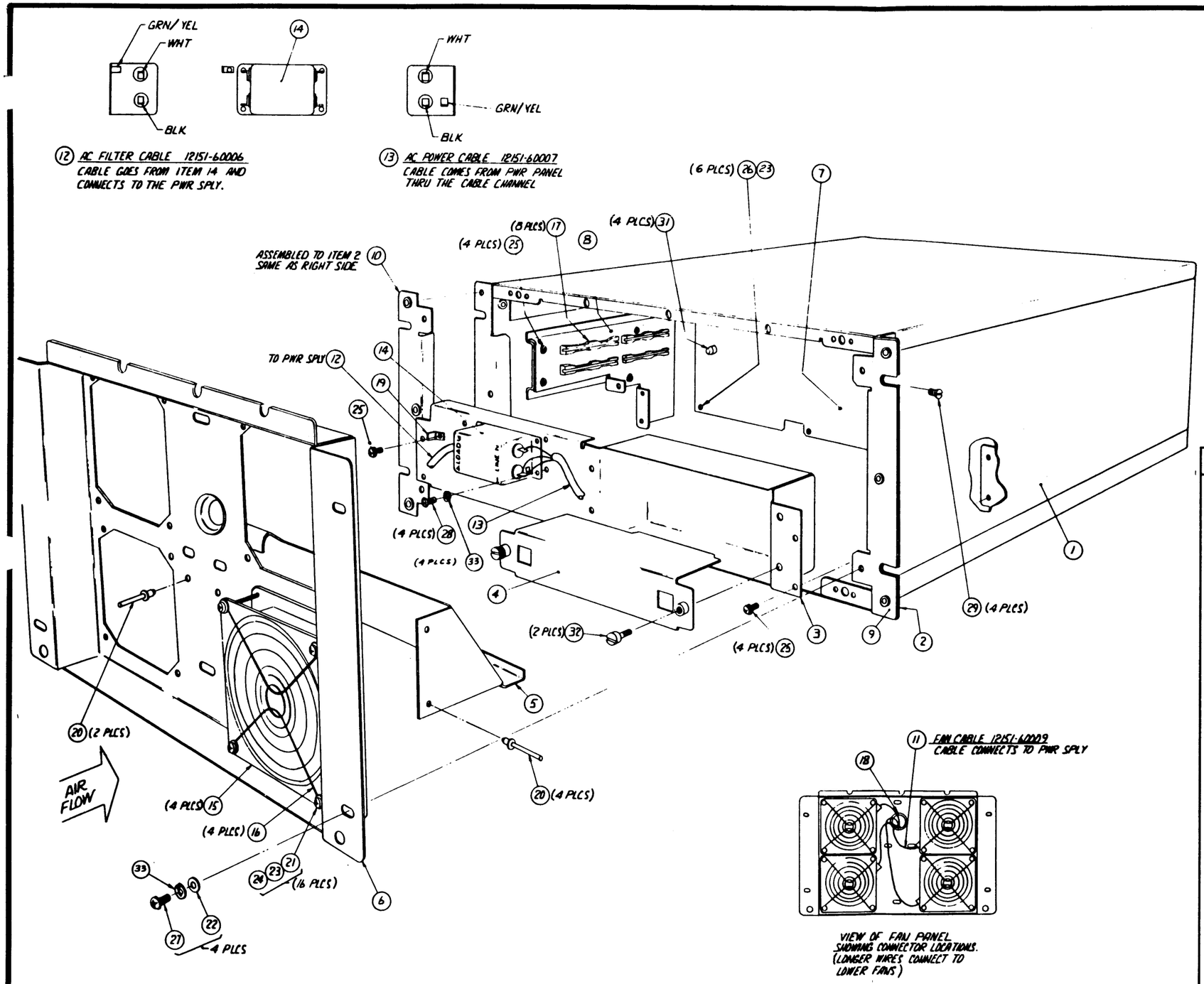


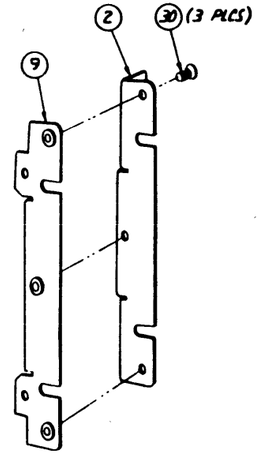
NOTES:

1. TUCK CABLE UNDER FAN FLANGE AND INSTALL CABLE TIE. ROTATE CABLE TIE AFTER INSTALLATION SO THAT HEAD DOES NOT PROTRUDE ABOVE THE PLANE OF THE FANS.
2. TIE ONLY ITEM (20) AT THESE 2 POSITIONS.
3. WIRE FROM ITEMS (16) (21) & (25) MUST NOT TOUCH ITEM (22).
4. INSTALL WITH HP LOGO AS SHOWN IN DETAIL "C".
5. ORIENTATION UNIMPORTANT (NO POLARITY).
6. INSTALL CONNECTOR WITH #1 UP.
7. INSTALL ITEMS (26) (27) BEFORE SOLDERING ITEM (16) TO ITEM (19). SEE DETAIL "E"

ITEM	QTY	MATERIAL-DESCRIPTION	MAT'L-PART NO.
27	1	STRAIN RELIEF GROMMET	0400-0155
26	1	COVER	02430-00028
25	1	SWITCH BRACKET	02430-00027
24	1	FAN CABLE-SHORT	8120-4271
23	4	SCREW-4-40 X .438	2200-0145
22	2	RESISTORS 200 Ω	0811-3643
21	1	FAN CABLE-LONG	8120-4272
20	1	CA. ASSY. BATT. BKUP. - SW.	02430-60011
19	1	PCB-FAN RESISTOR	02430-80010
18	2	LOCK WASHER, EXT. #6	2190-0008
17	8	NUT 6-32 W/LOCK	2420-0001
16	1	CABLE-PCA TO P.S.	02430-60008
15	1	CABLE-A.C. SW. TO P.S.	02430-60007
14	2	SCREW-4-40 X .375 F.H.	2200-0144
13	6	WASHER-FLAT #4	3050-0229
12	10	WASHER-LOCK #4	2190-0108
11	9	CABLE TIE	1400-0249
10	12	CLIP	0590-1516
9	6	NUT #4	2260-0002
8	1	A.C. POWER CABLE	02430-60006
7	16	SCREW #6 F.H. .375	2360-0196
6	2	SCREW #6 F.H. .312	3260-0194
5	1	SWITCH PLATE	02430-00009
4	2	SWITCH-RKR. DPST	3101-0402
3	2	THERMAL SWITCH	3103-0113
2	4	FAN-4.125"	3160-0420
1	1	FAN PANEL	02430-00008

Figure 7-12. 16-Slot Power Distribution Unit (Sheet 3 of 3)



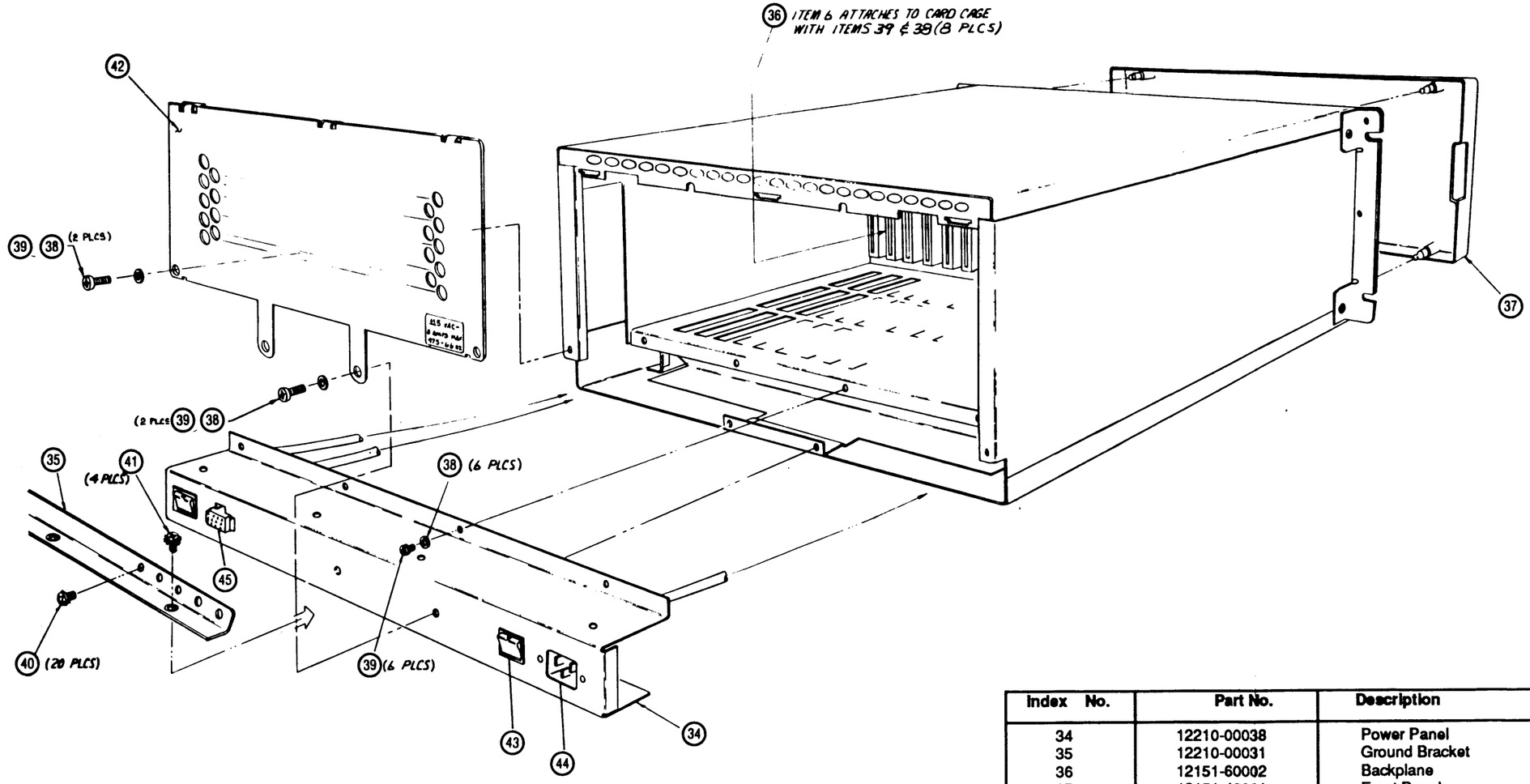


TYP. ASSY. OF INNER RACK EAR TO OUTER RACK EAR

VIEW OF FAN PANEL SHOWING CONNECTOR LOCATIONS. (LONGER WIRES CONNECT TO LOWER FANS)

Index No.	Part No.	Description
1	12151-60026	Chassis A400
2	12151-00032	Rack Ear
3	12210-00020	Battery Support
4	12151-00034	Battery Tray
5	12210-00009	Front Deflector
6	12210-00010	Fan Panel
7	12210-00022	Rear Shield
8	12210-00013	Guide Mounting Bracket
9	12151-00039	Right Inner Rack Ear
10	12151-00038	Left Inner Rack Ear
11	12151-60009	Fan Cable
12	12151-60006	AC Filter Cable
13	12151-60007	AC Power Cable
14	9135-0312	Line Filter
15	3160-0315	Fan
16	3160-0092	Fan Guard
17	0403-0436	Card Guide, Narrow
18	0400-0085	Grommet
19	0360-1263	Terminal
20	0361-1072	Rivet, Blind
21	3050-0228	Flat Washer, #6
22	3050-0139	Flat Washer, #8
23	2190-0851	Lock Washer, #6
24	2360-0318	Screw, PH, 6-32 x 1.875
25	2360-0359	Screw, PH, 6-32 x 0.375
26	2360-0203	Screw, PH, 6-32 x 0.625
27	2510-0103	Screw, PH, 8-32 x 0.375
28	2510-0099	Screw, PH, 8-32 x 0.25
29	2510-0195	Screw, PH, 8-32 x 0.375
30	2360-0333	Screw, FH, 6-32
31	12210-20001	Pin, Locating
32	1390-0607	Panel Fastener
33	2190-0073	Lock Washer, #8

Figure 7-13. 20-Slot Box Exploded View, Front (Sheet 1 of 3)

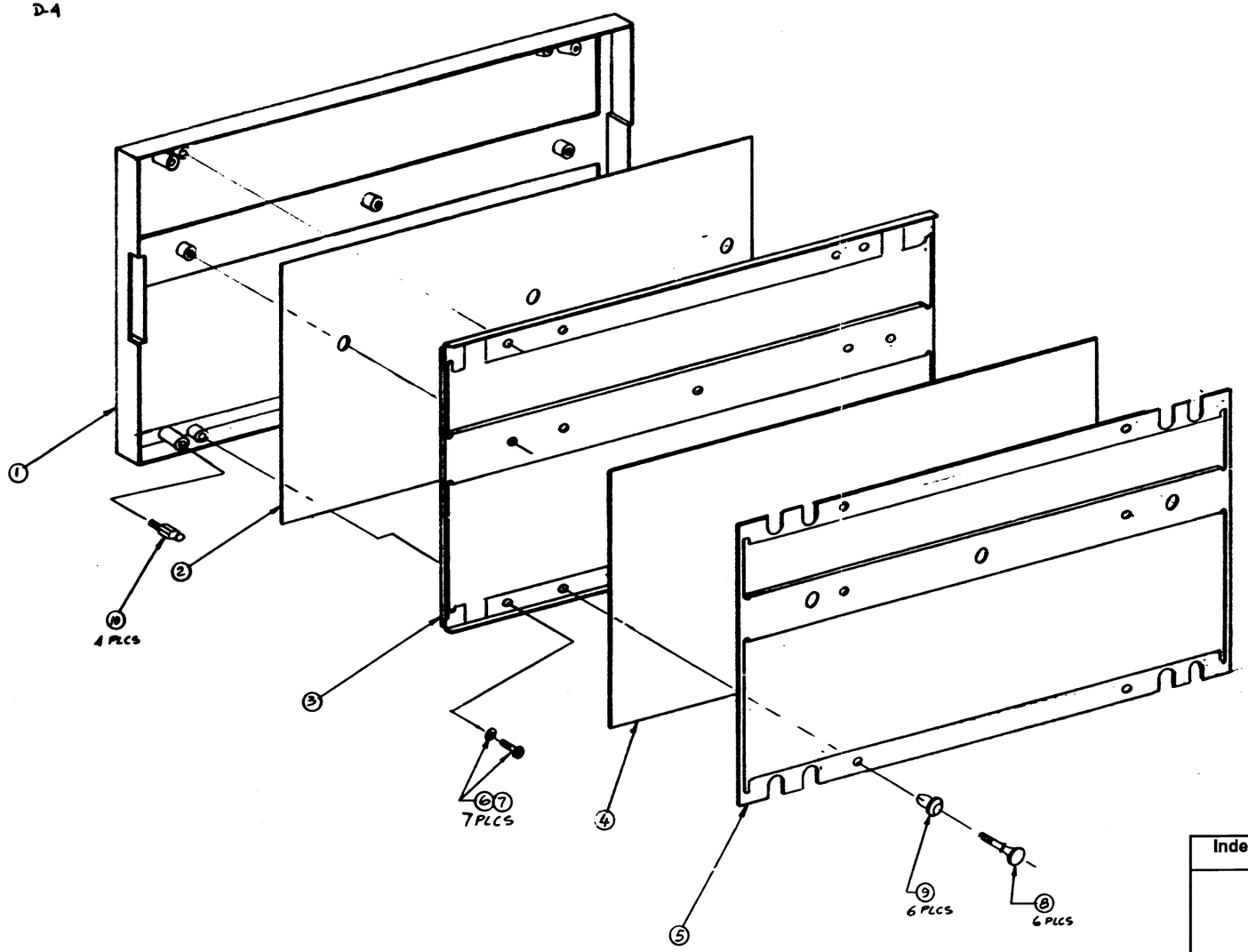


REAR VIEW

Index No.	Part No.	Description
34	12210-00038	Power Panel
35	12210-00031	Ground Bracket
36	12151-60002	Backplane
37	12151-40001	Front Panel
38	3050-0228	Flat Washer, #6
39	2360-0359	Screw, PH, 6-32 x 0.375
40	2510-0045	Screw. 8-32 x 0.375
41	2360-0116	Screw, FH, 6-32 x 0.312
42	5061-6652	Rear Panel
43	3101-0402	Power Switch
44	1251-4470	Power Receptable
45	12151-60008	Test Point Cable

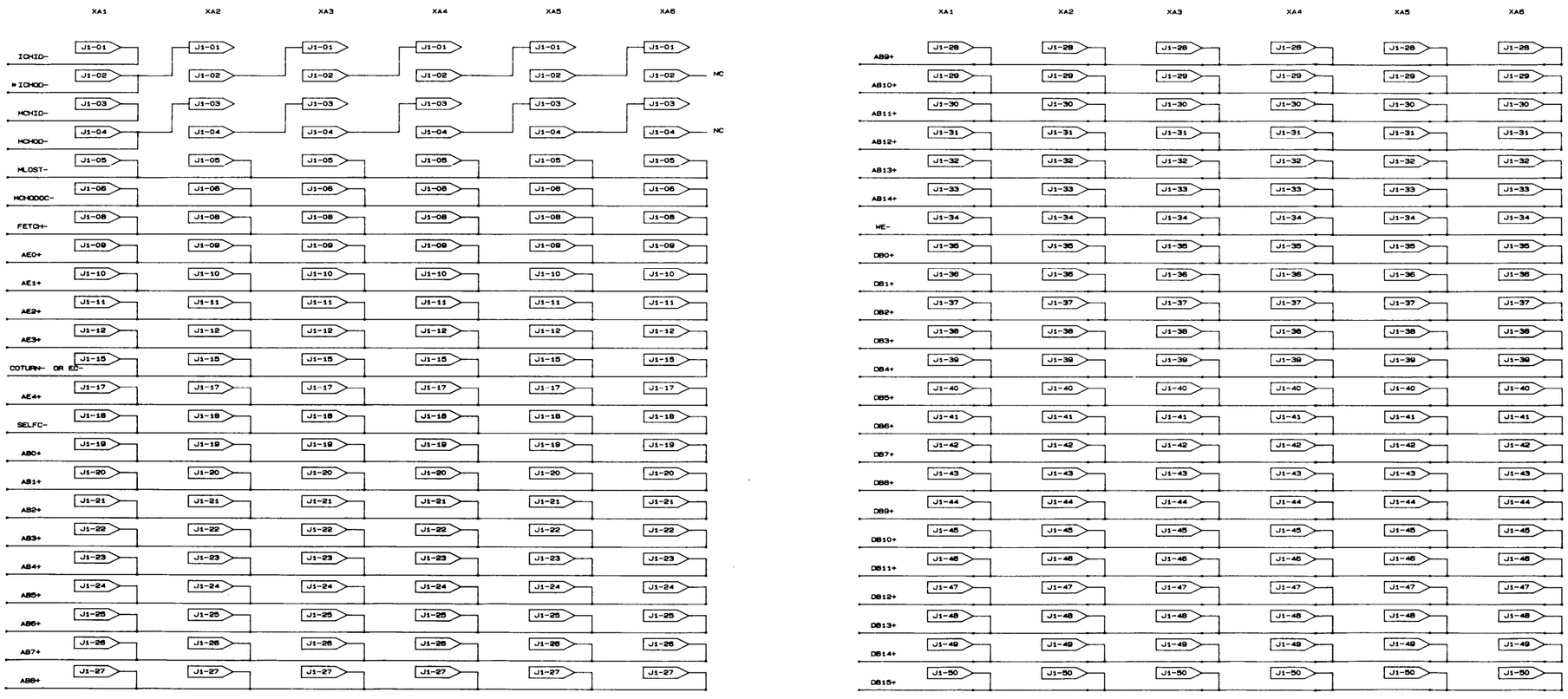
Figure 7-13. 20-Slot Box Exploded View, Rear (Sheet 2 of 3)

REF. DWGS: D-1
D-2
D-4



Index No.	Part No.	Description
1	12151-40001	Front Panel
2	12210-00026	Grill — Flat
3	12210-00025	Front Panel Support
4	4208-0405	Filter Foam
5	12210-00027	Filter Retainer
6	2360-0359	Screw 6-32 x .312
7	3050-0228	Flat Washer
8	1390-0365	Snap in Plunger
9	1390-0366	Snap in Grommet
10	0510-1107	Ball Stud

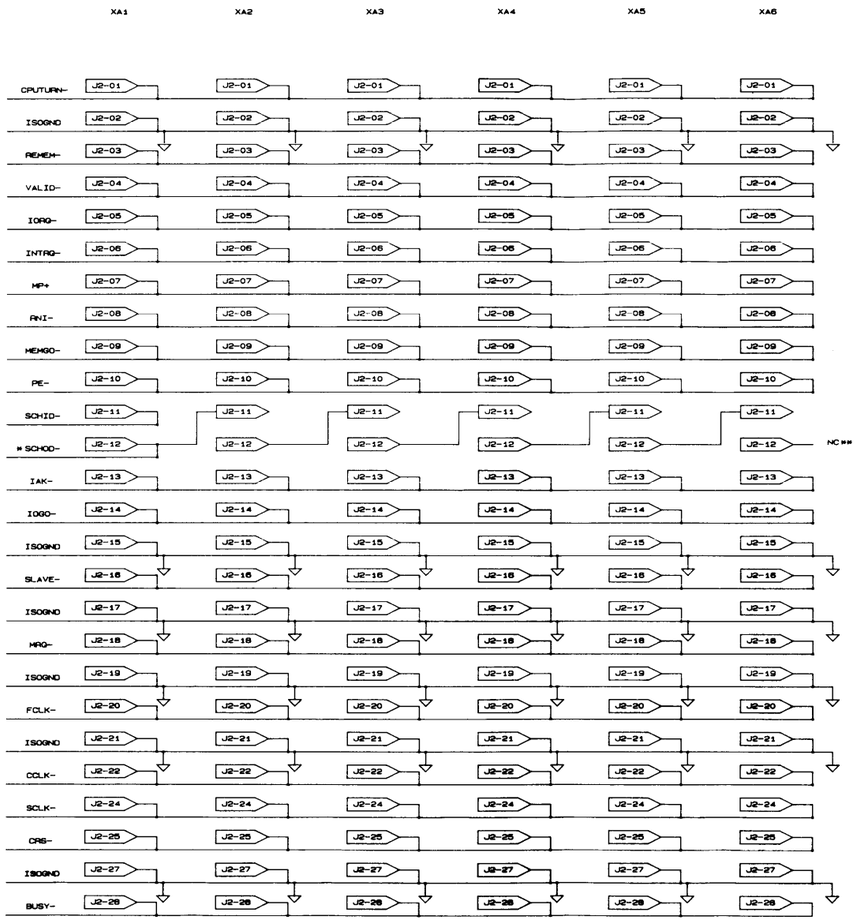
Figure 7-13. 20-Slot Box Front Panel Assembly (Sheet 3 of 3)



*NOTE: THIS SIGNAL IS CALLED PS- ABOVE THE PROCESSOR CARD.

KEITH OKA DRAWN BY	3-24-86 DATE	SCHEMATIC DRAWING BACKPLANE	HEWLETT PACKARD
KEITH OKA ENGINEER	3-24-86 DATE	SIGNALS - J1 CONNECTIONS TITLE	
RELEASE TO PROD	3-25-86 DATE		02420-60001 PART NUMBER
SUPERSEDES DWG		SHEET 1 OF 3	D-02420-60001-51

Figure 7-14. 6-Slot Box Backplane Schematic (Sheet 1 of 3)



SPARES

J2-23 — NC **
J2-39 — NC
J2-40 — NC
J2-47 — NC
J2-48 — NC
J2-49 — NC
J2-50 — NC

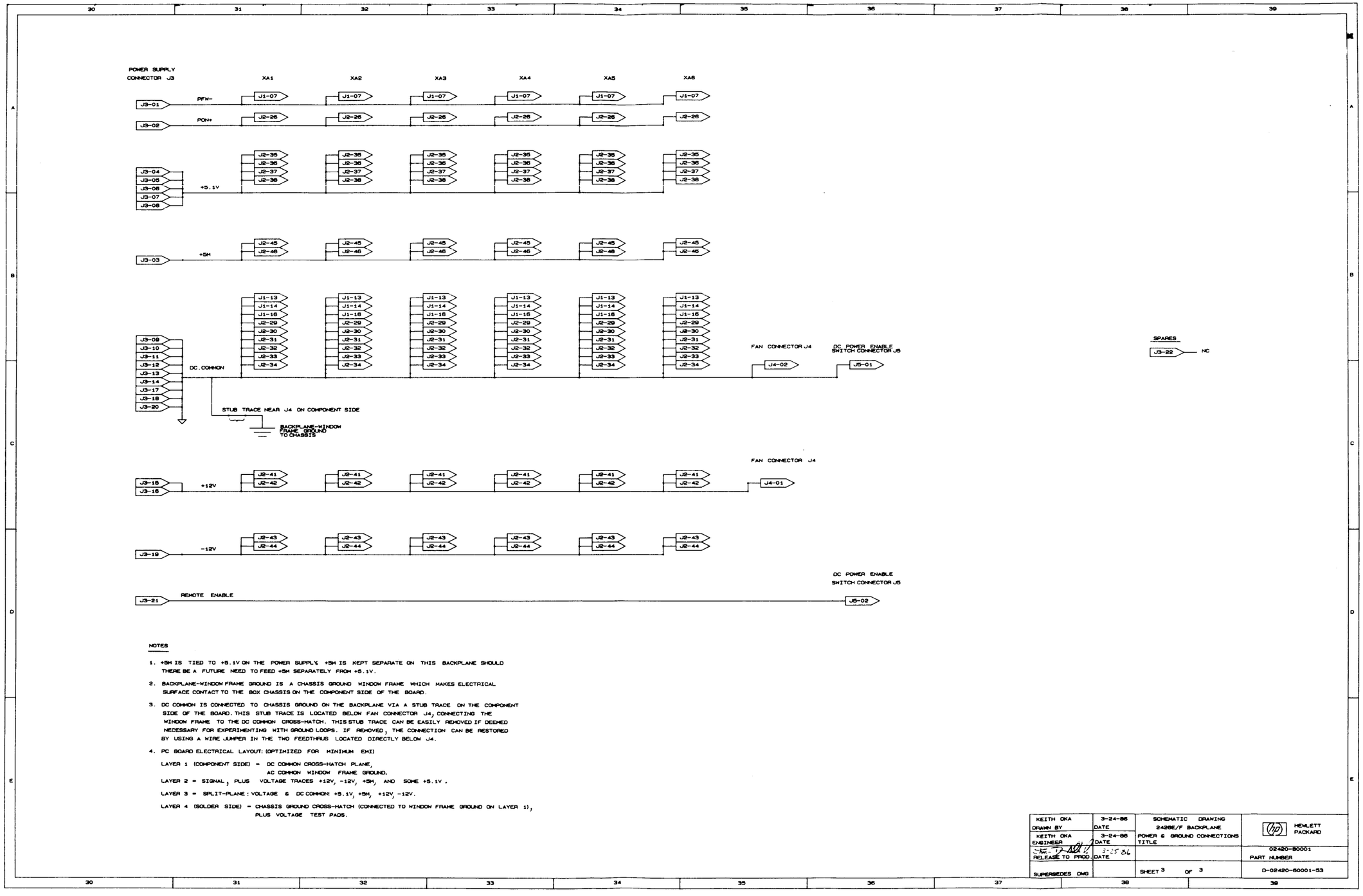
** NC = NOT CONNECTED
J2-23 IS A SPARE BECAUSE IT IS ONLY USED ON THE A700 PROCESSOR. THIS BACKPLANE ONLY SUPPORTS THE A600+ AND A400 PROCESSORS.

*NOTE: THIS SIGNAL IS CALLED MEMDIS- ABOVE THE PROCESSOR CARD.

ISOGND IS A GROUND TRACE WHICH ISOLATES CROSSTALK BETWEEN ADJACENT SIGNAL TRACES.
ISOGND TRACE IS TIED TO DC COMMON PLANE AT EACH SLOT LOCATION FOR OPTIMUM EFFECTIVENESS.

KEITH OKA DRAWN BY	3-24-86 DATE	SCHEMATIC DRAWING BACKPLANE	HEWLETT PACKARD
KEITH OKA ENGINEER	3-24-86 DATE	SIGNALS - J2 CONNECTOR TITLE	
RELEASE TO PROD	1-25-86 DATE		02420-60001 PART NUMBER
SUPERSEDES DWG		SHEET 2 OF 3	D-02420-60001-52

Figure 7-14. 6-Slot Box Backplane Schematic (Sheet 2 of 3)



NOTES

1. +5M IS TIED TO +5.1V ON THE POWER SUPPLY. +5M IS KEPT SEPARATE ON THIS BACKPLANE SHOULD THERE BE A FUTURE NEED TO FEED +5M SEPARATELY FROM +5.1V.
2. BACKPLANE-WINDOW FRAME GROUND IS A CHASSIS GROUND WINDOW FRAME WHICH MAKES ELECTRICAL SURFACE CONTACT TO THE BOX CHASSIS ON THE COMPONENT SIDE OF THE BOARD.
3. DC COMMON IS CONNECTED TO CHASSIS GROUND ON THE BACKPLANE VIA A STUB TRACE ON THE COMPONENT SIDE OF THE BOARD. THIS STUB TRACE IS LOCATED BELOW FAN CONNECTOR J4, CONNECTING THE WINDOW FRAME TO THE DC COMMON CROSS-HATCH. THIS STUB TRACE CAN BE EASILY REMOVED IF DEEMED NECESSARY FOR EXPERIMENTING WITH GROUND LOOPS. IF REMOVED, THE CONNECTION CAN BE RESTORED BY USING A WIRE JUMPER IN THE TWO FEEDTHRUS LOCATED DIRECTLY BELOW J4.
4. PC BOARD ELECTRICAL LAYOUT: (OPTIMIZED FOR MINIMUM EMI)

   LAYER 1 (COMPONENT SIDE) = DC COMMON CROSS-HATCH PLANE, AC COMMON WINDOW FRAME GROUND.

   LAYER 2 = SIGNAL, PLUS VOLTAGE TRACES +12V, -12V, +5M, AND SOME +5.1V.

   LAYER 3 = SPLIT-PLANE: VOLTAGE & DC COMMON: +5.1V, +5M, +12V, -12V.

   LAYER 4 (SOLDER SIDE) = CHASSIS GROUND CROSS-HATCH (CONNECTED TO WINDOW FRAME GROUND ON LAYER 1), PLUS VOLTAGE TEST PADS.

KEITH OKA DRAWN BY	3-24-86 DATE	SCHEMATIC DRAWING 2428E/F BACKPLANE	HEWLETT PACKARD
KEITH OKA ENGINEER	3-24-86 DATE	POWER & GROUND CONNECTIONS TITLE	
RELEASE TO PROD.	3-25-86 DATE		02420-60001 PART NUMBER
SUPERSEDES DWG		SHEET 3 OF 3	D-02420-60001-53

Figure 7-14. 6-Slot Box Backplane Schematic (Sheet 3 of 3)

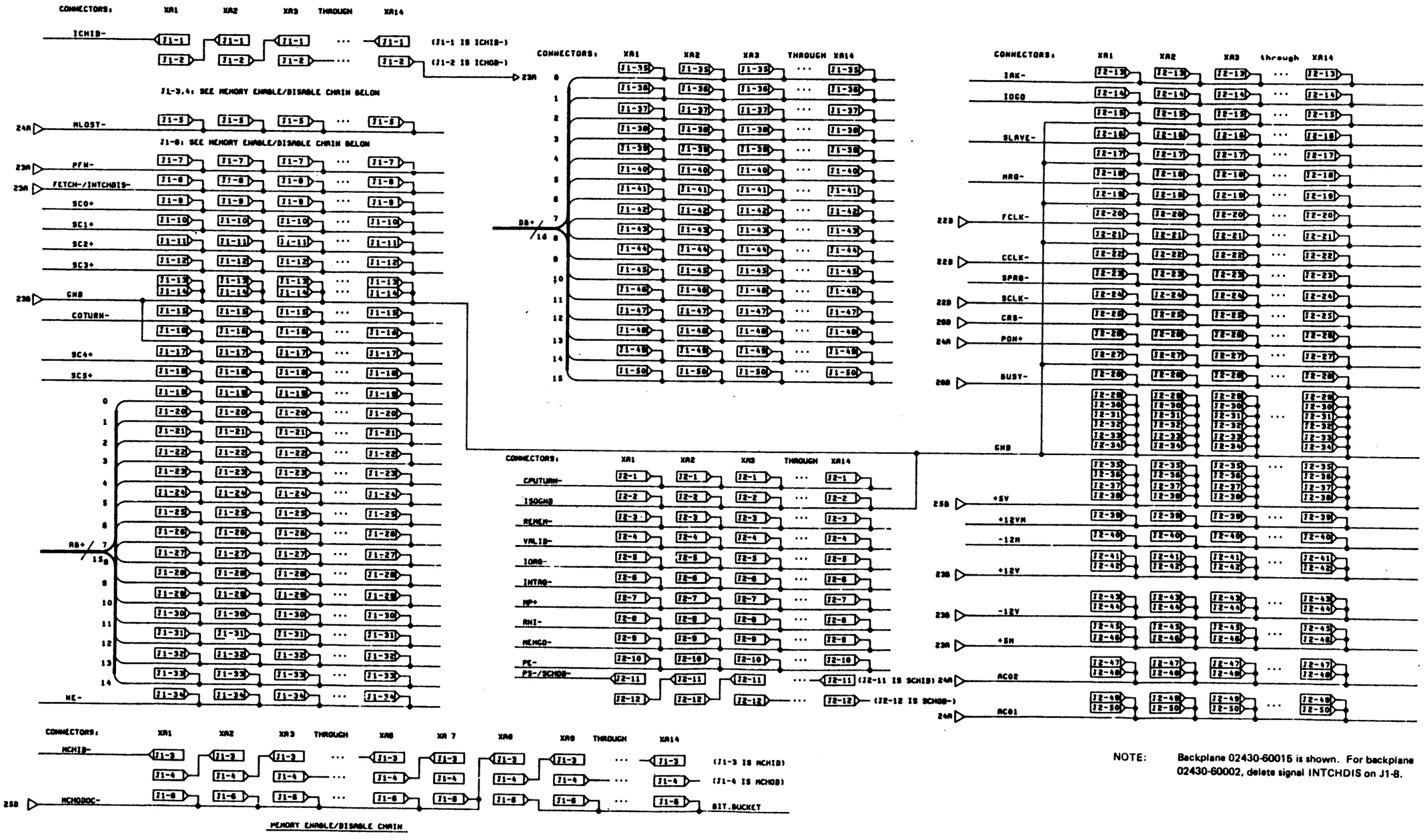


Figure 7-15. 16-Slot Box Backplane Schematic (Sheet 1 of 2)

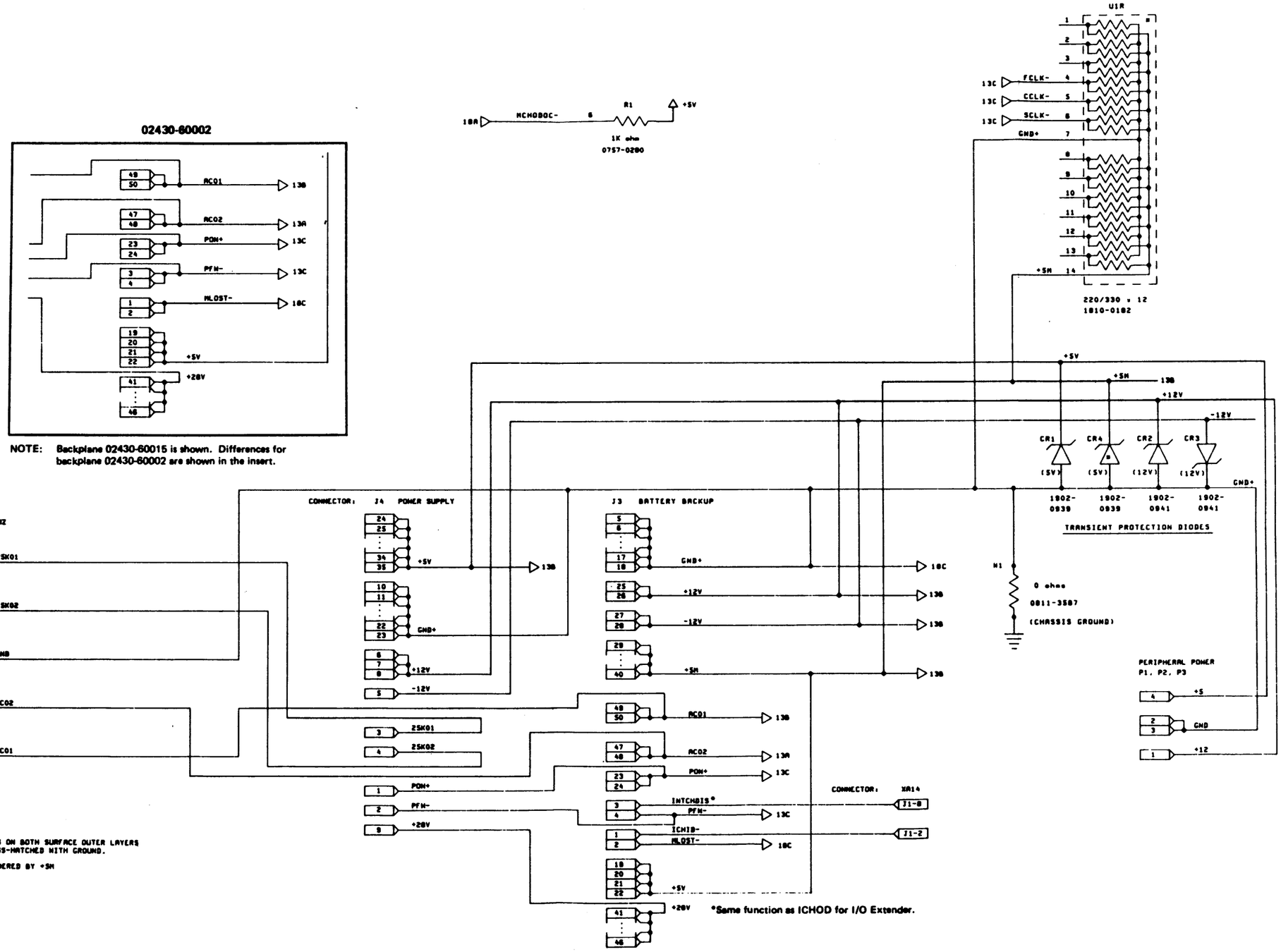


Figure 7-15. 16-Slot Box Backplane Schematic (Sheet 2 of 2)

8

Power Supply

Introduction

There are three power supplies used with the A400 Computer. A 160-Watt power supply is for the 6-slot backplane, a 300-Watt power supply is for the 16-slot backplane, and a 440-Watt power supply is for the 20-slot backplane. All power supplies are modules that plug into the appropriate backplane. With the exception of replacing the fuse due to failure, these power supplies are considered non-repairable in the field and, in case of failure, the entire unit should be replaced with an exchange unit from Hewlett-Packard and the original unit returned for repair.

This chapter provides information required to evaluate the performance of the power supply. Included are an overall operating description, control signal descriptions, and mechanical and electrical specifications.

This chapter is divided into sections covering the following topics:

- the 160-Watt power supply (part no. 0950-1822)
- the Micro/1000 300-Watt power supply (part no. 0950-1788)
- the 440-Watt power supply (part no. 0950-2039)
- the HP 12154A Battery Backup Module for Micro/1000 systems
- the HP 12159A 25 kHz Module for Micro/1000 systems
- applications of the 25 kHz power

160-Watt Power Supply

The 160-Watt power supply is used with the 6-slot backplane. The power supply operates from either 115/120 Vac or 220/240 Vac. It is configured by a switch on the front of the power supply (that is, the back of the computer). The power supply powers one DC fan for system cooling. Battery backup and 25 kHz are not supported with the 160-Watt power supply.

The power supply has three main DC outputs which are +5.1V, +12V, and -12V. Logic signals PON+ and PFW- are provided by the power supply to monitor the system power conditions. A block diagram of the 160-Watt supply is shown in Figure 8-1.

There are two features on this power supply that are not used in the 6-slot box. They are the AC power switch and the remote AC voltage configuration connector (J3). Both of these features are described later in this chapter.

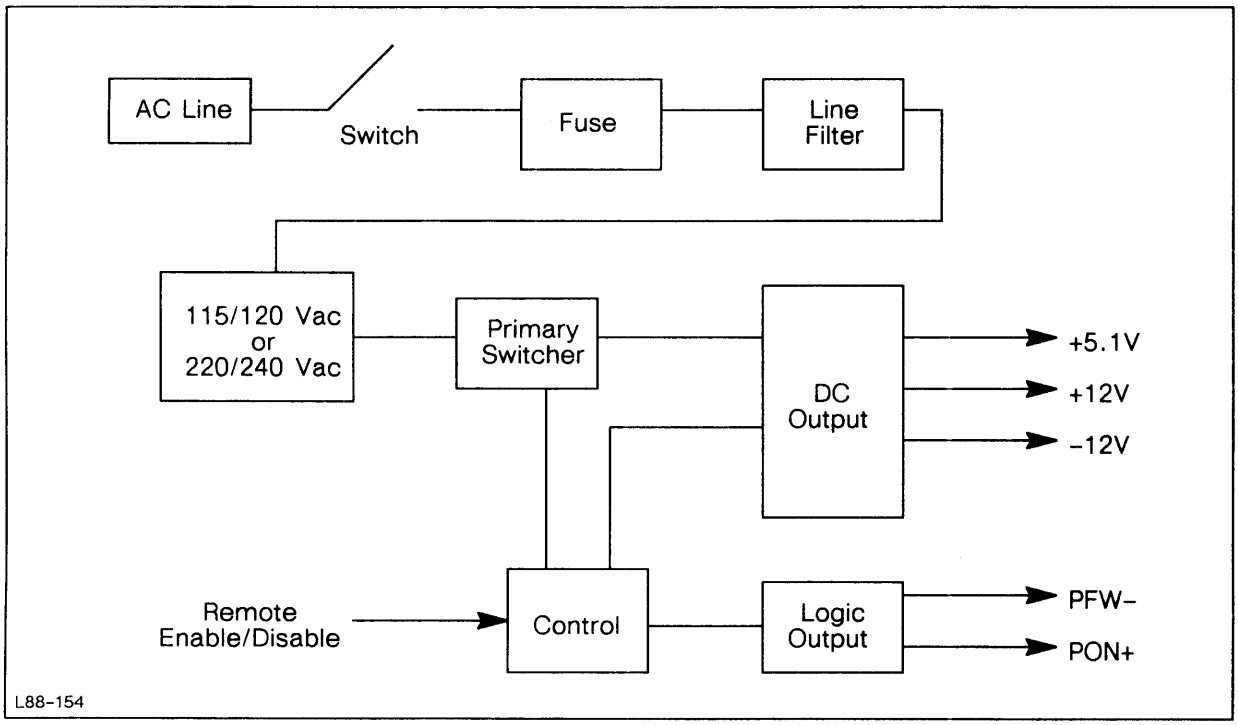


Figure 8-1. 160-Watt Power Supply Block Diagram

Logic Signals

The power supply provides logical control signals (PON+ and PFW–) to the CPU backplane to indicate the status of the AC line and the output voltages. Figures 8-2 through 8-4 show the timing relationships between PON+ and PFW– during power-up or remote enable, during power down, and during remote disable.

PON+

PON+ (Power-On) indicates the status of the three main outputs and is High True when all of the following conditions are met:

Output +5.1V is at least +4.83V
Output +12.0V is at least +10.90V
Output –12.0V is at least –10.90V

PON+ is a bussed signal driven by the power supply. During a power-up sequence it stays low for at least 150 milliseconds after the +5.1V output is valid and for at least 10 milliseconds after PFW– goes high. PON+ remains high while output power is on and stable. When power fails, PON+ must go low at least 50 microseconds before the power supply goes out of regulation.

PON+ behaves the same regardless of the source of power failure. PON+ must be in a valid state (whether it be high or low) at all times. This includes when AC power is not present; that is, PON+ is defined as low when no AC is present and PON+ remains low with no deviation or glitches until AC power is recovered and the outputs meet the threshold conditions listed above.

PFW–

PFW– (Power-Fail Warning) is a system flag which is Low True when the AC line has dropped below the following minimum rms voltages:

Range 1 (115/120 Vac) is less than 84 Vrms
Range 2 (220/240 Vac) is less than 168 Vrms

PFW– is a bussed signal driven by the power supply. When power fails, it is pulled low by the power supply at least 5 milliseconds before PON+ goes low. When power is restored, it is high at least 10 milliseconds before PON+ goes high.

The logic state of PFW– must be valid at all times. This includes holding a valid low even before AC power is ever applied to the unit. Therefore, PFW– must remain low with no deviation or glitches until AC power is above the minimum PFW– threshold (as specified above).

It is valid to have PFW– momentarily deasserted during continuous operation without affecting PON+ (that is, PON+ remains high). This condition can occur if PFW– (and therefore, AC power) is restored high before the power supply bulk charge drops below its safe value to maintain proper operation and carry-over/hold-up times.

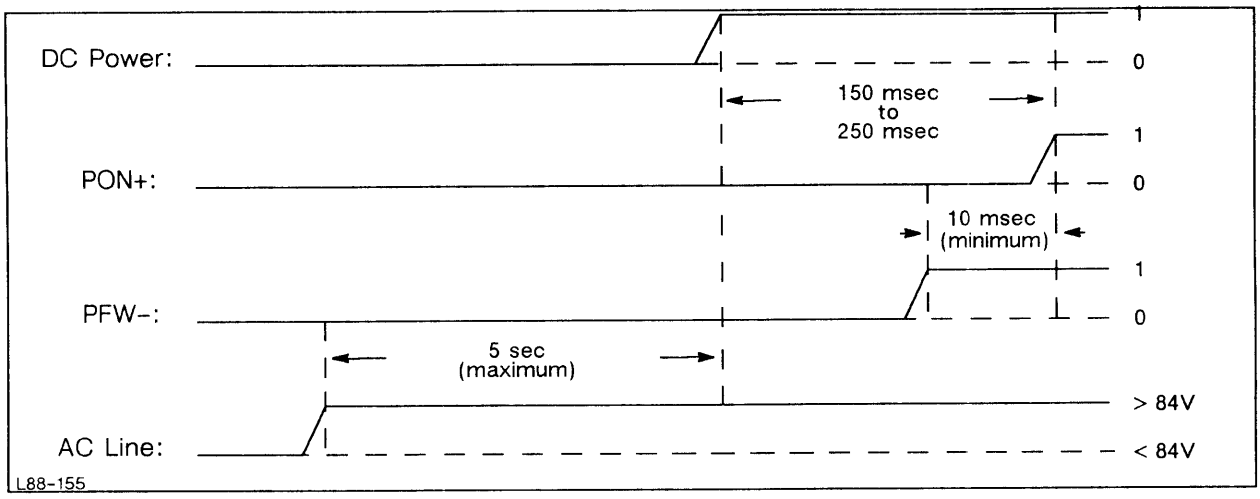


Figure 8-2. Timing Relationship between PON+ and PFW– During Power-Up or Remote Enable

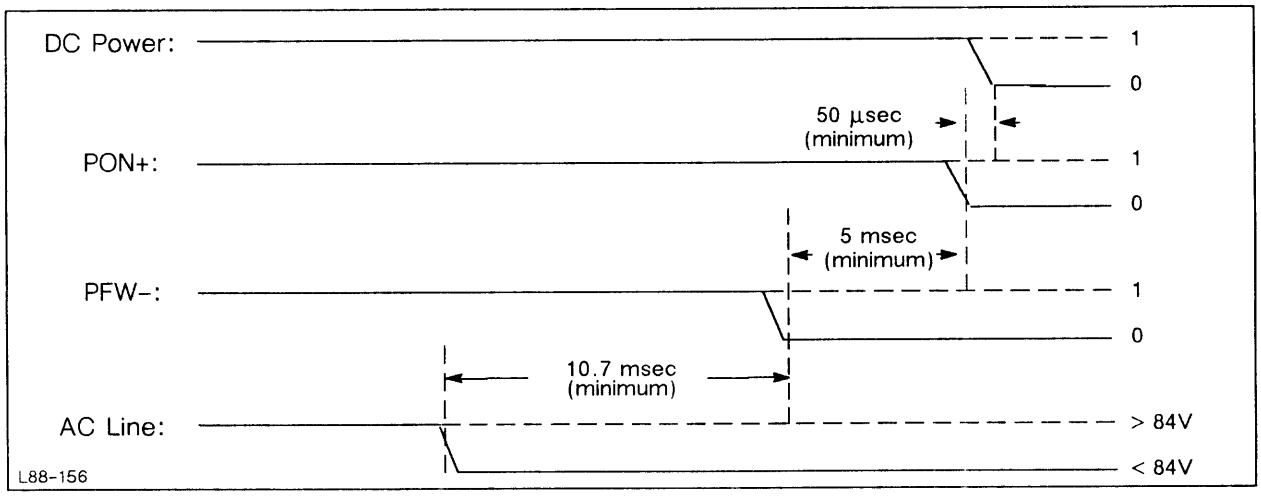


Figure 8-3. Timing Relationship between PON+ and PFW– During Power Down

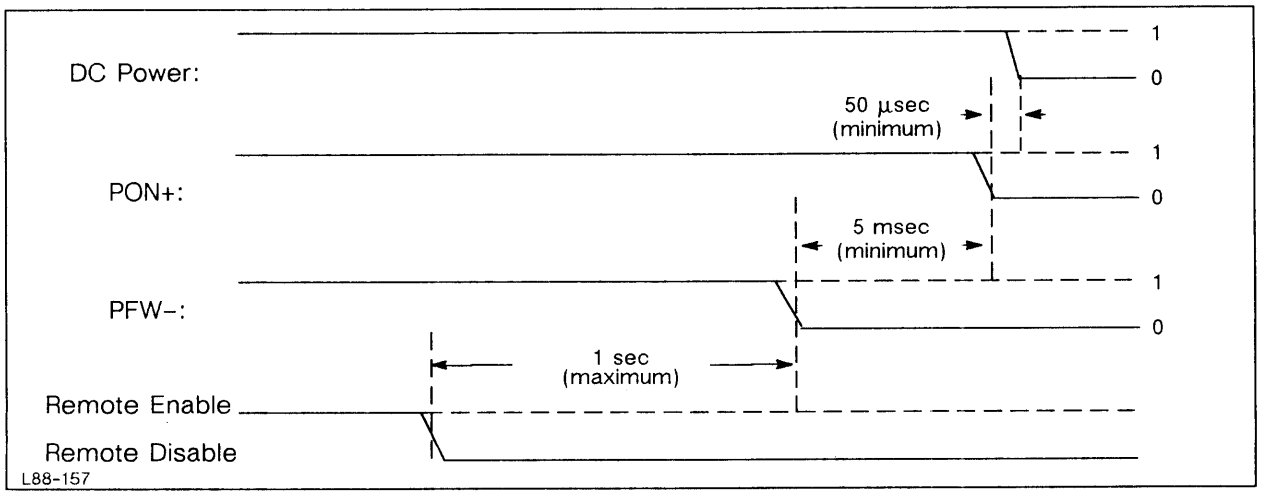


Figure 8-4. Timing Relationship between PON+ and PFW– During Remote Disable

Mechanical Specifications

The overall mechanical dimensions and connector locations of the power supply are shown in Figure 8-5. The connector specifications are given in Table 8-1.

The power supply should be cooled by forced air flowing in one of two directions. The two directions of airflow are shown in Figure 8-5. The volumetric flow rate of air in direction 1 should be a minimum of 15 cubic feet per minute (CFM). The volumetric flow rate of air in direction 2 should be a minimum of 6 CFM.

Table 8-1. Connector Specifications (160W Supply)

Connector	Vendor Part Number	Vendor Mating Part Number
P1*	MOLEX #26-01-1106 (10-position) MOLEX #26-01-1126 (12-position)	MOLEX #09-67-1023 (22-position)
J2	Switchcraft EAC-303	(standard power cord)
J3	MOLEX #19-09-2028 (connector) MOLEX #02-09-2103 (contact)	MOLEX #19-09-1029 MOLEX #02-09-1104

* Connector P1 is made up of one 10-position connector and one 12-position connector for 22 positions total.

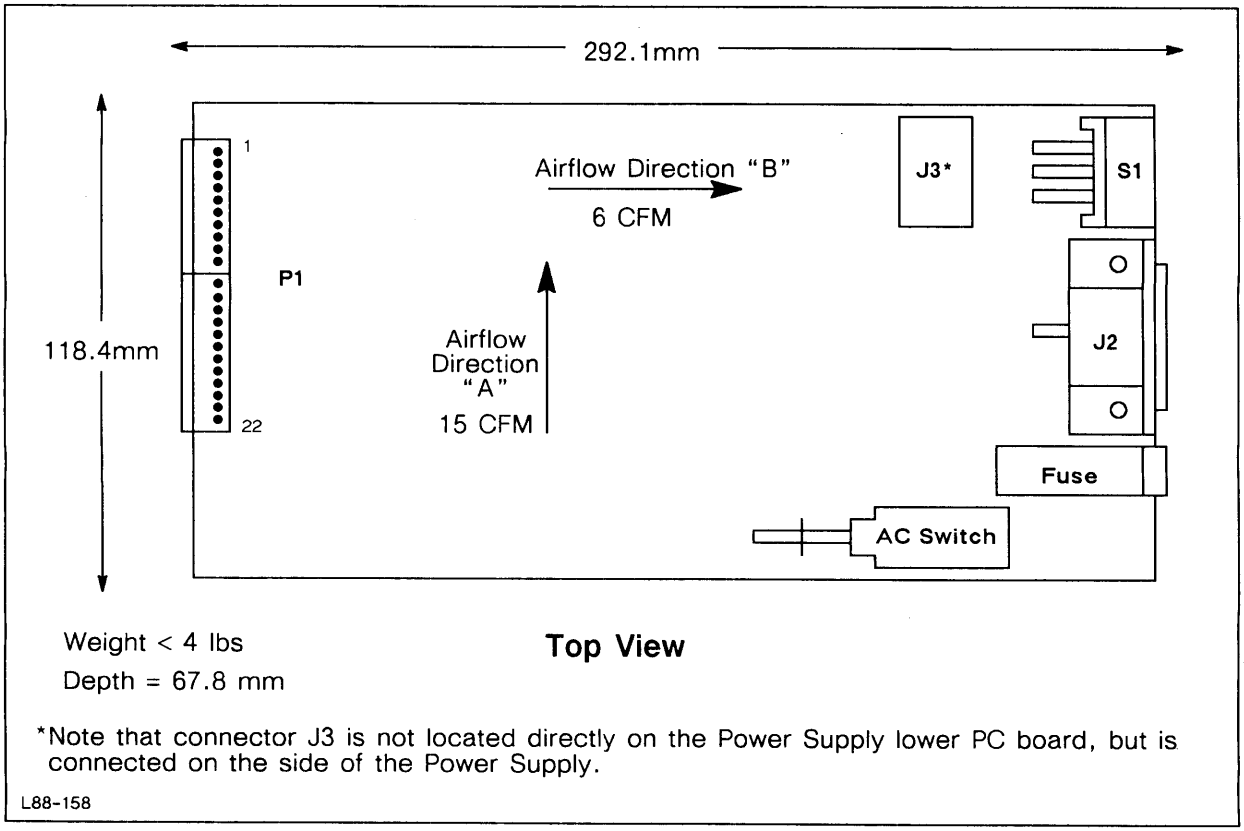


Figure 8-5. 160-Watt Power Supply Dimensions and Connector Locations

Electrical Connections

The electrical contacts for the 160-Watt power supply are provided by three connectors. One is a 22-pin connector that plugs into the backplane, one is the AC line input, and the other (which is not used by the 6-slot box) is the remote AC voltage configuration connector. A power supply connector diagram is shown in Figure 8-6, and electrical connector pin definitions are given in Table 8-2.

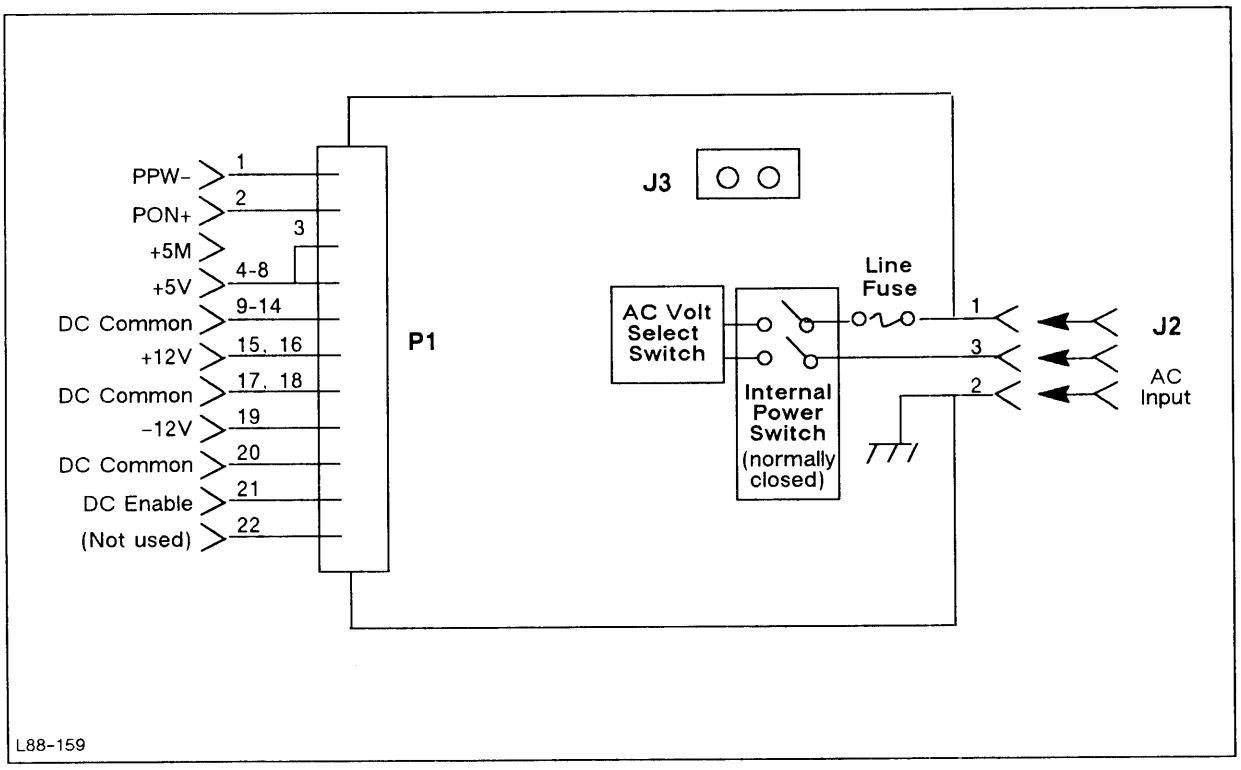


Figure 8-6. 160-Watt Power Supply Connector Diagram

Table 8-2. Electrical Connections (160W Supply)

P1 - DC Output Connector:

Pin Number	Signal Name
1	PFW-
2	PON+
3	+5.1 Volts DC
4	+5.1 Volts DC
5	+5.1 Volts DC
6	+5.1 Volts DC
7	+5.1 Volts DC
8	+5.1 Volts DC
9	DC Common
10	DC Common
11	DC Common
12	DC Common
13	DC Common
14	DC Common
15	+12 Volts DC
16	+12 Volts DC
17	DC Common
18	DC Common
19	-12 Volts DC
20	DC Common
21	Remote Enable
22	Not Used (spare)

J2 - AC Line Input:

Pin Number	Signal Name
1	AC Line
2	AC Ground
3	AC Neutral

J3 - Remote AC Range Select:

Pin Number	Signal Name
1	Range Select
2	Range Select Return

Electrical Specifications

The electrical connectors and switches on the 160-Watt power supply are described in the following sections. The electrical specifications are provided in Tables 8-3 and 8-4.

Voltage Configuration Switch

A switch configures the power supply for either 115/120 Vac nominal or 220/240 Vac nominal operation. It is user selectable from the AC input panel.

The power supply recovers with no permanent damage if the input line voltage conflicts with the line voltage configuration of the power supply. The line fuse is allowed to blow.

AC Power Switch

The power supply has an AC power switch mounted on the PC board and must be kept in the **in** position for proper operation of the power supply in the 6-slot box. The switch can be actuated by pushrod mechanism. AC power is turned on when the switch is **in**; it is turned off when the switch is **out**. The switch is located on the power supply just behind the fuse.

Remote AC Voltage Configuration

The remote AC voltage configuration connector (J3) is not used in the 6-slot box. It is a two-position connector that is provided to allow remote selection of the AC voltage configuration when the standard voltage configuration switch is set to the 220/240 Vac position.

Remote voltage range selection is achieved by connecting a switch (located elsewhere in the computer) to this connector. This new switch then performs the same function as the standard voltage configuration switch. The connector for remote voltage configuration is located along the side of the power supply just behind the standard voltage configuration switch.

Remote Enable/Disable

Pin 21 of the output connector P1 is designated for remotely switching the power supply outputs on and off. This line is a low energy DC signal (approximately 15V or less). When the line is disconnected, the DC outputs are enabled. When the line is connected to DC COMMON the DC outputs are disabled.

Enabling the power supply does not require cycling AC power as long as there have been no failing conditions (for example, overcurrent, overvoltage, overtemperature).

Line Fuse Replacement

The power supply line fuse is user-replaceable and accessible from the AC input panel. To replace the fuse, use a tool, such as a flat blade screwdriver to push in and turn the fuse counter-clockwise until it comes out.

The proper fuse for replacement is labeled on the power supply. It is a 5A 250V normal blow fuse (HP part no. 2110-0010). The same fuse is used for either 115/120 or 220/240 Vac operation.

Table 8-3. Input Electrical Specifications (160W Supply)

AC Line Specifications:

	Min	Nominal	Max	
Range 1 (120V)				
Voltage	84	120	142	Volts RMS
RMS Current (Max)	3.43	2.40	2.03	Amps
Inrush	–	–	20.0	Amps peak
Range 2 (240V)				
Voltage	168	240	278	Volts RMS
RMS Current (Max)	1.71	1.20	1.04	Amps
Inrush	–	–	40.0	Amps peak
Carry Over	15.64	–	–	milliseconds
PFW Trip Point				
Range 1	–	–	84	Volts RMS
Range 2	–	–	168	Volts RMS
Line Frequency	47	60	66	Hz
Line Fuse	–	–	5.0	Amps
Input Power	–	–	213	Watts
Power Factor	.74	–	–	PF

Notes:

1. The line filter reduces conducted noise to 2 dBuV below the VDE Level B conducted emission specification. Conducted noise is measured with the power supply configured for 220/240 Vac operation and its output loaded for 160W by a resistive load. For 115/120 Vac operation of the power supply, conducted noise must be 2 dBuV below the FCC Class B conducted emission specification.

2. Power supply operation permits input transients of up to 3000V for periods of less than 10 microseconds.

Table 8-4. Output Electrical Specifications (160W Supply)

Maximum Dynamic Load: 10% of load over 10 microseconds

Output Stress Conditions Allowed:

The power supply will shut down in the event of any of the following output stresses (it is necessary to cycle the AC power to restore normal operation upon removal of the failing condition; allow about 20 seconds recovery time with the AC powered off):

1. Shorted output
2. Overcurrent
3. Overvoltage
4. Excessive temperature

Output Regulation:

For a 3.0 Amp or greater load on output #1:

Output #	Nominal Voltage	Regulation	Output Current Min	Output Current Max
1	+5.1V	+2% -2%	3.0 Amps	23.0 Amps
2	+12.0V	+6% -3%	0.0 Amps	3.6 Amps
3	-12.0V	+6% -4%	0.0 Amps	1.1 Amps

Note that the combined output is not to exceed 160 Watts for any given combination of output loads.

With no load (open circuit):

Output #	Nominal Voltage	Regulation	Output Current Min	Output Current Max
1	+5.1V	+10% -10%	0.0 Amps	3.0 Amps
2	+12.0V	+10% -9%	0.0 Amps	3.6 Amps
3	-12.0V	+12% -9%	0.0 Amps	1.1 Amps

Environmental Specifications

The environmental specifications of the 160-Watt power supply are provided in Table 8-5. These specifications are based on the power supply in the 6-slot box.

Table 8-5. Environmental Specifications (160W Supply)

Non-Operating Temperature: -55° to 75°C (-67° to 167°F)

Operating Temperature: -5° to 65°C (23° to 149°F)

Operating Survival Temperature: -20° to 75°C (-4° to 167°F)

Operating Humidity: 5% to 95% non-condensing

Vibration:

The power supply is capable of operating in a continuous random vibration environment. Shown below are the power spectral density levels allowed in this environment:

Frequency (Hz)	Power Spectral Density (g^2/Hz)
5	0.002
5–15	-1.5 dB/octave
15	0.0015
12–200	-6.0 dB/octave
200	0.00012

Shock:

Non-Operating
33g peak force applied as an 11-millisecond half-sine pulse. Tested 3 times on each of 6 surfaces (18 tests).

Operating
16g peak force applied as an 11-millisecond half-sine pulse. Tested 3 times on each of 6 surfaces (18 tests).

Altitude:

Non-Operating
50,000 feet

Operating
Operation in all specifications in an altitude range of sea level to 15,000 feet. There is no specification for operation above 15,000 feet.

300-Watt Power Supply

The 300-Watt power supply (part no. 0950-1788) is used with the 16-slot backplane for the Micro/1000 Computers. The power supply operates from either 115 Vac or 230 Vac. There are four fans for cooling (two fans blow across the power supply and two fans blow through the I/O card cage). The fans plug into either connector J3 for 115 Vac operation or into J2 for 230 Vac operation.

The power supply has four DC outputs at +5V, +12V, -12V, and +28V (battery backup source). The power supplies for the battery backup (BB) +5M voltage and the 25 kHz AC outputs are provided by separate optional cards that plug into the backplane. The main power supply generates a 25 kHz square wave that is input to the 25 kHz sine-wave card as the source for its sine-wave output. The 25 kHz sine-wave is used as a power source for certain I/O cards. A block diagram of the 300-Watt power supply is shown in Figure 8-7.

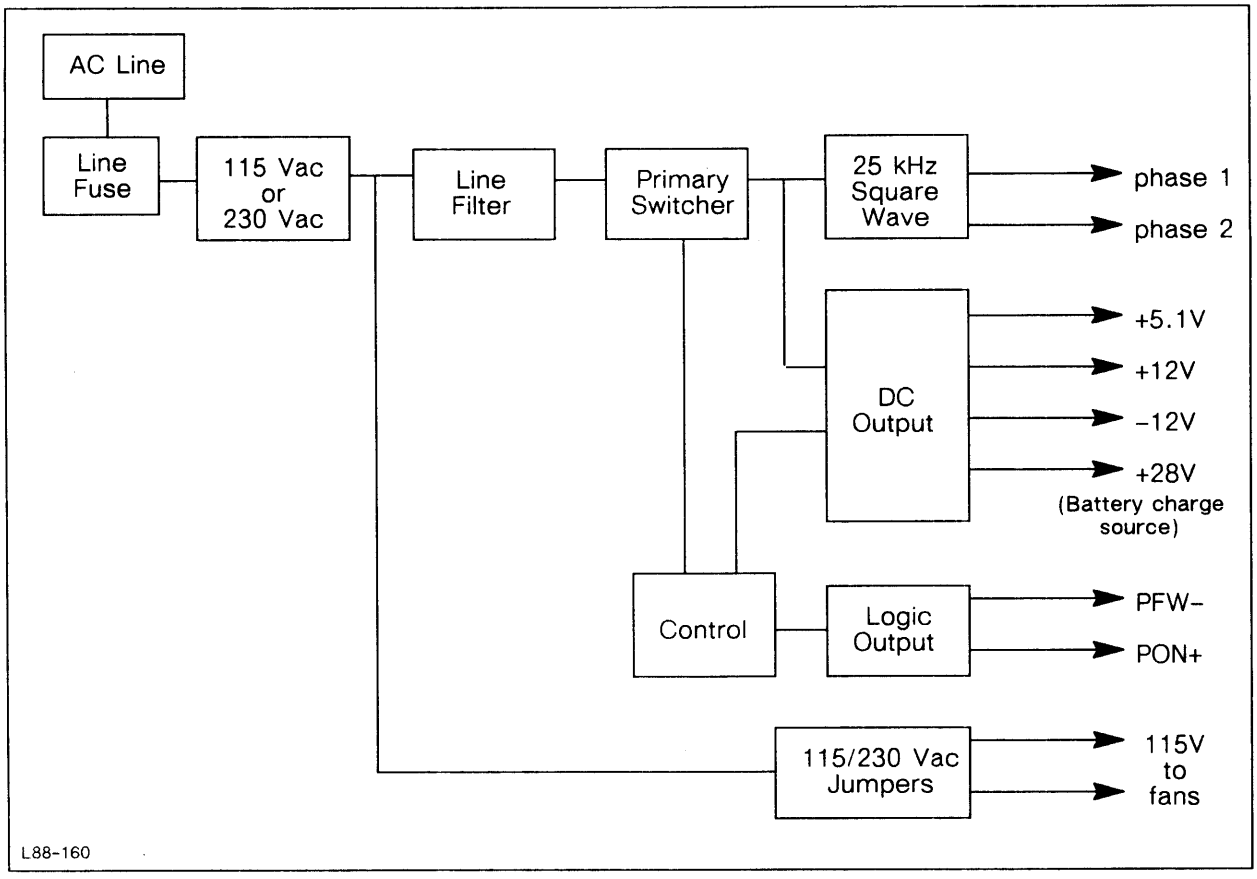


Figure 8-7. 300-Watt Power Supply Block Diagram

Logic Signals

The power supply provides logical control signals to the computer to indicate power availability so that appropriate action can be taken.

PON+

PON+ is a signal that indicates the condition of the DC outputs. When the outputs are within specification, PON+ will be 2.4V to 5.2V. When the outputs are outside of specification, PON+ will be 0.2V plus or minus 0.2V. This definition includes the time when AC power is not applied (that is, when AC power is down, the PON+ signal should be the out-of-specification condition).

The PON+ signal is true when all of the following conditions are met:

Output +5.1V is at least +4.83V
Output +12.0V is at least +10.90V
Output -12.0V is at least -10.90V

A green LED on the front panel of the power supply indicates the condition of PON+. The LED is lit when PON+ is high.

PFW-

The PFW- signal indicates the condition of AC power into the power supply. When the input line voltage is above the power fail trip point, PFW- is 0.2V plus or minus 0.2V.

MLOST-

The MLOST- signal indicates the condition of the memory backup voltage as the main power supply is being powered up. At all other times this signal is of no importance to the system. MLOST- is a pulse that is valid for 1 millisecond before and 5 milliseconds after the rising edge of PON-. The MLOST- pulse during power up will be 2.4V to 5.2V if the memory supplies were within specification during the last power down. If the memory supplies are not within specification, MLOST- will be 0.2V plus or minus 0.2V.

Mechanical Specifications

The overall mechanical dimensions and connector locations of the power supply are shown in Figure 8-8. The power supply connectors are shown schematically in Figure 8-9. The connector specifications are given in Table 8-6.

The cooling air flow should be a minimum of 40 CFM of air flowing across the power supply in the direction indicated in Figure 8-8.

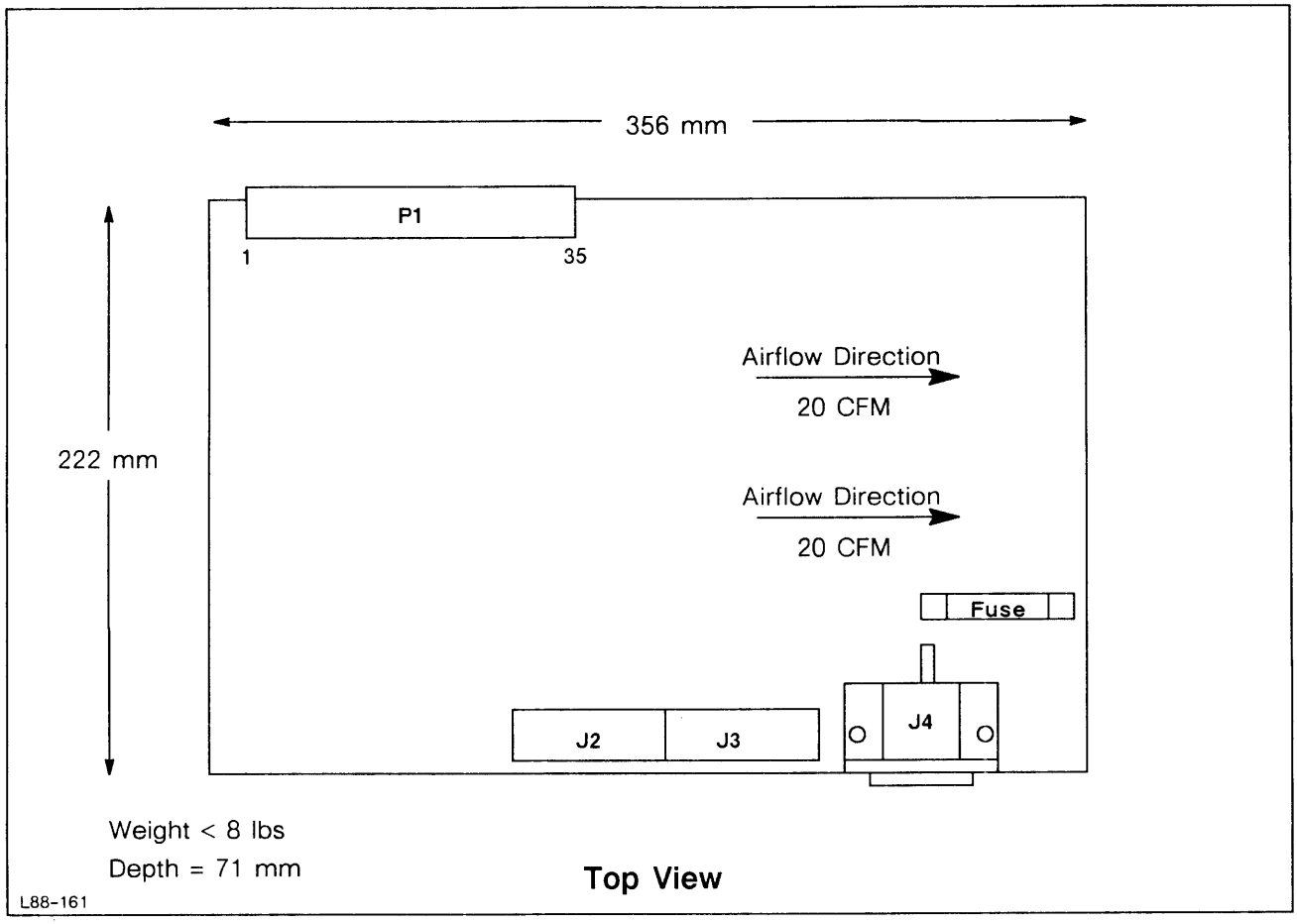


Figure 8-8. 300-Watt Power Supply Dimensions and Connector Locations

Table 8-6. Connector Specifications (300W Supply)

Connector	Vendor Part Number
P1	AMP 1-582390-4
J2	AMP 207378-1
J3	AMP 207378-1
J4	Switchcraft EAC-303

Electrical Connections

The electrical contacts for the 300-Watt power supply are provided by four connectors. One is a 35-pin connector that plugs into the backplane (P1), one is the AC line input (J4), and the other two connectors configure the fans and AC input for 115 or 230 Vac (J3 and J2, respectively). A power supply connector diagram is shown in Figure 8-9. The electrical connector definitions are given in Table 8-7.

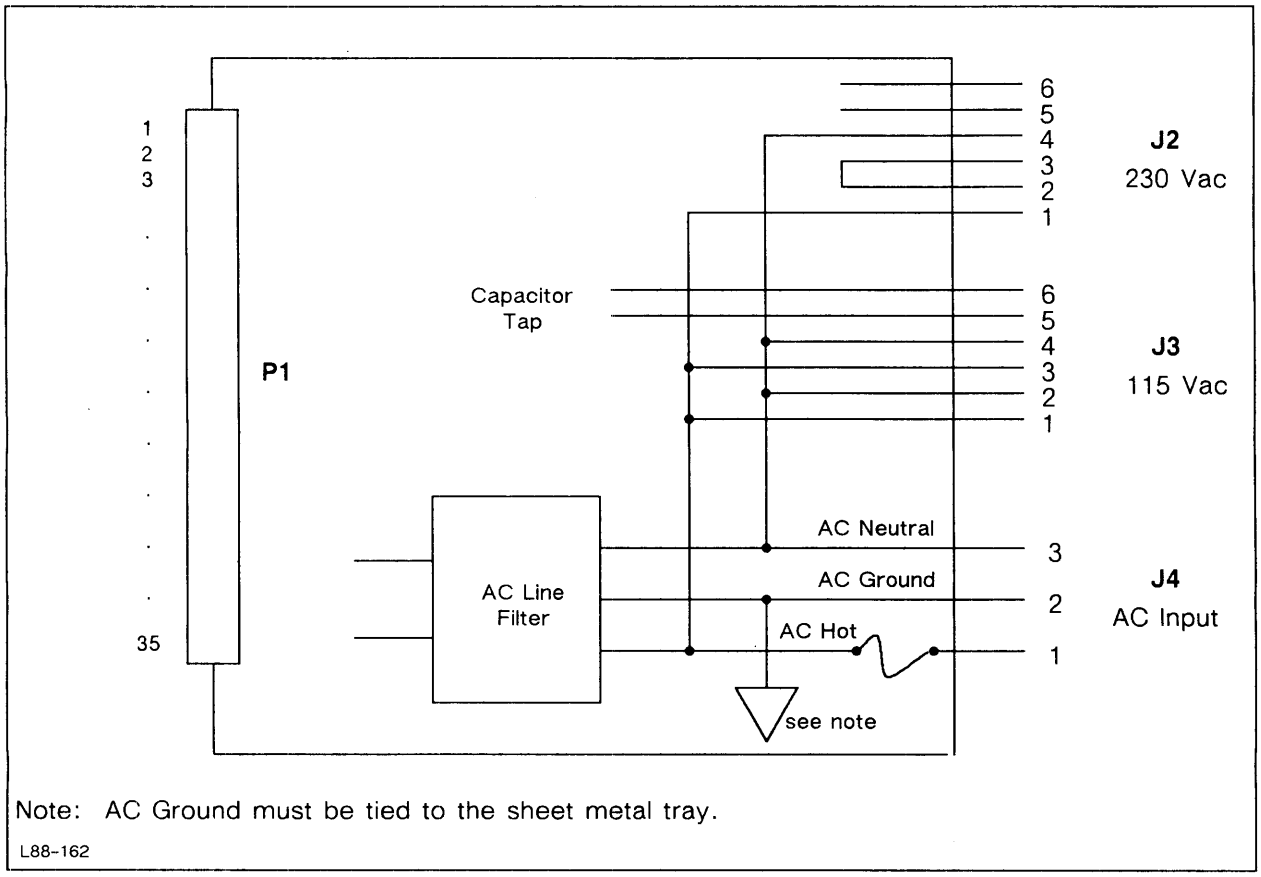


Figure 8-9. 300-Watt Power Supply Connector Diagram

Table 8-7. Electrical Connections (300W Supply)

P1 - DC Output Connector:

Pin Number	Signal Name
1	PON+
2	PFW-
3	25 kHz Phase 1
4	25 kHz Phase 2
5	-12 Volts DC
6 thru 8	+12 Volts DC
9	+28 Volts DC
10 thru 23	DC Common
24 thru 35	+5.1 Volts DC

J4 - AC Line Input:

Pin Number	Signal Name
1	AC Line
2 *	AC Ground
3	AC Neutral

* Pin 2 of this input connector must be tied to the sheet metal base.

J2/J3 - AC Line Configuration/Fans:

Pin Number	Signal Name
1	Fan #1
2	Fan #1
3	Fan #2
4	Fan #2
5	115/230 Vac
6	115/230 Vac

Electrical Specifications

The electrical specifications of the 300-Watt power supply are provided in the tables below. AC line input specifications are given in Table 8-8 and the power supply output specifications are given in Table 8-9.

Table 8-8. Input Electrical Specifications (300W Supply)

AC Line Specifications:

These specifications do not include the power required for the fans.

	Min	Nominal	Max	
Range 1				
Voltage	84	115	140	Volts RMS
RMS Current (Max)	5.7	4.5	4.3	Amps
Inrush	-	-	102	Amps
Range 2				
Voltage	168	230	280	Volts RMS
RMS Current (Max)	2.8	2.3	2.1	Amps
Inrush	-	-	204	Amps
Carry Over	16.0	-	-	milliseconds
PFW Trip Point				
Range 1	-	-	84	Volts RMS
Range 2	-	-	168	Volts RMS
Line Frequency	47	60	67	Hz
Line Fuse	-	-	10.0	Amps
Input Power (not including fans)	-	-	400	Watts

Notes:

1. The line filter reduces conducted noise to 2 dBuV below the VDE 0871 Level B conducted emission specification. Conducted noise is measured with the power supply configured for 230 Vac operation and its output loaded for 300W by a resistive load. For 115 Vac operation of the power supply, conducted noise must be 2 dBuV below the FCC Level B conducted emission specification.

2. Power supply operation permits input transients of up to 3000V for periods of less than 10 microseconds.

Table 8-9. Output Electrical Specifications (300W Supply)

Maximum Dynamic Load: 10% of load over 10 microseconds

Output Stress Conditions Allowed:

a. The power supply will recover from a short to ground or to another regulated output and excessive ambient temperature.

b. Over-rated operated temperature.

Output Regulation:

Note: For the following specifications to be valid, Output #1 will have at least a 3.0 Amp load. With a load less than 3.0 Amps on Output #1, the maximum ripple on Outputs #1, 2, 3, 4, and 6 must not exceed 1.5 Volts peak to peak.

Output #1 - Nominal Voltage = 5.1 Volts
Maximum Current = 50 Amps

Regulation:
0.0 to 3.0 Amps +/- 10%
3.0 to 6.2 Amps +/- 5%
6.2 to 50.0 Amps +/- 2%

Maximum Ripple = 0.10 Volt

Output #2 - Nominal Voltage = 12.0 Volts
Maximum Current = 7.0 Amps

Regulation:
0.0 to .03 Amps +/- 10%
.03 to 7.0 Amps +6% / - 3%

Turn-On Surge = 9.0 Amps +6% / -30% (for 10 seconds maximum)

Maximum Ripple = 0.12 Volt

Output #3 - Nominal Voltage = -12.0 Volts
Maximum Current = 3.0 Amps

Regulation:
0.0 to .10 Amps +/- 12%
.10 to 3.0 Amps +/- 6%

Maximum Ripple = 0.12 Volt

Output #4 - Square Wave

The Square Wave outputs must be in regulation when the load on +5.1 Volts is greater than 6.2 Amps.

	Min	**Nominal**	**Max**	
Phase to Phase	11.20	11.87	12.54	Volts RMS
Phase to Ground	5.60	5.94	6.27	Volts RMS
RMS Current	0.00	-	3.30	Amps/Phase
Frequency	24	28	32	kHz
Output Power	-	-	36	Watts

Table 8-9. Output Electrical Specifications (300W Supply) (Continued)

Output #5 -	Fan Power Nominal Voltage = 115 Volts RMS Maximum Current = 1.25 Amps
Output #6 -	Nominal Voltage = +28.0 Volts Maximum Current = 2.50 Amps Regulation: 0.0 to 2.5 Amps +/- 20% Maximum Ripple = 0.30 Volt
Note:	Although the sum of the maximums listed above exceeds the 300-Watt specification of the power supply front end, not all of the outputs wil be at maximum load at the same time and the actual power is 325 Watts for a maximum of 10 seconds.

Environmental Specifications

The environmental specifications of the 300-Watt power supply are provided in Table 8-10.

Table 8-10. Environmental Specifications (300W Supply)

Non-Operating Temperature:	-40° to 75°C (-40° to 167°F)
Operating Temperature:	0° to 55°C (32° to 131°F)
(Type Tested to ensure margins	-5° to 60°C (23° to 140°F))
Operating Survival Temperature:	-20° to 65°C (-4° to 149°F)
Operating Humidity:	5% to 95% at 40°C wet bulb temperature

Vibration:

Sweep
From 5 to 55 Hz and back at a rate of one octave per minute, with an excursion of .025", for 15 minutes.

Resonance
At each resonant point, not to exceed 4 points, dwell for 10 minutes at the following excursions:

5 - 10 Hz	.125"
11 - 25 Hz	.060"
25 - 55 Hz	.025"

Operating
Random vibration (0.21 Grms) 0.0001 G2 from 5 to 350 Hz. -6 dB/octave from 350 to 500 Hz. 10 minutes per axis.

Non-Operating
Sine sweep 0.5 G from 5 to 500 to 5 Hz. Resonance search 1 octave/minute 5 minutes dwell, 4 resonance per axis.

Random vibration (1.99 Grms) 0.015 G2/Hz from 5 to 100 Hz. -6 dB/octave from 100 to 150 Hz. 0.0067 G2/Hz from 150 to 350 Hz. -6 dB/octave from 350 to 500 Hz.

Shock:

30g peak force applied as an 11-millisecond half-sine pulse. To be tested 3 times in each direction of each axis (18 tests).

Altitude:

Full operating temperature, at 300 Watts output power (not including fan power), at altitudes up to 10,000 feet. From 10,000 feet to 15,000 feet, a linear derating of 2°C per 1,000 feet is allowed. The power supply will survive a 50,000 foot non-operating altitude.

440-Watt Power Supply

The 440-Watt power supply is used with the 20-slot backplane. The power supply operates from either 115 Vac or 230 Vac. There are four fans for cooling the power supply and the computer. The fans plug into either connector P7 for 115 Vac operation or into P8 for 230 Vac operation.

The power supply has four DC outputs at +5V, +5V memory backup (+5M), +12V, and -12V. It also provides 25 kHz AC power that is used as a power source for certain I/O cards. The +5M battery backup (BB) and the 25 kHz AC outputs are standard. However, to sustain memory during a power failure, an optional battery pack, 12157B, must be ordered in order to utilize the battery backup circuitry. A block diagram of the 440-Watt supply is shown in Figure 8-10.

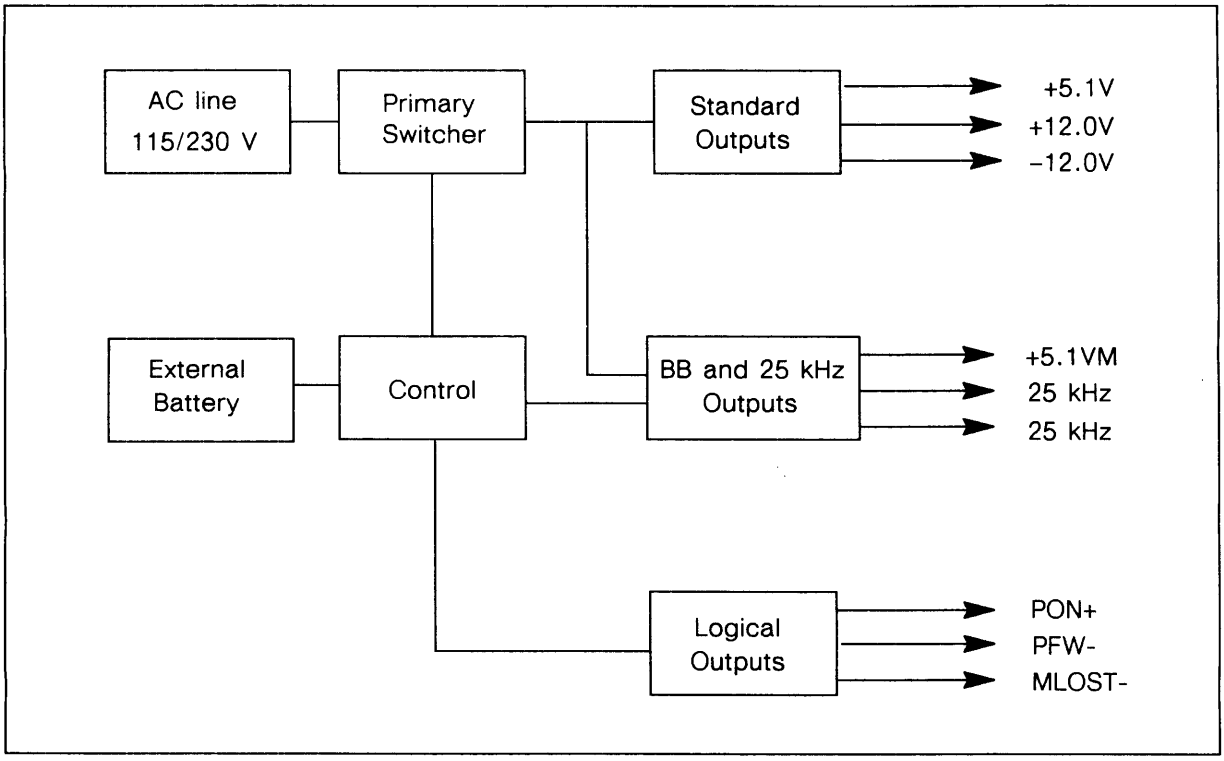


Figure 8-10. 440-Watt Power Supply Block Diagram

Logic Signals

The power supply provides logical control signals to the computer to indicate power availability so that appropriate action can be taken.

PON+

PON+ is a signal that indicates the condition of the DC outputs. When the outputs are within specification, PON+ will be 2.4V to 5.2V. When the outputs are outside specification, PON+ will be 0.2V plus or minus 0.2V. The definition includes the time when AC power is not applied (that is, when AC power is down, the PON+ signal should be the out-of-specification condition).

PFW-

The PFW- signal indicates the condition of AC power into the supply. When the input line voltage is above the power fail trip point, PFW- is 2.4V to 5.2V. When the input line voltage is below the power fail trip point, PFW- is 0.2V plus or minus 0.2V.

MLOST-

The MLOST- signal indicates the condition of the memory backup voltage as the main power supply is being powered up. At all other times this signal is of no importance to the system. MLOST- is a pulse that is valid for 1 millisecond before and 5 milliseconds after the rising edge of PON+. The MLOST- pulse during power up will be 2.4V to 5.2V if the memory supplies were within specification during the last power down. If the memory supplies are not within specification, MLOST- will be 0.2V plus or minus 0.2V.

Mechanical Specifications

The overall mechanical dimensions and connector locations of the 440-Watt power supply are shown in Figure 8-11. The connector specifications are given in Table 8-11.

The cooling air flow should be a minimum of 70 CFM of air flowing across the power board in the direction indicated in Figure 8-11.

Table 8-11. Connector Specifications (440W Supply)

Connector	AMP Part Number	AMP Mating Part Number
P1/P3	Edge Card	-
P2/P4	Edge Card	-
P5	9-350255-2	350240
P6	9-350264-2	350243
P7	207584-1	207396-1
P8	207584-1	207396-1
P9	207365-1	207360-1

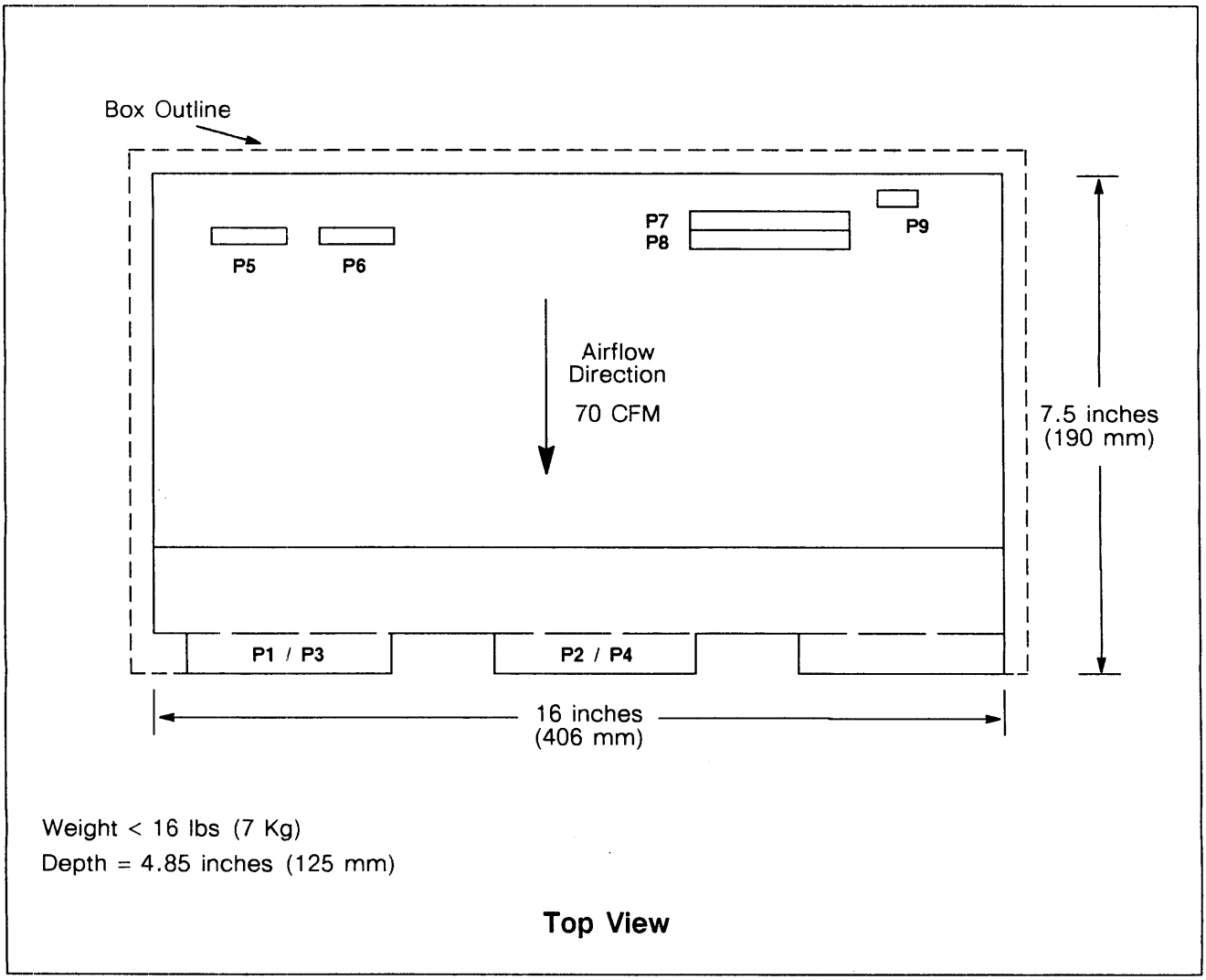


Figure 8-11. 440-Watt Power Supply Dimensions and Connector Locations

Electrical Connections

The electrical contacts for the 440-Watt power supply are provided by nine connectors. Two of these are edge connectors that plug into the backplane. A power supply connector diagram is shown in Figure 8-12, and the electrical connector pin definitions are given in Table 8-12.

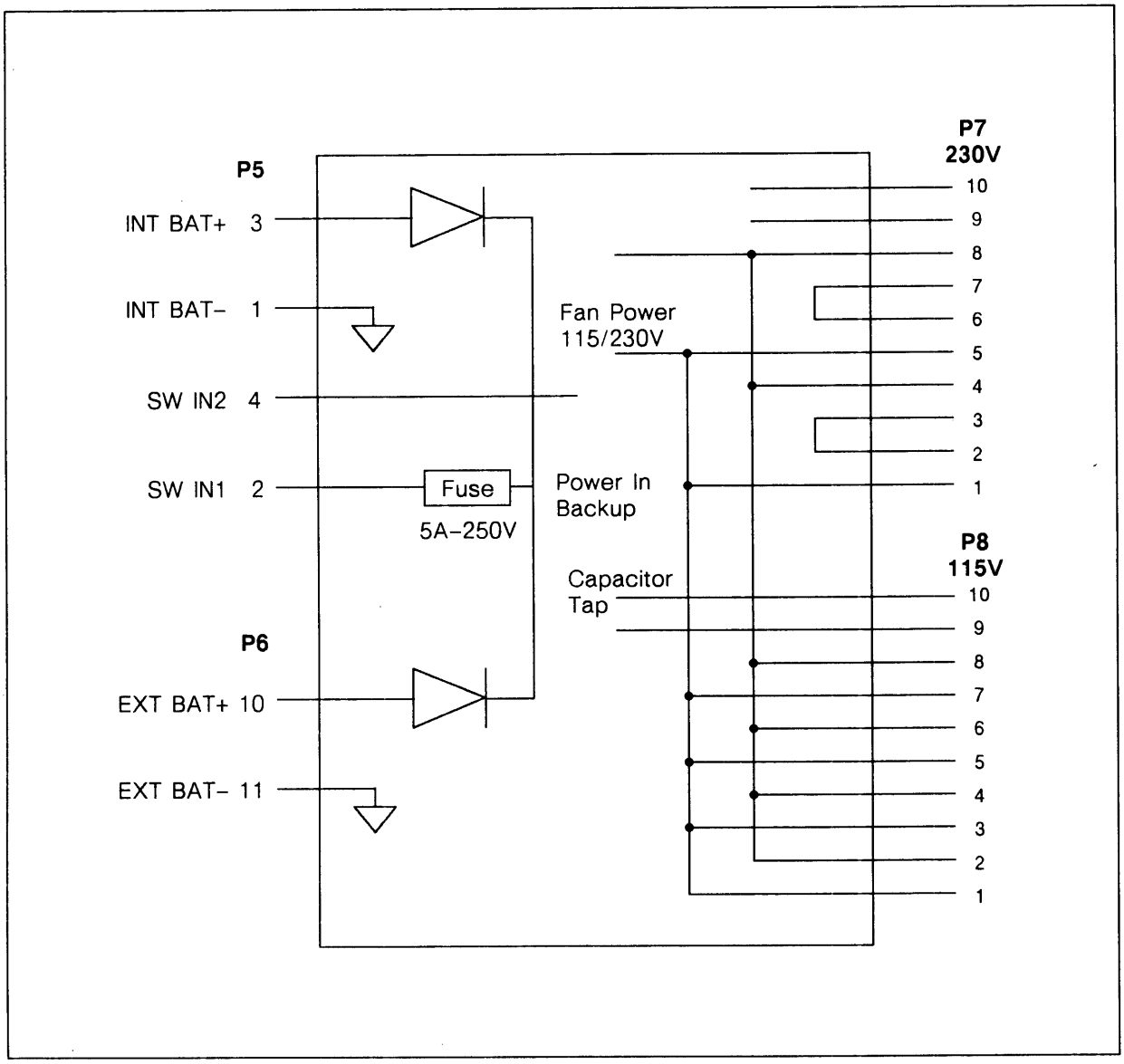


Figure 8-12. 440-Watt Power Supply Connector Diagram

Table 8-12. Electrical Connections (440W Supply)

P1 - DC Output Connector: (PC Edge Board)

Pin Number	Signal Name
1 thru 36	+5.1 Volts DC
37 thru 50	Common

P2 - DC Output Connector: (PC Edge Board)

Pin Number	Signal Name
1 thru 28	Common
29 thru 32	+12 Volts DC
33, 34	-12 Volts DC
35 thru 38	+5.1 Volt Memory Backup
39 thru 42	25 kHz Phase 1
43 thru 46	25 kHz Phase 2
47	PON+
48	PFW-
49	MLOST-
50	+5.1 Volts Memory Sense

P5 - Battery Switch Connector:

Pin Number	Signal Name
2	Switch in 1
4	Switch in 2
1	Internal Battery -
3	Internal Battery +

P9 - AC Line Input:

Pin Number	Signal Name
1	AC Line
2	No Connection
3	AC Neutral

Table 8-12. Electrical Connections (440W Supply) (Continued)

P7/P8 - AC Line Configuration / Fans:

Pin Number	Signal Name
1	Fan #1
2	Fan #1
3	Fan #2
4	Fan #2
5	Fan #3
6	Fan #3
7	Fan #4
8	Fan #4
9	230V / 115V
10	230V / 115V

P6 - Test Points / External Battery:

Pin Number	Signal Name
1	+5V Test
2	+12V Test
3	-12V Test
4	+5VM Test
5	PON+
6	PFW-
7	MLOST-
8	25 kHz Test
9	25 kHz Test
10	Battery +
11	Battery -
12	Common

Electrical Specifications

The electrical specifications of the 440-Watt power supply are provided below in several tables. AC line input specifications are given in Table 8-13, battery input specifications are given in Table 8-14, and power supply output specifications are given in Table 8-15.

Table 8-13. Input Electrical Specifications (440W Supply)

AC Line Specifications:

These specifications do not include the power required for the fans.

	Min	Nominal	Max	
Range 1				
Voltage	84	120	140	Volts RMS
RMS Current (Max)	9.4	7.2	6.2	Amps
Inrush	-	-	100	Amps
Range 2				
Voltage	176	230	278	Volts RMS
RMS Current (Max)	4.7	3.7	3.1	Amps
Inrush	-	-	100	Amps
Carry Over	10.6	-	-	milliseconds
PFW Trip Point				
Range 1	-	-	84	Volts RMS
Range 2	-	-	176	Volts RMS
Line Frequency	47	60	67	Hz
Line Fuse	-	-	10.0	Amps
Input Power	-	-	700	Watts
Power Factor	.6			

Note: Power supply operation permits input transients of up to 3000V for periods of less than 10 microseconds.

Table 8-14. Battery Input Specifications (440W Supply)

	Minimum	Nominal	Maximum
Battery Voltage	10.0	12.0	14.4 Volts
Discharge, Continous	-	-	40.0 Amps
Internal Resistance	-	10.0	- mOhms

Note: 10.0V is the approximate input disconnect voltage. Disconnect occurs when Output #1 (5.1V) drops to 4.9V, as measured at the battery backup board (coincident with the assertion of MLOST–).

Table 8-15. Output Electrical Specifications (440W Supply)

Maximum Dynamic Load: 10% of load over 10 microseconds

Output Stress Conditions Allowed:

a. The power supply will recover from a short to ground or to another regulated output. Shorted outputs will cause the power supply to turn off; the AC line must be recycled to resume normal operation.

b. Over-rated operated temperature and excessive ambient temperature.

Output Regulation:

Output #1 – Nominal Voltage = 5.1 Volts
Maximum Current = 70 Amps (1) (3)
Maximum Ripple = 0.1 Volt

Regulation: 0.0 to 3.0 Amps +/– 10%
3.0 to 6.2 Amps +/– 5%
6.2 to 70.0 Amps +/– 2%

Output #2 – Nominal Voltage = 12.0 Volts
Maximum Current = 5.6 Amps (3)
Maximum Ripple = –12 Volts

Regulation: 0.0 to .03 Amps +/– 10%
.03 to 5.6 Amps +6% / – 3%

Output #3 – Nominal Voltage = –12.0 Volts
Maximum Current = 3.5 Amps (3)
Maximum Ripple = 0.12 Volt

Regulation: 0.0 to .10 Amps +/– 12%
.10 to 3.5 Amps +/– 6%

Table 8-15. Output Electrical Specifications (440W Supply) (Continued)

Output #4 (opt.) –
Nominal Voltage = 5.1 Volts
Maximum Current = 10.0 Amps (2)
Maximum Ripple = 0.1 Volt

Regulation:
0.0 to .10 Amps +/- 10%
.10 to 10.0 Amps +/- 2%

Output #5 –
Nominal Voltage = 39 Volts RMS
Split Phase = 19.5 Volts RMS
Maximum Current = 1.5 Amps

Regulation:
0.0 to .02 Amps +10% / -12%
.02 to 1.5 Amps +/- 8%

Output #6 – Battery Charger

Minimum Current < .050 Amps (4)
Maximum Current = .200 Amps
Maximum Voltage = 14.4 Volts

Output #7 – Fan Power

Nominal Voltage = 115 Volts RMS
Maximum Current = 1.25 Amps

Notes:
(1) When no battery backup module is installed, the Output #4 current is supplied by Output #1. The total current drawn from Output #1 will not exceed 70 Amps.

(2) Output #4 shall be limited to 7 Amps when the battery backup is selected.

(3) The power supply shall not deliver more than the maximum current +20%. The power supply shall turn off if the maximum current +20% is exceeded.

(4) When the battery is fully charged.

Environmental Specifications

The environmental specifications of the 440-Watt power supply are provided in Table 8-16.

Table 8-16. Environmental Specifications (440W Supply)

Non-Operating Temperature:	-40° to 75°C (-40° to 167°F)
Operating Temperature:	0° to 55°C (32° to 131°F)
(Type Tested to ensure margins	-5° to 60°C (23° to 140°F))
Operating Survival Temperature:	-20° to 65°C (-4° to 149°F)
Operating Humidity:	5% to 95% at 40°C wet bulb temperature

Vibration:

Sweep
From 5 to 55 Hz and back at a rate of one octave per minute, with an excursion of .025″, for 15 minutes.

Resonance
At each resonant point, not to exceed 4 points, dwell for 10 minutes at the following excursions:

5 - 10 Hz	.125″
11 - 25 Hz	.060″
25 - 55 Hz	.025″

Shock:

30g peak force applied as an 11-millisecond half-sine pulse. To be tested 3 times
in each direction of each axis (18 tests).

Altitude:

Full operating temperature, at 300 Watts output power (not including fan power), at altitudes up to 10,000 feet. From 10,000 feet to 15,000 feet, a linear derating of 2°C per 1,000 feet is allowed. The power supply will survive a 50,000 foot non-operating altitude.

HP 12154A Battery Backup Module

The HP 12154A battery backup module for the Micro/1000 computers is designed to provide current that will retain the current status of the system in memory if AC power is interrupted. The HP part number for this card is 12154-60001. The schematic for this card is shown in Figure 8-13.

Configuration

The battery backup module is installed in the 16-slot backplane of the Micro/1000. The sixth, seventh, and eighth physical slots down from the top of the left side of the card cage are dedicated to the battery backup module. There are three slots reserved to allow for the height of the batteries and the space necessary for component heat sinks.

Physical Description

The module (or card) dimensions are the following:

Width: 171 mm (6.75 in) Standard card width

Depth: 324 mm (12.75 in) Attaches to bulkhead connector panel

Max. Component Height: 51mm (2.0 in) for D-size battery packs

Electrical Specifications

The module is comprised of the battery charging circuit, enable/disable circuit, D-size battery pack, and a control circuit. When power is present, the module will charge the 9.6V Nicad (nickel/cadmium) batteries. When power fails, the 9.6V battery voltage is reduced to 5.1V through the regulator, and supplies the +5M power line to sustain memory.

The module derives its power from the 12V DC output of the system power supply. When the voltage of the batteries drops below 8.0V, the module will inhibit the +5.1V memory regulator circuit.

Theory of Operation

The internal battery pack is charged from both 28V and 12V. The 12V backplane voltage is used to provide a heavy charge for discharged batteries. As the batteries charge to about 11.3V, the 28V supply is used as a trickle charger. The input selector is essentially three diodes that select the highest input voltage. Note that the 28V supply would be the normal input, until a power fail when the batteries would become the input. This is important because the output of this charger/comparator circuit, +5VM, is produced by the circuitry on the battery backup PCA. Thus, to troubleshoot the failing component (that is, the battery pack or PCA) if memory is not being sustained when the battery backup is enabled and power is off, disable the battery pack by turning off the battery enable switch on the front panel and turning on the power. If the +5VM is present, then the battery pack is probably at fault (providing the 28V and 5V voltages are present).

The DC-to-DC converter, coupled with the control circuit, make this a switching power supply. The control block switches the DC input voltage to maintain a pulse width with a constant amount of power. For example, a 28V input will have a tall narrow pulse, an 8V input will have a low wide pulse. The pulses feed an inductor that creates a constant voltage output for a capacitor-resistor integrator that produces the +5VM. This supply will stop if the battery voltage drops below 8V (to protect the Nicad batteries) and will shut down if an overcurrent condition exists. The 2.5V reference has a +/– accuracy of 0.5%. The feedback circuit drives the control block to regulate the pulse width of the DC-to-DC converter. Overall voltage regulation is 2%.

The battery charger circuit consists of four parts. Diode CR2 is connected to the +12V supply and to 10-ohm resistor R2. R2 is connected to the positive side of the battery. Diode CR1 is similarly connected to +28V and 100-ohm resistor R1 which is also connected to the positive battery connection. Diode CR2 conducts until the battery voltage approaches 11.3V. CR2 becomes reverse biased and CR1 now trickle charges the battery. Because of the simplicity of this scheme, if a battery does not retain a charge, the battery pack is probably faulty.

Also on the front of this PCA are two LEDs, one green and one red. The red LED indicates that an overcurrent or overvoltage condition has occurred and the battery backup card is shut down. This could be caused by a short in the +5VM line that goes to memory. Either a memory PCA, a processor PCA, or the backplane could be faulty, as well as the battery backup PCA itself. To reset after isolating and repairing the problem, turn off the battery enable switch, turn off the power, then turn both back on.

The green LED indicates that the +5VM is within specifications. If both red and green LEDs are on, the battery backup PCA is faulty. As long as the green LED is on, the memory is being sustained.

Parts List

Parts for the HP 12154A are listed in Table 8-17 and the parts manufacturer's names and addresses are listed in Table 8-18. A parts location diagram for the module is shown in Figure 8-14.

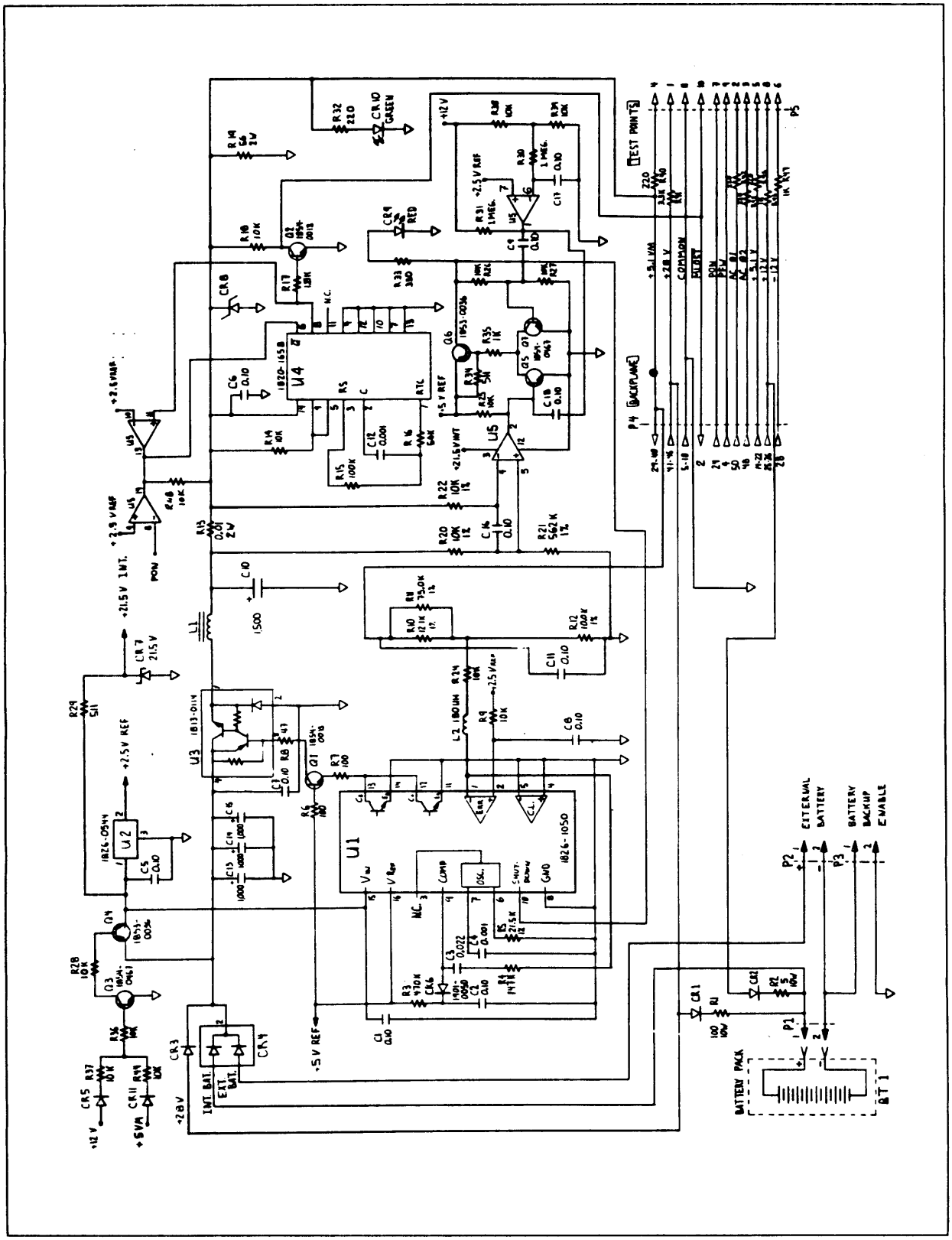


Figure 8-13. HP 12154A Battery Backup Module Schematic

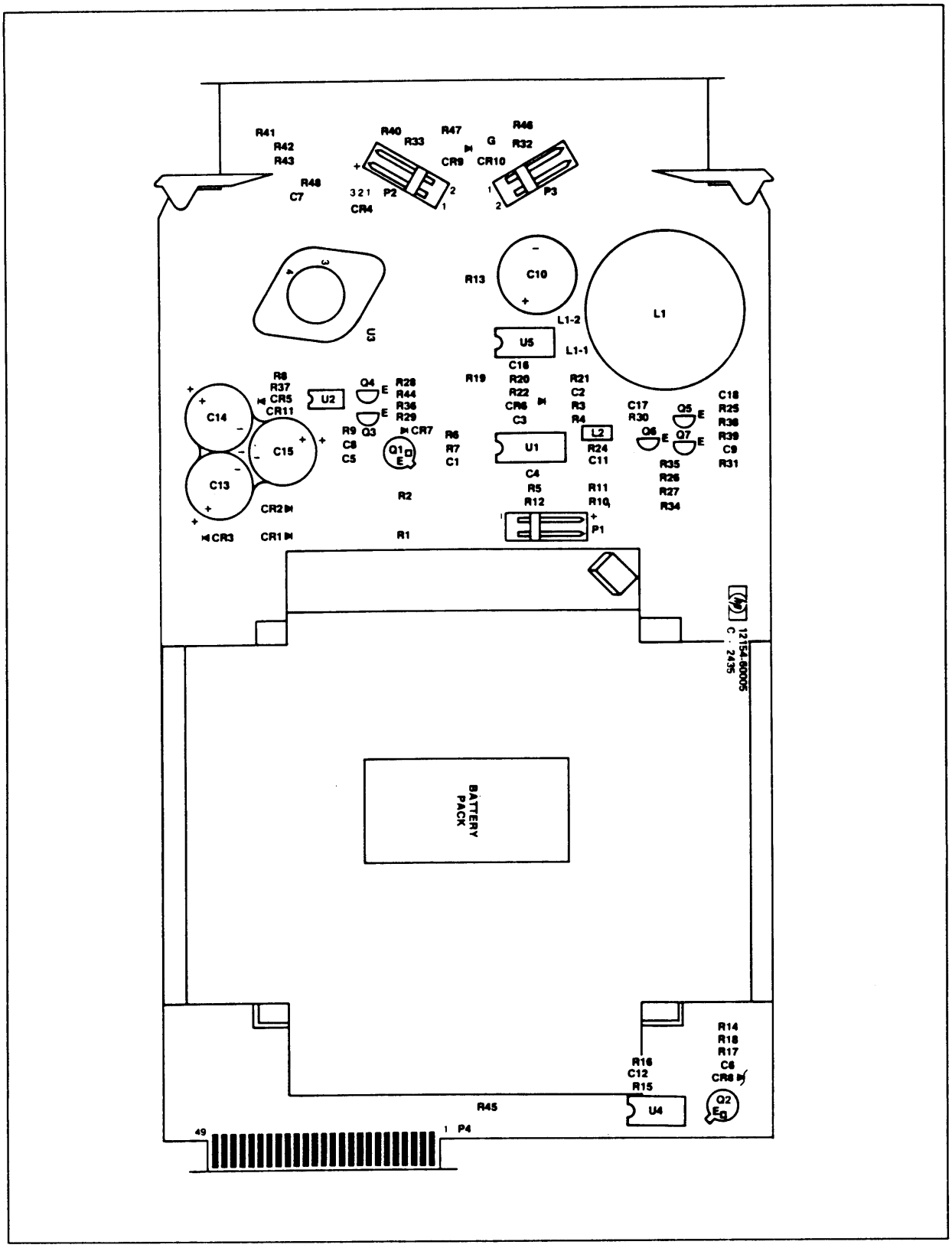


Figure 8-14. HP 12154A Parts Location Diagram

Table 8-17. HP 12154A Parts List (Sheet 1 of 2)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
	12154-60005	7	1	PCA-BACKUP	28480	12154-60005
C1	0160-4835	7	11	CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C2	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C3	0160-4833	5	1	CAPACITOR-FXD .022UF +-10% 100VDC CER	28480	0160-4833
C4	0160-4847	1	2	CAPACITOR-FXD 1000PF +-10% 100VDC CER	28480	0160-4847
C5	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C6	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C7	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C8	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C9	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C10	0180-2987	8	1	CAPACITOR-FXD 1500UF+100-10% 25VDC AL	56289	674D158H025HJ5A
C11	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C12	0160-4847	1		CAPACITOR-FXD 1000PF +-10% 100VDC CER	28480	0160-4847
C13	0180-3019	9	3	CAPACITOR-FXD 1000UF+50-10% 50VDC AL	28480	0180-3019
C14	0180-3019	9		CAPACITOR-FXD 1000UF+50-10% 50VDC AL	28480	0180-3019
C15	0180-3019	9		CAPACITOR-FXD 1000UF+50-10% 50VDC AL	28480	0180-3019
C16	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C17	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C18	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
CR1	1901-0673	6	3	DIODE-PWR RECT 100V 5A SUS	03508	A15A
CR2	1901-0673	6		DIODE-PWR RECT 100V 5A SUS	03508	A15A
CR3	1901-0673	6		DIODE-PWR RECT 100V 5A SUS	03508	A15A
CR4	1906-0265	2	1	DIODE-RECT.	28480	1906-0265
CR5	1901-0050	3	2	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR7	1902-3245	6	1	DIODE-ZNR 21.5V 5% DO-35 PD=.4W	28480	1902-3245
CR8	1902-0839	9	1	DIODE-ZNR 5V PD=5W TC=+.06% IR=300UA	11961	1N5908
CR9	1990-0486	6	1	LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
CR10	1990-0485	5	1	LED-LAMP LUM-INT=600UCD IF=30MA-MAX	28480	5082-4984
CR11	1901-0460	9	1	DIODE-STABISTOR 30V 150MA DO-7	28480	1901-0460
L1	9140-0811	8	1	INDUCTOR 350UH 10% 1.70X1.2LG	28480	9140-0811
L2	9100-2279	2	1	INDUCTOR RF-CH-MLD 180UH 10% .105DX.28LG	28480	9100-2279
Q1	1854-0013	7	2	TRANSISTOR NPN 2N2218A SI TO-5 PD=800MW	04713	2N2218A
Q2	1854-0013	7		TRANSISTOR NPN 2N2218A SI TO-5 PD=800MW	04713	2N2218A
Q3	1854-0467	5	3	TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	03508	2N4401
Q4	1853-0535	8	2	TRANSISTOR PNP SI TO-92 PD=350MW	02041	SPS8929
Q5	1854-0467	5		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	03508	2N4401
Q6	1853-0535	8		TRANSISTOR PNP SI TO-92 PD=350MW	02041	SPS8929
Q7	1854-0467	5		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	03508	2N4401
R1	0811-3644	5	1	RESISTOR 100 10% 10W PW TC=0+-300	28480	0811-3644
R2	0811-3656	9	1	RESISTOR 5 10% 10W PW TC=0+-300	28480	0811-3656
R3	0683-4745	6	1	RESISTOR 470K 5% .25W FC TC=-800/+900	01121	CB4745
R4	0698-3452	1	1	RESISTOR 147K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1473-F
R5	0757-0199	3	1	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R6	0683-1015	7	2	RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R7	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R8	0683-4705	8	1	RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R9	0683-1035	1	13	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R10	0757-0444	1	1	RESISTOR 12.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1212-F
R11	0757-0462	3	1	RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7502-F
R12	0757-0442	9	4	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4 1/8-T0-1002-F
R13	0811-3511	5	1	RESISTOR .01 1% 2W PWW TC=0+-150	28480	0811-3511
R14	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R15	0683-1045	3	1	RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
R16	0683-5635	5	1	RESISTOR 56K 5% .25W FC TC=-400/+800	01121	CB5635
R17	0683-1825	7	1	RESISTOR 1.8K 5% .25W FC TC=-400/+700	01121	CB1825
R18	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R19	0764-0013	5	1	RESISTOR 56 5% 2W MO TC=0+-200	28480	0764-0013
R20	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F

Table 8-17. HP 12154A Parts List (Sheet 2 of 2)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
R21	0698-8824	1	1	RESISTOR 562K 1% .125W F TC=0+-100	28480	0698-8824
R22	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R24	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R25	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R26	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R27	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R28	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R29	0757-0416	7	2	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R30	0683-1055	5	2	RESISTOR 1M 5% .25W FC TC=-800/+900	01121	CB1055
R31	0683-1055	5		RESISTOR 1M 5% .25W FC TC=-800/+900	01121	CB1055
R32	0683-2215	1	5	RESISTOR 220 5% .25W FC TC=-400/+800	01121	CB2215
R33	0683-3315	4	1	RESISTOR 330 5% .25W FC TC=-400/+800	01121	CB3315
R34	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R35	0683-1025	9	3	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R36	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R37	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R38	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R39	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R40	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+800	01121	CB2215
R41	0683-3325	6	1	RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
R42	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+800	01121	CB2215
R43	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+800	01121	CB2215
R44	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R45	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+800	01121	CB2215
R46	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R47	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R48	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
TP1	1251-3917	8	3	CONNECTOR 2-PIN M POST TYPE	28480	1251-3917
TP2	1251-3917	8		CONNECTOR 2-PIN M POST TYPE	28480	1251-3917
TP3	1251-3917	8		CONNECTOR 2-PIN M POST TYPE	28480	1251-3917
U1	1826-1050	5	1	IC V RGLTR-SWG 4.9/5.1V 16-DIP-P PKG	28480	1826-1050
U2	1826-0544	0	1	IC V RGLTR-V-REF-FXD 2.5V 8-DIP-C PKG	28480	1826-0544
U3	1813-0114	3	1	IC V RGLTR TO-3	12969	PIC646
U4	1820-3516	0	1	IC TIMER CMOS	28480	1820-3516
U5	1826-0138	8	1	IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N
	0330-0377	5	2	INSULATION-POLYU .25-IN-THK 3.2-IN-WD	02918	
	0340-0703	2	1	INSULATOR-XSTR MICA	28480	0340-0703
	0361-1072	4	4	RIVET-BLIND PL-STEM DOME-HD .156DIA	02570	AAP-52
	0380-0342	9	5	STANDOFF-RVT-ON .125-IN-LG 6-32THD	00000	ORDER BY DESCRIPTION
	0403-0289	3	2	EXTR-PC BD RED POLYC .063-BD-THKNS	28480	0403-0289
	0590-0157	9	1	NUT-HEX-PLSTC LKG 6-32-THD .178-IN-THK	28480	0590-0157
	0890-1159	9	1	TUBING-HS 1.5-D/.75-RCVD .045-WALL PVC	28480	0890-1159
	1420-0321	1	1	BATTERY ASSEMBLY 9.6V NOM; RECHARGEABLE	28480	1420-0321
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
	2200-0728	7	1	SCREW-MACH 4-40 .312-IN-LG PAN-HD-SLT	00000	ORDER BY DESCRIPTION
	2360-0113	2	4	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	2360-0117	6	3	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	2360-0119	8	2	SCREW-MACH 6-32 .438-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	2360-0302	1	1	SCREW-MACH 6-32 1.625-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	3050-1105	0	1	WASHER-SPR BLVL NO. 8 .187-IN-ID	01113	
	8040-0239	9	1	LUBRICANT-GREASE SIL	05820	120
	12154-00001	7	1	HEAT SINK	28480	12154-00001
	7121-2061	2	1	LABEL-INFORMATION .15-IN-WD .5-IN-LG	28480	7121-2061
	12154-00002	8	1	BATTERY BOX	28480	12154-00002
	12154-00003	9	1	COVER-BATT. BOX	28480	12154-00003
	12154-80001	5	1	PCB-BATT. BACKUP	28480	12154-80001
	12154-80003	7	1	LABEL-WARNING	28480	12154-80003
	ET16770	3	1	RPR BTRY BKUP	28480	ET16770
	ET16797	4	1	3060 TEST UNIT	28480	ET16797

Table 8-18. Manufacturer's Code List

MFR Number	Manufacturer Name	Address	Zip Code
01121	Allen-Bradley Co	Milwaukee, WI	53204
01295	Texas Instr Inc Semicond Cmpnt Div	Dallas, TX	75222
03508	GE Co Semiconductor Prod Dept	Auburn, NY	13201
04713	Motorola Semiconductor Products	Phoenix, AZ	85008
11236	CTS of Berne Inc	Berne, IN	46711
11961	Semicon Inc	Burlington, MA	01803
12969	Unitrode Corp	Watertown, MA	02172
24546	Corning Glass Works (Bradford)	Bradford, PA	16701
28480	Hewlett-Packard Co. Corporate Hq	Palo Alto, CA	94304
31585	RCA Corp Solid State Div	Somerville, NJ	08876
56289	Sprague Electric Co.	North Adams, MA	01247
75915	Littlefuse Inc	Des Plaines, IL	60016

HP 12159A 25 kHz Power Module

The HP 12159A is a module that takes the 25 kHz square-wave power from the 300-Watt power supply and provides 25 kHz sine-wave power to the 16-slot backplane of a Micro/1000 computer for distribution to certain I/O cards having on-card power supplies. The module plugs into slot 8 of the backplane, and does not need forced air flow for cooling. The HP part number for this module is 12159-60001.

Specifications

The HP 12159A electrical specifications are provided in Table 8-19, and the connector pin definitions are listed in Table 8-20.

Theory of Operation

For this theory of operation, refer to the schematic shown in Figure 8-15. The input transformer T1 steps the input 24 volt peak-to-peak square wave up to 114 volts peak-to-peak across 3-6. The winding 5-6 regulates the output as described below.

L1, L2, C1, and C2 are the main harmonic filters of the square wave. The regulator coil L3 also contributes to filtering.

Components R1, R2, C3, and C4 attenuate the noise generated by the switching diodes CR1 and CR2.

The regulator limits the amplitude of the output sine wave to less than 59 volts and imposes no minimum value. The output of CR1, CR2, and C5 is the peak of the output sine wave. If this voltage exceeds 26 volts (zener diode CR3 voltage) plus the 6-E drops across Q1 and Q2, then a current flows into the base of Q1, causing current flow through CR4 and Q2. This current adds to the main circuit current through L3, causing a voltage drop across L3. This voltage drop is a strong function of excessive output voltage which has the effect of providing regulation.

The regulator clamps the output to be less than or equal to the sum of the zener voltage plus the 6-E drops of the transistors.

Parts List

Parts for the 12159A are listed in Table 8-21 and the names and addresses of the parts manufacturers are listed in Table 8-22. The parts locations are shown in Figure 8-16.

Table 8-19. HP 12159A 25 kHz Module Electrical Specifications

Input Specifications:

	Min	Nominal	Max	
Phase to Phase	11.28	12.00	12.72	Volts RMS
RMS Current (max)	0.00	–	3.20	Amps
Frequency	24	25	32	kHz
Input Power	–	–	36	Watts

Output Specifications:

Maximum output power	30 Watts
Maximum distortion	10% total harmonic distortion
Maximum dynamic load change	10% of load over 10 microseconds

Output Stress Conditions:

The module will recover, with no permanent damage from a shorted regulated output (it may be necessary to replace the fuse to resume normal operation).

Output Loading:

The load on the 25 kHz module can be applied from phase-to-phase (39 Vrms) or from phase-to-common (19.5 Vrms). Up to one-half of the maximum rated power can be drawn from each phase (phase-to-common) or up to all of the rated power can be drawn phase-to-phase as long as the total power does not exceed the maximum rated power. The phase-to-common load need not be balanced between the two phases.

Regulated Output Specifications:

Nominal Voltage	39 Volts RMS	
Split Phase	19.5 Volts RMS	
Maximum current	0.84 Amps	
Regulation	0.0 to 0.02 Amps	+10% / −12%
	0.02 to 0.84 Amps	+/− 8%

Table 8-20. HP 12159A Electrical Connector (P1) Pin Definitions

Pin	Signal Name
11 - 14	25 kHz 1
15 - 18	25 kHz 2
19 - 22	GND
23 - 26	ACϕ2 (phase 2)
27 - 30	ACϕ1 (phase 1)

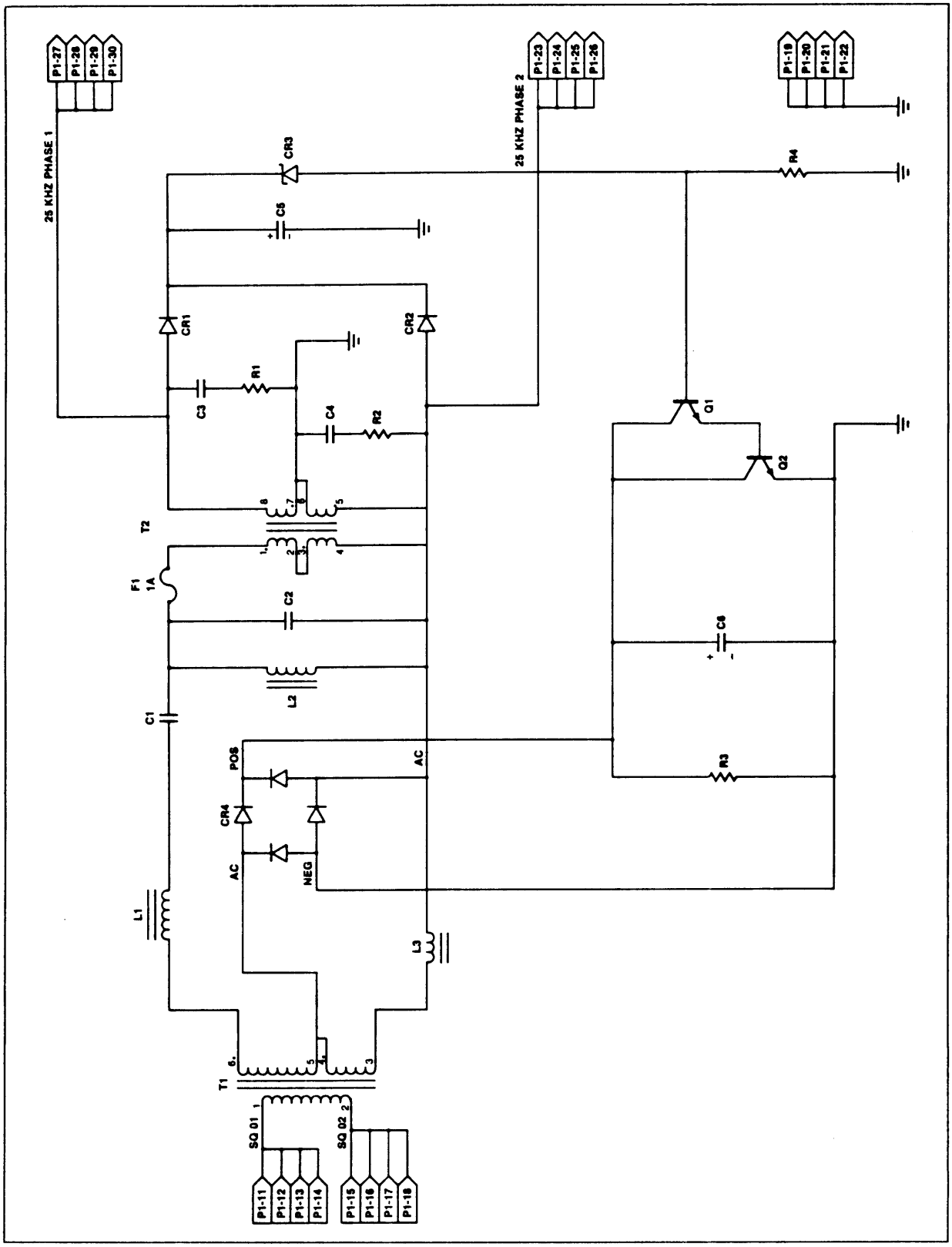


Figure 8-15. HP 12159A 25 kHz Power Module Schematic

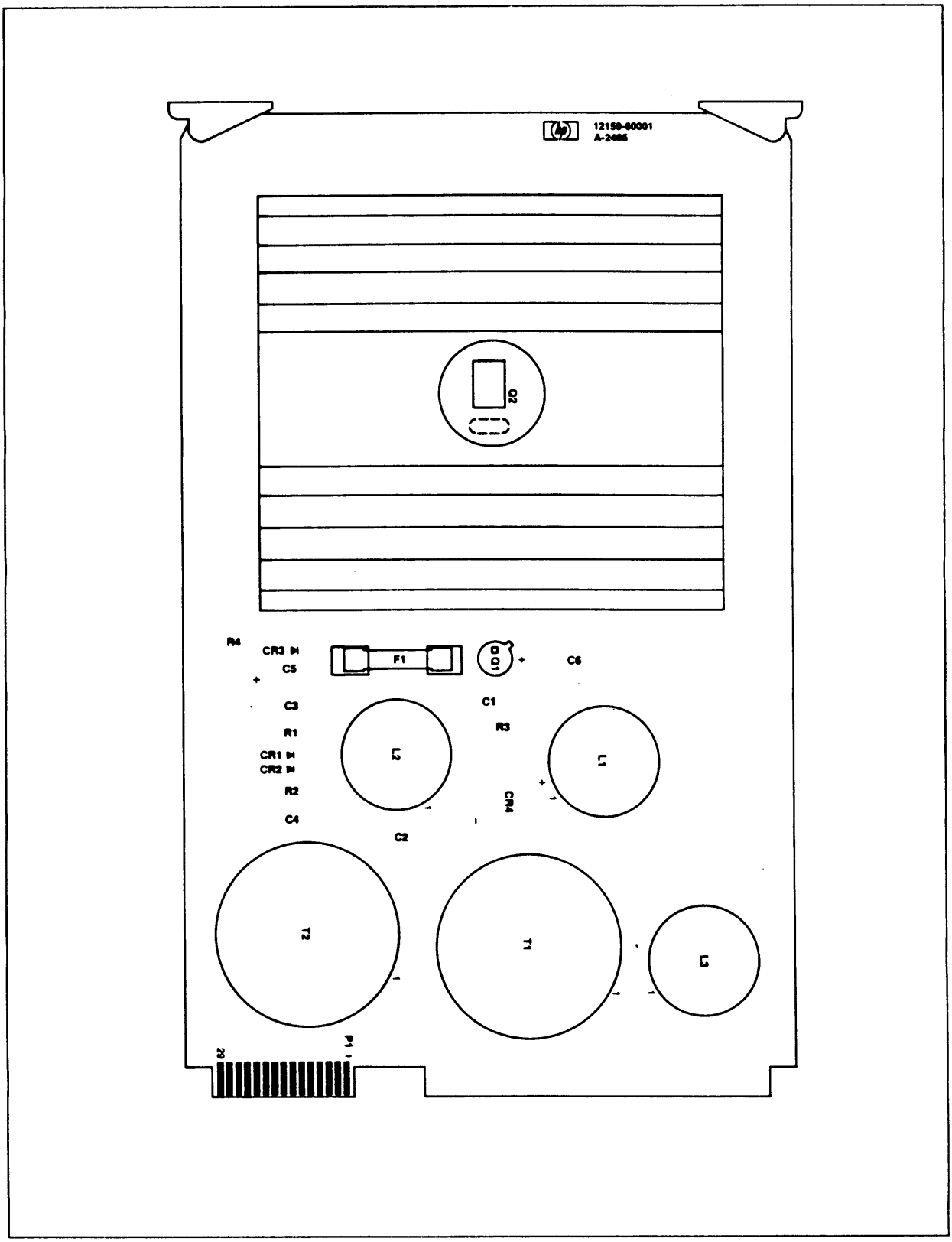


Figure 8-16. HP 12159A Parts Locations

Table 8-21. HP 12159A Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12159-60001	8	1	PCA-25KHZ	28480	12159-60001
C1	0160-6040	8	2	CAP 0.1 UF	28480	0160-6040
C2	0160-6040	8		CAP 0.1 UF	28480	0160-6040
C3	0160-0161	4	2	CAPACITOR-FXD .01UF +-10% 200VDC POLYE	28480	0160-0161
C4	0160-0161	4		CAPACITOR-FXD .01UF +-10% 200VDC POLYE	28480	0160-0161
C5	0180-0269	5	1	CAPACITOR-FXD 1UF+50-10% 150VDC AL	56289	30D105G150BA2
C6	0180-0141	2	1	CAPACITOR-FXD 50UF+75-10% 50VDC AL	56289	30D506G050DD2
CR1	1901-0096	7	2	DIODE-SWITCHING 120V 50MA 100NS	28480	1901-0096
CR2	1901-0096	7		DIODE-SWITCHING 120V 50MA 100NS	28480	1901-0096
CR3	1902-3269	4	1	DIODE-ZNR 26.1V 2% DO-35 PD=.4W	28480	1902-3269
CR4	1906-0077	4	1	DIODE-FW BRDG 400V 5A	28480	1906-0077
F1	2110-0001	8	1	FUSE 1A 250V NTD 1.25X.25 UL	75915	312001
L1	9140-0863	8	1	IND-FXD 240UH	28480	9140-0863
L2	9140-0861	8	1	IND-FXD 335 UH	28480	9140-0861
L3	9140-0862	9	1	IND-FXD 95UH	28480	9140-0862
Q1	1854-0079	5	1	TRANSISTOR NPN 2N3439 SI TO-5 PD=1W	3L585	2N3439
Q2	1854-0727	8	1	TRANSISTOR NPN 2N6474 SI TO-220AB PD=40W	3L585	2N6474
R1	0698-3628	5	2	RESISTOR 100 5% 2W MO TC=0+-200	28480	0698-3628
R2	0698-3628	5		RESISTOR 100 5% 2W MO TC=0+-200	28480	0698-3628
R3	0683-2735	8	1	RESISTOR 27K 5% .25W FC TC=-400/+600	01121	CB2735
R4	0683-2215	1	1	RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
T1	9140-0859	4	1	XFMR	28480	9140-0859
T2	9140-0860	7	1	XFMR	28480	9140-0860

Table 8-22. Manufacturer's Code List

MFR Number	Manufacturer Name	Address	Zip Code
00000	Any Satisfactory Supplier		
01121	Allen-Bradley Co	Milwaukee, WI	53204
01295	Texas Instr Inc Semicond Cmpnt Div	Dallas, TX	75222
03888	K D I Pyrofilm Corp	Whippany, NJ	07981
04713	Motorola Semiconductor Products	Phoenix, AZ	85008
07263	Fairchild Semiconductor Div	Mt. View, CA	94042
07910	Teledyne Semiconductor	Hawthorne, CA	90250
11236	CTS of Berne Inc	Berne, IN	46711
11961	Semicon Inc	Burlington, MA	01803
14936	General Instr Corp Semicon Prod Gp	Hicksville, NY	11802
19701	Mepco/Electra Corp	Mineral Wells, TX	76067
24546	Corning Glass Works (Bradford)	Bradford, PA	16701
27014	National Semiconductor Corp	Santa Clara, CA	95051
28480	Hewlett-Packard Co. Corporate Hq	Palo Alto, CA	94304
32293	Intersil Inc	Cupertino, CA	95014
34335	Advanced Micro Devices Inc	Sunnyvale, CA	94086
34649	Intel Corp	Mt. View, CA	94043
50088	Mostek Corp	Carrollton, TX	75006
50364	Monolithic Memories Inc	Sunnyvale, CA	94086
56289	Sprague Electric Co	North Adams, MA	01247

25 kHz Backplane Power Applications

25 kHz backplane power can be used when designing special interfaces on the 12010A Breadboard Interface to provide AC input power for compact, lightweight on-interface DC power supplies to meet any of the following requirements.

1. Provision of DC voltages in addition to those supplied by the power supply.
2. Provision of DC supplies whose analog grounds are isolated from the computer ground.
3. Provision of multichannel isolated power to digital communication circuits to eliminate ground noise paths and maximize the reliability of serial data transfers.
4. Low voltage, high current power for supplying large arrays of integrated circuits.

Non-Isolated Power Supply

Purpose and Basic Design

Where additional +7.5V to +12V DC at up to 1 amp is needed for interface circuits, the 25 kHz backplane power can be used to provide a non-isolated positive regulated power supply as shown in Figure 8-14. The 19.5V rms potential on either side of common provides at least +15.4V DC after rectification and filtering. An adjustable, off-the-shelf, three-terminal integrated circuit voltage regulator (National Semiconductor Series LM11 7 or equivalent) can be used to set the regulated output voltage within the range of +7.5V to +12V DC. The regulated voltage output is dependent upon the values of resistors R2 and R3. A negative output voltage supply similar to the positive supply shown in Figure 8-17 can be made by reversing the polarities of the rectifiers and using a negative adjustable regulator (National Semiconductor Series LM137 or equivalent).

Preserving Purity of Input Sine Wave

To maintain the purity of the input 25 kHz sine wave, near 180-degree conduction should be provided in the rectification process, which necessitates the use of a choke input filter. This filter also limits the surge current at turn-on if the requirements for L_{min} are met. The equation for L_{min} with a 25% safety factor is given by:

$$L_{min} \text{ (in henries)} = (K/fs) \times Rl$$

where: fs = 25 kHz
Rl = Minimum load resistance
K = 0.06 for full wave rectifiers

This implies the need for a minimum load. If the circuits to be powered allow the load current to go to zero, a preloading bleeder resistor is required. The final value of L_{min} would then be determined by the allowed power loss (dissipation) of the preloading resistor. When the L_{min} requirement is met, the surge current will be acceptable and sine wave distortion will be minimized.

Rectifier Selection

Rectifiers used with 25 kHz input power must be of the fast recovery type with less than 200 nanosecond recovery time. Allowing for possible transients from leakage instances, overshoot, and MTBF derating, the rectifiers should also have 100V peak inverse voltage rating.

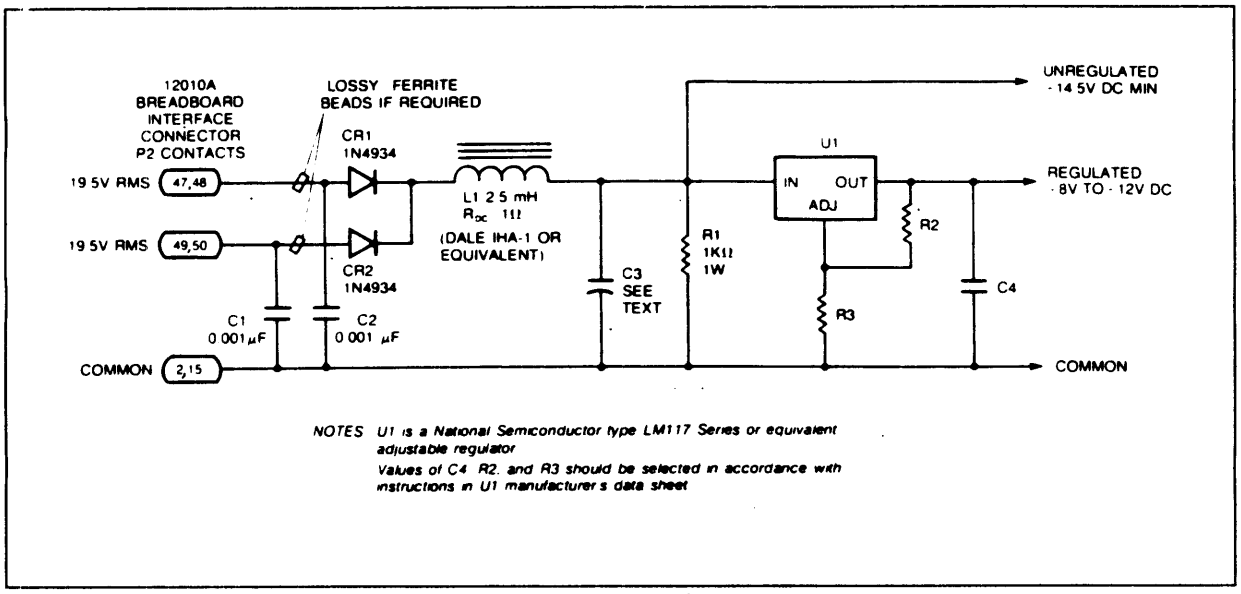


Figure 8-17. On-Interface Regulated Power Supply

Input Noise Reduction

During rectifier recovery, the removal of stored charge in the rectifiers will appear as spikes on the rectifier inputs. These spikes should be suppressed to keep them from traveling along the 25 kHz AC input lines in the backplane. Small 0.001 to 0.1 microfarad ceramic capacitors (C1 and C2 in Figure 8-17) will usually damp out these spikes, with the required capacitor value dependent upon the magnitude of stored charge being removed. If underdamped ringing is present because of leakage inductance, small ferrite beads, tubes, or toroids can be threaded onto the rectifier leads to provide a "lossy" inductive reactance at high frequencies to effectively dissipate undesirable recovery currents.

Input Filtering

The value of C3 is determined by the amount of ripple voltage that can be tolerated at the input of integrated circuit regulator U1. The Vin-Vout differential of 3 volts must be met for any chosen output voltage as noted in Reference 2. The Ripple factor (r) for a full-wave rectifier circuit is given by:

$$r = (0.83)/(L1 \times C1) \times 5.76 \times 10^{-6}$$

The case size and construction of capacitor C3 must be capable of conducting the ripple current without excessive dissipation. Ripple current will be at 2 fs and will be sinusoidal when L_{min} requirements are met. The rms ripple current in amps is given by:

$$Ir = Vrms/(4\pi \times fs \times L1)$$

where: Vrms = the input voltage phase-to-common
fs = 25 kHz
L1 >= L_{min}

The minimum inductive value of L1 must be present with the DC current flowing through it over the complete load current range. This requires an inductor with gaps in the magnetic circuit, either fixed or distributed, such as in powdered iron cores, or solenoid-wound inductors over ferrite rods (available from Reference 9).

Regulator Dissipation

Since the regulator is a linear series pass type, the difference between the voltage developed across C3 at the regulator input and the desired output at the load current must be dissipated in the regulator. This dissipation is given by:

$$P_{diss} = (V_{in} - V_{out}) \times (I_L + V_{in} I_q)$$

where: I_q = the quiescent current of the regulator.

Case to junction thermal resistances are given in the regulator manufacturer's data sheet. The dominant thermal resistance will be the case to air stream, which is usually available on heat sink manufacturer's data as a function of air velocity. You can assume a minimum 200 ft/min flow across the board with a maximum air temperature on the exit side of 66°C under worst case conditions. For low power on-card DC supplies, the copper foil on the printed circuit board can be used as a heat sink. However, the suitability of this arrangement should be checked carefully with thermocouples to confirm that the temperature rise of the regulator is not excessive.

Isolated or Floating DC Power

A major advantage of the 25 kHz backplane power is its ease of use for isolated power supplies that can have separate analog grounds, thereby reducing the effects of ground-conducted noise as discussed in References 3 and 4. Isolation is provided by an on-interface transformer, as shown in Figure 8-18. The use of 25 kHz AC input makes it possible for the isolation transformer to be very small and inexpensive. Toroidal printed circuit mounting types or "P" core (Reference 7) shielded printed circuit mounting types generally offer the best price-performance combination. However, small E-E types can also be used at lower cost with some sacrifice in electromagnetic and electrostatic shielding. High permeability ferrite materials having low losses at 25 kHz are readily available with matching bobbins and mounting hardware from References 6 through 10.

Primary-to-secondary isolation of both DC and high frequency can be somewhat complex. References 3 and 4 describe single and double shielded transformers. It is possible to achieve high isolation with small ferrite cores and proper inter-winding shield design. Simple copper foil inter-winding shields are relatively inexpensive and are effective in decreasing primary-to-secondary electrostatic coupling at frequencies from 100 Hz to about 100 kHz. For higher frequencies, "link" coupling of two cores or other techniques may be required (Reference 3). The ground isolation provided by the multi-channel +10V 30 mA power supply circuits depicted in Figure 8-18 eliminates errors caused by ground-induced noise. In analog voltage measurement applications, power supply isolation minimizes common mode noise, improving measurement accuracy. With respect to digital data transmission uses, power supply isolation allows data terminals to operate at greater distances from the local system with fewer data errors than would otherwise be possible. When the power supply is not isolated, noise in the 50/60 Hz mains power distribution and grounding system supplying the computer can cause current noise loops that degrade signal integrity.

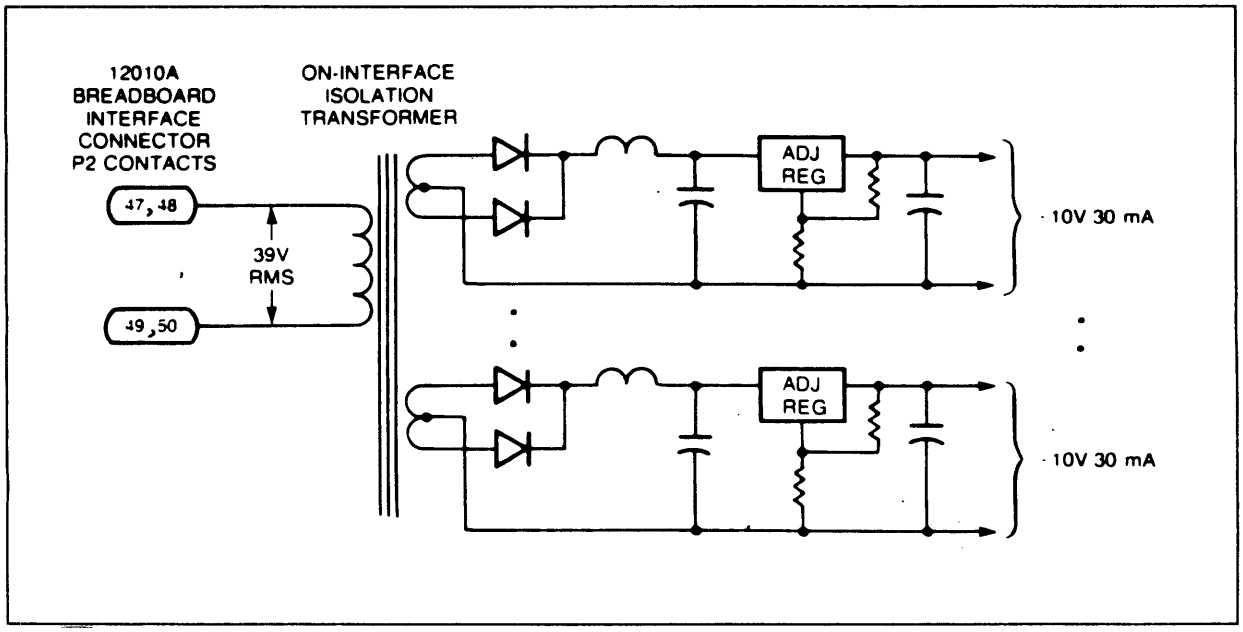


Figure 8-18. Multiple, Isolated, On-Interface Power Supplies

Low-Voltage, High-Current Power Supply

Heat dissipation is often the main factor limiting the current output of on-interface power supplies. This is particularly true for lower voltage, high current power supplies, such as required for many digital integrated circuit families. For example, at the +5V used for TTL families of integrated logic circuits, even the dissipation of the rectifiers can be a significant 40% to 20% of total power, because of the inherent 0.7V to 1.0V forward drop across silicon rectifiers, and heat sinking may be required at 3-5 Amp currents. Use of hot carrier or Schottky junction rectifiers, which have a lower forward drop presenting a power loss of only 4% to 5% of the total power output, have peak inverse voltage ratings that are suitable for lower voltage power supplies and may not require heat sinks because of their lower power dissipation.

At low output voltages, the 2-3 volt drop required across most three-terminal adjustable integrated circuit series regulators for proper regulation can account for 40% to 60% of the total power output, which is lost in the regulator and must be dissipated. Regulator heat sinking becomes difficult for even 1-3 Amp current outputs and impossible for the higher current levels that larger three-terminal regulators are able to pass. Because of these efficiency and dissipation problems, a more efficient circuit approach has evolved, as shown in Figure 8-19.

The circuit of Figure 8-19 uses a driven switching regulator for more efficient delivery of low voltage, high current output. This circuit regulates on the basis of the conduction angle of the pulsating rectified, unfiltered DC from the on-interface Schottky rectifiers. The result is efficiencies of 70% to 85% with 1 Amp to 5 Amp loads. The duty cycle control is uniform over the half sine wave and the instantaneous energy is low at the switching transitions, which minimizes waveform distortion and RFI emission. Because the regulator operates on the incoming frequency as a driven circuit, it also eliminates the generation of other frequencies that would be a problem if an on-interface switching regulator integrated circuit were used. The circuit eliminates sum and difference noise frequencies and a host of non-repetitive noise problems, while optimizing efficiency.

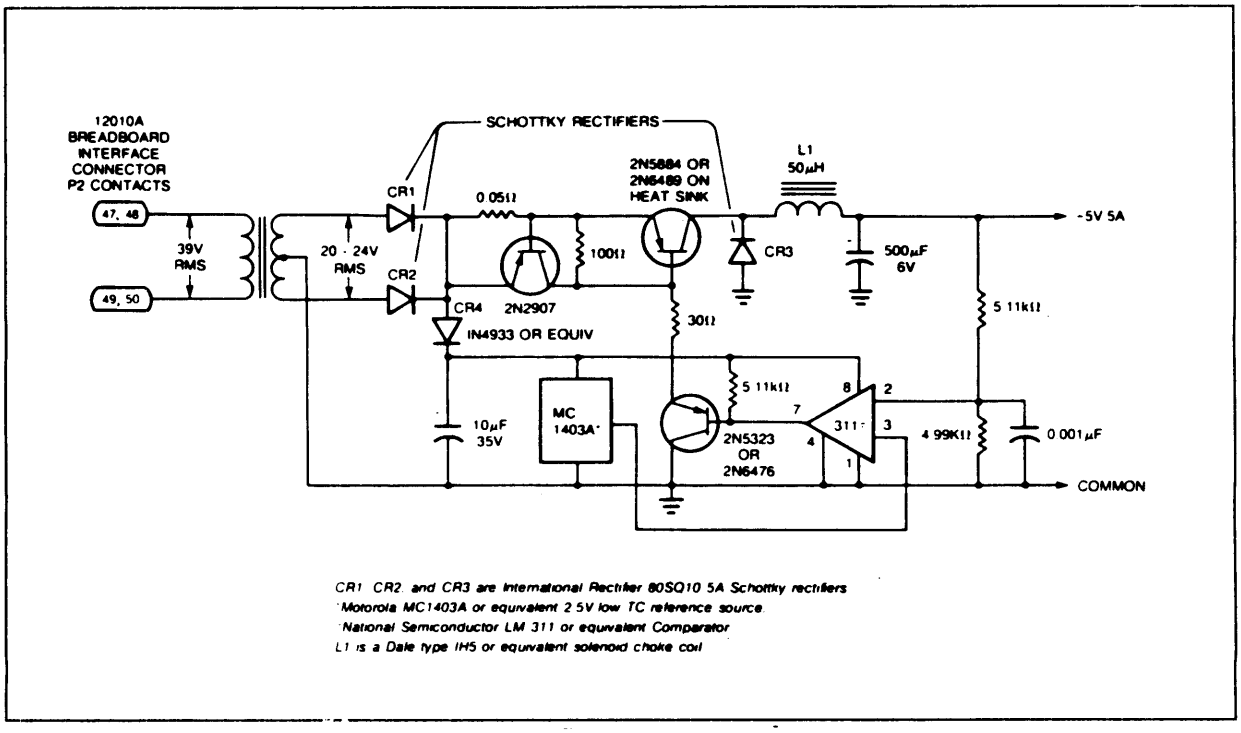
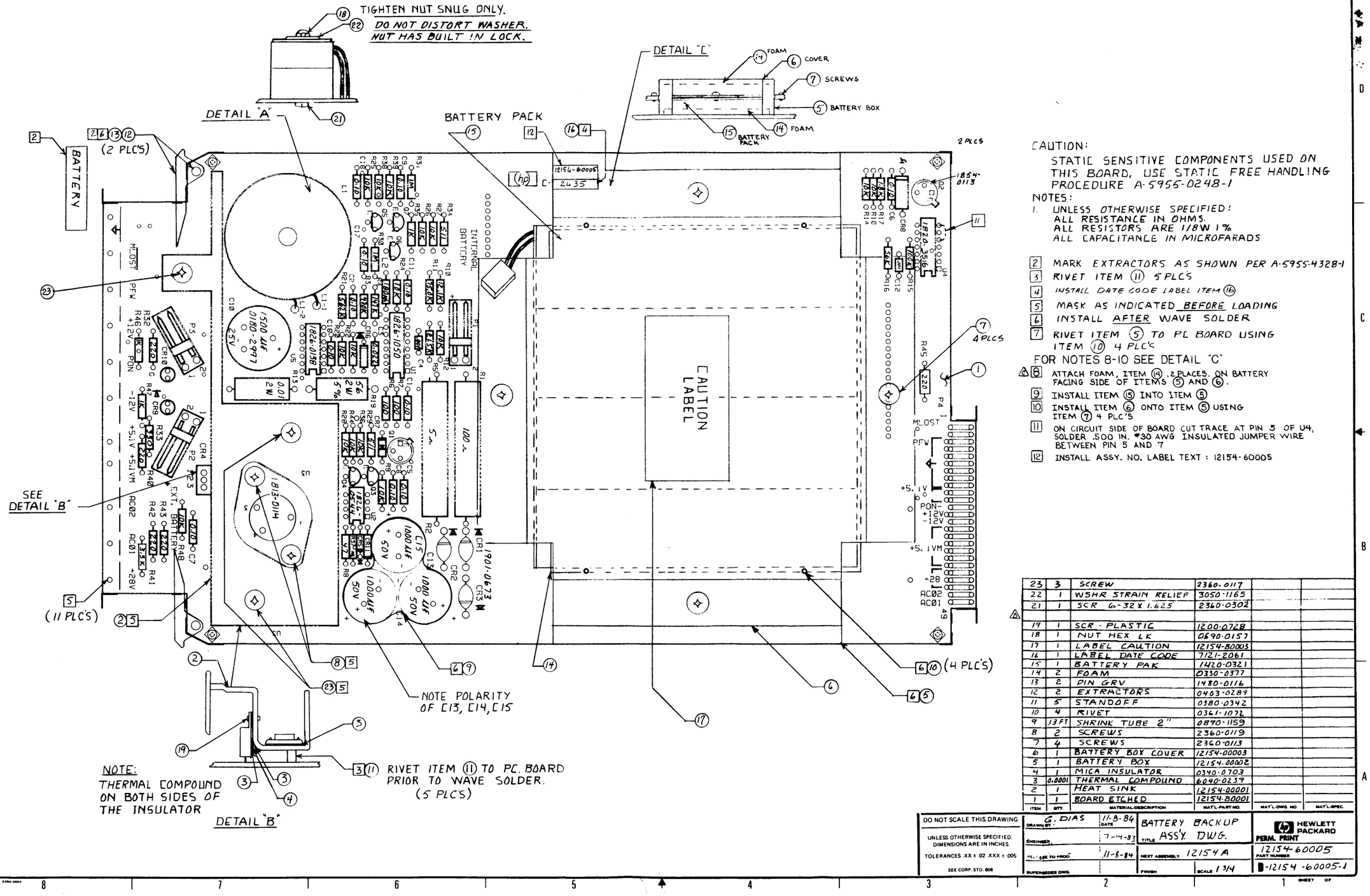


Figure 8-19. On-Interface, High Current Switching Power Supply

References:

1. Reference Data for Radio Engineers, Fifth Edition, Howard W. Sams & Co., Inc., 1974; Chapter 13, pp 28-30.
2. National Semiconductor Linear, Data Book, 1978, Section I, pp 15-22 and 50-54.
3. Morrison, Ralph, "Grounding & Shielding Techniques in Instrumentation", Second Edition, Wiley Publications, Inc., 1977.
4. Ott, Henry, "Noise Reduction Techniques in Electronic Systems", Wiley Publications, Inc., 1976.
5. Fairchild "Voltage Regulator Handbook" or "Hybrid Data Book", available from Fairchild Semiconductor.
6. Ferroxcube "Linear Ferrite Materials and Components".
7. TDK Data Book, Ferrite Cores - 2 DLE 88-002A.
8. Siemens Data Book, "Soft Magnetic Siferit", 1975.
9. Fair-Rite Materials Data Book (Rods).
10. Micrometals "Shielded Coil Forms".
11. White, Donald, "EMI Control Methodology and Procedures", Don White Consultants, 1978.



CAUTION:
STATIC SENSITIVE COMPONENTS USED ON THIS BOARD, USE STATIC FREE HANDLING PROCEDURE A-5955-0248-1

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W 1%
ALL CAPACITANCE IN MICROFARADS

2 MARK EXTRACTORS AS SHOWN PER A-5955-4328-1
3 RIVET ITEM (11) 5 PLC'S
4 INSTALL DATE CODE LABEL ITEM (16)
5 MASK AS INDICATED BEFORE LOADING
6 INSTALL AFTER WAVE SOLDER
7 RIVET ITEM (5) TO PC BOARD USING ITEM (10) 4 PLC'S

FOR NOTES 8-10 SEE DETAIL "C"

A 8 ATTACH FOAM, ITEM (14), 2 PLACES. ON BATTERY FACING SIDE OF ITEMS (5) AND (6).
9 INSTALL ITEM (15) INTO ITEM (5)
10 INSTALL ITEM (6) ONTO ITEM (5) USING ITEM (7) 4 PLC'S
11 ON CIRCUIT SIDE OF BOARD CUT TRACE AT PIN 5 OF U4, SOLDER .500 IN. #30 AWG INSULATED JUMPER WIRE BETWEEN PIN 5 AND 7
12 INSTALL ASSY. NO. LABEL TEXT : 12154-60005

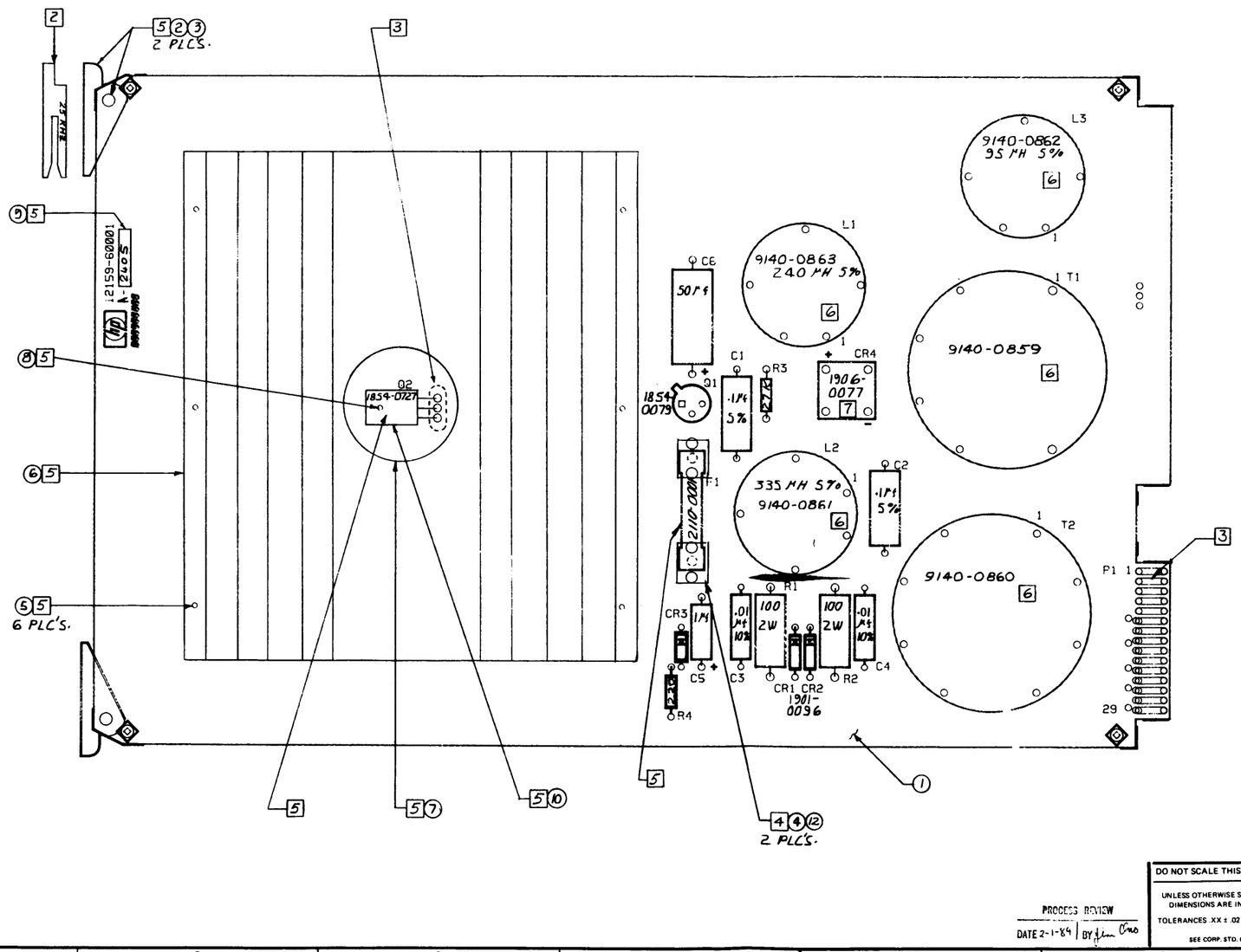
ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
23	3	SCREW	2360-0117		
22	1	WSHR STRAIN RELIEF	3050-1165		
21	1	SCR 6-32X1.625	2360-0302		
A					
19	1	SCR-PLASTIC	1200-0728		
18	1	NUT HEX LK	0590-0157		
17	1	LABEL CAUTION	12154-80003		
16	1	LABEL DATE CODE	7121-2061		
15	1	BATTERY PAK	1420-0321		
14	2	FOAM	0350-0377		
13	2	PIN GRV	1480-0116		
12	2	EXTRACTORS	0403-0289		
11	5	STANDOFF	0380-0342		
10	4	RIVET	0361-1072		
9	.13FT	SHRINK TUBE 2"	0890-1159		
8	2	SCREWS	2360-0119		
7	4	SCREWS	2360-0113		
6	1	BATTERY BOX COVER	12154-00003		
5	1	BATTERY BOX	12154-00002		
4	1	MICA INSULATOR	0340-0703		
3	0.0001	THERMAL COMPOUND	6040-0239		
2	1	HEAT SINK	12154-00001		
1	1	BOARD ETCHED	12154-80001		

DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005
SEE CORP. STD. 608

DRAWN BY: G. DIAS 11-8-84
ENGINEER: 7-14-83
RELEASE TO PROD: 11-8-84
SUPERSEDES DWG.

TITLE: BATTERY BACKUP ASS'Y DWG.
NEXT ASSEMBLY 12154A
FINISH
SCALE 1 3/4

HEWLETT PACKARD
PERM. PRINT
PART NUMBER 12154-60005
D-12154-60005-1
SHEET OF



NOTES:

1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTANCE IN OHMS
   RESISTORS 1/4 W 5%
   ALL CAPACITANCE IN MICROFARADS
2. MARK EXTRACTOR PER DWG. A-5955-4328-1
3. MASK PRIOR TO WAVE SOLDER.
4. TACK-GLUE ITEM (4) TO PC BOARD WITH SMALL AMOUNT OF ITEM (12).
5. INSTALL AFTER WAVE SOLDER.
6. BEND PINS FLAT AFTER PARTS ARE INSTALLED ON BOARD.
7. SPACE CR4 UP OFF THE BOARD APPRO. .125 IN.

SCHEMATIC D-12159-60001-51

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
12	A/R	ADHESIVE-RTV, CLEAR	0470-0251		
10	A/R	THERMAL COMPOUND	6040-0239		
9	1	LABEL-DATE CODE	7121-2061		
8	1	NYLON SCREW 4-40	2200-0721		
7	1	TRANSISTOR INSULATOR	0340-0703		
6	1	HEATSINK	1205-0575		
5	6	RIVET .156"D BLIND	0361-1072		
4	2	FUSE CLIP	2110-0269		
3	2	EXTRACTOR	0403-0289		
2	2	PIN-GROOVED	1480-0116		
1	1	BOARD-ETCHED	12159-60001		

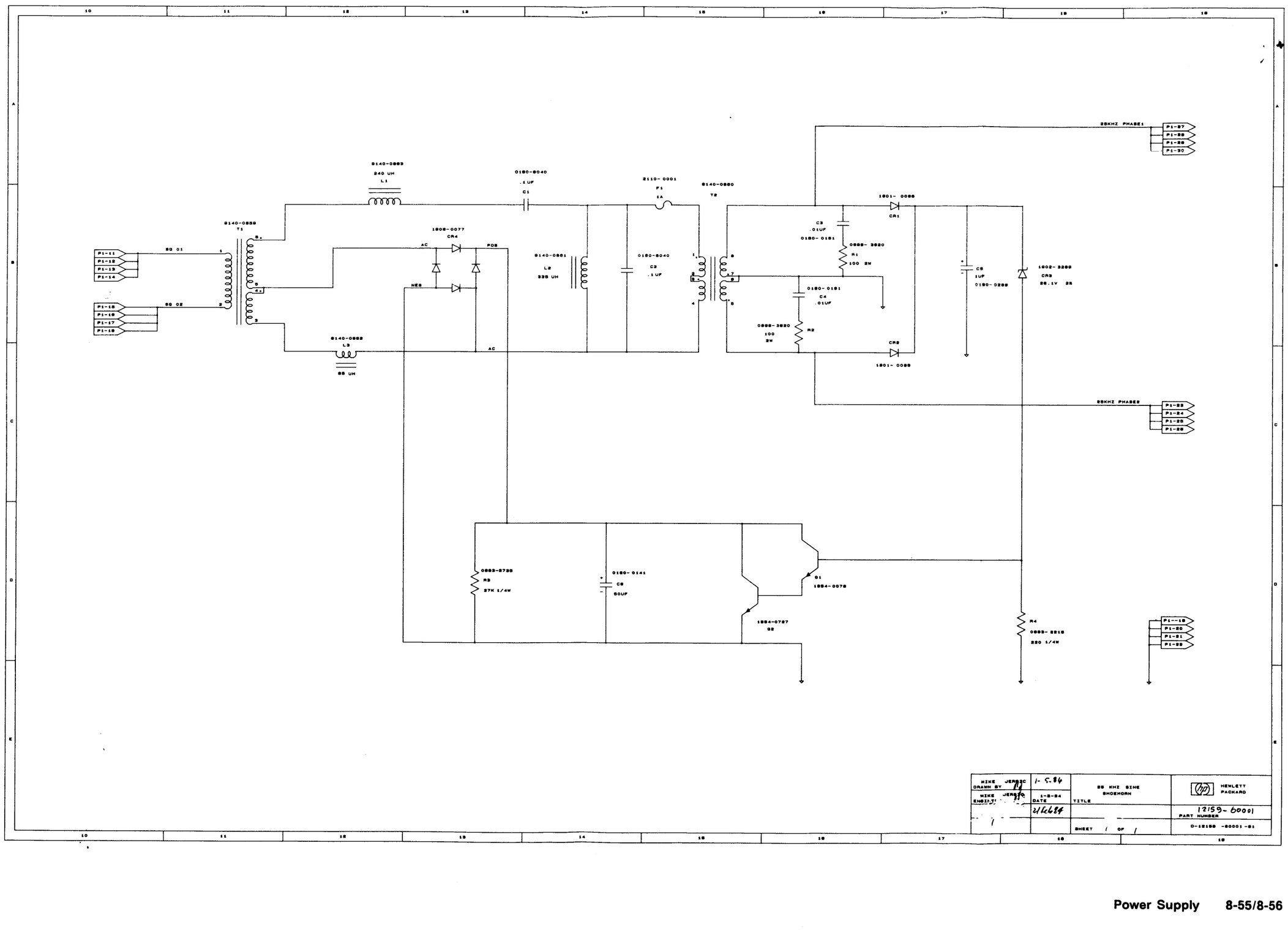
PROCESS REVIEW
DATE 2-1-84 | BY

DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005
SEE CORP. STD. 808

DRAWN BY	R.ESPARZA	12-13-83
ENG. APPR.		1-11-84
MFG. APPR.		2 Feb 84
SUPERSEDES DWG.		

TITLE: PCA-25 KHZ (ASSY. DWG.)
NEXT ASSEMBLY: 12159A
FINISH: —
SCALE: 1/4

HEWLETT PACKARD
PART NUMBER: 12159-60001
12159-60001-1
SHEET 1 OF 1


P1-11
P1-12
P1-13
P1-14
SQ 01
P1-15
P1-16
P1-17
P1-18
SQ 02
9140-0838
T1
9140-0883
240 UH
L1
0180-0040
.1UF
C1
9140-0882
L3
88 UH
1808-0077
CR4
AC
POS
NEG
9140-0881
L2
335 UH
0180-0040
C2
.1UF
2110-0001
F1
1A
9140-0880
T2
C3
.01UF
0180-0181
0698-3820
R1
100 2W
C4
.01UF
0180-0181
0698-3820
R2
100
2W
1901-0088
CR1
CR2
1901-0088
C5
1UF
0180-0228
1902-3206
CR3
20.1V 2%
25KHZ PHASE1
P1-27
P1-26
P1-29
P1-30
25KHZ PHASE2
P1-23
P1-24
P1-25
P1-26
0683-2735
R3
27K 1/4W
0180-0141
C6
50UF
1854-0078
Q1
1854-0787
Q2
R4
0683-2215
220 1/4W
P1-19
P1-20
P1-21
P1-22
MIKE JERSIC
DRAWN BY
MIKE JERSIC
ENGR'G
1-5-84
DATE
2/4684
25 KHZ SINE
SHOEHORN
TITLE
HEWLETT
PACKARD
12159-60001
PART NUMBER
SHEET 1 OF 1
D-12159 -60001 -S1

A

Bus Control Timing Diagrams

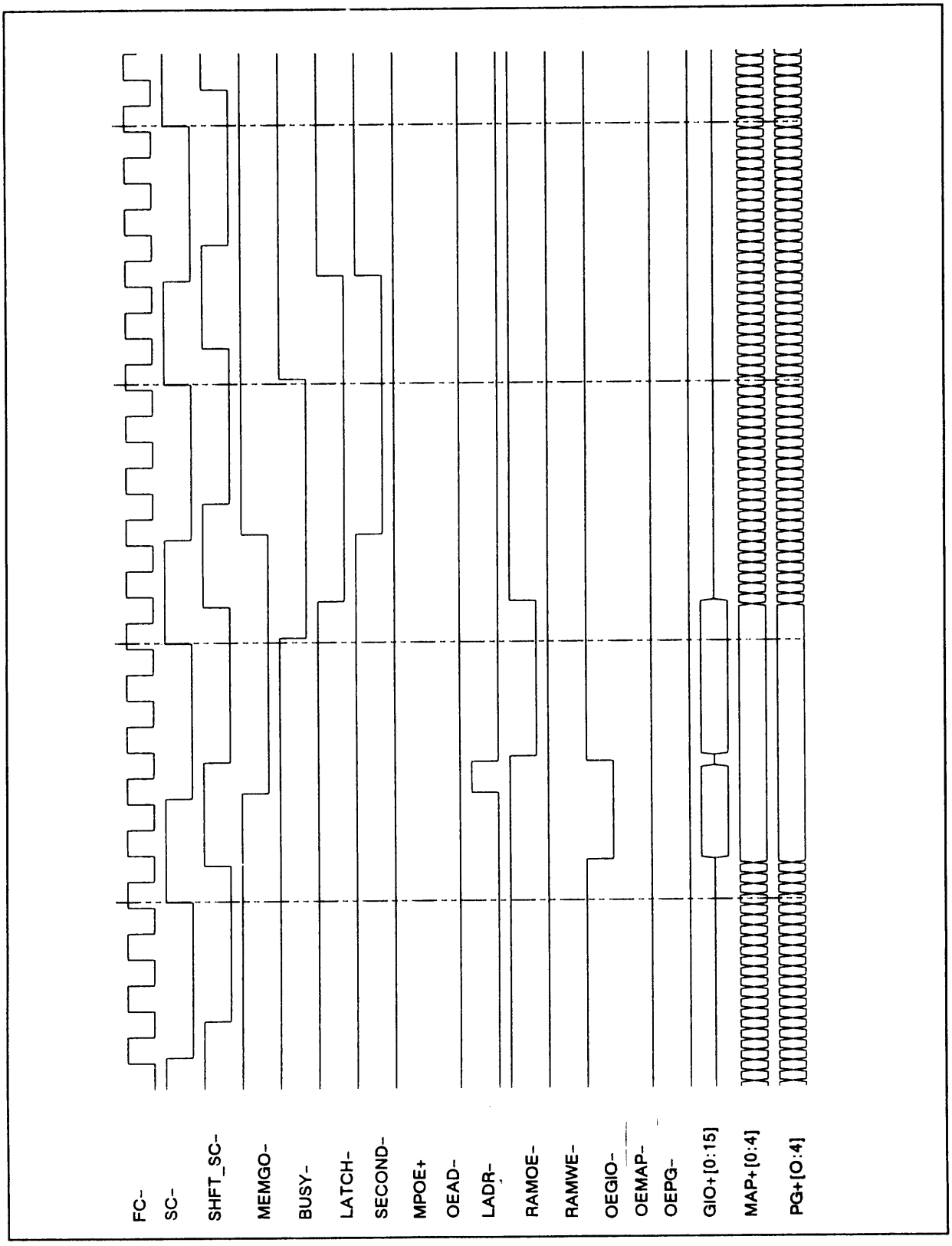


Figure A-1. Basic Processor Main Memory Access

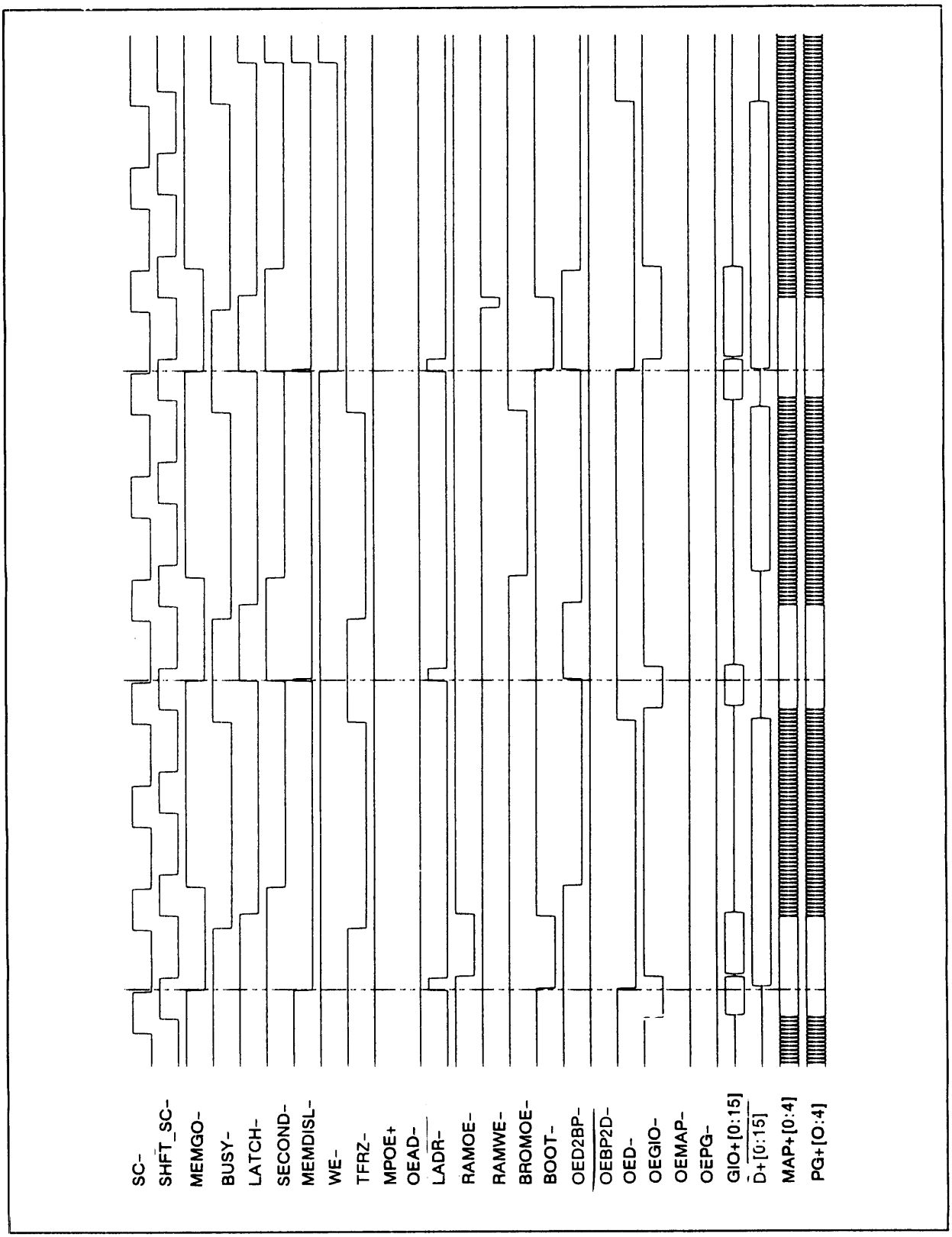


Figure A-2. Boot Memory Accesses

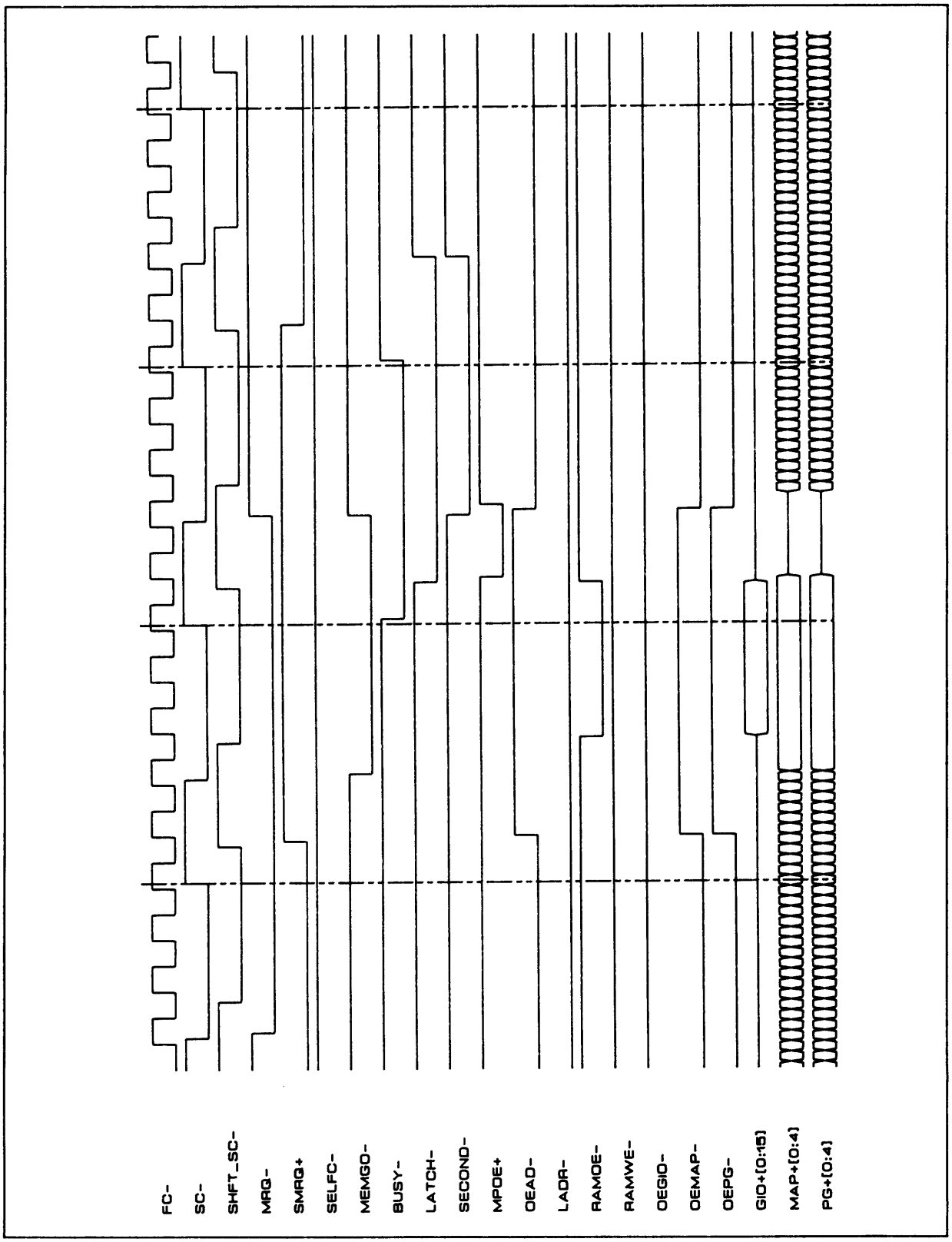


Figure A-3. Basic DMA Memory Access

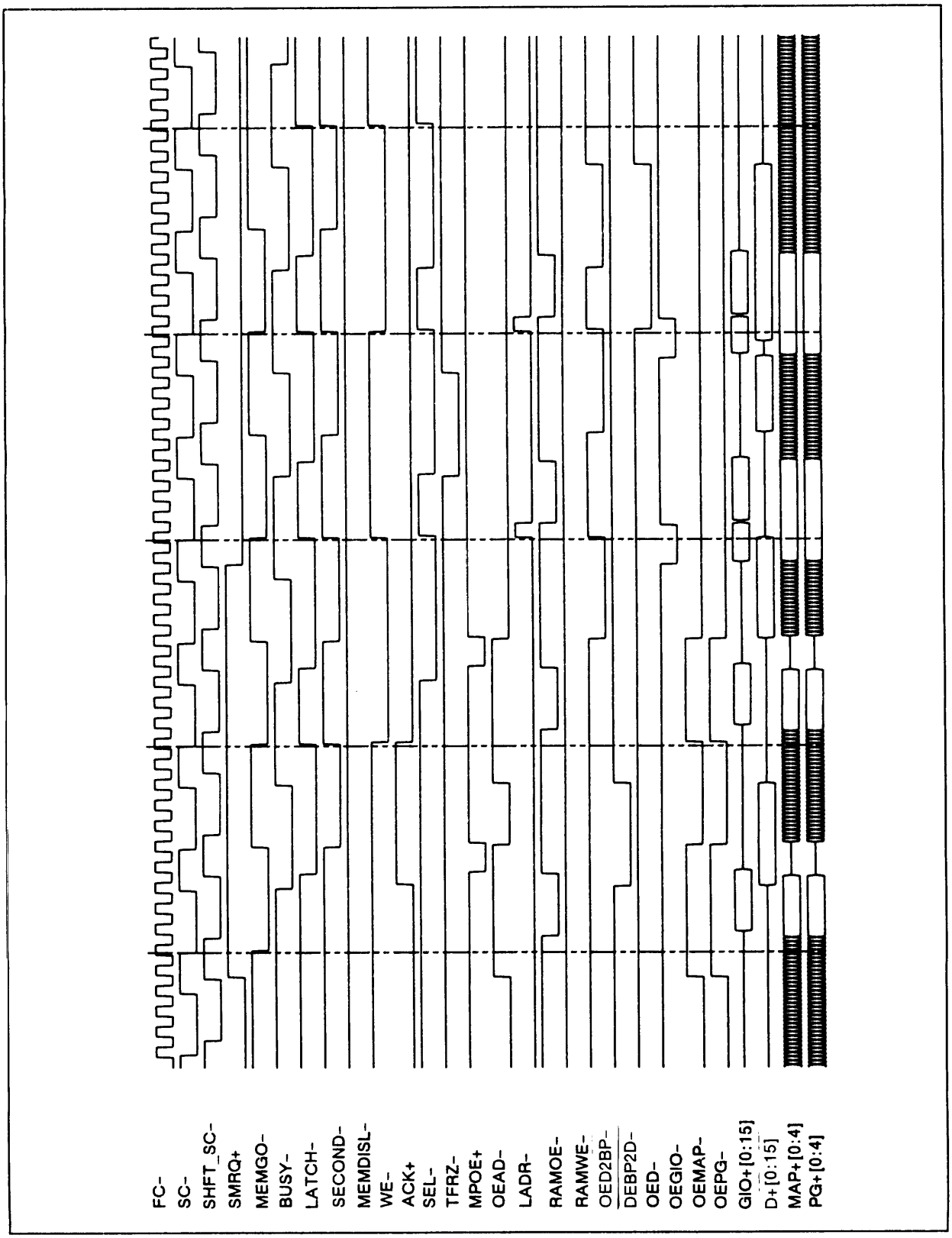


Figure A-4. Miscellaneous Full-Speed Memory Accesses

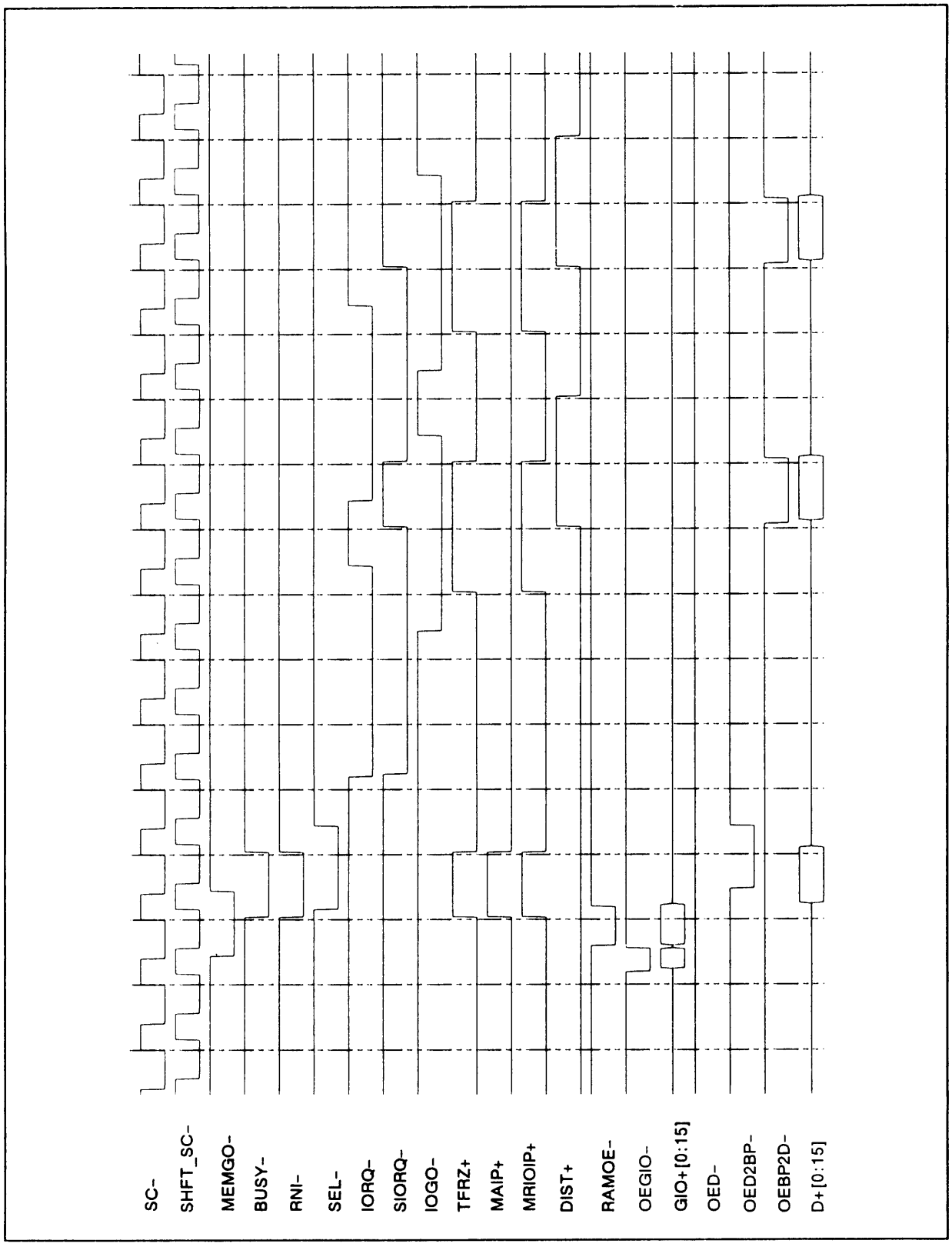


Figure A-5. I/O Handshake Read Cycle

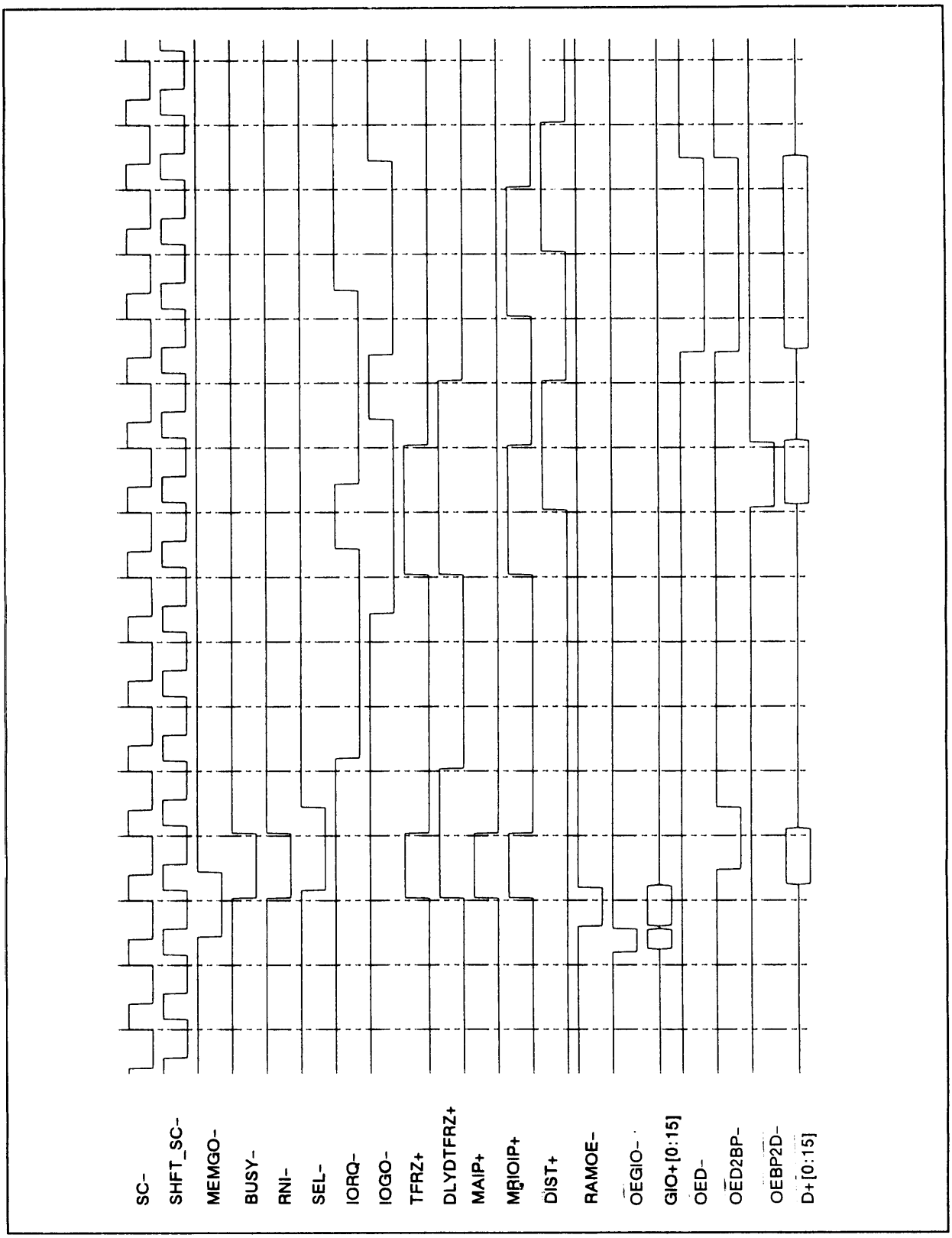


Figure A-6. I/O Handshake Write Cycle

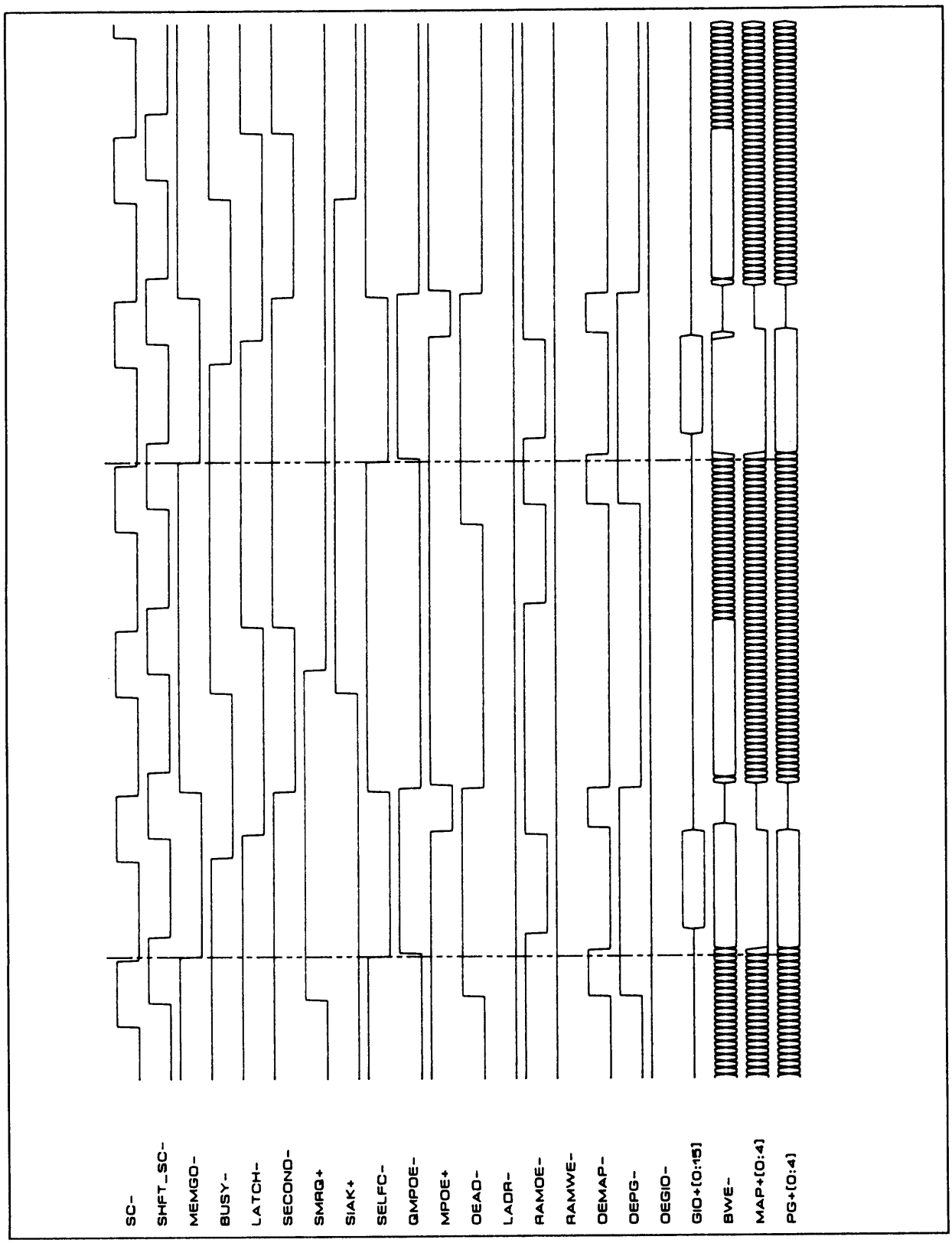


Figure A-7. IAK and Self-Configuring DMA Cycles

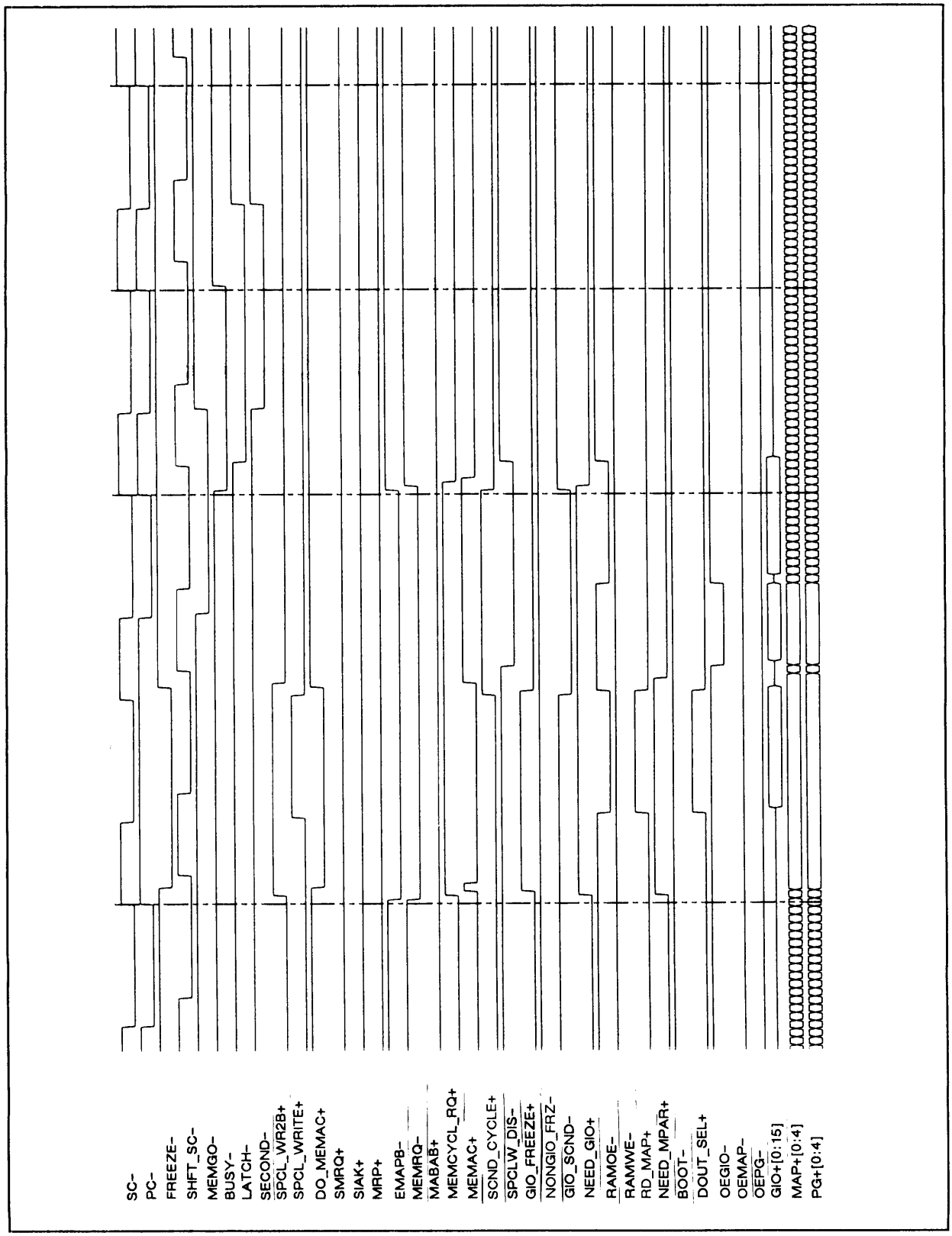


Figure A-8. Special Map Read Cycle

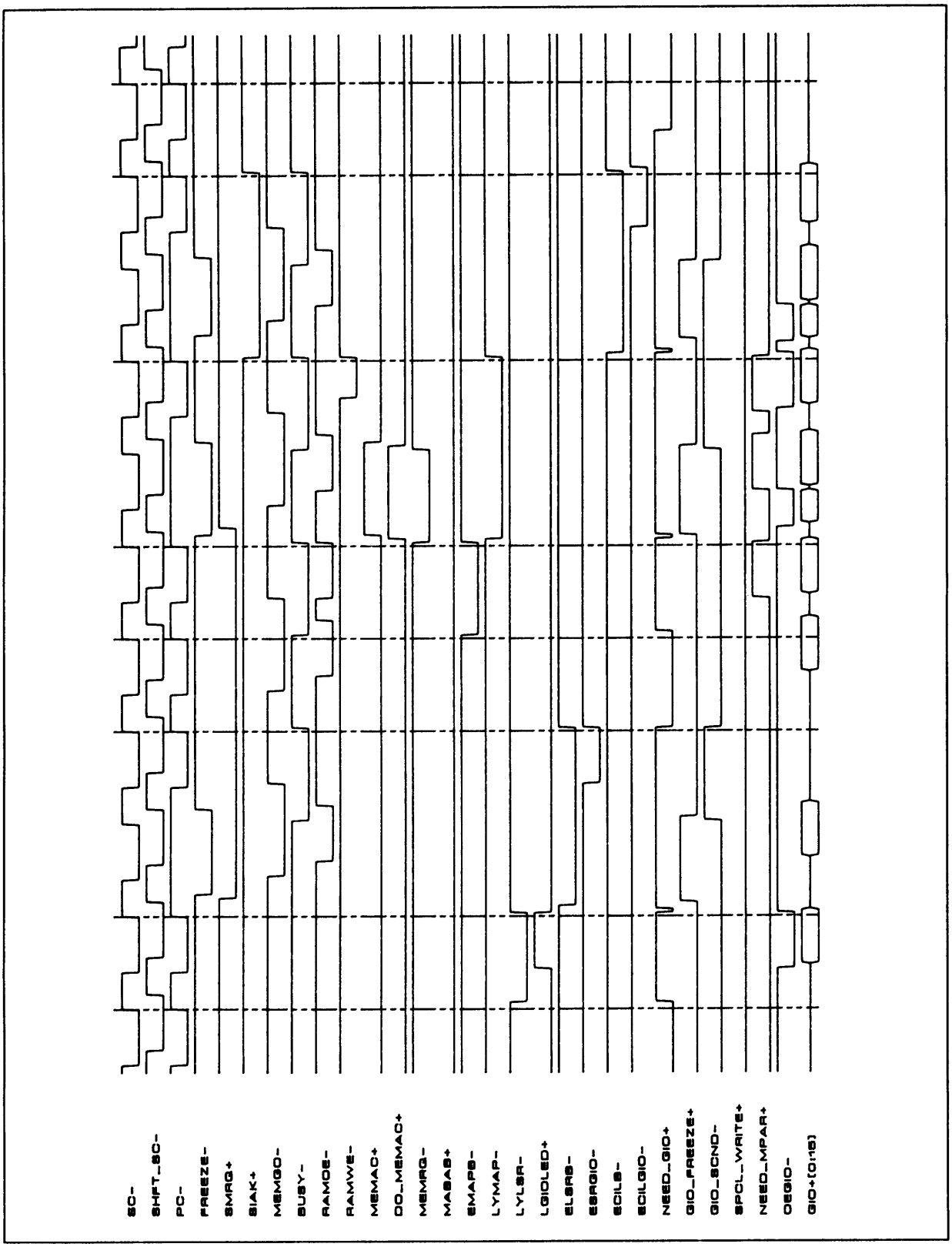


Figure A-9. GIO-BUS Contention

B

Memory Control Timing Diagrams

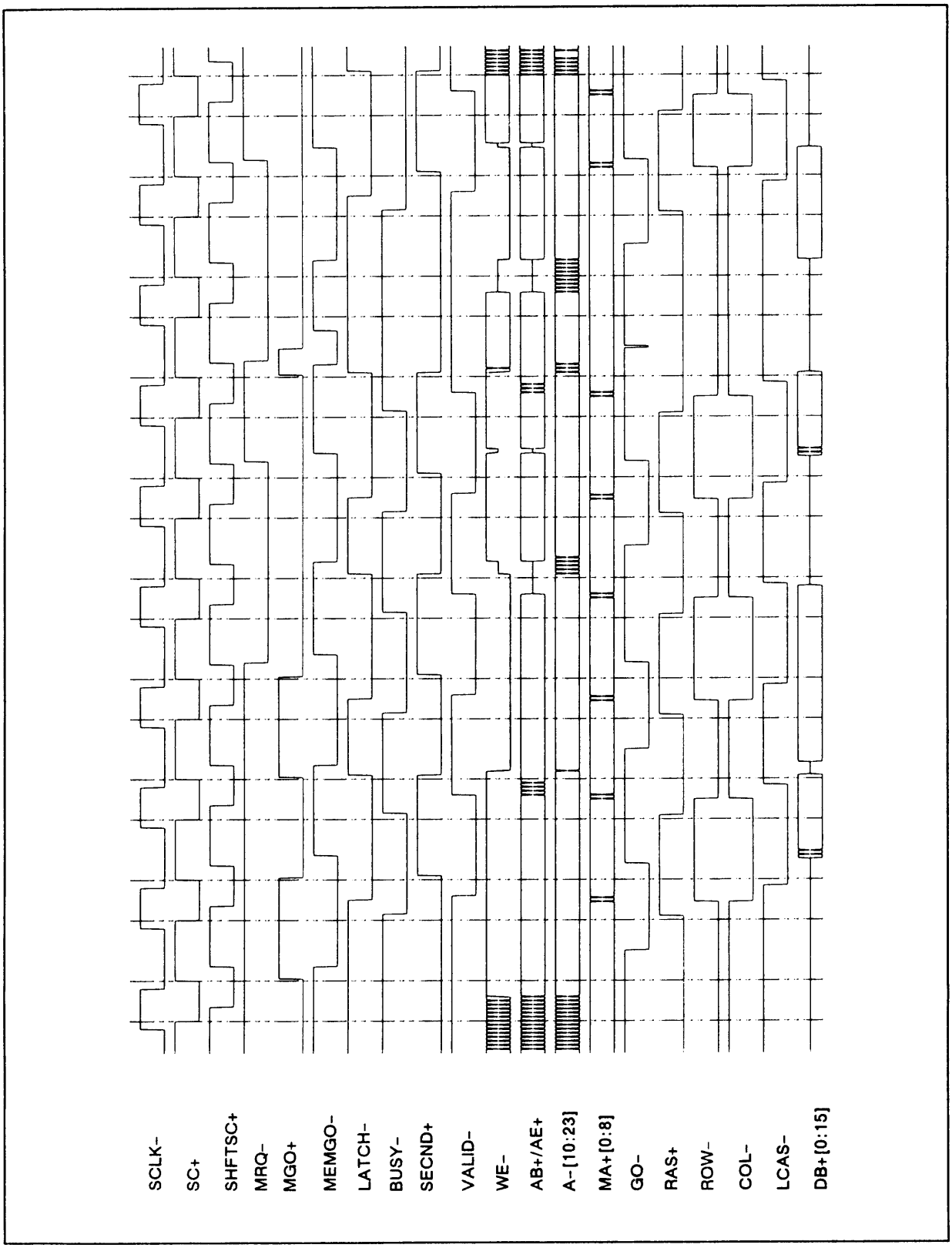


Figure B-1. Processor and DMA Accesses W/ADDR & Data

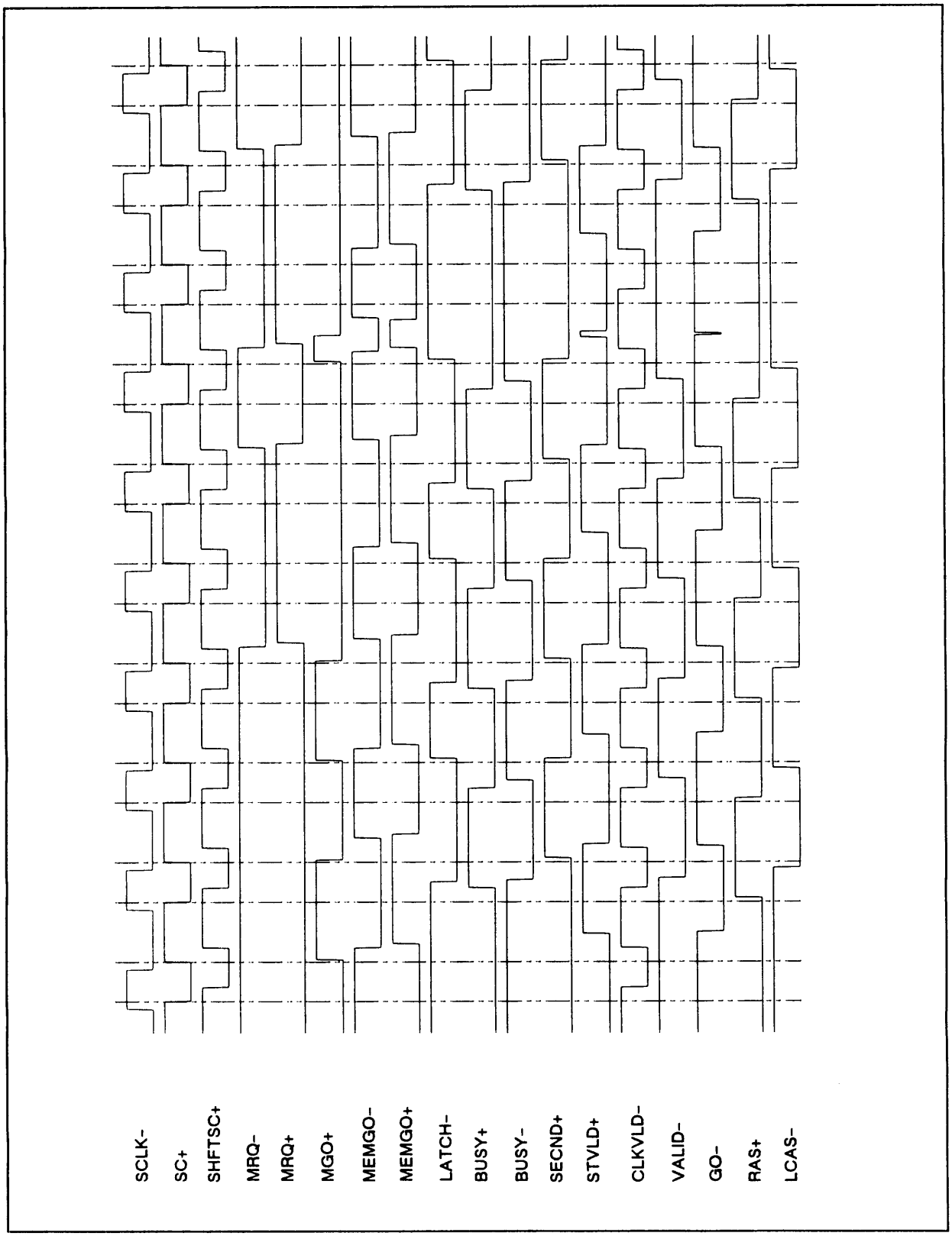


Figure B-2. Two Cycle Processor and I/O RAM Accesses

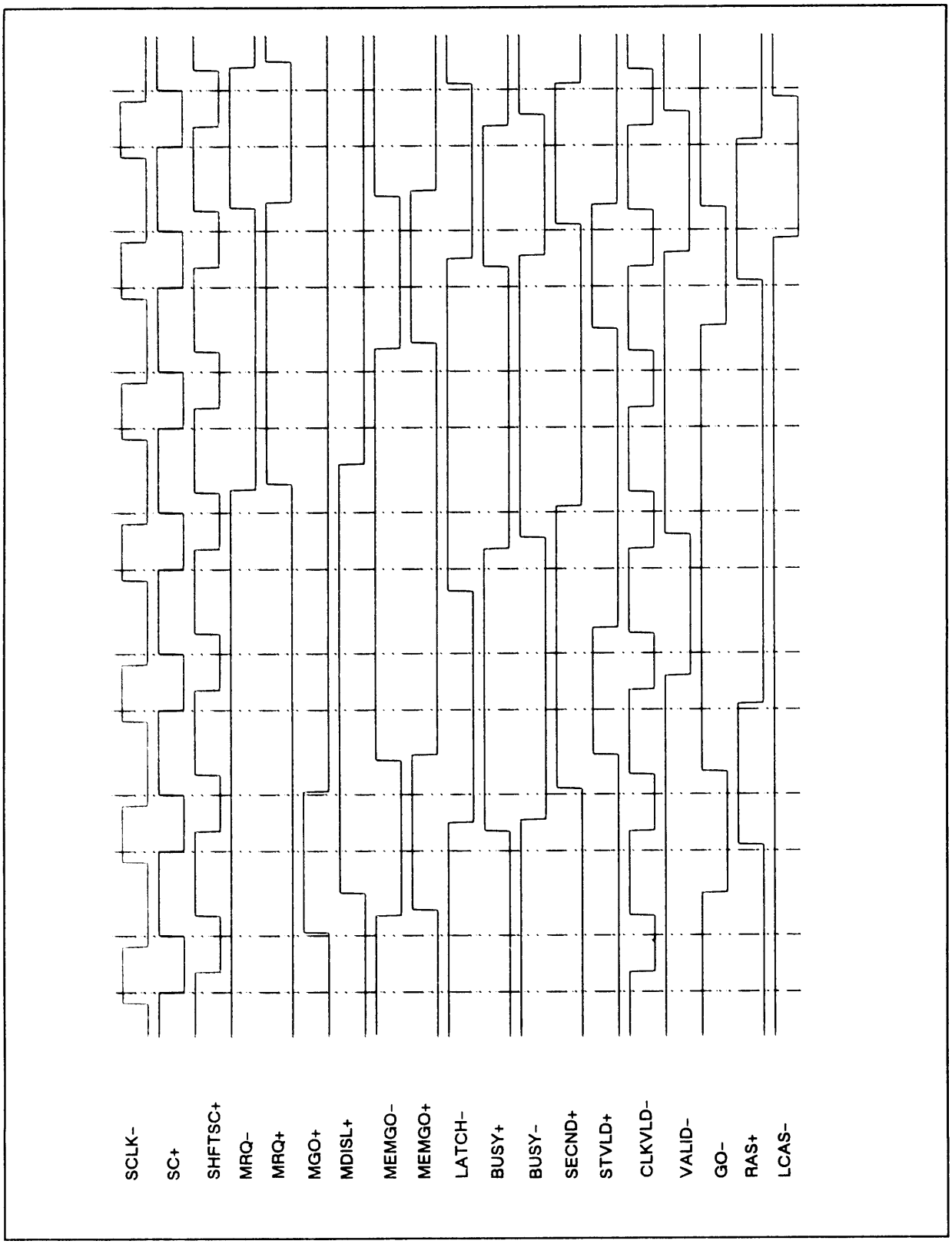


Figure B-3. Boot Memory and I/O to RAM Accesses

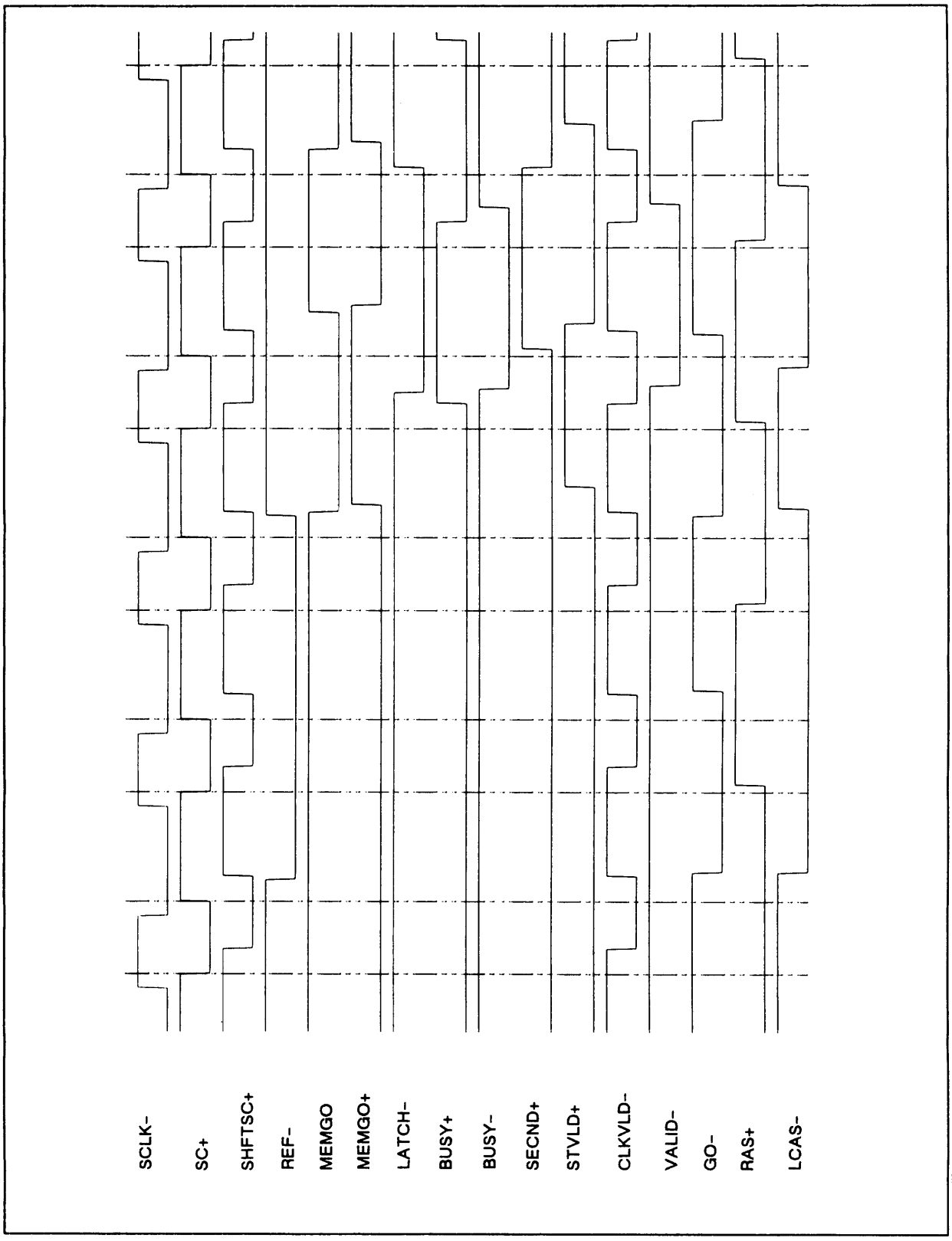


Figure B-4. Refresh Cycle

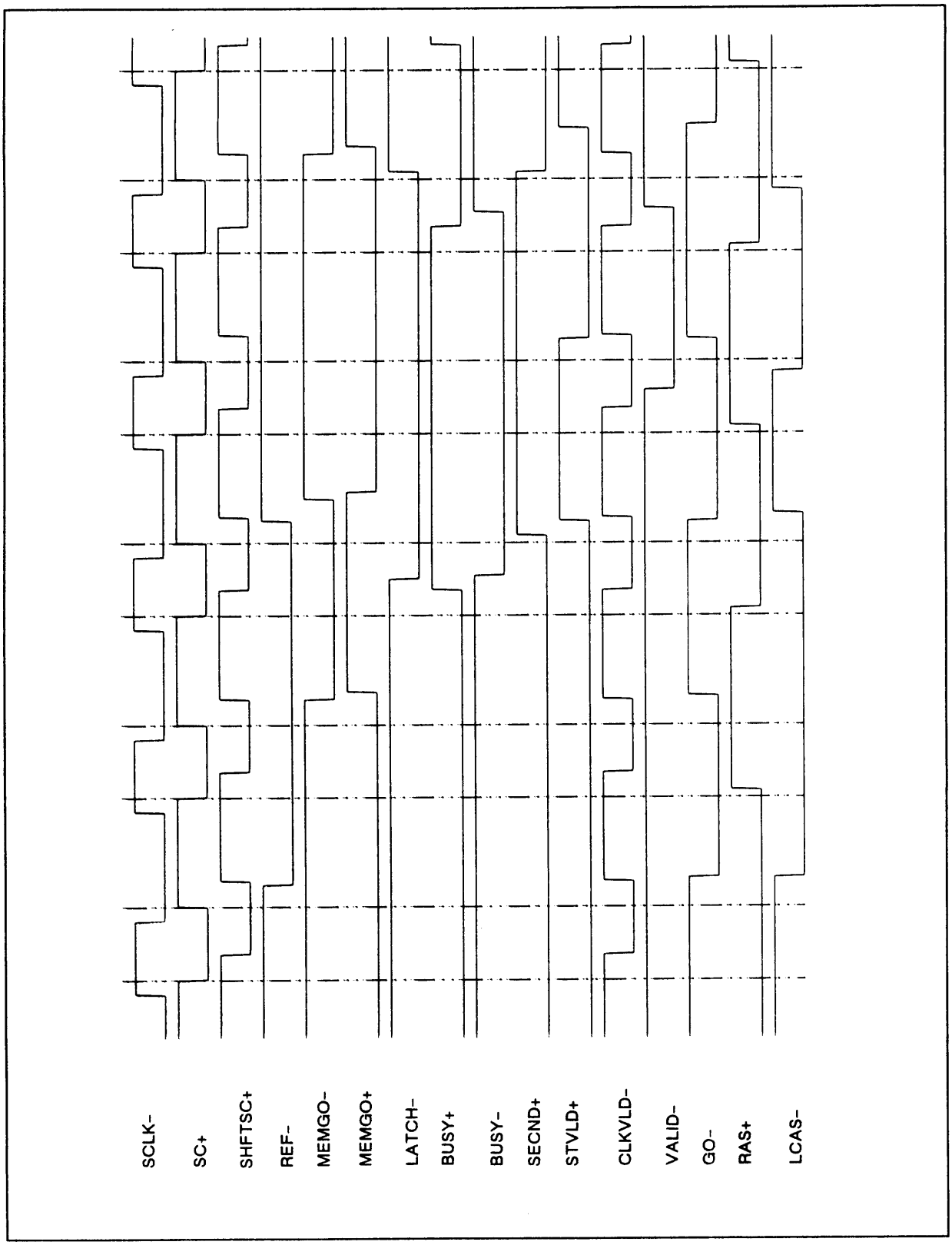


Figure B-5. Refresh with Three Cycle Access

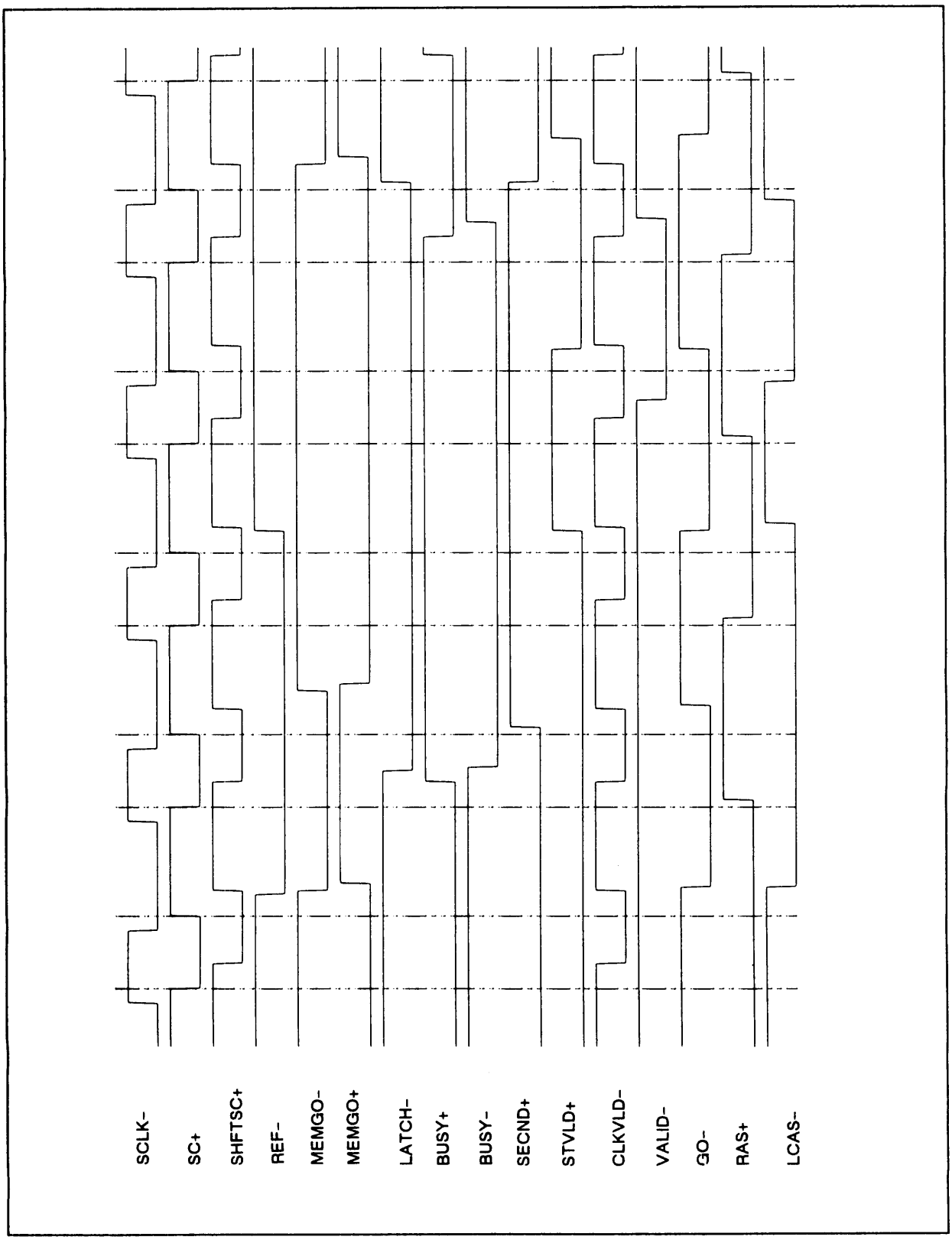


Figure B-6. Four Cycle Refresh

C

Processor Memory Access Cases

In order to clarify the information presented, simple processor memory access cases will be discussed. The Memory and I/O State Machine (MIOSM) state diagram is used as a basis for understanding the actions of the processor. The timing diagrams presented here were generated from simulations of the actual circuitry. The timing diagrams, therefore, are not idealistic representations but close to the real world waveforms. Therefore, glitches may be seen in the diagrams as signals change state.

Most of the memory accesses pictured here were actually Boot ROM accesses. These are similar to main memory accesses except they take an extra cycle. Keep in mind that in normal operation, almost all of the memory accesses will be two-cycle accesses to main memory, rather than the three-cycle accesses shown here.

MIOSM States

The states of the MIOSM can be interpreted by examining the binary level of each MIOSM signal, near the end of each SC- clock period, SC-↑. The binary value of each signal, from DIST+ to MRIOIP+, taken together, form an octal number. This octal number is then the state of the MIOSM.

Figure C-1 shows some of the states of the MIOSM. Refer to the MIOSM sections in Chapter 3 for more information on the behavior of the MIOSM. The MIOSM state diagram, in Figure 3-12, gives the definition of each state.

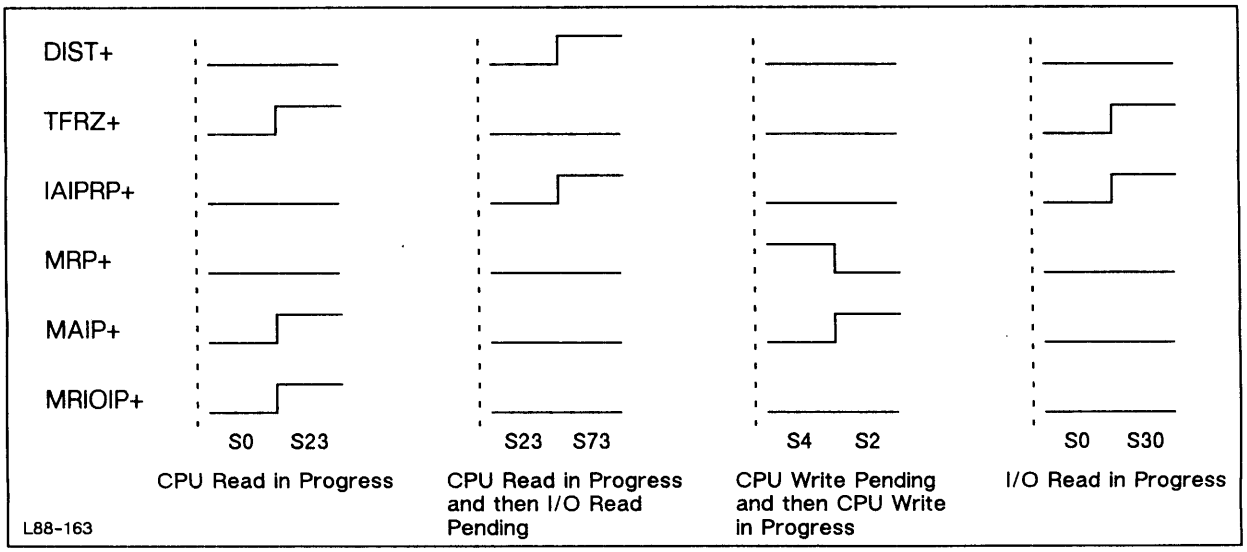


Figure C-1. Memory and I/O State Machine (MIOSM) States

Processor Read

The timing diagram in Figure C-2 illustrates the case of a simple processor read.

① The FCHP microorder has been executed by the microsequencer. This asserts MEMRQ_2B+. Because there are no freeze conditions present (IFREEZE- is false), MEMAC+ is asserted.

② The assertion of MEMAC+ initiates the memory cycle within the processor. The MIOSM asserts MGO+, the processor's precursor to MEMGO- (on the backplane). MGO+ is the actual signal used to request a memory cycle for the processor.

③ The memory controller responds to MEMGO- by asserting BUSY- to inform other memory requesters that it is currently involved in a memory access.

At the same time, the assertion of MEMAC+ causes the MIOSM to sequence through its processor read states. This is shown by the MIOSM transitioning from State 0 to State 23.

The FETCH+ signal is asserted to distinguish this memory access as an instruction fetch. It is also used as a trigger for monitoring the backplane. FETCH+ can be traced by a logic analyzer to observe fetches.

Note that this BUSY- is "stretched" due to the three-cycle access. Normally, BUSY- would be only one cycle long (also, VALID- would be asserted one cycle earlier).

④ When the memory system has obtained the desired memory word, the memory controller asserts VALID-. The A400 processor clocks the data off the D-Bus on the board at the next SC-↑. The MIOSM uses this signal to leave State 23.

MEMCE- is used to indicate the last cycle of a memory access. It has roughly the same timing as VALID-. During MEMCE- a freeze occurs if the microcode attempts to read the T-Register. The T-Register does not contain valid data until MEMCE-↑.

ENDMRDP1+ is similar to MEMCE-, but delayed by one cycle. ENDMRDP1+ is used for events that occur after the memory cycle completes. Parity errors, for instance, are not detected until after VALID-↓. Therefore, parity error uses ENDMRDP1+ to qualify parity errors.

In this case, TCNT- asserts since this memory access was a fetch. TCNT- causes the returning data to be clocked into the CT-Register, as well as the T-Register. TCNT- enables the synchronous load of the CT-Register on DC-↑. MEMCE- is used to enable the load of the T-Register on DC-↑.

⑤ The MIOSM returns to S0. Another MEMAC+ follows immediately after the completion of the first memory access.

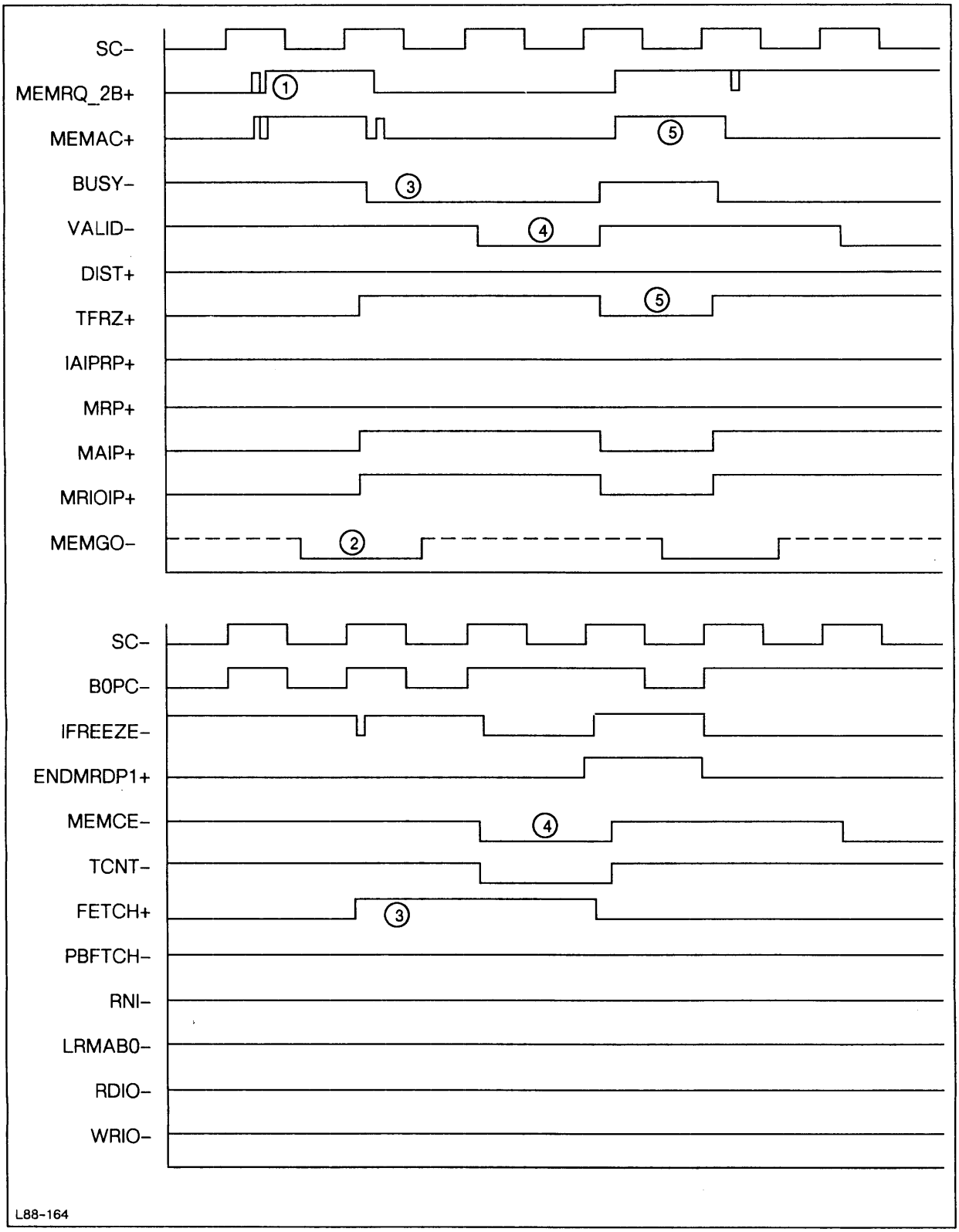


Figure C-2. Processor Read

Processor Write

Figure C-3 shows the case of a processor write. The previous macro-emulation routine has executed the FCHP microorder to fetch the next macroinstruction.

The macroinstruction fetched is a STB "memwrd". A STB writes the contents of the B-Register into the memory location whose address is represented by the symbol "memwrd".

① The CPU fetches the macroinstruction, STB. This is performed as described in the previous Processor Read section.

② The STB macroinstruction is latched into the processor. VALID– indicates the end of this memory cycle. Note also that FETCH+ is asserted to distinguish this access as a fetch.

③ The processor decodes the STB and asserts MEMWR–, along with MEMGO–. This indicates that the pending memory cycle is a write. On the next SC–^, the MIOSM transitions to State 2.

④ During the second cycle, when the MIOSM is in State 2, VALID– goes true indicating the memory cycle is about to complete. This implies that the contents of the B-Register has been written to memory. The MIOSM then returns to S0.

⑤ The MIOSM is now ready to fetch the next instruction. Note that the processor has been waiting on the MIOSM to do the fetch. This can be seen by MEMRQ2B+ and BUSY– both being asserted during period four. As a result, the processor has been frozen.

Now, however, IFREEZE– is deasserted and MEMGO– is fired off.

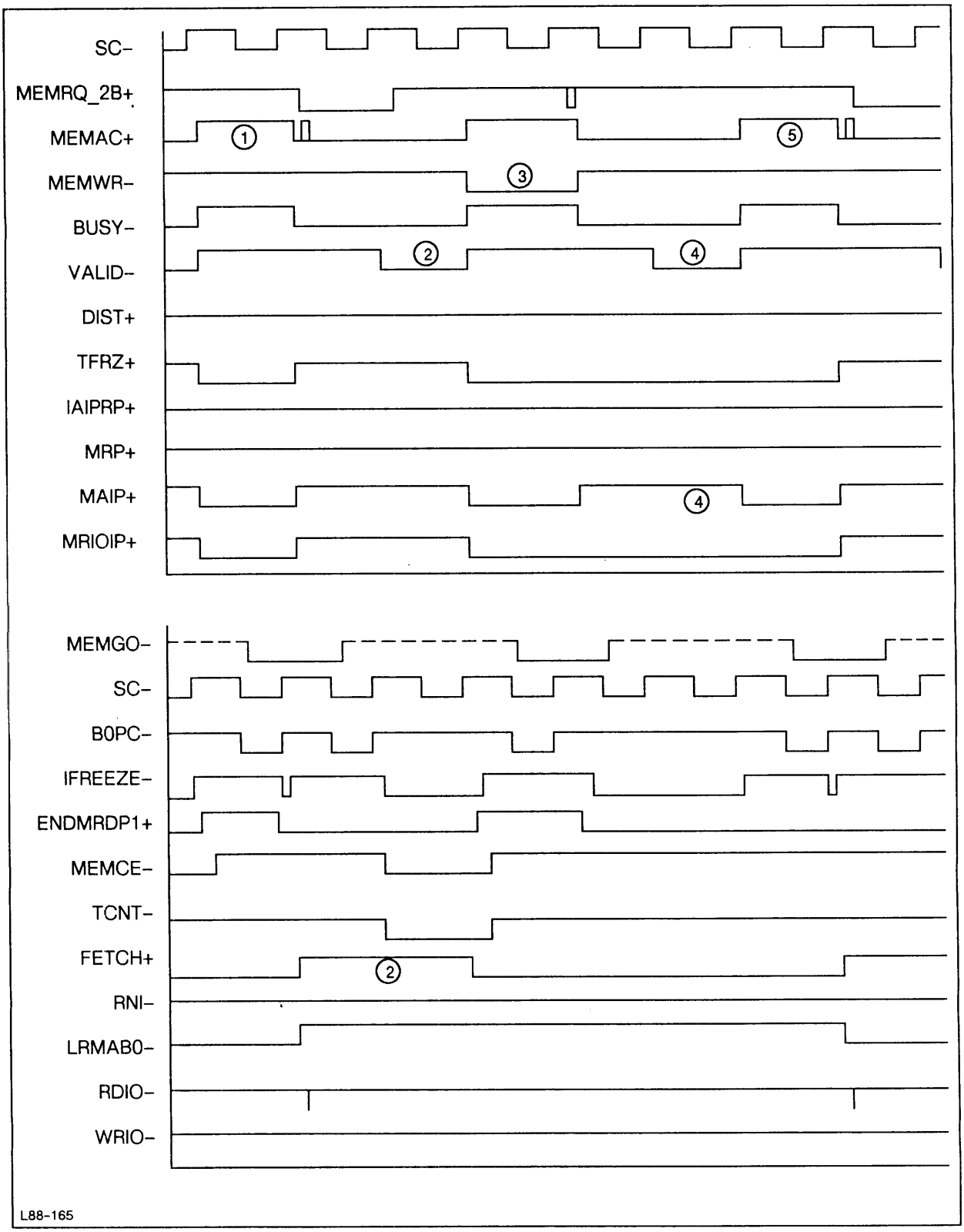


Figure C-3. Processor Write

I/O Instruction Handshake Overview

Figure C-4 shows an overview of an I/O handshake. This is meant to give an overall picture of I/O Handshake (IOHS) cycles. The next two sections discuss the particular cases of IOHS Reads and Writes.

① The processor fetches an OTA instruction. It decodes the OTA as an I/O instruction. Some overhead is incurred before the instruction is re-fetched (or broadcasted).

② The processor initiates another memory access of the OTA instruction. This is identical to the original fetch, except the signal RNI– is asserted. RNI– informs all I/O interfaces to latch the instruction when it returns from memory. Only the selected I/O interface, however, executes the instruction. This is known as an instruction broadcast.

Note also that neither FETCH+ nor TCNT– is asserted. TCNT– is the result of FETCH+. Since this is a broadcast, it is unnecessary to return the OTA instruction to the CT-Register because it is already there.

③ The I/O interface initiates an I/O handshake with the processor. In this case, a double-handshake is performed.

This double-handshake transfer is discussed further in the following two sections.

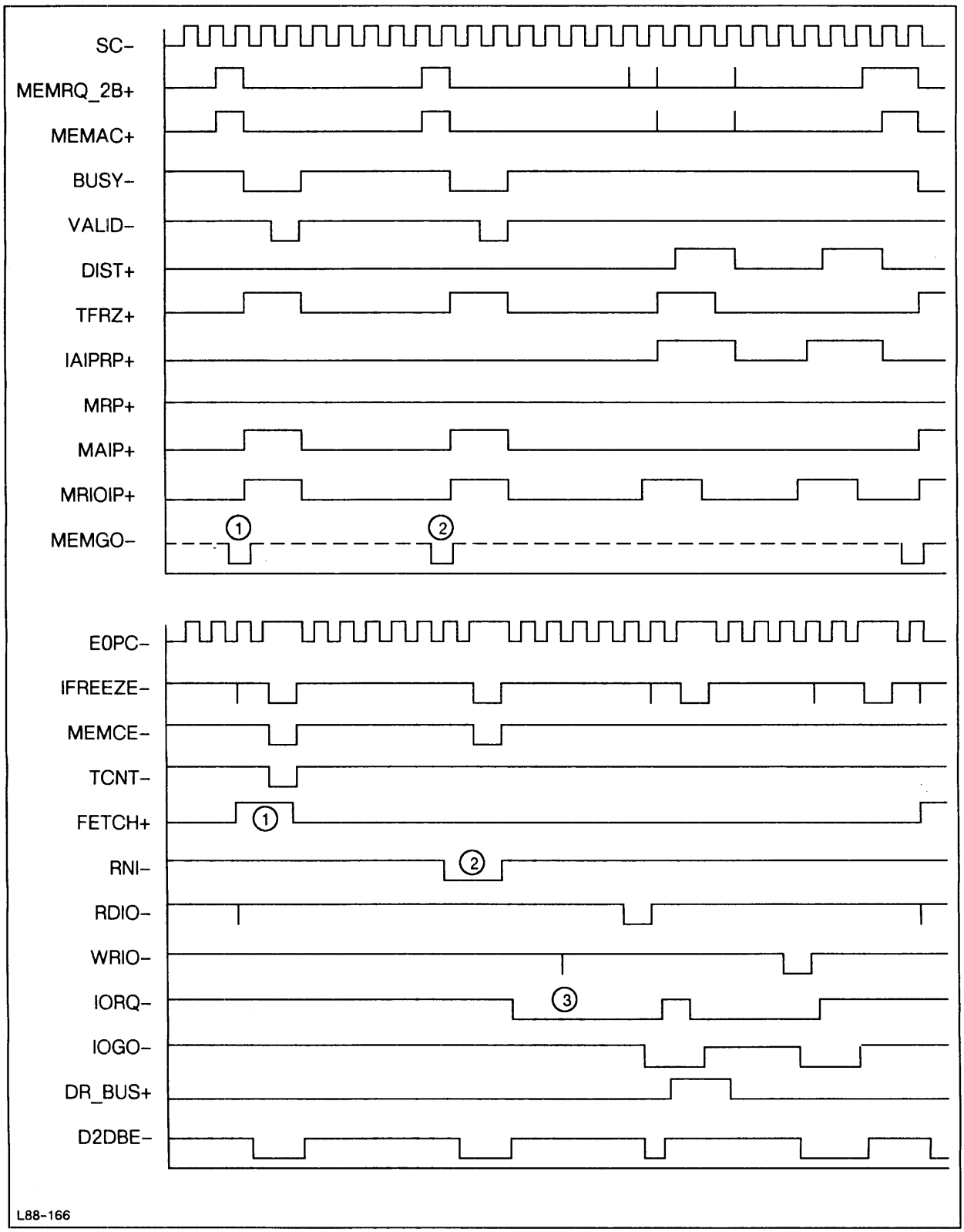


Figure C-4. I/O Instruction Handshake Overview

I/O Handshake Read

Figure C-5 is a continuation of figure C-4. In this case, the processor (MIOSM) is performing an I/O handshake read. An LIA (Load Into A-Register from I/O) macro-instruction generates the IOHS read. After decoding the LIA, the processor realizes it is an I/O instruction and re-fetches the LIA with RNI- asserted. The I/O card whose select code matches that of the re-fetched instruction (LIA 25, for example), latches and executes the LIA. This is as explained in the I/O Instruction Overview section.

① The I/O interface realizes it needs interaction with the processor in order to execute the LIA. Therefore, it asserts IORQ- to request interaction with the processor.

② The processor detects IORQ- and eventually executes microcode containing the RDIO microcode. This generates a signal called RDIO-.

③ RDIO- tells the MIOSM to handshake with the I/O interface. The MIOSM complies by asserting IOGO- as it transitions to State 31.

④ The I/O interface sees IOGO- as an acknowledgment that the processor is ready to receive data. The I/O interface releases IORQ- for one cycle and drives out a control word. This control word instructs the processor as to what type of transaction the I/O interface wishes to perform. Specifically, the base set microcode uses the control word to decide how to process the I/O instruction.

The control word also includes a bit which indicates whether another transfer is needed after the pending one. Because the LIA requires only two transfers (one for the control word and one for data), another transfer is not needed. Two transfers are referred to as a "double handshake".

The DR_BUS+ signal is an artificial signal (part of the simulator model) that indicates when the I/O interface is driving the backplane. The signal d2dbe- indicates when the processor is driving the backplane.

⑤ The MIOSM transitions automatically to S71. In this state it waits for IORQ- to deassert.

⑥ The MIOSM sees IORQ- being deasserted. This tells it the first half of the double-handshake is complete. The MIOSM releases IOGO- and returns to State 0 (from State 71 via State 50). This action causes the processor, if frozen, to resume. The processor examines the control word which has been returned. In this case, the control word indicates a load into A from the I/O interface. The processor now prepares to receive this data from I/O.

⑦ When the processor is ready to receive data from the I/O interface, it issues another RDIO to the MIOSM. This causes the MIOSM to assert IOGO-, which tells the interface to send the data. The interface sends the data and releases IORQ-, since it is now done with the double-word handshake. When the MIOSM returns to S0, it releases IOGO-.

In both handshakes, the processor freezes (IFREEZE- asserted) after it issues the RDIO-. This is because the processor tries to access the T-Register before the handshake is complete.

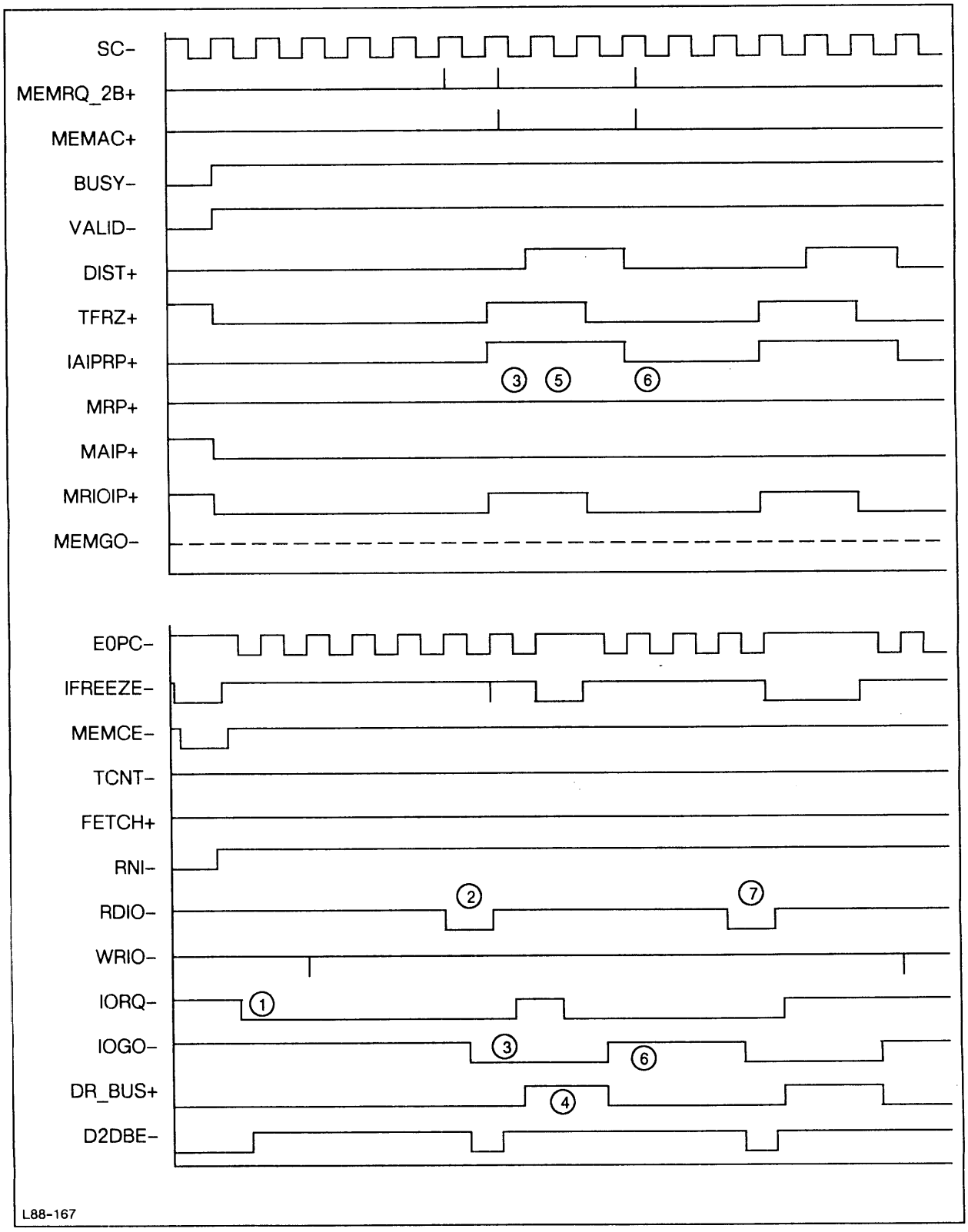


Figure C-5. I/O Handshake Read

I/O Handshake Write

The I/O Handshake write is identical to IOHS read, except for Step 7. IOHS Writes are generated from instructions such as OTA (Output from A to I/O interface). The processor must send data to the interface. It does so in the second transfer of the double-word transfer. This is shown in Figure C-6.

⑥ The processor examines the control word driven out during DR_BUS+. The control word indicates that the second transfer is a write.

⑦ When the processor is ready to send data to the I/O interface, it issues a WRIO to the MIOSM. This causes the MIOSM to assert IOGO–, to inform the interface to prepare to receive data.

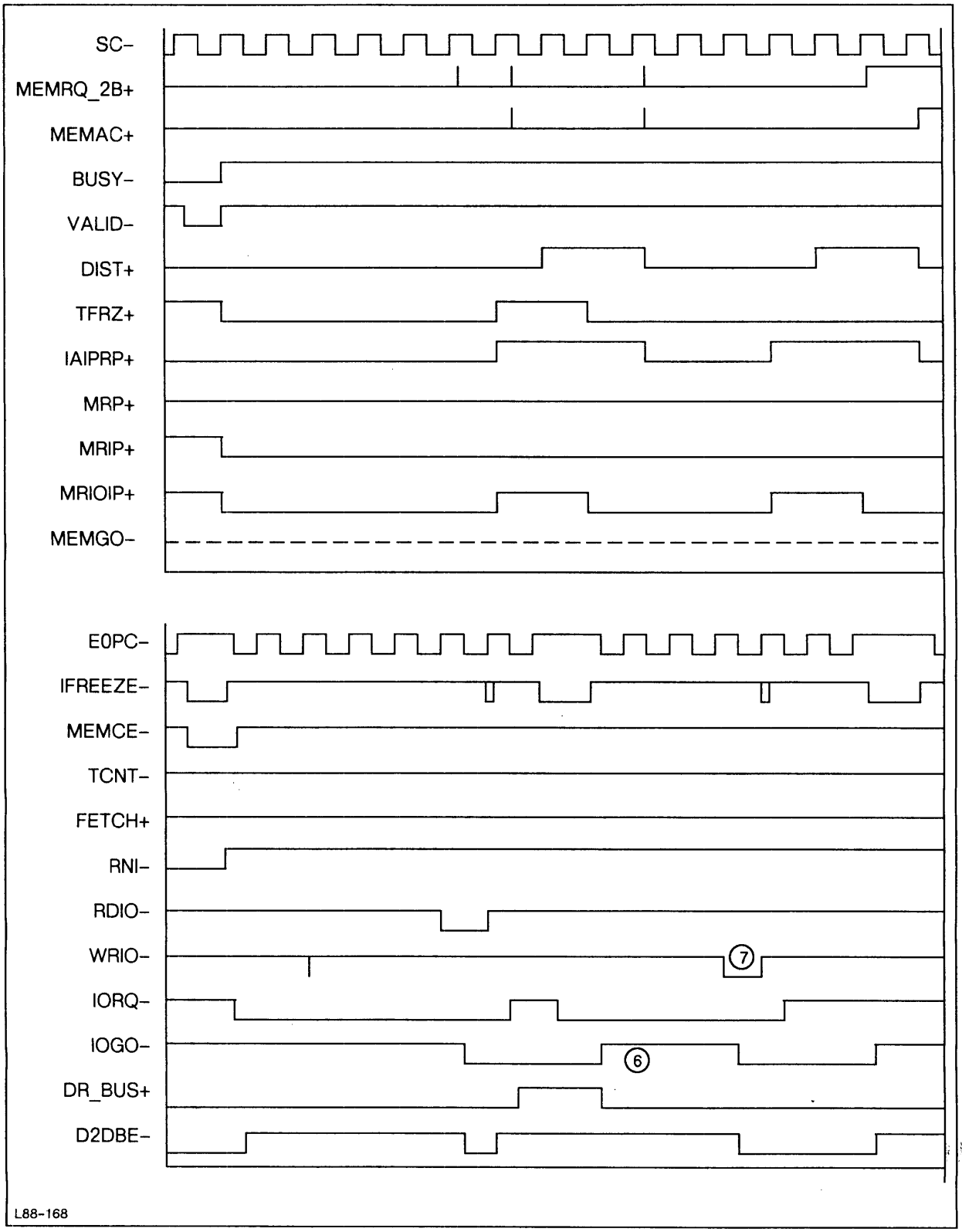


Figure C-6. I/O Handshake Write

Slave Mode Transfer

Slave mode transfers occur whenever a BREAK on the VCP device is detected, or a HLT instruction is encountered. Slave mode transfers cause the processor to enter VCP.

Slave mode transfers may be thought of as a special case of I/O handshakes. Five I/O Handshakes are performed in the process of executing a slave mode transfer. Figure C-7 illustrates the behavior of slave mode transfers.

IOHS 1: An RDP control word is received by the processor. This indicates that the slave interface wants to read the processor's program counter (P-Register).

IOHS 2: The processor completes this double handshake by sending its program counter value to the slave interface. The slave interface now has the location of where to restart the processor when it terminates VCP.

IOHS 3: An LDP control word is received by the processor. This indicates that the slave interface wants to load a value into the processor's program counter.

IOHS 4: The processor completes this double handshake by loading the data word from the slave interface into its program counter. This presets where the processor begins execution (in the VCP code) when the slave mode transfer completes. This VCP start address has been previously written to the interface.

IOHS 5: An ENR control word is received by the processor. This enables the VCP ROMs so that the processor can begin executing VCP code. The slave mode transfer completes with this single handshake (the continue, or "do another transfer" bit is zero).

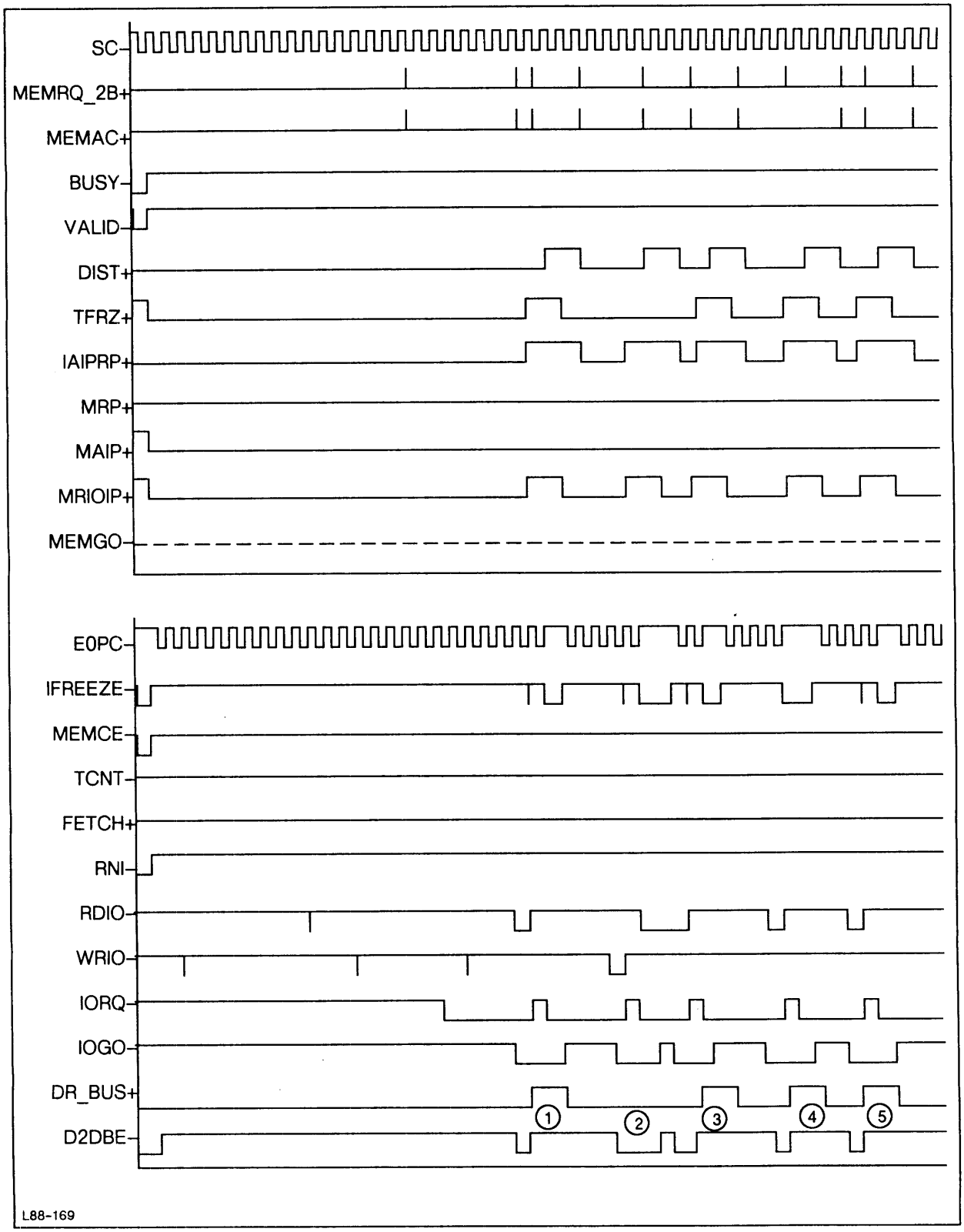


Figure C-7. Slave Mode Transfer

I/O Interrupt

This case illustrates an I/O Interrupt. Note that this is a fundamentally different mechanism than I/O handshakes. I/O handshakes are used in the execution of I/O instructions, such as LIA and OTA. I/O handshakes are used to transfer data between the A and B-Registers and the I/O interface.

I/O interrupts, on the other hand, serve to notify the processor of a specific event at the I/O interface. I/O interrupts cause the processor to invoke microcode interrupt handling routines to service the interrupt. Figure C-8 illustrates this.

① The I/O Interface asserts INTRQ– to notify the processor of an I/O event that requires service.

② INTRQ– sets the INTRQFF+ flip-flop, which in turn sets the INTP+ flip-flop. These flip-flops are part of the interrupt logic within the processor chip.

INTP+ is a signal which microcode may poll to determine if there is an interrupt pending.

③ INT+ is asserted when microcode does a fetch and INTP+ is set. INT+ causes microcode to abort the fetch and instead to trap to an interrupt handler. INT+ lasts for only one SC+ cycle.

④ The processor asserts IAK– to notify the I/O interface that it is now ready to service the interrupt. Note that the processor does not know which I/O interface has interrupted, or what interrupt handler to run. Therefore, IAK– also causes the interrupting I/O interface to drive its select code onto the backplane so that the processor knows this information.

Note that the processor requires several microseconds before it can service the interrupt. This is because the processor must save some of its state before servicing the interrupt.

⑤ At the same time, the processor microcode asserts IFCH– to fetch the interrupt handler address. This leads to MEMAC+ going true in the timing diagram.

This fetch proceeds as a normal one, except that the I/O interface is supplying the address. The I/O interface does this in response to IAK–. The I/O interface drives its select code out during MEMGO–.

The instruction returned from the interrupt fetch trap cell is usually a jump to the starting location of the interrupt handler.

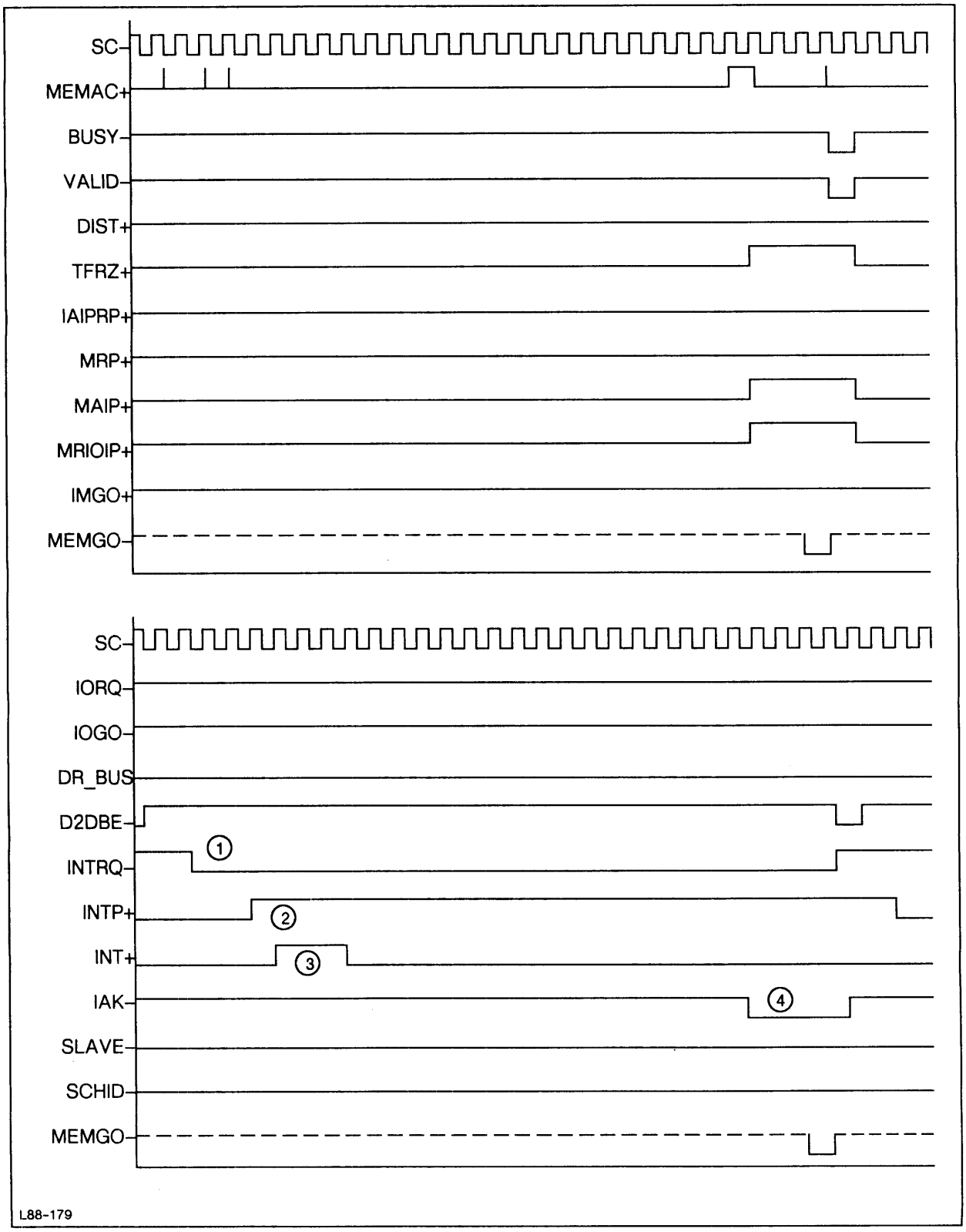


Figure C-8. I/O Interrupt

DMA Collision

This case illustrates the effects of DMA on the processor operations. Figure C-9 shows the start of a continuous stream of DMA transfers. This startup collides with a processor fetch.

① The processor asserts MEMAC+ to fetch an instruction. Shortly after this, an I/O interface asserts MRQ- to initiate a DMA transfer.

Both of these requests, MRQ- and MEMAC+, are received by the MIOSM. The MIOSM always gives priority to MRQ-, the DMA request signal.

② The MIOSM asserts IMGO+ in response to MEMAC+. However, IMGO+ is "killed" by the MRQ- signal. The result of this collision is a small glitch on MEMGO-.

③ Since BUSY- is false, memory is available therefore, the I/O interface asserts MEMGO- to start the memory access. Recall that MEMGO- is an open collector signal. It can be asserted by one of the following:

a) The processor (MIOSM) doing a memory access or fetch.

b) The interface driving a trap cell address during an I/O interrupt.

c) The interface performing a DMA transfer.

In this case, it is the interface driving MEMGO-. The MIOSM has aborted its own MEMGO- generation. This can be seen by IMGO+ remaining deasserted.

④ At the same time, the MIOSM goes to State 24 to "remember" there is a memory access pending, that is, the memory access corresponding to MEMAC+. The MIOSM waits for MRQ- to be deasserted before it carries out the pending memory access.

⑤ The processor does not know about the DMA activity, and assumes that the fetch has succeeded. When it goes to read the T-Register, a freeze occurs. The processor remains in this frozen state until the T-Register has the desired data.

The remaining MEMGOs are due to the stream of DMA transfers being performed by the interface card.

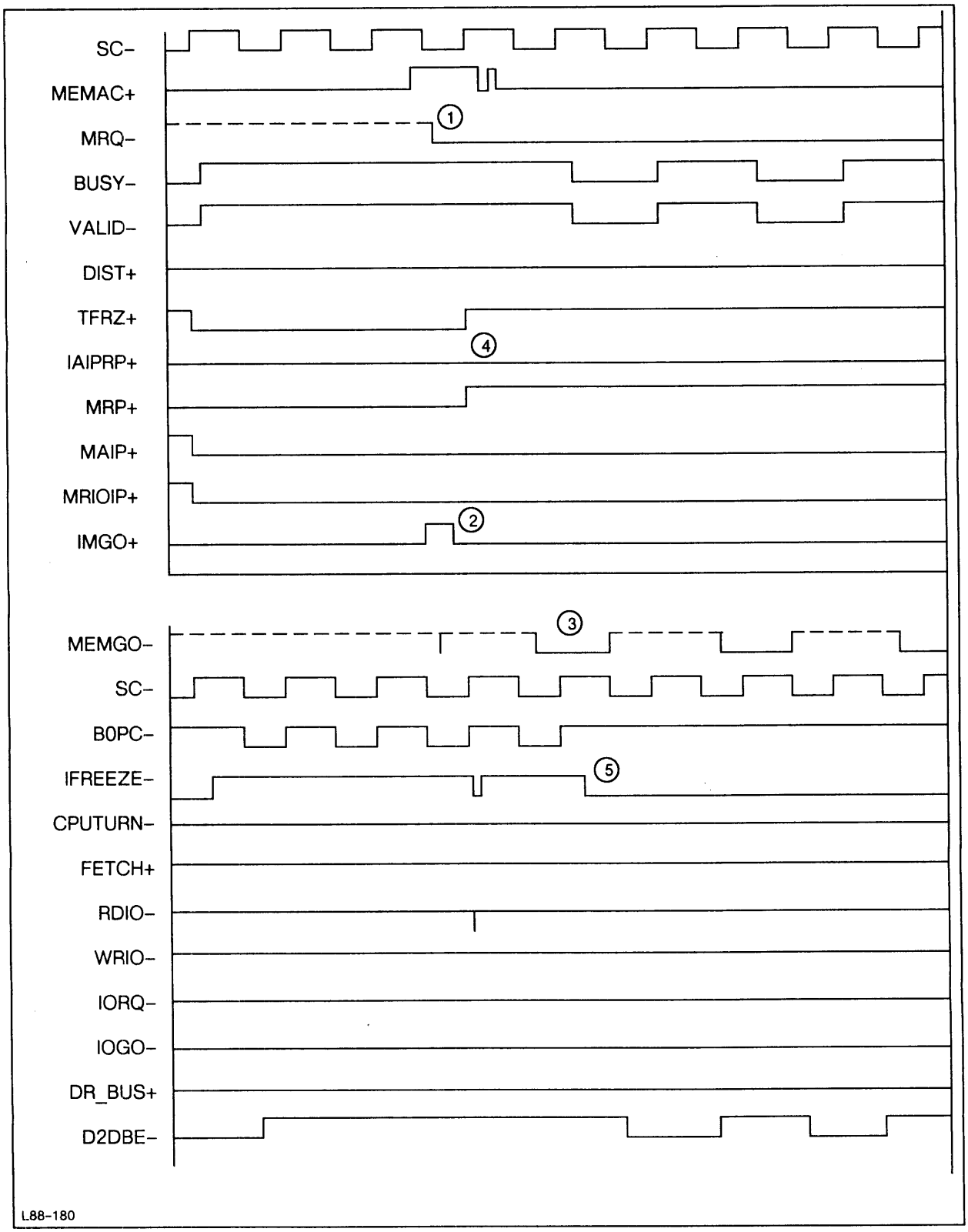


Figure C-9. DMA Collision

DMA Termination

Figure C-10 shows the termination of the DMA stream. In particular, it shows the processor asserting CPUTURN–, after being locked out of memory.

① In Figure C-10, the processor asserts CPUTURN– to command the interface to release MRQ–. The processor does this if it has been inhibited from getting a memory access for more than 32 consecutive memory access cycles.

② The interface complies by completing its DMA transfer in progress, and then deasserting MRQ–.

③ The MIOSM sees MRQ– and BUSY– deasserted so it asserts IMGO+ (which asserts MEMGO–) to initiate the memory fetch.

④ The MIOSM then goes to State 23 to wait for VALID– (not shown). When VALID– goes true, the fetch is complete and the MIOSM leaves State 23.

⑤ The processor sees that the T-Register has valid information, so the processor resumes operation. This causes the processor to also release CPUTURN–, since it is no longer frozen.

The interface may now reassert MRQ– to start up DMA transfers again.

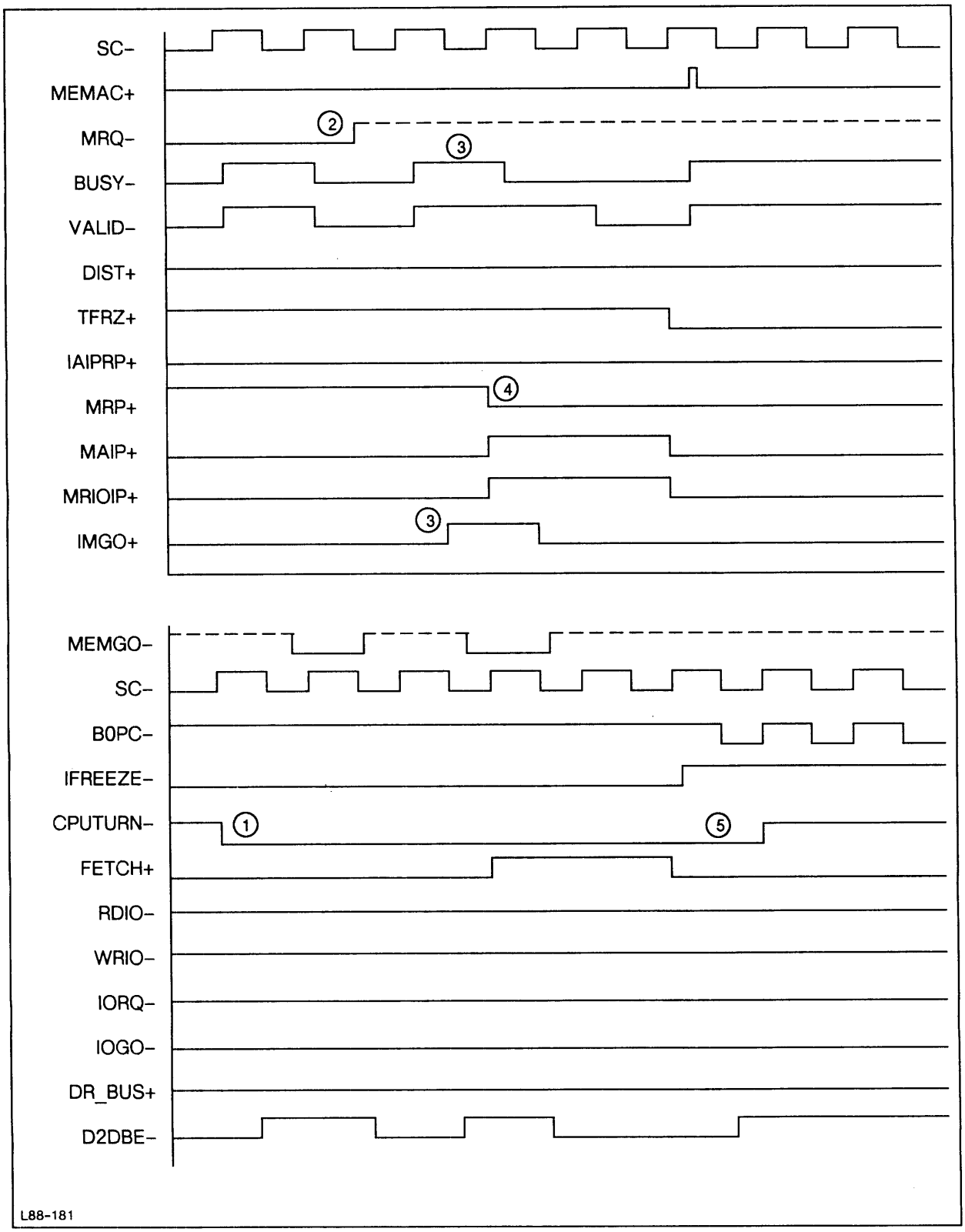


Figure C-10. DMA Termination

Index

F

G

I

L

M

Q

R

S

T

U

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