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NOTE

This EPS-1, if not revised within one year, should be considered obsolete and therefore reference should be made to the appropriate Product Manual.

| Honeywell<br>HONEYWELL INFORMATION SYSTEMS | | SPEC. NO.<br>60132445 | SHEET<br>1.1 | REV.<br>F |
|---|---|---|---|---|

HONEYWELL INFORMATION SYSTEMS
SYSTEMS ENGINEERING - BOSTON

# ENGINEERING PRODUCT SPECIFICATION ( EPS - 1 )

SUBSYSTEM LEVEL

TITLE: LEVEL 66 FEP COUPLER

VERSION: APPROVAL DATE: 11/23/77

PRODUCT CALENDAR REFERENCE:
5A0503

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## ILLUSTRATIONS



## TABLES

# 1 INTRODUCTION

## 1.1 SCOPE

This document describes the functions, operation, performance, interfaces and design requirements of a Front End Processor Coupler for connecting a Level 66 Central System, through its Direct Interface to a Front End Processor System.

## 1.2 APPLICABLE DOCUMENTS

1. Engineering Product Specification, Part I, General Remote Terminal Supervisor - 355 [GRTS], drawing number 43A219619.
2. Engineering Product Specification, Part I, Network Processing Supervisor [NPS 355], drawing number 58001149.
3. Engineering Product Specification, Part I, 355 Direct Interface Adapter, drawing number 58001131.
4. Engineering Product Specification, Parts I and II, New Minicomputer Line System, drawing number A60126448.
5. Product Functional Specification, NML Product Line, document number 60124991.
6. Engineering Product Specification, Part I, NML Bus, document number 60126298.
7. Engineering Product Specification, NML L100 CPU, EPS-1, document number 60126882.

8. Engineering Product Specification, Part I, NML 150 CPU, document number 60130080.
9. Product Functional Specification, Level 6 Model 6/40, document number 60129734.
10. Engineering Product Specification, HNP Direct Interface Adapter, drawing number 58008520.
11. Engineering Product Specification, Part I, NML Full Secure Memory Management, drawing number 60131306.
12. Engineering Product Specification, Part I, NML 150 CPU Memory Management, drawing number 60130079.
13. Engineering Product Specification, Part I, NML Multi Line Communications Processor, drawing number 60126885.
14. Engineering Product Specification, 6000 Input/Output Multiplexer (IOM) Central, drawing number 43A219604.
15. Interface Specification, Direct Channel, drawing number A58001102.

## 1.3 DEFINITIONS

CPU - Central Processor Unit
DCW - Data Control Word
DIA - Direct Interface Adapter
FEP - Front End Processor
HDIA - HNP Direct Interface Adapter
HMLC - HNP Multi Line Controller
HNP - Honeywell Network Processor (Datanet 6678)
ICW - Indirect Control Word
IOM - Input/Output Multiplexer
LPW - List Pointer Word
MLCP - Multi Line Communications Processor
MMO - Memory Management Option
NML - New Minicomputer Line (Level 6)
NPS - Network Processor Supervisor
PCW - Peripheral Control Word
RFU - Reserved for Future Use
RHU - Reserved for Hardware Use
SPM - Security Protection Module
TBD - To Be Defined
VMIU - Virtual Memory Interface Unit

# II
# ARCHITECTURE

## 2.1 GENERAL OVERVIEW

The coupler is a controller which under program control provides a path for program intercommunications and data transfer between a Level 66 processor system and a Front End Processor System. The Front End Processor may be a DN6678, in which case the functionality of the coupler is the same as described in the reference specification for the HDIA. Alternatively, the Front End Processor may be a Level 6 system, in which case the coupler's functionality is as described in this specification.

Program intercommunication between programs in the two processors is carried out by means of messages transferred in or out of a set of logical channel Mailboxes located in processor system memory, and data transfers move quantities of data between data buffers of the two systems memories; these operations are carried out by the coupler either under direct command of a processor instruction or as part of execution of a channel program resident in processor system memory which is executed by the coupler when a channel program starting command is issued by the processor.

The overall interprocessor communication function is implemented by the hardware-firmware of the coupler under control of driving software in both processors. A software package already exists for the Level 66 processor which provides intercommunication to a DN355 or HNP Front End Processor via the DIA or HDIA. The coupler provides an interface to the Level 66 processor such that this software can continue to be used to provide intercommunication to a Level 6 Front End processor; a new software package must be written for the Level 6 to furnish the same functionality on Level 6 as existed in the DN355/HNP software.

The coupler provides for Bootload of the FEP by the central system.

The coupler will operate with the Level 6 Model 4X Memory Management Option in commercial applications as represented in Figure 2-1.

In addition, the coupler provides support for Full Secure Communication processor applications. A special Level 6 processor and Security Protection Module is used for these applications as shown in Figure 2-2.

## 2.2 OPERATIONS OVERVIEW

### 2.2.1 Control Intercommunication

In Level 66 memory, at a location known to the coupler and to Level 6 software is a mailbox area consisting of an Overhead mailbox and 7 Channel mailboxes. The size, relative positions, and contents of these areas are known only to software. The channel mailboxes are used, on a half-duplex basis, for control intercommunications between processors; Level 66 software is responsible for selection and traffic control among mailboxes.

Interrupts, sent from one processor to the other, signal the availability of a control message in a channel mailbox. The interrupt, by setting a particular cell or interrupt level, indicates which mailbox contains a message. It is a software responsibility to move a message into or out of a mailbox from the Level 6 system.

The Overhead mailbox contains information which aids the Level 66 software in managing the channel mailboxes. The formats, contents and updating of this area is entirely a software function, controlled by Level 66 and Level 6 software.

A view of these areas is shown in Figure 2-3.

### 2.2.2 Typical Operation

Operation as described here is based on existing software. A typical sequence of operations to input a transaction from Level 6 to Level 66 would be as follows:

a. Level 6 software, which is initiating the intercommunication, sends an interrupt to the Level 66 system. The cell number at which it interrupts the Level 66 has a correspondence with the channel mailbox number which it would like to use for the message. The coupler simply sets the indicated interrupt cell in the Level 66 system.

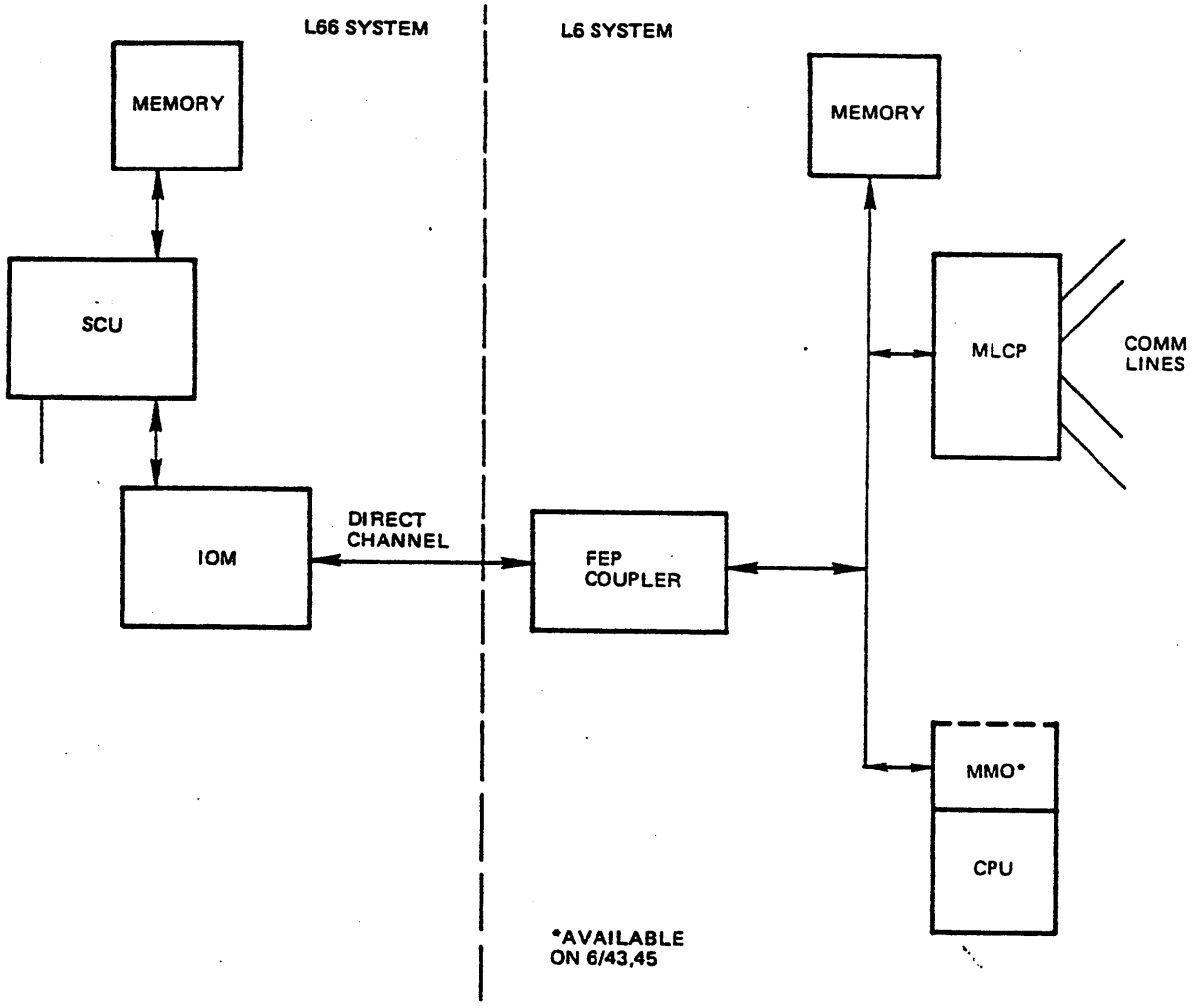



Figure 2-1 L6 FEP (Commercial) System

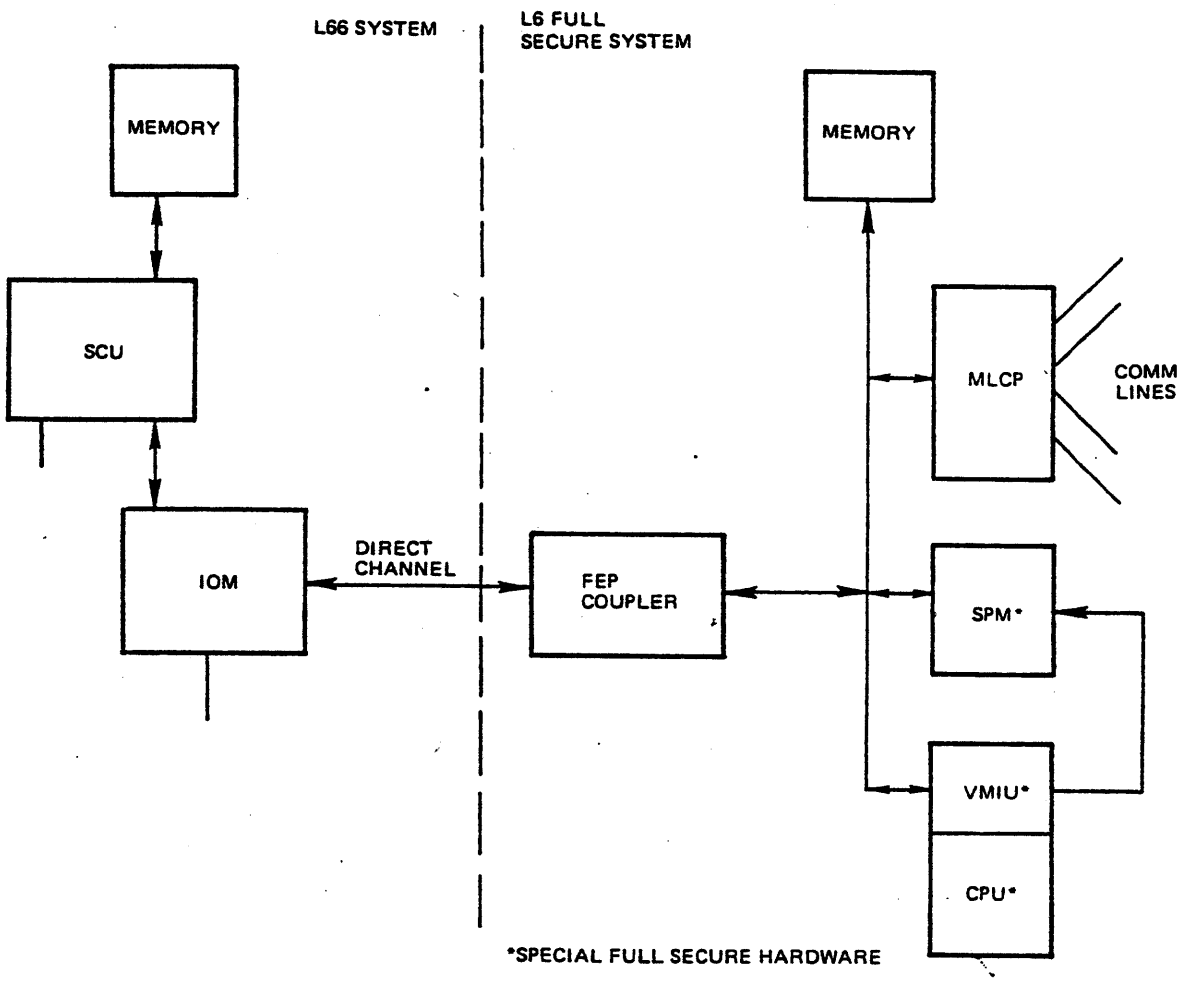



Figure 2-2 L6 FEP (Full Secure) System

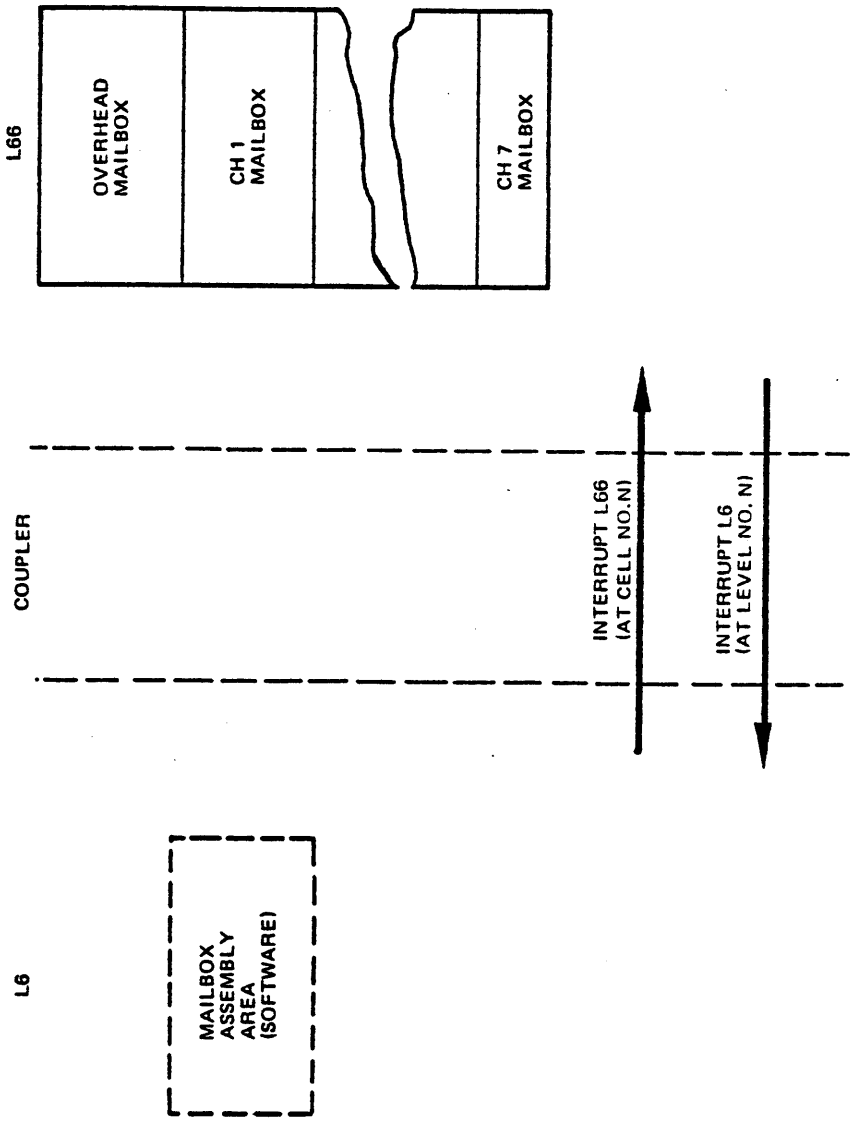



Figure 2-3 Control Intercommunication

b. Level 66 software, if the indicated mailbox is available, places a Read Control Data message in the mailbox in its memory and sends an interrupt to the Level 6 system; the cell number used on this interrupt corresponds to the channel number. The coupler interrupts the Level 6 system at a fixed level and stores the cell number internally.

c. Level 6 software issues an IO order to the coupler to obtain the cell number. It then composes and issues a DCW to the coupler in order to transfer the contents of the appropriate mailbox from L66 memory to a working area in its own memory.

d. When the coupler has completed this transfer, Level 6 software sees the Read Control Data message. It then composes a return message for the mailbox and composes and issues two DCWs to the coupler (one to transfer the message into the mailbox in the Level 66 memory, and one to interrupt the Level 66 at a cell number corresponding to the channel). The coupler does the transfer and sets the indicated cell.

e. Level 66 software sees the control information sent by Level 6 and takes appropriate action. In many, if not most cases, some sort of acknowledgement or further command would also need to be sent to Level 6; this would be done via a series of operations similar to parts (b) and (c) above and finally Level 6 software would acknowledge receipt of this final message by operations similar to part (d) above. Level 66 software would then see this acknowledgement and release the mailbox.

### 2.2.3 Data Transfer Architecture and Intercommunications

All data transfer operations (other than for T&D) must be initiated by a channel program issued by the Level 6 system. Thus Level 66 software must always furnish primitive DCWs (i.e., a Level 66 memory starting address and Tally) to Level 6 software through information placed in a mailbox.

Whenever Level 6 software wishes to initiate a request for data transfer a series of intercommunications similar to parts (a) through (e) of Section 2.2.2 must be performed; the final command, of part (e), from the Level 66 would be a Write Text or Read Text command and would include address and Tally of a primitive DCW. The Level 6 software would then compose the DCW and issue it to the coupler; on completion of the transfer, a final acknowledgement would be sent to Level 66 to release the mailbox.

If Level 66 software wishes to initiate a request for data transfer a similar series of intercommunications would be carried out, except that part (a) would be omitted since Level 66 can select an available mailbox immediately.

Only one channel program can be executed at a time by the coupler; however, Read and Write transfers, sending and receiving of mailbox messages by Level 6, and sending of interrupts may all be interspersed in a single channel program as needed.

### 2.2.4 Mailbox and DCW Formats

Figure 2-4 shows the formats of mailboxes in Level 66 memory as defined by existing Level 66 software usage. As noted previously, these formats are defined entirely by software usage since the coupler has no knowledge of their extent or contents.

Figure 2-5 shows the format of DCWs issued by Level 6.

OVERHEAD AREA

| | 0 | 18 | 24 | 30 | 35 |
|---|---|---|---|---|---|
| 0 | | 0 | | CHANNEL # | COMMAND |
| 1 | | # SPECIAL INTERRUPTS | | | |
| 2 | TERMINATE 1 2 3 4 5 6 7 | | | | |
| 3 | | | | | |
| 4 | | | | | |
| 5 | 355 CONTROL SOURCE | # LINES CONFIGURED | | | |
| 6 | POINTER FOR LINE CONFIG. | | | | |
| 7 | POINTER FOR ANOTHER SYSTEM | | | | |

CHANNEL MAILBOX AREA

| | 0 | 3 | 9 | 18 | 27 | 35 |
|---|---|---|---|---|---|---|
| 10,20,...70 | 355 # | LINE NUMBER | | TERMINAL ID | | |
| 11,21,...71 | TERMINAL TYPE | # CHAR IN COMM DATA | | OP CODE | I/O COMMAND | |
| 12,22,...72 | | | | | | |
| 13,23,...73 | | | | | | |
| 14,24,...74 | | | | | | |
| 15,25,...75 | RELATIVE DATA ADDRESS | | | | WORD COUNT | |
| 16,26,...76 | | STATUS CODE | | DCW RESIDUE | | |
| 17,27,...77 | SLAVE PROGRAM LIMITS | | | CHECKSUM | | |

Figure 2-4 Mailboxes

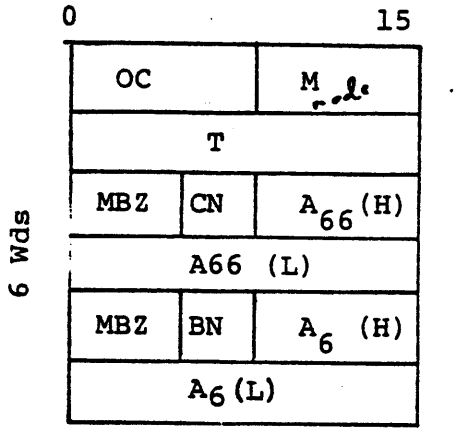



Figure 2-5 DCW Format

# III FUNCTIONAL DESCRIPTION

## 3.1 GENERAL

The Coupler provides a data and control link between a Front-End Processor (FEP) and a Level 66 host central system. In normal inter-computer transfer activities the Coupler acts as an agent of the FEP which controls all detailed activities. The Coupler responds to external stimuli from the FEP and host central system.

The Coupler consists of FEP and central system interfaces, registers to retain information during transactions, information path steering/packing/unpacking, parity checking and generation, configuration information, and control functions. The implementation of the Coupler allows for secure and non-secure FEP hardware subsystems.

## 3.2 INTERFACES AND CONFIGURATIONS

The Coupler provides a connection between a single host and a single FEP system. The use of more than one Coupler allows interfacing for configurations of multiple FEP's connected to a single host or a single FEP connected to multiple hosts. When multiple Couplers are needed, multiple central IOM/DCA interfaces are required. For a multiple host configuration, there will be a minimum of one Coupler per host (a single FEP may support multiple Couplers).

Note that HIS-supplied communications software does not necessarily support all possible physical configurations.

The Coupler interfaces with the L66 Direct Channel and with the appropriate FEP bus as described in reference specifications. Each interface contains address, data, timing, control, and miscellaneous signal information.

## 3.3 DATA TRANSFER MODES

Transfers to/from the L66 through the Direct Interface are always performed on a 36 bit word basis. The L6 bus interface has a byte write functionality which may be used occasionally by the coupler; but, in the main, transfers to/from the L6 are performed on a 16 bit word basis. The effective beginning and ending locations and extent of a transfer as viewed from the effect upon memory contents may be either word-bound or byte oriented, depending upon the mode used for the transfer.

### 3.3.1 Transfer Formats

Three transfer format modes (pack/unpack) are provided: Binary mode, BCD mode, and ASCII mode. The mode to be used for a transfer is specified in the DCW. There are three commands which can be issued by L66 by means of a PCW which result in a transfer; these are the Test Data Transfer and the Bootload; these transfers will always be performed using ASCII mode transfers.

In Binary mode, shown in Figure 3-1, transfers always begin on a word boundary in both L66 and L6 and the extent (Tally) is always in terms of a number of 36 bit words. Binary transfer always ends on a word boundary in L66 but may end on a word, byte or partial byte in L6; when ending on a byte, the other byte in the word is not accessed while if ending on a partial byte unused bits are discarded or zero filled as appropriate.

In BCD mode, shown in Figure 3-2, transfers always begin and end on a word boundary in both L66 and L6 and the extent (Tally) is always in terms of a number of 36 bit words.

In ASCII mode, shown in Figure 3-3, transfers may begin and end on any byte boundary in both L66 and L6 and the extent (Tally) is always in terms of a number of bytes. The case shown in Figure 3-3 is the special case when both start on a byte which is also a word boundary.

### 3.3.2 Transliteration Modes

Two transliteration modes of transfer are provided: Transliteration Mode A and Transliteration Mode B. These modes use the same packing/unpacking algorithm as ASCII mode including Tally interpretation and starting and ending boundaries, but also provide translation of the data from one 8-bit code to another 8-bit code. The translation tables are shown in Section IV. Figure 3-4 shows transliteration mode in the special case when both L66 and L6 start on a byte which is also a word boundary.

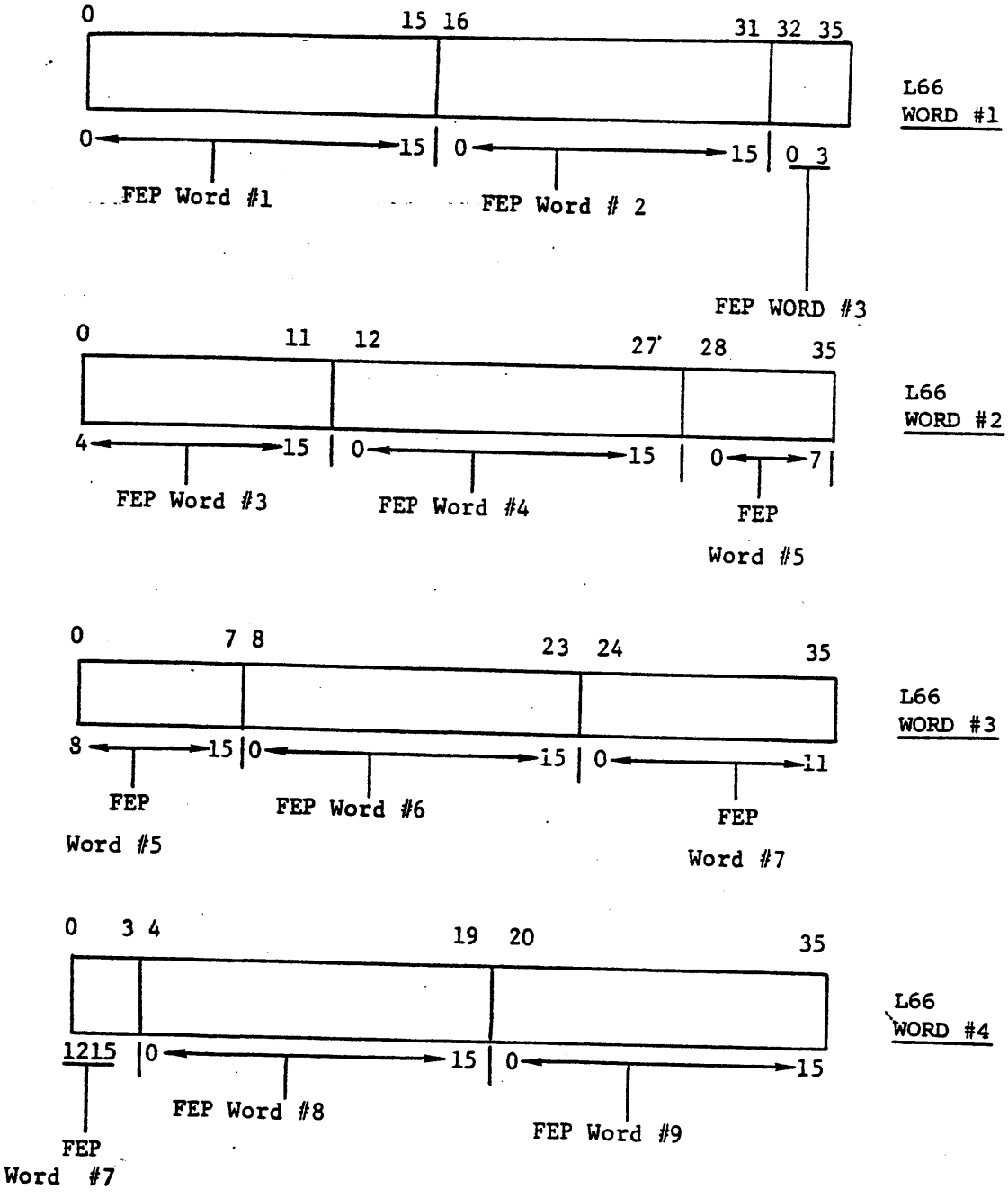
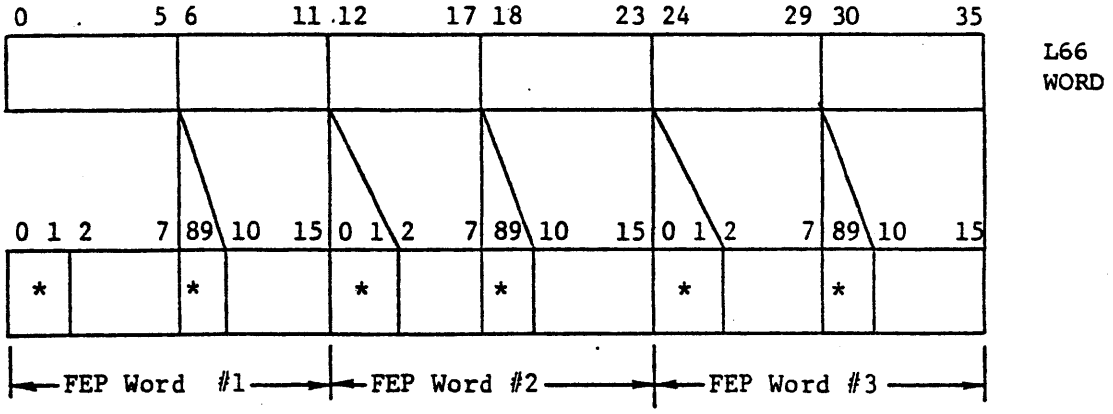
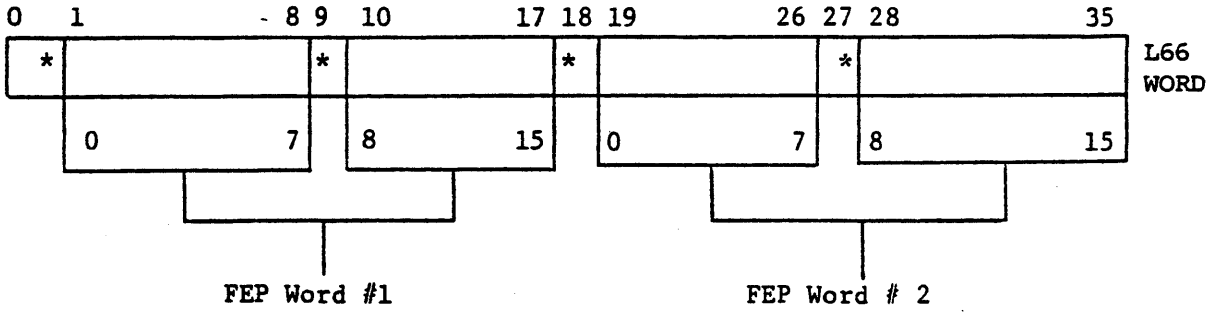



Figure 3-1 Binary Format



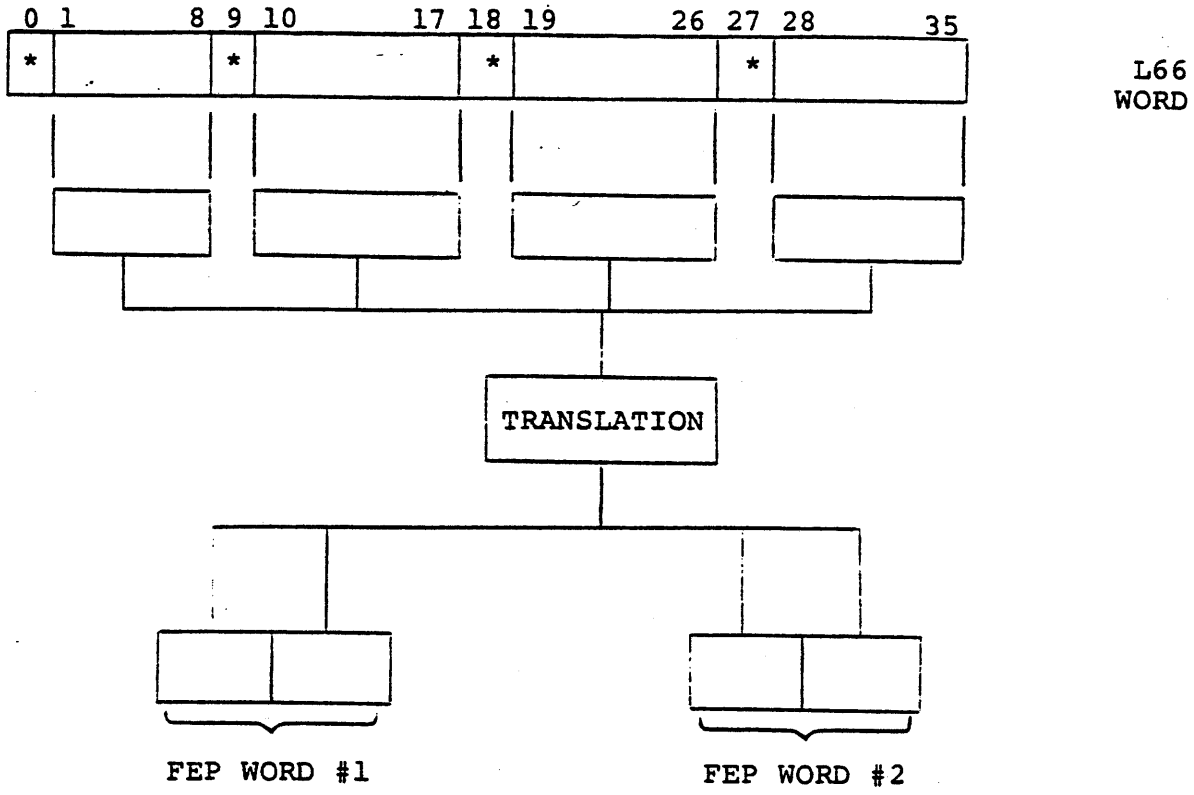

*Bits forced to zero or discarded during transfer

Figure 3-2 BCD Format




*Bits to be forced or interpreted as zero

Figure 3-3 ASCII Format




*Bits to be forced or interpreted as zero.

Figure 3-4 Transliteration Mode

## 3.4 HARDWARE ORGANIZATION

Figure 3-5 is a conceptual block diagram of the coupler showing registers and information paths for accomplishing the functions required.

### 3.4.1 Data Registers (L66 and L6)

These registers interface with the appropriate data bus as shown.

### 3.4.2 Address, Control and Status Registers

#### 3.4.2.1 L66 Bus Address Register

This register contains the L66 address to or from which information is to be transferred via the L66 Data Register.

#### 3.4.2.2 L6 Bus Address Register

This register contains the L6 address to or from which information is to be transferred via the L6 Data Register.

#### 3.4.2.3 L6 DCW List Registers

These registers contain the starting address and range of an area in L6 memory which contains DCWs. They are loaded by a DCW list IOLD.

#### 3.4.2.4 Barricade Registers

One register set is provided, the set consisting of a base and a size register. When the FEP BAR is set their contents define an area in L6 memory in which reading or writing is permitted. They are loaded by Load Barricade IOLD orders.

#### 3.4.2.5 DCW Offset Register

The DCW Offset Register contains the offset of the next L6 DCW to be executed by the coupler relative to the start of the list. It is set to Zero by a DCW List IOLD and is loaded by a Jump DCW and is also incremented during list processing.

#### 3.4.2.6 Checking Logic and Status Registers

This logic performs checking and generation of parity for data transfers, legality checks on commands, format checks on DCW lists, checks on range exhausts, timeouts on response from L66 or L6, etc. Results are stored in status register(s) for transmittal to the processor.

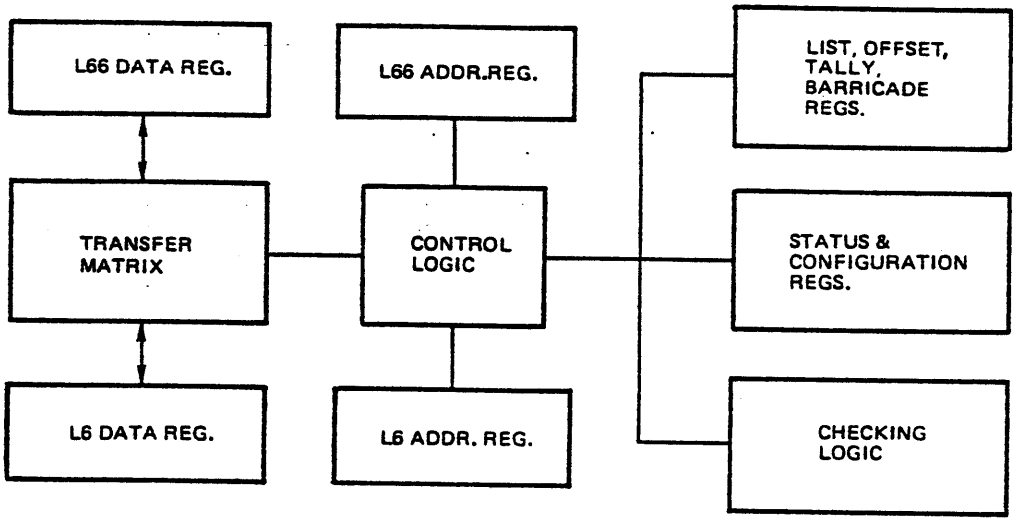



Figure 3-5 Coupler Block Diagram

Status register(s) retain the results of the various checks.

The program must execute specific IO orders to retrieve status. The format of the status registers is shown in Section IV.

### 3.4.2.7 Task Register

The register contains a Throttle Control bit, a Bootload Inhibit bit and cells to be used for L66 Test/Termination Interrupts and L66 Special Interrupts.

### 3.4.2.8 Tally Register

The register contains a count of the number of L66 data words or bytes remaining to be transferred under the current DCW. It is loaded from the contents of a DCW.

## 3.4.3 Configuration Registers and Switches

Configuration registers may be implemented either in hot storage registers or in cold switch registers as specified below. All switch registers and switches are implemented using rotary DIP switches mounted on the coupler board.

3.4.3.1 L66 Mailbox Address

This 12 bit register is implemented with switches and is set to define the location in L66 memory known as the L66 mailbox. The location of this mailbox can be any modulo 64 word address between zero and 777700 octal. The setting of this register can be read by the L6 by means of the Report Configuration Status command.

3.4.3.2 Coupler Channel Number Switches

These switches define the coupler's channel numbers in the L6 system. The high order 8 bits of the channel number can be set by these switches and define a set of 4 channels to which the coupler will respond.

Channels 0 and 1 must be used for all IOLD and all IO orders except interrupts. Channels 2 and 3 must be used for the interrupt type IO orders.

3.4.3.3 L6 Interrupt Control

This register contains the channel number of the L6 CPU to which the coupler is to report interrupts destined for the L6 system. It also contains the 6 bit interrupt level to be used for normal terminations of a DCW list issued by L6. The register may be loaded or read by L6 program as specified in section 3.6.

3.4.3.4 Configuration Register A

This register contains security control bits, test mode control bits, and interrupt level to be used on Interrupt L6 commands. The register may be loaded or read by L6 program as specified in sub-section 3.6.

3.4.4 Transaction Timer

The coupler provides a time-out function on transactions with the L66 system. If the L66 system fails to respond within 10 milliseconds, the timer will cause the coupler to terminate the operation and disconnect. A Terminate interrupt is sent to the L6 and suitable indication of the timeout occurrence is given in the status. The timeout is forced to occur if "DC-INIT" on the Direct Channel interface is true. No timeout function is required in the coupler for the L6 since this system includes a "dead man" timer on the bus which insures that a NAK response will occur if no unit responds to a bus transaction. Receipt of a NAK response from the L6 system causes the coupler to disconnect, set Non-existent Resource status and interrupt the L6; if the L6 CPU fails to respond to the interrupt the coupler will send a Special interrupt to the L66.

### 3.4.5 Rate Throttle

The coupler provides a rate throttle which can be turned on or off under software control and which enforces a maximum transfer rate on the coupler (when the TH bit in the Task Register is a ONE).

## 3.5 OPERATIONS

The Coupler has two interfaces, one through a Direct Channel of the Central System and the second through the bus of the FEP. It will respond to a stimulus from either interface although it does not use the same functional abilities on both interfaces. The interface to the Central System provides less functionality in that List Processing is not used, so the command set is more restricted. This simply reflects the fact that the FEP has responsibility for detailed control of the Coupler; the Central System is still the overall master.

At the coupler's interface with the central system the stimulus to which it responds is that of a Connect.

At the coupler's interface with the L6 the stimulus is that of an IOLD or IO.

### 3.5.1 Commands Issued by Central System

In the issuing of an order by the Central System to the Coupler, the following sequence occurs:

1. The L66 program creates a List Pointer Word (LPW) and a PCW for the Central System Connect Channel. It also generates and stores a control word containing a command in the L66 mailbox which was set up for the Coupler (see section 3.4.3.1). A Connect is then issued to the L66 IOM.

2. The Connect Channel in the L66 IOM, on receipt of the Connect, accesses the LPW and uses its contents as an address to fetch the PCW. The PCW contains the channel number of the Direct Channel to which the Coupler is connected. As a result of this PCW the Direct Channel sends a signal to the Coupler indicating that a Connect has been issued to it by the Central System.

3. The Coupler now reads the content of its L66 mailbox, thereby obtaining the control word placed there by the Central System program. If the control word is legal, the Coupler will write a word of all zeros into the L66 mailbox after successful completion of the requested operation.

4. When the L66 program sees a word of zeros in the mailbox location it knows the command has been accepted and acted upon and may if it wishes store a new PCW in the mailbox for issuance to the coupler.

The central system cannot initiate a list of operations in the coupler; the op codes used in mailbox words define a single operation which the coupler is to perform as a result of the L66 Connect.

Following is a list of op codes which may be used in a PCW issued by the central system to the coupler. Certain of these op codes are conditionally legal, indicated with an asterisk (*); the conditions for legality of these is given in the description of the operation. All other op codes are illegal.

| OP Code (Octal) | Operation |
|---|---|
| 71 | Interrupt L6 |
| 72* | Bootload L6 |
| 73 | Interrupt L66 |
| 75* | Test Data Transfer from L6 to L66 |
| 76* | Test Data Transfer from L66 to L6 |

If an illegal op code is received from the L66 system, the action taken by the coupler depends upon whether the coupler is also currently busy performing a list of operations for L6.

If the coupler is busy performing a list of operations for the L6 when the illegal op code is found in the L66 mailbox, the coupler will restore the PCW containing it into the L66 mailbox except with bit 18 inverted from the value given it initially by the L66 (by software convention, the L66 always gives bit 18 a value of Zero). The occurrence of the illegal PCW will now be registered in the coupler's status register along with Attention status; the list processing is stopped and a termination interrupt is sent to L6. The coupler enters a Status Pending state (see subsection 3.5.3).

If the coupler is not busy performing a list for the L6 when the illegal op code is found in the L66 mailbox, the coupler will restore the PCW containing it into the L66 mailbox except with bit 18 inverted from the value given it initially by the L66 (by

software convention, the L66 always gives bit 18 a value of Zero). The occurrence of the illegal PCW will now be registered in the coupler's status register and the L6 will be interrupted at the Terminate interrupt. The coupler enters a Status Pending state (see subsection 3.5.3).

If a fault (parity, etc.) occurs in executing an operation initiated by L66, the operation is not completed and the PCW in the L66 mailbox is left there unaltered. If the coupler is also busy performing a list for the L6 when this fault occurred, the list processing is stopped, the occurrence is registered in the coupler's status along with Attention status, and a termination interrupt is sent to the L6. If the coupler is not busy performing a list for the L6 when the fault occurred, the occurrence is registered in the coupler's status and a termination interrupt is sent to L6. The coupler enters a Status Pending state (see subsection 3.5.3) in either case.

If the coupler cannot communicate with the L6, it will set the L66 Special Interrupt cell in the L66 system (the cell number is defined in the Task Register).

### 3.5.2 Commands Issued by L6 FEP

As opposed to the L66 interface which initiates only a single operation in the coupler for each order issued by the processor, the FEP interface uses list processing as the predominant mode. Each order issued by the FEP will start the coupler executing a pre-stored list of instructions, essentially a channel program. The FEP uses a richer command repertoire than the Central System as far as the coupler is concerned.

The following gives a general idea of the sequence of steps which occur for I/O initiated from the FEP.

1. The FEP program generates and stores in its memory a list of Data Control Words (DCWs) and other control words if required, which define a sequence of data transfers, etc., to be done by the coupler.

2. The FEP program executes an initiation order to the coupler (i.e., a DCW List IOLD).

3. The coupler obtains the address of the DCW list from the order and fetches the first DCW.

4. The coupler performs the operation specified in the DCW. When completed, and assuming that the operation did not result in an abort condition, before proceding to the next DCW the coupler scans for other demands upon its facilities and performs the requested operation:

a. An accepted but as yet unexecuted interrupt order from the L6

b. An outstanding PCW in the L66 mailbox.

When these inter-DCW demands have been satisfied, the coupler fetches the next DCW from the list and performs the indicated operation.

5. The sequence of fetching and performing DCWs continues until a terminate condition, typically a disconnect operation, is reached.

6. The coupler interrupts the FEP to indicate termination.

If a fault (parity, etc.) occurs in executing a DCW or in executing one of these operations, the coupler will abort the operation and stop list processing. The occurrence will be registered in status along with Attention status and a termination interrupt will be sent to L6. The coupler enters the Status Pending state (see subsection 3.5.3).

The L6 processor uses both word I/O (IO) and Address and Range I/O (IOLD) orders to control the coupler. The IOLD orders are used in initiating list processing while the IO orders are used to configure and read status of the coupler and to send interrupts.

There are two kinds of IOLD used for the coupler. One of these (DCW List) is used to point to the list of DCWs to be performed and the other (Load Barricade) is used to delimit the FEP data area to be used on list processing operations when the FEP BAR bit is on. The latter order must be used whenever the FEP BAR bit is on; otherwise its use is ineffective.

Before issuing the DCW List IOLD, the L6 program generates a list of DCWs, each of which defines an operation to be done and includes other required information for the operation, such as addresses, tallies, transfer modes, etc. Each DCW occupies six L6 word locations. In addition, if the FEP BAR bit is ON the transfer must occur from or to a single contiguous data area in the L6 store; the data must be so located and a Load Barricade IOLD must be executed before the list processing IOLD is executed.

Following is a list of Function Codes and Op codes which are used in IO orders, IOLD orders, and DCWs issued by L6 to the coupler.

Function codes used in orders addressed to channel 0 or 1 of coupler:

| Function Code | Operation |
|---|---|
| 01 | Output Control |
| 02/03 | Interrupt Control Register |
| 06/07 | Task Register |
| 09 | DCW List IOLD/Input Stored Boot |
| 0B | Load Barricade IOLD |
| 0C | Read DCW Offset Register |
| 10/11 | Configuration Register A |
| 18/1A | Read Status Register 1/2 |
| 26 | Read Device ID |
| 19 | Dump Scratchpad IOLD (T&D only) |

NOTE

All other function codes to channel 0 or 1 are illegal.

Function codes used in orders addressed to channel 2 or 3 of coupler (interrupt orders):

| Function Code | Operation |
|---|---|
| X1,X5,X7,X9, XD,XF | RFU |
| X3/XB | Interrupt L66 |

NOTE

All even numbered function codes addressed to channel 2 or 3 will be rejected. "X" denotes a "don't care" hex digit.

DCW op codes used in list processing:

| DCW Op Code | Operation |
|---|---|
| 30 | Disconnect |
| 37 | Internal Wraparound (T&D only- see subsection 7.3.3) |
| 38 | Disconnect & Interrupt |
| 39 | Interrupt L6 |
| 3A | Jump |
| 3B | Interrupt L66 |
| 3C* | Store Configuration Status |
| 3D* | Data Transfer from L6 to L66 |
| 3E* | Data Transfer from L66 to L6 |
| 35* | Read & Clear L66; OR to Store L6 |
| 33 | No Operation |
| 34 | Stall |

NOTE

All other op codes are illegal. *These op codes are conditionally legal as described in subsection 3.6.

If the coupler is busy processing a list or L6 order it will accept and execute any legal order from L66 on completion of the current DCW or operation; handling of faults or an illegal PCW is also described above and in subsections 3.5.1 and 3.5.3.

When the coupler is busy processing a list or L66 order, it will accept an Output Control order from the L6 and will also accept interrupt orders from the L6; however, it will accept only one such interrupt at a time. It will not accept a new interrupt from L6 until it has completed execution of the prior issued interrupt order; as described above, this occurs on completion of the current DCW.

Acceptance or rejection of orders issued by L6 to the coupler is made visible to software by the state of the I bit in the L6 Indicator register; L6 software should always test this bit after every order it issues to the coupler.

If a fault occurs in executing an IO order and the coupler is not busy processing a list, the coupler will indicate the fault in status and will sent a Termination interrupt to L6. The coupler enters Status Pending state (see subsection 3.5.3).

If an illegal Function Code is issued by L6, the coupler will store that fact in its status register and the L6 will be sent a termination interrupt. If an illegal DCW Op Code is issued by L6, the coupler will store that fact in its status register along with Attention status and aborts list processing and interrupts L6. Software may then read the DCW Offset register to locate the offending DCW. If a DCW must be aborted during execution due to a parity error or protection violation, for example, the coupler so indicates in status, sets Attention status and interrupts L6. In all of these cases, after sending the interrupt to L6 the coupler enters the Status Pending state.

### 3.5.3 Status Pending State

The Status Pending state is a state which the coupler enters whenever an event concerning an order issued to it has occurred and must be reported to the L6; in all such cases appropriate indication will have been entered into the Status registers and if the Terminate interrupt level is not Zero, a Terminate interrupt will have been sent to the L6. Events include the following:

1. Normal completion of a list porcessing operation
2. Abort of a list processing operation due to hardware or software fault in DCW execution
3. Execution of an Interrupt L6 DCW (OC=39) or an Interrupt L6 PCW (OC=71)
4. Issuance of a STOP I/O command by L6 (subsection 3.6.2.8) while list processing is under way
5. Hardware or software fault in execution of an order received from the L66
6. Hardware or software fault in execution of an IO order received from the L6.

The last two types of events may occur while the coupler is concurrently processing a list or may occur when no list processing is being performed. In the former case, the occurrence will cause list processing to be stopped (prematurely terminated) and the Attention bit in status will be set ON (in addition to other bits in status describing the event) to indicate that this was done.

When the coupler is in the Status Pending state, it will not commence execution of any order from L66, whether previously pending or subsequently issued, except Bootload. It will not commence execution of any IO orders from L6 addressed to channel 2 or 3 whether previously pending or subsequently issued. Also, it will not begin execution of any DCWs since, as described above, the event causing entry to the Status Pending state will also have caused termination or abort of any list processing which was being done.

When in Status Pending state, the coupler will accept and execute IO orders from L6 addressed to channel 0 or 1; this allows the L6 program to retrieve the contents of Status registers 1 and 2. When both Status registers have been read (and therefore cleared) by the L6 program, the coupler leaves the Status Pending state and proceeds to execute any pending orders from L66 or L6 and then to accept and execute new orders from L66 or L6.

The Status Pending functionality is thus a means of insuring that each event is separately and distinctly reported to software.

Level 6 software should always read both Status registers (#1 first) after receiving a Termination interrupt.

## 3.6 COMMAND FUNCTIONALITY

### 3.6.1 L66 PCWs

#### 3.6.1.1 Interrupt L6 ($OC=71_8$)

The coupler fetches the interrupt cell field from the PCW and places it in its Status Register 2. It then sends an interrupt to L6 using the L6 Special Interrupt Level specified in its Configuration Register A and enters Status Pending state and stops list processing, if list processing was being performed.

#### 3.6.1.2 Bootload L6 ($OC=72_8$)

This op code is legal only if the Bootload Inhibit (BT INH) bit in the coupler's Task Register is ZERO.

When Bootload is legal, the coupler will initialize itself and then set the Stored Boot bit. It obtains the L6 address and Tally from the Transfer Control Word pointed to by the L66 mailbox word and stores these internally; it also stores internally, as the L66 address for the Bootload, the address plus one of the above Transfer Control Word.

The coupler then pulls the Power On line, BSPWON, of the L6 bus to a False state for 10 milliseconds and then allows it to return to a True state again. This causes the L6 CPU to perform a power fail interrupt and then a normal power-up sequence including an Initialize (Master Clear); the coupler will not reset Stored Boot on this Initialize. The coupler then awaits receipt of an Input Stored Boot IOLD (FC=09) order

from L6 to complete the overall bootload function (see subsection 3.8 for a description of bootload). If some order calling for transfer of some sort between L6 and L66 is received before the Input Stored Boot order, the Stored Boot bit will be cleared and that order performed as it normally would be.

The Bootload transfer is accomplished in ASCII mode.

3.6.1.3 Interrupt L66 ($OC=73_8$)

This op code causes the coupler to set one interrupt cell in the low order L66 system controller. Bits 27-29 of the interrupt cell field of the L66 mailbox word determine which interrupt cell is to be set.

If the interrupt cell specified in the L66 mailbox word is not implemented in the L66 system controller, there will be no direct indication of this fact to the FEP program.

3.6.1.4 Test Data Transfer from L6 to L66 ($OC=75_8$)

This op code is legal only if the CS BAR bit in the coupler's Configuration register is OFF.

When this op code is legal, the coupler will use the L66 mailbox word to obtain a 36 bit word from L66 memory which contains an FEP Address field and a Tally field. The area in L66 memory which will be used to receive data lies in locations immediately following this 36 bit word. The Tally specifies the number of 36 bit words to be transferred. The coupler will transfer data from the FEP memory, beginning at the specified FEP Address, to the L66 memory until the Tally becomes zero. If the Tally is initially zero, 4096 words are transferred. The transfer is accomplished in ASCII mode.

When the transfer is complete, the coupler will interrupt the Central System using the interrupt cell specified in its Task Register for L66 Test/Termination interrupts.

3.6.1.5 Test Data Transfer from L66 to L6 ($OC=76_8$)

This op code is legal only if the CS BAR bit in the coupler's Configuration register is OFF.

This operation is the same as that described above (op code $75_8$) except that the direction of data transfer is from the L66 to the FEP.

3.6.2 L6 IO Orders

3.6.2.1 Interrupt Control (FC=02/03 addressed to channel 0/1)

Function Code 03 loads a 16 bit word into the coupler's interrupt control register; Function Code 02 reads the contents of this register. This register defines the CPU channel number

to which the coupler is to send all interrupts on the L6 side; it also defines the interrupt level to be used for terminations. The format of this register is given in section IV.

Whenever an interrupt is sent to the L6, the CPU channel number is sent on the address bus and the interrupt level is sent on the data bus. For interrupts other than termination (e.g., Interrupt L6) the level is obtained from Configuration Register A. Consistent with NML standards, an interrupt level of all Zeros inhibits that interrupt from being sent to the CPU.

3.6.2.2 Task Register (FC=06/07 addressed to channel 0/1)

Function Code 06 reads the contents of the coupler's Task Word register; Function Code 07 loads this register. This register contains Rate Throttle and Bootload Inhibit control bits and cell numbers for L66 Test/Termination Interrupts and L66 Special Interrupts. Format of the register is given in Section IV.

3.6.2.3 Interrupt L66 (FC=X3/XB addressed to channel 2/3)

This order causes the coupler to set an interrupt cell in the L66. The cell number to be used is contained in bits 13-15 of the word delivered to the coupler by this order. All other bits of the word must be zeros.

3.6.2.4 Read DCW Offset Register (FC=0C addressed to channel 0/1)

This order causes the coupler to read the contents of its DCW Offset Register. Format is shown in Section IV.

3.6.2.5 Configuration Register A (FC=10/11 addressed to channel 0/1)

Function Code 11 addressed to channel 1 loads a 16 bit word into the coupler's Configuration Register A; Function Code 10 addressed to either channel reads the contents of this register. Function code 11 addressed to channel 0 is treated as a No Operation.

This register contains the CS BAR and FEP BAR bits which control portions of coupler checking functions related to security. It also contains fields for defining the level to be used on an Interrupt L6 operation. Test mode control bits are also contained here (see Section VII for usage).

Format of the register is given in Section IV. Consistent with NML standards, an interrupt level of all Zeros inhibits that interrupt from being sent to the CPU.

3.6.2.6 Read Status Register 1/2 (FC=18/1A addressed to channel 0/1)

Function Codes 18 or 1A read the contents of Status Register 1 or Status Register 2 respectively. The format of these registers

is given in Section IV.

All status bits in a status register, other than those forced, are cleared to Zero when that register is read.

3.6.2.7 Read Device ID (FC=01 addressed to channel 0/1)

Function Code 26 reads the coupler's Device ID number which is $(2408)_{16}$.

3.6.2.8 Output Control (FC=01 addressed to channel 0/1)

Function Code 01 delivers an output control word to the coupler. This order is accepted at any time. Bit 0 of the output control word when a ONE causes the coupler to initialize itself and perform its QLT. Bit 1 of the word is the STOP I/O bit. When this bit is a ONE and the coupler is processing a list, it causes the coupler to stop list processing and send a termination interrupt to L6; Attention status will be set but with no fault indicated. If a STOP I/O is issued as list processing is about to stop for some other reason, a termination interrupt is sent and status is set to reflect that other reason and no separate interrupt and status indication is given to reflect the STOP I/O. If a STOP I/O is issued when no list processing is being performed, no interrupt occurs and no indication is given in status. Remaining bits are RFU.

3.6.3 L6 IOLD Orders

3.6.3.1 DCW List (FC=09 addressed to channel 1)

Function Code 09 addressed to the coupler channel 1 will initiate list processing by the coupler, if it is not already busy. The address and range given by this order are loaded into the DCW List registers and the DCW Offset register is set to Zero. The DCW Offset is added to the DCW List Starting Address and the DCW is fetched from the resulting address. The DCW Offset register is incremented during list processing DCW fetching or is loaded from a Jump DCW. If the DCW Offset exceeds the value given in the DCW List Range or if the DCW List Range is Zero, list processing will be aborted and Control Word Exhaust status will be set. Further details on sequencing during list processing and a listing of legal DCWs have been given in subsection 3.5.

3.6.3.2 Load Barricade Register (FC=0B addressed to channel 0)

Function Code 0B must be addressed to the coupler's input channel 0. It loads the coupler's barricade register set with an address and a range. A range of zero is treated as specifying zero bytes and will cause termination and Barricade Violation in status. These registers are used in connection with enforcement of security restraints on data transfer operations on L6 memory. Details are given in subsection 3.8.

3.6.3.3 Input Stored Boot (FC=09 addressed to channel 0)

Function Code $(09)_{16}$ addressed to coupler channel 0 causes the coupler to complete any previously commanded Boot load (OC 72).

If the coupler's Stored Boot bit has not been set by a prior Bootload L6 command (OC=72) from L66, the coupler will treat this order as a No-op. If the Stored Boot bit has been set, the coupler will proceed to complete the bootload transfer as specified in the Bootload L6 command. The coupler ignores the address and range values given with the Input Stored Boot order. During the interval while the coupler is performing the bootload transfer, it is busy to any other L6 order sent to it (i.e., it will NAK) except Interrupt L66 or Output Control. When the transfer is complete, the Stored Boot bit is cleared and the coupler will accept any order.

The bootload transfer is accomplished in ASCII mode.

### 3.6.4 DCW Commands

#### 3.6.4.1 Disconnect (OC=30)

This op code causes the coupler to stop processing the DCW list of which this DCW is a part and to become available to accept a new list processing order from this processor, when and if issued.

Status is retained internally for retrieval by software via the Read Status Register IO orders (FC=18/1A).

#### 3.6.4.2 Disconnect & Interrupt (OC=38)

The coupler ceases processing the list and handles status as described in subsection 3.6.4.1 for the Disconnect DCW. The coupler then sends a Terminate interrupt to L6 using the interrupt level given in the coupler's Interrupt Control Register.

#### 3.6.4.3 Store Configuration Status (OC=3C)

This op code causes the coupler to store in memory L66 configuration information, specifically, the L66 Mailbox Address.

Two 16 bit words containing the information are stored in L6 memory. Formats of the stored information are given in Section IV. If the FEP BAR bit is ON, this op code is legal for L6 only if the DCW list IOLD was preceded by a Load Barricade IOLD.

#### 3.6.4.4 Data Transfer from L6 to L66 (OC=3D)

This op code causes the coupler to move one block of data from the L6 memory to the L66 memory, using the transfer mode specified in the DCW. Starting addresses for both memories are given in the DCW; for Binary and BCD transfer modes these are interpreted as word-bound addresses, while for ASCII and for transliteration modes they are interpreted as byte addresses. The length of transfer is given by a Tally in the DCW; for Binary and BCD transfer modes this length is defined in L66 36 bit words, while for ASCII and for transliteration modes, it is defined in bytes. An initial Tally of zeros is treated as one greater than a Tally of all ones

(i.e., 65K bytes/words). The operation ends when the transfer has been completed but may be aborted without completion of the transfer if a parity error is detected in the data or a violation of protection occurs. If the FEP BAR bit is ON, this op code is legal for L6 only if the DCW List IOLD was preceded by a Load Barricade IOLD.

3.6.4.5 Data Transfer from L66 to L6 (OC=3E)

This op code causes an operation similar to that described for op code 3D in section 3.6.4.4 with the only difference being that the direction of data transfer is from L66 memory to L6 memory. If the FEP BAR bit is ON, this op code is legal for L6 only if the DCW List IOLD was preceded by a Load Barricade IOLD.

3.6.4.6 Read and Clear L66; OR to Store L6 (OC=35)

This op code may be used by the L6 software to access words in L66 store which are subject to change by either the L66 or L6, such as "gate" words, and prevents possible loss of control information due to race conditions.

This op code causes one block of data to be transferred from the L66 to the L6. Each word read from the L66 store is accessed using a read-and-clear single precision cycle. The data is then ORed into the appropriate store location in the L6 using the read & lock and write & unlock bus cycles. The L66 starting address and tally are specified in the DCW. The L6 starting address is specified in the DCW. The transfer mode is binary. If the FEP BAR bit is ON this op code is legal only if the DCW List IOLD was preceded by a Load Barricade IOLD.

3.6.4.7 Interrupt L6 (OC=39)

This op code causes the coupler to stop list processing, enter Status Pending state and interrupt the L6 using the L6 Special Interrupt Level defined in the coupler's Configuration Register A. The coupler will also place a 6 bit interrupt cell value, given in the DCW, in the coupler's Status Register 2. The final effect is the same as for a L66 issued PCW op code $71_8$ (see subsection 3.6.1.1).

3.6.4.8 Jump (OC=3A)

This op code causes the coupler to load the 15 bit word offset address given in the DCW into the DCW Offset register. The next DCW is then fetched for execution from the location indicated by the sum of the DCW offset and the DCW List Starting Address. If the DCW offset value exceeds the value given in the DCW List Range, list processing will be aborted and the Control Word Exhaust status will be set.

3.6.4.9 No Operation (OC=33)

This op code causes no operation to be performed. The coupler proceeds to the next DCW in the list. The other fields in this DCW are not inspected or interpreted by the coupler. This DCW is used as an aid to dynamic modification of DCWs.

3.6.4.10 Stall (OC=34)

This op code causes no operation to be performed. The coupler does not proceed to the next DCW in the list but proceeds to re-fetch this DCW. The other fields in this DCW are not inspected or interpreted by the coupler. This DCW is used as an aid to dynamic modification of DCWs.

3.6.4.11 Interrupt L66 (OC=3B)

This op code causes the coupler to set one interrupt cell in the low order L66 system controller. 3 bits in the DCW determine which of 8 cells is set. This operation is essentially the same as the Interrupt L66 described in section 3.6.2.3 except that the instruction is contained in a DCW processed as part of a list instead of being contained in an IO order.

## 3.7 BARRICADE AND MEMORY MAPPING FUNCTIONS

### 3.7.1 Level 6 Interface

A definition of addressing terminology, as applied to memory addresses seen by the coupler is in order here:

1. A Physical address is the memory address used by a device, such as the coupler, on memory accesses and which results in a particular memory physical location being directly accessed.

2. A Mapped address is a memory address used by a device, such as the coupler, on memory accesses but which is actually intercepted by the Security Protection Module and converted to a physical address and the access then performed; the interception and conversion is transparent to the device. The only visible difference between a Physical address and a Mapped address on the bus is that the highest order bit (bit 0) on the address bus is a ONE for a Mapped address and a ZERO for a physical address.

3. A Virtual address is an address given in an I/O order which requires conversion to a Physical/Mapped/Real address before use. This address is the address as seen by the user program in a system having memory management.

4. A Real address is an address given to the coupler which does not require conversion to a physical address by the coupler; such conversion, if required, has already been done in the CPU or by the SPM. In a system without memory management in effect, all addresses seen by the user program are Real.

There are four levels of memory management/protection system on the L6 side with which the coupler must be able to operate:

1. A configuration having no memory management functionality or a disabled memory management functionality; in this sytem all addressing has a one-to-one relationship between program-visible and physical addresses and there is no memory protection. When used in such a system, the coupler's FEP BAR bit is left in a reset (OFF) condition and the Barricade registers are not loaded or used. All of the addresses given to the coupler by L6 in IOLD orders, and DCWs are Real. The CS Bar bit is left in the OFF condition.

2. A configuration using the commercial memory management option of the 6/40 series (see reference document) primarily for memory management and without particularly stringent security requirements. In this system the user program creates virtual addresses in IOLD orders and in DCWs since all the addresses it generates are virtual. All IOLD orders are trapped by the CPU for handling by a privileged program, the Monitor. The Monitor validates the memory areas defined in IOLD orders and the CPU hardware converts these addresses to Real addresses when the order is executed by the Monitor. The Barricade functionality of the coupler is used to relieve the Monitor of the necessity of scanning, validating and converting the DCWs in the list. The FEP BAR bit must be ON and the Barricade registers must be loaded and used. The CS BAR bit may be left OFF.

   The imposition of the FEP barricade function tends to restrict the data transfers which can be issued in a single DCW list since a DCW can effectively only specify a starting offset, in its L6 address field, while the Load Barricade IOLD specifies a base address for all input and output performed by a given DCW list. There are no restrictions on mixing of input and output DCWs in the same DCW list.

A base virtual address is specified for the data transfers of a given DCW list in the Load Barricade IOLD which is intercepted by the Monitor. The Monitor validates and the CPU converts the address in the Load Barricade IOLD to a Real base address which is sent to the coupler's Barricade registers.

The Monitor also intercepts and validates the memory area and the CPU converts the address given in the DCW List IOLD to a Real address which is sent to the coupler's DCW Address Register. The DCWs in the list are never seen by the Monitor and CPU hardware. When the coupler starts execution of a data transfer DCW, it adds the low order sixteen bits of the L6 address field in the DCW to the base in the Barricade placing the result in the Bus Address Register which now contains a full physical address with which it can address memory. As each word is accessed in L6 memory, the Bus Address Register is incremented. The Barricade Range register is checked. The DCW list will be aborted if the Barricade Range is exceeded; the value of the range is the maximum extent of input or output L6 bytes which can be transferred under control of the current list. After the DCW list is completed or stopped for any reason, the Barricade registers are marked invalid by the coupler. Figure 3-6 shows conceptually how these addresses are handled (note that the functionality ascribed to "SPM" is, in this system, provided by a combination of Monitor software and CPU hardware).

3. A Full Secure Communications processor application. In this system both the processor and its software differ from a commercial system. There is a Security Protection Module (SPM) attached to the bus which intercepts memory accesses and I/O orders and validates them. I/O orders are not trapped to a software monitor but are intercepted and validated by the SPM on the bus before being passed on to the I/O unit. In the SPM considered here, there is no ability to dynamically absolutize and validate I/O DMA operations so that an I/O operation initiated by an IOLD must involve only a single area of memory which is both virtually and physically contiguous. The Barricade functionality of the coupler is used to support the SPM by relieving it of the necessity of scanning the DCW's in a list; instead, the SPM validates the Barricade and the coupler then enforces the Barricade upon operations performed by the list. Note that the SPM will also intercept and validate IO orders to the coupler (e.g., those

which set up configuration, etc.,) but since this function is entirely invisible to the coupler and does not affect its functionality, no further mention will be made of this fact. In this system both the CS BAR and FEP BAR bits must be ON.

Figure 3-6 shows conceptually how addresses are handled. From the coupler's viewpoint, there are many similarities with the preceding system.

4. A configuration using a Full Secure Security Protection Module (SPM) with dynamic I/O mapping ability (see reference document). The CS BAR and FEP BAR will both be ON as in the previous system.

   The primary difference from the preceding system is that the SPM has the ability to dynamically convert memory addresses as I/O devices perform their DMA accesses with memory; this permits I/O operations to cross page boundaries with ease (generally these virtual pages are not physically contiguous in memory). The sequence of operations is similar to the preceding system except that the SPM converts the address in the Load Barricade IOLD to a mapped address which contains a page number and operation number; the highest order bit of this address is a ONE. The coupler handles this address the same as in the preceding system; when it performs an access to L6 memory, the access request is intercepted on the bus by the SPM because of the high order bit value. The SPM then uses the operation number in this mapped address to identify the original issuer program and thus the correct map to use, and completes the actual physical memory access for the coupler. Figure 3-7 shows conceptually how the addresses are handled.

### 3.7.2 L66 Interface

Depending upon the model of IOM and its possible modes, there are three addressing mode possibilities on the Direct Channel interface to the L66: Real/Mapped/Extended. Only the Real and Mapped modes are of current interest to the coupler.

In Real mode, the 24 bit address furnished by the coupler is used directly as a physical address to access a memory location. All L66 addresses furnished the coupler, whether in switch settings or in PCW address fields, are Real and are not converted by either the coupler or the IOM.

In Mapped mode, the address furnished by the coupler to the IOM is interpreted as an offset and a page number by the

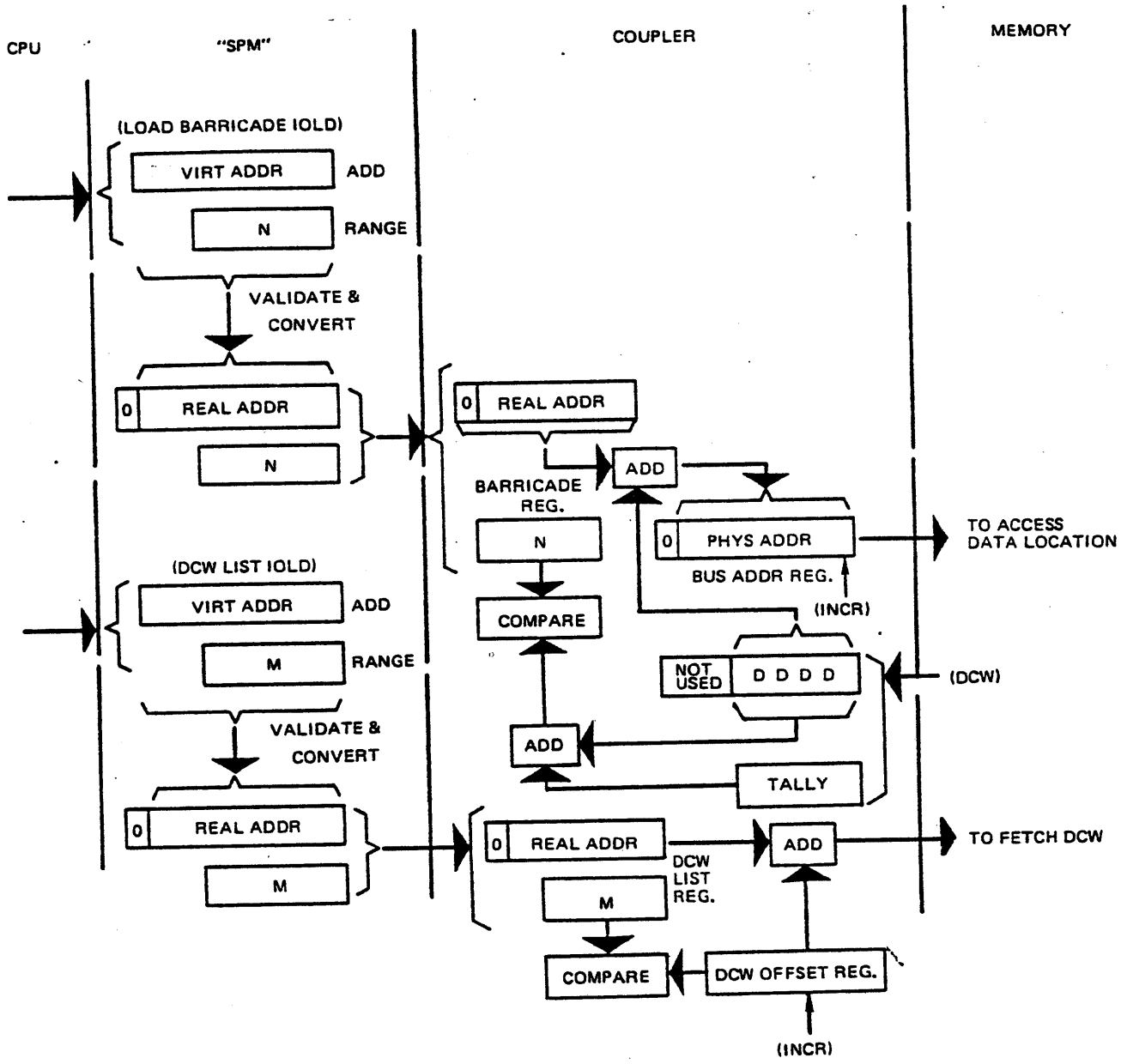



Figure 3-6 Real Address Conversions Under Barricade

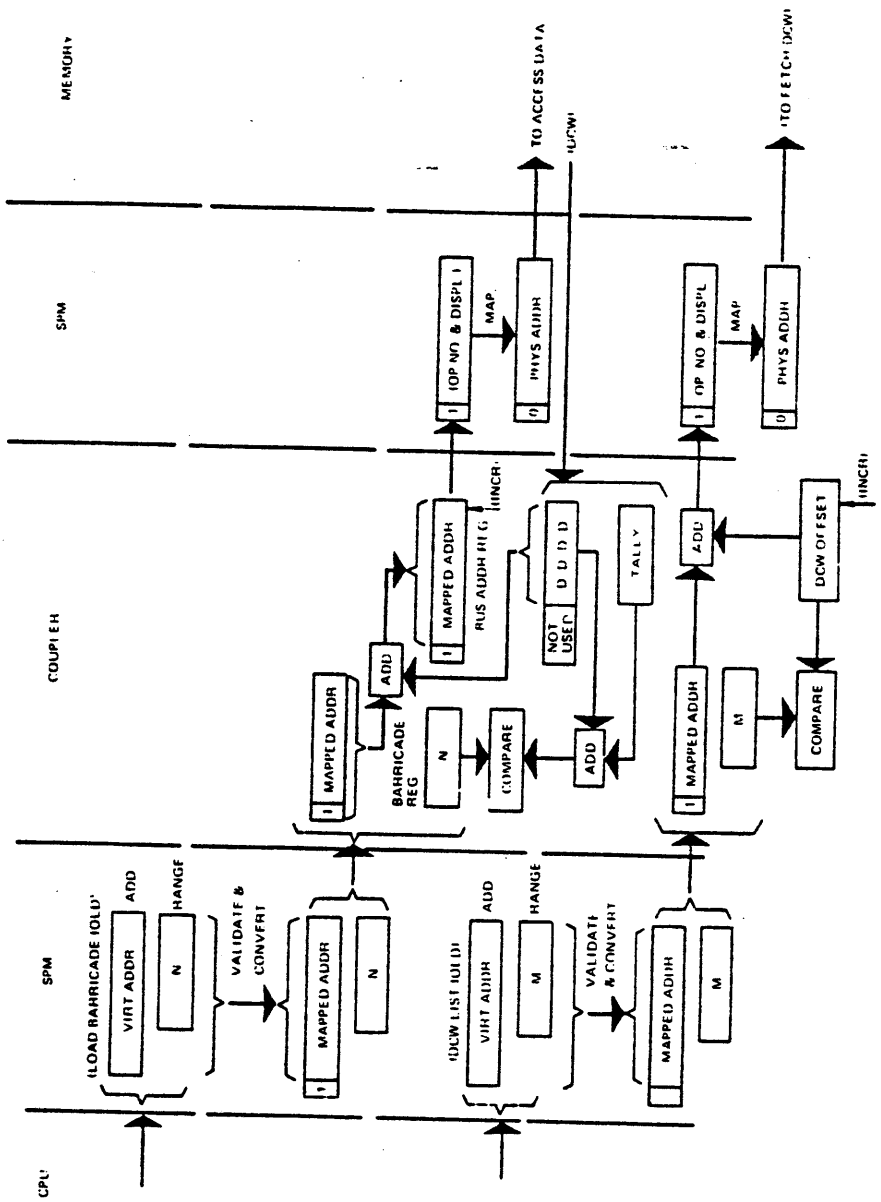



Figure 3-7 Mapped Address Conversions Under Barricade

IOM. All addresses furnished the coupler, whether in switch settings or in PCW address fields, are Mapped and are not converted by the coupler.

Thus the coupler is not aware of the addressing mode being used in the L66 and simply uses the addresses furnished it to access the L66 memory.

A switch on the L66 IOM selects the operating mode of the IOM; the second word of the CIOC defines the page table used by the IOM. When mapped mode is used, the L66 mailbox accesses are also mapped; the general approach used in this case is to assign page 0 for mailbox use with other pages used for data buffers. In this case the L66 Mailbox Address switches should be set up so as to specify page 0.

## 3.8 BOOTLOAD OF L6 BY L66

This section discusses the requirements and sequence of steps to perform a Bootload of L6 from the L66 Host system.

The L6 processor (CPU #0) must be configured to perform an automatic power-up bootload.

The coupler contains two bits associated with its bootload functionality: "Boot Inhibit" and "Stored Boot". Both of these bits are initialized to OFF state; Boot Inhibit may be set ON or OFF under L6 software control.

When the L66 program issues a Bootload order to the coupler, the coupler (if Boot Inhibit is OFF) loads the given addresses and Tally into its registers, initializes itself and sets its Stored Boot bit ON. It then pulls the L6 bus line BSPWON to False state for 10 milliseconds and then allows it to return to True State.

The L6 processor, as a result of these actions by the BSPWON line, performs a Power Fail interrupt and then performs an automatic power-up sequence, including Master Clear, QLT, memory test, and an automatic bootload. The coupler, being aware that the Master Clear is occuring as a result of its own actions, does not clear its Stored Boot bit (normally it would).

The L6 processor will at some point issue an Input Stored Boot IOLD order to the coupler. Note that prior to issuing this order the L6 CPU can access other registers in the coupler without ill effect such as Status Register 1/2, Device ID, Interrupt Control, Task Register; but that receipt of any order by the coupler which involves a transfer between processors will cause clearing of the Stored Boot.

The receipt of the Input Stored Boot order causes the coupler, if the Stored Boot bit is ONE, to input data into L6 memory as specified by the L66 Bootload order. On completion of this the Stored Boot bit is cleared.

If there is more than one coupler through which a Boot might arrive, the program should first inspect the Stored Boot bits returned by Read Status Register 2 orders.

The L66 program which issues the Bootload order normally expects a return of status from the FEP as a result of the bootload. According to the GRTS manual, if the bootload does not proceed to completion for any reason and therefore the status return does not occur, the L66 program will, after a time-out interval, type out a "No Response to Boot" message on the L66 console.

The L6 automatic bootload which supports bootload from L66 can be accomplished either by the CPU's Bootload PROM, through Main Memory PROM, or through a diskette (or other bootload device). In any case the panel must be locked and the Volatile Memory jumper in the CPU must be set so that an automatic bootload operation will occur (note that the memory need not actually be volatile).

The CPU Bootload PROM will probably be the method of choice when the L6 is to function solely as a Front End and is always loaded through one particular coupler. In this case the coupler will be connected to channel 400. The PROM program, having obtained the coupler ID in response to its query to that channel, follows the same sequence of operations as for a card reader. This sequence consists of a Load Configuration Register A (FC=11)IO, an IOLD (FC=09), and a Read Status Reg 1 (FC=18), all addressed to channel 400. The coupler will stall the CPU by means of NAK responses until the load is completed. The PROM program tests that Device Ready is a ONE and then logically ANDs the status from Status Register 1 with the constant $(3F97)_{16}$ and if this result is $(0000)_{16}$ transfers control to memory location $(0100)_{16}$; otherwise the PROM program repeats itself.

The diskette device, if present on the L6 for other reasons, can be used to support a bootload by L66. In this case, when the L6 is to be loaded from L66, the disk mounted on the diskette device will contain an L66 bootload support program which will cause an Input Stored Boot IOLD order to be issued to the coupler. The diskette is connected as channel 400 and is booted first into location $(0100)_{16}$ and then the L66 load writes over it. When the L6 is to be operated as an independent system, a different disk should be mounted and L6 software should set the coupler's Boot Inhibit bit so that any attempted Boots from L66 will not disturb the L6.

If Main Memory PROM is provided, the program contained in it should test one of its option switches to determine whether L66 bootload or standalone operation is desired; for L66 bootload operation the PROM program issues the Input Stored Boot IOLD order to the coupler, otherwise it sets the Bootload Inhibit of any couplers and proceeds with its load of the system.

In all cases, the L66 Bootload command specifies the L6 memory locations into which the load from L66 is to occur and the extent of the load; location $(0100)_{16}$ in L6 would always be the first location to be executed by L6 after the load from L66 assuming that the L66 bootload is independent of the mechanization used in L6.

## 3.9 INITIALIZATION

The coupler is initialized by receipt of an Output Control IO order with its Initialize bit (bit 0 of the data word) a ONE, or by receipt of a Master Clear signal from the L6 bus, providing that the coupler itself is not causing the Master Clear to occur as part of a bootload (see section 3.8). Initialization causes the coupler to perfrom its internal QLT and enter the state listed below.

- Not Busy
- Barricade Register invalidated
- Status Registers 1 & 2 cleared to ZEROs
- Interrupt Control Register cleared to ZEROs
- Register control/state bits cleared to ZEROs

  TH
  BT INH
  CS BAR
  FEP BAR
  TEST
  STORED BOOT

- Operational state (OPL set to ONE)

# IV INTERFACE REQUIREMENTS

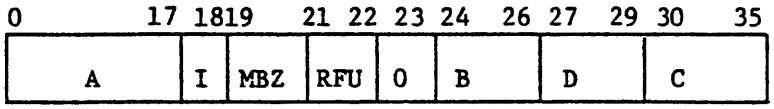
## 4.1 SOFTWARE INTERFACE

Communication between L6 and L66 is controlled via mailbox region(s) in processor memory. Part of a mailbox region is used for overall control and the remainder is for individual channel control. Mailbox communications are entirely a programmed function; thus, other than fetching the Direct Channel Mailbox word from the location specified as the L66 Mailbox, the coupler has no built-in knowledge of the format or extent of the region.

### 4.1.1 L66 Command Formats

The formats of the LPW and PCW for the IOM Connect Channel are shown in the IOM EPS-1, document number 43A219604.

#### 4.1.1.1 Direct Channel Mailbox Word




This word is found in the location in L66 memory known as the L66 Mailbox and given via configuration switches to the coupler. The interpretation of these fields by the coupler is dependent upon the operation specified in the Op code field as shown in the following table.

If the coupler accepts the Op Code as legal, it will store a word of all Zeros in the Mailbox location after completion of the operation; if the Op Code is not legal, it will invert the value of bit 18 (the I field above). The L66 program should not attempt to put a new PCW in the L66 mailbox until it has seen one or the other indication with respect to a previously issued PCW.

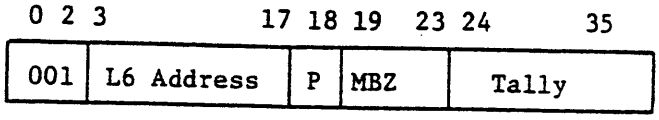
| Operation | C 30-35 | A 0-17 | B 24-26 | D 27-29 | 18 I |
|---|---|---|---|---|---|
| Interrupt L6 | $(71)_8$ | # | Interrupt | Level LLLLLL | * |
| Bootload L6 | $(72)_8$ | L66 Address A6-A23 | L66 Address A0-A2 | L66 Address A3-A5 | * |
| | | Transfer Control Word | | | |
| Interrupt L66 | $(73)_8$ | # | # | Interrupt Cell CCC | * |
| Test Data Xfer L6 to L66 | $(75)_8$ | L66 Address A6-A23 | L66 Address A0-A2 | L66 Address A3-A5 | * |
| | | Transfer Control Word | | | |
| Test Data Xfer L66 to L6 | $(76)_8$ | L66 Address A6-A23 | L66 Address A0-A2 | L66 Address A3-A5 | * |
| | | Transfer Control Word | | | |

# = Not inspected or interpreted by the coupler.

* = Normally will be zero by software convention. If the Op Code in the C field is illegal (see subsections 3.5.1 and 3.5.2), this bit will be inverted (complemented) by the coupler.

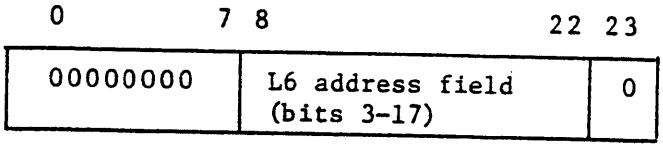
4.1.1.2 Transfer Control Word

The transfer control word, which is pointed to by the mailbox word in L66 memory on Op Codes 72, 75, 76 contains a starting address which applies to L6 memory and a Tally of the number of 36 bit words to be transferred. The L66 memory locations to/from which the transfers occur are those immediately following the location where this word was obtained.

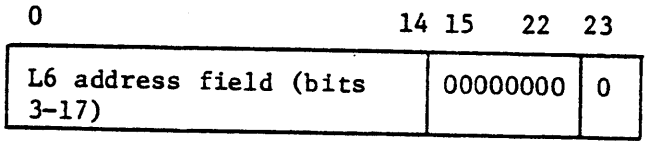



The L6 address field is interpreted as an effective L6 byte address as follows:

if P = 0



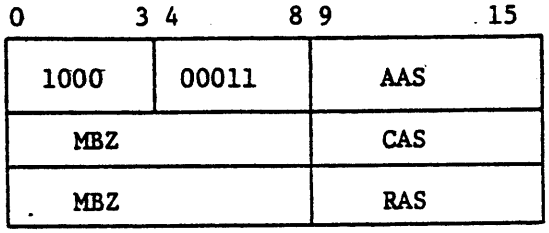

if P = 1



## 4.1.2 L6 Command Formats

### 4.1.2.1 DCW List IOLD

Although any legal format may be used, only the non-procedural form of the IOLD order is shown below. It occupies three consecutive words in FEP memory.

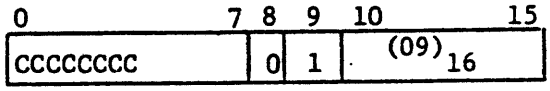



AAS is an address syllable which points to the start of the DCW list which is to be executed.

CAS is an address syllable which points to a control word which defines the channel and function as shown below.

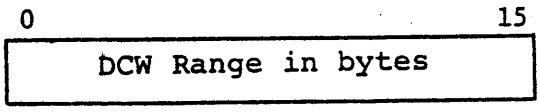
RAS is an address syllable which points to a DCW range word which defines the range of the DCW list, as shown below.

#### 4.1.2.1.1 DCW List Control Word




CCCCCCCC is the high order eight bits of the coupler's channel number as set on its configuration switches.

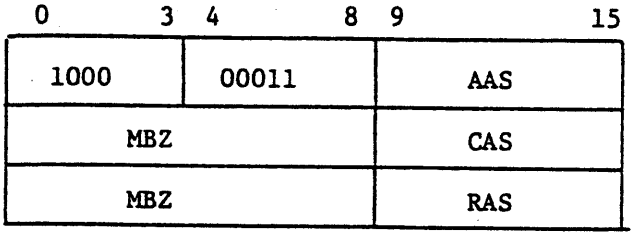
#### 4.1.2.1.2 DCW Range Word




The DCW Range allows for a DCW list up to $2^{16}-1$ bytes in extent. The DCW list is in ascending memory locations.

4.1.2.2 Load Barricade Register IOLD

Although any legal format may be used, only the non-procedural form of the IOLD order is shown below. It occupies three consecutive words in FEP memory.

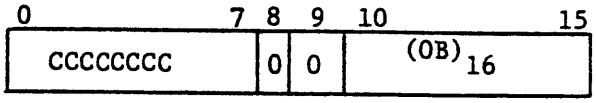



AAS is an address syllable which points to a memory location which must be a modulo 256 word address. The high order 16 bits of this address is stored in one of the Barricade registers as a starting value.

CAS is an address syllable which points to a control word which defines the channel and function as shown below.

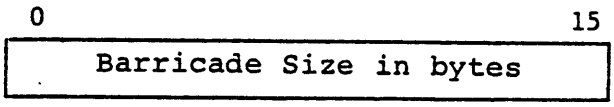
RAS is an address syllable which points to a Barricade size word which is stored in one of the Barricade registers as a size value.

4.1.2.2.1 Load Barricade Control Word




CCCCCCCC is the high order eight bits of the coupler's channel number as set on its configuration switches.

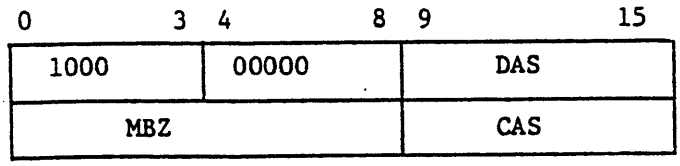
4.1.2.2.2 Barricade Size Word




The Barricade size allows for a data area up to $2^{16}$-1 bytes in extent. This area is in ascending memory locations with respect to the barricade initial value.

4.1.2.3 IO Order Formats

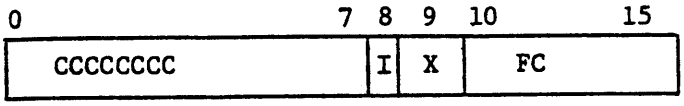
Although any legal format may be used, only the non-procedural form of the IO order is shown below. It occupies two consecutive words in FEP memory.




DAS is an address syllable which points to the location from or to which a word of information is obtained or delivered by the coupler. The various forms of information thus transferred consist of configuration and status. These forms are shown in sections 4.1.3 and 4.1.4

CAS is an address syllable which points to a control word which defines the channel and function as shown below.

4.1.2.3.1 IO Control Word




CCCCCCCC is the high order eight bits of the coupler's channel number as set on its configuration switches.

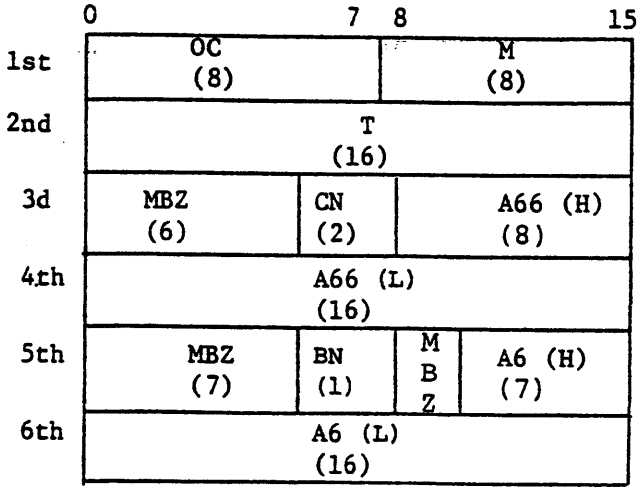
X is a "don't care" bit (lowest order channel number bit)

FC is the function code which defines the direction of transfer and the destination/source within the coupler. All defined function codes are given in section 3.6.2.

I is a bit which is a ONE for interrupt orders and ZERO for all other IO orders (see subsection 3.5.2).

4.1.2.4 Direct Control Word (DCW)

Each DCW occupies six consecutive words in L6 memory as shown below.

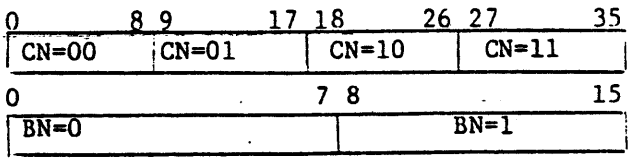



The interpretation of these fields by the coupler is dependent on the operation specified in the Op Code field as shown in the following table.

| Operation | OC | M | T | A6 | CN | A66 | BN |
|---|---|---|---|---|---|---|---|
| Disconnect | 30 | # | # | # | # | # | # |
| Disc, & Intpt | 38 | # | # | # | # | # | # |
| Store Config. Status | 3C | # | # | L6 Address A0-A22 | # | # | # |
| Data Transfer L6 to L66 | 3D | Transfer Mode * | Tally | L6 Address A0-A22 | Char No | L66 Addr A0-A23 | (A23) Byte No. |
| Data Transfer L66 to L6 | 3E | Transfer Mode * | Tally | L6 Address A0-A22 | Char No | L66 Addr A0-A23 | (A23) Byte No. |
| Interrupt L6 | 39 | (00LLLLLL) | # | # | # | # | # |
| Jump | 3A | # | # | A0-A7MBZ<br>A8-A22 Offset Addr | # | # | # |
| Interrupt L66 | 3B | Intpt Cell (00000CCC) | # | # | # | # | # |
| Read & Clear OR to Store | 35 | # | Tally | L6 Address A0-A22 | Char No | L66 Addr A0-A23 | (A23) Byte No. |
| No Operation | 33 | # | # | # | # | # | # |
| Stall | 34 | # | # | # | # | # | # |

\# = Not inspected or interpreted by the coupler
* = Transfer Mode
$(01)_{16}$ = ASCII mode
$(02)_{16}$ = BCD
$(03)_{16}$ = Binary
$(11)_{16}$ = Transliteration Mode A
$(21)_{16}$ = Transliteration Mode B

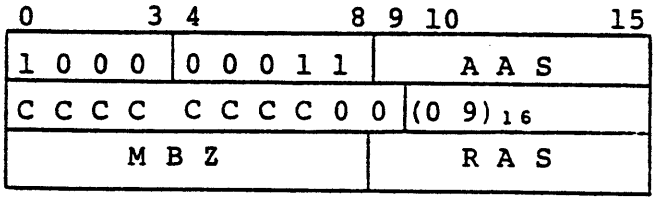
For Binary and BCD modes, Tally specifies the number of 36 bit words to transfer and CN and BN are ignored. For ASCII mode and for the Transliteration modes, Tally specifies the number of bytes to transfer and CN and BN specify positions in the L66 and L6 words as shown below.




The translation performed in the Transliteration modes is shown in Tables 4-1 and 4-2.

4.1.2.5 Input Stored Boot IOLD

The format of this order is shown below. It occupies three consecutive words in FEP memory.




AAS is an address syllable. The address indicated herein is ignored by the coupler.

CCCCCCCC is the high order eight bits of the coupler's channel number as set on its configuration switches.

RAS is an address syllable. The content of this location is ignored by the coupler.

Table 4-1 Transliteration Mode A
(ASCII to EBCDIC Translation)

| INPUT CHAR. | | MOST SIGNIFICANT DIGIT | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| LEAST SIGNIFICANT DIGIT | 0 | 00 | 10 | 40 | F0 | 7C | D7 | 79 | 97 | 00 | 10 | 40 | F0 | 7C | D7 | 79 | 97 |
| | 1 | 01 | 11 | 4F | F1 | C1 | D8 | 81 | 98 | 01 | 11 | 4F | F1 | C1 | D8 | 81 | 98 |
| | 2 | 02 | 12 | 7F | F2 | C2 | D9 | 82 | 99 | 02 | 12 | 7F | F2 | C2 | D9 | 82 | 99 |
| | 3 | 03 | 13 | 7B | F3 | C3 | E2 | 83 | A2 | 03 | 13 | 7B | F3 | C3 | E2 | 83 | A2 |
| | 4 | 37 | 3C | 5B | F4 | C4 | E3 | 84 | A3 | 37 | 3C | 5B | F4 | C4 | E3 | 84 | A3 |
| | 5 | 2D | 3D | 6C | F5 | C5 | E4 | 85 | A4 | 2D | 3D | 6C | F5 | C5 | E4 | 85 | 44 |
| | 6 | 2E | 32 | 50 | F6 | C6 | E5 | 86 | A5 | 2E | 32 | 50 | F6 | C6 | E5 | 86 | A5 |
| | 7 | 2F | 26 | 7D | F7 | C7 | E6 | 87 | A6 | 2F | 26 | 7D | F7 | C7 | E6 | 87 | A6 |
| | 8 | 16 | 18 | 4D | F8 | C8 | E7 | 88 | A7 | 16 | 18 | 4D | F8 | C8 | E7 | 88 | A7 |
| | 9 | 05 | 19 | 5D | F9 | C9 | E8 | 89 | A8 | 05 | 19 | 5D | F9 | C9 | E8 | 89 | A8 |
| | A | 25 | 3F | 5C | 7A | D1 | E9 | 91 | A9 | 25 | 3F | 5C | 7A | D1 | E9 | 91 | A9 |
| | B | 0B | 27 | 4E | 5E | D2 | 4A | 92 | C0 | 0B | 27 | 4E | 5E | D2 | 4A | 92 | C0 |
| | C | 0C | 1C | 6B | 4C | D3 | E0 | 93 | 6A | 0C | 1C | 6B | 4C | D3 | E0 | 93 | 6A |
| | D | 0D | 1D | 60 | 7E | D4 | 5A | 94 | D0 | 0D | 1D | 60 | 7E | D4 | 5A | 94 | D0 |
| | E | 0E | 1E | 4B | 6E | D5 | 5F | 95 | A1 | 0E | 1E | 4B | 6E | D5 | 5F | 95 | A1 |
| | F | 0F | 1F | 61 | 6F | D6 | 6D | 96 | 07 | 0F | 1F | 61 | 6F | D6 | 6D | 96 | 07 |

Table 4-2 Transliteration Mode B
(EBCDIC to ASCII Translation)

| INPUT CHAR. | | MOST SIGNIFICANT DIGIT | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| LEAST SIGNIFICANT DIGIT | 0 | 00 | 10 | 7F | 7F | 20 | 26 | 2D | 7F | 7F | 7F | 7F | 7F | 7B | 7D | 5C | 30 |
| | 1 | 01 | 11 | 7F | 7F | 7F | 7F | 2F | 7F | 61 | 6A | 7E | 7F | 41 | 4A | 7F | 31 |
| | 2 | 02 | 12 | 7F | 16 | 7F | 7F | 7F | 7F | 62 | 6B | 73 | 7F | 42 | 4B | 53 | 32 |
| | 3 | 03 | 13 | 7F | 7F | 7F | 7F | 7F | 7F | 63 | 6C | 74 | 7F | 43 | 4C | 54 | 33 |
| | 4 | 7F | 7F | 7F | 7F | 7F | 7F | 7F | 7F | 64 | 6D | 75 | 7F | 44 | 4D | 55 | 34 |
| | 5 | 09 | 7F | 0A | 7F | 7F | 7F | 7F | 7F | 65 | 6E | 76 | 7F | 45 | 4E | 56 | 35 |
| | 6 | 7F | 08 | 17 | 7F | 7F | 7F | 7F | 7F | 66 | 6F | 77 | 7F | 46 | 4F | 57 | 36 |
| | 7 | 7F | 7F | 1B | 04 | 7F | 7F | 7F | 7F | 67 | 70 | 78 | 7F | 47 | 50 | 58 | 37 |
| | 8 | 7F | 18 | 7F | 7F | 7F | 7F | 7F | 7F | 68 | 71 | 79 | 7F | 48 | 51 | 59 | 38 |
| | 9 | 7F | 19 | 7F | 7F | 7F | 7F | 7F | 60 | 69 | 72 | 7A | 7F | 49 | 52 | 5A | 39 |
| | A | 7F | 7F | 7F | 7F | 5B | 5D | 7C | 3A | 7F | 7F | 7F | 7F | 7F | 7F | 7F | 7F |
| | B | 0B | 7F | 7F | 7F | 2E | 24 | 2C | 23 | 7F | 7F | 7F | 7F | 7F | 7F | 7F | 7F |
| | C | 0C | 1C | 7F | 14 | 3C | 2A | 25 | 40 | 7F | 7F | 7F | 7F | 7F | 7F | 7F | 7F |
| | D | 0D | 1D | 05 | 15 | 28 | 29 | 5F | 27 | 7F | 7F | 7F | 7F | 7F | 7F | 7F | 7F |
| | E | 0E | 1E | 06 | 7F | 2B | 3B | 3E | 3D | 7F | 7F | 7F | 7F | 7F | 7F | 7F | 7F |
| | F | 0F | 1F | 07 | 1A | 21 | 5E | 3F | 22 | 7F | 7F | 7F | 7F | 7F | 7F | 7F | 7F |

### 4.1.3 Coupler Control & Configuration Register Formats

The following table shows the detailed format of Control and Configuration registers in the coupler which can be read or loaded by the L6 program by means of IO orders. These registers cannot be accessed from the L66.

In all cases where two Function Codes are given, the even numbered code reads the register contents to memory and the odd numbered code loads the register from memory.

| FC | Register | Acc | Contents |
|---|---|---|---|
| 02/03 | Interrupt Ctl | R/W | 0 … 9 10 … 15<br>CPU Channel No \| L6 Termination Intpt Level |
| 06/07 | Task Register | R/W | 0 1 2 4 5 7 8 … 15<br>TH \| BT INH \| L66 Test Term Intpt \| L66 Spec Intpt \| RFU |
| 0C | DCW Offset Reg | R | 0 … 15<br>DCW Offset in words |
| 10/11 | Config Reg A | R/W | 0 1 2 … 7 8 9 10 … 15<br>CS BAR \| FEP BAR \| RFU \| OPL \| TEST \| Special L6 Intpt Level |
| 26 | Device ID | R | 0 … 15<br>$(2408)_{16}$ |
| 01 | Output Control | W | 0 1 2 … 15<br>Initialize \| Stop I/O \| RFU |

### 4.1.4 Status and Configuration Status Formats

Coupler status may be retrieved on the L6 side by means of the IO order with function codes 18 or 1A for status registers 1 or 2 respectively (16 bits each).

- Status Register 1 Format

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DR | ATT | 0 | ESE | ESP | CNO | CSP | CSR | CSW | COP | TT | W2NZ | MY | NER | L6B | MR |

- Status Register 2 Format

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 ... 15 |
|---|---|---|---|---|---|---|---|---|---|---|
| BV | CWE | IFC | IDCW | IPCW | HF6 | HF66 | HFDCW | STBT | RFU | Interrupt L6 Cell No. (LLLLLL) |

DR = Device Ready. Set to ONE whenever the following combination of signal states exist on the Direct Channel Interface:

"DC-OPL" is true, AND

"DC-TEST" is not true, AND

"SYS-FLT" is not true.

0 = Always a Zero (Data Service Rate Error).

The remaining bits in these registers are cleared when the register is read.

ATT = Attention. Set to ONE whenever the coupler stops or aborts processing a list due to a fault.

BV = Barricade Violation. Set to ONE if FEP BAR is ON and a data transfer was attempted outside the area defined by a Barricade Register or Barricade register contents were invalid with attempted data transfer.

CWE = Control Word Exhaust. Set to ONE is the DCW Range register was initially set zero or if the DCW Offset exceeded the DCW Range.

CSP = Central System Parity. Set to ONE if the coupler detects a parity error in information received from L66.

L6B = Level 6 Bus. Set to ONE if the coupler detects a parity error in information received from L6.

MR = Memory Red. Set to ONE if L6 memory indicated an uncorrectable error in information sent to the coupler.

MY = Memory Yellow. Set to ONE if L6 memory indicated that it corrected an error in information sent to the coupler.

NER = NonExistent Resource. Set to ONE if a NAK response is received from the L6 bus to an attempted operation by the coupler.

RFU = Reserved for Future Use.

W2NZ = Word 2 Non Zero. Set to ONE if some bit(s) in status word 2 is ONE.

HF6 = Hardware Fault 6. Set to ONE if a hardware fault occurs during execution of an IO order issued by L6.

HF66 = Hardware Fault 66. Set to ONE if a hardware fault occurs during execution of an order issued by L66.

HFDCW = Hardware Fault on DCW. Set to ONE if a hardware fault occurs during execution of a DCW.

TT = Transaction Timer. Set to ONE if no response was received from L66 within 10 milliseconds or "DC-INIT" on the Direct Channel Interface is true.

CNO = Central Non-Operational. Set to ONE whenever Device Ready (DR) makes a transition from a true to false state.

ESE = External System Error. Set to ONE when "CMD-PAR-ERR" on the Direct Channel Interface is true.

ESP = External System Parity. Set to ONE when "DTA-PAR-ERR" on the Direct Channel Interface is true.

CSR = Central System Read. Set to ONE when "U-BUS-PAR-ERR" on the Direct Channel Interface is true.

CSW = Central System Write. Set to ONE when "IOM-PAR-ERR" on the Direct Channel Interface is true.

IFC = Illegal Function Code. Set to ONE if an illegal Function Code is used by L6.

IDCW = Illegal DCW Op Code. Set to ONE if an illegal DCW op code is encountered.

IPCW = Illegal PCW Op Code. Set to ONE if an illegal PCW op code is encountered.

COP = Central Operational. Set to ONE whenever Device Ready (DR) makes a transition from false to true state.

ST BT = Stored Boot. Set ONE by acceptance of a Bootload command from L66.

Interrupt L6 Cell Number. This contains the interrupt cell value (LLLLLL) given in the most recently executed Interrupt L6 command issued by either L6 or L66.

The bits which make up Status registers 1 and 2 may be considered to serve one of three purposes:

- General Information. These are DR, MY, ST BT, Interrupt Cell, CNO, COP, ATT.
- Fault Classification. These consist of software faults BV, CWE, IFC, IDCW, IPCW and the hardware fault indicators IIF6, IIF66, IIFDCW.
- Hardware Fault Detail. These are CSP, CSR, CSW, ESE, ESP, L6B, MR, NER, TT.

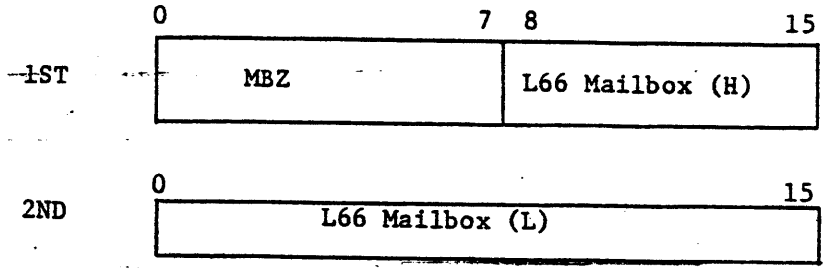
The state of these bits under some typical conditions is shown in the following table:

| FAULT CLASS | | | | | | | | GEN. INFO | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SOFTWARE | | | | | HARDWARE | | | | | | | | |
| BV | CWE | IFC | IDCW | IPCW | HF6 | HF66 | HFDCW | ATT | DR | CNO | COP | HARDWARE FAULT DETAIL | CONDITION |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Zero | Normal termination of list processing operation |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Zero | Illegal order issued by L6 (no list in process) |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | Zero | Stopped list processing due to illegal order issued by L66 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | Zero | Aborted list processing due to Barricade violation |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | Nonzero | Hardware fault in executing L6 order (no list in process) |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | Nonzero | Stopped list processing due to hardware fault in executing L66 order |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | Nonzero | Aborted list processing due to hardware fault in executing DCW |
| X | X | X | X | X | X | X | X | X | Other Than 1 0 0 | | | X | Central System Faults and/or tests are occurring |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | Nonzero | Hardware fault in executing L66 order (no list in process) |

- Configuration Status Formats

Configuration Status is stored in L6 memory by the coupler as a result of the execution of a Store Configuration Status DCW (op code 3C) in a list processing operation initiated by L6.

When stored into L6 memory, the Configuration Status occupies two consecutive word locations as shown below.




A Full 24 bit address is supplied as the L66 Mailbox; this consists of six high order zeros, followed by twelve bits from the L66 Mailbox switches, followed by six low order zeros.

## 4.2 HARDWARE INTERFACE

The coupler interfaces with the L66 Direct Channel and with the Level 6 bus as described in reference specifications. Each interface contains address, data, timing, control, validity, and miscellaneous signal information.

The coupler may be connected at any convenient priority position on the L6 bus since it has no real-time requirement and observes a built-in transfer rate limit.

# V PERFORMANCE

The coupler will dynamically adjust its instantaneous transfer rate, without loss of information, according to the rates at which information can be sent or received across its interfaces. To avoid contention problems with other system components the coupler is provided with a rate throttle which when ON sets a limit of 125,000 words (36 bits) per second. The TH bit in the Task Register controls this.

Couplers may be located at any convenient priority position of the L6 bus to which they are connected since they have no real time requirements and observe a built-in transfer limit.

Neglecting bus contention, the natural (unthrottled) rate of the coupler will be as follows:

- In ASCII and Transliteration modes with starting addresses even-aligned: 235,000 words (36 bits) per second.
- In all other cases: 125,000 words per second (approximately).

# VI ENVIRONMENT

## 6.1 PACKAGING

The coupler is packaged on a mother board plus a full size daughter board.

## 6.2 ENVIRONMENTAL CONDITIONS

- Temperature: $0^{\circ}C$ to $50^{\circ}C$ Ambient
- Humidity: 5% to 95%

## 6.3 ELECTRICAL SPECIFICATIONS

The coupler will draw all of its power from the L6 chassis into which it is connected. The coupler itself meets all applicable Underwriter Laboratories and Canadian Standards Association requirements.

Power requirements are 22 amp at +5V.

## 6.4 CABLING

The coupler connects the Direct Channel interface of the L66 IOM through two cables as described in reference specification A58001102. As described therein, cable lengths of 75 feet maximum are permitted.

# VII RELIABILITY AND MAINTAINABILITY

## 7.1 GENERAL REQUIREMENTS

1. Mean Time Between Failures (MTBF): 71,000 hours
2. Mean Time To Repair (MTTR): 1 hour

MTTR represents the average repair time for a service engineer to diagnose, isolate, repair or replace and verify the fix.

Each board of the coupler is an Optimum Replaceable Unit (ORU).

## 7.2 MAINTENANCE FEATURES

### 7.2.1 Quality Logic Test (QLT)

The coupler contains a QLT which is initiated after an initialization of the coupler.

This QLT will verify that the command interface of the L6 to the coupler functions such that a software test and verification routine can be run from L6.

### 7.2.2 Error Checking and Reporting

Extensive integrity checks are built into the coupler on the data stream, for op code checking, etc. The coupler also senses all integrity signals from both interfaces and reports problems in its status to the L6 processor.

## 7.3 DIAGNOSTIC AIDS

### 7.3.1 Dump Scratchpad IOLD (FC=19 addressed to channel 0/1)

This order causes the coupler to store the contents of its 16 scratchpad locations in memory. The addresses are interpreted as word addresses (i.e., the lowest order bit is ignored) and the range is ignored; a total of 16 words are stored. A tentative layout of the scratchpad data is shown in Figure 7-1.

### 7.3.2 Test Modes

These modes are controlled by the OPL and TEST bits of Configuration Register A as follows:

| OPL | TEST | MODE |
|---|---|---|
| 0 | 0 | INTERNAL TEST |
| 0 | 1 | RFU |
| 1 | 0 | NORMAL MODE |
| 1 | 1 | EXTERNAL TEST |

In internal test mode, all L66 interface cycles (read L66 memory, write L66 memory or interrupt L66) are inhibited within the coupler. Any attempted cycles will result in a terminate interrupt with Transaction Timeout status. This can be used to verify the transaction timeout function.

The coupler is initialized to Normal Mode.

In external test mode, the L66 interface unit will not access L66 memory. Instead, data sent to it in write L66 operations is retained in its interface register (36 bits) and is delivered back to the coupler on a subsequent read operation. The coupler disables its parity checker in this mode because the L66 does not generate parity in this type of operation.

### 7.3.3 Internal Wraparound DCW (OC=37)

This DCW causes a fixed amount of data to be read from L6 memory by the coupler. The appropriate transfer pack/unpack is performed and the data is temporarily placed in the couplers L66 interface registers. Next, the reverse transfer pack/unpack is performed and the data is stored back in memory. The tally serves as a positive displacement of the input buffer relative to the output buffer. The addition of this displacement is performed by incrementing the address and decrementing the tally until the tally reaches zero in order to at least partially check the address increment and tally decrement mechanism.

| LOC | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | CP CHAN NO | | | | | | | | | | TERM INTP LEVEL | | | | | |
| | 1 | CS BAR | FEP BAR | RFU | | | | | | OPL | TEST | SPEC INTP LEVEL | | | | | |
| | 2 | RFU | | | | | | | | | | | | | | | |
| | 3 | 0 | ATT | 0 | ESE | ESP | CNO | CSP | CSR | CSW | COP | TT | 0 | MY | NER | LGB | MR |
| | 4 | BV | CWE | IFC | IDCW | IPCW | HF6 | HF66 | HFDCW | ST BT | RFU | INTP L6 CELL NO | | | | | |
| | 5 | TH | BOOT INH | TEST/TERM INTP CELL | | | SPECIAL INTP CELL | | | DCW | | | | | | | |
| | 6 | DCW LIST BASE ADDR | | | | | | | | | | | | | | | |
| | 7 | DCW RANGE | | | | | | | | | | | | | | | |
| | 8 | DCW DISPL | | | | | | | | | | | | | | | |
| | 9 | BARRICADE BASE (8-15) | | | | | | | | BARRICADE BASE (0-7) | | | | | | | |
| | A | BARRICADE SIZE | | | | | | | | | | | | | | | |
| | B | TALLY | | | | | | | | | | | | | | | |
| | C | L6 ACTV | L66 ACTV | DCW ACTV | RHU | INTP REQD | FLT | RHU | | TERM PDG | RHU | RHU | STATUS PDG | RHU | | | |
| | D | RHU | | | | | | | | | | | | BN | | CN | |
| | E | RHU | | | | | | | | | | | | | | | |
| | F | LAST DCW OP CODE | | | | | | | | MODE/CELL/LEVEL | | | | | | | |

NOTE

Firmware revision number is stored in Loc. F after initialize.

(Tentative Information - Shown for Reference only)

Figure 7-1 Scratchpad Memory Data Format

The operation varies slightly depending on the transfer mode as follows:

- Binary

  The address is forced even byte. The tally is in words.

  Nine bytes are transferred and packed into 72 contiguous bits. The data is then unpacked and stored at Initial Addr (forced even) + 2 * Tally.

  The lower half of the fifth word is ignored on output and not altered on input.

  If the tally is less than 5, the output is stopped when the tally reaches zero but 5 words are still stored using the previous contents of the couplers L66 interface registers as the remaining data. In particular, a tally of 0 will result in the entire previous contents of these registers (address register first, followed by the data register, 36 bits each) to be stored starting at the initial address.

- BCD

  The address is forced even byte. The tally is in words.

  Twelve bytes are transferred, the lower six bits of each byte are packed into the interface registers. The reverse unpacking is then performed and the data is stored at Initial Addr (even) + 2 * Tally.

  The upper two bits of each byte are ignored on output and zero filled on input.

  If the tally is less than 6, the result is the same as for tally less than 5 in Binary mode.

- ASCII

  The address may be any byte address. The tally is in bytes.

  Eight bytes are transferred, loaded into the interface registers and stored back in memory at Init Addr + Tally. In all cases only eight bytes of memory are altered regardless of address alignment.

  If the tally is less than 8, the result is the same as for a low tally in the other modes with the exception that only the lower eight bits out of each nine are stored.

  If data that has been loaded in ASCII mode is retrieved in either of the other modes (with tally, etc.), the MSB of each nine-bit group will be 0.

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|---|---|---|---|---|

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