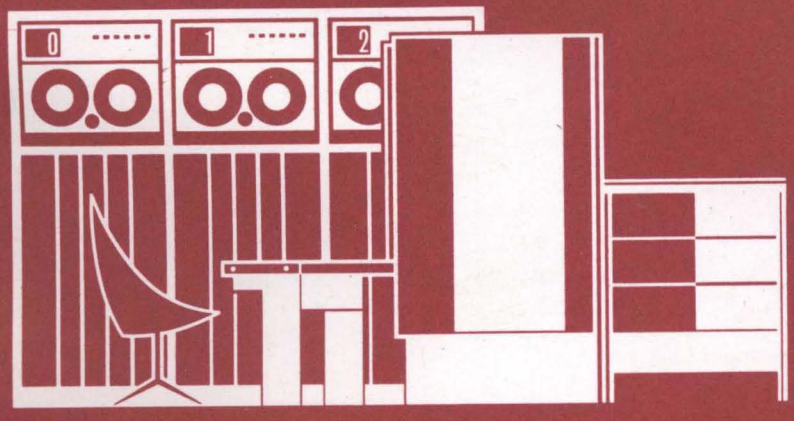
HONEYWELL 300

PROGRAMMERS' REFERENCE MANUAL



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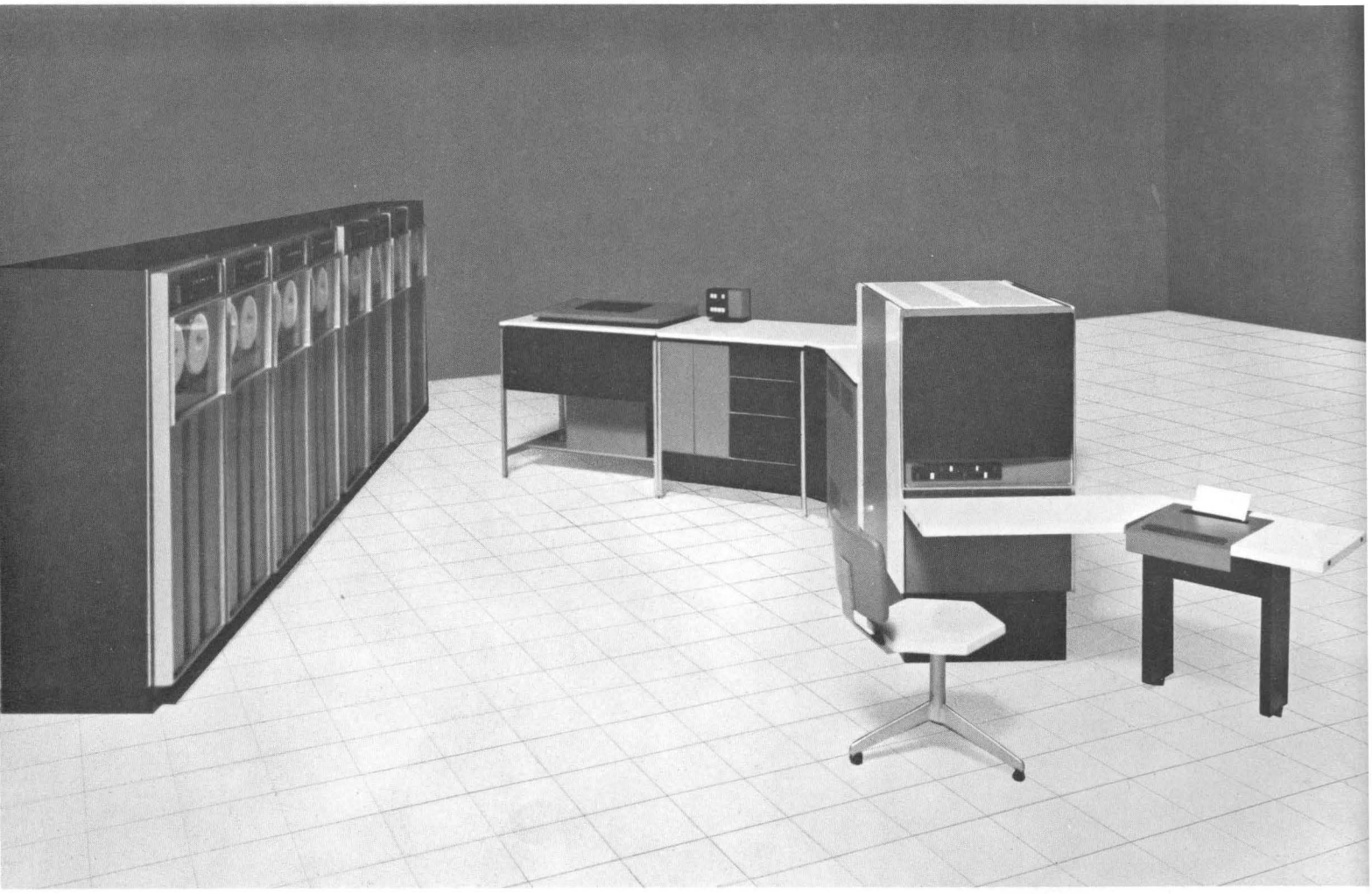
ELECTRONIC DATA PROCESSING



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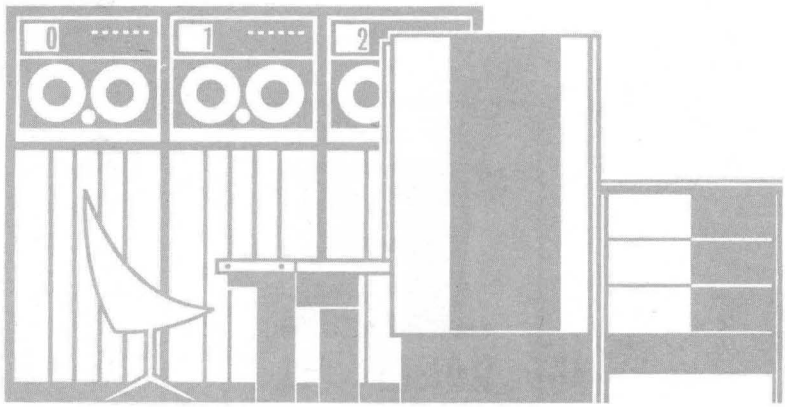

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ELECTRONIC DATA PROCESSING

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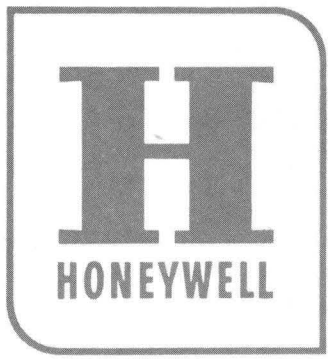
Questions and comments regarding this manual should be addressed to:

Honeywell Electronic Data Processing
Information Services
60 Walnut Street
Wellesley Hills, Massachusetts 02181



FIRST EDITION
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PREFACE

This manual is intended as a detailed reference source for programming the Honeywell 300 Electronic Data Processing System. It contains a functional description of the system components and a detailed explanation of the instruction repertoire. No previous knowledge of the Honeywell 300 is assumed.

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SECTION I
THE CENTRAL PROCESSOR

The Model 301 central processor is the computing and control center of the Honeywell 300 system. Functionally, it is composed of high-speed magnetic core main memory and control memory, an arithmetic unit, a control unit, and a direct input/output channel.

A major design feature of the central processor is the use of integrated system modules. Each module contains all of the circuitry required for a specific function. For example, one module contains all of the card control circuitry, another contains the arithmetic unit, and so on. This modularity greatly enhances the expandibility of the system. In most cases, expansion involves little more than plugging in additional modules. The reliability of the modular components has been enhanced through the use of high-temperature lithium ferrite cores and silicon semiconductors.

CONTROL PANEL

An operator's control panel is included in the basic system. This panel contains displays for the important arithmetic and control unit registers together with six sense switches for manually controlling the path of the program. Controls are also provided for starting and stopping a program and for interrogating main memory and control memory.

MAIN MEMORY

The main memory contains 4,096 locations, each capable of storing one 24-bit word and one automatically generated and checked parity bit. Additional memory is available in modules of 4,096 words up to a system total of 32,768 words. Thereafter, additional memory is available in modules of 8,192 words up to a system total of 65,536 words.

One memory cycle (that is, the time required to retrieve a word from a memory location and restore the cores to their original states) is 1.75 microseconds. The memory has an operating range of 0° to 125° Fahrenheit. The contents of memory are protected when power is turned on or off.

CONTROL MEMORY

The control memory contains sixteen 24-bit words of storage, comprising six index registers, eight general-purpose registers, the accumulator (A register), and the auxiliary arithmetic register (B register). It is driven as a linear-select memory with a split 500-nanosecond cycle (250-nanosecond read and 250-nanosecond write). The contents of control memory are protected when power is turned on or off.

Summary of H-300 Central Processor Characteristics

INFORMATION UNIT	24-bit word.
MEMORY CAPACITY	4,096 words (16,384 characters), expandable to 65,536 words (262,144 characters).
CONTROL MEMORY	16 words.
ACCESS TIME	Main memory: 875 nanoseconds. Control memory: 250 nanoseconds.
CYCLE TIME	Main memory: 1.75 microseconds. Control memory: 500 nanoseconds.
PROCESSOR SPEED	Fixed-point add to accumulator: 3.5 microseconds. 285,000 fixed-point binary add instructions per second without memory interlace; up to 380,000 with interlace. Gibson mix: 180,000 instructions per second without interlace; 236,000 with interlace.
INTERNAL OPERATIONS	Fixed-point, twos-complement binary arithmetic; logic; control; and input/output. Optional multiply, divide, floating-point, and character instructions.
INSTRUCTION FORMAT	Single-address, variable format. A typical instruction includes an op code, a variant character, and an address field.
ADDRESSING	Direct main memory within a 32,768-word bank, indexed main memory, indirect main memory, and indirect indexed main memory. Optional facility to address individual characters.
CHECKING	One parity bit automatically generated and checked in each main memory word.
HARDWARE BYPASS	Use of an optional instruction which is not installed in the machine causes a subsequence to a fixed memory location. The program may there identify the instruction and execute it by means of a subroutine.
DIRECT INPUT/OUTPUT CHANNEL	One 24-bit, non-buffered input bus and one 24-bit non-buffered output bus, with control lines and an interrupt line. Up to 64 peripheral devices may be directly addressed by this channel. A standard peripheral control is supplied which services the keyboard printer, the paper tape reader, and the paper tape punch.
EXTERNAL LINES	15 external sensing lines and 15 external activating lines.
READ/WRITE CHANNELS	Up to three optional read/write channels. Data transfer over these channels can occur simultaneously with computing.
SENSE SWITCHES	Six.
INDEX REGISTERS	Six.
PRIORITY INTERRUPT	Six levels, expandable to 24 levels.
TEMPERATURE RANGE	The temperature range of the central processor (including memory) is 0° to 125° Fahrenheit.
POWER FAILURE PROTECTION	Sensing circuitry is provided which detects power failure and causes a subsequence. Sufficient energy is retained to store the status of the machine. Power cycling, on and off, is done in such a way as to protect the contents of main memory and control memory.

CONTROL UNIT

The control unit controls the flow of information within the central processor; it selects, interprets, and controls the execution of all instructions and governs address selection within the main memory. The control unit includes a sequence register, an operation code register, a shift counter, a clocking system, and subcommand generators.

ARITHMETIC UNIT

The arithmetic unit performs twos-complement arithmetic operations, as well as logical, shift, and comparison operations. The arithmetic registers that are accessible by program are located in the control memory. The arithmetic unit also includes an addend register, an augend register, and some auxiliary circuitry; these are not accessible by program.

MEMORY INTERLACE

In systems containing more than 8,192 words of memory, an interlace option is available which permits simultaneous addressing of two or more 8,192-word blocks. Using this option, if the program is stored in one block and data are stored in another, the central processor can automatically overlap operand processing for the current instruction with retrieval of the next instruction. Execution times for instructions may thereby be reduced by as much as one memory cycle.

In systems containing both the buffered input/output (i.e., one or more read/write channels) and the memory interlace features, if data transfer uses a memory block not used in computing, the transfer is overlapped with computing. That is, data may be transferred into or out of one block while the program is processing instructions in another block. To achieve both the instruction interlace and the input/output interlace, more than two blocks of memory are required. Then operand processing, instruction retrieval, and input/output can be overlapped in their respective blocks.

SECTION II
THE INPUT/OUTPUT SYSTEMS

The standard input/output systems consist of two sets of external lines, a direct input/output channel, a standard peripheral control, and a priority interrupt system.

EXTERNAL LINES

There is a set of 15 activating lines from the central processor to external points and another set of 15 sensing lines from external points to the central processor. Two instructions address these lines. The STE (Set External Point) instruction delivers a pulse to the external activating line(s) specified by the low-order 15 bits of the instruction. The SKE (Skip if Signal Not Set) instruction examines the external sensing line(s) specified by the low-order 15 bits of the instruction. If any of the external sensing lines tested is not set, the next instruction is skipped. Any combination of external lines may be set or tested with the appropriate instruction.

DIRECT INPUT/OUTPUT CHANNEL

The H-300 is equipped with a direct input/output channel consisting of a 24-bit input bus, a 24-bit output bus, an interrupt line, and a set of control lines (see Figure 1). The control lines carry control pulses, data pulses, and responses from peripheral control units. Control pulses and data pulses are used to define the meaning of the information that is on the input or output bus. The addressed peripheral control interprets the pulses and control information and either issues a response or directs the actions of the attached peripheral devices.

Standard Peripheral Control

A standard peripheral control which services a keyboard printer, a paper tape reader, and a paper tape punch is part of the central processor. The control is permanently attached to the direct input/output channel as illustrated in Figure 1. Up to seven additional peripheral controls handling up to 60 additional devices may be attached to the direct input/output channel. Since the devices controlled by this unit read or write one character at a time, the control is designed to receive or transmit the largest of the characters, which is the eight-bit character from the eight-channel paper tape device. The devices that may be connected to the standard control are as follows:

Model 309 Paper Tape Reader (300 characters per second)
Model 310 Paper Tape Punch (120 characters per second)
Model 320 Keyboard Printer (10 characters per second)

As illustrated in Figure 1, the keyboard printer is attached to separately addressable input and output lines.

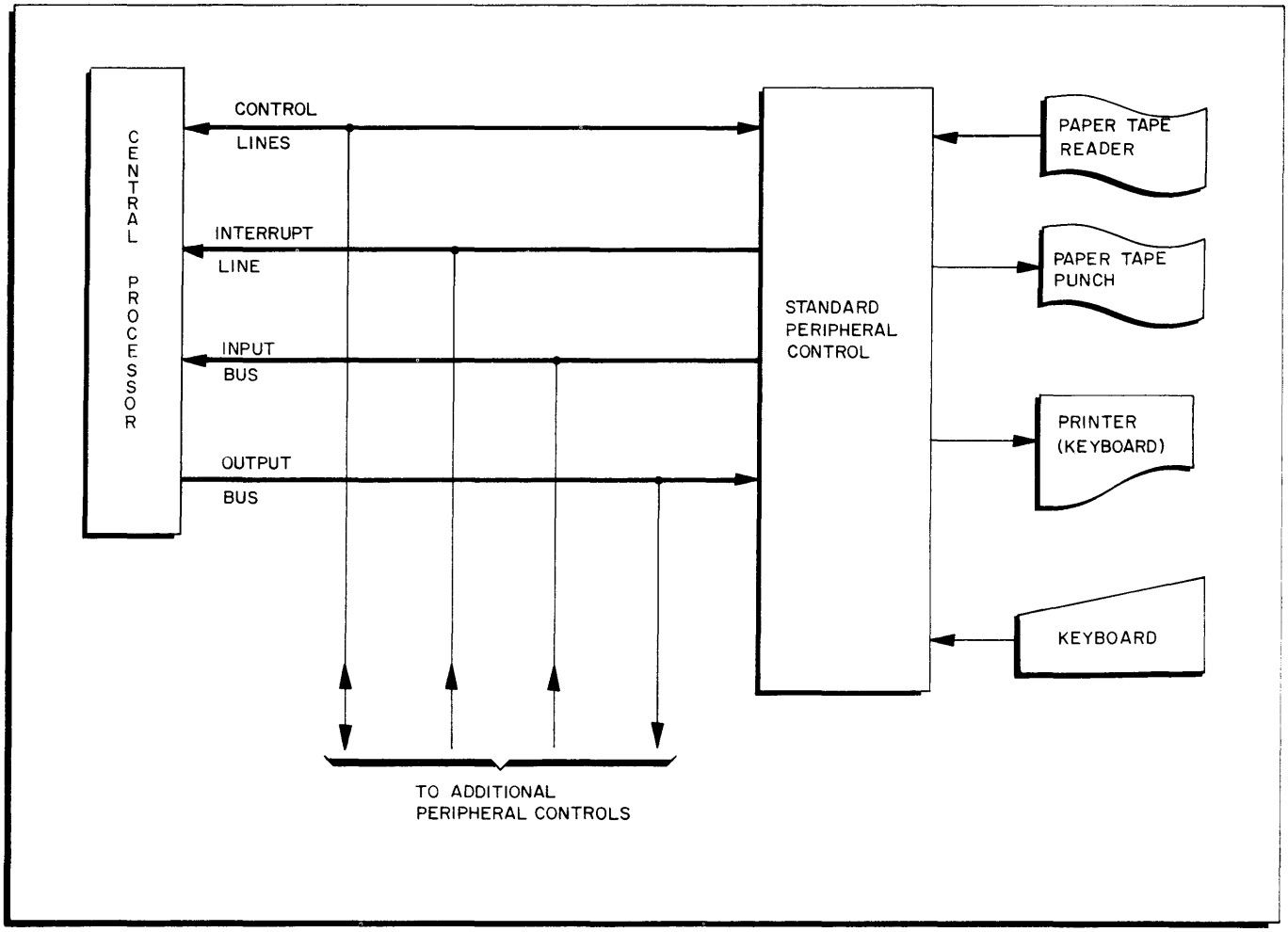


Figure 1. The Direct Input/Output Channel

Three instructions are used in conjunction with the direct input/output channel. These are the Control and Skip instruction (SKC), the Peripheral Input instruction (PIN), and the Peripheral Output instruction (POT). The SKC instruction generates control pulses to inform the peripheral controls attached to the direct input/output channel that the bus contains control information. The PIN and POT instructions transfer data to and from the central processor, respectively.

Operation of the Standard Peripheral Control

When any one of the devices attached to the standard peripheral control is ready to transmit or receive information, an interrupt signal is generated on the interrupt line servicing the direct input/output channel. The program may then scan the devices connected to the standard control to determine which one caused the interrupt. This is done by means of a series of SKC instructions which interrogate each attached device in turn. When the device issuing the interrupt is determined, it can be serviced by a PIN or POT instruction as appropriate.

When an SKC instruction is executed, the specified control line is energized. All the peripheral controls attached to the bus examine the bits on the control line. These bits designate the address of the device to which the SKC instruction is directed as well as the question or command to be interpreted by the peripheral control.

Only the addressed device responds to the SKC instruction by connecting itself logically to the bus. If a response is requested by the SKC instruction, it is sent over the appropriate response line to the central processor; if a response is not received within a set time period (e.g., if a non-existent device is addressed or if the addressed device has been powered down), a negative response is assumed.

When a PIN or POT instruction is issued, a "ready" response is required. Since only one device may be connected logically to the bus at a time, there can be no ambiguity as to which device is to respond. If the response is positive, the instruction is executed and the next instruction is skipped. If the response is negative, the instruction is not executed but the next instruction is executed. In any case, the central processor does not stall while waiting for a peripheral device.

Priority Interrupt

The H-300 has six levels of priority interrupt. These may be optionally expanded in groups of six levels to a maximum of 24 levels. One of the basic six interrupt lines is associated with the direct input/output channel.

The priority interrupt system features automatic generation of subsequence addresses for each external line according to a fixed priority, with the ability to block (disable) individual lines selectively. Priority of the interrupt lines is determined according to bit position in the interrupt register, with the high-order bit position having the highest priority.

Blocking

Only the bit positions in the interrupt register for which there is a corresponding one-bit in the interrupt mask register can cause a subsequence. The mask register may be loaded from memory by using the LIM (Load Interrupt Mask) instruction or its contents may be exchanged with memory using the XML (Exchange Interrupt Mask) instruction.

The interrupt block is automatically set when a subsequence occurs. It remains set until cleared by the SRB (Set/Reset Interrupt Block) instruction. The block may also be set by the program using the SRB instruction.

Operation of the Interrupt System

If (1) an interrupt signal exists when execution of an instruction has been completed, (2) one or more bits of the interrupt register contain a one, (3) the corresponding bit(s) in the interrupt mask register are one, and (4) the interrupt block is not set, a subsequence is automatically made to the address corresponding to the bit of highest priority and the interrupt block is set. The bit corresponding to the interrupt line which caused the subsequence is cleared to zero in the interrupt register. All other interrupts which are present when the block is set or which are generated after the block is set are remembered for later servicing when the interrupt block is cleared. Clearing of the interrupt block by means of the Set/Reset Interrupt Block instruction (SRB) is delayed long enough to permit one additional instruction to be executed before the block is cleared. Thus, uninterrupted execution of the instruction following the SRB instruction is guaranteed.

BUFFERED INPUT/OUTPUT

Up to three optional read/write channels may be installed which permit simultaneous operation of up to three peripheral devices with either a direct input/output operation or computing. Buffered input/output makes it possible, for example, to print, read and write tape, and compute — all at the same time.

Simultaneity of operation is achieved through time sharing and is based on the fact that all input/output operations require access to the main memory for only a small part of the time that they are in progress. Therefore, when an input/output operation is in progress but is not using the main memory, another peripheral device or the central processor may gain access to the main memory. It is the function of the input/output traffic control to direct the time sharing of the main memory by the various peripheral devices and the central processor.

In order to understand how the traffic control does this, the programmer must have an understanding of how data is transferred between a peripheral device and the main memory. Figure 2 illustrates the basic elements which form the data path between a peripheral device and the main memory.

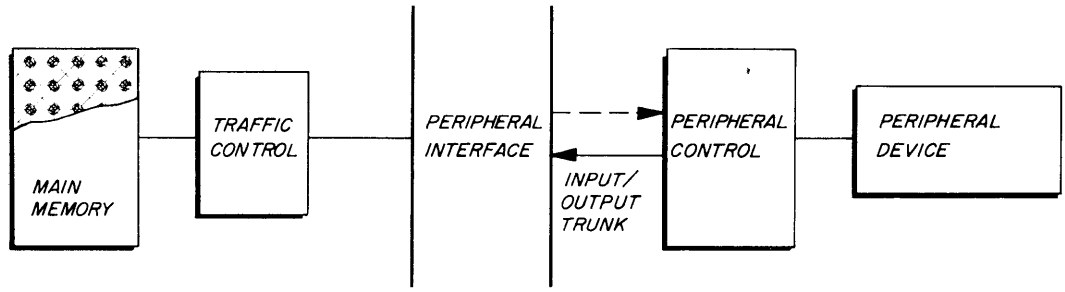


Figure 2. Buffered Input/Output Data Path

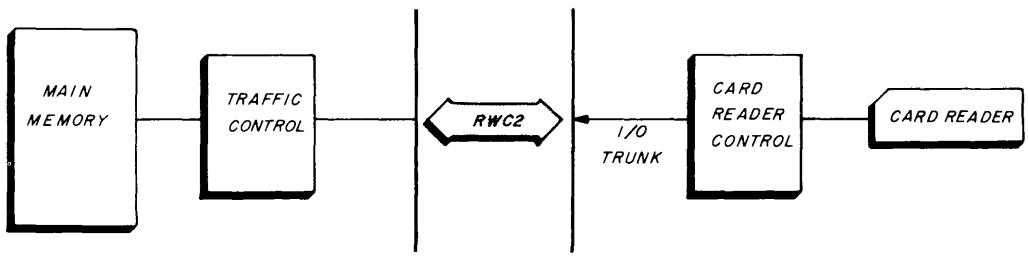
Input/Output Trunks

The H-300 System can be equipped with eight input/output lines (expandable to 16) which permanently connect the control units of the various peripheral devices to the peripheral interface. For example, a card reader and its control are permanently connected to the interface via an input trunk, while a printer and its associated control are attached via an output trunk. Each of these trunks is 6 bits wide and is therefore compatible with all standard Honeywell peripheral controls.

Read/Write Channels

Notice that the data path shown in Figure 2 is incomplete: there is no connection across the peripheral interface. This final link in the data path, known as a "read/write channel," is inserted when an input/output instruction is executed. Up to three read/write channels, labeled RWC1, RWC2, and RWC3 are available as options.

When the programmer codes an input/output instruction, he specifies, among other things, the peripheral control that is to receive or transmit data and the read/write channel over which the data transfer is to take place. For example, an instruction might specify a card read operation in which the card reader control transmits data over RWC2. When this instruction is executed in the stored program, the data path will look like this.



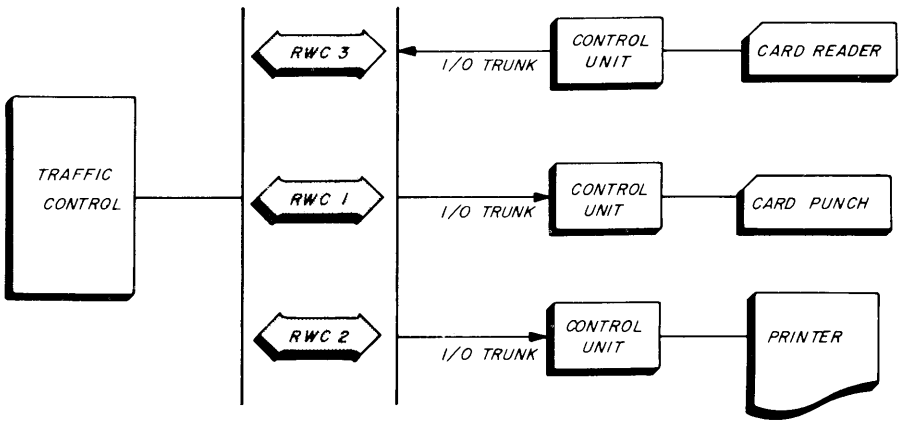
As soon as the data transfer is completed, RWC2 is automatically removed from the interface. This means that the programmer can assign RWC2 to another peripheral control in another input/output instruction. This is an extremely important feature. There is no predefined relationship between the read/write channels and the peripheral devices. The programmer can assign read/write channels with complete freedom.

Each read/write channel consists of a current location counter, a starting location counter, two buffer registers, a current word counter, a starting word counter, and a character counter. Most of these registers are accessible to the program by means of the Alter Register instruction (ALR). When a peripheral transfer is to be performed, the address at which the transfer is to begin is stored in both location counters.

When a six-bit (character) trunk is being controlled, there is provision for automatic packing or unpacking of the characters to or from 24-bit words. The character counter is incremented by one as each successive character is transferred. Each time the character count passes four, the contents of the present location counter and the word counter are also incremented by one.

Traffic Control

While a peripheral operation is in progress, it requires access to the main memory for only a fraction of the total time to complete the operation; most of the time is taken up by mechanical activities. Therefore, there is time available for another peripheral control to transfer data to or from the memory via another RWC. This second input/output operation can in turn share access to the main memory with a third operation which uses the remaining RWC. A typical data path configuration is shown below.



The rate at which each of the above devices transfers data over the programmer-assigned channel is dependent upon the mechanical characteristics of the particular device. For instance, the transfer rate for the printer is considerably faster than that for the card punch; therefore, the printer will require access to the main memory more frequently than the card punch. It is the function of the traffic control to monitor the requests for access to the main memory and to insure that all requests are honored within the prescribed time interval for each unit. Any device connected to a buffered I/O trunk is guaranteed an opportunity to transfer data once every 6 microseconds.

SECTION III
INFORMATION FORMAT

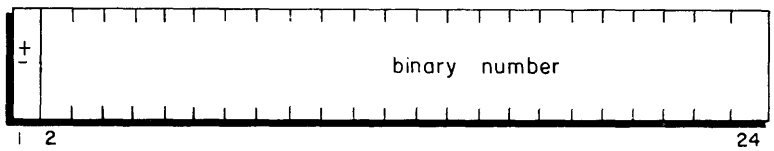
The Honeywell 300 uses a fixed-length, 24-bit word. Associated with each word is a parity bit, the value of which is not subject to program control. Subsequent discussion of the H-300 word, therefore, refers only to the 24 information bits, unless otherwise noted.

Each memory location and each arithmetic register is capable of storing one word. A machine word may represent an instruction or one or more units of data.

The H-300 is a twos-complement machine. That is, all negative numbers are stored in memory in their twos-complement form, and twos-complement arithmetic is used exclusively. Appendix A contains a discussion of twos-complement arithmetic.

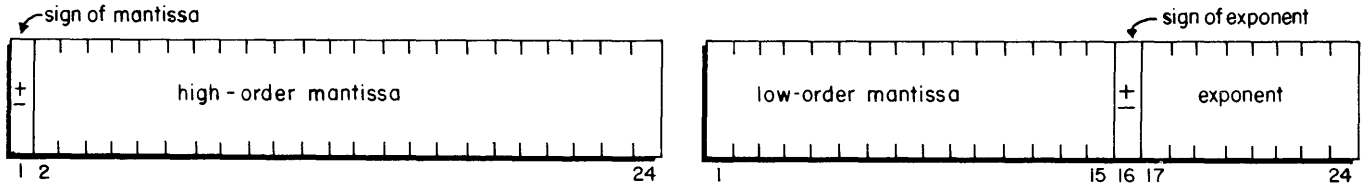
FIXED-POINT WORD

The fixed-point word contains a 24-bit, twos-complement binary number in the range minus 8, 388, 608 to plus 8, 388, 607.



FLOATING-POINT WORD

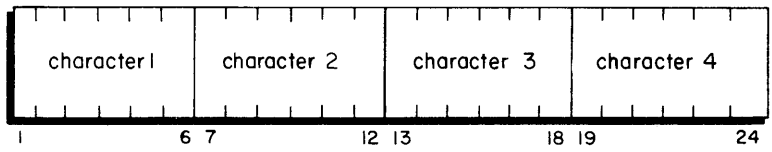
A floating point number occupies two machine words, as shown below. The first word, and the high-order 15 bits of the second word, make up the mantissa. These 39 bits hold a twos-complement binary number in the range $\pm$ 2.56 x 10^{11}. The high-order bit of the first word represents the sign of the mantissa. The exponent occupies bits 16-24 of the second word and is a 9-bit, twos-complement binary number in the range minus 256 to plus 255.



ALPHANUMERIC WORD

The alphanumeric word consists of four six-bit groups. Each group can represent one of 26 characters, 10 decimal digits, or 29 special characters such as punctuation marks, plus and minus signs, etc., or a blank. See Appendix B for a list of the H-300 character codes.

The optional character-handling instructions (Section VI) provide for the loading, testing, and storing of individual characters.



THE INSTRUCTION WORD

Bits 1 through 6 of the instruction word represent the operation code. Up to 64 instructions may be specified by this field. Additional instructions are uniquely identified by parameters in the address field and in the variant character.

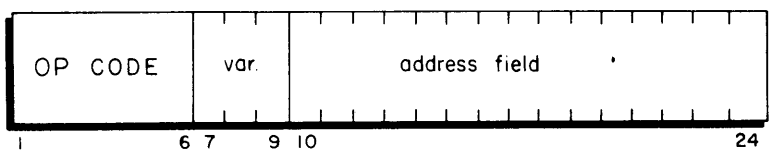
Bits 7 to 9 constitute the variant character. This octal character specifies whether the address of the word in which it appears is direct, indexed, or indirect as follows:

Variant	Type of Addressing
0	Direct
1	Indexed by index register #1
2	Indexed by index register #2
3	Indexed by index register #3
4	Indexed by index register #4
5	Indexed by index register #5
6	Indexed by index register #6
7	Indirect

The types of addressing are described in Section IV.

The remaining bits of the instruction word are the address field, which provides for direct addressing of 32,768 words of memory.

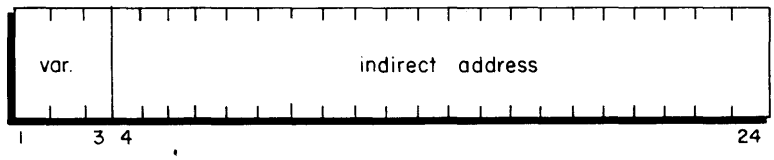
In some instructions, the address field does not specify the address of an operand. Instead, this field contains one or more parameters specifying the number of words to be moved, the number of binary positions to be shifted, etc.



THE INDIRECT ADDRESS WORD

In the indirect address word, the address variant occupies the high-order three bit positions. It has the same format and functions as in the instruction word.

The indirect address word contains no operation code. Bit positions 4 through 24 are a 21-bit address field which provides the capability of addressing memories larger than 32,768 words.



SECTION IV
ADDRESSING

DIRECT ADDRESSING

When direct addressing is used, the variant character of the instruction word is zero. Direct addressing means that the address field contains the absolute main memory address of the operand. Accordingly, the address field is loaded directly into the address register, the operand so addressed is retrieved, and the instruction is executed.

INDEXED ADDRESSING

When indexed addressing is used, the variant character of the instruction word has a value from one to six, specifying one of the six 21-bit index registers. In this case the contents of the address field are augmented by the contents of the specified index register. The contents of the address field and the index register are not altered. The resulting sum is the absolute machine address of the operand; the operand so addressed is retrieved and the instruction is executed.

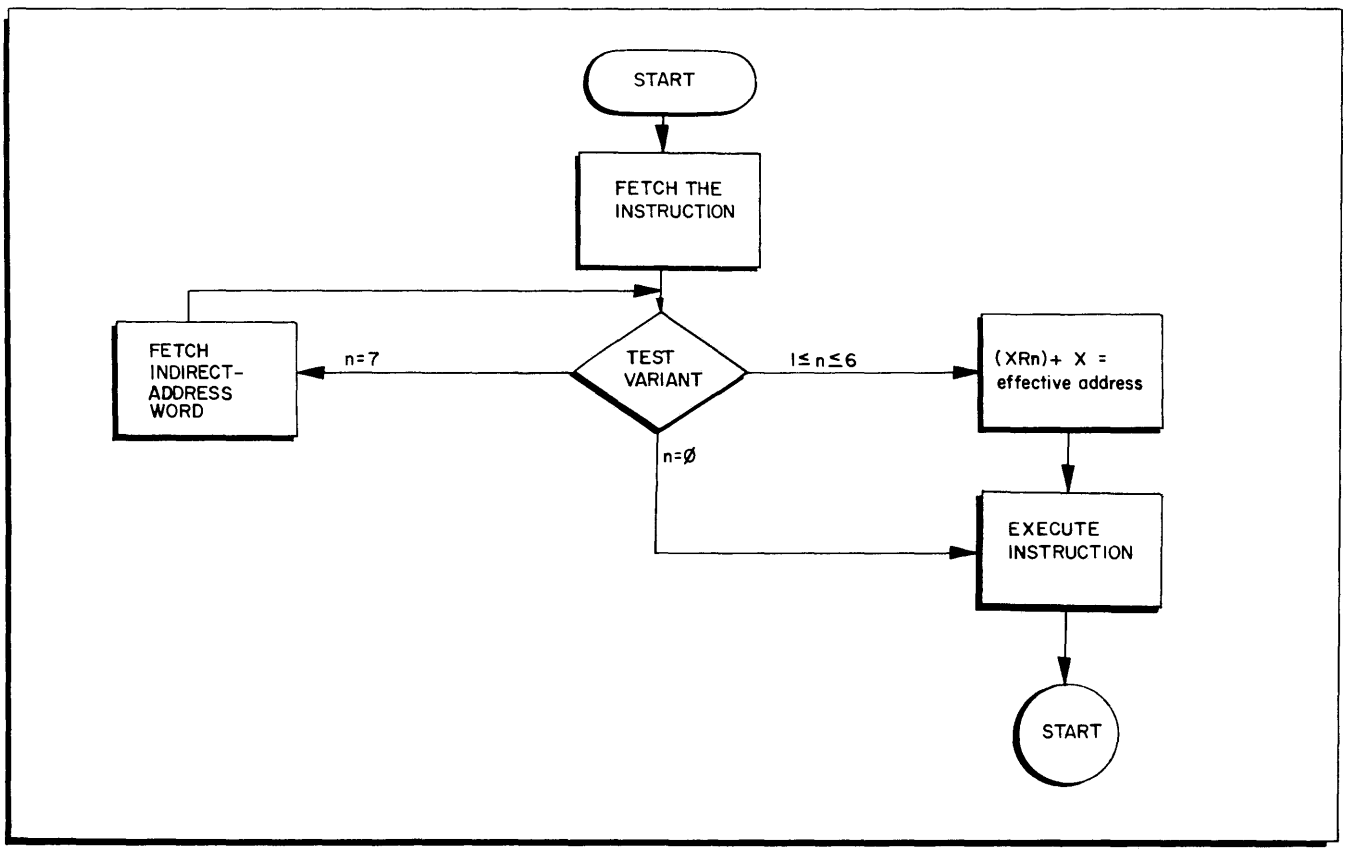


Figure 3. Types of Main Memory Addressing

INDIRECT ADDRESSING

When indirect addressing is used, the variant character of the instruction word is seven. Indirect addressing means that the address field contains not the absolute main memory address of the operand but the address of a main memory location containing another address. The contents of the location specified by the address field of the instruction word are retrieved. The variant character of the word at that address has the normal meaning but is located at the high-order end of the word to allow a 21-bit address field.

If the variant character of the indirectly addressed word is zero, bits 4 through 24 of the word are interpreted as the absolute address of the operand. This address is loaded directly into the address register, the operand so addressed is retrieved, and the instruction is executed.

If the variant character of the indirectly addressed word is seven, the addressing is multi-level indirect. The procedure for indirect addressing is repeated until a word is addressed whose variant character is not octal seven. This feature is represented by the loop in the flow chart in Figure 3.

INDIRECT INDEXED ADDRESSING

If the variant character of the indirectly addressed word has a value from one to six, the addressing is indirect indexed. That is, the 21-bit contents of the address field of the addressed word are augmented by the contents of the index register specified by the variant character. The instruction is then executed, using the operand addressed by the resulting sum.

EXPANDED MEMORY ADDRESSING

For systems with more than 32,768 words of memory, there is additional logic which includes a bank register, additional bits in the sequence register, and three additional instructions. The memory is handled in banks of 32,768 words. The additional bits in the sequence register and those of the bank register are used to specify which bank is being addressed. The instructions are divided into two sets: those whose address field normally references data (e.g., ADD, LDA) and those whose address field normally references the sequence register (e.g., JMP, JAZ). Instructions that reference the sequence register retrieve the bank indicator from the sequence register; those that reference data take their bank indicator from the bank register.

The bank indicator in the sequence register is changed by normal incrementing or by execution of a Jump instruction with indirect or indexed addressing. The bank register is changed by means of the optional instructions Load Bank Register (LBR) and Equalize Bank Register (EBR). The Store Bank Register (SBR) instruction is used to store the status of the bank register in memory.

Effective addresses for instruction execution are derived from the appropriate bank indicating register. The instructions themselves are taken from the bank specified by the bank indicator bits of the sequence register. If direct addressing is used, the bank indicator is taken from the appropriate bank indicating register. If indirect addressing is used, the bank indicator is taken from the indirectly addressed word. If indexed addressing is specified, the effective address is computed from the sum of the contents of the index register, the low-order 15 bits of the instruction word, and the appropriate bank indicator.

SECTION V
STANDARD INSTRUCTIONS

GENERAL SPECIFICATIONS

The following considerations apply to both the standard and the optional instructions (see Section VI).

Execution Timing

The execution time represents the time required to retrieve the instruction, execute it, and store the result. The following rules apply to the timing of instructions and should be used in conjunction with the timing formulas in the text. If only one timing formula is given for an instruction, the execution time is the same with and without interlace.

1. For conditional jump or skip instructions, the shorter time applies when the jump or skip is not made.
2. Indexed addressing requires, at most, an additional one-half cycle.
3. Indirect addressing requires one extra cycle per iteration.

Execution times are given in main memory cycles, where one cycle equals 1.75 microseconds.

Indicators

OVERFLOW INDICATOR. This indicator denotes the occurrence of twos-complement overflow of the accumulator. Overflow occurs when the precision of the fixed-point word is exceeded. This indicator is cleared (reset) upon being tested by an SKN instruction.

CARRY INDICATOR. The carry indicator stores the true binary carry from the high-order position of the 24-bit accumulator. This indicator is not cleared by being tested; instead, it always indicates whether the result of the last operation that involved the accumulator produced a carry.

No-Address Instructions (NAD)

There is a group of instructions all of which have the same operation code (NAD). Instead of specifying the addressing mode, the variant character is used to differentiate these instructions. The variant characters and the corresponding mnemonic operation codes are as follows:

Octal Variant	Mnemonic Operation Code
0	PAS, EBR, LBR
1	SFT

Octal Variant	Mnemonic Operation Code
2	ALR
3	SKN
4	SKC
5	STE
6	SKE
7	SRB

The PAS, EBR, and LBR instructions are differentiated by means of bits in the address field of the instruction word.

Registers

The contents of control memory registers in the central processor remain unchanged during the execution of an instruction unless otherwise specified.

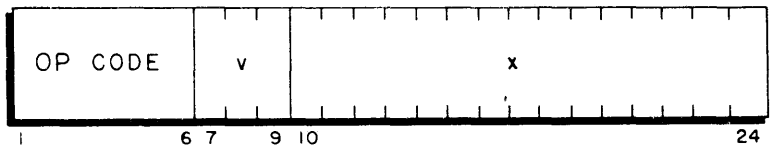
Symbology

The following symbology is used to describe H-300 instructions:

1. A = the accumulator.
2. B = the auxiliary arithmetic (B) register.
3. SR = the sequence register.
4. ( ) = the contents of the location(s) indicated within the parentheses. For example, (SR) means "the contents of the sequence register."
5. Lower-case letters represent information that must be supplied by the programmer.
6. Upper-case letters and all digits and special characters except ellipsis (dots indicating progression) are coded literally in the position indicated. For example, digits appearing in the diagram of an instruction word must be coded literally in the positions shown for proper execution of the instruction. Thus, bits 7 through 11 of the Pass instruction (page 22) must be zero.

CONTROL INSTRUCTIONS

BAR - Branch and Return

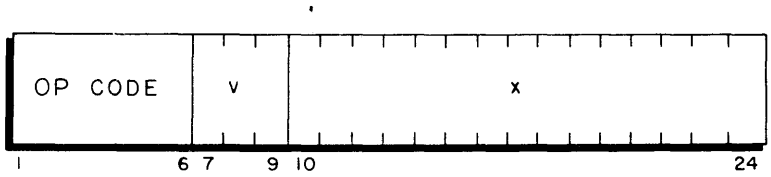


(SR) replace (x). Then the address x+1 replaces (SR) and the instruction at that address is executed.

By storing (SR), this instruction provides the option of performing a subroutine beginning at x+1 and then returning to the main sequence by jumping indirectly to x.

Timing. 2 cycles.

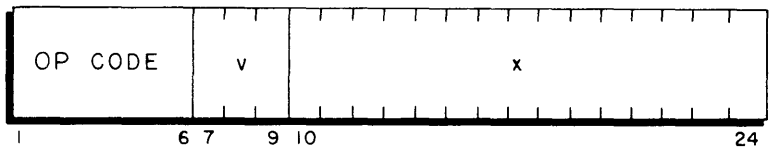
EXC - Execute



The instruction at location x is executed out of sequence. That is, (SR) are not altered. The address of the next instruction is (SR).

Timing. 1 cycle plus the time required to execute the addressed instruction.

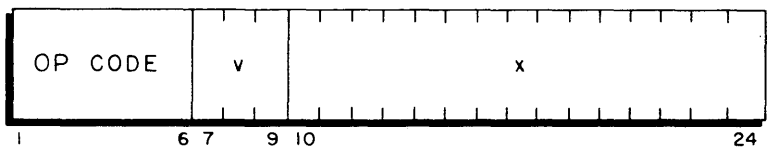
HTJ - Halt Jump



(x) replace (SR). Then the central processor halts.

Timing. 1 cycle.

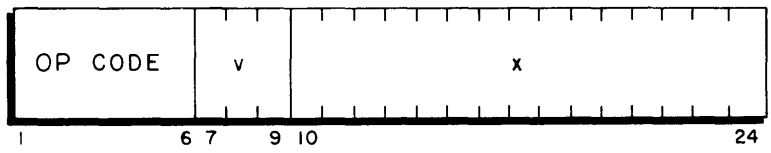
JAN - Jump on Accumulator Negative



The main memory address x replaces (SR) if the (A) are less than zero (i.e., if the high-order bit is one); else (SR) are incremented by one.

Timing. 1 or 2 cycles.

JAP – Jump on Accumulator Positive



The main memory address x replaces (SR) if (A) are equal to or greater than zero; else (SR) are incremented by one.

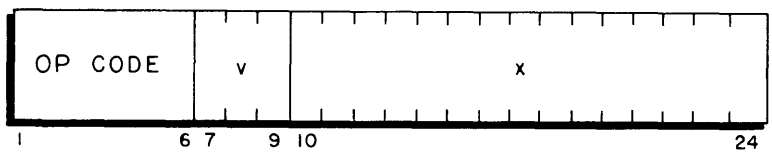
Timing. 1 or 2 cycles.

JAZ – Jump on Accumulator Zero

The main memory address x replaces (SR) if (A) equal zero; else (SR) are incremented by one.

Timing. 1 or 2 cycles.

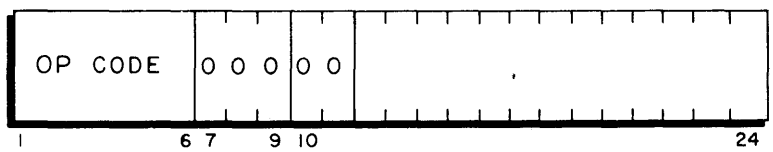
JMP – Jump



The address x replaces (SR) unconditionally.

Timing. 1 cycle.

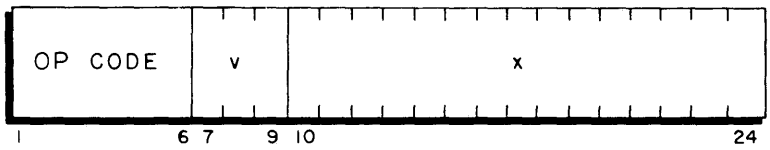
PAS – Pass (NAD)



No operation. (SR) are incremented by 1.

Timing. 1 cycle.

SKM – Skip if Accumulator and Memory are Equal



If (A) equal (x), (SR) are incremented by two (thus the next instruction is skipped); else (SR) are incremented by one.

Timing. 2 or 3 cycles. With interlace: 1 or 2 cycles.

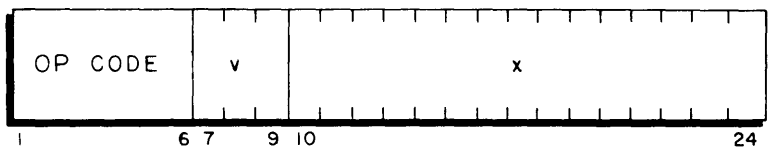
SKN – Skip if Signal is Not Set (NAD)

Each 1-bit in the address field x specifies an internal test point to be sensed. If any of the test points that are sensed is not set, (SR) are incremented by two (thus the next instruction is skipped); else (SR) are incremented by one. Any combination of test points may be sensed with one SKN instruction. The internal test points are:

Overflow	Sense Switch #5
Carry	Sense Switch #6
Sense Switch #1	Exponential Overflow
Sense Switch #2	Exponential Underflow
Sense Switch #3	Division Overcapacity
Sense Switch #4	

Timing. 2 cycles.

SMZ – Skip if Memory is Zero

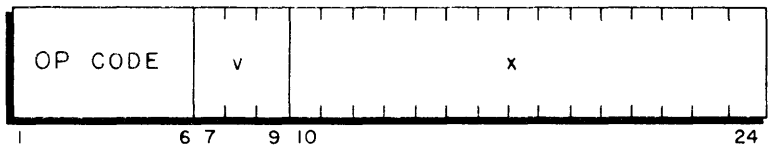


If (x) equal zero, (SR) are incremented by two (thus the next instruction is skipped); else (SR) are incremented by one.

Timing. 2 or 3 cycles. With interlace: 1 or 2 cycles.

FIXED-POINT INSTRUCTIONS

ADD - Add to Accumulator

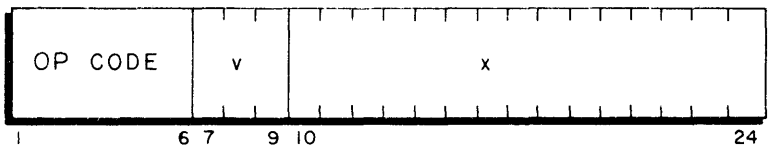


(A) are added to (x). The sum replaces (A).

Indicators. Overflow, carry.

Timing. 2 cycles. With interlace: 1.5 cycles.

ADM - Add to Memory

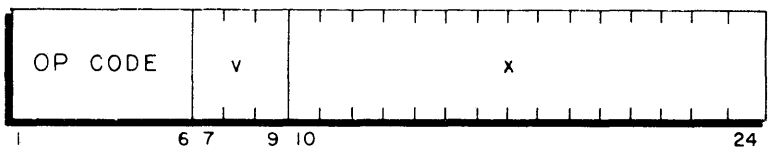


(A) are added to (x). The sum replaces (x). (A) are not altered.

Indicators. None. The current contents of the overflow and carry indicators are not altered.

Timing. 3 cycles. With interlace: 2.5 cycles.

SUB - Subtract from Accumulator

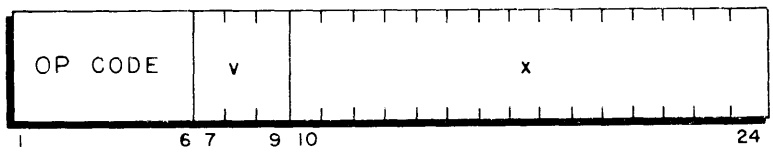


(x) are subtracted from (A). The difference replaces (A).

Indicators. Overflow, carry.

Timing. 2 cycles. With interlace: 1.5 cycles.

TLY - Tally



(x) are incremented by one. The sum replaces (x).

Timing. 3 cycles. With interlace: 2.5 cycles.

INDEXING INSTRUCTIONS

Indexing instructions are those that manipulate the contents of general purpose register 0 or the contents of one of the six index registers. The desired register is specified by the variant character of the instruction word as follows:

Octal Variant	Register
0	General Purpose Register 0
1	Index Register #1
2	Index Register #2
3	Index Register #3
4	Index Register #4
5	Index Register #5
6	Index Register #6
7	Indirect Addressing

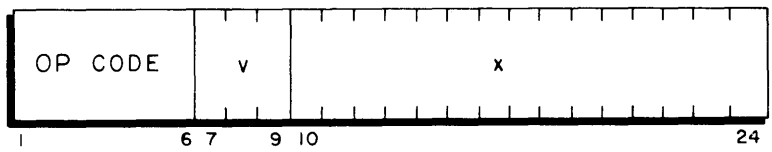
Note that a variant character of zero does not specify direct addressing.

For indexing instructions, the effective address (i.e., x in the specifications) is the contents of the address field of the first non-indirectly addressed word (namely, the first word whose variant character is not 7).

Indexing instructions can be divided into two classes depending on whether they use the effective address itself or the contents of the location specified by that address. They are designated as class I and class II indexing instructions, respectively. Class I instructions are DJX, JIX, and STX; these instructions use x and not (x). Class II instructions are AUX, LDX, and SKX; these instructions use (x) and not x.

Class I Indexing Instructions

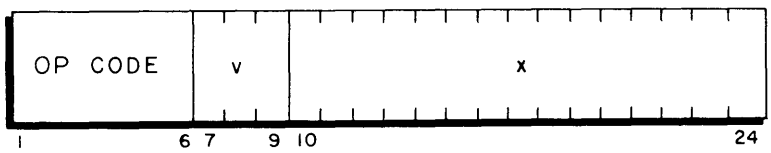
DJX - Decrement and Jump on Index Not Zero



The contents of register v are decremented by one. The result replaces the contents of that register. Then if the contents of that register are not zero, the address x replaces (SR); else (SR) are incremented by one.

Timing. 2 cycles.

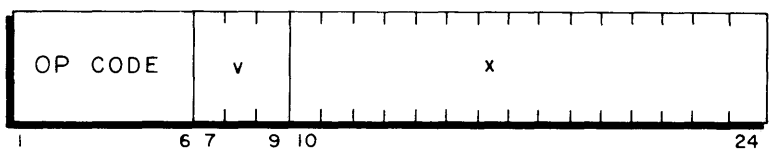
JIX - Jump on Index Not Zero



The address x replaces (SR) if the contents of register v are not zero; else (SR) are incremented by one.

Timing. 1 or 2 cycles.

STX - Store Index Register

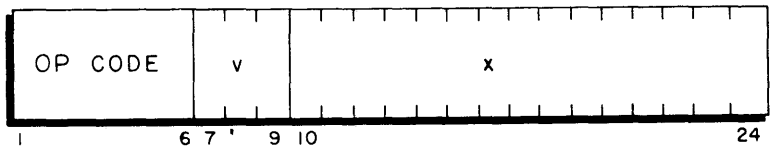


The contents of register v replace (x).

Timing. 2 cycles. With interlace: 1 cycle.

Class II Indexing Instructions

AUX - Augment Index



(x) are added to the contents of register v. The sum replaces the contents of that register.

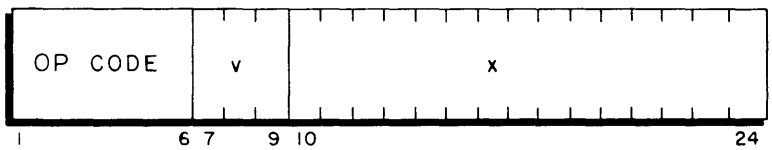
Timing. 2 cycles. With interlace: 1 cycle.

LDX - Load Index Register

(x) replace the contents of register v.

Timing. 2 cycles. With interlace: 1 cycle.

SKX - Skip on Index High



If the contents of register v are greater than (x), (SR) are incremented by two (thus the next instruction is skipped); else (SR) are incremented by one.

Timing: 2 or 3 cycles.

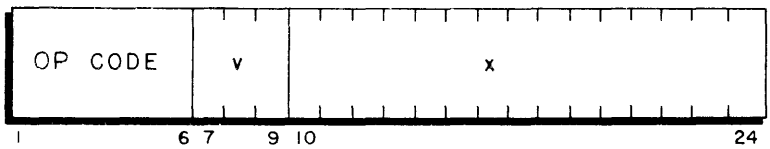
INPUT/OUTPUT INSTRUCTIONS, DIRECT

PIN – Peripheral Input

If the device connected to the input bus is not ready, the next instruction in sequence is executed; else the 24-bit word on the input bus replaces (x), and (SR) are incremented by two (thus the next instruction is skipped).

Timing. 3 cycles. With interlace: 2 cycles.

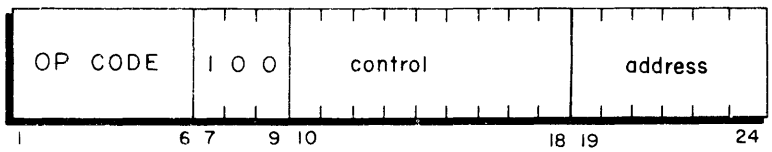
POT – Peripheral Output



If the device connected to the output bus is not ready, the next instruction in sequence is executed; else (x) are transferred to the output bus and (SR) are incremented by two (thus the next instruction is skipped).

Timing. 3 or 4 cycles. With interlace: 2 or 3 cycles.

SKC – Control and Skip (NAD)



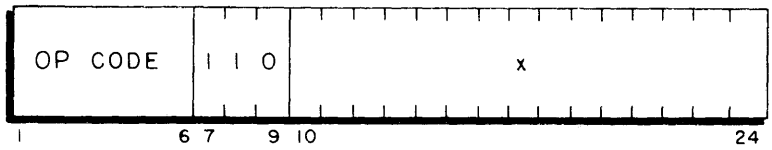
This instruction interrogates and controls peripheral devices by way of peripheral controls attached to the direct input/output channel. If a positive response is received, (SR) are incremented by one; if a negative response or no response is received, (SR) are incremented by two (thus the next instruction is skipped).

The commands that may be directed to the keyboard printer, the paper tape reader, and the paper tape punch by way of the standard peripheral control unit are as follows:

Test the addressed device for an interrupt signal.
Test the addressed device for a stored error condition.
Test the addressed device for a busy condition.
Start the addressed device.
Stop the addressed device.

Timing. 2 cycles.

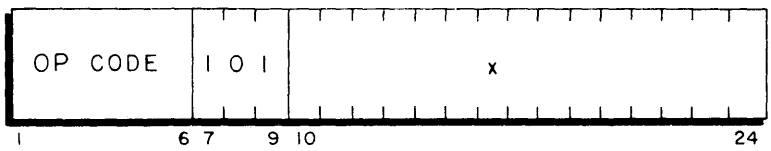
SKE – Skip if External Signal is Not Set (NAD)



Each 1-bit in the address field x specifies one of 15 external sensing lines to be tested. If all of the lines that are tested are set (carry a logical 1), (SR) are incremented by one; else (SR) are incremented by two (thus the next instruction is skipped). The status of the sensing lines is not altered.

Timing. 1 or 2 cycles.

STE – Set External Point (NAD)

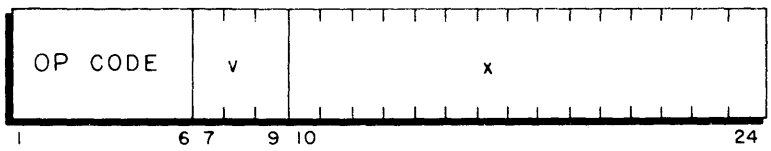


Each 1 bit in the address field x causes a pulse to be sent over one of 15 external activating lines.

Timing. 1 cycle.

INTERRUPT INSTRUCTIONS

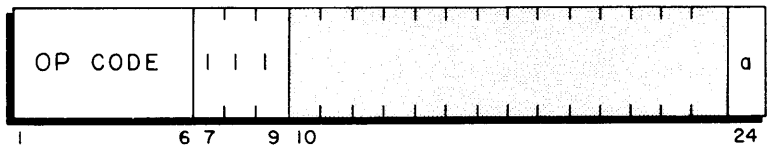
LIM – Load Interrupt Mask



(x) replace the contents of the interrupt mask register.

Timing. 2 cycles. With interlace: 1 cycle.

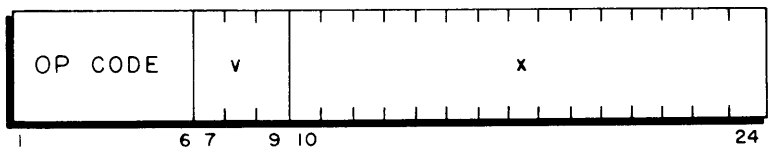
SRB – Set/Reset Interrupt Block (NAD)



If parameter a (the low-order bit of the address field) is one, the interrupt block is set, blocking all peripheral interrupts. If parameter a is zero, the interrupt block is cleared, enabling all peripheral interrupts; in this case the next instruction in sequence will be under way before the status change occurs and is therefore not interrupted.

Timing. 1 cycle.

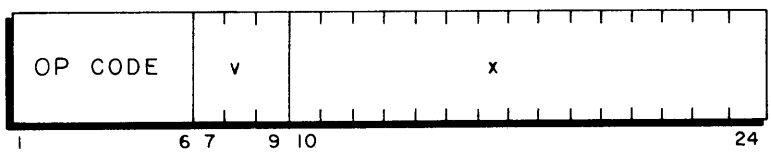
STI – Store Interrupt Register



The contents of the interrupt register replace (x) and are not altered.

Timing. 2 cycles. With interlace: 1 cycle.

XML – Exchange Interrupt Mask

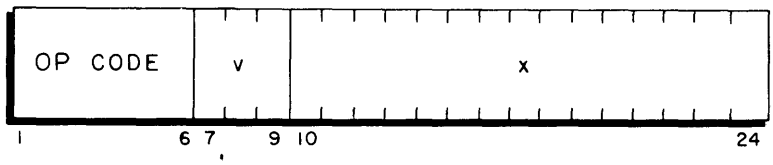


The contents of the interrupt mask register are exchanged with (x).

Timing. 3 cycles. With interlace: 2 cycles.

LOGIC INSTRUCTIONS

EXT - Extract (Logical AND)

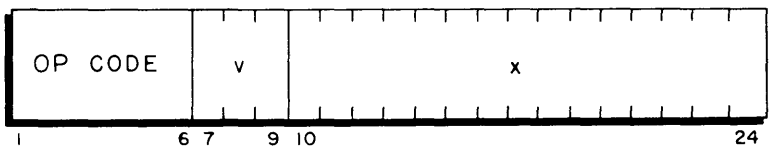


(A) logical-AND (x) replace (A). That is, if corresponding bits in (A) and (x) are both one, a one replaces the bit in (A); else a zero replaces the bit in (A). (x) are unchanged. Hence the following truth table:

(A)	AND (x)	GIVING (A)
0	0	0
0	1	0
1	0	0
1	1	1

Timing. 2 cycles. With interlace: 1 cycle.

HAD - Half Add (Exclusive OR)

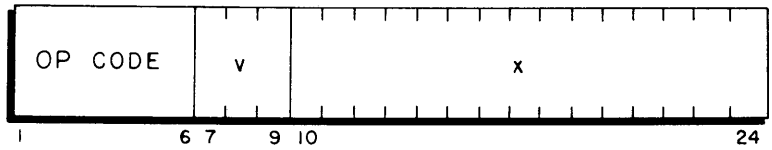


(A) exclusive-OR (x) replace (A). That is, if corresponding bits in (A) and (x) are not identical, a one replaces the bit in (A); else a zero replaces the bit in (A). Hence the following truth table:

(A)	OR (x)	GIVING (A)
0	0	0
0	1	1
1	0	1
1	1	0

Timing. 2 cycles. With interlace: 1 cycle.

SMP – Superimpose (Inclusive OR)

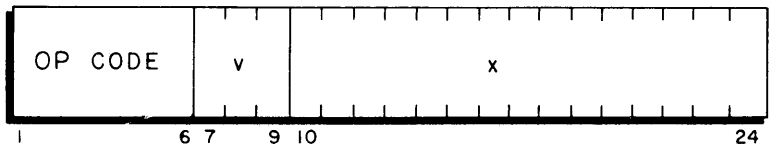


(A) inclusive-OR (x) replace (A). That is, if corresponding bits in either (A) or (x), or both, are one, a one replaces the bit in (A); else a zero replaces the bit in (A). Hence the following truth table:

(A)	OR	(x)	GIVING	(A)
0		0		0
0		1		1
1		0		1
1		1		1

Timing. 2 cycles. With interlace: 1 cycle.

SST – Substitute



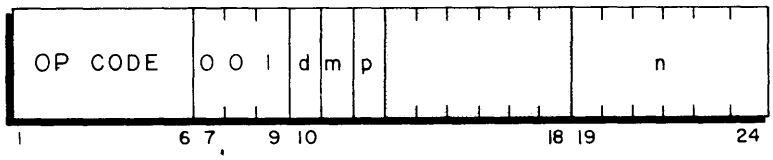
For corresponding bit positions in (A), (B), and (x), if the bit in (B) is one, the bit in (A) replaces the bit in (x); else the bit in (x) is protected. Thus, (B) are a mask. Hence the following truth table:

(A)	(B)	(x)	GIVING (x)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Timing. 3 cycles. With interlace: 2 cycles.

SHIFT INSTRUCTION

SFT – Shift (NAD)



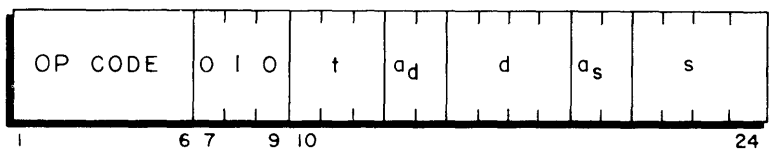
(A), or, if double precision is specified, (A, B) are shifted n places to the left or right in the rotate or arithmetic mode. In a left arithmetic shift, zero replaces each of the emptied positions. In a right arithmetic shift, the high-order bit of (A) is duplicated in each of the emptied positions.

PARAMETER	INTERPRETATION
d	Direction Indicator Left shift if d is 0. Right shift is d is 1.
m	Mode Indicator Rotate if m is 0. Bits moved off the end of the word(s) are transferred end-around to the other end of the word(s). Arithmetic if m is 1. Bits moved off the end of the word(s) are lost.
p	Precision Indicator Single precision if p is 0. Only (A) are operated upon. Double precision if p is 1. (A, B) are operated upon.
n	Number of binary places to be shifted.

Timing. $1+\frac{3n}{7}$.

WORD TRANSMISSION INSTRUCTIONS

ALR – Alter Register (NAD)



The contents of the control memory register specified by the source address s, under control of parameter a_s, replace the contents of the register specified by the destination address d. For an exchange, in addition to the above, the contents of the control memory register

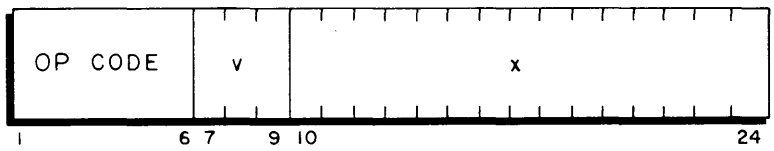
specified by the destination address d, under control of parameter a_d, replace the content of the register specified by the source address s. If d = s, the contents of the register so specified are altered as specified by a_s. The control memory registers are addressed as follows:

Register	Octal Address
General-Purpose Register 0	00
Index Register 1	01
Index Register 2	02
Index Register 3	03
Index Register 4	04
Index Register 5	05
Index Register 6	06
A Register (Accumulator)	07
General-Purpose Register 1	10
General-Purpose Register 2	11
General-Purpose Register 3	12
General-Purpose Register 4	13
General-Purpose Register 5	14
General-Purpose Register 6	15
General-Purpose Register 7	16
B Register (Auxiliary Arithmetic Register)	17

PARAMETER	INTERPRETATION
t	Transfer Mode One-way transfer within control memory if t is 0. The contents of the source register s replace the contents of the destination register d as specified by a_s. Exchange within control memory is t is 1. The contents of the source register s replace the contents of the destination register d as specified by a_s. Also, the contents of the destination register d replace the contents of the source register s as specified by a_d. One-way transfer from the counters associated with the read/write channels if t is 2.
a_d	Alter Mode for Destination Register Transfer the contents unaltered if a_d is 0. Transfer the twos-complement of the contents if a_d is 1. Transfer the absolute value of the contents if a_d is 2.
d	Destination address. Address of a control memory register.
a_s	Alter mode for source register. Same options as for a_d.
s	Source address. Address of a control memory register.

Timing. 1.5 cycles.

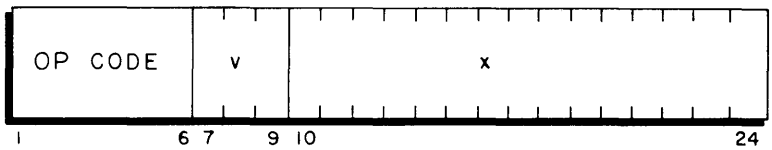
DLD - Double-Precision Load



(x) replace (A); (x+1) replace (B).

Timing. 3 cycles. With interlace: 2 cycles.

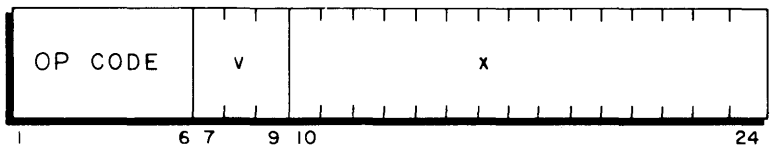
DST - Double-Precision Store



(A) replace (x); (B) replace (x+1).

Timing. 3 cycles. With interlace: 2 cycles.

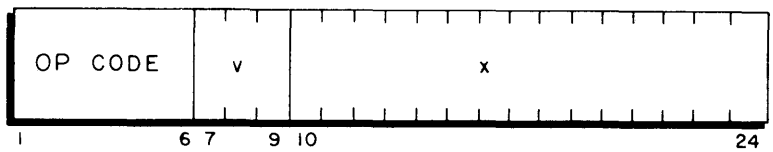
LDA - Load Accumulator



(x) replace (A).

Timing. 2 cycles. With interlace: 1 cycle.

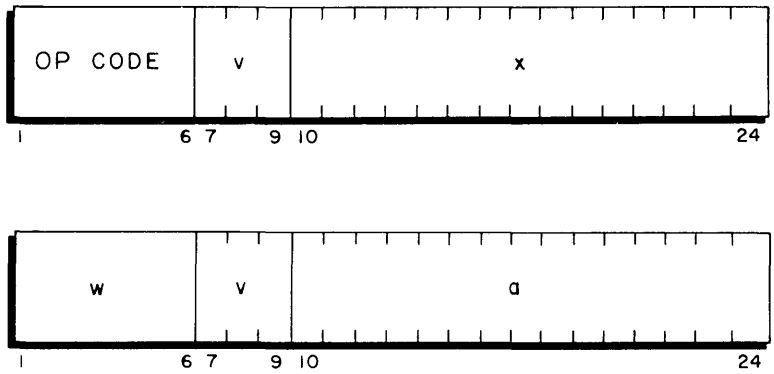
LDB - Load B Register



(x) replace (B).

Timing. 2 cycles. With interlace: 1 cycle.

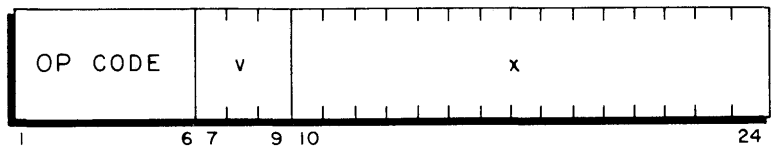
MTR - Multiple Transfer



Starting with (x), w words ($0 \leq w \leq 63$) are transferred to consecutive main memory locations starting with address a. The addresses x and a have independent variant characters. This is a two-word instruction.

Timing. 2.5 + 2w cycles. With interlace: 3.5 + w cycles.

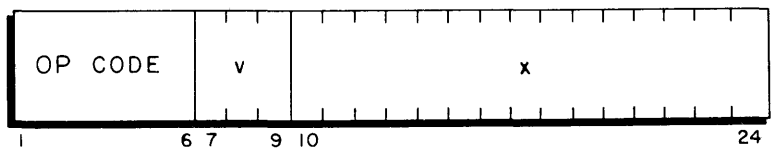
STA - Store Accumulator



(A) replace (x).

Timing. 2 cycles. With interlace: 1 cycle.

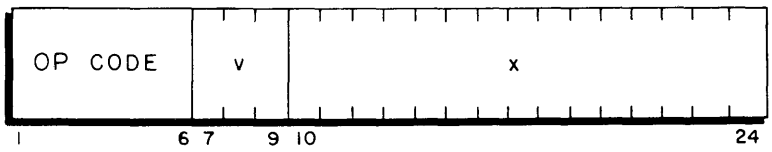
STB - Store B Register



(B) replace (x).

Timing. 2 cycles. With interlace: 1 cycle.

STZ – Store Zeros in Memory



24 zeros replace (x).

Timing. 2 cycles. With interlace: 1 cycle.

SECTION VI
OPTIONAL INSTRUCTIONS

Four categories of optional instructions are available with the H-300. The character instructions permit manipulation of individual characters within words while protecting the rest of the addressed word. The multiply/divide instructions, either by themselves or together with the floating-point instructions, increase the power of the system in scientific applications. The expanded memory instructions are included in all systems having more than 32,768 words of memory.

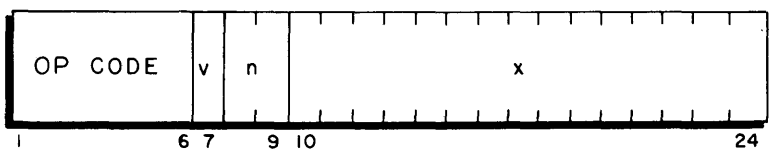
All systems include the hardware bypass feature: use of an optional instruction which is not installed in the machine causes a subsequence to a fixed memory location. The program there may identify the instruction and execute it by means of a subroutine.

CHARACTER INSTRUCTIONS

The character instructions interpret the H-300 main memory word as four alphanumeric (six-bit) characters. The low-order two bits, shown below as bits n, specify which of the four characters is to be used, counting from left to right in the addressed word.

The high-order bit of the variant character, shown below as bit v, specifies one of two available addressing modes. If the bit is zero, it specifies direct addressing; else it specifies indirect addressing.

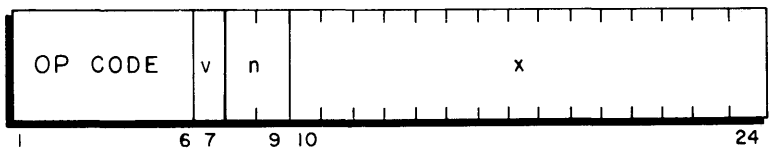
CSK – Characters Skip if Equal



(SR) are incremented by two if character n in (A) equals character n in (x) (thus the next instruction is skipped); else (SR) are incremented by one.

Timing. 2 or 3 cycles. With interlace: 1 or 2 cycles.

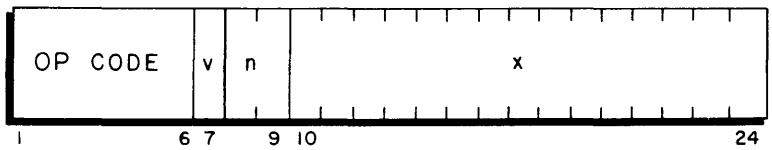
LCH – Load Character



Character n of (x) replaces character n of (A). The other characters of (A) are unchanged.

Timing. 2 cycles. With interlace: 1 cycle.

SCH — Store Character

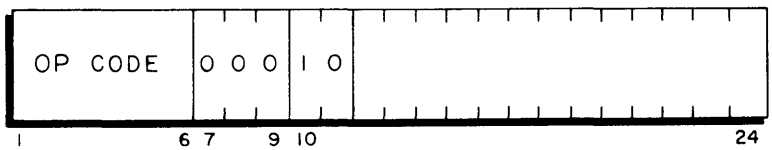


Character n of (A) replaces character n of (x). The other characters of (x) are unchanged.

Timing. 2 cycles. With interlace: 1 cycle.

EXPANDED MEMORY INSTRUCTIONS

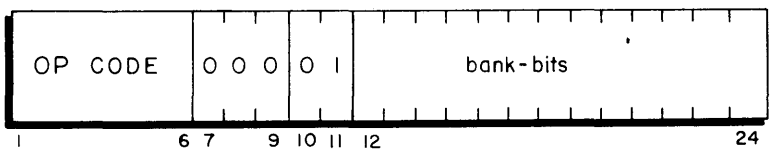
EBR – Equalize Bank Register (NAD)



The contents of the bank indicator in the sequence register replace the contents of the bank register. Thus the contents of the sequence register bank indicator and the bank register are equalized.

Timing. 1 cycle.

LBR – Load Bank Register



The contents of the bank-bit field of the instruction word replace the contents of the bank register.

Timing. 1 cycle.

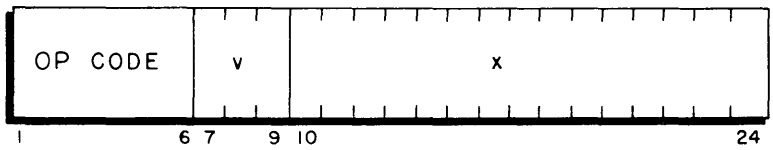
SBR – Store Bank Register

The contents of the bank register replace the low-order portion of (x). The rest of (x) is protected. The format of (x) is compatible with the Load Bank Register (LBR) instruction.

Timing. 2 cycles.

MULTIPLY/DIVIDE INSTRUCTIONS

DIV – Divide

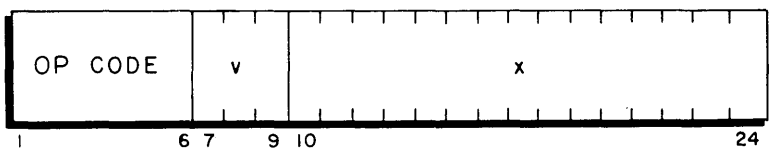


(A, B) are treated as a 48-bit dividend and divided by (x). The quotient replaces (A). The remainder replaces (B).

Indicators. Division overcapacity.

Timing. 12 cycles.

MPY – Multiply



(A) are multiplied by (x). The product replaces (A, B) taken as a 48-bit register.

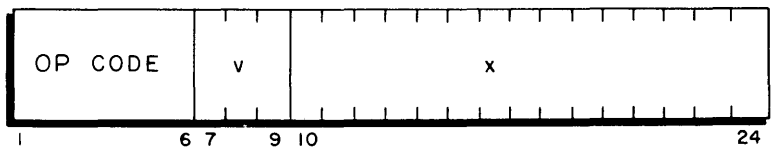
Timing. 4 cycles.

FLOATING-POINT INSTRUCTIONS

This set of instructions provides a complete floating-point repertoire for the H-300. The multiply/divide instructions are a prerequisite to the floating-point instructions.

The variable N in the timing formulas in this section represents the number of shifts required to justify the operands and/or to normalize the result.

FAD - Floating Add



(A, B) are treated as one 48-bit register, as are (x, x+1). The two operands are justified and then added together. The normalized sum replaces (A, B). An operand can be normalized by adding it to a floating-point zero.

Indicators. Exponential overflow and underflow.

Timing. $4 + \frac{N}{7}$ cycles.

FDV - Floating Divide

(A, B) are treated as one 48-bit register, as are (x, x+1). (x, x+1) are divided into (A, B). The quotient replaces (A, B). The operands are not justified and the quotient is not normalized. The remainder can be retrieved by means of the Floating Unload instruction (see page 43).

Indicators. Exponential overflow and underflow.

Timing. 26 cycles.

FMP - Floating Multiply

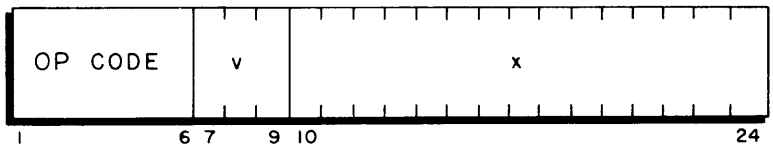
(A, B) are treated as one 48-bit register, as are (x, x+1). (A, B) are multiplied by

(x, x+1). The normalized high-order product replaces (A, B). The low-order product can be retrieved by means of the Floating Unload instruction (see below).

Indicators. Exponential overflow and underflow.

Timing. $9 + \frac{N}{7}$ cycles.

FSB – Floating Subtract

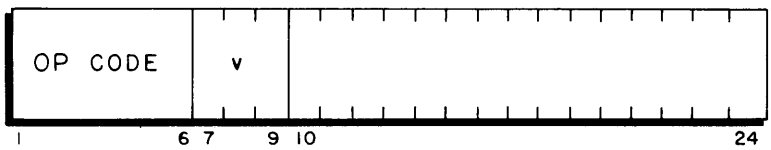


(A, B) are treated as one 48-bit register, as are (x, x+1). The two operands are justified and (x, x+1) are subtracted from (A, B). The normalized difference replaces (A, B).

Indicators. Exponential overflow and underflow.

Timing. $4 + \frac{N}{7}$ cycles.

FUL – Floating Unload



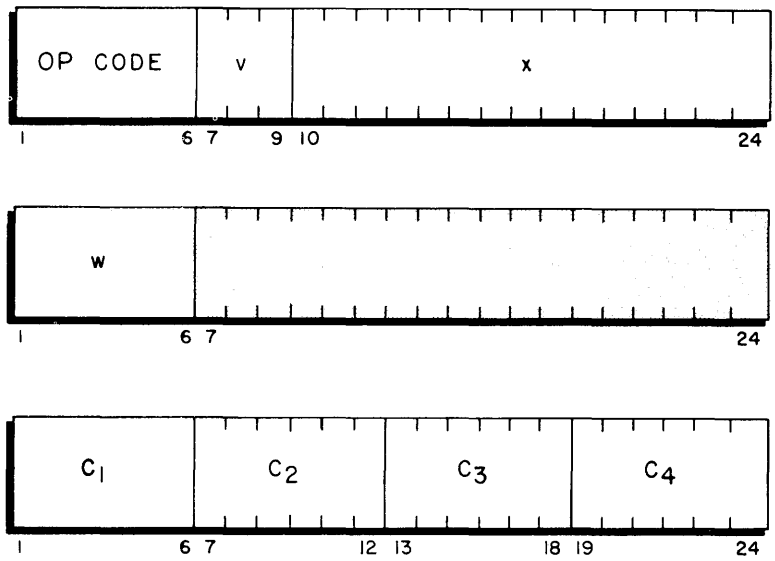
The floating-point low-order product or remainder replaces (A, B).

Timing. 4 cycles.

INPUT/OUTPUT INSTRUCTIONS, BUFFERED

The following instructions are used in conjunction with the optional read/write channels and the associated input/output traffic control described on page 8.

PCB – Peripheral Control and Branch (General Description)



(x) replace (SR) if the test(s) specified by the control characters is met; else the next sequential instruction is executed. Through the use of control characters, the PCB instruction can initiate operations such as error-card rejection on the card reader and tape rewind on magnetic tape units. Or it can test peripheral indicators such as error indicators, control unit busy indicators, and read/write channel busy indicators.

Timing. 3 + 4w cycles.

<table>
<tr><th>PARAMETER</th><th>INTERPRETATION</th></tr>
<tr><td>w</td><td>Second Word
The number of words containing control characters. Each four control characters require one word of storage. Parameter w is the number of words in this instruction, minus 2.</td></tr>
<tr><td>c_1</td><td>Third Word
Read/write channel designation. Control character one specifies the read/write channel that is to complete the data path between the main memory and the peripheral device. (The low-order five bits are the address of a current location counter.) Control character one may be one of the following octal addresses:
<table>
<tr><th>Octal Address</th><th>Read/Write Channel</th></tr>
<tr><td>11</td><td>1</td></tr>
<tr><td>12</td><td>2</td></tr>
<tr><td>13</td><td>3</td></tr>
</table></td></tr>
</table>

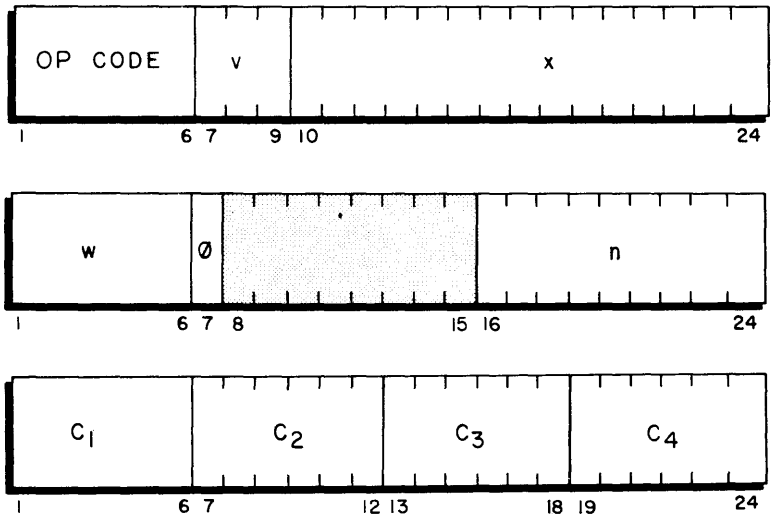
PARAMETER	INTERPRETATION
c_2	Peripheral control designation. This character designates the logical address of the peripheral control (and associated device) to be used in the operation or status test. This address is established individually at each installation and depends on the I/O trunk to which the peripheral control is permanently attached. In general, a peripheral control is designated by the number of the input/output trunk to which it is permanently attached. Any peripheral control capable of both reading and writing (e.g., the magnetic tape control) must be assigned two addresses: one for reading and one for writing. In such cases, the high-order bit of control character two must be one for input and zero for output, and the low-order three bits of the two addresses must be identical.
c_3, ...	Additional parameters. One or more two-digit control characters are used to specify status tests or control functions. See Table I for a summary of these options. The x's in the table represent information that must be supplied by the programmer, whereas the digits should be coded literally.

Table I. Summary of PCB Instruction I/O Control Characters

Test & Control Operations \ Control Characters (Octal)			1 RWC Test (00=No RWC 12=RWC2, 11=RWC1, 13=RWC3)		2 Control Unit Designation		3 Control & Test Parameters	
CARD READER	Branch if device busy		X	X	X	X	1	0
	Branch if cycle check error		X	X	X	X	4	1
	Branch if illegal punch		X	X	X	X	4	2
	Branch if device inoperable	If operable, set control unit to read Hollerith code	X	X	X	X	2	7
		If operable, set control unit to read special code	X	X	X	X	2	6
		*If operable, set control unit for direct transcription reading	X	X	X	X	2	5
		If operable, set control unit to reject cards with cycle check errors	X	X	X	X	2	1
		If operable, set control unit to reject cards with illegal punches	X	X	X	X	2	2
		If operable, set control unit to generate busy signal if cycle check error	X	X	X	X	2	3
		If operable, set control unit to generate busy signal if illegal punch	X	X	X	X	2	4
CARD PUNCH	Branch if device busy		X	X	X	X	1	0
	Branch if cycle check error		X	X	X	X	4	1
	Branch if device inoperable	If operable, set control unit to punch Hollerith code	X	X	X	X	2	7
		If operable, set control unit to punch special code	X	X	X	X	2	6
		*If operable, set control unit for direct transcription punching	X	X	X	X	2	5
		*If operable, set control unit to reject cards with echo check errors	X	X	X	X	2	1
		*If operable, set control unit to generate busy signal if error-check error	X	X	X	X	2	3
PRINTER	Branch if device busy		X	X	X	X	1	0
	Branch if print error		X	X	X	X	4	0
	Branch if end of form		X	X	X	X	0	1
	Branch if head of form		X	X	X	X	0	2
MAGNETIC TAPE	Rewind		X	X	X	X	2	Tape Drive X
	Rewind and release		X	X	X	X	2	X
	Branch if read busy		X	X	X	X	0	X
	Branch if write busy		X	X	X	X	0	X
	Branch if read/write error		X	X	X	X	4	X
	Branch if beginning of tape		X	X	X	X	6	X
	Branch if end of tape		X	X	X	X	6	X

* Optional instructions

PDT - Peripheral Data Transfer (General Description)



The PDT instruction transfers data to or from main memory starting with location x. Data transfer terminates when an external end-of-record signal occurs or when n words have been transferred, whichever occurs first. Each of the n words transferred will contain four characters, even if some zero characters are supplied to fill out the last word. The next instruction in sequence is in the first word after the control characters.

Timing. 3 + 4w cycles.

PARAMETER	INTERPRETATION
	Second Word
w	The number of words containing control characters. Each four control characters require one word of storage. Parameter w is the number of words in this instruction, minus 2.
n	The number of words in the record that is to be transferred, where $0 \leq n \leq 511$.
	Third Word
c_1	Read/write channel designation. Control character one specifies the read/write channel that is to complete the data path between the main memory and the peripheral device. (The low-order five bits are the address of a current location counter.) Control character one may be one of the following octal addresses:

Octal Address	Read/Write Channel
11	1
12	2
13	3

PARAMETER	INTERPRETATION
c_2	Peripheral control designation. This character designates the logical address of the peripheral control (and associated device) to be used in the data transfer. This address is established individually at each installation and depends on the I/O trunk to which the peripheral control is permanently attached. In general, a peripheral control is designated by the number of the input/output trunk to which it is permanently attached. Any peripheral control capable of both reading and writing (e.g., the magnetic tape control) must be assigned two addresses: one for reading and one for writing. In such cases, the high-order bit of control character two must be one for input and zero for output, and the low-order three bits of the two addresses must be identical.
c_3, ...	Additional parameters. See Table II for a summary of these options. The x's in the table represent information that must be supplied by the programmer; the digits should be coded literally. When associated with a magnetic tape operation, this character specifies direction of tape motion, odd or even parity, tape unit, and presence or absence of data transfer.

Table II. Summary of PDT Instruction I/O Control Characters

Input/Output Operation \ Control Characters (octal)	C1		C2		C3	
	RWC Designation 11 = RWC1 (no interlock) 12 = RWC2 13 = RWC3		Control Unit Designation		Additional Parameters	
Card Read	x	x	x	x		
Card Punch	x	x	x	x		
Print	x	x	x	x	See page 64.	
Tape Read Forward	x	x	x	x	6*	Tape Drive 0-7
Tape Read Reverse	x	x	x	x	2**	Tape Drive 0-7
Tape Write	x	x	x	x	2***	Tape Drive 0-7
Tape Space Forward	x	x	x	x	4	Tape Drive 0-7
Tape Backspace	x	x	x	x	0	Tape Drive 0-7

*Odd parity is assumed. If even parity is required, character should be 7.
**Odd parity is assumed. If even parity is required, character should be 3.
***Odd parity and short gap length are assumed.

SECTION VII
BUFFERED INPUT/OUTPUT OPERATIONS

This section describes the programming of those input/output devices most commonly used with the buffered input/output system, viz., the card readers, card punches, magnetic tape units, and high-speed printers. Other devices available with the Honeywell 300 include paper tape readers and punches, random access disc and drum files, communication controls, magnetic ink character recognition device controls, and a keyboard printer.

CARD READ OPERATIONS, MODEL 223

The Model 223 Card Reader and Control is an end-feed device capable of reading cards at the rate of 800 per minute (one card every 75 milliseconds). The cards are standard 12-row, 80-column (or 51-column) cards punched in Hollerith code (See Appendix B).[1] Cards are read a column at a time starting with column 1, all 12 rows in a column being read simultaneously. The card code is decoded in the card reader control and an 80-character (20-word) card image is formed in the main memory image area specified by the programmer. The card image is stored in the standard Honeywell 6-bit character code with four columns per word. Columns 1-4 make up word one, etc.

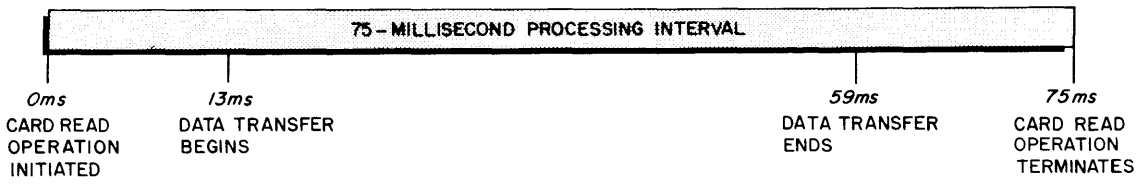


Figure 4. Model 223 Card Read Operation

Card reading is performed concurrently with central processor activities. A single card read operation can be performed during a 75-millisecond processing interval, as shown above. This time interval is determined by the mechanical operations which must be performed when a card is read. The interval begins when a card read signal activates the card reader control. Thirteen milliseconds later, initial mechanical card-feed operations are completed and information transfer begins. During the next 46 milliseconds, the card reader control delivers 20

[1] Direct transcription reading is optional. In this mode, each possible punch position is read into memory individually: those with a punch are read as 1; those without a punch are read as 0.

words to main memory, one word for each four card columns. The total time during which central processor activity is suspended due to word transfer is somewhat less than 50 microseconds. Thus, after 59 milliseconds of the processing interval has elapsed, the entire card image is stored in the main memory. The remaining time is required for terminal card-feed operations which have no effect on central processor activity.

It is important to realize that during a card read operation, central processor activity is interrupted for a total of less than 50 microseconds. In other words, over 99.9% of a 75-millisecond processing interval which is shared by a card read operation is available to the central processor for execution of other instructions and control of additional input/output operations.

Programming Considerations

1. The card reader control contains two indicators: a card read error indicator and a control unit busy indicator. If a card read error occurs, the error indicator is turned on when information transfer terminates. The busy indicator is on during the first 59 milliseconds of the card read operation.

   The status of either indicator may be tested by a PCB instruction. However, the control unit busy indicator should be tested before the card read error indicator is tested to insure that information transfer has terminated. The card read error indicator, in turn, should be tested before a subsequent card read instruction addresses the same control unit, since the error indicator is automatically reset when a new card read operation begins.

2. To maintain continuous card reading at the maximum rate of 800 cards per minute, a card read instruction must be issued before the preceding card read operation terminates. This is necessary to insure that the new card read operation will begin immediately following the preceding one.

   On a conventional clutch-operated reader, failure to time the read instructions properly severely reduces reading speed. This clutchless reader initiates the read cycle whenever it is activated instead of waiting for fixed clutch points.

   If a second read instruction is issued to the card reader during the first 59 milliseconds of the current card read operation, the central processor senses a control unit busy signal and stalls; that is, it performs no further activities until the end of the 59-millisecond period. At that point, the control unit busy signal is removed and the central processor is free to execute the second read instruction. To avoid stalling the central processor and still maintain full reading speed, a card read instruction should be issued within the last 16 milliseconds of the preceding card read operation (or from a programming standpoint, after a PCB instruction finds the control unit busy indicator off).

Use of the PCB Instruction

A Peripheral Control and Branch instruction that addresses a card reader control can initiate the following activities:

1. Test the status of the device for busy, error, or inoperable conditions.

2. Set the control unit to perform a specific control function (e.g., accept error cards, reject error cards, read Hollerith code).

If the condition tested for exists, the program branches to the location specified by the address field of the PCB instruction.

Timing. 7 cycles minimum.

Table III. Summary of Card Reader PCB Functions (Model 223)

Control Character 3 (octal)	Function
	Test Functions
10	Branch if device busy.
41	Branch if cycle check error.
42	Branch if illegal punch is detected.
	Control Functions
27	Branch if device inoperable. If operable, set control unit to read Hollerith code.
26	Branch if device inoperable. If operable, set control unit to read special code.*
**25	Branch if device inoperable. If operable, set control unit for direct transcription reading.
21	Branch if device inoperable. If operable, set control unit to reject cards on which cycle check errors are detected.
22	Branch if device inoperable. If operable, set control unit to reject cards with illegal punches.
23	Branch if device inoperable. If operable, set control unit to generate busy signal if cycle check error is detected. Busy status must be manually cleared at the card reader.
24	Branch if device inoperable. If operable, set control unit to generate busy signal if illegal punch is detected. Busy status must be manually cleared at the card reader.

*This code is shown in Appendix B.

**Optional Control Functions.

Notes

1. A PCB instruction can test the status of a read/write channel. The first I/O control character (C1) is used for this purpose. If the RWC specified by this character is busy, the program branches to the location specified in the address field of the PCB instruction. If an RWC status test is not desired, C1 must contain zeros.

2. In any program, the first instruction directed to the card reader must be PCB instruction in which control character 3 contains a 27. In effect, this instruction "initializes" card read operations.

3. Additional control characters can be written in sequence following control character 3 when more than one control function is to be performed by a single PCB instruction. If more than two control functions are performed by a single PCB instruction, the timing of the instruction increases.

Use of the PDT Instruction

This instruction initiates a card read operation and causes all information on the card to be read into the main memory image area whose initial location is specified in the address field of the instruction. Data transfer terminates when the entire card image has been transferred or when the specified number of words has been transferred. General specifications for the PDT instruction are on page 47.

Timing. 7 cycles for instruction execution.

CARD PUNCHING OPERATIONS, MODEL 224

The Model 224 is an end-feed card punch. Cards are punched a column at a time starting with column 1. All 12 rows of a column are punched simultaneously. Each six-bit character in the punch image area specified by the programmer is encoded into the corresponding card code (see Appendix B)[1] by the card punch control.

There are two models of punch available. The model 224-1 punches from 50 to 262 cards per minute, while the model 224-2 punches from 91 to 354 cards per minute. Card punching is performed concurrently with central processor activities. The length of the processing interval depends on the number of columns punched. There is a fixed clutch-engaging time at the start of the interval and a fixed card stacking and feed cycle at the end of the interval. Between these fixed intervals, the actual punching takes a fixed amount of time per column. These times and the resulting punching speed formulas are shown in Table V. Note that during a card punch operation, central processor activity is interrupted for less than 50 microseconds, so that over 99.9% of the processing interval which is shared by a card punch operation is available to the central processor for execution of other instructions and control of additional input/output operations.

There are also two models of card punch control available with the 224 punches: the model 208-1 and the model 208-2. Either punch is capable of operating with either control for normal punching operations. If either punch is to be used for punch-feed read operations, it must be connected to the model 208-2 control.

[1] Direct transcription mode punching is optional. In this mode, each possible punch position is punched individually: a 1-bit results in a punch, and a 0-bit results in no punch.

Table IV. Model 224 Card Punching Speeds

Punch	Clutch Engage	Punching Time	Stacking and Feeding	Formula
224-1	6.25 μs	12.5 μs/column	210 μs	$CPM = \frac{60,000}{216.3 + 12.5n}$
224-2	3.13 μs	6.25 μs/column	160 μs	$CPM = \frac{60,000}{163.2 + 6.25n}$
where n is the number of columns punched.				

Programming Considerations

The following points must be considered when programming card punch operations:

1. The card punch control contains two indicators: a control unit busy indicator and an echo-check indicator. The busy indicator is on during the punch operation. If an echo-check error occurred during the preceding punch operation, the echo-check indicator is turned on when information transfer in the current punch operation is completed.
2. The status of either indicator may be tested by a PCB instruction. However, the echo-check indicator should be tested after the control unit busy indicator is found to be off and before a subsequent card punch instruction addresses the same control unit.

Use of the PCB Instruction

A PCB instruction directed to the card punch control can test the status of the device or can set the control unit to perform a specific control function. If the condition tested for exists, the program branches to the location specified in the address field of the PCB instruction.

Timing. 7 cycles, minimum.

Table V. Summary of Card Punch Control Parameters

Control Character 3 (octal)	Function
	Test Functions
10	Branch if device busy.
**41	Branch if echo check error.
	Control Functions
27	Branch if device inoperable. If operable, set control unit to punch Hollerith code.
**25	Branch if device inoperable. If operable, set control unit for direct transcription punching.
**21	Branch if device inoperable. If operable, set control unit to reject cards on which echo-check errors are detected.

Table V (cont). Summary of Card Punch Control Parameters

Control Character 3 (octal)	Function
**23	Branch if device inoperable. If operable, set control unit to generate busy signal if echo-check error is detected. Busy status must be manually cleared at the card punch.
*26	Branch if device inoperable. If operable, set control unit to punch special code.

*This code is shown in Appendix B.

**Optional control functions.

Notes

1. The first I/O control character (C1) is used to test the status of a read/write channel. If an RWC status test is not desired, 61 must be zero.
2. In any program, the first instruction directed to the card punch must be a PCB instruction in which control character 3 is 27. This instruction initializes card punch operations.
3. Additional control characters can be written in sequence following control character 3 when more than one control function is to be performed by a single PCB instruction. If more than two control functions are performed by a single PCB instruction, the timing of the instruction increases.

Use of the PDT Instruction

The content of the main memory area whose initial location is specified in the address of the PDT instruction is punched into an 80-column card. The operation is terminated when a complete 80-character image has been punched or when the specified number of words has been transferred.

Timing. 7 cycles, minimum.

MAGNETIC TAPE OPERATIONS, SERIES 204B

The H-300 magnetic tape system consists of one or more tape controls, each capable of directing from one to eight tape drives. Each tape control is attached to both an input and an output line. This means that one of the tape drives attached to a tape control may be reading while another is writing simultaneously. In addition, any number of tape drives attached to a tape control may rewind simultaneously. As an optional feature, the tape controls can be modified to permit the interchange of tapes from other manufacturers with the H-300 system.

Information is recorded on magnetic tape in groups of characters called records. Since the number of characters in a record is variable, depending on the amount of information

required, the duration of the processing interval shared by a magnetic tape operation is likewise variable. This is in contrast to the fixed-length processing intervals associated with card and print operations.

Programming Considerations

Table VI summarizes the tape unit characteristics necessary to estimate the processing interval shared by a tape read/write operation, and the total time during which central processor activity is interrupted due to character transfers.

Table VI. Tape Unit Characteristics

TAPE UNIT		204B-1,2	204B-3,4	204B-5	204B-6	204B-7	
TAPE SPEED		36"/sec.	80"/sec.	120"/sec.	150"/sec.	36"/sec	
RECORDING DENSITY		200 or 556 CHAR./INCH				556 or 800 char/inch	
INTER-RECORD GAP	SHORT GAP	0.45"	0.60"	0.70"	n/a	n/a	
	LONG GAP	0.75"	0.75"	0.75"	0.75	0.75"	
* TIME TO CROSS INTER-REC. GAP	SHORT GAP	12.5ms	7.5ms	5.8ms	n/a	n/a	
	LONG GAP	20.8ms	9.4ms	6.3ms	5.0ms	20.8ms	
REWIND SPEED		108"/sec	240"/sec	360"/sec	360"/sec	108"/sec	
CHAR. RATE BETWEEN CONTROL UNIT AND MEMORY		.437μs/ch	.437μs/ch	.437μs/ch	.437μs/ch	.437μs/ch	
CHAR. RATE BETWEEN TAPE AND CONTROL UNIT	200 CPI	0.139ms/ch	0.061ms/ch	0.042ms/ch	0.033 ms/ch	556 CPI	0.050 ms/ch.
	556 CPI	0.050ms/ch.	0.022ms/ch.	0.015 ms/ch	0.012 ms/ch.	800 CPI	0.035 ms/ch.

* Cross-gap time represents time required to read past gap at full speed.

In order to estimate the duration of the processing interval shared by a tape read/write operation, three factors must be considered: the character rate between the tape and the control unit, the time required to cross the inter-record gap, and the number of characters in the record. Once these parameters have been determined, the following formula can be used to estimate the processing interval.

$$\text{PROCESSING INTERVAL (in milliseconds)} = \text{CROSS-GAP TIME} + \left(\text{NUMBER OF CHARACTERS IN RECORD} \times \text{CHARACTER RATE}\right)$$

As an example, consider the following parameters:

Tape Unit – 204B-5

Recording Density – 200 characters per inch

Number of Characters in Record – 400

Operation – Read

The read operation defined by these parameters would share a processing interval of 22.64 milliseconds:

22.64 milliseconds = 5.84ms + (400 char. X .042 ms/char.)

Within a processing interval which is shared by a magnetic tape operation, the total time during which central processor activity is suspended due to character transfers is expressed by the following formula.

TOTAL CENTRAL PROCESSOR INTERRUPT TIME (in milliseconds)	= 0.437 μs/char. X NUMBER OF CHARACTERS IN RECORD

In the example above, for instance, the total time during which central processor activity is interrupted due to character transfers is 0.174 milliseconds. In other words, 22.46 milliseconds is available for the execution of other instructions and other data transfer operations.

Tape Checking

Automatic error-detection techniques are incorporated in the H-200 tape units and controls which verify the validity of information transferred to or from tape. The presence or absence of an error condition during a read or write instruction can be tested by issuing a PCB instruction following the completion of the read or write instruction.

PARITY CHECKING: Data can be recorded on tape with either odd or even parity (as specified by the programmer). Parity checking is applied to each character transferred from the tape, and if the required bit count is not present, the error indicator is turned on.

LONGITUDINAL CHECK: A longitudinal check frame is automatically appended at the end of each record stored on tape. When a record is written on tape, the bits in each channel are counted and the bits in the check frame are set to insure an even bit count for each channel. When the same record is read from tape, the longitudinal bit count is repeated, and if each channel in the complete record (including the check frame) does not have an even bit count, the error indicator is turned on.

Note: the contents of the check frame are not transferred to the main memory.

READ AFTER WRITE: Parity and longitudinal checks are performed only when information is read from tape. The read after write feature permits the detection of errors at the time that information is written on tape. In effect, when a character is written on tape, it is automatically read to determine if the information has been recorded correctly. If any discrepancy occurs, the error indicator is turned on.

ECHO CHECK: The error indicator is turned on if the write head is not writing at least one "1" bit in each frame.

Tape Control Options

Three optional features are available with the H-300 1/2-inch tape system. Two options provide compatibility with other character-oriented systems. The first allows the H-200 tape control to recognize the end-of-file on magnetic tapes written by other systems. This is accomplished by sensing a special character called a "tape mark" which marks the end of recorded information on such tapes. The second feature equips the tape control with a translator which converts the BCD (binary coded decimal) code of such tapes into Honeywell internal code, and vice versa. Another feature is the ability to read tapes in the reverse direction and transfer the data in the normal (forward) direction into memory.

Inter-Record Gaps

The 204B-1, -2, -3, -4, and -5 magnetic tape units have the ability to read and write tape using either of two inter-record gap lengths. A "short" or a "long" gap is specified in the control field of a tape write instruction and is automatically sensed during a tape read operation. The short gap length is normally used, since more tape surface is made available for data and less cross-gap time is used. The long gap is used when processing non-Honeywell tapes, since tapes read or written by non-Honeywell equipment require additional start/stop time (and consequently a longer inter-record gap). The different gap sizes and the time required to cross them during processing are listed in Table IV.

Beginning and End of Tape

The first record on tape is recorded approximately 2.25 inches beyond the reflective spot located near the beginning of the tape. Succeeding records, normally separated by "short" inter-record gaps, are then recorded on the remainder of the tape. When the tape is positioned at the physical beginning of tape (the reflective spot), the Backspace, Rewind, and Read Reverse instructions do not move the tape or transfer data. A Rewind and Release instruction interlocks the tape unit at this point.

The physical end of tape is also marked by a reflective spot near the end of the tape. When either the physical beginning or end of tape is sensed, the corresponding indicator is turned on. Both the beginning-of-tape and the end-of-tape indicators can be tested by means of a PCB instruction.

Simultaneity and Busy Conditions

Simultaneous operations can be performed by tape units connected to the same tape control, depending upon the instructions which the designated tape units are executing. These instructions can be divided into three groups, as shown in Table VII. Simultaneity exists between groups 1, 2, and 3; there is no simultaneity within a particular group except for group 3.

A PDT instruction issued to a particular tape unit places the designated unit in a busy condition. Group-1 instructions place the input/output trunk assigned for reading in a busy condition, while group-2 instructions place the trunk assigned for writing in a busy condition. When an input/output trunk becomes busy, it remains busy until the inter-record gap is reached (in the case of group-1 instructions), until an entire record is written (in the case of writing), or until 3-1/2 inches of tape is erased (in the case of an Erase operation). While a given trunk is busy, any other instruction addressed to the same trunk will stall in the central processor until that trunk becomes not busy, at which time the instruction will be accepted by the tape control.

Table VII. Tape Unit Simultaneity and Busy Conditions

GROUP	STANDARD INSTRUCTIONS			OPTIONAL	IMPLEMENTED BY:	TEST FOR BUSY
1	READ FORWARD	SPACE FORWARD	BACK-SPACE	READ REVERSE	PERIPHERAL DATA TRANSFER	READ BUSY
2	WRITE FORWARD	ERASE				WRITE BUSY
3	REWIND / REWIND WITH INTERLOCK				PERIPHERAL CONTROL & BRANCH	N/A

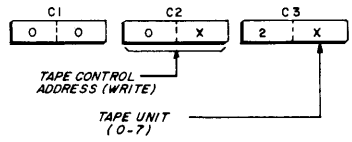
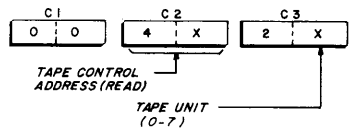
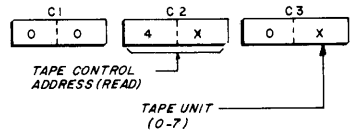
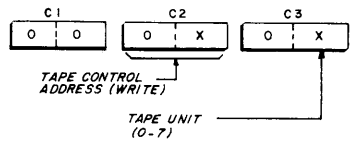
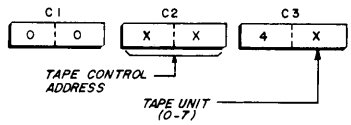
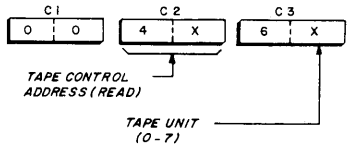
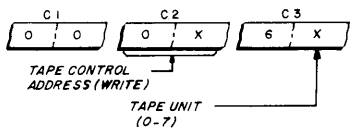
Executable Instruction Sequences

Any sequence of PDT and PCB instructions may be issued to a tape control except for the sequence of Write (or Erase) followed by a Read Forward instruction.

Use of the PCB Instruction

The test and control functions performed by a PCB instruction directed to a magnetic tape unit are defined in Table VIII. General specifications for the PCB instruction are on page 44.

Table VIII. Summary of Magnetic Tape PCB Functions (Series 204B)

FUNCTION	DESCRIPTION	I/O CONTROL CHARACTERS
REWIND	Rewind the tape on the tape drive specified in control character 3. If the tape drive is busy, branch to the location specified in the address field. This operation will not move a rewound tape.	
REWIND AND RELEASE	Same as rewind except that when rewind is completed, tape drive is disconnected from system and is not available again until operator restores ready status.	
TEST FOR READ BUSY	Branch if specified tape control or tape unit is performing a read operation.	
TEST FOR WRITE BUSY	Branch if specified tape control or tape unit is performing a write operation.	
TEST FOR READ/ WRITE ERROR	Branch if error indicator is on. The error indicator is not reset by this operation but is reset by a subsequent PDT instruction.	
TEST FOR PHYSICAL BEGINNING OF TAPE	Branch if beginning-of-tape indicator is on.	
TEST FOR PHYSICAL END OF TAPE	Branch if end-of-tape indicator is on.	

Timing. 7 cycles, minimum.

Notes.

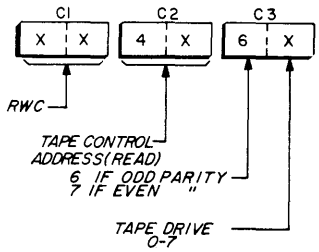
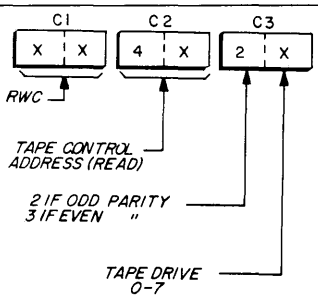
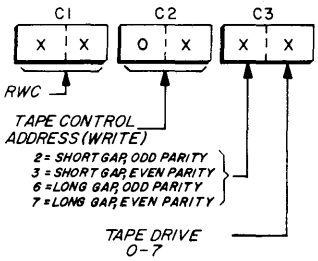
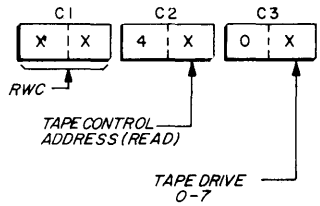
1. The first I/O control character (C1) is used to test the status of a read/write channel. If an RWC test is not desired, C1 must contain zeros.
2. A PCB instruction which tests for a read/write error condition or for beginning

or end of tape should not be issued until the completion of the read or write instruction. The completion of such a PDT instruction is indicated by testing the device for a busy condition. Therefore, the valid sequence of commands when testing for a read/write error or for beginning or end of tape is as follows: PDT (Read or Write) followed by PCB (test for read or write busy) followed by PCB (test for read/write error) or PCB (test for physical beginning or end of tape).

Use of the PDT Instruction

The magnetic tape data transfer operations that can be initiated by a PDT instruction are defined in Table IX.

Table IX. Summary of Magnetic Tape PDT Functions (Series 204B)

OPERATION	FUNCTION	I/O CONTROL CHARACTERS
READ FORWARD	Read forward one record from tape into memory area whose leftmost location is specified by the X address. Terminate the transfer when either an inter-record gap is sensed or the specified number of words is transferred.	
• READ REVERSE	Same as Read Forward except that the direction of tape movement is backward and data is read into the memory area whose initial location is X. The order of information in memory is the same as in Read Forward.	
WRITE	Transfer data from successive memory locations (X, X+1, X+2, etc.) to magnetic tape. Terminate the transfer when the specified number of words has been transferred.	
BACKSPACE	The tape drive specified in C3 backspaces over one tape record. No information is transferred as a result of this operation.	

• Optional

Timing. 7 cycles, minimum.

Notes.

1. If the number of characters read from tape is not a multiple of four, the contents of the main memory location which receives the last character read are completed with zeros.

PRINT OPERATIONS, SERIES 222

Data to be printed on a high-speed printer is stored as standard Honeywell six-bit character codes in a print image area specified by the programmer. When a print instruction is executed, the contents of the print image area are transferred character-by-character to the printer control, which then directs the actual printing of the line. The transfer is terminated by either of two conditions: (1) a complete print image has been transferred, or (2) the specified number of words has been transferred. After the line has been printed, spacing occurs as specified either in the print instruction or in a separate PDT instruction.

Printing, like other input/output operations, is performed concurrently with central processor activities. The duration of a single print operation (i.e., printing a line and spacing once after the line has been printed) and the portion of this time in which central processor activity is suspended depend upon the printer model being used. Four high-speed printers (including printer controls) are available for use with the H-300.

Models 222-1, 222-2, and 222-3

The model 222-1 printer is equipped to print 96 characters per line, model 222-2 prints 108 characters per line, and model 222-3 can print 120 characters per line (standard) or 132 characters per line (optional). These printers operate at the rate of 650 lines per minute (one line every 92 milliseconds) when the output data uses a standard set of any 51 contiguous drum characters and at the rate of 550 lines per minute (one line every 110 milliseconds) when all of the 63 characters on the drum are used.

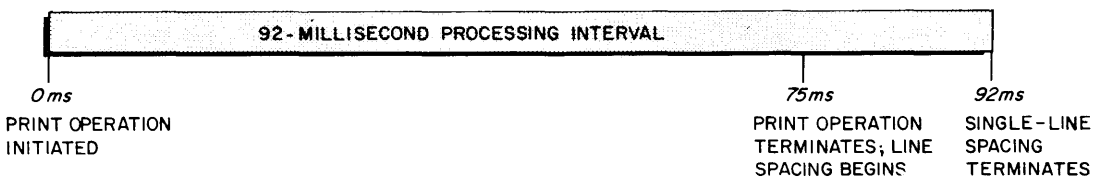


Figure 5. Print Operation for Models 222-1, 222-2, and 222-3

A processing interval of 92 milliseconds (see Figure 5) is in effect at the single-spacing speed of 650 lines per minute when the printer output uses any 51 contiguous characters on the

drum. Printing begins immediately after a print instruction activates the printer control. Line spacing begins immediately after a line has been printed (at the 75-millisecond point in the processing interval). During the first 75 milliseconds of the print operation, the printer control interrupts the central processor for a total of approximately 3 milliseconds. The central processor is therefore free to perform other activities during approximately 97% of the print operation.

A full line which uses all 63 drum characters is printed in a processing interval of 110 milliseconds (550 lines per minute). In this case, the central processor is also free for approximately 97% of the print operation. If the print record in the image area is logically less than the unit record length of the particular printer model (e.g., less than 108 characters when using the Model 222-2, etc.), the percentage of available processing time is even higher than stated above.

Model 222-4

The Model 222-4 is equipped to print 120 characters per line (standard) or 132 characters per line (optional). It operates at the rate of 950 lines per minute (one line every 63 milliseconds) when the output data uses a standard set of any 46 contiguous drum characters and at the rate of 750 lines per minute (one line every 80 milliseconds) when all of the 63 characters on the drum are used.

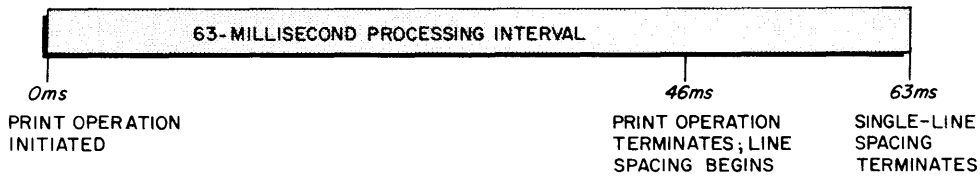


Figure 6. Print Operation for Model 222-4

A processing interval of 63 milliseconds (see Figure 6) is in effect at the single-spacing speed of 950 lines per minute when the printed output uses any contiguous 46 characters on the drum. Printing begins immediately after a print instruction activates the printer control. Line spacing begins immediately after a line has been printed (at the 46-millisecond point in the processing interval). During the first 46 milliseconds of the print operation, the printer control interrupts the central processor for a total of approximately 3 milliseconds. The central processor is therefore free to perform other activities for 95% of the print operation.

A full line which uses all 63 drum characters is printed in a processing interval of 80 milliseconds (750 lines per minute). Again, the central processor is free to perform computations and other I/O operations during 95% of the print operation. As noted previously, the

percentage of available time is even higher if the print record is logically less than the unit record length.

Programming Considerations

The following points must be considered when programming print operations:

1. The printer control contains two indicators: a control unit busy indicator and a print error indicator. The busy indicator remains on during the printing portion of the entire processing interval. If a print error is detected, line spacing is suppressed and the error indicator is turned on when printing terminates (at the end of the printing portion of the cycle). The status of either indicator can be tested by a PCB instruction. However, the print error indicator should be tested after the control unit busy indicator is found to be off and before a subsequent print instruction addresses the same control unit (a new print operation will automatically reset the error indicator).
2. Continuous printing at the rated printing speed can be achieved if a print instruction is issued before the preceding print operation terminates. However, to avoid stalling the central processor, a new print instruction should be initiated during the line-spacing portion of a print operation.
3. The performance of the system is unspecified if the programmer attempts to manipulate the contents of the print image area during the line-printing interval.

Use of the PCB Instruction

This instruction tests the status of the printer as specified in control character 3. If the condition tested exists, the program branches to the location specified by the address field of the instruction.

Timing. 7 cycles, minimum.

Table X. Summary of Printer PCB Functions (Series 222)

Control Character C3 (Octal)	Test Function
10	Branch if device busy.
40	Branch if print error.
01	Branch if channel two of the format tape was the last channel in which a hole occurred (end of form).
02	Branch if channel one of the format tape was the last channel in which a hole occurred (head of form).

Notes

The first I/O control character (C1) is used to test the status of a read/write channel. If an RWC status test is not desired, C1 must be zero.

Use of the PDT Instruction

This instruction causes the contents of the main memory area whose initial location is specified in the address field to be printed. The operation is terminated when a complete print image has been printed or when the specified number of words has been transferred.

Timing. 7 cycles, minimum.

Table XI. Summary of Printer PDT Functions (Series 222)

Control Character C3 (Binary)	Operation
00nnnn	Print, then space the number of lines specified by nnnn (0-15).
01nnnn	Print, then space to channel one of the format tape (head of form) if channel two of the format tape (end of form) is sensed; otherwise space the number of lines specified by nnnn (0-15).
11nnnn	Do not print; space the number of lines specified by nnnn (0-15).
100xxx	Print, then space to channel xxx.
101xxx	Do not print; space to channel xxx.
xxx:	
000	Channel 3
001	Channel 4
010	Channel 5
011	Channel 1 (head of form)
100	Channel 6
101	Channel 7
110	Channel 8
111	Channel 1 (head of form)

SECTION VIII
PERIPHERAL DEVICES

DIRECT INPUT/OUTPUT DEVICES

Devices that may be connected to the direct input/output channel include the Model 309 Paper Tape Reader (300 characters per second), the Model 310 Paper Tape Punch (120 characters per second), and the Model 320 Keyboard Printer (10 characters per second).

PAPER TAPE READER, MODEL 309

The Model 309 Paper Tape Reader is capable of reading up to 300 characters per second. The reader stops on a single character. Standard five-, six-, seven-, or eight-channel (plus sprocket channel) tapes may be used. Tapes may be dry, oiled, or Mylar* and may have up to 40% transmissivity. The reader can be adjusted to operate with tapes of from .0025 to .008 inches thickness. The variable tape guides may be adjusted to 11/16, 7/8, or 1 inch tape width.

PAPER TAPE PUNCH, MODEL 310

The Model 310 Paper Tape Punch is capable of punching 120 characters per second. Standard five-, six-, seven-, or eight-channel (plus sprocket channel) tapes may be used. Tapes may be dry, oiled, or Mylar. The variable tape guides may be adjusted to 11/16, 7/8, or 1 inch tape width. The supply and take up reels accommodate up to 1,000 feet of tape.

KEYBOARD PRINTER, MODEL 320

The Model 320 Keyboard Printer consists of a keyboard and a page printer which operates at the rate of 10 characters per second. The keyboard printer may be used to interrogate the contents of memory and to start and stop programs. The page printer produces a printed record of communication with the central processor.

BUFFERED INPUT/OUTPUT DEVICES

Buffered input/output devices operate semi-independently of the central processor. That is, after they have been addressed by an instruction, these devices require access to main memory only during data transfer. Data validity checks and hardware checks are performed by the control units and do not interrupt computing.

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*Mylar is a registered trademark of E. I. DuPont de Nemours and Co., Inc.

The buffered input/output devices are used with one or more read/write channels, as described in Section II. Generally, each device is connected to the central processor by means of its own control unit.[1] Any configuration of peripheral controls can be connected to the buffered input/output trunks according to the following rules:

1. Any trunk can be connected to an input control.
2. Any trunk can be connected to an output control.
3. Two trunks must be connected to any control that is used for both input and output (e.g., a magnetic tape control).

The trunks are the half-duplex type, each capable of both input and output but not both simultaneously.

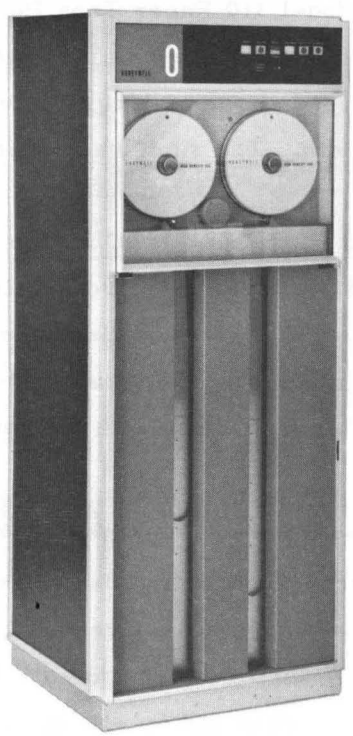
MAGNETIC TAPE UNIT, SERIES 204

Magnetic tape (and its associated tape control) provides compact storage and high-speed data transfer in response to programmed instructions. It is used for high-speed input of programs and data files, for temporary storage of intermediate computations, and for storage of output. The 1/2-inch and the 3/4-inch tape units are summarized in the following tables. Detailed programming considerations for the 1/2-inch tape units are presented in Section VII.

Operating Characteristics

A magnetic tape unit operates in the following manner:

1. A programmed instruction prepares the tape unit to transfer or receive data. The instruction addresses a specific unit, designates the direction of transfer (read or write), and indicates the memory location at which the transfer is to begin. The magnetic tape control directs the operation from this point.
2. Data transfer proceeds until an interrecord gap is sensed on the tape or until the number of words specified by the programmer have been transferred. The transferred block of information is called a record.



[1] A notable exception is that up to eight 1/2-inch magnetic tape units can be connected to a single tape control.

Table XII. 1/2-Inch Magnetic Tape Units, Series 204B

Characteristics	Model 204B-1,2	Model 204B-3,4	Model 204B-5	Model 204B-6	Model 204B-7
Associated Tape Control	203B-1		203B-2		203B-3
Tape Speed (Inches per Second)	36	80	120	150	36
Recording Density (Frames/Inch)	200 or 556				556 or 800
Transfer Rate (Char./Sec.) 556 cpi:	19,980	44,400	66,700	83,250	800 cpi: 28,800
200 cpi:	7,200	16,000	24,000	30,000	556 cpi: 20,000
Inter-Record Gap (Inches) Short:	0.45	0.60	0.70	N/A	N/A
Long:	0.75	0.75	0.75	0.75	0.75
Cross Gap Time (Ms.) Short:	12.5	7.5	5.8	N/A	N/A
Long:	20.8	9.4	6.3	5.0	20.8
Rewind Speed (Inches/Second)	108	240	360	360	108
Checking	Frame and channel parity checks for read, and read after write.				
Programmed Operations	Read Forward, Read Backward, Space Forward, Backspace, Write, Erase, Rewind.				
Tape Type	Oxide coating on 1/2-inch Mylar* base.				
File Protection	File-protect ring and manual protect switch.				
Mechanism	Vacuum capstan.				

*Mylar is a registered trademark of E. I. DuPont de Nemours and Co., Inc.

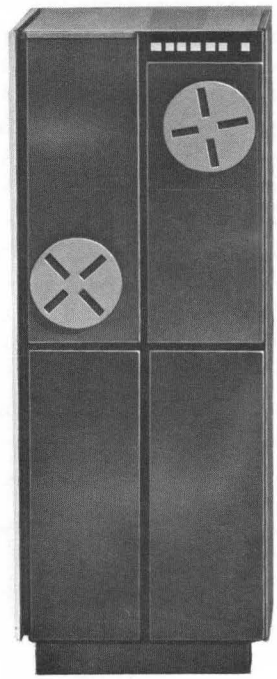
Table XIII. 3/4-Inch Magnetic Tape Units, Series 204A

Characteristics	Model 204A-1	Model 204A-2	Model 204A-3
Associated Tape Control	203A-1	203A-2	203A-3
Tape Speed (Inches per Second)	60	120	120
Recording Density (Frames/Inch)	400	400	555
Transfer Rate (Char./Sec.)	31,760	63,520	88,800
Inter-Record Gap (Inches)	0.67		

Table XIII (cont). 3/4-Inch Magnetic Tape Units, Series 204A

Characteristics	Model 204A-1	Model 204A-2	Model 204A-3
Cross Gap Time (Ms.)	11.1	5.55	5.55
Rewind Speed (Inches/Second)	180	360	360
Checking	Orthotronic control.		
Programmed Operations	Read, Write, Backspace, Rewind.		
Tape Type	Oxide coating on 3/4-inch Mylar* base.		
File Protection	File protect ring and manual protect switch.		
Mechanism	Vacuum capstan.		
*Mylar is a registered trademark of E. I. DuPont de Nemours and Co., Inc.			

PAPER TAPE READER AND CONTROL, MODEL 209



The Model 209 Paper Tape Reader and Control reads paper tape at the rate of 600 frames (characters) per second in response to programmed instructions. The control unit can be programmed to process either codes of 5 to 6 levels or codes of 7 to 8 levels. This facility minimizes the amount of central processor time required for data transfer when 5- or 6-level codes are used. Paper tape is an ideal medium for recording data that originates at locations distant from the central processor. Paper tape can be used to record data originating from a variety of source devices each having its own data transfer characteristics.

Operating Characteristics

The reader operates as follows:

1. A programmed instruction prepares the reader to read tape in the forward or reverse direction. The control directs the operation from this point.
2. Information is transferred in the transcription mode: a punch in the tape generates a binary 1 in memory and an unpunched position generates a

binary 0. Information is transferred to the control a frame at a time until a stop character is encountered or until the number of words specified by the programmer have been transferred.

3. The stop distance is less than the length of a frame. Tape can be rewound by program or run out manually.

Checking

Frame parity can be checked by the program when frames are read into memory. The reader can also be equipped to check each frame for odd or even parity and to set a program-accessible indicator if this check fails.

Table XIV. Paper Tape Reader and Control, Model 209

Tape Speed	60 inches per second
Recording Density	10 frames per inch.
Transfer Rate	600 characters per second.
Transfer Time	0.437 μs for 5- or 6-level characters; 0.875 μs for 7- or 8-level characters.
Cycle Time	1.667 ms
Cycle Available For Other Operations	99.9%.
Code	5- through 8-level. Transcription mode.
Checking	Parity read into memory for program check. Optional reader check for odd or even parity.
Programmed Operations	Read tape forward or backward until stop character or until character count, rewind, and runout.
Tape Type	5- through 8-channel 11/16", 7/8", or 1" chadded tape in rolls up to 700 feet or in strips; dry or oiled paper, Mylar*, metallic.
Mechanism	Photoelectric.

*Mylar is a registered trademark of E. I. DuPont de Nemours and Co., Inc.

PAPER TAPE PUNCH AND CONTROL, MODEL 210

The Model 210 Paper Tape Punch punches alphanumeric information at the rate of 120 frames per second. The control unit can be programmed to process either codes of 5 to 6 levels or codes of 7 to 8 levels. This facility minimizes the amount of central processor time required for data transfer when 5- or 6-level codes are used.

Operating Characteristics

The punch operates as follows:

1. A programmed instruction prepares the punch to punch the contents of an output area onto tape. The control directs the operation from this point.
2. Information is transferred in the transcription mode: a binary 1 in memory generates a punch in the tape, and a binary 0 generates no punch. Information is transferred a frame at a time until a stop character is encountered or until the number of words specified by the programmer has been transferred.
3. The stop distance is less than the length of a frame.

Checking

Data protection is achieved by means of program-generated frame parity.

Table XV. Paper Tape Punch and Control, Model 210

Tape Speed	12 inches per second.
Recording Density	10 frames per inch.
Transfer Rate	120 characters per second.
Transfer Time	0.437 μs for 5- or 6-level characters; 0.875 μs for 7- or 8-level characters.
Cycle Time	8.33 ms.
Cycle Available For Other Operations	99.9%
Code	5- through 8-level. Transcription mode.
Checking	Data protection by means of program-generated frame parity.
Programmed Operations	Punch contents of output area onto tape.
Tape Type	11/16", 7/8", or 1" non-metallic tape in reels up to 700 feet.
Mechanism	Die punch.

PRINTERS AND CONTROLS, SERIES 222

Models 222-1, -2, -3

These printers produce single-spaced copy at the rate of 650 lines per minute using a standard set of 51 characters. The three models are identical except for the number of print positions available.

Model 222-4 Printer

Model 222-4

This printer produces single-spaced copy at the rate of 950 lines per minute using a standard set of 46 characters. By means of a manual control, the drum speed can be reduced to produce 633 lines per minute where extra fine print quality is required.

Operating Characteristics (All Models)

1. A programmed instruction prepares the printer to print. The printer control directs the print operation from this point.

2. The printer control buffers the electronic speed of the central processor with the mechanical speed of the printer, limiting central processor interruptions due to data transfers to three milliseconds out of each print cycle. Data checking to insure correct transfer of information is automatic.

3. A total of 63 characters is available at each print position. Included are 26 alphabetic, 10 numeric, and 27 special characters. The characters are embossed on a drum in 63 axial rows. During print operations, the drum revolves at a constant speed, moving each row of characters past the print hammers. When the desired row passes the hammers, they are actuated and the characters are printed.

The print line contains 10 characters per inch. Manual selection of six or eight lines per inch vertical spacing is provided. Paper advance is under control of the program and/or an eight-channel paper tape loop. Form widths from 4 to 18-3/4 inches are acceptable. Up to eight clean carbon copies can be printed, depending on the thickness of the stock. The type drum can be changed by an operator in two minutes to permit the use of another type drum having more or fewer print positions per line or a different type font.

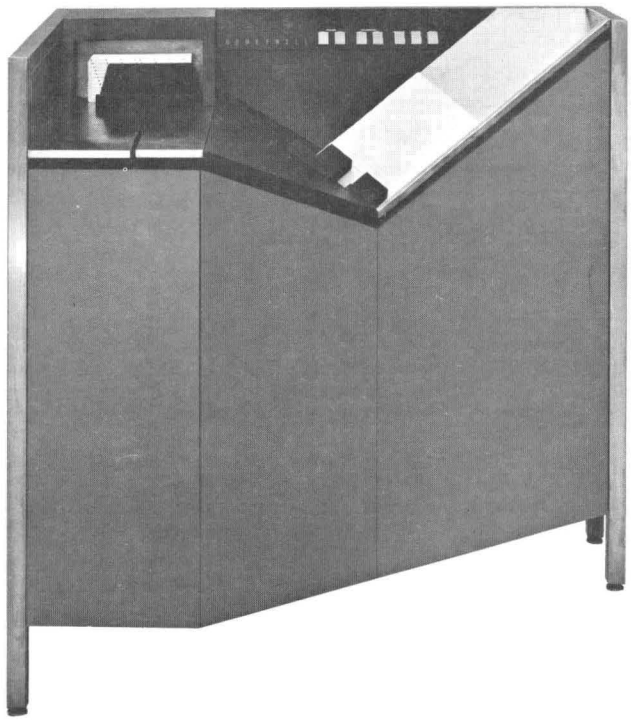
Table XVI. Printers, Series 222

Characteristics	Model 222-1	Model 222-2	Model 222-3	Model 222-4
Printing Speed (Lines per Minute)	650 (using 51 characters) 550 (using 63 characters)			950 (46 char.) 750 (63 char.)
Print Positions Per Line	96	108	120 (132 optional)	120 (132 optional)
Print Cycle	92 milliseconds			63 milliseconds
Cycle Time Available For Other Operations	89 milliseconds			60 milliseconds

Table XVI (cont). Printers, Series 222

Characteristics	Model 222-1	Model 222-2	Model 222-3	Model 222-4
Skip Speed (Inches per Second)	35			35 minimum
Vertical Spacing	Six or eight lines per inch			
Characters Per Print Position	63 (26 alphabetic, 10 numeric, 27 special symbols)			
Format Control	Paper tape loop			
Reproducing System	Hammer stroke against embossed drum			

CARD READER, MODEL 223



The Model 223 Card Reader reads standard 80-column cards at a speed of 800 per minute by an end-feed process. This is a Honeywell-developed photoelectric device employing solid-state circuitry throughout.

Operating Characteristics

The reader operates as follows:

1. Card acceleration begins immediately when the control receives a card read instruction. That is, the control does not have to wait for a clutching point in the operating cycle of the reader.
2. The card is read a column at a time by 12 photoelectric cells. Data transfer interrupts the central processor for 35 microseconds; computing may proceed during 99.9% of the 75 millisecond card read cycle.
3. The card passes to the output stacker and is stacked normally, or, if it is rejected, it is offset.

Cards may be loaded into the 3,000-card input hopper or removed from the 2,500-card output stacker without stopping the reader. Hollerith code is standard. Direct transcription is optional and is specified by program.

Checking

Accuracy of input data is monitored by a validity check and a cycle check. The validity check detects illegal punches, and the cycle check detects failure of the photo-sensing system. Either type of failure automatically sets an indicator which may be tested by the program.

Table XVII. Card Reader, Model 223

Reading Speed	800 cards per minute.
Transfer Rate	1,066 characters per second.
Cycle Time	75 ms.
Cycle Available For Other Operations	74.9 ms.
Code	Hollerith. Direct transcription is optional.
Checking	Hardware detection of illegal punches and of photo-sensing failure. Failure sets an indicator.
Programmed Operations	Read.
Card Type	80- or 51-column.
Mechanism	Photoelectric reading.

CARD PUNCHES, SERIES 224

The punching speed of 224 series depends on the number of columns punched. The range for the model 224-1 is from 50 cpm when all 80 columns are punched to 176 cpm when only the first ten columns are punched. Punching speed of the model 224-2 ranges from 91 cpm when all 80 columns are punched to 265 cpm when only the first 10 columns are punched. As the number of columns punched decreases, punching speeds increase proportionately provided that the punched columns are grouped at the left side of the card.

Operating Characteristics

The punch operates as follows:

1. A programmed instruction prepares the card punch to punch a card. The card punch control directs the punch operation from this point.
2. The card passes through a punch station. Information is punched onto the card column by column, beginning with column 1. For both models, data transfer from the central processor interrupts computing for no more than 35 microseconds times the number of (left-justified contiguous) columns punched. Thus, computing proceeds during 99.9% of the card punching cycle.
3. The card is placed in one of two output stackers. The second stacker is optional on the model 224-1.

Either model may be equipped with a punch-feed read option which permits punching of additional information onto cards already containing information.

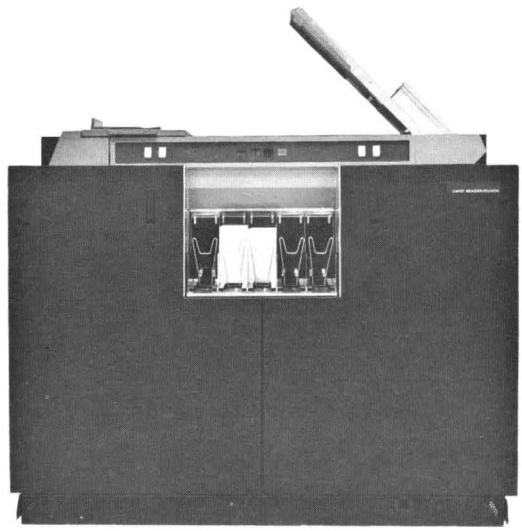
Checking

An echo check in the 224-1 senses which punch dies have been actuated and performs an automatic comparison with the data specified for punching. In the 224-2 equipped with the punch-feed read option, data protection is provided by a check for illegal card codes and a read registration check.

Table XVIII. Card Punch, Models 224-1, -2

Characteristics	Model 224-1	Model 224-2
Punching Speed	50 to 176 cpm	91 to 265 cpm
Cycle Time	335 to 1,210 ms	222.5 to 660 ms
Cycle Available For Other Operations	(cycle time) - (≤ .035 ms.)	
Code	Hollerith. Direct transcription is optional.	
Checking	Echo check.	
Programmed Operations	Punch.	
Card Type	80-column	
Mechanism	Die punch.	

CARD READER-CARD PUNCH, MODEL 227



The Model 227 Card Reader-Card Punch is a dual-purpose device. The reader portion reads standard 80-column cards at the rate of 800 cards per minute. The card punch is capable of operating simultaneously with the reader and punches standard 80-column cards at the rate of 250 cards per minute.

Operating Characteristics

The reader, which is on the right in the above illustration, operates as follows:

1. A programmed instruction prepares the card reader to read a card. The card reader control directs the read operation from this point.
2. The card passes under two read stations. The first station counts the holes in the card for checking purposes. The second station reads the data from the card into the control.

3. The second read station also counts the holes in the card. This hole count is compared with the count obtained by the first read station. If the two counts are not equal, an error indicator is set which can be tested by the program.
4. The card is ejected into one of three output stackers.

The card punch, which is on the left in the above illustration, operates as follows:

1. A programmed instruction prepares the card punch to punch a card. The card punch control directs the punch operation from this point.
2. The card passes through a punch station consisting of 80 punch dies. The card is punched as directed by information transferred from memory.
3. The card is ejected into one of three output stackers.

The punch can be equipped with a punch-feed read option which permits punching of additional information into cards already containing information.

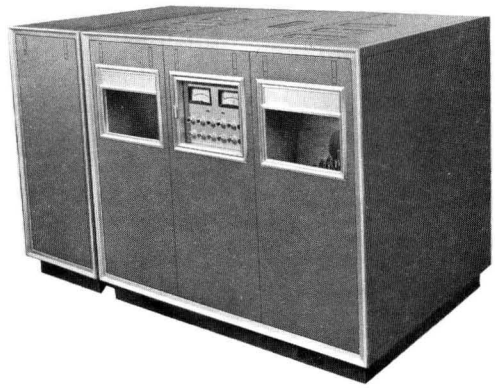
Table XIX. Card Reader- Card Punch, Model 227

Speed (Cards/Minute)	Reading: 800. Punching: 250.
Cycle Time	Reading: 75 ms. Punching: 240 ms.
Cycle Available For Computing	Reading: 74.6 ms. Punching: 239.6 ms.
Code	Hollerith. Direct transcription is optional.
Checking	Illegal punch check on reading. Hole-count check on punching.
Programmed Operations	Read, Punch, Stacker Select.
Card Type	80-column.
Mechanism	Reader: electromechanical. Punch: die punch.

MICR SORTER-READER CONTROL, MODELS 233-1, -2

Magnetic Ink Character Recognition (MICR) is a data input medium which was developed to enable data processing systems to handle such banking applications as check processing more efficiently. The MICR system permits direct entry of data into the computer without the necessity of converting it to another medium such as punched cards. Two types of MICR controls are offered. Model 233-1 is used in conjunction with an MICR sorter-reader capable of reading magnetically imprinted card or paper documents at the rate of 1600 documents per minute. The central processor stores the data, updates accounts, prepares reports, analyzes the data, and sorts the documents under program control. The model 233-2 performs the same functions in conjunction with an MICR sorter-reader capable of reading 1560 documents per minute.

RANDOM ACCESS DISC STORAGE AND CONTROL, SERIES 260



A Series 260 Random Access Disc Unit permits random access to any record in a file. (This is in direct contrast to the sequential access characteristic of magnetic tape.) Disc storage units are suited to applications requiring high-speed access and very large storage capacity. Each unit can be equipped with up to 24 magnetic discs, providing a storage capacity of up to 100.66 million characters.

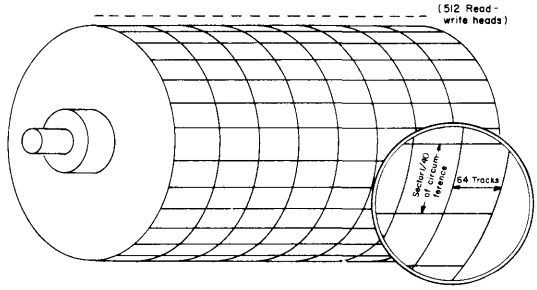
Operating Characteristics

1. A programmed instruction prepares the disc file for an information transfer. The instruction specifies an area on a disc, specifies the type of transfer (read or write), and indicates the memory location at which the transfer is to begin. The control unit directs the operation from this point.
2. Information transfer proceeds until an inter-record gap is sensed or until the number of words specified by the programmer have been transferred.

Table XX. Random Access Disc Units, Series 260

STORAGE CAPACITY	1 to 6 discs, each capable of storing 4,194,304 characters, expandable to 12, 18, or 24 discs.
HEAD POSITIONING (track to track)	60 milliseconds minimum.
LATENCY	33.3 milliseconds average.
TRANSFER RATE	23,550 to 64,300 characters per second.
DATA FORMAT	128-character records standard, longer records can be handled.
CHECKING	Parity check.
PROGRAMMED OPERATIONS	Search and read, Search and write.
CODE	Same as central processor code.
DISC SPEED	900 rpm.

RANDOM ACCESS DRUM STORAGE AND CONTROL, SERIES 270



A Model 270 Random Access Drum Unit permits random access to any record in a file. Because of its extremely high access and transfer speeds, the drum storage unit is used in systems in which speed rather than capacity is a governing factor.

Operating Characteristics

1. A programmed instruction prepares the drum for an information transfer. The instruction specifies an area on the drum, specifies the type of transfer (read or write), and indicates the memory location at which the transfer is to begin. The control unit directs the operation from this point.
2. Information transfer proceeds until an inter-record gap is sensed or until the number of words specified by the programmer have been transferred.

Table XXI. Random Access Drums, Series 270

AVERAGE ACCESS TIME	27.5 milliseconds.
TRANSFER RATE	102,000 characters per second.
STORAGE CAPACITY	2,621,440 characters per drum; up to eight drums per control.
DRUM SPEED	1200 rpm.
RECORDING DENSITY	580 bits per inch.
FILE PROTECTION	Protect/Permit switch.
DATA FORMAT	Variable-length records.
CHECKING	Parity checking.
PROGRAMMED OPERATIONS	Search and Read, Search and Write.

SINGLE-CHANNEL COMMUNICATION CONTROLS, SERIES 281

The Series 281 Communication Controls enable the central processor to receive and transmit data over a single toll or leased-wire line. The operations performed by the control include establishing synchronization with the remote equipment, controlling the flow of data between the central processor and the remote equipment, translating the Honeywell and communications codes, and implementing parity checking. The central processor is equipped with a priority interrupt system which automatically tests for the presence of incoming data or the readiness of the communication control to transmit data.

Table XXII. Single-Channel Communication Control, Series 281

Model Number	Service & Line	To Be Used With: Data Set	Speed	Terminal	Notes
281-1A	W. U. Telex	-	66 wpm	TTY 32	Manual Dial
281-1B	TWX Prime	103A	100 wpm	TTY 33, 35	
281-1C	5-Level Telegraph	-	60-100 wpm	TTY 19, 28	Private Line Use
281-1D	8-Level Telegraph	103F	100 wpm	TTY 35	Private Line Use
281-1E	TWX Prime	103A	15 cps	IBM 1050	(1) (2)
281-1F	Voice Lines	202C-D	50 cps	GE DAT. 600	(1) (2)
281-1G	Dialed Telex	-	66 wpm	TTY 32	Automatic Dial (3)
281-1H	Voice Lines	202C-D	105 cps	DATASPEED 2	(1) (2)
281-1J	AT&T 150-Baud Line	103F	15 cps	-	Not yet available; Service approval pending
281-1K	W. U. 180-Baud Line	Type 70	14.8 cps	IBM 1050	(1) (2)
281-2A	Voice Lines	202C-D	1200/1800 bps	IBM 7701, 1013	(1) (2)
281-2B	Voice Lines	201A-B	2000/2400 bps	H-200, 300, 2200, and other computers and high-speed devices*	(1) (2)
281-2C	Voice Lines	202C-D	1200/1800 bps	DIGITRONICS D505	(1) (2)
281-2D	Voice Lines	201A-B	2000/2400 bps	IBM 7702, 1013	(1) (2)
281-2E	Voice Lines	201A-B	2000/2400 bps	DIGITRONICS D505	(1) (2)
281-2F	TELPAK A	301B	5100 cps	H-200, 300, 2200, and other computers and high-speed devices*	(1) (2)
281-3A	Voice Lines	402C	75 cps Paral. Send	DATASPEED	(1) (2)
281-4A	Voice Lines	402D	75 cps Paral. Rec.	DATASPEED	(1) (2)

*Consult Applications Engineering in each case.

[1] Parity check is available at no extra cost.

[2] Option 087 - Long Check - is available.

[3] To be available soon from Western Union.

MULTIPLE-CHANNEL COMMUNICATION CONTROL, SERIES 284

The Model 284 Communication Control enables the central processor to receive and transmit data over toll or leased-wire lines. The operations performed by the control include establishing synchronization with the remote equipment, controlling the flow of data between the central processor and the remote equipment, translating Honeywell and communications codes, and implementing parity checking. The central processor's priority interrupt system automatically tests for the presence of incoming data or the readiness of the control to transmit data. The control employs a series 285 Communication Adapter as interface between the control and each communication line. The basic control serves two communication lines. The following features are available for use with it:

Feature	Description
085-1	Expansion feature. Expands 284 line-handling capability by 1 line. Up to 3 may be connected to a 284.
085-13	Expansion feature. Expands 284 line-handling capability by 13 lines.
085-61	Expansion feature. Expands 284 line-handling capability by 61 lines.
086	Parity check on reception and parity generation on transmission. One per 284.
087	Long check. One per 284. Available only with 085-13 or 085-61.

Expansion features (085-1, 085-13, 085-61) of different types cannot be attached to a single 284.

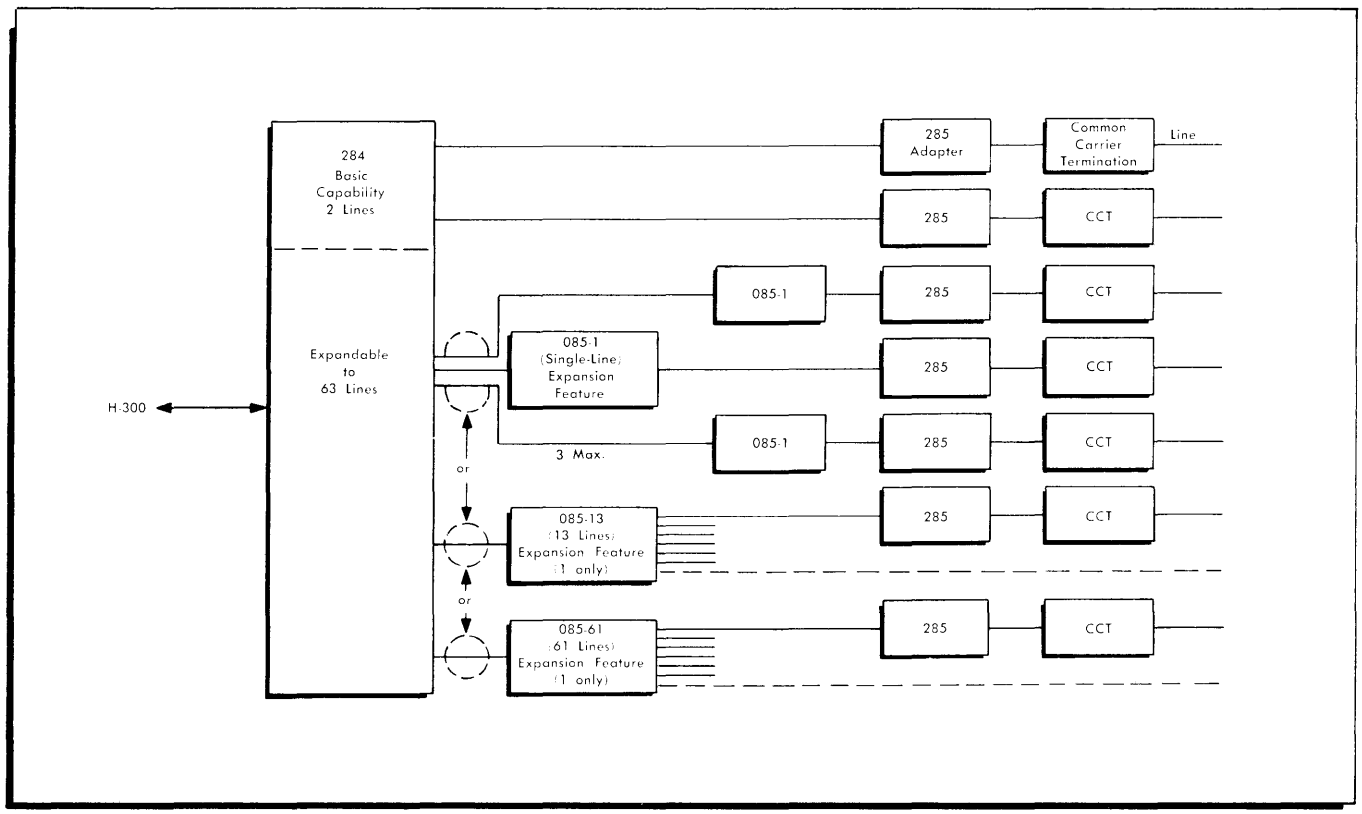


Figure 7. Multiple Communication Control, Series 284

COMMUNICATION CONTROL ADAPTER, SERIES 285

When the 284 multiple-channel control is used, each communication line requires its own series 285 adapter unit as an interface between the control and the signal requirements of the communication line.

Table XXIII. Series 285 Adapter Units

Model Number	To Be Used With				Notes
	Service & Line	Data Set	Speed	Terminal	
285-1A	W. U. Telex	-	66 wpm	TTY 32	Manual Dial
285-1B	TWX Prime	103A,	100 wpm	TTY 33, 35	
285-1C	5-Level Telegraph	-	60-100 wpm	TTY 19, 28	Private Line Use
285-1D	8-Level Telegraph	103F	100 wpm	TTY 35	Private Line Use
285-1E	TWX Prime	103A	15 cps	IBM 1050	
285-1F	Voice Lines	202C-D	50 cps	GE DAT. 600	
285-1G	Dialed Telex	-	66 wpm	TTY 32	Automatic Dial (1)
285-1H	Voice Lines	202C-D	105 cps	DATASPEED 2	
285-1J	AT&T 150-Baud Line	103F	15 cps	-	Not yet available; Service approval pending
285-1K	W. U. 180-Baud Line	Type 70	14.8 cps	IBM 1050	
285-2A	Voice Lines	202C-D	1200/1800 bps	IBM 7701, 7702, 1013	
285-2B	Voice Lines	201A-B	2000/2400 bps	H-200, 300, 1200, (and other computers and high-speed devices**)	
285-2C	Voice Lines	202C-D	1200/1800 bps	DIGITRONICS D505	
285-2D	Voice Lines	201A-B	2000/2400 bps	IBM 7702, 1013	
285-2E	Voice Lines	201A-B	2000/2400 bps	DIGITRONICS D505	
285-3A	Voice Lines	402C	75 cps Paral. Send	DATASPEED	
285-4A	Voice Lines	402D	75 cps Paral. Rec.	DATASPEED	
285-5A*	Voice Lines	801A1 801C1	-	ANY	Automatic Dialing Unit

*This is an automatic dialing unit, not an adapter unit; it will complement the 285 adapter when desired.
**Contact Applications Engineering in each case.
[1]Service to be available soon from Western Union.

FAMILY INTERFACE UNITS

The family interface (switching) units enable various combinations of Honeywell systems (H-200, H-2200, H-300) to share the same set of peripheral controls and devices and/or communications lines, to transfer data from memory to memory, and to switch various peripheral units among the peripheral control units of a single system.

MAGNETIC TAPE SWITCHING UNITS, SERIES 205

The Model 205 Magnetic Tape Switching Unit switches a set of tape units between two tape controls, allowing the corresponding two computers to share one set of tape units (see Figure 11). A set may consist of up to eight 1/2-inch tape units or up to four 3/4-inch tape units. All tape units connected to a switching unit are switched simultaneously.

As many tape units can be attached to a tape control by means of a switching unit as can be connected to the control directly (viz., eight 1/2-inch tape units or four 3/4-inch tape units).

Up to eight switching units may be attached to a 203B (1/2-inch) tape control, and up to four switching units can be attached to a 203A (3/4-inch) tape control.

Conditions for switching are as follows:

1. An H-200, 2200, or 300 must be involved.
2. Only Honeywell tape units can be switched.
3. 3/4-inch and 1/2-inch tape units cannot be intermixed on one switching unit.
4. If a switching unit is used with a 203B-1 tape control, and any one of the tape units connected to that control is not connected via the switching unit, all tape units attached to that control, either directly or by way of a switching unit, must be primary units.

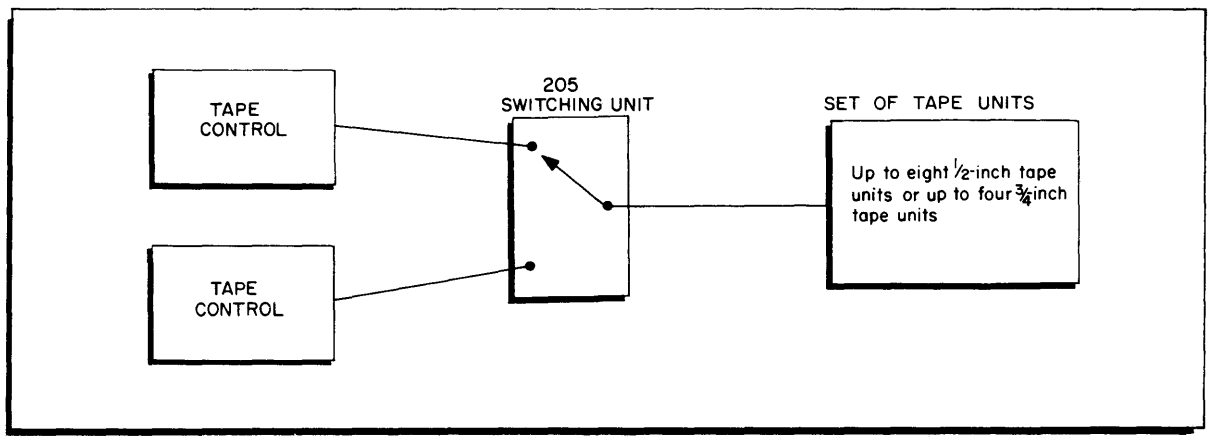
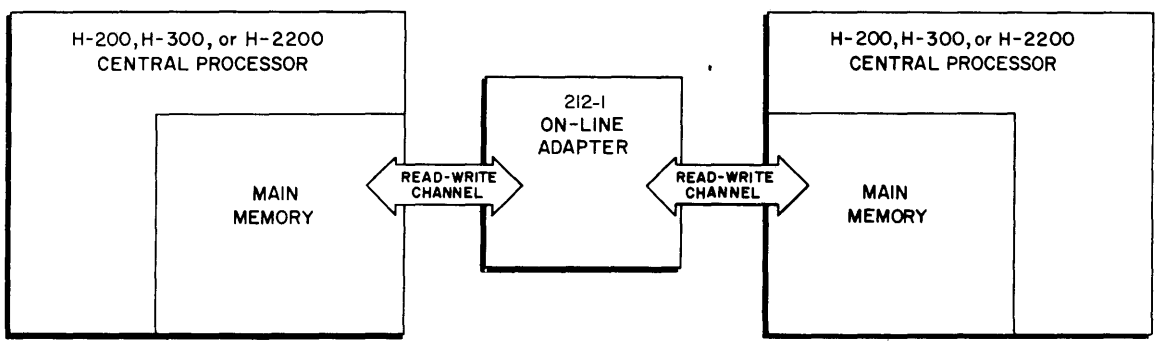


Figure 8. Magnetic Tape Switching Units, Series 205

ON-LINE ADAPTER, MODEL 212-1

The Model 212-1 On-Line Adapter provides bi-directional data transfer between two central processors which may be any combination of H-200, H-2200, and H-300 central processors. Data transfers are initiated and monitored under program control by means of standard input/output instructions. Data transfer is in one direction at a time at the rate of 167,000 characters per second. Completion of the data path between the adapter and the two central processors is by means of read/write channels, as illustrated below.



COMMUNICATION SWITCHING UNITS, SERIES 215

A Model 215-1 or -2 Communication Switching Unit switches either one group of communication lines between two model 284 Communication Controls (each of which is connected to its own H-200, H-2200, or H-300), or else it switches one such 284 between two groups of communication lines, as illustrated below, where a group contains up to eight lines.

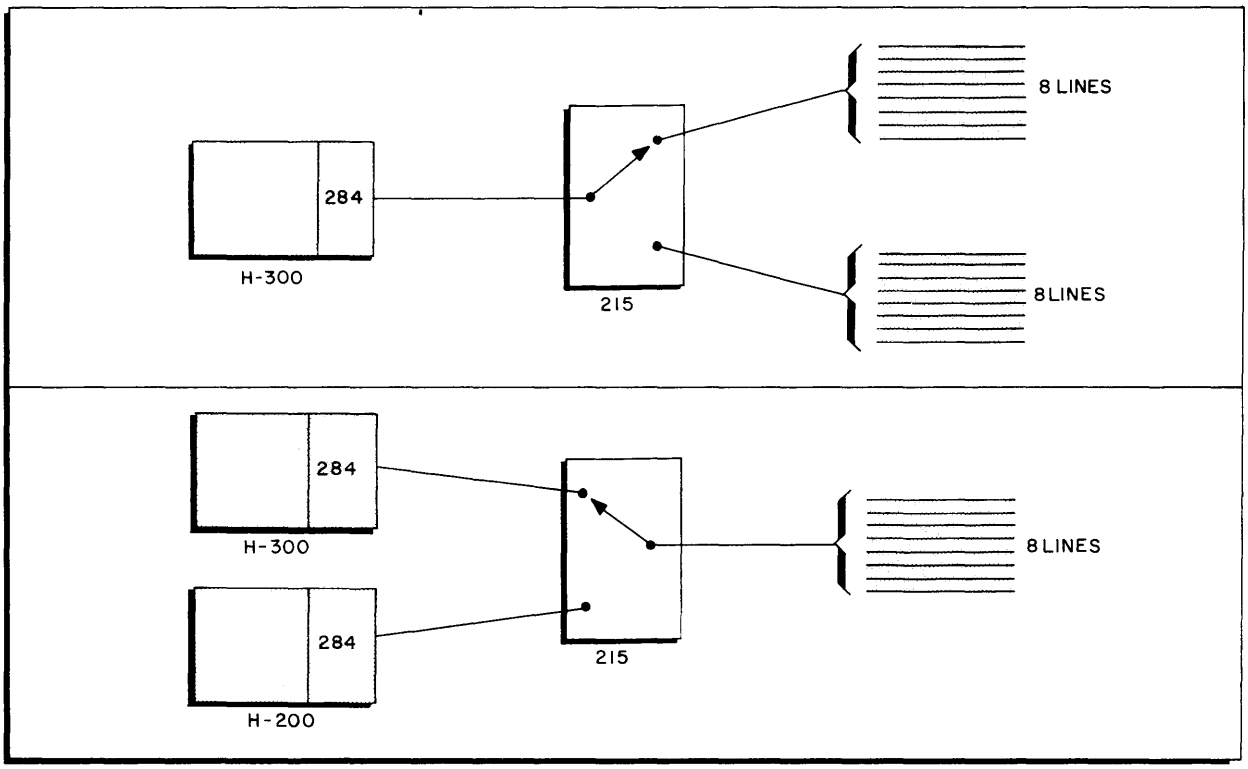


Figure 9. Communication Switching Unit, Models 215-1, -2

Each communication line requires its own series 285 adapter unit. The model 215-1 switching unit is used with the model 285-1 and -2 adapters, and the model 215-2 is used with the model 285-3 and -4 adapters.

By adding the appropriate 083 or 084 expansion features, the group switching capability can be expanded in increments of eight lines up to a total of 63 lines. All lines connected to a switching unit are switched simultaneously.

PERIPHERAL CONTROL SWITCHING UNITS, SERIES 216

The Models 216-1 and -2 Peripheral Control Switching Units allow two central processors, which may be any combination of H-200, H-2200, and H-300, to share the same set of peripheral controls and devices.

The model 216-1 switching unit accepts from one to eight standard peripheral controls (maximum of eight input/output assignments). In certain cases, attachment of a second 216-1 is possible and may be deemed practical. All units attached are switched simultaneously.

The basic model 216-2 unit also accepts from one to eight standard peripheral controls (maximum of eight input/output assignments), but up to three 053 modules can be added, each handling the switching of from one to eight standard peripheral controls. Each module and the basic unit may be switched independently, while all control units handled by any one such switching unit are switched simultaneously. In certain cases, an additional 216-2 (and 053 modules) may be added to the system for a total of eight switching units and even greater system flexibility.

APPENDIX A
TWOS-COMPLEMENT ARITHMETIC

COMPLEMENTATION

Two types of complements are commonly used for a number of given radix.[1] These are the radix-minus-1 complement and the true complement. It is the purpose of this appendix to demonstrate the distinction between the two and the use which the H-300 makes of the true complement.

TO FIND THE RADIX-MINUS-1 COMPLEMENT, SUBTRACT EACH DIGIT FROM THE RADIX MINUS 1. In the decimal system, the radix minus 1 is 9. To find the radix-minus-1 complement of decimal 44, subtract 44 from 99, giving 55. A convenient property of the binary number system is that the radix-minus-1 complement may be generated by changing all 0's to 1's and all 1's to 0's, as illustrated below.

(radix-minus-1)'s:	9 9	n_2:	100
subtract n_{10}:	4 4	invert:	⇩
9's complement:	5 5	1's complement:	011

Specifically, the radix-minus-1 complement of a binary number is called the ones complement, the radix-minus-1 complement of an octal number is called the sevens complement, and the radix-minus-1 complement of a decimal number is called the nines complement.

TO FIND THE TRUE COMPLEMENT OF A NUMBER, ADD 1 TO ITS RADIX-MINUS-1 COMPLEMENT. As demonstrated above, the radix-minus-1 complement of decimal 44 is 55; adding 1 by the rules of decimal addition gives 56, which is the true complement of decimal 44. Likewise, the true complement of binary 100 is 011 plus 1, which, by the rules of binary addition, is binary 100.

Specifically, the true complement of a binary number is called the twos complement, the true complement of an octal number is called the eights complement, and the true complement of a decimal number is called the tens complement.

TWOS-COMPLEMENT NOTATION

To clarify some essential properties of twos-complement numbers and twos-complement

[1] The radix of a number system is the quantity of permissible symbols in the system.

arithmetic, a four-bit word is used below as a frame of reference. The properties of this word that are discussed apply as well to the 24-bit Honeywell 300 word. The numbers that can be represented by a four-bit word are listed in Table A-1 below.

Table A-1. Twos-Complement Notation

Decimal Number	Binary Number	Decimal Number	(2's Complement) Binary Number
		- 8	1 0 0 0
+ 7	0 1 1 1	- 7	1 0 0 1
+ 6	0 1 1 0	- 6	1 0 1 0
+ 5	0 1 0 1	- 5	1 0 1 1
+ 4	0 1 0 0	- 4	1 1 0 0
+ 3	0 0 1 1	- 3	1 1 0 1
+ 2	0 0 1 0	- 2	1 1 1 0
+ 1	0 0 0 1	- 1	1 1 1 1
+ 0	0 0 0 0		

The table shows that positive numbers are represented in main memory in pure binary, as distinguished from twos-complement binary. The high-order bit is always zero and can be interpreted as a plus sign. The rest of the word can be interpreted directly from binary to decimal using the rules of positional notation. For example, 0111 may be interpreted as plus 7_{10}.

There is only one zero in twos-complement notation. Therefore zero ambiguity is impossible.

Negative numbers are represented in twos-complement form. The high-order bit is always 1 and can be interpreted as a minus sign. Such numbers, including the sign bit, must be recomplemented if they are to be interpreted directly from binary to decimal using the rules of positional notation. Any of the following equivalent methods may be used:

1. RECOMPLEMENT THE BINARY NUMBER (take the true complement). That is, invert all 1's to 0's and all 0's to 1's. Then add 1 to the low-order bit.
2. UNCOMPLEMENT THE BINARY NUMBER. That is, subtract 1 from the low-order bit using the rules of binary subtraction. Then invert all 1's to 0's and all 0's to 1's.
3. BINARY TRUE COMPLEMENTATION. Beginning with the low-order bit position, proceed to the high-order end of the number as follows. If the bit is 0 or the first-encountered 1, put it in the corresponding position of the result; else invert it and put it in the corresponding position of the result.
4. OCTAL TRUE COMPLEMENTATION. Beginning with the low-order octal digit, proceed to the high-order end of the number as follows. If the digit is 0, put it in the corresponding position of the result; else take the 8's complement of it, and take the 7's complement of the remaining (higher-order) digits.
5. GENERAL TRUE COMPLEMENTATION. Beginning with the low-order digit, proceed to the high-order end of the number as follows. If the digit is 0, put it in the corresponding position of the result; else take the true complement of it, and take the radix-minus-1 complement of the remaining (higher order) digits.

TWOS-COMPLEMENT ARITHMETIC

One of the advantages of twos-complement notation is that negative numbers stored in memory as twos-complement operands can be added together as full-word, unsigned integers during arithmetic operations. Yet the high-order bit of the result can be interpreted as the sign of the result, with the qualification, stated above, that a negative result must be recomplemented if it is to be interpreted directly by the rules of positional notation.

The first example in Figure A-1 illustrates subtraction as it is normally performed using decimal arithmetic. The second example shows that the same problem can be solved by adding the true complement of the subtrahend instead of by subtracting the subtrahend itself. And the third example demonstrates that the same principle applies to binary numbers. Note that, when subtraction is performed by adding the true complement, all operands must have the same number of digits. The need for this can be understood by observing that the complement of, for example, 100_2 is not identical to the complement of 0100_2.

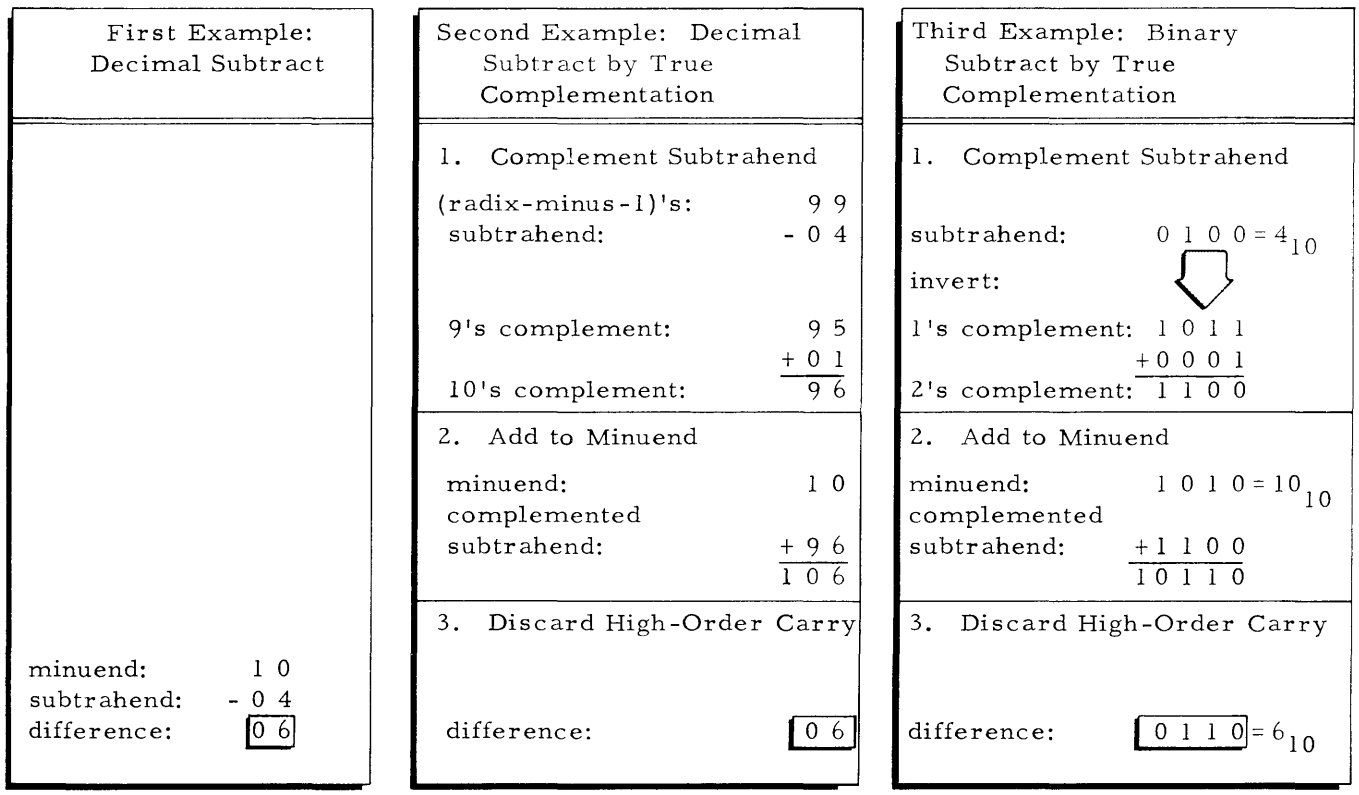


Figure A-1. Twos-Complement Arithmetic

The following examples illustrate the way in which the H-300 performs arithmetic operations. Again, a four-bit word is used for brevity.

Example 1: 7 + (-8) = -1

Assume that -8 has been loaded into the accumulator (A) and that +7 has been stored at address x. Then, using the ADD (Add to Accumulator) instruction, (A) plus (x) replace (A) as follows:

(A):	1 0 0 0 ("-8")
(x):	0 1 1 1 (+7)
new (A):	1 1 1 1 ("-1")

The result, 1111_2, is minus one according to the twos-complement collating sequence (Table A-1). The quotation marks merely indicate that the number is in its twos-complement form.

Example 2: 2 - (+3) = -1

Assume that the minuend, +2, is in the accumulator (A) and that the subtrahend, +3, has been stored at address x. Then, using the SUB (Subtract from Accumulator) instruction, the contents of x are twos-complemented:

(x):	0 0 1 1 (+3)
complemented (x):	1 1 0 1 ("-3")

The complemented subtrahend is then added to the contents of the accumulator. The sum replaces the contents of the accumulator.

(A):	0 0 1 0 (+2)
complemented (x):	1 1 0 1 ("-3")
new (A):	1 1 1 1 ("-1)

APPENDIX B

H-300 CHARACTER CODES

H-200 CHARACTER CODES

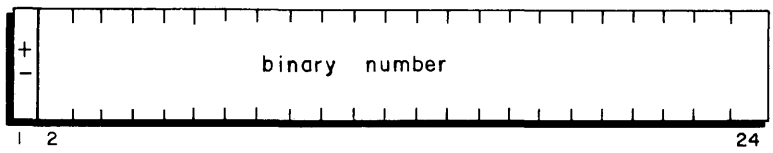
Key Punch	Card Code	Central Processor Code	Octal	High Speed Printer	Key Punch	Card Code	Central Processor Code	Octal	High Speed Printer
0	0	000000	00	0		X, 0 or X†	100000	40	-
1	1	000001	01	1	J	X, 1	100001	41	J
2	2	000010	02	2	K	X, 2	100010	42	K
3	3	000011	03	3	L	X, 3	100011	43	L
4	4	000100	04	4	M	X, 4	100100	44	M
5	5	000101	05	5	N	X, 5	100101	45	N
6	6	000110	06	6	O	X, 6	100110	46	O
7	7	000111	07	7	P	X, 7	100111	47	P
8	8	001000	10	8	Q	X, 8	101000	50	Q
9	9	001001	11	9	R	X, 9	101001	51	R
	8, 2	001010	12	'		X, 8, 2	101010	52	#
#	8, 3	001011	13	=	$	X, 8, 3	101011	53	$
@	8, 4	001100	14	:	*	X, 8, 4	101100	54	*
Space	Blank	001101	15	Blank		X, 8, 5	101101	55	"
	8, 6	001110	16	>		X, 8, 6	101110	56	≠
	8, 7	001111	17	&	-	X or X, 0 †	101111	57	!
&	R, 0 or R†	010000	20	+		8, 5	110000	60	<
A	R, 1	010001	21	A	/	0, 1	110001	61	/
B	R, 2	010010	22	B	S	0, 2	110010	62	S
C	R, 3	010011	23	C	T	0, 3	110011	63	T
D	R, 4	010100	24	D	U	0, 4	110100	64	U
E	R, 5	010101	25	E	V	0, 5	110101	65	V
F	R, 6	010110	26	F	W	0, 6	110110	66	W
G	R, 7	010111	27	G	X	0, 7	110111	67	X
H	R, 8	011000	30	H	Y	0, 8	111000	70	Y
I	R, 9	011001	31	I	Z	0, 9	111001	71	Z
	R, 8, 2	011010	32	;		0, 8, 2	111010	72	@
.	R, 8, 3	011011	33	.	,	0, 8, 3	111011	73	,
□	R, 8, 4	011100	34	)	%	0, 8, 4	111100	74	(
	R, 8, 5	011101	35	%		0, 8, 5	111101	75	$^{C}_{R}$
	R, 8, 6	011110	36	■		0, 8, 6	111110	76	□
	R or R, 0 †	011111	37	?		0, 8, 7	111111	77	¢

† Special Code. This card code-central processor code equivalency is effective when control character 26 is coded in a card read or punch PCB instruction.

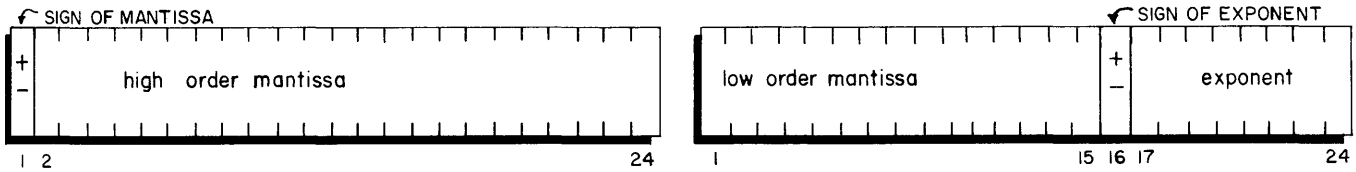
APPENDIX C

TYPES OF MACHINE WORDS

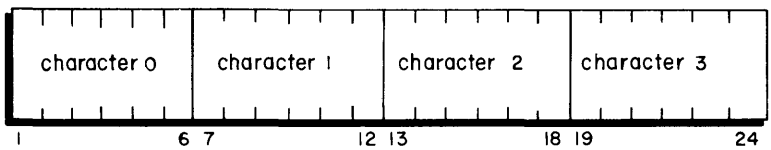
Fixed-Point Word



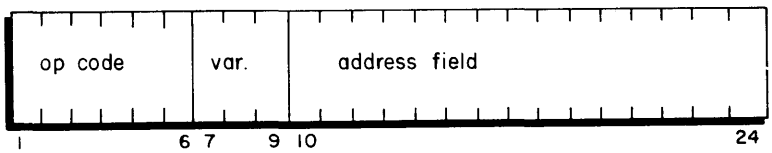
Floating-Point Word



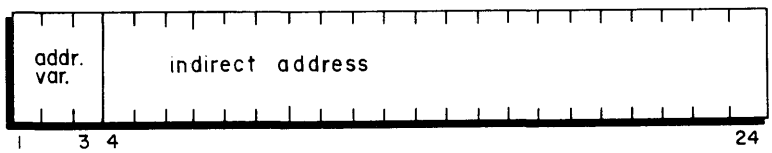
Alphanumeric Word



Instruction Word



Indirect-Address Word



APPENDIX D
OCTAL-DECIMAL INTEGER CONVERSION TABLES

The resolution (4,096) of the small octal/decimal integer conversion table below equals the range of the octal/decimal integer conversion tables following it. Used together, these tables provide an integer conversion capability of from 0 to 70 000 octal or 28,672 decimal.

Octal	Decimal
10 000	4 096
20 000	8 192
30 000	12 288
40 000	16 384
50 000	20 480
60 000	24 576
70 000	28 672

OCTAL 0000 to 0777	DECIMAL 0000 to 0511

	0	1	2	3	4	5	6	7
0000	0000	0001	0002	0003	0004	0005	0006	0007
0010	0008	0009	0010	0011	0012	0013	0014	0015
0020	0016	0017	0018	0019	0020	0021	0022	0023
0030	0024	0025	0026	0027	0028	0029	0030	0031
0040	0032	0033	0034	0035	0036	0037	0038	0039
0050	0040	0041	0042	0043	0044	0045	0046	0047
0060	0048	0049	0050	0051	0052	0053	0054	0055
0070	0056	0057	0058	0059	0060	0061	0062	0063
0100	0064	0065	0066	0067	0068	0069	0070	0071
0110	0072	0073	0074	0075	0076	0077	0078	0079
0120	0080	0081	0082	0083	0084	0085	0086	0087
0130	0088	0089	0090	0091	0092	0093	0094	0095
0140	0096	0097	0098	0099	0100	0101	0102	0103
0150	0104	0105	0106	0107	0108	0109	0110	0111
0160	0112	0113	0114	0115	0116	0117	0118	0119
0170	0120	0121	0122	0123	0124	0125	0126	0127
0200	0128	0129	0130	0131	0132	0133	0134	0135
0210	0136	0137	0138	0139	0140	0141	0142	0143
0220	0144	0145	0146	0147	0148	0149	0150	0151
0230	0152	0153	0154	0155	0156	0157	0158	0159
0240	0160	0161	0162	0163	0164	0165	0166	0167
0250	0168	0169	0170	0171	0172	0173	0174	0175
0260	0176	0177	0178	0179	0180	0181	0182	0183
0270	0184	0185	0186	0187	0188	0189	0190	0191
0300	0192	0193	0194	0195	0196	0197	0198	0199
0310	0200	0201	0202	0203	0204	0205	0206	0207
0320	0208	0209	0210	0211	0212	0213	0214	0215
0330	0216	0217	0218	0219	0220	0221	0222	0223
0340	0224	0225	0226	0227	0228	0229	0230	0231
0350	0232	0233	0234	0235	0236	0237	0238	0239
0360	0240	0241	0242	0243	0244	0245	0246	0247
0370	0248	0249	0250	0251	0252	0253	0254	0255
0400	0256	0257	0258	0259	0260	0261	0262	0263
0410	0264	0265	0266	0267	0268	0269	0270	0271
0420	0272	0273	0274	0275	0276	0277	0278	0279
0430	0280	0281	0282	0283	0284	0285	0286	0287
0440	0288	0289	0290	0291	0292	0293	0294	0295
0450	0296	0297	0298	0299	0300	0301	0302	0303
0460	0304	0305	0306	0307	0308	0309	0310	0311
0470	0312	0313	0314	0315	0316	0317	0318	0319
0500	0320	0321	0322	0323	0324	0325	0326	0327
0510	0328	0329	0330	0331	0332	0333	0334	0335
0520	0336	0337	0338	0339	0340	0341	0342	0343
0530	0344	0345	0346	0347	0348	0349	0350	0351
0540	0352	0353	0354	0355	0356	0357	0358	0359
0550	0360	0361	0362	0363	0364	0365	0366	0367
0560	0368	0369	0370	0371	0372	0373	0374	0375
0570	0376	0377	0378	0379	0380	0381	0382	0383
0600	0384	0385	0386	0387	0388	0389	0390	0391
0610	0392	0393	0394	0395	0396	0397	0398	0399
0620	0400	0401	0402	0403	0404	0405	0406	0407
0630	0408	0409	0410	0411	0412	0413	0414	0415
0640	0416	0417	0418	0419	0420	0421	0422	0423
0650	0424	0425	0426	0427	0428	0429	0430	0431
0660	0432	0433	0434	0435	0436	0437	0438	0439
0670	0440	0441	0442	0443	0444	0445	0446	0447
0700	0448	0449	0450	0451	0452	0453	0454	0455
0710	0456	0457	0458	0459	0460	0461	0462	0463
0720	0464	0465	0466	0467	0468	0469	0470	0471
0730	0472	0473	0474	0475	0476	0477	0478	0479
0740	0480	0481	0482	0483	0484	0485	0486	0487
0750	0488	0489	0490	0491	0492	0493	0494	0495
0760	0496	0497	0498	0499	0500	0501	0502	0503
0770	0504	0505	0506	0507	0508	0509	0510	0511

OCTAL 1000 to 1777	DECIMAL 0512 to 1023

	0	1	2	3	4	5	6	7
1000	0512	0513	0514	0515	0516	0517	0518	0519
1010	0520	0521	0522	0523	0524	0525	0526	0527
1020	0528	0529	0530	0531	0532	0533	0534	0535
1030	0536	0537	0538	0539	0540	0541	0542	0543
1040	0544	0545	0546	0547	0548	0549	0550	0551
1050	0552	0553	0554	0555	0556	0557	0558	0559
1060	0560	0561	0562	0563	0564	0565	0566	0567
1070	0568	0569	0570	0571	0572	0573	0574	0575
1100	0576	0577	0578	0579	0580	0581	0582	0583
1110	0584	0585	0586	0587	0588	0589	0590	0591
1120	0592	0593	0594	0595	0596	0597	0598	0599
1130	0600	0601	0602	0603	0604	0605	0606	0607
1140	0608	0609	0610	0611	0612	0613	0614	0615
1150	0616	0617	0618	0619	0620	0621	0622	0623
1160	0624	0625	0626	0627	0628	0629	0630	0631
1170	0632	0633	0634	0635	0636	0637	0638	0639
1200	0640	0641	0642	0643	0644	0645	0646	0647
1210	0648	0649	0650	0651	0652	0653	0654	0655
1220	0656	0657	0658	0659	0660	0661	0662	0663
1230	0664	0665	0666	0667	0668	0669	0670	0671
1240	0672	0673	0674	0675	0676	0677	0678	0679
1250	0680	0681	0682	0683	0684	0685	0686	0687
1260	0688	0689	0690	0691	0692	0693	0694	0695
1270	0696	0697	0698	0699	0700	0701	0702	0703
1300	0704	0705	0706	0707	0708	0709	0710	0711
1310	0712	0713	0714	0715	0716	0717	0718	0719
1320	0720	0721	0722	0723	0724	0725	0726	0727
1330	0728	0729	0730	0731	0732	0733	0734	0735
1340	0736	0737	0738	0739	0740	0741	0742	0743
1350	0744	0745	0746	0747	0748	0749	0750	0751
1360	0752	0753	0754	0755	0756	0757	0758	0759
1370	0760	0761	0762	0763	0764	0765	0766	0767
1400	0768	0769	0770	0771	0772	0773	0774	0775
1410	0776	0777	0778	0779	0780	0781	0782	0783
1420	0784	0785	0786	0787	0788	0789	0790	0791
1430	0792	0793	0794	0795	0796	0797	0798	0799
1440	0800	0801	0802	0803	0804	0805	0806	0807
1450	0808	0809	0810	0811	0812	0813	0814	0815
1460	0816	0817	0818	0819	0820	0821	0822	0823
1470	0824	0825	0826	0827	0828	0829	0830	0831
1500	0832	0833	0834	0835	0836	0837	0838	0839
1510	0840	0841	0842	0843	0844	0845	0846	0847
1520	0848	0849	0850	0851	0852	0853	0854	0855
1530	0856	0857	0858	0859	0860	0861	0862	0863
1540	0864	0865	0866	0867	0868	0869	0870	0871
1550	0872	0873	0874	0875	0876	0877	0878	0879
1560	0880	0881	0882	0883	0884	0885	0886	0887
1570	0888	0889	0890	0891	0892	0893	0894	0895
1600	0896	0897	0898	0899	0900	0901	0902	0903
1610	0904	0905	0906	0907	0908	0909	0910	0911
1620	0912	0913	0914	0915	0916	0917	0918	0919
1630	0920	0921	0922	0923	0924	0925	0926	0927
1640	0928	0929	0930	0931	0932	0933	0934	0935
1650	0936	0937	0938	0939	0940	0941	0942	0943
1660	0944	0945	0946	0947	0948	0949	0950	0951
1670	0952	0953	0954	0955	0956	0957	0958	0959
1700	0960	0961	0962	0963	0964	0965	0966	0967
1710	0968	0969	0970	0971	0972	0973	0974	0975
1720	0976	0977	0978	0979	0980	0981	0982	0983
1730	0984	0985	0986	0987	0988	0989	0990	0991
1740	0992	0993	0994	0995	0996	0997	0998	0999
1750	1000	1001	1002	1003	1004	1005	1006	1007
1760	1008	1009	1010	1011	1012	1013	1014	1015
1770	1016	1017	1018	1019	1020	1021	1022	1023

OCTAL 2000 to 2777 **DECIMAL 1024 to 1535**

	0	1	2	3	4	5	6	7
2000	1024	1025	1026	1027	1028	1029	1030	1031
2010	1032	1033	1034	1035	1036	1037	1038	1039
2020	1040	1041	1042	1043	1044	1045	1046	1047
2030	1048	1049	1050	1051	1052	1053	1054	1055
2040	1056	1057	1058	1059	1060	1061	1062	1063
2050	1064	1065	1066	1067	1068	1069	1070	1071
2060	1072	1073	1074	1075	1076	1077	1078	1079
2070	1080	1081	1082	1083	1084	1085	1086	1087
2100	1088	1089	1090	1091	1092	1093	1094	1095
2110	1096	1097	1098	1099	1100	1101	1102	1103
2120	1104	1105	1106	1107	1108	1109	1110	1111
2130	1112	1113	1114	1115	1116	1117	1118	1119
2140	1120	1121	1122	1123	1124	1125	1126	1127
2150	1128	1129	1130	1131	1132	1133	1134	1135
2160	1136	1137	1138	1139	1140	1141	1142	1143
2170	1144	1145	1146	1147	1148	1149	1150	1151
2200	1152	1153	1154	1155	1156	1157	1158	1159
2210	1160	1161	1162	1163	1164	1165	1166	1167
2220	1168	1169	1170	1171	1172	1173	1174	1175
2230	1176	1177	1178	1179	1180	1181	1182	1183
2240	1184	1185	1186	1187	1188	1189	1190	1191
2250	1192	1193	1194	1195	1196	1197	1198	1199
2260	1200	1201	1202	1203	1204	1205	1206	1207
2270	1208	1209	1210	1211	1212	1213	1214	1215
2300	1216	1217	1218	1219	1220	1221	1222	1223
2310	1224	1225	1226	1227	1228	1229	1230	1231
2320	1232	1233	1234	1235	1236	1237	1238	1239
2330	1240	1241	1242	1243	1244	1245	1246	1247
2340	1248	1249	1250	1251	1252	1253	1254	1255
2350	1256	1257	1258	1259	1260	1261	1262	1263
2360	1264	1265	1266	1267	1268	1269	1270	1271
2370	1272	1273	1274	1275	1276	1277	1278	1279
2400	1280	1281	1282	1283	1284	1285	1286	1287
2410	1288	1289	1290	1291	1292	1293	1294	1295
2420	1296	1297	1298	1299	1300	1301	1302	1303
2430	1304	1305	1306	1307	1308	1309	1310	1311
2440	1312	1313	1314	1315	1316	1317	1318	1319
2450	1320	1321	1322	1323	1324	1325	1326	1327
2460	1328	1329	1330	1331	1332	1333	1334	1335
2470	1336	1337	1338	1339	1340	1341	1342	1343
2500	1344	1345	1346	1347	1348	1349	1350	1351
2510	1352	1353	1354	1355	1356	1357	1358	1359
2520	1360	1361	1362	1363	1364	1365	1366	1367
2530	1368	1369	1370	1371	1372	1373	1374	1375
2540	1376	1377	1378	1379	1380	1381	1382	1383
2550	1384	1385	1386	1387	1388	1389	1390	1391
2560	1392	1393	1394	1395	1396	1397	1398	1399
2570	1400	1401	1402	1403	1404	1405	1406	1407
2600	1408	1409	1410	1411	1412	1413	1414	1415
2610	1416	1417	1418	1419	1420	1421	1422	1423
2620	1424	1425	1426	1427	1428	1429	1430	1431
2630	1432	1433	1434	1435	1436	1437	1438	1439
2640	1440	1441	1442	1443	1444	1445	1446	1447
2650	1448	1449	1450	1451	1452	1453	1454	1455
2660	1456	1457	1458	1459	1460	1461	1462	1463
2670	1464	1465	1466	1467	1468	1469	1470	1471
2700	1472	1473	1474	1475	1476	1477	1478	1479
2710	1480	1481	1482	1483	1484	1485	1486	1487
2720	1488	1489	1490	1491	1492	1493	1494	1495
2730	1496	1497	1498	1499	1500	1501	1502	1503
2740	1504	1505	1506	1507	1508	1509	1510	1511
2750	1512	1513	1514	1515	1516	1517	1518	1519
2760	1520	1521	1522	1523	1524	1525	1526	1527
2770	1528	1529	1530	1531	1532	1533	1534	1535

OCTAL 3000 to 3777 **DECIMAL 1536 to 2047**

	0	1	2	3	4	5	6	7
3000	1536	1537	1538	1539	1540	1541	1542	1543
3010	1544	1545	1546	1547	1548	1549	1550	1551
3020	1552	1553	1554	1555	1556	1557	1558	1559
3030	1560	1561	1562	1563	1564	1565	1566	1567
3040	1568	1569	1570	1571	1572	1573	1574	1575
3050	1576	1577	1578	1579	1580	1581	1582	1583
3060	1584	1585	1586	1587	1588	1589	1590	1591
3070	1592	1593	1594	1595	1596	1597	1598	1599
3100	1600	1601	1602	1603	1604	1605	1606	1607
3110	1608	1609	1610	1611	1612	1613	1614	1615
3120	1616	1617	1618	1619	1620	1621	1622	1623
3130	1624	1625	1626	1627	1628	1629	1630	1631
3140	1632	1633	1634	1635	1636	1637	1638	1639
3150	1640	1641	1642	1643	1644	1645	1646	1647
3160	1648	1649	1650	1651	1652	1653	1654	1655
3170	1656	1657	1658	1659	1660	1661	1662	1663
3200	1664	1665	1666	1667	1668	1669	1670	1671
3210	1672	1673	1674	1675	1676	1677	1678	1679
3220	1680	1681	1682	1683	1684	1685	1686	1687
3230	1688	1689	1690	1691	1692	1693	1694	1695
3240	1696	1697	1698	1699	1700	1701	1702	1703
3250	1704	1705	1706	1707	1708	1709	1710	1711
3260	1712	1713	1714	1715	1716	1717	1718	1719
3270	1720	1721	1722	1723	1724	1725	1726	1727
3300	1728	1729	1730	1731	1732	1733	1734	1735
3310	1736	1737	1738	1739	1740	1741	1742	1743
3320	1744	1745	1746	1747	1748	1749	1750	1751
3330	1752	1753	1754	1755	1756	1757	1758	1759
3340	1760	1761	1762	1763	1764	1765	1766	1767
3350	1768	1769	1770	1771	1772	1773	1774	1775
3360	1776	1777	1778	1779	1780	1781	1782	1783
3370	1784	1785	1786	1787	1788	1789	1790	1791
3400	1792	1793	1794	1795	1796	1797	1798	1799
3410	1800	1801	1802	1803	1804	1805	1806	1807
3420	1808	1809	1810	1811	1812	1813	1814	1815
3430	1816	1817	1818	1819	1820	1821	1822	1823
3440	1824	1825	1826	1827	1828	1829	1830	1831
3450	1832	1833	1834	1835	1836	1837	1838	1839
3460	1840	1841	1842	1843	1844	1845	1846	1847
3470	1848	1849	1850	1851	1852	1853	1854	1855
3500	1856	1857	1858	1859	1860	1861	1862	1863
3510	1864	1865	1866	1867	1868	1869	1870	1871
3520	1872	1873	1874	1875	1876	1877	1878	1879
3530	1880	1881	1882	1883	1884	1885	1886	1887
3540	1888	1889	1890	1891	1892	1893	1894	1895
3550	1896	1897	1898	1899	1900	1901	1902	1903
3560	1904	1905	1906	1907	1908	1909	1910	1911
3570	1912	1913	1914	1915	1916	1917	1918	1919
3600	1920	1921	1922	1923	1924	1925	1926	1927
3610	1928	1929	1930	1931	1932	1933	1934	1935
3620	1936	1937	1938	1939	1940	1941	1942	1943
3630	1944	1945	1946	1947	1948	1949	1950	1951
3640	1952	1953	1954	1955	1956	1957	1958	1959
3650	1960	1961	1962	1963	1964	1965	1966	1967
3660	1968	1969	1970	1971	1972	1973	1974	1975
3670	1976	1977	1978	1979	1980	1981	1982	1983
3700	1984	1985	1986	1987	1988	1989	1990	1991
3710	1992	1993	1994	1995	1996	1997	1998	1999
3720	2000	2001	2002	2003	2004	2005	2006	2007
3730	2008	2009	2010	2011	2012	2013	2014	2015
3740	2016	2017	2018	2019	2020	2021	2022	2023
3750	2024	2025	2026	2027	2028	2029	2030	2031
3760	2032	2033	2034	2035	2036	2037	2038	2039
3770	2040	2041	2042	2043	2044	2045	2046	2047

OCTAL 4000 to 4777	DECIMAL 2048 to 2559

	0	1	2	3	4	5	6	7
4000	2048	2049	2050	2051	2052	2053	2054	2055
4010	2056	2057	2058	2059	2060	2061	2062	2063
4020	2064	2065	2066	2067	2068	2069	2070	2071
4030	2072	2073	2074	2075	2076	2077	2078	2079
4040	2080	2081	2082	2083	2084	2085	2086	2087
4050	2088	2089	2090	2091	2092	2093	2094	2095
4060	2096	2097	2098	2099	2100	2101	2102	2103
4070	2104	2105	2106	2107	2108	2109	2110	2111
4100	2112	2113	2114	2115	2116	2117	2118	2119
4110	2120	2121	2122	2123	2124	2125	2126	2127
4120	2128	2129	2130	2131	2132	2133	2134	2135
4130	2136	2137	2138	2139	2140	2141	2142	2143
4140	2144	2145	2146	2147	2148	2149	2150	2151
4150	2152	2153	2154	2155	2156	2157	2158	2159
4160	2160	2161	2162	2163	2164	2165	2166	2167
4170	2168	2169	2170	2171	2172	2173	2174	2175
4200	2176	2177	2178	2179	2180	2181	2182	2183
4210	2184	2185	2186	2187	2188	2189	2190	2191
4220	2192	2193	2194	2195	2196	2197	2198	2199
4230	2200	2201	2202	2203	2204	2205	2206	2207
4240	2208	2209	2210	2211	2212	2213	2214	2215
4250	2216	2217	2218	2219	2220	2221	2222	2223
4260	2224	2225	2226	2227	2228	2229	2230	2231
4270	2232	2233	2234	2235	2236	2237	2238	2239
4300	2240	2241	2242	2243	2244	2245	2246	2247
4310	2248	2249	2250	2251	2252	2253	2254	2255
4320	2256	2257	2258	2259	2260	2261	2262	2263
4330	2264	2265	2266	2267	2268	2269	2270	2271
4340	2272	2273	2274	2275	2276	2277	2278	2279
4350	2280	2281	2282	2283	2284	2285	2286	2287
4360	2288	2289	2290	2291	2292	2293	2294	2295
4370	2296	2297	2298	2299	2300	2301	2302	2303
4400	2304	2305	2306	2307	2308	2309	2310	2311
4410	2312	2313	2314	2315	2316	2317	2318	2319
4420	2320	2321	2322	2323	2324	2325	2326	2327
4430	2328	2329	2330	2331	2332	2333	2334	2335
4440	2336	2337	2338	2339	2340	2341	2342	2343
4450	2344	2345	2346	2347	2348	2349	2350	2351
4460	2352	2353	2354	2355	2356	2357	2358	2359
4470	2360	2361	2362	2363	2364	2365	2366	2367
4500	2368	2369	2370	2371	2372	2373	2374	2375
4510	2376	2377	2378	2379	2380	2381	2382	2383
4520	2384	2385	2386	2387	2388	2389	2390	2391
4530	2392	2393	2394	2395	2396	2397	2398	2399
4540	2400	2401	2402	2403	2404	2405	2406	2407
4550	2408	2409	2410	2411	2412	2413	2414	2415
4560	2416	2417	2418	2419	2420	2421	2422	2423
4570	2424	2425	2426	2427	2428	2429	2430	2431
4600	2432	2433	2434	2435	2436	2437	2438	2439
4610	2440	2441	2442	2443	2444	2445	2446	2447
4620	2448	2449	2450	2451	2452	2453	2454	2455
4630	2456	2457	2458	2459	2460	2461	2462	2463
4640	2464	2465	2466	2467	2468	2469	2470	2471
4650	2472	2473	2474	2475	2476	2477	2478	2479
4660	2480	2481	2482	2483	2484	2485	2486	2487
4670	2488	2489	2490	2491	2492	2493	2494	2495
4700	2496	2497	2498	2499	2500	2501	2502	2503
4710	2504	2505	2506	2507	2508	2509	2510	2511
4720	2512	2513	2514	2515	2516	2517	2518	2519
4730	2520	2521	2522	2523	2524	2525	2526	2527
4740	2528	2529	2530	2531	2532	2533	2534	2535
4750	2536	2537	2538	2539	2540	2541	2542	2543
4760	2544	2545	2546	2547	2548	2549	2550	2551
4770	2552	2553	2554	2555	2556	2557	2558	2559

OCTAL 5000 to 5777	DECIMAL 2560 to 3071

	0	1	2	3	4	5	6	7
5000	2560	2561	2562	2563	2564	2565	2566	2567
5010	2568	2569	2570	2571	2572	2573	2574	2575
5020	2576	2577	2578	2579	2580	2581	2582	2583
5030	2584	2585	2586	2587	2588	2589	2590	2591
5040	2592	2593	2594	2595	2596	2597	2598	2599
5050	2600	2601	2602	2603	2604	2605	2606	2607
5060	2608	2609	2610	2611	2612	2613	2614	2615
5070	2616	2617	2618	2619	2620	2621	2622	2623
5100	2624	2625	2626	2627	2628	2629	2630	2631
5110	2632	2633	2634	2635	2636	2637	2638	2639
5120	2640	2641	2642	2643	2644	2645	2646	2647
5130	2648	2649	2650	2651	2652	2653	2654	2655
5140	2656	2657	2658	2659	2660	2661	2662	2663
5150	2664	2665	2666	2667	2668	2669	2670	2671
5160	2672	2673	2674	2675	2676	2677	2678	2679
5170	2680	2681	2682	2683	2684	2685	2686	2687
5200	2688	2689	2690	2691	2692	2693	2694	2695
5210	2696	2697	2698	2699	2700	2701	2702	2703
5220	2704	2705	2706	2707	2708	2709	2710	2711
5230	2712	2713	2714	2715	2716	2717	2718	2719
5240	2720	2721	2722	2723	2724	2725	2726	2727
5250	2728	2729	2730	2731	2732	2733	2734	2735
5260	2736	2737	2738	2739	2740	2741	2742	2743
5270	2744	2745	2746	2747	2748	2749	2750	2751
5300	2752	2753	2754	2755	2756	2757	2758	2759
5310	2760	2761	2762	2763	2764	2765	2766	2767
5320	2768	2769	2770	2771	2772	2773	2774	2775
5330	2776	2777	2778	2779	2780	2781	2782	2783
5340	2784	2785	2786	2787	2788	2789	2790	2791
5350	2792	2793	2794	2795	2796	2797	2798	2799
5360	2800	2801	2802	2803	2804	2805	2806	2807
5370	2808	2809	2810	2811	2812	2813	2814	2815
5400	2816	2817	2818	2819	2820	2821	2822	2823
5410	2824	2825	2826	2827	2828	2829	2830	2831
5420	2832	2833	2834	2835	2836	2837	2838	2839
5430	2840	2841	2842	2843	2844	2845	2846	2847
5440	2848	2849	2850	2851	2852	2853	2854	2855
5450	2856	2857	2858	2859	2860	2861	2862	2863
5460	2864	2865	2866	2867	2868	2869	2870	2871
5470	2872	2873	2874	2875	2876	2877	2878	2879
5500	2880	2881	2882	2883	2884	2885	2886	2887
5510	2888	2889	2890	2891	2892	2893	2894	2895
5520	2896	2897	2898	2899	2900	2901	2902	2903
5530	2904	2905	2906	2907	2908	2909	2910	2911
5540	2912	2913	2914	2915	2916	2917	2918	2919
5550	2920	2921	2922	2923	2924	2925	2926	2927
5560	2928	2929	2930	2931	2932	2933	2934	2935
5570	2936	2937	2938	2939	2940	2941	2942	2943
5600	2944	2945	2946	2947	2948	2949	2950	2951
5610	2952	2953	2954	2955	2956	2957	2958	2959
5620	2960	2961	2962	2963	2964	2965	2966	2967
5630	2968	2969	2970	2971	2972	2973	2974	2975
5640	2976	2977	2978	2979	2980	2981	2982	2983
5650	2984	2985	2986	2987	2988	2989	2990	2991
5660	2992	2993	2994	2995	2996	2997	2998	2999
5670	3000	3001	3002	3003	3004	3005	3006	3007
5700	3008	3009	3010	3011	3012	3013	3014	3015
5710	3016	3017	3018	3019	3020	3021	3022	3023
5720	3024	3025	3026	3027	3028	3029	3030	3031
5730	3032	3033	3034	3035	3036	3037	3038	3039
5740	3040	3041	3042	3043	3044	3045	3046	3047
5750	3048	3049	3050	3051	3052	3053	3054	3055
5760	3056	3057	3058	3059	3060	3061	3062	3063
5770	3064	3065	3066	3067	3068	3069	3070	3071

OCTAL 6000 to 6777	DECIMAL 3072 to 3583

	0	1	2	3	4	5	6	7
6000	3072	3073	3074	3075	3076	3077	3078	3079
6010	3080	3081	3082	3083	3084	3085	3086	3087
6020	3088	3089	3090	3091	3092	3093	3094	3095
6030	3096	3097	3098	3099	3100	3101	3102	3103
6040	3104	3105	3106	3107	3108	3109	3110	3111
6050	3112	3113	3114	3115	3116	3117	3118	3119
6060	3120	3121	3122	3123	3124	3125	3126	3127
6070	3128	3129	3130	3131	3132	3133	3134	3135
6100	3136	3137	3138	3139	3140	3141	3142	3143
6110	3144	3145	3146	3147	3148	3149	3150	3151
6120	3152	3153	3154	3155	3156	3157	3158	3159
6130	3160	3161	3162	3163	3164	3165	3166	3167
6140	3168	3169	3170	3171	3172	3173	3174	3175
6150	3176	3177	3178	3179	3180	3181	3182	3183
6160	3184	3185	3186	3187	3188	3189	3190	3191
6170	3192	3193	3194	3195	3196	3197	3198	3199
6200	3200	3201	3202	3203	3204	3205	3206	3207
6210	3208	3209	3210	3211	3212	3213	3214	3215
6220	3216	3217	3218	3219	3220	3221	3222	3223
6230	3224	3225	3226	3227	3228	3229	3230	3231
6240	3232	3233	3234	3235	3236	3237	3238	3239
6250	3240	3241	3242	3243	3244	3245	3246	3247
6260	3248	3249	3250	3251	3252	3253	3254	3255
6270	3256	3257	3258	3259	3260	3261	3262	3263
6300	3264	3265	3266	3267	3268	3269	3270	3271
6310	3272	3273	3274	3275	3276	3277	3278	3279
6320	3280	3281	3282	3283	3284	3285	3286	3287
6330	3288	3289	3290	3291	3292	3293	3294	3295
6340	3296	3297	3298	3299	3300	3301	3302	3303
6350	3304	3305	3306	3307	3308	3309	3310	3311
6360	3312	3313	3314	3315	3316	3317	3318	3319
6370	3320	3321	3322	3323	3324	3325	3326	3327
6400	3328	3329	3330	3331	3332	3333	3334	3335
6410	3336	3337	3338	3339	3340	3341	3342	3343
6420	3344	3345	3346	3347	3348	3349	3350	3351
6430	3352	3353	3354	3355	3356	3357	3358	3359
6440	3360	3361	3362	3363	3364	3365	3366	3367
6450	3368	3369	3370	3371	3372	3373	3374	3375
6460	3376	3377	3378	3379	3380	3381	3382	3383
6470	3384	3385	3386	3387	3388	3389	3390	3391
6500	3392	3393	3394	3395	3396	3397	3398	3399
6510	3400	3401	3402	3403	3404	3405	3406	3407
6520	3408	3409	3410	3411	3412	3413	3414	3415
6530	3416	3417	3418	3419	3420	3421	3422	3423
6540	3424	3425	3426	3427	3428	3429	3430	3431
6550	3432	3433	3434	3435	3436	3437	3438	3439
6560	3440	3441	3442	3443	3444	3445	3446	3447
6570	3448	3449	3450	3451	3452	3453	3454	3455
6600	3456	3457	3458	3459	3460	3461	3462	3463
6610	3464	3465	3466	3467	3468	3469	3470	3471
6620	3472	3473	3474	3475	3476	3477	3478	3479
6630	3480	3481	3482	3483	3484	3485	3486	3487
6640	3488	3489	3490	3491	3492	3493	3494	3495
6650	3496	3497	3498	3499	3500	3501	3502	3503
6660	3504	3505	3506	3507	3508	3509	3510	3511
6670	3512	3513	3514	3515	3516	3517	3518	3519
6700	3520	3521	3522	3523	3524	3525	3526	3527
6710	3528	3529	3530	3531	3532	3533	3534	3535
6720	3536	3537	3538	3539	3540	3541	3542	3543
6730	3544	3545	3546	3547	3548	3549	3550	3551
6740	3552	3553	3554	3555	3556	3557	3558	3559
6750	3560	3561	3562	3563	3564	3565	3566	3567
6760	3568	3569	3570	3571	3572	3573	3574	3575
6770	3576	3577	3578	3579	3580	3581	3582	3583

OCTAL 7000 to 7777	DECIMAL 3584 to 4095

	0	1	2	3	4	5	6	7
7000	3584	3585	3586	3587	3588	3589	3590	3591
7010	3592	3593	3594	3595	3596	3597	3598	3599
7020	3600	3601	3602	3603	3604	3605	3606	3607
7030	3608	3609	3610	3611	3612	3613	3614	3615
7040	3616	3617	3618	3619	3620	3621	3622	3623
7050	3624	3625	3626	3627	3628	3629	3630	3631
7060	3632	3633	3634	3635	3636	3637	3638	3639
7070	3640	3641	3642	3643	3644	3645	3646	3647
7100	3648	3649	3650	3651	3652	3653	3654	3655
7110	3656	3657	3658	3659	3660	3661	3662	3663
7120	3664	3665	3666	3667	3668	3669	3670	3671
7130	3672	3673	3674	3675	3676	3677	3678	3679
7140	3680	3681	3682	3683	3684	3685	3686	3687
7150	3688	3689	3690	3691	3692	3693	3694	3695
7160	3696	3697	3698	3699	3700	3701	3702	3703
7170	3704	3705	3706	3707	3708	3709	3710	3711
7200	3712	3713	3714	3715	3716	3717	3718	3719
7210	3720	3721	3722	3723	3724	3725	3726	3727
7220	3728	3729	3730	3731	3732	3733	3734	3735
7230	3736	3737	3738	3739	3740	3741	3742	3743
7240	3744	3745	3746	3747	3748	3749	3750	3751
7250	3752	3753	3754	3755	3756	3757	3758	3759
7260	3760	3761	3762	3763	3764	3765	3766	3767
7270	3768	3769	3770	3771	3772	3773	3774	3775
7300	3776	3777	3778	3779	3780	3781	3782	3783
7310	3784	3785	3786	3787	3788	3789	3790	3791
7320	3792	3793	3794	3795	3796	3797	3798	3799
7330	3800	3801	3802	3803	3804	3805	3806	3807
7340	3808	3809	3810	3811	3812	3813	3814	3815
7350	3816	3817	3818	3819	3820	3821	3822	3823
7360	3824	3825	3826	3827	3828	3829	3830	3831
7370	3832	3833	3834	3835	3836	3837	3838	3839
7400	3840	3841	3842	3843	3844	3845	3846	3847
7410	3848	3849	3850	3851	3852	3853	3854	3855
7420	3856	3857	3858	3859	3860	3861	3862	3863
7430	3864	3865	3866	3867	3868	3869	3870	3871
7440	3872	3873	3874	3875	3876	3877	3878	3879
7450	3880	3881	3882	3883	3884	3885	3886	3887
7460	3888	3889	3890	3891	3892	3893	3894	3895
7470	3896	3897	3898	3899	3900	3901	3902	3903
7500	3904	3905	3906	3907	3908	3909	3910	3911
7510	3912	3913	3914	3915	3916	3917	3918	3919
7520	3920	3921	3922	3923	3924	3925	3926	3927
7530	3928	3929	3930	3931	3932	3933	3934	3935
7540	3936	3937	3938	3939	3940	3941	3942	3943
7550	3944	3945	3946	3947	3948	3949	3950	3951
7560	3952	3953	3954	3955	3956	3957	3958	3959
7570	3960	3961	3962	3963	3964	3965	3966	3967
7600	3968	3969	3970	3971	3972	3973	3974	3975
7610	3976	3977	3978	3979	3980	3981	3982	3983
7620	3984	3985	3986	3987	3988	3989	3990	3991
7630	3992	3993	3994	3995	3996	3997	3998	3999
7640	4000	4001	4002	4003	4004	4005	4006	4007
7650	4008	4009	4010	4011	4012	4013	4014	4015
7660	4016	4017	4018	4019	4020	4021	4022	4023
7670	4024	4025	4026	4027	4028	4029	4030	4031
7700	4032	4033	4034	4035	4036	4037	4038	4039
7710	4040	4041	4042	4043	4044	4045	4046	4047
7720	4048	4049	4050	4051	4052	4053	4054	4055
7730	4056	4057	4058	4059	4060	4061	4062	4063
7740	4064	4065	4066	4067	4068	4069	4070	4071
7750	4072	4073	4074	4075	4076	4077	4078	4079
7760	4080	4081	4082	4083	4084	4085	4086	4087
7770	4088	4089	4090	4091	4092	4093	4094	4095

APPENDIX E
OCTAL-DECIMAL FRACTION CONVERSION TABLES

The octal/decimal fraction conversion table is in two parts. The first part lists three octal digits of precision. The second part lists six octal digits of precision, the first three of which are always zero. Used together, these tables provide a fraction conversion capability of six digits.

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000	.000000	.100	.125000	.200	.250000	.300	.375000
.001	.001953	.101	.126953	.201	.251953	.301	.376953
.002	.003906	.102	.128906	.202	.253906	.302	.378906
.003	.005859	.103	.130859	.203	.255859	.303	.380859
.004	.007812	.104	.132812	.204	.257812	.304	.382812
.005	.009765	.105	.134765	.205	.259765	.305	.384765
.006	.011718	.106	.136718	.206	.261718	.306	.386718
.007	.013671	.107	.138671	.207	.263671	.307	.388671
.010	.015625	.110	.140625	.210	.265625	.310	.390625
.011	.017578	.111	.142578	.211	.267578	.311	.392578
.012	.019531	.112	.144531	.212	.269531	.312	.394531
.013	.021484	.113	.146484	.213	.271484	.313	.396484
.014	.023437	.114	.148437	.214	.273437	.314	.398437
.015	.025390	.115	.150390	.215	.275390	.315	.400390
.016	.027343	.116	.152343	.216	.277343	.316	.402343
.017	.029296	.117	.154296	.217	.279296	.317	.404296
.020	.031250	.120	.156250	.220	.281250	.320	.406250
.021	.033203	.121	.158203	.221	.283203	.321	.408203
.022	.035156	.122	.160156	.222	.285156	.322	.410156
.023	.037109	.123	.162109	.223	.287109	.323	.412109
.024	.039062	.124	.164062	.224	.289062	.324	.414062
.025	.041015	.125	.166015	.225	.291015	.325	.416015
.026	.042968	.126	.167968	.226	.292968	.326	.417968
.027	.044921	.127	.169921	.227	.294921	.327	.419921
.030	.046875	.130	.171875	.230	.296875	.330	.421875
.031	.048828	.131	.173828	.231	.298828	.331	.423828
.032	.050781	.132	.175781	.232	.300781	.332	.425781
.033	.052734	.133	.177734	.233	.302734	.333	.427734
.034	.054687	.134	.179687	.234	.304687	.334	.429687
.035	.056640	.135	.181640	.235	.306640	.335	.431640
.036	.058593	.136	.183593	.236	.308593	.336	.433593
.037	.060546	.137	.185546	.237	.310546	.337	.435546
.040	.062500	.140	.187500	.240	.312500	.340	.437500
.041	.064453	.141	.189453	.241	.314453	.341	.439453
.042	.066406	.142	.191406	.242	.316406	.342	.441406
.043	.068359	.143	.193359	.243	.318359	.343	.443359
.044	.070312	.144	.195312	.244	.320312	.344	.445312
.045	.072265	.145	.197265	.245	.322265	.345	.447265
.046	.074218	.146	.199218	.246	.324218	.346	.449218
.047	.076171	.147	.201171	.247	.326171	.347	.451171
.050	.078125	.150	.203125	.250	.328125	.350	.453125
.051	.080078	.151	.205078	.251	.330078	.351	.455078
.052	.082031	.152	.207031	.252	.332031	.352	.457031
.053	.083984	.153	.208984	.253	.333984	.353	.458984
.054	.085937	.154	.210937	.254	.335937	.354	.460937
.055	.087890	.155	.212890	.255	.337890	.355	.462890
.056	.089843	.156	.214843	.256	.339843	.356	.464843
.057	.091796	.157	.216796	.257	.341796	.357	.466796
.060	.093750	.160	.218750	.260	.343750	.360	.468750
.061	.095703	.161	.220703	.261	.345703	.361	.470703
.062	.097656	.162	.222656	.262	.347656	.362	.472656
.063	.099609	.163	.224609	.263	.349609	.363	.474609
.064	.101562	.164	.226562	.264	.351562	.364	.476562
.065	.103515	.165	.228515	.265	.353515	.365	.478515
.066	.105468	.166	.230468	.266	.355468	.366	.480468
.067	.107421	.167	.232421	.267	.357421	.367	.482421
.070	.109375	.170	.234375	.270	.359375	.370	.484375
.071	.111328	.171	.236328	.271	.361328	.371	.486328
.072	.113281	.172	.238281	.272	.363281	.372	.488281
.073	.115234	.173	.240234	.273	.365234	.373	.490234
.074	.117187	.174	.242187	.274	.367187	.374	.492187
.075	.119140	.175	.244140	.275	.369140	.375	.494140
.076	.121093	.176	.246093	.276	.371093	.376	.496093
.077	.123046	.177	.248046	.277	.373046	.377	.498046

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000000	.000000	.000100	.000244	.000200	.000488	.000300	.000732
.000001	.000003	.000101	.000247	.000201	.000492	.000301	.000736
.000002	.000007	.000102	.000251	.000202	.000495	.000302	.000740
.000003	.000011	.000103	.000255	.000203	.000499	.000303	.000743
.000004	.000015	.000104	.000259	.000204	.000503	.000304	.000747
.000005	.000019	.000105	.000263	.000205	.000507	.000305	.000751
.000006	.000022	.000106	.000267	.000206	.000511	.000306	.000755
.000007	.000026	.000107	.000270	.000207	.000514	.000307	.000759
.000010	.000030	.000110	.000274	.000210	.000518	.000310	.000762
.000011	.000034	.000111	.000278	.000211	.000522	.000311	.000766
.000012	.000038	.000112	.000282	.000212	.000526	.000312	.000770
.000013	.000041	.000113	.000286	.000213	.000530	.000313	.000774
.000014	.000045	.000114	.000289	.000214	.000534	.000314	.000778
.000015	.000049	.000115	.000293	.000215	.000537	.000315	.000782
.000016	.000053	.000116	.000297	.000216	.000541	.000316	.000785
.000017	.000057	.000117	.000301	.000217	.000545	.000317	.000789
.000020	.000061	.000120	.000305	.000220	.000549	.000320	.000793
.000021	.000064	.000121	.000308	.000221	.000553	.000321	.000797
.000022	.000068	.000122	.000312	.000222	.000556	.000322	.000801
.000023	.000072	.000123	.000316	.000223	.000560	.000323	.000805
.000024	.000076	.000124	.000320	.000224	.000564	.000324	.000808
.000025	.000080	.000125	.000324	.000225	.000568	.000325	.000812
.000026	.000083	.000126	.000328	.000226	.000572	.000326	.000816
.000027	.000087	.000127	.000331	.000227	.000576	.000327	.000820
.000030	.000091	.000130	.000335	.000230	.000579	.000330	.000823
.000031	.000095	.000131	.000339	.000231	.000583	.000331	.000827
.000032	.000099	.000132	.000343	.000232	.000587	.000332	.000831
.000033	.000102	.000133	.000347	.000233	.000591	.000333	.000835
.000034	.000106	.000134	.000350	.000234	.000595	.000334	.000839
.000035	.000110	.000135	.000354	.000235	.000598	.000335	.000843
.000036	.000114	.000136	.000358	.000236	.000602	.000336	.000846
.000037	.000118	.000137	.000362	.000237	.000606	.000337	.000850
.000040	.000122	.000140	.000366	.000240	.000610	.000340	.000854
.000041	.000125	.000141	.000370	.000241	.000614	.000341	.000858
.000042	.000129	.000142	.000373	.000242	.000617	.000342	.000862
.000043	.000133	.000143	.000377	.000243	.000621	.000343	.000865
.000044	.000137	.000144	.000381	.000244	.000625	.000344	.000869
.000045	.000141	.000145	.000385	.000245	.000629	.000345	.000873
.000046	.000144	.000146	.000389	.000246	.000633	.000346	.000877
.000047	.000148	.000147	.000392	.000247	.000637	.000347	.000881
.000050	.000152	.000150	.000396	.000250	.000640	.000350	.000885
.000051	.000156	.000151	.000400	.000251	.000644	.000351	.000888
.000052	.000160	.000152	.000404	.000252	.000648	.000352	.000892
.000053	.000164	.000153	.000408	.000253	.000652	.000353	.000896
.000054	.000167	.000154	.000411	.000254	.000656	.000354	.000900
.000055	.000171	.000155	.000415	.000255	.000659	.000355	.000904
.000056	.000175	.000156	.000419	.000256	.000663	.000356	.000907
.000057	.000179	.000157	.000423	.000257	.000667	.000357	.000911
.000060	.000183	.000160	.000427	.000260	.000671	.000360	.000915
.000061	.000186	.000161	.000431	.000261	.000675	.000361	.000919
.000062	.000190	.000162	.000434	.000262	.000679	.000362	.000923
.000063	.000194	.000163	.000438	.000263	.000682	.000363	.000926
.000064	.000198	.000164	.000442	.000264	.000686	.000364	.000930
.000065	.000202	.000165	.000446	.000265	.000690	.000365	.000934
.000066	.000205	.000166	.000450	.000266	.000694	.000366	.000938
.000067	.000209	.000167	.000453	.000267	.000698	.000367	.000942
.000070	.000213	.000170	.000457	.000270	.000701	.000370	.000946
.000071	.000217	.000171	.000461	.000271	.000705	.000371	.000949
.000072	.000221	.000172	.000465	.000272	.000709	.000372	.000953
.000073	.000225	.000173	.000469	.000273	.000713	.000373	.000957
.000074	.000228	.000174	.000473	.000274	.000717	.000374	.000961
.000075	.000232	.000175	.000476	.000275	.000720	.000375	.000965
.000076	.000236	.000176	.000480	.000276	.000724	.000376	.000968
.000077	.000240	.000177	.000484	.000277	.000728	.000377	.000972

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000400	.000976	.000500	.001220	.000600	.001464	.000700	.001708
.000401	.000980	.000501	.001224	.000601	.001468	.000701	.001712
.000402	.000984	.000502	.001228	.000602	.001472	.000702	.001716
.000403	.000988	.000503	.001232	.000603	.001476	.000703	.001720
.000404	.000991	.000504	.001235	.000604	.001480	.000704	.001724
.000405	.000995	.000505	.001239	.000605	.001483	.000705	.001728
.000406	.000999	.000506	.001243	.000606	.001487	.000706	.001731
.000407	.001003	.000507	.001247	.000607	.001491	.000707	.001735
.000410	.001007	.000510	.001251	.000610	.001495	.000710	.001739
.000411	.001010	.000511	.001255	.000611	.001499	.000711	.001743
.000412	.001014	.000512	.001258	.000612	.001502	.000712	.001747
.000413	.001018	.000513	.001262	.000613	.001506	.000713	.001750
.000414	.001022	.000514	.001266	.000614	.001510	.000714	.001754
.000415	.001026	.000515	.001270	.000615	.001514	.000715	.001758
.000416	.001029	.000516	.001274	.000616	.001518	.000716	.001762
.000417	.001033	.000517	.001277	.000617	.001522	.000717	.001766
.000420	.001037	.000520	.001281	.000620	.001525	.000720	.001770
.000421	.001041	.000521	.001285	.000621	.001529	.000721	.001773
.000422	.001045	.000522	.001289	.000622	.001533	.000722	.001777
.000423	.001049	.000523	.001293	.000623	.001537	.000723	.001781
.000424	.001052	.000524	.001296	.000624	.001541	.000724	.001785
.000425	.001056	.000525	.001300	.000625	.001544	.000725	.001789
.000426	.001060	.000526	.001304	.000626	.001548	.000726	.001792
.000427	.001064	.000527	.001308	.000627	.001552	.000727	.001796
.000430	.001068	.000530	.001312	.000630	.001556	.000730	.001800
.000431	.001071	.000531	.001316	.000631	.001560	.000731	.001804
.000432	.001075	.000532	.001319	.000632	.001564	.000732	.001808
.000433	.001079	.000533	.001323	.000633	.001567	.000733	.001811
.000434	.001083	.000534	.001327	.000634	.001571	.000734	.001815
.000435	.001087	.000535	.001331	.000635	.001575	.000735	.001819
.000436	.001091	.000536	.001335	.000636	.001579	.000736	.001823
.000437	.001094	.000537	.001338	.000637	.001583	.000737	.001827
.000440	.001098	.000540	.001342	.000640	.001586	.000740	.001831
.000441	.001102	.000541	.001346	.000641	.001590	.000741	.001834
.000442	.001106	.000542	.001350	.000642	.001594	.000742	.001838
.000443	.001110	.000543	.001354	.000643	.001598	.000743	.001842
.000444	.001113	.000544	.001358	.000644	.001602	.000744	.001846
.000445	.001117	.000545	.001361	.000645	.001605	.000745	.001850
.000446	.001121	.000546	.001365	.000646	.001609	.000746	.001853
.000447	.001125	.000547	.001369	.000647	.001613	.000747	.001857
.000450	.001129	.000550	.001373	.000650	.001617	.000750	.001861
.000451	.001132	.000551	.001377	.000651	.001621	.000751	.001865
.000452	.001136	.000552	.001380	.000652	.001625	.000752	.001869
.000453	.001140	.000553	.001384	.000653	.001628	.000753	.001873
.000454	.001144	.000554	.001388	.000654	.001632	.000754	.001876
.000455	.001148	.000555	.001392	.000655	.001636	.000755	.001880
.000456	.001152	.000556	.001396	.000656	.001640	.000756	.001884
.000457	.001155	.000557	.001399	.000657	.001644	.000757	.001888
.000460	.001159	.000560	.001403	.000660	.001647	.000760	.001892
.000461	.001163	.000561	.001407	.000661	.001651	.000761	.001895
.000462	.001167	.000562	.001411	.000662	.001655	.000762	.001899
.000463	.001171	.000563	.001415	.000663	.001659	.000763	.001903
.000464	.001174	.000564	.001419	.000664	.001663	.000764	.001907
.000465	.001178	.000565	.001422	.000665	.001667	.000765	.001911
.000466	.001182	.000566	.001426	.000666	.001670	.000766	.001914
.000467	.001186	.000567	.001430	.000667	.001674	.000767	.001918
.000470	.001190	.000570	.001434	.000670	.001678	.000770	.001922
.000471	.001194	.000571	.001438	.000671	.001682	.000771	.001926
.000472	.001197	.000572	.001441	.000672	.001686	.000772	.001930
.000473	.001201	.000573	.001445	.000673	.001689	.000773	.001934
.000474	.001205	.000574	.001449	.000674	.001693	.000774	.001937
.000475	.001209	.000575	.001453	.000675	.001697	.000775	.001941
.000476	.001213	.000576	.001457	.000676	.001701	.000776	.001945
.000477	.001216	.000577	.001461	.000677	.001705	.000777	.001949

APPENDIX F

TABLE OF POWERS OF TWO

2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0.000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0.000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0.000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0.000 000 000 001 818 989 403 545 856 475 830 078 125
1 099 511 627 776	40	0.000 000 000 000 909 494 701 772 928 237 915 039 062 5
2 199 023 255 552	41	0.000 000 000 000 454 747 350 886 464 118 957 519 531 25
4 398 046 511 104	42	0.000 000 000 000 227 373 675 443 232 059 478 759 765 625
8 796 093 022 208	43	0.000 000 000 000 113 686 837 721 616 029 739 379 882 812 5
17 592 186 044 416	44	0.000 000 000 000 056 843 418 860 808 014 869 689 941 406 25
35 184 372 088 832	45	0.000 000 000 000 028 421 709 430 404 007 434 844 970 703 125
70 368 744 177 664	46	0.000 000 000 000 014 210 854 715 202 003 717 422 485 351 562 5
140 737 488 355 328	47	0.000 000 000 000 007 105 427 357 601 001 858 711 242 675 781 25
281 474 976 710 656	48	0.000 000 000 000 003 552 713 678 800 500 929 355 621 337 890 625
562 949 953 421 312	49	0.000 000 000 000 001 776 356 839 400 250 464 677 810 668 945 312 5
1 125 899 906 842 624	50	0.000 000 000 000 000 888 178 419 700 125 232 338 905 334 472 656 25
2 251 799 813 685 248	51	0.000 000 000 000 000 444 089 209 850 062 616 169 452 667 236 328 125
4 503 599 627 370 496	52	0.000 000 000 000 000 222 044 604 925 031 308 084 726 333 618 164 062 5
9 007 199 254 740 992	53	0.000 000 000 000 000 111 022 302 462 515 654 042 363 166 809 082 031 25
18 014 398 509 481 984	54	0.000 000 000 000 000 055 511 151 231 257 827 021 181 583 404 541 015 625
36 028 797 018 963 968	55	0.000 000 000 000 000 027 755 575 615 628 913 510 590 791 702 270 507 812 5
72 057 594 037 927 936	56	0.000 000 000 000 000 013 877 787 807 814 456 755 295 395 851 135 253 906 25
144 115 188 075 855 872	57	0.000 000 000 000 000 006 938 893 903 907 228 377 647 697 925 567 626 953 125
288 230 376 151 711 744	58	0.000 000 000 000 000 003 469 446 951 953 614 188 823 848 962 783 813 476 562 5
576 460 752 303 423 488	59	0.000 000 000 000 000 001 734 723 475 976 807 094 411 924 481 391 906 738 281 25
1 152 921 504 606 846 976	60	0.000 000 000 000 000 000 867 361 737 988 403 547 205 962 240 695 953 369 140 625
2 305 843 009 213 693 952	61	0.000 000 000 000 000 000 433 680 868 994 201 773 602 981 120 347 976 684 570 312 5
4 611 686 018 427 387 904	62	0.000 000 000 000 000 000 216 840 434 497 100 886 801 490 560 173 988 342 285 156 25
9 223 372 036 854 775 808	63	0.000 000 000 000 000 000 108 420 217 248 550 443 400 745 280 086 994 171 142 578 125
18 446 744 073 709 551 616	64	0.000 000 000 000 000 000 054 210 108 624 275 221 700 372 640 043 497 085 571 289 062 5
36 893 488 147 419 103 232	65	0.000 000 000 000 000 000 027 105 054 312 137 610 850 186 320 021 748 542 785 644 531 25
73 786 976 294 838 206 464	66	0.000 000 000 000 000 000 013 552 527 156 068 805 425 093 160 010 874 271 392 822 265 625
147 573 952 589 676 412 928	67	0.000 000 000 000 000 000 006 776 263 578 034 402 712 546 580 005 437 135 696 411 132 812 5
295 147 905 179 352 825 856	68	0.000 000 000 000 000 000 003 388 131 789 017 201 356 273 290 002 718 567 848 205 566 406 25
590 295 810 358 705 651 712	69	0.000 000 000 000 000 000 001 694 065 894 508 600 678 136 645 001 359 283 924 102 783 203 125
1 180 591 620 717 411 303 424	70	0.000 000 000 000 000 000 000 847 032 947 254 300 339 068 322 500 679 641 962 051 391 601 562 5
2 361 183 241 434 822 606 848	71	0.000 000 000 000 000 000 000 423 516 473 627 150 169 534 161 250 339 820 981 025 695 800 781 25
4 722 366 482 869 645 213 696	72	0.000 000 000 000 000 000 000 211 758 236 813 575 084 767 080 625 169 910 490 512 847 900 390 625

APPENDIX G

INSTRUCTION TIMING SUMMARY AND INDEX

		(Cycles) Standard Timing	(Cycles) Interlace Timing	Page
STANDARD INSTRUCTIONS				
Control Instructions				
BAR	Branch and Return	2	2	20
EXC	Execute	1 + inst.	1 + inst.	21
HTJ	Halt Jump	1	1	21
JAN	Jump on Accumulator Negative	1 or 2	1 or 2	21
JAP	Jump on Accumulator Positive	1 or 2	1 or 2	22
JAZ	Jump on Accumulator Zero	1 or 2	1 or 2	22
JMP	Jump	1	1	22
PAS	Pass (NAD)	1	1	22
SKM	Skip if Accumulator and Memory are Equal	2 or 3	1 or 2	23
SKN	Skip if Signal is Not Set (NAD)	2	2	23
SMZ	Skip if Memory is Zero	2 or 3	1 or 2	23
Fixed-Point Instructions				
ADD	Add to Accumulator	2	1.5	24
ADM	Add to Memory	3	2.5	24
SUB	Subtract from Accumulator	2	1.5	24
TLY	Tally	3	2.5	25
Indexing Instructions				
Class I				
DJX	Decrement and Jump on Index Not Zero	2	2	26
JIX	Jump on Index Not Zero	1 or 2	1 or 2	26
STX	Store Index Register	2	1	26
Class II				
AUX	Augment Index	2	1	27
LDX	Load Index Register	2	1	27
SKX	Skip on Index High	2 or 3	2 or 3	27
Input/Output Instructions, Direct				
PIN	Peripheral Input	3	2	28
POT	Peripheral Output	3 or 4	2 or 3	28
SKC	Control and Skip (NAD)	2	2	28
SKE	Skip if External Signal is Not Set (NAD)	1 or 2	1 or 2	29
STE	Set External Point (NAD)	1	1	29
Interrupt Instructions				
LIM	Load Interrupt Mask	2	1	29
SRB	Set/Reset Interrupt Block (NAD)	1	1	30
STI	Store Interrupt Register	2	1	30
XML	Exchange Interrupt Mask	3	2	30

		(Cycles) Standard Timing	(Cycles) Interlace Timing	Page
Logic Instructions				
EXT	Extract (Logical AND)	2	1	31
HAD	Half Add (Exclusive OR)	2	1	31
SMP	Superimpose (Inclusive OR)	2	1	32
SST	Substitute	3	2	32
Shift Instruction				
SFT	Shift (NAD)	$1 + \frac{3s}{7}$	$\frac{1 + 3s}{7}$	33
Word Transmission Instructions				
ALR	Alter Register (NAD)	1.5	1.5	33
DLD	Double Precision Load	3	2	35
DST	Double Precision Store	3	2	35
LDA	Load Accumulator	2	1	35
LDB	Load B Register	2	1	35
MTR	Multiple Transfer	2.5 + 2w	3.5 + w	36
STA	Store Accumulator	2	1	36
STB	Store B Register	2	1	36
STZ	Store Zeros in Memory	2	1	37
OPTIONAL INSTRUCTIONS				
Character Instructions				
CSK	Characters Skip if Equal	2 or 3	1 or 2	39
LCH	Load Character	2	1	40
SCH	Store Character	2	1	40
Expanded Memory Instructions				
EBR	Equalize Bank Register (NAD)	1	1	40
LBR	Load Bank Register (NAD)	1	1	40
SBR	Store Bank Register	2	2	41
Floating-Point Instructions				
FAD	Floating Add	$4 + \frac{S}{7}$	$4 + \frac{S}{7}$	42
FDV	Floating Divide	26	26	42
FMP	Floating Multiply	$9 + \frac{S}{7}$	$9 + \frac{S}{7}$	42
FSB	Floating Subtract	$4 + \frac{S}{7}$	$4 + \frac{S}{7}$	43
FUL	Floating Unload	4	4	44
Multiply/Divide Instructions				
DIV	Divide	12	12	41
MPY	Multiply	4	4	41
Input/Output Instructions, Buffered				
PCB	Peripheral Control and Branch	3 + 4w	3 + 4w	44
PDT	Peripheral Data Transfer	3 + 4w	3 + 4w	47

Notes:

1. Where two timings are listed, the smaller one applies when the instruction does not branch.
2. The variable (s) in the Shift instruction timing represents the number of binary shifts specified in the instruction word.
3. The variable (w) in the Multiple Transfer instruction timing represents the number of words transferred.
4. The variable (S) in the floating-point timings represents the number of shifts required to justify the operands and/or to normalize the result.
5. The variable (w) in the timing formulas for the Peripheral Data Transfer and the Peripheral Control and Branch instructions represents the number of words containing the control characters.

Honeywell 300 Programmers' Reference Manual, DSI-297

CHANGE NOTICE ONE, August, 1964

The following additions and corrections apply to the Honeywell 300 Programmers' Reference Manual, DSI-297, effective immediately.

1. Page 5. Under "Standard Peripheral Control," the third sentence now reads as follows: "Up to seven additional peripheral controls servicing up to 508 additional devices may be attached to the direct input/output channel."

2. Page 15. Under "INDEXED ADDRESSING," the first sentence should read: "When indexed addressing is used, the variant character of the instruction word has a value of from one to six, specifying one of the six 24-bit index registers."

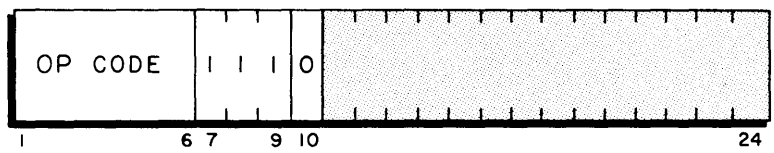
3. Page 16. Under "EXPANDED MEMORY ADDRESSING," the fourth sentence should read: "The instructions are divided into two sets: those whose address field normally references the sequence register (namely, BAR, DJX, EXC, JAN, JAP, JAZ, JIX, JMP, SBR, STS, and PCB) and those whose address field normally references data (that is, all other instructions).

4. Page 19. Under "Mnemonic Operation Code" the instructions having an octal variant of zero are: PAS, EBR, LBR, and RSS.

5. Page 20. Under "Mnemonic Operation Code" the instructions having an octal variant of seven are SRB and HLT. The first sentence should read: "Instructions having the same operation code and variant character (e.g., PAS, EBR, LBR, and RSS) are differentiated by means of bits in the address field of the instruction word."

6. Page 21. The HTJ instruction is deleted and is replaced by the following instruction. The HTJ entry in the index on page 105 is changed to HLT.

HLT — Halt (NAD)

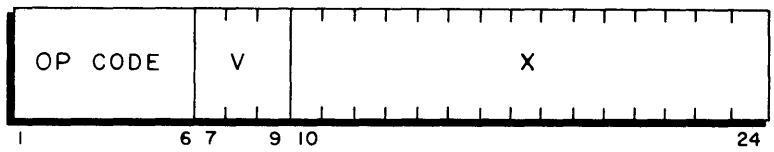


An interruptable halt occurs. That is, an interrupt signal can cause a subsequence.

Timing. 1 cycle.

7. Page 26. Add the following instruction before the DJX instruction. The index on page 105 is updated accordingly.

AIX — Augment Index Immediate

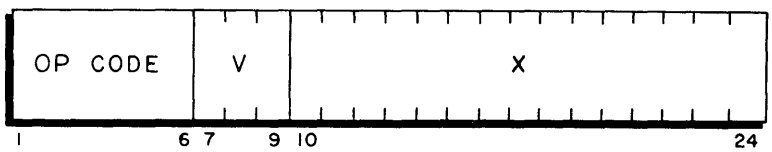


The contents of register v are incremented by x. The result replaces the contents of that register.

Timing. 1 cycle.

8. Page 26. Add the following instruction at the bottom of the page. The index on page 105 is updated accordingly.

SXI — Skip Immediate on Index High



If the contents of register v are greater than x, (SR) are incremented by two (thus the next instruction is skipped); else (SR) are incremented by one.

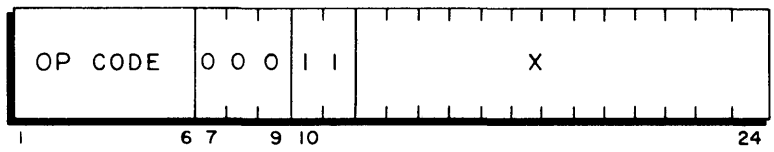
Timing. 1 or 2 cycles.

9. Page 28. In the SKC instruction word diagram, bit positions 10 through 15 constitute the control field. Bit positions 16 through 24 constitute the address field.

10. Page 30. The SRB instruction word diagram contains a 1 bit in position 10.

11. Page 36. Insert the following instruction after the MTR instruction. The index on page 106 is updated accordingly.

RSS — Restore Status (NAD)



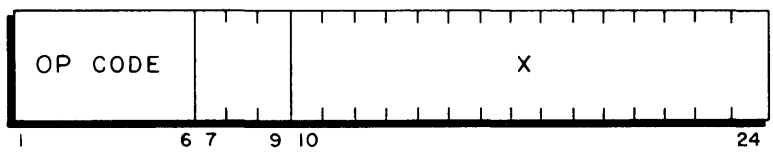
For each of bits 13-24 of x, if the bit is one, the corresponding indicator is set if installed in the system. The indicators are:

Bank Register
Carry
Divide Overcapacity
Exponential Overflow
Exponential Underflow
Overflow

Timing. 1 cycle.

12. Page 37. Delete the STZ instruction and add the following instruction in its place. The index on page 106 is updated accordingly.

STS — Store Status



For each of the following indicators that is set, a one replaces the corresponding bit in positions 13-24 of (x). Bits 1-12 are protected. All the indicators are set to zero when the instruction has been executed. This instruction can be used to load information into the address field of the RSS instruction word. The indicators are:

Bank Register
Carry
Divide Overcapacity
Exponential Overflow
Exponential Underflow
Overflow

Timing. 2 cycles. With interlace: 1 cycle.

13. Pages 44 and 47. Opposite "w" in the PARAMETER column, the paragraph under "Second Word" in the INTERPRETATION column should read: "The number of control characters in the instruction. Each four control characters require one word of storage. Note that bit 7 of the second word of the instruction must be one."

HONEYWELL
ELECTRONIC
DATA
PROCESSING
WELLESLEY HILLS,
MASSACHUSETTS 02181