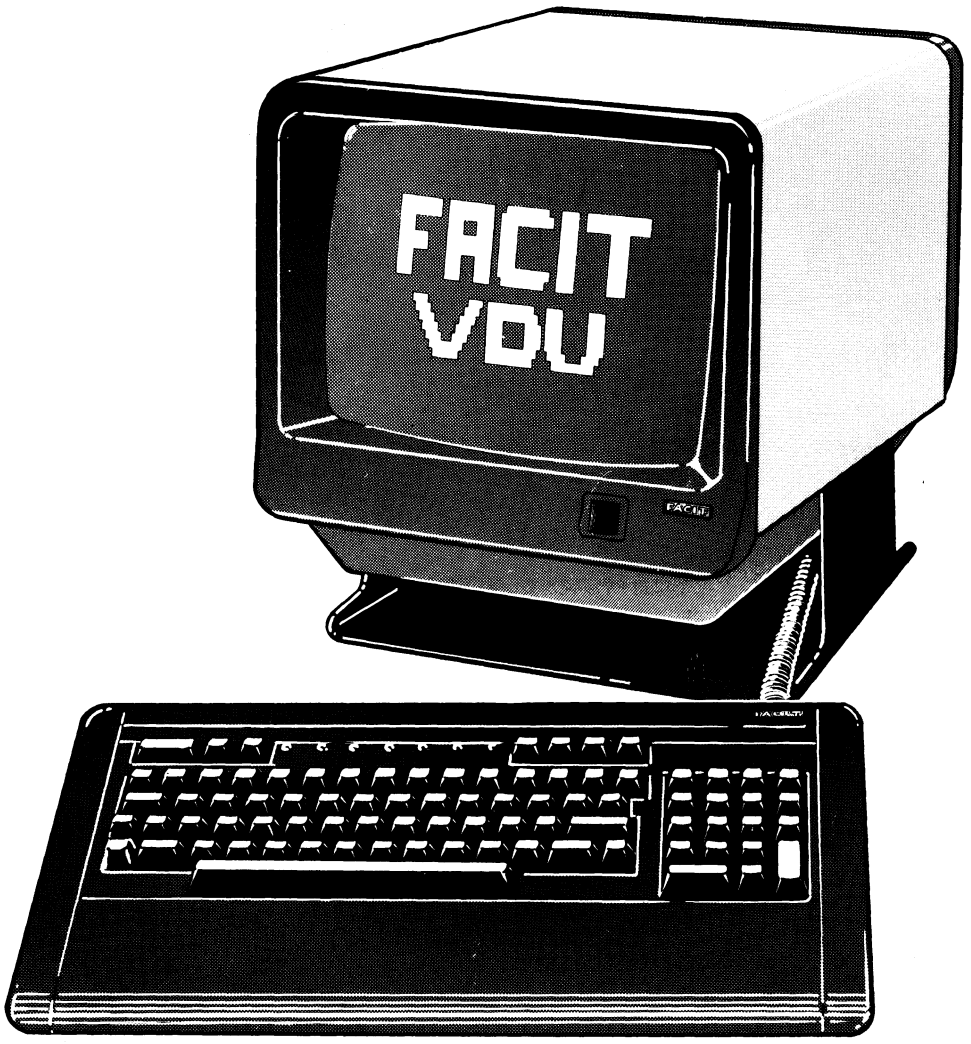
FACIT
DATA
PRODUCTS

DETAILED LIST OF CONTENT AT PAGES 42-43



SERVICE INSTRUCTION

4431

VIDEO TERMINAL

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Facit AB · Technical Service Department · S-597 00 ÅTVIDABERG · SWEDEN

SCOPE OF THE MANUAL

The information contained in this manual is intended for the maintenance group, other available documents are:

Facit 4431 Technical Description
Facit 4431 Operator Guide

1 INTRODUCTION

As with any electronic equipment, all standard safety precautions should be observed while servicing the Facit 4431 Video Terminal. Any servicing which requires opening the cabinet must be performed only by qualified service personnel.

****

WARNING

Hazardous voltages are exposed when the cabinet top is removed. Use extreme caution when servicing the monitor assembly or power supply. Under certain conditions dangerous potentials may exist even when the power is off due to the cathode ray tube.

****

In the text and on the schematics, locations are referenced in the following manner:

Part number (IC number) (:pin number) (Signal name) (Schematic page).

Example:

Reference to Pin 19 of D71 located at page MEM
Circuit Diagram: D71:19 RD ATT.(MEM)

Acronyms and Abbreviations:

Main Logic Board Schematic Drawings:

I/O	Input/output interface
KBD	Keyboard interface
MEM	Display Refresh RAM
CPU	Processor
SG	Sync Generator
VG	Video Generator

Devices:

CPU	Central Processing Unit
CRT	Cathode Ray Tube
CRTC	CRT Controller
EAROM	Electrically Alterable Read-Only Memory
EPROM	Eraseable Programmable Read-Only Memory
LED	Light Emitting Diode
RAM	Random Access Memory
ROM	Read Only Memory
SIO/DART	Serial Input/output or Dual channel Asynchronous Receiver/Transmitter

1.1 DESIGN

The terminal consists of three major physical subassemblies:

the Main Logic Board (MLB)
the Keyboard (KBD)
the Monitor assembly
and the Power Supply (PS)

The majority of servicable components are on the Main Logic Board, which provides six (6) major circuit functions:

1. Keyboard Interface
2. Microprocessor Control
3. Input/Output Interfaces
4. Display Refresh Memory
5. Synchronization Generator
6. Video Generator

Chapter 6 contains a general circuit description and each of these circuits are described in detail in Section 7 of this manual. A block diagram showing the main functional components **of the terminal is given in Fig 7.1. The rest of Section 7 describes how these components combine to perform all terminal operations.**

1.2 SPECIFICATIONS

Monitor

Screen capacity	1920/3168 characters
Characters per line	80/132
Number of lines	25(24 + 1 status line)
Screen	Green phosphor, P42 C Non glare with medium short percistance (300uS)
Tube size	30.5 cm (12") diagonal
Veiwing area	310 sq. cm (48 sq.in.) 20 cm x 15 cm (8"x6") rectangele (centered on screen) +/-0,2"
Character size	(80col) 5mm high x 2 mm wide(0.2"x0.08") (132col) 5mm high x 2mm wide (0.2"x0.05")
Referesh rate	50 or 60Hz
Scan method	Raster
Character generator	128 displayable char. (inc. space) Alternativ set possible 7 x 9 character definition with 2 dot separation between characters.
Frequency	**15 700Hz +/- 500Hz**

Interface
CCITT V24/RS-232-C
Current Loop (Optional)
Composite video output (Optional)

Protocols	X-ON/X-OFF protocol
Environmental Conditions	
Temperature	10° to 40°C (operational) -10° to 60°C (storage)
Voltages	117V 220V
Frequencies	49-61Hz
Consumption	65 Watts
Dimensions Display Unit	
Width	32.6cm (12.8")
Depth	40.2cm (15.8")
Height	37cm (14.7")
Keyboard	
Width	43.8cm (17.25")
Depth	26cm (10.2")
Height,rear	6.4cm (2.5")
Height,front	1.0cm (0.4")
Total weight	20 Kg (44lb)
Data format	
Data bits	8 or 7 asynchronous
Data bit 8	0 or deleted
Parity	Odd,even or inhibited
Data transfer rate	75 to 19.200 bits/-sec.
Operator controls Switches: ON/OFF	

2 RECEIVING, UNPACKING AND INSPECTION

The Facit 4431 terminals are carefully packed to insure safety during shipment, however, when the terminal arrives check the following:

- the invoice against your original purchase order
- examine the outside of the shipping container closely for signs of abuse or damage in transit

A chrushed or punctured carton naturally calls for a careful inspection of the contents, if any damage is found inform the delivery agent about any damage found.

2.1 POWER AND SIGNAL WIRING

The 4431 terminal wiring consists of an AC power cord which is included with the display unit.

The keyboard is connected to the display unit by a flexible coiled cable. The V24/RS232C signal cables are provided by the customer.

2.2 POWER ON/PERFORMANCE CHECK

Inspection before power on:

- check that the model plate corresponds to order and packing case marking
- check for proper keyset
- check that accessories and documentation are supplied
- check, and if not appropriate, modify the power connection to your national standard. Make sure that proper grounding is performed and that proper voltage is selected. Also check fuse value, should be 0.5Amp slow at 220/240Volts and 1Amp at 115Volt.

Power On

This test require a Test gear such as Facit Text Generator or a 4208 Casset Drive with special Demo or Test program.
NOTE: Before connecting the terminal to ANY external data source, see to it that the terminal is connected to the Mains with proper grounding, this procedure will take care of any eventuall high voltage discharge through the interface cable causing damage to the Line driver/Receiver circuits.

- wait approx. 1 minute to observe normal screen illumination (the raster may be visible during few minutes of warm up).
- upon power-up all seven LED´s will be lit for about 0.5 sec. The country/product select code is displayed on the LED´s for approx. 1 second (See the country/product select table below).

LED´s	Meaning
xxx xx00	4420
xxx xx10	4430
xxx xx11	4431
000 xxxx	US
001 xxxx	Swe/Fin
010 xxxx	Germany
011 xxxx	Denmark
100 xxxx	Britain
101 xxxx	Spain
110 xxxx	France
111 xxxx	Norway

NOTE If during initialization a suspected fault is detected, the bell will ring 5 times and an error code will be displayed in the upper left portion of the screen. If the terminal halts with all the LED´s on, then the processor has determined that the scratchpad RAM D72 is defective and no furhter tests are attempted.

ERROR CODES:

1 display memory fault

2 EAROM parity error

4 EAROM checksum error

(For instruction how to repair, see Chapter 10)

- disconnect the keyboard from the terminal and power on the terminal, after approx. 5 sec. a presentation of the terminal program revision is shown at the upper left corner of the display.
  Ex. FACIT 4431 rev. "D.X." 9/82

- if no fault is detected you may continue with the performance check, first enter Set-Up mode and do as follows: (use the Operator Guide as reference if necessary)

1 SET-UP A.

a change the brightness setting using cursor up for increased brightness and cursor down to reduce the brightness, minimum brightness should be with the half intensity area just visible, if the intensity need adjustment, see chapter 9 for instructions.

b depress key (3) to clear all tabs, move the cursor and depress key (2) to toggle Change Tabs, set the tabs in random positions. Reset the terminal and check that the Tabs are in proper positions again, when entering the SETUP A mode.

c depress key (9) to enter into 132 column mode, control that the left or right margins of the screen does not fold back, if so adjustment is needed and is explained in chapter 9. Enter 80 column mode again.

d depress PF1 and PF2 and to change pages, see upper right corner of the screen.

e enter SET-UP B, depress key (5), move cursor and toggle the displayed switches by using key (6), set all (1) to (0) and all (0) to (1) (note that in column 3 switch 4 can not be changed from 0) and change the T SPEED and R SPEED to 75 by depressing of key (7) and (8). Recall fac tory settings by depressing the Shift key and R at the same time, (SHIFT)+(R). Return to SET-UP B mode.

f depress key (5) to enter SET-UP C mode. Make the same procedure as above with the displayed switches and the printer speed. Note that in column 4, switches 2,3, and 4 can not be changed from 0.

g reset the terminal. Enter SET-UP A and set the terminal in LOCAL MODE, depress key (4).

h depress (ESC) (Shift + 3) (8) (The terminal must be in ANSI mode). This command fills the entire screen area (exept row 25) with E´s for screen focus and screen geometry alignment. If any adjustment is necessary see chapter 9 for advice. Reset the terminal.

i with the terminal in local mode, test all keys for proper movement and function.

j connect a suitable data source to the I/O connector and a Printer to the Printer connector, use speciall test program or demo program for this test.

k depress (ESC) (5B) (2) (;) (9) (y). Note that the key for the 5B Hex code is to be selected by the aid of National version keyboard code and command summary listing in the Technical description for the 4431 terminal. This com mand initiates a series of special tests for use by servicing personnel. The test is repeated until a failure occurs or until the power is switched off.

- Finally, fill in and send the test report to

  Facit AB, Technical Service Department

  S-597 00 Åtvidaberg SWEDEN

3 INSTALLATION

3.1 INITIAL SETTING-UP

The Facit 4431 display unit should be positioned on a firm surface; the display unit tilts on its stand to allow the user to optimise the viewing angle. The keyboard connector (at the end of the coiled connector lead) plugs into the rear of the display unit, in the lefthand socket (viewed from the read, see Fig). The keyboard may then be positioned to suit the user.

Ensure that the mains supply lead is terminated in a suitable plug for the local power outlet (a ground connection must be incorporated).

Refer to section 4 for interface connections to both the host and local printer (if required).

3.2 ACCESS TO MAIN LOGIC BOARD IN DISPLAY UNIT

The user will need access to the main logic board to alter the setting of jumpers described in sections to and access in gained as follows:

1 Switch off the unit and disconnect from the mains supply.

2 There are four slot-head fixing screws which retain the display unit top cover. These are located at the bottom of the cover, under the lip, close to where the stand enters the display unit body. The screws can be accessed from below by means of a short screw-driver. To remove the cover the screws must be screwed IN (clockwise) as far as they will go.

3 Grasp the lip of the cover on each side, pull outwards and simultaneously lift the cover.

4 Access to the jumpers on the main logic board is now possible.

5 Replacement of the cover is the reverse of the removal. The retaining screws must then be screwed OUT (anticlockwise) as far as they will go.

3.3 ACCESS TO KEYBOARD PCB

The user will need access to the keyboard p.c.b. to allow the setting of jumpers described in sections and access is gained as follows:

1 Switch off the unit and disconnect the keyboard from the display unit.

2 Remove the two retaining screws at the right hand end of the keyboard, and then remove the end cap.

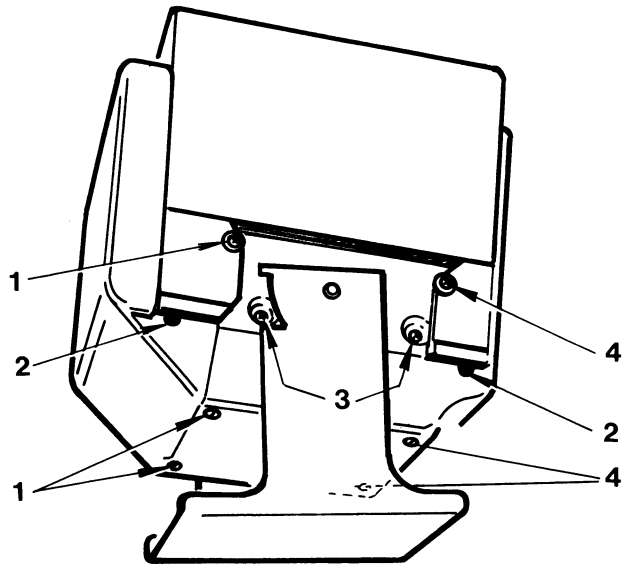
3 Slide out the printed circuit board (disconnecting the loudspeaker lead if necessary) and lift off the top plate.

4 The jumpers and associated components are to be found along the top of the p.c.b.

5 Reassembly of the keyboard is the reverse of the above. Ensure that the p.c.b. and top plate slide in the retaining grooves in the keyboard housing.

3.4 KEYCLICK/BELL VOLUME ADJUSTMENT

The audible tones produced by the unit are generated by a small loudspeaker mounted in the keyboard. The level of sound produced may be adjusted by rotating (by means of a small screw-driver) the SPKR VOL ADJ potentiometer. This is located in the left hand top corner of the keyboard p.c.b.



1 Rear panel
2 Top cover
3 Monitor (CRT) retaining screws
4 Front panel
5 Volume adj. pot
6 End cap screw

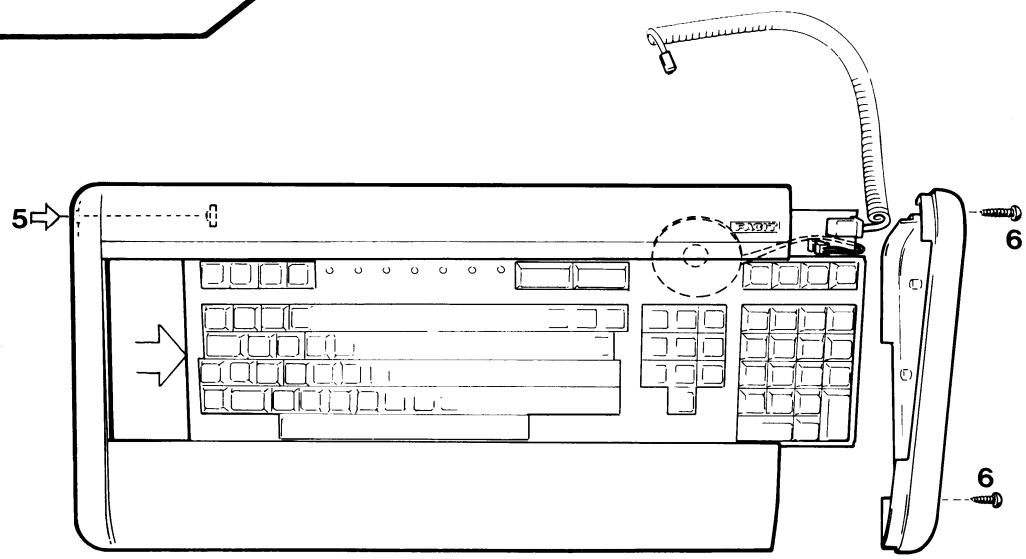


FIG 3.1

3.5 JUMPERS ON THE MAIN LOGIC BOARD

Jumper W1. With jumper W1 inserted, +5V is applied to the I/O connector pin 18.

Jumper W3. This jumper makes it possible to choose either 2716 or 2732 as character generator (D40). See Fig 3.3 for details.

Jumper W4. Inserted = Test mode, (factory test only).

Jumper W5. Inserted = EROM Write Enable.

3.5.1 KEYBOARD PCB

Two groups of jumpers are fitted to the keyboard PCB.

3.5.1.1 Facit 4431 Selection (W2)

Jumper W2 on the keyboard PCB must be fitted for Facit 4431 operation. Jumper W1 is not fitted.

3.5.1.2 National Keyboard Selection (W4,5,6)

Jumpers W4, W5 and W6 on the keyboard PCB are used to select which country the keyboard is for use in. Jumper W3 is not fitted. The table below shows the possible combinations. The keyboard will be supplied set to one particular configuration with appropriate keytops fitted. If a change is made to the jumper settings the keytops should also be changed (and a new character generated ROM fitted).

Country	Jumper		
	W4	W5	W6
U.S. (ASCII)	Down	Down	Down
Sweden/Finland	Up	Down	Down
Germany	Up	Up	Down
Denmark	Down	Up	Down
Britain	Down	Up	Down
Spain	Down	Down	Up
France	Up	Up	Up
Norway	Up	Down	Up

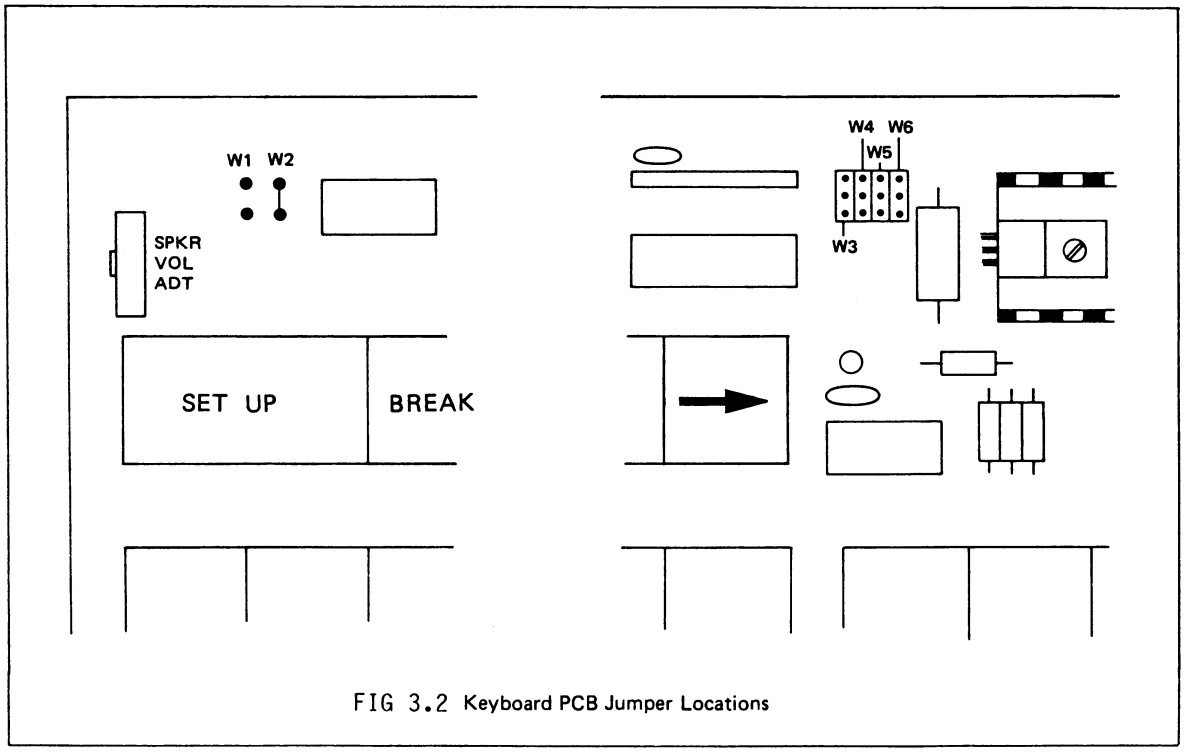


FIG 3.2 Keyboard PCB Jumper Locations

3.5.2 MAIN LOGIC PCB

There are 4 jumpers fitted to the main logic board as shown in Fig 3.3.

3.5.2.1 +5V on I/O Connector Pin 18 (W1)

Pin 18 on the I/O connector may be linked to +5V by fitting jumper W1. +5V on pin 18 is required by the Facit 5165/66 Current Loop Adapter. When the jumper is not fitted pin 18 is connected internally.

3.5.2.2 Standard/Extended Character Generator (W3)

When the standard character generator PROM is fitted (type 2716) the jumper W3 must link the centre and right hand pins (see Fig 3.3). When extended character generator is used (type 2732) the jumper must link the centre and left hand pins.

3.5.2.3 Production Test (W4)

This jumper is used only during production. It must not be fitted during normal operation.

3.5.2.4 Disable/Enable Save (W5)

The user may prevent the operator saving alternative Set-up parameter values (using the SAVE function) by removing the jumper W4. When this jumper is fitted the SAVE function works as described in section 5.

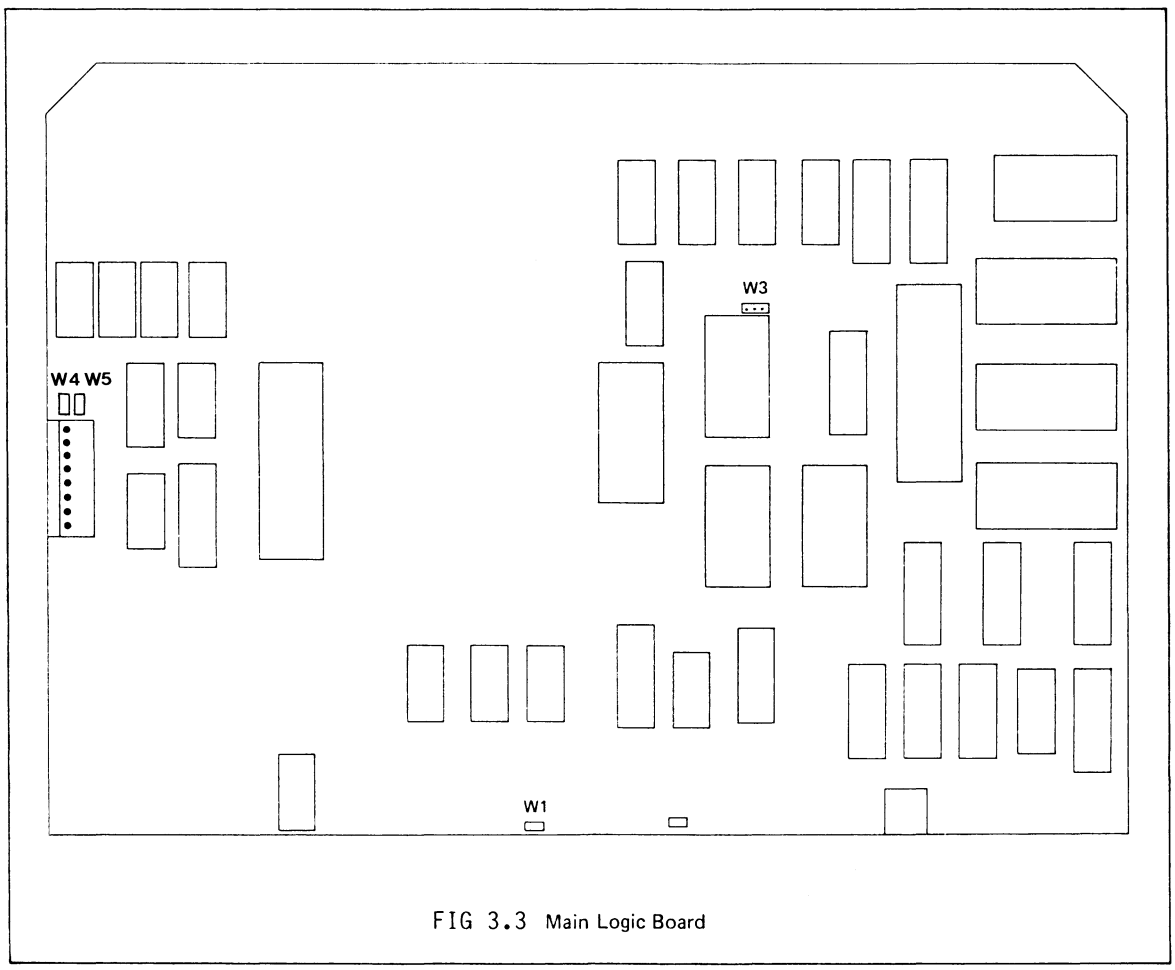


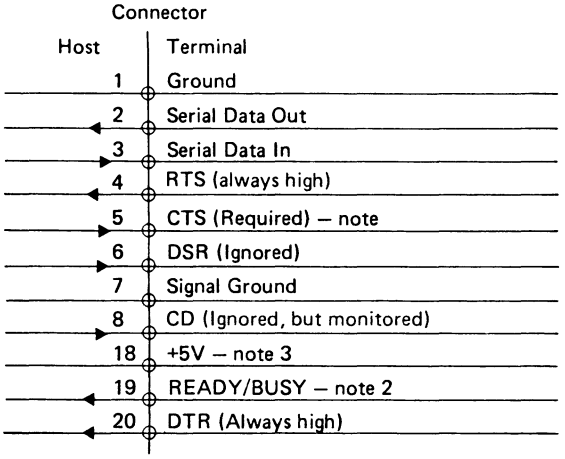
FIG 3.3 Main Logic Board

4 INTERFACE INFORMATION

The interface connectors at the rear of the terminal are shown below.

4.1 V.24/RS-232-C COMMUNICATION INTERFACE

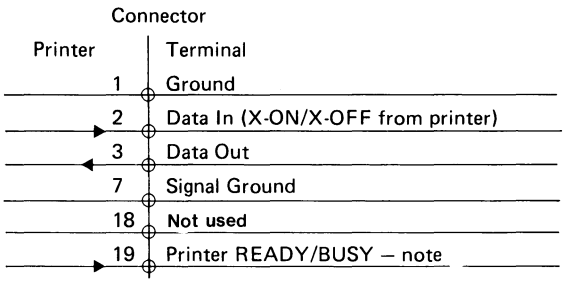
The pin assignments for the 25-pin male V.24/RS -232-C communication connector are as follows:



NOTES: (1) CTS signal must be present at the terminal (high) before data can be sent to the host.
(2) READY = High
BUSY = Low
(3) +5V for Facit 5166 current loop adapter, supplied by fitting a jumper on the main logic board.

4.2 V.24/RS-232-C PRINTER INTERFACE

The pin assignments for the female V.24/RS-232 -C printer connector are as follows:



NOTES: READY = High
BUSY = Low

4.3 CURRENT LOOP INTERFACE

Current loop interface adapter may be fitted onto the I/O interface connector (Facit 5166) of the Facit 4431. The terminal connectors may be internally linked (via jumper), to provide a +5V supply to the adapter, which is all that is required for passive/passive operation. Where the user wishes to employ an active transmitter an external 12V supply must be provided.

4.4 COMPOSITE VIDEO OUTPUT

The Facit 4431 provides a composite video for use with an external video device. The composite signal is a combination of the video signal and horizontal and vertical synchronisation signals. Connection is via a female phono connector. The output impedance is 75 ohms. The video signal is of the RS170 type.

5 SET - UP FEATURES

5.1 GENERAL FEATURES OF SET-UP MODE

Set-Up mode is entered by depressing the (SET-UP) key on the keyboard. Initially the SET-UP A display is shown.

At any time in the SET-UP mode the operator may adjust the brightness of the screen, switch between on-line and local operation, change or recall the EAROM values or reset the terminal to its initial state.

Exit from Set-Up mode (A, B or C) may be at any time pressing the (SET-UP) key again. On exit from SET-UP mode, the parameter value are preserved and will be displayed again whenever SET-UP mode is entered (exept after Power Off)

You will find a detailed information about the SET-UP mode in the Technical Description.

5.2 SET-UP MODE SUMMARY

GENERAL SET-UP FEATURES (SET-UP A, B and C)

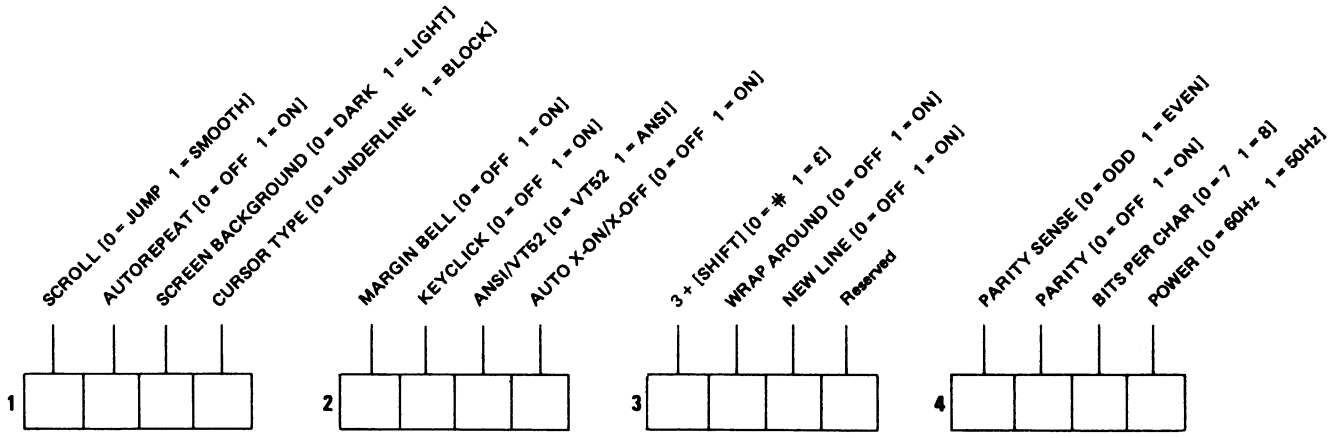
Line/Local	– [4] to toggle
Screen Brightness	– [↑] to increase [↓] to decrease
Save Set-up Features	– [SHIFT]+[S]
Recall Set-up Features	– [SHIFT]+[R]
Recall Factory Settings	– [SHIFT]+[D]
Recall Factory Tabs	– [SHIFT]+[T]
Reset Terminal	– [0]

SET-UP A

Change Tabs	– [2] to toggle
Clear All Tabs	– [3]
80/132 Column	– [9] to toggle
Page 1/Page 2	– [PF1] / [PF2] (80 column, 2 page mode)
Set-up B	– [5]

SET-UP B

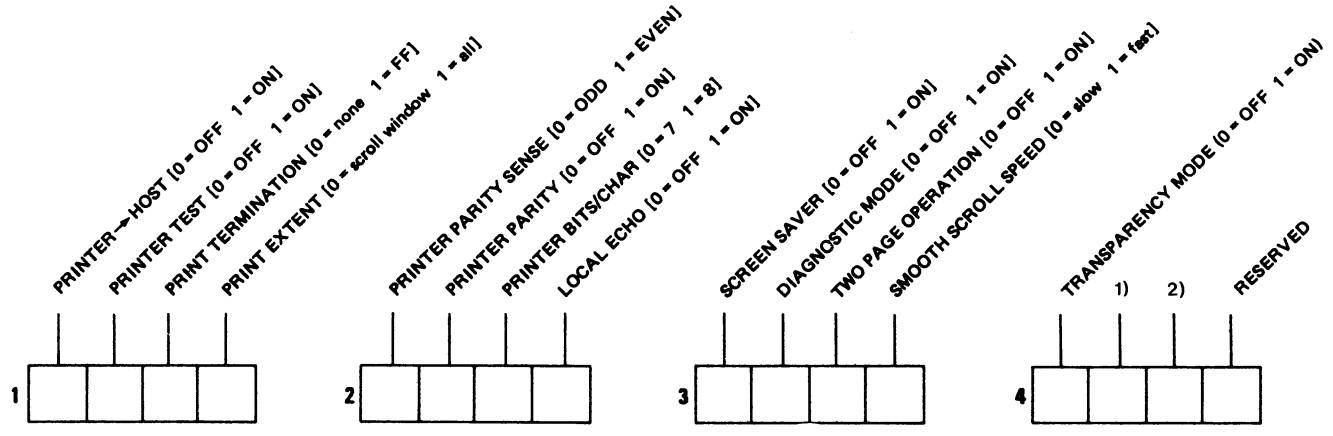
Set PF Keys sequence – [SHIFT]+[PFx] [delimiter] sequence [delimiter] (x = 1 to 4)
Set Answerback message – [SHIFT]+[A] [delimiter] message [delimiter]
Toggle displayed switches – [6]



Increment T SPEED – [7]
Increment R SPEED – [8]
Set-up C – [5]

SET-UP C

Toggle displayed switches – [6]



Increment PRINTER SPEED – [7] or [8]
Set-up A – [5]

1) DISCARD "XOFF/XON FROM HOST" (0=OFF, 1=ON)
2) CHARACTER TO HOST (limited to 60cps/unlimited

6 GENERAL BLOCK DIAGRAM DESCRIPTION

6.1 MICRO-PROCESSOR CONTROL UNIT

The Facit 4431 terminal is based upon the Z80A Microprocessor. The principal function is to decode each character as it is received (from keyboard or host computer), detect characters and character sequences representing terminal commands, and obey these commands. The microprocessor also performs background tasks of keyboard scanning, character and cursor blinking, bell generation, loading the display refresh RAM starting address for each of the 25 display rows, and various other real-time functions. The microprocessor controls all communication on the CPU bus, reading data from the EPROMS, EAROM, display refresh RAM, SIO, and the keyboard, and writing to the display refresh RAM, SIO, CTC, CRTC, EAROM, and various hardware latches.

A block diagram of the Microprocessor control unit is shown in Fig 6.1.

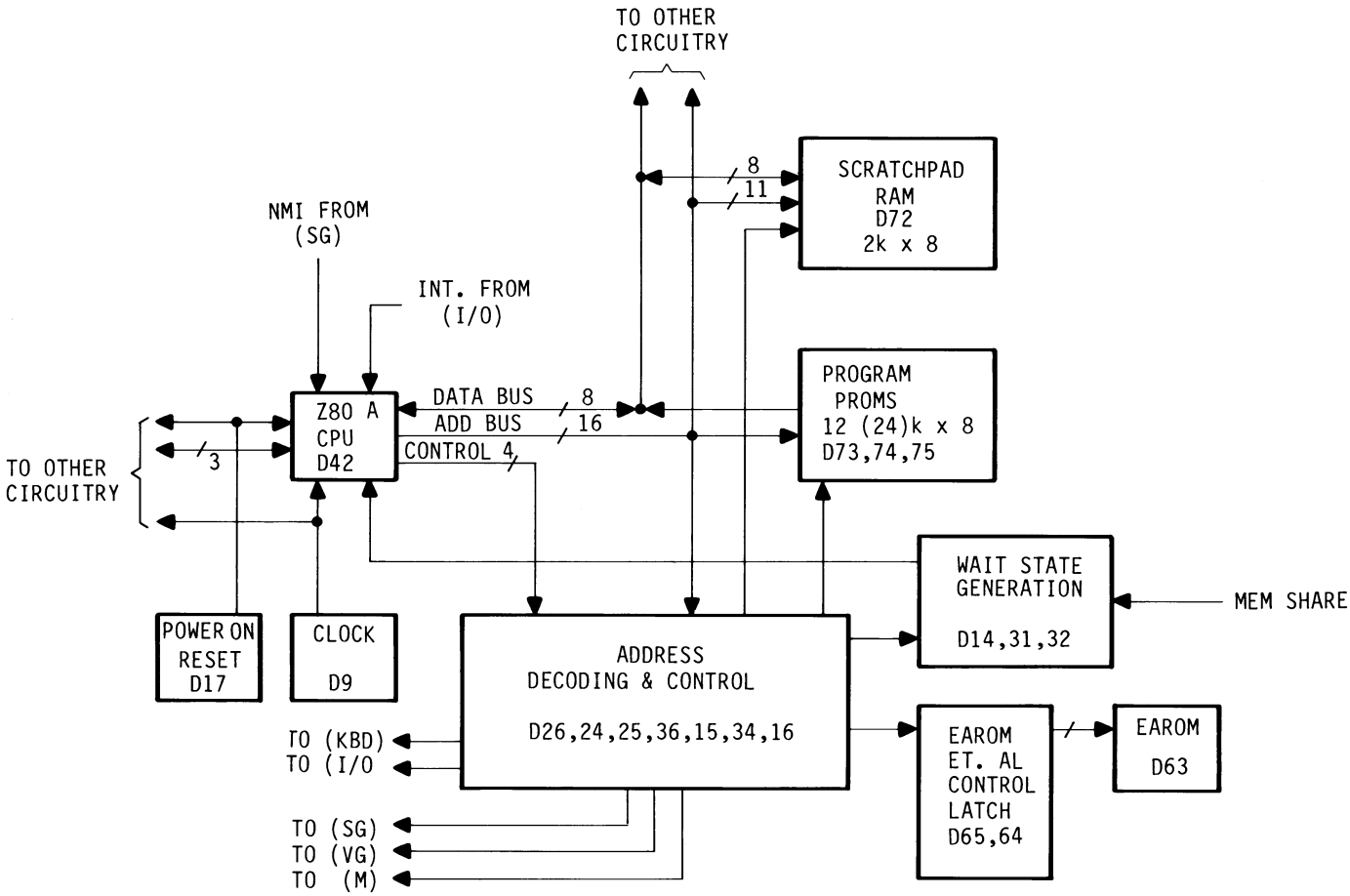


FIG 6.1 MICROPROCESSOR CONTROL UNIT

6.2 DISPLAY REFRESH MEMORY

The Display Refresh Memory stores the ASCII code and video attribute status of each charater to be diplayed on the screen. The Facit 4431 has 4k (4096) 12 bit words of display memory to provide 2 pages of memory in the 80 column mode, or 1 page of memory in the 132 column mode. Access to the display memory by the CPU (to write and read data) is controlled by the DISPLAY ACCESS HANDLER circuitry. A block diagram of the Display Refresh Memory is shown in Fig 6.2.

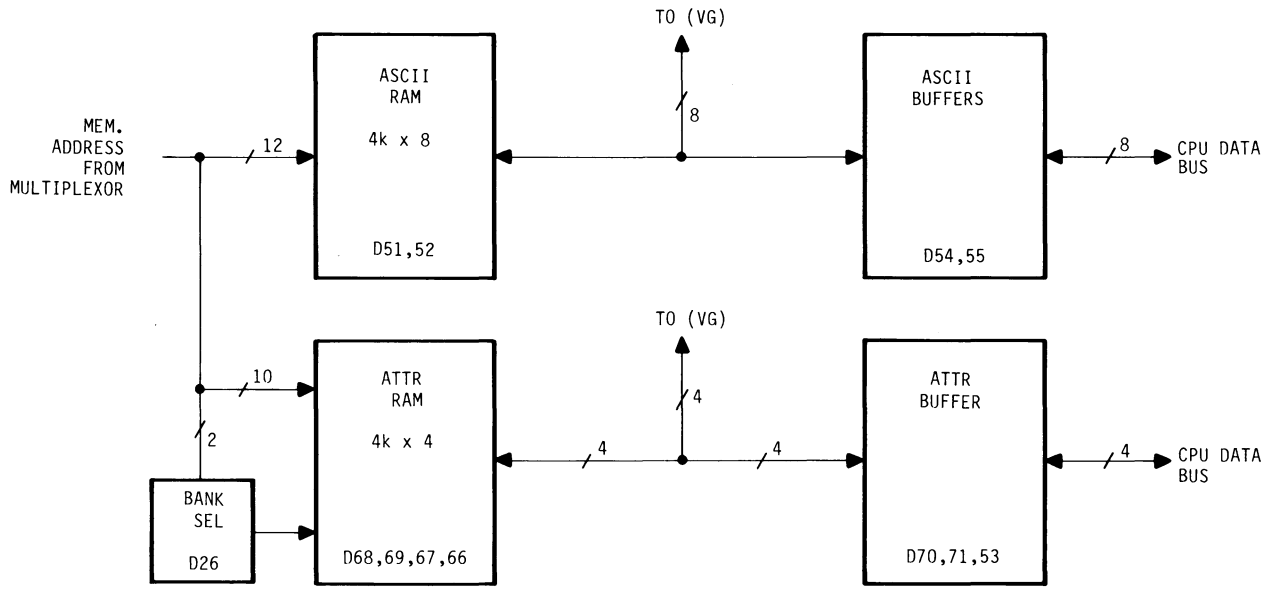


FIG 6.2 DISPLAY MEMORY

6.3 SYNCHRONIZATION GENERATOR

Figure 6.3 is a block diagram of the Sync Generator Circuits.

The Sync Generator circuit provides all timing signals required to:

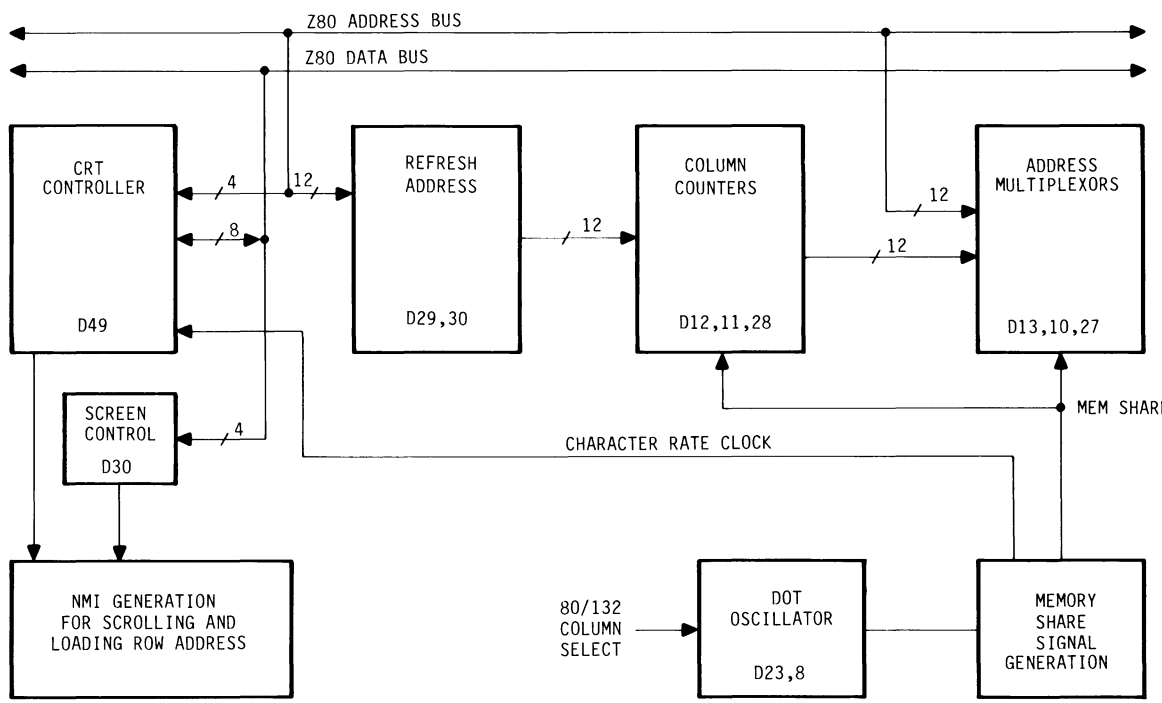


FIG 6.3 SYNCHRONIZATION GENERATOR

- address the display refresh memory to extract extract characters to be passed on to the video generator circuit.
- indicate to the video generator circuit the presence of double wide and/or double high character rows.

- provide shift and load commands to the video shift registers.
- interrupt the Z80A every vertical retrace, and every 10 horizontal scans to request row start information.

The Sync Generator circuitry consists of the 80 and 132 column dot oscillators, CRT Controller, Interrupt Generator, MEMSHARE Generator, and the Refresh Address Generator/Multiplexer.

6.4 VIDEO GENERATOR

The Video Generator circuit uses the outputs of the Sync generator and the display memory circuits to create the appropriate video signals for each character to be displayed. The ASCII character code from the display memory, the scan line count, and the double high/double wide control lines are combined to generate the address in the character generator EPROM where the dot pattern for the character to be displayed is stored. The dot pattern is then converted to serial form by the video shift registers and combined with the attribute data before geing sent to the monitor. A block diagram of the Video Generator is shown in Fig 6.4.

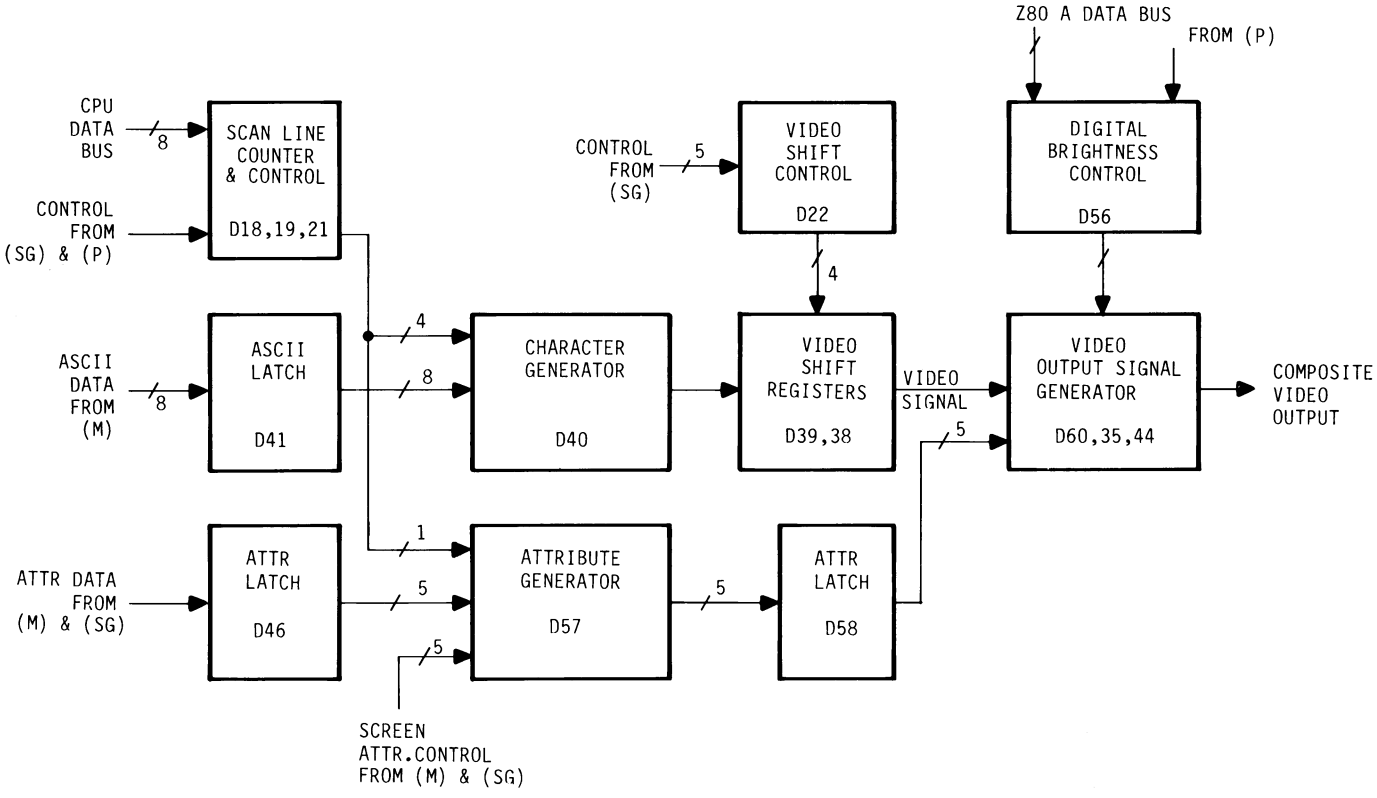


FIG 6.4 VIDEO GENERATOR

6.5 INPUT/OUTPUT INTERFACE

Figure 6.5 is a block diagram of the Input/Output Interfaces. Communication between the Facit 4431 and the host computer and local printer is through bidirectional, asynchronous serial V24/RS-232-C ports. A dual channel SIO (Serial Input/output controller) performs the parallel/serial data conversion required to adapt and synchronize the terminals internal parallel data to the serial format of the external devices. Communications parameters such as data rate , parity, and word lenght are selected by the operator in the SET-UP MODE, and stored from one session to the next in the non-volatile EAROM. The Z80A CPU reads these parameters from the EAROM upon power-up, and uses this data to configure the SIO and the baude rate clock generators.

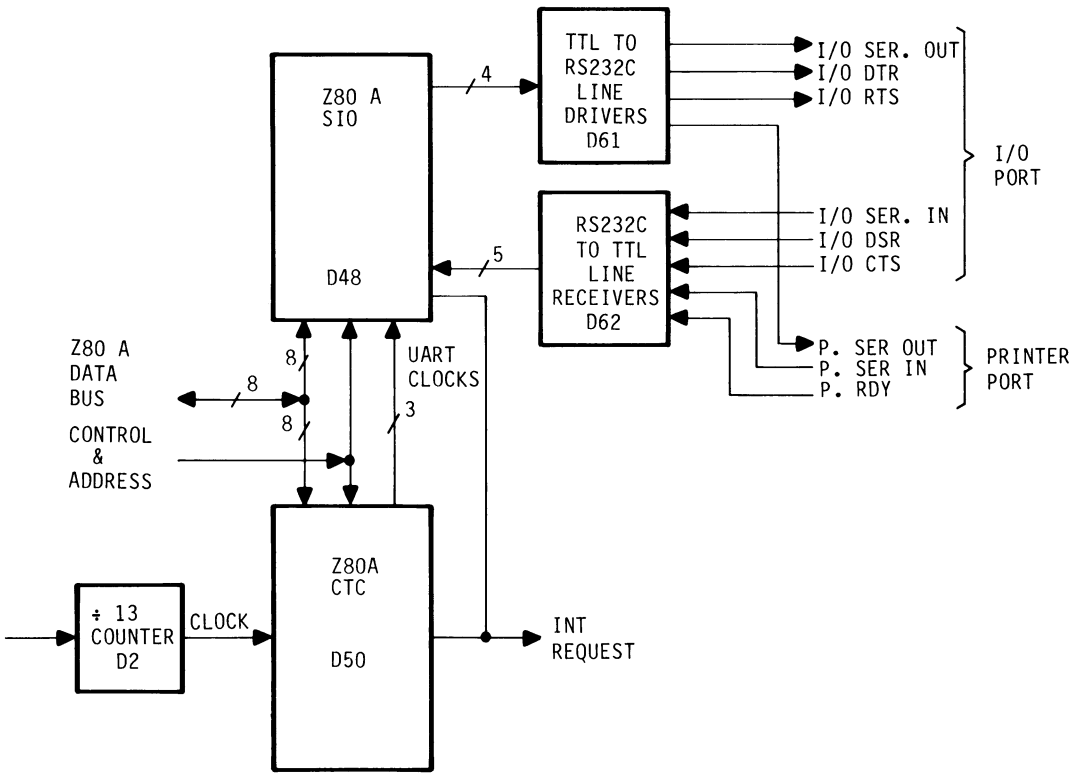


FIG 6.5 INPUT/OUTPUT, PRINTER INTERFACES

6.6 KEYBOARD SYSTEM

The keyboard is a seperate item connected to the display unit by a flexible coiled cable. To simplify the connection, the keyboard encoding is performed on the keyboard itself producing a serial code which is received by a UART on the Main Logic board of the terminal. The keyboard logic is based on the INTEL 8035 microprocessor using 2k byte program.National character versions are jumper selectable. Keyboard encoding is done using an encoder ROM. Depression of each encoded key or key combination produces a unique ROM address, and in each ROM location is the code for associated key depression(s). The selected code is then transmitted in serial form to the keyboard UART in the display unit. A block diagram of the Keyboard system is shown in Fig 6.6.

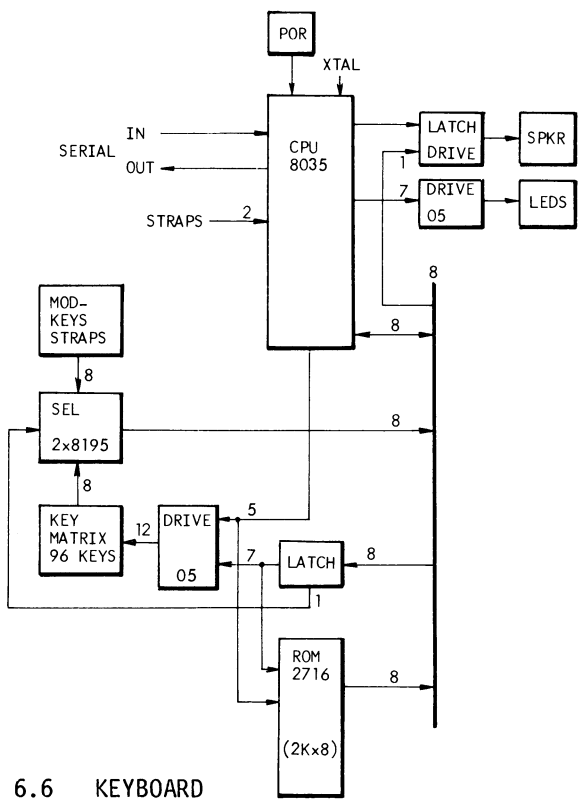


FIG 6.6 KEYBOARD

7 DETAILED FUNCTIONAL DESCRIPTION

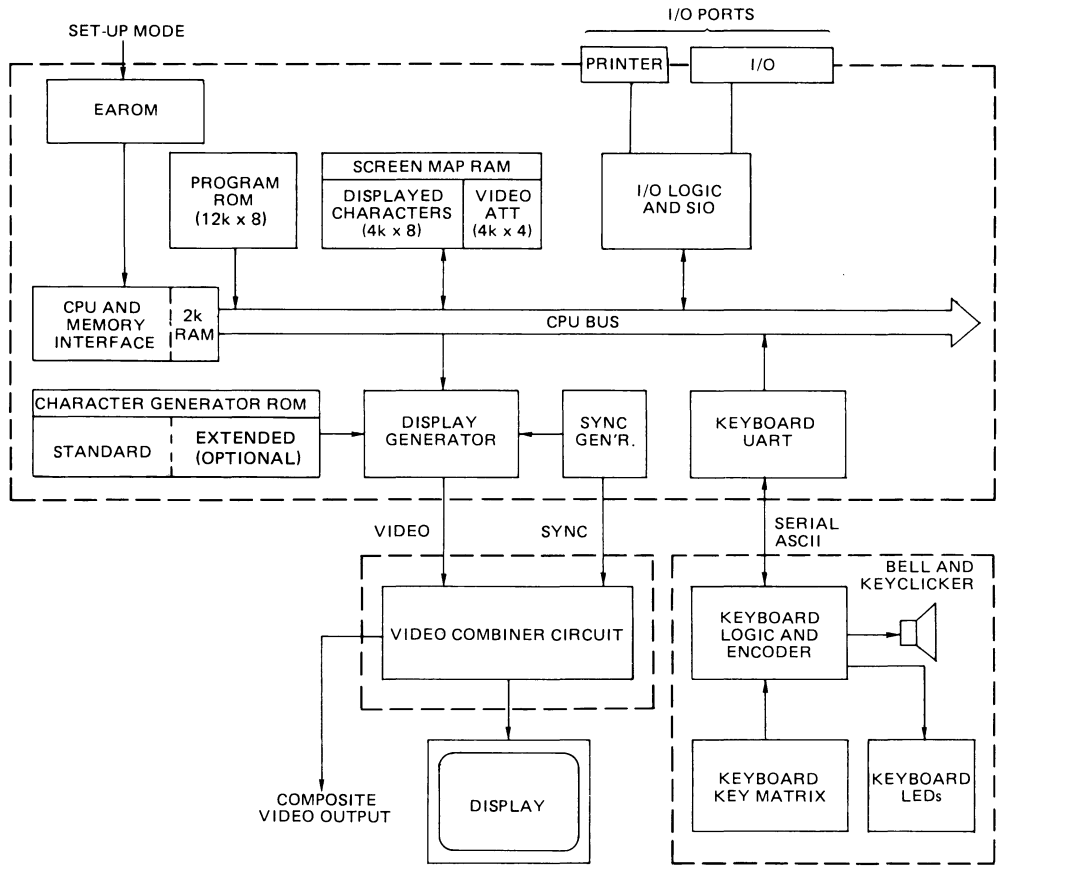


FIG 7.1 Functional Block Diagram

7.1 MICRO-PROCESSOR CONTROL UNIT

Familiarity with microprocessor terminology and procedures is necessary for understanding this section. Specific knowledge of the Z80A processor is desirable but not absolutely essential.

The Facit 4431 uses a Z80A microprocessor (D42) to control all terminal operations based on the instructions contained in the program EPROMs (D73,74,75). The processor has access to all memory and I/O mapped devices on the bus, including the 2k scratchpad RAM (D72), the Z80 SIO (D48-DART-)and CTC (D50) (see section 7.5), the EAROM (D63), various hardware latches, and under control of the bus arbitration circuitry, the display refresh RAM (D51,52) and the attribute RAM (D68,69,67 and D66).

Address decoding for all devices exept the program EPROMs and display refresh memory is provided by D36 (write) and D15 (read). Address decoding for program EPROMs is described in section 7.1.3 , and decoding for the display refresh RAM is described in section 7.2.

7.1.1 CPU CLOCK

Crystal B3 and D9 (a 74LS00 NAND gate) are used to generate the 4MHz., 50% duty cycle system clock signal for the microprocessor and the other Z80 family chips. Transistor V101 provides an active pull-up for the clock by taking the normal TTL level (which ranges from 3.6 to 4 volts) and pulling it up to full 5 volts, while maintaining the standard TTL rise time. (Z80 family chips other than the processor are discussed in section 7.3 of this manual.)

7.1.2 POWER ON RESET

During power up it is necessary to hold the reset pin of the Z80 family chips at the logical 0 level until the 5 Volt power supply is stabilized to insure that the microprocessor begins executing instructions at address 0, and that the Z80 peripheral chips are reset to a known state. After the 5 volt supply has stabilized, this reset line must rize cleanly.

The reset circuit consisit of capacitor C1 (22uF), charged through a 22k resistor (R24), diode V1, and D17. The votage across C1 is coupled to a noninverting CMOS gate D17 through a 12k resistor (R22). The output of gate is fed back to the input through a 82k resistor (R23), which guarantees that the circuit will not jitter when passing the switching threshold (which is approximately half the power supply voltage for CMOS). Diode V1 quickly discharges C1 to ensure that the processor will go through its reset procedure and start up at address 0 in the event of a brief power failure.

7.1.3 PROGRAM MEMORY ACCESS

The design of Facit 4431 allows the use of either 2732 or 2764 EPROMs for the Z80 program memory, resulting in a maximum of 24k when 3 2764s are used. Program memory decoding is accomplished in D17, which is enabled by D34-11 (the OR of read and memory request). Address line A15 allows the processor to access program memory when low, or to access the screen refresh RAM when high.

7.1.4 SCREEN ATTRIBUTE LATCH

Octal latch D64 is used to write data and control information to the EAROM (see section 7.1.5) and to latch data that controls the display attributes. When the screen saver feature is enabled and approximately 9 minutes have elapsed without reception of data from either the host or keyboard D64-16 will go high to blank the display. The level of D64-19 selects either 80 or 132 column mode (low=80). Finnaly, D64-2 is used to kill interrupts as discussed in the Synch Generator portion of this manual (Section 7.4).

7.1.5. EAROM

In the Facit 4431, operational characteristics which are defined in most other terminals by switches or jumpers are selected in Set-Up Mode and are saved from one operating session to the next in the EAROM D63. The EAROM is accessed during power-up, terminal reset, and when a Save or Recall Set-Up Features operation is performed. At all other times the EAROM is in the standby mode with pins 6, 7, 8, and 9 at 12V potentials. All data and control information from the CPU is latched in D64 and passes through the open collector gates of D65, which, through the pull-up resistors of R34, provide the additional current required by the EAROM. The control lines D63-7, 8 and 9 select the read/write address/data modes of the EAROM.

The EAROM contains one hundred 14 bit words which are accessed serially through pin 12. During any EAROM access operation (read, erase, or write) a 14KHz clock signal appears on pin 6 and control signals on pins 7, 8 and 9. Due to the critical timing constraints of the EAROM, the CPU must suspend all other operations while generating the clock, data and control signals. To insure that non-maskable interrupts are disabled, the CPU latches a high to D64-2 for the duration of the EAROM access. EAROM read/write operations access the entire device address space and take about 2.5 seconds for a read and 6.5 seconds for a write. The data last written to the device is retained when power is removed Transistor V105 guarantees that the -23 Volt supply is removed in sequence before the +12 volt supply to protect the EAROM during power-down.

7.2 DISPLAY REFRESH MEMORY

The Facit 4431 was designed to allow the processor transparent access to the display refresh memory when the display is not active. Without this means of resolving potential conflicts between the CPU and the refresh memory circuitry, both could attempt to access the display refresh RAM during the active display interval, resulting in a chaotic display. The Display Access Handle circuitry controls CPU access to the display refresh RAM in the following manner:

The MEMSHARE signal (see Section 7.4.3) allocates one half of each character time to the CPU to access the display memory and the other half to the refresh circuitry. If the CPU attempts to access the display refresh memory during the refresh portion of the MEMSHARE signal the Display Access Handler circuitry places the processor in the wait state until at least one character position cycle is completed, at which time the MEMSHARE signal will again be in the CPU phase. When the Z80 enters the WAIT state, it holds the address, data and read or write lines at the active level until the end of the WAIT state, at which time it completes the read or write cycle.

7.2.1 WAIT STATE GENERATION

The MREQ signal from the processor is inverted in D31 and ANDed with the MI signal so that the output at D32-11 represents an attempt by the processor to access memory other the the program EPROMs. This signal is then ANDed with address line A15 so that the output at D32-3 signifies an attempt by the CPU to access the display RAM. This output is tied to D14-1, which takes shift register D14 out of the load state so that the next CPU clock on D14-2 will cause D14-9 to go low, as the parallel data is serially shifted out. The low D14-9 goes to D32-5, which results in D32-6 going low and placing the CPU in the WAIT state. The low at D14-9 also goes to the D input of the F/F D31-12, which will be clocked with the next rising edge of the MEMSHARE signal to appear at the Q output D31-9. This will force D32-6 low to ensure that the CPU remains in the WAIT state until the CPU portion of the MEMSHARE signal. D14-9 will remain low for three clock periods, until the da-

ta loaded in to the D input D14-14 appears at D14-9. At this point D14-9 and D31-12 are high, but the signal are D32-6 will not go high until the next rising edge of the MEMSHARE signal clocks the data through F/F D31 to D32-4. This synchronizes the end of the WAIT pulse with the rising edge of MEMSHARE, which is the beginning of the next CPU portion of the character time cycle.

7.2.2 WRITING TO THE ASCII (Character) DISPLAY MEMORY

The inputs to D25 (RD at D25-15, WR at D25-1, the AND of A15 and MRQ at D25-13 and D25-3, and A14 at D25-14 and D25-2) are used to decode reads and writes to either the ASCII (character) or ATTR (attribute) display memory. Note that the write ASCII signal from D25-6 is the only signal from D25 to go through some extra gating before proceeding to the memory section. This was done to ensure that write pulse is present only during a specific portion of the CPU part of a character time. As the WR ASCII signal at D25-6 goes low, which is coincident with the WR pulse from the CPU at enable input D25-1, it is allowed through D34 only when the WAIT signal from D32-6 is present at D34-10. This gate ensures that the actual write to the display memory takes place while the processor is in the WAIT state, and terminates synchronously with end of the WAIT state.

Remember that on the rising edge of the MEMSHARE signal (which indicates the start of the CPU portion of the character time) the address multiplexers to the display RAM are switched over to the CPU address bus from the refresh circuit column counters. Also remember that the OK to Write signal (See section 7.4.3) starts low about a third of the way into the CPU portion of MEMSHARE, and terminates as the MEMSHARE signal goes low at start of the refresh portion of the character time cycle. Thus the output at D34-6, which is the OR of OK to Write and WR ASCII, ensures that the address from the multiplexers will have had a chance to properly settle before the write pul se comes along. The signal from D24-2 to D54-11 latches the data into D54, and the output at D34-6 enables the output of the latch. The signal from D34-6 also goes to the write enable inputs of the ASCII display RAM at D51-21 and D52-21 to actually write the data into the RAM.

7.2.3 READING THE ASCII (Character) DISPLAY MEMORY

When the CPU attempts to read the display memory it will be placed in the WAIT state, as explained in section 7.2.2, and the address and read lines from the processor will be held in the active state. At the start of the processor portion of the character time cycle the rising edge of the MEMSHARE signal will switch the display RAM address multiplexers D27, D10 and D13 over to the CPU address bus, and at the end of the CPU portion of the character time cycle the rising edge of MEH SH at D55-11 will latch the data into D55. Since the multiplexers had the entire CPU portion of the character time cycle in which to settle, it is guaranteed that correct data was latched into D55. The processor, however, will not actually read the data from the latch until after WAIT state ends, which occurs on the rising edge of MEMSHARE at the start of the next CPU portion of the character time cycle.

7.2.4 WRITING/READING THE ATTR (Attribute) DISPLAY RAM

Once again, when the processor attempts to access the Display Memory it will be placed in the WAIT state as described in Section 7.2.1, but the attribute data will be immediatly latched into D53 by the WR ATTR signal from D25-7 to D53-11. The upper four bits of the attribute latch D53 are used to control full screen attributes and are discussed in Section 7.3.3. 3. The lower four bits of the CPU data bus, DO-D3, are latched into D53 to set the video attribute of individual characters. As it is ineffecient to write an attribute every time a character is written, the write enable inputs on pin 10 of D68, D69 and D66 and the enable line of tristate octal buffer D71 are tied to the WR ASCII line so that whenever an ASCII character is written into D51 or D52 the attri butes are automatically written into the corresponding location in the attribute memory. Thus the attribute latch D53 need be written to only when an attribute change is desired.

Reading the attributes is done through D70 in 1a manner similar to that for reading an ASCII character from the display memory, as described in Section 7.2.3. The attribute data is placed on the lower four bits of the CPU data bus when RD ATTR signal from D25-9 to D71-19 goes low.

7.3 SYNCHRONIZATION GENERATOR

7.3.1 CRT CONTROLLER (CRTC)

The CRTC D49, allows programming of terminal sync characteristics by loading the controller's internal registers. The registers which controls these parameters are addressed via the address lines AO through A3 and are loaded via the 8-bit wide CPU data bus. The CRTC is selected for loading By D36, the WRITE decoder in the Processor section using the addresses 3000-300F Hex.

Data in the internal registers of the CRTC determines the number of display rows (24 data rows and 1 status row), the number of columns (80 or 132), the number of scan lines per display row (10). The number of scan lines per frame is altered for 50 or 60 Hz.

After initialization of the CRTC on power up, positive horizontal sync pulses, with duration of about 8 microseconds, will be visable at D49-15 every 64 microseconds. Positive vertical sync pulses, with a duration of about 200 microseconds. appear at D49-11. The data row counter outputs (DR0-DR4), the character counter outputs (H0-H7), and the scan counter outputs (R0-R3) are generally not used for displaying the characters on the screen. However, some of these signals are used in generating the non-maskable interrupt at the appropriate time as described in Section 7.3.4.

7.3.2 DOT OSCILLATOR

The Dot oscillator D8, provides timing information for the video portion of the Facit 4431 a 9.828MHz oscillator is used in 80 column mode and a 14.976MHz oscillator in 132 column mode. The appropriate oscillator is enabled by D5-6, whose input is determined by the MSB of data word written into the octal latch 74LS273 D64,(see Section 7.2.4 for details about writing to this latch).

The buffered output at D23-6, is the basic dot clock for the video section, and is passed as the input to the modulo 12 counter D4. Since each character is six dots wide a jam pulse is caused to occur every sixth dot by ANDing the A (pin12) and C (pin9) outputs of the counter in D33-9,10, this pulse is then chopped to one half its width by the dot clock in D7 and the output is used in the video generator section for single and double width character display.

Since in the double wide character mode this pulse is required only every other character position, D7-11 is inverted by D45 and gated with the LSB of the column counter D28-14, in D7-9,10. Thus, at D7-8, we have a negative going pulse one dot wide for every chararcter position.

In addition to the selection of the proper oscillator, a change between 132 and 80 chararcters per row requires a different set of parameters to be loaded into the CRT controller, which is handled by the terminal firmware.

7.3.3 MEMORY SHARE SIGNAL

The screen refresh memory is accessed in a transparent manner. This requires that one half of the character time be devoted to CPU access, and the other half to the refresh memory circuitry. To synchronize the various events, a signal called "MEMSHARE", (MEMSH & MEMSH(L) on schematic),is generated which acts as the basic character clock for the CRTC. One cycle of MEMSHARE has a duration of six dot clock cycles and is generated as the output of D5-12, which is the inverted (A and B) or C signal of the A, B and C outputs of the 7492 counter D4. The inverted MEMSHARE (MEMSH(L) signal at D20-3 is used in reading the ASCII data and attributes from the display memory.

The rising edge of the MEMESHARE signal selects the address multiplexors D27, D10, and D13 to enable the CPU to access memory. At the same time it increments the column counters D28, D11 and D12 in preparation for displaying one scan line of the next character on the screen.

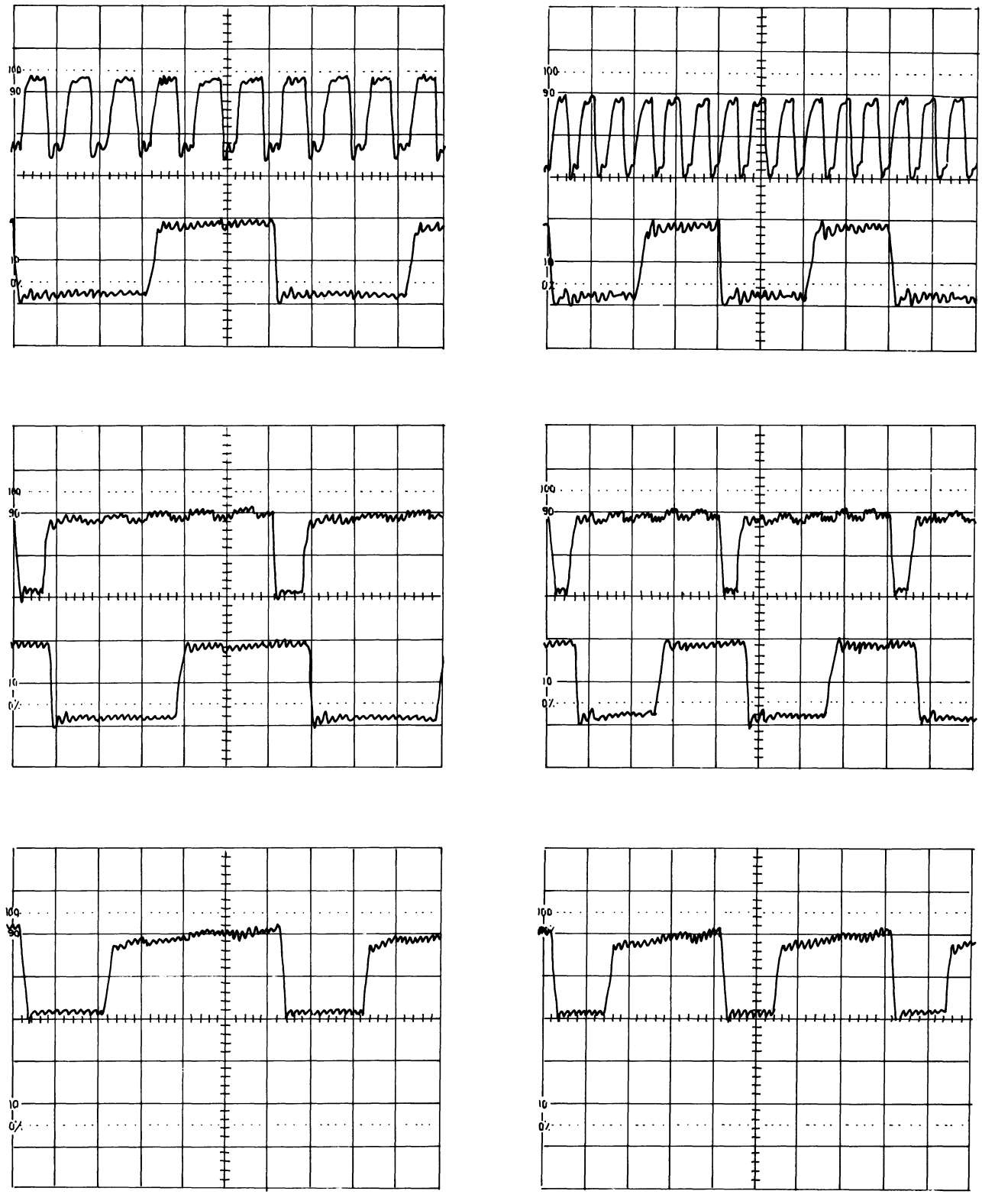
Since the CPU and the MEMSHARE circuitry are operationg with two entirely different clocks, any attempt by the CPU to write to the display memory while the multiplexors are switching over should be prevented. For this reason a signal called OK TO WRITE (OK WR) is generated which will restrict CPU access to the memory to the proper time intervals.

The divide by 2 output of the modulo 12 counter D4-12, is used as the clock signal for double wide characters and in generating the OK WR signal.

The OK WR signal is generated as the Q NOT output of the F/F D3. When this signal goes low it allows the processor to write to the RAM memory. The MEMSHARE signal keeps the OK WR signal high during the refresh portion by keeping the F/F in reset state. This signifies that the display RAM is inaccessible by the CPU during the refresh portion of the MEMSHARE signal. When the MEMSHARE goes high indicating CPU access, the OK WR goes low only after one dot clock delay (one third into the CPU portion of MEMSHARE). This delay ensures that the multiplexers will have enough time to switch over.

Note, Section 7.2.4 describes how this signal is used with the CPU for writing into the display memory.

Fig 7.2 illustrate the timing signals derived in the sync generator circuitry.



80 column mode

132 column mode

VERT: 2V/cm
HORIZ: 100ns/cm

FIG 7.2 DOT OSCILLATOR, MEM SHARE, AND RELATED SIGNALS

7.3.4 NON-MASKABLE INTERRUPT

To make the display as versatile as possible, the processor updates the row start address for every character row, each character row has 10 scan lines, and consequently a NON-MASKABLE INTERRUPT (NMI) is generated every 10 scan lines. If smooth scroll is selected, and a scrolling window is defined, extra NMIs may be required.

7.3.4.1 Non-smooth scroll or full screen window

The vertical sync pulse is used as real time reference in updating the display. Therefore, upon power-up, the processor looks for the vertical sync pulse, which is read in through the latch D43. Once the Vertical sync pulse position is established the processor will be ready to process the NMIs. To avoid the possibility of the processor having to process the NMI before the vertical sync is established, the NMI is disabled by the signal KILL INT at D20-5 which is set high by writing to the EAROM latch D64. When the vertical sync is determined this signal is removed, enabling the NMI.

The negative going vertical sync pulse appears at D5-8. It is ANDed with the carry pulse from the scan line counter D21-12 in D7. This ensures that whenever the refresh memory is scanning the 10th scan line of any character row, the processor will be ready to update the row address, and also loads D30 with information about wheter the row needs to be blanked, if it is a double wide or high row, and if it is the TOP or BOTTOM half of the row. Incidentally, this also loads information about the extra interrupt used in case of smooth scroll which is described in Section 7.3.4.2.

The column counters are loaded with the row address values whenever the Blank signal from the CRTC is active, which indicates the screen is in the retrace period. This resets the column counters to address of the first character position on the row for every scan line and the column counters count up to the last column on the line. When the register D30 is loaded with four bits of information from the data bus, the other four bits are used to load the scan line count into the 74LS192 (D21) in the Video Generator section. In the case of non-smooth scroll this will always be zero.

The new row start address is written during the horizontal blanking period which guarantees that the screen will not be disturbed. When the processor, under software control, has set up the address and data information for D29, D30 and D21, a WRITE operation is attempted. At this point the 74LS138 (D2), enables the output pin 9 thus resetting the F/F D31 which in turn causes D32-6 to go low and place the processor in a WAIT state. The WAIT state ensures that the address and data lines will have had time to settle, and that the new row start address is not written before the horizontal blanking interval at the end of scan line 10.

The WRITE pulse appears at D36-9, and after buffering in D24 is gated with the BLANK signal delayed by two character times in D23-9,10. It then emerges at D23-8 as the write pulse that strobes the scan line counter D21-11, and the registers D30-11 and D29-11 latching the new scan line count and the row start address. The horizontal blanking pulse is generated at D49-17 as a positive going BLANK SIGNAL and is latched into the octal latch D46-17, by the character rate clock MEMSHARE signal. The output of the latch D46-16 is the BLANK signal delayed by one character time and is gated with the BLANK signal at D22-1,2 to load the column counters D12, D11, and D28 in the sync. generator circuitry with the new row start address.

The BLANK pulse delayed by one character time, is also used as an input to the octal latch D46-17 to generate a BLANK signal that is delayed by two character times at D46-19. This signal is used to gate the write pulse at D23-9 and also to disable the line decoder D16. Thus the output D16-9 will go high and remove the reset from F/F D31, and the rising edge of the next MEMSHARE pulse will terminate the WAIT state.

Figure 7.3 shows the various BLANK signals, the write row start register signal and the load column counter signal.

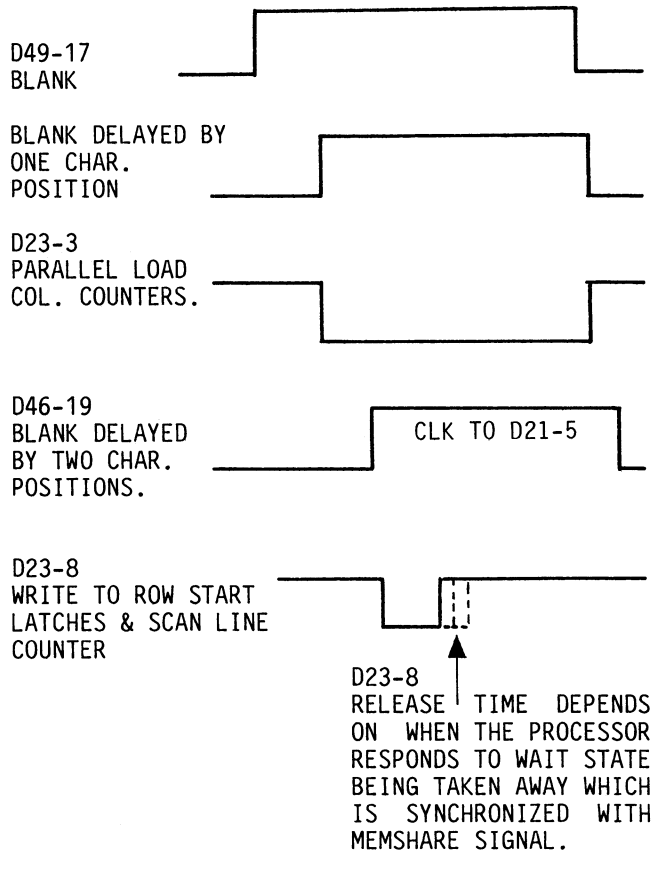


FIG 7.3 SIGNALS GENERATED DURING BLANKING

7.3.4.2 Smooth scroll or scrolling window

The Facit 4431 has two smooth scrolling speeds, fast and slow. In a slow smooth scrolling operation the character rows within the scrolling window are shifted upwards or downwards by one scan line once during every refresh cycle. (A refresh cycle is the period from one vertical sync pulse to the next.) In fast smooth scroll the character rows are shifted by two scan lines during each refresh cycle. If the operator has not explicitly defined a scrolling window, then the entire screen is, in effect, a scrolling window.

In the first screen refresh cycle of as smooth scroll operation the first scan line of the scrolling window will display the data from the second line of the chararcter row (slow speed). Recall that the scan line counter D21 generats an NMI during the 10th scan line of each character row, and that this interrupt allows the CPU to set the scan line count and row start address of the next character row. Thus, at the start of the scrolling window, the processor sets the scan line counter D21 to display the second scan line of the character row.

Since the scan line counter D21 only generates a carry on the 10th scan line of each character, and the last scan line of the scrolling window is now the first scan line of a new character row, it is necessary to generate an extra nonmaskable interrupt. This extra interrupt is needed so that the CPU can set the row start address and scan line count of the first character row below the scrolling window. Since the scan line counter outputs of the CRT Controller are referenced to the start of the screen and not the start of the scrolling window, they are used to decode the end of the window. Thus, the CRTC scan line outputs at D49-4,8 are ANDed in D6-12,13 to decode scan line 10, and the output at D6-11 is ANDed with the extra interrupt enable signal at D6-1,2 so that the output at D6-3 will generate the extra NMI. (The extra interrupt enable signal comes from D30-19, and is set by the processor when smooth scroll is enabled.)

The Q outputs of the F/F D3 controls whether or not interrupts are let through to the processor. Since the vertical sync pulse must always be allowed to generate NMI, the vertical sync pulse presets F/F D3. As interrupts from the scan line counter would normally occur at the very beginning of a scan line, the processor would be forced to waste a relatively long time in the WAIT state. To improve efficiency, therefore, F/F D3 is used to delay the interrupt towards the end of the scan line. The F/F is set to enable the interrupts when the column count reaches 64 if 80 column mode and 96 if in 132 column mode.

When in 80 column mode D17-13 is high and the column count of 64 from D49-32 passes through D34-2 to clock the F/F. When in 132 column mode D17-13 is low, disabling the D17-11 from clocking the F/F. When the column count reaches 96, D17-8,9 gate a high at D17-10 which clocks the F/F D3. Note the the F/F is reset by the twice delayed blank signal.

7.4 VIDEO GENERATOR

The Video Generator (VG) circuit receives parallel data from the memory (M) and the Sync generator (SG) circuits and generates both a composite video output signal to drive an external monitor (optional features) and a direct drive signal to drive the internal 12" (diagonal) data display monitor.

7.4 1 CHARACTER FONT

The display may be sectioned into 24 rows of either 80 or 132 columns of basic character cells and a 25th status row of either 80 or 132 character cells.

The basic cell is illustrated below in Fig 7.4.

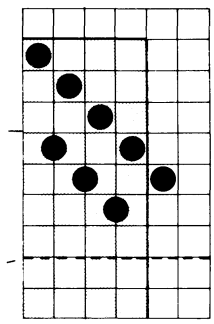


FIG 7.4 BASIC CHARACTER CELL AND EIGHT INDEPENDENT DOT LOCATIONS

The basic cell is six dots wide by ten dots high. There are eight horizontal positions where dots may be placed. Note that three of these eight positions lie on half-dot boundaries and the rightmost position extends for two dot widths into column 0 of the next cell to the right. Columns 4 and 5 are normally blank to allow horizontal spacing between characters, but as will be seen later, these columns may be filled if continuous horizontal lines are to be drawn. Rows 8 and 9 are used to display decending lower case or underlined characters and the line cursor.

Eleven bits are required to address the character (seven ASCII data bits and four bits for the character scan line 0-9) to be displayed. The octal latches D41 and D46 provide the seven ASCII code bits and multiplexer D18 provides the four scan line number bits. These address lines to the character generator ROM are summarized in table below.

SOURCE		D40 PIN NUMBER
ASCII BIT (DM0)	D41-9	8 (A1)
ASCII BIT (DM1)	D41-6	7 (A2)
ASCII BIT (DM2)	D41-5	6 (A4)
ASCII BIT (DM3)	D41-16	5 (A8)
ASCII BIT (DM4)	D41-15	4 (A16)
ASCII BIT (DM5)	D41-12	3 (A32)
ASCII BIT (DM6)	D46-5	2 (A64)
SCAN LINE 1 (S1)	D18-4	1 (A128)
SCAN LINE 2 (S2)	D18-7	22 (A512)
SCAN LINE 3 (S3)	D18-9	19 (A1024)
SCAN LINE 4 (S4)	D18-12	23 (A256)

Table Character generator addressing

An example of how a particular character's dot pattern is stored in the character generator ROM is illustrated in table below for the letter "A".

SCAN LINE	D40 ADDRESS	DATA	DOT PATTERN
0	041 Hex	00 Hex	....
1	0C1	10	...**.....
2	141	28	..****....
3	1C1	44	.**..**...
4	241	82	**....**..
5	2C1	AA	********..
6	441	82	**....**..
7	4C1	82	**....**..
8	541	00	....
9	5C1	00	....

Table Character Generaetor Data for "A".

7.4.2 DISPLAY SEQUENCING

The character clock period (610nS in the 80 column mode and 410nS in the 132 column mode) is not sufficient to look up the ASCII character in the refresh memory, to use it as the address for reading the video data from the character genera tor D40 and load this data into the video shift registers D39 and D38. To provide enough time to accomplish the lookup sequence, the ASCII character is read from the screen refresh memory say at character time 0, during the refresh portion of the memory character cycle (when the MEMSHARE signal is low). At the end of that half cycle, the character is latched along with the attributes associated with that character into the octal latches D41 and D46.

During character time 1, the sixth dot pulse generated in the sync. generation circuitry loads the character dot information into the video shift registers D39 and D38. During character time 2, this information is shifted out for a particular scan line of the character and is displayed on the screen.

This type of sequencing is reminicent of a bucket brigade since the character generator is always looking up the data for the next character to be displayed (i.e., it is always one character ahead of the video beam) and the display RAM is accesing data for the second character to be displayed after the present one (i.e., it is two charcters ahead of the video beam).

Figure 7.5 illustrates this process. Suppose the beam is passing through scan line 1 of the letters ABC and the cursor is positioned over the character C. Assume the shift register is shifting out the second scan line information for the letter A which is found to be 10 Hex from Table above (The character generator contents for the second scan lines of letter B and C are AC and 2C Hex respectively). The sixth dot pulse generated when the beam finishes scanning this scan line of the letter A, loads the dot pattern for the second scan line of the letter B (AC Hex) into the shift register while simultaneously loading the ASCII code for the letter C (43 Hex) and the associated cursor and attribute information into the octal latches D41 and D46.

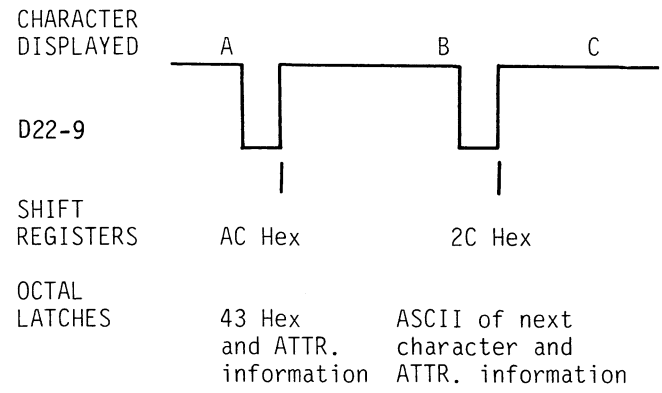


FIG 7.5 DISPLAY SEQUENCING

When the code 43 Hex appears at the outputs of the latches along with the cursor and attribute information, the character generator ROM begins looking up the dot pattern for the second scan line of the letter C (2C Hex). This dot pattern data will be loaded into the shift register when the beam passes through the sixth dot in the second scan line of the letter B. Also the ASCII code for the next character on the screen will be loaded into the octal latches.

7.4.3 DISPLAY TIMING GENERATION

The display timing generation for the videogenerator section begins at the sync generator with the dot oscillator and the sixth half dot jam pulse. The dot clocks and the jam pulses are multiplexed in D22 to select one set of signals for the single or double wide character mode.

7.4.3.1 Single wide characters

The "A, 0" inputs are selected for the multiplexer in case of single wide characters. The dot clock from D23-6 is given to D22-14 and the output D22-12 drives the video shift registers. The sixth half dot jam pulse from D7-11, which occurs every character cycle is input to D22-11 and the corresponding output at D22-9 is used as the parallel load input to the shift registers.

Note that the shift clock to these two parallel to serial shift registers D39 and D38 are inverted. Four bits of the character generator D40, go to D39 and three interleaved bits go to D38.

It is to be noted that the rising edge of the load pulse is synchronized with the falling edge of the shift clock for D39 and therefore, there is a half clock time before data is shifted out. Also, D39 is the first one to shift out data and half a dot clock later D38 is shifted. This implements a half dot shift in the character composition.

7.4.3.2 Double wide characters

For the terminal to produce double wide characters, the dot rate clock must be divided by 2 and where, in single wide characters, the jams came every 610nS (80 column mode) or 410nS (132 column mode) respectively, they must now occur every 1.22 microseconds or 820 nanoseconds. The double wide characters mode is selected by writing to the latch D30. The Data bus bits D37 and D39 determine double wide characters and these bits are ORed in D20-9,10. The output of D20-8 is used to select the A0 or A1 inputs to the multiplexer D22. The A1 set of inputs are enabled in the case of double wide characters.

The half dot clock frequency signal from D4-12, is used as the clock input to the multiplexer at D22-13; the jam pulse is needed only every other character cycle and this signal is obtained from D7-8 and is input to the multiplexer at D22-10. These signals follow the same gating as in the case of the single wide characters. As a result, the data in the shift registers takes twice as long to clock out in double wide mode as in single wide mode, resulting in double wide characters.

7.4.3.3 Double high character

The scan line circuitry uses two normal character rows (two screen memory locations per character) to produce the complete double high charcters. The operation of the scan line counter D21 is discussed in the sync generator portion. Since the operation of the 4431 requires characters to be double high double wide, or single high double wide, the scan count outputs of the 74LS192 (D21) have to be modified to allow the double high characters to be formed.

The outputs of D21 go to the address inputs A1,A2 A4, and A8 of D19 the 74LS288 bipolar ROM. The A16 input D19-14, can be considered as the double high input. This signal comes from D35-3, which is selected for double high operation by writing to D30.

When single high characters are being formed, the outputs DO through D3 (pin 1,2,3,4) of D19 are mirrored by the outputs D37 through D18 (pin 5,6,7 and 9). Also, these are one to one correspondents of the outputs of D21. If double high characters are selected by a logical 1 at D19-14 the DO through D3 outputs of D19 follow the outputs of D21 at half the rate. Therefore, if the DO through D3 are allowed through the multiplexer D18, to the character generator, only the top half of a character would be displayed over the entire 10 scan lines of row space. If the select input of the multiplexer D18-1 is pulled high by D30-15, to display the bottom half of the character, then, outputs D4 through D7 are allowed through D7 which translates the D9 outputs from count 5 to 9 over the 10 scan lines.

7.4.3.4 Effect of the attribute bits

The serial outputs of the video shift registers at D39-9 and D38-9 are ORed together in D44-4,5 and the video output at D44-6 is modified by the various attribute information.

Four video attributes are supported by the 4431, viz., REVERSE VIDEO, INTENSITY, BLINK, and UNDERLINE on a character by character basis. This information is retrieved from the Refresh Display Memory and is latched into D46. This information forms a part of the address to the attribute PROM D13.

Another set of inputs to this PROM consists of the screen attributes, viz., SCREEN BACKGROUND which determines whether dark or bright background is in effect, CURSOR TYPE which selects line or block cursor, CURSOR BLINK which blinks the cursor at the selected frequency, and the CHARACTER BLINK which blinks the character at the selected frequency. These attributes are written to the latch D54 by the processor and the outputs of this latch form a set of inputs to the attribute PROM.

To display the Underline for the displayed character, scan line 8 is decoded from the scan line multiplexer D18, using the AND gate D37 (D37-11=LINE 8) and is fed to D57-22.

The cursor bit which originates from the row and column comparators within the CRTC is latched in to D41 and becomes an address for the Attribute PROM. The Attribute PROM acts as a large combinational circuitry and outputs five bits of information based on its inputs. These attributes form the inputs to the Attribute latch D58. These attributes are latched in when the jam pulse loads the parallel data into the video shift registers.

The video signal coming out of D44-6, is exclusive ORed with the reverse video bit in D35-9,10 to allow any particular bit of information to be reversed out on a character by character basis. The underline or reversed screen blanking output of the attribute latch D58 determines whether the video signal at D35-8 is to be unaltered or made completely white.

The use of reverse screen blanking is as follows:

In SETUP modes only a few rows of information on the screen (top and bottom rows) are saved by the firmware. This requires that the center rows of the screen be undisturbed and also blanked out so that they are not visible. If bright back ground is selected by the user, it is necessary to white out the center portion of the screen. The reverse screen blanking signal is used to achive this. Also if an underline is required, scan line 8 needs to be whitened out and the att ribute PROM will set the underline attribute at the appropriate time.

The video signal that emerges from the OR gate D44-8 goes to three open collector NAND gates D60, to provide three levels of video signal intensity. All of these gates are combined with the blanking signal coming from D58-5. This blanking signal is the OR of retrace blank signal which is required to blank out the screen during screen retrace periods, and the Video blank signal which comes out of the attribute PROM D57-13 whenever a row of data or the whole screen needs to be blanked.

The blinking bit out of the attribute latch is combined with one of the three NAND gates and when this gate is turned on its output goes low along with the video signal and provides a more intense picture. The bottom NAND gate, (D60-1, 2, 13), is gated with the intensity bit, but in a non-blinking fashion such that when turned on, causes the video to be constantly brighter.

When the cursor bit is active (D57-23), the cursor blink bit is active (D57-3), and the display is in scan line 9 (D57-22) or some other row with block type cursor selected (D57-4), the reverse video output D57-9 becomes complemented to effect a blinking reverse image cursor.

7.4.3.5 Retrace blanking

During retrace the screen must be blanked to black while data continues to emanate from the character generator memory D40, and shift register D39, and D38. The blanking output at D49-17 representing both vertical and horizontal blanking is buffered through D46 and then through D35.

The blank output at D2-11 is ANDed (D37-1,2) with the LSB data out of the character generator. This data bit D0 is the extension bit of the line drawing set which runs into the next character so that continuous horizontal lines may be drawn. This bit passes through to the shift register during non blank periods but is masked during blanking so that this random bit will be loaded into the shift register D39 and thus appear in the first dot position of the first character after blanking.

This line drawing input extends into the next character position as its output occurs at the first clock position before jam of the new character at D39-9. This output is looped back to the first parrallel input D39-6, so the output is jammed in and displayed once again at the beginning of the new character position.

As explained above, the blanking signal also comes out of the attribute latch and forms an input to all three NAND gates D60 to completely shutdown video during retrace. To keep the edges of the display absolutely uniform, it is necessary to reset the attribute latch D58 during horizontal and vertical blanking periods. This is done by the OR gate D44-3 when the load pulse to the shift registers clocks the blank attribute into D58 while the other input D44-1 remains low. The reset is released when blanking is over synchronously with the MEMSHARE signal. At the same time the jam pulse loads the last random attributes into D58 but the blank output at D58-5 is still low insuring that the random data will not be displayed.

7.4.3.6 Brightness control and video output

To allow for keyboard control of brightness and to set the brightness value stored in the EAROM, the octal latch D56 is used which drives the buffers D59, terminated with approximately binary weighted resistors. These are paralleled in various combinations with R18 to trim the video out voltage to the monitor.

Q2 is wired as a voltage control current source where the voltage across R15 sets the current dumped into R18 and binary weighted resistors. As the voltage across R15 is greater, the video level is brighter and as the resistors R8, R10 and R9 come on, the video level is made brighter by pulling the non emitter end of R14 further toward ground.

V103 is wired as an emitter follower which combines the video signal from the collector of V102 with the composite sync from D59-2 to generate the composite video to drive an external monitor.

7.5 INPUT/OUTPUT INTERFACES

The Facit 4431 I/O interface utilizes an Z80A - DART (Dual channel Asynchronous Receiver/Transmitter) D66, in conjunction with a programmable clock generator D65 and D76, a Line Driver D74, a Line Receiver D75, Transistor V108 to provide two independent serial data channels and keyboard UART D58 with baud rate generator D57, KBD Line driver D73/D70 and KBD Line Receiver V104/D73. The primary channel is dedicated to communication with the host and is labeled the I/O port (X1). The second channel allows communication with a local printer (X2). Keyboard communication is through a coiled cabel from connector X3 to the external keyboard. The Z80A receives vectored interrupts from the DART when I/O operations require service.

7.5.1 BAUD RATE CLOCK GENERATION

The 4MHz CPU clock is divided by 13 in D76 and the resulting 30.8KHz signal at D76-7 goes to the clock inputs D65-21, 22, 23 of the Z80A CTC (Counter Timer Circuit). The CTC provides separate baud rate clocks for the transmit and receive functions of the I/O channel and one baud rate clock for both the transmit and receive functions of the printer channel. Also, D76-7 goes to the divider D57 and the output D57-3 is used as keyboard communication baud rate clock. The CPU programs the CTC to generate the proper baud rates as selected in the SET-UP mode. All three clocks oscillate at sixteen times the desired data rate. The I/O transmit and receive clocks are connected to channel A clock inputs of the DART at D66-14 and D66-13 respectively. The printer clock is connected to the channel B clock input of the DART at D66-27.

The CTC D65 is also programmed by the CPU to generate interrupts at 8msec intervals which the CPU uses as a real-time reference. It should be noted that the interrupt priority structure established by the connection from the IEI (Interrupt Enable Input) at D65-13 allows the DART interrupt to be processed before the CTC interrupt.

7.5.2 DART OPERATIONS

The Z80A CPU determines the proper data format (data bits, stop bits, parity, word lenght, etc) from the Set-Up mode soft switches and programs the DART for these characteristics. The DART then takes care of all parallel/serial data conversion and data formating. Data to be transmitted is stored in a 128 character buffer and received data is stored in a 256 character buffer which are controlled by the CPU. TTL to RS232C/V24 level conversion is provided by D74, and RS 232C/V24 to TTL conversion is performed by D75 and V108.

7.5.3 KEYBOARD COMMUNICATION

The keyboard communication is controlled by CPU through the UART D58. The parallel to serial and serial to parallel conversion and data formating is taken care of by the UART. The UART transmits and receive data to/from the keyboard using standard RS232C/V24 formating (8 data bits, no parity, 2 stop bits) no protocol is used and the baud rate is 300 baud. D57 is a frequency divider and D73 is a Transmit/Receive buffer, D70 is used as a line driver and V104 as line receiver.

8 MONITOR AND POWER SUPPLY

8.1 GENERAL

The video monitor assembly consists of the video electronic board, the display tube, and the power supply unit. The monitor assembly is serviced by replacement of the entire assembly.

8.2 MONITOR

Electrical Design

The horizontal sync, vertical sync and video signals from the Main Logic Board drive the horizontal, vertical and intensity modulation circuits on the video board to produce a non-interlaced raster display on the CRT. The display area is defined as a rectangle 8" wide by 6" high in the middle of the screen to minimize distortion and ensure optimum resolution. The circuit is conceived to operate with a 12 Volt power supply.

It consists of:

- an IC for the horizontal processing (TDA 1180P 5IC2)
- a split transformer for the horizontal output
- an IC for the vertical processing (TDA 1170 S 6IC2)
- a focusing voltage modulation circuit

Performances:

- picture tube with "non-glaring" treatment
- green phosphor P42 C with medium short persistence (300uS)
- size of the picture 8"x6" +/- 0.2"

Input voltages:

- Video min 1V to max 2V (positive)
- Hor.sync. pulse between +2.5V and +5V
- Frequency 15 700Hz +/- 500Hz
- Vertical sync. negative going between 2V and 5V
- Frequency 49Hz -- 61Hz
- Supply voltages 12V approx 1A

Adjustments:

- Focus
- Vertical Amplitude
  Linearity
  Frequency
- Horizontal Frequency
  Phase
  Amplitude
  Linearity
- Brightness (black level adjustment)

8.3 POWER SUPPLY

Electrical design

- The circuit operates with a SMPS at 25kHz (approx)
- The switch processor is from SIEMENS (TDA4600)

Performance

- Input voltages 220V 49-61Hz
  (Jumper select) 117V 49-61Hz
- Regulation range 187V --- 264V
  100V --- 135V
- Output voltages and currents:

+5V	+/-0.3V	2.5A (for the Logic)
+12V	+/-0.2V	0.3A (for the Logic)
+12V	+/-0.6V	1.0A (for the Monitor)
+17V	+/-1.5V	0.25A (for the Keyboard)
-12V	+/-0.6V	0.10A (for the Logic)
-23V	+/-1.5V	10mA (for the EAROM)

- All outputs are overload and short circuit protected
- Operating frequency is 20kHz --- 70kHz depending on the load
- Output power 35W max.
- Efficiency approx 70%
- Mains current 0.3A RMS
  8.0 during on

Adjustments:

- The output voltages are adjusted on the +12V 0.3A line by a potentiometer. See Chapter 9 Troubleshooting and Repair for details

Mains Voltage conversion

- In order to convert between 117 and 220V AC operation, a jumper on the power supply circuit board is provided. See power supply assembly drawing for visual aid

9 SERVICE

9.1 TROUBLESHOOTING AND FAULT ISOLATION

This section suggests methods for determining which circuit is faulty in a malfunctioning unit. The primary objective is to determine which subassembly (Main Logic Board, Keyboard, Power Supply or Monitor) is faulty.

9.1.1 POWER-UP SELF-TEST

Upon Power-Up, the 4431 tests the program EPROM 's EAROM, processor scratchpad RAM, and the display refresh memory. If the terminal halts with the LEDs on, then the processor has determine that the scratchpad RAM D72 is defective and no further tests are attempted. If any other error is detected, the bell will ring 5 times and an error code will be displayed in the upper left portion of the screen.

ERROR CODES:

1	DISPLAY MEMORY FAILURE
2	EAROM parity error
4	EPROM checksum error

9.2 SUBASSEMBLY DIAGNOSIS

If the Bell rings (beeps two times) when the terminal is turned on then the main logic board is in fairly good shape, for in order to sound the bell the entire processor section must be functional and the +5V logic supply must be operating. If the bell does not sound on powerup then either the keyboard, the power supply or the main logic board is at fault. Also note if the keyboard communication is at fault the Bell will beep four times, this will result in, (after approx. 6 sec. delay) two times two beeps as the keyboard internal test sequence will be turned on.

Should the Monitor fail, one of the following symptoms may be observed:

- no picture, regardless of brightness setting
- a bright horizontal line in the middle of the screen
- a raster at high brightness, but no cursor or characters

9.3 KEYBOARD FAULT DIAGNOSIS

The keyboard perform the following self-diagnostic sequence upon power-up:

If a suspected hardware fault is detected the bell will "quack" five times, the appropriate error code (see table below) will flash at ap-

prox. 10Hz on the LEDs, and the signature analysis routine will be executed continuously.

Except otherwise noted, these diagnostics detect circuit nodes that are effectively shorted to ground potential. In situations where there is more than one possible cause of a fault condition the diagnostic routine displays the error code of the first component tested.

Exemple: In the grid buffer test (Item 3 below) a bad keyboard column driver would have the same effect (as far as the diagnostic routine is concerned) as a bad grid buffer, but since the grid buffer is tested before the keyboard drivers the grid buffer error code would be displayed. The fault can then be located by signature analysis.

TEST PROCEDURE

1 Upon POWER UP all seven LEDs will be lit for 0.5 seconds.

2 A checksum test is performed on the keyboard EPROM (U3).

3 The grid buffer (U5) is tested as follows:

The twelve keyboard drivers are deactivated and the grid buffer is read. If any low voltage levels are detected the grid buffer is faulty.

4 The modifier keys/country select buffer (U6) is tested as follows:

The Shift and Control keys are read in through their buffer. (The Caps and Num keys lock so they are excluded, the country select Nibble is similarly ignored).

If a low voltage level is detected the special keys buffer is faulty.

5 The country/product select code is displayed on the LEDs for at least one second. (See country and product select tables page 3).

6 Initialization is requested from the Main Logic Board. If no response is detected with in 5 seconds the keyboard assumes it is in the test fixture and enters the keyboard test mode. If a response from the MLB occurs within 5 seconds of the initialization request then normal keyboard operation ensures

7 The keyboard test mode is entered only if there is no communication between the keyboard and the main unit, which means that either the keyboard is in the test fixture that has the serial I/O lines tied together or tha the serial I/O lines are faulty.

The bell will ring twice to signify the start of the Keyboard Test Mode. The technician will then type the following twelve character sequence:

X B G L Return O K LINE FEED D J F SET UP

After each keystroke the bell will sound if the grid driver for that column of the keyboard is functioning properly.

Each keybaord column driver (A0 through A11) is sequentially activated and the keyboard is continuously scanned until a key in that column reads. When a key closure is detected the column drivers are disabled and the grid is read again. If a low voltage level is detected the column driver is faulty.

If the bell fails to ring after any keystroke then it is possible that either the column driver or one line (row) of the grid buffer is open. The problem can be localized to the faulty component either by signature analysis or by the following procedure:

Restart the keyboard test sequence by POWER ON/OFF. Choose the keys for the 12 columns from the same grid row. If keys from different column driver ICs fail to ring the bell then the grid buffer line for that row is open. See Schematic Appendix.

8 The ASCII "DEL" character (7F) is sent out over the serial line. If this character with valid start and stop bits is received on the input line then all seven LEDs are lit and the signature analysis loop is executed. If no character or an invalid character is received then the serial I/O driver IC (U7) is faulty.

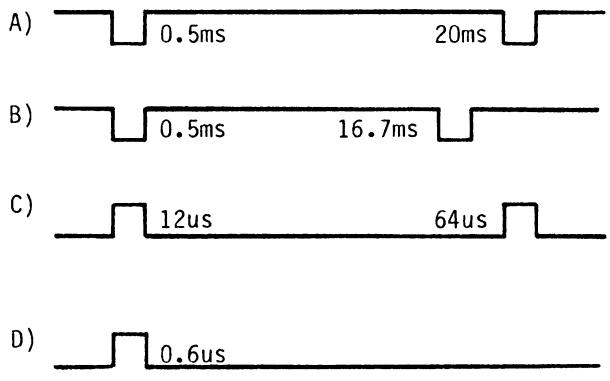
ERROR CODES

(FLASHING)	CAUSE
000 0001	U3 EPROM CHECKSUM ERROR
000 0010	U5 GRID BUFFER ERROR
000 0011	U6 SPECIAL KEYS BUFFER ERROR
000 0100	U7 KEYBOARD DRIVER ERROR
000 0101	U8 KEYBOARD DRIVER ERROR
000 0110	U9 KEYBOARD DRIVER ERROR
000 0111	U7 SERIAL I/O RECEIVER-DRIVER ERROR
(NOT FLASHING)	
111 1111	PASSED ALL DIAGNOSTIC TEST

9.4 TESTING THE MONITOR

For a definite test to determine whether the Monitor or Main Logic Board is at fault, check the Power Supply for +12V and that the signals running from the Main Logic to the monitor through connector X4, see fig below. If these signals are present and no Video or abnormal video is observed, then the monitor control circuit board or the complete monitor should be replaced.

Timing diagram for H-sync, V-sync and Video.



	SIGNAL NAME	LOGIC LEVEL AT X4
A)	V-SYNC 50Hz	X4-1 5V
B)	V-SYNC 60Hz	X4-1 5V
C)	H-SYNC	X4-2 5V
D)	VIDEO	X4-4 appr. 1-2V

If the video and sync signals are not present, check the logic power supply voltages at X3 on the main logic board.

X3-1 +17 Volts
X3-2 +12 Volts
X3-3 -23 Volts
X3-4,5 +5 Volts
X3-6 -12 Volts
X3-7,8 Ground

If these voltages are correct, then the Main logic board is faulty. If these voltages are not correct check the mains fuse, if the fuse is good, then the power supply should be replaced.

9.5 DISASSEMBLY

Before attempting to gain access to the internal circuitry, TURN OFF THE POWER AND UNPLUG THE LINE CORD.

1 There are four slot-head fixing screws which retain the display unit top cover. These are located at the bottom of the cover, under the lip, close to where the stand enters the display unit body. The screws can be accessed from below by means of a short screwdriver. To remove the cover the screws must be screwed IN (clockwise) as fas as they will go.

2 Grasp the lip of the cover on each side, pull outwards and simultaneously lift the cover.

3 Replacement of the cover is the reverse of the removal. The retaining screws must then be screwed OUT (anticlockwise) as far as they will go.

9.5.1 MONITOR REPLACEMENT

The Monitor may quickly be replaced by unscrewing the four retaining screws that fasten it to the cabinet, disconnect the wiring harness from the power supply and the ten pin connector from the Main Logic and remove the CRT assembly by tilting it back and lifting it up carefully. The above operation should be reversed to install the replacement monitor.

CAUTION: When handling a monitor that has been turned on recently (in last hour), care should be exercised to avoid touching the dag or envelop discharge lead. The picture tube is a capacitor and when operating, or recently thereafter this led has a very high voltage on it.

9.5.2 MAIN LOGIC BOARD REPLACEMENT

The Main Logic Board is secured to the rear cover by seven screws.

9.5.3 ACCESS TO KEYBOARD

1 Switch off the unit and disconnect the keyboard from the display unit.

2 Remove the two retaining screw at the right hand end of the keyboard, and then remove the end cap.

3 Slide out the printed circuit board (disconnecting the loudspeaker lead if necessare) and lift off the top plate.

4 Reassembly of the keyboard is the reverse of the above. Ensure that the p.c.b. and top plate slide in the retaining grooves in the keyboard housing.

9.6 ADJUSTING THE MONITOR

The terminal should have been powered on for about 15 minutes before any adjustment is performed, also the +12 Volt to the Monitor should be checked, and if necessary adjusted to +12 Volt +/-0.6 Volt.

Adjustments are to be performed with Video signals at default value (normal Brightness).

- VERTICAL LINEARITY CONTROL

  No character shall vary in height by more than +/- 10% of the average height of all characters in a row or column respectively.

- VERTICAL SIZE CONTROL

  This control is used to adjust the size of the display on the vertical axis. Adjust the Vertical size (height) to 6" +/- 0.2". (This adjustment should be performed in 60Hz mode).

- VERTICAL FREQUENCY

  The Vertical frequency should by adjusted so that the potentiometer is positioned half way between the points there the picture starts to roll.

  Adjustment instructions:

  In SET-UP mode B, set the terminal to 50Hz.

  Move the Vertical Frequency adjustment potentiometer CCW (counter clockwise) until the display starts to roll, note the potentiometer position and change the terminal to 60Hz (in SET-UP B mode) now turn the potentiometer CW (clockwise) until the display starts to roll, note this position and adjust the potentiometer so that it is positioned half way between the points there the picture starts to roll.

- HORIZONTAL FREQUENCY CONTROL

  Adjust the potentiometer so that it is positioned half way between the points there the picture starts to roll.

- HORIZONTAL PHASE CONTROL

  In 132 column mode, adjust the potentiometer CW and CCW so that the display folds over the margins, note these positions and adjust the potentiometer half way between these points.

- BRIGHTNESS CONTROL
  SET UP A mode.

  First reset the terminal to delivery status by typing (SHIFT) and D simultaneously, then adjust the brightness potentiometer so that low intensity portion of the display in SET UP A mode are just visiable.

- HORIZONTAL WIDHT CONTROL

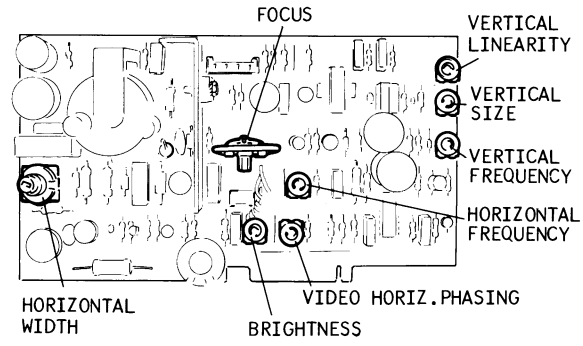
  This control is to adjust the horizontal widht of the display. Adjust the horizontal widht to 8" +/- 0.6".

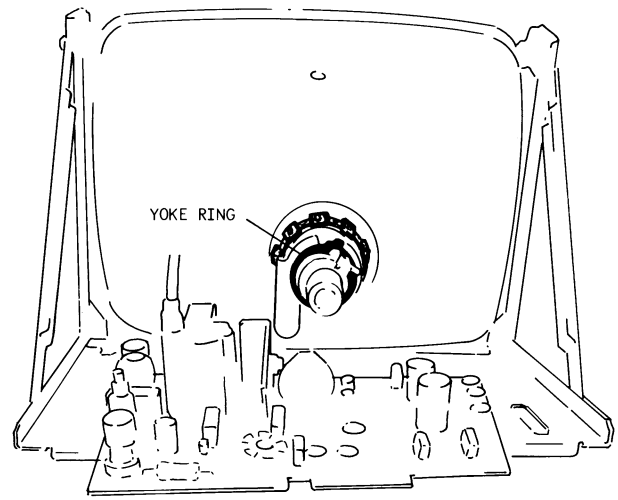
- CENTERING

  The yoke rings are used for centering the display area on the screen of the CRT.

- PINCUSHION

  Rubber magnets to be used to correct the concave lines at outer edges of the display pattern.

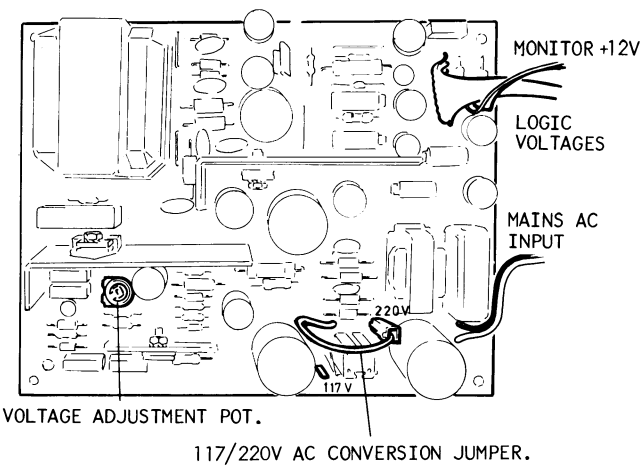




9.7 POWER SUPPLY

The power supply output voltages are adjustable by the power supply potentiometer located on the power supply circuit board.

Use +12 Volt to the monitor at Main Logic Board connector X3 Pin 4,5 as reference when measuring (+12V +/- 0.6V).



9.8 TROUBLESHOOTING BY SYMPTOM

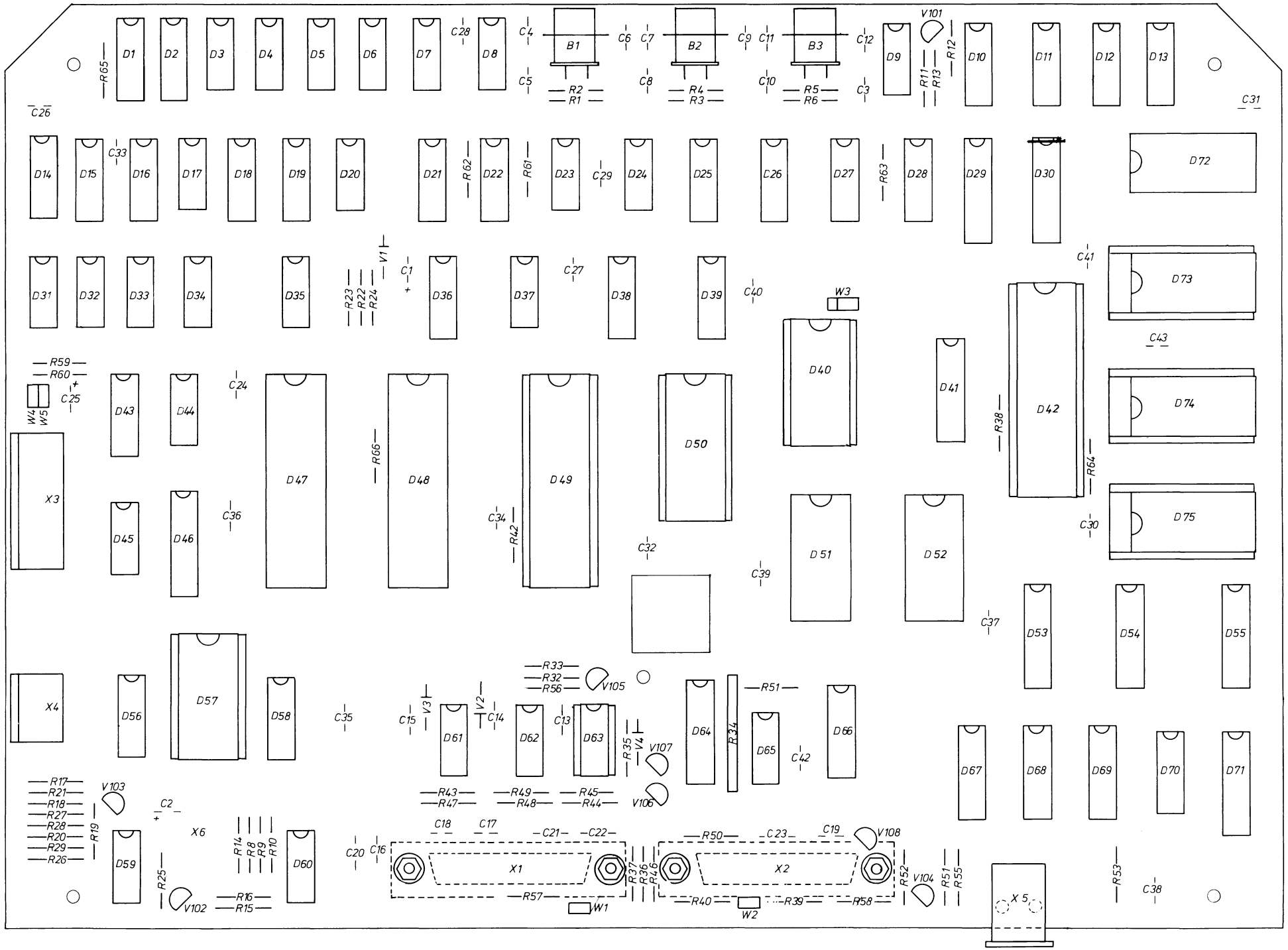
SYMPTOM	CAUSE
High pitched squeal, No terminal function	Check power supply Check 4MHz clock ↓ Check D42-26 reset line ↓ Check D42, D49, D50, D48
Set-Up features not retained (Error code 2)	-23 Volt at D63-2 missing or D63 bad
Terminal will not communicate with host	Is terminal ON LINE ? Check Xmit/Rcv Baud rates, Word lenght, parity ↓ Check +/-12 Volt ↓ Check D61, D62 ↓ Check clock at D50-7, 8, 9
Printer Port does not work	Check +/-12 Volt ↓ Check D61, D62 ↓ Check D48 ↓ Check D50 ↓ Check V108 (Ptr. Ready)
No Keyboard operation and Cursor does not blink	Check D50, D42, D72 ↓ Check interrupt priority chain
No video but Bell works	D57 bad (screen blank) Bad CRT
Missing dots in characters	Bad Chr.Gen. D15 Bad D39 or D38 shift register
Brightness control not working	Bad D36
Video attributs wrong	Bad 12 Bad Prom D57
Double high chars. wrong	Bad ROM D8 Bad D18
80 or 132 col. mode nor working	Bad osc. select line ↓ Bad 80 col.osc. ↓ Bad 132 col.osc.
Every row displays same data	Non-maskable interrupts missing

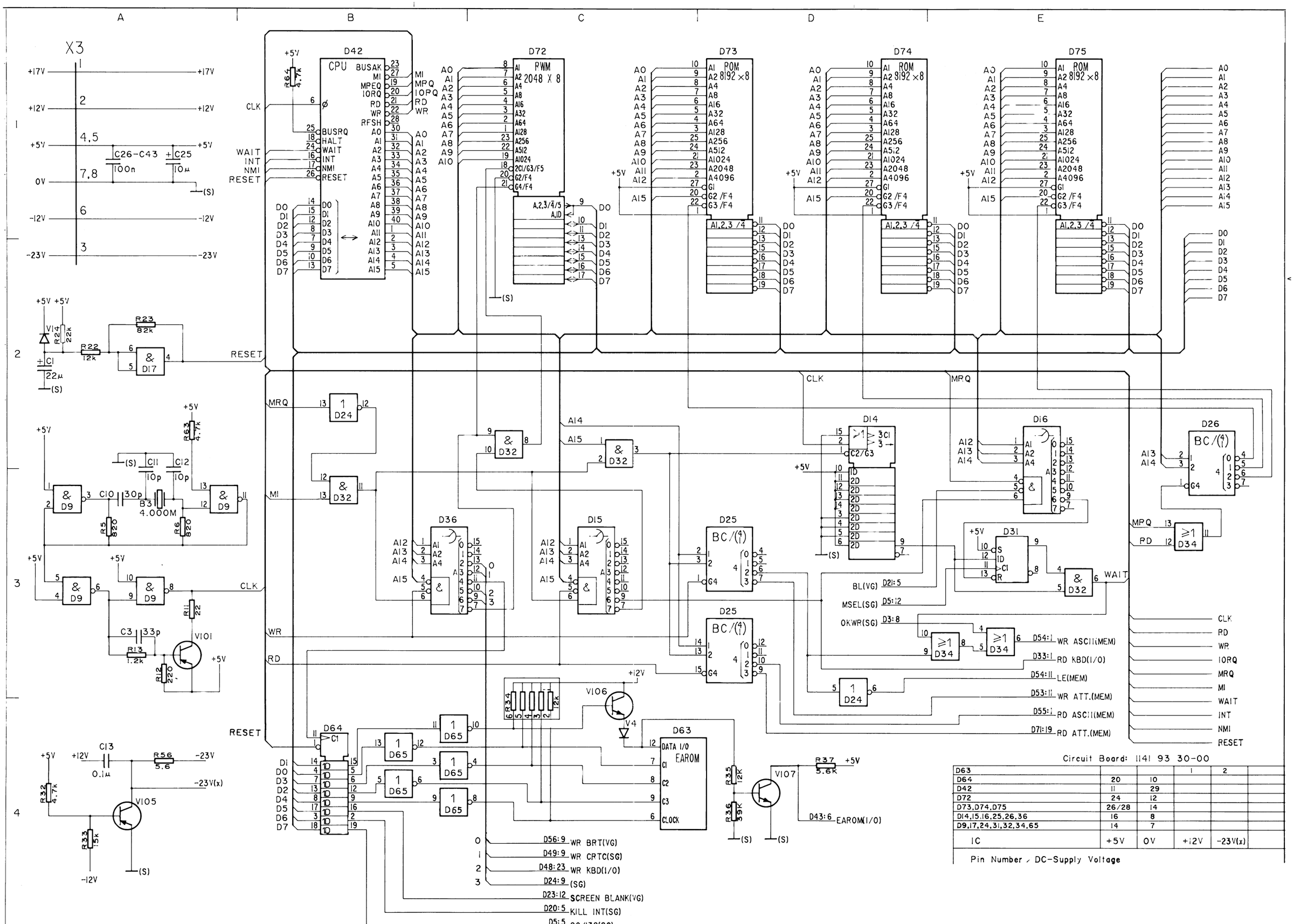
ERROR CODE 1 check displayed diagnostic:

address	Bad IC
8000-87FF	D52
8800-8FFF	D51
C000-C3FF	D68
C400-C7FF	D69
C800-CBFF	D67
CC00-CFFF	D66

bad address 8000 suggests buffers D54, D55
bad address C000 suggests D70, D71, D53

ERROR CODE 4 Replace EPROM D73, D74, D75

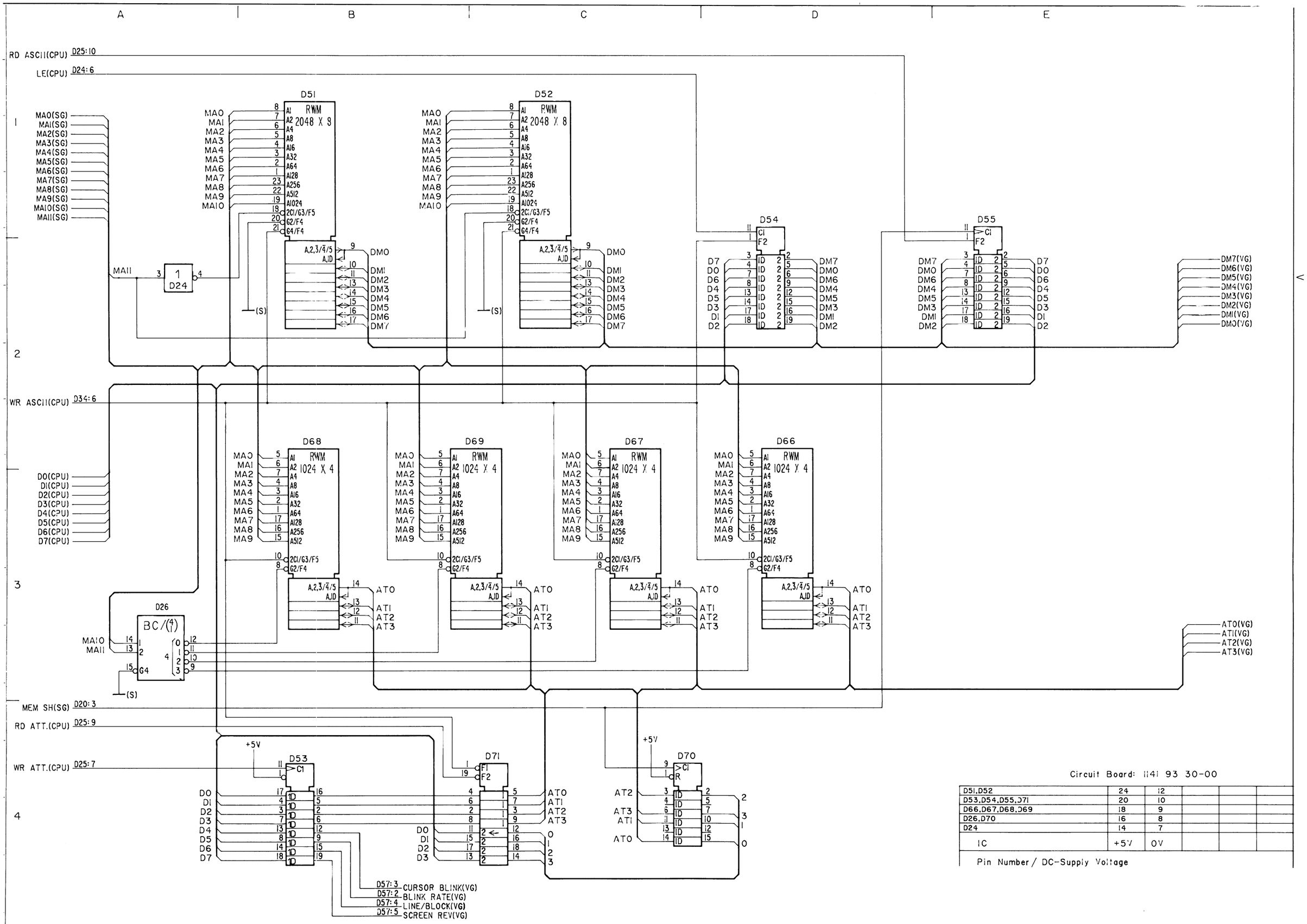

D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13
D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25 D26 D27 D28 D29 D30
D31 D32 D33 D34 D35 D36 D37 D38 D39 D40 D41 D42 D43 D44 D45 D46 D47 D48 D49 D50 D51 D52 D53 D54 D55 D56 D57 D58 D59 D60 D61 D62 D63 D64 D65 D66 D67 D68 D69 D70 D71 D72 D73 D74 D75
B1 B2 B3
X1 X2 X3 X4 X5 X6
V101 V102 V103 V104 V105 V106 V107 V108
W1 W2 W3 W4 W5
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43
R1 R2 R3 R4 R5 R6 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R32 R33 R34 R35 R36 R37 R38 R39 R40 R42 R43 R44 R45 R46 R47 R48 R49 R50 R51 R52 R53 R55 R56 R57 R58 R59 R60 R61 R62 R63 R64 R65 R66



Circuit Board: 1141 93 30-00

D63			1	2	
D64	20	10			
D42	11	29			
D72	24	12			
D73,D74,D75	26/28	14			
D14,15,16,25,26,36	16	8			
D9,17,24,31,32,34,65	14	7			
IC	+5V	0V	+12V	-23V(x)	

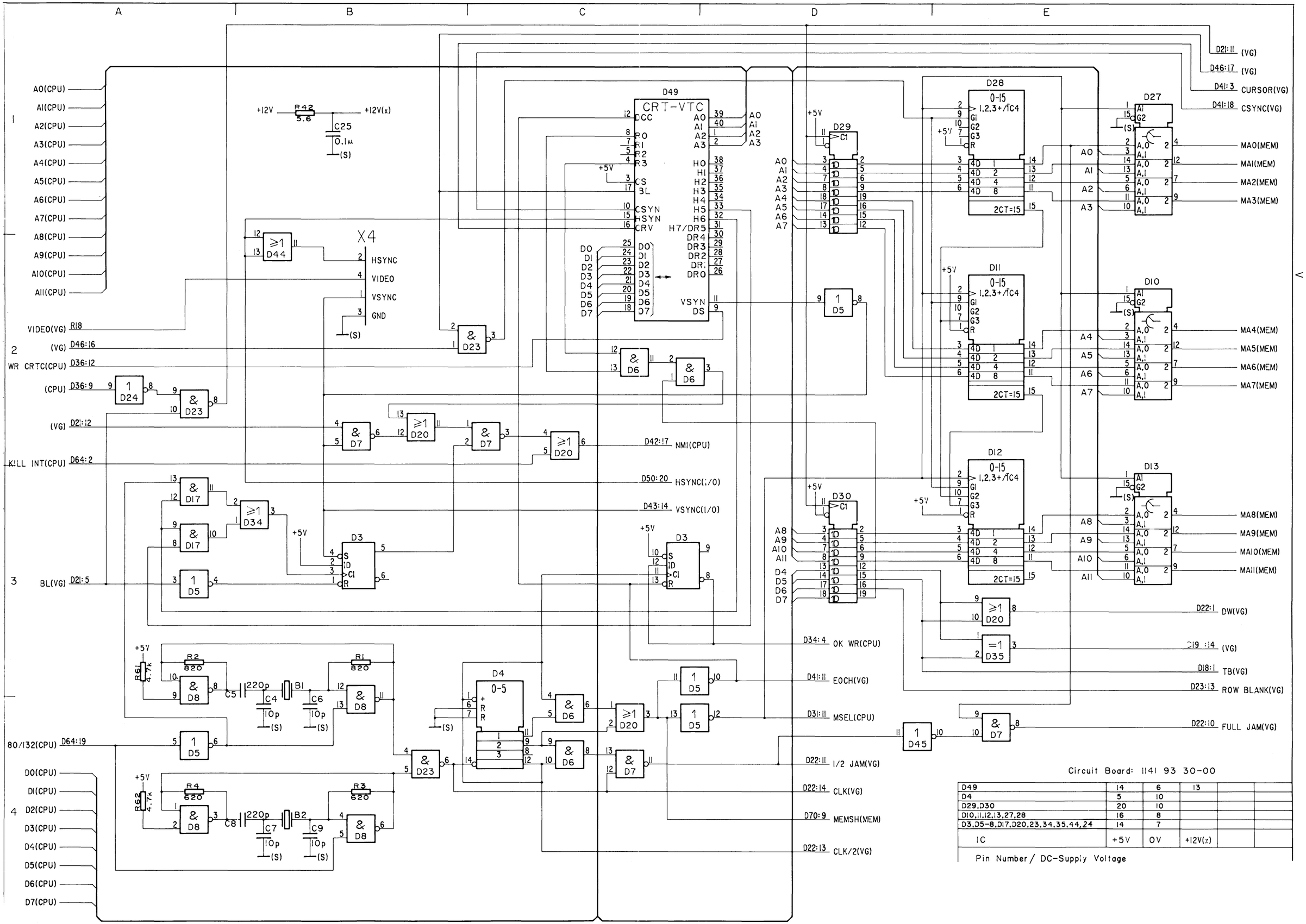
Pin Number / DC-Supply Voltage



Circuit Board: 1141 93 30-00

D51,D52	24	12			
D53,D54,D55,D71	20	10			
D66,D67,D68,D69	18	9			
D26,D70	16	8			
D24	14	7			
IC	+5V	0V			

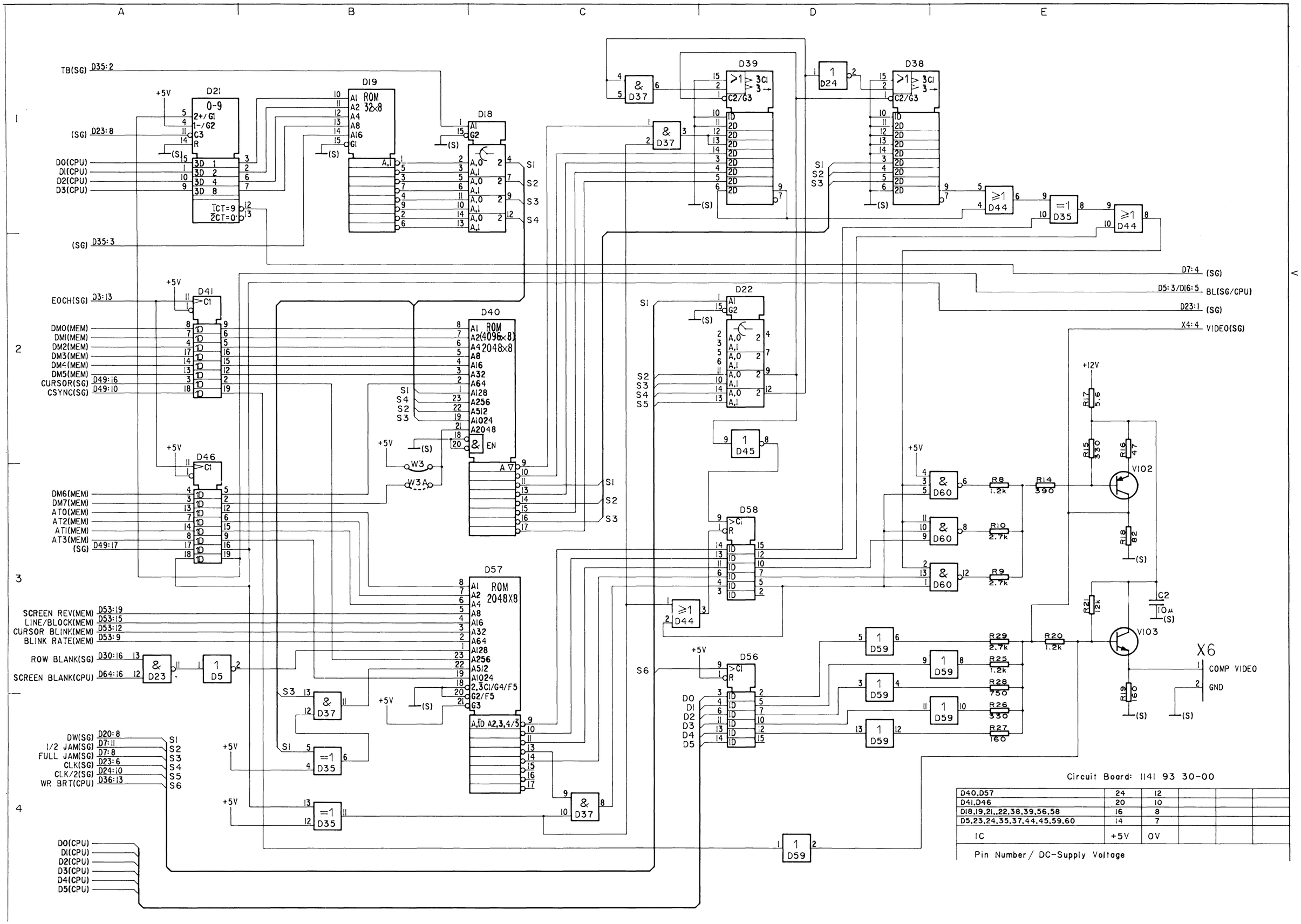
Pin Number / DC-Supply Voltage



Circuit Board: 1141 93 30-00

D49	14	6	13		
D4	5	10			
D29,D30	20	10			
D10,11,12,13,27,28	16	8			
D3,D5-8,D17,D20,23,34,35,44,24	14	7			
IC	+5V	0V	+12V(x)		

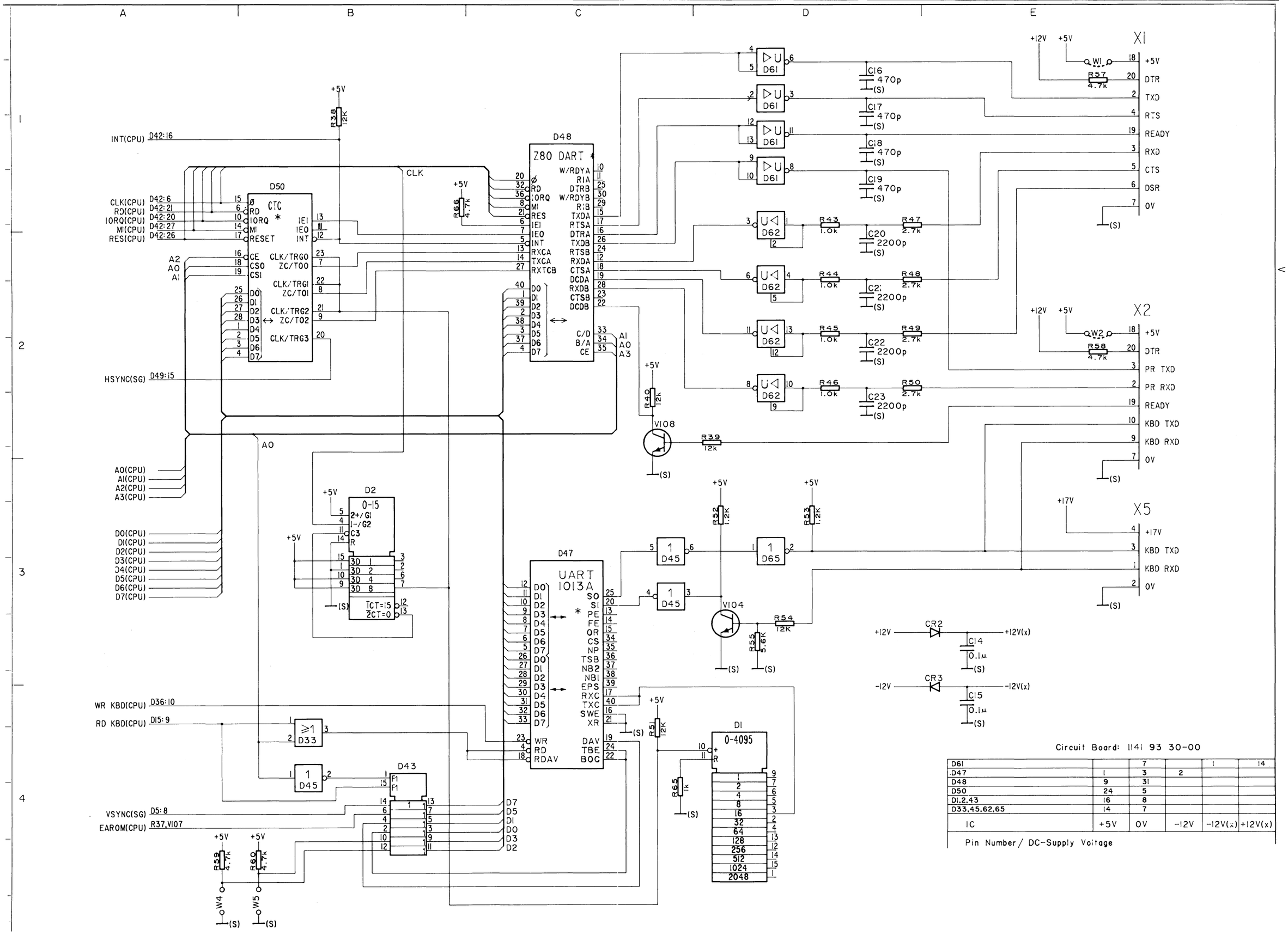
Pin Number / DC-Supply Voltage



Circuit Board: 1141 93 30-00

D40,D57	24	12			
D41,D46	20	10			
D18,19,21,,22,38,39,56,58	16	8			
D5,23,24,35,37,44,45,59,60	14	7			
IC	+5V	0V			

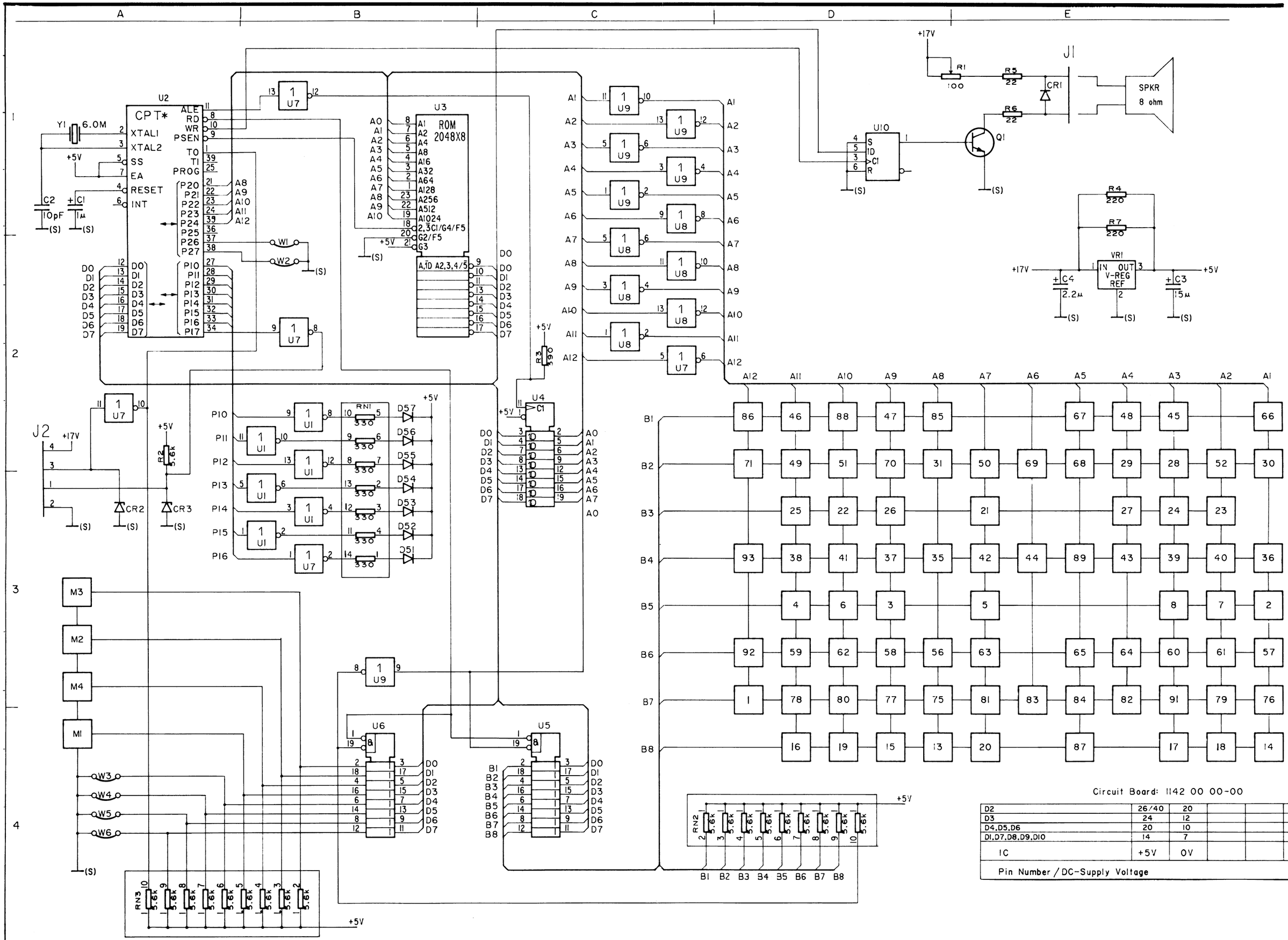
Pin Number / DC-Supply Voltage



Circuit Board: 1141 93 30-00

D61		7		1	14
D47	1	3	2		
D48	9	31			
D50	24	5			
D1,2,43	16	8			
D33,45,62,65	14	7			
IC	+5V	0V	-12V	-12V(x)	+12V(x)

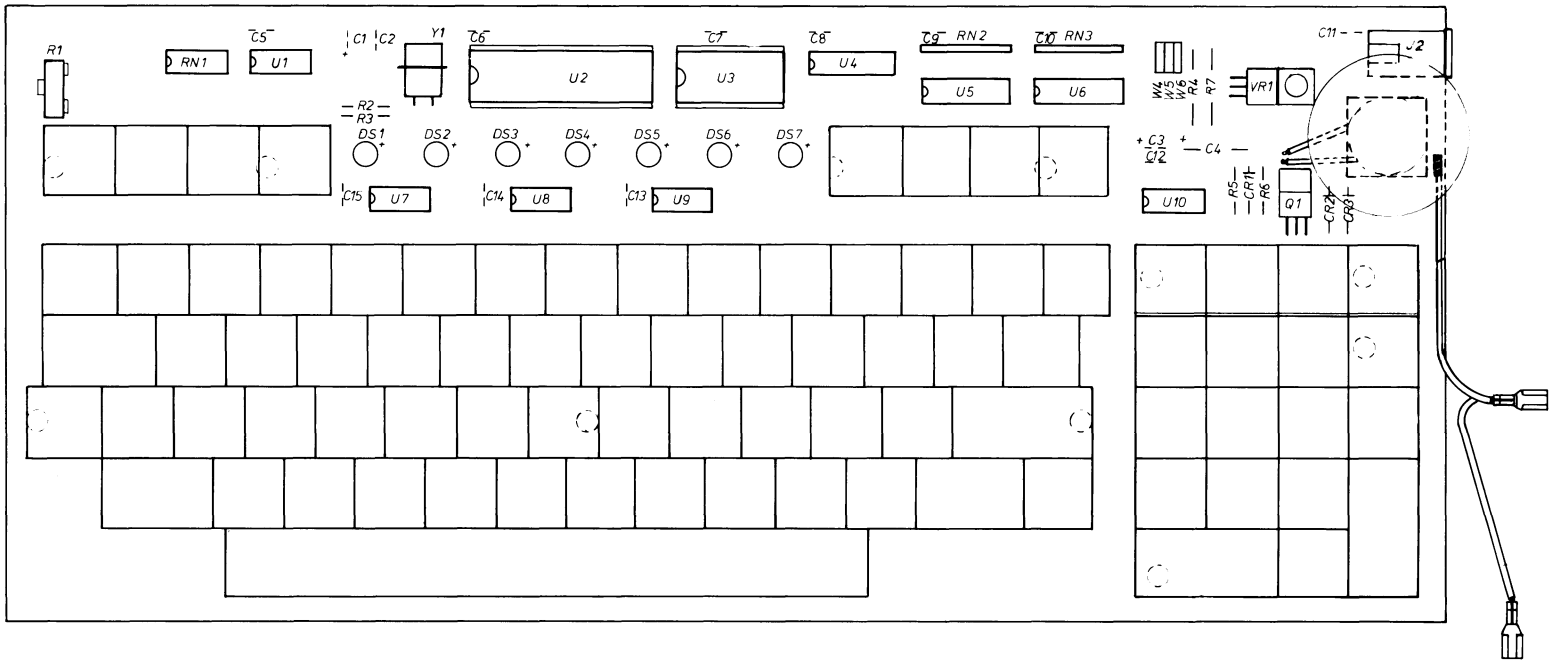
Pin Number / DC-Supply Voltage



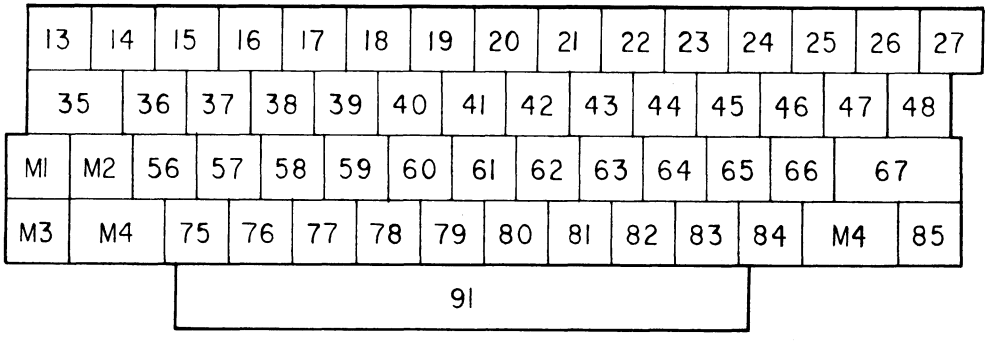
Circuit Board: 1142 00 00-00

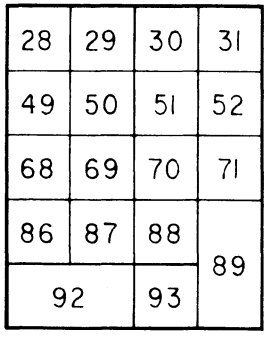
D2	26/40	20			
D3	24	12			
D4,D5,D6	20	10			
D1,D7,D8,D9,D10	14	7			
IC	+5V	0V			

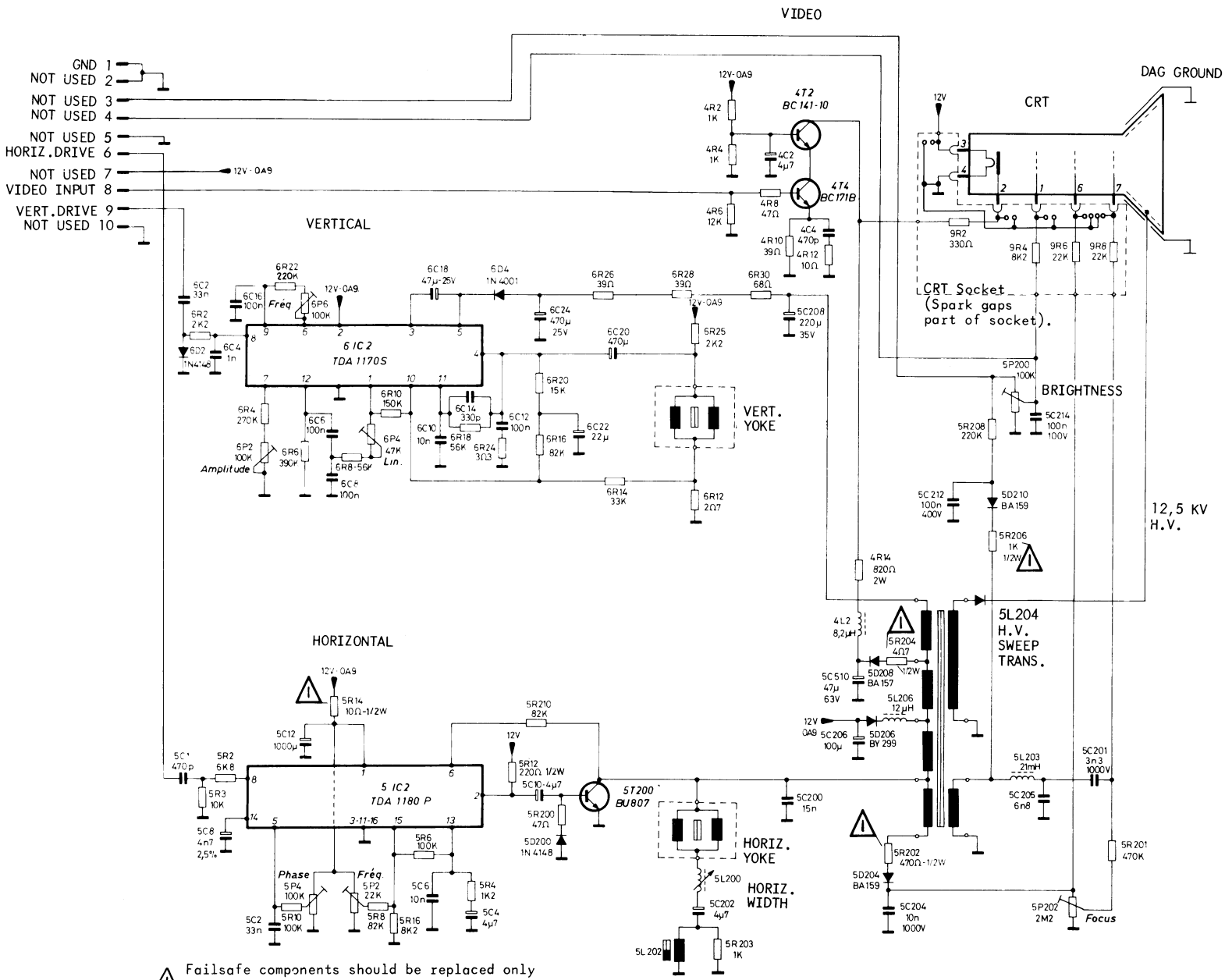
Pin Number / DC-Supply Voltage

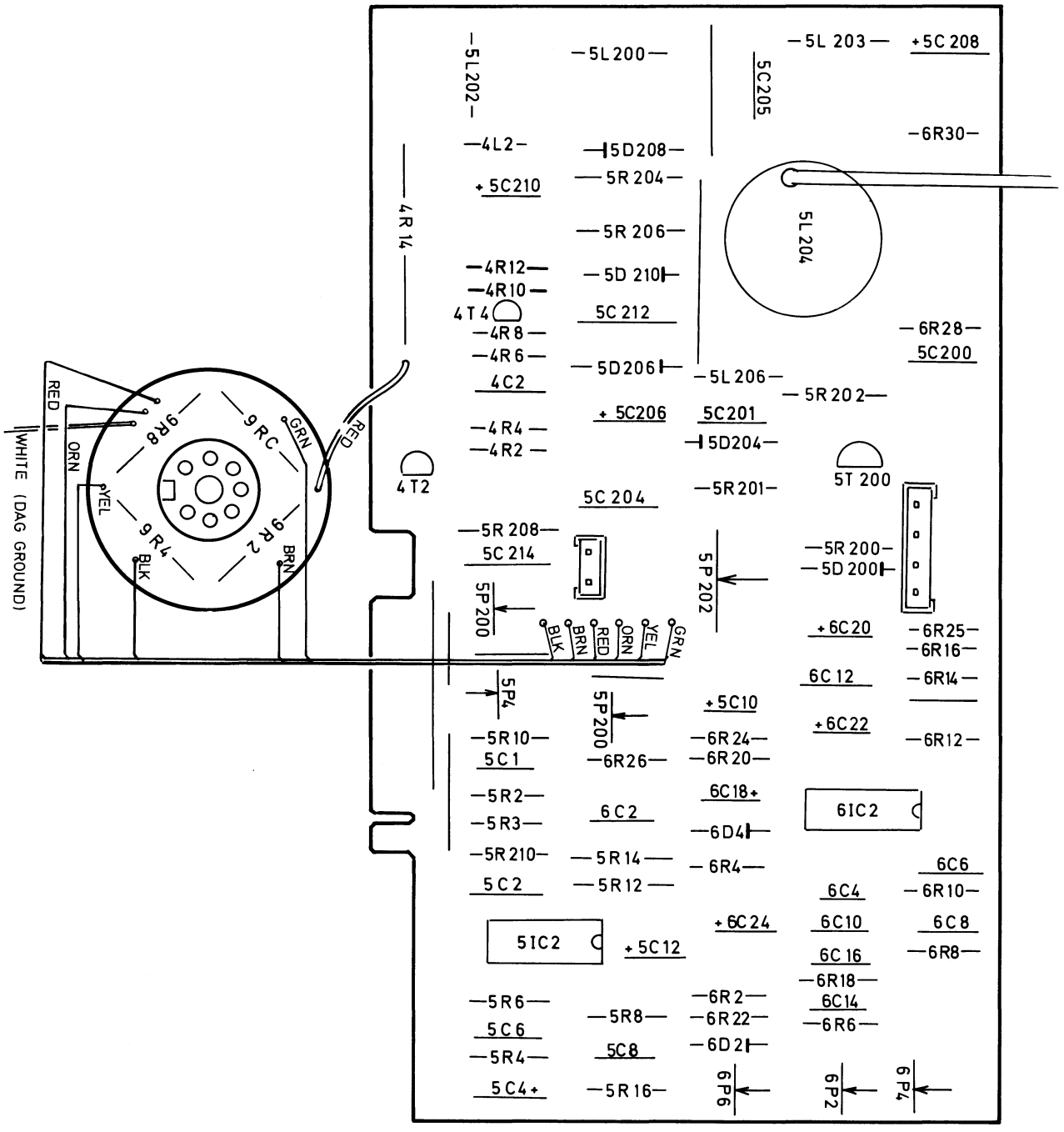

R1
RN1
C5
U1
C1
C2
Y1
C6
U2
C7
U3
C8
U4
C9
RN2
C10
RN3
U5
U6
C11
J2
W4
W5
W6
R4
R7
VR1
R2
R3
DS1
DS2
DS3
DS4
DS5
DS6
DS7
C3
C12
C4
C15
U7
C14
U8
C13
U9
U10
R5
CR1
R6
Q1
CR2
CR1

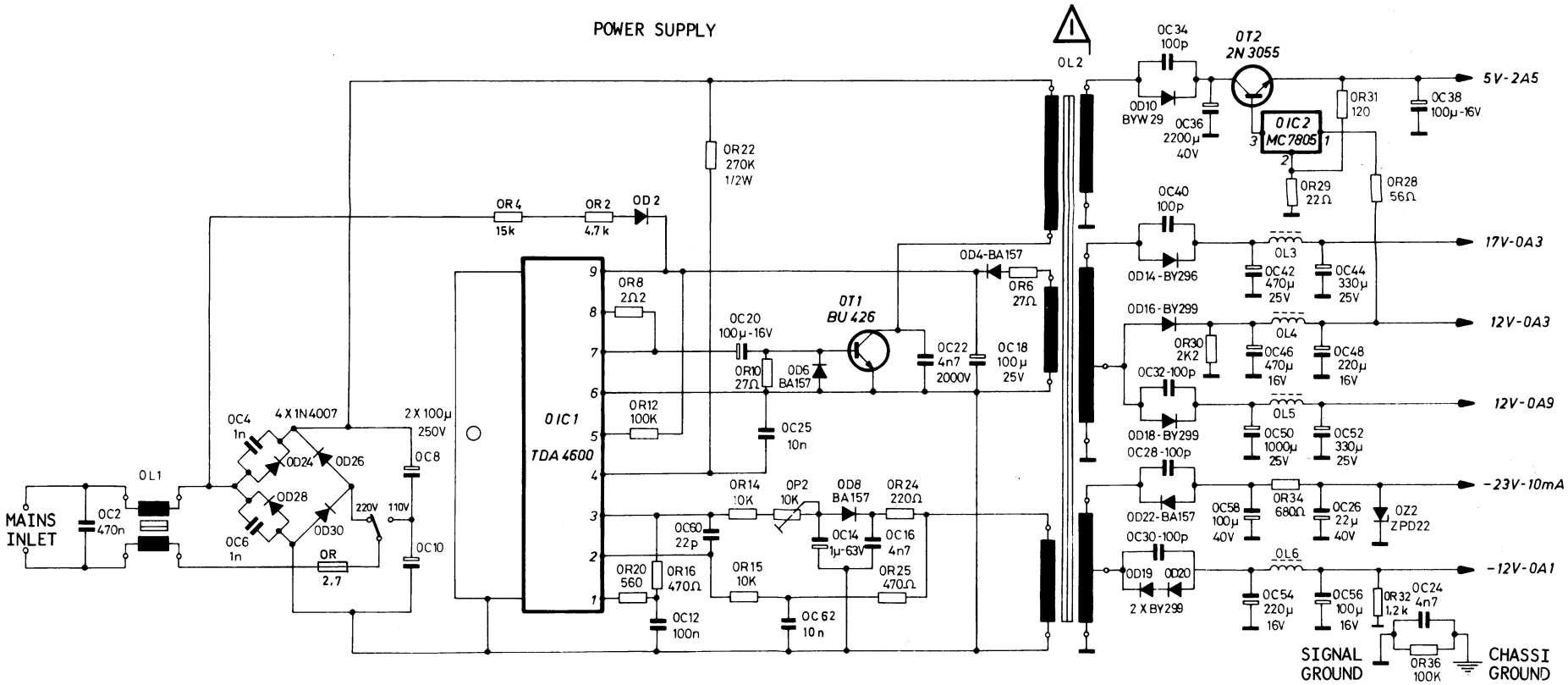

1 2 3 4
5 6 7 8

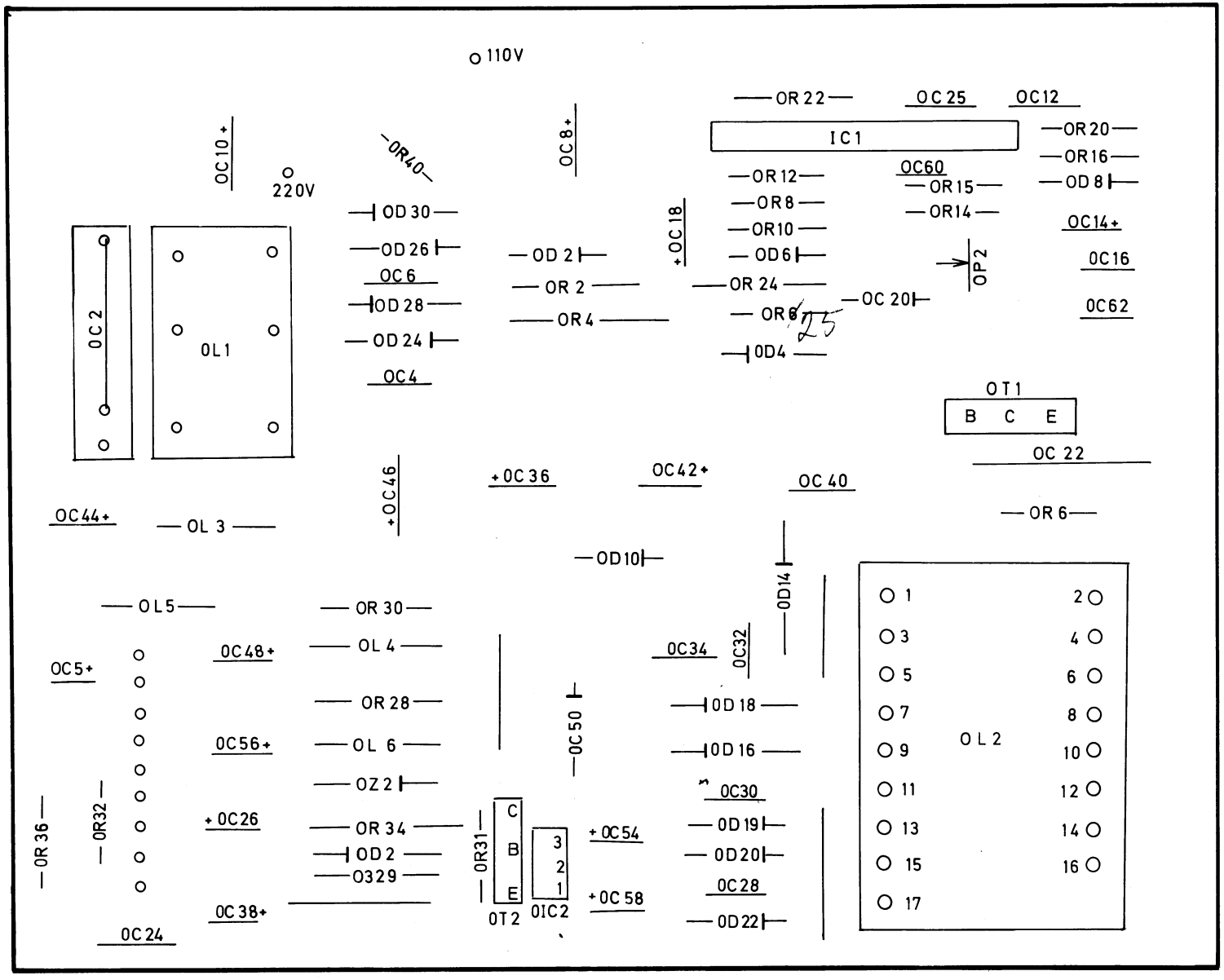

13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
35 36 37 38 39 40 41 42 43 44 45 46 47 48
M1 M2 56 57 58 59 60 61 62 63 64 65 66 67
M3 M4 75 76 77 78 79 80 81 82 83 84 M4 85
91


28 29 30 31
49 50 51 52
68 69 70 71
86 87 88 89
92 93


VIDEO
GND 1
NOT USED 2
NOT USED 3
NOT USED 4
NOT USED 5
HORIZ.DRIVE 6
NOT USED 7
VIDEO INPUT 8
VERT.DRIVE 9
NOT USED 10
12V-0A9
DAG GROUND
CRT
CRT Socket (Spark gaps part of socket).
VERTICAL
6 IC 2 TDA 1170S
VERT. YOKE
BRIGHTNESS
12,5 KV H.V.
5L204 H.V. SWEEP TRANS.
HORIZONTAL
5 IC 2 TDA 1180 P
5T200 BU807
HORIZ. YOKE
HORIZ. WIDTH
Fréq
Amplitude
Phase
Focus
Failsafe components should be replaced only with types identical to those in the original circuit.


5L202
5L200
5L203
+5C208
5C205
4L2
5D208
6R30
+5C210
5R204
4R14
5R206
5L204
4R12
5D210
4R10
4T4
5C212
6R28
4R8
5C200
4R6
5D206
5L206
4C2
5R202
+5C206
5C201
4R4
5D204
4R2
4T2
5T200
5C204
5R201
5R208
5C214
5R200
5D200
5P200
5P202
BLK
BRN
RED
ORN
YEL
GRN
+6C20
6R25
6R16
6C12
6R14
5P4
+5C10
+6C22
5R10
6R24
6R12
5C1
6R26
6R20
5R2
6C18+
6C2
6IC2
5R3
6D4
5R210
5R14
6R4
6C6
5C2
5R12
6C4
6R10
+6C24
6C10
6C8
5IC2
+5C12
6C16
6R8
6R18
5R6
6R2
6C14
5R8
6R22
6R6
5C6
6D2
5C8
5R4
6P6
6P2
6P4
5C4+
5R16
WHITE (DAG GROUND)
RED
ORN
YEL
BLK
BRN
GRN
RED
9R8
9RC
9R4
9R2


POWER SUPPLY
MAINS INLET
0C2 470n
0L1
0C4 1n
4 X 1N4007
0D24
0D26
0D28
0D30
0C6 1n
220V
110V
OR 2.7
2 X 100µ 250V
0C8
0C10
0IC1 TDA 4600
0R4 15k
0R2 4.7 k
0D 2
0R22 270K 1/2W
0R8 2Ω2
0R12 100K
0C25 10n
0C20 100µ-16V
0R10 27Ω
0D6 BA157
0T1 BU 426
0C22 4n7 2000V
0C18 100µ 25V
0D4-BA157
0R6 27Ω
0C60 22p
0R14 10K
0P2 10K
0D8 BA157
0R24 220Ω
0C14 1µ-63V
0C16 4n7
0R20 560
0R16 470Ω
0R15 10K
0R25 470Ω
0C12 100n
0C62 10 n
0L2
0C34 100p
0D10 BYW 29
0C36 2200µ 40V
0T2 2N 3055
0IC2 MC7805
0R31 120
0C38 100µ-16V
0R29 22Ω
0R28 56Ω
5V-2A5
0C40 100p
0D14-BY296
0L3
0C42 470µ 25V
0C44 330µ 25V
17V-0A3
0D16-BY299
0R30 2K2
0C32-100p
0D18-BY299
0L4
0C46 470µ 16V
0C48 220µ 16V
12V-0A3
0L5
0C50 1000µ 25V
0C52 330µ 25V
12V-0A9
0C28-100p
0D22-BA157
0C58 100µ 40V
0R34 680Ω
0C26 22µ 40V
0Z2 ZPD22
-23V-10mA
0C30-100p
0D19 0D20
2 X BY299
0L6
0C54 220µ 16V
0C56 100µ 16V
0R32 1,2 k
0C24 4n7
0R36 100K
SIGNAL GROUND
CHASSI GROUND


110V
220V
OC10+
OR40
OC8+
OR22
OC25
OC12
IC1
OR20
OR16
OD8
OC60
OR15
OR14
OR12
OR8
OR10
OD6
OR24
OR6
OD4
OC14+
OC16
OC62
OC20
OP2
+OC18
OD30
OD26
OC6
OD28
OD24
OC4
OD2
OR2
OR4
OC2
OL1
OT1
B C E
OC22
OR6
+OC46
+OC36
OC42+
OC40
OC44+
OL3
OD10
OD14
OL5
OR30
OL4
OR28
OL6
OZ2
OR34
OD2
0329
OC48+
OC56+
+OC26
OC38+
OC24
OC5+
OR36
OR32
OR31
C
B
E
OT2
3
2
1
OIC2
+OC54
+OC58
+OC50
OC34
OC32
OD18
OD16
OC30
OD19
OD20
OC28
OD22
OL2
1
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