(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 494 869 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
04.09.1996 Bulletin 1996/36

(21) Application number: **90911072.8**

(22) Date of filing: **11.07.1990**

(51) Int Cl.[6]: **G11B 21/10**, G11B 5/596

(86) International application number:
PCT/US90/03883

(87) International publication number:
WO 91/02354 (21.02.1991 Gazette 1991/05)

(54) DISK DRIVE SYSTEM USING MULTIPLE EMBEDDED QUADRATURE SERVO FIELDS

PLATTENANTRIEBSSYSTEM MIT MEHREREN EINGEBETTETEN QUADRATUR-SERVO-FELDERN

SYSTEME D'UNITE DE DISQUES UTILISANT DE MULTIPLES CHAMPS DE QUADRATURE D'ASSERVISSEMENT ENCASTRES

(84) Designated Contracting States:
DE FR GB IT

(30) Priority: **27.07.1989 US 386504**

(43) Date of publication of application:
22.07.1992 Bulletin 1992/30

(73) Proprietor: **CONNER PERIPHERALS, INC.**
San Jose, CA 95134-2158 (US)

(72) Inventors:
- **SHRINKLE, Louis, J.**
Boulder, CO 80302 (US)
- **SQUIRES, John, P.**
Boulder, CO 80455 (US)

(74) Representative: **Sanders, Peter Colin Christopher**
BROOKES & MARTIN
High Holborn House
52/54 High Holborn
London WC1V 6SE (GB)

(56) References cited:
EP-A- 0 094 314
EP-A- 0 240 745
JP-A- 0 623 475
JP-A- 1 154 376
US-A- 4 669 004
US-A- 4 823 212

Note: Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

EP 0 494 869 B1

Description

Cross Reference to Related Application:

The present application is related to the following Applications, all assigned to the Assignee of the present Application:

1. DISK DRIVE SYSTEM CONTROLLER ARCHITECTURE, invented by John P. Squires, et al, Application Serial Number 057,289, filed June 2, 1987 (US-A-4 979 056);
2. DISK DRIVE SOFTWARE SYSTEM ARCHITECTURE, invented by John P. Squires, et al, Application Serial Number 057,806, filed June 2, 1987;
3. DISK DRIVE SYSTEM CONTROLLER ARCHITECTURE UTILIZING EMBEDDED REAL-TIME DIAGNOSTIC MONITOR, invented by John P. Squires, et al, Application Serial Number 058,289, filed June 2, 1987 (US-A-4 979 055);
4. LOW POWER HARD DISK DRIVE SYSTEM ARCHITECTURE, invented by John P. Squires and Louis P. Shrinkle, Application Serial Number 152,069, filed February 4, 1988 (US-A-5 402 200);
5. VOICE COIL ACTIVATED DISK DRIVE PARKING DEVICE WITH MAGNETIC BIAS, invented by Kurt Michael Anderson, Application Serial Number 269,573, filed November 10, 1988 (EP-A-445 146).

Field of the Invention:

The present invention generally relates to closed-looped, embedded servo disk drives and their control systems, and, in particular, to a disk-drive control system utilizing a nearly continuous band gray code and a quadrature servo pattern field provided one or more times per track sector.

Background of the Invention

JP-A-1 154 376 relates to a disk drive control system for positioning the data read/write head in alignment with tracks on the disk using embedded servo information. The servo pattern described involves four servo bursts fields which together define the data track center line.

Disk drive systems utilizing closed-looped head positioning control systems rely on servo data stored on the rotating disks as the source of data track positioning feedback information. One approach to providing such servo information is to dedicate an entire disk surface and corresponding servo read data channel for the near-continuous sourcing and capture of positioning information. However, dedication of an entire disk surface and the need to provide special servo control read circuitry results in a significant increase in the cost per unit data of the disk drive control system and disk drive as a whole.

An alternate approach is to provide servo information within each track sector on every data surface of the disk drive system, i.e. embedded servo. Conventionally, A/B servo bursts of constant frequency and amplitude servo information are recorded as sequential fields within the sector header of each data sector. The servo burst fields are written symmetrically offset from and on respective sides of the data track center line by at least one-half of the head width. That is, the servo bursts do not overlap the track center line. Consequently, the differences between the relative voltage amplitudes (V_A - V_B), as read by the head while track following, may be utilized as a direct indication of the distance and direction of the head from the track center line.

There are, however, a number of drawbacks to providing servo information in each sector header. Since the servo information is in-line with the sector data, the percentage of sector length available for storing user data is reduced. The aggregate reduction in user data storage space is often many megabytes, if not tens of megabytes, as a consequence of using embedded servo information.

Another problem with conventional embedded servo systems is that the servo information is received only once per sector. Each sector, however, follows a uniform arc proportional to its radial distance from disk center. There are non-linear forces acting on the actuator arm and head that require active compensation. These forces include shock and vibration, and to a lesser extent, the air drag of the arm and head and the torquing force of the flex circuit. However, such forces and any error in the previous position correction will result in head drift that remains uncompensated until the next sector's servo burst can be obtained and a new correction applied.

Head drift during a sector read operation will result in data errors if the drift is significant. Conversely, excessive drift during a write operation is unacceptable due to the compromise of data stored on adjacent tracks. Therefore, track spacing is predominantly limited by the accuracy or tightness of the servo control loop, that is, in turn, dependent on sector length and disk rotation rate, i.e., the effective frequency of occurrence of servo bursts with respect to the read head.

Another limitation of A/B servo burst control systems arises from the extent of off-track error that can be unambiguously determined based on the servo burst fields. Whether as the end condition of a seek operation or the consequence of vibration or mechanical impact, a read head may be at a position substantially offset from the desired track center line. Beyond an off-track range limit from track center line, the servo control loop will fail to produce a proper position correction as a consequence of reading servo burst data from an adjacent track. The servo control loop will therefore issue an inaccurate position correction or incorrectly select the then closest track center line as being the desired track center line for track following. A time-consuming additional seek operation is then required to change tracks. Typically the off-track capture range of A/B burst servo control systems is no more than about ±3/8 of a track width.

The conventional A/B servo burst pattern itself may give rise to loss of tracking accuracy as a consequence of incorrect placement of the servo burst fields. Track formatting, or servo track writing, is done to provide the servo burst fields as part of the initial drive fabrication. Although done under the electromechanical control of a precision servo writer controller, variances due to vibration, out of round spindle bearings, and nonlinearities in the servo writer's own mechanics will result in one or more servo bursts being written offset from their ideal location. Surface defects can also distort the shape and effective position of servo bursts. If left uncorrected, subsequent track following operations will follow an improper track center line or slip entirely off track. For conventional A/B burst patterns, the off-track error is equal to the net servo burst field offset error. Typically, data sectors having incorrectly written servo bursts are marked as simply unusable.

Another concern relevant to the use of embedded servo is the consequence of increased track density. Conventional A/B burst patterns are written by a servo pattern writer using a series, typically four, of write head passes. This results in a series of overlap erasures of the partial patterns written during prior passes. The erasure is a consequence of a fringe electromagnetic field extending beyond the head element when the head is energized to write. The problem is that, as the track density is increased, the proportion of the servo bursts that are fringe field erased increases. That is, the total width of the bursts perpendicular to the track center line is decreased, but the width of the erasure is constant. Consequently, there is a loss of track following accuracy due to the decreased ability to discriminate track offset errors based on the decreased recoverable signal strength of the A/B servo bursts.

Quad-burst servo field patterns have been proposed for use in embedded servo systems. U.S. Patent No. 4,669,004 discloses a quad-burst pattern where one of four sequential servo fields is disposed symmetrically across the track center line, two others are symmetrically offset from the track center line, and a fourth field is asymmetrically disposed well above the track center line. This burst pattern identically repeats every fourth track at the same sector.

The individual burst offsets are related as integer multiples of less than or equal to one-half of the head width. Each servo field is identically provided with absolute track identification information as well as a track center line relative burst field. The significance of providing four such servo fields, as opposed to just two servo bursts, is that all modes of track-seeking, up to a preset maximum seek rate, will result in the read head crossing substantially over at least one of the servo fields.

The quad-burst servo pattern disclosed in U.S. Patent No. 4,669,004, however, is also sensitive to servo burst offset errors. Although four servo bursts are present, only two of the bursts are used in determining the relative off-track center line distance and direction. These two bursts are functionally and positionally equivalent to the A/B bursts. Accordingly, this quad-burst servo system obtains no better insensitivity to servo burst position offset errors than the conventional two-burst servo pattern systems. Further, another limitation of the quad-burst servo pattern of U.S. Patent No. 4,669,004 is that it appears to place a constraint on the track pitch based on the width of the read/write head.

Statements of Invention

According to one aspect, the present invention provides a data storage medium having a servo pattern for providing servo information for the positioning of a head with respect to data tracks provided on its surface, each data track including a series of data sectors, said servo pattern comprising four servo burst fields provided in each data sector in a series ordered along the length of each data sector, each pair of servo burst fields in a predetermined data sector defining the data track center line of a respective data track as the mid-point of the mutual radial overlap of said pair of servoburst fields; characterised in that the radial width W of a servo burst field is related to the track radial width T by $0.5T < W <= 1.0T$, said pairs of servo burst fields radially overlapping by W-(T/2).

According to another aspect, the present invention provides a disk drive control system operating from embedded servo control information comprising:

(a) a data storage medium according to the first aspect of the present invention;

(b) actuator means, responsive to a position control signal, for positioning a head with respect to said data tracks; and

(c) control means, coupled to said actuator means, for controlling the positioning of said head with respect to said data tracks, said control means including means, coupled to said head, for obtaining a relative position value for

each of said servo burst fields of a data sector, means for determining a track center line offset value as the difference of sums of pairs of said relative position values, and means, responsive to said track center line offset value, for providing said position control signal to said actuator means.

Therefore, a general purpose of the present invention is to provide a high performance embedded servo disk drive control system suitable for use in high-track density disk drive systems.

An advantage of the present invention is that the actuator seek rate is not limited by the nature of the track identification information or its presentation as part of the embedded servo information.

Another advantage of the present invention is that it provides a substantially increased servo lock or track-following range of approximately ±5/8 of a track width as measured from track center line.

A further advantage of the present invention is that it provides for a true quadrature-based track following algorithm. A difference of sums of servo burst pair read voltages provides a substantially increased degree of accuracy in determining both position and direction to the current track center line. In addition, any misposition of the servo burst fields, relative to one another and track center line results in a track following error of no more than one-half of the net error offset of the servo bursts.

Still another advantage of the present invention is that the provision of the quad-servo burst pattern of the present invention does not limit track pitch as a function of head width due to the fringe field erasure phenomenon.

A still further advantage of the present invention is that the provision of a second, mid-sector gray code and quad-burst servo pattern doubles the effective servo information frequency, resulting in substantially improved track following accuracy that, in turn, allows a substantially increased track density to be realized.

Another significant advantage of the present invention is that the quad-servo burst fields may be relied on selectively during servo-track writing to correct previous servo writer errors, thereby substantially reducing the aggregate sensitivity of the servo writing process to errors and the number of unusable sectors.

Other advantages of the present invention include adaptability to the use of data heads having a read profile width significantly smaller than their write profile width, such as magneto-resistive heads, and glass substrate disks.

Brief Description of the Drawings:

These and other advantages and features of the present invention will become apparent when considered in conjunction with the following detailed description of the present invention and the drawings, wherein like reference numerals designate like parts throughout the figures thereof, and wherein:

Figure 1 is a simplified block diagram of a disk drive control system consistent with the present invention;

Figure 2 is a simplified representation of a portion of a data track with the plurality of sectors provided thereon;

Figures 3a-b illustrate the distribution of servo control information and data in a simple, exemplary sector as provided in accordance with the present invention;

Figure 4 illustrates the task management control system flow structure of the microcontroller of the present invention in processing the servo control information of the sector shown in Figures 3a-b;

Figure 5 illustrates the detailed presentation of the servo control information of the exemplary sector, shown in Figures 3a-b, as provided in accordance with the present invention;

Figure 6 provides a simplified block diagram of the servo burst capture circuitry of the present invention;

Figure 7 provides a block diagram of the sector mark, gray code and servo burst capture control circuitry of the present invention;

Figure 8 is a detailed representation of the distribution of gray code and servo burst fields over a number of representative data tracks as provided in accordance with the present invention;

Figure 9 provides a graphical representation of the track following quadrature result value of the present invention as a function of range from track center line;

Figures 10a-e illustrate the sequential process for providing the continuous band gray code and quad-servo burst fields of the present invention; and

Figures 11a-c illustrate a number of representative cases of the repair of servo burst information in accordance with the present invention.

Detailed Description of the Invention:

A disk drive system consistent with the principles of the present invention, generally indicated by the reference numeral 10, is shown in Fig. 1. The preferred embodiments of the present invention utilize an embedded microcontroller control system to manage and direct all essential functions of the mechanical aspects of the disk drive system. The drive system includes one or more disks 12 spun in parallel planes by a spindle motor 14. Data is stored in a data track

band on each surface of a disk 12 defined by an outer (OD) and inner (ID) track diameter. An actuator assembly 16, including an arm and load beam 18 and a read/write head 20, is utilized to transfer data with respect to concentric data tracks 22 within the track band. Thus, the primary control aspects include controlling the spin rate of the spindle motor 14 and the control of the actuator assembly 16 in positioning of the read/write head 20 for the transfer of data with respect to a preselected data track 22.

A microcontroller 24 and a minimum number of dedicated control support circuits direct all functions of the drive system 10. The electronic architecture of the present invention is described in detail in the co-pending related applications cited above.

In the preferred embodiments of the present invention, the microcontroller 24 is a three megahertz clock rate Motorola MC68HC11 HCMOS single chip microcontroller, as described in the MC68HC11A8 HCMOS Single Chip Microcomputer Technical Data Book (ADI 1207) available from Motorola, Inc., Motorola Literature Distribution, P.O. Box 20912, Phoenix, AZ, 85036.

A read-only memory (ROM) 26 is coupled to the microcontroller 24 by way of a general purpose data, address and control bus 40. The ROM 26 is utilized to store a microcontroller control program for supporting five principle tasks necessary to implement the full functionality of the disk drive system 10. These tasks include interface, actuator, spin motor, read/write and monitor.

An interface control circuit 28 is provided to support the microcontroller 24 in execution of the interface task. The interface controller 28, in a preferred asynchronous SCSI embodiment of the present invention, is implemented as a Cirrus Logic CL-SH250 Integrated SCSI Disk Controller, manufactured and distributed by Cirrus Logic, Inc., and described by their CL-SH250 Technical Data Sheet, available from Cirrus Logic, Inc., 1463 Centre Pointe Drive, Milpitas, CA 95035. A comparable synchronous SCSI interface controller, the AIC-6110, is available from Adaptec, Inc., 691 South Milpitas Boulevard, Milpitas, California 95035. A functionally equivalent interface controller, suitable for interfacing to the IBM Personal Computer Model "AT" peripheral bus, is also available from Cirrus Logic, Inc.

The interface controller 28, in general, provides a hardware interface between the disk drive system 10 and a host computer system, typically a data processing system, via an SCSI communications bus 60. Thus, the interface controller 28 operates to manage bi-directional data streams between the communications bus 60 and the bus 40.

An actuator controller 32 is provided as an internal interface between the microcontroller 24 and actuator assembly 16. The actuator controller 32 provides for digital-to-analog conversion of a digital position control word and the current buffering of the resultant analog voltage provided on line 46 to the voice coil motor of the actuator assembly 16. The digital word, as provided via the bus 40 from the microcontroller 24, represents the desired actuator position. Enabling of the actuator controller 32 in general is provided via the control support circuit 30 via control lines 44. The control support circuit 30, to this end, acts as a parallel port expander for latching a control data word also provided by the microcontroller 24 via the bus 40.

A read/write controller 36 similarly acts as an internal interface between the bus 40 and the read/write heads of the actuator assembly 16 via the raw data lines 56. The read/write controller 36 functions to provide for the buffered serialization/deserialization and data clock encoding/decoding of data. Configuration and initiation of read/write controller 36 functions are performed under the direct control of the microcontroller 24 by the transfer of control and data words to the read/write controller 36 via the bus 40.

Finally, a spin motor controller 34 is provided to directly support the commutation of the spin motor 14 via the commutation current lines 50. Commutation state selection is effected by provision of a digital word from the microcontroller 24 to the control support circuit 30. This digital word is latched and provided on the commutation select lines 48 to the spin motor controller 34. A commutation current is switched by the spin motor controller 34 to a corresponding field winding phase pair of the spin motor 14 via the commutation current lines 50. A voltage proportional to the current conducted through the selected field winding phase pair of the spin motor 14 is provided via the feedback line 52 to an analog-to-digital converter input of the microcontroller 24.

The mechanical configuration of the disk drive embodying a preferred embodiment of the present invention is described in the application VOICE COIL ACTIVATED DISK DRIVE PARKING DEVICE WITH MAGNETIC BIAS cited above. The aspects of the mechanical structure pertinent to the present invention are set forth in Table 1 and Table 2 below.

Table 1

Number Data Cylinders	1368 cylinders
Sectors per Track	39 sectors
Number of Disks	4
Number of Data Surfaces	8
Bytes per Sector	662 bytes

Table 1 (continued)

Data Bytes per Sector	512 bytes
Data Capacity per Data Surface	27.3 Mbytes
Total Data Capacity	219 Mbytes

Table 2

Disk Diameter	96 millimeters
Data Track Band Width	30 millimeters
Track Density	1700 tracks/inch
Bit Density (max)	22,000 fci
Head Width	11 micrometers
Track Width	15 micrometers

As generally represented in Fig. 2, each track of the concentric data tracks 22 provided on the surface of a disk 12 are further subdivided into sectors N_{0-n}. In accordance with the present invention, and as generally shown in Fig. 3a, each sector is composed of a servo 1 field, a data 1 field, first error correction code (ECC) field, mid-sector gap field, servo 2 field, data 2 field, second ECC field, and final gap field. As shown in Fig. 3b, the servo 1 field is further composed of a servo mark field, gray code field, servo burst field, ID sync field, ID field, and data sync field. Similarly, the servo 2 field is composed of a second sector mark field, second gray code field, and servo burst field and finally, a data sync field. The order and size of these fields are set forth in Table 3.

Table 3

Half Sector "A"		Half Sector "B"	
Field	Bytes	Field	Bytes
Servo Sync	3	Servo Sync	3
Gray Code	8	Gray Code	8
Servo Burst A	4	Servo Burst A	4
Servo Burst B	4	Servo Burst B	4
Servo Burst C	4	Servo Burst C	4
Servo Burst D	4	Servo Burst D	4
Pad	1	Pad	1
ID Sync	12	Data Sync	12
ID (Header)	4	Data	267
ID CRC	2	ECC	7
Pad	4	Gap	17
Data Sync	12		
Data	245		
ECC	7		
Gap	17		
331 Bytes (1st half)		662 Bytes Total	

The sector mark fields are provided to synchronize the microcontroller with the control information present in the remaining portions of the servo 1 and 2 fields as well as the data 1 and 2 fields. The gray code fields provide an unambiguously encoded track number. The unambiguous coding of the gray code values is further qualified in that the gray code values of like sectors on adjacent tracks differ by a single bit and that no more than two consecutive zero bits are allowed in a valid gray code value.

The servo burst fields, in accordance with the preferred embodiments of the present invention, are sequentially arranged burst fields of constant amplitude and constant frequency offset in a pre-defined pattern from the center line of the data sector.

The ID sync field of the servo 1 field is also written at constant frequency and voltage, though centered on the track center line. The ID sync field allows the read/write controller to distinguish the first bit of the ID field. The ID field is used to store the cylinder, sector, and head numbers.

Finally, the data sync fields are constant frequency and amplitude fields provided to define the first bits of the respective data fields 1 and 2. The read/write controller synchronizes to the frequency of the data sync field. The first discontinuity in the sync frequency is therefore taken as the first data representative transition.

Referring now to Fig. 4, task execution as performed by the microcontroller 24 is shown mapped against the real time occurrence of the servo 1 and 2 fields with respect to a read/write head 20. The basic real time relations pertinent to the present invention are set forth in Table 4.

Table 4

Disk Rotational Speed	3550 rpm
Average Access Time	19 millisecs.
Minimum Track-to-Track Transition Time	28 microsecs.
Sector Period	433 microseconds
Average Track Seek Rate	15 tracks/sec.
Time Over Burst (each)	2.665 microsecs.
Bytes Read per Track at Max Seek Rate	43 bytes/track
Time over Gray Code	5.33 microsecs.
Out of Round Error	±1.27 micrometers
Core Write Fringe Width	4 micrometers

Specifically, a sector task is initiated in response to a countdown timer interrupt just prior to the occurrence of the servo 1 field. From this interrupt, the microcontroller 24 enables the control support circuit 30 to detect and process the sector mark field. A control value is then provided to the spin motor controller 34 to commutate the spin motor 14.

As shown in Fig. 5, the sector mark field is defined by the trailing end of the servo sync filled gap field and the sector mark. The gap field is another constant amplitude constant and frequency field. The sector mark is defined as the first read data transition following the absence of any servo sync transitions for three bytes of servo sync clock cycles. The time of occurrence of the sector mark is recorded by a hardware timer within the microcontroller 24 for use in subsequent tasks as well as scheduling the countdown timer interrupt necessary for processing the servo 2 field.

During the sector task, the gray code and sector bursts are captured by the control support circuit 30 via a raw data transfer line of the control lines 54 as coupled to the read/write controller 36. An automatic gain control circuit (AGC) is provided to adjust the amplitude of the raw data signal. In anticipation of the gray code and servo burst fields, the read/write controller is enabled by the microcontroller 24 to boost the gain of the AGC to compensate for reduced signal amplitudes. Although the AGC would automatically adjust its gain, the response time of the AGC is enhanced by direct adjustment of its gain just prior to or at the beginning of the gray code field. Capture of the gray code, though also earlier enabled by the microcontroller 24 during the servo sync corresponding portion of the sector task, is triggered by a sector mark signal produced upon detection of the sector mark. Similarly, capture of the four servo burst fields is triggered following a pre-defined delay, equal to the gray code length, following detection of the servo mark. The actual capture of the analog read amplitudes corresponding to each of the servo burst fields is performed by four sample and hold circuits individually gated to match the real time occurrence of the respective servo burst fields.

Meanwhile, the microcontroller 24 completes the sector task and transitions to a spin motor control task. The primary function of spin control task is to determine any rotational speed error of the spin motor 14 based on the previous actual and expected time of occurrence of the sector mark. A spin rate adjustment value may then be determined for use in the next servo 1 field sector task.

Next, an actuator task is executed by the microcontroller 24. This task is initiated subsequent to the A/D conversion of the D servo burst field. The first action undertaken by the microcontroller 24 in execution of the actuator task is to determine whether an actuator seek operation is pending or on offtrack error was prior determined. In either case, execution continues with a setup of a corresponding seek operation for subsequent execution. If, however, track following is to be performed, the four servo burst corresponding digital values are processed by the microcontroller 24 to derive a quadrature-based track following error value (T_{ERR}). Assuming that the B and C servo burst fields overlap the center line of the current data sector (known by whether the current track numbering is odd or even), the quadrature processing of the servo burst field values is done in accordance with Equation 1:

$$T_{ERR} = (A + B) - (C + D) \qquad \text{Eq. 1}$$

Where the A and D sector bursts overlap the center line of the current data sector, i.e., every other track, the quadrature processing is performed in accordance with Equation 2:

$$T_{ERR} = (C + D) - (A + B) \qquad \text{Eq. 2}$$

A positive track following error result is interpreted to indicate that the read/write head needs to be moved toward the inner diameter of the disk 12. The magnitude of the result gives an indication of the distance to the track center line. Thus, the microcontroller 24 may readily compute an error adjustment value based on the polarity and magnitude of the quadrature derived track following error. The error adjustment value is combined with the current actuator position control value and written to the digital-to-analog converter of the actuator controller 32. The adjusted analog actuator position control signal thereby produced by the actuator controller 32 results in a corrective change in the position of the actuator assembly 16 and the head 20 relative to the current data track.

The microcontroller 24 then transitions to a read/write task. Execution of the read/write task provides for the set up, continuance, or completion of the transfer of data with respect to the current data sector.

Finally, any pending seek operation is executed by the microcontroller 24 just prior to the conclusion of the read/write task. In general, the seek operation selected during the actuator task determines an actuator position value to initiate, continue, or complete a seek operation of the actuator assembly 16. This position value is now provided to the D/A converter of the actuator controller 32. The read/write task then completes with the execution of a return from interrupt instruction.

The sector task of the servo 2 field is initiated in response to the countdown timer interrupt as scheduled in the servo 1 sector task. The microcontroller 24 then executes sector, actuator, read/write and seek tasks that are substantially identical to their counterparts executed with respect to the servo 1 field, including scheduling the count down timer interrupt for the next sector's servo task start.

The balance of the sector period not otherwise spent processing the servo 1 and servo 2 fields is used to execute the interface task and, if active, the monitor task. Thus, the microcontroller 24 operates as an essentially multitasking processor in the control and management of the disk drive system 10.

Fig. 6 details the servo burst capture circuitry used in the preferred embodiments of the present invention. An AGC 71, of the read/write controller 36, processes the raw data input from the read/write head 20 via the raw data line 56. Although implemented as part of an application specific integrated circuit (ASIC), the AGC 71 is functionally equivalent to conventional AGCs, such as the National Semiconductor, Inc. 8464 AGC. The gain of the AGC 71 is inversely proportional to the voltage across a capacitor 73, coupled between ground and an input line of the AGC 71. The voltage across the capacitor 73 is .driven by the AGC 71 as part of its gain control feedback loop. In accordance with the preferred embodiments of the present invention, a small value resistor is also coupled to the capacitor input line of the AGC 71. While normally open circuited, the resistor provides a current path to allow at least a partial discharge of the voltage across the capacitor 73, and a corresponding immediate boost in the gain function of the AGC 71. The raw data amplitude on the AGC output line 56' is nominally 500 millivolts, peak to peak, single ended, in the preferred embodiments of the present invention. However, due to overlap erasure in the gray code fields and reduced width of the burst fields, the comparable raw data amplitude for these fields may be typically 350 millivolts. By coupling the resistor 75 to ground, preferably through an open drain transistor, for a short period of time chosen in view of the RC time constant of the capacitor 73 and resistor 75, the voltage across the capacitor 73 can be reduced in a controlled manner sufficient to immediately boost the gray code and servo burst raw data amplitude to the desired 500 millivolts. The resistor and capacitor values can be chosen so that the discharge time of the capacitor 73 is substantially faster than the intrinsic control loop response time of the AGC 71. In a preferred embodiment of the present invention, a 1000 ohm resistor 75 and 0.01 microfarad capacitor 73 is used. A grounding pulse of approximately 500 nano seconds provides the desired AGC gain adjustment.

A data separator 70, of the read/write controller 36, receives the AGC processed raw data via raw data line 56'. Based on a crystal controlled clock reference signal provided on a clock reference line 72 to the data separator 70, separated data and the formerly encoded data clock signal are provided on a data line 74 and an oscillator line 76, respectively. A buffered raw data signal is also output on a line 78 from the data separator. These lines, 74, 76, 78 are a subset 54' of the control lines 54 interconnecting the read/write controller 36 and control support circuit 30, as shown in Fig. 1.

The data and oscillator lines 74, 76 connect to a timing logic block 80 within the control support circuit 30. The timing logic block 80 includes a sector mark detection circuit, a gray code serial shift register and dedicated timing logic for enabling capture of the servo burst fields. The function of the timing logic block 80 is enabled in response to a control word written by the microcontroller 24 at the beginning of its sector task. Once enabled, a reset AGC signal is provided via line 77 to the resistor 75 to initial the AGC gain adjustment. The timing logic block 80 removes the reset AGC signal when the adjustment is completed. Upon detection of a sector mark, the timing logic block 80 provides a sector mark signal via line 122 to the microcontroller 24. Simultaneously, the gray code serial shift register is enabled to sequentially shift in the eight gray code data bytes. Since the clocking of gray code bits is done synchronous with the data clock, registration of the read data is maintained through the reading of the gray code and all subsequent operations of the timing logic block 80. Upon completion, a gate A (G_A) signal is provided to a full wave rectifier configured operational amplifier 82 via enable line 90. The input of the operational amplifier 82 is coupled to the raw data line 78. When enabled, the operational amplifier 82 provides a voltage corresponding to its input voltage on the output

line 98. A resistor R_A and capacitor C_A are coupled in a single pole, low-pass configuration to an output line 98. Preferably, the resistors R_{A-D} and capacitors C_{A-D} have values of 150 ohms and 0.001 microfarads respectively. When subsequently disabled by the withdrawal of the G_A signal, the operational amplifier 82 switches to a high impedance output state thereby effectively capturing an analog voltage across the capacitor C_A proportional to the read amplitude of the A sector burst field. The voltage across the capacitor C_A is coupled to a high-impedance input positive gain operational amplifier 114. In the preferred embodiments of the present invention, the gain is fixed at 2.5:1. The output of the operational amplifier 114 is, in turn, coupled to a first multiplexed input (P_A) of an analog-to-digital converter provided within the microcontroller 24.

The timing logic block 80 removes the gate A enable signal from the operational amplifier 82 after approximately 2.665 microseconds; the period of time that the read/write head 20 is over the A servo burst field. At the same time a gate B (G_B) enable signal is provided to an operational amplifier 84 via an enable line 92. The gate B enable signal is maintained for the duration of the B servo burst field and then withdrawn. Thus, an analog voltage corresponding to the B servo burst is captured by the capacitor C_B. This voltage is separately provided via an operational amplifier 116 to a second multiplexed input (P_B) of the microcontroller 24 analog-to-digital converter.

In similar fashion, gate C (G_C) and gate D (G_D) enable control signals are provided to operational amplifiers 86, 88 to sequentially capture the C and D servo burst field read voltages on capacitors C_C and C_D. These voltages are provided via operational amplifiers 118, 120 to the P_C and P_D multiplexed inputs of the microcontroller 24 analog-to-digital converter. Consequently, the circuitry of the control support circuit 30 provides an efficient yet simple circuit for capturing the quad-servo burst provided in accordance with the present invention.

Although captured, the analog voltages corresponding to the quad-servo bursts must still be converted to digital values. In accordance with the present invention, flash conversion of the analog values is not required. Rather, the onboard multiplexed input analog-to-digital converter of the microcontroller 24 is adequate to sequentially convert the analog values in time for the microcontroller 24 to effect an actuator position adjustment prior to any loss of significance of the servo burst information.

Once the microcontroller 24 has processed the converted digital servo burst values, the capacitors C_{A-D} must be cleared in preparation for capturing the next sequence of servo burst fields. This is accomplished, in accordance with the present invention, by the timing logic block 80 enabling the connection of reset lines R_{A-D} 106, 108, 110, 112, to ground after the servo bursts have been converted to digital values. Since the reset lines 106, 108, 110, 112 are coupled to the inputs of the buffer operational amplifiers 114, 116, 118, 120, respectively, the capacitors C_{A-D} are effectively shorted and thereby cleared. The timing logic block 80 then returns the capacitors C_{A-D} to an open circuited state with a zero voltage potential across the capacitors C_{A-D}.

Fig. 7 details the portion of the timing logic block 80 that is of significance to the present invention. A decoder 124 receives the control word from the microcontroller 24, via the bus 40, early in the sector task to enable the operation of a sector mark detector 126 and gray code shift register 128. The sector mark detector 126 continuously receives raw data from the raw data line 78 and the data clock from the oscillator line 76. The sector mark detector enable signal is provided from the decoder 124 via control line 136 in response to the control word being written to the decoder 124 by the microprocessor 24. Once enabled, the sector mark detector 126 provides a sector mark signal on its output line 122 upon detecting three bytes of servo sync clock cycles without a raw data transition.

The sector mark signal is also provided to the gray code shift register to synchronize the gray code capture operation to the beginning of the gray code field. As shown in Fig. 5, the gray code field immediately follows the sector mark. The gray code capture enable signal, as provided from the decoder 124 on the enable line 138, is provided simultaneously with the sector mark detector enable signal on control line 136. However, the gray code shift register 128 does not begin operation until it also receives the sector mark signal from the sector mark detector 126. A counter 130, operating from the data clock signal on line 76, provides a gray code count signal on control line 142 to the gray code shift register 128 to clock in each bit of the gray code field. The counter 130 halts the provision of count signals on the control line 142 once the full eight bytes of the gray code field have been serially shifted in. The counter 130 then begins providing count signals on the servo burst count lines 144 to a gate switch 132. The function of the gate switch 132, based on the count signals provided on the servo burst count lines 144, is to provide and then withdraw in succession the gate A-D enable signals on the gate control lines 90, 92, 94, 96. Each gate enable signal is provided for a duration of four bytes. Since this four byte duration is based on the data clock signal received by the counter 130 on the oscillator line 76, the gate enable signals are closely correlated with the real time occurrence of servo burst fields with respect to the read/write head 20. Once all of the gate enable signals have been enabled and then disabled, the counter 130 ceases to provide count signals to the gate switch 132. Consequently, the gray code of the current sector has been captured by the gray code shift register 128 and the analog read data values corresponding to each of the servo burst fields have been captured by the capacitors C_{A-D}.

The gray code may be read from the gray code shift register 128 in response to the microcontroller 24 reading from eight successive memory locations mapped by the decoder 124 to the eight bytes stored in parallel by the gray code shift register 128.

The reset switch 134 operates to ground, in common, the reset lines 106, 108, 110, 112 for a duration sufficient to discharge the capacitors C_{A-D}. Operation of the reset switch 134 is initiated by the counter 130 through the provision of count signals to the reset switch via count line 146. This count signal is delayed from the occurrence of the sector mark signal by a period greater than the combined gray code and servo burst capture time and subsequent maximum A/D conversion time. In the preferred embodiments of the present invention, this delay is between 80 and 400 microseconds, and preferably approximately 200 microseconds. A second count signal provided by the counter 130 defines the discharge period. In the preferred embodiments of the present invention, a discharge period of at least 10 microseconds is used to discharge the capacitors C_{A-D}.

The gray code and quad-servo burst pattern of the present invention is illustrated in Fig. 8. A portion of the servo fields of sectors on adjacent tracks is shown. The continuous band of gray code is shown as the fields N_{-1} through N_{+2}. The individual gray code fields are separated by gaps due to a phenomenon known as overlap erasure. This phenomenon is a consequence of the overlapping writing of the fields to the disk surface. A fringe field created at the borders of the read/write head when writing data to the disk surface will erase any pre-existing data for the width of the fringe field. For conventional read/write head voltages during writing, the overlap erasure width will range from between 100 and 160 microinches. While there is, therefore, a loss in recorded surface area carrying gray code information, the gray code fields of the present invention are written across the entire track width to form an effectively continuous gray code field band. Further, as previously noted, the gray code itself is chosen to encode the necessary information while differing as between the same sector on adjacent tracks by only a single bit. Consequently, even while seeking at high speed across the data tracks, an apparent gray code field read that captures a first portion of the gray code associated with one track and the remainder of the gray code field from an adjacent track will still generally yield an identification of the correct track number. An exception occurs where the single differentiating bit of the two adjacent tracks gray code is misread at the point that the read/write head is equally over adjacent gray code fields. In this exceedingly unique circumstance, there is an equal probability of reading the differentiating bit as either a one or a zero. Although this may result in decoding a wrong track number, the error is soft, i.e, non-repeating, and limited in the scope of the possible error. As a consequence of the present invention, there is no practical limitation on seek rate nor seek trajectory of the head with respect to gray code field crossings or servo bursts.

Also illustrated in Fig. 8 is the quad-servo burst pattern characteristic of the present invention. Each servo burst is independently written with a radial offset of one-half track width from the previous burst. The read/write head width, in accordance with the preferred embodiments of the present invention, is greater than or equal to sixty percent, but less than one hundred percent of the track width. Consequently, each servo burst overlaps its two radially-nearest servo bursts by less than one-half of a head width. The burst overlap, in terms of track width, is given as:

$$\text{Burst Overlap} = H - \frac{T}{2} \qquad \text{Eq. 3}$$

where H is the head width and T is the track width.

As illustrated in Fig. 8, a unique characteristic of the present invention is that none of the servo bursts are disposed symmetrically across the track center line of a data track. The servo bursts are servo track-written at one-half track offsets. However, the servo track-written tracks do not align with the data tracks that are subsequently used to store user data. Rather, as shown in Fig. 8, pairs of servo bursts, such as A and D with respect to track T_o (and T_{+2}) and bursts B and C with respect to track T_{-1} (and T_{+1}), will overlap a track center line. The overlap is asymmetric with respect to the individual servo bursts, but with respect to the pair displays a symmetric offset to either side of the data track center line. The other two servo bursts of a set of quad-servo fields are similarly offset in mirror symmetry from the same data track center line. The pattern of servo bursts repeats every other data track. However, the information content of the quad-servo burst field, and gray code fields, is the same for every data track.

As can be seen from Fig. 9, the position value determined by either Eq. 1 or Eq. 2 will vary nonlinearly depending on the read/write head offset from track center line. For an exemplary data track T_{+1}, a read head H_{+1} following its track center line will read equal voltage amplitudes from the B and C servo bursts. Equal but smaller values will be read from the A and D bursts. Consequently, the track error T_{ERR} will be zero. However, head drift toward track T_0 will result in a decrease, from zero, of the value computed by Eq. 1. As the center of the head moves radially past a point H-3/4T from the track center line, the D servo burst field associated with T_{+1} will no longer contribute to the value determined by Eq. 1. However, the contribution of the A and B servo burst fields will continue to increase at a rate greater than the decreasing contribution by the servo burst field C until the center point of the head radially moves past a point 1/4T from the track center line. After this point, as the head continues to move away from the track center line, the contribution due to servo burst field B decreases. However, Eq. 1 will continue to give an increasing result value until the center point of the head moves past a distance of 5/4T-H from track center line. At this point, the upper or outer edge of the read head will begin to read the D servo burst associated with the track T_0. As shown in Fig. 9, the result value of Eq. 1 thereafter begins to decrease and is no longer a directly proportional indicator of the distance of the head from the correct track center line. Consequently, the present invention affords a servo track following lock range of ±5/4T-H.

Since the head width H must be at least one-half the track width T, the maximum lock range of the present invention is ±6/8T. However, in accordance with the practical implementation of the present invention, a servo track following lock range of approximately ±5/8T utilizing a head width of approximately 70% of the track width or greater can be realized.

A particular advantage of the present invention is that the head to track width limitation applies only to the effective write profile width of the head. Consequently, a magneto-resistive head having a read profile width substantially less that the write profile width can be used. The read head profile width should be at least equal to the burst overlap H-T/2.

Inasmuch as the servo track following algorithm of the present invention is implemented in firmware executed by the microcontroller 24, the rate of change in the result value of either Eq. 1 or Eq. 2, depending on the specific track being followed, can be used to determine whether the head has drifted past the threshold distance of 5/4T-H. That is, the microcontroller 24 is well-suited and can readily adjust for the nonlinearities in the result value of Eqs. 1 and 2.

Referring now to Figs. 10a-e, the process of providing the continuous gray code band and quad-servo burst pattern in accordance with a preferred embodiment of the present invention is illustrated. As shown in Fig. 10a, a gray code field N_{-1} and servo burst A are written on the first pass of the head under the direction of a servo track-writer controller. The read/write head is then offset by 1/2 of a track width toward the inner diameter of the disk and a gray code field N and servo burst field B are written. The gray code field overwrites a portion of the N_{-1} gray code field. The overlap erasure associated with the writing of the gray code field N results in a gap between the N_{-1} and N gray code fields.

As shown in Fig. 10c, a second gray code field N is written, again offset by one-half of a track width toward that inner diameter of the disk. The servo burst field C is also written as shown. The servo burst pattern is completed as shown in Fig. 10d by the writing of a gray code field in N_{+1} and servo burst D field.

The next pass of the head, as shown in Fig. 10e, provides a second N_{+1} gray code field partially overlapping the N_{+1} provided in Fig. 10d. The same pass of the head is used to provide the next servo burst field A also at a one-half track offset from the fields provided in Fig. 10d. Consequently, the provision of the continuous gray code band and quad-servo burst fields of the present invention can be provided in a ready repeating pattern for all sectors and tracks.

Referring now to Fig. 11, the facility of the present invention to provide for the correction of servo track writer errors is illustrated. As shown in Fig. 11a, the servo burst field associated with the data track center line T_0 has been miswritten offset away from the track center line. The servo burst field B associated with the data track center line T_2 has been miswritten due to the presence of a surface defect at its position.

Referring now to Fig. 11b, the incorrect servo burst field C of track T_0 can be erased by track following exclusively on the B and D servo burst fields of the To data track, though offset a quarter track in complimentary directions on two successive passes to completely erase only the servo burst C. In a similar manner, the incorrectly written servo burst field associated with the T_2 data track can be erased. However, since the physical defect will prevent direct correction of the servo burst field B, two additional erasure passes are also made to erase the servo burst field C associated with the T_2 data track.

In a single pass, a replacement servo burst field C' can be written in its proper location with respect to the data track T_0 as shown in Fig. 11c. Accordingly, what would otherwise be a permanent source of offtrack errors has been completely corrected with the provision of the servo burst C'.

The servo burst error associated with the data track T_2, however, cannot be completely corrected, though the presence of a servo burst co-located defect does not require that the entire sector be declared as defective. Rather, by removal of the defective servo burst B and its pair servo burst C, the present invention can still maintain an adequate degree of track following accuracy based solely on the presence of the servo bursts A and D. The loss of the B and C servo burst fields, however, does result in a loss of track following range at the affected track and sector.

Thus, a system and method of using a quad-servo burst pattern for embedded servo track following and a quadrature algorithm having a significantly increased servo track following lock range has been disclosed. Further, utilization of the quad-servo burst pattern in conjunction with a continuous gray code band further utilized in conjunction with a second gray code band and quad-servo burst pattern at a mid-sector location within each data sector permits disk drive systems to operate with a very high track density for the realization of a high performance and high capacity disk drive system.

Claims

1. A data storage medium (12) having a servo pattern for providing servo information for the positioning of a head (20) with respect to data tracks (22) provided on its surface, each data track (22) including a series of data sectors, said servo pattern comprising four servo burst fields (A,B,C,D) provided in each data sector in a series ordered along the length of each data sector, each pair of servo burst fields in a predetermined data sector defining the data track center line (T_{CL}) of a respective data track as the mid-point of the mutual radial overlap of said pair of servoburst fields; characterised in that the radial width W of a servo burst field is related to the track radial width

T by 0.5T < W <= 1.0T, said pairs of servo burst fields radially overlapping by W-(T/2).

2. A data storage medium as claimed in claim 1, wherein each one of said servo burst fields radially uniformly overlaps its two radially nearest ones of said servo burst fields.

3. A data storage medium as claimed in claim 1 or claim 2, wherein the center points of each one of said four servo burst fields (A,B,C,D) are offset from the nearest radial ones of said four servo burst fields by one-half of a data track width, and wherein the center line of the associated data sector is defined as a line having a net zero radial offset from the center points of said servo bursts.

4. A disk drive control system operating from embedded servo control information comprising:

(a) a data storage medium (12) as claimed in any one of claims 1 to 3;
(b) actuator means (18), responsive to a position control signal, for positioning a head (20) with respect to said data tracks (22); and
(c) control means, coupled to said actuator means (18), for controlling the positioning of said head (20) with respect to said data tracks (22), said control means including means, coupled to said head, for obtaining a relative position value for each of said servo burst fields of a data sector, means for determining a track center line offset value as the difference of sums of pairs of said relative position values, and means, responsive to said track center line offset value, for providing said position control signal to said actuator means.

5. A system as claimed in claim 4, wherein said head (20) obtains a read voltage amplitude (V) corresponding to the proportion of the whole of a servo burst field that it crosses over, wherein the four servo burst fields are designated as A, B, C and D, respectively, and wherein said head is aligned with the predetermined data track center line when $\left|(V_A + V_B)-(V_C+V_D)\right| = 0$.

Patentansprüche

1. Datenspeichermedium (12), mit einem Servomuster zum Bereitstellen von Servoinformationen für die Positionierung eines Kopfes (20) hinsichtlich Datenspuren (22), die auf ihrer Oberfläche vorgesehen sind, wobei jede Datenspur (22) eine Folge von Datensektoren umfaßt, das Servomuster vier Servodatenblockfelder (A, B, C, D) aufweist, die in jedem Datensektor in einer Folge entlang der Länge jedes Datensektors angeordnet vorgesehen sind, jedes Paar von Servodatenblockfeldern in einem vorbestimmten Datensektor die Datenspur-Mittellinie (T_{CL}) einer jeweiligen Datenspur als den Mittelpunkt eines gegenseitigen radialen Überlappens des Paares von Servodatenblockfeldern definiert,
dadurch gekennzeichnet,
daß die radiale Breite W eines Servodatenblockfeldes zu der radialen Spurbreite T durch 0,5 T<W<=1,0T gegeben ist, wobei die Paare von Servodatenblockfeldern radial um W-(T/2) überlappen.

2. Datenspeichermedium nach Anspruch 1, wobei jedes der Servodatenblockfelder seine zwei radial am nächsten liegenden Servodatenblockfelder radial gleichförmig überlappt.

3. Datenspeichermedium nach Anspruch 1 oder 2, wobei die Mittelpunkte jedes der vier Servodatenblockfelder (A, B, C, D) von den radial am nächsten gelegenen der vier Servodatenblockfelder um die Hälfte einer Datenspurbreite versetzt sind, und wobei die Mittellinie des zugeordneten Datensektors als eine Linie mit einem radialen Nettoversatz von Null von den Mittelpunkten der Servodatenblöcke definiert ist.

4. Plattenlaufwerk-Steuersystem, das anhand eingebetteter Servosteuerinformationen arbeitet und folgendes aufweist:

a) ein Datenspeichermedium (12) nach einem der Ansprüche 1 bis 3;
b) eine Stellgliedeinrichtung (18), die auf ein Positionssteuersignal anspricht, um einen Kopf (20) hinsichtlich der Datenspuren (22) zu positionieren; und
c) eine Steuereinrichtung, die mit der Steligliedeinrichtung (18) verbunden ist, um die Positionierung des Kopfes (20) hinsichtlich der Datenspuren (22) zu steuern, wobei die Steuereinrichtung folgendes umfaßt: eine Einrichtung, die mit dem Kopf verbunden ist, um einen relativen Positionswert für jedes der Servodatenblockfelder eines Datensektors zu erhalten, eine Einrichtung, um einen Spurmittellinien-Versatz als die Differenz

der Summen von Paaren der relativen Positionswerte zu bestimmen, und eine Einrichtung, die auf den Spurmittellinien-Versatzwert anspricht, um das Positions-Steuersignal an die Stellgliedeinrichtung zu liefern.

5. System nach Anspruch 4, wobei der Kopf (20) eine Lesespannungsamplitude (V) erhält, die dem Gesamtanteil eines Servodatenblockfeldes entspricht, das er überquert, wobei die vier Servodatenblockfelder mit A, B, C bzw. D bezeichnet sind, und wobei der Kopf auf die vorbestimmte Datenspur-Mittellinie ausgerichtet ist, wenn $|(V_A + V_B)-(V_C+V_D)| = 0$ ist.

Revendications

1. Milieu support de données (12) comportant un motif d'asservissement destiné à procurer une information d'asservissement pour positionner une tête (20) par rapport à des pistes de données (22) formées sur sa surface, chaque piste de données (22) comprenant une série de secteurs de données, ledit motif d'asservissement comprenant quatre champs de séquence d'asservissement (A, B, C, D), prévus dans chaque secteur de données dans une série rangée selon la longueur de chaque secteur de données, chaque paire de champs de séquence d'asservissement dans un secteur prédéterminé de données définissant l'axe de piste de données (T_{CL}) d'une piste de données respective comme étant le point médian du chevauchement radial mutuel de ladite paire de champs de séquence d'asservissement ; caractérisé en ce que la largeur radiale (W) d'un champ de séquence d'asservissement est liée à la largeur radiale de piste (T) par la relation $0,5T < W \leq 1,0T$, lesdites paires de champs de séquence d'asservissement se chevauchant radialement de : W - (T/2).

2. Milieu support de données selon la revendication 1, dans lequel chacun desdits champs de séquence d'asservissement chevauche radialement de façon uniforme ses deux champs radialement les plus proches parmi lesdits champs de séquence d'asservissement.

3. Milieu support de données selon les revendications 1 ou 2, dans lequel les points centraux de chacun desdits quatre champs de séquence d'asservissement (A, B, C, D) sont décalés à partir des champs radialement les plus proches desdits quatre champs de séquence d'asservissement par une moitié d'une largeur de piste de données, et dans lequel l'axe du secteur de données associé est défini comme étant une ligne ayant un décalage radial net nul à partir des points centraux desdits champs de séquence d'asservissement.

4. Système de commande pour unité de disque fonctionnant à partir d'information intégrée de commande d'asservissement, comprenant :

   (a) un milieu support de données (12) selon l'une quelconque des revendications 1 à 3 ;
   (b) des moyens qui actionnent (18), sensibles à un signal de commande de position, pour positionner une tête (20) par rapport auxdites pistes de données (22) ; et
   (c) des moyens de commande, couplés auxdits moyens qui actionnent (18), pour commander le positionnement de ladite tête (20) par rapport auxdites pistes de données (22), lesdits moyens de commande comprenant des moyens, couplés à ladite tête, pour obtenir une valeur de position relative pour chacun desdits champs de séquence d'asservissement d'un secteur de données, des moyens pour déterminer une valeur de décalage d'axe de piste comme étant la différence des sommes des paires desdites valeurs de position relative, et des moyens, sensibles à ladite valeur de décalage d'axe de piste, pour donner audits moyens qui actionnent ledit signal de commande de position.

5. Système selon la revendication 4, dans lequel ladite tête (20) obtient une amplitude de tension de lecture (V) correspondant à la proportion de la totalité d'un champ de séquence d'asservissement qu'elle traverse, dans lequel les quatre champs de séquence d'asservissement sont respectivement désignés par A, B, C et D, et dans lequel ladite tête est alignée avec l'axe prédéterminé de piste de données lorsque $|(V_A + V_B)-(V_C+V_D)| = 0$.

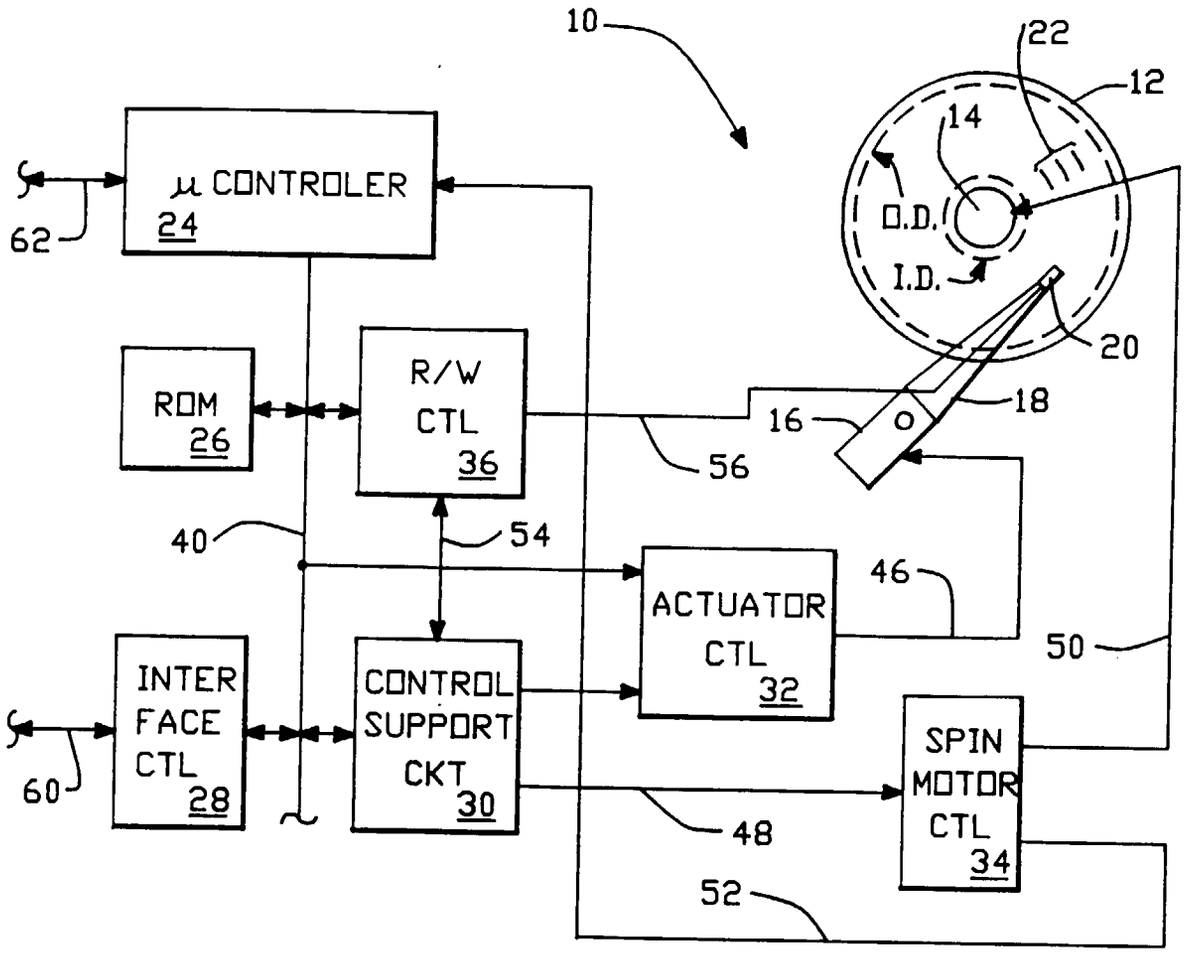

10
22
12
14
D.D.
I.D.
20
18
16
μ CONTROLER
24
62
ROM
26
R/W
CTL
36
56
40
54
46
ACTUATOR
CTL
32
50
INTER
FACE
CTL
28
60
CONTROL
SUPPORT
CKT
30
48
SPIN
MOTOR
CTL
34
52

FIG.-1

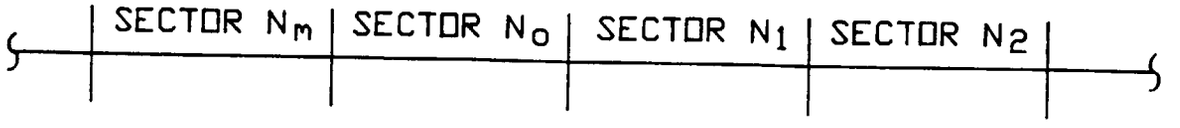

SECTOR N_m
SECTOR N_o
SECTOR N_1
SECTOR N_2

FIG.-2

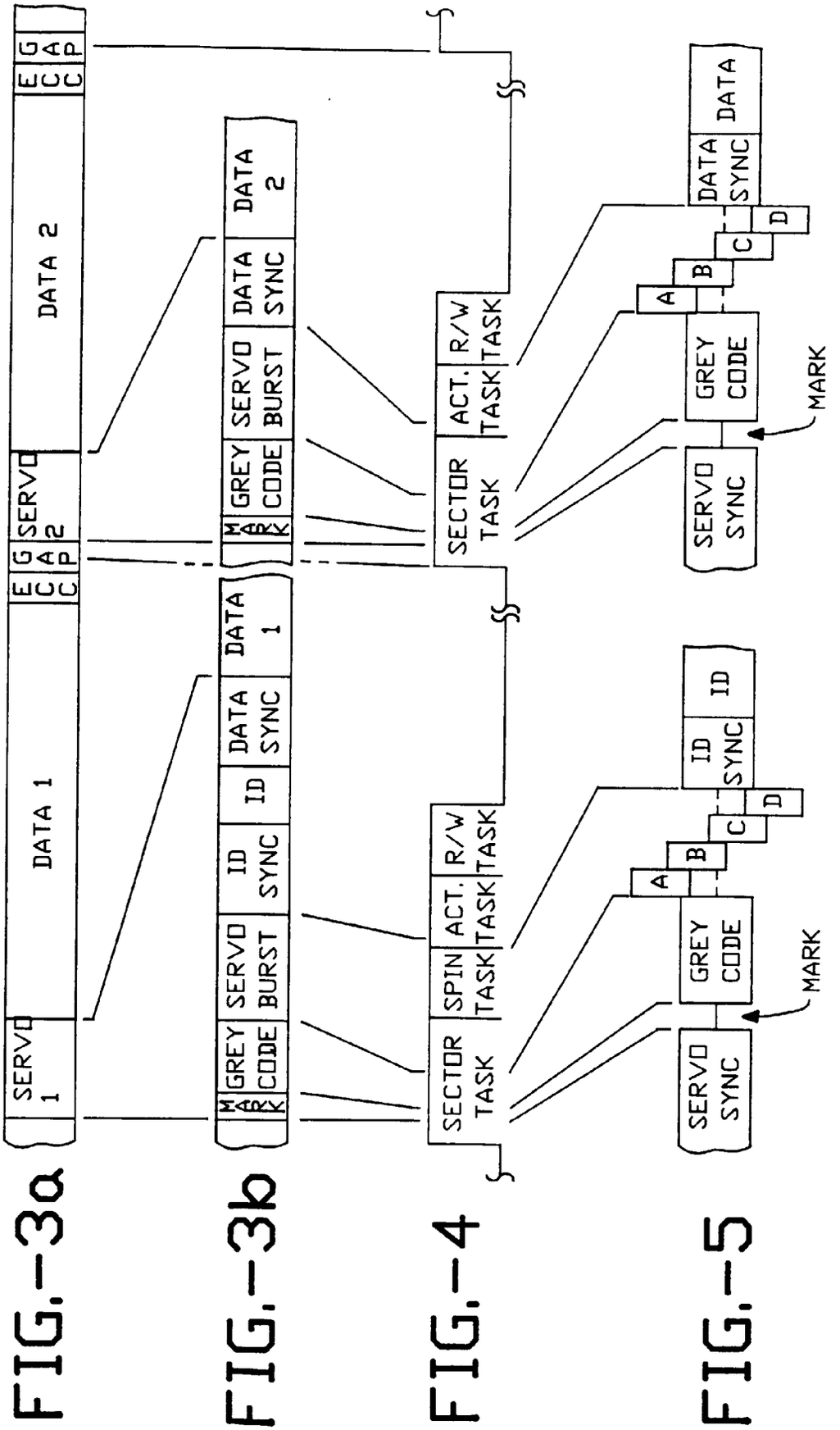


FIG.-3a

FIG.-3b

FIG.-4

FIG.-5

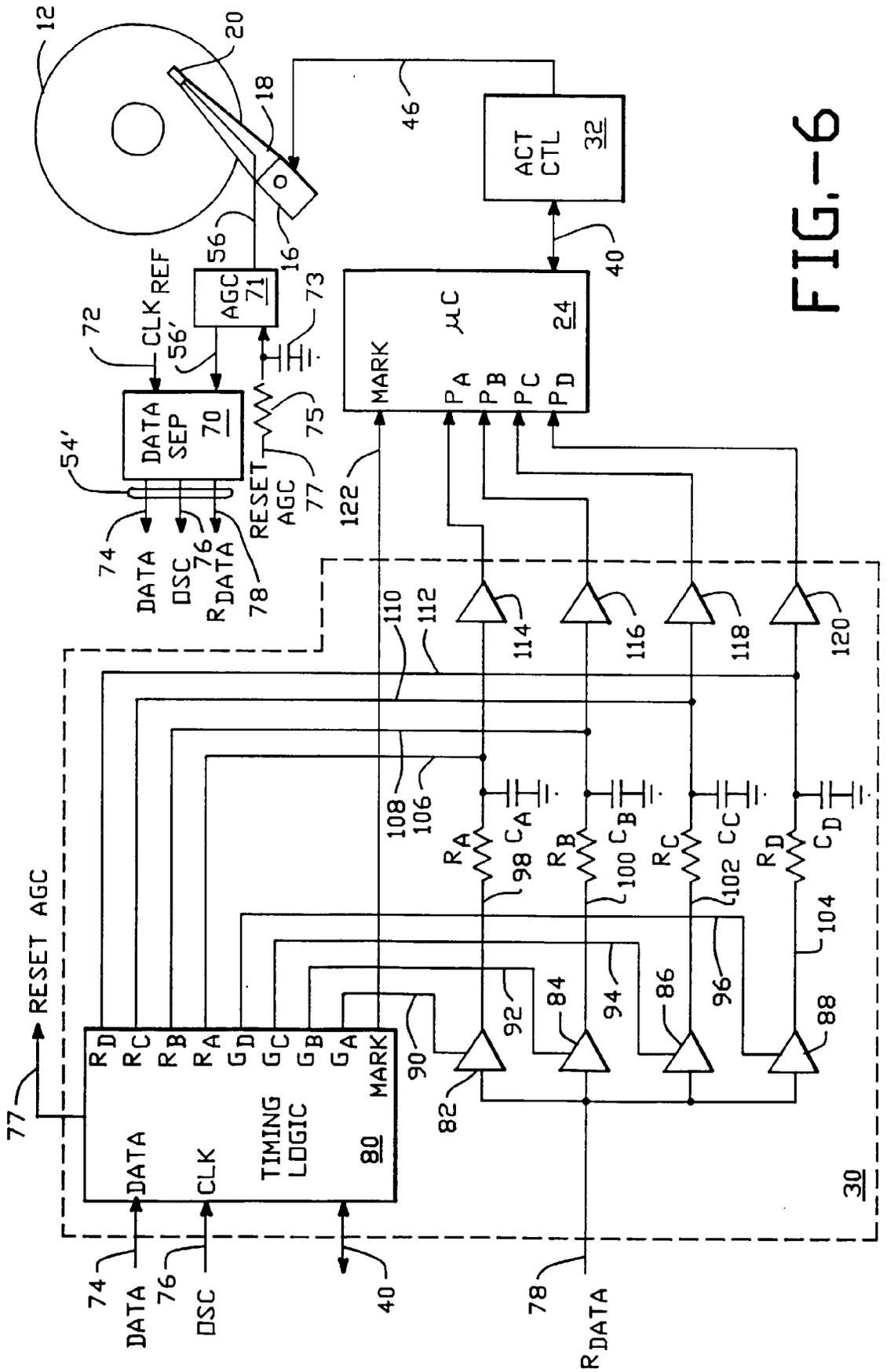

12
20
18
46
ACT CTL 32
40
56
16
AGC 71
CLK REF
72
56'
73
DATA SEP 70
54'
75
RESET AGC
77
74
DATA
OSC
76
R DATA
78
MARK
μC
24
P A
P B
P C
P D
122
110
112
114
116
118
120
108
106
R A
C A
98
R B
C B
100
R C
C C
102
R D
C D
104
RESET AGC
77
R D
R C
R B
R A
G D
G C
G B
G A
MARK
DATA
CLK
TIMING LOGIC
80
90
92
84
94
86
96
88
82
30
74
DATA
76
OSC
40
78
R DATA

FIG.-6

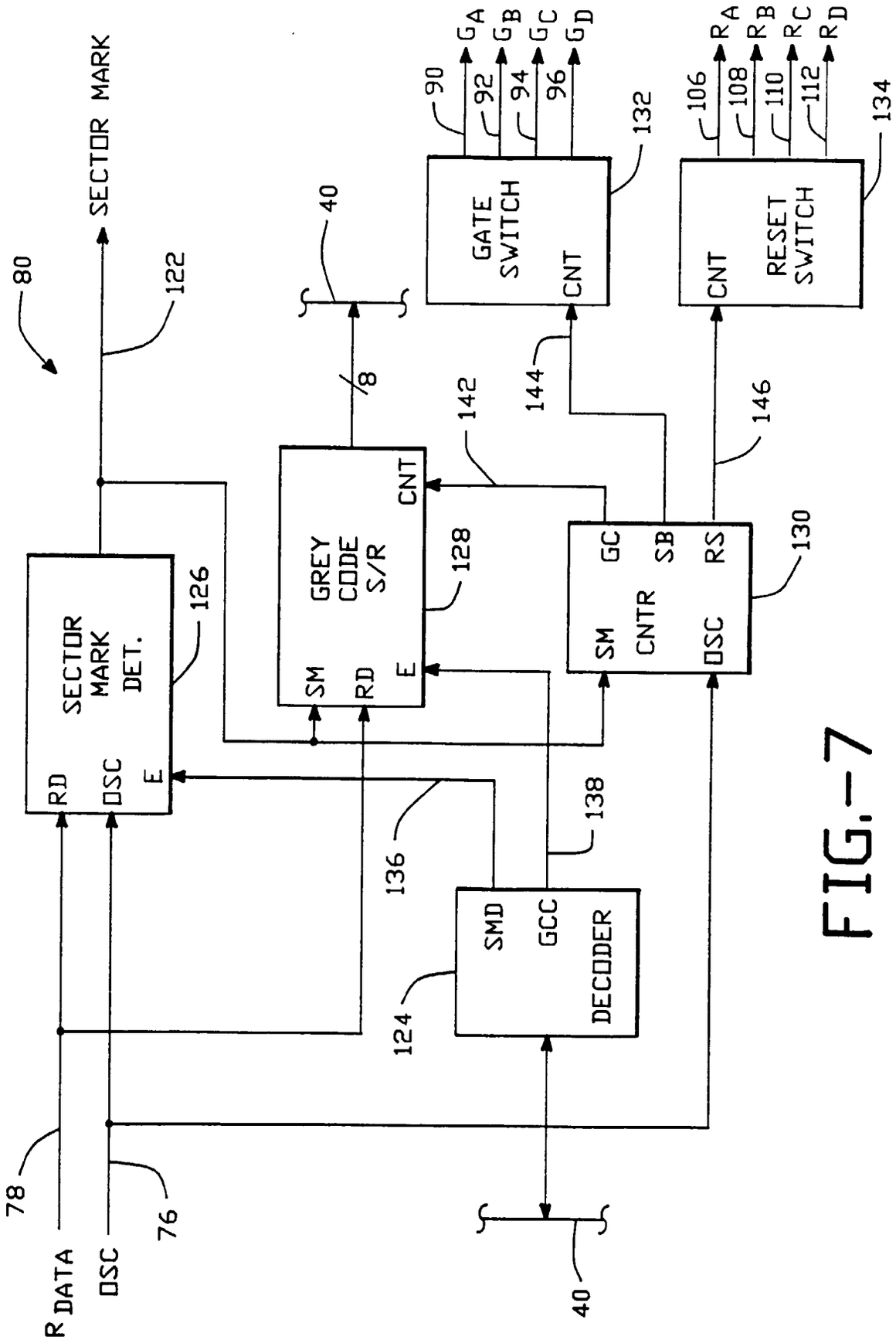
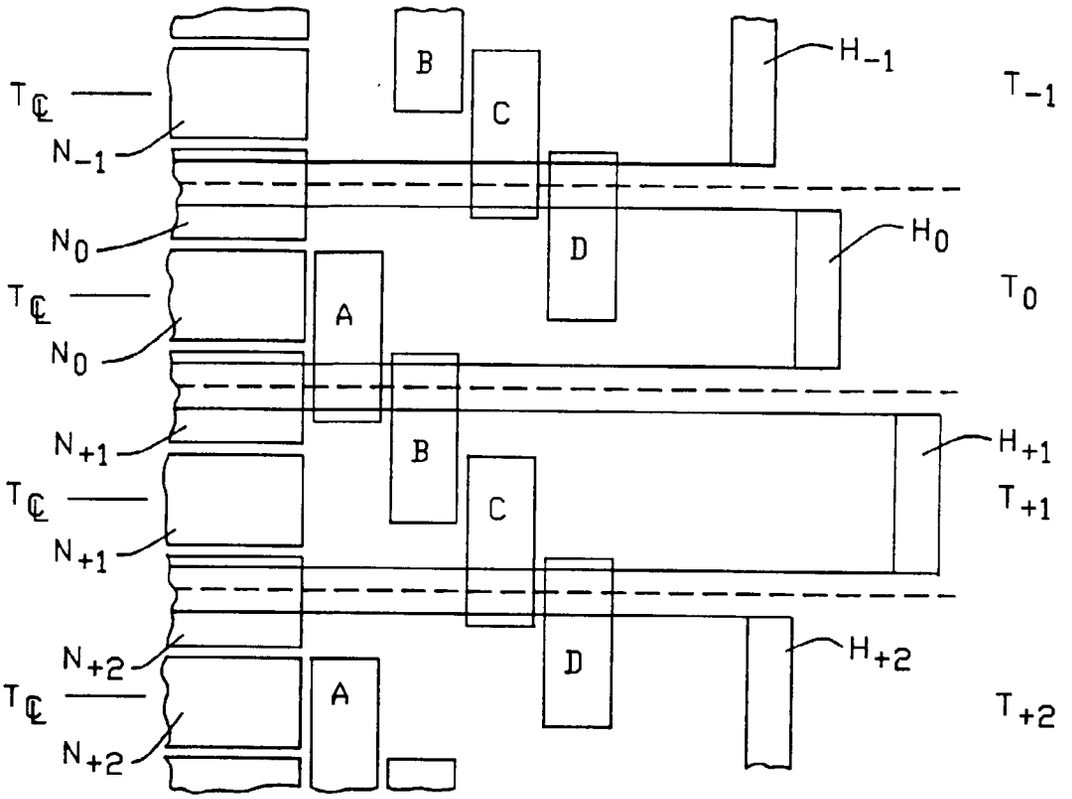
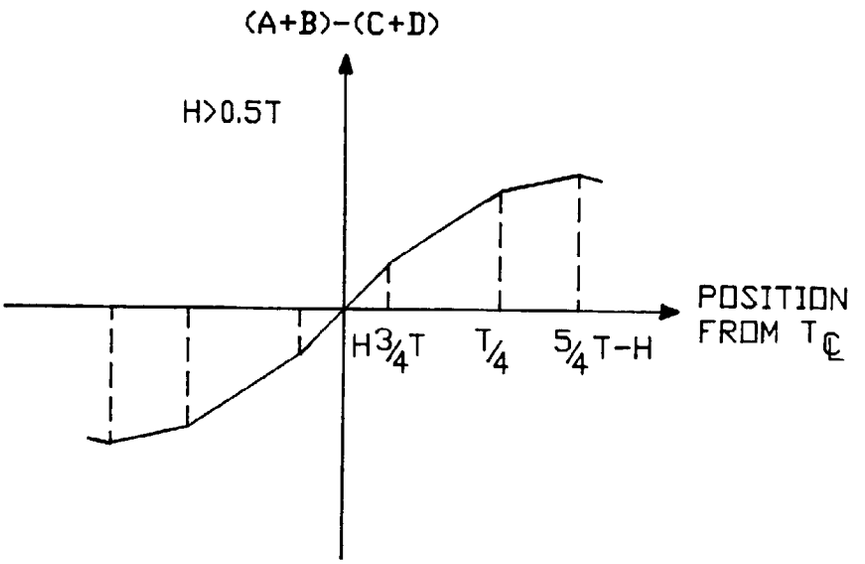

80
SECTOR MARK
122
40
8
GATE SWITCH
CNT
132
90
92
94
96
G_A
G_B
G_C
G_D
RESET SWITCH
CNT
134
106
108
110
112
R_A
R_B
R_C
R_D
142
144
146
GREY CODE S/R
CNT
128
SM
RD
E
SECTOR MARK DET.
126
RD
OSC
E
CNTR
GC
SB
RS
SM
OSC
130
136
138
SMD
GCC
DECODER
124
78
76
R_{DATA}
OSC
40

FIG.-7



$T_{\mathbb{C}}$
N_{-1}
N_0
$T_{\mathbb{C}}$
N_0
N_{+1}
$T_{\mathbb{C}}$
N_{+1}
N_{+2}
$T_{\mathbb{C}}$
N_{+2}
B
C
D
A
B
C
D
A
H_{-1}
T_{-1}
H_0
T_0
H_{+1}
T_{+1}
H_{+2}
T_{+2}

FIG.-8



(A+B)-(C+D)
H>0.5T
POSITION FROM $T_{\mathbb{C}}$
H
3/4T
T/4
5/4T-H

FIG.-9

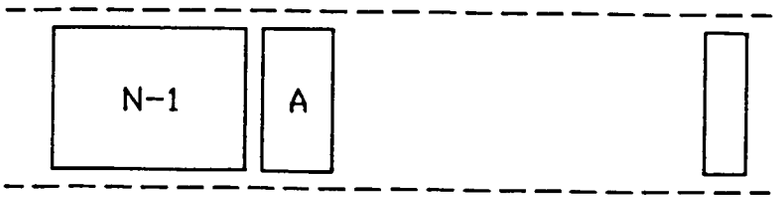


FIG.-10a

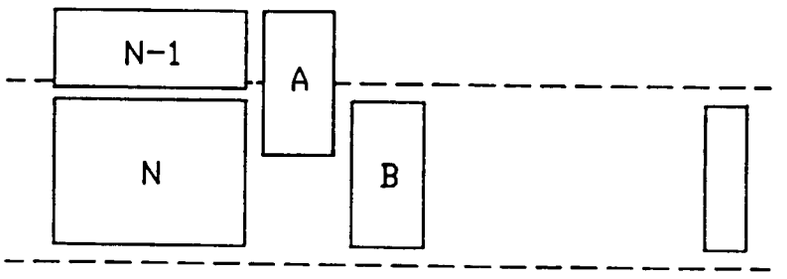


FIG.-10b

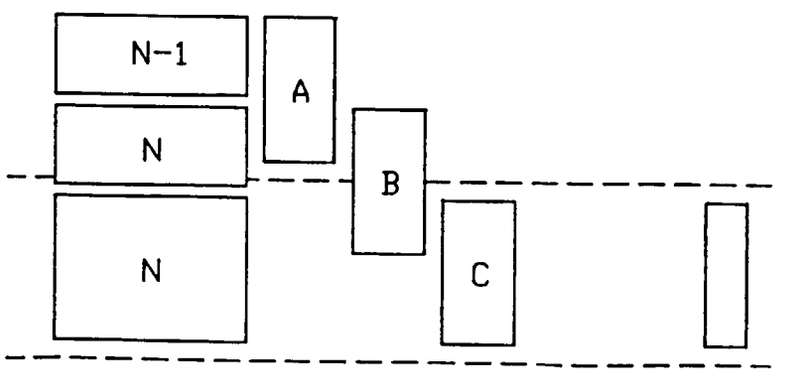


FIG.-10c

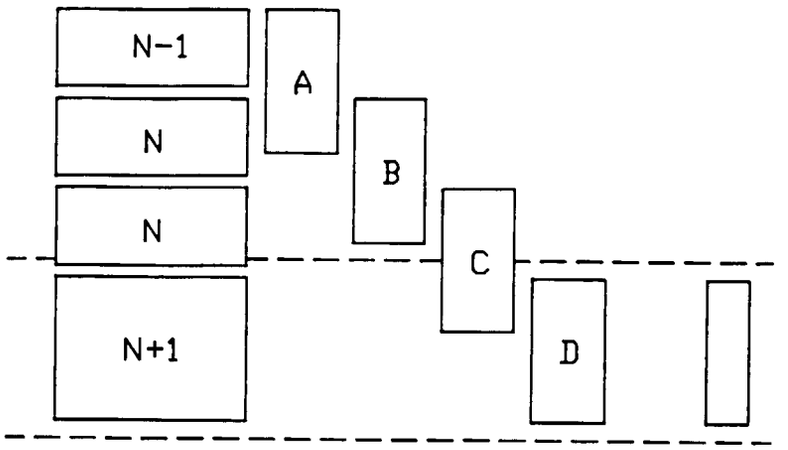


FIG.-10d

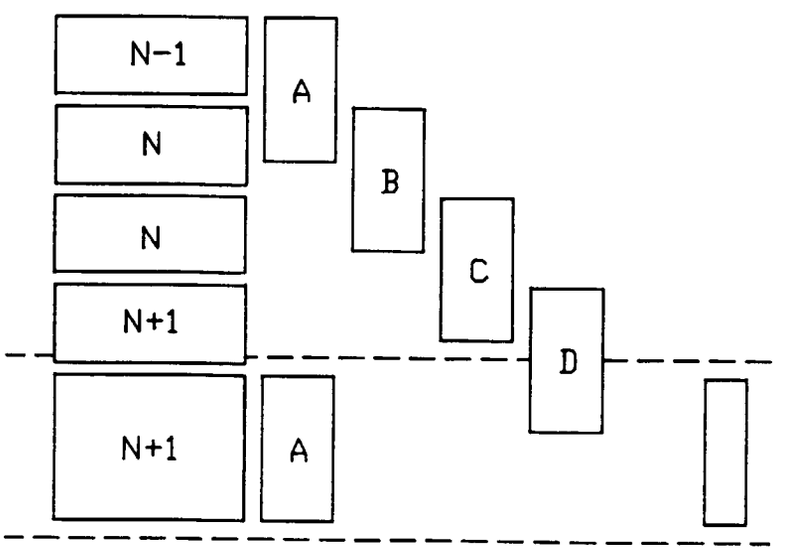


FIG.-10e

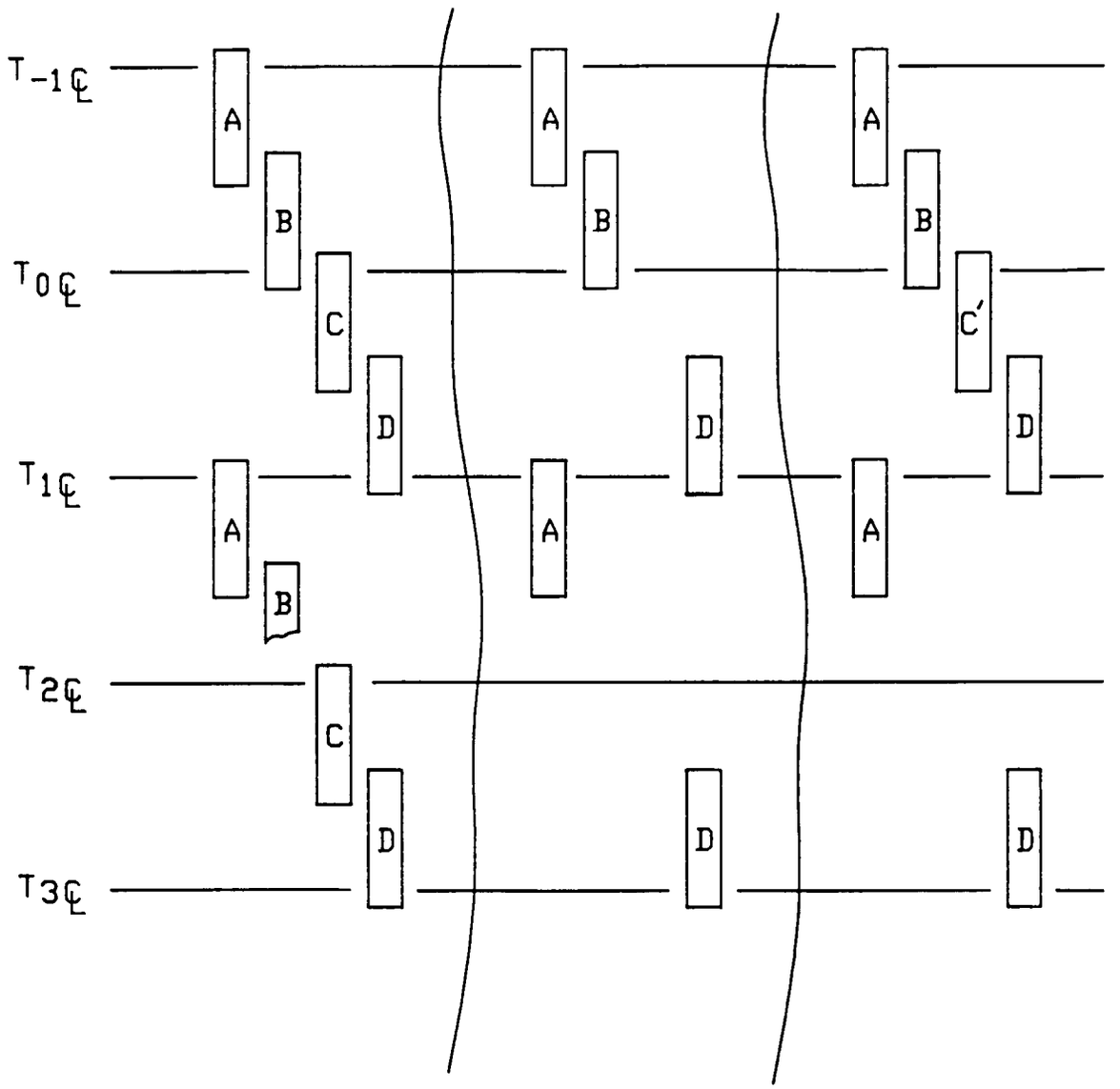


FIG.-11a FIG.-11b FIG.-11c