DESIGN GUIDELINES FOR PERIPHERAL ADAPTERS

USED ON THE

MP MICRO PROCESSOR DIGITAL COMPUTER

Second Edition

Revised

January 1974

CONTROL DATA CORPORATION
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INTRODUCTION

The MP micro processor digital computer is a general-purpose micro-programmable processor/emulator designed for application in a broad range of requirements. One basic hardware design, made up of modular elements, serves a variety of functions.

The architecture of the MP is based on the micro-programmable processor (MPP) developed by Control Data's Military Products Division. The MP is currently being developed by the Small Computer Development Division in La Jolla, California (LJLOPS). The physical structure of the MP is based on the NCR 605 mini-computer manufactured by NCR at Rancho Bernardo, California.

The MP is intended to be an "engine" for products designed by the various divisions of CDC. An individual user may find it necessary to design interface logic, and may find it desirable to put this logic on 11×14 printed wiring boards. Space and power are available in the MP card cage for this purpose.

The user may also elect to use his own card cage and card type to solve his problem. There is no intention to discourage the use of such hardware.

This document has been prepared to aid the user division in planning the design of 11×14 boards. You will also need:

- CDC Specification No. 88786800, MP17 System Specification
- CDC Specification No. 88782600, MP17 Power Supply Procurement Specification
- CDC Standard 1.60.004, Processing Multilayer Printed Wiring Boards, Using Plated Through Holes

MANAGEMENT GUIDELINES

Three plans can be followed in designing cards for the MP. The user division may lay out the card themselves, or have the Small Computer Development Division do it, or have NCR do it.

DO IT YOURSELF

The do-it-yourself approach has the advantage that the work is done close at hand and can be intimately controlled and followed by the user. If expected production quantities are small, the schedule is tight, and your drafting department has experience in PC board layout, this is the recommended procedure.

This document contains a set of PWB layout ground rules to assist you in laying out your PWB. Drawings of the three- and four-layer boards used on the MP program are also included for your information (see Figures 11 and 12).

If it is more economically feasible to house the user's interface, etc., in his own card cage on his desired board size, this is also acceptable. This document addresses only the 11×14 requirement; it should not be taken to exclude the above alternate approach.

LAYOUT BY SCDD

The drafting department at SCDD in La Jolla is experienced in the layout of 11×14 boards and offers this service to those divisions which do not have such resources. This offer is dependent on our workload of the moment, so you must contact the manager of engineering or the MP program manager at SCDD. We can provide layout, art work, parts lists, and assembly drawings, and can procure prototype boards for you. This cycle will take two to three months.

Logic diagrams which you provide to SCDD should follow the ground rules described in this document. We also suggest that you use circuits that are standard with CDC and/or the MP program. The logic designer should plan on close interface with the SCDD drafting department, preferably in person.

The SCDD prototype shop can order components and assemble small quantities (1 to 10) of boards for you. The SCDD preproduction facility in Sorrento Valley can assemble larger quantities (up to 100). A board tester is available in Sorrento Valley but requires test programming. Preparation of this test program is an effort that must be negotiated.

One layout cycle will cost about $5K. SCDD will estimate each specific job; an IDWO will be necessary to authorize the effort.

LAYOUT BY NCR

If the cards are to be produced in large quantities (at least 100, preferably 500 or more), at NCR, the layout and preparation of the manufacturing drawings must be done by NCR. In accordance with the CDC/NCR agreement, NCR will charge costs + 10% for the engineering effort. We have found that NCR costs are about the same as ours (or others). In accordance with the MP program policy, NCR will prepare all manufacturing drawings and specifications to their own practice and formats, using their part numbers. NCR will qualify all new parts by procuring and testing samples to their written component specs.

Your designer will be expected to interface intimately with the NCR layout man for several days. This time will be spent answering questions and advising the NCR test engineer who will be providing for test outputs so that the board can be tested later by computerized test equipment on the NCR production line. This test diagnostic is provided as part of the NCR factory overhead and, therefore, does not appear as a direct charge to you.

SCDD normally budgets $25K for two cycles of layout, sample boards, re-layout, and new sample boards and drawings. All this takes from five to six months.

Contact with NCR must be channeled through the MP program manager at SCDD. This is necessary to control the proliferation of instructions from CDC to NCR and to maintain a sensible program.

SCDD can obtain an estimate of NCR costs prior to start of work, but regardless of the estimate you will be billed actual costs.

NCR/RB is a high-volume manufacturing plant, and will design using their approved parts which are usually plastic. Plastic ICs are permitted in the MP17 program.

Logic diagrams presented to NCR for layout should follow the ground rules outlined in this document.

THE BACK PANEL

Several back panels are offered as standard on the MP program, and they should be used if at all possible. Each panel has 26 card spaces. Standard configurations rarely use all the spaces, so empty ones are available for your use.

At present, the MP power supply has sufficient power to run a full MP card cage, so power is probably available to run your cards. In addition, the MP power supply frame can hold an additional power supply. The MAGOPS and Scott designs are modular and permit paralleling of several supplies.

Wire-wrapping of the back panel is normally done on Gardner-Denver machines. If the back panel wire-wrapping is complex and/or volume is high, NCR will machine-wrap it for you. This scheduling into the NCR production flow must be arranged and planned in advance. All back panels can be wire-wrapped manually.

A special back panel for your particular use can be provided.

PRODUCT DESCRIPTION

The MP is a small-scale, stored program, parallel mode, digital computer. The MP is a basic micro processor which can be configured in many different forms with the same basic hardware. The following definitions are given for a common base of reference:

- MP16 - A 16-bit MP processing element with an application-defined micro program. May have no main memory or up to 256K of main memory, as defined by the application.
- MP32 - A 32-bit MP processing element with an application-defined micro program. May have no main memory or 8K or 16K of either 16-bit or 32-bit main memory, as defined by the application.
- MP17 - A 16-bit MP processing element operating as an enhanced CDC 1700 computer.
- MP17 Mini - A 16-bit MP processing element configured with 900 nanosecond 1704 capabilities and enhanced instruction set with from 8K to 32K of main memory.
- MP17 Maxi - A 16-bit MP processing element configured with 900 nanosecond 1714 capabilities and enhanced instruction set with 8K to a maximum of 256K main memory, and multiprocessor capabilities to four CPUs sharing common direct-addressable main memory.

The processor is made up of a minimum of three of the six blocks shown in the system block diagram (Figure 1). The minimum blocks are:

1. Micro Processor
2. Maintenance Interface/Maintenance Panel*
3. Micro Memory

---

*Optional if ROM micro memory is used.

This minimum configuration can be utilized in a peripheral controller or I/O processor type application. However, the complete configuration (shown in Figure 1) is more typical of a two-level computer with the micro processor emulation program stored in the main memory. Figure 2 is a block diagram of the micro processor.

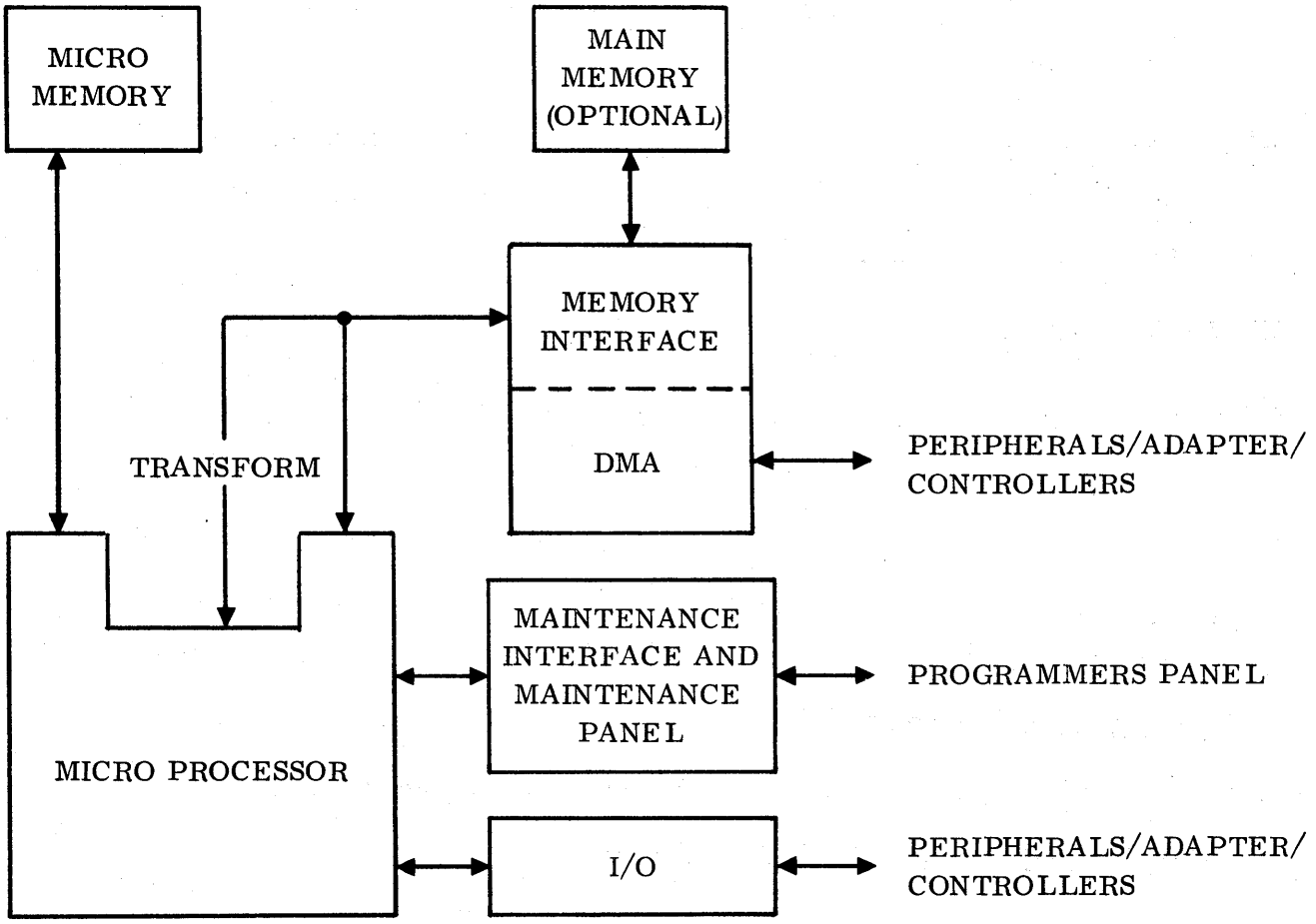


Figure 1. System Block Diagram

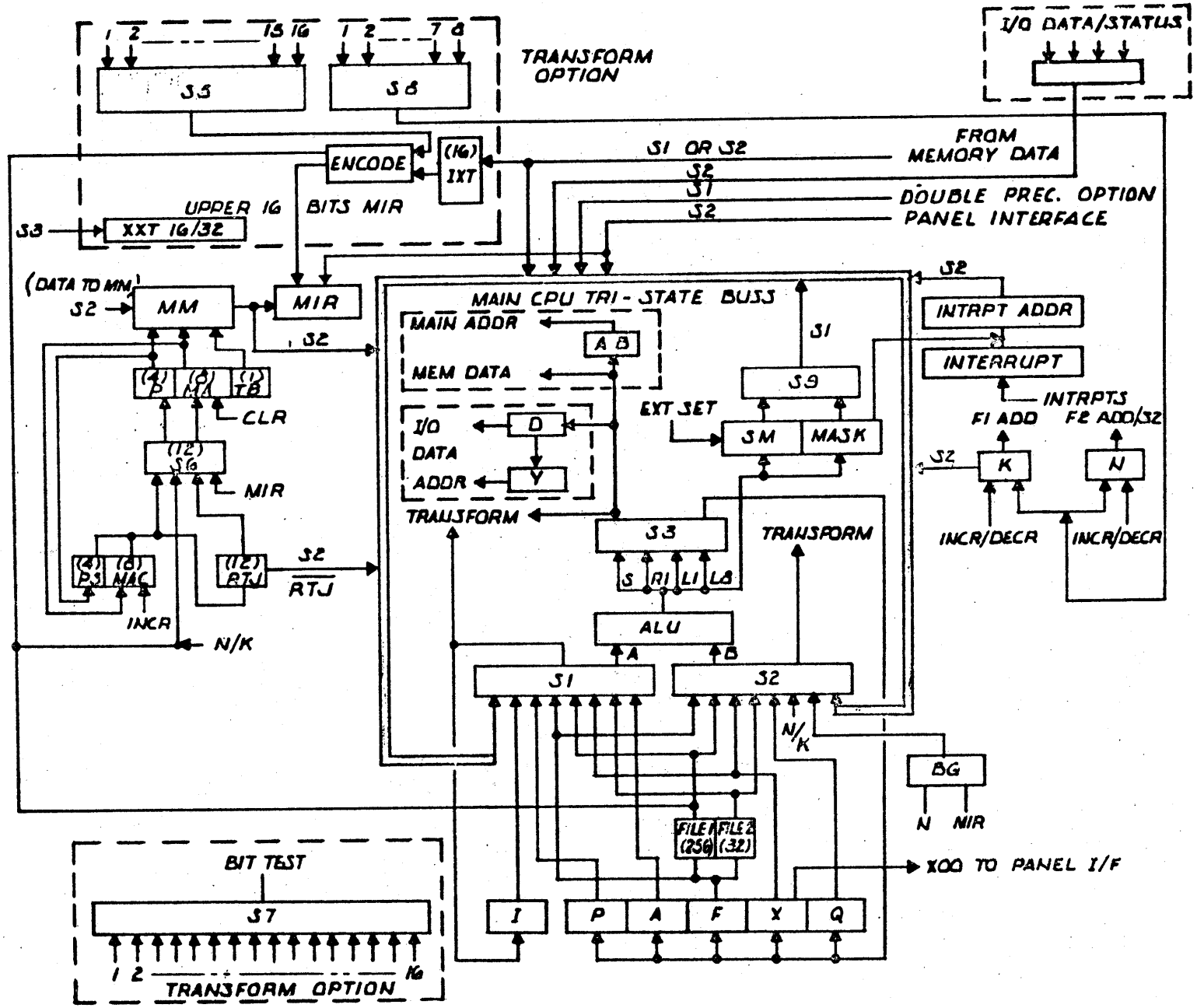


Figure 2. Detailed Micro Processor Block Diagram

BACK PANELS

Four prewired back panels are available depending upon the equipment configuration:

1. MP32
2. MP16 or MP17 Mini

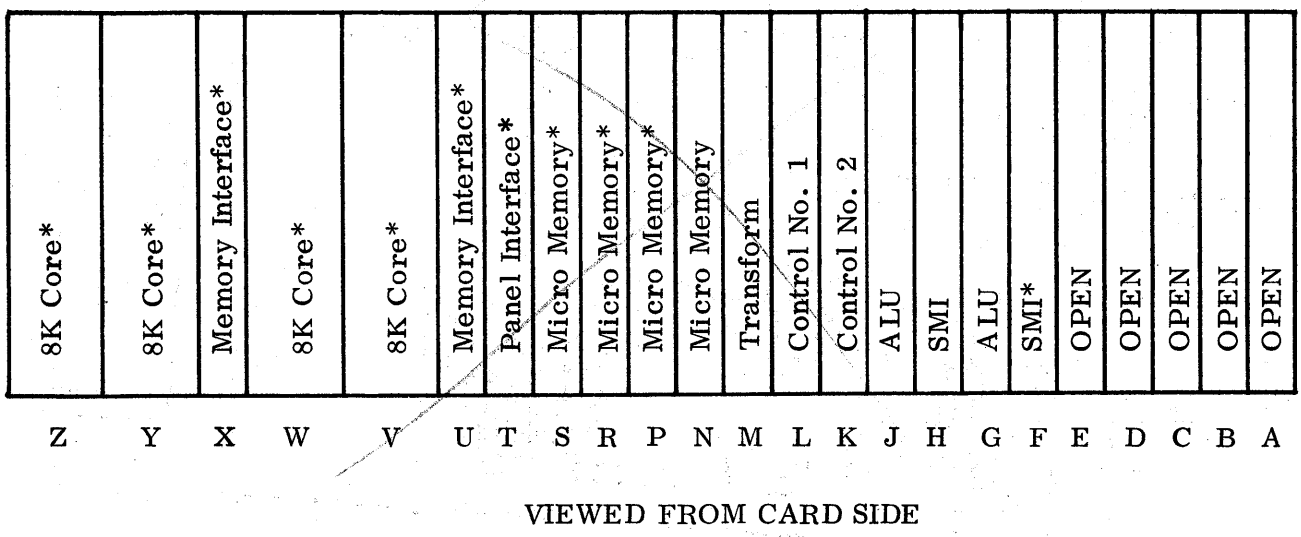
3A. MP16 or MP17 Maxi with CPU

3B. MP MOS memory, I/O, DMA expansion without CPU

4. MP core memory, I/O, and DMA expansion

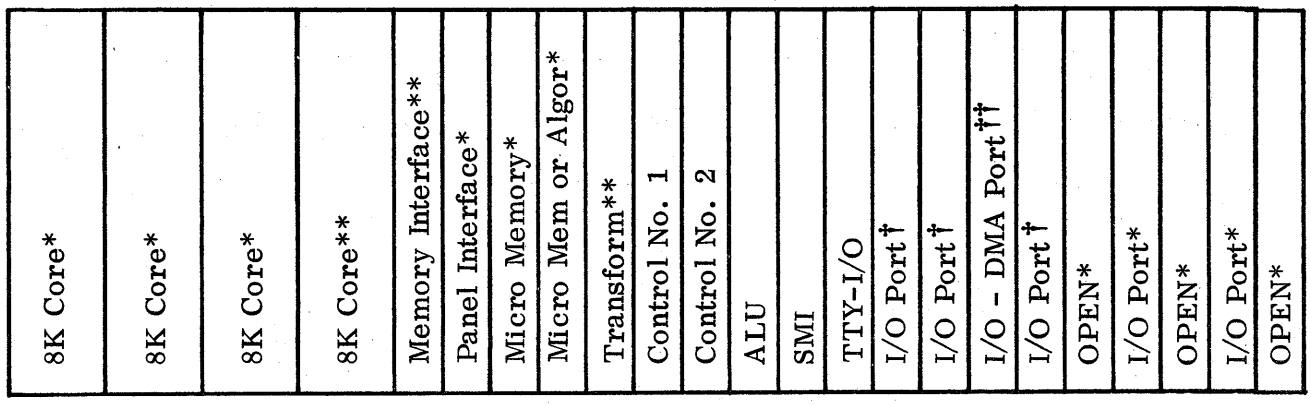
Refer to Figures 3 through 7 for the slot assignments for the various configurations.

NOTE: Space/open slots adjacent to I/O ports are unwired except for power; they may be custom-wired to accommodate multiboard controllers. Open slots in the MP32 chassis are unwired; they may be custom-wired to accommodate 16- or 32-bit I/O operation.



*Optional Cards

Figure 3. Configuration No. 1 (MP32)



VIEWED FROM CARD SIDE

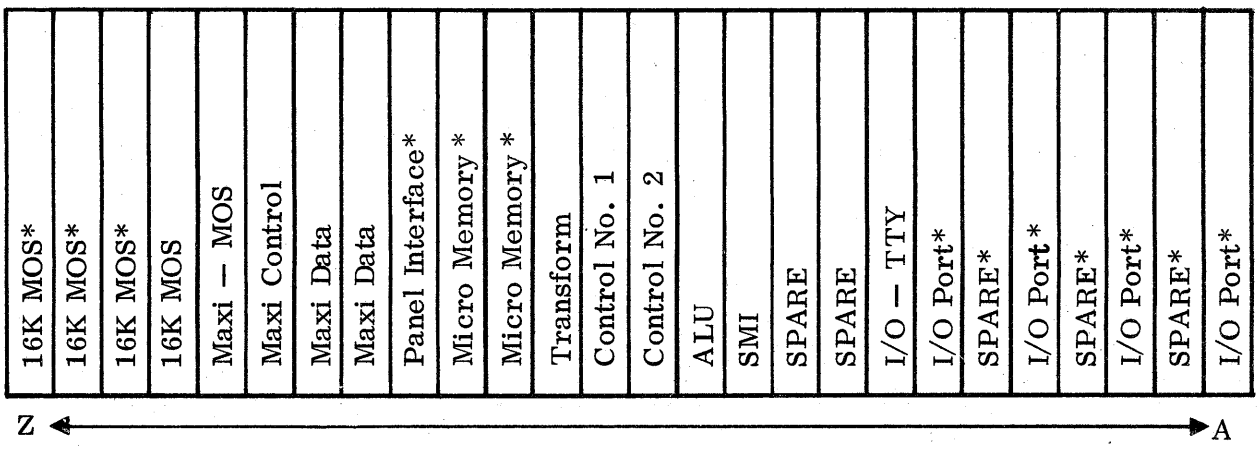
*Optional cards (MP16 and MP17)

**Optional cards (MP16 only)

†Prewired to include all the MO5 and A/Q-I/O signals

††Prewired to include all the MO5, A/Q-I/O, and DMA signals

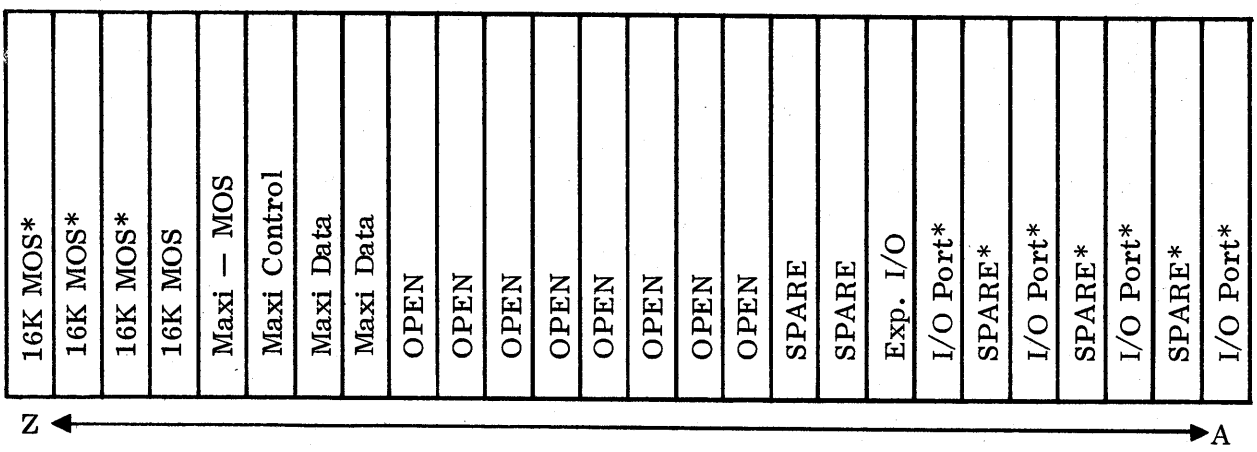
Figure 4. Configuration No. 2 (MP16 or MP17 Mini)



VIEWED FROM CARD SIDE

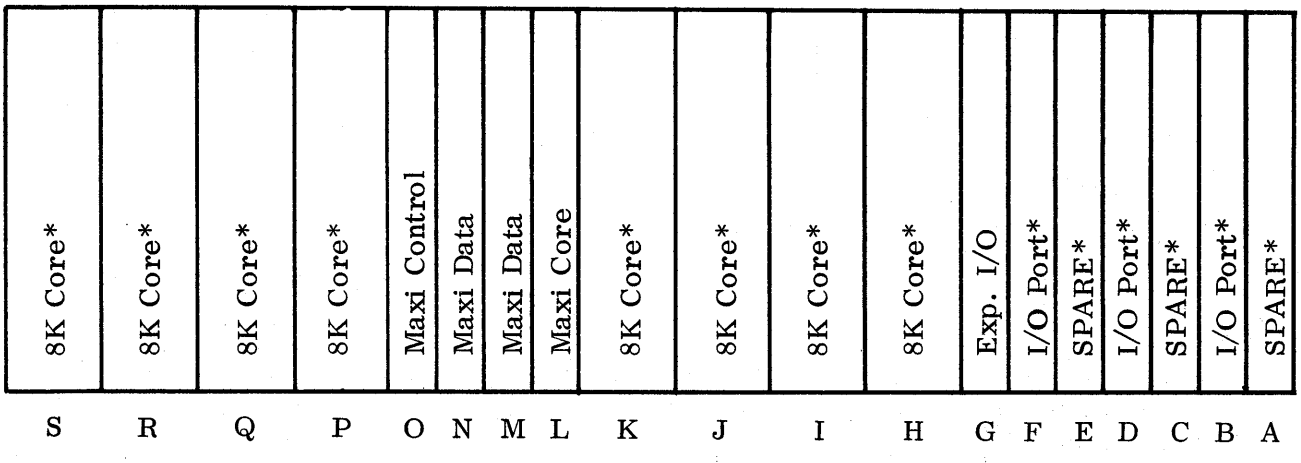
*Optional cards

Figure 5. Configuration No. 3A (MP16 or MP17 Maxi with CPU)



VIEWED FROM CARD SIDE

Figure 6. Configuration No. 3B (MP MOS Memory)



VIEWED FROM CARD SIDE

*Optional cards

Figure 7. Configuration No. 4 (MP Core Memory)

MP PHYSICAL PROPERTIES

The MP main chassis, expansion chassis, maintenance panel, and power supply enclosure can all be mounted on any standard 19-inch RETMA rack. Physical dimensions of each are:

	Height	Depth	Width
Main/Expansion Chassis	18.50 inches	12 inches	17.5 inches
Power Supply	8.75 inches	16 inches	17.5 inches
Maintenance Panel	4.50 inches		16.0 inches

See Figures 8 and 9 for front and rear views of the components.

NOTE: The maintenance panel is intended to be attached to the logic chassis as shown in Figure 8.

CABINETS

Two cabinets to house the CPU are currently under development by SCDD. Figure 10 is an artist's rendering of both the single unit and the double, together with a CRT and a card reader. These cabinets will be available to users of the MP and may be ordered from SCDD.

ELECTRICAL PROPERTIES

The power supply enclosure can accommodate various combinations of the power supplies listed in Table 1. Equipment configuration will determine which voltage and current outputs are required. For example, main memory requires ±15v and I/O requires ±12v. TTL logic requires ±5v. Refer to CDC Specification 88782600 for additional power supply information.

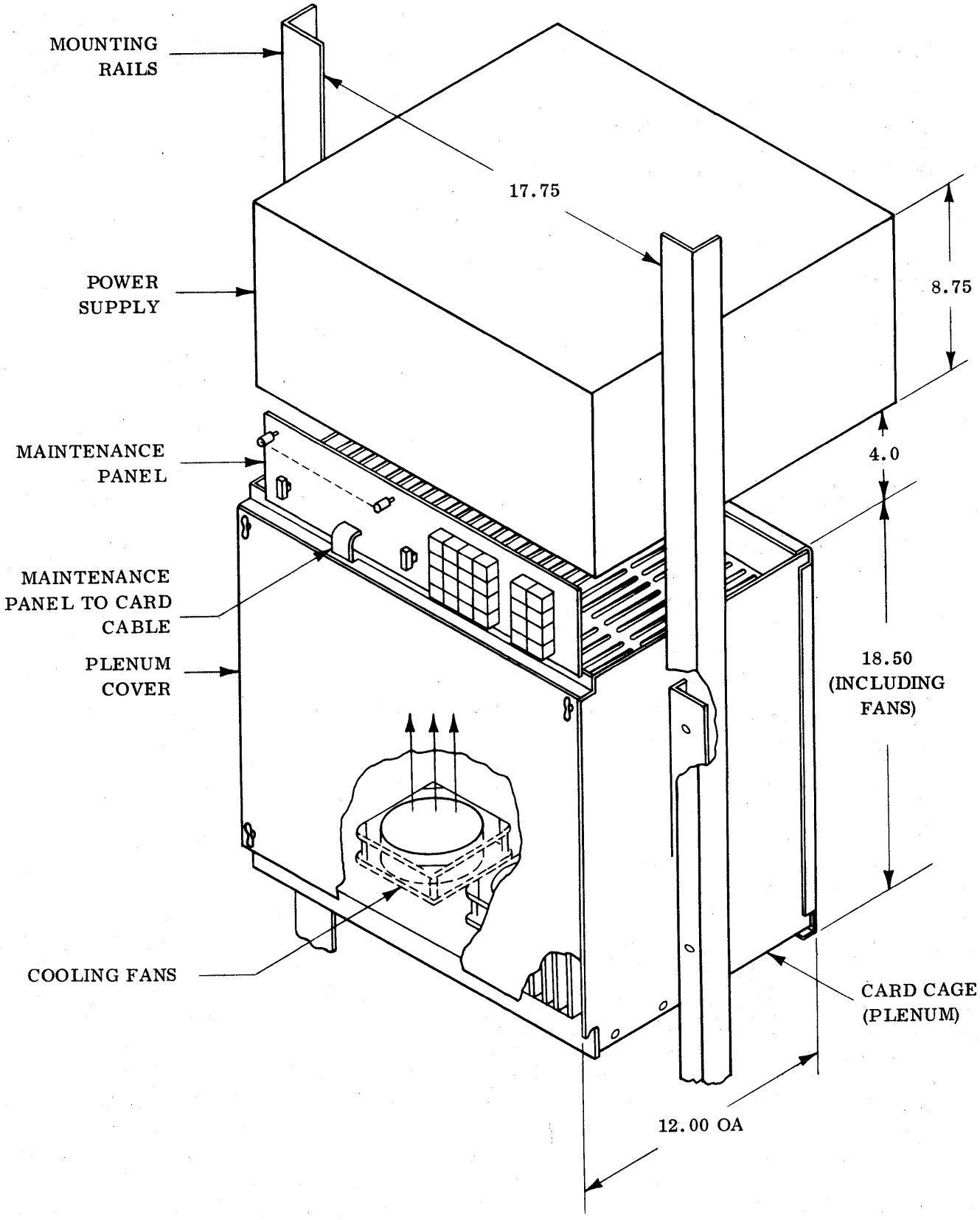


Figure 8. MP, Front View

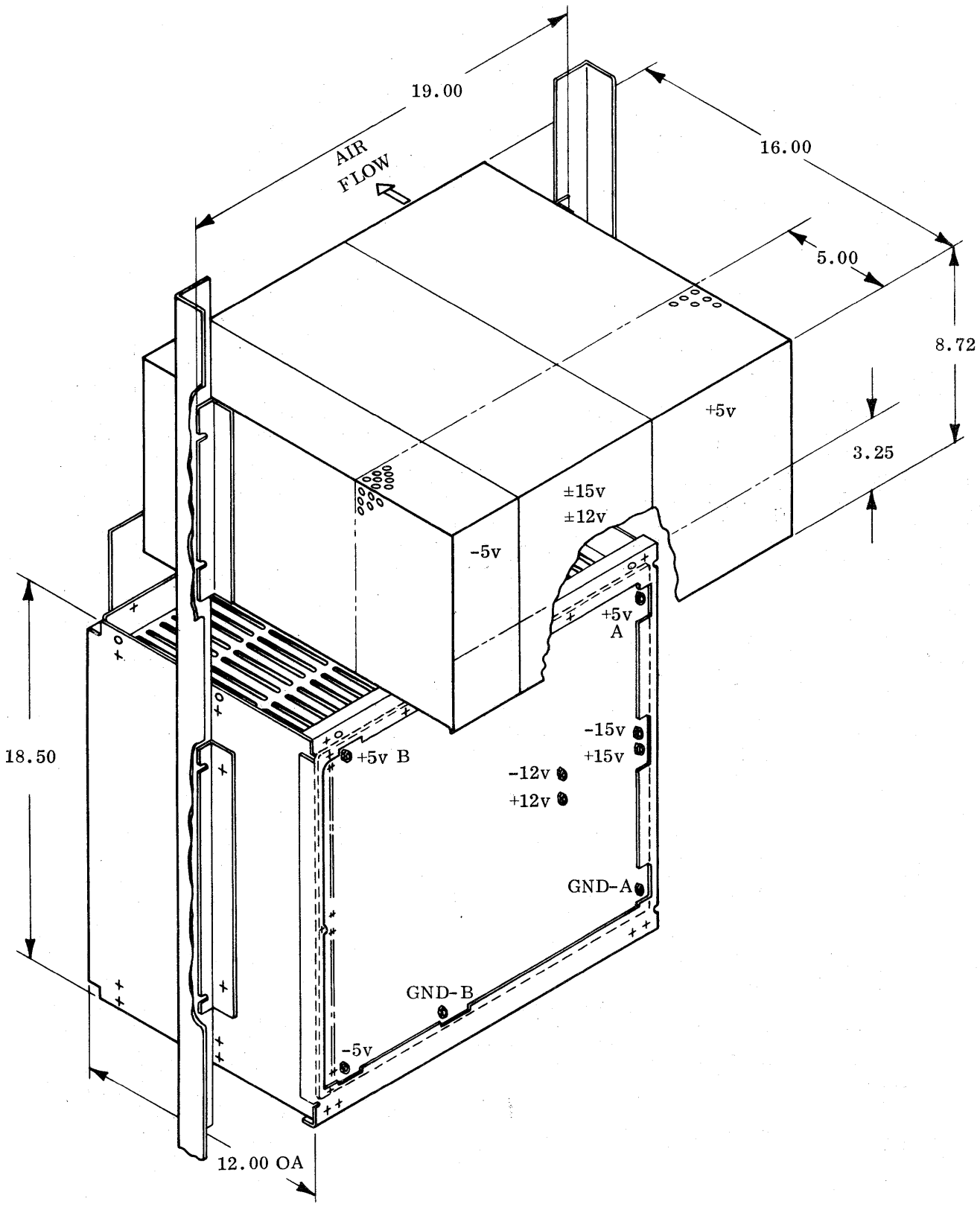


Figure 9. MP, Rear View

Table 1. MP Power Supplies

(1) (MAGOPS) CDC P/N	(2) (SCOTT) CDC P/N	NOM. OUTPUT VOLTAGE (VOLTS)	OVER-VOLTAGE MAX VOLTS	OUTPUT CURRENT (AMPS)	OVER CURRENT CUT OFF POINT (AMPS MAX)	WEIGHT (POUNDS)
88782601		+5	+6.2	50	55	20
88782602		+5	+6.2	100	110	35
	88782623	+5	+6.2	112	125	35
88782604	88782624	+12 -12 +15 -15	+15 -15 +18 -18	2 2 5 9	4 4 7 10	20
88782605	88782625	-5	-6.2	10	12	15
88782606		+12 -12 +15 -15 -5	+15 -15 +18 -18 -6.2	2 2 5 9 10	4 4 7 10 12	35
88782607	88782627	N/A	N/A	N/A	N/A	N/A

(1) MAGOPS POWER SUPPLIES CANNOT BE INSTALLED WITH SCOTT POWER SUPPLIES OR MOUNTING FRAME.

(2) SCOTT POWER SUPPLIES CANNOT BE INSTALLED WITH MAGOPS POWER SUPPLIES OR MOUNTING FRAME.

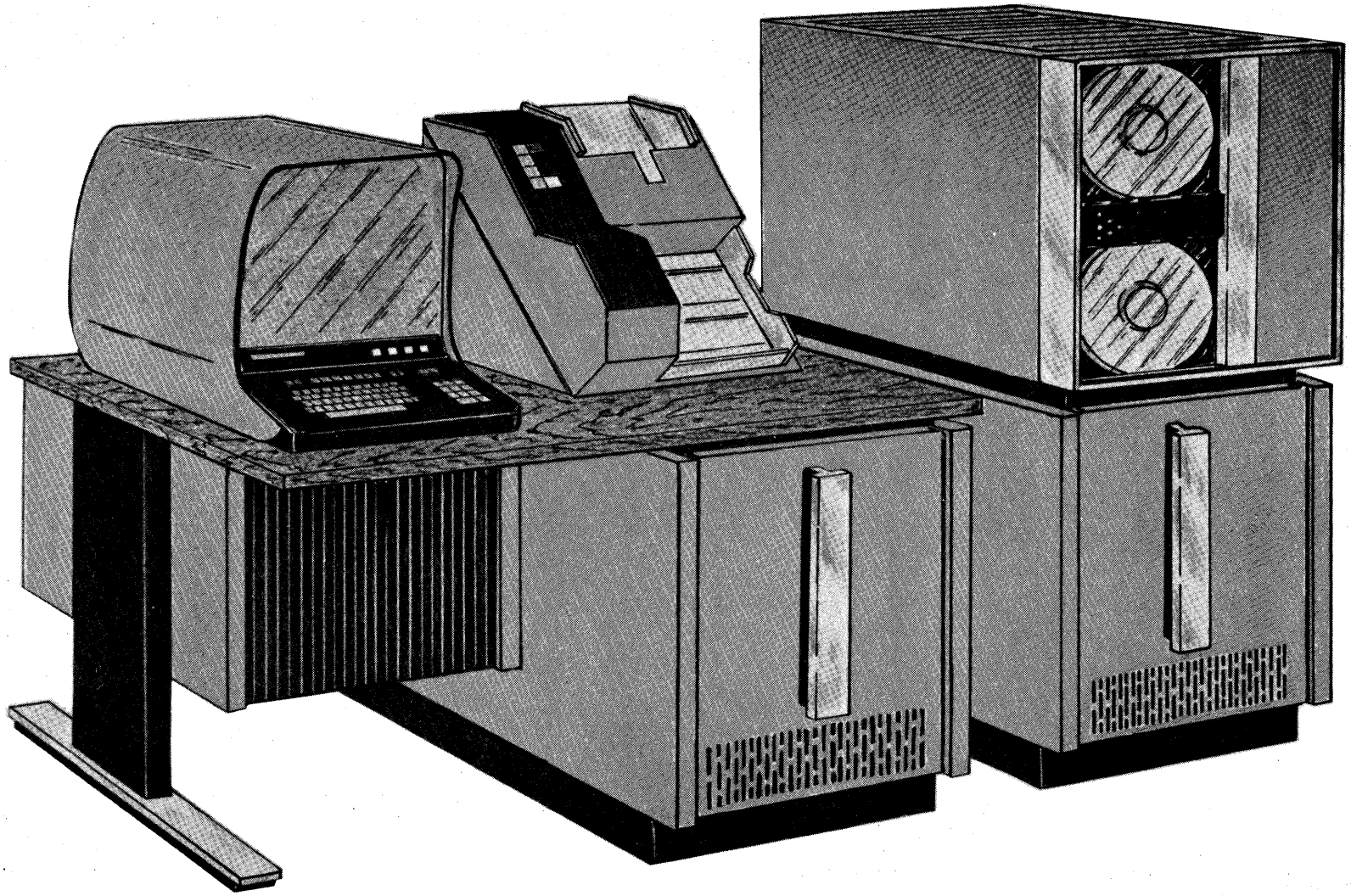


Figure 10. The Single- and Double-Unit Cabinets

Standard power connections to MP boards are as follows:

Board Type	Pin No.	Function
All	1, 2, 201, 202	+5v
All	101, 102, 301, 302	Ground
Memory	52, 53, 252, 253	+15v (if used)
Memory	50, 51, 250, 251	-15v (if used)
Interface	52	+12v (if used)
Interface	51	-12v (if used)
Special	100, 300	-5v (if used)

COOLING

Forced air cooling is provided by fans in the main chassis, expansion chassis, and power supply enclosure.

NOTE: Bus bars on MP boards must be parallel to the connector so as to not inhibit air flow.

GROUND RULES AND LOGIC DESIGN GUIDELINES

CIRCUITS

The logic circuits must be standard 74 (medium-speed) and 74H (high-speed) units. Special circuits, such as line drivers (75325), line receivers (75107), sense amplifiers (7539), etc. are allowed.

GROUND PLANE

The ground plane is a printed conducting plane which serves as the reference zero potential and return current sink. It is recommended that the ground plane cover 50% of the PC board.

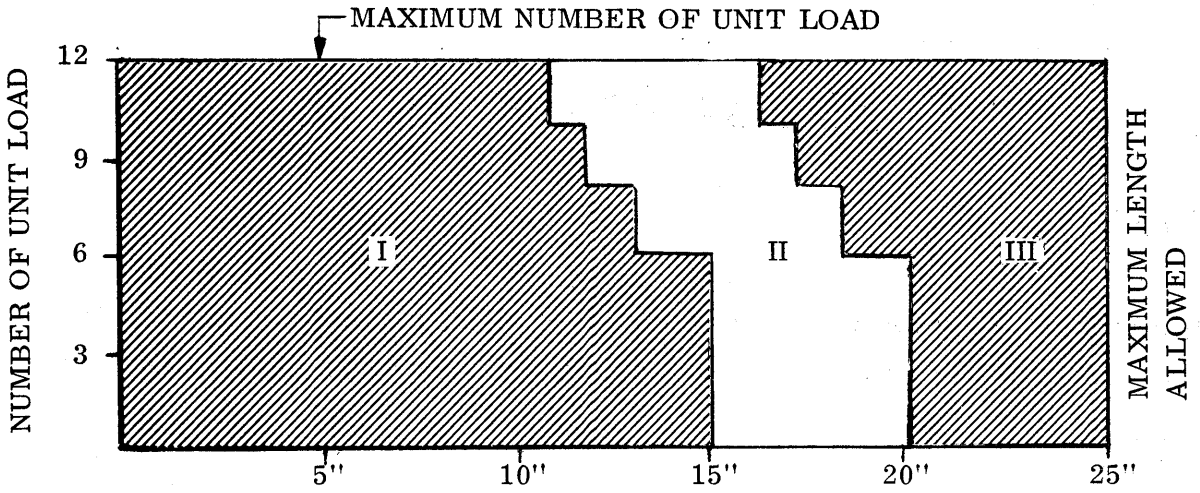
SIGNAL INTERCONNECTION PATHS

The characteristic impedance of the clad should be about 82 to 90 ohms.

Only serial nets are allowed on the PC board. A serial net is defined as a net with its source and load(s) connected in a daisy-chain fashion. Stub lengths should be less than 1/4 inch.

Radial nets are allowed on the back panel only. For example, a clock signal may have to be distributed to every card, so each stub on those cards may be another series net. In this case, a buffer must be located near the edge connector so the stubs become less than two inches long.

The maximum length of the microstrip line is shown in the following diagram.



Where: Area I — There are no restrictions on the load space for either high- or medium-speed circuits.

Area II — There are no restrictions on load space for medium-speed circuits, and the equal space rule should be observed for high-speed circuits.

Area III — The equal space rule should be observed for both high- and medium-speed circuits.

Equal Space Rule

When the total length of the net is longer than specified in the diagram above, then:

(1) Medium-speed circuits allow no more than 4 unit loads/3 inches.

(2) High-speed circuits allow no more than 3 unit loads/1 inch, when the total length is from 9 to 15 inches.

(3) High-speed circuits allow no more than 4 unit loads/2 inches, when the total length is from 15 to 20 inches.

---

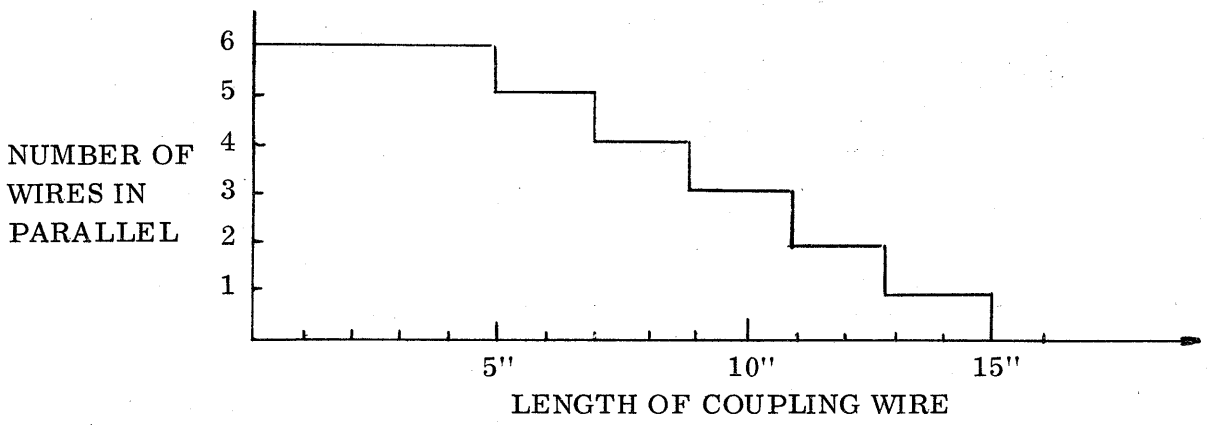
*Unit Load = The equivalent input impedance of the 74 TTL family at a specific voltage level; i.e., $I_{IL} \approx -1.6$ ma, $I_{IH} \approx 40$ μa, shunt with 4 pf capacitance.

(4) High-speed circuits allow no more than 3 unit loads/2 inches, when the total length is from 20 to 25 inches.

Parallel Paths

Two or more printed wires have parallel paths. Their signals may switch simultaneously, in which case the following rule should be observed:

The medium-speed line is parallel to all other medium-speed lines.



One line driven by a high-speed circuit is equivalent to two lines driven by a medium-speed circuit, because of the rise and fall times. Therefore, the above diagram applies to both types of circuits once you know the equivalent number of parallel lines.

POWER DISTRIBUTION

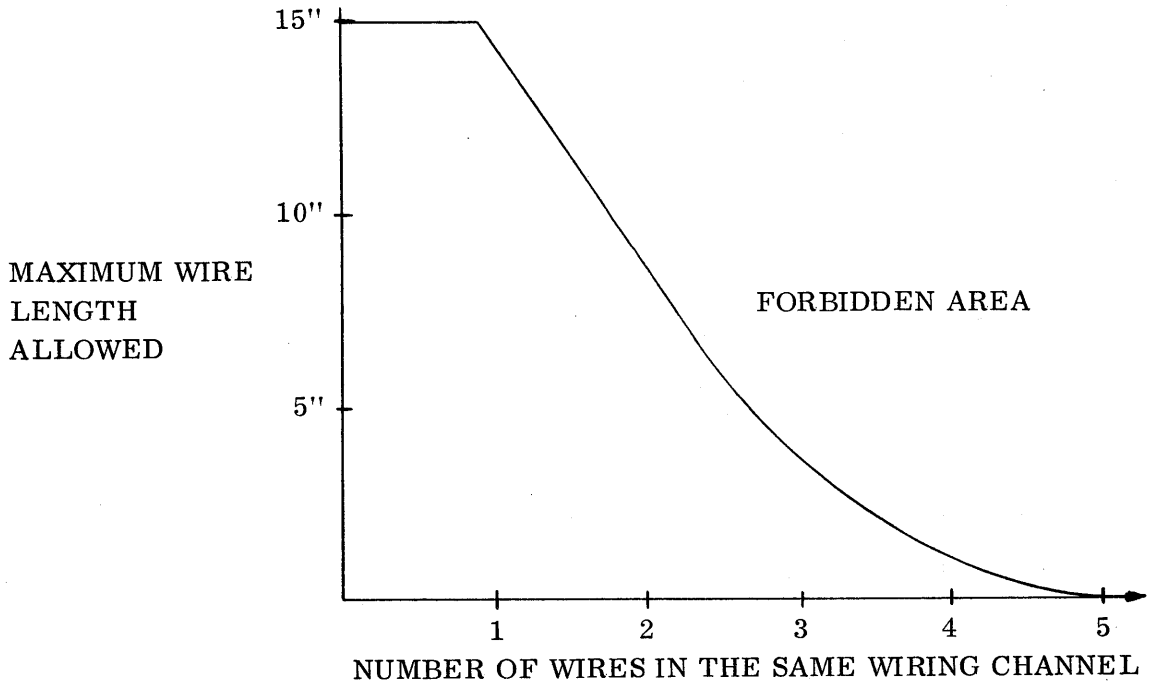
The total number of IC packages on the PC board should be proportional to the number of V_{CC} pins at the rate of 80 unit power per pin.*

*Unit Power = The average power of one 74 standard TTL gate which is approximately 10 mW at output low. The 74H family gate is equivalent to 2 unit power. The equivalent power for an MSI circuit can be found by dividing the current by a factor of 10.

V_{CC} decoupling capacitors (12 μf) are required for every 10 unit power and should be located less than 1-1/2 inches away from the chips to be decoupled. Decoupling capacitors are intended to eliminate current transient due to circuit change state. Power bus(ses) (bars or printed wire) will be provided for V_{CC} and decoupling capacitors.

BACK PANEL WIRING

The number of wires in each wiring channel* should follow the maximum length specification shown in the following diagram:



Twisted pair or coaxial cable (wire-wrap) can be used on the back panel for better noise rejection. The preferred impedance is above 80 ohms. At the receiving end, the cable should be properly terminated. Twisted pair should be driven differentially by a balanced output device. The stub length should be less than 2 inches.

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*The space between pins on the back panel where the wire passes through, either vertically or horizontally.

REFERENCES

Additional information pertaining to TTL logic design can be found in the following documents:

- CDC Specification 52338300, Design Guide for TTL Logic
- CDC Specification 52339100, Detail Characterization of TTL Logic Circuits

PRINTED WIRING BOARD DESIGN

CONFIGURATION

The physical dimensions of the MP type boards are 11.000 × 14.000 inches ±.015, with a thickness of .053 inches + .004 - .009. A board may be two sided or it may be a multi-layer board of three or four layers. (See Figures 11 and 12.)

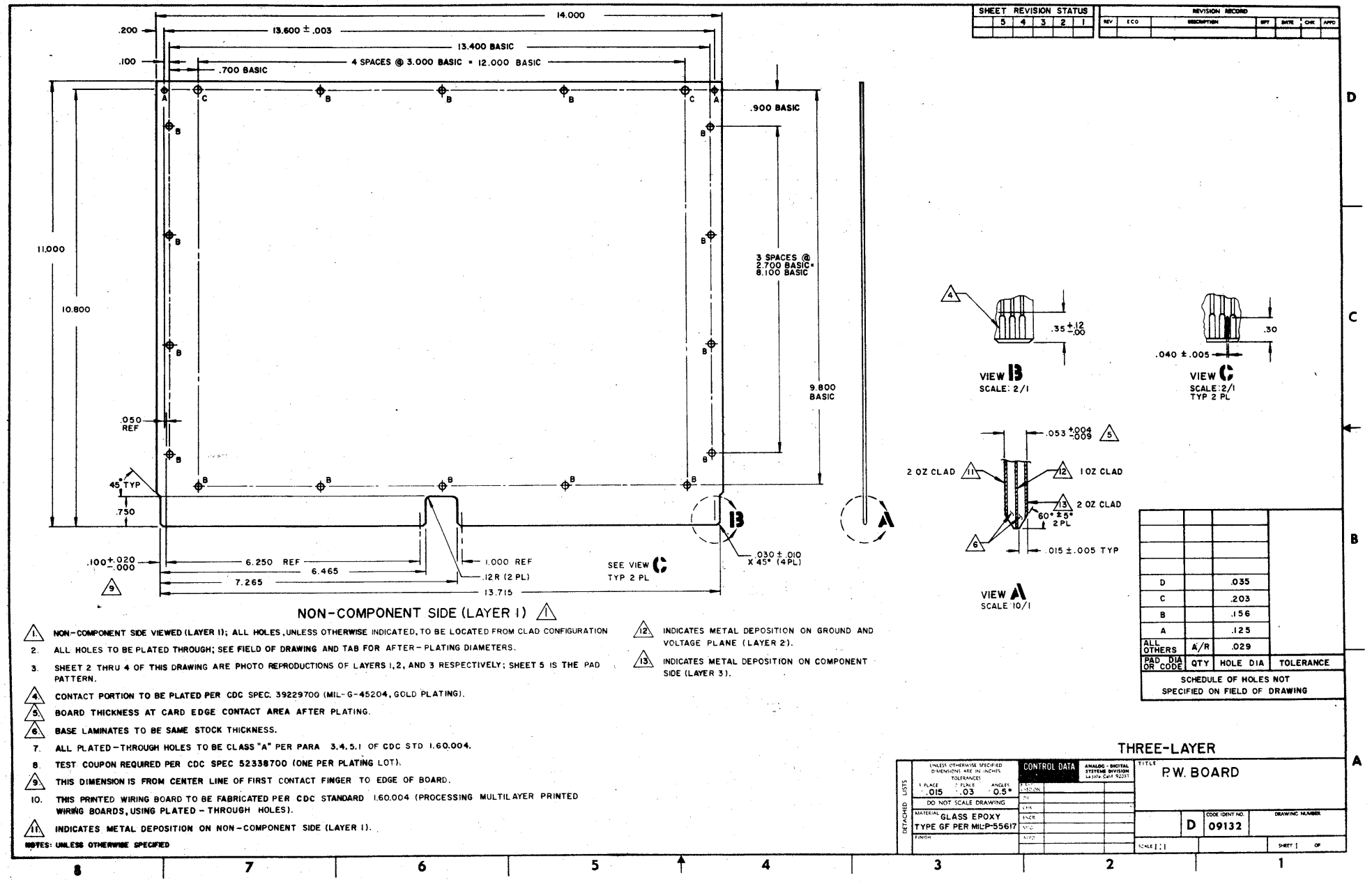
The dielectric insulator thickness between the two inner planes on a four-layer board is .006 inches +.003 -.000.

All boards have one or two keying slots .040 inches wide × .30 inches deep ±.005, in the positions indicated by Engineering, to prevent improper insertion.

All boards have two contact areas of 51 positions each on the component and the non-component sides of the board, for a total of 204 input/output contacts.

The maximum density of the board is 136 integrated circuits, laid out on a 17 × 8 matrix with 17 decoupling capacitors. This will allow one capacitor per file, or one capacitor for each group of eight ICs. This is the maximum limit and it will be reduced as additional decoupling capacitors, resistors, diodes, transistors, or special power requirements are added, as well as by the complexity of the logic.

Two types of board assemblies can be provided: with a frame all around the board for maximum rigidity, or with a board stiffener along the contact area of the board, plus externally mounted power busses. The second method is not recommended for high density boards since the bus bars minimize the efficient use of the board area.



NON-COMPONENT SIDE (LAYER 1)

1. NON-COMPONENT SIDE VIEWED (LAYER 1); ALL HOLES, UNLESS OTHERWISE INDICATED, TO BE LOCATED FROM CLAD CONFIGURATION
2. ALL HOLES TO BE PLATED THROUGH; SEE FIELD OF DRAWING AND TAB FOR AFTER-PLATING DIAMETERS.
3. SHEET 2 THRU 4 OF THIS DRAWING ARE PHOTO REPRODUCTIONS OF LAYERS 1, 2, AND 3 RESPECTIVELY; SHEET 5 IS THE PAD PATTERN.
4. CONTACT PORTION TO BE PLATED PER CDC SPEC. 39229700 (MIL-G-45204, GOLD PLATING).
5. BOARD THICKNESS AT CARD EDGE CONTACT AREA AFTER PLATING.
6. BASE LAMINATES TO BE SAME STOCK THICKNESS.
7. ALL PLATED-THROUGH HOLES TO BE CLASS "A" PER PARA 3.4.5.1 OF CDC STD 1.60.004.
8. TEST COUPON REQUIRED PER CDC SPEC 52338700 (ONE PER PLATING LOT).
9. THIS DIMENSION IS FROM CENTER LINE OF FIRST CONTACT FINGER TO EDGE OF BOARD.
10. THIS PRINTED WIRING BOARD TO BE FABRICATED PER CDC STANDARD 1.60.004 (PROCESSING MULTILAYER PRINTED WIRING BOARDS, USING PLATED-THROUGH HOLES).
11. INDICATES METAL DEPOSITION ON NON-COMPONENT SIDE (LAYER 1).
12. INDICATES METAL DEPOSITION ON GROUND AND VOLTAGE PLANE (LAYER 2).
13. INDICATES METAL DEPOSITION ON COMPONENT SIDE (LAYER 3).

NOTES: UNLESS OTHERWISE SPECIFIED

D		.035
C		.203
B		.156
A		.125
ALL OTHERS	A/R	.029
PAD DIA OR CODE	QTY	HOLE DIA

TOLERANCE

SCHEDULE OF HOLES NOT SPECIFIED ON FIELD OF DRAWING

THREE-LAYER

P.W. BOARD

MATERIAL GLASS EPOXY TYPE GF PER MIL-P-55617

FINISH

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES: 1 PLACE .015, 2 PLACE .03, ANGLES 0.5°

CONTROL DATA

ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037

DETACHED LISTS

D | CODE IDENT NO. 09132 | DRAWING NUMBER

SCALE [:] | SHEET [ ] OF

Figure 11. Three-layer PWB

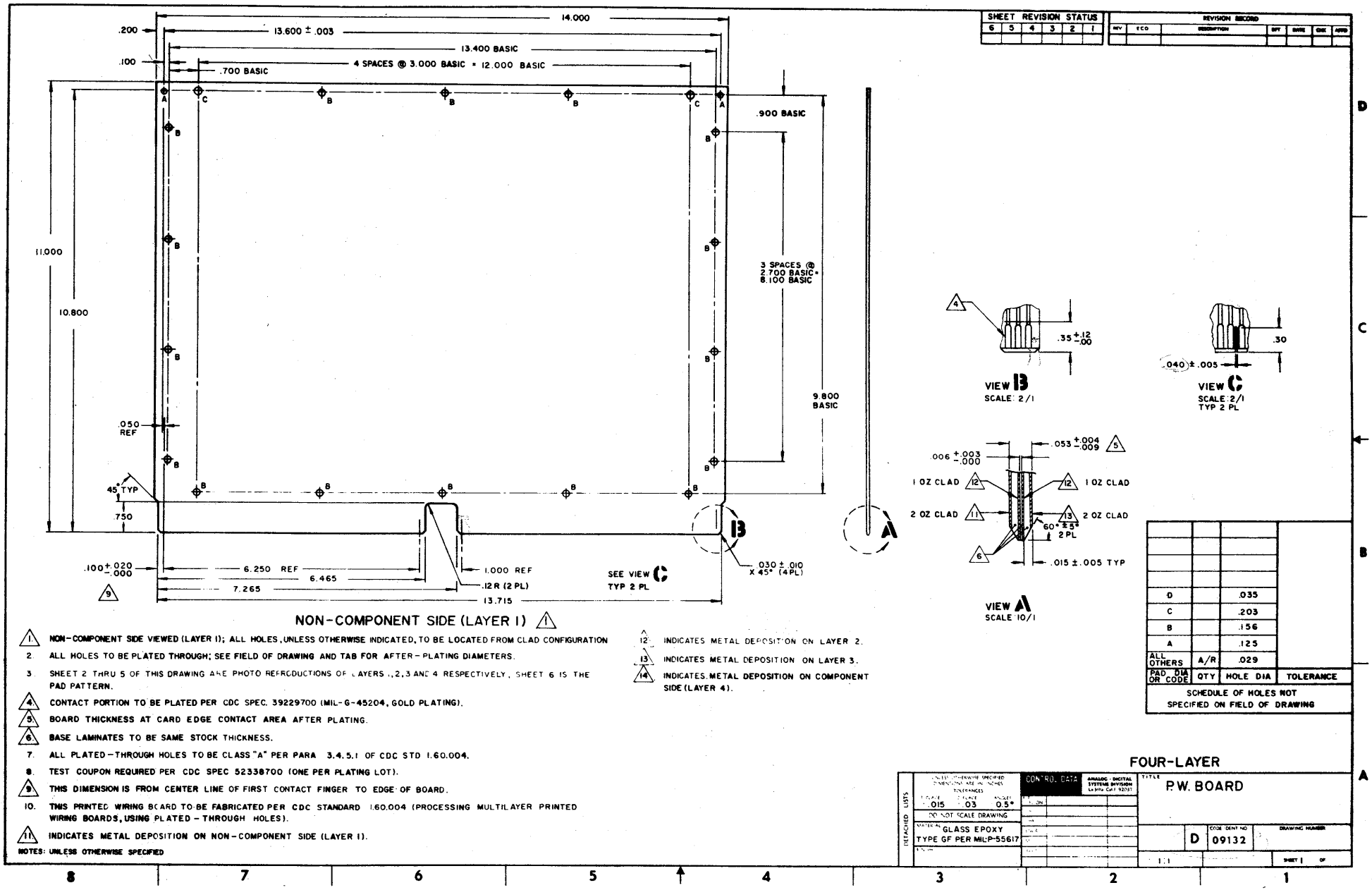


Figure 12. Four-layer PWB

If used, bus bars will be mounted on the component side of the board in the horizontal direction to allow maximum air flow. A minimum of two bus bars will be used.

PRINTED WIRING BOARD LAYOUT GUIDELINES

- Minimum signal conductor width is .015 inch.
- Minimum power conductor width is .050 inch.
- Minimum air gap between conductors is .015 inch.
- Minimum spacing between conductors and board edge is not less than .125 inch.
- Minimum spacing between conductors and non-functional holes is .062 inch.
- Dual in-line pads are of the elongated type, .055 × .075 inch, with a pad for pin #1 .060 inch square (see Figure 13).
- Feed-through pads may be .060 or .050 inch in diameter. No feed-throughs are located under an IC or any other component mounted flush on the board.
- A minimum of six feed-throughs with .093 inch pads and .043 diameter holes are used for transferring power or ground from one layer to another.
- Transistor pads are the "teardrop" type shown in Figure 14.
- Large solid circuit areas are stress-relieved.
- Layout and artwork is done on a 2/1 scale, using a master grid of .100 inch square on a 2/1 scale.
- All holes are located on the grid intersections. A tooling hole is provided and used as a datum for grid X and Y coordinates.
- All predominant conductors are horizontal to the connector edge on the component side, and perpendicular to the connector edge on the non-component side of the board.

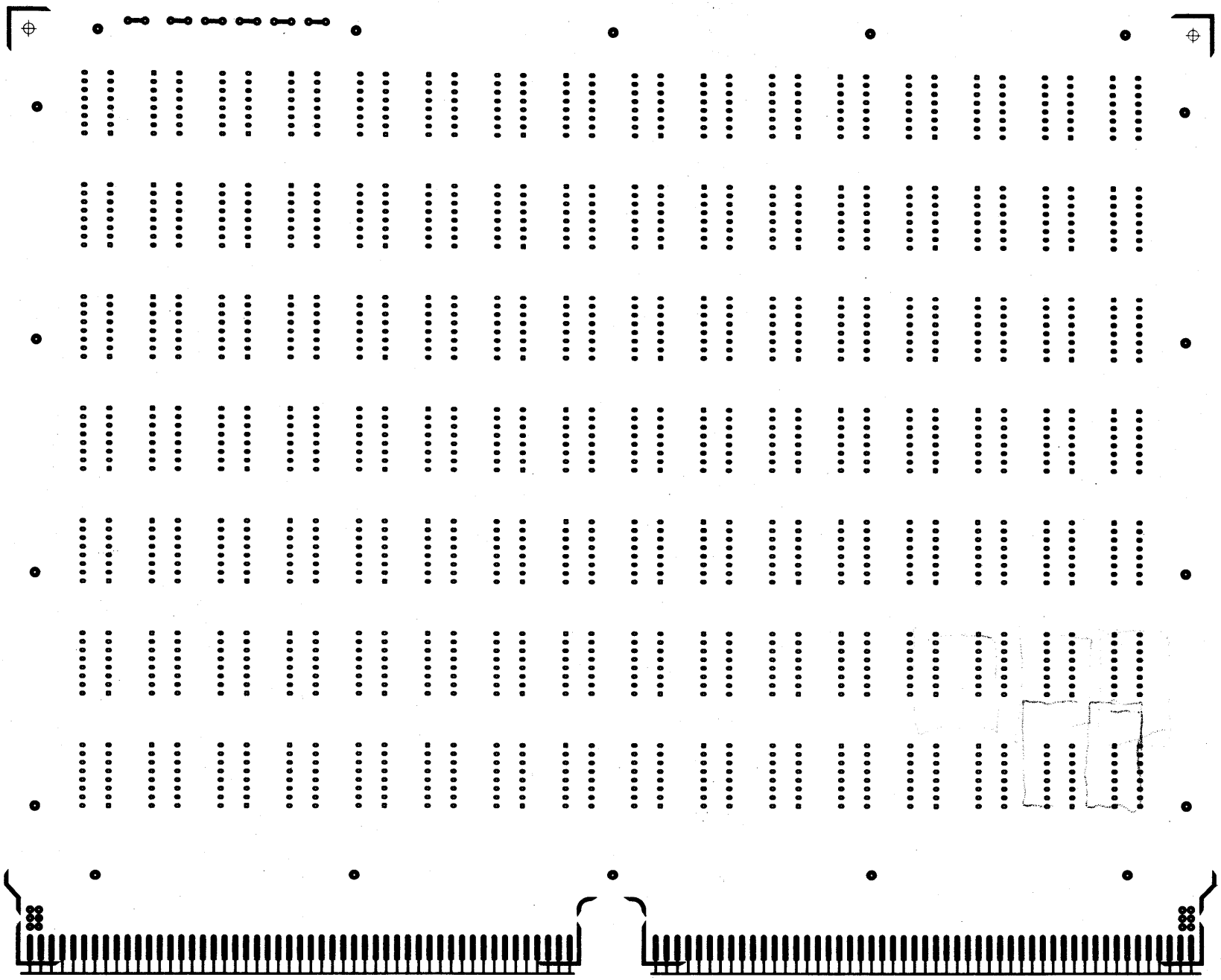
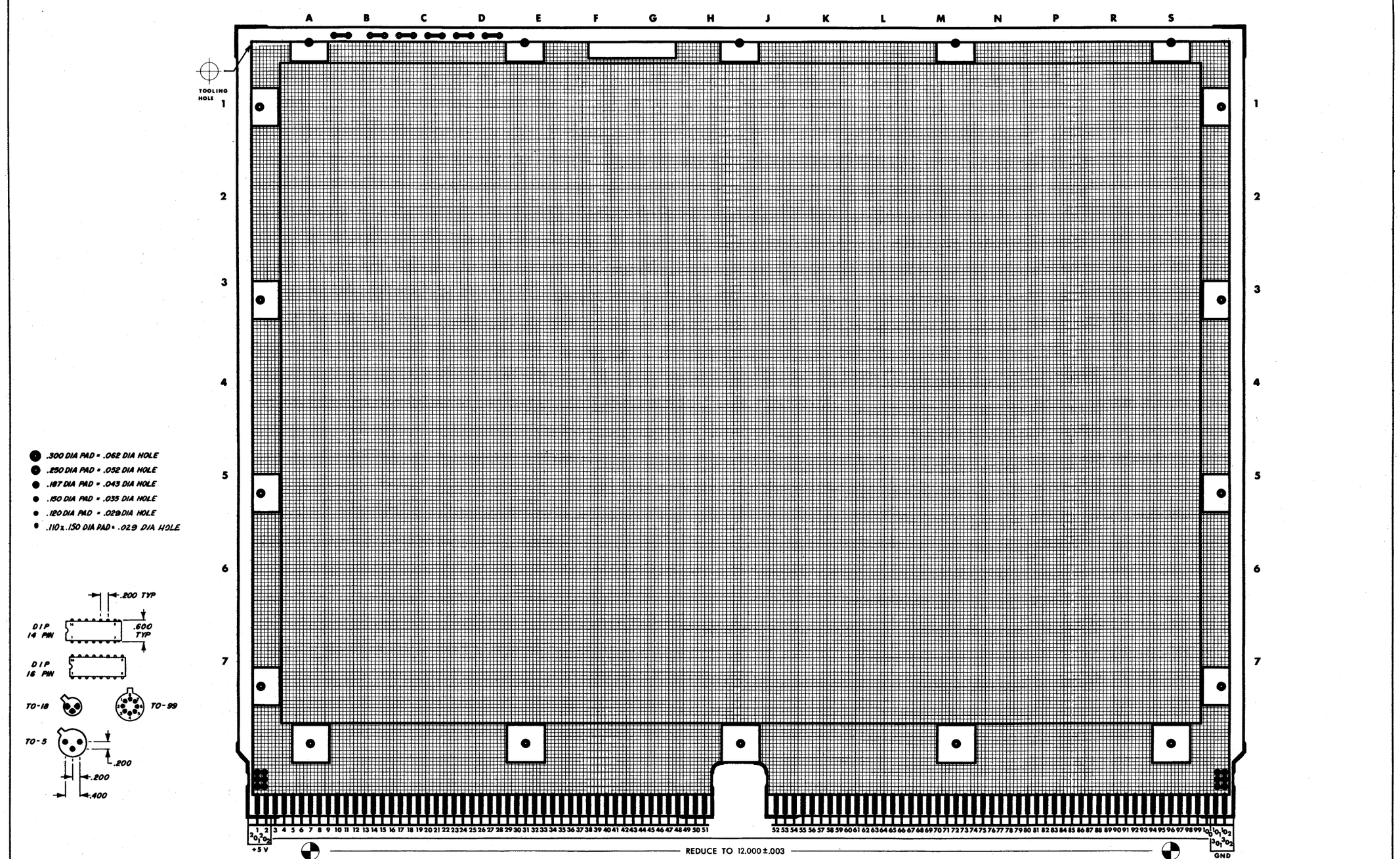


Figure 13. Pad Pattern



5. ALL DIMENSIONS ARE "LAYOUT" SIZE.
4. "AIR GAPS" .030 WIDE (MIN).
3. VOLTAGE & GND STRAPS .100 WIDE (MIN).
2. SIGNAL STRAPS .0 WIDE (MIN).
1. COMPONENT HEIGHT .312 (MAX).

NOTES: UNLESS OTHERWISE SPECIFIED

VIEWED FROM COMPONENT SIDE

LISTS DETACHED	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES 3 PLACE ± 2 PLACE ± ANGLES ±	CONTROL DATA SMALL COMPUTER DEVELOPMENT DIVISION La Jolla, CA 92037	TITLE
	DO NOT SCALE DRAWING	FIRST USED ON	
	MATERIAL	DR	
		CHK	
		ENGR	
	FINISH	MFG	
		APPD	
		F CODE IDENT NO. 09132	DRAWING NUMBER
		SCALE	SHEET OF

M-146-A M-146-C

Figure 14. Precision Grid Master

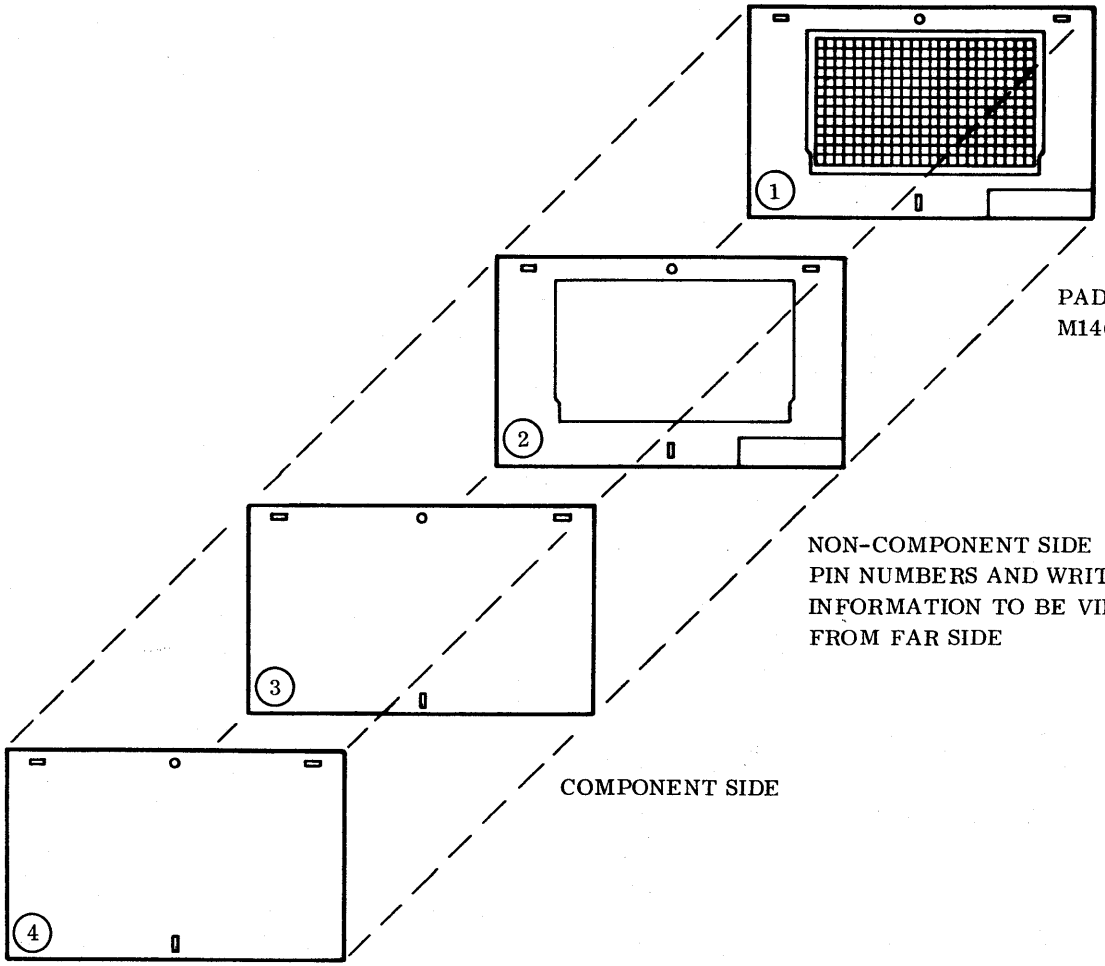
Holes

- Plated-through holes are used for all connections between layers.
- Tooling holes are .125 inch in diameter.
- All dual-in-line hole diameters are .029 inch.
- Other hole diameters are as follows:

Pad Diameter	Hole Diameter
.050 inch	.029 inch
.060 inch	.029 inch
.075 inch	.035 inch
.093 inch	.043 inch
.125 inch	.052 inch
.150 inch	.062 inch

Precision Pin System

- All MP boards can be laid out using the precision pin system and masters created at SCDD in La Jolla. See Figure 15.
- A precision grid master (see Figure 14) and a blank mylar are used for creating a planner or logic layout.
- A second mylar is used to create a "pad pattern" which contains every single pad required on the board (Figure 13).
- A third mylar is used to make the horizontal connections on the component side layer of the board.
- A fourth mylar is used to make the vertical connections on the non-component side layer of the board.
- For multilayer boards, an additional mylar is required for each layer.



NOTE:

1. TO OBTAIN NON-COMPONENT SIDE NEGATIVE, PHOTOGRAPH PAD PATTERN M146B TOGETHER WITH NON-COMPONENT SIDE.
2. TO OBTAIN COMPONENT SIDE NEGATIVE, PHOTOGRAPH PAD PATTERN M146B TOGETHER WITH COMPONENT SIDE MYLAR.

Figure 15. MP Precision Pin System

- To create 1/1 positives or negatives, each layer is imposed onto the "pad pattern" and photographed.

DOCUMENTATION

An MP board documentation package consists of the following:

a. A set of artworks

b. Drill information drawing

c. Assembly and parts list drawing

d. Logic diagrams

e. Specifications

f. Vendor package, which consists of a complete set of the 1/1 negatives required to manufacture the board.

ENGINEERING INPUTS REQUIRED

In addition to a complete up-to-date logic diagram, the following information is supplied by the design engineer:

a. Pin assignments

b. Electrical limitations

c. Possible areas with noise problems

d. Power requirements

e. Grounding requirements

f. Components selected

g. Filter capacitors needed

h. Any special shielding requirements

i. Amount of layers

j. Minimum dielectric insulator thickness for four-layer boards

k. Thickness of copper required

l. Solder mask requirements

m. Type of symbology to be used on logic diagrams

n. Keying slot locations

For additional information or assistance regarding the MP program, you may contact the following people at La Jolla:

Program Management	J. Rickert	Ext. 314
Engineering	R. Snyder	Ext. 304
Project Engineer	T. Heideman	Ext. 235
Drafting/PC Layout	B. F. Marshall	Ext. 216

COST

SCDD costs for a manually laid out PWB of the MP type (11×14 inches) is approximately $5K. This includes complete documentation and an assembled prototype.

Cost at NCR for a digitized PWB, including recycling of the artwork for design changes, is estimated to be $25K.

The costs from our vendors for the manufacturing of blank PWBs are as follows:

Qty.	Unit Price
1	$ 200
3	133
5	110
500	44

In addition, the following costs apply:

Drill tape	$ 100
Negatives	120
Routing Guide	60

APPENDIX A

The following components, listed by generic designator, are used in the MP program:

1488
1489A
7402
7407
7413
7437
7475
7485
7486
7489
7487
74125/8093
8123/74S257
8205
8214/74S253
9615
8831
9309
9318
9602
74150
74151A
74154/74S138
74155
74156
74157
74161/9316
74174
74175
74180
74191
74194
74H00
74H01
74H04
74H08
74H10
74H11
74H20
74H21
74H51
74H52
74H74
74S00
74S04
74S10
74S11
74S20
74S113
74S138
74S151A
74S175
74S181
74S182
74S200/5523A
75108A
75110
75450A
75154
93415
TR1602B/TMS6011
IM5610C
IM5623
74S85
74S258
93S62
82S09
Delay Line, EC^2, TDR 1084, 100 ns
9024
Transistor, 2N2905
Transistor, 2N2219A
R. Network, 220 ohms, R Pack
Delay Line, EC^2, TDR 1035, 30 ns
R. Network, 56 ohms, R Pack
R. Network, 1K, R Pack, 14 pin
R. Network, 510 ohms, R Pack
Crystal, 4.9152 MHz
R. Network, 56 ohms/5.1K