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OPC DESIEN SECTION


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| Device | Op Amps per Pkg | Supply Current per Amp （ $\mu \mathrm{A}$ ）max | Vos （mV）max | $\begin{aligned} & \mathrm{IB}_{\mathrm{B}} \\ & (\mathrm{pA}) \end{aligned}$ | Bandwidth （kHz） | Input Voltage Range $(\mathrm{V}+=5 \mathrm{~V}, \mathrm{~V}-=\text { GND })$ | Rail－to－Rail Output | Price ${ }^{\dagger}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MAX406 | 1 | 1.2 | 0.5 | ＜0．1 | 40 | GND to +3.9 V | Yes | \＄2．50 |
| MAX407 | 2 | 1.2 | 3 | $<0.1$ | 8 | GND to +3.8 V | Yes | \＄2．95 |
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- Communications ICs
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## "Build Things People Will Buy"

Looking out my window down at our building's parking lot, a pile driver continues its relentless pounding of a 60 -foot wooden piling into the ground for who-knows-what future construction, nearly bouncing me out of my chair at every impact. It's arresting in its simplicity - just pound the thing into the ground, and then go on to the next one. Designing electronic systems is a lot more complex, of course, but there's something appealing about a team carrying out a tightly focused job to produce something that clearly satisfies a need.

Success in the electronics industry might, but rarely does, stem from a sophisticated, unique philosophy of a company's mission. Most of the time, it results from more basic approaches: hard, steady teamwork turning out products that customers want. A recent article in the Harvard Business Review by Gerard H. Langeler, president of Mentor Graphics' Systems Group, drives this point home. In "The Vision Trap," Langeler presents an unusually candid review of the evolution of Mentor's philosophy, or "long-term vision," during the 1980s.

Langeler, one of Mentor's founders, notes that the company's vision early on was simple: "Build things that people will buy." However, as the company grew through the decade, this vision expanded to levels of greater and greater sophistication and abstraction. These concepts became increasingly difficult to translateinto specific marching orders for the engineering staff. Then, Langeler notes, Mentor's management came face-to-face with some unpleasant facts. The release of its 8.0 software was slipping, as was workers' morale, and layoffs and losses were in the offing.

It was time to get down to basics. Stronger scheduling discipline measures were imposed for 8.0 , with cutoff dates implemented to prevent perpetual refinement. The product was soon shipped.

Now, says Langeler, the company has come full circle in its thinking. When asked by an employee at a recent company meeting to elucidate the company's vision, he responded simply, "Our current short-, medium-, and long-term vision is to build things people will buy." This, he says, was greeted with immediate and lengthy applause.

There's something about this story that an engineer has to like. It seems to capture the essence of hard-nosed, real-world engineering: Forget the fancy management theories and just go ahead and build the products that


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## ormance of your entire system.

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| Model | Voltage Noise $\mathrm{nV} / \mathrm{VHz}$ @1 kHz typ | Current Noise $\mathrm{f} A / \sqrt{\mathrm{Hz}}$ <br> @1 kHz typ | $\begin{aligned} & \text { Vos } \\ & m V \\ & \max \end{aligned}$ | Supply Current mA typ | Input Bias Current max | $\begin{gathered} \text { SR } \\ V / \mu \mathrm{s} \\ \text { typ } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| AD829 | 2.0 | 1.5 | 0.5 | 5 | $7 \mu \mathrm{~A}$ | 230 |
| OP-27/OP-37 | 3.0 | 400 | . 025 | 3 | 40 nA | 2.8/17 |
| AD743/745 | 3.2 | 6.9 | 0.5 | 8 | 250 pA | 2.8/12.5 |
| OP-275 (dual) | 6 | 1500 | 1 | 4 | 350 nA | 22 |
| AD645 | 9 | 0.6 | 0.25 | 3 | 1.5 pA | 2.0 |
| AD712 <br> (dual) | 18 | 0.01 | 0.7 | 5 | 75 pA | 20 |
| AD548/648 <br> (dual) | 30 | 1.8 | 0.25/0.3 | . 34 | 10 pA | 1.8 |
| AD549 | 35 | 0.11 | 0.5 | . 60 | 60 fA | 3 |

impedance sources. The AD548 (single) and AD648 (dual) deliver low bias current ( 10 pA ), extremely low current noise ( $1.8 \mathrm{fA} / \sqrt{\mathrm{Hz}}$ ) and low power consumption at a highly attractive price. And the industry-standard OP-27 and OP-37 offer ultralow noise ( $3 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ at 1 kHz ) and precision dc performance.

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## TECHNOLOGY BRIEFING

## A Decade 0f SCSI

Anumber of major anniversaries seem to be springing up lately. ELECTRONIC DESIGN is celebrating its 40th anniversary, and the 10 -year anniversaries of the personal computer and the VMEbus have recently passed. This pattern continues with the Small Computer Systems Interface (SCSI), which also observes its 10th year. The goal of SCSI, developed by NCR Corp., Fort Collins, Colo., and Shugart Associates was to improve performance because the existing interfaces, such as RS232, IEEE-488, MIDI, Centronics, and others, were running out of steam.

SCSI is based on the Shugart Associates System Interface


RICHARD NASS COMPUTER SYSTEMS (SASI), which was introduced in an August 20,1981 cover article in ELECTRONIC DESIGN. SASI was comparable to SCSI electrically, but its command set was simpler than that of SCSI. In 1982,NCR worked with Shugart Associates to evolve SASI into SCSI by including differential drivers, a more generic interface, better software, and other features.

Before SCSI, adding a new peripheral to the host meant designing a dedicated hardware and software interface. By the time the host computer "learned" how to communicate with the new peripheral, more advanced peripherals were emerging. This trend held the host one generation behind the current peripheral technology. SCSI's standardization kept the host from learning a new way to communicate with each peripheral, thus reducing integration time. SCSI became an ANSI standard in June 1986.

SCSI was originally conceived to support multiple device types, including se-quential- and direct-access devices, printers, and processors. The proposal was extended to include write-once read-many (WORM) drives, CD-ROMs, mediachanger devices, scanners, optical-memory drives, and communication hardware. A maximum of eight devices in any mix of hosts and peripherals were permitted in the original specification. The bus contains ninebidirectional datalines plus parity, controlled by nine signals. Data is usually sent in an asynchronous mode, although synchronous operation is an option.

A SCSI controller must have intelligence, and should process one-byte messages (the bus logical interface) and multibyte command-descriptor blocks (the I/O logical interface). Most of the error recovery, data buffering, and other de-vice-specific tasks are handled by the peripheral controller, presenting a de-vice-independent interface to the host. A typical SCSI bus controller translates signals, performs speed matching, and orders bytes between the microprocessor and SCSI buses.

The original SCSI was replaced by the SCSI-II upgrade, which features more speed and increased bandwidth among other enhancements while maintaining backward compatibility with the original SCSI specification. To improve speed, the SCSI bus has options for wider data paths called "wide SCSI" and faster data-transferratescalled "fastSCSI."The wideSCSI busfeatures synchronous data transfers that are either 16 bits for $10 \mathrm{Mbits} / \mathrm{s}$ or 32 bits for $20 \mathrm{Mbits} / \mathrm{s}$. The fast SCSI bus offers synchronous data transfers that are 8 bits for $10 \mathrm{Mbits} / \mathrm{s}$.

NCR based its redundant-array-of-inexpensive-disks (RAID) technology on SCSI-II, introduced on ELECTRONIC DESIGN's March 14, 1991 cover. When combined with fast and wide SCSI controllers, the RAID systems offer higher I/O throughputs to keep up with the parade of faster microprocessors. Data is also protected against drive failures because data from one down drive can be recreated by the other drives within the array. RAID subsystems are being implemented in systems ranging from file servers to mainframes.

Work has just begun on SCSI-III. Some features that may appear in the next generation include a single 16 -bit wide SCSI cable, a serial SCSI protocol that can utilize fiber-optic cable, the ability to connect more than eight devices on the SCSI bus, and a more standardized logical interface.


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# dc to $3 \mathrm{CHz}^{\mathbf{S}} 1745$ lowpass, highpass, bandpass 

- less than 1 dB insertion loss $\bullet$ greater than 40 dB stopband rejection • surface-mount $\bullet$ BNC, Type N, SMA available $\bullet$ 5-section, 30dB/octave rolloff •VSWR less than 1.7 (typ) • rugged hermetically-sealed pin models • constant phase - meets MIL-STD-202 tests • over 100 off-the-shelf models • immediate delivery

Iow pass, Plug-in, dc to 1200 MHz



Price, (1-9 aty), all models: plug-in $\$ 19.95$, BNC $\$ 36.95$, SMA $\$ 38.95$, Type $N \$ 39.95$
NOTE: A: -933 and -1870 only with connectors, at additional $\$ 2$ above other connector models.
high pass, Plug-in, 27.5 to 2200 MHz

| Model No. | Stopband MHz |  | $\begin{gathered} \text { Passband } \\ \mathrm{MHz} \\ \text { loss } \\ <1 \mathrm{~dB} \\ \hline \end{gathered}$ | VSWR <br> Passband Typ. | Model No. | Stopband MHz |  | $\begin{gathered} \text { Passband } \\ \mathrm{MHz} \\ \text { loss } \\ <1 \mathrm{~dB} \\ \hline \end{gathered}$ | VSWR <br> Passband Typ. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\begin{aligned} & \text { loss } \\ & <40 \mathrm{~dB} \end{aligned}$ | $\begin{aligned} & \text { loss } \\ & <20 \mathrm{~dB} \end{aligned}$ |  |  |  | $\begin{aligned} & \text { loss } \\ & <40 \mathrm{~dB} \end{aligned}$ | $\begin{aligned} & \text { loss } \\ & <20 \mathrm{~dB} \end{aligned}$ |  |  |
| PHP-25 | DC-13 | 13-19 | 27.5-200 | 18:1 | PHP-400 | DC-210 | 210-290 | 395-1600 | 17.1 |
| PHP-50 | DC-20 | 20-26 | 41-200 | 1.5:1 | PHP-500 | DC-280 | 280-365 | 500-1600 | 1.8:1 |
| PHP-100 | DC-40 | 40-55 | 90-400 | 1.8:1 | PHP-600 | DC-350 | 350-440 | 600-1600 | 2.0:1 |
| PHP-150 | DC-70 | 70-95 | 133-600 | 1.8:1 | PHP-700 | DC-400 | 400-520 | 700-1800 | 1.6:1 |
| PHP-175 | DC-70 | 70-105 | 160-800 | 1.5:1 | PHP-800 | DC-445 | 445-570 | 780-2000 | 2.11 |
| PHP-200 | DC-90 | 90-116 | 185-800 | 1.6 .1 | PHP-900 | DC-520 | 520-660 | 910-2100 | 1.81 |
| PHP-250 | DC-100 | 100-150 | 225-1200 | 1.3:1 | PHP-1000 | DC-550 | 550-720 | 1000-2200 | 1.9:1 |
| PHP-300 | DC-145 | 145-170 | 290-1200 | 1.7:1 |  |  |  |  |  |

Price, (1-9 qty), all models: plug-in \$14.95, BNC \$36.95, SMA \$38.95, Type N $\$ 39.95$
bandpass, Elliptic Response. 10.7 to 70 MHz

|  | Center | Pa | 3 dB | Stopbands |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Model No. | Freq. <br> (MHz) | $\begin{aligned} & \text { I.L. } 1.5 \mathrm{~dB} \\ & \text { Max. } \\ & (\mathrm{MHz}) \\ & \hline \end{aligned}$ | Bandwidth Typ. (MHz) | $\begin{aligned} & 1 . \mathrm{L} \\ &> 20 \mathrm{~dB} \\ & \text { at } \mathrm{MHHz} \end{aligned}$ | $\begin{aligned} & \mathrm{IL} \\ &> 35 \mathrm{~dB} \\ & \text { at } \mathrm{MHz} \end{aligned}$ |
| PBP-10.7 | 10.7 | 9.6-11.5 | 8.9-12.7 | 7.5 \& 15 | 0.6 \& 50-1000 |
| PBP-21.4 | 21.4 | 19.2-23.6 | 17.9-25.3 | 15.5 \& 29 | 3.0 \& 80-1000 |
| PBP-30 | 30.0 | 27.0-33.0 | 25-35 | 22 \& 40 | 3.2 \& 99-1000 |
| PBP-60 | 60.0 | 55.0-67.0 | 49.5-70.5 | 44 \& 79 | 4.6 \& 190-1000 |
| PBP-70 | 70.0 | 63.0-77.0 | 68.0-82.0 | 51 \& 94 | 6.0 \& 193-1000 |

Price, (1-9 qty), all models: plug-in $\$ 18.95$
BNC \$40.95, SMA \$42.95, Type N $\$ 43.95$

Constant Impedance,
21.4 to 70 MHz

| Model No. | Center Freq. <br> MHz | $\begin{gathered} \text { Passband } \\ \mathrm{MHz} \\ \text { loss } \\ <1 \mathrm{~dB} \\ \hline \end{gathered}$ | Stopband loss <br> $>20 \mathrm{~dB}$ <br> at MHz | VSWR $1.3: 1$ Total Band MHz |
| :---: | :---: | :---: | :---: | :---: |
| PIF-21.4 | 21 | 18-2 | 1.3 \& 150 | DC-220 |
| IF-30 | 30 | 25-35 | 1.9 \& 210 | D-330 |
| IF-40 | 52 | 35-49 | 2.6 \& 300 | DC-400 |
| PIF-50 | 50 | 41-58 | 3.1 \& 350 | DC-440 |
| F-60 | 60 | 50-70 | 3.8 \& 400 | DC-500 |
| -70 | 70 | 58-82 | 4.4 \& 490 | DC-550 |
| Price, (1-9 qty), all models: plug-in $\$ 14.95$, BNC \$36.95, SMA \$38.95, Type N \$39.95 |  |  |  |  |
|  |  |  |  |  |

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Yoar order is shiped vo one of 2 gi Keys 43 standard deliveg options. Next day delivery would fypicaly pace this orde ing your han ds the nex morning? Cyrix Corp., Richardson, Texas, surprised the industry by releasing a chip Fits 386SX Pinout that implements the 80486 instruction set, yet plugs into sockets intended for the 386SX. Even though it has the same 100-lead plastic quad-sided flat package pinout of the 386SX, the chip also offers superset functions controlled by several pins that were no-connects on the 386 SX . With a 1 -kbyte on-chip merged-instruction and data cache, the fully static CMOS 486SLC can access data two clock periods faster than a zero-wait-state external 16 -bit bus access. The words are re-merged in the cache, forming 32 -bit words for transfers over the chip's internal data paths to the five-stage pipelined execution unit. The five overlapped stages permit successive instruction overlap to minimize instruction cycle times. By combining the cache and pipeline, as well as some single-cycle instructions, the chip can execute software up to 2.4 times faster than a 386 SX or 386 SL , and 1.7 times faster than IBM's cache-based 386SLC (if the data or instructions are in the cache). Adding a 16 -bit integer multiplier to the CPU's circuitry allows the CPU to perform many graphics- or DSP-related computations in less then one-third the number of cycles required by the 80486 CPU .
The 486SLC CPU will come in $3-$ and $5-\mathrm{V}$ versions. The $3-\mathrm{V}$ units are ideal for portable systems. With the clock stopped, the chip consumes a mere $100 \mu \mathrm{~A}$; when running at 20 MHz , the power is just 600 mW . Suspend/Resume instructions permit easy chip stoppage, dropping power to the microwatt range, even when running programs like Microsoft Windows. Contact Jim Chapman at (214) 234-8387. DB

## Fiber-Optic System

By using an optical power amplifier from Philips, Australia's Telecom PTT was able to send 2.5 -Gbit/s signals over a fiber-optic route of more than 200 km (about 120 miles) without the need for an intermediate amplifier. This record distance for a repeater-less link, Philips says, is four times the previous record of 50 km ( 30 miles). The Australian tests also showed that attenuation is the only factor limiting the potential distance that can be bridged using a fiber-optic cable. The $1550-\mathrm{nm}$ optical power amplifier, the result of a cooperative effort between the Philips Development Labs in Nuremberg, Germany, and the Philips Research Labs in Eindhoven, the Netherlands, has an optical pump laser as its active optical component. It makes available a transmission signal of +12 dBm (about 14 mW ). The SDH (synchronous digital hierarchy) transmission system uses a monomode glass fiber with an optical dispersion of $1300 \mathrm{~nm} . J G$

## CVD Grows BaTi0 ${ }_{3}$ Film 0n Semiconductors

Advanced Technology Materials Inc., Danbury, Conn., has been awarded a contract by the U.S. Defense Dept.'s Strategic Defense Initiative Office (SDIO) to develop chemical-vapor-deposition (CVD) techniques for fabricating piezoelectric barium titanate $\left(\mathrm{BaTiO}_{3}\right)$ thin films. The ability to grow such thin films, as well as thin films of other advanced dielectric materials (diamond, silicon carbide), on a semiconductor substrate is critical for the commercialization and high-volume production of nextgeneration ( 256 -Mbyte) DRAMs. $\mathrm{BaTiO}_{3}$ films will be used to make devices for high-precision and low-intensity lasers, for CD-ROM and medical applications. When combined with its nonlinear optical properties, $\mathrm{BaTiO}_{3}$ can accelerate the development of high-speed optical computers by allowing integrated optical phase modulators, switches, and couplers to be built. Call Gene Banucci at (203) 794-1100. FG

Sub-2-IN. Disk Drives Pack Up T0 85 MbyTes

A trio of 1.8-in. disk-drive families from MiniStor Peripherals Corp., San Jose, Calif.; Aura Associates, Saratoga, Calif.; and NEC Corp., Tokyo, Japan, offer storage capacities ranging from 32 to 85 Mbytes. The drives aim at portablecomputer and other battery-powered systems. MiniStor drives with operating and non-operating shock resistances of 20 Gs and 200 Gs , respectively, were designed to withstand high shock. With a shock sensor circuit, the drive can sense jarring movements during write commands, allowing the drive to take data-protection measures. Other features include a ruggedized spindle motor that provides high durability to shock, and a positive mechanical actuator lock that keeps the heads secure when they're parked. MiniStor's drives come in 32- or 64Mbyte options and in two versions. One version has IDE interfaces for embedded applications, and the other includes the PCMCIA 68-pin memory-card connector, suiting it for removable applications. A 256 -kbyte buffer helps eliminate unnecessary disk spin-ups by holding large chunks of data in temporary storage.
Aura Associates together with NEC designed a pair of 1.8 -in. drives that employ 32 -kbyte buffers, but offer 42.6 or 85.6 Mbytes of storage-about $33 \%$ more than the MiniStor drives. Access time is about 19 ms (just slightly slower than MiniStor) and the data-transfer rate is 4.5

## Test Results

$\begin{array}{lllllll}\mathbf{R} & \mathbf{E} & \mathbf{A} & \mathbf{L} & \mathbf{I} & \mathbf{T} & \mathbf{Y}\end{array}$
go
$\begin{array}{lllllll}D & \mathbf{R} & \mathbf{I} & \mathbf{V} & \mathbf{I} & \mathbf{N} & \mathbf{G}\end{array}$
$\begin{array}{llllll}\text { V } & \text { I } & \text { S } & \text { I } & \text { O } & \text { N }\end{array}$

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Mbytes/s over an IDE interface. The first versions will consume just 880 or 960 mW in their idle modes (platters spinning but no reads or writes). Read and write accesses increase power consumption to 2 to 3 W . Both Aura and NEC will offer nearly identical drives. However, Aura would like to also embed portions of its drive technology into other companies' systems. Contact Jim Miller at MiniStor, (408) 943-0165; and John Scott at Aura (408) 252-2872. DB

# Single Chip Compresses Data Locally 

 By placing lossless data compression on the motherboard through a local-bus interface to the CPU, the 9706 chip can perform compression without any negative impact on system performance. The device, a local-bus interface version of a data-compression chip from Stac Electronics Inc., Carlsbad, Calif., handles data transfers at rates exceeding $30 \mathrm{Mbytes} / \mathrm{s}$. All that's needed to incorporate it on PC motherboards are two 32 -kbyte static RAMs to hold the coding tables. Average data throughputs during compression of $2.5 \mathrm{Mbytes} / \mathrm{s}$, and $6 \mathrm{Mbytes} / \mathrm{s}$ during decompression, enable the IC to operate transparently to the user. The chip also contains a special sleep mode that drops oper-ating-current consumption from about 100 mA to just 0.3 mA when idling. Thus, the chip becomes an attractive option for portable PC motherboards, giving the system manufacturer a wider range of features to offer. Samples of the chip are immediately available and sell for $\$ 19.90$ each in lots of 50,000 . Contact Robert Lutz at (619) 431-7474. DB
## Consortium Backs PA-RISC ARCHITECTURE

Hewlett-Packard's Precision-Architecture RISC (PA-RISC) technology has gained worldwide acceptance since its inception. So much so that a consortium, the Precision RISC Organization (PRO), is being formed to back the architecture. The first high-end system to incorporate PA-RISC came in September 1990, with mid-range systems arriving a few months later. Then HP announced its 9000 Series 700 family of desktop workstations, which offers 76 MIPS for under $\$ 21,000$. PRO will establish a set of PA-RISC-related standards, including an application programming interface (API) and an application binary interface (ABI). The association will supply compliance verification and certification services, and will license a trademark to products that comply with these standards. PRO has developed a list of standard APIs that are supported by HP-UX, HP's version of Unix, as well as APIs that the organization expects will be supported by the OSF's operating system, OSF/1. The API supplies a common source-code interface, improving application portability from non-PA-RISC architectures. The initial members of PRO include Convex, HP, Hitachi, Hughes, Mitsubishi Electric, Oki, Prime, Sequoia, and Yokogawa Electric. For more information, call PRO at (408) 447-4249. $R N$

By lowering the sampling rate of its nonvolatile memory chip by a factor of 0.8, Information Storage Devices, San Jose, Calif., increased the device's EEPROM FINDS A H0ME storage time from 16 to 20 seconds. ISD introduced the $64-$ mil $^{2}$ nonvolatile analog memory, which provides better-than-telephone quality audio, just over a year ago (ELectronic design, Jan. 31, 1991, p. 39). By offering 20 seconds of memory for under $\$ 6$ in high volume, it becomes economically viable in mass-marketed telephone-answering ma-chines-those that sell to the consumer for under $\$ 100$. It will thus replace the tape recorder, which usually provides the owner's outgoing message. The 20 -second version of the chip is called the ISD520 TAD (tapeless-answering device). Sanyo will design a line of machines around the IC as well as market the chip in Japan. ISD's goal is a one-minute chip within a year, and ultimately an IC to store at least 30 minutes of speech. For additional information, call Steve Stephansen at (408) 428-1400. FG To accelerate cooperative technology development between the Department of Energy (DOE) and the computer industry, three research agreements, called CRADAs (cooperative research and development agreements), were To Aid DOE RESEARCH reached. The participating companies are Cray Research Inc., Mendota Heights, Minn., and the Los Alamos National Laboratory, Los Alamos, Calif. The first CRADA calls for the development of a more accurate oceanic-atmospheric (whole-earth) model to study global climate change. The DOE has a unique expertise in computer analysis of complex phenomena, such as large-scale global modeling. The second CRADA aims to develop advanced software to simulate electromagnetic-wave effects in ultra-high-speed electronic devices. That will reduce the cost of designing and developing advanced ICs. The third CRADA calls for the partners to collaborate on improving their capabilities in computational chemistry to support studies on the dynamics of large molecules. $R N$


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MCL NO. NSN
TMO2-1 5950-01-183-6414 TMO2.5-6 5950-01-215-4038 TMO2.5-6T 5950-01-215-8697 TMO3-1T 5950-01-168-7512 TMO4-1 5950-01-067-1012 TMO4-2 5950-01-091-3553 TMO4-6 5950-01-132-8102 TMO5-1T 5950-01-183-0779 TMO9-1 5950-01-141-0174 TMO16-1 5950-01-138-4593


TH, TT

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## Improved Spectrogram Algorithm

 B0osts Throughput, Increases ResolutionAnew spectrogram, based on the Gabor transform, overcomes the limitations of spectrograms based on the short-time fast-Fourier transform (STFT). Developed by National Instruments Inc., Austin, Texas, the spectrogram can perform calculations four to six times faster than a sliding FFT. It can also deliver four to eight times better resolution. In traditional frequency analysis used for such applications as speech, sonar, and vibration analysis, information concerning the time at which a sound occurs isn't available. Consequently, joint time-frequency analysis (JTFA) techniques must be used to view the time and frequency information simultaneously.
The STFT spectrogram is the most-commonly used approach to view information when performing JTFA. For each slice of windowed data, the frequency spectrum is computed with FFTs. The time index of the frequency information is assumed to be in the middle of each slice of windowed data. A complete 3D spectrogram can then be established by stepping the window to the right in some regular time interval and recomputing the spectrum.
However, STFT spectrograms do have limitations. For instance, the choice of window type and length can distort the outputspectrum. A wide window gives good resolution in the frequency domain but poor resolution in the time domain. Conversely, a nar-
row window gives good time-domain resolution but poor frequency-domain resolution. Furthermore, the STFT requires a considerable set of computational resources-the FFT must be calculated at each point in the input waveform to produce a complete spectrogram. Most STFT systems,

Fourier transform, the Gabor spectrogram avoids the limitations of the STFT spectrogram (Dennis Gabor, the Hungarian-born British physicist, first postulated the transform in an article "Theory of Communication" published in the Journal of the IEE in London in Nov., 1946). The combination of the Gabor

The Gabor transform is defined as:

$$
\begin{aligned}
& s(i)=\sum_{m=0}^{\infty} \sum_{n=0}^{N-1} C_{m, n} h_{m, n}(i) \\
& C_{m, n}=\sum_{i=0}^{\infty} s(i) \gamma_{m, n}^{*}{ }^{(i)} \\
& h_{m, n}(i)=h(i-m \Delta M) W_{L}^{n \Delta N i}, \gamma_{m, n}(i)=\gamma(i-m \Delta M) W_{L}^{n \Delta N i} \\
& \text { where: } \quad \mathrm{s}(\mathrm{i}) \text { is the discrete time-domain signal, } \\
& \mathrm{C}_{\mathrm{m}, \mathrm{n}} \text { is a Gabor coefficient, } \\
& \mathrm{h}_{\mathrm{m}, \mathrm{n}} \mathrm{i}^{(\mathrm{i})} \text { is the basis Gaussian function, } \\
& \gamma_{m, n}(\mathrm{i}) \text { is called the biorthogonal auxiliary function, } \\
& \Delta \mathrm{M}, \Delta \mathrm{~N} \text { are sampling intervals in the time and fre- } \\
& \text { quency domain. }
\end{aligned}
$$

though, use only about half their data points to maintain an acceptable throughputlevel.

Good joint time-frequency representation is difficult to achieve with STFT. When looking at a spectrogram, the sidelobe leakage from the FFT results in a smearing of the STFT spectrogram. That makes it difficult to detect individual formants. In contrast, the Gabor spectrogram is optimized for both time and frequency resolution. The resulting intensity plot shows very distinct transitions from one sound to another.
By employing a Gabor transform rather then a the Gaussian function is
known. Therefore, many computations can be done in advance and placed in a lookup table for use in the future.

The heart of the Gabor spectrogram is the discrete Gabor transform, which is computed using two specific equations (see the figure). In the calculations, it's important to obtain unique Gabor transform pairs. That's accomplished by selecting gamma(i) similar in shape to h(i). Gam$\mathrm{ma}(\mathrm{i})$ is a biorthogonal auxiliary function; $h(i)$ is the basis Gaussian function.

Computing the Gabor coefficients is very efficient because only a fraction of the number of coefficients required by the STFT are needed to accurately represent the original signal. A six-fold throughput improvement can be attained with the Gabor transform versus the STFT for the same data set. The Gabor spectrogramalso achieves a better signal-to-noise ratio in the output intensity plot. The higher SNR is obtained because the Gabor coefficients better reflect the local behavior of a signal, resulting in a higher signalenergy concentration in the joint time-frequency domain.

National Instruments has incorporated the Gabor transform as a virtual instrument under its LabView graphical programming system for data acquisition and analysis. When coupled with a dataacquisition board, the system allows users to transform signals into Gabor spectrograms and display the signals as a 2D intensity plot of time-frequency data.

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# FDDI Moves To The DeskTop <br> On Twisted-Pair Lines 

Although the 100 Mbit/s data rate and the $2.5 \times 10^{-10}$ bit-error rate of the FDDI (Fiber Distributed Data Inter face) are desirable for networking desktop computers and peripherals, the high cost of adapter cards is a major stumbling block. Where Ethernet adapter cards are available for under $\$ 200$, the $\$ 1500$ price tag for an FDDI card is prohibitive for most applications. A large part of this cost comes from the optoelectronic transceiver that connects networked terminals to fiber-optic cables. Another problem stems from present standards that call for fiber-optic cable to be routed from the FDDI backbone to the desktop-a costly outlay for buildings already wired for Ethernet or Token Ring networks.
These problems can be solved when the FDDI standard, which currently specifies only fiber-optic cable, is expanded to include twisted-pair copper wire as the transmission medium. Bringing twistedpair wire to FDDI cuts the cost of adapter cards by allowing the transceiver to be made with standard silicon processes. This reduces transceiver cost to about $\$ 200$. Another benefit is that twisted-pair copper wiring for network connections is already widely installed. However, the transition from fiber to copper wiring reintroduces the problems that caused the industry to select fiber over copper for a 100 -Mbit/s network in the first place: copper's high
attenuation, EMI and RFI noise-generation and susceptibility, and its low sig-nal-to-noise ratio
Searching for a solution to these objections, the ANSI X3T9.5 TP-PMD working group has looked at three types of twistedpair wiring. Shielded twist-ed-pair (STP) wiring is a two-pair, $150-\Omega$ cable consisting of individually shielded pairs contained within a shielded outer jacket. Referred to as IBM Type 1, the wire has a specific number of twists per foot and is used in tokenring networks. Datagrade, unshielded twisted pair (DTP) has tight tolerances on crosstalk, attenuation, and impedance characteristics. Referred to as IBM Type 3 or AT\&T Category 5, DTP is often used for 10Base-T Ethernet wiring. Distributed inside wire (DIW) is a voicegrade, unshielded twistedpair cable commonly used for telephone installations. Also referred to as AT\&T Category 3, this cable has no guaranteed number of twists per foot and thus no accurately predicted crosstalk, attenuation, and impedance characteristics.

It's easier to meet FCC requirements for electromagnetic interference by using STP. But users generally prefer using the same copper FDDI adapter card with data- or voicegrade unshielded-twistedpair cable at distances up to 100 meters. Since implementing new silicon for FDDI DIW could take up to three years, the standards committees have considered using separate
standards for data-grade and voice-grade cabling. However, new encoding schemes under evaluation may this solve the problem.

The primary objective of these schemes is to lower the frequency of the transmitted signal without reducing data rates. This would satisfy the data-rate requirements of other parts of the FDDI network while complying with FCC EMI and RFI requirements. The encoding scheme specified by FDDI for fiber transmission is NRZI (nonreturn to zero, inverted), which uses a two-level (logic high and low) waveform to reduce the data-flow frequency from 125 MHz to 62.5 MHz . To provide noise immunity and meet FCC copper requirements, the X3T9.5 working group is evaluating two proposals for modified NRZI encoding.

The first proposal comes from Crescendo Communications, Sunnyvale, Calif., and is co-sponsored by AT\&T, British Telecom, Fibronics International, Hewlett-Packard Co., and Ungermann-Bass Inc. Called MLT-3, this scheme uses a scrambled, threelevel NRZI-like waveform with three voltage levels. At the receiver end, the voltage difference be-
tween high and low logic levels is 110 mV . This type of coding requires dynamic adaptive equalization to account for different cable lengths. Post-compensation is employed at the receiver end to boost the sig-nal-to-noise ratio.

The second proposal from National Semiconductor, Santa Clara, Calif., and Cabletron Systems Inc., Rochester, N.H., uses a pre-compensated twolevel NRZI signal. Called 100Base-T by its proponents, this encoding scheme provides a $180-\mathrm{mV}$ step voltage at the receiver end. Like MLT-3, it requires a scrambling circuit for DTP cable, but doesn't need adaptive equalization. The performances of both approaches are being tested by Hewlett-Packard's communications laboratory in Austin, Texas. Even if one system exhibits a slight advantage over the other, the ultimate choice will hinge on the silicon cost and the cost of system implementation.

These and other FDDIrelated issues will be examined in detail at this year's Silicon Valley Networking Conference, to be held at the Santa Clara Convention Center, Santa Clara, Calif., April 27-29.

MILT LEONARD

## Deep-Etch Lithography Yields 0.5 Mm Diameter Motors

In from the believe it or not department: An electric motor so small that it takes a microscope to recognize its details.

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chanics, the emerging technology for fabricating inexpensive structural elements with dimensions in the millimeter to micrometer range.
The electrostatic stepping motor, resulting from work at the Institute for


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CIRCLE 258 FOR U.S. RESPONSE

## TECHNOLOGY ADVANCES

Microstructure Technology in Karlsruhe, Germany, has a rotor whose diameter is less than 0.5 mm (see the photo). Surrounded by six stator segments, the $100-$ $\mu \mathrm{m}$-high rotor turns on an axis with a radius of about $120 \mu \mathrm{~m}$. The motor is made of galvanized nickel.

The institute, which is part of the Karlsruhebased Nuclear Research Center, has readied working samples of its micromotor. Using voltages in the order of 100 V , its stator segments produce the alternating field needed to turn the rotor. The stator's and rotor's adjacent areas are toothed to make the electrostatic attraction between them, and hence the motor's driving force, as high as possible. At its present state of development, the motor turns at 50 revolutions/s. Some samples have reached 80 revolutions/s.

Similar micromotors have also been developed elsewhere, at U.S. universities, for example. But these are made of polysilicon and are relatively flat. The Karlsruhe motor, by contrast, can be several hundred micrometers high, and that makes for greater forces.

The institute's process for fabricating arbitrarilyshaped 3D microstructures, such as the stepping motor, is based on deepetch synchrotron lithography, electroforming, and plastic molding. The LIGA process (its name derives from the German words for lithography, electroforming and molding) allows microstructures of any lateral shape to be made with structural heights of several hundred micrometers, lateral di-
mensions down to $1 \mu \mathrm{~m}$, and with sub-micrometer accuracy over the structure's total height.

Moreover, different materials like plastics, metals,
the LIGA process steps. A resist layer, several hundred micrometers high, is polymerized directly onto the substrate and exposed to synchrotron radiation

and ceramics, or a combination of these, can be used. The LIGA process can be applied to various technologies, including micromechanics, microoptics, and integrated optics, as well as sensors and actuators. The Karlsruhe institute has extended its process to allow free-moving oscillating or rotating microstructures to be made.
In preparing a substrate for the LIGA process, a thin silver layer for the electrical contacts is deposited onto the insulating substrate, which may be a ceramic or silicon wafer. Next, a titanium layer, a few $\mu \mathrm{m}$ thick, is sputtered onto the substrate.

This titanium layer serves as the sacrificial layer. It guarantees good adhesion of the X-ray resist to the substrate and constitutes a plating base for the electrodeposited structures. The titanium layer is patterned by conventional photolithography and wet etching.
The substrate so prepared is then subjected to
through an X-ray mask that's precisely adjusted to the patterned titanium sacrificial layer. This adjustment positions the movable parts of the microstructure on top of the titanium layer. The fixed parts are placed on the substrate's metallized areas.

The irradiated resist is subsequently removed and a complementary structure is built up by electrodepositing a metal. After stripping the resist, the titanium sacrificial layer is selectively etched against the overlying and underlying metals using hydrofluoric acid. After this etching process, certain parts of the microstructure remain firmly attached to the substrate while other parts can move freely.

According to the institute, the micromotor samples in their present form serve for demonstration purposes; they would hardpressed to find any applications. But once modified and perfected, the micromotor could be used in measurement and control equipment; robots; and medical electronic systems for purposes of switching, for operating valves, and for adjusting miniature micropumps.

JOHNGOSCH

## Simple Serial Bus Eases PC-Peripherals Interconnect

Although most desktop and portable PCcompatible computers pack multiple I/O ports and expansion-card slots, those ports and slots often require long bulky cables or shutting the machine down and opening it up before installing the hardware. Now, however, a moderate-speed serial bus thatoperates at $100 \mathrm{kbits} / \mathrm{s}$ promises to give PC users the same and more flexibility than the Apple desktop bus offers Macintosh system users. Called Access.bus by its developer, Phil-ips-Signetics Corp., Sunnyvale, Calif., the bus was
originally created with Digital Equipment Corp., Maynard, Mass., and is used by DEC on its RISCbased workstations family.

The commercial "open" version of Access.bus differs slightly from the initial DEC version-it uses a $5-\mathrm{V}$ supply and can access 125 peripherals, while the initial version uses a $12-\mathrm{V}$ supply and is limited to 14 peripherals (DEC plans to upgrade its hardware to the open version). Based on the patented Philips interIC $\left(\mathrm{I}^{2} \mathrm{C}\right)$ bus, the scheme requires just two active signal wires-one for data


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and one for the clock. Two more conductors can be used in the cable for power and ground.
The bus' 100 -kbit/s data rate yields an actual information transfer rate of about $80 \mathrm{kbits} / \mathrm{s}$-more than adequate for modems, faxes, keyboards, mice, hand scanners, and low-to-moderate-speed peripherals. If power lines are included in the cable, the bus can also power the peripherals it connects to, up to a maximum current of 500 mA .

Besides offering a simple two- or four-wire connection, the bus allows peripherals to "hot plug" into a system. Each peripheral with the Access.bus port uses a microcontroller that
"announces" its presence on the bus when the unit is plugged in.

The host system's Access.bus port polls the bus regularly. When it detects a peripheral not in its bus map, it updates the bus map, adding the device to the list of available resources and assigning the device an address. The system then sends an acknowledgement signal to the peripheral to turn off the announcement. The entire operation takes just a few milliseconds.
The bus is aimed at three basic types of peripherals commonly used in desktop and portable computing-keyboard-like data-entry systems; positioning systems, such as mice; and
data-stream peripherals, including modems and facsimile units or hand-operated scanners. Unlike Apple's Desktop Bus scheme, which is a somewhat simple network with devices daisy-chained from one peripheral to the next, the Access.bus is a simple twowire bus: Peripherals simply tap all of the wires just like a connector taps the expansion bus on the PC motherboard. The Access.bus can have a maximum cable length of 8 meters.

Because the Access.bus is a bus-topology network, devices are distinguished by unique identification strings. Strings are defined for protocol and module revision, vendor and module name, and device
number. This data can be integrated into the peripheral and read out by the host during configuration.

Non-handheld peripherals built for the Access.bus should contain two female connectors that internally form the internal "T" connector. Handheld units might typically have a dedicated cable or a single female connector, and they come with a separate "T" connector that attaches to an existing cable. The host system need only have one female connector. Cables would typically be male-tomale. The simple four-contact male and female connectors are available from various suppliers, including Amp and Molex.
The message format


## TECHNOLOGY ADVANCES

used for communication between the host system and the Access.bus peripheral consists of three opening bytes of header information. They contain the destination address, the source address, a protocol flag bit, and the length of the data transfer ( 1 to 127 bytes). Following the header are the data bytes, and a checksum byte ends the packet. Messages are either data stream (protocol flag $=0$ ) or control/status information (flag $=1$ ).

The packetized protocol limits each interactive peripheral to occupy the bus for no more than 8 ms at a time. That ensures the other devices have a chance to update the screen every frame time and thus have

$\bar{T}$

## WIST TO COP?

 he first Access.bus developer's conference will be hosted by Philips-Signetics on April 22 at the Techmart Center in Santa Clara, Calif. There's no registration fee. Call Sharon Baker for details at (408) 991-3518.the system operate in real time. Non-interactive peripherals can become a bus master for 5 ms at a time, and must allow at least 12 ms from the time they relinquish the bus to the time they can again request to be a bus master.
All of the protocol and data transfers are handled
by a dedicated microcon-troller-a version of the 80C51 that includes 16 kbytes of ROM or EPROM, 256 bytes of RAM, two 16 -bit timercounters, four 8 -bit I/O ports, a full-duplex UART, and special low-power modes to trim power during idle conditions. The 83C654/87C654 acts as an interface converter and FIFO buffer, eliminating protocol overhead from the device driver and host.
One of the first companies to specialize in Access.bus products, Computer Access Technology Corp., Sunnyvale, Calif., is developing a PC/AT bus-interface adapter that will allow developers or users to add Access.bus capability to an
existing PC. The company will develop standard products as well as offer design consulting services.

Free copies of the Access.bus definition (version 1.1) are available from Philips-Signetics; contact Sharon Baker at (408) 9913518. A development kit with some MCUs, cables, connectors, source code for typical applications, and a PC adapter card will also be available in the late second or early third quarter. There's no royalty or licensing fee for using the Access.bus standard. The interface board will be available in the third quarter. Contact Dan Wilnai, Computer Access Technology, (408) 732-8910.

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# A Tiny IC Steps Up, Steps Down, Regulates, And Controls The Battery Drain In Portable PCs, And Laboratory And Medical Instruments. <br> Synchronous Rectifier UPS PC Battery Life 

Frank Goodenocgh

When power MOSFETs hit the scene over ten years ago, they were hailed as the ultimate device for efficient rectification at the output of low-voltage, high-current switching power supplies. Operating as synchronous rectifiers, they were expected to replace the diode. But Schottky diodes and other rectifiers that didn't need the "fancy" control circuits of synchronous rectifiers improved, pushing synchronous rectifiers out of the picture. Now, with the emergence of battery-powered PCs plus the need to conserve power, synchronous rectifiers have been given new life.
Today, you've got an edge on the competition if your laptop/notebook PC runs just 5\% longer on a battery charge. And exactly the same advantage applies to portable batterypowered instruments or remote (e.g., solarpowered) data-acquisition and/or control systems. Now Micro Linear Corp. has developed the ML4860, a combination of buck-regulator dc-dc converter and power controller aimed at providing that extra $5 \%$.
In the converter, power MOSFET $Q_{2}$ operates as a synchronous rectifier, replacing the usual Schottky diode (Fig. 1). The forward voltage drop of the rectifier falls from the 500 mV of a typical diode to the 50 mV of a low onresistance FET. Because both FETs in the ML4860 dissipate virtually zero power, the technique ups the efficiency of the main $5-\mathrm{V}$ supply by more than $5 \%$, dropping battery drain by a similar percentage. With a 6 -to-20V battery, this supply provides 5 to 30 W of

regulated $5-\mathrm{V}$ power for the PC's CPU, memory, and disk drive. (see "A simple synchronous rectifier, " $p .49$ ).
As noted, de-de conversion isn't the only task performed by this half-inch-on-a-side IC. Its control and regulation functions eliminate six space-hungry ICs typically priced at about $\$ 6$ in 0EM quantities.
Seven additional tasks performed by the ML4860 are:

## LAPTOP/NOTTEBOK.PC POWER CONTROLLLER

- When the laptop is connected to an external power source such as an ac adapter, it disconnects the battery from the input to the converter via external MOSFET switch $\mathrm{Q}_{3}$.
- It provides the system's off-chip power-management logic with a regulated 5 V from the battery at all times.
- Its second dc-dc converter (a boost circuit) provides a high-side-gatedrive voltage ( 11 V above the battery
voltage) for the system's six, external, n-channel MOSFET switches. They cost about $20 \%$ that of the p channel FETs needed if high-sidedrive voltages aren't used.
- It converts three, CMOS-level inputs from the power-management logic to three separate outputs that swing from ground to the high-side drive voltage. Each can drive an external FET switch to control power to a peripheral.
- It supplies a regulated 12 V for programming EEPROMs.
- It has two power-down operating modes offering quiescent currents as low as $75 \mu \mathrm{~A}$.
- It provides a battery-low signal to the power-management logic.

The chip operates from either an external ac adapter, or from a NiCd or alkaline battery pack. Input supply voltages range from 6 to 20 V . If


1. THE ML4860 IC DEVELOPS and controls the power for battery-powered PCs and instruments. Its buck-type switching regulator $_{\text {D }}$ employs two off-chip power MOSFETs. The upper one $\left(\mathbf{Q}_{1}\right)$ is the basic PWM switch. The lower one $\left(\mathbf{Q}_{2}\right)$ acts as a synchronous rectifier, replacing the typical Schottky diode, and increases the regulator's efficiency by $5 \%$.

## LAPTOP/NOTEBOOK-PC POWER CONTROLLER

the adapter is in use, with or without a battery charger, comparator $\mathrm{C}_{1}$ senses its output voltage (pin 26) relative to the battery voltage $V_{\text {battery }}$ (pin 28), and opens the off-chip battery switch MOSFET $Q_{3}$. If the ac adapter isn't in use, the comparator's output is high, turning on MOSFET $Q_{3}$ and connecting the battery to the pair of dc-dc converters and to the chip's $V_{\text {in }}$ port (pin 25). Internally, $\mathrm{V}_{\text {in }}$ is always connected to the micropower linear regulator because its 5V output (pin 10) runs the system's power-management logic, which in turn must have power at all times.
A second comparator, $\mathrm{C}_{2}$, provides
a low-battery signal. It compares the battery voltage appearing at pin 28 to the chip's $2.5-\mathrm{V}$ reference. Highresistance external resistors $\mathrm{R}_{1}$ and $\mathrm{R}_{2}$ set the voltage at the pin, depending on the battery voltage. The comparator's output goes high when the voltage at pin 28 drops below 2.5 V , providing a low-battery signal at pin 1 to the power-management logic. This logic can provide the user with a warning and/or start to shed the load by disconnecting peripherals via MOSFETs $Q_{3}, Q_{4}$, and $Q_{5}$.
The buck and the boost converters are driven synchronously by the chip's oscillator at 100 kHz . Al-

A SIMPLE SYNGHRONOUS REGTIIER

Increasing efficiency by implementing a synchronous rectifier in a switch-mode buck-type regulator is quite simple. All that's involved is replacing the typical Schottky diode $\mathrm{D}_{1}$ with power MOSFET $\mathrm{Q}_{2}$ (see

Given that $V_{\text {out }}=V_{\text {in }} \times D$, where D is the duty cycle, the diode will be on for $1 / 2$ of the PWM cycle for a 10 -V input (the nominal voltage from a six-cell battery pack). This yields an average conduction loss of about 250 mW , which translates into a $5 \%$ efficiency loss in the diode alone, for a $5-\mathrm{W}$ ( 5 V at 1 A ) output.

A forward drop of just 30 mV can be attained by using synchronous rectification and replacing the Schottky diode with an available power MOSFET that provides a mere 30 $\mathrm{m} \Omega$ of on-resistance. Average power loss drops to only 15 mW , increasing supply efficiency by almost $5 \%$. Because the duty cycle (on time) of the regulator's switch $\left(Q_{1}\right)$ decreases with increasing battery the figure). The MOSFET is turned on by the controller while the regulator's switch $Q_{1}$ is off, and vice versa. When conducting, the typical Schottky diode has a forward drop of about 500 mV at a current of 1 A .

voltage, the rectifier FET will be on for a greater percentage of the cycle. Thus, at higher battery voltages, the difference in system efficiency between Schottky-diode and FET rectifiers will be even more significant.
though optimized to run at 100 kHz , the converters' frequency-setting resistor connected between pin 2 and ground can program them to run at up to 200 kHz . The boost converter creates potential $\mathrm{V}_{\text {gate }}$, which will always be 11 V more positive than the battery or other input supply voltage. The converter's output (pin 6) is applied internally to four circuits: the two high-side drivers $\left(\mathrm{FD}_{1}\right.$ and $\mathrm{FD}_{2}$ ), the logic-to-MOSFET gatedrive block, and the $12-\mathrm{V}$ regulator.
High-side drivers $\mathrm{FD}_{1}$ and $\mathrm{FD}_{2}$ alternately drive (bring high to $\mathrm{V}_{\text {gate }}$ ) the gates of the buck regulator's FET switch $Q_{1}$ and the synchronous rectifier $Q_{2}$ with pulse-width-modulated pulses from pins 23 and 21, respectively. The logic-to-MOSFET gate-drive circuit takes 5 -V logic-level inputs from the power-manage-ment-logic circuit (pins 12, 14, and 16) and converts them to a trio of highside drive-level outputs. The three outputs (pins 13,15 , and 17 ) are at ground for an input of logic-level zero, and at $\mathrm{V}_{\text {gate }}$ for an input of log-ic-level one. They turn FET switches $\mathrm{Q}_{3}, \mathrm{Q}_{4}$, and $\mathrm{Q}_{5}$ on and off. The $12-\mathrm{V}$ linear regulator's output (pin 9) supplies as much as 100 mA to program EEPROMs. Logic-level signals from the power-management-logic circuit turn it on and off (pin 8).
By way of pins 3 and 4 , power-management logic puts the chip/system into one of three operating modes: run, standby, or sleep. Holding pin 4 high puts the chip in the "all-sys-tems-go" run mode, and the IC draws 4 mA of quiescent current. Bringing pin 3 high and pin 4 low puts the IC into standby. Only the low-battery comparator and the $5-\mathrm{V}$ linear regulator for the power-management logic are on and the IC draws just $110 \mu \mathrm{~A}$. Pulling pins 3 and 4 low puts the chip to sleep. Only the 5 -V regulator remains on, and quiescent current drops to $75 \mu \mathrm{~A}$.
One unique circuit can provide "lossless" current sensing to protect MOSFETs $Q_{1}$ and $Q_{2}$. When $Q_{1}$ is turned on hard (in saturation), the voltage at $Q_{1}$ 's source is measured by the IC (pin 22) relative to $\mathrm{V}_{\text {in }}$. If that voltage is more than 200 mV , the converter shuts down. Essentially,

## LAPTOP/NOTEBOOK-PC POWER CONTROLLER



I2. A COMPLETE power-supply/control subsystem for a battery-powered PC is easy to build on this 2 -in. ${ }^{2}$ evaluation board from Micro Linear, which uses the company's ML4860 controller IC. The two $100-\mathrm{kHz}$ Coiltronics inductors are quite small when compared with inductors used for higher-power, higher-frequency switching-regulator supplies.
the FET's on-resistance becomes the current-sense resistor. The default threshold of 200 mV represents the drop across a $50-\mathrm{m} \Omega$ MOSFET passing 4 A . If a higher current-limit threshold voltage is required-for example, if a larger current is controlled, or smaller FETs (higher on-resistance) are used-a resistor is connected from pin 24 to ground. The conventional, volt-age-mode controller gets its feedback voltage from the output via pin 20. A softstart capacitor between pin 18 and ground limits the
pulse width at power-up.
As noted earlier, the "jack-of-alltrades" control and regulation features of the ML4860 can save significant pc-board space in a notebook PC, a laptop, or a portable instrument. Though not a true indicator of the minimum circuit size possible from the chip, Micro Linear's evaluation board illustrates what can be accomplished (Fig. 2). The 2 -in. ${ }^{2}$ board is laid out for ease of use (for probing with an oscilloscope and a meter).

The board's single ML4860 replaces various parts needed in a typical power-management and control system, including: a LinCMOS PWM controller (such as the TLC $4 \times x x$ ), a micropower linear-regulator IC (such as the MAX667), a dual comparator (like the TLC393), a boostregulator IC (such as the MAX63x), a multiple n-channel FET driver (like the MAX621), and some glue logic. In OEM quantities, their combined cost would run about $\$ 6$.


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## LAPTOP/NOTEBOOK-PC POWER CONTROLLER

The three, small square D-PAKs on the evaluation board contain MOSFETs $Q_{1}, Q_{2}$, and $Q_{3}$. A pair of Siliconix "Little foot" devices could easily replace them. Each "Little foot" contains two isolated $50-\mathrm{m} \Omega$ MOSFETs in an 8-pin SOIC. Poten-
tially, in some applications, just three 8-pin SOICs could hold the six external FETs.

The ML4860 isn't limited to smaller PC designs. Like so many new analog ICs originally aimed at narrow niches, the breadth of its applica-

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# Digital Audio DRIVES 14-T0-20. BIT DAC Designs 

Although little new appears to be happening in the generalpurpose high-resolution (greater than 13 bits) monolithic digital-to-analog converter domain, IC DACs aimed strictly at digital-audio applications are on a roll. And some of this audio-DAC tech-nology-primarily several new DAC architectures-is being transferred to the general-purpose arena. In fact, several of the newest generalpurpose DACs are based on audioDAC technology, with a potential for much more in the future.

Today, you can buy 16 -to-20-bit IC

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## InNOVATIVE

 Designs For Audio Hint At Future 16-To-20-Bit DACs With More Than 16-Bit Dc Accuracy.audio DACs that offer a dynamic range of more than 100 dB and a sig-nal-to-noise ratio of 120 dB (Table 1). Also available are 16-to-20-bit gener-al-purpose IC analog-to-digital converters (ADCs) with similar dynamic range that provide accuracy levels of 16 bits or greater at dc and over temperature.

But when it comes to general-purpose monolithic DACs offering dc accuracy over temperature, only a few that are even 16 -bit accurate exist (Table 2). In fact, like their 14-bit kin, about half are only 14 -bit accurate (monotonic) at dc, even at a temperature of just $25^{\circ} \mathrm{C}$.

The low level of high-resolution general-purpose DAC development runs directly opposite the 12 -bit gen-eral-purpose ADC arena, in which a broad range of new-design activity is underway (ELECTRONIC DESIGN, Sept. 12, 1991, p. 63). Examples of these new designs range from quad and even octal DACs to RF-generating DACs. This action at 12 bits stands as a precursor of future action at higher resolution.

The most exciting development in the general-purpose field comes from TriQuint Semiconductor Corp., whose 14-bit gallium-arsenide DAC, which has a $2-\mathrm{GHz}$ update rate (at a temperature of $25^{\circ} \mathrm{C}$ ), is close to fru-
ition (see the opening figure). Funded jointly by General Electric, Motorola, Hughes, and Sciteq, it's the only high-resolution DAC aimed at direct digital synthesis (DDS) of high-frequency RF waveforms. This application area has been heating up, as witnessed by the recent announcement of a pair of 12 -bit DACs with fast $100-$ and $500-\mathrm{MHz}$ update rates (Electronic design, Feb. 20, pps. 41 and 152).

Multiple DACs per die are now following this trend, with both a little help from digital-audio DAC technology and new architectures. In fact, a pair of 14 -bit, octal, voltage-output DACs with a new architecture will appear within the next 30 to 60 days. And these multiple DACs provide a digital I/O more conducive to a microprocessor interface, rather than the typical brute-force approach with latchless 14 to 18 parallel inputdata lines.
Though aimed at digital-signalprocessing applications instead of waveform synthesis, a few of the lat-
est DACs provide a serial I/O and dynamic (ac) specifications. These specifications include total harmonic distortion and signal-to-noise ratio.

## 20 Bits 0R Bust

After more than ten years in development, the compact-disc player exploded on the U.S. consumer market about six years ago. And most of these sophisticated machines from Japan contained one or two 16-bit IC DACs made by Burr-Brown. The first of these 16 -bit DACs, the PCM53, is a 24 -pin DIP that contains a single, very conventional, 16 -bit voltage-output DAC with an unbuffered, 16 -line, parallel-digital input (see "Compact-disc players, digi-tal-audio DACs, and oversampling," $p .64$ ). Its architecture forms the basis of most general-purpose monolithic DACs.
A segment decoder in the PCM53 monolithic DAC converts the three most-significant-bit inputs to seven lines that drive seven current switches, which in turn control (switch on
and off) seven equal-current sources. Thirteen additional current switches control the remaining least-significant-bit currents. These LSB currents are developed by a binaryweighted, laser-trimmed, thin-film resistor network.

The PCM53 contains its own bur-ied-Zener voltage reference and output op amp, setting the standard for most future audio DACs. Currentoutput ( $\pm 1-\mathrm{mA}$ ) versions are also available. The DAC puts out $\pm 10 \mathrm{~V}$ at $\pm 5 \mathrm{~mA}$ and runs off $\pm 15-\mathrm{V}$ rails (both typical of the general-purpose genre then and now). However, while its "audio" specifications are limited to harmonic distortion and dynamic range, virtually all of the specifications expected on the data sheet for a typical general-purpose DAC are included.
Driven by the requirements of $C D$ players for higher performance at lower cost, these once general-purpose DACs quickly evolved through several generations. Early on, digital oversampling filters were added

## TABE 1: MONOLTHIG 16-, 18-, ANJ 20-BIT DGTAL-AUDIO DAGS

| Company | Model | Total harmonic distortion plus noise (dB) at outputs of |  |  |  |  | Signal-tonoise ratio (dB) | Dynamic range (dB) | Channel separation (dB) | Midscale error | $\begin{aligned} & V_{\text {out }}^{\text {Out }} \\ & (\mathrm{V} / \mathrm{mA}) \end{aligned}$ | $I_{\text {out }}$ (mA) | Maximum oversampling Factor |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Analog Devices | AD1862 | 20 | 1 | -96 | -80 | -42 | 113 | 102 | NA | $\pm 5 \mu \mathrm{~A}$ | NA | $\pm 1$ | 16 |
| Burr-Brown | PCM63 | 20 | 1 | -96 | -82 | -44 | 116 | 104 | NA | $\pm 10 \mathrm{mV}$ | NA | $\pm 2$ | 16 |
| Philips/ Signetics | SAA7340 (alone) with TDA1547 | $\begin{aligned} & 20 \\ & 20 \end{aligned}$ | $\begin{aligned} & 2 \\ & 2 \end{aligned}$ | $\begin{aligned} & -93 \\ & -93 \end{aligned}$ | $\begin{aligned} & \text { NS } \\ & -84 \end{aligned}$ | $\begin{aligned} & \text { NS } \\ & -44 \end{aligned}$ | $\begin{aligned} & 100 \\ & 101 \end{aligned}$ | $\begin{array}{r} 93 \\ >93 \end{array}$ | $\begin{gathered} 100(t) \\ 101 \end{gathered}$ | $\begin{aligned} & \text { NS } \\ & \text { NS } \end{aligned}$ | $1 \mathrm{~ms} / \mathrm{NS}$ | $\begin{aligned} & \text { NA } \\ & \text { NA } \end{aligned}$ | $\begin{aligned} & 16 \\ & 16 \end{aligned}$ |
| Analog Devices | AD1865 <br> AD1868 <br> AD1864 <br> AD1860 <br> AD1861 | $\begin{aligned} & 18 \\ & 18 \\ & 18 \\ & 18 \\ & 18 \end{aligned}$ | $\begin{aligned} & 2 \\ & 2 \\ & 2 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & -87 \\ & -84 \\ & -92 \\ & -92 \\ & -87 \end{aligned}$ | $\begin{aligned} & -73 \\ & -61 \\ & -73 \\ & -73 \\ & -75 \end{aligned}$ | $\begin{aligned} & -54 \\ & -46 \\ & -34 \\ & -34 \\ & -36 \end{aligned}$ | $\begin{gathered} 107 \\ 95 \\ 102 \\ 102 \\ 107 \end{gathered}$ | $\begin{aligned} & 94 \\ & 86 \\ & 94 \\ & 94 \\ & 96 \end{aligned}$ | $\begin{aligned} & 110 \\ & 101 \\ & 110 \\ & N A \\ & N A \end{aligned}$ | $\begin{aligned} & \pm 4 \mathrm{mV} \\ & \pm 15 \mathrm{mV} \\ & \pm 4 \mathrm{mV} \\ & \pm 3 \mathrm{mV} \\ & \pm 10 \mathrm{mV} \end{aligned}$ | $\begin{gathered} \pm 3 / \pm 8 \\ \pm 1(t) / \pm 1(\mathrm{t}) \\ \pm 3 / \pm 8 \\ \pm 3 / \pm 8 \\ \pm 3 / \pm 8 \end{gathered}$ | $\begin{aligned} & \pm 1 \\ & N A \\ & \pm 1 \\ & \pm 1 \\ & \pm 1 \end{aligned}$ | $\begin{gathered} 16 \\ 16 \\ 16 \\ 8 \\ 16 \end{gathered}$ |
| Burr-Brown | $\begin{aligned} & \text { PCM61 } \\ & \text { PCM67 } \\ & \text { PCM1700 } \\ & \text { PCM58 } \end{aligned}$ | $\begin{aligned} & 18 \\ & 18 \\ & 18 \\ & 18 \end{aligned}$ | $\begin{aligned} & 1 \\ & 2 \\ & 2 \\ & 1 \end{aligned}$ | $\begin{aligned} & -92 \\ & -92 \\ & -92 \\ & -96 \end{aligned}$ | $\begin{aligned} & -74 \\ & -70 \\ & -74 \\ & -80 \end{aligned}$ | $\begin{aligned} & -34 \\ & -40 \\ & -34 \\ & -40 \end{aligned}$ | $\begin{gathered} 112(t) \\ 110(t) \\ 96 \\ 126(t) \end{gathered}$ | $\begin{aligned} & 108(t) \\ & 108(t) \\ & 108(t) \\ & 108(t) \end{aligned}$ | $\begin{gathered} \text { NA } \\ 106(t) \\ 96 \\ \text { NA } \end{gathered}$ | $\begin{gathered} \pm 30(\mathrm{t}) \\ \mathrm{NS} \\ \pm 10 \mathrm{mV} \\ \pm 10 \mathrm{mV} \end{gathered}$ | $\begin{gathered} \pm 3(t) / \pm 8 \\ N A \\ \pm 3 / \pm 8(t) \\ N A \end{gathered}$ | $\begin{gathered} \pm 1(t) \\ \pm 1.2(t) \\ \pm 0.7(t) \\ \pm 1 \end{gathered}$ | $\begin{gathered} 8 \\ 16 \\ 16 \\ 8 \end{gathered}$ |
| Crystal | CS4328 | 18 | 2 | -90 | -73 | -33 | 120 | 93 | 100 | $\pm 1 \mathrm{mV}$ | $\pm 1.9 / \pm 3$ | NA | 8 |
| Sony | CXD2558 | 18 | 2 | -80(t) | NS | NS | 90 (t) | NS | NS | NS | (1) | NA | 16 |
| Analog Devices | AD1851 AD1866 AD1856 | $\begin{aligned} & 16 \\ & 16 \\ & 16 \end{aligned}$ | $\begin{aligned} & 1 \\ & 2 \\ & 1 \end{aligned}$ | $\begin{aligned} & -87 \\ & -80 \\ & -92 \end{aligned}$ | $\begin{aligned} & -75 \\ & -74 \\ & -74 \end{aligned}$ | $\begin{aligned} & -36 \\ & -34 \\ & -34 \end{aligned}$ | $\begin{gathered} 107 \\ 95(t) \\ \text { NS } \end{gathered}$ | $\begin{gathered} 96 \\ 90(t) \\ \text { NS } \end{gathered}$ | $\begin{aligned} & \text { NA } \\ & 108 \\ & \text { NA } \end{aligned}$ | $\begin{aligned} & \pm 10 \mathrm{mV} \\ & \pm 30 \mathrm{mV} \\ & \pm 30 \mathrm{mV} \end{aligned}$ | $\begin{aligned} & \pm 3 / \pm 8 \\ & \pm 1 / \pm 1 \\ & \pm 3 / \pm 8 \end{aligned}$ | $\begin{aligned} & \pm 1 \\ & N A \\ & \pm 1 \end{aligned}$ | $\begin{gathered} 16 \\ 16 \\ 8 \end{gathered}$ |
| Burr-Brown | PCM60 PCM66 PCM56 PCM55 PCM54 PCM53 | $\begin{aligned} & 16 \\ & 16 \\ & 16 \\ & 16 \\ & 16 \\ & 16 \end{aligned}$ | $\begin{gathered} 1 \\ 2 \text { outputs } \\ 1 \\ 1 \\ 1 \\ 1 \end{gathered}$ | -86 -86 -92 -87 -92 -93 | $\begin{gathered} 68(\mathrm{t}) \\ -68(\mathrm{t}) \\ -74(\mathrm{t}) \\ -67 \\ -74 \\ -74 \end{gathered}$ | $\begin{gathered} -28(t) \\ -28(t) \\ -34(t) \\ -28 \\ -34 \\ -34 \end{gathered}$ | $90(\mathrm{t})$ $90(\mathrm{t})$ NS NS NS NS | 96(t) <br> 96(t) <br> 96(t) <br> 96(t) <br> 96(t) <br> 96(t) | $\begin{aligned} & \text { NA } \\ & N S \\ & N A \\ & N A \\ & N A \\ & N A \end{aligned}$ | $\begin{aligned} & \pm 30 \mathrm{mV} \\ & \pm 30 \mathrm{mV} \\ & \pm 30 \mathrm{mV} \\ & \pm 30 \mathrm{mV} \\ & \pm 30 \mathrm{mV} \\ & \pm 50 \mathrm{mV} \end{aligned}$ | $\begin{aligned} & 2.8 / 0.028 \\ & 2.8 / 0.028 \\ & \pm 3 / \pm 8 \\ & \pm 3 / \pm 2 \\ & \pm 3 / \pm 2 \\ & \pm 10 / \pm 5 \end{aligned}$ | $\begin{aligned} & \text { NA } \\ & \text { NS } \\ & \pm 1 \\ & \pm 1 \\ & \pm 1 \\ & \pm 1 \end{aligned}$ | $\begin{gathered} 4 \\ 4 \\ 8 \\ 16 \\ 16 \\ 16 \end{gathered}$ |

All specifications are at $25^{\circ} \mathrm{C}$ and are maximums or minimums unless noted typical ( t ). $\mathrm{NA}=$ not available. $\mathrm{NS}=$ not specified. $\mathrm{FSR}=$ full-scale range.
(1) Each of the two differential outputs of the Sony delta-sigma DAC consists of a 5-V train of ones and zeros ready for application to an analog low-pass filter.
ahead of the DAC, and the digital I/ 0 was changed from parallel to serial. To handle the simpler serial I/ 0 , DACs like the Burr-Brown PCM56 added a serial-to-parallel shift register between the serial input and the DAC itself.

General-purpose DAC specifications gradually gave way to audioDAC specifications (Table 1, again). The supply rails dropped to $\pm 5 \mathrm{~V}$, the standard output voltage became $\pm 3 \mathrm{~V}$, and SOIC packages appeared. Resolution moved to 18 bits and single $5-\mathrm{V}$ supply devices appeared. Analog Devices joined the fray and two 18 -bit DACs were crammed into DIPs and SOICs in 1989. Oversampling factors went from 1 to 16 , but basic DAC architectures remained virtually unchanged.

Over the last two years, dramatic changes have evolved in high-resolution IC DACs. New architectures began to emerge, such as those on Crystal Semiconductor's dual 18-bit delta-sigma CS4328 audio DAC (also called a one-bit or bit-stream DAC),
and Burr-Brown's 20-bit PCM63P audio DAC, a single-channel currentoutput device based on a unique variant of the conventional multibit architecture. More recently, BurrBrown used an innovative architecture on its 18-bit dual current-output PCM67 DAC, combining one-bit and multibit circuits (see "New DAC architectures and noise shaping,"p. 62).

ICs designed specifically for nextgeneration digital-audio systems are now appearing. Take Crystal's CS4215 and CS4216 dual 16-bit deltasigma codecs, for example, aimed at multimedia applications (ELectronIC Design, Sept. 12, 1991, p.53). Designed to give PCs the ability to generate and/or process high-quality stereo audio, each IC's core contains a pair of 16-bit delta-sigma ADCs and a pair of 16 -bit delta-sigma DACs. By mid-year, a similar device, the AD1849, is expected from Analog Devices.

Because nearly all but the leastexpensive compact-disc players

| Linearity dB | Gain <br> Error <br> (\% of | $\begin{aligned} & \text { Match } \\ & \text { FSR) } \end{aligned}$ | Architecture | $(\mathrm{V} / \mathrm{mA})^{\text {Power }}$ | (mW) | Package type | $\begin{aligned} & \text { Price } \\ & (1000 \mathrm{~s}) \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\pm 1$ | $\pm 2$ | NA | Conventional | $\pm 12 / \pm 6$ | $288(t)$ | 16-pin DIP | \$13.50 |
| $\pm 1$ | $\pm 2$ | NA | Sign-magnitude | $\pm 5 /+15,-45$ | 300 | 28 -pin DIP | \$11.80 |
| $\begin{array}{r}  \pm 1 \\ \pm 0.2 \end{array}$ | $\begin{aligned} & \text { NS } \\ & \text { NS } \end{aligned}$ | $\begin{aligned} & 0.25 \\ & \text { NS } \end{aligned}$ | Delta sigma Delta sigma | $\begin{gathered} 5 / 75 \\ \pm 5 / \pm 80 \end{gathered}$ | $\begin{gathered} 375 \\ 1300 \end{gathered}$ | $\begin{aligned} & \text { 44-pin QFP } \\ & \text { 32-pin DIP } \end{aligned}$ | $\begin{aligned} & \$ 26.00 \\ & \$ 17.50 \end{aligned}$ |
| $\begin{aligned} & \pm 2 \\ & \pm 3 \\ & 2(t) \\ & \text { NS } \\ & \text { NS } \end{aligned}$ | $\begin{aligned} & \pm 1 \\ & \pm 1 \\ & \pm 1 \\ & \pm 2 \\ & \pm 1 \end{aligned}$ | $\begin{aligned} & 0.8 \\ & \pm 1 \\ & \pm 0.8 \\ & \text { NA } \\ & \text { NA } \end{aligned}$ | Conventional Conventional Conventional Conventional Conventional | $\begin{gathered} \pm 5 / \pm 26 \\ +5 / 14 \\ \pm 5 \text { to } \pm 12 / \pm 28 \\ \pm 5 \text { to } \pm 12 / \pm 15 \\ \pm 5 / \pm 15 \end{gathered}$ | $\begin{gathered} 260 \\ 70 \\ 265 \\ 300 \\ 100(t) \end{gathered}$ | 24-pin DIP, 28-pin SOIC <br> 16 -pin DIP,SOIC <br> 24-pin DIP <br> 16-pin DIP <br> 16 -pin DIP,SOIC | $\begin{aligned} & \$ 14.25 \\ & \$ 9.95 \\ & \$ 14.25 \\ & \$ 9.55 \\ & \$ 5.00 \end{aligned}$ |
| $\begin{aligned} & \text { NS } \\ & \pm 1 \\ & \pm 1 \\ & \text { NS } \end{aligned}$ | $\begin{aligned} & \pm 2(t) \\ & \pm 10 \\ & \pm 3 \\ & \pm 2 \end{aligned}$ | $\begin{aligned} & N A \\ & \pm 5 \\ & \pm 3 \\ & N A \end{aligned}$ | Conventional One-bit + multibit Conventional Conventional | $\begin{gathered} \pm 5 \text { to } \pm 12+17,-35 \\ 5 / 20 \\ \pm 5 /+40,-16 \\ 5,-12 / 10,-30 \end{gathered}$ | $\begin{aligned} & 260 \\ & 105 \\ & 380 \\ & 410 \end{aligned}$ | $\begin{aligned} & \text { 16-pin DIP } \\ & \text { 16-pin DIP,20-pin SOIC } \\ & 28 \text {-pin DIP } \\ & 28 \text {-pinDIP } \end{aligned}$ | $\begin{aligned} & \$ 7.40 \\ & \$ 10.00 \\ & \$ 10.95 \\ & \$ 14.55 \end{aligned}$ |
| NS | $\pm 5$ | 0.1 dB | Dellta-sigma | $\pm 5 / \pm 55,5 / 60$ | 850 | 28-pin DIP | \$29.00 |
| NS | NS | NS | Delta-sigma | 5/NS | NS | 28 -pin SOIC | \$12.00 |
| $\begin{aligned} & \text { NS } \\ & \pm 3 \\ & \text { NS } \end{aligned}$ | $\begin{gathered} \pm 1 \\ \pm 3 \\ \pm 2(t) \end{gathered}$ | $\begin{aligned} & \text { NA } \\ & \pm 3 \\ & N A \end{aligned}$ | Conventional Conventional Conventional | $\begin{gathered} \pm 5 / \pm 15 \\ 5 / 14 \\ \pm 5 \text { to } \pm 12,+17,-35 \end{gathered}$ | $\begin{gathered} 100(t) \\ 70 \\ 260 \end{gathered}$ | 16-pin DIP,SOIC <br> 16 -pin DIP,SOIC 16-pin DIP | $\begin{aligned} & \$ 4.65 \\ & \$ 8.95 \\ & \$ 9.00 \end{aligned}$ |
| NS NS NS NS NS NS | $\begin{aligned} & \pm 10 \\ & \pm 10 \\ & \pm 2(t) \\ & \pm 2(t) \\ & \pm 2(t) \\ & \pm 1(t) \end{aligned}$ | $\begin{aligned} & \pm 1(t) \\ & \pm 1(t) \\ & \text { NA } \\ & \text { NA } \\ & \text { NA } \\ & \text { NA } \end{aligned}$ | Conventional <br> Conventional <br> Conventional <br> Parallel in, conventional <br> Parallel in, conventional <br> Parallel in, conventional | $\begin{gathered} 5 / 9.5(\mathrm{t}) \\ 5 / 9.5(\mathrm{t}) \\ \pm 5 \mathrm{to}+12+17,-35 \\ \pm 5 /+20,-25 \\ \pm 5 \text { to } \pm 12,+20-25 \\ \pm 15,+5 / \pm 30,+10 \end{gathered}$ | $\begin{gathered} 50 \\ 50 \\ 260 \\ \text { NS } \\ \text { NS } \\ \text { NS } \end{gathered}$ | 16 -pin SOIC <br> 20 -pin SOIC <br> 16 -pin DIP <br> 24 -pin SOIC <br> 28 -pin DIP <br> 24-pin DIP | NA <br> $\$ 7.40$ <br> $\$ 6.80$ <br> $\$ 9.25$ <br> $\$ 9.25$ <br> $\$ 11.80$ |

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## TABLE 2: MONOLTHIC GENERIL-PUBPOSE 14-18 BIT DIGS

| Company | Model | $\begin{aligned} & \text { Resolution } \\ & \text { (bits) } \end{aligned}$ | $\begin{gathered} \text { Outpu } \\ \text { Voltage } \end{gathered}$ | type Current |  | ence <br> Internal | Monotonic Over tem- <br> at per$25^{\circ} \mathrm{C}$ ature <br> (bits) (bits) |  | $\begin{aligned} & \text { Integral } \\ & \text { non-linearity } \end{aligned}$ (bits) |  | scale <br> ling <br> full <br> le <br> ( $\mu \mathrm{s}$ ) | Features and output range | $\begin{gathered} \text { Digital } \\ \text { l/0 } \end{gathered}$ | Package type | $\begin{aligned} & \text { Price } \\ & \text { (1000s) } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Analog Devices | AD7534 AD7535 AD7536 AD7538 AD7840 AD7244 (dual) | $\begin{aligned} & 14 \\ & 14 \\ & 14 \\ & 14 \\ & 14 \\ & 14 \end{aligned}$ |  | $:$ |  | - | $\begin{aligned} & 14 \\ & 14 \\ & 14 \\ & 14 \\ & 14 \\ & 14 \end{aligned}$ | $\begin{aligned} & 14 \\ & 14 \\ & 14 \\ & 14 \\ & 14 \\ & 14 \end{aligned}$ | $\begin{aligned} & 13 \\ & 13 \\ & 13 \\ & 13 \\ & 13 \\ & 13 \end{aligned}$ | $\begin{gathered} 0.003 \\ 0.003 \\ 0.003 \\ 0.003 \\ 112.2 \mathrm{SB} \\ 1 / 2 \mathrm{LSB} \end{gathered}$ | $\begin{aligned} & 1.5 \\ & 1.5 \\ & 1.5 \\ & 1.5 \\ & 4 \\ & 4 \end{aligned}$ | $\begin{gathered} 1,2 \\ 1,2 \\ 1,2,3 \\ 1,2 \\ 4 \\ 70 \end{gathered}$ | $\begin{aligned} & 25 \\ & 26 \\ & 26 \\ & 27 \\ & 28 \\ & 63 \end{aligned}$ | $\begin{gathered} 40,41 \\ 40,41,42 \\ 42,43,44 \\ 45 \\ 42,45 \\ 45,46 \end{gathered}$ | $\begin{aligned} & \$ 14.00 \\ & \$ 16.00 \\ & \$ 16.00 \\ & \$ 9.00 \\ & \$ 9.00 \\ & \$ 15.00 \end{aligned}$ |
| Harris Semiconductor | ICL7134 | 14 |  | - | - |  | 14 | 13 | 14 | 1/2 LSB | 3 | 17 | 26 | 43 | \$14.00 |
| Micro Power Systems | MP7614 | 14 |  | - | - |  | 13 | 13 | 12 | 0.01 | 2 (t) | 19 | 35 | 40,51 | NA |
| Sipex | SP7514 | 14 |  | - | - |  | 14 | 14 | 14 | NS | $2(t)$ | 1,12 | 35 | 40 | \$16.00 |
| Analog Devices | $\begin{aligned} & \text { AD569 } \\ & \text { AD669 } \\ & \text { AD766 } \\ & \text { AD7846 } \end{aligned}$ | $\begin{aligned} & 16 \\ & 16 \\ & 16 \\ & 16 \end{aligned}$ |  | - | - | - | $\begin{aligned} & 16 \\ & 16 \\ & 15 \\ & 16 \end{aligned}$ | $\begin{aligned} & 16 \\ & 15 \\ & 15 \\ & 16 \end{aligned}$ | $\begin{aligned} & 12 \\ & 14 \\ & \text { NS } \\ & 12 \end{aligned}$ | $\begin{aligned} & 0.001 \\ & 0.0008 \\ & 0.00015 \\ & 0.003 \end{aligned}$ | $\begin{gathered} 6 \\ 13 \\ 1.5(t) \\ 9 \end{gathered}$ | $\begin{aligned} & 5 \\ & 6 \\ & 7 \\ & 8 \end{aligned}$ | $\begin{gathered} 29 \\ 30 \\ 31 \\ 30,37,38 \end{gathered}$ | $\begin{gathered} 43,44 \\ 43,46 \\ 47 \\ 42,44,48 \end{gathered}$ | $\begin{aligned} & \$ 16.00 \\ & \$ 14.00 \\ & \$ 9.00 \\ & \$ 16.00 \end{aligned}$ |
| Burr-Brown | DAC700, 01, 02, 03 DAC707, 08, 09 DAC710 DAC725 (dual) | $\begin{aligned} & 16 \\ & 16 \\ & 16 \\ & 16 \end{aligned}$ |  |  |  |  | $\begin{aligned} & 14 \\ & 14 \\ & 15 \\ & 14 \end{aligned}$ | $\begin{aligned} & 14 \\ & 14 \\ & 15 \\ & 14 \end{aligned}$ | $\begin{aligned} & 14 \\ & 14 \\ & 14 \\ & 14 \end{aligned}$ | $\begin{aligned} & 0.003 \\ & 0.003 \\ & 0.003 \\ & 0.003 \end{aligned}$ | $\begin{aligned} & 8 \\ & 8 \\ & 8 \\ & 8 \end{aligned}$ | $\begin{gathered} 9 \\ 9 \\ 9,20 \\ 10 \end{gathered}$ | $\begin{aligned} & 33 \\ & 33 \\ & 32 \\ & 34 \end{aligned}$ | $\begin{aligned} & 49 \\ & 49 \\ & 49 \\ & 48 \end{aligned}$ | $\$ 15$ to $\$ 27$ $\$ 16.00$ $\$ 32.00$ |
| Datel | DAC-HP163* | 16 | - |  |  | - | 14 | 14 | 14 | 0.005 | 15(t) | 16 | 32 | 49 | \$67.00 |
| Harris | ICL7121 | 16 |  | - | - |  | 16 | 16 | 15 | 1/2 LSB | 3 | 18 | 29 | 43 | \$18.00 |
| Micro Networks | M 3 3290* | 16 | - | - |  | - | 14 | 14 | 15 | 0.003 | 8 | 9 | 32 | 49 | \$30 to \$60 |
| Micro Power Systems | MP7616 MP7626 MP7636 | $\begin{aligned} & 16 \\ & 16 \\ & 16 \end{aligned}$ |  | - |  |  | $\begin{aligned} & 13 \\ & 16 \\ & 16 \end{aligned}$ | $\begin{aligned} & 13 \\ & 15 \\ & 16 \end{aligned}$ | $\begin{aligned} & 12 \\ & 14 \\ & 14 \end{aligned}$ | $\begin{gathered} 0.01 \\ 0.1 \\ 1 / 2 \mathrm{LSB} \end{gathered}$ | $\begin{aligned} & 2(t) \\ & 2(t) \\ & 2(t) \end{aligned}$ | $\begin{aligned} & 19 \\ & 19 \\ & 19 \end{aligned}$ | $\begin{aligned} & 32 \\ & 36 \\ & 29 \end{aligned}$ | $\begin{gathered} 52,54 \\ 43,46,44 \\ 40 \end{gathered}$ | $\begin{aligned} & \text { NA } \\ & \text { NA } \\ & \text { NA } \end{aligned}$ |
| SPT | HDAC52160 | 16 |  | , |  | - | 15 | 14 | 14 | 0.0015 | 0.15 | 15 | 32 | 53 | NA |
| Sipex | $\begin{gathered} \text { HS9390* } \\ \text { SP1148* } \\ \text { SP7516/SP3160 } \\ \text { HS9371* } \\ \text { S9P3316 } \\ \text { SP9320(dual) } \\ \text { SP9321(dual) } \end{gathered}$ | $\begin{aligned} & 16 \\ & 16 \\ & 16 \\ & 16 \\ & 16 \\ & 16 \\ & 16 \end{aligned}$ | - |  | $!$ |  | $\begin{aligned} & 14 \\ & 16 \\ & 14 \\ & 16 \\ & 15 \\ & 16 \\ & 16 \end{aligned}$ | 13 15 14 16 15 15 15 | $\begin{aligned} & 14 \\ & 14 \\ & 14 \\ & 16 \\ & 15 \\ & 13 \\ & 13 \end{aligned}$ | $\begin{aligned} & 0.006 \\ & 0.00076 \\ & \text { NS } \\ & 0.0015 \\ & 0.0015 \\ & \text { NS } \\ & \text { NS } \end{aligned}$ | $\begin{aligned} & 0.15 \\ & 20 \\ & 2(t) \\ & 5(t) \\ & 5(t) \\ & 3(t) \\ & 3(t) \end{aligned}$ | $\begin{gathered} 22 \\ 23 \\ 1,12 \\ 13 \\ 1,12 \\ 14 \\ 14 \end{gathered}$ | $\begin{gathered} 60 \\ 61 \\ 35 \\ 29 \\ 30 \\ 29 \\ 34,37,38 \end{gathered}$ | $\begin{gathered} 56 \\ 56 \\ 50 / 52 \\ 48 \\ 49 \\ 43 \\ 45 \end{gathered}$ | $\begin{aligned} & \$ 184.00 \\ & \$ 130.00 \\ & \$ 9 . \$ 22 \\ & \$ 69.00 \\ & \$ 30.00 \\ & \$ 32.00 \\ & \$ 32.00 \end{aligned}$ |
| Analog Devices | AD1139* | 18 | - | - |  | - | 18 | 16 | 18 | 1/2 LSB | 40 | 24 | 65 | 56 | \$175.00 |
| Burr-Brown | $\begin{aligned} & \text { DSP201/202(dual) } \\ & \text { DAC729** } \end{aligned}$ | $\begin{aligned} & 18 \\ & 18 \end{aligned}$ |  |  |  |  | $\begin{aligned} & 14 \\ & 18 \end{aligned}$ | $\begin{aligned} & 14 \\ & 16 \end{aligned}$ | $\begin{aligned} & 14 \\ & 17 \end{aligned}$ | $\begin{gathered} 0.006 \\ 0.00076 \end{gathered}$ | $\begin{gathered} 2.5(t) \\ 8(t) \end{gathered}$ | $\begin{aligned} & 11 \\ & 20 \end{aligned}$ | $\begin{aligned} & 64 \\ & 39 \end{aligned}$ | $\begin{aligned} & 48 \\ & 55 \end{aligned}$ | $\begin{gathered} \$ 21 / \$ 26 \\ \$ 98.00 \end{gathered}$ |
| Sipex | SP9380* | 18 | - |  |  | - | 18 | 16 | 18 | 1/2LSB | 30(t) | 24 | 62 | 56 | \$160.00 |

All specifications are maximum or minimums over temperature unless otherwise noted typical (t). Specifications are shown for the model offering monotonicity over temperature for the greatest number of bits. Prices have been rounded off to the nearest dollar. NS $=$ not specified. $N A=$ not available.
${ }^{*}=$ Hybrid unit.
Features and output range: $1=$ micropower, $\mathrm{R}-2 \mathrm{R}$ ladder, reference input of 3.5 to $10 \mathrm{k} \Omega .2$ $=$ bringing ground rail to -300 mV minimizes leakage when operating above $70^{\circ} \mathrm{C} .3=$ contains application resistors for four-quadrant multiplication. $4=$ output is $\pm 3 \mathrm{~V}$ at 1.5 mA ; ac specifications provided (see text). $5=$ output is $\pm 5 \mathrm{~V}$ at 5 mA ; inherently monotonic architecture (see text). $6=$ output is $\pm 10 \mathrm{~V} / 0-10 \mathrm{~V}$ at $5 \mathrm{~mA} .7=$ output is $\pm 3 \mathrm{~V}$ at 8 mA or 0 1 mA ; designed for DSP applications; ac specifications provided. $8=$ output is $\pm 10 \mathrm{~V}, \pm 5 \mathrm{~V}$, $0-10 \mathrm{~V}$, and $0-5 \mathrm{~V}$, all at 5 mA (similar to 5); has Readback and Clear lines. $9=$ A family of volt-age- and current-output DACs. Voltage-output models provide 5 mA at one or more of the following voltages: $\pm 5, \pm 10,0-5$, and $0-10 \mathrm{~V}$. Current-output models provide $0-2 \mathrm{~mA}$ and/or $\pm 1 \mathrm{~mA}$ with a compliance of $\pm 2.5 \mathrm{~V} .10=$ dual voltage-output DAC; each output supplies $\pm 10 \mathrm{~V}$ at $5 \mathrm{~mA} .11=$ single (DSP201) and dual (DSP202) voltage-output DACs for digitalsignal processing; output is $\pm 3 \mathrm{~V}$ at 8 mA ; ac specifications provided. $12=$ reference bandwidth of $1 \mathrm{MHz} .13=$ current output of $\pm 1 \mathrm{~mA}$ or $0-2 \mathrm{~mA}$ with application resistors. $14=$ dual current-output multiplying DAC; reference input is $1.875 \mathrm{k} \Omega( \pm 50 \%)$. $15=$ high-speed, 5 mA current-output DAC with application resistors to provide voltages of $\pm 2.5, \pm 5,0-5$, and $0-10 \mathrm{~V}$; compliance voltage of $\pm 2.5 \mathrm{~V} .16=$ output of $\pm 5 \mathrm{~V}$ and $0-10 \mathrm{~V} .17=\mathrm{R}-2 \mathrm{R}$ reference ladder of $7 \mathrm{k} \Omega( \pm 50 \%)$; uses correction DAC. $18=\mathrm{R}-2 \mathrm{R}$ reference ladder of $4.2 \mathrm{k} \Omega$ ( $\pm 50 \%$ ); uses correction DAC; total unadjusted error specified at $0.02 \% .19=R-2 R$ reference ladder of $1 \mathrm{k} \Omega$ to $10 \mathrm{k} \Omega .20=$ designed for closed-loop servo systems; monotonic to 15
bits around zero. $21=$ hybrid, user-trimmable to 18 -bit accuracy; output voltages at $\pm 5 \mathrm{~mA}$ of $\pm 2.5 \pm 5, \pm 10,0-5$, and $0-10 \mathrm{~V} .22=$ high-speed, hybrid, 4 - or $\pm 2-\mathrm{mA}$ (t) current-output DAC with application resistors to provide voltages of $\pm 10, \pm 5,0-5$, and $0-10 \mathrm{~V}$; compliance voltage of $\pm 1 \mathrm{~V} .23=$ voltage-output $( \pm 10-\mathrm{V})$ hybrid DAC containing two 8 -bit DACs to adjust gain and offset errors to within $\pm 1 / 2$ LSB. $24=$ voltage-output ( $\pm 5$-, $\pm 10$-, +5 and $+10-\mathrm{V}$ ) hybrid DAC. $70=$ dual outputs each providing nominally $\pm 3 \mathrm{~V}$ at $\pm 20 \mathrm{~mA}$.

Digital Interface: $25=$ double-buffered, 14 bits, in 2 bytes ( 8 bits +6 bits). $26=$ doublebuffered, 14 bits, parallel, or 2 bytes ( 8 bits +6 bits). $27=$ double-buffered, 14 bits, parallel. $28=$ double-buffered 14 bits, parallel or serial. $29=$ double-buffered, 16 bits, parallel, or 2 bytes ( 8 bits +8 bits). $30=$ double-buffered, 16 bits, parallel. $31=16$ bits, serial. $32=$ unbuffered (no input latches), 16 bits, parallel. $33=$ double-buffered, 16 bits in two 8 -bit bytes, or serial. $34=$ double-buffered to either of two DACs in two 8 -bit bytes. $35=14$ bits, parallel, no latches. $36=$ single-buffered, 16 bits, parallel, or two 8 -bit bytes. $37=$ Clear command sets registers to all zeros. $38=$ Readback command permits host to check digital word in registers. $39=$ unbuffered, 18 bits, parallel. $60=$ single-buffered, 16 bits, parallel. $61=$ single-buffered, 16 bits, parallel; 8 -bit DACs also single-buffered. $62=$ single-buffered, 18 bits, parallel, or in two 9-bit bytes. $63=$ separate serial interface for each of two DACs. 64 $=16 / 18$ bits, serial. $65=$ single-buffered, 18 bits, parallel.

Packages: $40=20$-pin DIP. $41=20-$ pin PLCC. $42=28$-pin LCC. $43=28$-pin DIP. $44=28$ pin PLCC. $45=24$-pin DIP. $46=28$-pin SOIC. $47=16$-pin DIP. $48=28$-pin double DIP. 49 $=24$-pin double DIP. $50=24$-pin SOIC. $51=20$-pin SOIC. $52=22$-pin DIP. $53=32$-pin DIP. $54=24$-pin SOIC. $55=40$-pin double DIP. $56=32$-pin triple DIP.

## ELEGTRONIC DESIGN REPORT <br> HGHH-RESOLUTION DACs

the ideal output of 0 V when the input code representing half scale is loaded into the DAC's input register. It's expressed in millivolts and is measured with half-scale output signal levels.

Most humans will be unable to hear any difference between CD players using either 16 - or 18 -bit DACs (listed in the table) that provide -92 dB of THD +N at full output, an SNR of 100 dB , and a dynamic range of 93 dB , and a CD player using DACs with superior performance. The higher-performance DACs are for the world's "golden ears," and professional studio digi-tal-audio equipment that must always be better than what the CDs will be played on. These DACs also aim at a wide variety of general-purpose applications, particularly in dig-ital-signal processing.

Different high-resolution IC DAC architectures offer different tradeoffs. For example, while the THD + N and dynamic-range specifications for Crystal's delta-sigma CS4328 dual DAC aren't quite up to those of most other 18 -bit DACs or any of the 20-bit ICs, no other DACs can touch its SNR. And channel separation is low on the CS4328's two DACs. While the conventional DACs also appear to offer an advantage in power requirements, an advantage that's important in portable applications, their power needs don't reflect exactly what's required by the input interpolating filter or the output ana$\log$ filter.

All other things being equal, the CS4328 offers a distinct advantage when it comes to pc-board space. Complete unto itself, it needs neither a digital oversampling filter on the input nor an analog filter on the output. Its two outputs are ready to put $\pm 1.9 \mathrm{~V}$ of audio across $600 \Omega$.

Other suppliers of one-bit (deltasigma) DACs include Philips/Signetics and Sony. Sony's two-channel delta-sigma DAC, the CXD2558, has no analog output filter. Each channel provides the train of precision ones and zeros from the one-bit DAC in differential form-that is, two outputs per channel, one going high and the other low. The user-added analog
filter determines ultimate system performance. Crystal will soon announce a similar device (the CS4303), which is essentially the front end of its CS4328. With the proper filter, it expects to raise dynamic range to well over 103 dB . The DACs in the Phillips/Signetics chip set, while containing a switched-capacitor ana$\log$ filter, still require an external continuous-time filter.
For the most part, overall DAC performance rises with increasing resolution and oversampling (Table 1, again). And, of course, so does price. However, there are some exceptions to the rule, like BurrBrown's 16-bit PCM60 and PCM66 compared with the 18-bit PCM67, and Analog Devices' 16-bit AD1866 compared with the 18 -bit AD1868. These devices, aimed at portable, automotive, and CD-player applications, must necessarily use low power by operating from single 5 -V supplies and dissipating less than 100 mW , sacrificing some performance. These DACs include circuits that create a zero signal at 2.5 V . In addition, the high oversampling factors move the handling of precision analog signals to several hundred kilohertz, and speed takes power.

## Back To Basics

Not long ago, vector-scan CRT displays, such as those used for air-traffic control, and DACs in high-resolution successive-approximation-register (SAR) hybrid ADCs, represented two of the three major applications for high-resolution DACs. Raster-scan displays using higher-speed 8- or 10-bit video DACs have now virtually replaced highresolution DACs in CRT displays. And high-speed, high-resolution ADCs, including the DAC if a successive approximation design, have been integrated into one IC. However, the third major application, com-puter-directed control systems, still exists and is growing. In these systems, the DAC provides the set point for open- and closed-loop control and/or acts as the vital feedback element in a closed-loop system.

Signal synthesis of arbitrary waveforms from ultra-pure sine









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## NEW DIC ARGHITEGTURES AND NOISE SHIPING

Midscale error, the error at or near zero signal level, represents a major cause of distortion in multibit DACs, particularly at low signal levels and in the higherresolution DACs, where other sources of error have been reduced. It's caused by the most-sig-nificant-bit transition that occurs at midscale as the input code switches between a code of 1 and all 0 s , and a code of 0 and all 1 s . To attack the problem, Analog Devices added a digital offset circuit in its 20-bit AD1862, which shifts creation of the midscale output away from the most significant bit. To minimize until-now-sec-ond-order errors, which at 20 bits of resolution become first-order errors at least to the "golden ears" of music, Analog Devices limited the AD1862 to one channel of current output. The user must add an op amp of choice, which can of course be part of the still-mandatory analog filter.

For their 20 -bit PCM63P DAC, Burr-Brown created a completely new, multibit DAC architecture to beat the midscale problem (Fig. 1). Dubbed "Colinear," the PCM63P, like the AD1862, contains just a single-channel, cur-

rent-output DAC. The circuit represents a form of sign-magnitude architecture. It uses a pair of 19bit current DACs, one providing positive currents and the other negative currents. The DACs are summed to form the output current. Only the least-significant-bit current changes at zero. Transparent logic circuitry between the input shift register and the DACs converts the input code to the sign-magnitude code (on-chip reference circuits aren't shown). Future DACs based on this architecture may raise the performance of general-purpose DACs above 14 to 16 bits of resolution at de and over temperature.

The buzz word today in digitalaudio DAC circles is the one-bit DAC, such as Crystal's CS4328
delta-sigma IC (Fig. 2). This twochannel DAC is complete with its own pair of 8 X -oversampling input filters, which are followed by 64X-oversampling digital deltasigma modulators. The modulators drive 1 -bit switched-capacitor DACs that are followed by on-chip low-pass filters and output amplifiers. The on-chip 8X input-interpolation filters do the same job as the off-chip filters used with multibit DACs. They remove the images of the input signal that are present at multiples of the input sampling frequency, $f_{s}$ (the frequency at which the original music signal was sampled), or 44.1 kHz (Fig. 2a).
The signal at the filters' output has a frequency spectrum with images at multiples of $8 \mathrm{f}_{\mathrm{s}}$ (Fig.


8 X interpolated-data spectrum

(a)


Delta-sigma modulator output spectrum
(d)


Spectrum after continuous-time filter


Spectrum after sample-and-hold amplifier Spectrum after switched-capacitor filter

(g)

2b). The filters drive a digital sam-ple-and-hold stage in which the data points from the interpolator are held for eight clock cycles, creating a $64 \mathrm{f}_{\mathrm{s}}$ data stream carrying $a \sin x / x$ frequency response with zeros at multiples of $8 f_{s}$. The $\sin x /$ x zeros completely attenuate signals at $8 \mathrm{f}_{\mathrm{s}}$ and largely suppress the energy remaining in the images (Fig. 2C).

The digital delta-sigma modulator modulates the digital 18 -bit audio data, creating a 1 -bit $64 \mathrm{f}_{\mathrm{s}}$ signal, followed by a 5th-order noise shaper. The shaper moves the quantization noise created in the oversampling process beyond the band of interest (Fig. 2d). The modulator's output drives the 1bit DAC that translates the bit stream into a series of charge packets.

The magnitude of the charge in each packet is determined by sampling (switching) a precision voltage reference onto a capacitor. The polarity of each packet's charge is controlled by the 1 -bit signal, and is a positive charge for a 1 , and a negative charge for a 0 . A string of alternating 1 s and 0 s results in 0 V out. Midscale (zero) error is nonexistent or is a function of the circuits that follow the DAC.

The final stage of the DAC consists of a 5th-order switched-capacitor, analog, low-pass filter, followed by a 2 nd-order, continu-ous-time analog low-pass filter. The 5th-order filter eliminates out-of-band signal energy resulting from the noise-shaping process (Fig. 2e).

The filter scales with the master clock driving the digital circuits, permitting operation at different clock rates. The 2 nd-order filter eliminates high-frequency energy at multiples of the $64 \mathrm{f}_{\mathrm{s}}$ sample rate (Fig. 2f). Together, the digital and analog filters compensate for each other's phase errors, resulting in a phase error (simulated) of zero (Fig. 2 g ).
waves represents a fourth and growing class of high-resolution DAC applications. Moreover, while controlsystem bandwidths are relatively low, waveform-generation frequencies can run from de (programmable power supplies) to whatever maximum update rate is available in a DAC. TriQuint Semiconductor is working on a 14 -bit $2-\mathrm{GHz}$ DAC. One new general-purpose DAC application that's coming on-stream is to use the DAC as the output device for a DSP circuit. DSP applications need bandwidths from de to the maximum signal frequencies the digital-signal processors can handle.

Each of these applications demands maximum performance for several specifications. DACs for control systems must guarantee monotonicity to a certain number of bits over their operating-temperature range. A system (or device) is monotonic if the magnitude of its output remains constant, or increases in value, as the input increases in magnitude. Thus, a DAC is monotonic if its analog outputnever decreases in value when its digital input code increases in value, and vice versa. To put it another way, a monotonic system's output is always a single-val-
ued function of the input. The derivative of a DAC's transfer function must never change sign.
Monotonicity is mandatory if the DAC is in the feedback loop of a control system. If the error signal from the processor says go left or put on more heat, but the DAC output says go right or cuts the heat, the system becomes unstable.

If you can settle for operation at a temperature of or close to $25^{\circ} \mathrm{C}$, you have over a dozen DACs that can provide 16 -bit monotonicity. You can even get 18 -bit monotonicity, albeit from more-expensive hybrid chip-and-wire types (Table 2, again). And you can get monolithic 16 -bit ICs for under $\$ 20$. However, if your control system must use the commercial temperature range, your choice of affordable DACs drops in half.

## Migrating DACs

There's hope, however, for future migration from the audio-DAC arena. One-bit (delta-sigma) DACs are inherently monotonic, as is BurrBrown's PCM63 sign-magnitude DAC. Presently available delta-sigma DACs don't lend themselves to anything but the slowest control systems (those with, say, sub-one-hertz


## COWPAGT-DISE PLAYERS, DIGITAL-AUDIO DAGS, AND OUERSAWPIDG

A$t$ the heart of every com-pact-disc player lies either one or two 16-bit (or more) digital-to-analog converters (DACs). First-generation systems took a 16 -bit parallel word from the digital error-correction circuitry at 44.1 kHz , and applied it to a 16 -bit DAC (see the figure, top). The DAC alternately produces samples of analog voltages representing the left- and right-channel audio signal. The analog signals are applied to a pair of sample-and-hold amplifiers (deglitchers). While one amplifier samples the left channel, the other applies its previously sampled, now-held, output to an analog, low-pass filter.
The low-pass filter removes all unwanted frequency components (images) caused by the initial sampling of the signal prior to recording, and those caused by the discrete nature of the DAC output. The filter must combine a flat amplitude response with linear phase from de to 20 kHz . But it mustalso have deep attenuation ( 100 dB ) above 24 kHz . Such so-called "brick-wall" filters aren't only large and expensive because they require as many as 9 to 13 poles, but their phase response is nonlinear, which can disturb the pulselike transients in music.

To answer the filter problem, system designers added a digital circuit called an oversampling, or interpolation, filter between the digital-signal-processor output and the DAC input. The first filters, which were used with paral-lel-input DACs like the BurrBrown PCM53, multiplied the sampling frequency by two ( 2 X oversampling), resulting in an $88.2-\mathrm{kHz}$ data rate. The first images now start to appear at about 68 kHz , but the audio frequencies of interest still stop at 20 kHz . A much simpler filter can now be used in these systems.

It became clear that one serial data line was easier to handle than

16 , and 18 -bit systems were being developed. So designers asked Burr-Brown to put a serial-to-parallel converter in the DAC, resulting in a third-generation system with an oversampling filter (see the figure, bottom). If 2 X oversampling is good at simplifying the analog filter, $4 \mathrm{X}, 8 \mathrm{X}$, or 16 X oversampling is even better. Even just 4X oversampling pushes the first images out to 156 kHz and the sampling rate to 176.4 kHz . Now, filters with just 3 to 5 poles can do the trick.

Why the move to 18 - and even 20 -bit digital-audio DACs when the basic music is initially sampled and quantized with 16 -bit resolution? It's not for CD-player marketing hype. Rather, higherresolution DACs are needed to re-
duce truncation noise, which is added to the audio passband during the oversampling process by digital filters. Digital filters perform multiply-accumulate operations in which two 16 -bit binary numbers are multiplied by each other. The answer can run over 40 bits, which takes lots of silicon. Of more importance, to preserve true signal purity a fast 40 -bit DAC is required, which is impossible even to conceive, let alone build. As a result, the latest interpolators round off, or truncate, the accumulation, producing a choice of "practical" 16 -, 18 - and 20 -bit output words. The system designer can choose which to use, knowing that at least theoretically, the higher the resolution, the better the music will sound.


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bandwidths) due to the delay in their filters.

However, future devices may be able to lick this problem by using new filter designs analogous to the way the filters were changed in del-ta-sigma ADCs to permit multiplex-
ing their inputs. Control systems using conventional DACs add some low-pass filtering to the DAC outputs withoutaffecting system stability. Of course, the first audio DACs were 16 -bit general-purpose data converters.

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While no longer reflected in audioDAC specifications, monotonicity, particularly at midscale (zero), impacts audio characteristics. However, gain and offset errors are less important. For example, a typical audio DAC might have a gain error of 0.5 $d B$ (that's $5 \%$ ), which would be totally unacceptable in most general-purpose applications. However, some brave industrial-system designers are doing their own migration, using present low-cost 16 -bit audio DACs in lieu of 12 -bit general-purpose types.

## Controlled Temperatures

The audio DAC works best in a temperature-controlled environment, where it's generally higher, unspecified and untested gain and offset drift can be tolerated. And the designer must learn to live with the serial input and $\pm 3$-V output. On the other hand, all of the latest audio DACs work off $\pm 5$-V rails. And lowpower (under 100 mW ) devices are available for battery-powered instrumentation. Furthermore, you can get a pair of IC audio DACs in a 16 -pin SOIC package for just $\$ 10$. But these DACs also need a low-jitter high-frequency clock, something not always available in an instrumentation system.

Several low-cost 16 - and 18 -bit audio DACs already represent the migration path to industrial applications. Analog Devices' AD669 and AD766, and Burr-Brown's DSP201 and DSP202 are some examples. The last three aim at DSP and frequencysynthesis applications. Their serial inputs and ac specifications show their audio heritage. Even the AD669, which is designed for paral-lel-input signals, can handle update rates up to 500 kHz and produce lowdistortion sine waves well beyond the audio band, according to Analog Devices.

Integral linearity, or relative accuracy, along with gain and offset errors, are of secondary importance in control systems. While they do determine the system's absolute accuracy in set-point applications, errors in both set-point and feedback applications can be calibrated out. Gain and


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offset can be trimmed as well. Obviously, if system calibration isn't used, these errors must be considered. In feedback loops, gain and integral linearity errors have significantly less effect while resolution and monotonicity are all important, because the system is homing in on a set point.

## Glitching Guitches

Each of the many waveform-synthesis applications have their own sets of critical specifications. As frequencies rise, glitches become more important.

In the past, sample-and-hold amplifiers on the output, called deglitchers, eliminated the effects of skew on the arrival of data bits, particularly at the major carry. However, today's low-glitch DACs load all of the bits into a register as they arrive, and then strobe them all into the DAC in a few nanoseconds.

As synthesis moves to the generation of RF signals, the spurious-free dynamic range (SFDR) specification becomes the prime parameter. You don't want any spurious frequencies (spurs) generated above some minimum level.

According to TriQuint Semiconductor, their 14-bit GaAs DACs show an SFDR of about 72 dB . If you're looking for high-speed high-resolution voltage- or current-output DACs for any purpose, the pickings are pretty slim. Just three DACs are available: Analog Devices' voltageoutput AD766, SPT's current-output HDAC52160, and Sipex's currentoutput HS9390, a $\$ 184$ hybrid.

Multiple DACs per die are also beginning to appear, with 16 -bit dual units coming from Burr-Brown and Sipex. However, none are 16-bit monotonic over temperature. On the other hand, Micro Power Systems will soon be offering a pair of octal 14-bit voltage-output DACs, one with a serial I/O and the other with a parallel I/O. $\square$

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# 0p Amps Expand VOLtage Reference Options 

## Bootstrap Feedback Adds Polarity And Magnitude Options To Conventional Dc-Voltage References.

## JERALD GRAEME

Burr-Brown Corp., P. O. Box 11400, Tucson, AZ 85734; (602) 746-7412.


1. A CONVENTIONAL INVERTING AMPLIFIER reverses the polarity of a reference voltage, but adds resistor errors to the result.

ecause dc-voltage references predominately supply positive, fixed voltages, engineers must build specialized opamp circuits to add voltage-polarity and magnitude options beyond those provided by conventional circuits. That's where bootstrap techniques come into play. With bootstrap feedback, designers can create every possible combination of reference-voltage magnitude and polarity. Basically, applying this feedback inverts the reference voltage without introducing errors from any gainsetting resistors.

Generally speaking, the bootstrap technique produces reference circuits with dual voltage outputs. However, in contrast with conventional options, bootstrapping doesn't restrict either output magnitude to that of the original voltage reference. And any polarity combination is available for the two bootstrap outputs. In other words, the two output polarities can be the same or opposite, relative to each other, and the same or opposite relative to the original reference voltage.

Together, the magnitude and polarity degrees of freedom produce various voltage combinations not possible with conventional circuits. Bootstrapping options include an inverted output without resistor errors, inverted polarity for both circuit outputs, and a noninverting output with gain magnitude less than unity. In addition, a variable-output circuit delivers a voltage control that spans all magnitude and polarity combinations.

Consider first the inversion of reference-voltage polarity. Although most available voltage references supply positive voltages, negative references are also widely needed. A simple approach to the problem uses an inverting amplifier to reverse polarity (Fig. 1). The inverter converts the $\mathrm{V}_{\mathrm{R}}$ output of the voltage reference to a new reference voltage of $-\mathrm{R}_{2} \mathrm{~V}_{\mathrm{R}} / \mathrm{R}_{1}$. Resistor selection provides magnitude control along with the polarity inversion. However, the inverter adds resistor errors that can degrade the voltage accuracy.

In truth, reference, amplifier, and resistor errors all affect the accuracy of the inverted voltage. The initial tolerance of reference voltage $V_{R}$ transfers directly to the circuit output in a relative sense. The relative or percentage error of voltage $V_{R}$ produces the same percentage error in the output of $-R_{2} V_{R} / R_{1}$. For the REF10K reference voltage shown, the voltage tolerance error is 5 mV or $0.05 \%$ of the nominal $10-\mathrm{V}$ output. Output effects of amplifier input errors depend on the resistor values used. Together, the amplifier input offset voltage, $\mathrm{V}_{\mathrm{OS}}$, and input bias current, $\mathrm{I}_{\mathrm{B}}$, produce an output error of $\left(1+R_{2} / R_{1}\right) V_{\text {OS }}+I_{B} R_{2}$. For the

# VOLTAGE REFERENCE OPTIONS 

OPA77G and the resistors shown, this error is $128 \mu \mathrm{~V}$ or about $0.0013 \%$ of the $-10-\mathrm{V}$ output.
Resistor tolerance errors directly affect the output voltage through the $-\mathrm{R}_{2} / \mathrm{R}_{1}$ circuit gain. Two $0.1 \%$ resistors produce as much as $0.2 \%$ output error. This overshadows the $0.05 \%$ and $0.0013 \%$ errors of the reference and the op amp. Worst-case output error totals $0.25 \%$ or 25 mV for the $10-\mathrm{V}$ output shown. Obviously, a better approach is needed.
To preserve reference-voltage accuracy, bootstrap feedback inverts the voltage polarity without gainsetting resistors. The basic bootstrap circuit includes phase compensation elements $\mathrm{R}_{\mathrm{C}}$ and $\mathrm{C}_{\mathrm{C}}$ (Fig. 2). However, these elements are ignored for the basic dc function of the circuit: capacitor $\mathrm{C}_{\mathrm{C}}$ has no dc effect and $\mathrm{R}_{\mathrm{C}}$ produces only a small de voltage with the amplifier input current. Bootstrap feedback drives the common return terminal of the voltage reference. The voltage-reference output follows this drive to control the op amp's inverting input.
The voltage reference's connection places it in the amplifier feedback path where feedback forces the two op-amp inputs to the

2. A B00TSTRAP AMPLIFIER inverts reference
voltage polarity without the error of gain-setting resistors.
output with unity gain. The previous inverting amplifier multiplies $\mathrm{V}_{0 S}$ by a gain of $1+R_{2} / R_{1}$. In addition, the bootstrap inverter also removes output loading effects from the voltagereference output. This output no longer supplies load currents, and its output resistance won't produce a loading-error voltage. Instead, the op amp supplies the load currents from an output resistance reduced by the amplifier's high dc gain.
In practice, the bootstrap amplifier adds some error in the referencevoltage inversion. However, amplifier selection controls this error to be much less than the error of the voltage reference itself. The voltage tolerance error of the REF10K again offsets the ideal $-10-\mathrm{V}$ output by 5
ultimate trimmed accuracy. Because temperature variations in the normal application environment react with the circuit's drift sources, the trimmed result is only as dependable as its stability in this environment.

Thermal drifts affect the voltage reference, the op amp, and any gainsetting resistors used. The REF10K voltage reference drifts $1 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$, or $10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$. Careful op-amp selection avoids adding to the drift. Drift from the amplifier's dc errors adds directly to the circuit output. For the conventional inverter, the dc error is (1 $\left.+R_{2} / R_{1}\right) V_{\text {OS }}+I_{B} R_{2}$. The components in Figure 1 make the associated output drift $3 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$. For the bootstrap inverter, the drift of error $\mathrm{V}_{\mathrm{OS}}+$ $\mathrm{I}_{\mathrm{B}} \mathrm{R}_{\mathrm{C}}$ is $1.2 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$. No gain-setting re$\mathrm{I}_{\mathrm{B}} \mathrm{R}_{\mathrm{C}} 1.2 \mu$ sistors add to this invertsistors add to this invert-
er's drift, so the worstcase total drift is just 11.2 $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$, or $1.12 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$.

However, with the conventional inverter, two resistor temperature coefficients add to the output drift. There, two $0.1 \%$ wirewound resistors typically dominate drift effects with a combined drift as high as $30 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$. Worst-case total drift for this circuit is then $31.3 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$. For a $\pm 5^{\circ} \mathrm{C}$ environment, the bootstrap circuit limits trimmed accuracy to 5.5 ppm, while the convention-
mV . Amplifier dc-input errors add to this by an amount $V_{\text {OS }}+I_{B} R_{C}$. With the OPA77G shown in Figure 2, $\mathrm{V}_{\text {OS }}$ $=0.1 \mathrm{mV}$, or $1 / 50$ of the initial reference error. Moreover, the amplifier draws an input current of $\mathrm{I}_{\mathrm{B}}=2.8 \mathrm{nA}$ through the $1-k \Omega$ resistor $R_{C}$. This develops a negligible 0.0028 mV of dc error. Eliminating the error guides the selection of the $R_{C}$ value. A worst-case combination of the reference and amplifier errors predicts a $5.1-\mathrm{mV}$ output error, much less than the 25 mV encountered with the conventional inverting amplifier.

In both the conventional inverter and the bootstrap circuit, trimming the voltage reference removes the initial error of the polarity inversion. However, thermal drifts define the
al inverter restricts this accuracy to around 160 ppm .

The amplifier selected in the preceding analysis didn't introduce any major dc errors. However, to retain this condition, the op amp's offset control shouldn't be used to remove output error because the offset control also affects the amplifier's offset drift. In other words, using the control to null the amplifier's own offset error results in little drift effect, but using the amplifier's offset control to null other circuit errors introduces significant amplifier drift.

The bootstrap inverter obtains reduced dc error at the price of added phase compensation. In Figure 2, the voltage reference adds a feedback pole to one that's already present

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## DESICN APPICATIONS <br> VOLTAGE Reference OPTIONS

from the op amp. Ideally, the voltage reference $V_{R}$ supplies a unity-feedback factor for the opamp and transfers any amplifier-output change directly to the amplifier input. In practice, a phase shift through $V_{R}$ delays this transfer at higher frequencies. It also adds to the amplifier's phase shift, increasing net phase shift in the feedback loop that can cause oscillation.
To ensure frequency stability, the phase compensation bypasses the phase shift of $V_{R}$ at higher frequencies. Phase-compensation elements $\mathrm{R}_{\mathrm{C}}$ and $\mathrm{C}_{\mathrm{C}}$ shown in Figure 2 decouple the op amp from the feedback of the voltage reference. At higher frequencies, resistor $\mathrm{R}_{\mathrm{C}}$ blocks the volt-age-reference output with the bypass effect of capacitor $\mathrm{C}_{\mathrm{C}}$. The common node of these two elements is the op amp's feedback input. Control of this input shifts with frequency. At low frequencies, $\mathrm{C}_{\mathrm{C}}$ presents a high impedance and offers little feedback signal to the feedback input. Then, feedback through the voltage reference prevails and sets the level of that input. At higher frequencies, the impedance of $\mathrm{C}_{\mathrm{C}}$ becomes less than that of $\mathrm{R}_{\mathrm{C}}$, and the capacitor assumes control of the op amp's feedback. There, $\mathrm{C}_{\mathrm{C}}$ delivers direct feedback between the amplifier's output and the feedback input. This bypasses the phase shift of the $\mathrm{V}_{\mathrm{R}}$ feedback and the op amp alone controls feedback phase shift.
$\mathrm{R}_{\mathrm{C}}$ and $\mathrm{C}_{\mathrm{C}}$ set the transition between the two feedback control paths. Optimum settling time results when the break frequency of these elements is set well below the dominant response pole of the reference. Unfortunately, voltage reference data sheets don't specify this pole frequency, and empirical selection sets the phase compensation break frequency. First, $\mathrm{R}_{\mathrm{C}}$ is chosen to limit the dc error created with the flow of the amplifier's input current. Then, $\mathrm{C}_{\mathrm{C}}$ is selected using a square-wave-output load current. The output voltage response to the load guides the selection of $\mathrm{C}_{\mathrm{C}}$ for optimum settling time.

A second bootstrap circuit provides an inverted reference polarity
and includes a second, noninverting output. The only difference between this circuit and Figure 2 is an added feedback voltage divider (Fig. 3). The op amp's output again drives the common terminal of the voltage reference to shift the reference output relative to ground. Once again, the voltage reference's output drives the op-amp input, but now through a feedback divider.

The additional voltage divider restores the voltage reference output as a useful reference source. The bootstrap amplifier had previously forced the voltage reference output to zero. With the feedback divider, the zero-voltage condition shifts to the voltage-divider junction. To zero this junction, the feedback develops voltages on both of the divider resistors, and the sum of these two voltages equals the original reference voltage $V_{R}$. The voltage divider connects the output and the common terminals of the voltage reference. $\mathrm{V}_{\mathrm{R}}$ divides between the two resistors according to their relative resistances. The equal-valued resistors in Figure 3 support equal voltages of $\mathrm{V}_{\mathrm{R}} / 2$.

Relative to ground, the two resistor voltages present opposite-polarity output voltages in $V_{01}$ and $V_{02}$. Zero voltage resides at the junction of the resistors. One resistor's voltage rises above ground, while the other drops below. This sets the op amp's output at a level of $V_{02}=-V_{R} /$ 2. Then, feedback through the voltage reference produces a second volt-age-reference output of $V_{01}=V_{02}+$ $\mathrm{V}_{\mathrm{R}}=\mathrm{V}_{\mathrm{R}} / 2$. Thus, the circuit supplies equal and opposite reference voltages with magnitudes equal to one-half the original reference voltage. Digi-tal-to-analog converters employ this reference-voltage combination by having one polarity
supply the basic reference requirement, and the opposite polarity serve the bipolar-offset function.

Errors in Figure 3's reference outputs follow from Figure 2, and are combined with the additional error effects of the feedback divider. Tolerance error of the initial reference voltage $V_{R}$ divides equally between the two circuit outputs through the equal resistors of the divider. Thus, the two outputs tend to track with respect to this error, which benefits the DAC application already mentioned. For the REF101J shown in Figure 3, a $5-\mathrm{mV}$ tolerance error alters the circuit's ideal $10-\mathrm{V}$ output by $0.05 \%$. The same percentage error transfers to $V_{01}$ and $V_{02}$, because $V_{R}$ is a direct multiplier in the related output expressions.
Amplifier input errors also affect the two circuit outputs equally. Offset voltage $V_{\text {OS }}$ directly shifts the voltage divider junction away from 0 V. No change results in the resistor voltages, but the junction shift moves the two circuit outputs relative to ground. Both outputs move an amount equal to $\mathrm{V}_{\text {os. }}$. Input bias current $\mathrm{I}_{\mathrm{B}}$ shifts the outputs through associated voltage drops on the feedback resistors. With equal-valued resistors, one-half of $I_{B}$ flows in each resistor to shift the two outputs by an amount equaling $I_{B} R / 2$. The net

3. B00TSTRAPPING AND a voltage divider split a reference voltage into two output voltages of opposite polarity.
error is then $V_{\text {OS }}+I_{B} R / 2$ for both outputs. With the OPA177G and resistor values given in Figure 3, net error is $64 \mu \mathrm{~V}$, or about $0.0013 \%$ of the 5 -V outputs.

The dominant error in Figure 3 results from the resistors added by the feedback divider. The divider resistors introduce errors like those described for the inverter in Figure 1. Wirewound $0.1 \%$ resistors increase the initial errors in $V_{01}$ and $V_{02}$ by as much as $0.2 \%$, or four times the above $\mathrm{V}_{\mathrm{R}}$ tolerance error.

Circuit trim removes the net output errors within the limit imposed by thermal drifts. First, trimming the voltage reference adjusts the difference between $V_{01}$ and $V_{02}$ so that it's equal to the ideal value of $V_{R}$. Then, resistor trimming sets a monitored circuit output to its ideal value. Either circuit output can be monitored because the resistor trim actually adjusts both outputs to their ideal values after the first trim adjusts the difference between the two voltages. The second trim, which merely modifies the two voltages so they're relative to ground, compensates for errors due to both the resistors and the amplifier offset. The most convenient resistor trim is obtained with a potentiometer inserted between the two resistors. In this case, the potentiometer wiper rather than the resistor junction connects to the op-amp input.

Trimmed accuracy in Figure 3 depends upon the temperature coefficients of the circuit components. The REF101J's output drifts $3 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$, and this relative sensitivity transfers directly to the two circuit outputs. Op-amp-induced errors of $\mathrm{V}_{\mathrm{OS}}$ $+\mathrm{I}_{\mathrm{B}} \mathrm{R} / 2$ also contribute output drifts. The $0.7-\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ drift of $V_{O S}$ and $60-\mathrm{pA} /{ }^{\circ} \mathrm{C}$ drift of $\mathrm{I}_{\mathrm{B}}$ produce $1.3-\mu \mathrm{V} /$ ${ }^{\circ} \mathrm{C}$ output drifts for the $10-\mathrm{k} \Omega$ resistors. This drift component translates to a relative sensitivity of $0.26 \mathrm{ppm} /$ ${ }^{\circ} \mathrm{C}$. Net drift effect of the two circuit outputs is then $3.26 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$.

4. MAGNITUDE CONTROL without polarity reversal for $V_{0} \geq V_{R}$ can be supplied by variable-gain noninverting amplifiers.

Drift effect remains small compared to that produced by typical resistor drift. Resistor drift alters the division of voltage $\mathrm{V}_{\mathrm{R}}$ between the two circuit outputs. Typical $0.1 \%$ wirewound resistors drift $15 \mathrm{ppm} /$ ${ }^{\circ} \mathrm{C}$, or about five times that of the other components previously mentioned. Combined, the worst-case drift error of the components limits trimmed accuracy to around $0.09 \%$ in $\mathrm{a} \pm 5^{\circ} \mathrm{C}$ environment. A resistor network produces greater precision for the voltage divider. Then, the resistors track with temperature so that their temperature coefficients have canceling effects in the division of voltage $V_{R}$.

Phase compensation for Figure 3 follows from the Figure 2 discussion.

R is selected to limit the quiescent current consumed by the feedback network. Then, $\mathrm{C}_{\mathrm{C}}$ is selected for good output settling time under loadcurrent transients. To simulate the effect of these transients, a squarewave current load is applied to the $\mathrm{V}_{01}$ output. The resulting $\mathrm{V}_{01}$ settling response guides the capacitor selection.

A unique capability occurs in the noninverting output of the Figure 3 configuration. The $\mathrm{V}_{01}$ output presents a voltage of the same polarity as the voltage reference, but with a lesser magnitude. Change of voltage magnitude without changing polarity typically involves noninverting amplifier connections of op amps (Fig. 4). The figure illustrates this case with variable gain (a bootstrap alternative will be presented next). The noninverting amplifier in Figure 4 provides a circuit gain of $1 /(1-x)$, where $x$ is the potentiometer fractional setting. Because 0 $\leq x \leq 1$, this gain is never less than unity. Thus, the circuit constrains the out-put-voltage magnitude to be $V_{0} \geq V_{R}$. Moreover, the $1 /(1-x)$ relationship produces nonlinear gain variation as x varies.

To retain the voltage polarity and reduce magnitude, two inverting amplifiers could be connected in

The compensation decouples the opamp feedback from the high-frequency phase shift of the voltage reference. As before, capacitor $\mathrm{C}_{\mathrm{C}}$ offers a direct high-frequency feedback path for the op amp. At higher frequencies, the impedance of $\mathrm{C}_{\mathrm{C}}$ becomes low compared to that of the feedback resistance, decoupling the feedback through the voltage reference in favor of the direct feedback through $\mathrm{C}_{\mathrm{C}}$. Previously, this decoupling required the addition of an isolating resistance, $\mathrm{R}_{\mathrm{C}}$. However, in this case, the feedback network provides the required resistance.

Selecting the phase-compensation components requires empirical evaluation. First, the value of resistance
series. However, this straightforward approach introduces the errors of two amplifiers and their feedback resistors. Instead, a variable-magnitude circuit serves the reduced voltage requirements by using the bootstrap in Figure 3 (Fig. 5). A potentiometer replaces the previous feedback resistors, and compensation resistor $R_{C}$ is reintroduced. These changes open up a variable-gain option that's also available to the circuits discussed later in the article.

In Figure 5, $\mathrm{V}_{\mathrm{R}}$ remains across the feedback divider now provided by the potentiometer. $\mathrm{V}_{\mathrm{R}}$ divides between the segments of this divider depending on the potentiometer fraction x . At the noninverting $\mathrm{V}_{01}$

## DESIGN APPIICATIONS VOLTAGE REFERENCE OPTIONS


5. A VARIABLE-GAIN bootstrap amplifier provides noninverting gain ( $\mathbf{V}_{0} \leq \mathbf{V}_{\mathrm{R}}$ ) and linear gain control. A potentiometer replaces the previous feedback resistors, and compensation resistor $R_{C}$ is reintroduced.
output, the circuit produces $\mathrm{V}_{01}=$ $\mathrm{xV}_{\mathrm{R}}$. Here, $\mathrm{x} \leq 1$, and the desired magnitude reduction occurs while the polarity of $\mathrm{V}_{01}$ remains the same as that of $\mathrm{V}_{\mathrm{R}}$. Consequently, the circuit produces $\mathrm{V}_{0} \leq$ $\mathrm{V}_{\mathrm{R}}$ without reversing polarity. As a side benefit, the circuit linearizes the variable gain control. Note that $V_{01}$ $=\mathrm{xV}_{\mathrm{R}}$ shows a linear relationship between $x$ and the output voltage.

Figure 5 also retains the second output of Figure 3, $\mathrm{V}_{02}$. This output in-
verts polarity and also provides a gain magnitude below unity. At the second output, $\mathrm{V}_{02}=(\mathrm{x}-1) \mathrm{V}_{\mathrm{R}}$. Because $0 \leq \mathrm{x} \leq 1, \mathrm{~V}_{02}$ supplies a reduced voltage magnitude and a polarity opposite that of $\mathrm{V}_{\mathrm{R}}$. A constraint on the magnitude of $\mathrm{V}_{02}$ results from its relationship to $\mathrm{V}_{01}$. The difference between the two output voltages equals $\mathrm{V}_{\mathrm{R}}$ because the original voltage reference connects between the two circuit outputs. Either $V_{01}$ or $V_{02}$ can be set to any voltage magnitude $\leq V_{R}$, but the other output is then constrained by the requirement $\mathrm{V}_{01}-\mathrm{V}_{02}=\mathrm{V}_{\mathrm{R}}$.

Many application circuits overcome the output constraint through resistor scaling. Connecting a reference voltage to a resistor input acquires an extra degree of freedom from Ohm's Law. The resistor input converts the reference voltage to a current used by the application circuit. The bipolar offsetting of DACs

## Breakthrough multichip modules



# DESIGN APPLICATIONS VOLTAGE REFERENCE OPTIONS 

is one such example. In this case, $\mathrm{V}_{01}$ sets the desired level for the DAC reference voltage, and the opposite polarity $\mathrm{V}_{\mathrm{O} 2}$ supplies the bipolar offsetting. The offsetting $V_{02}$ connects to a resistor for voltage-to-current conversion. Choosing this resistor accommodates the actual voltage of $\mathrm{V}_{02}$. Similar freedom prevails when applying a reference voltage to an op-amp summing resistor.

Output errors for the two reference voltages in Figure 5 generally follow from the discussion on Figure 3. Errors from the voltage reference and op amp repeat with allowance for the potentiometer setting x . The $5-\mathrm{mV}$ tolerance error of the REF101J represents $0.05 \%$ of the reference's output. This 5 mV divides between the two circuit outputs in proportion to their output-voltage magnitudes. As a result, the relative error transferred to the outputs remains $0.05 \%$.

The net effect of amplifier errors
varies with the potentiometer setting. Amplifier input-offset voltage again transfers directly to the two circuit outputs. The offset shifts both outputs by the total amount $\mathrm{V}_{\text {OS }}$, independent of the individual output magnitudes. Amplifier inputbias current reacts with the two segments of the potentiometer, and splits between the segments in inverse proportion to their resistances. Resulting error voltages are in direct proportion to the segment resistances, and the inverse and direct proportionalities produce counteracting effects in the error voltages developed. The two output errors produced are again equal. Both outputs shift by an amount $x(1-x) I_{B} R_{v}$. Thus, the net amplifier error transferred to the two outputs is $\mathrm{V}_{0 S}+\mathrm{x}(1$ $-x) I_{B} R_{v}$. A potentiometer setting of $x=0.5$ maximizes the error. For the OPA177G, the error shifts the outputs by $95 \mu \mathrm{~V}$.

In contrast to the circuit in Figure 3 , no resistance tolerance affects the outputs in Figure 5. The initial reference voltage $V_{R}$ divides between the two potentiometer segments in accordance with the relative segment resistances. The absolute value of the total potentiometer resistance is unimportant. However, the nonlinearity error of the potentiometer control raises a potential new error source because it causes variation in the relationship between output voltage and potentiometer rotation. In most cases, an output voltage monitor guides the potentiometer adjustment and bypasses this nonlinearity error. If not, precision potentiometers offer control nonlinearities as low as $0.1 \%$.

Thermal drift again limits the final accuracy of the circuit outputs. The reference voltage, amplifier offset, and potentiometer each introduce thermal sensitivities that alter the

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trimmed output values. Reference voltage $V_{R}$ from the REF101J introduces a 3 -ppm $/{ }^{\circ} \mathrm{C}$ drift to both outputs. Then, the OPA177G's drift alters the $V_{O S}+x(1-x) I_{B} R_{v}$ outputerrors for additional drifts as large as $1.3 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$. Potentiometer construction inherently limits the effect of its drift. As stated, the actual value of the potentiometer resistance is unimportant, and drift in this resistance doesn't alter the output voltages. Only the difference in drifts of the $x R$ and $(1-x) R$ potentiometer segments affects the circuit outputs. The same material forms both segments, and a $100-\mathrm{ppm} /{ }^{\circ} \mathrm{C}$ potentiometer provides segment drift tracking to within $5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$. Combined, the drift sources limit practical trimmed accuracy to around 40 ppm .
Phase compensation for Figure 5's circuit follows the approach used in Figures 2 and 3 . As with the circuit in Figure $2, \mathrm{R}_{\mathrm{C}}$ and $\mathrm{C}_{\mathrm{C}}$ decouple the opamp feedback from the phase shift of the voltage reference. Figure 3 's circuit adds capacitor $\mathrm{C}_{\mathrm{C}}$ for the phase compensation, but the feedback network provides the resistive portion of the decoupling. With potentiometer feedback, the equivalent feedback resistance varies with the potentiometer setting, and even goes to zero. Then, by adding $\mathrm{R}_{\mathrm{C}}$, a minimum decoupling resistance is set. Once again, choosing a low value for $\mathrm{R}_{\mathrm{C}}$ minimizes the error created with the amplifier-input current. After that, empirical testing defines the optimum value for $\mathrm{C}_{\mathrm{C}}$ as described in Figure 2's discussion.
The circuit in Figure 5 supplies two output reference voltages of opposite polarity. Other polarity relationships result by adding positive feedback. Then, bootstrap circuits supply two outputs of the same polarity, which is either the same as or opposite that of the original reference voltage. In the noninverting version of the positive feedback configuration, the voltage-follower op amp sets the negative feedback of the circuit at unity (Fig. 6). The negative feedback retains circuit stability in the presence of the positive feedback. Positive feedback from the amplifier output travels through the
voltage reference and then through a feedback voltage divider. The divider's output connects to the amplifier noninverting input, defining a positive polarity for the feedback path.
Combined negative and positive feedbacks produce two noninverting reference outputs that overcome two magnitude constraints of conventional solutions. The conventional alternative for a dual-output, noninverting reference

6. CONNECTING THE voltage reference in a positive feedback path produces two noninverting outputs.
simply connects a noninverting amplifier to the volt-age-reference output. However, the first output of this alternative remains that of the reference itself, $\mathrm{V}_{\mathrm{R}}$. In addition, the second output has the magnitude constraint of $V_{0}$ $\geq V_{R}$. Bootstrapping removes both magnitude constraints in the circuit shown in Figure 6.
Here, two circuit gains scale the two output voltages. The feedback divider delivers a fraction of $V_{01}$ to the op amp's noninverting input. Connected as a voltage follower, the op amp transfers this fraction to the amplifier's output. Therefore, $\mathrm{V}_{02}=$ $\mathrm{R}_{2} \mathrm{~V}_{01} /\left(\mathrm{R}_{1}+\mathrm{R}_{2}\right)$. Also, the op amp's output drives the common terminal of the voltage reference to shift its output voltage relative to ground, producing $\mathrm{V}_{\mathrm{O} 1}=\mathrm{V}_{\mathrm{O} 2}+\mathrm{V}_{\mathrm{R}}$. Combining this result with the previous $\mathrm{V}_{02}$ expression defines the output voltages in figure 6 as:
$\mathrm{V}_{01}=\left(1+\mathrm{R}_{2} / \mathrm{R}_{1}\right) \mathrm{V}_{\mathrm{R}}$
$\mathrm{V}_{02}=\left(\mathrm{R}_{2} / \mathrm{R}_{1}\right) \mathrm{V}_{\mathrm{R}}$
Thus, the circuit develops two resis-tor-controlled gains for two distinct output voltages.
Both $V_{01}$ and $V_{02}$ retain the same polarity as the original $V_{R}$. Neither output voltage is constrained to equal $V_{R}$, and $V_{02}$ can have a magnitude greater than or less than $V_{R}$.

The only constraint on the output voltages results from the voltagereference connection between the two circuit outputs. With this connection, the difference between the two output voltages equals $V_{R}$. For the specific resistors shown in Figure 6, the circuit transforms an original $10-\mathrm{V}$ reference into output voltages of 12 V and 2 V .

Accuracy limitations for the circuit in figure 6 parallel those described for previous circuits, but with reduced error from the resistors and increased error from the amplifier offset. The voltage reference introduces static errors and thermal drifts identical to those of the circuit in Figure 5. The associated relative errors directly affect the $V_{R}$ terms of the output expressions for Figure 6. For the REF102A, a $10-$ mV tolerance error in a $10-\mathrm{V}$ output makes the relative tolerance error $0.1 \%$. This $0.1 \%$ tolerance affects both $\mathrm{V}_{01}$ and $\mathrm{V}_{02}$. Similarly, the outputs repeat $\mathrm{V}_{\mathrm{R}}$ 's $10-\mathrm{ppm} /{ }^{\circ} \mathrm{C}$ drift.
The op amp's voltage-follower connection reduces resistor-error effect in only one of the output voltages. Resistor errors produce out-put-voltage deviations through the two gains of the circuit. Although different voltage gains set the circuit's two output voltages, both

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gains depend on the feedback resistors. As stated previously, $\mathrm{V}_{02}=$ $\left(\mathrm{R}_{2} / \mathrm{R}_{1}\right) \mathrm{V}_{\mathrm{R}}$, and the errors of the two resistors directly affect the gain producing this output. Consequently, $0.1 \%$-resistors produce as much as a $0.2 \%$ error in $\mathrm{V}_{02}$, and $15 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ resistor drifts introduce as much as 30 $\mathrm{ppm} /{ }^{\circ} \mathrm{C}$ output drift.
The voltage follower reduces these errors for the other output where $V_{01}=\left(1+R_{2} / R_{1}\right) V_{R}$. The " 1 " term reduces the gain sensitivity to
plifier-input errors. Positive feedback reduces the circuit's net feedback factor, $\beta$. With both negative and positive feedback, the circuit's net feedback factor becomes the difference between the two factors ${ }^{1}$. Op-amp circuits amplify input errors by a gain of $1 / \beta$, so positive feedback increases the resulting output error. ${ }^{2}$ The negative feedback of the voltage follower sets $\beta_{-}=1$, and the positive feedback through the resistors sets $\beta_{+}=\mathrm{R}_{2} /\left(\mathrm{R}_{1}+\mathrm{R}_{2}\right)$. Then,

7. MOVING THE VOLTAGE reference to the negative feedback path produces two inverting outputs. the net feedback factor is $\beta=\beta_{-}-\beta_{+}$ $=1-\mathrm{R}_{2} /\left(\mathrm{R}_{1}+\mathrm{R}_{2}\right)=$ $\mathrm{R}_{1} /\left(\mathrm{R}_{1}+\mathrm{R}_{2}\right)$.
The input errors amplified by $1 / \beta$ include $V_{\text {OS }}$ and the error-voltage effect of $I_{B}$. Amplifi-er-input current $I_{B}$ reacts with the parallel combination of $\mathrm{R}_{1}$ and $\mathrm{R}_{2}$ to develop a second component of input-offset voltage. Net amplifier input-offset error is then $V_{0 S}+$ $\mathrm{I}_{\mathrm{B}} \mathrm{R}_{1} \mid \mathrm{R}_{2}$. Thus, the amplifier input errors produce output offsets of ( $V_{\text {os }}$ $\left.+\mathrm{I}_{\mathrm{B}} \mathrm{R}_{1} \mid \mathrm{R}_{2}\right) / \beta=$ $\mathrm{V}_{\text {oS }} / \beta+\mathrm{I}_{\mathrm{B}} \mathrm{R}_{2}$. This offset shifts both circuit-output voltages by the full offset amount. With the components shown in Figure 6,
$R_{1}$ and $R_{2}$. Resistor errors only affect the $R_{2} / R_{1}$ portion of the gain, and this portion is the fraction $\mathrm{R}_{2} /\left(\mathrm{R}_{1}+\right.$ $\mathrm{R}_{2}$ ) of the total gain. For the specific resistors shown in Figure 6, this fraction is $1 / 6$. A $0.2 \%$ total resistor error produces a $0.033 \%$ error in $\mathrm{V}_{01}$, and a total resistor drift of $30 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ produces a $5-\mathrm{ppm} /{ }^{\circ} \mathrm{C}$ output drift. The error-reducing " 1 " term results from bootstrap feedback through a voltage follower. The follower needs no error-producing resistors to set the amplifier's unity gain.

However, the positive feedback of Figure 6 increases the effect of am-
ming the voltage reference sets $\mathrm{V}_{01}$ $-V_{02}$ at the ideal value of $V_{R}$. Then, resistor trimming sets $\mathrm{V}_{\mathrm{O2} 2}$ at its ideal value relative to ground. Here, the $\mathrm{V}_{02}$ output serves as the trim monitor because of this output's greater gain sensitivity to resistor value. As mentioned earlier, this sensitivity reduces for $\mathrm{V}_{01}$. However, the trim of $\mathrm{V}_{02}$ automatically adjusts $\mathrm{V}_{01}$ as well, because the previous trim sets the difference between the two voltages. Following these trims, the thermal drifts set the practical trimmed accuracy in Figure 6 at $0.02 \%$ for $\mathrm{V}_{02}$ and $0.008 \%$ for $\mathrm{V}_{01}$.
The circuit's positive feedback removes phase-compensation components, while previous circuits require phase compensation to bypass the phase shift of the voltage reference. In previous circuits, a negativefeedback connection of the voltage reference adds the reference's response pole to the negative feedback loop. This added pole degrades stability. However, in Figure 6, the voltage reference's pole rolls off the positive, rather than negative, feedback, which benefits rather than compromises the circuit's stability. As a result, the circuit requires no added phase compensation.

Though previously mentioned positive feedback transforms a reference voltage into two voltages that retain the original polarity, modified positive feedback also makes this transformation for two output voltages with inverted polarities. To invert the result, the voltage reference returns to the negative feedback path (Fig. 7). Feedback through the voltage reference then replaces the follower feedback of the preceding circuit. This feedback switch requires reintroduction of phase-compensation elements $\mathrm{R}_{\mathrm{C}}$ and $\mathrm{C}_{\mathrm{C}}$. However, these elements don't affect the basic de function of the circuit.
The circuit in Figure 7 combines Figure 2's bootstrap inverter with the positive-feedback resistors of the last circuit. In Figure 2, the grounded noninverting input of the amplifier forces the voltage-reference output to 0 V relative to ground. To accomplish this feat, the amplifier output moves to $-\mathrm{V}_{\mathrm{R}}$. The circuit in

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Figure 7 doesn't ground the noninverting input, but instead drives this input with a positive feedback signal from the amplifier output. The added drive shifts the amplifier output below $-V_{R}$, and drags the voltage reference output with it. Then, both output voltages are non-zero and inverted in polarity relative to $V_{R}$.
Net circuit feedback controls the magnitudes of the two output voltages. Simple loop analysis combines the amplifier's negative and positive feedback effects. Ignoring the small effect of $R_{C}$, the output voltage $V_{01}$ equals the voltage at the op amp's inverting input. In turn, this voltage equals that at the noninverting input. The common input voltage develops through the positive feedback of $\mathrm{R}_{1}$ and $\mathrm{R}_{2}$. Output voltage $\mathrm{V}_{02}$ drives these resistors, and the resis-tor-divider action sets the amplifier's input voltages through $\mathrm{V}_{01}=\mathrm{R}_{2} \mathrm{~V}_{02}$ / $\left(R_{1}+R_{2}\right) . V_{01}$ also relates to $V_{02}$ through the bootstrap feedback of the voltage reference. This feedback sets $\mathrm{V}_{01}=\mathrm{V}_{02}+\mathrm{V}_{\mathrm{R}}$. Solving the two $\mathrm{V}_{01}$ equations simultaneously shows that the outputs in Figure 7 are:
$\mathrm{V}_{01}=-\left(\mathrm{R}_{2} / \mathrm{R}_{1}\right) \mathrm{V}_{\mathrm{R}}$
$\mathrm{V}_{\mathrm{O} 2}=-\left(1+\mathrm{R}_{2} / \mathrm{R}_{1}\right) \mathrm{V}_{\mathrm{R}}$
These output voltages mirror the last circuit's outputs except for inverted polarity and reversed output terminals. As desired, the circuit in Figure 7 inverts the polarity of both outputs from that of $\mathrm{V}_{\mathrm{R}}$, and neither output magnitude is constrained to $\mathrm{V}_{\mathrm{R}}$. However, the voltage $\mathrm{V}_{\mathrm{R}}$ retains control over the difference between the two output voltages. In the figure, the voltage reference again connects directly between the two circuit outputs. For the specific components shown, the original $+10-\mathrm{V}$ reference produces output voltages of -2 V and -12 V .
Output errors duplicate those described for the last circuit. The expressions for $\mathrm{V}_{01}$ and $\mathrm{V}_{02}$ demonstrate this for output errors that are caused by the voltage reference and resistors. Note that these expressions again reflect direct dependence on $\mathrm{V}_{\mathrm{R}}$. The relative tolerance error and drift of the voltage reference transfer directly to the circuit out-
puts. The output expressions also reflect the effect of resistor errors through the circuit gains. The two gains defining the outputs are $-\mathrm{R}_{2} / \mathrm{R}_{1}$ and $-\left(1+R_{2} / R_{1}\right)$. Resistor errors alter these gains to produce output errors. The circuit gains are identical to those described for the last circuit, and the resistor-error effects determined before apply here as well.

Analysis shows that the output errors caused by the amplifier also repeat in Figure 7's circuit. The op amp's net input error consists of the amplifier input-offset voltage plus the offset voltage created by the amplifier input bias current. This current reacts with the parallel combination of $R_{1}$ and $R_{2}$, with the net amplifier input error becoming: $\mathrm{V}_{\text {OS }}+$ $\mathrm{I}_{\mathrm{B}} \mathrm{R}_{1} \mid \mathrm{R}_{2}$, producing the same error as did the preceding circuit. The circuit amplifies this error by a gain of $1 / \beta$ to produce output errors. While feedback differs from the previous circuit, the net $1 / \beta$ gain is the same.

In Figure 7, the feedback through the voltage reference sets the nega-tive-feedback factor at unity, and the feedback through the resistor divider produces a positive feedback factor of $R_{2} /\left(R_{1}+R_{2}\right)$. Subtracting these two feedback factors defines the circuit's net feedback factor as: $\beta$ $=\beta_{-}-\beta_{+}=R_{1} /\left(R_{1}+R_{2}\right)$. Thus, the amplifier input errors produce output offsets of $\left(V_{\text {os }}+\mathrm{I}_{\mathrm{B}} \mathrm{R}_{\|}| | \mathrm{R}_{2}\right) / \beta=$ $\mathrm{V}_{\text {os }} / \beta+\mathrm{I}_{\mathrm{B}} \mathrm{R}_{02}$. This amplifier-error expression generates offsets equal to those from the preceding circuit.

Consequently, errors from the reference, resistors, and amplifier all transfer to the circuit outputs in the same way as described for the circuit in Figure 6. In addition, the two circuits have the same specific components, as well as the same numerical-
error results. The voltage reference produces $0.1 \%$ initial errors and 10 $\mathrm{ppm} /{ }^{\circ} \mathrm{C}$ drifts in the two outputs. As before, resistor errors affect the two outputs differently due to the " 1 " term in one of the gain equations. Between the two circuits, this term switches from $V_{01}$ to $V_{02}$, and the re-sistor-error effects also switch. Then, resistor errors produce as much as $0.2 \%$ error and $30 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ drift in $\mathrm{V}_{01}$. Corresponding errors for $\mathrm{V}_{02}$ are $0.033 \%$ error and $5 \mathrm{ppm} /$ ${ }^{\circ} \mathrm{C}$. Amplifier-input errors again produce output offsets of $94 \mu \mathrm{~V}$ and drifts of $1.6 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$.
Error trim first removes the volt-age-reference-tolerance effect by setting the voltage difference between $V_{01}$ and $V_{02}$. Trimming the voltage reference sets this difference at the ideal $V_{R}$ value. Then, resistor trim simultaneously corrects the two outputs relative to ground. For this trim, monitoring $\mathrm{V}_{01}$ offers the best resolution because of its greater sensitivity to the resistor values. Trimmed accuracy in a laboratory temperature environment is $0.02 \%$ for $V_{01}$ and $0.008 \%$ for $V_{02}$.

Phase compensation for the circuit in Figure 7 follows the approach taken in Figure 2. Compensation elements $\mathrm{R}_{\mathrm{C}}$ and $\mathrm{C}_{\mathrm{C}}$ decouple the circuit feedback from the phase shift intro-


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## VOLTAGE REFERENCE OPTIONS

duced by the voltage reference. Carefully choosing $R_{C}$ limits the dc error that the resistor creates with the amplifier's input current. Then, empirical selection of $\mathrm{C}_{\mathrm{C}}$ optimizes output settling response to a loadcurrent transient.

The final voltage-reference circuit offers variable control of both magnitude and polarity (Fig. 8). It achieves this control through a variable combination of positive and negative gain. ${ }^{3}$ Both inverting and noninverting responses result from the two connections of $V_{R}$ to the op amp. Superposition separates the two responses for analysis. First, V $\mathrm{R}_{\mathrm{R}}$ connects to the amplifier's inverting input through the feedback network of the two $R$ resistors. This connection sets an inverting gain of -1 , and the first component of output voltage becomes $-V_{\mathrm{R}}$.

A second output component results from connecting $V_{R}$ to the am-
plifier's noninverting input. $\mathrm{V}_{\mathrm{R}}$ drives this input through the potentiometer $\mathrm{R}_{\mathrm{v}}$. Potentiometer adjustment varies the noninverting gain from 0 to +2 depending on the potentiometer fractional setting, x. A setting of $x=0$ grounds the noninverting input of the op amp for a noninverting gain of 0 . Then, the inverting gain alone controls the circuit output and $V_{0}=-V_{R}$. At the opposite potentiometer extreme, $x=1$ and $V_{R}$ connects directly to the amplifier's noninverting input. Under superposition conditions, this connection produces a noninverting-gain component of +2 through the equal-valued $R$ feedback resistors. Superposition combination then results in a net circuit gain of $-1+2=+1$, and $V_{0}=V_{R}$. Thus, the potentiometer varies the circuit output from $-V_{R}$ to $+V_{R}$.

In between the potentiometer extremes, the output voltage varies linearly with the setting x. Potentiome-
ter variation produces a output response of:
$\mathrm{V}_{0}=(2 \mathrm{x}-1) \mathrm{V}_{\mathrm{R}}$
With the REF10 shown in Figure 8, $\mathrm{V}_{\mathrm{R}}=10 \mathrm{~V}$. Consequently, the circuit provides a continuously variable reference voltage from -10 V to 10 V . Traditional amplifier connections lack this bipolar range because neither the inverting or noninverting amplifier can switch gain polarity. Moreover, the circuit offers the less-than-unity noninverting gains not possible with the traditional noninverting amplifier.
As before, the output voltage deviates from the ideal because of the errors of the voltage reference, the op amp, and the resistances. Relative error in the voltage-reference output translates directly to the circuit output because $V_{R}$ is a direct multiplier term in the output equation. With the REF10J, a $5-\mathrm{mV}$ tolerance skews the

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## DIEITAN APPLICATIONS VOLTAGE REFERENCE OPTIONS

ideal $10-\mathrm{V}$ output by $0.05 \%$. This percentage error transfers directly to the circuit's output, independent of the potentiometer setting. Similarly, the relative $3 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ drift of the voltage reference shows up in the circuit's output.

Amplifier-input errors add to this output error. The op amp's offset voltage transmits an error to the output through a gain of $1 / \beta$. Here, $1 / \beta$ $=2$ because of the equal-valued feedback resistors. The effect of amplifier input current $I_{B}$ adds to this offset, and the resulting output offset is $\mathrm{I}_{\mathrm{B}}$ R. Combined, the two amplifier errors produce an output error of $2 \mathrm{~V}_{\text {OS }}$ $+I_{B} R$. This error remains independent of the potentiometer setting. Drift in this combined offset further adds to output error. With the precision OPA177G in Figure 8, the amplifier offset and drift effects produce negligible output errors of $134 \mu \mathrm{~V}$ and $2.7 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$.

The fixed resistors' tolerance errors and drifts influence the output voltage in a variable amount, depending on the potentiometer setting. Resistance errors of the $R$ feedback resistors directly alter the -1 gain component of the circuit's inverting connection. With $0.1 \%$ resistors, these tolerance errors introduces as much as $0.2 \%$ error in the output voltage. Also, the $15 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ drift of these resistors produce as much as $30 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ output drift.
However, the relative significance of these resistor errors varies with the potentiometer setting. When $\mathrm{x}=$ 1 , the -1 gain component totally controls the circuit, and the errors of the fixed resistors transfer directly to the circuit output. Yet, when $x=0$, these errors have no effect. Then, the voltage reference connects directly to the op amp's noninverting input, leaving 0 V on the input R resistor. Zero feedback current re-
sults, which also leaves 0 V on the output R resistor. Then, the two fixed resistors exert no influence on the output voltage. In between the potentiometer extremes, the output error due to the fixed resistors varies linearly between the values stated for $x=1$ and $x=0$.

Tolerance error in the potentiometer doesn't affect the output because the potentiometer's actual resistance is unimportant. The noninverting gain is affected by the potentiometer through the resistance ratio of the potentiometer segments. This ratio is independent of the total potentiometer resistance. However, the ratio does rely on the potentiometercontrol nonlinearity, which affects the potentiometer-resistance division versus control rotation. Still, circuit adjustment with an output-voltage monitor removes adjustment dependence on control rotation.

When combined, Figure 8's error


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sources produce an output-error voltage of:
$\mathrm{V}_{0 \epsilon}=(2 \mathrm{x}-1) \delta \mathrm{V}_{\mathrm{R}}+2 \mathrm{~V}_{\mathrm{OS}}+$ $2(\mathrm{x}-1) \mathrm{V}_{\mathrm{R}} \delta \mathrm{R} / \mathrm{R}$
Here, $\delta \mathrm{V}_{\mathrm{R}}$ represents the voltage tolerance of the input reference and $\delta \mathrm{R} / \mathrm{R}$ represents the fractional tolerance of the fixed resistors. None of the three error terms in the equation expresses the same dependence on the potentiometer setting x . Thus, each error must be trimmed independently to achieve error reduction throughout the control range. First, $\mathrm{V}_{\mathrm{R}}$ trim removes the voltage-reference error while observing the reference's output voltage. Then, with $x$ $=1$, amplifier offset adjustment sets $V_{0}=V_{R}$. Finally, with $x=0$, trim of the fixed resistors sets $V_{0}=-V_{R}$.

Following the above trim sequence, the circuit accuracy remains a function of thermal-drift sources. As mentioned, reference, amplifier, and resistor drifts each affect this accuracy. Total output drift varies with the potentiometer setting due to the varied effect described for the fixed resistors. The $\mathrm{x}=1$ condition represents the worst case, and limits the trimmed accuracy to around $0.016 \%$ in a $\pm 5^{\circ} \mathrm{C}$ environment. The x $=0$ condition exemplifies the best case, with a trimmed accuracy of $0.0015 \%$.

## References:

1. Graeme, J., Feedback Plots Define Op Amp AC Performance, AB \# 28, published by Burr-Brown, Tucson, Ariz., 1991.
2. Ibid., AB \# 1 .
3. Graeme, J., Designing with Operational Amplifiers, McGraw-Hill, New York, N.Y., 1977.

Jerald Graeme, manager of a linear IC development group at BurrBrown, holds a BSEE from the University of Arizona, Tucson, and an MSEE from Stanford University, Stanford, Calif.

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|  | MHz | $\begin{gathered} 100 \\ \mathrm{MHz} \end{gathered}$ | $\begin{aligned} & 1000 \\ & \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 2000 \\ & \mathrm{MHz} \end{aligned}$ | Min. (note) |  |  |  |  |
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| MAR-2 | DC-2000 | 13 | 12.5 | 11 | 8.5 | +3 | 6.5 | 1.35 | (25) |
| MAR-3 | DC-2000 | 13 | 12.5 | 10.5 | 8.0 | +8口 | 6.0 | 1.45 | (25) |
| MAR-4 | DC-1000 | 8.2 | 8.0 | - | 7.0 | +11 | 7.0 | 1.55 | (25) |
| MAR-6 | DC-2000 | 20 | 16 | 11 | 9 | 0 | 2.8 | 1.29 | (25) |
| MAR-7 | DC-2000 | 13.5 | 12.5 | 10.5 | 8.5 | +3 | 5.0 | 1.75 | (25) |
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# AC-DC CONVERTER RUNS OFF ONE SUPPLY 

W. STEPHEN WOODWARD

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Precision full-wave conversion of low-level ac signals to de is a commonly performed function in measurement apparatus. Not surprisingly, therefore, many circuits have been de-
scribed as capable of doing the job. Most of them, however, require bipolar power supplies, and all depend upon precise resistor matching for good rectification symmetry.

In addition, the symmetry of those circuits is limited by the offset voltages of their amplifiers. That is, only ac voltages that are much greater than the amplifier offset voltages can be rectified accurately. As a result, ac-coupled gain stages are often needed, increasing circuit complexity and introducing potential sources of error.

This circuit avoids those shortcomings (see the figure). It accepts the ac input on differential inputs 1 and 2 , where capacitors $\mathrm{C}_{1}$ and $\mathrm{C}_{2}$ block any dc components of the input and isolate the input signal from the bias generated by resistors $\mathrm{R}_{3}$ through $\mathrm{R}_{6}$.

To see how the rectifier works, suppose that a signal excursion drives input 1 more positive than input 2. Amplifier $\mathrm{A}_{1}$ responds by driving diode $\mathrm{D}_{1}$ into conduction, thereby forcing its inverting input to track input 1.
At the same time, amplifier $\mathrm{A}_{2}$ responds with a negative output excursion. That forces transistor $Q_{2}$ to conduct sufficiently to
cause the inverting input of $\mathrm{A}_{2}$ to track input 2. The $Q_{2}$ emitter current that must flow to satisfy this condition is given exactly by:
$\mathrm{I}_{\mathrm{e}}=\mathrm{V}_{\mathrm{i}} / \mathrm{Z}_{\mathrm{rc}}$
$\mathrm{Z}_{\mathrm{rc}}$, the series impedance of $\mathrm{R}_{1}$ and $C_{3}$, can be replaced by just $R_{1}$ if $C_{3}$ is large enough to have a very low reactance at the frequencies of interest. In that case, and if $Q_{1}$ and $Q_{2}$ are very high gain transistors, then the $Q_{2}$ collector current will track the emitter current to within better than $0.5 \%$, and will be given by:
$\mathrm{I}_{\mathrm{c}}=\mathrm{V}_{\mathrm{i}} / \mathrm{R}_{1}$
The instantaneous output voltage, therefore, is given by:
$\mathrm{V}_{\mathrm{o}}=\mathrm{R}_{2} \mathrm{I}_{\mathrm{c}}=\mathrm{V}_{\mathrm{i}} \mathrm{R}_{2} / \mathrm{R}_{1}$.
For input excursions of opposite polarity, with $\mathrm{D}_{2}$ and $\mathrm{Q}_{1}$ conducting, the roles of the amplifiers reverse. An important characteristic of the circuit is that rectification symmetry does not depend upon matching of resistors. Rectification symmetry is limited only by the matching of the transistor alphas, which is better than $1 \%$ for high-gain transistors.

Because $\mathrm{C}_{3}$ prevents amplifier offset voltages from affecting circuit performance, the ratio $R_{2} / R_{1}$ can be made large to provide high gain as well as the conversion function.

## IFD Winner

## IFD Winner for December 19, 1991

Charles Ho, Jet Propulsion Lab, Section 357, 4800 Oak Grove Dr., MS 18-104, Pasadena, CA 91109 (818) 354-7666. His idea: "Simplest Driver Yet For Stepper Motors."

## UOTI!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $\$ 150$ Best-of-Issue award and becomes eligible for a $\$ 1,500$ Idea-of-the-Year award.

# 522 <br> GIve TTL Gates 3-STATE OUTPUTS 

D. BHANUMURTY

Government of India, Ministry of Defence, Defence Research \& Development Organisation, Defence Electronics Research Laboratory, Chandrayanagutta, Hyderabad-500 005, India; (0832) 239061.

At times, it's necessary to make an ordinary TTL gate act like a three-state device, such as when a suitable three-state part isn't available. A Siliconix Si9405 load switch can be connected between the power source and the gate to achieve just that function (Fig. 1).

To appreciate how the circuit


1. A LOGIC ONE at the control input of the load switch will cut off the power to the rest of the TTL circuit.
Consequently, its output is placed into a high-impedance state.
works, consider the operation of a three-state TTL gate (Fig. 2). In that configuration, the high-impedance condition is incorporated by means of a control input connected to an extra emitter on transistor $\mathrm{Q}_{1}$. The control input is also connected to the collector of $Q_{2}$ and the base of $Q_{3}$ through a (reversed) diode, as shown in Fig. 2.

Applying a logic ZERO to the control input turns off transistors $Q_{2}$ and $\mathrm{Q}_{3}$. Turning off $\mathrm{Q}_{2}$ will then turn off Q. So a logic ZERO at the control input turns off $Q_{3}$ and $Q_{4}$, isolating the output from both $V_{C C}$ and ground.

Referring back to Figure 1, it can be seen that a conventional TTL output stage will present a high output impedance when $\mathrm{V}_{\mathrm{CC}}$ is disconnected. More specifically, removing $\mathrm{V}_{\mathrm{CC}}$ creates a condition impedance state.

2. CONVENTIONAL THREE-STATE circuits have an extra (control) emitter on their input transistors. A logic ZER0 on the control input positions the output into the high-

# चด马 Make Local/Remote 023 SWITCHING SIMPLER 

JOHN DUNN
181 Marion Ave., Merrick, NY 11566; (516) 378-2149.

Most schemes for switching between a local frontpanel control potentiometer and a remote analog control voltage involve analog SPDT switches. Implementing such schemes becomes complicated be-
cause many popular switch ICs are configured as arrays of SPST switches that have the same switching phase. In other words, all of the switches respond to ones and zeros at their control inputs in the same way (by opening or closing). Thus, to

## IDEAS FOR DESIGN

get the desired SPDT action, it's necessary either to use two ICs of opposite switching phase or to create two logic signals of opposite switching phase. In the former case, a single control signal drives the dissimilar switches; in the latter, the out-ofphase control signals drive two similar switches on the same IC.

A simpler alternative circumvents the problem by using two switch sections of one IC wherein both switches are open for local control and closed for remote (see the figure). As a result, a single logic signal can be used to drive both switch control inputs together. With this scheme, the local input is always connected, but through a resistor $\left(\mathrm{R}_{3}\right)$; only the remote input is switched in and out. When remote control is desired, the remote signal is switched in. It then swamps the local input and takes over.

The off-impedance of most good
analog switches exceeds the $10 \mathrm{k} \Omega$ of resistor $R_{3}$ by a sufficient margin so as not to affect the linearity of the 5 $\mathrm{k} \Omega$ potentiometer in the local mode. Conversely, the on-impedance of
those switches is low enough so that just a modest amount of amplifier gain allows the remote signal to override the effect of the local potentiometer when desired. $\square$


ONE LOGIC SIGNAL drives both switches in this simple local/remote selector circuit. The analog switches, which are on the same IC, open up for local operation and close for remote.

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| SM5813 | $\begin{aligned} & 153+2 \\ & 9+17 \end{aligned}$ | $\pm 0.00005$ | 5 110 db | Serial | Serial | High-performance 8ts filter |
| SM5818 | $\begin{gathered} 61+13 \\ \hline 9 \end{gathered}$ | $\pm 0.00005$ | 5 110 db | Serial | Serial | 8ts filter with 20bit output resolution for low end user |
| SM5840 | $\begin{aligned} & 61+13 \\ & +9 \end{aligned}$ | $\pm 0.00005$ | 5 55 db | Serial | Serial | $\begin{aligned} & \begin{array}{l} \text { For CD, DAT, PCM } \\ \text { playback } \end{array} \\ & \hline \end{aligned}$ |
| D/A Converter |  |  |  |  |  |  |
| $\begin{array}{\|c\|} \hline \text { Part } \\ \text { Number } \\ \hline \end{array}$ | Package | $\begin{aligned} & \text { Pin } \\ & \text { NO } \\ & \hline \end{aligned}$ | Description |  | Characteristics |  |
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| SM5861 | $\begin{aligned} & \hline \text { DIP } \\ & \text { QFP } \end{aligned}$ | 40 F | For Digital Audio EQ Delta-Sigma Converter |  | 2 channel D/A converter, match with 8 fs oversampling digital filter, PWM output, ZSNS |  |

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| SM5851 | QFP | 64 | Incorporate all major <br> Dolby Prologic <br> Surround system | - $48 \mathrm{kHz}, 44.1 \mathrm{kHz}$ or 32 kHz <br> sampling frequencies <br> - Dolby Prologic decoder <br> - Deemphasis filter <br> - Level meter flag |
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# ELECTRONIC DESIGN <br> QUICKL00K 

## MARKET FACTS

Ihe success of night attack operations in the Persian Gulf ensures a place for night vision devices in U.S. military procurement. Despite cutbacks in military budgets and forces, spending for passive night vision devices is expected to increase $9 \%$ between 1991 and 1996, according to market researcher Frost \& Sullivan International, of New York, N. Y. The biggest increase should come in the narrowest slice of the night vision market. The imaging infrared (IIR) missile seekers segment is expected to double, increasing from $\$ 67$ million in fiscal 1991 to $\$ 143$ million in 1996. New IIR technology, which use novel detector materials and focal place array technology, should help fuel this growth.

Other sectors won't fare as well in the face of cutbacks in tank, tactical aircraft, and armed helicopter production. Soldier/aviator night vision devices are predicted to drop $33 \%$ from 1991 's $\$ 189$ million to $\$ 128$ million in 1996. Airborne IIR sights, worth $\$ 434.5$ million last year, are expected to remain about the same in five years, at $\$ 436.4$ million. Vehicle/launcher sights, a $\$ 152.9$ million market last year, should rise $17 \%$ to $\$ 179.4$ million in 1996 . Not surprisingly, spending for research and development of night vision equipment is expected to rise $53 \%$, going from $\$ 76.1$ million to $\$ 116.2$ million in 1996.

## H O T PG PR O D G T S

Alow-cost auto resume (electronic bookmark) utility lets a PC user pick up where he or she left off. PCResume, from Powercard, is compatible with most memory managers, Windows 3.0, and Novell networks. It works with DOS 3.0 and higher. List price is $\$ 49$ per unit. Quantities are discounted. Delivery time is 60 days after ordering. Contact Powercard, 12231 S. W. 129 th Ct., Miami, FL 33186; (305) 251-5855; fax (305) 251-2334.

CIRCLE 453

The SCSI Software Developer's Kit is a complete toolkit for developing Small Computer Systems Interface (SCSI) drivers for PC peripherals. For SCSI peripheral makers and ASPI third-party developers, the Adaptec kit simplifies creating software drivers based on the Advanced SCSI Programming Interface. For makers of SCSI peripherals and ASPI third-party developers, the kit simplifies creating ASPI-based software drivers for any SCSI peripheral.

Each kit contains a copy of the ASPI specification documents and expanded programming guides for DOS, OS/2, and Novell NetWare. A DOS/ASPI interface is provided for developers to test and debug their ASPI device drivers.

Also included in the developer's kit are an ASPI Exerciser Program and a working ASPI disk driver. The kit sells for $\$ 150$ from Adaptec Inc., 691 S. Milpitas Blvd., Milpitas, CA 95035; (408) 9456761.

CIRCLE 454



Ademo program gives an overview of LabWindows 2.0 software development system for data acquisition and instrument control applications. The program, based on a working version of LabWindows 2.0 , includes example programs that show how LabWindows is used to develop application programs. Japanese and Spanish versions of the demo are available; a French version is in the works. Contact National Instruments Corp., 6504 Bridge Point Pkwy, Austin, TX 78730-5039; (800) 4333488 or (512) 794-0100; fax (512) 7948411.

CIRCLE 455

A31-page catalog contains specifications and applications for Star Micronics' audio transducers and buzzers. For the catalog contact Star Micronics America, 0EM Division, 70-D Ethel Rd. West, Piscataway, NJ 08854; (908) 572-9512.

CIRCLE 456

Wultiple DACs save board space, power, insertion costs, and increase reliability owing to fewer ICs. These devices are featured in Analog Devices' Multiple Digital-to-Analog Converter Integrated Circuit Selection Guide. A selection table sorts the multiple DACs by resolution and number of DACs. For the guide, contact Analog Devices Literature Center, 70 Shawmut Rd., Canton, MA 02021; fax (617) 821-4273. CIRCLE 457

The NIST Calibration Services Users Guide lists at least 500 calibration services and measurement assurance programs (MAPs) available for industry from the National Institute of Standards. MAPs are quality control programs for calibrating a company's entire measurement system. The catalog also lists NIST technical experts who may be contacted for information on services or measurement problems. For a free guide (SP 250), send a self-addressed mailing label to Calibration Program, Room A104, Building 411, National Institute of Standards and Technology, Gaithersburg, MD 20899; (301) 975-2002.

Abooklet gives technical assistance in designing aluminum enclosures. From AAvid Engineering, the free material gives design details on drawing layout and points to ways to reduce packaging costs, improve appearance, and extend the system's life. For a copy, contact AAvid Engineering Inc., One Kool Path, Laconica, NH 03247-0400; (603) 528-3400, fax (603) 528-1478. CIRCLE 458

# K M E T'S K O R N E R ...Perspectives on Time-to-Market 

## BY RON KMETOVICZ

President, Time to Market Associates Inc.
Cupertino, Calif;; (408) 446-4458; fax (408) 253-6085

success in the next-generation quadrant often kills off an
 existing product-that's viewed as good if it's your competitor's and bad if it's yours. Incremental product development strategies don't work in this cell: You start by hitting a home run and then begin hitting singles. Product developers make a conscious effort to leapfrog their competition; inspired organizations make a conscious effort to leapfrog themselves. Developers push and focus technology to do familiar things in better and different ways. It takes a lot of money to work in the next-generation cell and time pressure is intense-nothing comes easily.

Data on the realization of predecessor products about to be replaced by the nextgeneration product helps put a number of items into perspective. Collecting data on two facets, total person months of effort and time to market, of previous efforts can reveal a great deal about the current effort. The data is easy to obtain. First, identify the time to market interval. Remember the stopwatch starts when the product concept has had some review by individuals external to its synthesis, some concept analysis has taken place and the concept is simply documented on a few sheets of paper. It stops when the first dollar of revenue is collected. With the time to market interval defined, then determine how cross-functional, professional staff was applied to realize the product. How were marketing and manufacturing staffed as a function of time? How was R\&D staffed over the time to market interval?

Possessing this information makes it possible to make two dramatic predictions about the succeeding next generation effort. One, expect the number of person months of effort that goes into the production of a next generation product to be greater than the number of total person-months it took to get its predecessor to market; and two, time to market of the successor will be longer than that of the predecessor. How can this be? Simply stated, next generation products have to do things better in a big way, and doing things much better takes many people working together for a relatively long time.
Two examples follow to illustrate next generation efforts and their inherent complexity: Storagetek, now at $\$ 1.7$ billion in sales, the maker of Jukebox style mass storage systems, is reporting that it will soon offer next generation capability. This time instead of having robots move tape cassettes around, the company plans to package up 128 Hewlett-Packard, 1.600 -Gbyte, 5.25 inch, disk drives into a fault-tolerant, rapid I/0 system. It does what it replaces plus a whole lot more. Expected price of the product is $\$ 700,000$ a deal when viewed from a dollar per megabyte perspective. How long did it take and how many person months of effort were required? The answer is that it took more person-months and more calendar time than the predecessor Jukebox version. Would anyone from Storagetek care to comment?

Coloray Display Corp. is attempting to bring Charles Spindt's field-emitter technology flat panel display to market. In this device, small electron guns shoot at phosphors much as it's done in a conventional CRT. It could be a leapfrog technology from a price and color performance perspective, offering better visibility than active matrix LCDs. Reports out of Japan suggest that it cost billions to get active matrix LCDs to market in high volumes. If Coloray Display can reconstruct the Japanese staffing profile and their time to market, the company can then use this information to scope the organization's development time and development cost barriers. Or may be they already have. Coloray is assembling a group of 20 U.S. companies to discuss the technology, according to a Feb. 3 report in Business Week. Could it be looking for lots of money?

Ron Kmetovicz will lead a Time-to-Market seminar entitled "New Product Devvelopment: Doing It Better, Faster, and Cheaper" at Santa Clara University's Executive Development Center, to be held May 9, 1992. For more information on attending the seminar, contact Elmer Luthman, executive center director, at (408) 554 4521; fax (408) 554-4571.

## what's new

## No MATTER HOW YOU LOOK AT IT, SHARP'S

 NEW PASSIVE COLOR DISPIAY REALLY SHINES.Today's exploding growth in notebook computer sales is matched only by the almost dizzying array of improvements in compatible flat panel displays as manufacturers slim down, lighten up and improve the aesthetics of notebook compatible displays, while expanding screen size.

One of the latest breakthroughs from Sharp is a super-
efficient passive matrix color display whose viewing quality leapfrogs anything previously available in its class.

The new LM64C031 passive color LCD provides the compact size, light weight and low power consumption of traditional passive displays - for about half the price of equivalent TFT color models. At the same time, thanks to

Sharp's exclusive three-dimensional film compensation process, the display achieves high brightness, superior color saturation and excellent contrast without

passive color displays. The product offers VGA-quality resolution, a response speed of 450 ms and contrast ratio of $13: 1$, with mousecompatible speeds and even higher contrast ratios to be available soon.

IMAGINATION AT WORK

$$
\begin{aligned}
& \text { MAKING IT BIG WITH TFTS } \\
& \text { TAKES VISION AND } \\
& \text { ENORMOUS INVESTMENT. }
\end{aligned}
$$

Thanks to its early and continual investment in the manufacturing process, Sharp supplies some $70 \%$ of the world's thin film transistor (TFT) displays. TFT's compact, light, energyefficient package provides color, clarity and full-motion video equal to or better than CRTs.

Sharp's new flagship TFT manufacturing plant in Tenri, Japan, incorporates the cutting edge in the "giant scale integration" tools required to produce virtually flawless matrices
of hundreds of thousands of transistors. New advancements in photolithography, chemical vapor deposition and fusiondrawn glass continue to keep Sharp the quality leader in a market expected to grow to


COMING NEXT ISSUE: COLOR FLAT PANEL DISPLAYS. THEY'RE GETTING MORE COMPACT, MORE ENERGY EFFICIENT, WITH LARGER, CLEARER screens. get the big picture ABOUT WHAT'S NEW IN TFT AND OTHER COLOR DISPLAYS IN THE NEXT ISSUE OF SHARP INSIGHTS.

Sharp: NOW A MAJOR U.S. MANUFACTURER.
demonstrated an unprecedented commitment to its U.S. customers by augmenting IC research and development activities at the company's new facility in Camas, Washington, with an
additional $\$ 30$ million investment in LCD production.

The first Japanese company with an LCD manufacturing operation in the U.S., Sharp is now able to assure the fastest response and repair time possible, backed by the largest support team in the country.
 (B)


## THE SHAPE OF THINGS TO COME

PRICEIESS PREVIEWS.

The latest issue of Sharp's Memory Data Book includes several "sneak previews" of Sharp memory components now under development: a 32M Mask ROM, for examplethe world's largest; a $1024 \times 36$ unidirectional FIFO with the most fully synchronous feature set available; and a 20 ns Static RAM in a 64 K x 18 configuration. For your free copy of the ' $91 /{ }^{\prime} 92$ Memory Data Book, or for other informa-
 tion
about Sharp IC, Opto and
LCD components, call your regional Sharp office listed at right.
N. American Headquarters:

Camas, WA
$\mathrm{Ph}(206) 8342500$, Fax (206) 8348903
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## INSIG패풍



New 36-biT
FIFO MERGES

## MOST-ASKED-FOR

 FEATURES.Variously described as "data accordions" or "logical rubber bands," FIFO (First-In, First-Out) memories serve as data buffers between different CPUs running at different speeds, or between controllers and their peripheral equipment. This data-ratematching

## ANSWERING THE WISH LIST.

THE LH5420 COMES PACKED WITH FEATURES WHICH DESIGNERS TOLD SMARP THEY WANTED IN A FULL-WORD-WIDTH FIFD, INCLUDING ON-THEFLY PARITY CHECKING, TWO-WAY MAILBOX COMMUNICATIONS, SYNCHRONOUS REQUEST/ ACKNOWLEDGE SIGNALS AND PROGRAMMABLE
ALMOST-FULL AND ALMOSTEMPTY FLAGS. IT IS TIMES OF 25, 30 AND
35 NS, AND IN BOTH PQFP AND PGA PACKAGES.
systems to be interconnected by efficient data "superhighways."

Designed to meet the wish lists of top system designers, the LH5420 offers bidirectional, twoway "funneling/defunneling" from a 32 -bit bus to a 16 -bit or an 8 -bit bus, with two-way parity checking built in. Fully synchronous, the 36 -bit LH5420 also is able to provide full-word-width, two-way communications between most 32 -bit processors.

By replacing eight or more standard byte-wide FIFOs, the LH5420 saves real estate, simplifies the design process and accelerates system performance.

Its full-word width helps eliminate the problems of race conditions, metastabilities and speed differentials of side-byside partial-word FIFOs.

The newest addition to Sharp's broad line of FIFOs including both small-capacity ("shallow") and large-capacity ("deep") buffer memories -
represents the
evolution of FIFOs from byte-sized to system-wide solutions. No longer a mere piece part, the LH5420 handles system-level problems, allowing even the most highperformance

the LH5420 represents the industry's first system-level FIFO, requiring no external glue to integrate. It is available from Sharp for immediate delivery.

## QUIGK NEWS: GONFERENGES

more than half the laptop computers sold in the next decade, rather than rely solely on a keyboard, will be pen-, or stylus-based, or use both a stylus and a keyboard, experts say. To stay abreast of that trend, a conference on pen-based computing will be held in Boston, Mass., May 4-5, 1992 at the Sheraton Boston. Keynote speakers include Ed Yourdon, a pioneer in structured systems analysis, Portia Isaacson, of Dream Machine Inc., and Kirk Cruikshank of Grid Systems Inc. Besides product demos, the conference, sponsored by Digital Consulting Inc., will focus on hardware, user/applications, software, management issues, and communications. For more information, contact DCI, 204 Andover St, Andover, MA 01810; (508) 470-3880.

CIRCLE 451

## TALES FROM THE SKUNK WORKS

1he subtlety, uncertainty, rapid change, and chaos surrounding a skunk works requires the most fundamental and rigorous trust possible. This is true both between and within teams. In North America, we don't do well at trusting, collaborating, or working together. Our national divorce rate and the success rate of business teamings are tragedies.

The industrial decline in the U. S. further undermines trust. It doesn't help when CEOs pay themselves large salaries while laying off loyal workers. Lean and mean corporations are no substitute for having the right products.

A skunk works requires that we create trust and interdependence. Unfortunately, our home training, schooling, and corporate experience largely neglects these things. Our government is rife with bureaucratic bungling and distrustful, divisive attitudes.

I have discovered through painful life experience that there are three essential components to trust. These are rare, but a skunk works needs all three. The first component of trust is, of course, honesty. A recent national survey showed that $97 \%$ of those polled admitted lying. Some $61 \%$ admit regularly lying to their bosses.

Another poll showed that while $87 \%$ of employees consider management honesty and ethics essential, only $39 \%$ believe their management is. And attempts to deceive are increasing, say experts.

An organization that wants a skunk works needs integrity. Punishing deceit is best-or at least let's refrain from rewarding it.

The next component is competency. However honest you may be, I cannot trust you unless you are also competent. We screen and groom well for competency in technical areas. We need to do it better for marketing gurus and small team leaders.

The last component is psychological balance. If you are honest and competent- but emotionally distorted-I must set limits to my trust. Creative people are sometimes eccentric. Some allowances can be made for colorful personalities, yet deadlines must be met. We've all known sincere, creative people who are incapable of ever finishing a product. How about a competent, candid contributor who views the world as out to get her and is always predisposed to fight? What of engineers who take undue credit?

A senior VP I know of in a large corporation overtly and pathologically hated all marketing people. He nearly killed his company. Over a decade it wasted almost a billion dollars of R\&D.

The firm often had "killer" technology, but it consistently lost to competitors with better market fit, cycle time, cost, and quality. The company preached empowerment, skunk works, market focus, and multidisciplined teams, but the VP retained control and destroyed such practices ruthlessly. Before the firm "retired" him, it became notorious for technical arrogance, missed opportunities, annual layoffs, and management turnover.

Winners demand integrity, set limits, tolerate diversity, and compensate for human frailties. If you reward the entire team based on results, the team will help you with trust issues. The team itself knows better than outsiders who is trustworthy and contributing value.
John D. Trudel lectures and provides business development consulting. Trudel is founder and director of The Trudel Group, 52001 Columbia River Hwy., Scappoose, OR 97056; (503) 690-3300; fax (503) 543-6361. He is also the author of High Tech with Low Risk. To order High Tech, phone Eastern Oregon State College at (503) 962-3755.

## DID Y O U K N O W?

. . . that the U. S.-Japan semiconductor trade agreement signed last June is on the verge of failure. With nine months left for the U. S. to achieve a $20 \%$ foreign market share in Japan, market share stands at $14.3 \%$, where it stood in the first quarter of 1990.
... that a national opinion poll by the Roper Organization shows that $73 \%$ of Americans think the government should take a stronger stand against foreign companies that don't open their markets to American goods. Twothirds of those polled support economic penalties against countries with closed markets, even if it means paying higher prices for consumer goods. Only $23 \%$ of those polled are satisfied with the response of the Japanese government to these trade issues.

Semiconductor Industry Association
... that 10 years ago, overseas sales of Taiwan information products amounted to just US $\$ 105$ million. By 1990, sales of these products were worth US $\$ 5.25$ billion. Today, motherboards made in Taiwan accounted for $66 \%$ of world production in 1990. Taiwan is the largest producer of mouse units, snaring $72 \%$ of the world market in 1990. Keyboards, color monitors, graphics cards, and scanners from Taiwan each cornered about one-third of sales volume worldwide.
China External Trade Development Council

## DEFENSE FRONT

Ictual design files of military defense system customers are available from Target Marketing, a market research and consulting company. Files identify component parts designed into military equipment by prime and subcontractors as required by the Department of Defense. Component use can be identified by program, part type, part numbers, and contractor.

With the files, users can perform flexible searches of contractor's design files to pinpoint sales opportunities and size up the competition. The service covers more than 2000 active programs. Files come in book, tape, or floppy-disk format. Among other military/ defense products, the company has a list of key contacts in defense programs. For more information, contact David Trotz, Target Marketing, 1308 Centennial Ave., Suite 266, Piscataway, NJ 08854; (908) 424-0551; fax 4240552.

CIRCLE 452


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## PEASE PORRIDGE

# Bob's Mallibox 



Dear Mr. Pease:
I have been able to tolerate your vilification of Spice as that of an uninformed user. However, your publication of a letter from another such user forces me to respond.

Check the words leading to the acronym Spice sometime. A review of the original treatise by Vladimirescu and Liu might be informative. See anything about board design? Ifyouare going touse a tool for a purpose other than what it was intended for, you had betterunderstand how toapplyit. Thecustom Integrated Circuit designs that I have done performed as well or better than indicated by Spice simulation.

There is no reason Spice can't be used for board design, if you pay attention tohow the program converges, and why it converges to a particular solution. Any professional who uses public domain versions gets what they deserve. The program was developed for those of us that can't breadboard a design, not those so foolish not to.

## KEVIN J. McCALL

## Custom Analog IC Design Engineer

 Leominster, Mass.Whatirritates me is when people say I am uninformed and Spice has to be telling the truth-when the truthturns out to be vice versa. I'm delighted Spice works for you. $-R A P$

## Dear Bob:

I particularly enjoyed your article last year about your calibrated cardboard boxes. I work for a well-known temperature-controller company. We were having customer problems with C-type thermocouples and chasing every last tenth of a degree. Needless to say, it wasn't the customer's fault or our fault- the compensation cable didn't match the thermocouple table. It turned out that the errors of an earlier instrument matched the bad cable better than the new one that 0had smaller errors!
...However, my fingers started to rattle the keys after reading one letter in your mailbag. Namely the guy from

Boeing looking for some strain-gauge power supplies.

Well, "my own bit on the side" just happens to be precisely that. I sell them, at the recommendation of our National Physical Laboratory, to people wanting very high stability for precision force measurement. Now, I took a lot of care to develop a circuit that would give Kelvin buffering to both the positive and negative outputs, and add minimal errors to the basic reference.
I haven't taken that much care over the noise immunity and earthing that Mr. Iverson is looking for. However, I've checked afew details and can quite easily get shielded transformers specially for him. So if anyone else is after stable $10-\mathrm{V}$ power supplies - mine will put out up to an amp, making it a good laboratory reference, too. Please pass them my address.

And now while I'm writing to you, here's a poser that bemuses me. If I, as an engineer, wish to start up my own business at home while working for someone else, it causes all sorts of chaos. "Company loyalty, design rights, conflict of interests" - you name it and it's there. But now, if having left that company, I apply to a new company for a job, and openly declare my own private business, I'll be greeted by enthusiasm. "This man has initiative..."

## JIM EDWARDS

## Quiet Electronic Designs

60 Clayton Rd.

## Selsey, Sussex P028 9DF

Tel: (0243) 602132
That's a good conundrum. Thanks for the info on good supplies.-RAP

## Dear Mr. Pease:

I enjoyed the Pease Porridge about splices in speaker wire. It reminded me of the philosopher Paul Thagard's essay about astrology. He says the thing that really marks astrology as a pseudoscience is not that astrologers don't know why it should work; it's that they don't care why it should work.
The same could be said for the
speaker-wire cult. If these people had really found an empirical correlation between splices and poor audio quality, they'd be scrambling to find a physical explanation. But no. Like Peter Pan, "ya gotta believe" (and, in this case, pay money).

## MICHAEL A. COVINGTON

Assistant to the Director The University of Georgia Artificial Intelligence Programs Athens, Georgia

A good point, nicely worded.- $R A P$

## Dear Bob:

Re: What's All This Reflex Response Stuff, Anyhow? ...This is in response to dropping a very small important item (also valuable in terms of inconvenience if lost), such as a $1-\mathrm{mm}$ left-handed screw from a "grungle plunger." Don't try to catch it or deflect it. Just watch where it goes!
The reason? Small items often bounce and roll a long way. If you lose sight of it, it can take a frustratingly long time to find because it's small.
JOHN FLEMING

## Research technologist

Department of Midwifery University of Glasgow Queen Mother's Hospital

## Glasgow, Scotland

In your business, when you drop something, you darned well better watch to see where it rolls! $-R A P$

## Dear Bob:

Sometimes I have a hard time getting my colleagues to take a simple path to an end. But if I remember correctly, you are currently collecting other people's common-sense stuff for yournextbook. I know I will have more luck getting my cohorts to try thistrick if it appears in your book first. So please accept this widow's mite.

People who design electronic projects often need to be concerned about temperature. Hot spots accelerate degradation of materials and thereby cause premature (whatever that means) failure. So how do we find hot

# PEASE PORRIDGE 

spots? If we really care about temperature uniformity, for example in a precision analog instrument, we set up a tangle of thermocouples on a sacrificially modified prototype, and wait. A long measurement period in which we collect lots of data is followed by hours of disagreeable evaluation, culminating in dubious conclusions.

If all we want to do is find hot spots, though, we can use a simpler approach - liberal use of mercury-inglass fever thermometers. Fever thermometers have a number of favorable characteristics for surveying hot spots in electronic systems.
First, remember how you have to initialize a fever thermometer? It's a


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peak recorder. You have to shake it down to the arrow points before you use it. You can shake down a few thermometers and then leave them in the system for as long as you like. You can operate the system in all it's various modes, some of which certainly generate different temperature distributions than others.
At the end of the exercise you simply take the thermometers out and look at them, and learn what the worst peak temperatures were in all of the spots you monitored. There is no excess data to discard.
Second, the fever thermometer's temperature range, $94^{\circ}$ to $106^{\circ} \mathrm{F}$, is near ideal for surveying commercial equipment. By testing yourequipment at room temperature ambient, you can learn about an internal $25^{\circ}$ to $35^{\circ}$ rise. If it turns out to be less than $25^{\circ}$, it's safe and you don't care to know any more about it. If it's more than $35^{\circ}$, you need to understand it better and will want to investigate it in more detail.
Third, a fever thermometer is selfcontained, tiny, and (unless you break it) electrically insulative. You can insulate it right where you want it and secure it with sticky tape. Compared to the average thermocouple wire, a glass thermometer is an easily tamed instrument.
Fourth, the mercury bulb of the fever thermometer offers a small, well-focused sensitive target. If located in a convective plume above a heat sink, a fever thermometer will give a surprisingly high (but accurate) reading.

If you think you want a larger target to average over a larger area, wrap the bulb end of the thermometer with several thicknesses of 1-in.-wide aluminum foil, and insulate with clear tape before installing in the system. Or,survey theplume with three or four thermometers all at once.

## DOUG RAYMOND

## Teradyne ATWC

## Walnut Creek, Calif.

The temperature of a hot spot is the room ambient plus its rise above ambient. Ifyouwantto resolvelargerises, work in a cold room. To resolve small rises, start in a warm room. So, your thermometers are even more useful than at first glance. $-R A P$

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BOOLE 1


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And OrCAD Programmable Logic Design Tools offer indexed equations. Imagine taking rows of similar Boolean equations and expressing them all in one or two lines of code.

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## Low-VoltaGE And Faster 486s <br> Debut

 microprocessors, as well as the long-awaited clock-doubler version. The lower operating voltage trims power consumption by 30 to $40 \%$. And when additional $3.3-\mathrm{V}$-compatible logic is used, overall system power consumption can be reduced to allow several hours of battery operation. Moreover, Intel designers expect to incorporate improved power management, based on the SL power-management technology, into future implementations of 486 processors. Limited quantities of the $3.3-\mathrm{V} 486 \mathrm{SX}$ are available in 16 -, 20 -, and $25-\mathrm{MHz}$ versions, with volume production planned for July. In quantities of 1000 units, the $16-\mathrm{MHz}$ version of the processor sells for $\$ 174$ and the $25-\mathrm{MHz}$ unit goes for $\$ 341$. DX versions of the processor will be ready for sampling in the second half of this year.The i486DX2 clock-doubler will be offered initially in a $25-\mathrm{MHz}$ (external) version that operates internally at 50 MHz . The device, which is intended for new systems, fits in the same socket as the 486DX and requires no hardware redesign. However, some BIOS software may have to be adjusted-especially if software timing loops are used. The chip's high internal speed gives the CPU a throughput of about 40 Dhrystones. An even faster ver-sion- $33-\mathrm{MHz}$ external, $66-\mathrm{MHz}$ internal-will be released later this year. The $50-\mathrm{MHz}$ (internal) version of the DX2 is in production and sells for $\$ 550$ each in 1000unit lots. CIRCLE 586

## Dozens OF SYStem Makers To USE DK2

ON THE HEELS OF Intel Corp.'s release of the clock-doubler version of the 80486, almost two dozen system makers have released speed-upgrade versions of their desktop computers. Acer America Corp., San Jose, Calif., for instance, created a novel variable-speed oscillator and autosensing BIOS that will detect which CPU has been installed and adjusts the system to operate at maximum performance levels. With the "ChipUp" scheme, the company can build a common base system and just install the proper CPU module to hit the desired price/performance mark. Systems with "modular" architectures and full motherboard architectures can also

TAKING AIM AT HIGHperformance portable and desktop systems, designers at Intel Corp., Santa Clara, Calif., released the first $3.3-\mathrm{V}$ versions of the i80486DX and
be easily upgraded.
In addition to IBM Corp.'s upgrades to its Models 90 and $95 \mathrm{PS} / 2$ systems, commitments from Advanced Logic Research Inc., Irvine, Calif.; American Megatrends Inc.; Norcross, Ga.; AST Research Inc., Irvine, Calif.; Compaq Computer Corp., Houston, Texas; Dell Computer Corp., Austin, Texas; and many other desktop system makers indicate the wave of interest in offering higherperformance alternatives to cost-conscious power users. The DX2 clock doubler device was also incorporated into departmental systems like file servers-Apricot Computers Ltd., Birmingham, U.K., for example, has released a version of its fault-tolerant FT server with the clock-doubler CPUs. CIRCLE 587

## Frame-Buffer Graphics Comes TO PCS

TO IMPROVE THE SPEED of graphic displays, Chips and Technologies Inc., San Jose, Calif., turned to the Apple Macintosh and workstations for an architectural solution already in use by those platforms. The company's Wingine chip set implements a frame-buffer interface that delivers several times the speed offered by other VGA accelerators. The 64200 accelerator and the 64201 glue chip (for the Peak/DM motherboard logic chip set) require a "rethinking" of the system architecture because they're intended only for new motherboard designs. They do, though, allow designers to maximize the transfer rate between the microprocessor and the video memory subsystem. By employing a memory architecture in the main memory that divides the storage into standard DRAM and moderate-speed video RAMs, datatransfer rates can hit 20 to $30 \mathrm{Mbytes} / \mathrm{s}$-four to six times those of the AT bus. And because the data-transfer speed is tied directly to the CPU speed, graphics response improves as well when higher-speed CPUs are substituted.
The first Wingine version supports $72-\mathrm{Hz}$ refresh rates and 1024 -by- 768 -pixel by 256 -color displays, as well as the emerging 64 -kcolor standard. With the two-chip set, designers at Chips and Technologies estimate that building a video control subsystem will cost about the same or less than current accelerator schemes. In large volumes, the 64200 accelerator chip sells for $\$ 18$ each, while the 64201 glue chip goes for $\$ 7$ each. For more information on the Wingine chip set, Contact Chips and Technologies at (408) 434-0600. circle 588

# Local Bis Speeds Video 

Local-bus connections are making waves as a method to increase video performance. By using a local bus rather than the existing ISA, EISA, or Micro Channel Architecture (MCA) system bus, data can be passed at a higher speed without any conflict from othersignals being passed on the system bus. The local bus' popularity has raised a few eyebrows among those concerned with system compatibility, because many companies are implementing proprietary local-bus schemes. Hence, the Video Electronics Standards Association (VESA) has formed a committee to standardize a lo-cal-bus connector and device interfaces across ISA, EISA, and MCA platforms.

Over the past year, such vendors as CompuAdd, Dell, Micronics, NEC, and Orchid Technologies have released proprietary local-bus motherboards and graphics adapters. Systems implementing a local bus often report a $400 \%$ to $600 \%$ increase in graphics performance over standard configurations. Local-bus-based systems are receiving more attention because they improve performanceinWindows3.0, AutoCAD, X-Windows, and other graphics-based environments. However, because these systems are proprietary, there's no aftermarket for future expansion and no assurance of overall compatibility. The VESA local bus, dubbed VL-Bus, addresses these issues head on.

Some considerations were made while forming the VL-Bus standard, including ease of implementation, flexibility and reliability, compatibility, mechanical stability, and cost effectiveness. The goal is for end users to be able to buy any VL-Bus adapter board that can plug into their systems without any configuration concerns. VESA directly solicited and invited the participation of CPU, coprocessor, controller, network, and compression chip vendors to ensure compatibility of a wide variety of local-bus peripherals. This resulted in participation of over 40 member companies, including Cirrus Logic, Everex, Micronics, and Tseng Labs.

Currently, up to three devices are supported on the VLBus. These devices can reside on an add-in adapter card or directly on the motherboard. Each device or slot is optimized for a 32-bit data path while allowing bus sizing down to 16 bits. This protocol offers an open environment for the most widely available and cost-effective 16 -bit devices, and it defines a clear path for future 32-bit devices.

Signals provided on the VL-Bus can implement a localbus device without accessing the standard I/O bus. However, the option of using standard I/O bus signals is clearly defined. At the device level, this allows for easier, less expensive implementations, because components that don't directly benefit from local accesses can be placed on the I/O bus. For example, rather than use four EPROMs for the BIOS on a purely local device, designers can route BIOS calls through the I/O bus and eliminate two EPROMs. A

second application might employ a conventional 16-bit dig-ital-to-analog converter on the I/O bus while the graphics controller sits on the local bus.

The VL-Bus connector is a standard 112-pin MCA type that lines up directly with the ISA/EISA/MCA slot connectors. Pin One of the VL-Bus slot connector is $1 / 2 \mathrm{in}$. from the last pin of the ISA/EISA/MCA slot. This connector supplies the lowest cost and the best electrical characteristics for signals up to 66 MHz . Moreover, local-bus adapter boards can utilize the ISA/EISA/MCA signals as needed while using the extra slot length for greater mechanical strength.

The maximum size of the adapter board is the same as the form factor of the IBM PS/2 Model 30 add-in card. Hence, the VL-Bus adapter fits into slim-line as well as standard-size cases. The three local-bus slots can be aligned with any of the system slots. However, it's recommended that the VL-Bus slots are aligned with the system slots closest to the CPU. At high frequencies, the distance from the slots to the CPU can affect performance. The larger the distance, the greater the degradation in performance.

Up to three bus masters, other than the CPU, can be supported by the VL-Bus. The bus master and the target can both reside on the VL-Bus, or one or more can sit on the I/O bus. A VL-Bus device can communicate with any DMA slave or ISA/EISA/MCA bus master.
The VL-Bus is optimized for 80386 and 80486 CPUs because the signals are closely matched for these processors and their 32-bit data path. Provisions have been made to expand to a 64-bit data path as those processors become available.

The VL-Bus can operate at speeds up to 66 MHz and supports systems that can dynamically switch CPU speeds. Support is also included in the VL-Bus specification for future CPUs that will operate at higher clock rates.

Although the VL-Bus standard is comparatively robust today, allowances for future expansion have been made. These include expansion to multiple processors, additional interrupts, and widening of the data path. Toaccommodate future signals, the connector can be extended with a 32 -bit MCA connector. Any future VL-Bus extensions must be downward compatible with previous revisions.

The maximum bandwidth of the VL-Bus specification is 133 Mbytes/s at 66 MHz . This contrasts a maximum transferrate of 5 Mbytes/s on an ISA bus or 33 Mbytes/s on EISA or MCA systems. The bandwidth will supply the horsepower needed today, as well as for tomorrow's high-performance graphical environments.

The VL-Bus specification is complete, and will be formally ratified by the full VESA membership as soon as modeling and verification are done (sometime during the summer). For more information on the VL-Bus or other graphics-related issues, contact VESA at (408) 435-0333.

# Evaluating the Communications Performance of Your Next Board 

 1 ITI $\begin{aligned} & \text { Limitations from physical media, system bus latency, and } \\ & \text { software may hinder communications speed. }\end{aligned}$BY ROBERT W. O' DELL

Motorola Inc., MS OE216, 6501 William Cannon Dr. West, Austin, TX 78735-8598; (512) 891-2000.

Take a look at your last board design. Was it an island of computation, or did it communicate with the outside world? Whether you designed a PC add-in card or a motherboard, it's likely that some form of data communications had to be dealt with.

Of course, data communications problems aren't limited to PCs. Even if your last board was for embedded control, it probably communicates with other boards, or systems, or has options for doing so. Who would deny that a critical function in a laser printer's design is its need to link to a personal computer or local network, via Ethernet, AppleTalk, Centronics, or UART?

So, given the fact that communications exist on most board designs, the question you must ask yourself on each new project is: Will this solution meet the communication performance goals? The answer can be obtained in terms of three factors-physical media limitations, system bus latency and throughput limitations, and software limitations. This article looks at these limitations to see how they can be used to evaluate a board's communications performance, and differentiates their effectiveness for low- and high-speed communications.

This article uses Motorola's MC68302 Integrated Multiprotocol Processor as an example of low- and medium-speed communications. It contains an MC68000 core, generalpurpose peripherals, and three serial communications channels (SCCs). It's currently being employed in PC addin cards for such applications as V. 32 modems, as well as embedded control applications such as laser printers.

Motorola's Fiber Data Distributed Interface (FDDI) chip set is used as an example of high-speed communications. It can connect PCs and workstations to the emerging FDDI local-area networks (LANs), as well as in other embedded applications, such as concentrators and bridges. Regardless of the application, however, the principles are the same.

As a design engineer, you know what it's like to try to meet the performance goals of the board. Often these goals are generated from the marketing group. Everyone is counting on you to create an architecture that meets all of the functional and performance requirements. This would be easy except for that "it's got to be as cheap as possible" item lurking near the top of the list, not to mention that unbelievable schedule required. Most projects start with these things in common, but once beyond this point, the approach from designer to designer and company to company diverges immensely.
For instance, if you're lucky, you might have a performance evaluation model to simulate the devices' behavior. This could take the form of specific component software models that you use to run code on a simulated board made from a library of components. Similarly, hardware models are available that can simulate one or several chips' performance using the actual component. Typically, though, you won't use these models until after you've committed to a given solution and started the actual board design. In fact, these models may never be used.

0ther types of behavioral models can also work at a high level to quickly generate analysis. In fact, the brave might even generate their own model in C. Typically, though, it's not possible to do such a thorough analysis before making a decision. There never seems to be enough time to get the board out the door, much less play around with modeling decisions beforehand. It may actually be wisest to take the time beforehand, but convincing your boss of that can be another story altogether.

Therefore, most designers are left to make the decision using their experience, the experience of other company projects, and a healthy safety margin. The marketing group will clamor to your desk if the performance goals aren't met, but will they ever know if you could have met the goals with less

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## EVALUATING BOARD COMMUNICATIONS PERFORMANCE


2. The Fiber Distributed Data Interface (FDDI) solution provided by Motorola currently consists of four chips. The MC68836 FDDI clock generator (FCG) connects to the twisted-pair driver or fiber-optic module. The MC68837 elasticity buffer and link monitor (ELM) also performs part of the physical-interface functions. The MC68838 media-access controller (MAC) executes the media access portion of the FDDI standard. Finally, the MC68839 FDDI system interface (FSI) provides the buffering and connection to the system bus.
cost? Probably not. The result is a tendency for you to overengineer the design, increasing cost to meet the performance goals.
So what steps can be taken to home in more accurately on the performance you can expect? A simple model, called a triple bottleneck model, can help clear up a number of ideas that designers have about the communications performance on their board (Fig. 1). The model illustrates that the throughput of the board's communications section is gated first by the physical media, second by the system bus latency and throughput, and third by the software protocol
these factors aren't truly independent. For instance, increasing the bus performance will usually boost the software performance as well. In another example, increasing the physical performance may cause a faster burst of data to be received, requiring a decrease in the system bus latency. However, let's look at each of the three bottlenecks in more detail before discussing their interdependencies.

The physical performance of the media is the most obvious characteristic of the communications system. It's certainly the most well understood of the three bottlenecks. Depending on your application, the physical performance may not be much of an issue at all. For instance, if you're connecting up to a standard local-area network, such as Fiber Distributed Data Interface (FDDI), you're committed to providing a $100-\mathrm{Mbps}$ connection on your board. In such a case, an FDDI chip set like that from Motorola will be required (Fig. 2).
In the case of a well-defined standard protocol, the only physical performance issue is ensuring that the physical requirements of the connection are satisfied. In a standard LAN environment, the chip vendor will usually supply you with the cookbook solution for making a media connection. If they can't do this, buyer beware-they may not have verified it themselves!
For example, an FDDI solution can be made with the MC68836 FDDI clock generator (FCG) from Motorola (Fig. 3). The FCG is part of the four-chip set for FDDI. The FCG implements the lower portion of the physical layer (PHY) functions of the FDDI standard, including clock recovery, data recovery, and nonreturn-to-zero-inverted (NZRI) conversions. It also does a 5-bit parallel-to-serial conversion during transmission, and a serial-to-5-bit-parallel conversion during reception. The FCG uses the 5-bit parallel interface to communicate with the MC68837 elas-ticity-buffer-and-link-monitor (ELM) device, and directly connects to fiber-optic modules through differential driver/receiver pins.
If you're making a proprietary connection, however, you may be able to personally choose the data rate of the sys- overhead. What permeates all the way through is the real data communications rate. Actually, the performance of the system is gated by the smallest bottleneck rather than all three. This statement is mathematically expressed as:

System throughput $=$ Minimum (physical, bus, and software performance)

Board designers typically worry too much about physical performance because it's the easiest to deal with. On the other hand, software performance isn't paid much attention because it's not directly related to the hardware. Often, the reverse of these two is a far better scenario.

It should also be pointed out that

| High-speed channels |  | Low-speed channels |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Number | Speed | Number | Speed | Comments |
| 1 HDLC | 2.8 Mbps | - | - | Buffers in dual-port RAM |
| 1 HDLC | 2.2 Mbps | . | . | Buffers in external RAM |
| 2 HDLC | 909 kbps | - | - | Buffers in external RAM |
| 3 HDLC | 540 kbps | - | - | Buffers in external RAM |
| 1 HDLC | 2.2 Mbps | 1 UART | 62.5 kbps | Buffers in external RAM |
| 1 HDLC | 2.2 Mbps | 2 UART | 3100 baud | Buffers in external RAM |
| 1 HDLC | 2.0 Mbps | 2 UART | 12500 baud | Buffers in external RAM |
| 1 HDLC | 2.0 Mbps | 1 BISYNC | 204 kbps | BISYNC is half-duplex |
| 2 HDLC | 869 kbps | 1 UART | 4100 baud | Buffers in external RAM |
| 3 UART | 500 kbaud | - | - | Buffers in external RAM |
| 3 BISYNC | 333 kbaud | - | - | Buffers in external RAM |
| 3 DDCMP | 266 kbaud | - | - | Buffers in external RAM |
| 1 Transp | 2.0 Mbps | - | - | Transparent protocol |
| 2 Transp | 869 kbps | - | - | Transparent protocol |
| 3 Transp | 571 kbps | - | - | Transparent protocol |

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tem. For example, in a terminal connection, you may need to provide the option for a connection as low as 300 baud, and as high as 57,600 baud. Moreover, when connecting two systems with a proprietary serial link, a high-level datalink control (HDLC) type of protocol is often used. In such cases, the media speed is arbitrary, and is often chosen by the designer to be between 64 kbps and 10 Mbps .

Higher media speed may accomplish nothing for your connection, and may do more harm than good. If the processor handling the protocol is saturated with work, an increase in the media speed won't help the overall throughput (Fig. 4). In fact, if the protocol doesn't allow for graceful degradation, the actual throughput can actually decrease once a peak is reached. Nevertheless, one may argue that an increase in the media speed may help the response time when one isolated message needs an immediate response. But if software is involved in the response, a point of diminishing returns is reached (Fig. 5). The decision on media speed, therefore, can't be made without consulting the bus and software factors.

Having touched on the physical interface issues, let's move on to the system bus issues-throughput and latency. The bus throughput involves the protocol device moving data to and from memory, still leaving enough time for the software to use the bus in its protocol processing. Bus latency is the delay incurred when the protocol device needs to acquire the bus for a transfer.
Although most of today's new serial devices have built-in direct-memory-access channels, older protocol devices don't, and may not even allow an external direct memory access to be easily used. In such a case, the DMA movement is replaced by software instructions, and the protocol device's bus latency is replaced by the software routines interrupt or polling latency. In any case, the principles are the same.
There are two important goals in bus-performance analysis. The first goal is to analyze the percentage of the bus that will remain for the processor and any other peripherals on the system bus. The second goal is to determine that no underruns or overruns will occur on the protocol devices during operation.

Where do you get such information? Some calculations can be done by yourself, and others may require help from the manufacturer. You can easily calculate the percentage of the bus required by the protocol device during peak periods. This is done as:
$[(2 \times$ Sbps $/ 8) \div$ NBPT $] \times$ NCPT
NSBC
where:
$\mathrm{Sbps}=$ serial data rate in bits $/ \mathrm{s}$. Sbps is the rate of real data flowing through the serial device to memory. For example, in UART applications, remember that start and stop bits aren't considered real data because they're overhead that's created and stripped by the UART itself. Sbps is then divided by 8 to convert this number into bytes per second. Note that Sbps is multiplied by 2 if the link is full duplex, other-

3. This example of a physical-interface cookbook solution for FDDI uses Motorola's FDDI clock generator. Physical-interface issues can be more easily dealt with when a well-known, standard protocol like FDDI is used.
wise it's multiplied by 1 .
NBPT = number of bytes per transfer. When data is moved from the protocol device to memory, how many bytes at a time can be moved?

NCPT $=$ number of clocks per transfer. How many clocks does it take to move this data to memory? If no direct memory accesses exist, all software instructions should be counted. If direct memory accesses are used, then the average bus arbitration overhead per transfer should be included in this number.

NSBC $=$ number of system bus clocks that can occur per second.

One typical application for the MC68302 integrated multiprotocol processor might use $\mathrm{SCC}_{1}$ and $\mathrm{SCC}_{2}$ to connect to the two B channels at 64 kbps each, with $\mathrm{SCC}_{3}$ connected to the D channel at 16 kbps (the integrated-ser-vice-digital-networks (ISDN) standard defines that B channels be used for voice and data services and that the D channel facilitate the signaling on the ISDN physical interfaces; basic access provides two $B$ channels and a D channel, commonly referred to as $2 \mathrm{~B}+\mathrm{D}$ ). This means that Sbps is $64 \mathrm{k}+64 \mathrm{k}+16 \mathrm{k}=144 \mathrm{kbps}$. Each channel is full duplex.
The MC68302 processor is a 16 -bit device, and can move 2 bytes of serial data at a time over the local bus (NBPT $=$ 2). These numbers assume that the add-in card contains a local bus for the MC68302 to operate on, as opposed to the
"When I think about density, a few things come to mind. For example, the Earth is the densest planet in our solar system- 5.515 times denser than water. The most densely populated place on the densest planet is Macao, on the coast of China. 479,000 people in an area of 6.5 square miles. Hope they like each other. As for programmable logic, the award for the highest density goes to Altera's MAX7000. With 1,000 to 20,000usable gates. And morel/Othan any other PLD family. Bye-bye masked gate arrays. That's as dense as it gets. Well, there is Rocko Miller, my old col-
 crushed empty beer cans into his head. You know the type."

[^6]
# EVALUATING BOARD COMMUNICATIONS PERFORMANCE 


system bus of the PC. There are usually three clocks of arbitration for the serial direct memory accesses to acquire the bus, four clocks for a no-wait-state access, and one clock of arbitration following each 16 -bit transfer. The direct memory accesses acquire the bus for each 16-bit transfer. This means that NCPT $=3+4+1=8$. With a $20-$ MHz clock, there are 20 M system bus clocks/s available. Thus:
$\frac{[(2 \times 144 \mathrm{kbps} \div 8 \mathrm{bits} / \text { byte }) \div 2 \text { bytes }] \times 8 \text { clocks }}{20 \mathrm{M} \text { clocks } / \mathrm{s}}=0.0072$
Less than $1 \%$ of the system bus is required in this situation. Having calculated this for the multiprotocol processor, it makes sense to consider some cost-saving alternatives. First, why not choose cheaper static RAM and add one wait state? Second, the 8 -bit bus mode of the processor could be considered. Using this mode means that the 2 bytes of data will have to be moved in two consecutive bus cycles. However, EPROM and RAM width on the board will be saved, potentially saving two chips. With these two changes, the number of clocks per transfer increases from 8 clocks to $3+5+5+1=14$. The resulting equation gives:
$[(2 \times 144 \mathrm{kbps} \div 8$ bits $/$ byte $) \div 2$ bytes $] \times 14$ clocks
$=0.0126$

## 20M clocks/s

Even with the two changes, just barely over one percent of the bus is used.

Modifying the bus will affect processor performance. The 68000 processor on the MC68302 in 8 -bit mode is around $60-70 \%$ as fast as the regular 68000 under the same conditions, which implies a software performance degradation of around $30-40 \%$. Is that acceptable? Obviously, it depends on the application software that must be run. That will be discussed in detail later.

The above analysis is made assuming there's continuous activity on all three serial channels at the same time. If this isn't true, you can factor these effects into the equation. This isn't really important if the bus utilization is low, as in the previous example. But by using the last equation and running the MC68302 serial channels at maximum speed (an aggregate of around 2.2 Mbps full duplex), the bus utili-


[^7]
5. An increase in the media speed may help your response time in a situation where one isolated message needs an immediate response. However, the response can involve a number of different steps (like bus cycles, interrupts, and software). If any of those steps have a fixed time associated with them, a minimum response time is the result. Increasing the media speed eventually provides little or no benefit to the system.
zation goes up to $10.5 \%$.
The MC68839 FDDI system interface (FSI) device is designed for much higher speed operation than the MC68302 processor. It moves data to memory either 64 or 32 bits at a time, and can move data in as fast as 1 clock time at 25 MHz (although 2 clocks will be assumed here). The FDDI is a $100-\mathrm{Mbps}$ network, but it's half-duplex because a station can't receive one message and transmit a different message at the same time. Using the previous equation for the FSI in its 32 -bit mode, we have:
$$
\frac{[(1 \times 100 \mathrm{Mbps} \div 8 \mathrm{bits} / \text { byte }) \div 4 \text { bytes }] \times 2 \text { clocks }}{25 \mathrm{M} \text { clocks } / \mathrm{s}}=0.25
$$

As this equation shows, the FSI will use $25 \%$ of the bus during periods of transmission or reception. This is a reasonable figure considering that it only applies when data frames are actually sent to or received from this particular station.

The bus-utilization numbers indicate how much of the bus the processor will have remaining for software tasks. But the second goal in looking at the bus is to determine that no underruns or overruns will occur on the protocol devices during its operation. In most synchronous protocols, once data transmission or reception begins, it's impossible to delay the process. As serial data is received into the protocol device, some sort of buffering is made for the data because there's no guaiantee that the system bus will be immediately accessible to the peripheral. On older UARTtype devices, this buffer may be just two bytes, known as double buffering. On the MC68839 FSI, supporting 100Mbps data rates requires more internal buffering. The FSI supports its internal buffering in an 8-kbyte internal RAM shared in various configurations between the receive and transmit machines. On the multiprotocol processor, the buffering depends on the protocol used-either 3 bytes or 3


# NICE and simple math exposes the myth of ST-NIC. 

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[^8]
## EVVALUATING BOARD COMMUNICATIONS PERFORMANCE

## Designina

words on receive, and 3 bytes or 4 words on transmit. Stream-oriented protocols like HDLC and Transparent use the larger buffering.

From the time that the first receive data arrives, it's fairly easy to calculate the bus latency allowed by your protocol device. The latency is simply the time it takes to fill up the internal receive buffer. This can be calculated as:

FIFO size in bytes
(Sbps) $\div(8$ bits/byte)
With a $20-\mathrm{MHz}$ multiprotocol processor working at the maximum sustainable data rate of 2.2 Mbps in its HDLC or Transparent protocols, the bus latency is:
$\frac{6 \text { bytes }}{(2.2 \mathrm{Mbps}) \div(8 \text { bits/byte })}=21.6 \mu \mathrm{~s}$
With a $25-\mathrm{MHz}$ FSI working at 100 Mbps , the bus latency is:
$\frac{3.2 \text { kbytes }}{(100 \mathrm{Mbps}) \div(8 \text { bits/byte })}=256 \mu \mathrm{~s}$
The FSI FIFO size is calculated by dividing the 8-kbyte RAM into a receive and transmit portion, after accounting for overhead caused by buffer descriptors and internal parameters.

Actually, the latency supported by the FSI depends on the configuration. If the 8-kbyte memory is configured with 2 receive queues and 4 transmit queues, the latency is reduced to $80 \mu \mathrm{~s}$-still a reasonable number in most systems.

1he problem with those latency calculations is that they don't include the dynamics of every factor that can influence the state of the internal buffers or FIFOs. For instance, on the multiprotocol processor, a complex web of actions can occur between the transmit and receive sections of the three serial channels that it supports. Furthermore, information received at the start of a frame may be checked
for address recognition, a task accomplished by a RISC coprocessor on the multiprotocol processor. Thus, a true latency model depends on numerous factors. If a true latency equation could be developed on the MC68302 processor, it would be a function of many parameters, such as:

- The number of SCCs used
- The data rate on each SCC: receive and transmit
- The type of protocol run on each SCC: HDLC, Transparent, BISYNC, DDCMP (digital data communications message protocol), UART, V.110)
- The length of the received and transmit frames on all SCCs and their relationships to each other over time
- The number of flags or idles sent between each frame
- The frequency of the system-bus side of the MC68302 processor
- The addresses to be automatically recognized (if any)
- The location and position of control characters in the frame (if any)
- The use of single or multiple buffers per frame
- The external bus width
- The number of wait states to memory
- The maximum time it takes for the SCC to acquire the bus when needed
- The decision to put certain data buffers in the internal dual-port RAM or in external RAM

Needless to say, this becomes a job for experimentation or simulation, not a mathematical equation. The decision made for the MC68302 processor was to run a number of experiments in different configurations to get real results on the actual device (Table 1). The results show the maximum performance that was obtained with the MC68302 using different protocol combinations on different SCCs. In all cases, full-duplex operation is assumed, unless noted, and the SCCs obtained the bus within 20 system clocks of requesting it. The numbers assume a $20-\mathrm{MHz}$ system clock, and can be scaled linearly for different clock speeds.

These results are superior to laten-

TABLE 2: LAPB OR LAPD SOFTWIRE PERFOBMEIUE OW THE MCG8302

| Serial bit rate | Frame length | Window size | Iframes/s | Theoretical limit |
| :---: | :---: | :---: | :---: | :---: |
| 64 kbps | 30 bytes | 3 frames | 412 | 533 |
| 500 kbps | 30 bytes | 3 frames | 470 | 4167 |
| 500 kbps | 30 bytes | 7 frames | 875 | 4167 |
| 500 kbps | 30 bytes | 9 frames | 890 | 4167 |
| Notes: <br> 1. The theoretical limit of the line assumes no overhead (such as flags, CRCs, zero insertion, and receiver-ready frames) and an infinite window size. <br> 2. The window size (also known as $k$ ) is the number of frames that may be sent without receiving an acknowledgement (modulo 128). This value can impact performance considerably. <br> 3. Only layer-2 information frames are counted in the total shown. The rate shown is the total full-duplex channel rate. Thus, 890 I frames/s equals 445 transmitted and 445 received I frames/s. <br> 4. The frame length is defined as all bytes between the opening flag and the first CRC byte. <br> 5. Performance numbers for LAPB or LAPD are virtually the same. <br> 6. The following Motorola-developed tasks were running during this experiment: <br> Layer 7-file transfer application <br> Layer 2-LAPB or LAPD (1988 blue-book compatible) <br> Layer 2-MC68302 chip drivers <br> EDX-real-time kernel |  |  |  |  | cy-calculation results because they show the true maximum performance that was achieved without incurring a FIFO underrun or overrun. Even though the SCC's clocking limit is 8 MHz , the highest long-term sustainable rate is less ( 2.8 Mbps full duplex), and this value assumes that data buffers are held in the internal dual-port RAM of the chip, as opposed to external memory.

In your project, you probably won't have the luxury of testing a given configuration of your protocol device to see if it will work. For fast results, ask the manufacturer for any available performance data. If you can't get the performance data for the particular configuration you need, ask their applications group about their experience. For instance, although Motorola

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6. The protocol-device driver's performance can be significantly enhanced if the protocol device supports automatic descriptor rings and on-chip direct memory access, like that on the MC68839 FSI and MC68302 multiprotocol processor. The FDDI system interface provides a user-definable number of descriptors, and the multiprotocol processor offers 8 receive and 8 transmit descriptors for each of its three SCC channels.
didn't publish performance data for the MC68302 for any RAM other than zero-wait-state accesses, it was found through experience that each wait state added to the system decreases serial performance by about only $1 \%$.

TWe last performance-analysis area is the software itself. This is the software-protocol overhead that must execute along with the protocol device to complete the communications desired on the board. The software overhead can be thought of as performing two distinct activities. The first activity is the protocol-device driver, and the second is the upper-layer software execution.

In your application, the device driver in your performance analysis may not be a concern because the driver could be considered as part of the communications software. But, a distinction must be made if the protocol-device driver can be the cause of speed limitations. For instance, the buffer descriptor ring of the multiprotocol processor can receive up to 8 HDLC frames without software intervention. However, consider the effect of a ring only two frames long. HDLC-type frames can be as short as five bytes ( 1 address; 1 control; 2 cyclic-redundancy-check, or CRC, bytes; and a closing flag that serves as the opening flag of the next frame). Now consider the case of receiving multiple 5-byte HDLC frames back-to-back. After the first frame is received, the software only has five byte times to process the first data buffer before the protocol device reports some kind of "out of buffers" error, and stops receiving. Is the interrupt overhead in the driver low enough to meet this time in all conditions? If not, you have another performance bottleneck to consider.

Obviously, whether or not there's a device-driver bottleneck depends a great deal on the serial data rate (the lower the better), and whether the protocol supports flow control. For instance, link-access protocol, D channel (LAPD) and link-access protocol, balanced (LAPB) support a window function that ensures they will never send more than $k$
frames (where k is a variable) without receiving an acknowledgement. Similarly, UART protocols may support XON or XOFF characters or out-of-band flow-control signals (such as CTS) to prevent overflowing the receiver.

If the protocol device requires polling or interrupts on a per-byte basis, then the protocol-device driver gets even more important to analyze. The required response time of the driver is one byte. If the protocol device has on-chip direct memory access, yet won't actively switch between data buffers without software control, then your driver must still have a low response time. If your protocol device is like the MC68302, your driver must have a response time of 8 buffers/frame-the number of buffer descriptors the device offers for the receive and transmit sides of each SCC. If your protocol device is like the MC68839 FSI, then it has a user-definable buffer ring capability built into the external RAM, and the driver's response time can be as large as the memory will allow (Fig. 6). Of course, don't overlook the fact that as you wait to process the incoming frames, the amount of work grows.

What do you do if the protocol-device driver in its worstcase situation can't meet the needs of the protocol devices for a particular data rate? You have three possible choices:

1. Do nothing. Based on your analysis, you agree to live with the fact that the out-of-buffers condition will occur once in a while. The only reliable way to decide how often this will happen is to directly measure the system. In any case, your communications protocol has a method of recovering from this error in some manner (for example, this frame and others are possibly retransmitted again later). And the frequency of this occurrence is not great enough to significantly affect the performance.
2. Decrease the software driver latency. This can be done by code optimization, a better software architecture, or a faster main processor (at more cost, of course).
3. Lower the serial data rate. You decide that better total throughput will be obtained by eliminating or decreasing the chance of an out-of-buffers condition.

The upper-layer software includes everything required to make the communications software a full usable package. For instance, in an application that includes an FDDI connection, the FDDI chip set implements the media access control (MAC) and physical (PHY) layers, while the upper-layer software may implement the transfer-control protocol/internet protocol (TCP/IP) layer-3 and -4 functions. In addition, if a home-grown UART-based protocol were used, the MC68302 processor could implement the UART-character formatting, control-character recognition, and part of the flow-control functions, while the up-per-layer software does the rest.

As a final example, consider the MC68302 multiprotocol processor used in an application that needs an X. 25 connection (consisting of layers 1,2 , and 3 ). The line driver and the processor would implement layer 1 . The processor with its layer-2 support functions and software running on its 68000 core would implement LAPB, which comprises layer 2. The packet-layer protocol (PLP) would be implemented totally by upper-layer software. Even if the physical is-

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## EVALUATING BOARD COMMUNICATIONS PERFORMANCE


sues, bus-throughput and latency issues, and device-driver issues are dealt with appropriately, the upper-layer software may be the real communications bottleneck in the system. No matter how fast data can be correctly stashed in buffers, it's all wasted capability if the upper-layer software can't keep up.

Consider, for example, an X. 25 application running on the MC68302 multiprotocol processor. Experiments were performed using two MC68302 application-development-system (ADS302) boards. Each board contained one MC68302 operating at 16.67 MHz , and 512 kbytes of 1-wait-state DRAM, with all code executed out of 3-wait-state EPROM. The two boards passed frames (created and stored in DRAM) to each other with one SCC operating as a full-duplex HDLC channel.

The software running on each board consisted of different tasks that communicate with message passing, along with the real-time kernel EDX. The results assume 30-byte frames in all cases, and show the data communications rate of the data in frames per second (Table 2).

Under the high serial data rate conditions, adding the PLP layer-3 software decreases the overall throughput by about a factor of 2 . This is consistent with results found on other processors in combination with other protocol devices in an X. 25 environment.

If the serial data rates are low, the software throughput approaches the physical serial rate. However, when the serial data rate is increased, the software tops out at its own performance limit. The varying results between entries is attributed to whether the software or the physical line is the performance bottleneck. If the result is close to the theoretical limit, the line is clearly the bottleneck. Because the amount of code executed in these experiments is virtually the same regardless of the frame length and the number of serial communications channels used, the software limit is the highest value shown in the results table-about 900 frames/s.

If more software throughput is needed, you must increase the clock speed or change the processor. The MC68302 processor has a feature called slave mode that turns off the CPU and allows it to be used as a peripheral chip to another processor. For instance, software runs four times faster using an MC68302 in slave mode with a 25 MHz 68020 as a master.

There are several alternatives available if there's no software performance on hand, such as:

1. You can compare what you're trying to accomplish with that of other known results. For instance, the LAPD and LAPB results would be generally applicable for any HDLC-type protocol, such as synchronous data-link control (SDLC).
2. If you're changing processors, run some of your old existing communications software, perhaps time-critical routines, on the new processor.
3. Talk to the protocol-device manufacturer to see if they have any unpublished information available.
4. Talk to third-party communications-software-develop-
ment houses about their software performance using the manufacturer's devices.
5. Take a look at the work that must be performed for each frame, add a healthy adder for the unknown, and then scale this up based on the number of frames you expect to receive per second. This should be your last resort.

Now consider an FDDI software application. Although the FDDI chip set can buffer data at 100 Mbps , there's no standard processor that can process FDDI frames at this speed with a full software application running (such as TCP/IP). In fact, even high-end FDDI stations can only process data in the neighborhood of $5 \mathrm{Mbytes} / \mathrm{s}=40$ Mbps, well under the $100-\mathrm{Mbps}$ limit.

So, why are people designing with FDDI? Basically, they want to obtain better throughput for the LAN as a whole. Even if each FDDI node can only support a low communications rate, an FDDI LAN could support many such stations simultaneously with no real loss in throughput at a given node.

To estimate the maximum performance of a given application, all you need to do is find the bottleneck in the system. As we have seen, it may be found in a number of different places. Once you find the bottleneck, you can take two courses of action-eliminate the bottleneck while being wary of cost; or decide that the performance is satisfactory and look for ways to reduce cost in the design. When looking to reduce cost, you must ask yourself several questions, such as:

1. Do I have the option to reduce the media speed? If so, I may be able to save money on the media, line drivers, and/ or protocol device. Note that the protocol device may be available in a lower-cost version when run at a slower speed.
2. Do I have the option to modify the bus characteristics? If so, can I reduce cost by using memory with more wait states? Can I design a narrower bus to eliminate a number of components? Did I add more expensive components or glue in the system to keep the bus latency down to a minimum? If so, perhaps they can be eliminated.
3. Is the software device driver non-critical? If so, then use only high-level languages, such as C , and reduce design time.
4. Is the data rate so slow that the full processor speed isn't required? Perhaps its speed can be reduced, or a less expensive processor chosen.

Robert W. O'Dell, a senior applications engineer in the data communications group at Motorola, received a BSES from the University of South Florida, Tampa, and a MSCS from the University of Texas, Austin.

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Three chips that bring Edge-Enhancement Technology (EET) to laser printers are the D9001L, D9001B, and D9001H. Like the original D9001, the chips detect and smooth jagged edges of printed raster images without any assistance from external software. This results in higher quality and faster output.
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Also available is an integrated GUI controller called the WinStyler that enables users to get what-you-see-is-what-you-get (WYSIWYG) output on their laser printers. Unlike other GUI-based solutions, it can handle encapsulated PostScript files and Bezier curves. Where other configurations require a card that fits into the printer's I/O slot, another card that goes into the host PC, and a heavy video cable, the WinStyler uses the standard Centronics port and cable. Hence, it's an easy plug-and-play solution.

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MODEM, FAX INTERFACE FITS IN TINY PACKAGE


Referred to as a data-access arrangement, the CH1834 is an internationally approved telephone line interface that fits in a 26 -by-60-by- $9-$ mm package. The part links modem and facsimile chips to the telephone line to protect the line from unwanted power surges. It employs a proprietary solid-state transformer to reduce size and weight. The CH1834 contains isolation and surge protection, ring detection, and a two-to-four-wire converter. It can be used with modems ranging up to V.32bis and fax applications to V. 17.

Cermetek Microelectronics Inc.
1308 Borregas Ave.
Sunnyvale, CA 94088
(408) 752-5000

- CIRCLE 602


## LOCAL-BUS VGA CHIP SUPPORTS 24-BIT COLOR

By employing a local-bus-type interface to the host CPU, the TVGA8900CX gives designers a fast-responding graphics controller that can support 24 -bit true-color modes at 640-by-480-pixels. In addition, the Trident chip can also control 256 -color screens at resolutions ranging from 640 -by- 480 to 1024-by768 pixels (either interlaced or noninterlaced). A 1280-by-1024 mode with 256 colors using interlaced monitors or 16 colors with noninterlaced monitors provides top resolution. To deliver the pixels, the chip employs a dot-clock of 108 MHz . That rate also supports the VESA (Video Electronics Standards Association) $70-\mathrm{Hz}$ refresh standard.

The chip achieves zero-wait-state performance with the host CPU thanks to an on-chip command FIFO register. That register maximizes the bus transfer speeds for applications like Windows or AutoCAD, because such applications write directly to the video memory. Other enhancements include the using the fast local-bus interface, which employs a $50-\mathrm{MHz}$ DRAM clock, to
pump data from fast-page-mode DRAMs. Furthermore, the controller has a 2-Mbyte linear address space that eliminates overheads imposed by the bank-switching schemes used by most other highresolution drivers.

The TVGA8900CX can also take advantage of Trident's library of high-resolution drivers that were created for previous graphic controllers (the 8900 C and 9000 ). Drivers support a wide variety of application packages as well as the Analog Devices CEG RAMDAC and the Sierra HiColor RAMDAC.

DRAMs with word widths of 4,8 , or 16 bits can be used by the controller. The device includes programmable timing so that the memory interface can be optimized. Automatic monitor detection, memory detection, and data bus transceivers are also incorporated in the 160 -lead PQFP-housed TVGA8900CX. In lots of 1000 , the chip sells for $\$ 20$ apiece. Samples are available from stock.

> Trident Microsystems Inc.
> 205 Ravendale Dr.
> Mountain View, CA 94043
> (415) 691-9211
> - CIRCLE 603

## 65.5-MBYTE, 2.5-IN. DRIVE STANDS JUST 12.5 MM HIGH

The latest in a line of $2-1 / 2-\mathrm{in}$. hard drives combines advanced durability, reliability, power management, and reduced form factor. Seagate's ST9080A holds 65.5 Mbytes of data in a $12.5-\mathrm{mm}$ high package. The company says that this is the lowest-profile platform currently available. The 4.8 -oz. drive features a 16 -ms average seek time, a standard PC/AT interface, an MTBF of 150,000 hours, and can withstand a nonoperating shock of 150 Gs . The power-management features support active, idle, standby, and sleep modes. High data integrity is achieved through 88 -bit on-the-fly error-correction code. The ST9080A disk drive is priced at $\$ 395$. Evaluation units are available now, with production starting in the third quarter.

Seagate Technology Inc.<br>920 Disc Drive<br>Scotts Valley, CA 95066<br>(408) 488-6550<br>$\rightarrow$ CIRCLE 604<br>3255 Scott Blvd.<br>Bldg. \#3, Suite 102<br>Santa Clara, CA 95054<br>(408) 980-9565<br>- CIRCLE 605

## TINY MODEM FITS <br> PORTABLE APPLICATIONS

A fax-data modem that's designed for portable and pen-based systems can send and receive data at 2400 bits/s and facsimiles at 9600 bits/s. The 2-by-1-in. modem's power-down mode can be implemented to extend a portable system's battery life. The module, which weighs just $1.5-\mathrm{oz}$., uses surface-mounting technology to increase reliability. It also makes the part easy to integrate onto a motherboard. The modem implements CCITT V.22bis data-correction and V. 42 error-correction technology. Housed in a 40 -pin DIP, the part operates on a single $5-\mathrm{V}$ supply with less than a $200-\mathrm{mA}$ operating current. In power-down mode, the modem draws just 1 mA .

## Micro Integrated

## Communications Corp.

## KIT HELPS DESIGN PORTABLE 386SX SYSTEMS

The ESP 386SX development and evaluation kit gives designers the opportunity to develop full PC/ATcompatible systems in packages measuring 5.3 by 4.1 by 2 in . The system's small size tailors it to medical devices, portable communications, and field test equipment. Combining ESP's small form factor with the use of standard ISA bus signals makes it suitable for embedded control and motherboard markets.

ESP was designed for upgradability due to its modularity. The backplane can be modified to conform to the existing space. The kit comes with a 386 SX processor running at 16,20 , or 25 MHz ; a super-VGA driver that supports liquid-crystal displays and monitors; floppy- and hard-drive controllers; and up to 20 Mbytes of RAM. Optional modules include analog-to-digital and digital-to-analog converters, a network or SCSI interface, and a modem.

## Dover Electronics

P. O. Box 1532

Longmont, CO 80502
(303) 772-5933

## - CIRCLE 608

## GRAPHICS CARD DOUBLES PERFORMANCE

Delivering twice the performance as its predecessor at $40 \%$ of the price, the Spectrum/ 24 PDQ Plus graphics card runs on Macintosh NuBus systems. The accelerated, 24 -bit card includes SuperVideo, a powerful dis-play-management utility; and SuperMatch, a color-fidelity solution to ensure that on-screen colors match the printer's output. In addition, a digi-tal-frequency synthesizer eliminates the need for oscillators. The card adds functionality for color desktoppublishing, illustration, design, layout, and photo-retouching applications. It supports NTSC RGB and PAL RGB displays and NuBus blockmode transfer in slave mode. Displays up to 21 in. can be accommodated with resolutions to 1152 by 870 pixels. Available now, the Spectrum/ 24 PDQ Plus sells for $\$ 2399$.

## SuperMac Technology

485 Potrero Ave.
Sunnyvale, CA 94086
(408) 245-2202

- CIRCLE 609


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# CMOS Op Amps Not Only Swing Their Outputs To Both Rails, But Also Handle + And -Common-Mode Input Voltages Beyond Them. RaIL-T0-RAIL OP AMPS USE DEPLETION-MODE PMOSFETS 

The growing demand that analog and mixed-signal systems operate from a single, positive, sub-$15-\mathrm{V}$ power-supply rail has brought about a new breed of op amps specifically designed for those conditions. These op amps must handle common-mode voltages (CMVs) at the input that exceed the positive power-supply rail and/or swing below the negative powersupply rail. Just as important, their outputs must be able to swing within a few tens of millivolts of both the ground potential and the positive
power-suply rail while driving a practical load (less than $100 \mathrm{k} \Omega$ ).

System designers need more than a universal device, like the ubiquitous 741 op amp -they want an opamp family that includes generalpurpose, micropower, precision, and even precision-micropower and highspeed devices. Pushed for pc-board space, today's designers also demand dual and quad op amp ICs.

To meet these demands, National Semiconductor is adding four new op amps to its family of CMOS op amps: the dual/quad LMC6482/84, the dual LMC6062, and the dual LMC6082. These devices represent the third generation of CMOS op amp circuit


[^11]
## RAIL-TO-RAIL OP AMPS

designs. The LMC6482/84 addresses both input-CMV range and outputswing demands, while the LMC6062 and 6082 only address outpüt-swing demands. The 6082 adds precision to the mix, while the 6062 combines precision performance with a quiescent current of less than $19 \mu \mathrm{~A} / \mathrm{op} \mathrm{amp}$ (see the table).
While over a dozen IC op amps are available with outputs that can swing close to the power-supply rails, the LMC6482/84 is one of the few that can also handle commonmode voltages that exceed both pow-er-supply rails (felectronic deSIGN, June 13, 1991, p. 135). To do the job, National's IC designers took advantage of a unique, depletion-mode, p-channel MOSFET for the pair of transistors-FETs $\mathrm{M}_{1}$ and $\mathrm{M}_{2}$ forming the differential-pair input circuit (Fig. 1).
To handle input CMVs beyond the power-supply rails, existing op amps have used two differential stages with their inputs connected in parallel and their outputs in a push-pull configuration. One differential pair is built of p -type transistors and the other of n-type transistors (both bipolar and CMOS op amps have used the architecture). This topology suf-
fers from several problems including noise, offset-voltage change with CMV, cross-over distortion and gain variation.

## Low Power

The demand for op amps that run off single- and lowvoltage power-supply rails was driven by the need for circuit simplicity and the desire to save power. Designers want both the ana$\log$ and the digital circuits in mixedsignal systems to run off a single $5-\mathrm{V}$ logic supply-an industry standard that's rapidly dropping. And more and more systems are running off batteries. In laptop and notebook PCs, cameras, camcorders, and laboratory and medical instruments, low-voltage power-sup-ply-rail operation is a must to save power and often to permit operation directly from battery-voltage levels

2. WHEN A 12-V PK-PK SINE WAVE is applied
to the LMC6482 op amp, the output is clipped cleanly at the 0 and $+10-\mathrm{V}$ rails. The op amp runs off a single $+10-\mathrm{V}$ supply and is connected as a unity-gain follower.

| MATOMA SEMHOMDUHOR' GMOS OP AMPS |  |  |  |
| :---: | :---: | :---: | :---: |
| Specification | LMC6482/84 | LMC6082 | LMC6062 |
| Output-voltage swing (with load connected to supply voltage $\div 2$ ), V With $2-\mathrm{k} \Omega$ load and $15-\mathrm{V} / 5-\mathrm{V} / 3-\mathrm{V}$ supply With $600-\Omega$ load and $15-\mathrm{V} / 5-\mathrm{V} / 3-\mathrm{V}$ supply | $\begin{gathered} 0.3 \text { to } 14.6 / 0.1 \text { to } 4.87 / \mathrm{NS} \\ 0.8 \text { to } 13.9 / 0.3 \text { to } \\ 4.61 / 0.32 \text { to } 2.65 \end{gathered}$ | 0.5 to 14.3/0.2 to 4.7/NS <br> 1.3 to 12.9/ 0.5 to $4.3 / \mathrm{NS}$ | 0.04 to $14.96 / 0.02$ to $4.98 / \mathrm{NS}^{1}$ 0.15 to $14.85 / 0.04$ to 4.97/ $\mathrm{NS}^{2}$ |
| Common-mode-voltage range, dB At $15-\mathrm{V} / 5-\mathrm{V} / 3-\mathrm{V}$ supply, for CMRR $\geq 50 \mathrm{~dB}$ | $\begin{aligned} & 0.2 \text { to } V^{+}+0.21 \\ & -0.2 \text { to } V^{+}+0.2 / \\ & -0.1 \text { to } V^{+}+0.1 \end{aligned}$ | $\begin{gathered} -0.1 \text { to } \mathrm{V}^{+}-2.5 / \\ -0.1 \text { to } \mathrm{V}^{+}-2.5 / \\ \mathrm{NS}^{3} \end{gathered}$ | $\begin{gathered} -0.1 \text { to } \mathrm{V}^{+}-2.3 / \\ -0.1 \text { to } \mathrm{V}^{+}-2.3 / \\ \mathrm{NS}^{3} \end{gathered}$ |
| Common-mode rejection ratio (CMRR), dB At 15-V/3-V supply | 85/NS | 75/ S $^{4}$ | 75/ S $^{4}$ |
| Offset voltage, mV | 500 | 350 | 350 |
| Offset-voltage drift, $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ | 2 | 1 (t) | 1 (t) |
| Slew rate, $\mathrm{V} / \mu \mathrm{S}$ | 1.2 | 1.2 | 0.02 |
| Unity-gain bandwidth, MHz | 1.3 | 1.3 (t) | 0.1 (t) |
| Quiescent current per op amp, $\mu \mathrm{A}$ At $15-\mathrm{V} / 5-\mathrm{V} / 3-\mathrm{V}$ supply | 625/500/375 | 850/750/NS | 23.5/19/NS |
| Package type | 8 -pin DIP/SOIC <br> 14-pin DIP/SOIC | 8-pin DIP/SOIC <br> 14 -pin DIP/SOIC | 8 -pin DIP/SOIC <br> 14 -pin DIP/SOIC |

[^12]as low as 3 V .
To retain even a smidgen of the 120 -or-so-dB dynamic range formerly possible when $\pm 15-\mathrm{V}$ power-supply rails were once used, analog designers need op amps as such these new National ones with power-supply rail-to-rail input and output circuits. For years, analog designers grew used to running off $\pm 15-\mathrm{V}$ power-supply rails, which provided $\pm 10-\mathrm{V}$ full-scale output signals. Most op amps easily put more than $\pm 10 \mathrm{~V}$ across 2000 $\Omega$, and typically these bipolar devices offered inputvoltage noise below 10 nV per $\sqrt{\mathrm{Hz}}$, and many had offset voltages below 500 $\mu \mathrm{V}$. And in most applications, it was usually easy to keep CMVs inside the power-supply rail-and with $\pm 10$-V signals and $\pm 15$-V power-supply rails, the output signal never had to

#    

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## Tektronix

Test and Measurement
swing even close to either powersupply rail.

However, most of today's single-power-supply op amps are different animals. Many, like National's, are CMOS. Although they simplify pow-er-supply rail-to-rail output swings, they can't touch bipolar devices on input-voltage noise. In addition, per-formance-particularly speed/ bandwidth and common-mode rejection ratio (CMRR)-drops with supply voltage. Thus, to maximize dynamic range (the difference between the maximum signal and the noise floor) and signal-to-noise ratio (SNR), IC designers are developing op amps to swing as close to the pow-er-supply rail as possible. Moreover, data sheets are specifying multiple power-supply voltages.

For example, the basic specifications for all four new op amps are written around a +5 -V power-supply rail. In addition, CMRR, CMV range, output swing, and quiescent current of the LMC6482/84, are also specified running off a +3 -V power-supply rail (see the table, again)-some data is also given running off 15 V .

An unbelievably low typical bias current of 10 fA represents one feature common to all members of the new CMOS op-amp family: It is a typical specification because it can't be measured "economically" in production quantities. Guaranteed specifications drop as low as 4 pA , however that's at a temperature of $85^{\circ} \mathrm{C}$. Because bias current is halved for every $10^{\circ} \mathrm{C}$ drop in temperature, bias current should be less than 0.07 pA at $25^{\circ} \mathrm{C}$. And current noise becomes truly unmeasurable, albeit a typical value of $0.0002 \mathrm{pA} / \sqrt{\mathrm{Hz}}$.

All four of these ICs offer low quiescent currents. Quiescent current of the dual LMC6062 is a maximum of just $19 \mu \mathrm{~A}$ per op amp running on a +5 -V power-rail, and is less than 24 $\mu \mathrm{A}$ per op amp on a +15 -V powersupply rail. Running off either +5 - or $+15-\mathrm{V}$ power-supply rails, the LMC6082 needs less than $850 \mu \mathrm{~A} / \mathrm{op}$ amp. Running off $+3-,+5$-, and $+15-$ V power-supply rails, the LMC6482/ 84 typically needs 416,500 , and 625 $\mu \mathrm{A}$ per op amp, respectively. Also note that these are true op amps with
typical open-loop gains of more than 100 dB while driving loads of $2000 \Omega$, and somewhat less while driving loads of $600 \Omega$. And all but the LMC6062 can drive loads of $2 \mathrm{k} \Omega$ to within a few 100 mV of both powersupply rails while running off $\mathrm{a}+5-\mathrm{V}$ power supply, and within about a volt of both power-supply rails when using a $+15-\mathrm{V}$ power supply. In addition, the LMC6482/84 can all drive $500-\mathrm{pF}$ loads, at a closed-loop gain of unity, without oscillating.
A good low-voltage single-powersupply application for the LMC6484 might be to form the heart of a micropower data-acquisition system running off a +3 -V battery. Two of the LMC6484's four op amps can form a very high-input-impedance instrumentation amplifier to monitor a low-level sensor such as a strain gage excited by the power supply. The instrumentation-amplifier's output drives a third op amp, which acts as the input stage of a sample-andhold amplifier, whose output can easily charge a hold capacitor with a value of up to 100 pF . The IC's fourth op amp buffers the charge on the hold capacitor, taking full advantage of the device's low bias current. Each op amp's low output impedance is ideal for driving an analog-to-digital converter.
The silicon-MOSFET world is largely dominated by enhancementmode transistors, devices whose gates must be brought positive with respect to the source to turn them on. However, depletion-mode n-channel devices whose gates, like the grids of vacuum tubes, must be brought to a potential negative with respect to their sources to turn them off, can be used to do some interesting tricks, like the depletion-mode devices in the LMC6482/84 (Fig. 1, again). The pair operates as depletion-mode FETs for signals close to the plus power-supply rail, and as enhance-ment-mode FETs for signals close to the minus power-supply rail. This socalled soft-depletion, p-channel FET was developed by National Semiconductor's process engineers especially for the company's double-polysilicon analog CMOS process, on which all their CMOS op amps are made.

A folded-cascode circuit consisting of FETs $\mathrm{M}_{3}$ and $\mathrm{M}_{4}$ was chosen for the second section of the input stage (Fig. 1, again). It provides simple level shifting and the near powersupply rail-to-rail biasing required by the first section of the circuit. The output stage consists of two large complementary, common-source connected, n- and p-channel FETs driven in a push-pull manner. Output swing is limited by the transistor's transconductance and the minimum load resistance.

An oscilloscope trace represents the best indication of the ability of the LMC6482/6484 to handle CMVs beyond the op-amp's power-supply rails (Fig. 2). The op amp is connected as a unity-gain follower and runs off a single $+10-\mathrm{V}$ power supply. A sine wave whose peaks swing from 1 to +11 V is applied to the input and the output clips cleanly at 0 and +10 V. The smooth transitions in the output, shown coming off the powersupply rails, indicate that when overdriven, the op amp recovers quickly without any aberrations in the waveform. That is, the output waveform can be laid over the input waveform, both of which coincide over the complete linear operating range of the device from ground to the $+10-\mathrm{V}$ power-supply rail.

## Price And Availability

The LMC6062, LMC6082, LMC6482, and LMC6484 are rated for operation from $40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ and for the military-temperature range. In quantities of 100, pricing ranges from $\$ 1.70$ to $\$ 7.60$ each for the LMC6062, and $\$ 1.60$ to $\$ 7.50$ each for the LMC6082, depending on temperature version and package type. In the same quantities, the LMC6482 is priced at $\$ 1.65$ and $\$ 3.30$ each for industrial- and military-temperature-range versions, respectively; the LMC6484 is priced at $\$ 2.40$ and $\$ 4.94$ each for industrial- and military-temper-ature-range versions, respectively. Samples of the LMC6482/84 are available now and full production will start by June.
National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95052-8090; Bettina Briz, (408) 721-2274.

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# HaRDWARE EmULATOR SUPPORTS AlL TyPES OF DESIGN STYLES 

Synchronous, nonsynchronous, and asynchronous designs are all supported in RPMplus, Quickturn's fourth-generation hard-ware-emulation system. The product is based on a technology the company calls Precision Emulation, which helps automate design-mapping. Precision Emulation technology works through the Precision-Prototype-Synthesis and Timing-Sensitive-Partitioning algorithms. These algorithms enable users to precisely control emulation timing to deal with the asynchronous portions of designs.

Engineers can use RPMplus to emulate designs of up to 50,000 gates. If more gates are needed, RPMplus is compatible with Quickturn's mRPM products that emulate up to 1 million gates. In addition, new CAE interfaces let users automatically transfer data from Mentor Graphics and Verilog databases to the RPMplus emulator. This eliminates the need to use ASIC-vendors tools to generate an emulation net
list for each design change.
The tight integration with the Mentor and Verilog simulation environments makes it easier to use hardware emulation for accelerating functional verification before in-circuit emulation. Users can apply simulation test vectors and compare results without leaving their familiar simulation environment. In the Verilog environment, the portion of the design configured in the RPMplus can be cosimulated with the rest of the design being simulated in software. Consequently, system validation can take place at the software level before users create a hardware prototype for in-circuit emulation.

RPMplus runs under X-Windows and can be used in existing HP/Apollo, IBM, and Sun environments. Production shipments begin this month. The base price for the RPMplus 50,000 -gate system is $\$ 175,000$.

Quickturn Systems Inc., 325 E.
Middlefield Rd., Mountain View,
CA 94043; (415) 967-3300. बांGIF 460

- LISA MALINIAK


## VHDL Simulator Runs FASTER WITH LESS MEMORY

Features of Version 4.0 of the VantageSpreadsheet VHDL simulation system include faster compiler speed, a $50 \%$ reduction in memory requirements, and a C interface to other design tools. Also new is a code-coverage tool that grades test stimulus, the Concurrent Compiler for distributed VHDL-code compilation, and a new back-annotation tool called the Generic Loader.

Version 4.0 is twice as fast as the previous version of Vantage's simulation tools for simulating and compiling at the gate level. For complex behavioral models, simulation and compilation are improved by up to a factor of five.

A new code-coverage tool is essentially a VHDL equivalent of the toggletest found in older simulators, which helps engineers grade test stimulus by checking that each source path in the code was exercised. It improves model testing by counting the number of times each line of code is executed, and also counting the number of events on each signal.

A major enhancement for VantageSpreadsheet is the Concurrent Compiler, a parallel version of Vantage's VHDL compiler that distributes compilation tasks across an HP or Sun network using an intelligent partitioning system. The compiler system has robust errorrecovery capabilities, including the ability to retarget faults automatically if a network or machine problem occurs. Compiling portions of a job in parallel can reduce overall project compilation time by a factor of ten or more.

The Generic Loader loads generic timing information from a test file at a rate of 100,000 parameters $/ \mathrm{min}$. In addition, the simulators don't have to stop to complete the loading of a new generic set, which allows users to quickly switch from best, worst, or nominal conditions. Pricing for VantageSpreadsheet 4.0, which runs on Unix workstations, starts at $\$ 44,000$ per copy.

Vantage Analysis Systems Inc.,
42808 Christy St., Suite 200, Fre-
mont, CA 94538; (510) 659-
0901. GIVGIF 461

- LISA MALINIAK


## PCB TOOL CALCULATES Manufacturability

PCB Design for Assembly, a PC-based software tool, analyzes the cost of pcboard component assembly, and provides indices reflecting the manufacturability of the board. The tool reduces design-cycle time and cost-tomanufacture by enabling users to

generate manufacturable design alternatives in minutes. Jointly developed by Texas Instruments and Boothroyd Dewhurst, PCB Design for Assembly assists users in five critical board-design areas: placement and density analysis, height analysis, auto-insertion analysis, quality and labor analysis, and cost analysis. In addition, a librarymanagement feature filled with indus-try-proven components helps users identify part types. PCB Design for Assembly is shipping now. Site licenses start at $\$ 9500$.

Boothroyd Dewhurst Inc., 138 Main St., Wakefield, RI 02879; (401) 7835840. HIRGIF 462

## BUILDING-BLOCK LIBRARY INCLUDES LARGE CORES

Version 1.2 of the Soft-Design library of synthesizable architectures includes versions of the 8051 microcontroller, the 2900 series of bit-sliced microcontrollers, and a multiplier macro-function group. The architectures are actually Verilog or VHDL representations of complex parts used by ASIC and system designers as core building blocks in their high-level design descriptions. After the high-level design is verified, these building blocks are synthesized using industry-standard synthesis tools. The Soft-Design toolkit is offered in Verilog or VHDL for use with Cadence, Mentor, Synopsys, or Vantage simulation and synthesis tools. The architectures are provided in source code, along with a test validation suite, synthesis scripts, data sheets, and documentation. Call the company for pricing and availability.

[^13]
## DESIGN MIXED-SIGNAL ASICS WITH ONE T00L

Engineers can use Path Programmable Logic (PPL) version 5.0 to design both the analog and digital portions of a circuit. PPL's physical context-switching capabilities allow it to change rules, libraries, and constraints based on area definitions. In addition, version 5.0 incorporates the WYSIWYG (what you see is what you get) operation that has made desktop publishing easy to use. Users define a physical boundary between analog and digital sections of a circuit that causes the tool to switch to new libraries and rules for the respective areas. Then the software can interconnect elements across the boundary. The standard PPL ASIC package includes design entry, extraction, mixedsignal simulation, layout generation, schematic generation, and libraries for Mosis or Foresight shared-silicon services. PPL version 5.0 runs on PCs, and is shipping now for $\$ 14,500$. A Sunworkstation version is also available.
Bonneville Microelectronics Inc., 1399
S. 700 E, Suite 10, Salt Lake City, UT 84105; (801) 467-4698. HIRGI 464

## 44 NEW M0DELS EXPAND SIMULATION LIBRARY

Analogy has added 44 popular a-d converters to its simulation model library. These behavioral models, which include the AD 574 A , have been fully characterized by the company for use with Saber, its mixed-signal simulation tool. Analogy worked from complete component specifications from Analog Devices and Burr-Brown, so the models are accurately characterized for performance parameters. In addition, because the models are behavioral, simulation times are greatly improved over transistor-level models. Analogy is now shipping the a-d converter models as part of its library of more than 4500 analog and mixed-signal parts.
Analogy Inc., 9205 S.W. Gemini Dr.,
Beaverton, OR 97075; (503) 626-
9700. CIBGIF 465

## ASIC DELAY CALCULATOR DRIVES MANY SIMULATORS

An enhanced version of Mentor Graphics' TimeBase ASIC delay calculator now supports third-party logic simulators. TimeBase calculates design-specific timing delays based on design topology and layout parasitics. In the past engineers have had to develop and maintain a separate calculator for each
simulator they used. With TimeBase, however, they can support a diverse set of simulators, proprietary or third party, with one ASIC library. This allows tighter integration of third-party simulators with Mentor's Falcon Framework for concurrent design. The enhanced version of TimeBase will begin shipping by the second half of this year for $\$ 4900$. In addition, it will be included at no charge with purchases of Mentor's logic simulator, QuickSim II.

Mentor Graphics Corp., 8005 S.W. Boeckman Rd., Wilsonville, OR 970707777. GIVGIF 466

## UTILITIES SOFTWARE EDITS ORCAD SCHEMATICS

The SDT Utilities 1.0 software performs automated schematic editing and annotation of OrCAD SDT schematics. Engineers can locate signals

quickly with a function that annotates the schematic with the source- and des-tination-sheet numbers of all off-sheet signals. In addition, they can use the program's language to build commands that perform editing operations on any sheets in a schematic design. These commands may include titleblock changes, reference-designator changes, part-field entry, and deleting objects. SDT Utilities 1.0 runs on PCs. It's shipping now for $\$ 99$.

Robertson Engineering, 3721 Arlen Ct., San Jose, CA 95132; (408) 9461200. GIBGIF 467

## Create Logic Models FROM SPICE NET LISTS

Engineers can automatically generate ASIC-cell functional models from Spice net lists with the spice2logic software. Model creation starts with a Spice net list of a CMOS cell, a side file describing model attributes, and a golden simulation environment, such as Verilog. Spice2logic transforms the Spice file into a switch-level representation that's exhaustively simulated. The simulation results are then used to synthesize the functional behavior of the CMOS cell, which is stored in an intermediate description file called Cell Description Format (CDF). The tool uses the CDF
to fabricate functional simulation, synthesis, and timing-analysis models that represent the exact behavior of the Spice net list. Users can create Ikos, Mentor, OrCAD, Synopsys, Verilog, and Viewlogic models. The spice2logic software runs on Unix workstations. Pricing starts at $\$ 17,500$ for the core product with one model generator. Additional generators cost $\$ 10,000$.

SimQuest Corp., 3235 Kifer Rd., Suite 300, Santa Clara, CA 95051; (408) 7397582. GIIGIF 468

## FPGA LAYOUT T00LS COMPLETE MOST DESIGNS

An improved version of the NeoRoute tools for the physical layout of Xilinx FPGAs increases design-completion rates and reduces net delays. In addition, NeoRoute is three to five times faster than Xilinx routines, requires fewer place-and-route iterations, and almost eliminates clock-skew problems in Xilinx 3000 devices. The Xilinx-version of NeoRoute is a subset of FPGA Foundry, a device-independent CAD toolset for FPGAs. NeoRoute is available now. It runs on 80386- and 80486based PCs under MS Windows, and on Unix-based workstations running XWindows and Motif. The PC and workstations versions cost $\$ 7500$ and $\$ 12,000$, respectively.

NeoCAD Inc., 2585 Central Ave., Boulder, CO 80301; (303) 442-9121.
GITGIF 469

## VHDL PRICE TAG REDUCED FOR FIRST-TIME USERS

The VHDL Consulting Group has significantly reduced the price of its Std DevelopersKit software package so that any VHDL-model builder can afford it, even for demonstration projects. Because first-time users need a low-cost entry point to VHDL, the company offers the package at $\$ 9200$ for a site-wide source-code license that includes more than 40,000 lines of VHDL code and extensive documentation. The Std DevelopersKit is made up of five VHDL subroutine packages that supply a foundation to build simulator-independent models. In addition, the kit includes Std__ModelSpec, a VHDL model-development guidebook packed with the years of model-writing experience. The Std_DevelopersKit is shipping now. Licenses are also available on a division- or corporate-wide basis for $\$ 25,000$ and $\$ 50,000$, respectively.

VHDL Consulting Group, 974 Marcon Blvd., Suite 260, Allentown, PA 18103;
(215) 266-9791. GIBGIF 470

## Batteries

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Nonvolatile random access memory doesn't need batteries anymore. It doesn't need an extra chip either. All it needs is this. The nvSRAM from Simtek.

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We think you'll find our nvSRAM is well suited to applications ranging from cellular phones to the most advanced military hardware. To prove it, we'll send you a free design kit. And we guarantee you'll get it within 48 hours of your request. So call Simtek at 1-800-637-1667 right now for your free design kit (For production quantities, call your local Arrow/Schweber Electronics branch). And find out why, when it comes to nonvolatile RAM, batteries are dead.

## CHIP Integrates Four Digitally CONTROLLED POTENTIOMETERS

The X9241 Quad E ${ }^{2}$ POT from Xicor contains four digitally controlled resistor arrays, each composed of 63 resistive elements connected in series. Sixty-four taps located between each element and at the ends of each array are accessible to the wiper elements, whose position is controlled by the user through a two-wire serial-bus interface. Each resistor array has an associated wiper counter register and four 8 -bit data registers that can be directly written and read by the user. In addition, the contents of the data registers can be transferred to the wiper counter register to position the wiper. The current wiper position can be transferred to any one of its associated data registers.

Mask-programmable resistance values range from 2 to $20 \mathrm{k} \Omega$. The resistor arrays can be cascaded to form resistive elements with 127,190 , or 253 taps,
for a total resistance value of $500 \Omega$ to $200 \mathrm{k} \Omega$, depending on the mask-programmed resistance values. The X9241 supports a bidirectional bus-oriented protocol that defines the origin and destination of any traffic on the bus. Each direct-write cell consists of 16 bytes of $\mathrm{E}^{2} \mathrm{PROM}$ memory, and each register has an endurance of 100,000 write cycles and 100-year data retention.

In thousands, the 20 -pin plastic DIP version costs $\$ 4.00, \$ 4.40, \$ 7.00$, and $\$ 15.12$ for the commercial, industrial, military, and MIl-STD-883 temperature ranges, respectively. Pricing for the 20 pin SOIC package is $\$ 4.80$ and $\$ 5.25$ for the commercial and industrial temperature range, respectively. The chip is sampling now with production quantities available in the second quarter.

Xicor Inc., 851 Buckeye Ct., Milpi-
tas, CA 95135-7493; (408) 432-
8888. CHIGLE 471

- MILT LEONARD


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## EEPR0M-BASED LOGIC ICS DELIVER FPGA DENSITIES

The first in a family of electrically erasable programmable logic chips, the pLSI 1032-80 supplies the highest gate count- 6000 gatesof any EE-based field-programmable gate array. Lattice, which introduced the chips last year (Electronic Design, June 27, 1991, p. 137), has improved the chips' performance.

Now the EEPROM logic chips can run with $80-\mathrm{MHz}$ clocks, rather than with $70-\mathrm{MHz}$ ones. The 1032 chip-originally the ispLSI32-will have three other family members- the 1016, 1024, and 1048 , which pack 2000,4000 , and 8000 gates, respectively. All four ICs come as either the pLSI-series and require a high-voltage external programming signal, or as the in-system programmable (ispLSI) series that can be configured (or reconfigured) with the 5-V power supply.

When running with system clocks of 80 MHz , the pLSI 1032 has an input-tooutput delay of just 15 ns . The logic consists of 32 generic logic blocks (GLB) in the 1032 (and 16, 24 or 48 blocks in the other chips). Each GLB has 18 logic inputs that drive a product-term array that, in turn, sends four outputs to the output macrocell. The macrocell contains a D flip-flop that has an Exclu-sive-OR input gate, and combinatorial logic. Additionally, the 1032 includes 192 registers, 64 I/O pins, 8 dedicated inputs, 4 dedicated clock inputs, and a global routing pool for interconnections.

The family will be supported by pDS, Lattice's development system for IBM 386/486-based PCs and compatibles in a Microsoft Windows environment. Also available is the isp engineering kit, which includes a chip, a programming module, cable, and power adapter . The pDS software and kit sell for $\$ 995$ and $\$ 395$, respectively. The 84 -pin pLSI 1032 comes in both 50 - and 80 MHz versions, and sells for $\$ 49$ and $\$ 81$ apiece, respectively, in thousands. Either speed grade of the chips is immediately available.

Lattice Semiconductor Corp., 5555 Northeast Moore Ct., Hillsboro, OR 97124-6421; (503) 681-0118.
GIBGIF 472
DAVE BURSKY

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# HIGH-SPEED SRAM 0FFERS Widest Data Path 

Packing the industry's widest data path for a static RAM-32 bits wide-the SDT8640 CMOS static RAM is the first of a family of wide-bus memories from Silicon Design Technology. The initial RAM, offered in a 32 -kword by 32 -bit organization, is an asynchronous memory with transparent address latches and the ability to operate with either $3-\mathrm{V}$ or $5-\mathrm{V}$ bus logic. Additional control lines on the chip include both active-high and active-low Chip-Enables, an OutputEnable, an Address-Latch Enable, and four Byte-Select lines so that the chip can perform single-byte writes.

There will be four speed grades of the SDT8640, with the first three consisting of the $15-, 17-$, and 20 -ns devices. A 12 -ns version is also in development. Slightly wider RAMs with 36 -bit buses ( 32 bits plus byte parity) are also in development, as are smaller-bus-width SRAMs with 18 - and 16 -bit buses, still other commodity fast SRAMs, and some CPU-specific SRAMs.

Housed in an 80-lead plastic quad-sided flat package with $0.8-\mathrm{mm}$ lead spacings, the SRAMs have common data input and output lines. The package also has many power and ground pins (two for every byte) and a separate output buffer power supply pin to minimize power-line noise. The chip can serve as a single-chip cache for processors in the


Intel X86 family. Its wide word size also suits the IC for RISC systems and communication controllers. When operating at maximum speed, the SRAMs draw from 240 to 400 mA ( 20 to 12 ns , respectively) from a 5 -V supply. Samples of the chips will be available in May; production is slated for August. The 15ns version sells for $\$ 50$ apiece in thousands; the $17-\mathrm{ns}$ chip is $\$ 40$ in similar quantities.

Silicon Design Technology, 39899 Balentine Dr., Ste. 200, Newark, CA 94560; Jeff Hall, (510) 651-
9343. GIIGE 474

DAVE BURSKY

## SBUS DMA CONTROLLER D0ES 32-BIT ADDRESSING

Extending the addressing capability to the full 32 -bit range of the SBus interface, the NIM618 DMA controller chip from Nimbus Technology can access any part of the 32 -bit address space. In contrast, the original L68453 SBus DMA control chip from LSI Logic has only limited 24 -bit addressing. The NIM618 is completely pin- and software compatible with LSI Logic's chip and can interface any type of peripheral that requires bus master DMA data transfers to the SBus-intelligent network and disk controllers, for example. Its $\$ 35$ price-apiece, in hundredssuits it for slave-only peripherals. Samples are available.
Nimbus Technology, 2900 Lakeside
Dr., Ste. 205, Santa Clara, CA 95054;
Spencer Greene, (408) 727-5445.
GIRGLE 475

## USE 64 BITS T0 D0UBLE VME PERFORMANCE

By using 64- rather than 32-bit transfers, VMEbus board makers can double performance without making changes to the backplane hardware. This can be done using the VIC64 VMEbus interface controller, a VME64-compatible bus interface chip. By using the VMEbus' 32 -bit address bus for data during its frequent idle periods, designers can increase system performance by implementing 64-bit transfers at 70 Mbytes/s. The chip, from Cypress Semiconductor, is compatible with the company's VIC068 pin-out and with software for the VIC068. In hundreds the chip sells for $\$ 140$ each; 144-lead PGAs and 160-lead plastic quad flat packs are available.
Cypress Semiconductor Corp., 3901
North First St., San Jose, CA 95134;
(408) 943-2600. GThGIF476

## Megacell Cores Ease C0MPLEX ASIC DESIGN

By adding complex predesigned functions-"CoreWare"-to its standard-cell library, LSI Logic eases designing systems on a chip. CoreWare cells consist of large functions like RISC microprocessors and related support functions like di-rect-memory-access control, blocks of RAM or ROM, SCSI disk controllers, DSP functions, and custom-created

blocks. Predesigned and pretested blocks means designs can be completed faster and with fewer errors.
Some of the major cores that are currently available include the CW33000 RISC CPU core based on the R3000 microprocessor from Mips Computer Inc., the companion CW3230 read/write buffer, the CW900 embedded SPARC processor, the CW853A SBus DMA controller, along with a multiprocessor bus interface. High-speed math blocks such as pipelined and non-pipelined 32bit ALUs, multipliers, and dividers, as well as non-pipelined 64 -bit ALUs and multipliers. For military projects, LSI also offers the CW1750A 16-bit CPU.

All CoreWare cells are fully compatible with the company's MDE design environment and submicron CMOS processes. The large cells are supplemented with a library of over 1000 macrocells and other large building blocks. Pricing is based on an access fee to the CoreWare blocks (minimum of $\$ 25,000$ ) plus an engineering charge (minimum of $\$ 30,000$ ), production costs and package requirements.

LSI Logic Corp., 1551 McCarthy Blvd., Milpitas, CA 95035; Thomas Harington, (408) 954-4875.
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## 4-GSAMPLE/S SC0PE B0ASTS 1.5 MHz BANDWIDTH

Designers of systems with clock rates to 100 MHz and edge speeds below a nanosecond will find the HP 54720A 4-Gsample/s, 2channel oscilloscope to be a valuable debugging tool. The scope accurately reconstructs signals with $1-\mathrm{GHz}$ of real-time bandwidth and $1.5-\mathrm{GHz}$ of equivalent-time bandwidth, which is enough to examine the overshoot and ringing found in fast digital circuits.

The unit supplies 8 -bit vertical resolution and $1 \%$ vertical gain accuracy. Time-interval accuracy is better than 30 ps , and memory depth is 32 ksamples on 2 channels and 16 ksamples on 4 channels. The scope can trigger on logic bits, timed logic patterns, or glitches as narrow as 500 ps .
The scope's modular signal-conditioning section allows users maximum flexibility and, together with a built-in disk drive and flash ROM, permit future upgrades with new hardware or application-specific software. For example, users can configure the quad 2Gsample/s analog-to-digital converters for 2 channels at 4 Gsamples/s or 4 channels at 2 Gsamples/s.

An optional active probe, the HP 54701 A , features $1 \%$ flatness over 2.5


GHz. The probe's input capacitance is only 0.6 pF and its input resistance is $100 \mathrm{k} \Omega$. The HP 54701 A draws its power from the scope but can also be used with the HP 1143A power supply.

The 4-Gsample/s, 2-channel HP 54720A mainframe costs $\$ 42,900$, and a 2-Gsample/s, 2-channel version, the HP 54710 A , costs $\$ 29,900$. Modules range in price from $\$ 2400$ to $\$ 4700$ for the 4 -Gsample/s, $1-\mathrm{GHz}$ amplifier. The HP $54701 \mathrm{~A} 2.5-\mathrm{GHz}$ active probe costs $\$ 2300$. Delivery is estimated at 16 weeks.

Hewlett-Packard Co., 19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900. GLVGIF 478

- JOHN NOVELLINO


## VXI MODULE MEASURES POWER T0 100 GHZ

A one-slot C-size VXIbus module measures power levels from $100 \mathrm{pW}(-70$ dBm ) to 7 W . Sensors are available to make measurements from 100 kHz to 100 GHz . The Model 4052 power meter may be ordered with from one to four channels, all housed in the same size module. Calibration requires only one bus command, which stores the results in an on-card battery-backed memory. To ensure measurement integrity, the module features additional stabilization and noise-rejection circuitry in a fully shielded housing. The meter can be used with microwave sweepers, a frequency counter, and appropriate directional couplers to form a low-cost scalar network analyzer. With additional sensors the setup can make simultaneous return loss measurements. The Model 4052 costs $\$ 3750$ and is available with delivery in 6 weeks.

Racal-Dana Instruments Inc., 4 Goodyear St., Irvine, CA 92718; (800) 7223262. GIRGIF 478

## POWER MeTER MAKES MULTIPLE MEASUREMENTS

An easy-to-use precision, single-phase power analyzer makes many power-related measurements including true power, harmonics, power factor, and voltage and current crest factors. The PM1200 performs autoranging peak voltage and current measurements from 2 to 1000 V and 10 mA to 175 A . The meter also makes direct readout measurements of harmonics (phase and angle) and total harmonic distortion to the 50th harmonic and crest factor to 19.9. Basic accuracy is $0.25 \%$, even for distorted waveforms. Readings are made over a range of dc to 50 kHz . The PM1200 comes in benchtop or half-rack versions, and includes IEEE488, RS-232C, Centronics printer, and analog chart recorder interfaces. The bench version costs $\$ 5950$ and the rackmount version $\$ 6170$. Delivery is from stock to 4 weeks.

Voltech Inc., 200 Butterfield Dr., Ash-
land, MA 01721; (508) 881-7329.
GIVGIF 481


You're in the initial stages of design. You need a prototype and you're facing a deadline. You also need a power supply with specific voltage/current outputs. And you need it fast!

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# ANALOG/DIGITAL SCOPES OFFER SPEED, CHANNEL CHOICES 

Afamily of oscilloscopes offers users a wide range of choices for varying applications. The scopes operate in analog and digital modes and come in $100-\mathrm{MHz}$ and $200-$ MHz versions with a choice of full 4channel or 2+2-channel operation.
The two pairs of scopes, the PM 3382/84 and PM 3392/94, combine the ease of operation and real-time 100 - or $200-\mathrm{MHz}$ bandwidth of an analog instrument with a digital sampling rate of 200 Msamples/s. Users can take advantage of the "live" signal representation and infinite resolution of the ana$\log$ mode for applications that require such capability. Or they can quickly switch to the digital mode, which offers an extensive set of built-in automated voltage and timing measurements. Direct access control eliminates the need for menus.

Triggering modes include logic-state and pattern triggering, and glitch triggering down to 2 ns . Besides pre- and post-trigger display, the instruments allow event delay and time-after-event
delay. The acquisition memory can store 32 ksamples. A unique Touch Hold and Measure feature lets users initiate a measurement by pushing a probe-mounted button.
The PM 3384 and PM 3394 are true 4channel scopes. That is, all four channels provide full sensitivity with complete attenuation ranges on each channel. The $2+2$ versions have limited sensitivity on the two additional channels.

A comprehensive Math+ option performs more complex calculations, like integration, differentiation, template testing, and FFTs. An optional IEEE488.2 (GPIB) interface permits full remote programmability using the Standard Commands for Programmable Instruments. A serial printer-plotter interface is standard.
The $100-\mathrm{MHz}$ PM 3382 and PM 3384 cost $\$ 4490$ and $\$ 5490$, respectively. The $200-\mathrm{MHz}$ PM 3392 and PM 3394 are priced at $\$ 5990$ and $\$ 6490$, respectively.

John Fluke Mfg. Co. Inc. P. O. Box 9090, Everett, WA 98206; (800) 443 5853. GIIGIF 481

- JOHNNOVELLINO


## Fast Testers Handle Up T0 64 DRAMS IN PARALLEL

Apair of memory testers with excellent speed and accuracy capabilities are the first members of the J990 series of memory test systems. The systems also offer a high degree of parallel test capability.
The J997 is a general-purpose highperformance memory tester well-suited for engineering and wafer test. Maximum operating frequency is 200 MHz , and overall timing accuracy is 300 ps . The J997 can test 32 DRAMs in parallel on two test stations. The J994 is optimized for final test of packaged devices, with a capacity of 64 DRAMs in parallel. The system's maximum operating frequency is 120 MHz , and overall timing accuracy is 500 ps .
The new testers are the first to use Tester-per-Site, a proprietary architecture evolved from the pin-slice concept used in Teradyne's VLSI test systems. This architecture gives the J990 series the flexibility and speed needed to test multiple wide-width DRAMs and specialty memory devices in parallel. Con-
ventional shared-architecture testers cannot deliver the accuracy and site-tosite correlation that IC manufacturers need.

The Tester-per-Site architecture applies a complete set of parallel electronics to each pin of the devices to be tested in parallel. For example, one set of pin electronics is assigned to pin 1 of each device, and another set is dedicated to pin 2. The systems include Teradyne's patented E/MOS design, which takes advantage of the high-performance of ECL technology in the critical timing circuitry and employs the economy and reliability of CMOS in other, less sensitive areas.

Prices for a J997 single-station system configured for engineering start at about $\$ 1$ million. A J994 system for production costs from $\$ 1$ million to $\$ 1.5 \mathrm{mil}-$ lion, depending on configuration.

Teradyne Inc. Semiconductor Test
Div., 30801 Agoura Rd., Agoura Hills, CA 91301; (818) 991-2900.

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JOHN NOVELLINO

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25.3 FLA, 110 LRA

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20A @ 28VDC

Expected Life
300K operations 100K operations 100K operations 100K operations 100K operations 100K operations

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## RISC-Based Plotter Produces C-SIze Drawing In Under 5 Min.

To get high-quality C-size plots, users typically had to spend $\$ 7000$ to $\$ 15,000$ for a laser or thermal printer. Now, with the ProTracer, from Pacific Data Products, they can get those plots for just $\$ 1499$. The ProTracer combines an Intel 1960 embedded RISC processor and a highperformance Canon ink-jet engine to produce final-quality drawings in less than 5 min .
The ProTracer offers 360- by $360-$ dots/in. output to print crisp lines and

smooth curves. Area fills are solid with no bonding or streaking. For check plots, the plotter can be placed in a high-speed, low-resolution mode. It supports commonly used media such as plain and bond paper, plotter paper, and vellum. Two optional sheet feeders can feed A-and B-size cut-sheet paper or business-size envelopes automatically. The plotter can also be used for laser-quality office documents on standard paper. It easily fits on any desktop because of its small footprint.

By adding HP-GL and PostScript emulation cards, users can customize the printer to match a specific software application. Adding 2 Mbytes of memory and an HP-GL cartridge costs an extra $\$ 500$. A PostScript card and 8 Mbytes of memory costs $\$ 1398$. The ProTracer and its accessories will be available in April.

Pacific Data Products, 9125 Rehco Rd., San Diego, CA 92121; (619) 5520880. GIBGIF 483

- RICHARD NASS


## DESKSIDE FAMILY IS BASED ON MIPS R4000

The Iris Crimson family of deskside computer systems from Silicon Graphics is based on the Mips R4000 64-bit RISC microprocessor. Starting below $\$ 28,000$, the family includes seven models that span a full range of graphics capabilities.

Binary compatible with the company's line of Iris 4D workstations and servers, the family incorporates the $50-$ MHz R4000SC, delivering 70 SPECmarks of performance. The R4000SC, the fastest version of the R4000, offers balanced floating-point and integer performance and tightly integrated support for a large secondary cache, a critical element of the systems' performance. The processor contains an internal clock rate of 100 MHz , achieved through superpipelining. This technique breaks each instruction into tasks, allowing several tasks to be handled by one clock cycle.

By maximizing ASIC technology, the Crimson family can achieve memory transfer rates of $400 \mathrm{Mbytes} / \mathrm{s}$. This tight coupling of the compute and memory subsystems, combined with a sophisticated two-level caching scheme, reduces the long wait states typically
associated with CPU access to main memory.
The seven models of the family include the S, the Entry, the XS, the XS24, the Elan, the VGX, and the VGXT. The S is the base system, while the Entry adds some entry-level graphics capabilities, suitable for X-Windows and 2D or 3D vector applications. The XS supplies an optional hardware Zbuffer and a Geometry Engine graphics processor to increase polygon performance and the XS24 adds 24 -bit plane color. The Elan includes the hardware Z-buffer and Geometry Engine.

The VGA includes the Silicon Graphic's PowerVision graphics to deliver the fast polygon performance, hard-ware-assisted antialiasing, and tex-ture-mapping capabilities. The VGXT delivers the company's top-of-the-line graphics performance.

All the systems include up to 256 Mbytes of memory, 3.6 Gbytes of internal disk storage, two SCSI channels, and four VME slots.

[^14]

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## New 14-Bit, 5.12MHz Sampling ADC Delivers -88dB SFDR



## Clearer, Cleaner Signals

ADC614 is a complete two-step subranging subsystem containing an ADC, sample/hold, voltage reference, timing and error correction circuitry. Packaged in a compact 46-pin DIP, the hybrid's excellent wideband linearity allows 14-bit performance with a Nyquist spurious-free dynamic range of -88 dB (typ). It's an excellent choice for spectral analysis in radar, medical, and digital receiver applications. The device dissipates just 6. IW and is specified for $0 /+70^{\circ} \mathrm{C}$. Logic is TTL.

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ADC614 is pin-consistent with Burr-Brown's 12-bit ADC603 family. Speed and dynamic range trade-offs can be made by simply plugging in an ADC614, ADC603 or ADC604. Insuring the highest performance, "KH" units are not only thoroughly DC and AC tested, but they're also shipped with free test data summaries.

## Key ADC614

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CIRCLE 253 FOR RESPONSE OUTSIDE THE U.S.
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## LaSER-DIODE M0DULES PuMP Data Through Fiber Pipes

$T$wo types of laser-diode modules from Mitsubishi Electronics America are designed for longdistance data-transmission systems. The $1480-\mathrm{nm}$ FU-622SLD-1 pump-laserdiode module is for use in long-haul, er-bium-doped fiber amplification (EDFA) systems. The module provides continuous output for optical pumping in undersea and terrestrial long-distant EDFA transmission. Typical output power is 45 mW with an rms spectral width of 10 nm . The module includes a built-in thermoelectric cooler. Samples are available for $\$ 10,000$ each.

For Sonet and other high bit-rate applications, Mitsubishi's FU-68SDF-2 multiple-quantum-well laser-diode module transmits data at a rate of 2.5 Gbits/s over distances greater than 70
km without a bit-error-rate floor. The spectral width is typically 0.2 nm , and typical side-mode suppression is 40.0 dB. The input of the single-mode fiberpigtail module is impedance-matched to $25 \Omega$. The device has a built-in thermoelectric cooler, and an optical isolator limits noise to $-155 \mathrm{~dB} / \mathrm{Hz}$.
The laser diodes' minimum output power is 2 mW ; minimum cutoff frequency is 3.5 GHz , and maximum rise and fall times are 150 ps . Typical lightemission central wavelength is 1550 nm . Packaged in a standard butterfly housing, the laser diode module sells for $\$ 9000$ each.

Mitsubishi Electronics America,
Ltd., 1050 E. Arques Ave., Sunnyvale, CA 94086; (408) 730-5900 Chider 483

- MILT LEONARD


## SLIC CUTS STANDBY POWER, DEVICE COUNT

A two-chip subscriber line interface circuit (SLIC) kit offers low dissipation in the standby mode and high integration. Aimed at applications in central offices, PABXs, digital key systems, terminals and multiplexers, this kit from SGSThomson Microelectronics consists of the new L3092 SLIC control unit and the company's existing L3000 highvoltage SLIC line interface IC.

The two ICs integrate all functions of a subscriber line interface, including ringing signal rejection, a function typically performed by external circuits. This contributes to a low component count.

Another important benefit is the greatly reduced dissipation in stand-by-less than 50 mW with signaling functions active. This is important in central office and PABX applications where lines are in the standby state most of the time.

The L3092/L3000 SLIC can also measure the length and conditions of the line so that the card can choose an appropriate feeding scheme. For example, in the case of short loops, the battery feed can be reduced to limit dissipation, and the coefficients can be modified to optimize matching. Comprehensive development support is provided by evaluation boards, software, Spice models and detailed application notes to make application development fast and simple.

Available now, the two-chip SLIC kit sells for about $\$ 14$ apiece in quantities of 100 .

SGS-Thomson Microelectronics, I20041 Agrate Brianza, Via C. Olivetti 2, Italy. Contact: Maria Grazia Prestini; phone (00) 39396035597.

## GTiBIF 486

## SI MODULUS DEVICES OUTPERFORM GAAS

A line of silicon modulus divider ICs can outperform gallium arsenide devices in communication and instrumentation applications. The five devices in the SP8900 series have ratios of $2,4,8$, 10 , or 16 . An "A" grade option guarantees $5.5-\mathrm{GHz}$ operation at $-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ and 5.0 GHz over $-55^{\circ}$ to $+125^{\circ} \mathrm{C}$, while the B grade option guarantees 5.0 GHz at $-40^{\circ}$ to $+85^{\circ} \mathrm{C}$, the company says. The devices fabricated on the company's 14$\mathrm{GHz} \mathrm{F}_{\mathrm{t}}$ HE bipolar process.

Input sensitivity is -2 dBm and does not require pre-amplification for typical GaAs parts, the company says. GPS also claims they use less power than gallium arsenide devices, at 350 mW from a single $5-\mathrm{V}$ supply. Noise floor for the dividers is typically $-144 \mathrm{dBc} /$ Hz at 5 GHz . The 1000 -unit price for the B grade dividers is $\$ 33$ in eight-pin ceramic, dual in-line packages. A grade price is $\$ 57$.

GEC Plessey Semiconductors, Cheney Manor, Swindon, Wiltshire, SN2 2QW, UK; + 44 (0)793 518411. GIRGIF 487

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## Dual, CONTINU0US LOW-PASS Filter Is Programmed Digitally

Sswitched-capacitor filters that are digitally programmable are noisy while time continous (CT) filters are quiet, yet not easily programmed by a microprocessor. Now Maxim's MAX270 IC contains a pair of CT low-pass filters on a single chipand their cutoff frequencies are digitally programmable. Writing a 7 -bit word to each of the MAX270's two memory addresses sets the cut-off frequency $\left(\mathrm{C}_{\mathrm{f}}\right)$ of each of its second order SallenKey, Chebyshev filters to one of 128 frequencies between 1 kHz and 25 kHz .

Alternatively, for fixed $\mathrm{C}_{\mathrm{f}}$ operation, pin-strapping can replace the programming. $\mathrm{C}_{\mathrm{f}}$ resolution is best shown by giving examples of sets of adjacent $\mathrm{C}_{\mathrm{f}} \mathrm{S}$ : $1 \mathrm{kHz}, 1.011 \mathrm{kHz} ; 1.605 \mathrm{kHz}, 1.635 \mathrm{kHz}$; $3.620,3.671$; 6.481, 6.645; and 22.826 $\mathrm{kHz}, 25 \mathrm{kHz}$.

Programmed $\mathrm{C}_{\mathrm{f}}$ accuracy typically runs $\pm 2.9 \%$ with $\mathrm{C}_{\mathrm{f}}$ set at 2.536 kHz ; $\pm 9.5 \%$ with $\mathrm{C}_{\mathrm{f}}$ set at 25 kHz . Gain within the pass band runs between -0.5 and -6 dB . These filters, plus their output

operational amplifiers, achieve a maximum total harmonic distortion (THD) of -70 dB while putting a $3.5-\mathrm{V}$ pk-pk $390-\mathrm{Hz}$ sine wave across $5 \mathrm{k} \Omega$ with $\mathrm{C}_{\mathrm{f}}$ set at 2.01 kHz . Similarly, spurious-free dynamic range (SFDR) runs a minimum of 70 dB . In its 20 -pin plastic DIP the MAX270 low-pass filter chip sells for $\$ 7.72$ in 1000-unit quantities.

Maxim Integrated Products Inc., 120 San Gabriel Dr., Sunnyvale, CA 94086; Steven Leandro, (408) 7377600. GTRGIF 488

FRANK GOODENOUGH

## SHAs Grab Four Fast Signals Simultaneously, In 900 NS MAX

Capable of simultaneously sampling four analog voltages, Datel's MSH-840 is aimed at applications in which the amplitude of multiple analog signals must be measured and measurements made virtually si-

multaneously. Measuring simultaneously is mandatory if the time or phase relationship between them is important. The four sample-and-hold amplifiers (SHAs) in the MSH-840 can each independently, and if directed simultaneously, acquire a $10-\mathrm{V}$ voltage
step to $0.01 \%$ accuracy in a maximum of 900 ns .

Once the voltage is acquired, if in turn the SHAs are simultaneously commanded into HOLD, the aperture delay for each is 60 ns maximum, and the aperature uncertainty 50 ns maximum. Thus all four samples will have been taken within less than 100 ns of each other. The MSH-840 also contains an output multiplexer followed by a buffer amplifier. Acquisition time for the SHAs includes that for the multiplexer. Minimum small-signal bandwidth runs 8 MHz , minimum full-power bandwidth, 300 kHz .

Two of the four channels can be given a gain of ten by the user. This unique feature adapts the MSH-840 for sampling the same voltage before and after analog signal processing, which may include gain. In OEM quantities the commercial grade MSH-840 goes for $\$ 224$ each; its military coounterpart sells for $\$ 244$ each.

Datel Inc., 11 Cabot Blvd., Mans-
field, MA 02048; Bob Leonard (508)
339-3000. EIRGIE 488
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## SINGLE CHIP DRIVES BIPOLAR STEPPER MOTOR

Containing on one chip all the circuitry needed to control and drive a two-phase bipolar stepper motor, the L6219 smart power IC from SGS-Thomson Microelectronics replaces two-chip solutions, making a compact motor drive.

The IC incorporates two bridge power stages rated at 750 mA plus two current control chopper circuits. The latter are of the fixed OFF time type, which minimizes current ripple and makes it possible to drive motors with low resistance.

Two logic inputs allow the output current to be programmed in four levels, permitting motor operation in the full-step and half-step modes. Moreover, by using an external D/A converter to vary the voltage applied to a reference voltage input, it's possible to micro step the motor.

The L6219 is housed in a 24 -lead DIP package, which is both compact and convenient for automatic assembly. Four leads conduct heat from the die to circuit board tracts; no other heat sinking is necessary. A PLCC-44 plastic chip carrier version will be introduced later in the year. Available now, the L6219 sells for $\$ 1.70$ apiece in quantities of 25,000 units.
SGS-Thomson Microelectronics, 100
East Bell Rd., Phoenix, AZ 85022; J.P.
Rossomme: (602) 867-6228. GIBGIF 490

## TRANSISTORS B00ST BASE STATION EFFICIENCY

Featuring input and output-matching networks optimized for 800 to 900 MHz and 900 to 960 MHz operation, respectively, the BLV101A and BLV101B RF power transistors are suitable for the driver and output stages of cellular radio base-station transmitters. Both transistors are high-gain, npn types de-
livering output power of up to 50 W at operating efficiencies exceeding $50 \%$.
The double-input and output matching networks integrated into the devices make designing the transistors in to RF circuits fairly easy. An implanted ballast resistor stabilizes their performance over a wide operating temperature range. Power gain for both types is a minimum of 8.5 dB for the 101 A and 7.5 dB for the 101B.

Devices are fabricated in a silicon planar epitaxial process. Gold metallization improves reliability. They are housed in a six-lead SOT273 flanged en-
 software support for all the popular languages. A software library and time saving utilities are included that make instrument control easier than ever before. Ask about our no risk guarantee.
capsulation with a ceramic cap. Samples of the BLV101A and BLV101B are available for about $\$ 70$ each. Production volumes can be delivered six weeks after receipt of order.

Philips Semiconductors, 2001 West Blue Heron Blvd., Riviera Beach, FL 33404-5099; Mirian Coleman: (407) 881-3257. GIBGIF 491

## Circuits 0fFER HighSpeed Switching

The closely controlled gain and switching specifications of a new line of 1500 V bipolar transistors allows designers to minimize the size and cost of heat sinks without compromising device reliability. Designed for horizontal linedeflection circuits for TV sets and CRT monitors, the BU2508A, BU2520A, and BU2525A transistors are intended for operation in applications with nominal collector current requirements of up to $4.5 \mathrm{~A}, 6.0 \mathrm{~A}$, and 8.0 A , respectively. The
larger devices are suitable for use in line-deflection circuits operating at line frequencies as high as 64 kHz and are available with or without an integral damper diode.

Fabricated in an advanced triple-diffused, mega-glass passivated process, the transistors have closely controlled switching parameters. The BU2508A, BU2520A, and BU2525A transistors are available in SOT199 and SOT93 plastic power packages. Delivery is six weeks after receipt of order. Prices are given on request.

Philips Semiconductors, 2001 West Blue Heron Blvd., Riviera Beach, FL 33404-5099; Miriam Coleman: (407) 881-3257. GIBGIF 492

## 75-W BENCH SUPPLY HAS KEYPAD CONTROL

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Kepco Inc., 131-38 Sanford Ave., Flushing, NY 11352; (718) 4617000. GliGIF 493


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## AUDIO COURSE TEACHES OS-9 ReALTTME OS

To help engineers become familiar with real-time multitasking programming, Gespac has produced a self-study audio course on Microware's OS-9 operating system. The complete package contains over five hours of audio material,

as well as 270 pages of documentation. An exercise disk lets the user implement the concepts detailed in the course. Examples on the disk can also be used as templates for writing application programs.
The course uses C as the primary language to interact with OS-9. It describes the operating system's basic operation, the structure of modules, and how to use signals, events, pipes, and data and subroutine modules. The material is hardware independent and is applicable to any OS-9 680X0-based platform. The course is available now for $\$ 595$.

Gespac Inc., 50 W. Hoover Ave., Mesa,
$A Z 85210$; (602) 962-5559. GIIGIF 494

## TRANSACTION SOFTWARE DOUBLES IN SPEED

Release 3.0 of Burr-Brown's TMV9000 transaction-processing software doubles the speed of earlier versions. The software performs real-time networked data-collection on Digital Equipment Corp.'s VAS/VMS-based computer systems. Users also get access to Rdb/VMS databases and ISAM files, which enhances the read, write, and append functions in earlier releases. An external programmer's interface affords access to system routines written in standard programming languages. TMV9000 release 3.0 offers connection through such interfaces as direct RS-423, DECservers, LAT, and polled RS-422; as a result, existing wiring can be used. Contact the company for price information.
Burr-Brown Corp., P. O. Box 11400, Tucson, AZ 85734; (602) 746-1111; fax (602) 889-1510. GIBGIF 495

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(T2) INTERNETWORKING
(T3) NETWORK MANAGEMENT

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## APRIL 27-29, 1992

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