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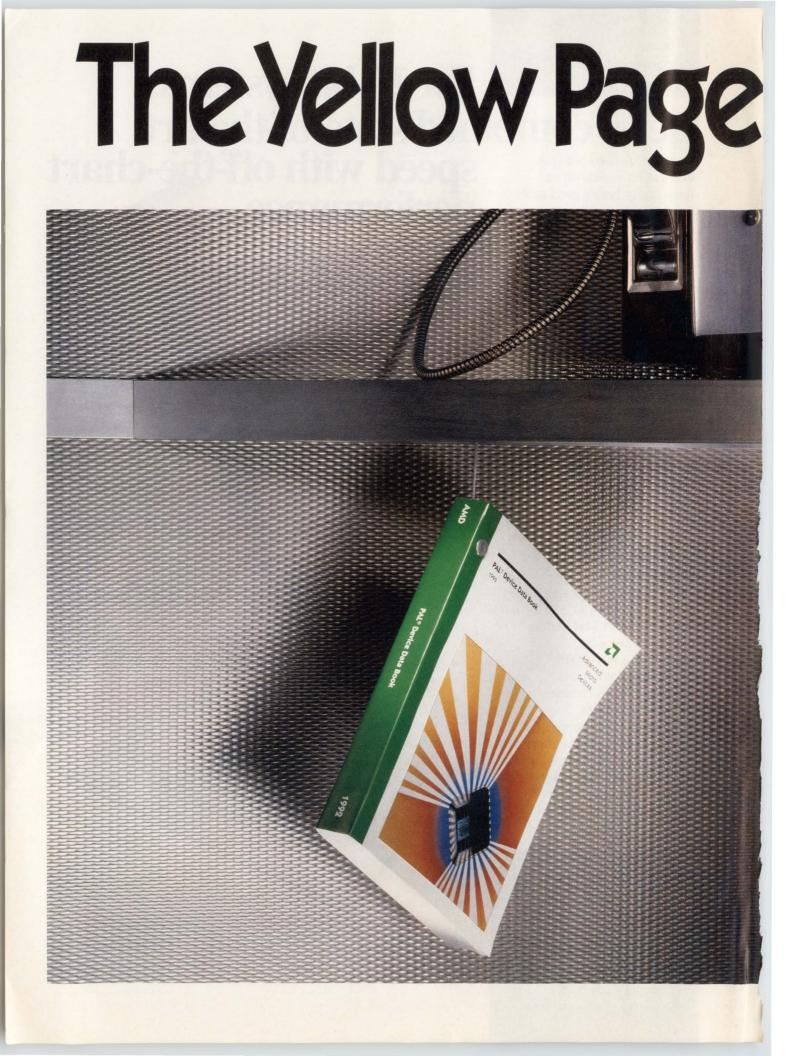
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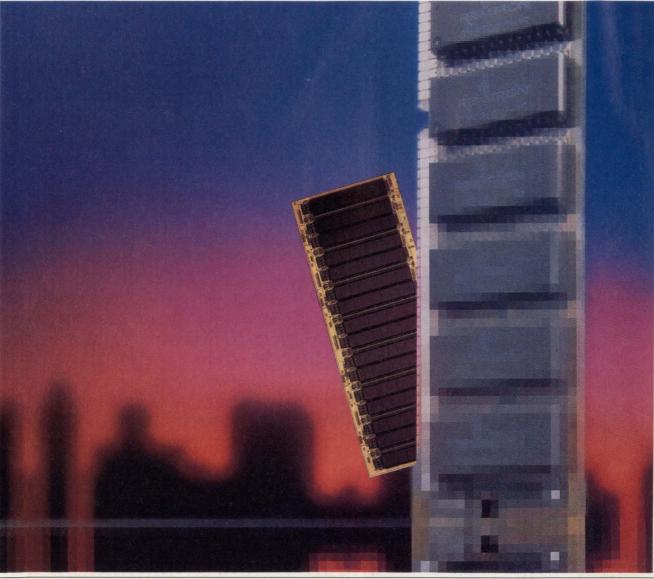
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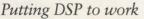
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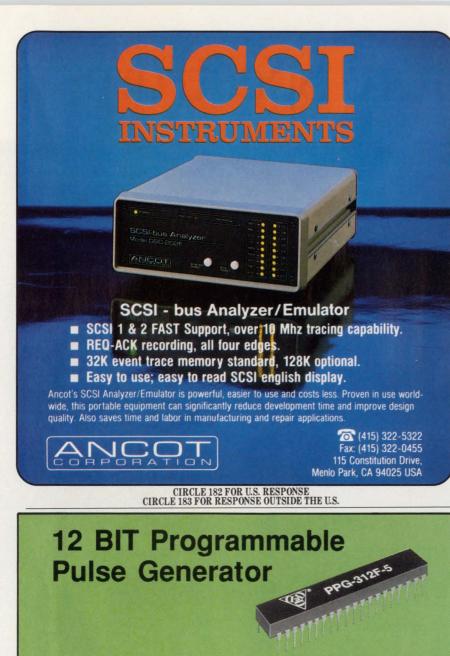


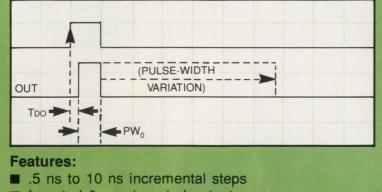
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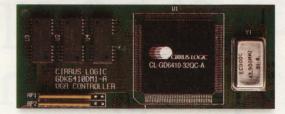
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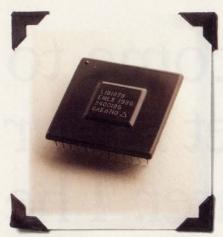


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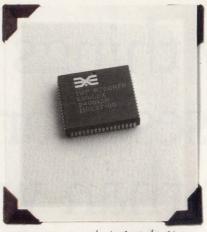
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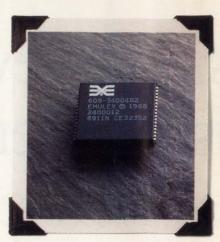
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1986 MAC 100. We introduce a combined disk formatter and buffer controller in a single disk controller chip.



1987. ESP 100. The inclustry's first high: parformance. SCSI chip is born at Emulex.



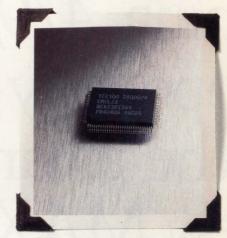
1988-ESP200, Second generation SCSI anives with SCSI-2 support and Parity Pass Through.



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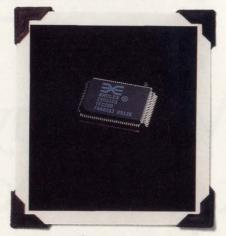
1989-BC200. A dynamic 4-Dort DMA controller for DRAMSis created.



1989-TEC.100. EMD combines disk, bubber, and SCSI controllers in a single chip.



1990-FAS 236. We delive the first Fast SCS1 chips with a 16-bit DMA Port.



1991-TEC 200, Our secondgeneration TEC becomes the industry's first Fast single-chip disk controller.



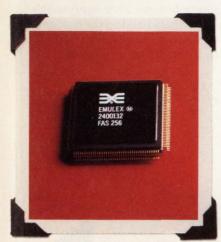
1991. TEC 256. The first Fast and Wide SCS1 click controller also Goasts the Eastest click data. nate and highest system bandwidth.



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EDITORIAL

NON-FACTS AND NEW FOUND FREEDOM

wo unrelated topics have captured our attention recently. First, here at home in New Jersey, engineers have that well-known feeling of "With friends like these, who needs enemies?" being stirred up once again. The state public television network is running a three-part special on a topic that just won't die, no matter what the facts might be: the supposed shortage of scientists and engineers.

As might be expected, the program's tone was set by a professor at a statesupported university, who dredged up the National Science Foundation's prediction of an engineering shortage early in the next century. The program also included comments from a panel that was hardly representative of working engineers: a personnel manager for a petroleum company, a high-school science teacher, a representative of a group encouraging more minorities in science and engineering, and a high-school senior planning to be an engineer. We agree with the importance of attracting more minorities to engineering, as well as the need to improve science education in the public schools. But we wish that someone would have mentioned the unemployment among EEs, and the difficulties they face in making engineering a lifetime profession.

This type of television program highlights the need for national engineering leadership to point up the plight of the working engineer to the general public and to government. As mentioned in an editorial a few issues ago, there is some hope that, with a new president, the IEEE will step up its efforts in this cause. But if the IEEE doesn't follow through on that end, it should at least cooperate with, and support the efforts of, a group like the American Engineering Association (also mentioned in a recent editorial) in carrying the engineers' banner.

Secondly, we would feel remiss if we let slip by one of the most momentous world events of the 20th century: the dissolution of the Union of Soviet Socialist Republics. Before the break-up, the 70-year Russian Revolution had in one way or another directly affected nearly everyone's lives. Though it's outside our purview to comment on political ramifications, we can note that Soviet technology during those Cold War years clearly had its triumphs: Sputnik I, Yuri Gagarin's orbital flight, extended space-station flights – it took more than raw rocket power to pull off these technological coups. Now, a new world beckons for applications of Russian Commonwealth technology. We wish our colleagues in the newly independent republics of the former U.S.S.R. well as they work to become a force in international technological commerce. We also hope that the U.S. will soon lift its restrictions on high-technology exports, because it's in everybody's

interests to help build up the economy and the non-military industrial base of the Russian Commonwealth.

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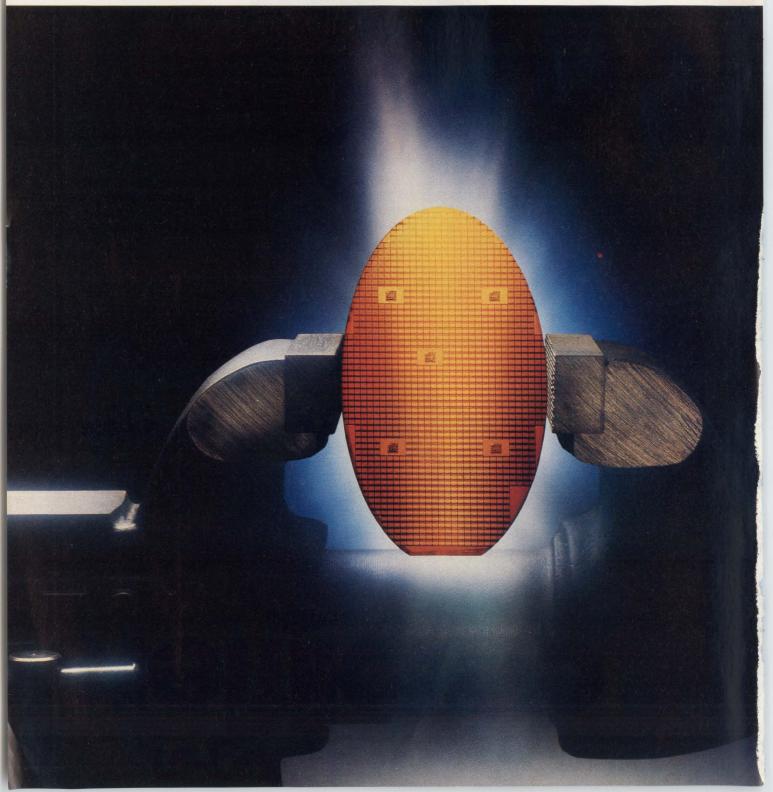
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Other critical performance parameters are as impressive. Drive capability is 32 to 64 mÅ. Static power consumption is typically 2 mÅ (I_{CCH}, I_{CCZ}) and 30 mÅ (I_{CCL}). Ground bounce is less than 800 mV typ.

All this in Widebus

Our ABT family, a second-generation advance of our leadership BiCMOS (BCT) family, includes versions of our 16-, 18- and 20-bit-width Widebus[™] functions.

Among the many ABT Widebus functions released is the 'ABT16244, a 16-bit buffer and line driver. It exhibits much greater stability of propagation delay (*see chart*), which results in a lower derating factor across the number of outputs switched.

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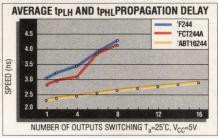
Also in volume production are the Widebus 'ABT16245 16-bit bidirectional bus transceiver and the 'ABT16543 and 'ABT16952 16-bit bidirectional registered bus transceivers.

As in our successful Advanced CMOS Logic (ACL) Widebus family, these devices come in our leadership surface-mount shrink small-outline package (SSOP) that gives you twice the number of I/Os as a standard smalloutline package in the same space.

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Unique additions included

There are also new devices in our ABT Widebus family featuring greater density and functionality. Our 'ABT16500A is a good example. An 18-bit registered transceiver, it combines D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes.



TI's speed advantage: In a one-to-one comparison, a TI 'ABT16244 16-bit Advanced BiCMOS driver proves to be much faster and more stable than Advanced Bipolar and standard CMOS octal drivers.

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CIRCLE 189 FOR RESPONSE OUTSIDE THE U.S.

TECHNOLOGY BRIEFING

ISO 9000: THE KEY TO SUCCESS IN EUROPE

s European executives see it, many American companies and their quality-control engineers aren't aware of the ISO 9000 set of standards. If that's the case, firms seeking to do business in Europe had better know what these quality norms are all about. And they must stick to them if they want to succeed in the single European market to be created by January 1, 1993. To be sure, if they don't abide by the 9000 standards, non-European firms won't be discriminated against. "However, they'll be in a better competitive position if they do," says an executive of a U.S. company in Germany.



JOHN GOSCH FIELD EDITOR

The Single Market will tear down the trade barriers between the 12 countries that make up the European Community, as well as bring a free flow of goods, services, and capital across national borders. Moreover, there will be common standards for all EC countries, replacing the hodgepodge of national norms that impede across-the-border trade, which some countries also use to protect their home markets.

One set of standards already common in Europe is ISO 9000, which was recommended by the International Standards Organization in 1987. Globally, more than 30 countries have opted for ISO 9000. Among them is the U.S., where the American National Standards Institute and the American Society for Quality Control adopted it as the ANSI/ASQC Q90 standard. But many U.S. firms "seem to be unaware of it and are following MIL standards or in-house guidelines," says an official at the German Society for Quality. However, that doesn't mean Americans are less quality-conscious than Europeans. An expert at Germany's Siemens AG states, "It's only because of their huge home market that U.S. firms are using their own standards and are unfamiliar with others."

While the giants in the U.S. industry know about ISO 9000, most smaller firms eager to enter foreign markets are unaware of it. Actually, ISO 9000 doesn't specify product design and operation. Instead, it's a set of quality system standards and guidelines complementing product or service requirements. It aims to help firms set up procedures to achieve optimum quality in all operations, from incoming inspection to product installation and service.

The first standard in the five-norm set, the actual ISO 9000, defines quality terms and offers advice on how to use the other four norms. ISO 9001 describes a model for quality assurance in the design and development of a product and its fabrication, installation, and servicing. It shows the customer that a supplier can deliver and service a product. ISO 9002 goes into more details on quality assurance in production and installation than ISO 9001. The next norm is ISO 9003, which provides a model for quality assurance in test and final inspection. Finally, ISO 9004 offers guidelines on elements of quality management and quality systems. The ISO 9000 set is flexible: It will be periodically reviewed using customer feedback, and may be extended to include software development, supply, and maintenance.

In Europe, ISO 9000 is gaining popularity, especially among high-tech and export-intensive firms. Considered an important element in a company's business strategy, the norms are often used as a sales argument in product ads and negotiations. Classified ads will sometimes specify that engineers seeking jobs in quality control know about it. Customers are beginning to pressure their suppliers to implement ISO 9000 and many have started to rate suppliers on how well they can fill an order for quality products.

To qualify as an "ISO 9000 firm," an accredited agency must certify that the quality system it is using meets the standard's requirements. A number of agencies can give such certification, including the British Standards Institute in the United Kingdom and the Society for the Certification of Quality Assurance Systems in Germany.



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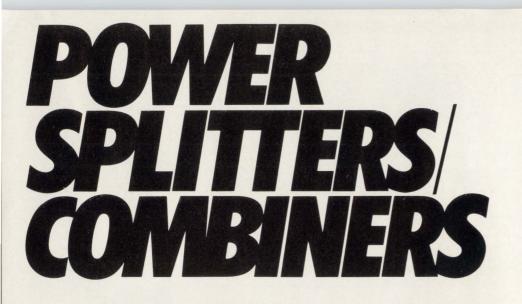
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TECHNOLOGY NEWSLETTER

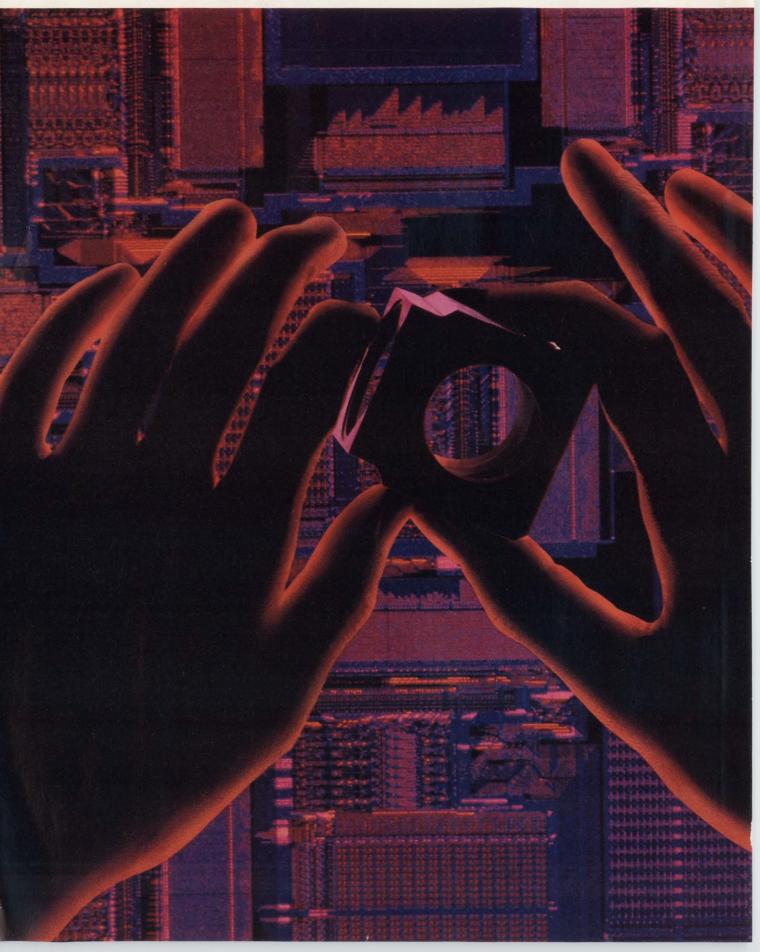
COPPER IS DEPOSITED An additive technique for depositing copper circuit lines directly onto Teflon in only three steps has been developed by researchers at Sandia National Laboratories and the University of New Mexico, both in Albuquerque. Earlier processes for depositing copper on Teflon took at least eight steps, created relatively wide traces, and required subtractive processing. But the famous "non-stick" properties that make Teflon so desirable in frying pans made additive deposition of copper a challenge. The break-through came when researchers discovered that copper won't adhere to Teflon that's been irradiated with X-rays or electrons (step one), but will stick to areas that are subjected to a commercial chemical-etching solution (step two). At first, copper was applied with chemical-vapor deposition (step three). But it was subsequently found that standard electroless copper plating works as well. Interestingly, only the initial irradiation step requires a patterning mask. The entire Teflon surface is subjected to the etchant in step two, but the irradiation apparently makes the unmasked areas immune to the solution. In addition to printed-circuit applications, Sandia's Microelectronics Development Laboratory is exploring copper interconnects as wiring for next-generation ICs. *DM*

DMOS PROCESS MIXES 600-V FETS WITH BIPOLAR LOGIC By extending its proven high-voltage IC process from 500 to 600 V and adding a few proprietary circuit tricks, International Rectifier, El Segundo, Calif., developed the first three-phase power MOSFET-gate driver. The process puts 600-V DMOSFETs on the same chip as low-voltage bipolar transistors and CMOS logic. Increasing the voltage rating required enlarging device size and improving termination techniques. The new IC, the IR2130, is aimed at controlling fractional- and integral-horsepower three-phase motors, up to 5 horsepower, in pulse-width-modulated and six-step drive systems. Alternatively, two of its three half-bridge drive circuits can be used with four power FETs in any of several full-bridge switching-regulator topologies, while the remaining pair of FETs drives two power MOSFETs in a power-factor-correcting pre-regulator. The IR2130 contains three ground-referenced low-side and three floating high-side drivers, all capable of sourcing and sinking 250 and 500 mA, respectively. For additional information, call Shawn Fogarty at (800) 245-5549. FG

PARTNERSHIP TO YIELD IMAGE-PROCESSING ICS In an enhancement of a partnership inked nearly a year ago, Array Microsystems Inc., Colorado Springs, Colo., and Samsung Semiconductor Inc., San Jose, Calif., have agreed to develop a family of image-compression chips. The programmable circuits, based on a core CPU technology optimized for video processing, could be configured to perform JPEG, MPEG, Px64, and other image-processing algorithms. By making the core programmable instead of hardwired, the chips can overcome many shortcomings inherent in currently available image-processing ICs. The cores can also switch quickly between algorithms and thus perform multiple tasks, while still permitting real-time video processing compatible with the NTSC CCIR 601 standards. The chips will implement a parallel-processing architecture so that multiple chips or chip sets can be added to improve system performance. Furthermore, derivative products—specialized versions of the chips—will also be possible thanks to the flexible design and support tools also being developed. Software tools will be released in the late second quarter. However, initial samples of the first chips in the family are slated for release in the fourth quarter. DB

NORMAL-PAPER FAX CLAIMS SMALLEST SIZE So far, telefax systems using normal paper have been bulky and space-consuming because of the many electromechanical components needed to implement laser- or ink-jet-based normal-paper systems. Now Siemens AG is coming out with a fax machine using electrophoretic printing methods (in electrophoresis, the movement of charged particles suspended in a fluid medium is exploited under the influence of an electric field). That, the Munich, Germany company claims, makes it the smallest normalpaper fax system developed to date. It occupies an area no larger than a page of this magazine (8 1/2 by 11 in.). The Teamfax HF2312 delivers copies that can be marked up with pencil or ballpoint pen, much easier than copies on specially layered paper. It prints four pages/min. at document-quality levels and has a high degree of sharpness—resolution is 300 dots/in. At only 44 dBA, the noise the machine generates is rather low. The Teamfax HF2312 features such functions as abbreviated and automatic repeat dialing and has a 15-page memory. Transmission speed per page is 13 seconds. An error-correction scheme eliminates any errors that may

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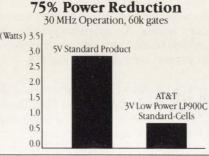
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TECHNOLOGY NEWSLETTER

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DENSE TERMINATIONS ELIMINATE VIA HOLES A patented process creates high-density terminations that eliminate the need for the traditional via hole connecting an internal conductor with a component pad. In the Microdot process, developed by Advanced Interconnection Technology (AIT), Islip, N.Y., the ends of 0.0025-in. polyimide-insulated copper wire are displaced vertically in the Z axis into an epoxy resin. Then, the circuit is planarized to expose the wire ends and electroplated copper is deposited on the surface to form a component pad on top of the wire ends. With no holes required, signal termination can be achieved directly on pad pitches down to 0.012 in. This eliminates fan-out to the typical 0.050-in. pitch and dramatically increases I/O density. In addition, there's no more capacitance and inductance associated with vias. Contact AIT at (516) 968-1400. DM

SIEMENS AND IBM TO PRODUCE 16-MBIT DRAMS An agreement made in July 1991 between Siemens AG of Munich, Germany, and IBM Corp., Armonk, N.Y., to produce 16-Mbit dynamic RAMs at IBM's factory in Corbeil-Essonnes, France, will soon bear fruit. Data measured on first samples will be used to fine-tune production lines this spring, and products will be available in volume quantities toward the end of 1992. The first 16-Mbit DRAM will be a device with a 4-Mbit-by-4-bit organization. It will have an access time between 50 and 70 ns and come in a 400-mil-wide SOJ plastic package with 28 or 24 pins. The device will integrate some 35 million elements on a 137 mm² chip. The smallest structures will be 0.5 μm. Other versions will follow in 1993, among them byte-oriented 16-Mbit DRAMs with a 2-Mbit-by-8-bit and 1-Mbit-by-16-bit organization, as well as DRAM parts supplied in a TSOPII package. JG

FAST TWO-STEP PROCESS MAKES COPPER CIRCUITS A two-step process makes 100% copper circuit traces in just 10 seconds—50 times faster than permitted by current technology. The Pathways system, developed by Printron Inc., Albuquerque, N.M., uses atmospheric pressure to print metal slurries on a wide variety of substrates, including paper, plastics, and ceramics. Initial circuit resolution for lines and spaces is 4 mils. The metal-slurry inks consist of micron-sized metal particles of either copper or a combination of copper, silver, and gold suspended in a proprietary media. A proprietary technique directs intense energy to the printed-slurry patterns, which fuses them into solid-copper conductors. The initial version of the system is targeted at prototyping applications. *DM*

SGS, PHILIPS, TEAM UP IN VLSI PROCESSES advanced CMOS logic processes below 0.7 μm, including design rules and libraries. The first common process will be a 0.5-μm CMOS logic process on 8-in. silicon wafers. It's expected to be completed by the end of 1993. Activities will take place at SGS-Thomson's new R&D Center in Italy and at the French telecommunication research institute at Crolles, France. JG

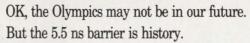
RISC ICS PUSH PROCESSOR ADVANCES Three new developments based on the 32-bit RISC architecture from MIPS Computer Systems, Sunnyvale, Calif., should enhance the position of Siemens AG, Munich, Germany, in the microprocessor market. The first is the Siemens SAB-R3500, which integrates an integer- and floating-point-processor on one chip. The second development is the SAB-R3223, a read/write buffer for use between the main memory and a 32-bit processor core. Finally, the Munich company housed its standard SAB-R3000A and SAB-R3010A processors in a low-cost surface-mounted plastic quad flat package, the PQFP-160. These processors have an integrated heat sink and are designed for applications where clock frequencies go beyond 25 MHz. Main applications for these RISC devices are workstations, laser printers, robotics, and in the aerospace field. The single-chip SAB-R3500, now being sampled, is pin-compatible with the company's SAB-R3000A processor and comes in the CPGA-161 pin grid array as well as the PQFP-160 packages. It can be clocked at 40 MHz. The SAB-R3223 read/write buffer, which has an 8-word-deep read memory and a one-stage write memory, raises a system's computing performance by up to 30%. JG

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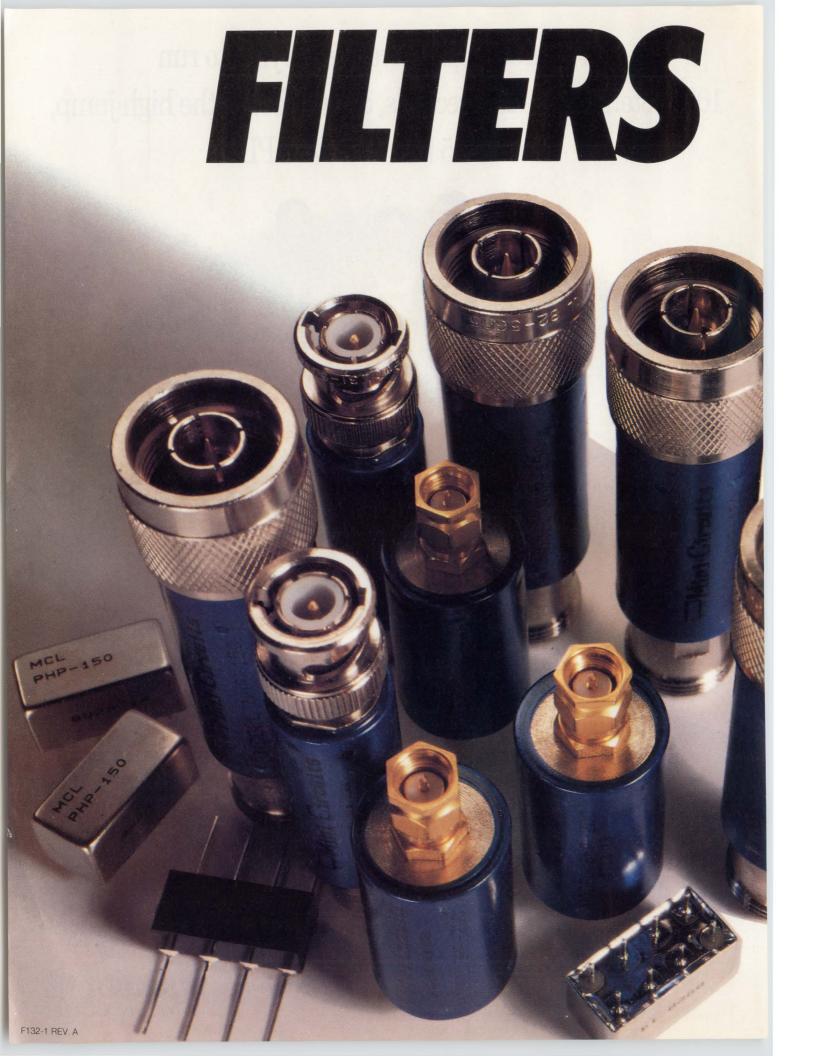
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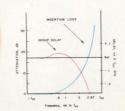


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frequency

frequency

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BP attenuation

attenuation

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Model No.	Passband MHz loss < 1dB	Stopbar loss > 20dB	nd, MHz loss >40dB	Model No.	Passband MHz loss < 1dB	Stopba loss > 20dB	nd, MHz loss >40dB
PLP-5 PLP-10.7 PLP-21.4 PLP-30 PLP-50 PLP-70 PLP-90 PLP-100 PLP-150 PLP-200	DC-5 DC-11 DC-22 DC-32 DC-48 DC-60 DC-81 DC-98 DC-98 DC-140 DC-190	8-10 19-24 32-41 47-61 70-90 90-117 121-137 146-189 210-300 290-390	10-200 24-200 41-200 90-200 117-300 167-400 189-400 300-600 390-800	PLP-250 PLP-300 PLP-450 PLP-550 PLP-600 PLP-750 PLP-800 PLP-800 PLP-800 PLP-1000 PLP-1200	DC-225 DC-270 DC-400 DC-520 DC-680 DC-700 DC-700 DC-760 DC-760 DC-900 DC-1000	320-400 410-550 580-750 920 840-1120 1000-1300 1080-1400 1340-1750 1620-2100	400-1200 550-1200 750-1800 920-2000 1120-2000 1300-2000 1400-2000 1400-2000 1750-2000 2100-2500
Price, (1-9 qt	y), all models: plug Su		nc \$32.95, SMA Dunt, dc to	\$34.95. Type N \$3 570 MHz	5.95		
SCLF-21.4 SCLF-30 SCLF-45 SCLF-135	DC-22 DC-30 DC-45 DC-135	32-41 47-61 70-90 210-300	41-200 61-200 90-200 300-600	SCLF-190 SCLF-380 SCLF-420	DC-190 DC-380 DC-420	290-390 580-750 750-920	390-800 750-1800 920-2000

Price, (1-9 qty), all models: \$11.45

Flat Time Delay, dc to 1870MHz

	Passband MHz	Stopt			WR ge, DC thru		Delay Variat	
Model No.	loss < 1.2dB	loss >10dB	loss >20dB	0.2fco X	0.6fco X	fco X	2fco X	2.67fco X
PBLP-39 PBLP-117 PBLP-156 PBLP-200 PBLP-300 PBLP-467 ▲BLP-933 ▲BLP-1870	DC-23 DC-65 DC-94 DC-120 DC-180 DC-280 DC-280 DC-560 DC-850	78-117 234-312 312-416 400-534 600-801 934-1246 1866-2490 3740-6000	117 312 416 534 801 1246 2490 5000	1.3.1 1.3.1 1.6.1 1.25.1 1.25.1 1.3.1 1.45.1	2.3:1 2.4:1 1.1:1 2.2:1 2.2:1 2.2:1 2.2:1 2.9:1	0.7 0.35 0.3 0.4 0.2 0.15 0.09 0.05	4.0 1.4 1.1 1.3 0.6 0.4 0.2 0.1	5.0 1.9 1.5 1.6 0.8 0.55 0.28 0.15

Price, (1-9 qty), all models: plug-in \$19.95, BNC \$36.95, SMA \$38.95, Type N \$39.95 NOTE: ▲ - 933 and -1870 only with connectors, at additional \$2 above other connector m connector models

high pass, Plug-in, 27.5 to 2200 MHz

		band Hz	Passband MHz	VSWR Pass-			band Hz	Passband MHz	VSWR Pass-
Model No.	loss < 40dB	loss < 20dB	loss <1dB	band Typ.	Model No.	loss < 40dB	loss < 20dB	loss <1dB	band Typ.
PHP-25 PHP-50 PHP-100 PHP-150 PHP-175 PHP-200 PHP-250 PHP-300	DC-13 DC-20 DC-40 DC-70 DC-70 DC-70 DC-90 DC-100 DC-145	13-19 20-26 40-55 70-95 70-105 90-116 100-150 145-170	27.5-200 41-200 90-400 133-600 160-800 185-800 225-1200 290-1200	1.8:1 1.5:1 1.8:1 1.5:1 1.5:1 1.6:1 1.3:1 1.7:1	PHP-400 PHP-500 PHP-600 PHP-700 PHP-800 PHP-900 PHP-1000	DC-210 DC-280 DC-350 DC-400 DC-445 DC-520 DC-550	210-290 280-365 350-440 400-520 445-570 520-660 550-720	395-1600 500-1600 600-1600 700-1800 780-2000 910-2100 1000-2200	1.7:1 1.8:1 2.0:1 1.6:1 2.1:1 1.8:1 1.9:1

Price, (1-9 qty), all models: plug-in \$14.95, BNC \$36.95, SMA \$38.95, Type N \$39.95

bandpass, Elliptic Response, 10.7 to 70 MHz

	Center	Passband	3 dB	Sto	opband
Model No.	Freq. (MHz)	I.L. 1.5 dB Max. (MHz)	Bandwidth Typ. (MHz)	I.L. > 20dB at MHz	> at
PBP-10.7 PBP-21.4 PBP-30 PBP-60 PBP-70	10.7 21.4 30.0 60.0 70.0	9.6-11.5 19.2-23.6 27.0-33.0 55.0-67.0 63.0-77.0	8.9-12.7 17.9-25.3 25-35 49.5-70.5 68.0-82.0	7.5 & 15 15.5 & 29 22 & 40 44 & 79 51 & 94	0.6 & 3.0 & 3.2 & 4.6 & 6.0 &

Price, (1-9 qty), all models: plug-in \$18.95, BNC \$40.95, SMA \$42.95, Type N \$43.95

Constant Impedance, 21.4 to 70 MHz

I.L. 35dB t MHz	Model No.	Freq.	MHz loss <1dB	loss > 20dB at MHz	1.3:1 Total Band MHz
50-1000 80-1000 99-1000 190-1000 193-1000			18-25 25-35 35-49 41-58 50-70 58-82 models: plug A \$38.95	1.3 & 150 1.9 & 210 2.6 & 300 3.1 & 350 3.8 & 400 4.4 & 490 g-in \$14.95, Type N \$39	DC-220 DC-330 DC-400 DC-440 DC-500 DC-550

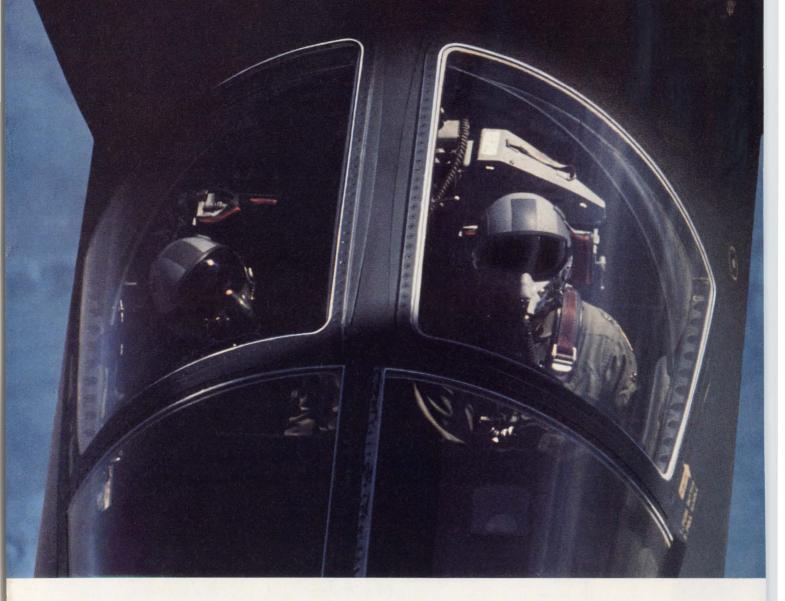
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PROGRAMMABLE INTERCONNECTION MATRIX IN SILICON SPEEDS SYSTEM DESIGN

reating the first custom pc boards during system design can be an expensive, time-consuming process that requires many iterations and is error-prone. That's true even though most designers take advantage of PCor workstation-based pcboard design tools. And, with few exceptions, current prototyping boards still require designers to hand wire-wrap point-topoint connections. Seeking a better solution, designers at Aptix Corp., San Jose, Calif., created a programmable signal-wiring matrix in silicon that can replace pc-board wiring.

The concept, dubbed by the company "field-programmable interconnect components" (FPICs), makes possible user-configurable component-tocomponent interconnections. Unlike cross-point switching matrices, which typically have a set of dedicated inputs and a set of dedicated outputs, the Aptix concept let any pin be routed to any pin or pins, says Aptix's founder Dr. Amr Mohsen. Expandability of the concept, he adds, is only limited by the number of package pins—not by the number of programming points, as in crosspoint matrices.

More than 20 patents protect the concept, in areas such as device and system architectures, programming elements, and packaging technology. Aptix will demonstrate the concept next quarter, when it plans to unveil two field-programmable components, one built around reprogrammable static-RAM-based control cells, and the other around onetime-programmable control elements.

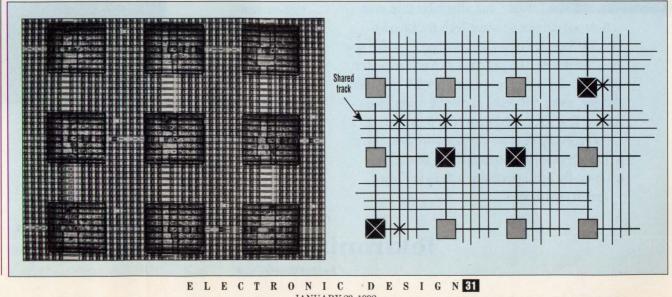
The two FPICs, though, are pin compatible. Consequently, designers could do early prototyping with the SRAM-based chip, which permits quick configuration changes to alter signal routing. Once the pattern is firm, lower-cost one-time programmable versions can be used for low-to-medium-volume production.

One major advantage of the SRAM-based chip is that it can be dynamically reconfigured in the system to adjust the interconnection paths. The SRAMbased chip also consumes minimal power once it's configured-aside from a small current needed to maintain the contents in the SRAM cells, the chip requires no power except when it's being reconfigured, which only takes several seconds. The onetime programmable version needs even less power once programmed because there are no memory cells to keep alive.

The SRAM-based version of the FPIC is made by a 0.8- μ m CMOS process and packs over 1 million transistors in its configuration logic (assuming six transistors per SRAM cell, that translates into about 160,000 configuration cells). Similarly, just over 160,000 interconnection elements are used in the equivalent one-time programmable version.

The one potential drawback of an FPIC is the large number of pins such interconnection components would require. To counter that limitation, Aptix developed a novel 1024contact, land-grid array, multilayer ceramic package. The high-density LGA package can be seated into a matching socket that, in turn, is mounted in the target system.

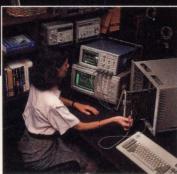
Comprised of a regular grid of attachment points (the I/O pads), the internal array architecture employs multiple, segmented signal-routing "tracks" in each wiring channel to carry the signals routed onto them by the configuration elements (see the figure, left). There are several different types of tracks, arranged in a hierarchy. At the top are continuouswire tracks that span the length or width of the chip (good for long routes). Next down are tracks that are divided into a few independent segments (good for moderate routes). And at the bottom are tracks



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that have many physical divisions (the short segments are good for localized routing between adjacent I/O pads). Routing control elements or memory cells are at the intersections of orthogonal tracks (see the figure, right).

Signal paths through the FPICs are bidirectional and passive, and have typical pin-to-pin path delays of less than 10 ns. Either version of the FPIC allows more than 1000 externally accessible interconnects to fit in one package, while permitting systems to op-

erate at over 50 MHz.

Any combination of pins can be universally interconnected to any other combination of pins by the matrix. Consequently, if a group of chips on a pc board must be interconnected, all signal pins from that group of ICs could be directly routed to pins on the FPIC. The configuration pattern loaded into the FPIC would then connect IC1 pin 1 to IC3 pin 3, IC1 pin 2 to IC 5 pin 5, etc., until all chips in the group are interconnected. Multiple FPICs can also be used in a system, with some signal pins used for the FPIC-to-FPIC interconnections to route signals between large logic blocks.

Proprietary programming and configuration software developed by the company can perform automatic signal routing to 100% completion. Furthermore, it allows users to control critical path placement and deal with incremental changes or updates to the design files. Signals are also observable—the FPICs include several "viewing ports" that can access any of the signals in the array. That feature should come in very handy during system debugging.

When the software runs on a Sun SparcStation IPC workstation, the interconnection routing time needed to fully configure the 1024-pin FPIC device is less than two minutes. In-circuit configuration time for the SRAM version is a few seconds; the one-time programmable version needs less than five minutes in a special device programmer for full configuration.

DAVE BURSKY

SILICON BIPOLAR ICS SET RECORD OF 30 GBITS/S

group of researchers at the Ruhr University in Bochum, Germany, set a speed record for semiconductor devices by developing siliconbased multiplexer and demultiplexer ICs that operate at up to 30 Gbits/s. Consequently, the researchers upstaged themselves; about nine months ago they reported a speed of 24 Gbits/s-the highest for silicon at that time (ELECTRONIC DESIGN, Apr. 25, 1991, p. 23).

The 30-Gbit/s rate is a record not only for silicon but for any type of material. The new chips outperform even ICs using the more expensive gallium arsenide material, for which speeds of 28 Gbits/s have been reported, according to Hans-Martin Rein, a professor at the university's Electrical Engineering Department and head of the research group.

What's more, the silicon approach taken is not some exotic laboratory technology, but rather the kind that the industry is now transferring into production. The group's extremespeed multiplexer and demultiplexer ICs were fabricated in a 0.8-µm selfaligned silicon bipolar process at the Hewlett-Packard Company in Palo Alto, Calif.

The Bochum feat again demonstrates silicon's usefulness in extremely fast semiconductor devices. At one time, experts predicted that it wouldn't be long before silicon would be replaced by gallium arsenide as a material in high-speed circuits. But researchers everywhere have kept pushing out the speed limits for the good old silicon-so often, that experts have stopped predicting silicon's diminishing role.

The ICs that the Bochum group developed are intended for high-speed measuring equipment and future glass-fiber transmission systems. Their 30-Gbit/s data rate is more than ten times that of the fastest glass-fiber links now being installed. The latter's speed is around 2.5 Gbits/s.

In addition to the latest silicon bipolar technology, the new devices owe their performance to improved techniques for optimizing circuit design, as well as to high-accuracy transistor models for simulating extreme speeds. The Rein group has used these techniques and transistor models for several years. This work is now paying off.

The transistor models are so flexible that they can be applied in a simple way to different technologies used in IC fabrication. A suitable computer program, also developed at the Ruhr University, allows fast calculations of the models' parameters for any transistor dimension. This enables chip designers to optimally adapt a transistor's characteristics to the task it's to perform in a specific circuit.

Optimizing transistors individually is a prime factor responsible for the 30 Gbit/s speed, Rein says. Using this and other design aids, his group developed a number of highspeed ICs in the past among them decision circuits, frequency dividers, driver stages for laser diodes, and various types of amplifiers. Meanwhile, the industry uses the Bochum design techniques and transistor models.

One problem the Bochum researchers faced was checking the extremespeed chips. As a solution, they built a pulse generator that could produce pulses at up to 30 Gbits/s more than twice that of the fastest pulse generator on the market.

The self-made generator consists essentially of the 30-Gbit/s multiplexers that the group developed and special frequency dividers operating at more than 15 GHz. The dividers were developed together with Siemens AG, Munich, as part of the Esprit program (the European Strategic Program for Research in Information Technologies).

The Bochum researchers also took into account that the pulse rise time is less than 17 ps, which in-

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cludes the inherent rise time of the oscilloscopes used. 17 ps is about the time it takes light to travel a distance of 5 mm. Such steep pulses must be fed into and out of the chip via conductors, connectors, and contact wires.

Here, the Rein group used a novel approach for best measuring results. While other groups generally measure fast ICs on the wafer, these researchers mounted their chips on a measuring fixture using a conventional bonding technique. A careful design of the measuring fixture and precise calculations of the critical interfaces helped solve the measuring problems.

Rein expects that further records will be achieved with some of the silicon devices his group is currently developing together with German companies such as Siemens, ANT in Backnang, and Telefunken Electronic in Heilbronn. In this work, duplication of effort is avoided as the circuits each firm develops differs in device type, technology used, and the chips' tasks.

Under development are decision circuits, frequency dividers, driver stages, and amplifiers, as well as multiplexers and demultiplexers—all intended mainly for future opticalfiber transmission links sporting data rates exceeding 10 Gbits/s. The development work also aims to demonstrate to what extent today's silicon technologies can be used in high-speed device design.

According to Rein, the results obtained by his group are still far from the speed limits achievable with silicon technologies. Further improvements in speed can be expected from modifying the transistor base or emitter, by

chips that will be offered

for Sonet, CEPT, and Japa-

nese wideband communi-

cation applications. Those

chips include a multi-rate

line interface that termi-

nates CEPT E2 (8448-kbit/ s), CEPT E3 (34,368-kbit/

s), or Japanese T2 (6313-

kbit/s) lines, and an E2/

E3F framer that frames

wideband payload signals

into any one of four digital

hierarchy signals, speci-

adding other atoms (such as germanium atoms to the base). In this way, heterojunction bipolar transistors (HBTs) are obtained.

ICs using HBTs are currently made elsewhere on the basis of compound semiconductor materials such as gallium arsenide. In the long run, these ICs, which are still in the laboratory stage, will be faster than silicon-based circuits, Rein says. However, because of certain disadvantages—among them high cost—the application of these circuits will be limited.

JOHN GOSCH

BICMOS TECHNOLOGY TACKLES DEMANDING PERFORMANCE NEEDS OF SONET SYSTEMS

The changeover from copper to optical-fiber-based telecommunications is increasing the need for high-speed chips, with internal operating speeds two to four times that of the data rate. The result is that performance needs have leapt past the levels that most CMOS processes can deliver, making biCMOS the technology of choice. As data rates migrate from the 1.54- and 44.7-Mbit/s levels of asynchronous DS1 and DS3 channels, to the 51.84-Mbits/s base rate (and its multiples) of the synchronous transport signal 1 (STS-1), high-performance digital interface and system-logic chips are being called for.

In a deal struck in 1991, Texas Instruments Inc., Dallas, has worked with TranSwitch Corp., Shelton, Conn., to create a family of biCMOS chips specifically targeted at the DS3 and synchronous optical network (Sonet) equipment makers. The chips will be released later this year and are expected to perform key functions such as signal encoding and decoding, serial-toparallel and parallel-to-serial conversion, framing, clock recovery, and overhead processing.

Sonet's 51.84-Mbit/s throughput is the root rate the U.S. The equivalent in Europe, the synchronous digital hierarchy (SDH), is 155.52 Mbits/s (STM-1). Three multiplexed STS-1 lines form an STS-3 line, which is equivalent to one STM-1 channel.

The international agreement regarding the use of Sonet benefits the system designer as it allows semiconductor suppliers to slice up the systems into integratable sections to further reduce cost and simplify system designs.

TranSwitch created five 36-or 34 E L E C T R O N I C

fied by the Consultative Committee on International Telephony and Telegraphy (CCITT). CEPT stands for European Conference on Postal and Telecommunications Administrations. Another framer chip, the JT2F, is for the 6312-kbit/s format specified in CCITT recommendation G.702 and Japan's NTT technical specifications. The other two chips are high-level data-link control (HDLC) ICs—both operate at up to 51.84 Mbits/s. One has a 36- or 9-bit interface on the DESIGN **JANUARY 23, 1992**

HDLC side; the other only has a 9-bit interface.

Asynchronous ICs coming from TI include a full DS3 receive/transmit interface (DS3RT) and a high-speed HDLC that are similar to the multi-rate line interface chip and the 9-bit HDLC chip from TranSwitch. Synchronous products include a Sonet overhead terminator (SOT-3) chip for STS-3 line rates, and a synchronizer chip (SYN155) for STS-3 systems. The interface requirements for the chips revolve around one key point-the ICs must initially interface to systems with data rates up to 155 Mbits/s.

Additional chips are being jointly defined by TranSwitch and TI, which the companies hope to release in 1993. Some of those functions may have to operate at four times the speed of the STS-3 line— 622 Mbits/s, and at the next level above that at four times that speed—2.5 Gbits/s. To operate at such speeds, TI's designers ex-

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16K x 18	MT58C1618**	13,15,17, 20,25ns	5,6,7,8,10ns	52-pin PLCC and PQFP
128K x 9	MT58C1289	16.6,20ns	*	32-pin SOJ

* Output Enable is a synchronous signal on the 128K x 9

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TECHNOLOGY ADVANCES

pect to transition to gallium-arsenide technology and exploit advanced packaging technologies. Initial chips will use familiar plastic-leaded chip carriers with 1.27-mm pin pitches. However, finer-pitch packages, with lead spacings of 0.635, 0.5, and eventually 0.4 mm, will be available to improve the package I/O without greatly increasing needed pc-board space.

At data rates of 155 Mbits/s, TI's designers believe that the bipolar output structure of biCMOS logic offers a more-stable. well-behaved, signal swing than pure CMOS. That results in less simultaneous switching noise and higher system reliability. Furthermore, because biC-MOS does not swing railto-rail, its overall power dissipation is less than that of an equivalent CMOS output that runs at high frequency. As a result, the chips will consume less current and will run cooler.

Both CMOS and biCMOS will be used, where appropriate, for the various chips that were jointly defined with TranSwitch. For DS3 applications, a 1- μ m CMOS-only process will deliver the best mix of performance at low cost. For the Sonet SOT-2 and SYN155 circuits, a 0.8- μ m biCMOS process will be used.

The DS3RT chip provides the interface between the bipolar transmission line (DS3) and the digital-signal processing functions on the equipment terminal side. The receiver section converts the incoming bipolar signal, which is coded as a special string of bits, into its digital equivalent. It also determines the number of bipolar violations as a bit-error rate, when an external 8-kHz clock is supplied. The chip must also recover the data clock from the incoming DS3 signal. Both "loss-of-signal" and "clock" alarms warn of potential signal errors.

Data is ultimately delivered by the chip to the terminal equipment in a nonreturn-to-zero (NRZ) format. When it transmits the NRZ data from its terminal port to the DS3 line, the chip also monitors the clock line for loss of the clock. The chip can simultaneously receive a signal from a DS3 line, while it sends data to a DS3 line.

The HDLC chip sends and receives packets into serial or parallel communication-line interfaces at up to 51.84 Mbits/s, letting it be used in DS3, Sonet, and CCITT line interfaces. It generates warning flags, does zero insertion and deletion, and abort detection and byte framing.

Handling all aspects of section, line, and pathoverhead processing for an STS-3 155-Mbit/s signal channel, the SOT-3 overhead terminator offers a byte-parallel interface. Overhead bytes may be

passed through or modified in either or both receive and transmit directions. The companion SYN155 supplies complete STS-3/STM-1 frame synchronization, including synchronizing with the 155-Mbit/s signal, and providing, as an output, the signal bytes or nibbles along with a byte/nibble clock and frame-indication signal. In the transmit direction, the signal flow is reversed-the chip accepts a byte-wide signal and clock, while delivering a serial data stream and clock.

DAVE BURSKY

SILICON DRYING METHOD PROMISES TO IMPROVE IC QUALITY AND YIELDS

Cetting new standards Sin cleanliness, Philips Research Laboratories in Eindhoven, the Netherlands, has come up with a novel, ultra-clean method for drying silicon wafers and glass plates. The technique promises to improve the quality and yield levels of IC devices. It relies on the Marangoni effect: The flow of liquid along the surface of another liquid induced by local variations in surface tension, due to a gradient in temperature or concentration along the surface. The method is of particular interest in IC production, where demands for cleanliness are very high.

The fabrication of ICs, liquid-crystal displays, and pc boards often necessitates wet-processing steps, which usually involve rinsing the devices in water and subsequently drying them. After drying, dissolved or dispersed contaminants in even the pur-

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est water may be left on the device's surface. This can have disastrous effects on further processing and on product quality.

A device that's withdrawn from a water bath after rinsing is covered with a water film about 10- μ m thick. Conventional spin drying reduces this thickness about ten times. But the equipment involved usually generates tiny contaminating particles that are deposited on the device surface. These methods may also lead to stress-induced damage of fine surface structures.

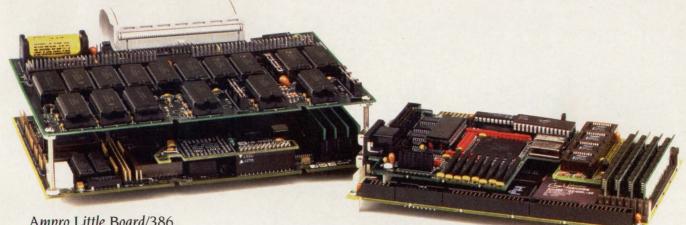
If, however, vapor of a water-soluble organic compound like isopropyl alcohol is directed toward the device surface at the point where it emerges from the rinsing bath, water on the surface absorbs the vapor. This leads to a larger concentration increase at the top of the meniscus against the device than further down where the dissolved I C D E S I G N

vapor can more easily diffuse away from the surface (the meniscus is the curved upper surface of a liquid column that's concave when the containing walls are wetted and convex when not). Thus, a concentration gradient is set up along the meniscus resulting in a surface tension gradient. This gradient, in turn, induces a Marangoni flow of water back into the rinsing bath. The water film on the device is cut to a thickness of only a few nanometers, and the device emerges from the water bath dry and clean.

Marangoni drying, Philips says, doesn't pollute the environment and consumes little energy. It doesn't call for expensive safety measures when a low-vapor-pressure organic compound is used. Most important, its application ensures the highest degree of cleanliness to date in device drying.

JOHN GOSCH

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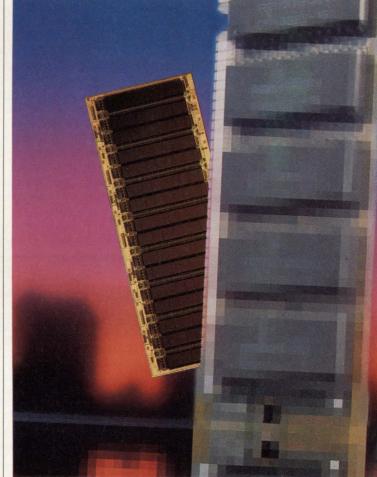
DAVE BURSKY

igh-performance microprocessor-based systems almost universally include high-speed secondary cache subsystems between the main memory and the RISC

or CISC CPU. The cache minimizes the time the processor must spend waiting for data or instructions to be read from the slower main memory, thus reducing the bandwidth requirement of the main-memory bus. However, the high-speed static RAMs required for the cache consume valuable board space and are relatively power hungry—two negatives for systems that designers are continually trying to reduce in size or trim in power drain.

By integrating a slice of the SRAM-based cache and DRAM-based main memory onto one chip, designers at Ramtron solved some of the bus-bandwidth issues, reduced board space, and lowered system power. The DM 2202 enhanced DRAM (EDRAM) combines a 1-Mword-deep by 4-bit-wide DRAM with 512 4-bit nibbles of static RAM. Additional features include write posting (for no wait-state writes) to the DRAM section, making it possible for a system to achieve maximum-speed system-bus transfers.

A second version of the EDRAM, the DM 2212, includes a write-per-bit capability—a feature that permits selective writes to each of the four I/O pins. Such an attribute is handy for video applications and when the 2212 is used to hold the parity bits in systems that incorporate parity checking to improve data integrity. For memory systems that need more than 4 Mbytes, the DM 2200, a 4-M-by-1 EDRAM, can be used to form a 16-Mbyte main-memory subsystem with a tightly-coupled internally integrated 8-kbyte cache.



Data reads from the cache portion of the chip (a cache hit) can be done in just 15 ns. That permits the host CPUs to perform nowait-state reads, burst reads, and back-toback reads, at system clock rates of up to 50 MHz, by using a simple two-way interleaving scheme with two banks of EDRAMs. If a single-bank architecture (no interleaving) is employed, systems can run at speeds up to 40 MHz without requiring any memory wait

E L E C T R O N I C D E S I G N 39 JANUARY 23, 1992

COMBINATION CACHE AND DRAM CHIP

states or stand-alone secondary caches.

If a cache miss occurs, the EDRAMs have a 35-ns row-enable access time and a 65-ns row-enable cycle time. Those short times are due "to a fast DRAM process, highspeed circuit design, and the close internal coupling of the DRAM section to the high-speed integrated SRAM" explains Dave Bondurant, the company's director of concept engineering (Fig. 1a). "Because of the proximity," he says, "chip architects were able to take advantage of IC metalization technology to create a very wide data path on the chip between the DRAM and SRAM. That 2048-bit-wide path permits the entire cache to be updated in a single cycle, thus greatly reducing the cache-line refill time. The equivalent transfer speed during a cache refill hits 7.3 Gbytes/s over the 2048-bit-wide onchip bus between the DRAM and cache blocks.'

Input latches for both the address and data lines allow the system to send addresses or data, or both, and then continue on to another operation. This minimizes delays caused by slow write operations. One write operation (from the host CPU to the

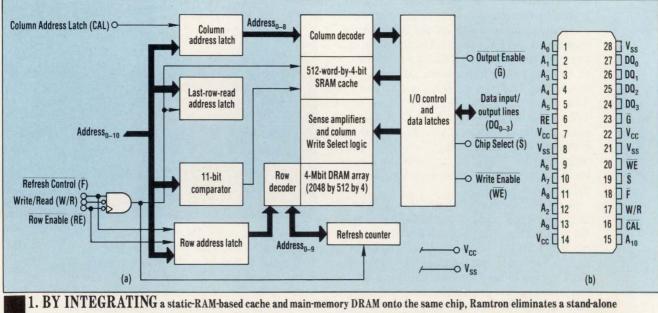
Processor	Clock rate	Read/write cycles(hit)	Read/write cycles(miss)	Burst read cycles(miss)	Burst read cycles(hit)
386DX	20 MHz	2-2	2-2	NA	NA
	25 MHz	2-2	2-2	NA	NA
	33 MHz	3-2	2-2	NA	NA
	40 MHz	3-2	2-2	NA	NA
486DX	25 MHz	2-2	2-2	2-1-1-1	2-1-1-1
	33 MHz	3-2	2-2	3-1-1-1	2-1-1-1

MEMORY SUBSYSTEM PERFORMANCE,

EDRAM) requires just 15 ns, because the word is written into the onchip latch (posting register). Once the data is latched to the chip, the write to the DRAM array is performed. While the write is being done, the CPU can go off and start another operation-such as a memory read. Because the cache operates in a write-through mode, if the address of the data being written into the DRAM array matches the lastrow-read address, data is also written back into the cache portion of the chip to maintain coherency. The address matching procedure is done by an 11-bit comparator that's built into the chip.

If two back-to-back random writes must be done in systems that run at 33 MHz or faster, a two-way interleaved memory architecture is recommended. Although data can be posted in 15 ns, in a single-bank system, the write to the DRAM block imposes a 65-ns cycle time, so one wait state would have to be added between back-to-back writes. For 25-MHz and slower buses, the EDRAM cycle time is not noticed as the CPU posts each word. In the two-way interleaved memory architecture, accesses are alternated between memory banks, consequently each bank is written to just every other cycle (see the table).

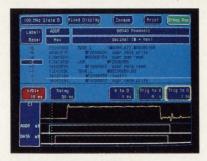
Compared to standard 4-Mbit DRAMs, the 2202 has a few more signal lines—dedicated Array Function and Write/Read (F and W/R, respec-



1. DI INTEGRATING a static KAM-based cache and main-memory DRAM onto the same chip, Ramtron eliminates a stand-alone secondary cache memory and simplifies system design. The close proximity of the SRAM and DRAM allows the entire cache to be refilled in one bus cycle via a 2048-bit-wide bus between the two sections (a). Flaunting a new pinout, the combination cache-DRAM chip packs many of the same control signals as a standard 1-M-by-4 DRAM. Added to the memory are refresh-control, array write and read, chip-select, and four center power and ground pins (b).

40 E L E C T R O N I C D E S I G N JANUARY 23, 1992

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COMBINATION CACHE AND DRAM CHIP

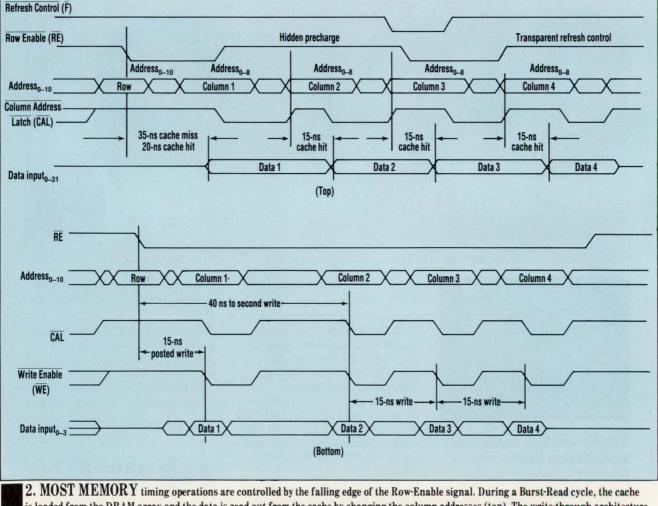
tively) pins, which determine DRAM array functions. A dedicated Chip Select— \overline{S} —is also available, and four dedicated center power and ground pins help minimize noise on the fast I/O lines (*Fig. 1b*). Most of the other pins are similar to the pins on a standard 1-M-by-4 DRAM. There are 11 address lines, corner power and ground pins, and four more control lines. The control lines are Row-Enable (RE), Column Address Latch (CAL), Output Enable (\overline{G}), and Write Enable (WE).

The memories have two types of read cycles: Major and minor. Major cycles begin when the \overline{RE} line is brought low when the \overline{F} and W/R pins are respectively high and low. In that state, the row addresses are latched into the address buffer as well as retained in the last-read-row (LRR) latch. Access is then possible to the DRAM array, the cache is filled, and data is valid on the output pin—all within 35 ns of the $\overline{\text{RE}}$ being asserted (brought low). If the row being read is the same as the last row that was read, then the cache is not refilled and the data is valid in 20 ns from $\overline{\text{RE}}$ (Fig. 2, top).

Minor read cycles don't require the assertion of the $\overline{\text{RE}}$ line and only need the presentation of a column address in conjunction with the assertion of the $\overline{\text{S}}$ and $\overline{\text{G}}$ signals. Data from the cache reaches the output pins in 15 ns from the column address. That data represents the contents of the most-recently read row (from the last major read cycle) as modified by subsequent write cycles that have a row address common to that of the current cache.

The short, 25-ns, RE precharge time, coupled with the EDRAM's ability to release the RE line as soon as row addresses are latched in, permits the precharge to take place during data accesses. This eliminates the need for interleaved memory banks and, in turn, simplifies system design. The fast access time for reads from the embedded cache allows most CPUs to burst in data at the rate of one word every clock cycle, again, without interleaving or a bank of SRAMs for a discrete secondary cache.

The \overline{F} pin is polled by the on-chip



2. MOST MEMOR I timing operations are controlled by the falling edge of the Row-Enable signal. During a Burst-Read cycle, the cache is loaded from the DRAM array and the data is read out from the cache by changing the column addresses (top). The write-through architecture of the cache allows the first word to be latched into the posted-write register on the memory chip. Data, however, can be read from the cache portion of the chip while the posted word is being written into the DRAM array. If the processor generates sequential write bursts within a row, the effective write time is 25 ns for the first cycle and 15 ns for each subsequent write cycle (bottom).

42 E L E C T R O N I C D E S I G N JANUARY 23, 1992

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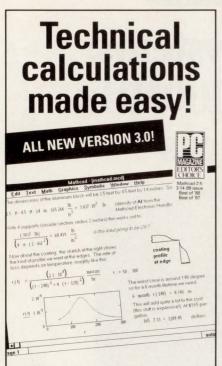
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COMBINATION CACHE AND DRAM CHIP

DRAM logic when \overline{RE} is asserted. When \overline{F} is detected on the falling edge of RE, an internal refresh cycle is executed. An internal counter supplies the row address, and the counter is updated at the end of the $\overline{\text{RE}}$ cycle. When $\overline{\text{F}}$ refresh is used, at least $1024 \overline{F}$ cycles must be executed every 16 ms. Minor reads (reads from the cache) can be performed during an \overline{F} refresh cycle. Data can be accessed in the cache by changing the column addresses and optionally toggling the \overline{CAL} and \overline{G} (with \overline{S} low). S must also be asserted if minor cycle reads are executed during the \overline{F} refresh operation.

Write cycles take place when the \overline{F} and W/R pins are both high and the RE pin is asserted. Data gets latched into the chip when the \overline{WE} line is asserted. Once the data is latched in, the chip can ignore the logic state of the data-input pins. That, in turn, permits the subsequent cache accesses to be concurrent with the internal physical write operations. Such a capability is possible when the address to be written is equal to the address to be read (a special case of the Read-Modify-Write operation). This scheme permits very fast memory-to-memory transfers and makes it easy to implement write "posting" without external datapath latches.

The on-chip cache employs a writethrough architecture to ensure coherency between the cache data and the DRAM-hosted array data. An onchip 11-bit address comparator monitors the write-cycle row addresses. If the address is equal to the current cache address, the comparator will appropriately modify the selected data. Writes are physically initiated on the chip by the later assertion of either the CAL or WE line. A minor read cycle can begin as soon as CAL and WE are both high if a cache hit has occurred (*Fig. 2, bottom*).

To build a memory subsystem for a 32-bit CPU, one bank of eight 2202 chips would form a 4-Mbyte main memory with 2 kbytes of cache (organized as 1 M by 32 of DRAM and 512 by 32 of integrated secondary cache). If parity is needed, one of the 2212s with the write-per-bit capability can be added to form a 36-bit-wide, 1-Mword-deep memory—similar to the DM1M36SJ, a 72-contact singlein-line memory module.

To control such a memory subsystem, a custom chip or high-performance a field-programmable gate array would be used to implement the logic that controls the cache and DRAM accesses. At 25 MHz and below, an FPGA could probably be used to handle the timing requirements, while for 33-MHz and faster systems, gate-array or standard cellbased controllers would probably have to be used to handle the sub-15ns critical signal timing.

The logic required for that controller chip would include multiplexers for the parity data and two banks of address lines (A2-10 and A11-21), as well as decoders for the bank selection, and boot memory address. Additional logic is needed for a refresh signal divider, address comparators, and a state machine that controls the timing for boot-memory control. Banks 0-3 and Banks 4-7, and the processor. In small systems, a single SIMM provides the entire 4 Mbyte DRAM space and 2 kbytes of cache. Larger systems can be created by adding more SIMMs.

PRICE AND AVAILABILITY

The three versions of the 4-Mbit/2-kbit cache-enhanced DRAM include the DM 2200 with a 4-M-by-1 organization, the DM 2202 with a 1-M-by-4 organization, and the DM 2212 which is also a 1-M-by-4 chip, but with a write-per-bit capability. The chips will initially be offered in 28-lead smalloutline J-lead 300-mil-wide plastic pack-ages. In lots of 10,000 units, the chips sell for \$19.50 apiece (any organization). A reduced-speed version (20-ns cache access) will sell for \$15.60 in similar quantities. Samples of the DM 2202 are immediately available. The DM 2212 and 2201 will be sampled in the second quarter. Also available is the DM1M36SJ, a 36-bit-wide 1-Mword SIMM built from the 2202s and the 2212. In lots of 100, the 15-ns SIMMs sell for \$290 apiece, while the 20-ns version goes for \$236.

Ramtron International Corp., 1850 Ramtron Dr., Colorado Springs, CO 80921; Andy Brock, (719) 481-7000.

CIRCLE 511

HOW VALUABLE?	CIRCLE
HIGHLY	525
MODERATELY	526
SLIGHTLY	527

electronic design report 1/0, MEMORY CARDS



IC-CARD SPEC ADAPTS I/O TO MEMORY-CARD SLOT

breakthroughs in the plug-in IC card arena promise to impact all segments of the computing industry, from portable systems to high-end workstations, including test-andmeasurement equipment. Last Sep-

ecent technology

measurement equipment. Last September saw a major stride taken in this direction, when the Personal Computer Memory Card International Association (PCMCIA) took the wraps off Release 2.0 of the PC Card Standard (see "What is the

JANUARY 23, 1992

ELECTRONIC

RICHARD NASS

PC-CARD STANDARD RELEASE 2.0 UNLEASHES A MYRIAD OF APPLICATIONS.

PCMCIA?," p. 46).

The standard was jointly accepted by the PCMCIA and the Japanese Electronics Industry Development Association (JEIDA). JEIDA was responsible for laying the initial ground work on many card issuesthe PCMCIA actually adopted many of their standards. When the Release 2.0 discussions began, the two groups put their heads together on many issues. They realized the importance of working collectively, because while many of the card-related systems come from Japan, the Japanese supply card-related components, as well as the cards themselves, to the U.S. The two groups plan to continue their joint cooperation in future endeavors.

Release 2.0 is divided into three parts-electrical (interface), physical, and software. Six different types of chips are outlined for use in the cards: ROM, one-time programmable ROM, static RAM, UV EPROM, flash EPROM, and EEPROM. One of the keys to Release 2.0 is that it introduces new applications in the form of I/O cards (Release 1.0 only defined memory cards). While memory cards find their niches in portable and industrial applications, I/O cards are sure to turn up for countless applications because of their ruggedness.

Che Personal
ard Interna-
MCIA) tookBefore this can happen, though, a
number of challenges brought on by
I/O cards must be conquered. These
include designing and implementing
the needed hardware for I/O expan-
D E S I G N 45

ELECTRONIC DESIGN REPORT 1/O, MEMORY CARDS

sion on the card. Another challenge is that many lines of complex code must be written to make this a viable solution. The code includes BIOS, device-driver software, and core-BIOS modifications. While most PCMCIA members are working on hardware solutions, companies like Phoenix Technologies, Norwood, Mass., and Award Software, Los Gatos, Calif., and others, are plugging away with the software.

The PCMCIA card slot will eventually serve as an I/O expansion slot, similar to the expansion slots found in the backplanes of desktop systems. Hence, users can plug in any number of expansion cards when they become available. "Think of the IC card of the future as the add-in slot of the present. Almost all PC add-in cards can be used in a similar way in the form of IC cards," says Bill Ringer, product manager for modem cards at Intel Corp., Folsom, Calif. For example, SunDisk Corp., Santa Clara. Calif., is developing a solid-state disk drive on a card that will take advantage of the I/O expansion capabilities. One card that's already in production is a plug-in modem, the Modem 2400+, from Intel (Fig. 1).

COMMUNICATIONS ON A CARD

The Modem 2400+ contains a UART, a microcontroller, and an analog front-end. It supports the Hayes AT command set and most communication software, as well as the MNP 5 protocol for error correction and data compression. Two versions of the card are available, one for use in North America and one for Japan. In quantities of 1000, the Modem 2400+ sells for \$200 (\$230 for the Japanese card).

Intel says that no trade-offs were necessary to fit the modem into such a small package. The company felt that just achieving the small size and innovative packaging was breakthrough enough. But expect a 9600baud product in the not-too-distant future.

Intel also announced a third member of its flash-card family, a 2-Mbyte version (iMC002FLKA); the family already has 1- and 4-Mbyte



1. THE MODEM 2400 + fits in a PCMCIA Type II package (5-mm thick). The 2400-baud modem, from Intel, is compatible with the PCMCIA Release 2.0 specification, as well as the company's ExCA standard. No external power is needed to run the modem.

cards. And higher densities are looming on the horizon. The 2-Mbyte card is built with the same architecture that was used on the previous two cards. In large quantities, it sells for \$375.

Other applications under investigation include facsimile and cellular modem cards. The cellular modem card would allow a portable computer to access the phone system without being connected to a phone line. Wired and wireless LAN cards are another possibility. This would permit users to own just a portable system. If the portable could be connected to a LAN, a desktop wouldn't be needed. A SCSI port is also being looked into because of the growth of SCSI peripherals.

T AND M, TOO

Another area where memory cards are making some strides is in test and measurement. LeCroy Corp., Chestnut Ridge, N.Y., recently released a PCMCIA-compatible card containing 23 standard templates to test various communications signals. The card comes as a \$700 option to the company's latest family of oscilloscopes, Models 9410, 9414, 9424, 9430, and 9450A.

Release 2.0 contains enhancements, changes, and additions to Release 1.0, which was announced in May of 1990. The enhancements include clearer card-function definitions, improved memory performance using the +Reset and -Wait signals, the addition of IEEE nomenclature to timing charts, and reliability-requirement and testing-methods definition. Some additions include dual-voltage operation and an execute-in-place (XIP) specification. The XIP spec lets a system execute code directly from a card without loading the code into the system's RAM.

The specification outlines two types of cards: Type I and Type II. Each is 85.6 by 54 mm, yet Type I is 3.3 mm thick and Type II is 5 mm thick. The two different card types appear in different applications. The 5-mm cards are used for PLCC-type

WHAT IS THE PCMCIA?

he Personal Computer Memory Card International Association (PCMCIA) is made up of over 150 members, including major manufacturers and OEMs worldwide, representing every level of PC-card development. These companies include Apple, AT&T, Fujitsu, IBM, Intel, Mitsubishi, Phoenix Technologies, Poqet Computer, SunDisk, and To-

shiba. There are three levels of membership: Executive, Associative, and Affiliate. The association's objectives are to establish, maintain, and promote a worldwide standard for IC cards. For more information, call or write to the PCMCIA at 1030B E. Duane Ave., Sunnyvale, CA 94086; (408) 720-0107. A Taiwan-based chapter is located at the Institute for Information Industry in Taipei.

electronic design report 1/0, MEMORY CARDS

Memory-only card interface I/O and memory card interface (always available at card insertion) (available only after card and socket are configured)									
Pin	Signal	1/0	Function	+/-*	Pin	Signal	1/0	Function	+/-*
1	GND		Ground		1	GND		Ground	
2	D3	1/0	Data bit 3		2	D3	1/0	Data bit 3	
3	D4	1/0	Data bit 4		3	D4	1/0	Data bit 4	
4	D5	1/0	Data bit 5		4	D5	1/0	Data bit 5	
5	D6	1/0	Data bit 6		5	D6	1/0	Data bit 6	
6	D7	1/0	Data bit 7		6	D7	1/0	Data bit 7	
7	CE1	1	Card Enable	-	7	CE1	1	Card Enable	100 -
8	A10	1	Address bit 10		8	A10	1	Address bit 10	
9	OE	1	Output Enable	-	9	OE	1	Output Enable	-
10	A11	1	Address bit 11		10	A11	. 1	Address bit 11	
11	A9	1	Address bit 9		11	A9	1	Address bit 9	
12	A8	1	Address bit 8		12	A8	1	Address bit 8	
13	A13	1	Address bit 13		13	A13	1	Address bit 13	
14	A14	1	Address bit 14		14	A14	1	Address bit 14	
15	WE/PGM	1	Write Enable	-	15	WE/PGM	1	Write Enable	_
16	RDY/BSY	0	Ready/Busy	+/-	16	IREQ	0	Interrupt request	- 1
17	VCC				17	VCC			
18	VPP1		Programming supply voltage 1		18	VPP1		Programming and peripheral sup	pply voltage 1
19	A16	1	Address bit 16		19	A16	1	Address bit 16	
20	A15	1	Address bit 15		20	A15	1	Address bit 15	
21	A12	1	Address bit 12		21	A12	1	Address bit 12	
22	A7	1	Address bit 7		22	A7	1	Address bit 7	
23	A6	1	Address bit 6		23	A6	1	Address bit 6	
24	A5	1	Address.bit 5		24	A5	1	Address bit 5	
25	A4	1	Address bit 4		25	A4	1	Address bit 4	
26	A3	1	Address bit 3		26	A3	1	Address bit 3	
27	A2	1	Address bit 2		27	A2	1	Address bit 2	
28	A1	1	Address bit 1		28	A1	1	Address bit 1	
29	AO	1	Address bit 0		29	AO	1	Address bit 0	
30	DO	1/0	Data bit 0		30	DO	1/0	Data bit 0	
31	D1	1/0	Data bit 1		31	D1	1/0	Data bit 1	
32	D2	1/0	Data bit 2		32	D2	1/0	Data bit 2	
33	WP	0	Write Protect	+	33	IOIS16	0	I/O port IS 16 bit	and so a
34	GND		Ground		34	GND	Ŭ	Ground	
35	GND		Ground		35	GND		Ground	
36	CD1	0	Card Detect	-	36	CD1	0	Card Detect	
37	D11	1/0	Data bit 11		37	D11	1/0	Data bit 11	
38	D12	1/0	Data bit 12		38	D12	1/0	Data bit 12	
39	D13	1/0	Data bit 13		39	D13	1/0	Data bit 12	
40	D14	1/0	Data bit 14		40	D14	1/0	Data bit 14	
41	D15	1/0	Data bit 15		41	D15	1/0	Data bit 15	
42	CE2	1	Card Enable	_	42	CE2	1/0	Card Enable	
43	RFSH	i	Refresh		43	RFSH		Refresh	
44	RFU		Reserved		44	IORD		I/O Read	
45	RFU		Reserved		44	IOWR	1	I/O Write	
46	A17	1	Address bit 17		45	A17		Address bit 17	
47	A18	1	Address bit 18		40	A17 A18		Address bit 18	
48	A19	1	Address bit 19		47 48	A19		Address bit 19	
49	A20	1	Address bit 20		40	A19 A20	1	Address bit 20	
49 50	A20 A21		Address bit 20		49 50	A20 A21		Address bit 20 Address bit 21	
51	VCC		Auguess bit 21		50	VCC		Address Dit 21	
52	VPP2		Programming supply voltage 2		52	VPP2		Programming and poriphoral sur	nly voltage 0
52 53	A22	1	Address bit 22		52	A22	1	Programming and peripheral sup	phy voltage 2
53 54	A22 A23		Address bit 22 Address bit 23		53 54	A22 A23	1	Address bit 22 Address bit 23	
55	A23 A24		Address bit 23		54	A23 A24			
56	A24 A25	100	Address bit 25		55	A24 A25	1	Address bit 24	
50 57	RFU	1	Reserved					Address bit 25	
57 58		1			57	RFU		Reserved	
	RESET	0	Card reset	+	58	RESET	1	Card reset	+
59	WAIT	0	Extend bus cycle	-	59	WAIT	0	Extend bus cycle	-
60	RFU		Reserved		60	INPACK	0	Input port acknowledge	-
61	REG		Register select	-	61	REG	1	Register select	-
62	BVD2	0	Battery voltage detect 2		62	SPKR	0	Audio digital waveform	-
63	BVD1	0	Battery voltage detect 1		63	STSCHG	0	Card status	-
64	D8	1/0	Data bit 8		64	D8	1/0	Data bit 8	
65	D9	1/0	Data bit 9		65	D9	1/0	Data bit 9	
66	D10	1/0	Data bit 10		66	D10	1/0	Data bit 10	
67	CD2	0	Card detect	-	67	CD2	0	Card detect	
68	GND		Ground		68	GND		Ground	

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ELECTRONIC DESIGN REPORT

packages, such as UV-erasable PROMs. They permit a greater variety of circuitry, suitable for present and future I/O cards. Applications that only require memory cards, such as handheld computers and digital cameras, can take advantage of the 3-mm card, thus saving 2 mm. However, notebook and palmtop systems are now being developed with 5mm slots. Manufacturers of these systems feel that the 2-mm trade-off is a small price to pay for the vast number of applications that will be available.

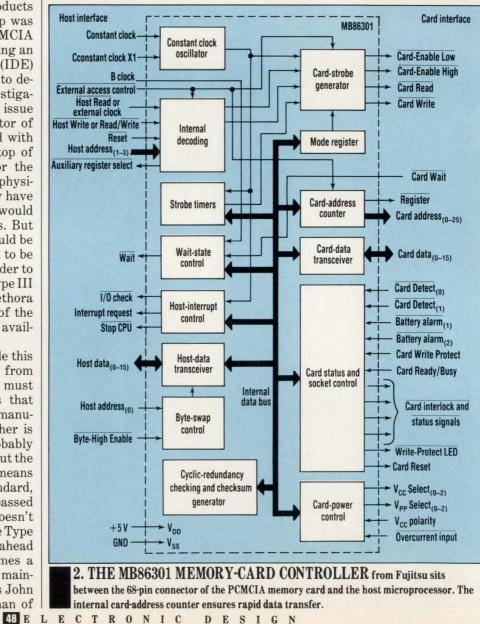
A third card, Type III, is currently under investigation. With the Type III card, rotating-storage products can be used. A working group was recently formed within the PCMCIA to explore the viability of putting an integrated-device-electronics (IDE) interface into a PCMCIA slot to determine whether further investigations are necessary. One key issue here is the physical form factor of such a slot. Systems designed with two PCMCIA slots-one on top of the other-are candidates for the Type III slot. In this case, the physical form factor wouldn't really have to change; the Type III card would just occupy both Type II slots. But more than a few eyebrows would be raised if the Type III card had to be increased in height or made wider to fit into that form factor. The Type III form factor could open up a plethora of new applications, because of the additional space that becomes available in the cards.

The PCMCIA feels that while this issue does invite competition from the rotating-media makers, it must be addressed. One reason is that some of the group's members manufacture rotating media. Another is that those members would probably pursue the issue, with or without the consent of the PCMCIA. "If it means a radical change to the standard, then it probably wouldn't be passed by the association. But if it doesn't pass, then the group behind the Type III specification might just go ahead and do it anyway. If it becomes a standard, the PCMCIA could maintain some control over it,"says John Reimer, president and chairman of the PCMCIA (Reimer is also the vicepresident of marketing at SunDisk Corp.).

Types I and II card connectors contain 68 pins, some of which are saved for future definitions *(see the table)*. One pin, a "no-connect" pin, was left entirely undefined. In addition, some informal discussions have bandied about the issue of applying some of the unmultiplexed pins to direct memory access.

Under the specifications of Release 2.0, the card socket transparently changes from a memory card to an I/O slot, from the user's perspective. Release 2.0 defines the elec-

trical signals at the interface and stops there. Intel decided to take the specification one step further by developing its Exchangeable Card Architecture (ExCA), which sits on top of the PCMCIA interface specification. The company felt that this was necessary because some cards and interfaces being built were compliant with Release 2.0, yet weren't interchangeable between systems. That was because the cards contained different internal architectures. ExCA ensures that all of the cards will have the same architecture, thereby guaranteeing compatibility between systems.





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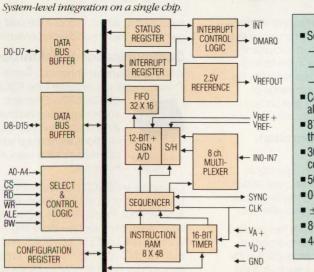
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ELECTRONIC DESIGN REPORT I/O, MEMORY CARDS

The PCMCIA is reserving judgment on ExCA because the group hasn't yet fully evaluated all aspects of the standard. But the initial reaction is that it could be a viable solution after resolving some of the issues. "Because of Intel's clout in the 80X86 marketplace, the ExCA architecture will have an impact on PCMCIA slots," says Reimer. He feels that as long as the specification remains open to the whole market. without creating a monopoly for Intel, hindering future performance, or prohibiting cost reductions, there's a good chance that it will forge ahead as a de facto standard. Reimer notes that although the PCMCIA has only had a few informal discussions with Intel to make ExCA a PCMCIA standard, both parties are open to suggestions.

Intel simultaneously announced an interface controller that supports both memory and I/O cards. The 82365SL, built to the ExCA specification, works in tandem with the 386SL low-power microprocessor. The chip features power-management support and supplies a direct interface to the ISA bus and two PCMCIA sockets. It eliminates the need for system-configuration jumpers by dynamically configuring any card in the system upon power-up and reset. This entire interface can be implemented in less than 2 in.² of board space. In OEM quantities, the 82365SL sells for \$35.

The MB86301 from Fujitsu Microelectronics Inc., San Jose, Calif., is

similar to Intel's 82365SL-it's also compatible with Release 2.0. The chip was jointly developed by Fujitsu and Databook Inc., Ithaca, N.Y., the latter one of the pioneers in IC-card applications. Unlike the Intel chip, however, the single-chip interface controller handles just memory cards, not I/O cards. Built-in features include cyclic redundancy checking (CRC) and checksum error detection. Checksum control is done by adding up all of the bytes, throwing out the high-order result, and keeping the lower-order one or two bytes. That's the method commonly used on EPROMs to verify their integrity when they're programmed. The chip lies between the generalpurpose host microprocessor's data, address, and control lines, and the memory card (Fig. 2).

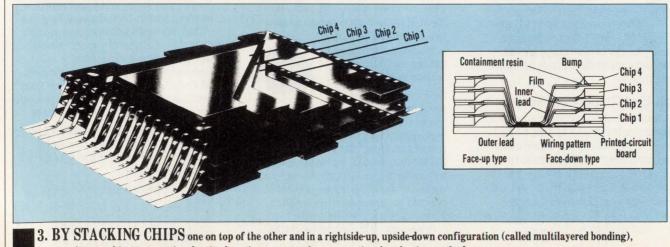
"This configuration minimizes the overhead that's needed to control the host microprocessor while interfacing the memory card," says Dan Sternglass, president of Databook. The MB86301 is available now; an evaluation board can be obtained from Fujitsu for \$499.

A second part from Fujitsu, the MB86965 EtherCoupler, is an integrated Ethernet LANchip that includes a controller, a 10Base-T transceiver, an encoder-decoder, bus-interface logic, and filters. With the device, designers can build a LAN adapter with just five chips, making it suitable for PCMCIA-compatible LAN cards. Samples of the MB86965 are available now. Production should commence at the beginning of the second quarter. In 1000-unit quantities, the chip sells for \$30.60. Additional discounts exist for larger quantities.

Dual-operating voltages add another dimension to Release 2.0. Although all cards will initially operate at 5 V, some will be able to powerdown to 3 V. When the card is first plugged in, the system will read the card-information structure, then determine whether the card is intended for operation at 3 or 5 V. Cutting the voltage to 3 V reduces the power consumption, a critical factor in portable systems. The dual-voltage card differs from a 3-V-only card, which won't work in a PCMCIA slot.

RESET UPON POWER-UP

As outlined in Release 2.0, a card can be reset to a known state by employing the +Reset signal. In other words, a card already in place in a system will reset itself when the system is powered up. The +Reset signal clears the card-configuration option register, placing the card in an unconfigured state. +Reset also signals the beginning of card initialization. The system must place the +Reset signal in a high-impedance mode whenever a card is being powered up. The signal must remain at high impedance for at least 1 ms after V_{CC} becomes valid. The specification points out that all configurable cards must monitor +Reset and return to an unconfigured state when the signal is active.



Panasonic can achieve a mounting density four times greater than conventional packaging methods. 52 E L E C T R O N I C D E S I G N

JANUARY 23, 1992

ELECTRONIC DESIGN REPORT

A card remains in the unconfigured state until the card-configuration option register has been written to with a valid configuration. The card could generate a power-on +Reset internally or the signal can be pulled up to V_{CC} through a resistor greater than 100 k Ω on any cards that require the reset feature. This will ensure that an inserted card is reset before the signal pins make contact with the socket. While the PCMCIA recognizes the need for a live-insertion specification, a standard to guarantee data retention hasn't yet been decided on, although it's in the works.

The –Wait signal was included in Release 2.0 to synchronize fast hosts with slow cards. In other words, the signal tells the high-speed host system (with a 386 or 486 processor) to wait for the card that doesn't operate as fast. The card asserts this signal to delay completion of the memoryor I/O-access cycle in progress.

Error detection, a necessary feature for IC cards, is a key concern because the environment and operation of any removable media has the potential to introduce errors. Some causes of errors include electrostatic discharge (ESD) exceeding the card's rating, users pulling cards out of systems while the cards are being accessed, or mechanical shock interrupting the "keep-alive" power of a battery-backed card. These events are rare enough that consumergrade products might not require protection against them.

High-reliability applications, such as industrial, military, or medical systems, require error detection. CRC and checksum approaches are both recognized by the PCMCIA standard, and are appropriate for proprietary formats. Error detection isn't as important for random errors because the intrinsic error rate in a system that's properly designed is quite low.

THE LAYERED METAFORMAT

The first piece of information contained in each card's memory is a metaformat header that describes the card's data organization, including both hardware and software. The

metaformat is organized in four layers. The basic compatibility layer contains only the minimal information needed to access the card, such as device speed, type, and size, as well as a programming algorithm if it's required. The second layer, the data-format layer, specifies what type of data blocking and error checking the card implements. This is analogous to a floppy disk's physical formatting. Both blocked-data and raw-byte formats (a block of data that's just a binary image or a bunch of data with no higher-level organization) are supported, as well as CRC and other types of error detection. Mixed-format cards like ROM and RAM are allowed. In the data-format level, nothing is DOSspecific.

The third level, the data-organization layer, is DOS-specific. Here, the defined file system can be the fileallocation-table (FAT) file system used on conventional disks, the flash file system (FFS) developed for UV and flash memories, or XIP. When a FAT file system is used, certain defaults are defined that make up a minimum interchange format. The last layer can be customized so users can define their own data organizations. Even cards with a proprietary data format at this level can be recognized by any system, as long as they contain the proper metaformat header.

X-ECUTE IN PLACE

Two types of XIP support are defined within Release 2.0: EXIP and LXIP. EXIP refers to the ability of 386- and 486-type processors, with their virtual-memory capability, to map a whole card into one address space. For example, instead of forcing the system's RAM to store 16kbyte pages, the whole card (containing a few Mbytes) or just portions can be mapped because 386/486 systems have such large virtual- and physical-address spaces.

MATLXIP is used in applications struc-
tured to operate in a 16-kbyte paged-
execution mode, similar to the Lo-
tus/Intel/Microsoft (LIM) 4.0 envi-
udingudingronment. The differences between
LXIP and EXIP don't change theELCTRONICDESI

JANUARY 23, 1992

card's metaformat, data structures, or driver architecture. They're only noticeable in the applications-programming interface. However, a significant difference exists in the hardware support required and in the way applications are structured for the two environments.

The standard assumes that an XIP partition only stores XIP applications and isn't part of a FAT or FFS partition. Only two tuples are relevant to XIP-format and organization (a tuple is a block of data that appears in the card-information structure and records pieces of data concerning the card's layout). The format tuple defines the card's datarecording format and the location and size of its associated memory region. The organization tuple defines the organization of the data within a specific partition. The organization tuple must follow a format tuple in the card's memory to be associated with it.

Descriptive information, such as the card-hardware and data-formatting information, is stored in an attribute memory-address space and is accessible when the REG pin is active. Release 2.0 allows physically separate memory to be used. This type of non-card ROM could convey detailed card information to the system software, relieving the end user from this burden.

In cases where there's no attribute memory, the REG pin is a no connect, and the hardware and format descriptions are stored starting at the beginning of the main memory. This is standard practice with ROM cards, where the descriptions can be split among the two address spaces. In this case, user flexibility is retained to define the data organization, partitions, or other information, while allowing the card manufacturer to supply the hardware information in ROM.

To retain compatibility with 8-bit host systems, the card-information structure must be stored on even bytes only. The contents of odd-byte attribute memory are undefined. The specification describes the tuples as if the bytes were recorded consecutively. When the tuple is re-N 53

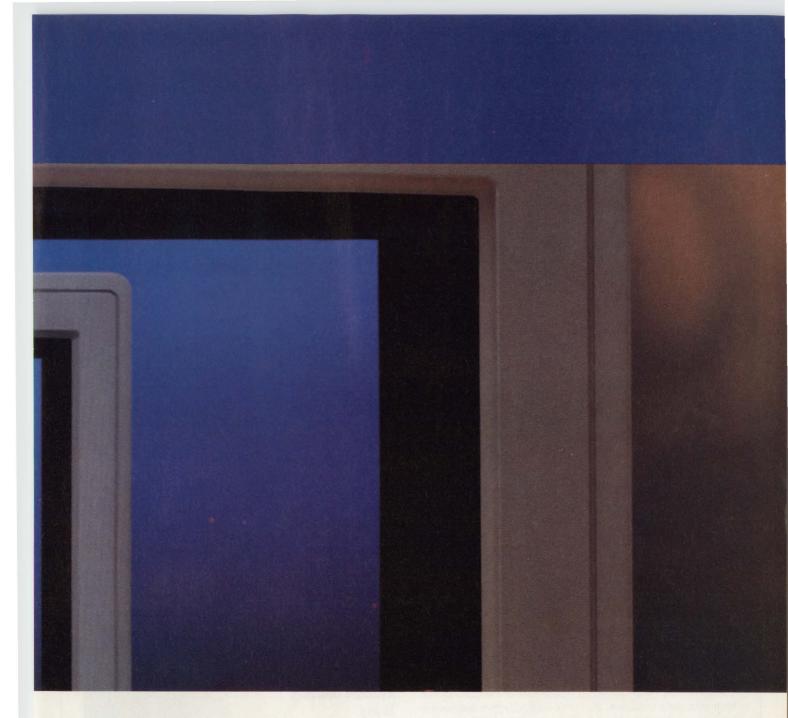
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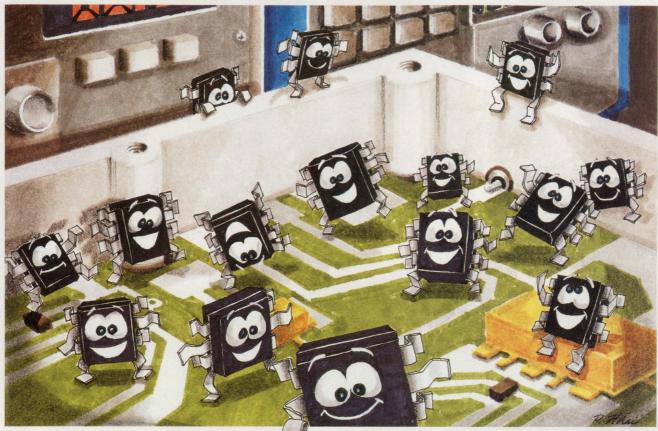
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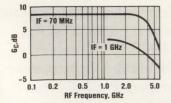
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electronic design report I/O, MEMORY CARDS

corded in attribute memory space, it occupies even bytes. However, when a tuple is recorded in common memory space, it must be recorded in consecutive bytes. Using common memory for tuple storage is indicated by a long-link tuple. Card-information structure stored entirely in common memory must begin with even bytes only. The tuple is then linked to the region of common memory containing the remainder of the card-information structure in contiguous bytes.

Tuples can be put into three categories: control, basic compatibility, and card information. Control tuples govern the metaformat-linked list, including national language definition and checksum control. The basic compatibility tuples describe device characteristics, such as type, speed, and size. The card-information tuples contain specific information regarding organization of data within a partition.

A sequence of tuples containing at least the minimum required information constitutes a partition descriptor. The card-information structure can contain multiple partition descriptors, allowing several, independent logical volumes on one card. These partitions can contain standard formats. Each independent partition's definition begins with a format tuple. Programmable memory cards, including ROM and flash, are identified by the JEDEC identifier tuple. A RAM card is characterized by its device-information, ID, speedtype, and size fields.

In a memory-card system, buffering, control-signal isolation, and power switching are major circuitdesign aspects affecting system and card reliability. Card power-up and buffer-enabling must be triggered by detecting card presence after an appropriate delay. This is where the -Wait signal comes in. Typically, system software leaves these buffers disabled, and removes the power to avoid problems when a card is removed. Furthermore, the analog switches and their control inputs that isolate the control signals must be biased to avoid possible data corruption during system power-up and

-down with the card inserted. A diode-isolated supply solves this problem, with buffers controlled by an analog power monitor.

ESD can also cause reliability problems. System designers must supply a low-impedance path to ground to dissipate any charge that may build up on a card, which affects packaging design. In addition to ensuring that the cards pass all of the reliability tests, companies must try to squeeze the maximum storage capacity into the cards. Panasonic Industrial Co., Secaucus, N.J., does just that by using a multilayer-bonding technique (MBT). MBT increases the mounting density of the cards by stacking the chips on top of each other (Fig. 3). Several stacks of up to four chips can be interconnected on the same substrate.

RELIABILITY AND TEST

Release 2.0 specifies strict reliability standards for the interconnect system. In office and harsh environments, the guaranteed number of insertions and ejections must surpass 10,000 and 5000, respectively. An office environment is defined as having year-round air conditioning and humidity control. The harsh environment has no air conditioning or humidity control, yet contains normal heating and ventilation.

Standards for the total insertion and pulling forces are 8.8 lbs. and 1.5 lbs./min., respectively, at a speed of 1 in./min. The outermost plating of the socket- and pin-contact areas must be fabricated with gold or some other plated material that's compatible with gold. The cards must be fully functional in the 0 to +55°C temperature range while withstanding storage temperatures from -20 to +65°C. All cards must undergo tests for thermal shock, moisture resistance, ESD, X-ray and ultraviolet light exposure, vibration, shock, bending, dropping, torque, and card warpage.

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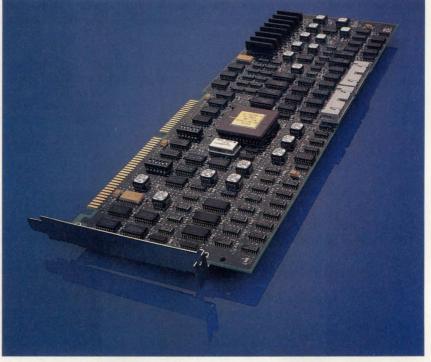
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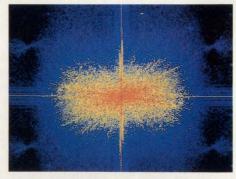
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DESIGN APPLICATIONS

MICROCONTROLLER-BASED DESIGN USES MINIMAL SUPPORT ICS AND CODE TO GET HIGH-ACCURACY ANALOG-TO-DIGITAL CONVERSION

TRY SINGLE-SLOPE A-D CONVERSION FOR A LOW-COST 12-BIT SOLUTION



hen high speed isn't a top priority, several options exist for implementing high-resolution analog-to-digital conversion in cost-sensitive products. Typical of such applications are measurements for automotive (oil temperature/pressure), industrial (process temperature control, weighing scales), and consumer (home thermostats and ranges) products. Functions like these are often performed cost-effectively with microcontrollers. For example, the cost of a discrete single-slope analog-to-digi-

tal converter (ADC), including additional interface hardware to the microcontroller, is less than \$1. This compares favorably with dedicated 12-bit hardware solutions that can cost more than \$10 in high volume.

Before going into detail on how to build a discrete single-slope circuit, let's look at some alternative solutions. One is the 12-bit successive- approximation integrated circuit, which has the advantage of easy system interface and relatively high conversion speed (between 7 and 100 µs). The major disadvantage is very high cost, especially for wide operating temperature ranges. Two other options are the single- and dual-slope ADC. For applications up to 14 bits, the easier-to-apply single-slope approach can be used.

For applications requiring greater than 14-bit resolution, consider a dual- or multi-slope approach, which uses the input signal to drive an integrator that can easily average out noise. There are several variations of a dual-slope ADC. Typically, the input V_{in} is integrated for a fixed amount of time (determined by the required resolution). Then the integration is ramped in the opposite direction by switching in a reference voltage of opposite polarity to $V_{\rm in}.$ The amount of time required to ramp back to zero determines the magnitude of Vin. However, compared to the single-slope approach, the software overhead and hardware is more involved. The dual-slope technique requires more analog switches and two voltage references to produce multiple ramps, plus an additional calibration cycle within software to eliminate offset errors.

Earlier integrated-circuit versions of the single-slope ADC have the major drawbacks of low accuracy (8 bits typical), poor linearity ($\pm 0.5\%$), and a cost

KEVIN DAUGHERTY

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exceeding \$1, which is about the same as a common 8-bit successive-approximation ADC.

Before starting the design of an ADC, the first thing to determine is system accuracy and resolution requirements. Absolute accuracy requires a stable voltage reference that matches the system accuracy needs.

For example, 12-bit accuracy requires a 0.025% tolerance $(1/4096 \times 100)$, for which some calibration is necessary, and low temperature drift (about 5 ppm/°C). Applications that require relative measurements between two or more signals (ratiometric) can use a low-cost voltage reference with no calibration.

The host microcontroller's workload and the rate of change of the signal to be measured dictates the required speed and conversion technique for the ADC. More often than not, the time needed to perform all system tasks is the limiting factor. In applications where the microcontroller needs to perform monitoring and control functions that can't be easily interrupted, a relatively software-independent method is best. This approach determines how the ramp voltage is timed with the onchip timer. The conversion speed is directly proportional to the required resolution and the microcontrollertimer clock rate.

Low-cost microcontrollers, such as National Semiconductor's COP800 line, have 16-bit timers that clock at 1 μ s. This results in a conversion speed of approximately 5 ms for 12-bit accuracy. When higher speed is needed, microcontrollers like the NSC COP820CJ can operate as fast as 250 ns, resulting in 1.5-ms conversions.

LAYOUT CONSIDERATIONS

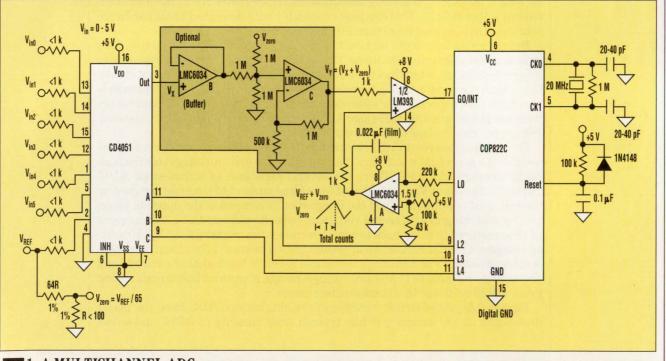
Good layout is critical for any high-accuracy analog circuit. This involves using decoupling capacitors on the integrated circuits, minimizing circuit traces, using input filters, and separating analog and digital grounds. In addition, a guard ring around the integrator inputs could be added and connected to the reference voltage. This will limit the leakage current caused by the circuit board.

To create a single-slope ADC, a

voltage ramp, comparator, and a multiplexer in addition to a microcontroller are required. The heart of the design is the voltage ramp. The basic idea behind the single-slope ADC is to time how long a ramp voltage takes to reach a voltage input to a comparator. Full-scale counts can be determined by applying a reference voltage V_{REF} to the comparator and measuring the time to go from zero volts to V_{REF} . This time, T_X , is later used to measure other input voltages, V_X . For example, from equation 1, if T_{REF} is 4000 for a V_{REF} of 5 V and T_X is 2000 for V_X , then $V_X = 5$ V (2000/4000) = 2.5 V.

 $V_{X} = V_{REF}(T_{X} \text{ counts}/T_{REF} \text{ counts})(1)$

The voltage ramp for a singleslope ADC can be implemented with an LMC6034 quad CMOS amplifier set up as an integrator (Fig. 1). This arrangement offers a 12-bit accuracy, which requires very low input leakage current compared to the ramp charge current. The LMC6034 has a maximum input leakage current of 200 pA over a temperature range of -40 to +85°C. Other key features of the LMC family of op amps



1. A MULTICHANNEL ADC with 12-bit accuracy can be designed with an 8-bit microcontroller, a voltage comparator, a multiplexer, and an op amp. The LMC6034 op amp configured as a voltage-integrating ramp generator, A, is the heart of the ADC. Optional buffer op-amp B may be required to offset errors caused by the multiplexer input resistors. Op-amp C isn't mandatory for limited measurement ranges.

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is the ability to operate to ground on |the input with a single supply, and to swing extremely close (± 10 mV) to the supplies on the outputs.

This performance provides maximum ramp-voltage swing and range for the ADC. The 0.022- μ F integrating capacitor across the negative input and output of op-amp A uses a charging current of 6.8 μ A (1.5 V/ 220 k Ω resistor) to generate a positive linear ramp.

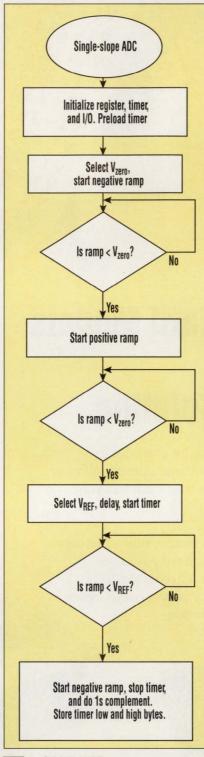
This capacitor must be a highquality film type, such as a polypropylene with high insulation resistance over temperature. Tolerances of the capacitor and resistor don't affect the circuit's accuracy because the changes in values would affect each measurement equally.

The values of the integrating capacitor and resistor are determined by the clock rate of the timer, the resolution, and the maximum voltage range. The component values shown are for a 16-ms ramp, a 5-V input range, and a counting rate of $1-\mu s/$ count (Fig. 1, again).

This counting rate produces overcounting because only 4096 counts (4.096 ms) are needed. Overcounting is required only if a software polling method is used to time the ramp, as opposed to the input-capture method. The capacitance value C can be calculated from $C = (\Delta T/\Delta V) \times I$, where ΔT is the resolution multiplied by 1/clock rate, ΔV is the differential input voltage range, and I is the charge current.

The microcontroller output L0 toggles between 0 and 5 V to ramp the integrator up and down. Conversions are performed during ramp-up, which is when L0 is at 0 V. The positive input of the op amp is referenced to 1.5 V, causing a constant 6.8- μ A (1.5 V/220 k Ω) current flow through the capacitor. When the positive-going ramp reaches the input threshold voltage at the comparator, the timer is stopped.

To get ready for the next conversion, L0 switches to 5 V and the discharge current is $(5 \text{ V} - 1.5 \text{ V})/220 \text{ k}\Omega$, or about 16 μ A. As a result, ramp-down is much faster than ramp-up, minimizing the time between conversions.



converthe dis- V)/220result, r than me be-**52** E L E C T R O N I C D E S

JANUARY 23, 1992

Comparator selection should be made on the basis of input bias current, single-supply operation, and input-voltage range. In the example shown in Fig. 1, the comparator is fed by the CD4051 8-channel multiplexer, which has several input resistors. Comparator input-bias offset current multiplied by the total input resistances leading up to the comparator must be kept below the resolution voltage of one LSB (least significant bit), or 1.2 mV for a 0-to-5-V range.

The LM393 dual comparator has an input-bias offset current of ± 100 nA. If this causes undesirable errors, then an LMC6034 CMOS buffer (B) can be used to eliminate the effects of the input resistance to the multiplexer. However, low-value resistors are still required for the inputs to the comparator.

Using a low-cost, 8-channel multiplexer (CD4051) makes a 6-channel ADC, with two channels reserved for a reference (full scale) and zero threshold. Crosstalk is the only important multiplexer specification of concern, and should not be a factor for the frequencies at which most applications operate.

The power-supply requirement depends on the voltage range required by the ADC. The 8-V supply shown in the example for the integrator and comparator is needed only for applications measuring input voltages above 3.5 V, which is the limitation of the comparator operating at 5 V. The multiplexer and microcontroller (COP822) are powered by 5 V. That enables the microcontroller's logic levels to drive the CMOS-level inputs of the CD4051.

In the example, V_{zero} is derived from V_{REF} using 1% tolerance resistors to equal $V_{REF}/65$. The idea is to create a zero voltage that allows some headroom for the ramp function. When the microcontroller drives the integrator down, the negative input must remain at 1.5 V. If the integrator overshoots by letting the output ramp bottom out at its lowest output voltage, the negative input will charge above 1.5 V.

surement of
sible.This condition would cause a sig-
nificant delay error when restartingDESIGN

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the positive ramp cycle for another conversion. Using a value for V_{zero} sufficiently above the minimum amplifier output voltage prevents this error. Op-amp C is used as a noninverting summing amplifier to add V_{zero} to each input (*Fig. 1, again*). This allows full 0 to V_{REF} measurements while restricting the ramp voltage swing to within the integrator output-voltage range.

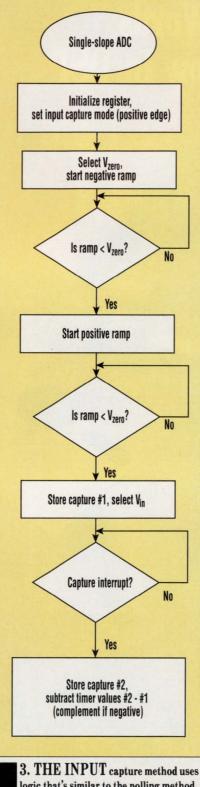
The conversion cycle starts with ground selected on the multiplexer. The summing amplifier, which adds V_{zero} to all inputs, sets the comparator threshold at $V_{in} + V_{zero}$. When the integrator ramps down and reaches V_{zero} , the microcontroller starts the positive ramp. When the positive-going ramp again crosses V_{zero} from the low side, V_{in} is selected and the timer starts counting. The integrator will continue to ramp up until the ramp equals the input voltage at the comparator.

The ramp time is directly proportional to the voltage input. The ramp starts with V_{zero} and continues until it reaches $V_{in} + V_{zero}$, so that the total differential voltage on the ramp is simply V_{in} .

For limited measurement ranges, op-amp C is optional. Feeding in V_{zero} $= V_{REF}/65$ on one of the input channels and operating the circuit without adding V_{zero} to each input provides a conversion range of 1/65 to full scale. Then V_{REF} should be measured, dividing the counts by 64 with simple shifting. Finally, the result in software should be added to each conversion. When V_{REF} is measured this way, the voltage range is just 64/65 of full scale with the first 1/ 65th of full scale not measured. The following illustrates how to handle the mathematics for this technique:

$$\begin{split} V_{\rm zero} &= 1/65 V_{\rm REF} \\ T_{\rm REF} &= 64/65 \ full \ scale \\ {\rm counts/volt} &= T_{\rm REF}/(64/65 V_{\rm REF}) \end{split}$$

Therefore, $T_{zero} = 1/65V_{REF}[T_{REF}/(64/65V_{REF})] = 1/64T_{REF}$, where T_{REF} is the time measurement for V_{REF} , which is actually only 64/65 of V_{REF} . Using the value of T_{zero} for the untimed portion of the ramp added to each measurement in software provides a linear result:



3. TILE TIVE OF capture method uses logic that's similar to the polling method. But for a given resolution, it generates less jitter. Input-capture measurements also have quicker conversions because overcounting and averaging aren't used.

$$\begin{split} V_{\text{in}} &= V_{\text{REF}} (T_{\text{in}} + T_{\text{zero}}) / \\ (T_{\text{REF}} + T_{\text{zero}}) \end{split}$$

If an accurate reference voltage is used, errors caused by the hardware circuitry are minimal and require no calibration.

As mentioned previously, the integrator resistor and capacitor don't cause any error if a good film capacitor is used. The conversion process automatically cancels the offset voltages of every op amp and the comparator. By starting the conversion with the ramp below V_{zero} and going in the positive direction, the threshold voltage of V_{zero} will include a net V_{offset} . This V_{offset} has the same magnitude and polarity when the ramp voltage again reaches the voltage to be measured later on in the conversion cycle. The delta voltage on the ramp is still only $V_{in} = (V_{in} + V_{zero} + V_{offset}) - (V_{zero} + V_{offset})$.

$$\begin{split} & V_{offset}) - (V_{zero} + V_{offset}). \\ & \text{In applications requiring only a} \\ & \text{limited range (excluding 0 - [1/65] \\ times voltage range]), the error \\ caused by the V_{zero} resistor network \\ & \text{is only 1/65\% using 1\% resistors. For \\ the full 0 V to V_{REF} range option, the \\ & \text{actual value of } V_{zero} \text{ isn't important, } \\ & \text{but the effect on the summing ampli-fier is. Because a CMOS amplifier (C) \\ & \text{with extremely low input-leakage } \\ & \text{current can be used, high-value input } \\ & \text{resistors (1 M\Omega) can also be employed. These, combined with a low \\ & \text{value R } (<100 \ \Omega) \text{ for deriving } V_{zero}, \\ & \text{don't alter } V_{zero} \text{ appreciably with } \\ & \text{changes in } V_{in}. \text{ Therefore, a buffer } \\ & \text{amplifier for } V_{zero} \text{ is unnecessary.} \end{split}$$

SOFTWARE OPERATION

Polling-method software requires comparator transitions to be monitored by polling the microcontroller input G0 within a consistent tight loop. Keeping the loop down to the fewest cycles possible (four cycles) keeps the delta time to a minimum when the microcontroller exits the loop. This translates to minimum jitter or error when measuring $V_{\rm in}$.

The maximum jitter is the loop cycles divided by the total counts. Potential error can be greatly reduced by either averaging a few measurements or overcounting—that is, counting to 14 bits for 12-bit accura-

D E S I G N CIRCLE 122 FOR U.S. RESPONSE \rightarrow CIRCLE 123 FOR RESPONSE OUTSIDE THE U.S. \rightarrow

DESIGN APPLICATIONS DESIGNING SINGLE-SLOPE ADCs

cy (see the table).

Code for the polling method begins by initializing the I/0 to control the integrator and multiplexer (Fig. 2). The B register is then loaded with the address to read the G input register, which provides a single-cycle instruction to poll GO (IFBIT 0, [B]). The 16-bit timer is set to run in autoreload mode and will count down from the initialized value of FFFF (hexadecimal). The next step is to select V_{zero} by selecting channel 7 on the multiplexer and then drive the ramp down by setting L0 high with the LD LDATA, #0 1D instruction. Once the ramp is below V_{zero}, the ramp is driven positive by RBIT 0, LDATA, which drives L0 low.

ACCURACY CONSIDERATIONS

The accuracy of the polling method is largely determined by keeping the polling loop as short as possible. During the V_{in} measurement, the tight loop consists of the IFBIT 0, [B] and JP LOOP instructions. There's a maximum of four cycles from the time G0 goes high and the loop is exited. This same number of cycles are used when starting and stopping the timer and will tend to cancel out.

The same principle applies if an interrupt is used instead of polling the G0 input. An interrupt will take a fixed amount of cycles (seven) to push the program counter onto the stack and increment the stack pointer by two. The amount of additional cycles depends on which instruction was in progress at the time (between one and four cycles). A two-cycle instruction can be assumed. This time, plus the cycles required by an interrupt routine to stop the timer, is addtional delay that's required before starting the timer. Therefore, the only potential jitter error would be the two cycles of uncertainty.

The loop is exited once the comparator threshold is exceeded. Then V_{REF} is selected and the timer is started by an instruction sequence that takes a total of eight cycles:

3	cycles	LDLDATA, #018	;SELECT VREF
1	cycle	NOP	;DELAY
4	cycles	SBIT 4, CNTRL	;START TIMER

The NOP instruction is inserted in the previous sequence so that it has the same number of cycles as the sequence for exiting the loop and stopping the timer once the ramp equals V_{REF}:

4 cycles SBIT 0, LDAT ; START NEGA-TIVE RAMP

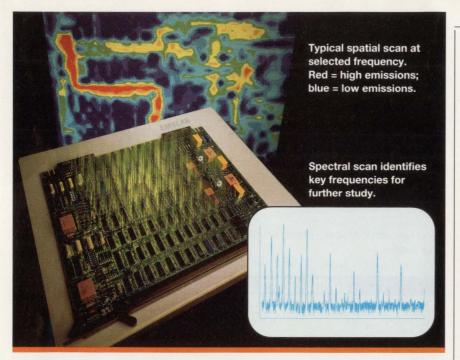
4 cycles RBIT 4, CNTRL ; STOP TIMER

The potential error caused by the delay while selecting V_X and starting and stopping the timer is eliminated if the total number of cycles is kept the same. This will provide eight cycles of delay to start and stop the timer and therefore cancel. After V_{REF} is measured, the 16-bit value in the timer is inverted (since it counts down) by exclusive ORing it with the

		CINCIE	
			-SLOPE A/D POLLING ROUTINE
			A/D POLLING ROUTINE FOR THE BASIC COP800 ERS THAT COUNTS TO 14 BITS FOR 12 BITS OF
	; ACCURACY		RED IN RAM 00,01 AND VIN IS STORED IN RAM
	;02,03.		
	CHIP 820		
	TLOW=0EA THIGH=0EB		
	LCONF=0D1		
	LDATA=0D0 GCONF=0D5		
	GDATA=0D4 GIN=0D6		
	CNTRL=0EE		
	; INITIALI2	ZE REGISTERS AN LD LDATA,#01	
		LD LCONF, #0FF	;SET LPORT = OUTPUTS
		LD B,#0D6 LD GDATA,#01	SET B REG POINTING TO GIN REG SET GO = WEAK PULL UP
		LD GCONF, #030	;G4,5 = OUTPUTS; G0,1,2,3,6 = INPUTS
	RESET CAR	LD CNTRL,#08A P AND COUNT VRE	
		LD TLOW, #0FF LD THIGH, #0FF	
	and the second se	LD LDATA, #01D	;SELECT Vzero ON CHANNEL 7
	WAIT:	SBIT 0,LDATA IFBIT 0,[B]	;START NEGATIVE RAMP, L0 = HIGH ;WAIT UNTIL COMPARATOR IS HIGH JP RAMP
	The Lake	JP WAIT	
	;CAP IS RE RAMP:	RBIT 0.LDATA	START POSITIVE RAMP
	LOOP :	IFBIT 0,[B] JP LOOP	CHECK FOR + Vzero CROSSING
	manulance	LD LDATA, #018	;SELECT Vref ON CHANNEL 6
		NOP SBIT 4, CNTRL	PROVIDE EQUAL DELAY START TIMER
	POLL :	IFBIT 0,[B]	;WAIT UNTIL RAMP IS > Vref
	- apinantan?	JP POLL SBIT 0,LDATA	START NEGATIVE RAMP
	at waa be	RBIT 4, CNTRL	STOP TIMER
		LD A, TLOW XOR A, #0FF	; INVERT A
	Contra and	X A,00 LD A,THIGH	;STORE Vref RESULT IN RAM 00 & 01
		XOR A, #0FF	; INVERT A
		X A,01	
	START VI	N MEASUREMENT	
	marks in the	LD TLOW, #0FF LD THIGH, #0FF	
	WAIT1:	LD LDATA, #01D IFBIT 0, [B]	;SELECT Vzero ON CHANNEL 7 ;WAIT UNTIL COMPARATOR IS HIGH JP RAMP1
		JP WAIT1	, WATE ONTITE CONFANATOR 13 HTGH 3F HAMFT
	;CAP IS RE RAMP1:		START POSITIVE RAMP
	LOOP1:	IFBIT 0,[B]	; CHECK FOR + Vzero CROSSING
	- Line area	JP LOOP1 LD LDATA,#04	SELECT VIN ON CHANNEL 1
	shi melar	NOP	; EQUALIZE TIME TO START TIMER
	POLL 1:	SBIT 4, CNTRL IFBIT 0, [B]	;START TIMER ;SIT AROUND AND DO NOTHING UNTIL
		JP POLL1 NOP	;RAMP IS > THAN Vref ;EQUALIZE TIME TO STOP TIMER
		NOP	, EGORETZE TIME TO OTOF TIMEN
		NOP	
		RBIT 4, CNTRL	STOP TIMER
		LD A, TLOW XOR A, #0FF	; INVERT A
		X A,02	STORE Vin LOW RESULT IN RAM 02 LD
		A,THIGH XOR A,#0FF	; INVERT A
	. END	X A,03	;STORE Vin HIGH IN RAM 03
1	, LIND		

← CIRCLE 122 FOR U.S. RESPONSE E C T R O N I C D E S I G N 65 U.S. JANUARY 23, 1992 E L

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FF XOR A, #OFF instruction. Finally, the result is stored in the first two bytes of RAM (00/01) using the x A,00/01 command.

The code for measuring V_{in} is nearly identical to that for V_{REF} with the following minor exceptions: V_{in} is selected instead of selecting V_{REF} , the result is stored in RAM locations 02/03, and the ramp is continued in the positive direction. Instead of using the SBIT 0,LDATA instruction, four NOPs are substituted to provide an equal number of cycles.

The reason for not driving the ramp negative is to avoid over driving the integrator toward its minimum output voltage. This situation could occur if additional microcontroller code takes longer to execute than the time for the integrator to ramp down.

A benefit is realized when using the input-capture method to measure the ramp time to equal V_{in} —the conversion is completed with minimal jitter, which is limited to the level of circuit noise. Conversions will also be quicker for a given resolution since overcounting or averaging isn't needed.

The logic used for the input-capture method is very similar to the polling method (*Fig. 3*). However, because it's unnecessary to poll the input G0 after V_{in} is switched in, other software functions can be performed while the conversion is in progress.

When the ramp reaches V_{in} at the comparator, the captured value in the timer will be automatically saved. This value can be read after the comparator transition either by generating an interrupt upon capture or by simply polling the status register when convenient.

Kevin Daugherty, a staff field application engineer at National Semiconductor Corp., holds a BSEE from Wayne State Univ., Detroit, Mich.

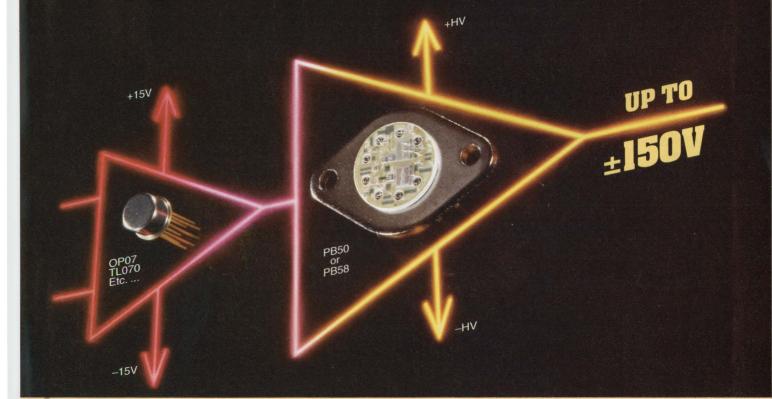
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T1-1T	5950-01-153-0668	TMO3-1T	5950-0
T2-1	5950-01-106-1218	TMO4-1	5950-0
T3-1T	5950-01-153-0298	TMO4-2	5950-0
T4-1	5950-01-024-7626	TMO4-6	5950-0
T9-1	5950-01-105-8153	TMO5-1T	5950-0
T16-1	5950-01-094-7439	TMO9-1	5950-0

5950-01-178-2612

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6	5950-01-215-4038
6T	5950-01-215-8697
Т	5950-01-168-7512
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any adjustable dc current sources typically exhibit nonlinear control characteristics—most often an inverse relationship between pot rotation and current. That nonlinearity, which is most pronounced at high current levels, means that the control tends to be hypersensitive at one end of its adjustment range and unresponsive at the other. By employing bootstrap feedback (see the figure), it's possible to provide an inherently linear control that works equally well at all current levels.

Reduced to its essentials, the circuit consists of a voltage reference (IC_1) , which drives a load (Z_L) through a sensing resistor (R_S) . Amplifier feedback controls the voltage across R_S to set the current.

Unlike conventional implementations that adjust the current by varying R_s , the bootstrap circuit varies the voltage directly by controlling the bootstrap gain. That produces direct, rather than inverse, proportionality between the control setting and the output current.

Potentiometer R_V varies the bootstrap gain to control the fraction of reference voltage V_R that appears across R_S . Op-amp feedback forces that voltage, V_S , to equal the voltage | across the xR_v portion of R_v.

Because the voltage reference is in parallel with the control pot, the volt-

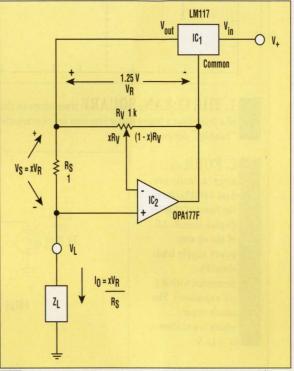
paranel with the control pot, the age across R_V is constrained to be V_R , and the voltage fraction across xR_V is simply xV_R . The voltage across the sensing resistor is the same. Hence, the output current is given by: $I_0 = xV_R/R_S$. For the components shown in the diagram, I_0 can be varied from 0 to 1.25 A.

In addition to linearizing the current control, this approach keeps the control potentiometer out of the main current path. Because the pot needn't carry the full output current, it can have a high value, making its end resistance negligible. That eliminates an extra source of nonlinearity.

With nonlinearity removed, component errors set the limits on circuit performance. The LM117 regulator drifts 0.01% per °C and R_s may drift 0.015% per °C. Thus, even assuming that all errors have been trimmed out at nominal temperature, a ± 5 -°C environment limits trim accuracy to around 0.125%. Error also results from a circuit output resistance of:

$R_0 = R_S/(xL_R + 1/PSRR)$

where L_R is the line regulation of the regulator and PSRR is the powersupply rejection ratio of the amplifier. For the components shown, and x = 1, $R_0 = 8 k\Omega$. A 10-V change in load voltage produces a 0.1% change in output current.



LINEAR CURRENT CONTROL results from bootstrap feedback, which redefines the control characteristic. This circuit has a current range of 0 to 1.25 A, an output resistance of $8 \text{ k}\Omega$, and a maximum drift of 0.025% per °C.

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n inexpensive yet effective way to evaluate semiconductor component quality is to display the device's I-V characteristics on an oscilloscope. Sharp, clear transitions indicate "healthy" junctions (Fig. 1). Soft, gradual ones imply leakage or possibly even shorts.

All that's needed to set up an appropriate I-V display are a pair of dual op amps and a handful of passive components (Fig. 2). Op $amp A_{1A}$ generates a 300-Hz sine wave with a peak-to-peak amplitude of 20 V. That sinusoid is buffered by op $amp A_{1B}$ to drive the device under test (DUT).

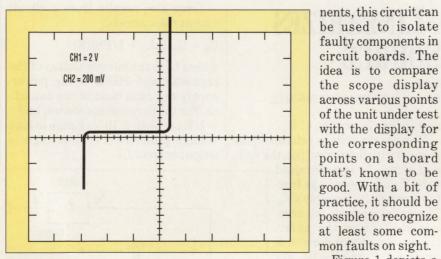
Op amp A_{2A} provides a return path for the current from the DUT and converts that current into a voltage. Finally, op amp A_{2B} inverts the voltage before feeding it to the scope for a correct I-V display.

The scope must, of course, be in its X-Y mode. A good initial gain setting is about 2 V/division.

In addition to individual compo-

E L E C T R O N I C D E S I G N 69 JANUARY 23, 1992

IDEAS FOR DESIGN



1. THE CLEAN, SQUARE transitions on this display of a transistor's base-emitter junction are characteristic of a "healthy" device.

2. FOUR op

amps (actually two dual AD647s) form the heart of this I-V display circuit. All of the op amp power supply leads should be decoupled with 0.1- μ F capacitors. The power supply, which is not shown, is ± 15 V.

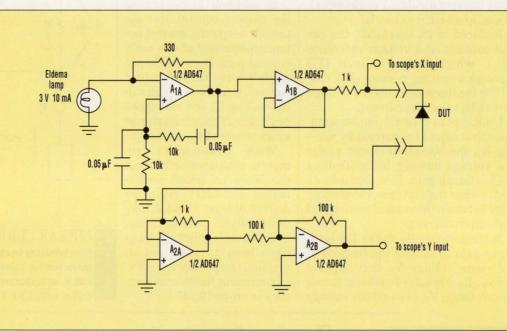


Figure 1 depicts a

junction

transistor's base-

characteristics. \Box

emitter

523 CIRCUIT AUTOSELECTS CLOCK SOURCE

MICHAEL A. WYATT

Honeywell Inc., 13350 US Highway 19N, M.S. 931-4, Clearwater, FL 34624; (813) 539-5653.

his simple circuit automatically chooses between internal and external clock sources with no need for a selector switch or any other input

(see the figure). If an external clock signal is present, the circuit chooses it. If not, it selects the internal clock source.

The circuit has proven valuable in

DESIGN

70 E L E C T R O N I C JANUARY 23, 1992 Send in Your Ideas for Design

Address your Ideas-for-Design submissions to Richard Nass, Ideas-for-Design Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604.

VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a \$150 Best-of-Issue award and becomes eligible for a \$1,500 Idea-of-the-Year award.

laboratory test equipment, where it provides a simple and economical way to set up clock inputs. It should also find use in complex gear, where an automatic clock-selection feature has the potential to eliminate human error.

The circuit's operation is as follows: When no external clock signal is present, R_1 pulls one of the gate's inputs low, and fixes the output of U_{1A} at V_{CC} . That fixed dc level charges the capacitor through resis-

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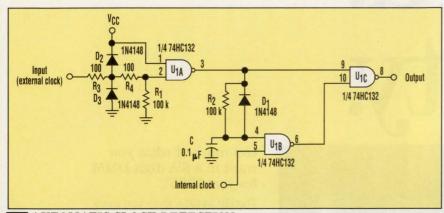
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IDEAS FOR DESIGN



AUTOMATIC CLOCK DETECTION is provided by U_{1A} in combination with R_1 . Resistors R_3 and R_4 and diodes D_2 and D_3 protect the input of U_{1A} .

tor R_2 , enabling the internal clock signal to pass through U_{1B} , and then U_{1C} , to the output.

Upon application of a clock signal from an external source, the output of gate U_{1A} toggles at the external clock frequency and discharges the capacitor through diode D_1 to a logic Zero.

With one of its inputs driven low, the output of U_{1B} goes high, blocking the internal clock signal and enabling U_{1C} to pass the external clock signal to the output.

For proper operation, the R_2C time constant should be made 10 times longer than the longest expected clock period.

IFD WINNER

IFD Winner for September 12, 1991

Yishay Netzev, Yuvalim 112, Israel 20142; (972) 480-1017. His idea: "Voltage Reference Has Dual Polarity."

IFD Winner for September 26, 1991

James Wong, Analog Devices Inc., 1500 Space Park Dr., Santa Clara, CA 95052; (408) 727-9222. His idea: "Low-Cost ISO Amp Has High Precision."



CIRCLE 104 FOR U.S. RESPONSE CIRCLE 105 FOR RESPONSE OUTSIDE THE U.S. 72 E L E C T R O N I C D E S I G N JANUARY 23, 1992

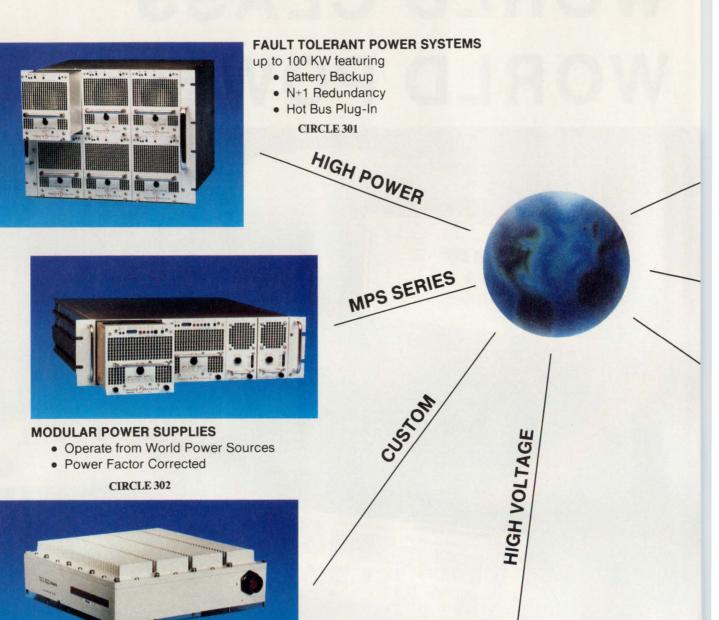
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DESIGN OUTOEK LOOK EDITED BY SHERRIE VAN TYLE

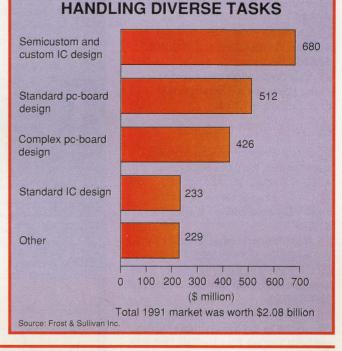
MARKET FACTS

esigners and companies are racing to put ever more complex ICs on the market. Tight schedules and competitive pressure are fueling growth in the market for computer hardware and software that supports electronic design. In response to designers' needs, suppliers are coming up with front-end tools that accept and simulate circuit descriptions simultaneously in terms of behavior, structure, and gate-level design. Designers are turning to new implementations of hardware-description languages (HDL) to represent designs. Debugging will become more efficient with concurrent multilevel simulators. Translating high-level de-

thesis tools. Total sales in the electronic design automation (EDA) market should surge from \$2.08 billion last year to \$4.92 billion in 1995, according to New York market researchers Frost & Sullivan Inc. EDA hardware, worth \$518 million in sales last year, should be worth \$1.24 billion by 1995. Software for electronic design should more than double in sales, from \$1.56 billion last year, to \$3.69 billion in 1995.

scriptions to gate-level implementations calls for powerful logic syn-

In other developments, designers will have at hand better layout tools to handle developing complex mixed-block and standard-cell designs. Also, look for tools for board layout that cope with multichip modules and pc boards crammed with application-specific ICs (ASICs) and surface-mounted devices.



SYSTEMS FOR ELECTRONIC DESIGN:

QUICK NEWS: EDUCATION

exas Instruments is giving one-day seminars on control using its family of digital signal processors. The seminars focus on using digital technology for control and how to implement control applications like hard disk drives, robotics, and motor control with TI TMS20 DSPs. Seminars will be held in various U. S. cities from Jan. 27 through Feb. 7. Registration fee is \$50, which includes lunch, seminar workbook, and TI's application book, *Digital Control Applications with the TMS320 Family*. Contact TI, Semiconductor Group, SC-91082, P. O. Box 809066, Dallas, TX 75380-9066; (800) 336-5236, ext. 700 or (214) 995-6611, ext. 700. CIRCLE 451

series of short courses takes aim at managers in technical environments. Course offerings include project management, finance for non-financial managers, and influence skills—getting results without direct authority. Course sites range from Washington DC to Los Angeles through June, 1991. Further information is available by calling Learning Group International at (800) 421-8166, or (703) 709-9019 East Coast or (310) 417-8888 West Coast. CIRCLE 452

HOT PC PRODUCTS

BC Flowcharter from Roykore is a what-you-see-is-whatyou-get (WSIWYG) drawing package to create, edit, and print flowcharts. The program does multidimensional charts—pointing to a shape in one chart causes a linked chart to be displayed automatically. Shapes can be numbered for cross-referencing and error checking. The program, which runs on PC ATs, PS/2s, and compatibles, supports Windows 3.0 and works on Windows networks. Registered users receive free updates and unlimited free technical support for up to one year after purchase. Flowcharter lists for \$295.

Also from Roykore, Instant ORGcharting works with Windows 3.0 to make organizational charts with a few clicks of the mouse. Pieces of charts can be cut and pasted into another through the Windows Clipboard. When boxes are resized or moved, lines are rerouted automatically. The program also can be used for personnel management employee pictures can be linked to boxes and reports created from the information. The charting software, which runs on PC ATs, PS/2s, and compatibles, sells for \$195.

For further information, contact Rykore, 2215 Filbert St., San Francisco, CA 94123; (415) 563-0836. CIRCLE 453

QUICKLOOK

BEST SELLER

Which technical books are the most popular in Silicon Valley?

ELECTRONICS:

1. Art of Electronics, 2nd ed., by Paul Horowitz and Winfield Hill. Cambridge University Press, 1989. **\$54.50**.

 C Language Algorithms for Digital Signal Processing by Paul Embree and Bruce Kimble. Prentice-Hall, 1990. \$55.
 Noise Reduction Techniques in Electronics by Henry Ott. Wiley, 1988. \$47.95.

4. Switching Power Supply Design by Abraham Pressman. McGraw-Hill, 1991. \$49.95.

5. Spice for Circuits and Electronics Using PSpice by Mohammed Rashid. Prentice-Hall, 1990. \$55.

COMPUTER SCIENCE:

 C++ Programming Language, second edition, by Bjarne Stroustrup. Addison-Wesley, 1991. \$34.50.
 C++ Primer, second edition, by Stanley Lippman. Addison-Wesley, 1991. \$32.25.

 Motif Programming Manual, vol. 6, by Dan. Heller. O'Reilly, 1991. \$34.95.
 C Programming Language by Brian Kernigan and Dennie Ritchie. Prentice-Hall, 1989. \$33.50.

5. Unix System Administration Handbook by Evi Nemeth, Garth Snyder, and Scott Seebass. Prentice-Hall, 1990. \$38. This list is compiled for *Electronic Design* by Stacey's Bookstore, 219 University Ave., Palo Alto, CA 94301; (415) 326-0681; fax (415) 326-0693.

QUICK NEWS: CONFERENCES

he U.S. gallium arsenide Mantech Conference will take up manufacturing issues for GaAs and its application in high-speed digital and analog ICs. Emphasis will be placed on processing, design for manufacturability, materials, and testing. The technical program focuses on quality in manufacturing and includes papers from industry and government experts. An informal workshop will be held on application of statistical process control/ design of experiments techniques as the basis for continuous measurable improvement. The conference will be held in San Antonio, Texas April 21-23. Further information is available by calling (215) 758-4061 or (508) 453-3100.

ID YOU KNOW?

... that one of five buyers of used computers is female and on average younger than her male counterparts. Of the female buyers polled, 60% were 29 or younger, whereas 86% of the male buyers were 30 or older. Professionals buy 28% of used PCs; self-employed professionals and entrepreneurs, 32%; managers, 17%; students, 15%; and nonmanagers, 8%.

Nacomex Insider, newsletter published by National Computer Exchange, New York, N.Y.

....Perspectives on Time-to-Market

BY RON KMETOVICZ

President, Time to Market Associates Inc. Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085

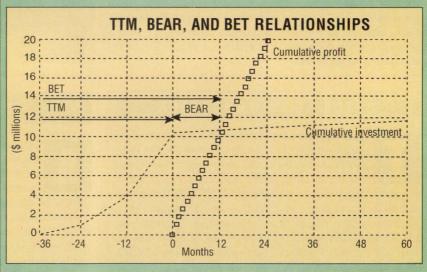


'd co fo

'd like to discuss the link between nomenclature and timing concepts (developed in previous columns) and financial performance of a project.

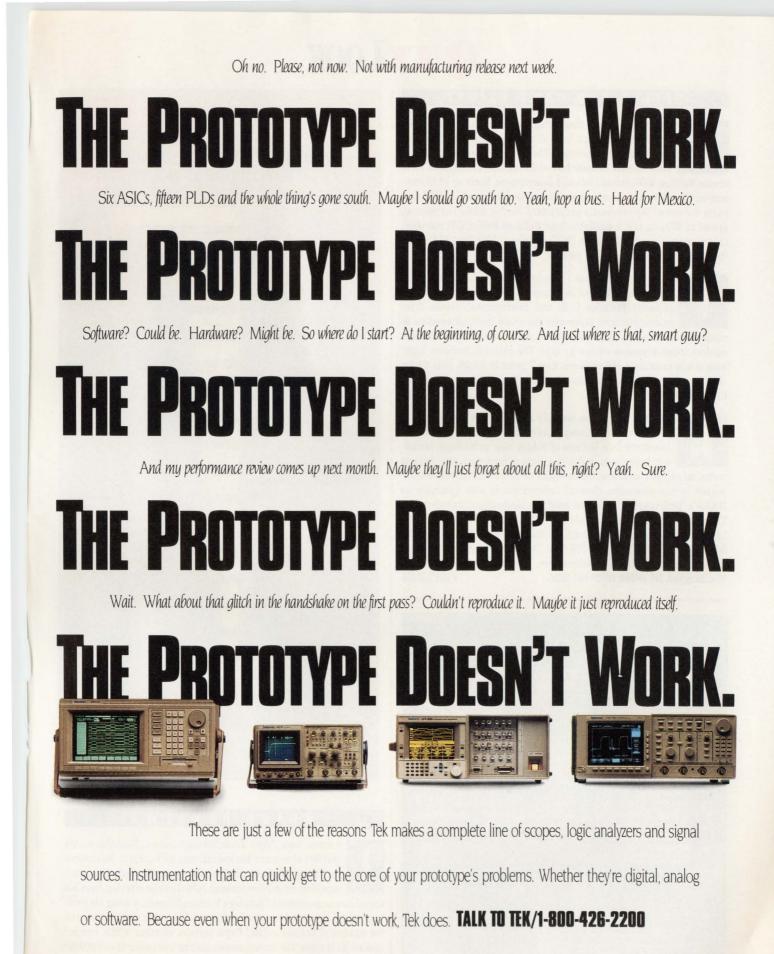
The horizontal axis (see the figure) begins at month -36, when the one-page document of the product idea appears. This point begins the measurement of time to market (TTM) and break-even time (BET). The axis continues to month 60. Between the -36 to +60 time interval, the product-development effort completes the promotion, definition, plan, execution, and revenue phases.

The vertical axis is calibrated in millions of dollars. Cumulative investment and profit dollars are plotted on the same scale. Investment expenses start at month -36 and accumulate up to month 0, displaying three changes in slope. At month 0, the slope of the investment curve is significantly reduced. As illustrated, profit dollars begin to flow in during this month. As a result, month 0 is where emphasis shifts from investment to profit generation.



The start of TTM and BET have been established. TTM ends when product is delivered to customer in exchange for monetary compensation. BET ends when the compensation, expressed as profit, equals the cumulative investment in the product's development. BET is always greater than TTM. Break-even after release (BEAR) measures the time from when profit dollars are generated to when cumulative profits equal cumulative expenses on the project. As such, TTM + BEAR = BET.

Under most business conditions, it is optimal to minimize **TTM** and **BEAR**. Doing so naturally results in minimizing BET. Knowing BET without knowing its constituents supplies limited information about the complexities of the development and revenue-generating processes.





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CIRCLE 178 FOR U.S. RESPONSE

CIRCLE 179 FOR RESPONSE OUTSIDE THE U.S.

QUICKLOOK

OFFERS YOU CAN'T REFUSE

reference manual describing the Verilog Hardware Description Language is available from the Open Verilog International committee. The 300-page Language Reference Manual Release 1.0 has all the information needed to create Verilog HDL-based tools and descriptions. Made up of 18 companies, 17 non-voting members, and six university members, OVI supports the use of the previously proprietary Verilog HDL. The manual, priced at \$50 plus tax, is available from Deborah Kelley, OVI membership manager at (408) 776-1684. OVI's address is 1016 East El Camino Real, Suite 408, Sunnyvale, CA 94087. CIRCLE 453



he Computer Events Calendar lists 200 high-technology trade shows, analyst conferences, and special events. The calendar includes U. S. and international events from semiconductors, supercomputers, and bank automation to

consumer electronics. An index gives contact information for shows. A subject index arranges events by type. The calendar includes hightech trivia questions and answers. Retail price is \$29.95, plus \$4 for shipping. Contact Tech Trade Events, 5637 Ocean View Dr., Oakland, CA 94618; (510) 428-2439. CIRCLE 454

subscription to the monthly NASA Tech Briefs magazine is free to engineers who qualify for it. The publication has up-to-date listings of NASA new technology, including inventions and ideas. Subscribers may also request technical support packages, which supply details about innovations reported in the magazine. General information is also available on NASA's Technology Utilization program (technology transfer). For Tech Briefs information, contact the NASA Scientific and Technical Information Facility, Technology Utilization Office, P. O. Box 8757, SWI Airport, MD 21240; (309) 859-5300. For information on technology transfer, contact NASA Headquarters, Leonard A. Ault, Code IU, Washington, DC 20546; (202) 453-2636. CIRCLE 455

ELECTRICAL ENGINEERING CITATION IMPACT

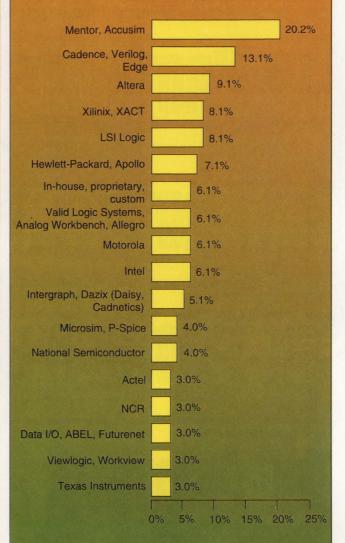
No.	University	Papers 1986-90	Citations 1986-91	Citations per paper
1 2	Stanford University University of Rochester	243 51	1,283 269	5.28 5.27
	University of Illinois, Urbana	211	1,100	5.21
	Columbia University	74	343	4.64
5	Caltech	69	294	4.26
6	University of Southampton (UK)	150	631	4.21
	Purdue University	95	366	3.85
8	Cornell University	97	351	3.62
9	University of Tokyo (Japan)	82	293	3.57
10	University of So. California	58	195	3.36

A survey from JPT Publishing Group's Institute for Scientific Information shows a U.S. advantage over Japan in basic electrical engineering research. The statistics show that research papers published by scientists at American universities and companies have been the most-often cited by other researchers. The data was compiled from 38,535 articles, reviews, and technical notes published in 70 EE journals from 1986 to 1990. A list of the top 10 shows a British university ranked sixth for the number of citations and a Japanese university in ninth place.

Source: Institute for Scientific Information's Science Watch, JPT Publishing Group

CAD/CAE SURVEY

WHICH IC DESIGN PRODUCTS ARE YOU USING NOW?



Source: a survey of Electronic Design readers by the Adams Co., Palo Alto, Calif.; (415) 325-9822.

Readers wrote in responses and gave more than one answe

QUICK REVIEWS

n a new book, *High Tech Startup*, John L. Nesheim writes that 60% of venture-backed startups go bankrupt. To reverse that trend, Nesheim analyzes 25 successful high-tech startups from conception through initial public offering from his experience as president of Satatoga Venture Finance. Among his findings: mixed sources of venture funding are becoming more common as the number of venture capital firms shrinks; startups within companies are on the rise. The book draws on six years of research and 300 interviews with 180 people in 120 U. S. companies. It lists for \$49.50 from

Electronic Trend Publications, 12930 Saratoga, Suite D1, Saratoga, CA

95070; (800) 726-6858; (408) 996-7416.

PEASE PORRIDGE

WHAT'S ALL THIS CUSTOMER SATISFACTION STUFF, ANYHOW?

et's start off with another esaeP's fable. Once upon a time, there was a King who told his Courtiers, "Send up the Royal Wizard." The Wizard promptly came running up, asking, "Sire, what is your desire?" The King said, "Make me invisible." So the Wizard went down to his cavern, got his book of potions, brought up an Eve of Newt, a Wing of Bat, and all of the other good things he needed, and went to see the King. He sprinkled the right potion and incanted the correct phrase and, presto, the King was INVISI-BLE. The King's robes and crown kept



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCT-OR CORP., SANTA CLARA, CALIF. moving around the throne room, but the King himself was invisible. The whole court was impressed. Good stuff! Good magic!

The next morning, the King awoke early and roared, "Get that lousy wizard up here." The Wizard came running up, in fear for hislife, as soon as he got the word. "Sire, what is the problem?" The King replied, "Dammit, I asked you to make me invisible, but I'm still bumping into things." End of fable.

Think about it. The Wizard did what he was asked to do, yet he didn't get a satisfied customer. The King specified what he wanted, yet when he got what he asked for, he was unhappy.

Does this ever happen with your cus-

tomers? How can we avoid this in the future? It sure takes much better communication than the King had with his Wizard. Perhaps the Wizard should ask what the King was trying to accomplish. What did he really want?

Here's something to think about: Do you ever ask your customers what they really want? And are you then prepared to give them what they really want, rather than what they said they wanted?

For example, once an engineer at company A went out for a bid on a signal conditioner circuit, and he defined the function he wanted. "This function must consist of an input filter followed by an amplifier/comparator. When you put in 200 mV pk-pk at 100 kHz, the output must give a TTL signal at 100 kHz. When you put in a 4-V pk-pk signal at 5 MHz, the output must not respond." His intention was to specify a steep roll-off of the frequency response, but he never really said that. He just specified a couple of tests that a good part ought to pass.

The Marketing Engineer at Company Blooked at this specification and figured out, "If I put a 200-mV clipper or limiter on the input stage, I can meet that spec with a simple 2-pole roll-off." Sure enough, this approach gave a very simple and low-cost circuit. Company B won the bidding with a low price that many would consider a lowball bid. They began production and had no problem meeting the incoming inspection tests. But when these signal conditioners were put into service, some worked well. Others, though, worked very badly if they happened to be in a noisy environment (which was the whole reason behind having a filter anyhow).

After some side-by-side compar-

isons, the circuit with the limiter was found to perform quite differently from the intention of Company A. The filter circuit passed the specified tests and fulfilled the spec. But it failed to meet the intention of Company A, because they never spelled out what they really wanted. They really wanted to be able to put in BOTH the 5-MHz noise and the 100-kHz signal and get a 100-kHz TTL output, while rejecting the 5-MHz noises. The circuit from Company B passed all of the specified tests, but it did not meet this unwritten spec. So, most users found that circuit unusable, and the business fell apart, even though the units met every spec. But, YOU would never get caught making that kind of mistake. Would you?

All for now. / Comments invited! RAP / Robert A. Pease / Engineer

Address: Mail Stop C2500A National Semiconductor P.O. Box 58090 Santa Clara, CA 95052-8090

BOB'S MAILBOX

Dear Bob,

Your reasoning on the Little Egbert problem in the Sept. 12, 1991 issue is wrong. Consider a horn whose radius is $1/x^2$ instead of 1/x. Both its area and volume are finite. Yet by your reasoning, an infinite amount of paint would be required to paint the outside, since the surface is still infinitely long. On the other hand consider a horn whose radius is $1/x^{1/2}$. Both its area and volume are infinite. Yet again by your reasoning, only a finite amount of paint is required to paint the inside, since there will be some point at which a single molecule will no longer fit. Thus the math tells us nothing about the real-life situation because it is improperly applied.

NORMAN D. MEGILL Lexington, Mass.

I appreciate your restraint in puncturing my <u>ad hominem</u> arguments. You're correct and I apologize.-RAP

E L E C T R O N I C D E S I G N 81 JANUARY 23, 1992

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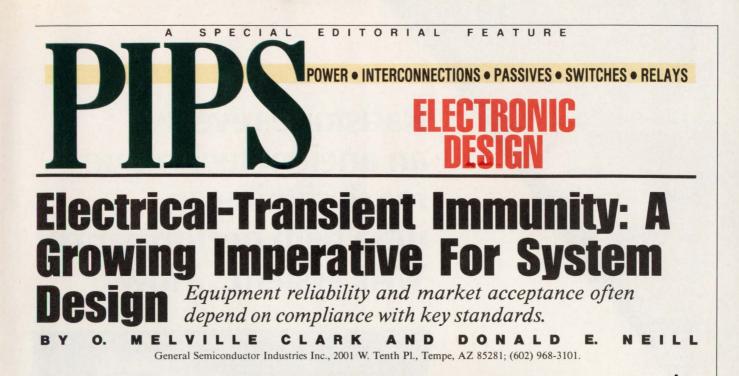
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CIRCLE 134 FOR U.S. RESPONSE

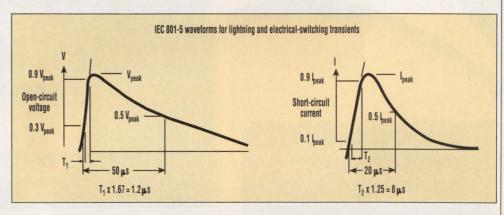
CIRCLE 135 FOR RESPONSE OUTSIDE THE U.S.



Inderstanding transientvoltage threats and immunizing electronic equipment and systems against them is becoming essential for a growing segment of the electronic-engineering community. In particular, designers of equipment incorporating the latest in IC technology and requiring reliability and/or global marketing acceptance must heed the call.

Gains in IC technology dramatically boost performance, cut equipment costs and, in most cases, improve reliability. But the corresponding shrinking of circuit geometries and trend toward CMOS make ICs more vulnerable to voltage-transient events. To address this situation, the IEC 801 international transient-immunity standards have evolved. Several key documents are either completed or close to it. These documents will likely form the basis for future mandatory transient-immunity requirements within the European Community (EC). They'll also serve as a criteria for the purchase of electronic equipment among many companies, regardless of their location.

In May 1989, the European Community issued a Council Directive (No. 89/336/EEC) requiring that electronic and electrical apparatus have "an adequate level of intrinsic im-



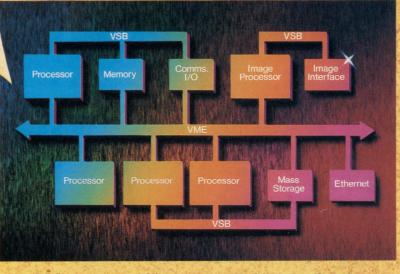
1. As defined by IEC 801-5, the short-circuit current waveform is for power-line applications. The current waveform for signalline applications approaches that of the voltage waveform.

munity" to "electromagnetic disturbance to...operate as intended." Originally, compliance was required by January 1992; but this date was recently amended to January 1996. The European Committee for Electrotechnical Standardization (CENELEC), with representation from the 12 EC-member states and the six European Free Trade Association Countries, was designated to develop the associated standards "to facilitate proof of conformity." Typically, CENELEC adopts IEC standards with little or no change. That's why the IEC 801 series takes on paramount importance for those companies expecting to sell electronic products into the EC market after 1995, and even before.

There are several compelling reasons for designers to strive ELECTRONIC DESIGN = PIPS SPECIAL EDITORIAL FEATURE = JANUARY 23, 1992 for their projects to comply with the applicable IEC 801 standards. For one, as CENELEC adopts these standards through issuance of European Norms (EN) numbers, equipment conformance, along with the acquisition of a CE identification (the EC conformity mark), will meet the requirements of all ECmember states.¹ Furthermore, products sold into the EC that already meet the subject standards will have a competitive edge, all else being equal.

Another reason is that standards agencies outside the EC, such as ANSI and IEEE, are also beginning to adopt IEC standards. This is likely to heighten awareness of the immunity standards and induce purchasers of electronic equipment to either require or prefer products that meet the applicaRadstone reveals an ancient technique for designing an ultra high performance VME system...now.

Lurking right there in the VMEbus designer's bag of powerful tricks is the overlooked, under-utilized and very potent VSB with all of its board and system enhancing features. There's even a complete range of VME/VSB boards just waiting to be designed into a superfast, super-flexible system...right now.



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ble IEC 801 standards. And aside from the standards' legalistic demands, conforming equipment will offer superior reliability with protection from what's reportedly the most common cause of failures.

This article discusses three standards within the IEC 801 series and associated design guidelines that lead not only to compliance, but protection against a real-world transient environment. All important transient events are addressed except for very unique situations, like those found in aircraft. In most instances, such applications already have their own standards.

Three standards are discussed: IEC 801-2 addresses electrostatic discharge (ESD), IEC 801-4 is aimed at electrical fast transients (EFTs), and IEC 801-5 governs electrical surges. Each standard defines the transient sources and applicable equipment-entry paths; transient-severity levels by installation or environmental classes; and details regarding immunity testing including test instrumentation, setup, and procedures. Also included are definitions of performance criteria. This article's goal is to equip the designer with methods of protecting electronic equipment that's exposed

to the defined threats. Therefore, only those aspects of the standards necessary to this end are discussed in detail.

The most severe of all transient conditions, in terms of peak current and duration, are those described in IEC 801-5, which specifies surge immunity for both power and signal lines. As indicated within the standard, the defined origin of electrical surges falls into two major categories, switching and lightning. The first category comprises switching disturbances, electrical system faults, and resonating circuits associated with switching devices.

Within the latter category are surges resulting from lightning directly striking outdoor power circuits, as well as electromagnetic energy generated by nearby strokes. More distant lightning may induce significant voltages only on long outside conductors, while nearby activity has been known to induce damaging voltages on conductors within structure interiors.

The power-service entry sustains the greatest impact, because the electrical mains receive residual current directly from lightning strikes on power lines. In addition to ac-line suppressors, insulation resistance, and power-supply filters can greatly increase equipment resistance to these surges. They can also increase resistance to the milder transients resulting from lightning-related electromagnetic coupling into the lines. However, in spite of these measures, equipment protection may be incomplete because of voltage differences developed through ground loops and resulting overstress to sensitive data-I/O ports.² Driver and receiver chips that interface with signal and communication lines are quite vulnerable to even lowlevel transient voltages with threshold failures ranging down to 40 V or less.

The IEC 801-5 standard recognizes the threat of direct coupling both switching and lightning-related transients into signal and data lines. This reinforces the importance of protecting across these lines as well as power-supply lines.

IEC 801-5 provides critical design information by quantifying what many engineers regard as the "elusive threat." For each of the entry points and a set of installation conditions, the transient is defined in terms of a generator producing a given waveform and having specified Thevenin-equivalent parameters (in other words, open-circuit voltage and source impedance).

A look at some waveforms also serves to define the waveforms' time-related parameters (*Fig. 1*). The voltage waveform is defined as $1.2/50 \ \mu$ s, having a $1.2-\mu$ s front time and a 50- μ s duration.

Looking specifically at power-line applications, the shortcircuit current waveform has a 8/20- μ s configuration. The specified Thevenin-equivalent source impedance is 2 Ω for the "line-to-line" application, and an additional 10 Ω is required for "line-to-ground" applications. The open-circuit voltage depends on the chosen equipment-installation class, which is discussed later on.

TABLE 1: IEC 801-5 THREAT LEVELS	
AS FUNCTION OF INSTALLATION CLASS	
Peak voltage with 1.2/50 μ s** waveform	1

All and a state of the		and the second			A the second	and the second sec
	Powe	Power supply		Unsym lines (long-distance bus)		Data bus (short distance)
Class	Coupl	ing mode	Coupling mode		Coupling mode	Coupling mode
	$\begin{array}{c} \text{Line-Line} \\ \textbf{Z}_{\text{s}} = \textbf{2}\Omega \end{array}$	$\begin{array}{c} \text{Line-GND} \\ \text{Z}_{\text{S}} = 12\Omega \end{array}$	Line-Line $Z_s = 42\Omega$	Line-GND $Z_s = 42\Omega^{***}$	$\begin{array}{c} \text{Line-GND} \\ \text{Z}_{\text{S}} \!=\! \! \textbf{42}\Omega \end{array}$	$\frac{\text{Line-GND}}{\text{Z}_{\text{S}}=42\Omega}$
0			NO RI	EQUIREMENTS		
1	-	0.5 kV	-	0.5 kV	1.0 kV	-
2	0.5 kV	1.0 kV	0.5 kV	1.0 kV	1.0 kV	0.5 kV
3	1.0 kV	2.0 kV	1.0 kV	2.0 kV	2.0 kV	
4	2.0 kV	4.0 kV	2.0 kV	4.0 kV	-	-
5	*	*	2.0 kV	4.0 kV	4.0 kV	

* Depends on class of local power-supply system.

** Short-circuit waveform—8/20 µs for Z_s = 2 Ω. Not applicable to telecommunication applications where open-circuit voltage waveform is 10/700 µs and short-circuit current waveform is 5/300 µs with Z_s = 40 Ω.

*** For telecommunication, R_s = N×25 Ω to each line with resistors terminated at surge generator with Z_s = 15 Ω. N = number of lines (this formula applies for N > 2).

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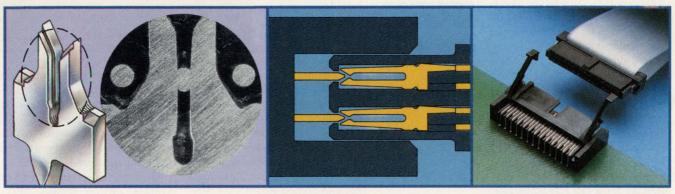
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In contrast to the 2- Ω impedance associated with power-line surges, the defined source impedance for data- and signal-line applications requires the addition of a 40- Ω resistive component. This results in a current waveform that approaches the 1.2/50- μ s waveform of the open-circuit voltage.

For the two-wire telecommunication interface, the specified open-circuit voltage has a 10/ 700- μ s waveform and the shortcircuit current is a 5/300- μ s waveform. The dynamic source impedance equals 40 Ω .

It's important to note that suppressors with the common 20-µs-duration current rating must be derated for longer durations. For example, a typical avalanche-junction, transientvoltage suppressor (AJTVS) with a stated current rating for a 8/20-µs waveform must be derated 50% for the 1.2/50-µs current waveform required for data-line applications. Most manufacturers of discrete suppression devices supply applicable derating data as a function of waveform duration.

Thevenin-equivalent, opencircuit voltages for both powersupply and signal- and data-line applications depend on installation conditions. These values, which define the required equipment- and system-immunity levels, are provided within the IEC 801-5 document by installation classes. These are listed in ascending order of threat level:

• Class 0: Well-protected environment

• Class 1: Partially-protected environment

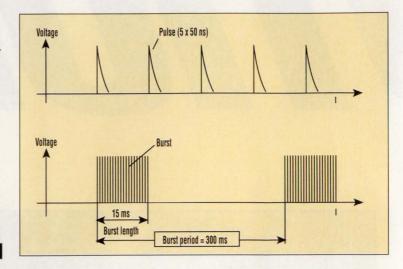
Class 2: Cables well-separated

Class 3: Cables run in parallel
Class 4: Multi-wire cables for

all circuitry

• Class 5: Connection to telecommunication cables and overhead power lines (low-density population)

The classes are self-descriptive. Class 0 represents a com2. IEC 801-4 specifies the model waveform for immunity testing against transients typically generated by arcing across switching contacts. Unlike the surge-voltage waveform in Fig. 1, the time segment before the crest is de-fined from 10 to 90% of peak value, while the time duration is the interval from 50% of peak before the crest to 50% of peak after the crest. The standard specifies repetitive bursts of at least 1 minute.



puter room that satisfies all of the inherent conditions for protection, including power conditioning, a common ground reference, short data lines, and well-separated power and data cables. At the opposite end of the spectrum, Class 5 exemplifies the highest threat level typical of the small, remote system connected to long "antennas" presented by telecommunication and overhead-power lines.

As defined in IEC 801-5, surge-severity levels (in terms of Thevenin-equivalent, open-circuit voltages) can be shown for both power and data lines by the aforementioned installation classes (*Table 1*). The required protection ranges from "none" to 4 kV for those sites with virtually no inherent hardening.

Short-circuit current, with its waveform description, is the key parameter in choosing a suppression device. Therefore, a second table shows how surge-current levels were calculated for each installation class by dividing the open-circuit voltages by the appropriate source impedances as given in the first table (*Table 2*).

The standard offers a practical means of characterizing the surge threat. The next engineering task is to design in the required immunity. The first and most vital step is to ensure that all insulations and electrical spacings exposed to the applicable maximum open-circuit voltage (up to 4 kV) can withstand voltages of equal or greater magnitude. Exposure from both line-to-line and line-to-ground surges must be considered. Components requiring the appropriate insulation stand-off voltage ratings include transformers, optocouplers, and capacitors.

Using ac-surge protectors, as discussed below, can drop the required insulation ratings to just above the suppressionclamping voltage levels. European applications, however, need more precautions. Qualification to existing TUV/VDE documents preclude the insertion of suppressor components from line to ground, but they can be installed from line to line. The only component allowed between line and ground is a socalled "Y" capacitor, which is basically ineffective as a surge protector. Hence, associated power-supply insulations and spacings to ground as well as **RF-bypass** capacitors require ratings up to 4 kV to prevent failure from neutral-to-ground and line-to-ground surges (known as common-mode surges).

For line-to-line surge suppression on incoming power, metal-oxide varistors (MOVs) are usually chosen because of their high surge-current ratings and low cost. A device with an operating voltage of at least 275

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V ac rms is recommended for 240-V ac service to accommodate high-line conditions. This also prevents the breakdown voltage from eroding to the maximum operating-voltage level after too many current pulses. A 20-mm-diameter MOV will withstand more than 50 pulses at 1 kA for a 8/20- μ s surge. This exceeds the Class 5 requirement of five positive and five negative 1-kA pulses at a rate of one per minute.

For optimum clamping-voltage performance, the device must be installed with minimal series-parasitic lead impedance. A 2.5-to-5-A fuse should be placed directly in series with the MOV to remove it from the circuit in the event of failure. An indicator light wired across the MOV helps detect failures.

Historically, protection across ac-power lines is better understood because of early awareness of the threat. Model waveforms were first published in the 1980 version of the IEEE 587 (now designated as ANSI/ IEEE C62.41) guide. Today, with the broader distribution and networking of systems and the greater susceptibility of data lines, a new dimension is brought to the transient-suppression discipline. That's why the IEC 801-5 standard's pioneer effort to address protection across data lines fulfills an important need. However, many informal requirements existed among major electronic-equipment suppliers as reliability insurance for their products.

As noted, the maximum specified current threat for data lines is 24 A for Class 2 (Table 2, again). This covers most office and residential locations, which are typically in semi-protected environments. For most applications, AJTVSs are best because of their superior clamping-voltage characteristics, which lend better protection to I/O-interface ICs. For this purpose, board-level suppressors are available, including both surface-mounted- and throughhole-discrete and multi-chip/ multi-pin offerings.

The designer must heed several factors in choosing and applying board-level protectors. After determining the peak-current requirement corresponding to the applicable installation class (such as 24 A for Class 2), the component must be able to handle this magnitude for a 1.2/50- μ s (not 8/20- μ s) current waveform. Furthermore, with most bipolar driver/receiver devices having reported failure thresholds in the 40-to-90-V range, a suppressor should be chosen with a clamping voltage no greater than 40 V at the maximum anticipated peak current.

Special care should be taken

AS FUNCTION OF INSTALLATION CLASS Calculated short-circuit peak current (8/20 μ s) for Z_s = 2 Ω and approximately 1.2/50 μ s for Z_s = 42 Ω^{**} **Unsym lines** Data bus **Power supply** (long-distance bus) Sym lines (short distance) Class **Coupling mode Coupling mode Coupling mode Coupling mode** Line-Line Line-GND Line-Line Line-GND Line-GND Line-GND $Z_{c} = 2\Omega$ $Z_e = 12\Omega$ $Z_{c} = 42\Omega$ $Z_{c} = 42\Omega$ $Z_c = 42\Omega$ $Z_s = 42\Omega$ 0 NO REQUIREMENTS 1 42 A 12 A 24 A 2 250 A 83 A 12 A 24 A 24 A 12 A 3 500 A 167 A 24 A 48 A 48 A _ 1 kA 333 A 48 A 95 A 4 * * 48 A 5 95 A 95 A

TABLE 2: IEC 801-5 THREAT LEVELS

* Depends on class of local power-supply system.

** Current levels for telecommunication applications not shown

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Future CMOS driver/receiver chips will be more sensitive to transients than today's bipolar de-

vices.

when choosing the AJTVS location and associated conductor layouts. The suppressor should be mounted on the pc board as close as possible to the signal-input connector. This reduces the effects of radiation energy coupling into sensitive areas of the circuitry. Because induced voltages (proportional to the product of parasitic inductance and the rate transient current rises) can add to the suppressorclamping voltage, leads and conductor lengths directly in series with the suppressor must be kept to a minimum.

Emerging generations of CMOS driver/receiver chips are expected to be far more sensitive to lightning-related currents than today's bipolar devices. As a result, failure-threshold voltages are expected to be lower, driving the need for increasingly effective suppression methods.

In the presence of long outdoor signal-line runs, it is necessary to protect I/O ports to higher current levels. This is achieved by placing "primary" protection at either the cable-entry location into the structure or near the protected equipment. Primary protectors typically consist of a combination of elements to handle large currents and, at the same time, provide low clamping levels. Combinations of gas-discharge tubes and AJTVSs are often used in these assemblies.

Because of the potentially high surge currents associated with primary protectors, lowimpedance ground paths are required. When placing such assemblies next to the protected equipment, the ground connection should be tied to the equipment-frame ground using the shortest and most direct route. Where possible, a common "ground window" should serve as a reference for all externalsystem protection involving both power and signal lines. This reduces ground-potential differences in the presence of the large current transient, and

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keeps clamping levels close to the true capability of the suppressor assembly.

Thanks to its potential to corrupt data and memories without equipment failure or apparent software errors, the EFT may properly be described as the "insidious disturbance." IEC 801-4 specifies applicable EFT-immunity testing involving both power and data lines. The defined threat consists of high-voltage spikes occurring at a repetition rate of either 2.5 kHz or 5 kHz (depending on the voltage level) within periodic 15-ms-wide bursts every 300 ms. This lasts over a specified time interval of not less than one minute (Fig. 2).

EFT disturbances will most likely occur in industrial environments, and can be attributed to arcing mechanical contacts on power mains. The rapid cycles of interruption and restoration of the current path interacts with distributed and lumped reactive components to produce the usual repetitive bursts.

3. IEC 801-2 specifies

an ESD generator that

allows testing using either the "air-dis-

charge" or "contact"

recommended contact

methods. Using the

method for conduc-

tive-surface applica-

tions, the storage capacitor (Cs) is

charged to the appro-

priate value, and with

the discharge switch open, a pointed tip is

brought into contact

with the target. The

switch is then closed.

Within the standard, severity levels are given in terms of opencircuit voltages as a function of four installation environments. In addition, the standard stipulates a nominal dynamic source impedance of 50 Ω for the EFT generator and specifies the voltage waveform shown across a 50- Ω terminating resistance (*Fig. 2, again*).

Because the clamping voltage and dynamic impedance of a given suppressor are expected to be far less than the EFT-generator's open-circuit voltage and source impedance, respectively, estimated peak currents through the suppressor will be double those values through a 50- Ω load. Therefore, if it's assumed that the suppressor presents a short circuit, the corresponding estimated values are calculated by dividing the EFT open-circuit voltage by its $50-\Omega$ source impedance (Table 3). Levels are shown for both incoming power and data lines.

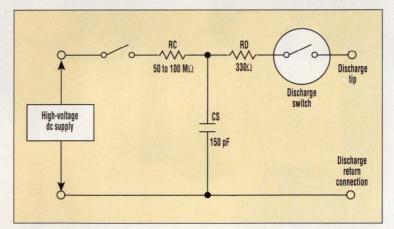
Attempts to mitigate the EFT

threat have been made using MOVs, AJTVSs, and off-theshelf EMI/RFI filters.⁴ All devices evaluated were found to clamp bursts of kilovolt spikes to levels low enough to be harmless to microchips within the hardware. The energy level for each pulse is relatively low and steady-state power dissipation for a 1-minute burst was reported at less than 1/2 W. This earlier work indicates that the EFT isn't a major threat on incoming power lines. But for data lines, problems may still loom.

A test-system clamp for EFT injection, as specified by IEC 801-4, capacitively couples the specified waveform to the data lines by introducing a series value within the range of 50 to 200 pF. This presents a relatively low impedance with little effect

ware that recognizes the disturbance and asks for retransmission. However, in extremely dirty electrical environments, the efficiency of high-performance computers may be compromised or the system rendered ineffective by such measures. In fact, some systems have been completely disabled by unexpected and extensive repetitions of EFT. Parity checks and error-correcting codes must supplement suppressor devices to achieve satisfactory protection. Most high-end systems now have these features.

For data lines, the threat levels for EFT pulses extend over a broad range of both voltage and current, from 250 V through 2 kV, with worst-case short-circuit currents estimated at 5 A through 40 A, respectively (*Ta*-

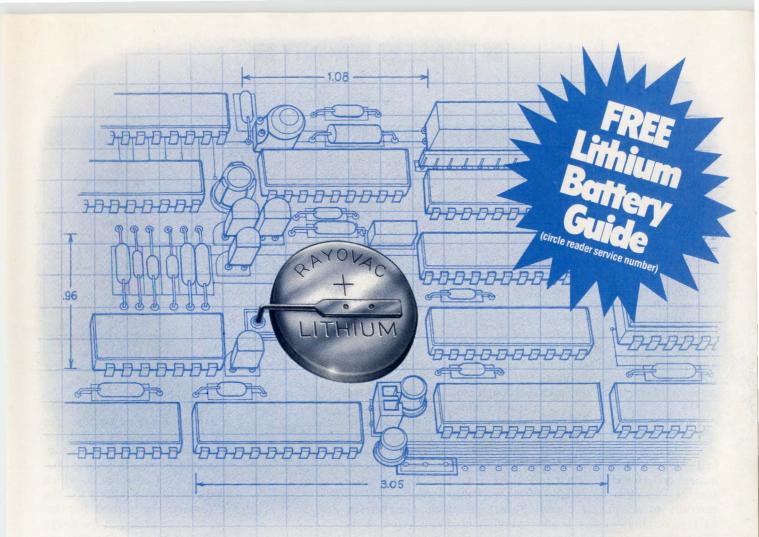


on the rise time. In the absence of intervening suppression, the stress levels associated with the parametric values specified across a 50- Ω load are retained. Consequently, a string of rapid, high-voltage pulse bursts appears across the system or equipment-interface microchips. As indicated earlier, AJTVS devices easily suppress this disturbance to a level that's harmless to data-I/O ports. But it also introduces noise that may be interpreted as part of the signal, corrupting the transmitted data.

When equipment must work within an environment experiencing an occasional EFT, it may be necessary to design soft-ELECTRONIC DESIGN = PIPS SPECIAL EDITORIAL FEATURE = JANUARY 23, 1992 ble 3, again). Because the pulses last only 50 ns, their maximum energy content is a relatively low 4-mJ/pulse. Any suppressor devices installed for protection from lightning surges as specified in IEC 801-5 are more than capable of withstanding and protecting against EFT-originated spikes. But installing them for the fast-rising transient voltages demands more care than for applications involving lightning's slower rise times.

Parasitic impedances associated with the length of pc-board traces between the source and the protector, and between the protector and I/O chip along with the terminating impedance

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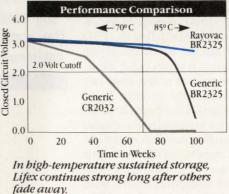


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presented by the interface chip, play a major role in determining the magnitude of the transient let-through voltage.5 The study cited generally concluded that parasitic impedance ahead of the suppressor was beneficial. It's desirable, however, to minimize the impedance between the suppressor and load. This study joins with earlier work to illustrate the adverse effects of excessive parasitic inductance in series with the suppressor, including that presented by suppressor-lead lengths⁶. For example, under nanosecond rise-time conditions, the induced voltage across a 12-cm trace can reach 1200 V.

Therefore, although EFTs as defined in IEC 801-4 can be severe in voltage magnitude, their low energy content allows easy mitigation. However, suppression devices must be installed carefully to adequately clamp EFTs to acceptable levels. In addition, the system must differentiate between induced noise and transmitted data.

The most prevalent of transients, electrostatic discharge (ESD), is addressed by IEC 801-2. The presence of ESD doesn't depend on connections to any outside power or data line, and it poses a universal threat to equipment without special protection. This applies even to the otherwise well-protected class-0 environment specified in IEC 801-5.

ESD results from environmental conditions in which a low relative humidity allows electrical charges to build up from contact and subsequent separation of dissimilar materials. The resulting potential of the human body can exceed 15 kV in arid or sub-freezing environments, especially when surrounding materials, floors, or furniture are nonconductive and synthetic.

The ESD-related standard defines immunity requirements against electrostatic-discharge energy, which couples into the equipment either directly or

TABLE 3: IEC 801-4 SEVERITY LEVELS (EFT THREAT)

		Peak amplitudes			
Level	On power supply		On I/O signal, data, and control lines		
	V _{oc} *	I _{sc} **	V _{oc} *	I _{sc} **	
1	0.5 kV	10 A	0.25 kV	5 A	
2	1 kV	20 A	0.5 kV	10 A	
3	2 kV	40 A	1 kV	20 A	
4	4 kV	80 A	2 kV	40 A	
Repetition frequency: 5 kHz 2.5 kl	t for V_0 across 50- Ω load = Hz for V_0 across 50- Ω load				
Burst duration: 15 ms Burst period: 300 ms				The A	

Note: Voltage waveform across 50-Ω load: 5-ns risetime; 50-ns duration

through radiation. Included are such events as direct-injection discharge to keyboards, switches, metal housings, connector pins, and any other parts accessible to people. Without adequate protection, ESD stresses inadvertently applied at any of these locations can cause brief or permanent malfunction. This demands built-in immunity.

* Open-circuit voltage

** Short-circuit current

Other adverse effects are caused by radiated energy resulting from discharge between two objects outside the equipment. The resulting electromagnetic energy is coupled into unpredictable and possibly sensitive sections of the circuit and may cause problems.

IEC 801-2 uses a "humanbody model" to define the ESD threat against which qualifying equipment is protected. Following the pattern of the other two standards, four severity levels are defined. The chosen level depends on anticipated conditions of humidity and materials within the installation (Table 4). One extreme is a humidity-controlled computer room with static-controlled surfaces. The other is a remote monitoring station without air conditioning and special protective measures. Within the referenced table, three columns with voltage-related headings are given. The first, labeled "maximum charge," is the assumed voltage of the human body under the deThe ESD potential of the human body can exceed 15 kV in arid or sub-freezing (low-humidity) environments. fined conditions.

The next two columns indicate the charging voltage of a storage capacitor (Cs) within a specified ESD generator for subsequent immunity testing (Fig. 3). One set of voltages, which ranges up to 8 kV, is for the "contact" test method. For this case, the relay (discharge switch) is initially in an open position, the storage capacitor is charged to the chosen level, and the generator probe with a pointed tip is brought into contact with the target. Closing the relay applies the ESD stress.

The last column involves the "air-discharge" method, in which the relay is kept closed and, with the storage capacitor charged to the indicated voltage, a rounded tip probe is advanced rapidly toward the target. The ESD-stress event occurs through arcing.

The "air-discharge" method is recommended only for insulation-withstand voltage tests. This method also indirectly tests for upset under corona discharge at the probe tip.

Although in practice injection is almost always by air discharge, the contact method is preferred for conductive surfaces. That's because the resulting applied current, which is the principal parameter of interest, is more easily repeated. However, it's important to note that the air-discharge approach can pro-

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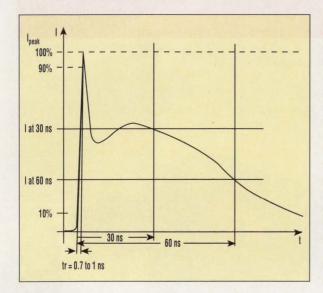
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duce intense localized radiation that may not be present with contact discharge. Therefore, in a practical sense, the contact method may fail to adequately test for certain aspects of radiation immunity.

The standard specifies the ESD-current waveform and associated peak amplitudes for the four levels (Fig. 4 and Table 5. respectively). All of the related times are in the range of nanoseconds. Included are the extremely fast rise time between 0.7 and 1 ns, a second peak current close to 30 ns, and a short overall duration (based on the peak of the second amplitude) of 60 ns.

Although it's evident that ESD events contain very little energy (on the order of tens to hundreds of microjoules), the extremely fast rise time plays a major role in the destruction of microcircuits. Both bipolar and CMOS ICs typically have ESDfailure thresholds of less than 2000 V. Consequently, failures occur at levels imperceptible at the fingertip, where the sensitivity threshold is around 3500 V.

ESD protection is generally provided by good shielding and bonding practices against externally radiated emissions, and by transient suppressors to divert ESD-conducted currents. The important parameters in the 4. The simulated ESD current waveform involves extremely short times. The rise time of the first peak is 1 ns or less with a second peak achieved in less than 30 ns. Consequently, parasitic impedances play a significant role in voltage-suppression performance.



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choice of a suppressor are low clamping voltage, a fast response time, and a package with minimal lead inductance. The last two attributes are essential in handling the fast ESD-current rise time with a low clamping-voltage overshoot. These requirements invariably point to the AJTVS as the component of choice. Axial-leaded devices are proven to be effective in suppressing ESD. Surface-mounted devices, however, offer very low inductance-about 3 nH for discrete offerings.

Note that peak power rating was not mentioned. With no surge-suppression requirements, and with the small ESD energy involved, the size of the suppressor die is determined by the required clamping voltage (and also by capacitance requirements for high data rate applications) rather than by power rating. To further illustrate this point, a data-line AJTVS suppressor chosen to provide lightning-surge immunity at the Installation Class 2 Level (24 A for a 1.2/50-µs waveform) is stressed at less than 10% of its full rating with application of the maximum specified level of ESD current.

Of primary importance in ESD-suppression design is the accompanying circuit-board layout. Current flow, resulting from voltage suppression, must be diverted through a low-impedance path to a common reference on the board. Ideally, this reference is a full conductive layer in the board. Low parasitic inductance in this total shunt path reduces the self-induced voltage, the L (di/dt) effect, which would otherwise add to the suppressor's clamping voltage.

The prior EFT-related discussion on the influence of parasitic impedances presented by board traces to and from the suppression network is equally, if not more, applicable to the ESD case. Refer to that discussion for important guidelines in this area.

Circuit-layout precautions are also critical in skirting problems from internally generated radiation. The fast rise time of the ESD current in a circuitboard conductor produces radiation that can generate induced voltages into parallel and adjacent traces. That's why it's necessary to carefully restrict conducted-ESD currents to strategically located traces away from the circuit's sensitive areas. As a general rule, place suppression devices close to data ports. which are typically the immediate points of ESD entry.

Finally, when threats from surges and EFT are also present with ESD, the meeting of all immunity specifications requires careful choice and coordination of circuit-board layouts. It's important to consider the recommended suppression practices for each of the stresses and formulate an approach that satisfies each requirement within the protection scheme.

As indicated at the outset, both market forces (driven by emerging and eventually mandatory standards) and reliability requirements dictate that designers learn transient-voltage suppression. Fortunately, the formulation of the IEC 801 immunity standards is a major and practical step toward defining essential parameters of the three

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TABLE 4: SEVERITY LEVELS AND RECOMMENDED **TEST VOLTAGES (FOR IEC 801-2)** Voltages (kV) **Relative humidity** Maximum Test Test Class as low as C% Anti-static Synthetic Charge (contact) (air) 35 X 2 2 2 10 X 4 4 4

X

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TABLE 5: IEC 801-2 WAVEFORM PARAMETERS					
Levels	Indicated voltage	First peak current of discharge (+/-10%)	Risetime (tr) with discharge switch	Current (+/-30%) at 30 ns	Current (+ /-30%) at 60 ns
1	2 kV	7.5 A	0.7 to 1 ns	4 A	2 A
2	4 kV	15.0 A	0.7 to 1 ns	8 A	4 A
3	6 kV	22.5 A	0.7 to 1 ns	12 A	6 A
4	8 kV	30.0 A	0.7 to 1 ns	16 A	8 A

major threats, namely, electrical surge, EFT, and ESD. The documents also "harmonize" requirements so that both manufacturers and suppliers of equipment agree on what makes for acceptable transient immunity.

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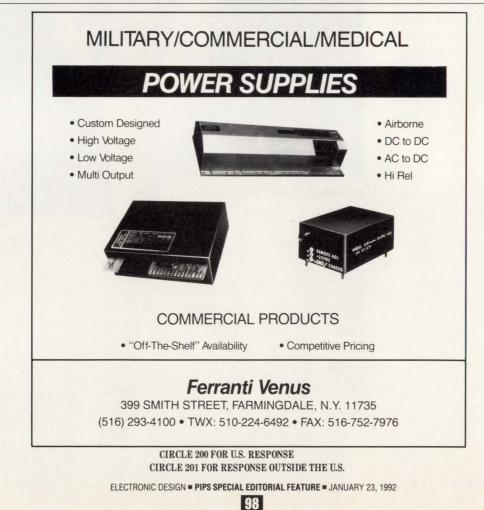
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O. Melville Clark, senior member of the technical staff at General Semiconductor Industries Inc., holds a BA and MA in physical science from Arizona State University, Tempe.

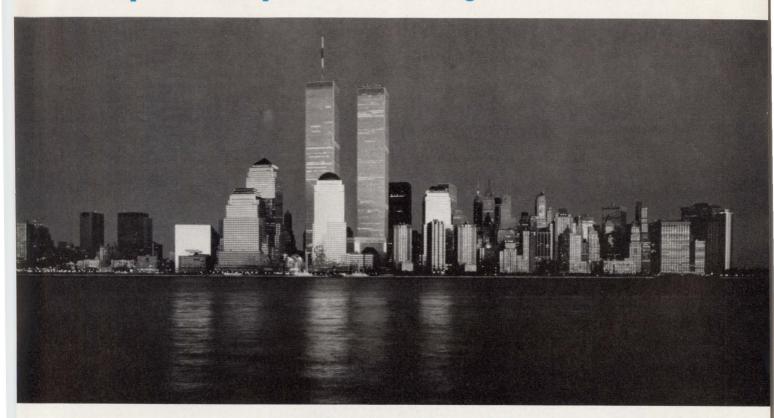
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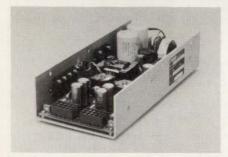


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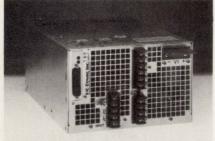
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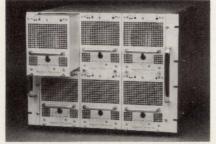
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Computer Products Inc. Power Conversion America P.O. Box 5102 Fremont, CA 94537-5102 (415) 657-6700

(50S) (LA) (CV) (RP) (UN) CIRCLE 649 **Controlled Power Co.** 1955 Stephenson Hwy. Troy, MI 48083 (313) 528-3700 (50S) (51S) (500S) (10S) (11S) (200S) (50R) (51R)

Our newest line of defence against heat.



Insist on Interpoint.

A full line of high-temperature DC-DC converters from the industry leader.

Get the hottest technology in board-mounted power supplies. Full military temperature range. Unsurpassed reliability. The lowest profiles. You can get it all with Interpoint's new line of DC-DC converters.

From arctic blasts to desert storms, Interpoint's new generation DC-DC converters stand up to the toughest military environments. They deliver full power over the entire -55° to +125° C. temperature range. And over an unprecedented power range, too. Interpoint can now offer you an off-the-shelf hybrid power supply for any power level from 2 to 200 watts.

For more than a decade, Interpoint DC-DC converters have proven their reliability in many of the world's most

MSA Series: 5 W, 125° C.

Interpoint's new line of DC-DC converters features constant PWM switching frequencies from 500 to 700kHz. Built-in sync. Parallel operation. Up to 50 dB audio rejection. Line and load regulation as low as 0.1%. And full MIL-STD-704 input for 28- and 270-volt systems.

CIRCLE 120 FOR U.S. RESPONSE

CIRCLE 121 FOR RESPONSE OUTSIDE THE U.S.

advanced weapons systems — including mission-critical electronics on the Leopard II Tank and Harrier Aircraft, the Bradley Fighting Vehicle and F/A-18 aircraft. Our new generation converters are the most reliable yet. Each of them was designed with the specific intent of being qualified to the full performance and reliability standards of MIL-STD-883C.

And Interpoint continues to lead the way in power supply miniaturization. With power densities as high as 40 watts per cubic inch and package heights as low as 6.8 mm, this new generation of converters is built for the tightly packed boards in today's military and commercial avionics, ground vehicles and portable equipment.

> It's the hottest new technology in DC-DC converters. And it's available only from Interpoint. For more information, call 44 (0)276-26832.



The Parade, High Street Frimley, Surrey GU165HY, England

POWER

SWITCHING SUPPLIES **ARE EASILY INTEGRATED**

Ease of integration into systems is featured in the LZ Series switching power supplies. The 1000-W unit offers auto-selectable ac input from 85



to 132 V ac or from 170 to 265 V ac. Other features include operation from -30 to +71°C, single-wire current sharing, and all status indications. Pricing starts at \$1025 in lots of 25 and delivery is from stock.

Lambda Electronics 515 Broad Hollow Rd. Melville, NY 11747 (516) 694-4200 ► CIRCLE 845

LOGIC-CONTROLLED SUPPLY SHRUGS OFF INPUT SWINGS

The model 70423 logic-controlled switcher self-adjusts to any input from 92 to 264 V ac, 47 to 450 Hz, with no jumpers, taps, switches, or other circuit modifications. The 160-W unit monitors the output of each of its six



channels and latches itself off if any voltage is out of specification (high or low), if output currents exceed ratings, or if an overtemperature condition occurs. Pricing is \$259 in lots of 1000. Large lots are delivered in 16 weeks.

Onan Power/Electronics 9713 Valley View Rd. Minneapolis, MN 55344 (612) 943-4642 ► CIRCLE 846

POWER-SOURCE MANUFACTURERS

Conversion Devices Inc. 15 Jonathan Dr Brockton, MA 02401

(508) 559-0880 (50C) (DC) **CIRCLE 651**

Crydom Co. 6015 Obispo Ave. Long Beach, CA 90805 (310) 865-3536 (RE) (TH) **CIRCLE 652**

Current Technology 101 W. Buckingham Rd. Richardson, TX 75081 (214) 238-5300 (50S) (51S) (11S) (200S) (RM) (CV) (PR) (UN) (PF) (50C) (51C) (11C) (200C) (AC) (SW) (MU)

CIRCLE 653

Custom Power Systems

33 Comac Loop Ronkonkoma, NY 11779 (516) 467-5328 (50S) (51S) (500S) (10S) (11S) (200S) (LA) (RM) (OF) (CV) (RP) (MD) (PF) (50C) (51C) (500C) (10C) (11C) (200C) (DC) (MO) (MI) (50R) (51R) (500R) (10R) (11R) (200R) (LI) (SW) (MU) (ML) CIRCLE 654

Cyberpak Co.

Custom Design 251 S. Frontage Rd., #23 Burr Ridge, IL 60521 (800) 328-3938 (11S) (200S) (OF) (CV) (11C) (200C) (11R) (200R) (SW) **CIRCLE 655**

D&B Power Inc. 204 N. Fehr Way, P.O. Box 40M Bayshore, NY 11706 (516) 586-5955 (50S) (10S) (11S) (OF) (CV) (MD) (50C) (11C) (MI) (50R) (10R) (11R) (LI) **CIRCLE 656**

Datel Inc. 11 Cabot Blvd. Mansfield, MA 02048 (508) 339-3000 (51S) (10S) (LA) (CV) (PR) (50C) (DC) (MO) CIRCLE 657

Delta Products Corp. 3225 Laurelview Cl Fremont, CA 94538 (510) 770-0660 (50S) (51S) (10S) (11S) (200S) (OF) (PF) (50C) (51C) (10C) (11C) (DC) (AC) (50R) (51R) (10R) (11R) (200R) (SW) CIRCLE 658

Deltec Electronics Corp. PowerRite Div. 2727 Kurtz St. San Diego, CA 92110 (619) 291-4211

(200S) (UN) **CIRCLE 659** **Deltron Inc.** 290 Wissahickon Ave. North Wales, PA 19454 (215) 699-9261 (50S) (11S) (200S) (OF) (PF) (714) 979-4440 (50S) (EX) **CIRCLE 660**

Endicott Research Group Inc.

P.O. Box 267 Endicott, NY 13760 (607) 754-9187 (50C) (10C) (11C) (DC) (AC) (50R) (LI) (SW) **CIRCLE 661**

Entran Devices Inc. 10 Washington Ave Fairfield, NJ 07004 (201) 227-1002

(50S) (LA) (RM) (CV) CIRCLE 662

Ericsson Components Inc. Power Products Div. 403 International Pkwy., #500 Richardson, TX 75081 (214) 997-6561 (50S) (11S) (200S) (RM) (OF) (50C) (10C) (11C) (DC)

CIRCLE 663 **Ericsson Network Systems** Power Systems Div P.O. Box 833875

Richardson, TX 75083-3875 (214) 669-0906 (50S) (200S) (PF) **CIRCLE 664**

Exide Electronics 8521 Six Forks Rd. Raleigh, NC 27615 (919) 872-3020 (LC)

CIRCLE 665

Fedco Electronics Inc. P.O. Box 1403 Fond Du Lac, WI 54936 (800) 542-9761 (50S) (10S) (11S) (50C) (10C) (11C) (200C) (AC) (AL) (CZ) (LC) (LT) (ME) (NC) CIRCLE 666

Fiskars Electronics Corp. P.O. Box 1490, Newton Rd. Littleton, MA 01460 (508) 486-9551 (51S) (200S) (LA) (RM) (CV) (PR) (MD) (50C) (51C) (11C) (200C) (DC) (AC) **CIRCLE 667**

Fujitsu Microelectronics Integrated Circuits Div. 3545 N. First St. San Jose, CA 95134-1804 (408) 922-9000 (BT) (PI) (PC) CIRCLE 668

Gamma High Voltage Research 1096 N. U.S. Hwy. #1 Ormond Beach, FL 32174 (904) 677-7070 (51S) (500S) (10S) (11S) (200S) (LA) (RM) (CV) (RP) (51C) (500C) (10C) (11C) (200C) (DC) (MO) CIRCLE 669

Gates Energy Products Inc. Portable Battery Div P.O. Box 147114 Gainesville, FL 32614-7114 (904) 462-3911 (LC) (NC) (NH) (NM) CIRCLE 670

Gennum Corp. P.O. Box 489, Station A Burlington, Ontario Canada, L7R 3Y3 (416) 632-2996 (PC) CIRCLE 671

Georator Corp. 9617 Center St

Manassas, VA 22110 (800) 523-9938 (200S) (OF) (PR) (MD) (51C) (200C) (MI) (AT) CIRCLE 672

Germanium Power Devices Corp.

P.O. Box 3065, SVS Andover, MA 01810-3065 (508) 475-5982 (REC) CIRCLE 673

Glassman High Voltage P.O. Box 551, Route 22 Whitehouse Station, NJ 08889 (908) 534-9007 (500S) (200S) (LA) (RM) (CV) (RP) CIRCLE 674

HC Power Inc. 17032 Armstrong Ave. Irvine, CA 92714-5716 (714) 261-2200

(50S) (RM) (CV) (PF) (DC) (50R) (SW) CIRCLE 675

Harris Semiconductor IC Products Div.

1301 Woody Burke Rd. Melbourne, FL 32902 (407) 724-3886 (50C) (DC) (IC) (50R) (51R) (LI) (SW) (ID) (PC) CIRCLE 676

Harris Semiconductor 724 Rte. 202, P.O. Box 591 Somerville, NJ 08876 (201) 685-6920 (50S) (51S) (10S) (11S) (OF) (CV) (MD) (50C) (51C) (DC) (AC) (IC) (50R) (51R) (10R) (11R) (LI) (SW) (MU) (ID) (ML) (BT) (MF) (RE) (TH) (PI) (PC) CIRCLE 678

Hewlett-Packard Co. Power Supplies Div. 19310 Pruneridge Ave. Cupertino, CA 95014 (800) 452-4844 (50S) (51S) (LA) (RM) (CV) (RP) CIRCLE 679

(see p. 116 for key) (continued on p. 106)

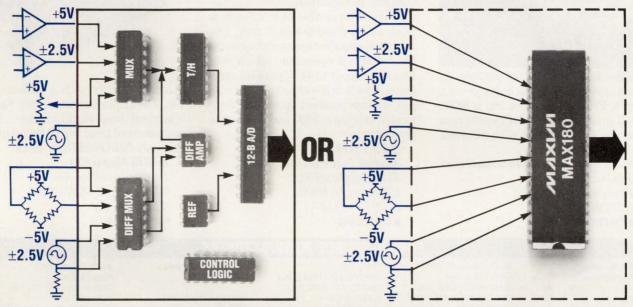
ELECTRONIC DESIGN = PIPS SPECIAL EDITORIAL FEATURE = JANUARY 23, 1992



COMPLETE 12-BIT DAS HAS PROGRAMMABLE MUX

Plus On-Chip T/H, ADC and 25ppm/°C Voltage Reference

Maxim's new MAX180 is a complete 10µs data-acquisition system (DAS) that combines a no-missing codes 12-bit A/D, a wide-bandwidth (6MHz) track-hold, a 25ppm/°C voltage reference, a fast-parallel µP interface, and a Flex-Mux, Maxim's flexible 8-channel analog multiplexer—all in a single package. Program each channel independently to fit your ranges: differential or single-ended, unipolar +5V or bipolar ±2.5V. Simplify your design. Save time and \$\$.



The MAX180's Flex-Mux easily handles single-end, differential, bipolar, or unipolar signals from any input source.

Add a Filter or PGA Easily

For applications where a programmable-gain amplifier (PGA) or a filter is required following the multiplexer, Maxim's 6-channel MAX181 gives you access to the Flex-Mux output, and otherwise works the same as the MAX180. With the same simplicity, and even more flexibility.



FREE A/D Converter Design Guide

Simply circle the reader response number, contact your Maxim representative or Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086, (408) 737-7600, FAX (408) 737-7194.



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* 1000-up FOB USA, suggested resale

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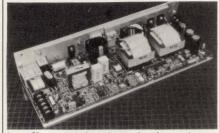
CIRCLE 190 FOR U.S. RESPONSE

CIRCLE 191 FOR RESPONSE OUTSIDE THE U.S.

POWER

350-W SWITCHING SUPPLY **CORRECTS POWER FACTOR**

A four-output, 350-W switcher incorporates built-in active power-factor correction and accepts universal inputs. The PFQ350 switcher takes any input from 90 to 264 V ac with no jumpers. Main output rating is 5 V at 50 A. One of the auxiliary outputs



handles 10 A/16 A peaks for spin-up loads associated with hard-disk drives. Pricing in lots of 100 is \$339. Small quantities are delivered from stock to three weeks with 12-week leads for large lots.

Switching Systems International 500 Porter Way Placentia, CA 92670 (714) 996-0909 ► CIRCLE 847

Miami Lakes, FL 33014

(51S) (500S) (RM) (OF) (CV) (51C) (500C) (DC)

San Jose, CA 95131-1109

(MF) (RE) (TH) (PI) (PC)

Advanced Analog

Santa Clara, CA 95050

(50C) (10C) (11C) (DC)

Integrated Power Designs

Lawrenceville, NJ 08648

(50R) (10R) (11R) (SW)

International Power DC

Power Supplies Inc.

355 N. Lantana, Suite 710

Camarillo, CA 93010-9030

(50S) (200S) (RM) (OF) (LI)

(50S) (11S) (200S) (OF) (CV)

(50C) (10C) (11C) (DC) (MO)

2270 Martin Ave.

(408) 988-4930

9C Princess Rd.

(609) 896-2122

CIRCLE 688

(805) 987-7900

155 N. Beacon St

Brighton, MA 02135

CIRCLE 689

CIRCLE 687

Inc.

(305) 822-2558

CIRCLE 685

IXYS Corp.

2355 Zanker Rd.

(408) 435-1900

CIRCLE 686

Intech Inc.

VARIABLE DC BENCH SUPPLY **IS THREE SUPPLIES IN ONE**

Designed to power a mix of analog and digital circuitry, the model 1651 triple-output bench supply is three



supplies in one. Included within the unit are two variable 24-V, 0.5-A supplies and a fixed 5-V, 4-A unit. The two 24-V supplies are switch-selectable for series operation, which doubles the output to 48 V; parallel operation, which delivers up to 1 A of output; or independent operation. Suggested pricing is \$395 and delivery is from stock.

B&KPrecision

Maxtec International Corp. 6470 Cortland St. Chicago, IL 60635 (312) 889-1448 CIRCLE 848

POWER-SOURCE MANUFACTURERS

(617) 782-3331 (50C) (51C) (10C) (11C) (200C) (DC) (MO) (IC) **CIRCLE 690**

International Power Sources Astec High Voltage 200 Butterfield Dr. Ashland, MA 01721 (508) 881-8407 (51S) (500) (10S) (11S) (200S) (LA) (RM) (CV) (RP) (MD) (51C) (500C) (10C) (11C) (200C) (DC) (AC) (MI) CIRCLE 691

International Power Sources 200 Butterfield Dr. Ashland, MA 01721 (508) 881-7434 (50S) (50C) (DC) (MO) (IC) CIRCLE 692

10301 Willow Rd. Redmond, WA 98073-9705 (206) 882-3100 (50C) (10C) (11C) (DC) (MI) **CIRCLE 694**

Intronics Inc. 150 Dan Rd. **International Power Devices** Canton, MA 02021 (617) 828-4992

(DC) (MO) (IC) (SW) CIRCLE 695

Jameco Electronics 1355 Shoreway Rd. Belmont, CA 94002 (415) 592-6718 (11S) (200S) (RM) (OF) (CV) (PR) (LT) (NC) (BT) (RE) CIRCLE 696

James Electronics Inc. 4050 N. Rockwell St. Chicago, IL 60618 (312) 463-6500 (50S) (10S) (11S) (RM) (OF) (50C) (11C) (DC) CIRCLE 697

Jerome Industries 730 Division St. Elizabeth, NJ 07201 (201) 353-5700 (50S) (10S) (11S) (CV) (50C) (50R) (LI) (SW) CIRCLE 698

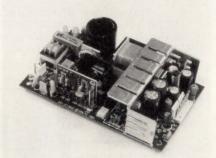
Jeta Power Systems Inc. 2675 Junipero Ave. Signal Hill, CA 90806 (213) 427-0095 (50S) (200S) (CV) CIRCLE 699

John Fluke Mfg. Co. Philips T & M Group Box 9090 Everett, WA 98203 (206) 356-6157 (50S) (51S) (LA) (RM) (CV) (RP)

CIRCLE 700

WIDE-INPUT SUPPLY **SPANS 85 TO 265 V AC**

Automatic operation with any voltage from 85 to 265 V ac and from 120 to 364 V dc at a 100-kHz switching frequency is featured in the ZPS-45 switcher. The 45-W unit is a 3-by-5-in.



board assembly with a 1.25-in. profile. The triple-output supply has no minimum load requirements. Suggested retail price is \$55. Small quantities are delivered from stock.

Zenith Magnetics 1000 Milwaukee Ave. Glenview. IL 60025-2493 (708) 391-7733 ► CIRCLE 849

Hitachi America Ltd. Semiconductor & IC Div. 2000 Sierra Point Pkwy Brisbane, CA 94005-1819 (415) 589-8300 (SW) (BT) (MF) (PI) (PC) CIRCLE 680

Hitran Corp.

Power Systems Div. 362 Highway 31 Flemington, NJ 08822 (908) 782-5525 (50S) (51S) (200S) (CV) (51C) (200C) (AC) CIRCLE 681

Hokuriku USA, Ltd. 8145 River Dr. Morton Grove, IL 60053 (708) 470-8440 (50C) (DC) (MO) CIRCLE 682

Hydrocap Corp. 975 N.W. 95th St Miami, FL 33150-2095 (305) 696-2504 (LC) (NC) **CIRCLE 683**

ILC Data Device Corp. 105 Wilbur Pl Bohemia, NY 11716 (516) 567-5600 (50C) (11C) (200C) (DC) (MO) (MI) CIRCLE 684

IMC Magnetics Corp. Florida Div 14025 N.W. 60th Ave.

International Rectifier 233 Kansas St El Segundo, CA 90245 (213) 772-2000 (MF) (RE) (TH) (PI) CIRCLE 693 Interpoint Corp.

(LA) (RM) (OF) (CV) (50C)

Joule Power Inc. Summer Rd. Boxborough, MA 01719 (508) 263-9712 (50S) (RM) (OF) (CV) (UN) (PF) (50C) (DC) (50R) (SW) CIRCLE 701

Kaiser Systems Inc. 126 Sohier Rd. Beverly, MA 01915 (508) 922-9300 (500S) (200S) (LA) (RM) (CV) **CIRCLE 702**

Keltec Florida Inc. 84 Hill Ave Ft. Walton Beach, FL 32548 (904) 244-0043 (50S) (51S) (500S) (10S) (11S) (200S) (MD) (50C) (11C) (DC) (MI)

CIRCLE 703

Kepco Inc. 131-38 Sanford Ave. Flushing, NY 11352 (718) 461-7000 (50S) (51S) (500S) (10S) (11S) (200S) (LA) (RM) (OF) (CV) (PR) (RP) (PF) (50C) (10C) (11C) (DC) (AC) (MO) (50R) (51R) (500R) (10R) (11R) (200R) (LI) (SW) (MU) CIRCLE 704

(see p. 116 for key) (continued on p. 108)

ELECTRONIC DESIGN = PIPS SPECIAL EDITORIAL FEATURE = JANUARY 23, 1992



SMALL +5V REGULATOR HAS 94% EFFICIENCY!

No Design Required for Guaranteed 300mA or 750mA Outputs

The new MAX730 and MAX738 step-down switching regulators are compact and simple solutions for batterypowered portable applications. They extend battery life by providing high-efficiency step-down regulation. The MAX730 comes in an 8-pin SOIC package, making it the smallest PWM step-down regulator available. They are easy to use, requiring no design effort or inductor selection. Using the single set of component values listed in the data sheet, the standard application circuit delivers the guaranteed power over all specified line, load, and temperature conditions.

The MAX730/738 are loaded with features, including short-circuit and soft-start protection, and a pin-controlled shutdown that cuts quiescent supply current to 6μ A. High-frequency 160kHz pulse-width modulation (PWM) current - mode control provides low-noise operation and reduces output voltage ripple to less than 50mVp-p.

EFFICIENCY vs. OUTPUT CURRENT No Component or Inductor Selection Required **Guaranteed Output Currents:** 90 750mA for V+ > 10.2V (MAX738) **MAX738** 80 300mA for V+ > 6.0V (MAX730) MAX730 EFFICIENCY (%) 70 Space Saving Footprints: 60 8-Pin SOIC and DIP Packages (MAX730) 16-Pin SOIC and 8-Pin DIP (MAX738) 50 Wide Input Voltages: 40 200 400 600 800 1000 +5.2V to +11.0V (MAX730) OUTPUT CURRENT (mA) +6.0V to +16.0V (MAX738) The MAX730 and MAX738 deliver high efficiency over a wide load range EXTEND BATTERY LIFE AND SAVE SPACE INCHES INPUT +5.2V TO +11V 150µF MAXIM 330pF 510 OUTPUT +5V @ 300mA 100µH 0.1 IN5818 100ul CENTIMETERS

The MAX730 application circuit fits into 1.125in² (7.25cm²) of board space

FREE Power Supply Design Guide



Includes: Application Notes + Data Sheets + Cards For Free Samples

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CIRCLE 192 FOR U.S. RESPONSE

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POWER

HIGH-VOLTAGE SUPPLIES BOAST PRECISE OUTPUTS

Easy front-panel controls with analog voltage and current meters are featured in the Alpha III series of precision lab power supplies. Three units are available with positive or negative outputs of 0 to 5 kV at 10 mA (model 3507), 0 to 15 kV at 3 mA (model 3707), and 0 to 30 kV at 1.5 mA (model 3807). Output drift is less than 20 ppm and noise is less than 0.01% pk-pk. Line and load regulation values are 0.001% and 0.002%, respectively. Fine and coarse adjustments are provided for the output voltage. Pricing is \$3995 each with delivery from stock.

Astec High Voltage

200 Butterfield Dr. Ashland, MA 01721 (508) 881-8407 ▶ CIRCLE 850

TWO SUPPLIES TEAM UP TO DELIVER 10 KW

Two independent-output supplies are combined to provide up to 10 kW in the Series 5600, 5700, and 5800 switching-regulator supplies. The unit, which fits in a single 19-in. rack, saves over 50% in rack space and 40% in weight compared with two separate units. Nineteen different output voltage-current combinations are available. Pricing ranges from \$3250 to \$4900 with delivery from stock to 60 days.

Power Ten Inc. 486 Mercury Dr.

Sunnyvale, CA 94086 (408) 738-5959 ▶ CIRCLE 851

ON-LINE UPS SYSTEM KEEPS POWER CLEAN

A reliable source of clean, continuous, sine-wave ac power is provided to computers and other sensitive equipment by the UPSY Series of uninterruptible power supplies. The 120-V, 60-Hz systems come in 400-, 800-, and 1250-VA models. Units are also available with 220/240-V and 50-Hz ratings. Pricing ranges from \$1150 to \$2995 depending on the model. Delivery is from stock.

Superior Electric Co. 383 Middle St. Bristol, CT 06010 (203) 582-9561 ▶ CIRCLE 852

POWER-SOURCE MANUFACTURERS

Kikusui International 1980 Orizaba Ave. Signal Hill, CA 90804 (800) 545-8784 (50S) (51S) (500S) (11S) (200S) (LA) (RM) (CV) (PR) (RP) CIRCLE 705

LH Research Inc.

14402 Franklin Ave. Tustin, CA 92680 (714) 730-0162 (505) (105) (115) (2005) (RM) (OF) (CV) (UN) (PF) (50C) (10C) (11C) (200C) (DC) (MO) (50R) (10R) (11R) (200R) (LI) (SW) (MU) CIRCLE 706

LZR Electronics Inc. 8051 Cessna Ave. Rockville, MD 20855 (301) 921-4600 (50S) (51S) (LA) (OF) (CV) (PR) (50C) (51C) (DC) (AC) CIRCLE 707

Lambda Electronics Inc. 515 Broad Hollow Rd. Melville, NY 11747-3700 (516) 694-4200 (50S) (51S) (10S) (11S) (200S) (LA) (RM) (OF) (CV) (RP) (MD) (UN) (PF) (50C) (51C) (10C) (11C) (200C) (DC) (MO) (MI) CIRCLE 708

Linear Technology Corp. 1630 McCarthy Blvd. Milpitas, CA 95035-7487 (408) 432-1900 (50C) (10C) (DC) (IC) (MI) (50R) (51R) (11R) (10R) (LI) (5W) (ID) (ML) (PI) (PC) CIRCLE 709

Logitek Inc.

101 Christopher St. Ronkonkoma, NY 11779 (516) 467-4200 (50S) (51S) (500S) (10S) (11S) (200S) (RM) (CV) (MD) (50C) (51C) (50C) (10C) (11C) (200C) (DC) (MO) (MI) CIRCLE 710

M.S. Kennedy Corp. 8170 Thompson Rd. Clay, NY 13041 (315) 699-9201 (50R) (51R) (10R) (11R) (LI) (ML) CIRCLE 711

MIL Electronics Inc. 106 Perimeter Rd. Nashua, NH 03063 (603) 882-3200 (50S) (51S) (10S) (11S) (CV) (500C) (10C) (11C) (DC) (MO) (MI) (50R) (51R) (500R) (10R) (11R) (SW) (ML) CIRCLE 712

Marathon Power

Technologies Filitetronics Div. P.O. Box 8233 Waco, TX 76714-8233 (817) 776-0650 (51S) (11S) (200S) (RM) (PR) (MD) (50C) (DC) (AC) (MI) (NC) CIRCLE 713 Marconi Circuit Technology 160 Smith St. Farmingdale, NY 11735 (516) 393-8686 (BT) (TH) (PC) CIRCLE 714

Maxell Corp. of America 22-08 Route 208 S.

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Maxim Integrated Products

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Micrel Semiconductor 560 Oakmead Pkwy. Sunnyvale, CA 94086 (408) 245-2500 (SW) (ID) CIRCLE 718

Micro Linear Corp. 2092 Concourse Dr. San Jose, CA 95131 (408) 433-5200 (PC)

CIRCLE 719

Micropac Industries Inc. 905 E. Walnut St. Garland, TX 75040 (214) 272-3571 (50S) (51S) (10S) (11S) (CV) (MD) (50C) (51C) (10C) (11C) (DC) (MO) (MI) (50R) (10R) (11R) (LI) (MU) (ML) CIRCLE 720

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Microsemi Corp.

Micro Quality Semiconductor 1000 N. Shiloh Rd., P.O. Box 469013 Garland, TX 75046-9013 (214) 272-7811 (RE) CIRCLE 722

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Modular Devices Inc. One Rone Rd. Brookhaven Shirley, NY 11967 (516) 345-3100 (50S) (51S) (50OS) (10S) (11S) (200S) (RP) (MD) (50C) (51C) (500C) (10C) (11C) (DC) (AC) (MO) (IC) (MI) (50R) (51R) (500R) (10R) (11R) (200R) (LI) (SW) (MU) (ID) (ML)

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Motorola Inc.

Semiconductor Products Sector 3102 N. 56th St. Phoenix, AZ 85018-6606 (602) 952-4103 (50R) (10R) (LI) (SW) (ID) (BT) (MF) (RE) (TH) (PI) (PC) CIRCLE 726

MultiProducts International 250 Lackawanna Ave.

West Paterson, NJ 07424 (201) 890-1344 (50S) (51S) (10S) (11S) (LA) (CV) (EX) (50C) (51C) (10C) (11C) (DC) (AC) (MO) (50R) (10R) (11R) (LI) (SW) (MU) CIRCLE 727

Multiplier Industries

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4607 S.E. International Way Milwaukie, OR 97222 (503) 659-7932 (505) (51S) (500S) (200S) (OF) (CV) (PR) (RP) (MD) (50C) (51C) (500C) (11C) (200C) (DC) (MI) CIRCLE 731

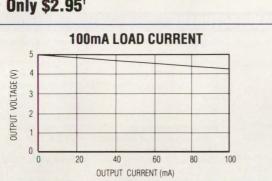
(see p. 116 for key) (continued on p. 110)

NO INDUCTORS! +5V IN/-5V OUT INVERTER **POWERS 100mA LOAD**

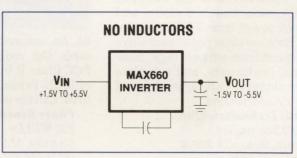
MAX660 Plus 2 Capacitors Deliver 95% Efficiency

Using two low-cost capacitors, Maxim's new MAX660 charge-pump voltage inverter converts a 1.5V to 5.5V input to a -1.5V to -5.5V output. The charge pump's 100mA output replaces switching regulators, eliminating the need for inductors and their associated cost, size and EMI. For instance, with a 5V input, the MAX660 delivers 100mA at -4.35V. Compact 8-pin DIP and SOIC* packages coupled with a 95% powerconversion efficiency make the MAX660 ideal for battery-powered applications.

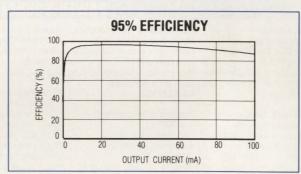
- Only 2 Capacitors, NO Inductors
- 10kHz and 45kHz Internal Oscillator
- Voltage Inverter Mode: Vout = -VIN
- Voltage Doubler Mode: Vout = 2 x Vin
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- 200µA No-Load Supply Current
- Only \$2.95⁺



Maxim's new MAX660 voltage inverter powers 100mA loads.



The MAX660 uses only 2 external components and is available in space-saving 8-pin DIP and SO packages.



High efficiency makes the MAX660 ideal for portable applications.



Includes: Application Notes Data Sheets Cards For Free Samples

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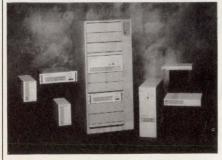
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CIRCLE 195 FOR RESPONSE OUTSIDE THE U.S.

POWER

SINGLE-PHASE UPS PROTECTS MAINFRAMES

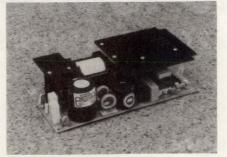


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Pacific Power Source Corp. 15122 Bolsa Chica St Huntington Beach, CA 92649 (714) 898-2691 (50S) (51S) (11S) (200S) (LA) CIRCLE 742 CIRCLE 737

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Philips Components 2001 W. Blue Heron Blvd. Riviera Beach, FL 33404 (407) 881-3308 (BT) (MF) (RE) (TH) (PI) (PC) **CIRCLE 741**

Phoenix Contact Inc. P.O. Box 4100

Harrisburg, PA 17111-0100 (717) 944-1300 (50S) (11S) (LA) (CV) (50R) (LI) (MU)

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Pioneer Magnetics Inc.

1745 Berkeley St. Santa Monica, CA 90404 (213) 829-6751 (50S) (10S) (11S) (200S) (RM) Crystal Lake, IL 60014 (CV) (RP) (UN) (PF) (50C) (10C) (11C) (200C) (DC) (MO) (50R) (10R) (11R) (200R) (SW) CIRCLE 744

Plainview Batteries Inc. 23 Newtown Rd. Plainview, NY 11803 (516) 249-2873 (AL) (LC) (LT) (NC) CIRCLE 745

Polytron Devices Inc. P.O. Box 398 Paterson, NJ 07544 (201) 345-5885 (50S) (LA) (RM) (CV) (MD) (50C) (DC) (MO) (IC) (MI) (50R) (LI) (SW) (MU) (ML) CIRCLE 746

Powell Electronics Inc. P.O. Box 8765 Philadelphia, PA 19101 (215) 365-1900 (AL) (CZ) (LC) (LT) (ME) (NC) (SO) (ZA) CIRCLE 747

Power Components Div. of Vanguard Electronics 1480 W. 178th St. Gardena, CA 90248 (213) 323-8120 (50S) (10S) (11S) (200S) (RM) (OF) (CV) (50C) (DC) CIRCLE 748

Power Conversion Products Inc.

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Power Integrations Inc. 411 Clyde Ave. Mountain View, CA 94043 (800) 552-3155 (PI) CIRCLE 751

Power Solutions Inc. 21 Fairwind Ct Northport, NY 11768 (516) 757-8749 (50S) (51S) (10S) (11S) (200S) (RM) (OF) (CV) (PR) (PF) (50C) (10C) (11C) (DC) (IC) (50R) (10R) (11R) (LI) (SW) (MU) (ID) CIRCLE 752

Power Switch Corp. 17 Vreeland St. Lodi, NJ 07644 (201) 478-5788 (50S) (11S) (200S) (50C) (10C) (11C) (200C) (DC) (MO) (LI) (SW) (MU)

Power Systems Inc. 45 Griffin Rd. South Bloomfield, CT 06002 (203) 726-1300 (50S) (51S) (500S) (11S) (200S) (OF) (CV) (PF) CIRCLE 754

CIRCLE 753

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(see p. 116 for key) (continued on p. 112)

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CIRCLE 856

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Powercube Corp. 1810 N. Glenville, #102 Richardson, TX 75081 (214) 480-9281 (50S) (51S) (10S) (11S) (200S) (MD) (50C) (51C) (10C) (11C) (200C) (DC) (MO) (MI) (50R) (51R) (10R) (11R) (200R) (L1) (SW) (MU) (ML) CIRCLE 762

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(619) 575-1100 (50S) (51S) (11S) (200S) (RM) (CV) (RP) (PF) (50C) (51C) (11C) (200C) (DC) (50R) (51R) (11R) (200R) (SW) (MU) CIRCLE 765

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Rantec Microwave & Electronics 9401 Oso Ave. Chatsworth, CA 91311 (818) 885-8223 (50S) (51S) (500S) (11S) (200S) (OF) (CV) (MD) (50C) (51C) (500C) (11C) (200C) (51C) (500C) (11C) (200C) (DC) (MO) (MI) (50R) (51R) (500R) (11R) (200R) (LI) (SW) (MU) (ML) CIRCLE 767

Rantec Microwave & Electronics 1173 Los Olivos Ave. Los Osos, CA 93402 (805) 528-5858 (500S) (10S) (11S) (OF) (MD) CIRCLE 768

Rayovac Corp. 601 Rayovac Dr. Madison, WI 53711-2497 (608) 275-3340 (AL) (LT) (SO) CIRCLE 769

Reich Associates Inc. Route 4, Box 4620 Lakehills, TX 78063 (512) 751-3220 (LA) (RM) (OF) (CV) (MD) (50C) (51C) (500C) (10C) (11C) (200C) (DC) (AC) (MI) (50R) (51R) (500R) (10R) (11R) (200R) (LI) (SW) (ML) CIRCLE 770

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Renata Batteries U.S. Electronics Div. 990 North Bowser Rd. Ste.900 Richardson, TX 75081 (214) 234-8091 (AL) (LT) (ME) (SO) (ZA) CIRCLE 772

Resonant Power Technology Inc. 3350 Scott Blvd., Bldg. 42/01 Santa Clara, CA 95054 (408) 982-0200 (50S) (51S) (11S) (200S) (OF) (CV) (MD) (PF) CIRCLE 773

Ritz Electronics Ltd. 196 Queens St. N. New Dundee, Ontario, Canada NOB 2EO (519) 696-2616 (505) (515) (LA) (RM) (OF) (CV) (UN) (50C) (DC) (AC) (LI) CIRCLE 774

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Sanyo Energy Corp. OEM Div. 2001 Sanyo Ave. San Diego, CA 92173 (619) 661-6620

(AL) (LT) (NC) (NM)

CIRCLE 778

Schaeffer Inc. 200 Butterfield Dr. Ashland, MA 01721 (508) 879-8658 (508) (518) (RM) (50C) (51C) (DC) (LI) (SW) CIRCLE 779

Sem Tech Corpus Christi 121 International Blvd. Corpus Christi, TX 78406 (512) 289-0403 (50R) (10R) (11R) (200R) (LI) (SW) (MU) (ID) (ML) (BT) ((PI) (PC) CIRCLE 780

Semiconductor Circuits Inc. 49 Range Rd. Windham, NH 03087 (603) 893-2330 (50S) (11S) (RM) (50C) (11C) (DC) (MO) (IC) CIRCLE 781

Semikron Inc. 11 Executive Dr., P.O. Box 66 Hudson, NH 03051 (603) 883-8102 (BT) (MF) (TH) CIRCLE 782

(see p. 116 for key) (continued on p. 114)

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CADNICA EXTRA. Sanyo's Cadnica E series incorporates high-density electrode plates in a new concept design for 40% greater capacity than conventional batteries and 1-hour charge capability via Sanyo's - ΔV voltage sensor changing method.

SOLAR. Sanyo leads the development of solar cells with the application of amorphous silicon for physical flexibility and the ability to be fabricated into large-area cells

NIMH. Sanyo's proprietary electrode manufacturing process and built-in resealable safety vent lead the development of high capacity, high performance rechargeable, Nickel Metal Hydride batteries.

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DNICA SUM

In New Jersey: (201) 641-2333 In Georgia: (404) 279-7377 In Dallas: (214) 480-8345

CAL

SANYO CADNICA BACKUP

> SANYO Energy (USA) Corporation CIRCLE 162 FOR U.S. RESPONSE **CIRCLE 163 FOR RESPONSE OUTSIDE THE U.S.**

CONVERTERS

SMALL 10-W CONVERTER HAS WIDE INPUT RANGE

Two input ranges of 10 to 33 V dc and 18 to 72 V dc are offered in the IPS 10 dc-dc converter. The 10-W unit comes with one or two isolated outputs of



 ± 5 , 12, or 15 V dc. Packaged in a 2by-2-by-0.41-in. metal case, the converter delivers 80% efficiency with 500-V rms input-to-output isolation.

Melcher Inc. 200 Butterfield Dr. Ashland, MA 01721 (800) 828-9712 ► CIRCLE 859

10-W DC-DC CONVERTERS **HAVE 1 OR 2 OUTPUTS**

Single or dual outputs are offered in the XWR Series of wide-input-range dc-dc converters. The 10-W units come in input ranges of 4.7 to 7 V dc, 9 to 18 V dc, and 18 to 72 V dc. A highfrequency, current-mode design yields fully regulated, low-ripple (25-



mV minimum) output power with efficiencies of up to 84%. Pricing starts at \$120 with delivery from stock.

Datel Inc. 11 Cabot Blvd. Mansfield, MA 02048 (508) 339-3000 ► CIRCLE 860

RUGGED PACKAGING HOUSES CONVERTERS

A packaging technology with inherent low-temperature gradients, wave solderability, and ruggedness distinguishes the DB2800 Series of dc-dc converters. The hermetic units are 22.5-W, 12- and 15-V converters that offer 33% more power at a 125°C case temperature than competitive units. There is no power derating over the full military temperature range. Pricing starts at \$298 in lots of 100. Samples are delivered from stock with production quantities delivered in six weeks.

Apex Microtechnology Corp. 2895 W. Rudasill Rd. Tucson, AZ 85741 (800) 421-1865 ► CIRCLE 861

SINGLE-OUTPUT CONVERTERS POWER MANY CIRCUITS

The DCU1-5-WR series of single-output dc-dc converters includes three models with one tightly regulated



output of 5, 12, or 15 V dc. The units accept inputs of 7 to 32 V (5-V output), 14 to 32 V (12-V output), and 17 to 32 V (15-V output). Each unit comes in a 1-by-2-by-0.38-in. copper case for low-noise operation. Pricing is \$82 in quantities up to 24.

Power General 152 Will Dr. Canton, MA 02021 (617) 828-6216 ► CIRCLE 862

POWER-SOURCE MANUFACTURERS

Shindengen America Inc. 5999 New Wilke Rd. Rolling Meadows, IL 60008 (708) 593-8585 (50S) (51S) (10S) (11S) (200S) (OF) (CV) (50C) (10C) 811 E. Arques Ave., (11C) (DC) (MO) (BT) (MF) (RE) (TH) (PI) (PC) CIRCLE 783

Shogyo International Corp. 287 Northern Blvd. Great Neck, NY 11021-4799 (516) 466-0911 (50S) (50C) (DC) (AC) (MO) (50R) (LI) CIRCLE 784

Siemens Components Inc. Integrated Circuit Div. 2191 Laurelwood Rd. Santa Clara, CA 95054 (408) 980-4547 (MF) (PI) (PC) CIRCLE 785

(BT) (MF) (RE) (TH) Sierra West Power Systems CIRCLE 789 2615 Missouri Ave., Bldg. 5 Las Cruces, NM 88001 (505) 522-8828 (50S) (51S) (500S) (10S) (11S) (200S) (RM) (OF) (CV) (RP) (MD) (PF) (50C) (51C) (500C) (10C) (11C) (200C) (DC) (AC) (MO) (MI) (50R)

(51R) (500R) (10R) (11R) (200R) (LI) (SW) (MU) (ML) CIRCLE 786 Signetics Corp.

P.O. Box 3409 Sunnyvale, CA 94088-3409 (408) 991-2000 CIRCLE 787

Silicon General Inc. Semiconductor Div. 11861 Western Ave. Garden Grove, CA 92641 (714) 898-8121 (50R) (10R) (LI) (SW) (MU) (ID) (ML) (BT) (PI) (PC) CIRCLE 788

Silicon Transistor Corp.

BBF 2 Katrina Rd. Chelmsford, MA 01824 (508) 256-3321

Siliconix Inc. 2201 Laurelwood Rd. Santa Clara, CA 95054-1516 (408) 970-5697 (MF) (PI) (PC) CIRCLE 790

Sola Electric a Unit of General Signal 1717 Busse Rd. Elk Grove Village, IL 60007 (708) 439-2800 (50S) (51S) (10S) (11S) (200S) (RM) (OF) (PR) (50R) (51R) (500R) (10R) (11R) (200R)CIRCLE 791

Solidstate Controls Inc. 875 Dearborn Dr Columbus, OH 43085 (614) 846-7500 (51S) (UN) (51R) (LI) CIRCLE 792

Sorensen Co. 5555 N. Elston Ave. Chicago, IL 60630 (312) 775-0843 (50S) (51S) (500S) (11S)200S) (LA) (RM) (OF) (CV) (RP) (MD) (500R) (LI) CIRCLE 793

Speco/Emco Electronics 1172 Rt. 109 Lindenhurst, NY 11757 (516) 957-8700 (50S) (LA) **CIRCLE 794**

Spellman Electronics 7 Fairchild Ave. Plainview, NY 11803 (516) 349-8686 (500S) (10S) (11S) (200S) (LA) (RM) (CV) (RP) (500C) (10C) (11C) (DC) (MO) CIRCLE 795

Sprague Semiconductor 363 Plantation St Worcester, MA 01613 (508) 7995-1300 (BT) (PI) (PC) **CIRCLE 796**

Square D/Topaz 9192 Topaz Way San Diego, CA 92123-1165 (619) 279-0111 (11S) (200S) (UN) (11C) (200C) (AC) (11R) (200R) (SW) CIRCLE 797

Stanford Research Systems 1290 D. Reamwood Ave. Sunnyvale, CA 94089 (408) 744-9040 (500S) (LA) (RM) (CV) (RP) CIRCLE 798

Superior Electric Co. 383 Middle St. Bristol, CT 06010 (203) 582-9561

(200S) (RM) (UN) CIRCLE 799

Supertex Inc. 1225 Bordeaux Dr. Sunnyvale, CA 94088 (408) 744-0100 (MF) CIRCLE 800

Switching Power Inc.

3601 Veterans Hwy. Ronkonkoma, NY 11779 (516) 981-7231 (50S) (200S) (OF) (CV) (PF) (50C) (DC) (50R) (200R) (SW) CIRCLE 801

Switching Systems International 500 Porter Way

Placentia, CA 92670 (714) 996-0909 (50S) (200S) (OF) (PF) (50C) (11C) (DC) CIRCLE 802

TNR Technical Inc. 279 Douglas Ave. Altamonte Springs, FL 32714 (407) 682-4311 (AL) (CZ) (LC) (LT) (NC) CIRCLE 803

(see p. 116 for key) (continued on p. 116)

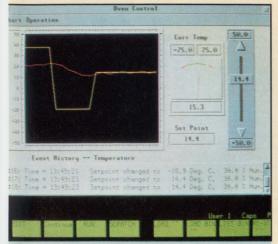
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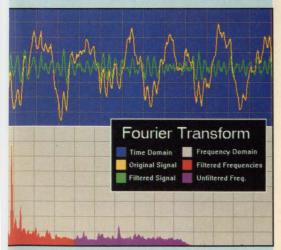
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Tadiran Electronic Industries **Batteries** Div 40 Seaview Blvd. Port Washington, NY 11050 (516) 621-4980 (AL) (LT) (SO) CIRCLE 804

Taltronics Corp. 404 Armour St., P.O. Box 339 Davidson, NC 28036 (704) 892-8872 (50S) (10S) (11S) (200S) (OF) (CV) (50C) (200C) (DC) CIRCLE 805

Tamura Corp. of America 1150 Dominguez St. Carson, CA 90746-3518 (213) 638-1790 (50S) (10S) (11S) (200S) (OF) (CV) (50C) (10C) (DC) (AC) (IC) (50R) (10R) (11R) (200R) (LI) (SW) (MU) (ID) CIRCLE 806

Tauber Electronics Inc. 4901 Morena Blvd. #314 San Diego, CA 92117 (619) 274-7242 (51S) (500S) (UN) (AL) (CZ) (LC) (LT) (ME) (NC) (NH) (NM) (SO) (ZA) (ZC) CIRCLE 807

Technology Dynamics Inc. 100 School St Bergenfield, NJ 07621 (201) 385-0500 (50S) (51S) (500S) (10S) (11S) (200S) (LA) (RM) (OF) (CV) (RP) (MD) (50C) (51C) (500C) (10C) (11C) (200C) (DC) (MO) (MI) CIRCLE 808

Teledyne Components 1300 Terra Bella Ave Mountain View, CA 94039 (415) 968-9241 (DC) (ID) (MF) (PC) **CIRCLE 809**

Teledyne Microelectronics 12964 Panama St. Los Angeles, CA 90066 (213) 822-8229 (50S) (51S) (10S) (11S) (200S) (CV) (RP) (MD) (50C) (51C) (10C) (11C) (200) (DC) (MO) (MI) (50R) (51R) (10R) (11R) (200R) (LI) (SW) (MU) (ML) CIRCLE 810

Texas Instruments Inc. 8360 LBJ Dallas, TX 75380-9066 (214) 997-5453 (50R) (10R) (11R) (LI) (SW) (ID) (ML) (BT) (PI) (PC) CIRCLE 811

Todd Products Corp. 50 Emjay Blvd. Brentwood, NY 11717 (516) 231-3366 (50S) (51S) (10S) (11S) (2005) (RM) (OF) (CV) (RP) (2005) (RM) (OF) (CV) (RP) (PF) (50C) (51C) (10C) (11C) (200C) (DC) (MO) (50R) (51R) 7 Continental Blvd.

(10R) (11R) (200R) (SW) CIRCLE 812

Toko America Inc. 1250 Feehanville Dr. Mount Prospect, IL 60056 (708) 297-0070 (50S) (10S) (11S) (RM) (OF) (CV) (PR) (50C) (10C) (11C) (DC) CIRCLE 813

Toshiba America

Electronic Components 9775 Toledo Way Irvine, CA 92718 (714) 455-2000 (BT) (MF) (RE) (TH) (PI) (PC) Phoenix, AZ 85040 CIRCLE 814

Total Power International 418 Bridge St. Lowell, MA 01850 (508) 453-7272 (50S) (10S) (11S) (200S) (RM) (OF) (50C) (11C) (DC) (AC) (MO) (IC) (50R) (10R) (11R) (LI) (SW) (MU) (ID) CIRCLE 815

Transistor Devices Inc. 85 Horsehill Rd. Cedar Knolls, NJ 07927 (201) 267-1900 (50S) (51S) (500S) (11S) (3003) (313) (3003) (113) (2003) (RM) (CV) (PR) (RP) (MD) (UN) (PF) (50C) (51C) (500C) (11C) (200C) (DC) (AC) (MO) (MI) (50R) (51R) (500R) (200R) (LI) (SW) (MU) (ML) CIRCLE 816

Tri-Mag Inc. 1601 N. Clancy Ct. Visalia, CA 93291 (209) 651-2222 (50S) (51S) (500S) (10S) (11S) (200S) (RM) (OF) (50C) (51C) (10C) (11C) (DC) (AC) (MO) (SW) CIRCLE 817

U.S. Elco Inc. 2930 Scott Blvd. Santa Clara, CA 95054 (408) 980-5144 (50S) (10S) (50C) (10C) (DC) (SW) (MU) CIRCLE 818

USSNA/U.S. Power 21517 Ocean Ave Torrance, CA 90503 (213) 316-9984 (50S) (51S) (500S) (10S) (11S) (200S) (LA) (RM) (OF) (CV) (UN) (LI) CIRCLE 819

Unipower Corp. 2981 Gateway Dr. Pompano Beach, FL 33069 (305) 974-2442 (50S) (200S) (RM) (CV) (UN) (PF) (50C) (11C) (200C) (DC) CIRCLE 820

Unitrode Integrated

Merrimack, NH 03054-0399 (603) 424-2410 (IC) (ID) (PI) (PC) CIRCLE 821

Universal Voltronics Corp. 27 Radio Circle Dr. Mount Kisco, NY 10549 (914) 241-1300 (500S) (200S) (LA) (RM) (OF) (CV) (PR) (RP) (MD) (500C) (200C) (DC) (MO) (MI) (500R) (200R) (LI) (SW) (MU) (ML) CIRCLE 822

VSR Corp. 4609 S. 33rd Pl. (602) 243-6200 (PR) (RP) (UN) (AC) CIRCLE 823

Valor Electronics 6275 Nancy Ridge Dr San Diego, CA 92121-2245 (619) 458-1471 (50C) (10C) (DC) CIRCLE 824

Varta Batteries Inc.

300 Executive Blvd. Elmsford, NY 10523-1202 (914) 592-2500 (AL) (CZ) (LC) (LT) (ME) (NC) (NM) (SO) (ZA) (ZC) CIRCLE 825

Vicor Corp. 23 Frontage Rd. Andover, MA 01810 (508) 470-2900 (50S) (51S) (11S) (200S) (RM) (MD) (PF) (50C) (51C) (10C) (11C) (200C) (DC) (MO) **CIRCLE 826**

Viking Industrial Products 729 Farm Rd. Marlboro, MA 01752 (508) 481-4600 (50S) (51S) (10S) (11S) (200S) (OF) (CV) (PR) (50C) (51C) (10C) (11C) (200C) (DC) (AC) (50R) (LI) (SW) CIRCLE 827

Viteq Corp. 10000 Aerospace Rd. Lanham, MD 20706 (301) 731-0400 (51S) (200S) (PR) CIRCLE 828

Voltex Co. Inc. 3460 Great Neck Rd. N. Amityville, NY 11701 (516) 842-2772 (50S) (51S) (500S) (10S) (11S) (200S) (RM) (OF) (CV) (RP) (50C) (51C) (500C) (10C) (11C) (200C) (DC) (MO) (50R) (51R) (500R) (10R) (11R) (200R) (LI) (SW) CIRCLE 829

Walker Scientific Inc. Walker Magnetics Group Rockdale St. Worcester, MA 01606

(508) 852-3674 (50S) (51S) (500S) (200S) (LA) (CV) CIRCLE 830

Wall Industries Inc. 5 Watson Brook Rd. Exeter, NH 03833 (800) 321-9255 (50S) (51S) (500S) (10S) (11S) (200S) (OF) (CV) (50C) (51C) (500C) (10C) (11C) (200C) (DC) (MO) (IC) (MI) CIRCLE 831

Wayne Kerr Inc. 600 West Cummings Park Woburn, MA 01801 (617) 938-8390 (50S) (51S) (10S) (11S) (200S) (LA) (RM) (OF) (CV) (RP) (MD) (UN) CIRCLE 832

Wells-Gardner Electronics 2701 N. Kildare

Chicago, IL 60639 (312) 252-8220 (50S) (51S) (OF) (CV) (50C) (51C) (50R) (51R) (SW) CIRCLE 833

Westcor Corp. 485-100 Alberto Way Los Gatos, CA 95032 (408) 395-7050 (50S) (200S) (RM) (CV) (MD) (PF) (50R) (200R) (SW) CIRCLE 834

Xentek Inc. 5501 Los Robles Laursbad, CA 92083 (619) 727-0940 (50S) (51S) (11S) (200S) (RM) (OF) (CV) (MD) (50C) (10C) (DC) (MO) (50R) (51R) (11R) (200R) (LI) (SW) (MU) (ML)

Yuasa-Exide Inc. 9728 Alburtis Ave. Santa Fe Springs, CA 90670 (213) 949-4266 (LC) (NC) CIRCLE 836

Yuasa-Exide Inc. Stationary Div. 645 Penn Ave.

CIRCLE 835

Reading, PA 19601 (215) 378-0333 (LC) (NC) CIRCLE 837

Zenith Electronics Corp. Magnetics Div. 1000 Milwaukee Ave. Glenview, IL 60021 (708) 391-8510 (50S) (51S) (11S) (200S) (OF) (CV)

CIRCLE 838

Zytronics Inc. 70 Tirrell Hill Rd. Bedford, NH 03110 (603) 623-8888 (51S) (200S) (RM) (OF) (CV) (PR) (RP) (UN) (PF) (50C) (200C) (DC) (AC) CIRCLE 839

Power Supplies Output Up to 50 V (50S) 51 to 500 V (51S)Over 500 V (500S)(10S)Up to 10 W 11 to 200 W (11S)Over 200 W (200S)Types (LA) Laboratory (RM) **Rack mounting** Open-frame OEM Constant voltage/current Precision ac output Remote programming Military designs Uninterruptible Power-factor-corrected External **Power Converters** Output (50C) Up to 50 V (51C) 51 to 500 V (500C) Over 500 V

(OF)

(CV)

(PR)

(RP)

(MD)

(UN)

(PF)

(EX)

(IC)

KEY

(10C) Up to 10 W 11 to 200 W (11C) Over 200 W (200C) Types

(DC) Dc to dc (AC) Dc to ac (AT) Ac to dc (MO) Modular IC DIP

(MI) Military designs **Power Regulators**

Output (50R) Up to 50 V 51 to 500 V (51R) (500R) Over 500 V (10R) Up to 10 W (11R)11 to 200 W (200R) Over 200 W

Types (LI) (SW) Linear Switching (MU) Modular (ID) IC DIP (ML) Military designs

Batteries

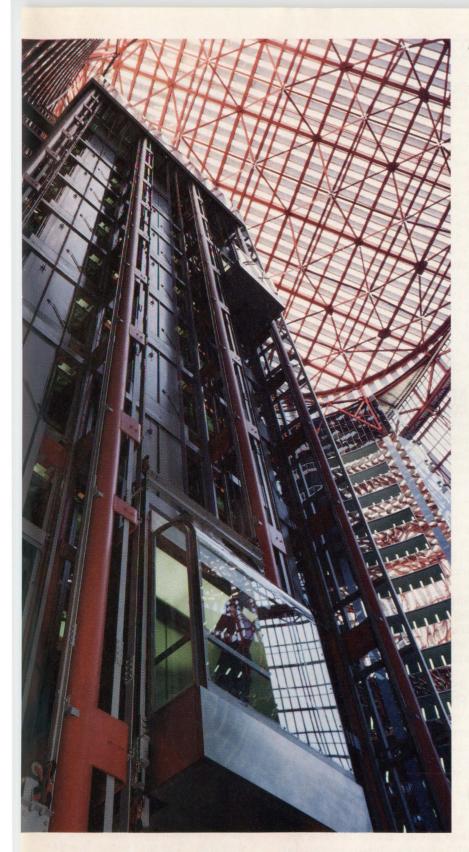
Output Alkaline (AL) (CZ) Carbon zinc (LC) Lead acid (LT) Lithium (ME) Mercury (NC) Nickel cadmium (NH) Nickel hydrogen (NM) Nickel metal hydride (SO) Silver oxide (ZA) Zinc air (ZC) Zinc chloride

Power Semiconductors Output

Bipolar transistors (BT) (ME) MOSEETS (RE) Rectifiers (TH) Thyristors (PI) Power ICs (PC) Power-control ICs

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CIRCLE 161 FOR RESPONSE OUTSIDE THE U.S.



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CONVERTERS

DC-DC UNITS OFFER ULTRA-HIGH DENSITY

Over 30 W/in.³ power density is offered by the UHD Series dc-dc converters, a tenfold improvement compared with conventional models which typically deliver 3-to-5-W densities. All models in the series measure 3.8 by 2.4 by 0.635 in. and can be plugged directly into pc boards. Output options are 3.3, 5, 6, 12, 15, 24, and 28 V dc. The single-output units in parallel or current-sharing modes. Pricing starts at \$139 in lots of 250. Call for delivery.

Lambda Electronics 515 Broad Hollow Rd. Melville, NY 11747 (516) 694-4200 ▶ CIRCLE 863

STANDARD CONVERTERS COME FROM CUSTOM HOUSE

Long known for its custom dc-dc converters, Shindengen America is now rolling out a line of standard dc-dc products. The family includes both high- and low-power models. There's 1-, 2-, and 3-W units for small distributed-power tasks and analog-digital conversion circuits, mid-level 5-to-50-W models for telecommunications, and 100-to-150-W units for computer applications. Call for pricing and delivery.

Shindengen America Inc. 2649 Townsgate Rd., Suite 200 Westlake Village, CA 91361 (800) 634-3654 ► CIRCLE 864

RECORD QUIET LEVEL FOR DC-DC CONVERTER

The military's MIL-STD-461C CE03 conducted-emission standard is met without external components by the MQO Series dc-dc converters. The 16.5-W, board-mountable units integrate four individual outputs, an EMI filter, and a user-programmable hold-up function that protects against power failure. The independently regulated outputs are rated at +5, -5, and either ± 12 or ± 15 V dc from a 28-V input bus. Availability is scheduled for the first quarter of 1992. Call for pricing.

Interpoint Corp. P.O. Box 97005 Redmond, WA 98073-9705 (206) 882-3100 ► CIRCLE 865

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▼ UP TO 1000 V POUR FROM TINY CONVERTER

Up to 1000 V dc output is available from the 0.5-in.-tall Series AV dc-dc converter. The 36-model series delivers 1.25 W at 70°C ambient temperatures. Input voltages are 5, 12, 24, and 28 V dc. Input-to-output isolation is 100 M Ω at 1000 and 1500 V dc. The series comes in an ultra-miniature encapsulated package that weighs just 4 grams. Call for pricing and delivery.

Pico Electronics Inc. 453 N. MacQuesten Pkwy. Mount Vernon, NY 10552 (800) 431-1064 ► CIRCLE 866

LOW-VOLTAGE MODULES OFFER TIGHT REGULATION

A line of low-voltage power modules offer system designers power-conservation solutions in a range of computer, telecom, and industrial applications. The MH Series operates from inputs of 4.5 to 5.5 V. The MA Series accepts from 10 to 14 V. Both series have maximum power ratings of 5 and 10 W and offer precisely regulated dc outputs at high efficiencies. Full input-to-output isolation permits polarity versatility. The 5- and 10-W models cost \$39 and \$45, respectively, for 500 pieces. Delivery is from stock.

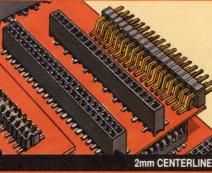
AT&T Microelectronics Dept. 52AL040420 555 Union Blvd. Allentown, PA 18103 (800) 372-2447 ► CIRCLE 867

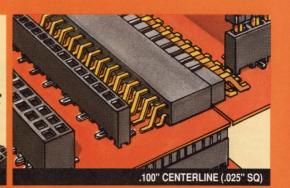
▼ DIP DC-DC CONVERTER POWERS ETHERNET LANS

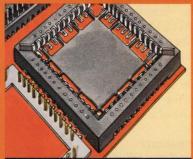
The LPR3XX Power Convertible series is specifically designed for highvolume, low-cost local-area-network applications and provides isolated power for LAN-transceiver devices. The series operates from inputs of 5 or 12 V dc and supplies an isolated –9-V dc output. The unit comes in a 24pin DIP for upgrading of existing systems. Pricing is \$6.40 in lots of 1000. Delivery is from stock to four weeks.

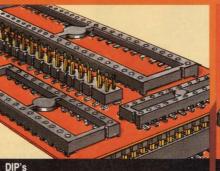
Burr-Brown Corp. P.O. Box 11400 Tucson, AZ 85734 (800) 548-6132 ► CIRCLE 868













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REGULATORS & POWER ICS

LAPTOP LOAD SWITCH TAKES LOGIC SIGNALS

A logic-level load switch overcomes the problems of high-side load switching in portable computers. The Si9405DY comes in an SO-8 package for use in space-limited laptop and notebook machines. It doesn't

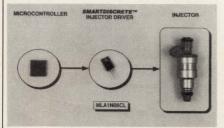


require the extra drive circuitry typical of n-channel high-side switches and has an extremely low on-resistance $(0.12 \ \Omega)$ even when operating from logic signals. The low on-resistance means more power is available to the load. Pricing is \$0.95 in large OEM quantities. Samples are available now with production quantities in eight to 12 weeks.

Siliconix Inc. 2201 Laurelwood Rd. Santa Clara, CA 95054 (800) 554-5565, ext. 1400 ▶ CIRCLE 869

SMART POWER MOSFETs OFFER VOLTAGE CLAMPING

Voltage-clamping capability is now available in the MLP1N06CL and MLA1N06CL logic-level MOSFETs. The SmartDiscrete monolithic TMOS devices have integrated onchip current limiting, drain-to-source



voltage clamping, and gate-voltage protection. The voltage-clamping capability protects the device against unclamped inductive-switching transients and overvoltage-stress conditions. Pricing starts at \$1.48 in lots of 1000. Samples and small quantities are from stock.

Motorola Inc. 5005 E. McDowell Rd. Phoenix, AZ 85008 (602) 244-3370 ► CIRCLE 870

MONOLITHIC MOSFET IS FULLY PROTECTED

The industry's first monolithic, fully protected MOSFET provides temperature and short-circuit protection using n-channel, enhancement-mode DMOS technology. The TOPFET's integrated design eliminates the need for external components as it guards against junction temperatures above 150°C, shorts, overvoltage for repetitive switching of inductive loads, input ESD problems, and reverse-battery situations. A 50-m Ω unit is available now with others by the second quarter of 1992. Pricing is about \$2.25 in lots of 1000. Delivery is in 12 to 16 weeks.

Philips Components 2001 W. Blue Heron Blvd. Riviera Beach, FL 33404 (800) 447-3762 ► CIRCLE 871

BATTERY-CHARGER ICs FAILSAFE NICAD USE

Nickel cadmium and nickel metal hydride batteries can be charged with no risk of overcharge and potential explosion with the TC675 and TC676 smart battery-charger ICs. The charge cycle ends in one of two ways: an external thermistor input stops it when a selected battery-temperature rise is achieved, or a built-in timer limits charging time to 90 minutes. Packaging is in 14-pin DIPs, 14-pin ceramic DIPs, and 16-pin (wide) small-outline ICs. Pricing is \$7 in lots of 10,000. Samples are available from stock.

Teledyne Components P.O. Box 7267

Mountain View, CA 94039-7267 (415) 968-9241 ▶ CIRCLE 872

▼ IC CONTROLS UP TO FOUR POWER SUPPLIES

A four-channel, switching-regulator control IC is capable of independently controlling up to four power supplies. The MB3785 IC is targeted for use in portable devices such as notebook computers and camcorders. Each of the four channels uses pulsewidth-modulation control circuitry to ensure $\pm 1\%$ regulation and accuracy. Each channel also operates at a maximum frequency of 1 MHz. The 48-pin quad flat pack device goes for \$2.99 in lots of 1000. Samples are

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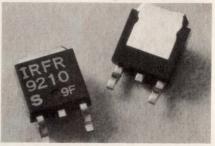


from stock.

Fujitsu Microelectronics Inc. Integrated Circuits Div. 3545 N. First St. San Jose, CA 95134-1804 (800) 642-7616 ► CIRCLE 873

SWITCHING REGULATOR RUNS AS DC-DC CONVERTER

A monolithic, bipolar switching-regulator subsystem IC intended for use as a dc-dc converter is available. The KA34063AN device integrates a temperature-compensated bandgap reference, a comparator, a con-



trolled-duty-cycle oscillator with an active peak-current limit circuit, a driver, and a high-current output switch. The device operates from a 3to-40-V input and has an outputswitch current of up to 1.5 A. Pricing is \$0.65 in lots of 1000.

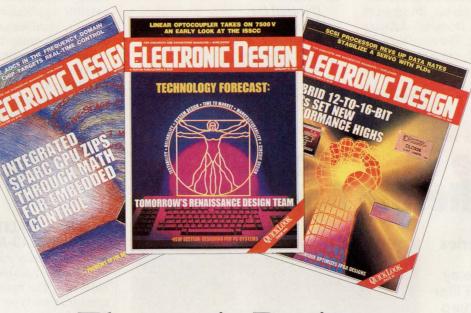
Samsung Semiconductor 3725 N. First St. San Jose, CA 95134-1708 (800) 423-7364 ► CIRCLE 874

▼ PWM-CONTROL IC OPERATES AT 100 MHZ

A phase-shifted, pulse-width-modulation (PWM) control IC combines the advantages of resonant and PWM control for switching power supplies. The UC3875 controllers implement control of a bridge power stage by phase shifting the switching of one half-bridge with respect to the other. This allows constant-frequency PWM in combination with resonant, zero-voltage switching for high efficiency at high frequencies. In lots of 1000, the commercial grade UC3875N goes for \$4.50. Small quantities are delivered from stock.

Unitrode Integrated Circuits Corp. P.O. Box 399 Merrimack, NH 03054-0399 (603) 424-2410 ► CIRCLE 875

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BATTERIES

▼ REPLACEABLE BATTERIES MEAN USER CONVENIENCE

When Fujitsu Network Transmission wanted to enhance the convenience of using its Pocket Commander Stylus cellular phone, it turned to user-replaceable Duracell AA-size alkaline batteries. The alkaline cells make the unit truly portable and free users from the burden of carrying spare battery packs. Talk time with the alkaline cells (80 minutes) is comparable to that of standard rechargeable cells. Call for volume pricing and delivery.

Duracell Inc.

Berkshire Industrial Park Bethel, CT 06801 (800) 431-2656 ▶ CIRCLE 876

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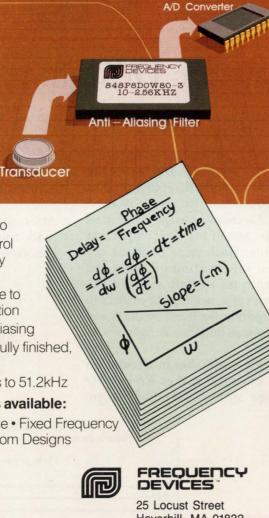
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CIRCLE 112 FOR U.S. RESPONSE (8 CIRCLE 113 FOR RESPONSE OUTSIDE THE U.S. ELECTRONIC DESIGN = PIPS SPECIAL EDITORIAL FEATURE = JANUARY 23, 1992

NI-H₂ BATTERIES FIT SMALL-SAT TASKS

A scaled-down version of proven nickel-hydrogen space-battery technology has been developed for smallsatellite applications. The small-diameter, small-capacity (2 to 20 Ah) cells incorporate the same electrochemical components as the flightproven hardware. These cells displace non-avionic products that have been used in lieu of a better solution. Call for pricing and delivery.

Eagle-Picher Industries Inc. Electronics Div. P.O. Box 47 Joplin, MO 64802-0047 (417) 623-8000 ► CIRCLE 877

▼ HIGH-CAPACITY MODEL JOINS LEAD-ACID LINE

A high-capacity model has joined a line of rechargeable, sealed lead-acid batteries. The maintenance-free, recombination-type battery delivers 3.25 A for 20 hours, which represents an energy density of 1.26 W-Hrs/ in.³. The low 9-m Ω internal resistance yields discharge currents of up to 195 A for 5 minutes and up to 650 A for short periods. Both deep-cycle use and standby service in back-up systems are possible. Call for pricing and delivery.

Power-Šonic Corp. P.O. Box 5242 Redwood City, CA 94063 (415) 364-5001 ► CIRCLE 878

COMPUTER BATTERY OFFERS HIGH CAPACITY

Capacity of 150% compared with competitive batteries is offered by the DL2/3ASE-F2X computer realtime clock and memory backup battery. The cell is designed to offer more than five years of service under typical usage conditions. Output is 6.4 V dc with a 1.8-Ah current capacity at 70°F. A peel-and-stick adhesive fastener makes for easy mounting within IBM XT and AT computers and clones. The two-lithium-battery assembly goes for \$8.50 in lots of 100. Call for delivery.

Tauber Electronics Inc. 4901 Morena Blvd., Suite 314 San Diego, CA 92117 (800) 829-4747 ► CIRCLE 879

BATTERIES

▼ TWO-CELL LITHIUM BATTERY BACKS UP COMPUTER MEMORIES

A two-cell encapsulated lithium battery is available for computer-backup applications. The 2ER6K batteries offer a 1900-mAh capacity and come in 6.8- (containing resistor and diode) and 7.2-V (diode-only) formats. The cells can be customized with various lead-wire connector configurations as well as with different values of resistors and diodes. Call for pricing and delivery.

Maxell Corp. of America 22-08 Route 208 Fair Lawn, NJ 07410 (201) 796-8790 ▶ CIRCLE 880

RECHARGEABLE LAPTOP, PHONE CELLS BOOST RUN TIMES BY UP TO 70%

The Ultramax line of rechargeable nickel cadmium batteries increase run times as much as 50 to 70% in products such as cellular phones and portable computers. The family includes AA cells with 800-mAh capacity, 2/3A cells at 600 mAh, Cs size at 1800 mAh, and D cells at 5000 mAh, to name a few. All cells accept 3-to-5-hour quick charging and 1-hour fast charging. Samples are available now. Call for pricing and delivery.

Gates Energy Products Inc. Inquiry Fulfillment Dept. P.O. Box 667850 Charlotte, NC 28266-9961 (800) 67-POWER ► CIRCLE 881

▼ LEAD-ACID CELLS' CONSTRUCTION MEANS IMPROVED CAPACITY BY 10%

Thanks to construction improvements, three sealed leadacid batteries offer 10% more capacity than earlier models in the same form factors. The 6-V, 12-Ah LCR6V12P supports high discharge rates in UPS and emergencylighting systems. The 6-V, 7.2-Ah LCR6V7.2P and the 12-V, 7.2-Ah LCR12V7.2P fill both of those applications and add engine-start tasks. Delivery is in 10 to 12 weeks.

Panasonic Industrial Co. OEM Battery Sales Group Two Panasonic Way Secaucus, NJ 07094 (201) 348-5266 ► CIRCLE 882

9-V, 950-MAH LITHIUM BATTERY LASTS 10 YEARS IN BACKUP ROLE

A life expectancy of up to 10 years is predicted for the model CR 9-V lithium battery. The manganese dioxide battery offers 950-mAh capacity and is built from cells with 25% more energy density than conventionally built LiMnO² cells. Applications include memory backup, instruments, and remote controls. Pricing is \$9.99 for lots up to 1000. Delivery is in three to five weeks.

Varta Batteries Inc. 300 Executive Blvd. Elmsford, NY 10523 (914) 592-2500 ▶ CIRCLE 883

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INTERCONNECTIONS

HIGH-SPEED CONNECTOR **KEEPS CROSSTALK LOW**

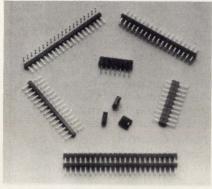


The Quiet Zone SC modular coaxial cable assemblies offer the highest signal fidelity available in 0.025-in. square post packages. Over 90% V_p signal speeds and 0.5% crosstalk at sub-nanosecond rise times is featured. A patented 360° shielding technique completely shields the signal line, both within the cable and through the connector. This keeps insertion loss to around 2 dB at 1 GHz for 10-ft lengths. Call for pricing.

W.L. Gore & Associates 555 Paper Mill Rd. Newark, DE 19714 (800) 638-7775 ► CIRCLE 884

2-MM PCB CONNECTORS **REPLACE 0.100-IN. TYPES**

A line of 2-mm interconnects are exact replacements for standard 0.100in. center types. The smaller 2-mm units (0.79-in. centers) do not change



any pc-board layout parameters. The header, socket, and shunt versions of these units have been tooled to accommodate the new design. Singleand double-row configurations are available. Volume pricing is \$0.02 per contact. Small quantities are delivered from stock.

Comm Com Connectors Inc. 4111 Ocean View Blvd. Montrose, CA 91020 (818) 957-2018 ► CIRCLE 885

V ONE-PIECE CONNECTOR LINKS FIBER OPTICS

Fewer parts in the 308 Series SC fiber-optic connectors means simple field or factory termination in less time. The single-mode connector's grip has a posi-latch action for en-



hanced mating retention. Zirconia or alumina-ceramic ferrules are available configured for PC polishing. Call for pricing and delivery.

Methode Electronics Inc. Fiber Optic Products Div. 7444 W. Wilson Ave. Chicago, IL 60656 (800) 323-6858 ► CIRCLE 886

FINE-PITCH IDCs SAVE SPACE IN SYSTEMS

The reliability of mass termination combines with the space savings of a 0.050-by-0.100-in. mating interface in the System 311 fine-pitch IDC interconnects. The female socket features a dual-beam coined contact that increases reliability. The male header features vertical lock and eject configuration. Call for pricing and delivery.

Thomas & Betts Corp. Electronics Div. P.O. Box 24901 Greenville, SC 29616-2401 (800) 344-4744 ► CIRCLE 887

TWO HEADER VERSIONS HAVE BREAK-AWAY KEYS

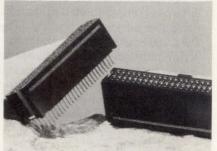
Both shielded and unshielded versions of the Durabak headers feature break-away keys in four- and five-key schemes. The units mate with 0.100-by-0.100-in. receptacle connectors, including AMP-Latch cable connectors. Riveted top-release latches provide superior retention and strength. Call for pricing and delivery.

AMP Inc. P.O. Box 3608 Harrisburg, PA 17105-3608 (800) 522-6752 ► CIRCLE 888

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IDC CABLE ASSEMBLIES OFFER 0.050-IN. CENTERS

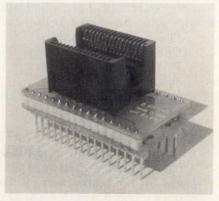


A micro IDC system for mating with terminal strips on 0.050-by-0.100-in. centers is available. Socket (female) strips in the FCSD Series feature a dual-beam, tuning-fork-style BeCu contact. Terminal (male) strips in the FCMD Series also feature BeCu contacts. Both male and female strips come in from five to 40 positions per row. Each three-prong contact makes two gas-tight links with each wire. Pricing starts at \$0.06 per contact. Delivery is in two weeks.

Samtec Inc. P.O. Box 1147 New Albany, IN 47151-1147 (800) SAMTEC-9 ► CIRCLE 889

PROGRAMMING CONVERTER TURNS SOJ INTO DIP

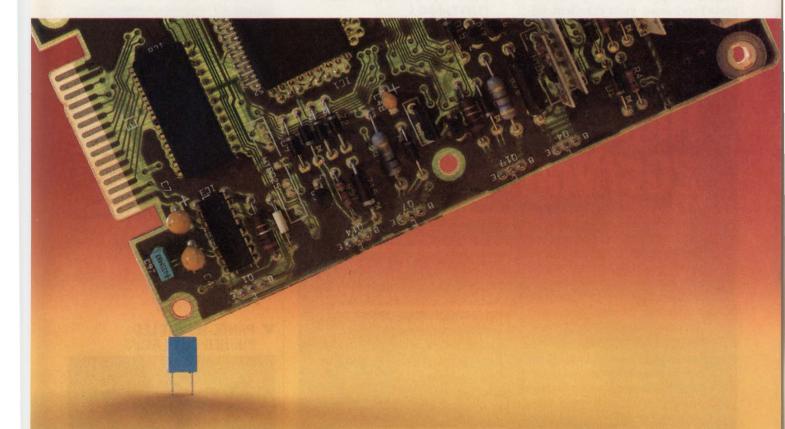
The 32SJ4/D6 programming converter accepts a device packaged in a 32-pin, 50-mil-pitch, 400-mil-wide SOJ package and changes its footprint to a 100-mil DIP for insertion into a pro-



grammer's socket. The converters can also be used directly on prototyping boards. Unit price is \$85. Delivery is from stock.

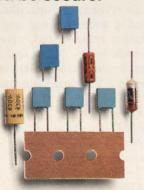
EDI Corp. P.O. Box 366 Patterson, CA 95363 (209) 892-3270 ► CIRCLE 890





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PASSIVES

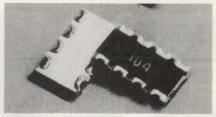
MILITARY-TYPE CAPS JOIN CERAMIC TRIMMERS

Military-type 7-by-9-mm models have been added to a line of ceramicdielectric trimmer capacitors. The GKBxxx31 and GKBxxx37 units are offered in seven capacitance ranges from 2 to 8 pF to 7 to 70 pF. Silverplated terminals yield excellent solderability, while phosphor-bronze rotor terminals provide maximum durability. Prices start at \$0.75 in lots of 1000. Delivery is stock to eight weeks.

Sprague-Goodman Electronics Inc. 134 Fulton Ave. Garden City Park, NY 11040 (516) 746-1385 ▶ CIRCLE 891

SMT RESISTOR NETWORKS ARE THERMALLY STABLE

Temperature coefficients of better than ± 200 ppm/°C are offered by two families of surface-mounted arrays and networks for terminating and decoupling ECL circuitry. The CRM Series thick-film resistor ar-



rays are comparable in size to discrete 1/8-W resistors. The MRGF Series resistor networks come in 16-pin SOIC packages in values from 33 Ω to 2.2 M Ω . Pricing in lots of 10,000 starts at \$0.80 for the CRM Series and \$0.30 for the MRGF Series. Delivery is in eight weeks.

Raltron Electronics Corp. 2315 N.W. 107th Ave. Miami, FL 33182 (305) 593-6033 ▶ CIRCLE 892

PANEL-MOUNT LED PUSHES OUT LAMPS



The first true LED version of an 11/ 16-in. incandescent lamp for panel mounting is represented by the Series 557 super-bright LED array. The unit offers the light intensity of incandescents and the long life of LEDs. Multiple-LED construction and a proprietary lens design result in high-tech styling, uniform illumination, and a wide viewing angle. The indicators come in red, green, and amber and in 4.3-, 5-, 12-, and 28-V versions. A bicolor (red-green) version comes in 5 V. Pricing is around \$4 in lots of 1000.

Dialight Corp. Dept. P557 1913 Atlantic Ave. Manasquan, NJ 08736 (908) 223-9400 ▶ CIRCLE 893

High Voltage 20¢/Volt

The PS300 programmable power supply series provides up to 5kV at 25 Watts for laboratory and ATE applications. These supplies offer a wide range of features including programmable current and voltage limits, selectable overload response, and short circuit protection.

Dual LED displays monitor both output current and voltage, while a third display allows error-free front panel entry. A full GPIB interface is available for ATE systems.

The combination of features, price, and performance make the PS300 series the perfect choice for laboratory or systems use.

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PS325	0 to 2.5kV
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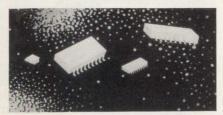
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SMT TERMINATOR NETWORKS **AID 4-MBIT DRAM USERS**

A solution to the challenge of memory-damping applications with 4-Mbit DRAMs is offered by the 4800P Series of terminator networks. Rather than using discrete chip resistors,



which eat up board space, the 4800P networks cut board-space requirements by more than 50%. The gullwing devices mount on 0.350-in.-wide land patterns. Call for pricing. Delivery of samples is in eight weeks.

Bourns Networks Inc. 1400 North 1000 West Logan, UT 84321 (801) 750-7200 ► CIRCLE 894

MINI SMD OSCILLATOR **OFFER HCMOS TECHNOLOGY**

The MM Series of quartz-crystal oscillators offer HCMOS technology and an AT-strip crystal in a miniature, ceramic surface-mounted package. The unit's output is TTL/ HCMOS-compatible from 1.5 to 40 MHz (A version) and HCMOS-compatible from 40.1 to 60 MHz (G version). Tristate output is optional in both versions. Call for pricing and delivery.

M-tron Industries Inc. P.O. Box 630 Yankton, SD 57078 (800) 762-8800 ► CIRCLE 895

BRIGHT LED CLUSTERS LIGHT UP DISPLAY BOARDS

A line of multicolored LED clusters is available for use in outdoor display boards. The units, which are clearly readable in daylight from up to 1/3of a mile, are contained within a rainwater-proof structure and feature a wide viewing angle, low power consumption, and freedom from maintenance. Call for pricing and delivery.

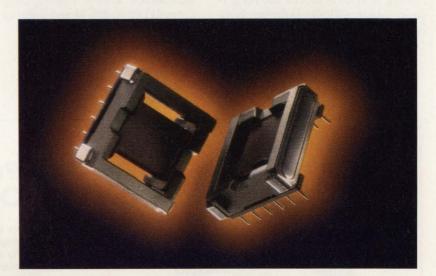
II Stanley Co. Inc. 2661 Gates Ave. Irvine, CA 92714 (800) LED-LCD1 ► CIRCLE 896

STRINGS OF BRIGHT LEDS **GIVE LIGHT BY THE INCH**

A string of tiny, closely spaced bright LEDs is surface-mounted on a thin, extremely flexible 0.23-in.-wide plastic strip. The Striplight LED product is made up of continuous chains of low-profile, 1.5-in. segments. Each segment contains five LEDs wired in series (segments are in parallel) and spaced on 0.27-in. centers. A 6-in. Striplight can be bent into a 3-in.-diameter circle or twisted 360° across its length. Call for samples, pricing, and delivery.

Ledtronics Inc. 4009 Pacific Coast Hwy. Torrance, CA 90505 (213) 549-9995 ► CIRCLE 897

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SCI-1014

CIRCLE 166 FOR U.S. RESPONSE **CIRCLE 167 FOR RESPONSE OUTSIDE THE U.S.**

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SWITCHES & RELAYS

1/2-IN. ROTARY SWITCH CUTS INSTALLED COST



A 1.2-in.-diameter rotary switch is capable of withstanding wave soldering and board-cleaning techniques. The slight premium for the Series 50/51T switch is more than offset by the savings in assembly costs. Solder-lug terminals and water-tight panel seals are optional. Pricing is \$7.50 in lots of 100 for a 1deck, 1-pole switch. Delivery is in four weeks.

Grayhill Inc. P.O. Box 10373 LaGrange, IL 60525 (708) 354-1040 ► CIRCLE 898

SEALED TOGGLE SWITCH TAKES TOUGH CONDITIONS

Designed to meet severe-environment application needs, the NT Series toggle switch features moldedin elastomer seals from lever to bushing and cover to case. Options include one-, two-, or four-pole cir-



cuitry; screw, quick-connect, or solder terminations; and momentary or maintained action. Pricing ranges from \$11.59 to \$26.44 and delivery is in four to six weeks.

Micro Switch 11 W. Spring St. Freeport, IL 61032 (815) 235-6600 ▶ CIRCLE 899

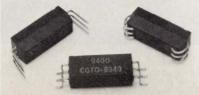
SUBMINI SMD RELAY SIPS POWER SLOWLY



With 140 mW of nominal power consumption, the G6H-2F submini surface-mounted relay needs less power to energize than earlier models. The 2 Form C unit comes in coil voltages of 3, 5, 6, 9, 12, and 24 V dc and can switch up to 1 A. It also conforms to FCC Part 68 surge-withstand requirements of 1.5 kV. List price is \$2.45 in lots of 1000.

Omron Electronics Inc. One E. Commerce Dr. Schaumburg, IL 60173 (708) 843-7900 ► CIRCLE 900

2 GHz Micro Miniature Reed Relays (0.255"W x 0.550"L)



Coto Wabash's 9400 Series surface mount package offers you the world's most compact reed relay package currently available. A 50 Ω coaxial shield makes this relay suitable for switching applications up to 2 GHz. The 9400 Series offers very low capacitance, excellent RF Characteristics, and is available with "J", Gull, Axial, or Radial Leads. The thermoset epoxy package withstands 430°F reflow soldering which makes this relay compatible with surface mounting manufacturing techniques. Call or write to us today for a free full line "Partners is Design" catalog.

COTO WABASH

A Kearney-National Company 55 Dupont Drive, Providence, R.I. 02907 Tel: (401) 943-2686 Fax: (401) 942-0920

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"Trade shows are valuable, but I learn more from my industry publications."

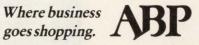
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For a free copy of the study, please write to American Business Press, 675 Third Avenue, Suite 400, New York, NY 10017.

Where business



SWITCHES & RELAYS

SOLID-STATE RELAYS SUIT 150/270 V DC TASKS

Designed specifically for power control and switching applications, the RD and VD families of solid-state power controllers are designed for 150/270-V dc applications. Optical isolation between load and control protects the control circuit from load-side surges and transients. The relays are available with W- or Y-level screening per MIL-R-28750. Volume pricing starts at \$370. Prototype quantities are available from stock to 14 weeks.

Teledyne Solid State 12525 Daphne Ave. Hawthorne, CA 90250 (213) 777-0077 ► CIRCLE 901

TELECOM RELAY MEETS BELLCORE SPECS

The Bellcore specification requiring 2500-V surge isolation for telecommunication relays is met by the FBR12 relay. With dimensions of 10 mm high by 7.5 mm wide by 15 mm

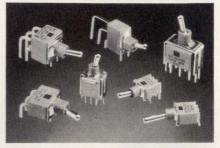


long, the unit offers a 43% size reduction in pc-board area compared with earlier telecom relays. Coil power has also been reduced to 140 mW compared with the typical range of 200 to 500 mW. Maximum switching voltage for the 12-pin DIP unit is 150 V dc and 125 V ac. Maximum current is 1 A. List price is \$6. Volume production is scheduled for the first quarter.

Fujitsu Microelectronics Inc. 3545 N. First St. San Jose, CA 95134-1804 (408) 922-9000 ► CIRCLE 902

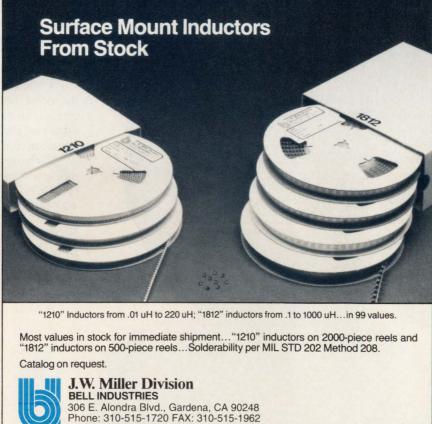
SEALED TOGGLE SWITCH DISSIPATES ESD TO 20 KV

Conductive-plastic actuator bushings enable the E and ET Series sealed toggle switches to dissipate up to 20 kV of ESD from the toggle actuator to ground before any measurable current shows up at the ter-



minals. A variety of configurations include 18 pc-mounted styles; miniature and submini sizes; eight switching functions; and up to 3 poles. Prices start at \$4.38 in lots of 1000.

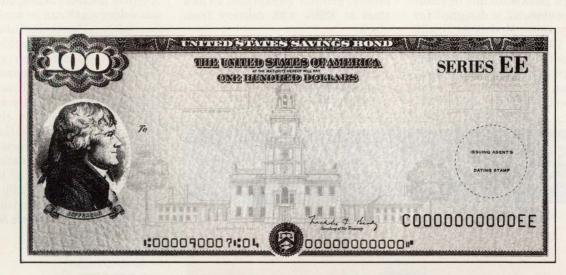
C&K Components Inc. 15 Riverdale Ave. Newton, MA 02158-1082 (617) 964-6400 ► CIRCLE 903



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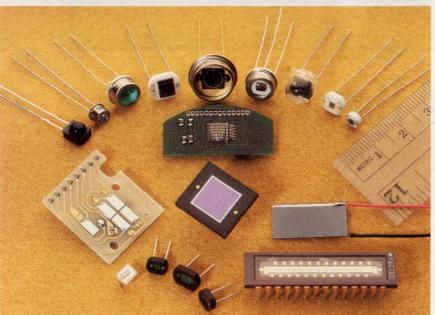
PACKAGING & MATERIALS

COMPUTER ENCLOSURES HOLD SUN SYSTEMS

The Omega DeskMate line of floorstanding enclosures is designed for Sun-bus systems. Models 8, 10, and 14 offer 8, 10, and 14 slots (9U by 400 mm), respectively. All three systems include card cages, backplanes, power supplies, wiring, and an engineered cooling system. Each features a quiet, 10-layer VME monolithic J1/J2 backplane as well as a J3 power/ground backplane. Prices start at \$2995 with delivery from stock.

Electronic Solutions 6790 Flanders Dr. San Diego, CA 92121 (800) 854-7086 ▶ CIRCLE 904





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Call or write for new catalog: EG&G Vactec, Inc. 10900 Page Blvd. St. Louis, MO 63132 (314) 423-4900 TWX 910-764-0811 FAX 314-423-3956

▼ LIQUID SOLDER MASK OFFERS HIGH RESOLUTION

A liquid, photodefinable, fully aqueous solder mask can be applied with conventional screen-printing techniques. The PC 801 solder mask achieves high definition and complete encapsulation of dense circuits. The single-part, epoxy-based photopolymer system is for use over bare copper and tin-lead. It eliminates voids, adhesion loss, and the brittleness of dry films. The mask's flow characteristics mean coating flexibility for a wide range of board-design techniques, especially in SMT types. Call for pricing and delivery.

AMP-AZKÔ Electronic Materials 710 Dawson Dr. Newark, DE 19713 (302) 292-6246 ▶ CIRCLE 905

AQUEOUS SOLDER MASK IS PROCESSED EASILY

The Hysol SR8100 liquid photoimageable solder mask offers consistent high adhesion and hardness through any number of soldering processes. The acrylate-epoxy-based liquid is intended for use as a permanent solder resist coating on high-density, copper printed-wiring boards. It consists of two components which are mixed in ratio to yield the working compound. Features include elimination of solder balling. Call for pricing and delivery.

Dexter Electronic Materials 15051 E. Don Julian Rd. Industry, CA 91746 (818) 968-6511 ► CIRCLE 906

▼ FREE-STANDING ENCLOSURE BOASTS STAINLESS FINISH

The ES 5000 enclosure, already endowed with high-impact resistance, now offers corrosion protection thanks to a stainless-steel finish. The finish on the housing, door, and rear panel functions as a no-maintenance, lifetime barrier against corrosion. Electrical and control components are protected by the unit's 10-fold metal profile. Call for pricing and delivery.

Rittal Corp. 3100 Upper Valley Pike Springfield, OH 45504 (800) 477-4000 ► CIRCLE 907

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ELECTRONIC DESIGN = PIPS SPECIAL EDITORIAL FEATURE = JANUARY 23, 1992

132

DC-DC CONVERTERS SPAN WIDE POWER RANGE

A 20-page catalog of a standard line of dc-dc converters neatly divides the line in terms of power-output level and explains the products in detail. Sections describe converters ranging in power from 1 W to 150 W. Complete tables of specifications, mechanical diagrams, and ordering information are included. A section on application considerations accounts for fusing and thermal conditions.

Shindengen America Inc. 2649 Townsgate Rd., Suite 200 Westlake Village, CA 91361 (800) 634-3654 ► CIRCLE 908

LITHIUM-BATTERY GUIDE COVERS CELL SELECTION

Battery types and selection, calculation of battery life, performance characteristics, product specifications, and battery-handling procedures are all covered in a lithium product guide. A tear-out worksheet can be used to relay your lithium-battery requirements to the company's technical-support team, who will recommend an optimal selection.

Rayovac

601 Rayovac Dr. Madison, WI 53711 (608) 275-4694 ▶ CIRCLE 909

▼ LED-INDICATOR GUIDE HELPS GET PANELS LIT

Featuring 75 new indicators, an eight-page guide to LED panelmount indicators addresses a broad range of industrial and consumer applications that require design flexibility. Exact measurements and dimensions along with helpful charts and photos assist in ordering panelmount and snap-in-mount indicators.

Dialight Corp. Dept. PMIL 59110 1913 Atlantic Ave. Manasquan, NJ 08736 (908) 223-9400 ► CIRCLE 910

WIRE-HANDLING CATALOG HELPS NEATEN PACKAGING

Non-wire products for interconnection needs are grouped into six distinct families in a wire-management catalog. The 180-page catalog covers harnessing, shielding, handling, connecting, identifying, and routing of wire and enables users to spec a complete line of applicable products for each category. Extensive cross-referencing is included.

NEW LITERATURE

Alpha Wire Corp. 711 Lidgerwood Ave. P.O. Box 711 Elizabeth, NJ 07207-0711 (800) 52-ALPHA ▶ CIRCLE 911

208-PAGE CATALOG COVERS MANY SUPPLIES

One of the industry's broadest power-supply selections is covered in detail in Lambda's 1992 catalog. Ac-dc switching and linear units, dc-dc converters, and test and lab-bench supplies are illustrated and described in full. Industrial, commercial, and MIL-type supplies are included. Mechanical drawings for all types are found in a large section.

Lambda Electronics Inc. 515 Broad Hollow Rd. Melville, NY 11747-3700 (516) 694-4200 ► CIRCLE 912

SHORT-FORM CATALOG OUTLINES SWITCHERS

A full range of encapsulated switchers, open-frame supplies, and dc-dc converters is covered in a 16-page short-form catalog. Eight new series are included in the booklet. Specifications for all products include input and output voltages, output current, and case styles. Dimensional drawings are included.

Power General P.O. Box 189 Canton, MA 02021-3798 (617) 828-6216 ▶ CIRCLE 913

▼ 906-PAGE DATA BOOK BRIMS WITH DISCRETES

Hundreds of npn power transistors and n- and p-channel power MOS-FETs are described in detail in a 906page data book. Complete specifications are included for each device. The book also covers a wide range of linear ICs as well as ICs for graphics applications.

Samsung Semiconductor Inc. 3725 N. First St. San Jose, CA 95134 (800) 423-7364 ▶ CIRCLE 914

Spectrol's Model 63 Available in 12 Different Models



Spectrol's 3/8-inch square single-turn cermet trimmer, the Model 63 is offered in four terminal styles with pin configurations to suit any standard PCB application as well as two top-adjust and two side-adjust versions, and two different knob types. Quick adjustment is achieved with a multi-fingered wiper. Resistance range is from 10 ohms to 2 megohms with a \pm 10% resistance tolerance. Features include improved solder-plated terminals, and an "0" ring seal for solvent and aqueous washing. Tempco is 100 ppm/°C, and a CRV of 2% or 2 ohm. The Model 63 continues to provide excellent performance as the industry standard across a broad spectrum of applications.



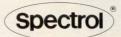
Spectrol Electronics Corporation 4051 Greystone Drive, Ontario, CA 91761 Phone: (714) 923-3313 Fax: (714) 923-6765 CIRCLE 144 FOR U.S. RESPONSE

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CYM6001K Uniprocesson SPARCore Module



CYM6002K Dual Processon SPARCore Module



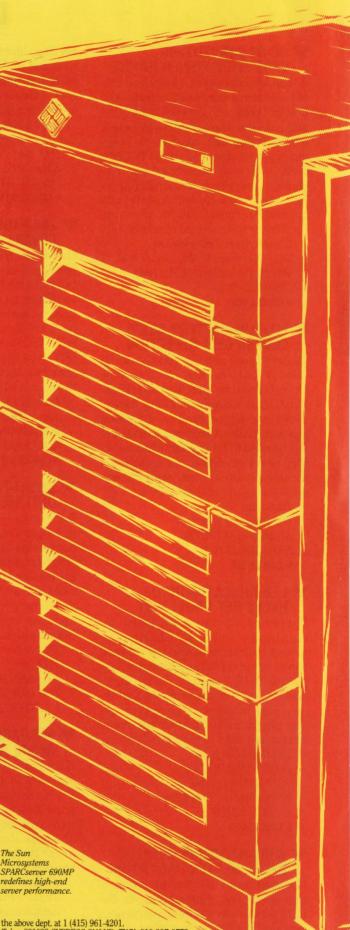
CYM6003K Uniprocesso SPARCore Module for Multiprocessing systems





The Sun Microsystems SPARCserver 690MF redefines high-end

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PRODUCT INNOVATION

Enhanced Epides Tackle Tackle Tophysics Tophysics Epidemic Systems Programmable Logic Devices Also Deliver Top I/O.



DAVE BURSKY

lthough density levels for UV-EPROM-based programmable logic devices (EPLDs) are now exceeding 7000 gates, many applications can utilize only 50% of the available gate count. For designers who need fast a

turnaround time, the flexible architectures of antifuse or RAM-based programmable gate arrays are two alternatives to EPLDs. To curb potential designer defections to these other technologies, as well as attract new users, San Jose, Calif.-based Altera Corp. has developed the MAX 7000 EPLD family of high-gate-count, high-I/O-count EPROM- and EEPROM-based fieldprogrammable logic.

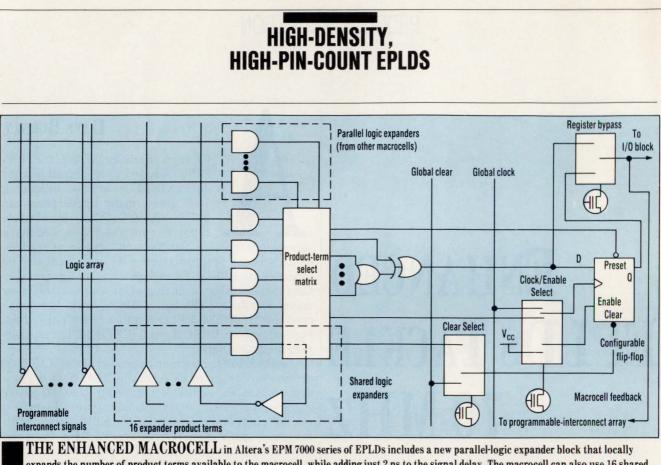
The MAX 7000 series is an extension of the MAX 5000 architecture released by Altera in 1988. With the new architecture, the devices can have up to 20,000 usable gates (on a chip with 40,000 available gates). In its first release, chips in the new MAX 7000 EPLD family offer in-system operating speeds of over 83 MHz. The chips will also offer a higher ratio of I/O pin count to internal logic than any other FPGA family, with the largest chips expected to offer up to 288 pins. Moreover, the enhanced architecture includes a number of significant improvements that result in shorter and more predictable propagation delays, and more flexible logic implementations.

Initially, the company will release two members of the 7000 family of EPLDs, the EPM7032 and the 7256. The 7256 has input-to-output propagation delays (input pin to one macrocell and macrocell output to an output pin) of just 15 ns, while the smaller 7032 has an input-tooutput delay of 12 ns, which yields an upper operating frequency of 83.3 MHz in the system.

The 7032 is the smallest member of the family, and represents the company's first venture into electrically-erasable technology. The chip contains 32 macrocells and comes in a 44-lead package. The other released chip is based on the familiar UV EPROM technology and is one of the highest-density devices. Within the family, however, it's regarded as a mid-range-density device, because it packs about 10,000 available (about 5000 usable) gates and 164 user-I/O pins (192 total pins on the windowed ceramic pin-grid-array package).

Both chips contain the same basic architecture, with the 7032 supplying 32 macrocells—two banks of 16 each, plus four lines dedicated as inputs. When running at top speed, the 7032 consumes just 45 mA, which the company claims is less than half that of its closest competitor, the Mach 110 from Advanced Micro Devices Inc., Sunnyvale, Calif.

Compared to other high-density FPGAs, the 7256 reportedly includes more macrocells, more programmable I/O lines, and can operate at higher frequencies than just about every other RAM- or fuse-based FPGA. A simple function, such as a 16-bit loadable counter im-



expands the number of product terms available to the macrocell, while adding just 2 ns to the signal delay. The macrocell can also use 16 shared expander-product terms. They add about 6 ns to the signal delay, but can be distributed across all logic blocks on the chip.

plemented on the Altera chip, can operate at 71.4 MHz. In contrast, Altera says, the same function programmed into the XC4005-7 from Xilinx Inc., San Jose, Calif., can only operate at 38 MHz. The higher I/O count and performance suits the 7000-series well for various applications, including support logic for RISC-based systems, graphics engines, data-communication controllers, 32-bit coprocessors, and busmaster interfaces.

The basic architecture of the 7000 family is similar to that of the 5000 series. The logic array blocks (LABs), each containing 16 macrocells, are laid out around a central programmable interconnect array (PIA) that ties all of the blocks together. Because the PIA has no EPROM (or EEPROM) transistors in its signal paths, the PIA provides a predictable, 3-ns delay for signals that flow from one LAB to any other LAB. In addition to the 16 macrocells in each block, there are some limitedflexibility parallel-logic expanders. There are also more flexible, sharedlogic expanders, that are part of each macrocell.

Parallel expanders add product

terms into the product-term array without the penalty of a large delay incurred by the use of traditional logic expanders. To keep the delay short (just 2 ns), the "reach" of the parallel expanders had to be limited to just the immediate LAB.

The expanders are connected by the product-term select matrix in parallel with the five basic product terms in the borrowing macrocell. In contrast, the 16 shared-logic expanders provide additional logic resources to any LAB. But they provide those additional logic resources at the expense of adding a larger signal delay (6 ns each time a signal passes through).

The macrocell also includes a configurable flip-flop that can be programmed to implement D, T, J-K, or S-R flip-flops with individually programmable clock control (see the figure). The flip-flop can also be bypassed when the cell must operate in a combinatorial mode.

Each cell has five basic product terms. The basic product terms can be used as primary inputs for combinatorial functions. They can also be used as secondary inputs for either an additional XOR input, or an individual Clear, Preset, Clock, and Clock Enable logic function for the flip-flops. Furthermore, the basic product terms can be used as logic expanders to assist in the generation of complex functions.

Global Clock, Clear, and Output Enable (OE) control signals come in directly from device pins, eliminating the logic-array delay (about 6 ns) as well as minimizing control-function delays.

Designers can also trade off speed to lower chip power consumption. As part of the macrocell library, each logic function comes in either the high-performance standard version or a half-power option. By selectively applying the low-power option to non-speed-critical portions of the design, power can be decreased by as much as 75%. The average speed penalty for the low-power option is 8 ns per macrocell.

Unlike most other PLD architectures, in which the macrocell associated with an I/O pin is lost for use if that I/O pin has been dedicated as an input, the 7000 architecture avoids that type of logic waste by decoupling the I/O pins and macrocell logic resources. Two global OE signals

136 E L E C T R O N I C D E S I G N JANUARY 23, 1992

"Salespeople are often helpful, but my industry publications tell me more of what I need to know."

> Your salespeople can be effective when they get to see a customer or prospect. But, on a day-to-day basis, the buying influences you need to reach turn to specialized industry publications for more of the important information that helps them make buying decisions. A recent study, conducted by the Forsyth Group, proves it.

> In the study, 9,823 business and professional buying influences were asked what sources they find most useful in providing information about the products and services they purchase for their companies. The results were somewhat surprising. Overall, specialized business publications emerged as the source business people turn to first. In other words, trade magazines are where business goes shopping.

Many other sources of information, including sales representatives, direct mail and trade shows, have their place in the total marketing mix. But if you want to reach the highest number of qualified buyers at the lowest cost, specialized business publications are clearly the best choice.

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Actual Size

DC-DC Converter Transformers and Power Inductors

These units have gull wing construction which is compatible with tube fed automatic placement equipment or pick and place manufacturing techniques. Transformers can be used for self-saturating or linear switching applications. The Inductors are ideal for noise, spike and power filtering applications in Power Supplies, DC-DC Converters and Switching Regulators.

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- Transformers have input voltages of 5V, 12V, 24V and 48V. Output voltages to 300V.
- Transformers can be used for self-saturating or linear switching applications
- Schematics and parts list provided with transformers
- Inductors to 20mH with DC currents to 23 amps
- Inductors have split windings



CIRCLE 188 FOR U.S. RESPONSE 138 I CIRCLE 189 FOR RESPONSE OUTSIDE THE U.S.

FLEXIBLE RAM-BASED FPGAs

make it possible for the chips to communicate with more than one bus at a time. Because the signals are global, both OE pins can be controlled directly from device pins, ensuring high-speed operation.

SOFTWARE TOOLS

To capture a design and program the configuration data. Altera offers its MAX+Plus II design software, which was released last year. For the 7000 series, just a simple upgrade to the software is required to add the macrocell library and some architecture-specific details. The software will then be able to support all three of the company's EPLD familiesthe original Classic family, the MAX 5000 series, and the just-released MAX 7000 family. That spans devices from the 8-macrocell EP330 PAL/GAL device replacement up to the 1024-macrocell EPM71024 that will be released late this year.

The software runs under the Microsoft Windows graphical user interface on PCs and compatibles, and thus can access up to 64 Mbytes of extended memory to handle very large designs. Furthermore, the multitasking capability in windows enables the designer to simultaneously compile a design, view a simulation, and make changes to the schematic. That combination reduces the time it takes for designs to move from the concept stage to the silicon stage.□

PRICE AND AVAILABILITY

The EPM7032 is available immediately. It comes in a 44-lead plastic leaded chip carrier and sells for \$14.75 apiece in 100-unit lots. Housed in a 192-pin ceramic windowed pin-grid array package, the EPM7256 sells for \$395 in single-unit quantities. A lower-cost one-time programmable version, housed in a 208-lead plastic quad-sided flat package, can be obtained in the second half of 1992. The MAX-+Plus II development tools are available now.

Altera Corp., 2610 Orchard Pkwy., San Jose, CA 95134-2020; Stan Kopec, (408) 984-2800. CIRCLE 512

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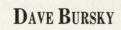
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JANUARY 23, 1992

PRODUCT INNOVATION

MICROCONTROLLERS SPAN 8- AND 16-BIT APPLICATIONS

By Applying A Register-Based Architecture To Solve Control Problems In The 8- And 16-Bit Worlds, An MCU Series Can Add Up To 29 On-Chip Functions.



ingle-chip microcontrollers can now be had with word sizes from 4 to 32 bits at prices from under \$1.00 to over \$50.00. However, most older architectures, especially in the 8- and 16-bit worlds, aren't robust enough to handle the complex control tasks that

today's applications demand. Most recent MCU introductions, though, focused either on the very low end or the very highest, with little attention paid to chips for applications in what Hitachi calls the "leading center."

Such applications stretch the limits of 8-bit processors, while not necessarily justifying the cost of full-16-bit processors. To satisfy most of those types of applications, Hitachi designers created the H8/500 series of microcontrollers. These controllers are implemented in a 1.3- μ m CMOS process and offer a 16-bit CPU core with 8-bit external data paths. Boasting instruction cycle times of as little as 200 ns with a 10-MHz clock rate, the CPU cores are moderately high-performance processors, offering about 50% to 100% better throughput than previous generation 8- and 16-bit MCUs, such as the 8051, 68HC11, Z8, and the 80C196. Furthermore, performance is compara-

Part #	ZTAT masked ROM	HD6415108	HD6475208 HD6435208	HD6475328 HD6435328	HD6475348 HD6435348	HD6475368 HD6435368
Descripti	on	H8/510	H8/520	H8/532	H8/534	H8/536
ROM/RA	M (bytes)	0/0	16K/512	32K/1K	32K/2K	62K/2K
16-bit free-run		2-channel	2-channel	3-channel	3-ch	annel
	Output comparator	4	4	6	6	
Timers	Input capture	2	2	3	3	
	8-bit general purpose	1	1	1	1	
	Pulse-width modulator	0	0	3	3	
	Watchdog	1	1	1	1	
Serial ch	annel	2	2	1		2
ADC		10-bit, 4-channel	10-bit, 8-channel	10-bit, 8-channel	10-bit, 8-channel	
Interrupts		5 external	9 external	3 external	7 ext	ernal
		18 internal	18 internal	19 internal	23 internal	
		8-level priority	8-level priority	8-level priority	8-level priority	
Data-tran	-transfer control Yes Yes Yes Yes Yes		es			
Wait-state control		Yes	Yes	Yes	Yes	
I/O ports		561/0	47 1/0	57 1/0	57 1/0	
		4 input only	8 input only	8 input only	8 input only	
Package			PLCC-68	PLCC-84	PLC	C-84
		QFP-112	QFP-64	QFP-80	QFF	P-80
			DP-64S windowed	LCC-84 windowed	LCC-84 v	vindowed

E L E C T R O N I C D E S I G N 139 JANUARY 23, 1992

FEATURE-PACKED MCU FAMILY

ble to the latest 8/16-bit offerings from such companies as NEC and OKI Semiconductor.

As many as 29 different application support functions—counters, timers, RAM, EPROM, ROM, analog-to-digital and digital-to-analog converters, and many others-can be integrated on the chip along with the CPU. The controllers allow the most on-chip EPROM of any 8- or 16bit controller-62 kbytes-and they can be had in either windowed, reprogrammable versions, or plastic onetime-programmable options. Furthermore, the multiple functions integrated on the various chips in the family give the chips an I/O range that's second to none. Pin counts for the chips range from 64 leads for the smaller members to 84 leads for the feature-packed devices. A ROMless, RAMless microcontroller version requires just 112 pins to access off-chip memory as well.

The H8/500 microcontroller family is a complementary upward extension of the previously released H8/300 8-bit microcontrollers. Both families employ a general-purpose register architecture that allows easy implementation of high-levellanguage compilers.

The register-based architecture of the CPU allows high-level language support tools to be developed—tools that will help shorten product development cycles. Although control software written in a high-level language might compile less efficiently than the same routines created in assembly code, the higher performance of the CPU can often compensate for some code inefficiency.

However, if code can be written in C, for example, compilers will let designers quickly port the code to any of the family members in the H8/500 series, or even the previously-released H8/300 family (or H8/300 Ccode can be recompiled to run on the H8/500 series chips). This considerably shortens time-to-market for costreduced or higher-performance versions of the product. C code written for non-Hitachi processors could even be transferred over. Development tools are available from both Hitachi and third-party suppliersMicrotec and Avocet offer compilers and assembler packages, and Togai Infralogic makes available a fuzzylogic compiler.

To achieve performance levels considerably higher than even most 16-bit MCUs, the H8/500 CPU core employs an instruction format that locates the effective address field at the beginning of the instruction and the operation code at the end. By positioning the information in this manner, the effective address can be calculated and data fetched while the instruction is being decoded. The CPU's 16-bit arithmetic-and-logic unit and on-chip 16-bit data paths provide fast throughput. Two 16-bit numbers can be multiplied in just 2.3 µs and 32-bit values can be divided by a 16-bit value in just 2.6 µs.

Real-time operations are well served by the sophisticated on-chip interrupt controller that can respond to an internal or external interrupt in just 1.8 μ s. Real-world interfaces can be dealt with thanks to either a 10-bit 4-channel analog-to-digital converter included on the H8/510, the ROMand RAM-less controller. The other family members, the H8/520, 532, 534, and 536, all include a higher-resolution, 10-bit 8-channel ADC. Each of the five chips includes a different set of resources that are probably best summed up in the *table*.

Furthermore, the H8/500 series claims to pack more on-chip peripherals than any other family, including the multichannel ADC that delivers digitized samples in just 13.8 ms and a full-duplex serial communications port. The port operates in asynchronous or clock-synchronous modes, and transfers data at up to 2.5 Mbits/ s. An on-chip data-transfer controller can be programmed for automatic direct-memory access transfers for 8- or 16-bit values between any of the on-chip peripherals and memory without CPU intervention.

The microcontrollers also contain eight on-chip timers. Three are 16-bit free-running units, handy for pulse generation and pulse and frequency measurements. Three additional timers can be used for pulse-width-modulation applications. Another 8-bit timer can be programmed for multiple applications and can deliver variable duty-cycle pulses. And a watchdog timer lets the chips recover from runaway errors.

To handle many of the more complex applications, the CPU core can address a large external memory-16 Mbytes-and can handle even some of the most data-intensive control needs. Even long-word (32-bit data types) can be handled by the core processor, so it can tackle applications such as hard-disk control, automobile engine control, and other "soft-DSP" requirements. The orthogonal instruction set of the series permits instructions to use all seven addressing modes the processor offers. Instructions are variable in length, and can range from just 2 bytes up to 7 bytes.

The CMOS process used for chip implementation allows an option for 3-V operation. As part of the processor design, Hitachi engineers included both sleep and standby powerdown modes. The sleep mode halts the CPU during idle periods, trimming power by about 33% from the active mode. An even lower-power mode, standby, will trim current drain to less than 0.1 μ A. In the standby mode, all functions are halted and the contents of the on-chip RAM and CPU registers are maintained.

PRICE AND AVAILABILITY

The first five members of the H8/500 series are immediately available in three speed grades—6, 8, and 10 MHz. Prices for the memory-less H8/510 start at \$11.85 in 5000-unit lots (6 MHz); the H8/520 start at \$11.45 each for the masked-ROM version in 10,000-unit lots, or \$22.50 each for the ZTAT one-time-programmable version in 1000-unit lots. Prices for the masked-ROM versions of the H8/532 start at \$14.20 apiece in 10,000-unit lots; the H8/536 goes for \$19.40. ZTAT versions of the 532, 534, and 536 are \$25.80, \$29.60, and \$34.10, respectively, in lots of 1000. Samples of the ZTAT versions are immediately available.

Hitachi America, Ltd., Semiconductor and IC Div., 2000 Sierra Point Pkwy., MS-080, Brisbane, CA 94005-1819; John Hull, (415) 244-7136. CIRCLE 513

HOW VALUABLE?	CIRCLE	
HIGHLY	544	
MODERATELY	545	
SLIGHTLY	546	

140 E L E C T R O N I C D E S I G N JANUARY 23, 1992

WORKSTATION DUO FILLS LOW END, DOES 35 MIPS FOR UNDER \$5000 Richard Nass

COMPUTERS & PERIPHERALS

ewlett-Packard's has added two new members to its Series 700 family of workstations—the Models 705 and 710. The 705 offers 35 million instructions/s (MIPS) for just \$4990. In addition, the 710 is the first workstation to perform 50 MIPS for under \$10,000, the company says. Also, HP is adding two graphics options, the CRX-24 and CRX-24Z, and rendering software called Power Shade. Power Shade performs three-dimensional entry- to moderate-level solids modeling.

The 705 and 710 workstations are based on the same PA-RISC architecture as its 720, 730, and 750 predecessors. The series 700 is software compatible with the company's series 800 workstations. At least 4500 applications are available to the two families, including electronic-design automation, mechanical CAD, desktop publishing, and scientific applications. With Soft PC, a 25-MHZ 386 emulator, the systems can run DOS applications. The two systems can be expanded using SCSI, RS-232, and parallel ports to connect up to 10 peripheral devices.

The 710 model is based on the same 50-MHz PA-RISC microprocessor as the 720, previously the low-end system. The 710's floating-point processor does 12.2 double-precision MFLOPS compared to the 720's 17.9 MFLOPS. The lower floating-point performance is partly caused by the system's higher integration-HP aimed to squeeze the 710 into a smaller box at a lower price. Also, cache memory was cut in half to 32 kbytes in the instruction cache and 64 kbytes in the data cache. Three different graphics configurations are available for the 710. Users can choose between a 19-in. color (1280 by 1024 pixels) or gray scale (1280 by 1024) display or a smaller footprint, 16-in. color (1024 by 768) display. All three systems can perform 950,000 2and 3-D vectors/s. The workstation has an internal disk capacity of 840



Mbytes and 9.4 Gbytes, external.

The entry-level price for the 710 is \$9490. That includes 16 Mbytes of memory and a 19-in., gray-scale display. The second-level 710 system, priced at \$11,490, adds a 16-in. color display. The high-end system includes a 19-in. color display and sells for \$13,990. Another feature of the 710 is that it can be coupled with one or more X-terminals, further reducing the cost per seat.

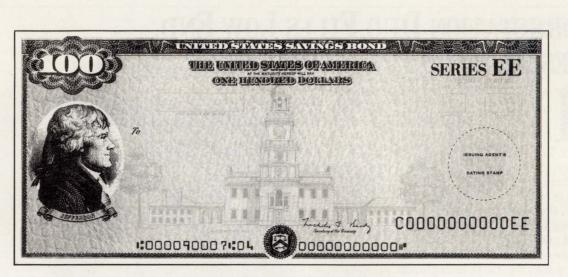
The 705 is only being offered with a 19-in. gray-scale display. The \$4990 diskless system comes with 8 Mbytes of main memory (expandable to 64 Mbytes). A 16-Mbyte system costs \$6340. Based on a 35-MHz processor, it delivers 34 SPECmarks and 8 MFLOPS. The system can house two internal disk drives to hold 840 Mbytes of mass storage, the same as the 710. The 705 incorporates the same quiet, compact desktop or deskside package as the 710. This system lets HP make inroads into the commercial and CASE markets. As for new graphics capabilities, the CRX-24 and -24Z are compatible with the three previous models of the 700 series, but not with the 705 or 710, whose graphics capabilities are integrated onto the motherboard.

The CRX-24 is aimed at imaging tasks in the scientific and visualization markets. The CRX-24Z, targeting mechanical CAD markets, is similar to the CRX-24, but contains a built-in accelerator and a Z-buffer. Both the 24 and 24Z products feature double buffering as well as eight overlay planes. They can perform 1.15 million 2- and 3D vectors/s, transferring data at 44 Mbytes/s. The 24Z features antialiasing and volumetric rendering, with accelerated shading.

The Power Shade rendering software, which runs on all series 700 platforms, comes bundled with the CRX-24Z graphics and is a \$2000 option with all the other color graphics products.

Hewlett-Packard Co., 19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900. CIRCLE 457

ELECTRONIC DESIGN 141



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UPGRADABLE WORKSTATIONS OFFER PERFORMANCE OPTIONS

A redesigned motherboard architecture places the R3000A RISC processor, caches, and floating-point coprocessor on a field-replaceable card. That gives the latest ACE-compliant DECstation workstations and servers the power to handle today's computing needs as well as tomorrow's. Four 5000-series workstations and three servers were released last month by Digital Equipment Corp.

The workstations range from 16.3 SPECmarks for the budget-priced Personal DECstation up to the 20-MHz Model 20, which sells for \$3995 with a 17-in. grayscale monitor. At the high end is the 32.4 SPECmark, 40-MHz, Model 240, which sells for \$11,995 with 16 Mbytes of RAM, and a 19-in. monochrome 1280-by-1024 pixel monitor. In the middle are the 25-MHz DECstation 5000/25, and the 33-MHz model 133, which deliver 19.1 and 25.5 SPECmarks, respectively.

Server models include the low-cost DecSystem 5000/25 and 5000/240, which are offshoots of the workstations and sell for \$4995 and \$13,495, respectively. Also released was the highend DecSystem 5900, which has SPECmark ratings of 32.8 or 42.9, depending on the CPU option selected. That system price starts at \$59,050. Included



with the model 5900 server is the Prestoserve file system accelerator that can boost network file system performance by as much as 300%. It is available as an option on the other servers for \$4000.

All the workstations and servers are upgradable with a simple 3-by-5-in. daughtercard replacement to the R4000 processor, which will be available on daughtercards later this year. Three TURBOchannel-based graphics upgrade options, the HG, PXG+, and PXG Turbo+ offer 2D, 3D, and 24plane color capabilities as well as the ability to handle multimedia applications. All system hardware is available now or it will be released this quarter. R4000-based CPU upgrades will be released in the second half of 1992.

Digital Equipment Corp., 146 Main Street, Maynard, MA 01754; (508) 493-5111. GERCLE 458 ■ DAVE BURSKY

UPGRADE SPARC WORKSTATION TO 40 MHZ

By taking advantage of the Opus Systems upgrade kit, users can boost the performance of their Personal Mainframe Sparc workstations from 15.8 to 29 MIPS. The kit consists of a 40-MHz motherboard, Solaris 1.0, documentation, and installation instructions. The 40-MHz microprocessor replaces the existing 20- or 25-MHz processor. The upgrade is binary-compatible with all Sun Microsystems hardware and software and adheres to Sparc International SCD 1.1 compliance specifications. Now, users have the power needed for such complex applications as mechani-cal analysis and design and circuit simulation. Upgrading with the kit requires replacing the original motherboard and loading the software. The kit, available now, sells for \$4195.

Opus Systems Inc., 329 North Bernardo Ave., Mountain View, CA 94043; (415) 960-4040. CIRCLE 459

NONVOLATILE DISK ZIPS DATA AT 3 MBYTES/S

PC users are always seeking faster data speeds. The BlueFlameIII solidstate nonvolatile disk emulator operates more than 20 times faster than a traditional hard disk drive, while performing identical tasks. In addition, the emulator isn't susceptible to environmental conditions such as shock, vibration, thermal sensitivity, and physical wear and tear. The BlueFlameIII is actually an I/O mapped device that uses battery-backed DRAM fitted into 14 single-inline memory modules (SIMMs). 1- and 4-Mbyte by 9 SIMMs are supported. The speed of the device is limited only by the speed of the I/O bus. Typical transfer rates are 3 Mbytes/s. Capacities for the fulllength 16-bit card range from 2 to 56 Mbytes. Prices start at \$595.

SemiDisk Systems Inc., P. O. Box GG, Beaverton, OR 97075; (503) 626-3104. CIRCLE 460



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E L E C T R O N I C D E S I G N 143 JANUARY 23, 1992



Control any IEEE-488 (HP-IB, GP-IB) device with our cards, cables, and software for the PC/AT/386. EISA, MicroChannel, and NuBus.

SYNTHESIS TOOL CREATES **TESTABLE CIRCUITS**

A new version of the Test Compiler synthesis tool has more features that design testability into synthesized circuits. Test Compiler Version 2.2 outputs test patterns for HDL simulators. In addition, its automatic-test-patterngeneration (ATPG) capabilities are two to three times faster than the previous version for large designs. Through optimization and test-pattern-compaction techniques, Version 2.2 brings the penalties for scan design to a minimum, ultimately reducing the cost of manufacturing testability. A new test mode in Test Compiler lets users specify a chip configuration for test that may be different from that of normal operation, and still meet area and speed objectives. Other Version 2.2 features include an integrated scan-rule checking with schematic generation so that users can immediately identify feedback loops, even across hierarchical boundaries. Test Compiler Version 2.2 runs on Unix workstations, and is shipping now starting at \$40,000.

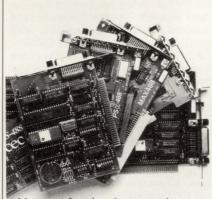
Synopsys Inc., 700 E. Middlefield Rd., Mountain View, CA 94043-4033; (415) 962-5000. CIRCLE 461

VHDL DESIGN SYSTEM COSTS LESS THAN \$5000

For less than \$5000, engineers can design and simulate with VHDL on their Sun workstations using the V-System/ Sparc software from Model Technology. V-System/Sparc, which is fully IEEE-1076 compatible, includes a VHDL compiler, interactive VHDL simulator, and VHDL source-language debugger. Its multi-windowed, mousedriven environment can handle designs with more than 100,000 lines of VHDL. Six different interactive windows let users simultaneously view and interro-

gate the design hierarchy, view the VHDL source code during execution, display variables and signals, control the simulator, display selected processes, and list the simulator output. In addition, compilation time is more than 15.000 lines/min. on a Sun workstation. A single-user license for V-System/ Sparc costs \$4995 plus 15% annual maintenance fee. Floating network licenses are also available.

Model Technology Inc., 15455 N. W. Greenbrier Pkwy., Suite 210, Beaverton. OR 97006; (503) 690-6838. CIRCLE 462



You get fast hardware and software support for all the popular languages. A software library and time saving utilities are included that make instrument control easier than ever before. Ask about our no risk guarantee.

ORCAD UPDATES BOTH TOOLS AND FRAMEWORK

OrCAD has updated its ESP Framework and Schematic Design Tool Release IV. The enhancements to ESP include a hot-key capability, which lets users select and run any given tool with one user-defined strike. Also, additional information in the View Reference Materials menu supplies users with more help files. Version 4.10 of the schematic tool creates net lists 35% faster than the previous version and includes support of AMD's MACH devices. ESP Framework and Schematic Design Tools Release IV Version 4.10 run on PCs and are available now. ESP is included with the schematic tools for \$595. All OrCAD products include free technical support and access to the company's bulletin board for one year.

OrCAD, 3175 N. W. Aloclek Dr., Hillsboro, OR 97124-7135; (503) 690-9881. CIRCLE 463

TIMING-ANALYSIS TOOL SIMPLIFIES BUS DESIGN

BusDesigner/AT, an interactive tim-ing-analysis tool from Chronology Corp., speeds and optimizes bus-interface design for AT-based board-level products. The tool reduces the hundreds of stringent timing specifications embedded in IBM AT, ISA, and EISA standards into a small group of requirements that determine bus compatibility. Consequently, engineers can quickly check a variety of architectures while still in the design stage, then automatically generate and analyze detailed timing diagrams once an architecture is chosen. BusDesigner/AT was developed by On Target Associates, Sunnyvale, Calif., using Chronology's core software offering, TimingDesigner. To use BusDesigner/AT, users simply select the type of bus cycle and the appropriate options, and the software automatically generates the proper timing diagrams using a gener-ic delay library. TimingDesigner then redraws and analyzes the diagrams, highlighting any timing violations. BusDesigner/AT, which includes bus timing models, a step-by-step users' guide, a book on AT-bus design, and fully documented design examples, runs on personal computers with TimingDesigner and MS Windows 3.0. It's shipping now for \$695.

Chronology Corp., 2721 152nd Ave. NE, Redmond, WA 98052. (206) 869-4227. CIRCLE 464

Free: Informative catalog 800-234-4232 Applications help (617) 273-1818



Capital Equipment Corp. Burlington, MA. 01803

CIRCLE 94 FOR U.S. RESPONSE CIRCLE 95 FOR RESPONSE OUTSIDE THE U.S.



144 ELECTRONIC DESIGN **JANUARY 23, 1992**



PORTABLE DIGITAL SCOPES BOAST 1-MSAMPLE MEMORIES

vailable in both 2- and 4-channel versions, the Model 9300 series portable digital oscilloscopes offer record-memory lengths of up to 1 million samples per second. All models have 300-MHz analog bandwidths and independent 100-Msample/ s digitizers on all inputs.

Users can select from three memory configurations. The basic units have a 10-ksample record length per channel. The M (medium) versions have 50ksample record memories, and the L (long) versions have 1-Msample record lengths for each channel. The extremely long record lengths make these scopes particularly useful for applications involving radar, magnetic media, data communications, and electromechanical systems.

Features of the 9300 series include fast automatic setup for repetitive signals and a sequence mode, which allows users to store multiple events in segmented acquisition memories. Additional capabilities such as pass/fail testing; fastglitch, dropout, and window triggering; signal processing; and



FFT analysis add to the scopes' functionality.

All members of the scope family incorporate a PC-compatible memory card system. The system is based on the Personal Computer Memory Card International Association standard, which is supported by most major personal computer manufacturers.

The 2-channel Model 9310 (10 ksamples) costs \$4990; the 9310M (50 ksamples) costs \$5990, and the 9310L (1 Msamples), \$9990. The 4-channel Model 9314 is \$7490, the 9314M \$8990, and the 9314L \$14,990.

LeCroy Corp. 700 Chestnut Ridge Rd., Chestnut Rdige., NY 10977-6499; (914) 425-2000. ☐ JOHN NOVELLINO

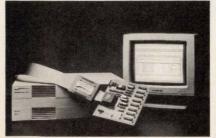
SMT PROBE ADAPTER WORKS TO 350 MHZ

The PQFP100 KwiKlip probe adapter allows users to probe JEDEC plastic quad flatpack (PQFP) devices at speeds to 350 MHz. The adapter works with 100-pin devices such as the Intel 80386SX and 100-pin ASICs. The device's high bandwidth is made possible by a low-profile design that shortens lead lengths and decreases crosstalk. The result is minimal reactive loading. The low profile also offers easy access to surrounding components. The top portion of the adapter, which fits snugly over a PQFP surface-mount chip carrier, is a pin-grid-array socket. This arrangement offers users a number of probe interconnection schemes. The PQFP100 costs \$260 and is available from stock.

Tektronix Inc., P. O. Box 1520, Pittsfield, MA 01201; (800) 426-2200.

EMULATOR HANDLES i960 CACHE ANALYSIS

The Step Express III emulator expands the line of Step Express emulators to include cache-analysis support for the Intel i960CA microprocessor. Cacheanalysis is handled by an advan/ l triggering facility and a performance analysis facility using cache-based execution information. Both features are connected through the SDBUG960, a fully integrated source-level symbolic



debugger. The Express III includes features to selectively store execution cycles from cached operation, identify conditions that are in and out of cached execution range for transition to other trigger levels, and measure system performance with the cache on. The Step Express III is priced from \$35,000 and is available 30 days after receipt of an order.

Step Engineering Inc., 661 E. Arques Ave., P. O. Box 3166, Sunnyvale, CA 94088-3166; (800) 538-1750 or (408) 733-7837. CHROLE 467



Behlman's AC Power Source works perfectly to simulate the power that's available in all 172 nations. Use it to do sophisticated 50 Hz testing of trash compactors for tiny Tuvala, as well as 400 Hz avionics testing in Alaska. It gives you up to 9000 VA of clean power, at prices that won't clean you out, starting at just \$2,350. Call (800) 456-2006 today, or write: Behlman, 6 Nevada Drive, Lake Success, New York 11042.



CIRCLE 208 FOR U.S. RESPONSE CIRCLE 209 FOR RESPONSE OUTSIDE THE U.S.

BOUNDARY SCAN LOGIC COMES IN TRANSCEIVERS

ide-word transceivers, offering 18-bit wide data paths, have been designed to be fully compliant with the JTAG (Joint Test Action Group) 1149.1 serial boundary-scan test standard. Moreover, not only do the chips in National Semiconductor's SCAN family include the JTAG port, but they are also compatible, from a pinout and signal viewpoint, with existing non-boundary-scan transceivers. Thus, the 18-bit circuits can be replaced with 16-bit FACT-compatible chips without redesigning the pc board (but dropping the two parity bits). In contrast, other transceivers that include JTAG ports have unique pinouts and cannot be directly replaced with a non-JTAG transceiver.

National will initially offer four transceivers and one serial/parallel test access port (TAP) that allows a non-scan device to talk to a JTAG bus. The four transceiver parts include the SCAN18540 and 18541T 18-bit buffers, the SCAN18373T 18-bit register, and the SCAN18374 18-bit latch. The TAP chip's number is SCANOSC100F. The JTAG logic on all the chips implements the required JTAG commands (Sample/preload, External Test, and Bypass), as well as two additional com-



NEW PRODUCTS

mands (Clamp, and High Impedance) to better test the parts. The CMOS chips draw minimal power during standby, yet allow system speeds of 25 MHz and faster.

The transceivers come in 56-lead, fine-pitch (25-mil) shrink small outline IC packages (SSOPs), while the TAP chip comes in a 28-lead (50-mil spacing) SOIC. The chips also have controlledoutput-waveshaping circuits to minimize noise and crosstalk. Samples are immediately available and in 100-unit lots sell for \$5.75 apiece except for the TAP chip, which sells for \$9.95.

National Semiconductor Corp., 2900 Semiconductor Dr., P. O. Box 58090, Santa Clara, CA 95052-8090; Gary O'Donnell, (408) 721-5000. CINCLE 468 DAVE BURSKY

BURST CACHE RAM IN BICMOS ACCESSES IN ONLY 14 NS

llowing designers to build 50-MHz, no-wait-state systems based on the 80486, the CY7B173 cache RAM incorporates many support functions right on the chip. Built in biCMOS, the 256-kbit chip is organized as 32 kwords by 9 bits and has a basic access time of 14 ns. Along with the memory, the chip includes a burst counter, address and data registers, and synchronous, self-timed write-control logic. On-chip decoders also simplify memory expansion from one bank of four devices (128 kbytes) to two banks of four chips, thus doubling the size of the cache with no performance penalty.

The high speed of the part coupled with the glueless interface to the 80486 CPU, the cache controller and the system clock keeps the system running at top speed. Separate pins for processor

and cache controller address strobes enable the CY7B173 to switch control from the 486 to the cache controller during cache misses. Since the CPU doesn't relinquish control to the cache controller during a cache miss, designs done with previously available cache RAMs required external logic to control the cache. The CY7B173 eliminates that external logic and thus further improves system speed. A companion burst RAM that handles linear burst sequences rather than the required sequence for loading the 486 is also available from Cypress (CY7B174). Both cache RAMs are housed in 44-lead plastic leaded chip carriers. In lots of 100 either chip sells for \$69. apiece. Samples are available from stock.

Cypress Semiconductor Corp., 3901 N. First Street, San Jose, CA 95134-1599; (408) 943-2600. CHRCH 469 ■ DAVE BURSKY

ICS SEGMENT TEST PATHS FOR EASIER BOUNDARY SCAN

wo scan-path support ICs help designers isolate problems on printed-circuit boards more easily by partitioning boundary-scan test paths into smaller segments. The smaller scan paths, or chains, reduce the number of bits being scanned, which simplifies test software development. The ability to switch to alternative scan paths also increases fault tolerance.

The SN74ACT8997 scan-path linker allows the designer to switch the primary scan path to any combination of four secondary scan paths (SSP). In that way several SSPs can be accessed simultaneously. The device is useful when the designer has functional blocks of circuitry (or boards) that are not autonomous. The test program can then open single SSPs to test one functional block or board or open multiple SSPs to test multiple boards.

The SN74ACT8999 scan-path selector allows the designer to switch the primary scan path to one SSP at a time. When the one SSP is being used, the other three remain in stable test access port states. This device is useful for partitioning SSPs when the system under test has several functional boards.

Both devices have module identification pins, which are useful when the ICs are installed on multiple printed circuit boards with boundary-scan access across the backplane. Each board can have a unique ID code so the scan controller can automatically configure the sequence in which the boards will be tested.

Fabricated in 1- μ m Epic advanced CMOS, both devices come in 28-pin plastic DIP or SOIC packages for commercial use. Military versions will be introduced in 28-pin ceramic 300 MIL DIP and 28-pin leaded ceramic chip carrier packages. The ICs are characterized for commercial operation over a range of 0° to 70°C.

The 'ACT8997 costs \$5.00 in 1000piece quantities, and the 'ACT8999 costs \$5.50 in similar quantities. Both are available immediately.

Texas Instruments Inc. Semiconductor Group (SC-91078), P. O. Box 809066, Dallas, TX 75380-9066; (800) 336-5235, ext. 700 or (214) 995-6611, ext. 700. **CIEDE 470** ■ JOHN NOVELLINO

146 E L E C T R O N I C D E S I G N JANUARY 23, 1992

NEW PRODUCTS

MOTHERBOARD CHIP SET EASES 386/486 SYSTEM UPGRADES

A motherboard chip set for 80386 and 80486-based PCs allows designers to implement a modular architecture that permits CPU upgrades. To make upgrading possible, the OPTi chip set "pushes" the CPU, FPU, and optional cache cluster onto an add-in card that employs an EISA bus format. Rather than use the standard EISA-bus signals, however, the EISAspecific pins carry CPU signals back to the chip set. Thus, the two-chip DXBB concept simplifies motherboards since only the chip set, main system DRAM and BIOS, and I/O functions need be on the motherboard.

The three chips in the set consist of the 82C496, the CPU, block interleave DRAM and AT bus controller; the 82C497, a write-back cache controller; and the previously available 82C206 peripheral controller. When implemented with the three chips, a typical motherboard would contain both ISA and EISA-connector card slots. The EISA slots, however, cannot accept standard EISA cards since all the EISA-specific signal lines are different. Instead, they accept compute-cluster cards that each system manufacturer can create. And since the bus set up by the OPTi chip set is the common connection point, CPU cards from different suppliers should be interchangeable.

The 82C496 comes in a 184-lead PQFP and provides support for 80386DX, 486SX, and 486DX CPUs and control of up to four banks of DRAM (256k, 1-Mbit, or 4- Mbit chips). The controller also supports DRAM transfer bursts and through interleaving allows very compact non-cached 33-MHz systems to be built. The 160-lead 82C497 supports cache sizes from 64 to 256 kbytes. For systems above 33 MHz, the controller uses an asynchronous interface to the 82C496. As a result, the motherboard runs at a constant 33 MHz when higher speed CPUs are plugged into the system.

Samples of the chip set (the 82C496 and 497) are available now and sell for \$27.50 per set in lots of 10,000.

OPTi Inc.,2525 Walsh Ave., Santa Clara, CA 95051; Raj Jaswa, (408) 980-8178. [□□□1411] ■ DAVE BURSKY

CHARGE CONTROLLER MANAGES BATTERY POWER

Anaging the quick charging and monitoring of nickelcadmium batteries, the ISC1700-01 employs a patented "Reflex" charge algorithm licensed by ICS to achieve full battery charges in just 20 minutes. The CMOS chip can safely charge the batteries while minimizing memory effects, restoring faded capacity, improving battery life and reliability, enhancing charge acceptance, and increasing charge efficiency. The chip also operates in a pulsed maintenance mode that keeps batteries at peak charge. By providing smart control, the chip permits the use of less costly "standard-charge" batteries, rather than the more expensive "fast-charge" cells. That permits more cost-effective systems to be designed.

As many as eight charge-termination methods ensure safe charging, reduce excessive heating, detect defective cells, and reduce internal pressure to avoid cell venting. Some of the monitoring schemes include examining the linear regression slope of the battery voltage, sensing the battery temperature, use of a "deadman" timer, short sensing, checking for high-impedance cells, and detecting voltage rise.

The IC has a dedicated processor, DSP, dataROM, RAM, comparators, ADC, and a bandgap reference. An external 1.2-V reference can be fed into the chip. Other inputs include lines for a thermal sensor and an analog voltage, as well as some selection control inputs and R-C connections for the on-chip oscillator (1 MHz, nominal). Output lines provide LED drive for charge status, battery, and contact problem indicators. The ICS1700 is housed in a 16-pin plastic DIP and consumes just 3 mA, typical, from a 5-V supply. It is available now and sells for \$11 apiece in lots of 1000.

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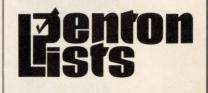
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ON PCS, WORKSTATIONS Available in either a DOS version for

IBM PCs and compatibles or in an Open Look or Motif environment under Xwindows for a variety of Unix workstations, S-Plus provides an interactive computing environment for graphical

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ment permits the software to be used

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namic graphics (3D rotatable and

linked) with brushing and point identifi-

cation, as well as 2D plotting, basic sta-

tistics, multivariate statistics and

graphics, time series analysis, and sur-

vival analysis. Data can be transferred

into and out of the software with ASCII

files, or keyboard input, or binary files.

Included with the software is its own

object-oriented language for program-

ming. Single-user DOS price is \$1195

and \$2800 for workstations (plus a \$600

annual maintenance fee for worksta-

tion versions). DOS systems should be 386/387 or 486-based with at least 2 Mbytes of RAM, an EGA, VGA or Her-

cules display adapter, and 25 Mbytes of

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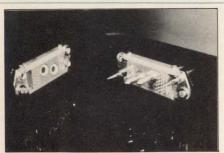
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RF Input (max dBm VSWR "on" Video Bkthru	1) 1.25 30	- 20 1.35 30	1.5 30	22 1.4 30	
	3 SWA-2-50 NA-2-50[3 YSW- ZYSW-2	

Reflective SPDT YSW-2-50DR ZYSW-2-50DR

21	000-2-00	00- 2000-				
dc-	500-	2000-				
500	2000	5000				
0.9	1.3	1.4				
50	40	28				
20	20	24				
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S.R.	Slew Rate (Typ)	250	400	450	1000	80	V/µsec
G.B.W	. Gain Bandwidth (Typ)	45	45	90	100	14	MHz
ts	Settling Time (to 0.1%) (Typ)	90	90	100	75	340*	nsec
Avol	Open Loop Gain (Typ)	50	7	45	28	450	V/mV
Vos	Offset Voltage (Max)	1	2	6	3	0.9	mV
Ios	Offset Current (Max)	0.3	0.4	1	-	.00005	μA
IB	Bias Current (Max)	0.3	8	1.7	3	.0001	μA
en	Voltage Noise ($f = 10 K Hz$)	17	22	25	3.3	15	nV/VHz
in	Current Noise ($f = 10 KHz$)	3	1.5	4	2.1	.002	pA/VHz
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