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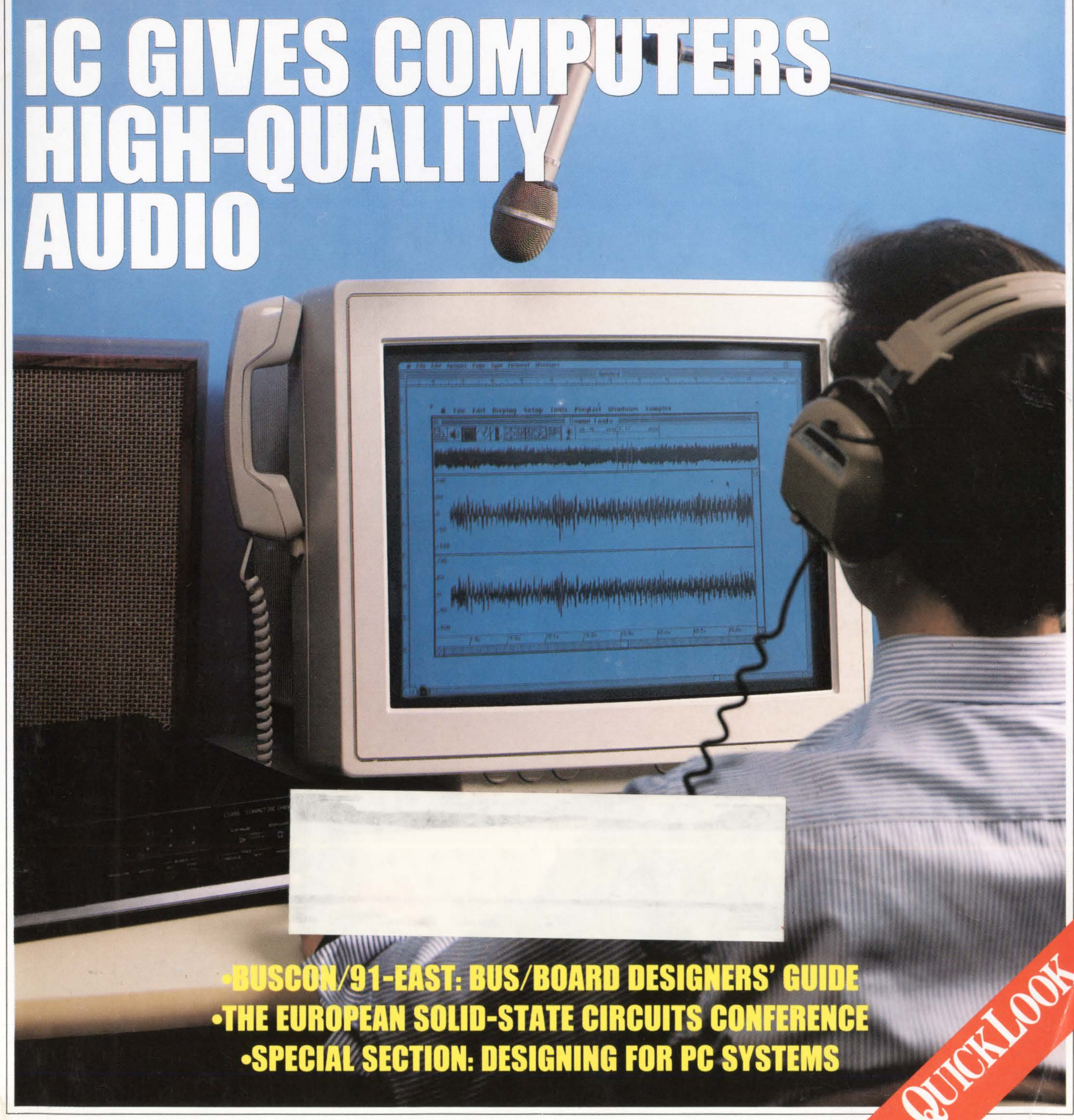

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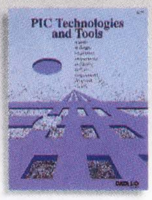

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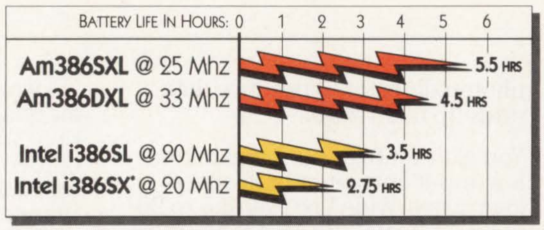

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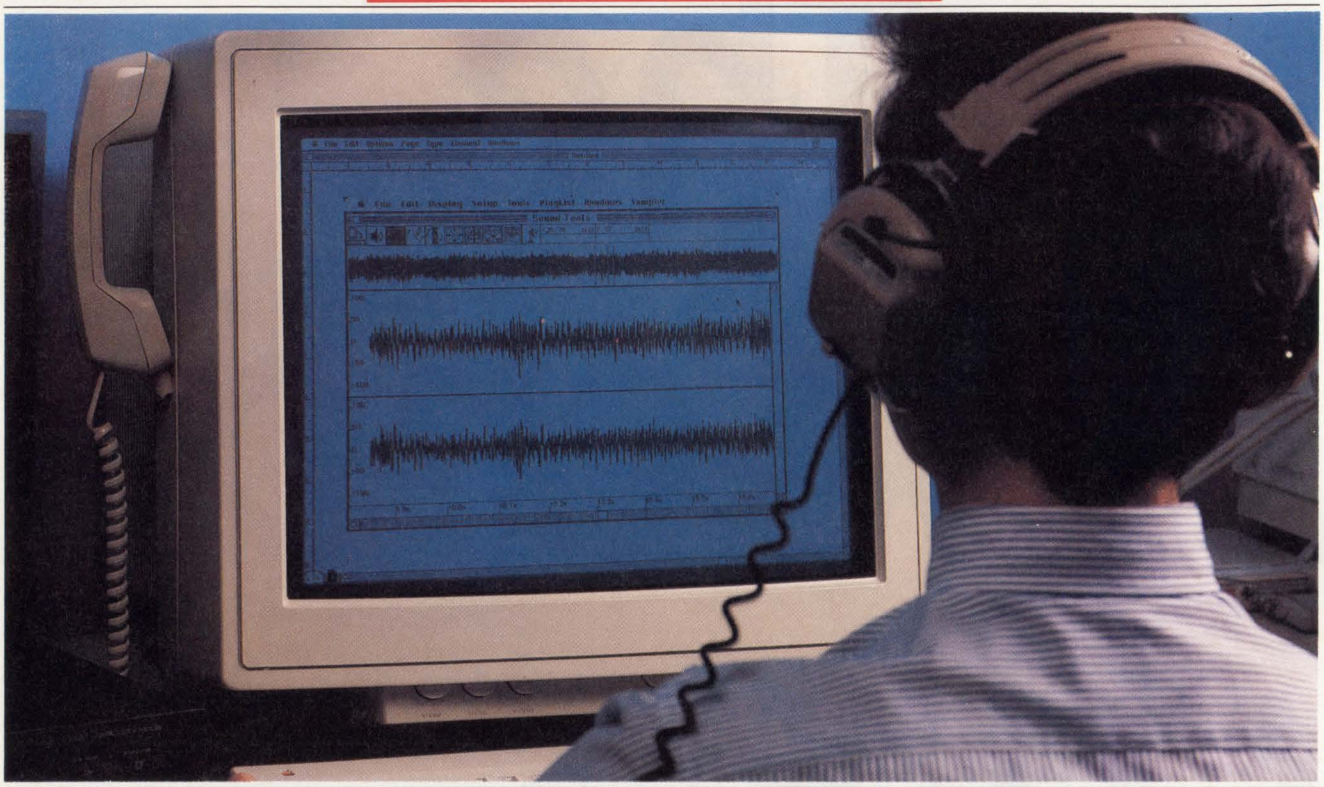

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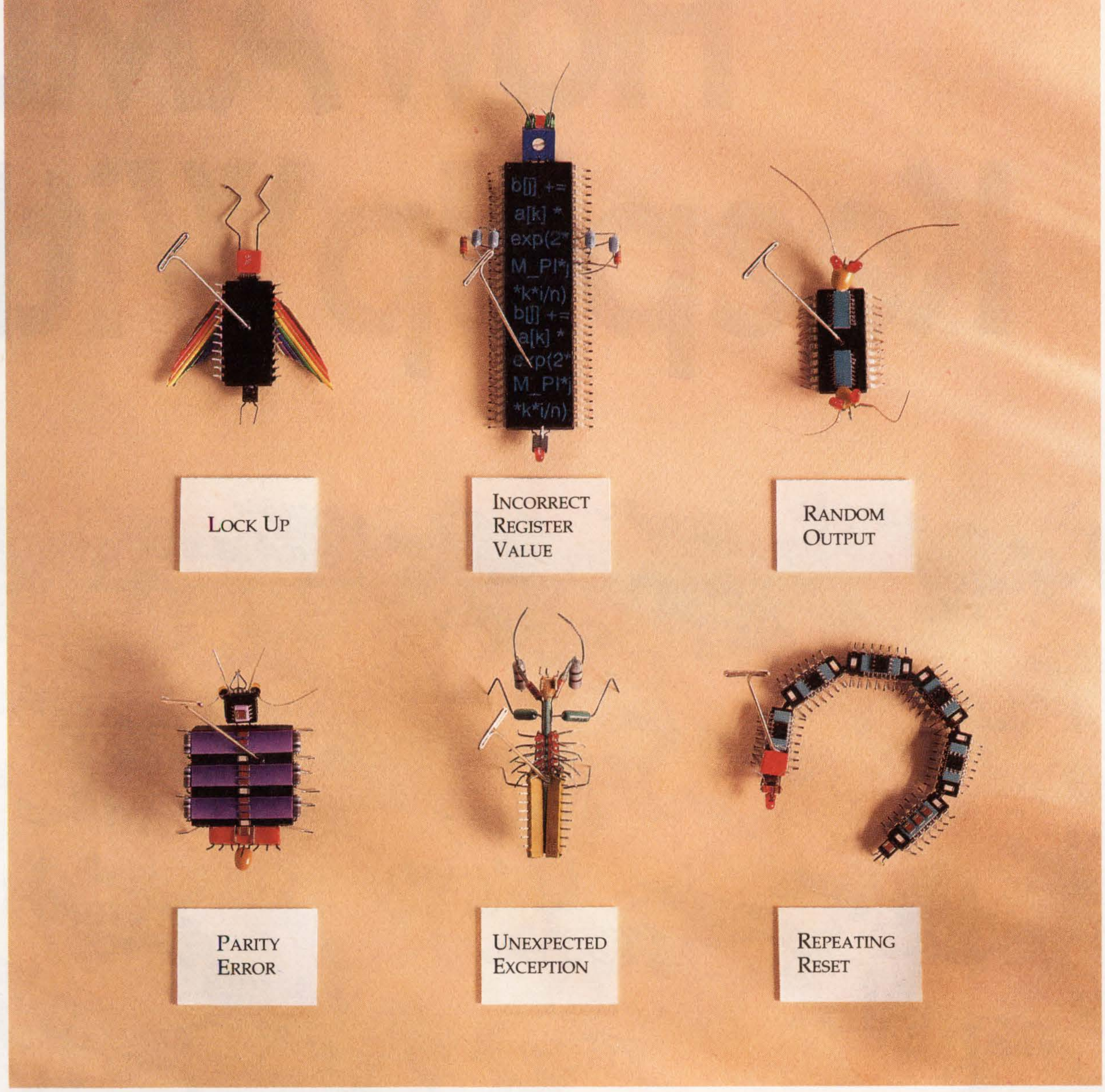

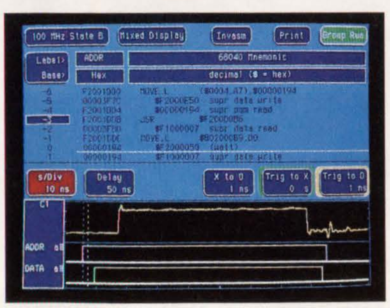

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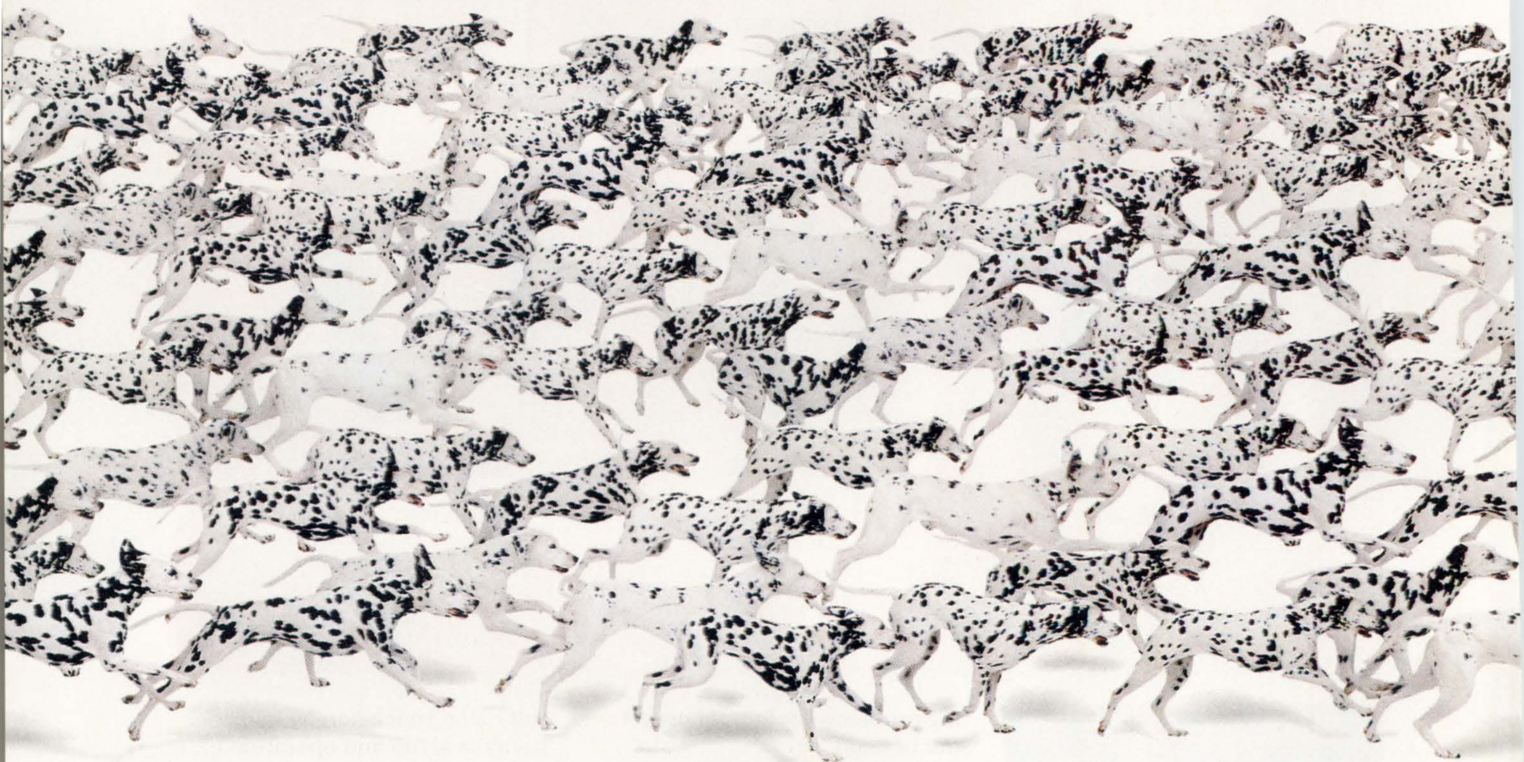

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THE U.S. PICTURE LOOKS BRIGHTER

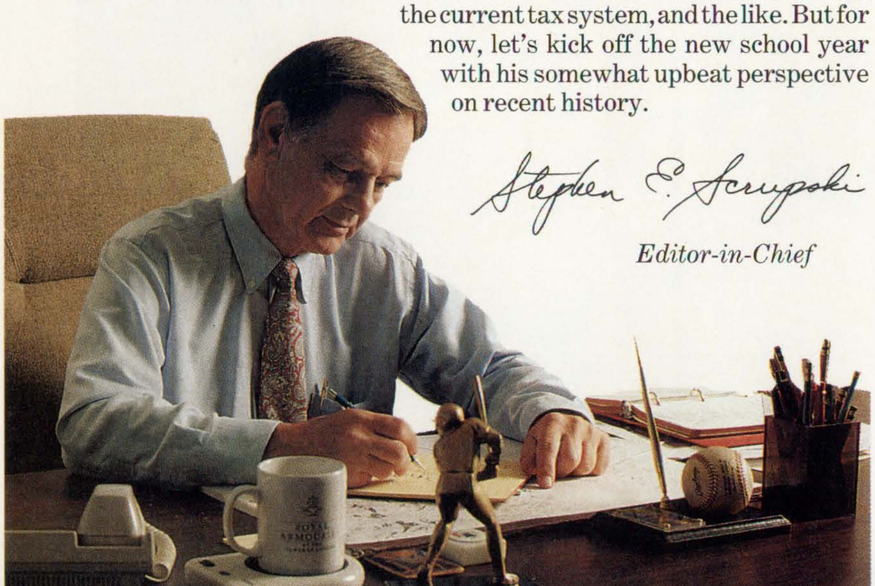
Previously, at this time of year, we've commented on the annual "back to school" ritual. September always feels more like a time for beginnings and optimism, rather than, say, January. Apropos of that feeling, T.J. Rodgers, president and CEO of Cypress Semiconductor Corp., San Jose, earlier this summer offered a wide-ranging analysis of the semiconductor industry's problems in a statement to the House Subcommittee on Technology and Competitiveness. Rodgers, an outspoken critic of any direct involvement in the semiconductor industry by government—such as Sematech—maintained that "The American chip industry is quite healthy right now," adding that America's slide began in 1979 and ended in 1985.

Citing industry-watcher Dataquest's figures, Rodgers notes that between 1982 and 1989, a 37-point reversal apparently occurred in market share between Japan and the United States—Japan's share went up from 34% to 52%, while the U.S. slipped from 54% to 35%. However, he feels those troubling figures tend to obscure the picture. The dramatic market-share reversal is based on nominal revenues rather than volumes. "The figures reflect currency exchange rates more than they do underlying competitive strength," he says.

Rodgers points out that if a constant yen-dollar exchange rate is used for the 1982-89 year span, the trend looks much less dire. In 1982, the rate was 249 yen to the dollar; in 1989, it was 138; and in 1990, it was 144 (at present time, the rate is about 137). Using the 1990 rate, he calculates that Japan held 47% of the world semiconductor market in 1982 while the United States held 43.5%; in 1989, the Japanese share was 51% while the U.S. share was 36%. In other words, according to Rodgers, 25 points of the 37-point market-share reversal cited by the "doom and gloom" school reflect currency fluctuations rather than true competitiveness. "These adjusted trends are nothing to celebrate," he adds, "but they offer a less distorted picture than the nominal statistics." He also argued that Japan has gained no ground on the U.S. in semiconductors since 1987: Japan's worldwide market share has hovered within 2 points of 50%, while the U.S.'s has hovered within 2 points of 37%.

Furthermore, Rodgers stated that innovative American companies lead when it comes to specialized logic chips, such as math, digital-signal, and video processors. He feels the U.S. is right where it should be—dominating the high-value, high-margin, innovation-driven parts of the business.

Rodgers had much more to say about Sematech, deficit government spending, the current tax system, and the like. But for now, let's kick off the new school year with his somewhat upbeat perspective on recent history.



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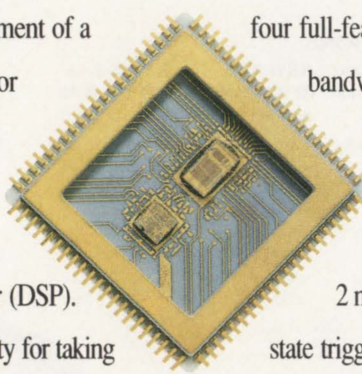

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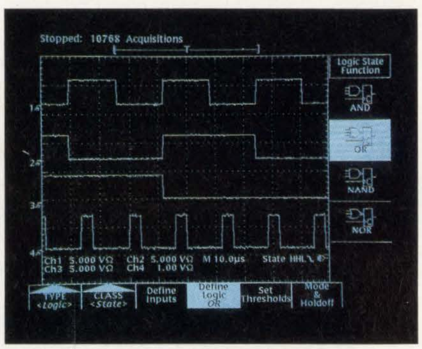

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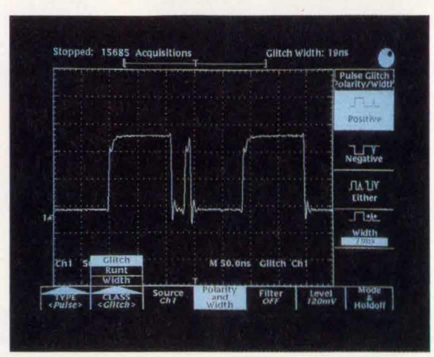
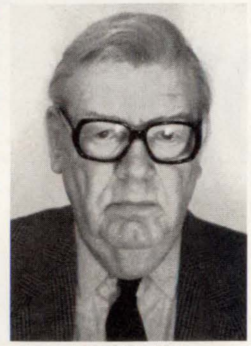


PRODUCTION TECHNOLOGY: A GLOBAL VISTA



JOHN GOSCH
FIELD EDITOR

From November 12 to 16, Munich, Germany, will again host one of the world's biggest production-technology shows—Productronica. More than 1600 exhibiting firms from over 25 countries will display their wares at the Bavarian capital. An estimated 80,000 visitors from around the world will have the chance to listen to technical-paper presentations and roam the 20-odd exhibit halls on Munich's sprawling fairgrounds. The biennial show provides an excellent view of the current trends and future outlook for the systems, tools, and materials needed to fabricate, assemble, and test microelectronic components, pc boards, and hybrid integrated circuits. Here are a few of those trends, based on pre-show interviews with some of the leading Productronica exhibitors:

In semiconductor-device manufacture, semiconductor-processing experts once felt that 64-Mbit DRAMs would require a new technology during the 1990s, with X-ray lithography the best candidate because of its shorter-than-light wavelengths. Ten years ago, 0.8 µm was considered the limit for photolithography.

However, announcements set for this year's show indicate that photolithography will continue to play a dominant role in producing chips in volume quantities. The experts now seem convinced that photolithography will hold its ground at least until the turn of the century. Today, 64-Mbit DRAMs are being made with "conventional" photolithography. For this process, engineers use phase shifting, a clever technique that's still difficult to employ in mass production. Combined with the shorter wavelengths of laser-generated ultraviolet light and better demagnification lenses and photosensitive materials, the technique should make it possible to eventually fabricate circuits with 0.2-µm, or even 0.1-µm, line spacing.

Automatic test equipment is of growing concern for both makers and users of semiconductor devices. Though past emphasis in ATE development was on software, the focus has now shifted to equipment that helps cut the error rate in components production. ATE will become an integrated part of a device production process, rather than being misused as a tool for merely determining device output. As for board testers, the demand is for simpler operation and for systems that can cope with the growing diversity of pc boards. Users are apt to fall back more and more on in-circuit testers that allow fast programming, whereas function testers will be used only in exceptional cases. In logic testers, a technological transition is taking place, as speeds of 100 MHz are no longer adequate and device pin counts up to 512 aren't unusual.

According to industry analysts, surface-mounting technology is now accelerating toward use of ASICs, multichip modules, and tape-automated bonding. In addition, image processing and visual display systems are taking over jobs in the surface-mounting assembly process, including placement, screen printing, soldering, and repair. Furthermore, continued efforts in standardization, such as a common soldering standard, should result in greater use of surface-mounting technology in military and aerospace applications.

Experts anticipate continued problems with cleaning equipment and materials until the electronics industry agrees to use environmentally safe solvents and non-corrosive fluxes, as well as soldering pastes that don't require cleaning. But it's also likely that soldering technology itself will speed the trend to environmental safety, with flux systems using convection or infrared heating in an inert-gas atmosphere.

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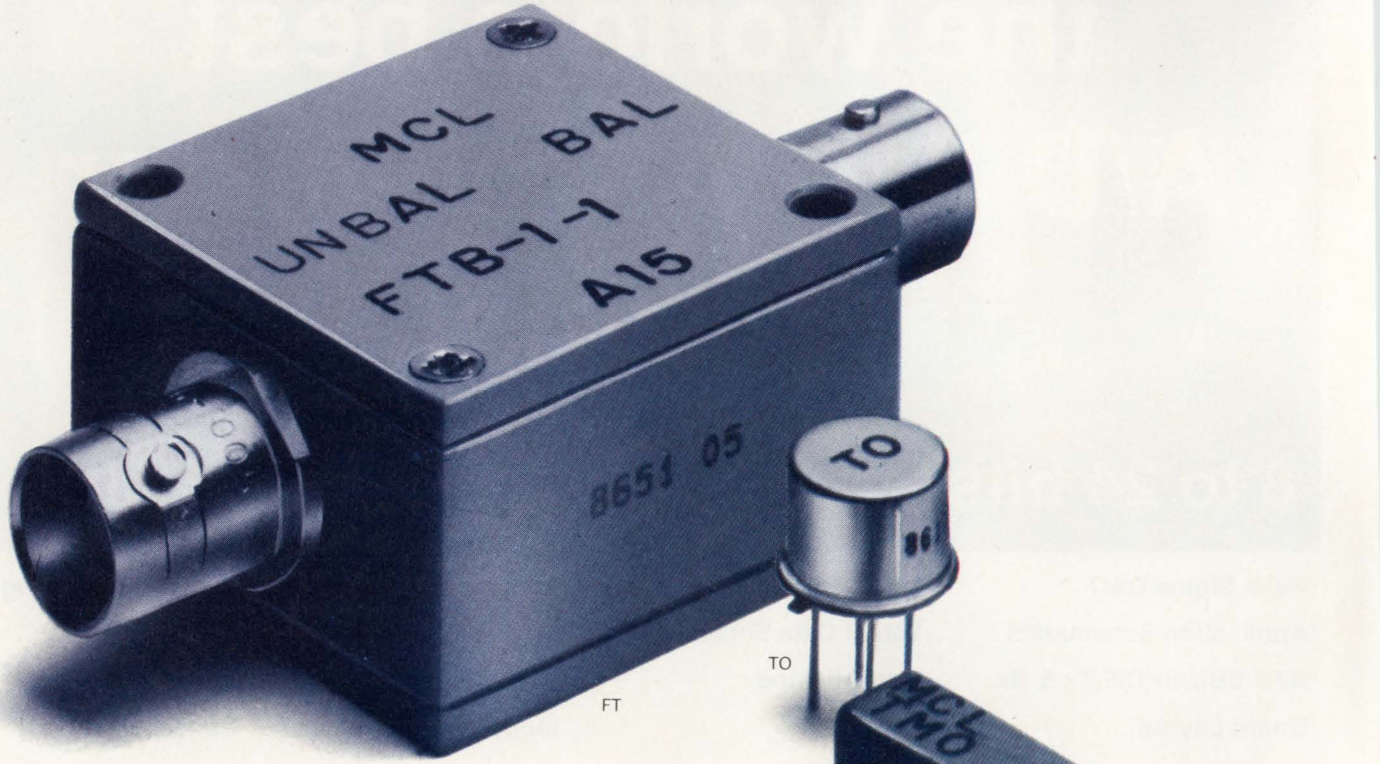

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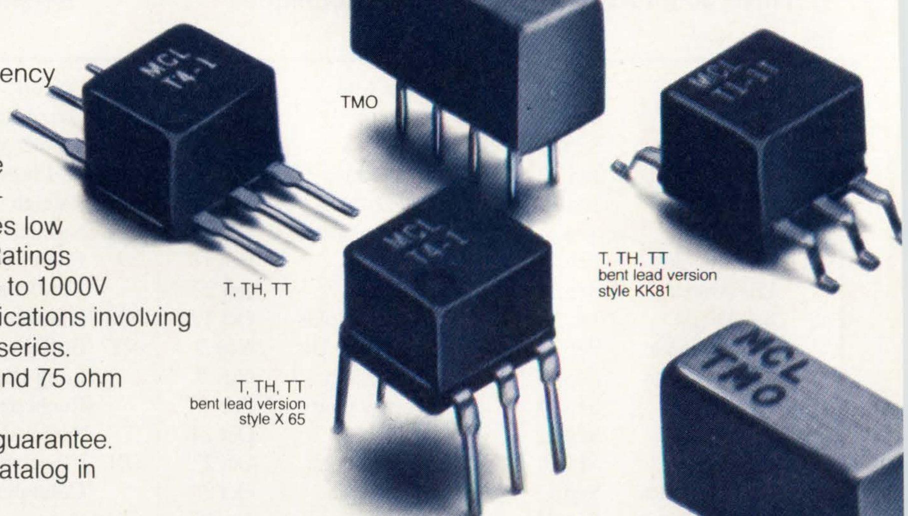

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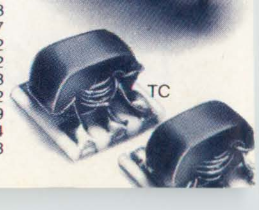

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T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
TMO1-1	5950-01-178-2612	TMO16-1	5950-01-138-4593

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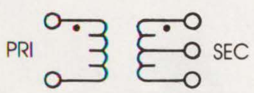
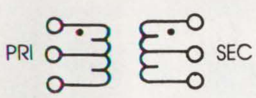
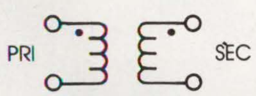
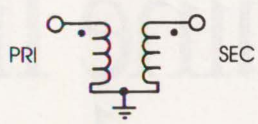
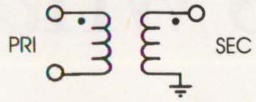
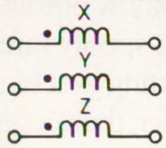
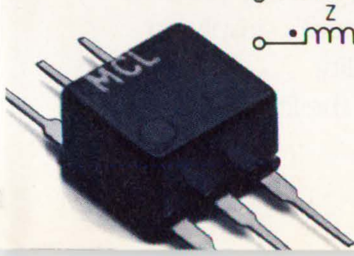
case style number see opposite page		MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS 3dB MHz	2dB MHz	1dB MHz	PRICE $ Qty. (1-9)
A* 	T	T1-1T	1	.05-200	.05-200	.08-150	.2-80	4.45
		T1-6T	1	.003-300	.003-300	.01-150	.02-50	6.95
		T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.95
		T2.5-6T	2.5	.01-100	.01-100	.02-50	.50-20	4.95
		T3-1T	3	.05-250	.05-200	.1-200	.5-70	4.95
		T4-1	4	.2-350	.2-350	.35-300	2-100	3.25
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	4.45
		T5-1T	5	.3-300	.3-300	.6-200	.5-100	4.95
		T8-1T	8	.03-140	.03-140	.10-90	1-60	7.95
		T13-1T	13	.3-120	.3-120	.7-80	5-20	4.95
		T16-6T	16	.03-75	.03-75	.06-30	.1-20	5.65
	TH	T4-1H	4	10-350	10-350	15-300	25-200	5.95
	TMO	TMO1-1T	1	05-200	.05-200	.08-150	.2-80	7.95
		TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	8.45
		†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	8.45
		†TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	7.95
		TMO4-1	4	.2-350	.2-350	.35-300	2-100	6.25
		TMO5-1T	5	.3-300	.3-300	.6-200	5-100	8.45
		TMO13-1T	13	.3-120	.3-120	.7-80	5-20	8.45
B* 	TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	6.95
		TT1.5-1	1.5	.075-500	.075-500	.2-100	1-50	5.95
		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	6.45
		TT4-1	3	.05-200	.2-50	.2-50	1-30	5.95
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95
		TT25-1	25	.02-30	.02-30	.05-20	.1-10	9.95
	TTMO	TTMO25-1	25	.02-30	.02-30	.05-20	.1-10	11.95
		TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	11.45
		TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95
C 	T	T1-1	1	.15-400	.15-400	.35-200	2-50	3.25
		T1.18-3	1.18	0.01-250	0.01-250	0.02-200	0.03-50	5.65
		T1-6	1	.01-150	.01-150	.02-100	.05-50	5.65
		T1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	4.45
		T1.5-6	1.5	.02-100	.02-100	.05-50	0.1-25	5.65
		T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	4.45
		T4-6	4	.02-200	.02-200	.05-150	.1-100	4.45
		T9-1	9	.15-200	.15-200	.3-150	2-40	3.95
		T16-1	16	.3-120	.3-120	.7-80	5-20	4.45
		T36-1	36	.03-20	.03-20	.05-10	.1-5	6.95
	TO	TO-75	1	10-500	—	10-500	40-250	6.95
	TH	T1-1H	1	8-300	8-300	10-200	25-100	5.95
		T9-1H	9	2-90	2-90	3-75	6-50	6.45
		T16-H	16	7-85	7-85	10-65	15-40	6.45
	TMO	TMO1-02	1	1-800	1-800	2-500	—	9.45
		TMO1-1	1	.15-400	.15-400	.35-200	2-50	6.25
		TMO1.5-1	1.5	.1-300	.1-300	.2-150	.5-8	8.45
		†TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	7.95
		†TMO4-6	4	.02-200	.02-200	.05-150	.1-100	7.95
		TMO6-1	6	.3-200	.3-200	.5-150	5-50	7.95
		TMO9-1	9	.15-200	.15-200	.3-150	2-40	7.95
		TMO16-1	16	.3-120	.3-120	.7-80	5-20	7.95
D 	T	T2-1	2	.050-600	.050-600	.1-400	.5-200	3.95
		T3-1	3	.5-800	.5-800	2-400	—	4.45
		T4-2	4	.2-600	.2-600	.5-500	2-250	3.95
		T8-1	8	.15-250	.15-250	.25-200	2-100	3.95
		T14-1	14	.2-150	.2-150	.5-100	2-50	4.95
	TMO	TMO2-1	2	.050-600	.050-600	.1-400	.5-200	7.95
		TMO3-1	3	.5-800	.5-800	2-400	—	8.45
		TMO4-2	4	.2-600	.2-600	.5-500	2-250	7.95
		TMO8-1	8	.15-250	.15-250	.25-200	2-100	7.95
		TMO14-1	14	.2-150	.2-150	.5-100	2-50	8.45
	FT	FT1.22-1	1.22	.005-100	.005-100	.01-50	.05-25	35.95
		FT1.5-1	1.5	.1-400	.1-400	5-200	1-100	35.95
E 	FTB	FTB-1	1	.2-500	.2-500	.5-300	1-100	36.95
		FTB1-6	1	.01-125	.01-125	.05-50	.1-25	36.95
		■FTB-1-75	1	.5-500	.5-500	5-300	10-100	36.95
F 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25
		T626	1	0.01-10	0.01-10	0.2-5	.04-2	3.95



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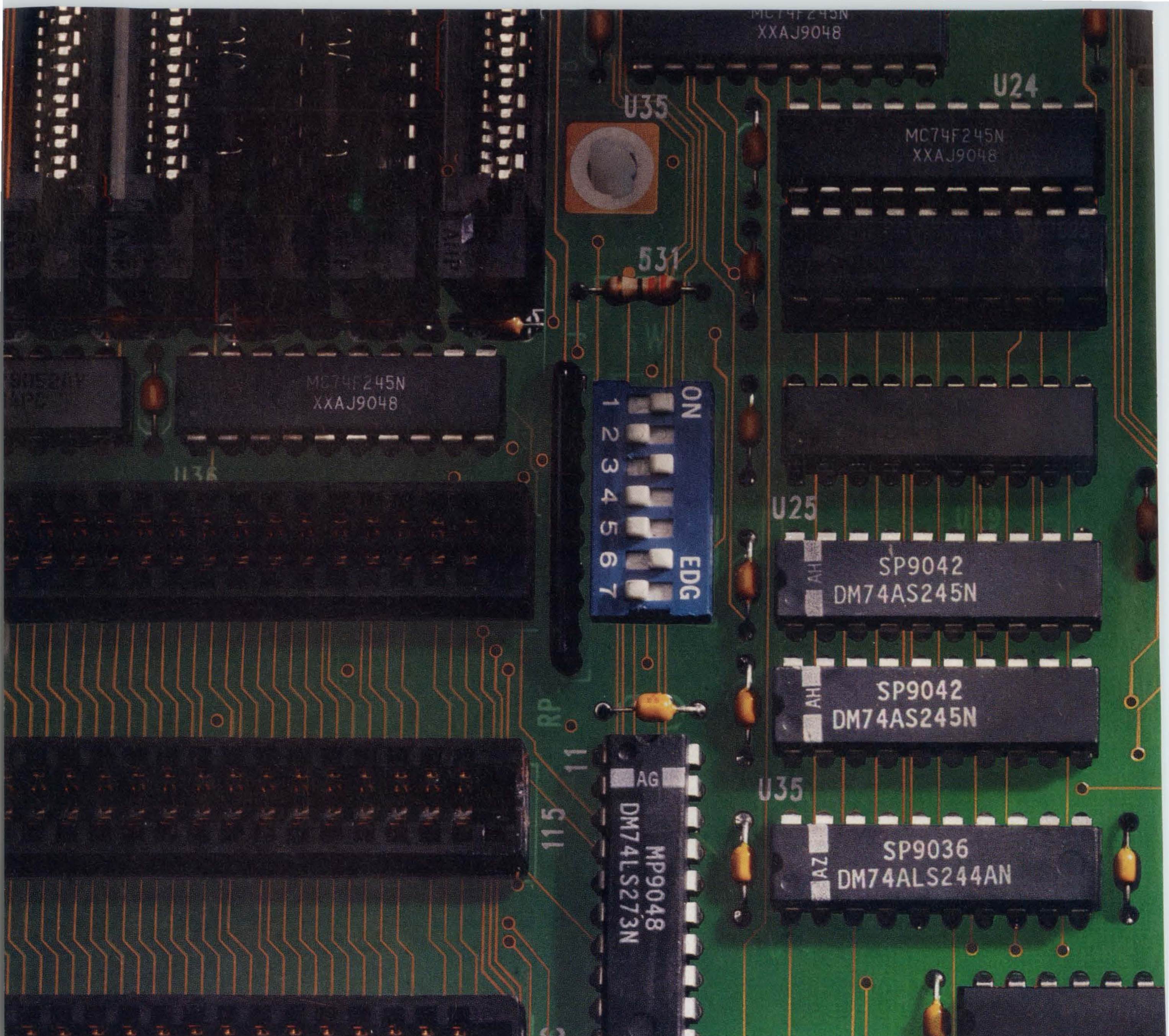
CIRCLE 168 FOR U.S. RESPONSE **CIRCLE 169 FOR RESPONSE OUTSIDE THE U.S.**



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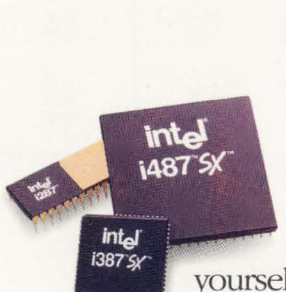

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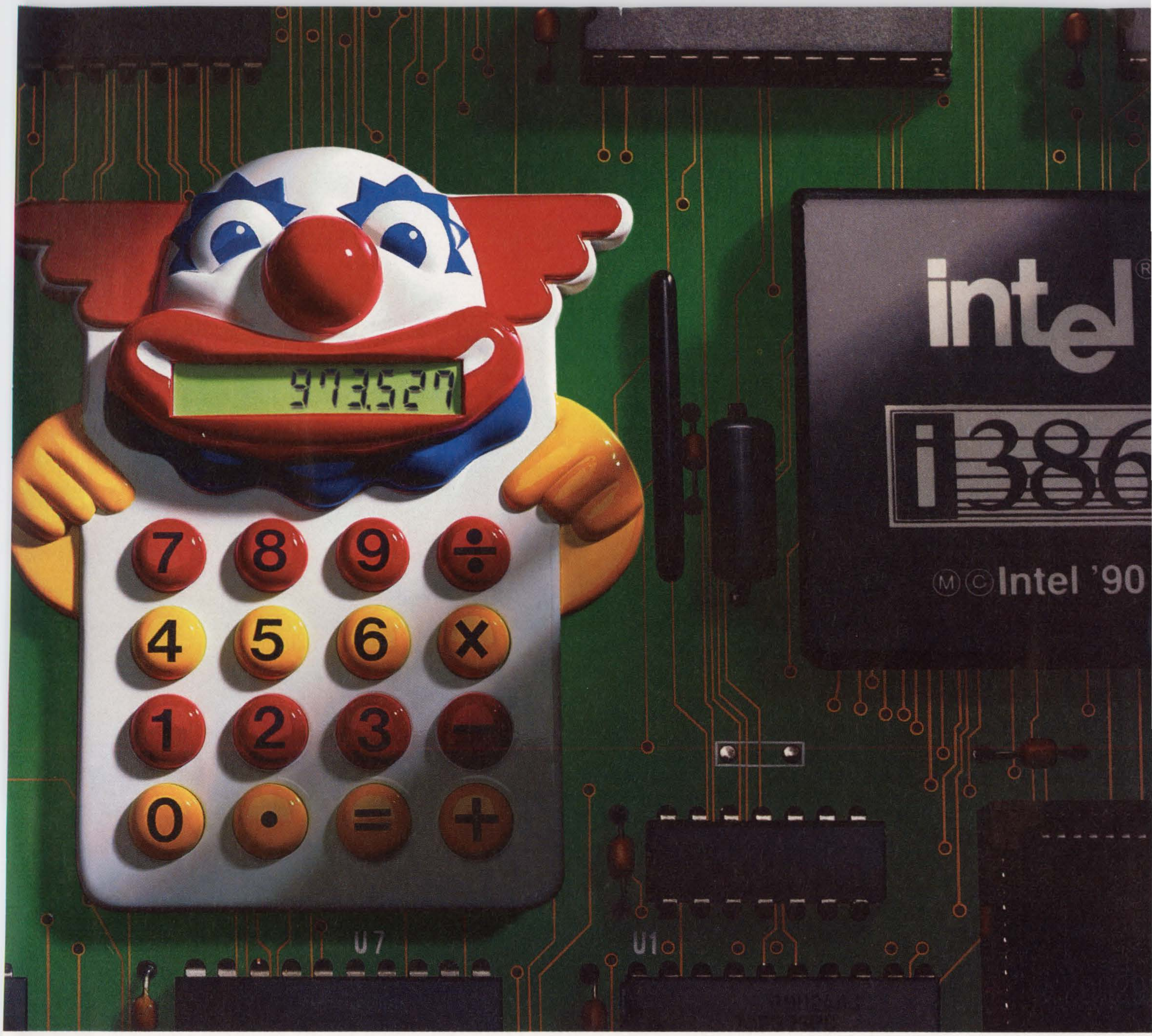

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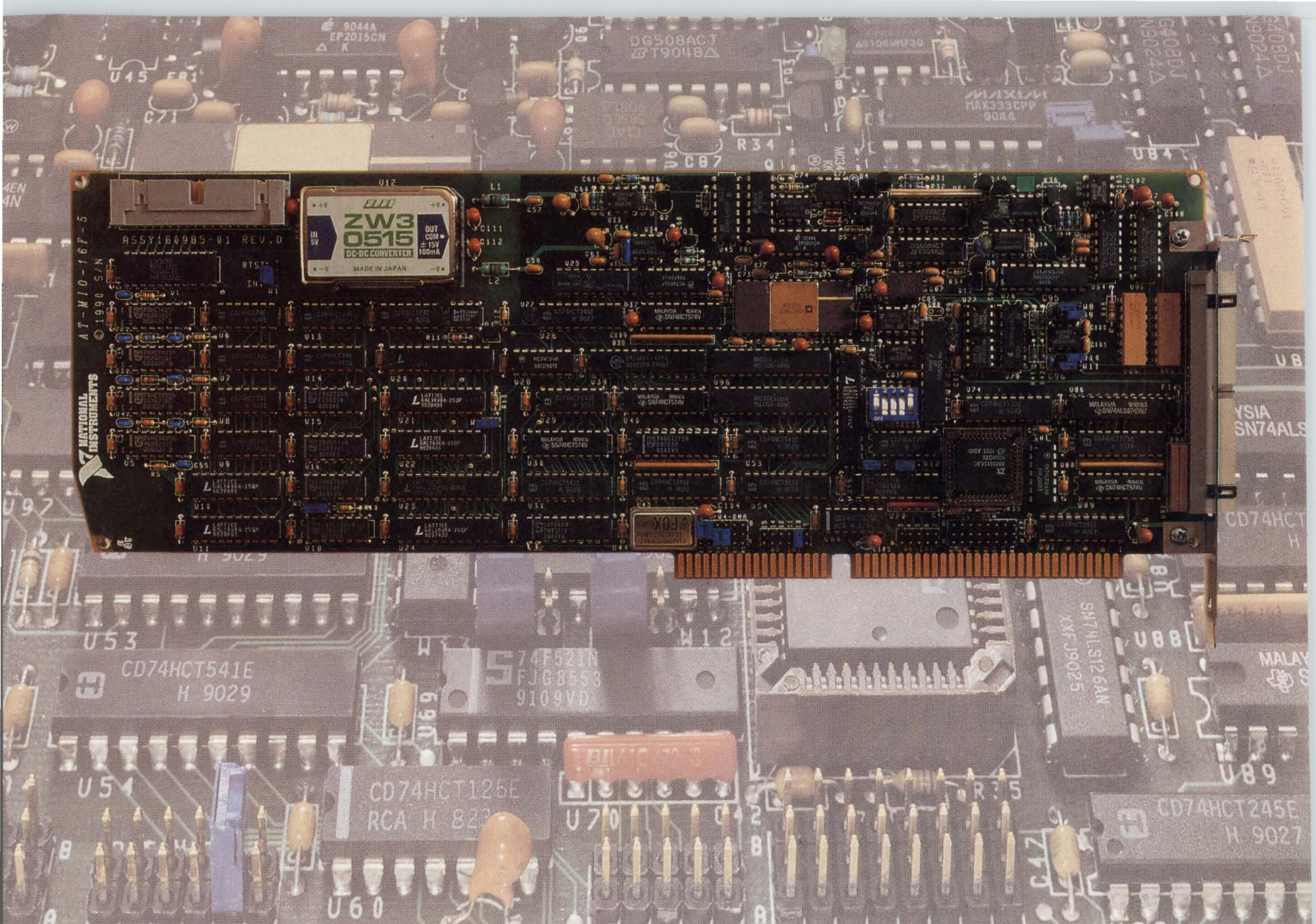
CIRCLE 1



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		ANALOG INPUT					ANALOG OUTPUT				SOFTWARE					
Data Acquisition Board	Computer Bus	Channels*	Max Sampling Rate (samples/sec)	Resolution (bits)	Ranges (V)	Gains	Channels	Resolution (bits)	Digital I/O Channels	Counter/Timers	LabWindows	LabDriver for DOS	LabDriver for Windows	Measure	VisionScope	Third Party
EISA-A2000	EISA	4 SE SS	1,000,000	12	±5	1	–	–	–	–	✓	✓	✓		✓	
AT-MIO-16F-5	AT	16 SE 8 DI	200,000	12	±5, 0 to 10	0.5, 1, 2, 5, 10, 20, 50, 100	2	12	8	3	✓	✓	✓			✓
AT-MIO-16H-9 AT-MIO-16H-25	AT	16 SE 8 DI	100,000	12	±10, ±5, 0 to 10	1, 2, 4, 8	2	12	8	3	✓ ✓	✓ ✓	✓ ✓	✓ ✓		✓ ✓
AT-MIO-16L-9 AT-MIO-16L-25	AT	16 SE 8 DI	100,000	12	±10, ±5, 0 to 10	1, 10, 100, 500	2	12	8	3	✓ ✓	✓ ✓	✓ ✓	✓ ✓		✓ ✓
Lab-PC	XT	8 SE	62,500	12	±5, 0 to 10	1, 2, 5, 10, 20, 50, 100	2	12	24	3	✓	✓	✓	✓		✓
PC-LPM-16	XT	16 SE	50,000	12	±5, 0 to 10 ±2.5, 0 to 5	1	–	–	16†	3	✓	✓	✓			
AT-DIO-32F PC-DIO-96 PC-DIO-24	AT XT XT	– – –	– – –	– – –	– – –	– – –	– – –	– – –	32 96 24	– – –	✓ ✓ ✓	✓ ✓ ✓	✓ ✓ ✓			✓ ✓
PC-TIO-10	XT	–	–	–	–	–	–	–	16	10	✓	✓	✓			

* SE – Single-Ended, DI – Differential, SS – Simultaneous Sampling

† 8 Channels In, 8 Channels Out

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CIRCLE 176 FOR U.S. RESPONSE **CIRCLE 177 FOR RESPONSE OUTSIDE THE U.S.**

No-Clean Flux Method Beats Low-Yield Barrier

The two largest barriers hampering the acceptance of no-clean fluxing techniques—low process yields and flux residue—have fallen to a new no-clean flux technique for hand soldering of electronic assemblies. The technique involves dispensing a liquid-flux product onto the joint and finishing it with a solid-core 63/37 roll solder. Unlike current no-clean methods that use a hollow-core solder with flux incorporated within it, the new technique maintains high process yields and completely removes flux residue, which can create cosmetic problems as well as testability bugs. The technique was developed by Pensar Corp., Appleton, Wis. Contact Stan Plzak at (414) 278-7788. *DM*

CAE, IC Firms Target ASIC Environment

An open, top-down, framework-based design environment for ASIC designers is the goal of a joint development between Texas Instruments, Dallas, and Cadence Design Systems Inc., San Jose, Calif. TI will contribute synthesis and logic-simulation libraries, as well as design-analysis tools, to support the design process of its TGB1000 biCMOS ASICs. Cadence will provide the framework and design tools. The two companies are working with "teaching customers" to develop a system that will be practical for designers. The finished product will be the TGB1000 Amadeus Design Kit. It will let clients take advantage of an open design environment without compromising vendor-specific design rules. The TGB1000 Amadeus Design Kit will ship by the end of the year on HP/Apollo and Sun workstations. Call Texas Instruments at (800) 336-5236, ext. 700, in the U.S. and (214) 995-6611, ext. 700, outside the country. *LM*

Display Consortium Spans Flat-Panel Field

A consortium of U.S. flat-panel-display manufacturers has been formed with a focus on automated inspection and repair technologies, as well as generic technologies for interconnections and packaging. The nine-member group is called the American Display Consortium and includes Cherry Display Products, Electro-Plasma Inc., Magnascreen, Optical Imaging Systems, Photonics Imaging Inc., Planar Systems, Plasmaco Inc., Standish Industries, and Tektronix Inc. Every member designs and manufactures products for all major branches of the flat-panel market, including electroluminescent, gas-plasma, and active- and passive-matrix LCDs. The consortium will be administered by the Microelectronics and Computer Technology Corp., Austin, Texas. Its research is being funded by a $7.5 million grant from the U.S. Department of Commerce's National Institute of Standards and Technology's Advanced Technology Program. *DM*

Standards Appear For CAD Framework

The Technology CAD (TCAD) Framework Group, part of the CAD Framework Initiative, Austin, Texas, recently demonstrated working prototypes of its first two proposed standards. TCAD tools include CAE for semiconductor device and process design, technology characterization for circuit design, and IC design for manufacturability. For instance, modeling fabrication processes falls under TCAD. The first standard, a semiconductor-wafer-representation standard, models semiconductor devices and wafers at the physical level, describing such characteristics as material geometries, dopant concentrations, and electric fields. The second standard, a semiconductor-process-representation standard, describes the processes used to manufacture ICs. The TCAD Framework Group has representatives from TCAD-software vendors; universities; and IC, computer, and communication-products manufacturers. The organization is developing standards that will allow TCAD tools to operate with each other and with other EDA tools without the large investment currently required to link them. For more information, call the group's chairman, Wally Dietrich, at the IBM Research Div. at (914) 945-2073. *LM*

Texas Instruments, GE, Join Onchip Packaging

Extremely short and dense chip-to-chip interconnections are the key to an advanced chip-packaging technology developed by General Electric Co., Schenectady, N.Y., and now to be commercialized by Texas Instruments, Dallas. Under an agreement between the two companies, TI will produce and market digital and analog multichip modules based on GE's high-density-interconnect (HDI) process. According to Dr. Kenneth A. Pickar, manager of the GE R&D Center's Electronic Systems Research Center, the tremendous gains in the speed and power of microchips is bottled up by outmoded packaging approaches. The HDI process exploits the "closer-is-better" rule and permits a

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1.8-In. Hard Drive Hits The Street

The 1.8-in. hard-disk drive has arrived—and ahead of schedule. As reported earlier (ELECTRONIC DESIGN, *July 11, p. 27)*, the 20-Mbyte drive, called the Mustang 1820, is a single-platter unit, while the Stingray 1842 is a dual-platter drive that holds 40 Mbytes. These drives should make a significant impact in the notebook and palmtop computing environments. The Mustang measures just 50.88 by 76.85 by 15 mm. According to Intégral Peripherals Inc., Boulder, Colo., the drives' manufacturer, the Mustang drive's overall height could be reduced further to 10 mm by separating the head-disk assembly from the drive electronics. In this configuration, the pc board can be incorporated into the system's motherboard. Another feature of the Mustang is its low power consumption: 0.5 W in the power-savings mode and 15 mW in the sleep mode. The drive, which weighs just 95 g, recovers from the sleep mode in less than one second. *RN*

Better GaAs Models Improve Spice Runs

Engineers simulating high-speed systems and components with the HSpice simulator from Meta-Software, Campbell, Calif., can accurately model GaAs devices with TriQuint's Own Model (TOM) from TriQuint Semiconductor, Beaverton, Ore. TOM accurately represents MESFET devices, correcting deficiencies in existing Spice models while adding several features unique to GaAs. For instance, with current Curtis and Raytheon/Statz Spice models, drain conductance can only be fitted for a small range of drain-current values. Consequently, when drain current falls outside this narrow range, predictions of conductance are inaccurate. If the drain current falls below this range, predicted conductance is too small, and if the current is above the range, drain conductance is too large. An HSpice simulation using TOM overcomes these deficiencies by making pinch-off voltage a function of drain voltage. A data parameter further improves the fit to accurately predict small-signal parameters over many bias conditions. For more information, call Meta-Software at (800) 346-5953. *LM*

Electro-Optical Board Speeds Interconnections

A method for embedding fine optical fibers in complex, geometric patterns on planar substrates to form high-speed links between optical components has been developed. The technology will be demonstrated by Advanced Interconnection Technology Inc., Islip, N.Y., at the International Electronics Packaging Conference, in San Diego, Calif., Sept. 15-19. The interconnection technology permits fibers as fine as 50 μm to cross each other without damage to the sensitive fiber cladding. *DM*

VHDL Users, Vendors, Set To Meet Next Month

"Enabling Design Creativity" is the theme of the fourth annual VHDL Users' Group meeting taking place from Oct. 27-30 in Newport Beach, Calif. The technical program includes language tutorials and user and vendor presentations, including a 1992 standardization panel. There will also be three days of vendor exhibits. For more information, call the VHDL Users' Group, c/o Conference Management Services, at (415) 329-0510. The voice-mail information number is (415) 329-8673. *LM*

Three More Firms Join FPGA Alliance Group

Three additional companies—Aldec, Gould/AMI, and Teradyne EDA—have joined Actel's Industry Alliance Program, which was established to foster technical relationships and cooperative marketing efforts. Actel Corp., Sunnyvale, Calif., provides members with their FPGA design software for product development, and technical assistance in the development of Actel product support. Furthermore, Actel is working with members for cross-training of sales forces, joint product literature, customer product demonstrations, and other marketing activities. Other Alliance companies include Cadence Design Systems, LSI Logic, Mentor Graphics, and Valid Logic. For more information, call (408) 739-1010. *LM*

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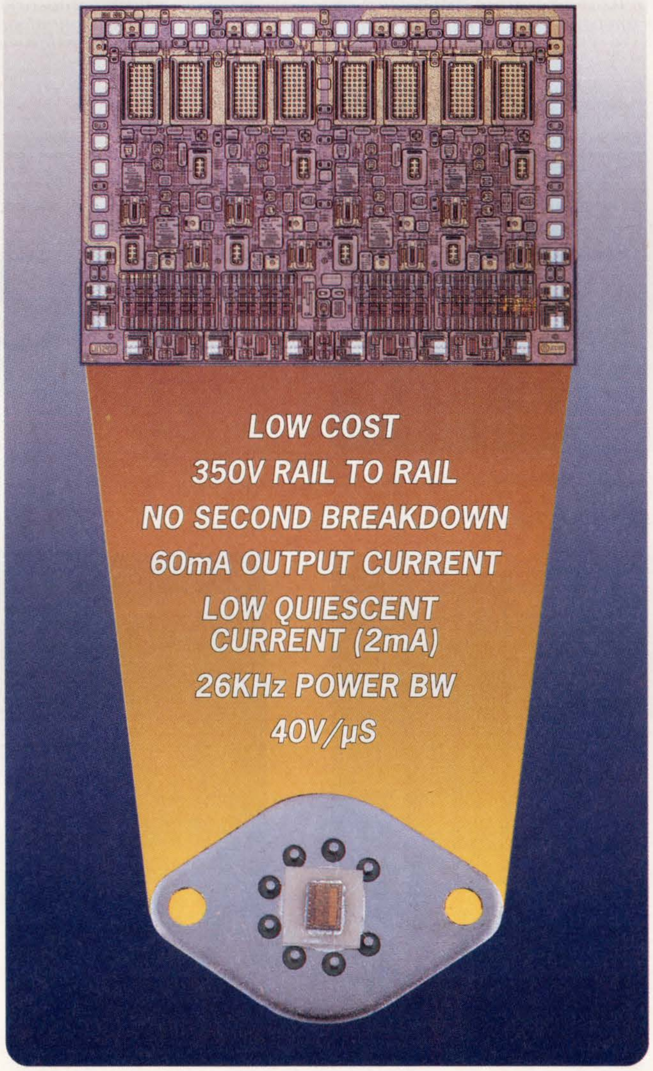

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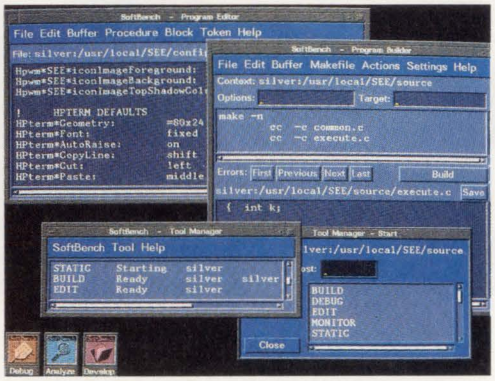
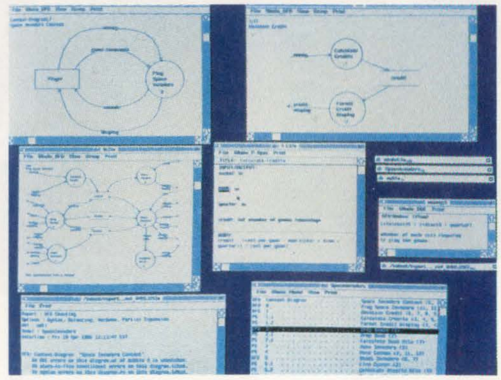
CIRCLE 92 FOR U.S. RESPONSE

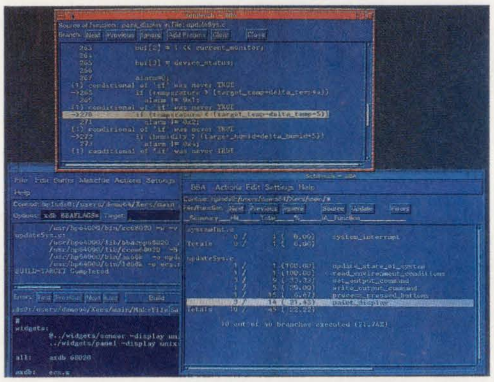
CIRCLE 93 FOR RESPONSE OUTSIDE THE U.S.



HP's SoftBench: A tool integration framework and a program construction toolset.



Cadre Teamwork: A family of tools that implement system analysis and software design methodologies.



HP Branch Validator: Provides accurate branch information quickly and easily, reducing software test time while increasing confidence.

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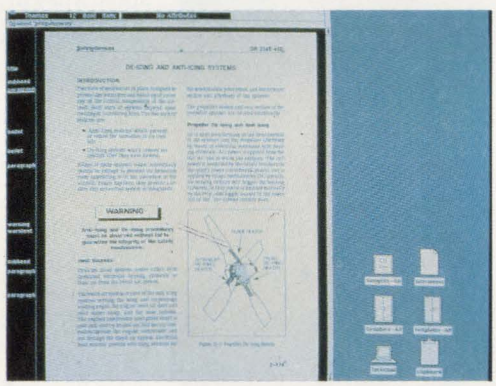
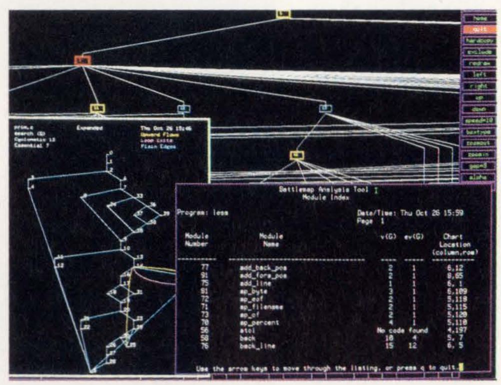
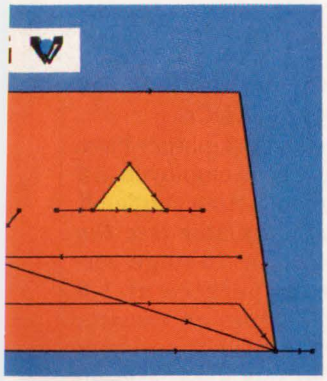


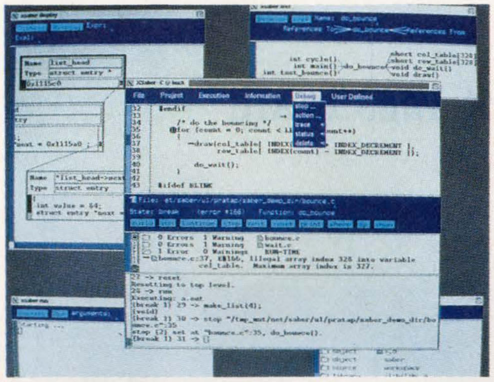
Interleaf Technical Publishing Software: A documentation software and management system that features integrated text and graphics.



McCabe Test Tools: An automated software testing and reverse engineering application.



Verilog LOGISCOPE: Automated testing of source code analysis for reverse engineering.



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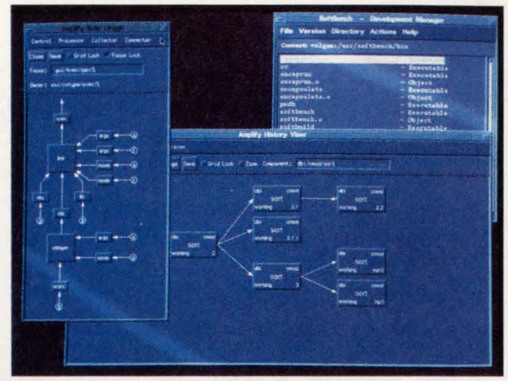

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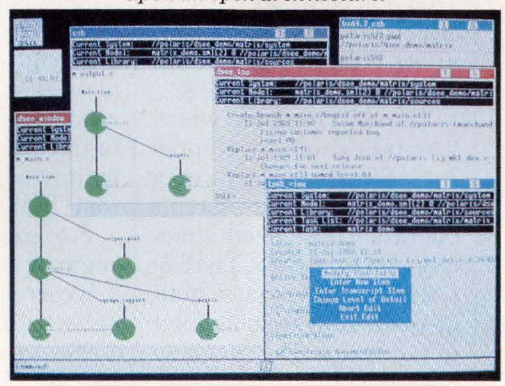

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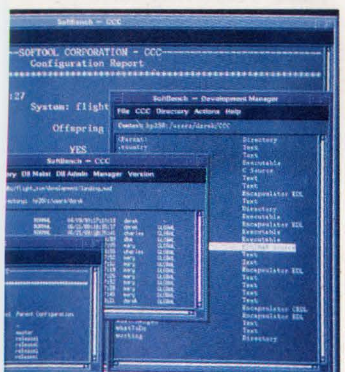
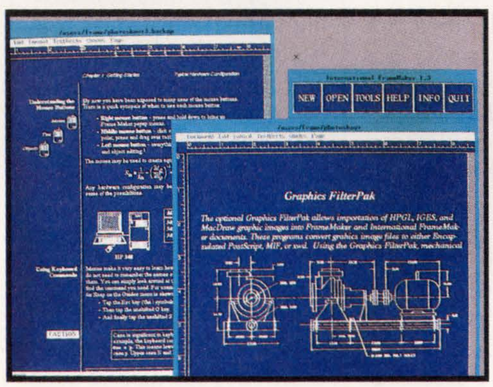


Softool Corporation CCC: A complete, automated solution for change control and configuration management.



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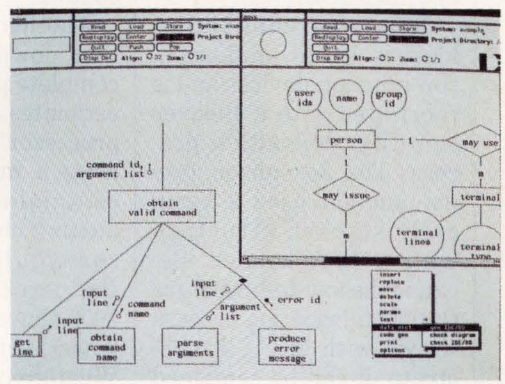

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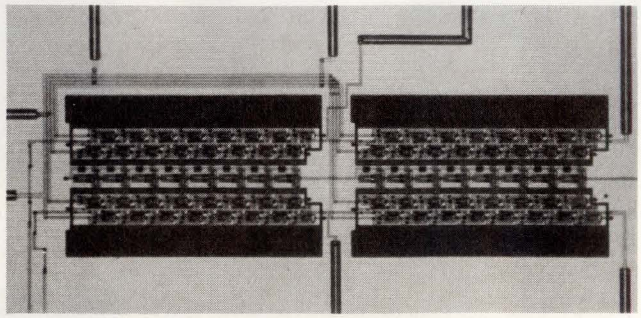
CIRCLE 152 FOR U.S. RESPONSE CIRCLE 153 FOR RESPONSE OUTSIDE THE U.S.

9.6-GHz Shift Register Blazes Trail For Superconducting Logic

A superconducting 4-bit shift-register chip that operates at 9.6 GHz and dissipates only 40 μW may be the world's fastest device of its kind. The register reaches its high speed using relatively wide 3.0-μm geometries. That's in contrast to GaAs circuits, which typically require 0.5-μm geometries for similar performance.



The shift register, which was fabricated by Hypres Inc., Elmsford, N.Y., may actually go faster—circuit operation has been simulated up to 25 GHz. The 9.6-GHz clock rate was a limit of the test system and not of the device. The company is expanding its test capability to accommodate higher speeds. The circuit operates at 4K.

The superconducting logic is based on Josephson-junction devices and is fabricated with a 10-layer thin-film deposition process. The Josephson tunnel-junction uses a vertically stacked structure with a 10-Å barrier. Because the low-temperature (150°C) fabrication process works with any flat substrate, it can be combined with silicon and GaAs technologies. The entire process-fabrication cycle is five days.

The four-bit shift register isn't intended as a standalone product, nor would it typically be dropped into an existing system. According to Edwin Stebbins, director of advanced programs, "To commercialize superconducting microelectronics, the cooling and interface requirements dictate that we build reasonably complete subsystems." In fabricating superconducting logic, the company ultimately hopes to offer custom OEM subassemblies.

For example, the shift register is a basic element in a correlator. A complete subsystem might include a 4096-stage correlator running at 10 GHz, which has applications in a military-communication or radar system.

Another goal, albeit further down the road, is a complete processor. Initial estimates are that a RISC-processor core could comprise a multichip module containing 16 superconducting chips. The processor would use a 500-ps first-level cache and have 1000 times the processing power of the VAX 11/780. What's more, it would need just 500 mW for the active circuitry.

The 4-bit shift register's operation verifies Hypres' circuit design for building logic devices, which uses edge-triggered logic. That logic is characterized by a two-phase rather than a three-phase clock and by wide operating margins. Two-phase clocks are easier to generate than three-phase clocks.

Hypres is also fabricating high-density shift registers and has demonstrated functional operation of 80-, 160-, 512-, and 700-bit shift registers. None, however, have yet been tested at high speeds.

These shift registers also use edge-triggered logic, and are suitable for building digital-signal processors operating at 10 GHz. They can also be used as storage devices for high-speed ADCs.

The shift registers have already been employed in a superconducting single-bit digital correlator *(see the figure)*. The 16-stage correlator operates at 1.6 GHz. The design consists of two 16-bit shift registers with an XOR gate between each bit of both shift registers. The XOR outputs are added to produce a sum-of-products output. The company is now testing a 128-stage correlator of similar design.

The correlator can serve in secure communications and low-probability-of-intercept (LPI) radar applications. The correlation process detects a signal from several multiple low-power components spread broadly across the spectrum. Because the individual signal components each have relatively low power, they're difficult to distinguish from noise when separate.

Part of this work is being done under contract to Rome Laboratories, Hanscom AFB, Mass., and is funded by the Strategic Defense Initiative Organization. For more information, call Edwin Stebbins at (914) 592-1190, ext. 7821.

DAVID MALINIAK

CPU-To-CPU Bus Suits High-Speed Multiprocessing

In desktop/deskside computer systems, designers have a choice of I/O buses—XT, AT, EISA, Microchannel, NuBus, SBus, Turbochannel, etc. However, there's no standardized intermediate bus that allows CPU-to-CPU communication when multiple processors must communicate. Some companies have created dedicated local buses or a direct processor bus, but such buses have limited expandability and do not support symmetrical multiprocessing. Furthermore, because each bus is proprietary, each has only garnered a small following of users.

To counter each of the negatives while offering designers a high-performance bus for symmetric multiprocessing, Corollary Inc., Irvine, Calif., has placed the technical bus description for its third-generation C-bus, the C-bus II, into the public domain. The company will also make available the symmetric in-

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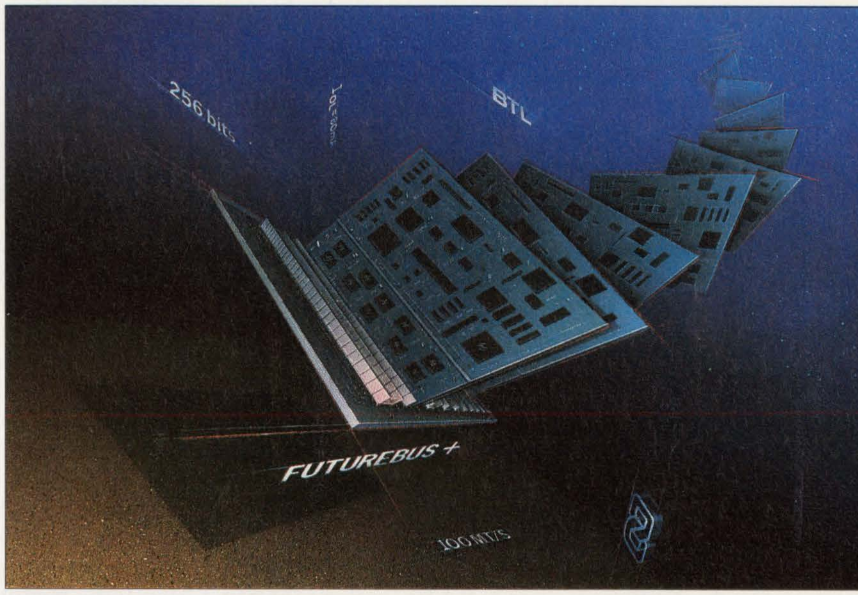

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tegrated multiprocessor logic (SIMPL) chip set—a pair of ICs that eliminates just about all of the interface glue logic needed to build bus-compatible boards. The multiplexed and synchronous C-bus II keeps the number of control signals small—less than five each for control and arbitration operations. It also employs a fair arbitration scheme, such as employed on NuBus and Multibus II, eliminating any idle time during arbitration.

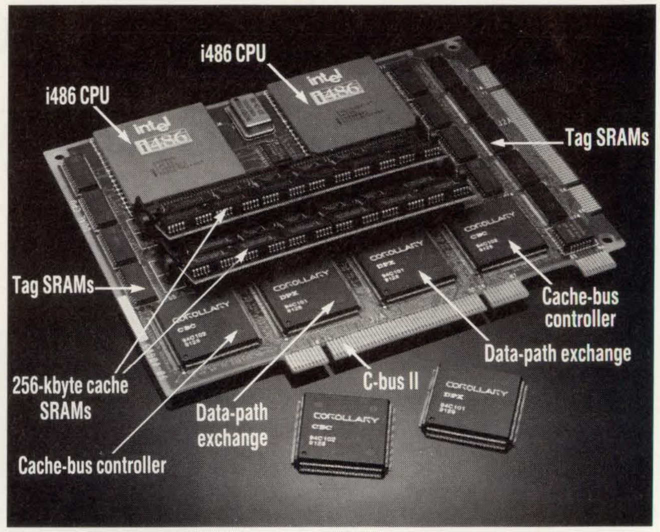
The C-bus II supports up to 16 modules, each of which could have two CPUs (such as Intel 80486 microprocessors). There can be as many as 30 logical CPUs on the bus. Realistically, though, the bus bandwidth for linear performance increases would limit the number to about 16 actual 50-MHz i486 processors, each with 256 kbytes of cache. Some compute-bound problems could use a larger number of CPUs without hitting the bandwidth limits. Any-speed processor can be supported by the bus thanks to the SIMPL chip set that decouples the CPU speed from the bus.

Data transfers occur over the C-bus II's 64-bit-wide data bus at burst rates of 267 Mbytes/s. Error checking and correction bits protect the data and address bus contents from noise and other signal hazards. A 2-Gbyte physical address space lets the bus handle large applications with ease. The bus can also readily support processors other than the i486, such as the MIPS R4000 or other RISC or CISC CPUs.

Two basic 208-lead chips tie the CPU boards into the bus. One of them is called the data-path exchange (DPX) circuit, which manages a 32-bit section of the 64-bit data bus. The other chip, called the cache and bus controller (CBC), controls an off-chip second-level cache of 256 kbytes to 1 Mbyte for each CPU and manages small, third-level caches for each processor. Those level-3 caches are part of the logic in the DPX chip. In a one-CPU card, two DPX chips and one CBC chip are needed to tie the processor to the bus. For dual CPU cards, just a second CBC must be added to the logic. Samples of the chips will be ready in the first quarter of 1992.

CPU cards that attach to C-bus II will typically contain one or two CPUs and the associated cache memory, cache tags, and control logic *(see the figure)*. Both the data cache and the tag RAMs include parity checking to ensure data integrity. These second-level direct-mapped caches implement the MESI protocol, and employ a write-back strategy for data updates. The CBC chip contains a tagged prefetch buffer that when enabled, automatically obtains the next sequential DMA cache line. This feature uses two cache lines in the level-3 cache to maximize burst-DMA-transfer throughput. Although a direct-mapped cache is faster than a two-way set-associative cache, the direct-mapped approach suffers from many cache evictions that involve two pieces of data whose addresses have the same low-order bits (like moving data to a location 1 Mbyte away).

To overcome the cache



problem, the six-line (32 bytes/line) fully-associative level-3 cache for each processor works with the level-2 cache. The secondary/tertiary cache combination allows some common operations to be done with no evictions, thus improving performance. In contrast, a two-way cache causes evictions for each step to be performed. The level-3 cache, also known as the victim cache, saves the last six lines that were evicted from the level-2 cache, and employs a least-recently-used algorithm to replace lines if the level-2 cache sends out another line.

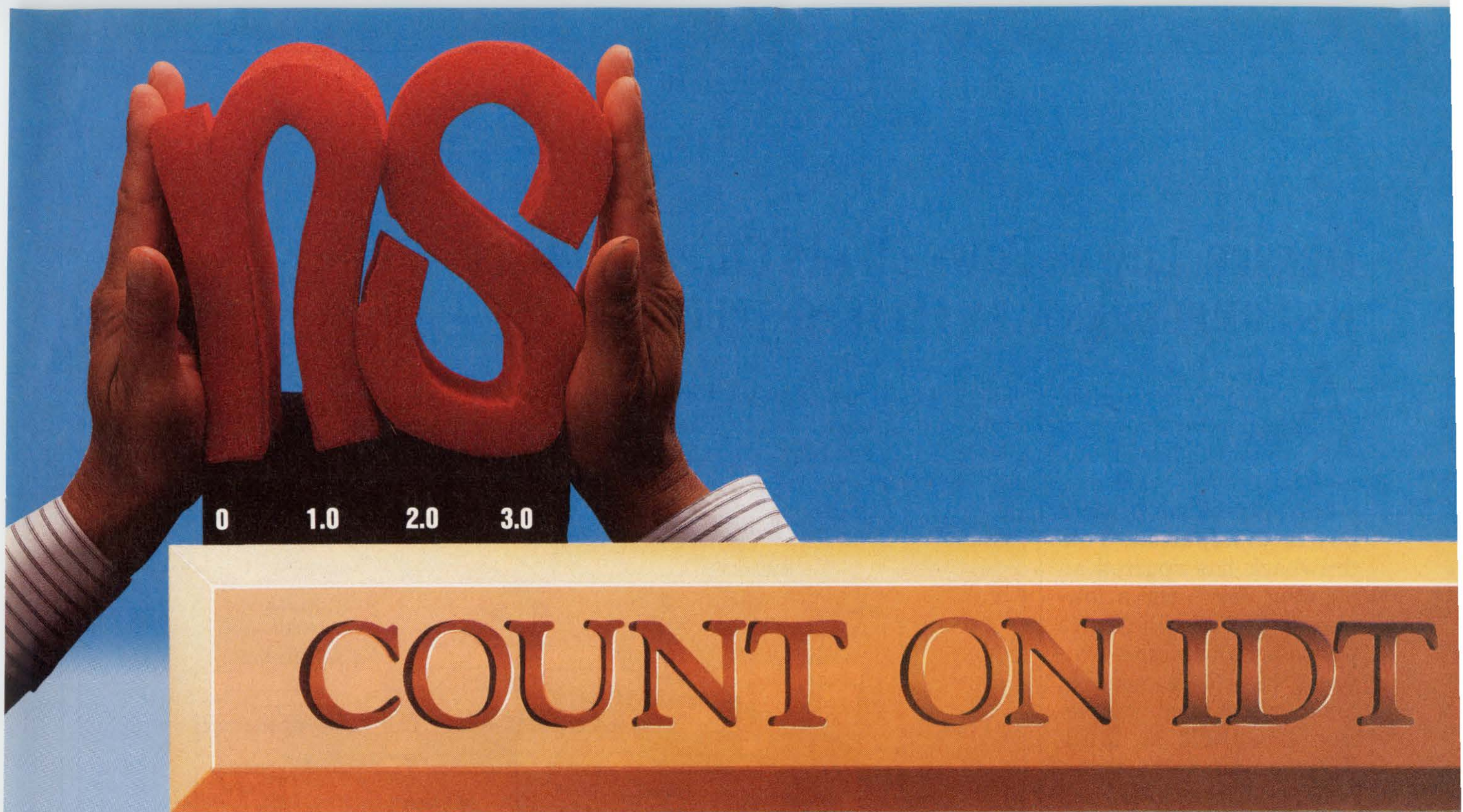
The tertiary cache also helps to I/O bridge applications in which the CPU cards connect across C-bus II and talk to an I/O card that, perhaps, connects the system to a disk controller, or another bus (EISA, for instance). The cache then serves as an array of FIFO buffers to decouple the data-transfer speed from the bus.

Unlike previous TTL buses used in PCs and workstations, the C-bus II interface employs 3.3-V signal levels to reduce the ringing and signal noise over the high-speed bus. Using 3.3-V levels eliminates the need for bus buffers on the CPU cards, further reducing the board complexity. However, the bus doesn't use the trapezoidal waveforms that Futurebus+ has adopted. When linking to other buses, such as a PC bus, a bridge interface can be implemented. Each bridge has one fixed 16-Mbyte window and two relocatable 4-Mbyte windows that view the PC bus. References to these windows are translated into PC-bus memory transactions. The address of the relocatable windows is controlled by registers located in the board's I/O space.

Corollary also developed system software to make the symmetrical processor system do productive work. The software, a modified version of standard Unix operating-system software, is offered by the Santa Cruz Operation, Santa Cruz, Calif., as the MPX Kernel.

For more information, contact George White, (714) 250-4040.

DAVE BURSKY



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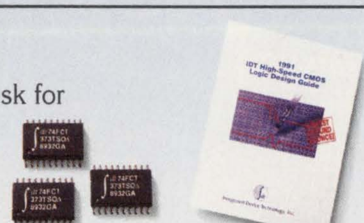

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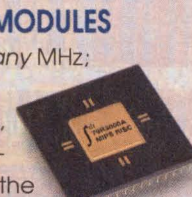

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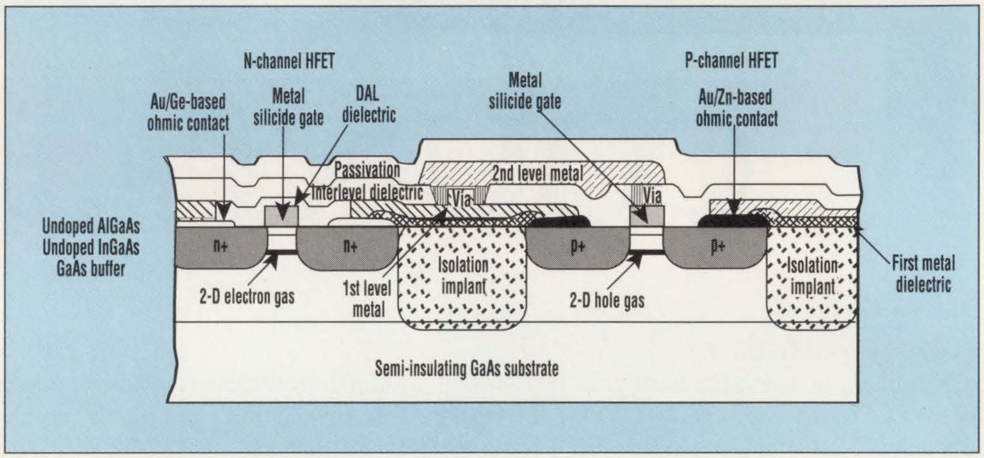
Denser, Lower-Power GaAs Chips Promised By Complementary Heterostructures

Although gallium arsenide delivers higher-performing chips over any silicon-based commercial process, it comes with the problem of high power dissipation. This drawback has spurred an ongoing quest for a low-power CMOS-like GaAs process, and some progress has been made in low-performance complementary JFET or MESFET transistor structures. Now, researchers at Honeywell Inc.'s Systems and Research Center, Minneapolis, Minn., have created a true complementary structure based on heterojunction field-effect transistors. The structure provides GaAs chip designers with the equivalent of CMOS from a circuit design viewpoint.

The devices are built as an aluminum-gallium-arsenide/indium-gallium-arsenide heterostructure, rather than bulk GaAs, to achieve higher-performing devices. As in CMOS circuit designs, significant power consumption only occurs when the transistors switch states. Thus, with reduced power, levels of chip integration can be increased, because many



more logic functions can be placed on one chip.

One recent test chip developed by Honeywell with its complementary HFET (C-HFET) process was a 4-kbit static RAM that can be accessed 250 million times per second (4 ns), yet dissipates just 100 mW. That low power consumption, according to David Tetzlaff, head of advanced microcircuits development at Honeywell, is just one-fifth that of similar GaAs memories made with noncomplementary processes.

Transistors are fabricated with molecular-beam epitaxy (MBE) deposition, which creates the precise atomic-layer regions of the heterostructure on top of a bulk-GaAs buffer region *(see the figure)*. A self-aligned 1-μm metal-silicide gate structure eases some of the stringent lithography-alignment requirements. Furthermore, the gate could be further scaled to about 0.3 μm to achieve even higher-speed operation and smaller chips. Two levels of metallization interconnect transistors on the chip.

Additional benefits from the C-HFET structure and process include its high tolerance for radiation, and its ability to operate at either cryogenic (liquid nitrogen) or high temperatures (150° to 200°C). However, according to Tetzlaff, it will take several more years of research before the technology can be commercialized.

DAVE BURSKY

ELECTROCHEMICAL PROCESS PROMISES TO MAKE SILICON A LIGHT EMITTER

Results of experiments with silicon carried out at the Siemens research laboratories in Munich, Germany, raise hopes that this semiconductor material can be used in optoelectronics not only as a light receiver but also as a light emitter.

Until now, the emission of visible light from solid-state lasers and light-emitting diodes has been possible only with compound semiconductors, such as gallium arsenide or indium phosphide. But GaAs and InP material combinations aren't only expensive, they're also difficult to handle.

In the case of silicon, however, the industry would have at its disposal an inexpensive light-emitting material for which process technologies are well established and relatively simple.

To get light emission from silicon, the Siemens researchers subjected the material to a simple and inexpensive electrochemical etching process. This process changes the material into porous silicon, giving it a structure with tiny pores and bars. If properly carried out, the etching process results in pore and bar structures with 1- to 2-nm diameters.

In the porous silicon, the motion of the charge carriers is restricted to atomically small distances. According to the principles of quantum mechanics, the material's energy states and the area of light absorption and emission will shift considerably following the treatment.

In their experiments at the Munich labs in which the porous silicon was excited with blue laser light, the Siemens researchers produced visible red and yellow light with the material. By altering the dimensions of the bars and pores during the etching process, the wavelength of the emitted light can be changed, which is proof that the emission is due to quantum-mechanical effects.

For designers of optoelectronic devices, a light emitter made of silicon would offer many advantages. With optoelectronic receiving and amplifying elements already based on silicon, a light emitter that also uses silicon would lead to very dense and compact devices.

That is, the circuits will have a much higher level of integration than would be possible with different materials employed for the receiver and amplifier on the one hand, and for the emitter on the other.

JOHN GOSCH

THALLIUM-ARSENIC-SELENIDE BOULE CONVERTS CO_2 LASER OUTPUT TO INFRARED RADIATION

Using a technique called second-harmonic generation (SHG), a team of researchers at the Westinghouse Science and Technology Center, Pittsburgh, Pa., have converted the output of a carbon-dioxide laser to mid-infrared wavelengths. In addition, conversion efficiency runs 57%, the highest yet achieved by SHG, and it's the most efficient mid-IR energy source. In fact, until this development, intense infrared sources capable of operating at high repetition rates and moderate levels of average power have not existed. Mid-IR-wavelength sources have military and non-military applications because they can be tuned to lie within the three windows of wavelength, offering very low transmission losses through the atmosphere.

The wavelengths of the three windows or ranges encompass 1.7-2.5 μm (range I), 3.4-4.2 μm (range II), and 4.5-5 μm (range III). The laser also represents a powerful energy source that can tune into the absorption bands of a broad range of pollutant gas molecules. In that application, the need for a technique to provide rapid, remote atmospheric monitoring from an airborne, or rooftop, platform is met. Military applications include tactical defense against IR-sensing missiles.

Second-harmonic generation is achieved by passing the output of the CO_2 laser through non-linear (birefringent) crystals (boules) of thallium arsenic selenide or TAS (Tl_3AsSe_3), home-grown at Westinghouse. In actuality, SHG produces the second, third, and fourth harmonics of the CO_2 laser, all of which are mixed to create the final beam at a conversion efficiency of 57% (the fifth harmonic has also been produced by SHG).

The complete laser, called the Middle InfraRed Tunable (MIRT) Laser starts with an efficient, low-pulse-energy (about 0.1 mJ) CO_2 laser oscillator tunable over the wavelengths of interest. It puts out short (20-ns) pulses at 50 kHz. The pulses are amplified by high-power laser amplifiers to about 2 mJ. A collimating telescope focuses the linearly polarized CO_2 laser beam on the TAS crystal.

In one MIRT configuration, the crystal has been grown and fabricated with its axis inclined 19° to the optical or C axis of the boule. A stepper motor rotates the crystal into a position to send a 9.25-μm laser beam down the C axis. When the beam leaves the crystal, the laser frequency has doubled and the wavelength cut in half to 4.63 μm. The shorter wavelength beam is now passed through a TAS crystal that was grown and fabricated with its axis inclined 24° to the C axis. This crystal is rotated by its stepping motor so that the input beam enters 28.3° off the C axis. At this angle, the crystal again doubles the frequency and the wavelength is halved to 2.31 μm. The output beam now contains three wavelengths, 2.31 μm lying in transmission window I, 4.63 μm lying in window III, and some residue of the original 9.25-μm beam.

To get a laser wavelength for window II, the laser is tuned to a longer wavelength, for example 10.3 μm. The first crystal is rotated to propagate the laser beam along an axis inclined 18.5° to the C axis. The frequency doubles and the wavelength halves to 5.15 μm. The second crystal is rotated so that the beams enter it inclined 20° to the C axis. The two frequencies mix, producing the third harmonic and a wavelength of 3.43 μm, which lies in window II.

This ongoing work is partially supported by the Wright Laboratory Aeronautical Systems Division at the Wright-Patterson Air Force Base, Dayton, Ohio. For additional information, call B. H. Taylor at (412) 256-1650.

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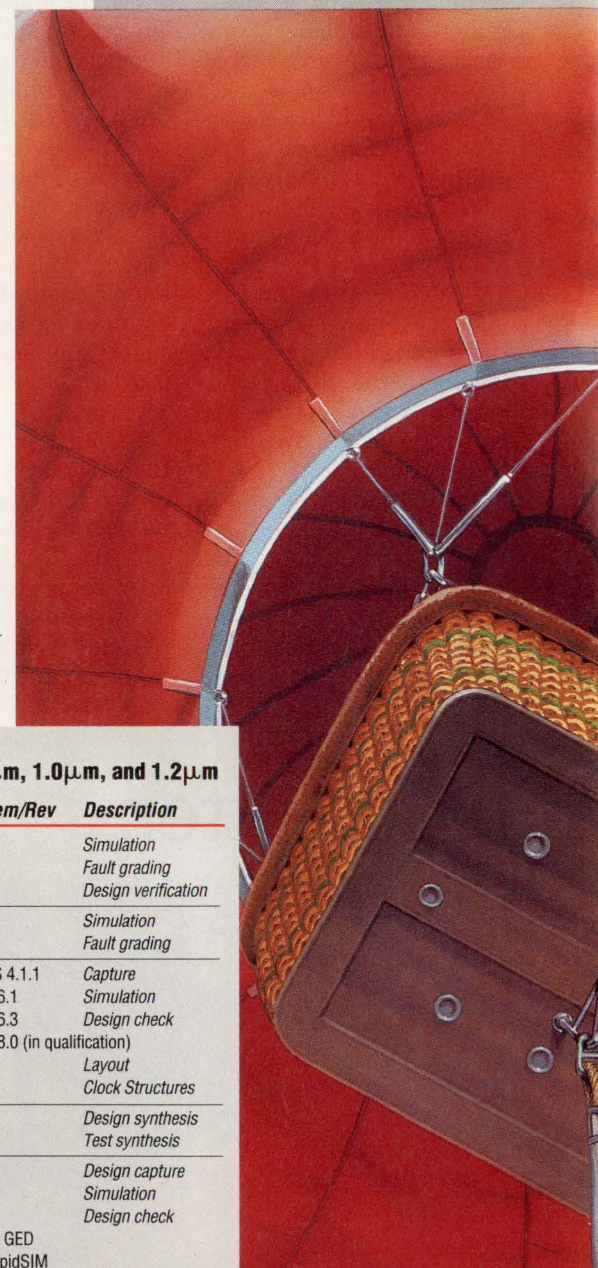

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Cadence	Sun/SPARC Solbourne	Sun OS 4.1.1 Verilog 1.5C	*Simulation* *Fault grading* *Design verification*
IKOS		4.0 up	*Simulation* *Fault grading*
Mentor Graphics	HP/Apollo DNx Series HP9000 Sun/SPARC Solbourne	DNIX 5.03, Sun OS 4.1.1 Digital application 6.1 Digital application 6.3 Digital application 8.0 (in qualification) Parade	*Capture* *Simulation* *Design check* *Layout* *Clock Structures*
Synopsys	Sun/SPARC Interface to Mentor, Valid, Viewlogic	Sun OS 4.1.1	*Design synthesis* *Test synthesis*
Valid	Sun/SPARC Sun-3 DECstation 3100 IBM RS6000	Sun OS 4.1.1 GED, ValidSIM, RapidSIM ULTRIX, ValidSIM, GED GED, ValidSIM, RapidSIM	*Design capture* *Simulation* *Design check*
Viewlogic	Sun/SPARC PC386	Sun OS 4.1.1 Workview 4.0 DOS 3.3, Workview 4.0	*Design capture* *Simulation*

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ESSCIRC TAKES A FORWARD LOOK AT IC TECHNOLOGY

JOHN GOSCH

THE ANNUAL EUROPEAN SOLID STATE CIRCUITS CONFERENCE IN MILAN EXAMINES GLOBAL IC ADVANCES.

The European Solid State Circuits Conference, Europe's answer to the annual International Solid State Circuits Conference held in the U.S., may not yet have the visibility and exposure that the ISSCC generates, nor does it draw as many people. But the ESSCIRC organizers think their conference features papers whose quality matches that of the presentations at the ISSCC. There's much proof of that at the 17th ESSCIRC in Milan, Italy, Sept. 11-13.

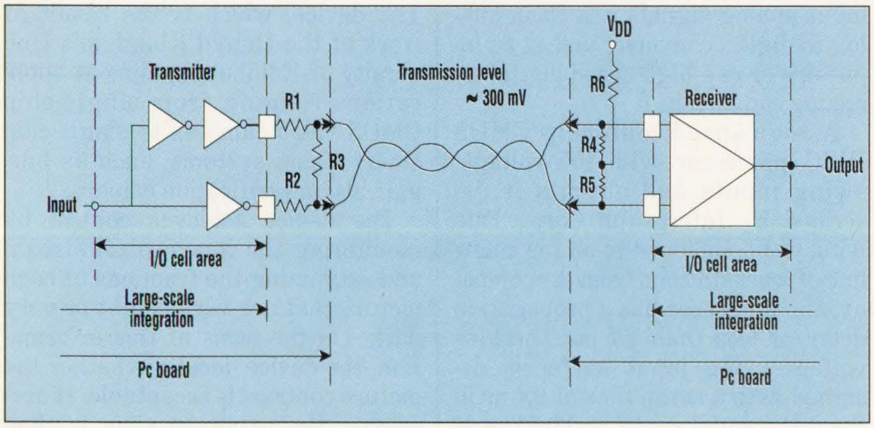
The quality is evident in that the 72 contributed papers presented this year were selected from more than 170 submitted. "We tried to pick papers representing the best in microelectronics and describing avant-garde developments," says Rinaldo Castello, technical committee chairman of ESSCIRC '91.

In addition to quality, there's ESSCIRC's aspect of internationality. What started out in 1975 as a regional event—almost all papers at that time were from European authors—has grown into a conference of global stature. Of the contributed papers given by speakers from 13 countries this year, 20% are from American and Japanese authors.

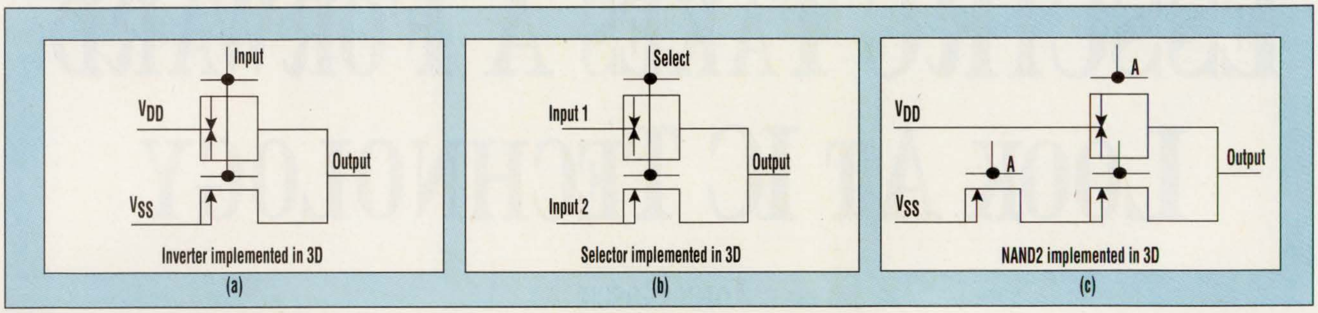
Also, ESSCIRC is steadily becoming *the* venue for first exposure of new semiconductor developments. For example, experts from Hitachi, Tokyo, first discussed circuit concepts for their 64-Mbit DRAM at last year's conference in Grenoble, France.

This year, the 400 attendees are witnessing something new, at least for ESSCIRC conferences. That's the presentation of invited papers from representatives of industries using circuits, as well as from companies producing them. "In these presentations, the components-using industries are informing producers about the direction their particular field will take in the years ahead," says Bruno Murari, conference chairman of ESSCIRC '91. "For their part, device makers are making known to users where they stand at present, giving state-of-the-art reports on technology and design and on what microelectronics has in store for them."

A good example of such dialogue, Murari says, are invited papers from Ettore Panizza of the Italian car maker Fiat and Joachim Melbert of the German chip producer Siemens. Panizza discusses automotive systems and functions that car makers envision for the next few years, while Melbert describes the resources circuit designers will have at their disposal to handle future functions. "This type of dialogue gives both sides an idea of what to expect in the years ahead," Murari adds.



1. IN THE ADVANCED LOW-LEVEL transmission system from Hitachi, the transmitter sends TTL differential signals. Resistor values are chosen to match the twisted-pair cable's characteristic impedance.



2. BASIC ELEMENTS from a vertically integrated process are inverter (a), selector (b), and NAND2 circuits (c). These can be used to build a cell library with latches, flip-flops, NOR gates, and the like. Special macro blocks, such as multipliers and static RAMs, complete the circuit library. The process was developed by the German Institute for Microelectronics.

Similar invited papers come from Johan Danneels of France's Alcatel communications group, who represents telecommunications chip users, and Pietro Erratico of SGS-Thomson Microelectronics, the Italian/French device maker, who speaks for telecommunications chip producers. Another pair of invited papers comes from Erich Geiger of France's Thomson Consumer Electronics group, representing TV chip users, and R.P. Kramer of Philips Components, for the TV chip makers.

Traditionally, ESSCIRC conferences have a large proportion of papers dealing with analog circuits, more than do the ISSCC events, Castello says. That's also the case in 1991. Of the 16 sessions this year, five are strictly on analog circuits while half of all subjects discussed deal with analog and mixed technologies and design. New sessions this year are "Smart Sensors," a reflection of what's hot in the industry, and "Testing," which is becoming increasingly important.

Efficient Communications

In recent years, communications-equipment designers have shown much interest in asynchronous transfer-mode (ATM) switching systems. Although ATM device development has progressed considerably, some problems remain to be solved. One is how to get high-bit-rate data transmission efficiently and economically. Though optical fibers are best to bridge long distances, twisted-pair cables are most economical for transmissions between pc boards within a system and in inter-office data communications.

A directly driven transmitter-receiver circuit system described by Hitachi, is designed for such ATM applications. The system handles 320 Mbits/s, an incredibly high speed for a twisted-pair cable up to 10-m long. The result of research at Hitachi, Tokyo, the system uses low-swing 0.3-V differential signal levels to realize the high data rate. The transmitter and receiver circuits of the advanced low-level transmission system (ALTS) are contained in a 0.8-μm CMOS gate-array I/O device *(Fig. 1)*.

A latched comparator from the Fraunhofer Institute for Integrated Circuits in Erlangen, Germany, shows high speed and performance. Thanks to a design that combines 0.5-μm gallium-arsenide and high-electron-mobility-transistor (HEMT) technologies, the comparator operates at up to 4 Gsamples/s. Its sensitivity is 10 mV. The device can be used for the parallel comparison of input analog signals in a flash analog-to-digital converter and as an input driver in a high-speed digital-to-analog converter.

A high-speed multichip CMOS RISC processor with low-voltage-swing inputs and outputs is described by Intergraph Corp., Palo Alto, Calif. Believed to be for a new line of workstations from the company, the processor has a propagation delay of less than 1.7 ns. The low-voltage-swing input buffer is designed with a setup time of 0.4 ns in the differential mode, and 0.75 ns in the single-ended mode. A custom ceramic 299-pin PGA package with controlled-impedance lines and shield planes minimizes crosstalk.

A floating-point cell library, offering high flexibility and performance for logic synthesis of image-signal processors, has been developed at Toshiba, Kawasaki, Japan. The library's 32-bit ALU and 32-by-32-bit multiplier support not only IEEE-754-format floating-point operations, but also fixed-point and logical operations that are often used in image-signal processing. A new vector processor was synthesized with a logic-synthesis tool using the library. Designed in 1.2-μm CMOS, the processor has a peak performance of 100 MFLOPS at 33 MHz.

A CMOS image sensor array chip integrating an electronic aperture and a simple exposure controller achieves wide-range exposure control of 40,000:1. That equals 15 stops of a mechanical iris system. Such performance compares with an equivalent of only 8 stops for on-chip electronic apertures reported so far. The device, which is the result of work at the United Kingdom's University of Edinburgh, aims at applications ranging from single-chip CMOS video cameras to single-chip smart vision systems, such as burglar-alarm verification cameras.

The device achieves control by monitoring the image pixel stream and estimating the fractions of each picture that are very bright or very dark. On the basis of this information, the device decides whether the picture contrast is acceptable. If necessary, the exposure time is then changed in the appropriate direction for the optimum setting.

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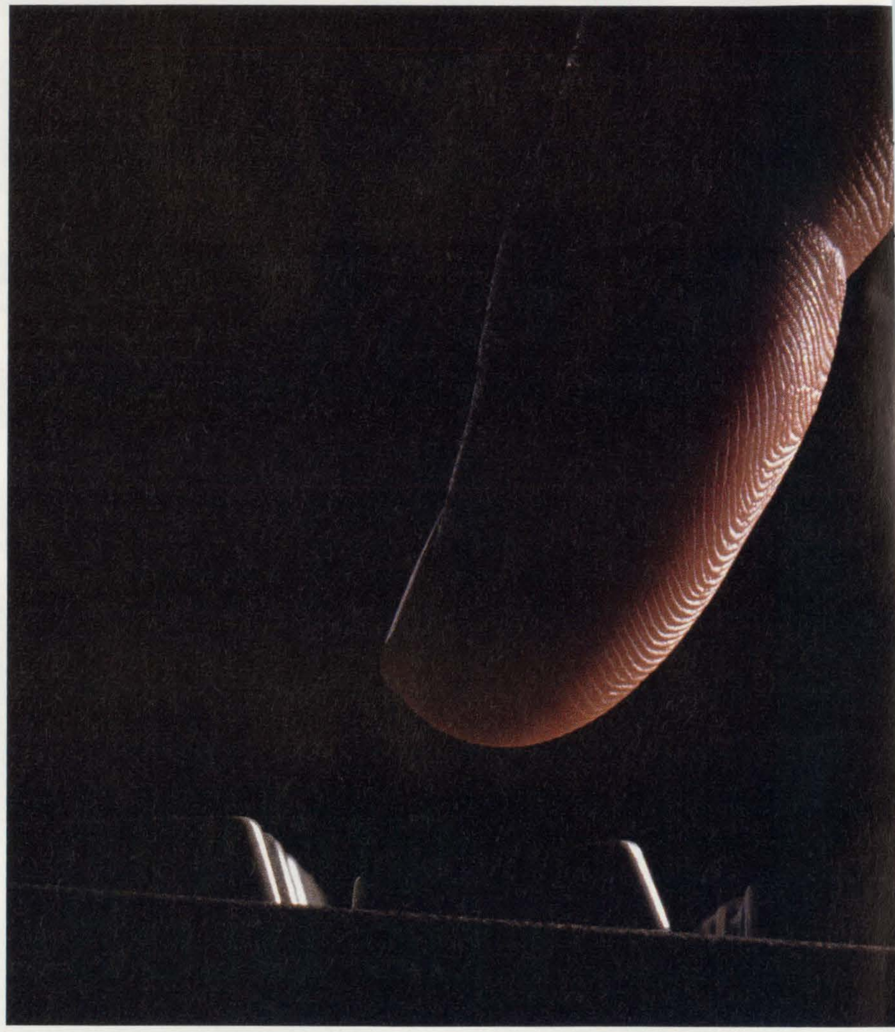

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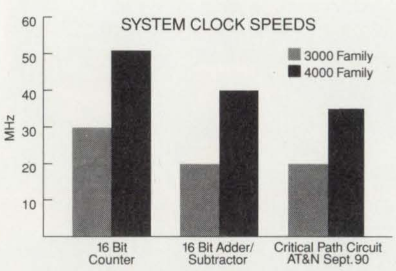

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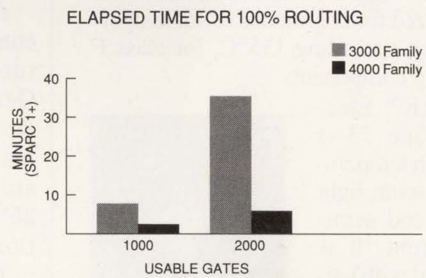

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cell from Italy's University of Pavia has excellent performance, even though it uses conventional 2-μm technology. Key to its performance is the biCMOS design that the second-order lowpass filter cell uses. The device can be tuned over an 8-MHz to 32-MHz range and has a quality factor of 2. Total harmonic distortion stays lower than 42 dB for an output signal up to 2.4 V pk-pk at 5 MHz. The cell's area is 500 $mils^2$ and power consumption at a cutoff frequency of 25 MHz is 30 mW. Intended for disk drives, the device will be a commercial product from SGS-Thomson.

CMOS Advances

An unconventional approach to IC construction comes from the Institute for Microelectronics, Stuttgart, Germany. The complex 3D CMOS circuit is based on a triple-decker cell made by using a process with three stacked transistor channels. Area is 25% to 50% less than that of a conventional 2D CMOS device.

The Stuttgart group's process has led to efficient basic circuits, such as inverter, selector, and NAND2 elements *(Fig. 2)*. These elements can be used to build a cell library with, for example, latches, flip-flops, and NOR circuits. Special macro blocks including multipliers and static RAMs complete the circuit library.

Three-dimensional, or stacked, CMOS technologies have been pursued for more than 10 years. However, none have led to any significant products because of problems with silicon film quality, planarity, vias between different layers, and the like. The Stuttgart group's technology, which starts from a standard bulk NMOS process, tackles these problems and brings true 3D CMOS circuits closer to volume production.

A codec from Alcatel Bell, Antwerp, Belgium, can be used for applications in hand-portable terminals, such as telephones used in cellular digital radio mobile communications. The device, made in 1.2-μm CMOS and occupying a 14-mm^2 die area, has a dedicated processor serving digital filter calculations. An interpolator and sigma-delta modulator transform incoming signals to an oversampled 1 Mbit/s pulse-density-modulation signal that's converted to obtain the earpiece signal.

A fourth-order sigma-delta converter comes from the United Kingdom's University of Southhampton. The circuit gets around the problems associated with switched-capacitor samplers by using a self-tuning continuous-time noise shaper. The device, made in 1.6-μm CMOS and operating from a single 5-V supply, is unconditionally stable and recovers immediately from overload without resetting integrators.

As VLSI chip complexity increases to several hundred thousand transistors, testing becomes more important. In an invited paper, Eckhard Wolfgang of Siemens, Munich, Germany, reviews the state-of-the-art for three contactless testing techniques: electron-beam testing, laser-beam testing, and emission microscopy. Reasons are given why contactless testing is important for chip verification and failure analysis. Also, a scenario of contactless testing describes the influence of chip, package, and CAD environments.

Built-in self-test (BIST) methods are increasingly applied on-chip to raise fault coverage, minimize the expense for test equipment, and guarantee high-quality parts. Philips Kommunikations Industrie AG, Nuremberg, Germany, has developed a BIST-based test strategy for a 16-bit digital-signal processor employed in digital mobile telephones. The strategy uses the architectural and functional properties of the processor.□

Electronic Design would like to thank conference chairman Bruno Murari and technical committee chairman Rinaldo Castello for their thoughts on ESSCIRC conferences and their help in obtaining details of the papers at this year's conference in Milan.

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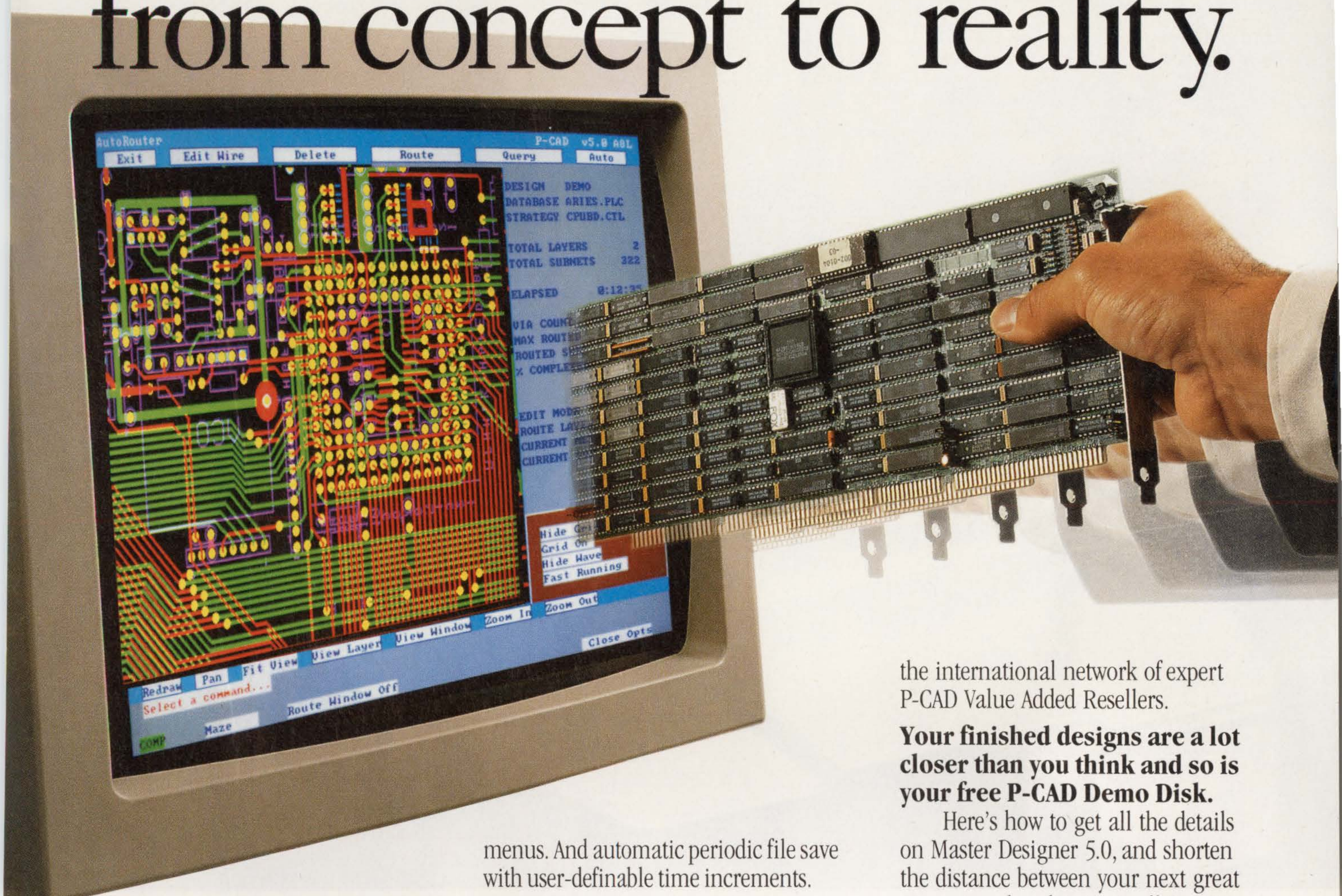

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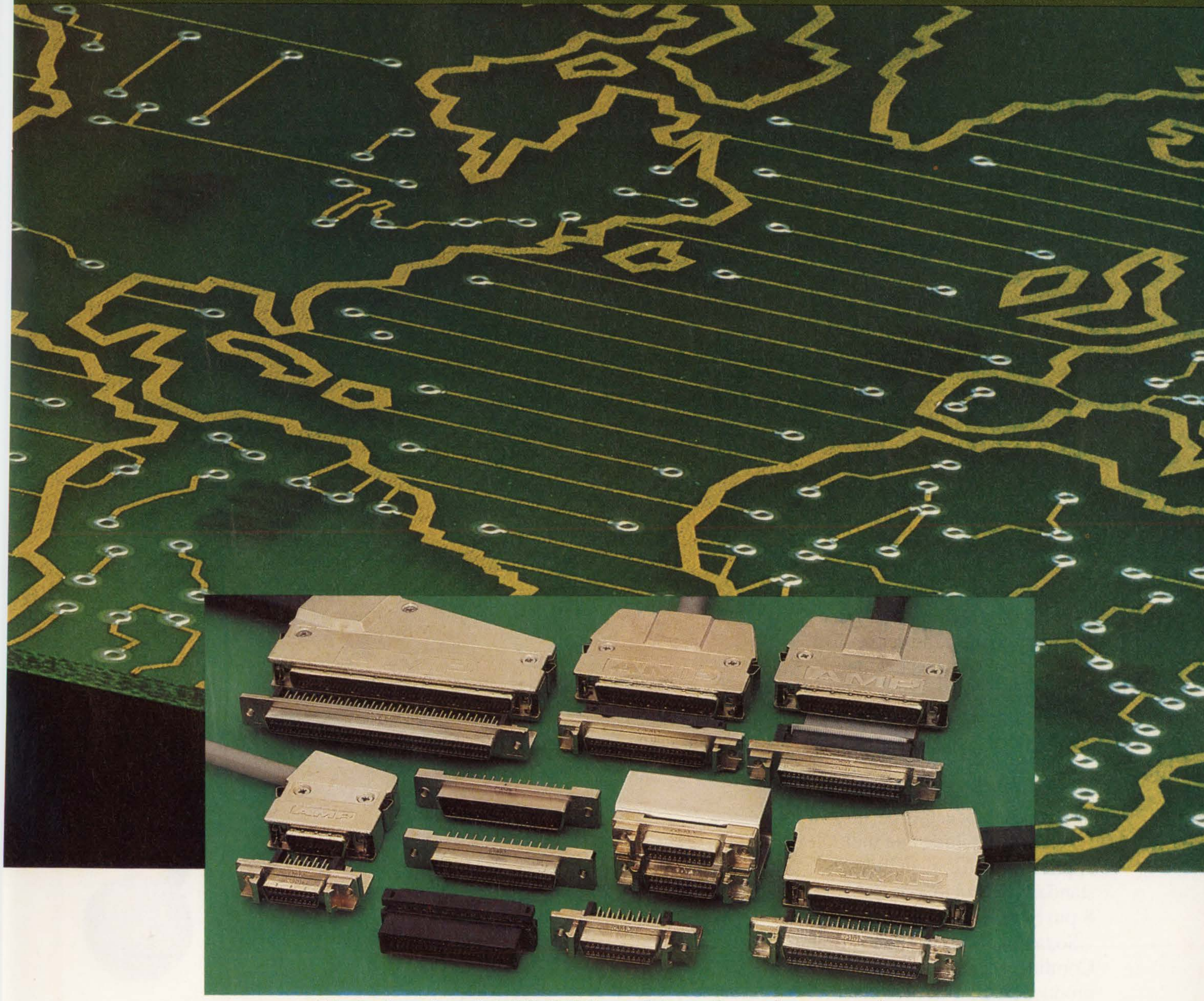

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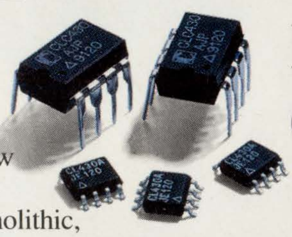

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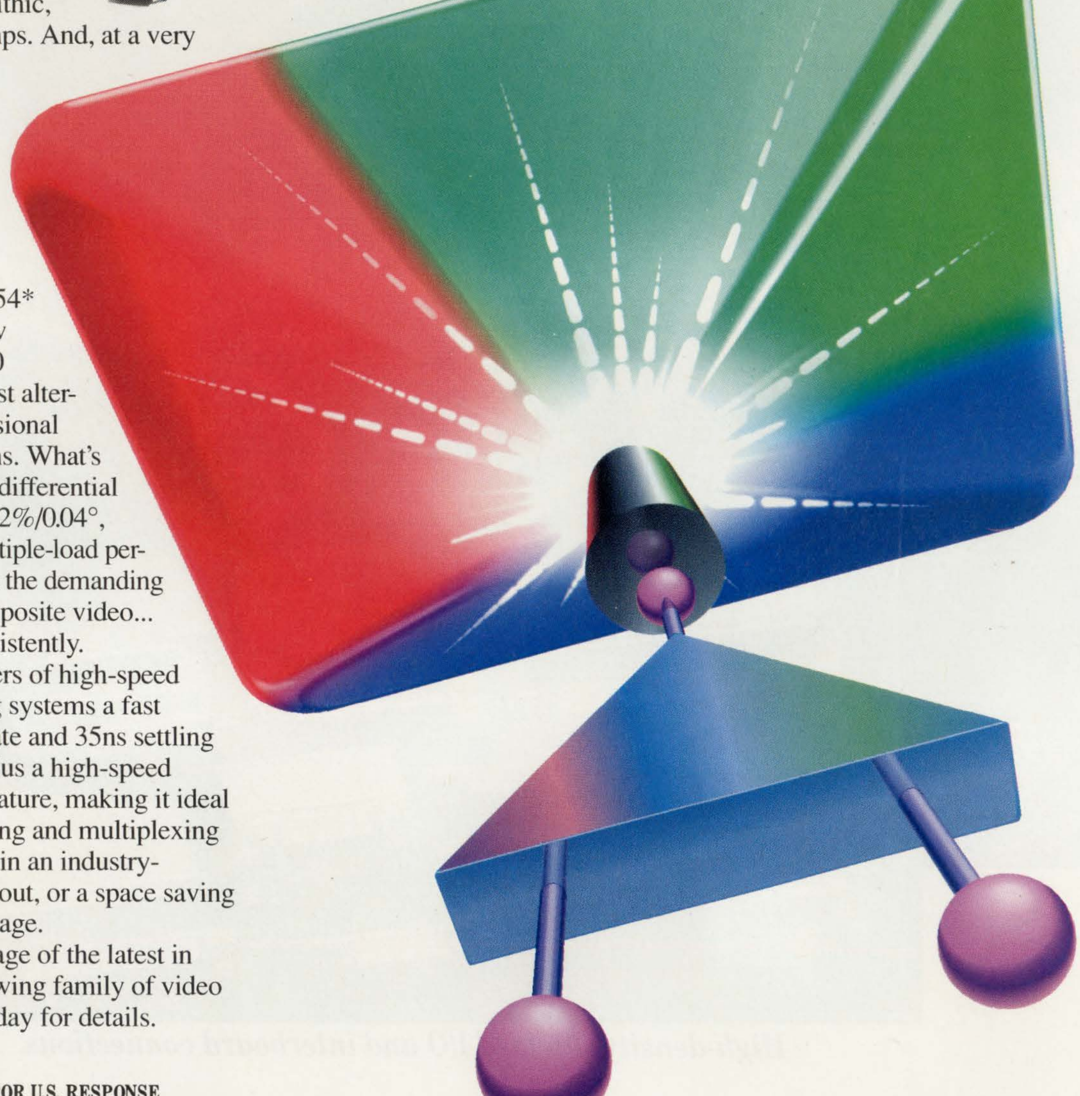

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Codec Teams Delta-Sigma Converters With DSP To Shuttle Stereo Sound Between Multimedia Peripherals.

Multimedia Codec Chip Adds Voice And Music

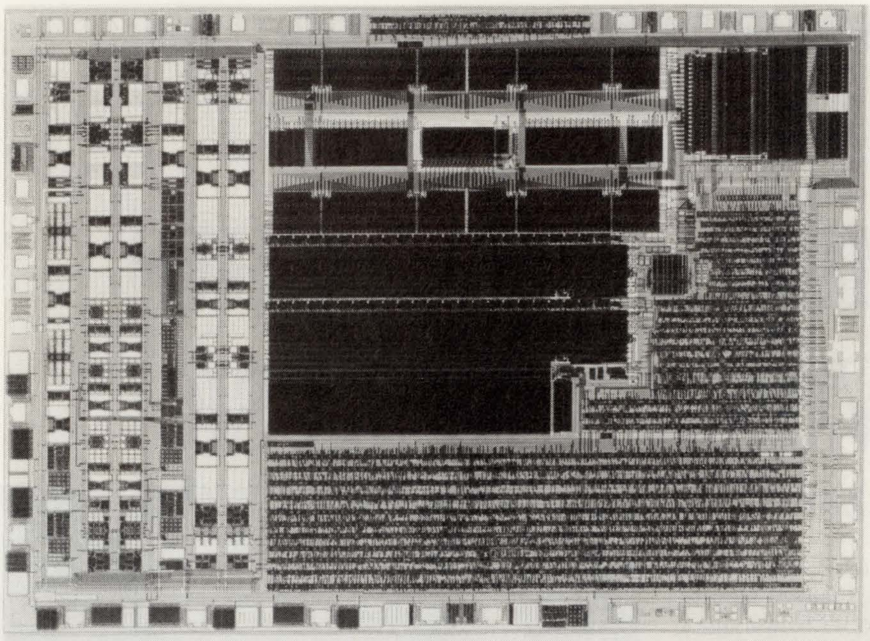
Milt Leonard

Until now, multimedia technology has focused on integrating text with high-quality still, as well as moving, images on desktop-computer screens. Little attention has been paid, however, to the quality of the sound that accompanies those images. This, despite the fact that people are more likely to retain information they have heard as well as seen, and the clear strides made in digital sound in the consumer electronics arena. Linking such audio components as telephones, digital audio tapes, and compact disks with multimedia computers has required an expensive collection of discrete analog and digital ICs. However, two single-chip stereo audio codecs, based on delta-sigma data conversion and digital-signal processing, promise to remedy this situation.

The CS4215 and CS4216 codecs, developed by Crystal Semiconductor, are the first devices to integrate both delta-sigma analog-to-digital and digital-to-analog converters on one chip *(Fig. 1)*. Beyond the data-conversion capabilities, the CS4215 is the first stereo audio codec to integrate microphone and line-level inputs, input and output gain setting, antialiasing and output-smoothing filters, stereo headphone drive, and monitor-speaker drive. Equally impressive, the device also includes data-compression/decompression circuitry consistent with telephony A-law and μ-law standards.

Delta-sigma data converters offer the lowest system cost, highest dynamic range, and more integrated features than any other data-conversion technology available for digital audio systems. They also offer several

benefits for audio applications. For example, they allow the use of digital antialias filtering to minimize the need for analog antialias filtering, which is vulnerable to audible phase distortion. Digital filtering also has perfectly linear phase performance and no drift. Also, the 1-bit delta-sigma architecture is inherently monotonic. Another benefit is that no sam-



1. MIXED-SIGNAL TECHNOLOGY enables the CS4215 stereo codec to use digital-signal processing techniques to enhance the performance of analog circuitry. The chip contains 140,000 transistors, 2000 of which are analog devices. Interpolation filters for data conversion occupy about one-third of the die (dark area). Analog circuits for the data converters are across the top of the chip. Compression, decompression, interface functions, etc. are along the left edge.

ple-and-hold function is required.

The CS4215's features are optimized to add voice capability to a workstation or personal computer. A lower-cost sister part, the CS4216, uses the same data-conversion core circuitry, but has fewer value-added features.

This part is useful for systems that simply require basic data-conversion functions, such as computers that support the Microsoft Multimedia Windows 3.0 standard.

The CS4215 stereo audio codec has two channels of 16-bit analog-to-digital conversion along with two channels of digital-to-analog conversion *(Fig. 2)*. The codec's programmable conversion rates cover the range from 8 to 48 kHz. At the analog input section, an on-chip multiplexer selects between line-level inputs and microphone-level inputs.

Each line-level input requires an external antialiasing filter composed of a 150-Ω resistor and a 0.01-μF capacitor to ground. These pins are driven with 1.0-V rms signals centered around +2.5 V.

Operation from a 5-V-only power source makes the 4215 eligible for use in workstations and personal computers. Packaged in a 44-pin PLCC with J leads, the codec's are made with a 1-μm, single-poly, double-metal CMOS process based on gate-array technology. Power dissipation is 500 mW in the active and 10 mW in the power-down modes.

Ac-coupled microphone-level inputs connect to internal amplifiers with 20-dB gain. Full-scale input level, with no gain, is 0.1 V rms. For dc-coupled microphone or line inputs, a common-mode output pin is provided for using an optional dual-op-amp, level-shifting buffer. Microphone and line inputs are routed to a programmable-gain circuit, which provides up to 22.5 dB of gain in 1.5-dB steps. Following the conversion to digital form, these signals are processed by a selectable 16-bit linear, 8-bit μ-law, or 8-bit A-law encoder, and then exit the chip through the serial I/O bus.

Following output attenuation, which provides 0 to 94.5 dB of attenuation in 1.5-dB steps, the mixed signals exit the codec through pins for connecting to stereo headphones and telephone lines. Maximum line output for both headphones and telephone is 1 V rms, centered about +2 V. The recommended minimum load impedance is 8 kΩ for line outputs, and 20 Ω for headphones. The headphone outputs are provided with an additional fixed gain of 6 dB to allow reasonable listening levels with weak digital-signal sources.

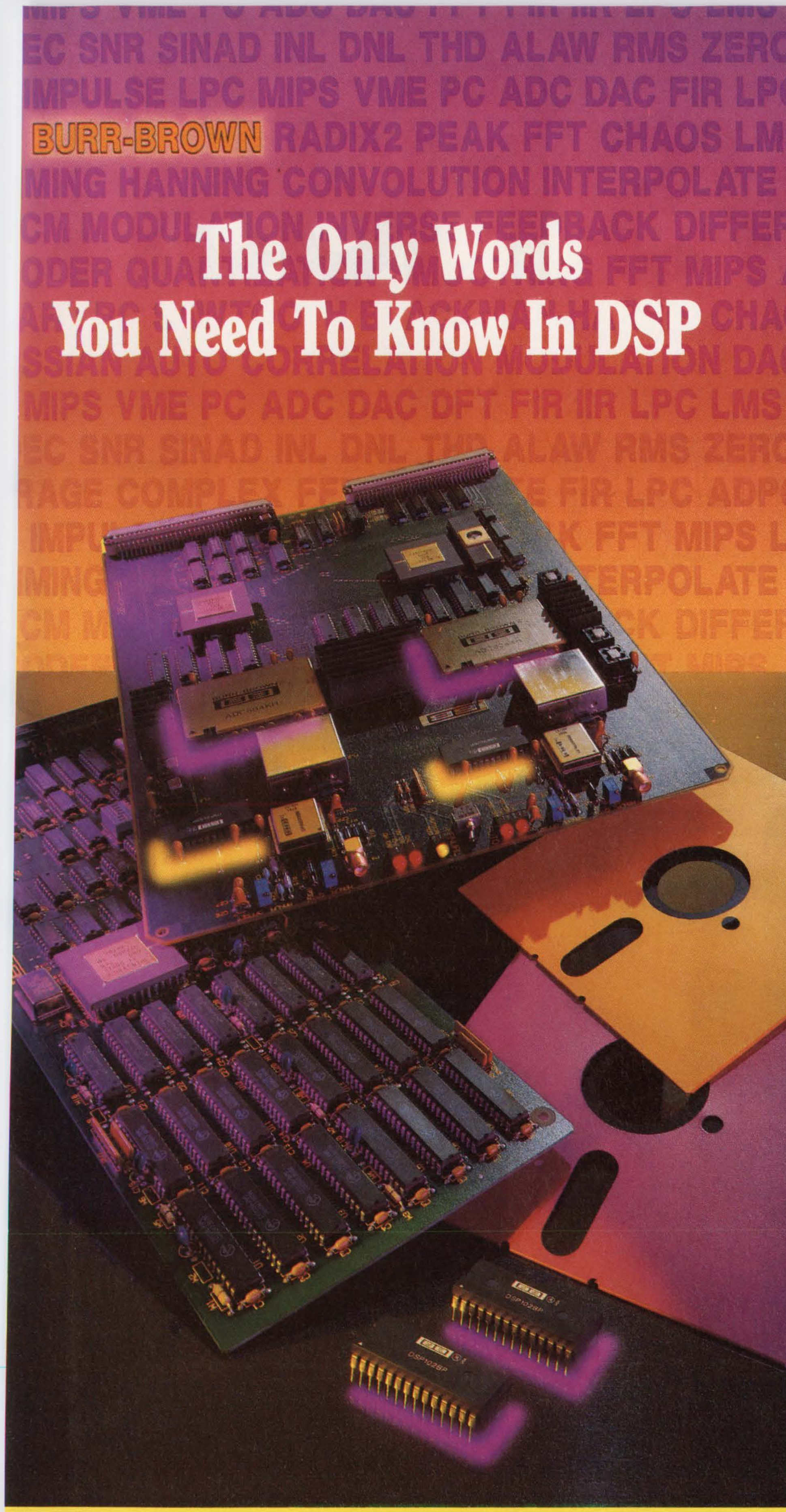
The output attenuator is also connected through an amplifier to differentially drive a small monaural loudspeaker, whose minimum impedance should be 32 Ω. The maximum signal level at the speaker pins is typically 2 V rms. All audio outputs can be independently varied. The 4215's serial interface transfers digital data and control signals to and from the codec. Signal-to-noise ratio is greater than 80 dB for CD-quality sound.

Operating Modes

The codec's operating modes are selected by a host microcontroller through the Data/$\overline{\text{Control}}$ Select line to the 4215's control interface and registers. The control mode loads the internal registers that control data-mode operations. Register content determines such operating functions as handshaking, data-compression/expansion format, monaural or stereo mode, and data-conversion frequency. The registers also control data-transmission operations, including clock-source selection, bit rate, bits per frame, and loopback testing.

Digital loopback causes data on the serial-data input to be sent out on the serial-data output pin for monitoring. Analog loopback internally connects attenuated right and left analog signals to the input gain stage. This allows most of the codec to be functionally tested from the CPU by sending a known digital signal to the DACs and monitoring the ADC data.

In the data mode, digital data transmission between the 4215 and external devices occurs during data-conversion operations. Data frame-



Easy, Plug-In Solutions

The world of DSP is far from simple. You need a secret code book to wade through its bevy of acronyms, a doctorate in mathematics to create its complex algorithms, and years of signal processing expertise to develop the necessary hardware.

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- Need a direct interface ADC or DAC for one of today's DSP processor chips?
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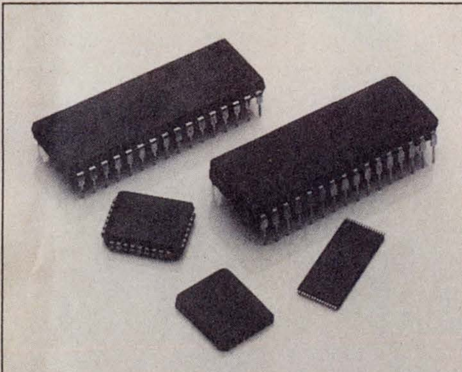
AMD Ships 2 PLCC Flash



How Fast Is A Flash? A Direct Comparison

Density	AMD	Fastest Competitor
256K	90ns	120ns
512K	90ns	120ns
1 Mbit	90ns	120ns
2 Mbit	90ns	150ns

SUNNYVALE — The computer industry takes a giant leap forward in performance with the help of the new Flash memory family from Advanced Micro Devices, Inc.

Flash memory is a high-density, reprogrammable, non-volatile technology that has a bright future in computation, laser printers, network and telecommunications hardware. Many military systems use Flash technology in radar and navigational applications.

Flash memory also has the potential to eliminate mechanical hard disks and the need for cumbersome batteries. These are two of the biggest and heaviest obstacles in laptop and notebook computer applications.

Today, Flash memory is the most cost effective replacement technology for UV EPROMs and EEPROMs in applications that require in-system programming. Flash memories can literally be reprogrammed in a flash — hence the name.

Standard, But With A Little More Flash

AMD's Flash memory family effectively etches in silicon the de-facto standard for this burgeoning technology that is compatible with Intel's initial Flash architecture.

Because AMD Flash memories are pin-for-pin compatible with the now standard architecture, AMD is positioned as an alternate source for design engineers and purchasing agents alike.

"Alternate source may be an inadequate term," said Jerry Sanders, chairman and CEO of Advanced Micro Devices. "Given our speed and feature set, our customers think of us as a superior resource."

Indeed, AMD's Flash memory family offers designers significant performance advantages (see chart), with speeds almost twice as fast as the nearest competitor.

Engineer Spontaneously Combusts At Meeting

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From AMD.


FOOD

Chips And Salsa

A Business Person's Guide To Silicon Valley Restaurants PAGE 7F

zette

MORNING EDITION

ASHES!

Megabit, 90ns, Memories

The AMD Flash family offers designers and purchasers many packaging options. Particularly popular is AMD's advanced 2 Megabit, PLCC part. Other packaging options include PDIP, CDIP and LCC in 256K, 512K, 1 Mbit and 2 Mbit capacities. TSOP packages will be available in the second half of this year. (LCC not currently available in 2 Mbit.)

AMD's 2 Mbit Flash memories come complete with embedded program and erase algorithms on board. These automatic algorithms speed up the design process and considerably shorten time to market. Previously, engineers were required to develop tedious and time-consuming algorithms to implement in-system reprogrammability. AMD's automatic algorithms also allow several Flash memories to be written or erased at once, without tying-up the CPU. The system is now free to perform other tasks while these operations are in progress. AMD plans to include embedded algorithms in a future release of its 1 Mbit part.

The Ultra-Violet Blues

Flash technology is particularly suited to applications requiring reprogramming in place, because these devices can be reprogrammed in seconds, and within the system.

To update the code on a UV EPROM, the part must first be removed from the system. Once removed, erasure can take up to a full 20 minutes. After reprogramming, the part is then plugged back into the system. The process can result in damage to other components, costly service calls, and headaches.

Flash memories, on the other hand, can be bulk erased in about one to two seconds, without system disassembly. Reprogramming can then be accomplished via floppy disk, over phone lines, or even ISDN (continued)

sident To Speak

Stop the presses!

Advanced Micro Devices makes big news again—this time with an enhanced family of Flash memory devices.

That's good news for veteran and new Flash users alike.

Because our Flash devices are pin-for-pin compatible with Intel's existing Flash memory architecture, they establish the *de facto* industry standard.

Our standards, however, are a bit higher. And so are yours.

That's why our Flash Memory family offers densities, speeds and packaging options that improve performance and save board space. For instance, our advanced 2 Mbit PLCC part with a scant 90 nanosecond delay.

You can also choose from Flash devices in 256K, 512K and 1 Mbit densities. As well as packaging options that fit your design best, including CDIP, PDIP, LCC, TSOP, and PLCC.

And you'll find implementation faster and easier than ever, because we've included automatic programming algorithms on all our 2 Mbit devices, and soon on our 1 Mbit parts, too. So you'll spend less time writing code, and take less time getting products to market.

To keep up to date with all the latest and greatest in Flash memory, call AMD today at **1-800-222-9323.** And start making some headlines of your own.

Advanced Micro Devices

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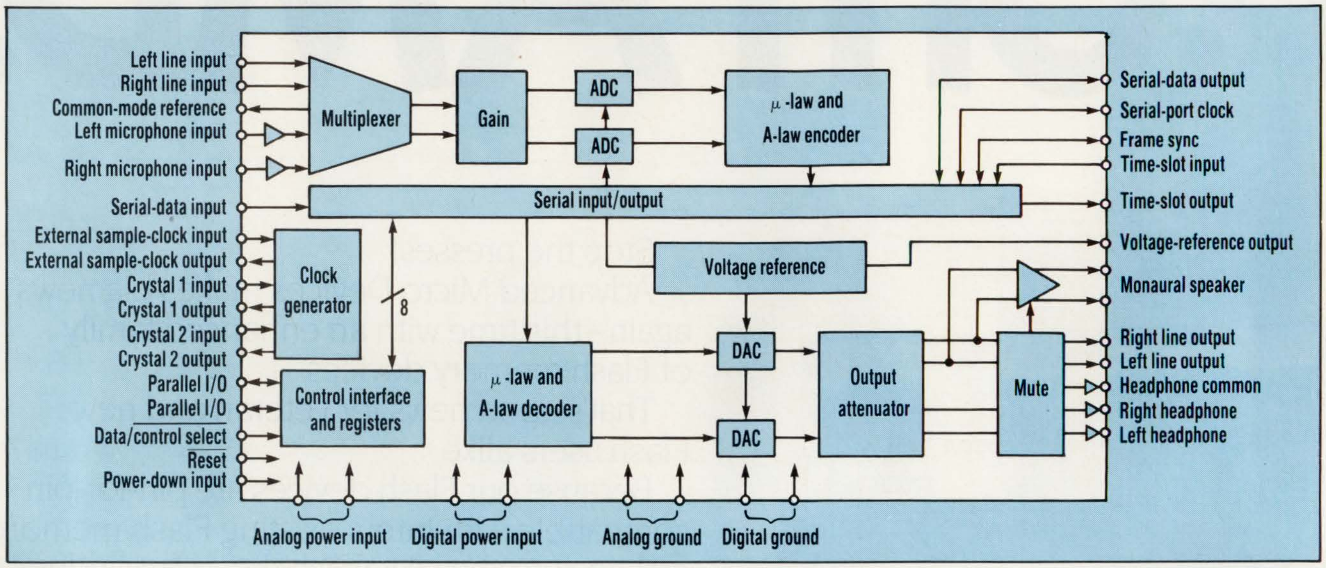
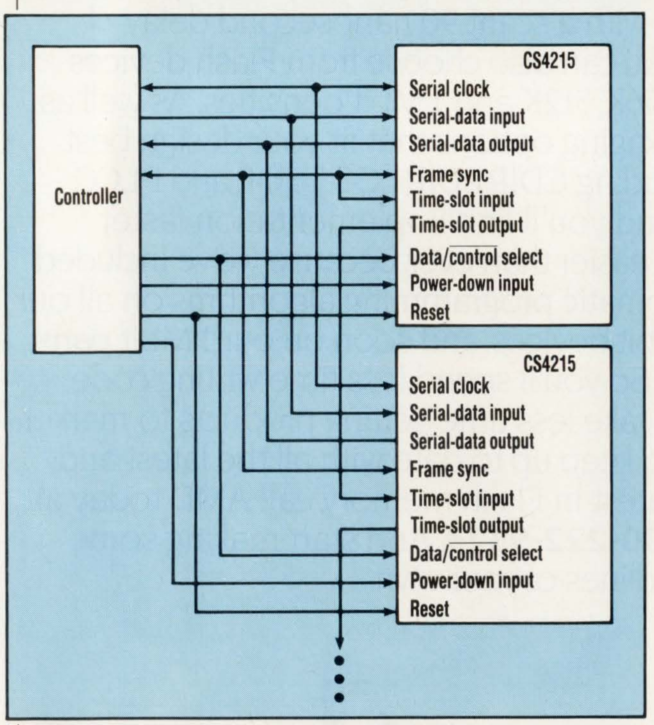
CIRCLE 88 FOR U.S. RESPONSE CIRCLE 89 FOR RESPONSE OUTSIDE THE U.S.



2. THE CS4215 INTEGRATES all of the function blocks necessary to mix analog and digital voice and music signals from different sources, and then deliver a monaural or stereo output to external speakers, headphones, and telephone lines. Left and right volume levels can be controlled independently. The input multiplexer selects between line- and microphone-level inputs.

sync rate is equal to the conversion frequency selected by bits in the data-format register.

As determined by the content of the serial control register, each frame has 64-, 128-, or 256-bit periods, allowing up to four 4215s on one bus. Control of gain, attenuation, input selection, and output muting is embedded in the data stream.



3. MULTIPLE STEREO CODECS can share the same data lines of a system controller. In this case, the serial-data output and input lines are time-division-multiplexed between the codecs, and the time-slot output and input pins are daisy-chained.

Because one crystal can't drive all of the data rates encountered in multimedia sound requirements, the 4215 supplies four pins for connecting external crystals to two on-chip crystal oscillators. For master clock-signal generation, one internal oscillator generates clock frequencies in multiples of 8 kHz, and the other creates the remaining clocks. Typical crystal-oscillator frequencies are 24.576 and 16.9344 MHz.

Another pin accepts an optional external clock input, which must be precisely 256 times the system sampling rate. The system clock is provided on an output pin for use by an external transmitter or another 4215 codec. By using time-division multiplexing, multiple devices can share the same data lines of various digital-signal processors, including the 56001 form Motorola and any devices using the CHI bus from AT&T and Intel. *(Fig. 3)*.

The serial interface format has a variable number of 8-bit time slots, depending on the number of 4215s attached to the bus. Each codec requires 8 time slots, or 64 bits to communicate all data. Eight control registers have time slots for bits associated with status, data format, serial and parallel port control, test, and revision. Time-slot assignments for data registers include left and right audio bits, output control, and input control.□

PRICE AND AVAILABILTY

The CS4215 stereo codec will be available in October for $30 each in quantities of 1000. The CS4216 is priced at $23 each for the same quantities.

Crystal Semiconductor Corp., P.O. Box 17847, Austin, TX 78760; Brad Fluke, (512) 445-7222. **CIRCLE 511**

HOW VALUABLE?	CIRCLE
HIGHLY	544
MODERATELY	545
SLIGHTLY	546

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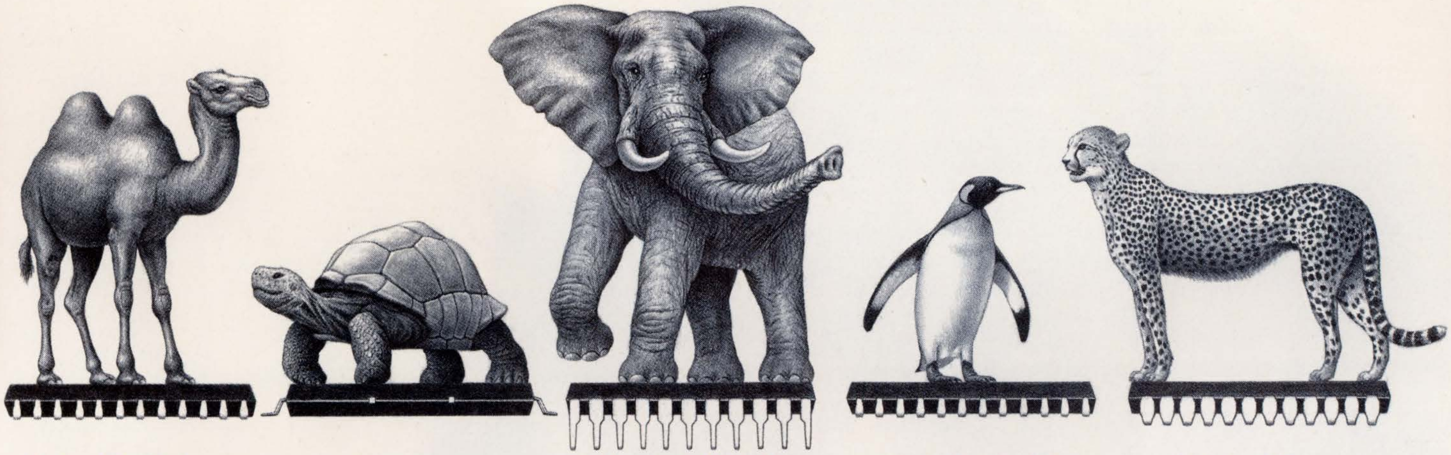

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1-Meg SRAM

	Model	Speed (ns)	Packaging	Data Retention Current	Special Features	Availability
128Kx8	CXK581000P	100/120	DIP 600mil	L/LL	B/X	Now
	CXK581000M	100/120	SOP 525mil	L/LL	B/X	Now
	CXK581100TM	100/120	TSOP (normal)	L/LL	B/X	Now
	CXK581100YM	100/120	TSOP (reverse)	L/LL	B/X	Now
	CXK581001P	70/85	DIP 600mil	L/LL		Now
	CXK581001M	70/85	SOP 525mil	L/LL		Now
	CXK581020SP	35/45/55	SDIP 400mil			Now
	CXK581020J	35/45/55	SOJ 400mil			Now
128Kx9	CXK77910J	17/20	SOJ 400mil		Sync ASM	3/Q '91
256Kx4	CXK541000J	25/30/35	SOJ 400mil			3/Q '91

L = Low LL = Low,Low B = 3 Volt X = Extended Temperature

SONY

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Sony Canada, 411 Gordon Baker Rd., Willowdale, Ontario M2H 256

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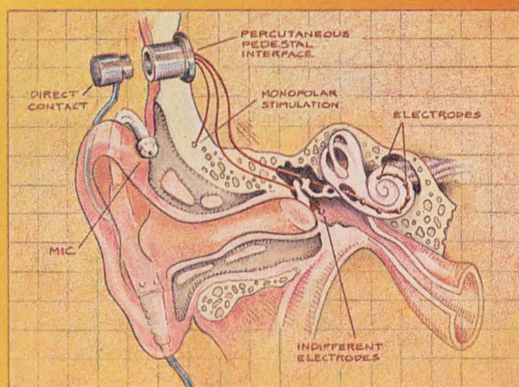
We call it a FET Array.

She'd call it a Miracle.



Hammer. Anvil. Stirrup. Drum. Simple names for the complex natural "hardware" that allows us to hear. If it's injured—or congenitally defective—the deafness that occurs can't always be helped by conventional hearing aid.

A *cochlear implant* bypasses the damage, delivering filtered and processed analog signals directly to electrodes implanted deep in the inner ear. These signals stimulate the audio nerves in a natural way, allowing—in most cases—the deaf to hear.

The variety of applications for our new *RFA120* never ceases to amaze us. But then, a linear array that combines *both* bipolar *and* JFET gain blocks can provide some pretty versatile characteristics:

RFA120 FET Array
Operating Range: ±5V to ±15V
Input Offset Voltage: 5 mV typ.
Input Bias Current: 30 pA typ.
Gain Bandwidth Product: 3.0 MHz typ.
Slew Rate (Gain = +1): 8 Vμs

The RFA120 is a low power device that's ideal for signal conditioning applications. One of our favorites also takes advantage of its small size.

It's a *cochlear implant system* that bypasses injured or congenitally defective "hardware" in the ear canal. The system converts audio signals to analog signals, routing them deep into the inner ear to stimulate the natural audio nerves that are "hardwired" to the brain.

We're committed to analog technology.

And we're committed to helping you develop creative, cost effective solutions.

Our *Win-Win* program is a good example. It lets you get to market quickly with a semicustom array, then shift to full custom as sales increase. It's fast, flexible and makes good business sense because it eliminates the risk of going full custom before you're really ready.

If you'd like more information on our analog arrays, give us a call at **1-800-722-7074**. We'll send you our new brochure.

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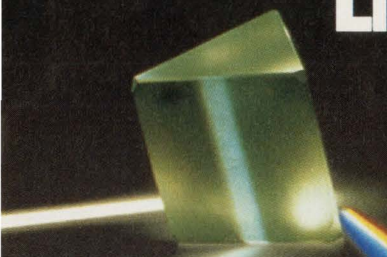

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When you need to convert low-level current signals to precision voltage outputs, try our unique ACF2101dual switched integrator. It's the only complete IC solution on the market, with ***Difet***® op amps, 100pF capacitors, HOLD and RESET switches, and output multiplexers on a single chip.

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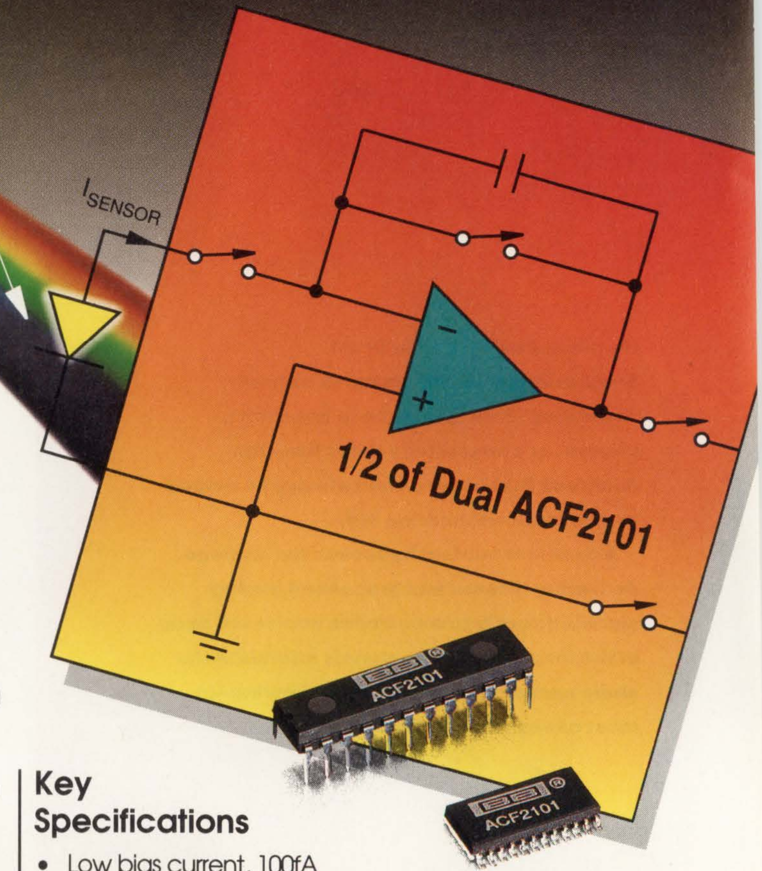

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- Two complete integrators
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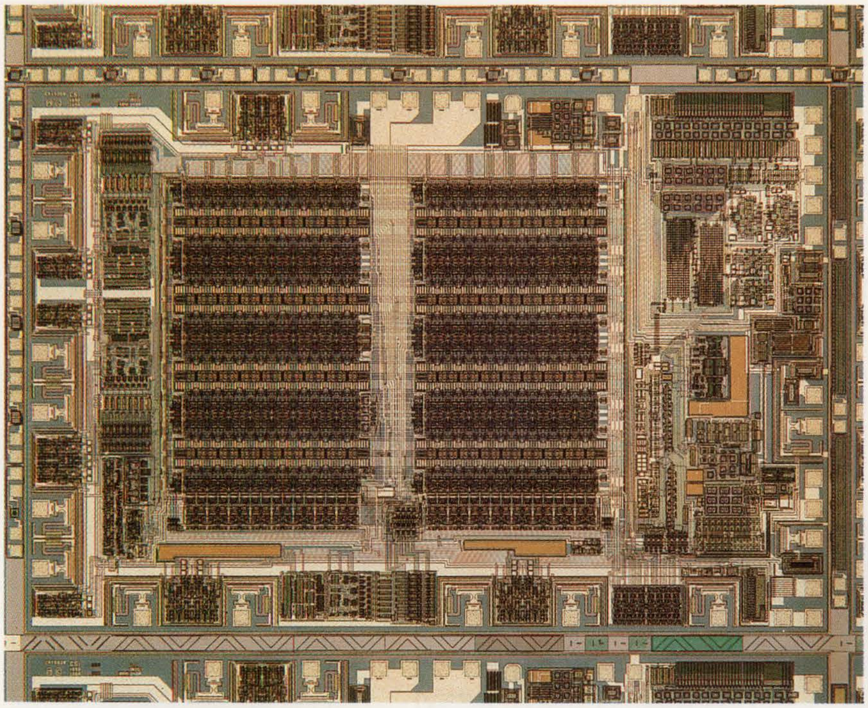


FRANK GOODENOUGH

UBIQUITOUS 12-BIT DACS UNDERGO CHANGE TO MEET USER NEEDS.

12-BIT DACS TAKE ON A NEW LOOK

Once thought by experts to be impossible in monolithic form, the evolving 12-bit digital-to-analog converter has come to defy those predictions. Today, it's as common as the IC op amp. Monotonic performance over temperature, long the dream of DAC users, is now the norm. In fact, it's virtually impossible to buy a 12-bit monolithic DAC that's not monotonic over its operating-temperature range. However, 12-bit DACs are far from representing a mature technology.

Monolithic 12-bit DACs can be roughly divided into two major categories, general purpose *(Tables 1-3)* and high-speed *(Tables 4-5)*. No matter what type, though, system designers (the market) are the driving force behind these ICs, not technologists. As a result, old applications like vector-stroke displays and analog-to-digital converters have virtually disappeared, and new applications spurred on by dropping prices have materialized. Such new applications as waveform reconstruction as well as trimming circuits and systems under host control are becoming more cost-effective.

Among general-purpose 12-bit IC DACs, several trends can be discerned:

- Multiple DACs are being placed on the same chip.
- Users are emphasizing features and packaging as more important selection criteria than performance specifications.
- A move is on to serial, digital I/Os that can be daisy-chained with other DACs.
- Lower power dissipation, lower supply voltages, and/or single-supply operation are emerging trends.
- Voltage-output DACs are beginning to dominate.
- 12-bit general-purpose IC DACs are becoming smaller, and are often available in surface-mounting packages.
- DACs are appearing with a Clear input that sets the output to zero.
- DAC architectures and processes are taking advantage of digital semi-

conductor technology.

As for high-speed 12-bit IC DACs:

• Old applications are rapidly evaporating, with new market-driven applications taking over.

• Specifications are becoming more vital.

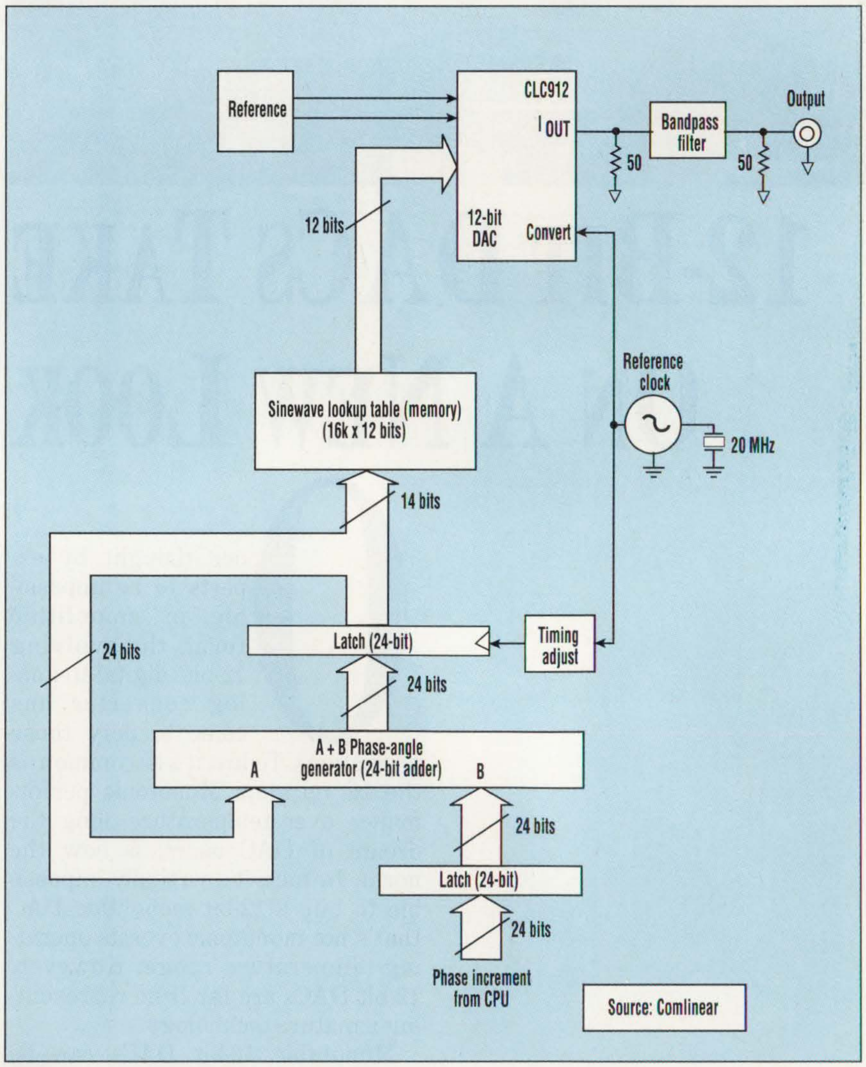
• Current-output DACs are dominating.

More For The Money

A few years ago, designers could purchase dual 12-bit DACs on the same chip, and they were soon followed by quads. Now an octal 12-bit DAC has arrived—Analog Devices' AD7568 *(Table 2, again)*. Albeit a current-output multiplying DAC (MDAC), it illustrates many of the general-purpose trends. Its serial, digital I/O enables eight DACs to be crammed into a 44-pin quad surface-mounted flat pack that's less than 0.5 in. on a side. Board space is cut significantly. Moreover, the AD7568 needs just 1 mW of power from a single 5-V supply. At $23 each in 1000s, its eight DACs cost under $3 each, a significantly lower unit cost than an equivalent quantity of single, serial-I/O, current-output MDACs. In addition, its serial digital output can be tied to the serial input of another AD7568. In this way, many DACs can be fed their input word on a single line in a technique called daisy-chaining. Inside and outside each package, a serial digital word from each DAC feeds the serial input of another DAC.

Though digital designers are at home with AD7856's serial I/O, having a basic knowledge of analog design is helpful with the analog I/O. The latter requires selecting and hooking up one or more dc or ac references and up to eight op amps. On the other hand, dual and quad voltage-output DACs truly simplify the design job. For example, Burr-Brown's recently announced family of three dual DACs (the DAC2813/14/15, each with two op amps), and three quad DACs (DAC4813/14/15, each with four op amps), are all complete with references *(Table 3, again)*. The DAC2813/4813 offer a double-buffered 12-bit-wide I/O, the DAC2814/4814 have a serial I/O, and the DAC2815/4815 include a double-buffered 8-bit-wide I/O that takes data in two bytes (the eight most-significant plus the four least-significant bits). For true versatility, the 12-bit-wide digital I/O of the AD664 quad MDAC can take data in one, two, or three bytes, in any combination of three, 4-bit nibbles. Each DAC's output is applied to an external op amp. Only a single external reference (dc or ac) is required, because the single reference input feeds all four DACs (a feature or a problem, depending on the application).

Because some DACs provide a degree of flexibility in the analog output, you can select unipolar- or bipolar-output voltages and/or one of several full-scale output ranges using application resistors in the package. Usually, the op amp's summing junction is available to add, for example, a high-current buffer within the feedback loop, or even a higher-speed external op amp. However, in many cases, the flexibility should not be used. Adding your own gain-setting resistors may cause a problem. That's because the temperature coefficient (TC) of the resistors in the IC track each other and the DAC,



IN A DIRECT-DIGITAL frequency synthesis system, a phase-angle generator takes inputs from a CPU and generates fractional increments of a sine wave, which are then applied to a lookup table (memory). The system's output, the digital representation of a perfect sine wave, is applied to a digital-to-analog converter for conversion (when strobed by the clock) to an analog waveform with high spectral purity.

TEXAS INSTRUMENTS

A PERSPECTIVE ON DESIGN ISSUES:

Breaking the analog barriers to optimum system design

IN THE ERA OF

MegaChip

TECHNOLOGIES

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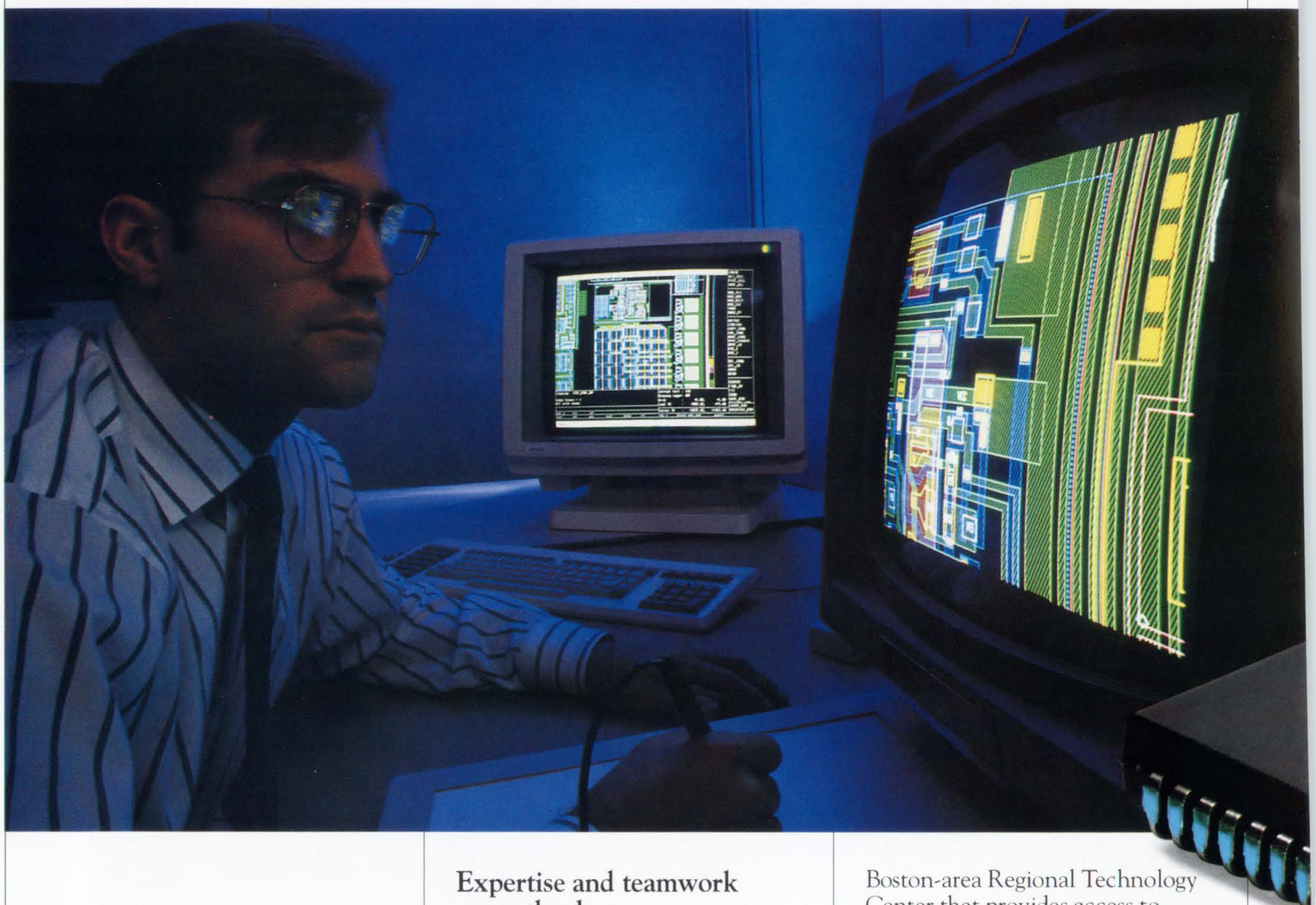
Innovative analog circuits from Texas Instruments add a new edge to Digital Equipment's proven market winners. They can do the same for you.



The goal Digital Equipment Corporation set was clear: Strengthen its position as the leading supplier of Ethernet-based local area network products. Achieving the goal has been spurred by the use of Advanced Linear circuits from Texas Instruments.

These leadership ICs meet growing industry demand for linear circuits that can improve overall system performance and reliability, reduce costs and speed design cycles.

These were precisely the advantages Digital's designers needed.

Expertise and teamwork carry the day

For many years, Digital has used a wide variety of TI linear circuits — from op amps to mixed-signal devices — and values our analog viewpoint toward system design.

As Digital defined the requirements to meet its market goal, the decades-long relationship entered a new era of even more intense cooperation. With Digital handling system-level design and TI applying its linear expertise, the two teams fully utilized our LinASIC™ design methodology to create a series of mixed-signal Ethercell™ functions. They are the basis for the advanced linear devices Digital requires.

The design flow was aided by our Boston-area Regional Technology Center that provides access to LinASIC development tools and by the extensive use of EDIF to exchange information.

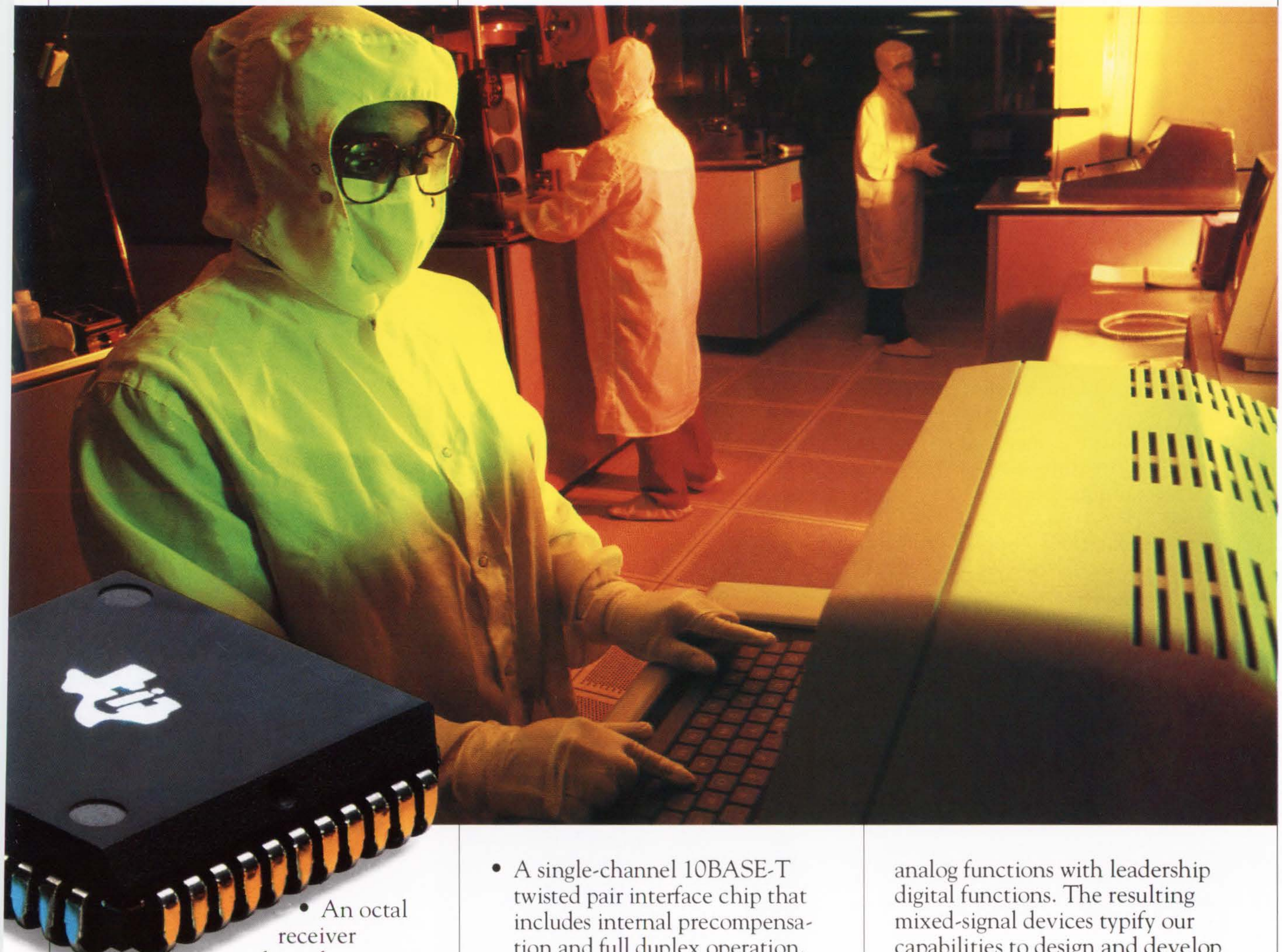
Enhancing Digital's competitive edge

To date, close teamwork has produced components that can enhance Digital's ability to respond quickly to market demands for feature-rich but lower cost Ethernet and communications products:

- A dual driver and dual receiver IC that minimizes the number of components required for the Attachment Unit Interface (AUI) function in an Ethernet network.

"Utilizing TI's LinASIC mixed-signal design methodology allows us to design cost-effective solutions with aggressive time-to-market goals."

— Nick Ilyadis, Product Engineer
Telecommunications and Networks Group
Digital Equipment Corporation



- An octal receiver created to solve system-level cross-talk noise problems in RS-232, -485 and -423 applications. This full-custom device, fabricated in TI's Advanced LinCMOS™ process, is designed to meet EIA and CCITT specs.
- A device that will be a complete AUI multiport concentrator on a chip. Fabricated in our LinBiCMOS™ process, it will replace a 6-inch by 12-inch circuit board that incorporates nine discrete ports, logic devices and analog circuitry. The new device will tie any combination of as many as eight units into Ethernet.
- A single-channel 10BASE-T twisted pair interface chip that includes internal precompensation and full duplex operation. Also fabricated in our LinBiCMOS process, this IC cuts component count and improves data transmission.

The Ethercell devices developed by Digital and TI will be incorporated into our existing LinASIC cell library.

Extensive mixed-signal capabilities

As Digital recognizes, few in the industry can match our experience in analog design and digital design. This expertise enables us to effectively combine high-performance analog functions with leadership digital functions. The resulting mixed-signal devices typify our capabilities to design and develop the Advanced Linear circuits our customers need.

Let us help you meet your challenge

We are ready to provide information and assistance, as well as access to the hardware and software development tools you need, to help extend the boundaries of your system performance.

Our service circles the globe, and our worldwide manufacturing capability can support your production schedules wherever you are.

TI's analog viewpoint: From process technologies come Advanced Linear ICs.

TI's LinASIC mixed-signal methodology —

A cell-based design methodology allowing the combination of high-performance analog and digital functions on the same chip. This mixed-signal capability is used for many of our catalog products and for custom/semicustom solutions. It is supported by large cell libraries, design-automation tools and these TI Advanced Linear wafer process technologies:

LinBiCMOS — Combines Advanced LinCMOS, digital ASIC CMOS and up to 30-V bipolar technologies to allow the integration of digital and analog standard cells and handcrafted analog components on a monolithic chip.

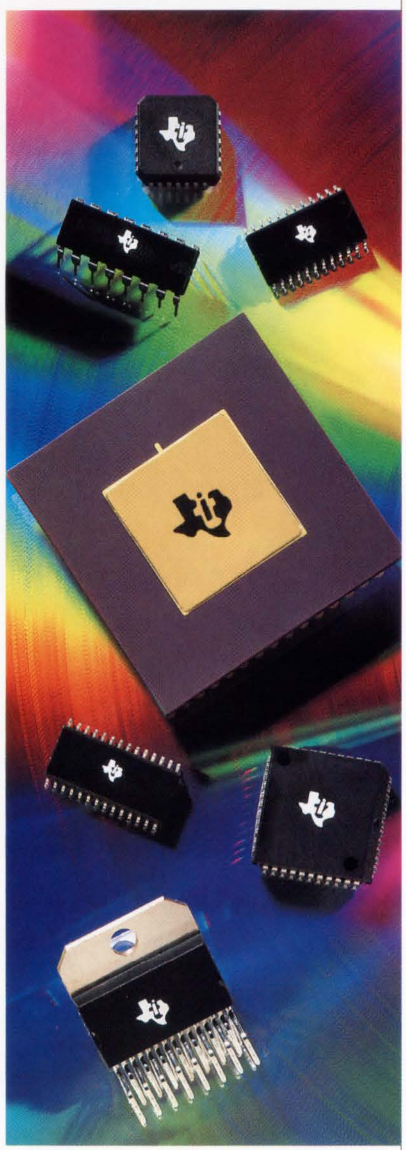
LinEPIC™ — One-micron CMOS double-level metal, double-level polysilicon technology that adds highly integrated, high-speed analog to the high-performance digital EPIC™ process.

Advanced LinCMOS — An N-well, silicon-gate, double-level polysilicon process featuring improved resistor and capacitor structures and having three-micron minimum feature sizes.

Power BIDFET™ — Merges standard linear bipolar, CMOS and DMOS processes and allows integration of digital control circuitry and high-power outputs on one chip. Primarily used for circuits handling more than 100 V at currents up to 10 A.

Multi-EPI Bipolar — A very cost-effective technology that utilizes multiple epitaxial layers instead of multiple diffusion steps to reduce mask steps by more than 30%. Used to produce intelligent power devices that can handle loads as high as 20 A and voltages in excess of 100 V.

Excalibur — A true, single-level poly, single-level metal, junction-isolated, complementary bipolar process developed for high-speed, high-precision analog circuits providing stable op amp performance.



For more information on our Advanced Linear process technologies and the products they are producing, call **1-800-336-5236, ext. 3425.**

TI's LinASIC methodology and Advanced Linear process technologies are enhancing these product families

Data Transmission — This family meets the needs of most industry-standard interfaces (EIA, IEEE, ANSI) and ranges from drivers/receivers/transceivers to fully integrated controller/transceivers.

Data Acquisition — The family ranges from stand-alone A/Ds and D/As to complete data conversion subsystems on a chip; from general-purpose functions to highly integrated digital signal processor and graphics signal processor analog interface circuits. Other specialized family members include telecom and speech synthesis functions.

Intelligent Power — These devices combine high-voltage and/or high-current switches with the analog and digital circuitry required to perform interface, control, protection and diagnostic functions in microcontroller-based systems.

Operational Amplifiers — A family of op amps and comparators ranging from standard bipolar to leadership high-performance CMOS and Excalibur complementary-bipolar devices, meeting needs ranging from low power and/or low noise to high speed and/or high precision.

Custom/semicustom Functions — In modifying existing products to fit your needs or in defining your own unique functions, our LinASIC methodology allows access to existing analog cells used in the development of our catalog products and compatibility with our digital cell libraries.

TEXAS INSTRUMENTS

08-1009

OCTOBER COMING ATTRACTIONS...

Did you know that the average *Electronic Design* reader is a 41-year-old male with 15 years of experience and an income of $55,000? Our annual Careers Special: Reader Salary Survey examines some of the issues that are uppermost in the minds of design engineers. News Editor Sherrie Van Tyle presents data gathered from a study of our domestic readers. Read about it in the October 10 issue of *Electronic Design*...

As digital signal-processing technology becomes more pervasive, semiconductor manufacturers are being pushed to come up with ever-more-powerful DSP chips. In the October 10 issue of *Electronic Design*, a Special Report by Semiconductor Editor Dave Bursky will give you a clear picture of the latest trends and issues surrounding these important ICs...

Our PC Design Series was created specifically to serve the needs of our many readers developing PCs and peripherals. Everything from chip sets and single-chip solutions to CISC and RISC microprocessors, high-density memories, graphics, microprocessors, chip sets, peripherals, add-on/add-in boards, buses, interfaces, input devices, and software are thoughtfully discussed from the systems designers' point of view. In addition to these features, *Electronic Design's* October 24 issue will also carry our definitive PC Chip Sets Designer's Guide. This is an issue you'll want to keep and refer back to...

Because of the complexity of today's design's, testing has become a significant cost factor. In our October 24 preview of the ITC (International Test Conference), John Novellino, our resident Test & Measurement expert, examines the ATE/VLSI products and technologies that help reduce the high cost of testing...

Boasting over 125,000 attendees and 1,700 exhibitors, COMDEX is the definitive showcase for new computer-related products, from systems and software to semiconductors and peripherals. *Electronic Design's* show preview examines the latest technology and product introductions. We offer an insider's look at trends in the computer marketplace and analyze the implications of these trends. Computers Editor Richard Nass will also take a close look at the latest trend in storage technology...

In every issue of *Electronic Design*, our Technology Newsletter, New Products, and Quick Look sections bring you the latest in test & measurement, computer-aided engineering, and components. And our innovative Ideas For Design show you how to hook up the total system—from passive to active components.

while the TC of external resistors won't track the DAC, and may not track each other.

IT TAKES ALL KINDS

Although simpler in complexity and operation, DACs are more difficult to categorize than ADCs. As mentioned earlier, general-purpose and high-speed DACs represent two major categories. The former breaks down into current- and voltage-output types, and into the number of DACs per IC. For example, you can have single-DAC ICs with voltage output *(Table 1, again)*. Or you can have dual, quad, and octal current-output DACs *(Table 2, again)*, or dual and quad, voltage-output DACs *(Table 3, again)*. Every category contains fixed-reference DACs and MDACs, and each DAC within each category may or may not have a reference. That is, a DAC without its own reference isn't necessarily an MDAC, and an MDAC may contain a dc reference. On the other hand, high-speed IC DACs can be broken out into current-output types *(Table 4, again)* and deglitched voltage-output types *(Table 5, again)*.

Like ADCs, DACs can also be categorized by technology (process and/or architecture), features, and applications. And, as noted earlier, while performance specifications are growing less important for general-purpose types, features and I/O are becoming the way to differentiate between DACs.

Using specifications to select a DAC has dwindled in importance for two quite different reasons. First, virtually all of the DACs available today meet basic dc-accuracy specifications—they're 12-bit accurate over temperature. Second, most applications for general-purpose DACs don't need more speed or bandwidth than is readily available.

Though monotonicity for 12-bit DACs is usually guaranteed over temperature, and differential nonlinearity or DNL (which determines monotonicity) is usually guaranteed to be within 1 LSB over temperature, and always within 1 LSB at 23°C, both specifications are often actually better. Most suppliers offer DACs with superior dc specifications. Integral nonlinearity (INL), or relative accuracy, are similarly specified. For example, Analog Devices' AD667J guarantees a DNL of ±3/4 LSB at 25°C and monotonicity over temperature *(Table 1, again)*. The higher-grade AD667K guarantees a DNL of ±1/2 LSB at 25°C and it too guarantees monotonicity over temperature. Minimum INL for the two models run ±1/2 and ±1/4 LSB at 25°C, and ±3/4 and ±1/2 LSB over temperature, respectively.

TABLE 1. GENERAL-PURPOSE, VOLTAGE-OUTPUT, 12-BIT DACs

Model	Company	Reference: Int.	Reference: Ext.	Reference: Mult.	Settling time (μs)	Offset error (±LSB) Unipolar 25°C	Unipolar Over temp.	Bipolar 25°C	Bipolar Over temp.	Full-scale range(V)	Bus access time (ns)	Nominal supply voltage (V)	Power dissipation (mW)	Price (1000s)	Digital I/O	Features	Packages
AD667	Analog Devices	•	•		3	0.5	0.5	0.5	0.5	±2.5, ±5, ±10, 5, 10	100	±15	375	$9.90	1, 2, 3, 4	21, 22	41, 42
AD767	Analog Devices	•	•		3	0.5	0.5	0.5	0.5	±2.5, ±5, ±10, 5, 10	50	±15	600	$8.40	9	21, 22	43
DAC-HZ12	Datel	•	•		3(t)	2	2	NS	3	±2.5, ±5, ±10, 5, 10	NS	±15	390	$42	1	21	41
DAC-HK12	Datel	•			3(t)	2	2	NS	3	±2.5, ±5, ±10, 5, 10	NS	±15, 5	700	$68	1, 2, 3	21	41
AD7848	Analog Devices	•	•		4	NS	NS	4	4	±3	57	±5	95	$8.40	1, 5	24, 25	41, 44
AD7845	Analog Devices	•	•		5	0.5	0.5	0.5	0.5	Up to 10, ±10	140	±15	210	$6.30	1, 4	22, 23, 24	42, 43, 44
DAC813	Burr-Brown	•	•		5	0.5	0.5	9	9	±5, ±10, 10	NS	±15	270	$9.00	1, 2, 4, 8	26	43, 48
MAX501	Maxim		•	•	5	NS	NS	0.5	0.5	±10	55	±15	210	$5.65	10	24, 29	43, 49
MAX502	Maxim		•	•	5	NS	NS	0.5	0.5	±10	55	±15	210	$5.65	9	24, 29	43, 49
AD7233	Analog Devices	•			10	8	8	6	6	±5	NS	±15	210	$5.95	6	28	45
AD7343	Analog Devices	•	•		10	8	8	6	6	±5, 5, 10	NS	±15	210	$5.95	6, 7	26, 27	46, 47

Digital I/O
1 = 12-bit parallel
2 = two banks of latches (double-buffered)
3 = 12-bit parallel input register with three sets of 4-bit latches. Takes data in any combination of 3-bit nibbles in one, two, or three bytes.
4 = 12-bit DAC latch
5 = 8-word FIFO with input and DAC registers
6 = serial
7 = can be daisy-chained
8 = 2-byte input latch, 4 MSBs + 8 LSBs
9 = 12-bit single-input latch (single-buffered)
10 = 12-bit-wide, 2-byte input latch, 8 MSBs + 4 LSBs

Features
21 = op-amp summing junction available
22 = microprocessor compatible
23 = four on-chip gain-setting resistors
24 = ac specifications
25 = FIFO
26 = Clear/Reset logic input sets all bits to zero
27 = operates from single or dual supplies
29 = three on-chip gain-setting resistors

Packages
41 = 28-pin double-width DIP
42 = 28-pin LCCC
43 = 24-pin "skinny" DIP
44 = 28-pin PLCC
45 = 8-pin DIP
46 = 16-pin DIP
47 = 16-pin SOIC
48 = 28-pin SOIC
49 = 24-pin SOIC

All specifications are maximums or minimums are at 25°C, unless noted typical (t), and are over temperature. Int. = internal. Ext. = external. Mult. = multiplying. Settling time is to within ±1/2 LSB of final value for a full-scale step. All devices are lowest-cost models, which guarantee 12-bit monotonicity over temperature. NS = not specified.

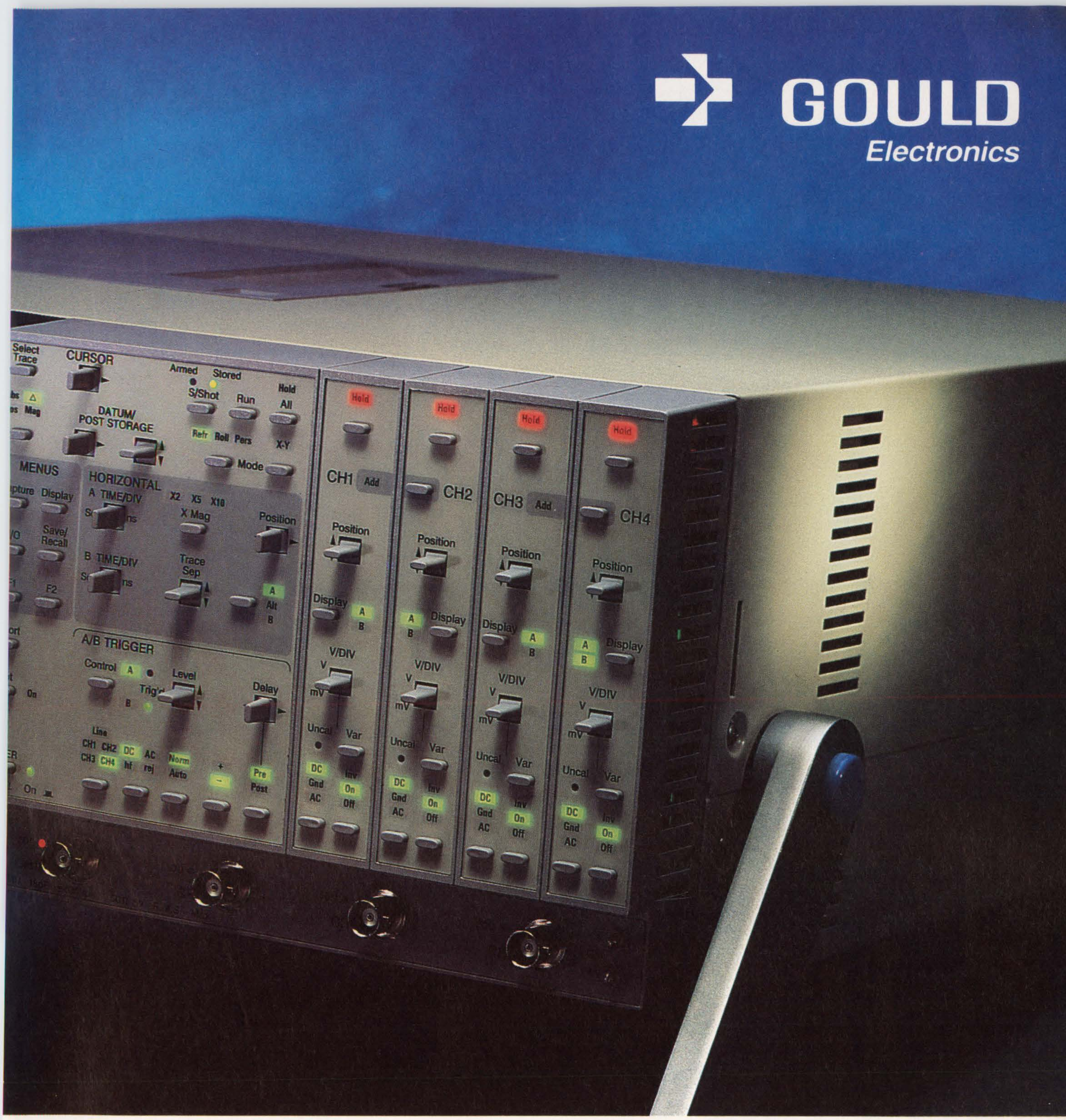


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TABLE 2. DUAL, QUAD AND OCTAL, GENERAL-PURPOSE 12-BIT CURRENT-OUTPUT DACs

Specifications/features	Units	DAC7800/01/02	AD7537/47/49	HS7584	AD7568
Company	NA	Burr-Brown	Analog Devices	Sipex	Analog Devices
DAC type					
Number of DACs	NA	Two	Two	Four	Eight
On-chip reference	Y/N	N	N	N	N
External reference	Y/N	Y	Y	Y	Y
Multiplying	Y/N	Y	Y	Y	Y
Specifications					
Monotonic (OT)	Y/N	Y	Y	Y	Y
Settling time	μs	0.8	1.5	3	0.5
Full-scale output	mA	1	1	1	1
Bus access time	μs	0.04	0.1	0.1	0.04
Supply voltage	V	5	15	5	5
Power	mW	10	30/30/45	50	17.5
Price	1000s	$8.40	$12/$12/$14	$27	$23
Feedthrough (10 kHz)	dB	–72	–70	NS	–66
DAC matching	%	3	3	NS	2
Crosstalk (10 kHz)	dB	–90	–70/–70/–62 (t)	NS	–76 (t)
Digital I/O	NA	2, 6/2, 10/9	2, 10/9/12	1, 2, 10	6, 7
Features					
Clear/Reset input	Y/N	Y/Y/N	Y/N/Y	N	Y
Reference input/DAC	Y/N	Y	Y	Y	Y
Analog ground/DAC	Y/N	Y	Y/N/Y	N	Y
Latch/DAC	Y/N	Y	Y/Y/Y	Y	Y
Readback	Y/N	N	N	N	Y
Packages	N/A	46, 47/43, 49/43, 49	43, 44/43/50-52	53, 55	56

Digital I/O
1 = 12-bit parallel
2 = two banks of latches (double-buffered)
6 = serial
7 = can be daisy-chained
9 = 12-bit single-input latch (single-buffered)
10 = 12-bit-wide, 2-byte input latch, 8 MSBs + 4 LSBs
12 = 8-bit-wide, two-byte (double-buffered) input, 4 MSBs + 8 LSBs

Packages
43 = 24-pin "skinny" DIP
44 = 28-pin PLCC
46 = 16-pin DIP
47 = 16-pin SOIC
49 = 24-pin SOIC
50 = 20-pin DIP
51 = 20-pin PLCC
52 = 20-pin LCCC
53 = 44-pin PLCC
55 = 40-pin DIP
56 = 44-pin quad flat pack

All specifications are maximums or minimums at 25°C, unless noted typical (t), and are over temperature (OT). Settling time is to within ±1/2 LSB of final value for a full-scale step. All devices are lowest-cost models, which guarantee 12-bit monotonicity over temperature. NS = not specified. NA = not applicable.

Offset and gain errors also run less than an LSB over temperature, and these are usually adjustable to zero. In a system with an autocalibration mode, additional DACs, such as 8-bit devices, can often trim the offset and gain errors to zero.

CAVEAT EMPTOR

Because DAC data-sheet specifications are often confusing and difficult to understand, making an error budget has become a designer's nightmare. There's a need to standardize units used to define dc errors, for example. One number should also be used to specify bus-access time. More and better MDAC ac specifications are needed, as are additional specifications for dual, quad, and octal DACs.

Not only should there be standardization among suppliers, but standardization throughout individual data sheets as well. All dc errors should be in LSB at 25°C or in LSB over temperature. Although some improvement has been made in recent years, data-sheet error units are still typically distributed between LSB, percent of full-scale range (FSR), percent of FSR/°C, ppm of FSR/°C, and sometimes even in millivolts or mV/°C.

Recently, several suppliers of 12- and 8-bit ADC suppliers have begun moving to a "total unadjusted error over temperature" (TUEOT) specification. Such a specification can truly help a designer determine system performance. A TUEOT specification can slash production costs by reducing test time.

Bus access time usually must be deciphered from a table that lists half-a-dozen time periods, such as address-setup time, address-hold time, data-setup time, data-hold time, chip-select-to-write setup time, write-to-chip-select hold time, and write-pulse width. But when selecting a DAC, the user first wants to know how long that DAC needs to be on the processor's bus. And processors are getting faster every day.

MDACs need ac specifications for the reference input, including feedthrough, bandwidth, settling time, and distortion. Adding such details can potentially increase their use significantly. Moreover, multiple-DAC ICs need the matching and isolation between DACs on the chip to be specified. Some suppliers, however, provide some of these specifications *(Tables 1-5, again).*

Several new features, aimed directly at simplifying system design, are now being added to general-purpose 12-bit DACs. For example, the Clear or Reset input permits a host processor to reset a DAC's output to zero at power-up or at the start of a calibration cycle. A Readback input, which lets the host check the last digital word latched in the DAC, relieves the host's memory of that chore prior to each update. It also increases system reliability by permitting the host to double-check the word in the DAC at any time. It's an inherent feature of most serial-I/O DACs, which also have a serial digital output that can be daisy-chained.

A feature found on some multiple-DAC chips is a separate reference input per DAC. Such a feature may be mandatory for some circuits, especially on MDACs that may be used to set the gain of multiple channels. When this feature is unavailable, it's usually because of a pin-limited package—remember, the bigger the package, the more expensive the device. It's obviously most practical to offer this feature on a device with a serial I/O like the Analog Devices AD7568, which still uses 42 of its 44 pins.

Eight of the 44 pins are used for a separate ground per DAC. Thus, dc bias can be added to the output to take advantage of the chip's operation from a single 5-V rail. A feedback resistor is also provided for each DAC. Multiple DACs containing undedicated op amps (like the Burr-Brown DAC2814/15 and DAC4814/15), and/or op amps on the reference input (such as the Burr-Brown AD7237 and AD7242) are also beginning to arrive. The op amps make it easier to drive the circuit's resistor networks and/or invert input or output signal polarity.

Application Dynamics

It wasn't long ago that true 12-bit DACs were expensive. Major applications included using the DAC in a successive-approximation ADC (often military) and in creating vector-scan CRT images, such as those used in "heads-up" displays for military aircraft and air-traffic control. Both demanded speed in the form of minimal settling time. And the displays

TABLE 3. DUAL, QUAD GENERAL-PURPOSE 12-BIT VOLTAGE-OUTPUT DACs

Specifications/features	Units	DAC2813/14/15	DAC4813/14/15	AD7237/47	AD7242	AD7837/47	AD664	AD75004	DAC8412/13	MAX526	SP9345	MN1900
Company	NA	Burr-Brown	Burr-Brown		Analog Devices			Analog Devices		Maxim	Sipex	Micro Networks
DAC type												
Number of DACs	NA	Two	Four	Two	Two	Two	Four	Four	Four	Four	Four	Four
On-chip reference	Y/N	Y	Y	Y	Y	N	N	Y	N	N	N	Y
External reference	Y/N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N
Multiplying	Y/N	N/Y/Y	N/Y/Y	N	Y	Y	Y	N	N	N	N	Y
Specifications												
Monotonic (OT)	Y/N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Settling time	µs	6/10/10	6/10/10	10	3	4	10	4	6(t)	10	15(t)	NS
Output range	V	c/c,e,h/c,e,h	c/c,e,h/c,e,h	b,d,e	g	c	c,e or e	b	c,e	e	c	c
Supply voltage	V	±15/±15,5/±15,5	±15/±15,5/±15,5	15,-15 (opt.)	±5,±15	±15	±15, 5	±12	5 to ±15	10, -5	±15	±15, 5
Power	mW	570/430/430	1140/830/830	165, 300 (opt.)	195	240	525	720	60 to 330	400	618	1845
Price	1000s	$18/$15/$15	$26/$22/$22	$13	$12	$13	$30	$30	$30	$35	$45	$327 (100s)
Feedthrough (10 kHz)	dB	NS	NS	NS	NS	-90(t)	-75 (1 kHz)	NS	NS	NS	NS	NS
DAC matching	LSB	NS	NS	±0.2(t)	NS	±0.2(t)	±1/2	±1	±1	NS	NS	NS
Crosstalk (10 kHz)	dB	NS	NS	NS	-110(t)	-95(t)	NS	NS	NS	NS	NS	-80
Digital I/O	NA	1,2/6,7/2,10	1,2/6,7/2,10	2,12/1,9	6	12/9	2,3	12	1,2	12,13	1,2,10	1,2
Features												
Clear reset input	Y/N	Y	Y	N	N	N	Y	N	Y/Y	N	Y	N
Reference input/DAC	Y/N	N/Y/Y	N/Y/Y	Y/N	Y	Y	N	N	N	N	N	Y
Analog ground/DAC	Y/N	N	N	N	Y	Y	N	N	N	N	N	N
Undedicated op amp	Y/N	N/Y/Y	N/Y/N	N	N	N	N	N	N	N	N	N
Input amplifier/DAC	Y/N	N	N	Y/N	Y	N	N	N	N	N	N	N
Readback	Y/N	N	N	N	N	N	Y	N	Y	N	N	N
Packages	NA	41	41	43,44	43,48	43,49	41,53	54	41,42,43	43	41	57

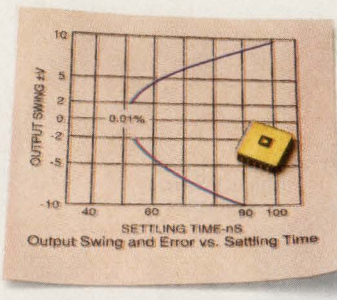
Full-scale output ranges
b = ±5 V, c = ±10 V, d = 5 V, e = 10 V, g = ±3 V, h = -10 V

Digital I/O
1 = 12-bit parallel
2 = two banks of latches (double-buffered)
3 = 12-bit parallel input register with three sets of 4-bit latches. Takes data in any combination of 3-bit nibbles in one, two, or three bytes.
6 = serial
7 = can be daisy-chained
9 = 12-bit single-input latch (single-buffered)
10 = 12-bit-wide, 2-byte input latch, 8 MSBs + 4 LSBs
12 = 8-bit-wide, two-byte (double-buffered) input, 4 MSBs + 8 LSBs
13 = 8-bit-wide, two-byte (double-buffered) input, 8 MSBs + 4 LSBs

Packages
41 = 28-pin double-width DIP
42 = 28-pin LCCC
43 = 24-pin "skinny" DIP
44 = 28-pin PLCC
48 = 28-pin SOIC
49 = 24-pin SOIC
53 = 44-pin PLCC
54 = 24-pin double-width DIP
57 = 40-pin triple-width DIP

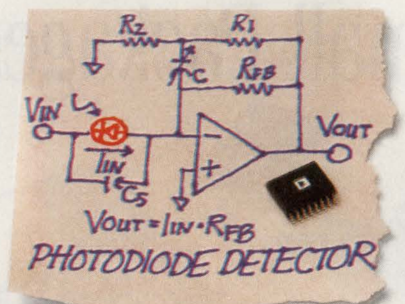
All specifications are maximums or minimums are at 25°C, unless noted typical (t), and are over temperature (OT). Settling time is to within ±1/2 LSB of final value for a full-scale step. All devices are lowest-cost models, which guarantee 12-bit monotonicity over temperature. NS = not specified. NA = not applicable. Opt. = optional.

Whether you fax it, fire it, send it, measure it, wire it, compute it, The Analog family of



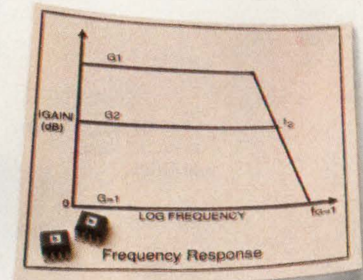
Precision

With the AD840, AD841 and AD842, there's no need to trade speed for accuracy. All three settle to 0.01% within 100 ns (840/842) and 110 ns (841) – critical in data acquisition and instrumentation applications – and offer low offset voltages and drifts, and fast slew rates.



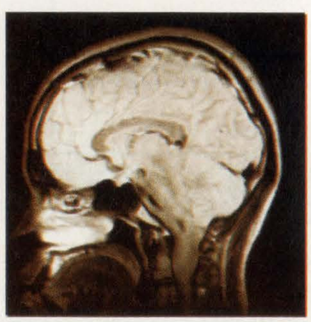
FET Input

For op amps requiring low input current, the OP-42, OP-44, AD845 and AD843 are all remarkably fast – slew rates are 58, 120, 100 and 250 V/μs, respectively. In addition, they offer offset voltages of less than 1 mV and extremely low current noise.



Transimpedance Amplifiers

The OP-160, OP-260, AD844, AD846, AD9617 and AD9618 all utilize a current feedback architecture to achieve slew rates from 450 to 2000 V/μs without compromising stability – even in hostile environments. Other benefits include low power dissipation and high unity-gain bandwidth.



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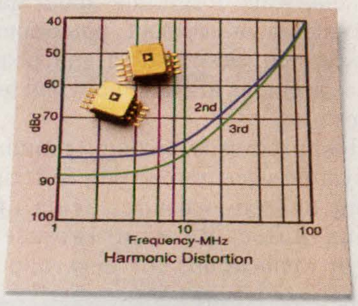
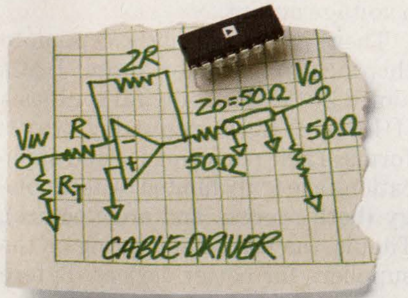
shoot it, launch it, land it, test it, display it or air it, we've got it. high-speed op amps.



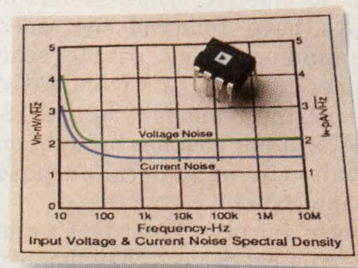
Buffers

If you're looking for extremely low distortion buffers, look at the specs of the AD9620 and AD9630 – distortion at 20 MHz: − 73 dBc and − 66 dBc, respectively; fast settling time: less than 8ns to 0.02%; and extremely low noise: 2.2 nV/$\sqrt{Hz}$.



General Purpose

With the right combination of speed, precision, power dissipation and high output drive capability, the AD827, AD829, AD847, AD848, AD849 and OP-64 are ideal general purpose solutions. And they're ideally priced solutions – most singles are under $3, and duals are under $5.



Low Noise

It used to be you had to choose between speed or low noise. But with the AD829, you get both. It features voltage noise of 2 nV/$\sqrt{Hz}$ and current noise of 1.5 pA/$\sqrt{Hz}$ with a 50 MHz unity-gain bandwidth. Those specs, combined with the low price of $2.95/100s, make it ideal for both audio and video applications.

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needed minimal glitches as well *(Tables 4 and 5, again)*. They also found more mundane applications in the feedback loop of industrial control systems and machine-tool and military-positioning systems. Moreover, all of these applications required monotonicity over temperature.

Applications are now changing as prices for monolithic 12-bit IC DACs continue to drop. Vector-scan CRT displays have gone the way of the steam locomotive. High-resolution displays have followed the video game and workstation to raster-scan machines driven by 8-bit RAMDACs. However, the availability of true 12-bit DACs at low cost has brought on an avalanche of general-purpose DAC applications.

General-purpose 12-bit DACs aim to be practical devices that simplify system design. This means that most general-purpose applications don't need to be blazing fast. While settling times from 5 to 50 μs are sufficient for a majority of general-purpose applications, the settling time of most voltage-output general-purpose DACs now runs between 3 and 10 μs. If that's not fast enough, current settling times can run as low as 0.5 μs, and plenty of op amps can convert that to a 0.5-μs settling time for a voltage output.

There is one glaring exception to this lack of need for speed: DACs aimed at the direct-digital synthesis (DDS) of high-frequency waveforms. Their performance and applications are truly limited by technology (both process and architecture). That is, the market is beating on the suppliers for better devices. Before talking about these denizens of the RF world, you may want to know just where are all of the zillions of general-purpose 12-bit DACs being used? And why do they need 12 bits?

True, not all applications need 12-bit resolution, let alone 12-bit accuracy. However, you should consider 12-bit devices if more than 8 bits is required, because few 10-bit DACs are available. Moreover, you can usually drop 12-bit DACs directly into 8-bit-DAC sockets, while forgetting about gain and offset adjustment potentiometers. Again, design time and board space is cut, as are assembly and test times.

Host-processor analog trimming of system zeros and setting and trimming system voltage levels and gains (autocalibration) represent major applications for general-pur-

TABLE 4. HIGH-SPEED 12-BIT CURRENT-OUTPUT DACs

Specifications/ conditions	Units	AD568k/ 668	AD9712/13	DAC65	DAC812	CAT104/ 105/506	CLC912	DAC-HF12	TDC1012/1112
Company	NA	Analog Devices		Burr-Brown		Catalyst	Comlinear	Datel	TRW
Basic applications	NA	TD	FD	FD	TD	FD	FD	TD	FD
Basic specifications									
DNL over temperature	±LSB	0.5	4	0.75	1	2	0.5	0.5	2
INL over temperature	±LSB	0.25	4	0.75	0.5	2	1	0.5	2
Monotonic over temperature	Y/N	Y	N	Y	Y	Y	Y	Y	NS
DAC type									
In-package reference	Y/N	Y	Y	Y	Y	Y	N	Y	N
Multiplying	Y/N	N/Y	Y	N	N	N	N	N	N
Logic	NA	TTL	ECL/TTL	ECL	TTL	TTL	TTL	TTL	TTL/ECL
Input latches	Y/N	N	Y	N	N	Y	N	N	N
Supply voltage	V	±15	±5	±15	±15, 5	5	±5	±15	±5, -5
Quiescent current	mA	32 (+15), -9 (-15)	20 (+5), -165 (-5)	30 (+15), -65 (-15)	40 (+15), -50 (-15), 40 (+5)	75	35 (+5), -150 (-5)	45 (+15), -15 (-15)	25 (+5), -180 (-5), -180 (-5)
Full-scale output current	mA	a,b	c	d	e,f	j	j	h,i	40
Compliance-voltage range	V	-2 to 1.2	-2 to +3	±1.25	±4	±1	±1.2	±1.2	±1.2
Dynamic Specifications									
Update (clock) rate	MHz	NS	100/80	35	NS	25/25/40	20	NS	20/50
Settling time									
From digital input	μs	0.035(t)/ 0.09(t)	0.03(t)	0.030(t)	0.055(t)	0.040/ 0.040/ 0.020	0.025(t)	0.050(t)	0.02
To % of full-scale range	%	±0.025	±0.025	±0.024	±0.012	NS/NS/ ±0.025	±0.025	±0.025	0.02
Glitch impulse (area)	pV-s	350(t)	100(t)	250 LSB-ns	NS	100(t)	25(t)	NS	25(t)/20(t)
Spurious-free dynamic range	dBc	NS	-65(t)/-55(t)	-66	NS	NS/NS/-58	-58	NS	70(t)
Update (clock) rate	MHz	NS	50	20	NS	NS/NS/20	20	NS	20
Output frequency	MHz	NS	5	5	NS	NS/NS/1	5	NS	5
Package	NA	a	b,c	d	e	a	d	d	d
Price	1000s	$28	$30	$25	$75	$44/NS/$54	$30	$155	$28/$31

TD = time domain. FD = frequency domain. DNL = differential nonlinearity. INL = integral nonlinearity. NS = not specified. NA = not applicable. All specifications are maximums or minimums at 25°C unless noted typical (t).

Full-scale output current
a = 10.24 mA, b = ±5.12 mA, c = 20.48 mA, d = ±6.25 mA, f = -10 mA, g = ±5 mA, h = 5 mA, i = ±2.5 mA, j = 40 mA.

Packages:
a = 24-pin "skinny" DIP, b = 28-pin DIP, c = 28-pin PLCC, d = 24-pin double-width DIP, e = 24-pin triple-width DIP

pose 12-bit DACs. In ATE systems, they set the levels on the pin-receiver comparators and on the pin drivers, and de-skew the time delays. In industrial control systems, the DACs provide both set-point and feedback signals. Taking the output of a host computer or processor, they control position, velocity, and acceleration of linear and rotary motion. Typical examples include the relative position and speed of motion between a machine tool's work piece and the cutting head, the position of robot arms and valves, the acceleration and deceleration of material movers, and the speed control of the motors in a printing press.

Instrument applications for 12-bit DACs include programmable power supplies/voltage-current sources, waveform generators (sine, function, and arbitrary), and pen-motor positioning in X-Y recorders. In instruments and data-acquisition systems, they implement autocalibration, adjusting gain and offset. Previously, 12-bit DACs positioned electron beams in CRTs. Now they can do it in electron-beam lithography systems. Feeding a high-voltage op amp, such as the Apex PA41, these DACs can drive a piezo "inchworm" micropositioning motor (ELECTRONIC DESIGN, *June 27, p. 47)*. DACs with a serial digital I/O save pins, package size, and space on the pc board needed for running parallel buses, and permit readback operation. They're also a natural for digital-signal processors, where they can pump out serial data while the processors run calculations. MDACs lend themselves to digitally-programmable, variable-frequency filters and remote gain control.

WHERE IT'S AT

Almost from their introduction, DACs have been used to generate waveforms. But in this instance, designers usually used whatever devices were available to do the job. It was only recently that a true market was defined: DDS or reconstruction of clean low-distortion high-frequency waveforms. Such applications are rampant in military and commercial sectors. The military uses these DACs in jam-proof and/or secure spread-spectrum and frequency-hopping radar and communications systems. Programmed by processors, 12-bit IC DACs shift carrier frequencies at far greater rates and more accurately than was possible with earlier techniques (such as voltage-controlled oscillators and phase-locked loops). In all of these systems, both receiving and transmitting, the DACs do the job of the local oscillator.

Spread-spectrum and frequency-hopping systems are also wending their way into the commercial and consumer worlds. Applications range from wireless LANs on the factory floor to cellular-telephone and other personal communication systems currently under development. Once available at reasonable cost, microwave systems can also use DDS. Presently, professional video equipment is moving from 8-bit DACs to higher-resolution converters. And, if devices with the right mix of specifications and price become available, the move to 12 bits—especially with the rapid rise of HDTV—will accelerate.

Conceptually, DDS systems are simple *(see the figure, p. 64)*. Moreover, the theory and basic techniques for such systems have been around for 25 years. Only recently, though, have DACs and digital ICs been able to do the job in a DDS system, outside the audio range.

A DDS system consists of three basic blocks: a phase-angle generator, a sine-wave lookup table (a memory), and a DAC. The phase-angle generator is typically a regenerative adder with latches. It functions simply as a phase register, adding appropriate phase increases at specific intervals. The lookup table converts the phase position from the phase generator into a specific input code for the DAC. It, in turn, generates the analog output signal. The length of the word from the phase generator, and the frequency of the reference clock, determine the system's frequency resolution.

The phase-angle generator (the register) holds the output frequency's phase angle in the form of a fraction of one cycle. Additional bits just give the fraction greater resolution. The output frequency consists of the clock frequency multiplied by the phase-increment fraction—the amount the actual phase is updated every reference-clock cycle. Using a 24-bit adder, the output frequency f_{OUT} becomes:

$$f_{OUT} = \frac{2^{24}}{\text{Phase increment}} f_{clock}$$

Much of the output-phase noise is controlled by ensuring that the reference-clock signal sent to the DAC latches has very low phase noise. Most DDS systems operate over a well-defined, relatively narrow bandwidth in the range of a few tens of kilohertz to several megahertz. The DAC output is filtered to smooth the sharp edges of the output staircase and eliminate any harmonics of the carrier in its operating band.

TABLE 5. HIGH-SPEED 12-BIT DEGLITCHED VOLTAGE-OUTPUT DACs

Specifications/conditions	Units	DAC-02320DAC	02315/DGL-02316
Company	NA	ILC Data Devices	
Basic applications	NA	Time domain	
In-package reference	Y/N	Y	Y
Logic	NA	TTL	ECL
Input latches	Y/N	N	N
Full-scale output voltage	mA	±10, ±5, 10	NS
Update (clock) rate	MHz	15	35
Settling time			
From digital input	ns	180	50
To % of full-scale range	%	0.01	0.01
Glitch impulse (area)	pV-s	750	530
Package	NA	24-pin double DIP	Two, 24-pin double DIPs
Price	1000s	$163	$455

All specifications are maximums or minimums at 25°C, unless noted typical (t), and are over temperature. Settling time is to within ±1/2 LSB of final value for a full-scale step. All devices are lowest-cost models, which guarantee 12-bit monotonicity over temperature. NS = not specified. NA = not applicable.

The key to superior DDS performance, however, is the DAC. That's because the spectral purity of the sine wave represents the single most important system specification. The DAC must convert the theoretically-pure digital-input words into a usable analog waveform. Any nonlinearity in the DAC creates unwanted signal energy in the form of noise and increased harmonics. The latter are usually called spurious frequencies, or "spurs." The key specification for DDC DACs is called a "spurious-free dynamic range," or SFDR. It's essentially the ratio of the amplitude of the output sine wave's largest harmonic to the amplitude of that output sine wave (the carrier), expressed in dBc, or dB below the carrier. Because the ratio is a fraction, it will usually carry a negative sign. However, some DAC suppliers delete the sign. They home in on the word "range," considering that SFDR is a measurement of the number of decibels between the harmonic and the carrier.

Two additional specifications are required to define DDS-DAC performance for the rated SFDR: the maximum update rate (maximum reference-clock frequency) the device can handle, and the maximum useful output frequency. Theoretically, output frequency can go up to one-half the clock frequency (Nyquist). However, system designers use a "rule of thumb" that says useful outputs are possible up to about 20% of the clock frequency. Though settling time, glitches, DNL, and INL are all important specifications, particularly for fast 12-bit DACs, no one has been able to correlate any of these specifications directly to the SFDR parameter. In essence, we're revisiting the 1970s. DAC suppliers must use all their magic (and luck) to design the best possible DAC. Then they build it and characterize it—then they know what they have. In fact, it may be possible to build lower-cost 10-bit DACs with SFDRs that will do jobs now using 12-bit DACs.

Two families of these DACs from three suppliers virtually own the DDS field. But they're being challenged by another pair *(Table 4, again)*. Presently, the AD9712/9713 (ECL/TTL) from Analog Devices, offering maximum clock rates of 100 and 80 MHz, respectively, are capable of the highest output frequencies. At a 50-MHz clock rate, and while providing an output frequency of 5 MHz, the data sheet specifies a typical SFDR of –60 and –55 dB for the ECL and TTL devices, respectively (the only conditions for which SFDR is specified). However, the settling times of both are typically 30 ns. The DNL and INL of both are also the same. DNL runs a maximum of 2 LSB, and INL a maximum of 3 LSB. The glitch impulse (area under the glitch) for each is typically 100 pV-s (picovolt-seconds).

MYSTERY CHIPS

The best SFDR is provided by TRW's TDC1012/TDC1112 (TTL/ECL) DACs, the first of which is also available from Comlinear as the CLC912. Both company's basic specifications are similar. But their data sheets, although very complete, are very different. Comlinear doesn't use SFDR, but rather calls out a signal-to-(noise + distortion) or SINAD specification. However, this is just a difference in wording. Either way, both specifications indicate the dynamics of the DACs' operations. According to Comlinear, if they had created the data sheet (dated December 1988) just a few months later, they too would have used SFDR (TRW's data sheet is dated 1990)—an indication of this fast-moving field.

TRW specifies the TDC1012's SFDR at its maximum clock rate of 20 MHz (typically 25 MHz) within a 10-MHz bandwidth at four output frequencies of 1, 2, 5, and 6 MHz. Minimum SFDR at 6 MHz runs 60 dB (TRW uses dB, not –dBc). Typical SFDRs at 1, 2, and 5 MHz run 78, 75, and 70 MHz, respectively.

The TDC1112 guarantees a minimum clock rate of 50 MHz and specifies SFDR with 32- and 40-MHz clocks. With the 32-MHz clock, typical SFDR is 67 dB when putting out 12 MHz, and 68 dB when putting out 10 MHz. With a 40-MHz clock, typical SFDRs run 72, 70, and 63 dB at output frequencies of 1, 5, and 16 MHz, respectively. Note that SFDR isn't substantially improved with the faster DAC.

A look at linearity specifications shows that even the DAC manufacturer has difficulty correlating DNL and INL specifications with SFDR data. TRW, for example, provides four versions of the DACs with maximum DNLs of 1/2, 1, 2, and 4 LSBs (remember, DNL must be better than ±1 LSB for monotonicity), while their maximum INLs run 1, 2, 2, and 4 LSBs, respectively. All four versions, however, offer identical SFDR specifications, all settle to within 1/2 LSB in under 35 ns maximum, and all have maximum glitches of 35 pV-s.

Burr-Brown and Optimum represent the newcomers to the field of DACs for DDS applications. Burr-Brown announced the DAC65 a few months ago, and now "startup" Optimum is announcing the CAT506 *(Ta-*

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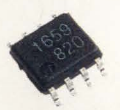

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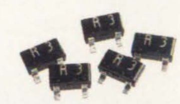

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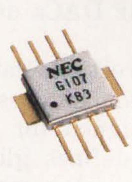

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ble 4, again). The DAC65 specifies SFDR at clock rates of 20 and 35 MHz. At 20 MHz, SFDR typically runs –73, –70, and –66 dBc for output frequencies of 0.1, 1, and 5 MHz, respectively. For the same output frequencies, but with a 35-MHz clock, SFDR typically runs –71, –68, and –61 dBc, respectively. The DAC65 typically settles to 1/2 LSB in under 35 ns, and its glitches typically run under 250 LSB-ns. Maximum INL and DNL are better than 1 LSB.

The CAT506 is built on a biCMOS process, unlike all of the other DDS DACs that employ bipolar technology. Its footprint meets that of the discontinued Brooktree CMOS Bt104 and Bt105. Like Comlinear, Optimum specifies SINAD instead of SFDR. With a 20-MHz clock, the CAT506 typically runs –59 dB while putting out 500 kHz, and –58 dB putting out 1 MHz. With a 5-MHz clock, SINAD increases to –65 and –64 dB, respectively. Maximum clock rate is 40 MHz. The DAC typically settles to within 1/2 LSB in 22 ns and 35 ns maximum. Glitch impulse is typically 100 pV-s. And like the DAC65, INL and DNL are better than an LSB. Both of these DACs meet general-purpose-DAC criteria.

Though conventional current-output DACs provide only 1 or 2 mA of current, DDS DACs offer quite a bit more. Their full-scale currents range from 6.25 mA for the DAC65, to 20 mA for the AD9712/13, to 40 mA for the remainder of the DDS DACs. Most DDS DACs have an internal load resistor through which the current can be passed to develop an ac voltage on the order of 1 V. In fact, the settling time specification is usually based on the voltage developed across this resistor. On the other hand, with the exception of the DAC65, none have the usual application resistors used with an op amp to create a voltage output found in conventional current-output DACs. And the TRW/Comlinear DACs don't contain a reference.

While there's no direct correlation between DAC SFDR and glitches, all DDS DACs are designed for low glitches. Comlinear defines glitch-impulse area as the analog output transient that occurs when switching between two adjacent codes as a result of unequal turn-on and turn-off times for the internal current sources. Burr-Brown defines it as the difference in the waveform at the DAC's output when skew between the data bits is and isn't present. A glitch occurs when the digital data changes from one code to the next and the bits don't all switch at the same time. The delay between when the first and last bits switch is called skew time. During the skew time of the digital data, which includes the DAC switching, the digital code is undefined and the DAC output can go to any current or voltage level between full-scale maximum and minimum values.

In the past, so-called deglitched DACs were built by adding sample-and-hold amplifiers at the output *(Table 5, again)*. DDS DACs, on the other hand, are carefully designed to minimize internal skew. External skew in the arriving words on the digital bus is minimized by adding latches ahead of the DAC and strobing all of the bits into the DAC after they've been latched. All but the DAC65 contain such latches on the chip. Burr-Brown suggests that adding a deglitcher can improve SFDR by as much as 10 dB. It would be interesting to see what adding a deglitcher to other DDS DACs could do for system performance.

In most high-resolution DACs, one or more of the higher-order bits are segmented to ensure monotonicity. In a segmented DAC, multiple equal-current sources replace the more-common binary-weighted sources and the R-2R networks. However, an n-bit segmented DAC requires 2^n-1 current sources. For example, in a segmented 4-bit DAC, eight equal current sources would be used for the MSB, four more identical sources for the next lower bit, two more sources for the next lower bit, and one source for the LSB. A totally-segmented, 12-bit DAC doesn't make efficient use of silicon compared with one that employs binary-weighted techniques using one source per bit.

Until the recent arrival of the DAC65, it could at least be considered that the greater the number of MSBs segmented, the better the SFDR. The TRW/Comlinear DACs segment the six MSBs. With about 10 dB less SFDR, the Analog Devices units only segment the top four MSBs. The DAC65, on the other hand, employs no segmentation, relying instead (like the 8 LSBs of the AD9712/13) on a well-trimmed and stable thin-film R-2R network. The remainder of these DDS DACs use diffused resistors. In a different twist, the CAT506 is trimmed with an on-chip EEPROM.

The major DDS applications for high-speed 12-bit IC DACs potentially represent just the tip of the iceberg. These DACs essentially replace phase-locked loops in current designs, because they switch frequency quicker, more accurately, and often at lower power and cost. In most cases, the signal's output bandwidth is a few megahertz at most. That is, the output frequency may be varied from 1 to 1.1 MHz, or from 5 to 7 MHz. As faster DACs become available and users begin to realize what truly can be achieved with them, clock rates and their associated output frequencies will begin to climb.

On the horizon for 12-bit DAC IC applications include local oscillators for IF amplifiers in the 20-MHz range, then on to 35 MHz, 80 MHz, and finally to the raw, transmitted output signal itself. Even clock rates of 2 GHz aren't out of the question. By using MDACs like those from Analog Devices, the modulation can be applied to the reference input, letting the clock create the carrier.

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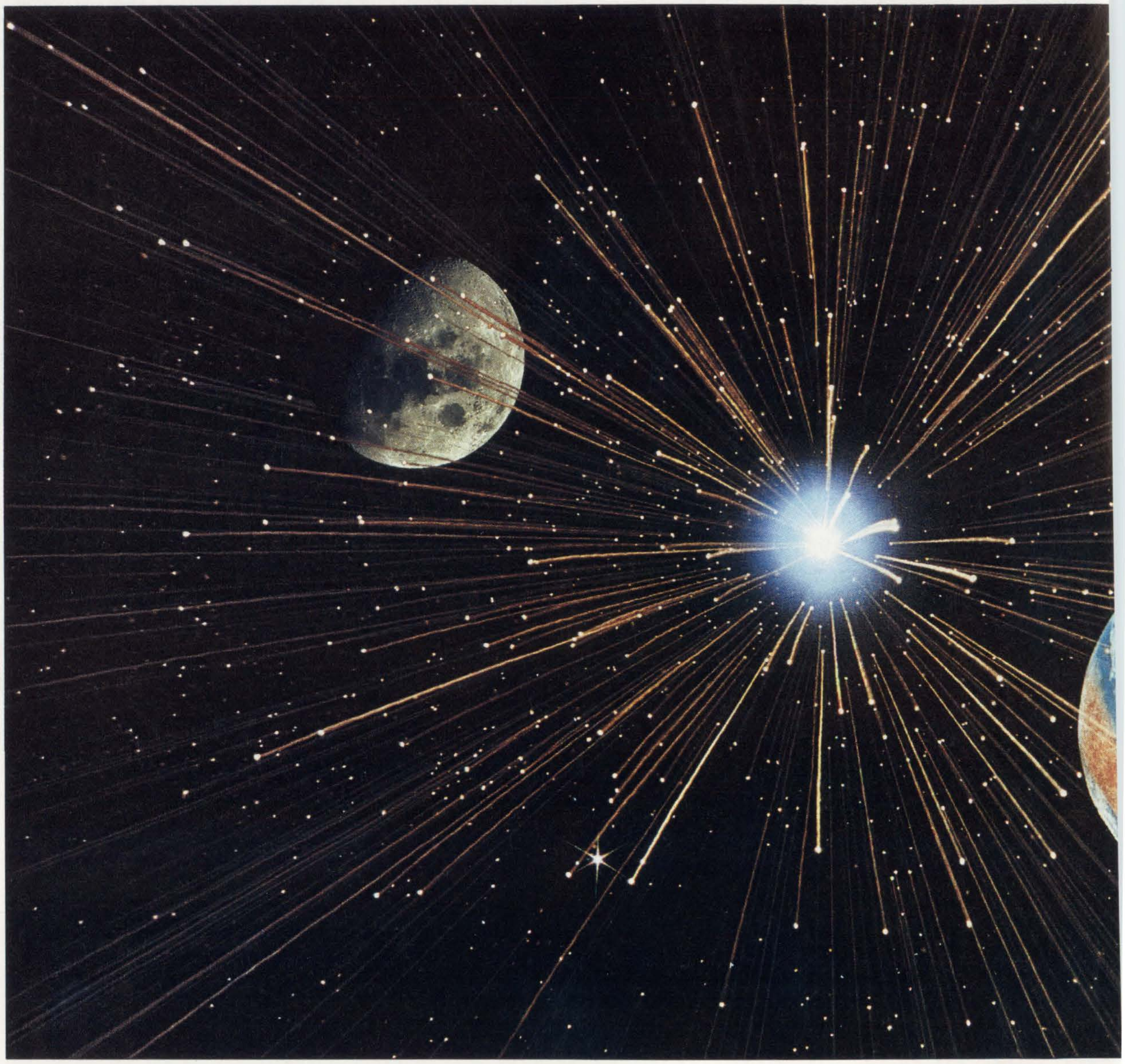

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ELECTRONIC DESIGN REPORT

12-BIT DIGITAL-TO-ANALOG CONVERTERS

The first quantum jump in actual hardware could occur late this year or early next in Burr-Brown's DAC650. This mixed-technology 12-bit DAC is expected to have a clock rate of 500 MHz and settle to 1/2 LSB in 5 ns. The two-chip hybrid uses silicon for those circuits that determine accuracy, stability, and linearity, and employs gallium arsenide for speed-driven circuits. In addition, Triquint Semiconductor has a contract with the Defense Applied Research Agency to produce a 14-bit, ultra-fast, GaAs DAC.

In the future, general-purpose DACs will to continue to offer additional features and octal DACs picking them up. Very low-cost single and multiple 12-bit DACs designed for trimming circuits and systems, most probably circuits with serial I/O, are also in the works. These DACs' monotonicity will be a must, but INL will be less important—perhaps 10 LSBs or whatever specification will provide a 6-sigma yield without testing. There will be further use of on-chip EEPROM for trimming, initially by the supplier, and ultimately by the user. Power needs and supply voltages will continue to drop, because the need for DACs to run off 3.3- and even 2-V rails is just a matter of time. Such DACs will have to be true single-supply devices.

More and more custom, or customer-specific, DACs will enter the fold, such as the Analog Devices quad AD75004 *(see Table 3, again)*. Called an LSM for Linear System Macro, it's made of cells from a standard-cell library. It's the fastest-settling 12-bit quad, voltage-output DAC available, with a 4-μs maximum rating. And while you can buy it off-the-shelf, the company would just as soon tailor and package it to fill specific user needs. Because the cells needed for such changes are in a library, NRE costs to modify an LSM typically run one-third to one-half those of conventional ASICs.□

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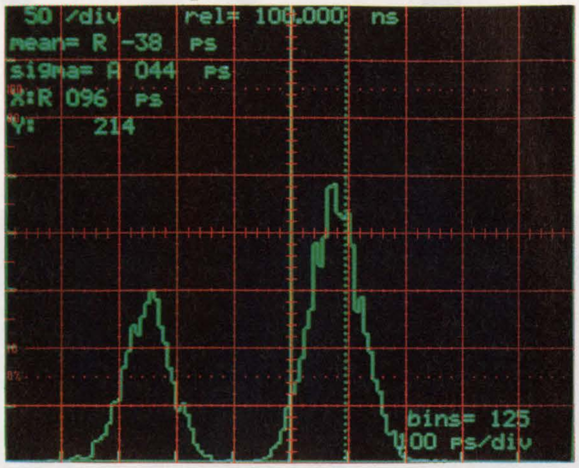

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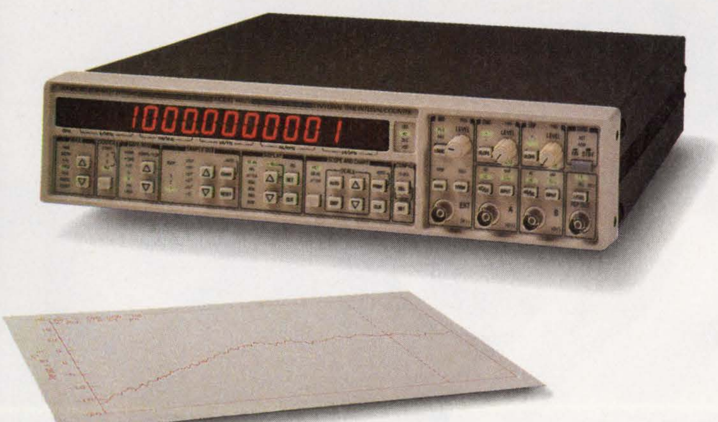

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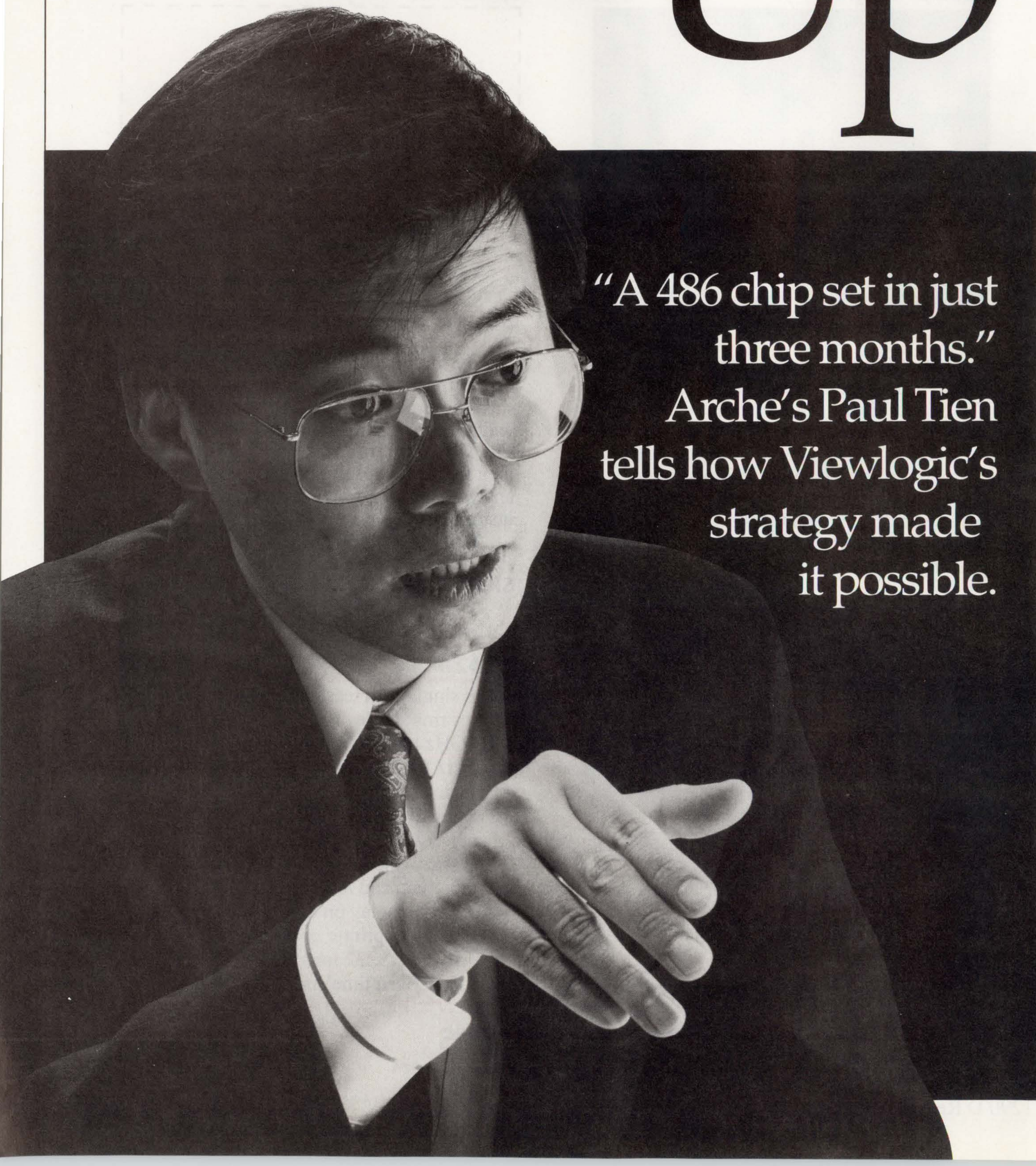

“A 486 chip set in just three months.”
Arche’s Paul Tien tells how Viewlogic’s strategy made it possible.

GUIDE TO DESIGNING WITH HIGH-SPEED CMOS ICs

DESIGNERS NEED TO KNOW HOW TO DEAL WITH CMOS'S INPUT IMPEDANCE AND FAST SWITCHING.

RUDY STERNER
Advanced Micro Devices, 901 Thompson Pl., P. O. Box 3453, Sunnyvale, CA 94088-3000; (408) 732-2400.

CMOS has undergone a major revolution. It started out as a slow, low-power solution with limited application. However, CMOS manufacturers have dramatically increased their products' speed. In fact, CMOS is now a viable alternative to bipolar technology in all but the fastest applications.

This trend is expected to continue, with the fastest CMOS devices equaling or exceeding the performance of the fastest bipolar devices. In particular, high-speed CMOS programmable logic devices are pushing leading-edge technology.

But to use this technology efficiently, a highly disciplined approach based on an understanding of high-speed design methods is required. For most designers, a CMOS device's internal architecture is a less compelling consideration than linking it to the real world in which it lives.

A good analogy to designing with high-speed CMOS devices is the difference between driving a good family car and a high-performance race car. The family car is a slow to fast vehicle, designed to get someone from point A to point B in relative comfort. The driving skills required are well within the realm of any good driver. In contrast, the high-performance race car is an exceedingly fast vehicle designed for optimum performance. The driver of this vehicle must understand the car's interface with the road—at high-speeds—to fully exploit the added performance.

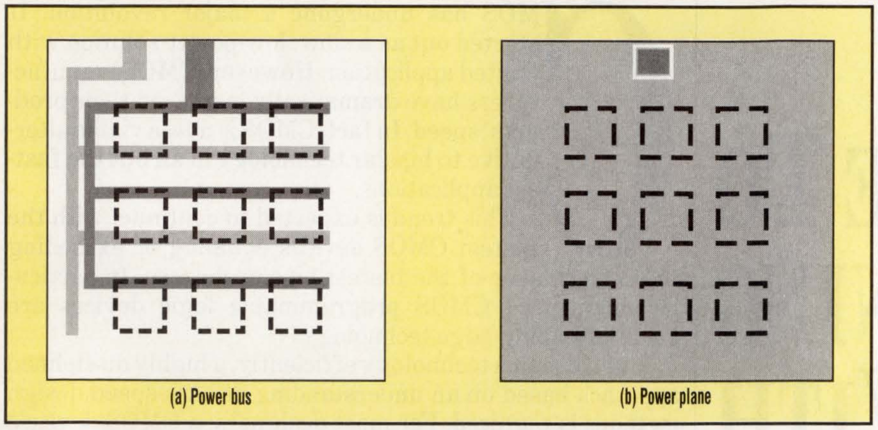
In the same manner, the designer of high-speed systems must be aware of the device-board interface. For instance, failing to consider signal-return paths could result in increased inductance, which causes excessive ringing and crosstalk. Improper termination could cause a signal to be so distorted that it would be rendered unusable. And ground bounce could result in reduced system speed or double clocking. As speed increases, these issues become even more pressing.

Two aspects of CMOS are critical to designing with the technology: high input impedance and fast switching. Input impedance is typically hundreds of thousands of ohms, effectively an open circuit. Switching time can be just 5 ns for a relatively slow part, such as a device with 25-ns propagation delay (t_{PD}).

Because MOS transistors are voltage-controlled devices, the only input current is the leakage current, which is usually less than 10 μA. As a result, the input impedance is extremely high. A signal line terminated only with high-impedance CMOS inputs has poor high-frequency characteristics. Spurious high-frequency noise is more easily coupled because there's nothing to dissipate the energy. In addition, the mismatch in impedance between the signal line and the CMOS input can result in reflections if the line is long enough to be considered a transmission line. Therefore, it's desirable to reduce the CMOS device's input impedance. This is usually done at the system level by terminating the signal line with an appropriate resistor value.

Fast edge rates with CMOS are of prime concern. Paradoxically, designers of CMOS devices must figure out how to slow down the edge, while designers of bipolar devices must find a way to speed up the edge. To date, the fastest

DESIGNING WITH HIGH-SPEED CMOS



1. BETWEEN THE POWER-DISTRIBUTION options, the power bus (a) is the most economical, but it has a relatively high resistance and contributes to larger current loops. The power plane (b) solves both of these problems. But an entire layer, or a large part of one, must be reserved for the power plane.

devices are bipolar but CMOS may overtake bipolar in the near future.

CMOS devices have faster edge rates because the CMOS transistor has a much higher gain than the equivalent bipolar transistor. Because of its higher gain, the CMOS device can conduct more current when it first turns on. This allows the load capacitor to discharge faster. Higher gain results in the CMOS output turning on sharper than the totem-pole-bipolar output. The extra kick CMOS gets at the start of a transition causes many problems. The extra energy contributes to ringing and transmission-line problems.

The power-distribution network has two separate functions. The first is to supply good, noise-free power to the devices on the board. Generally well-understood, this function should not present a problem to the system designer. The second is to supply a return path for every signal on the board. Noise and interference problems can occur if the signal return path isn't properly regarded. This especially holds true on high-speed boards.

Two options for power distribution are power buses and power planes *(Fig. 1)*. The power-bus network consists of two or more wide traces. One is for V_{CC}, another for ground, and the rest for other dc voltages required. This scheme is used whenever separate layers for power distribution are unavailable, typically when two-layer boards are employed. Power planes use an entire layer as a continuous-metal sheet. A separate layer is used for each voltage level required. Power planes require costly multilevel boards, yet they're the preferred solution for high-frequency systems.

The economical power buses are generally a poor choice technically. The buses have a higher dc resistance, which could result in a significant voltage drop. Buses also contribute to ground loops that cause noise problems.

Dc resistance of a trace is proportional to its cross-sectional area. By nature, power buses must be relatively narrow to make room for the signal traces. However, narrow traces mean high dc resistance and large voltage drops. Therefore, it's easier than might be expected to wind up with a 0.5-V drop from the power input connector to the device farthest from the connector.

On a power plane, the cross-sectional area includes the entire width of the board. This results in the smallest dc resistance possible and virtually eliminates dc voltage drops across the board.

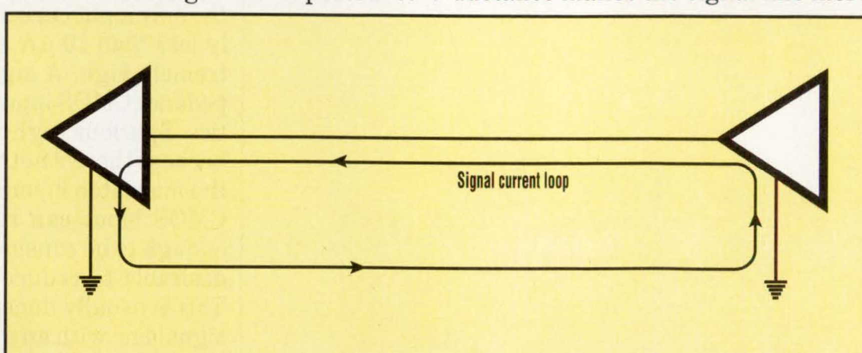
Power buses also contribute to ground loops, because the bus restricts the signal-return path, making it artificially long. A long return path results in a large ground loop.

To help visualize this, consider the source and load. A source is anything that generates a signal—dc, ac, or a logic transition. A load, the final destination of the signal, can be an unterminated input to a CMOS device. For this discussion, CMOS input impedance is so high that it can be considered an open circuit.

If the signal is dc, the load may not draw current. This depends on the nature of the termination. However, if the signal is ac or a transition, the load draws current because the load always has some capacitance (typically around 5 pF for a CMOS PLA device). Current flow is guaranteed by the relationship $i = C dv/dt$.

Current flow requires a closed loop. Therefore, with ac and transitions, there is a corresponding signal return path, which is through ac ground, either ground or V_{CC}. The combined signal and return path form a current loop that has an associated inductance *(Fig. 2)*.

In a signal line, inductance should be kept to a minimum. Excessive inductance makes the signal line more



2. THE SIGNAL PATH AND RETURN PATH for all signals make up an inductive loop. The return path is ac ground, which can be either ground or V_{CC}. Good design practice minimizes this loop.

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susceptible to problems, such as ringing, interference, and crosstalk. Power distribution schemes that contribute to signal-line inductance should be avoided.

The signal line and its corresponding return path can be considered two wires in an inductive loop *(Fig. 2, again).* Loop inductance can be approximated by:

$$L = Kl\,ln(d-r/r)$$

where

L = inductance
K = a constant
l = line length
r = radius of the wire
d = separation of the wires

The variable of interest is the wire separation (d). As the formula shows, inductance increases with wire separation. So inductance is minimized when the two paths are as close as possible—when the return path follows the signal path. With power buses, the signal return is constrained to follow the bus path. Unless the designer has the ground bus follow the signal line (which isn't always practical or possible), a large current loop develops. With power planes, the return path has no such constraint and follows the path resulting in the smallest loop.

In nature, everything tends to take the easiest path. The return path of a power plane is no different—it has the least impedance for ac signals. The impedance of a current loop is proportional to its inductance ($X_L = 2\pi fL$). The impedance is smallest when the inductance is smallest. Therefore, if no constraints exist, as with power planes, the signal return path follows the signal path whenever possible.

Ground and power planes supply the best overall power-distribution solution. They give wide paths for minimum inductance and resistance and allow the signal to take the optimal return path *(Fig. 3a).*

As good as power planes are, their benefits can be overridden by sloppy layout. If the plane is broken underneath the signal line, the return path must go around the break *(Fig. 3b).* Because the cut will make the loop larger, the signal will be more susceptible to noise problems.

It is possible to inadvertently put a break in the power plane. Components on the board require feedthroughs. These vias must be surrounded by a space to keep the signal from shorting to the power bus. Connectors and ICs have a whole row of vias. If they are wide enough to touch, they will result in a break in the power plane.

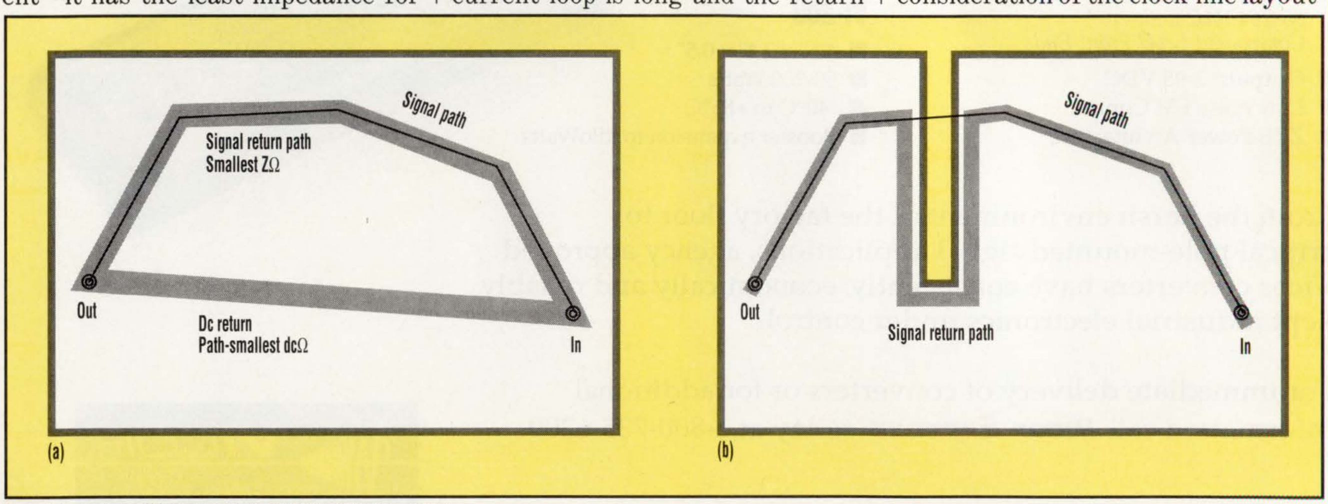
A VMEbus is a likely place for this kind of break to occur. If the holes for the connector pins are wide enough, the return current path is forced to the edge of the board. Here we have the worst of everything. The current loop is long and the return paths of various signals share the edge of the board. There's also high inductance and maximum crosstalk.

Layout Rules

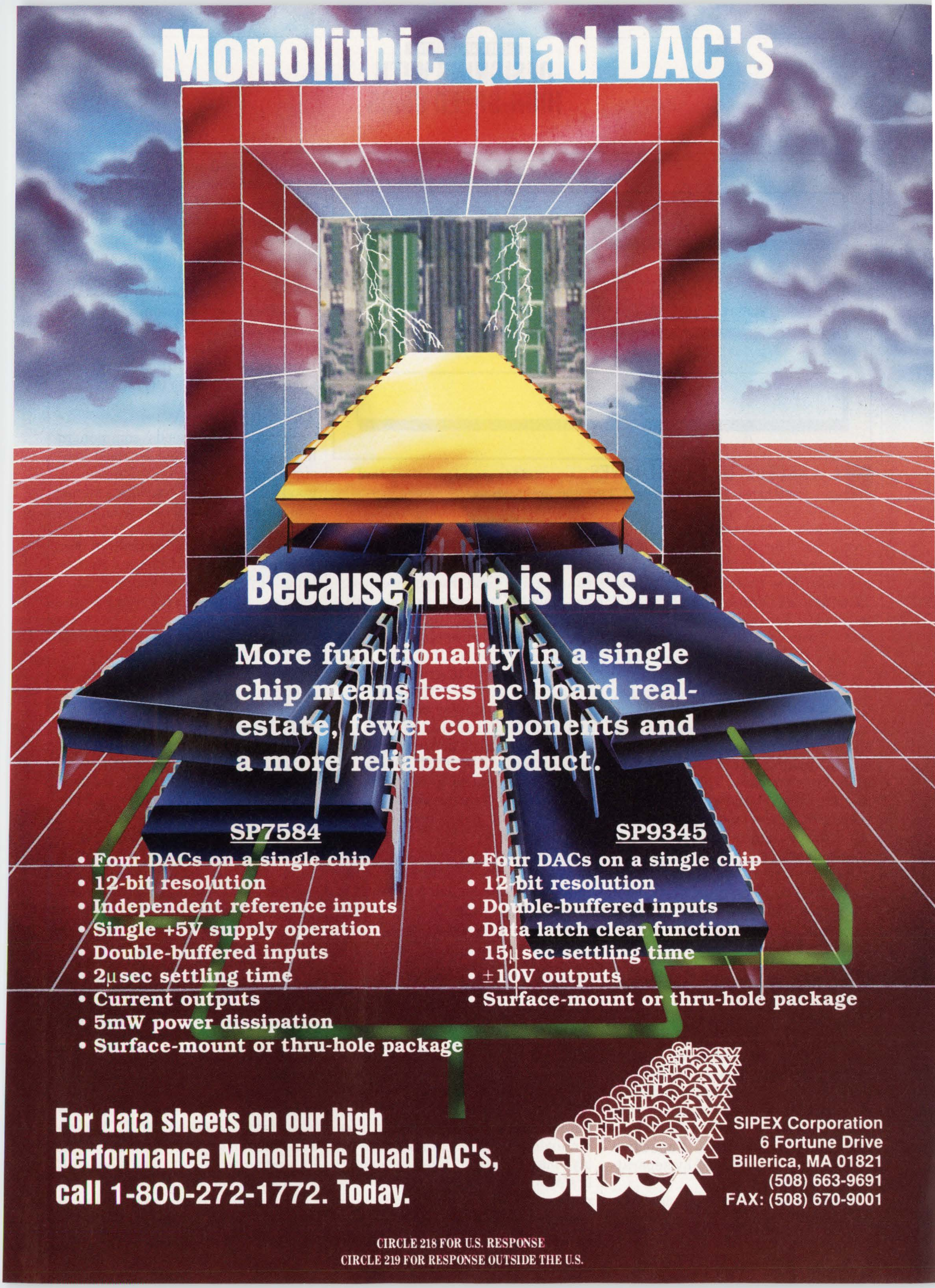
Armed with a handful of layout rules—besides using ground planes—a designer can avoid noise problems when using CMOS devices.

1. *Avoid artificial loops.* Any time a line loops back on itself or two sections of a signal line are reconnected after a split, there's a current loop. These loops have inductance and are subjected to all the associated problems. Keep a single line from the source to the loads; don't loop back.
2. *Keep signal lines as short as is practical.* Smaller signal lines are less susceptible to noise problems, such as radiation and crosstalk. If the devices were infinitesimal, this would not pose much of a problem. However, all devices have physical dimensions that must be accounted for. Inevitably, some related devices would have to be placed a distance from each other. It's a good rule of thumb to consider the physical layout issues at the early stages of the design cycle. Later headaches could thus be avoided.

A good example is the clock line, which has the system's highest frequency components. Radiation from long clock lines could cause interference both on and off the board. Early consideration of the clock-line layout



3. IN A SIGNAL RETURN PATH, dc follows the path of least resistance, which is the shortest path (a). Ac follows the path of least impedance, which is along the signal line. Note that any break in the return makes the loop larger (b). This could arise from an actual cut in the plane or vias for devices that are too close together.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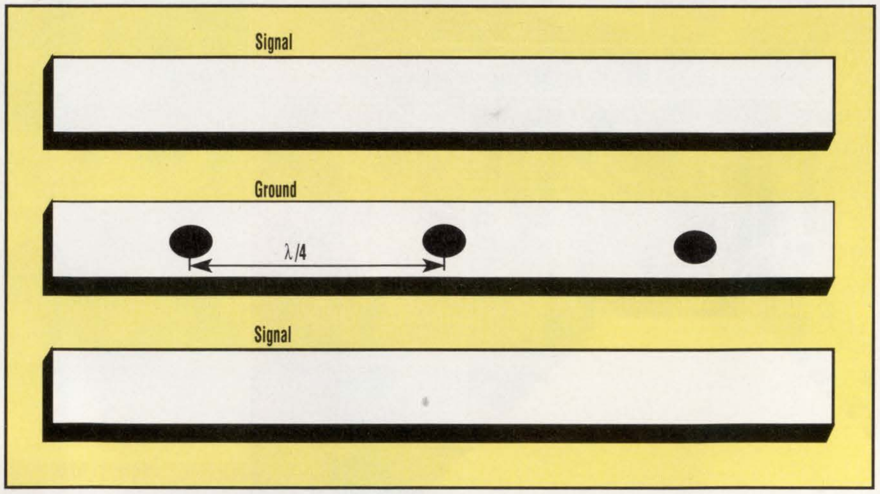


4. A SECTION OF SIGNAL LINES is separated by a ground trace. The ground trace should have taps to ground every λ/4 to ensure low impedance.

could help minimize potential for problems. The clock line should be laid out before any other signal lines.

3. *Signal-line traces should be 8 to 15 mils wide.* Traces thinner than 8 mils wide are more susceptible to noise. Traces wider than 15 mils tend to filter the signal, which increases the rise time.

4. *Avoid overlapping power planes.* Boards with mixed analog and digital signals usually have separate analog- and digital-power planes to isolate the analog-return path from the digital-return path. The planes are tied together at the power input to the board. If the power planes overlap (for example, the analog V_{CC} plane overlaps the digital-ground plane), the return paths can capacitively couple across planes, causing interference. It may be worthwhile to sacrifice a board and cut it around the plane boundary. No metal should be exposed on the cut edges except signal lines specifically intended to cross the boundary.

A common problem associated with long signal lines is crosstalk—unwanted coupling of data between signal lines. It comes in two flavors: inductive and capacitive. Inductive crosstalk is the transformer coupling between loops. It can be lowered by reducing loops. Capacitive crosstalk can be avoided by separating signal lines.

Sometimes signal lines can't be separated. Physical constraints may require running some signal lines in parallel for a few inches. In cases like this, crosstalk can be eliminated by running a ground trace between signal traces. Capacitive coupling will be to ground and not the other signal trace. A little care is required in this instance. The separating trace must be a short circuit to ground. A long trace tied to ground at the ends is the same as an inductor connected to ground. For maximum decoupling, the trace should be tied to the ground plane at periodic intervals. One tap to the ground plane every quarter wavelength (λ) of the signal's highest frequency component is sufficient *(Fig. 4)*.

The highest frequency component is related to the rise time (t_R) or fall time (t_F) of the signal, whichever is fastest. Separating the ground taps is determined by the formula:

$$\lambda/4 = \pi t_R / t_{PD} ft$$

where

λ = wavelength
t_R = rise or fall time (ns) (fastest)
t_{PD} = signal delay time (ns/ft)

By the way, t_R doesn't necessarily have anything to do with the clock or operating frequency. CMOS has inherently faster transitions than bipolar, even though the propagation delays may be longer. Even a seemingly slow CMOS device can have 2- or 3-ns transitions. Therefore, crosstalk could be a problem on relatively slow and high-speed systems.

For both inductive and capacitive coupling, the effect is maximized when load impedance is maximum. CMOS input impedance is extremely high (hundreds of thousands of ohms). As a result, CMOS devices are highly susceptible to crosstalk. The effect can be minimized by terminating the line at the load with a relatively small resistor. If practical, the resistor should equal line impedance, usually 50 Ω to 100 Ω.

TERMINATION

At switching speeds common to high-speed CMOS devices, most long signal lines are transmission lines. A good guideline is to consider a signal line a transmission line when line length exceeds two inches for every nanosecond of signal transition. For example, if a signal has a 3-ns rise time, any signal line longer than 6 inches should be considered a transmission line.

The layout philosophy discussed earlier (keeping close physical proximity between the signal line and ac ground) results in very good transmission lines—sometimes called controlled-impedance lines because the impedance of the signal line is nearly constant over its entire length.

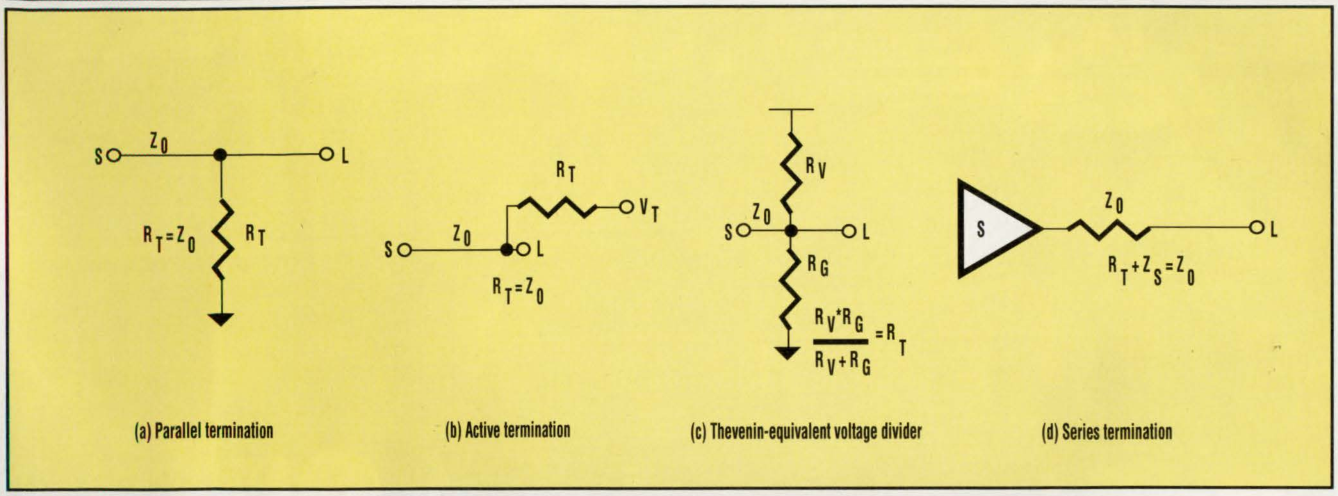
Good layout isn't enough, though. Even a well-laid-out controlled-impedance line tends to generate signal reflections if not terminated properly. Termination impedance should equal transmission-line impedance.

Now, let's turn to termination techniques. One basic scheme prevents reflections at the load, usually with parallel termination. The other method allows the first reflection at the load but prevents the second reflection at the source, usually with series termination. Each approach has advantages and drawbacks.

To stop reflections at the load, a designer must match load impedance (Z_L) to line impedance (Z_O). Remember that CMOS input impedance is essentially an open circuit. As a result, we must reduce Z_L to match Z_O by placing a resistor in parallel with the load that equals Z_O *(Fig. 5a)*.

Although parallel termination is cleanest, it may not always be practi-

DESIGNING WITH HIGH-SPEED CMOS



5. TWO TYPES OF TRANSMISSION-LINE termination schemes are parallel and series. Parallel can be implemented with one terminating resistor (a); a resistor and a separate voltage source (b); or a Thevenin-equivalent network (c). Series termination is implemented with a series resistor at the source (d). Parallel gives the cleanest results, but series has the smallest power drain on the source.

cal. Many CMOS devices are HCT compatible. This means that the devices are designed to work with TTL-level signals. The logic high level is rated at 2.4 V and –3 mA. A properly terminated 100-Ω transmission line (not unusual) would draw about 24 mA, which can't be maintained by the output driver. Obviously, an alternative approach is required.

One such approach is active termination *(Fig. 5b)*. The terminating resistor (R_T) is tied to a voltage source (V_T). V_T is ac ground, selected so that the high-level and low-level currents are within the driver's capabilities.

The advantage of active termination is that it allows correct termination of the line's load end without undue stress on the driver. Its disadvantage is that a separate power supply is required, which may be too expensive for many applications.

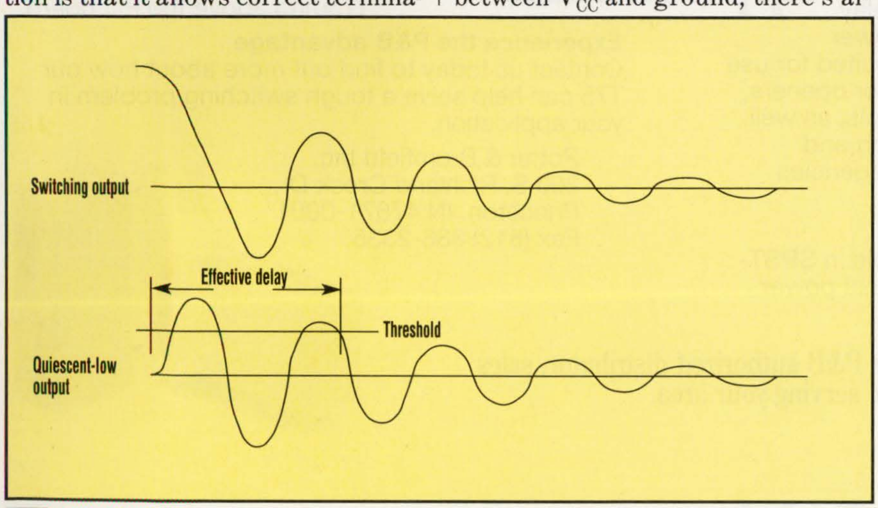
The expense of an active termination can be greatly reduced by replacing it with its Thevenin equivalent of two resistors: one to ground and one to V_{CC} *(Fig. 5c)*. Resistor values are chosen so that Thevenin-equivalent resistance is equal to R_T and the Thevenin voltage is equal to V_T. This technique has the benefit of the active termination without the extra power-supply expense. Unfortunately, because the resistors are between V_{CC} and ground, there's always some current flow. With active termination, this isn't the case. Sometimes, the active termination is chosen because it's less of a drain on the power budget.

The other approach to termination is to stop the second reflection at the source. The source is matched to the line. Driver impedances are typically in the range of 5 Ω to 20 Ω, which is lower than the line impedance. The terminating resistor must increase the source impedance to the line impedance by placing a resistor in series with the driver output *(Fig. 5d)*.

The advantage is that the series resistor doesn't provide a load to the driver. The disadvantages involve the difficulty of matching the source and a slow down of the signal caused by series termination.

HCT compatible drivers have three different impedances: low-state impedance, transition impedance, and high-state impedance. The low-state impedance is the smallest—around 20 Ω for 24-mA devices. The high-state impedance is usually greater than 50 Ω. Transition impedance is the output's impedance as it switches through the driver's linear region. It's somewhere between the two extremes.

Because the driver has different output impedances, the terminating resistor can't match exactly. Designers must choose a compromise value that allows some reflections, but at a



6. RINGING INDUCED ON A LOW OUTPUT, because of ground bounce, can be large enough to cross the input threshold of the receiving device. The ringing can be severe enough to cause false signals or double clocking.

DESIGNING WITH HIGH-SPEED CMOS

tolerable level. This is usually done empirically.

The series resistor also slows down the signal. The resistor and the capacitance of the line forms an RC time constant. This increases the delay of the output signal.

GROUND BOUNCE

Ground bounce is a type of intrachip crosstalk. A high-to-low transition is coupled to any output in the quiescent-low state. The coupling mechanism is the inductance of the common ground bus and ground-pin bonding wire. The transition causes a current surge through the chip ground. This surge leads to a ringing of the inductance, which is coupled to any output that's in the low state.

The CMOS device and the load make up an RLC network with a fast switch. The CMOS-output transistor is a fast switch. The load capacitance is the network's capacitance. The leads of the CMOS device are the resistance and inductance, of which inductance is more important.

As discussed earlier, CMOS's higher gain allows the load capacitance to discharge faster. The fast switching speeds result in a larger di/dt. The voltage across an inductor is $V = Ldi/dt$; therefore, the chip internal ground has a corresponding voltage spike.

Standard packaging techniques use one ground pin. Any signal on the ground pin is coupled to any output sitting low. When more than one output signal switches, the currents add and the voltage drops across the lead inductance increases. As much as 2 or 3 V can be seen on a quiescent output *(Fig. 6)*.

The first method when dealing with ground bounce should involve PLCC packages. The lead length in a PLCC package is a quarter of the maximum lead length in a DIP. Therefore, inductance associated with PLCC packages is a fourth of the inductance with DIP packages. By shrinking the inductance, the voltage pulse can be reduced.

Another way to reduce the voltage pulse is to lower the switching speed. Because $V = Ldi/dt$, lowering di/dt results in a smaller ground bounce.

A look at a data sheet shows that a safe input level is above –0.5 V. Dc input voltages below –0.5 V can cause a condition called latchup. When the device goes into latchup, V_{CC} is effectively shorted to ground. The resulting high current can destroy the device. The only way to bring a device out of latchup is to remove V_{CC}.

On high-speed systems, overshoots exceeding –1 V are common. But this does not cause the device to go into latchup. Latchup requires at least 200 mA and must be present for hundreds of nanoseconds. Overshoot typically lasts less than 20 ns. The signal itself won't have nearly enough energy to support 200 mA.

Overshoot shouldn't be ignored, though. Overshoot is usually followed by ringing *(Fig. 6, again)*. This slows down the system because the signal isn't valid until the ringing settles below the threshold voltage.

Ringing can be diminished by placing a diode between the end of the signal line and ground. When the signal goes to a diode drop below ground, the diode turns on and snubs the signal, thereby stopping the ringing. The diode must be faster than the signal's fall time. The longer it takes the diode to turn on, the less effective it will be. Any diode designed for microwave or RF applications would be a good candidate: One such example is the MBD101.□

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Rudolph Sterner, a senior applications engineer (member of the technical staff) at Advanced Micro Devices' Programmable Logic Group, holds a BSEE from San Jose State University.

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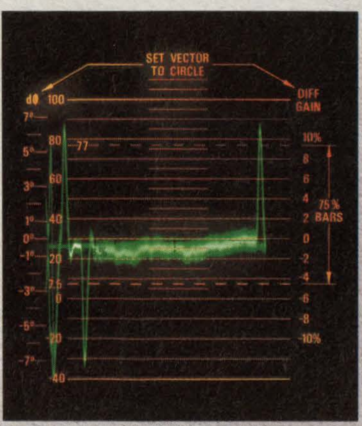

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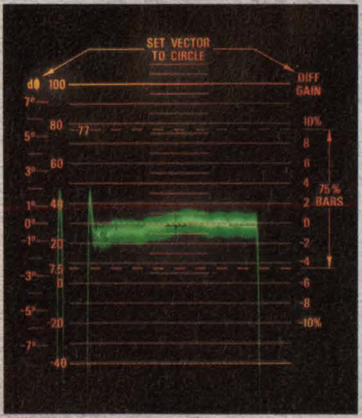

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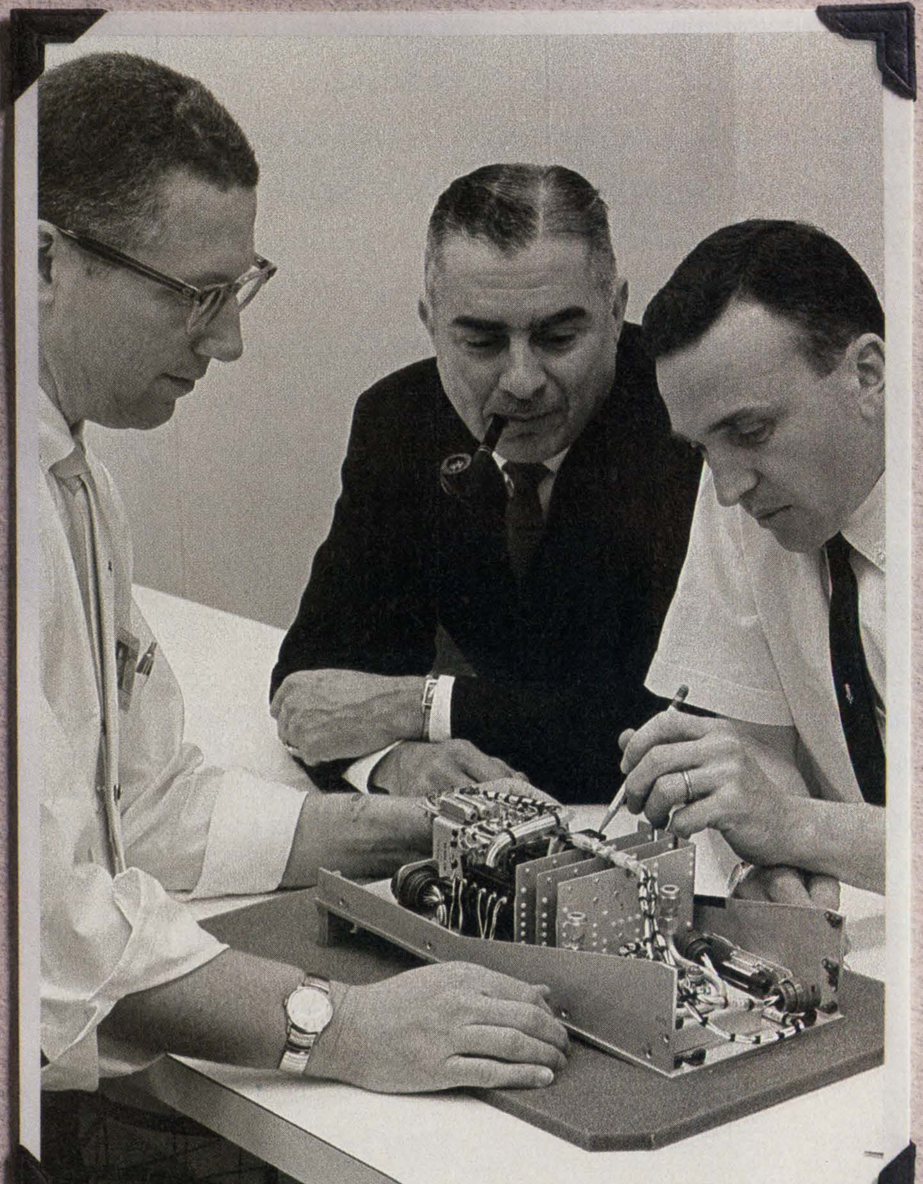

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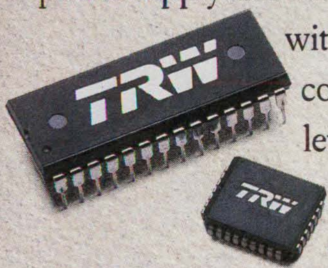

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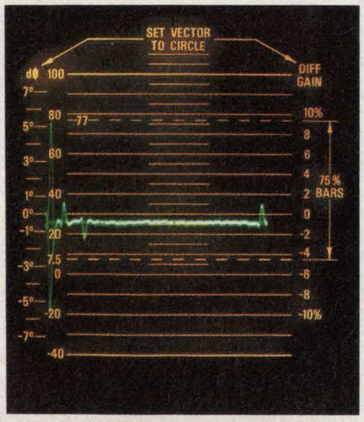

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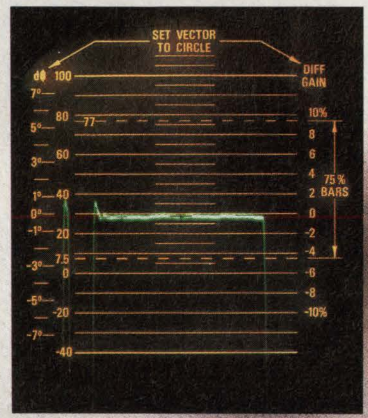

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A SPECIAL EDITORIAL FEATURE

Designing For PC SYSTEMS

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MULTICHIP MODULE PACKS PC NOTEBOOK LOGIC

AIMED AT THE HEART of most space-conscious notebook computers, a multichip module containing all of the motherboard control logic for 80386SX-based systems provides designers with one of the most compact solutions to date. Developed by Appian Technology Inc., Sunnyvale, Calif., the A90 module contains all standard peripheral control and power management functions in a 262-lead plastic pin-grid array package or a 256-lead quad-sided flat package. Appian also developed the logic chip set employed in the module—the System 90/SX local-bus chip set. The company's P94 power-management controller also is included. The local bus architecture of the logic chips bypasses the historically slow address and data-path bottlenecks of typical systems. By reducing the board area required by the large chips, the motherboard of a notebook PC can be reduced to an area measuring less than 30 in.^{2}. In 100-unit lots, the plastic PGA version of the A90 sells for $95. Contact Lou Williams, (408) 730-5465. DB **CIRCLE 560**

PADDLE FLOPPY CHIP SIMPLIFIES IDE CARDS

A SINGLE "PADDLE chip," which saves as many as ten chips currently used to implement the floppy-disk controller and IDE interface logic, makes the design of IDE interface cards a snap. The FDC37C75 puts the functionality of an entire floppy-disk controller and integrated-drive-electronics (IDE) interface into one 68-lead package. The chip, from Standard Microsystems Corp., Hauppauge, N.Y., includes the 765B floppy-disk controller, a digital data separator, address decoder, crystal oscillator, software and hardware power-down and reset capability, game-port decode logic, the IDE interface logic, and a 1.8432-MHz clock output for direct drive of external I/O devices. In lots of 10,000, the chip is $3.95. Call John Burgess, (516) 273-3100. DB **CIRCLE 561**

NOTEBOOK PC INCLUDES OVERHEAD LCD SCREEN

RATHER THAN FORCE users to purchase a separate LCD overhead projection screen when making computer-based presentations, designers at Rever Computer Inc., Taiwan, embedded the projection LCD as part of the standard flip-up flat panel used for typical data entry. For presentations, the display can be easily removed and placed on an overhead projector. The LCD panel provides a VGA-resolution, paper-white image with 16 shades of gray and a high contrast ratio. With an optional remote control or a wireless mouse, presenters can operate the system from anywhere in the room. A cooling cassette is included to prevent a projector's heat from harming the panel during long presentations. Both machines offered by the company—the 386SX-based Rever Cruiser 3S notebook and the older 286-based Cruiser 2—have the removable display. Both systems also include a normal-size keyboard, a 40-Mbyte hard-disk drive, a 1.44-Mbyte 3.5-in. floppy-disk drive, two serial ports, and one parallel port. The 3S has a list price of $3495 while the Cruiser 2 lists at $2495. Both systems will be sold in the U.S. by NovaCorp International Inc., Rochester, N.Y. Contact Gabe Hamidian, (716) 723-8640. DB **CIRCLE 562**

CHIP SET TRIMS EISA LOGIC TO A TRIO OF ICS

TAKING AIM AT SIMPLIfying the design of EISA-based PC motherboards, a chip set developed by Symphony Laboratories, Santa Clara, Calif., cuts the logic to just three 160-lead chips. Those chips include the SL82C471 cache and DRAM controller, the 82C472 EISA bus controller, and the 82C473 DMA controller. The chips enable a 386-based system to run at clock frequencies of up to 40 MHz, and 486-based systems to run at up to 50 MHz. Included on the 82C471 is a write-back cache controller with built-in tag comparator. Integrating the cache and DRAM control allows concurrent CPU-cache and DMA/master operations with bus snooping, improving system performance. To build a complete EISA motherboard with a baby-AT footprint requires just ten simple TTL components. Contact the company at (408) 986-1701. DB **CIRCLE 563**

CPU CARD TURNS MAC INTO MIPS WORKSTATION

A NUBUS CARD CONtaining an R3000 32-bit CPU module can turn an Apple Macintosh platform in a MIPS-based Unix workstation. The card, developed by Integrated Device Technology Inc., Santa Clara, Calif., contains IDT's version of the R3000 RISC processor, the companion floating-point unit, instruction and data caches, local DRAM storage, and space for an optional SCSI port that offers higher throughput than the standard Apple SCSI interface on the Mac. The Macstation 3 card comes in two versions, one that delivers about 15 MIPS and another that delivers about 25 MIPS. The slower card contains data and instruction caches of 16 kbytes each and 8 Mbytes of DRAM; the faster card has dual 64 kbyte caches and 16 Mbytes of DRAM. The faster card includes the optional higher-speed SCSI port as a standard feature. Software that ensures seamless communication between the card and the Macintosh is included, as is the Mips Inc. RISC/os Unix operating system, which comes pre-installed on a Macintosh-compatible hard disk. To allow Unix and Macintosh files to coexist on the same drive without partitioning the drive and enabling the files to be accessed by either processor, the company includes IDT/envY. It's an Ethernet virtual bridge software package that creates a virtual TCP/IP connection between the two operating systems. The card will initially be sold bundled with either a Mac IIci on the low end and with a Macintosh IIfx on the high end, for $17,175 and $21,175, respectively. It will include a 19-in. Supermac monitor and a 200-Mbyte external hard disk. Contact John Springer, (408) 727-8230. **CIRCLE 564**

Improve Clock Synthesis In Laptops With A Frequency Generator

A programmable frequency generator facilitates board layout that removes clock jitter and EMI.

RICHARD S. MILLER
Avasem Corp., 1271 Parkmoor Ave., San Jose, CA 95126; (408) 297-1201.
PAUL F. BEARD
Technical Success, 3823 Perie Ln., San Jose, CA 95132; (408) 254-2780.

Computer systems require several different clock frequencies to operate the CPU, integrated chip set, and various peripheral devices. For example, in video graphics applications, various frequencies are used to support different monitors and graphics standards (such as EGA and VGA). At present, expensive oscillators and crystals generate these frequencies.

Integrated programmable frequency generators (PFGs) eliminate the need for multiple oscillators and crystals. Phase-locked-loop (PLL) circuitry is the foundation for the integrated frequency generators. These circuits reduce board space, lower power consumption, and improve power management while decreasing component costs. In addition, frequency generators are easier to place on the circuit board with IC packages in either a through-hole or surface-mounted manufacturing environment.

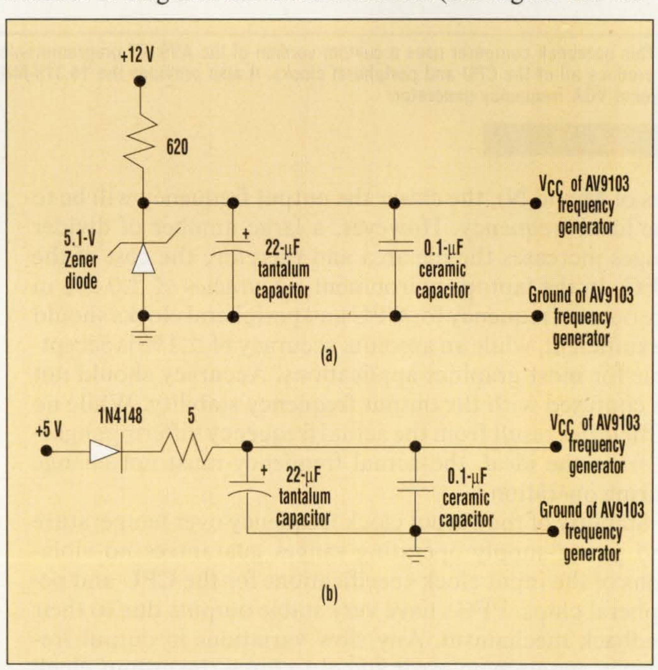
A PLL system configured for frequency generation consists of a phase comparator/charge pump, a loop filter, a voltage-controlled oscillator (VCO), and two divider blocks. The VCO is an oscillator whose output clock frequency is proportional to the VCO input voltage. During normal operation, the input voltage to this oscillator is forced to a given value to produce the desired output frequency. The phase detector has two input clocks, one that's the input reference frequency (f_R) divided by N (an integer value), and a second that's a scaled version of the output f_{out} divided by M (another integer value). A low-frequency signal output by the phase detector is proportional to the phase difference between the two input signals. The phase detector controls the charge pump.

The loop filter converts the charge pump's output to a voltage and eliminates any high-frequency components. The filter's voltage is the VCO input voltage, completing the loop. The PLL system causes the frequencies f_R/N and f_{out}/M to be equal. If f_{out}/M drifts to a higher frequency, an error signal is generated by the phase detector/charge pump. This reduces the input voltage to the VCO, causing the output frequency to be forced back to the desired value. Because of this feedback mechanism, the system can synthesize a stable output frequency that's proportional to a reference frequency.

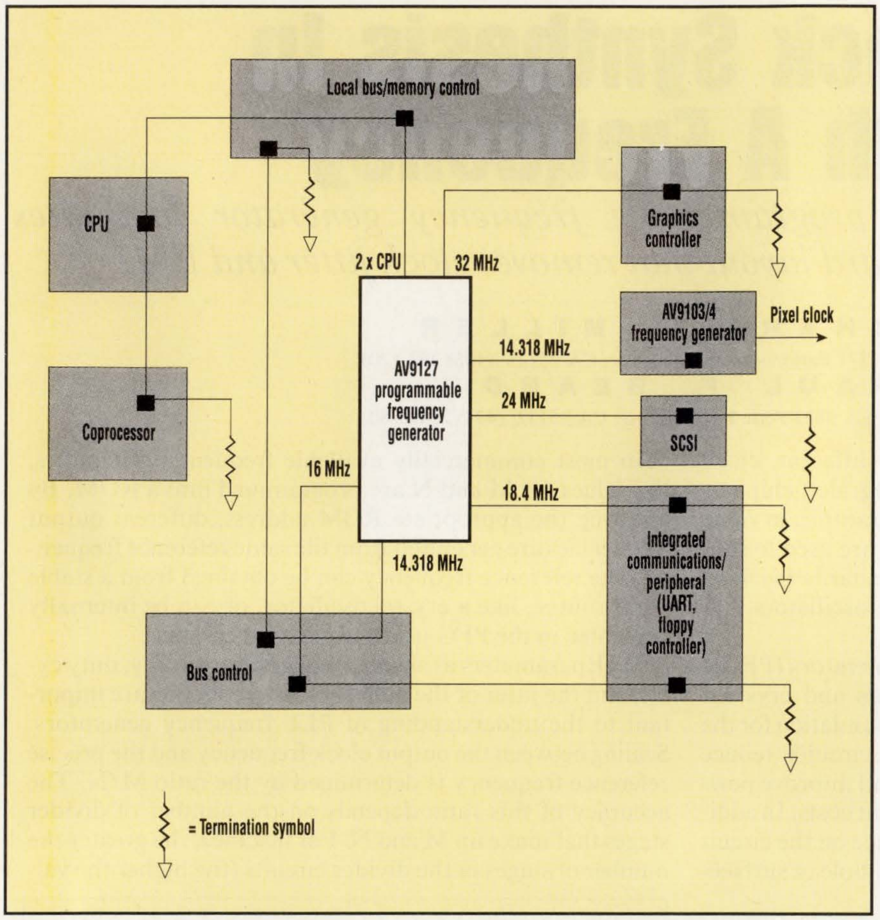
$$f_{out} = (M \div N) \times f_R$$

In most commercially available frequency generators, the values for M and N are programmed into a ROM. By selecting the appropriate ROM address, different output frequencies are generated from the same reference frequency. The reference frequency can be obtained from a stable clock source, like a crystal oscillator, or can be internally generated in the PFG using an external crystal.

Such parameters as absolute accuracy, stability, duty cycle, and the jitter of the output clock frequency are important to the understanding of PLL frequency generators. Scaling between the output clock frequency and the precise reference frequency is determined by the ratio M/N. The accuracy of this ratio depends on the number of divider stages that make up M and N. For instance, the greater the number of stages in the divider circuits (the higher the val-



1. Power-supply noise is reduced in video-graphic circuits using two techniques. When the supply is very noisy, a 5-V regulator consisting of a resistor, Zener diode, and filter capacitors ensures maximum isolation of the PFG from noise generated on the laptop supplies (a). The second technique uses an inexpensive circuit that functions as a peak detector and filter to reduce noise spikes on the power line (b).



2. This notebook computer uses a custom version of the AV9127 programmable frequency generator to produce all of the CPU and peripheral clocks. It also provides the 14.318-MHz clock to drive an additional VGA frequency generator.

ues of M and N), the closer the output frequency will be to the ideal frequency. However, a large number of divider stages increases the die area and therefore the cost of the PFG. In the laptop environment, accuracies of ±0.5% in the output frequency for CPU and peripheral clocks should be sufficient, while an absolute accuracy of ±1% is acceptable for most graphics applications. Accuracy should not be confused with the output frequency stability. While no difficulties result from the actual frequency differing slightly from the ideal, the actual frequency must not change during operation.

Stability of the output clock frequency over temperature and power-supply operating ranges guarantees no violations of the input clock specifications for the CPU and peripheral chips. PFGs have very stable outputs due to their feedback mechanism. Any slow variations in output frequency generate an error signal to force the output clock frequency back towards the desired value. A typical tolerance for frequency drift in a PFG over a commercial temperature and power-supply range is ±20 ppm. This compares favorably with typical tolerances of ±50 ppm for commercially available oscillators.

Another important parameter for a clock generator is the duty cycle of the output. An asymmetric output waveform may violate the minimum high or low time of a CPU or peripheral device. Most PFGs have a typical duty cycle of 48%/52%, with rise and fall times that work with all popular CPUs.

Clock jitter is the undesirable variation in frequency of a digital frequency reference due to noise processes in the clock generation and amplification circuitry. Many sources of noise can affect stable-clock generation: variations in temperature and humidity, physical vibration, ground bounce, power-supply noise, slow transitions, reflections, electromagnetic coupling, and 1/f, which is thermal and shot noise in semiconductors. Environmental factors are low in frequency and not considered sources of jitter. Susceptibility to physical vibration is a concern with crystals, but typically not with semiconductors. Semiconductor noise provides a theoretical limit to maximum performance and suggests minimizing the number of gates in the clock path.

The largest controllable source of clock jitter is noise on the power supply. PFG circuits don't have ideal power-supply rejection characteristics. Variations in the ground or supply voltage can directly affect the threshold voltage of an internal gate, thereby inducing an instantaneous phase shift. Design and layout techniques help to reduce power-supply noise.

Several methods are acceptable for measuring jitter. Time-interval analysis is well-suited for PFGs used for CPU- and peripheral-clock generation. The analysis measures the difference in the periods of subsequent clock cycles. A large number of samples (> 10,000) are taken to create a statistical distribution. This technique accurately measures the instantaneous clock jitter.

PFGs are good for laptop designs because of their cost, size, and power savings. The most appropriate types for laptops can be divided into two categories: PFGs for CPU- and peripheral-clock generators, and PFGs that supply the clocks compatible with video-graphics standards. The PFGs for CPU- and peripheral-clock generation are characterized by multiple PLL systems integrated onto one chip. Each PLL uses a common reference frequency (typically 14.318 MHz) to generate a clock for a specific function, such as CPU master clock or the 1.843-MHz clock required by many communication devices. An example of a multiple-PLL chip is the Avasem AV9127 programmable frequency generator. This chip consists of four clock generators, some with multiple outputs, that produce clock frequencies for the system clock (14.318 MHz), CPU and 2-×-CPU clocks, a communication/timer clock, bus clocks, and a floppy-disk-controller clock. The mask-programming feature of PFGs allows the device to be customized to meet the specific clock-frequency requirements of most systems.

One key advantage to the PFG is power consumption. The typical power-supply current for an AV9127 with 11 output clocks is 45 mA. Oscillators and discrete components providing equivalent performance would require over 60 mA of current. The current consumption of the AV9127 can be further reduced by powering down the PLL block of a clock function that's not in use. Power-management chips, such as Appian P94 and Vadem 82C347, facilitate this technique. The supply-current breakdown for a custom version of an AV9127 with six clock outputs shows the possible supply-current savings obtained by turning off unused clocks *(see the table)*. When just the CPU clock is running (communication, floppy-disk, and bus clocks are powered down), the chip current is reduced to 21 mA. Of this total, approximately 14 mA is used by the CPU-clock generator, and 7 mA by the reference clock. The reference clock must be kept running to operate any of the other clocks.

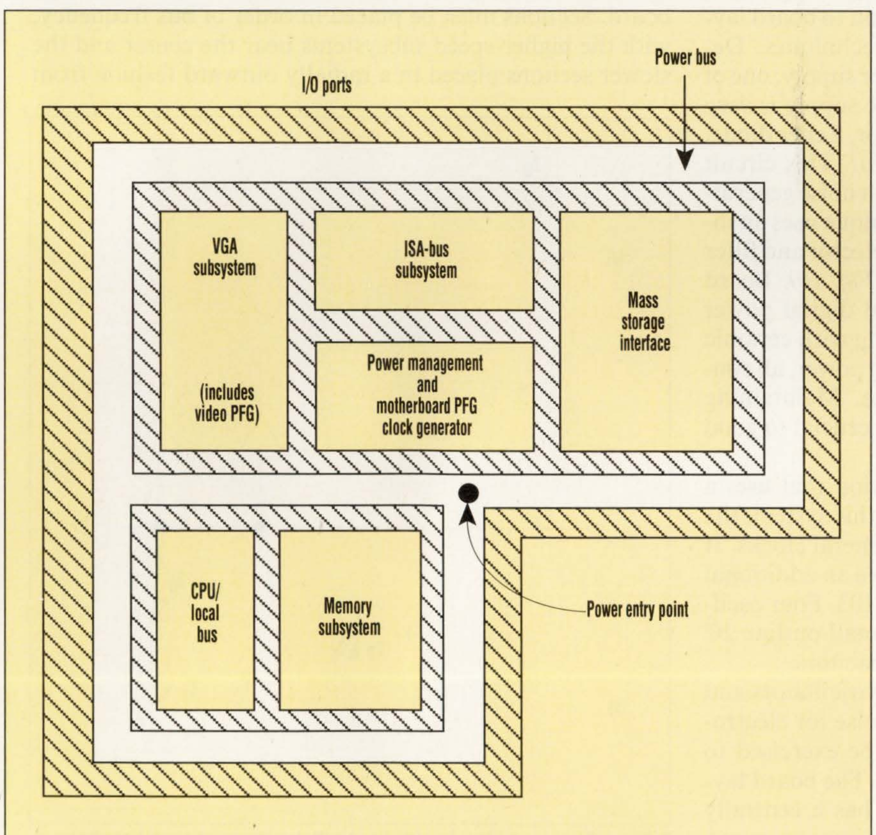
TYPICAL POWER BREAKDOWN OF AV9127-04 FREQUENCY GENERATOR

Circuit portion	Frequency (MHz)	mA
Reference clock	14.318	7
Communications clock	18.409	3
SCSI clock	24.00	4
Bus clock	32.00 + 16.00	6
CPU clock (40-pF load) (5-pF load)	40.09 40.09	14 7
Total current in full operation		27-34mA

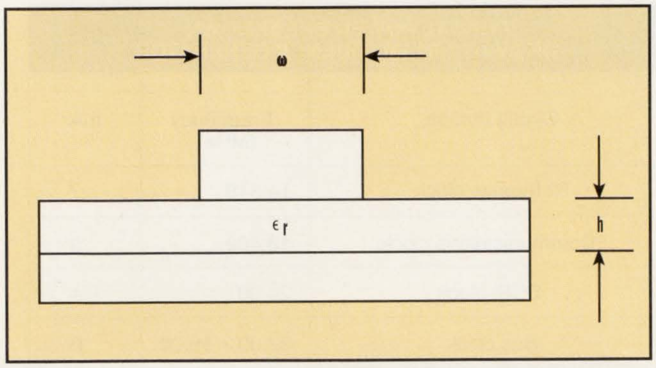
A second method for reducing a laptop's power consumption is to slow down the processor speed when the system performs a non-CPU intensive operation, such as keyboard entry by the operator. This can be accomplished easily with a PFG by switching between two ROM address locations programmed with a reduced CPU-clock frequency and the normal CPU-clock frequency. During the transition between the two frequencies, the PLL circuit generates a clock of approximately 50% duty cycle. This characteristic avoids any glitches that could be caused by narrow pulses generated when multiplexing between two oscillators. The PLL's change of frequency is determined by the loop-filter configuration.

PFGs intended for graphics applications consist of devices with one PLL block for synthesizing the pixel clock or a dual device with two PLL blocks. The second clock of the dual device drives the memory clock input of a video controller, such as the Cirrus Logic 610. One PFG can replace many oscillators by programming the internal ROM with the coefficients corresponding to the various video standard pixel frequencies.

A critical performance parameter for PFGs in video applications is jitter. Because the pixel clock drives the display, instantaneous variations in the frequency can be observed on the graphics monitor as line-to-line displacements of images. Jitter in the graphics application is particularly troublesome because of the time delay between pixels in a given column. Cumulative jitter can cause large im-



3. In the typical layout of a notebook-computer motherboard, each functional block must be grouped and powered by a separate power plane. Power-plane grouping minimizes the cross radiation of noise sources and helps to isolate external-interface drivers from any internal noise source.



4. A cross-section of the pc board and clock trace shows that the resulting transmission line has a characteristic impedance determined by the geometry of the trace and the thickness and permittivity of the insulating board material.

age displacements even when the jitter of each pixel sample is small. In addition, due to internal crosstalk, clock jitter increases with the number of PLLs on one chip. It's not good practice to use a device with greater than two separate PLL blocks to generate the pixel (or video) clock.

The major source of clock jitter in a laptop video application is noise on the power supply. The key to optimum performance in the laptop is careful attention to board layout and good power-supply decoupling techniques. Depending on the severity of noise on the power supply, one of two techniques is recommended. When the supply is very noisy, a 5-V regulator consisting of a resistor, Zener diode, and filter capacitors is appropriate *(Fig. 1a)*. This circuit ensures maximum isolation of the PFG from noise generated on the laptop supplies. The second technique uses an inexpensive circuit that functions as a peak detector and filter to reduce noise spikes on the power line *(Fig. 1b)*. Board layout issues, such as separate analog and digital power planes, sufficient low-impedance decoupling with ceramic capacitors, and inductive isolation of analog power, all contribute to controlling power-supply noise. Maintaining short return paths and small loops are also crucial to good pc-board design.

Consider a notebook-computer application that uses a custom version of the AV9127 *(Fig. 2)*. In this system, the AV9127 produces all of the CPU and peripheral clocks. It also provides the 14.318-MHz clock to drive an additional VGA frequency generator, such as an AV9103. Four oscillators were replaced by a single 28-pin small-outline IC (SOIC) package and some resistors and capacitors.

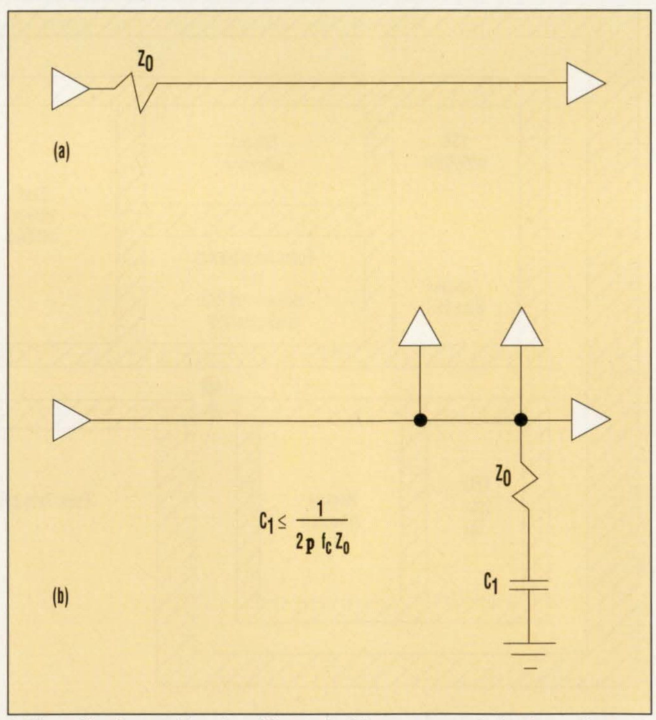
Systems with distributed high-frequency oscillators and crystals present problems in minimizing noise for electromagnetic interference (EMI). Care must be exercised to ensure that radiated signals are controlled. The board layout of a laptop that incorporates a PFG has a centrally located high-frequency clock source, so the engineer can design the board's topology to minimize the overall effects of EMI.

When the designer places the various subsystems on the computer board, each functional block must be grouped and powered by a separate power plane *(Fig. 3)*. This method of power-plane grouping minimizes the cross radiation of noise sources and helps to isolate external-interface drivers from any internal noise source.

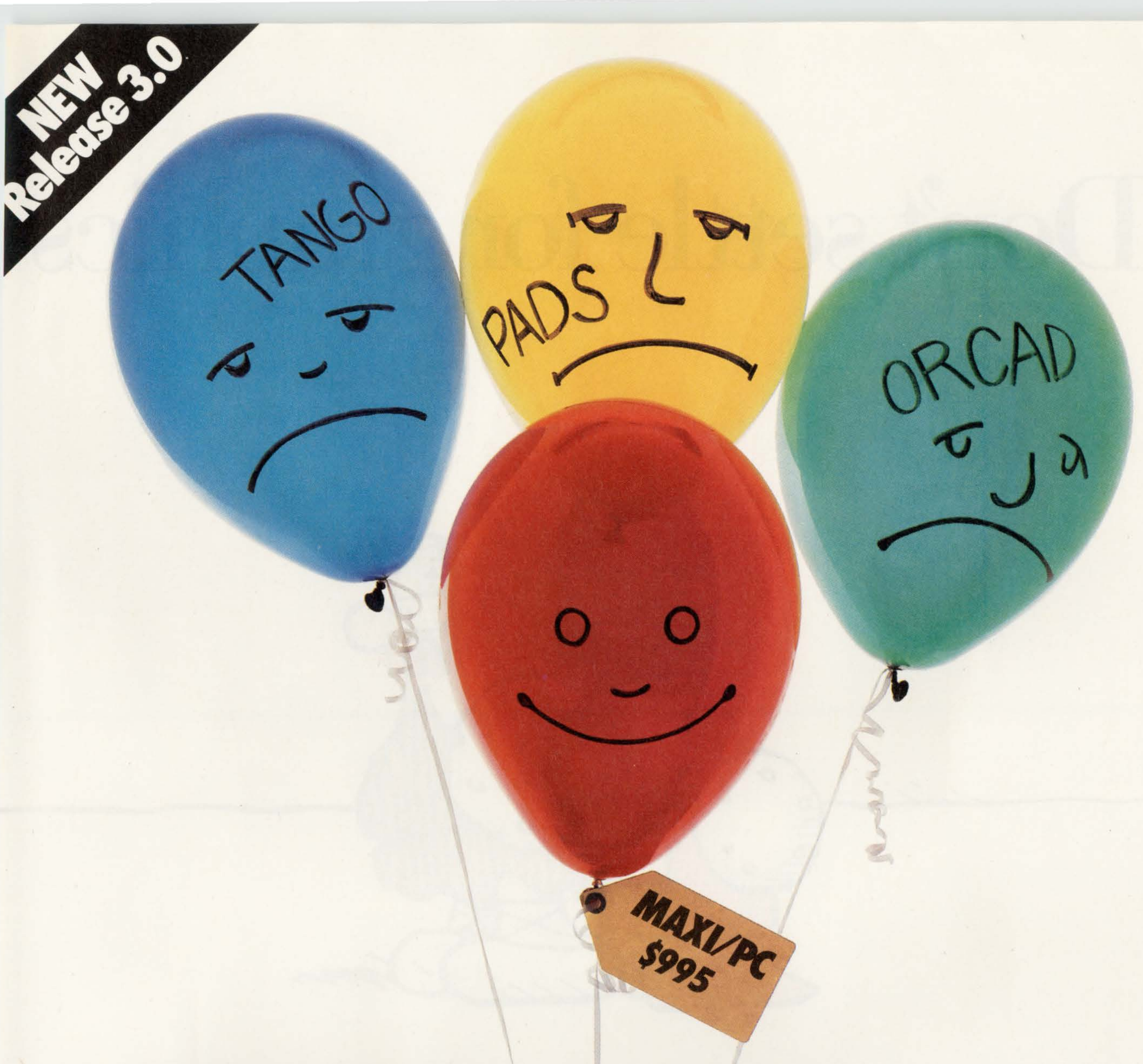
The notebook motherboard segments fit nicely into six power planes: local bus devices, ISA bus interface, CPU and power management, mass storage interface, memory subsystem, and VGA subsystem. The motivation behind these device-group allocations is to partition the system so that synchronous subsystems are segmented and signals with like periodic characteristics share the same power plane. Consequently, the noise-producing devices and subsystems are isolated from each other. When devices share a common clock, such as those on the local bus, they should also share the same power plane.

Another point to consider is that this notebook computer's power-plane grouping can relate to the power-management scheme employed. For instance, devices grouped on common, switched-power sharing planes can coincide with the segmented V_{CC} assignments.

The AV9127 frequency generator should be centrally located and in close proximity to the chips that require the highest clock frequency (for example, CPU or coprocessor). This approach minimizes the length of the high-frequency radiating traces and resistance of the supply traces. The power entry point must be near the center of the pc board. Sections must be placed in order of bus frequency, with the higher-speed subsystems near the center and the slower sections placed in a radially outward fashion from



5. The reflection problem is addressed with two types of circuit configurations. Series termination is effective for a single receiver at the end of the line (a). Multiple receivers should be grouped together near the end of the line and shunt-terminated to minimize both clock skew and reflections (b).



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the center of the board.

When this is ignored, all of the digital noise from the high-speed circuits will interfere on the circuit between the high-speed sections and the power entry point.

The AV9103 Laptop VGA Frequency Generator should be located in the VGA subsystem section. By placing this chip close to the VGA controller, the high-frequency clock traces can be short. If a memory clock is required by the VGA controller, it should be generated in the AV9127 device to minimize crosstalk between the memory clock and the pixel clocks generated in the AV9103.

Board layout techniques help minimize clock jitter and EMI. These techniques, such as proper termination and shielding, are important skills that should be mastered by any computer board design.

As mentioned, clock jitter can be introduced into a PFG by noise on the power supplies. From this standpoint, an optimum pc-board design that minimizes power-supply and ground noise includes separate analog and digital ground planes, low-impedance ground returns, and decoupling at each IC power-supply input. If this isn't possible, care must be exercised in designing the ground return path for the clock generator to reduce impedance and return current.

Coupling of digital signals into sensitive analog circuits contributes to the clock jitter. The loop-filter pins are high-impedance inputs to the VCO circuits, and are susceptible to induced coupling. Lines to these pins must be as short as possible and shielded from high-frequency digital lines by an analog ground or analog V_{CC} plane. The analog ground plane should be connected to the system ground at one point to reduce ground loops.

Slow transitions, reflections, and electromagnetic coupling fall in the domain of clock distribution. The slowest edge is at the crystal input to the reference oscillator. This high-impedance input determines the jitter performance for the clock system. The lines from the crystal to the IC should be as short as possible and shielded from high-frequency digital and analog lines.

Clock reflections are a problem when interfacing a PFG to another circuit because they can cause false triggering and jitter at the receiving gate. Reflections arise from traces on multilayer boards with ground planes that can be modeled as transmission lines. The transmission lines have a characteristic impedance determined by the geometry of the trace and the thickness and permittivity of the insulating board material *(Fig. 4)*. The characteristic impedance, Z, of a trace is given by the following equation:

$$Z = (377 \times h) \div (\epsilon_r \times \omega)$$

where:

h = the thickness of the glass/epoxy material
ω = the trace width
ϵ_r = 4 (5.8) for FR-4 glass/epoxy material

Any change in impedance along the transmission line results in a reflection, the amplitude of which is determined by the deviation from the characteristic impedance. Fast CMOS logic is particularly susceptible to reflections because of its high-speed transitions.

Reflection can be alleviated by controlling the impedance along the trace and keeping the trace short. The ideal case would be a single constant-width trace, over a ground plane, and with no vias, that ends at one receiving gate. The trace would be driven by the Thevenin equivalent of the characteristic impedance (series termination), and received with the characteristic impedance to ground (shunt termination). Signal amplitude would be reduced by a factor of two, but no reflections would exist at either end of the line.

Practical limitations demand deviation from the ideal case. Typical characteristic impedances fall in the range of 50 to 150 Ω. More than one receiver may be distributed along the line, which disturbs the controlled impedance and introduces clock skew because of propagation delay down the line.

Controlled rise and fall times lessen the reflection problem by limiting the high-frequency content of the clock. This also helps the radiation problem for FCC and VDE certification. The multiple output drivers for the CPU (or 2-×-CPU) clock on the AV9127 allow for flexibility in designing the clock-distribution scheme.

Series termination is effective for a single receiver at the end of the line *(Fig. 5a)*. Multiple receivers in the middle of the line, however, are subject to flat spots in the rising and falling edges due to reflections from the receiving end of the line. If the flat spots occur in the threshold region of the receiver, a large quantity of jitter can be introduced. Multiple receivers should be grouped together near the end of the line and shunt-terminated to minimize clock skew and reflections *(Fig. 5b)*.

International EMI standards are concerned with conducted emissions below 30 MHz and radiated emissions above 30 MHz. Conducted emissions refer to energy transmitted on the power cord from the equipment under test (EUT). Radiated emissions refer to energy emanating from the EUT that's received by a separate antenna. In the U.S., the Federal Communications Commission (FCC) is the governing organization.

EMI is controlled by many of the same techniques described in minimizing clock jitter. Close decoupling with ceramic capacitors, the use of ground and power planes, and isolated planes for analog or high-frequency circuitry all contribute to decreasing emissions. In addition, input power-supply filtering in the form of ferrite beads and ceramic capacitors can contain noise generated by digital-logic and clock circuitry.

Radiated emissions are primarily due to fast edges on high-frequency clock and data lines. Special care must be given to clock distribution and termination.

Series termination can slow edge speed to reduce radiated emissions, but clock jitter and propagation delay may be impacted when the slow edge increases the noise at a gate threshold. Using a ground plane significantly improves radiated emissions.

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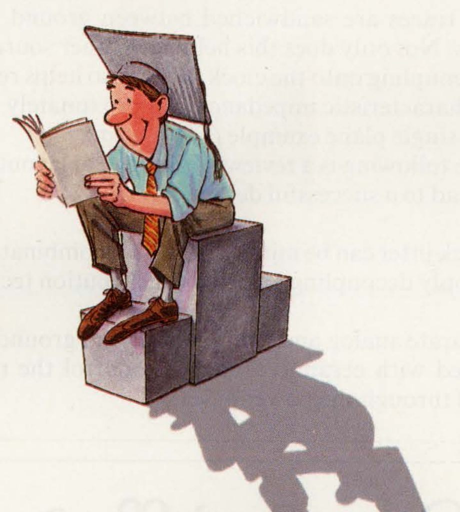

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CIRCLE 151 FOR RESPONSE OUTSIDE THE U.S.

Efficient antennas are associated with conductor lengths equal to one-quarter of the wavelength of the frequency of interest. For example, the quarter wavelength in free space at 200 MHz is 14.5 in. ($l = c/f$, where l is the wavelength in m, c is the speed of light in m/s, and f is the frequency in cycles/s or Hz). Most clock lines on a board will be much shorter and the corresponding frequencies of efficient radiation much higher.

In summary, an ideal system for minimizing clock jitter and EMI uses a multilayer board, where all high-speed clock traces are sandwiched between ground and power planes. Not only does this help keep other sources of noise from coupling onto the clock, but it also helps reduce EMI. The characteristic impedance is approximately half of that in the single plane example *(Fig. 4, again)*.

The following is a review of the critical layout issues that will lead to a successful design:

- Clock jitter can be minimized with a combination of power-supply decoupling and clock-distribution techniques.

- Separate analog and digital power and ground planes decoupled with ceramic capacitors control the noise introduced through the power buses.

- Short isolated traces to the crystal and loop filters minimize radiated noise coupling at the most sensitive points in the circuit.

- Short clock-distribution lines minimize skew and the effect of reflections due to imperfect termination.

- A line with multiple receivers should be shunt-terminated at the end of the line with its characteristic impedance.

Richard S. Miller, vice president of analog product for Avasem Corp., received a BSEE from Renssalear Polytechnic Institute, Troy, N.Y., and a MSEE and PhD in electrophysics from the University of Southern Calif., Los Angeles.

Paul F. Beard, who leads a team of engineering consultants as the CEO of Technical Success, San Jose, Calif., holds a BSEE from the University of Manchester, England.

HOW VALUABLE?

HIGHLY	CIRCLE 551
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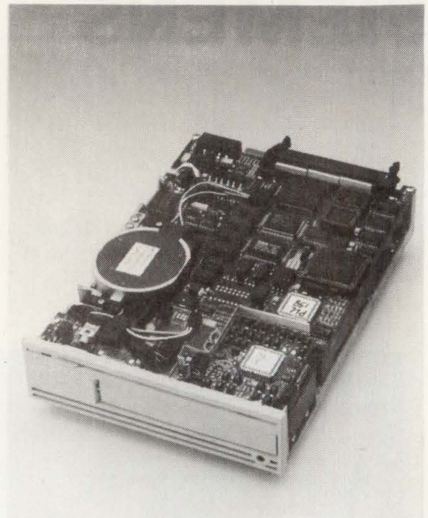
▼ 1/4-IN. TAPE DRIVE BACKS UP 1.35 GBYTES

Archive Technology Inc. claims that their latest 1/4-in. cartridge tape drive is the first to achieve 1.35 Gbytes of storage with a data throughput rate of 36 Mbytes/min. The Viper 2750 offers data integrity that exceeds less than one unrecoverable error for every 10^{15} bits. This level is achieved by using the QIC-1350 Development Standard, which specifies a frame format that supplies level-6 Reed-Solomon error-correcting code.

The drive is suitable for network file servers, graphics workstations, and minicomputer backup. It's backward compatible with most of the 1/4-in. drives in the field. It can read



and write tapes in the QIC-1350, QIC-1000, QIC-525, QIC-150, and QIC-120 formats. It also has the capability to read tapes written in the QIC-24 format. The Viper 2750 supports the tape command set of SCSI-I or SCSI-II, operating in synchronous mode at 5 Mbytes/s or in asynchronous mode at 2 Mbytes/s. The drive is available now. In large quantities, it is priced at $700.

Archive Technology Inc.
1650 Sunflower Ave.
Costa Mesa, CA 92626
(714) 641-1230.
▶ **CIRCLE 577**

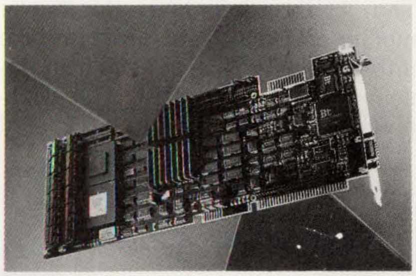
▼ VGA GRAPHICS CONTROLLER FITS IN ONE CHIP

Moving one step up the performance ladder for graphics controllers is the CL-GD5410 from Cirrus Logic Inc. The single-chip controller is 100% hardware and BIOS compatible with the IBM VGA display standard. It requires no external support other than the display memory and a frequency reference. A motherboard VGA implementation supporting 1 Mbyte can be achieved using two DRAMs. And the GD5410 connects directly to an ISA, EISA, or MCA bus.

Operating at dot clock rates up to 65 MHz, the CL-GHD5410 supports resolutions to 1024 by 768 at up to 8 bits/pixel. The internal RAMDAC can be configured as a standard part to supply a palette of 262,144 colors. The chip sells for $25 and will sample in October with production starting next February.

Cirrus Logic Inc.
3100 West Warren Ave.
Fremont, CA 94538
(415) 623-8300.
▶ **CIRCLE 578**

▼ GET WORKSTATION-LIKE GRAPHICS FROM A PC



By adding the XHR Gemini20 graphics card, users can get workstation-level performance from their PCs. Intended for IBM PC/XT/AT and PS/2 systems and compatibles, the card is designed around a TI TMS34020 graphics processor. In addition, the card contains a TMS34082 math coprocessor. This part is a graphics floating-point unit that exponentially improves graphics throughput. The resulting combination of 8 MIPS makes the board suitable for even the most complex graphics applications, such as shading or 3D display lists. Throughput is further increased by the on-board high-speed cache memory. The board, available now, starts at $2895.

Elsa America Inc.
400 Oyster Point Blvd. #109
South San Francisco, CA 91080
(415) 588-6285.
▶ **CIRCLE 579**

▼ TRACKBALL MAKES INPUT EASIER, FASTER

Arm and wrist movements are eliminated using the Mouse-trak trackball. Available with two or three buttons on a host of different platforms, the Mouse-trak makes input faster and easier. A soft wrist pad cushions the hand, and the 2-in. polished phenolic ball rests on hardened stainless steel shafts and precision bearings for precise control. Users can program the buttons, so it's just as easy with either hand. A speed-control button allows for adjustable cursor speed. The trackball comes with the interface cable and sells for $159 to $199. An industrial version is available for harsh environments. The M5-IND model sells for $295.

ITAC Systems Inc.
3121 Benton
Garland, TX 75042
(800) 533-4822 or (214) 494-3073.
▶ **CIRCLE 580**

▼ 9600-BAUD MODEM WORKS WORKS WITH A MAC

The Practical Smart Pack 9600 is a 9600 bps modem designed for the Apple Macintosh. The peripheral is a full-duplex CCITT V.32, V.42, V.42bis standalone device. Its error-correction technology offers added flexibility. The modem includes Hayes' Smartcom II for the Mac plus a hardware flow-control cable. The package contains front-panel controls and status lamps. The Practical Smart Pack 9600 sells for $759 and is available now.

Practical Peripherals Inc.
31245 La Baya Dr.
West Lake Village, CA 91362
(818) 706-0333.
▶ **CIRCLE 581**

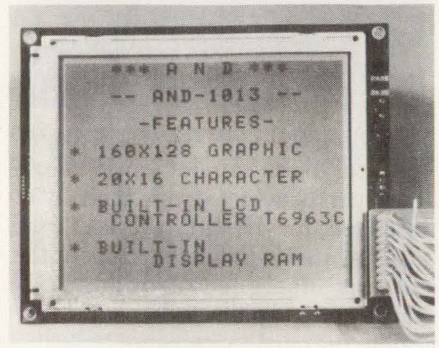
▼ 3.5-IN. DDS DRIVE STORES 2 GBYTES

Up to 2 Gbytes of uncompressed data can be stored on one 4-mm DDS tape using the SDT-2000 tape drive. Built to a standard 3.5-in. format, the drive maximizes reliability by having all of its electronics on one pc board. An embedded SCSI II interface allows an asynchronous burst transfer rate of 3 Mbytes/s and a synchronous burst rate of 5 Mbytes/s. The drive contains flash memory so the drive can be upgraded easily.

Sony Corp.
Magnet Storage Products Div.
655 River Oaks Pkwy.
San Jose, CA 95134
(408) 944-4223.
▶ **CIRCLE 582**

▼ LCD SHOWS GRAPHICS AND TEXT SIMULTANEOUSLY

The AND1013ST LCD dot-matrix module allows both text and graphic information to be displayed simultaneously. The supertwist 160-by-128-pixel module contains an integrated



controller, display RAM, character-generator ROM, and display drivers. This internal circuitry can link directly to a microprocessor. Individual pixel control allows for user-definable characters up to 256 symbols. The module's viewing area is 101 by 82 mm. In quantities of 100, the display costs $100.

AND Corp.
770 Airport Blvd.
Burlingame, CA 94010
(415) 347-9916
▶ **CIRCLE 583**

▼ EISA MOTHERBOARDS RUN AT 25, 33, OR 50 MHZ

Two new EISA motherboards, one baby-sized and the other full-sized, meet every EISA design requirement and operate at 25, 33, or 50 MHz. The AIR486ES and the AIR486EL each contain a socket to hold a Weitek 4167 math coprocessor as well as 8 kbytes of internal cache memory. The full-sized board can carry 64 or 256 kbytes of external cache, while the baby-sized board has room for 128 kbytes. The smaller board has six 32-bit EISA slots and two 16-bit slots, while its larger cousin has eight 32-bit EISA slots. The baby-sized board costs from $1600 to $2500 and its counterpart sells for $1900 to $2800.

Advanced Integration Research Inc.
657 N. Pastoria Ave.
Sunnyvale, CA 94086
(408) 737-8200.
▶ **CIRCLE 584**

▼ RACK-MOUNT INDUSTRIAL PC COSTS UNDER $4000

For under $4000, users can get a ruggedized, rack-mountable microcomputer platform for industrial environments that's easy to service. Any component in the system can be replaced in less than eight minutes. The Model 302i is a full-featured 25-MHz Intel 386-based computer that can operate at higher temperatures, with dirtier air, and added vibration. The platform can run either real-time or traditional PC applications. The unit's hard disk is shock-mounted for vibration protection and covered to keep dust out. Add-in cards are held in place by a locking bar. The system comes with 64 kbytes of cache memory, 8 expansion slots, and up to 40 Mbytes of zero-wait-state memory. Configured with 4 Mbytes of DRAM; a 52-Mbyte hard disk; and a 3.5-in., 1.44-Mbyte floppy drive; the 302i sells for $3995 and is available now.

Intel Corp.
P.O. Box 7641
Mt. Prospect, IL 60056
(800) 548-4725.
▶ **CIRCLE 585**

▼ TAKE PEN-BASED PC ON THE ROAD

Computer users can take their systems wherever they go when using the System 3125, a pen-based notepad PC. The 3125 has all of the functionality of a typical PC, yet users can print directly on the digitized screen with a cordless pen. The computer contains built-in handwriting recognition to turn the input into data. Weighing 3.9 lbs., it can replace keyboard-based systems, paper pads, and order forms. Microsoft's Windows for Pen Computing and GO Corp.'s PenPoint are supported as well as MS-DOS. The system is built with Intel's 20-MHz 386SL microprocessor. Up to 16 kbytes of cache memory are supported as well as 20 Mbytes of RAM (4 Mbytes come standard). Nonvolatile flash memory is also available as an option. The base configuration is priced at $4765 and is available now.

NCR Corp.
Workstation Products Div.
Dayton, OH 45479.
▶ **CIRCLE 586**

▼ CUSTOMIZE KEYBOARD CONTROLLER BIOS

Firmware for Intel's 8242 keyboard controller is now available from Award Software Inc. The 8242 operates from ROM BIOS. The firmware features a modular design architecture that makes it possible to support almost any custom OEM keyboard configuration. Two versions of the 8242 keyboard controller are available from Intel. The 8242WA is a PC/AT-compatible device, while the 8242WB supports an IBM PS/2 platform.

Award Software Inc.
130 Knowles Dr.
Los Gatos, CA 95030
(408) 370-7979.
▶ **CIRCLE 587**

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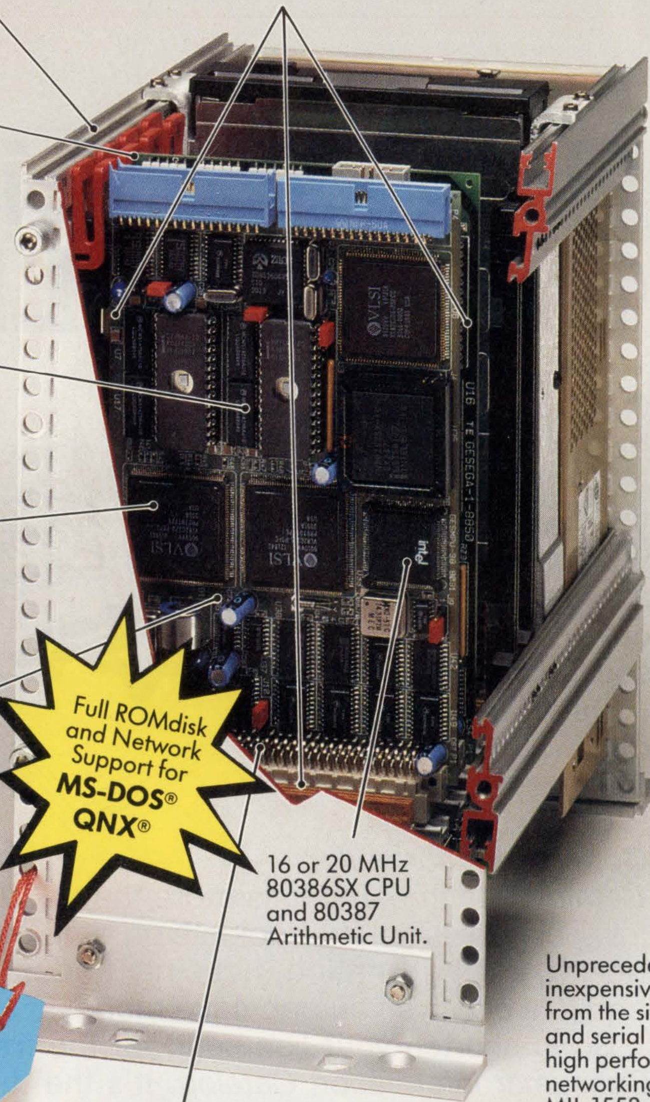

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CIRCLE 130 FOR U.S. RESPONSE

CIRCLE 131 FOR RESPONSE OUTSIDE THE U.S.

Military And Multibus II Technology Storm Into Buscon

Aided by a Washington, D.C. location, the conference promotes military and Multibus II to top guns.

BY RICHARD NASS

With military applications invading all areas of the electronics industry, it's only natural that Washington D.C. hold this year's Buscon/91 East. The technical conference has sessions devoted to most of the popular buses, including Futurebus+, SBus, VMEbus, and Multibus II. In addition, an entire day is being devoted to military applications. Bob Marshall, military marketing manager for Signetics Co., Sunnyvale, Calif., says, "Although people aren't looking for military parts for non-military applications, it's starting to go the other way. Some of the commercial components are going into military equipment to save money." This particular issue among others will be discussed in the technical sessions.

The military won't be the only hot topic, though. Multibus II should garner its share of the attention. Some of the technology discussed by the technical committees at Buscon/91-West this past January has taken root, and several of the ensuing products should start to emerge.

Two major issues concerning Multibus II materialized from those committee meetings. First, there's now a live-insertion capability that enables all existing Multibus II boards to be placed into live systems. It's actually a backplane specification that's critical for areas like communications and simulation. The latest Multibus II systems will have the ability to power-down individual slots without shutting down the entire system. This feat is accomplished by adding some circuitry to the backplane. Using software and firmware protocols that already exist for Multibus II, the newly-inserted board will be powered up in the already live system.

The second issue deals with an increase in backplane speed. Parts like the message-passing coprocessor (MPC), which appear on almost every Multibus II board, continue to shrink in physical size. This fact, coupled with the many advances in backplane technology, permit the backplane speed to double from 40 to 80 Mbytes/s. This is performed by changing the backplane frequency from 10 to 20 MHz. Silicon has been sent to a limited number of board makers to evaluate the capability.

The higher speed could be used in existing boards, but two changes must be in place. First, a faster MPC chip is needed. Because most boards use socketed ICs, that shouldn't be a problem. Users can simply pull off the old chip and insert a new one. Second, the transceivers also must be replaced. Resoldering may have to be done for certain transceivers, which is usually an unacceptable solution.

The speed increase will impact existing board designs rather than existing boards. The new transceivers use the Advanced biCMOS TTL (ABT) technology that's pin-for-pin compatible with present transceivers. Thus, the board redesign would be a fairly simple one—just substitute the new transceivers and the 20-MHz MPC chip.

One Multibus II advance comes in the form of a board from Aeon Systems, Albuquerque, N.M. Its MBII 300 allows VAX software to run in a Multibus II environment. Aeon took the DEC rtVAX 300 modular chip set, coupled it with an Intel i960 microprocessor, and integrated them into a Multibus II board, which is similar to the company's VME board that's built around the same chip set. Any code compilation that's required is done on the VAX, then ported down through an Ethernet connection to the MBII 300 board. Thus, the VAX back-end is connected to the Multibus II front-end. The board becomes a communications center for the rest of the system, speeding up the whole system in the process.

On the military side, a host of presentations in the technical program are based on military issues. One such presentation, by Kim Clohessey of

Dy-4 Systems, Nepeon, Ontario, Canada, goes into detail about the militarization of VME. It discusses the marketplace, standards activity, and general design considerations. In Clohessey's dialogue on the marketplace, he states that the military market is growing at a rapid pace. More specifically, he says that the market, which presently stands at $30 million, is projected to balloon to $300 million by 1995.

A second presentation, given by David DeKing and Anthony Comito of the Armored Vehicle Technologies Associated, Troy, Mich., deals with the Standard Army Ventronics Architecture (SAVA). The paper addresses such issues as physical and electronic vehicle integration and the SAVA specifications and building blocks *(Fig. 1)*. The building blocks show all of the elements of a SAVA system, one that's suitable for military environments.

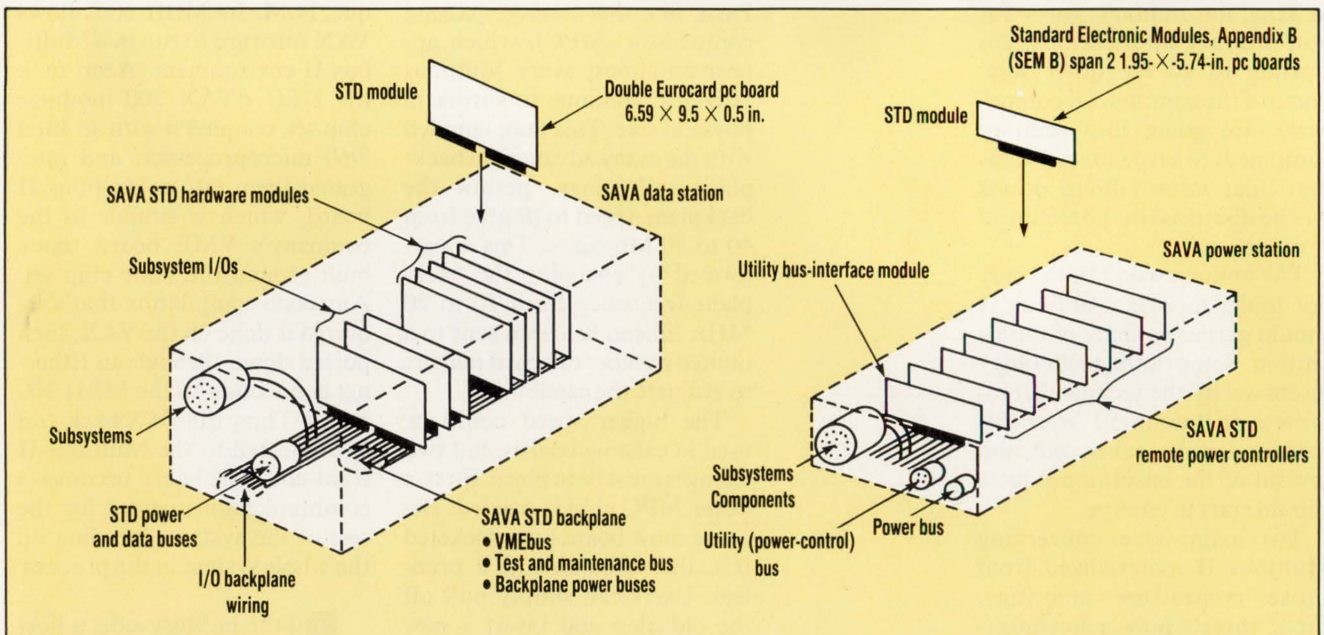
Signetics is releasing its ABT family of 8- to 10-bit bus-interface parts for military applications. ABT was originally developed for commercial use. The new parts are built on the company's proprietary QUBiC advanced biCMOS process, which is a very fast, 13-GHz bipolar, 0.8-μm CMOS process. The parts combine high speed, low power, and low noise, all essential characteristics for bus interface.

Signetics feels that the military market is concerned with noise and reliability problems due to heat. It contends that present offerings haven't addressed these problems inherent to high-current-drive CMOS parts. The ABT devices, the 54ABT543, 54ABT646, and 54ABT2952, solve both problems simultaneously. The low-power feature keeps the system relatively cool, which directly affects system reliability, while the low-noise features increase the system's reliability. In addition, the biCMOS process, when compared to bipolar CMOS, has relatively flat temperature characteristics with respect to performance features like speed, output drive, noise, and power dissipation. The flat temperature characteristics are particularly significant for military applications requiring wide temperature ranges. Bipolar transistors get stronger as temperatures rise (betas get larger with higher temperatures) and CMOS transistors get stronger as temperatures fall *(Fig. 2)*. The fastest point that a pure CMOS circuit will work at is the low-temperature range, the opposite of bipolar.

Signetics will also display its Multibyte and Futurebus+ products at Buscon. The company says five transceivers will be in production by show time. A Futurebus+ protocol controller is presently sampling and a central arbiter will sample right after Buscon.

Multibyte is similar to ABT because it's made from the same process, but each Multibyte IC contains two or four ABT parts. It has the same functionality and performance as ABT, but with a higher level of integration.

Another vendor focusing on military and aerospace parts is



1. The SAVA station architecture is constructed with a family of modular buses, allowing for quick and easy repair. The hardware modules come with built-in test features.

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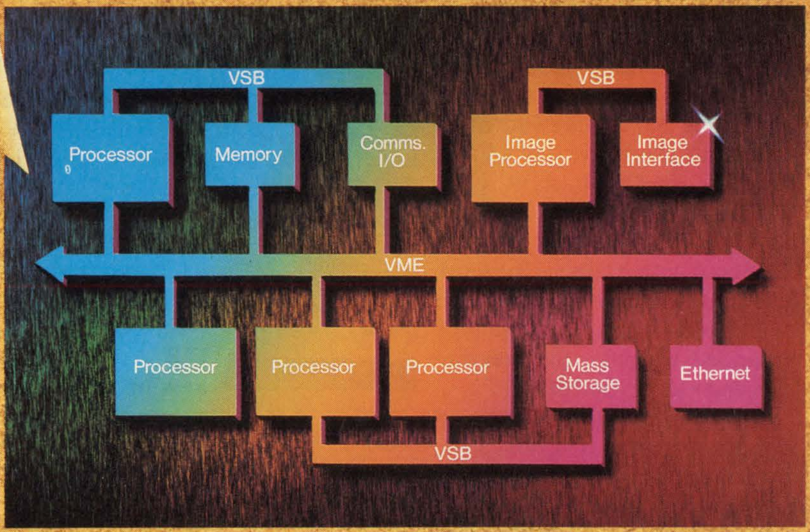

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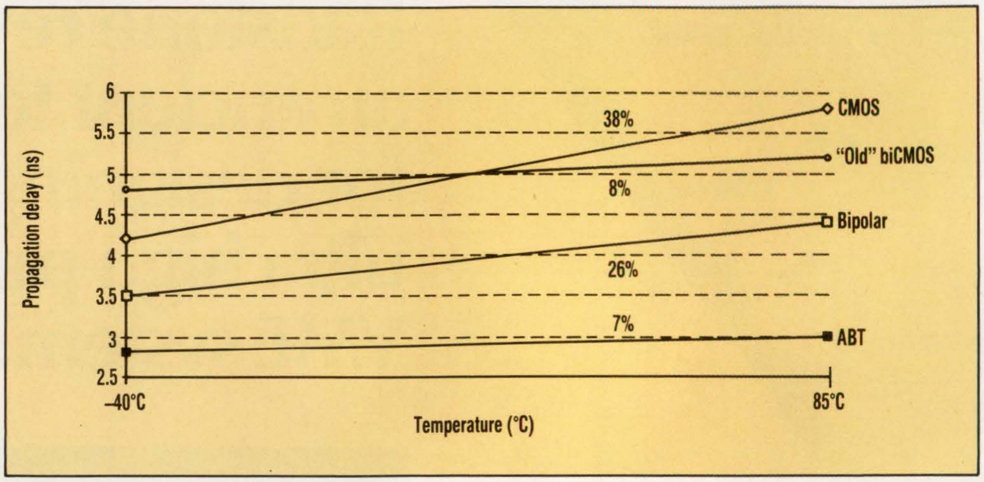
CIRCLE 266 FOR U.S. RESPONSE **CIRCLE 267 FOR RESPONSE OUTSIDE THE U.S.**

National Semiconductor Corp., Santa Clara, Calif. Aerospace parts differ from military parts in that they don't necessarily have to meet all of the military requirements, but must meet some. National's Pi-Bus line is popular in military avionics. The architecture follows a standard set by the Joint Integrated Avionics Working Group (JIAWG), one of the task forces formed to standardize military and avionics electronics.

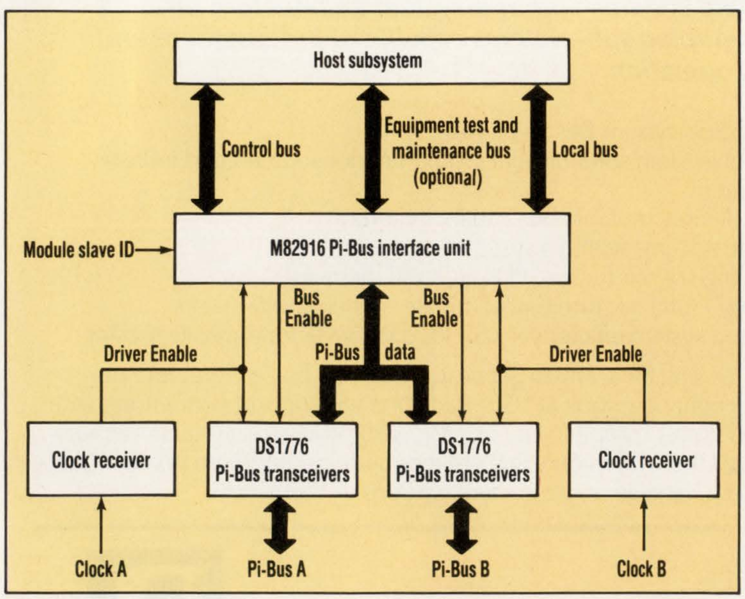
A presentation by Chuck Roark, from Texas Instruments' Defense Systems and Electronics Group, Plano, Texas, offers insight into the Pi-Bus architecture. The paper gives an overview and the history of Pi-Bus and discusses the current issues surrounding the bus. One issue involves adding 32-bit requirements. Another allows for more efficient message transfers, in which a datagram message type is added to make the message passing more efficient.

There are different ways to configure Pi-Bus. The bus can be configured as 16- or 32-bits wide, and for error correction or error detection. All of the configurations are based on the Pi-Bus controller *(Fig. 3)*. Because many different configuration schemes exist, various companies use an assortment of controllers. National chose to produce the Pi-Bus transceivers, which are common to each different scheme.



2. Advanced biCMOS TTL (ABT) has relatively flat temperature characteristics with respect to propagation delay, compared to other technologies. This is a particularly significant characteristic for military applications that require wide temperature ranges.

JIAWG, supported by the U.S. Army and Air Force, was looking to work with tangible products. Because Futurebus still hasn't delivered any complete products, Pi-Bus was chosen. On the other hand, Next-Generation Computer Resource (NGCR), the standards group for the Navy, was willing to go with Futurebus+ after evaluating the many available resources. Naval documents mandate that starting in September 1992, all products must comply with the Futurebus+ specifications. Companies presently designing products are trying to ensure that an upgrade path to Futurebus+ is possible.



3. The Pi-Bus interface unit is the central point in the system. The host subsystem connects to the interface unit through the control bus; the local bus; and the equipment, test, and maintenance bus.

A bus that's gaining lots of momentum is the SBus. VMetro Inc., Houston, Texas, is working on a bus analyzer for the SBus. The instrument follows the company's existing product architecture for bus analyzers. They currently have analyzers for VME and VSB buses, and a general-purpose tool with a P2 connector that's a daughterboard module.

Basically, VMetro had to alter their core analyzer component to make it SBus-compatible. This was a difficult project because an SBus board is much smaller than a VME board. The analyzer can capture all signals and cycles from the SBus. It also has a programmable-event comparator. VMetro hopes that the analyzer will be ready for Buscon/92-West early next year.

Due to the recent surge in STD 32 (the 32-bit version of the STD bus), an interest group is being formed around the architecture. Initially known as Special Interest Group 32 (SIG 32), the group's first meeting will take place at Buscon. Among the topics to be discussed are the significant issues and applications surrounding STD 32 and STD developments as they relate to PC/AT, EISA, and VME buses.

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Circle 303 for Literature (Response Outside U.S.)

▼ C COMPILER OFFERS FLEXIBLE DEVELOPMENT

Supplying full-spectrum development, the PDOS/MRI ANSI C native compiler is based on Microtec Research's ANSI C cross compiler. Full-spectrum development means the ability to develop on a cross (host) and/or native (target) system and generate compatible code from both platforms. The compiler is tailored with PDOS cross and native interface libraries so that programmers can develop real-time applications using a standard compiler on a host and/or native system. The compiler is designed for the Motorola 68000 family of microprocessors. The native version costs $2500 and goes up to $7900 for the cross version on a Sun SparcStation.

Eyring Inc.
1455 West 820 North
Provo, UT 84601
(801) 375-2434.
▶CIRCLE 690

▼ CONNECT SBUS TO HIGH-SPEED SERIAL LINES

Sbus systems calling for an interface to high-speed serial lines running at speeds up to 2.048 Mbits/s now have an answer: The SB-302 serial communications controller from SBE Inc. The high-performance, dual-port adapter card supports X.25, LAPB, and other wide-area network protocols. The board is built with a 20-MHz 68302 microprocessor for E1 (2.048 Mbits/s) applications, with a 16-MHz option for T1 (1.544 Mbits/s) requirements.

The SB-302 comes with 256 kbytes of SRAM, 2 Mbytes of DRAM, and 512 kbytes of EPROM. Two serial ports, one channel at E1 or T1 and one at 128 kbits/s, support multiple protocols. Each port can be independently configured to meet EIA-232-D, EIA-449, EIA-530, or V.35 requirements using interface modules. The board is available with SunOS and X.25 device drivers. Shipments should start in the fourth quarter.

SBE Inc.
2400 Bisso Lane
Concord, CA 94520
(415) 680-7722.
▶CIRCLE 691

▼ SCSI-II HOST ADAPTER CONNECTS TO VME, VME64

The V/SCSI 4220 Cougar is a high-performance SCSI-II host bus adapter for VME and VME64 systems and supports a data-transfer rate of 10 Mbytes/s. The adapter intends to reduce SCSI-II command overhead. The board, which comes with a multifunction daughterboard connecter that's supported by Interphase, is based on the Motorola 68030 microprocessor. It will be available in the first quarter of next year.

Interphase Corp.
13800 Senlac
Dallas, TX 75234
(214) 919-9000.
▶CIRCLE 692

SAMPLING OF BOARD MANUFACTURERS

Companies with a ★ will be exhibiting at Buscon/91-East

Acromag Inc.
30765 Wixom Rd. PO Box 437
Wixom, MI 48393-7037
(313) 624-1541
(VME) (I/O)
CIRCLE 600

Adaptec Inc.
691 South Milpitas Blvd.
Milpitas, CA 95035
(408) 945-8600
(SCSI) (EISA) (PC/AT)
CIRCLE 601

Alacron
71 Spitbrook Rd. Suite 204
Nashua, NH 03060
(603) 891-2750
(VME) (PC/AT)
CIRCLE 602

Analogic Corp.
8 Centennial Dr.
Peabody, MA 01960
(508) 977-3030
(PC/AT) (VME)
CIRCLE 603

Andrew KMW Systems Inc.
6034 W. Courtyard Dr.
Austin, TX 78730
(512) 338-3000
(VME) (MBII) (SCSI)
CIRCLE 604

★AP Labs
6215 Ferris Sq.
San Diego, CA 92121
(619) 546-8626
(VME) (SBus)
CIRCLE 605

★Ariel Corp.
433 River Rd.
Highland Park, NJ 08904
(201) 249-2900
(DSP)
CIRCLE 606

Atlanta Signal Processors
770 Spring St.
Atlanta, GA 30308
(404) 892-7265
(PC/AT) (DSP)
CIRCLE 607

★Augment Systems Inc.
19 Crosby Dr.
Bedford, MA 01730
(617) 271-0230
(VME) (NuBus)
CIRCLE 608

★Bus-Tech Inc.
129 Middlesex Turnpike
Burlington, MA 01803
(617) 272-8200
(N) (SCSI)
CIRCLE 609

★Central Data
1602 Newton Dr.
Champaign, IL 61821
(217) 359-8010
(SBus) (SCSI) (MBI) (MBII)
CIRCLE 610

Centralp Automatismes
25 Cedar St.
Clinton, MA 01510
(508) 368-1301
(PC/AT) (MBI) (MBII)
CIRCLE 611

Ciprico Inc.
2955 Xenium La.
Plymouth, MN 55441
(612) 559-2034
(SCSI)
CIRCLE 612

★Clearpoint Research Corp.
35 Parkwood Dr.
Hopkinton, MA 01748
(617) 435-2000
(VME)
CIRCLE 613

★Communication Automation & Control
1642 Union Blvd. Suite 200
Allentown, PA 18103
(215) 776-6669
(DSP) (VME) (PC/AT) (STD)
CIRCLE 614

Computer Dynamics
107 S. Main St.
Greer, SC 29650
(803) 877-8700
(STD) (PC/AT)
CIRCLE 615

★Concurrent Technologies
701 Devonshire Dr.
Champaign, IL 61820
(217) 356-7004
(MBI) (MBII)
CIRCLE 616

Coreco Inc.
6969 Trans-Canada Hwy., Suite 113
St. Laurent, Quebec H4T 1V8
(514) 333-1301
(PC/AT) (G)
CIRCLE 617

★CSPI Inc.
40 Linnell Cir.
Billerica, MA 01821
(617) 272-5020
(VME) (PC/AT) (EISA)
CIRCLE 618

Cubit Div.,
Proteus Industries
340 Pioneer Way
Mountain View, CA 94041
(415) 962-8237
(STD)
CIRCLE 619

Cyclone Microsystems
25 Science Park
New Haven, CT 06511
(203) 786-5536
(VME) (N)
CIRCLE 620

Data Translation Inc.
100 Locke Dr.
Marlboro, MA 01752
(508) 481-3700
(DSP)
CIRCLE 621

Datel Inc.
11 Cabot Blvd.
Mansfield, MA 02048
(508) 339-3000
(PC/AT) (I/O)
CIRCLE 622

★Digital Equipment Corp.
Continential Blvd.,
M/S MK02-2/F10
Merrimack, NH 03054
(603) 884-5384
(VME) (SCSI) (T)
CIRCLE 623

Diversified Technology
117 East State St.
Ridgeland, MS 39158
(800) 443-2667
(PC/AT)
CIRCLE 624

DY 4 Systems Inc.
21 Fitzgerald Rd.
Nepean, Ontario K2H 9J4
(613) 596-9911
(VME)
CIRCLE 625

Dynatem/Oettle and Reichler
15795 Rockfield Ave., Suite G
Irvine, CA 92718
(714) 855-3235
(VME)
CIRCLE 626

Force Computers Inc.
3165 Winchester Blvd.
Campbell, CA 95008-6557
(408) 370-6300
(VME)
CIRCLE 627

★Formation Inc.
121 Whittendale Dr.
Moorestown, NJ 08057
(609)234-5020
(VME) (N)
CIRCLE 628

★General Micro Systems Inc.
4740 Brooks St.
Montclair, CA 91763
(714) 625-5475
(VME)
CIRCLE 629

(continued on p. 134)

NOTES

(MBI)	Multibus I
(MBII)	Mulitbus II
(N)	Network
(G)	Graphics
(T)	Turbo Channel
(FB+)	Futurebus+

▼ CONVERT EISA SYSTEM TO FILE SERVER

Converting EISA computers into high-performance file servers, multiperipheral workstations, or multiuser networks is now made easier with the EISA SCSI Master. The host-adapter kit comes with an EISA-to-fast SCSI host adapter (AHA-1740), software, cables, and documentation. System performance is maximized by transferring 32-bit data to and from memory at 33 Mbytes/s, independent of the system processor. Up to seven SCSI devices are supported, including disk, tape, CD-ROM, WORM, and DAT. The kit is available now for $695.

Adaptec Inc.
691 S. Milpitas Blvd.
Milpitas, CA 95035
(408) 945-8600.
▶ **CIRCLE 693**

▼ COMMUNICATIONS, STORAGE MODULES ADD PUNCH

Two new products, a high-speed, parallel communications expansion module and a high-performance data-storage module (DSM) are available from Matrix Corp. The DB-PCOMM communications expansion board exceeds 30 Mbytes/s in a 32-bit data transfer, independent of the host CPU. It's appropriate for any applications where full 32-bit data must be downloaded quickly. The daughterboard attaches to any double-height host CPU with a Dbus 68 interface. Based on a public-domain specification, Dbus 68 is available on several Matrix CPU boards. The DB-PCOMM also attaches to the VSB extension bus. It sells for $2995 and will be available in the fourth quarter.

The DSM employs standard drives to achieve up to 100 Mbytes of formatted hard-drive capacity and 1.44 Mbytes of floppy-drive capacity. The modules takes up two slots in a VME-bus system on a 6U form-factor board. Several combinations of floppy and hard drives are available. The DSM supports single-, double-, and quad-density formats, including PC/AT. The DSM is priced at $860 and is available now.

Matrix Corp.
1203 New Hope Rd.
Raleigh, NC 27610
(919) 231-8000.
▶ **CIRCLE 694**

SAMPLING OF BOARD MANUFACTURERS

Gespac
50 West Hoover Ave.
Mesa, AZ 85210
(602) 962-5559
(I/O) (N) (G)
CIRCLE 630

Graphic Strategies Inc.
549 Weddell Dr.
Sunnyvale, CA 94089
(408) 745-6500
(VME)
CIRCLE 631

★Green Spring Computers Inc.
1204 O'Brien Dr.
Menlo Park, CA 94025
(415) 327-1200
(VME) (NuBus) (I/O)
CIRCLE 632

★Heurikon Corp.
8000 Excelsior Dr.
Madison, WI 53717
(608) 831-0900
(VME) (MBI) (MBII)
CIRCLE 633

I-Bus
9596 Chesapeake Dr.
San Diego, CA 92123
(619) 569-0646
(PC/AT)
CIRCLE 634

★ICS Pte. Ltd.
2 Alexandra Rd.
07-09 Delta House
Singapore 0315
065-278-8288
(EISA)
CIRCLE 635

★Image & Signal Processing Inc.
120 Linden Ave.
Long Beach, CA 90802
(213) 495-9533
(VME) (MBII) (PC/AT)
CIRCLE 636

★Imagraph Corp.
11 Elizabeth Dr.
Chelmsford, MA 01824
(508) 256-4624
(VME) (PC/AT) (EISA) (G)
CIRCLE 637

★Intel Corp.
3065 Bowers Ave.,
M/S GR1-68
Santa Clara, CA 96051
(408) 765-1710
(MBII)
CIRCLE 638

★Interactive Circuits & Systems Ltd.
5430 Canotek Rd.
Gloucester Ont. CN K1J 9G2
(613) 749-9241
(VME) (DSP)
CIRCLE 639

★Interphase Corp.
13800 Seniac
Dallas, TX 75234
(214) 919-9000
(VME) (MBII) (EISA) (SBus)
(N) (SCSI)
CIRCLE 640

Ironics Inc.
798 Cascadilla St.
Ithaca, NY 14850
(607) 277-4060
(VME)
CIRCLE 641

★Lockheaed Sanders Inc.
9 Townsend W.
Nashua, NH 03061
(603) 885-3522
(VME)
CIRCLE 642

Logical Design Group Inc.
6301 Chapel Hill Rd.
Raleigh, NC 27607
(919) 851-1101
(VME)
CIRCLE 643

★Macrolink Inc.
1500 N. Kellogg Dr.
Anaheim, CA 92807
(714) 777-8800
(VME)
CIRCLE 644

★Matrix Corp.
1203 New Hope Rd.
Raleigh, NC 27610
(919) 231-8000
(VME) (STD)
CIRCLE 645

Matrox Electronic Systems
1055 St. Regis
Dorval, Quebec H9P 2T4
(800) 361-4903
(PC/AT) (G)
CIRCLE 646

★Micro Industries
691 Greencrest Dr.
Westerville, OH 43081
(614) 895-0404
(VME) (MBI) (MBII) (FB+)
(PC/AT)
CIRCLE 647

★Micro Memory Inc.
9540 Vassar Ave.
Chatsworth, CA 91311
(818) 998-0070
(VME) (MBI) (MBII) (SBus)
(PC/AT)
CIRCLE 648

Micro/sys Inc.
1011 Grand Central Ave.
Glendale, CA 91201
(818) 244-4600
(STD)
CIRCLE 649

Mizar Inc.
1419 Dunn Dr.
Carrollton, TX 75006
(214) 446-2664
(VME)
CIRCLE 650

★Motorola Computer Group
2900 S. Diablo Way
Tempe, AZ 65282
(602) 438-3512
(VME)
CIRCLE 651

★Nanotek Inc.
3690 E. Sunnyside Rd.
Idaho Falls, ID 83406
(208) 523-4468
(FB+)
CIRCLE 652

★Newbridge Microsystems
603 March Rd.
Kanata, Ontario K2K 2M5
(613) 592-0714
(VME) (PC/AT)
CIRCLE 653

New-Mark Systems Inc.
5319 Randall Pl.
Fremont, CA 94538
(415) 770-8350
(PC/AT) (STD)
CIRCLE 654

Omnibyte Corp.
245 W. Roosevelt Rd.
West Chicago, IL 60185
(800) 638-5022
(VME) (I/O)
CIRCLE 655

★Parsytec Inc.
245 W. Roosevelt Rd.
Bldg. 9, Unit 60/61
West Chicago, IL 60185
(708) 293-9500
(VME) (PC/AT) (NuBus)
(SBus)
CIRCLE 656

PC/M Corp.
6805 Sierra Ct.
Dublin, CA 94568
(415) 829-8700
(VME) (DSP)
CIRCLE 657

★Pentek Inc.
55 Walnut St.
Norwood, NJ 07648
(201) 767-7100
(DSP) (VME) (MBI) (MBII)
CIRCLE 658

★Pentland Systems ltd.
5627 Stoneridge Dr.
Pleasanton, CA 94588
(415) 460-3820
(VME) (I/O)
CIRCLE 659

PEP Modular Computers Inc.
600 North Bell Ave.
Pittsburgh, PA 15106
(412) 279-6661
(N) (VME) (G) (SCSI)
CIRCLE 660

(continued on p. 136)

NOTES

(MBI)	Multibus I
(MBII)	Mulitbus II
(N)	Network
(G)	Graphics
(T)	Turbo Channel
(FB+)	Futurebus+


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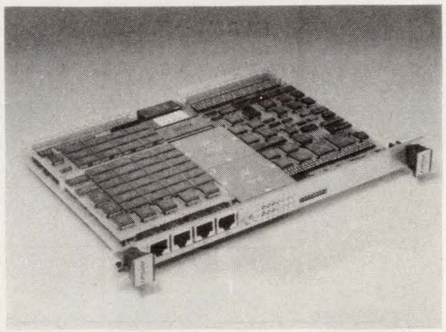
CIRCLE 156 FOR U.S. RESPONSE CIRCLE 157 FOR RESPONSE OUTSIDE THE U.S.

▼ SBC GETS 40 MIPS FROM DUAL 68040S

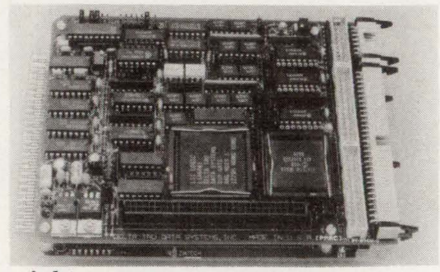


The SV420 is a single-board computer that's built with two 68040 microprocessors. The two processors share up to 32 Mbytes of high-speed DRAM and can operate in one of two modes, either tightly- or loosely-coupled. The VMEbus board offers 40 MIPS of processing power, supports zero wait-state memory cycles, and can offload 68040 tasks to an independent DMA coprocessor. VME64 is employed to double VME transfer speeds. Prices for the board start at $3745.

Synergy Microsystems Inc.
179 Calle Magdalena
Encinitas, CA 92024
(619) 753-2191.
▶ **CIRCLE 695**

▼ MULTI-AXIS MOTION CONTROLLER GAINS DSP

Adding digital-signal processing to gate-array technology equals an intelligent, programmable multi-axis controller (PMAC) for the STD and STD 32 buses operating at 10 MIPS. The ZT 8931 controls dc brush and brushless motors, as well as ac induction, stepper, and variable-reluctance motors. The controller is a two-board set that contains a Motorola 56001 digital-signal processor, four axes of motion control, and encoder feedback and ancillary-control functions. It supplies a 100-μs servo update rate per axis. A third board could be added to support a total of eight axes.



By using DSP technology, the controller allows more sophisticated servo algorithms, complex programming tasks, and faster throughput. The ZT 8931 can operate in a stand-alone configuration through an RS-232 port or within a system. Applications include general automation, robotics, and machine tooling. The four-axes version sells for $2988 and is available now.

Ziatech Corp.
3433 Roberto Ct.
San Luis Obispo, CA 93401
(805) 541-0488.
▶ **CIRCLE 696**

SAMPLING OF BOARD MANUFACTURERS

Performance Semiconductor
610 E. Weddell Dr.
Sunnyvale, CA 94089
(408) 734-8200
(VME)
CIRCLE 661

★Performance Technologies Inc.
435 W. Commercial St.
East Rochester, NY 14445
(716) 586-6727
(VME) (MBI) (SBus) (SCSI)
CIRCLE 662

★Polaris Communications
8219 SW Cirrus Dr.
Beaverton, OR 97005
(503) 643-1533
(VME) (PC/AT)
CIRCLE 663

Pro-Log Corp.
2555 Garden Rd.
Monterey, CA 93950
(408) 372-4593
(STD) (I/O)
CIRCLE 664

★Radisys Corp.
19545 NW Von Neumann Dr.
Beaverton, OR 97006
(503) 690-1229
(PC/AT) (VME)
CIRCLE 665

★Radstone Technology Corp.
20 Craig Rd.
Montvale, NJ 07645
(201) 391-2700
(VME) (MBI) (I/O) (SCSI) (N) (G)
CIRCLE 666

RGB Spectrum
2550 Ninth St.
Berkeley, CA 94710
(415) 848-0180
(G)
CIRCLE 667

Rockwell CMC
125 Cremona Dr.
Santa Barbara, CA 93117
(805) 968-4262
(VME) (N) (MBII) (PC/AT)
CIRCLE 668

★SBE Inc.
2400 Bisso La.
Concord, CA 94520
(415) 680-7722
(VME) (N)
CIRCLE 669

SGS-Thomson
Microelectronics/Inmos Div.
1000 E. Bell Rd.
Phoenix, AZ 85022-2699
(602) 867-6235
(VME)
CIRCLE 670

Siemens AG Auto Group
Gleiwitzer Strasse 555
Nurnberg, FRG D8500
911-895-3141
(MBI) (MBII)
CIRCLE 671

Sigma Information Systems
5775 Polaris Ave.
Las Vegas, NV 89118
(702) 597-5111
(SBus)
CIRCLE 672

★SMT
1080 Linda Vista Dr.
San Marcos, CA 92069
(619) 744-3590
(PC/AT) (I/O)
CIRCLE 673

★Sun Microsystems Inc.
2550 Garcia Ave.
M/S PAL 1-507
Mountain View, CA 94043
(415) 969-9131
(SBus)
CIRCLE 674

Synergy Microsystems Inc.
179 Calle Magdalena
Encinitas, CA 92024
(619) 753-2191
(VME)
CIRCLE 675

★Tadpole Technology
6310 Capitol Of TX Hwy N
Suite 375
Austin, TX 78731
(512) 338-4221
(VME)
CIRCLE 676

Teknor Microsystems Inc.
P.O. Box 455,
Sainte Therese, Quebec J7E 4J8
(514) 437-5682
(PC/AT) (G)
CIRCLE 677

Texas Microsystems Inc.
10618 Rockley Rd.
Houston, TX 77099
(713) 933-8050
(PC/AT)
CIRCLE 678

★Themis Computer
6681 Owens Dr.
Pleasanton, CA 94588
(415) 734-0870
(VME) (SBus) (N)
CIRCLE 679

★Trenton Terminals Inc.
2900 Chamblee Tucker Rd., Bldg. 10
Atlanta, GA 30341
(404) 457-0341
(PC/AT)
CIRCLE 680

★Vigra Inc.
4901, Morena Blvd. Suite 502
San Diego, CA 92117
(619) 483-1197
(VME) (G) (SBus)
CIRCLE 681

★VME Microsystems International Corp.
12090 S. Memorial Pkwy.
Huntsville, AL 35803
(205) 880-0444
(VME)
CIRCLE 682

★Workstation Products Inc.
322 Meadowlark Dr.
Richardson, TX 75080
(214) 669-9587
(VME) (SCSI) (N)
CIRCLE 683

★Xycom Inc.
750 N. Maple Rd.
Saline, MI 48176
(313) 429-4971
(VME) (PC/AT)
CIRCLE 684

Xylogics Inc.
53 Third Ave.
Burlington, MA 01803
(617) 273-5392
(VME) (MBII)
CIRCLE 685

XYZ Electronics Inc.
4700 North 600 West
McCordsville, IN 46055
(317) 335-2128
(STD)
CIRCLE 686

Yarc Systems Corp.
27489 W. Agoura Rd.
Agoura Hills, CA 91301
(818) 889-4388
(PC/AT)
CIRCLE 687

Zendex Corp.
6780A Sierra Ct.
Dublin, CA 94568
(415) 828-3000
(MBII)
CIRCLE 688

★Ziatech Corp.
3433 Roberto Ct.
San Luis Obispo, CA 93401
(805) 541-0488
(STD) (I/O)
CIRCLE 689

NOTES

(MBI)	Multibus I
(MBII)	Mulitbus II
(N)	Network
(G)	Graphics
(T)	Turbo Channel
(FB+)	Futurebus+

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FUJITSU MICROELECTRONICS ASIA PTE LTD. (Head Office, Singapore): Ph: 65-336-1600 Fax: 65-336-1609. HONG KONG SALES OFC: Ph: 852-723-0393 Fax: 852-721-6555.
TAIPEI SALES OFC: Ph: 886-2-757-6548 Fax: 886-2-757-6571. JAPAN SALES OFC: Ph: 81-3-3216-3211 Fax: 81-3-3216-9771. KML CORP. (Rep., Korea): Ph: 82-2-588-2011 Fax: 82-2-588-2017.
PACIFIC MICROELECTRONICS, PTY. LTD., (Rep., Australia): Ph: 61-2-481-0065 Fax: 61-2-484-4460.
FUJITSU MIKROELEKTRONIK GmbH (Dreieich-Buchschlag, Germany): Ph: 06103-6900 Fax: 06103-690122.

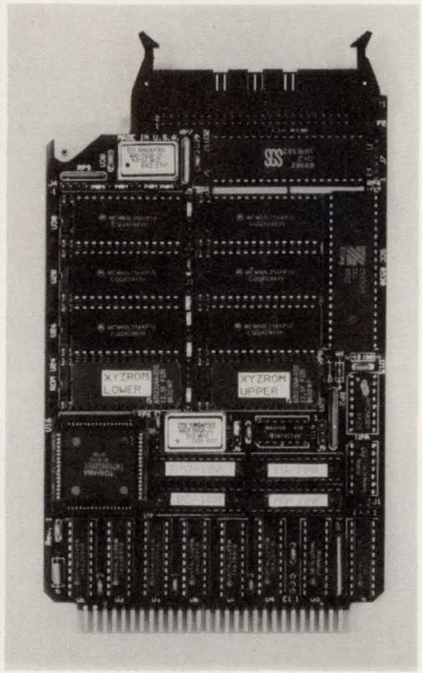
CIRCLE 126 FOR U.S. RESPONSE

CIRCLE 127 FOR RESPONSE OUTSIDE THE U.S.

BUS/BOARD PRODUCTS

▼ STD DEVELOPMENT BOARD USES 16-MHZ 68000

Based on the XYZ CPU-68K16, the SB-68K16 processor card for the STD bus comes with a C compiler, assembler, and text editor. In addition, 512 kbytes of RAM as well as a 256-kbyte RAMdisk are included. All the user needs to supply is an STD card cage and a 9600-baud terminal or a



PC with a communications package. No disk drive is required. Hardware features include a 16-MHz 68000 processor, three timers, and two RS-232/422/485 serial ports. The board's software is based on Microware's OS-9/68000 operating system. The board is priced at $1300.

XYZ Electronics Inc.
4700 North 600 West
McCordsville, IN 46055
(317) 335-2128.
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▼ FUTUREBUS+ SUBRACKS HOLD 70% HEAVIER LOAD

The Metrix 2000 is a family of "hard metric" products designed specifically for the packaging of Futurebus+ systems. The family includes a complete range of electronic cabinets, cases, and Metripac subracks and plug-in units to meet the recently established mechanical standards for the next generation of Futurebus+ products.

The line of subracks features 70% more weight-carrying capacity than traditional Eurocard systems used by VME. This is done without sacrificing airflow over the boards. They also feature complete conductivity and shielding capability for electromagnetic compatibility, as well as specially designed PVC guide rails for protection from electrostatic discharge when inserting a plug-in unit. Prices for the subracks start at $300.

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Warwick, RI 02886
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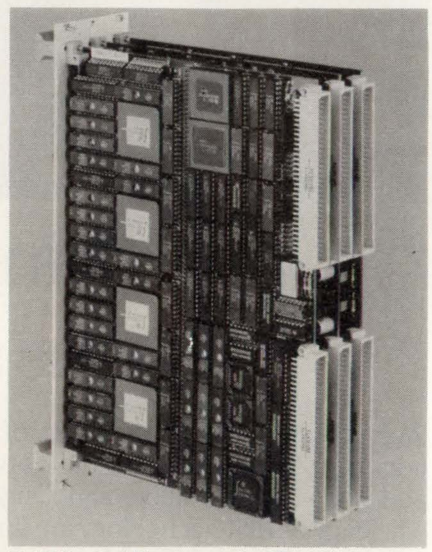
▼ 68040 VME CPU BOARD STANDS BY MIL SPECS

A VME board based on a 25-MHz 68040 microprocessor is fully designed to military specifications. The CPU-40 is an NDI (non-developmental item) solution for military applications. Suited for high-speed, real-time embedded systems, the board holds up to 8 Mbytes of dual-ported



RAM, 2 Mbytes of EPROM or 4 Mbytes of flash EPROM, and 128 kbytes of EEPROM. It comes in five software-compatible versions: full military standard air- and conduction-cooled, ruggedized air- and conduction-cooled, and commercial grade for low-cost product development and prototyping. The full military board is priced at $29,480 and will be available in the third quarter of next year.

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Montvale, NJ 07645
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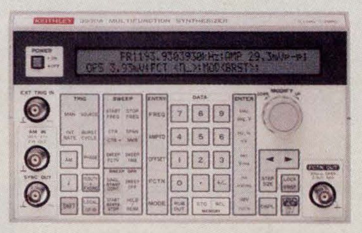

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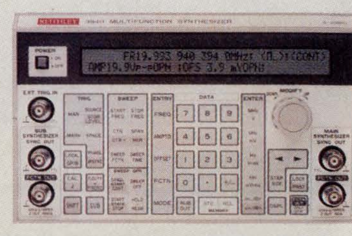

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KEITHLEY INSTRUMENTS

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CIRCLE 159 FOR RESPONSE OUTSIDE THE U.S.

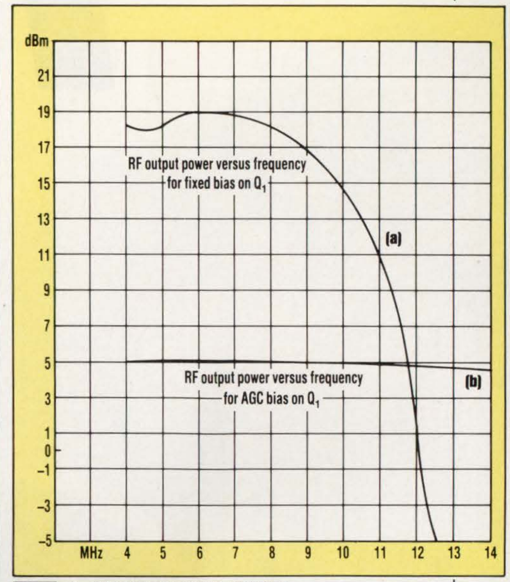
CIRCLE 521

AGC Gives Top Tuning Range

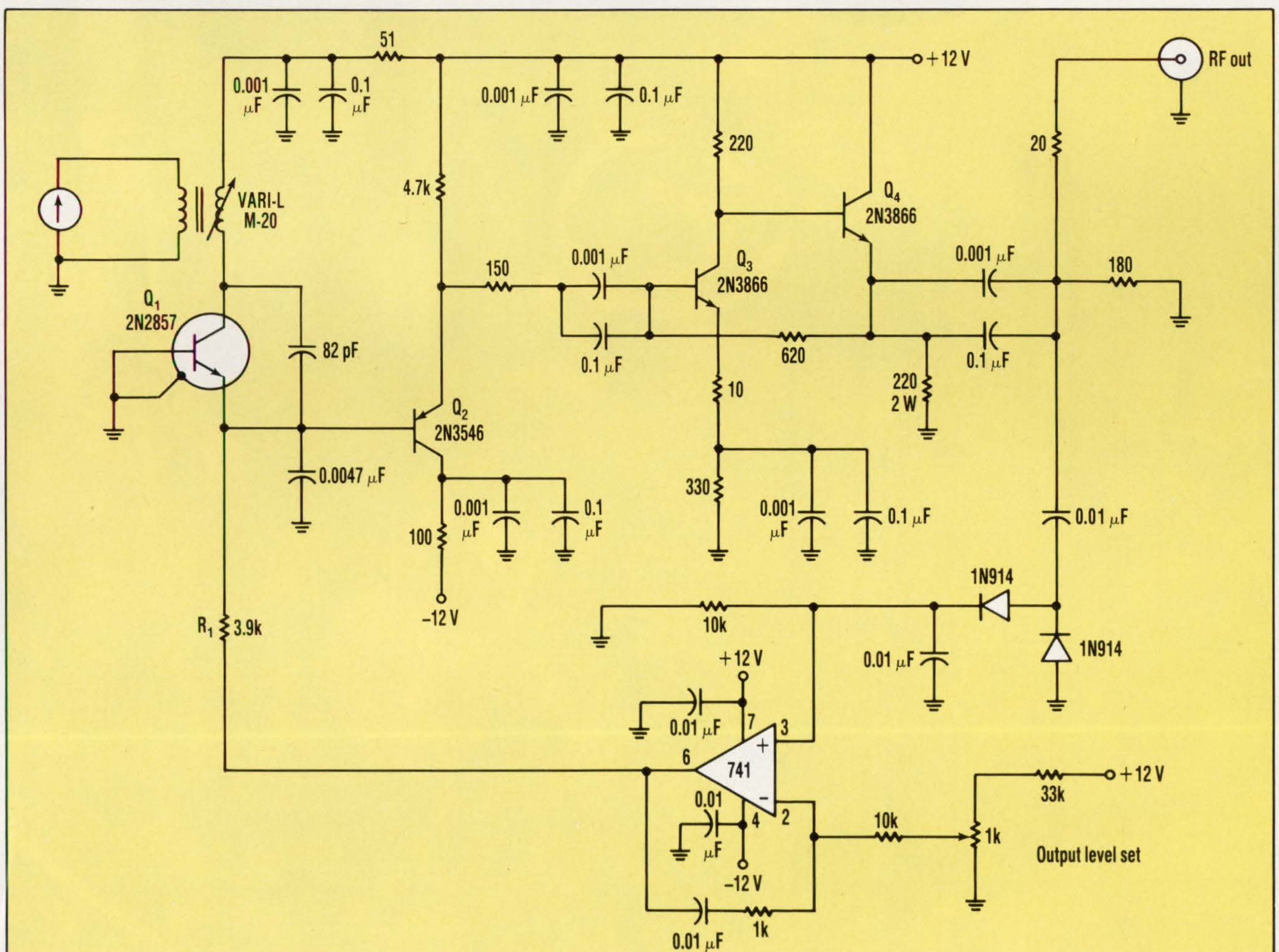
JOHN DUNN
181 Marion Ave., Merrick, NY 11566.

This variable frequency oscillator can be tuned from 4 to 14 MHz using a current-controlled variable inductor *(Fig. 1)*. The RF output power delivered to the load is stabilized by an automatic-gain-control (AGC) loop. Without the AGC loop, the full tuning range couldn't have been achieved. This is illustrated in the power versus frequency curves, which show the dramatic effect the AGC loop has in leveling the output power. *(Fig. 2)*.

Without AGC, the changing LC ratio of the oscillator tank circuit causes the RF amplitude to vary so much versus frequency that the full frequency range can't be achieved. However, with AGC feedback applied to transistor Q_1, the transconductance of the transistor is adjusted automatically to the value that's required to produce the desired output level. As a result, the full tuning range that's specified for the variable inductor can be properly exploited.□



2. WITHOUT THE AGC loop, the oscillator's output varies with frequency (a). The output is stable with the loop (b).



1. BY USING A current-controlled variable inductor, this variable frequency oscillator can be tuned from 4 to 14 MHz. The wide tuning range is achieved with an automatic-gain-control loop.

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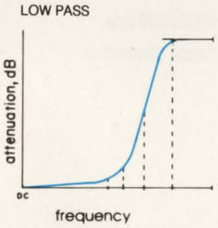
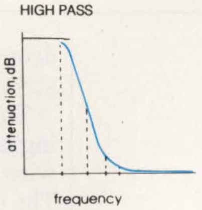
LOW PASS



low pass dc to 1200MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	STOP BAND, MHz (loss>40dB) Max.	STOP BAND, MHz Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45

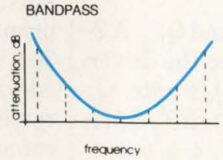
HIGH PASS



high pass dc to 2500MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	PASSBAND, MHz Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	STOP BAND, MHz (loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95

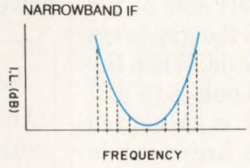
BANDPASS



bandpass 20 to 70MHz

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	PASS BAND, MHz Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	STOP BAND, MHz (loss > 10 dB) Max. F4	STOP BAND, MHz (loss > 20 dB) Min. F5	STOP BAND, MHz (loss > 20 dB) Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95

NARROWBAND IF



narrowband IF

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	STOP BAND, MHz I.L. > 20dB F6	STOP BAND, MHz I.L. > 35dB F7	STOP BAND, MHz I.L. > 35dB F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

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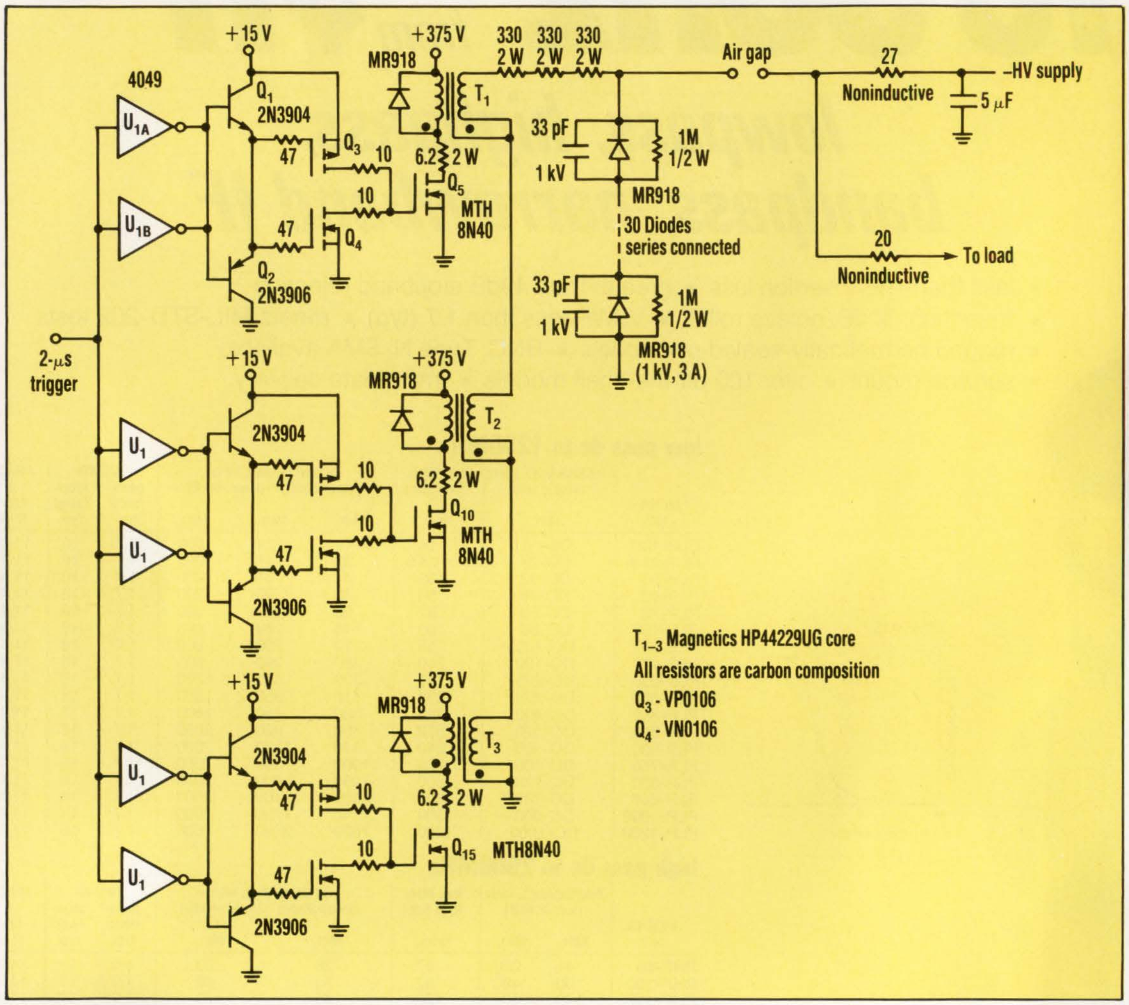
F132-2 REV. ORIG.

CIRCLE 172 FOR U.S. RESPONSE **CIRCLE 173 FOR RESPONSE OUTSIDE THE U.S.**



THE triggered, two-electrode air gap can switch 2.4 MW. The crowbar pulls the output voltage from 8 kV to 150 V in less than 2 μs. The implementation is for a negative supply. To crowbar a positive supply, the transformer primary connections and the diode string must be reversed.

CIRCLE **522**

HV Crowbar Switches 2.4 MW

DAVE CUTHBERT
1308 SE 65th Ave., Hillsboro, OR 97123.

High-voltage crowbars typically come in four flavors: thyratron, ignitron, vacuum gap, and air gap. This particular circuit is a triggered two-electrode air gap that can switch –8 kV at 300 A (2.4 MW) *(see the figure)*. It was designed to crowbar microwave-tube power supplies with capacitor banks under 5 μF. The crowbar pulls the output voltage from –8 kV to –150 V in under 2 μs.

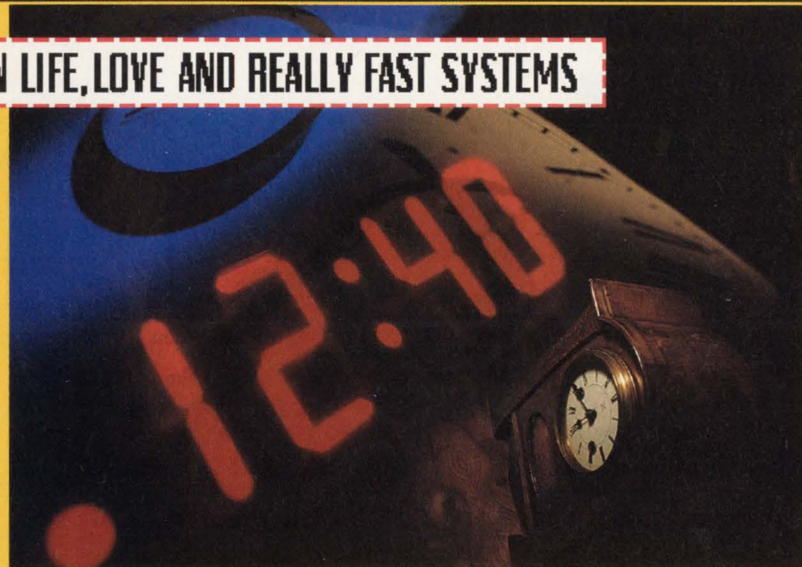
The crowbar consists of a high-voltage (HV) pulse generator, a current-steering diode, and an air gap. The first of three identical FET drivers consists of U_{1A}, U_{1B}, and Q_{1-4}. A 2-μs positive trigger causes the driver stage to pulse 1 A into Q_5's gate. Q_5 then switches 45 A through T_1's primary. T_1 outputs a 9-kV, 1-A pulse. With T_{1-3}'s secondaries in series, the output is 27 kV. The left side of the air gap is at –8 kV and the gap is set to break down at 15 kV dc. When the left side of the air gap pulses to +27 kV, a total of 35 kV is measured across the gap and it arcs over in about 300 ns. The negative HV supply now discharges across the air gap and through the current-steering diodes to ground. The voltage drop across the air gap and diode string is 150 V.

The transformer secondary winding is a single layer of #32 enameled wire (75 turns) on a plastic bobbin. The core of the pot core is connected to one end of the secondary, so it must be insulated from ground. The primary is wound with three turns of 30-kV wire. The air gap is constructed with two 1/4-in. carriage bolts. By reversing the transformer primary connections and the diode string, the crowbar can be used with positive power supplies.□

Send in Your Ideas for Design

Address your Ideas-for-Design submissions to Richard Nass, Ideas-for-Design Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604.

TIMING IS EVERYTHING, IN LIFE, LOVE AND REALLY FAST SYSTEMS



Imagine you had a fully adjustable TTL delay line, accurately programmable from 25 to 400ns. Would that change the way you control the timing of clock and control signals? It would give you the flexibility you need to get your design in sync with today's 33, 40, 50 MHz or faster CPUs. It also would eliminate the need to stock a broad range of fixed full-scale devices.

Brooktree's new Bt630 was designed with you in mind. It's the first CMOS digital delay line that's adjustable to meet all TTL timing requirements. And it's packed into a 14-pin plastic DIP package.

Handling small pulse width signals as a percentage of the delay is not a problem for the Bt630, nor is specifying leading and trailing edge delay accuracies.

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Betcha don't know the difference between a PC and a Workstation

It's come to our attention that the industry is lacking a precise definition for separating PCs and workstations.

At first we blamed that on the ubiquity of high speed 386 and 486 processors and fast Motorola MPUs used in Macs. Then we pinned the confusion on low memory prices, making every desktop machine a candidate for 8 megs or more. Suddenly we realized that super sophisticated applications software for PCs and Macs was the real culprit.

Guess what? It turns out it's probably all our fault. Our new Bt484 RAMDAC blurs the line between PCs and workstations. It's a true-color solution loaded with workstation features. But VGA-compatible and with a PC-like price.

Sorry to add to the confusion.

MAKE 1600 X 1280 YOUR NEW YEAR'S RESOLUTION

The continued evolution of workstation monitor resolution is about to write a new chapter. The evidence: 1600 x 1280 displays have dropped into the $4,000 range, just the price point that made today's widely popular 1280 x 1024 monitors "acceptable" several years ago.

Besides price—and the fact that higher resolution is an unending "gotta have" for workstation users—1600 x 1280 resolution acceptance is being driven by the growing desktop video/ multimedia movement in the U.S. and Europe and, in Japan, by the high-resolution demands of displaying kanji.

Customers using our Bt468 RAMDAC are ready for the move to 1600 x 1280. That's because the frame buffer architecture for 1280 x 1024 and 1600 x 1280 monitors are the same. It's an easy upgrade path. At 200 MHz or more, with 8:1 MUX and 25 MHz VRAM compatibility, it's a necessary component for 1600 x 1280 screens. If "early to market" is part of your systems strategy, you may want to take a good look at the readily available Bt468.

Editorial contributions: Tim Wilhelm, Luis Pineda, Ali Mesri and Cynthia Jones.

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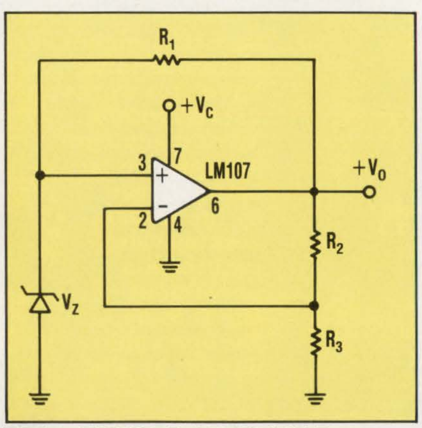
CIRCLE 523

Voltage Reference Has Dual Polarity

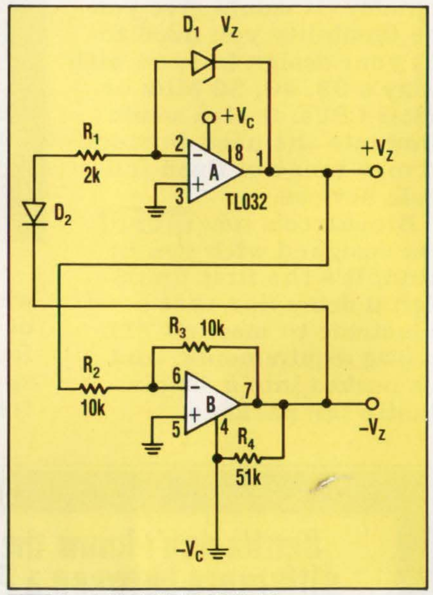
YISHAY NETZER
Yuvalim 112, Israel 20142; (972) 480-1017.

Zener diodes need a stable bias current to supply optimal performance, particularly precision-reference diodes. A classical approach employs a circuit that offers a buffered output and self-biasing for the Zener or reference diode that's stable and independent of the supply voltages *(Fig. 1)*. The output voltage of this circuit, which is given by the equation $V_Z(R_2 + R_3)/R_3$, is usually adequate. However, two possible shortcomings could develop. First, the output stability depends on resistors R_2 and R_3. Second, because it's based on a positive-feedback mechanism, it may latch on a negative saturation at power-up. This condition would forward-bias the Zener diode. Grounding the negative power-supply connection of the op amp can remedy this situation. However, the supply might be needed if other op amps share the same package.

An improved circuit is slightly more complex but is protected from a wrong latch-up by D_2 and R_4 *(Fig. 2)*. This is done without compromising the negative-supply connection. Its positive output only depends on the Zener diode. In addition, a complementary negative output is supplied.□



1. THIS TRADITIONAL circuit offers a buffered output and self-biasing for the Zener diode, which is stable and independent of the supply voltages. However, latch-up can occur when split supplies are used.



2. AN IMPROVED circuit uses D_2 and R_4 to protect against wrong latch-up. Here, the negative-supply connection needn't be eliminated. A complementary negative output is also available.

IFD Winner

IFD Winner for April 25, 1991

Christopher Gass, Motorola Inc., Bipolar IC Div., 2100 East Elliot Rd., MD EL340, Tempe, AZ 85284; (602) 897-3833. His idea: *"Select Line Voltages Instantly."*

VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $150 Best-of-Issue award and becomes eligible for a $1,500 Idea-of-the-Year award.

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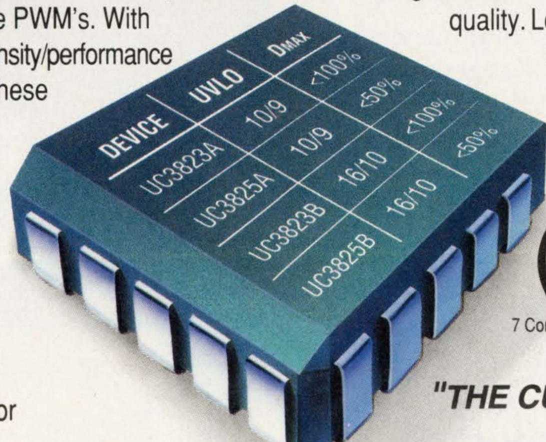

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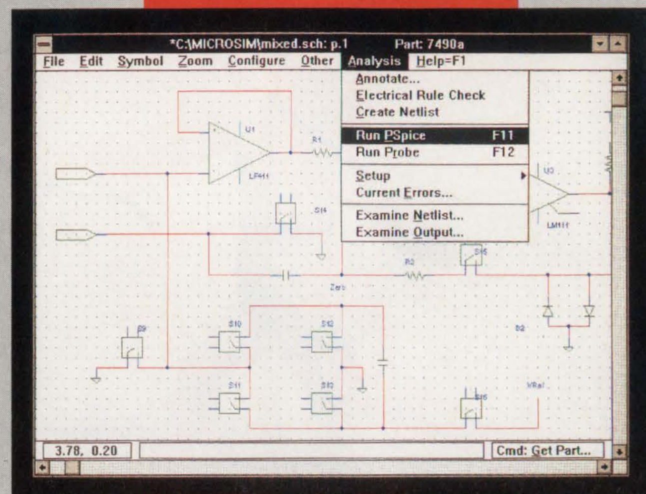

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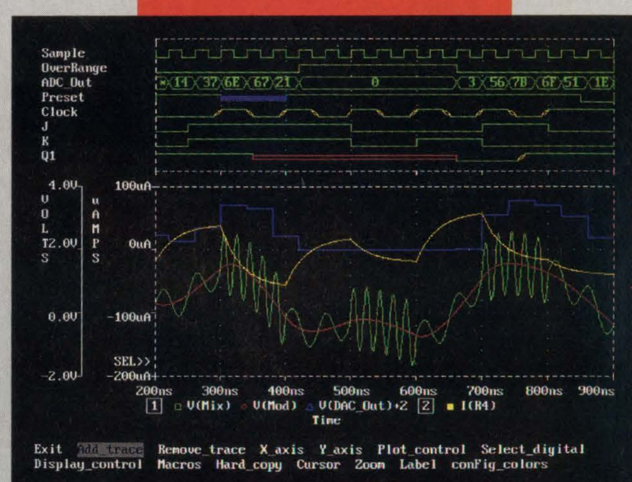

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CIRCLE 162 FOR U.S. RESPONSE **CIRCLE 163 FOR RESPONSE OUTSIDE THE U.S.**

ELECTRONIC DESIGN

QUICK LOOK

EDITED BY SHERRIE VAN TYLE

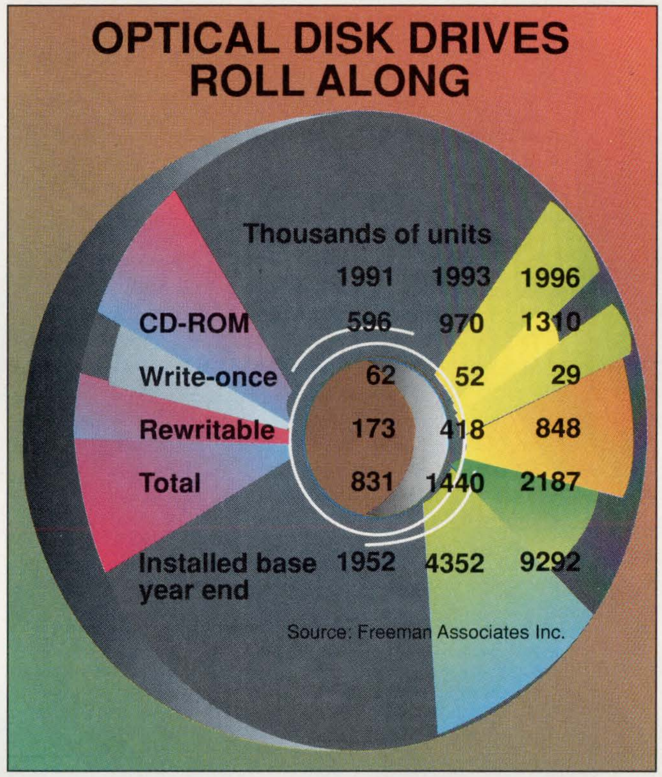
MARKET FACTS

In the wake of evolving technology, the optical drive market is changing in a big way. Write-once drives, which have led the market in revenues, this year will fall behind rewritable/multifunction drives, according to Freeman Associates' *Optical Data Storage Outlook.* Drive shipments last year increased 68% compared with 1989; 1990 revenues increased 34% from 1989, say the Santa Barbara, Calif., market researchers.

The worldwide market for all optical drives should hit $1.5 billion for OEMs in 1996, an 18% compounded growth rate from the $593 million value of the 1990 market. In 1996, 2.1 million units will ship—1.3 million CD-ROM drives, 848,000 rewritable and multifunction devices, and 28,900 write-once drives.

IBM and Sony each introduced 3.5-in. rewritable optical drives this year. Unit shipments of 3.5-in. drives will eclipse those of 5.25-in. drives in 1996 but the drives will lag in revenue throughout the period. Rewritable/multifunction drives will increase in terms of units shipped from 99,200 last year to 848,400 in 1996, a compound growth rate of 43%. Revenues during that period are expected to go from $224 million to $900 million, or 28% annually.

On the CD-ROM front, falling prices for hardware, software, and replication are widening the market for these drives. Shipments are expected to increase 22% a year to 1996; last year 404,000 units were sold vs. 1.3 million forecast for 1991. Revenue is expected to grow from $133 million last year to $229 million in 1996, or about 9% a year.



QUICK REVIEWS

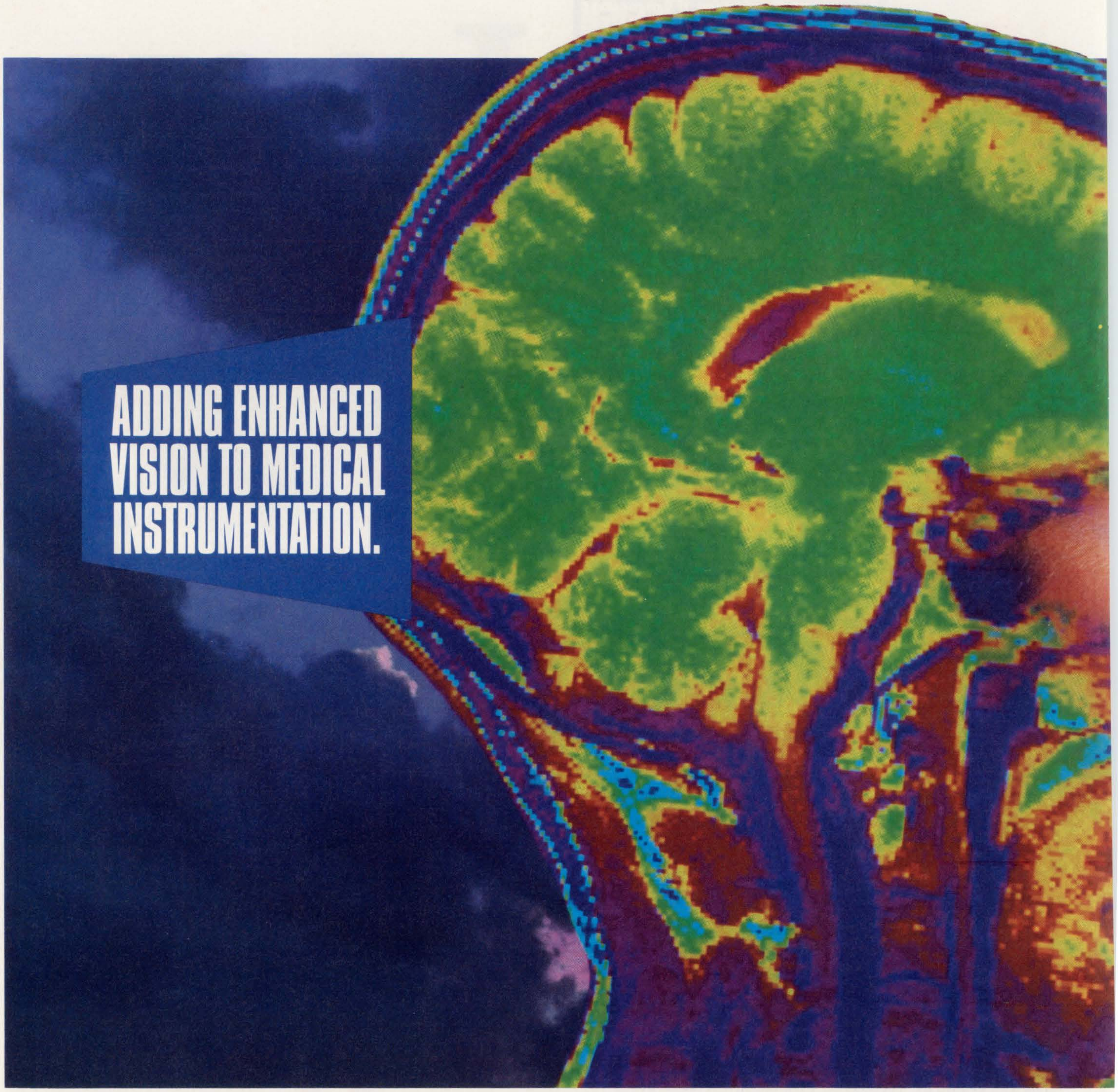
The Master IC Cookbook has saved designers thousands of hours of digging to find specifications for various ICs—analog and digital. By Clayton L. Hallmark and Delton T. Horn, the IC cookbook now has a second edition. The update has sections on TTL, CMOS products, memories, op amps, audio amplifiers, RF amplifiers, and other analog devices. The IC cookbook has other information, like pinouts, block diagrams, temperature ranges, truth tables, schematics, and voltage and current ratings. Published by TAB Books, Blue Ridge Summit, Pa., the book lists for $22.95.
CIRCLE 451

Defense electronics is a procurers' market at present. As a result, knowing how the buyer's bureaucracy works is a must for contractors. Now it's all set out in a book entitled *Defence Electronics—Standards and Quality Assurance* published in the UK by Butterworth-Heinemann Ltd of Oxford. Written by an Army officer, Lt. Col. Ray Tricker, its 378 pages give a detailed guide through labyrinthine U. S., European, and NATO military quality-assurance procedures, agencies, and standards.

Tricker says, "I wanted to provide a reference manual that will serve as an engineer's and manufacturer's guide to standards and organizations involved and to provide an indication of the way ahead—especially with respect to the European single market and the growth in market potential from ex-Warsaw Pact countries." Tricker is currently serving in Brussels, Belgium, as chief engineer of the NATO ACE COMSEC activity. The book also covers the more significant civilian quality standards and procedures, and includes a complete set of glossaries of terminology, abbreviations, signs, symbols and labels.

Defence Electronics—Standards and Quality Assurance has a list price of $119US. (ISBN 0-7506-0095-0). Contact: Butterworth Heinemann Ltd., Linacre House, Jordan Hill, Oxford, OX2 8DP England; 44 (0) 865-310366.
CIRCLE 452

To stay profitable or to expand, many U. S. electronics companies are expanding overseas. Small and medium-size companies rarely have the deep pockets to expand without help, however. Enter *Inside Washington: The International Business Executive's Guide to Government Money and Resources* by William A. Delphos. The book lists relevant programs and gives contact names and phone numbers. Appendices give local contacts and foreign offices. The 182-page book has a list price of $24.95 and is available from Venture Publishing NA, 600 New Hampshire Ave. NW, Washington, D.C. 20037; (202) 337-6300.
CIRCLE 469



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DSP Development Corp. offers an evaluation disk of DAPiSP, interactive graphics and data analysis software for engineers. Multiple windows can display data or analyses. With the program, designers can do fast Fourier transforms, digital filter design, convolutions, and waterfall plots. With DADiSP-488, engineers can bring data from instruments directly into a program window for viewing and analysis. Contact DSP at One Kendall Square, Cambridge, MA 02139; (800) 424-3131; fax (617) 577-8211. CIRCLE 454

Intelligent building technology is picking up steam in Japan. Among the developments are systems to monitor earthquakes and building sway, infrared systems to regulate HVAC, lighting, and blinds, and fiber-optic systems to send sunlight into windowless offices. For a copy of *Intelligent Building Technology* (NISTIR 4546), a report from the National Institute of Standards and Technology, send a self-addressed mailing label to Arthur Rubin, A313 Building Research Bldg., NIST, Gaithersburg, MD 20899; (301) 975-2762. CIRCLE 455

A 12-page bulletin describes Sprague-Goodman Electronics line of ceramic dielectric trimmer capacitors. Bulletin SG-305C has features, specifications, standard rating charts, schematic drawings, and application notes. Contact Bernice Feller, Sprague-Goodman Electronics Inc., 134 Fulton Ave., Garden City Park, NY 11040-5395; (516) 746-1385; fax (516) 746-1396. CIRCLE 456

What You Should Know About the Pension Law" explains your rights under current law, including benefits, payment schedules, and protections. The 60-page booklet, which costs 50 cents, is among a list available free or for a nominal fee from the government's Consumer Information Center, P.O. Box 100, Pueblo, CO 81002. CIRCLE 468

BEST SELLERS

Which technical books are the most popular in Silicon Valley?

ELECTRONICS:

1. *Art of Electronics, 2nd ed.*, by Paul Horowitz. Cambridge University Press, 1989. ***$49.50***
2. *Spice for Electronics Using Pspice* by Mohammed H. Rashid. Prentice-Hall, 1990. ***$24.***
3. *C Language Algorithms for Digital Signal Processing* by Paul Embree. Prentice-Hall, 1991. ***$55.***
4. *Spice Guide to Circuit Simulation* by Paul Tuinenga. Prentice-Hall, 1988. ***$23.***
5. *Logic Design Principles* by Edward McCluskey. Prentice-Hall, 1986. ***$61.***

COMPUTER SCIENCE:

1. *Inside Macintosh*, vol. 6. Apple Computer. Addison-Wesley, 1991. ***$39.95.***
2. *Power of Penpoint* by Robert Carr. Addison-Wesley, 1990. ***$22.95.***
3. *Postscript Language Reference, 2nd ed.* Adobe Systems. Addison-Wesley, 1990. ***$28.95.***
4. *Object Orientation Concepts, Languages, and Databases* by Setrag Khoshafian. John Wiley & Sons, 1990. ***$32.95.***
5. *Object-oriented Design with Applications* by Grady Booch. Addison-Wesley, 1991, ***$40.50***

This list is compiled for *Electronic Design* by Stacey's Bookstore, 219 University Ave., Palo Alto, CA 94301; telephone (415) 326-0681; fax number (415) 326-0693.

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085

Discovery of new things to do as the Executive Phase progresses can extend the product's time to market. Tasks are often omitted in the planning phase because some individuals lack a clear vision of what to expect in the future and are overly optimistic. There is generally more work to do than the planners think. As I noted in the Aug. 22 column, inexperienced workers tend to be the norm, and wishful thinking suppresses realistic thoughts. So it should be expected that most plans, produced without historical data, will contain major omissions.

My experience and data from major applications suggest that the preceding scenario holds true. On one program I managed, the KMET chart had the number of tasks grow by a factor of two over the program's duration. For this program, the growth in task count occurred because I did not have the vision to predict the structural detail of the task network 12 to 16 months into the future. Contributing to my lack of predictive vision was the limited vision of the team members who contributed to the plan. They also saw less to do in the future than they saw closer to the present.

Now that I've gone through the predictive process in detail and have coached others in doing this type of work, I'm better prepared to deal with this phenomenon. Experience is the best teacher. Only by recording task structure of present projects is it possible to create a history for future projects and build the experiential elements into the new product development team culture. Memories from previous projects and their historical databases become a new project's means to view the future.

Each project/program that follows the time-to-market methodology described in these columns leaves behind task data that contains detailed information for use by future project teams. Managers and their teams can use the data to become better synthesizers of work structures and to make more accurate time estimates. Critical information that can be used to reduce time to market can now be transferred to new teams with little training or effort.

DESIGN TIPS

MTBF: What does it mean to you? If I say my product has a mean time between failure (MTBF) of 100,000 hours, does this mean:

A. The product will last for 100,000 hours.

B. The average life of the product is 100,000 hours.

C. If the product operates for 10,000 hours per year (and has a useful life greater than 10,000 hours), there is a 9.05% chance that it will fail the first year.

What answer did you choose? Or more important, what does your customer think MTBF represents? The correct answer is C. However, many people (and possibly your customers) think MTBF means the useful life of the product.

MTBF means the failure distribution is exponential and the hazard rate—conditional probability of failure during a specific time interval–is constant. The reciprocal of constant failure rate is commonly referred to as mean time between failure. Using the MTBF value and time interval for a specific product, you can calculate the probability of survival for that product. Equation 1 gives the relationship for MTBF, time interval, and reliability for an exponential distribution:

$$R = \theta^{-\lambda t}$$

R = probability of survival or reliability
t = time interval of probability
λ = 1/MTBF

So, let's play with these numbers. If your customer thinks the product will last for 100,000 hours (t) before failing, what would your MTBF have to be? Answer: A. To calculate MTBF, convert equation 1:

$$\text{MTBF} = \frac{-t}{\ln R}$$

With this relationship, if the probability of no failure (R = 100%) before 100,000 hours, the MBTF would be infinity. So, we'll use a reliability of 99.99%. This product's MTBF for a probability of survival of 99.99% in a 100,000-hour time interval would be a little less than 1 billion hours.

Say your customer thinks the product, on the average, will last 100,000 hours (answer B). This can translate into a 50% probability of surviving in a 100,000 time interval and the MTBF would have to be a little less than 150,000 hours. What is the probability of the product surviving (reliability) for the entire 100,000 time interval? Using equation 1, the reliability of the product having a MTBF of 100,000 hours during a 100,000 time interval would be 36.78%.

What is the real MTBF of your products? Let's say you manufacture computer keyboards. The customer tells you the keyboards operate about 8 hours per day and that over a one-year period about 500 keyboards per million are returned. So, you have one million keyboards, each accumulati&g 2920 hours of operation per year for a total operation time of 2.92 billion hours. MTBF is now calculated by dividing total operational time by total number of failures during that operational time. For this example, the MTBF is 5.84 million hours.

$$\text{MTBF} = \frac{2.94 \times 10^9 \text{hours}}{500 \text{ failures}} = 5.84 \times 10^6 \text{hours/failure}$$

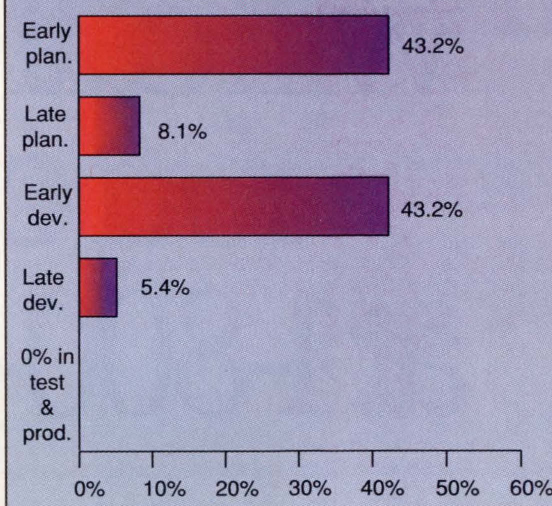
What should you do if your customer does not understand the real meaning of MTBF? In the total quality management frenzy sweeping the country, you should give customers what they want. If your customer expects your product to operate for a specific period of time without failure and your competitors are giving the customer products that operate over a specific period of time without failure, you should begin adopting useful-life design techniques.

Many classical reliability prediction tools and demonstration tests won't help a manufacturer achieve a useful life of the value of the MTBF figure of merit. Adopting rigorous physics-of-failure approaches to design, combined with analyses and tests that identify wearout mechanisms associated with fatigue, help reach useful life goals in line with current MTBF misperceptions.

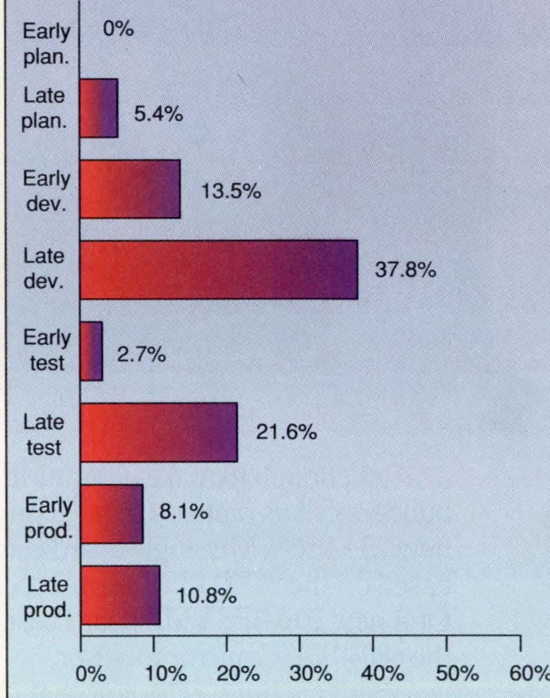
Michelle Lindsley works with commercial and defense electronic companies to improve the effectiveness of their reliability programs (206) 481-7391. She is working on a doctorate in industrial engineering at the University of Washington, Seattle.

DRAM SURVEY

WHEN DO YOU DETERMINE DRAM SPECS?



WHEN DO YOU PICK A DRAM SUPPLIER?



Source: a survey of Electronic Design readers by Penton Publishing Inc. Percentages total more than 100% because readers gave multiple answers.

DID YOU KNOW?

. . . that an estimated 69.2 million video displays are in use in the U. S. today; 55.7 million are monitors attached to PCs in monochrome or color graphics format. By 1997, more than half of all workers will use a VDT on the job.

International Data Corp., U. S. Department of Labor

What's All This Mathematics Stuff, Anyhow?

When I was at MIT, the math instructors had some famous problems. They were all about some mythical person called Little Egbert, and all of the interesting mathematical things that happened to him. I've been intending to find some more Little Egbert problems, and I even intended to ask some guys when I was at a class reunion this summer. But I guess I didn't ask the right people. Still, I remember one problem very well:

Little Egbert got a horn for Christmas, and the shape of the horn was a radius of r = (1/x) feet, from x = 1 to ∞. Egbert decided he wanted to paint his horn. (a) He decided to compute the area of the outside of the horn, so he would know how much paint to buy. Then, (b) he decided to compute the volume of the inside of the horn, so he would know how much paint to buy for that. What did Little Egbert decide?

BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

If you do your integration, the first answer is the integral of 2 π (1/x) dx, from 1 to ∞. That's the natural log of x, and the natural log of ∞ is still ∞. So, (a) would take an infinite amount of paint.

But if you integrate to get the *volume* of the horn, that's the integral of pi$(1/x^2)$dx, which works out to $-\pi(1/x)$, evaluated at 1 and at ∞. That works out to barely 3.14 cubic feet of paint, or about 23-1/2 gallons—definitely a finite number for (b).

Hey, there's a neat paradox. Little Egbert can paint the inside of his horn—but he can't paint the outside. What's the math trying to tell us? Well, at any time, thinking is permitted (even if not required). If you had a horn with a diameter of even 1 micro-inch, or a thousandth of a micro-inch, you would still have to wrap two or three molecules of paint around this very thin shaft, to say that you had painted it. Then if the thin end of the horn goes on forever, an infinite amount of paint will be needed to try and cover it. Conversely, by the time the diameter of the horn gets down to a small fraction of 1 milli-inch, a molecule of paint will refuse to go any further down inside the very narrow passage. At this point, you know that only a finite amount of paint will be needed to fill it up. So, Little Egbert can paint the inside of his horn by filling it up, even though it would be impossible to paint the outside of the horn. You can philosophize about the math, or you can philosophize about the paint. Either way, the answer makes some sense.

When I was a freshman at MIT, I took the standard class—was it M21?—on Fourier analysis. I did all of the problems; I passed the tests. Then I went on to more classes in math and physics. Years later, when I was transferring into Electrical Engineering, the instructors showed you how to predict what would happen if you tried to shove a broadband signal into a wire or cable that did not have infinite bandwidth. How do you compute what kind of modified, filtered, attenuated signal comes out at the far end? Why, Fourier analysis tells you which components will be attenuated.

Well, I was astonished. You mean to tell me that Fourier analysis was *good for something*?? Why didn't they say so back in Freshman math? Nobody ever indicated that Fourier analysis was *useful*. As I got further and further into E.E., I found that a whole bunch of the mathematical techniques we had been taught were, indeed, actually good for something. These mathematical techniques had been invented to help solve a problem, and they were presented because they had the potential for being useful, even if they forgot to tell us students. So, math is a very useful science—the handmaiden of the sciences, as they used to say—and sure enough, math is still useful every day. Some people say, why learn math or geometry or calculus or algebra if it's something you will never need? Of course, in some parts of the world, you do need math every day. How will you know if you will need it if you never try it? If you have the aptitude, it may indeed turn out to be very useful.

Now, what's all this "math aptitude" stuff, anyhow? Well, I've taken a bunch of aptitude tests, and it won't surprise you to hear that I get high scores in several kinds of math aptitudes. I took tests with the Johnson O'Connor Research Foundation (with offices in 12 major cities)* and they found I'm good at Number Reasoning, Accounting Aptitude, Analytical Reasoning, Number Memory, and Structural Visualization. Now, when I took these tests, I already suspected I was good at these things, because I sure didn't get through MIT by being ultra-intelligent. I got through because I was good at taking tests, and at manipulating the data to get reasonable answers. I went to take the aptitude tests because I was curious why I was having so much fun taking tests, and the aptitude tests confirmed my suspicions. Not everybody has good math aptitudes. Only a small fraction of women have as good "Structural Visualization" scores as 1/4 of the men do. But the best women are just as good as the best men. Both of my sons have taken these aptitude tests, and both

PEASE PORRIDGE

score very high on Structural Visualization. But one son has low scores for other kinds of math aptitudes, which means he is great at geometry, but lousy at algebra and calculus (which we already knew...).

I still do lots of math in my head, or on a slip of paper. I rarely use my calculator—maybe once a week, and I use my slide rule about as often. For example, I used my slide rule to get the 23.5 gallons of paint. There's no point in knowing if it was 23.4875 or any other number, because there are still cases where "engineering accuracy" of a percent or so is quite adequate. The rest of the time, I just do the math in my head, or on paper. But I *do* use a *digital* calculator to do my taxes; I stopped using my slide rule for that. I figure it would be hard to explain a few bucks of round-off error to the IRS guys....

For example, the other day, a friend of mine wanted to know how big her old aquarium was, as she was draining it to transfer the fish to a new tank. I took a piece of graph paper and measured out the number of inches in each dimension. I did some quick-and-dirty multiplication, and then used long division to divide by 231, which is the number of cubic inches in a gallon. I told her about 30 gallons. Another guy got a foot ruler, and used his calculator to multiply the number of cubic feet by 62.4, to convert the cubic feet into pounds, and divided by 16, the number of pounds in a gallon. He got 16.18 gallons. My friend found this amusing, as she had already removed 18 gallons of water and had a good bit more to go. Of course, as we reconstructed the scene of the crime, we realized that there are about 8 pounds in a gallon, not 16, so the answer of 30 or 32 was indeed about right.

Still, when I interview a prospective engineer, I try to find out if he has any aptitude for math, and if he is rusty or on his toes. I wouldn't refuse to hire a guy who used a calculator to get the right answer, but it had better not slow him down. Math is a tool, and if we're prepared to use it with skill and ease, it leaves us more time to work on the serious aspects of our project. If a guy tells me he plans to double a resistor so he can get more current through it, it makes me suspicious because he's liable to waste a lot of time on wild-goose chases.

These days, Spice is supposed to help us on our circuit analysis, and when it does, that's nice. But many circuits don't need the full precision and power of Spice to give a suitable answer. Sometimes a good rule-of-thumb answer is just right. Then you can use that as a sanity check, to confirm that Spice is performing a reasonable computation, and that nobody mistyped anything.

When I was in the 7th grade, I got in some squabble with the math teacher. He "won" the argument. So he forced me to stay after class to memorize the square roots of all the digits from 1 to 10. What a horrible punishment!! It did take me a little time to get them memorized correctly—and to this day, they're awfully useful (with the exception of the square root of 7, which really does not get used once in a decade....). I mean, the square root of 2 and of 10 are used all the time in engineering. And the square root of 3 tells you about the side of a 30/60/90-degree triangle. And the square root of 5, about 2.236, is the voltage you see on your ac voltmeter when you add 1 V and 2 V of noise.

Come to think of it, I don't recall that he ever forced any other kids to memorize square roots. I remember a couple of kids who had good music aptitudes, and he set them the "punishment" of learning "Stella by Starlight," which he said was his favorite song. I bet they remember that, to this day, too!! I don't think I gave him much credit, at the time, for being a very bright fellow. But, maybe I ought to admit that Mr. Holmes was a pretty smart cookie, after all. Please, Bre'r Fox, don't throw me in the briar patch....

All for now. / Comments invited! / RAP / Robert A. Pease / Engineer

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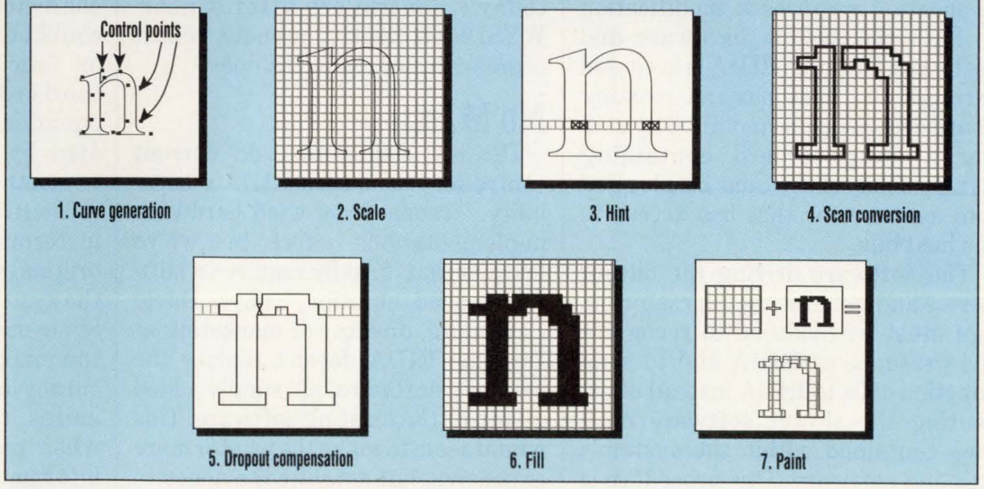
HARDWARE ELIMINATES BOTTLENECK ASSOCIATED WITH LASER PRINTERS TO PUMP OUT 7500+ CPS.

ASIC PUSHES LASER PRINTER TO ITS LIMIT

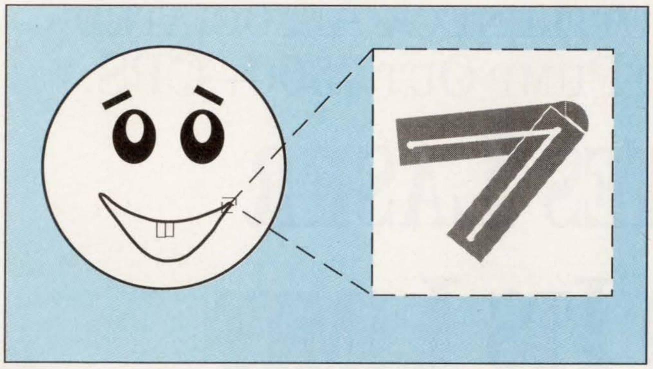
RICHARD NASS

Higher performance at a lower cost is the catch-phrase of the electronics industry. With that concept in mind, laser-printer manufacturers have migrated to RISC processors rather than their CISC counterparts. At some point, however, performance overkill can set in. The hardware can only run as fast as the software will allow. For instance, although printer engines are rated at a particular speed, the printer rarely runs at that speed because of the software bottleneck. This is where RIDA (Raster Image Device Accelerator), from Destiny Technology Corp. comes into play. Not only can RIDA, an ASIC, let the printer run at its rated engine speed, it can also support a much faster engine.

Destiny wanted to address several areas when designing RIDA, including the acceleration of outline fonts, line-art graphics, and half-tone images. The software is processor-independent and highly modular, allowing designers to integrate RIDA into existing controllers and motherboards quickly. Destiny tried to eliminate the boundaries typically associated with traditional laser printers. For example, the company created characters with a 1000-point size maximum. Moreover, RIDA supports even-odd and nonzero winding



1. WHEN PRODUCING AN OUTLINE FONT, RIDA first assigns control points to an image or character, then scales the character. Hinting minimizes the distortion. Scan conversion followed by dropout compensation fills in any inadvertent gaps. The last steps include filling in the outline and painting the character to the frame buffer.



2. THE TIP of the smiling face is constructed of three parts—two rectangles and a circle. One step is saved when RIDA determines that the rectangles are identical. It simply makes a copy of one and slides it into the correct position.

fills, as well as Type 1, Intellifont, Bullet, TrueType, and Speedo font formats.

RIDA can be applied in a hard-copy controller, a cartridge, a graphics adapter, or on a system board. Because it consists of just one chip, it easily fits onto almost any motherboard. As a hard-copy controller, it offers fast page composition, even at resolutions above 300 by 300 dots/in. It also offers universal font rendering. To employ RIDA as a printer controller, the hardware redesign is fairly simple. All that's needed is to ensure that RIDA has access to the bus and the single-character cache memory where the bit-mapped characters are stored.

Incorporating RIDA into a display application requires a modification to both the system hardware and software. Because RIDA is accessed through the host bus, an existing board design can be modified by adding a daughtercard containing RIDA. This card would be plugged into a connector that has access to the host bus.

The software driving the output device and generating the raster image must be modified to recognize the presence of RIDA and to send function calls to RIDA instead of executing the slower software modules contained within the system's existing software. This procedure is similar to the way a math coprocessor is accessed.

When used in a cartridge, RIDA can upgrade and accelerate an existing printer. In this case, the cartridge would command complete control of an Hewlett-Packard LaserJet-type printer. After initialization, the printer's firmware detects whether there's a command program stored in the cartridge. If so, then the printer allows the cartridge to take over by passing control over to the cartridge's firmware.

When employed as a graphics adapter, RIDA supplies a WYSIWYG (what you see is what you get) display, as well as scrolling and screen repaints for font-intensive applications, such as desktop publishing. In the still-unreleased Windows 3.1, TrueType is included, giving users scalable outline fonts for both the display and printer. TrueType is Microsoft's and Apple's scalable outline-font rendering technology—it's included in Apple's recent System 7.0 release. If placed directly on a system's motherboard, RIDA can act as a controller for both the printer and the display to accelerate both outputs. Destiny says that today's controllers offer a near-WYSIWYG display, but not an exact representation, as RIDA does.

No Match

Destiny claims that no current controller can match RIDA's capability. "People have tried hardware implementations before, but we've learned that it really requires a software-based solution," says David Larrimore, director of marketing at Destiny. RIDA doesn't replace the printer's software; it's simply added on top of the existing software. This would seem to make the printer more expensive, but actually the opposite is true. With RIDA, a lower-performance and less-expensive processor can be used, more than offsetting RIDA's price. And, at the same time, the performance is improved.

Simulation results show that the ASIC offers an outline font generation of better than 7500 characters/s. This translates to 3-3/4 full text pages/s, regardless of the font type being implemented. The number of characters/s can be determined by multiplying the number of characters produced in a cycle by the number of cycles/s. The number of characters produced in a cycle can be approximated because the algorithm's run time is measurable.

With RIDA's universal font rendering, display or hard-copy devices can handle any of the standard fonts used by application programs. The universal font rendering also adds a proprietary font hinting with dropout compensation and y-alignment. Dropout compensation enables high-quality outline fonts to be printed or displayed without any performance degradation. This feature is also responsible for true rendering of Japanese Kanji characters and other non-Roman fonts.

Acceleration Methods

Destiny defines three different methods of graphics-object acceleration—outline font, line-art graphics, and half-toned images. The first step in producing an outline font is to generate the control points *(Fig. 1)*. For a Roman character, there are typically 20 to 50 control points defining the character. For a Kanji symbol, there could be up to 250 points. Any three or four points could constitute a third-order curve. A mathematical equation defining the curve is generated by calculating the curve between the points.

There may be some inconsistency in terms of accuracy between the original source information and how the system defines that information. Some distortions are created during the mapping process because of accuracy loss. The hinting process minimizes the distortions that occur when mapping the high-resolution information to a lower resolution. Quite often, gaps are formed when a pixel is turned off because less than 50% of the pixel is being used. RIDA has built-in dropout compensation

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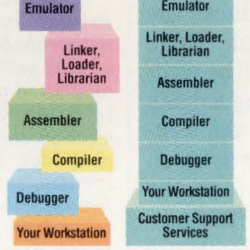

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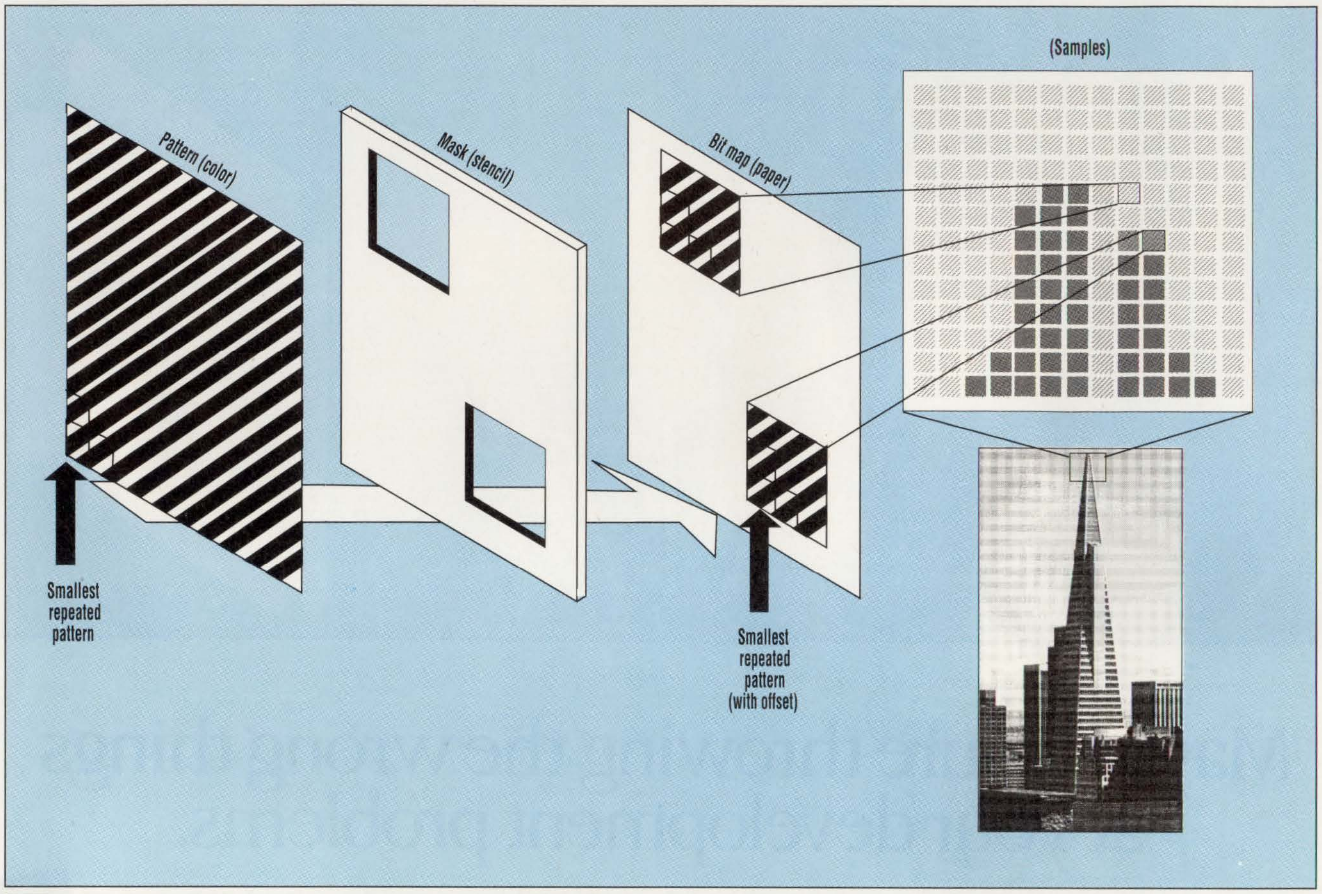


3. IN THE HALF-TONE IMAGE ACCELERATION, a pattern is first created. RIDA takes the smallest repeated pattern and creates a mask. The pattern is written through the mask and sent to the frame memory.

that fills these gaps. The outline font is then filled and converted to 300 dots/in. so it can be handled by the print engine.

The second type of acceleration can best be seen using an example of a smiling face *(Fig. 2)*. Here, the tip of the mouth (the stroke) is a large area consisting of many pixels. The stroke now has length and width, as well as an interior pattern, not necessarily solid black. Each stroke is an independent graphic object with length and width. To construct the tip of the mouth, three components are constructed—the two rectangles, and the circle that joins them. But the three components are made up of two strokes because RIDA identifies that the two rectangles are identical. The first rectangle is copied and simply slid into the correct position.

The half-tone process consists of three elements *(Fig. 3)*. A pattern (or colors for a color printer) is generated to simulate the gray scales. RIDA uses the smallest repeated pattern—using the smallest area reduces the amount of memory needed. Then, the area that the pattern will be written to is determined, creating a mask or stencil. The final step is the writing process. The pattern is written through the mask and sent to the frame memory. Typically, the pattern generation is general-purpose computation that's handled for each individual macro pixel by the printer's main CPU. But the mask is handled very efficiently by RIDA.

Destiny says that better than 80% of the laser printers sold today get shipped to the U.S., rather than staying in Japan where they're manufactured. This is because the Kanji characters are very difficult to produce. Thus, the laser printers that are available in Japan run extremely slowly when printing the Kanji characters. Destiny feels that RIDA will open the door to the Japanese laser-printer market.□

PRICE AND AVAILABILTY

Printers implementing RIDA technology will probably start to emerge around June of next year, although RIDA will be demonstrated at this year's Comdex/Fall '91 in October. RIDA may make an appearance in the first quarter of next year in cartridge form. The RIDA family will eventually consist of three members. The first member, available in the third quarter, will focus on the outline fonts, because that's presently the slowest part of the printing process. It'll be housed in a 144-pin quad flat pack and sell for $35 each. The second release, planned for the second quarter of next year, will accelerate all elements of the printing process equally. And the third chip, due out by the third quarter of 1992, will enhance the half-tone image acceleration.

Destiny Technology Corp., 300 Montague Expwy., Suite 150, Milpitas, CA 95035; (408) 262-9400. **CIRCLE 512**

HOW VALUABLE?	CIRCLE
HIGHLY	565
MODERATELY	566
SLIGHTLY	567

BUILD MIXED-SIGNAL ASICs WITHOUT ANALOG CELLS

A SUITE OF CAE TOOLS HELPS DIGITAL DESIGNERS CREATE MIXED-SIGNAL ASICs SPORTING ON-CHIP TEST OF ANALOG CIRCUITS.

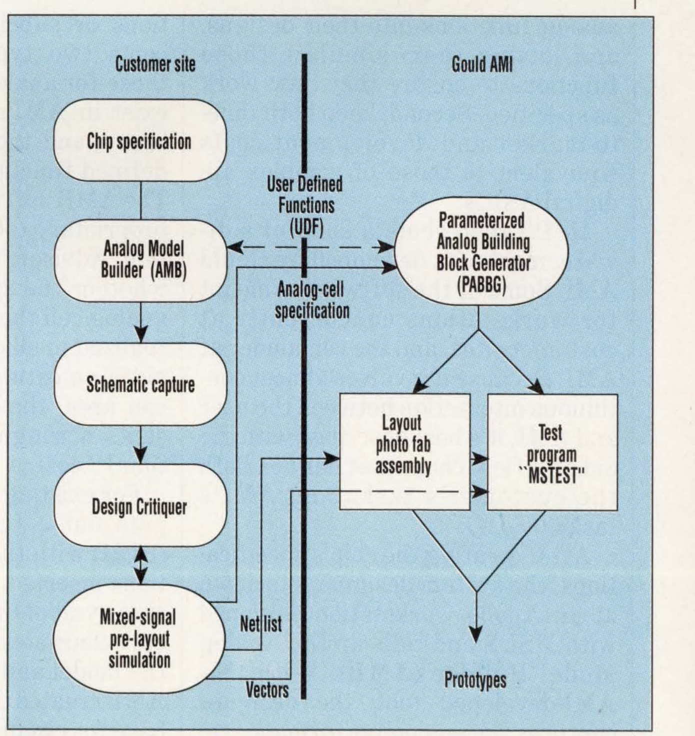
FRANK GOODENOUGH

Today, system designers aren't taking advantage of mixed-signal ASICs for several interrelated reasons. At the top of the list, of course, sits the specialized nature of the analog world, where each new system requires its own unique circuits. No matter how "well characterized" an analog design may be, a designer working with a standard-cell analog library may call for a couple of cells that just happen to need some minor modifications. Worse yet, some required analog cells may not exist in that library.

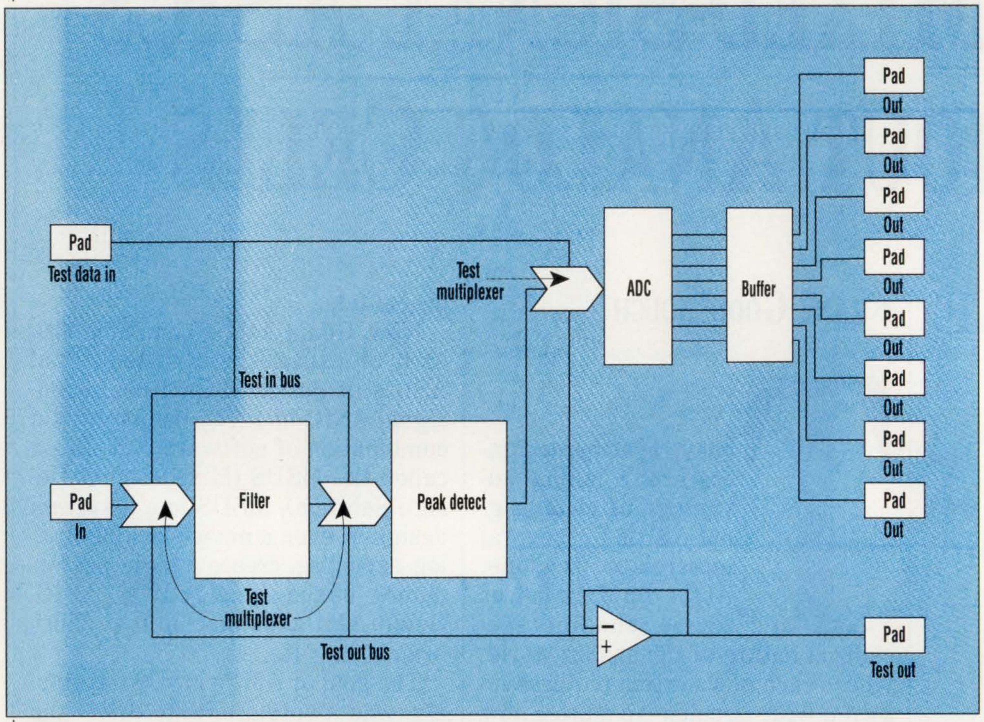
The well-publicized shortage of skilled analog designers and the formidable task of testing mixed-signal ICs compounds this problem. For instance, a modern 100,000-gate digital IC truly represents a test engineer's nightmare. Adding op amps, comparators, and data converters to such a chip, to interact with the chip's RAM, ROM, logic, and ALU, exacerbates the already tough testing task several orders-of-magnitude.

Now, Gould AMI, a company with early-on experience in mixed-signal ASICs (it designed its first mixed-signal ASIC in 1977), has created a combination of software and silicon called the MSDS (Mixed-Signal Design Solution). MSDS lets a system designer, even a novice lacking analog expertise, create a high- performance mixed-signal CMOS ASIC. Gould AMI adds on-chip testability prior to layout.

The goal of AMI's MSDS developers was twofold. First, drive the mixed-signal design process "down the digital path." System designers can do this by incorporating custom



1. BEHAVIORAL MODELS OF functional blocks are created by Gould AMI's mixed-signal ASIC design system at the customer's site, with a software tool called the Analog-Model Builder. Thus, the company doesn't need to offer a large library of analog cells.



2. ANALOG MULTIPLEXERS permit the isolation and testing of a chip's individual analog circuits, like the filter, peak detector, or analog-to-digital converter. The multiplexers are added to a customer-designed mixed-signal ASIC by Gould AMI's designers.

analog functions into their designs, and letting them simulate those functions to ensure that they work as specified. Second, keep both time-to-market and development costs equivalent to those of complex all-digital ASICs.

MSDS represents a suite of software, most of it developed by Gould AMI. Some of the software is meant for workstations concurrently at customer sites, and the remainder at AMI. Because it involves almost continuous interaction between the user and AMI, it's best described with the aid of a flow chart that defines both the customer's tasks and AMI's tasks *(Fig. 1)*.

After creating the chip's specifications, the system designer sits down at an Apollo workstation equipped with MSDS and calls up the Analog Model Builder (AMB). With this AMI-developed tool, the designer captures the analog performance requirements and the cell specifications. These include such characteristics as slew rate, offset voltage, output voltage and current, and bandwidth, for various analog functions or subcircuits. The AMB accepts two types of specifications: those for analog blocks that already exist in AMI's configurable cell library, and those for the customer-defined functions not in the library. The AMB software includes another proprietary tool called the Specification Advisor. It tells the designer whether the specifications for each analog cell they need can or can't be realized in silicon. The tool also provides an estimate of each cell's silicon area, the total of which represents a rough estimate of production-IC cost.

For existing analog cells, the AMB puts out a behavioral level model (BLM) with the user's cell specifications inserted, plus a schematic-capture symbol that has properties (circuit characteristics) attached. With the model and its specifications, the AMB creates the analog/digital data base for circuit simulation later. The AMB also takes the data for the customer-defined functions and creates data sheets and specification files for the Parameterized Analog Building Block Generator (PABBG) software at Gould AMI in Pocatello, Idaho. The circuits created by the generator replace new cells for a library. The PABBG creates both the capture symbol and the BLM for the customer-defined functions. The AMB, in addition, creates the performance parameters used by AMI's test software in Idaho (known as MSTEST), to create test programs for the future mixed-signal ICs.

The rapidly growing list of analog functions supported by the AMB includes:

- Elliptic, Bessel and Butterworth filters.
- Pierce-type crystal and RC oscillators.
- A bandgap reference.
- Inverting and noninverting gain stages (that can include a chopper-stabilized op amp).
- A shunt-type voltage regulator.
- A comparator.
- An 8-bit resistive DAC.
- An 8-bit ADC (using the DAC and successive approximation).
- A sampling amplifier.
- A peak detector.
- An analog switch.
- A buffered analog multiplexer.
- A buffered input pad.
- A variable-drive output buffer.

After grabbing the schematic with a standard capture tool from Mentor Graphics Corp., Beaverton, Ore., the user examines his design with another AMI tool, the Design Critiquer. This neat expert system reviews the mixed-signal ASIC's database, looking for combinations of functional blocks that can create flaws in the design.

Once the Critiquer finishes its analysis, the mixed-signal ASIC is ready for simulation. AMI chose the mixed-signal simulator Saber CADAT, developed jointly by Analogy Inc., Beaverton, Ore., and Racal-Redac, Westford, Mass., to do that job for the MSDS. Well-known today as a mixed-signal simulator, it handles feedback loops that include both analog and digital elements, operating at levels from device through behavioral to HDL. In addition, it can handle a complete system, including non-electronic devices like motors, and thus aid in partitioning the system and its simulation. When the user is satisfied that the future chip will work as specified, the database and simulation files serve as the input for physical chip design (layout, photo-fab and assembly), and MSTEST circuit and program generation, respectively, at AMI *(Fig. 1, again)*.

Invisible to the user, a suite of software called Application Tool Interfaces (ATIs) simplify the user's task. They generate all of the information needed to run a tool, eliminating extensive customer training as well as continual reference to manuals and memorization of complex commands and syntax.

Incorporating on-chip circuitry to test the mixed-signal analog circuits in a customer-designed ASIC represents true innovation. Using the inputs from the customer's database, AMI designers added CMOS analog multiplexers to the circuit *(Fig. 2)*. Circuit nodes that must be stimulated and/or provide the results of stimulation, as well as the bus controlling the mutiplexers, are connected to test pads on the chip. At the wafer-probe stage, each circuit block can be checked separately. Some or all of the pads can be brought out to pins for testing after packaging.

Following the simple circuit shown, during chip operation, the signal flows from the pad labeled "In" (lower left), through the test multiplexer to the filter, through another multiplexer to a peak detector, through another multiplexer to an analog-to-digital converter, and then to a set of output pads *(Fig. 2, again)*. However, during testing, stimulation is applied to the input pad, and through the multiplexer to the filter. The filter's output multiplexer connects the filter to the "test-out bus" and through a buffer op amp to a test-out pad (lower right). As a result, the filter's response is measured. If it's okay, the filter's output is reconnected to the peak detector and its output is connected to the test-out bus, instead of the ADC. Finally, the whole circuit is tested.

Such a sequence of events is ideal when looking at prototypes. In fact, because the test circuitry increases the silicon area by 8 to 10%, once a designer is satisfied with the prototypes, some or all of the test circuits can be deleted, if financially feasible, because the signal flows from the input pad to the converter in production. However, if a number of chips showed up later with similar bugs, the multiplexers make troubleshooting easy.

AMI's MSDS is available for virtually all of their sixty odd CMOS processes. These include 1.5-μm digital/3.5-μm analog processes with double-metal and double-polysilicon capability. Digital supply voltages can range from 2.5 to 12 V and analog supply voltages from 5 to 12 V. Electrically-erasable-programmable memory cells as well as 40-V drivers are also available.□

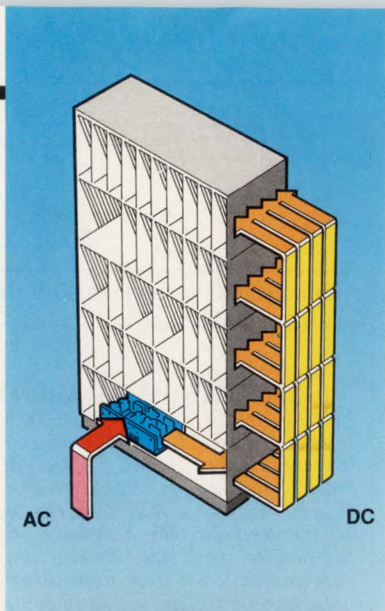
PRICE AND AVAILABILTY

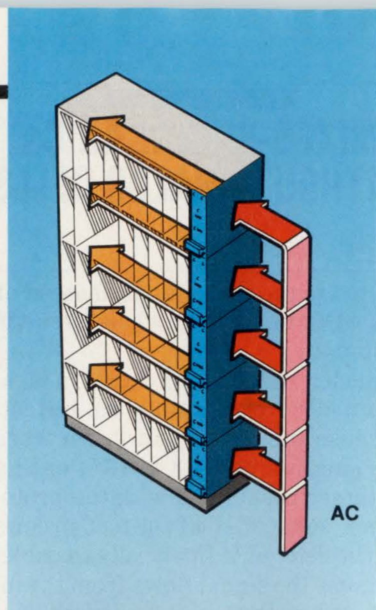
Pricing for MSDS starts at $75,000, including Saber CADAT. Purchasing an equivalent version of Saber-CADAT directly from Analogy or Racal-Redac costs $71,500. Typical NRE costs run between $20,000 and $45,000, depending on chip complexity and size. Production chips run from $2 to $20 each, depending on volume, packaging, die size, and complexity. Chip-design time is in the hands of the user. Turnaround time by AMI, from receipt of final design to availability of packaged prototypes, typically runs 12 weeks.

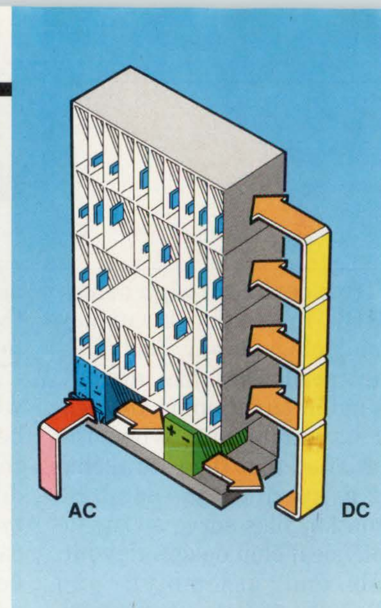
Gould AMI, 2300 Buckskin Rd., Pocatello, ID 83201; Traci Mousetis (pronounced mo see' tis), (208) 234-6679.

CIRCLE 514

HOW VALUABLE?	CIRCLE
HIGHLY	571
MODERATELY	572
SLIGHTLY	573







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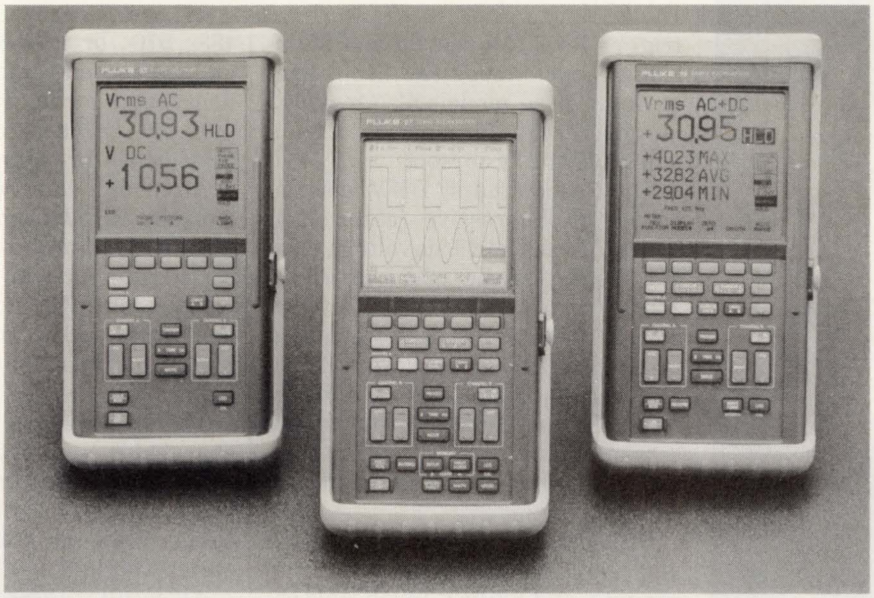
CIRCLE 124 FOR U.S. RESPONSE
CIRCLE 125 FOR RESPONSE OUTSIDE THE U.S.

ERICSSON



THE SERIES 90 ScopeMeters use a 5-in. diagonal supertwist LCD display with 240-by-240-pixel resolution. Electroluminescent backlighting on the top-of-the-line Model 97 (center) improves visibility.

50-MHz DSO Melds With Full-Feature DMM

John Novellino

A 50-MHz, 25-Msample/s dual-channel digital storage oscilloscope (DSO) for under $1800 is quite a bargain. Add a feature-rich digital multimeter (DMM) and even a limited-function signal source, and the result is a powerful as well as economical test instrument. More specifically, what you have is the 90 Series handheld ScopeMeters from Fluke and Philips *(see the figure)*.

The ScopeMeter's DSO captures waveforms in real-time or equivalent-time sampling modes. In the real-time mode, the 25-Msample/s rate delivers a 40-ns timing resolution. For repetitive signals, the equivalent-time sampling mode allows 400-ps resolution. The scope's rise time is 7 ns. Vertical resolution is 8 bits, and the record length is 512 points.

Eight waveforms and 10 setups can be stored for future use. The 240-by-240-pixel, 5-in. supertwist LCD screen displays up to four waveforms, in any combination from among the stored signals or two inputs. On the Model 97, electroluminescent backlighting improves visibility. With the roll mode, users can view signals over a long period by scrolling the waveform as a chart recorder would, while still capturing 40-ns or longer glitches.

To examine longer data streams, users can select a pretrigger mode (up to two screens) or a post-trigger mode (up to 100 screens). The display shows the actual

DIGITAL SCOPEMETERS

trigger level. Models 95 and 97 include N-cycle mode and event triggering. These models also make 12 automatic waveform measurements using the DSO's cursors.

The ScopeMeters' DMM also includes an impressive feature set. True RMS ac or ac + dc voltage measurements can be made to 600 V (1700 V pk-pk), and resistance measurements to 30 MΩ. The meter also takes dBm, dBV, and dBW readings, and makes diode and continuity tests. In the recording mode, the screen simultaneously displays maximum, minimum, average, and present readings.

Other features include relative and percent-relative modes, autoranging, and Fluke's Touch Hold capability, which holds the measurement on the display. A scaling function lets users set 0% and 100% points so that the reading is scaled accordingly. A dc millivolts input accepts a wide range of Fluke and Philips accessories, such as temperature probes and current probes and shunts. The ScopeMeter probes, which are used for both DSO and DMM functions, come with high-voltage and high-frequency tips.

The DMM's basic accuracy is within 0.5% for dc volts. For ac volts, basic accuracy is within 1% at 60 Hz, 2% through the audio range, 3% to 1 MHz, and 10% to 5 MHz.

EASE OF USE

To make all of this capability easy to use, the ScopeMeters incorporate autoset, soft keys, and pop-up menus, features traditionally found on larger bench instruments. In the scope mode, autoset adjusts the volts and time per division, position, and triggering controls for the input signal. In the DMM mode, the function automatically tracks the input for the proper range, time-per-division display, and triggering.

Five softkeys help the user select the desired functions. The pop-up menus clear up any questions about the instrument's capabilities.

An added feature on the Model 97 is a limited-function frequency generator. The instrument creates three waveforms: a 976-Hz sinewave; a 488-, 976-, or 1950-Hz squarewave; and a 4-second ramp. In the component-tester mode, these simple outputs can be used to check transistors, diodes, or other devices.

All models come with an optically isolated RS-232C interface for instrument calibration. On the Model 97, the interface can also be used for remote control, reading waveforms and setups with a computer, or printing to an HP ThinkJet or Epson FX/LQ printer.

The instruments come with rechargeable NiCd batteries, a built-in charger, and an ac-line adapter. They will also run on C-size alkaline batteries. With the holster, the ScopeMeter weighs 4 lbs.

All in all, the ScopeMeter series meets the needs of field-service technicians who repair a broad variety of electronically-controlled devices. In applications as diverse as testing biomedical equipment, or repairing and maintaining office machines, the instruments have the portability and measurement flexibility to tackle the problem at hand.

The ScopeMeters are the first instruments jointly developed by Fluke and Philips Test and Measurement under a joint agreement signed in 1987. Although the pact was primarily aimed at marketing, the companies also agreed to share technology and development programs, with Fluke contributing its 40-plus years of multimeter experience, and Philips its 50-plus years of knowhow in oscilloscope design.□

PRICE AND AVAILABILTY

List prices for the 90 Series ScopeMeters are $1195 for the Model 93, $1495 for the Model 95, and $1795 for the Model 97. The instruments are available from Fluke or Fluke-authorized distributors and representatives in North America, and from Philips Test and Measurement in Europe.

John Fluke Mfg. Co. Inc., P.O. Box 9090, Everett, WA 98206; (206) 347-6100.

Philips Test and Measurement, Bldg. TQIII-4 5600 MD, Eindhoven, The Netherlands. **CIRCLE 513**

HOW VALUABLE?	CIRCLE
HIGHLY	568
MODERATELY	569
SLIGHTLY	570

OPTOCOUPLER ZIPS ALONG AT 50-MBAUD DATA RATE

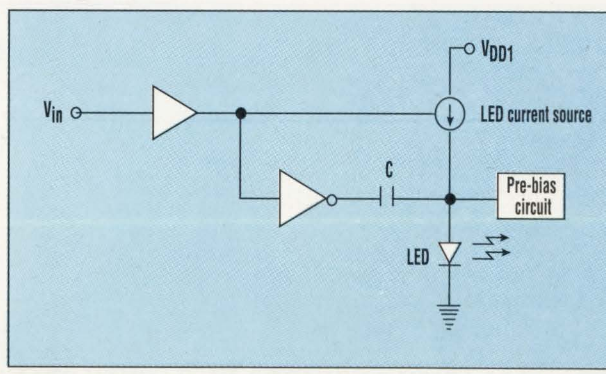
UNIQUE DESIGN COMBINES ELECTRICAL ISOLATION WITH PRECISION PULSE EDGES.

MILT LEONARD

Multiplexed data-transmission, computer-to-peripheral interfaces, I/O-port isolation in instruments, motor control, power inversion, and other similar applications often share a common requirement: The need for electrical isolation between electrically incompatible circuits. As an example, a data-transmission network may require communication links between system elements operating at different ground potentials. Without the use of a circuit-isolating mechanism, pulse distortion would render the transmitted data useless.

Optocouplers isolate a signal source and its destination by coupling signal-modulated light pulses between an LED and a photodiode. For high-speed data transmission, optocouplers have been speed-limited by the external circuitry required to compensate for low light-coupling efficiency, LED aging, logic interfacing, and external noise sources. However, an optocoupler from Hewlett-Packard introduces improved optical and circuit designs to set new performance standards. The HCPL-7101 optocoupler switches signals at a maximum nonreturn-to-zero (NRZ) rate of 50 Mbaud with a typical pulse-width distortion of less than 1 ns, versus 10 to 12 ns for conventional designs.

The 7101 includes a CMOS driver chip, an AlGaAs LED, and a CMOS detector IC. A CMOS or TTL input signal controls the driver IC that supplies LED current. The detector chip includes a photodiode, a transimpedance amplifier, and a voltage comparator with hysteresis. The 3-state output is CMOS- and TTL-compatible, and is controlled by an output-enable pin. The only external devices required are two ceramic bypass capacitors (0.01 to 0.1 **m**F) connected across the supply-voltage and ground pins of the two leadframes. External components required by prior solutions are no longer needed.



1. THE LED DRIVER IC for the 7101 optocoupler contains circuitry for forcing fast LED switching. The pre-bias circuit minimizes the effect of LED capacitance on turn-on time. G2 and C in the peaking circuit assist in shortening both turn-on and turn-off times. G1 converts TTL/HCT inputs to CMOS levels.

Due to the CMOS circuits and a unique light-coupling system, the 5-V 7101 uses just 12 mA of supply current, including LED current. The light-pipe design also contributes to the device's approval by international safety standards of such agencies as the Underwriters Laboratories in the U.S. and the Verbande Deutscher Electrotechniker (VDE) in Germany.

To reach a 50-Mbaud performance level, an optocoupler must have fast LED turn-on and turn-off times. This is the job of the LED driver. H-P's driver chip consists of a buffer with high input impedance for CMOS-logic-drive signals, a switched-LED current source, a pre-bias circuit, and a peaking circuit *(Fig. 1)*.

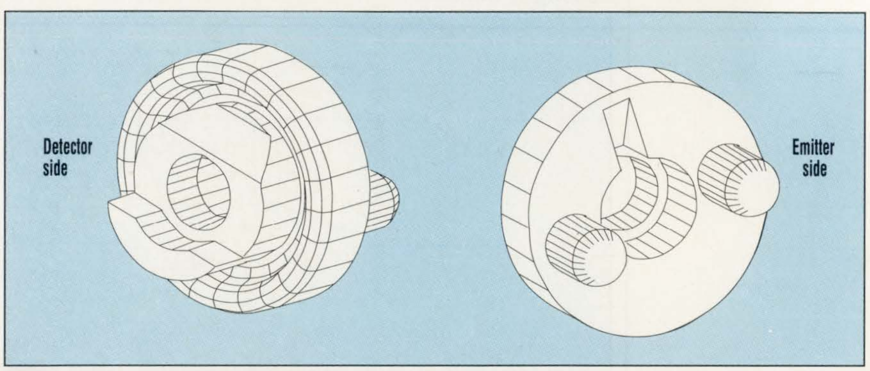
The pre-bias circuit minimizes turn-on time and propagation delay by precharging the LED capacitance while the LED is off, resulting in a faster rise time of LED current. This current is supplied by an amplifier that scales 20 μA of reference current up to 4 mA. The current-source and LED impedances have opposite temperature coefficients. As a result, changing temperatures have no effect on LED performance.

Early in its life, the LED needs only about 2 mA of current to turn on and deliver a given light intensity. As it ages, though, a higher current is required by the LED to get the original amount of light output. The peaking circuit *(G2 and C in Fig. 1)* offsets aging effects by charging capacitor C during LED turn-off. Upon arrival of an input pulse, the capacitor dumps its charge through the LED, forcing turn-on and minimizing the required on-current. Peaking results in a 10,000-hour guaranteed operation for the 7101.

The easiest way to couple light from an LED to a photodiode while providing separation is to mount the light emitter and detector face-upward in the same plane. Light from the LED reaches the photodiode by bouncing off the inside surface of a silicone globule encapsulating the two devices. Although this technique is low in cost, it has poor light-coupling efficiency because much of the emitted light is scattered and doesn't reach the photodiode.

In contrast, the H-P method mounts the LED on the input leadframe facing downward, and the photodiode on the output frame facing upward. The light pipe is a plastic structure containing a silicone-filled tunnel that forms the silicone into the desired shape for optimum light coupling *(Fig. 2)*.

Staked between the input and output leadframes, the light pipe has up to five times the light-coupling efficiency of planar designs, says H-P. At the same time, the double-heterostructure AlGaAs LED converts current to light energy with ten times the efficiency of GaAsP LEDs. All of these factors contribute to high light-coupling efficiency. They also allow greater spacing between the emitter and detector to meet the most stringent national and international safety requirements.



2. ISOLATION REQUIRED BY SAFETY STANDARDS is ensured by the 7101's light pipe, which provides a 0.5-mm separation between the LED mounted on the input leadframe and the photodiode mounted on the output leadframe. The cylindrical cavity through the center of the light pipe is filled with silicone, whose light-transmission properties are better than air.

In addition to providing electrical isolation, an optocoupler should duplicate the input waveform as closely as possible, especially for high-speed data transfer. H-P accomplishes this with several patented circuit designs, beginning with an active Faraday shield at the photodiode *(Fig. 3a)*. The photodiode converts LED light pulses into current pulses. However, when mounted on the output leadframe, it reacts to signal-degrading noise picked up from the environment and radiated by the input leadframe.

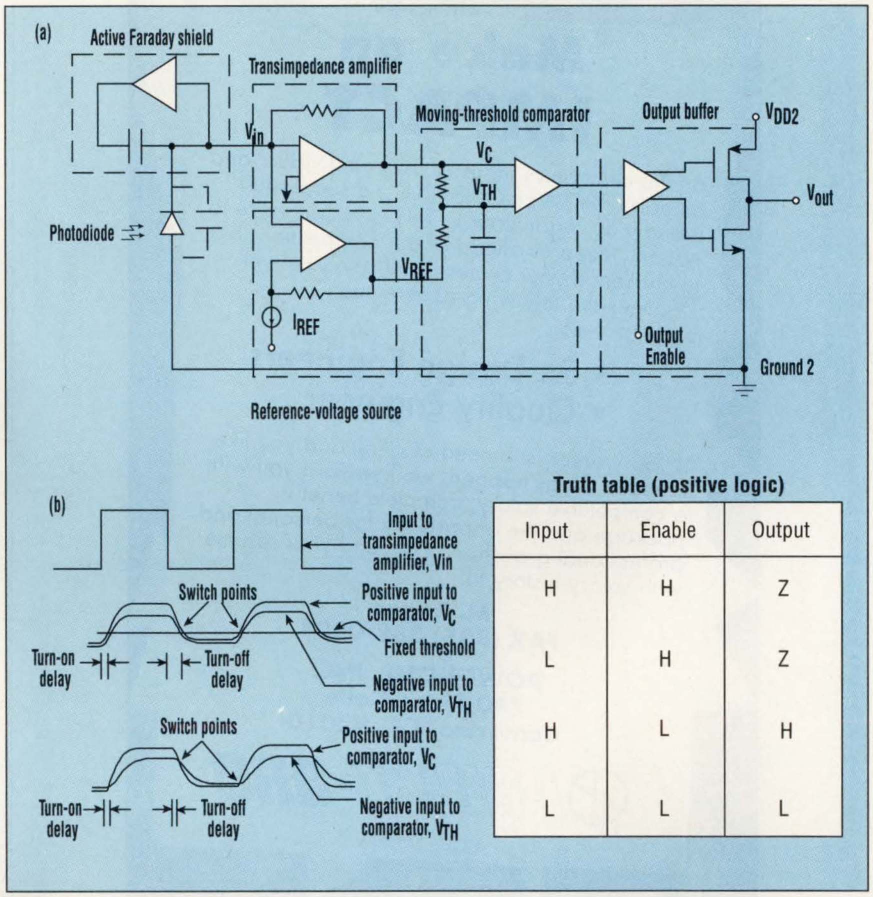
One way to shield a photodiode from common-mode signals is to cover it with a grounded, transparent conductive material. However, a photodiode is effectively a capacitor between two layers of silicon. Adding the capacitance of a grounded shield increases photodiode capacitance, which is typically 6 pF. Because shield capacitance can double or triple photodiode capacitance, the result is reduced bandwidth of the circuitry that follows.

Instead of using a grounded shield, the 7101 has it's shield connected to a fast buffer amplifier in a negative-feedback loop so that shield current cancels most of the input-noise current. This design preserves bandwidth with only a slight reduction in common-mode noise rejection.

Ideally, the threshold voltage for switching on the photodiode should be as close to zero as possible for minimum switching power, yet high enough to be immune to unintentional changes in photocurrent, such as from common-mode effects. Unfortunately, photodiode capacitance distorts the edges of input waveforms so that turn-on and turn-off times can be significantly different with a fixed threshold voltage *(Fig. 3b)*. Due to the propagation delay of the IC, turn-on time is typically 2 ns. But it takes from 10 to 20 ns for the falling edge of the input waveform to drop to the threshold voltage and switch off the photodiode. The result is pulse-width distortion.

In a simple but elegant solution, the 7101 avoids this problem by using a moving-threshold comparator

PRECISION OPTOCOUPLER



Truth table (positive logic)

Input	Enable	Output
H	H	Z
L	H	Z
H	L	H
L	L	L

3. PATENTED CIRCUITS integrated on the photodiode chip help duplicate the input-signal waveform as closely as possible (a). An active Faraday shield uses a negative-feedback loop to cancel common-mode signals radiated from the input leadframe. To avoid pulse-width distortion resulting from a fixed threshold voltage, the 7101 has a voltage divider that effectively drags the threshold voltage along with the input signal (b).

that effectively "drags" the threshold voltage along with the input current pulse. Here's how it works:

The transimpedance amplifier converts photodiode current into a voltage signal V_C, which is fed to one input of the comparator. A voltage-divider cir!uit comprised of two series resistors connects across V_C and a fixed reference voltage V_{REF}. The junction of the two resistors provides the threshold voltage V_{TH} to the other comparator input.

Consequently, V_{TH} tracks V_C with a slight offset in amplitude. However, a capacitor connected from V_{TH} to ground also causes V_{TH} to lag V_C slightly in phase. As a result, turn-on and turn-off delay are the same for both positive- and negative-going edges of the input waveform. Thus, the 7101 has a typical pulse-width distortion specification of less than 1 ns. This is important for data-communications applications in which precise, predictable location of pulse edges is vital. Such precision is also valuable for parallel data transfers that can't tolerate propagation-delay skews between channels.□

PRICE AND AVAILABILTY

The 50-Mbaud HCPL-7101 optocoupler comes in a standard 8-pin plastic DIP and is available now for $4.95 each in quantities of 1000. The HCPL-7100 15-Mbaud version is priced at $3.96 each.

Hewlett-Packard Co. Inquiries, 19310 Pruneridge Ave., Cupertino, CA 95014; 1-800-752-0900. **CIRCLE 515**

HOW VALUABLE?	CIRCLE
HIGHLY	574
MODERATELY	575
SLIGHTLY	576

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United Kingdom: John Maycock
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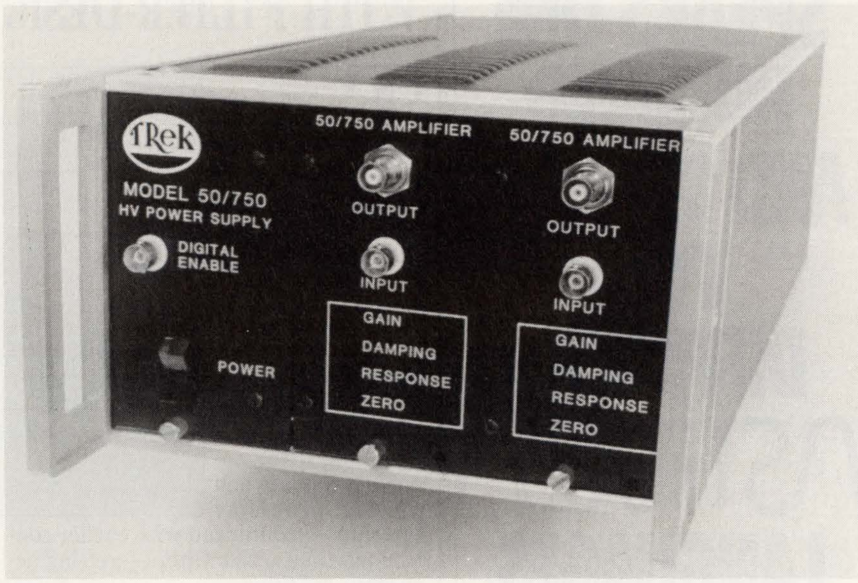
HV Op-Amp-In-A-Box Puts ±750 V Across 7.5 kΩ For 10 μs

Frank Goodenough



The Model 50/750 High-Voltage Solid-State Amplifier from Trek Inc. isn't your plain-vanilla op amp, but it's an op amp, albeit with an internally-closed feedback loop *(see the figure)*. By employing cascoded power MOSFETs in the output stage, each of the two all-solid-state amplifiers in the box can continuously put out ±750 V at 50 mA rms, or peak currents twice that, for 10 μs. Alternatively, because the amplifiers employ floating, optoisolated, linear drivers, their output stages can be strapped to provide 0 to 1500 V or 0 to –1500 V. In the present model, the strapping commits both amplifiers to the same output-swing range. By early next year, a revised version will permit each to be strapped separately. These aren't just variable high-voltage power supplies, though. They drive highly-reactive loads while remaining stable and the outputs can slew at over 125 V/μs, giving them a full power 3-dB bandwidth on the order of 30 kHz.

Such amplifiers (and even higher-voltage ones to ±20,000 V) are used in the ion implanters employed today in most IC processes. They also represent a valuable laboratory tool in piezoelectric and piezoceramic research and can drive the piezo micropositioning motors ("inchworms") used in precision optical systems. In addition, they're widely used in electrostatic-copier (Xerography) research and development, and for driving lasers and testing insulation. With their ac power bandwidth, they can drive audio and low-frequency ultrasonic piezo transducers. And of course, they perform well as general-purpose, high-voltage power supplies. They also find their way into the feedback loop of systems using high voltage.

Source And Sink

The full-scale input range of the Model 50/750 is specified as 0 to 10 V, 0 to –10 V and ±5 V, depending on the output swing selected. Screwdriver adjustments on the amplifiers' front panel independently adjust the gain of each between 10 and 150. Thus, the amplifier's output swing can be set by adjusting either the gain, or the input-signal level. Their true four-quadrant outputs continuously source and sink 50 mA at any voltage. As a result, with their inputs driven 180° out of phase by a 16-bit digital-to-analog converter, and their outputs driving each side of a floating load in a bridge configuration, the amplifier pair can produce a low-distortion 1500-V pk-pk sine wave well beyond the audio band. Alternatively, these solid-state amplifiers can develop a ±1500-V arbitrary waveform with a resolution of 22 mV, and that's while slewing at 125 V/μs. The 22-mV resolution is well above the 0.5-mV offset of the amplifiers (and the offset can be zeroed on the front panel). However, broadband (dc to 20 kHz) noise at the output runs about 60 mV rms, although most of it is high-frequency noise emanating from the unit's switching power supply.

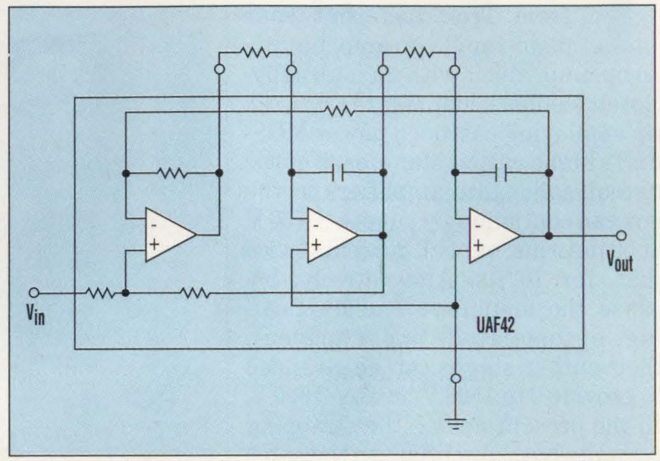
The next model of the 50/750, which will let one amplifier swing from 0 to –1500 V while the other swings to +1500 V when connected in a bridge circuit, will be able to produce peak-to-peak voltages of 3000 V across a load. However, generation of sine waves will take a little care.

Because they're dedicated, closed-loop amplifiers, linearity (Trek calls it dc accuracy) is specified. At the maximum (manually set) gain, it runs to within less than 0.5%. However, since the gain control is within the feedback loop, decreasing gain increases loop gain, which in turn improves linearity. Gain and offset temperature coefficient run 50 ppm/°C and 250 μV/°C, respectively. In addition to gain and offset, front-panel screwdriver adjustments enable the user to adjust the circuit's damping and response characteristics to best handle a particular input signal, load, and gain.

With a TTL-compatible input on the Model 50/750, an external logic signal, or relay, can turn the amplifiers on and off. The Model 50/750 is rated for operation from 0 to 40°C at a relative humidity of 75%. Its dimensions are 8.5-in. wide, 5.8-in. high, and 17-in. deep. It weighs 17 pounds. In unit quantities, it goes for $2495 each.

Trek Inc., 3932 Salt Works Rd., Medina, NY 14103; Lorna Finch, (716) 798-3140. **CIRCLE 470**

CONTINUOUS-TIME FILTER IC HAS ON-CHIP 0.5% CAPACITORS, COMES WITH FILTER-DESIGN SOFTWARE



To avoid the aliasing and noise problems of switched-capacitor IC filters, many designers are returning to continuous-time IC filters, like Burr-Brown's UAF42 universal active filter. Capable of implementing virtually any common filter topology, it beats one of the problems typically encountered with earlier continuous-time active filters—getting accurate capacitors.

The UAF42 filter IC contains a pair of 1000-pF oxide capacitors that have been trimmed to within 0.5% accuracy. As a result, you need only add two external resistors in order to build a two-pole Chebyshev low-pass filter *(see the figure)*. Its circuit represents an example of the classic state-variable architecture with an inverting amplifier and two integrators.

It can also be used for Sallen-Key, low-pass designs. The fourth (uncommitted) of the chip's four FET-input op amps (not shown) can be used in more complex filters. Because the gain-bandwidth and open-loop gain of the op amps run 4-MHz typical and 90-dB minimum, respectively, useful filters with cutoff frequencies ranging up to 100 kHz can be readily built.

Typically, Q factors of 400 and Q-frequency products of 500 kHz can be achieved. Input voltage noise typically runs less than 25 $nV/\sqrt{Hz}$ at 10 Hz and less than 10 $nV/\sqrt{Hz}$ at 10 kHz. Broadband noise from 0.1 to 10 Hz typically runs under 2 μV pk-pk.

The chip is supported by free, menu-driven filter-design software on a floppy disk in addition to 28 pages of application notes. The basic device is rated for the extended-industrial-temperature range. Mil-grade devices are also available. Packaged in a 14-pin plastic DIP, the device's pricing starts at $6.95 each in quantitites of 100.

***Burr-Brown Corp.**, P.O. Box 11400, Tucson, AZ 85734; John Conlon, 1-800-548-6132 or their electronic bulletin-board service through a modem at (602) 741-3978 (300/1200/2400 8,N,1).* **CIRCLE 471**

■ *FRANK GOODENOUGH*

SMART-POWER ICs DRIVE AUTO MULTIPLEX LOADS

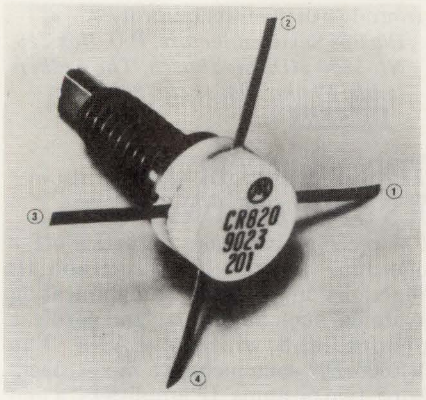
Two smart-power ICs are designed for automotive multiplex wiring systems and set new records for current handling. The most powerful is the L9936 half-bridge that delivers up to 25 A, allowing window-lift motors to be directly driven for the first time. The L9936 is assembled in an 8-lead version of the company's Multiwatt plastic power package, a version with 0.1-in. lead spacing to suit high current tracks on circuit boards. The other device is the L9937, a 6-A full-bridge. It comes in an 11-lead version of the Multiwatt package. In a typical auto multiplex scheme, the L9936 is used for high current loads (such as window-lift motors), while the L9937 drives various other motors, such as headrest adjustment motors or doorlock actuators. Typically, the power ICs are used with a custom control and interface circuit because the protocols are proprietary.

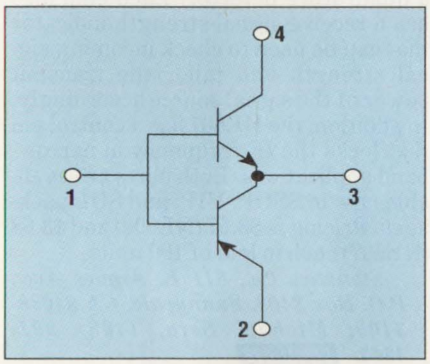
Available now, the L9936 and L9937 power ICs sell for $5 each in quantities of 100 or more.

SGS-Thomson Microelectronics Inc., 1000 E. Bell Rd., Phoenix, AZ 85022-2699; (602) 867-6228. **CIRCLE 472**

NPN/PNP PAIR HANDLE HIGH-VOLTAGE VIDEO

If a complementary pair of transistors is needed that can put ±50 V, or even higher-voltage video waveforms across 1000 Ω, while connected as emitter followers, Motorola's CR820 could be the answer. The npn transistor has a collector-to-base breakdown voltage, $V_{(BR)CBO}$, between pins 1 and 4 of 120 V. Its pnp cohort's $V_{(BR)CBO}$ runs –80 V between pins 2 and 3. Collector-emitter breakdown voltages run 70 and –65 V, respectively. Cutoff frequencies f_T for both transistors run 1 GHz, while the current gain is 40 at a collector current of 50 mA.





Motorola RF Products Div., 325 Maple Ave., Torrance, CA 90503; Elden Young, (213) 783-5785. CIRCLE 473

EXCALIBUR YIELDS IMPROVED OP-27/OP-37S

Texas Instruments' Excalibur process has yielded improved second sources of the popular, standard, precision OP-27 and OP-37 op amps. The high-speed complementary process includes high-speed vertical pnp transistors that complement the fast vertical npns from the process. Called the TLE2027 and TLE2037, the op amps offer performance and features not previously available. While offset voltage is comparable with that of the OP-27 and OP-37 (25 μV maximum), input noise runs 35% lower. Operating with a source resistance of 100 Ω, premium-device noise runs a maximum of 4.5 $nV/\sqrt{Hz}$ at 10 Hz and 3.8 $nV/\sqrt{Hz}$ at 1 kHz. Peak-to-peak input noise from 0.1 Hz to 10 Hz is a maximum of 130 nV. The TLE 2027's small-signal unity-gain bandwidth and open-loop gain are also superior to that of earlier devices. The former runs a minimum of 9 MHz. Large-signal differential-voltage gain, while driving 2000 Ω with ±11 V, is typically over 150 dB, and a minimum of 132 dB. Driving 600 Ω with ±10 V, these drop to 145 dB and 126 dB, respectively. An added feature, called output-saturation recovery, prevents the output from saturating when the op amp is overdriven. The feature eliminates the usual recovery-time-from-saturation effects that can often mask signals for milliseconds in other op amps. In quantities of 1000, the op amps start at $1.19 each.

Texas Instruments Inc., Semiconductor Group (SC-91047) P.O. Box 809066, Dallas, TX 75380-9066; (800) 336-5236, ext. 700 or (214) 995-6611, ext. 700. CIRCLE 474

FAST OP AMPS FEATURE 1.8-MHZ BANDWIDTHS

Low-power requirements combined with optimized speed and high precision are the hallmarks of a new family of single, dual, and quad op amps. The MC3317x family offers a high bandwidth of 1.8 MHz and a fast slew rate of 2.1 V/μs. It uses a bipolar process with pnp transistors in the differential input stage. The input common-mode range extends down to the lower supply rail, allowing single-supply operation even with supply rails as low as 3 V. The upper limit is 44 V. All three devices need supply currents of only 200 μA/amplifier. The Darlington input stage provides high input resistance, low input offset voltage, and high gain. The amplifier output stage does away with the conventional npn/pnp configuration, using an all-npn stage instead. This approach brings an increased output-voltage swing, a high-current sink, and better high-frequency performance. In quantities of 1000, the MC33171 single op amp, MC33172 dual op amp, and MC33174 quad op amp each sell for 46, 50, and 60 cents, respectively.

SGS-Thomson Microelectronics Inc., 1000 E. Bell Rd., Phoenix, AZ 85022-2699; (602) 867-6228. CIRCLE 475

V.32 DATA PUMP HEADS FOR LAPTOPS

For modem applications in portable and laptop computers, the WE DSP16A-V32 data pump comprises the 16-bit fixed-point DSP16A, the T7525 linear codec, and an interface controller. The ROM-coded DSP16A-V32 implements V.32 (9600-baud) and slower-speed standards by receiving and transmitting data, performing echo cancellation, and automatically selecting the highest data rate available in a given modem transaction. Located on the telephone-line side of the data pump, the T7525 linear codec has 12-bit linearity for 60 dB of echo cancellation, and serves as the analog front end. The data-pump controller provides an internal universal synchronous/asynchronous receiver-transmitter (USART), programmable-host interface, user registers, clock separation and control, and V.13 and V.54 support. The combined chips provide V.24, microprocessor-bus, eye-pattern, and line interfacing. Typical power consumption is 450 mW; 50 mW in power-down mode. Pricing is $70 per set in quantities of 10,000.

Call AT&T Customer Response Center; 1-800-372-2447; or write to AT&T Microelectronics, Dept. 52AL300240, 555 Union Blvd., Allentown, PA 18103. **CIRCLE 476**

RS-422/23 TRANSCEIVER IC SIMPLIFIES BOARDS

One of the first CMOS transceiver chips to include RS-422 drivers and receivers in the same package, the Startech ST86C87, is pin-compatible with the recently-released transceiver chip developed by Motorola Inc. Two differential drivers and two differential receivers are integrated on one chip. Because most systems typically only need two channels, one ST86C87 can replace two quad driver and receiver packages. However, for applications that need more than two channels, the company also has the ST26C31 and ST34C87 quad differential line drivers, and the ST26C32 and ST34C86 differential receivers. These chips are also direct replacements for the Quad drivers and receivers developed by National Semiconductor Corp. In lots of 1000, all of the Startech drivers, receivers, and transceivers sell for about $3 per chip.

Startech Semiconductor Inc., 1101 S. Winchester Blvd., No. A101, San Jose, CA 95128; (408) 247-8781. **CIRCLE 477**

HYBRID AMPLIFIERS WORK AT UP TO 2 GHZ

Satellite TV and cellular-radio receivers operating at up to 2 GHz can now use hybrid wideband amplifiers to replace discrete versions in the IF stages. The OM926 and OM956/2 amplifier modules work between 10 MHz and 2 GHz and between 950 MHz and 1750 MHz, respectively. Featuring low noise and high output levels, the amplifiers can also be used in high-frequency measuring equipment. The OM926 is a two-stage amplifier with a sloped gain of 15 to 18 dB over the 950-to-1750-MHz range to compensate for cable-transmission losses. The module has an output level of 103 dBμV at –60-dB intermodulation distortion. The noise figure is 6.5 dB. The device is encapsulated in a 5-pin single-in-line package. The OM956/2 is a three-stage module encapsulated in a plastic package suitable for surface mounting. It has 24-dB gain that's flat to within ± 1 dB. The output level is 114 dBμV at intermodulation distortion of –35 dB. Both thin-film amplifiers work from 12 V, have a matched impedance of 75 Ω, and return losses of 12 dB. Available now, the OM926 costs about $4 and the OM956/2 around $6 in medium quantities.

Philips Semiconductors, P.O. Box 218, NL-5600 MD, Eindhoven, The Netherlands; Phone: (0031) 40-722091. **CIRCLE 478**

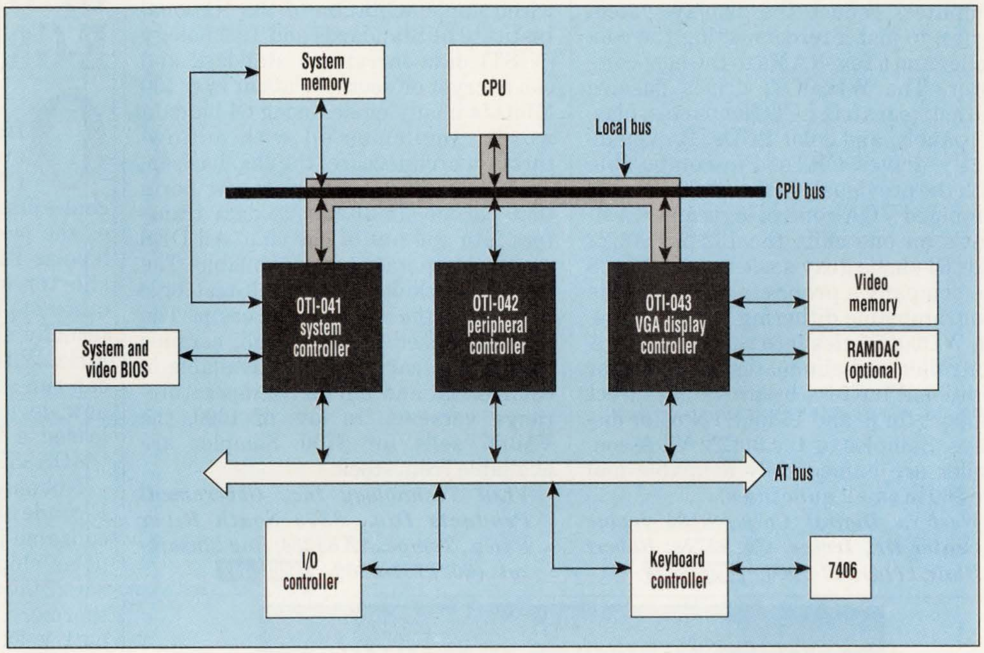
TINY FM RECEIVER ICS OPERATE ON 3 V

FM receiver ICs from Signetics offer one-chip solutions for mixer and IF functions in portable communication systems, such as cellular and cordless phones, and wireless LANs. The NE606/607 each include a mixer/oscillator, two op amps, IF amplifiers, a limiter amplifier, a voltage regulator, and a quadrature detector. Each chip also has a receive-signal-strength indicator that can be used to check incoming signal strength and tailor the transmit power of the signal source accordingly. In addition, the NE607 has a control pin that locks the IF frequency in narrowband applications. Both parts are available now in SSOP, DIP, and SOL packages. Pricing is $3.57 (NE606) and $3.68 (NE607) each in lots of 100 units.

Signetics Co., 811 E. Arques Ave., P.O. Box 3408, Sunnyvale, CA 94088-3409; Michael Sera, (408) 991-4544. **CIRCLE 479**

Three-Chip Set Compresses Laptop Logic And Video Control

Dave Bursky



The quest for smaller and lower-power notebook computers has pushed logic integration close to its limit with the release of the OakNote chip set from Oak Technology. The three-chip set consists of a system controller, a peripheral controller, and a VGA display controller—the OTI-041, 042, and 043, respectively. All three chips communicate with each other and with either an 80286 or 80386SX CPU and main memory over a local bus rather than over the AT-bus, which was used in most previous system implementations. Using a local-bus interface for the display controller greatly improves the display performance because the display subsystem can run at CPU clock rates rather than at the AT bus rate. That also eliminates the synchronization and bandwidth constraints of the AT bus.

Providing all system memory and AMA control logic for 80286- and 80386SX-based systems, the OTI-041 can be used to implement systems that run at clock speeds from 8 to 20 MHz. Also integrated on the chip are the bus controller (with local bus support for the VGA controller), the AT-bus address buffers, and all address and data-path control circuits. Clock and Reset-generation logic, along with fast Reset and GateA20 support, were also included on the chip. Working with the system controller, the 042 peripheral controller combines power-management circuitry with the standard peripheral devices (interrupt controller, I/O and chip-select logic, real-time clock with 128 bytes of RAM, and 287/387SX coprocessor support) and support for the Intel 82385SX cache controller.

The VGA controller can simultaneously drive the flat-panel display and a CRT (with an optional RAMDAC). Separate timing circuits are included on the chip for both display types. Fully VGA compatible, the controller can provide standard VGA resolution of 640 by 480 pixels, or deliver the enhanced 800-by-600-pixel mode with 64 gray-scale levels on the flat-panel display, and 256 colors on a CRT. An on-chip page-mode data buffer and a command buffer enable the chip to take full advantage of the local-bus interface. DRAM configurations of 256k-by-4 and 64k-by-16 are supported by the controller chip. The VGA chip can also be used in systems that don't employ the entire OakNote chip set. For those applications, the OTI-043 can tie into the standard AT-bus architecture.

Combining the three control chips onto a motherboard requires an area of less than 34 in.^{2} for a system with 1 Mbyte of DRAM. The additional logic that must typically be added to round out the system include an I/O controller that provides the serial and parallel ports, floppy-disk controller, an IDE hard-disk interface, some serial-port buffers, one 7406 TTL chip, the keyboard controller, some crystals, a video-clock generator, and the various memories (DRAMs for main memory and the video memory, and a BIOS EPROM or ROM).

Power-management features implemented as part of the chip set logic include activity monitors that track interrupts, keyboard activity, serial-port usage, as well as programmable I/O pins, and an automatic wake-up capability.

The OTI-041 and 043 come in 160-lead plastic quad-side flat packages, while the 042 comes in a 144-lead version of the same package. Samples of the chips are immediately available. In 1000-unit lots, the OTI-41/42 chip pair sells for $56/set, and the OTI-043 sells for $43 each in similar quantities. Oak has also developed an extended-memory-manager driver and a comprehensive system BIOS. Work is also underway with several other BIOS suppliers to provide additional BIOS options.

Oak Technology Inc., 139 Kifer Ct., Sunnyvale, CA 94086; William Wong, (408) 737-0888. **CIRCLE 480**

VIDEO CONTROLLER TRIMS PC CHIP COUNT

A VGA-compatible display controller and companion color-LCD panel support chip will help laptop and notebook computers reduce the display-system design to just interconnecting the controller and a few RAMs to the host computer. The WD90C22 drives passive and active matrix LCD flat panels, plasma panels, and color LCDs. It even directly drives CRTs. Pin-compatible with the previously released 90C20 that combined VGA control logic and RAMDACs on one chip, the 132-pin 90C22 adds 64-shade gray-scale imaging, with the company's proprietary TrueShade programmable dithering logic. The 44-pin WD90C55 ties into the 90C22 VGA controller and eliminates the need for additional buffers by providing direct support for 8- and 16-bit STN color displays. Samples of the 90C22 VGA controller are immediately available and are $60 in small quantities.

Western Digital Corp., 8105 Irvine Center Dr., Irvine, CA 92718; Robert Blair, (714) 932-5000. CIRCLE 481

DATA-ENCRYPTION IC CIPHERS 190 MBITS/S

The VM007 provides designers with a complete programmable cryptographic system on a chip. It contains a hard-wired implementation of the National Institute of Standards and Technology (NIST) data-encryption standard and can encrypt or decrpyt data at over 190 Mbits/s in any mode, using 64-bit data words. Implemented with a flow-through architecture, the chip has separate plain-text and cipher-text ports that permit simultaneous data transfers into and out of the chip. All DES modes of operation are available. The chip also includes built-in self-test logic that tests the chip at power-up. The chip is housed in an 84-lead, ceramic leaded chip carrier and is available in commercial and military temperature-range versions. In lots of 1000, the VM007 sells for $750. Samples are available from stock.

VLSI Technology Inc., Government Products Div., 8375 South River Pkwy., Tempe, AZ 85284; Ray Slusarczyk, (602) 752-6300. CIRCLE 482

CMOS PLDs MATCH SPEED OF BIPOLAR E-GRADE

Offering the shortest input-to-output delay of any 24-bit CMOS programmable-logic chip—just 7.5 ns—the 85C224-7 matches the performance of E-grade 24-pin bipolar PLDs. The new Intel chip has shorter input-to-output delays than other 24-pin CMOS PLDs and can be internally clocked at rates of up to 100 MHz. With external feedback, the chip can run at 74 MHz. In addition to this new device, the company also has released a 7.5-ns version of the 20-pin CMOS 85C220.

Not only are the chips as fast as their E-grade bipolar counterparts, they also consume just half the power of the bipolar chips. At maximum speed, the 85C224 draws 105 mA maximum. Furthermore, because the chips are based on UV EPROM cells, windowed-package versions can be erased and reprogrammed. In contrast, once a bipolar chip is configured, it can't be reprogrammed.

The 85C224 PLD contains eight I/O macrocells, up to 22 inputs (14 dedicated and 8 programmable I/O lines), and has some features that aren't included on other 24-pin PLDs. The 85C220-7 device can have up to 18 inputs (10 dedicated and 8 programmable I/O lines). Each of the I/O macrocells contains eight product terms as well as an individual output-enable P-term, plus a programmable inversion option. All of these features are in addition to the basic macrocell, which consists of an EX-OR input to a D-type register and various configuration switches to select the output source, and the routing of the input signal.

In addition to the chips, an enhanced version of the free PLDshell PLD design software has also been released by the company.

Prices for the 85C224-7 and 220-7 are $10 and $6.10 each, respectively, when purchased in 1000-unit lots (windowless plastic leaded-chip-carrier version). Delivery for both programmable devices is from stock.

Intel Corp., *Literature Packet IP-82, P.O. Box 7641, Mt. Prospect, IL 60056-7641; (408) 765-8080.*

CIRCLE 483

■ *DAVE BURSKY*

Gate-Array Family Boosts I/O Line Count

By employing a double pad ring with staggered pads, the HG62G family of gate arrays gives users a higher I/O line-to-gate-count ratio than any previous family offered by Hitachi. Fabricated in a 0.8-μm CMOS process, the arrays have from 15 to 35 kgates arranged in a channel-free array. However, by staggering the I/O pads in two rings and tightening the pitch between I/O pads, the company was also able to reduce the chip size of each new array by 40 to 60% over a chip fabricated with a standard single pad ring. The smaller chip size (and thus lower cost), high I/O count, and higher performance position the family well for high-performance I/O-intensive applications.

There are four masterslices in the HG62G series whose gates on the chips are interconnected with two levels of metal wiring. The arrays have raw gate counts of about 14,500, 19,500, 27,500 and 34,800, and respective I/O pad counts of 160, 184, 216, and 240. Internal gates have propagation delays of just 450 ps, typical, and a power dissipation of about 9 μW/gate/MHz (for a 2-input NAND with a fan-out of 2 and 2-mm of metal). Even shorter delays are possible for special "power" gates. I/O buffers have an output delay of about 1.8 ns, typical, with a 50-pF load, and input buffers have an 800-ps delay when loaded by 2 mm of metal and with a fan-out of 2. Buffer output drive levels can be selected as 2, 8, 16, or 24 mA. The arrays are characterized for 5-V operation over a temperature range of –20 to +75°C.

In addition to the basic cells included in the library, the company has a RAM compiler slated for release in early 1992 to custom-create memory blocks. To simplify chip testing, the company also has some scan-type auto-diagnostic functions that can be selected from the cell library and incorporated in the system design. Plastic quad-sided flat packages for the 62G series chips will range in lead count from 64 to 208 pins, with higher pin counts expected in 1992. Initial array prices range from 7 to 10 cents per I/O line in lots of 10,000.

***Hitachi America Ltd.,** Semiconductor and IC Div., 2000 Sierra Point Pkwy., Brisbane, CA 94005-1819* **CIRCLE 484**

■ *DAVE BURSKY*

Megabit SRAMs Trim Access Time To 17 ns

A family of five 1-Mbit static RAMs with access times as short as 17 ns give designers x1, x4, and x8 word-width options, as well as single or dual Chip Enables or common or separate I/O lines. The first three standard offerings, the EDI88128CSA, 84256CSA, and 811024CSA, consist of a 128-kword-by-8-bit unit, a 256-kword-by-4-bit device, and a 1-Mword-by-1-bit device, respectively. The 128 k by 8 is available in two versions: the first is the standard device with one Chip Enable, the other has two Chip Enable lines (the EDI88130CSA). In addition, the 256 k by 4 comes in two versions. The standard version has multiplexed data-input and data-output lines, and the second has separate data-input and output lines (EDI 84285CSA). All of the chips will be housed in 400-mil DIPs or SOJ packages and will be available in speed grades from 17 to 35 ns. Prices for the 17-ns chips are $221 each in 100-unit lots, while 35-ns versions sell for $64 each. Samples are available from stock.

Electronic Designs Inc., 42 South Street, Hopkinton, MA 01748; Mark Hampson, (508) 435-2341. **CIRCLE 485**

HIGH MAGNIFICATION BRINGS THERMAL ANALYSIS TO FINE PITCH

Thanks to the addition of a magnification-lens option, the Compix 6000 thermal-imaging system can detect and analyze "hot spots" on electronic components with feature sizes as small as 2 mils (0.002 in.). As a result, the system is well-suited for fine-pitch, small-geometry component applications, such as those found in semiconductors, hybrid circuits, and multichip modules.

Because nearly all of the power supplied to a circuit appears as heat in some location, the Compix 6000 system helps zero in on the thermal weak points in a design. Often, semiconductor devices are the hottest spots in a circuit. The system bypasses bulky thermocouples and contact probes, which are often too large and may provide misleading readings because they serve as heat sinks themselves. In addition, contact probes may become elements of hybrid, RF, or stripline circuits and skew performance.

The magnification lens provides a vertical field view of 0.4 by 0.5 in. and magnification power of 7.5X. The option also includes a camera stand and x-y-z positioners that allow the device being examined to be positioned relative to the lens. Without the lens option, basic system resolution is 15 mils.

With the lens, designers and manufacturers can conduct component-level reliability testing and design verification. Also, they can perform component failure analysis and thermal inspection of design prototypes. Using the COM6 software package, a PC can be used for off-line storage, analysis, and comparison of thermal images previously captured by the 6000 system.

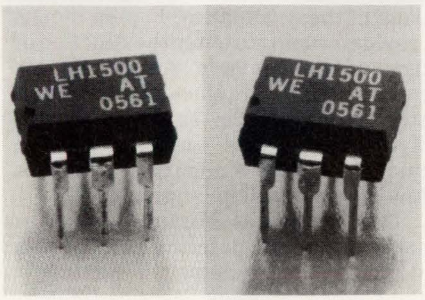
The basic price of the Compix 6000 thermal-imaging system with the COM6 software is $18,500. The magnification-lens option package brings the price to $28,500. Existing systems can be retrofitted to add the magnification package.

Compix Inc., 16195 S.W. 72nd St., Tigard, OR 97224-7766; (503) 639-1934. **CIRCLE 486**

■ *DAVID MALINIAK*

SOLID-STATE RELAY FAMILY OFFERS UP TO 3750-V ISOLATION

By meeting or exceeding domestic and international standards for input-to-output isolation, the LH1500 family of solid-state relays makes its case for being one of the most complete lineups of relays rated at 1 A or less. With isolation ratings of up to



3750 V rms, the relays pass FCC 68.302 and other regulatory voltage-surge requirements when coupled with overvoltage protection. The 21-product family continues the market trend toward replacing electromechanical relays with smaller, faster solid-state types. This trend, as exemplified by the LH1500 line, extends to applications in telecommunication, modems, security equipment, programmable controllers, instruments, and industrial controls.

Among the 21 models are the most common relay forms: normally open (1 Form A), normally closed (1 Form B), and various combinations, such as 1 Form A/B/C, 2 Form A, dual Form A, and dual Form B.

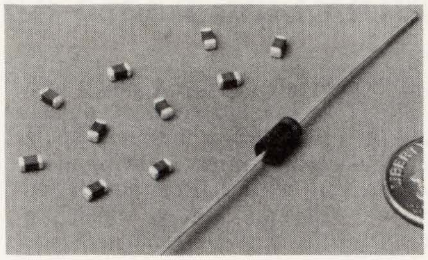
Within the relays, a GaAlAs diode is used for actuation control and an integrated monolithic die provides the switch output. The BCDMOS die contains a photodiode array, various switch-control circuits, and DMOS switches. The Form A/B relays include break-before-make circuitry, which eliminates extra timing logic.

In lots of 1000, the relays range in price from $2.60 for a 1 Form A to $4.75 for a dual 1 Form B. Samples are available now with production quantities shipping in the fourth quarter.

AT&T Microelectronics, *Dept. 52AL040420, 555 Union Blvd., Allentown, PA 18103; (800) 372-2447.* **CIRCLE 487**

■ *DAVID MALINIAK*

MLC SURGE SUPPRESSORS PROTECT LOGIC CIRCUITS

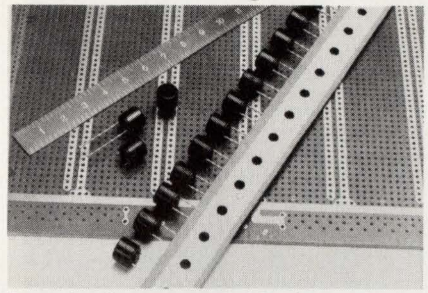


Maximum continuous-voltage ratings from 3.5 to 68 V dc are now available in the ML series of surface-mounted transient voltage suppressors. With 10 new multilayer ceramic devices, the series extends transient protection to logic-level circuits (3.5 to 5.5 V), automotive (14 to 18 V), computer communication (26 V), and telecommunication line cards using high-voltage circuits (33 to 68 V). Typical pricing is 40 cents in lots of 100,000. Delivery is from stock.

Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901; (800) 4-HARRIS, ext. 1135. **CIRCLE 488**

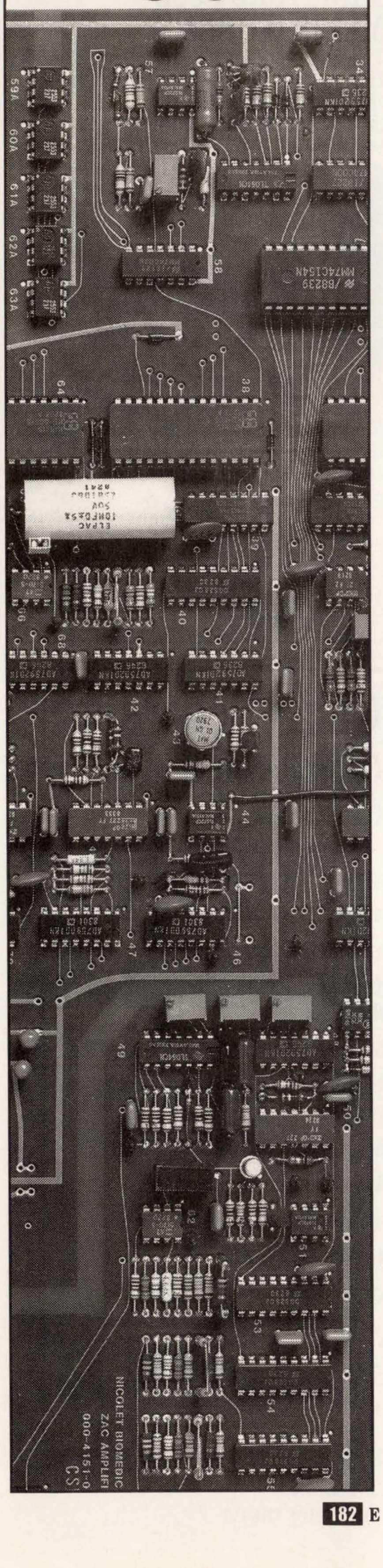
MINIATURE FUSE MEETS IEC SPECS

The gap between export versus domestic circuit protection is narrower thanks to the MSF 250 microfuse. The device combines IEC blowing characteristics with UL recognition. Short or



long leads are available for pc-board mounting. Current ratings range from 50 mA to 5 A with a breaking capacity of 35/50 A at 250 V. A 1-A fuse costs 28 cents in lots of 1000. Delivery is from stock to eight weeks.

Schurter Inc., P.O. Box 750158, Petaluma, CA 94975-0158; (707) 778-6311. **CIRCLE 489**

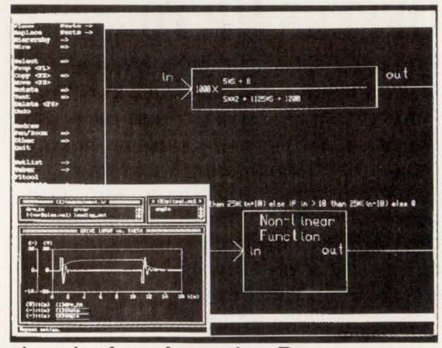


GRAPHICAL DESIGN CAPTURE AND MODELING EASES ANALOG DESIGN

Designers using Analogy's Saber simulator can now quickly create schematics and simulation models in a graphical environment. At the core of the graphical environment is Design Capture, which provides menus, drawing commands, and output formats tailored to the needs of analog designers. For example, designers using the schematic product don't need to know a wide range of layout, packaging, and pin requirements, which are long-standing obstacles to quick creation of analog-circuit schematics. In addition, voltages and values created during simulation are back-annotated to the schematic for easy access and viewing.

Design Capture is an enhanced version of a commercial schematic-capture program. Its menus provide access to stimulus definition and common analog simulation analyses, such as dc-operating-point, transient, and frequency analysis. Symbol libraries cover Analogy's range of simulation models, including electrical parts, mechanical elements, and control blocks. Users can access the Saber simulator directly. In addition, the Analogy system works with other systems, such as those of Mentor Graphics and Cadence Design Systems, by exporting and importing symbols and drawings through the company's graphical EDIF interface.

Another new tool, Graphical Model Generator, eases the creation of simulation models. Users can enter functions without having to translate them into a modeling language. They choose symbols from the menus of Design Capture to place components or functions in the schematics. Pop-up menus provide a means to enter the function of those components in standard math equations. The Graphical Model Generator translates the equations into a MAST model and automatically includes it in the simulation. MAST is Analogy's modeling language.



The Graphical Model Generator helps designers describe components in three modeling domains, the time, s, and z domains. They describe time-domain models using non-linear and piece-wise differential functions, and enter the model equations in the s- and z-domains directly as rational polynomials. Time- and s-domain functions appear on the schematic next to their symbols. The resulting circuits can represent both conservative (electrical) and control (signal flow) circuits.

Analogy's new environment, including Design Capture and Graphical Model Generator, will be available by the end of this month on Unix workstations. Pricing starts at $1950.

***Analogy Inc.**, 9205 S.W. Gemini Dr., Beaverton, OR 97005; (503) 626-9700.* **CIRCLE 490**

■ *LISA MALINIAK*

TOOLKIT CUSTOMIZES PROCESS MANAGEMENT

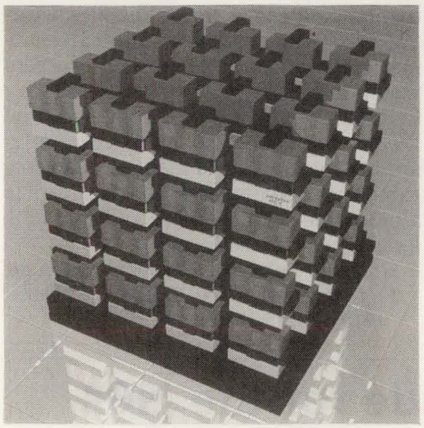
Project managers can customize process-management functions in TeamOne System's TeamNet concurrent-engineering environment with the company's Process Automation Kit (PAK). PAK enables users to automate the flow of information between work groups, project leader, and corporate management. Engineers use object-oriented data and process modeling to customize the TeamNet environment with reusable process modules. They can construct applications, such as a navigation system that tracks development processes and determines the next steps required to build or release a product. The kit can automate processes, like sign-off requests, at each release level and dependency management. In addition, PAK can be used to develop software that automatically generates bills of materials and build procedures. It can configure programs that relate cost and part data from MRP databases to the current design. PAK will be shipping by the end of the year. One kit will support an entire development group, and will cost $45,000. The price also includes five days of on-site training.

TeamOne Systems Inc., 710 Lakeway Dr., Sunnyvale, CA 94086; (408) 730-3500. **CIRCLE 491**

TRANSPUTER-BASED SYSTEM MAXES OUT AT 400 GFLOPS

Up to 400 GFLOPS of performance can be supplied by the GC System, from Parsytec Inc., using from 64 to 16,384 T9000 transputers. The massively parallel computer is suitable for such applications as climatic research and detailed long-term weather forecasting, drug design, and fluid dynamics.

Each T9000 transputer contains a 32-bit integer processor, a 64-bit floating-point unit, a 16-kbyte cache memory, a communications processor, and four communication links. The transputer can reach levels of 200 MIPS and 25 MFLOPS.



The GC System is designed with a cluster-based multiple-instruction multiple-data (MIMD) architecture. Each cluster contains 17 transputers equipped with error-protected memory and four C104 wormhole routing chips. The system's building block is formed from 16 nodes, while the 17th node supplies processor redundancy to ensure a backup in the event of a node failure.

Communications between clusters is done through six data streams that offer a 3D interconnection among clusters. The data streams consist of 8 T9000s to supply a throughput of 200 Mbytes/s. Prices for a GC System start at $250,000 per GFLOP. Shipments will begin in the first quarter of next year.

***Parsytec Inc.**, 245 W. Roosevelt Rd., Bldg. 9, Unit 60/61, West Chicago, IL 60185; (708) 293-9500.* **CIRCLE 492**

■ *RICHARD NASS*

REMOVABLE HARD DRIVE HOLDS 90 MBYTES

Combining a 19-ms access time with a rugged, crash-resistant design, the Bernoulli 90 is a 90-Mbyte removable hard-disk drive that can transfer data at 20 Mbits/s. Higher linear-density recording is achieved by incorporating metal-particle media and metal-in-gap heads. A higher rotational speed and a high-performance head-actuator system are responsible for the quick access time. That time could further be cut to 13 ms by taking advantage of caching software. The drive comes with 32 kbytes of cache memory. An automatic head-cleaning feature eliminates periodic cleaning, resulting in longer life and more reliable operation (60,000-hr MTBF). Four configurations of the Bernoulli 90 are available: two 5-in., half-height internal drives, an ac-powered transportable unit, and a dual system with two drives in one case. The drives are completely read compatible with lower-capacity Bernoulli 44 drives. All are available now. Prices run from $999 to $2249.

Iomega Corp., 1821 W. 4000 South, Roy, UT 84067; (801) 778-1000. **CIRCLE 493**

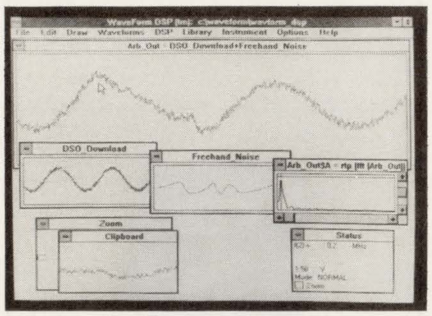
SPARC WORKSTATIONS FILL OUT LOW END

Two systems have been released to extend and enhance Solbourne's desktop product line: the S4000DX and the S3000. The former is an enhancement of the S4000 workstation, designed with a 256-kbyte second-level cache memory to accelerate compute-intensive electronic-design applications. The S3000 is a full-function transportable system that incorporates a 16-in. monochrome plasma display that offers fast, CRT-like interaction. Weighing just 25 lbs. and having a footprint of 18 by 7 in., the S3000 can be carried to remote locations. A range of configurations are available. A system containing 8 Mbytes of system memory, a 500-Mbyte hard disk drive, and a 3-1/2-in. floppy drive sells for $14,995.

The S4000DX boasts performance specifications of 28.3 MIPS and 18.3 SPECmarks. The system operates at 36 MHz and offers a 256-kbyte second-level cache memory. Moreover, both workstations are 100% Sparc compatible. S4000DX systems start at $9995.

Solbourne Computer Inc., 1900 Pike Rd., Longmont, CO 80501; (303) 772-3400. **CIRCLE 494**

TOOOLKIT CREATES, EDITS, ANALYZES WAVEFORMS



WaveForm DSP is a digital-signal processing toolkit that allows PC users to capture, create, edit, or analyze waveshapes on the PC screen and then upload digitized versions to an arbitrary waveform generator. Users can create waveforms by any combination of drawing, mathematical expression, downloading from a digital oscilloscope, or inserting a waveform from a 20-function library. Once created, waveforms can be added to the library for reuse. WaveForm DSP lets users manipulate, combine, or compare waveforms in the graphical Windows 3.0 environment.

The waveforms can be created, as well as edited, in the frequency or time domain. A waveform's frequency content is able to be viewed, analyzed, and edited, and then the waveform can be converted to the time domain with only a mouse click on a pull-down menu. WaveForm DSP costs $895, with delivery in 4 to 6 weeks.

Wavetek San Diego Inc., 9045 Balboa Ave., San Diego, CA 92123; (800) 874-4835 or (619) 279-2200. **CIRCLE 495**

DIGITAL OSCILLOSCOPE TESTS VIDEO SIGNALS

The ODFA digital oscilloscope is intended for the quality control of video signals in TV studios, and on TV transmitters and receiving systems. Easy to operate because of softkey-controlled menus, the instrument is used for the display and automatic analysis of video signals, as well as for individual measurements using cursors. The ODFA is a 10-bit signal analyzer for high-precision DSP and high-speed analysis. It features various automatic test routines required for commissioning and quality control of TV transmitters and receiving systems.

The individual signals can be displayed on the flicker-free screen with high resolution (1/1000 of the display height and width). Thanks to digitization of the test signals with subsequent storage and numerical processing, the instrument offers many advantages, such as: noise elimination from test signals by averaging; a no-parallax graticule that is free from geometrical distortion; tolerance mask display; storage of displays with text and scales; numerical correction of inherent errors when used as a sweep video display unit; cursors for timing, amplitude and frequency-response measurements; automatic analysis of video test-line parameters, and display of parameters in alphanumeric form. Price and availability are given on request.

Rohde & Schwarz, D-8000 Munich 80, P.O. Box 80 14 69, Germany; Phone: (0049) 89 4129-2625. **CIRCLE 496**

RUN VGA GRAPHICS 30X FASTER

A family of high-resolution PC graphics boards, with speeds up to 30 times faster than nonaccelerated VGA graphics controllers, is available for designers of high-performance graphics systems. The GA2000 family comes with drivers for Microsoft Windows 3.0, Presentation Manager 1.2 and 1.3, AutoCAD Release 11, X-Windows for Interactive Systems Architect Series, and the Santa Cruz Operation's Open Desktop. The boards support PC/AT and Micro Channel buses and are configured with a minimum of 512 kbytes of VRAM. Resolutions of 1024 by 768 and 1280 by 1024 pixels with 16 or 256 colors are available, along with refresh rates up to 72 Hz in the noninterlaced mode. The 16-color, 1024-by-768-pixel board sells for $795 and is available now.

Spectragraphics, GSS Personal Graphics Div., SW Gemini Dr., Beaverton, OR 97005; (503) 641-2200. CIRCLE 497

BOARD LETS MAC SOFTWARE RUN ON A PC

Using Andor One, a PC add-in board, IBM PC users can run Apple Macintosh software on their PCs. The board is compatible with all types of PCs, from XTs to 486 models. Users switch between PC and Mac modes by simultaneously pressing both shift keys on the PC's keyboard. Once the board is installed, peripherals like the keyboard, mouse, video display, and hard and floppy disks can be accessed from the Mac software. In addition, the PC's floppy drive can directly read from and write to Mac disks. The board contains an AppleTalk-compatible RS-422 connector so it can be linked directly to an Apple Laserwriter, LocalTalk, Phonenet, or other networking device. The accompanying software occupies about 60 kbytes of the PC's RAM. The board is available now and sells for $995.

Hydra Systems Inc., 1340 South Saratoga-Sunnyvale Rd. No. 106, San Jose, CA 95129; (408) 253-5800. CIRCLE 498

MINI PCBS ALLOW INNOVATIVE PACKAGES

Using miniature modular pc boards, Dover Electronics has come up with an innovative method of packaging a 386SX-based computer. The technique could be used for a notebook PC, an embedded-control system, or some other type of mass-market computer. The company's Smart SIM CPU cards fit into a custom backplane in a three-dimensional fashion. The standard board size is 5.2 by 1.7 in. and can be stacked in the backplane on a 0.5-in. pitch. Custom sizes are available. The boards come with a 386SX processor, on-board VGA support for either LCDs or CRTs, an internal power supply, controllers for floppy and hard-disk drives, from 2 to 16 Mbytes of RAM, one serial and two parallel ports, and keyboard and mouse controllers. Additional modules offer support for a network interface, a modem, or a SCSI port.

Dover Electronics, 1198 Boston Ave., Longmont, CO 80501; (303) 772-5933. CIRCLE 499

TOUGH SEMICONDUCTORS

Details on the GEC Plessey line of radiation-hard and silicon-on-sapphire (SOS) integrated circuits are described in a 700-page data book. Products covered in the data book include RAMs up to 64 kbits, logic, 1553 protocol devices, 29XX bit slice parts, and a range of MIL-STD 1750A microprocessors and peripherals. The company also offers SOS ASICs with up to 30,000 available gates.

Marconi Circuit Technology Corp., 160 Smith St., Farmingdale, NY 11735; (516) 293-8636, ext. 596, Dale Wilson. **CIRCLE 500**

POWER COMPONENTS

The latest catalog of electrical power components from Schurter Inc. gives details on such parts as fuses, fuse holders, connectors, power entry modules, and voltage selectors. It includes details on the company's recently acquired line of Feller PCC components, which enhances Schurter's offerings with 1-to-20-A IEC 320 inlets, outlets, plugs, snap-in and chassis-mounted filtered power-entry modules, and the Felcom series of modular power-entry modules for custom configurations.

Schurter Inc., P.O. Box 750158, Petaluma, CA 94975-0158; (707) 778-6311. **CIRCLE 501**

SWITCHMODE RECTIFIERS

Details on the electrical specifications, operating characteristics, and design benefits of the TwinPack line of switchmode rectifier systems are presented in a 23-page condensed catalog from Power Conversion Products. The company is a manufacturer of power-conversion equipment and systems for the telecommunications market. Among the covered products are system status and control panels, low-voltage disconnect panels, digital equalize panels, fuse panels, fuse alarm panels, bus bars, dc-to-ac static inverters, dc-dc converters, ringing generators, battery trays, relay racks, and a microprocessor monitor.

Power Conversion Products Inc., P.O. Box 380, Crystal Lake, IL 60014; (815) 459-9100, Chris Seyer. **CIRCLE 502**

PC BOARD DESIGN

The P-CAD line of products for the computer-aided design of printed-circuit boards is described in a six-page brochure from Cadam. Among the covered products are schematic capture software; a symbol library; analog and digital simulation tools; automatic, interactive, and analytical placement tools; and routers. The brochure explains how the P-CAM line of integrated tools helps ensure design integrity with effective engineering-change-order processing and complete design-rule checking.

Cadam, 1935 N. Buena Vista St., Burbank, CA 91504; (408) 971-1300, Ray Turner. **CIRCLE 503**

POWER CONVERSION

A very broad line of dc-dc converter modules, ac-dc power supplies and modules, benchtop and handheld calibrators, and miniature digital panel meters are described in a 148-page catalog from Datel. The catalog also includes a tutorial article on modern power-supply principles and practices, which gives details on some of the most recent innovations in power converter design.

In addition to describing over 170 power-conversion products, the catalog provides a complete overview of Datel's other products, which include data converters, data-acquisition systems, IBM PC/XT/AT analog and digital I/O boards, software, and printers.

Datel Inc., 11 Cabot Blvd., Mansfield, MA 02048; (508) 339-3000. **CIRCLE 504**

CONTRACT MANUFACTURING

A 12-page booklet from Philips Industrial Electronics Company (PIEC), a supplier of contract manufacturing services, helps users decide whether using a contract manufacturer makes sense for a particular application. It also gives advice on selecting a contract manufacturing company, and suggests what performance criteria to build into a contract with that company. In addition, the booklet discusses how to define and document procedures ahead of time, how to audit a contract manufacturer, and the pricing of contract manufacturing services.

Philips Industrial Electronics Co., 813 S. Grandstaff Drive, Auburn, IN 46706; (219) 925-8700. **CIRCLE 505**

CORRECTIONS

Two Product Features in our July 25 issue had their photographs switched. The stories were "Modular Power Supplies Offer Broad Flexibility" on page 168, and "Data-Acquisition Boards Eliminate Aliasing" on page 175. Also, on p. 53 in the Electronic Design Report, incorrect pricing was provided for the Harris HV1205 and HV2405 switching-regulator ICs. In quantities of 1000, the former goes for \$1.50 each (not \$2.55), and the latter for \$1.88 each (not \$2.93).

In the June 27 issue, p. 154, the New Product story for Micro Networks Inc. listed the wrong telephone number. It should have been (508) 852-5400.

VIDEO OPTICS

The 1991 Video Optics Guide is a 70-page full-color catalog on the Zoom 6000 Video Microscope and related products. It includes extensive applications information with illustrations, and tutorial information: brief notes, guidelines, and a glossary. The Zoom 6000 is an optical lens system that connects to a video camera and television monitor to provide magnifications from 6.9X to 1350X. Working distances range from 1.5 to 12 inches.

D.O. Industries Inc., 200 Commerce Dr., Rochester, NY 14623; (800) 828-6778 or (716) 359-4000. **CIRCLE 506**

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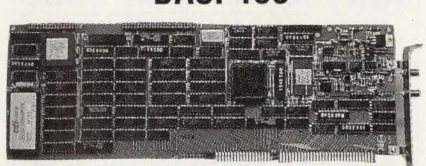

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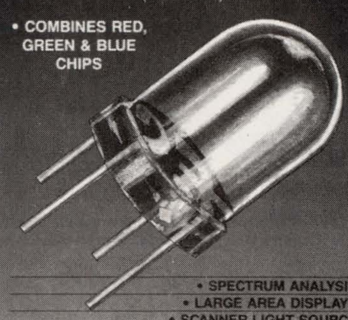

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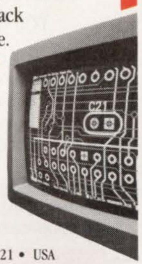

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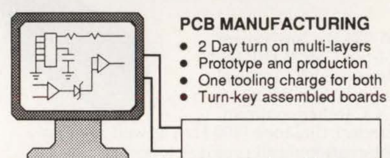

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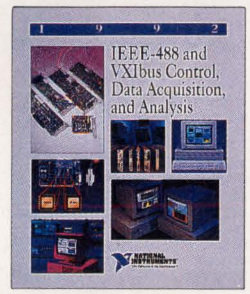

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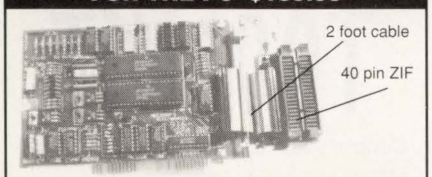

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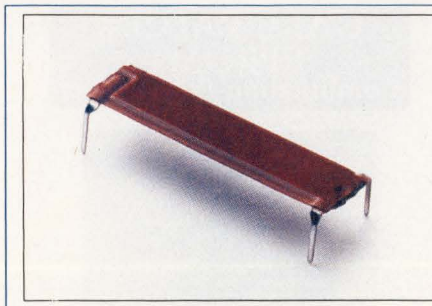

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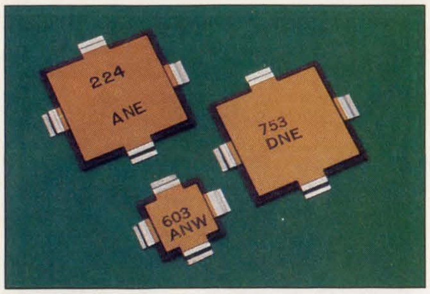

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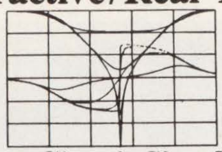

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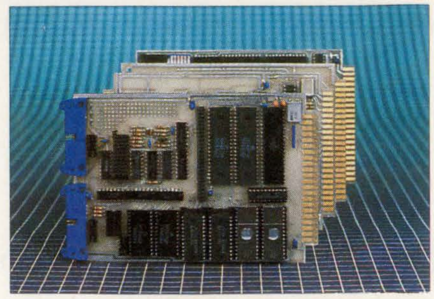

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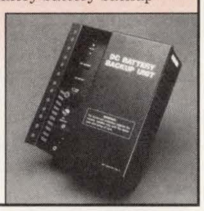

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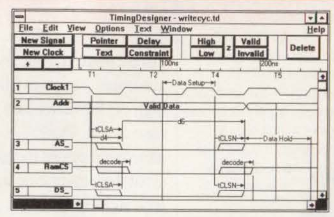

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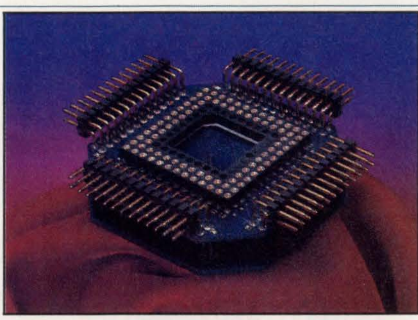

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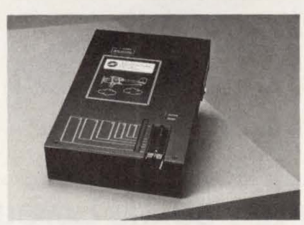

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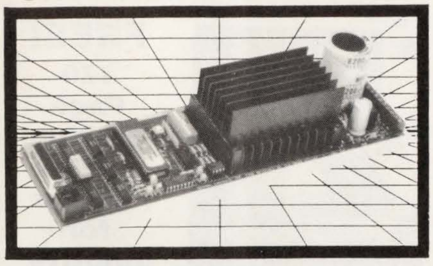

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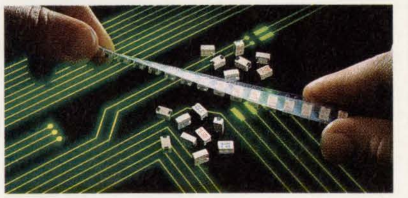

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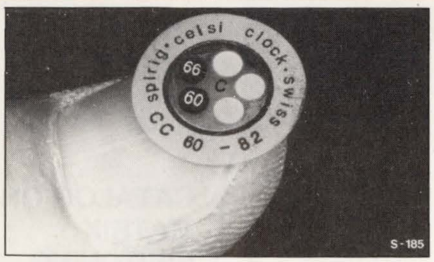

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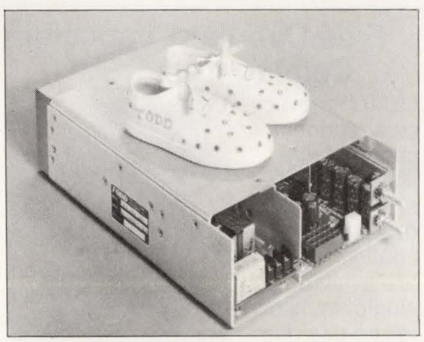

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