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FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

ELECTRONIC DESIGN®

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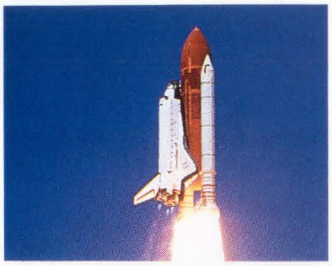
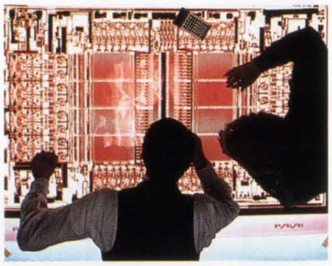
APRIL 11, 1991

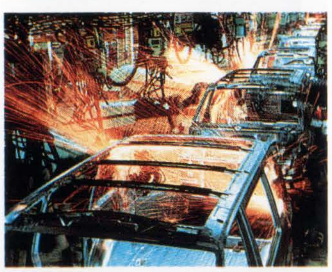
A NEW ANALOG BUILDING BLOCK: GROUND

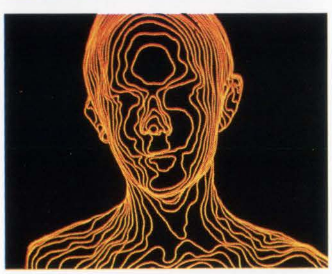
•SPECIAL REPORT: HIGH-RESOLUTION ADCs

•CAD DESIGNERS' GUIDE TO PC BOARDS









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CIRCLE 152

Extraordinary disc drives require extraordinary parts.

H N O L O G Y

Today's disc drives are smaller in size and larger in capacity than ever before due to advances in component technology. By designing and manufacturing most of the components ourselves—a concept called vertical integration—we can control the technology, cost, availability and quality of these critical parts.

Technically speaking, no one builds more advanced thin-film discs and recording heads than Seagate. These core technologies help us put 3 gigabytes of storage in a box the size of a toaster. And because we design our own components, we can bring our new products to market faster.

Of course, a key consideration in building our own parts is the cost. By controlling the manufacturing process down to the component level, we can have a significant impact on the cost of our finished products. The end-result is a better value for the customer without sacrificing quality or performance.

In terms of availability, it's important to know that Seagate shipped over 7 million disc drives last year alone. With volumes like these, building our own components helps us avoid the parts shortages that often plague other disc drive manufacturers.

Most importantly, vertical integration allows us to maximize the quality of every component we produce. With the industry's most advanced equipment and testing techniques, we consistently turn out components and finished products that are beyond reproach.

Obviously, it takes an extraordinary capital investment to pursue this strategy. But the disc drive companies who control their critical component production will be better able to control their own destinies, as well as those of their customers.

For more information on our complete line of high-performance disc storage products, contact your authorized Seagate distributor. Or call Seagate at 800-468-DISC, or 408-438-6550.

A COMMITMENT TO QUALITY

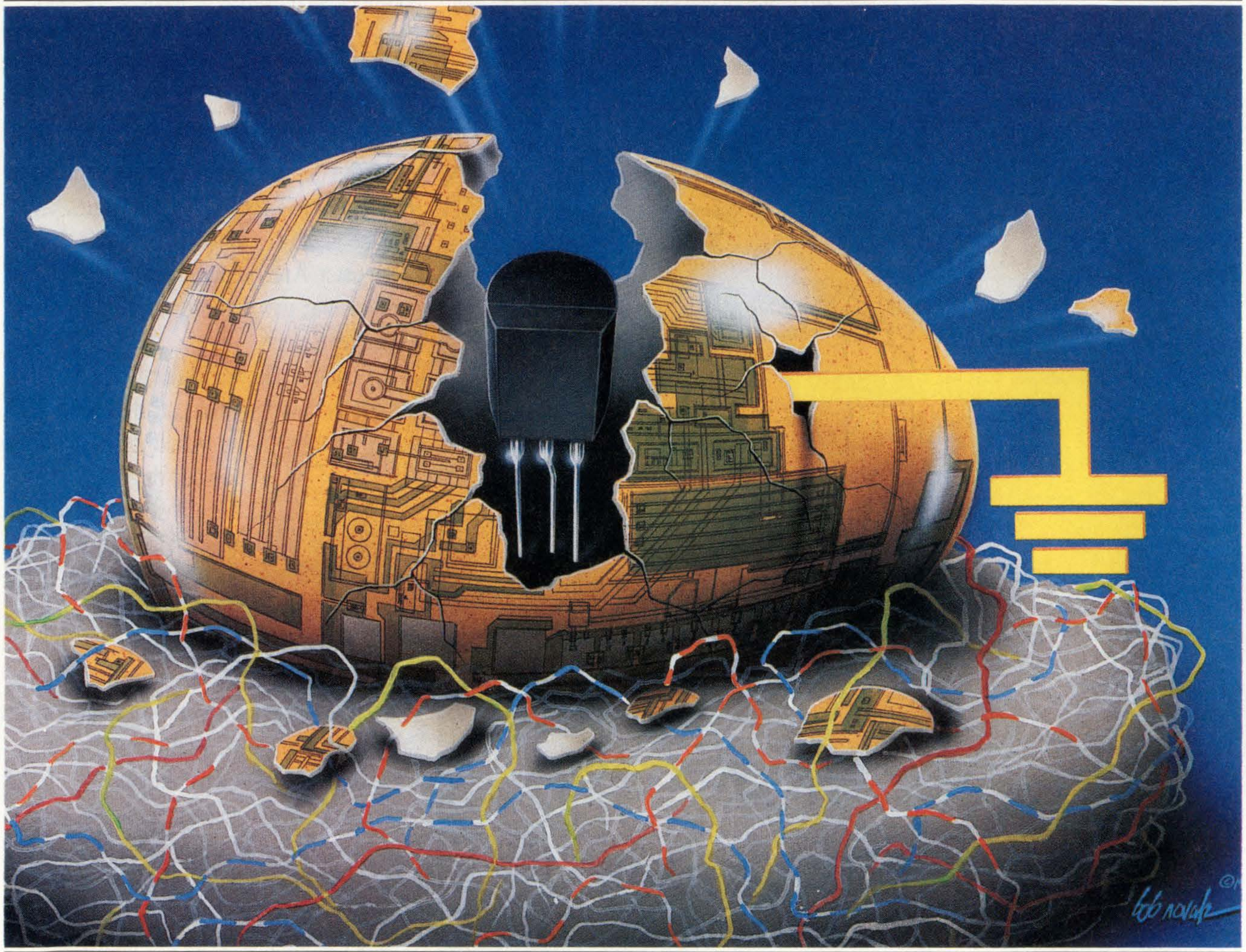
Seagate

The first name in disc drives

CIRCLE 97

APRIL 11, 1991 VOL. 39, NO. 7

ELECTRONIC DESIGN



Certificate of Merit
Winner, 1988
Jesse H. Neal Editorial Achievement Awards

Cover: Bob Novak

Correction: We goofed! On p. 35 in our Mar. 14 cover story, we incorrectly referred to Intel's 80960 microprocessor as an Intel 68020 microprocessor. Ed.

COMING NEXT ISSUE
- Special Report: The growing diversity in DRAM architectures
- Adapting terminals to ISDN data rates
- Using phase modulation to cut losses in large switching supplies
- 20-bit delta-sigma ADCs take on integrator applications
- Sea-of-gates arrays challenge standard-cell ASICs
- PLUS:

Pease Porridge
Ideas for Design
QuickLook
Technology Advances

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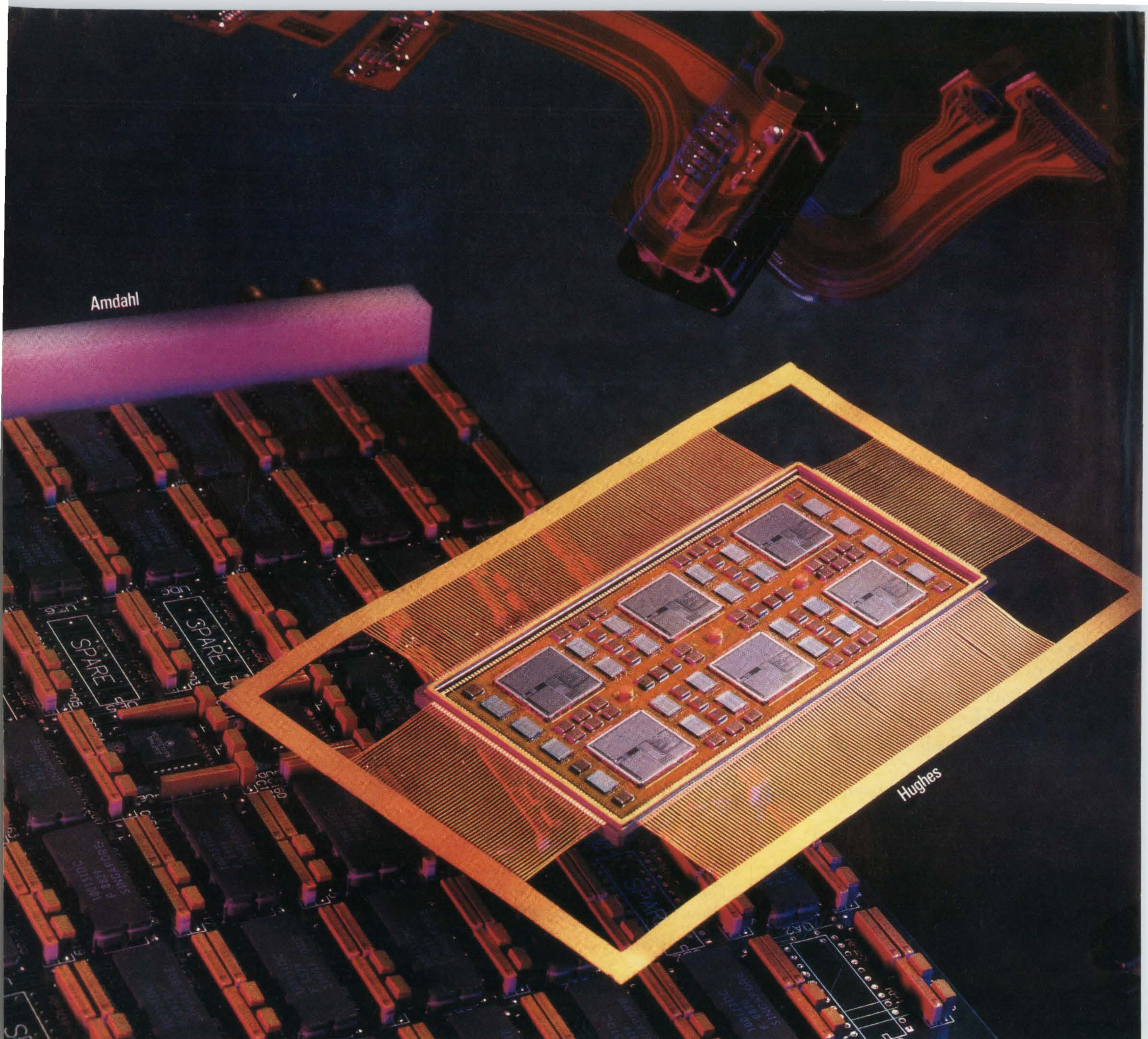


THE LEADERS IN PCB DE
WE SUPPLY

You're looking at some truly outstanding examples of advanced systems technology. PCB, hybrid, MCM. From some of the most prominent players in the electronics industry.

In each case, Mentor Graphics design tools helped leverage these complex board technologies into successful products:

A ten-layer ECL board from Amdahl with 1257 components and 1659 nets, each with a length or impedance constraint.

A board from Tektronix combining very high-speed digital and low-noise analog circuitry.

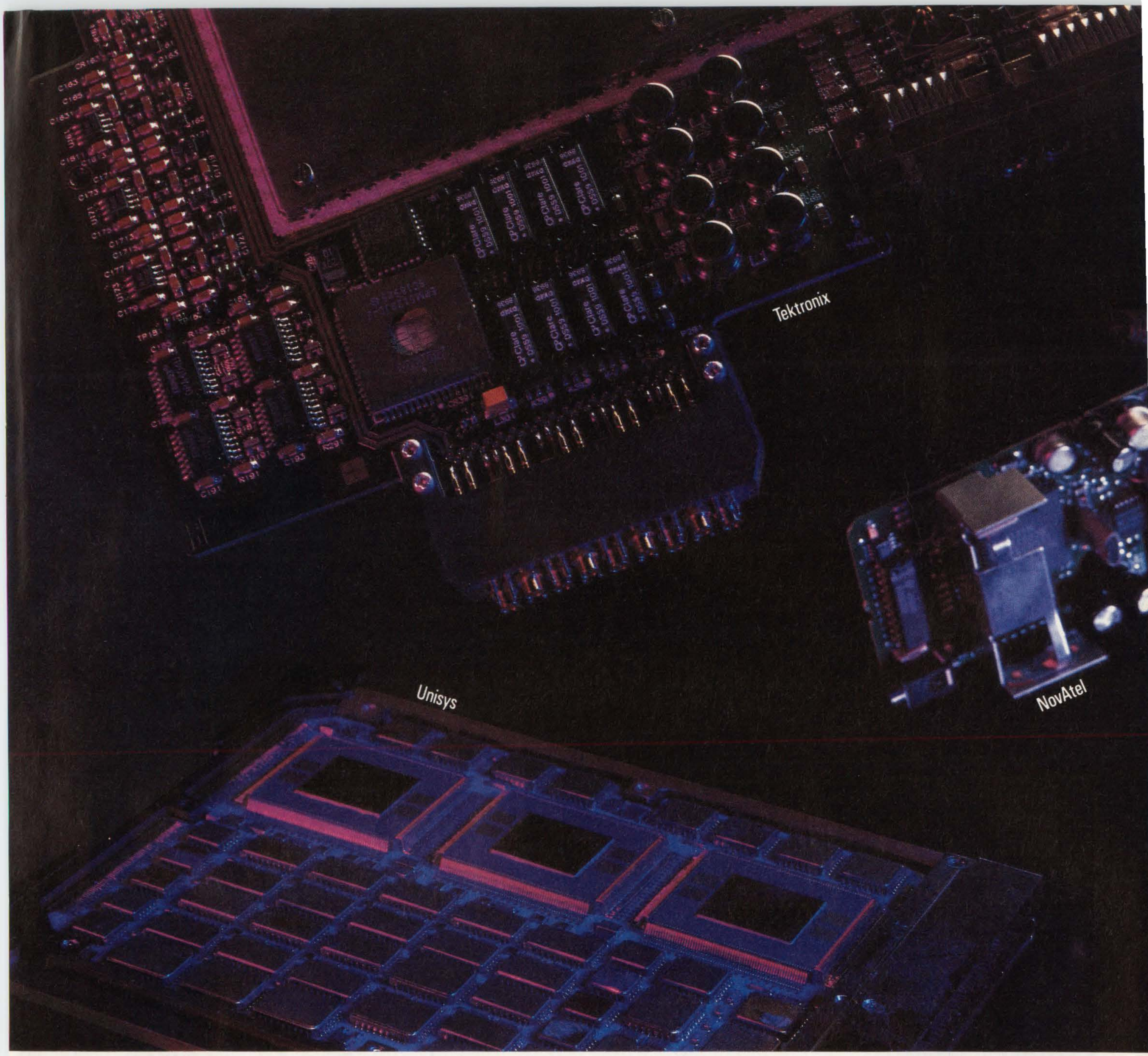
A PCB from NovAtel using chip-on-board (COB) technology for dramatic space savings.

A flexible circuit board from a major hard disk manufacturer with complex curved geometries.

A multi-chip module (MCM) from Hughes with 82 devices and 3300 interconnects on a 96x45 mm (3.8″ x 1.8″) silicon substrate.

A Mil-Std multi-layer ceramic module from Unisys that packs 57 chips and 2834 pins into a 6″x6″ space less than .6″ thick.

Each of these designs required superior engineering combined with superb tool technology. Precisely the kind of partnership



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you get with Mentor Graphics, the leader in design automation. We offer tools that span the entire bandwidth of electronics systems technology, from PCB to hybrid to MCM.

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But tools are only half the story.

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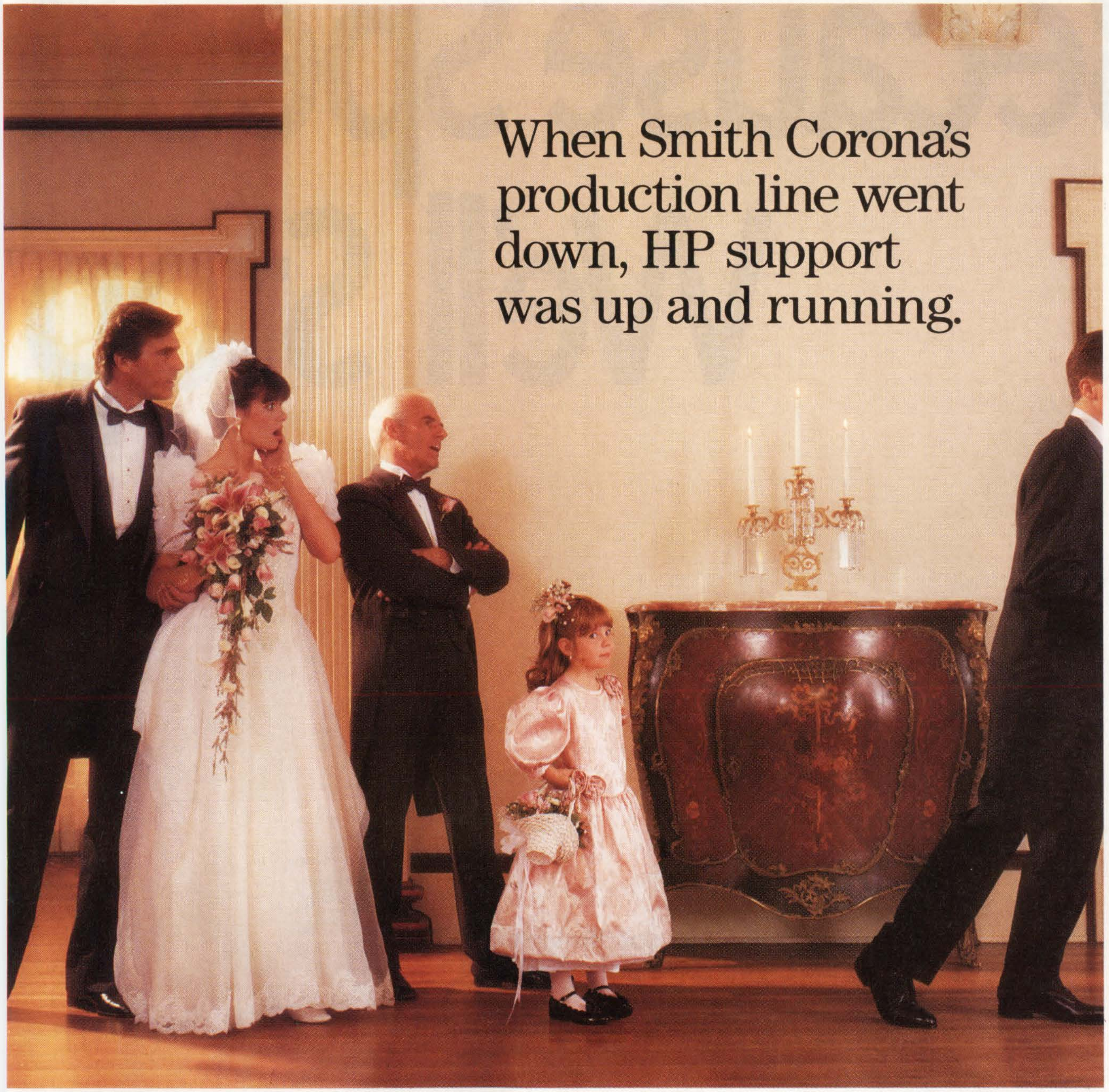

It happened on a freezing Saturday in February.

Joe Reiley, a Hewlett-Packard test and measurement support engineer, was at a wedding in Pottstown, Pennsylvania. The office was the furthest thing from his mind, when suddenly his beeper went off.

In minutes, Joe was on the phone to Travis Field, the support engineer for Smith Corona in Cortland, New York. An HP test system crucial to Smith Corona's production line had gone down. Suddenly, Joe's thoughts turned to figuring out how to get Smith Corona's production line back up. Joe bid the other guests goodbye and ran to his car.

After driving through a blinding snow storm over icy mountain roads, Joe pulled into Smith Corona at 10:30 pm. A thorough analysis of the problem made it clear they needed extra parts, so Joe called another HP support engineer, Pete Nahrgang, in Valley Forge. Working through the early morning, Pete took parts from a back-up HP system, then flew them to Cortland by special courier. By Sunday afternoon, just 24 hours after Joe's beeper first went off, Smith Corona's production line was up again.

True stories like this prove HP's dedication to responsive customer support throughout the world. We'll tailor our hardware, software and education services to your test and measurement needs. With one of the largest support organizations in the industry, we're committed to keeping your production line up and running. For more information, call your local HP sales office or circle the reader service number.

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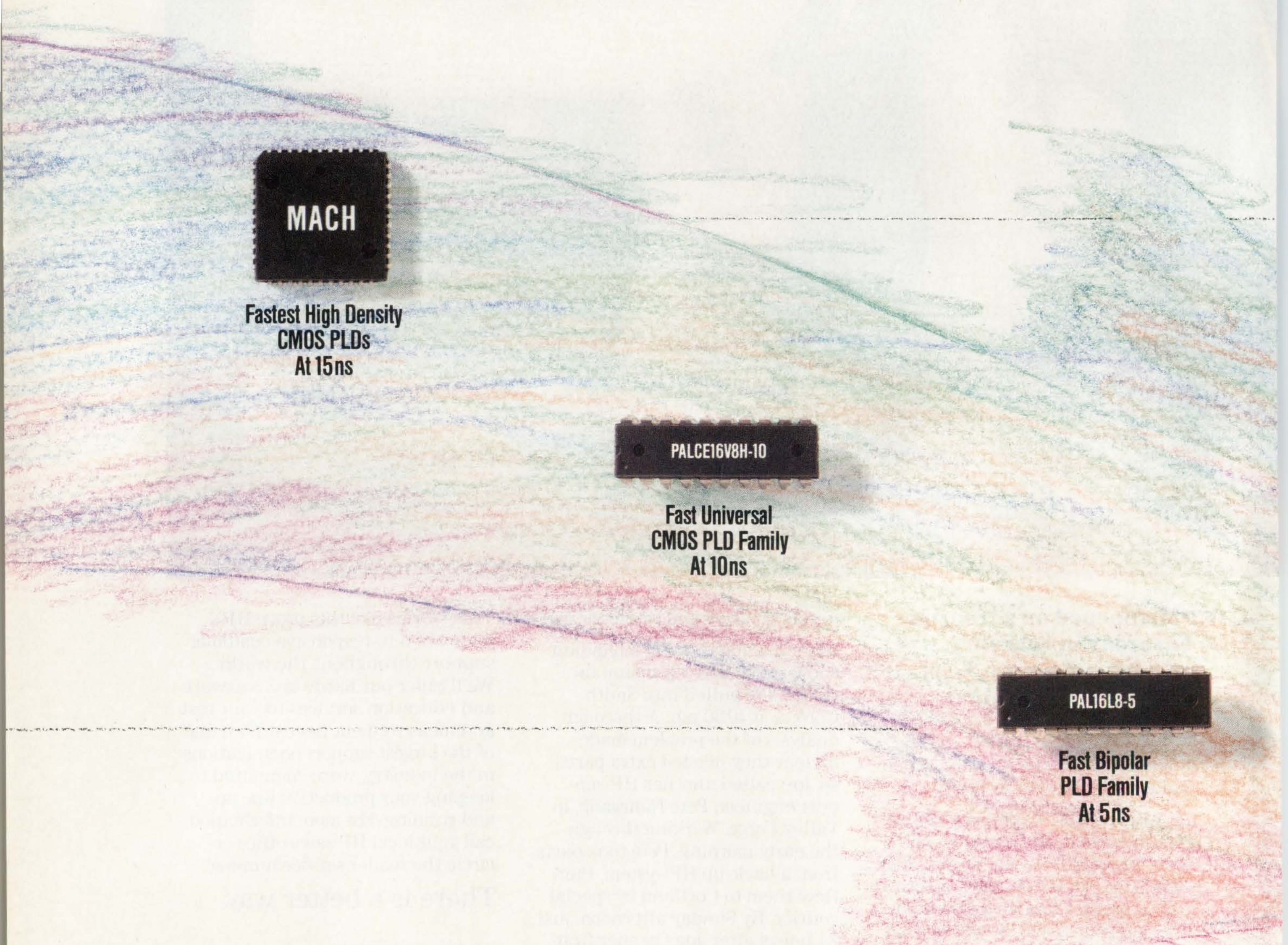
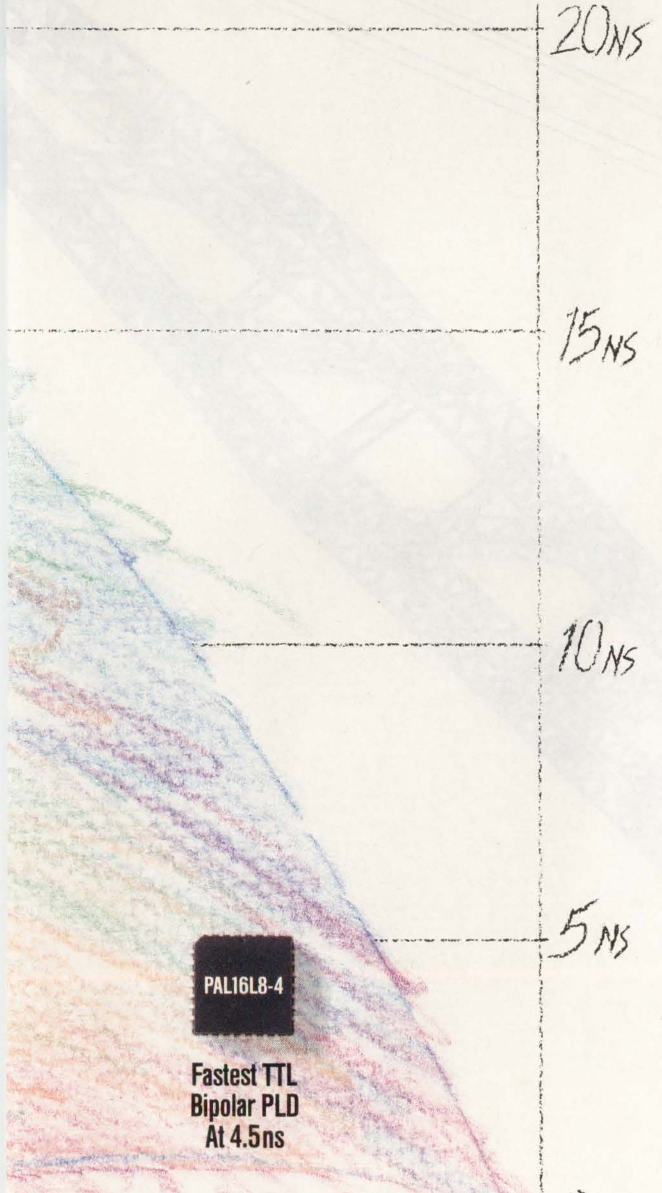
CIRCLE 168

Because Speed We'll Stop



Is Everything, At Nothing.



Whatever kind of PLD you need, the fastest comes from AMD.

We'd love it if all our work amounted to "zero." As in zero delay. And we're not far off.

Not surprising—because AMD invented the PAL® device. That's why we know programmables better. And offer you the most choices of the best devices.

Say you want speed, but can't sacrifice density. Don't. Use our new MACH™ products (Macro Array CMOS High-density) that give you up to 3600 gates and 15ns performance. They're two to three times faster than the competition and cost 40% less.

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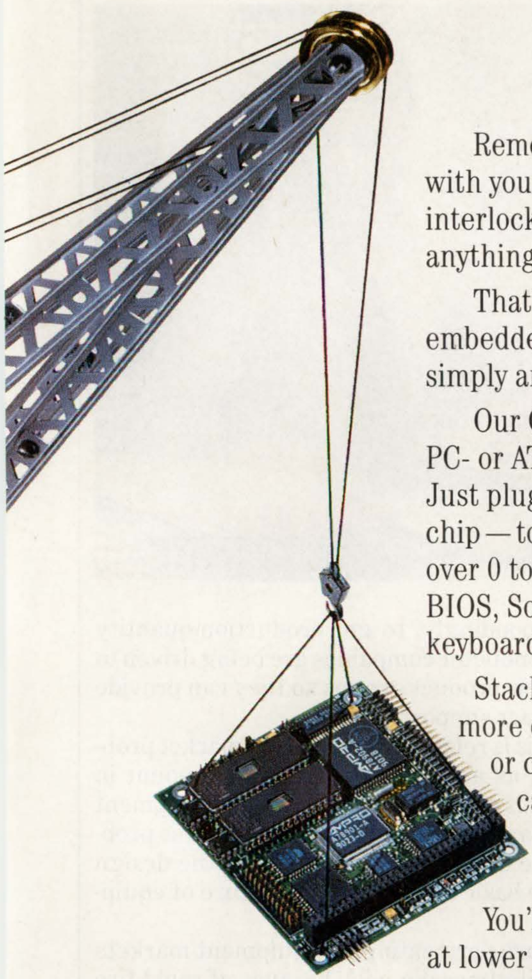
Advanced Micro Devices

CIRCLE 149

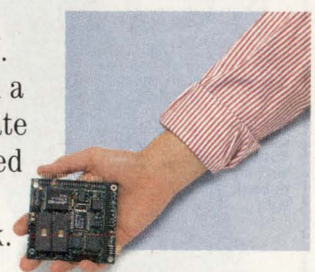
AMPRO'S EMBEDDED SYSTEM MODULE FAMILY

Introducing The Erector Set for Embedded Control Applications



Remember the challenge of constructing "engineering marvels" with your Erector® set? That red metal box held a complete set of interlocking pieces — all that was needed to assemble just about anything. Your imagination was the only limitation.

That's the idea behind Ampro's new way for OEMs to build embedded control applications. Put your application together, simply and quickly, using Ampro Embedded System Modules.



Our CoreModule™ family packs ready-made full PC- or AT-compatible intelligence into 3.6″ x 3.8″ x 0.6″. Just plug one into your circuit board — like plugging in a chip — to easily interface to your own logic. They operate over 0 to 70°C, and include a CMOS CPU, RAM, extended BIOS, Solid State Disk, serial and parallel I/O ports, keyboard and speaker interfaces, and a real-time clock.

Stack a CoreModule unit together with one or more of our expansion MiniModule™ peripherals (no backplanes or card cages needed). MiniModule products, also 3.6″ x 3.8″, can be used to add display controllers, more Solid State Disk capacity, network controllers, modem and facsimile features, additional I/O, and much more.

You'll get your product to market faster, with less risk, and at lower cost, because the CoreModule family is based on the most economical industry standard architecture. Now you can focus on the more challenging part of your system — the application itself.

Ultrasound monitors, point-of-sale terminals, robotics, network controllers — no matter what kind of "engineering marvel" you're building, you should be using Ampro's "Erector set" for your embedded control application.

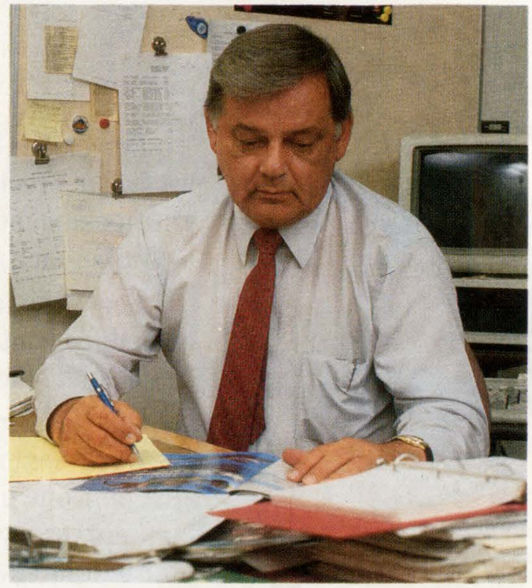
Call **1-800-966-5200.** Get the Information Kit on CoreModule and MiniModule products today.

AMPRO®

Pioneering Solutions for Embedded Control

CIRCLE 136

Ahead: Five Tough Challenges



Basic changes in technology, customer demands, and level of competition have hatched several challenges that are reshaping operations in the electronics industry. We at Electronic Design believe that these trends can be distilled into five major categories:

Designing with high-complexity parts: Designers cannot perform their jobs with just a sample and an application note any more—it simply takes too long to learn all of the subtleties of VLSI-device operation. Besides more powerful design-automation tools, designers will need more design support from semiconductor vendors. And, correspondingly, to get production-quantity deliveries in a reasonable time, semiconductor companies are being driven to reorganize and more tightly focus their product groups so they can provide those higher levels of designer-customer support.

Design for manufacturability: This is related to the time-to-market problem, but its importance to designers as a separate issue is paramount in today's equipment market. Little time is allowed in the product development process for iterations between design and manufacturing. To solve this problem, networked workstations must be deployed, the makeup of the design team should be changed, and even the basic organizational culture of equipment manufacturers must be altered.

Time-to-market: These pressures are permeating all equipment markets as competition heats up and product lifetimes diminish because of rapid-fire introductions of more powerful devices.

Quality: Total quality programs are also infiltrating electronics manufacturers as they attempt to achieve higher and higher standards of total customer satisfaction. For designers, this means more contact—more intense and meaningful contact—with potential customers than ever before.

Dealing with fewer vendors: As customers demand closer support from suppliers, they're cutting their lists of suppliers to manageable numbers. Costs of qualifying suppliers have also increased, leading to further reductions in their numbers. Another reason is that more VLSI devices are becoming single-sourced items. For designers, this means closer collaboration with those suppliers on their company's approved vendor list.

The impact of each challenge would be strong enough in itself. But add to their recent convergence a kicker: All of these challenges are being played out against a backdrop of global competition. Needless to say, there's a strong cause for concern. You'll hear more from us on these issues as we continue to address the needs of the renaissance design team—the theme we laid out in our January 10, 1991, Technology Forecast issue.

Stephen E. Scrupski, *Editor-in-Chief*

TINY SPDT SWITCHES
ABSORPTIVE...REFLECTIVE

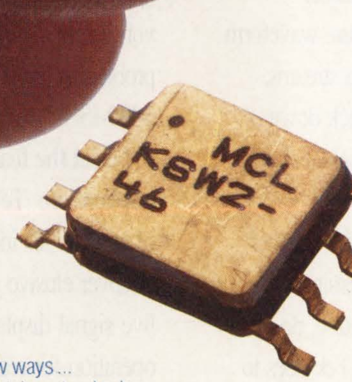
dc to 4.6GHz from $32.95 (10-24)

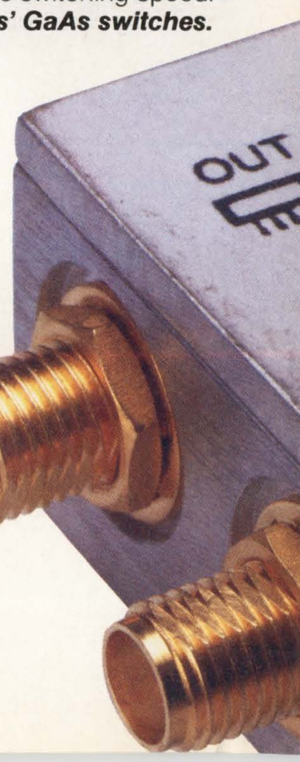
Tough enough to pass stringent MIL-STD-883 vibration, shock, thermal shock, fine and gross leak tests...useable to 6GHz...smaller than most RF switches...Mini-Circuits' hermetically-sealed (reflective) KSW-2-46 and (absorptive) KSWA-2-46 offer a new, unexplored horizon of applications. Unlike pin diode switches that become ineffective below 1MHz, these GaAs switches can operate down to dc with control voltage as low as -5V, at a blinding 2ns switching speed.

Despite its extremely tiny size, only 0.185 by 0.185 by 0.06 in., these switches provide 50dB isolation (considerably higher than many larger units) and insertion loss of only 1dB. The absorptive model KSWA-2-46 exhibits a typical VSWR of 1.5 in its "OFF" state over the entire frequency range. These surface-mount units can be soldered to pc boards using conventional assembly techniques. The KSW-2-46, priced at only $32.95, and the KSWA-2-46, at $48.95, are the latest examples of components from Mini-Circuits with unbeatable price/performance.

Connector versions, packaged in a 1.25 x 1.25 x 0.75 in. metal case, contain five SMA connectors, including one at each control port to maintain 3ns switching speed.

Switch fast...to Mini-Circuits' GaAs switches.





SPECIFICATIONS

Pin Model	**KSW-2-46**		**KSWA-2-46**	
Connector Version	**ZFSW-2-46**		**ZFSWA-2-46**	
FREQ. RANGE	dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (db)	typ	max	typ	max
dc-200MHz	0.9	1.1	0.8	1.1
200-1000MHz	1.0	1.3	0.9	1.3
1-4.6GHz	1.3	1.7	1.5	2.6
ISOLATION (dB)	typ	min	typ	min
dc-200MHz	60	50	60	50
200-1000MHz	45	40	50	40
1-4.6GHz	30	23	30	25
VSWR (typ) ON	1.3:1		1.3	
OFF	—		1.4	
SW. SPEED (nsec)				
rise or fall time	2(typ)		3(typ)	
MAX RF INPUT (bBm)				
up to 500MHz	+17		+17	
above 500MHz	+27		+27	
CONTROL VOLT.	-8V on, OV off		-8V on, OV off	
OPER/STOR TEMP.	-55° to +125°C		-55° to +125°C	
PRICE (10-24)	**$32.95** **$69.95**		**$48.95** **$79.95**	

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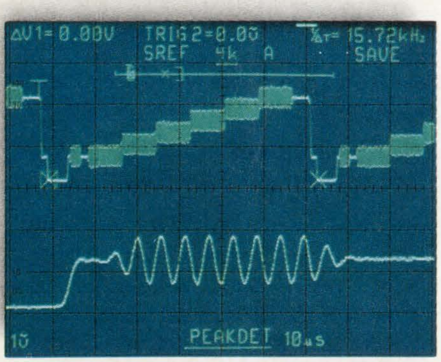
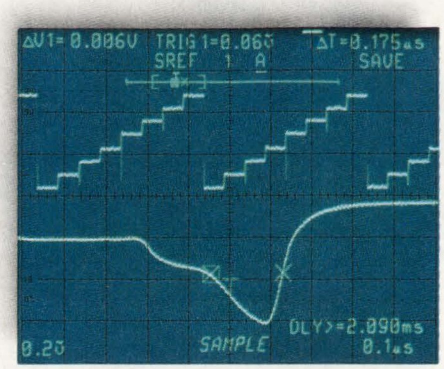
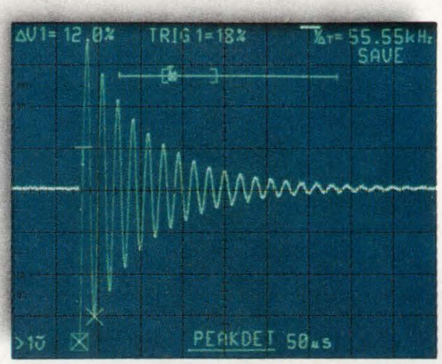
What's you



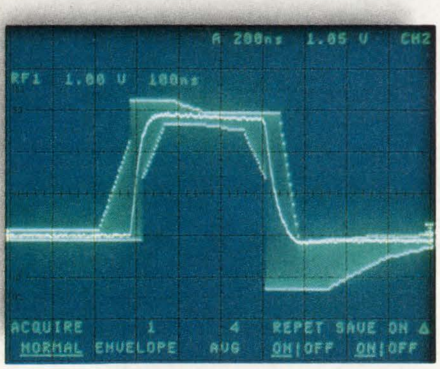
Analyzing TV and complex video signals?



Uncovering elusive glitches?

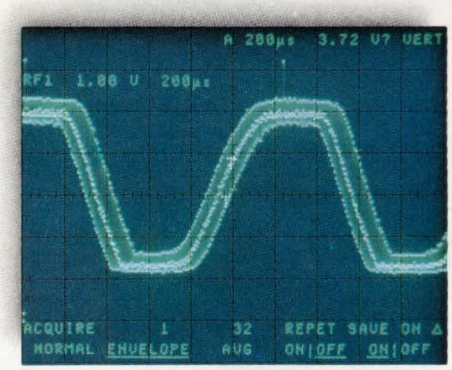


Capturing single-shot events?



Testing telecommunications signals?

Finding aberrations buried within a signal?



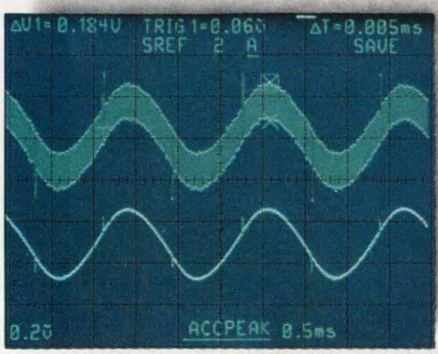
Automatic PASS/FAIL testing?

You can't depend on banner specs alone to solve problems like these. Whether you're trying to measure waveform parameters or analyze long data streams, identify infrequent events or track down glitches as narrow as 2 ns — there's all the difference between the depth of Tek troubleshooting and the trade-offs in other DSOs that compromise your results.

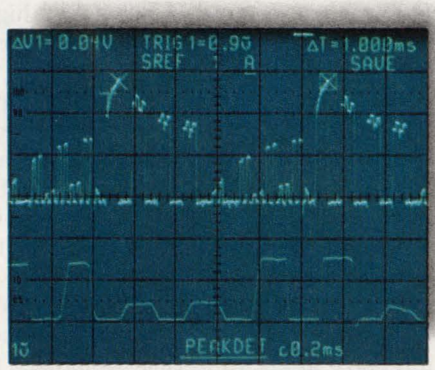
Spec for spec, feature for feature, no other company offers the credentials Tek does to effectively match DSO performance to your application needs. Whatever your criteria, you'll find a perfect solution in our line of problem-solving portable DSOs, from 10 to 500 MS/s.

Select the features to support your application. Tek DSOs offer a diverse set of capabilities including peak detect to uncover elusive glitches. Fast update rate for live signal display. Combined analog/digital operation for real-time verification of your

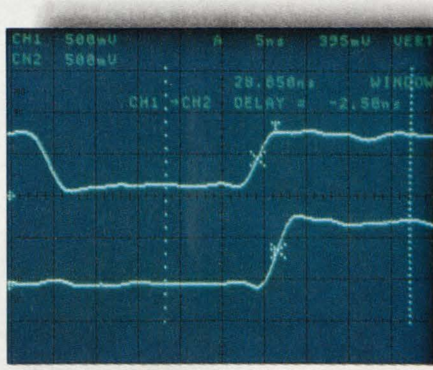
r problem?



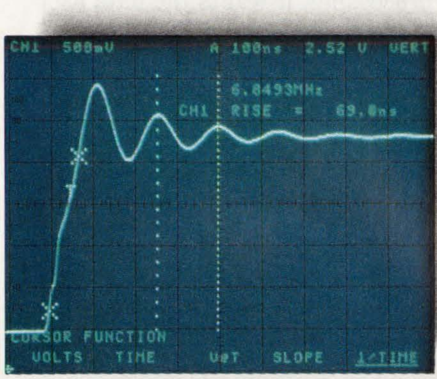
Characterizing signal noise?



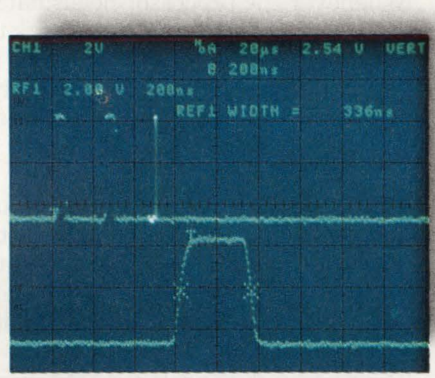
Capturing and analyzing long data streams?



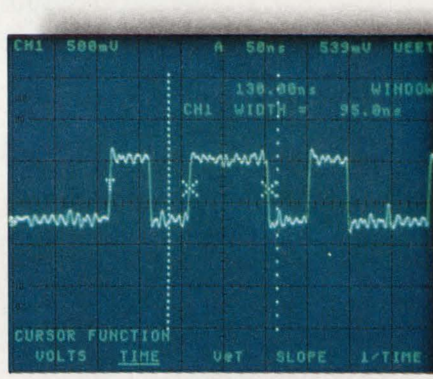
Measuring timing relationship between signals?



Performing complex measurements automatically?



Expanding glitches for close analysis?



Windowing in on signal details?

signal. Or Save on Delta to automatically verify that all parts of your signal fall within prescribed limits. Best of all, Tek's line of 100 MS/s digitizing scopes start at just $3995.

To find out which Tek scope is right for you, contact your Tek representative, return the card or call Tek direct. We can answer your questions and show you a scope that doesn't just look good on paper. It makes your toughest troubleshooting challenges routine.

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Cache Revitalizes VME

RICHARD NASS
COMPUTER SYSTEMS

Theoretically, 32-bit-wide VME systems transfer data at 40 Mbytes/s and 64-bit-wide VME 64 sends about 80 Mbytes/s. The much faster 256-bit Futurebus+ transfers data at 3.2 Gbytes/s. However, according to Ray Alderman, technical director of the VFEA (VME Futurebus+ Extended Architecture) International Trade Association, which also coordinates Futurebus+ programs, "The first high-end control-oriented systems on Futurebus+ are probably still about three to four years away." As a result, until Futurebus+ systems appear, systems builders appear limited in the bus transfer rates they can offer. However, there has been work on an interim solution that may relieve the transfer-rate limitations. At the recent Buscon/West Trade Show, VME suppliers discussed what appears to be a workable solution: Put cache memory onto their VME boards to relieve the bus of high-speed memory-to-processor data transfers.

With cache on VME boards, data isn't passed along the bus any faster, but it certainly zips along between processors on the same board. A computation-intensive application thus would see marked improvement. Adding cache, though, would not do much for an I/O-intensive application.

Whenever the processor needs data for processing, it wants the data as fast as possible. The quickest way is through cache memory. Although the processor must take the initial data it requires from the board's DRAM, subsequent accesses are taken directly from cache. This is because the data is put into cache when the processor takes it. Now the data is available for rapid reuse from the cache or it can be used to update the cache memories on other boards.

When the data leaves one board and moves to update others, the first board sends the data out on the bus with a cache modifier. Any other board in the system that has cache memory reads the modifier and gets the data. If a board doesn't have cache memory, it lets the modifier and the associated data bypass it. The processor can also be filling the cache memory while other data is being processed.

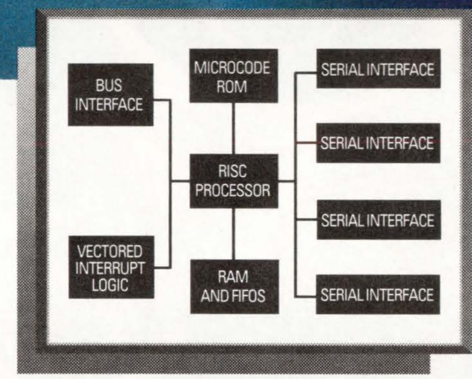
Previously, dual-ported RAMs were used when multiple-processor systems had to pass data to each other. But with dual-ported RAMs situated on several boards, there's the danger of the data stored in multiple sites lacking coherency. For example, to pass the same data to five boards, five separate write cycles would have to be sent out. In this case, the boards may not receive the data simultaneously. Moreover, they may not even receive the latest data. This can chew up valuable bus bandwidth.

In the proposed caching scheme, one global write cycle can update all of the boards that need updating. Even with shared data, the cache memories always get the latest copy of the data. The processor places the protocol overheads into the cache. Therefore, all of the boards in that cache domain are updated automatically.

Cache memory does carry some problems. There must be new control lines added to the boards to control the cache. In addition, current VME interface chips don't recognize cache, meaning the chips would have to be redesigned. This may shorten the life cycle of some chips. But, as Alderman maintains, "that's the price that you have to pay for progress."

The debate over multiple-processor issues usually leads to interprocessor communications. The data structure for this type of communication isn't defined. Caching on VME is the first step in defining these needed software standards. It creates a foundation on which interprocessor communication software standards can be developed. Cache on VME can also extend the bus' life, while offering an easy migration path to Futurebus+.

UXART
The Wait Is Over.
Now there's a serial I/O chip designed for UNIX.



An on-chip 10 MIPS RISC-based processor handles transmit and receive functions, buffer management, flow control, and all special character processing. On-chip FIFOs reduce host interrupts to give you more efficient interrupt handling. The result: faster system throughput, lower host overhead, and less waiting.

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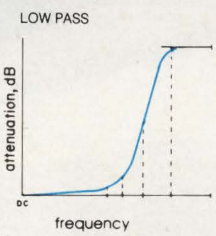
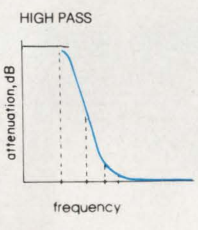


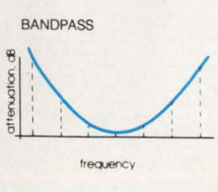
low pass dc to 1200MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	STOP BAND, MHz (loss>40dB) Max.	Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45



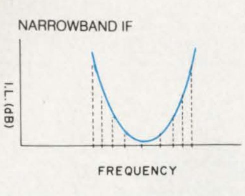
high pass dc to 2500MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	(loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95



bandpass 20 to 70MHz

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	Max. F4	(loss > 20 dB) Min. F5	Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95



narrowband IF

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	F6	STOP BAND, MHz I.L. > 35dB F7	F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

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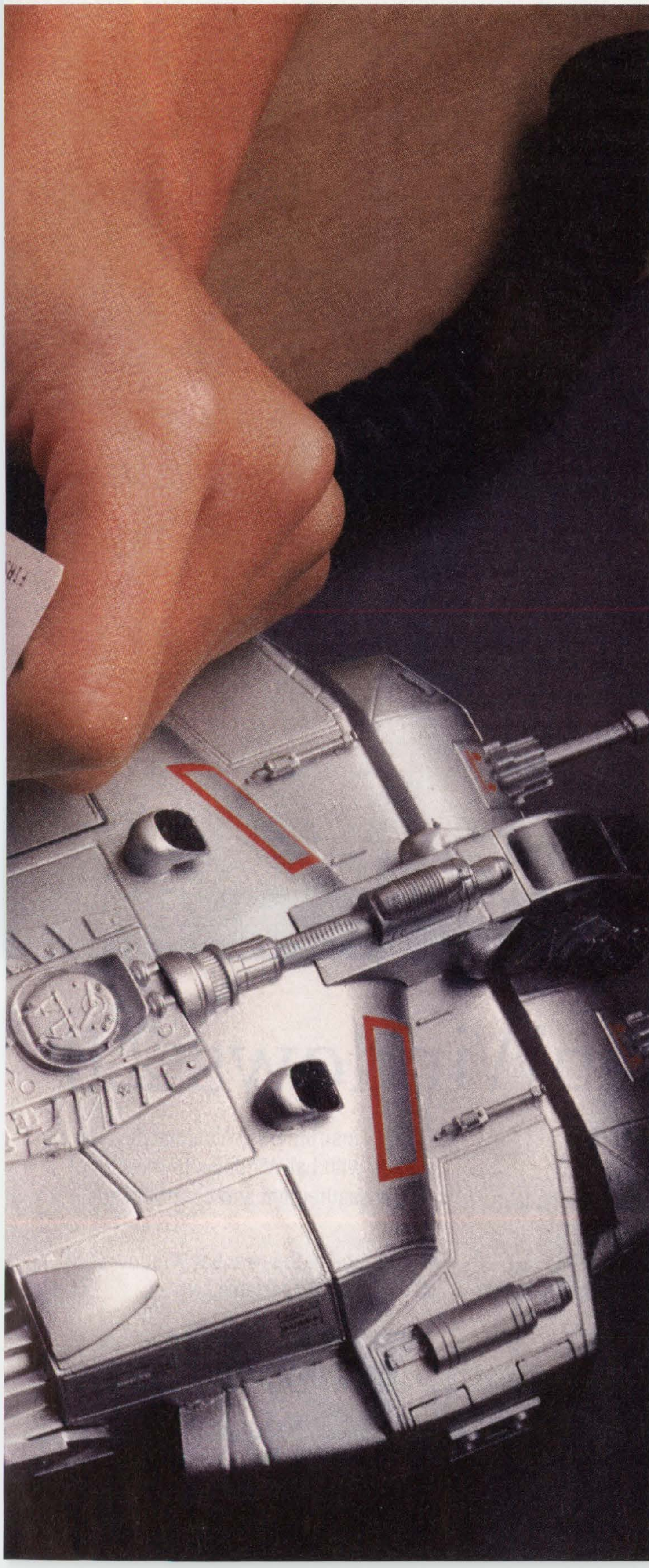

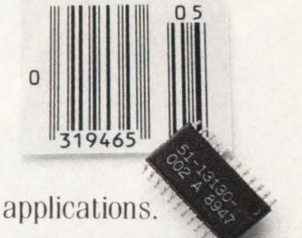

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CIRCLE 118

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CIRCLE 112

SINGLE-MODE FIBER TRANSMITS 10 GBITS/S

Data-transmission rates as high as 10 Gbits/s have been obtained over a 50-km (30-mile) repeaterless optical link made of standard and inexpensive single-mode glass fibers. This transmission capacity, achieved at the Central Laboratories for Communications Technology at Siemens AG, Munich, Germany, is 16 times that of 565 Mbits/s used for trunk lines between long-distance central exchanges. It's also four times that of 2.5-Gbit/s optical transmission systems based on single-mode fibers. The rate exceeds the specifications of German telecommunications authorities and other network operators, which stipulate 36 kms (22 miles) between repeaters. Up to now, 10-Gbit/s data rates could be obtained only with systems using special dispersion-shifted—and expensive—optical fibers. The Siemens system employs a 3-mW laser signal with a 1310-nm wavelength. It's directly modulated by on-off keying and detected with a gallium arsenide receiver. The link has an attenuation of about 19 dB and a bit-error rate of less than 10^{-10}. It uses highly efficient bipolar components made at the company's Research and Development Labs located in Munich. *JG*

MODELERS EXPAND TO LOW AND HIGH ENDS

To fill the need for increased system-level simulation, Logic Modeling Systems Inc., Milpitas, Calif., expanded its line of hardware modelers to include the low- and high-end of electronic design. The LM-1200 modeler's speed suits large design groups and complex device models, while the LM-500 brings affordable hardware modeling to small device groups with simpler device models. These two modelers, along with the existing LM-1000 modeler, can be networked together as multi-user, shared resources. The LM-1200, which can support 2560 signal pins, runs six times faster than the company's LM-1000. The speed gain results from using a 68040 processor, an improved networking server, and enhanced software algorithms. In addition, larger CPU memory expands the system's capacity for fault simulation by a factor of ten. The LM-500 uses a 68020 processor and supports 400 signal pins. Prices for the LM-1200 and LM-500, which will both ship in June, are $87,000 and $35,000, respectively. For more information, call (408) 957-5200. *LM*

ACTUAL RELEASE OF 386 WORKALIKE NOW AT HAND

Besides offering a top operating speed of 40 MHz in its first release, the Am386DXL—the first socket-compatible replacement for the 32-bit Intel 80386DX microprocessor—will operate at lower power levels than the original. The device also delivers a 21% performance boost over the 33-MHz version of the DX. By employing a fully static CMOS logic design, engineers at Advanced Micro Devices Inc., Austin, Texas, have cut the active power and considerably reduced the standby power. The DXL processor, in the sleep mode, draws less than 1 mA. In contrast, the Intel 80386DX consumes over 130 mA when idling. The low standby power of the DXL version enhances the battery life time of portable systems that would incorporate the full 32-bit processor. A reduced-bus version, the Am386SXL, will be released in the second half of the year. Sample prices for the socket-compatible Am386DXL will start at $306 for the 40-MHz version in 100-unit lots. Contact the company at (512) 462-4360. *DB*

UPGRADED 486 CPU DUE SOON FROM INTEL

Although Intel Corp., Santa Clara, Calif., has demonstrated it can push the 80486 to 100 MHz in the laboratory, the industry is waiting for the company to release its rumored 50-MHz versions to the general market. The upgraded chips will employ the same triple-level metal technology and logic improvements Intel's designers made to get the chip to operate at 100 MHz. However, many timing margins were relaxed so that the chip can operate in most system motherboards and cache subsystems with minimum redesign to handle the higher operating frequencies. No specific date has been set for the release of samples, but the mid to late second quarter is the purported target. *DB*

CFI TO SET UP COMPONENT SUBCOMMITTEE

The CAD Framework Initiative Inc. (CFI), Boulder, Colo., is set to launch a new technical subcommittee, Component Information Representation (CIR). The committee will focus on developing guidelines for digital representation of electrical components. Three CFI guideline efforts were highlighted in the proposal for the new subcommittee. First, a library effort will address the data-management and tool-interface aspects. Next, a meta-data effort will develop the information model for component representation by defining the structure, relationships, and characteristics of data used to

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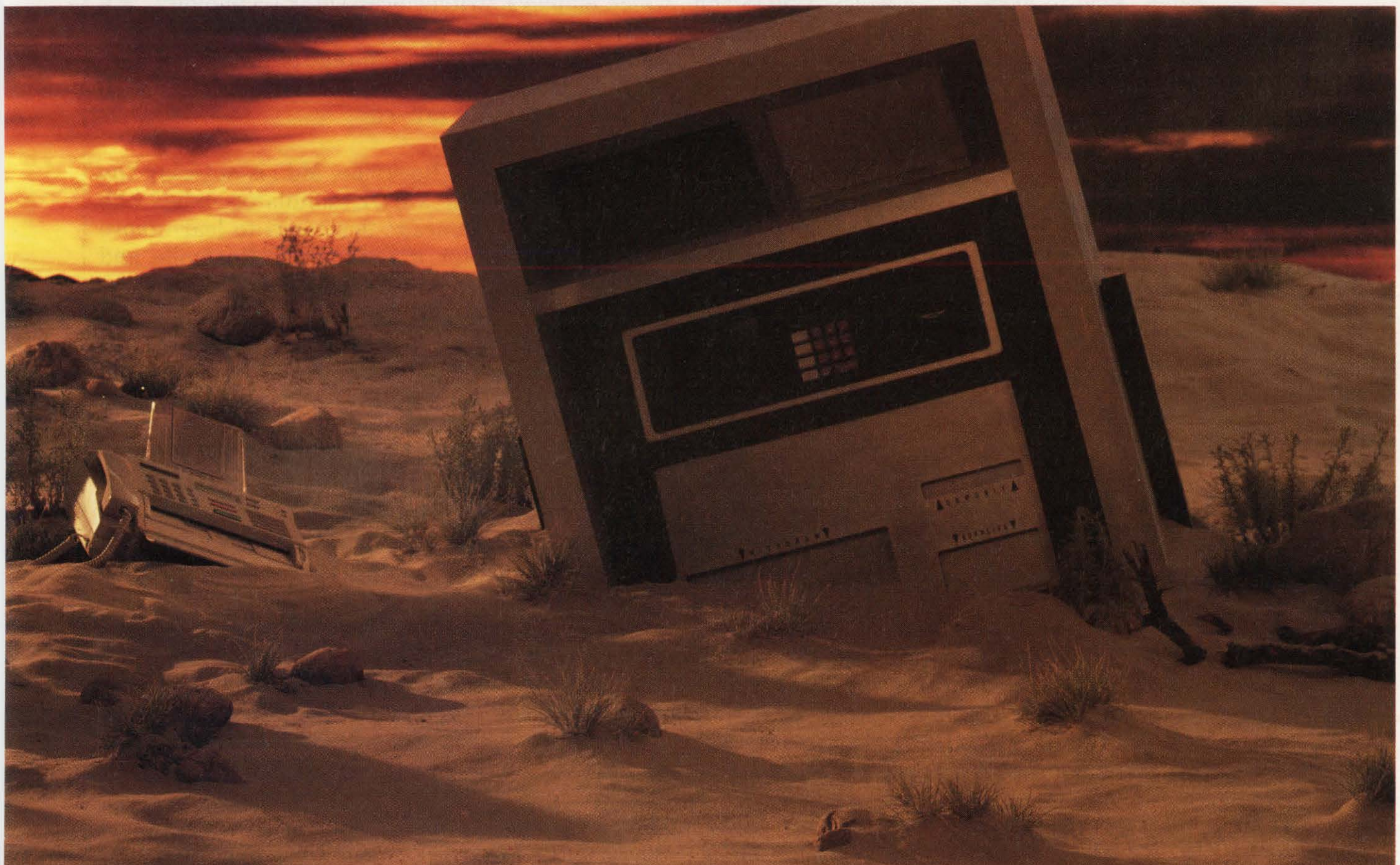

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Upgradability isn't something we tack on. It's ingrained in our design culture. A distinct advantage, your advantage, as you gear up to compete successfully in the exploding telecommunications marketplace.

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describe components. Finally, the electronic data-book effort will define the representation means for distributing component information, because electronic data books must be in a form that suits CAD tools. The first CIR project will involve drafting a requirements document by the end of this year. It will outline the scope and focus of CIR's efforts. For more information, call Andy Graham at (512) 338-3338. *LM*

OP AMPS AND ADCS ARE READY FOR 3-V RAILS

At an ISSCC evening panel session two years ago, the move to supply rails below 5 V was bandied about. The panel's gurus agreed the move would happen first in memories, followed by glue logic, microprocessors, and finally much later by analog chips. High-performance analog circuits and processes need headroom, so 3-V mixed-signal systems soon were out of the question. The experts hadn't noticed the paper earlier that day describing an op amp that laughed at 3-V rails—it worked off a mere 1 V. You can now buy real op amps based on that paper. But data converters were still left out in the cold. Now IC designer Sam Lum of Linear Technology, Milpitas, Calif., has come up with a 12-bit ADC with 574-like speed (25 μs conversion time) that runs off a 3-V rail. And its guaranteed to work at 2.7 V. The CMOS chip, which employs switched-capacitor technology, is a based on LTC's present 12-bit ADC, the LTC1290, which can operate down to 5 V. However, it took a process modification to achieve 3-V operation. The threshold voltage of the CMOS transistors from their standard process was lowered, optimizing it for 3 V. The ADC operates with a standard 2.5 V reference and needs just 1.5 mA from its 3-V rail. *FG*

LOW-COST SIMULATOR HELPS USERS LEARN VHDL

A new company called Open Solutions Inc., Rockville, Md., is entering the EDA market with a low-cost, interactive VHDL simulator called the VHDLearning Kit. The kit intends to encourage designers to learn more about VHDL. It was designed by CAD Language Systems Inc. (CLSI), also of Rockville, and costs $1495 on Sun workstations. VHDLearning Kit is based on CLSI's VHDL Tool Integration Platform, which is the basis for many companies' VHDL products. Open Solutions is offering the Learning Kit to users as an inexpensive starter system to learn on until they're ready for a full-function system. In fact, the Kit includes a catalog of VHDL products from leading EDA vendors. For more information on the VHDLearning Kit, call Frank Munero at (301) 963-5200. *LM*

TRIPLE 8-BIT FLASH ADC SPEED UPPED TO 30 MHZ

The 15-MHz Bt253, the only triple 8-bit flash ADC, has doubled its speed to 30 MHz in a new device called the Bt254. Like its antecedent, the Bt254 from Brooktree Corp., La Jolla, Calif., is designed to digitize three channels of video signals, such as RGB, generating up to 24 bits of color pixel data. It has a unique (for an ADC) lookup table, which enables it to convert a 24-bit true-color word to 15-bit or 8-bit true-color words, or to an 8-bit pseudo-color word. Six analog inputs (two for each flash) followed by a multiplexer are provided. Inputs can be selected by a host. The host can also adjust gain and offset by sending digital words to six, 6-bit on-chip trim-DACs. The Bt254 goes for $64 each in quantities of 100. Brooktree is also doubling the speed of its single-channel flash ADCs—the Bt208 and Bt251—to 30 MHz. The two new devices are the Bt218 and Bt252, respectively. For more information, call Joe Santen, (619) 452-7580. *FG*

INCLUDE FPGAS WHEN SYNTHESIZING DESIGNS

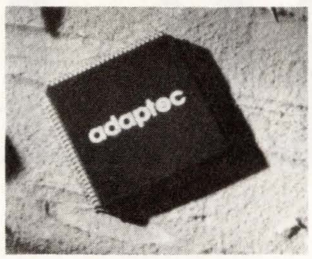
Engineers can now incorporate field-programmable gate arrays (FPGAs) in their synthesis plans if they use the Design Compiler from Synopsys Inc., Mountain View, Calif. The design methodology remains unchanged when targeting FPGAs. Library support for the Synopsys software has been announced by Actel Corp., Sunnyvale, Calif.; AT&T Microelectronics, Berkeley Heights, N.J.; and Texas Instruments Inc., Dallas. Designers can use VHDL or Verilog to describe an ASIC's function, and then quickly synthesize the design in an FPGA for production and prototyping. Descriptions can also be in the form of state tables, programmable-logic arrays, equations, or net lists. Optimized designs are written in EDIF 2 0 0 format so that FPGA-vendor tools can pick up the design for mapping and routing. Call Synopsys at (415) 962-5000. *LM*

DISK-CONTROLLER-IC PACKAGING SHRINKS FOR 1.8-IN. DRIVES

With each new generation of disk drives, system integrators demand more memory density and more operational features from drive manufacturers in an ever-shrinking form factor. In designing the coming generation of 1.8-in. disk drives, though, the drive manufacturers face a serious space crunch. They're turning to the makers of disk-drive-controller ICs to ease their task by squeezing the same, if not more, functionality into a thinner package. Fortunately, help is arriving in the form of the thin quad flat package (TQFP).

IC packaging for disk drives over the last several years has evolved from PLCCs to standard quad flat packages (QFPs). The QFP has been the mainstay in nearly all of the 3.5-in. drives and most 2.5-in. drives for the last couple of years. The first of the new 1.8-in. drives, which are intended for the next generation of laptop, notebook, and palmtop computers, will probably be satisfied with these QFPs as well. But, according to at least one controller-IC manufacturer, Adaptec Inc., Milpitas, Calif., the more advanced 1.8-in. drives will demand the thinner TQFP package.

The 100-lead package, which was developed in Japan, is just now getting attention in the United States. Japanese manufacturers have used the package for some time in smart cards, calculators, digital diaries and phones, and notebook computers. Its body, which is fabricated



of plastic for moisture resistance, is currently 1.4-mm thick. But now that the package is in preliminary review by both the Electronic Industry Association of Japan (EIAJ) and JEDEC committees, refinement of the emerging standard may shrink that dimension further. Internally, low-profile wire bonds link the chip to its leadframe. The body size is 14 by 14 mm, and the lead pitch, or spacing between leads, is 0.5 mm. The actual footprint, after factoring in a lead length of 1 mm, is 16 by 16 mm.

The first-generation 1.8-in. drives are likely to stand about 19-mm, or 0.741-in. tall. As the 1.8-in. specification moves on, a three-quarter-height drive will appear, which will stand 15-mm, or 0.585-in. tall. A half-height 1.8-mm drive will be 10-mm, or 0.390-in. tall. Obviously, the height of the controller chip becomes a factor at these thicknesses, and that's where the TQFP comes in. To put things in perspective, the body thickness of conventional QFPs is about 2.5 mm. After adding the leads and standoff from the top of the pc board to the bottom of the package, the total height is about 3 mm, which is 30% of the height of a half-height 1.8-in. drive. There simply won't be room on top of the drive's single disk for a chip with that profile.

Adaptec's initial offering in the new package is its AIC-6060, the well-known single-chip PC/AT disk-controller IC. According to Dennis Van Dalsen, marketing director for Adaptec's Peripheral Products Operation, that familiar chip was a clean, simple way for the company to get its feet wet with the TQFP. The AIC-6060 is being sampled in the package now. The next device to be offered in the TQFP is Adaptec's forthcoming AIC-7160, an AT disk-controller IC that encompasses constant-density recording, 88-bit Reed-Solomon on-the-fly error correction, and other advanced feature sets specifically intended for 2.5- and 1.8-in. drives. That chip will appear in the TQFP in the next couple of months.

According to Adaptec, the TQFP's space savings will cut costs for drive makers. Some 2.5-in. drives now using two-sided boards could move to single-sided boards. And, more importantly, a TQFP may even make it possible to shoehorn two-sided boards into the 10-mm height of advanced 1.8-in. drives.

Among the TQFP's advantages are its very short lead lengths. The leads, which are 1-mm long from the body's edge to the lead's tip, are less subject to damage and loss of coplanarity from handling. In comparison, typical QFP leads run anywhere from 1.6 to over 2 mm in length. On the downside, the new package's thermal resistance is about 10% worse than that of conventional QFPs. That's due to its reduced volume, which is about 50% of the QFP. But according to Van Dalsen, Adaptec's relatively low-power ICs don't approach the package's power-handling capacity.

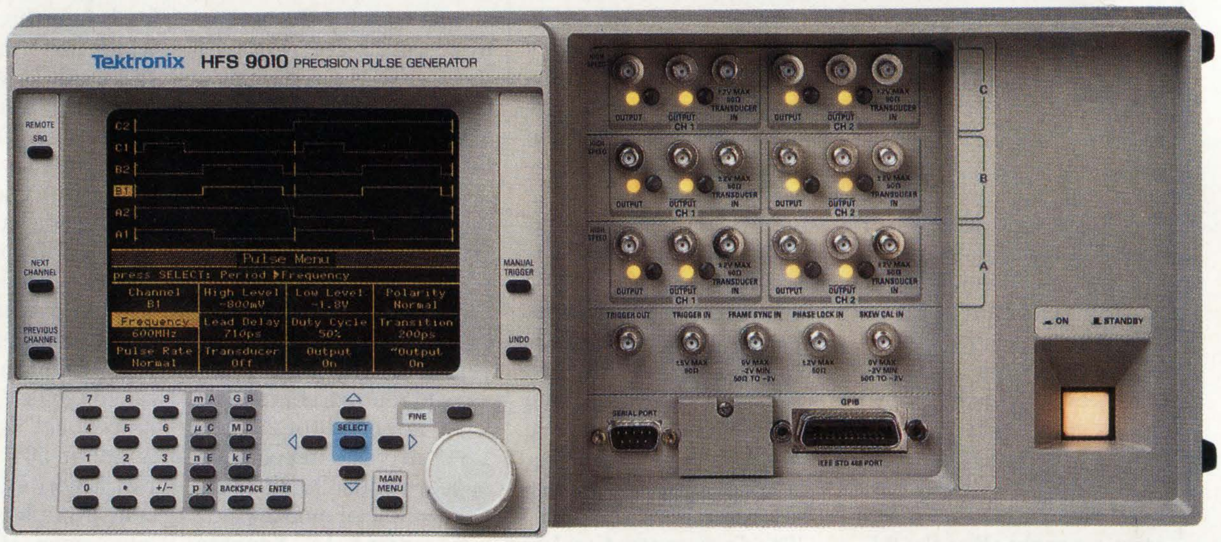
DAVID MALINIAK

NEW VERSION OF SYNTHESIS TECHNOLOGY RAISES DESIGN ABSTRACTION

Every advance in logic-synthesis technology helps tighten its grip on being number one in design methodology. The latest of these advances is embedded in the newest generation of tools from Synopsys Inc., Mountain View, Calif. Improvements in the second release of the company's synthesis software, which includes the Design Compiler and HDL Compiler, have brought more functionality, broadened technology coverage, and introduced a higher level of design abstraction.

Changes to the logic-synthesis technology enable users to synthesize circuits that are an average 14% faster than circuits designed with the previous technology. The Design Compiler can now maintain hierarchy when optimizing a design that includes multiple modules with multiple levels. It also optimizes multiple mod-

Making



You're looking at the biggest news in signal sources in years: two new families of pulse generators from Tektronix.

You can already see one reason why Tek's new pulse generators are stirring up so much interest: their what-you-see-is-what-you-get user interface vastly simplifies your life.

Now you can stop piecing the big picture together from one-line LEDs, blinking error lights and trial-and-error iteration. Tek's new scope-like display lets you set up and modify a whole set of parameters at once, with a true representation of your pulses and instant, visual feedback.

You name your application and logic technology: Tek has a signal source to match. For the first time, you can choose channel capacities from one to *six* channels, or rep rates from 50 MHz to a remarkable 600 MHz. Choose tools designed for logic, fast logic, or *mixed* technologies. Vary transition times from 200 ps to 10 ms. Test complex timing relationships with ease.

Add to all this our popular pulse generator plug-ins from Tek TM500/

ules concurrently. Taking this approach, the tool can do a better job of synthesizing a critical path that runs through the multiple modules. Other optimization improvements include new timing optimization algorithms and busing support.

Both the VHDL and Verilog versions of the HDL Compiler family were enhanced to choose the best circuit architecture while translating the hardware description language (HDL) to gates. Both now use resource allocation to make the most of the shared resources, such as adders. For example, the optimizer may reduce the number of adders from eight to three using a multiplexing scheme. This is done automatically, or can be controlled interactively by users.

In addition, the HDL compilers will use timing and area constraints to select the best architecture for arithmetic and comparator blocks. For instance, a fast carry-lookahead adder will be chosen when optimizing a design for speed, while a small ripple-carry adder will be chosen when optimizing for area.

Optimization occurs at the HDL level in version 2.0, unlike previous versions of the tools where it was performed on compiled code. The optimization includes the trade-offs on resource allocation. Version 2.0 changes circuit structure before it's targeted to libraries.

Also included in version 2.0 is Design Analyzer, a Motif-based graphical user interface and desktop design viewer. A Motif-based user interface helps ease the transition from gate-level design to top-down HDL design because most users are familiar with it. In addition, Design Analyzer includes intuitive pull-down menus that make synthesis software easier to learn how to use. Users can thus view schematics, rearrange design hierarchy, and set design constraints prior to synthesis and optimization.

Field-programmable gate-array (FPGA) synthesis has been added to the 2.0 toolset. The Design Compiler can now implement circuits in an FPGA, increasing the users' choices. Those choices already included CMOS and ECL gate arrays and standard cells. Companies that have announced FPGA synthesis libraries for Synopsys' version 2.0 products include Actel Corp., Sunnyvale, Calif.; AT&T Microelectronics, Berkeley Heights, N.J.; and Texas Instruments, Dallas.

Other features new to version 2.0 are tighter integration with VHDL simulation stemming from Synopsys' acquisition of Zycad's simulation technology, and the shipping of the Test Compiler and ECL Compiler. The Test Compiler incorporates design for test into the synthesis process and provides automatic test-pattern generation. ECL Compiler is a synthesis tool for ECL-based designs. In addition, users may license the software in a multi-user or single-user configuration. In the new single-user configuration, the software floats on the network. Users check out a copy of the software when it's needed, and return it to the pool when finished.

LISA MALINIAK

SUPPORT FOR FDDI SYSTEMS GROWS BEYOND TRANSCEIVERS

As time passes, so do the major issues with the fiber distributed data interface (FDDI). It seems like yesterday when transceiver standardization and the definition of the host-interface chip sets on each end were hot topics. Now the focus has shifted to routers that connect Ethernet local-area networks to FDDI networks, message concentrators, and network traffic controllers.

Routers direct data packets through a group of interconnected networks. They implement network data-link and physical-layer specifications set forth by the seven-layer model of the Open Systems Interconnect reference model. A router with reasonable performance should handle 15,000 packets/s over 125-Mbit/s FDDI and 10-Mbit/s Ethernet network ports. To achieve these tasks, engineers at National Semiconductor Corp., Santa Clara, Calif., employ a local CPU to control operations on a board that includes the router. The router is designed to take the single FDDI channel and convert the network's bit stream into four bidirectional Ethernet channels that include the TCP/IP protocol. Timing for the Ethernet portion of the board is controlled by a 25-MHz clock.

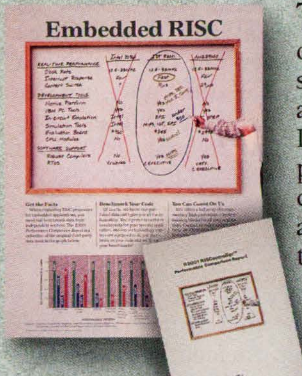
Employing National's Sonic network controllers, the Ethernet portion of the board can transfer data at 22 Mbytes/s over the host-system's parallel bus. The four bidirectional channels achieve such rates by taking advantage of the page-mode-access option included in most dynamic RAMs. The DRAMs are typically employed to form a large buffer memory that holds the packets to be transferred.

Message concentrators are proving invaluable in upgrading FDDI network reliability and flexibility. That's what National's engineers also found when they designed an FDDI topology consisting of a dual-ring-of-trees arrangement rather than the simple dual-ring approach usually found in the FDDI. On one side of each concentrator are ports to connect to the FDDI trunk rings. On the other side are additional ports, allowing other stations to be connected to the concentrator and then incorporated into the logical token path(s). By linking concentrators to the trunk rings, and with endstations attached to each concentrator, a star topology can be formed.

Designing a concentrator is pretty straightforward: Start with a microprocessor to act as the device's controller and add a real-time operating system and station-management software. Then the FDDI interfaces and data-routing logic must be added. The system logic can be designed to buffer or queue the incoming frames when the bus is busy. It must also do DMA operations between frame queues and

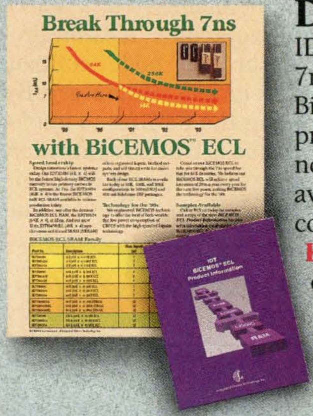
Count On IDT

The R3001 RISController™: The Embedded Processing Solution



The R3001 is the first derivative of the R3000 processor designed specifically for embedded control applications. Compared to the Intel 960 and AMD 29K processors, the R3001 is the most cost-effective solution for these applications—we have the data to prove it! Call and ask for **KIT CODE 0091A** to get an ***R3001 Performance Comparison Report***.

BiCEMOS™ ECL SRAMs: Technology for the '90s

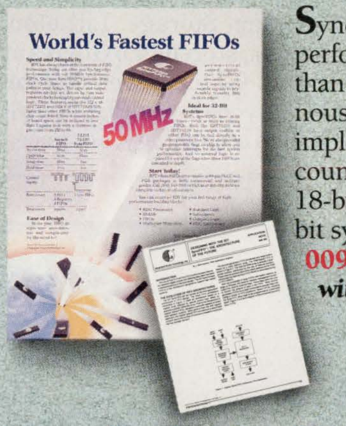


Design the fastest systems with IDT's BiCEMOS ECL family. At 7ns, the IDT10494 is the fastest BiCMOS 64K ECL SRAM in production. 256K and synchronous self-timed SRAMs are also available in 10K/100K/101K configurations. Call and ask for **KIT CODE 0091B** to get a copy of the ***BiCEMOS ECL Product Information*** booklet.

FCT-T Logic: Fastest Speed/ Lowest Ground Bounce

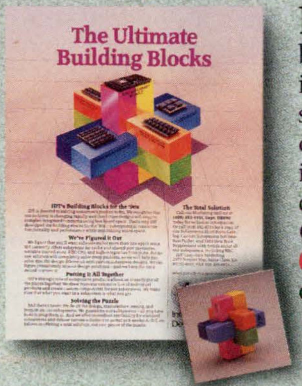
IDT's FCT-T Logic Family is the fastest logic family available and has the lowest ground bounce—up to 40% less than previous FCT devices! The FCT-T family provides direct TTL logic compatibility and is available in FCT, FCT-AT, and FCT-CT speeds. Call today for **KIT CODE 0091C** and get a copy of the ***High-Speed CMOS Logic Design Guide***.

The SyncFIFO™ Family: Double Your FIFO Performance



SyncFIFOs offer leading-edge performance that is 50% faster than other FIFOs. The synchronous architecture is easy to implement and reduces chip count 9-to-1. SyncFIFOs have 18-bit buses and are ideal for 32-bit systems. Ask for **KIT CODE 0091D** to get ***AN-60*: *Designing with the IDT SyncFIFO™***.

IDT Subsystem Modules: Building Blocks for the '90s



IDT offers a complete line of board-level subsystem products, including cache memory, shared-port memory, writable control store, RISC CPU, high integration modules, and custom designs for specific applications. Call today for **KIT CODE 0091E** and receive technical data and ***a free IDT puzzle!***

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IDT's cache tag SRAMs have the features you want to design in: single-pin block reset, totem-pole match output, 4K and 8K depths, industry standard pinouts, and an on-board comparator to simplify design. Call and ask for **KIT CODE 0091F** to get ***free samples*** of the IDT6178 cache tag.

Contact us today to receive data sheets and other design information on IDT's products.

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When cost-effective performance counts

Integrated Device Technology, Inc.

shared memory.

A circuit based on a pair of field-programmable gate arrays (FPGAs) from PlusLogic Inc., San Jose, Calif., shows how to efficiently direct system data traffic. It controls data-transmission and reception processes between a VMEbus-based host-system's memory and an FDDI board. The controller design's complexity enables the functions to be split across two of the company's 2020A FPGAs—one that handles the DMA control over the VMEbus and the other the memory interface. Frames as large as 4500 bytes can be transferred by the DMA controller. The remaining circuitry on the FDDI card consists of an FDDI chip set to deal with data recovery and transmission, a VMEbus controller, a 32-bit processor for node control, and some local memory. By using the FPGAs to implement the traffic controller, updates to the control logic can be done without a major board redesign.

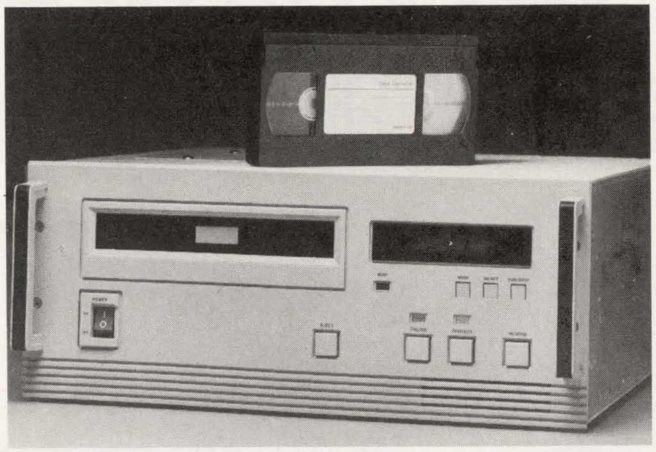
The National Semiconductor and PlusLogic developments are just three of many developments that will be described at the upcoming Silicon Valley Networking Conference. The conference, which will be jointly sponsored by ELECTRONIC DESIGN and SysTech Research Corp., San Jose, Calif., will be held at the Santa Clara Convention Center, Santa Clara, Calif., on April 23-25. For last-minute registration details, call Ken Majithia at (408) 924-3930.

DAVE BURSKY

VHS Drive Offers 14.5-Gbyte Storage At 0.1 Cent/Mbyte

With one VHS style T-120 1/2-in. cartridge tape, designers at Metrum Information Storage, Littleton, Colo., stored 14.5 Gbytes at just 0.1 cent per Mbyte. They combined helical-scan technology, advanced design/write magnetic heads, and a high level of linear packing density to create the drive. The T-120 cartridge is the same kind of tape that plugs into a standard VCR and has a recording time of about 2 hours *(see the figure)*. The drive's development emerged from a partnership formed between Metrum (formerly Honeywell's Test Instruments Div.) and Teac of Japan. The backup system records digital data on a premium-grade cartridge, the highest-quality VHS tape currently available.

The company claims that the cartridge has at least three times more storage capacity than other data-archiving technology. It's also more than four times faster, accepting data from the host computer at a sustained transfer rate of 2 Mbytes/s and a burst rate of 4 Mbytes/s. The drive can identify files and volumes at a high speed using a unique format implementation. Any file on the cartridge can be located in an average of 45 seconds. The maximum time for a full end-to-end search is 90 seconds, equating to a search rate of 160 Mbytes/s. The drive permits fixed- and variable-length records.



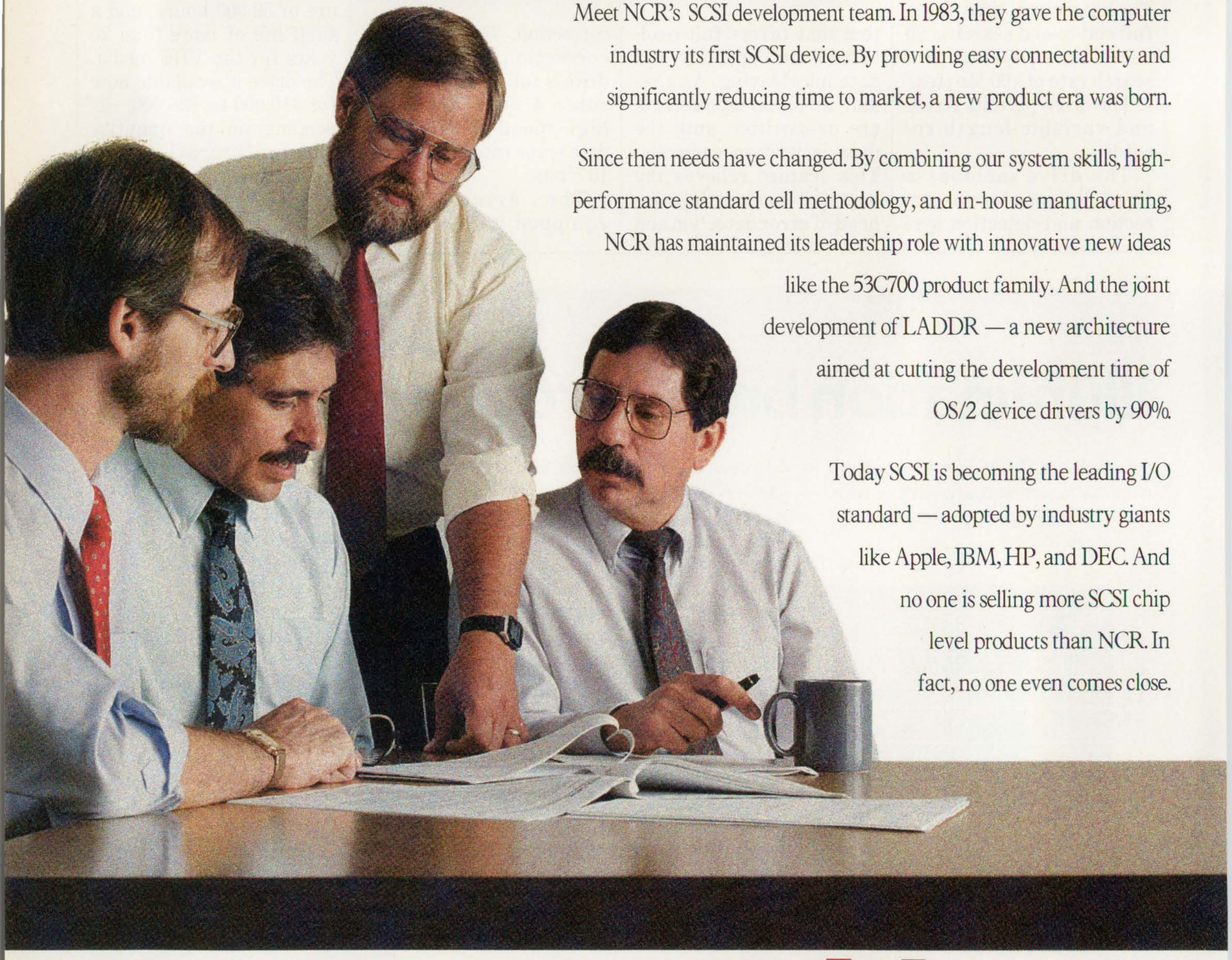
The drive includes a Reed-Solomon error-correction and detection system that offers full read-after-write capability and data interleaving. As a result, all initial tape defects are overwritten until the data is written correctly. This feature relieves the host system from the overhead of error detection and correction. To extend the correction feature, the drive is fully buffered with either 4 or 8 Mbytes of high-speed DRAM. The data error rate is less than 10^{-13} bits.

The drive comes equipped with either a SCSI or Pertec/Cipher Data Products interface. It also allows for a custom interface through the company's proprietary interface bus, whose protocol and bus specifications are available to users. Moreover, the drive contains an interface that can be connected to a modem for remote diagnostics.

The RSP-2150, which is 15.5 by 13.4 by 7 in., has a mean-time-between-failure of 50,000 hours, and a shelf life of more than 20 years for the VHS media. The drive is available now for \$10,000 to \$25,000, depending on the quantity and configuration. For more information, call Metrum at (303) 773-4700.

RICHARD NASS

Here's one reason that over half of all SCSI devices sold are NCR.



We created the market… and we still lead the way.

Meet NCR's SCSI development team. In 1983, they gave the computer industry its first SCSI device. By providing easy connectability and significantly reducing time to market, a new product era was born.

Since then needs have changed. By combining our system skills, high-performance standard cell methodology, and in-house manufacturing, NCR has maintained its leadership role with innovative new ideas like the 53C700 product family. And the joint development of LADDR — a new architecture aimed at cutting the development time of OS/2 device drivers by 90%.

Today SCSI is becoming the leading I/O standard — adopted by industry giants like Apple, IBM, HP, and DEC. And no one is selling more SCSI chip level products than NCR. In fact, no one even comes close.

Part of the NCR SCSI Development Team: (left to right)
Jerry Armstrong, Sr.Software Engineer; **Harry Mason**, Strategic Marketing Manager; **John Lohmeyer**, NCR Sr. Consulting Engineer and Chairman of the ANSI X3T9.2 Committee and **Dave Skinner**, SCSI ProductManager.

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Electro® International

ELECTRO GOES INTERNATIONAL

JOHN NOVELLINO

In the face of rapidly changing technology, engineers must keep pace with the latest innovations to stay competitive in the marketplace. But technology isn't the only area that's evolving. The electronics industry is growing more global every day. To remain viable, engineers must also monitor the developing global marketplace—how it affects the technology they deal with and the way their companies do business.

Recognizing these dual needs, Electro, the broad-based East Coast regional conference and exhibition, has changed its name to Electro/International. To underscore that the name change wasn't cosmetic, the conference will feature a number of international speakers and a Global Business Colloquium as part of its professional program. The latter includes seven seminars that will examine global marketing, government and trade organizations, and transnational programs. The event is scheduled for the Jacob K. Javits Convention Center in New York City, April 16-18.

The program also features a keynote address by congressman Don Ritter from Pennsylvania, who will discuss key issues American companies will face in the 21st century. Ritter will offer advice on how to secure market positions in key end-use electronic-product industries. Specifically, he will talk about reversing a trend that has made many sectors of the electronics business unprofitable for American companies. This trend is the result of governmental and industry policies, as well as strategies of international competitors. Ritter will address a broad industry consensus that high-resolution imaging systems, particularly high-definition television, are the key to a revival of the U.S. consumer electronics industry.

Ritter's technical background makes him well-qualified to address a gathering like Electro/International. He holds a bachelor of science degree from Lehigh University, Bethlehem, Pa., and master and doctor of science degrees from the Massachusetts Institute of Technology, Cambridge, Mass. Ritter has taught at Lehigh, was manager of research and development there, and was a

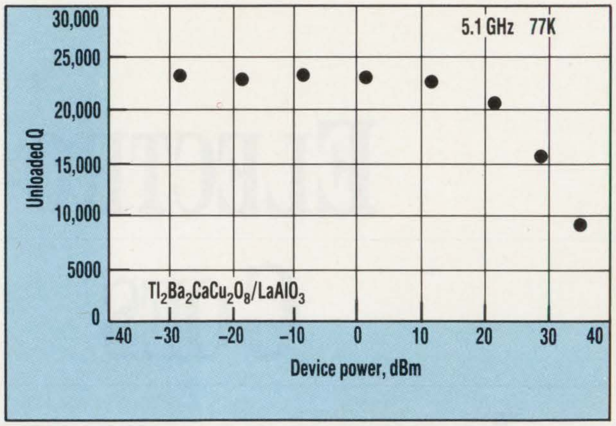
ELECTRO/INTERNATIONAL

consultant in the materials and manufacturing industries.

Electro/International's technical sessions cover a wide range of topics. General headings include computers, digital systems, and software; manufacturing and test; communications; IC technology; and medical electronics. Also covered will be such leading-edge technologies as superconductivity, magnetic levitation, photovoltaics, and sensors.

In the superconductor area, much of the research is concentrated on high-temperature superconducting (HTSC) materials. Researchers have already found some materials that become superconductive above the boiling point of liquid nitrogen, 77K, leading to the possibility of more practical systems. For example, researchers at Superconducting Technologies Inc., Santa Barbara, Calif., fabricated superconducting thin films that exhibit nearly 100 times lower losses at microwave frequencies than do the best normal metals.

The results are reported by George V. Negrete and McDonald Robinson, members of the technical staff, and Robert B. Hammond, vice president for technology. At 77K, a $Tl_2Ba_2CaCu_2O_8$ thin film on a $LaAlO_3$ substrate had a surface resistance of 0.2 mΩ at 9.55 GHz. This figure was 50 times lower than that for high-purity copper.



1. A straight-line resonator built with a high-temperature superconducting material exhibited an unloaded Q of 24,000 at 5.1 GHz at power levels to 10 dBm. This corresponds to a surface resistance of only 0.11 mΩ.

The team used wet-etch photolithography to pattern the film into a 7-by-1-mm straight-line resonator. At 5.1 GHz, the unloaded Q of this device at powers to 10 dBm was 24,000, corresponding to a surface resistance of 0.11 mΩ, nearly 100 times lower than the best normal metals. The Q falls slowly above 10 dBm, reaching 45% of its original value at the 36-dBm level *(Fig. 1)*.

As testability becomes more of an issue in today's complex circuits, scan-based design-for-test schemes gain popularity. But because scan testing uses a serial interface to transmit data to and from the circuit under test, communication between the scan ring and a processor's parallel bus can be inefficient. To solve this problem, Jay Brown of the Advanced CMOS Design Department in National Semiconductor's Standard Products Division, South Portland, Maine, describes a parallel/serial converter. The device acts as an in-

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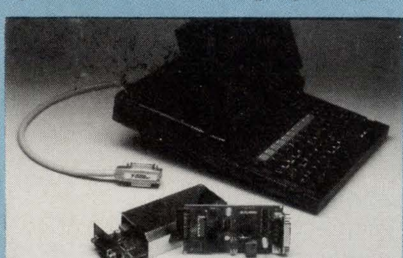
Module turns laptop into IEEE-488 controller. Equipped with the GD-GPIB plug-in module, the GRiD System 1500 Series laptop comput-



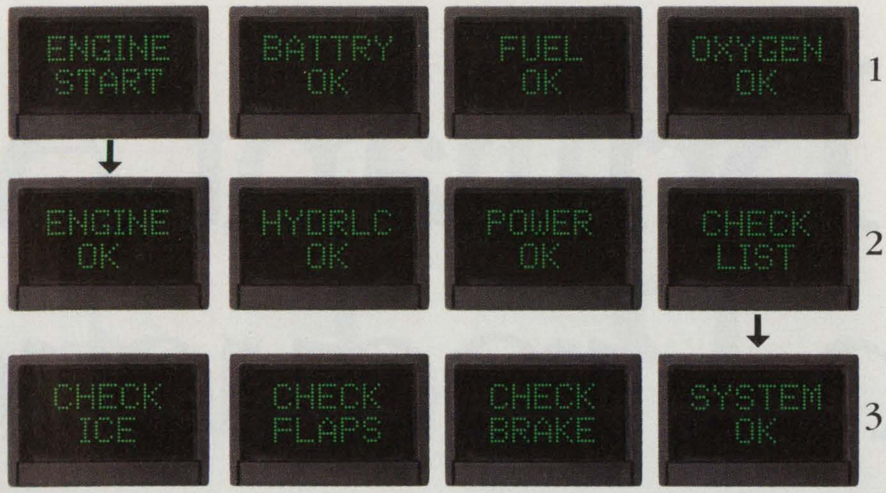
er can be used for portable test applications. The module fits the standard GRiD adapter case for easy installation, and comes with an RF-shielded IEEE-488 receptacle. Capabilities include six interrupt lines, transparent interrupt enabling/disabling, three DMA channels, transparent DMA enabling/disabling, and interrupt capability. Sustained 400-kbyte/s data rates in read and write operations are possible. The GD-GPIB costs $695 and comes with either the NI-488.2 Windows 3.0 or NI-488.2 MS-DOS software driver.

National Instruments Corp.
Austin, TX; (800) 433-3488 or (512) 794-0100.
Booth 2034 **Circle 481**

Photometric sphere aids quality control in lamp production. The model 504D MOD 1 photometric integrating sphere is an ac-operated, bench-mounted instrument for measuring average luminous intensity (mean spherical candlepower). The unit, which is useful in maintaining quality control over production quantities of incandescent lamps, has a range of 1999.9 spherical millicandelas. A photooptically corrected silicon photosensor ensures rapid measurements without hysteresis, fatigue, or memory errors. A chopper-stabilized amplifier optimizes loading so the conversion from luminous intensity to electrical output remains linear.

Western Photometric Laboratories
Chino, CA; (714) 597-4889.
Booth 2062 **Circle 482**

Dual optical encoders boast compact size. The Series D688 Miniature Optical Encoder assembly contains two concentric-shafted encoders and can be mounted in a 1/2-in.



AN APPLICATIONS EXAMPLE. While the following example is for aircraft, it could apply to any air, land, sea or space system.

SEQUENCE ONE: The four-pushbutton display reads "ENGINE START," "BATTERY OK," "FUEL OK," OXYGEN OK." The operator selects "ENGINE START."

SEQUENCE TWO: The four-pushbutton display now changes to read "ENGINE OK," "HYDRLC OK," "POWER OK," "CHECK LIST." The operator selects "CHECK LIST."

SEQUENCE THREE: The four-pushbutton display now reads "CHECK ICE," "CHECK FLAPS," "CHECK BRAKE," "SYSTEM OK." In this manner, the designer can program in as many sequences as required.

Design flexibility: The programmable display system.

Vivisun Series 2000, now the leading programmable display pushbutton system, interfaces the operator with the host computer. The user-friendly LED dot-matrix displays can display any graphics or alpha-numerics and are available in green, red or amber. They can efficiently guide the operator through any complex sequence with no errors and no wasted time.

They also simplify operator training as well as control panel design. One Vivisun Series 2000 programmable display system can do the work of 50 or more dedicated switches. In short, Vivisun Series 2000 gives the design engineer more control over the design.

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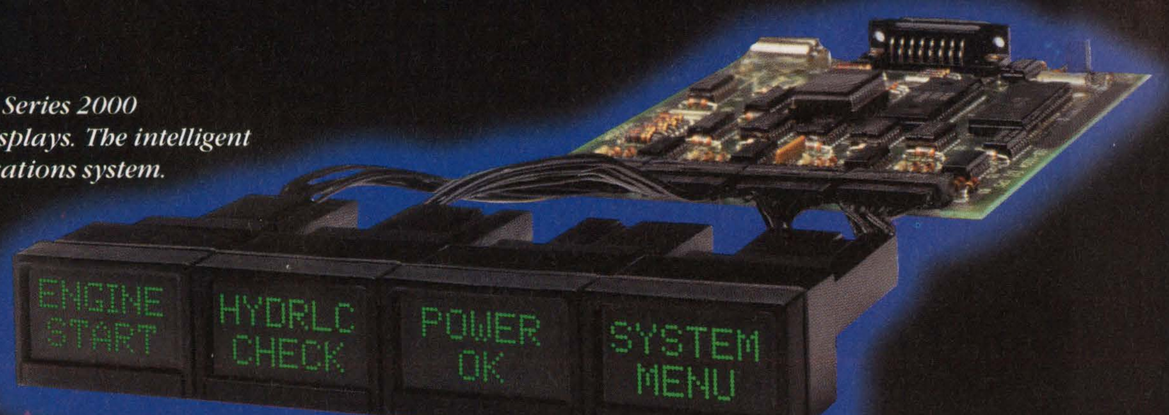

SERIES
VIVISUN 2000™

CIRCLE 85

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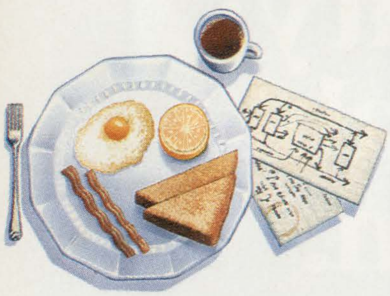
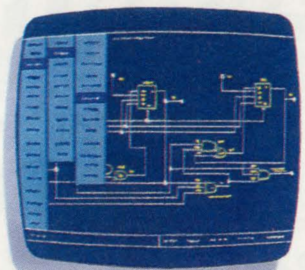
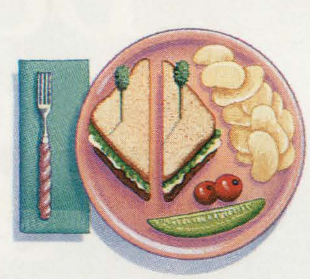


7:05 am : Breakfast
Suddenly, between bites, the answer to that new system design jumps right into your brain. But how to make it work in silicon? Use an Actel field programmable gate array!



8:50 am : Design
You warm up the design program on your 386 and put in the final touches. Then a quick rule check and 25 MHz system simulation with the Action Logic System software.

11:00 am : Place & Route
You watch the system place and route all 1700 gates (out of 2000 available) in under 40 minutes. 100% automatically! A final timing check. Then think of something to do until lunch.



12:00 pm : Lunch
Remember lunch? Normal people actually *stop working* and have a nice meal—right in the middle of the day! With Actel's logic solution, this could become a habit.

Actel Field Programmable Gate Array Systems.

They're a feast for your imagination.

Actel's ACT™ 1 arrays bring you a completely new approach to logic integration. Not just another brand of EPLD, PAL® or LCA™ chips. But true, high density, desktop configurable, channeled gate arrays.

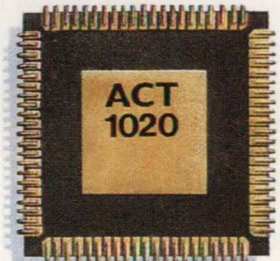
They're the core of the Action Logic System, Actel's comprehensive design and production solution for creating your own ASICs. Right at your desk. On a 386 PC or workstation. With familiar design tools like Viewlogic,™ OrCAD,™ and Mentor.™

And do it in hours instead of weeks. Even between meals.

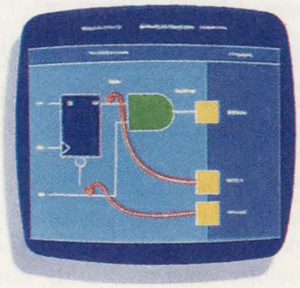
How? With features like 85% gate utilization. Guaranteed. Plus 100% automatic placement and routing. Guaranteed. So you finish fast, and never get stuck doing the most

Actel FPGA Product Family		1010A	1020A
Equivalent Gates	Gate Array	1200	2000
	PLD/LCA	3000	6000
User I/O		57	69
System Clock (MHz)		20-40	20-40
Availability		NOW	NOW
Technology (micron)		1.2	1.2

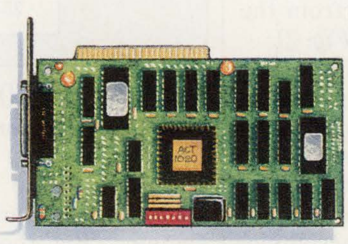
Breakfast And n By Dinner.



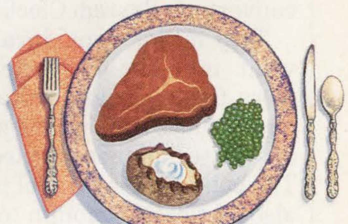
1:15 pm : Program
You load the Activator™ programming module with a 2000-gate ACT 1020 chip and hit "configure." Take a *very* quick coffee break while your design becomes a reality.



1:25 pm : Test
You do a complete, real-time performance check, with built-in test circuits that provide 100% observability of all on-chip functions. *Without* generating any test vectors.



4:00 pm : Production
Your pride and joy is designed, created, tested, and off to the boys in Production. And you're finished *way* ahead of schedule! Better think of something to do until 5:00.



6:00 pm : Dinner
Remember dinner? Normal people actually *go home* and eat with their families. On your way, start thinking about how Actel's logic solution can help you be brilliant tomorrow.

tedious part of the job by hand.

Design verification is quick and easy with our Actionprobe™ diagnostic tools, for 100% observability of internal logic signals. Guaranteed. So you don't have to give up testability for convenience.

In fact, the only thing you'll give up is the NRE you pay with full masked arrays. You can get started with an entry level Action Logic System for under $5000. Guaranteed.

And Actel FPGAs are even 883 mil-spec compliant.

You can be brilliant right now with 1200- and 2000-gate devices, and a whole new family of 8000-, 4000- and 2500-gate parts are on the way. Call **1-800-227-1817, ext 60** today for a free demo disk and full details about the Action Logic System.

It could make your whole day.

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Risk-Free Logic Integration

You loved ACT 1. Now catch ACT 2. Phone 1-800-227-1817, ext 62 to reserve a place at the Actel FPGA Technology Seminar coming soon to your area.

CIRCLE 117

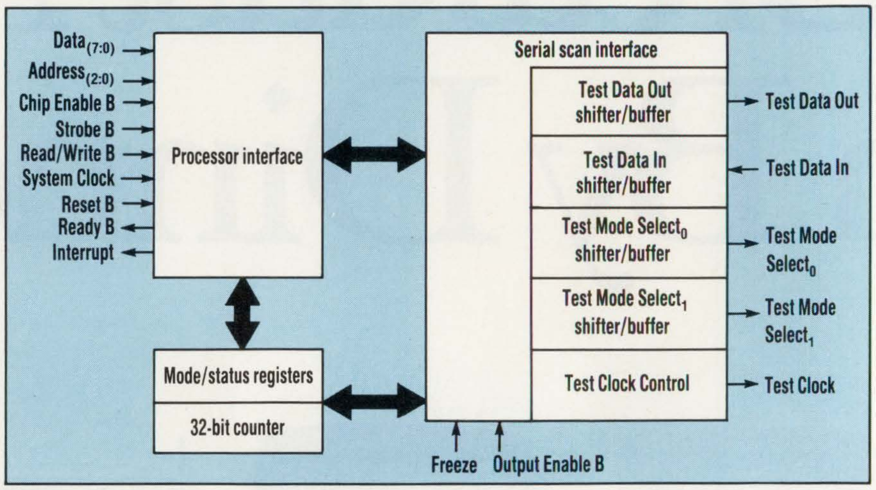
ELECTRO/INTERNATIONAL

terface between a circuit's parallel host bus and the serial test bus.

The conversion is managed by a bank of double-buffered, parallel-to-serial shift registers. Brown notes that double buffering allows a parallel write or read to occur while data is shifting, increasing throughput. The serial port's pin names follow the IEEE-1149.1 boundary-scan convention. Three pins—Test Data Out, Test Mode Select$_0$, and Test Mode Select$_1$—output serial data. Data is shifted in on the Test Data In pin. The Test Clock is derived from the converter's System Clock *(Fig. 2)*.

Two major considerations that went into the converter's design were flexibility and testability. The device must support the many types of scan techniques that are available. The converter's parallel port should also be flexible enough to accommodate various choices for the host bus. And because testability is the main reason for implementing scan techniques, the converter itself must be easily testable.

Another area of increasing interest is fuzzy logic for control systems. A previously reported systolic array is well-suited to perform the fast fuzzy inference processes for these systems. But the systolic array is based on VLSI technology, and its complexity makes it prone to failure. To combat this problem, Mahmoud A. Manzoul and Dinesh Jayabharathi of Southern Illinois University's Department of Engineering, Carbondale, added a fault-detection capability to the array.



2. TO IMPROVE **scan-based-testing efficiency, a parallel-to-serial converter connects the host processor's parallel bus to the circuit under test's serial test bus.**

The technique is called duplication with complementary logic. According to the authors, their architecture adds minimal hardware to each of the array's processing elements, which are called fuzzy inference step processors (FISPs). In the complementary-logic method, both the needed function, f(x), and its dual, $f_d(x)$, are performed using the normal input and its complement, re-

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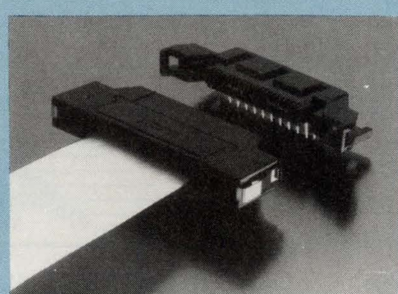
square panel hole. Each encoder outputs two square waves in quadrature using from 20 to 64 pulses/revolution. Voltage level ranges from 0.4 to 2.4 V. Their small size makes suits them for instrument-style control applications in medical, electrical, and electronic equipment. Required input power is 30 mA at 5 V dc ±5%. Operating temperature range is –20 to +65°C, and rotational life is a minimum of 1 million revolutions. Prices start at $33.98 each in quantities of 1000.

Clarostat Mfg. Co. Inc.
Dover, NH; (603) 742-0481.
Booth
2525 **Circle 483**

Connectors pass fast signals with minimal distortion. The Micro-Strip connectors maintain a 50-Ω ±10% interconnection impedance and limit crosstalk to less than 4% for signals with rise times as fast as 1 ns (measured as active/quiet/active). With contacts on 0.050-by-0.100-in. center-line spacing, the connectors can pack 40 signal lines and their



associated grounds into a linear inch. They're available as right-angle and vertical-stacking board-to-board connectors and cable-to-board connectors. In high-volume quantities, the Micro-Strip stacking connectors cost $0.15 per mated line and the right-angle connectors go for approximately $0.21 per mated line.

AMP Inc.
Harrisburg, PA; (800) 522-6752.
Booth
2322 **Circle 484**

Tiny VCXO boasts very high control sensitivity. The Model VC-7025 voltage-controlled crystal oscillator features a control sensitivity of ±50 ppm/V typical, but can be delivered with sensitivities as high as ±70 ppm/V. The device comes in a 14-pin DIP measuring only 0.52-in. wide by 0.82-in. long by 0.31-in. high. The unit's frequency range is 2 to 35 MHz, with a stability of ±25 ppm from 0 to 70°C. With full com-

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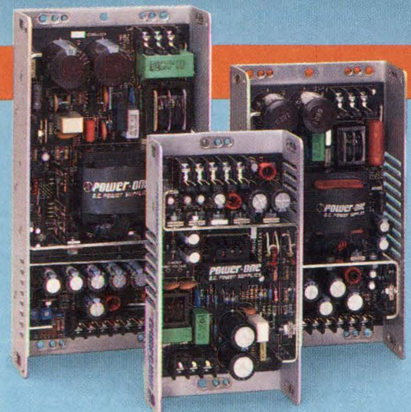

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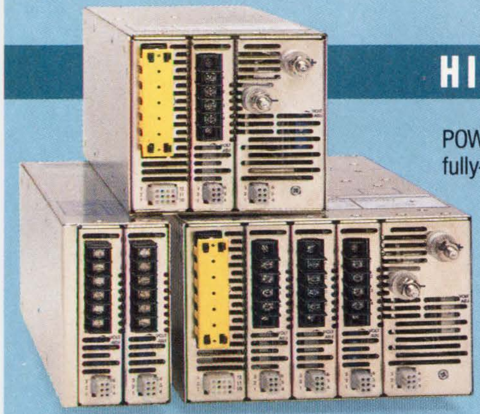

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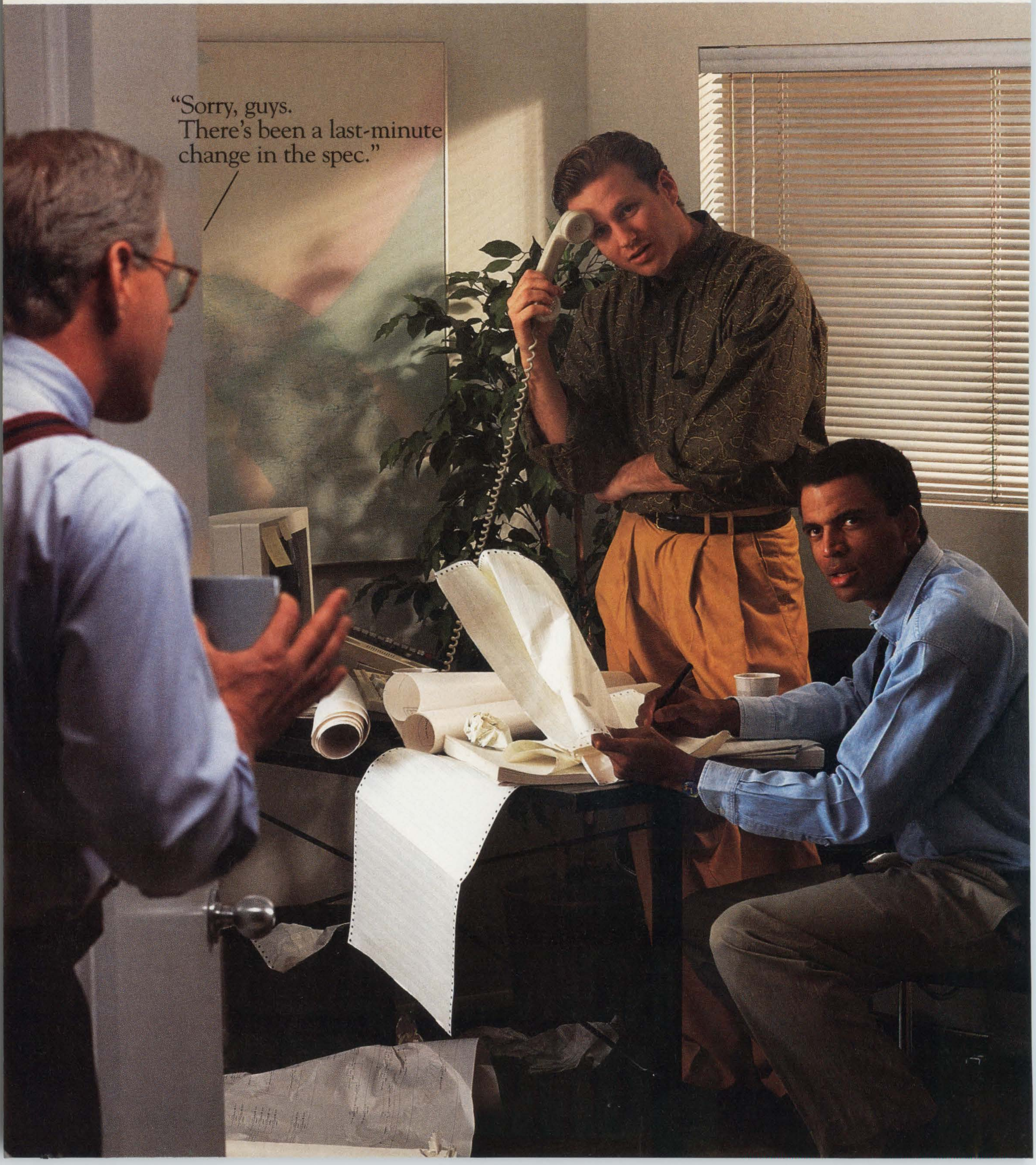

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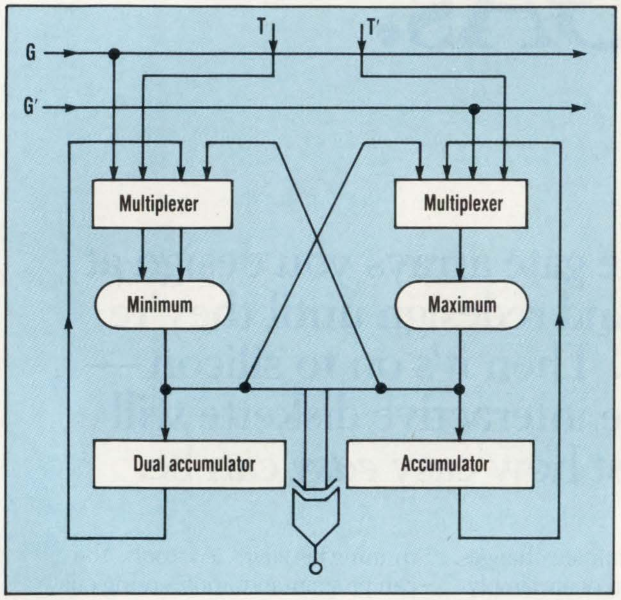

3. WITH minimal added hardware, this fuzzy inference step processor has been modified to permit fault detection using a technique called duplication with complimentary logic.

spectively. If the two operations are fault-free, the two outputs will be complements of each other.

Because fuzzy logic uses two operations (min and max), the dual function is obtained by interchanging them. The resulting FISP employs its normal inputs, one from the fuzzy relation T and one from the fuzzy input G, and their complements, T' and G' *(Fig. 3)*. The authors say that their technique can be used in any fuzzy systolic array regardless of size, dimensions, or interconnections.☐

HOW VALUABLE?	CIRCLE
HIGHLY	524
MODERATELY	525
SLIGHTLY	526

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patibility using the Motorola K-1523-B, the oscillator is ideal for phase-locked loops in such high-volume applications as telephones, laboratory instruments, PBXs, and local-area networks. The VC-7025 costs $14.50 each in lots of 1000. Delivery is in 8 to 10 weeks after receipt of order.

Raltron Electronics Corp.
Miami, FL; (305) 593-6033.
Booth
2625 **Circle 485**

Voltmeter features high sensitivity, low noise. The Model 182 Sensitive Digital Voltmeter offers 1-nV sensitivity with 6-1/2-digit resolution. Noise is only 15 nV pk-pk, even on the meter's lowest range. More than 50 readings/s are possible, with storage available for 1024 readings. Helping to ensure accuracy is the instrument's input resistance, which is greater than 10 GΩ on all ranges. Also contributing to high accuracy is a special low-thermal-input connector and cable, which substantially reduces thermal electromotive force. Ranges include 3 mV, 30 mV, 300 mV, 3 V, and 30 V. The Model 182 is programmable using the GPIB.

Keithley Instruments Inc.
Cleveland, OH; (216) 248-0400.
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2040 **Circle 486**

Fuses feature solid matrices. A line of subminiature fuse packages uses solid-matrix construction rather than the traditional technique in which the fusible element is suspended in air and enclosed in a glass or ceramic tube. Advantages include better current-rating stability after exposure to soldering and cleaning processes, extremely low I^2t let-through energy under short-circuit conditions, and resistance to mechanical shock and vibration. Versions available are the axial-lead Microtron, the radial-lead PC-Tron, and the surface-mounted SMD Tron. In 10,000-piece lots, prices range from $0.18 to $0.53, each depending on current rating and package.

Cooper Industries Inc., Bussmann Div.
St. Louis, MO; (314) 527-1444.
Booth
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Ultra-small optical interrupter sensors mount on pc boards. A line of solid-state optical sensors measuring only 4-mm^2 delivers square-wave, no-noise outputs. The EE-SX1038, EE-SX1052, EE-SX1067, and EE-SX1068 are available with slot widths from 0.9 to 2.0 mm. The sensors have a phototransistor output and a 40-μs typical response time. Models EE-SX1038 and EE-SX1068 have standard-size 0.100-in.^{2} footprints. The units are suitable for use in cameras, tape and disk drives, computer peripherals, typewriters, and other small systems requiring precise switching or linear-motion feedback. Prices start at $0.78 each in lots of 1000.

Omron Electronics Inc.
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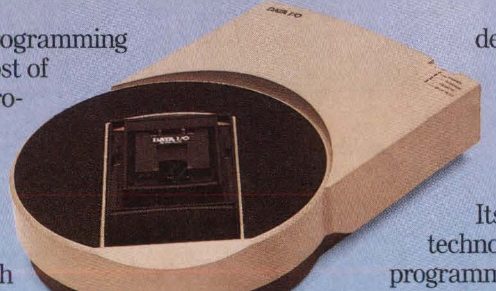

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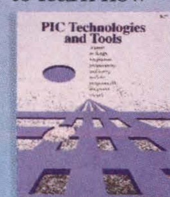

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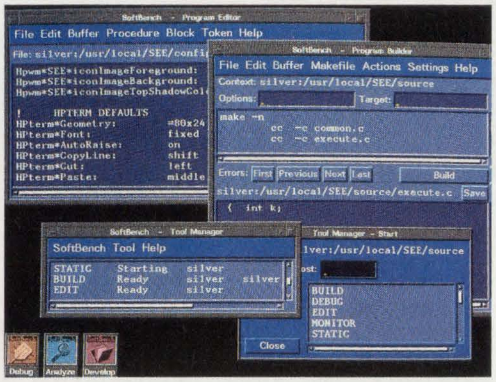
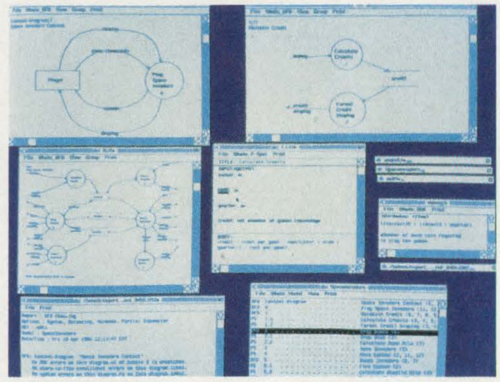


HP's SoftBench: A tool integration framework and a program construction toolset.



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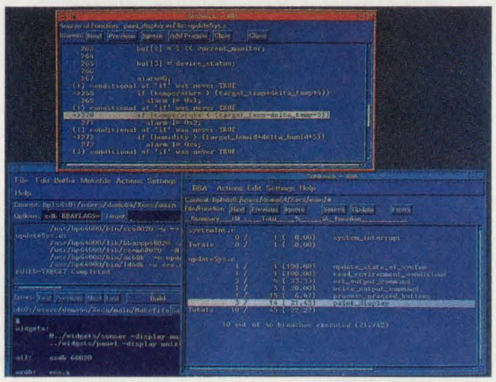

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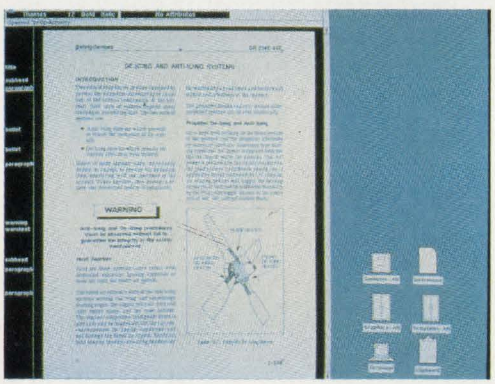

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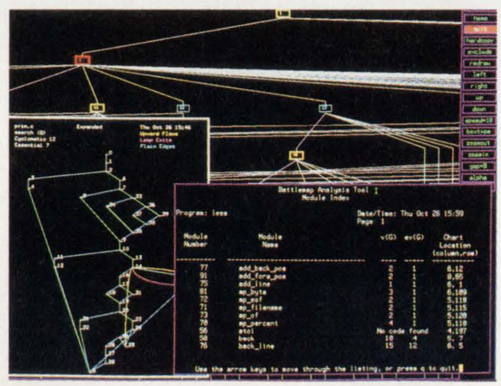


McCabe Test Tools: An automated software testing and reverse engineering application.

That Was Then...

Quality Comes Through

Company Delivers On Its Promise Of 12-ns SRAMs

By Hugh G. Willett

SANTA CLARA, CALIF. — Silicon Valley start-up Quality Semiconductor Inc. this week will fulfill its plan to move into high-performance static RAMs.

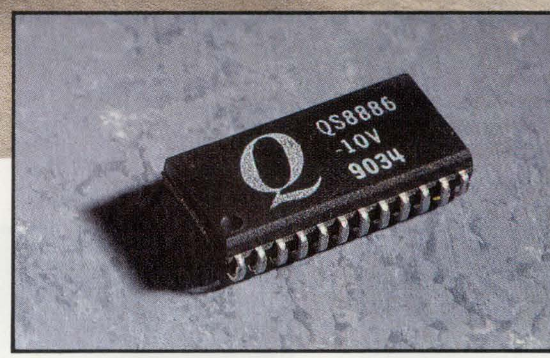
Quality Semiconductor will introduce a line of five 16-kilobit × 4 SRAMs, implemented in 1-micron CMOS, capable of access speeds as fast as 12 ns. The SRAMs follow by one month the debut of the company's first product line of standard logic devices, and by two weeks its introduction of high-speed first-in first-out (FIFO) memories.

The new SRAMs are designed for the fast-access primary and secondary cache requirements of high-performance RISC- and CISC-based systems, said Sunneel Rajpal, director of marketing at Quality Semiconductor, Santa Clara, Calif.

"These SRAMs are targeted at systems with clock rates of at least 25 MHz," he said. "Our fast CMOS process lets us add value through performance

[to page 22]

...This Is Now!



New **10ns,** *16Kx4 Cache SRAM*

Remember last May when 33-MHz seemed incredibly fast? That's when Quality delivered 12ns 16Kx4 SRAMs for ultra-fast cache designs.

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Our 1-micron QCMOS process means low power and high density, and our 6-T cell design eliminates static hold and adds reliability over 4-T and BiCMOS designs.

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Phone: (408) 986-1700 FAX: (408) 496-0773

Article shown was published in Electronic Buyers News, May 7, 1990

CIRCLE 120

VIRTUAL-GROUND IC, IN A TO-92, LETS YOU RUN A SINGLE-SUPPLY OP AMP OFF 5 V AND AMPLIFY PLUS/MINUS INPUT VOLTAGES WITHOUT CLIPPING.

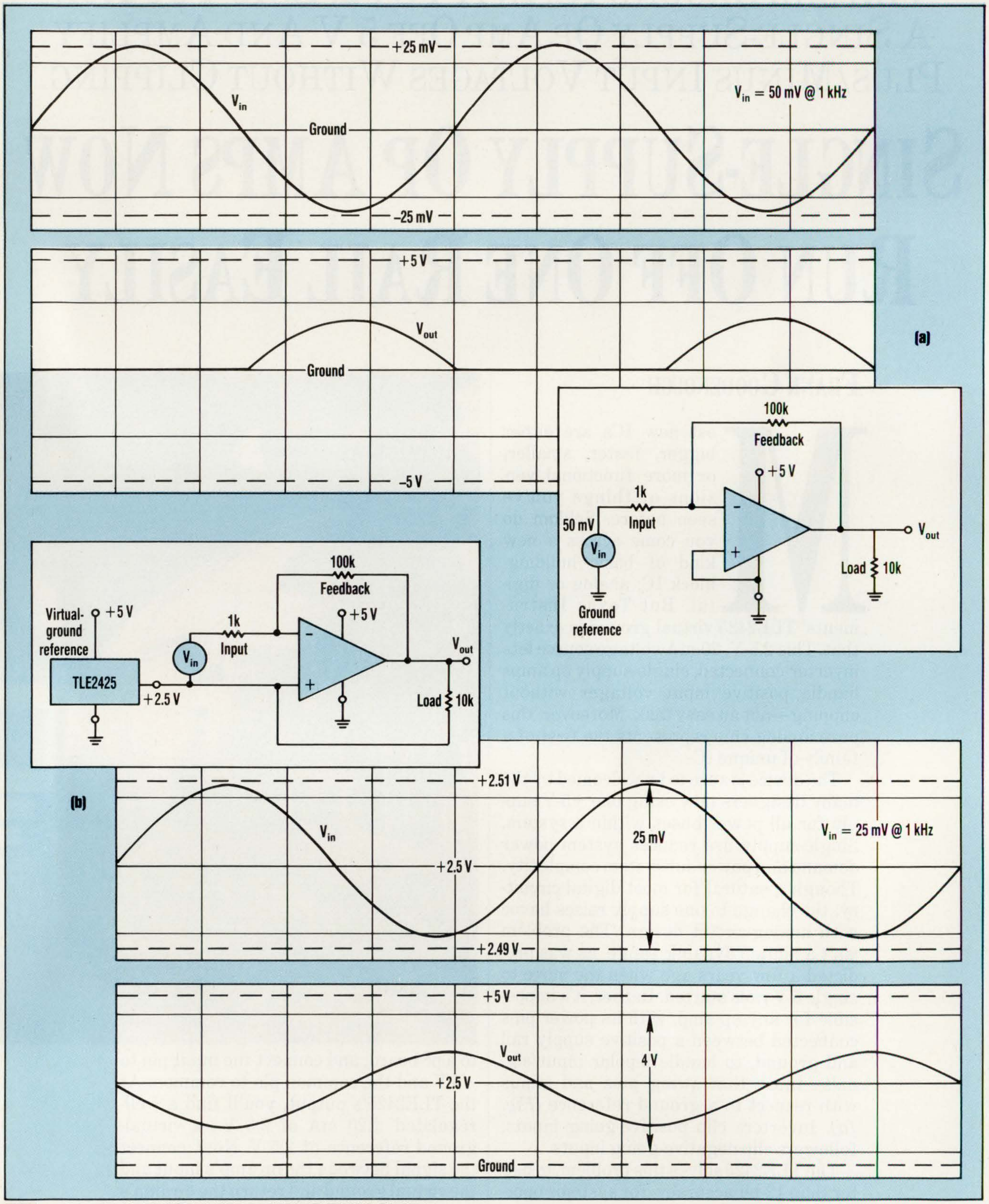
SINGLE-SUPPLY OP AMPS NOW RUN OFF ONE RAIL EASILY

FRANK GOODENOUGH

Most new ICs are either bigger, faster, smaller, or more functional versions of things you've seen before. Seldom do you come across a new kind of basic building-block IC, analog or digital. But Texas Instruments' TLE2425 virtual ground is exactly that. This 2.5-V, 20-mA voltage source lets inverter-connected, single-supply op amps handle positive input voltages without clipping—not an easy task. Moreover, this pure analog chip represents the first of a family of unique ICs.

The device is sure to be welcomed by the many designers now using one +5-V supply for all power buses within a system. Single-supply use reduces system power demand and power subsystem complexity. Though a natural for most digital circuitry, the change to one supply raises havoc with analog-circuit design. The problem isn't a limited dynamic range, as was predicted a few years ago when the move to single 5-V rails started. Rather, it's impossible for any op amp, with its power pins connected between a positive supply rail and ground, to handle bipolar input signals—those that swing plus and minus with respect to a ground reference *(Fig. 1a)*. Inverters clip positive-going inputs; followers clip negative-going inputs.

The TLE2425 solves this problem, to better than 12-bit accuracy, for systems operating from a single +5-V supply, handling signals between 0 and +5 V. Just add the simple, three-terminal, TO-92-packaged IC to a pc board, and connect the input pin to +5 V and the common pin to common. At the TLE2425's output, you'll find a well-regulated ±20 mA of 2.5 V—a virtual-ground reference of 2.5 V. Now, connect the signal between the op amp's input and the virtual ground and return the op amp's load resistor to it as well *(Fig. 1b)*. With the op amp set for a closed-loop gain of 100, a 25-mV input sine wave produces a clean



1. OPERATING IN THE INVERTING MODE, all positive input voltages with respect to the ground reference for a single-supply op amp are clipped (a). But with a virtual-ground reference, such as the TLE2425, at one-half the supply voltage (in this case, 2.5 V), the op amp handles input voltages both positive and negative relative to the new ground (b).

2500-mV output, with overhead left for larger output swings.

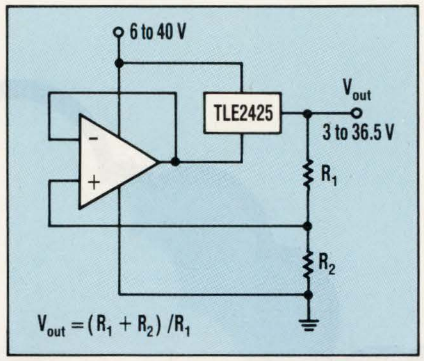
Linear-IC application and design engineers are most likely thinking to themselves "How many times have we shown a customer how to build a circuit to perform that function using an additional op amp and/or discrete parts?" In fact, this simple IC replaces any one of a family of "home-grown" virtual grounds, ranging from a couple of resistors and a capacitor to an additional op amp, a precision reference, a resistor, and a capacitor *(see "Home-grown grounds" p. 60)*. However, the TLE2425 eclipses them on performance, power, design time, and pc-board area. And at just $0.69 each in thousands, it surpasses them on cost too (unless transistors, resistors, and capacitors come free).

In general, applications for the chip range from 5-V TTL and CMOS digital systems that need a few op amps (for example, to condition a signal going to an analog-to-digital converter), to a pure analog system that must work from a single +5-V rail. An example of the latter might be portable instrumentation running off a 6-V battery, or automotive test equipment working in "cold-crank" conditions. The IC will most certainly find lots of homes as analog glue in mixed-signal systems.

Stiff Family

As noted earlier, the TLE2425 is the first of a family of virtual grounds. It will be followed over the next six months by devices for 9- and 12-V systems, putting out 4.5 and 6 V, respectively. All of these grounds are built on TI's 44-V Excalibur complementary process and may operate connected across any potential between 0 and 40 V. As long as the input voltage is greater than four, the output (the voltage between the output pin and the common pin) will be a stiff (well-regulated) 2.5 V. One family member is a general-purpose "rail-splitter" whose output is one-half the input voltage.

The TLE2425 also comes in 8-pin plastic and ceramic (military temperature range) DIPs, and 8-pin SOICs. By year's end, it will be available in the 3-pin SOT-89 package. In addition, there will be feedback nodes brought out to the extra pins of the 8-pin packages so you can add controlled, current-boosting circuits.

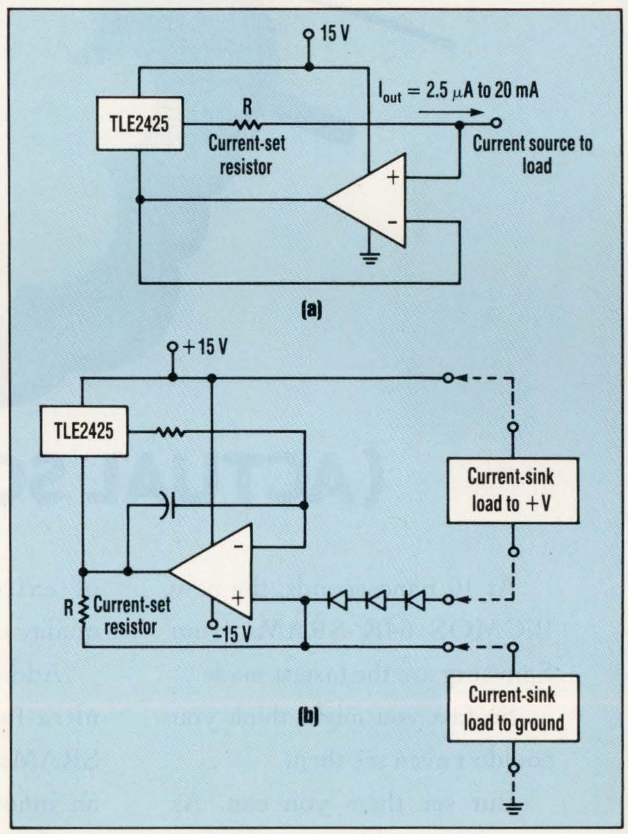


2. BY ADDING AN OP AMP and a couple of resistors to a TLE2425 virtual ground, you can have a programmable 3-to-36-V precision, 20-mA, voltage source.

The TLE2445 essentially consists of a precision reference buffered by an op amp with high open-loop gain. The op amp provides incredible line and load regulation relative to similarly priced 2.5-V references. To start, under no-load conditions at 25°C, the output voltage is initially 2.5 V ±20 mV. And it stays within ±30 mV over temperature (all specifications are maximums or minimums over the full commercial temperature range, unless noted otherwise). Rejection of 1 V pk-pk of 120-Hz ripple on the 5-V input typically runs 80 dB at 25°C.

With input voltages not just between 4.5 and 5.5 V (which could be expected), but between 4 and 40 V, the output changes no more than 25 μV. Load regulation is just as good. Either sourcing or sinking 0 to 10 mA, the output stays within 160 μV at 25°C, and within 250 μV over temperature. Sourcing and sinking 20 mA, the output stays within 450 μV at 25°C. Output impedance is typically 0.225 Ω at 25°C. This performance holds while operating with a supply current of just 250 μA. Noncumulative output drift for 1000 hours is typically under 15 ppm.

Output response, while not blazingly fast, is significantly faster than the typical references available. The output settles back to within 0.1% of its 2.5 V in under 115 μs for a ±10-mA output transient while driving 100 pF. A return to 0.01% of 2.5 V takes less than twice that. At turn-on time (applying 5 V to the input), the output is typically within 0.1% of 2.5 V in 125 μs, and within 0.01% in 210 μs. Response for an input step from



3. THE TLE2425 PLUS AN OP AMP can build precision current sources (a) and sinks (b) covering a range from 2.5 μA to 20 mA. A single resistor, R, sets the current. The sources' compliance voltages approach the positive rail. The current sink requires a split supply.

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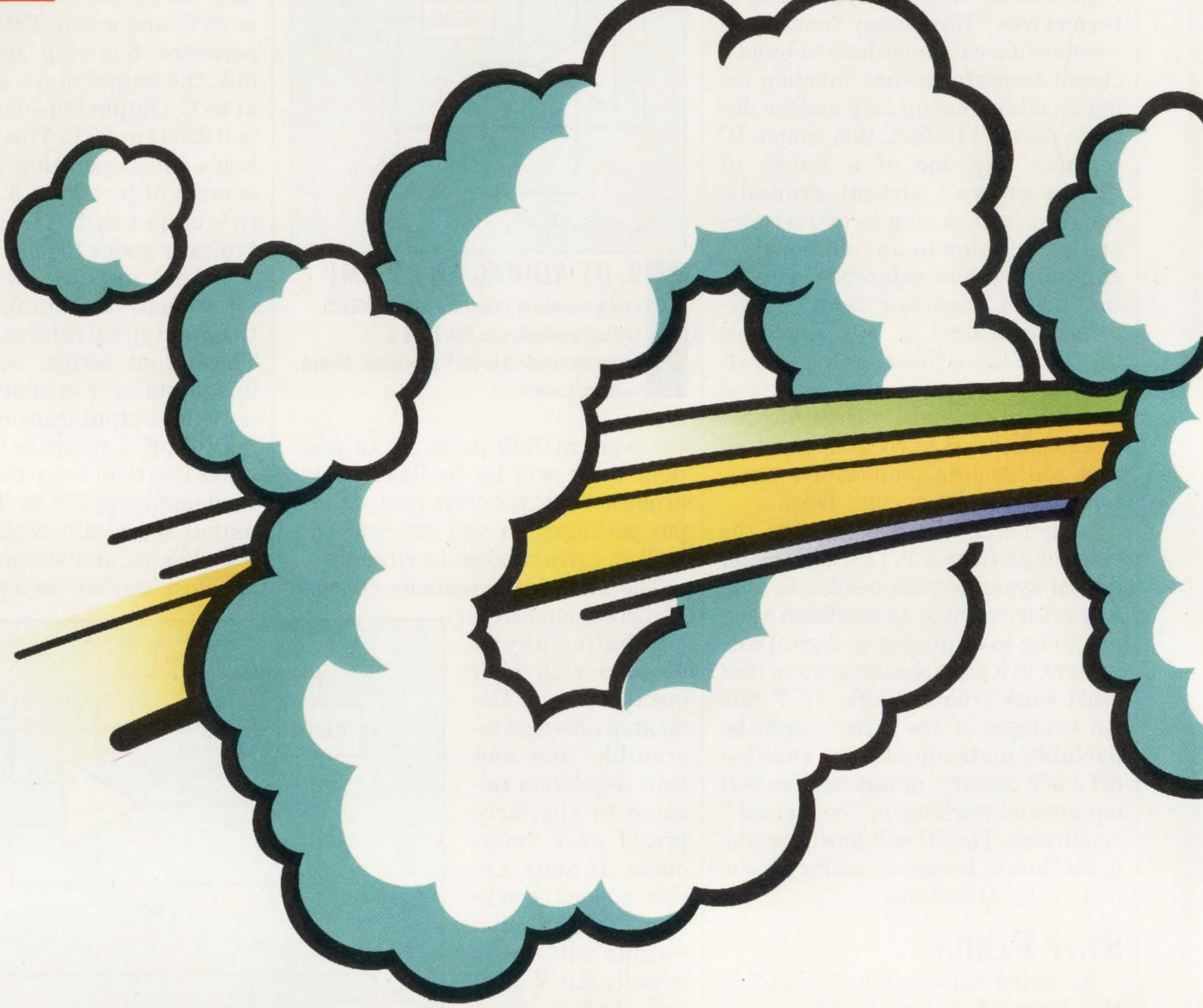

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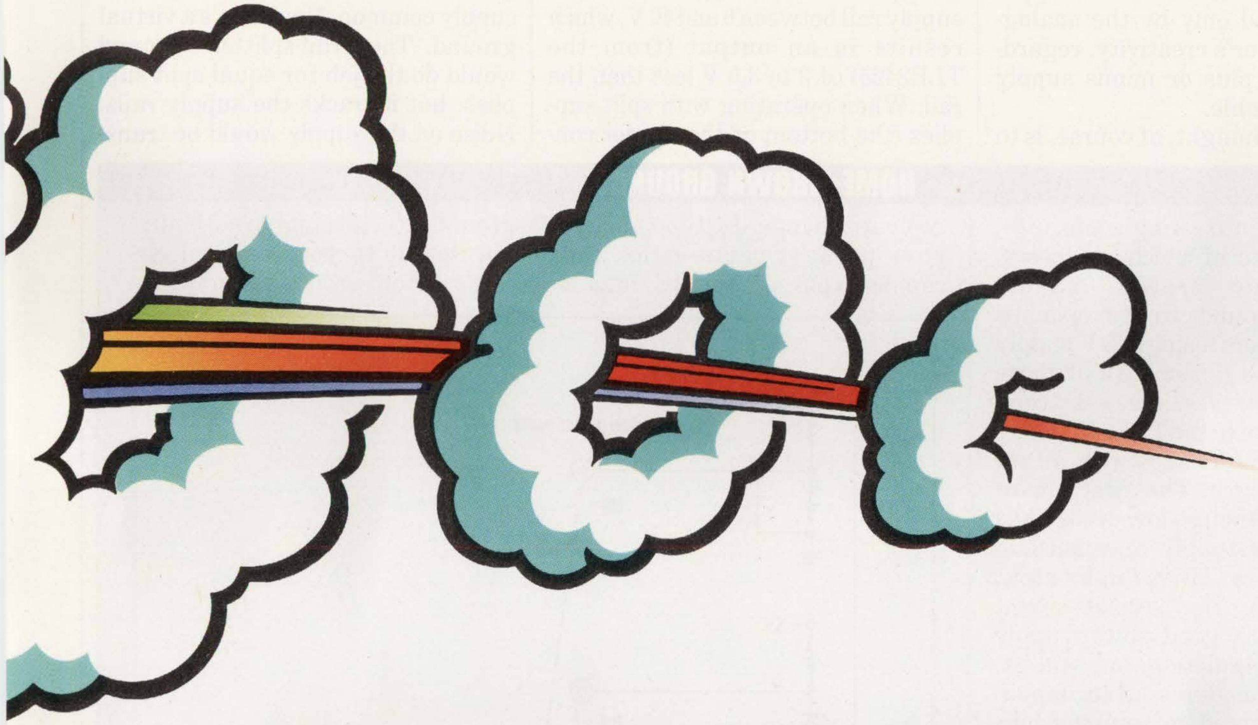

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CIRCLE 132

4.5 V to 5.5 V is under 12 μs to 0.1%, and under 30 μs to 0.01%.

Though outside of single-supply systems, these virtual grounds won't become as ubiquitous as the 555 timer IC. Their price, size, linearity, and low power lend them to applications limited only by the analog-circuit designer's creativity, regardless of what plus or minus supply rails are available.

Your first thought, of course, is to use them as a fixed or variable precision, 20-mA reference or voltage source. Adding one op amp (there's always a couple of those hanging around on a pc board) creates an extremely versatile circuit *(Fig. 2)*. One example is to operate with a single supply rail between 6 and 40 V, which results in an output (from the TLE2425) of 3 to 3.5 V less than the rail. When operating with split supplies (the bottom of the divider connects to the negative rail), the circuit provides output voltages ranging between a low (the negative rail, plus 3 V), and a high (the positive rail, minus 3 V). The circuit can build a stiff, noise-free, floating, zero-volt ground that's isolated from power-supply common. Now that's a virtual ground. The "rail-splitter" ground would do the job for equal split supplies, but it tracks the supply rails. Noise on the supply would be trans-

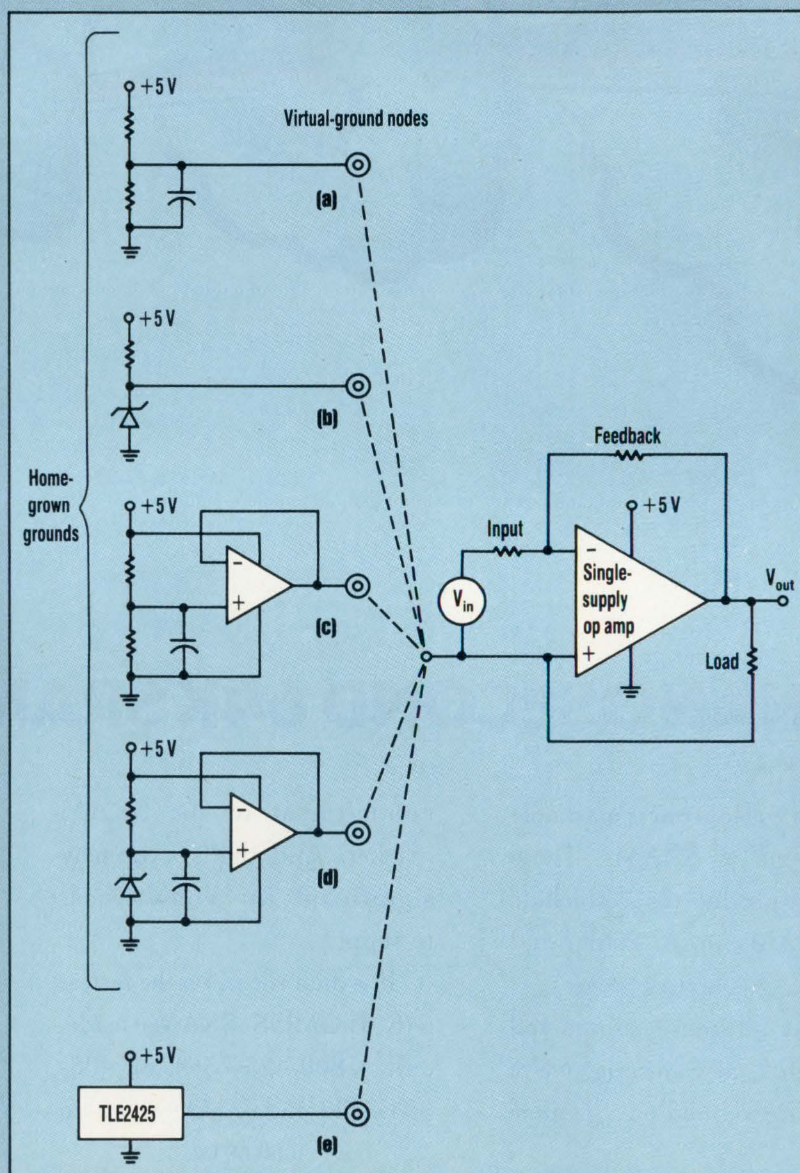
HOME-GROWN GROUNDS

Various simple circuits, four of which are shown, now provide virtual grounds to help op amps that run from a single 5-V supply rail *(see the figure)*. All of these circuits, however, have shortcomings relative to the TLE2425 virtual-ground IC. To start with, all are power hungry. The first circuit *(part a)*, although low in cost, has poor power-supply rejection and poor load regulation (high output impedance). The second circuit *(part b)* has good power-supply and load regulation, but still exhibits excessive source impedance, is limited to sourcing current, and is more expensive.

The third and fourth circuits *(parts c and d)*, which are essentially the first circuit plus an op-amp buffer and a Zener diode, offer good load regulation (low source impedance). However, power-supply rejection remains poor. Furthermore, both circuits are high in cost and take up a significant amount of pc-board space. The addition of the op-amp buffer, while offering good supply and load regulation, raises cost and pc-board area further.

A single TLE2425 on the other hand, offers significantly superior line and load regulation, lower dc and ac output impedance, and with the exception of the RC network, uses about 1/10 the power *(part e)*.

If you presently use any one of the four schemes shown, switching to the TLE2425 in its tiny TO-92 package is easy, and requires no board change. Just don't insert your present parts—stick the common pin of the IC into a ground hole, its input to +5 V, and the output to your original circuit's virtual-ground node.



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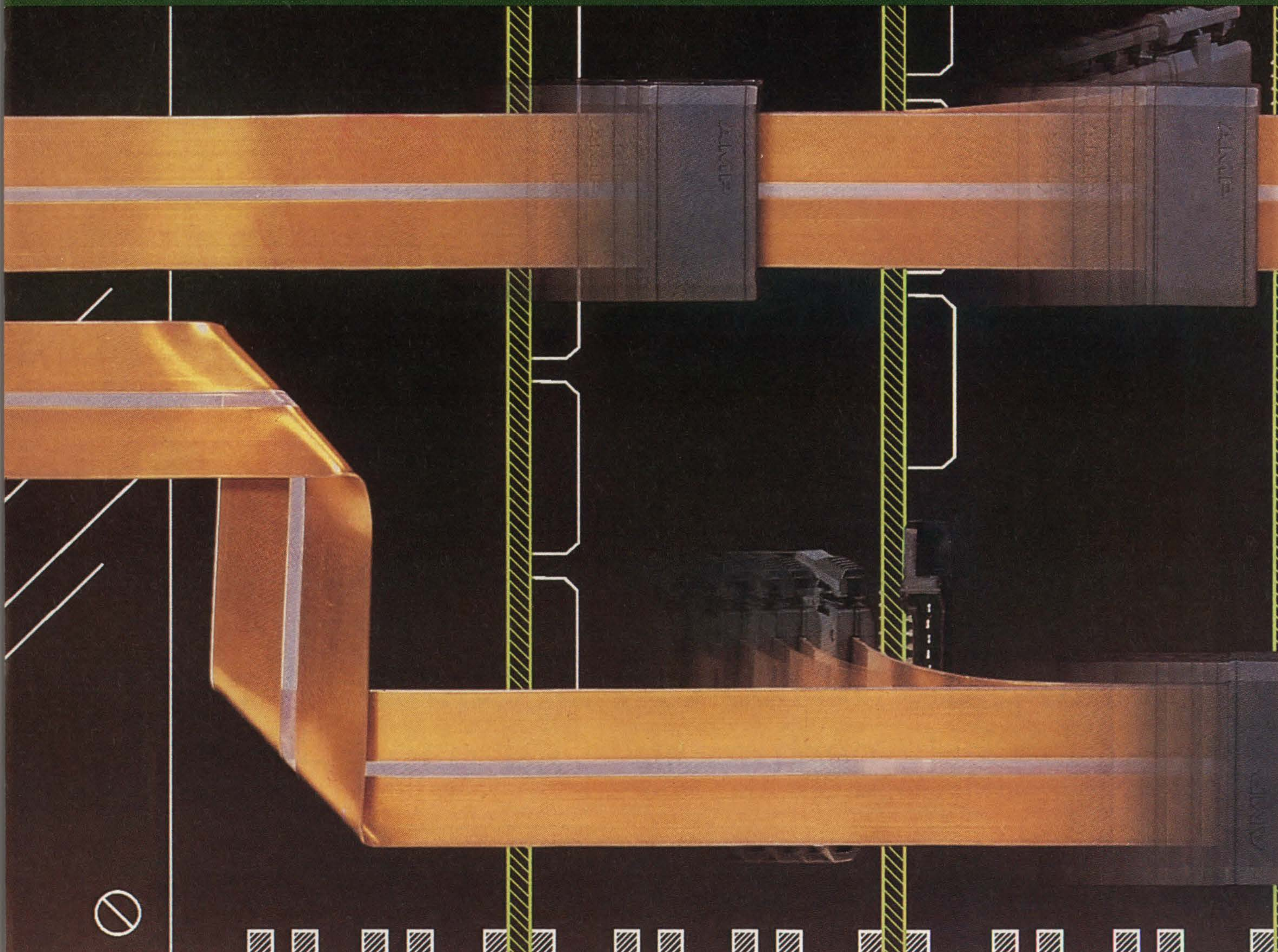

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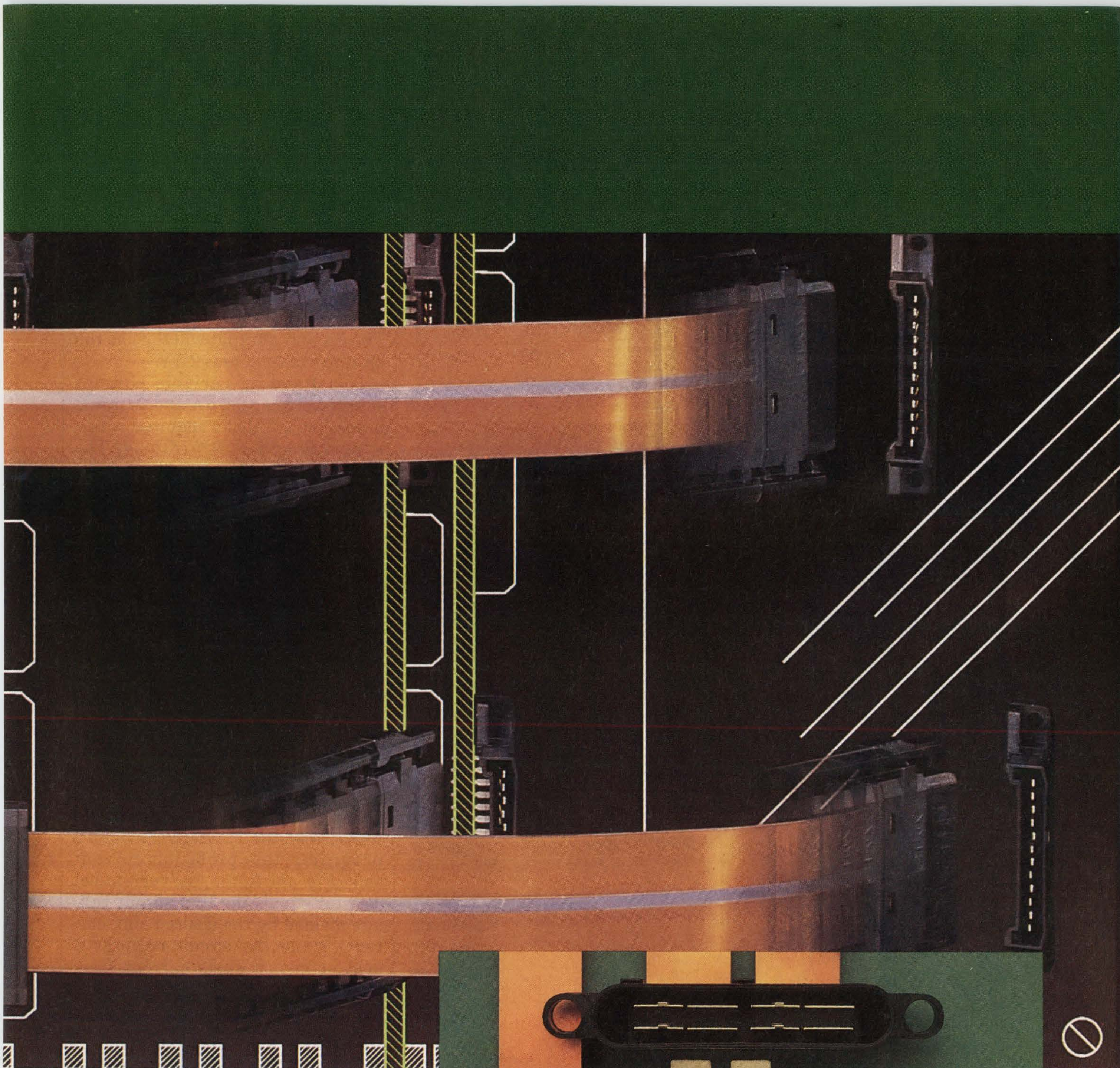
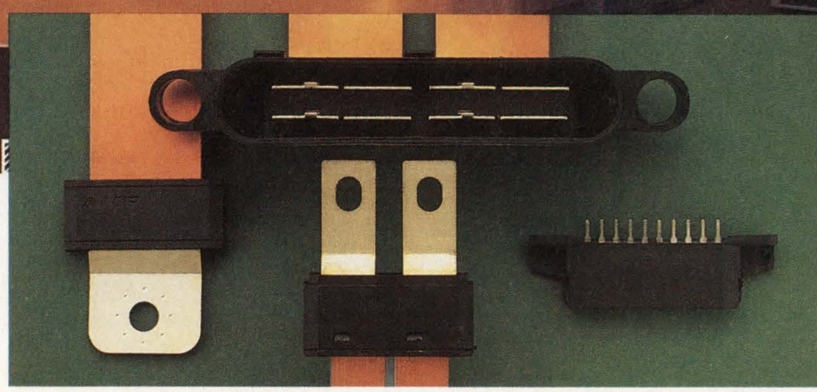




ferred to the output. That too will be remedied in future devices.

The chip makes an excellent level shifter. The only requirement is that the common pin of a TLE2425 be connected to the output of an op amp (or other low-impedance signal source). The ground's output will thus be the op amp's output, plus 2.5 V.

If a fixed or variable current source between 0.2 μA and 20 mA is necessary, all that's required is one op amp plus a TLE2425 *(Fig. 3a)*. The current is set with current-set resistor R, which is merely the output voltage of the IC divided by the desired current.

The circuit's compliance voltage is the supply rail minus 6 V. A CMOS op amp, such as the TLC271, is recommended due to its low supply current (50 μA) and because its common-mode voltage can include the negative rail.

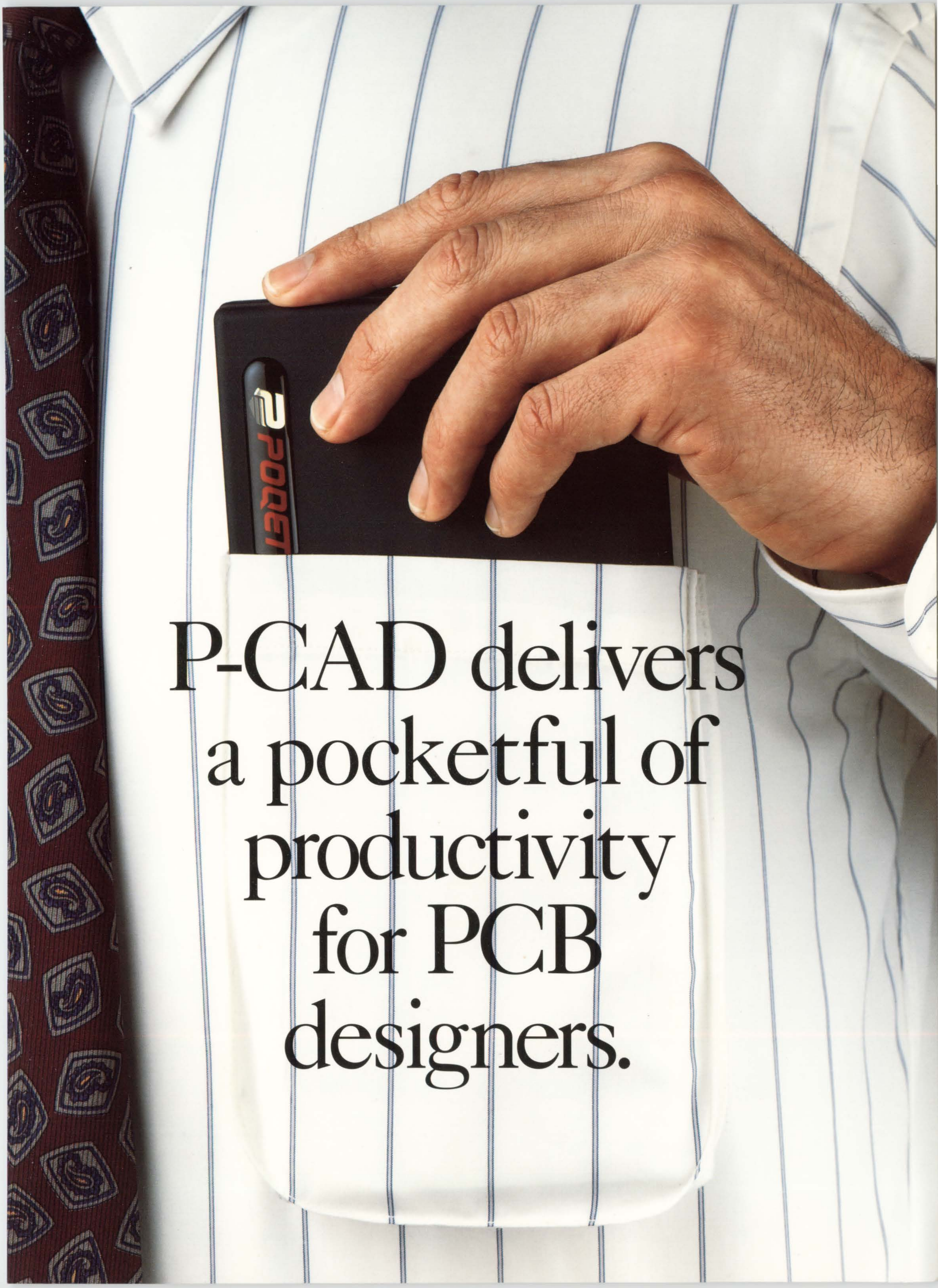
A pair of TLE2425s connected as current sources, plus a pair of op amps, can be used to build a number of 4-20-mA current loops in which both TLE2425s excite sensors and amplify the signals from them. Alternatively, the TLE2425 can build a programmable precision current sink *(Fig. 3b)*. Again, the current-set resistor equals the IC's output voltage divided by the desired sink current. While the circuit requires a split supply, it sinks current from loads connected to either the positive supply or ground.□

PRICE AND AVAILABILTY

The TLE2425 and its future relatives will be available in commercial, industrial, and military models. Present and future packages include the TO-92 (now called the 3-lead TO-226AA), plastic and ceramic 8-pin DIPs, 8-pin plastic SOICs, and the tiny, 3-pin, SOT-89. In quantities of 1000, commercial-grade TLE2425s in the TO-226AA and the 8-pin SOIC go for just $0.69 each. Small quantities are available from stock.

Texas Instruments Inc., Literature Response Center, P.O. Box 809066, Dallas, TX 75380-9066; Mark Granahan, (214) 997-3389. **CIRCLE 511**

HOW VALUABLE?	CIRCLE
HIGHLY	529
MODERATELY	530
SLIGHTLY	531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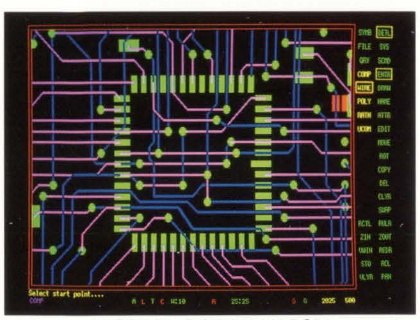

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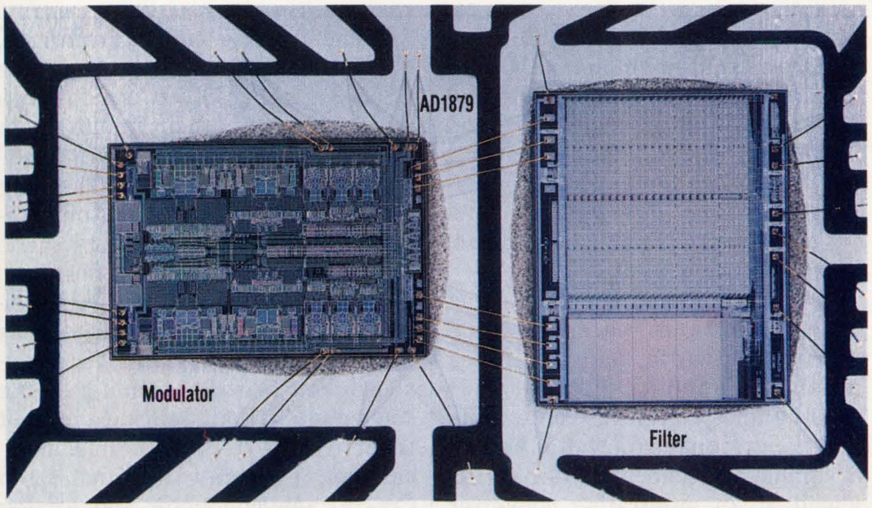


SOURCE: ANALOG DEVICES

FRANK GOODENOUGH

AN ARRAY OF ADCs OFFERS SIGNAL BANDWIDTHS FROM 500 HZ AT 24 BITS TO OVER 5 MHZ AT 14 BITS, WITH NO LIMITS IN SIGHT.

HIGH-RESOLUTION ADCs UP DYNAMIC RANGE IN MORE APPLICATIONS

Driven by applications as diverse as sensing seismic signals and military radar, high-resolution analog-to-digital converters (ADCs) have seen a dramatic upswing in their performance levels over the past several years. Satisfying these applications are improvements in ADC processing, packaging, and architectures (circuit design). Such advances in ADC performance were not previously deemed, nor even dreamed, possible just five years ago. Unlike most ICs, which are built for existing applications, evolving higher-performance (wider-dynamic-range) ADCs are actually technology-driven. Build a faster and/or higher resolution device and there will be somebody who needs it.

It's hard to believe that several years ago, ADC-design gurus on an evening panel session at the International Solid State Circuits Conference (ISSCC) pessimistically stated that practical (economic), and in some cases theoretical, limits of ADC performance were reached. They've since been proven unequivocally *wrong*. Already, monolithic ADCs are replacing top-performing multichip hybrids while offering superior performance at lower cost. And more are coming. We're truly in the midst of a major explosion in high-resolution ADC technology, where several architectures are vying with each other for sockets.

Though the performance of today's high-resolution monolithic ADCs is made possible by technological advances, most of these devices have been market-driven. In fact, they can be considered application-specific devices. That is, they were developed to digitize a signal from a unique source. Still, many designers have found that these ADCs also perform well in a multitude of other applications.

Most of these advanced converters have designs based on delta-sigma and multipass architectures, both relatively new. *(see the table and Fig. 1).* These new ADCs are challenging older and even new converters based on the entrenched successive-approximation-register (SAR) and integrating architectures. The delta-sigma converter is everywhere, handling signals from dc to 1 MHz and offering resolution from 12 to 24 bits. The multipass converter, originally employed in hybrid form to handle signals above 250 kHz, has moved into the general-purpose arena in IC form to handle signals from 50 to 100 kHz at resolutions of 14 to 16 bits. The hybrids have reached sampling rates of 10 MHz at 14 bits and 1 MHz at 16 bits, rates that are expected to keep climbing.

One thing is clear, regardless of the architecture employed: In the future, the number of general-purpose converters will dwindle while those aimed at linking with a particular type of signal, or sensor, will predominate. For example, while ADCs designed for digital audio find other applications, particularly as the I/O for IC digital-signal processors, their basic operation and specifications must first meet digital audio standards.

In the near future, more low-cost devices dedicated to specific applications will appear. One such example is the Analog Devices AD7711, which carries a pair of 200-μA current sources just to excite resistance temperature detectors (RTDs). In fact, some high-channel-count systems employing a multiplexer followed by an expensive high-speed 16-bit hybrid achieve superior performance by switching to low-cost, 14-bit ADCs per channel and followed by digital multiplexing. The technique is particularly useful when the signals come to the multiplexer from distant sites through noisy environments. The low-power 14-bit ICs can be located at the signal source.

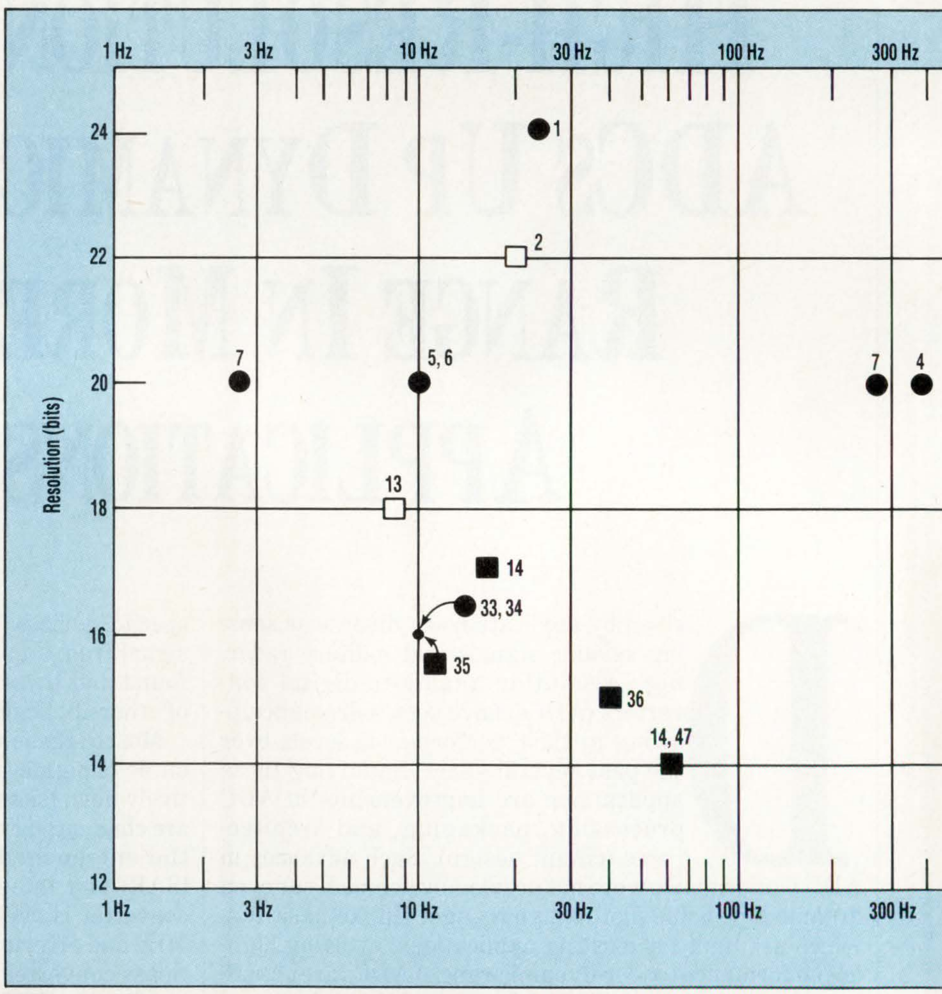
Most of the converters in the table are very recent—many have appeared just this year. The AD1879, Analog Devices' 18-bit two-chip audio ADC, was the subject of an ISSCC paper in February, and was announced formally at the Audio Engineering Society meeting the following week in Paris *(see opening figure)*. Its 106-dB dynamic range is 10 dB greater than other audio converters in one IC package.

There are four dominant ADC architectures: the multislope integrator, the delta sigma, the SAR, and the multipass circuit *(Fig. 2)*. The majority of new converters (particularly those with resolutions above 14 bits) employ some form of autozero and/or autocalibration techniques to ensure accuracy both at 25°C and over time and temperature.

The integrating converter has existed for years, and until the advent of the delta sigma, it owned the precision dc-measurement arena (14 to 22 bits at dc). Because its input signal must remain at a constant dc level during conversion, it lacks the ability to handle even slowly changing signals. However, it effectively integrates high-frequency noise and rejects power-line noise.

On the other hand, the delta-sigma converter samples the input over its signal bandwidth, and eliminates aliasing through its digital filter. It thus handles signals from dc to its maximum signal bandwidth. Adding a sample-and-hold amplifier (SHA) ahead of an integrating converter lets it handle signals of a few hertz. But an antialiasing filter is still needed—and no one makes SHAs, or filters, that can do the job.

While offering many advantages, early delta sigmas, such as the CS5503 and the CS5501, had to forgo multiplexers on their inputs (both are now also sourced by Analog Devices as the AD7701/03). The long settling times (hundreds of milliseconds) of their digital filters made multichannel systems impossible. Though the brick-wall low-pass digital filters in these early delta sigmas offer performance that's truly impossible with analog techniques, the converters' throughput delays limit them to converter-per-channel applications. Two new families from Crystal Semiconductor and Analog Devices use advanced filters, with 2-to-80-ms delays, depending on clock frequency and programming *(More details will be in the April 25 issue*



1. HIGH-RESOLUTION ANALOG-TO-DIGITAL CONVERTERS run a performance gamut that provides 24-bit conversions on signals beyond 1600 Hz, and 14-bit conversions on signals beyond 5 MHz.

of ELECTRONIC DESIGN).

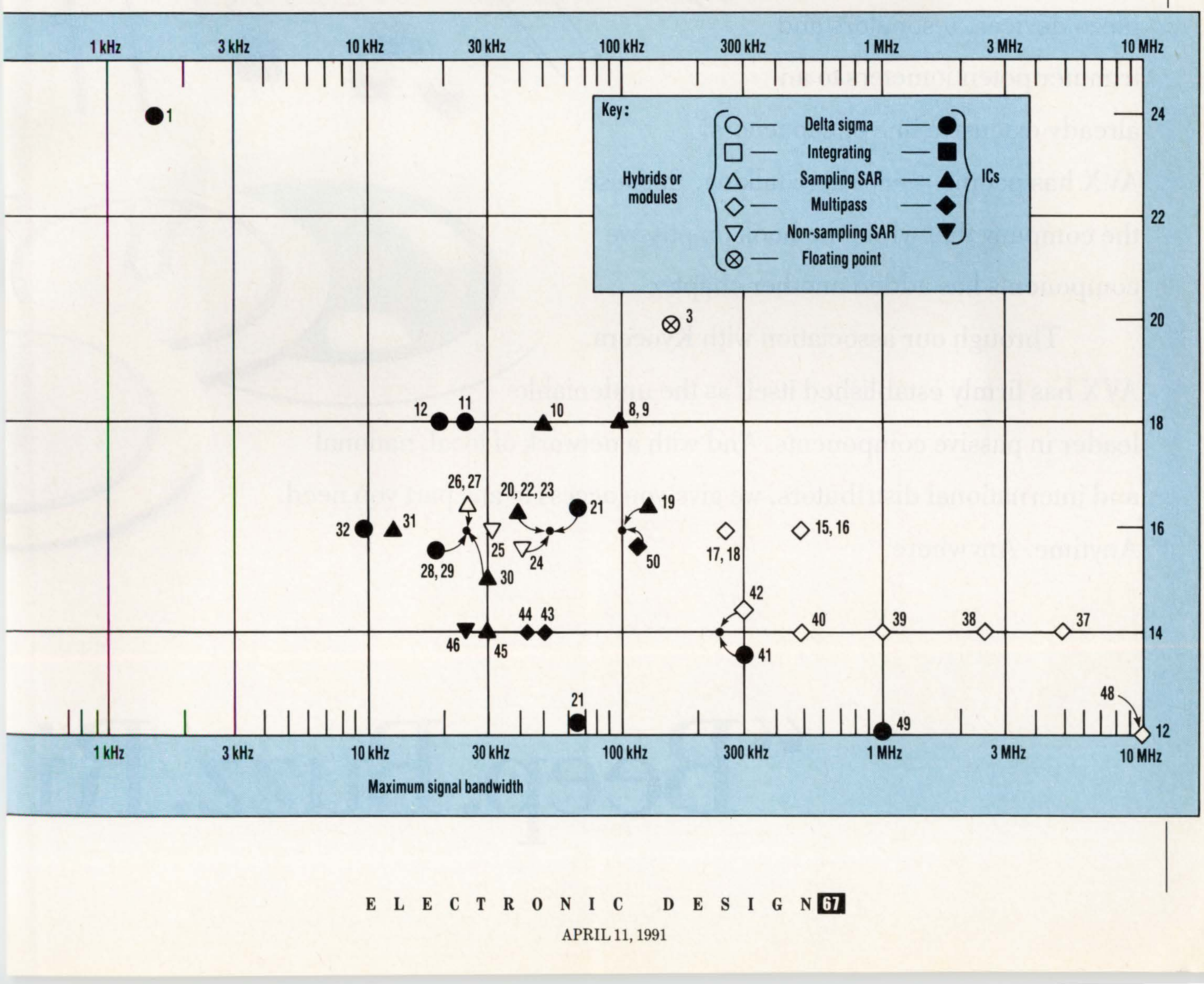
With the exception of the modular Analog Devices 22-bit AD1175 and 18-bit AD1170, all of the integrating converters are ICs and require external precision resistors and polypropylene, polystyrene, or teflon capacitors. These add cost and take up board space. On the other hand, the die size (at this time) of an integrating converter is significantly smaller than that of the delta-sigma unit, which is refelected in a lower cost *(Fig. 1, again).*

With its inherent linearity and its ability to sample ac signals and eliminate aliases, the delta-sigma converter has a unique hold on the very-high-resolution, low-frequency ac field (0.2 Hz to 2 kHz, 20 to 24 bits). The CS5322/23 and AD7710 are shown at two locations in the figure to illustrate their programmable signal bandwidth (although changing any delta sigma's clock frequency changes its signal bandwidth, with the bandwidth tracking the clock directly).

LONG LIVE THE SAR

The SAR converter, Bernie Gordon's creation, has been around for over 30 years. Today, hybrid SARs, such as the 16-bit AD1377 and ADC700 from Analog Devices, own the 12-to-16-bit field. Here, many channels of dc data are multiplexed and digitized at high speed (most 16-bit devices are only 14-bit accurate). And until recently, when used with a SHA (mandatory for signals beyond dc), these hybrid SARs have also owned the 14-to-16-bit ac arena, handling signals from dc to about 100 kHz (and at 12 bits to several megahertz). Monolithic 14-to-18-bit sampling SARs (SARs with an integral SHA), like the Burr-Brown PCM1750 and the Atmel AT76, are now challenging the hybrids.

In turn, these SAR ICs are being challenged by sampling, multipass ICs, such as the 16-bit-accurate Analog Devices AD7884, the 14-bit Analog Devices AD679/779 and AD7871/72, and a rash of 16-bit delta-sigma converters as well. Compared with the delta sigmas, the easily multiplexed SARs and multipass converters offer the ability to "allocate" each channel's bandwidth when dealing with various signals from many sources. That is, they can



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A SAMPLING OF HIGH-RESOLUTION ANALOG-TO-DIGITAL CONVERTERS

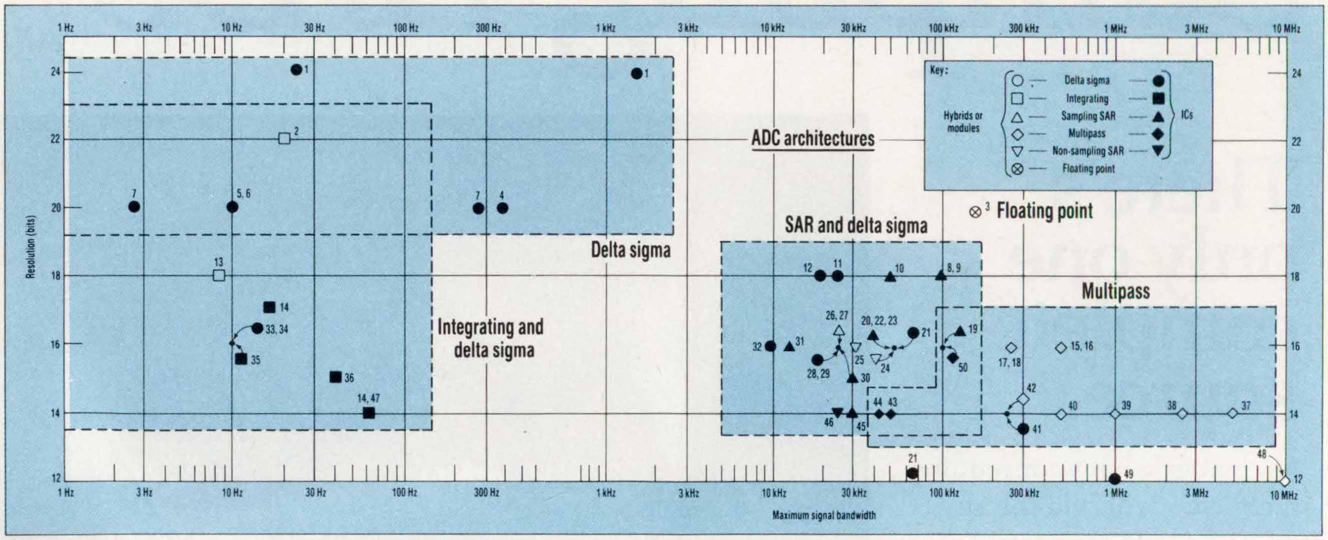
Company	Model	Sampling rate (1)	Signal bandwidth (2)	Architecture	Package	Price in 100s ($)
24 bits						
1) Crystal	CS5322/23	na	26-1650 Hz	Delta sigma	2 ICs	269
22 bits						
2) Analog Devices	AD1175	20 Hz	ns/dc	Integrating	Module	1175
20 bits						
3) Micro Networks	MN5420	320 kHz	160 kHz	Floating point	Module	1295
4) Crystal	CS5324	na	500 Hz	Delta sigma	IC	217
5) Crystal	CS5506/08	20 Hz	10 Hz	Delta sigma	IC	18/15
6) Crystal	CS5503	na	10 Hz	Delta sigma	IC	28
7) Analog Devices	AD7710/11/12	na	2 to 200 Hz	Delta sigma	IC	15/16/14
18 bits						
8) Burr-Brown	PCM1750	200 kHz	100 kHz	SAR (dual)	IC	37
9) Burr-Brown	DSP101/102	200 kHz	100 kHz	SAR (single/dual)	IC	19/25
10) Atmel	AT76	100 kHz	50 kHz	SAR (dual)	IC	25
11) Crystal	CS5328/29	na	23 kHz	Delta sigma (d)	IC	84 to 97
12) Analog Devices	AD1879	na	20 kHz	Delta sigma (d)	IC	50
13) Analog Devices	AD1170	9 Hz	ns/dc	Integrating	Module	98
17 bits						
14) Harris (17.3 bits)	HI-7159	15 Hz 60 Hz	ns/dc 200,000 count ns/dc 20,000 count	Integrating	IC	15
16 bits						
15) Analogic	ADC4344	1 MHz	500 kHz	2-pass	Module	750
16) Sipex	SP9490	1 MHz	500 kHz	3-pass	Hybrid	735
17) Analog Devices	AD1382	500 kHz	250 kHz	3-pass	Hybrid	595
18) Datel	ADS-930	500 kHz	250 kHz	2-pass	Hybrid	337
50) Analog Devices	AD7884/5	200 kHz	100 kHz	2-pass	IC	45
19) Burr-Brown	PCM78	200 kHz	100 kHz	SAR	IC	40
20) Analog Devices	AD1876	100 kHz	50 kHz	SAR	IC	34
21) Motorola	DSP56351	na	45 kHz	Delta sigma	IC	31
22) Crystal	CS5126	100 kHz	50 kHz	SAR	IC	40
23) Crystal	CS5101	100 kHz	50 kHz	SAR	IC	58
24) Analog Devices	AD1377	100 kHz	ns/dc	SAR	Hybrid	116
25) Burr-Brown	ADC700	58 kHz	ns/dc	SAR	IC	74
52) Fujitsu	MB87020	50 kHz	25 kHz	SAR	IC	10
26) Micro Networks	MN6400 family	50 kHz	25 kHz	SAR	Hybrid	192
27) Analog Devices	AD1380	50 kHz	25 kHz	SAR	Hybrid	126
28) Crystal	CS5326/27	na	25 kHz	Delta sigma (d)	IC	71 to 81
29) Crystal	CS5336/37/38/39	na	25 kHz	Delta sigma (d)	IC	56 to 73
30) Crystal	CS5016	50 kHz	25 kHz	SAR	IC	69
31) Crystal	CS5102A	25 kHz	12.5 kHz	SAR	IC	40
32) Crystal	CS5317	na	10 kHz	Delta sigma	IC	29
33) Crystal	CS5505/07	20 Hz	10 Hz	Delta sigma	IC	16/12
34) Crystal	CS5501	na	10 Hz	Delta sigma	IC	58
35) Teledyne	TSC500	10 Hz	ns/dc	Integrating	IC	5
15 bits						
36) Teledyne	TSC800	15-40 Hz	(ns) dc + sign	Integrating	IC	11
14 bits						
37) Analog Devices	AD9014	10 MHz	5 MHz	2-pass	Module	2800
38) Burr-Brown	ADC614	5 MHz	2.5 MHz	2-pass	Hybrid	1244
51) ILC Data Devices	ADC-00145	5 MHz	2.5 MHz	2-pass	Hybrid	950
39) Datel	ADS-942	2 MHz	1 MHz	2-pass	Hybrid	374
40) Datel	ADS-941	1 MHz	500 kHz	2-pass	Hybrid	337
41) Alcatel	(ISSCC paper)	Modulator	250 kHz	Delta sigma	IC	na
42) Sipex	SP9478	500 kHz	250 kHz	3-pass	Hybrid	385
43) Analog Devices	AD679/779	100 kHz	50 kHz	5-pass	IC	30
44) Analog Devices	AD7871/72	83 kHz	41 kHz	SAR	IC	30
45) Crystal	CS5014	56 kHz	28 kHz	SAR	IC	45
46) Harris	ICL-7115	25 kHz	ns/dc	SAR	IC	39
47) Teledyne	TSC500	60 Hz	ns/dc 20,000 count	Integrating	IC	5
12 bits*						
48) Comlinear	CLC936	20 MHz	10 MHz	2-pass	Hybrid	750
49) Stanford Univ.	(ISSCC paper)	Modulator	1 MHz	Delta sigma	IC	na
21) Motorola	DSP56351	200 kHz	66 kHz	Delta sigma	IC	31

(Numbers in bold at left of each line refer to figure 1.) na = not applicable ns/dc = non-sampling/only digitizes dc voltages d = dual

*12-bit converters are listed in the table to provide a frame of reference, because over 80% of today's general-purpose "high-resolution" ADC requirements still call for 12-bit converters. However, as lower-cost 14-bit devices become available, users are beginning to ask for them. They also represent a look at IC technology to come: "12 bits today, 14 bits tomorrow, 16 bits the day after." In addition, the Motorola DSP56351 offers two operating modes, one at 16 bits, one at 12 bits.

(1) Sampling rate for various ADC architectures
a) Sampling SARs: Maximum specified sampling rate.
b) Multipass: Maximum specified sampling rate.
c) Non-sampling SARs: Maximum throughput rate or reciprocal of conversion time.
d) Delta sigmas: Not applicable due to the range of oversampling rates.
e) Integrators: Specified conversions per second.

(2) Signal bandwidth for various ADC architectures.
a) Sampling SARs: Nyquist rate (half the sampling rate).
b) Multipass: Same as (a).
c) Non-sampling SARs: Nyquist rate assuming operation with an appropriate sample-and-hold amplifier.
d) Delta sigmas: Specified 3-dB signal bandwidth.
e) Integrators: Essentially dc.



2. TWO NOVEL ADC ARCHITECTURES, delta sigma and multipass, now challenge entrenched successive-approximation-register designs and integrating types across virtually the complete signal-frequency spectrum.

sample a thermocouple a few times a minute, an RTD a few times a second, and sample a vibration transducer hundreds, thousands, or even tens of thousands of times a second.

That's one reason there's a general consensus within the industry that 12-to-16-bit SARs with sampling will be around for a long time. Besides, "everyone" knows how to use them. On the other hand, the SAR's days could be numbered as chip designers make ADCs with other architectures "look like" sampling SARs (which is being done) and such features as signal conditioning are added. But before shedding any tears, just look at the 13-year-old 574. Even surprising its originators, it's still picking up design-ins, suppliers, features, performance, and even new footprints.

Until now, multipass ADCs with greater-than-12-bit resolution were limited to hybrids and modules designed to handle signals beyond 200 kHz. They have now successfully reached 1-MHz sampling rates at 16 bits (the Analogic ADC4344 and the Sipex SP9490) and 10-MHz sampling rates at 14 bits (the Analog Devices AD9014). And by year's end, 20-MHz, 14-bit hybrid ADCs may arrive. The general consensus within the industry feels that even the multipass architecture is running out of steam at the high end, whether it's one chip or several chips. Several new and proprietary architectures are now in development, possibly resulting in a low-chip-count, 14-bit, 30-MHz hybrid by the end of the year. There are even indications a 12-bit, 50-MHz IC can be built.

Stepping Out Fast

Keeping up with high-speed, high-resolution ADCs offers system designers a high-speed, high-resolution target. Just over six months ago, none of the 14- or 16-bit multistep devices in the table were available. The majority, including the Analog Devices AD9014, employ a two-step design in the form of two hybrids, one of them being the SHA, mounted on a small pc board.

A quick scan of the table or figure 2 shows SARs and two-, three-, and five-pass multistep devices (some ICs, some hybrids) battling it out to handle 50-kHz and higher signals at 14 to 18 bits. In fact, two new 14-bit, 5-MHz, single-package hybrids—the ADC-00145 from ILC Data Devices and the Burr-Brown ADC614—indicate technology is fast closing in on the two-package AD9014.

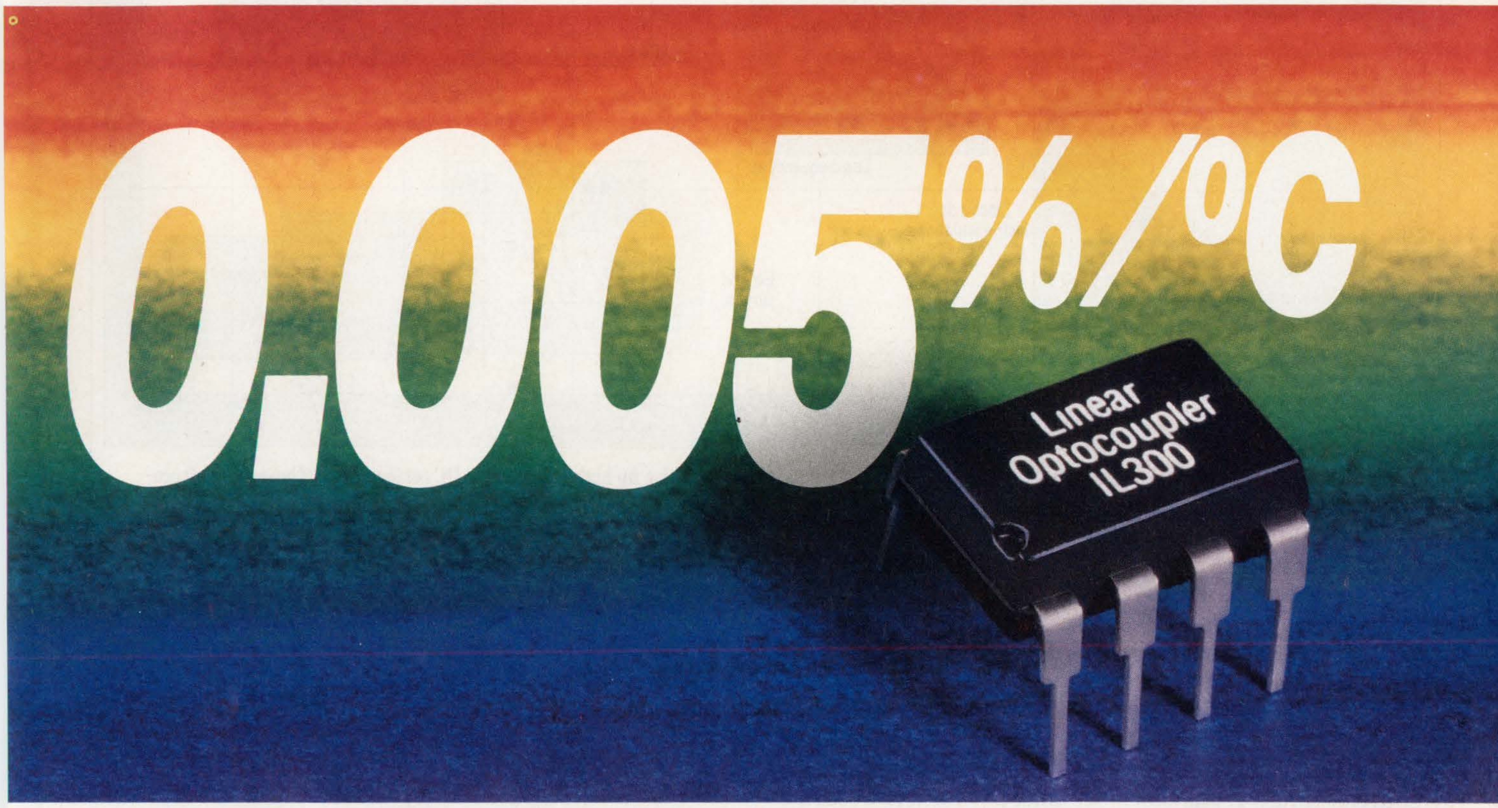
But as noted earlier, the delta-sigma converter is everywhere. In fact, if two papers at this year's recent ISSCC represent a hint of things to come, the suddenly ubiquitous delta-sigma ADC may soon even grab a slice of the multipass pie, albeit at the low end of performance. Two delta-sigma modulators were described: a 14-bit circuit with a signal bandwidth of 250 kHz and a 12-bit circuit with a signal bandwidth of 1 MHz. In fact, this ISSCC truly illustrated the impact of the delta-sigma architecture on our industry. A seven-paper session was devoted to it and a similar number of delta sigmas showed up in "systems on a chip" scattered through the conference (ELECTRONIC DESIGN, *Feb. 14, p. 51)*. A chip to monitor three-phase power lines had six of them.

One unique device should be mentioned—the 20-bit, 320-kHz sampling-rate MN5420 from Micro Networks. It has a pipelined, floating-point architecture that puts out a 16-bit digital word composed of a 12-bit mantissa and a 4-bit exponent.

Classy Classics

Since the advent of the dual-slope circuit over 30 years ago, the classic dc instrumentation field has belonged to the integrating ADC. Today, the field's denizens include virtually any dc application where wide-dynamic-range (14 bits and higher) conversion is required. It includes those where multiplexing multiple signals into a SAR isn't cost-effective or not accurate enough. While signals are easily multiplexed into integrating converters, 10 to 60 con-

SIEMENS



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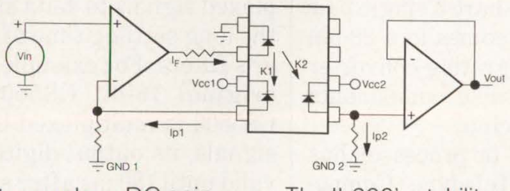

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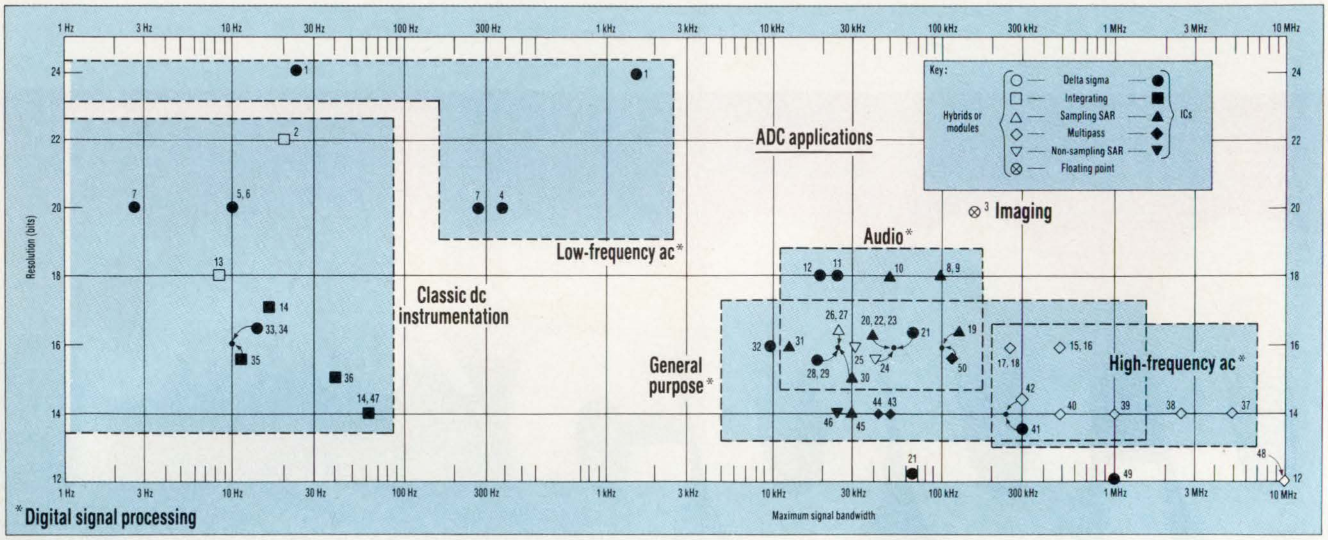


3. NEW AND OLD APPLICATIONS FOR ADCs continuously drive up high-resolution ADC performance. These range from digital audio, digital signal processing, imaging, and radio receivers, to a wide variety of sensor signals.

versions/s is the limit, depending on the resolution required *(Fig. 3)*.

Typical applications for integrators include industrial process control, medical instruments, laboratory instrumentation, and scales of all types from those used in supermarkets to ones for trucks. Signal sources range from thermocouples, RTDs, and strain gages, to pH probes and photodiodes.

The 22-bit Analog Devices AD1175 represents the highest-resolution integrator in modular form. The 4-by-5-by-1/2-in.-thick module offers the performance associated with bench instruments. Designed to link easily with a host PC, this 22-bit (4,600,000 counts, or the equivalent of 6-1/2 digits) converter guarantees an integral nonlinearity (INL) of 1 ppm of full scale and a differential nonlinearity (DNL) of ±1/2 LSB—while delivering 20 readings each second.

Who needs the AD1175's 133 dB of dynamic range? It was developed for stack-gas analysis to detect pollutants coming from power plants. Other applications include chemical analyzers, gas and liquid chromatography, and turning a PC into a high-performance digital voltmeter.

For similar applications, if you can settle for a somewhat reduced dynamic range, the 7-to-18-bit Analog Devices AD1170 offers an interesting alternative in a module. It occupies less than 20% of the AD1175's board space. Moreover, because it's based on a charge-balancing, or voltage-to-frequency-converter (VFC), circuit rather than a multislope architecture, its integration time (counting VFC pulses) can be programmed and traded off against resolution/accuracy.

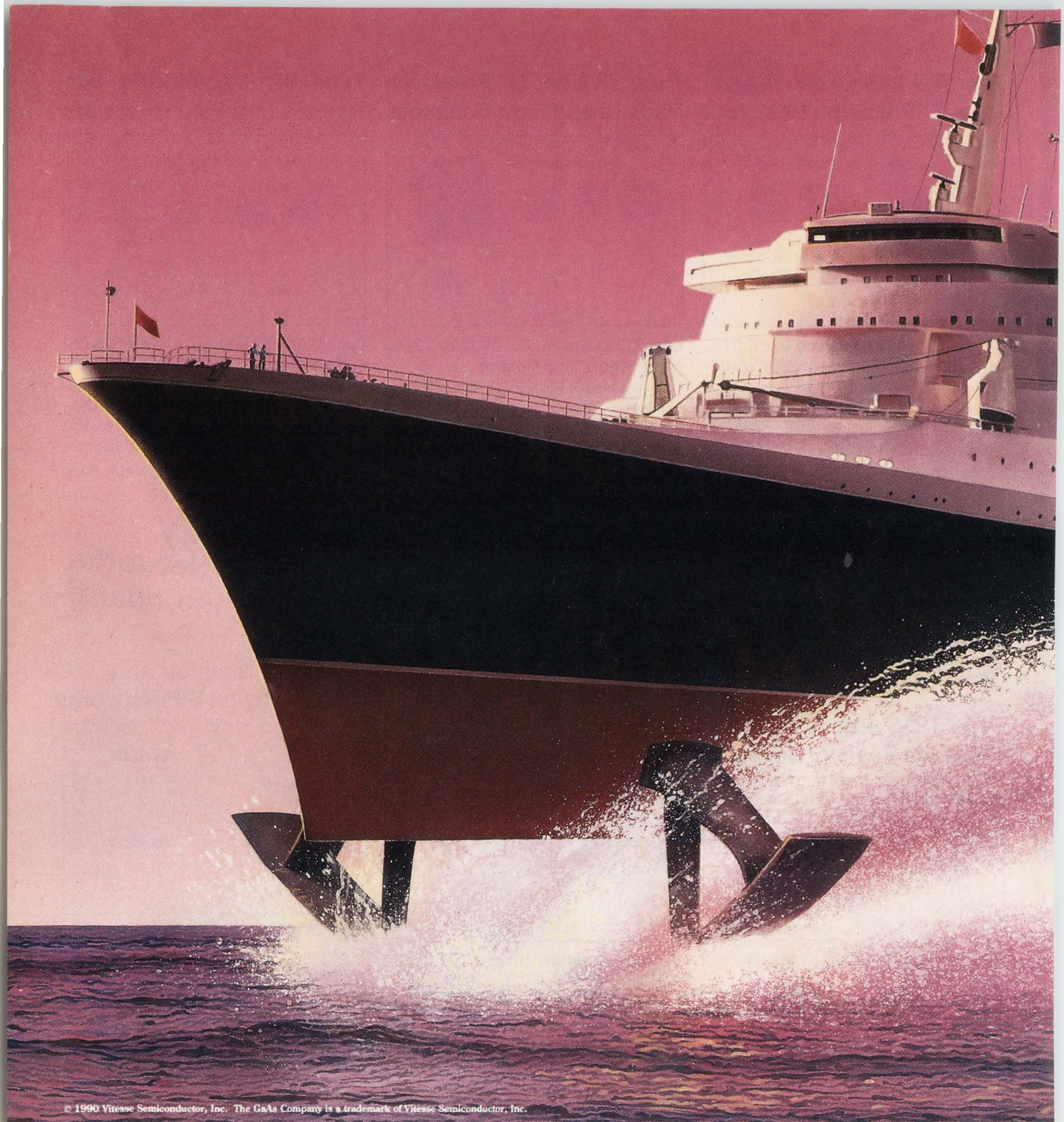
If space and cost are truly at a premium, the recently announced integrating 5-1/2-digit-plus-sign HI-7159 from Harris Semiconductor may be the best choice (ELECTRONIC DESIGN, *Jan. 10, 1989, p. 181*). The BCD machine can trade off conversion rate for resolution, plus it performs a 200,000-count conversion at 15 Hz, and a 20,000-count conversion at 60 Hz. It links a host via a serial or a parallel port, or through a universal asynchronous receiver-transmitter (UART) link. In the serial mode, up to 32 converters can share a single pair of wires. While it comes in a 28-pin DIP, like all integrating-converter ICs, precision passive components must be added off chip.

If your host PC or processor has spare time, the Teledyne Components integrating TSC500 may be the right converter. The device, which is capable of 10, 16-bit-plus-sign conversions/s, comes in a 16-pin DIP. However, it consists of just the analog front-end—the switches, op amps, comparators, and polarity-detection circuits. It also needs the off-chip passive parts. The host must provide all clocking and control functions (when the IC switches between autozero, integrate, and deintegrate modes), and must measure deintegration time (by counting clock pulses). If the host has little time available, the 16-pin-DIP TSC520 from Teledyne can be inserted between the host and the TSC500. The TSC520 performs every function previously asked of the host, which it feeds with serial data.

It isn't conceivable that these integrating converters will be displaced by the likes of the new application-specific delta-sigma converters. As noted previously, until now, users of dc-accurate delta-sigma converters have been forced to converter-per-channel operations. They haven't had the luxury of feeding multiplexed signals to delta sigmas due to the long settling time of the converter's filters. For example, if Crystal's original 16-bit CS5501 or 20-bit CS5503 is multiplexed between two signals, its output digital word isn't valid until 130 ms after switching between inputs.

SWITCHING SPOTS

Unlike leopards, two new delta-sigma families have truly changed their spots. Crystal's CS5505/06/07/08 and Analog Devices' AD7710/11/



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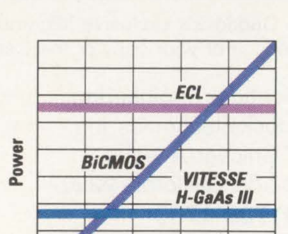

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12 are both aimed at the integrator's world. Switching from low-pass filters to comb filters, they now handle multiplexed inputs. They can provide data rates to 20 conversions/s while offering 20-bit resolution and 16-bit accuracy. The Crystal units even look like SARs, having added a convert-command input. And both autocalibrated ADC families provide a data-ready output. Several units have multiplexers, and Analog Devices units have programmable-gain amplifiers and sensor excitation *(More details will be in the April 25 issue of* ELECTRONIC DESIGN).

Recently, low-cost 16- and 18-bit audio IC converters have encroached on general-purpose 14- and 16-bit units in the bandwidth between 10 and 100 kHz *(Fig. 3, again)*. But whether such converters are to be employed in applications other than audio depends on one's needs. If 16 bits of dc accuracy is needed, the answer is a resounding no. In fact, most of the audio converters don't even provide dc specifications on the data sheet, let alone test for them.

On the other hand, most expensive, general-purpose hybrid 16-bit SARs are only 14-bit accurate, particularly over temperature. In the table, only the Crystal CS5016 16-bit SAR offers no missing codes to 16 bits and 0.0015% DNL, and it's an IC. However, the Analog Devices AD7884/85, a two-pass IC just now arriving on the scene, has similar specifications. And most of the audio ICs will meet 14-bit dc specifications. Thus, in many cases, you can get a pair (most audio converters are duals) of 14-bit converters quite inexpensively. For example, the Burr-Brown PCM1750s gives you two, 18-bit (14-bit-accurate), 200-kHz sampling-rate ADCs for $37 each in 100s.

Atmel, a newcomer to the ADC field, actually specifies a DNL error of ±1 LSB maximum at 18 bits for its dual AT76120. Its switched-capacitor-resistor-ladder SAR is trimmed at the factory with EEPROMs. The converter runs off 5 V and goes for just $25 each in 1000s. Of course, if you take the tack of trying audio ADCs, you'll have to handle the serial output. However, it cuts the number of package pins, thus reducing package size. Because both the PCM1750 and AT76120 are SARs, multiplexing isn't a problem.

If you're handling ac signals (for example, mechanical vibration, active sonar, acoustics, or any ac signal needing spectral analysis), audio converters may be an inexpensive way to go. This is the arena in which digital-signal processing has come to the fore. Today, many digitized ac signals are fed from ADCs to digital-signal processors for analysis or processing. To make that job easy, Burr-Brown took their PCM1750, added a gate array, and came up with single and dual converters (DSP101/102) that can link with all of the common digital-signal processors without any glue logic (ELECTRONIC DESIGN, *Nov. 8, 1990, p. 159)*. In some applications, its use can eliminate the need for over a dozen logic chips between the digital-signal processor and the converter.

In actuality, any of the converters now handling ac signals, particularly the delta sigmas, may be required to link with digital-signal processors, like the 24-bit Crystal CS5322/CS5323 chip set. Though designed to handle signals coming from the seismic sensors used in oil exploration, both converters and sensors adapt to other forms of low-frequency vibration, such as vehicular traffic on bridges. Chromatography and passive sonar are also naturals for these chips. And in most cases, system designers won't cringe at paying a rather stiff $270 for a couple of ICs.

Converters for ac signals must easily link to digital-signal processors, and they must have their dy-

DIGGING DEEPER

To investigate delta sigmas even further, check out the following references:

"Delta Sigma A/D Conversion Technique Overview," and "A Stereo 16-Bit Delta-Sigma A/D Converter For Digital Audio," both available from Crystal Semiconductor, Austin, Texas, (512) 445-7222.

"Principles Of Sigma-Delta Modulation For Analog-To-Digital Converters," from Motorola DSP operation, Austin, Texas, (512) 892-2039.

DSPATCH issues #15 through #18. Analog Devices, Norwood, Mass. (617) 461-3881.

For additional information on 12-bit ADCs, and details of the AD9014, ADC4344 and the ADS-930, see ELECTRONIC DESIGN, *Sept. 13, 1990, p. 47 and 37, respectively.*

For information on ADC dynamic specifications, see ELECTRONIC DESIGN, *Nov. 8, 1990, p. 89.*

A SAMPLING OF ADC SUPPLIERS

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Wakefield, Mass.
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Atmel Corp.
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Comlinear Corp.
Ft. Collins, Colo.
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Crystal Semiconductor Inc.
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CIRCLE 506

Mietec Alcatel
Brussels, Belgium
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Billerica, Mass.
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Teledyne Components Inc.
Moutain View, Calif.
(415) 968-9241
CIRCLE 510

namic, or ac, performance specified. These characteristics include signal-to-noise or signal-to-(noise + distortion) ratios, total harmonic distortion, spurious-free dynamic range, intermodulation distortion, and full-power bandwidth *(see "Digging deeper," p. 78)*.

Today, general-purpose converter applications reach sampling rates of 1 MHz. This usually occurs with the converter at the output of a multichannel high-speed multiplexer and driving a FIFO memory and/or a host's DMA port.

Forces that drive ADC speeds and/or resolutions up to and beyond those of the Analog Devices AD9014 or Sipex's 16-bit AP9490 lie in both the frequency and time domains. The former includes radar, broadband communications, and sonar receivers, as well as any applications in which fast Fourier transforms must be run for spectral analysis. In receiver applications, the ADC downconverts a band-limited signal, resulting in a digitized version of the IF signal. The most important specification is spurious-free dynamic range. A 16-bit specification on a 14-bit converter becomes a plus.

Time-domain applications include digital oscilloscopes, and digitizing the output of visible and infrared charge-coupled-device imagers (essentially digitizing baseband video). These converters also digitize the output of CAT-scan detectors. Vital specifications are DNL and signal-to-(noise + distortion) ratio.

In general, applications are pushing ADC performance to higher sampling rates not only at lower resolution/accuracy of 12 and 14 bits, but also at higher resolutions of 16 bits. As always in analog circuits, the greater the level of accuracy/resolution, the more difficult it is to raise speed/bandwidth. A 50-MHz 12-bit, or a 30-MHz 14-bit converter may be seen long before a 3-MHz 16-bit device comes on the scene.□

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GETTING TOP BANDWIDTH FROM TODAY'S FAST OP AMPS ISN'T EASY. HERE'S HOW TO DO IT WITHOUT LOSING STABILITY.

CAREFUL DESIGN TAMES HIGH-SPEED OP AMPS

Operational amplifiers continuously push the limits of speed and bandwidth. Today's high-speed IC op amps reach gain-bandwidth products in the hundreds-of-megahertz range—numbers unheard of just a few years ago. With such performance, designers must be extremely careful in preserving the op amp's stability without sacrificing bandwidth. Circuits and layouts previously used when designing with lower-frequency devices must be rethought in detail. Otherwise, circuit stability and ac performance can be impaired significantly.

Many factors cause instability in high-speed op amps. These include capacitive loading, inadequate power supply bypassing, input capacitance, and lead-lag compensation. Designers have dealt with both capacitive loading and supply bypass problems for some time. But at high frequencies, their effects are more critical and potentially harmful. Moreover, input capacitance and lead-lag compensation are usually ignored for lower-frequency circuits. Now their consideration is vital.

Driving a capacitive load is one of the most troublesome and difficult problems to overcome because it can easily cause circuit oscillation. When combined with an amplifier's output resistance (R_O), a capacitive load (C_L) creates a pole in the feedback loop that increases the closed-loop phase shift *(Fig. 1)*. Depending on its frequency, the phase shift can reduce phase margin, potentially causing the circuit to become unstable. This phase shift is easily calculated from the pole frequency (f_c):

$$f_c = 1/(2\pi R_O C_L)$$

$$\text{Additional phase shift} = \text{TAN}^{-1}(f_U/f_C)$$

where f_u is the open-loop unity-gain frequency (the op amp's unity-gain bandwidth).

To verify these equations, compare the open-loop gain and phase responses of a 10-MHz, unity-gain-stable op amp, such as the OP-42 with and without a capacitive load *(Fig. 1, again)*. The network analyzer plots indicate the no-capacitive-load condition *(Fig. 1a)*. They also show a loading of 450 pF *(Fig. 1b)*. The 450-pF capacitive load combined with the OP-42's 45-Ω output impedance introduces a

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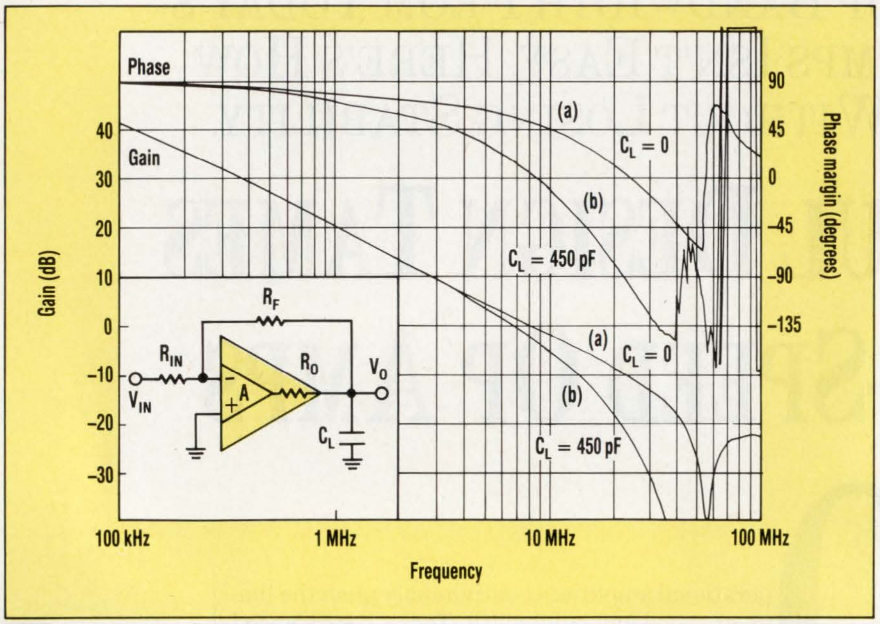

1. A CAPACITIVE LOAD **(C_L) combines with an op amp's output impedance (R_O) to alter the gain and phase response, and thus the phase margin. The upper curves (a) are for an unloaded device, the lower curves (b) are for the same op amp driving a 450-pF load.**

pole at $f_c = 8$ MHz. This results in an additional 45° of phase shift. Consequently, what used to be a stable circuit with 50° of phase margin degrades to a phase-margin of only 5°—potentially causing instability.

Classy Classics

The classical way to maintain stability is to compensate for load capacitance by adding a resistor (R_X) in series with the amplifier's output impedance and a shunt capacitor (C_F) in the feedback path *(Fig. 2, left)*.[1] The basic technique requires adding the proper shunt capacitance and series resistance so that the external feedback network adds a net 0° of phase shift to the loop. Amplifier stability depends on the phase shift of the signal that's fed back to the op amp's inverting input. The signal's phase shift must be less than 180° when the loop gain is greater than or equal to 1. If the feedback network contributes 0° of phase shift, the signal is only phase shifted by the op amp. Assuming the op amp has enough phase margin for the particular gain used, stability is ensured.

Now that the stability goal of the feedback network is established, how is it achieved? Redrawing the external feedback network helps clarify the analysis *(Fig. 2, right)*. Each capacitor contributes a pole and a zero to the feedback network. Intuitively, if the pole and zero contribution of one capacitor cancels the zero and pole contribution of the other capacitor, there will be 0° of phase shift. With this in mind, just derive the pole and zero locations for each capacitor, then set them equal to each other and solve for R_X and C_F. While it is straightforward in concept, the actual derivation is extremely involved and time consuming. But it can be approximated by taking an intuitive approach.

Because capacitive reactance changes with frequency, it can be assumed that a capacitor is an open circuit at 0 Hz and a short circuit at infinite Hz. To simplify network analysis, this principle is applied to one capacitor at a time. For the first case, assume that C_F is a short circuit, resulting in both a pole and a zero location as a function of C_L *(Fig. 3a)*. Next assume that C_L is an open circuit, again providing a pole and a zero location, but as a function of C_F *(Fig. 3b)*. Now there are two poles and two zeros. By equating the poles to the zeros, the necessary value for R_X and C_F can be found with the following two equations:

$$R_X = R_O R_{IN}/R_F$$

$$C_F = (1+1/|A_{CL}|)[(R_F + R_{IN})/R_F^2] C_L R_O$$

where A_{CL} is the closed-loop gain.

By experimenting, it was found that the $1/A_{CL}$ term needed to be added to the equation for C_F. Just these two equations enables virtually any op-amp circuit to be compensated for virtually any capacitive load. A complete derivation performed at the PMI division accurately predicts the previous two equations, including the $1/A_{CL}$ term.

Though this method of compensation yields a stable circuit for any capacitive load, it reduces circuit-bandwidth drastically. The bandwidth is no longer determined by the op amp, but rather by the external components. C_F and R_F dominate, creating a closed-loop bandwidth of:

$$f_{-3\,dB} = 1/2\pi C_F R_F$$

To show the limiting factors, substitute the equation for C_F into the previous equation and simplify:

$$f_{-3\,dB} = 1/2\pi C_L R_O (1 + 1/A_{CL})^2$$

This equation shows that the load capacitance (C_L) and the op amp's output impedance (R_O) need to be made as small as possible. Because R_O is internal to the op amp, the only way to minimize it is to choose an op amp with low R_O. However, there is much more flexibility in controlling C_L. Consider all of the possible sources for C_L in the circuit and try to minimize them. For example, driving an unterminated coaxial cable can add significant amounts of load capacitance. It's important to back-terminate the cable to remove this capacitive load. A pc-board trace with a surrounding ground plane can also add a small amount of capacitance. To reduce its capacitive loading, keep the trace short and keep the ground plane away from it. Even if capacitive loads don't cause the circuit to oscillate, they should be minimized so as not to limit the closed-loop bandwidth.

Power-supply bypassing is often

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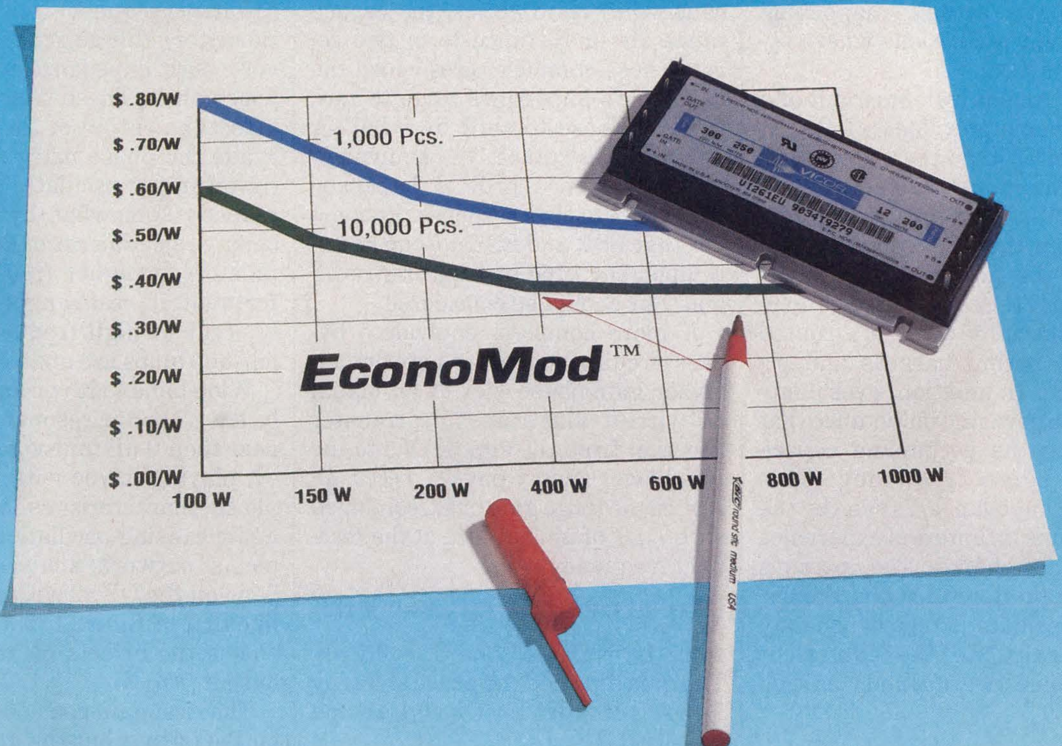

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dealt with by connecting a 10-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor between the supply line and ground. Though this works in many cases, an understanding of what's actually happening helps prevent oscillations where bypassing is critical.

To start, an equivalent circuit of a typical power supply line with the bypass capacitor in place can be represented by an inductor in series with the supply line and a capacitor connected from the IC to ground. The line from the power supply is far from a perfect zero-impedance source, especially after it's routed through a wiring harness and pc-board trace. In addition, every supply line has parasitic inductance that reacts with the decoupling capacitance at some frequency. This causes the impedance, as seen by the IC, to become infinite and experience a rapid phase change. The op amp's phase margin degrades and the circuit may oscillate. To see why it may oscillate, calculate the equivalent parallel impedance of L and C as seen by the IC, Z_{eq}.

$$Z_{eq} = sL(1/sC) / (sL + 1/sC)$$
$$= (1/C)s / (s^2 + 1/LC)$$

where: $s = \pm j(1/\sqrt{LC})$ the complex poles of the equation.

These complex poles cause the equivalent impedance to become infinite at a frequency:

$$f = (1/2\pi)(1/\sqrt{LC})$$

To show this, substitute the value for s into the original equivalent impedance equation:

$$s = j\omega = j(1/\sqrt{LC})$$

$$Z_{eq} = (1/C)s / \{[j(1/\sqrt{LC})]^2 + 1/LC\}$$

$$Z_{eq} = (1/C)s / (-1/LC + 1/LC)$$

The denominator then goes to zero, resulting in an expected infinite impedance. In reality, the impedance does not become infinite because of line losses—the small parasitic resistances that keep the denominator from going to zero. More importantly, the phase almost instantly changes by –180° at the pole frequency.

Like the supply line, the bypass capacitor also has a parasitic inductance, the equivalent series inductance (ESL). ESL creates another resonant frequency in combination with the bypass capacitor. But because they're in series, the capacitance and inductance form two zeros. These complex zeros cause the capacitor's impedance to go to zero and the phase to shift by +180°. A parasitic resistance, the equivalent series resistance (ESR) of the capacitor, dampens this response. Remember that ESR and ESL depend heavily upon the type of capacitor used, and thus should be considered.

A more complete equivalent bypass circuit along with a network analyzer gain-phase plot of an actual LC circuit illustrates the transfer function from the supply (V_P) to the IC's power supply pin (V_{IC}) *(Fig. 4)*. Notice the large gain peak, combined with –180° of phase shift, at the resonant frequency:

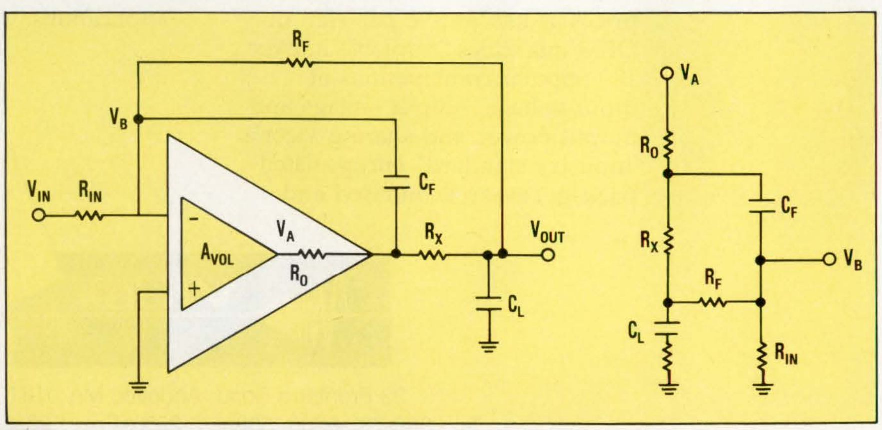
$$\text{Freq.} = (1/2\pi)(1/\sqrt{L_P C_C}) = 1 \text{ MHz}$$

when L_P = 250 nH and C_C = 0.1 μF. The gain dips and the phase shifts by +180° at 16 MHz for C_C = 0.1 μF and L_C = 1nH.

What does all of this mean to the op amp attached to this supply line? To start, a power supply with high impedance means that any current drawn by the op amp causes significant voltage noise on the power supply line. Secondly, any phase shift in the power supply can also feed into the op amp and cause additional phase shifts on its output. Remember that in a transistor-level analysis of an op amp, the power supplies are assumed to be an ac ground. This is true for most frequencies, but at the resonant frequency (with the bypass capacitor), this ac ground becomes a very high impedance with –180° of phase shift. These phase shifts can affect the output of the op amp, degrade the phase margin, and cause the op amp to oscillate. This effect is reduced somewhat by the power-supply rejection ratio (PSRR), which falls off at higher frequencies. Unfortunately, resonant peaks generally occur at high frequencies where most op amps are unable to reject it.

Wide-bandwidth op amps can easily have such a resonant frequency near their 0-dB (unity-gain) frequency, playing havoc with its gain and phase characteristics, and possibly again causing oscillation. For example, a network analyzer plot was done on the OP-42 with a supply line like that of figure 4. The plot clearly shows the effects on the op amp's output *(Fig. 5)*.

The first gain peak doesn't appear on the output but the gain dip does. This is a function of the drop in PSRR as the frequency rises. The OP-42's PSRR is high enough at 1 MHz, about 45 dB, to reject the first peak. But at 15 MHz, the PSRR has fallen to about 15 dB, allowing the gain dip to feed through to the output. There's a rapid change in both gain and phase at this frequency. In this



2. ADDING A RESISTOR (R_X) **in series with the output and a capacitor** (C_F) **between the output and input of an op amp can reduce phase shift in the feedback loop to a value close to zero. This restores stability to an op amp which would oscillate when driving a capacitive load** (C_L).

example, it happens that the gain dip is due to the complex zero and the phase jumps up, so the op amp maintains its phase margin.

However, if the complex pole had occurred at 15 MHz, the phase would have dipped drastically and could have resulted in –180° of phase shift, causing the op amp to oscillate. Clearly, what happens on its power supply line can severely degrade op-amp performance.

Because the supply line's inductance and the capacitor's ESL appear to be the main causes of circuit resonance, the inductance should be reduced. This is often easier said than done, and the inductance can never be completely eliminated. Furthermore, some inductance may actually be desirable to act as a filter. Consequently, liberal bypass capacitance is needed to move the resonance frequency lower to a point where the PSRR is high enough to reject the gain and phase changes. In addition, the bypass capacitor should be located as close to the IC as possible to minimize trace inductance between it and the IC.

Reducing the parasitic inductance within the capacitor is a matter of selecting the correct capacitor type for the job. Typically, a 10-μF tantalum in parallel with a 0.1-μF ceramic capacitor is specified for supply bypassing, and with good reason. The total bypass capacitance combined with the supply-line inductance sets the gain peak's position. To diminish its effect, the peak should be much lower in frequency than the amplifier's 0-dB frequency. As a result, a large capacitor is needed to move the peak lower in frequency to where the PSRR is high. A 10-μF tantalum fits this mold because large capacitance values are available in a reasonably sized component. In fact, in some applications where it's critical not only to maintain stability but also to ensure gain and phase-flatness out to the amplifier's 0-dB frequency, an even larger bypass capacitor is required to ensure rejection.

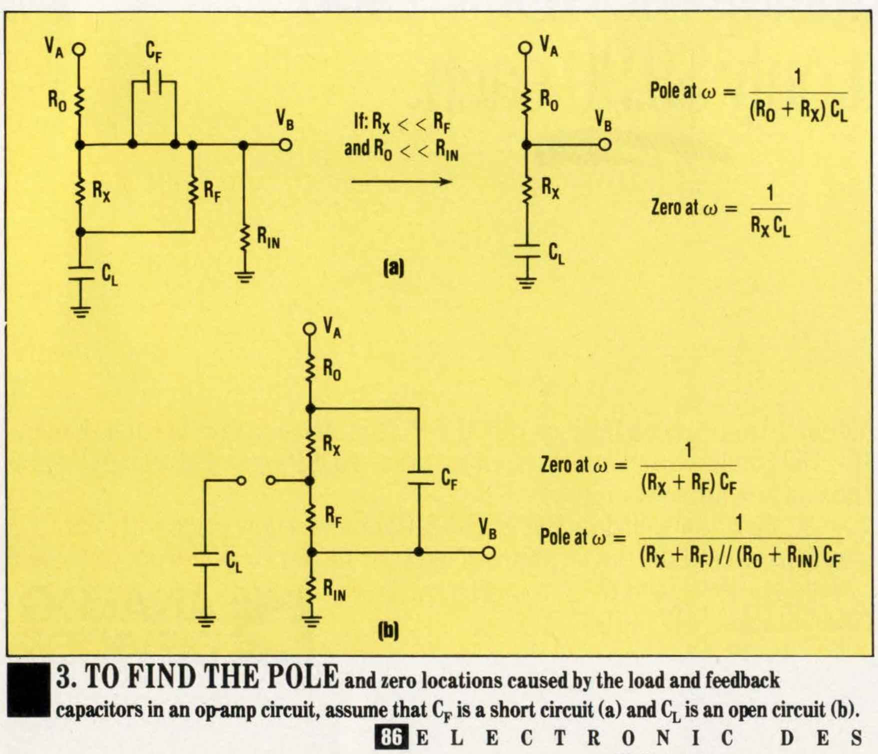
Unfortunately, tantalum capacitors aren't perfect because they have high ESR. On the other hand, ceramic capacitors have low ESR. Typical curves of impedance versus frequency for these two capacitors show that the ceramic capacitor has a much sharper dip in impedance (well below 1 Ω) at a much higher frequency due to its low ESR and ESL. However, the tantalum capacitor has much higher ESR, and thus has a shallow dip down to the range of 1-10 Ω. If just the tantalum is used, the impedance of the bypass won't come close to an ideal ac ground at high frequency. Consequently, a lower-value ceramic capacitor is used, in parallel, to further reduce the high-frequency impedance of the supply bypass circuit. The tantalum capacitor reaches its ESR limit around 1 MHz. Above this frequency, the ceramic continues to lower the bypass impedance until its own ESL dominates around 10 MHz.

Typical curves of ceramic capacitors will usually include a few tenths of an inch of lead length. Most of the ESL that causes the impedance to rise sharply above 10 MHz actually comes from the leads. Shortening the leads reduces ESL. This illustrates the importance of placing bypass capacitors close to the IC. Chip capacitors can be valuable for high-speed circuits for this reason. Because they're surface mounted, chip capacitors have almost no lead length except the pc-board trace and the amplifier leads. Minimizing every source of lead length ensures clean supply bypassing at high frequencies.

The discussion so far dealt with only one amplifier connected to the supply, but usually many amplifiers share the same power source. When this is true, the supply line should be as short and wide as possible, and each IC should be bypassed individually. This reduces noise on the supply line, which arises from the op amps' rapidly changing supply-current demands.

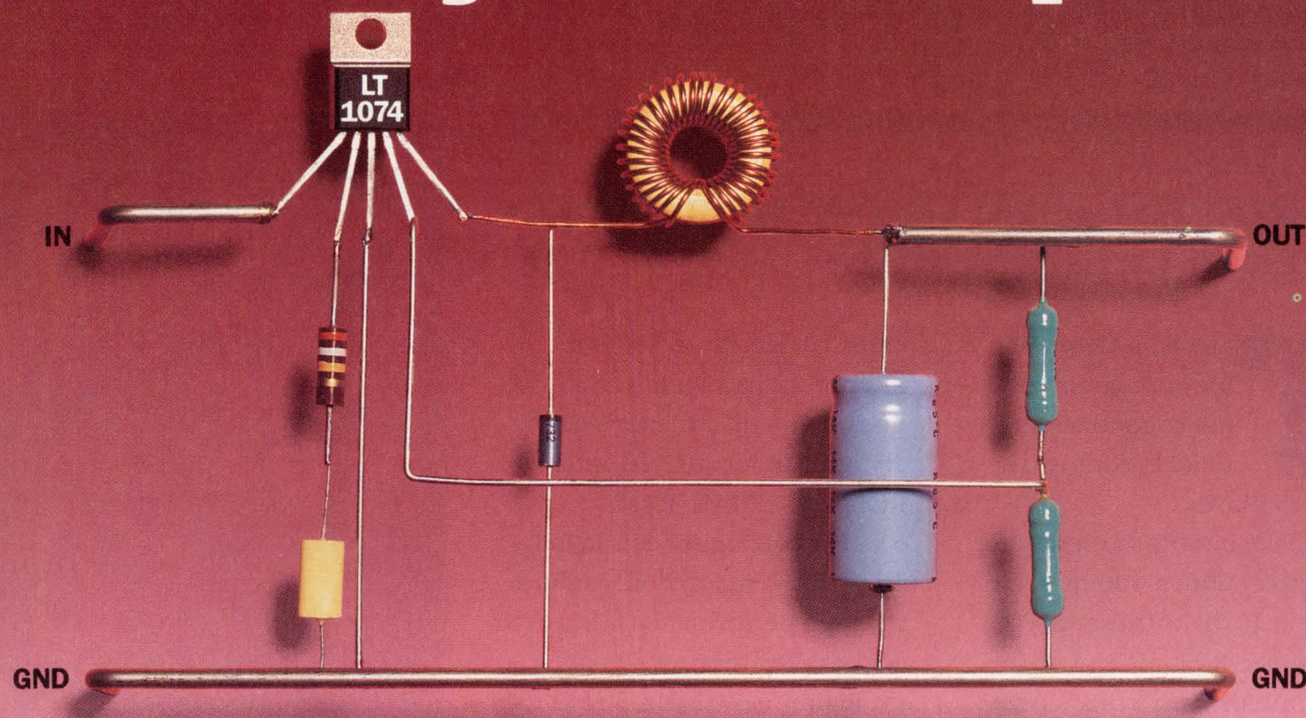
Stray capacitance on the input of lower bandwidth op amps, such as the 741, can often be overlooked without significantly impacting circuit performance. However, when dealing with high-speed circuits, this capacitance becomes critical. Not only will the input capacitance cause the closed-loop bandwidth to drop, it can also cause the op amp to oscillate. This capacitance, which comes from both the op amp's input circuitry and the pc-board (or breadboard) layout, can be looked at as a capacitor to ground on the inverting input *(Fig. 6a)*.

To see how this capacitance causes



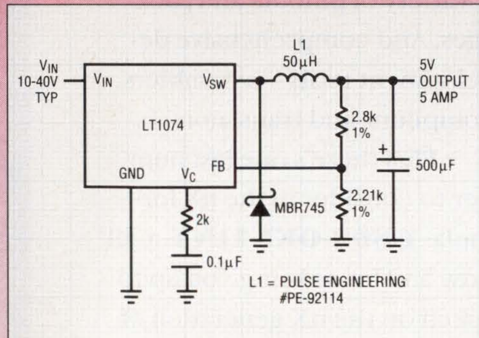
3. TO FIND THE POLE and zero locations caused by the load and feedback capacitors in an op-amp circuit, assume that C_F is a short circuit (a) and C_L is an open circuit (b).

Pretty & Simple



5A positive or negative stepdown or positive to negative voltage conversion.

Talk about easy. Linear's new LT1074 is a simple, elegant solution for your stepdown and inverting switching regulator applications. It's a 5 amp monolithic bipolar regulator with up to 200kHz switching frequency and internal adjustable current limiting. Power switch, oscillator and control circuitry and output monitor are also on the chip. It's a positive "buck" (stepdown) converter with several LTC innovations that also allow the device to be used as a positive to negative converter, a negative boost converter, and a flyback or forward converter.



Basic Step Down Converter

As a stepdown converter, the LT1074 input voltage range is 8V to 60V. The switch output can swing 40V below the ground, a feature that permits the regulator to perform positive to negative conversion with inputs down to 4.5V. It also allows the use of a tapped inductor for output currents up to 10A with no external switching transistor. A true analog multiplier in the feedback loop lets it respond quickly to input voltage fluctuations. The LT1074 is available in either a 5-lead TO-220 package or an 11-lead single-in-line package at $5.25 and $6.45, respectively, in 100-up quantities. For a data sheet and applications note contact: Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035 or call **800-637-5545.**

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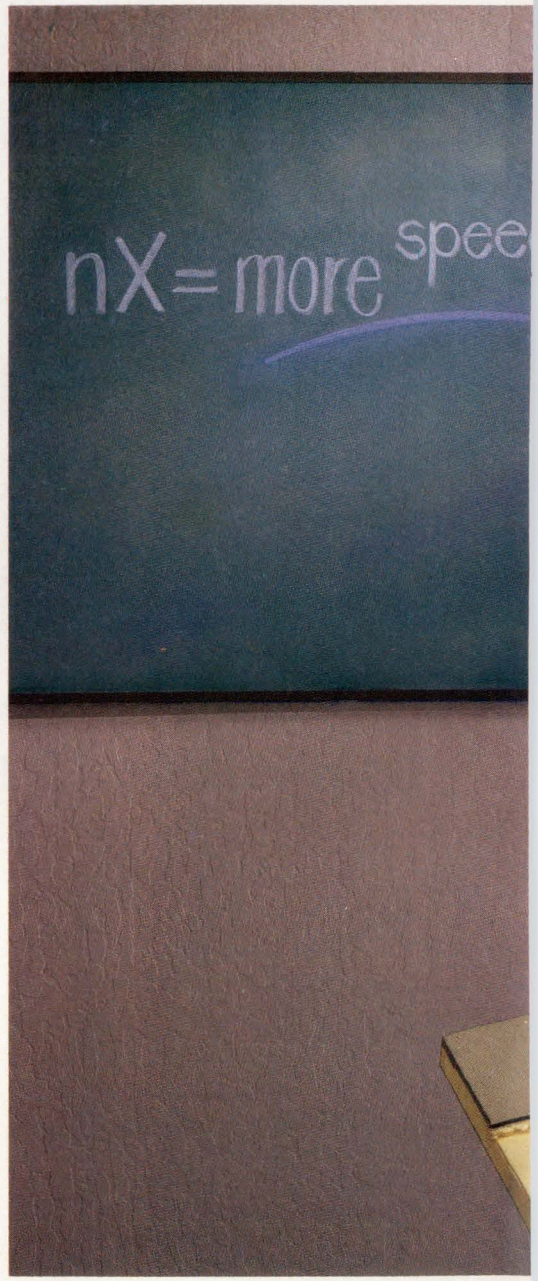

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instability, consider the feedback network that includes the amplifier's output impedance *(Fig. 6b)*. The capacitor's phase contribution to the feedback signal is determined by analyzing the circuit's transfer function from V_A to V_B. In other words, the signal is phase shifted by the amplifier's open-loop phase characteristic and then further shifted by the feedback network's phase response. The transfer function is easily determined to be:

$$V_B/V_A = R_1/[(R_1+R_2+R_O) + sC_1R_1(R_O+R_2)]$$

which produces a pole at:

$$fc = (R_1 + R_2 + R_O)/2\pi C_1R_1(R_O + R_2)$$

$$\approx (R_1 + R_2)/2\pi C_1R_1R_2$$

(Assuming $R_O << R_1$ and R_2)

This pole causes a phase shift at the unity-gain frequency, f_U, of:

$$\text{Phase Shift} = \text{TAN}^{-1}(f_U/f_C)$$

If this phase shift is large enough, the amplifier may oscillate. As an example, consider the OP-42 with 5 pF of input capacitance and $R_1 = R_2 = 10$ kΩ. This creates a pole at 6.4 MHz, creating a phase shift of 51° at the unity-gain crossover frequency of 8 MHz. Because the OP-42 has a phase margin of 48°, a phase shift of 51° can start the amplifier oscillating.

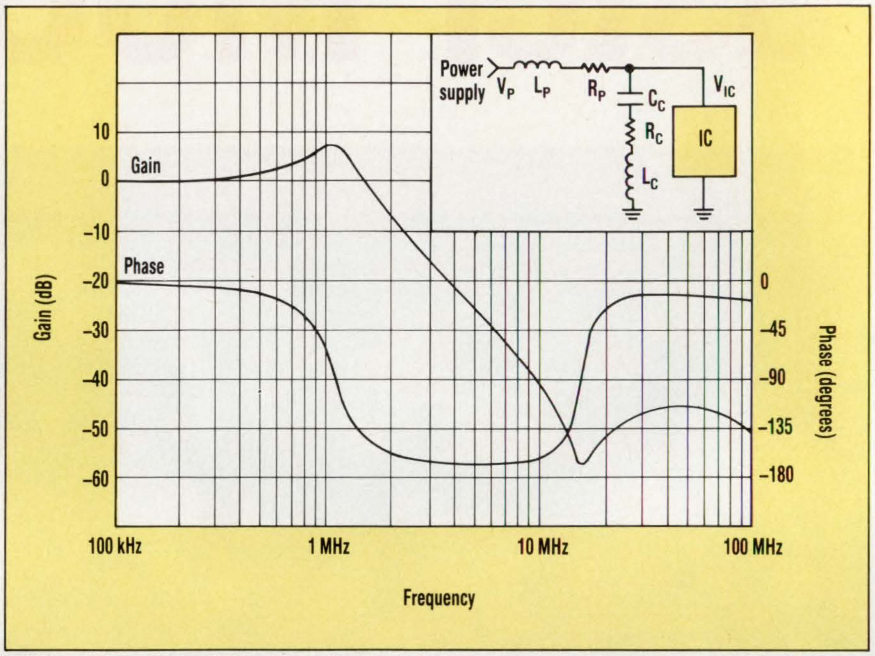
Fortunately, a feedback capacitor can be added in parallel with the feedback resistor to compensate for the input capacitance. The optimum value for the feedback capacitor is easily calculated by determining the pole and zero locations of the feedback network and setting them equal to each other:

$$\text{Pole} = 1/2\pi(C_1 + C_2)R_1//R_2$$

$$\text{Zero} = 1/2\pi C_2R_2$$

equating and solving these gives:
$C_2 \geq C_1R_1/R_2$

Using this value for C_2 provides for zero degrees of phase shift in the feedback network. A shift of 0° ensures stability (assuming the op amp itself is stable). An interesting note is that most resistors have about 1-2 pF of stray capacitance across them, which helps to stabilize the circuit. In the previous example, to compensate for the 5-pF input capacitance of the OP-42, C_2 also needs to be 5 pF.



4. DUE TO RLC PARASITICS, the bypassed power supply line of an IC can resonate at several frequencies. In this instance, pronounced gain and phase changes occur at 1 and 16 MHz.

The board layout can be a major source of stray input capacitance. This capacitance arises from the input traces to the summing junction of the op amp.

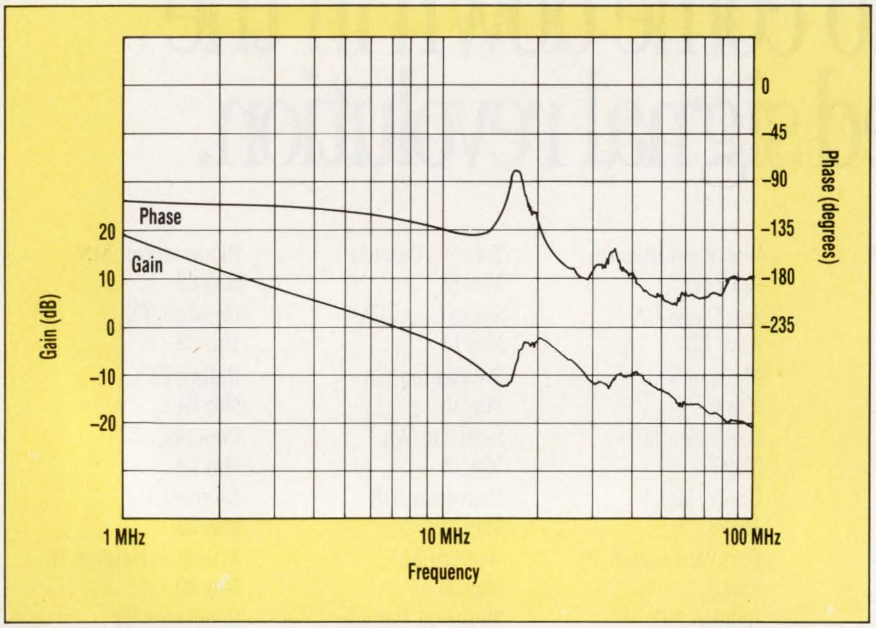
As a reference point, 0.025 in. of pc-board trace with a ground plane surrounding it, on the opposite side of the board, represents about 10 pF of capacitance per inch. Of course, this value varies depending upon the board thickness and the material its made of. But there can easily be enough input capacitance to cause an amplifier to oscillate.

The effects of the input capacitance can be reduced by moving the pole further out in frequency to reduce its effects near the 0-dB frequency. Most op amps have 3 to 5 pF of input capacitance—a combination of the differential-and common-mode capacitances.

For inverting applications, the two capacitances add. However, for noninverting configurations, the differential capacitance is effectively zero, leaving about 1 to 3 pF of common-mode capacitance on each input. This capacitance is fixed for any given op amp and can't be reduced.

On the other hand, some control of pc-board stray capacitance does exist. There are two key ways to reduce this capacitance. First, keep the input traces as short as possible. Put the feedback resistor and the input source very close to the op amp's input, minimizing pc-board trace length. Keep the analog section close together to further reduce trace lengths. Second, don't place the ground plane near the op amp except where it's needed for the circuit. Be especially careful to keep the ground plane away from the op amp's inputs. The obvious exception to this occurs when the noninverting pin is grounded. When ground really is needed, bring it in with a wide trace to ensure a low resistance ground. Don't locate the ground plane on the opposite side of the board from the analog section. Combining all of these measures will go a long way toward keeping the stray input capacitance to a minimum.

The best possible pc-board layout for high-speed analog circuits would pack the analog parts close together, attenuating trace length. Surface-mounted devices and chip capacitors



5. THE RESONANCES SEEN **by the supply pins of an op amp translate into rapid changes in op-amp gain and phase with an attendant loss in phase margin and increased potential for oscillation. The effect is shown here at 16 MHz.**

for power-supply bypassing can really help. The ground plane should be around the perimeter of the analog section and only come in through traces to make contact where ground is required. Try to avoid using sockets to mount the ICs on the board, because they can add another 1 to 3 pF of capacitance to the devices' input pins.

Referring back to the pole equation, it can be seen that minimizing the capacitance isn't the only way to reduce its effects. The parallel combination of the resistors, R_1 and R_2, should also be kept small. The op amp itself determines how small a feedback resistor can be used. Somewhere around 1-2 kΩ is best for most high-frequency amplifiers.

Lowering the resistors by a factor of 10 is the same as reducing the input capacitance by the same factor. However, the output circuit must be able to drive the feedback circuit and the load.

By compensating for the input capacitance with the feedback capacitor, C_2 can stabilize the circuit. However, it reduces bandwidth. Capacitor C_2 forms a pole with the feedback resistor, R_2, which limits the bandwidth to:

$$\text{Bandwidth} = 1/2\pi C_2R_2$$

Clearly the best way to deal with input capacitance is to minimize both it and the feedback resistance. This reduces the possibility of the circuit oscillating and preserves maximum closed-loop bandwidth.

Trick Those Op Amps

Unfortunately, not all op amps are created stable—at least not at unity gain. Many high-speed op amps are stable only for gains greater than five or even ten. These broadband op amps sacrifice unity-gain stability to achieve a much higher gain-bandwidth product. What happens if a design calls for unity gain and you can't find a unity-gain-stable op amp that fits the application? It's not hopeless—by simply adding a capacitor and resistor across the inputs, almost any amplifier can be made stable at unity gain *(Fig. 7)*. This configuration reduces the feedback factor beta (β) at high frequencies, and the amplifier "thinks" it's running at a gain greater than unity.

To understand this compensation technique, first assume that the capacitor is a short at high frequencies, so all that remains is R_C and R_F. The calculation for the value of R_C is based on the amplifier's minimum stable gain If the amplifier needs a gain of at least 5, make $R_C = R_F/4$ to get $\beta = 1/5$. Because the feedback is the equivalent of the minimum gain needed for stability, the amplifier thinks it's at a closed-loop gain of 5 and is therefore stable. However, the signal sees a closed-loop gain of unity, which can be shown by deriving the expression for the gain:

$$V_O = -A_{OL}(R_C/R_C + R_1)V_O + A_{OL}[V_{IN} - (R_1/R_C + R_1)V_{IN}]$$

where A_{OL} is the open-loop gain of the amplifier.

This expression simplifies to:

$$V_O/V_{IN} = A_{OL}\beta / (1 + A_L\beta) = 1/(1/A_{OL}\beta + 1)$$

where

$$\beta = R_C/(R_C + R_1)$$

When the open-loop gain is large, $V_O/V_{IN} = 1$. Unity gain in the signal path is maintained even though the amplifier thinks it is at a closed-loop gain of five.

Next consider the value of the compensating capacitor, C_C. It must be large enough to ensure that the amplifier satisfies the β requirement at a low enough frequency to ensure stability. A minimum value for C_C should provide an impedance equal to that of R_C at a frequency at least a decade below the corner frequency for the amplifier's lowest stable gain:

$$C_C = 1/2\pi R_C(f_C/10)$$

For example, consider the OP-64, a high slew-rate op amp. Its lowest stable gain (5) yields a corner frequency at 16 MHz. A feedback resistor of 1000 Ω results in an R_C of 250 Ω and a C_C of 398 pF—the minimum value that should be considered for C_C.

This equation holds true for operation in a noninverting configuration. Now consider an inverting circuit, whose analysis is very similar. The closed-loop gain equation becomes:

$$V_O/V_{IN} = -1/(1 + 1/A_{OL}\beta)$$

where

$$\beta = (R_C//R_1) / (R_C//R_1+R_2)$$

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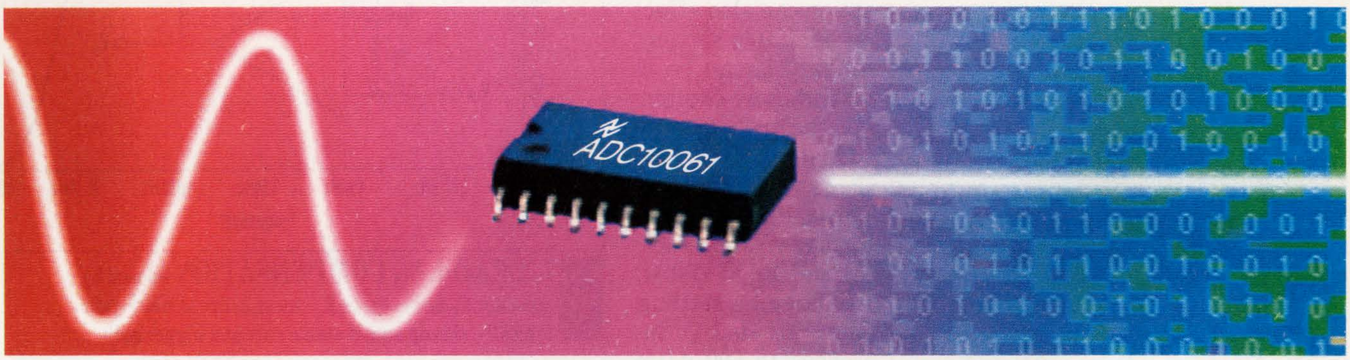

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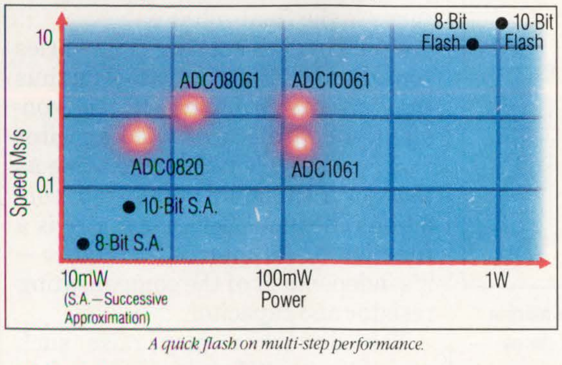

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This expression is similar to the noninverting case except for the sign and the value of β. The expression for β indicates that the input resistor, R_1, is parallel with R_C at high frequencies. This parallel combination calculates the value of R_C for minimum stable gain. The capacitor's value is calculated the same as for the noninverting case.

WHAT'S THE CATCH?

An op amp's bandwidth and settling time can be affected by lead-lag compensation. Don't make the mistake of thinking that because the amplifier is in a unity-gain configuration that its signal bandwidth equals the amplifier's full gain-bandwidth product. Using lead-lag compensation doesn't increase the bandwidth above that at the minimum stable gain. For example, the OP-64 has a gain-bandwidth product of 80 MHz but it's stable only for closed-loop gains of five or more. Therefore, its bandwidth is 16 MHz for a gain of five. When compensated for unity-gain operation, its bandwidth is still 16 MHz, as is seen in the results of the circuit's Spice analysis *(Fig. 7, again)*. To understand this effect, look at the closed loop gain expression for $\beta = 1/5$:

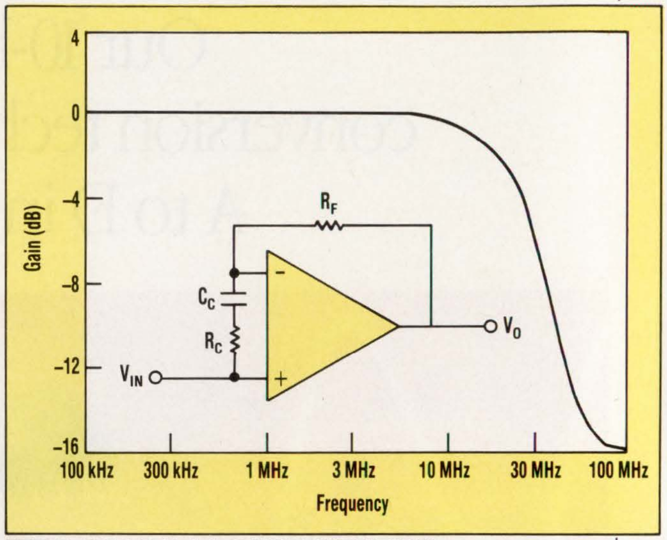
$$V_O/V_{IN} = 1/(5/A_{OL} + 1)$$

and compare it to a typical unity gain expression:

$$V_O/V_{IN} = 1/(1/A_{OL} + 1)$$

Due to β, the compensated amplifier's gain bandwidth is one-fifth that of the uncompensated OP-64.

Lead-lag compensation can also affect an op amp's settling time. This can be illustrated by examining the transient response of the OP-64 *(Figs. 8a and 8b)*. These tests were performed with $C_C = 470$ pF and $R_C = 250\ \Omega$. The circuit's settling time to 0.1% increases to 600 ns in contrast to the $A_V = 5$ settling time of 390 ns. However, this effect is easily overcome by increasing the value of C_C. Another test was performed with $C_C = 1\ \mu F$ and the results prove to be much better *(Fig. 8c)*. The settling time in this instance drops to 310 ns—comparable to the $A_V = 5$ settling time. Using a smaller capacitor while ensuring stability still causes significant overshoot, resulting in a long settling time.

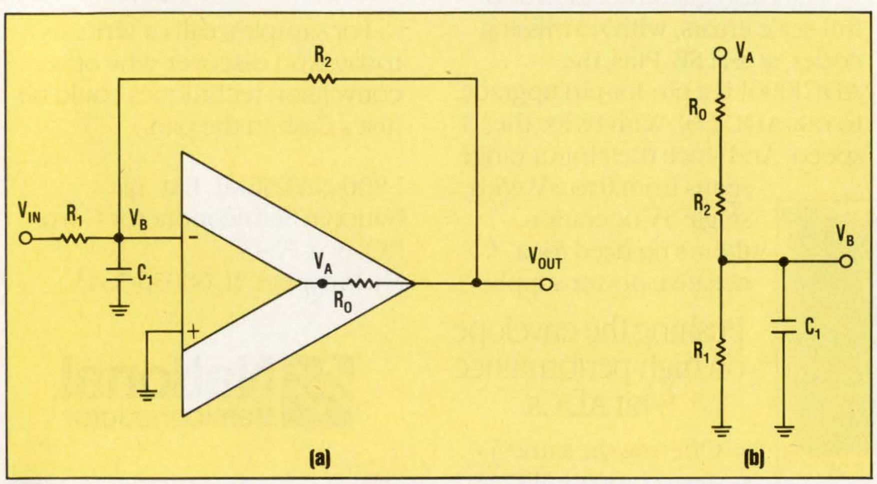


7. LEAD-LAG COMPENSATION formed by capacitor C_C and resistor R_C can stabilize at unity gain. Typically, this op amp is stable only at a higher gain.

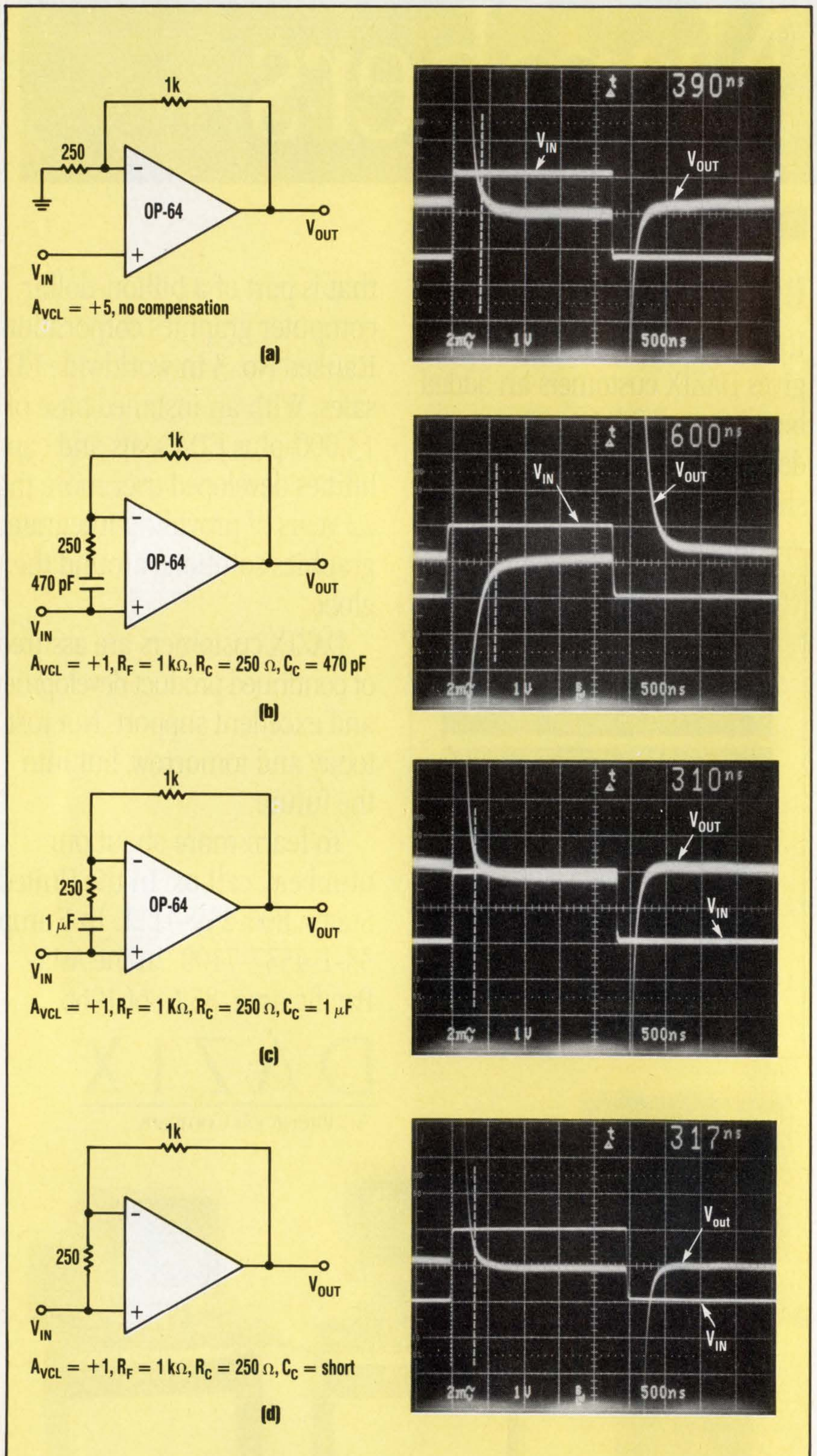
Changing the input voltage from −1 V to +1 V almost instantly creates a large differential voltage between the op amp's inverting and noninverting inputs. The smaller capacitor, combined with the compensating resistor, has a relatively small RC time constant. It charges quickly towards the full differential voltage. When the amplifier overshoots while trying to return to the final output voltage (the input voltage times the closed-loop gain, the capacitor is charged to enough differential voltage to continue forcing the output high. The long decay in the overshoot is caused by the slow discharge of the compensation capacitor. When the larger capacitor is used, the RC time constant becomes very large and the capacitor can only charge to a fraction of the differential voltage. Consequently, when the amplifier overshoots, the capacitor isn't charged to enough of the differential voltage to continue to force the output high. As a result, it quickly returns to the final voltage.

While overall settling time varies considerably, the slew rate (and thus the full power bandwidth) is constant. Regardless of the capacitor chosen, the slew rate is the same as that for a minimum-stable-gain condition. The amplifier's slew rate is a function of its internal structure—it's independent of the compensating resistor and capacitor.

This discussion may raise such questions as: "How big a capacitor



6. PARASITIC CAPACITANCE on an op amp's input (C_1) reduces phase margin and can cause oscillation (a). Its effect can be analyzed by considering C_1 as part of the op amp's feedback network (b).



8. WHEN AN OP AMP with a minimum stable gain of 5 is lead-lag compensated to run at a gain of one, its original settling time of about 400 ns (a) increases to about 600 ns (b). However, increasing the size of the compensation capacitor from 470 pF to 1 μF drops the settling time to about 300 ns (c). Shorting the capacitor shows similar results (d).

should be used? And if a bigger capacitor is better, then why use one at all?" To answer the first question experimentally, a capacitor that's roughly 1000 times the calculated value usually works to keep the overshoot down and the settling time to a minimum. The settling time with just the resistor in place was also measured *(Fig. 8d)*. It is 317 ns, almost the same as when using $C_C = 1\ \mu$F. However, dc errors will creep in if the capacitor isn't used. With the capacitor missing, the dc noise gain of this circuit is now also five. Therefore, any dc errors, such as voltage offset, are increased by a factor of five at the output. Because high-speed amplifiers typically have relatively large offsets, dc errors can be significant and certainly need to be considered.

More Noise Gain

High-frequency or ac noise gain must also be considered. Because the amplifier's feedback is now equivalent to a gain of 5, its ac noise is boosted by a factor of five at the output. Voltage noise is typically modelled as a noise generator on the amplifier's inverting input. A Spice analysis was performed to measure the noise gain by placing the input source on the inverting input and measuring the amplitude of the output for two different compensation capacitors, 470 pF and 1 μF *(Fig. 9)*. At unity gain, the noise gain would usually be one, but as the plot shows, the lead-lag compensation increases it to five (14 dB). By looking at these two plots, it seems that using a 1-μF capacitor generates significantly more noise than the 470-pF capacitor. However, the difference isn't that great. The equation for total rms noise over a given bandwidth is:

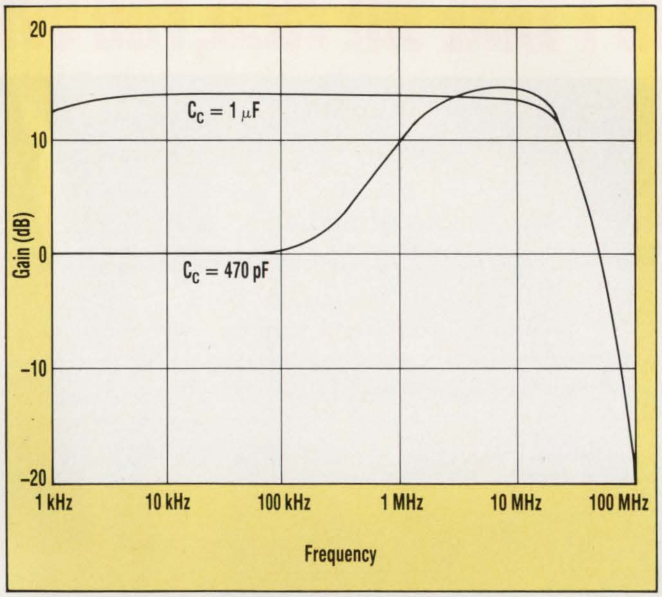
$$E_n = e_n \sqrt{(f_H - f_L)}$$

where:

e_n = the spectral voltage noise density
f_H = upper frequency limit
f_L = lower frequency imit

Examining the plot, both capacitors appear to have the same f_H—20

MHz—but the f_L is different. It's about 500 kHz for the 470-pF capacitor and about 500 Hz for the 1-μF capacitor. However, this only creates a difference of 1.3% for the total noise. Therefore, the noise trade-off with the 1-μF capacitor is minimal when compared to the difference in settling time resulting from the two capacitors. Lead-lag compensation is a valuable tool in dealing with high-frequency op amps. And, as the aforementioned discussion shows, it can offer stability for op amps that typically would be unstable at low gains. However, there are trade-offs, so care must be exercised when using this compensation scheme.□



9. UPPING THE VALUE of a lead-lag compensation capacitor from 470 pF to 1 μF raises the low-frequency noise gain by about 10 dB. Over a given bandwidth, however, the total rms noise is only raised by a small percentage.

Reference:
1. Precision Monolithics Inc., 1988 Analog Applications Seminar.

For a complete discussion of the op-amp stability criterion:

Gary, P., and Meyer, G. *Analog Integrated Circuits.* (New York: Wiley, 1984), pp. 527-70.

Joe Buxton, an applications engineer at the PMI Div. of Analog Devices, holds a BSEE degree from the Univ. of Calif. at Berkeley.

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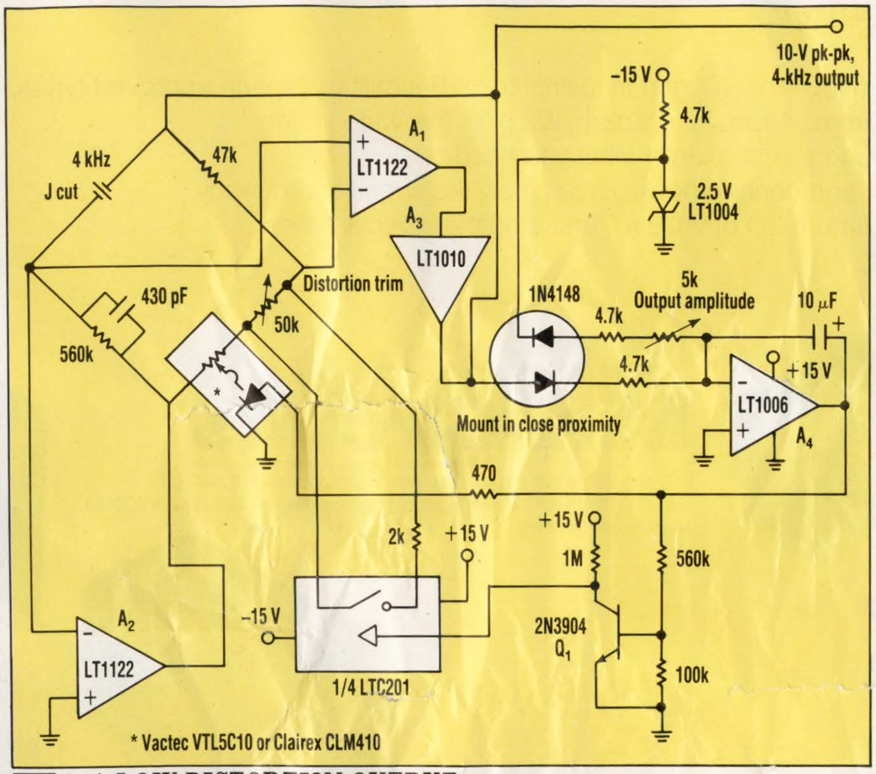


1. A LOW-DISTORTION OUTPUT is generated by this quartz-stabilized oscillator circuit. The 50-kΩ potentiometer is adjusted for minimum distortion while monitoring A_3's output with a distortion analyzer.

Data-converter, audio, and filter testing often require a spectrally pure sine-wave oscillator. This quartz-stabilized oscillator circuit supplies a stable frequency output with extremely low distortion *(Fig. 1)*. The 4-kHz oscillator has less than 9 ppm (0.0009%) distortion in its 10-V pk-pk output.

To understand the circuit's operation, temporarily assume that op amp A_2's output is grounded. With the crystal removed, A_1 and the power buffer (A_3) form a noninverting amplifier with a grounded input. The circuit's gain is set by the ratio of the 47-kΩ resistor to the 50-kΩ potentiometer-optoisolator pair. Inserting the crystal closes the positive feedback path at the crystal's resonant frequency. This causes oscillation to occur.

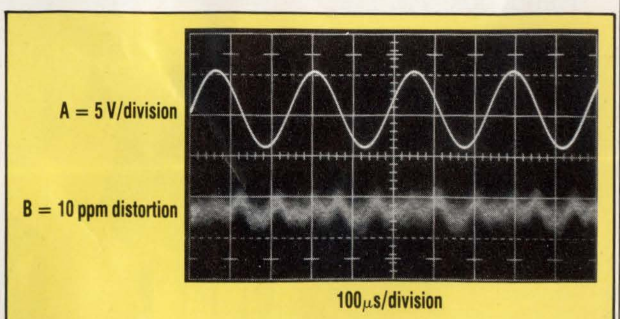
A_4 compares A_3's positive peaks with the LT1004 2.5-V negative reference. The diode in series with the LT1004 supplies temperature compensation for A_3's rectifier diode. A_4 biases the LED portion of the optoisolator, controlling the photoresistor's resistance. As a result, loop gain is set to a value that permits stable amplitude oscillations. The 10-μF capacitor stabilizes this amplitude-control loop.

A_2 eliminates the common-mode swing seen by A_1. This dramatically reduces distortion due to A_1's common-mode rejection limitations. A_2 does this by servo-controlling the 560-kΩ photocell junction to keep its negative input at 0 V. Common-mode swing is thus eliminated at A_1, leaving only the desired differential signal.

Transistor Q_1 and the LTC201 switch form a startup loop. When power is first applied to the circuit, oscillations may not occur or they may build very slowly. Under these conditions, A_4's output saturates positive. This turns Q_1 on. The LTC201 switch turns on, shunting the 2-kΩ resistor across the 50-kΩ potentiometer. This raises A_1's loop gain, forcing a rapid buildup of oscillations. When the oscillations rise high enough, A_4 comes out of saturation, Q_1 and the switch go off, and the loop functions normally.

The circuit is set for minimum distortion by adjusting the 50-kΩ potentiometer while monitoring A_3's output with a distortion analyzer. This trim sets the voltage across the photocell to the optimum value for lowest distortion.

After trimming, A_3's output contains less than 9 ppm distortion *(Fig. 2)*. Residual distortion components include noise and third-harmonic residue. Oscillation frequency, set by crystal tolerance, is typically within 50 ppm, with less than 2.5 ppm/°C drift.□



2. THE 10-V PK-PK OUTPUT OF A_3 has a distortion that's less than 9 ppm (trace A). The residual-distortion components include noise and third-harmonic residue (trace B).

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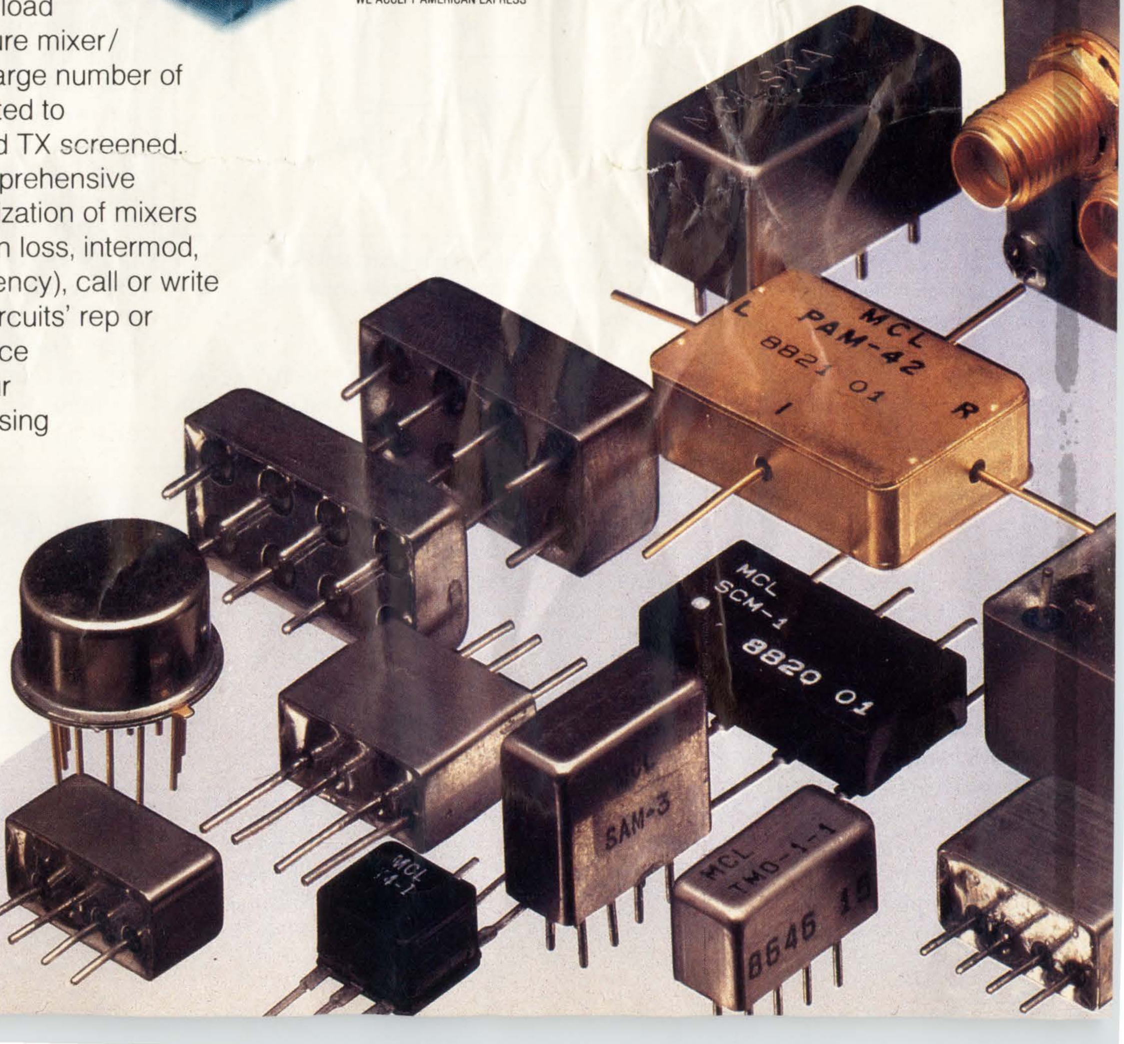
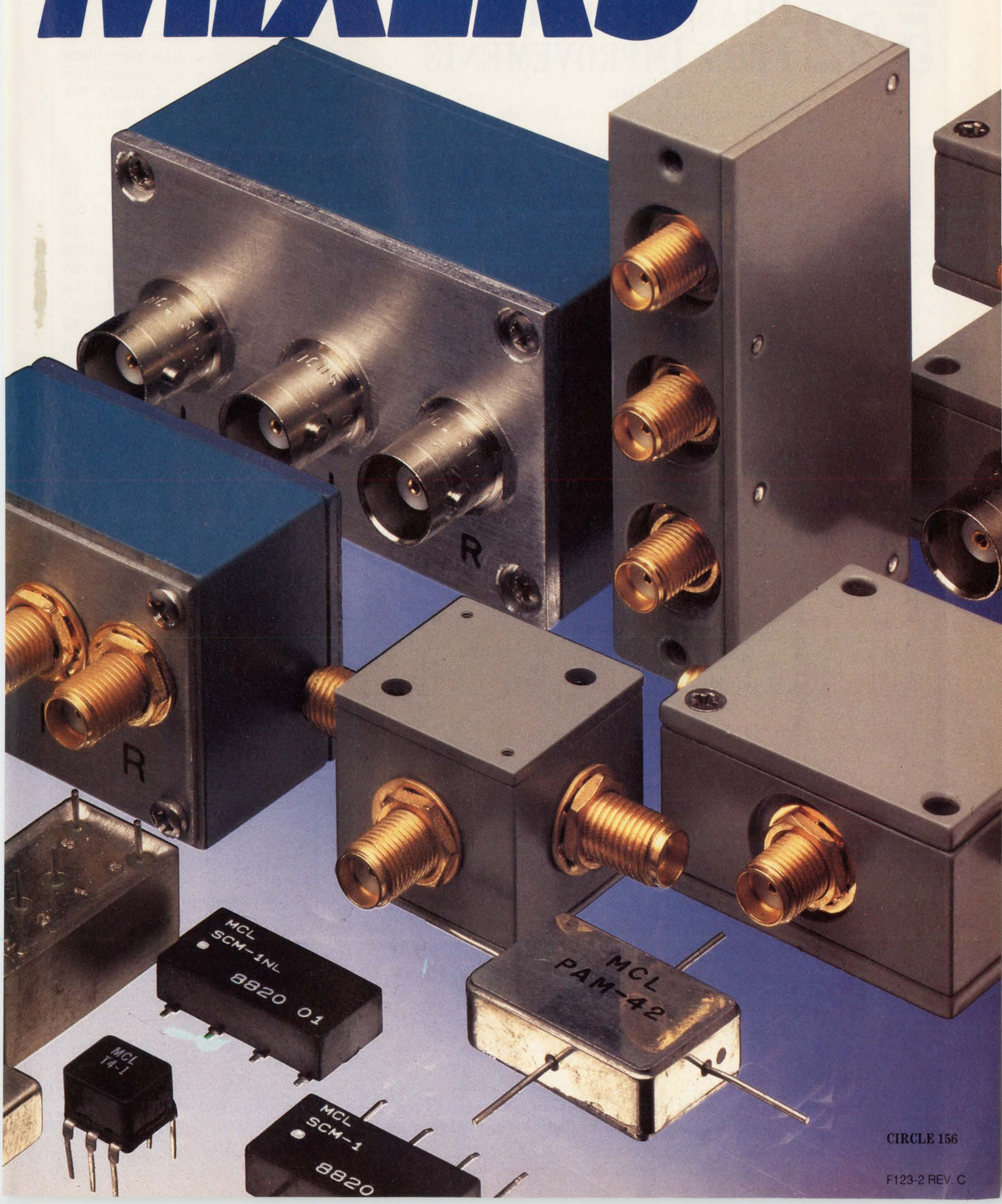


F123-1 REV. C

MIXERS



CIRCLE 156

F123-2 REV. C

CIRCLE 522

PHASE METER PROFITS FROM IMPROVEMENTS

M.J. SALVATI
Flushing Communications, 150-46 35th Ave., Flushing, NY 11354.

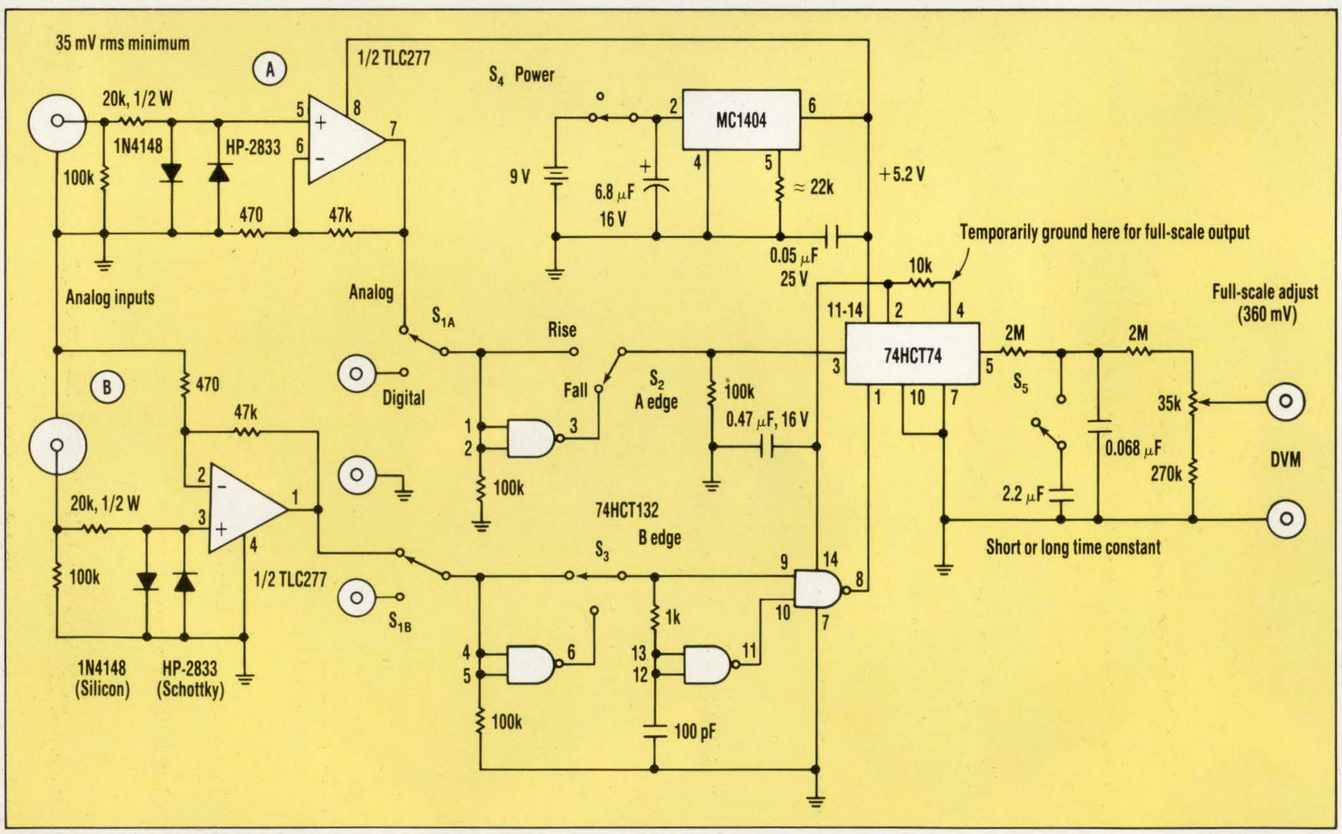
By making a few modifications to a phase-angle measuring circuit described in a previous Idea for Design *("Multimeter Finds Phase Angle,"* ELECTRONIC DESIGN, *July 26, 1990, p. 69)*, performance and usability can be enhanced. The original circuit had an output impedance of over 800 kΩ and a conversion ratio of 10 mV/degree of phase angle. The modified circuit has a 1-mV/degree conversion ratio, so the digital voltmeter (DVM) reads the phase angle directly in degrees on its 200-mV range. This eliminates moving the decimal point mentally. Also, its lower output impedance (around 280 kΩ) causes a smaller error if the DVM used for the readout has a different input impedance than the one used for calibration *(see the figure)*. This also reduces the error if the DVM's input impedance changes from range to range, as some do.

The long time constant used in the original circuit isn't required for all measurements. Here, a switchable time constant allows either a quick response for most measurements or a long time constant for low-frequency measurement, down to 5 Hz.

The phase meter's calibration accuracy is profoundly affected by supply voltage. Therefore, adding an MC1404 precision regulator and a 9-V battery makes the phase meter portable. Frequent recalibration isn't needed as would be the case if the measured circuit's V_{CC} or a bench supply energized the meter. This feature eliminates the calibration switch used in the original circuit because the one-time full-scale calibration can be done by temporarily grounding pin 4 of the 74HCT74. The circuit idles at just 1.5 mA and operates with the battery as low as 6.5 V.

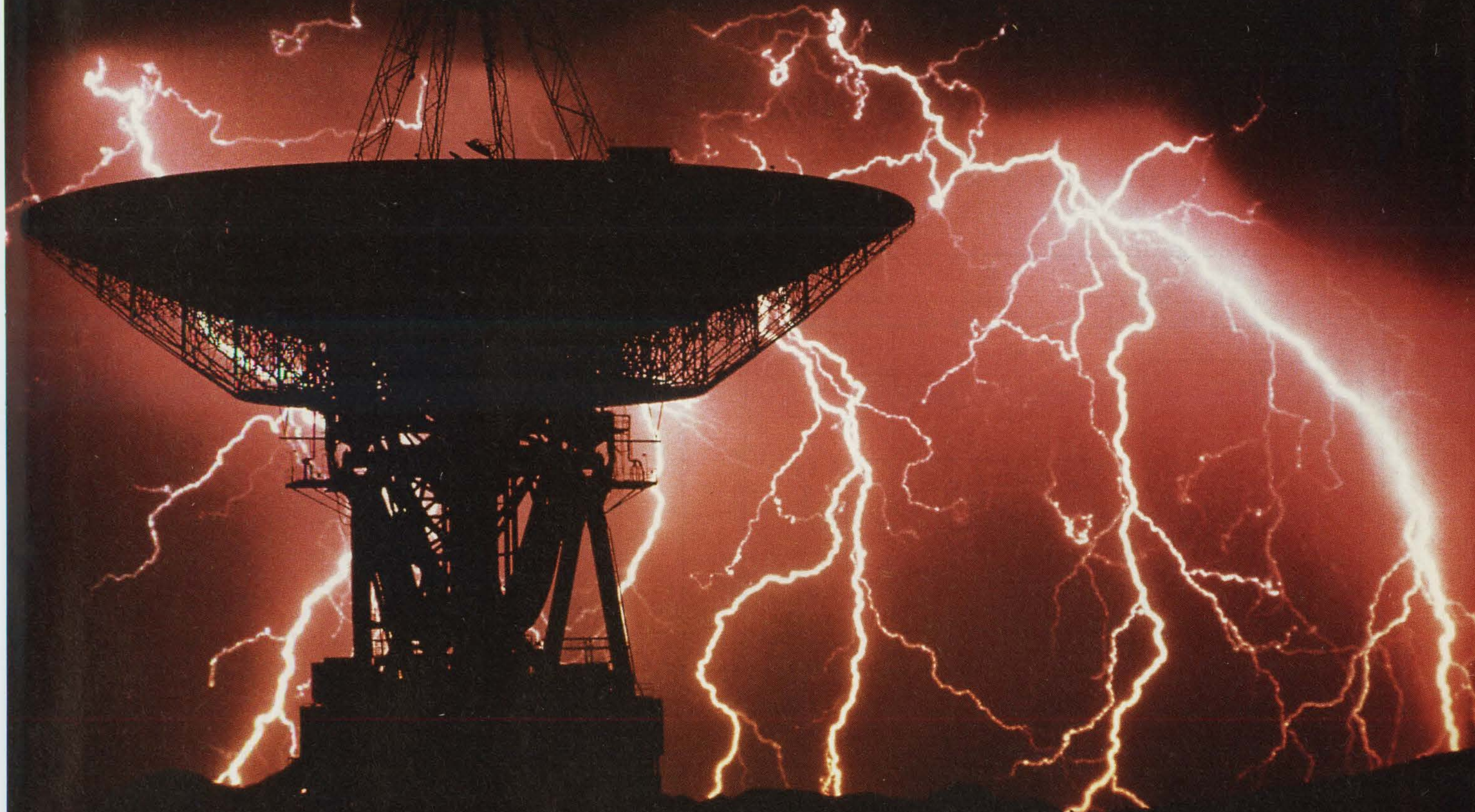
In this example, HCT versions of the ICs were used to ensure compatibility with all TTL-signal sources. In addition, the signal from pin 5 of the MC1401 goes through a resistor to ground to set the regulator's output voltage at 5.2 V. This keeps the circuit's supply voltage higher than that of the circuit being measured.

The input-protected 40-dB amplifiers makes it possible for the circuit to work with sine waves or other nondigital waveforms between 100 mV and 50 V rms. If the two input signals are comparable in amplitude and waveform, the circuit will work down to 30 mV rms. The TLC277 works well with sine waves up to 20 kHz. A CA3260 works for sine waves up to 50 kHz.□



THIS MODIFIED PHASE-ANGLE METER, which offers a 1-mV/degree conversion ratio, also has a lower output impedance and a switchable time constant. The circuit's MC1404 regulator increases its calibration accuracy.

Sampling ADCs With Zero Power Dissipation* Plus 100% Tested Dynamic Performance.



Anybody can guarantee the dynamic performance of a Sampling ADC. Like most other ADC suppliers, Sipex understands what dynamic performance means to the final image, and ultimate success of your system. That's why we run all-codes and full dynamic production testing on 100% of our Sampling ADCs — to give you guaranteed dc and SNR, THD and SINAD ac dynamic performance.

But, Sipex's 100% tested performance comes with one very important difference — *the lowest power dissipation in the industry.* *While we can't give you these high performance SADCs with *no* power dissipation, one look at "their" power dissipation specs will show you ours are almost zero by comparison. Think what that will mean to system reliability.

Of course, the high-level of integration, with single-package ADC, Sample-and-Hold and reference gets you an easier design-in, and less pc board space.

When you're ready to design your next medical imaging, radar or other high performance system with the lowest-power SADCs available, let us know. We'll get you a data sheet and application note on either of these two high performance Sampling ADCs, and a unit to evaluate.

Which will get you convinced. 100%.

12-BIT/10MHZ (SP9560)
(25°C at Nyquist)
- 72dB Spurious-Free Range
- 70dB SNR
- 64dB SINAD
- 3.0 Watts

16-Bit/1MHz (SP9490)
(25°C @ 1MHz Samping Rate)
- 90dB Spurious-Free Range
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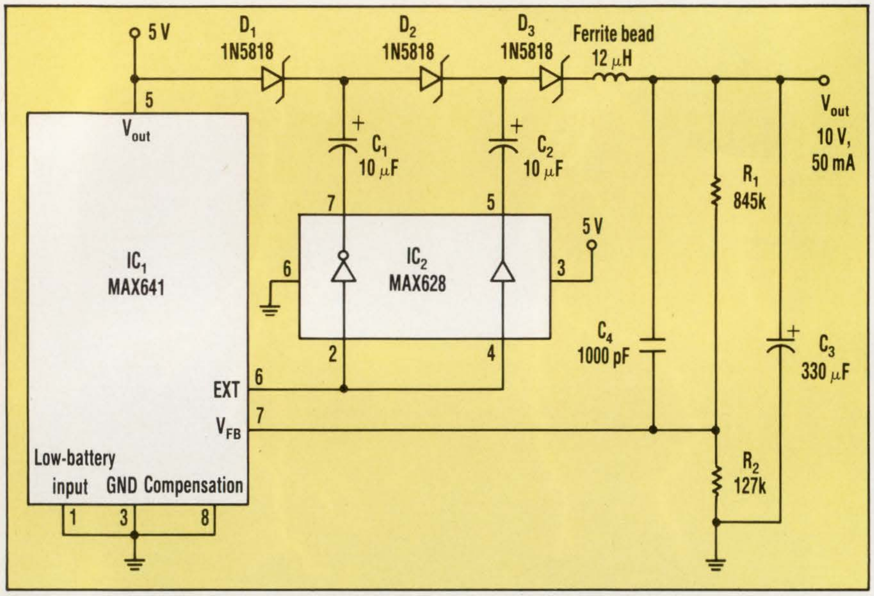
CIRCLE 170

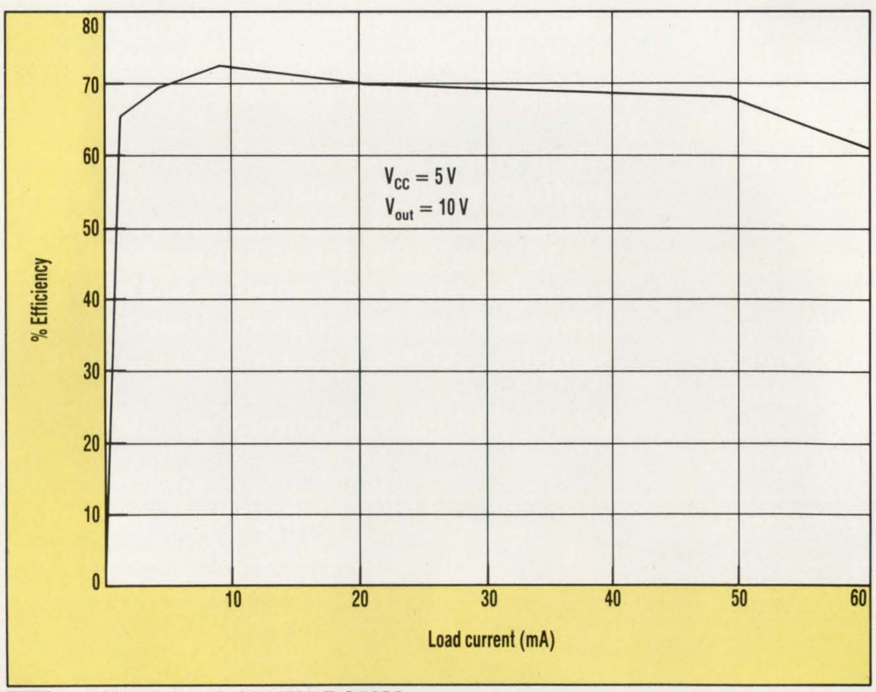
CIRCLE 523

Regulated Charge Pump Delivers 50 mA

GERALD GRADY
Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.



1. THE DIODE-CAPACITOR TRIPLER NETWORK in this step-up switching regulator develops 10 V from a 5 V input. V_{out} is determined by resistors R_1 and R_2. The circuit delivers 50 mA.



2. THE DC-DC CONVERSION efficiency varies with load current. The circuit's efficiency maintains about 70% up to 50 mA.

When compared with charge pumps based on single-polarity amplifiers, the buffer-inverter combination IC used in this circuit delivers more current with fewer parts. The dc-dc converter circuit substitutes a voltage tripler in place of the external inductor and the diode that's typically associated with the switching regulator, IC_1 *(Fig. 1)*. Inverting and noninverting amplifiers in the MOSFET-driver (IC_2) activate a diode-capacitor tripling network (D_{1-3}, C_{1-3}).

A 50-kHz oscillator residing within IC_1 produces the EXT signal (pin 6). IC_2 converts converts this signal into drive signals (180° out of phase) for the tripler. The resulting charge-discharge action in the capacitors recharges C_3 toward 10 V every 20 µs. The ferrite bead limits output ripple to about 20 mV pk-pk for a 50-mA load.

Conversion efficiency is about 70% for the 5-V in, 10-V out configuration *(Fig. 2)*. To assure 50-mA capability, low ESR (equivalent series resistance) capacitors, such as tantalum types, and Schottky diodes should be used. Resistors R_1 and R_2 determine V_{out}:

$$R_1 = R_2[(V_{out}/1.31\ V) - 1].$$

V_{out} can range as high as 15 V with proportionally lower output current.□

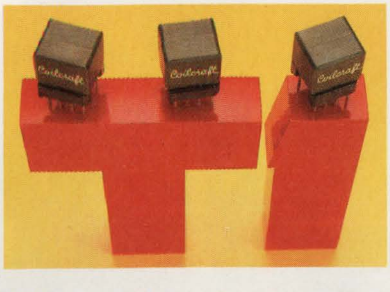
IFD Winner

IFD Winner for December 13, 1990

R. Mark Stitt, Burr-Brown Corp., PO Box 11400, Tucson, AZ 85734; (201) 746-7445. His idea: *"Adjust Voltage Through Zero."*

VOTE!

Read all the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $150 Best-of-Issue award and becomes eligible for a $1,500 Idea-of-the-Year award.



Coilcraft offers standard T1 carrier transformers

A family of low cost, pre-engineered transformers for T1 carrier system applications is offered by Coilcraft.

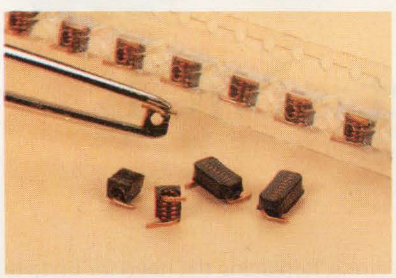
These low-cost transformers are designed for digital transmission at 1.544 Mbit/s using AMI coding, including AT&T B8ZS and European HDB3. They're designed to meet CCITT and FCC requirements.

Packaged in a low, 0.5" profile case, Coilcraft T1 transformers feature less than 50 nsec rise time and 1500 Vrms isolation, primary to secondary.

Surface mount versions and custom values are also available.

For more information, contact **Coilcraft**, 1102 Silver Lake Road, Cary IL 60013. 708/639-6400.

CIRCLE 125



Surface mount "Springs" have tight tolerance, high Q

Coilcraft's SMD "Spring" inductors are ideal for high frequency RF applications, combining the low cost and high Q of air core designs with the convenience of surface mounting.

They cover the inductance range from 2.5 to 43 nH with minimum Q values of 100 to 145 at 150 MHz. Tolerance is ±5% and self resonance is typically greater than 3 GHz.

High temp jacketing assures mechanical stability and very close tolerance. It also forms a flat top, making the parts suitable for automatic placement and reflow soldering. They're available packaged in standard 12 mm EIA tape and reel.

For more information, contact **Coilcraft**, 1102 Silver Lake Road, Cary IL 60013. 708/639-6400.

CIRCLE 126

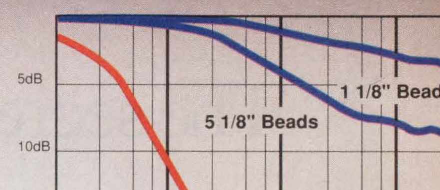
Higher performance EMI filtering for high speed data lines

All these ferrite beads can't equal the EMI suppression of a single Coilcraft Data Line Filter.

Our new DLFs are the most effective, low-cost way to eliminate common mode EMI from digital signals, logic level power lines, and inter-equipment cables.

Available in 8, 4, 3 and 2-line versions, Coilcraft DLFs provide >15 dB attenuation from 30 to 300 MHz. Up to 40 dB simply by adding capacitors!

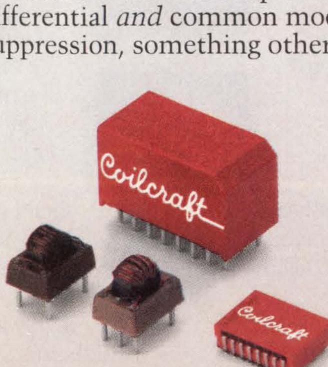
Because they use a single magnetic structure to filter multiple lines, you get differential *and* common mode noise suppression, something other filters can't do.



Attenuation
(50 Ohm System)

Coilcraft Data Line Filters are easier to install and usually take less board space than beads or baluns. And they're far less expensive than filtered connectors–around 2¢ per dB per line.

For details on our complete line of Data Line Filters, circle the reader service number. Or call **800/322-2645** (in IL 708/639-6400).



Designer's Kit D101 contains 2,3,4 and 8-line filters. $65.

CIRCLE 127

Coilcraft

1102 Silver Lake Road, Cary IL 60013

The secret to better Ethernet is NICE. And simple.

Introducing NICE.™ The new MB86960 Network Interface Controller with Encoder/Decoder from the Advanced Products Division of Fujitsu Microelectronics.

With the unveiling of NICE, Ethernet LAN technology reaches a new level of integration.

Now LAN system designers can have an Ethernet controller, buffer management unit and 10 Mbit per second Manchester encoder/decoder on a single chip. So you can now develop high-performance LAN boards more cost effectively than ever before.

For instance, design adapter cards for high-performance buses using just two Ethernet chips instead of the usual three. Simply combine NICE with our new MB86962 10BASE-T transceiver, the most advanced solution for twisted-pair needs. Or choose our MBL8392A if you need a coax interface.

And used with our MB86953 PC Bus Interface Unit, NICE can further reduce costs and complexity when developing PC XT/AT® adapter cards. Replacing the need for up to ten separate parts.

All in all, NICE has some impressive features to enhance your LAN's entire performance. Such as a data bus transfer rate of 20 Mbytes per second. A low-power standby mode. And bus compatibility for most standard microprocessors.

But what's really nice is our understanding of the marketplace. As Fujitsu's American arm, we know what it takes to get you there a lot faster. With greater cost effectiveness.

So now that the secret is out, call us at 1-800-866-8608. And discover NICE. The world's most advanced, highly-integrated Ethernet solution.

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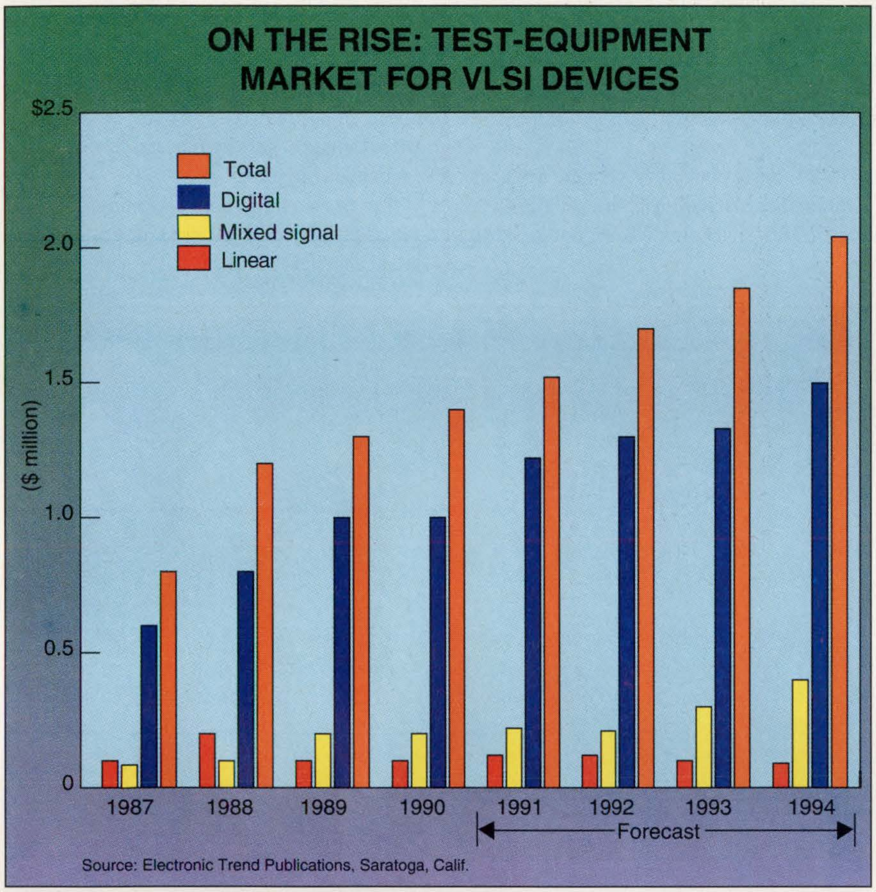
FUJITSU MICROELECTRONICS, INC., Advanced Products Division. 77 Rio Robles, San Jose, CA 95134-1807.

CIRCLE 159

ELECTRONIC DESIGN

QUICK LOOK

EDITED BY SHERRIE VAN TYLE



MARKET FACTS

The market for automated test equipment has hit some snags lately. The once-straightforward testing of pc boards and VLSI and ULSI devices has grown more complicated as boards and ICs becomes faster, smaller, and denser. Testing used to make up less than 11% of product cost. Now testing may amount to 45% of product cost. These findings come from market researcher Electronic Trend Publications, of Saratoga, Calif.

Notwithstanding technical hurdles, sales of ATE are expected to increase 7% to 13% a year from 1990 to 1994. Revenues will rise in that span from $2.1 billion to $3.2 billion.

The test industry has to catch up to such packaging trends as multichip modules and finer pitches. Building testability into a device at the design stage can reduce manufacturing time by 40% and shrink testing costs by half. Other ways to cope with complexity are building in to functional and in-circuit testers more memory and more test scanning per device pin. Open standards like EDIF, VHDL, PDES, and STEP will promote better communication between designers and test engineers.

OFFERS YOU CAN'T REFUSE

A free disk demonstrates TurboLab, integrated, high-speed signal-analysis software from Scentech Inc. The software can read at least 80,000 data points from an ASCII or binary disk file and plot them in less than one second. Menu and view modules create an operating environment using a graphical user interface for the analysis module. Analysis tasks include FIR/IIR filters, FFTs, correlations, interpolations, and polynomial curve fits. Contact Scentech, 800 West Cummings Park, Woburn, MA 01801; (617) 935-1770; fax (617) 935-3054.

A catalog of courses for engineers is free from the Association for Media-Based Continuing Education for Engineers, AMCEE, a consortium of 37 U. S. universities, including MIT and Stanford. Courses include technology—CASE, shared memory architectures, digital ICs, and Unix—and such topics as total quality management and doing business with the Japanese. Videotapes can be rented or purchased; some have a free preview. Contact AMCEE, 613 Cherry St., Swann Bldg. Suite 307, Atlanta, GA 30332-0210; (800) 338-9344; fax (404) 894-8714.

An evaluation package of Easytrax 2, a pc-board design program for PC and Macintosh users, is free from Protel Technology Inc. The full-blown program is menu-driven and has tutorials that take users step by step through board layout of multilayer boards of up to 32 by 32 inches. Contact Protel, 50 Airport Pkwy., San Jose, CA 95110; (800) 544-4186 or (408) 437-7771; fax (408) 437-4913.

To fill the U. S.-Japan information deficit, a twice-a-month magazine gathers news from Japanese technical and business publications. The *Japan Technology Monitor* covers semiconductors, telecommunications, computer hardware, and software. Publisher Douglas Fine speaks Japanese and has an engineering degree from Stanford and an MBA from Harvard.

Issues are 20 to 24 pages long, with no advertising. The magazine also offers English translations of articles abstracted in JTM. Subscriptions are $179 a year from Japan Technology Monitor, 3528 Torrance Blvd., Suite 213, Torrance, CA 90503; (800) 235-1339; (213) 792-1390; fax (213) 792-1392.

QUICKLOOK

HOT PC PRODUCTS

Neural networks—simulated thinking that excels at recognizing patterns, classifying objects, and predicting trends—are opening new avenues to problem solving. Some applications are analyzing chip-manufacturing failures, predicting code sequences in data transmission, and in the military, distinguishing between various types of vehicles from video images.

Intel Corp. is including Brainmaker Professional 2.0 from California Scientific Software in the development package for its neural network chip, the 80170, called ETANN, for electrically trainable analog neural network. The chip, which affords more than 10,000 neural connections, operates at 2 to 4 billion connections/s and links to analog or digital signals.

Brainmaker Professional runs up to 600,000 connections per second on a 486 PC, but it also runs on PCs, PS/2s, and compatibles with 512k and DOS 3.0. Said to be easy to use, Brainmaker has default settings, pull-down menus, and built-in graphics for printing or plotting network behavior.

Brainmaker Professional costs $795. Brainmaker 2.1, an introductory version, sells for $195 from California Scientific Software, 10141 Evening Star Drive No. 6, Grass Valley, CA 95945; (800) 284-8112; (916) 477-7481. Contact Intel at 2250 Mission College Blvd., Santa Clara, CA 95052-8125; (408) 765-9235; fax (408) 765-9220.

QUICK REVIEW

Tired of leafing through the huge manuals that come with Microsoft Windows 3.0? An 144-page book from Peachpit Press Inc., Berkeley, Calif., covers the basics of running and using Windows.

The Little Windows Book summarizes all the major features of the windowing environment and includes handy tricks, such as how to jump back to the program-manager window from anywhere within the software. Short, illustrated chapters get to the point with a summary at chapter end to review the commands discussed.

The book, available in bookstores, lists for $12.95 (ISBN 0-938151-30-4), or from Peachpit, phone (415) 527-8555.

BEST SELLERS

Which technical books are the most popular in Silicon Valley?

ELECTRONICS:

1. *Semiconductor Device Modeling with Spice* by Paolo Antognetti and Giuseppe Massobrio. McGraw-Hill, 1988. ***$29.95.***
2. *Printed Circuits Handbook*, third edition, by Clyde Coombs. McGraw-Hill. 1988 ***$64.95.***
3. *Antennas*, second edition, by John Kraun. McGraw-Hill, 1988. ***$65.75.***
4. *Discrete Time-Signal Processing* by Alan Oppenheim and Ronald Schafer. Prentice Hall, 1989. ***$56.***
5. *Noise Reduction Techniques in Electronic Systems*, second edition, by Henry W. Ott. John Wiley & Sons, 1988. ***$47.95.***

COMPUTER SCIENCE:

1. *Resedit Complete* by Peter Alley. Addison-Wesley, 1991. ***$29.95.***
2. *C++ Primer* by Stanley Lippman. Addison-Wesley, 1989. ***$31.50.***
3. *Programming Windows*, second edition, by Charles Petzold. Microsoft Press, 1990. ***$29.95.***
4. *Annotated C++ Reference Manual* by Margaret Ellis and Bjarne Stroustrup. Addison-Wesley, 1990. ***$31.50.***
5. *The Mac is not a Typewriter* by Robin Williams. Peachpit Press, 1990. ***$9.95.***

This list is compiled for *Electronic Design*'s Quick Look section by Stacey's Bookstore, 219 University Ave., Palo Alto, CA 94301; phone (415) 326-0681; fax (415) 326-0693.

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085

Doing too much or too little planning correlates with knowing when and how to produce a plan. When to initiate the planning effort depends upon the quality and stability of the product's definition. Obviously, trying to create a plan based on an unstable definition is an exercise in futility. The plan will be forced to track a rapidly moving target. That requires the plan to be modified often and extensively.

But it's unreasonable to expect that a definition will remain constant forever. As a result, a critical issue in new product development is identifying when the rate of change of the definition is small enough to allow production of a quality plan. Once the optimum time has been identified, then technique becomes important. Plans must be produced swiftly on a shared and distributed basis while using a collective process to enhance communication and teamwork.

Teams that know when and how to plan can then develop the other skills needed to determine the right number of progress reviews in a milestone sequence. What might be thought by some to be an elementary concept can profoundly affect the overall effort. The number of progress reviews needed by an experienced product-development team creating me-too-with-a-twist products over a short development time could be much different from what's needed for a first-of-a-kind effort that takes place over a multiyear scale. Developing the appropriate time line and milestone sequence for the project is only the beginning.

Attention must be given to developing a plan with just the right amount of detail. Is it necessary to define activity structure down to a daily level of specificity for each person on the team? Or will a framework that looks at a task, or two, a month per individual suffice? Likewise, the plan's structure will likely be influenced by the experience level of the team assembled to produce the new product. An experienced team may know full well the detail behind cross-functional interactions. Yet a new team may require crisp direction and documentation about what it is to give, to whom, and when. For a group of individuals doing something for the first time, a quality plan may be the only vehicle that eliminates, or minimizes, sins of omission while forcefully guiding the effort away from sins of commission. Creating the distributed plan must be sensitive to the experience level and size of each work group to ensure that the right balance is achieved.

ANNOUNCING THE NEW
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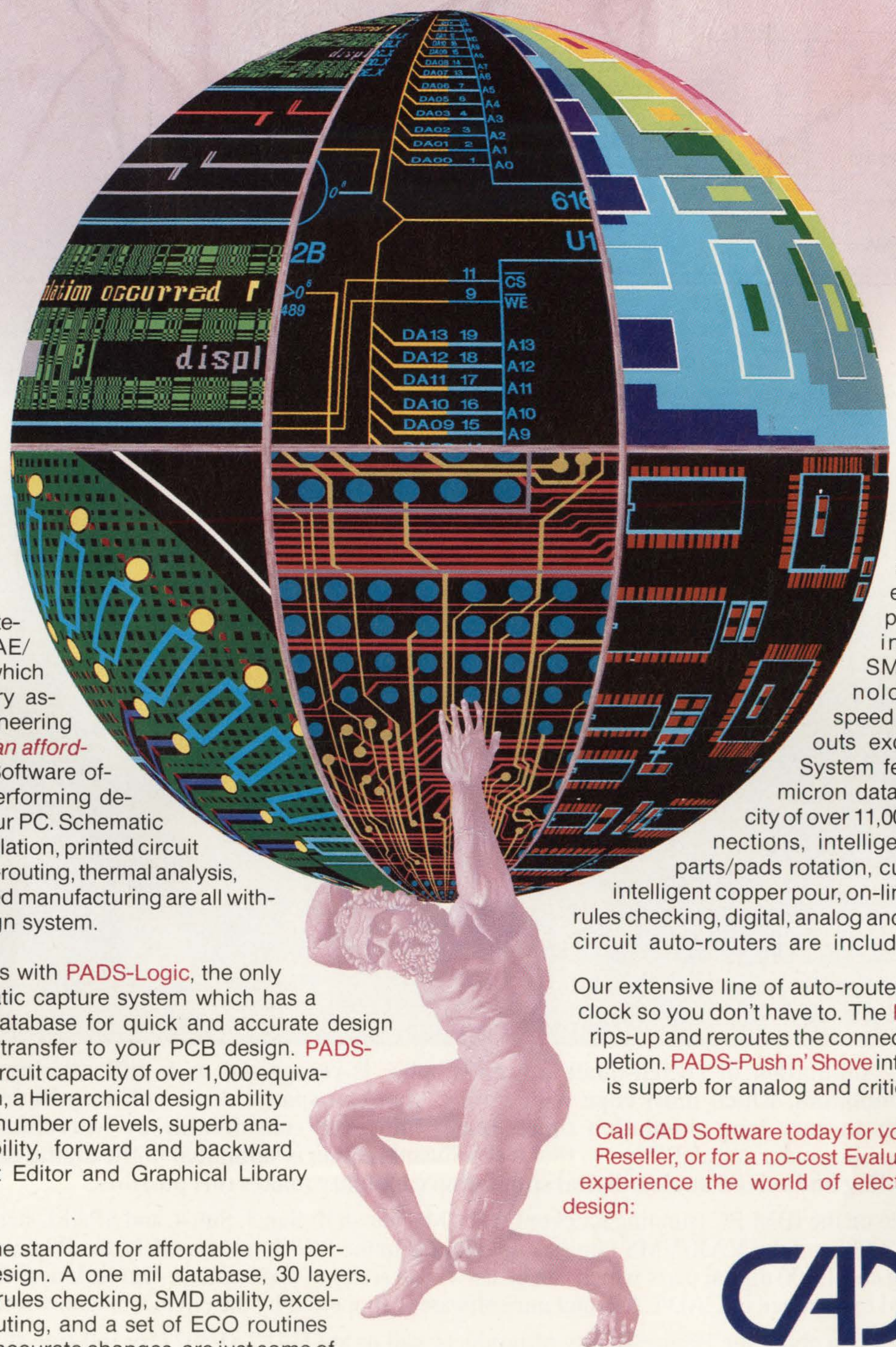

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Your design begins with PADS-Logic, the only PC-based schematic capture system which has a true multi-sheet database for quick and accurate design capture and data transfer to your PCB design. PADS-Logic has a large circuit capacity of over 1,000 equivalent IC's per design, a Hierarchical design ability with an unlimited number of levels, superb analog design capability, forward and backward annotation, a Part Editor and Graphical Library browsing.

PADS-PCB sets the standard for affordable high performance PCB design. A one mil database, 30 layers, automatic design rules checking, SMD ability, excellent interactive routing, and a set of ECO routines which ensure fast accurate changes, are just some of the features which have made PADS-PCB the #1 selling PC based PCB design system.

PADS-2000, the star that outshines any other PC-Based PCB design system, can handle even the most complex designs, including double sided SMD's, mixed technology boards, high speed designs, and layouts exceeding 2000 IC's. System features include a 1 micron database, design capacity of over 11,000 parts/32,000 connections, intelligent T-Routing, 0.1º parts/pads rotation, curved trace routing, intelligent copper pour, on-line and batch design rules checking, digital, analog and high speed/critical circuit auto-routers are included in PADS-2000.

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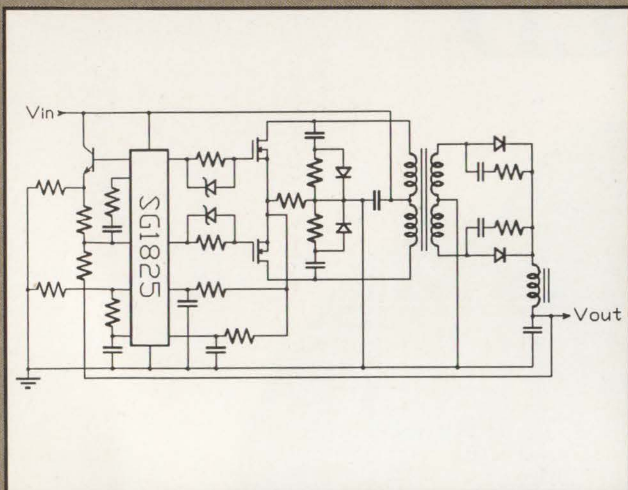
CIRCLE 164

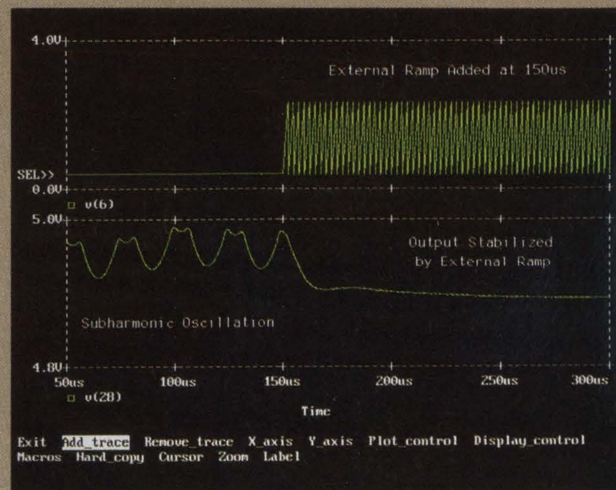
PSpice

MicroSim Corporation

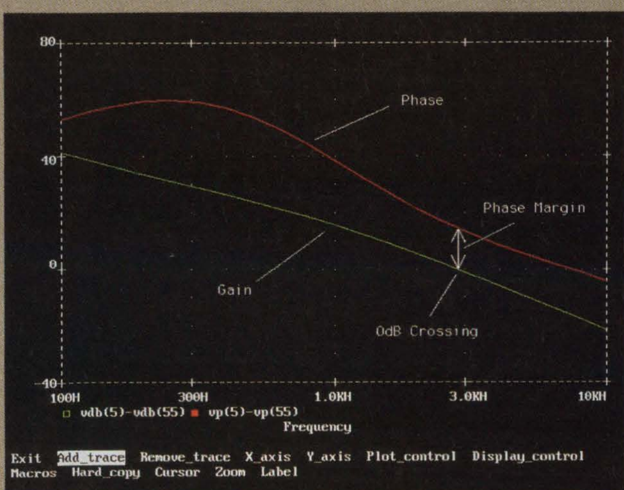
The Standard for Circuit Simulation Switch-Mode Power Supply Design



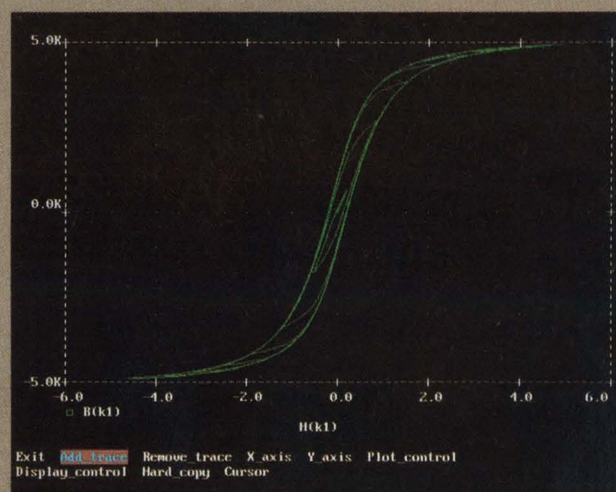
Current mode power supply schematic.



Power supply simulated using mixed analog/digital simulation. Plot shows subharmonic oscillation being suppressed by external ramp.



Simulation using the Vorperian switch model to examine the stability of a power supply.



Hysteresis curve of transformer.

A cycle by cycle simulation of switch-mode power supplies is recognized as a difficult simulation task for SPICE-based simulators, which must cope with timings that can span 4 orders of magnitude. This problem invariably results in very long simulation times, but is improved considerably by MicroSim's approach of building the controller macromodel chips so that a significant section is simulated in the digital domain. PSpice's behavioral modeling and mixed analog/digital simulation capability makes this possible.

PSpice is available on the IBM-PC (running DOS or OS/2); Macintosh II; Sun 3, Sun 4, and SPARCstation; DECstation 2100, 3100, and 5000; and the VAX/VMS families. In addition to the PWM macromodels, the PSpice library contains over 3,500 analog and 1,500 digital parts which can be used in a variety of applications. Our technical staff has over 150 years of combined experience in CAD/CAE, and our software is supported by the engineers who wrote it.

For further information about the PSpice family of products, call us at (714) 770-3022, or toll free at (800) 245-3022. Find out for yourself why PSpice has become the standard for circuit simulation.

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CIRCLE 94

QUICKLOOK

DID YOU KNOW?

... that the number of computer science degrees, once the most popular major on campus, has dwindled 27% since 1986, when 41,889 computer science degrees were earned. Nonetheless, the number of software jobs was up 4% last year and demand for software engineers is expected to stay strong during the 90s.

U. S. Bureau of Labor Statistics

... that laptop computers are the hottest segment of PC market. By 1993, the market for laptops should be worth $12 billion. By 1994, laptops will represent nearly one-third of all computers shipped.

Dataquest Inc.

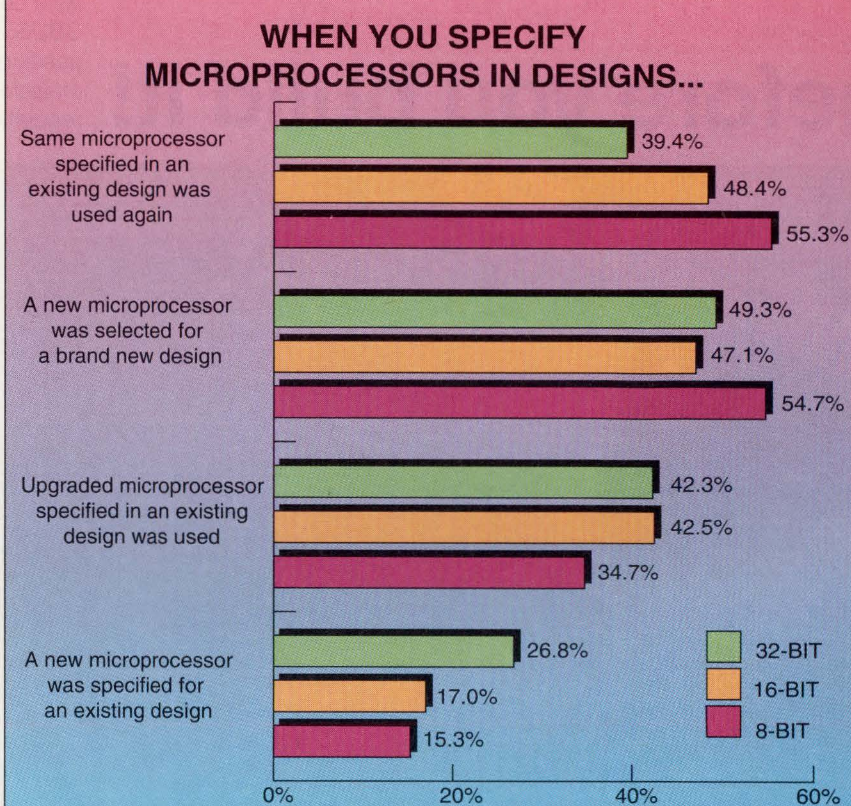
... that in the San Jose area designers of digital systems and peripherals with six or more years of experience earn an average of $58,000 a year.

Source Engineering 1991 salary survey

... that if a slide is not legible at arm's length, it will not be readable when projected from the back of a conference hall.

Rules of Thumb for Scientists and Engineers by David John Fisher (Gulf Publishing Co., Houston, 1991)

MICROPROCESSOR SURVEY



Source: a survey of Electronic Design readers conducted by the Adams Co., Palo Alto, Calif.

TIPS ON INVESTING

You're changing jobs or nearing retirement. Your company is terminating its tax-qualified pension, profit-sharing, or 401(k) plan, or you're 59 1/2 and still working. In each case, you may have to deal with the biggest windfall of your life—a payout of your pension or retirement plan account in a lump-sum distribution.

If you've worked many years for the same company, you could expect a distribution of more than $100,000. This money, which had grown tax-deferred for all these years within your retirement program, is now subject to federal income tax. You face an important financial decision, which must be made within 60 days. Should you roll over your lump-sum distribution to an IRA or pay the tax now? You may want to consider an IRA rollover to defer taxation on your lump sum. But you should determine the tax you'll pay if you don't roll it over—the income these assets earn will be taxed each year unless invested in tax-exempt or tax-deferred vehicles like municipal bonds or life insurance.

Electing to receive your distribution and pay taxes now may be preferable if your distribution is not very large and/or you can't afford to tie up the money for a long time. Also you may be eligible for special tax treatment, which applies to certain qualified lump-sum distributions. If deposited in an IRA rollover, your money continues to grow tax-deferred; it will be taxed as ordinary income as you withdraw it over time.

If you don't roll over the lump sum distribution, your tax rate depends on your age and the number of years that you participated in your company-sponsored plan. If you are more than 59 1/2 and have participated in the plan for five or more years, you are eligible for 5- or 10-year averaging, a special tax rate that allows you to treat the distribution as though it were received over 5- to 10 years. You pay the tax only once in the taxable year that you receive the distribution. These special tax rates can be considerably lower than ordinary income-tax rates because the distribution is taxed separately from other income.

If you were 50 before January 1, 1986 but are under 59 1/2 and participated in the plan for five or more years, you can also take advantage of 5- or 10-year averaging, because of a transitional rule in the Tax Reform Act of 1986. However, you will be subject to an additional 10% penalty tax (unless you are taking early retirement under the company plan after reaching age 55).

If you were under 50 before January 1, 1986, you will pay ordinary income tax and a 10% penalty tax. The only way to avoid the 10% penalty tax in this situation is to roll over your lump sum distribution.

The rules concerning special tax treatment are complicated and for nearly every rule, there's an exception. Talk to your tax adviser to determine your tax treatment.

For a free copy of "Making The Most of Your Lump Sum Distribution," a Shearson Lehman publication, call or write to me at the address below.

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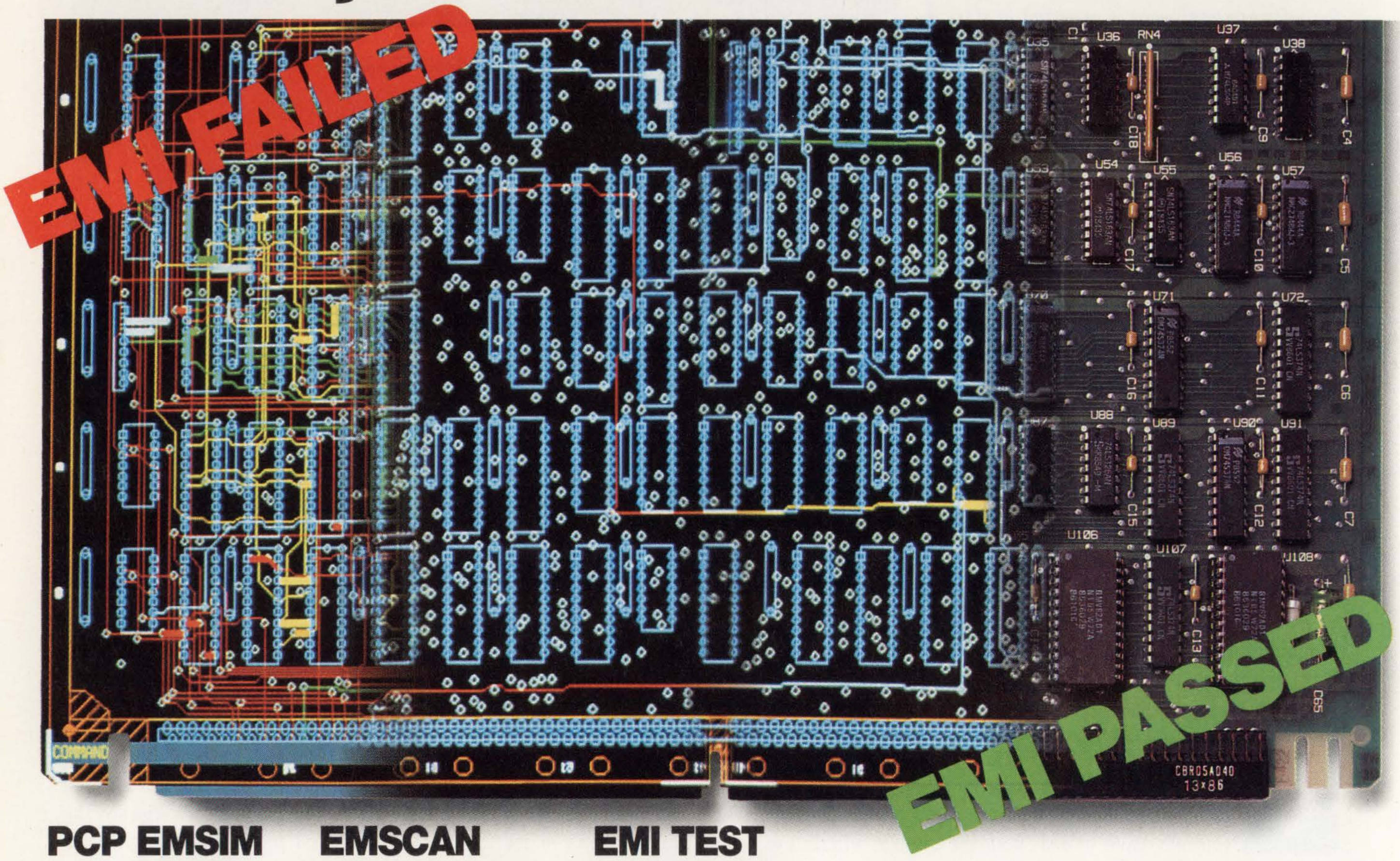

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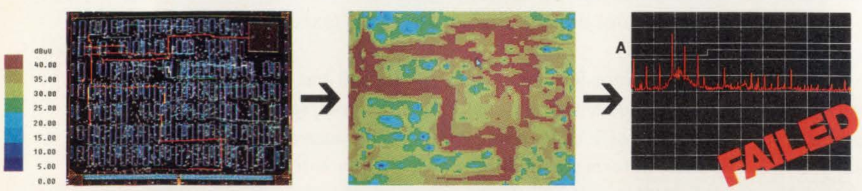

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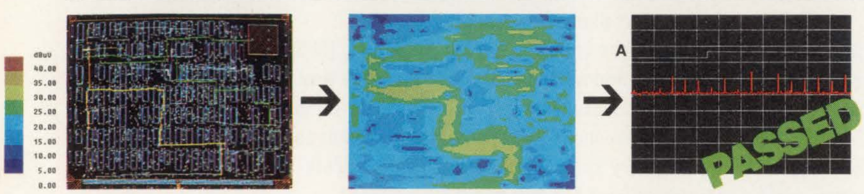

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CIRCLE 179

Simulate transmission-line effects in high-speed PCB and MCM systems

Circuit simulators with efficient models and algorithms can be powerful tools.

BY DILEEP DIVEKAR, RAJ RAGHURAM, AND PAUL K. U. WANG

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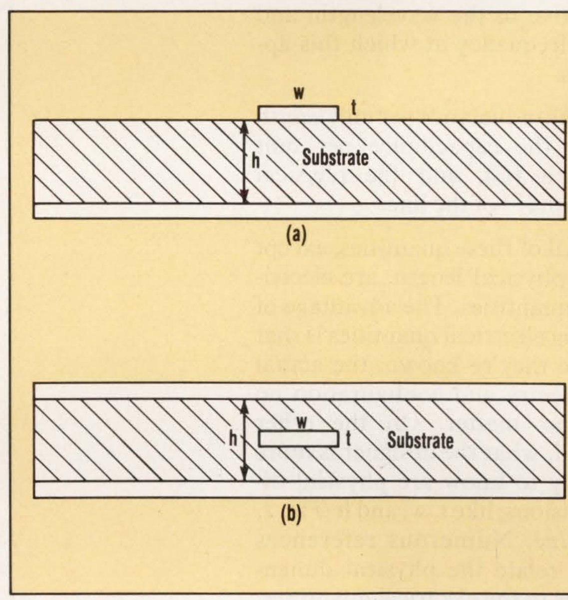
Increasing clock speeds of digital chips requires that more than just the logic and delays associated with each gate be simulated. In particular, the effects of transmission lines in pc boards and multichip modules (MCMs) are critical concerns in achieving more compact layouts and fewer surprises after fabrication. Transmission-line effects occur because of peripheral components, such as interconnects, backplanes, and connectors. These effects are an important consideration in modeling signal degradation due to ringing, impedance mismatches, reflections, and crosstalk.

Board-level designers must hurdle many obstacles to simulate transmission-line effects in digital circuits. If they're using a logic-level simulator rather than a circuit simulator, they can't look at voltage and current waveforms. In addition, circuit simulators without mixed-signal capability aren't easy to use when analyzing digital circuits. This is because it's difficult to create circuit- or transistor-level representation of such digital elements as flip-flops, and because low-level representations take too much time to simulate.

Most importantly, many circuit simulators don't handle transmission lines well. An alternative is special-purpose programs meant to analyze transmission-line portions of the circuit separately. These programs often can't handle nonlinear loads and drivers. Consequently, users aren't sure what happens when the circuit is put together. In addition, transmission lines transport engineers from the comfortable domain of voltages and currents (or the even more comfortable domain of 1s and 0s) to that of electric and magnetic fields. Considering these uncertainties, it's not surprising that pc-board designers often end up using ultra-conservative design rules that can drastically reduce the number of components on a board. The alternative is working with trial-and-error methods and performing extensive printed-circuit-board testing.

There are ways, however, for engineers to adequately simulate transmission-line effects. Circuit simulators with efficient models and algorithms for transmission lines provide a powerful simulation tool for high-speed pc-board and MCM systems. Engineers can simulate high-speed pc-boards and/or MCM systems using coupled lossy transmission lines to accurately model the effects of ringing, reflections, impedance mismatches, and crosstalk. In simple situations, a lossless single transmission line model may suffice. Other situations may require that coupling and crosstalk be considered. Dielectric loss, conductor loss, and skin effect are other important factors.



1. Any wire or trace on a pc board or MCM constitutes a transmission line. This figure shows microstrip (a) and stripline (b) configurations.

Any wire or trace on a pc board or multichip module constitutes a transmission line *(Fig. 1)*. For instance, a thin strip (as small as 0.1 mm) printed on a dielectric is a transmission line. On the other side of the dielectric is a metal ground plane whose width is essentially infinite. This kind of transmission line, known as a microstrip line, has been studied extensively. Curves and formulae are available in various literature.

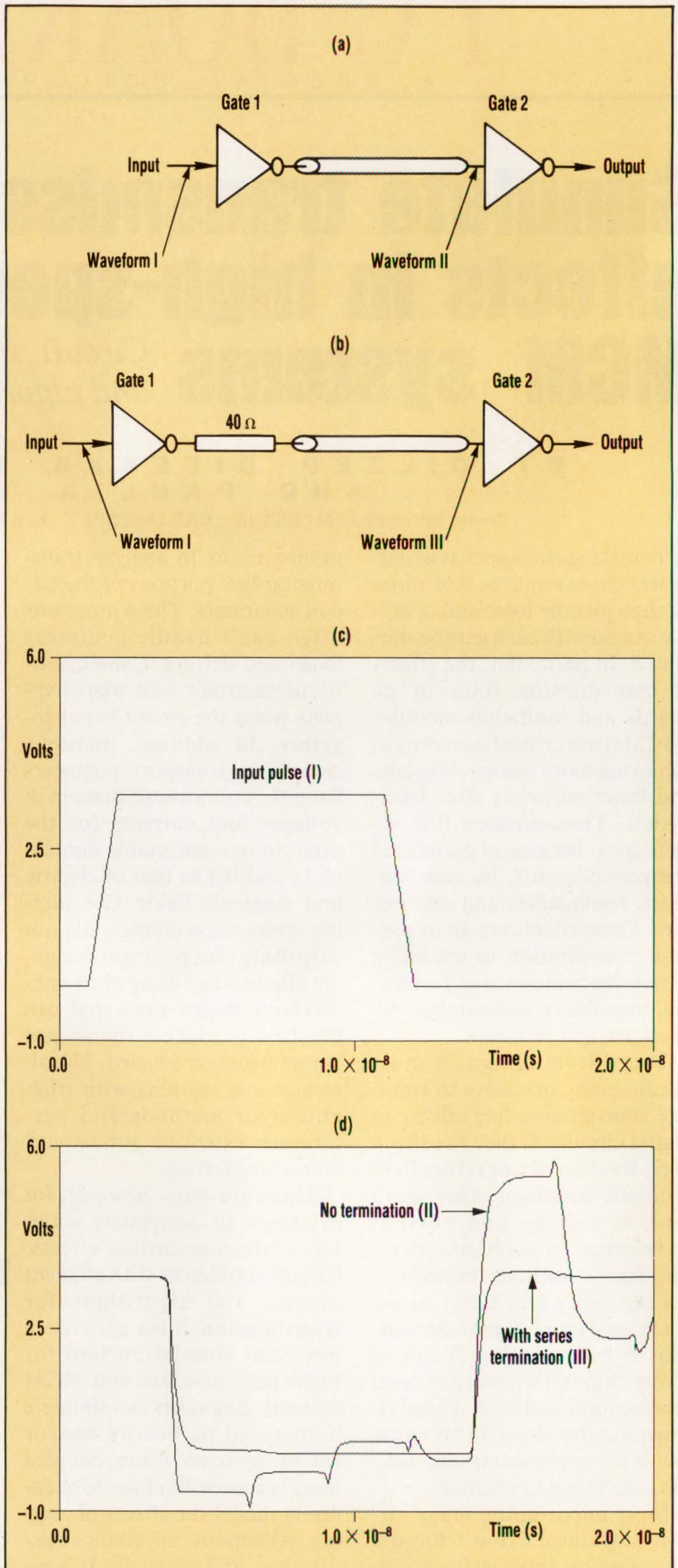
Early versions of Spice and other circuit simulators did not have models for transmission lines. But more recent circuit simulators, including the public-domain Spice3c1 from the Univ. of Calif. at Berkeley, can handle lossless single (or uncoupled) transmission lines. There are several ways of specifying the parameters of these lines. One of the following sets of parameters must be defined:

- The characteristic impedance (Z_0) and the transmission-line delay (TD).
- The characteristic impedance, the normalized electrical length relative to the wavelength, and the frequency at which this applies.
- The inductance per unit length (L), the capacitance per unit length (C), and the physical length (l) of the line.

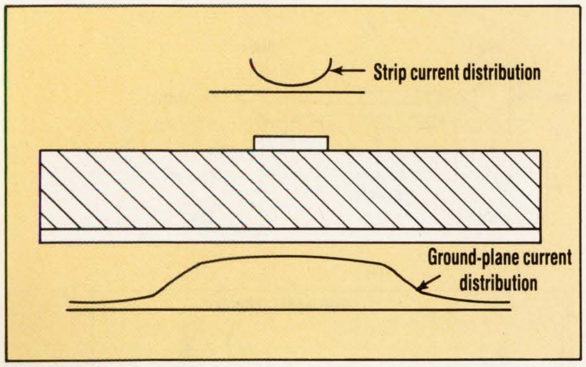
All of these quantities, except the physical length, are electrical quantities. The advantage of using electrical quantities is that once they're known, the actual geometry and configuration no longer matter. On the other hand, what the designer is more likely to know are physical dimensions, like t, w, and h *(Fig. 1, again)*. Numerous references can relate the physical dimensions to the electrical quantities. For example, the following empirical relation applies to the microstrip line:

$$Z_0 = \frac{87}{\sqrt{\epsilon_r + 1.41}} \times \ln\left[\frac{5.98h}{(0.8\,w + t)}\right] = \sqrt{\frac{L}{C}} \quad (1)$$

This equation is true for $0.1w < t < 0.8w$ and $h >> w$, where ϵ_r is the relative dielectric constant of the substrate. An effective relative dielectric constant



2. In this example, two TTL gates are linked by an unterminated transmission line (a), and one employing series termination (b). In both cases, gate 1 is driven by Waveform I, which is a pulse with 1-ns rise and fall times (c). Waveform II clearly depicts the unterminated line's effect on the waveshape applied to gate 2, while Waveform III illustrates the improvement achieved with series termination (d).



3. Current distribution is different for the microstrip conductor and for the ground plane.

can be defined for the microstrip as:

$$\epsilon_{re} = 0.475\epsilon_r + 0.67 \quad (2)$$

The capacitance and inductance per unit length can then be found by using equation 2 and the following relation:

$$\sqrt{LC} = \frac{\sqrt{\epsilon_{re}}}{3 \times 10^8} \quad (3)$$

Other relations that apply to any lossless single line are:

$$Z_0 = \sqrt{\frac{L}{C}} \quad (4)$$

$$TD = l \times \sqrt{LC} \quad (5)$$

The normalized electrical length is given by:

$$l \times (f \times \sqrt{LC}) \quad (6)$$

These relations can be used to calculate the required electrical parameters for simulation of a transmission line using a circuit simulator. Simulation with lossless single transmission lines can bring out the importance of proper matching or termination of interconnects.

Consider a simple circuit containing two fast TTL gates connected by a single transmission line *(Fig. 2a)*. The line has a propagation delay of 1.3 ns corresponding to a microstrip length of about 10 in. The line's length isn't unusual even in small or medium size boards. Simulation performed on this circuit used analog behavioral models for the digital gates. Using the behavioral models sped up the analysis without losing a significant amount of accuracy.

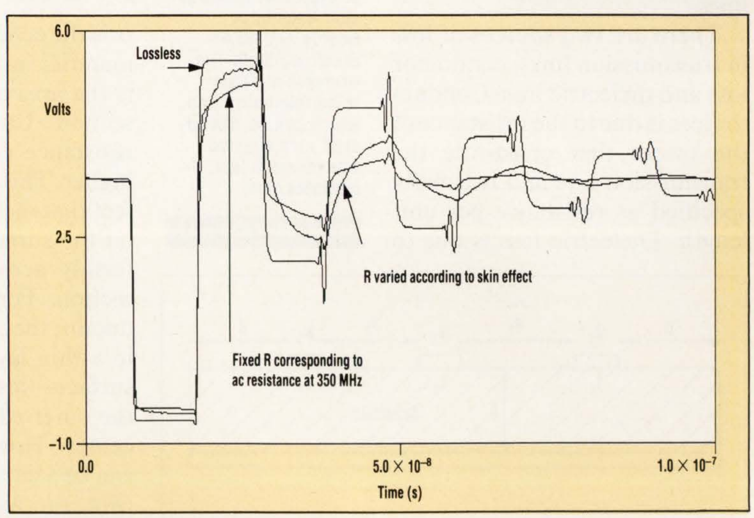
Simulation can be a very useful tool when checking if any circuit parts suffer from signal degradation due to transmission-line effects, and when finding a suitable scheme to solve the problem. Among the various schemes for properly terminating transmission lines are:

- Series termination
- Parallel termination
- Thevenin termination
- Ac termination

Parallel termination is usually unsuitable for TTL gates because of V_{OH} degradation. But it's common for pc boards using ECL gates because ECL gates are designed to drive 50-Ω loads. The other three schemes, however, are applicable for TTL gates. Series termination can be used when the line's characteristic impedance is more than its output impedance *(Fig. 2b)*. It involves adding a resistor between the input to the transmission line and the output of the driving gate (gate 1, in this instance).

Consider the effect of the unterminated transmission line when a pulse with a 1-ns rise time (Waveform I) is applied to the input of gate 1 *(Fig. 2c)*. Because of transmission-line effects, Waveform II at the input to gate 2 is unacceptable for most situations *(Fig. 2d)*. This is expected because the rise and fall times of the pulse applied to gate 1 are less than the propagation delay of the transmission line connecting gates 1 and 2. A rough rule of thumb is that to avoid transmission-line effects, the rise and fall times of the applied waveform should be at least three times the propagation delay of the transmission line (ELECTRONIC DESIGN, *Aug. 9, 1990, p. 89)*. Waveform III shows how the input to gate 2 improves when a series termination resistance is used *(Fig. 2d, again)*.

It's usually important to use a Spice-like circuit simulator because the loads and drivers are nonlinear transistor circuits, much like the TTL gates used in the example circuit. Their input and output impedances can vary significantly over the swing from V_{OH} to V_{OL} or vice versa, and simulators that use linear drivers and loads may not give the right answers. Using simulation greatly simplified the choice of the correct series termination resistor in this circuit. A value of 40 Ω was best found by trying out a few values. In addition, the waveform at the output of gate 1 was unimportant. If that had been important, a series-termination resistor of different value could have been used. Simulation with circuit simulators having transmission line models can make it easy to properly design terminations to



4. This graph shows the effects of simulating an unterminated transmission line with no losses, a fixed ac resistance, and a frequency- dependent resistance.

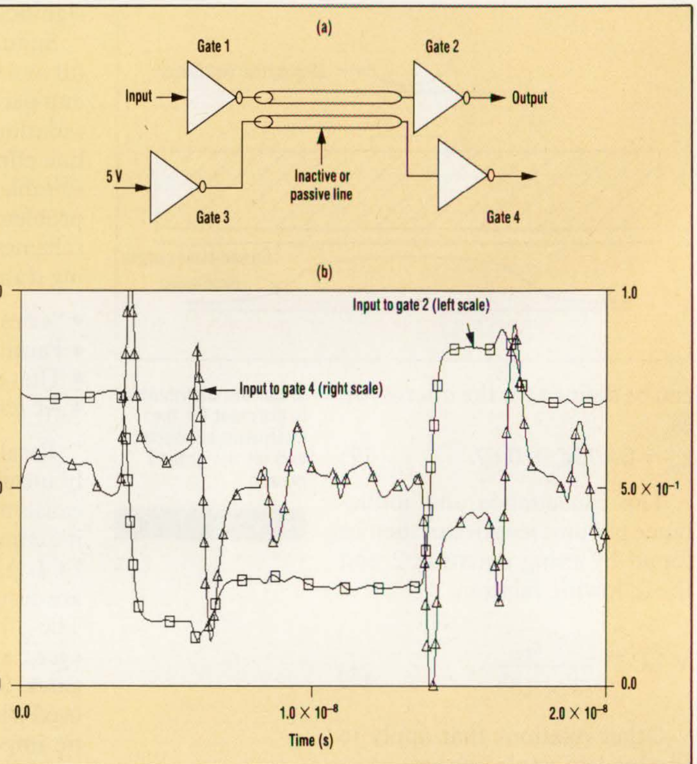
avoid the effects of mismatches.

Here, though, caution should be applied. Implementing transmission lines in many circuit simulators is still at an early stage. The public-domain Spice3c1 takes a long time to simulate transmission lines, and it generates huge output files. This is because of poor time-step control. Others use lumped equivalents to simulate the distributed capacitances and inductances. The corresponding input files may be tedious to generate, and many segments may be needed for longer lines. To effectively simulate transmission lines, it may be wise to employ a simulator such as ContecSpice, which is used in the example. ContecSpice is a general-purpose circuit simulator with fast algorithms to simulate transmission lines.

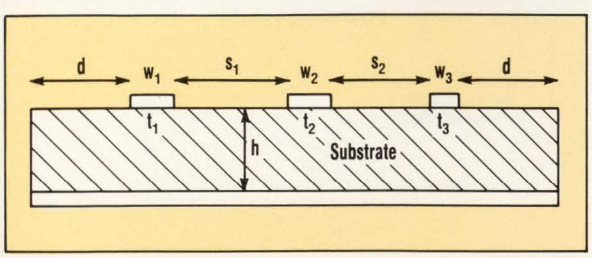
Sometimes a long line is loaded at periodic intervals with gates through smaller traces. These can be analyzed by considering them as separate lines. Otherwise, the engineer must use an effective loading per unit length of the long lines. This loading may have a resistive component in addition to a capacitive component, making the line effectively lossy.

The ability to simulate lossless uncoupled lines, though very important, isn't always enough. Loss and coupling are often important in transmission lines.

There are two sources of loss in transmission lines: conductor loss and dielectric loss. Conductor loss is due to the resistance of the traces that constitute the transmission line and is usually specified as resistance per unit length. Dielectric loss is due to



6. A driven transmission line can couple to a nearby passive line (a). Here, active transitions at the input of gate 2 cause more than a volt of crosstalk at the input of gate 4 (b).



5. Typically, transmission lines in pc boards and MCMs aren't isolated. The example multiple-trace microstrip line, which can be considered as a coupled transmission line, illustrates this.

losses in the substrate material. It's specified as a loss tangent for the substrate material. Both these quantities are functions of frequency and are hard to specify, especially when doing transient analysis. Moreover, very few circuit simulation programs can take even frequency-independent losses into account.

The easiest quantity to calculate is the resistance of the conductor at dc. The resistance per unit length R at dc is given by:

$$R = 1/\sigma A \qquad (7)$$

σ is the conductivity of the trace material (usually copper) and A is the area of conductor's cross section. Unfortunately, the ac resistance can be considerably higher. This is because of skin effect that makes the current flow on the surface rather than uniformly across the whole cross section. For a microstrip conductor, the current flows mainly in a thin layer near the bottom surface—it's much higher near the outer edges than it is at the center. However, the opposite can be said for the ground plane *(Fig. 3)*. As the current flows across a much greater width in the ground plane, the microstrip conductor resistance dominates.

Expressions for the ac resistance of a microstrip line are complex. An approximate resistance per unit length for a wide microstrip at high frequencies is given by:

$$R_{hf} = R_s/w \qquad (8)$$

The sheet resistance, R_s, is equal to $(\pi f \mu/\sigma)^{1/2}$, where f is the frequency and μ is the permeability ($\mu = 12.56 \times 10^{-7}$ H/m). The assumption that the microstrip is wide implies that w > h. The high-frequency assumption indicates that the thickness of the strip over which the current flows (i.e. skin depth) is much smaller than the thickness t of the strip. Equation 8 tends to overestimate the loss and the resistance, while equation 7 underestimates it.

Two loss mechanisms are associated with dielectrics. The first stems from the dielectric being slightly conducting with a finite conductivity σ_{dc} even at dc. The second arises because the polarization process dissi-

pates energy at higher frequencies even though the conductivity is zero. It is this polarization loss that dominates for most dielectrics used as substrates in pc boards and MCMs. However, for semiconductor substrates (such as GaAs), the conductivity may also be important. One can talk of an effective σ_{eff} due to both components of loss in a dielectric. The ratio of conduction current to displacement current in a lossy dielectric is called the loss tangent or dissipation factor and is given by:

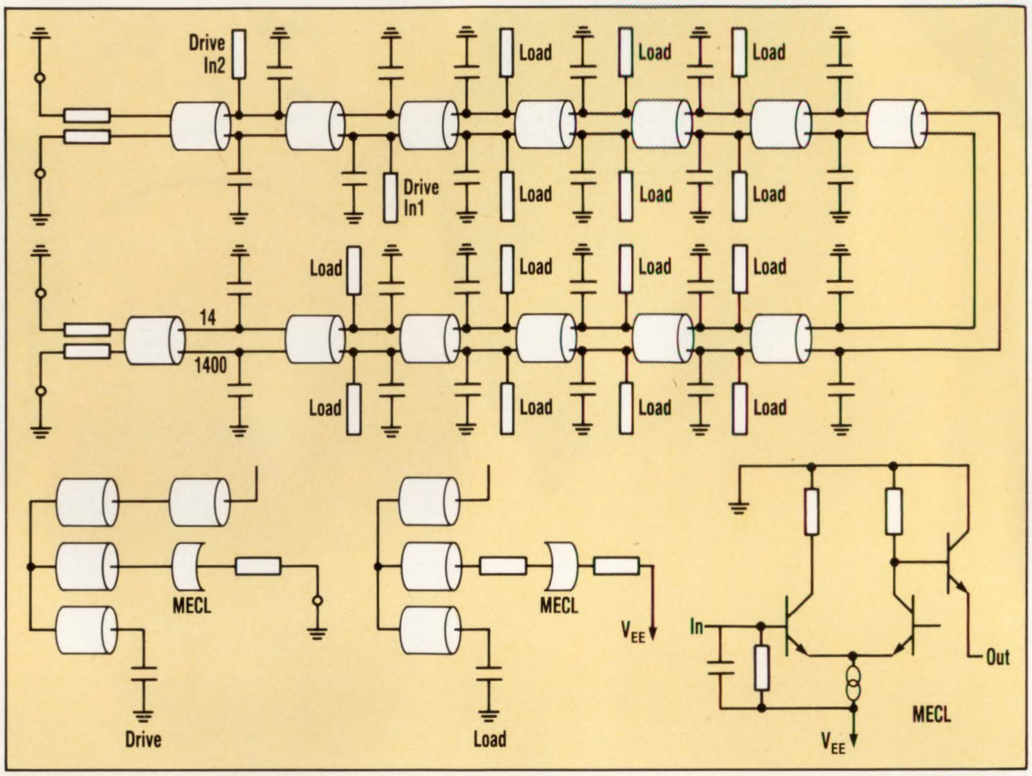
$$\tan \phi = \sigma_{eff}/\omega\epsilon \qquad (9)$$

ϵ is the dielectric constant ($\epsilon_r \times 8.854 \times 10^{-12}$ F/m).

Values for loss tangent for different substrates can be obtained from manufacturers' data sheets. Typical values in the gigahertz range are about 0.001. Where the polarization loss dominates, the loss tangent is roughly independent of frequency within at least one order of magnitude variation of frequency. In other words, the effective conductivity due to polarization loss increases somewhat linearly with frequency.

Even if a designer can accurately calculate, find, or measure resistances and loss tangents for a line, simulation still presents many roadblocks. Most circuit simulators, including the public-domain Spice3c1, can handle only lossless lines. Even if a circuit simulator can handle loss, it's usually only the conductor loss, as opposed to the dielectric loss. For conductor loss, skin effect (variation of ac resistance with frequency) is usually not considered.

ContecSpice, a circuit simulator with more sophisticated transmission-line models, uses the dc resistance and the limiting high-frequency resistance when doing transient analysis. The values are correct at dc and at extremely high frequencies, but approximate for intermediate frequencies. The simulation is correct where the waveforms



7. These ECL drivers drive ECL loads through coupled transmission lines. The drivers and loads themselves contain other transmission lines.

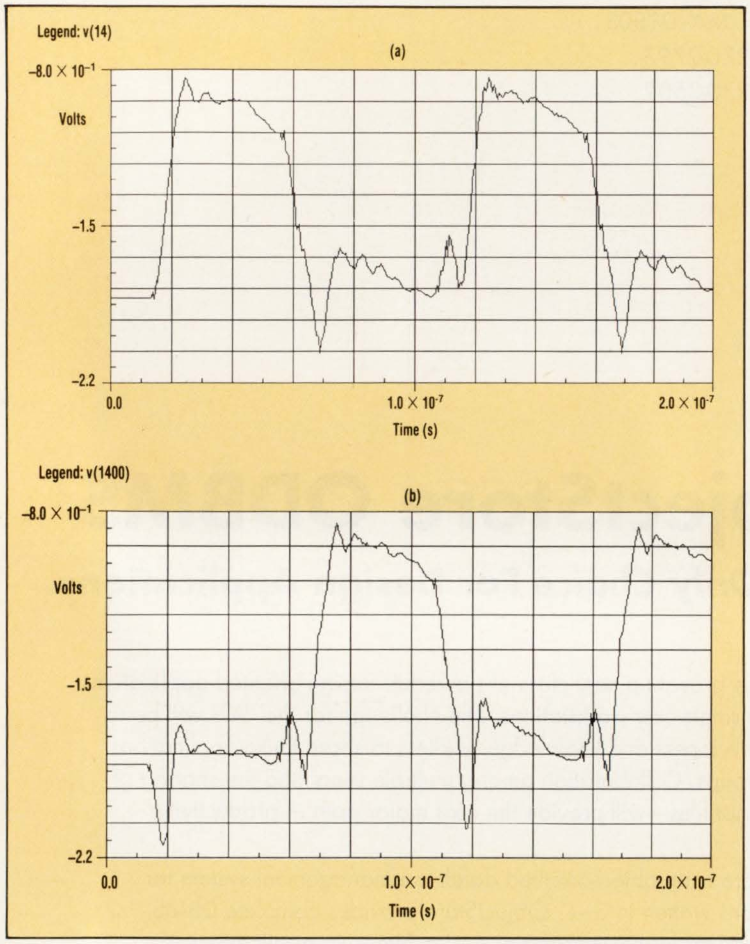
don't change at all, or if they change very fast. For digital circuits, this covers most of the waveform. ContecSpice expects users to give the loss tangent in terms of a parallel conductance (G) per unit length for the line. G can be calculated from the loss tangent or σ_{eff} using the following relation for a microstrip:

$$G = \frac{q\sigma_{eff}}{\sqrt{\epsilon_{re}}} \times \left[\frac{\sqrt{\frac{\mu}{\epsilon_0}}}{Z_0} \right] \qquad (10)$$

ϵ_{re} is the effective dielectric constant *(see equation 2)* and q is a dielectric filling factor, taking into account the fields of the microstrip line that go partly through lossless air and partly through the dielectric substrate. The filling factor q is given by $(\epsilon_{re} - 1)/(\epsilon_r - 1)$.

Most simulators can't handle frequency-dependent R and G (or loss tangent), so it's usually necessary to choose an approximate frequency when calculating these parameters. For transient analysis, it's common to select a frequency equal to $0.35/t_{rf}$ where t_{rf} is the smaller of the rise and fall times. If values of R and G calculated at this frequency are used, losses or attenuation predicted during times when the signals aren't changing rapidly will be exaggerated.

Though simulation of losses in a transmission line is difficult, losses are often important to consider. When they are considered, mismatch effects are usually less severe then what lossless lines may predict. Series losses (due to R) have roughly the same effect as a series termination. In addition, parallel losses (due to G) have almost the same effect as a parallel termination. The waveform changes at the circuit's gate-2 input without series resistance when losses are considered in the line *(Fig. 4)*. Rather than assume a Z_o, the C, L, R, and G per unit length were calculated from the physical dimensions using the program LINPAR. The dimensions of the line were: w = 0.1 mm, t = 0.01 mm, h = 0.075 mm, ϵ_r = 3.2, loss tangent = 0.001, and length l = 1 m.



8. The Waveforms v(14)(a) and v(1400)(b) at the end of the transmission line show effects of ringing and cross coupling. The two waveforms correspond to two-phase non-overlapping clocks.

The waveform shows results for the following three cases:

1. Lossless line

2. When ac resistance corresponding to 350 MHz is used

3. When frequency dependence of resistance due to skin effect is considered

The input in this case was a single pulse. It can be seen that the ringing in the case of the lossless line is much more pronounced. The simulation with fixed R overestimates the loss when the waveform doesn't change rapidly and underestimates when it does. The simulation with skin effect is closer to the lossless line when the waveform isn't changing rapidly and further away from the lossless line when it is. This is expected from skin effect considerations. Skin effect should also be considered when finding steady-state levels if there's significant V_{OH} degradation due to parallel termination. Using a fixed value of R calculated at a high frequency will exaggerate the degradation.

A convenient way of calculating electrical parameters to feed to circuit simulators for lossy lines is to use special programs that compute C, L, R, and G for various microstrip and stripline configurations.

The various examples explored to this point did not take into account coupling between lines. The transmission lines in a pc board and/or MCM are usually not isolated, and other lines are typically close to the one of interest *(Fig. 5)*. In a system of coupled transmission lines, coupling effects are often more important than losses. Unfortunately, it's even more difficult to simulate a set of coupled (lossless or lossy) transmission lines. The alternative is to design boards with traces widely separated, which is not always possible even if an engineer is willing to tolerate the inefficiency.

An example circuit containing fast TTL gates has a passive line adjacent to an active line *(Fig. 6a)*. Crosstalk effect exists on the passive line *(Fig. 6b)*. The dimensions for the two microstrip lines are as follows: w = 0.1 mm, t = 0.01 mm, h = 0.075 mm, l = 0.25 m (for both lines), separation s between lines = 0.1 mm, $\epsilon_r = 3.2$, and loss tangent = 0.001. The crosstalk on the inactive line going up to more than 1 V is enough to make it unacceptable. Therefore, both lines were terminated using a Thevenin termination. Rapid changes on the driven line cause coupling or crosstalk. If the driven line wasn't terminated, the crosstalk would have been much higher. The crosstalk is mainly forward crosstalk, which refers to signals coupling from the driven line to the inactive line and traveling toward the load end. Similarly, backward crosstalk concerns signals coupling onto the inactive line and traveling toward the source end.

Proper terminations are important *(Fig. 6b, again)*. Note that additional rising and falling edges are at the input to the driven gate because the matching termination isn't quite perfect (at 6.5 ns and 17.25 ns, for example). This introduces additional crosstalk in the passive line. If no termination was used, the crosstalk would have been as serious a problem as the ringing on the driven line.

In addition to the spacing s between the traces, the configuration can be very important from crosstalk considerations. Stripline configurations produce more than an order of magnitude less crosstalk as compared with similar microstrip configurations.

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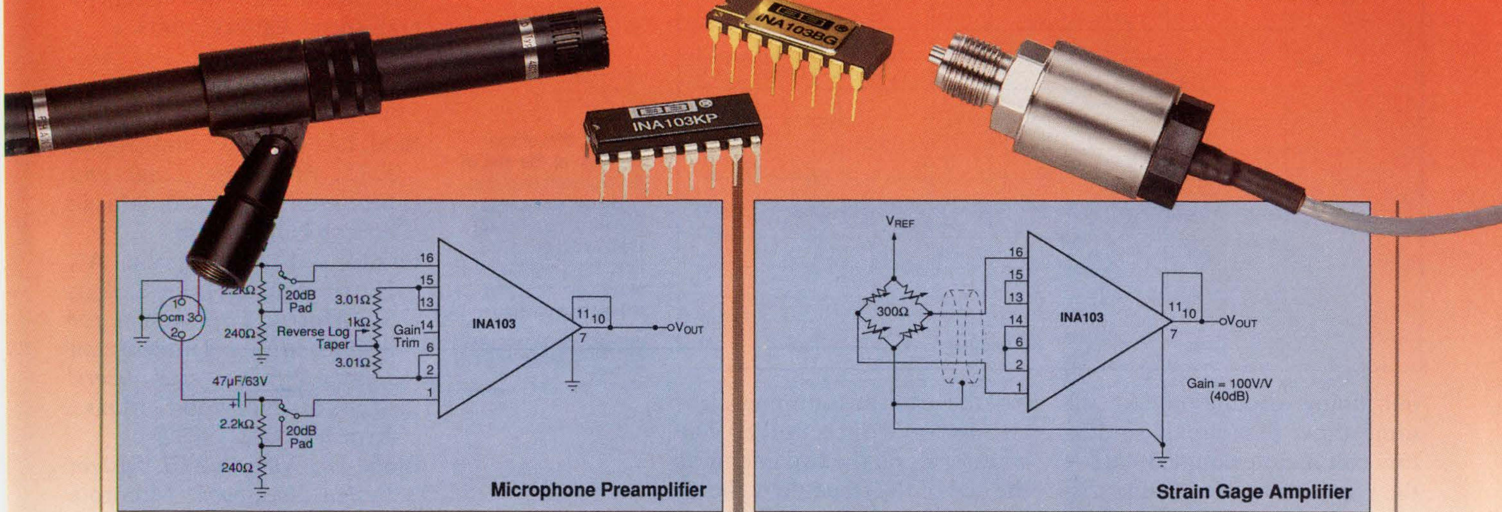

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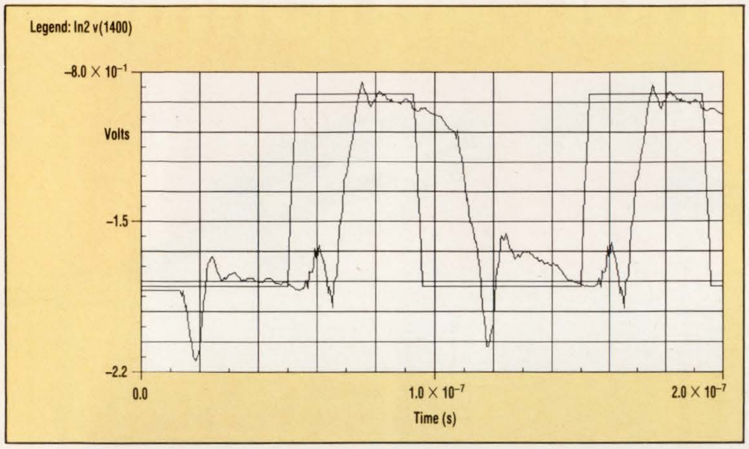

9. Here, Waveform v(1400), at the end of the transmission line, is shown along with the clock input (In2) that's applied to the line. The ringing, cross coupling, and delays are obvious.

out doing simulation. At the same time, few circuit simulators can handle coupled lines—they have to be modeled as distributed systems. Using lumped elements to represent the coupling can be very tedious and impractical. The results shown in Figure 6b were obtained using ContecSpice, which has models for coupled transmission lines. But even using the models does not completely suffice. The electrical parameters required to describe coupled lines are C, L, R, and G matrices. The task of calculating these matrices from the transmission line's physical description can be handled by relatively inexpensive programs.

As an example, consider ECL gates driving coupled transmission lines *(Fig. 7)*. Two ECL gates, labeled Drive, supply current to loads through a complex interconnection of transmission lines. The loads are also ECL gates, and they're labeled Load. The two long lines, driven by non-overlapping two-phase clocks, are coupled. Models for Drive and Load contain transmission lines themselves, but these are uncoupled or single transmission lines. The total circuit contains 13 sections of widely varying lengths of the coupled line. In addition, it has 50 sections of lossless lines with different delays. The ECL gates are represented at the circuit or transistor level; 48 transistors are in the circuit.

This system was analyzed using the transmission-line algorithms in ContecSpice. The waveforms on the two lines near the end of the trace show the effects of loss and coupling, evidenced by the ringing and crosstalk *(Fig. 8)*. The clock input In2 is also plotted with the corresponding signal near the end of the line *(Fig. 9)*. This shows the delay and distortion suffered by the signal. The simulation took about 15 minutes on a Sparcstation I, and required 328 kbytes of memory for the data.

Circuits of this complexity require simulation for both design and verification. The nonlinear loads and drivers require that a circuit simulator be used, rather than special-purpose transmission line programs. In the ECL-circuit example, the loading is distributed all along the line, which makes it more necessary to verify the effects of mismatches, crosstalk, and loss. It's also necessary to split the long line into sections. This way the effect of each load is fully accounted for.

This example brings out the power of present day circuit simulators in their ability to simulate coupled lossy transmission lines. Simulators like ContecSpice use analog behavioral models for digital gates. This makes it possible to develop macromodels for digital elements from the specifications without going to a transistor-level description. Combined with fast efficient algorithms to simulate transmission lines, simulators constitute a valuable tool to analyze transmission-line effects on high-speed digital circuits.

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Paul K. U. Wang, Contec's executive vice president, obtained a PhD EE from the University of Cincinnati.

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- 100's of models to choose from

For more information contact MELCHER at 800-828-9712.

CIRCLE 144

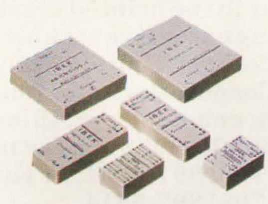
MELCHER

DC-DC'S FROM 1...10 WATTS
DISTRIBUTED POWER, 4:1 INPUTS

For distributed power or hand-held instrument applications, the ICR, IWR & IPS units offer the widest input ranges and fully regulated outputs in low profile, PC board-mount packages. These units are completely isolated and available with up to three outputs.

- Input ranges of 4.5...5.5, 10...33, and 18...72 Vdc
- Isolation voltages from 500...8kVdc
- Single, Dual, Triple outputs of 2...48 Vdc
- -25...71°C, -40...85°C ambient
- Industry Standard pinning

For more information contact MELCHER at 800-828-9712.



CIRCLE 145

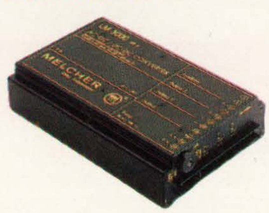
MELCHER

50 WATT DC-DC/AC-DC CONVERTERS
5:1 DC INPUT, UNIVERSAL AC INPUT

The M series offers complete versatility for systems requiring extremely wide AC or DC inputs, high isolation, and rugged power conversion products. These units are well-suited for Airborn Instrumentation, Locomotive/Process Controls, and Telecom applications.

- 8...35, 14...70, 28...140, 44...220 Vdc, 85...264 Vac Inputs
- Single, Dual, Triple outputs, 2...48 Vdc
- UL/CSA/VDE, British & French Rail Board Approved
- MIL-STD 704D (28V, 115V/400Hz)
- Isolation up to 4,000 Vrms
- Open/Short circuit proof

For more information contact MELCHER at 800-828-9712.



CIRCLE 146

MELCHER. DEMAND THE BEST FOR THE MOST DEMANDING CONDITIONS.

© Chuck O'Rear/West Light

Melcher builds power supplies that withstand the worst electrical and environmental conditions. All the components you need to combat extended temperature ranges, shock and vibration, and any input voltage. For more than 18 years designers around the globe have been specifying Melcher's leading edge power conversion technology for locomotive, telecommunications, off-road machinery, process controls and medical instrumentation applications. A gold medal reputation that promises the industry's best cost/performance ratio. Ask for the power supply you can 'fit and forget'. Ask for Melcher.

The standard of excellence.

CIRCLE 147

To receive additional technical literature or to speak to an application engineer, call

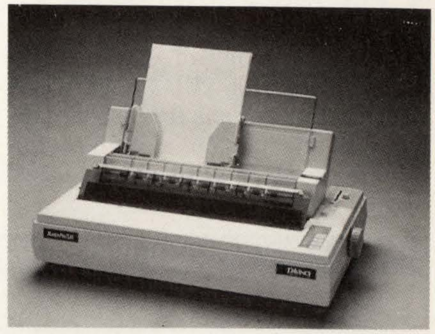
1-800-828-9712.

MELCHER

MELCHER, INC. 200 Butterfield Drive, Ashland Massachusetts 01721
Tel. 508-881-4715 Fax 508-881-5082

▼ PENLESS PLOTTER ADDS NEW UTILITIES

The newest version of the RasterPro 720 penless plotter has three new performance utilities: ProControl, ProADI, and ProLP. In addition, the plotter has more internal memory and a new controller board based on surface-mounted technology. ProControl is a menu-driven, DOS utility that designers use to set up plotter-output specifications directly from their computers. ProADI is a DOS software driver for plotting files

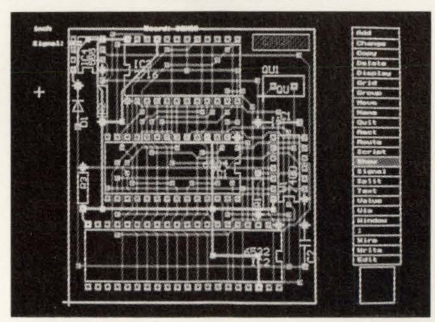


from within AutoCAD, and ProLP is a long plot firmware utility for creating A- and B-size drawings of any length. The base price of the RasterPro 720 penless plotter, which is shipping now, is $3495.

Da Vinci Graphics Inc.
870 Hermosa Dr.
Sunnyvale, CA 94086
(408) 737-8800
▶ **CIRCLE 341**

▼ MODULAR PCB SOFTWARE SUITS ANY NEEDS

Users can match their design system to their particular needs with the Eagle modular pc-board design system. It runs on PCs, and takes users from schematic capture through completed board design. Eagle consists of three main modules: layout editor,



autorouter, and schematic editor. Because all of the modules share the same database and operate within one environment, moving from one module to another doesn't require leaving the system or booting a separate program. The Eagle design system, which is shipping now, costs $399 without the autorouter and $699 with it. The schematic editor is an additional $495.

American Small Business Computers Inc.
327 S. Mill St.
Pryor, OK 74361
(918) 825-4844
▶ **CIRCLE 342**

PC-BOARD CAD TOOLS

Company	Component placement	Manual routing	Auto-routing	Analysis*	Other**
Accel Technologies Inc., 6825 Flanders Dr., San Diego, CA 92121-2986; (800) 488-0680. **CIRCLE 300**	D	D	D	D	
American Small Business Computers Inc., 327 S. Mill, Pryor, OK 74361; (918) 825-4985. **CIRCLE 301**	D	D	D		
Aptos Systems Corp., 1711 Trout Gulch Rd., Aptos, CA 95003; (408) 662-8364. **CIRCLE 302**	D	D	D		D
Cadam Inc., 1290 Parkmoor Ave., San Jose, CA 95126; (408) 971-1300. **CIRCLE 303**	U,D	U,D	U,D		U,D
CAD Innovations, 835 Blossom Hill Rd., Suite 216, San Jose, CA 95123; (408) 224-8088. **CIRCLE 304**				D	
CAD Software Inc., 119 Russell St., Littleton, MA 01460; (508) 486-9521. **CIRCLE 305**	D	D	D	D	D
Cadence Design Systems Inc., 555 River Oaks Pkwy., San Jose, CA 95134; (408) 983-1234. **CIRCLE 306**	U	U	U	U	
Cadisys Corp., 2099 Gateway Pl., Suite 400, San Jose, CA 95110; (408) 441-8800. **CIRCLE 307**	D	D	D	D	
Cadix International Inc., 2301 Maitland Center Pkwy., Suite 445, Maitland, FL 32751; (407) 875-0007. **CIRCLE 308**	U	U	U		U
Calay Systems Inc., 16842 Von Karman, #100, Irvine, CA 92714; (714) 863-1700. **CIRCLE 309**	U	U	U		U
Computervision, 100 Crosby Dr., Bedford, MA 01730; (617) 275-1800. **CIRCLE 310**	U	U	U		
Cooper and Chyan Technology Inc., 1601 Saratoga-Sunnyvale Rd., Suite 255, Cupertino, CA 95014; (408) 366-6966. **CIRCLE 311**			U		
Dazix, an Intergraph Co., One Madison Industrial Park, Huntsville, AL 35894-0001; (205) 730-8708. **CIRCLE 312**	U	U	U	U	U
Design Computation, 1306 State Hwy. 33, Farmingdale, NJ 07727; (908) 938-6661. **CIRCLE 313**	D	D	D		
The Great SoftWestern Co. Inc., 919 S. Carroll Blvd., Suite 103, Denton, TX 76201-6869; (800) 231-6880. **CIRCLE 314**	D,M	D,M	D,M		
HyperLynx Inc., P.O. Box 3578, Redmond, WA 98073-3578; (206) 869-2320. **CIRCLE 315**				D	
Integrity Engineering Inc., 1306 W. County Rd. F, Suite 100, St. Paul, MN 55112; (612) 636-6913. **CIRCLE 316**				D,M	
Interactive CAD Systems, 2352 Rambo Ct., Santa Clara, CA 95054; (408) 970-0852. **CIRCLE 317**	D	D	D		
Massteck Ltd., 95 Russell St., Littleton, MA 01460; (508) 486-0197. **CIRCLE 318**		U,D,M	U,D,M		

Key: U = Unix D = DOS M = Macintosh
* Tools that analyze heat, transmission-line effects, etc.
** Miscellaneous tools that aid pc-board design
Call companies for details.

▼ PCB TOOLS NOW RUN ON SPARC WORKSTATIONS

The Theda family of electronic-design-automation (EDA) software, which includes tools for pc-board design, now runs on a high-performance graphics workstation based on the Sparcstation 2 from Sun Microsystems. Called the 52P CADD-Station, the new workstation performs at 28.5 MIPS and 4.2 MFLOPS. Theda PCB Interactive is a bundled hardware-software package for schematic drafting and interactive pc-board layout. Theda PCB Design is a bundled package that offers automatic place and route, manufacturing output and documentation, simulation and analysis, and electronic-rules checking. The two packages cost $52,900 and $72,500, respectively.

Computervision, a Prime Co.
100 Crosby Dr.
Bedford, MA 01730-1480
(617) 275-1800
▶ **CIRCLE 343**

PC-BOARD CAD TOOLS

Company	Component placement	Manual routing	Auto-routing	Analysis*	Other**
Mentor Graphics Corp., 8005 S.W. Boeckman Rd., Wilsonville, OR 97070; (800) 547-3000. **CIRCLE 320**	U	U	U	U	U
Omation Inc., 801 Presidential Dr., Richardson, TX 75081; (214) 231-5167. **CIRCLE 321**	D	D	D		D
Orcad, 3175 N.W. Aloclek Dr., Willsboro, OR 97124; (503) 690-9881. **CIRCLE 322**	D	D	D		
Phase Three Logic Inc., 1600 N.W. 167th Pl., Beaverton, OR 97006; (503) 645-0313. **CIRCLE 323**	D	D	D		D
Protel Technology Inc., 50 Airport Pkwy., San Jose, CA 95110; (800) 544-4186. **CIRCLE 324**	D,M	D,M	D,M		
Quad Design Technology Inc., 1385 Del Norte Dr., Camarillo, CA 93010; (805) 988-8250. **CIRCLE 325**				U	
Quantic Laboratories Inc., 281 McDermot Ave., Suite 200, Winnipeg, Manitoba, Canada R3B OS9; (204) 943-2552. **CIRCLE 326**				U	
Racal-Redac Inc., 238 Littleon Rd., Westford, MA 01886; (508) 692-4900. **CIRCLE 327**	U,D	U,D	U,D	U	U
Royal Digital Systems, 2855 Kifer Rd., Santa Clara, CA 95050; (408) 980-9492. **CIRCLE 328**	U	U	U		U
Rubow Systems, 19102 Bridwell St., Glendora, CA 91740; (818) 914-3963. **CIRCLE 329**	D	D	D		D
Scientific Calculations, 7796 Victor-Mendon Rd., Fishers, NY 14453; (716) 924-9303. **CIRCLE 330**	U	U	U		
Shared Resources Inc., 3047 Orchard Pkwy., San Jose, CA 95134; (408) 434-0444. **CIRCLE 331**	U	U	U		U
Swiftlogic Inc., 5201 Great America Pkwy., Santa Clara, CA 95054; (408) 562-6060. **CIRCLE 332**				U	
Task Technologies Inc., 6 N. Main St., Fairport, NY 14526; (716) 377-1060. **CIRCLE 333**	U	U	U		U
Teradyne Inc., EDA Div., 5155 Old Ironsides Dr., Santa Clara, CA 95054; (800) 777-2432. **CIRCLE 334**	U,D	U,D	U,D		
Ultimate Technology, 1725 Montgomery St., San Francisco, CA 94111; (415) 391-2433. **CIRCLE 335**	D	D	D		
Valid Logic Systems Inc., 2 Omni Way, Chelmsford, MA 01824; (508) 256-2300. **CIRCLE 336**	U	U	U	U	U
Vamp Inc., 6753 Selma Ave., Los Angeles, CA 90028; (213) 466-5533. **CIRCLE 337**	M	M	M		
Viewlogic Systems Inc., 293 Boston Post Rd. West, Marloboro, MA 01752; (508) 480-0881. **CIRCLE 338**	U,D				
Visionics Corp., 3032 Bunker Hill Ln., Suite 201, Santa Clara, CA 95054; (408) 492-1440. **CIRCLE 339**	D	D	D	D	
Wintek Corp., 1801 South St., Lafayette, IN 47904; (800) 742-6809. **CIRCLE 340**	D	D	D		

Key: U=Unix D=DOS M=Macintosh
* Tools that analyze heat, transmission-line effects, etc.
** Miscellaneous tools that aid pc-board design
Call companies for details.

▼ PC-BASED SIMULATOR HAS WORKSTATION SPEED

The Ultisim interactive digital simulator for pc-board designers runs on PCs, but has the speed of workstation-based simulators. It's a 28-state simulator that performs functional simulation and timing analysis. In addition, Ultisim comes with TTL, CMOS, ECL, and PLD library models. With a Viewtrace option, users can view analog and digital simulation results at the same time. All Spice-compatible analog simulators are supported in the Viewtrace option. Ultisim runs in the 32-bit protected mode of 386- and 486-based PCs. Depending on capacity, prices range from $1295 to $7375.

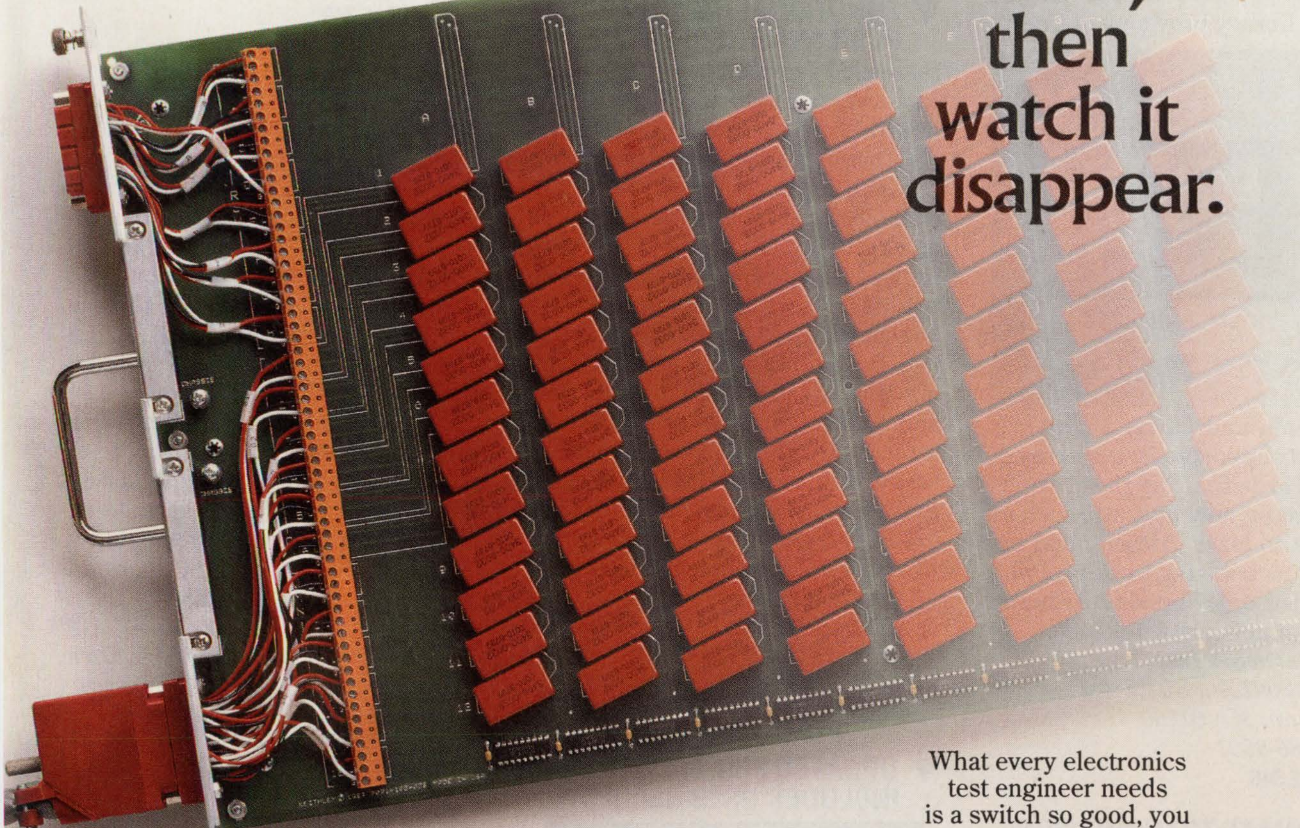
Ultimate Technology
1725 Montgomery St.
San Francisco, CA 94111
(415) 391-2433
▶ **CIRCLE 344**

▼ AUTOROUTER INCLUDES TESTABILITY FEATURES

Version 2.0 of the Specctra pc-board autorouter introduces routing for testability into the design cycle. The router's flexible Force Via command adds a testable via to each signal on the board for bed-of-nails testing later on. Force Via invokes the tool's push-and-shove algorithms to expose vias on either board surface. The Specctra Version 2.0 autorouter is shipping now for HP, IBM, and Sun workstations. Depending on the platform, it costs between $29,000 and $39,000.

Cooper and Chyan Technology Inc.
1601 Saratoga-Sunnyvale Rd.
Suite 255
Cupertino, CA 95014
(408) 366-6966
▶ **CIRCLE 345**

Hook up a Keithley switch, turn it on, then watch it disappear.



What every electronics test engineer needs is a switch so good, you hardly know it's there.

Try a Keithley switch. Switch signals down to a picoamp or nanovolt, and up to 1300V, 5A, or 500MHz. All with minimal signal degradation and maximum reliability.

Choose from a full line of switch mainframes and 40 different cards. There's a combination that's right for your application.

Call 1-800-552-1115 to speak directly with a Keithley applications engineer. We'll help you design a test system. Even FAX you a completed configuration diagram.

Keithley switches. Hook one up. Then watch it disappear.

KEITHLEY INSTRUMENTS

CIRCLE 192

▼ SCHEMATIC TOOL WORKS FROM FAST DATABASE

The Pads-Logic Version 2.0 schematic-capture software enjoys the advantages of a multisheet-oriented database, but still has the quick-response time of a single-sheet-oriented database. Multisheet databases can hold all of the design information in memory, and have 100% data tranfser to pc-board design. Version 2.0 boasts library browsing of graph-

ical symbols and parts; a graphics driver that supports a larger array of graphics cards than did the previous version; many new outputs, such as interfaces to laser printers; and improved data transfer to PSpice and Susie. Pads-Logic Version 2.0 runs on PCs. It's shipping now for $450.

CAD Software Inc.
119 Russell St., Suite #6
Littleton, MA 01460
(508) 486-9521
▶CIRCLE 346

▼ AUTOMATE TRANSMISSION-LINE ANALYSIS FOR PCBs

Pathfinder is a software program that automates methods of transmission-line analysis in pc boards. It uses the layout information from the routed board as an input so that the actual trace topology can be simulated. Then, users can scan an entire board to find timing and noise problems. The software takes a modular approach to cover three important areas: transmission-line analysis, crosstalk analysis, and static-timing analysis. The base module (transmission-line module) includes Netview, a graphical analysis tool that lets users work interactively with problem nets. They can perform "what-if" evaluation by changing line impedances and termination methods to fix noise problems. By combining the full board scan with Netview, users can find problem areas, and then fix them right on the screen. Pathfinder, which runs on PCs, costs between $4000 and $11,000, depending on the modules purchased.

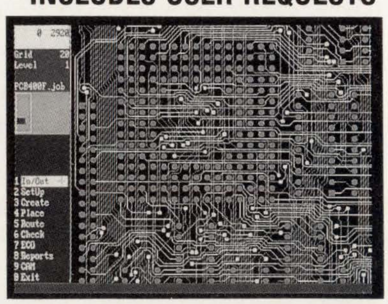
Integrity Engineering Inc.
1306 W. County Rd., Suite 100
St. Paul, MN 55112
(612) 636-6913
▶CIRCLE 347

▼ FUNCTIONALITY ADDED TO PCB LAYOUT SOFTWARE

Increased functionality is one benefit to Version 4 of the Schema-PCB board-layout software. Version 4 also includes an improved user interface and greater flexibility in output. Enhanced part editing and creation is combined with the ability to browse the library based on part attributes. Users can create their own keyboard macros to streamline tool use. In addition, a new net-highlighting feature includes both the pads and connections that are routed interactively. The software supports a large number of high-resolution graphics cards. Base price for Schema-PCB Version 4, which runs on PCs, is $975. It's shipping now.

Omation Inc.
801 Presidential Dr.
Richardson, TX 75081
(800) 553-9119
▶CIRCLE 348

▼ UPDATED PCB SYSTEM INCLUDES USER REQUESTS



Many user requests were incorporated into Version 4.0 of the Pads-PCB pc-board design system. One major enhancement is a new parts library and library manager. The CAE and pc-board libraries have been combined into one library to serve both applications. The library manager permits instant access and graphical browsing of thousands of parts. A checking feature ensures that all thermal pads are on power and ground planes. Users can create both stored and on-the-fly macros. In addition, the user interface has a "fill in the form" format to enter alphanumeric data. Pads-PCB Version 4.0 is available now for $975. Pads-PCB users without the support option can buy Version 4.0 for $350.

CAD Software Inc.
119 Russell St., Suite #6
Littleton, MA 01460
(508) 489-8929
▶CIRCLE 349

▼ ANALYSIS TOOL MODELS NONLINEAR DRIVERS

Release 4.1 of the Crosstalk Tool Kit (XTK) timing- and signal-analysis software for high-speed board design models nonlinear circuits more accurately. A new algorithm and input format support a simple and accurate method of modeling the current-drive characteristics of nonlinear drivers and receivers. In addition, the input format makes it easy to specify models from the physical measurements of the driver or directly from Spice models. Other enhancements to XTK 4.1 include enhanced output-reporting capability. XTK 4.1 runs on a range of workstations under X-Windows. It's available now, and costs between $27,000 and $69,000, depending on platform and configuration.

Quad Design Technology Inc.
1385 Del Norte Rd.
Camarillo, CA 93010
(805) 988-8250
▶CIRCLE 350

▼ THERMAL ANALYSIS FOR POWER SUPPLIES

Designers working on a PC can perform thermal analysis of power supplies during the design stage with the Betasoft-R CAE software. Betasoft-R accounts for various transformers, capacitors, and resistors in addition to the microelectronics in power supplies. The power supply can be located at any elevation; under natural or forced-air cooling; and with heat sinks or heat-spread planes attached. The software, which runs on PCs, models 3D flow and thermal fields. It's shipping now for $1995.

Dynamic Soft Analysis Inc.
213 Guyasuta Rd.
Pittsburgh, PA 15215
(412) 781-3016
▶CIRCLE 351

PCB CAD PRODUCTS

▼ MAJOR UPGRADE FOR PCB ANALYSIS SOFTWARE

The newest version of the Greenfield analysis software offers more simulation capability, customized unbundled solutions, easier access to programs in the Greenfield suite, and a range of user-friendly features. Greenfield is a high-speed simulator for printed circuit boards, cables, connectors, hybrids, and integrated circuits. It accurately simulates circuits with multiconductor, coupled transmission lines. With Version 3.0, the library of drivers and receivers includes behavioral models for Fast, ALS, CMOS, biCMOS, and ECL devices. In addition, a new front-end screen lists all of the programs available in the Greenfield suite. Consequently, the programs are easier to start and access. Greenfield Version 3.0, which runs on a number of Unix workstations, will ship in the second quarter. Pricing for the software starts at $24,500.

Quantic Laboratories Inc.
281 McDermot Ave., Suite 200
Winnipeg, Canada R3B OS9
(800) 665-0235
▶ CIRCLE 352

▼ PCB DESIGN SYSTEM RUNS ON MACINTOSH COMPUTERS

Designing either digital or analog boards is made easier with the Mac Autotrax pc-board design system for Macintosh computers. Autotrax handles large, multilayer boards with through-hole and surface-mounted components. It features automatic component placement, and interactive and automatic routing. Net lists can be generated from Autotrax or imported from other tools. Other highlights of the tool include: autopanning; automatic solid-copper polygon fills; 45°, 90°, and curved tracks; and on-the-fly library-component creation. The Autotrax user interface was designed around the Mac's graphical interface standards. In addition, all files created with Mac Autotrax are fully compatible with the software's IBM version. The Mac Autotrax software is shipping now for $2495.

Protel Technology Inc.
50 Airport Pkwy.
San Jose, CA 95110
(800) 544-4186
▶ CIRCLE 353

▼ TRANSMISSION-LINE TOOL USES EXTENDED MEMORY

LineSim Pro is a transmission-line analysis tool that runs on IBM-compatible 386- or 486-based computers in extended memory. Rather than surveying a board after layout, LineSim Pro is intended for design of critical traces before layout begins. It's can simulate complex pc-board trace geometries—a minimum of 200 transmission-line segments per electrical net. LineSim Pro also models pc-board traces. Windows for common trace geometries calculate transmission-line impedance based on trace dimension and board construction. The circuit to be simulated is specified in a "push-button" schematic, meaning that circuit elements are clicked in and out with a mouse. The simulation is shown in an oscilloscope-like display. LineSim Pro is available now for $995, which includes one year of updates. The software is shipped with both a hard-copy and on-line manual.

HyperLynx Inc.
P.O. Box 3578
Redmond, WA 98073-3578
(206) 869-2320
▶ CIRCLE 354

▼ COMPLETE ANALOG BOARD DESIGN IN ONE PACKAGE

The Analog Systems Lab (A/S Lab) from Valid Logic is the first software package to offer front-to-back design of analog pc boards. A/S Lab leverages the ValidFrame framework technology to combine the company's Analog Workbench II and Release 5.0 of the Allegro pc-board design system. The resulting system offers designers electrical and physical design, as well as in-process analysis tailored for analog boards. Other features specifically for analog design include curved traces and the creation of intelligent shapes with curved boundaries to minimize signal discontinuity and maximize signal-to-noise ratios. A/S Lab will begin shipping in May. The package, which can be shared over a network on DEC, IBM, and Sun workstations, goes for $45,000.

Valid Logic Systems Inc.
2820 Orchard Pkwy.
San Jose, CA 95134
(408) 432-9400
▶ CIRCLE 355

WHAT'S ALL THIS PERFECTION STUFF, ANYHOW?

Once upon a time, a lady went shopping for shoes. She went into a shoe store and said to the salesman, "My good man, I would like to buy some alligator shoes." The salesman showed her some alligator shoes. But *this* one had a flaw, and *that* one had a blemish, and *that* one had a scratch. He went back and got more shoes. But when the lady inspected them, she found an imperfection that was unacceptable to her every time. Finally, he brought out every pair of shoes he had, and she was not prepared to buy shoes with such defects. In great exasperation, the salesman told her, "Look, lady, you're not perfect. I'm not perfect. How do you expect an alligator to be perfect?"

BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

One of my latest ventures involves the writing of a book. On October 30, 1990, I handed in a complete, polished manuscript. I don't know how many words, or how many pages, but it was about 700,000 bytes, and the Fed Express guy had to struggle to get it on its way. This was a refinement of some stories on the troubleshooting of analog circuits I wrote a couple years ago. I took the old stories and added a lot of new info, tweaked and refined a lot of the text, and corrected some typo errors, finally rounding it into pretty good shape. With a little luck, the book will come out on schedule this month.

On November 14, I sent to the publisher a package of new corrections and changes. Only one envelope, but there were 28 items in there. When I talked with the publisher, I could tell she was smiling, seeing that I was willing to put so much effort into getting things right. On November 30, I assembled an envelope with more corrections, changes, refinements, and upgrades. I mean, some of the people had moved in the last month, so I certainly had to put in an address correction. In several cases, the distributors who sold things didn't sell them any more. In other instances, I remembered a new technique that I had forgotten previously. So, when I send in this package, I'm really making progress—because there are only 27 items.

Next week I expect to remember a couple more items. I'm not sure exactly when the smile will completely disappear from my publisher's face, but it's only a matter of time. She will say, "It's time to shoot the engineer, and put this to bed and print what we've got." And I'm sure I will have to agree with her pretty quickly. But meanwhile, I know I have to correct the spelling of one guy's name. We can't leave that wrong. And an old friend is mailing me some more info on some diodes...and there are curves that don't look quite right ...and there are some photographs that still have to be developed, not to mention the ones that haven't yet been taken....

"Time to shoot the engineer." That's a phrase that has been around for a long time. Almost as soon as I got out of school and into industry, I began to hear people explaining that the need for perfection was all very fine, but it *must* not go on much further. When is the circuit going to be *good enough*? Perfection isn't necessarily justifiable. What is *good enough*? And whose opinion is to be relied on? Sometimes the engineer is correct that there are some improvements that *have* to be made. Other times, it's not so clear.

For example, we were recently trying to release a new product, but the distribution of one parameter was not quite centered. The yields might occasionally fall off more than we liked. So we proposed an optional metal mask that would bring the distribution back close to center. But this might cause some problems at high temperatures. And it might cause some dynamic problems. And even if it didn't cause serious problems, it might get some of our customers cross if they had to re-qualify our product, because we had made a change in a mask, even though it would be a *very tiny* change.

What's the right thing to do? Accept the yield loss? Change the data sheet? Delay the release of the product and risk the loss of market share? If we wanted to compromise, where would we do it? Hey, I don't know how you run your business, but in our business, there aren't any easy questions. If you're making alligator shoes, and your QC department says you can ship only shoes that have no visible flaws under a magnification of 5X, you're not going to be selling a lot of shoes. But, most of the time, our shoes are on our feet, at least 3 or 4 feet away from our eyes or anybody else's eyes. From that vantage point, "imperfection" is quite different.

Now, I'm not proposing that we refuse to ship amplifiers because they're not "perfect." I mean, if a perfect amplifier is one that has less than 0.5 mV of offset voltage, we have a *lot* of perfect amplifiers. Just 10 years ago, customers were pretty happy to buy that kind of "perfect amplifier." But these days, even 15 μV isn't "perfect." And if you build lots of amplifiers with less than 10 μV, and they all test out good, and then you allow them to warm up, and you temperature cycle them through an oven, are they still "perfect"—better than 15 μV? If you want to buy a "perfect" amplifier, do you require big safety factors against every possible condition? You may wind up going barefoot: The price for a "perfect" pair of shoes might be more than you would be willing to pay. Sometimes we have considered that amplifiers at this level of precision might have a looser AQL than normal—perhaps 0.5% instead of the typical 0.01%. But our QC people don't want to concede that.

If we test an amplifier for noise, and we do it 30 times, the data might show low noise on 27 of the passes. But on 2 or 3, there might be a small deviation—an increase (or a decrease) in the test result—whether or not the *amplifier* actually made more noise. Heck, you can't design a noise test to be perfectly repeatable—that's inherent in the nature of noise. Now, if a unit passes a test at its "class" or final test, it must never be allowed to fail its guaranteed specs if you re-test it. That means you must have wide guardbands, as wide as the deviations of the system's noise. If an amplifier that reads 1 μV pk-pk most of the time can read 0.8 μV some times, and 1.2 μV other times, that would tell you that you must have a guardband of *at least* 0.4 μV, and maybe 2 or 3 times that. So you could sell to a guaranteed spec of 2.2 μV—even though most of the parts are 1 μV pk-pk. Is that the spec you want to buy?

Once, a long time ago, a bright young engineer was working on semiconductors in England. The transistors were passing a 27-V breakdown test very reliably. But this semiconductor company was a subsidiary of a large plumbing-supplies company. And if you're making boilers or gauges or pipes, you've got to have a 3:1 ratio between the working pressure and the bursting pressure. So, this semiconductor company wrote their data sheets for a 9-V transistor, while their competitors were selling to a 25-V spec. Needless to say, the young engineer knew there was no future in a business where perfection and safety factors make the playing-field so badly tilted. And that was why Bill Frusztajer left England and came to the United States, where he became head of Teledyne Crystalonics.

All for now. / Comments invited! / RAP / Robert A. Pease / Engineer

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CAE Technology Report

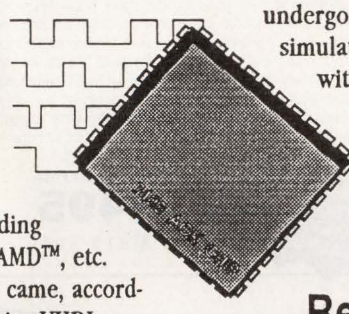
April 1991
Vol. 3, No. 4

Standard Universal Simulator

SUSIE is an acronym for Standard Universal Simulator for Improved Engineering, the world's only real-time simulator that allows concurrent design and test vector modifications while simulating. It took ALDEC only three years to promote SUSIE as a new logic simulation standard on PCs. Today, judging by the number of OEM vendors who have standardized on the SUSIE simulator, it clearly dominates the market. SUSIE is resold by CADAM/P-CAD™, Racal-Redac™, CAD Software™, Omation™, Phase Three Logic™, Accel™, and many other CAE vendors. To further increase SUSIE's international presence, ALDEC is working with four new European and two Japaneese CAE vendors who want to port SUSIE to their CAE environments.

VHDL Takes Over

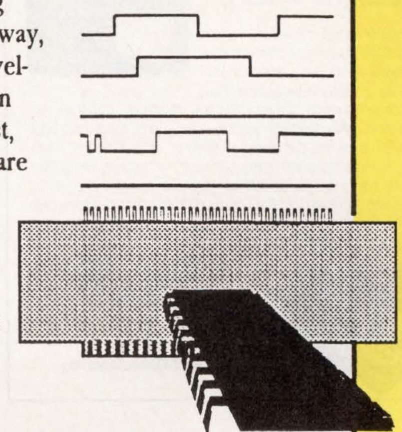
While many pundits still debate the merits of the VHDL standard, the leader in logic simulation on PCs, ALDEC Company (Newbury Park, CA) has already converted all its logic simulators to VHDL. According to Harry Tosado, Director of Sales at ALDEC, all IC models since March 1990 have been written in VHDL. The new SUSIE 6.0 simulator has exclusively VHDL IC models and supports most PLDs and FPGAs, including parts from Xilinx™, Altera™, Actel™, AMD™, etc. ALDEC's strong commitment to VHDL came, according to Mr. Tosado, as a result of superior VHDL model reliability and easy cloning of new parts by the user.



Easy Cloning of IC Models

Perceiving that IC modeling could be a major stumbling block to wider use of simulators, ALDEC has released ICMaker™ which allows for instant cloning of VHDL IC models. Since each of ALDEC's VHDL IC models is driven by a timing table that looks like an IC catalog sheet, the user can instantly create a new IC model just by changing timing data in this table. The method is so easy and simple that IC modeling with ICMaker has become a trivial task. The majority of CAE vendors have already standardized on ALDEC's SUSIE logic simulator because of its performance, ease of use, large IC libraries and superior IC modeling tools. **CIRCLE 101**

Simulators Replace Breadboarding



Simulators are replacing breadboarding in a big way, by cutting costs and development time to less than 20% in most cases. First, breadboarding in software takes only seconds but produces a perfect product. Second, the new simulators operate in real-time and behave like real hardware. The users can toggle switches, move jumpers, replace ICs, change JEDECs, etc., all within a fraction of a second. Some simulators such as SUSIE allow the user to move back in the simulation process, change design and test vectors and instantly analyze the effect of the latest changes. Also, IC modeling has undergone major improvements and the newest simulators allow for cloning of IC models within seconds. CAE tools are advancing at such a rate that they are catching up with the progress in silicon technologies. **CIRCLE 102**

Xilinx Leadership Reinforced

Good field programmable gate array (FPGA) architecture helps in getting user attention. However, since FPGAs are often used on small production runs, lowering development costs is a critical issue. Since Xilinx has worked closely with leading CAE vendors, its FPGAs have superior software support and designers can now test and modify multiple Xilinx FPGAs in real-time. For example, a designer can change a single cell in one FPGA and instantly see how this change affects another cell in a different FPGA. As design complexity grows, Xilinx leadership will be reinforced by the excellence of their support tools. **CIRCLE 105.**

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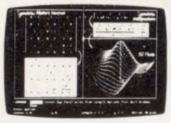

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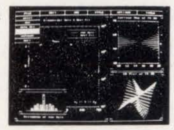

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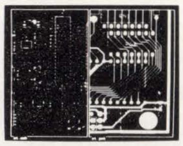

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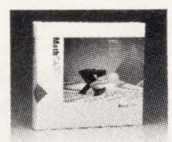

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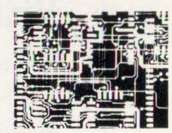

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CIRCLE 99

ED411

INDICATOR'S DESIGN GETS LIGHT FROM DEVICE BY INCORPORATING A PROCESS-PROOF LENS.

SURFACE-MOUNTED LED LIGHTS UP PC BOARDS

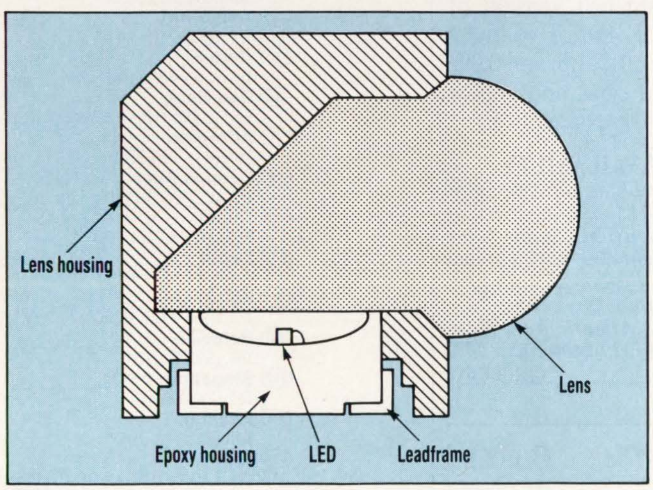
DAVID MALINIAK

A survey of today's electronic components would reveal that the industry's conversion of through-hole devices to surface-mounted-device (SMD) counterparts is nearly complete. An astute observer, however, would notice that some devices have lagged behind. Several components, like heavy transformers, are understandably difficult to translate into a part that's supported physically and electrically by a couple of solder fillets. But in other areas of componentry, such as optoelectronics, the difficulties are more subtle. Now these problems can be overcome with the first true SMD LED circuit-board indicator from Dialight Corp., a device that's process-friendly to boot.

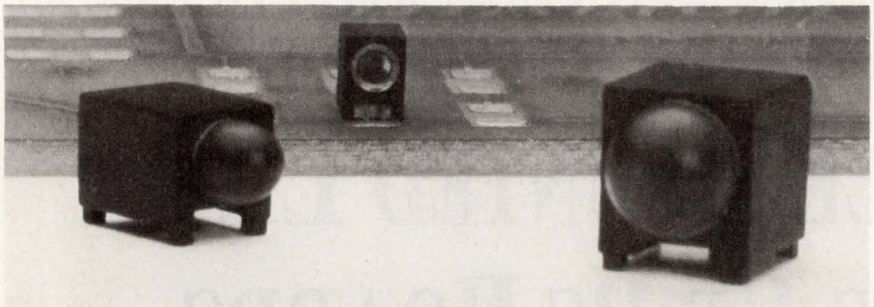
With a surface-mounted LED chip as its base operating element, Dialight's right-angle indicator resolves the problems of getting light out of the package. It does this by incorporating an optically pure lens that serves as a light pipe *(Fig. 1)*. The lens is transfer-molded from a clear epoxy that's specially formulated to withstand the 260°C temperatures of infrared soldering without deforming or discoloring. Initially, the device will be offered in AlGaAs red, and high-efficiency yellow and green colors, and in 1-, 3-, and 5-mm sizes. The three sizes correspond to T-3/4 (subminiature), T-1, and T-1-3/4 packages, respectively *(Fig. 2)*.

Contradictions between optoelectronics and the milieu of surface mounting made the component's development an interesting challenge. For one, the nature of optical elements (like lenses), where bigger is better, contradicts the usual SMD design goals of size reduction. To do its job efficiently and effectively, the lens element must have enough focal length to get light from the package into the viewer's domain. In addition, to obtain a usable viewing angle, the lens must have a rounded surface. That's at odds with the tape-fed automatic pick-and-place equipment used in device placement, which requires flat surfaces for device pickup.

In many cases, the first attempt at converting a through-hole component to an SMD device is to form the leads of the existing device. Almost three years ago, Dialight tried that with a standard-packaged LED and found that constructing a true SMD LED wasn't going to be so easy. The company also found that cus-



1. THE SMD INDICATOR **contains an LED with an integral leadframe molded within high-temperature epoxy. The LED's lens bends the light at a right angle for viewing.**



2. RED, GREEN, AND YELLOW versions of the indicator will be offered in three sizes: 1, 3, and 5 mm. These correspond to T-3/4 (subminiature), T-1, and T-1-3/4 packages, respectively.

tomer expectations in terms of reliability were much higher for an SMD device than for its through-hole equivalent because of the difficulties and expense of SMD rework.

From a reliability standpoint, Dialight helped itself by starting with an LED element that was developed specifically for surface mounting. The indicator chip, which is being supplied by both Siemens Components Inc., and Hewlett-Packard Co., Palo Alto, Calif., is a high-efficiency device that has a flat top and sides for easy handling. The component's base is made of a long-chain-polymer epoxy that withstands the extremely rapid thermal stresses of SMD processing. The epoxy, in fact, is of the same chemical composition as that of the Dialight-molded lens element. A leadframe is molded within the white housing, which has good light-reflecting properties. To accentuate the device's light output and focusing, the LED chip itself is situated within a well that serves as a reflecting bowl.

One of the biggest obstacles surmounted in the indicator's design was the lensing. Typically, LEDs are constructed by embedding a leadframe in a castable epoxy. At the high temperatures of solder reflow, castable epoxies tend to soften. As a result, the leadframe could move enough within the epoxy to break the wire bond from the chip to the leadframe, which means device failure. Attempts by manufacturers to use conventional lead-formed LEDs in SMD scenarios have resulted in unacceptable failure rates. Moreover, castable epoxies tend to discolor and/or lose their gloss when subjected to soldering.

The lens has a flat surface that picks up light from the LED chip resting beneath it on its leadframe. A prism-like formation in the lens then bends the light at a 90-degree angle to direct it toward the viewer.

The prime application for the indicator is on-board diagnostics. Another likely application is backlighting of front-panel legends.

Because the company is still in the process of characterizing early production versions of the indicator, there's no data sheet as of this writing. Luminous intensities for the LED itself range as high as 14 mcd typical for the AlGaAs red version, which has a dominant wavelength of 637 nm. The high-efficiency yellow and green types have luminous intensities of 5 and 8 mcd, respectively, as well as dominant wavelengths of 585 and 572 nm. Luminous intensities are likely to differ, however, when the bare LED is mated with the finished version of Dialight's lensing. Forward voltages at an I_F of 10 mA are 1.7, 1.9, and 2.0 V for the AlGaAs red type, and yellow and green versions, respectively.□

PRICE AND AVAILABILTY

Pricing for the SMD right-angle LED indicator will be below $.85 in quantities of 1000 pieces. Samples are available now, and production quantities will become available in June or July. Lead times for large lots will be eight weeks.

Dialight Corp., 1913 Atlantic Ave., Manasquan, NJ 08736; (908) 223-9400. Fax: (908) 223-8788. **CIRCLE 512**

HOW VALUABLE?	CIRCLE
HIGHLY	545
MODERATELY	546
SLIGHTLY	547

HARD DRIVE'S READ-CHANNEL ELECTRONICS FIT ON ONE CHIP

SMALL FORM-FACTOR DRIVES BENEFIT FROM ANALOG AND DIGITAL INTEGRATION.

RICHARD NASS

As hard-disk drives for PCs, laptops, and even workstations shrink, the need for control electronics to follow suit grows. In fact, a move is on to embed all of the electronics directly into the drive instead of using a separate controller board for space and power savings. The closeness of the electronics to the read/write head also reduces power consumption. In addition, this type of configuration minimizes the chip count, resulting in higher drive reliability.

To simplify the task of embedding the drive's electronics, National Semiconductor Corp. cut the number of chips needed to handle the read-channel functions to just one. The DP8491's complex analog and digital circuitry incorporates a pulse-servo detector, a data synchronizer, a frequency synthesizer, and write precompensation. Together, these functions process the disk's analog read signal into a coherent digital bit stream with an accompanying clock. From this signal, the recorded data can be retrieved with high integrity. Previously, each of the DP8491's four elements would be housed in a separate chip. In addition, the part is capable of 33-Mbit/s data rates. Because the device runs from a single 5-V supply, it should make an impact in battery-powered applications, such as notebook PCs.

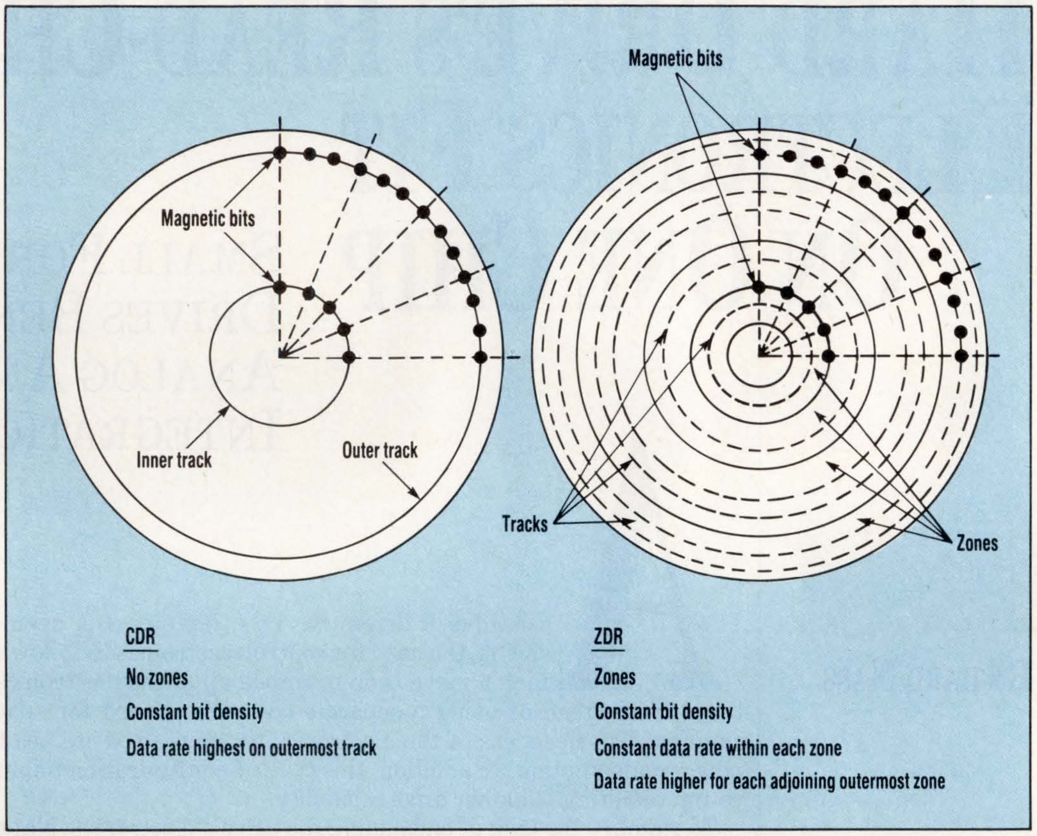
The DP8491 supports zoned data-recording (ZDR) techniques. The ZDR method increases the useful storage capacity of disk drives by dividing the disk into zones. Within each zone, the data rate is constant. This enables the disk's outer portions to be used more efficiently than conventional single-data-rate designs *(see the figure)*.

ZDR is a practical implementation of constant-density recording (CDR). CDR, currently employed by some drive manufacturers, increases data capacity by maintaining the same bit density (bits/in.) on every track, regardless of the track's radius. As a result, the data is rated highest on the innermost track and lowest on the outermost track. Because there are different radii on the disk, different data rates must be generated. ZDR, on the other hand, divides the disk into a number of zones, from 4 to 32. Each concentric zone consists of about 200 tracks, each with the same data rate. Consequently, the drive writes more data to the zones at the disk's outer edge. ZDR can increase effective storage capacity by as much as 50%. National claims they're the first manufacturer to ship a true ZDR design.

The disk drive manufacturers are given the freedom to choose and program the number of zones that will appear in the drives. Using more zones adds to the drive's capacity, but at the same time, it increases the complexity of the required hardware. By implementing just the minimal four zones, the increase in storage capacity is about 30% to 40%. Going up to the maximum of 32 zones increases that amount by about 10% to 20%.

The DP8491 comes with built-in power-reduction options, including partitioned power-down control modes and a separate power-down control pin for the pulse-detector servo circuits. The chip's partitioned-control options can be selected by programming the device's digital registers to optimize operation without the need for any external control circuitry. In other words, the major functional blocks of the chip can be powered down independently through dedicated power-control pins.

Operating modes and features of the DP8491 can be programmed by employing its on-chip control registers. The registers enable designers to configure the device to fit a specific drive. Features include changing the gain, determining which filters are used in the pulse detector, and varying the bandwidth. The chip is also responsible for adjusting the synthesizer frequency and determining whether a power-down mode is employed.



WITH ZONE-DATA RECORDING, National Semiconductor can increase the useful storage capacity of disk drives by up to 50% (right). ZDR, which is a refinement of constant-data recording (CDR), divides a disk into a number of zones, each with a constant data rate. However, the data rate increases with each outwardly radiating zone. CDR, on the other hand, has no zones, with the data rate highest at the outermost track (left).

Pulse Detection

The DP8491's pulse-detector section employs user-programmable equalization and has connections for two external filters to support multiple data rates for ZDR. The device also has an on-chip control register for selecting ZDR functions. Its on-chip frequency synthesizer generates all of the necessary clock signals for data encoding and synchronization. Full control of frequency selection is supplied by a programmable 10-bit word in the chip's control register.

A quadrature servo detector (four gated detectors) is used for accurate head positioning. In the drive's servo-burst area, there can be two or four bursts. The bursts are checked for their amplitude. These values are stored in a sample-and-hold buffer and then digitized. If it's determined that one burst is larger in magnitude than another, the drive is alerted that its head is out of alignment. A message is sent to the correcting element to position the head properly. Then, the detector compares the next burst to the last one. If these are equal, the head is in the correct position. Otherwise, it will correct itself again.

The remaining electronics that are required to complete the drive include a write preamplifier, a disk controller, a microcontroller, a motor-spindle speed controller, buffer memory, and a voice-coil positioning driver. Each of these parts is packaged in one or more chips. A digital or analog ASIC may also be required that contains the logic to link all the chips that are most likely from different manufacturers.☐

Price And Availabilty

The DP8491 is available now in sample quantities. Production will start around May. The price is $35 each in quantities of 100. The chip is housed in an 80-pin plastic quad flat pack or a 68-pin plastic leaded chip carrier.

National Semiconductor Corp., 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052; (408) 721-5000.

CIRCLE 513

How Valuable?	Circle
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Moderately	549
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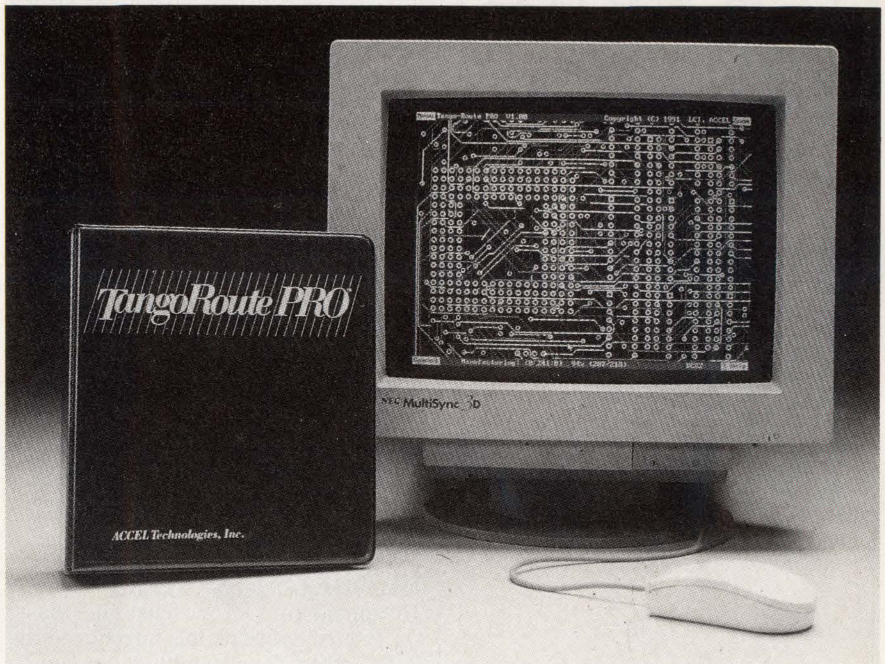
CIRCLE 134

PC-BASED ROUTER USES UNIQUE ALGORITHMS TO FINISH DENSE PC BOARDS

LISA MALINIAK



A reconstruct algorithm helps the Tango-Route Pro autorouter from Accel Technologies complete dense pc boards quickly. In addition, intelligent manufacturing-improvement algorithms increase yields, lower fabrication costs, and enhance the boards' aesthetics. User-selectable options mean the tool is flexible and easy to use.

The reconstruct algorithm is a remove-and-replace routing technique that reconstructs a network by removing and replacing nets in rapid iterations until 100% completion. The algorithm only removes connections that are in the way. The connections are then entirely reconstructed with new costing parameters. Local roadblocks are solved locally, while larger blocking connections are solved in a global manner. In addition, cleanup algorithms create board routes that are less expensive to manufacture. Consequently, the boards have fewer layers and vias, shorter total-trace lengths, improved electrical performance, and are aesthetically pleasing.

The router uses the 80386/80486 architecture for top speed and design-size capability. It supports virtual memory, which allows for routing completion without sufficient RAM.

Tango-Route Pro supports both uniform and non-uniform routing grids. Consequently, the designer has more freedom in placement. The software can handle packages of different pitches all on the same board. Moreover, it supports surface-mounted technology by routing to both top and bottom pads and performing smart-via fan-out. Fine-line routing aids in routing surface-mounted parts by allowing two or more tracks between pads.

Diagonal routing contributes to 100% completion of boards. It reduces the number of vias and connection inches, and produces more manufacturable results. Nets can have different routing-track widths assigned to them, which is useful for boards with routed lower and ground nets and for analog designs. T-routing, or copper sharing, aids completion rates, and reduces the amount of copper on the finished board design.

Boards can be routed with 1-mil resolution. The maximum board size is 32 in.^{2} with no more than 4000 components and 10,000 nets. Each board can have 15 layers: ten signal layers, one power and one ground plane, and three miscellaneous layers.

Users can perform a maximum of 29 routing passes. These passes are divided into constructive, rip-up and retry, and manufacturing-improvement phases. The manufacturing-improvement passes include the cleanup and spreading of tracks, removal of acute angles, and improved pad entry.

Tango-Route Pro is user-friendly software. The router runs under the company's Accel Productivity Interface (API). API is a Windows-like, menu-driven interface. A number of intelligent defaults make it easy for the novice designer to set up a route.

Other Tango-Route Pro features include user-definable design rules on an individual-layer basis, and simultaneous routing on all enable layers, not just on layered pairs. The software generates crash-recovery files, which spare users from lost routes and costly rerouting time. And with Tango-Route Pro, users can stop and restart anytime during the routing session.

A report generated at the end of each routing session describes results. The progress is displayed on the screen, detailing input and output file names, strategy settings, and after-pass routing results.

Tango-Route Pro, which must be used with the Tango-PCB or Tango-PCB Plus layout tools, comes with a reference manual featuring tutorial, reference, commands, error messages, glossary, and index sections. It requires a 80386-based PC with a 80387 coprocessor or a 80486-based PC, 4 Mbytes of RAM, and DOS Version 3.3 or later. The software costs $5500 and is available from stock.

Accel Technologies Inc., 6825 Flanders Dr., San Diego, CA 92121; (619) 554-1000. **CIRCLE 360**

CAE TOOLS RUN ON ANY X-WINDOW PLATFORM

The CapFast front-end EDA tools now run under the X-Window system, making them platform-independent. Called CapFast-X, the package contains a schematic editor, an on-line electrical rules checker, an interactive simulation grapher, parts libraries, an intelligent packager, and a symbol-creation editor. It also has interfaces to Spice, Hilo, Susie, Actel, and Xilinx tools, as well as to many of the popular pc-board tools. Schematic- and symbol-translator options based on the EDIF 2 0 0 standard are available for a nominal fee. In addition, the company will develop typical net listers at no charge if customers furnish the format of the target net-list interface. CapFast-X is shipping now for $995.

Phase Three Logic Inc., 1600 N.W. 1[illegible] Pl., Beaverton, OR 97006; (503) 6[illegible]-0313. **CIRCLE 361**

LOW-COST EMULATOR HANDLES 10K GATES

To appeal to a broad customer base, Quickturn Systems has introduced the RPM 10K, a low-cost 10k-gate version of its hardware-emulation system. Priced under $70,000, the RPM 10K has the same basic emulation functionality as the company's RPM 25K and RPM 50K models. The new system features in-circuit emulation with up to 272 I/O signal lines, up to 276 component-adapter pins for connecting existing ICs to the emulation logic, and a 160-channel logic analyzer and stimulus generator. The RPM 10K is available now for a base price of $69,000.

Quickturn Systems Inc., 325 E. Middlefield Rd., Mountain View, CA 94043; (415) 967-3300. **CIRCLE 362**

EDA TOOL SUITE SERVES MICROWAVE ENGINEERS

Version 3.0 of EEsof's design software for microwave and high-frequency analog circuits links upgraded versions of all of the company's microwave and RF simulators under one hierarchical design environment. Every circuit and system simulator can be operated from a common graphical interface called Academy, which furnishes schematic entry, multisimulator control, documentation, and optional IC and board layout. Running under the Academy software are upgraded versions of EEsof's Touchstone, Libra, OmniSys, and Microwave Spice simulators. Also included are enhanced versions of the EMSim electromagnetic planar simulator, and E-Syn and LineCalc support programs. Version 3.0 programs cost between $12,000 and $26,000, depending on the system, configuration, and options. All of the products run on HP/Apollo, IBM, and Sun workstations, and PCs running OS/2.

EEsof Inc., 5601 Lindero Canyon Rd., Westlake Village, CA 91362; (818) 991-7530. **CIRCLE 363**

FRAMEWORK SUPPORTS NETWORK LICENSING

Users of the Integrator CAE framework now have the option of network licensing. The Integrator is a tool that meshes CAE tools and other software packages into a heterogeneous networked environment. With network licensing, users are no longer locked into specific machines. Instead, a certain number of licenses are issued for any network access. Network licensing can drastically reduce costs because it eliminates paying for licenses on machines that are used less than 100% of the time. Single-network user prices for the User Station and the Integration Station are $10,000 and $30,000, respectively. The User Station includes the user interface, automatic tool sequencing, data-management facilities, and the Tool Encapsulation Library. The Integration Station also has the Tool Encapsulator. Discounts for multiple licenses are available.

InterAct Corp., 417 Fifth Ave., New York, NY 10016; (212) 696-3700. **CIRCLE 364**

SIMULATION LIBRARY NOW HAS AMD MACH MODELS

Behavioral software models are now available from Logic Automation for the AMD Mach family of programmable-logic devices. The models will feature Logic Automation's SmartModel Windows. With Windows, designers can look inside the registers of a device during simulation, set breakpoints, single-step through instructions, and change register values. And because all of this is done in software during simulation, problems can be identified and corrected prior to prototype development. SmartModels for the AMD Mach family run on many EDA systems and workstations. The entire SmartModel library, including the Mach family, can be licensed through Logic Automation's annual subscription service for $8900 per workstation.

Logic Automation Inc., 19500 N.W. Gibbs Dr., Beaverton, OR 97075; (503) 690-6920. **CIRCLE 365**

INTERFACE ICS TIE INTO WIDE BUSES

The Multibyte family of biCMOS bus-interface chips, which can directly drive 64-mA loads on 16-bit-wide buses, have near zero-static power consumption and input-to-output signal propagation delays of just 4.6 ns. The bus-interface chips come in 52-lead quad-sided flat packages that require only 174 mm^2 of board area—about half that required by two 8-bit chips. The first members of the family include the MB2244 16-bit line driver and the MB2245 16-bit transceiver. Also being sampled are the MB2543 latched transceiver and the MB2646 registered transceiver. These circuits are 16-bit biCMOS upgrades to the 8-bit 74xx244, 245, 543, and 546 functions. A total of 20 bus-interface chip types are slated for release through the rest of 1991. The MB2244 and 2245 go for $5.25 and $5.75, respectively, in 1000-unit lots.

Philips Components—Signetics Co., 811 E. Arques Ave., P.O. Box 3409, Sunnyvale, CA 94088-3409; (408) 991-2531. **CIRCLE 366**

PROGRAMMABLE-LOGIC CHIP PACKS 2500 GATES

Based on the previously released foldback NAND architecture of its programmable-logic family of macros, the PML2552 allows 100% connectability with no hand-routing of its internal logic paths. The CMOS chip packs about 2500 equivalent gates, permits a flip-flop toggle rate of 50 MHz, and has a typical internal NAND delay of 12 ns. The array's internal core has 96 NAND gates and 20 buried JK flip-flops that use a foldback architecture to make it possible for unrestricted interconnection among themselves. The chip has a total of 52 internal flip-flops and comes in either a 68-pin ceramic J-leaded windowed package, or a windowless 68-lead PLCC to trim cost.

In production quantities, the PML2552 programmable-logic chip sells for $20.00 each, while the Snap programming software sells for $795.

Signetics Co., Div. of North American Philips, 811 E. Arques Ave., P.O. Box 3409, Sunnyvale, CA 94088-3409; (408) 991-3266. **CIRCLE 367**

SERIAL I/O ICS EMPLOY NONVOLATILE CELLS

A family of serially programmable peripheral support chips, which include nonvolatile memory to hold their settings, offer a selection of functions handy for system trimming and configuration. The CMOS chips can be programmed over 1 million times.

For analog systems, the HC2003 provides a quad analog switch with each bidirectional switch controlled by a nonvolatile latch. The HC2004, an 8-channel data selector, contains eight programmable switches for data selection and summing operations.

A pair of trim potentiometers, the HC2010 and 2012, pack eight-stage R-2R ladder circuits with resistances of 1 and 100 kΩ, respectively. The wiper terminal setting is stored in a nonvolatile latch and has an output resolution of 0.4% of the voltage applied. The HC2021 offers an adjustable capacitance, containing eight binary-weighted capacitors that can be electronically switched to achieve capacitance values from 1 to 250 pF. Nonvolatile latches hold the value setting. A sine-cosine generator, called the HC2062, delivers output frequencies that are programmable subdivisions of an input clock frequency. Division ratios can range from 2^6 to 2^{16}, and the output amplitude is set by an external reference voltage so that it can be amplitude modulated.

Some digital functions are also available. The HC2063, a security-code generator-detector, can create and store a 16-bit code sequence and can be cascaded to form larger codes. Another chip, the HC2090, is a 16-bit divide-by-n counter. The counter has two modes: in the 16-bit mode, it divides the input frequency by a binary number from 1 to 2^{16}; in the 8-bit mode, it has two separately enabled sections that can each divide the clock by a number from 1 to 2^8. Also available is the HC2001, an 8-output solid-state DIP switch that can replace mechanical switches.

Chip prices are expected to range from $1.50 to $3.00 each, depending on quantity. Samples are available now.

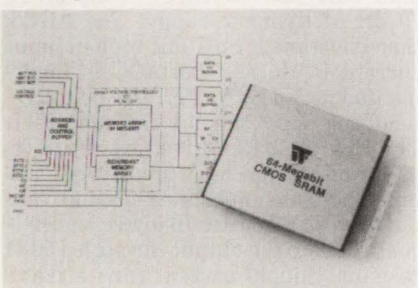
Hughes Semiconductor Products Center, P.O. Box H, Newport Beach, CA 92658; (714) 759-2665. **CIRCLE 368**

■ *DAVE BURSKY*

MEMORY MODULE LETS USERS ARRANGE 64 MBITS

A hybrid memory module packing 64 Mbits of low-power static RAM enables users to configure the memory in a variety of organizations: as either 8 Mwords by 8 bits, 4 Mwords by 16 bits, or as 2 Mwords by 32 bits. The system-level architecture of the WS-XM x X module is uncommitted until selected pins on the 3-by-3.5-by-0.32-in. flat package are connected to ground by the user.

Composed of 64 128-k-by-8-bit memo-



ry chips plus additional circuits and redundant memory chips, the 120-lead hermetic module keeps power low by adapting to its selected word organization. When placed in the byte-wide mode, only one RAM chip is activated at one time; in the 16-bit mode, two chips are active; and in the 32-bit mode, four chips are simultaneously active.

The selectable word organizations allow a variety of system architectures. With the proper bus-sharing system and user-developed hardware, one system could talk to the module with 8-bit buses, while another might communicate with 16- or 32-bit buses. Internal redundancy helps ensure operability even if some cells should fail. When a bit failure is identified, the entire sector containing the bit is ignored and the memory is rerouted and reformed with additional sectors, which are transparently mapped into the linear address space.

Special control circuits make it possible for the module to also operate in any of four modes—active, standby, data retention, and completely off. This allows the user to optimize system performance.

The module has an overall access time of 150 ns (including buffers and decoding logic), and typically consumes about 600 mW power when being accessed at 5 MHz. At 25°C, data-retention current is typically less than 1 mA. During standby, the module draws less then 15 mA. When switched to the Off mode, the device's current drops to less than 0.5 mA.

The module operates over the full military operating-temperature range of −55 to +125°C or the industrial operating-temperature range of −40 to +85°C. Prototypes are available. In small quantities, the 64-Mbit module sells for about $8000.

***White Technology Inc.**, 4246 E. Wood St., Phoenix, AZ 85040; Dan Tarantine, (602) 437-1520.*

CIRCLE 369

■ *DAVE BURSKY*

AMP'S ±320 V AT ±45 A DRIVES INDUCTIVE LOADS

By doubling its output to ±320 V, Copley Controls Corp.'s model 262 wideband pulse-width-modulation power amplifier overcomes coil inductance, improves rise time, repetition rate, and frequency response when energizing high-inductance, low-resistance loads. The amplifier develops ±45 A at ±320 V continuous (14 kW), and ±320 V at ±125 A peak (40 kW). Output current settles to within 0.1% of final value in 1.3 ms.

Up to 20 amplifiers may be paralleled for ±900 A continuous or ±2500 A peak. The amplifier has built-in power filtering, operates to 95% efficiency from a separate unregulated dc supply, and is protected against excessive temperature, short circuits, overload, and overvoltage.

The amplifier's switching frequency is 81 kHz. Such fast switching yields dc-to-5-kHz full-power bandwidth and 22-kHz small-signal response. The internal filtering removes harmonics of the 81-kHz switching frequency from the output, which enables the model 262 amplifier to look like a linear power amplifier. Total harmonic distortion is less than 0.2%.

The amplifier, which weighs 33 lbs., is designed to drive loads that contain a high ratio of inductance to resistance. Applications include MRI gradient-coil excitation, particle-beam steering, electron-beam scanning systems, and high-voltage dc motors. Pricing is $8900 in lots of one to nine with delivery in six to eight weeks after receipt of order.

***Copley Controls Corp.**, 375 Elliot St., Newton, MA 02164; (617) 965-2410.* CIRCLE 370

■ *DAVID MALINIAK*

TRANSIMPEDANCE-AMP IC HANDLES 150 MHZ

Designed to convert the high-speed current outputs of PIN diodes to voltages in applications ranging from 266 Mbyte/s glass-fiber data channels to Sonet or FDDI receivers, Anadigics' ATA01500 GaAs IC has a 3-dB bandwidth of 150 MHz. Its optical sensitivity at 220 Mbytes/s is a maximum of –35 dBm. With no load on the output and a dc input current of 300-nA (or less), transresistance is typically 14 kΩ. On-chip AGC, which starts to work at an input current of 30 μA, gives the device 70 dB of dynamic range. The AGC's time constant for a 1-mA step in input current is 10 ms. The AGC is implemented with a GaAs FET in a negative-feedback loop around the amplifier. The FET's gate is driven by the average value of the chip's unbuffered output. The transimpedance circuit's output drives an emitter follower, which is connected to the output through a 50-Ω resistor. Supply current runs a maximum of 40 mA from a 5-V rail. In quantities of 1000, the ATA01500 goes for $22 each. Small quantities are available from stock.

Anadigics Inc., 35 Technology Dr., Warren, NJ 07060; (201) 668-5000. CIRCLE 371

DIP HOLDS 4 OP AMPS PLUS A REFERENCE

The TDC4614 from TRW is designed to create up to four precision low-impedance voltage sources. This 16-pin DIP contains four independent, 324-type op amps plus an adjustable output (1.2 to 6.3 V) bandgap reference. Its cohort, the TDC4611, contains just one op amp and a reference in an 8- or 14-pin DIP. Many flash analog-to-digital converters offer improved linearity if one or more taps on their resistive divider are each driven by a precision voltage, a natural application for the TDC4614. Many additional flash and other types of ADCs require a positive and a negative reference. Alternatively, the IC can provide any mix of four positive or negative reference voltages for any mix of DACs or ADCs or for trimming op-amp offset voltages. In commercial and military grades, pricing for the DIP starts at $1.20 each for the commercial TDC4611 and $1.75 each for the TDC4614, both in quantities of 100. Small quantities of the TDC4614 16-pin DIP are available from stock.

TRW LSI Products Inc., P.O. Box 2472, La Jolla, CA 92038; Dan Watson (619) 457-1000. CIRCLE 372

EASY-TO-USE PULSE GENERATOR FEATURES MODULAR FLEXIBILITY

To ensure maximum flexibility, the Model 9210 GPIB-programmable pulse generator accepts up to two plug-in output modules with varying combinations of repetition rates, edge-transition times, and output swings. Resolution and accuracy are excellent. Maximum time resolution is 10 ps with a time-base accuracy of $\pm(0.5\% + 0.2\text{ ns})$. Amplitude resolution is 5 mV with a dc accuracy of 1%.

The Model 9211 output module has a maximum repetition rate of 250 MHz, edge times from 1 ns to 1 ms, and a 5-V pk-pk output into 50 Ω. The Model 9212 features a maximum repetition rate of 300 MHz, edge times from 300 ps to 1 ns, and a 5-V pk-pk output. The Model 9213 offers a large 16-V pk-pk output with a maximum repetition rate of 100 MHz and edge rates from 6.5 to 95 ms. The two high-speed modules have complementary outputs and can deliver preset TTL or ECL levels.

A number of special features make the units easy to use. Operators can set and change parameters using soft keys and menus on a touch-screen CRT. Or they can use a numeric keypad and rotary knob. In addition to help screens, the CRT alerts users to conflicts in parameter settings. At power-up, the generator calibrates itself using a built-in frequency counter and 12-bit analog-to-digital converter. The unit also features temperature compensation and automatic load-compensation.

The Model 9210 mainframe is $5900. The 9211, 9212, and 9213 modules cost $1600, $2200, and $1000, respectively. Delivery is in 4 to 6 weeks.

LeCroy Corp., Signal Sources Div., *700 Chestnut Ridge Rd., Chestnut Ridge, NY 10977-6499; (914) 578-6020.* **CIRCLE 397**

■ *JOHN NOVELLINO*

ICON-BASED TOOL BUILDS REAL-TIME PROGRAMS

The DEC RT Integrator lets OEMs and end-users build test and measurement and other real-time applications for manufacturing and quality-control operations. The DEC RT Integrator is a graphical programming language that creates analysis and test applications without the need to write programs. Library icons are placed on a DECwindows "work surface" and then connected with data-flow lines and set up using pop-up menus. Users can check, debug, and run applications with mouse clicks. The DEC RT Integrator runs on Digital's Unix-based RISC workstations and VMS-based VAX workstations. A development kit costs $2700. A run-time license is $600.

Digital Equipment Corp., 4 Results Way, MRO4-2/C17, Marlboro, MA 01752; (508) 467-4591. **CIRCLE 398**

DIAGNOSTIC SYSTEM ADDS AC AND RF ANALYSIS

Release 2.0 of the Electra Troubleshooting System contains several enhancements. Electra, which performs component-level diagnostics on analog and mixed-signal circuits, now can detect subtle ac faults, such as a wrong capacitor value in an active filter. The system also supports RF-voltmeter measurements and models defined in dB values, and can make passive measurements on suspect components to refine and confirm a diagnosis. The new release gives users added ability to create, edit, and modify custom block and component models. The system includes a rack-mountable chassis that houses a Sun board set, disk drive, IEEE-488 card, Ethernet card, and custom hardware. Prices start at $75,000. Delivery is in 8 to 10 weeks.

Applied Diagnostics Inc., 121 Industry Ave., Pittsburgh, PA 15275; (412) 787-3002. **CIRCLE 376**

16-BIT EMULATOR ADDS LARGE EMULATION RAM

The MIME-700 in-circuit emulator now has a 256-kbyte emulation RAM with an optional 2-Mbyte memory. First versions of the 16-bit emulator support the Motorola 68000 and 68010 microprocessors, but the instrument will be expanded to 32-bit emulation in the future, with personality cards for other devices. The MIME-700 is host-independent. Tracing can be started and stopped on any combination of events, and users can define a highly selective capture of trace information. Trace memory is 128 bits by 8 ksamples. The MIME-700 costs $14,000.

Pentica Systems Inc., 1 Kendall Sq., Bldg. 200, Cambridge, MA 02139; (617) 577-1101. **CIRCLE 374**

SCOPE MODULE IMPROVES LOGIC ANALYZER

The HP 16532A 1-Gsample/s digitizing oscilloscope module helps users of the HP 16500A logic-analysis system troubleshoot and test all CMOS and many ECL-based designs. The module offers a 250-MHz single-shot bandwidth with 8-bit vertical resolution. A sophisticated sampling technique allows time-interval accuracy of better than $\pm$150 ps. Up to 18 channels can be connected into one HP 16500A system. Operators can set up time-correlated measurements and mixed displays using the new module and the analyzer's 1-GHz timing and 100-MHz state modules. All modules can cross-trigger each other. The HP 16532A costs $9000 and the HP 16500A mainframe goes for $7000. Delivery is estimated at 8 weeks.

Hewlett-Packard Co., Colorado Springs Div., P.O. Box 2197, Colorado Springs, CO 80901-2197; (800) 752-0900. **CIRCLE 375**

8-CHANNEL SIGNAL ANALYZER IS PORTABLE

Designed for portable and laboratory use, the SD-390 dynamic signal analyzer offers dc to 105-kHz signal processing in a 2- to 8-channel instrument. An intuitive operating system based on Microsoft Windows 3.0 and a built-in trackball make the unit easy to use. With the trackball, operators can perform complex mathematical functions on live-signal inputs or stored data. Setups and test data can be stored on the 1.44-Mbyte floppy disk drive or on the 20-Mbyte hard drive. The SD-390 uses a high-contrast, 16-gray-scale, gas-plasma display with 640-by-480-line resolution. The unit can also drive an external color monitor. Prices start at under $17,000 for 2 channels.

Scientific Atlanta Inc., Spectral Dynamics Div., 13112 Evening Creek Dr. S., San Diego, CA 92128-4199; (619) 679-6000. **CIRCLE 377**

SYSTEM EVALUATES ICS' RESISTANCE TO ESD

The Model 1600 measures a semiconductor's ability to withstand accidental electrostatic discharges found in manufacturing, handling, packaging, and assembly environments. The tester generates charged-device model pulses that duplicate the discharge which occurs when ICs become charged to a high potential with static electricity, then rapidly discharge. The tester produces a waveform with less than 80-ps rise time and less than 300-ps in length. Charge voltage is programmable from $\pm$20 to $\pm$5000 V with 5-V resolution. Prices range from $30,000 for a semiautomatic system to $120,000 for a fully automatic system with waveform verification and a Tektronix SCD-5000 3.5-GHz transient digitizer. Delivery is in 10 to 12 weeks.

TriSys Inc., 15242 Greenbrier Pkwy., Beaverton, OR 97006; (503) 645-5504. **CIRCLE 378**

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CIRCLE 4

Avis features GM cars. Pontiac Grand Prix.

MAINTAIN AND REENGINEER EXISTING C PROGRAMS

Targeted at comprehension, maintenance, and reengineering of existing C-language software programs, the Smartsystem from Procase Corp. runs on Sun, DEC, IBM, and MIPS workstations. Version 1.7 of the Smartsystem enables programmers to view and address software at a system level with various abstractions, including graphical and filtered views.

The tool is structured around an object-oriented database that stores the program source, any modifications that are made, and all derived data. This common representation of the program lets users understand both the overall structure and detailed components of the source code, without using new methodologies or changing the existing programming environment.

The Smartsystem consists of five modules that either work together or independently to meet different needs. They are Smartview, a text-based comprehension facility that includes filtering, navigation, formatting, and editing; Smartcheck, a sophisticated analysis tool for incremental syntax and semantics checking; Smartgraph, a tool that presents a graphical view of a program's structure; Smartstore, a C++ object-oriented database that's used by the other modules; and Smartmake, an incremental symbolic-debugging tool for run- and compile-time analysis.

Smartsystem also helps in continually maintaining and updating new software. It's built around a reconfigurable user interface that can be tailored to suit existing environments or personal programming preferences. The modules are sold individually for $1750 or together for $8750. All five tools are available now.

***Procase Corp.**, 3130 De La Cruz Blvd., Suite 100, Santa Clara, CA 95054; (408) 727-0714.* **CIRCLE 379**

■ *RICHARD NASS*

ADA COMPILER TARGETED FOR SPARC PROCESSORS

Targeted toward Sun Microsystems' 32-bit Sparc microprocessor, the VADScross Ada cross-development system lets designers develop Ada applications on a Sparc-based workstation. Its common host-target environment significantly reduces the time spent testing and debugging. VADScross supplies real-time support for host-to-target system development. The development environment features an Ada cross compiler, improved code execution, a powerful window-oriented source-level debugger, and access to Ada source code during a debugging session. Users can access a target debug monitor that downloads executable code to the target through a serial or Ethernet connection. Contact the company for price and availability information.

Verdix Corp., Sullyfield Business Park, 14130-A Sullyfield Circle, Chantilly, VA 22021; (703) 378-7600. **CIRCLE 380**

REAL-TIME OS ADDS ENHANCEMENTS, X-WINDOW SUPPORT

Version 2.4 of Microware Systems' OS-9 real-time operating system includes a new symbolic debugger, noncontiguous boot files, and variable-sector-size random-block disk files. Version 2.4 runs on 680X0-based systems.

At the same time, Microware is offering an X-Windows version of OS-9, called OS-9/X Windows. It's a complete X-Windows client implementation and is available for resident OS-9-, Unix-, and DOS-based development environments. OS-9/X Windows client support includes the X-Windows development libraries, run-time client programs, sample source client programs, and a window manager. The run-time client programs enable programmers to perform system-level functions, such as opening terminal-emulation windows and initializing and starting up X-Windows.

OS-9/X Windows is compatible with a wide variety of networked X-Windows servers. Embedded server support will initially include Vigra's MMI-250 display board, which offers 1280-by-1024-pixel resolution with 256 displayable colors from a palette of 16.7 million.

X-Window applications can easily be ported between OS-9/X Windows and Unix because the new operating system is processor and operating-system independent. Also, the development toolset simplifies the design and development of graphics-based applications, resulting in applications that are easy to maintain and enhance.

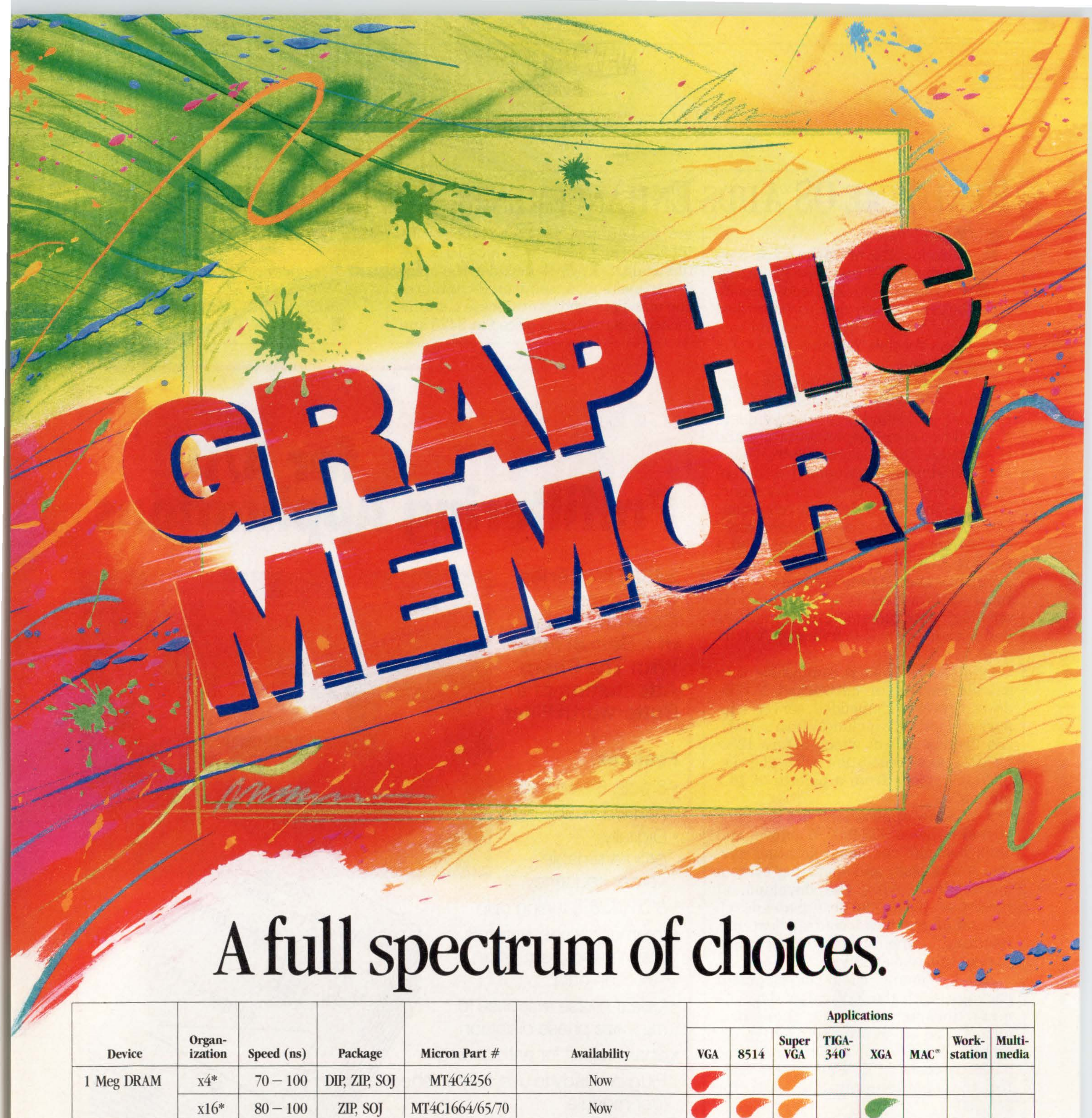
An X-Window client development package, with the X-Window development libraries, run-time client programs, and client-program source examples is priced at $995. A run-time package costs $195. Full source code for the operating system sells for $15,000.

Version 2.4 of OS-9 includes enhanced communications capabilities that support the 68332 communications controller. It also adds SCSI support, including the Common Command Set, connect-disconnect, and device installation. Other features include the ability to install bootstrap files on magnetic tape, 13 new utilities and shell commands, and a C-language ROM boot code that simplifies boot operations for multiple devices.

OS-9 Version 2.4 is available now in two versions. Professional OS-9, which includes the operating system, compiler, screen editor, debugger, file managers, and utilities, sells for $1150 for 32-bit CPUs and $800 for 16-bit CPUs. Industrial OS-9, which includes the operating system, a sequential-character file manager, and interprocess communication manager, is priced at $425 and $275 for 32- and 16-bit CPUs, respectively.

Microware Systems Corp., 1900 N.W. 114th St., Des Moines, IA 50322; (515) 224-1929. CIRCLE 381

■ *RICHARD NASS*



A full spectrum of choices.

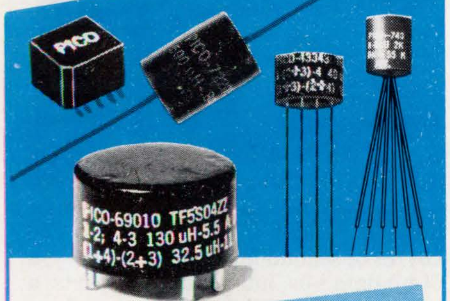
Device	Organ-ization	Speed (ns)	Package	Micron Part #	Availability	Applications: VGA	8514	Super VGA	TIGA-340™	XGA	MAC®	Work-station	Multi-media
1 Meg DRAM	x4*	70 – 100	DIP, ZIP, SOJ	MT4C4256	Now	●		●					
	x16*	80 – 100	ZIP, SOJ	MT4C1664/65/70	Now	●	●	●		●			
4 Meg DRAM	x16*	60 – 100	SOJ, TSOP	MT4C16256/7	Samp. Q4 '91; Prod. 1H '92		●	●		●			
256K VRAM	x4	100 – 120	DIP, ZIP	MT42C4064	Now	●	●	●	●		●	●	
1 Meg VRAM	x4	80 – 120	ZIP, SOJ	MT42C4255/6	4255 Now; 4256 Q4 '91		●	●	●	●	●	●	●
	x8	80 – 120	ZIP, SOJ	MT42C8127/8	8127 Now; 8128 Q4 '91		●	●	●	●	●	●	●
2 Meg VRAM	x8	70 – 100	SOJ	MT42C8256	Samp. Q4 '91; Prod. 1H '92			●	●	●	●	●	●
1 Meg Triple-Port DRAM	x4	80 – 120	SOJ	MT43C4257/8	Now							●	●
	x8	80 – 120	PLCC	MT43C8128/9	Now							●	●

*Also in low power versions.

MICRON
TECHNOLOGY, INC.

2805 E. Columbia Rd., Boise, ID 83706 (208) 368-3800

CIRCLE 95



IMPROVED SERVERS HIKE THROUGHPUT, TRIM COST

Two enhanced top-performing, low-end servers are designed for departmental networks that need balanced integer and floating-point support. The CMOS RC3360 is the highest-performance system yet released by MIPS, employing a 33-MHz R3000 CPU. The ECL RC6260 is a compact single-CPU server with the industry's fastest speed. The 3360 has a SPECmark rating of 26.4, while the 6260 has a rating of 44 using the R6000 ECL RISC processor. Prices for the RC3360 start at $65,000, which includes 32 Mbytes of RAM (expandable to 256 Mbytes), 663 Mbytes of disk (expandable to 20 Gbytes), and room for four Ethernet links and seven VME I/O slots. The base ECL system starts at $139,500 and comes with 32 Mbytes of RAM (expandable to 128 Mbytes) and 663 Mbytes of mass storage (expandable to 44 Gbytes). Both systems are available from stock.

MIPS Computer Systems Inc., 928 Arques Ave., Sunnyvale, CA 94086-3650; (408) 991-7777. **CIRCLE 382**

BURST CACHE UPS 386-SYSTEM'S SPEED

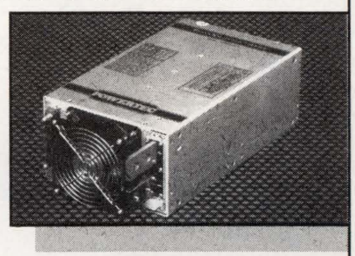
By adding a 256-kbyte burst-mode cache to an 80386-based 33-MHz system, that system can deliver the top performance possible for a 33-MHz system. Employing a burst-mode algorithm similar to that incorporated into Intel's 80486, the Topline 386/33 Burst system can set the cache as a two-way or direct-mapped memory, thanks to the use of the Austek 38202, a write-through cache controller. The burst mode is implemented by the Austek 38204 memory controller. Using version 2.00 of the Landmark rating software, the CPU achieves a speed rating of 54.5X and a power-meter (version 1.5E) of over 8 MIPS. Up to 64 Mbytes of RAM can be held on the motherboard. The Tiger chip set from Texas Instruments is used on the motherboard, allowing the company to remap the memory between 640k and 1 Mbyte to the top of main memory and three noncacheable memory regions. The tower cabinet holds four half-height and one full-height drive. The base model includes a 200-Mbyte ESDI drive with 32-kbyte cache, an advanced VGA adapter, and a multisynch monitor. The base system starts at $4295.

Topline Technologies Inc., 310 Orangethorpe Ave., Bldg. J, Placentia, CA 92670; Patsee Ober, (714) 524-3784. **CIRCLE 383**

DESKTOP SERVER DELIVERS 25 MIPS

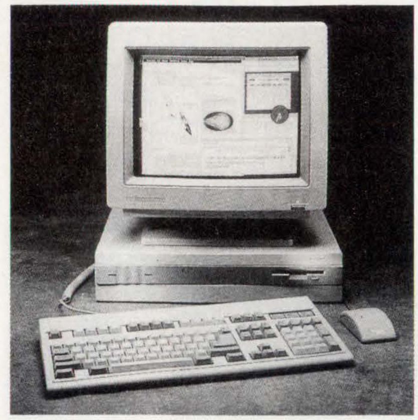
A dual-processor system—the NEWS 3870 RISC-based workstation—can also be used as a departmental server. The main system's CPU is based on the Mips R3000 RISC processor with 64 kbytes each of data and instruction cache, and a companion R3010 floating-point unit. That combination delivers 25 MIPS and 4.3 MFLOPS (double-precision). The system's second processor, a Motorola 68030, serves as an intelligent I/O processor. That enables the RISC processor to put its full attention to the user's tasks. The base system is configured with a 1.25-Gbyte hard disk, a 1.44-Mbyte floppy, a streaming-tape unit, and 64 Mbytes of main memory (expandable to 128 Mbytes). Serial, parallel, Ethernet, and dual SCSI interfaces are built in. A system with an optional 19-in. color monitor and an 8-plane 1280-by-1024-pixel graphics card goes for about $40,000.

Sony Microsystems Co., 645 River Oaks Pkwy., San Jose, CA 95134; (408) 434-6644. **CIRCLE 384**



RUN UNIX AND DOS ON SAME 486-BASED PLATFORM

Based on the Intel i486 microprocessor, the Voyager platform from Tyan Computer Corp. runs both DOS and Unix. It combines the high performance of Unix with the broad application base of DOS. The computer runs applications under either operating system concurrently, without sacrificing any speed or computing power. The Voyager's single-board architecture takes full advantage of the 33-MHz 486 processor's capabilities in a pizza-box-shaped chassis.



The system features 8 Mbytes of RAM expandable to 64 Mbytes, 256 kbytes of second-level cache memory, a 64-bit data bus, integrated I/O ports, a built-in Ethernet interface, and an 8514/A-compatible graphics adapter. Internal 3.5-in. hard-disk capacities range from 210 to 500 Mbytes.

The Voyager comes preinstalled with standard software. This includes Unix System V Release 4, X11 Window System Release 4, Motif and Open Look graphical user interfaces, and networking software. Also included is a 16-in. color monitor with noninterlaced 1024-by-768-pixel resolution and 256 colors. The base configuration is priced at $9999. The Voyager will begin shipping in the second quarter.

***Tyan Computer Corp.**, 612 N. Mary Ave., Sunnyvale, CA 94086; (408) 720-1200* **CIRCLE 385**

■ *RICHARD NASS*

MEASURE CONVERGENCE BETWEEN CRT COLORS

One quick and easy way to check display convergence on a color monitor is by using the Klein Convergence Gauge. The handheld gauge works on the principle of optical reconvergence of an image, where the required amount of reconvergence is a measure of the convergence error that's present. The gauge, used with a video-pattern generator, obtains measurements that are critical for precise engineering, manufacturing, calibration verification, quality assurance, and incoming inspection. Various models of the gauge are available for differing resolution displays.

Klein Optical Instruments, 8948 S.W. Barbur Blvd., Dept. 100, Portland, OR 97219; (503) 245-1012. **CIRCLE 386**

RISC-BASED LAPTOP PUTS POWER IN MOTION

Taking a cue from the adage that says good things come in small packages, Sony Microsystems did not sacrifice any major performance feature when putting an R3000-based RISC workstation in a laptop, transportable format. The NEWS 3250 laptop computer delivers workstation-level performance, 17 MIPS and 1.8 MFLOPS (when running at 20 MHz) in an 18-lb., 13.750-by-16.375-by-3.875-in. package that lets designers take their work with them when they travel. (However, power consumption for the RISC system is not low enough to permit batteries to handle the power required for the hardware and the backlit high-resolution LCD display.)

The base system consists of a full-function Unix System V.4 workstation with X-window version 11R4 and Motif. The 1120-by-780-pixel monochrome backlit LCD display provides plenty of work area. An embedded 240-Mbyte SCSI-compatible hard disk (406 Mbytes, optional) gives users enough storage to carry most of their workspace environment with them.

Several different built-in I/O ports are included: serial, parallel, SCSI, Ethernet, audio, and mouse, as well as one proprietary expansion slot. The standard base system also comes with a 1.44-Mbyte floppy disk drive, 8 Mbytes of random-access memory (expandable to 36 Mbytes of RAM), dual 32-kbyte caches, and a three-button mouse in its base configuration.

The base system sells for $9900. For a unit with the higher-capacity hard-disk drive, the price is $11,900.

Sony Microsystems Co., 645 River Oaks Pkwy, San Jose, CA 95134; (408) 434-6644 CIRCLE 387

■ *DAVE BURSKY*

CONNECT UP TO 96 USERS THROUGH ONE SLOT

Designed for ISA- and EISA-bus computers, the Megaplex-96 is a mainframe-class I/O subsystem that permits hundreds of terminal users to be efficiently connected to a Unix-based computer. The subsystem solves four problems associated with large multiuser systems: cost, performance, slot limitations, and cabling. Instead of connecting all 96 users to the host computer, the Megaplex-96 uses multiple 24-port cluster multiplexers. Each multiplexer connects up to 24 users to the host through a high-speed four-wire link. The multiplexers can be placed up to 2500 ft. from the host. The subsystem employs a custom RISC-type communications technology that implements serial I/O in hardware rather than software. An entry-level 24-port configuration is priced at $2395. Extra multiplexers are $1495.

Equinox Systems Inc., 14260 119 Ave. SW, Miami, FL 33186; (800) 328-2729 or (305) 255-3500. CIRCLE 388

ETHERNET OPTIONS TRIM MAC NETWORKING COST

Plug-in Ethernet local-area-network pc cards for Apple NuBus and LC Macintosh computers are designed to simplify and cut the cost of networking such computers together. One pc card is a NuBus intelligent card that offloads some operations from the host computer. It is being priced at $424 each. A simpler card, designed to work with the MAC LC computer, is priced at $199 each.

A thin-coaxial-cable self-terminating transceiver pc card terminates the network end without the need for a user-supplied terminator. This condition holds true even when using the Apple-supplied thin coaxial cable. Also included from Apple Computer are a twisted-pair-wire transceiver as well as an attachment-unit interface (AUI) to handle other types of local-area-network transmission media.

A local-area network built from such hardware eliminates the disruption caused by a user removing a computer from the network and leaving the coaxial cable disconnected. With Apple's cables, the network would be left neatly divided into two fully operational networks, making it easy to locate the fault.

The thin-coaxial-cable transceiver, the twisted-pair-wire transceiver, and the AUI adapter, are all priced at $175 apiece.

Apple Computer Corp., 20525 Mariani Ave., Cupertino, CA 95014; (408) 996-1010. **CIRCLE 389**

COMPRESSION BOARD DOUBLES STORAGE CAPACITY OF A MAC

Compatible with the Macintosh II family of computers, the DoubleUp lossless compression add-in board enables Mac users to double their mass-storage capacities. Sigma Designs boasts that the board works an average of eight times faster than software-based compression utilities. The board compresses all types of files by about 2:1. DoubleUp compresses all files, whether they contain images, nonimage data, or application programs. With lossless compression, no information is lost or changed, so decompressed files take exactly the same form they had prior to compression.

The compression technology is based on the Stac algorithm, which scans strings of digital information for recurring sequences of data. Once found, the recurring data is selected and replaced with tokens that represent compressed forms of the recurring data. As a result, files of virtually any size can be compressed and stored in far less space than they would typically occupy. During the decompression process, these tokens are then used to relocate the original data.

The Stac algorithm resides in a special processor from Stac Electronics, Carlsbad, Calif. The chip, a 40-MHz 9703, compresses and decompresses files at or above the speed taken by the Mac to access information from the hard disk. In many cases, disk speed is the limiting factor in storing and retrieving compressed files.

The DoubleUp board comes bundled with DiskDoubler 3.0, a compression software interface from Salient Software Inc., Palo Alto, Calif. With its consistent Macintosh finder interface, the software gives users the advantages of compression without interrupting the usual routine of working with Mac files. The DoubleUp board is available now for $299. A Macintosh SE version is expected later in the year.

Sigma Designs Inc., 46501 Landing Pkwy., Fremont, CA 94538; (415) 770-0100. **CIRCLE 390**

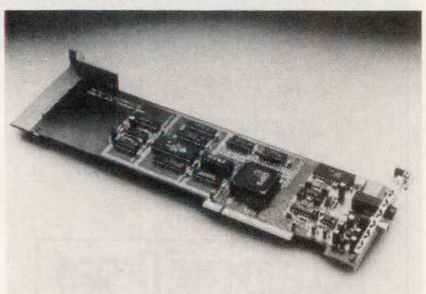
■ *RICHARD NASS*

SEE HIGH-RES AND VGA ON ONE MONITOR

By using the Video Seven SPEA 1280 graphics accelerator, users can display VGA and high-resolution graphics at the same frequency without any performance degradation. The VGA graphics can be displayed in a functional window or a full screen on a fixed frequency, high-resolution monitor. The board, designed for CAD applications, is based on TI's TMS34020 graphics processor. It supports resolutions up to 1280 by 1024 pixels with 16 or 256 colors. The 1280 minimizes flicker and eye strain by supporting refresh rates up to 84 Hz. The board shows no resynchronization delay when switching between high-resolution and VGA modes. It contains 2 Mbytes of VRAM for display memory and 1 Mbyte of DRAM for the display-list drivers. The 1280 supports Windows 3.0, Presentation Manager, and X-Windows. It's available immediately for $2999.

Headland Technology Inc., 46221 Landing Pkwy., Fremont, CA 94538; (415) 623-7857. **CIRCLE 393**

REPLAY DIGITAL AUDIO FROM MCA SYSTEM



Micro Channel users can now add direct-from-disk high-quality audio playback to their systems. The VP800 digital-audio board is useful for audio replay, where audio is created from a mastering workstation and replayed at standalone or remote locations. The board plugs directly into a PS/2 or other Micro Channel-compatible expansion slot. Sampling rates can be set at 6, 8, 10, 12, or 16 kHz. Menu-driven software is included for keyboard control of replay functions. Supported languages include C, Pascal, Assembly, and Quick Basic. With 10-bit resolution, dynamic range is rated at 60 dB with a signal-to-noise ratio of 55 dB at 16-kHz sampling rates. Frequency response is 200 to 7000 Hz at ±3 dB. The VP800 is available now for $325. Large-quantity discounts are available.

Antex Electronics Corp., 16100 South Figueroa St., Gardena, CA 90248; (213) 532-3092. **CIRCLE 391**

RUN MACINTOSH SOFTWARE ON A PC

IBM-compatible PCs are now able to run Macintosh software. The Hydra One also lets users continue to run the PC software, turning their systems into dual-environment computers. With this offering, users can tap into the large array of Macintosh applications. The product consists of a full-length add-on board, proprietary software, and a custom PC/Macintosh interface connector. The board's high performance comes from a combination of custom VLSI hardware, a 16-MHz 68000 processor, and streamlined software. A file-transfer program is also included. The installation procedure consists of simply plugging in the board and loading the software. RAM or ROM can be added separately. Hydra One is available now for $995.

Hydra Systems Inc., 20863 Stevens Creek Blvd., Suite 330, Cupertino, CA 95014; (408) 996-3880. **CIRCLE 392**

NEW PRODUCTS

COMPUTER BOARDS

68040 SINGLE-BOARD COMPUTER USES VME64

Incorporating VME64 optimized block-transfer techniques, the SV430 is a single-board computer that offers a data-transfer rate of 66 Mbytes/s. The board is designed around the 68040 microprocessor. Field-interchangeable DRAM modules enhance the board's performance by supporting one-wait-state memory reads and zero-wait-state writes. The modules have byte parity protection and support the 68040 burst-fill mode. Other features include an integrated SCSI controller, an Ethernet controller, and a real-time clock with battery-backed SRAM. The board is available now for $3985.

Synergy Microsystems, 179 Calle Magdalena, Encinitas, CA 92024; (619) 753-2191. CIRCLE 394

PARALLEL PROCESSOR CUTS IMAGING TIME

By using the EktronBoss parallel-processing system, imaging applications that once took hours can now be performed in seconds. The VME-based image processor is designed for such applications as visualization, simulation, and pattern recognition. With the fully programmable and scalable boards, the host-system's computational power increases to over 5000 MIPS and 700 MFLOPS. The EktronBoss consists of three boards: a controller interface, a data I/O interface, and a compute engine. The system is available now.

Ektron Applied Imaging, A Kodak Co., 23 Crosby Dr., Bedford, MA 01730; (617) 275-0475. CIRCLE 395

FLEXIBLE VMEBUS COMPUTER HOLDS 68040

The CPU-40 is a VMEbus-based single-board computer that's constructed with the Motorola 68040 microprocessor. The flexible board can be configured for various real-time and embedded applications. Its flexibility comes from the board's 32-bit interface that accepts plug-in daughterboards. Labeled Eagle modules, they let users run the CPU board and the I/O subsystem from the same VME slot. One Eagle module is currently available; others are expected throughout the year. Users can also design their own modules. The base price for the CPU-40 is $3990. With the I/O module and 4 Mbytes of DRAM, the board costs $5490.

Force Computers Inc., 3165 Winchester Blvd., Campbell, CA 95008; (408) 370-6300. CIRCLE 396

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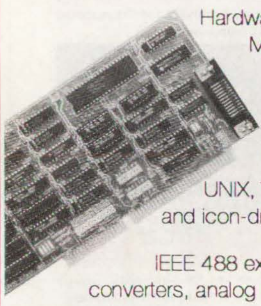

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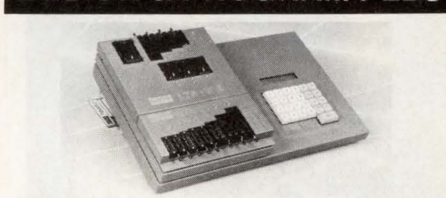

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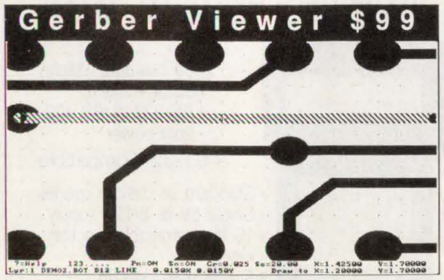

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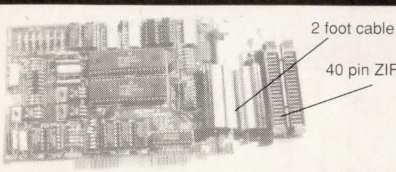

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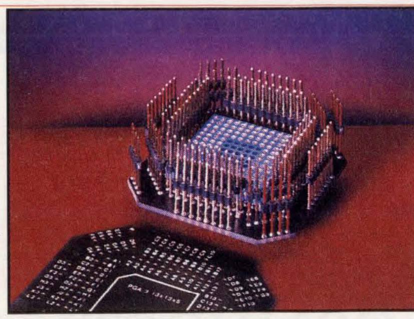

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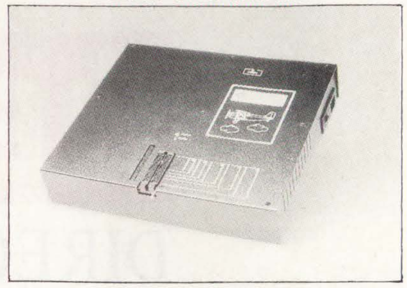

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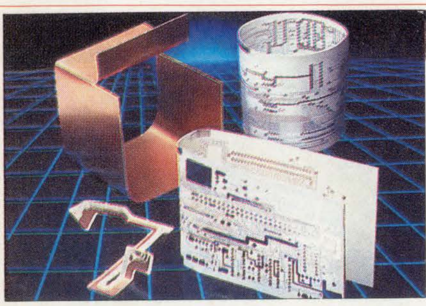

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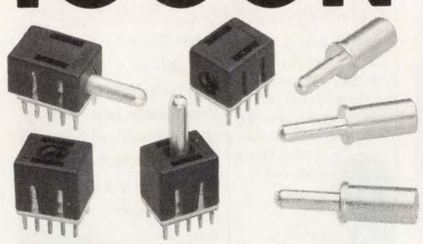

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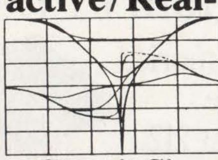

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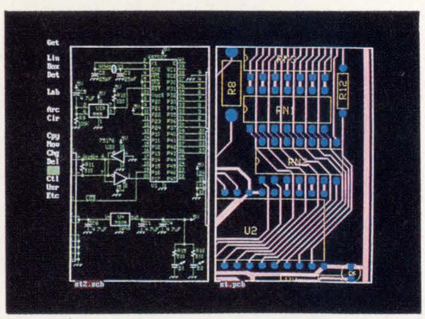

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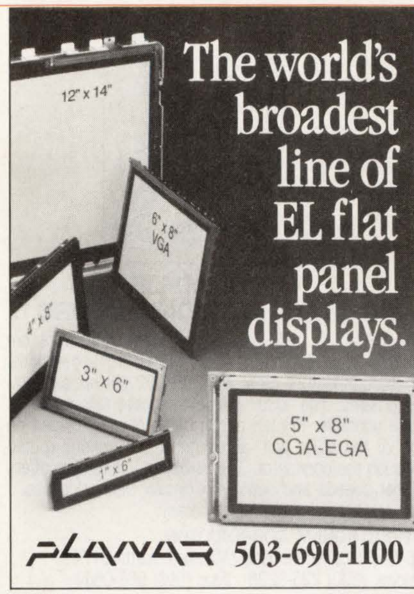

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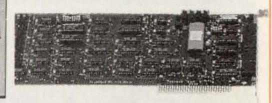

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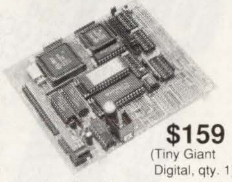

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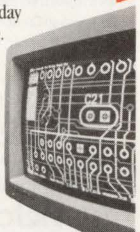

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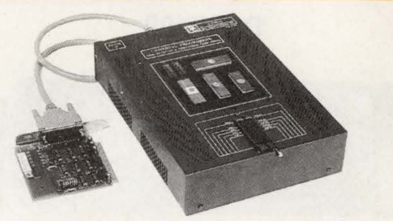

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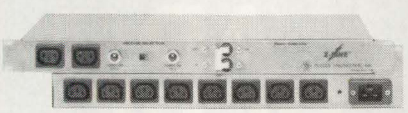

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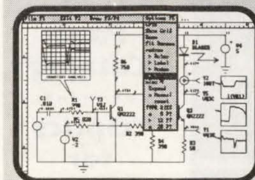

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