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90-132/180-264VAC, 47-63Hz,
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ELIMINATES UL/CSA/TUV
TESTING OF YOUR SYSTEM

AMP OUTPUT CONNECTOR

MODEL PAC 150-01
+5VDC @ 16A
+12VDC @ 5/8A
12VDC @ 3/4.5A, isolated
-12VDC @ 3A
-5VDC @ 0.5A

Power, approvals and cooling — Condor's new "PAC" Series enclosed switching power supplies have it all!

Want to save a lot of time on your next project? Just bolt a "PAC" Series power supply in place, plug into its mating amp connector and you're ready to go!

All "PAC" models feature fans for system cooling, and inside the system, they mount to an outside surface and include on/off switches, IEC 380 AC input plugs and air exhausts, all on that surface. Best of all, they automatically switch from 115 to 230VAC!

"PAC" Series features:

- 17 models, 4 power levels — 85 to 185 watts

- Multi-output — up to 5 outputs
- Fully protected— factory-set current limit, built-in OVP and reverse voltage protection
- Full load burn-in and 2-year warranty
- Powerfail signal at 150W and 185W levels
- High peak current disk drive outputs as well as closely regulated 3-terminal outputs
- Extremely versatile output configurations for tough applications
- Isolated outputs can be used for positive or negative sources or in series with other outputs
- Pass vibration and shock per MIL-STD 810D

The entire "PAC" Series is fully approved by CSA, UL, and TUV/VDE, and tested for compliance with VDE 0871 Level B and FCC Class B.

Why not try Condor's "PAC" Series power supplies for yourself? Call us today for a **free** 30-day evaluation unit!

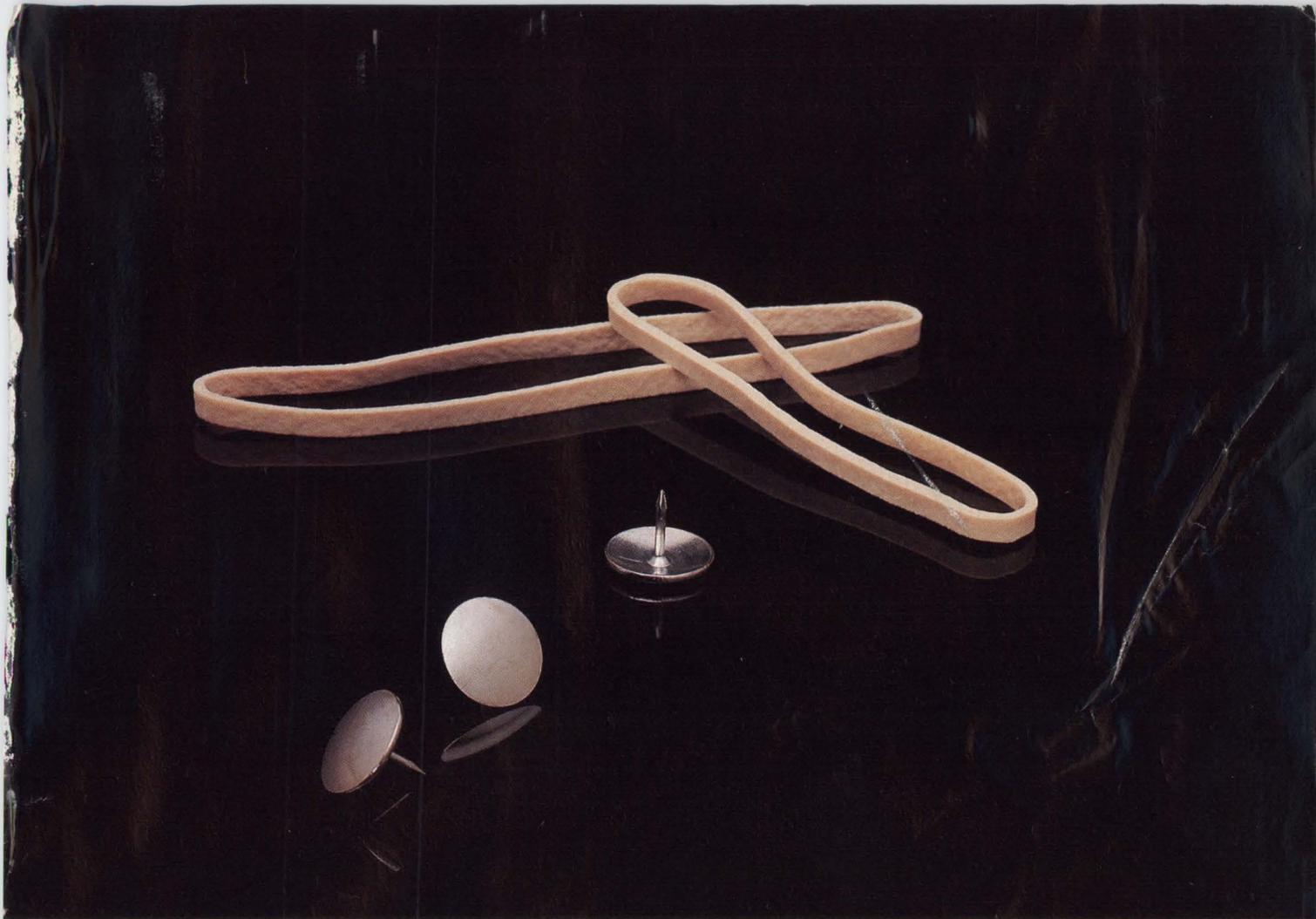
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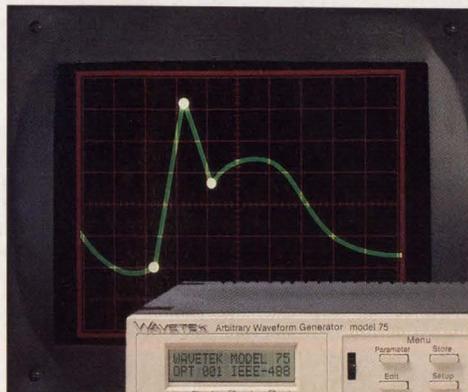


If you can use these simple tools, you can create any waveform.

The Model 75 Arbitrary Waveform/Function Generator lets you create and edit waveforms which it reproduces with digital precision. It's easy to do, because you use a thumbtack and rubberband editing system to stretch and shape the waveform on the x-y axis while you watch the results on your oscilloscope.

No other arbitrary generator lets you design waveforms from the front panel this way.

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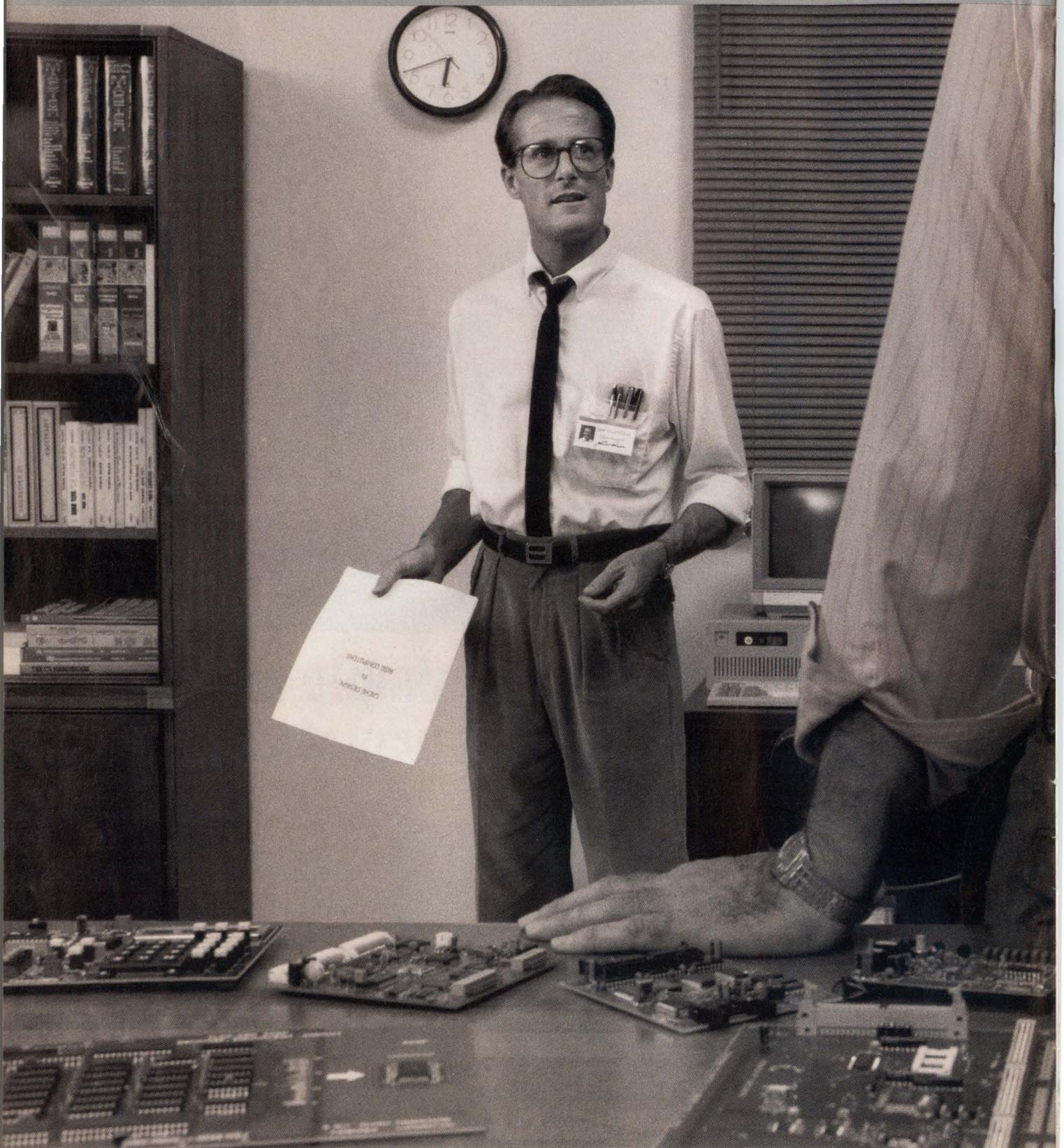


waveforms. Or use one of the nine built-in functions. The Model 75 memory provides a grid of 8,000 horizontal and 4,000 vertical points for reproducing signals with amazing purity.

You can see that Model 75 is the wave of the future. And at less than \$3,000, it's affordable now!

For literature or a hands-on demonstration of Model 75, call (619) 279-2200.

"What if I told you there's a 15ns 64K SRAM available"



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32K x 8	256K	20	25	35	Early '89	
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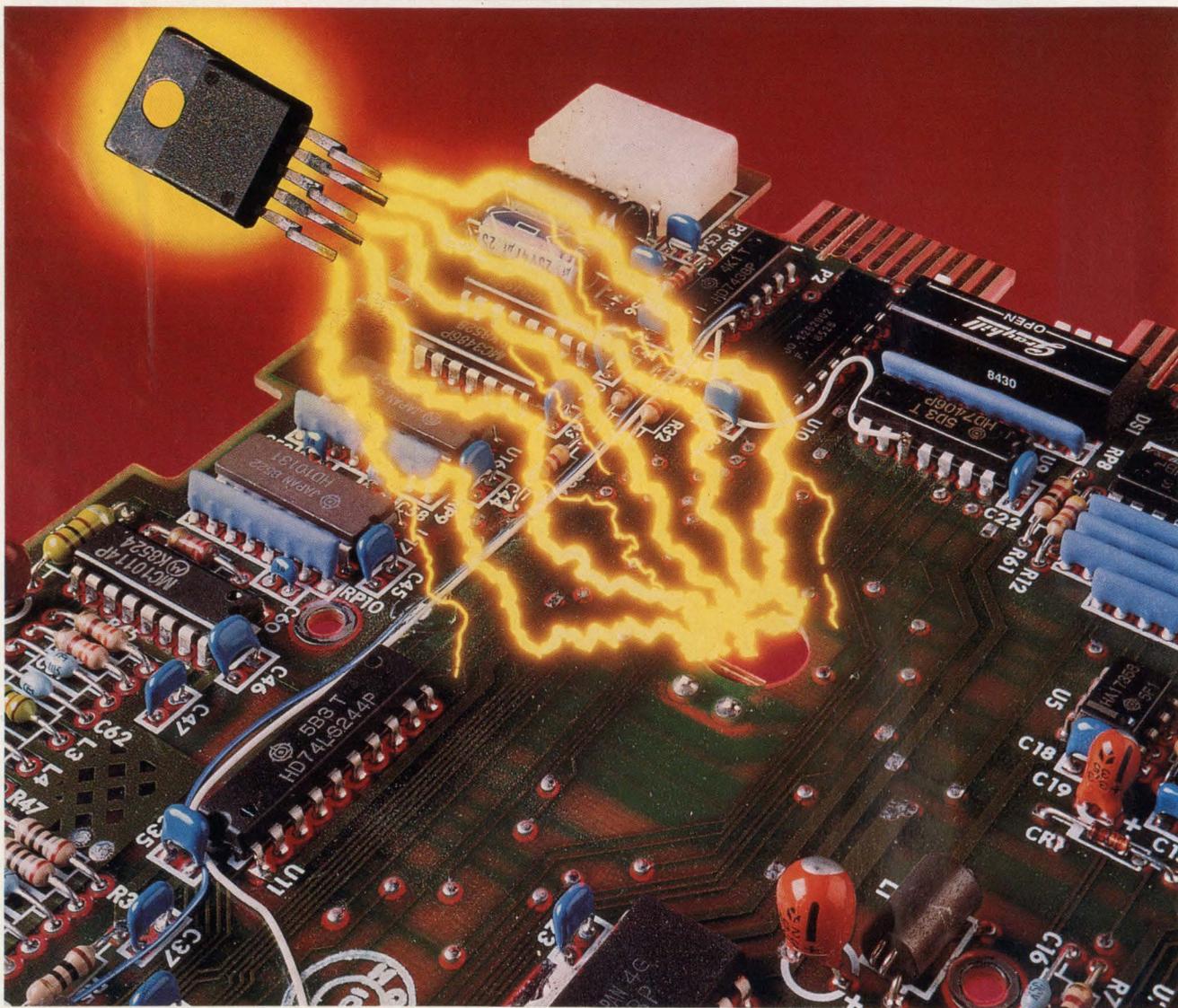
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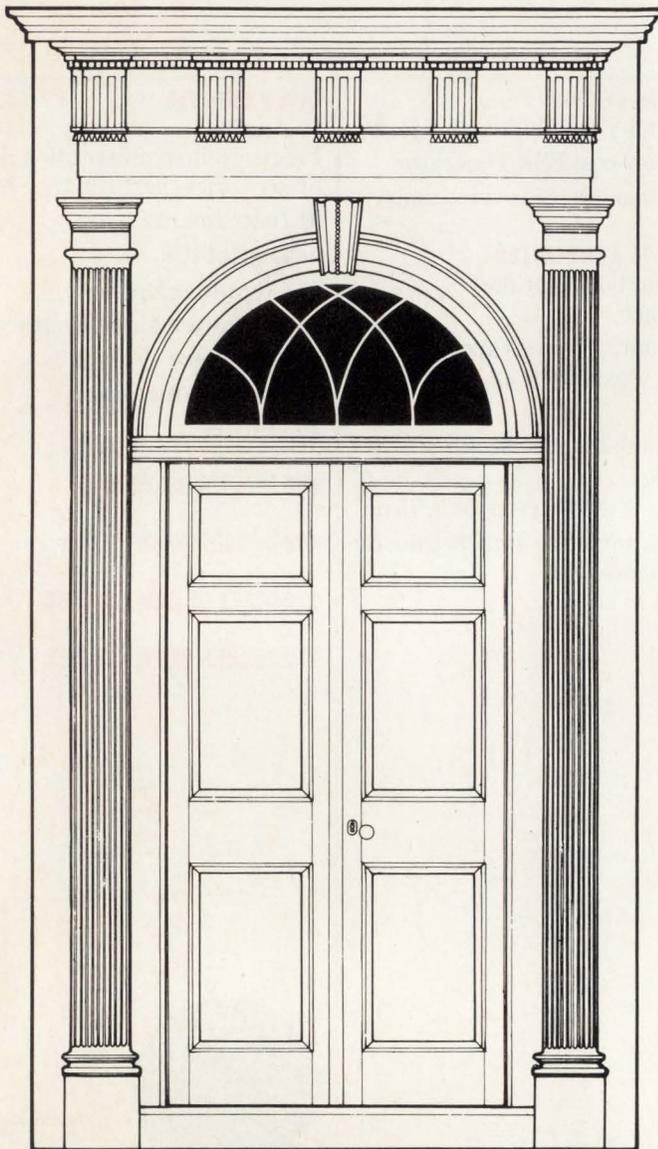


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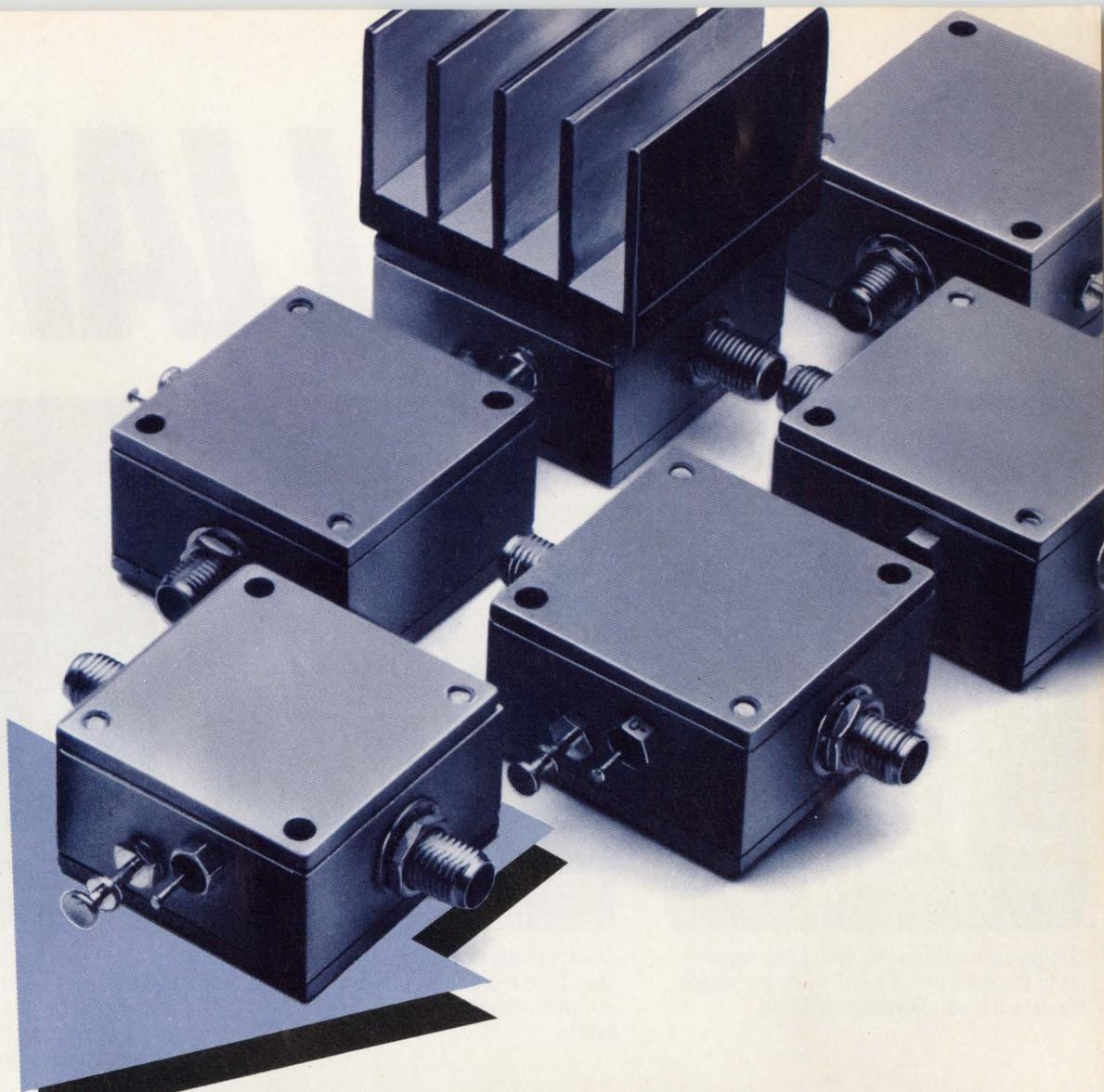
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ZFL-500LN	0.1-500	24	+5	2.9	79.95
ZFL-750	0.2-750	18	+9	6.0	74.95
ZFL-1000	0.1-1000	17	+9	6.0	79.95
ZFL-1000G*	10-1000	17	+3	12.0	199.00
ZFL-1000H	10-1000	28	+20	5.0	219.00
ZFL-500HLN	10-50	19	+16	3.8	99.95
ZFL-1000LN	0.1-1000	20	+3	2.9	89.95
ZFL-1000VH	10-1000	20	+25	4.5	229.00
ZFL-2000	10-2000	20	+17**	7.0	219.00

* 30dB gain control

**+15dBm below 1000MHz

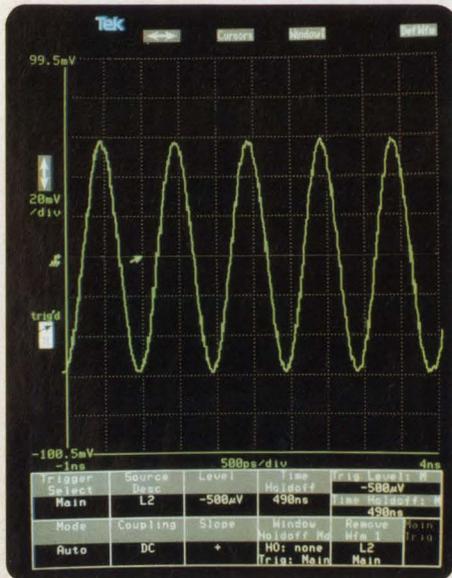
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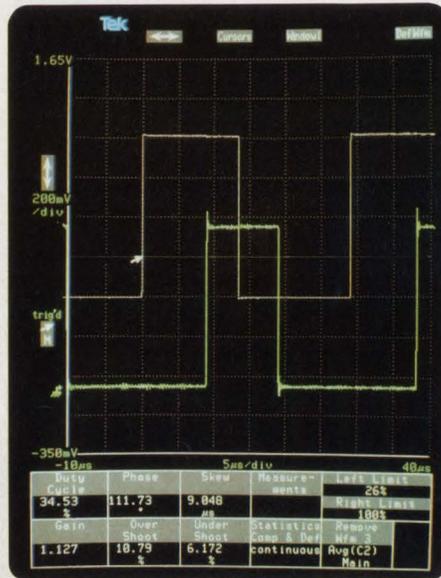
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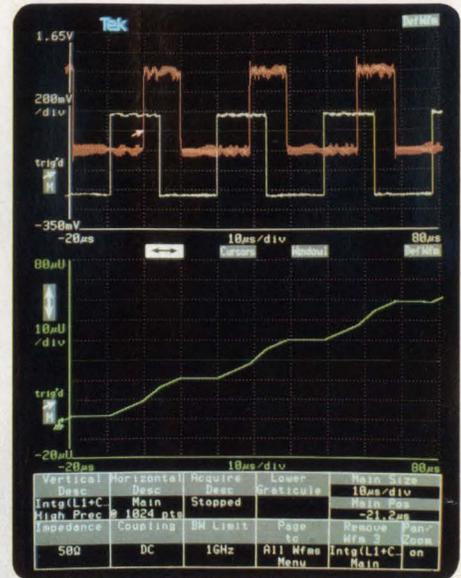
BRILLIANT



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24 automatic measurements let you use your time more efficiently by making fast, accurate, repeatable measurements at a touch.



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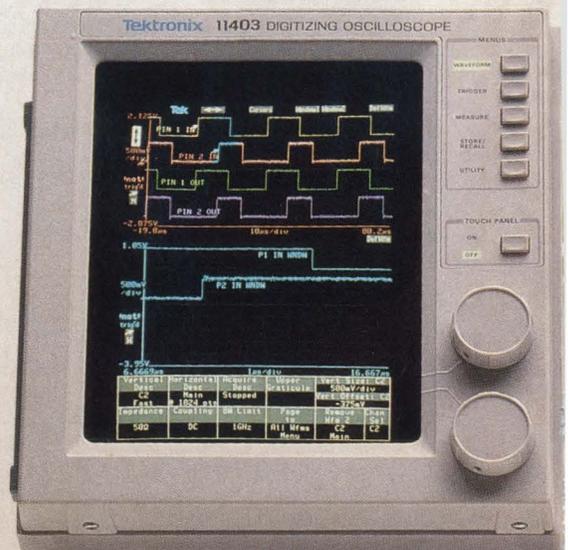
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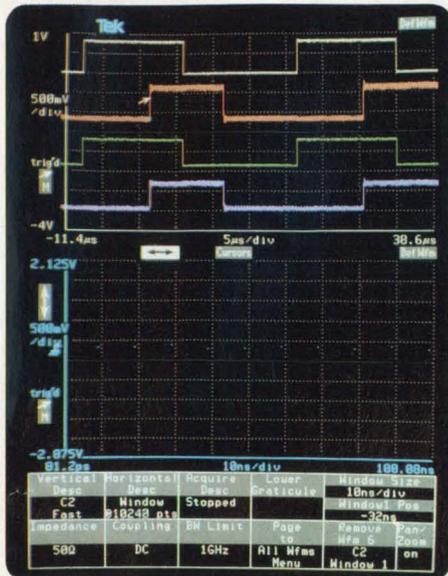
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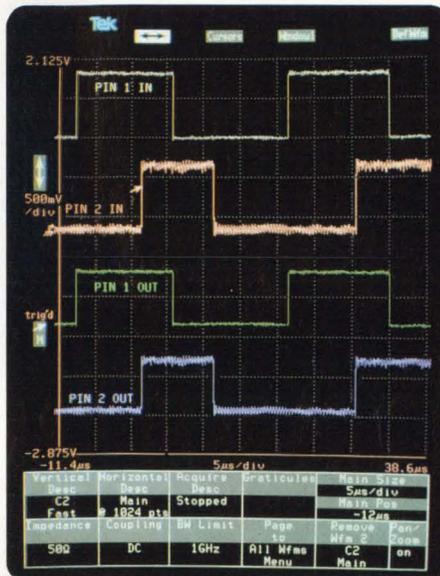
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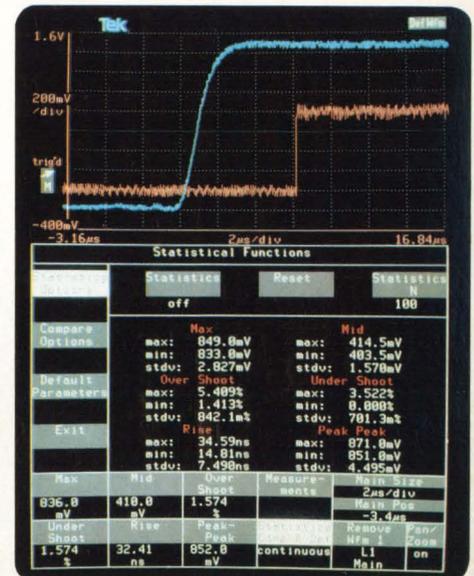
DEDUCTIONS



Examine fast signals in greater timing detail than ever before: the 11403 can window to 10 ps/div sweep rate in the zoom and pan mode.



Label waveforms with limitless versatility, to identify what each signal represents. Labels, plus automatic time and date stamps, are reproduced on all hard copy output.



Continuous statistics are automatically provided with each measurement, giving design and manufacturing a clearer picture of actual circuit performance as adjustments are made or as temperatures vary.

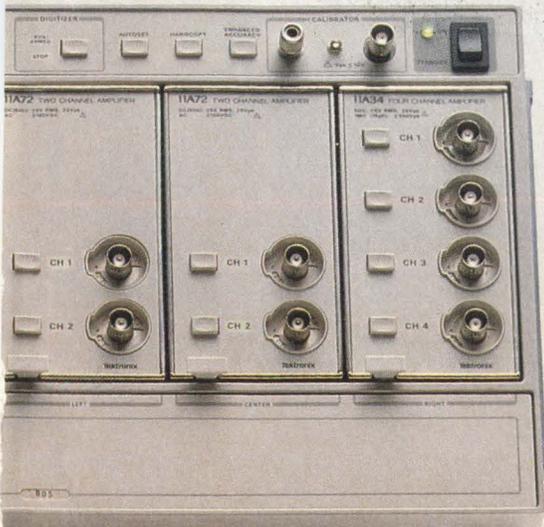
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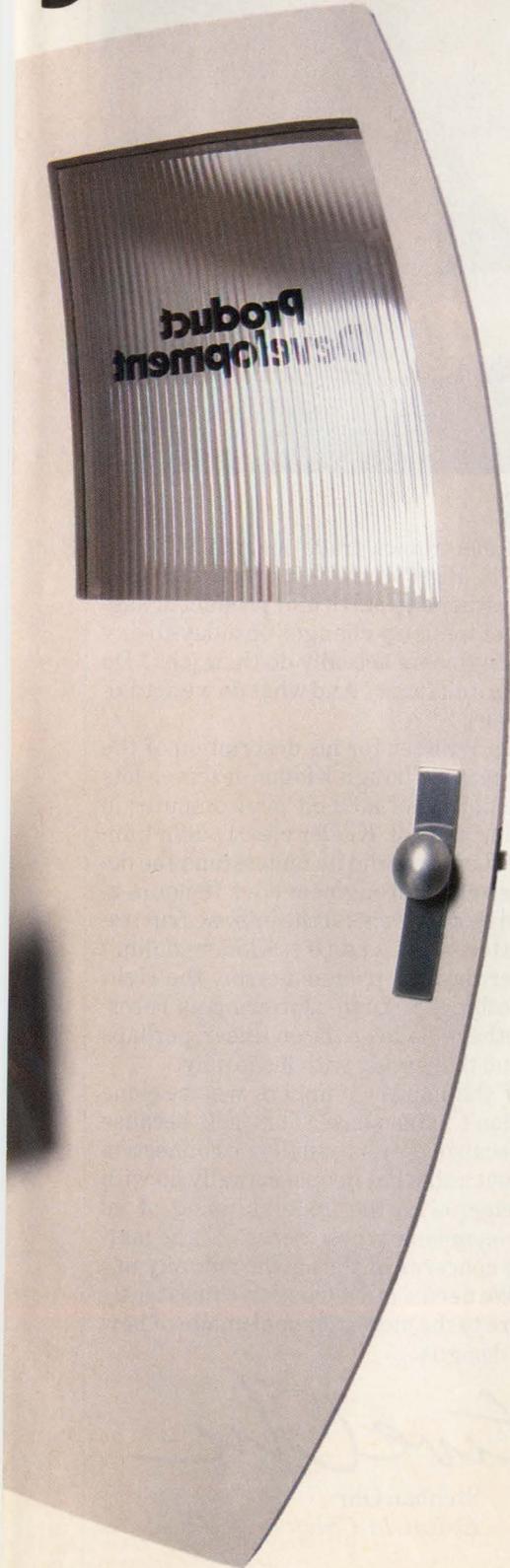
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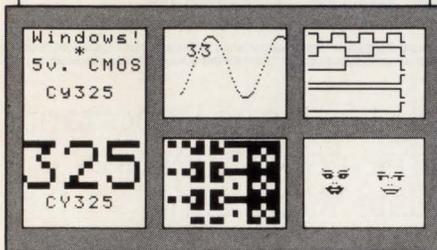
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What's Missing on this LCD?

(answers below)



If you peeked at the answers, then you know it's Motion. In the actual LCD every one of the windows is in motion. Think for a minute how you would make six or seven unique motions simultaneously with the low level LCD controllers that you have seen. No way! Now think what your instrument or new systems could do with dynamic text and graphics. Tests show that programmers can achieve animated presentations in only hours using the CY325.

The CY325 LCD Windows Controller Chip

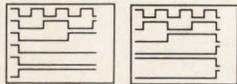


lets you: specify any of 250 built-in windows, or create your own with a single command; manage text and graphics with automatic cursor control; wrap or scroll text with window relative pixel plotting and clipping; read an A/D and write the waveform into the window; drive up to 6 I/O pins with logic waves, or use the 'soft-key' feature of the CY325 for menu management. Only \$75 each (\$20/1000)

Answer:

Motion is missing in each of the windows. Text actually scrolls up in the top left window above, and . . .

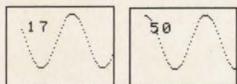
Logic waves flow right to left.



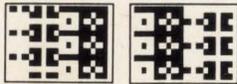
Boy and girl wink, smile, and flirt.



Counter counts and sine wave advances.



Pseudo random patterns change.



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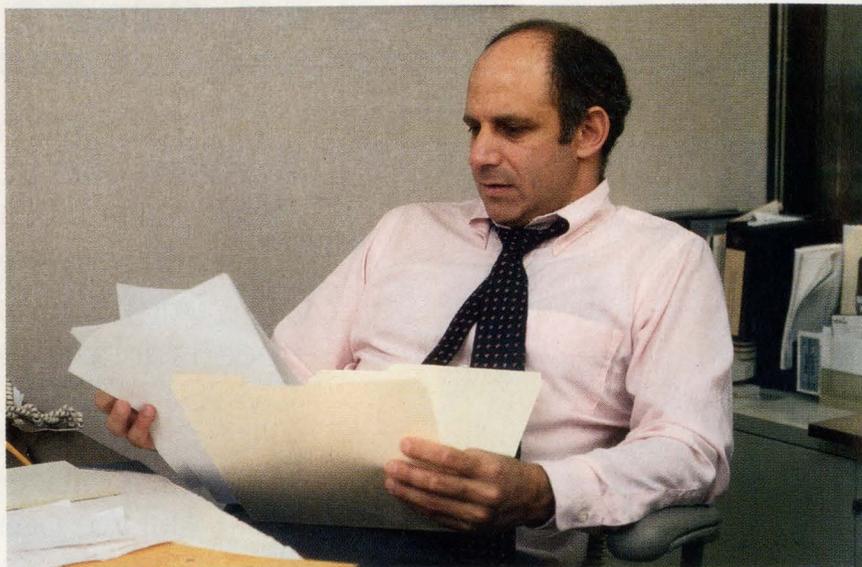


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CIRCLE 155

EDITORIAL



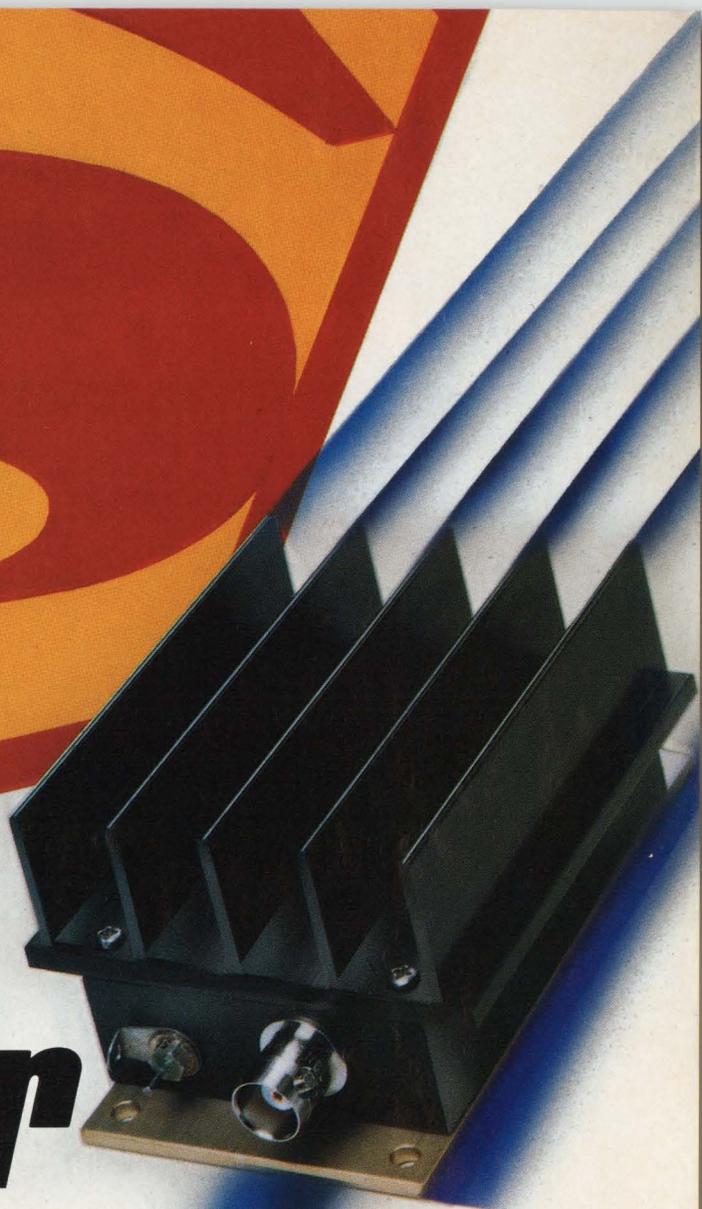
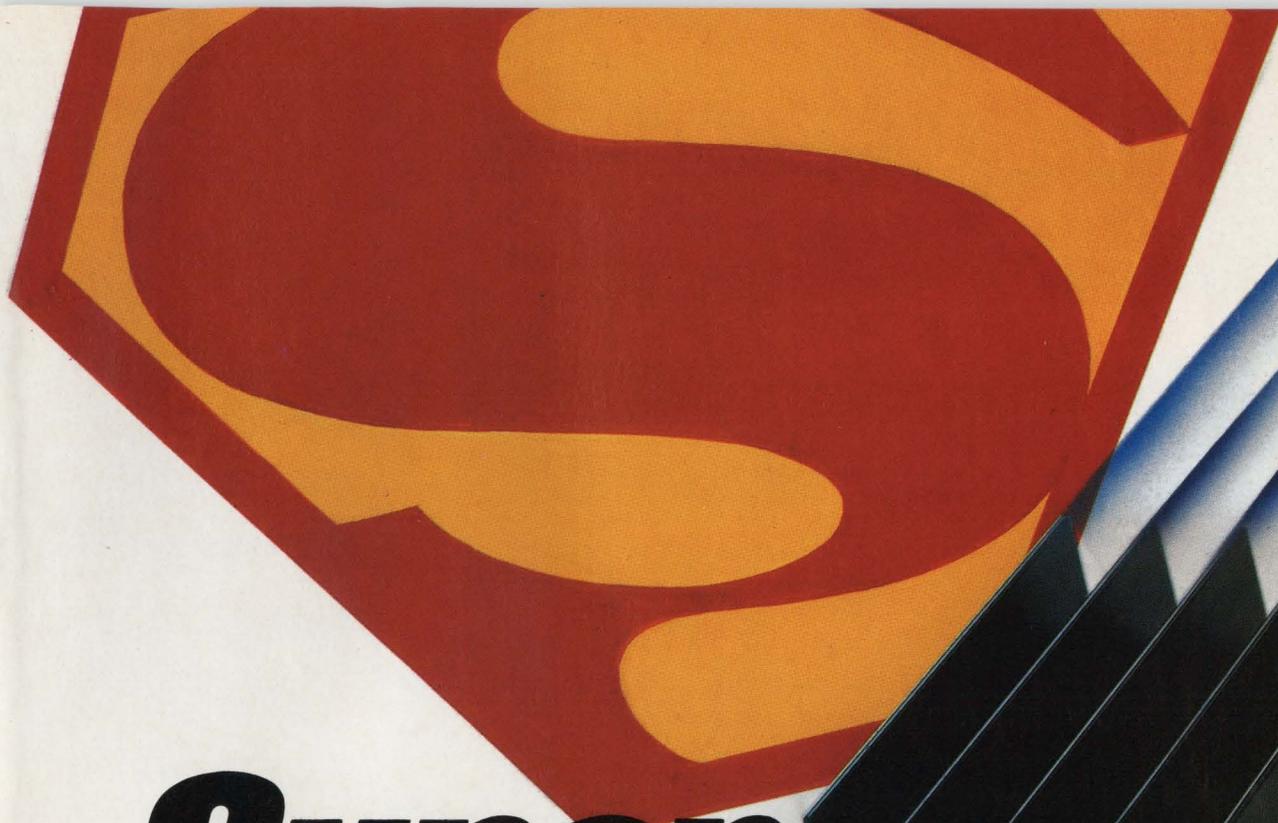
HOW WE DO OUR WORK

On the staff of an international electronics trade magazine, we're constantly forced to consider "The Big Picture"—a broad view that takes in the industry as a whole rather than any particular product or segment. But do we see the results of industry changes on a day-to-day basis? Do these events change the way engineers actually do their jobs? Do these events make their lives easier or more difficult? And what do we actually know about engineers and how they work?

Several years ago, Tracy Kidder won a Pulitzer for his description of the engineering world in *Soul of A New Machine*. Though Kidder deserves lots of credit for attempting to describe the design of a 32-bit minicomputer in literary terms, the book was disappointing overall. Kidder clearly didn't understand the technology he was writing about, nor did he understand the design and debug process. He couldn't grasp what an engineer does 18-hours-a-day in front of a logic analyzer, nor could he comprehend the intense frustrations in failing to find the flaw in the patterns of 1's and 0's. Kidder couldn't describe the magic moment when, after days of trial-and-error, the right logic patterns pop up on that screen. Nothing as earth-shattering as Perestroika—just a satisfied feeling that nonetheless allows the engineer, perhaps for the first time in weeks, to go home and truly relax with his family.

We've consistently said that most of the market numbers we see—one indicator of The Big Picture—usually don't make sense. This isn't because they're too big or too small, but rather because there's usually no connection between the market forecast for a product and what people actually do with it. What we need, perhaps, is a marketer with the understanding of an engineer and the empathy of a novelist—someone whose sense of "the market" manages to touch all of the human concerns of those who actually use ICs, logic analyzers, or CAE software. We need a guru who can consistently make the connection from The Big Picture to the more personal image of how engineers are actually completing their designs.

Stephan Ohr
Editor-In-Chief



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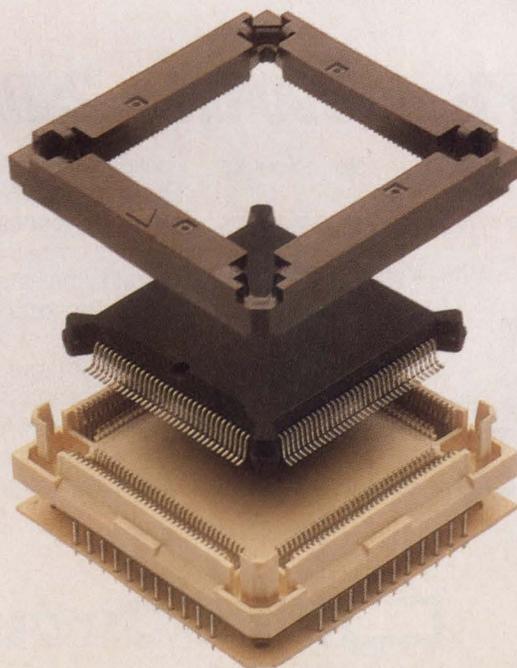
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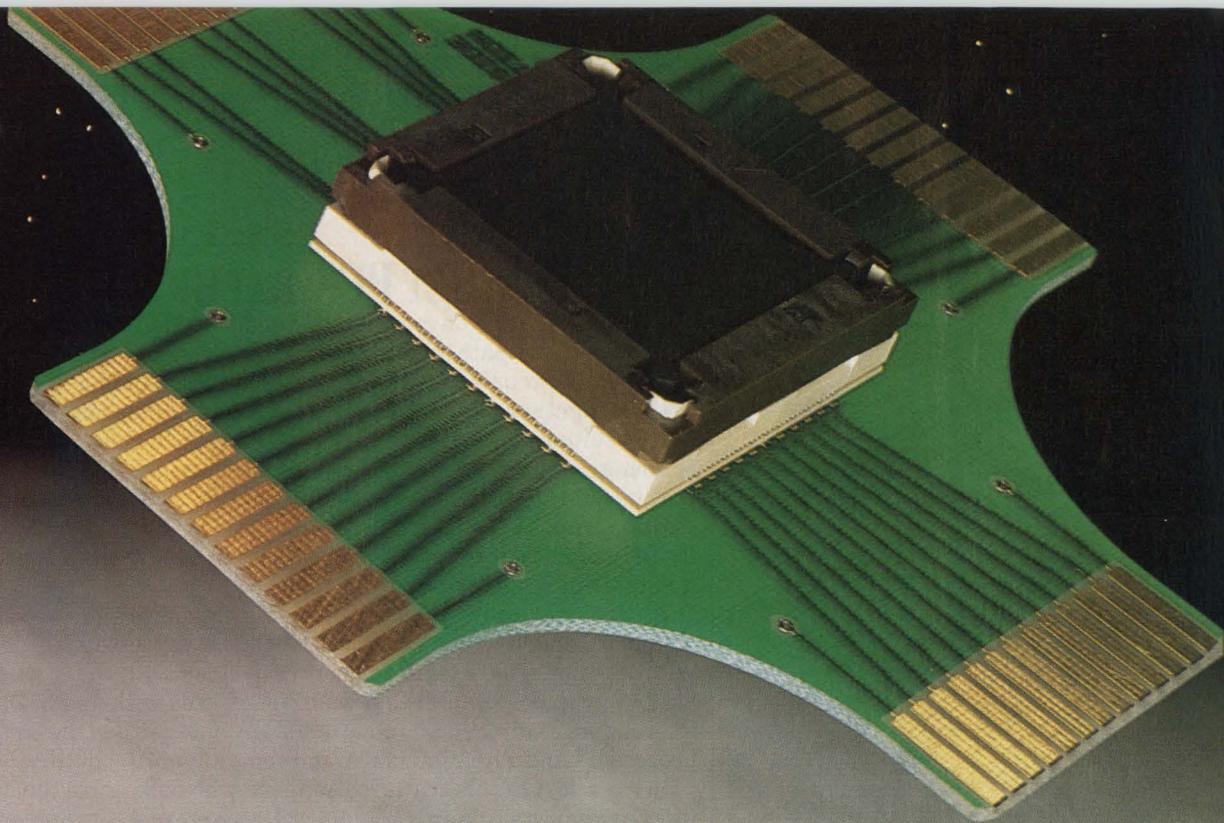
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CIRCLE 157

TECHNOLOGY BRIEFING

WHO WILL SET PC-GRAPHICS STANDARDS?

One are the days when PC vendors blindly follow the path blazed by IBM. PC vendors are now stepping away from Big Blue and banding together to develop next-generation standards better suited for users. IBM standards were already challenged with regards to 32-bit bus architecture. But now its 8514/A graphics controller must face stiff competition from Texas Instruments with its TMS340 family of graphics processors and TIGA (Texas Instruments Graphics Architecture) interface.

It was inevitable that PC users' graphics needs would extend beyond what VGA—640-by-480 pixels with 16 colors—has to offer. IBM responded with the 8514/A graphics adapter that was first offered with its PS/2 line. But not all PC vendors embraced this adapter. Many opted to use the 34010/20 graphics processors and TIGA interface, and some supported both.

In the midst of this scattered support, who will decide the next generation of PC-graphics standards? Last April, a group of PC-graphics hardware and software vendors formed the Video Electronics Standards Association (VESA) to set graphics standards for higher-than-VGA resolutions. The group's membership includes many industry leaders, such as Intel Corp., Hewlett-Packard, NEC, Philips, Sony, and Texas Instruments. VESA's charter is "to facilitate and promote personal-computer graphics through improved graphics standards for the benefit of the end user."

The new organization has begun to act on its charter. It attacked the lack-of-standards problem on several fronts by establishing subcommittees on Super VGA BIOS extensions, Super VGA monitor-timing specifications, and 8514/A specifications. Super VGA is an extended-resolution VGA mode that uses a VGA-type controller for 800-by-600 pixels. One VESA subcommittee established the 800-by-600 pixel, 16-color Super VGA mode BIOS extension, which means that one software driver supports all VESA VGA-display adapters operating in that extended mode. Such companies as Headland Technology and Genoa Systems are now offering products that support the VESA standards.

Establishing standards for extended VGA modes isn't as difficult as establishing them for the 1024-by-768-pixel resolution mode. This is the turf that IBM and TI are fighting over.

The IBM 8514/A adapter card uses two proprietary chips to form a graphics coprocessor. The most important issue concerning 8514/A is the absence of published specifications for the register set. This was done to encourage software developers to use IBM's Adapter Interface (AI) application-programming interface. Programming through the AI can hinder performance, though, and many software writers opt to bypass it. The VESA 8514/A subcommittee is looking into creating common hardware and software specifications, and companies like Western Digital Imaging are supporting it with products. Western Digital even published specifications for its 8514/A-compatible chip set containing the register information needed by software programmers.

But the majority of industry support seems to be behind TI's graphics processor and the TIGA interface. One of the first companies to announce a TMS340-based product was Compaq Computer. Compaq's graphics board boasts 1024-by-768-pixel resolution and 256 colors. Texas Instruments increased efforts to make its graphics system the standard. The TIGA interface specifications were released last April at NCGA when 28 manufacturers announced intent to support the TIGA interface with hardware and software products. Among these companies are Hewlett-Packard, Intergraph, and Microsoft.



LISA GUNN
MICROPROCESSOR EDITOR

A scope so good you have to see it.

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The HP 54501A Digitizing Oscilloscope is shown with its control panel and a video cassette tape. The oscilloscope screen displays a square wave and a pulse waveform. The control panel shows settings for TIMEBASE (500 ns/div), delay (2.10000 us), and reference (left, center, right). The video cassette tape is labeled "The HP 54501A - Affordable Digitizing Performance".

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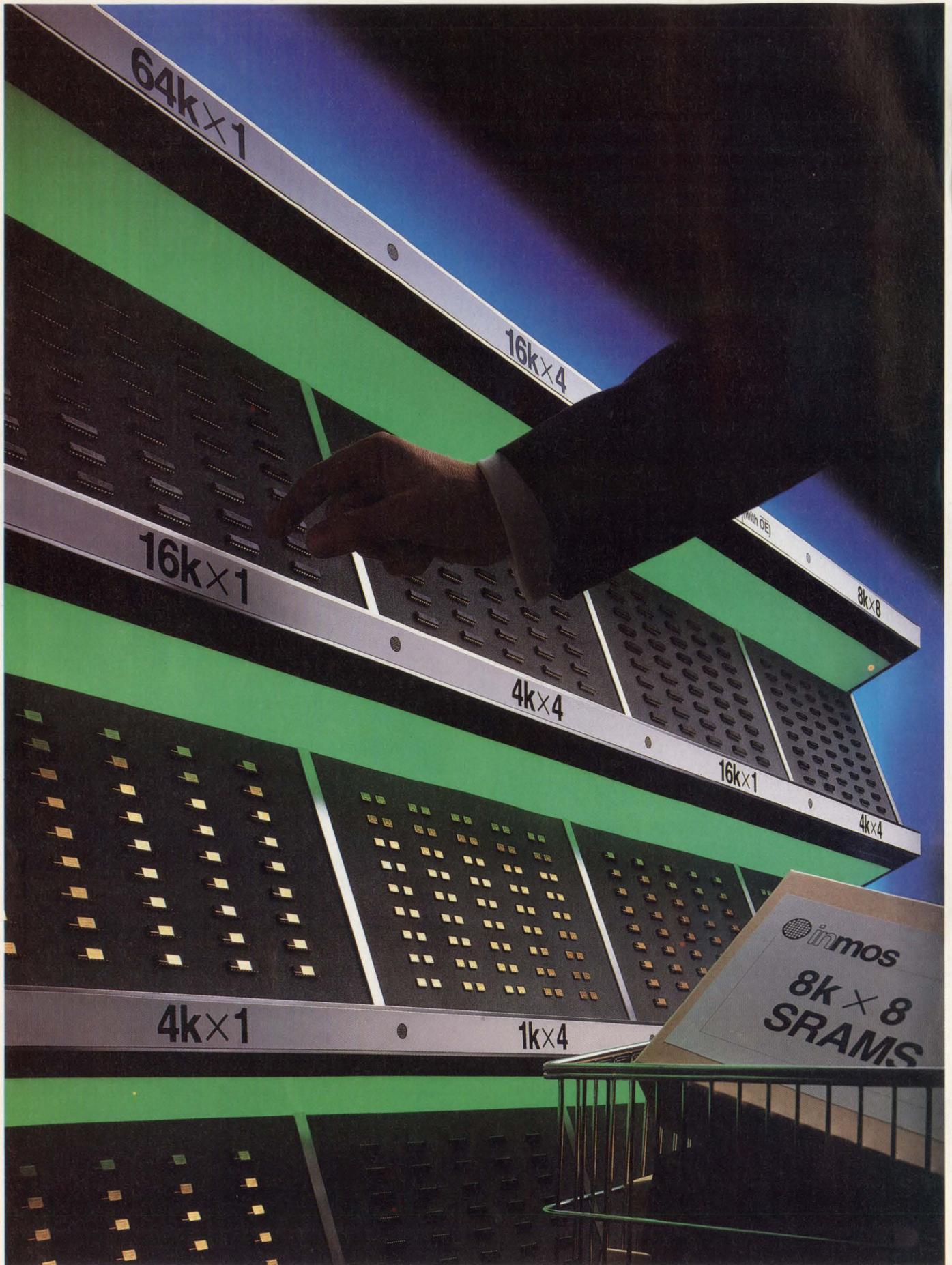
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	IMS 1203M	25,35,45		IMS 1601L	45,55
1K×4	IMS 1223	20,25,35,45		IMS 1600M	45,55,70
	IMS 1223M	25,35,45		IMS 1601LM	45,55,70
16K×1	IMS 1403	25,35,45,55	16K×4	IMS 1620	25,30,35,45,55
	IMS 1403M	35,45,55		IMS 1620M	45,55,70
	IMS 1403LM	35,45,55		IMS 1620LM	45,55,70
	IMS 1400M	45,55,70	IMS 1624	25,30,35,45,55	
4K×4	IMS 1423	25,35,45,55	IMS 1624M	45,55,70	
	IMS 1423M	35,45,55	IMS 1624LM	45,55,70	
	IMS 1420M	55,70	8K×8	IMS 1630M	55,70
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SINGLE-WAFER EPI SYSTEM CUTS COSTS

A new system promises to drop the cost of creating thin epitaxial silicon layers, which are critical for fast ECL and biCMOS circuits, and thus trim the cost of the finished circuits as well. The IPS 3000e epitaxial deposition system, from Rapro Technology Inc., Fremont, CA, processes wafers one at a time but still manages to cut the epi-layer cost to about 50% of other batch or single-wafer systems. The key is a small, low-pressure process chamber that minimizes chemical consumption. It takes about two minutes to deposit a 2- μ m epitaxial film on a wafer. That's not the industry's fastest time, but the company says its film has higher quality and much smaller transition depth (by two or three times) than epi layers created by other systems. Shorter transition regions, in turn, mean faster transistors. Furthermore, the system can be configured with multiple process chambers to combine several manufacturing steps in one machine, which results in less wafer handling and lower particulate contamination. DB

SUPERCONDUCTOR FILTER EXCELS AT 2 GHZ

A microwave comb filter made of high-temperature superconducting material exhibited a Q factor 100 times higher than a conventional copper filter. The filter, made of thin films of yttrium-barium-copper oxide on lanthanum-aluminum substrates, had a Q of 3000 at 2 GHz compared with 30 for conventional devices. And at 10 GHz, the filter was still 10 times more efficient. Developed by the David Sarnoff Research Center, Princeton, N.J., the component was made of thin-film material supplied by Bell Communications Research Inc. (Bellcore), Livingston, N.J. The filter's operating temperature reached 79° Kelvin. Working with Rutgers University scientists, Bellcore researchers created the material with a pulsed-laser deposition technique that was developed at Bellcore's Solid-State Science and Technology Laboratory. JN

IMAGING TECHNIQUE SHOWS BONE DEFECTS

Orthopedic researchers at the University of Michigan have found a unique imaging technique to help them study microscopic bone structures. The technique, which will help them see how age, disease, and physical forces effect the bone, was originally used by Ford Motor Co. to detect flaws in auto parts. The nondestructive imaging technology, called microcomputed tomography, draws 3D pictures with up to 200 times the resolution of a regular medical scanner. In the process, X-rays are passed through the sample and their intensity is measured with a high-resolution sensor. Image intensities are digitized and recorded before the sample is rotated a precise number of degrees and the process is repeated. A computer then combines the individual frames into a 3D image. LG

GATEWAY MAY BREACH E-MAIL BARRIERS

Communication barriers among incompatible electronic-mail systems could soon crumble. The X.400 Application Program Interface Association (APIA), a coalition of leading computer and communication vendors, has specifications for the industry's first vendor-independent e-mail interface. The e-mail application program interface (API), called X.400 Gateway API, helps programmers create gateways between any vendor's electronic-messaging system and an X.400-based message-transfer agent. X.400 is a set of CCITT procedures and formats that exchange e-mail among computer systems and the IEEE POSIX standards committee may make the new specifications a formal standard. APIA is also looking at specifications for an Application API, which will create a universal interface between nonmessaging applications like graphics or spreadsheets. To obtain published copies of the Gateway API specifications from the APIA, call David Knight at Retix, (213) 399-2200, or Stephen Layne at Telenet Communications Corp., (703) 689-5476. LG

ETCH-STOP BUILDS BETTER SILICON-ON-INSULATOR

Silicon-on-insulator (SOI) technology has existed as dielectric isolation (DI) for a long time. Now, Texas Instruments, Dallas, has come up with an SOI recipe that improves performance, lowers costs, and makes it possible for designers to place isolated tubs of any size anywhere on a wafer during layout. In contrast, conventional DI demands that each tub be sized and located during wafer creation. The company calls its new process Full Etchstop Layer Transfer (FELT). On a lightly doped silicon wafer, a thin p⁺ layer is diffused to act as an etch-stop. An epitaxial layer of silicon is grown on it, followed with oxide. A thick layer of polysilicon is deposited on the oxide to act as a "handle" or support. Removing the original wafer by grinding and selective etching leaves transistor-quality silicon sitting on a high-quality insulator. Trenching down to the insulation and back-filling with oxide results in desired DI tub sizes. Moreover, the narrow trenches are typically 2- μ m wide, one-tenth that of present DI techniques, resulting in a smaller die size. FG

SOLAR ARRAY BREAKS EFFICIENCY RECORD

Record-breaking efficiency for a photovoltaic-concentrator module—20.3%—was attained by researchers at Sandia National Laboratories, Albuquerque, N.M. The module packs a dozen plastic lenses that concentrate sunlight at 100 times its normal intensity onto 12 silicon solar cells. Those lenses have anti-reflective coatings that further improve the illumination efficiency. The researchers started with a new low-resistivity silicon solar cell developed at the University of New South Wales, Australia. To improve the cell's efficiency, a low-cost plastic lens and a prismatic cell cover were then molded onto the silicon. The prismatic cover reflects any light that's blocked by the grid of power lines crossing the chip back to the silicon surface. The cover also allows for wide grid lines on the silicon surface, which permits those lines to carry higher currents while reducing power losses. To draw heat from the cells, each one is mounted directly on a copper heat spreader, which doubles as an electrical contact. DB

TECHNOLOGY EXCHANGE TO DELIVER DSP TOOLS

One way chip makers and software-tool suppliers can ease the designer's task of writing increasingly complex code for digital-signal-processor chips is by sharing technology. These exchanges can spawn suites of software-development and debugging tools comparable to those for advanced microprocessors, as is the case with Motorola Inc., Austin, Texas, and Intermetrics Inc., Cambridge, Mass. As the result of a deal to share software technology with Motorola, Intermetrics will modify its popular Intertools software-development package to support Motorola's forthcoming 96002, a 32-bit digital-signal-processor chip that does IEEE-compatible floating-point math. Intermetrics estimates it will take about six months to convert its optimizing C compiler, assembler, XDB debugger, and utilities library to work with the chip's architecture and instruction set. Also, an exchange of technical notes on Motorola's software simulator for the 96002 and Intermetrics' XDB debugger will enable the debugger to troubleshoot simulations rather than target hardware. Besides cutting program-development time, that ability will reduce the pressure for designers to finish hardware prototypes early. DB

FOCUSED ION BEAMS HELP IC ANALYSIS

A precision ion-beam-milling and chemical-vapor-deposition system from Seiko Instruments Inc., San Jose, Calif., helps analyze ICs that have features 1 μm and smaller, and that have multiple levels of metal interconnections. Conventional cross-section and laser-cutting tools aren't precise enough for such small dimensions and vertical structures. This particular system serves four functions. As an ion microscope, it reveals chip aberrations with an induced secondary-electron imaging processor that magnifies from 100 to 100,000 times. Beam resolution is 500 \AA . With its focused ion beam, the system can also perform chip cross sections by cutting away material with a precision of 0.2 μm or better. Furthermore, the system can analyze aluminum-grain structures—its ion beam induces high-energy electron emissions from the aluminum with minimal sample preparation. Finally, by combining the focused ion beam and chemical-vapor deposition of tungsten, the system can cut and patch on-chip interconnections to let an analysis team perform post-fabrication circuit modifications. DB

LAYERED SOFTWARE EASES NETWORK INTEGRATION

Engineers and scientists who need supercomputing power and advanced graphics linked by a high-speed network, all compatible with the latest standards, will find it in the SuperCluster Integration Strategy and accompanying software products from FPS Computing, Beaverton, Ore. The Strategy is a layered-software approach to linking supercomputers and high-end visualization machines in a fast network. With the FPS software system, users see the X-Window system as the interface to applications and the network. Even a supercomputer needs no special access. The new software products include FPSMath, which is a set of more than 300 engineering and scientific algorithms to speed application development. FPSMath is available for an "at cost" charge; users pay only a nominal duplication and shipping charge. In addition to X-Windows, FPS offers a PHIGS+ interface for advanced 3D graphics, GKS for 2D graphics, an application-visualization system, and a network file system. LG

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CIRCLE 9

WIRELESS LAN RIDES ON SPREAD-SPECTRUM TECHNOLOGY

Spread-spectrum radio technology is the driving force behind a wireless local-area network from Agilis Corp., Mountain View, Calif. In spread-spectrum transmission, a low-power radio signal is transmitted over many frequencies within a band. The spread signals are then correlated back into a baseband signal at the receiver. Signal spreading reduces power density—the total rf power limit is 1 W—and susceptibility to interference.

The company originally designed the network for wireless communication among its recently introduced handheld workstations (ELECTRONIC DESIGN, June 22, p. 168). The wireless-communication system, now built with discrete components, will be implemented with three custom chips. The chips will include two bipolar ASICs—a baseband analog-signal processor and a high-speed mixer circuit—and one CMOS ASIC that serves as the spreader-correlator (see the figure).

Spreader-correlator technology is the key to spread-spectrum communication. It's easy to spread the signal but difficult to correlate it. A one or zero representation is more complex than just one digit. When a signal is transmitted, the spreader-correlator codes each baseband signal's bit into a sequence of bits called chips. These chips are then embedded in a signal and transmitted by using spread-spectrum techniques. The correlator rebuilds the spread signal.

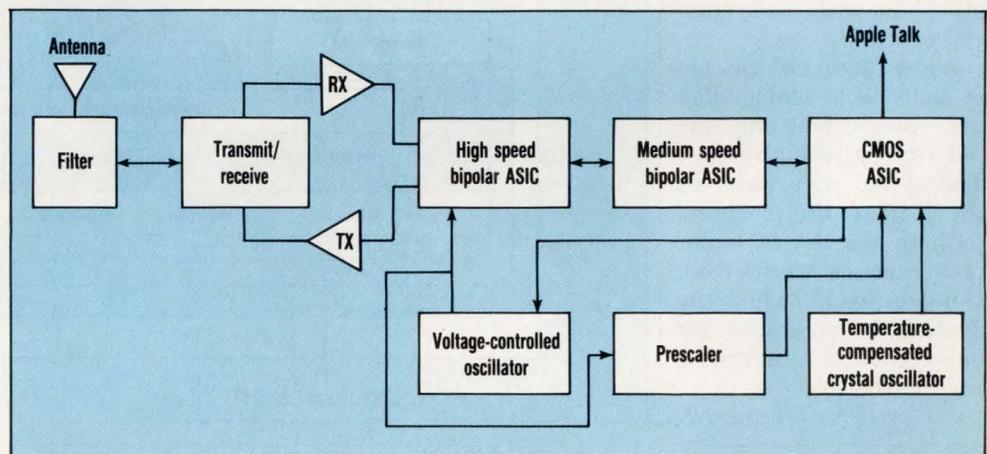
Two conventional methods of correlating the

transmitted signal are matched filter and delay-locked loop. However, Agilis opts for a proprietary technique using a 5000-gate digital-signal processor. A principal benefit of this spread-spectrum technology is that it doesn't require licensing by the Federal Communications Commission.

The network operates at 230.4 kbits/s. The current design could transfer up to 1 Mbit/s, with the spreader-correlator's clock speed as its primary limitation. Using two higher bandwidths could push rates to 10 Mbits/s—the same as Ethernet. Until then, a store-and-forward scheme matches the data rates of

wireless networks to those of wired networks. In this scheme, data is transmitted at the slower speed and stored at an intermediate location before its transmitted at the higher speed. The network is compatible with AppleTalk and can operate up to 1 km outdoors and 100 m indoors.

LISA GUNN



VLSI TECHNOLOGY SQUEEZES TESTER ONTO ONE CHIP

The cost of testing VLSI devices rises dramatically with each succeeding generation of chips. Production testers, for example, can cost \$2 million, and that doesn't include the cost of the air conditioners, the power lines, and the raised-floor their installation may require. In an effort to lower these costs, one test-instrument maker decided to fight fire with fire by applying a unique VLSI circuit to build small, cost-efficient testers. At least that's the route charted for the next generation of systems from ASIX Systems Corp., Fremont, Calif.

The heart of the forthcoming system is VChip, a

full-custom 120-cell ASIC that contains a complete dual-channel test system. The chip is a 1.6- μ m n-well CMOS device with double-metal interconnect layers. It was configured with layout tools from VLSI Technology Inc.

Each chip has two channels that generate six timing edges, pegging timing accuracy to better than 1 ns with a resolution of 100 ps. Because the chip can drive CMOS inputs, it connects directly to the device under test or to traditional pin electronics. Output data is generated as return-to, nonreturn-to, or complement-of formats. The outputs themselves offer three choices: three-

state or drive, one or zero, or surrounded-by-complement. Furthermore, a delay can be assigned to any output. Other features include built-in calibration, period and resolution control, and timing-overlap compensation for round-trip delays. Moreover, output changes can be made on-the-fly.

On power-up, each chip calibrates its timing to a ± 1 -ns accuracy without operator or program intervention. That accuracy holds as long as the chip directly drives the circuit under test. Intermediate pin electronics may require further calibration.

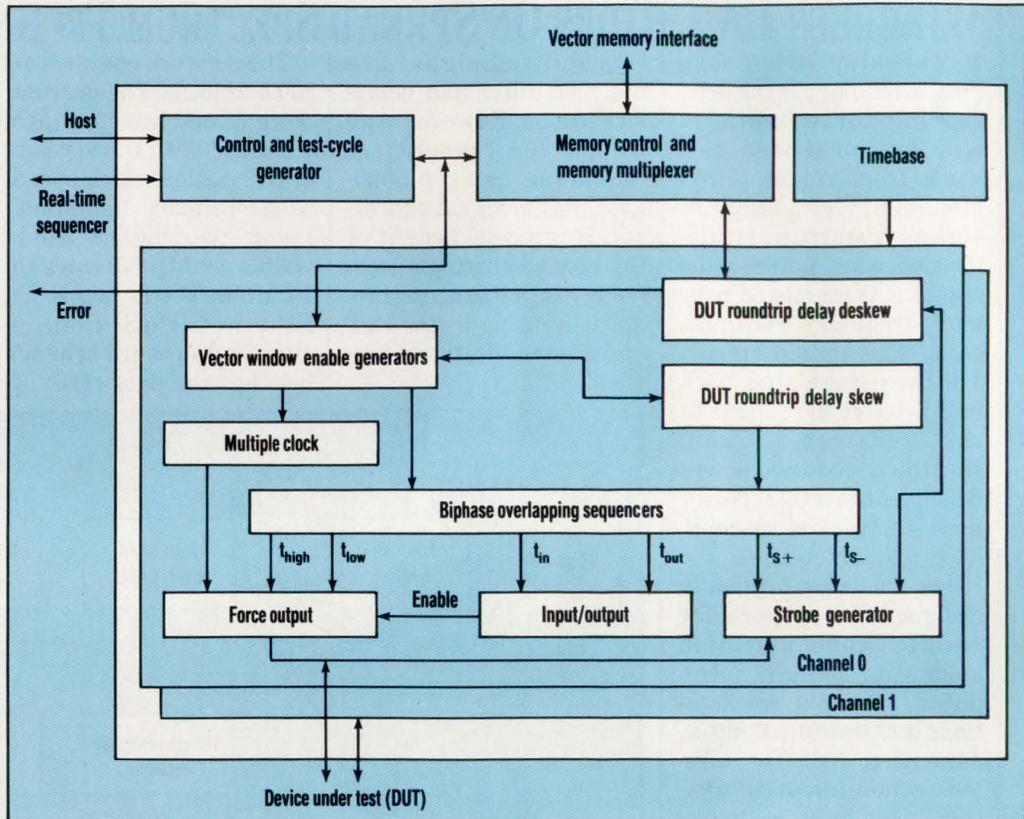
The compensation circuitry automatically and immediately corrects variations caused by semiconductor processes, the power supply, and tempera-

ture changes, and it also corrects for aging. The chip also automatically calibrates each timing generator for variations in channel-to-channel skew and internal or external driver and comparator delays.

As a result, more than 100 VChips can be connected in one system, linked only by a common oscillator. They're automatically synchronized with each other and with the system reference.

A key feature of the chip is that each timing-edge generator drives only one polarity, either high or low. Therefore, regardless of the format, the electrical path to the device under test remains unchanged. Consequently, when the system is calibrated for one format, it's calibrated for all formats.

JOHN NOVELLINO



SILICON GIVES RACE-CAR SIMULATOR THE FEEL OF REAL DRIVING

Real-time 3D simulators that cost millions of dollars are common tools for astronauts training for space travel and for airline pilots mastering the newest jets. However, an astonishingly realistic race-car simulator is now pulling into local bars and video arcades—at a cost of about \$15,000.

Players can test their skill on a game called *Hard Drivin'* from Atari Games Inc., Milpitas, Calif. The game harnesses five microprocessors to give players a realistic ride behind the wheel of a high-performance auto. Though the race-car simulator is only a game, it suggests applications in education. This relatively inexpensive machine, with a change in software, could teach

emergency driving to police-car, fire-truck, and ambulance drivers. Further modified, it could train future truck drivers or heavy equipment operators to handle their vehicles under various road, load, and speed conditions.

Simulated action enables the novice hot-rodder to make a vertical loop, jump an open drawbridge, and race at high speed through slow or on-coming traffic. If a maneuver causes the racer to roll over, the driver sees the displayed world upside down.

The driver interacts directly with the host processor through four mechanical links: the steering wheel, gas pedal, brake, and four-speed shift. A counter force is fed back to

the wheel for sharp turns, simulating the feel of high-speed cornering. Furthermore, a strain gage on the brake pedal translates increasing braking pressure into a proportional deceleration rate as it increases pedal resistance.

The combined processing power of the five microprocessors, which is behind the realistic action, approaches 30 MIPS. A Motorola 68010 oversees the other four processors, which include an Analog Devices ADSP-2100 video digital signal processor that executes the complex mathematical routines needed to manipulate the 3D images in real time. The processor handles more than 1000 polygons within each frame-time. It gets road and obstacle informa-

tion directly from a 32-kbyte program memory and communicates with the host through a 16-kbyte data memory.

At the same time, a Texas Instruments TMS34010 graphics processor pulls data from memory through a dual-port video RAM. This data is pulled at a rate that's fast enough to continuously change the 3D display.

Under the host's direction, a second 68010 and a TI TMS32010 simulate various sounds, such as breaking glass, the car's engine, and the subtle sound of a passing car that includes the Doppler-shift. The output of this processor pair drives a speaker through a 12-bit AMD6012 digital-to-analog converter.

FRANK GOODENOUGH

CAE Technology Report

Vol. 1, No. 4

July 1989

Mentor Graphics Opens The Door

Both the CAE industry and CAE users should benefit from Mentor Graphics recently-announced Open Door™ program that coordinates and integrates third-party CAE tools within Mentor's design environment. Acknowledging that no CAE vendor can provide all solutions to all users, Mentor has invited other CAE vendors to interface their tools with Mentor's CAE environment. A successful program will significantly increase Mentor's penetration of the CAE marketplace.

DAC '89 Confirms Growing Use of Personal Computers for CAE

The recent Design Automation Conference in Las Vegas confirmed what the industry already knew: PCs are the primary CAE engineering tools. Over 73% of engineers now use PCs for design, and 386-based PCs will further reinforce the major role of PCs in design applications. Despite the lower cost, some PC software is superior to their workstation counterparts. For example, *SUSIE™ is a PC-based realtime logic simulator, whereas all workstation simulators are still batch-based and simulate several times slower. Also, there is no simulation standard for workstations, whereas almost all PC-based CAE vendors have opted for the SUSIE realtime logic simulator. Standardization is coming much faster to PCs than workstations, which will further reinforce the leading role of PCs in the CAE field. Circle 101.

Libraries are the Key to Simulator Success

It is now clear that no single IC model supplier can follow the semiconductor industry and fill all the diverse user needs. To provide better support, ALDEC, SUSIE's manufacturer, has added 12 engineers for library support. In addition, ALDEC is developing tools that allow the designer to model industrial controllers, processors and complex ICs. To provide additional support, ALDEC is organizing a CAE franchise network and will lend tools to companies and individuals who want to share their models with the industry (on a royalty basis). For more details, call Keith McCann at (805) 499-6867. Circle 103.

Xilinx™ Parts Get a Realtime Simulator

The first realtime simulator for Xilinx parts is ALDEC's newly-announced SUSIE/LCA that automatically reports timing violations and bus conflicts. Also, the user can modify and simulate its IOB and CLB blocks "on-the-fly." Similarly, SUSIE can emulate cell layout delays, making fixes relatively simple. The SUSIE/LCA has many user-friendly options. Want more information? Circle 105 or call ALDEC at (805) 499-6867.

SUSIE Supports GigaBit GaAs Logic

ALDEC (Newbury Park, CA) has added a GigaBit GaAs chip model library for use in its SUSIE logic simulator. These models were created in a joint effort between ALDEC and Gigabit Logic (Newbury Park, CA). This insures exact functional and timing replication for these devices, as specified in GigaBit's GaAs IC data book. Circle 102.

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THE TECHNOLOGY BEHIND BETTER COMPUTER GRAPHICS

SIGGRAPH IS SHOWCASING THE LATEST INNOVATIONS
THAT ARE FUELING THE ADVENT OF ADVANCED
INTERACTIVE 3D GRAPHICS.

LISA GUNN

As they mature, computer graphics are edging their way into a bevy of new applications. Such tasks as scientific visualization and geometric modeling demand extremely fast, high-resolution graphics. This level of performance is being met by improvements in both hardware and software.

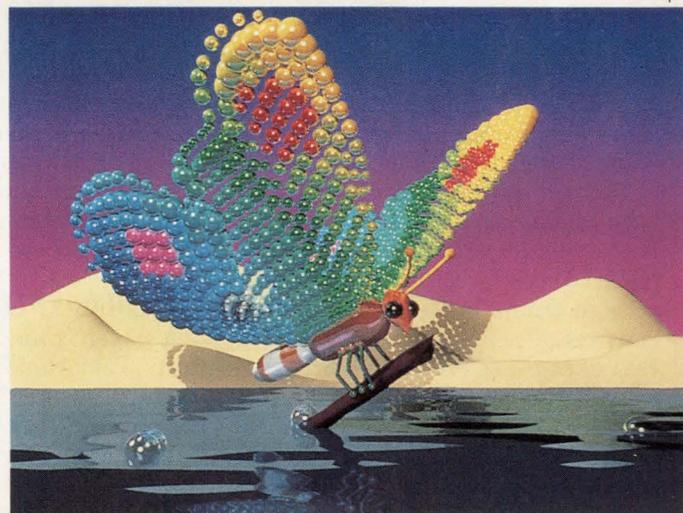
Some of the newest advances in computer graphics will be showcased at ACM Siggraph, July 31 through August 4, in Boston (*see the figure*). The 16th annual conference on computer graphics and interactive techniques plays host to 30 full-day courses and 11 technical-paper sessions, which will cover all aspects of hardware, software, and theory. Sixteen panel sessions will explore new trends in computer graphics. In addition, nearly 225 manufacturers will show state-of-the-art developments and products.

The paper sessions will cover the advanced technology found in today's highest-end graphics systems. Many graphics applications require rapid display of interactive computer-generated images. In light of this, researchers at the University of North Carolina developed Pixel Planes—a massively parallel image-generation architecture. A paper from the Department of Computer Science at the university, Chapel Hill, will describe the heterogeneous multiprocessor graphics system that uses processor-enhanced memories.

Dubbed Pixel-Planes 5, the system is

a heterogeneous multicomputer system designed for fast polygon and sphere rendering of up to 1 million Phong-shaded triangles/s. It also supports algorithm and application research in interactive 3D graphics. The Pixel-Planes 5 system addresses techniques for volume rendering at multiple frames/s, font generation directly from conic-spline descriptions, and rapid calculations of radiosity form factors.

The hardware consists of up to 32 math-oriented processors, up to 16 rendering units, and a conventional 1280-



THE NEW HARDWARE and software techniques being demonstrated at Siggraph are yielding more realistic 3D computer graphics. This computer-generated image is from the Los Alamos National Laboratory in N.M.

by-1024-pixel frame buffer, all linked by a 5-Gbit ring network. Each rendering unit consists of a 128-by-128-pixel array of processors with memory. Parallel quadratic expression evaluation is performed for every pixel. Implemented on 1.6- μ m CMOS chips designed to run at 40 MHz, this processor array has 208 bits/pixel on chip and connects to a video-RAM memory system that contains 4,096 bits of off-chip memory. Rendering units can be independently reassigned to any part of the computer screen or to non-screen-oriented computation. Both hardware and software are still under construction, with initial system operation scheduled for this fall.

PIXEL PROCESSORS

In the Pixel-Planes system, each pixel has its own processor, as well as local memory for storing pixel color, Z-axis depth data, and other pixel information. Custom VLSI chips contain pixel memory, the pixel processors, and a linear-expression evaluator. An array of these chips forms a smart frame buffer, which is a 2D-computing system that receives descriptions of graphics primitives in the form of coefficients with instructions. The buffer performs all pixel-level rendering computations.

Parallel processing of images is the subject of another Siggraph paper from AT&T Bell Laboratories, Holmdel, N.J. The AT&T Pixel Machine is a parallel image computer with a distributed frame buffer.

The computer's architecture is based on an array of asynchronous multiple-instruction, multiple-data (MIMD) nodes with parallel access to a large frame buffer. The machine consists of a pipeline of pipe nodes that execute sequential algorithms, as well as an array of $M \times N$ pixel nodes that execute parallel algorithms. A pixel node directly accesses every M th pixel on every N th scan line of an interleaved frame buffer. Each processing node is based on a fast, floating-point programmable processor. Because of the computer's programmability, all algorithms are executed in software.

User interfaces are an extremely

important part of the computer-graphics environment, and windows is the interface of choice in many systems. Hewlett-Packard's Graphics Technology Division, Fort Collins, Colo., will present a Siggraph paper on a hardware accelerator for window systems.

Not only must the window-interface system support fast graphics within multiple windows, but must also support interactivity (users must be able to simultaneously change parameters). Because window systems are so popular, graphics pipelines are expected to support multitasking workstations.

The main difficulty in context switching a graphics accelerator is the latency encountered during a pipeline flush. This latency slows the responsiveness and interactivity of the graphics system. In addition, pipeline latency increases as the system's pipelines grow longer and the graphics primitives become more complex.

HP attacks the latency problem with a hardware solution. In a windows environment, each process associated with a window views the workstation's resources as if it had them to itself. Therefore, resources must be shared in a manner that prevents conflicts.

The HP system's goal is to supply each process with a virtual graphics device whenever it requests one. In the past, sharing one graphics accelerator between processes traditionally required pipeline flushing and resynchronization. HP's new hardware speeds the window system by eliminating these needs.

BUILDING INTERFACES

A paper from Digital Equipment Corp., Palo Alto, Calif., also addresses the user-interface issue, describing a system for constructing graphical user interfaces according to a two-view paradigm. One view contains a textual representation of the interface in a special-purpose, descriptive language; the other contains a direct-manipulation, interactive editor for the user interface. Though the user interface can be edited in either view, the changes are

reflected in both.

With the special-purpose language, dialog boxes can be expressed simply and naturally. The language view also has well-defined mapping into the interactive editor view. This dual-view method of building user interfaces combines the advantages of direct manipulation with those of a textual, descriptive approach, without suffering the limitations of either. Digital Equipment's system, called Forms VBT, supports an extensive library of interactive objects.

RAY TRACING

Many applications using advanced graphics require realistic lighting effects. Most often, this type of realism is achieved with ray-tracing techniques. But when fast image rendering is needed, ray tracing is slow. A paper from the Electrical Engineering and Computer Sciences Department of the University of California, Berkeley, introduces a new technique to speed up the generation of successive ray-traced images. The geometry of the scene must remain constant and only the light-source intensities and the surface properties can be adjusted.

When a computer image is first ray traced, an expression with light-color parameters and surface-property coefficients is calculated and stored for each pixel. Redisplaying a scene with a new set of lights and colors entails substituting values for the corresponding parameters and re-evaluating the expressions for the pixels.

This parameter updating, re-evaluation, and redisplaying takes only several seconds, as compared with the many minutes or hours required to completely ray trace the entire scene again. But the faster method uses much more memory and disk space. Expression sharing can reduce the storage needs to an acceptable level. □

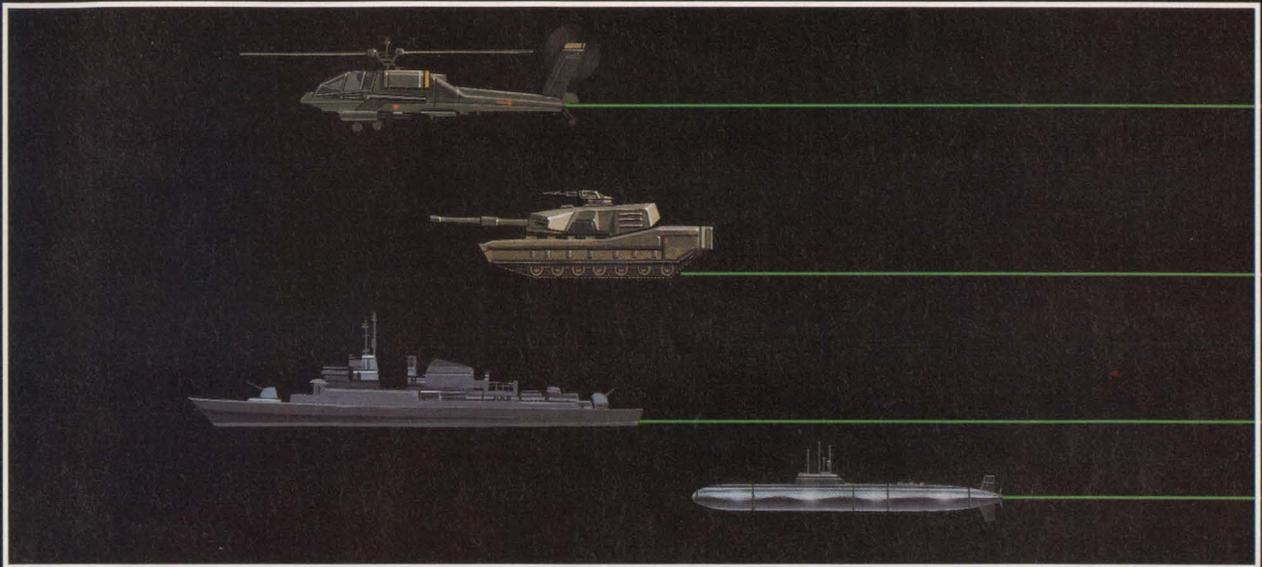
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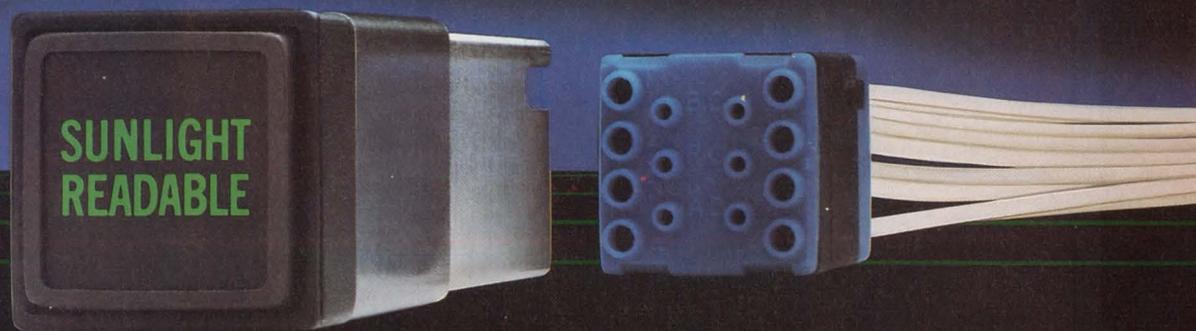
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Discharge resistor	150 Ω ± 5%
Charging resistor	100M Ω ± 10%
Rise time of the discharge current	5ns ± 30% at 4kV
Operating mode	SINGLE, COUNT, REPEAT and 20/S (20 discharges per second, activated for approx. 5 sec with each depression of the trigger switch)

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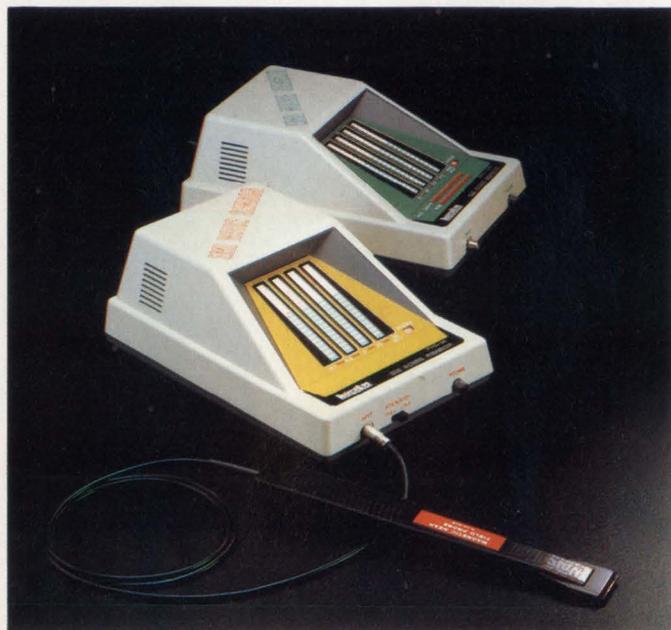
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4. An electric near field probe and a magnetic near field probe of high sensitivity are furnished as standard accessories.

Equipment summary

	FVC-NA1000	FVC-NA30
Frequency range	30MHz ~ 88MHz 88MHz ~ 216MHz 216MHz ~ 470MHz 470MHz ~ 1000MHz * Simultaneous 4 spectra measurement	100KHz ~ 500KHz 500KHz ~ 3MHz 3MHz ~ 10MHz 10MHz ~ 30MHz * Simultaneous 4 spectra measurement
Display	20-point LED bar graph display for each frequency band.	20-point LED bar graph display for each frequency band.



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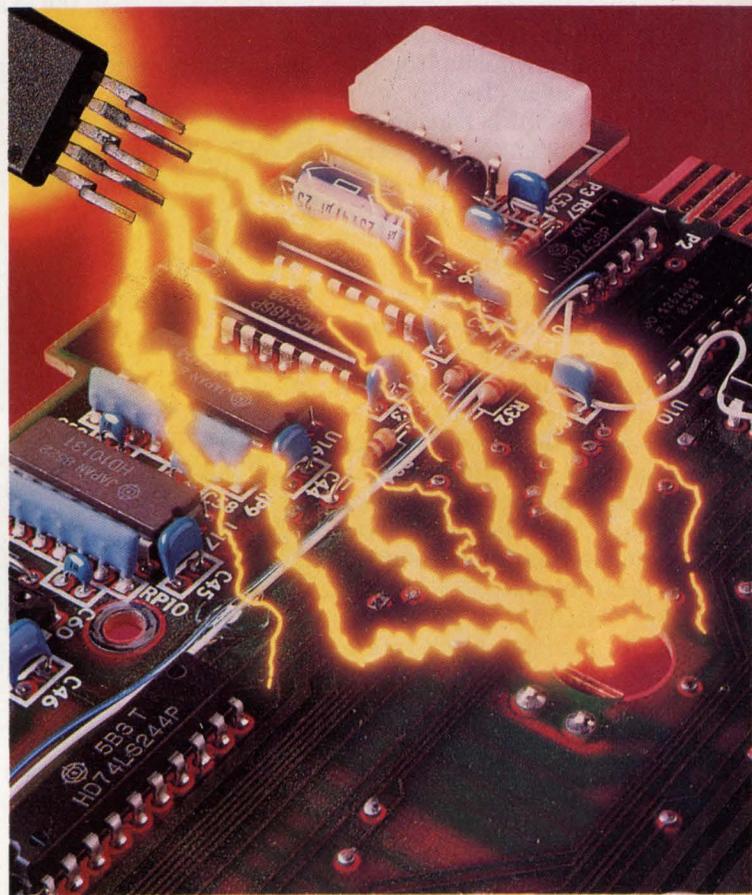
FRANK GOODENOUGH

Now you don't have to be an expert to use switching regulators. Linear Technology and National Semiconductor have made them as easy to use as linears. Furthermore, National is actually guaranteeing system designers a certain performance level when they use National's switching regulators with other supplier's parts.

For over a decade, well-established controller ICs, such as the 1524/25/26 and the 494 series, have made the job of designing switching-regulator power supplies easier. Numerous controller chips have appeared more recently, each with its own areas of application advantages and disadvantages. And these controllers have dropped in cost. The pulse-width-modulated (PWM) switch-mode power supply (SMPS), initially built from discrete devices, now makes use of regulator-controllers.

Though switching regulators have been around almost as long as linear regulators (15 and 20 years respectively), until now, designers had to be maven in magnetics to actually design them. Yet they could drop in three-terminal linear regulators as easy as a resistor. An experienced analog circuit/system designer blanches at the thought of taking on switching regulators in a moment of reckless optimism.

If logic or computer system design is your specialty, you're usually smart enough not to attack these beasts. To



think about trying to control a dc voltage to 1% or 2% accuracy by changing the width of 5-A, 50-V pulses coming at you at 50 kHz to 1 MHz through an inductor is mind boggling to the uninitiated in switcher design (just think what those pulses can do to nearby CMOS logic on the same board).

For years, a wide range of three-terminal linear regulator ICs made it easy for system designers to get clean, constant, supply voltages regulated for

COVER: SWITCHING REGULATORS

line and load changes. These chips respond fast and come right off the shelf in standard voltages and standard packages. If you're an analog, digital, mechanical, or optical designer, just determine the specifications of the device you need, find it in a catalog, buy it, and drop it onto the circuit board and/or heat sink. However, linear regulators are notoriously inefficient, and you can't get a higher voltage out than you put in. But the newest switching regulator ICs are now changing all that.

Both Linear Technology and National Semiconductor are announcing their own family of one-chip switching regulators. Linear Technology's LT1074 and National's LM1575/2575 and LM1577/2577 are as easy to use as linear regulators. Both companies will call out the performance of these power ICs when used in predefined switching-regulator circuits if the passive parts (including inductors and catch diodes) called out on the data sheet by model number and manufacturer are also used. Furthermore, National guarantees supply performance.

The LT1074 is a 5-A, classic, positive-buck (step-down) regulator. An innovative circuit and process wrinkle enables the power switch's output to swing 40 V below ground. As a result, the regulator adapts to other topologies. These include a buck converter with a tapped inductor—which gives you 10-A rather than 5-A output, a positive-to-negative converter, a negative boost converter, and a flyback or forward converter. As a buck converter, input voltages can run between 8 and 60 V, and output voltage is set between 2.5 and 50 V by two resistors (Fig. 1a). Only eight external parts

are required to run this complete switching regulator circuit.

Though it operates in the voltage mode, an internal analog multiplier supplies current-mode-like feed-forward operation. Thus, the circuit responds almost instantly to input-voltage changes. Loop gain is independent of input voltage, and loop stabilization over a wide range of input voltage and load current is simplified.

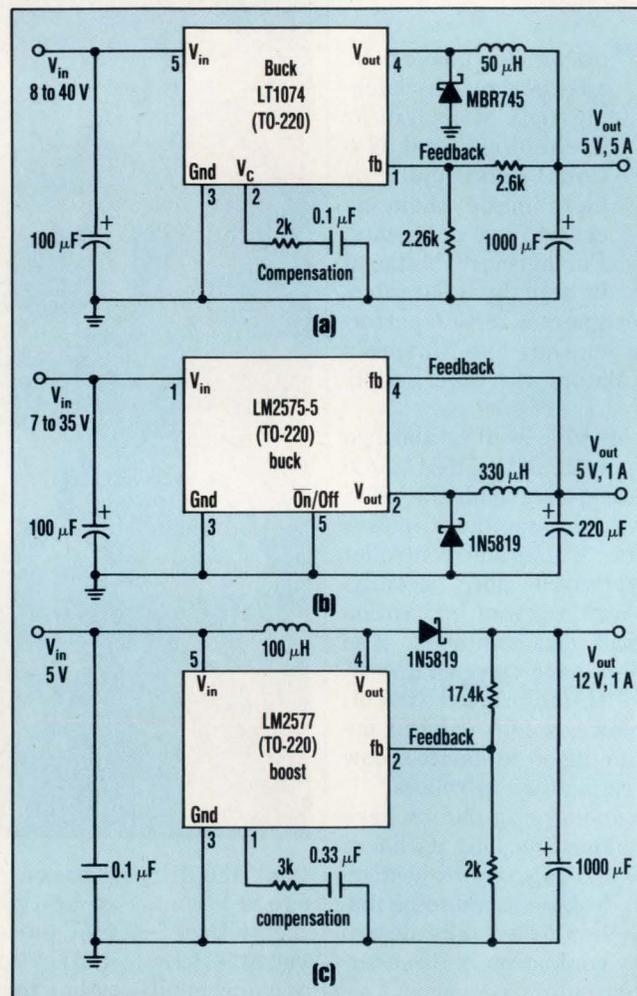
In addition to TO-3 and TO-220 packages, the LT1074 is also available in an 11-pin single-inline package. With the extra pins on the SIP,

you can up the frequency from a preset 100 kHz to as high as 200 kHz, adjust the internal pulse-by-pulse current limit from its fixed 7 A down to zero, and shut the chip down to a quiescent current of just 100 μ A. Furthermore, a Status output pin goes low when the circuit is out of regulation, and a COMOUT pin gives an output pulse that's the complement of the switch output. The pulse can drive external MOSFETs when the peak of efficiency is needed.

National's chip designers took a different tack by using two chips: the LM2575 1-A buck converter and the

LM2577 3-A boost converter. There are four output versions of the first, three of the second. The buck converters operate on inputs from 6 to 35 V. Like linear regulators, fixed 5-, 12-, 15-V and adjustable-output voltage versions are available. The fixed-voltage buck converter needs just four external parts; the adjustable version needs six (Fig. 1b). The boost chip operates with as little as 5 V on the input. Two fixed-output versions step the 5 V up to 12 V and 15 V, respectively. The adjustable version can develop outputs to 60 V. The fixed units require six external parts; the adjustable unit needs two more resistors in the feedback loop (Fig. 1c).

Like the LT1074, the LM2575, and LM2577 converters are equipped with adjustable current-limiting circuits and a fixed-frequency oscillator (52 kHz for the National parts). They're also protected by thermal-shutdown circuits with hysteresis characteristics. Furthermore, like the 11-pin LT1074, the LM2575 has a shutdown pin that cuts the quiescent current to a maximum of 500 μ A from its nominal 12 mA maximum, over tem-



1. THE LINEAR TECHNOLOGY LT1074 buck-regulator IC takes just eight parts for a complete circuit (a). The two resistors set the circuit's output voltage between 2.5 and 50 V. In National's buck regulator IC, the LM2575-5, both compensation and a fixed 5-V output are handled inside, dropping the total passive parts count to four (b). The LM2577 boost regulator from National requires both compensation and feedback (c).

BOGGED DOWN IN SILICON VALLEY?

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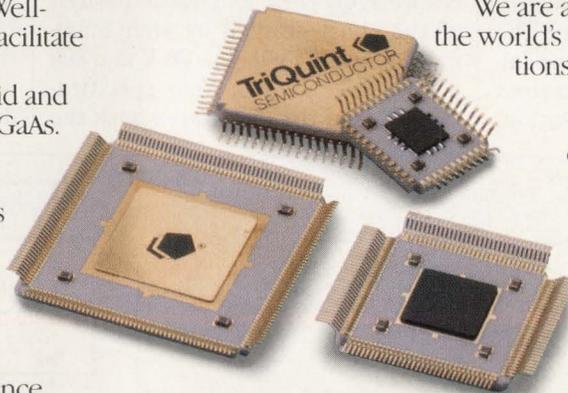


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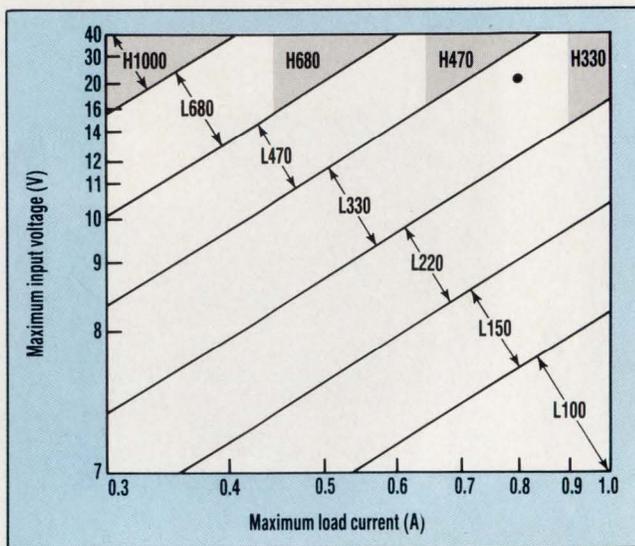
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CIRCLE 35

COVER: SWITCHING REGULATORS

perature. The boost chip, on the other hand, incorporates an undervoltage-lockout circuit that keeps the chip from starting up when the supply voltage is too low. It has a soft-start circuit as well. The 11-pin version of the LT1074 can be given a soft-start with user-selectable current limiting by tying a resistor between the current-limit pin and ground. Undervoltage lockout is achieved by setting the shutdown pin at 2.5 with a voltage divider. A resistor to ground from the FREQ pin raises the clock frequency and a 3-5 V pulse to the pin through a diode can synchronize the chip to a higher pulse rate.

The 52-kHz oscillators in the National converters aren't ordinary controller sawtooth or tri-wave oscillators. Rather, the slope of the ramp-like waveform from the patented circuit increases as the error voltage increases, essentially keeping loop gain constant. The waveform simplifies control-loop compensation and gain adjustment, insuring stability. In fact, the buck converter's compensation can't be externally trimmed. Like the LT1074 buck converter, the LM2575 operates in the voltage mode. The LM2577 takes advantage of the improved line regulation and transient response of current-mode operation.



2. YOU WILL FIND THE INDUCTOR TO USE

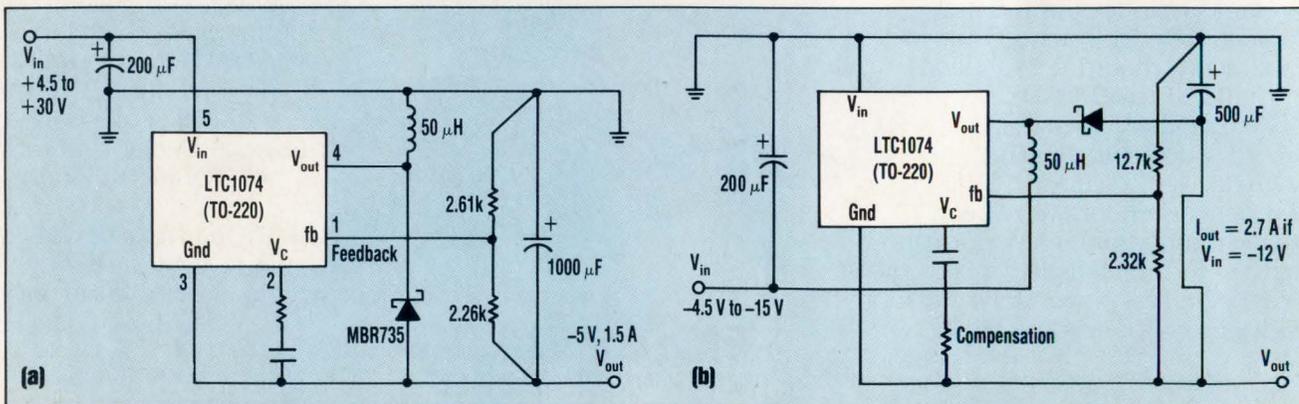
with the LM1575 buck regulator by first locating the area in the chart. The area is determined by your maximum expected load current and input voltage (for example, 20 V, 800 mA as shown by the dot). Then look up the code for the area (L330 for our example) in the table where you will find suppliers' model numbers.

In the past, the most difficult part of creating switching regulators was designing and getting the inductor. National's application engineers now make that job easy. All you need is the value of your maximum expected load current and your maximum expected input voltage. The LM2575 data sheet contains a chart where these two parameters are represented by the chart's X and Y axes, respectively (Fig. 2). Locate the area of the chart defined by your maximum line and load. Use 20 V and 800 mA as an example. Your specifications fall in the chart area with the

"inductor code" L330. Now move to a second chart, which gives the inductor's value (330 μH for our example) and the model number of a device that will do the job—from three different suppliers (see the table, opposite). If your requirements fall in a shaded area, a different coil with the same inductance value is required.

To design your supply, choose an inductor with the two charts, select a catch diode called out on a third data-sheet chart, and follow the simple directions to select the output filter capacitor. If you follow these steps, National Semiconductor guarantees that your supply's output voltage will be between 5.2 and 5.25 V over temperature. They also guarantee up to your maximum input voltage (between 8 and 35 V) and load current (between 200 mA and 200 A)—assuming you used the 5-V-output version, the LM2575-5. All LM2575s are rated for operation from -40 to $+125^\circ\text{C}$, and all mil-grade LM1575s from -55 to $+150^\circ\text{C}$. There are no lower-temperature grades.

In the same manner, circuits built with the TO-3 and TO-220-packaged LT1074s will perform as called out on the data sheet. Linear Technology was supplying model numbers for inductors (but not other devices) on the



3. BECAUSE ITS SWITCH OUTPUT can drop 40 V below ground, Linear Technology's buck-regulator can be connected to supply a negative output voltage from a positive input voltage (a). If given a low negative input voltage, it can also boost it to a higher value (b).

COVER: SWITCHING REGULATORS

INDUCTOR MAKERS' PART NUMBERS

Inductor code	Inductor value	AIE Magnetics	Pulse Engineering	Renco Electronics
L100	100 μ H	415-0930	PE-92108	RL1955
L150	150 μ H	415-0953	PE-53113	RL1954
L220	220 μ H	415-0922	PE-52626	RL1953
L330	330 μ H	415-0926	PE-52627	RL1952
L470	470 μ H	415-0927	PE-53114	RL1951
L680	680 μ H	415-0928	PE-52629	RL1950
H330	330 μ H	430-0635	PE-53117	RL1962
H470	470 μ H	430-0634	PE-53118	RL1961
H680	680 μ H	415-0935	PE-53119	RL1960
H100	1000 μ H	415-0934	PE-53120	RL1959

data sheets of their earlier LT1070 family of boost converters. The positive-to-negative converter topology is a good example (Fig. 3a).

The inductor in the positive-to-negative converter circuit is a Pulse Engineering model number PE-92114. According to Linear Technology, the input filter capacitor is only required if the filter capacitor for the raw dc feeding the LT1074 is more than 4 in. away from it, a situation encountered in distributed power applications. Unlike the simple positive buck converter that requires a mini-

mum supply voltage of 8 V, the chip works in this topology from as little as 4.5 V, thanks to a self-boot circuit.

As shown with a -5-V output set by the 2.61- and 2.26-k Ω resistors, the circuit supplies 1.5 A from a +5-V power source, and 3 A from a 15-V source. The negative output voltage can be as low as -3 V from a +4.5-V supply, and as high as the voltage rating of the chip. As with the LT1070 converters, the basic device is rated at 45 V, but there are 60-V versions, too. A simple modification of our positive-to-negative converter topology creates a negative-boost converter (Fig. 3b). Set for -15 V out, it runs with supply voltages between -4.5 and -15 V, which gives you 800 mA and 2.7 A, respectively.

You've seen some typical circuits. Now you want to know what these devices look like. The LM2575 in a TO-220 package takes up minimal space on a memory system pc board. Although it's in a heat-sinkable package, in many applications (such as the one shown) a heat sink isn't required. And there's enough free space on the board to fit in voltage-setting resistors for the adjustable units.

A TO-3 package will take up additional space, as will the 11-pin LT1074, particularly because it uses additional parts. The Linear Technology and the National buck converters are available in TO-3 and TO-220 packages and have different pinouts making them noninterchangeable. □

PRICE AND AVAILABILITY

National Semiconductor's LM2575-5 (5-V output buck regulator) in a TO-220 package cost \$2.75 each in quantities of 100. Small quantities are available from stock. A design kit is also available, containing a similarly packaged LM2575-5, an inductor, a catch diode, and a data sheet. The -5-V version in a TO-3 package, and the 12-V, 15-V, and adjustable-output voltage versions, as well as the LM2577 boost regulator (in its various versions) will be available over the next six to eight months. The LM2577 should cost \$5 each in quantities of 100.

Linear Technology's LT1074 in a TO-220 package costs \$5.25 each in quantities of 100. Samples are now available.

National Semiconductor Inc., 2900 Semiconductor Dr., Santa Clara, CA 95051; Hugh Wright (408) 721-5856.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035; (800) 637-5545. CIRCLE 513

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UV385 Series/85W	TABLETOP 30W,40W
*CUSTOM DESIGN	

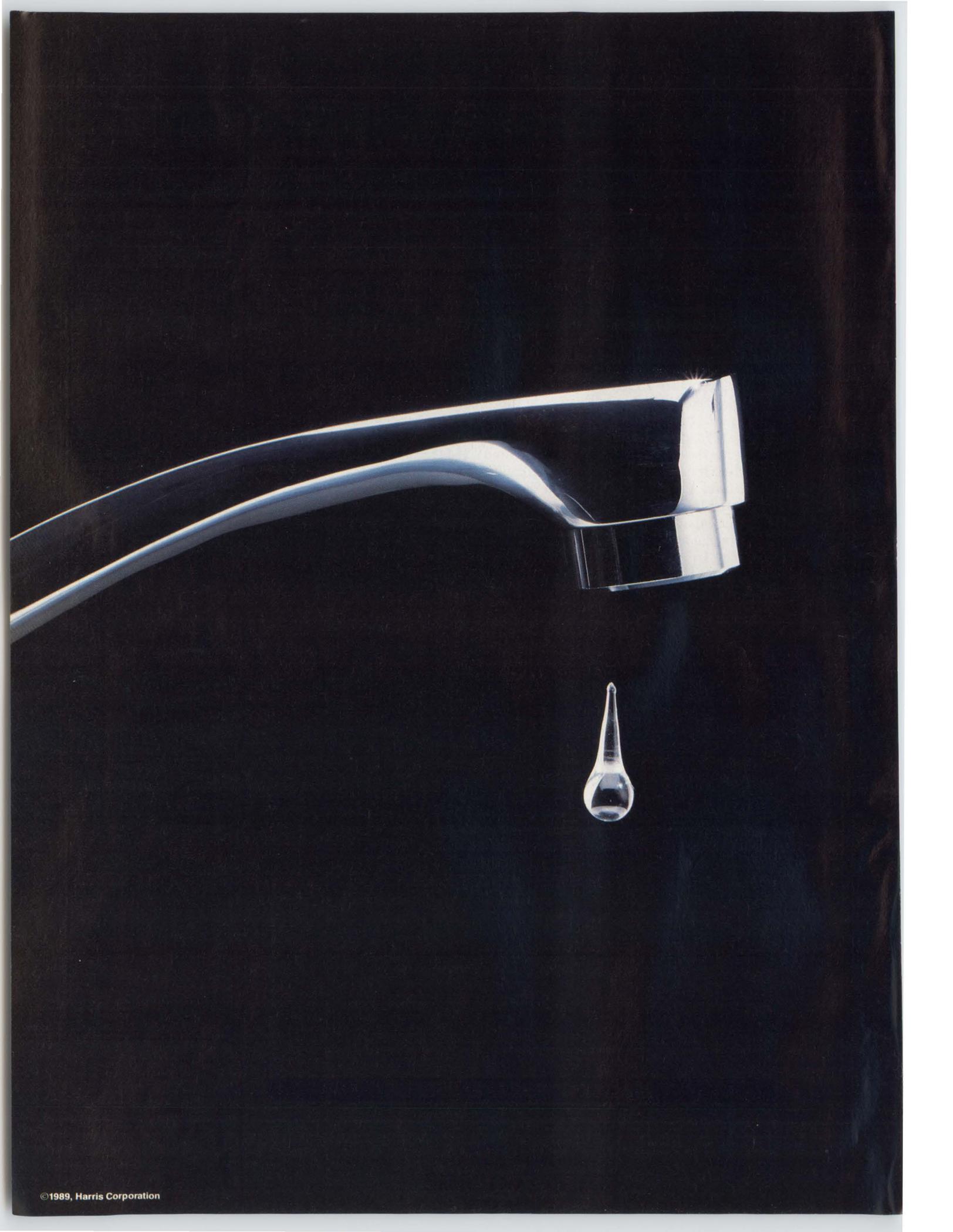
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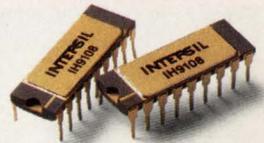
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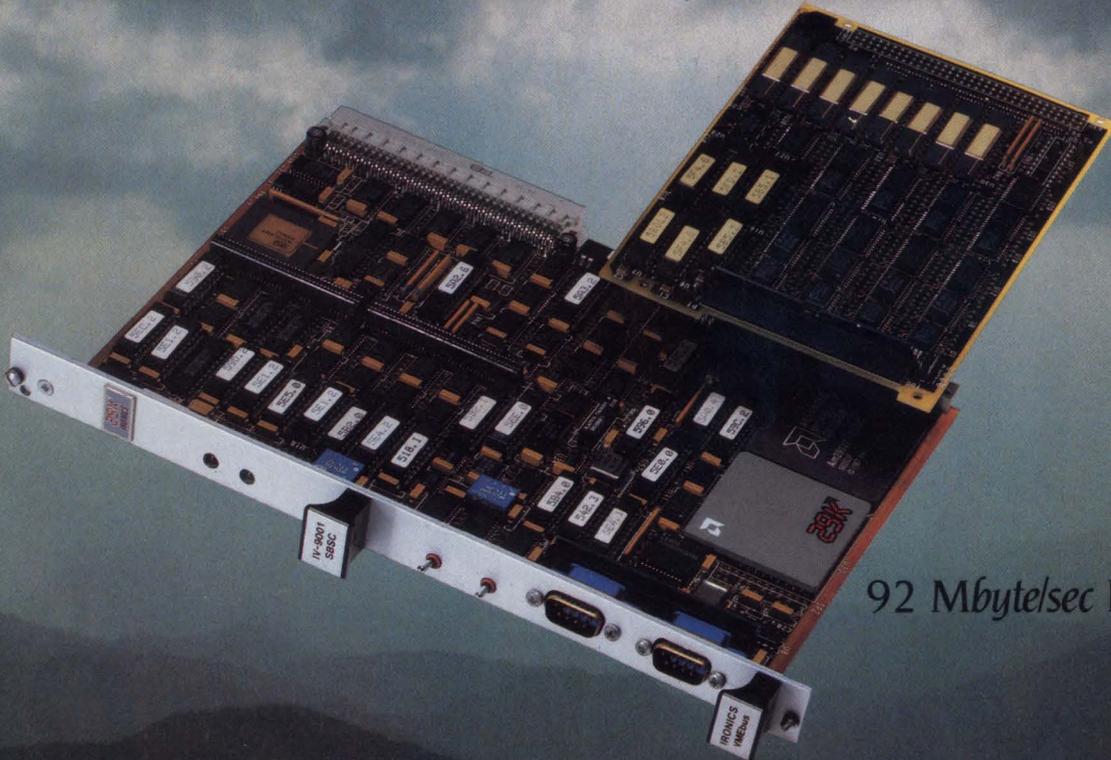


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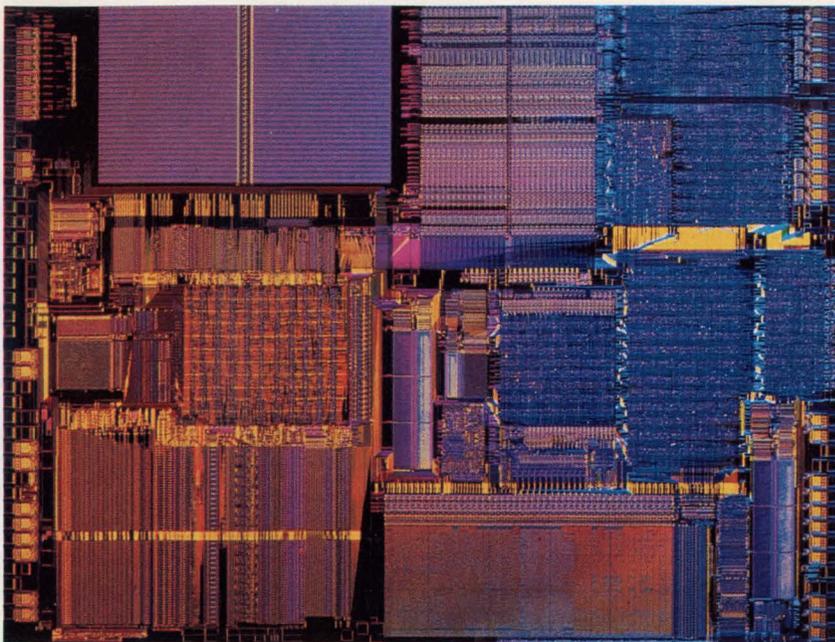
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ADVANCED CISC PROCESSORS CATCH UP TO RISC SPEEDS

The 32-bit complex-instruction-set (CISC) processors that dominate desktop, minicomputer, file-server, and embedded applications are facing an onslaught of competition from various reduced-instruction-set (RISC) processor chips. So far, the main de-

fense that CISC-based systems have against the faster RISC chips is the large CISC software base. The billion-dollar-plus software base that's established for the two most popular CPU architectures—the Intel iAPX80X86 and the Motorola MC680X0—and the cost of work required to translate those programs to run on another CPU type are two roadblocks that must be removed for RISC chips to gain ground.

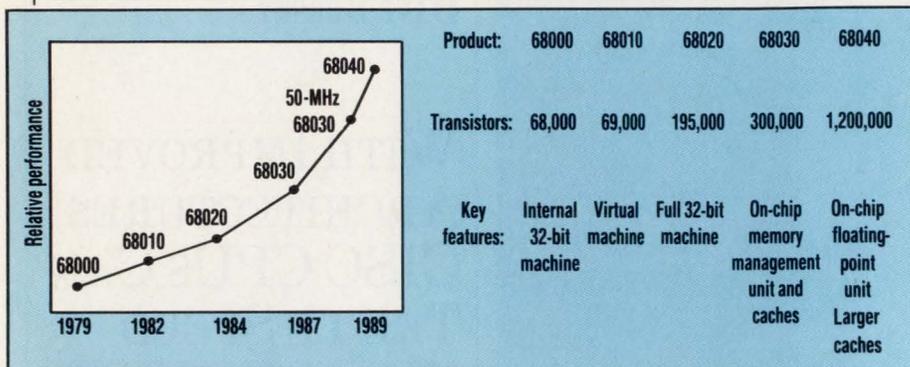
For embedded applications, such

as a graphics controller, laser-printer engine, robotics system controller, and many others, the CISC processors are losing ground to the RISC chips for new design wins. That loss of dominion is caused by two main factors: First, in most cases, the RISC chips are faster, typically offering throughputs of 8 to 17 MIPS vs. 3 to 7 MIPS for available CISC chips. Second, there are no pre-existing application software packages for the CISC chips that can be leveraged against the RISC solution since most embedded systems require custom software (see "32-bit CISC controllers", p. 44).

The latest CISC processors are now striking back. Recent advances in CISC architectures that take advantage of RISC concept developments will make it possible for the pending 32-bit CISC processors to challenge current RISC CPUs. For example, two recently unveiled CISC CPUs—the Intel 80486 and the Motorola 68040—have somewhat similar high levels of performance, with estimated throughputs for either chip in the range of 12 to 16 MIPS. That level of throughput is close to what current RISC chips can deliver. There's also the advantage that CISC CPUs can run all the software written for the previous generation.

To advance the iAPX-86 architecture further, Intel and Prime Computer Inc., Natick, Mass., have teamed up to develop a multichip ECL version of the 80486 that can deliver an eight-fold improvement in throughput. This will bring the

ADVANCED 32-BIT PROCESSORS



1. OVER THE LAST decade, the progression in chip complexity and performance has followed this exponential curve. Motorola created the curve, tracking the development of its MC68000 family from inception to the latest implementation, the 68040.

80486's performance to over 100 MIPS. Intel will have the rights to sell board-level versions of the processor, which is due in 1992. In addition, Intel is defining its next-generation CMOS CPU, the 80586.

A multichip implementation of the M68000 processor has already been done by Edgecore Technology. Their E2000 board-level implementation of the processor employs five custom chips that basically duplicate the data path of the MC68000 microprocessor. Built on VMEbus boards, the E2000 delivers a RISC-like sustained throughput of 16 MIPS (22 MIPS peak) as it executes all M68000 commands. A quad processor version offers a sustained throughput of 55 MIPS (88 MIPS peak).

Though Intel and Motorola control most of the CPU market for desktop PCs and workstations, Fairchild (now Intergraph), National Semiconductor, and Zilog tried to challenge those two by offering alternative processors for those applications. Unfortunately, these companies met strong resistance in the workstation and PC markets. Today, National has recast its 32000 family to tackle embedded control. Intergraph uses the Clipper family in its own workstation family, but the processors have seen limited use in other systems. And Zilog has focused its Z80,000 design efforts at embedded military systems that want to upgrade from the 16-bit Z8000 family.

In terms of its architecture, the Clipper falls between RISC and CISC technologies because its in-

struction set contains aspects of both. However, it's most often categorized as a RISC processor because many of its single-cycle instructions are hardwired for fast execution (*for more about the Clipper chip set, see "RISC Processors" ELECTRONIC DESIGN, June 8, p. 33*).

To challenge the dominance that Intel gained in the desktop PC market, a startup company, Nexgen, has begun to develop a multichip set that will run all operation codes of the 80386/80387 CPU and math coprocessors. Nexgen estimates that its chip set will run at throughput rates higher than the 80486. Initially, the company proposes to use the chip set as the heart of some system-level products they plan to release in early 1990, but the chips won't be sold.

To challenge the U.S.-based chip makers, Fujitsu, Hitachi, Mitsubishi, and Oki are developing a family of alternate-sourced 32-bit CISC processors as part of the Japanese TRON (The Real-Time Operating System Nucleus) project. Oki recently joined the group and will focus on developing a core cell for custom CPU chips. Other TRON group members are working on additional CISC CPUs: Toshiba has defined two chips for embedded applications—the TX-1 and TX-3—and Matsushita Electric defined a general-purpose TRON processor.

On its own, NEC developed advanced CISC processors for the high end of its V-series family. The V60, V70, and V80, have respective throughputs of 3, 8, and 12.5 MIPS

(at 25 MHz).

There's little activity with the 32-bit processor in Europe, except for some specialized military-sponsored research projects, and the continued efforts of Inmos to convince everyone of the benefits of its Transputer architecture. The latest Transputer version, the T800, packs an on-chip floating-point processor and 4 kbytes of cache RAM, as well as some serial communication ports. It can deliver a processing throughput of about 12 MIPS.

With greater than 80% of the CISC market owned by Intel and Motorola, both companies have fought to maintain their shares by evolving their CPU chips from a now seemingly humble beginning of 16 bits in the late 1970s. The Motorola 68000 family, for example, started in 1979 with the introduction of the 68000, which had an external 16-bit data bus. But internally it had a 32-bit arithmetic unit and used 32-bit buses to move data around the chip. As the family evolved through the 68010 and up to the 68020, the transistor count more than doubled from about 68,000 devices to about 195,000 for the full 32-bit CPU with virtual memory support (*Fig. 1*). Higher integration levels continued with the 68030, which added about 105,000 more transistors in the form of on-chip memory management and dual 256-byte caches to speed execution.

Not only has Motorola added more features to speed up execution, but they also fine-tuned the instructions so that many of them execute in fewer clock cycles than in previous generation versions. In addition, improved processing makes it possible to run the chips at higher clock frequencies. Nearly a 300% throughput improvement is possible on the 68030 alone, thanks to a boost of the clock rate from its original 16.67 MHz to the most recently released version, which runs at 50 MHz. Though not formally released, the 68040 processor combines all of the 68030 features with another 900,000 transistors that are used for greatly enlarged caches (4 kbytes each), an on-chip floating-point coprocessor, and bus-monitoring circuitry for multi-

ADVANCED 32-BIT PROCESSORS

processor systems.

A similar scenario has taken place with Intel's iAPX-86 family—its evolution from the 8086, 80286, and 80386 has followed a similar path, with the 80386 containing about 300,000 transistors, and the forthcoming 80486 packing about 1.2 million devices (*Fig. 2*). As Motorola and Intel's designers strive to achieve higher CISC performance, a natural evolution seems to be taking place that's causing both company's chip architectures to converge.

Both chips incorporate floating-point coprocessors and cache subsystems. The only major architectural difference is one 8-kbyte cache for data and instructions for the 80486, whereas the 68040 has split the cache into separate data and instruction caches to achieve a little more parallelism. In addition, both chips turn many instructions into single-cycle commands, improving their MIPS ratings while minimizing program

execution time.

Burst modes to reload the cache and to quickly transfer data between the processor chip and off-chip memory are also included in the 68040 and 80486. On the 80486, for example, a burst bus transfer of 106 Mbytes/s is possible with the processor running at 33 MHz.

To tackle a software-compatible multichip implementation that runs faster than the 80486, Nexgen started with a thorough analysis of CMOS processing technology and typical processor architectures. This analysis enabled them to obtain a sharp estimate of the expected system performance. The company developed a formula that made it possible for them to estimate on-chip machine cycle time, and a second formula that helps estimate the chip-to-chip machine cycle times:

$$Tmc1 = Ng(Tpd + L * Tic) + (Tsu + Tcko) + Tck-skew$$

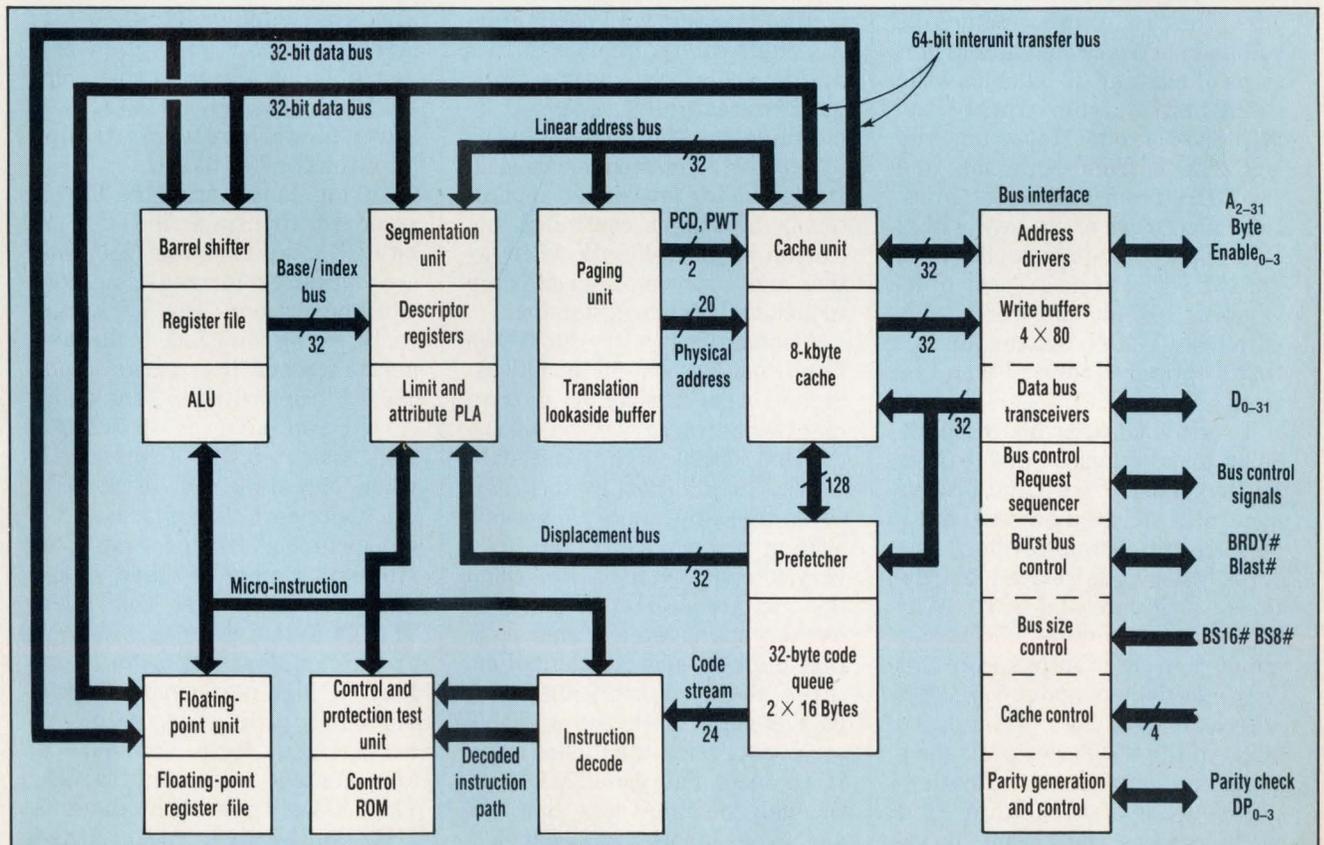
$$Tmc2 = (Tobf + Lb * Tbic) + Tbif +$$

$$Tbck-skew + (Tsu + Tcko) + Ng2(Tpd + L * Tic).$$

In the first equation, $Tmc1$ is the on-chip machine cycle time in nanoseconds, Ng is the number of gating levels in the combinatorial block within the chip, Tpd is the propagation delay per internal gate level, L is the on-chip interconnect net length, and Tic is the on-chip delay per unit length of interconnection. Additional terms in the equation include Tsu , the latch set-up time, $Tcko$ the latch clock-to-output delay, and $Tck-skew$ the on-chip clock skew.

In the second equation, $Tmc2$ is the chip-to-chip machine cycle time, $Tobf$ is the output buffer delay, $Tbif$ is the input buffer delay, Lb is the average board interconnect net length, $Tbic$ is the interchip interconnect delay per unit length, $Tbck-skew$ is the board-level clock skew, and $Ng2$ is the number of gate levels between an output buffer and an input buffer.

Some reasonable assumptions for



2. INTEL'S LATEST 32-BIT OFFERING, the 80486, contains virtually an entire system on chip. It packs the floating-point processor, 8 kbytes of cache memory, the cache memory manager for second-tier off-chip cache control, bus-snooping circuitry to ensure cache coherency in multiprocessor systems, and a paged virtual-memory management unit.

ADVANCED 32-BIT PROCESSORS

a single-chip processor may include about 10 levels of gates within the chip, an average gate delay of 1 ns, a typical wire length of 1000 μm , a loading factor of 0.7 ps/ μm , a latch set-up time and a clock-to-output time of 2 ns, and a clock skew of 1 ns. With those assumptions plugged into the first equation, a 1- μm CMOS process could deliver a circuit with

an on-chip cycle time of 22 ns. Assuming multiple chips can be tied together without external logic, N_{g2} would be zero, the output buffer delay may be about 2.5 ns, the average board wire length might be 25 cm, the wire loading factor could be 100 ps/cm, the input buffer delay might be 2 ns, and the board clock skew might be about 2 ns. With those val-

ues, the chip-to-chip signals need about 13 ns to cross the board.

Because a memory access requires that signals propagate in both directions across a bus, the minimum machine cycle time must be twice the T_{mc2} delay, or 26 ns. This tells the designers that the fastest running time for the processor is close to 40 MIPS, assuming all instructions exe-

32-BIT CISC CONTROLLERS

For certain classes of applications, a general-purpose microprocessor—even if it uses 32-bit data paths—is often underpowered to handle application-specific tasks. Such tasks include graphic manipulations and real-time control operations, such as counting and timing. To fill that market niche, Intel, Motorola, National Semiconductor, Philips-Signetics, and Toshiba introduced control-optimized versions of 32-bit processors. The first four companies developed software-compatible versions of existing 32-bit chips—the iAPX-80376 from Intel, the MC68332 from Motorola, the NS32GX32 from National, and the 68070 from Philips-Signetics. Intel also went on its own with a RISC-based 32-bit controller family, the 80960 series. Toshiba developed a 32-bit chip compatible with the TRON instruction set that's optimized for real-time systems.

To stay compatible with its 80386 instruction set, and to offer an inexpensive real-time processor, Intel stripped out the multitasking and virtual memory features, as well as related instructions, to create the 80376. The higher-performance 960 series employs a RISC-type processor that can deliver about 7.5 MIPS with a 20-MHz clock. Though the chips in the 960 series pack some cache memory and a floating-point processor capable of 4 MWhetstones and 15,000 Dhrystones, they don't carry any application-specific circuits to imple-

ment functions such as serial ports, counters, and so forth.

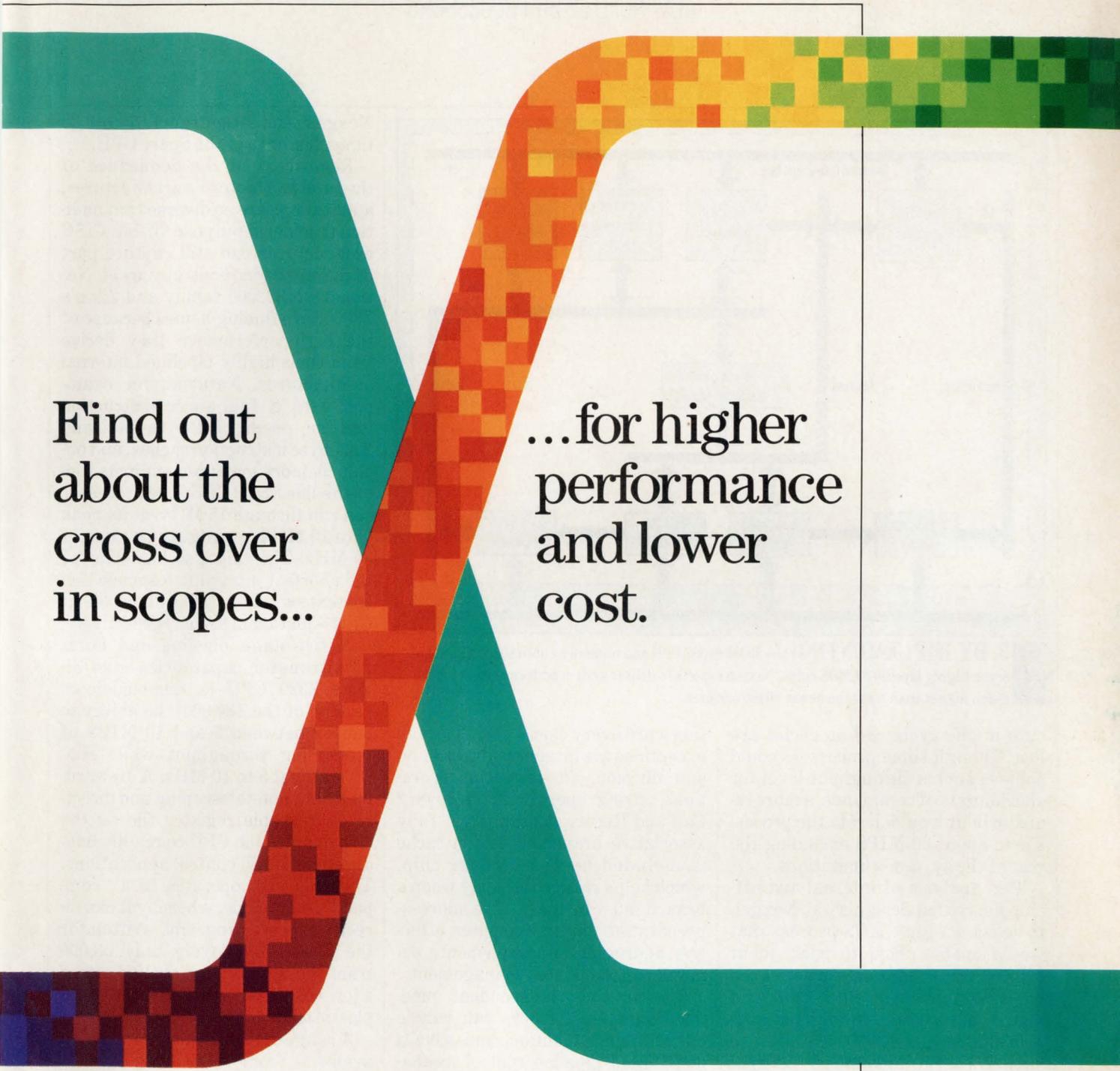
Motorola did some extensive rearchitecting of its 680X0 family to create the 68332, which packs the CPU core of a 68020 and an 8-MIPS instruction throughput. The chip also contains a complex and flexible timing processor with 16 timing channels, 2 kbytes of static RAM, a queued serial communications subsystem and a section that handles system protection, bus interfacing, and self-testing and software debugging. And, unlike most other CPUs that divide a high-frequency clock down to create all the internal timing functions, the 68332 multiplies up a 32-kHz low-frequency clock. Designed for low-power applications, the 132-pin controller chip consumes just 300 mW when active, and its power drain can drop to just 3 mW when in standby.

Also staying with the 68000-family instruction set, the Philips-Signetics 68070 gives designers a highly-integrated version of the original 68000 with 16-bit data buses. In addition to the CPU core, the chip contains various system resources that can build very compact systems. Packed on the chip are a 32-bit CPU core, a memory-management unit, a direct-memory-access controller, three 16-bit counter-timers, an RS-232 serial port, and a simple serial port using the Philips inter-IC protocol. Fabricated in CMOS, the chip consumes less than 1 W and comes in low-cost 84-pin plastic leaded chip carriers.

Optimized for laser-printer and

video applications, National's recently introduced NS32GX32 packs most of the features included in the general-purpose 32532 processor. But, the NS32GX32 also adds bit-block transfer logic to the chip to accelerate graphic operations, such as line-drawing primitives and bit-field instructions. Implemented in a 1.25- μm CMOS process, the chip can run at clock frequencies as high as 30 MHz and deliver throughputs up to 15 MIPS. On-chip data and instruction caches handle Postscript character generation and manipulation. Prior to this chip, National released the 32CG16, a lower-performance controller based on the 32016 CPU.

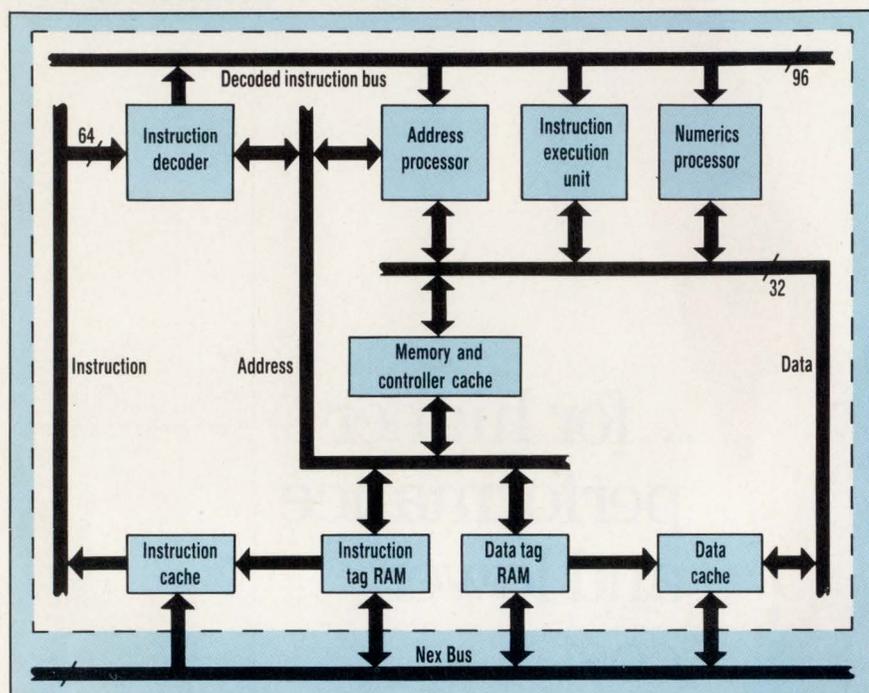
Taking its lead from the TRON standard, Toshiba defined two 32-bit CPUs, the TX-1 and TX-3, that are optimized for real-time control applications. The TX-1, currently being sampled, is an integer processor that packs about 450,000 transistors and can deliver a throughput of 12.5 MIPS peak (about 5 MIPS sustained) when operating with a 25-MHz clock. Support chips for the TX-1 will include a clock generator, an interrupt controller-timer, and a direct-memory-access controller. The TX-3, due in 1990, will pack about 1 million transistors that form a high-performance floating-point processor, memory-management logic, and dual 8-kbyte instruction and data caches. The TX-3 will operate at about 33 MHz and deliver a sustained throughput of about 10 MIPS (33 MIPS peak).



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ADVANCED 32-BIT PROCESSORS



3. BY IMPLEMENTING the 80386-80387 CPU and numerics coprocessor as a set of seven highly pipelined CMOS chips, Nexgen expects to deliver system performance that's much higher than what the newer 80486 achieves.

ecute in one cycle and no cycles are lost. Though some processors could achieve such a throughput level for short bursts of commands, a more realistic limit would derate the processor to about 30 MIPS excluding the rest of the system's limitations.

This analysis of internal and off-chip delays led designers at Nexgen to select a 1- μ m CMOS process that would enable them to pack about 300,000 transistors on each of seven chips to implement their CPU and math coprocessor. Additional off-chip high-speed RAMs are used to supply a large amount of external cache. The company took the 80386 and 80387 operation codes and developed a pipelined architecture split among seven chips that will sustain an execution rate of one cycle per instruction (Fig. 3). The seven chips defined by Nexgen include an instruction decoder, an address preparation unit, the integer execution unit, a memory and cache controller, both data and instruction cache-tag RAMs, and the numerics processor.

Incoming instructions are handled by the instruction decoder chip and assembled into a 96-bit microinstruc-

tion word every clock cycle. The only exceptions are integer multiplication and division, floating-point operations, string operations, and OS/2 Call and Return operations. A fully associative branch-prediction cache is included on the decoder chip, which helps reduce the delay when a branch must be taken. The address-preparation circuit computes effective addresses and implements demand-paged memory management.

The multiple, independent, pipelined functional blocks can handle out-of-order execution, and have a distributed pipeline control mechanism that performs dynamic re-scheduling, register reassignment, and instruction tagging. Thanks to pipelining, the processor can back up as many as seven instructions to restart a procedure. When Nexgen compared the Sun Sparc RISC processor to its own chip set using hand-coded sequences from the popular Sieve (inner loop) and Dhrystone (Func 1, Proc 8, and string copy) as benchmarks for both chips, they found that the code size for the Sparc was 1.73 to 7.6 times longer, depending on the sequence, and that the

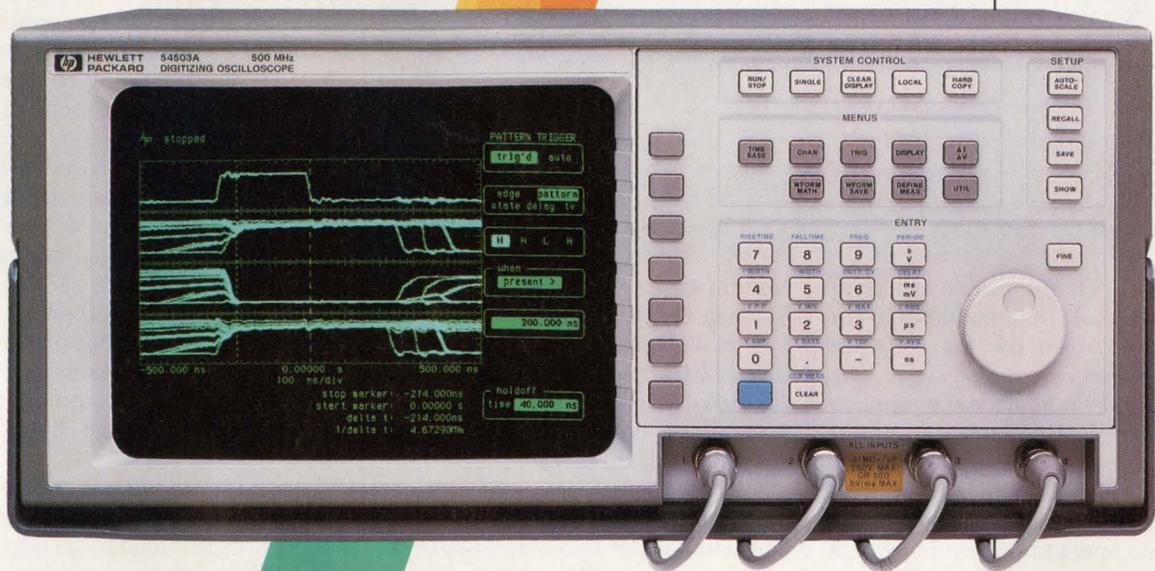
Nexgen simulation ran 1.67 to 3.25 times faster than the Sparc CPU.

Regardless of the dominance of the Intel and Motorola architectures, applications are so diverse that additional general-purpose 32-bit CISC architectures can still capture part of the embedded control market. National's NS32000 family and Zilog's Z80000 are finding homes because of the high-performance they derive from their highly pipelined internal architectures. National, for example, uses a four-stage instruction pipeline, on-chip 512-byte data and 1024-byte instruction caches, and on-chip memory management in its top-of-the-line 32532 CPU. The processor can run through 15 MIPS at its peak (8 to 10 MIPS average) at a clock of 30 MHz. The chip also has some of the shortest interrupt response and context switching times of any 32-bit CPU—just 1 and 3.6 μ s, respectively.

A five-stage pipeline and burst data-transfer capabilities give Zilog's Z320 CPU (a trimmed-down version of the Z80,000) the ability to deliver between 5 and 10 MIPS of processing throughput while running at just 8 to 10 MHz. A 16-word-by-32-bit, non-telescoping and directly addressable register file on the chip enables the CPU to readily handle some tough control applications. The chip also operates in a "compact" 16-bit mode, whereby it can directly execute programs written for the Z8000. Employing only 93,000 transistors, the compact CPU offers a low-cost 32-bit solution in a 68-lead plastic leaded chip carrier.

A range of 32-bit processors is also available from NEC—they have a trio of chips: the V60, 70, and 80 (the μ PD70616, 70632, and 70832, respectively), which deliver throughputs that begin at 2 MIPS and currently peak at about 12.5 MIPS. All three chips have a proprietary instruction set, unlike their 16-bit predecessors that implemented an extension to Intel's 8086 instruction set. The V60 is somewhat similar to Intel's 80386SX reduced-bus version of the 80386. The V60 contains a full 32-bit CPU with MMU, IEEE-compatible floating-point math capability, and a 16-bit data-bus interface (and 24-bit ad-

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dress bus). The chip also packs an emulation mode that enables it to run software written for the V20 and V30 microprocessors.

For higher-performance applications, the V70 processor encompasses all the features of the V60 and extends both the data and address buses to 32 bits. It also boosts the maximum operating frequency to 20 MHz to achieve a throughput of about 6 MIPS. An improved bus-timing scheme empowers the processor to transfer up to 40 Mbytes/s over the bus when operating at 20 MHz.

Adding both 1-kbyte data and 1-kbyte instruction caches to the V70, the latest member of NEC's family, the V80, employs a six-stage pipeline, similar to the pipeline in the V70, to achieve a large amount of internal parallelism. Also contained on the chip is a branch-prediction unit that can improve the system throughput by trying to predetermine whether the program will or will not take a program branch. When running at 25 MHz, the processor will deliver a throughput of 12.5 MIPS. Future versions will push the clock speed up to 33 MHz, which should move the chip's throughput past 16 MIPS.

A trio of processors has also emerged from a joint collaboration of Fujitsu, Hitachi, and Mitsubishi, though only the mid-range unit has been sampled to date. The General Micro family, better known as Gmicro/100, /200, and /300, will initially

contain three CPUs, one developed by each company. All three companies will then alternate-source all three CPUs, so each company can offer three performance-price points. A common core instruction set is shared by all three CPUs. The more advanced processors, such as the /200 and /300, augment the core with additional instructions and features.

The simplest CPU is the forthcoming chip from Mitsubishi, the Gmicro/100, which should have a throughput of about 3 MIPS and serve as a core processor in application-specific chips and in price-sensitive TRON systems. Though the TRON CPU will be the simplest, it still packs a five-level pipeline, branch prediction, and two protection rings. However, the chip won't have any instruction, data, or stack cache memories, or a math coprocessor interface.

For more complex applications, the /200 developed by Hitachi adds a sixth pipeline level, memory management, a 1-kbyte instruction cache, a 128-byte stack cache, a 4-entry branch window, and a 32-entry translation-lookaside buffer. Also included is an interface for an off-chip floating-point processor. Benchmark tests were run on samples of the chip, and based on those tests, the chip was given a throughput rating of 6 to 8 MIPS.

The /300 can handle even more demanding applications. This chip, be-

ing developed by Fujitsu, might be ready to sample in early 1990, and should deliver about double the throughput of the /200. To achieve the higher performance, the /300 boosts both the instruction and data cache sizes up to 2 kbytes and doubles the translation lookaside buffer.

As with all microprocessors, a system can't be built without a family of support chips, and the Gmicro series will sport a half-dozen support chips to simplify system design. These include a floating-point coprocessor, an interrupt-request controller, a DMA controller, a cache-tag memory, a cache controller and memory, and a clock-pulse generator. The floating-point unit can deliver a single-precision addition, subtraction, or multiplication in 500 ns (when running at 20 MHz) and supports graphics applications with dot-product and 3D clipping computations. All of the chips except for the floating-point coprocessor are already being sampled.

Seven interrupts are available on the interrupt-request controller that can be programmed to tie into either the VMEbus or the local bus of the Gmicro/200. Multiple controllers can be cascaded if over seven interrupts are needed. For high-speed data transfers, the DMA controller ships data over the buses at up to 27 Mbytes/s (at 20 MHz) on up to four independently-programmable channels. For the processors to operate at maximum speed, a cache-tag RAM, organized as 512 words by 98 bits, stores the tags for either a 512-entry four-way or a 1024-entry two-way set-associative cache and implements a least-recently used replacement algorithm. Packing the cache memory, the cache controller chip holds 16 kbytes of RAM and implements a 4-way set associative cache that is organized as 1024 16-word entries. Lastly, the clock generator supplies the timing for all the chips and synchronizes their operations. □

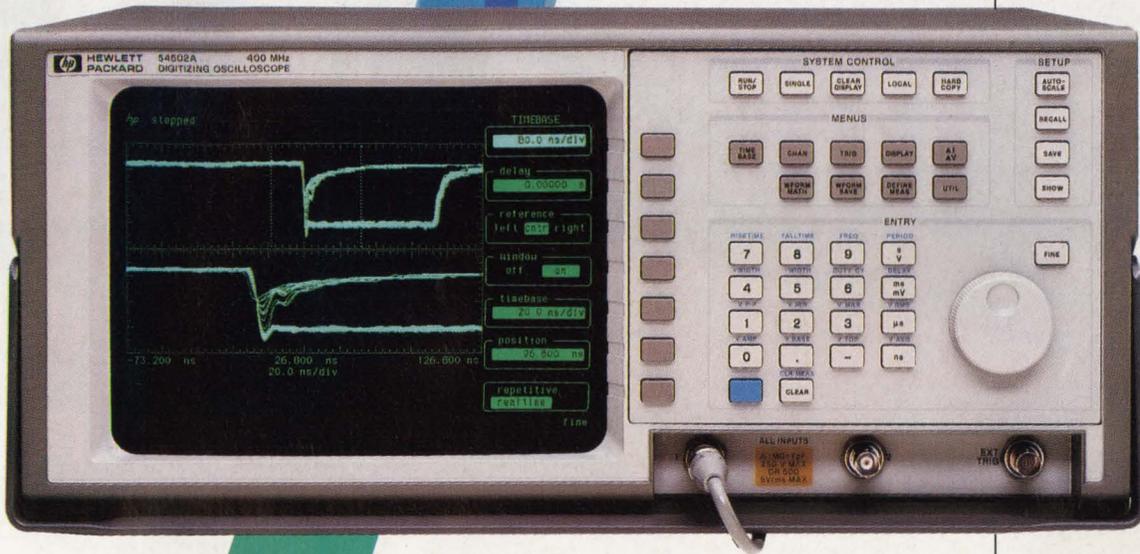
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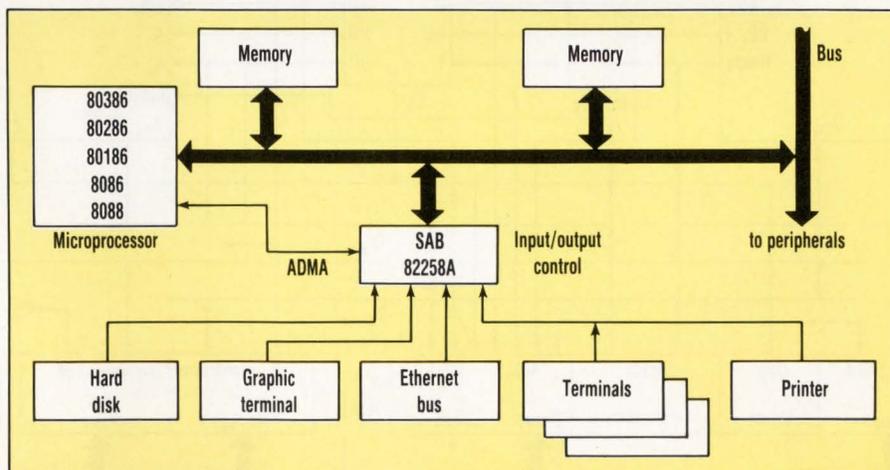
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DMA CONTROLLER MATCHES FAST CPUs TO SLOW PERIPHERALS

EXPLOITING THE FULL POTENTIAL OF A 32-BIT PROCESSOR CALLS FOR A FAST DMA CONTROLLER WITH LOTS OF FLEXIBILITY.

A high-performance system designed with a super-fast microprocessor, but lacking a fast direct memory access (DMA) controller, is comparable to a custom car designed with a Ferrari engine and a Yugo transmission. The DMA controller is critical when bridging the high-speed CPU to slower I/O devices. Microprocessor-based systems without DMA capability must pass transferred data through the CPU. Normally, the CPU would execute an instruction sequence for inputting, outputting, and tracking each byte or word in the transferred data block. This method's main



1. THE 82258A advanced DMA controller can simultaneously drive three high-speed peripherals and a cluster of slow equipment in systems hosted by a fast 8-, 16-, or 32-bit CPU.

VIJAY DESAI

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DMA CONTROLLER

disadvantage is slow data transfers that come from the consumption of extra CPU clock cycles. Throughput is further limited by long response time or by the startup time for the first byte transfer. This results from I/O devices that typically send an interrupt signal to the CPU to indicate readiness, followed by execution of the CPU's interrupt service routine prior to the first byte's transfer.

To resolve this problem, DMA controllers typically manage high-speed data transfers between system memory and I/O without CPU intervention. Some DMA controllers can also perform other transfer types that are usually done by the CPU. One such device is the SAB 82258A advanced DMA controller (ADMA), a VLSI coprocessor that supports

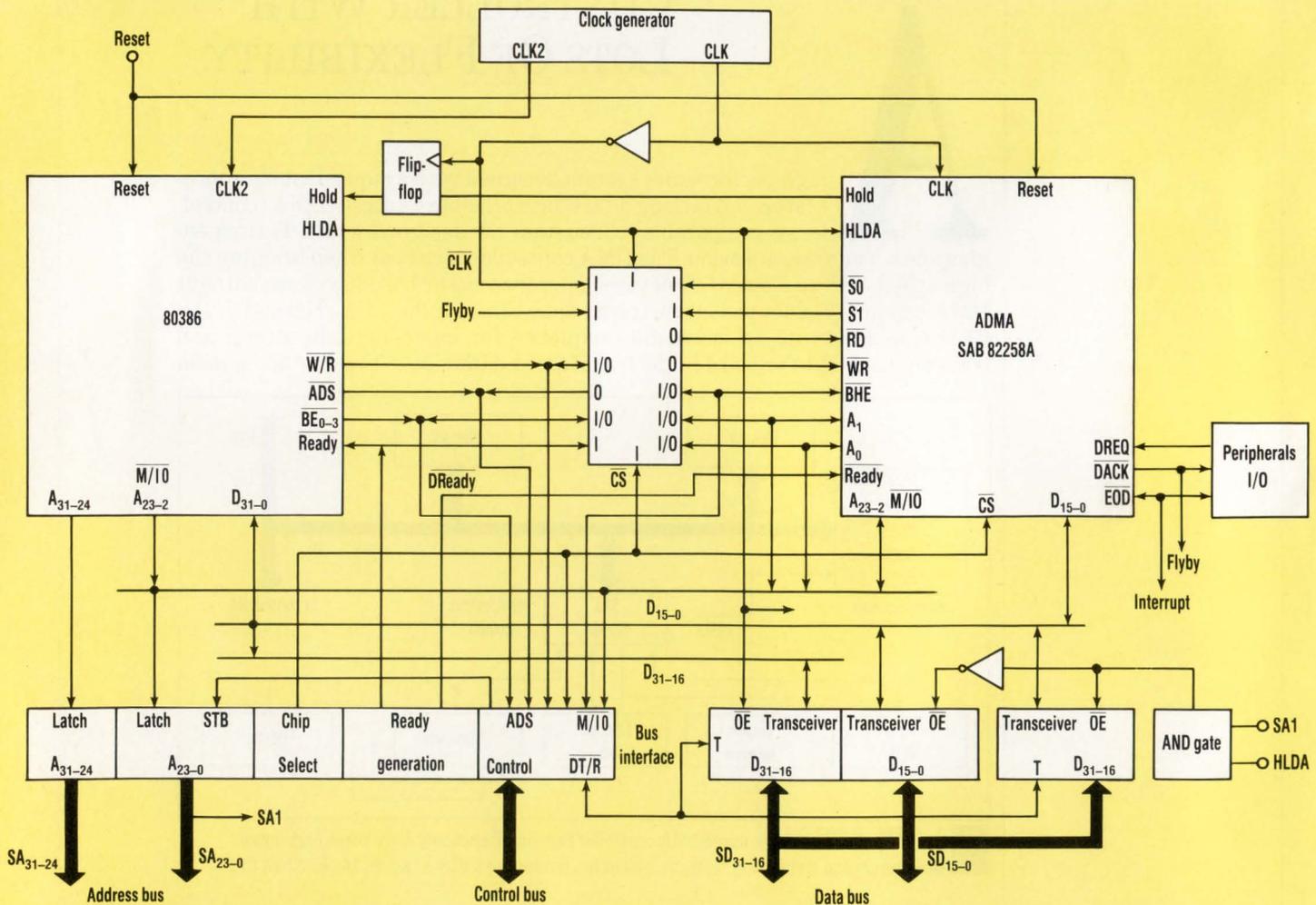
both a 20 Mbyte/s data throughput and the sophisticated functions of 32-bit machines, such as the 80386, 68020, and 68030 microprocessors (Fig. 1). An adaptive bus interface also facilitates connection to all 8- or 16-bit microprocessors, from the 8088 up to the 80286, without any interface logic.

The 82258A has two basic modes of operation. In the remote mode, the coprocessor operates as a stand-alone controller with a resident bus and interfaces to the processor through the system bus. The local mode enables the controller to be close-coupled to the CPU and share the same local bus (Fig. 2). External logic that consists of just one PAL and one flip-flop matches the timing and functionality of the controller's

bus control signals to those of the host processor, which in this case is the 80386.

80386 bus cycles are twice as fast as those of the 82258A, therefore the 80386 is supplied with a clock frequency (CLK 2) that's twice the controller's 20-MHz clock (Fig. 3). The Hold and Hold Acknowledge (HLDA) pins on the 80386 and controller transfer bus control between the two parts. When the controller needs bus access, it asserts a Hold Request signal, which is synchronized to Clock by an edge-triggered flip-flop to satisfy the synchronous setup-and-hold time requirement of the 80386.

The controller's data port (D_{15-0}) connects to the low-order half of the 32-bit local bus. A connection to the



2. IN LOCAL CONFIGURATION with the 80386 32-bit microprocessor, the 82258A shares the same local bus. An external flip-flop and PAL implement the logic that resolves the timing differences between the two parts.

DMA CONTROLLER

high-order half of the microprocessor's data port (D_{31-16}) is unnecessary, because the 80386 uses only 16-bit transfers when it accesses the controller's registers.

The connection to the system bus is different. To support both 8- and 16-bit transfers on a 32-bit system data bus, the controller's 16 data pins must connect to both halves of the bus (SD_{15-0} and SD_{31-16}). To write data from the controller to a system device, the transceivers that duplicate these data-line connections are always enabled. Only half of the data bus transceivers are enabled when data is read from the controller. These transceivers are controlled by address bit SA1 to the AND gate associated with them (Fig. 2, again).

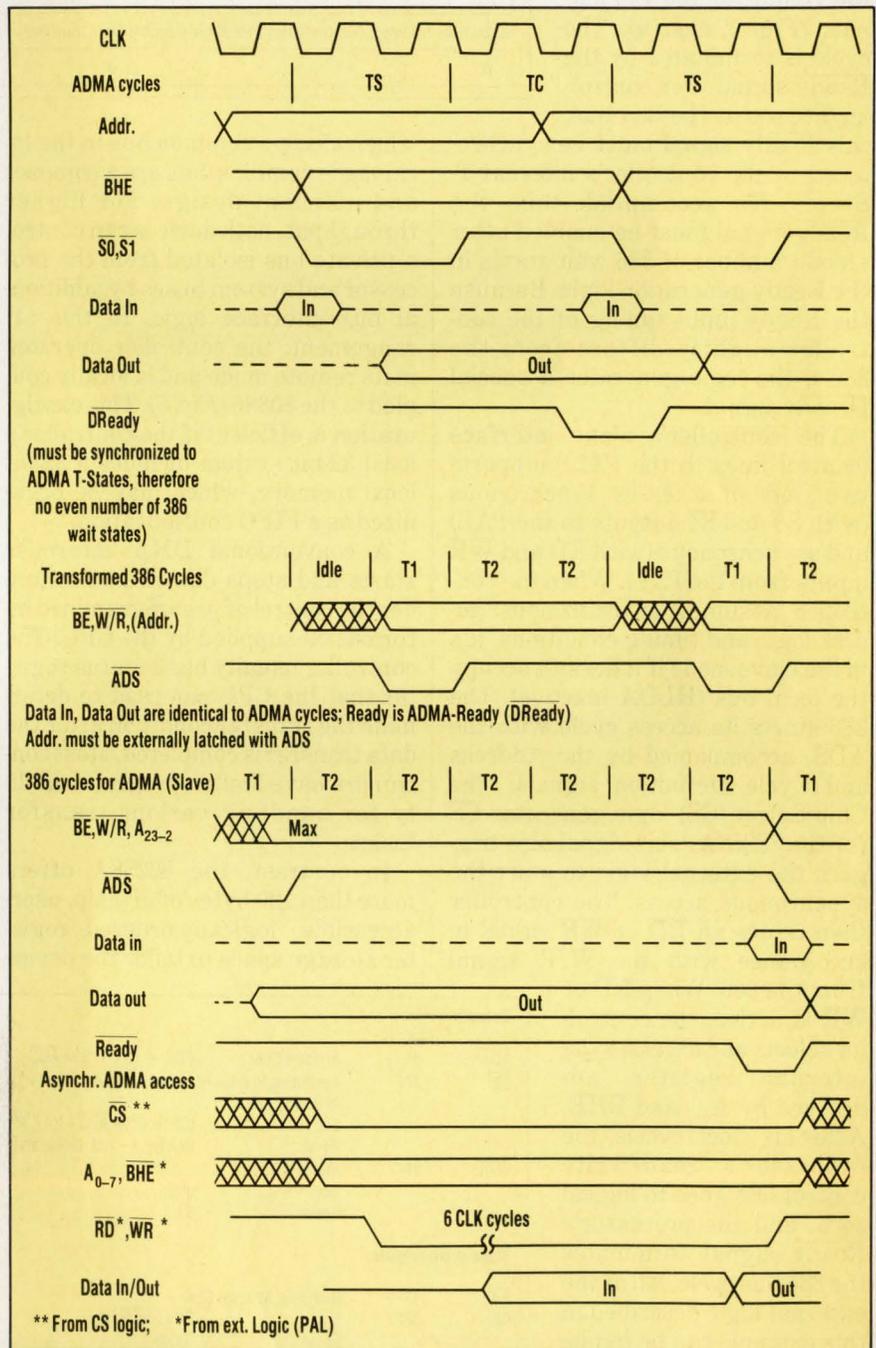
The transceivers are generally controlled for read direction during a 32-bit transfer executed by the controller. The controller's data port isn't influenced by 32-bit transfers, which are always flyby (single-cycle) transfers. The controller's data pins only need both the low and high-order 16-bit parts of double words during coincident data comparisons executed in on-the-fly operations. A 32-bit flyby data transfer indication is simply a Data Acknowledge (DACK) signal sent from the controller to a peripheral in a channel that is executing the 32-bit transfer. It's also possible to dynamically change a channel's transfer mode by using the controller's general mode register. In this case, either the Memory I/O (M/I/O) signal or a high-order address bit could also be sampled for detecting 32-bit flyby transfers.

The 82258A is designed to interface directly with the 16-bit 80286 microprocessor. However, external logic is required for use with the 32-bit 80386. For example, low-order address lines A_0 and A_1 and a BHE (Bus High Enable) signal are necessary to access both the controller and all 8- and 16-bit peripherals. Though the 80386 address bus doesn't offer these signals, its four BE (Byte Enable) signals can be transformed as needed by a PAL (see the table, p. 54). When an 80386 accesses the controller or peripherals, the PAL transforms all BE signals to A_0 , A_1 , and

BHE. Conversely, when the controller accesses the 32-bit memory or other 32-bit subsystems, the PAL transforms signals on its A_0 , A_1 , and BHE lines to BE signals.

The controller initiates bus cycles by issuing status signals $\overline{S0}$ and $\overline{S1}$. Because of the pipelined bus timing,

address outputs are issued in advance. Therefore, external address latching is necessary for all controller cycles and pipelined 386 cycles. Strobing is done with the ADS signal (Address Status). The PAL derives this signal from the controller's status signals that are synchronized



3. CONTROLLER ACCESS TO THE 386 BUS requires the Ready signal to be synchronized to the controller's internal T-States. The Ready input timing of the controller differs from the 386's, consequently the external logic generates a special \overline{DReady} signal by enabling the Ready signal after an odd number of 386 wait states.

DMA CONTROLLER

with the clock. The \overline{ADS} signal is generally used on the 386 local bus to indicate the start of a bus cycle. The $\overline{W/R}$ signal (Write/Read operation) is also generated from the $\overline{S0}$ and $\overline{S1}$ signals, but also with the timing of the \overline{BE} signals (Fig. 3, again). The cycle is terminated by the \overline{Ready} signal. For controller access to the 386 bus, this \overline{Ready} signal must be synchronized to the controller's internal T-States. To accomplish this, the \overline{Ready} signal must be enabled after an odd number of 386 wait states in the \overline{Ready} generation logic. Because the \overline{Ready} input timing of the controller slightly differs from the 386's, the logic generates a special \overline{Dready} signal.

The controller's slave interface (control lines to the PAL) supports two kinds of accesses: synchronous (with $\overline{S0}$ and $\overline{S1}$ outputs to the PAL) and asynchronous (with \overline{RD} and \overline{WR} inputs from the PAL). When the controller assumes asynchronous access logic and timing conditions, it's in the slave mode if it doesn't occupy the local bus (HLDA inactive). The 386 starts its access cycle with the \overline{ADS} , accompanied by the Address and Cycle Definition signals. The Chip Select (CS) logic generates \overline{CS} for the 82258A. This signal also triggers the external logic to start the synchronous access. The controller then issues an \overline{RD} or \overline{WR} signal in accordance with the $\overline{W/R}$ signal from the 386. When \overline{RD} or \overline{WR} is active, the controller selects and accesses the internal register addressed by A_{0-7} and \overline{BHE} . After six clock cycles, the processor's read/write control line goes to logical zero, and the processor's \overline{Ready} signal terminates the 386 bus cycle. All of the external logic described in this example can be implemented using one flip-flop and one properly programmed PAL (Fig. 4).

The 80386 and 82258A,

GENERATION OF 80386 SIGNALS

16/8-bit transfers (both directions)						
A1	\overline{BHE}	A0(BLE)	$\overline{BE3}$	$\overline{BE2}$	$\overline{BE1}$	$\overline{BE0}$
0	0	0	1	1	0	0
0	0	1	1	1	0	1
0	1	0	1	1	1	0
1	0	0	0	0	1	1
1	0	1	0	1	1	1
1	1	0	1	0	1	1

32-bit flyby transfers (supported only for aligned double-word transfers)						
0	0	0	0	0	0	0

which share a common bus in the local mode combination, are a compact and efficient design. For higher throughput, both devices can control a private bus isolated from the processor and system buses by additional bus interface logic. In this arrangement, the controller operates in its remote mode and is locally coupled to the 80386 (Fig. 5). This configuration is efficient if the controller's local 32-bit system includes a 32-bit local memory, which may be organized as a FIFO configuration.

A conventional DMA controller starts and stops data transfers under the control of preprogrammed information supplied by the CPU. The controller usually has a status register that the CPU can read to determine the transfer condition after the data transfer is completed. Most controllers have limited programmability for handling various transfer tasks.

In contrast, the 82258A offers more than 120 bytes of on-chip, user-accessible, logically-ordered register storage space to tailor the device

to numerous tasks and environments (Fig. 6). Unlike conventional controllers, CPU communication with the 82258A is also memory-based. The CPU generates a "command block" in memory, informs the controller of the memory location, and transmits a "start channel" command. The controller responds by loading the entire com-

mand block from memory into its on-chip channel registers and begins to execute the commands.

The CPU accesses just a few controller registers to control its activities. All registers, though, can be addressed for reading or writing: Consequently, all register states are always visible to users. The register states' transparency and variability are helpful during the debugging phase of system implementation.

Five general control registers define the overall environment of the DMA controller. Main system parameters are defined in the general mode register, which is programmed during system initialization. These parameters establish the controller in local mode with a 16-bit bus. This register also specifies several individual DMA channel parameters, including the type of data transfer (all two-cycle) and the mode of channel 3 (multiplexer). The channel priority can also be programmed in this register. For the multiplexer channel, the subchannels' priorities can be specified by programming a 8259 programmable interrupt controller connected to the \overline{DREQ} and \overline{DACK} lines for channel 3 of the 82258A.

Two registers are used to restrict the relative bus loading of the DMA controller. The burst register is loaded with a count representing the maximum number of contiguous clock cycles allowed for exclusive bus use. Similarly, the delay register specifies the minimum number of clock cycles permitted between successive DMA

Outputs:

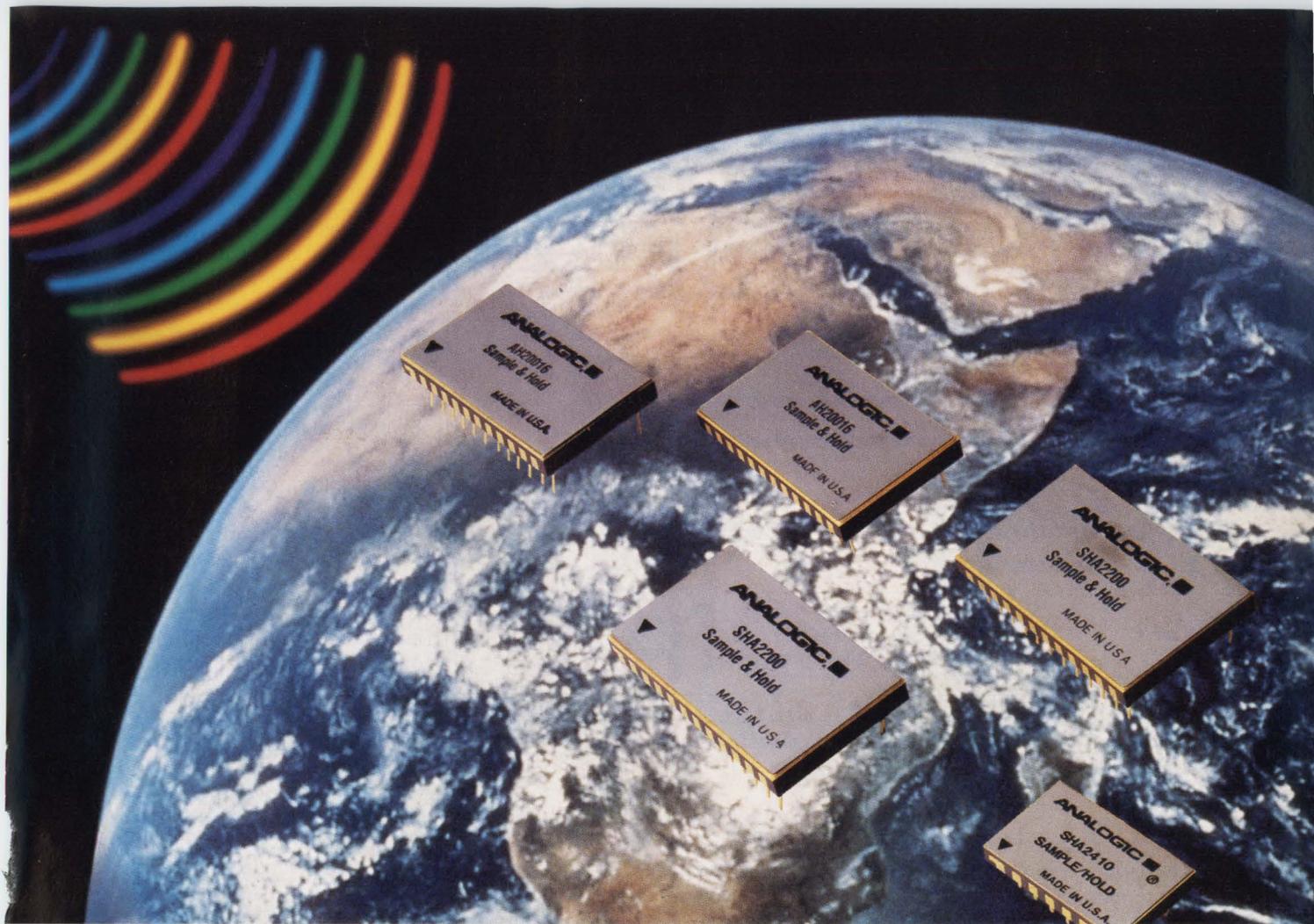
\overline{ADS} :	1FF	At down CLK:	$\overline{ADS} = (S^0 + S^1) \cdot \overline{ADS}$
\overline{BE} :	4FF	According to table (6 terms) and flyby:	
		At down CLK:	
		Set:	$(S^0 + S^1) \cdot \overline{ADS} \cdot f(A^1, A^0, \overline{BHE}, \text{flyby})$
		(Reset:	Ready) ← not necessary!
$\overline{W/R}$:	1FF	At down CLK:	
		Set:	S^0 ;
		Reset:	S^1 ;

Slave cycle outputs:

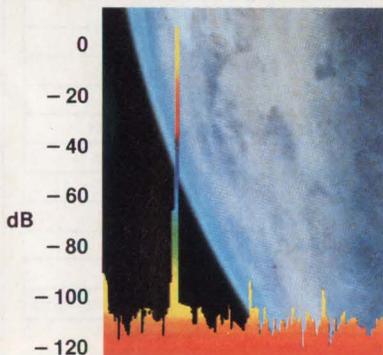
\overline{WR} :	1FF	Both FFs, at down CLK:	
\overline{RD} :	1FF	Set:	$\overline{CS} \cdot f(\overline{W/R} \text{ in});$
		Reset:	Ready
A0,A1, \overline{BHE} :	F	($\overline{BE0}$ in, $\overline{BE1}$ in, $\overline{BE2}$ in $\overline{BE3}$ in)	

FF = Flip-flop output

4. PAL PROGRAMMING involves seven PAL inputs, three outputs, and five input-output lines.



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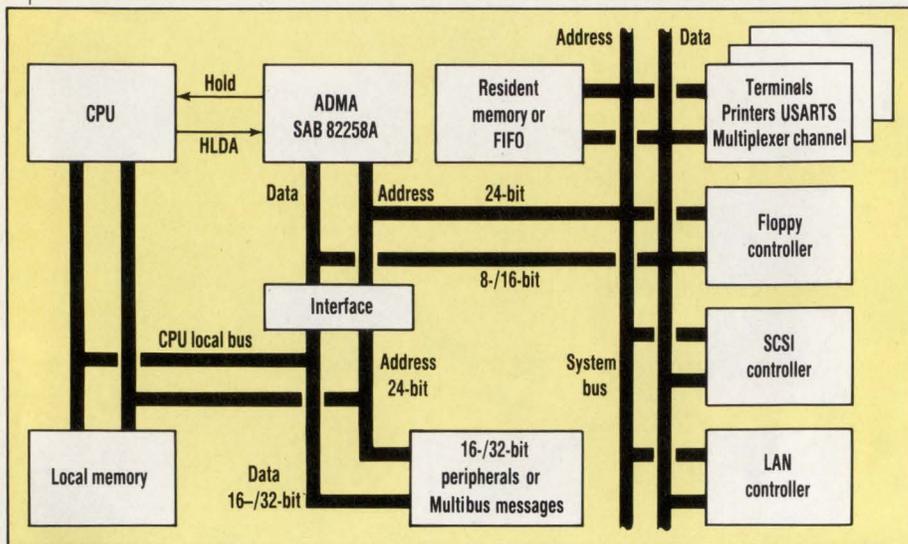
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DMA CONTROLLER



5. FOR HIGHER THROUGHPUT, THE CPU AND 82258A in the remote configuration can control a private bus isolated from the system bus by additional interface logic.

bursts.

To start or stop an individual DMA channel, the 80386 writes to the general command register as each channel's current state is shown in the general status register. Each channel is controlled by a set of registers accessible by the 80386 processor. The registers for a DMA channel are loaded by the controller from a command block in memory that was previously programmed by the 80386. After the DMA operation defined by this command block is performed, the controller writes updated register values and the channel status into memory. The basic command block in RAM specifies the channel command, DMA source address pointer, DMA destination address pointer, and DMA byte count.

The address pointers are 24-bit addresses, which make a 16-Mbyte address range possible. Also, a 24-bit byte count supports a maximum block length of 16 MBytes. The channel command specifies the details of the DMA operation. For example, the command defines the bus widths of the source and destination locations and whether the address pointers must be incremented, decremented, or kept constant.

To initiate a DMA operation, the 80386 loads the command pointer register of the relevant DMA chan-

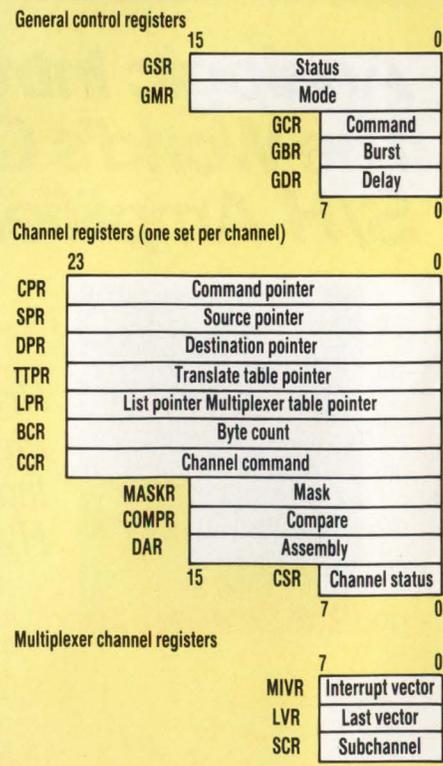
nel with the command block address in RAM. It then writes to the general command register to activate the DMA channel. Finally, the controller fetches the command block into its internal registers and performs the DMA operation. This operation normally continues until the byte count is decremented to zero or the channel is halted by the 80386. The controller's bidirectional End of DMA (EOD) control line can either be driven externally to halt a DMA operation or used as an output to indicate certain controller conditions, such as the end of DMA block.

The DMA controller can chain together blocks of commands to make a channel perform sequential operations. A command at the end of each command block in RAM specifies whether the channel must halt or jump to another command block upon completion of the current DMA. For command chaining, the next command block's location is given at the end of the current block in the form of a relative displacement or an absolute address. The channel continues to chain DMA operations until it encounters a stop command instead of another jump.

Memory-based command blocks also make it possible for the controller to perform data chaining. With this technique, data blocks from dif-

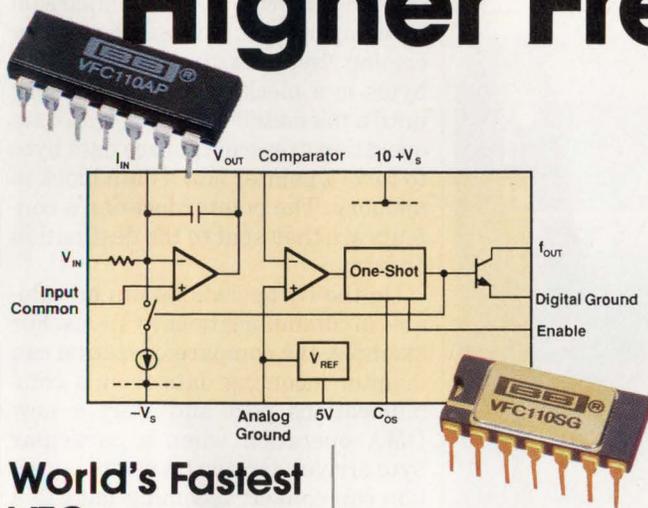
ferent areas in RAM can be linked together as one contiguous block during a single-channel command block execution. Source chaining gathers several data blocks in RAM and transfers them through a DMA channel as one block. Conversely, destination chaining splits a data block for storage in several different RAM locations.

Data chaining is specified at the beginning of a channel command block. To source chain, the source address pointer in the command block is replaced by a pointer to a list in RAM. This is a list of entries that define the length and location of each source data block to be chained. The DMA channel loads these entries into its byte count register and source address pointer. DMA operation continues until the controller reads a byte count of zero, which signifies the end of the list. For destination data chaining, the list contains pointers to the individual destination blocks in RAM.



6. ALL INTERNAL registers of the controller can be accessed by the CPU over an 8- or 16-bit bus. Total storage space is over 120 bytes.

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Handy Applications Guide

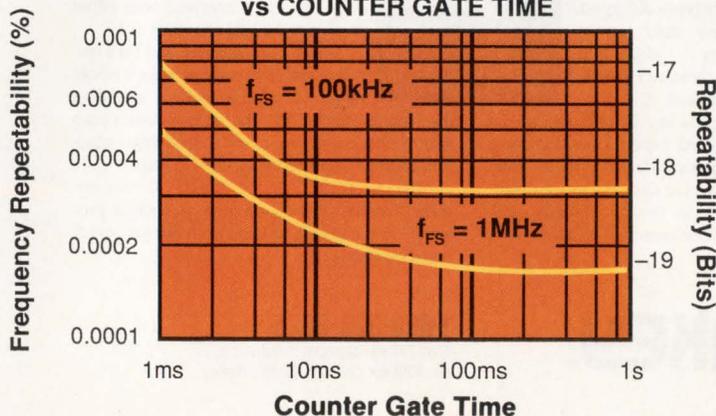
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FREQUENCY COUNT REPEATABILITY vs COUNTER GATE TIME



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DMA CONTROLLER

The data chain list can either be a sequential set of entries in RAM or a linked list. Each entry for a linked list is followed by a link pointer that specifies the RAM location of the list's next entry.

The 82258 doesn't usually look at

the data that's transferred. However, it can be programmed to perform an on-the-fly operation depending on what it sees as it inspects each transferred byte. There are three basic types of on-the-fly operations: mask-and-compare, verify, and translate.

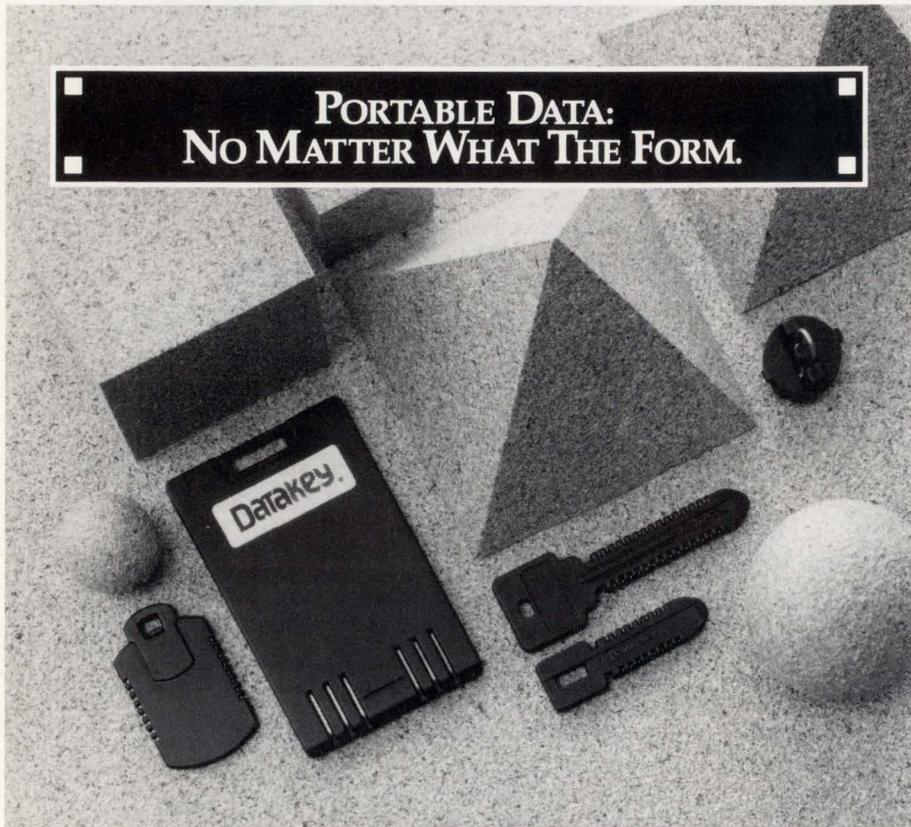
A mask-and-compare operation masks selected bits of a data byte and compares the masked byte with a specified bit pattern. The result of this comparison can initiate a new command block or execute a conditional stop command. The verify operation performs a block comparison by comparing the data stream's incoming bytes with corresponding bytes in a block of data in memory until a mismatch occurs. A translate operation uses each source data byte to form a pointer into a data block in memory. The pointer location's contents are then sent to the destination address.

On-the-fly operations can be valuable in communications systems. For example, the compare operation can monitor incoming data from a communications port and start a new DMA operation when a particular byte arrives. Or, the translate operation can convert incoming data to a different data code, for example, from EBCDIC (expanded binary coded decimal interchange code) bytes to ASCII characters.

Each of the four controller DMA channels can operate at a maximum data-transfer rate of 20 Mbytes per second using single cycle mode (two clocks per transfer). The maximum transfer rate is 10 Mbytes/s when the two-cycle mode is used. Channel 3 can alternatively be programmed as a multiplexer channel that supports up to 32 subchannels. On all DMA channels, the controller operates in the two-cycle mode. For each channel, the controller has a data assembly register where 8-bit bytes can be assembled to form 16-bit words. □

Vijay Desai, a product marketing engineer at Siemens Components, has a BSEE from M.S. University in India, an MSCS from Stevens Technology, Hoboken, N.J., and an MBA from the University of Phoenix, San Jose, Calif.

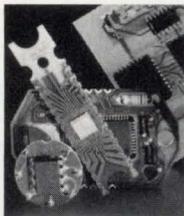
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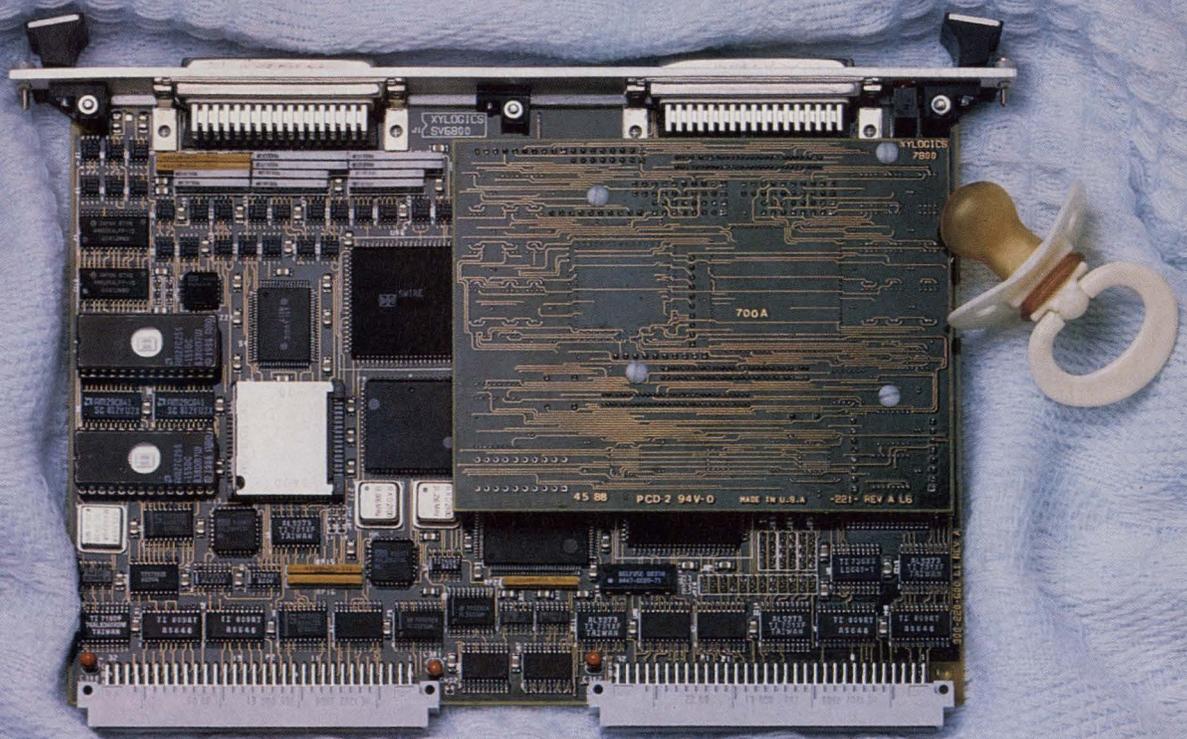
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			Channels	Resolution (bits)				
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	DT2811-PGL	Low Cost, Low-Level A/D, D/A; Interrupt	16SE/8DI	12			\$95	
	DT2814	Low Cost A/D, Int.	16SE	12			\$395	
	DT2815	Low Cost D/A	—	—			\$575	
	DT2817	Low Cost DIO	—	—			\$239	
GENERAL PURPOSE	DT2819	Am2935A Counter/Timer, DIO	—	—			consultatory	
	DT2808	Low Cost, DMA	16SE	10			\$595	
	DT2801	General Purpose, DMA	16SE/8DI	12			\$1,095	
	DT2801-A	Higher Throughput, DMA	16SE/8DI	12			\$1,970	
	DT2801/5716A	High Resolution, DMA	8DI	16			\$1,095	
	DT2805	Low Level, DMA	8DI	12			\$2,070	
	DT2805/5716A	Low Level, DMA	8DI	16			\$2,495	
	DT2809	16-bit SS&H, DMA	8SE, SS&H	16			\$1,895	
	DT2816	SS&H, DMA	4SE, SS&H	12			\$1,095	
	HIGH SPEED	DT2824-PGH	High Throughput, Low Cost A/D; DMA, Ints.	16SE/8DI	12			\$1,345
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— Fred Molinari, President

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OPERATE AN LCD DISPLAY FROM A VGA SYSTEM

A VGA DISPLAY SYSTEM IMPOSES SEVERAL SPECIAL REQUIREMENTS ON A LAPTOP'S LCD CONTROLLER.

Until recently no one display media offered all the desirable characteristics for a laptop: small size, low power, high contrast, and large viewing angle. Now, however, LCDs can meet all these requirements.

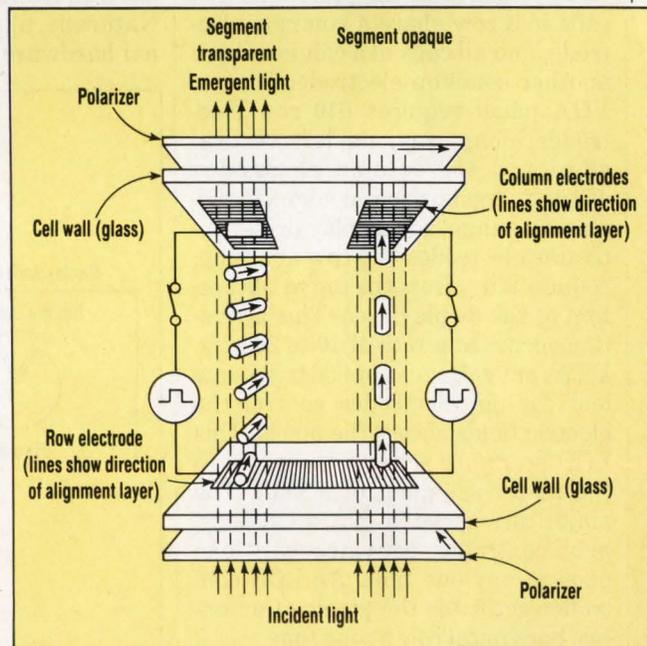
Liquid-crystal material is an organic crystalline compound characterized by a multistate molecular structure, which makes it particularly flexible. An LCD panel is made up of two parallel plain-glass plates that support and protect this crystalline compound (*Fig. 1*). An electrode matrix deposited on these glass plates divides the liquid-crystal material into a large number of separate tiny liquid-crystal cells, or pixels. The material rotates polarized light passing through it by $90^\circ \pm$. By applying an external electric field across a pixel of the material, the rotation can be reduced all the way to zero.

A polarizer placed on the back of the LCD sandwich extracts and passes only polarized light from ordinary nonpolarized light that enters. The liquid-crystal material then rotates this polarized light $90^\circ \pm$ when it isn't activated by an electric field. Another polarizer at the front of the panel, oriented to polarize at a right angle to the polarizer at the back

of the panel, allows almost free passage of the rotated light exiting from the liquid crystal. A pixel would thus appear to be bright. To brighten the display background, many LCD panels employ a special light source behind the display panel, called backlighting. With backlighting, the panel need not depend on the ambient light for brightness.

An electric field applied across the liquid-crystal material in a pixel, however, reduces the material's rotation of its incident light. The front polarizer now tends to block passage of the light. The lower the degree of rotation, the darker the pixel appears. Large LCD panels exploit this light-valving property of the liquid-crystal material to create images.

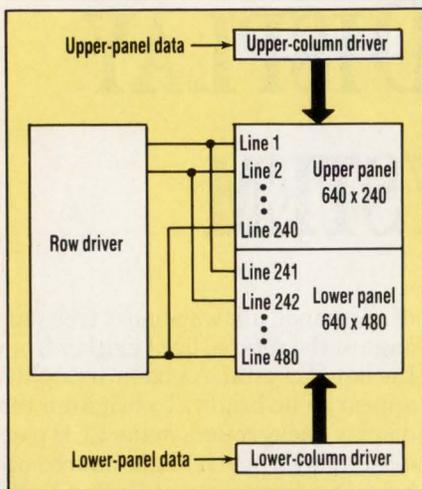
A VGA-compatible LCD panel must have 307,200 cells—the highest



1. AT THE CENTER of an LCD panel, two parallel plain-glass plates support and protect the liquid-crystal material. An electrode matrix on these glass plates divides the LCD material into a large number of separate cells or pixels.

ARUN JOHARY and T. OGUCHI
Chips and Technologies Inc.,
3050 Zanker Rd., San Jose, CA 95134;
(408) 434-0600.

LCD VGA DISPLAY SYSTEM



2. ALMOST ALL high-resolution (400-line and larger) LCD panels are organized as dual panels. This arrangement keeps two rows of the display, separated by 240 rows, on at the same time.

resolution under VGA—to accurately resolve a 640-pixel-by-480-line display. Since the brightness of each pixel must be controlled independently to form an image, the panel must offer a way to apply an electric field across any of the 307,200 cells.

To that end, rows and columns of electrodes define the pixel cells. All cells in a row share a common electrode, and all cells in a column share another common electrode. Thus, a VGA panel requires 640 row electrodes along, say, its left vertical edge and 480 column electrodes along its top horizontal edge. To display an image, the display driver activates electrodes one row at a time, sequentially, from the top to the bottom of the display area. This activation occurs at a rate of 10 to 20 kHz. Different voltages applied to the row and column electrodes control the electric fields across the pixels. This LCD scanning scheme is similar to the raster scanning of a CRT. The major difference is that a CRT display controller activates only one pixel at any one time. An LCD controller activates the pixels of an entire horizontal row at one time.

This characteristic of LCDs helps overcome the fact that individual LCD pixels are not as bright as CRT pixels. The LCD's row-scanning

scheme keeps every LCD pixel on for a much longer time than CRT pixels are kept on. In a 640-by-480 display, a CRT pixel is on for only one out of 307,200 pixel cycles. In a 640-by-480 LCD panel, a pixel is on for one out of 480 cycles—640 times longer than a CRT pixel. Although the absolute intensity of an individual LCD pixel is low, the perceived intensity of the total display is comparable to that of a CRT display.

Dual-panel construction is used to further enhance the brightness of LCDs. Today, almost all high-resolution (400 lines and greater) LCD panels incorporate a dual-panel design. The upper and lower halves of the display panel activate in parallel. This arrangement keeps two rows of the display, separated by 240 rows, on at the same time. In a 640-by-480 panel, then, each pixel is on for one out of 240 pixel cycles—a duty cycle of 1/240 (Fig. 2).

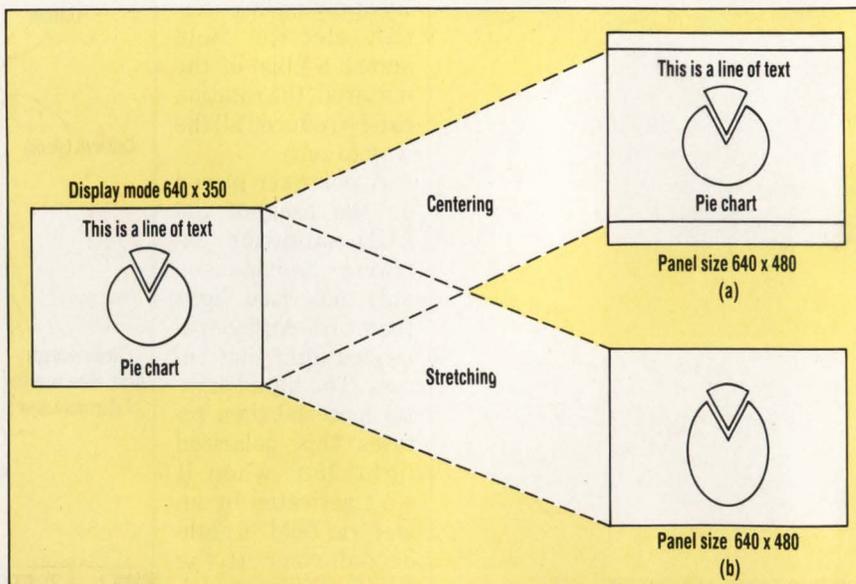
Unfortunately, a constant electric field applied across the liquid-crystal material has a tendency to disintegrate the material. To avoid this, the interfacing circuit must periodically switch the polarity of the applied voltage. A pixel that is on will then have an average dc voltage of zero. Naturally, all LCDs must have internal hardware to switch the polarity

of the voltage across a pixel, but the display's interface controller must generate the control timing for this hardware. LCDs from different vendors require different frequencies for this timing control signal. A good controller will be flexible enough to accommodate this variable.

Because most LCD panels today provide only monochrome displays, the interface controller circuit need supply only 1 bit/pixel to drive the panel. To drive an entire row of 640 pixels at one time, however, the interface would have to provide 640 line drivers. Supplying that many drivers is physically inconvenient, so most panels have internal shift registers that take 4 or 8 bits at a time from the display interface controller and assemble them internally to drive the 640 pixels.

In a single-drive dual-panel display that uses 4 bits at a time, the pixels for a row in the upper panel clock in first, followed by the pixels for the corresponding row in the lower panel. In a dual-drive panel that uses 8 bits at a time, four pixels for a row in the upper panel and four for the corresponding row in the lower panel clock in at the same time. A controller should be able to drive either type of dual-panel display.

A desktop VGA system supports



3. TO DISPLAY a lower-resolution mode on a high-resolution screen, the LCD-panel controller must use just a portion of the display surface and center a smaller image in it (a), or expand but distort the image to fill the full display surface (b).

LCD VGA DISPLAY SYSTEM

color on a CRT color monitor and displays gray scales on a CRT monochrome monitor. Gray-scale LCD panels eventually will become available.

Keeping the time that a pixel is on constant while changing the applied voltage creates a gray scale in an analog-driven monochrome CRT display. In a monochrome LCD, however, the controller is a digital circuit and cannot control the voltage across a pixel. To provide a gray scale, a digital controller must instead change the time that a pixel is on at a constant voltage, using either a frame or a line duty-cycle approach.

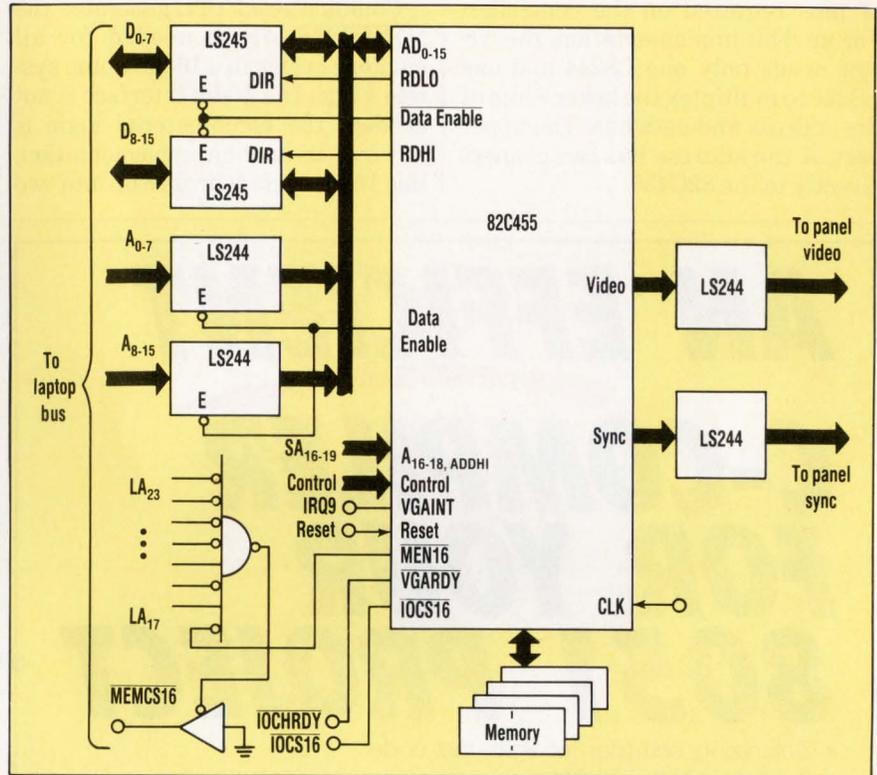
With the frame duty-cycle approach, called frame-rate control (FRC), the controller turns the pixel on in some frames and off in others. This action controls the pixel's average duty cycle, simulating a gray scale. With the line duty-cycle approach, called pulse-width modulation (PWM), a pixel turns on every frame, but not for an entire row-scanning period. Again, the control of the pixel's average duty cycle produces the gray scale.

The PWM-generated gray scale produces less display flickering than the FRC-generated one. The PWM approach requires a special panel, however. As is the case with single- and dual-drive panels, an LCD controller should be able to simulate gray scales with either method.

The VGA standard actually encompasses several resolution modes:

Mode	Resolution	Physical
Low text	40/25	360/720 × 400
High text	80/25	720 × 400
Low graph	320 × 200	320/640 × 400
Med graph	640 × 200	640 × 400
High graph	640 × 350	640 × 350
High graph	640 × 350	640 × 480

A VGA CRT handles the different resolutions by changing the horizontal and vertical sweep rates to the CRT monitor. The CRT, an analog device, adjusts the display to fill the full viewing surface. An LCD, being digital, cannot expand a lower-resolution display mode to fill the entire display surface. With an LCD, since the highest VGA resolution is 640 by



4. THE ONLY ADDITIONAL logic needed to integrate the 82C455 flat-panel VGA controller into a laptop system is supplied by a few buffers and some TTL.

480, the panel must provide 640 times 480—307,200—pixels. To display a lower-resolution mode, the LCD-panel controller can do one of two things. It can use only a portion of the display surface and center a smaller image in it (*Fig. 3a*). Or it can expand, but distort, the image to fill the full display surface (*Fig. 3b*). Ideally, the display controller should provide both options.

The 82C455 flat-panel VGA controller from Chips and Technologies Inc. meets these and all other criteria mentioned. In addition to gray-scale support for both the FRC and PWM techniques, the 82C455 can display color images on color LCD panels—although such panels are still in the early stages of development. The 82C455 can directly interface to a CRT display.

The 82C455 has several built-in power-saving features. In a power-down mode, the chip refreshes the video dynamic RAM, but no other activity takes place. Another mode shuts off the display, but the video subsystem remains active, again re-

ducing power consumption.

The 82C455 includes a high-performance 16-bit memory and I/O interface to the system microprocessor. Because the video subsystems of laptop computers reside on the motherboard, the 82C455 can share the board's resources. For instance, the video basic I/O system can be combined with the system BIOS and housed in a single ROM, thereby eliminating the need for a separate BIOS ROM. Also, because a VGA system requires 256 kbytes of memory, the 82C455 can directly interface to dynamic RAM comprised of 64k x 4-bit chips or 8-bit SIM modules. The 82C455 can be interfaced to static RAMs using simple circuitry.

The only additional logic needed to integrate the 82C455 into a system are a few buffers and some TTL (*Fig. 4*). Two 74LS244 and two 74LS245 octal bus-transceiver buffers multiplex the system address and data signals onto the bus of the 82C455. The 82C455 generates all control signals for the buffers. Multiplexing reduces the total number

LCD VGA DISPLAY SYSTEM

of pins required on the controller. For an 8-bit implementation, the circuit needs only one LS244 and one LS245 to multiplex the lower 8 bits of the address and data bus. The upper part of the address bus can connect directly to the 82C455.

Combinatorial TTL generates the MEMCS16 signal needed for all memory cycles to a 16-bit laptop system's bus. If a 16-bit interface is not needed, the combinatorial logic is left out. In an 8-bit implementation, this 16-bit cycle is broken up into two

8-bit cycles.

Since timing requirements for a MEMCS16 signal are very stringent for a 16-bit circuit, the signal is best generated by programmable array logic, not the controller. If the circuit isn't fast enough, the 16-bit memory cycle executes as two 8-bit memory cycles. Supporting 16-bit cycles is important, however, because two 8-bit memory cycles are significantly slower than the single 16-bit cycle, making the 16-bit bus more than twice as fast as an 8-bit bus.

Supporting 16-bit I/O and memory cycles is also important because most registers in a VGA system are accessed indirectly from an index-data pair of registers. VGA software accesses these registers in one 16-bit cycle. In particular, in a mode in which cursor movement is very frequent—such as text mode—the I/O cycles initiate the accesses. Even in graphics mode, I/O cycles initiate accesses for the color and plane masks, which accelerate drawing operations. The 82C455 has complete hardware support for 16-bit I/O cycles.

The 82C455 generates an IOCS16 signal, the same as for memory cycles, to indicate that a 16-bit I/O cycle can be executed. The VGARDY signal from the 82C455 connects to the IOCHRDY signal line on the laptop's bus. This signal inserts wait states when the laptop's CPU tries to access display memory that is unavailable. The 82C455 also supports a CRT interrupt to the CPU. This interrupt, generated once every display frame, can serve in special effects, such as smooth scrolling, double-buffer switching, or display animation. □

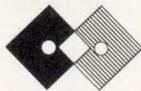
Arun Johary is a technical marketing engineer for Chips and Technologies, Inc., San Jose, California. He holds a MSEE from the University of Southern California.

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Max, 20dB Stop Frequency (MHz)			19	32	47	70	90	147	210	290	410	580	750	840	1000	1100	1340
Prices (ea.): Qty. (1-9)			P \$11.45, B \$32.95, N \$35.95, S \$34.95														

HIGH PASS	Model	*HP-	50	100	150	200	250	300	400	500	600	700	800	900	1000
Pass Band (MHz)		start, max.	41	90	133	185	225	290	395	500	600	700	780	910	1000
		end, min.	200	400	600	800	1200	1200	1600	1600	1600	1800	2000	2100	2200
Min. 20dB Stop Frequency (MHz)			26	55	95	116	150	190	290	365	460	520	570	660	720
Prices (ea.): Qty. (1-9)			P \$14.95, B \$36.95, N \$39.95, S \$38.95												

*Prefix **P** for pins, **B** for BNC, **N** for Type N, **S** for SMA

example: **PLP-10.7**

CIRCLE 52

C105 REV. E

CIRCLE
524 EFFICIENT
5-V SUPPLY
FROM BATTERIES

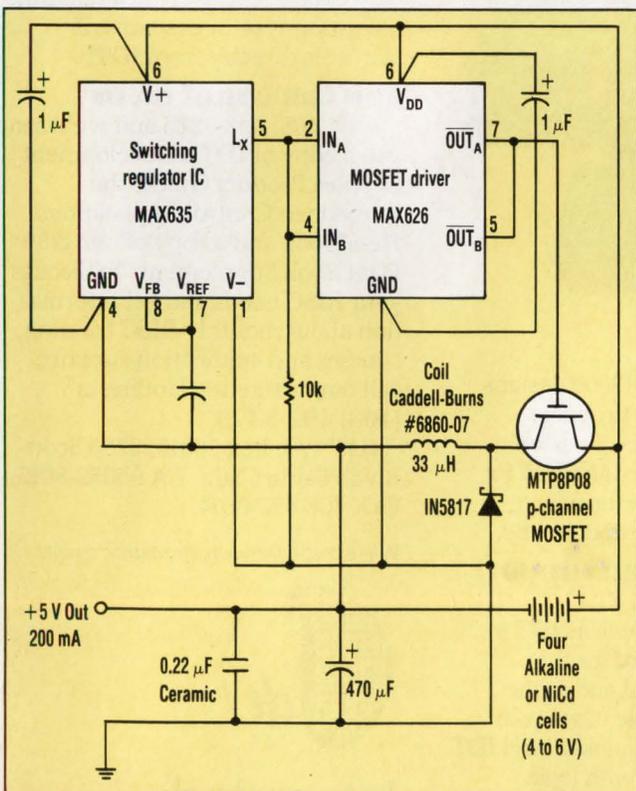
LEN SHERMAN

Maxim Integrated Products,
 120 San Gabriel Dr., Sunnyvale, CA 94086;
 (408) 737-7600.

From four alkaline or nickel-cadmium cells, an efficient power-supply circuit steps down to a 5-V regulated output when the batteries are new, or steps up to 5 V when the input drops below 5 V (see the figure). Fresh alkaline batteries supply about 6 V and fully charged nickel-cadmiums offer about 5.4 V. The circuit also uses fewer parts than other buck-boost types of converters.

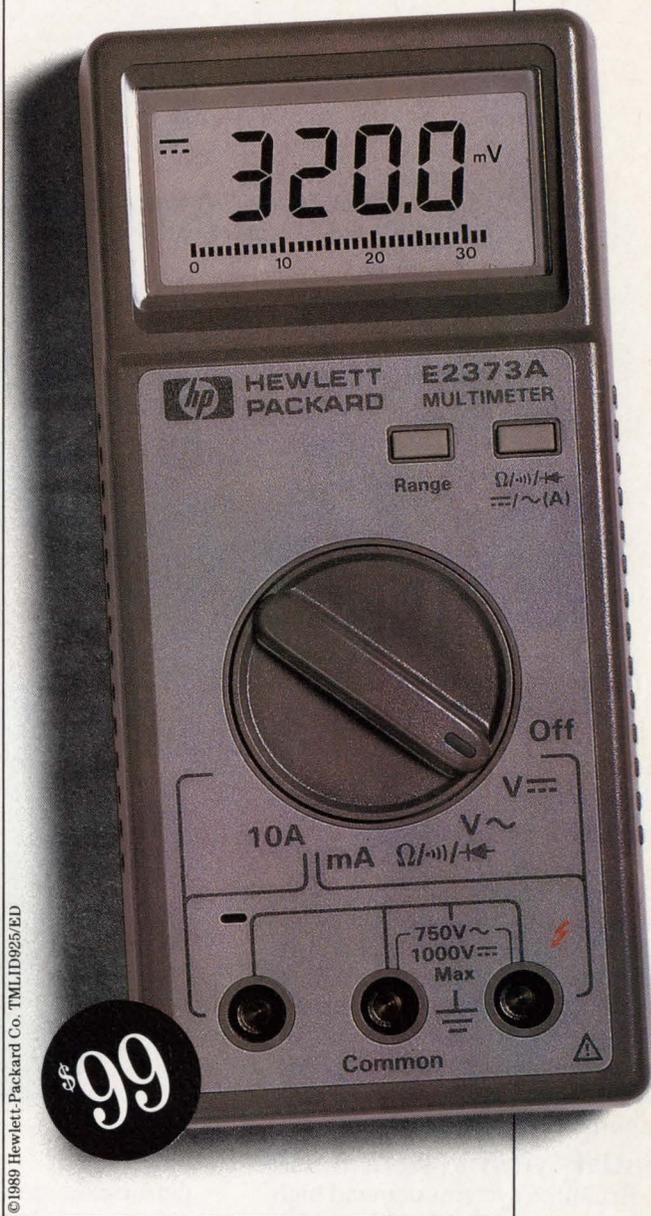
Connecting the battery's negative terminal to the circuit's +5-V output with an inverting topology avoids the need for transformers and more complex buck-boost conversion topologies. Because the batteries can be treated as a floating source, this battery connection isn't a problem for many portable and hand-held products.

The negative output and the pins of an inverting dc-to-dc MAX635 converter that normally connect to ground



THIS POWER-SUPPLY CIRCUIT steps down to a 5-V regulated output when the batteries are new, or steps up to 5 V when the input battery drops to about 4 V and lower.

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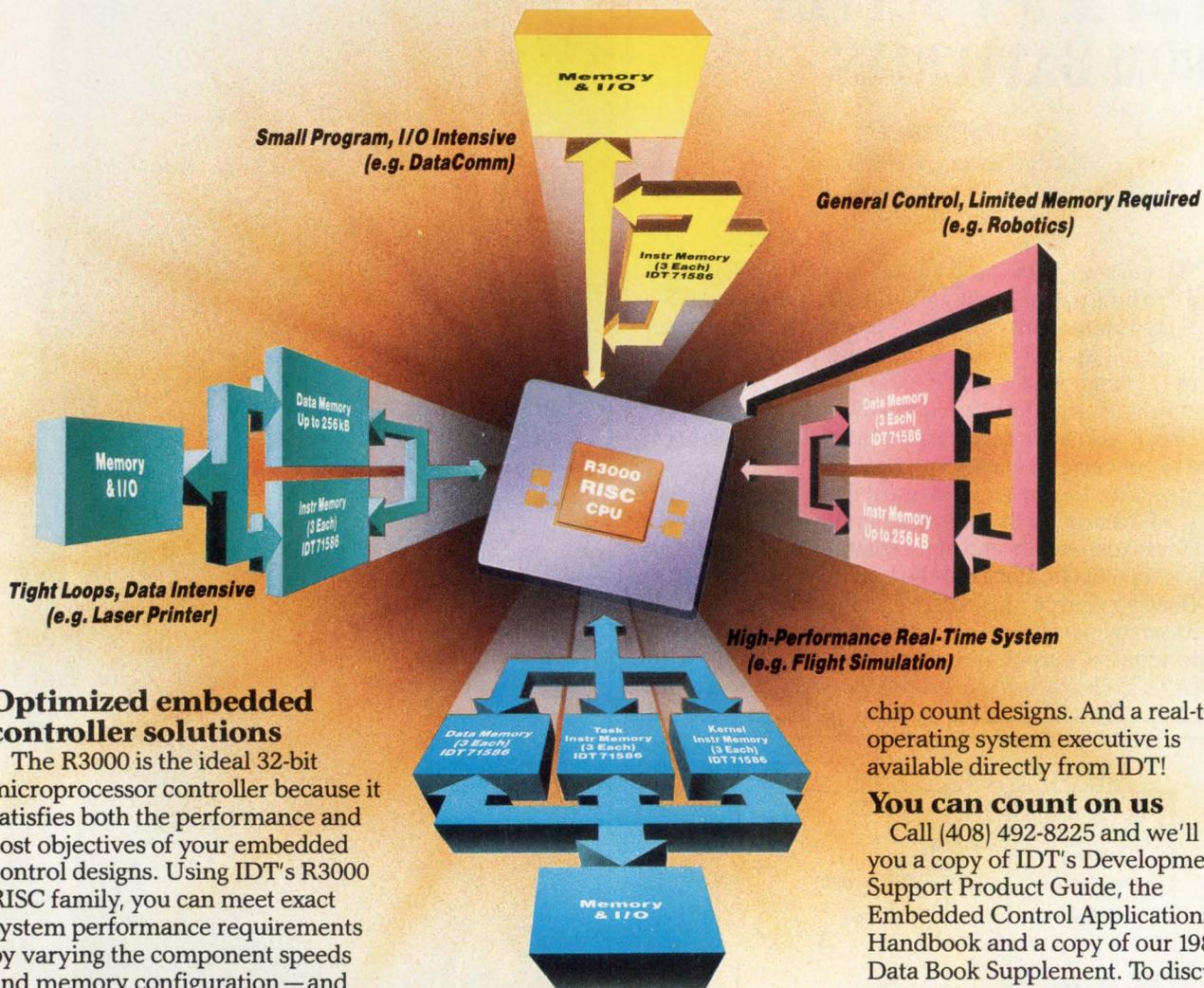
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**Integrated
Device Technology**

IDEAS FOR DESIGN

are swapped. Therefore, the normal negative output voltage (pin 1) connects to ground and the normal ground (pin 4) is +5 V with respect to pin 1. A low cost discrete p-channel MTP8P08 MOSFET and IC MAX626 driver can handle up to 200 mA, which may be required near the end of battery life.

For loads below 20 mA, the external MOSFET and the driver IC can be omitted if a 330- μ H inductor (Caddell-Burns #7070-31) is substituted for the one in the figure. In this case, the MAX635's L_X (pin 5) connects directly to the coil. \square

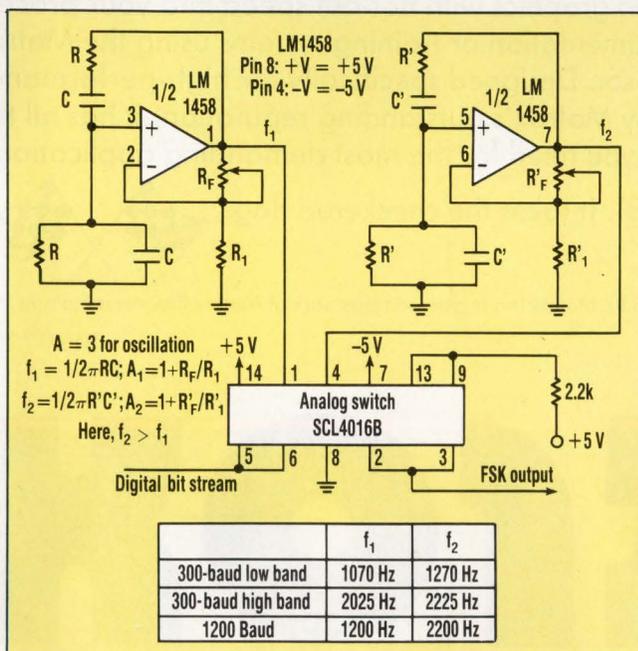
CIRCLE 525 BUILD A LOW-COST FSK GENERATOR

V. LAKSMINARAYANAN

Centre for the Development of Telematics,
Sneha Corp., 71/1 Miller Rd.,
Bangalore-560 052, India.

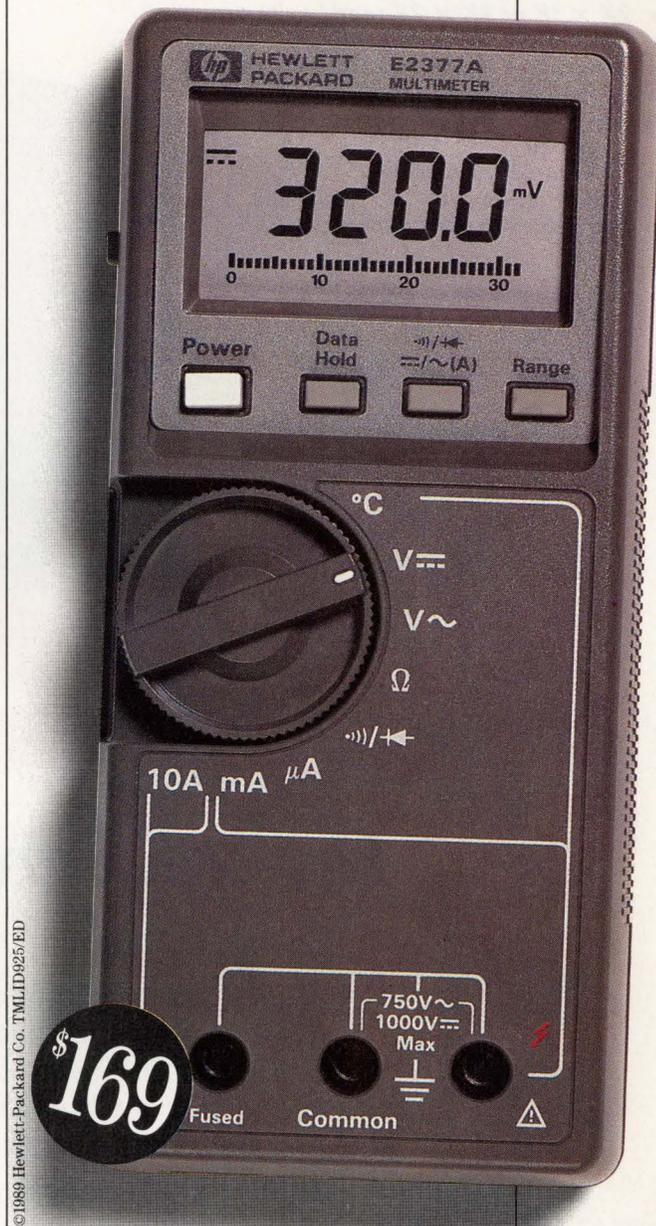
You can build a low-cost frequency-shift-keying (FSK) generator with just two common low-cost chips: an LM1458 dual op amp and an SCL4016 quad analog switch. This is a handy method when expensive FSK generator chips aren't available. The LM1458 forms two Wien-bridge oscillators, which generate the two discrete frequencies that represent the binary digits 0 and 1 (see the figure).

Two analog switches within the SCL4016 select one of



TWO COMMON LOW-COST CHIPS, a dual op amp and a quad analog switch, can form an FSK generator.

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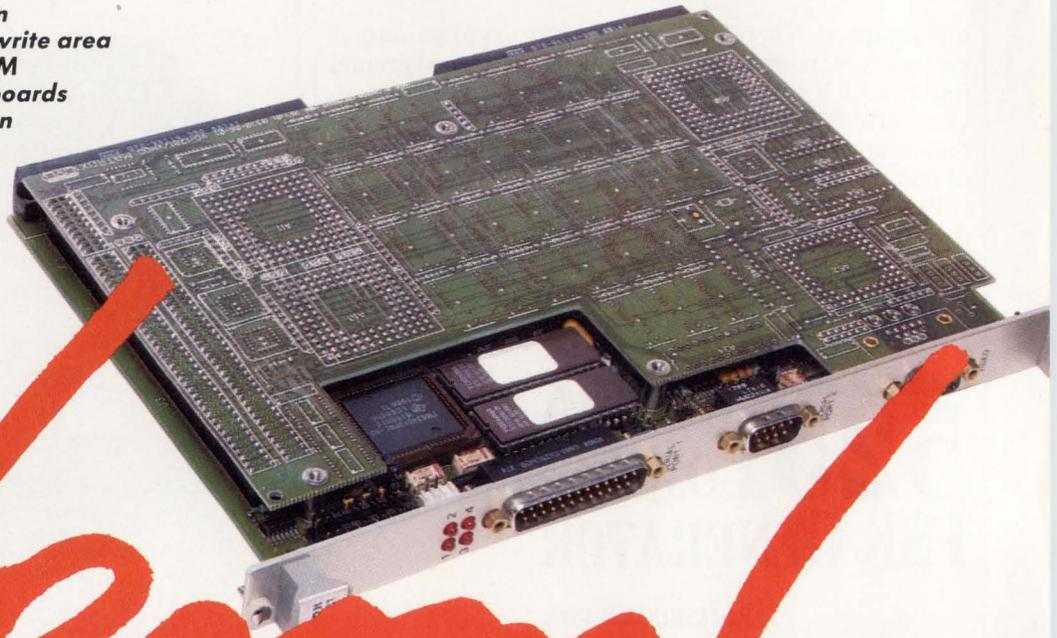
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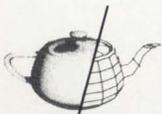


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ED-VG / 789

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IDEAS FOR DESIGN

the two frequencies that correspond to digital 1 and 0 data bits. One switch operates as an inverter to enable only one oscillator's output in accordance with the input digital bit stream.

Because the switching frequency limit of SCL4016 is 40 MHz, the circuit can easily accommodate high data rates. The two frequencies, f_1 and f_2 , primarily depend on the values of RC and R'C'. The values of R_F and R_V should be set slightly past the point where the circuits start oscillating. □

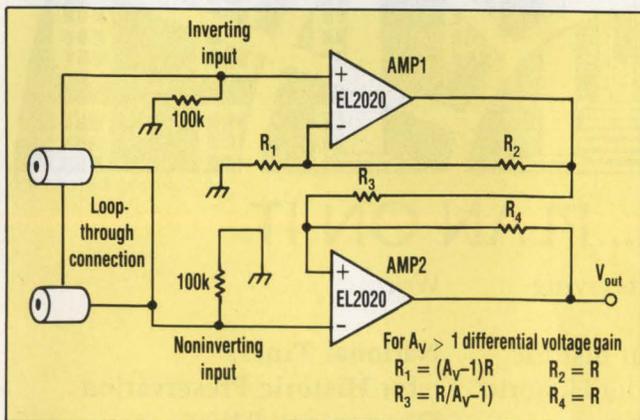
CIRCLE 526 CURRENT-MODE SPEEDS VIDEO AMPS

WILLIAM H. GROSS
Elantec Inc., 1996 Tarob Ct.,
Milpitas, CA 95035;
(408) 945-1323.

Current-mode-feedback amplifiers are frequently used for high-speed applications because of their wide bandwidth, ease of use, and excellent linearity. Merely scaling the feedback resistor values to the required low impedance level in most op-amp circuits can implement current-mode feedback. Unfortunately, the traditional differential-to-single-ended amplifier configured with current feedback has low input impedance, which causes difficulties in many applications.

Also, the loop-through cable connection of most video instrumentation inputs must be differential to reject common-mode power-line pickup, and must avoid loading the cable and introducing ground loops. Then, the last circuit in the chain terminates in the cable's characteristic impedance.

Though a three-amplifier circuit would avoid the low input-impedance problem, it's complex, and the overall



A HIGH INPUT-IMPEDANCE differential-to-single-ended amplifier with current feedback uses just two amplifiers and four resistors.

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CIRCLE 150

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IDEAS FOR DESIGN

bandwidth would suffer because the signal passes through two amplifiers. A better way to implement a high input-impedance differential-to-single-ended amplifier uses just two amplifiers and four resistors (see the figure).

The circuit's resistor values are based on the desired differential voltage gain A_v and an amplifier feedback value R . With two Elantec EL2020 op amps and four $1k\Omega$ resistors for R_{1-4} , the differential gain is 2 and the bandwidth is 30 MHz. The common-mode input range increases for larger differential gains. Gain values less than 1.1 are impractical: The $(A_v - 1)$ values in the equations approach zero.

With the supply voltage equal to ± 15 V, both the common and differential-mode input ranges are over ± 6 V. Common-mode rejection at low frequencies depends on resistor matching; tweaking R_1 can make the common-mode rejection greater than 70 dB. □

IFD WINNERS

IFD Winner for March 9, 1989

Errol Dietz, National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95052-8090. His idea: "Reduce Noise in Voltage Regulators."



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**CONTROLLER BOOSTS
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Packing dynamic-RAM control, direct memory access to the print engine, bit manipulation, and print-engine-interface logic on one chip, the CL-GP425 raster-printer accelerator from Cirrus Logic Inc., Milpitas, Calif., increases laser-printer speed by a factor of up to six. The CMOS controller supports up to 25 pages/min. In operation, the host microprocessor breaks complex polygons into trapezoids, which the GP425 draws in memory. Imaging is performed in parallel while the microprocessor describes other graphics objects. Bit manipulation automatically offloads the processor during pattern-fill operations for improved printer operation. Pricing is under \$35 each for quantities of 1000. ML

CIRCLE 301

**FASTER ROUTING
SPEEDS ARRAY DESIGN**

By harnessing parallel processors distributed across a network, a wire-routing program for large sea-of-gates arrays speeds designing with those gates. The software, from Descartes Automation Systems Inc., Santa Clara, Calif., can route connections 2 to 10 times faster than the company's last package. The rate depends on how many computation nodes are available on the network. The software needs the circuit net list, the base array's physical-layout description, and the library of macrocells to be used. All three sets of data are entered into a translator that first places the various blocks and then partitions the layout into a checkerboard-like grid. Some preprocessing optimizes cell-to-cell placement, the circuits in each grid block, and the placement of the grid blocks. Next, the routing is done in three passes—global, intermediate, and final. DB

CIRCLE 302

**20-MHZ, 80386 PCs
SELL FOR UNDER \$1,800**

Banking on its experience as a PC-motherboard maker, DTK Computer Inc., City of Industry, Calif., came up with a family of inexpensive 80386-based desktop and tower PCs. The 20-MHz KEEN-2000 series operates at 27.3 MHz with 80-ns dynamic RAM that requires one wait state. The systems pack two serial and one parallel port, 1 Mbyte of RAM, eight expansion slots, a 80387-coprocessor socket, and FCC class A verification. Base prices start at \$1695 for the desktop version and \$1795 for the tower. A small-footprint version of the desktop PC, the KEEN-2030, offers less expansion capability and costs \$1449. DB

CIRCLE 303

**SPICE SIMULATOR
ARRIVES FOR 80386 PCs**

Until now, Meta-Software's HSpice circuit simulator has been available only on workstations and mainframes from Apollo, Cray, IBM, Sun, and VAX. But the Campbell, Calif. company's new version for 80386-based IBM PCs and compatibles packs all the punch of the workstation product. Meta-Software has also joined forces with Silvaco International, Santa Clara, Calif., which kicks in its DDL2000 discrete-component and IC library of over 2,000 devices. The library includes models of diodes, zeners, JFETs, BJTs, power MOSFETs, SCRs, op amps, comparators, and 555-type timers. Unlike those in many libraries, these models are created from actual measurements taken over changes in temperature. If no model exists for a particular device, \$200 buys one—often with 24-hour turnaround. HSpice for the 80386 costs \$4000. FG

CIRCLE 304

**1000-V, 1-A DIODES
RECOVER IN 75 NS**

For snubbing the power MOSFETs in high-frequency switching power supplies, a line of ultrafast-recovery power diodes has arrived from Motorola Inc., Phoenix. The diodes carry maximum reverse-blocking voltage ratings of 700 to 1000 V. Besides recovering from 1 A of forward current in under 75 ns maximum, the MUR8100E family of diodes absorbs a minimum of 20 millijoules in a reverse-avalanche condition. Other ultrafast diodes fail instantaneously when their blocking voltage is exceeded. Maximum forward current at 150°C runs 8 A on average. Maximum instantaneous forward drop at 8 A is 1.8 V at 25°C, and drops to 1.5 V at 150°C. The die comes in a 2-pin (no center pin) TO-220 package. The price in hundreds runs \$2.13 to \$2.93 each. FG

CIRCLE 305

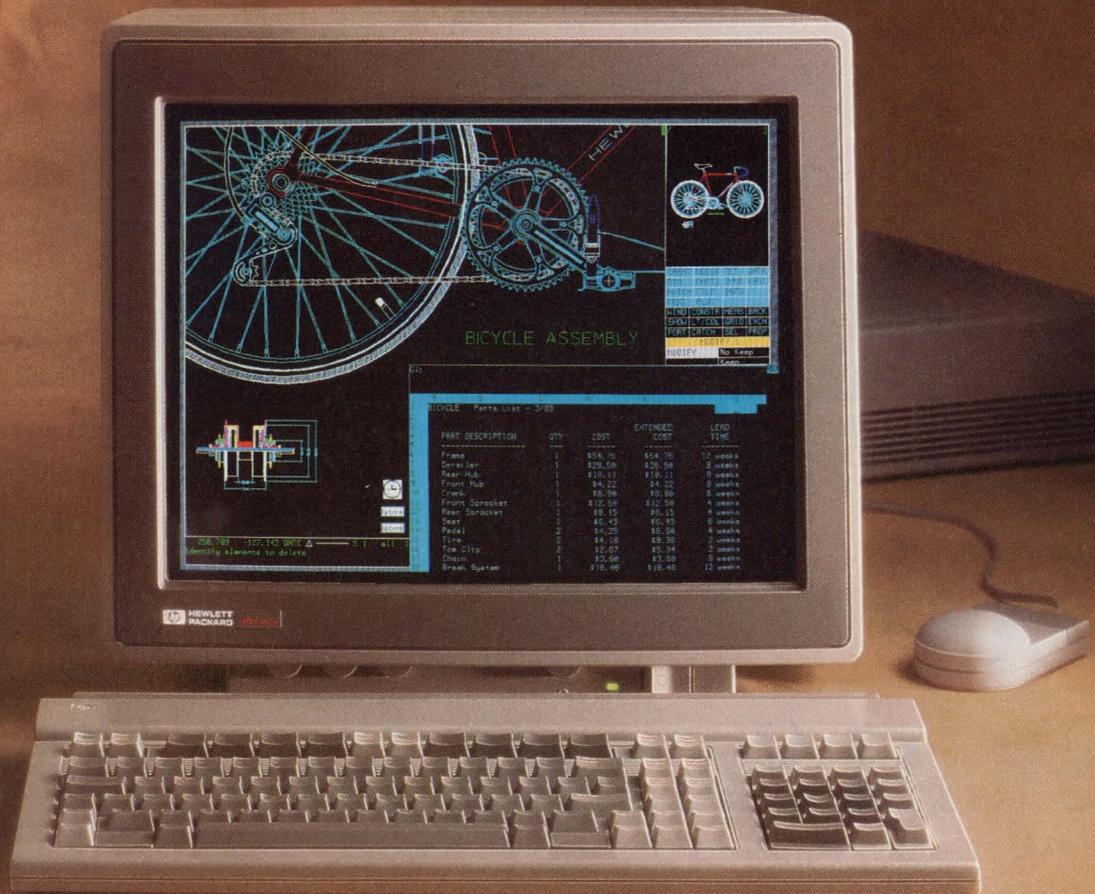
**NETWORK SOFTWARE GETS
DIAGNOSTIC ENHANCEMENTS**

Wandel & Goltermann is revising its network-management software for its DNE-2100 data-network diagnostics system. The new version of the West German company's SWP-120 program gives network managers several added benefits: remote control (unstaffed remote facilities can be accessed for monitoring and testing) and an IBM Netview-PC interface. Also, faulty network components can be automatically restored by alerts from the DNE-2100 or any network-management facility linked to Netview. The SWP-120 software retains such features as multiline switching; unlimited stored configurations; cost-effective modular design; and analog and digital patching facilities. The package's cost varies with user's needs. JG

CIRCLE 306

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Hewlett-Packard's adherence to proven standards and use of the Motorola MC68030 processor insure access to an extensive base

of application software. The 340C+ can either be used as a standalone workstation or in a network. Its built-in LAN interface provides access to a range of HP workstations and servers as well as to a multivendor computer environment.

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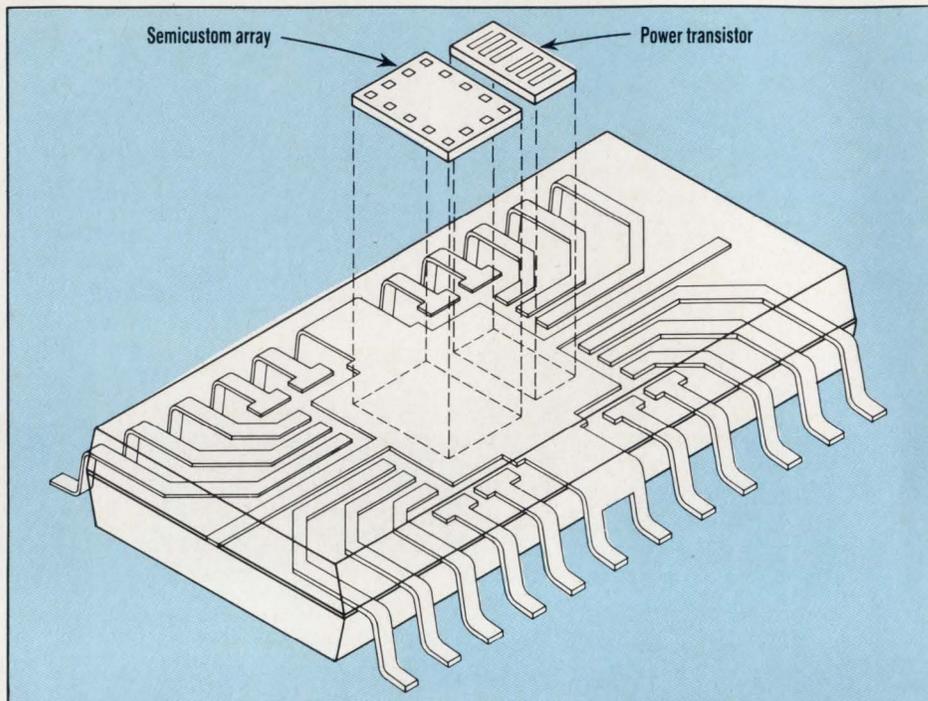
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CIRCLE 50



1. BY ADDING A DUAL 2.5-A, 50-V power transistor in a package with its analog-digital arrays, Cherry Semiconductor created the Genesis 6000 family of power IC arrays.

ANALOG ARRAYS ADAPT TO SMALL SIGNALS, HIGH POWER

FRANK GOODENOUGH

The explosive growth in the availability of analog and mixed analog-digital arrays over the last 18 months shows no sign of abating (ELECTRONIC DESIGN, June 22, p. 49). Designers now have two more array choices for condensing analog or mixed analog-digital pc-board circuits into one IC package: the Genesis 6000 family from Cherry Semiconductor, and the RFA line from the Semiconductor Division of Raytheon Co.

Cherry doubled the number of its analog and mixed analog-digital array offerings simply by adding a 5-A, 50-V power transistor to its 12 bipolar arrays. Raytheon's RFA line complements its RLA family of bipolar analog "gain-block" arrays. The new arrays have junction field-effect transistors (JFETs) onboard. They can be used to build analog switches and FET-input op amps, as well as supply greater slew rates.

Cherry chose a multichip approach with the Genesis 6000, eschewing the conventional approaches of putting small-signal analog and logic along with power circuitry on one chip, or putting small-signal circuitry on one chip and power on one or more discrete off-chip devices. In Cherry's design, small-signal logic and power circuitry are on separate chips, and both chips are mounted in one package.

The leadframe absorbs the heat from the power chip, transmits it to the package,

ANALOG ARRAYS

and minimizes heat transfer to the control chip (the array). The Genesis 6000 is available in a 20- or 24-pin surface-mount small outline "bat-wing" package, or a 15-lead multiwatt power tab single-inline package. In the bat-wing package, the two center pins on both sides of the package form two large tabs with the portion of the leadframe on which the power chip is mounted. Heat is carried from the chip through the leadframe tabs to the copper foil on a pc board.

The 5-A power device is actually a pair of vertical 2.5-A npn transistors, with the junctions isolated from each other (Fig. 1, right). The transistors have separate emitter, base, and collector contacts. Each npn can perform a different function, or both can be connected in parallel to handle 5 A. They also can be connected in series to form a totem-pole output capable of sourcing or sinking current. The forward voltage drop of each half at 2 A is 2 V, the saturation voltage at 1 A is 300 mV, the beta (current gain) is 100, and the transistor f_T s run 400 MHz.

IC OR NOT IC

Built on an IC process, the Genesis 6000 is basically a two-transistor bipolar power IC. Like the current in a bipolar IC's npns, the 6000's current

flows vertically from the emitter down to an n-type buried layer, laterally through that layer to an n-type sinker, or plug diffusion, and through it back to the top. There, it's picked up by the collector contact and connected to a bonding pad by metallization. The buried layer and sinker minimize resistance. The bottom of the die (the substrate of the IC) is bonded to the leadframe.

On-chip resistors sample 20% of each emitter's current. The voltages across the resistors appear between a sense bonding pad and the emitter pad. These voltages can be used as feedback to the control chip or as protection in the form of current limiting. Low current npns on an array could supply a constant current source for a strain gage; the power npn could drive an actuator.

Cherry's arrays have the transistors needed to build a dc amplifier that can amplify the millivolt output of a strain gage enough to drive the power chip. In fact, without those arrays, the Genesis 6000 is just a very expensive 5-A, 50-V transistor.

The 12 Genesis arrays offer a wide range of capabilities. The mixed analog-digital Genesis 1500 has a core of 98 Integrated Injection Logic (I²L) gates (Fig. 1, left). Around it are analog tiles with small-signal transis-

tors, 122 vertical npns, 41 lateral npns, and 16 substrate npns. The array also contains four 400-mA npns, over 400 diffused resistors (135 Ω to 4.8 k Ω), and two 60-k Ω pinch resistors. The Genesis 1500 runs off 1-to-12-V rails. Like the high-current npns on most arrays, the four on this chip and those on other Cherry arrays, can be paralleled.

The I²L can be programmed to use from 10 nA to 400 μ A per gate, with corresponding delays of 100 μ s to 40 ns. The f_T s of the npn transistors on these and most other Genesis 6000 arrays runs from 350 to 400 MHz. The Genesis 1500 has 30 pads and measures 123 by 140 mils. The Genesis 1100, which is 30% smaller (98 by 124 mils), features Schottky-clamped npns to ease interfacing with fast logic.

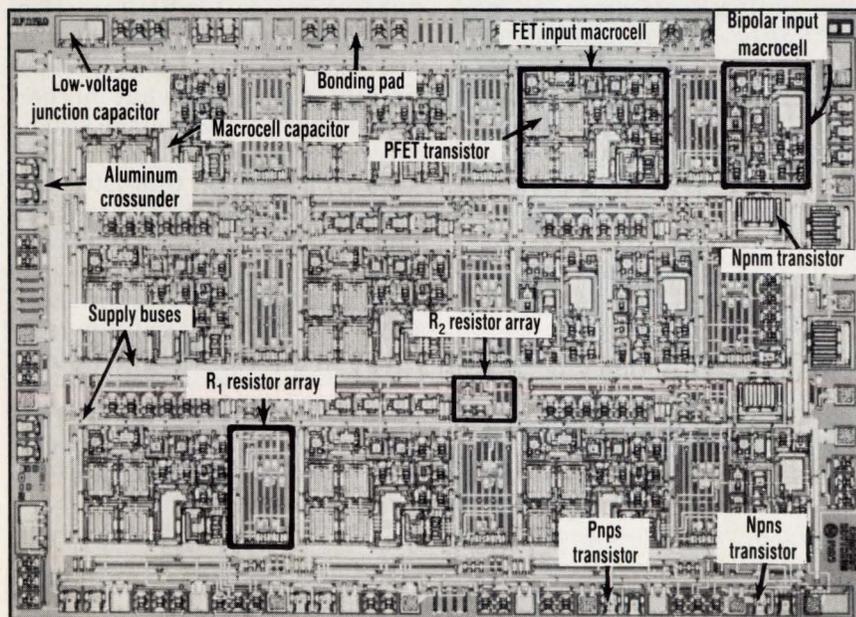
The Genesis 5000 analog tile array has 200 small-signal npns, 95 dual-collector npns distributed over 19 general-purpose analog tiles, several differential pnp input tiles, an undedicated band-gap reference tile, and eight pairs of matched npns. In addition, it contains eight 100-mA npns. Supply rails can run to 20 V.

Cherry's Genesis 7600 tile array is about the same size as the 1100 but it's built on a faster, 15-V process with an f_T of 800 MHz, permitting the use of low-power Schottky TTL. In addition, 139 ion-implanted resistors, totaling over 2 M Ω , replace the pinch resistors.

JFETs TO THE RESCUE

The RFA120, the first chip in Raytheon's RFA family of bipolar analog arrays with JFETs, does what earlier RLA arrays couldn't do: It switches analog signals accurately, easily, and fast, and supplies gain blocks with high input impedance and low input (bias) current for driving a lower-impedance load faster (see "Practical Progenitors Produce Potent Progeny," opposite).

The RFA120 can be used for a complete audio/telecommunications mixing circuit consisting of up to eight channels of input multiplexing with gain or buffering either before or after the switches. Precision gain switching can be coupled to an out-



2. TO GET LOW BIAS CURRENT op amps, analog switches, and greater speed, Raytheon added JFETs to its bipolar array process, resulting in the RFA120 array.

ANALOG ARRAYS

PRICE AND AVAILABILITY

Cherry Semiconductor's Genesis 6000 arrays come in 20- and 24-pin bat-wing small-outline ICs and 15-pin multiwatt power packages. NRE charges run \$6,000 and a typical unit price in quantities of 10,000 runs \$4. Typical prototype delivery is 12 weeks.

Raytheon's RFA120 array is available in a variety of cerDIP and plastic DIPs, as well as small-outline ICs and LCCs. NRE charges range from \$21,000 to \$25,000. Pricing, in quantities of 1,000 starts at \$5.75 each in plastic. Delivery of prototypes is six to eight weeks.

Cherry Semiconductor Corp., 2000 S. County Trail, East Greenwich, RI 02818; Bob LeFort (401) 885-3600.

Raytheon Co., Semiconductor Division, 350 Ellis St., Mountain View, CA 94043; Jim Shupenis, (415) 966-7697. CIRCLE 511

put stage that can handle at least a watt of low-distortion power, from dc to several hundred kilohertz. The device works in temperature ranges required by military specifications.

Like its RLA predecessors, the RFA120 has a gain-block-tile architecture with 12 tiles, called FET input macrocells (*Fig. 2*). Eight of the tiles dominate the array—three each in the top and bottom rows, two in the center row. They're easily identifiable by the four large green p-channel JFETs. One or two of these FETs can be used to build an analog switch with a typical on-resistance as low as 1000 Ω that can turn on in 1 μ s and off in 0.5 μ s. Adding several FETs in parallel drops the on-resistance.

The FETs also can be combined with the bipolar transistors on the tile to build an op amp with an open-loop gain of 100 dB, a bias current of 30 pA, and an offset voltage of 5 mV. Circuitry on the chip can set the operating current of the transistors at 0.1 to 200 μ A, resulting in slew rates of 0.02 to 18 V/ μ s. The latter translates

to a full-power bandwidth of about 600 kHz. Moreover, the transistors can drive a 20-V pk-pk signal across 600 Ω . Over the same range of transistor currents, small-signal bandwidth runs from about 10 kHz to about 20 MHz.

That combination of speed and bandwidth (about four to five times that of the RLAs) is a direct result of the JFET input transistors. On the other hand, the output drive—which is three times that of the RLAs—is a result of the gain blocks' output npns. The output npns are three times the size of similarly employed devices on the RLAs.

The remaining four bipolar input macrocell tiles are designed for ground-sensing input amplifiers. They're dominated by the large gray rectangular oxide capacitor, which provides op-amp compensation. Except for their higher output current, these tiles are similar to the pnp input circuits on the RLAs (ground-sensing input circuits handle common-mode voltages down to the negative rail).

All of the FET tiles may be used, without FETs, to build npn input op amps like those on the RLAs. As might be expected, typical offset voltage of these bipolar input circuits is less than that of the FET circuits (as low as 1 mV). The offset drift of the bipolar circuits typically runs 4 mV/ $^{\circ}$ C; that of the FET input circuits runs somewhat higher. Trimming the offset voltage also reduces the offset drift.

Four 100-mA npn transistors are available when 15 mA or more of output current is needed. In addition, a number of small-signal npns and pnps are distributed over the array, as well as 20-A vertical pnp (substrate) transistors. The die contains a total of 262 thin-film resistors ranging in value from 600 to 150 k Ω , for a total resistance of 7.5 M Ω . In addition, there are 18 50- Ω base (diffused) resistors. □

PRACTICAL PROGENITORS PRODUCE POTENT PROGENY

The original, four-member RLA family of analog tile arrays from Raytheon is based on a number of premises. The first is that most analog circuitry is built with gain blocks, either op amps or comparators. Second, most designers want to be able to set the gain of those blocks within a few percent—and that gain should remain constant over temperature. Third, most designs require offset voltages well below 10 mV, and many need several hundred milliamperes of output current. Fourth, while most designers still want to run their circuits from \pm 15-V rails, a few must operate from one 5-V or even lower supply voltage. Finally, most designers want low-power operation, but they also want the ability to trade off power for speed.

The RLAs are built on a standard bipolar process that supplies a maximum of 32 V between sup-

ply pins. However, the circuits operate on as little as 2 V. Raytheon added to the process precision (\pm 1%-matching, \pm 100-ppm/ $^{\circ}$ C temperature-coefficient, and no voltage coefficient) thin-film silicon-chrome resistors and a second layer of metal. The arrays range from 98 by 89 mils for the four-tile RLA40 to 189 by 123 mils for the 16-tile RLA160. The small-signal npn and pnp transistors in the tiles are partially interconnected by the first layer of metal to form gain blocks.

Using the second metal layer, users connect the gain blocks forming precise op amps or comparators—or other analog circuits—with the thin-film resistors.

Additional small-signal transistors, as well as npns that can handle up to 100 mA, are also available. The f_{TS} of the npns typically runs 400 MHz, about that of the Cherry arrays.

HOW VALUABLE?

HIGHLY	550
MODERATELY	551
SLIGHTLY	552

CIRCLE

ONE BOX HOLDS SEVERAL TOOLS.

DIGITAL SYSTEM ANALYZER HANDLES MULTIPLE ROLES

JOHN NOVELLINO

Imagine a scenario in which your digital system design goals aren't limited by the availability or price of the needed microprocessors and associated chips. Even the design process, as complex as it is, is well supported by automated design tools. Instead, your system's performance and complexity are restrained by your ability to verify the design and debug and optimize the system. Your problem could be solved by combining the functions of the conventional standalone tools used by digital designers into one instru-

ment that makes it easy to quickly acquire and examine the needed data.

The Logic Analyzer Division at Tektronix considered this scenario and decided that it occurred enough to warrant a new approach to digital system analysis. The company came up with the Prism 3000 Series, a tightly integrated set of tools focused squarely on system analysis tasks: software or firmware debug and optimization, hardware-software integration, timing analysis, and digital waveform analysis. All of the functions designers and integrators need to perform

these tasks—emulation; state, timing, and performance analysis; and microprocessor disassembly—are accomplished by one card that plugs into a modular Prism 3000 mainframe (*Fig. 1*).

All the information designers need can be shown conventionally on individual displays, or data can be combined into an integrated display for comparison and analysis. The advantage of this combined presentation is that designers need not mentally integrate information from several instruments and a terminal screen. The system's multiple display for-



1. THE PRISM 3000 SERIES packs several digital system-analysis functions into one instrument. Three versions are available, including one portable model.

DIGITAL SYSTEM ANALYZER

mats include state, timing, waveforms, histograms, listings of microprocessor control code, and breakpoints.

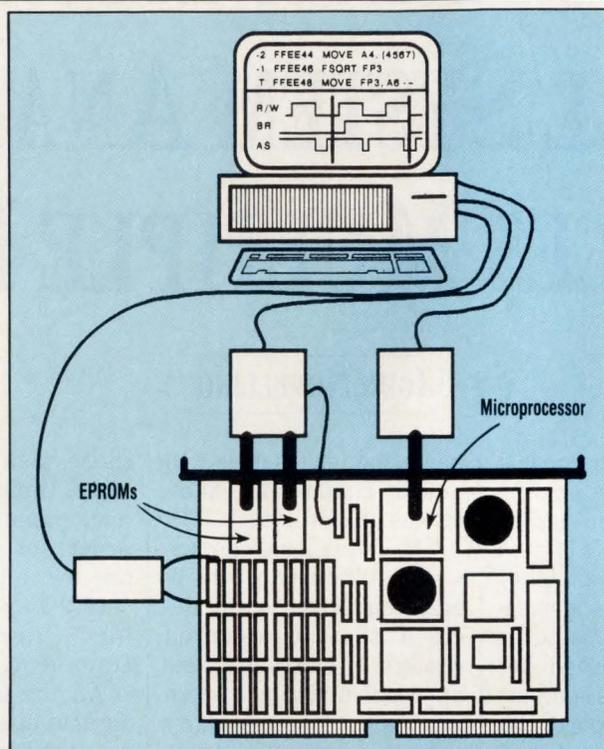
What makes it all work, though, is that the data is automatically time correlated. State, timing, and microprocessor events are shown in their correct time relationships. Designers don't have to set up complex triggering sequences and links between different instruments—a job that can be nearly impossible because of the varying time offsets between instruments.

To maintain the timing relationships, Tektronix moved the Prism 3000's logic analysis front end out of the mainframe and into the probes. Clocking and data latching are performed by ASICs located in the probes (Fig. 2). In addition, the analyzer uses

only one system clock, and an internal bus called TEKLink supplies intermodule triggering for multiprocessor systems. Four two-slot expansion mainframes can be added to the basic two-slot unit, making it possible for up to 10 application modules to run simultaneously.

The first modules available in the Prism 3000 Series, the MPM and MPX, are aimed at the integration of microprocessors, software, firmware, and supporting hardware. The MPM offers 64-channel support for 8- and 16-bit microprocessors, and the 96-channel MPX also handles 32-bit devices. Otherwise, the cards are the same.

The MPM/MPX state analysis sec-



2. BY MOVING THE CLOCKING and data-latching functions to the probe tips, Tektronix maintained the time correlation of all data acquired by the Prism 3000.

tion accommodates clock rates up to 33 MHz and has an 8-kword memory depth. State machine triggering includes eight word/range recognizers, eight counter-timers, eight trigger states, and four event lines to other modules. The state section also has links to the unit's Prototype Debugging Tool (PDT). The timing section has nine 200-MHz channels with 2-kword-deep memories. Both sections time-stamp the acquired data. Besides allowing for time correlation between the state and timing sections, TEKLink lets the two sections arm, synchronize, and cross trigger each other.

The PDT is a key ingredient of the Prism 3000. It supplies emulator-like control of the system under test without the intrusiveness of conventional emulators. Rather than rely on the traditional technique of emulating the microprocessor, the PDT replaces the target system's EPROMs. As a result, the microprocessor runs at full speed, with no wait states. Together with a microprocessor analysis section on the MPM/MPX card,

the PDT sets complex hardware breakpoints. It employs the 8-kword memory as a trace buffer.

The Prism 3000 software and probe packages perform mnemonics disassembly for all popular microprocessors without the need for personality modules. If the proper probe adapter is installed, the software automatically loads and configures at power up. During disassembly, designers can take advantage of the subroutine display format to look at a state table and quickly determine how much time the processor is spending on each subroutine in a program.

The MPM/MPX module features four performance analysis modes. The state overview and single-event measurement modes give designers an overview of the system's

operation. The other two modes—real-time timing overview and real-time count overview—measure code execution timing and event occurrences, respectively.

The Prism 3000 Series is available in three types of mainframes. One is a two-slot unit with separate keyboard and high-resolution monitor. Another is a similar mainframe but with a fold-down electroluminescent flat-panel display that makes it easy to move the instrument.

The third version takes the form of a traditional portable logic analyzer, with an integral display and front-panel keyboard controls. The portable unit maintains all of the capabilities of the two larger mainframes, including a 3.5-in., DOS-format disk drive, and an RS-232C port for use as a communications link or as an output to a serial plotter. □

PRICE AND AVAILABILITY

The base price of a Prism 3000 Series system is \$8,400. Deliveries will begin in August.

Tektronix Inc., Logic Analyzer Div., P.O. Box 12132, Portland, OR 97212; (800) 245-2036. **CIRCLE 512**

HOW VALUABLE?

HOW VALUABLE?	CIRCLE
HIGHLY	553
MODERATELY	554
SLIGHTLY	555

PRECISION INSTRUMENTATION AMPLIFIER BREAKS PRICE/PERFORMANCE BARRIERS

FRANK GOODENOUGH

The IC instrumentation amplifier, unlike its sibling the op amp, hasn't become a widely used component. According to Linear Technology, the reason is a combination of cost, performance, and size.

But the LT1101 may change this trend. The chip offers gain and offset specifications an order of magnitude better than devices that cost two to three times as much, and it combines features previously unavailable in one instrumentation amplifier (IA).

For instance, it is a true single-supply amplifier and micropower device. All specifications are met when it runs from one 5-V supply as well as from ± 15 V. During single-supply operation, both input and output voltages can swing within a few millivolts of ground.

Unlike most single-supply amplifiers, the output sinks current while swinging to ground—therefore no power-grabbing pull-down resistors are needed. The chip requires only 130 μ A of supply current, and it can operate at supply voltages as low as 1.8 V (one lithium or two Nicad cells). It runs equally as well from the ± 15 -V rails, too.

Furthermore, because the LT1101 has pnp input transistors, it can handle 30 V of differential input voltage without an increase in bias current. Some instrumentation amplifier ICs can't take more than 10 V, and their bias currents notably increase if the differential input exceeds 1.3 V. Also, because the chip's architecture includes two op amps, the LT1101 has no output offset voltage errors (see the figure). Ordinarily, at low gains IA output offset can represent a large portion of the total dc error.

Another important feature is that the chip has precise, pin-strappable gains of 10 and 100 without the need for external resistors. These gains are set internally by laser-trimmed thin-film resistors. The chip comes in 8-pin miniDIPs and TO-99 metal

cans, not 16- to 18-pin DIPs that are used by many IAs.

About 40 specifications truly define an instrumentation amplifier, but the most important are those built around gain and offset voltage. The LT1101 also excels here, starting with gain error as set by the internal resistors. With ± 15 -V supplies, gain error for the lower grade C model is a maximum of 0.06% at a gain of 10 while driving 2000 Ω with ± 10 V.

The error is the same at a gain of 100 driving 50k Ω . The maximum error increases to 0.07% at a gain of 100 as it drives 2000 Ω . These specs improve about 25% for the higher A-grade amplifier.

Gain errors increase slightly when the chips run off 5-V supplies. As 0.1 to 3.5 V is put across a 50k Ω load at a gain of 100, the gain error for the C version is a maximum of 0.075%. The gain error drops to 0.06% at a gain of 10. In the A version, these maximum errors are 0.05% and 0.04%, respectively. These specifications range from two to 10 times better than other available devices.

Because many systems have some form of gain adjustment, changes in gain can represent a more critical specification. The LT1101's gain temperature coefficient runs under 9 ppm/ $^{\circ}$ C for all versions. Gain nonlin-

earity can cause significant distortion in wide dynamic range signals. It ranges from 7 ppm for the A version at a gain of 10 and driving 50k Ω from 5-V rails, to 75 ppm for the C model under similar conditions at a gain of 100.

Maximum offset voltage at 25 $^{\circ}$ C is under 220 and 160 μ V for the C and A versions respectively, regardless of operating conditions. Similarly, maximum offset drift is under 2 and 2.8 μ V/ $^{\circ}$ C, respectively. If the chip has a weak spot, it's in the common mode rejection ratio (CMRR). At a gain of 10, the CMRR runs a minimum of 82 dB for the C version and 84 dB for the A version.

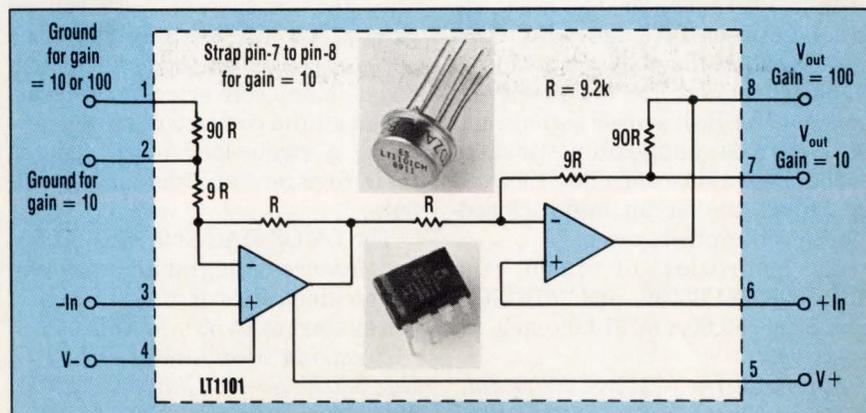
These figures rise to 98 and 100 dB at a gain of 100. Several available IAs specify a 10 to 20 dB greater CMRR.

Other significant specifications include an input offset voltage of 50 mV, input offset current of 130 pA, and voltage and current drift of only 0.4 mV and 0.7 pA per $^{\circ}$ C. Input noise at 0.1 to 10 Hz is 0.9 mV peak-to-peak, and input noise current is 2.3 pA peak-to-peak.

The unit price of the LT1101 runs \$4.95 in quantities of 100.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487; Bob Scott, (800) 637-5545.

CIRCLE 307



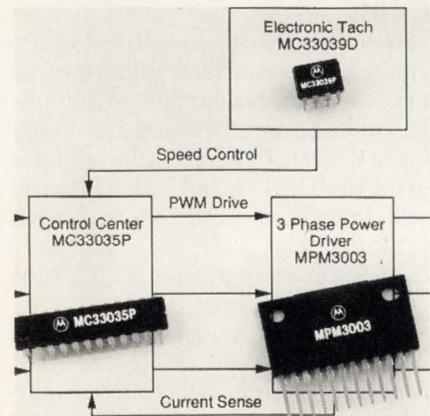
THE ARCHITECTURE OF THE LT1101 instrumentation amplifier IC includes two op amps, so the chip has no output offset voltage errors.

ONLY THREE ICs BUILD BRUSHLESS DC MOTOR SPEED-CONTROL SYSTEM

With just two DIPs and a SIP from Motorola, a complete control system for a 0.25-horsepower motor can now be built for under \$20.

The DIPs, the MC33035 and MC33039, are a second-generation pulse-width-modulation (PWM) brushless dc motor controller IC and an electronic tachometer, respectively. The third device, the MPM3003, contains six isolated (2000 V), 60-V, 10-A (continuous) power MOSFETs. The controller contains all of the functions required to build an open-loop three- or four-phase speed control system.

The MOSFETs in the MPM3003 power module, called an ICePAK, form a complementary three-phase bridge (three half bridges). The upper legs of the bridge are built of p-



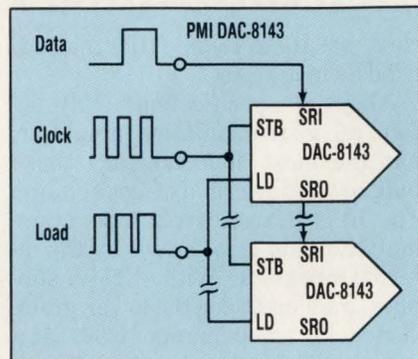
channel FETs, the lower legs of n-channel FETs. The 2000 V rms of isolation between FET die and the aluminum tab of the package make the IC easy to mount. The tachometer IC looks at the Hall sensor signals and develops a dc voltage proportional to speed. Fed to the controller, the voltage turns the circuit into a closed-loop speed control system.

In quantities of 1,000, the MC33035, MC33039, and MPM3003 cost \$2.88, \$0.60, and \$14.08 each, respectively.

Motorola Inc., 7402 S. Price Rd., PR340, Tempe, AZ 85283; Bob Benzer, (602) 897-3840. **CIRCLE 308**

FRANK GOODENOUGH

DAISY CHAIN DOZENS OF CURRENT DACs ON THREE SERIAL LINES



Precision Monolithics' DAC-8143 daisy-chain d-a converter needs only three lines—Data, Clock, and Load—to connect and drive as many of the 12-bit multiplying, current output converters as required by designers. The digital inputs to the daisy-chain converter look identical to the 7543's inputs. The clock shifts a 12-bit word on the data line into the chip's 12-bit shift register. Furthermore, when the register's data is fully updated, a strobe pulse on the Load line transfers the data to the converter register, which changes the analog output.

The DAC-8143 goes one step further. As a new word is moved into the shift register on pin 7, the current word is shifted out on the 16-pin DIP's one extra pin (pin 6). If this pin is connected to pin 7 of another DAC-8143, the outgoing word from the first converter is clocked into the second, and its current word can be clocked into a third converter. This process continues until the system has as many converters as it needs. When all the converters have a new word, a strobe-load pulse updates their registers and the analog outputs.

The CMOS DAC-8143 runs off 5 V and features integral and differential nonlinearities of $\pm 1/2$ LSB. Unit prices start at \$6.53 in lots of 100.

Precision Monolithics Inc., P.O. Box 58020, Santa Clara, CA 95052; Dave Capella, (408) 562-7459.

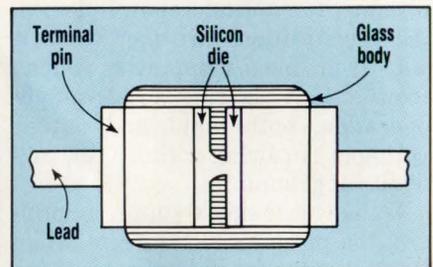
CIRCLE 309

FRANK GOODENOUGH

WAFER BONDING PROCESS ADDS STRENGTH TO SMALL-SIGNAL DIODES

The construction of small-signal glass diodes, such as the standard 1N4148, has hardly changed in over a decade. However, Unitrode took direct wafer bonding (DWB), which was a laboratory process at many companies for years, and came up with a more rugged diode for the DO-35 package. The new DWB process is patented and the diodes, called Unibond, aim at military applications. In fact, a military specification (MIL-S-19500/578) was generated to describe the chip.

Unlike conventional DO-35 diodes, where a silver button is held mechanically against a planar pn junction, p-



and n-type silicon are atomically bonded together at 1000° C with diffusion of a pn junction occurring at the same time.

The new diodes are free of cold start and intermittence problems, and loose particles. These headaches are common when conventional diodes are exposed to the rigors of the military environment and military packaging—including conformally coated, potted, multilayer pc boards. There were no failures among the packaged devices that went through a series of environmental tests.

The Unibond 1N6638 has a breakdown voltage of 150 V and a capacitance of 2 pF at 1 MHz. It recovers in 4.5 ns, and its forward voltage drop at 200 mA is 1.1 V. The respective specifications for the 1N4148-1JTX are 75 V, 5 pF, 5 ns, and 1.2 V. The 1N6638JTX costs \$2.70 each in lots of 1,000.

Unitrode Corp., 580 Pleasant St., Watertown, MA 02172; (617) 926-0404. **CIRCLE 310**

FRANK GOODENOUGH

NEW PRODUCTS

INSTRUMENTS

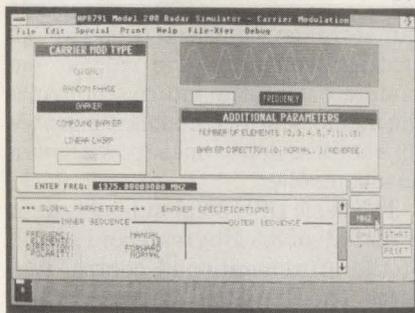
FREQUENCY-AGILE SIGNAL SIMULATOR EASES COMPLEX COMMUNICATION TESTING

Exotic, agile test signals for advanced electronic warfare-threat simulation, radar-target simulation, and secure communications are generated by the HP 8791 frequency-agile signal simulator (FASS) from Hewlett-Packard. The system's model 10 hardware platform provides an agile carrier that switches in less than 250 ns over a 10-MHz-to-3-GHz agile bandwidth.

The system's frequency resolution is 0.125 Hz. The carrier also has a direct-digital synthesis-modulation capability with a 40-MHz instantaneous bandwidth. This modulation capability permits advanced spread-spectrum formats like chirps, Barker codes, maximal-length sequences, QAM, and FSK.

For microwave applications requiring carriers above 3 GHz, band-oriented up-converters that provide about 2 GHz of agile bandwidth are available to 18.5 GHz. Broadband and millimeter-wave up-converters are available on a custom basis.

The system's software strategy



includes flexibility that adapts the system to a variety of applications and offers customization for particular user needs.

The HP 8791 model 10 FASS hardware platform goes for \$185,000. The signal-generator, radar-simulator, and waveform-generation software packages go for \$6000, \$11,000, and \$6500, respectively. Delivery is from stock.

Hewlett-Packard Co., 1920 Embarcadero Rd., Palo Alto, CA 94303; call local Hewlett-Packard sales office.

CIRCLE 311

DAVID MALINIAK

SIGNAL GENERATOR AND DEVIATION METER SERVES FIELD APPLICATIONS

Specifically designed to boost productivity in ATE and field-service applications, the model 2407 signal generator and deviation meter from Wavetek covers a frequency range of 0.01 to 550 MHz. An IEEE-488 interface is included as



standard equipment.

The instrument's alphanumeric display includes crisp, clear directions regarding operation of the embedded diagnostic and calibration routines, which nearly eliminates the need for operator training.

State-of-the-art autocalibration is also provided. This includes the ability to initiate calibration over the IEEE-488 bus for an entirely automatic operation and service process. Access to internal error-correction data is given through the bus to track aging and to facilitate scheduled maintenance instead of waiting for an emergency.

The unit is well suited for field-service applications. Its internal modular construction accepts field-installable options.

In operation, the instrument combines fractional division single-phase-lock-loop techniques with direct digital synthesis for a wide variety of frequency-step sizes. The unit offers an rf output of +13 to -127 dBm, and exhibits an output accuracy of ± 1.5 dB.

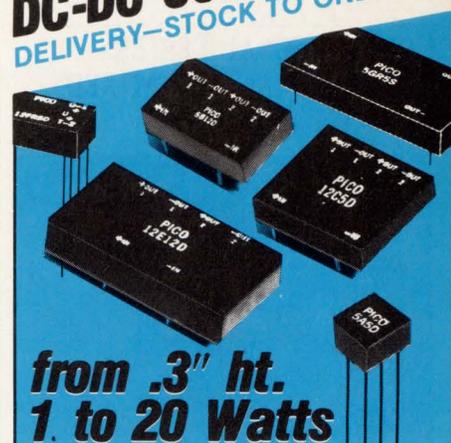
The model 2407 signal generator/deviation meter costs \$4595. Delivery is from stock.

Wavetek RF Products Inc., 5808 Churchman Bypass, Indianapolis, IN 46203-6109; (800) 851-1202.

CIRCLE 312

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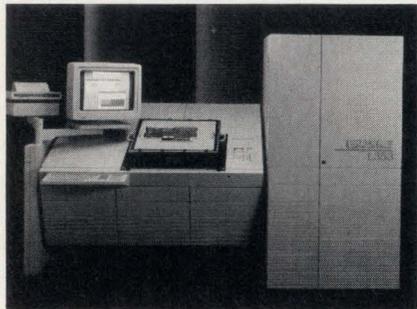
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CIRCLE 178

COMBINATIONAL TESTERS INCLUDE SCAN AND MIXED SIGNAL CAPABILITIES



A family of VLSI board test systems adds scan testing capability to the traditional in-circuit and functional test approaches of combinational testers. The four members of Teradyne's L300 series also introduce a parallel multiprocessor analog subsystem that helps cut overall test time to 30 s or less for a typical mixed-technology VLSI board.

The L353 (576 channels or 3,024 pins) and L357 (1,152 channels or 6,048 pins) use low-power CMOS channel cards that perform high-reliability combinational testing to 20 MHz. Employing the same bipolar channel electronics of the earlier L290 machines, the L393 and L397 handle 40-MHz functional testing on up to 576 or 1,152 channels, respectively. Interleaving any pair of adjacent channels doubles the test rate to 80 MHz.

The distributed-processor architecture is based on a high-performance VAXstation 3200 supervisory processor with up to 16 Mbytes of main memory and a graphical workstation interface.

For testing and diagnosing interconnect faults in boundary-scan circuitry, the L300 family includes a Boundary Scan Diagnosis software module.

Typical configurations of the L35x system cost from \$500,000 to \$1 million; typical L39x systems cost are \$800,000 to \$1.5 million. Deliveries will begin in the fourth quarter.

Teradyne Inc., 321 Harrison Ave., Boston, MA 02118; (617) 482-2700.

CIRCLE 313

JOHN NOVELLINO

TOOL SPEEDS WAVEFORM ACQUISITION IN E-BEAM PROBING SYSTEMS

Engineers can anticipate faster IC fault diagnosis and more efficient design verification with the Logic Analyzer Tool from Schlumberger Technologies. Based on the functionality and user interface of a standard logic analyzer, the Logic Analyzer Tool consists of multisampling hardware and software that overcomes extended pattern length and repetition rate limits inherent in electron-beam probing.

Working with Schlumberger's IDS 4000 and IDS 5000 e-beam probing systems, the tool uses new sampling strategies that fully exploit the available detector bandwidth. These techniques greatly reduce typical logic waveform acquisition times. Many logic waveforms can be acquired in a few seconds.

As a result, users can diagnose chips with test patterns that are up to two orders of magnitude longer than was previously possible. Furthermore, users can interactively manipulate large volumes of data and, for the first time, diagnose ICs with intermittent failures. Any engineer familiar with logic analyzer operation can use the Logic Analyzer Tool without special training.

The tool employs multiple beam pulses for each test-pattern repetition rather than one beam pulse, as with conventional probing methods. This simple technique is done with a novel pipelined memory and a signal-processing architecture that makes it possible for up to eight simultaneous sample-memory transactions to occur in parallel. Thus users can handle test patterns one to two orders of magnitude longer than was previously possible.

Purchased separately, the Logic Analyzer Tool costs \$45,000; as a retrofit onto an IDS 4000/5000, it goes for \$50,000. Deliveries will begin in October.

Schlumberger Technologies Inc., ATE Div., 1601 Technology Dr., San Jose, CA 95110-1397; (408) 437-5000.

CIRCLE 314

JOHN NOVELLINO

TARGET EMULATOR EASES THOROUGH TESTING OF SCSI SYSTEMS

The DSC-302 target emulator and error generator from Ancot can check the margins, sensitive bus timing, and many of the exotic conditions that occur on the SCSI bus. The first version of the DSC-302 targets the testing of random-access devices, such as disk drives.

Housed in a package about the size of a 5.25-in. disk drive, the instrument is configured to appear as a 128-kbyte disk drive when attached to the SCSI bus. In addition to responding to the standard SCSI disk functions, the system can be programmed to simulate a range of commonly seen errors.

Along with the SCSI port, the system has a serial communications port to talk with the host system (a terminal or PC, for example). Users



can store device characteristics, operating sequences, and various parameters within an internal nonvolatile memory, which makes it possible for the DSC-302 to operate without a host controller.

The basic DSC-302A supports data transfers of 3.3 Mbytes/s and has all of the aforementioned control features. The DSC-302B adds hardware-assisted error generation and handshake delay capabilities that make it possible for designers to perform realistic testing for margins and timing sensitivities. Tests for arbitrary parity error situations, incorrect phase sequences, subtle arbitration problems, and other problems can also be performed.

The DSC-302A is priced at \$1960; and the DSC-302B costs \$2450. Delivery is in 30 days.

Ancot Corp., 1755 E. Bayshore Rd., Suite 18A, Redwood City, CA 94063; (415) 363-0667.

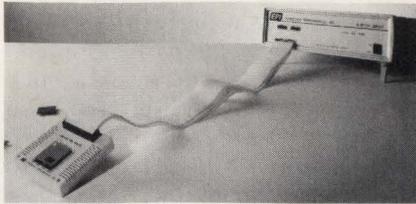
CIRCLE 315

DAVE BURSKY

NEW PRODUCTS

INSTRUMENTS

IN-CIRCUIT EMULATOR SUPPORTS AM29000



Designed to streamline the system-integration process, a full-featured in-circuit emulator supports the development of embedded systems based on the Am29000 32-bit RISC microprocessor. The emulator, part of EPI's EPIC 29000 software- and hardware-development system, runs at the full speed of the Am29000 and provides such capabilities as memory test and scope loop commands. Users can examine and edit both memory and registers in many formats, set unlimited software breakpoints, single-step, and continue their program without restarting. Up to 1 Mbyte of overlay memory is available to replace or supplement target memory, debug application code, or run diagnostics programs. In addition to the in-circuit emulator, the System 29000 hardware-development station includes a logic analyzer, an overlay-memory module, a real-time histogrammer, and software.

*Embedded Performance Inc.,
3707 Williams Rd. #2, San Jose, CA
95117; (408) 244-7900. CIRCLE 326*

MULTIMETER SPORTS DUAL DISPLAY

Priced at under \$600, the Fluke 45 digital multimeter is one of the first in the industry to be built with a multifunction dual display. A wide variety of different measurement combinations can be viewed on the bright vacuum-fluorescent primary and secondary displays, particularly useful when two different measurements are required from the same signal. The Fluke 45 is a 5-digit, 100,000-count meter with additional selectable resolutions of 30,000 and 3000 counts. It has a basic six-month V dc specification of 0.02%. Basic one-year accuracy specifications are:

0.025% V dc, 0.2% V ac, 0.05% A dc, 0.5% A ac, 0.05% Ω , and 0.05% Hz. The instrument is equipped with an RS-232-C interface for PC instrument applications. A built-in compare function for easy in-tolerance testing shows a high-low-pass evalu-

ation on all components. An IEEE-488 interface is optional. Available immediately, the list price is \$595.

*John Fluke Mfg. Co. Inc., P.O.
Box C9090, Everett, WA 98206; (800)
443-5853, ext. 33, or (206) 347-
6100. CIRCLE 327*

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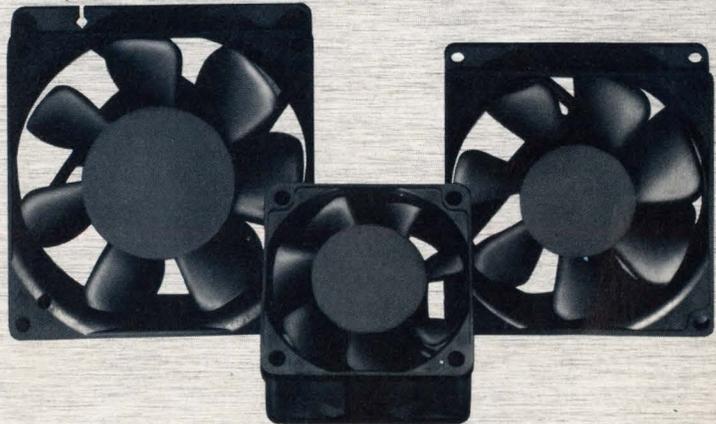
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CIRCLE 151

GATE-ARRAY FAMILIES OFFER HIGH I/O COUNTS PLUS ECL OPTION



With three families of CMOS or biCMOS gate arrays, the latest semicustom products from Hitachi cover most system requirements. One family consists of the HG62F high-I/O-count CMOS arrays, which pack about 20% to 30% more I/O lines than most other arrays with about the same number of gates. The second, the HG21T series, is a group of biCMOS arrays with both ECL- and TTL-compatible I/O lines. Last in the trio is a biCMOS family, the HG29A, with high-current-drive TTL- or CMOS-compatible I/O buffers.

The high I/O count arrays include three chips with up to 7488 gates and 192 I/O lines. The array output buffers can handle loads of up to 24 mA, or 48 mA if two are paralleled. Both biCMOS families use embedded bipolar transistors to deliver internal gate delays of 450 ps, and both families can operate at clock frequencies to 160 MHz. The HG21T ECL/TTL I/O family has one member with about 3000 gates and 90 I/O lines that can each be configured as TTL- or ECL-compatible. The HG29A family is similar to the HG21T series, but it contains 102 I/O lines that are LS-TTL compatible and have totem-pole or three-state open-collector outputs.

In 10,000-unit quantities, the HG62F chips cost \$8 to \$15 depending on the chip and package. In 5,000-unit lots, the HG21T30 sells for \$125 in a 120-lead PGA package, while the HG29A32 is priced at \$75 in the same quantity and package. Nonrecurring engineering charges are \$20,000 to \$60,000 for all families.

Hitachi America Ltd., 2000 Sierra Point Pkwy., Brisbane, CA 94005; Tom Wong, (415) 244-7141.

CIRCLE 316

DAVE BURSKY

RAMDAC DUO COVERS WIDEST BANDWIDTH AND LARGEST COLOR CHOICE

A pair of triple digital-to-analog converters with on-chip video-palette RAMs offer designers a choice of the widest bandwidth of any CMOS RAMDAC or the largest on-chip color palette. The Brooktree Bt468 pushes bandwidth to 200 MHz, fast enough to generate 1600-by-1200-pixel images. Its companion, the Bt460, offers the largest color palette—512 words by 24 bits—and operates at a maximum video data rate of 135 MHz.

Both chips include a 16-by-24-bit overlay color palette, a three-color 64-by-64-pixel cursor palette to hold a user-definable cursor, and a three-color full-screen (or full window) cross-hair cursor. Using software control, designers can configure the converters on either chip into a one-channel RAMDAC that employs the 24-bit-wide palette as an input to achieve 24-bit true-color images. Red, green, and blue video outputs from either chip are RS-343A compatible and can directly drive doubly-terminated 50- or 75-Ω coaxial cable.

The Bt468 contains a 256 word-by-24-bit color palette that feeds the 8-bit color values to each of the three d-a converters. That makes it possible for 256 simultaneous colors to be displayed from a total palette of 16 million. Providing more simultaneous colors, the Bt460 doubles the depth of the color palette and adds multiplexed pixel ports (1:1, 4:1, or 5:1) and 1-to-16X integer zoom support.

The Bt460, which is housed in a 132-lead-pin-grid-array package, operates off 5-V power and consumes less than 2-W at 135 MHz. A 145-lead PGA package houses the Bt468, and the chip consumes about the same power as the Bt460. In 100-unit lots, Bt460 prices start at \$227 for an 80-MHz version and go up to about \$260 for the 135-MHz chip. Prices for the Bt468 aren't set yet.

Brooktree Corp., 9950 Barnes Canyon Rd., San Diego, CA 92121; Allyn Pon, (619) 535-3464.

CIRCLE 317

DAVE BURSKY

AI CHIP EMPLOYS NEURAL NETWORK

Incorporating a digital hardware neural network, an artificial intelligence IC processes fuzzy data, such as inaccurate, noisy, or otherwise variable data, to perform pattern recognition. Called the MD1210 Fuzzy Set Comparator, the device can be taught to recognize patterns without the use of software algorithms or other preprogramming. Comparison functions are handled by the neural network. The MD1210 can learn or compare data at a rate of 20 MHz. A single MD1210 can simultaneously compare eight unknown data streams to one known data stream, or eight knowns to one unknown. As many as 32 devices can be used together by means of an expansion bus to provide simultaneous comparison of 256 patterns against a single input. Packaging options include 68-pin PLCCs and 40-pin DIPs. The chip sells for approximately \$38. An evaluation kit is available for \$250.

Micro Devices, 5643 Beggs Rd., Orlando, FL 32810; (407) 299-0211.

CIRCLE 328

SRAM ACHIEVES 9-NS OUTPUT ENABLE

Designed for cache-memory applications in high-end 80386-based PCs and workstations, an 8k-by-8-bit static RAM boasts an access time of just 25 ns and an Output Enable of 9 ns — one of the fastest in the industry. A fast Output Enable significantly improves the operation of a cache subsystem by allowing the processor to run at its full speed.

The fully CMOS part, designated the V63C64, can be interfaced with integrated cache controllers such as the Austek A38125 and A28285, as well as Intel's 82385. The device also has two chip-enable inputs for easy memory expansion. Parts are available now in 300-mil plastic DIPs. When sold in volume quantities, it is priced at \$17.

Vitellic Semiconductor Corp., 3910 N. First St., San Jose, CA 95134; (408) 433-6000.

CIRCLE 329

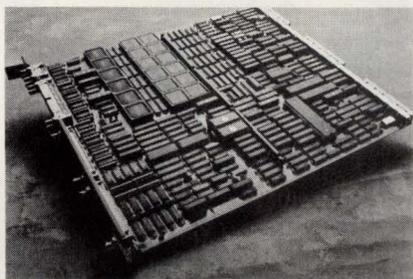
NEW PRODUCTS

COMPUTER BOARDS

BOARD SPEEDS DISK-DRIVE CONTROL FOR SUN, SILICON GRAPHICS WORKSTATIONS

Up to 1.6 Gbytes of formatted storage at sustained data-transfer rates of 15 Mbytes/s are now possible for Sun, Silicon Graphics, and other high-performance workstations. According to Maximum Strategy Inc., its Strategy SM disk controller is the world's fastest board-level disk controller for the Fujitsu 2380A 8-in. disk drive.

The controller consists of one 9U-by-400-mm plug-in board for mounting in a workstation's VME backplane. Support can be for one or two drives, each supplying a formatted storage capacity of 800 Mbytes.



Included in the controller is a standard VME interface, which supplies control, status, and data to a VME-based host. It also contains a High Speed Interface (HSI) data channel with both TTL and ECL connections. The TTL port is on the user-defined pins of the P2 connector. The ECL port is the same HSI channel designed into the company's Strategy 1 and 2 disk-array controllers.

The board automatically avoids flaws noted in the manufacturer's list of defects as well as those it discovers or that develop over time. Data integrity is further enhanced by a powerful 48-bit error-correction polynomial, which is stored with every sector written to disk. The controller incorporates error detection for all internal data paths and memories.

The Strategy SM disk controller costs \$12,000 in single quantities. Deliveries are from stock.

Maximum Strategy Inc., 1650-B Berryessa Rd., San Jose, CA 95133; (408) 729-1526. CIRCLE 318

DAVID MALINIAK

VME/VXI CARD DELIVERS 16-BIT, 200-KSAMPLE/S D-TO-A CONVERSION

An 8-channel VME/VXI data acquisition board from Analogic Corp. digitizes analog inputs at 200,000 conversions/s with 16-bit resolution and accuracy. Built on a 6U VME card (a B-size VXI card), the unit features a common mode rejection ratio greater than 100 dB at 60 Hz. The DVX 2502 is the company's first offering in a series of I/O boards that are targeted for real-time data acquisition in the VME/VXI environment.

The eight differential input channels are multiplexed to an instrumentation amplifier, which is followed by a fast programmable-gain amplifier. The amplifier's gain is dynamically selected on a channel-by-channel basis without degrading the system's accuracy or measurement rate. A 1,000-word FIFO buffer stores the converted signals to ensure data continuity during potential gaps in the direct memory access data transfer.

The converter output is also available on a standard VXIbus P2 connector for double-byte transfer to adjacent slots.

The system noise that's referred to the input over a 700-kHz equivalent noise bandwidth is 0.5 LSB \pm 30 μ V rms. The output has no missing codes and monotonicity is guaranteed from 0 to 50°C. The board's non-linearity of \pm 0.003% of full scale and -96-dB distortion at 10 kHz ensure true 16-bit accuracy.

A Unix V software driver, included as standard, supplies operational control of the board. The driver includes all the commands needed to configure and control the card's functions and any associated multiplexer system.

The DVX 2502 has a unit price of \$3,700; quantity pricing is available. Delivery is eight to ten weeks after receipt of order.

Analogic Corp., 8 Centennial Dr., Centennial Industrial Park, Peabody, MA 01961; (508) 977-3000. CIRCLE 319

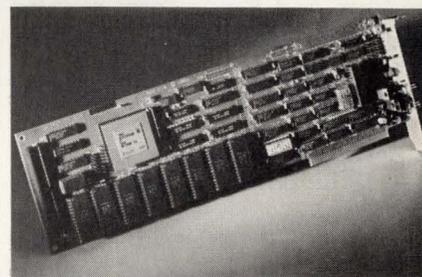
JOHN NOVELLINO

DSP-BASED ACCELERATOR COMBINES 33 MFLOPS WITH SOFTWARE SUPPORT

A 33-MFLOP accelerator board from Sonitech International Inc. targets compute-intensive applications such as graphics. The Spirit-30 digital-signal-processing (DSP) board, which supports various hosts and bus architectures, features a menu-driven, window-based software-development environment that includes a DSP library, C compiler, debugger, and real-time operating system.

At the Spirit-30 board's core is the Texas Instruments TMS320C30 digital-signal processor. The DSP board contains 128 kbytes of dual-access, 25-ns static RAM that both the board and the host can access. A daughter-board supplies an additional 512 kbytes of memory. Furthermore, data-transfer rates as high as 2 Mbytes/s are attainable.

To simplify application development, the board comes with a menu-driven, window-based evaluation, debugging, simulation, and real-time DSP software environment called EDSP. Optional support includes a DSP library (DSPL); a TMS320C30 C compiler, assembler, linker, and simulator; and the SPOX



real-time operating system. The DSPL has over 35 optimized DSP and utility modules.

The Spirit-30 system, which runs on IBM PC/XT/AT, Macintosh, PS/2, VMEbus, Multibus II, and Q-bus computers, costs \$2,495. Purchased separately, the EDSP software goes for \$495, and the DSPL costs \$295 in C and \$985 in source code.

Sonitech International Inc., 83 Fullerbrook Rd., Wellesley, MA 02181; (617) 235-6824. CIRCLE 320

LISA GUNN

NEW PRODUCTS

COMPUTER-AIDED ENGINEERING

PC-BOARD AUTOROUTER MAXIMIZES DESIGNS FROM START TO FINISH

The Rip-N-Route software from P-CAD is a 100% completion pc-board autorouter with an optimizer to ensure maximum design manufacturability. The package is fully integrated with the Master Designer, also from P-CAD. As a result, designers can easily move between board-layout editing and autorouting.

Rip-N-Route reaches its potential by routing all layers at once. Alternatively, users can specify any layer pair they wish to route together. With another feature, users can confine the routing to just one specified window. Also, a hierarchy of net classification can be used to specify routing priority. Combining a corner-costing technique with the digital-routing layer specification ensures the straightest possible signal path.

The autorouter fully supports surface-mount technology, including any mix of interstitial and through-hole vias. For surface-mount designs, the automatic via fan-out function (stringer generation) can save hours of manual editing. Other features that come standard include uniform and nonuniform routing grids, multiple trace widths, and in-plane connectivity recognition.

When used with the Master Router, the software can produce rounded corners. To maximize channel usage, 45° beveling can be specified either as a post-process or during routing. The fully interruptible router can reenter a design at any point, so prerouted nets can be fixed in place.

The Rip-N-Route package can be added to the Master Router for \$1,995 (\$1,495 if purchased before September 15). The Total Route package, which includes the Master Router, Rip-N-Route, and an auto-place routine, is available for \$6,495. Maintenance agreements can be purchased directly from P-CAD.

P-CAD, a Cadam Co., 1290 Parkmoor Ave., San Jose, CA 95126; (408) 971-1300.

CIRCLE 321

RICHARD NASS

DIGITAL TIMING ANALYZER SIMPLIFIES MANY PHASES OF THE DESIGN PROCESS

The latest addition to Motorola's set of CAE tools is the TrailBlazer digital timing-analysis system. The package analyzes a circuit's ac timing characteristics and generates the critical-path timing information for various stages in the design process, which include timing verification, floorplanning, placement, and routing. The timing information also drives test-pattern verification software for skew analysis.

Menu-driven and interactive, TrailBlazer accepts the standard electronic-design interchange format (EDIF) 2.0.0 net lists as well as CMOS, ECL, and biCMOS technologies. Rather than considering every timing path in the circuit, the package uses a block-oriented method for static-timing analysis so the software computes only the delays for the fastest and slowest paths. Consequently, computation time is shorter at higher gate counts and the tool can approximate the timing of asynchronous feedback loops.

The information gained in this analysis can then be used in the development stage of the design process. This follows a functional simulation to evaluate the design's timing performance based on statistically generated delays.

TrailBlazer checks setup-time (time required for a signal to stabilize prior to clock activation) and hold-time (time required for a signal to stabilize after clock activation) on every state element in the circuit to ensure that all elements interact as predicted. These checks, as well as the critical-path analysis and clock-distribution skew, can be modified with a user-defined variance factor to compute the relative minimum and maximum delays.

Available for Apollo, Sun, and DEC VAX platforms, TrailBlazer costs from \$7,000 to \$15,000 and is available immediately.

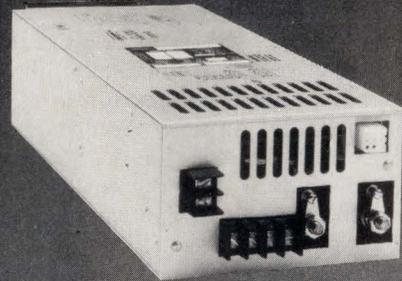
Motorola, ASIC Div., 1300 N. Alma School Rd., Chandler, AZ 85224; (602) 821-4426.

CIRCLE 322

RICHARD NASS

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CIRCLE 158

CASE TOOL ADDITIONS IMPROVE INTEGRATION AND AUTOMATION

Cardtools, a real-time embedded-system CASE environment from Ready Systems, has integrated three new products into its system. These new products are designated TraceBuilder, StateBuilder, and Cardbus Access.

Users can track backwards and forwards through a system, from its requirements all the way to design, with the TraceBuilder. The mouse-driven software automatically finds any changes made to the model data and flags all affected trace information. The mouse-driven module is interactive and available from any Cardtools view.

The StateBuilder makes it possible for users to draw and analyze state-transition diagrams that represent their software. It automatically generates an Ada language description of each diagram and produces the corresponding activation tables. Control specifications and flows are also represented.

Cardbus Access is Cardtools' underlying database-management system. Users can extract, add, or modify information from the software development models. Information can be transferred between models and other external tools, such as databases, software-development tools, and report generators.

This latest Cardtools release contains these enhancements as well as improvements to the Import/Export, Types, and Record facilities. The number of possible types was expanded to 4096, and the number of possible fields has grown to 256.

Cardtools is available for the complete line of VAX/VMS workstations and minicomputers and Sun-3 workstations. Prices start under \$10,000 for a single-user license. Cardbus Access and TraceBuilder are available as options (\$1,000 and \$10,000, respectively), while StateBuilder is shipped standard.

Ready Systems, 480 Potrero Ave., Sunnyvale, CA 94086; (408) 736-2600.

CIRCLE 323

RICHARD NASS

SOFTWARE MONITORS TOXIC GAS LEVELS

Two application software packages transform Bruel & Kjaer's 1306 toxic-gas monitors into a complete monitoring network, giving the user total control from the PC keyboard. The Type 7619 and 7621 programs collect all measurement and self-test data from each monitor. Each continuously updates information and automatically warns of high gas levels within the network, allowing for unattended gas monitoring over extended periods of time. Measurement results are presented in table, bar-chart, or graph format. The Type 7619 package controls networks of up to 31 monitors, while the 7621 program is designed to handle small networks consisting of only three monitors.

Bruel & Kjaer, 18, Naerum Hovedgade, DK-2850 Naerum, Denmark; (45) 02 80 05 00.

CIRCLE 330

6800 CROSS-ASSEMBLER WORKS ON MACINTOSH



Running on the Macintosh II, an assembly language cross-development system assembles 68HC11, 6801, 6301, and 6800 programs at a rate of over 30,000 lines/min. What's more, the Crossbow-6800 development system generates object code directly to the target system or emulator at speeds of up to 57,600 baud. Crossbow's assembler supports multi-file, conditional, macro, and sectioned assembly, generating object files in Intel Hex, Motorola S records, or absolute binary. It optionally creates tabulated source listings and symbol tables. The multi-window editor extends the standard Macintosh editing functions with block and auto-in-

dent, independent tab settings, selection print and save, and side-by-side window comparison.

Onset Computer Corp., 199 Main St., North Falmouth, MA 02556; (508) 563-2267.

CIRCLE 331

SOFTWARE LINKS PC WITH LOGIC CONTROLLER

A software driver package for Radix MicroSystems' EPC-1 VMEbus embedded personal computer includes a set of run-time I/O drivers that interface the EPC-1 with Allen-Bradley's VMEbus programmable logic controller, the PLC-5. The drivers allow application programs running on the EPC-1 to read and write commands and data to and from the PLC-5 via the VMEbus backplane. The VMEbus link provides a much higher interconnection than typical serial bus interfaces between PCs and logic controllers. The driver software is included in the latest release of Radix's EPConnect software environment, which is shipped with the EPC-1 CPU and disk modules for a combined package price of \$7500.

Radix MicroSystems Inc., 19545 N.W. Von Neumann Dr., Beaverton, OR 97006; (800) 950-0044 or (503) 690-1229.

CIRCLE 332

OPERATING SYSTEM BRIDGES MS-DOS VERSIONS

Release 3.4 of DR DOS, a low-cost, single-user, single-tasking operating system, provides major DOS 4.0 features while maintaining a very high level of compatibility with DOS 3.3 applications. Among its new functions are a quick and easy menu-driven installation procedure with simplified on-screen help, full support for DOS 4.0 disk partitioning, and LIM 4.0 memory support. Other benefits include a full-screen editor and an extended command line recall that stores previously entered multiple command lines. Additionally, GEM Desktop, a graphical interface shell from Digital Research, is being offered as an option.

Digital Research Inc., Box DRI, Monterey, CA 93942; (408) 649-3896.

CIRCLE 333

TOKEN-RING NETWORK ANALYZER IDENTIFIES, DIAGNOSES PROBLEMS

Supporting a balanced set of features, Excelan's LANalyzer Network Troubleshooter for token-ring local-area networks identifies, locates, and diagnoses real network conditions and problems. The flexible, powerful instrument incorporates intelligent analyzer circuitry that supports the needs of LAN-analysis software.

The system's analyzer controllers give it features and benefits uncommon among token-ring-network analysis tools. A token-rotation time/ring-recovery count facility, for example, makes it possible for users to check rotation time. This fea-



ture monitors performance and counts ring recoveries to spot potential problems.

A simultaneous send and receive capability enables system administrators to generate a load and monitor its impact at the same time. This capability is helpful when planning network changes and additions.

Thanks to its prefiltering packets, the LANalyzer captures only designated traffic for focused analysis, then saves that information to fixed or RAM disks for later examination. Users can also create custom tests to assess specific network conditions, saving these results to disk as well. The system's buffering packets bypass the speed limitations of the PC/AT bus, a capability that is especially important to address the high-speed requirements of emerging 16-Mbit/s

token-ring networks.

Furthermore, the LANalyzer promotes a proactive approach to network analysis by making it possible for administrators to chart a baseline of average network activity. Then deviations can be monitored and corrected before they adversely affect performance.

The LANalyzer network troubleshooter, including hardware, software, and its NEC PowerMate portable platform, costs \$19,995. It becomes available in August.

Excelan Inc., 2180 Fortune Dr., San Jose, CA 95131; (408) 473-2300.

CIRCLE 324

DAVID MALINIAC

OPTICAL POWER METER HAS DUAL CHANNELS

Operating over a wide range of 0.4 to 1.7 μm , an optical power meter accommodates two plug-in units that enable users to select wavelengths to meet their specific measurement needs. In addition, the AQ-2105 can perform simultaneous measurement and comparison of two separate optical power levels. Dynamic range is from -90 dBm to +10 dBm with a resolution of up to 0.001 dBm. Measurement results are obtained in both absolute (dBm/W) and relative (log/linear) values. An LED optical source unit can be plugged into the AQ-2105 to perform optical loss measurements.

Ando Corp., Measuring Instruments Division, 7617 Standish Pl., Rockville, MD 20855; (301) 294-3365.

CIRCLE 335

PROTOCOL ANALYZER EASES TROUBLESHOOTING

Nonintrusive monitoring of data communication transmissions can be achieved with the AE-5120 protocol analyzer. The unit provides fast analyses of the number, frequency, and nature of data and protocol failures. It is able to analyze complicated protocols, including ISDN LAPD, X.75, SNA/SDLC, and DDCMP, and can perform simulations and analysis of data communications on-line at 72 kbits/s in full-duplex mode. A 640-

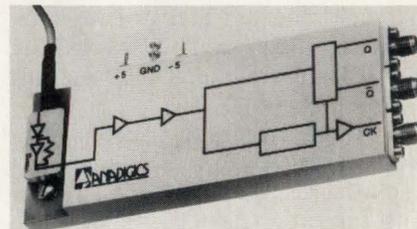


kbyte floppy-disk drive is used to store setup conditions and test programs. Using an optional 20-Mbyte hard-disk drive, the AE-5120 can record for as long as ten minutes at 64 kbits/s full duplex or more than one hour at 9600 bits/s, thus improving the diagnosis of intermittent failures.

Ando Corp., Measuring Instruments Division, 7617 Standish Pl., Rockville, MD 20855; (301) 294-3365.

CIRCLE 334

DIGITAL FO RECEIVER HITS 1.6 GBITS/S



Intended for use in high-speed data transmission, local-area networks, and secure data communication, a digital fiber-optic receiver is capable of handling 1.6 Gbits/s. What's more, the ADR16035 is equipped with an integral clock-recovery circuit. It is available for single or multi-mode fiber and includes a PIN photodetector and transimpedance receiver. Input sensitivity is -26 dBm. Optical dynamic range is rated at 20 dB. Other specifications include a data-output amplitude of 1 V pk-pk with jitter less than 50 ps rms. The recovered clock output amplitude is 1 V pk-pk with jitter of ± 5 degrees rms. Maximum transitionless bit stream at 10^{-9} BER is 60 bits. In large quantities, the receiver costs less than \$1000. Delivery takes eight to 12 weeks.

Anadigics Inc., 35 Technology Dr., Warren, NJ 07060; (201) 668-5000.

CIRCLE 336

NEW PRODUCTS

POWER

FAST, ANALOG-DIGITAL MINI-TILE ARRAYS CONTROL CURRENT TO 2 A

Mixed analog-digital arrays continue to arrive in increasing numbers and variety. The latest arrays, a pair of chips from Micro Linear, can control up to 2 A. The chips extend the company's mini-tile design philosophy, where groups of a few active and passive devices (mini-tiles) of various makes-ups are distributed over an array. New arrays are designed with tiles and combined to handle a particular task or set of tasks.

The new chips, the FB3622 and FB3623, are built with the company's 12-V bipolar process, which produces npn transistors with an f_T of 1 GHz. The FB3622 array is for high-frequency circuits that interface with inductive loads, such as tape drives and some motor controllers.

Grouped among the 28 bonding pads in the array's perimeter are Schottky-clamped npn transistors rated at 150 mA each. Because they're close to the pads, they serve well either as high-frequency off-chip load drivers or as low-noise input amplifiers. Similar to all transistors on an IC, they also may be paralleled without fear of using excessive current. The 112-by-125-mil array also has 276 npn transistors and 108 pnps.

The FG3623, with its four 0.5-amp npn transistors, is designed for very high-power output stages, such as motor controllers and voice coil or relay drivers. The essential pnp transistors that drive the pnps are in a complementary output stage. Furthermore, the 115-by-122-mil array has four high-current clamp diodes.

Nonrecurring engineering charges for these arrays are \$25,000 to \$40,000. Turnaround time after the design is completed is typically six to eight weeks to receipt of prototypes. Packaged chips in large volume cost \$2 to \$9 each, depending on the size of the array.

Micro Linear Corp., 2092 Concourse Dr., San Jose, CA 95131; Ken Fields, (408) 433-5200. CIRCLE 325
FRANK GOODENOUGH

-10-V REFERENCE SERVES 8- AND 10-BIT CONVERTERS

Particularly well suited for 8- and 10-bit converter applications, a negative 10-V reference delivers stable output voltage during variations of input voltage load and changes in temperature. A second output voltage of -10.24 V can be obtained by pin strapping, resulting in binary voltage levels. The REF-08 has an initial 30-mV output voltage tolerance with a 50-ppm/°C output voltage drift when held to temperature specification. A 50-ppm/V line regulation is available for input voltages from -11.4 to -36 V. A very low 25-ppm/mA load regulation is maintained as the load current varies from 0 to 10 mA. Packaging options include 8-pin Cerdips and plastic mini-DIPs, as well as SO-8 packages. Prices start at \$2.40 in lots of 100.

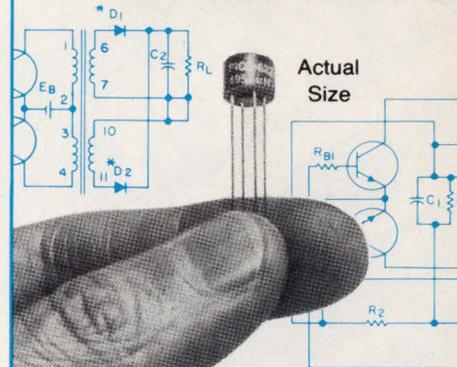
Precision Monolithics Inc., 1500 Space Park Dr., Santa Clara, CA 95052; (408) 727-9222. CIRCLE 337

PWM IC FAMILY TOUTS ENHANCED PERFORMANCE

An enhanced series of current-mode pulse-width modulators (PWMs) provides significantly improved performance over the original family of ICs introduced four years ago. While remaining pin-for-pin compatible with the older devices, the new A series, which includes the UC3842A, UC3843A, UC3844A, and UC3845A, guarantees start-up current of less than 0.5 mA. It also provides precise oscillator discharge current of 8.2 mA and a 1-A peak output stage. The output can sink at least 10 mA at less than 1.2 V during undervoltage lock-out (UVLO) for a V_{CC} of 5 V. Units differ in their UVLO thresholds and maximum duty cycle ranges. The UC3842A has UVLO thresholds of 16 V (on) and 10 V (off). Corresponding thresholds for the UC3843A and 3845A are 8.5 and 7.9 V. DIP and SOIC versions are available with prices starting at \$1.32 in lots of 1000 units.

Unitrode Integrated Circuits Corp., Merrimack, NH; (603) 424-2410. CIRCLE 338

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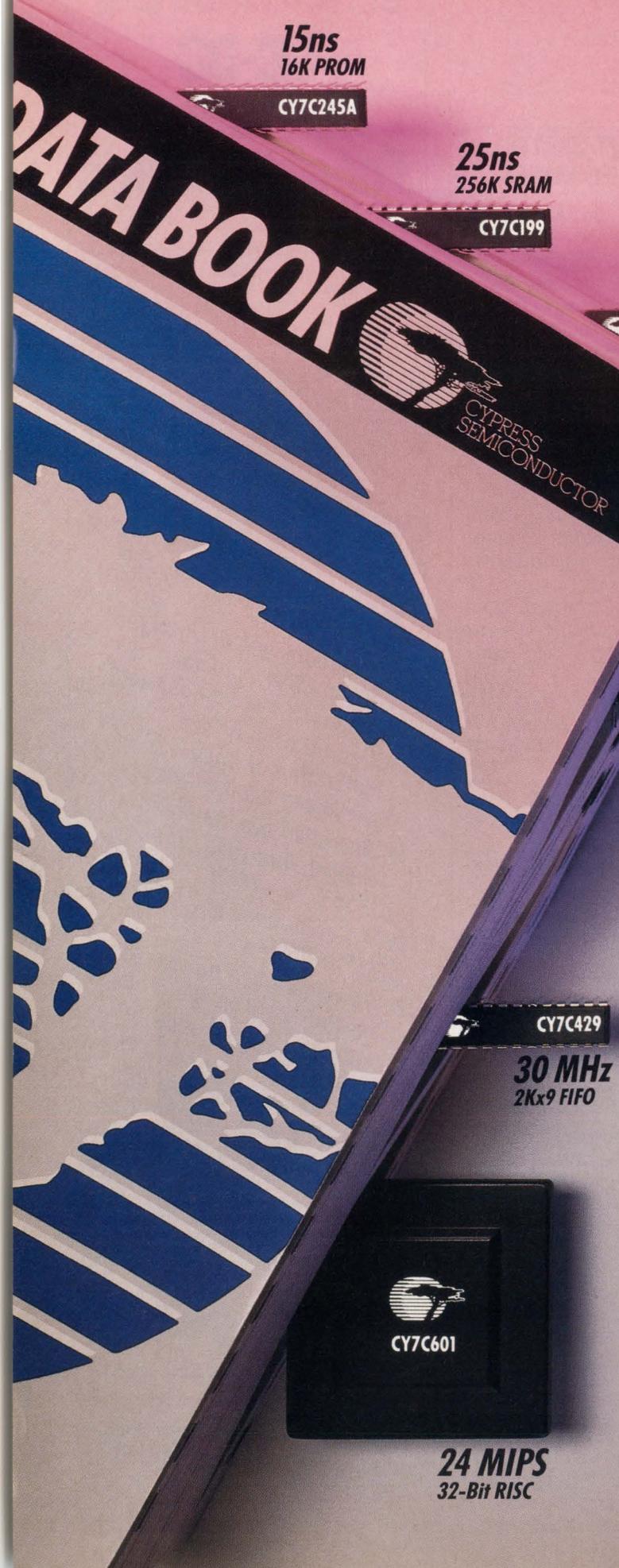
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PC IMAGE PROCESSING AND DATA ACQUISITION

Three comprehensive handbooks focus on Data Translation's products for image processing, data acquisition, and array processing on IBM PC compatibles, IBM PS/2, Macintosh II, and other popular microcomputers. The *1988/89 Image Processing Handbook* (326 pages), *1988/89 Data Acquisition Handbook* (696 pages), and *1989 New Products Handbook* (288 pages) contain detailed data sheets, product line overview charts, application articles, prices, and ordering information. Together, they describe more than 600 boards, software packages, and accessory products.

Data Translation, 100 Locke Dr., Marlboro, MA 01752; (508) 481-3700. CIRCLE 339

ELECTRICAL TESTING, MEASURING INSTRUMENTS

An at-a-glance overview of Biddle's extensive instrumentation capabilities comes from a 10-page condensed catalog of electrical testing and precision measuring instruments. Photos and descriptions help users select insulation testers, digital low-resistance ohmmeters, cable fault-locating equipment, time-domain reflectometers, transformer turn-ratio test sets, tachometers, speed indicators, high-voltage detectors, phase and motor-rotation testers, power-factor test sets, dc dielectric test sets, digital-thermocouple calibrators, resistance bridges, and decade boxes.

Biddle Instruments, 510 Township Line Rd., Blue Bell, PA 19422; (215) 646-9200. CIRCLE 340

POWER SUPPLIES FOR EVERY NEED

A 32-page catalog provides information on over 350 power supplies based on three technologies for those who need controlled and stabilized dc power. Major categories include industrial-grade switchers (ac-dc and dc-dc), OEM ac-dc switching modules, custom system power as-

semblies, linear power supplies, ferroresonant power supplies, bench-type power supplies, digital programmers, and accessories and hardware. Specifications are given for units in each group, along with photos and other pertinent information.

Kepeco Inc., 131-38 Sanford Ave., Flushing, NY 11352; (718) 461-7000. CIRCLE 341

DEVICES FOR POWER CONVERSION

Basic electrical and mechanical specifications for a line of ac-dc power supplies and dc-dc converters are supplied in a 20-page short-form catalog. Over 200 ac-dc supplies are described including open-frame switchers, encapsulated linear and switching modules, open-frame linears, and enclosed switchers from 15 to 1500 W. Also included are over 200 dc-dc converters ranging from 0.5 to 100 W. Part specifications are laid out for easy scanning.

Computer Products Inc., Catalog Dept., 3785 Spinnaker Ct., Fremont, CA 94538; (415) 657-9837. CIRCLE 342

TRANSPUTER-BASED PARALLEL PROCESSING

With *Performance by Paracom*, system engineers get a detailed look at the company's complete line of parallel processing products. The 24-page booklet is divided into categories which include bus-based boards, bus-less boards, systems, software compilers and development systems, and accessories. It also provides extensive tutorials on Transputer technology, on which all boards and systems are based, as well as system architecture, integration, and applications. An appendix completes the catalog.

Paracom Inc., Bldg. 9, Unit 60, 245 W. Roosevelt Rd., West Chicago, IL 60185; (312) 293-9500. CIRCLE 343



HIGH-VOLTAGE DIODES AND RECTIFIERS

Dimensional drawings, application information, and electrical specifications highlight this 12-page catalog of silicon rectifier products. Engineering information is provided to aid in specifying ultra-fast, fast, and standard recovery silicon devices. Product lines include high-voltage miniature diodes, night-vision assemblies, multipliers, high-voltage assemblies, bridge rectifiers, and others.

HV Component Associates Inc., 272 U.S. Hwy. 9, Howell, NJ 07731; (201) 431-0030. CIRCLE 344

2-A POWER SUPPLY MEETS TELECOM NEEDS

The subject of a four-color data sheet, the 9001 2-A power supply is typically used to power network channel terminating equipment (NCTE). It fits into a single Wescom 400, Tellabs Type 10, or equivalent-type customer-premises mounting. A complete listing of the unit's features is provided, along with a handy specifications chart and information on installation and ordering.

Tollgrade Communications Inc., P.O. Box 3188, Erie, PA 16508; (814) 455-0566. CIRCLE 345

POWER SEMICONDUCTOR DATA BOOK

Comprehensive data is provided in this 90-page data book on an extensive and varied line of power semiconductor devices consisting of bipolar transistors, Darlingtons, and diodes. Devices cover a current range from 3.5 to 60 A, a voltage range from 200 to 1500 V, and a power dissipation range from 100 to 250 W. A cross-reference guide lists PTC part numbers with corresponding parts from TRW, Motorola, International Rectifier, Delco, GE/RCA, Thomson, and Phillips, along with package type.

Power Technology Components, 23201 S. Normandie Ave., Torrance, CA 90501; (213) 534-3737. CIRCLE 346

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UPCOMING MEETINGS

JULY

16th Annual Conference & Exhibition on Computer Graphics & Interactive Techniques (SIGGRAPH '89), July 30-Aug. 4. Hynes Auditorium, Boston, MA. Chris Herot, Javelin Software Corp., 1 Kendall Sq., Cambridge, MA 02139.

AUGUST

26th National Heat Transfer Conference and Exposition, August 6-9. Adam's Mark Hotel, Philadelphia, PA. Jeff Lenard, American Society of Mechanical Engineers, 345 East 47th St., New York, NY 10017; (212) 705-7740.

SEPTEMBER

DEXPO West '89, September 6-8. Anaheim Convention Center, Anaheim, CA. Expoconsul International Inc., 3 Independence Way, Princeton, NJ 08540; (609) 987-9400.

BUSCON '89 East, September 11-14. Royal Plaza Trade Center, Marlborough, MA. Sharon Green, CMC, 200 Connecticut Ave., Norwalk, CT 06856-4990; (203) 852-0500.

Midcon/89, September 12-14. O'Hare Exposition Center, Chicago, IL. Midcon/89, 8110 Airport Blvd., Los Angeles, CA 90045; (800) 421-6816.

NCGA C⁴ Aerospace & Electronics '89, September 12-15. Santa Clara Convention Center, Santa Clara, CA. Michael Weiner, National Computer Graphics Association, 2722 Merrilee Dr., Ste. 200, Fairfax, VA 22031; (703) 698-9600.

1989 ASIC Seminar and Exhibit, September 25-28. Rochester Riverside Convention Center, Rochester, NY. William Bush, 2530 Parker Rd., Palmyra, NY 14522; (716) 244-5830.

Autotestcon '89, September 25-28. Philadelphia, PA. Fred Liguori, Autotestcon '89, P.O. Box 1185, Browns Mills, NJ 08015; (201) 323-2842.

Advanced Composites Conference and Exposition, September 26-28. Hyatt Regency, Dearborn, MI. ASM

International (216) 338-5151.

21st International SAMPE Technical Conference, September 26-28. Atlantic City, NJ. Holly Barnett, R.L. Couch Public Relations, (714) 474-9111.

OCTOBER

IEEE International Conference on Computer Design (ICCD '89), October 2-4. Hyatt Regency, Cambridge, MA. Gail Clanton, Computer Society of the IEEE, (202) 371-1013.

Electronic Imaging East '89, October 2-5. Hynes Convention Center, Boston, MA. MG Expositions Group, 1050 Commonwealth Ave., Boston, MA 02215; (800) 223-7126 or (617) 232-3976.

4th Annual PC EXPO, October 3-5. McCormick Place North, Chicago, IL. PC Expo, 385 Sylvan Ave., P.O. Box 1026, Englewood Cliffs, NJ 07632; (201) 569-4147 or (800) 777-2281.

IEEE 1989 Ultrasonics Symposium, October 3-6. Montreal, Quebec, Canada. Narendra Batra, Code 6385, Naval Research Laboratory, Washington, D.C. 20375-5000; (202) 767-3505.

FASTEC '89 Conference and Exposition, October 4-5. Sheraton CentrePark Hotel, Arlington, TX. Carol Anderson, Society of Manufacturing Engineers (SME), One SME Dr., P.O. Box 930, Dearborn, MI 48121-0930; (313) 271-1500.

SCAN-TECH '89 International Show and Seminar, October 16-19. New San Jose Convention Center, San Jose, CA. Donald Anderson, Automatic Identification Manufacturers (AIM USA), 1326 Freeport Rd., Pittsburgh, PA 15238; (800) 338-0206 or (412) 963-8588.

Supercomputing World Conference, October 17-20. San Francisco Civic Center, San Francisco, CA. MG Expositions Group, 1050 Commonwealth Ave., Boston, MA 02215; (800) 223-7126 or (617) 232-3976.

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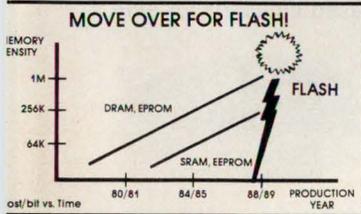
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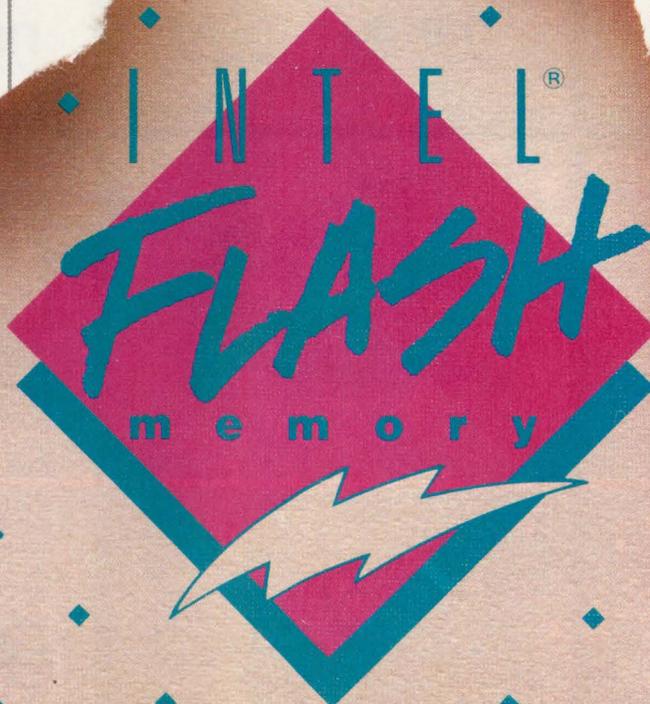
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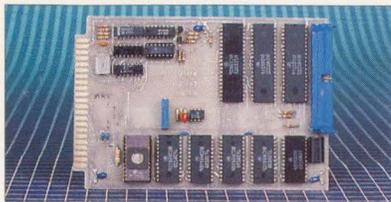


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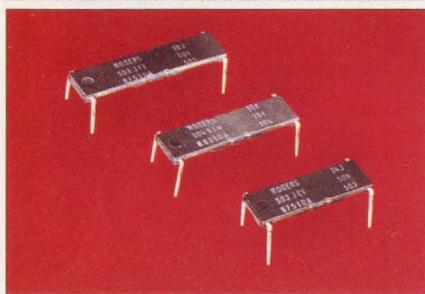
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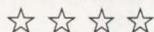


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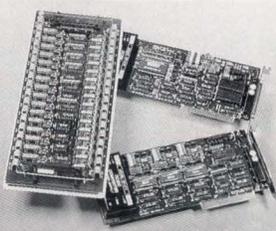
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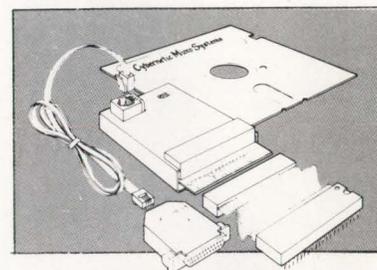
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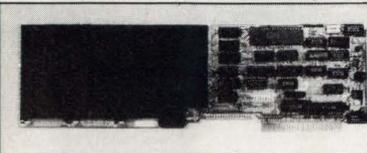


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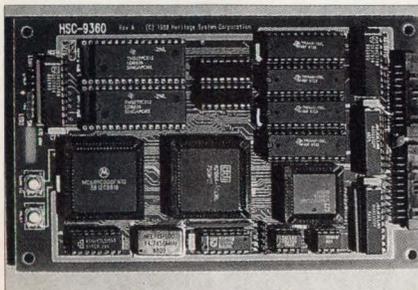
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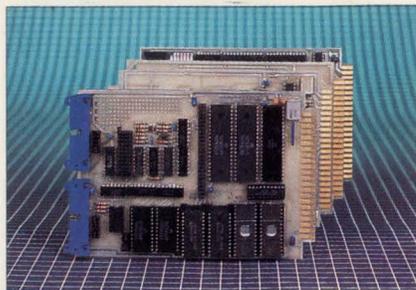
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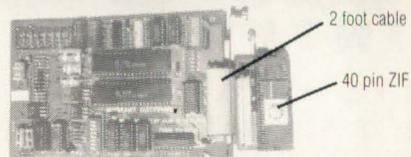
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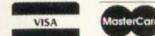
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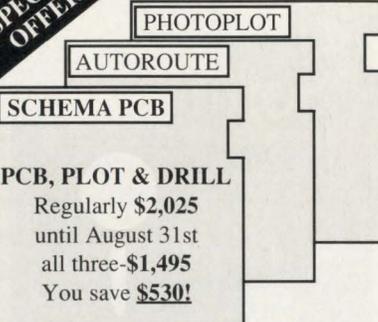
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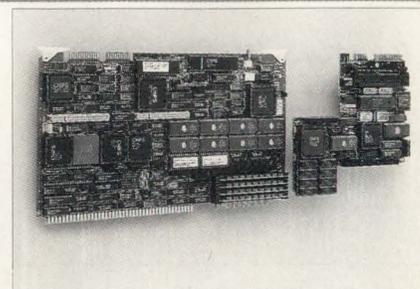
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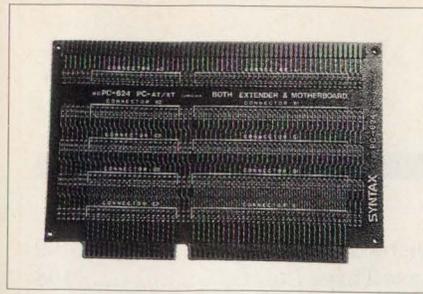
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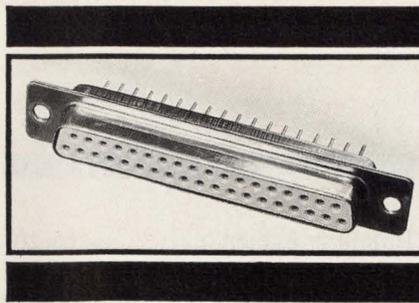
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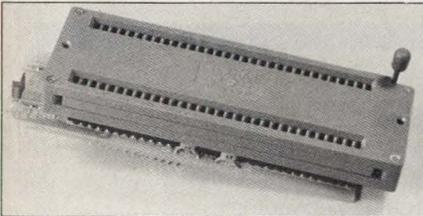
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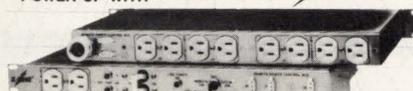
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