FPGA Editor Guide

About This Manual

This manual describes the Xilinx FPGA Editor, a graphical application used for displaying and configuring Field Programmable Gate Arrays (FPGAs).

Before using this manual, you should be familiar with the Xilinx design flow, including design entry and implementation. For more information on the Xilinx tools, refer to the *Development System Reference Guide*, *Design Manager/Flow Engine Guide*, and the *Alliance Series 2.1i Quick Start Guide*.

Additional Resources

For additional information, go to http://support.xilinx.com. The following table lists some of the resources you can access from this page. You can also directly access some of these resources using the provided URLs.

Resource	Description/URL
Tutorial	Tutorials covering Xilinx design flows, from design entry to verification and debugging http://support.xilinx.com/support/techsup/tutorials/index.htm
Answers Database	Current listing of solution records for the Xilinx software tools Search this database using the search function at http://support.xilinx.com/support/searchtd.htm
Application Notes	Descriptions of device-specific design techniques and approaches http://support.xilinx.com/apps/appsweb.htm
Data Book	Pages from *The Programmable Logic Data Book*, which describe device-specific information on Xilinx device characteristics, including read-back, boundary scan, configuration, length count, and debugging http://support.xilinx.com/partinfo/databook.htm

Resource	Description/URL
Xcell Journals	Quarterly journals for Xilinx programmable logic users http://support.xilinx.com/xcell/xcell.htm
Tech Tips	Latest news, design tips, and patch information on the Xilinx design environment http://support.xilinx.com/support/techsup/journals/index.htm

Manual Contents

This manual covers the following topics.

- Chapter 1, “Introduction,” describes the FPGA Editor’s function, features, and various design considerations.
- Chapter 2, “Getting Started,” describes how to start and exit the FPGA Editor, using the basic elements and operations of the FPGA Editor interface.
- Chapter 3, “Using the FPGA Editor,” describes how to perform various operations on your design files.
- Chapter 4, “Menu Commands,” describes the FPGA Editor graphical user interface commands, dialog boxes, and toolbar buttons.
- Chapter 5, “Working with Physical Macros,” explains how to create and work with macros.
- Chapter 6, “Command Line Syntax,” describes the complete set of commands needed to perform all the FPGA Editor operations.
- Chapter 7, “Customizing the FPGA Editor,” explains how to customize the FPGA Editor by showing how default values are set for many FPGA Editor features and how to override these default settings.
- Appendix A, “Glossary,” describes the basic terminology used in the FPGA Editor manual.
- Appendix B, “FPGA Editor Files,” provides an alphabetical listing of the files used by the FPGA Editor.
- Appendix C, “Configuring Xprinter,” provides detailed instructions on configuring a printer so you can print from the Xilinx

application. The information in this appendix applies only to workstation applications.

Conventions

This manual uses the following typographical and online document conventions. An example illustrates each typographical convention.

Typographical

The following conventions are used for all documents.

- `Courier font` indicates messages, prompts, and program files that the system displays.

  ```
  speed grade: -100
  ```

- **`Courier bold`** indicates literal commands that you enter in a syntactical statement. However, braces "{ }" in Courier bold are not literal and square brackets "[ ]" in Courier bold are literal only in the case of bus specifications, such as bus [7:0].

  `rpt_del_net=`

  `Courier bold` also indicates commands that you select from a menu.

  `File` → **`Open`**

- *Italic font* denotes the following items.

  - Variables in a syntax statement for which you must supply values

    `edif2ngd` *design_name*

  - References to other manuals

    See the *Development System Reference Guide* for more information.

- Emphasis in text

  If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.

- Square brackets "[ ]" indicate an optional entry or parameter. However, in bus specifications, such as bus [7:0], they are required.

  edif2ngd [*option_name*] *design_name*

- Braces "{ }" enclose a list of items from which you must choose one or more.

  lowpwr ={**on** | **off**}

- A vertical bar " | " separates items in a list of choices.

  lowpwr ={**on** | **off**}

- A vertical ellipsis indicates repetitive material that has been omitted.

```
IOB #1: Name = QOUT'
IOB #2: Name = CLKIN'
.
.
.
```

- A horizontal ellipsis ". . ." indicates that an item can be repeated one or more times.

  allow block *block_name loc1 loc2* . . . *locn;*

Online Document

The following conventions are used for online documents.

- Red-underlined text indicates an interbook link, which is a cross-reference to another book. Click the red-underlined text to open the specified cross-reference.
- Blue-underlined text indicates an intrabook link, which is a cross-reference within a book. Click the blue-underlined text to open the specified cross-reference.

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Chapter 5 Working with Physical Macros

Appendix A Glossary

Appendix B FPGA Editor Files

Appendix C Configuring Xprinter

Chapter 1

Introduction

This chapter briefly describes the FPGA Editor's function, features, and various design considerations. The following sections are included in this chapter.

- "Overview"
- "Design Flow"
- "FPGA Editor Files"
- "Architecture Support"

Overview

The FPGA Editor is a graphical application for displaying and configuring Field Programmable Gate Arrays (FPGAs). You can use this application to place and route critical components before running the automatic place and route tools on your design. You can also use the FPGA Editor to manually finish placement and routing if the routing program does not completely route your design.

The FPGA Editor requires a Native Circuit Description (NCD) file. This file contains the logic of your design mapped to components (such as CLBs and IOBs). In addition, the FPGA Editor reads from and writes to a Physical Constraints File (PCF).

Design Flow

The following steps provide an overview of the FPGA Editor design flow.

1. Enter your design using a schematic design tool or HDL (Hardware Description Language).
2. Save your design in EDIF (Electronic Data Interchange Format).

3. Run NGDBuild, which creates an NGD (Native Generic Database) file.
4. Run the MAP program, which creates an NCD (Native Circuit Description) file.
5. Load your design into the FPGA Editor, make necessary changes, and save the modified design as an NCD file.
6. Run the PAR (Place and Route) program on the modified NCD file.

The following figure shows the complete Xilinx design flow, including editing your design in the FPGA Editor.

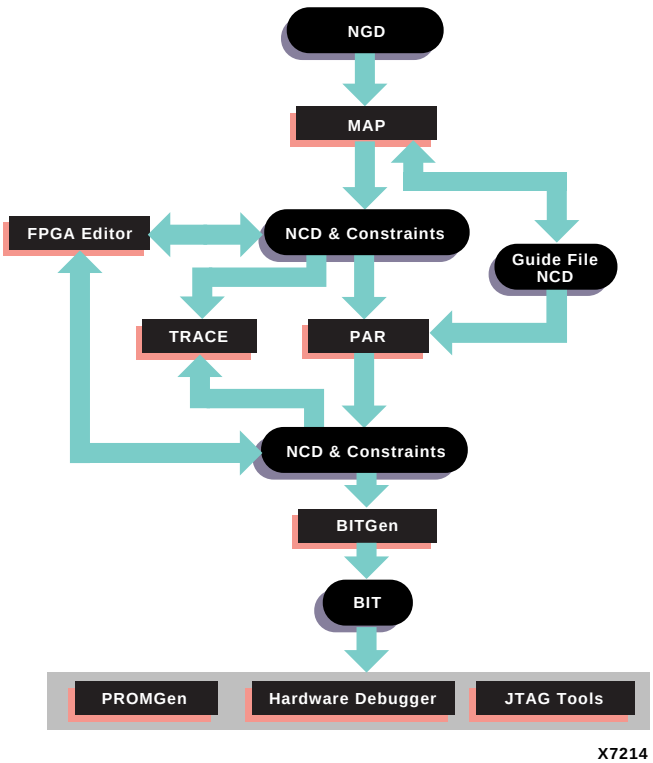


Figure 1-1 Design Flow

FPGA Editor Files

The following files are used with the FPGA Editor. See the “FPGA Editor Files” appendix for more information on FPGA Editor files.

NCD File

The NCD file is the output file from the MAP program and represents the physical design. This file describes your design in terms of CLBs and IOBs. You can edit your design in the FPGA Editor, save it, and then route your design with PAR.

PCF File

The PCF file is an ASCII file containing physical constraints created by the MAP program, as well as physical constraints entered by you. You can edit the PCF file in the FPGA Editor.

Architecture Support

The FPGA Editor supports the following Xilinx device subfamilies.

- XC3000A, XC3000L
- XC3100A, XC3100L
- XC4000E, XC4000EX, XC4000L, XC4000XL, XC4000XV, XC4000XLA
- XC5200
- Virtex
- Spartan, SpartanXL, Spartan2

Chapter 2

Getting Started

This chapter describes how to start and exit the FPGA Editor. It also explains the basic elements and operations of the FPGA Editor interface. This chapter includes the following sections.

- "Starting the FPGA Editor"
- "Exiting the FPGA Editor"
- "Using the Interface"

Starting the FPGA Editor

The FPGA Editor runs on PCs and workstations. You can start the FPGA Editor from the Windows Program Manager, the Xilinx Alliance Design Manager, the Xilinx Foundation Project Manager, or the command line.

This section contains the following topics.

- "From the Design Manager (Alliance Series)"
- "From the Project Manager (Foundation Series)"
- "Stand-Alone Tool"
- "From the Command Line"

From the Design Manager (Alliance Series)

To start the FPGA Editor from the Design Manager window (PC or workstation), click on the FPGA Editor icon, shown in the following figure. Or select the **`Tools`** → **`FPGA Editor`** menu command.

From the Project Manager (Foundation Series)

To start the FPGA Editor from the Project Manager window, select **Tools** → **Implementation** → **FPGA Editor**.

Stand-Alone Tool

Note: To run the FPGA Editor as a stand-alone tool on a PC, you must have the XILINX environment variable defined and the path must include $XILINX/bin/nt.

If you installed the FPGA Editor as a stand-alone tool on a PC, click on the FPGA Editor icon (shown in the previous figure) on the Windows desktop or select fpga_editor.exe from the Windows Start button.

From the Command Line

To start the FPGA Editor from a UNIX command line, type the following command.

```
fpga_editor
```

The following table includes the different options you can use when starting the FPGA Editor from the UNIX command line or from the Run option in the Windows Start button menu

Table 2-1 FPGA Editor Command Line Options

Option	Description
-n	Specifies No Logic Changes mode
-e	Specifies Read-Write mode
-r	Specifies Read-Only mode
-m	Specifies Macro Edit mode
-p	Specifies a script file to perform immediately after your design (or macro) is read or created, or after the FPGA Editor's initialization files have been read

The FPGA Editor window appears with the specified design loaded or, if you have not specified an existing design, the FPGA Editor window appears displaying an empty design with the specified part and speed. If you are creating a new design, you are placed in a mode that allows you to make changes to the design.

Syntax

fpga_editor [**-r** | **-e** | **-n**] *design_name*.**ncd** *pcffile_name*.**pcf** **-p** *script_file_name*

To run the FPGA Editor on an existing design use the following.

fpga_editor [**-n**|**-e**|**-r**] *design_name*.**ncd** [*pcffile_name*.**pcf**]

To run the FPGA Editor and create a new design use the following.

fpga_editor -e *design_name*.**ncd** [*pcffile_name*.**pcf**] [*arch device package speed*]

To run the FPGA Editor on an existing physical macro use the following.

fpga_editor [**-e**|**-r**] **-m** *macro_file_name*

To run the FPGA Editor to create a new physical macro use the following.

fpga_editor -e -m *macro_file_name* [*arch device package speed*]

Variables

- Design_name.ncd

  The name of your new or existing design file. You do not need to enter the .ncd suffix on the command line.

- Macro_file_name

  The name of your new or existing macro file.

- Pcffile_name.pcf

  The name of the new or existing constraints file that you want applied to your design file. The .pcf extension is optional.

- Script_file_name.scr

  Specifies the name of a command file that includes command line arguments. The .scr extension is optional.

- Arch

  Specifies the architecture (product family) of your design, for example, XC4000E or XC4000.

Note: To see what devices, packages, and speeds are available, select **File** → **New** and click the Select Part button to display the Part Selector dialog box, shown in the "Part Selector Dialog Box" figure of the "Menu Commands" chapter.

- Device

  Specifies a device within the selected architecture, for example, 4036 or 4028.

- Package

  Specifies a package within the selected architecture and device; for example, PC84 or PQ100.

Note: You can only enter a device and package from a part library that is installed on your system. For example, if you have not installed the Xilinx 4036EX series part library, you cannot create a design using the 4036EX device and the package.

- Speed

  Specifies the speed grade of the selected part. Allowable speeds are listed in the online Data Book at http://support.xilinx.com/partinfo/databook.htm.

Options

See the "Opening an Existing Design File" section of the "Using the FPGA Editor" chapter for other mode options.

-r

Read Only Mode—prevents overwriting your design. You can open and edit your design, but you cannot save changes to your original file. However, you can save your changes to a file with a different name.

-e

Read-Write Mode—makes any changes to your design, including changes to the logical configurations.

-n

No Logic Changes Mode (default mode)—makes placement and routing changes, but not changes to the logical configurations. For example, you cannot add or delete nets and components or reprogram programmable components. This mode ensures that the design database is consistent with the schematic or netlist from which it was created.

-p

Use this option to execute the command line arguments in the specified file after your design or macro is opened or created.

-m

Use this option when you want to edit or create a macro.

Exiting the FPGA Editor

1. Perform one of the following.
   - Select **File** → **Exit**.
   - Select **Exit** from the User toolbar.
   - Enter **exit** in the Command Line toolbar.

   The following dialog box appears.

Note: If you have not made any changes since you last saved the design, the FPGA Editor window closes without displaying this dialog box.

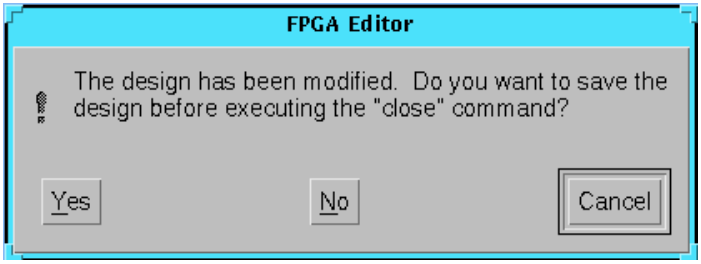


Figure 2-1 Exit Dialog Box

2. Click **Yes** to save changes and exit, **No** to discard changes and exit, or **Cancel** to return to your design without exiting.

Using the Interface

This section describes the FPGA Editor interface and how to use it.

Note: Menus, dialog boxes, and parts of the application window are documented as they appear on a UNIX workstation. Differences between the PC and the workstation applications are documented if there is a difference in operation between the two platforms.

This section contains the following topics.

- "Main Window"
- "Using Dialog Boxes"
- "Using Help"
- "Using the Mouse and Keyboard"

Main Window

This section describes the FPGA Editor main window. To work in a particular section of the interface, click the left mouse button in that section. The default layout of the main window is shown in the following figure. You can execute commands from the menus, toolbars, and command line. The client or work space area includes the Array window, List window, and World window.

Note: If you do not have a design open in the Array window, only the File, View, Tools, and Help menus are available.

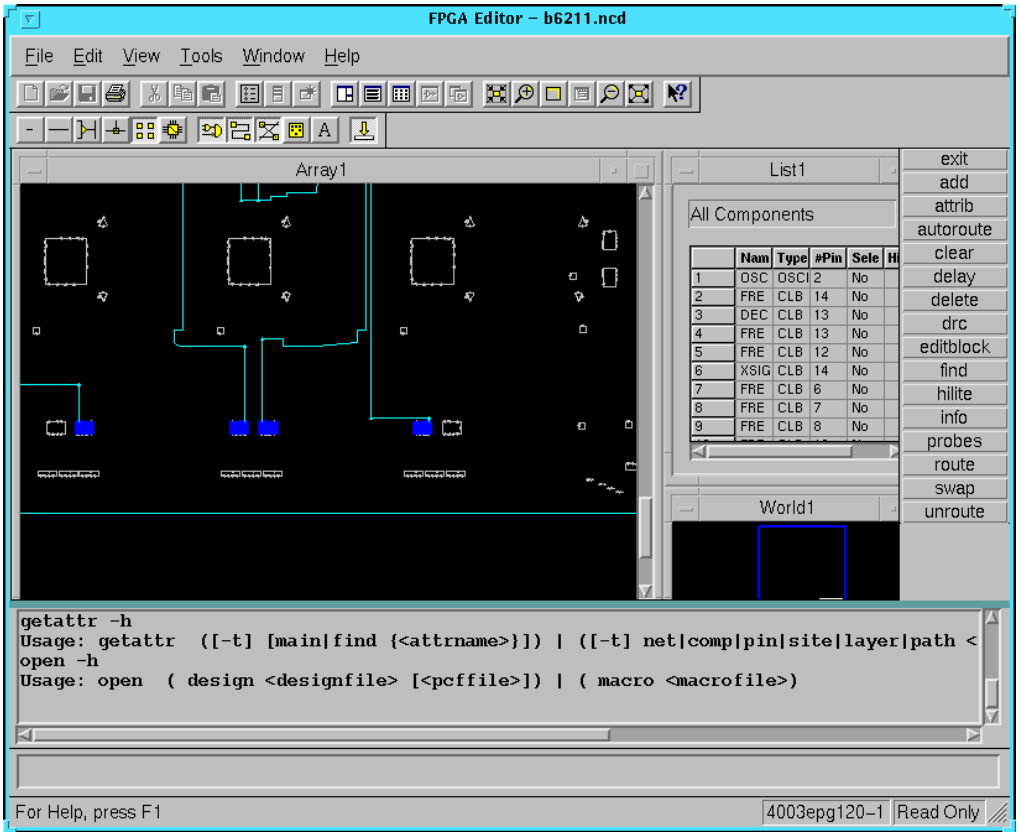


Figure 2-2 FPGA Editor Main Window

The main window includes the following areas.

- Title Bar
- Menu Bar
- Standard Toolbar
- Layer Visibility Toolbar
- Array Window
- List Window
- User Toolbar
- World Window

- History Area Toolbar
- Command Line Toolbar
- Status Bar

Note: The Block Window and Toolbar are displayed when you double click the left mouse button on a logic block

- Block Window
- Block Window Toolbar

Title Bar

The title bar displays the program name and the name of the currently loaded design.

Menu Bar

The menu bar is located above the Array window. Most of the FPGA Editor commands are available in the pull-down menus of the FPGA Editor window after a design is loaded.

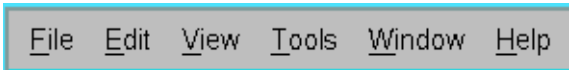


Figure 2-3 Menu Bar

You can select menu commands with the mouse or the keyboard. With the mouse, click the left mouse button on the command. With the keyboard, press the Alt key and type in the letter underlined in the menu for that command. When you select a menu command with either method, a brief description of the command's function appears in the Status Bar at the bottom of the FPGA Editor window.

Some menu commands include an ellipsis (...). When you select one of these commands, a dialog box appears. You can enter additional information for that command in the dialog box. Refer to the "Menu Commands" chapter for detailed information on the commands in each menu or select **Help** → **Help Topics**.

Standard Toolbar

The Standard toolbar contains commands for performing common operations on your designs, such as opening a design file, deleting objects from your design, and displaying a more detailed view of

your design. Click once on a button in the toolbar to access a command.

If you position the mouse pointer over a toolbar button, a short description, called a tool tip, appears next to the button and a longer description appears in the status bar at the bottom of the main window.

Layer Visibility Toolbar

The Layer Visibility toolbar allows you to specify which objects are displayed in the Array window. Use the left mouse button to select or deselect the layers you want displayed or hidden. You can control the display of the following objects.

Note: See the "Glossary" appendix for definitions of these objects.

- Local lines
- Long lines
- Pin wires
- Pips
- Sites
- Switch boxes
- Components
- Routes
- Ratsnests
- Macros
- Text (reference designators)

Array Window

The Array window displays a graphical representation of the FPGA device. The device components and the interconnections (both logical and routed) between these components are displayed in this window. When you edit the internal logic of a programmable component such as a logic block, a schematic of the interior of the component is displayed in the Block window.

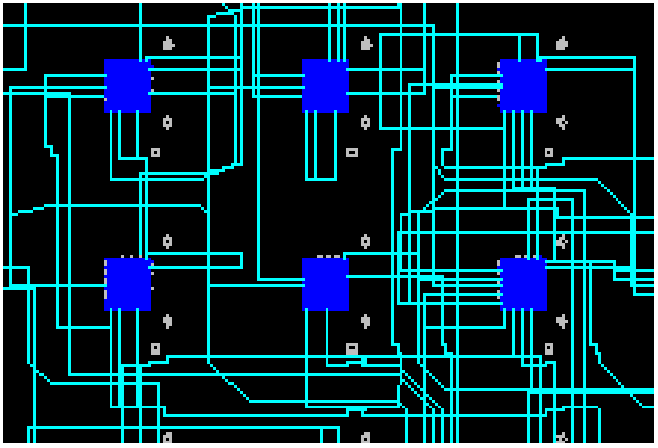


Figure 2-4 Section of Array Window

You can control the display of objects in the Array window with the Layer Visibility toolbar. You can turn off the display of individual object layers, such as switches, wires, and routed connections, to make your design easier to view. Selectively viewing objects also reduces the duration of each screen redraw.

Note: Symbols used in the FPGA Editor Array window for specific devices are described in *The Programmable Logic Data Book*.

A site is a programmable logic element (used or unused) located within the device. Sites are potential locations for components and are displayed in the Array window as outlines of components. Components are CLBs, IOBs, tristate buffers, pull-up resistors, oscillators, or clocks. When you place a component into a site, the outline is filled in.

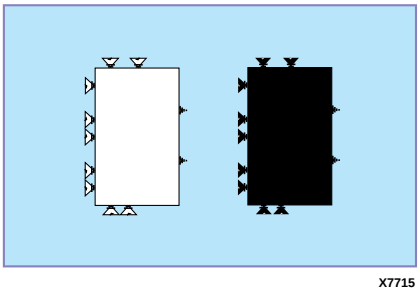


Figure 2-5 Sites and Components

Components are connected by nets. A net is a set of component pins that are electrically connected in the finished design. When a component is placed, but not yet routed, the connection between that component's net pins (those pins on the net) and net pins from other components is logical, not physical. The pins are associated with each other, even though there is no electrical connection between them. In the Array window, the logical connections that make up a net are displayed as ratsnest lines or direct point-to-point connections between net pins, as shown in the following figure.

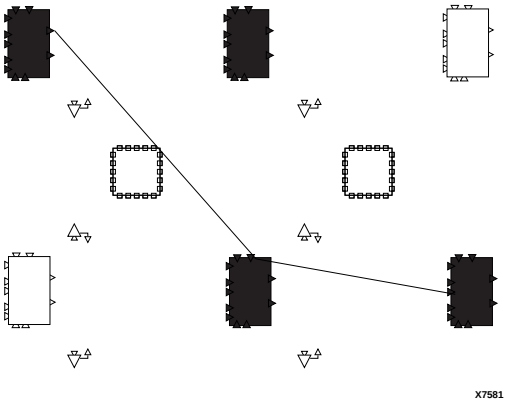


Figure 2-6 Ratsnest Display (Unrouted Net)

When the net is routed, electrical connections are made between the net pins. In the Array window, the routed connections appear as lines following the routing resources available on the device (long lines, pinwires, switch boxes, and so on). The following figure shows a routed net display.

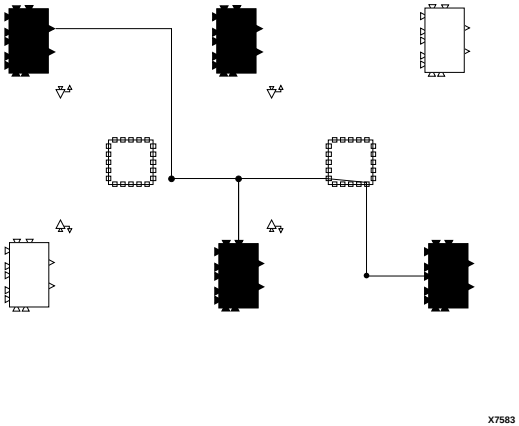


Figure 2-7 Display of Routed Net

List Window

The List window displays a list of the components, nets, layers, paths, and macros in your design. Use the pull-down list box at the top of the window to specify the items you want displayed in the List window.

Note: See the "Selecting Objects with the List Window" section of the "Using the FPGA Editor" chapter for a complete description of the List window.

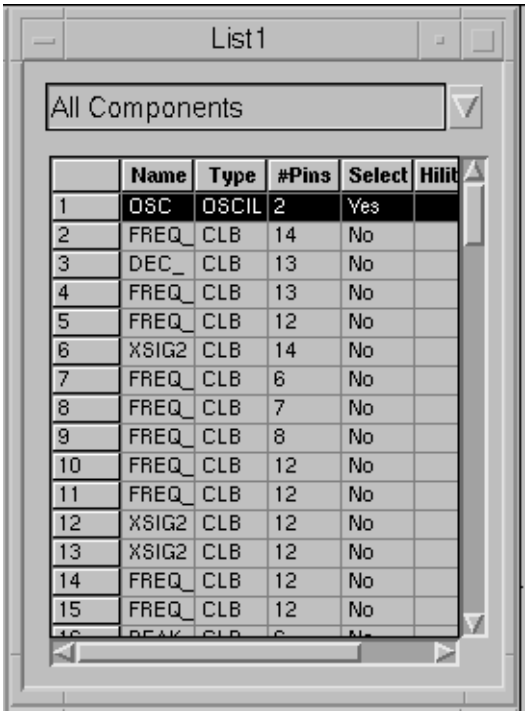


Figure 2-8 List Window

User Toolbar

The User toolbar, shown in the following figure, provides a convenient way to perform frequently used commands. To use a command, select the appropriate command button with the left mouse button.

You can customize the User toolbar with the Button and Unbutton commands described in the“Command Line Syntax” chapter or by editing the fpga_editor.ini or the fpga_editor_user.ini file. These files define the default User toolbar buttons that appear when the FPGA Editor window opens.

Table 2-2 Default User Toolbar Command Summary

Command	Description
exit	Exits FPGA Editor. If you edited your design, a dialog box appears to allow you to save changes.
add	Adds selected sites as components to your design.
attrib	Posts a dialog box containing property information for all selected items or for the main window if no item is selected.
autoroute	Automatically routes a selected component, macro, net, ratsnest, or net pin between selected routing resources.

Table 2-2 Default User Toolbar Command Summary

Command	Description
clear	Deselects all selected objects.
delay	Calculates and lists the path delay for a selected net or selected pins on a net. This information appears in the history area and in the List window when nets are selected.
delete	Deletes selected objects from the design.
drc	Performs a DRC (Design Rule Check), which checks for logical and physical errors in the design. The results appear in the history area and also in the log file.
editblock	Starts the logic block editor, which allows you to view or edit the internal logic of a selected logic block.
find	Posts a dialog box that allows you to find a specified component, macro, site, pin, or net.
hilite	Highlights a selected object.
info	Lists the properties for a selected object in the history area.
probes	Posts a dialog box that allows you to add probes to your design.
route	Routes selected objects (manual route).
swap	Moves a component to another site or swaps locations between two components or two logic block pins.
unroute	Unroutes selected objects.

World Window

The World window, as shown in the following figure, shows the area of the device that is currently displayed in the Array window. As you pan and zoom the Array window, notice the corresponding changes in the size and position of the rectangle within the World window. Also, any objects selected in the Array window appear in the World window. You can drag the inner box with the mouse button to pan the display to the desired position. If you have multiple Array windows, the World window displays a rectangle for each Array window.

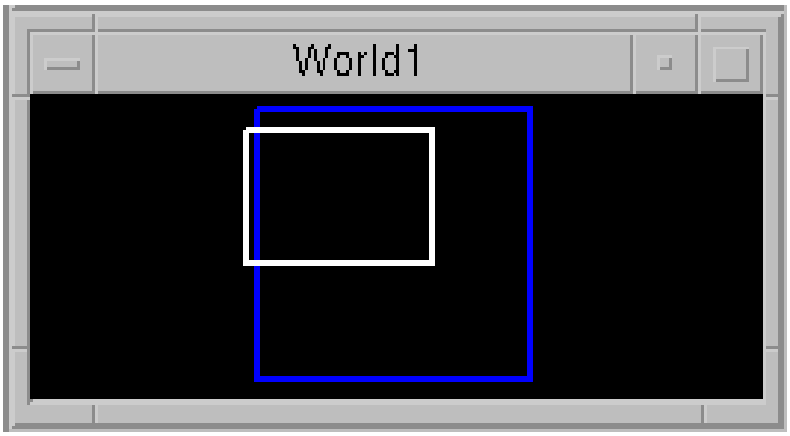


Figure 2-9 World Window

History Area Toolbar

The History toolbar, shown in the following figure, is located below the Array window and displays commands and responses. All error messages, warnings, and command responses are written to the History toolbar. Information in the History toolbar is especially useful for deciphering unexpected command results.

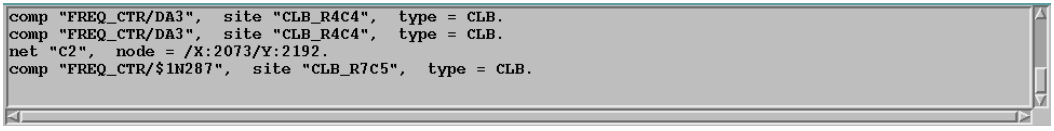


Figure 2-10 History Toolbar

Use the scroll bar located to the right of the History toolbar to view all the commands and responses recorded during an editing session. You can resize the toolbar by selecting the top of the toolbar, and using the left mouse button to move the double-headed arrow that appears up or down.

The history area accommodates 32,000 characters of output on Windows 95/98 platforms, and a much larger number of characters on Windows NT and UNIX platforms. To examine text beyond this limit, use any text editor to view the contents of the log file for your session. The log file is named *design_name*.out and is described in the“Recovering a Terminated FPGA Editor Session” section of the

"Using the FPGA Editor" chapter. You must remain in the FPGA Editor while you view this file because the file is renamed when you exit the FPGA Editor.

Note: Refer to the"Main Window" section for more information.

Command Line Toolbar

Use the Command Line toolbar, shown in the following figure, to enter commands from the keyboard.

Figure 2-11 Command Line Toolbar

Notes on Entering Commands

- Multiple commands can be issued on the same line as long as they are separated by a semicolon.
- Commands that might go across multiple command lines must use a back slash at the end of each line to be continued.
- On Unix platforms, commands are case-sensitive.
- If a command argument contains any special characters (" ' * ? \ ; #), embedded spaces in the argument, or leading dashes, the argument must be placed in quotation marks (for example, button "zoom in twice" "zoom in; zoom in") or escaped by preceding the reserved character with a back slash. For example, select net \ ;* selects a net of the name ";*."
- PC command line only.

  Since back slash serves as the FPGA Editor escape character, it affects DOS style path names. For example, the following command will not produce the desired effect.

  `load design \data\mydesign.ncd`

  The system responds with the following.

  ```
  ERROR – load: file "datamydesign.ncd" not found
  ```

  Use one of these solutions to solve this problem.

  - Use forward slashes (UNIX style) in the path name.

```
load design /data/mydesign.ncd
```

- Escape the escape characters.

```
load design \\data\\mydesign.ncd
```

- If you have trouble entering text, you may need to click first in the FPGA Editor Command Line toolbar.
- Press the F2 key to move the keyboard focus to the Command Line toolbar.

Status Bar

The status bar appears at the bottom of the main window. When you select a menu command, a brief description of the command's function appears in the status bar.

Block Window

Note: This window is displayed when you double click the left mouse button on a logic block.

The Block window shown in the following figure is used to edit logic blocks. You can use only one Block window at a time for editing; however, you can have additional Block windows open for viewing.

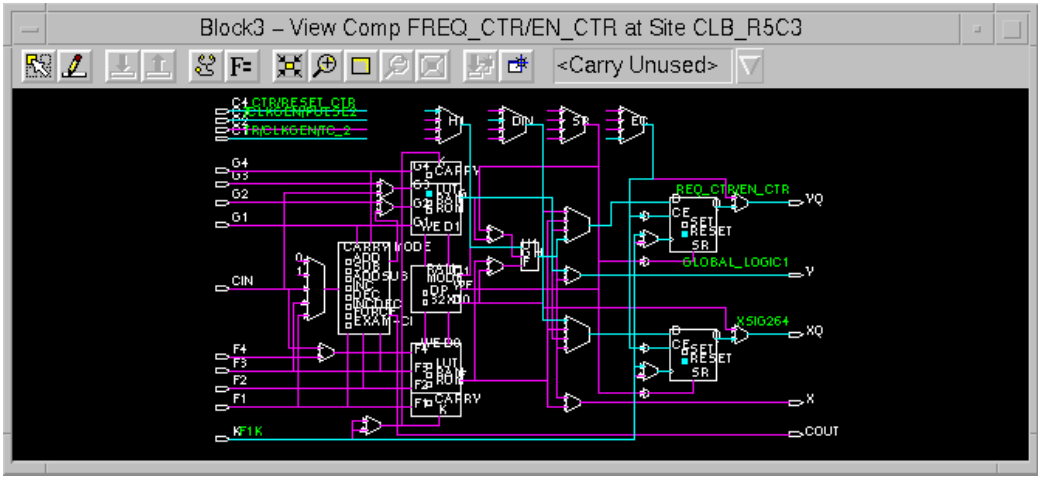


Figure 2-12 Block Window

Using Dialog Boxes

Many menu commands display dialog boxes in which you can enter information and set options.

Common Fields

The fields shown in the following table are common to most dialog boxes.

Table 2-3 Common Dialog Box Fields

Dialog Box Field	Function
OK	Closes the dialog box and implements the intended action according to the settings in the dialog box
Apply	Implements the intended action without closing the dialog box
Cancel	Closes the dialog box without effecting any action
Help	Displays information on that particular dialog box

Browse Buttons

Many dialog boxes contain browse buttons to allow you to navigate through your directory structure to find a particular file or to save a file to a specific location. In the FPGA Editor, the browse button appears as a small box with three dots to the right of the file name field.

Moving Items within List Boxes

Some of the dialog boxes feature list boxes. You can select and move items from one list box to another using either the mouse or the keyboard, or a combination of these methods.

Use the mouse to select items in list boxes as follows.

- To move an item to a list box on the right, select it with the left mouse button. Click the **>** button. To move an item to a list box on the left, select it, then click the **<** button.

- To move all items to a list box on the right, click the **>>** button. To move all items to a list box on the left, click the **<<** button.
- To move sequential items, select the first one with the left mouse button. Hold down the **Shift** key. Select the last item and release the **Shift** key. Click the **>** or **<** button to move the selected items to the right or left list box, respectively.

  You can also select the first item; drag the mouse up or down until all the desired items are highlighted; and then click the **>** or **<** button.
- To move multiple items in any order, hold down the **Ctrl** key while clicking individual items. When you finish selecting, release the **Ctrl** key and click the **>** or **<** button.

Use the keyboard to select items in list boxes as follows.

- To move an item in a list box, press the **Tab** key until the first item in the list box is highlighted. Press the down arrow key to select the desired item. Tab to the **>** or **<** button to move it to the right or left list box, respectively. Press the **Space** bar.
- To move all items to a list box on the right, tab to the **>>** button and press the **Space** bar. To move all items to a list box on the left, tab to the **<<** button and press the **Space** bar.
- To move consecutive items, tab to the first item in the list box. Use the down arrow key to highlight the first desired item. Press and hold the **Shift** key while using the down arrow key to select the other items in the sequence. Tab to the **>** button. Press the **Space** bar.

Using Filters with Commands

Some menu commands have dialog boxes that allow you to filter a list of choices, that is, display a subset of the listed items. These dialog boxes contain a filter field, Apply buttons, and Clear or Reset buttons.

In filter fields, you can enter a text string consisting of characters and wildcards. You cannot enter a range of items in filter fields.

- Characters can be any alphanumeric characters, text spaces, and the characters that appear on the top of the number keys on a keyboard. Alphabetic characters are case-sensitive. Control characters are not permitted.

- A wildcard can be an asterisk (*), which can represent any number of characters, or a question mark (?), which represents a single character.

The software does not strictly match patterns; it matches entire text strings. It does not find a string if it is embedded in a larger string unless you use wildcards. For example, it does not find $1N36 if it is embedded in ABC$1N36XYZ. However, if you searched for *$1N36*, it would find that string in ABC$1N36XYZ.

To use the Filter dialog boxes, follow these steps.

1. Specify the pattern to include in your list by typing the characters.
2. Include one or more wildcards (*) to do a global search on the specified string.

   Precede the character string with a wildcard to retrieve all signal names that end with the string of specified characters.

   Append the wildcard to the character string to retrieve all signal names that start with the specified character string.
3. Click **Apply**.

   The list displays only the choices that match the selection criteria.

Using Help

Most graphical user interfaces (GUIs) contain context-sensitive help and a Help menu. You can obtain help on commands and procedures with the Help menu or by selecting the Help toolbar button. In addition, the dialog boxes associated with many commands have a Help button that you can click to obtain context-sensitive help.

Help Menu

Use the following Help menu commands to obtain help.

- The Help Topics command opens Help and lists the online help topics available. From the Contents page, you can jump to command information or step-by-step instructions. After you open help, you can click the Help Topics button in the Help window whenever you want to return to the help topic list.

- The Online Documentation command opens the software manuals in the default Web browser.
- The About FPGA Editor command opens a popup window that displays the version number of the tool and a copyright notice.

Toolbar Help Button

You can obtain context-sensitive help from the toolbar as follows.

1. Click the Help button in the toolbar.

   The cursor changes to a question mark.

2. With the left mouse button, click the menu item or toolbar button for which you want help.

   Help appears for the selected command or option.

Note: You can also press **Shift F1** to obtain context-sensitive help.

F1 Key

Pressing the F1 key on a dialog box displays help on that dialog box. Pressing the F1 key is the same as selecting Help Topics from the Help menu, if no dialog boxes are displayed.

Help Button in Dialog Boxes

Many of the dialog boxes have a Help button that you can click to obtain help for the dialog box with which you are working. You can also press **Alt H** on your keyboard while the dialog has the keyboard focus to obtain help.

Using the Mouse and Keyboard

Use the mouse to perform the following operations on the workstation and the PC.

Table 2-4 Using the Mouse

Mouse Action	Function
Left Click	To select toolbar buttons, menus, menu commands, dialog box options, design objects
Ctrl+ Right Click	To zoom in
Shift+Ctrl+ Right Click	To zoom out
Right Drag	To pan

You can also customize the mouse buttons to perform operations other than those shown. The procedure for customizing mouse buttons is described in the "Customizing the FPGA Editor" chapter.

Zooming with the Mouse

To zoom in or out, click the appropriate button on your mouse. The FPGA Editor window zooms by a preset factor. The number of available zoom levels in the Array window is five by default.

Zoom Toggle

The zoom toggle feature allows you to toggle from an inner zoom level to the outermost zoom level and back. This feature is useful when you want to remain at a zoom level that provides good visibility for editing. For example, to move to a location outside your current editing area, but maintain the selected zoom level, use the zoom toggle to go to the outer zoom level, move the cursor to the desired location, and zoom back in.

To perform a zoom toggle, place the cursor in the Array window and type the letter "z" or "Z." If you begin at a zoomed-in level, you zoom out to the maximum zoom level; if you zoom toggle again, you return to the previous zoom level.

Panning

Panning keystrokes are defined in the FPGA Editor initialization (fpga_editor.ini) file and are summarized in the following table. You

can also use the World window to pan to a selected area. This panning method is described in the "Main Window" section.

To pan, you must zoom in at least one level and position the mouse cursor in the Array window. You can perform any of the following operations to pan in the FPGA Editor window.

- For smooth panning, hold down the right mouse button and drag the mouse. The window pans in the direction of the mouse movement. Panning continues until you reach the edge of the window or until you release the mouse button.
- When you reach the edge of the window with the cursor, the FPGA Editor will autopan the window until the edge of the FPGA device is reached. If you are near the edge of the window, the autopanning is slower than when you are far from the edge of the window.
- Use the keyboard arrow keys to pan left, right, up, or down.
- Use the Shift key with one of the arrow keys to pan the window to its furthest boundary in the direction of the arrow key.
- Press the space bar to center the display around the cursor position.

Table 2-5 Panning Keystrokes

Keystrokes	Result
Up arrow (↑)	Pan up 75% of one window height.
Shift + ↑	Pan to upper edge of device.
Down arrow (↓)	Pan down 75% of one window height.
Shift + ↓	Pan to lower edge of device.
Left arrow (←)	Pan left 75% of one window height.
Shift + ←	Pan to left edge of device.
Right arrow (→)	Pan right 75% of one window height.
Shift + →	Pan to right edge of device.
space bar	Center display around current cursor position.

Chapter 3

Using the FPGA Editor

This chapter includes information on performing various operations on your designs within the FPGA Editor. It includes the following sections.

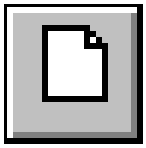
Note: You can select from the pull-down menus or the User toolbar, or you can enter commands in the Command Line toolbar. Selecting commands from the pull-down menus is described for most of the procedures in this chapter.

- "Creating a New Design File"
- "Opening an Existing Design File"
- "Saving a Design File"
- "Recovering a Terminated FPGA Editor Session"
- "Editing Your Design"
- "Adding Objects"
- "Deleting Objects"
- "Highlighting Objects"
- "Viewing and Changing Properties"
- "Moving and Swapping Components and Macros"
- "Editing Component Logic"
- "Placing and Unplacing Components"
- "Routing and Unrouting"
- "Constraints"
- "Adding Probes to Your Design"
- "Verifying Your Design"

Creating a New Design File

To create a new design in the FPGA Editor, follow these steps.

1. Select **File** → **New** or click on the New toolbar button.



   The New dialog box appears, as shown in the "New Dialog Box" figure of the "Menu Commands" chapter.

2. Select the **Design** option.
3. Enter the design name in the Design File field. If you do not enter the .ncd extension, it is automatically added when the file is created.

   You can open a new design under a directory other than the current working directory. Type in the path name of the target directory in the Design File field, or use the browse button to select your target directory and specify your design file name.

4. In the New dialog box, enter the constraints file name in the Physical Constraints File field, or use the browse button to specify the directory and file name. If you do not enter the .pcf extension, it is automatically added to your file name. If you do not enter a file name, a constraints file is created with the same name as the .ncd file but with a.pcf extension.
5. Click the Select Part button to display the Part Selector dialog box, shown in the "Part Selector Dialog Box" figure of the "Menu Commands" chapter.
6. Select a Family, Device, Package, and Speed Grade for your design.

Note: You can only select a part number from a part library you have installed on your system.

7. Click **OK**. The Part field in the New dialog box is filled in with your selections.
8. Click **OK** to close the New dialog box.

An empty (unprogrammed) design is loaded into the FPGA Editor window with the part number and speed as specified.

Opening an Existing Design File

To open an existing design file while you are in the FPGA Editor window follow these steps.

1. Select **File** → **Open** or click on the Open toolbar button.

   The Open dialog box appears, as shown in the “Open Dialog Box” figure of the “Menu Commands” chapter.

2. Select the **Design** option.
3. Enter the name of the .ncd file you want to open in the Design File field, or use the browse button to specify the design file name and directory.
4. Optionally, enter a constraints file name in the Physical Constraints File field, or click the browse button to specify the constraints file name and directory.

   If you do not enter a file name in the Constraints File field, the FPGA Editor looks for a constraints file with the same name as the .ncd file but with a.pcf extension.

5. Select an Edit Mode for the design from the pull-down list box.

   Select Read Only, No Logic Changes, or Read Write. The default is No Logic Changes. To always edit an existing design file in Read Write Mode, enter the following command in the fpga_editor.ini or fpga_editor_user.ini initialization files.

   setattr main edit-mode read-write

6. Click **OK**.

   The design file you specified is loaded in the FPGA Editor window.

Saving a Design File

You can save your design at any time during an FPGA Editor session in one of these variations.

- Current design under the same name
- Current design with a different name
- Design as a macro library file

Note: The first two methods are described following. The procedure for saving a design as a macro library file is described in the "Working with Physical Macros" chapter.

With the Same Name

To save your current design, select **File** → **Save**. The current design file is written to disk.

With a Different Name

1. Select **File** → **Save As** to display the Save As dialog box, shown in the "Save As Dialog Box" figure of the "Menu Commands" chapter.
2. Select the **Design** option.
3. Enter the design name in the Design File field. If you do not enter the .ncd extension, it is automatically added to the file name.

   You can save your design under a directory other than the current working directory. Type in the path name of the target directory in the Design File field, or use the browse button to select your target directory and specify your design file name.
4. If applicable, enter the constraints file name for the design in the Physical Constraints File field, or use the browse button to select a directory and specify a file name.

   If you do not enter a file name in the Constraints File field, a constraint file is saved with the same name as the .ncd file but with a.pcf extension. A constraints file is created only if there are existing constraints associated with your design.
5. Click **OK**.

The dialog box closes, and the design file and constraints files are saved with the names you specified. The file name in the Title Bar at the top of the FPGA Editor window changes to indicate that this new file is currently displayed in the window. When you later save or exit the file, it is saved to the new file name, not the original file name.

Recovering a Terminated FPGA Editor Session

During an editing session, the system keeps track of all commands performed on your design. The commands are written into a temporary command log file, *design_name*_fpga_editor.out, in the same directory where your design is located. This file is updated as each command is performed.

You can set the number of saved commands in the fpga_editor.ini file, or in the fpga_editor_user.ini file. See the flush_rate attribute in "Setattr" section of the "Command Line Syntax" chapter. The default is to update the file after each ten commands. Each time you save a design file, the commands are erased from *design_name*_fpga_editor.out.

When you end an FPGA Editor session, this file is erased when the FPGA Editor window closes. However, if a session is unexpectedly terminated (for example, if you lose power or a software error causes the session to end prematurely), the *design_name*_fpga_editor.out file remains in your current design directory.

The next time you start the FPGA Editor, the *design_name*_fpga_editor.out file is renamed *design_name*_fpga_editor.rcv. A new *design_name*_fpga_editor.out file is created for the current FPGA Editor session. A message box appears in the FPGA Editor Array window with a message similar to the following.

```
A crash recovery file was found for this design
indicating that fpga_editor previously terminated
abnormally. The changes that you made can be
recovered. (This process will overwrite your current
design file).

Do you want to run recovery?
```

If you want to run recovery, click **Yes**. Click **No** if you do not want to run the recovery process. The recovery process executes the

commands in the *design_name*_fpga_editor.rcv, restoring the session up to the point where it was terminated. If you do not run the recovery process, the *design_name*.rcv file is ignored and the commands in the file are not applied to the design file.

The recovery file records the number of valid commands in order to prevent repeating the command that caused the abnormal termination of the FPGA Editor. However, some commands issued before the command that caused the crash may not be replayed as well.

Editing Your Design

This section describes the various functions you can perform in the FPGA Editor to change the configuration of your design. The changes you make become part of your design's database. You can perform the following editing functions.

- Selecting objects
- Adding objects
- Deleting objects
- Viewing and changing object properties
- Swapping components and net pins
- Placing components
- Editing logic block contents
- Routing nets
- Editing constraints
- Canceling commands

The following sections describe each of these functions.

Note: The Automatic Routing option automatically routes any unrouted connections created as a result of any design edits. If you do not want these connections routed automatically, you can disable Automatic Routing in the Main Properties property sheet. This procedure is described in the "Automatic Routing Option" section.

This section contains the following topics.

- "Selecting Objects"
- "Deselecting Objects"

- "Selecting Objects with the Mouse and Keyboard"
- "Selecting Objects with the List Window"
- "Selecting Objects with the Find Command"
- "Notes On Selecting Objects"

Selecting Objects

You can use the following methods to select an object in the FPGA Editor window.

- Move the mouse over an object in the Array window, and click the left mouse button. This method is usually the easiest. See the "Selecting Objects with the Mouse and Keyboard" section for more information.
- Display an object list in the List window, and click the left mouse button on an object. See the "Selecting Objects with the List Window" section for more information.
- Type the Select command in the Command Line toolbar along with the appropriate arguments. See the "Select" section of the "Command Line Syntax" chapter for details.
- Use the Find dialog box. See the "Selecting Objects with the Find Command" section for details.

In some cases, you can only select from a list or from the command line, because there is no graphical representation of the object in the Array window. You can select any of the following objects.

- Sites
- Site pins
- Components
- Component pins
- Nets
- Paths
- Macros
- Switch box pins
- Wires (pinwires, long lines, local lines)

- Route lines
- Object layers
- Constraints
- Ratsnest lines

When you select an object, it changes color and its name and attribute are displayed in the history section of the window. When you select a used wire (pinwire, long line or local line), the name of the net using the wire is displayed in the history area. When you select a used component pin (or net pin), the history area shows the pin name, the name of the net to which this pin belongs, and the delay time from the net source to this pin.

When you select additional objects, they also change color. You can select multiple objects of the same type and multiple types of objects. However, the objects you select must be appropriate for the action you are performing.

You can control whether design objects remain selected or are deselected after a command is performed with the Automatic Deselect option in the Main Properties sheet.

After you select the appropriate object or objects, initiate the command with any of the methods available in the FPGA Editor (such as menu, User toolbar, command alias, and so on).

Deselecting Objects

Use one of the following methods to deselect objects in your design.

- Select **`Edit`** → **`Unselect All`** to deselect all selected objects
- Click Clear in the User toolbar to deselect all selected objects
- Enter the Clear command in the Command Line toolbar to deselect all selected objects

Use the Clear command before performing another command to deselect any selected objects in your design. You can also check which objects are selected by looking in the World window. This window displays selected objects even when they are not visible in the Array window.

Selecting Objects with the Mouse and Keyboard

The following table lists the mouse and keyboard combinations for selecting and deselecting objects in your design as defined in the fpga_editor.ini file. These are the default settings. To customize these settings, see the "Customizing the FPGA Editor" chapter.

Table 3-1 Selecting Objects with Mouse/Keyboard

Mouse/Keyboard	Function
Single left mouse button click	Selects an object, and deselects all previously selected objects
Ctrl+left mouse button click	Toggles the selection status of the object, selecting it if not selected, and deselecting it if selected; use to select / deselect more than one object in your design
Shift+left mouse button click	Selects object; use to select more than one object in your design
Left mouse button click on empty space	Deselects all selected objects
Double click of left mouse button on component	Opens Block window
Ctrl+Shift+left mouse button click on route segment	Selects the net
Ctrl+Shift+left mouse button click on site or component pin	Selects route-throughs

Selecting Objects with the List Window

You can use the List window, shown in the "List Window" figure of the "Getting Started" chapter to display a list of the components, nets, paths, layers, constraints, or macros in your design. You can open multiple list windows simultaneously for your design by selecting **`Window`** → **`New`** → **`List Window.`**

Use the pull-down list box at the top of the window to specify which of the following design objects appear in the list.

Note: For more information on the List window, see the "Main Window" section of the "Getting Started" chapter.

- Routed and unrouted nets

- Placed and unplaced components
- Placed and unplaced macros
- Layers
- Paths
- Constraints

You can select items in the list with the following mouse and keyboard combinations.

Mouse/Keyboard	Function
Single left mouse button click	Use to select a single object in the list
Ctrl+left mouse button click	Use to select multiple objects in the list that are not in sequential order
Shift+left mouse button click	Use to select multiple objects in the list in sequential order

When you select an item in the List window, you are selecting the corresponding object in your design with that name. The selected object in the Array window is highlighted. You can then perform the same operations on the selected object that you can perform when you select the object in the Array window.

Customizing the List Window

Use the vertical and horizontal scroll bars if necessary to view the complete list of objects. You can also resize the window by positioning the cursor on any corner of the window. Press the left mouse button and drag the corner to the appropriate size.

Also, to view the full name of an object in the list, place the mouse pointer over the name. The full name appears in a popup box over the name. Optionally, you can use the left mouse button to stretch or shrink the right side of any of the column headers to resize the column width.

You can sort the entries in the list by clicking on any of the column headers in the list. For example, click the left mouse button on the Name column and the list is sorted alphabetically. If you have All Components listed, and click the left mouse button on the Type column, the components are listed alphabetically by type. Clicking on

any of the column headers sorts the list based on what is displayed in that column.

Click the right mouse button on any of the column names in the List window to display a popup menu with the following choices.

Table 3-2 List Window Popup Menu Commands

Popup Menu Command	Function
Sort Ascending	Sorts the list in ascending order either alphabetically or numerically
Sort Descending	Sorts the list in descending order either alphabetically or numerically
Move Column Left	Moves the selected column to the left
Move Column Right	Moves the selected column to the right
Save Column Layout	Saves the current column layout
Restore Column Layout	Restores column layout to the layout used at the beginning of your editing session, or to the last saved layout
Default Column Layout	Restores the column layout to the Xilinx-defined layout

Selecting Objects with the Find Command

Note: For more information on the Find command, see the "Find (Edit Menu)" section of the "Menu Commands" chapter.

You can also select objects in your design with the **`Edit`** → **`Find`** menu selection. This command displays the Find dialog box shown in the "Find Dialog Box" figure of the "Menu Commands" chapter. Use the pull-down list to select the type of object you want to find in your design, and enter the name of the object in the Name field. If you are zoomed in when you select Find, the Auto Pan option automatically pans to the search object. The Auto Clear option clears all previous selections so only the item you are searching for is selected.

As an alternative to using the Find dialog box, you can use the Select command with the Zoom Selection command in the Command Line toolbar. See the "Command Line Syntax" chapter for details on the Find, Select, and Zoom commands.

Selecting Objects with the Select Command

You can also select objects with the Select command in the Command Line toolbar. See the "Select" section of the "Command Line Syntax" chapter for the command line syntax and examples.

Notes On Selecting Objects

This section includes some additional information on selecting objects in your design.

- You cannot select unplaced components, paths, or macros directly in the Array window. However, you can select them using the List window and the Select command.
- You can select object layers, such as the components layer or the ratsnest layer. Layers are selected in order to change attributes for all objects in the layer, for example, to display all layer components in green.
- When you select a component, net, or macro name in the List window, it is highlighted and the corresponding object changes color in the Array window. When you select a component, net, or macro in the Array window, it changes color and its name appears selected in the List window. Selecting a constraint in the List window does not cause a corresponding highlight in the Array window. The only time you may want to select a constraint in the List window is when you want to delete it.
- Switch box pins are selectable in the Array window. When you select a switch box pin, the allowable connections from the selected pin to other pins within the switch box are displayed. You cannot perform any other operations on a selected switch box pin.
- Bring up the Block window for a component by double clicking the left mouse button on the component.
- When you select a ratsnest line, the entire net containing the ratsnest line is highlighted.
- Select a portion of a routed net by pressing the Ctrl+Shift key while selecting the portion of the net with the mouse.

- For architectures that allow route-throughs, highlight all available route-through paths for a site or component pin by pressing the Ctrl+Shift key while selecting the pin.

Adding Objects

When you add objects to your design, these new objects become part of your design's database. Use the Add command to perform these functions.

- Create new components
- Create new nets
- Add a component pin to an existing net
- Add a macro to your design

You can add objects in any of the following ways.

- Select **Edit** → **Add**
- Select **Add** in the User toolbar
- Enter **add** in the Command Line toolbar

Note: Objects cannot be added if the design is in the No Logic Changes Mode.

This section contains the following topics.

- "Adding Components"
- "Adding a Net"
- "Adding Component Pins to an Existing Net"

Adding Components

To add new components to the database use this procedure.

1. Select vacant sites in which to place the new components.

   You can select any type of site, for example, CLB, IOB, tristate buffer, pull-up resistor.

2. Select **Edit** → **Add**.

   The sites become components, and these new components can be connected to other components in your design.

The Component Properties property sheet may appear on the screen for each newly created component. Whether the property sheet appears or not is controlled by the Automatic Post main window property, see the "Main Window Properties" section. Each property sheet shows the name of the new component and the name of the site in which the component is placed.

3. You can edit the component properties in the property sheet and click **OK** or **Apply** to apply them, or **Cancel** to close the property sheet and maintain the defaults. See the "Component Properties" section for details.

Notes on Adding Components

This section includes some additional information on adding component to your design.

- When you add a component, the name assigned to the new component is in the format $COMP_*number*, where *number* is a number assigned to each new component. Numbering starts at 0 and increases by one for each new component. For example, if you already have 100 components and you add a component at site HF, the new component is named $COMP_101. The next component, added at site CF, is named $COMP_102, and so on. You can change the component's name by modifying the Component Properties property sheet.
- Any characters special to the FPGA Editor command interpreter must be preceded by a backslash (\) escape character when used in a component name. Special characters are quotation marks (" or ') * ; ? # – (leading dash). The restriction only applies to commands entered at the command line or those in an FPGA Editor command script file; the special characters may be entered in the Component Properties property sheet without the escape character.

Note: If you use a tool set other than the Xilinx tools, additional naming restrictions may apply.

- All components and nets have their own name space and all components and nets must have unique names within their own name space. For example, you can have a component and a net named "FRED," but you cannot have two components named "FRED" or two nets named "FRED." The FPGA Editor prevents you from entering non-unique names within a name space.

- When you add a component in the FPGA Editor, the component is assigned default programming. To determine the default programming, add the component, select it, and click the **Info** button in the User toolbar. The defaults are listed in the history area.

Adding a Net

To add a new net to the database use this procedure.

1. Select all component pins comprising the new net.

   Each of the selected pins must be on a placed component (not a site), and the selected pins must not belong to any other nets.

2. Use the Add command in any of the following ways to add a net.

   - Select **Edit** → **Add**.
   - Select **Add** in the User toolbar.
   - Enter **add** in the Command Line toolbar.

   The selected pins are joined as a net.

   After using the Add command, a Net Properties property sheet may appear for the newly created net. Whether the property sheet appears or not is controlled by the Automatic Post main window property. See the "Main Window Properties" section for details. The property sheet shows the name of the new net, the number of pins and the routing status. You can edit the net properties in this property sheet or select **Cancel**. See the "Net Properties" section for details.

   If the Automatic Routing Option is enabled, the new net is routed as completely as possible. If Automatic Routing is Off, ratsnest lines will connect the pins on the new net. For a description of the Automatic Routing option, see the "Automatic Routing Option" section.

Notes on Adding Nets

This section includes additional information on adding nets to your design.

- When you add nets, the name assigned to the first new net is $SIG_0; subsequently added nets will be named $SIG_1, $SIG_2,

and so forth. You can change this net name by using the Net Properties property sheet that appears when the net is added.

- Any characters special to the FPGA Editor command interpreter must be preceded by a backslash (\) escape character when used in a net name. Special characters are quotation marks (“ or ‘) * ; ? # – (leading dash). The restriction only applies to commands entered at the command line or those in an FPGA Editor command script file; the special characters may be entered in the Net Properties property sheet without the escape character.

Note: If you use a tool set other than XILINX tools, additional naming restrictions may apply.

- All nets and components have their own name space and all nets and components must have unique names within their own name space. For example, you can have a net and a component named “FRED,” but you cannot have two nets named “FRED” or two components named “FRED.” The FPGA Editor prevents you from entering non-unique names within a name space.

Adding Component Pins to an Existing Net

To add component pins to an existing net follow these steps.

1. In the Array window, select the component pins you want to add to the net.

   The selected pins must be on a placed component (not a site), and the selected pins must not belong to any other net.

2. Select the net to which you will add the pins in one of the following ways.

   - Display a list of nets in the List window, then select the net name from this list.
   - Select any net pin, ratsnest line, or routed segment on the desired net.
   - Enter the **`Select`** command in the Command Line toolbar.

3. Select **`Edit`** → **`Add`**.

   The selected pins are added to the net.

   If the Automatic Routing option is enabled, the new net pins will be routed to the net. If Automatic Routing is Off, ratsnest lines

will be drawn to the new net pins. For a description of Automatic Routing, see the "Automatic Routing Option" section.

Adding a Macro

Adding a macro to your design is described in the "Adding Macros to Your Design" section of the "Working with Physical Macros" chapter.

Deleting Objects

Deleting an object permanently removes it from the current design. You can delete these objects.

- Components
- Nets
- Net pins
- Macros
- Paths

Select the objects you want to delete, and then perform one of the following commands.

- Select **`Edit`** → **`Cut`**.
- Select **`Delete`** in the User toolbar.
- Enter **`delete`** in the Command Line toolbar.

This section contains the following topics.

- "Deleting Components"
- "Deleting Nets"
- "Deleting Net Pins"
- "Deleting Macros"
- "Deleting Paths"
- "Deleting Path Elements"

Deleting Components

When you delete a component, each net pin on the component is unrouted, each net pin is removed from its net, then the component is removed from the design database.

Note: Do not use the Unplace command to delete an object.

To delete components use these steps.

1. Select the components to delete.
2. Select the **Delete** command.

   The components are eliminated from the database. You cannot delete a component that is part of an instantiated macro.

Deleting Nets

When you delete a net, all net pins on the net are unrouted, each net pin is removed from the design database, then the net itself is removed from the database.

To delete a net follow these steps.

1. In the List window, display a list of net names.
2. Select the nets to delete.

   If you are not sure of the name of a net you want to delete, select a pin, ratsnest line, or route on the desired net.
3. Select the **Delete** command.

   The nets are eliminated from the database.

Deleting Net Pins

When you delete a signal pin, the pin is unrouted from the net to which it is attached, then the pin is removed from the net. A deleted pin no longer has any connection (logically or physically) to the net from which it was deleted.

To delete net pins follow these steps.

1. Select the net pins to delete.
2. Use the **Delete** command.

The net pins are removed from the nets to which they are attached and from the database.

Deleting Macros

Deleting a macro from the design is described in the "Deleting Macros from Your Design" section of the "Working with Physical Macros" chapter.

Deleting Paths

When you delete a path, you remove the Define Path constraint that defines the path. You also remove all constraints that directly depend on the Define Path constraint, such as Maxdelay Path.

To delete a path follow these steps.

1. Select the path to delete.

   Select the path name in the List window or enter the command **`Select Path`** [*path_name*] in the Command line toolbar

2. Select the **`Delete`** command.

   The next time you save the design, the Define Path constraint that originally defined the path is commented out in the constraints file.

Deleting Path Elements

You can delete nets or components from path definitions. When you delete them, they are not deleted from the design; they are only removed as elements in the path.

To delete nets or components from a path follow these steps.

1. Select the nets or components to remove from the path.
2. Enter the **`Delete Path`** [*path_name*] command.

   The [*path_name*] is the name of the path from which you will remove the nets or components.

   The selected nets or components are removed from the path definition. The next time your design is saved, the constraints file is modified, and the selected nets or components are removed from the Define Path constraint.

Highlighting Objects

When you edit a design in the FPGA Editor, you may want to change the color of (highlight) one or more objects for easy reference. Highlighting is especially useful in dense designs.

You must select the automatic highlighting option in the main window property sheet. See the "Main Window Properties" section for more information. The automatic highlighting option determines whether objects are automatically highlighted. When the option is enabled, delay paths are highlighted after a delay command, and nets are highlighted after a manual route. By default, this option is disabled. You can also set highlighting from the Command Line toolbar. See the "Setattr" section of the "Command Line Syntax" chapter.

Here are some additional reasons for highlighting.

- Highlighting makes it easier to find objects in your design.
- After running a path delay, you may want to highlight the path you just checked.
- You may want to highlight the routes added during manual routing.

Before you can use the highlight feature, the layer containing the objects that you want to highlight must be selected in the Layer Visibility toolbar.

You can highlight selected objects in the following ways.

- Select **Hilite** in the User toolbar.
- Select **View** → **Highlight**.
- Enter the **Hilite** command in the Command Line toolbar.

To change the color of a selected object to yellow, enter the following in the Command Line toolbar.

```
hilite -c yellow
```

See the "Hilite" section of the "Command Line Syntax" chapter for more information.

Selected objects are deselected based on the setting of the Automatic Deselect option in the Main Properties property sheet. If this option is not enabled, selected objects do not appear highlighted until you

select another object. If this option is enabled, highlighted objects appear in the proper color automatically.

Viewing and Changing Properties

You can view and change various properties for the following design objects.

- FPGA Editor window
- Components
- Component pins
- Nets
- Sites
- Ratsnest lines
- Wires (pinwires, local lines, and long lines)
- Macros
- Paths
- Object layers

Some of the properties you view and change represent constraints applied to your design. If you change these properties in the FPGA Editor, the resulting constraints changes are written into the constraints file when you save your design.

Use one of the following methods to display a property sheet for a selected object.

- Select **`Edit`** → **`Properties of Selected Items`**.
- Select **`Attrib`** in the User toolbar.
- Enter **`post attr`** in the Command Line toolbar.

If you want to post properties for more than one object, select all of the objects first. The property sheets are displayed for all of the selected components. The property sheets appear in the order in which the objects were selected.

You can modify some of the properties in the property sheet; some of the properties are read-only fields and cannot be modified. To acti-

vate any changes, click **OK** to close the property sheet, or click **Apply** to keep the property sheet open.

This section contains the following topics.

- "Getattr and Setattr Commands"
- "Main Window Properties"
- "Component Properties"
- "Pin Properties"
- "Net Properties"
- "Site Properties"
- "Wire Properties"
- "Macro Properties"
- "Path Properties"
- "Layer Properties"

Getattr and Setattr Commands

Two other FPGA Editor commands are related to object properties. Use the Getattr command to display properties for selected objects in the history window. You can also use the Info button in the User toolbar to display properties. Use the Setattr command to change properties for selected objects.

The information provided by the Getattr command is the same as that displayed in an object's property sheet. The properties changed with the Setattr command are the same properties you can modify in an object's property sheet. You may want to use these commands when you do not want to display the property sheet for the object. Getattr and Setattr are also described in the "Command Line Syntax" chapter.

The Getattr, Setattr, and Post Attr commands are all affected by the Automatic Deselect option in the Main Properties property sheet. When Automatic Deselect is enabled, selected objects are automatically deselected after a command is executed. If the Automatic Deselect option is disabled, the object remains selected.

Main Window Properties

To view or change properties for the main FPGA Editor window, perform one of the following commands.

- Make sure nothing is selected in the Array window or the List window, and select **File** → **Main Properties**
- Make sure nothing is selected in the Array window or the List window, and select **Attrib** in the User toolbar
- Make sure nothing is selected in the Array window or the List window, and enter **post attr** in the Command Line toolbar.

The Main Properties property sheet appears, as shown in "Main Properties Property Sheet" figure of the "Menu Commands" chapter. The various properties of the Main window are described in detail in the "Main Properties (File Menu)" section of the "Menu Commands" chapter.

Component Properties

The Component Properties property sheet appears when you select a component and select **Edit** → **Properties of Selected Items**. This property sheet contains the General, Configuration, and Physical Constraints pages.

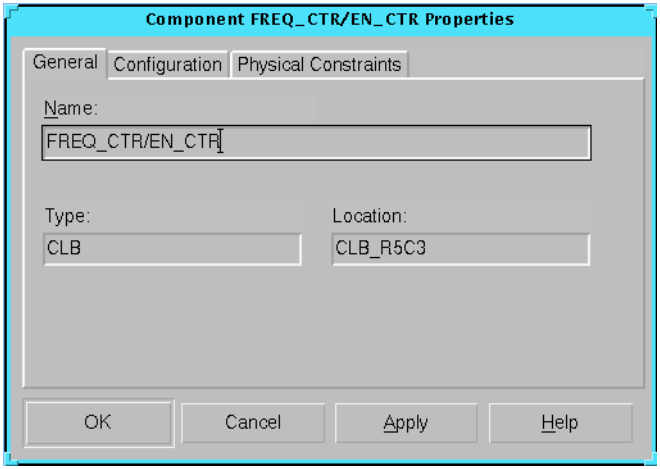


Figure 3-1 Component Properties Property Sheet

General Page

Refer to the following table for a description of the General page.

Property	Description
Name	Name of the component; there is no character limit
Type	Type of component, for example, CLB, TBUF, PULLUP
Location	Indicates the reference designator of the site in which the component is placed or indicates "unplaced"

Configuration Page

Note: The Configuration page is not displayed if the selected component is a protected or confidential component.

This page displays the internal programming of the CLB or IOB. You cannot edit any of the properties displayed on this page, and the properties may differ between device families. Use the Block window to modify CLB or IOBs. Refer to the following table for a description of some of the possible properties displayed in the Configuration page.

Property	Description
Base	Base mode of the component
Config	State of the component, including multiplexers and other logic elements
Feqn	Boolean equation for the F output of the component's combinatorial logic section
Geqn	Boolean equation for the Goutput of the component's combinatorial logic section
Heqn	Boolean equation for the Houtput of the component's combinatorial logic section
Carry	Component's carry strings

Physical Constraints Page

This page displays the constraints that are applied to the component. Refer to the following table for a description of the Physical Constraints page.

Property	Description
Lock Placement	Locks component to its current location
Requirement	Indicates whether the automatic placement range is an absolute requirement (HARD) or preferable (SOFT)
Effort	Sets up a priority for the autoplacer to resolve constraint conflicts
Location Range	Specifies the location of the site or range of sites for the autoplacer
Block Paths	A timing constraint to block the enumeration of all timing paths that go through this component
TSid	Assigns a timing period or frequency to a timing specification

Pin Properties

The Pin Properties property sheet appears when you select a site or component pin and select **Edit** → **Properties of Selected Items**. If the pin you select is a macro external pin, a different property sheet appears. See the “Macro External Pins in Your Design” section of the “Working with Physical Macros” chapter.

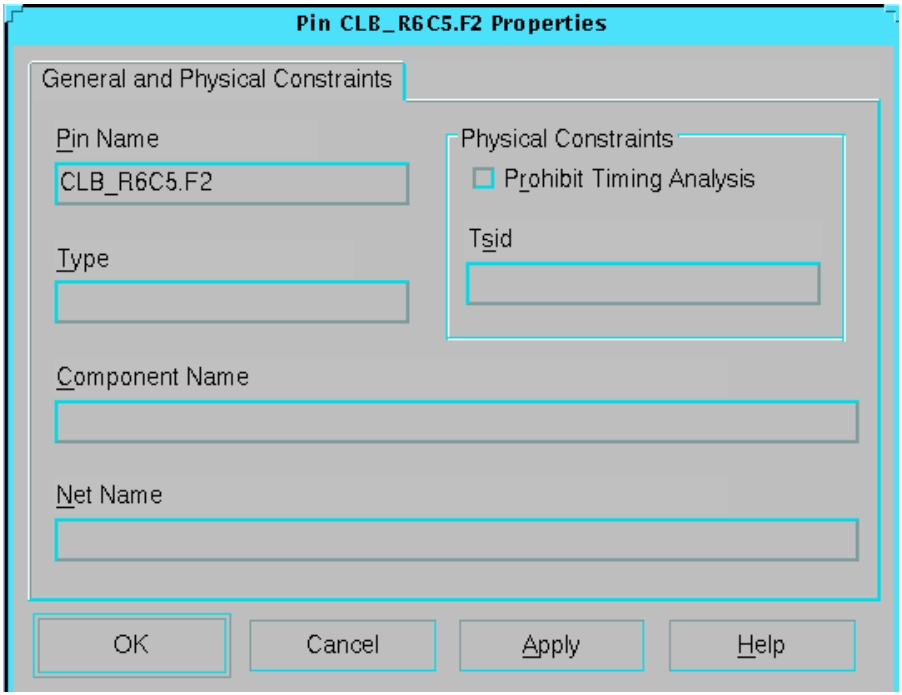


Figure 3-2 Pin Properties Property Sheet

Refer to the following table for a description of the General and Physical Constraints page properties. Only the Physical Constraints fields can be edited.

Property	Description
Pin Name	Name of the pin
Type	Indicates whether the pin is an INPUT, OUTPUT, TRISTATE, or CLOCK pin
Component Name	Name of the component containing the pin
Net Name	Name of the net to which this pin belongs. If the pin is unused, NO SIGNAL appears

Property	Description
Prohibit Timing Analysis	Applies a Timing IGnore (TIG) constraint to the pin, which prevents timing analysis on paths through that pin.
TSid	Assigns a timing period or frequency to a timing specification

Net Properties

The Net Properties property sheet appears when you select a net and select **Edit** → **Properties of Selected Items**. This property sheet contains the General, Physical Constraints, and Pins pages. A partially or fully routed net can be selected by pressing the Shift key while selecting any routed segment on the net. An unrouted net can be selected by selecting the ratsnest; by selecting its name from a list in the List window; or by using the Select command in the Command Line toolbar.

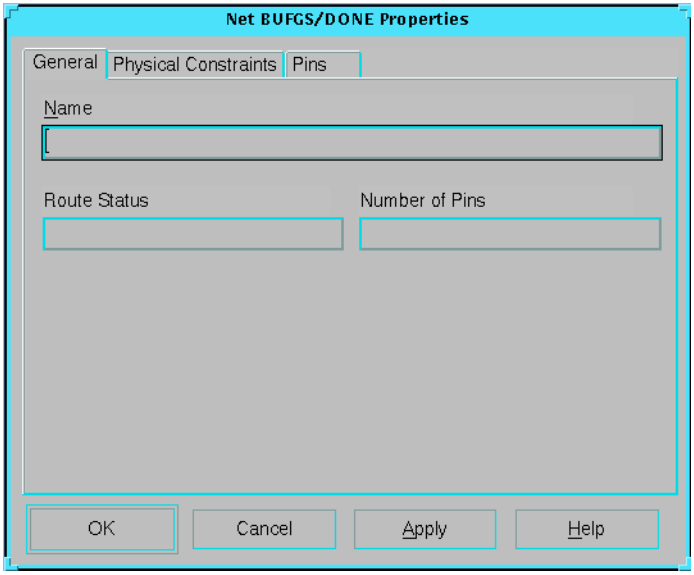


Figure 3-3 Net Properties Property Sheet

General Page

Refer to the following table for a description of the General page.

Property	Description
Name	Net name
Route Status	Indicates whether the net is UNROUTED, PARTIALLY ROUTED, or FULLY ROUTED. For VCC and Ground nets, the status is preceded with either PWR or GND.
Number of Pins	Indicates how many net pins this net contains

Physical Constraints Page

This page displays the constraints that have been applied to the net. Refer to the following table for a description of the Physical Constraints page.

Table 3-3 Physical Constraints Page

Property	Description
Lock Status	Indicates whether the net is locked or unlocked. If net is locked, also indicates whether the net is locked due to a lock net or lock routing constraints. A locked net cannot be unrouted or deleted. Pins and components connected to the net cannot be unplaced, swapped, or deleted.
Lock Routing of this Net	Locks the net by applying a Lock Net constraint; this net cannot be unrouted or deleted.
Prohibit Timing Analysis	Applies a Block Net constraint to the net, which prevents timing analysis on the named net and on all paths through the named net.
Period (ns)	Applies a Period constraint to the net, which assigns a clock period for all sequential output and input pins clocked by the net. Enter a period or a frequency in this field, but not both.
First Pulse	Specifies whether the first pulse of the duty cycle will be High or Low. The field immediately to the right of this field specifies the duration of the first pulse of the duty cycle.

Table 3-3 Physical Constraints Page

Property	Description
Duration (ns)	Specifies the duration of the first pulse of the duty cycle.
TSid	Assigns a timing period or frequency to a timing specification.
Phase (ns)	Generates a derived clock based on the period of an existing timing constraint. This constraint is the master and the derived constraint is the slave. Phase is the delay of the initial edge of the master to the slave.
Factor	Generates a derived clock based on the period of an existing timing constraint. This constraint is the master and the derived constraint is the slave. Factor is a multiplier period of the master used to create a relative one for the slave. For example, if the period for the slave is one half that of the master, use a value of 0.5.
Max Skew	Applies a maxskew constraint to the clock net. The maxskew constraint specifies the difference between the minimum and maximum load delays on the net.
Route Priority	Nets with a higher priority are routed first.
Delay (ns)	Applies a Maxdelay constraint to the net, which specifies a maximum total delay for the driver-to-load connections on the net.
Priority	Applies a Prioritize Net constraint to the net. The constraint assigns a weighted importance (0–100) to the named net (with 0 as least important and 100 as most important). A net with a priority of 3 or less is not considered critical.

Pins Page

This page displays the net pins comprising the net. You cannot edit any of the information in the Pins page. The Pins page only displays information for net pins on placed components. To view a pin in the Array window, click the left mouse button on any of the pins listed,

enable the Synchronize pin selection with array window option, and click Zoom. Refer to the following table for a description of the Pins page.

Property	Description
Name	Name of the pin, in the form, reference_designator.pin_name
Type	Indicates whether the pin is an INPUT, OUTPUT, TRISTATE, or CLOCK pin
Delay (ns)	Delay time from the net source to this pin. This field is blank if the pin is unrouted. For VCC and ground pins, the delay is indicated with a dash.

Site Properties

The Site Properties property sheet appears when you select a site and select **Edit** → **Properties of Selected Items**.

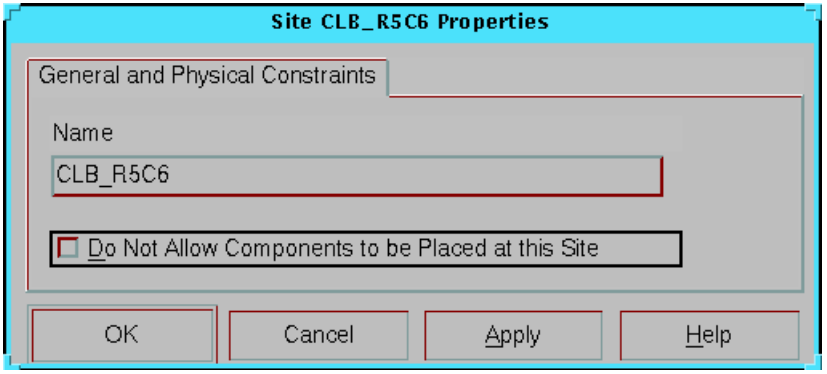


Figure 3-4 Site Properties Property Sheet

Refer to the following table for a description of the General and Physical Constraints page properties. Use the Do Not Allow Components to be Placed at this Site option to apply a Prohibit Site constraint to the site. This constraint specifies that a component cannot be placed at this site. You may want to reserve a site for future use.

Property	Description
Name	Name of the site

Wire Properties

The Wire Properties property sheet, shown in the following figure, appears when you select a pinwire, a local line, or a long line and select **Edit** → **Properties of Selected Items**. The property sheet appears whether you select a routed or an unrouted portion of a wire. You cannot modify any of the properties in this property sheet.

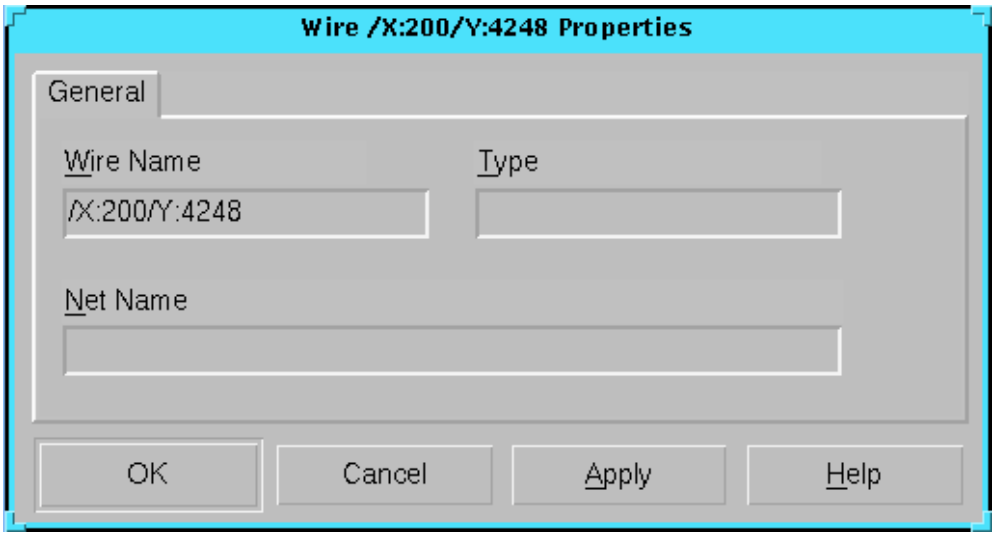


Figure 3-5 Wire Properties Property Sheet

Refer to the following table for a description of the Wire properties.

Property	Description
Wire Name	Name of the wire
Type	Indicates whether the selected wire is a PINWIRE, LOCAL line, LONG line, SWITCH BOX line, or PROGRAMMED SWITCH.
Net Name	Specifies the net routed along this wire.

Macro Properties

Macro properties are described in the “Viewing and Changing Macro Properties in Your Design” section of the “Working with Physical Macros” chapter.

Path Properties

The Path Properties property sheet, shown in "Path Properties" section appears when you select a path and select **Edit** → **Properties of Selected Items**.

Refer to the following table for a description of the Path properties.

Property	Description
Name	Name of the selected path
Elements	Names of the components and nets comprising the path.
Prohibit Timing Analysis	Indicates that a Block Path constraint is applied to the path, which blocks timing analysis on the path
TSid	Assigns a timing period or frequency to a timing specification
Maxdelay	Applies a Maxdelay constraint to the path, which specifies the maximum delay for the path
Priority	Lists the priority and the locked attribute for the Q1 net

Layer Properties

An FPGA Editor layer contains all of one type of object, for example, all long lines in the device or all components in the design database. To see a list of all available layers, select Layers in the List window.

The Layer Properties property sheet appears when you select any FPGA Editor layer and select **Edit** → **Properties of Selected Items**. Layers cannot be selected in the Array window; they must be selected from the layers list in the List window or by using the Select command in the Command Line toolbar.

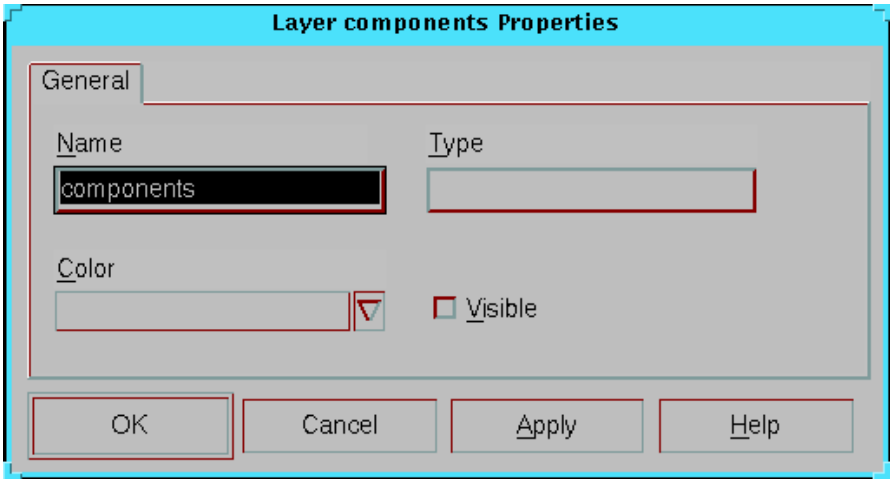


Figure 3-6 Layer Properties Property Sheet

Refer to the following table for a description of the Layer properties.

Property	Description
Name	Type of object in the layer
Type	Indicates what type of layer: BLOCK, WIRE, NODE, or OTHER
Color	Determines the color of objects in the layer; use the pull-down list box to select a color
Visible	If enabled, the layer appears in the Array window

Moving and Swapping Components and Macros

Use the Swap command to move a placed component to an unused site, to move a placed macro to an unused series of sites, or to swap the locations of two placed components.

Moving Components

To move a component to an unused site, perform the following steps. In this procedure, the component you are moving must be a placed component. Steps 1 and 2 can be done in either order.

1. Select the component you want to move.

2. Select the unused site to which you want to move the component.

   The component and the site must be the same type of block: IOB and IOB, or CLB and CLB.

3. Select **Edit** → **Swap**.

   The component moves to the unused site. If Automatic Routing is On, the component is routed after it is placed.

Moving Macros

Moving macros is described in the "Moving Macros in Your Design" section of the "Working with Physical Macros" chapter.

Swapping Components

To swap the locations of two components, perform the following steps.

Note: The components you are swapping must both be placed components.

1. Select one of the components to swap.
2. Select the second component.

   Both components must be the same type of block: IOB and IOB, or CLB and CLB.

3. Select **Edit** → **Swap**.

   The two components are unrouted, and their locations are switched. If Automatic Routing is Off, the components remain unrouted after the swap, even if they were routed before the swap. If Automatic Routing is On, the two components are routed after they are swapped.

Swapping Component Pins

You can also use the Swap command to swap pins on a component. You can swap pins on all Xilinx devices.

The FPGA Editor only allows you to swap pins that are permitted for the mode in which the component is programmed. When the pins are swapped, the internal component logic is modified to match the new pin positions.

To swap component pins, perform the following steps.

1. Select the two pins you want to swap.
2. Select **Edit** → **Swap**.

   The two pins are unrouted, and their locations are switched. If Automatic Routing is Off, the pins remain unrouted after the swap, even if they were routed before the swap. If Automatic Routing is On, the two pins are routed after they are swapped. The programming of the component changes to reflect the pin swap.

Editing Component Logic

You can use the Block window in the FPGA Editor to modify or create component logic. See the "Block Window" figure of the "Getting Started" chapter. You can use only one block window at a time for editing; however, you can have additional block windows open for viewing.

To edit a component's internal logic, perform one of the following.

- Double click the left mouse button on a component, and then press the second to the left button in the block window's toolbar (the Begin Editing button). If it is disabled, check to make sure the edit mode is read-write.
- Select a component and select the **Editblock** command in the User toolbar
- Select a component and enter **editblock** in the Command Line toolbar

Notes on Editing a Component

- Look-up tables (LUT) and flip-flops have several check boxes associated with them. You can enable a LUT or flip-flop by selecting the appropriate check box.
- You can also specify carry mode by selecting the appropriate check box.
- Multiplexer (MUX) symbols have triangular input pins. You can click on the appropriate pin to highlight the path through that pin.

- You can create LUT equations by using attributes for the component. In the Block window, click on the Show / Hide Attributes toolbar button. Equations are a boolean representation of the logic; for example, F4 + (~F3*F2).

Placing and Unplacing Components

Note: For information on placing or unplacing macros, see the "Working with Physical Macros" chapter.

Components can be placed in the Array window either automatically or manually. When you use automatic placement (AutoPlace), the system selects an appropriate site or sites for each component you select for placement. When you use manual placement, you select both a source component and the destination site in which to place it.

The automatic placement software selects sites based on routability. You can automatically place selected components or automatically place all remaining unplaced components in your design.

You can also unplace components. Unplacing unroutes each net pin on the components you select, and removes the components from the Array window and adds them to the list of your design's unplaced components.

This section contains the following topics.

- "Automatically Placing Selected Components"
- "Automatically Placing All Unplaced Components"
- "Manually Placing Selected Components"
- "Unplacing Components"

Automatically Placing Selected Components

You can automatically place selected components with the Autoplace command. To automatically place selected components, perform the following procedure.

1. In the List window, display a list of unplaced components.
2. In the list of unplaced components, select the components to automatically place.
3. Select **Tools** → **Place** → **AutoPlace**.

The selected components are automatically placed in vacant sites in the Array window. If the Automatic Routing Option is On, the components are routed after they are placed.

Notes on Placing Selected Components

This section includes some additional information on placing components.

- Before the selected components are automatically placed, any unplaced pull-ups or tristate buffers in your design are automatically placed.
- Placing certain components may cause other related components to be placed.
- Because the Place and Route program (PAR) unroutes and places components more efficiently than the FPGA Editor, when you automatically place components in the FPGA Editor, existing routing is *not* unrouted and rerouted to achieve better placement.

Automatically Placing All Unplaced Components

To automatically place all unplaced components, perform the following procedure.

1. Select **Tools** → **Place** → **AutoPlace All.**

   The "Autoplace All Components Dialog Box" figure of the "Menu Commands" chapter appears. Refer to this chapter for a description of the fields in this dialog box.

2. Click **OK**.

   All of your design's unplaced components are automatically placed in vacant sites in the Array window. If the Automatic Routing Option is On, the Autoroute All dialog box appears and you are prompted for information on the type of automatic placement. If it is not On, select autoroute -all.

Note: When you autoplace all remaining components in the FPGA Editor, existing routing is *not* unrouted and rerouted to accommodate the new placement. Because PAR unroutes components if necessary, placement done with PAR produces different results than placement done in the FPGA Editor. PAR places components more efficiently,

and a densely packed design can more easily be placed and routed with PAR than with the FPGA Editor.

Manually Placing Selected Components

To manually place an unplaced component, follow this procedure.

1. In the List window, display a list of unplaced components.
2. Select one name from the list.
3. Select a vacant site in the Array window.

   The component and the site must be the same type of block (for example, IOB and IOB, or CLB and CLB).
4. Select **Tools** → **Place** → **Manual Place**.

   The component is placed in the site. If the Automatic Routing Option is On, the component is routed after it is placed.

Unplacing Components

The Unplace command removes all or selected components from their current sites. Before unplacing a component, the system unroutes each component pin on the component.

Note: Locked components cannot be unplaced.

Selected Components

To unplace selected components use the following procedure.

1. Select placed components from the List window.
2. Select **Tools** → **Place** → **Unplace**.

   The selected components are unplaced. These components now appear as unplaced in the List window.

All Components

To unplace all placed components in your design, follow these steps.

1. Select **Tools** → **Place** → **Unplace All**.
2. Select **Yes** in the confirmation box that appears to unplace all components.

All unlocked placed components in your design are unplaced.

Routing and Unrouting

All or selected connections can be routed in the Array window automatically or manually. When you use automatic routing, the system selects the routing path for each connection you select. In manual routing, you specify the routing path.

You can enable the Automatic Routing option to automatically route any unrouted net pins created as a result of an editing action, such as placing a component or creating a new net. Automatic Routing, when enabled, occurs after add, place, autoplace, and swap operations.

You can also unroute connections. Unrouting removes the routing from any specified routes without eliminating the logical connections of the nets.

This section contains the following topics.

- "Automatic Routing"
- "Manual Routing"
- "Automatic Routing Option"
- "Unrouting"

Automatic Routing

Use the AutoRoute command to automatically route selected design objects, including the following.

- Nets
- Net pins
- Ratsnest lines
- Components
- Macros

In addition, you can autoroute between two resources including the following.

- Route segments
- Used wires

- Used or unused component pins

Note: If both resources are used, they must be on the same net.

To automatically route selected objects, follow these steps.

1. Select the objects you want to automatically route.

   You can select any combination of nets, net pins, ratsnest lines and components and macros. Net pins, ratsnest lines, components, macros, and partially or fully routed nets in the Array window. Unrouted nets can only be selected in the List window.

2. Select **Tools** → **Route** → **Auto Route**.

   The objects you selected are routed (if possible). The display for each routed connection changes from a ratsnest display to a routed net display. If an object could not be completely routed, an error message appears in the history area and the ratsnest remains.

Notes on Automatically Routing Selected Objects

This section includes additional information on automatically routing selected objects.

- When an output pin (a net driver) is automatically routed, the entire net is routed. When an input pin (a net load) is automatically routed, the connection between the pin and the net driver is routed.
- When a component is automatically routed, each net pin on the component is routed.
- When a net or a ratsnest line is automatically routed, the entire net is routed.
- Delay-based autorouting uses delay values when routing your design. If this type of autorouting is disabled, cost-based autorouting is performed instead. Delay-based autorouting takes longer, but can result in better routing, especially in a dense design. By default, delay-based autorouting is enabled; this option has no effect when you autoroute all nets.
- When selected objects are autorouted in the FPGA Editor, existing routing is *not* unrouted and rerouted to accommodate new routing. Also, component pins are not swapped for a better routing. Because the PAR program unroutes routes and swaps

pins if necessary, routing with PAR is more efficient than routing in the FPGA Editor.

- You can select and then autoroute two objects on a single net. The two objects can be any combination of a net pin, a route segment, a local line, a long line, or a pinwire used by the net. The Autoroute command attempts to route a path between the two selected objects.

If you do not want the pin to be routed with the vertical local line selected by the software, you can specify a different path for the route by selecting the pin and the horizontal local line already used for the net routing.

To automatically route your entire design use the following procedure.

1. Select **Tools** → **Route** → **Auto Route All**.

   The Autoroute All Nets dialog box appears, as shown in the "Autoroute All Nets Dialog Box" figure of the "Menu Commands" chapter.

   The fields in this dialog box are described in the "Autoroute All Nets Dialog Box Options" section of the "Menu Commands" chapter.

2. Specify the routing options you want and click **OK** to close the dialog box.

   All unrouted connections are routed if possible. The display for each routed connection changes from a ratsnest display to a routed net display. If a net cannot be routed to completion, an error message appears in the history area.

Notes on Automatically Routing the Entire Design

This section includes additional information on automatically routing your entire design.

- When your entire design is automatically routed, the following default routing options are performed.
  - Three iterations of the router
  - One cost-based cleanup pass
  - No delay-based cleanup passes

- To specify the number of routing iterations instead of accepting the default value (3), enter a different value in the Number of Passes field in the Autoroute All Nets dialog box. The number (1 to 999) specifies the maximum number of iterations performed. The router continues to perform iterations until one of the following events occurs.
  - Your design is routed to completion and constraints are met.
  - The router completes the number of iterations you specified.
  - The router cannot route your design to completion or meet constraints.
- When your entire design is routed, existing routing is *not* unrouted and rerouted to accommodate new routing. Because the PAR program unroutes routes and swaps pins if necessary, routing with PAR is more efficient than routing in the FPGA Editor.

Manual Routing

Use the Route command to manually route your design. Manual routing allows you to specify the path for the signal routing. Select the net pins or pinwires to connect and the routing resources to use, for example, long lines or local lines, and the system routes the specified path. As part of the manual routing, you can select unused pins on placed components and then route these pins together to form a new net, or route them to an existing net.

To manually route your design, follow these steps.

1. Select the net pins, pinwires, local lines, long lines, route segments, and unused components pins.
2. Select **Tools** → **Route** → **Manual Route**.

   The selected objects are routed in the specified order.

Notes on Manual Routing

This section includes additional information on manually routing your design.

- Selected objects must be part of the same net. For example, you cannot select a net pin that is part of one net and a long line that is part of another net.

- If a connection does not exist between specified objects that connection is not routed, and an error message appears in the history area. If enhanced routing is enabled, the FPGA Editor attempts to autoroute between the two selected routing resources. Enhanced routing is described in the "Main Window Properties" section.
- When you specify objects to route, consider the direction of current flow through the switches connecting the two objects. You can route from source to load or from load to source, but you cannot mix the two directions during a single Route command run.
- When you select an unused net pin or pinwire for a connection, it is added to the net you are routing.
- Manual routing only routes the specified connections. All other unrouted connections on the applicable net remain unrouted, unless enhanced routing is enabled.
- The Stub Trimming option displays only those portions of routing resources, for example, long lines and local lines, actually used by routes. If you disable Stub Trimming, the full routing resources taken up by the routes are displayed. For manual routing, disable Stub Trimming to determine which routing resources are available. Stub Trimming is described in the "Main Window Properties" section.
- Partially routed nets that do not terminate at pins (antennas) are unrouted by the Autoroute –all command if you do not lock the net. Unlocked antennas are also removed if you run PAR on your design file.
- Any segment added to a net with manual routing is locked or unlocked, depending on the net's lock status.
- You may want to specify Auto Highlight if you are manually routing a very dense design.
- You must select objects in the order in which you want them routed. When you select the objects, consider that connections are routed one by one from each selected object to the next. For example, if you select three objects in the order A, B, C, you are indicating that you want to route A to B, then route B to C.

Switch Boxes in Manual Routing

Switch boxes are located at the junctions of horizontal and vertical local lines and can connect local lines. The switch boxes have certain allowable matrices for pin connections. Allowable routes vary, depending on the location of the switch box on the chip. For example, switch boxes on the perimeter of the chip have fewer pins, so the routing matrices are different from those on switch boxes inside the perimeter.

To see the allowable paths for any pin in a given switch box, select the pin. To deselect the pin and clear the paths from your screen, click in an empty part of the screen. Click the Shift key and the left mouse button to select multiple switch box pins.

To route a connection through a switch box, select the local lines leading to the pins you want to connect. A “bank shot” is a way of indirectly connecting two switch box pins that cannot be connected directly. If you want to route a bank shot through a switch box, select in the correct order the local lines leading to all of the pins you want to connect.

Routing Through a Logic Block

A type of route called a route-through can pass through an occupied or an unoccupied CLB site. A route-through provides routing resources that would otherwise be unavailable.

Use Ctrl+Shift+left mouse button on a pin to highlight all available route-through paths for the pin at that site or component.

You can manually perform a route-through as shown in the following steps for a a CLB in an XC4000 design.

1. During manual routing, select input pin C1, C2, C3, or C4 on the CLB site (vacant or occupied) you want to route through.

   You can also select the pinwire associated with the pin.

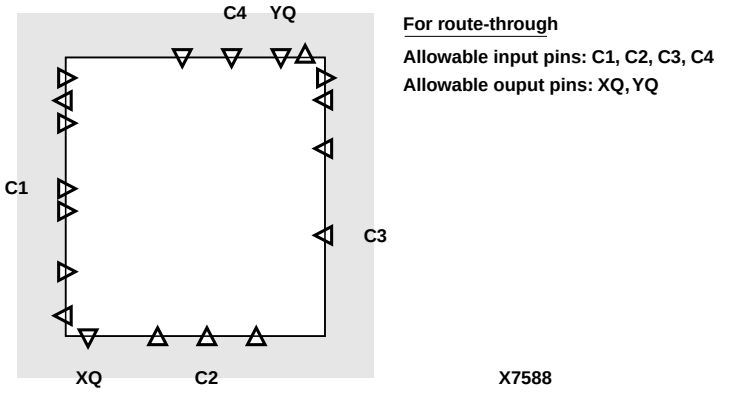


Figure 3-7 CLB Pins for Route-Throughs in XC4000/4000E Designs

2. Select output pin XQ or YQ on the same site.

   You can also select the pinwire associated with the pin.

3. Select **`Tools`** → **`Route`** → **`Manual Route`**.

   The net is routed through the site or component.

   An error message appears if the route-through is not possible because of interfering logic in the CLB or pre-existing signals on the route-through pins.

In the FPGA Editor, a route-through appears as a wide line connecting an input to an output pin. The line has the same width and color as other route line segments and is contained in the route graphics layer. If a component occupies the route-through site, the route-through line segment is displayed on top of the component.

Automatic Routing Option

The Automatic Routing option automatically routes any unrouted nets created as a result of an editing action, such as placing a component, creating a new net, or swapping components. If enabled, Automatic Routing is performed after each Add, Copy, Swap, Autoplace, and Place command.

The Automatic Routing option is included in the main window property sheet, and the default setting is enabled. You can change the

default setting by editing your fpga_editor.ini or fpga_editor_user.ini file. See the “Initializing the FPGA Editor” section of the “Customizing the FPGA Editor” chapter.

During an editing session, you can toggle the option between enabled and disabled with the following procedure.

1. S elect **File** → **Main Properties** to display the Main Properties property sheet.
2. Select **Automatic Routing**.
3. Click **OK** or **Apply**.

Unrouting

Unrouting disconnects routed connections for specified objects. The logical connections remain after the unroute. The unrouted routes are replaced with ratsnest lines. You can unroute selected objects or unroute your entire design.

Note: Locked nets cannot be unrouted.

You can unroute the following objects.

- Nets
- Net Pins
- Route Segments
- Macros
- Used local lines, long lines, and pinwires

Unrouting Selected Objects

To unroute selected objects, follow this procedure.

1. Select the objects to unroute.

   Select any combination of components, nets, net pins, route segments, macros, and used wires in the Array window. Nets and macros are selected by displaying a net or macro list in the List window; a net can also be selected by clicking the Shift key and left mouse button on a route segment. A macro can also be selected by pressing the Ctrl key while selecting a macro component.

2. Select **Tools** → **Route** → **Unroute**.

   The objects are unrouted; routed connections are replaced by ratsnest lines.

Unrouting Entire Design

1. Select **Tools** → **Route** → **Unroute All**.
2. Select **Yes** in the confirmation box that appears to unroute all nets.

   All routed connections in your design are unrouted except the locked signals and certain macro nets. See the "Routing and Unrouting Macros in Your Design" section of the "Working with Physical Macros" chapter.

Unrouting Notes

This section includes additional information on unrouting your design.

- When you unroute a net pin, only the connection to the net pin is unrouted. All other routed connections on the net are retained.
- When you unroute a net, the entire net is unrouted.
- When you unroute a component, each net pin on the component is unrouted.

Constraints

You can add certain constraints to or delete certain constraints from the .pcf file in the FPGA Editor. In the FPGA Editor, net, site, and component constraints are supported as property fields in the individual nets and components. Properties are set with the Setattr command and are read with the Getattr command. All Boolean constraints (block, locate, lock, offset, and prohibit) have values of On or Off; offset direction has a value of either In or Out; and offset order has a value of either Before or After. All other constraints have a numeric value and can also be set to Off to delete the constraint. All values are case-insensitive (for example, "On" and "on" are both accepted).

When you create a constraint in the FPGA Editor, the constraint is written to the PCF file whenever you save your design. When you

use the FPGA Editor to delete a constraint and then save your design file, the line on which the constraint appears in the PCF file remains in the file but it is automatically commented out.

Some of the constraints supported in the FPGA Editor are listed in the following table.

Table 3-4 Constraints

Constraint	Accessed Through
block paths	Component Properties and Path Properties property sheet
define path	Created, edited, and removed with Add and Delete; viewed with Path Properties property sheet
location range	Component Properties Constraints page
locate macro	Macro Properties Constraints page
lock placement	Component Properties Constraints page
lock macro	Macro Properties Constraints page
lock routing of this net	Net Properties Constraints page
lock placement	Component Properties Constraints page
lock routing	Net Properties Constraints page
maxdelay allnets	Main Properties Constraints page
maxdelay allpaths	Main Properties Constraints page
maxdelay net	Net Properties Constraints page
maxdelay path	Path Properties property sheet
maxskew	Main Properties Constraints page
maxskew net	Net Properties Constraints page
offset comp	Component Properties Offset page
penalize tilde	Main Properties Constraints page
period	Main Properties Constraints page
period net	Net Properties Constraints page
prioritize net	Net Properties Constraints page
prohibit site	Site Properties property sheet

All constraints properties can also be set with property sheets. Properties and corresponding constraints are listed in the following tables.

Main Properties	Constraint
penalize_tilde	penalize tilde
allnets_maxdelay	maxdelay allnets
allpaths_maxdelay	maxdelay allpaths
clknets_period	period
clknets_maxskew	maxskew

Component Properties	Constraint
lock	lock comp
locate	locate comp
offset	offset comp
offset_comp1	Argument to offset comp
offset_comp2	Argument to offset comp
offset_order	Argument to offset comp
offset_direction	Argument to offset comp
offset_time	Argument to offset comp
block	block comp

Net Properties	Constraint
lock	lock net
block	block net
prioritize	prioritize net
maxdelay	maxdelay net
maxskew	maxskew net
period	period net

Macro Properties	Constraint
locate	locate macro
lock	lock macro

Path Properties	Constraint
block	block path
maxdelay	maxdelay path

Site Properties	Constraint
prohibit	prohibit site

Locked Nets and Components

If a net is locked, you cannot unroute any portion of the net, including the entire net, a net segment, a pin, or a wire. To unroute the net, you must first unlock it. You can add pins or routing to a locked net.

A net is displayed as locked in the FPGA Editor if the Lock Net [*net_name*] constraint is enabled in the PCF file. You can use the Net Properties property sheet to remove the lock constraint.

When a component is locked, one of the following constraints is set in the PCF file.

- `lock comp` [*comp_name*]
- `locate comp` [*comp_name*]
- `lock macro` [*macro_name*]
- `lock placement`

If a component is locked, you cannot unplace it, but you can unroute it. To unplace the component, you must first unlock it.

Adding Probes to Your Design

You can add probes to your design to examine the signal states of the targeted FPGA device, as described in the following procedure.

Adding a Probe

1. Select **Tools** → **Probes** to display the Probes dialog box, as shown in the "Probes Dialog Box" figure of the "Menu Commands" chapter.
2. Select **Add** to display the dialog box shown in the "Define Probe Dialog Box" figure of the "Menu Commands" chapter.
3. Fill in the fields in this dialog box to define the probe. See the "Define Probe Dialog Box Options" section of the "Menu Commands" chapter for the definitions of the fields
4. Select **OK** to close the dialog box.

   The probe is automatically routed, and the defined probe is displayed in the Probes dialog box.
5. Select the BitGen option in the Probes dialog box to display the dialog box shown in the "Run BitGen Dialog Box" figure of the "Menu Commands" chapter.
6. The file name displayed in the Bit File Name field is the name of your probed design. If you change the name to *design_name*.bit, you are warned that this name represents your unprobed design. You can select **Yes** to save the bit file under this name or **No** to save the bit file under the name provided by the system.
7. Click **OK** to return to the Probes dialog box.
8. Select **Download** to start the Hardware Debugger tool so you can download your bit file to a test device. This tool is run in a separate process from the FPGA Editor.

Verifying Your Design

You can use the following FPGA Editor tools to verify your designs.

- Physical Design Rule Check (DRC)
- Delay Calculator

This section contains the following topics.

- "Physical Design Rule Check (DRC)"
- "Delay Calculator"
- "TRACE"

Physical Design Rule Check (DRC)

Physical Design Rule Check (DRC) is a series of tests to find logical and physical errors in your design. Physical DRC is applied to the FPGA Editor and BitGen. In addition to running in the FPGA Editor, the DRC runs during these conditions.

- You select the Run DRC toolbar icon in the Block window
- During manual routing
- Whenever you add pins to a net

The DRC runs in the background. Results of the DRC are written into the history area. DRC error messages indicate faulty or incomplete routing or component logic.

DRC runs can produce a large number of messages. Because the history area can only contain a limited number of characters, you may not be able to scroll to messages at the beginning of a DRC run or to messages from previous runs. If you want to view them, use a text editor to view the contents of the log file (*design_name*.out) for your session. See the "Recovering a Terminated FPGA Editor Session" section. When you exit the FPGA Editor, the log file is renamed *design_name*_fpga_editor_*YYMMDD_HHMMSS*.log, where Y is year, M is month, D is day, H is hour, M is minute, and S is second.

Note: When you run the DRC on selected objects, the objects are deselected if the Automatic Deselect Option main window property is turned On. If the option is turned Off, the objects remain selected after the DRC runs.

The DRC tests performed follow these rules.

- If you select one or any combination of net names, routes, or net pins, the Net Check is performed.
- If you select one or more components, the Block Check is performed.
- If you select objects that combine the first and second types, both Net Check and Block Check are performed.

Running a DRC

To run a DRC, follow these steps.

1. Select the design objects for the DRC run.

   Select any combination of components, net pins, route segments, or nets. To check all objects, do not select any objects.

2. Select **Tools** → **DRC** → **Setup** to display the DRC dialog box, as shown in the "DRC Dialog Box" figure of the "Menu Commands" chapter.

3. Select the corresponding button to perform a Net Check, Block Check, Chip Check, or All Checks

   You can select only one.

4. Select the corresponding button to perform the DRC on **All Objects** in your design or only on **Selected Objects**.

5. Select **All Messages** for all DRC messages, errors and warnings or **Error Messages**.

6. Click **Apply** or **OK**.

   The DRC tests are performed on the specified objects.

Delay Calculator

Delay is the time that it takes to propagate a signal from a driver pin to a load pin. If not otherwise indicated, delay values are given in nanoseconds (ns). The Delay Calculator tool calculates and displays the delay associated with load and driver pins in a given net or path.

Calculating Net Delay

You can either find the delay for all pins in the net or for specific pins.

To find the delay for all pins in a net, follow these steps.

1. Select a net name from the List window.

2. Select **Delay** in the User toolbar.

   If the net is fully or partially routed, a list of pins appears in the history area, along with their associated delays. If the net is unrouted, each pin is listed as "unrouted."

3. Select **Attrib** in the User toolbar to display the Net Properties property sheet.

4. Select the Pins page to display the delays for associated pins.

If a blank space appears next to a pin name, either in the pin list or in the history area, the pin is the net driver that has no delay or the pin is unrouted. A tilde (~) appearing with a delay, indicates that the value shown is an approximate.

Note: When you display delays for all of the pins in a net, the net is deselected if the Automatic Deselect Option in the Main Properties property sheet is turned On.

To display the delays for selected pins in a net, use the mouse to select the specific pins. If the net is fully or partially routed, the delays for the selected pins are automatically displayed in the history area. If the net is unrouted, no delays are displayed.

Calculating Path Delay

To display the delay between two pins in a path follow these steps.

1. Select the two pins with the mouse.
2. Select **Delay** in the User toolbar.

   The path delay between the two pins is displayed in the history area. If there are multiple paths between the two pins, the path with the maximum delay appears. If Auto Highlight is enabled, the path between the pins is highlighted.

TRACE

You can run TRACE (Timing Reporter and Circuit Evaluator) in the FPGA Editor to visualize timing errors and to make modifications without going back and forth between the FPGA Editor and TRACE.

Functions performed by TRACE in the FPGA Editor are the same as those outside of the FPGA Editor with a few exceptions, as noted in this section.

TRACE functionality within the FPGA Editor includes the following.

- Specify error or verbose report types
- Limit the number of errors reported per constraint in the timing error and verbose reports. The summary report is not supported in the FPGA Editor

Input and Output Files

- Input to TRACE is your currently loaded design file and the constraint file
- Output is sent to the history area, unless you specify otherwise, and to the OUT (log) file instead of to a timing report (TWR) file.

Running TRACE from the Tools Menu

To run TRACE from the Tools menu follow these steps.

1. Select **Tools** → **Trace** → **Setup and Run** to display the dialog box shown in the "Trace Dialog Box" figure of the "Menu Commands" chapter.
2. Make your entries in the TRACE dialog box as described in the "Trace Dialog Box Options" section of the "Menu Commands" chapter.
3. Click **OK** or **Apply**.

   TRACE runs timing analysis, and the Trace Summary dialog box appears, as shown in the "Trace Summary Dialog Box" figure of the "Menu Commands" chapter. This dialog box lists information on any constraints that failed to meet timing, as described in the "Trace Summary Dialog Box Options" section of the "Menu Commands" chapter.
4. For additional timing information on any of the constraints listed in the Summary dialog box, click on the listed constraint. The TRACE Errors dialog box appears, as shown in the following figure.

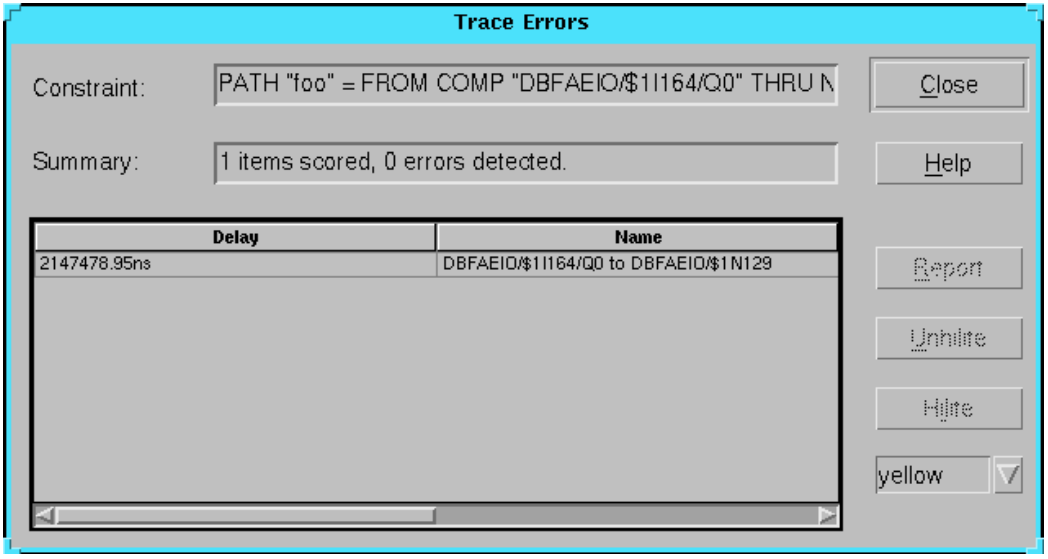


Figure 3-8 TRACE Errors Dialog Box

This dialog box contains the following fields.

- Constraint

  Displays the constraint. You cannot modify this field.

- Summary

  Displays a one-line summary of the constraint. You cannot modify this field.

- Delay / Name

  Delay specifies the delay of the selected path in nanoseconds. Name specifies the start and end point for the path.

- Report

  Outputs the detailed TRACE report for the selected path to the history area and to the OUT (log) file.

- Unhilite

  Unhighlights the selected path in the FPGA Editor window.

- Hilite

  Highlights the selected path, using the specified color.

Chapter 4

Menu Commands

This chapter lists and describes all the commands available in the menus of the FPGA Editor. This chapter contains these main sections.

- “Menus”
- “Commands”
- “Toolbars”
- “Keyboard Shortcuts”

Menus

The FPGA Editor has six menus, which are described in the following sections. If you do not have a design open in the Array window, only the File, View, Tools, and Help menus are available.

File Menu

Use the commands in the File menu to open, close, save, and create designs and macros. This menu also includes the print command for printing your designs and macros, as well as a command to open the property sheet for the main window. The following commands are available in this menu.

New	Creates a new design or macro
Open	Opens existing design or macro
Close	Closes current design or macro
Save	Saves current design or macro
Save As	Saves current design or macro to a different file name
Save As Macro	Saves current design as a macro

Print	Prints the design or macro file
Print Preview	Displays a preview of how the current design or macro will be printed
Print Setup	Changes the printer and printing options
1,2,3,4	Displays up to four of the most recently accessed designs
Main Properties	Shows the property sheet for the program and design
Exit	Quits the FPGA Editor

Edit Menu

Use the Edit menu commands to modify the configuration of your design in the FPGA Editor window, and to display and modify attributes for design objects. The Edit menu includes the following commands.

Cut	Deletes the selected design object(s)
Unselect All	Unselects all selected items
Properties of Selected Items	Shows the property sheets for the selected items
Add	Adds components, pins, or nets
Add Macro	Adds a macro instance to design
Add Macro External Pin	Designates a selected component pin in the macro file as an external pin
Set Macro Reference Comp	Designates a selected component in the macro file as the macro's reference component
Swap	Swaps the selected components or component and site
Unbind Macro	Unbinds the selected macro into individual components
Find	Finds components, nets, wires, macros, sites, and pins.

View Menu

Use the commands in the View menu to change what is displayed in the FPGA Editor window. The View menu includes the following commands.

Toolbars → Command	Shows or hides the command line toolbar
Toolbars → History	Shows or hides the history toolbar
Toolbars → Layer	Shows or hides the layer view toolbar
Toolbars → Standard	Shows or hides the standard toolbar
Toolbars → User	Shows or hides the user button toolbar
Toolbars → Default Layout	Shows all toolbars in their default locations
Status Bar	Shows or hides the status bar
Zoom In	Zooms in one level in the Array or Block window
Zoom Out	Zooms out one level in the Array or Block window
Zoom Selection	Adjusts the scale of the current view so that the selected objects can be seen in the Array window
Full View	Displays the entire device in the Array or Block window
Detailed View	Displays the device at the highest zoom setting in the Array or Block window
Pan Left	Scrolls the current window to the left in the Array or Block window
Pan Right	Scrolls the current window to the right in the Array or Block window
Pan Up	Scrolls the current window up in the Array or Block window
Pan Down	Scrolls the current window down in the Array or Block window
Highlight	Adds the selected items to the highlight layer in the Array window

Unhighlight	Removes the selected items from the highlight layer
Unhighlight All	Clears the highlight layer
Refresh	Redraws all the windows

Tools Menu

Use the commands in the Tools menu to place and route your design; run a design rule check; display net delays; run the TRACE program; add probes to your design; and create and run command scripts. The Tools menu includes the following commands.

Place → Auto Place	Automatically places selected unplaced components
Place → Manual Place	Allows you to manually place the selected components
Place → Unplace	Unplaces the selected components
Place → Auto Place All	Starts the autoplacement tool on all unplaced components
Place → Unplace All	Unplaces all components
Route → Auto Route	Automatically routes selected objects
Route → Manual Route	Routes selected objects using the specified routing resources
Route → Unroute	Unroutes all selected unlocked nets or portions of nets
Route → Auto Route All	Automatically routes all objects
Route → Unroute All	Unroutes all nets in the design except locked nets
DRC → Setup	Sets options for running DRC
DRC → Run	Runs DRC on selected objects or the entire design if nothing is selected
Delay	Displays net delays using FPGA Editor's Delay Calculator for selected components pins or nets.

Trace → Setup and Run	Sets options for running TRACE; runs TRACE on all constraints, then displays the TRACE summary information
Trace → Summary	Lists information on results of the TRACE run
Probes	Adds probes to design
Scripts → Begin Recording	Begins recording a script
Scripts → End Recording	Ends recording a script
Scripts → Playback	Allows you to select and play back a script

Window Menu

Use the commands in the Window menu to open additional windows, and to control the placement of the windows on your screen. The Window menu includes the following commands.

New → Array Window	Opens another instance of the Array window
New → Block Window	Opens a block window for the selected component or site
New → List Window	Opens another instance of the list window
New → World Window	Opens another instance of the world window
Arrange Windows → Cascade	Arranges the windows so they overlap
Arrange Windows → Tile Horizontally	Arranges the windows as non-overlapping tiles horizontally
Arrange Windows → Tile Vertically	Arranges the windows as non-overlapping tiles vertically
Arrange Windows → Default Layout	Arranges the windows using the default layout
Arrange Property Sheets → Cascade Vertically	Arranges the property sheets so they overlap vertically

Arrange Property Sheets → Cascade Horizontally	Arranges the property sheets so they overlap horizontally
Arrange Property Sheets → Cascade Diagonally	Arranges the property sheets so they overlap diagonally
Close Window	Closes the currently active window
Close All Property Sheets	Closes all property sheets

Help Menu

Use the Help menu to access the online help. The Help menu includes the following commands.

Help Topics	Displays help topics
Online Documentation	Opens the software manuals in the default Web browser.
About FPGA Editor	Displays the program information and copyright

Commands

This section describes in alphabetical order all the FPGA Editor menu commands.

1, 2, 3, 4 (File Menu)

The File menu displays up to four of the most recently accessed designs or macros. To open a design or macro, click on the appropriate file listed in the menu.

About FPGA Editor (Help Menu)

The About FPGA Editor command displays a pop-up window that displays the version number of the FPGA Editor software.

Add (Edit Menu)

Use this command to add objects, such as components, pins, or nets to your design.

Add Macro (Edit Menu)

Use this command to add a macro to your design. This command displays the following dialog box.

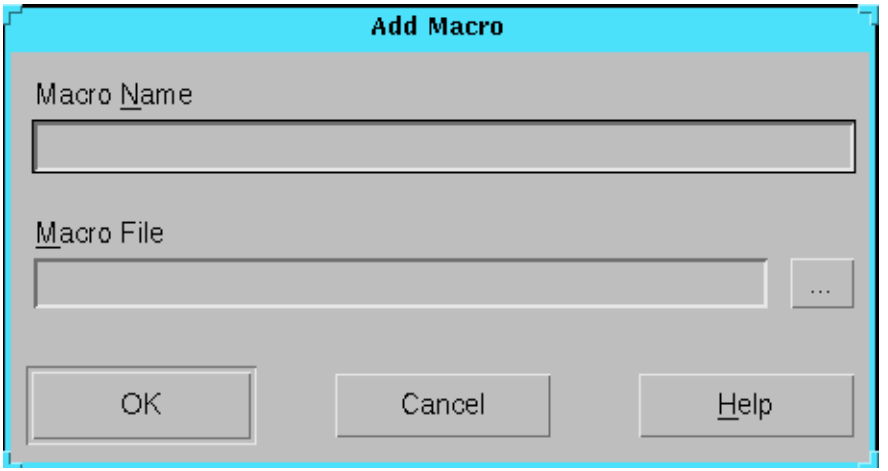


Figure 4-1 Add Macro Dialog Box

Add Macro Dialog Box Options

- Macro Name

  Specifies the name for the macro instance. If you do not enter a name, a name is assigned automatically when the macro is added.

- Macro File

  Specifies the name of the macro library file to add to your design. If you previously added this same macro to the design, the added macro will be a copy of the first instantiation. If you changed the macro library file since the original instantiation, these changes will *not* be reflected in this new instantiation

Add Macro External Pin (Edit Menu)

Use this command to define a selected component pin as a macro external pin. External pins connect the instantiated macro to other components in your design.

Arrange Property Sheets Submenu (Window Menu)

Arrange Property Sheets is a submenu in the Window menu. This submenu contains the following commands that arrange property sheets vertically, horizontally, or diagonally down the screen so that they overlap one another. The active property sheet is on top.

Note: Refer to the alphabetical listings of these commands for an explanation of their functions.

- Cascade Vertically
- Cascade Horizontally
- Cascade Diagonally

Arrange Windows Submenu (Window Menu)

Arrange Windows is a submenu in the Window menu. This submenu contains the following commands that arrange windows either horizontally across the main window, vertically across the main window, or diagonally down the screen so they overlap one another. The active window is on top or first in the selected arrangement.

Note: Refer to the alphabetical listings of these commands for an explanation of their functions.

- Cascade
- Tile Horizontally
- Tile Vertically
- Default Layout

Array Window (Window Menu)

Note: This command appears in the New submenu.

Use this command to open additional Array windows.

Auto Place (Tools Menu)

Note: This command appears in the Place submenu.

Use this command to automatically place selected unplaced components.

Auto Place All (Tools Menu)

Note: This command appears in the Place submenu.

Use this command to automatically place all unplaced components. This command displays the following dialog box.

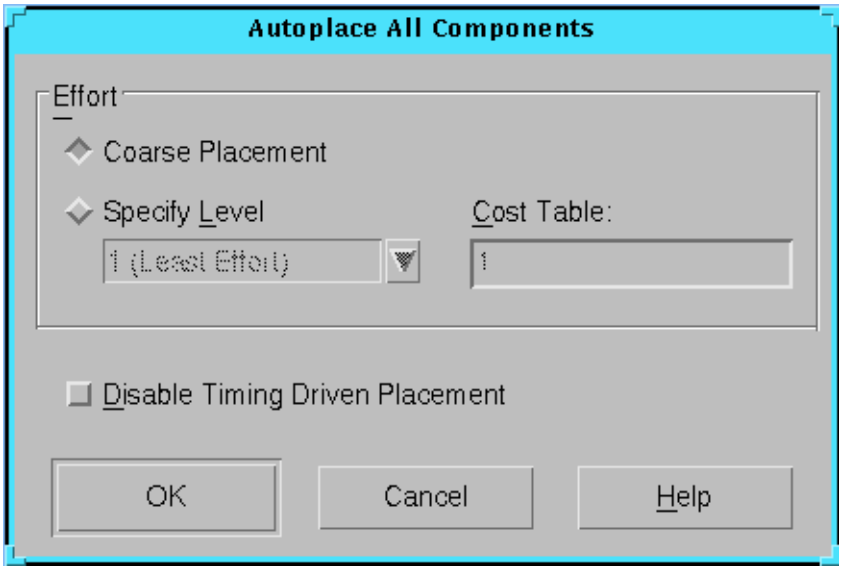


Figure 4-2 Autoplace All Components Dialog Box

Autoplace All Components Dialog Box Options

- Coarse Placement

  Use this option to perform a quick, less than efficient placement. This option places your design much faster than a placement at a selected level, but the results may not be suitable for routing. Select this option to quickly place your design to see how it maps, but you do not use this placement to route your design.

- Specify Level

  Use this option to specify the effort level for the placement of your design. Level ranges from 1 (Least Effort) to 5 (Most Effort) with intermediate ranges 2, 3, and 4.

- Cost Table

Use this option to specify the cost table (1—100) to use for the placement of your design at the specified Level.

- Disable Timing Driven Placement

  This option turns off timing-driven placement.

Auto Route (Tools Menu)

Note: This command appears in the Route submenu.

Use this command to automatically route selected unrouted components.

Auto Route All (Tools Menu)

Note: This command appears in the Route submenu.

Use this command to automatically route all unrouted components. This command displays the following dialog box.

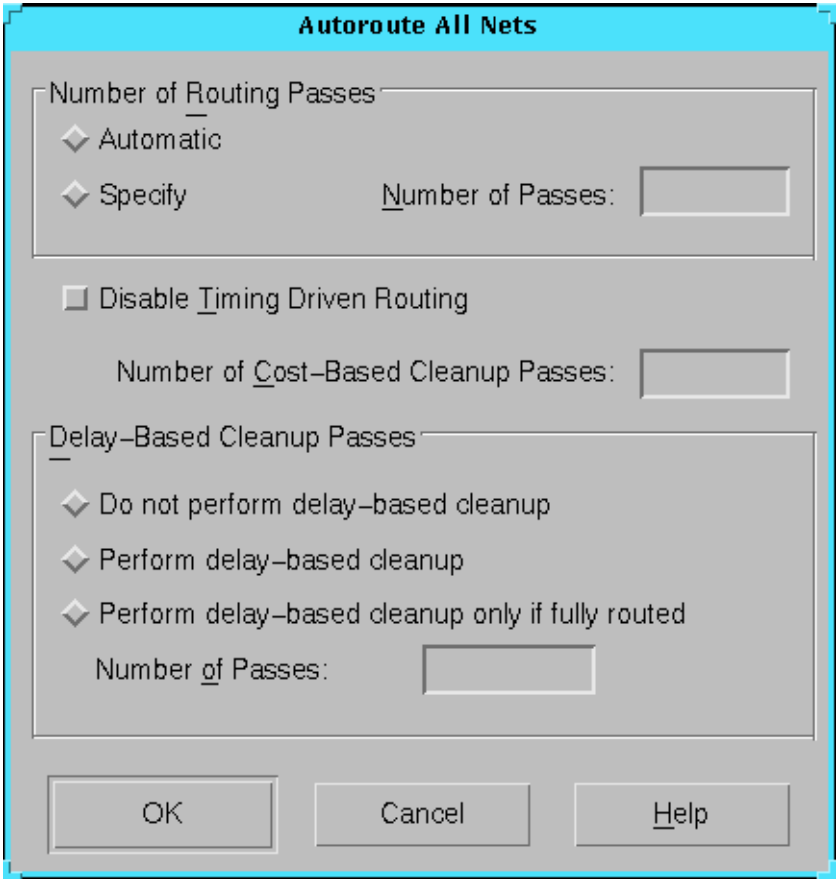


Figure 4-3 Autoroute All Nets Dialog Box

Autoroute All Nets Dialog Box Options

- Automatic/Specify

  Select Automatic to automatically route your design. Select Specify to run the number of routing passes entered in the Number of Passes field.

- Number of Passes

  If Automatic is not selected, sets the number of iterations for the router. Routing stops earlier than the maximum number of iterations if an iteration routes to 100% completion.

- Disable Timing Driven Routing

  This option turns off timing-driven routing.

- Number of Cost-Based Cleanup Passes

  Specifies the number of cost-based clean-up passes to run on your design. In cost-based clean-up passes, the router makes routing decisions by assigning weighted values to the factors affecting delay times between sources and nets, for example, the type of routing used.

- Delay-Based Cleanup Passes

Option	Description
Do not perform delay-based cleanup	Do not run any delay-based clean-up passes
Perform delay-based cleanup	Run delay-based cleanup passes based on the number entered in the Number of Passes field
Perform delay-based cleanup only if fully routed	Run delay-based cleanup passes only if the design is fully routed
Number of Passes	Number of delay-based cleanup passes to run; disabled if the Do not perform delay-based cleanup option is selected

Begin Recording (Tools Menu)

Note: This command appears in the Scripts submenu.

Use this command to record a series of commands into a script file. This command displays the following dialog box.

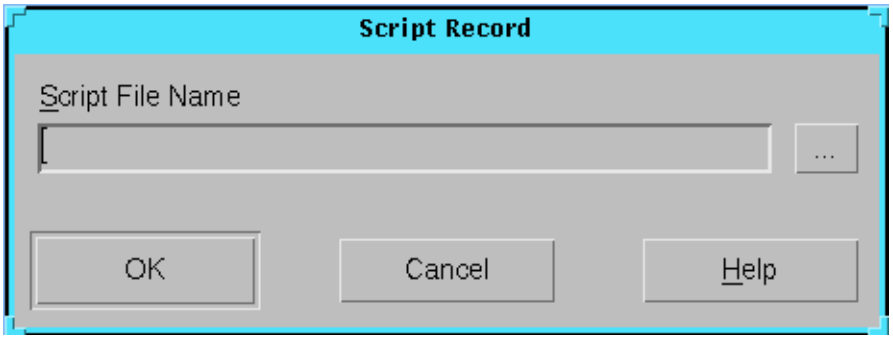


Figure 4-4 Script Record Dialog Box

Script Record Dialog Box Options

Use the Script File Name field to enter the name of the script file you want to use to record the commands, or use the browse button to display the Save As dialog box. Use this dialog box to select the directory structure and file name for your script file.

Block Window (Window Menu)

Note: This command appears in the New submenu.

Use this command to open additional Block windows. The Block window is used to edit logic blocks. You can use only one block window at a time for editing; however, you can have additional block windows open for viewing.

Cascade (Window Menu)

Note: This command appears in the Arrange Windows submenu.

Use this command to arrange the windows diagonally down the screen so that they overlap one another. The active window is on top.

Cascade Diagonally (Window Menu)

Note: This command appears in the Arrange Property Sheets submenu.

Use this command to arrange the property sheets diagonally down the screen so that they overlap one another. The active property sheet is on top.

Cascade Horizontally (Window Menu)

Note: This command appears in the Arrange Property Sheets submenu.

Use this command to arrange the property sheets horizontally across the screen so that they overlap one another. The active property sheet is on top.

Cascade Vertically (Window Menu)

Note: This command appears in the Arrange Property Sheets submenu.

Use this command to arrange the property sheets vertically down the screen so that they overlap one another. The active property sheet is on top.

Close (File Menu)

Use this command to close the active design file.

Close All Property Sheets (Window Menu)

Use this command to close all open property sheets.

Close Window (Window Menu)

Use this command to close the active window.

Command (View Menu)

Note: This command appears in the Toolbars submenu.

Use this command to show or hide the Command Line toolbar.

Cut (Edit Menu)

Use this command to delete components, nets, pins, and paths. The following table describes the results of using the Cut command on various design objects.

Design Object	Results of Cut Command
Component	Net pins are unrouted and removed from nets, and the component is removed from the design database
Net	Net pins on the net are unrouted, each net pin is removed from the design database, and the net is removed from the database
Signal Pin	Pins are unrouted from the associated net, and the pin is removed from the net. A deleted pin does not have a connection (logically or physically) to the net from which it was deleted.
Path	Removes the Define Path constraint that defines the path; also removes all constraints that directly depend on the Define Path constraint, such as, Maxdelay Path
Path Elements	When nets or components are deleted from path definitions, they are not deleted from the design; they are only removed as elements in the path.

Default Layout (View Menu)

Note: This command appears in the Toolbars submenu.

Use this command to display all FPGA Editor toolbars.

Default Layout (Window Menu)

Note: This command appears in the Arrange Windows submenu.

Use this command to arrange the FPGA Editor windows in the default layout pattern.

Delay (Tools Menu)

Use this command to display the delay for selected nets or paths. For pins with multiple paths, the Delay command computes the maximum delay path as the default.

Detailed View (View Menu)

Use this command to zoom in to a selected area in the Array or Block window. If you have more than one array view open at a time, the zoom command applies to the last activated one.

DRC Submenu (Tools Menu)

DRC is a submenu in the Tools menu. Use the commands in this submenu to run a Physical Design Rule Check (DRC) on your design. A DRC is a series of tests run on your design to find logical and physical errors. The following commands are included in the DRC submenu.

Note: Refer to the alphabetical listings of these commands for an explanation of their functions.

- Setup
- Run

End Recording (Tools Menu)

Note: This command appears in the Scripts submenu.

Use this command to end a script file recording session.

Exit (File Menu)

Use this command to exit the FPGA Editor. If you have unsaved changes to your design, you are prompted as shown in the following figure.

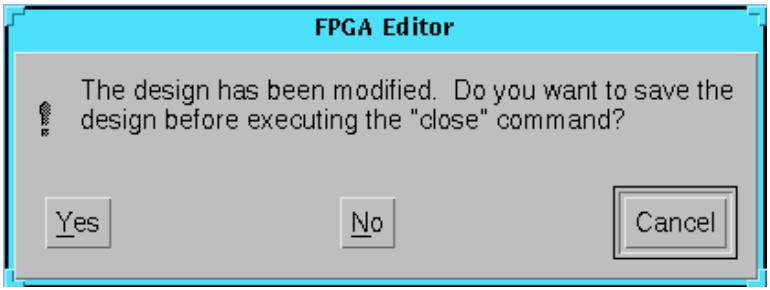


Figure 4-5 Exit Dialog Box

Find (Edit Menu)

Use this command to locate a specific object in your design. This command displays the following dialog box.

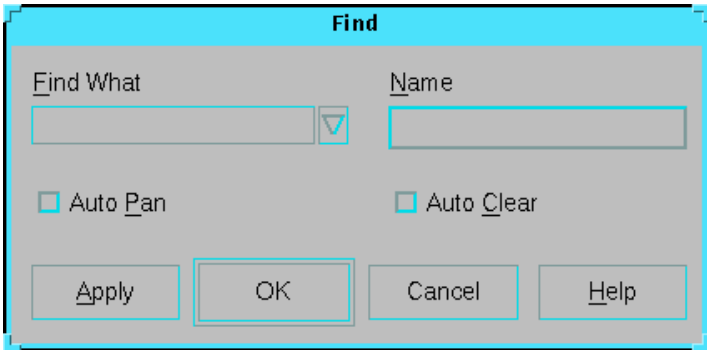


Figure 4-6 Find Dialog Box

Find Dialog Box Options

- Find What

  Specifies the type of object you are searching for in your design. Select the type of object from the list box.

- Name

  Specifies the name of the component, net, site, wire, pin, or macro that you are searching for in your design. You can use wildcards (“*” or “?”) in this field.

- Auto Pan

If you are zoomed in when you select Find, this option automatically pans to the search object. Otherwise, the object will only be selected.

- Auto Clear

  Clears all previous selections; only the item being searched for is selected.

Full View (View Menu)

Use this command to display your entire design in the Array window, or the entire component in the Block window.

Help Topics (Help Menu)

Use this command to display the opening screen of the FPGA Editor Help. From the opening screen, you can jump to step-by-step instructions for using the FPGA Editor and to various types of reference information. After you open help, you can click the Help Topics button in the Help window whenever you want to return to the opening screen of Help.

Highlight (View Menu)

Use this command to add the selected objects to the highlight layer using the default highlight color. See the "Hilite" section of the "Command Line Syntax" chapter for more information.

History (View Menu)

Note: This command appears in the Toolbars submenu.

Use this command to show or hide the History toolbar.

Layer (View Menu)

Note: This command appears in the Toolbars submenu.

Use this command to show or hide the Layer Visibility toolbar.

List Window (Window Menu)

Note: This command appears in the New submenu.

Use this command to open additional List windows.

Main Properties (File Menu)

Use this command to view or change properties for the main FPGA Editor window. This command displays the following property sheet.

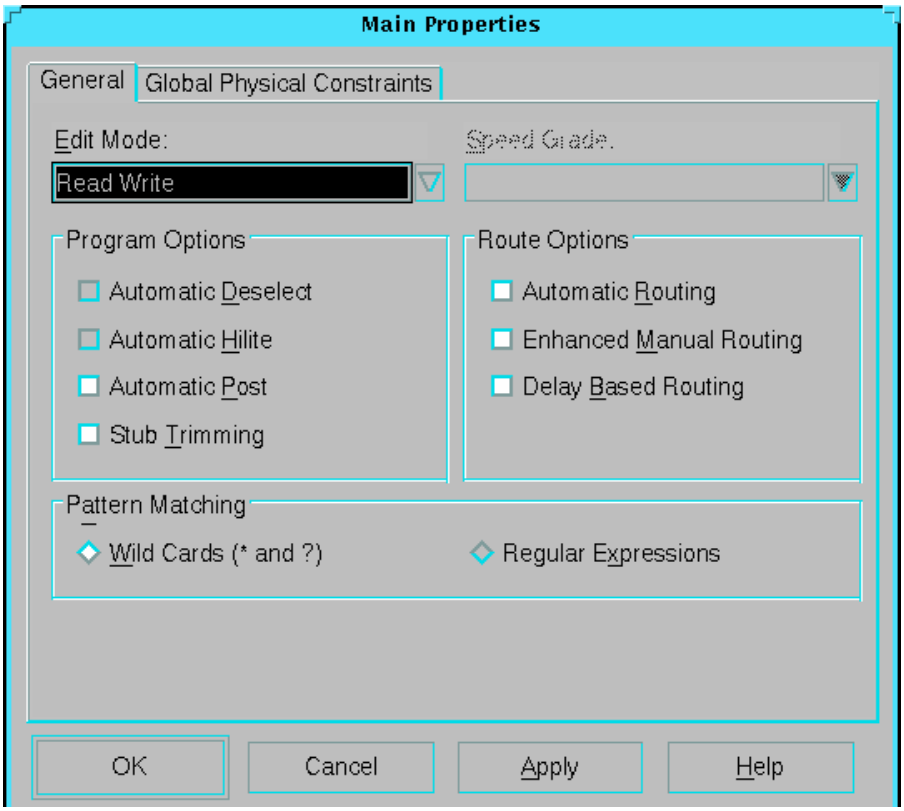


Figure 4-7 Main Properties Property Sheet

This property sheet contains the General page and the Global Physical Constraints page.

General Page Options

Refer to the following table for a description of the General page options.

Table 4-1 Main Properties General Page Options

Option	Description
Edit Mode	Specifies what modifications can be made to your design. You can select Read Only, No Logic Changes, or Read Write.
Program Options	
Speed Grade	Determines the speed (toggle rate) of the part you are editing. You can select an appropriate speed from the list box.
Automatic Deselect	When enabled, selected objects are deselected after a Delay, DRC, EditBlock, Hilite, Setattr, Getattr, or Post Attr command is performed. When disabled, selected objects remain selected after one of these commands is performed. The default is enabled.
Automatic Hilite	When enabled, delay paths are automatically highlighted after a Delay command, and the net being edited is highlighted after manual routing. By default, the option is disabled.
Automatic Post	When enabled, a component, net, path, macro, or external pin properties dialog box is automatically displayed after an Add command, or after a route or autoroute operation in which a new net is created. By default, this option is enabled.
Stub Trimming	When enabled, only the portion of a routing resource that lies directly on the path between two routed pins is displayed in the Array window (for example, a portion of a long line or a pinwire). When disabled, the entire routing resource taken up by the route, such as an entire long line, is displayed in the Array window. The default is enabled.
Route Options	
Automatic Routing	When enabled, the system automatically routes any unrouted nets created as a result of an editing action, such as placing components, creating new nets, swapping components. The default is enabled.

Table 4-1 Main Properties General Page Options

Option	Description
Enhanced Manual Routing	When enabled, the Route command attempts to make a connection between user-specified resources. If the connection fails, it autoroutes between those resources. When disabled, no call to the autorouter occurs. By default, the option is enabled.
Delay Based Routing	When enabled, the autorouter takes delay values into account. When disabled, cost-based autorouting is done. Delay-based autorouting takes longer, but can result in better results, especially in a dense design. By default, the option is enabled. This option has no effect on the Autoroute All operation.
Pattern Matching	
Wild Cards (* and ?)	In the Find dialog, and with commands that accept patterns (such as Select and Unselect), you can use the wildcard characters, * and ?, The asterisk (*) represents any string of zero or more characters. The question mark (?) indicates a single character.
Regular Expressions	Pattern is a grep-like regular expression.

Global Physical Constraints Page Options

Refer to the following table for a description of the Global Physical Constraints page options.

Table 4-2 Main Properties Global Physical Constraints Page Options

Option	Description
Route Locking	Applies a lock routing constraint to all partially or fully routed nets in your design. The lock routing constraint specifies that the current routing cannot be changed or unrouted.
Delays	Applies a Penalize Tilde constraint to your design. This constraint penalizes those delays that are reported as only approximate, signified with a tilde (~) in delay reports by the percentage specified in this field.

Table 4-2 Main Properties Global Physical Constraints Page Options

Option	Description
Max Delay for All Paths	Applies a Maxdelay Allpaths constraint to your design. This constraint specifies the maximum delay for all paths in the design.
Max Delay for All Nets	Applies a Maxdelay Allnets constraint to your design. This constraint specifies the maximum delay for all nets in the design.
All Clock Nets	
Period (ns)	Applies a period constraint to your design, which specifies the clock period for all clock nets in the design. Either a Period or a Frequency should be entered in this dialog box, but not both.
First Pulse	Specifies whether the first pulse of the duty cycle is High or Low.
Duration (ns)	Specifies the duration of the first pulse of the duty cycle.
Tsid	Assigns a timing period or frequency to a timing specification.
Phase (ns)	Phase and factor are used to generate a derived clock based on the period of an existing timing constraint. This constraint is the master and the derived constraint is the slave. Phase is the delay of the initial edge of the master to the slave.
Factor	Phase and factor are used to generate a derived clock based on the period of an existing timing constraint. This constraint is the master and the derived constraint is the slave. Factor is a multiplier period of the master used to create a relative one for the slave. For example, if the period for the slave is one half that of the master, use a value of 0.5.
Max Skew	Applies a Maxskew constraint to your design, which specifies the maximum allowable clock skew for all clock nets in the design.

Manual Place (Tools Menu)

Note: This command appears in the Place submenu.

Use this command to place a component in a selected site.

Manual Route (Tools Menu)

Note: This command appears in the Route submenu.

Use this command to route selected objects using the specified routing resources

New (File Menu)

Use this command to create a new design or macro. This command displays the following dialog box.

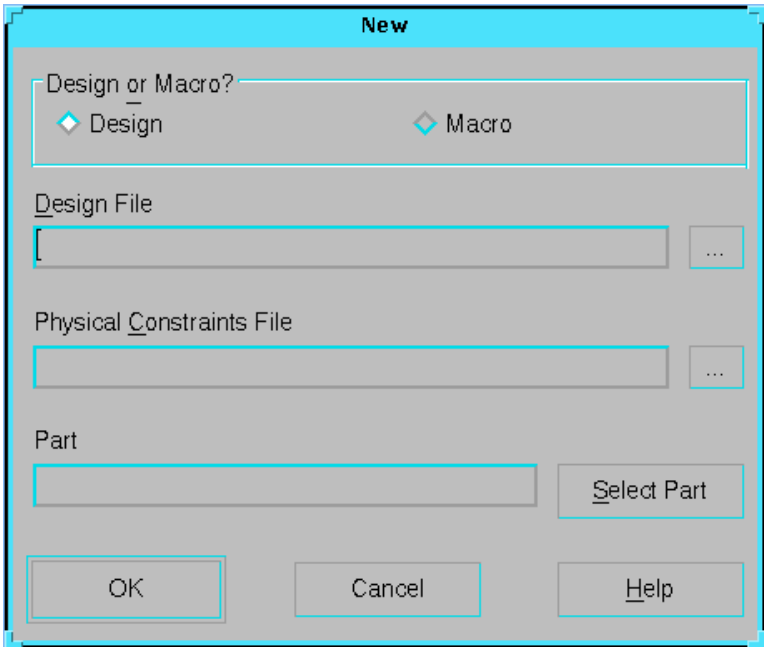


Figure 4-8 New Dialog Box

New Dialog Box Options

- Design or Macro?

  Specifies whether you want to create a new design or a new macro. If you select Macro, the Design File field is replaced with

the Macro File field, and the Physical Constraints File field is grayed out.

- Design File / Macro File

  Specifies the name of the design file or macro file you want to create. You can either enter the file name or click the browse button to display the Save As dialog box. Use this dialog box to select the directory structure and file name for your new design.

- Physical Constraints File (PCF)

  Specifies the name of the physical contraints file for your design. You can either enter the file name or click the browse button to display the Save As dialog box. Use this dialog box to select the directory structure and file name for your constraints file.

- Part

  Click the Select Part button to display the Part Selector dialog box. Use the list boxes in this dialog box to select the family, device, package, and speed grade.

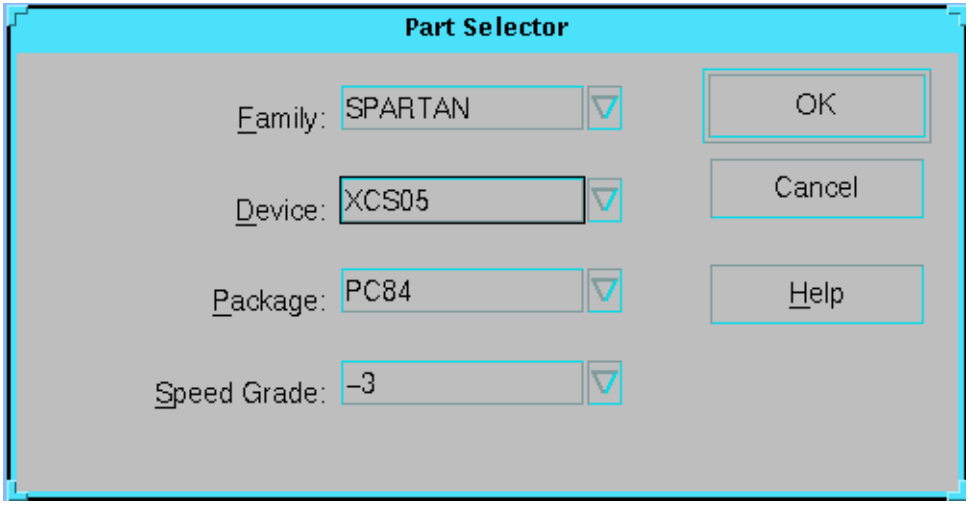


Figure 4-9 Part Selector Dialog Box

Part Selector Dialog Box Options

- Family

Specifies the architecture (product family) of your design, for example, XC4000E or Virtex.

- Device

  Specifies a device within the selected architecture, for example, 4036EX or 4028EX.

- Package

  Specifies a package within the selected architecture and device; for example, PC84 or PQ100.

Note: You can only enter a device and package from a part library that is installed on your system. For example, if you have not installed the Xilinx 4036 series part library, you cannot create a design using the 4036 device and the package.

- Speed

  Specifies the speed grade of the selected part. Allowable speeds are listed in *The Programmable Logic Data Book*.

New Submenu (Window Menu)

New is a submenu in the Window menu. Use the commands in this submenu to open additional Array, Block, List, and World windows. The following commands are included in the New submenu.

Note: Refer to the alphabetical listings of these commands for an explanation of their functions.

- Array Window
- Block Window
- List Window
- World Window

Online Documentation (Help Menu)

Use this command to open the software manuals in the default Web browser.

Open (File Menu)

Use this command to open an existing design or macro. This command displays the following dialog box.

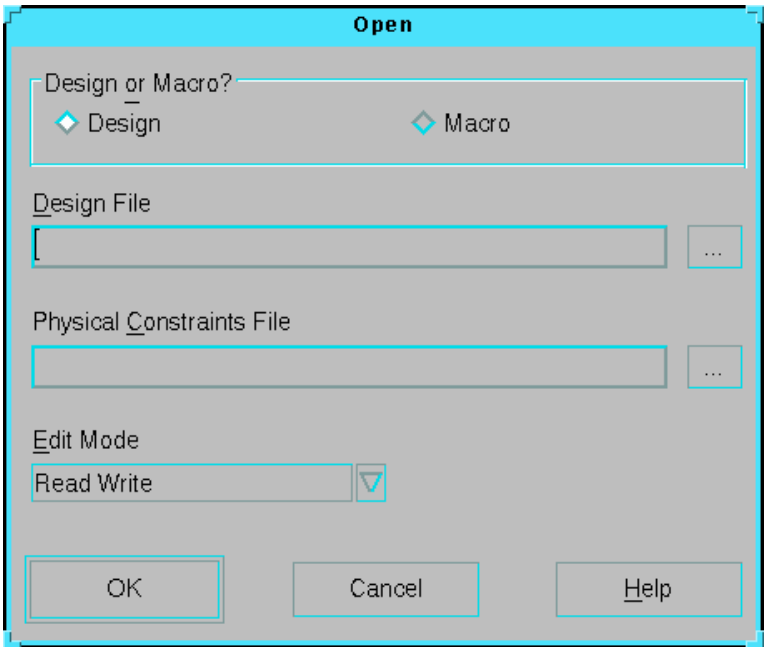


Figure 4-10 Open Dialog Box

Open Dialog Box Options

- Design or Macro?

  Specifies whether you want to open a design or a macro file. If you select Macro, the Design File field is replaced with the Macro File field, and the Physical Constraints File field is grayed out.

- Design File / Macro File

  Specifies the name of the design file or macro file you want to open. You can either enter the file name or click the browse button to navigate through the directories to find the design you want to open.

- Physical Constraints File (PCF)

Specifies the name of the physical contraints file for your design. You can either enter the file name or click the browse button to find the PCF for your design.

- Edit Mode

  Specifies what modifications can be made to your design. You can select Read Only, No Logic Changes, or Read Write.

Pan Left (View Menu)

Use this command to scroll the active Array or Block window to the left.

Pan Right (View Menu)

Use this command to scroll the active Array or Block window to the right.

Pan Up (View Menu)

Use this command to scroll the active Array or Block window up.

Pan Down (View Menu)

Use this command to scroll the active Array or Block window down.

Place Submenu (Tools Menu)

Place is a submenu in the Tools menu. Use the commands in this submenu to automatically or manually place some or all components, or to unplace some or all components. The following commands are included in the Place submenu.

Note: Refer to the alphabetical listings of these commands for an explanation of their functions.

- Auto Place
- Manual Place
- Unplace
- Auto Place All
- Unplace All

Playback (Tools Menu)

Note: This command appears in the Scripts submenu.

Use this command to select and play back a script. This command displays the following dialog box.

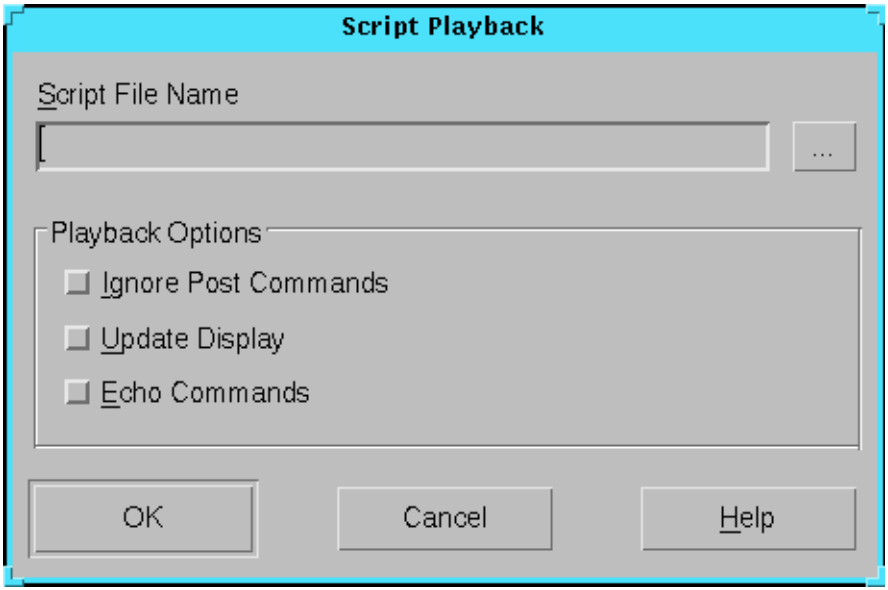


Figure 4-11 Script Playback Dialog Box

Script Playback Dialog Box Options

- Script File Name

  Use the Script File Name field to enter the name of the script file you want to play back, or use the browse button to display the Open dialog box.

- Playback Options

Option	Description
Ignore Post Commands	Does not post the dialog boxes resulting from commands in the script.
Update Display	Updates the display in the FPGA Editor window every time a command that normally redraws the window is run by the script.
Echo Commands	Echos the commands run by the script in the history area.

Print (File Menu)

Note: For detailed instructions on configuring your printer on a UNIX workstation, refer to the "Configuring Xprinter" appendix.

Use this command to send the design file displayed in the active window to the default printer. This command displays the following dialog box.

Note: The following figure shows the Print dialog box on a UNIX workstation; the PC dialog box looks different, but contains similar options.

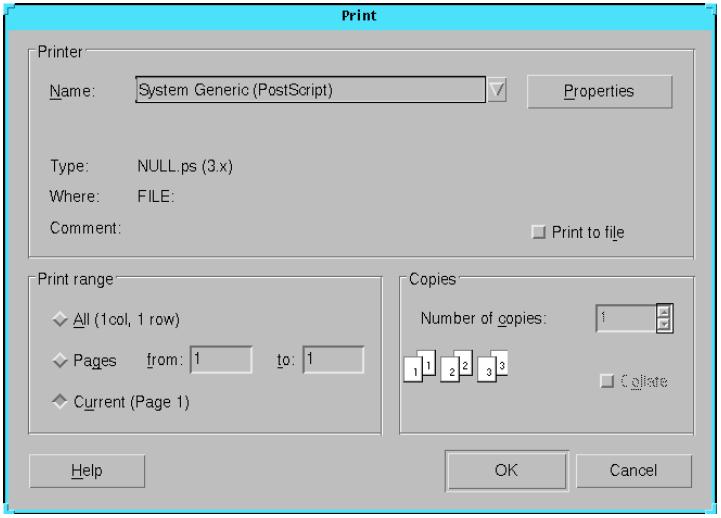


Figure 4-12 Print Dialog Box

Print Dialog Box Options

Note: Print dialog boxes vary between workstations and PCs. Four common print options are described in this section.

- Print Range
  - Use the All option to print the entire file
  - Use Pages From / To to print some of the file
- Use the Copies option to specify the number of copies you want to print
- Use the Print to File option to specify to print to a file

Print Preview (File Menu)

Use this command to display a preview window that shows what your design will look like printed. You can use options in this window to zoom in or out, move from page to page, print, or close the window and return to the FPGA Editor.

Print Setup (File Menu)

Note: For detailed instructions on configuring your printer on a UNIX workstation, refer to the “Configuring Xprinter” appendix.

Use this command to set print options. This command displays the Print Setup dialog box, shown in the following figure. You can set the print properties, such as the name of the printer, the size of the paper, and the orientation of the page.

Note: The following figure shows the Print dialog box on a UNIX workstation; the PC dialog box looks different, but contains similar options.

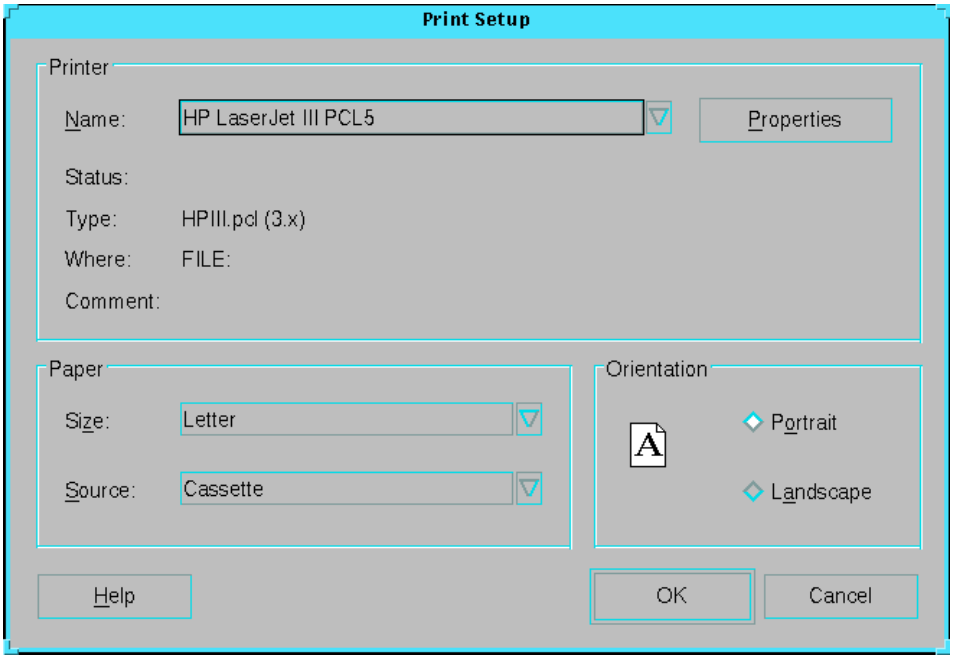


Figure 4-13 Print Setup Dialog Box

Probes (Tools Menu)

Use this command to add or remove probes from your design. This command displays the Probes dialog box. The following information is displayed in this dialog box for each probe.

Note: You can click on the column heading of the first four columns in this dialog box to sort the list in ascending or descending order.

- Pin Name

  Lists an optional user-supplied pin name for the probe.

- Net Name

  Lists the net that is probed.

- Pin Number

  Lists the pin number to which the net is connected if the probe is routed; if the probe is not routed, this column is blank.

- Delay

  Shows the delay from the net's source to the pin if the probe is routed; if probe is not routed, column is blank.

- Other Possible Pin Numbers

  Shows the set of pin numbers that can be used when the probe is routed, or it is blank if the probe command automatically locates a free pin.

The Probes dialog box is shown in the following figure.

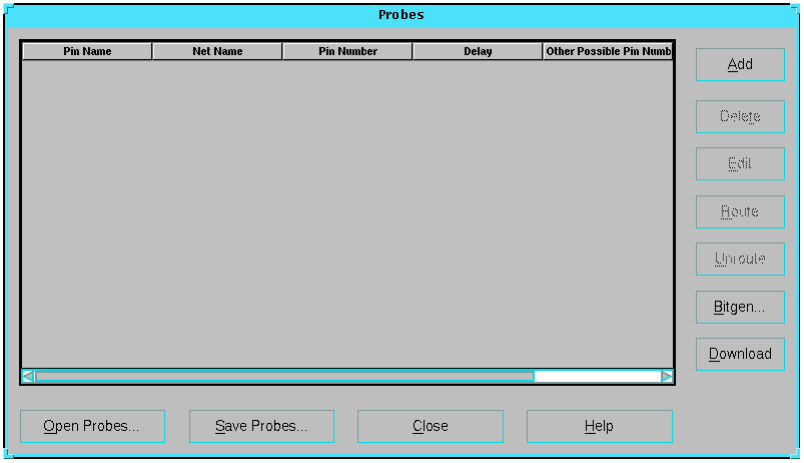


Figure 4-14 Probes Dialog Box

Probes Dialog Box Options

- Open Probes

  Displays the Open dialog box to allow you to select a script file containing the commands that define the probes. When the script is opened, the commands are performed, and the probe definitions are added to the probes list. The Open Probes option is always enabled.

- Save Probes

  Opens the Save As dialog box to allow you to specify a script file name for the probe definitions. This option is enabled when the probes list contains one or more probe definitions.

- Add

  Opens the Define Probe dialog box, shown in the “Define Probe Dialog Box” figure. Use the options in this dialog box to define and add a new probe to your list of probes.

- Delete

  Use this option to delete selected probes from the list of probes, unrouting the pins if needed. This option is enabled when one or more items are selected in the probes list.

- Edit

  Opens the Define Probe dialog box, shown in the “Define Probe Dialog Box” figure. Use the options in this dialog box to edit a probe definition. This option is enabled when only *one* item in the probes list is selected.

- Route

  Starts the interactive router to connect the net to one of the pins listed in the Other Possible Pin Numbers column; the pin with the smallest delay value is selected. Once routed, the pin and delay columns are filled in. This option is enabled when one or more unrouted probes are selected.

- Unroute

  Unroutes the pins and changes the status of the probe to unrouted. This option is enabled when one or more routed probes are selected.

- BitGen

  Opens the Run BitGen dialog box, shown in the “Run BitGen Dialog Box” figure. Use the options in this dialog box to create a BIT file from the probed design. You do not have to save your design first because the BitGen tool is run inside the FPGA Editor.

- Download

  Starts the Hardware Debugger tool so you can download your BIT file to a test device. This tool is run in a separate process from the FPGA Editor.

Define Probe Dialog Box Options

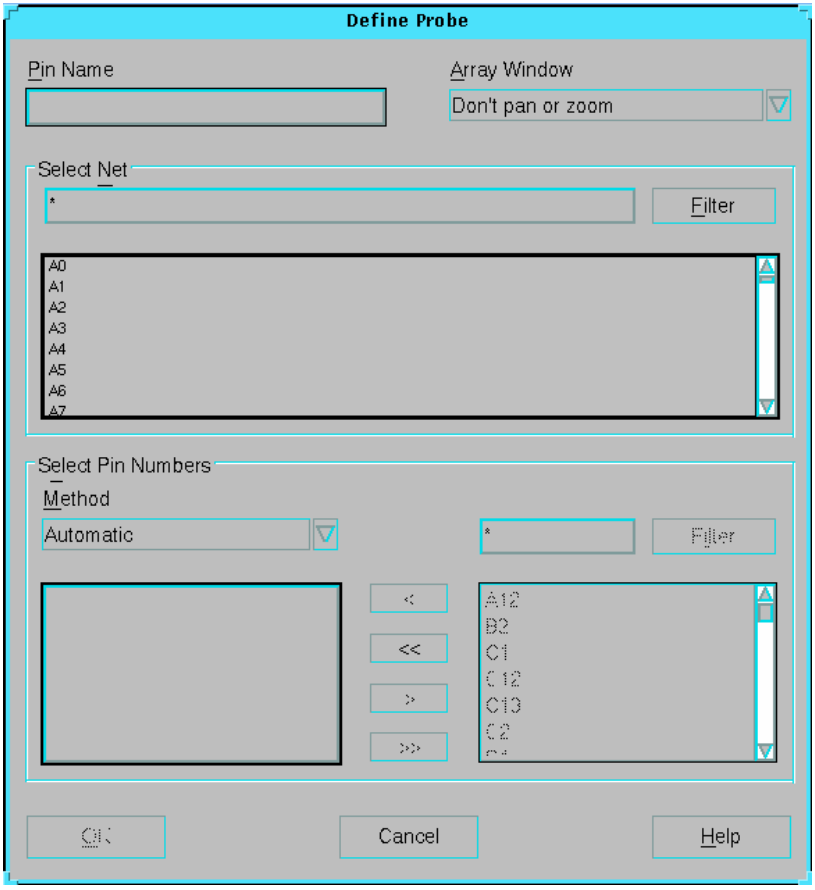


Figure 4-15 Define Probe Dialog Box

- Pin Name

  Specifies the logical name for the probe. This name is used for the IOB when the probe is routed. If you do not specify a name in this field, the net name is the default.

- Array Window

  Use one of the following options to control the display in the Array window when you select nets and pins.

  - Don’t Pan or Zoom

The Array window is not changed

- Zoom to Selected Nets and Pins

  The Array window zooms in to the selected nets and pins

- Zoom to See Entire Device

  The Array window displays the entire device

- Select Net

  Use this field to select a net. Enter a net name pattern (a name with “?” and “*”) to filter the names of unprobed nets in your design. Press return, the filter button, or Alt-F to display the nets that match your filter in the list box. You can then select one of the names in the list. If an Array Window zoom option is selected, the net is selected in the Array window.

- Select Pin Numbers

  Use one of the following options in the Method field to select pin numbers.

  - Automatic

    Disables the other options inside the Select Pin Numbers field; the list boxes are empty

  - Manual

    Enables the other options in the Select Pin Numbers field to allow you to specify the pin numbers for the routed probe. Enter a pin number pattern (a name with “?” and “*”) to filter unused, bonded pins. Press return, the filter button, or Alt-I to display the pins that match your filter in the list box. You can then move one or more pins to and from the left list. The left list is the set of pin targets for the routed probe. If an Array Window zoom option is selected, selected pins in the right list and all pins in the left list are selected in the Array window.

Run BitGen Dialog Box Options

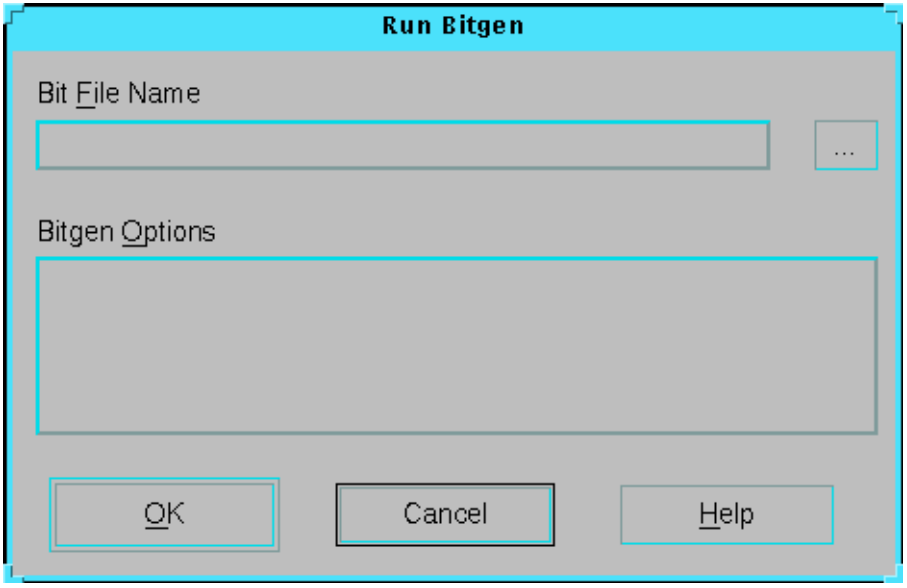


Figure 4-16 Run BitGen Dialog Box

- Bit File Name

  Use this field to enter the name of the BIT file, or use the browse button to select a file.

- BitGen Options

  This field displays the contents of the bitgen.ut file that is produced when BitGen is run in the Flow Engine. If you make any changes to the information in this field, they are saved and available the next time you open this dialog box.

Properties of Selected Items (Edit Menu)

Use this command to display the property sheet for the selected design object. You can use the property sheet to view and change various properties for the selected object. You can display properties for the FPGA Editor window, components, component pins, nets, sites, ratsnest lines, wires, macros, paths and object layers.

This command displays a property sheet similar to the component property sheet shown in the following figure. The property sheet

varies depending on the selected object. For more information, refer to the “Viewing and Changing Properties” section in the “Using the FPGA Editor” chapter.

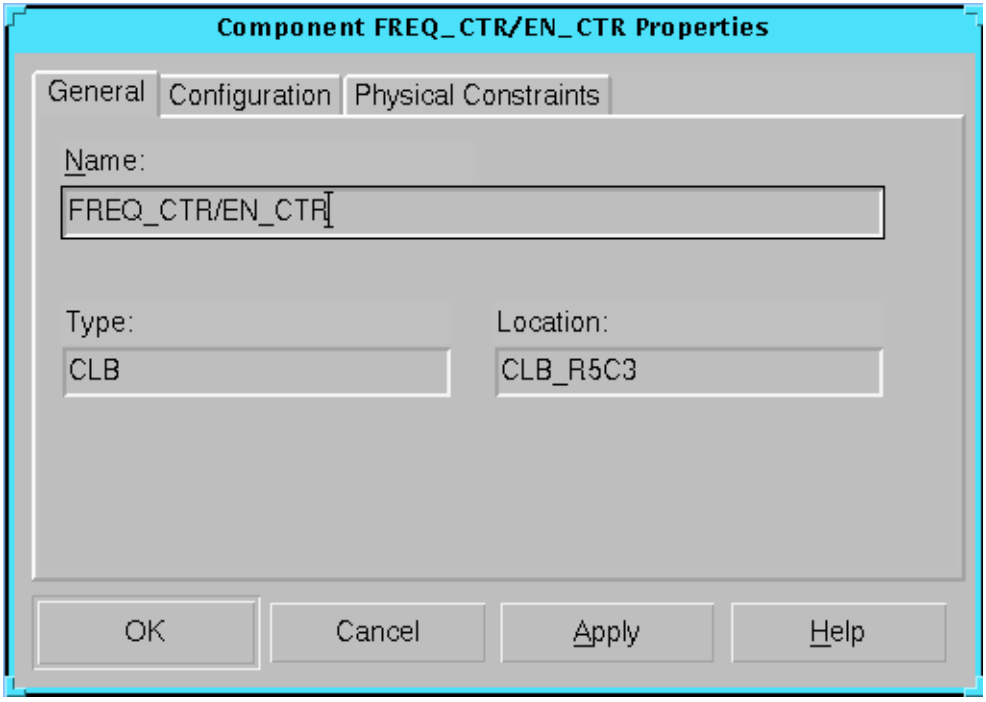


Figure 4-17 Component Property Sheet

Refresh (View Menu)

Use this command to redraw all of the windows in the FPGA Editor.

Route Submenu (Tools Menu)

Route is a submenu in the Tools menu. Use the commands in this submenu to automatically or manually route some or all design objects, or to unroute some or all objects. The following commands are included in the Route submenu.

Note: Refer to the alphabetical listings of these commands for an explanation of their functions.

- Auto Route

- Manual Route
- Unroute
- Auto Route All
- Unroute All

Run (Tools Menu)

Note: This command appears in the DRC submenu.

Use this command to run a design rule check on selected design objects or on your entire design if nothing is selected.

Save (File Menu)

Use this command to save your current design or macro.

Save As (File Menu)

Use this command to save the current design or macro to a different name. This command displays the following dialog box.

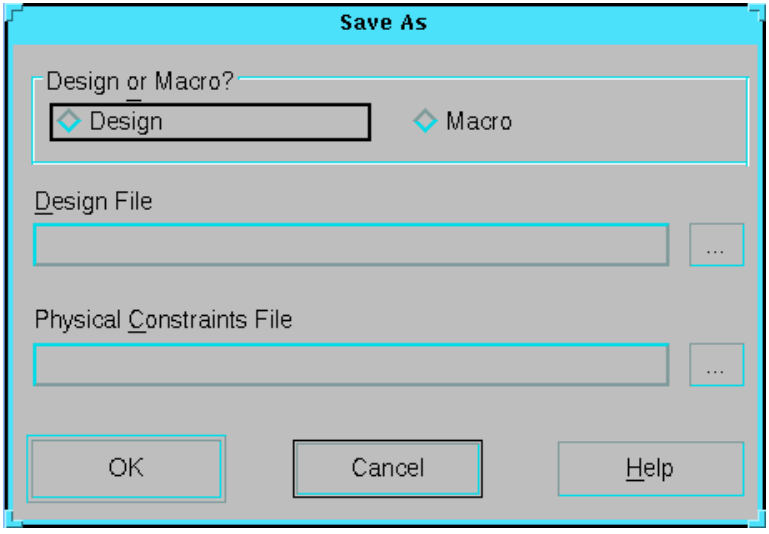


Figure 4-18 Save As Dialog Box

Save As Dialog Box Options

- Design or Macro?

  Specifies whether you want to save a design or a macro file. If you select Macro, the Design File field is replaced with the Macro File field, and the Physical Constraints File field is grayed out.

- Design File / Macro File

  Specifies the name of the design file or macro file you want to save. You can either enter the file name or click the browse button to navigate through the directories.

- Physical Constraints File (PCF)

  Specifies the name of the physical contraints file you want to save. You can either enter the file name or click the browse button to navigate through the directories.

Save As Macro (File Menu)

Use this command to save the current design as a macro.

Scripts Submenu (Tools Menu)

Scripts is a submenu in the Tools menu. Use the commands in this submenu to record a script and play it back.

Note: Refer to the alphabetical listings of these commands for an explanation of their functions.

- Begin Recording
- End Recording
- Playback

Set Macro Reference Comp (Edit Menu)

Use this command to designate a selected component in a macro file as the macro's reference component.

Setup (Tools Menu)

Note: This command appears in the DRC submenu.

Use this command to set the options for running a Design Rule Check (DRC). This command displays the following dialog box.

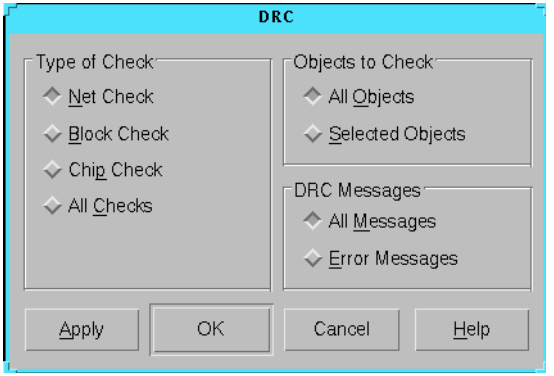


Figure 4-19 DRC Dialog Box

Option	Description
Type of Check	Runs DRC on nets, blocks, chips, or all three.
Objects to Check	Runs DRC on all objects in your design or only on the selected objects.
DRC Messages	Displays all messages produced by the DRC or only the error messages.

Setup and Run (Tools Menu)

Note: This command appears in the Trace submenu.

Use this command to set options for running TRACE; run TRACE on the selected constraint; and display the TRACE summary information. This command displays the following dialog box.

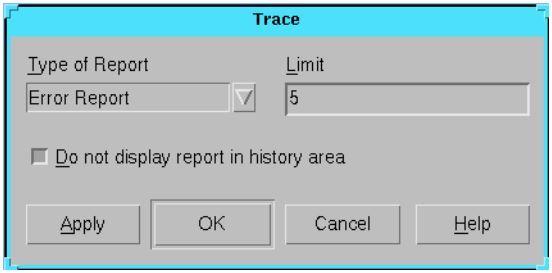


Figure 4-20 Trace Dialog Box

Trace Dialog Box Options

- Type of Report

  Specifies a verbose report or an error report.

- Limit

  Limits the number of errors reported (or the extent of verbose reporting) for each selected constraint. The limit value must be 1 or greater.

- Do not display report in history area

  Suppresses display of the report in the history area.

Standard (View Menu)

Note: This command appears in the Toolbars submenu.

Use this command to show or hide the Standard toolbar.

Status Bar (View Menu)

Use this command to show or hide the Status bar.

Summary (Tools Menu)

Note: This command appears in the Trace submenu.

Use this command to list information on each of the constraints selected for the TRACE run. This command displays the following dialog box.

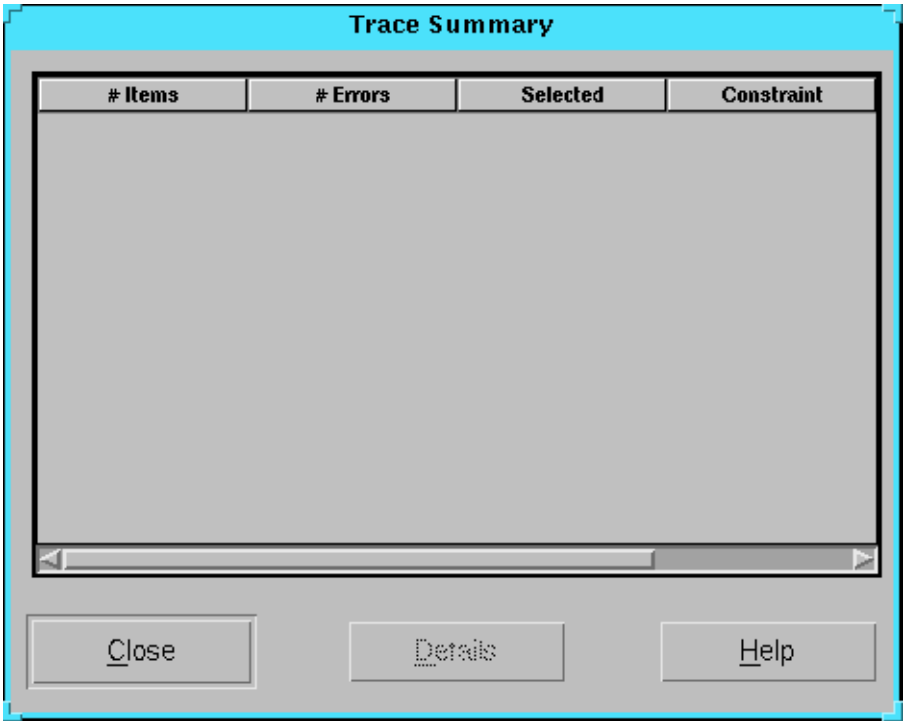


Figure 4-21 Trace Summary Dialog Box

Trace Summary Dialog Box Options

- #Items

  Number of nets and components in the analysis

- Errors

  Number of timing errors found for a particular constraint

- Constraint

  Displays the constraint that is analyzed

Swap (Edit Menu)

Use this command to swamp the selected components or components and site.

Tile Horizontally (Window Menu)

Note: This command appears in the Arrange Windows submenu.

Use this command to arrange the windows as non-overlapping tiles horizontally.

Tile Vertically (Window Menu)

Note: This command appears in the Arrange Windows submenu.

Use this command to arrange the windows as non-overlapping tiles vertically.

Toolbars Submenu (View Menu)

Use this command to show or hide the Command, History, Layer Visibility, Standard, or User toolbars. You can also select the Default Layout command to show all toolbars.

Trace Submenu (Tools Menu)

Trace is a submenu in the Tools menu. Use the commands in this submenu to set options for running TRACE; run TRACE on the selected constraint; display TRACE summary information; and list information on each of the constraints selected for the TRACE run.

Note: Refer to the alphabetical listings of these commands for an explanation of their functions.

- Setup and Run
- Summary

Unbind Macro (Edit Menu)

Use this command to separate a selected macro into its individual components.

Unhighlight (View Menu)

Use this command to remove highlighting from the selected highlighted design objects.

Unhighlight All (View Menu)

Use this command to remove highlighting from all highlighted design objects.

Unplace (Tools Menu)

Note: This command appears in the Place submenu.

Use this command to automatically unplace and unroute a selected, unlocked component.

Unplace All (Tools Menu)

Note: This command appears in the Place submenu.

Use this command to automatically unplace and unroute all unlocked components.

Unroute (Tools Menu)

Note: This command appears in the Route submenu.

Use this command to unroute all selected unlocked nets or portions of nets.

Unroute All (Tools Menu)

Note: This command appears in the Route submenu.

Use this command to unroute all nets in your design except locked nets.

Unselect All (Edit Menu)

Use this command to unselect all selected design objects.

User (View Menu)

Note: This command appears in the Toolbars submenu.

Use this command to show or hide the User toolbar.

World Window (Window Menu)

Note: This command appears in the New submenu.

Use this command to open additional World windows.

Zoom In (View Menu)

Use this command to move in one level in your design for a more detailed view. The zoom is centered around the point in the center of the Array or Block window.

Zoom Out (View Menu)

Use this command to move out one level in your design for a more overall view of your design.

Zoom Selection (View Menu)

Use this command to adjust the scale of the current view so that the selected objects can be seen in the window.

Toolbars

Toolbars provide convenient access to frequently used commands. Click once on a toolbar button to execute a command. When you position the mouse pointer over a toolbar button, a short description, called a tool tip, appears next to the button and a longer description appears in the status toolbar at the bottom of the main window.

The FPGA Editor window contains the following types of toolbars. This section lists and describes the buttons in each toolbar.

- Command Line Toolbar
- History Area
- Layer Visibility
- Standard
- User
- Block Window

Command Line Toolbar

Use the Command Line toolbar, shown in the following figure, to enter commands from the keyboard. Press the F2 key to move the keyboard focus to the Command Line. Refer to the “Command Line

Toolbar" section in the "Getting Started" chapter for more information.

Figure 4-22 Command Line Toolbar

History Toolbar

The History toolbar, shown in the following figure, is located below the Array window and displays commands and responses. All error messages, warnings, and command responses are written to the History toolbar. Information in the History toolbar is especially useful for deciphering unexpected command results. Refer to the "History Area Toolbar" section in the "Getting Started" chapter for more information.

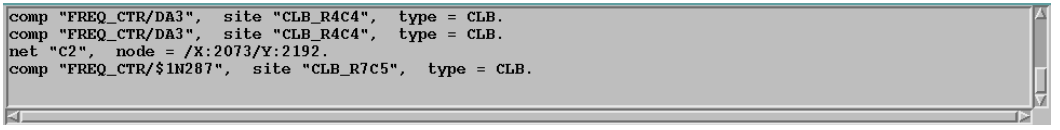


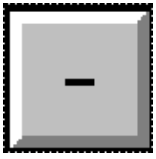
Figure 4-23 History Toolbar

Layer Visibility Toolbar

This section describes the function of the layer visibility toolbar buttons and includes a graphic of each button.

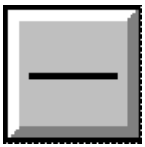
Local Lines

Click this button to show or hide local lines in the Array window.



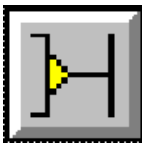
Long Lines

Click this button to show or hide long lines in the Array window.



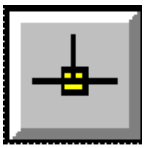
Pin Wires

Click this button to show or hide pin wires in the Array window.



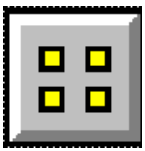
Pips

Click this button to show or hide pips in the Array window.



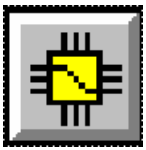
Sites

Click this button to show or hide sites in the Array window.



Switch Boxes

Click this button to show or hide switch boxes in the Array window.

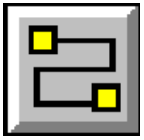


Components

Click this button to show or hide components in the Array window.

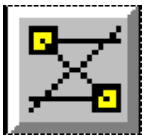
Routes

Click this button to show or hide routing in the Array window.



Rats Nests

Click this button to show or hide rats nests in the Array window.

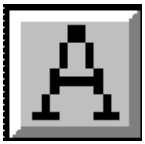


Macros

Click this button to show or hide macros in the Array window.

Text

Click this button to show or hide text in the Array window.



Apply

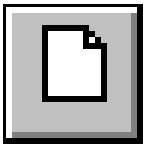
Click this button to apply the state of the layer buttons to the current display in the Array window. When the Apply button indicates “pressed” in the toolbar, any layer that you select is immediately displayed. If the Apply button is not pressed, a selected layer is not displayed until you press the Apply button.

Standard Toolbar

This section describes the function of the standard toolbar buttons and includes a graphic of each button.

New

Click this button to create a new design or macro.

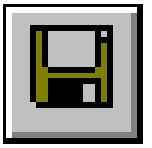


Open

Click this button to open an existing design or macro.

Save

Click this button to save the current design or macro.

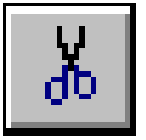


Print

Click this to send the contents displayed in the active window to the default printer.

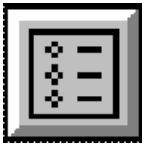
Cut

Click this button to delete the selected design object.



Properties

Click this button to display the property sheets for the selected items.

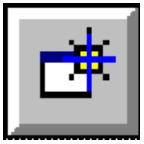


Cascade Property Sheets Vertically

Click this button to arrange the property sheets so they overlap vertically.

Close All Property Sheets

Click this button to close all open property sheets.



Default Window Layout

Click this button to arrange the windows using the default layout.

Maximize List Window

Click this button to expand the List window to its maximum size.

Maximize Array Window

Click this button to expand the Array window to its maximum size.

Maximize Block Window

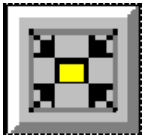
Click this button to expand the Block window to its maximum size.

New Block Window

Click this button to open a block window for the selected component.

Detailed View

Click this button to adjust the scale of the current design to its maximum zoom in level.

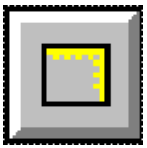


Zoom In

Click this button to adjust the scale of the current design to see a more detailed view.

Refresh

Click this button to redraw all the windows.



Zoom Selection

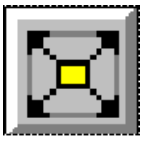
Click this button to zoom in on selected objects in the current design.

Zoom Out

Click this button to zoom out one level in the current design for a less detailed view.

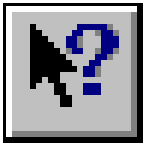
Full View

Click this button to display the entire design in the Array window.



Help

Click this button to open context-sensitive help.



User Toolbar

Use the User toolbar to perform frequently used commands. To use a command, select the appropriate command button with the left mouse button. You can customize the User toolbar with the Button and Unbutton commands described in the“Command Line Syntax” chapter or by editing the fpga_editor.ini or the fpga_editor_user.ini file. These files define the default User toolbar buttons that appear when the FPGA Editor window opens. For more information, see the “Main Window” section in the “Getting Started” chapter.

Block Window Toolbar

This section describes the function of the Block window toolbar buttons and includes a graphic of each button.

Select Component or Site

Click this button to select a component or site from the Select Component or Site dialog box.

Begin Editing

Click this button to edit the component logic.

Apply

Click this button to apply the changes you have made in the Block window.

Restore

Click this button to undo any previously applied changes to the component.

Run DRC

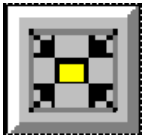
Click this button to run a design rule check on the component.

Show/Hide Attributes

Click this button to display the attributes for the component.

Detailed View

Click this button to adjust the scale of the component to its maximum zoom in level.

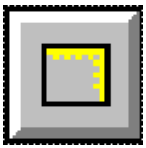


Zoom In

Click this button to adjust the scale of the component to see a more detailed view.

Refresh

Click this button to redraw the Block window.

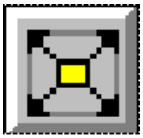


Zoom Out

Click this button to zoom out one level in the current component for a less detailed view.

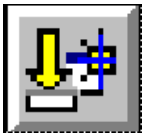
Full View

Click this button to display the entire component in the Block window.



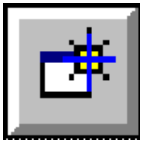
Save Changes and Closes Window

Click this button to save changes and close the Block window.



Ignores Changes and Closes Window

Click this button to ignore changes and close the Block window.



Keyboard Shortcuts

You can use the following keyboard shortcuts in the FPGA Editor.

Table 4-3 Keyboard Shortcuts

Action	Keyboard Shortcut
File → New	Ctrl N
File → Open	Ctrl O
File → Save	Ctrl S
File → Print	Ctrl P
Cut text from command line	Ctrl X
Copy (History area toolbar)	Ctrl C
Paste text to command line	Ctrl V
Help	F1
Go to command line	F2
Go to next window	Ctrl-F6
Go to previous window	Shift-Ctrl-F6

Chapter 5

Working with Physical Macros

A physical macro is a logical function created from components of a specific device family. Physical macros are stored in macro library files with a .nmc extension. In addition to components and nets, a macro can also contain placement and routing information. It can be unplaced, partially placed, fully placed, unrouted, partially routed, or fully routed.

You can create a new macro library file in the FPGA Editor or you can save an existing design as a macro. After creating a macro, you can instantiate it in your design. When you instantiate a macro, the contents of the macro library file are copied into your design file, and the link to the macro library file no longer exists. If you edit the macro library file, any new changes are not reflected in the instantiated macro in your design file. Refer to the following figure for an illustration of instantiating a macro.

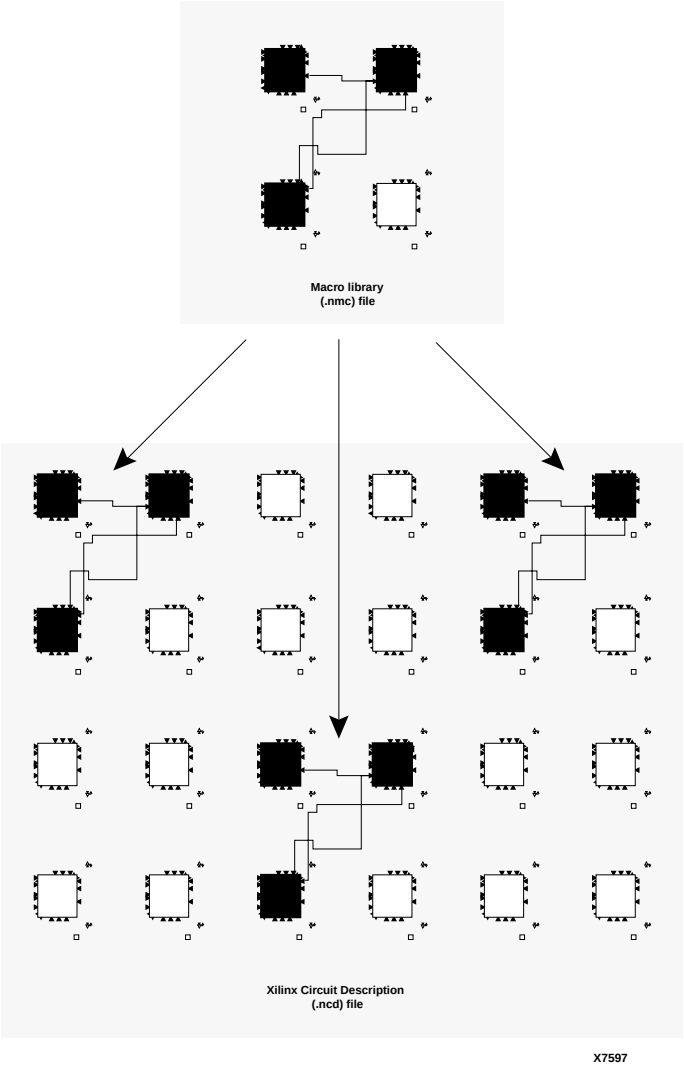


Figure 5-1 Instantiating a Macro in Your Design

You can also instantiate a macro into a schematic drawing by entering a block in the schematic, configuring the block appropriately, and placing a reference to the .nmc file in the schematic.

This chapter describes creating, editing, and using macros in the FPGA Editor. It contains the following sections.

- "Macro Terminology"
- "Creating a New Macro File"
- "Opening an Existing Macro"
- "Saving your Design as a Macro File"
- "Saving a Macro Library File"
- "Saving a Macro Library File as a Design File"
- "Adding Macros to Your Design"
- "Operating on Macro Components and Nets in Your Design"
- "Selecting Macros in Your Design"
- "Deleting Macros from Your Design"
- "Viewing and Changing Macro Properties in Your Design"
- "Moving Macros in Your Design"
- "Unbinding Macros in Your Design"
- "Placing and Unplacing Macros in Your Design"
- "Routing and Unrouting Macros in Your Design"
- "Macro External Pins in Your Design"
- "Editing Your Macro File"
- "DRC Checks in Your Macro File"

Macro Terminology

The definitions in this section are specific to macros. See the following figure for an illustration of some of these terms.

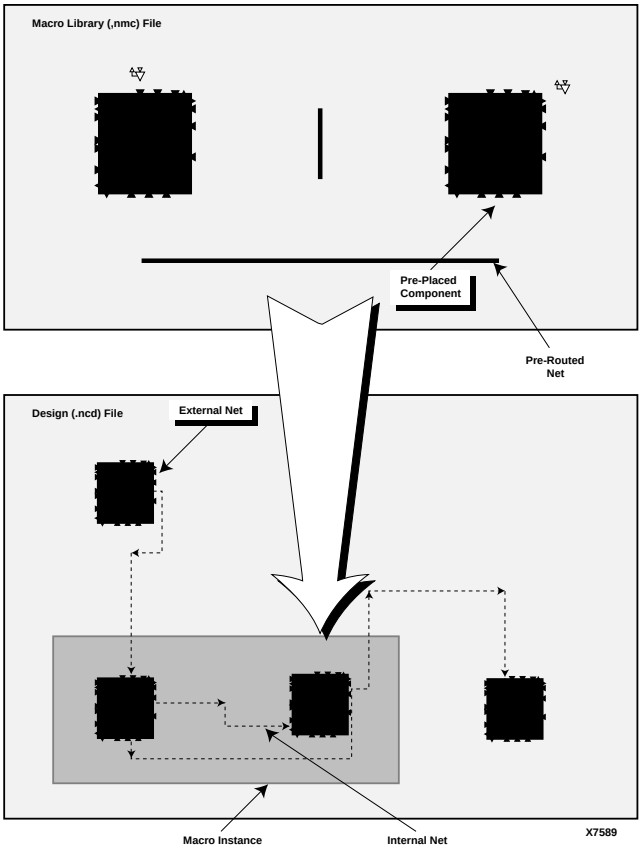


Figure 5-2 Macro Terminology

Macro Library File

A file containing the definition of a macro. Macro library files have a .nmc extension.

Macro Instance

A copy of a macro library file inserted in your design file. When you add a macro instance to your design, you “instantiate” the macro. Your design can contain multiple instances of the same library file,

each with a unique instance name. Because the library file is copied into the design file when you instantiate a macro, if you then edit the library file, the changes are not reflected in the macro instantiated in your design file.

Pre-placed Component

A component that is placed in the macro library file.

Pre-routed Net

A net that is completely routed in the macro library file.

Note: When you instantiate a pre-routed macro in your design, the design can take much longer time to place and route, depending on the routing complexity. Xilinx recommends allowing PAR to route the macro with your design.

Reference Component

A component in the macro library file used as a reference when a macro instance is placed, moved, or copied. Placement and routing of all other pre-placed macro components are determined relative to this component. If at least one of the macro's components is pre-placed, the macro will have a reference component. If none of the macro components are pre-placed, the macro will not have a reference component.

External Pin

A macro pin used to connect the components in an instantiated macro to other components in your design (outside of the macro).

Internal Net

A net in the macro library file that does not have a connection to any of the macro's external pins.

External Net

A net outside of a macro instance connected to one of the macro's external pins. Part of an external net can lie within the macro if the macro library file contains a net that is connected to an external pin.

Unbind

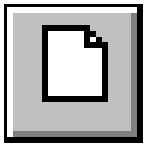
Use this command to disassociate a macro's components and nets from the macro. When you unbind a macro, the macro name is removed from your design's database. All of the components and nets formerly in the macro are then treated as separate components and nets.

Creating a New Macro File

Note: See the "From the Command Line" section of the "Getting Started" chapter for the command line options for creating a new macro.

To create a new macro in the FPGA Editor, follow these steps.

1. Select **File** → **New** or click on the New toolbar button.



   The New dialog box appears, as shown in the "New Dialog Box" figure of the "Menu Commands" chapter.

2. Select the **Macro** option.
3. Enter the macro name in the Macro File field. If you do not enter the .nmc extension, it is automatically added when the file is created.

   You can open a new macro under a directory other than the current working directory. Type in the path name of the target directory in the Macro File field, or use the browse button to select your target directory and specify your macro file name.

4. Click the Select Part button to display the Part Selector dialog box, shown in the "Part Selector Dialog Box" figure of the "Menu Commands" chapter.

Note: Although you must specify a part number and speed, a macro can be instantiated in any design file of the same family. For example, if you create a macro library file and specify a 4008PG191 package at a speed of 5, the macro can still be instantiated in a design file for a

4010PQ208 package at a speed of 6, or any other Xilinx XC4000 family design file.

5. Select a Family, Device, Package, and Speed Grade for your macro.

Note: You can only select a part number from a part library you have installed on your system.

6. Click **OK**. The Part field in the New dialog box is filled in with your selections.
7. Click **OK** to close the New dialog box.

   An empty (unprogrammed) macro is loaded into the FPGA Editor window with the part number and speed as specified.

Opening an Existing Macro

Note: See the "From the Command Line" section of the "Getting Started" chapter for the command line options for opening an existing macro.

To open an existing macro file while you are in the FPGA Editor window follow these steps.

1. Select **File** → **Open** or click on the Open toolbar button.

   The Open dialog box appears, as shown in the "Open Dialog Box" figure of the "Menu Commands" chapter.
2. Select the **Macro** option.
3. Enter the name of the .nmc file you want to open in the Macro File field, or use the browse button to specify the macro file name and directory.
4. Select an Edit Mode for the macro from the pull-down list box.

   Select Read Only, No Logic Changes, or Read Write. The default is No Logic Changes.
5. Click **OK**.

The macro file you specified is loaded in the FPGA Editor window.

Saving your Design as a Macro File

You can create a macro library file by saving your design as a macro. To use this macro, you must assign one or more external pins, as described in the "" section.

Note: Constraints are not retained when you save your design file as a macro library file. A constraint file is not generated, even if your design had constraints defined.

With the Same Name

To save your current design as a macro with the same name, select **File** → **Save As** **Macro**. Your current design file is saved as a macro file with the same name as your design but with a .nmc extension.

With a Different Name

To save your design as a macro library file with a different name, use this procedure.

1. Select **File** → **Save As** to display the Save As dialog box, shown in the "Save As Dialog Box" figure of the "Menu Commands" chapter.
2. Select the **Macro** option.
3. Enter the macro name in the Macro File field with a .nmc extension.

   You can save your macro under a directory other than the current working directory. Type in the path name of the target directory in the Macro File field, or use the browse button to select your target directory and specify your macro file name.
4. Click **OK**.

   The dialog box closes, and the macro file is saved with the name you specified. The file name in the Title Bar at the top of the FPGA Editor window changes to indicate that this new file is currently displayed in the window. When you later save or exit the file, it is saved to the new file name, not the original file name.

Saving a Macro Library File

When you save a macro library file, you cannot save a constraint file along with the NMC file, even if constraints were created when the macro library file was edited. All constraints are lost when you save the NMC file.

With the Same Name

To save your current macro library file as a macro file with the same name, select **File** → **Save**.

With a Different Name

To save your macro library file as a macro library file with a different name, use this procedure.

1. Select **File** → **Save As** to display the Save As dialog box, shown in the "Save As Dialog Box" figure of the "Menu Commands" chapter.
2. Select the **Macro** option.
3. Enter the macro name in the Macro File field with a .nmc extension.

   You can save your macro under a directory other than the current working directory. Type in the path name of the target directory in the Macro File field, or use the browse button to select your target directory and specify your macro file name.
4. Click **OK**.

   The dialog box closes, and the macro file is saved with the name you specified. The file name in the Title Bar at the top of the FPGA Editor window changes to indicate that this new file is currently displayed in the window. When you later save or exit the file, it is saved to the new file name, not the original file name.

Saving a Macro Library File as a Design File

To save your macro library file as a design file, use this procedure.

1. Select **File** → **Save As** to display the Save As dialog box, shown in the "Save As Dialog Box" figure of the "Menu Commands" chapter.

2. Select the **Design** option.
3. Enter the design name in the Design File field. If you do not enter the .ncd extension, it is automatically added to the file name.

   You can save your design under a directory other than the current working directory. Type in the path name of the target directory in the Design File field, or use the browse button to select your target directory and specify your design file name.
4. If applicable, enter the constraints file name for the design in the Physical Constraints File field, or use the browse button to select a directory and specify a file name.
5. Click **OK**.

   The dialog box closes, and the design file is saved with the name you specified. Any constraints in the macro library file are written to the specified constraint file. The file name in the Title Bar at the top of the FPGA Editor window changes to indicate that this new file is currently displayed in the window. When you later save or exit the file, it is saved to the new file name, not the original file name.

Adding Macros to Your Design

When you add a macro to your design, you are instantiating a macro or adding an instance of a library macro file to your design. A design can contain multiple instances of the same macro library file; each one has a unique name in your design. A macro can only be added if the design file and the macro library file are the same family. For example, if your design is an XC4000 part, you can only add an XC4000 macro library file.

The first time you instantiate a macro library file, a copy of the library file is placed into your design file. Any subsequent instantiations of the same library file into your design file refers to this local copy, and is not affected by changes in the external library file that was used for the original instantiation.

To add a macro to your design, follow this procedure.

1. If you want to place the macro when you add it, select a vacant site in which to place the macro.

The site must match the reference component specified in the macro library file. For example, if the macro library file specifies an I/O component as the reference component, the selected site must be an I/O component site.

If there is no reference component in the macro library file, the selected site is ignored and the macro is unplaced when it is instantiated. If you do not select a site, the macro is unplaced when it is instantiated.

2. Select **Edit** → **Add Macro** to display the Add Macro dialog box, as shown in the "Add Macro Dialog Box" figure of the "Menu Commands" chapter.
3. Fill in the dialog box fields and click **OK**. The fields in this dialog box are described in the "Add Macro Dialog Box Options" section of the "Menu Commands" chapter.

   An instance of the macro library file is added to your design. If you selected a site, the macro's reference component is placed at the specified site, and any other placed components in the macro library file are placed relative to the reference component.

When you close the Add Macro dialog box, a Macro Properties property sheet may appear for the newly created macro if the Automatic Post option is enabled in the Main Properties property sheet. You can edit the property sheet to modify macro properties or click **Cancel** to close the property sheet.

Notes on Adding Macros

- If you do not specify a macro name when you add a macro, the name assigned to the new macro is in the format: *$libfile_number*, where *libfile* is the name of the macro library file that defined the macro when it was added. *Number* is a number assigned to that instance of the macro library file. Numbering starts at 0, and increases by one for each new added macro. For example, if you add multiple instances of a macro library file named "adder" the first instance is $adder_0, the second is $adder_1, and so on.
- Any characters special to the FPGA Editor command interpreter must be preceded by a backslash (\) escape character when used in a macro name. Special characters are quotation marks (" or ') * ; ? # - (leading dash). The restriction only applies to commands entered at the command line or those in an FPGA Editor

command script file. The special characters can be entered in the Macro Properties property sheet without the escape character. If you use another vendor's tool set in conjunction with the Xilinx tools, they may have other naming restrictions.

- When a macro is added, the names of all components, nets, and external pins within the macro has this format: *macro_name*/*object_name*, for example, $adder_3/$comp_0 or $decoder_2/$extpin_0.
- All components, nets, and macros have their own name space and must have unique names within this name space. For example, you can have a component and a macro named "FRED," but you cannot have two macros named "FRED" or two nets named "FRED." The FPGA Editor prevents you from entering non-unique names within a name space. Also, the name cannot be empty.
- If the original (external) macro library file is changed or deleted, there is no effect on any instances of this library file in your design.
- If you change the external macro library file and want to update an existing design to use this revised library file, you can do one of the following.
  - Remap your design
  - Delete all instances of the revised macro library file, and then add new instances of the revised macro library file in place of the old instances.

Operating on Macro Components and Nets in Your Design

Normally you place, route, unplace, and unroute a macro instance as a whole object instead of performing these operations on the individual components and nets that comprise the macro. If a macro is instantiated from a completely placed and routed library file, these operations are always performed on the entire macro. However, because it is possible to define a macro that is not completely placed and routed, you must place and route those individual components and nets that do not have predefined placement and routing informa-

tion. The following rules govern a macro's internal components, nets, and pins.

- Components within a macro instance cannot be added, deleted, reconfigured, or renamed.
- Pre-placed components that are placed in the macro definition file cannot be manually or automatically placed, unplaced, or swapped in the macro instance, except by placing, unplacing, or swapping the entire macro instance.
- Components that are not pre-placed can be placed, unplaced, and swapped in the macro instance.
- Internal nets in a macro instance cannot be deleted or added. Pins cannot be added to or deleted from internal nets.
- Pre-routed nets that are routed in the macro library file cannot be manually or automatically routed or unrouted in the macro instance, except by routing the entire macro instance.
- Macro nets that are not pre-routed can be routed and unrouted.
- Unused pins on macro components cannot be used to create non-macro nets. Only external pins can be connected to external nets.

Selecting Macros in Your Design

To select a macro in your design, display a list of the appropriate macros (all, placed, or unplaced) in the List window, and then select the desired macro name. If you select the name of a placed macro, the components and nets making up the macro change color in the Array window.

Deleting Macros from Your Design

When you delete a macro, all of the macro's external pins are unrouted, all components and nets that are part of the macro are removed, and the macro name is deleted from the database.

To delete a macro, follow this procedure.

1. Display a list of macro names in the List window.
2. Select the macros to delete.
3. Select **Edit** → **Cut.**

The macros are eliminated from the database.

Viewing and Changing Macro Properties in Your Design

To view macro attributes, follow this procedure.

1. In the List window, display a list of macro names.
2. Select a macro from this list.
3. Select **Edit** → **Properties of Selected Items** to display the Macro Properties property sheet shown in the following figure. This property sheet contains the General and Physical Constraints pages.

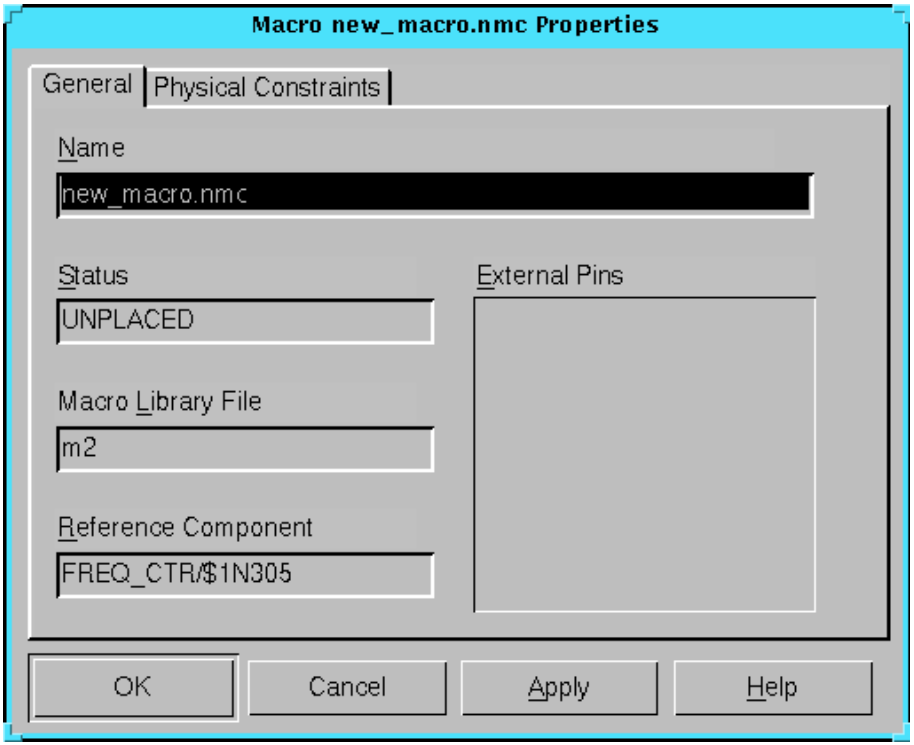


Figure 5-3 Macro Properties Property Sheet

General Page

Refer to the following table for a description of the General page.

Property	Description
Name	Name of the macro. If you change the macro name, all of the names of the components, nets, and external pins that are part of the macro are updated automatically to reflect this change.
Status	Indicates whether the macro is unplaced or placed. A macro is only shown as placed if all the components in the macro are placed.
Macro Library File	Name of the macro library file that defined this macro instance.
Reference Component	Indicates that the component is designated as a reference component. A macro without pre-placed components does not have a reference component; a macro with at least one pre-placed component has one.
External Pins	Lists the pins that are defined as external pins.

Physical Constraints Page

This page displays the constraints that are applied to the macro. Refer to the following table for a description of the Physical Constraints page.

Property	Description
Lock Placement	If enabled, indicates a lock macro or global lock placement constraint is applied. If a macro is locked, all macro components that were pre-placed that is, components that were placed in the macro's library file are locked. The macro cannot be unplaced.
Requirement	Specifies whether the value in the Location Range field is an absolute requirement (hard) or not (soft) for the placement tools.
Effort	Sets up a priority for the autoplacer to resolve constraint conflicts.

Property	Description
Location Range	Places the macro's reference component at a specified site, places all of the macro's pre-placed components (that is, all components that were placed in the macro's library file) in sites relative to the reference component, and locks all of these placed components at their sites.
Block Paths	Use this timing constraint to block the enumeration of all timing paths that go through this macro
TSid	Assigns a timing period or frequency to a timing specification

Moving Macros in Your Design

To move a macro with placed components to an unused group of sites, use the Swap command. When you move a placed macro by swapping, you save a step compared to unplacing the macro then placing it at the new location.

To move a macro to an unused group of sites, follow this procedure.

1. Select the macro to move.
2. Select an unused site for the macro's reference component.

   The reference component and the selected site must be the same type of block that is, I/O block and I/O block, or logic block and logic block.
3. Select **Edit** → **Swap.**

   The reference component moves to the unused site, and the other components in the macro move to maintain their positions relative to the reference component.

   If the Automatic Routing Option is on, each macro's external pins are routed after the macro is placed. Also, any non-prerouted macro nets are automatically routed.

Unbinding Macros in Your Design

When you unbind a macro, you disassociate the macro's components and nets from the macro. The macro name is deleted from your design's database. After unbinding, all of the components and nets

are treated as separate components and nets. Also, component names and net names are changed, replacing the forward slash (/) that indicates the macro's library file with an underscore (_).

To unbind a macro, follow these steps.

1. Display a list of macro names in the List window.
2. Select the macros to unbind.
3. Select **Edit** → **Unbind Macro**.

   For each of the selected macros, the included components and nets no longer are associated with the macro, and the macro name disappears from the List window.

Placing and Unplacing Macros in Your Design

Macros can be placed in the Array window either automatically or manually. When you use automatic placement (AutoPlace), the system selects an appropriate site or sites for each macro you select. When you use manual placement, you select both a macro and a site in which to place the macro's reference component.

When you manually place a macro, you only place the pre-placed components in the macro (those components that were placed in the macro library file defining this macro instance). You must place any unplaced components in the macro's library file in a separate operation. When you automatically place a macro, the system tries to place all of the macro components, whether they are pre-placed or not.

You can also unplace macros. Unplacing a macro unroutes each of the macro's external pins, removes the macro from the Array window, and adds the macro to the list of your design's unplaced macros.

AutoPlacing Macros

You can place macros automatically with the Auto Place command.

1. Display a list of unplaced macros in the List window.
2. Select the macros to automatically place.
3. Select **Tools** → **Place** → **Auto Place**.

   The macros you selected are automatically placed in vacant sites in the Array window. For each macro, any connections that were

unrouted in the macro's library file are routed when the macro is placed.

If the Automatic Routing Option is On, each macro's external pins are routed after the macro is placed. Also, any non-prerouted macro nets are automatically routed.

Manually Placing Macros

There are two macro manual placement procedures.

- Manually placing an unplaced macro in a vacant site.
- Moving a macro to another site after it has been placed.

To manually place an unplaced macro, follow this procedure.

1. Display a list of unplaced macros in the List window.
2. Select one name from the list of unplaced macros.
3. Select a vacant site in the Array window in which to place the macro's reference component.

   The macro's reference component and the selected site must be the same type of block (I/O component and I/O component or logic component and logic component).

4. Select **Tools** → **Place** → **Manual Place.**

   The macro's reference component is placed in the selected site, and all of the macro's pre-placed components (components placed in the macro's library file) are placed in sites relative to the reference component. Macro components that are not pre-placed must be placed in a separate operation.

   Any connections that were routed in the macro's library file are routed when the macro is placed. If the Automatic Routing Option is On, the macro's external pins are routed after the macro is placed. Also, any non-prerouted macro nets are automatically routed.

Unplacing

The Unplace command removes selected macros from their current sites and puts them into the unplaced macros list. The list of unplaced macros can be viewed in the List window. Unplaced macros can be

re-placed. Before unplacing a macro, the system unroutes each external pin on the macro.

Note: Locked macros cannot be unplaced.

To unplace selected macros, follow this procedure.

1. Select the macros to unplace in the List window.
2. Select **Tools** → **Unplace**.

   All of the selected macros are unplaced.

Routing and Unrouting Macros in Your Design

Routing and unrouting macros is similar to routing and unrouting components. These operations are described in the "Routing and Unrouting" section of the "Using the FPGA Editor" chapter.

Notes on Routing and Unrouting Macros

- To select a macro for automatic routing, you must display a list of placed macros in the List window, and then select the name of the desired macro.
- When you place a macro, any pre-routed connections are automatically routed after the macro is placed. You cannot unroute these connections in your design.
- When you place a macro without the Automatic Routing option enabled, any internal connections that are unrouted in the macro's library file are unrouted after the macro is placed. You must perform a separate route operation to route these connections.
- When you automatically route a macro, each external pin connected to a net is routed. Also, any nets that are not pre-routed are automatically routed.

Macro External Pins in Your Design

In your design, external macro pins are treated as other pins in your design. You can add them to nets in your design, route and unroute them (if external to the macro), and find them with the Find command. You cannot add or delete external pins in your design, and you cannot change the name of an external pin.

Editing Your Macro File

This section describes how to edit your macro library file. You can perform the following editing operations.

- Add, delete, list, and view properties of external pins
- Designate a macro's reference component
- Add a macro to the library file
- Place and route macros
- Perform a macro DRC

The FPGA Editor Edit menu includes the following macro commands.

Table 5-1 Edit Menu Macro Commands

Command	Description
Add Macro	Use this command to add a macro to your design
Add Macro External Pin	Use this command to define a selected component pin as a macro external pin
Set Macro Reference Comp	Use this command to designate a selected component in a macro file as the macro's reference component
Unbind Macro	Use this command to separate a selected macro into its individual components

Adding External Pins

External pins connect the instantiated macro to other components in your design. You define the external pins in the macro library file, and the pins cannot be modified in an instantiated macro. External pins are displayed in the same color as the macro layer in the Array window.

To add external pins to a macro library file, follow these steps.

Note: If you are adding a large number of external pins, you can create a User toolbar button to perform this operation. See the "Button" section of the "Command Line Syntax" chapter for more information.

1. Open a macro file in the FPGA Editor.
2. Select the pins that you want to define as external pins.
3. Select **Edit** → **Add Macro External Pin**.

   The selected pins are now external pins; the color of the external pins changes to the color used for the macro layer.

When you add external pins, the "External Pin Property Sheet" figure is displayed for each newly created external pin if the Automatic Post option is enabled in the Main Properties property sheet.Each property sheet displays the name of the new external pin and additional pin information. You can edit the property sheet to modify external pin properties, or you can click **Cancel** to close the property sheet. See the "Viewing and Changing External Pin Properties" section for details.

When you add an external pin, the name assigned to the new pin is in the format *$extpin_number*, where *number* is a number assigned to each new external pin. Numbering starts at 0, and increases by one for each new external pin. For example, if you add multiple external pins, the first one is $extpin_0, the second is $extpin_1, and so on.

Macro to External Net Recommendations

For macro nets connected to external nets, use the recommendations in this section to declare and name external pins, and to set their Type attributes.

- If a macro net is an output to the external circuitry (that is, one or more pins on the net are drivers for the external net), and the macro net has both input and output pins, declare one output driver pin as external. If there are multiple output pins on the net, it does not matter which one you select.
- If a macro net is an input to the external circuitry (that is, one or more pins on the net act as loads for the external net), and the net has both input and output pins, declare one input pin as external. If there are multiple input pins on the net, it does not matter which one you select.
- If you use the macro library file in a schematic, you must give the external pins in the macro library file the same names as the pins on the symbol used to instantiate the macro in the schematic.

Note: If your schematic symbol contains a multi-bit pin and your schematic is read into the Xilinx tools as an XNF file, you must name the corresponding macro external pins in the format: *pin_name number* (for example, DATA<0> or A<2>). When you name these external pins in the macro, you must insert the angle brackets (< and >) to denote the bit numbers for these pins.

- To ensure timing analysis works correctly when the macro is instantiated, you may have to set each external pin's Type property when you add the external pin to the library file. For most cases, the default Type set by the system is adequate. External pin attributes are described in the "Viewing and Changing External Pin Properties" section.

The following examples illustrate these recommendations.

- Example 1

  The following figure shows a macro that connects an external clock pin to multiple clock input pins. Only one K pin needs to be designated as the external clock pin to the macro.

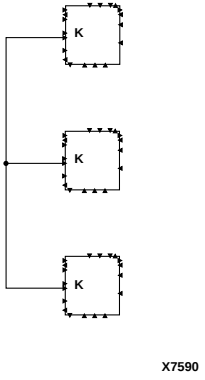


Figure 5-4 External Pins Example 1

- Example 2

  The following figure shows a macro that functions as a latch. External pins appear as filled-in triangles. There are two input external pins and one output external pin for the macro. The output external pin (Y) also feeds back to an input pin (the F1 pin) within the macro, but only the Y pin is used as an external

pin. Y is a driver to the external circuitry, and should be designated as an external pin.

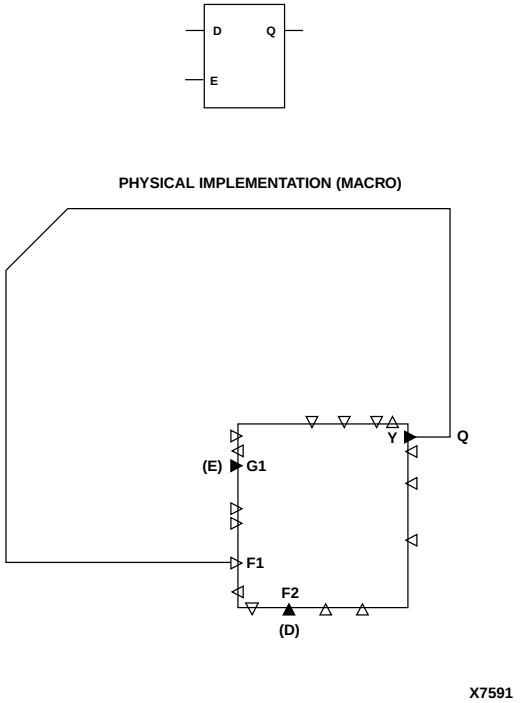


Figure 5-5 External Pins Example 2

Viewing and Changing External Pin Properties

To view or change external pin attributes, follow these steps.

1. Select an external pin.
2. Select **Edit** → **Properties of Selected Items** to display the External Properties property sheet, as shown in the following figure.

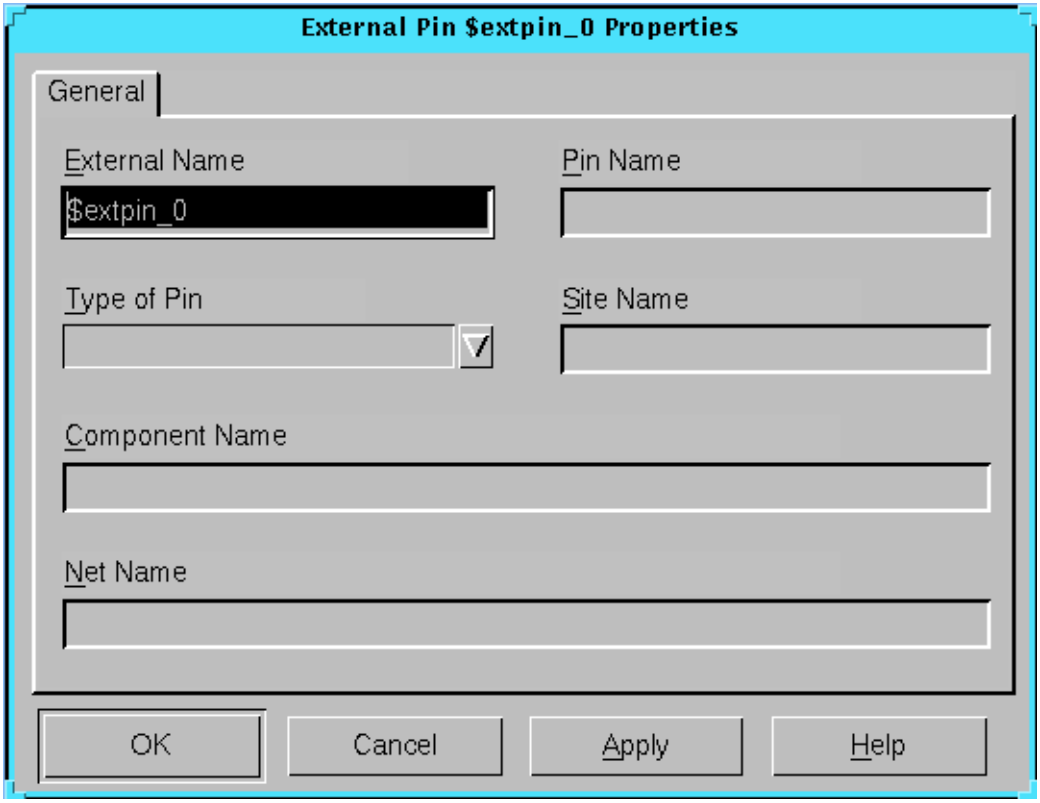


Figure 5-6 External Pin Property Sheet

Refer to the following table for a description of the properties in the External Pin Property sheet.

Property	Description
External Name	Name of this pin when the macro library file is instantiated in your design
Pin Name	Name of component or site pin
Type of Pin	Specifies the function of the pin within the macro. The pin type determines how paths passing through the pin are defined for timing analysis. Pin types are described in the following tables.
Site Name	Site in which the component containing the pin is placed.

Property	Description
Component Name	Name of the component containing the pin.
Net Name	Name of the net connected to the pin.

For an input pin, the pin types are the following.

Type	Description
INPUT	Pin is an input to combinational logic in the macro; it is not clocked.
CLOCK	Pin is used as a clock signal within the macro.
SRDIRECT	Pin is used as an asynchronous Set or Reset signal within the macro.
ENABLE	Pin is used as an asynchronous control line (for example, a tristate buffer enable) within the macro.
SYNCINPUT	Pin is an input that is clocked within the macro (for example, a register input).
SYNCENABLE	Pin is used as a control line synchronous to a clock within the macro.

For an output pin, the pin types are the following.

Type	Description
OUTPUT	Pin is an output from combinational logic within the macro; it is not clocked within the macro.
SYNCOUTPUT	Pin is an output from clocked logic within the macro. The pin is synchronous with respect to the macro clock.
DIRECTIN	Pin should be treated as a direct input pin, that is, a pin with no internal delay. This pin type **should not** be specified for an external macro pin.

Deleting External Pins

When you delete an external pin, the pin is no longer defined as external. If the external pin is connected to a net, it remains connected after you delete it as an external pin.

To delete external pins, follow this procedure.

1. Select the pins that you want to remove as external pins.
2. Select **Edit** → **Cut**.

   The selected pins are no longer external pins. If you display a list of external pins, these pins do not appear in the list.

Listing External Pins

To list all currently defined external pins, enter the **getattr main extpins** command in the Command Line toolbar. A listing of all of the external pins currently defined for the macro appears in the history area, as shown following, and is written to the log file.

```
#   External Pin Name  Pin Type      Comp.Pin Location
#   -----------------  ----------    -----------------
#   Input Pins:
#                A<0>       INPUT     Q0.F1
#                A<1>       INPUT     Q0.G4
#                A<2>       INPUT     Q2.F1
#                A<3>       INPUT     Q2.G4
#                   C       CLOCK     OFL.K
#                   R       INPUT     OFL.F3
#   Output Pins:
#                 OFL      OUTPUT     OFL.XQ
#                Q<0>      OUTPUT     Q0.XQ
#                Q<1>      OUTPUT     Q0.YQ
#                Q<2>      OUTPUT     Q2.XQ
#                Q<3>      OUTPUT     Q2.YQ
#   External Pin Summary:
#      Number of inputs:   6
#      Number of outputs:  5
#      Total pin count:   11
```

Designating a Reference Component

A reference component is a component in the macro library file used as the origin when a macro instance is placed, moved, or copied.

Placement and routing of all other macro components are determined relative to this component.

If a macro library file has at least one pre-placed component, the macro will have a reference component. A macro can have only one reference component. You can specify the reference component when you create a macro library file, or you can have the system assign one automatically. If you do not designate a reference component, the component in the lower-left corner is selected by default when the macro file is saved.

When you place, move, or copy a macro instance, select a site, and then execute the appropriate command, the macro's reference component is placed in the site you designated. All other placed components in the macro are located in sites relative to the reference component.

To designate a reference component, follow this procedure.

1. Select the component you want as the reference component.
2. Select **`Edit`** → **`Set Macro Reference Comp`**

To determine which component is the reference component, enter **`getattr main refcomp`** in the Command Line Toolbar. The name of the reference component appears in the history area.

You can define a macro with unplaced components and unrouted nets. In this case, there is no reference component, and it you cannot place an instance of this library file, except by placing each macro component individually.

Adding a Macro to a Macro File

You can add a macro instance to a macro file. Use the procedure described in the "Saving a Macro Library File" section.

When you add a macro instance to a macro file, the macro instance is unbound; the components and nets in the instance are added as separate components and nets, not as macro elements. After instantiation, there is no indication that these components or nets were added as a macro.

Macro File Placement and Routing

You can place components and route the connecting nets in your macro file. When you later instantiate the macro library file in your design, the placement of the components relative to each other is maintained in the instantiated macro. Also, routing in the instantiated macro follows the routing specified in the library file. Placement and routing operations in a macro file are identical to these same operations in a design file.

When you instantiate a pre-routed macro into your design, the design can take a substantially longer time to place and route, depending on the route complexity and the number of connections in the macro nets. Xilinx recommends not adding any unnecessary routing to your library file.

Do not define a macro with CLB K pins routed together using long lines. This configuration may be impossible to route when the macro is instantiated into your design.

DRC Checks in Your Macro File

There are a number of physical DRC checks for testing your macro file. You can run these tests in the FPGA Editor. These tests also run automatically whenever you save your macro library file.

To run the macro DRC check, follow these steps.

1. Make sure nothing is selected in the Array window or in the List window. If necessary, select **Clear** in the User toolbar to deselect any objects.
2. Select **Tools** → **DRC** → **Run.**

   The macro DRC is performed (along with other DRC tests). DRC results appear in the history area.

Chapter 6

Command Line Syntax

This chapter describes the complete set of commands needed to perform all the FPGA Editor operations. It includes the following.

- “Running Commands”
- “Command Summary”
- “Command Descriptions”

Running Commands

You can run the FPGA Editor commands many different ways, including.

- Directly from the FPGA Editor Command Line toolbar
- From a command script
- As part of a command alias or hot key
- By selecting from the pull-down menus
- By selecting a command button in the User toolbar

Command Conventions

The following are FPGA Editor Command Conventions.

- Any command line field containing more than one word or containing a semicolon must be placed in quotation marks. For example, the button command creates a new button in the User toolbar. If you want to create a button called “jump in” that zooms in the display one level, you must enter the command in the form button “jump in” “zoom in.” If you entered the command in the form button jump in zoom in (without quotation

marks), the command would not work and you would receive an error message in the history area.

- Some commands call for nested quotation marks (that is, quotation marks within quotation marks). If a command requires nested quotation marks, the inner quotation marks must be of the same type (for example, a single quote and a single quote or a double quote and a double quote) and the outer quotation marks must match and be of a different type than the inner quotation marks.
- A comment is preceded by a pound sign (#). Text from the pound sign to the end of the line will be ignored; the system will not interpret the text as a command. Comments are especially useful in text files such as the fpga_editor.ini and fpga_editor_user.ini files or user script files to describe what the commands in the file are doing.
- A backslash (\) at the end of a command, followed by a carriage return, causes the command to continue on the next text line. For example, the text below is all interpreted as one command line, even though the text appears on two lines.

  ```
  setattr layer direct_connects \
  view on
  ```

  Back slashes are used to allow you to place long commands on multiple lines. Back slashes are also used to make text more readable in text files.

  Back slashes are also used to escape characters special to the FPGA Editor. The characters are.

  * (asterisk) used for wild cards

  ? (question mark) used for wild cards for a single character

  # (pound sign) used for comments

  ; (semi colon) separates multiple commands on the same command line

  “(double quote) used to quote characters to be taken literally

  ' (single quote) used to quote characters to be taken literally

  \ (back slash) if at the end of a line, continues command to the next line. Otherwise it escapes characters to be taken literally.

Example 1

To select a net whose name has an embedded space in it, use one of the following methods.

```
select net “my net”
select net my\ net
```

The back slash precedes the space character.

Example 2

To select a component with special characters in it, enter the following.

```
select comp COUNT\*
```

To select all components that start with COUNT, enter the following.

```
select comp COUNT*
```

Command Summary

The following table provides a summary of the FPGA Editor commands, including syntax and a description of the command.

Table 6-1 Command Summary

Command	Syntax	Description
add	**extpin** [*pin_name*] **net**[**-pwr** | **-gnd**] [*net_name*] **comp**[**-s** *site_name*] [**-t** *comp_type*] [*comp_name*] **macro** *macrofile_name*.[**nmc**][*macro_name*]	Adds object to design
alias	**alias** [*alias_name* [*cmdstream*]]	Assigns name to a command stream
autoplace	**autoplace** [**-all**] [**-x**] [**-l** *level* [**-t** *table_entry*]	Automatically places one or more components or macros
autoroute	**autoroute [-all [-i** *number_iterations***] [-cc** *costclean***][-dc** *delayclean***][-ec** *delaycleanif***][-x]]**	Automatically routes one or more objects
button	**button [***button_name* **[***cmdstream***]]**	Creates a new button in the User toolbar

Table 6-1 Command Summary

Command	Syntax	Description
clear	**clear**	Deselects all items currently selected
close	**close [-s|-n]**	Closes your design
copy	**copy**	Copies the logical contents of one programmable component or macro into another
create	**create design** *design_name* **[***pcffile_name***]** *arch device package speed* **create macro** *macro_name arch device package speed*	Creates a design or macro using the specified architecture, device, package, and speed
delay	**delay [-t][-min|-all]**	Runs the delay calculator on selected paths and nets in a path
delete	**delete [path** *path_name***]**	Removes selected objects from your design
drc	**drc [-all] [-err] [net|block|chip|allchecks]**	Runs the DRC (Design Rule Check), which performs a series of tests to validate nets or components
echo	**echo [***message***]**	Writes a message to the history area
editblock	**editblock**	Allows you to view the logic in a programmable block; you can edit the logic if you are in Read / Write mode
end	**end [block]**	Ends a script recording session; "end block" ends an LBE session

Table 6-1 Command Summary

Command	Syntax	Description
exec	**exec** *command_text*	Executes a system command string entered in the FPGA Editor window
exit	**exit [-s]**	Closes your design and exits the FGPA Editor
focus	**focus** *window_name* **focus {history|cmd}** **focus {next|prev|previous}**	Moves the keyboard focus to the specified window, history toolbar area, command line toolbar, previous, or next window
getattr	**getattr [main** *attrname1 attrname2.....***]** **getattr {net|comp|pin|site|layer|path}** *name attrname1 attrname2....* **getattr** *attrname1 attrname2.....*	Lists properties and constraints for a specified object
hilite	**hilite** [**-c** *color*] **hilite traceerror** [**-c** *color*] {*pcf_index* | *error_index*}	Changes the color of selected objects
layout	**layout** {**use** *name* | **save** *name*} **layout** {**cascade** | **vertical** | **horizontal**} **layout propsheets** {**diagonal** | **horizontal** | **vertical**} **layout origin** *x:0, 32000 y:0, 32000* **layout delta** *dx:0, 1000 dy:0, 1000*	Saves the arrangement of windows and toolbars using a name specified by you. To change the FPGA Editor default layout, save your new layout with the name "default."
load	**load design** [**-s**] *design_name* [*arch device package speed*] **load design** [**-s**] *design_name pcffile_name* [*arch device package speed*] **load macro** [**-s**] *macro_name* [*arch device package speed*]	Loads a design or macro into the FPGA Editor window

Table 6-1 Command Summary

Command	Syntax	Description
null	**null**	An editor command that does nothing
open	**open design** *design_name* [*pcffile_name*] **open macro** *macro_name*	Opens the specified design or macro; if a PCF file exists for the design, it is automatically opened even if it is not specified
pan	**pan center** **pan {up|down|left|right} [far]** **pan {up|down|left|right}** **[***percent_amount:1,100***]** **pan delta** *x_pos:-32000, 32000 y_pos:-32000, 32000*	Pans the Array window in a specified direction by a specified amount
pause	**pause [***nseconds:1, 1000***]**	Pauses the editor for a specified number of seconds
pick	**pick [-e][-a][-q][-k][-n][-m][-s|r]** **[-p][***x_loc:-32000,32000 y_loc:-32000,32000***][***layer_name***][-order** *order_spec***]**	Allows you to select an object in the main window by location
pipe	**pipe {input|output} create** *pipe_name* **pipe {input|output} open** *pipe_name* **pipe {input|output} close** **pipe input interval** *milliseconds***:***10, 10000* **pipe input {pause|resume}** **pipe output write** *string*	Creates input and output files that are read from and written to, respectively
place	**place**	Places a selected component or macro at a selected site
playback	**playback [-d][-r][-i][-p][-s]** *file_name***.scr**	Plays back the commands in a script file

Table 6-1 Command Summary

Command	Syntax	Description
post	**post attr [main]** **post attr {net|comp|site|pin|layer|path|macro|wire}** *name* **post {array|list|world}** **post block [comp|site|sitetype** *name***]** **post {cmd|history|standard|user|view}** **post {drc|find|new|open|macnew|macopen|addmacro|playback|probes|record|trace|tracesum|autorouteall|autoplaceall}** *arg1 arg2 .....* **post traceerr** *pcf_index:0, 32000* **post msg [-t][-c|-ok|-okcancel|-yesno|-yesnocancel][-defbutton1|-defbutton2|-defbutton3][-info|-information|-question|-exclamation|-stop]** *message* **[-newcc][***cmdstream1* **[***cmdstream2* **[***cmdstream3***]]]** **post [-m] saveas** **post [-n] {cmd|exit}**	Posts a dialog box of the specified type
probe	**probe add [***net_name***] [-pinname** *pin_name***] [-targetpins** *pin_number1 pin_number2***] [-usedpin** *pin_number***][-noroute]** **probe change [-pinname]** *net_or_pin_name attr_name1 attr_value1 attr_name2 attr_value2* **probe {route|unroute|delete|list} [-pinname]** *net_or_pin_name* **probe {route|unroute|delete|list] [-all]** **probe save** *probe_script_name*	Defines and adds probes to your design
quit!	**quit!**	Closes out the FPGA Editor without saving changes to the design file

Table 6-1 Command Summary

Command	Syntax	Description
record	**record [-c [-r]][***scriptfile_name***]**	Records commands into a script file; creates a script file that, when played back, replicates the current design or macro; and writes routing commands into the script file to generate the routes in a design
refresh	**refresh**	Redraws the main window and writes the most recent commands into the command log file
route	**route**	Routes a series of specified connections
save	**save [***design_name* **[***pcffile_name***]]** **save design [***design_name* **pcffile_name]]** **save macro [***macro_name***]**	Saves your design or macro
select	**select [-k][-id] {comp|pin|net|node|layer|path|macro|site|wire}** *name* **select [-k] route** *net_name xpos:-32000, 32000 ypos:-32000, 32000* **select [-k]** *layer_name xpos:-32000, 32000 ypos:-32000, 32000 xpos:-32000, 32000 ypos:-32000, 32000* **select [-k]** *layer_name name xpos:-32000, 32000 ypos:-32000, 32000*	Selects an object using keyboard input only
setattr	**setattr {main|find|list}** *attrname1 attrvalue1 attrname2 attrvalue2* **setattr {net|comp|site|layer|path|pin}** *name attrname1 attrvalue1 attrname2 attrvalue2* **setattr** *attrname1 attrvalue1 attrname2 attrvalue2*	Sets specified properties and constraints for a selected object

Table 6-1 Command Summary

Command	Syntax	Description
setwin	**setwin [-c]** *name attrname1 attrvalue1 attrname2 attrvalue2*	Sets window related attributes, such as position and size
swap	**swap**	Changes the placement of a selected component or macro with that of another selected component, macro, or site; also swaps two pins
trace	**trace [-r][-e][-l** *limit***]**	Displays a timing report for selected constraints in the history area; also constructs an internal table of timing information for the selected constraints
unalias	**unalias [-all]** *aliasname1* **[***aliasname2***]**	Removes a defined command alias
unbind	**unbind**	Separates macro components and nets from the macro and deletes the macro instance from the database
unbutton	**unbutton [-all]** *button_name1* **[***button_name2***]**	Removes an existing User toolbar button
unhilite	**unhilite [-all]** **unhilite traceerror** *pcf_index***|***error_index*	Removes the highlight from selected or specified objects
unload	**unload [design][***design_name***[***pcffile_name***]]** **unload [macro][***macro_name***]**	Saves your design in the main window to an external file

Table 6-1 Command Summary

Command	Syntax	Description
unplace	**unplace [-all]**	Unplaces one or more selected components or macros
unpost	**unpost [-all]** **unpost [attr] main** **unpost [attr] {net|comp|site|pin|layer|path|macro|wire}** *name* **unpost {cmd|history|standard|status|user|view}** **unpost** *window_name* **[***key***]**	Closes all dialog boxes, or a dialog box of the designated type
unroute	**unroute [-all]**	Unroutes the selected object(s)
unselect	**unselect [-all] |** **{comp|pin|net|node|layer|path|macro|site|wire}[-id]** *name*	Unselects all or selected objects in your design
zoom	**zoom {in|out} [far][@cursor]** **zoom toggle [***xpos***][***ypos***]** **zoom selection**	Zooms the Array window in or out

Command Descriptions

This section contains an alphabetical listing of the commands, command line syntax, options, abbreviations, and command line examples.

Add

Use the Add command to create new design objects or modify existing ones. All components added with this command become part of your design's database.

Syntax

add extpin [*pin_name***]**

add net [-pwr|-gnd][*net_name***]**

add comp [-s *site_name*]**[-t** *comp_type*]**[***comp_name*]

add macro *macrofile_name.*[**nmc**][*macro_name*]

Options

extpin	External macro pin
macrofile_name	Name of the library file for the macro you are adding to your design
macro_name	Name of the macro within your design

Example

To add a component at site ED, enter the following.

```
select site ED
add
```

To create a new net, enter the following.

```
select pin ED.Y
select pin FE.A
add
```

To add two new net pins to net DA1, enter the following.

```
select pin AD.Y
select pin CE.A
select net DA1
add
```

Alias

Use the Alias command to assign a name to a command stream. You can then enter the alias name to perform the assigned commands. This is useful for abbreviating or renaming existing commands. If the command stream is omitted, the command stream associated with the named aliases is displayed in the history area.

You can also use the Alias command to define “hot keys” or characters you can enter when the Array window has the keyboard focus.

Use brackets around a character, control key combination, or function key combination to specify the hot key name as shown in the following examples.

```
alias [z] "zoom in"
alias [Ctrl+z] "zoom in"
alias [F3] "zoom in"
alias [Shift+F3] "zoom out"
alias [Ctrl+Shift+F3] "zoom out far"
```

Note: Some control and function keys are reserved, and cannot be given a new value with the Alias command. An error message is displayed if you try to use one of the reserved keys.

You can also use the Alias command to assign commands to mouse clicks as shown in the following example.

```
alias [Left Click] "pick -s"
```

Other possible mouse clicks are Right Click, Middle Click, Left Double Click, Middle Double Click, or Right Double Click. You can also use the Shift and Control keys with mouse clicks.

Syntax

alias [*alias_name* [*cmdstream*]]

Options

alias_name	Name of the alias to be added
cmdstream	Command(s) run when alias is entered

Example

To create a command called two_ in that zooms in two zoom levels and deselects any selected objects, enter the following.

```
alias two_in "zoom in;zoom in;clear"
```

To find out what commands are associated with the two_in alias, enter the following.

```
alias two_in
```

To display a list of available aliases and associated commands in the history area, enter the following.

```
alias
```

Autoplace

Use the Autoplace command to automatically place selected components or all unplaced components in your design.

Syntax

autoplace [-all][-x][-l *level* **[-t** *table_entry***]]**

Options

–all	Autoplaces all components
–x	Disables timing-driven placement
–l *level*	Specifies the effort level for the design
–t *table_entry*	Specifies how to start placement at the specified cost table

Example

- To place the LB1 component, follow these steps.
  - Enter **select comp LB1**
  - Enter **autoplace**
- To place all unplaced components in your design, enter the following.

  autoplace -all

Autoroute

Use the Autoroute command to automatically route the connection between specified objects.

Syntax

autoroute [-all [-i *number_iterations*]
[-cc *costclean*]**[-dc** *delayclean*]**[-ec** *delaycleanif*]**[-x]]**

Options

–all	Autoroutes all signals
–x	Disables timing-driven routing
–i *number_iterations*	Specifies the number of iterations performed by the router; you can only use this option with the –all option
–cc *costclean*	Specifies the number of cost-based cleanup iterations
–dc *delayclean*	Specifies the number of delay-based cleanup iterations
–ec *delaycleanif*	Specifies the number of delay-based cleanup iterations to be run if the design was successfully routed

Example

To automatically route every net connected to pins on components LB1 and LB2, enter the following.

```
select comp LB1
select comp LB2
autoroute
```

To automatically route net DH1, enter the following.

```
select net DH1
autoroute
```

To automatically route your entire design using twelve iterations of the router and one cost-based cleanup pass, enter the following.

```
autoroute -all -i 12
```

Button

Use the Button command to create a new button in the User toolbar.

Syntax

button [*button_name* **[***cmdstream***]]**

Options

button_name	Name of the button you want to add
cmdstream	Specifies the commands that are executed when this button is pressed

Example

To create a new button in the User toolbar with the name “two in” that zooms in two zoom levels and deselects all selected objects, enter the following.

```
button “two in” “zoom in;zoom in;clear”
```

To list the commands associated with the “two in” button, enter the following.

```
button “two in”
```

To list the commands associated with all User toolbar buttons, enter the following.

```
button
```

Clear

Use the Clear command to deselect all items currently selected.

Syntax

```
clear
```

Close

Use the Close command to close your design.

Syntax

close [-s|-n]

Options

-s	Saves your design before closing it
-n	Specifies that you do not want to save your design before closing it

Create

Use the Create command to create a design or macro using the specified architecture, device, package, and speed.

Syntax

create design *design_name* [*pcffile_name*] *arch device package speed*

create macro *macro_name arch device package speed*

Options

pcffile_name	Specifies the physical constraints file

Delay

Use the Delay command to compute the delay for selected nets or paths. For pins with multiple paths, the Delay command computes the maximum delay path as the default. To determine the delay for a net, select the net and use the Delay command without any options.

Syntax

delay [-t][-min|-all]

Options

Note: The following options are for paths only.

-t	Lists the total delay for the selected path (not the constituent parts)
-min	Lists the path with the smallest delay (when there are multiple paths)
-all	Lists the delays for all paths between two selected pins

Example

To list the delays for all paths between two pins, select the pins and enter the following.

delay -all

To list the path with the smallest delay (when there are multiple paths between two pins), select the pins and enter.

delay -min

To display the driver-to-load delays for a specific net, select the net name from the List window and click the Delay button in the User toolbar.

Delete

Use the Delete command to remove selected objects from your design.

Syntax

delete [**path** *path_name*]

Options

path_name	Specifies the path you want to delete

Example

To delete component DMA1 from your design, enter the following.

```
select comp DMA1
delete
```

To select and view net HRST and then delete it from your design, enter the following.

```
select net HRST
delete
```

To clear all current selections and delete the CE.RD and CF.RD net pins from their associated net, enter the following.

```
clear
select pin CE.RD
select pin CF.RD
delete
```

DRC

Use the DRC command to run a design rule check on objects in your design.

Syntax

```
drc [-all][-err][net|block|chip|allchecks]
```

Options

-all	Runs all DRC checks on all nets and blocks
-err	Reports errors only; does not report warnings
net	Runs net check only
block	Runs block check only
chip	Runs chip check only
allchecks	Runs net, block, and chip checks

Echo

Use the Echo command to write a message to the history toolbar area.

Syntax

echo [*message***]**

Editblock

Use the Editblock command to modify logic blocks in the Block window.

Syntax

editblock

End

Use the End command to end a script recording session, end a script playback, or close the logic block editor.

Syntax

end [block]

Example

To terminate a script recording session, enter the following.

end

To close the logic block editor, enter the following.

end block

Exec

Use the Exec command to execute a UNIX or Windows command.

Syntax

exec [**-g**] *command_text*

Options

-g Spawns a GUI (graphical user interface) program. The FPGA Editor does not wait for the GUI program to terminate before returning control back to you. It does not collect the output of GUI programs.

Example

To save your design to a different filename and then list the contents of the directory where this new file exists, enter the following.

```
unload design adder.ncd
exec “dir /home/designs”
```

Exit

Use the Exit command to close your design and exit the FGPA Editor. You are prompted to save any unsaved changes.

Syntax

```
exit [-s]
```

Options

-s Causes FPGA Editor to automatically save any changes without prompting you before exiting

Focus

Use the Focus command to move the keyboard focus to the specified window, history toolbar area, command line toolbar, previous, or next window. Xilinx recommends assigning this command to a “hot key.” See the “Alias” section for more information on using the Alias command, refer to the “Customizing with Command Aliases” section

of the “Customizing the FPGA Editor” chapter for information on hot keys.

Syntax

focus *window_name*

focus {**history** | **cmd**}

focus {**next** | **prev** | **previous**}

Options

window_name	Moves keyboard focus to specified window
history	Moves keyboard focus to history toolbar area
cmd	Moves keyboard focus to command line toolbar
next	Moves keyboard focus to next window
prev	Moves keyboard focus to previous window

Getattr

Use the Getattr command to list properties for a specified object.

Syntax

getattr [**main** *attrname1 attrname2*.....]

getattr {**net** | **comp** | **pin** | **site** | **layer** | **path**} *name attrname1 attrname2*....

getattr *attrname1 attrname2*.....

Options

main	Displays all or specified properties in the history area for your design
name	Specifies the name of selected object
attrname	Specifies valid attribute for the selected object

Example

To list the setting of the main window automatic routing option, enter the following.

```
getattr main auto_route
```

To list the properties for a selected net, enter the following.

```
getattr
```

This command list the priority and the locked attribute for the Q1 net.

```
getattr net Q1 prioritize lock
```

This command lists the values for the locate constraint.

getattr comp *comp_name* **locate**

The following table lists the valid attributes for objects that can have attributes. The table also lists the name expected for a layer when you specify a layer as the object type.

Note: You can use dashes instead of underscores in the attribute name.

Table 6-2 Object Attributes

Object	Name	Attribute Name
Main	Not Applicable	design_name program_version speed edit_mode flush_rate auto_deselect auto_hilite auto_post stub_trim auto_route enhanced_routing delay_based disable_draw lock_routing lock_placement penalize_tilde allnets_maxdelay clknets_period clknets_maxskew allpaths_maxdelay pattern_matching design_manager_mode design_manager_ncd_file probe_auto_pin_count probe_config_string array_view_params pan_style show_errors_in_box extpins (macros only) refcomp (macros only)
	clknets_period[1]	

Table 6-2 Object Attributes

Object	Name	Attribute Name
net	net_name	name route_status number_of_pins pin_list lock block period period prioritize
comp	comp_name	name type designator lock locate paths offset offset_comp1 (I/O comp only) offset_comp2 (I/O comp only) offset_order (I/O comp only) offset_direction (I/O comp only) offset_time (I/O comp only) base config
site	site_name	name prohibit
pin	pin_name	name pin_comp pin_site type pin_net pin_comp
layer	components, hilite, local lines, long lines, pinwires, pips, ratsnests, routes, select, sites, switch boxes, text	name type view color

Table 6-2 Object Attributes

Object	Name	Attribute Name
path	path name	name elements block maxdelay
find	Not Applicable	type name auto clear auto pan
macro	macro name	name libfile status refcomp extpins lock locate paths

[1] Syntax for listing the global period attribute is:
`getattr main clknets_period`
When you use the Getattr command to list the period attribute for a period with a duty cycle, it is displayed in the history area as in these examples:
clknets_period = 50.00
clknets_period = 50.00:low:10
clknets_period = 50.00:high:10
Also see Note 1 under the setattr command.

Hilite

Use the Hilite command to change the color of selected objects.

Syntax

`hilite [-c` *color*`]`

`hilite traceerror [-c color] {`*pcf_index*`|`*error_index*`}`**

Options

-c	Use –c *color* to change the color of a selected object. Valid colors are black, magenta, dark green, blue, yellow, dark cyan, green, white, dark red, cyan, grey, dark magenta, red, dark blue, and olive.
traceerror	Indicates an error discovered by the Trace command
pcf_index	Specifies the position of the constraint within the constraint file and the List window. For example, the first constraint listed is number 0. Value can be between 0 and 32,000.
error_index	Specifies the position of the error in the Trace Error dialog box. The first error listed is number 0. Value can be between 0 and 32,000.

Example

To change the color of a selected object to yellow, enter the following.

```
hilite -c yellow
```

Layout

Use the Layout command to save the arrangement of windows and toolbars using a name specified by you. To change the FPGA Editor default layout, save your new layout with the name “default.” Layouts are saved in the system registry file and are available each time you invoke the FPGA Editor. You can define and save several layouts, and then use the Button command to create buttons associated with the layouts. Use the buttons to quickly change to a different window arrangement. See the “Button” section for more information.

Syntax

layout {**use** *name* | **save** *name*}

layout {**cascade** | **vertical** | **horizontal**}

layout propsheets {**diagonal** | **horizontal** | **vertical**}

`layout origin` *x:0, 32000 y:0, 32000*

layout delta *dx:0, 1000 dy:0, 1000*

Options

use	Uses specified layout for windows and toolbars
save	Saves arrangement of windows and toolbars using the specified name
cascade, vertical, horizontal	Arranges FPGA Editor windows horizontally, vertically, or cascading
propsheets	Arranges property sheets in a cascading diagonal, horizontal, or vertical style
origin	Sets the point, in screen coordinates, for cascading dialog boxes. Point 0,0 is the upper left corner of the FPGA Editor window. These values are saved for future editing sessions.
delta	Sets the delta x and y values for cascading property sheets. These values are saved for future editing sessions.

Example

To save the arrangement of windows and toolbars with the name "good_layout", enter the following.

```
layout save good_layout
```

To apply a saved layout of windows and toolbars named "good_layout", enter the following.

```
layout use good_layout
```

To arrange the FPGA Editor windows horizontally, enter the following.

```
layout horizontal
```

Null

Use the Null command as a placeholder for a command to be specified later.

Syntax

null

Open

Use the Open command to open the specified design or macro. If a PCF file exists for the design, it is automatically opened even if it is not specified.

Syntax

open design *design_name* **[***pcffile_name***]**

open macro *macro_name*

Options

pcffile_name	Physical constraints file

Pan

Use the Pan command to move the Array window in a specified direction by a specified amount. If you have more than one array view open, the Pan command applies to the last one activated.

Syntax

pan center

pan {up|down|left|right} [far]

pan {up|down|left|right} [*percent_amount:1,100***]**

pan delta *x_pos:-32000, 32000 y_pos:-32000, 32000*

Example

To pan up one window height, enter the following.

pan up

To pan left one window width, enter the following.

pan left

To pan up to the extreme top edge of the Array window, enter the following.

```
pan up far
```

To pan right 50% of a window width, enter the following.

```
pan right 50
```

To pan the display left –1002 units and up 568 units, enter the following.

```
pan delta -1002 568
```

To center the window about the current cursor position, enter the following.

```
pan center
```

Pause

Use the Pause command to stop the FPGA Editor for a specified period of time.

Syntax

pause [*nseconds:1, 1000***]**

Options

nseconds	Number of nano seconds to pause; must be between 1 and 1000

Example

To pause the editor for 15 seconds, enter the following.

```
pause 15
```

Pick

Use the Pick command to select an object in the main window by location. If a location is not specified, the object under the cursor is selected. The pick command is most useful when it is assigned to a hot key or a mouse button.

Syntax

Note: The -order option and the -n, -m, -s, and -p options are mutually exclusive. If the -order option is used, the -n, -m, -s, and -p options are ignored.

pick [-e][-a][-q][-k][-n][-m][-s|r][-p][*x_loc:-32000,32000 y_loc:-32000,32000***][***layer_name***][-order** *order_spec***]**

Options

-e	Generates an editblock command (starts the logic block editor) if a component is found at the specified x, y coordinates
-a	Picks in all layers, whether they are visible or invisible (default is to pick only visible objects)
-q	Lists the name and other information of the object the cursor is currently over into the history area. It does this without selecting the object.
-k	Selects an item without using the mouse
-n	Picks a component if the pick location is over a component pin or picks a site if the pick location is over a site. Forces the FPGA Editor to pick the site or component rather than the pin.
-m	Selects a macro if a macro component is found at the specified x, y coordinates. Otherwise selects a regular pick.
-s	Selects a net if a route segment is found at the specified x, y coordinates
-p	Selects a pin if the pick location is over a pin
x_loc, y_loc	Represent absolute screen coordinates. For applicable commands, these coordinates appear in the log file. All x-y values must be between ± 32000. If coordinates are not specified, the default is to use the current mouse cursor position.

layer_name	Specific layer to pick in. If layer name is not specified, all layers are picked. Layer name can be components, hilite, links, local lines, long lines, pinwires, ratsnests, routes, select, sites, text.
-order	Controls the order in which objects are considered for picking.
order_spec	Specifies the order of objects for picking

Example

Enter the following to select the object the cursor is over.

```
pick
```

Enter the following to select the object at coordinates 12400 234.

```
pick 12400 234
```

Enter the following to select the site the cursor is over.

```
pick sites
```

Use the following to select a site when the site layer is not visible.

```
pick -a sites
```

Enter the following to select a route path. If *number* is less than zero, the route path is an uphill path; if *number* is greater than zero, the route path is a downhill path.

pick -order rpath *number*

Enter the following to select objects in the specified order.

```
pick -order comp:site:macro:comppin:sitepin:route:net
```

comp	Specifies a component
macro	Specifies a macro
site	Specifies a site
sitepin, comppin, pin	Specifies a site pin, component pin, or a pin
rthru	Specifies a route-through
net	Specifies a net

route	Specifies a route
rpath	Specifies a route path
etc	Continues pick in default order
end	Stops pick operation

Pipe

Note: The Pipe command is not available on Windows 95 platforms.

Use the Pipe command to create input and output files that are read from and written to, respectively. This command allows you to send commands to the FPGA Editor from another program, and from the FPGA Editor to another program.

On UNIX platforms, a pipe file remains in the file system and does not have to be re-created if you want to use it again after closing it. On NT platforms, the pipe file does not remain in the file system; you must re-create the pipe to use it again after closing it.

Syntax

pipe {input|output} create *pipe_name*

pipe {input|output} open *pipe_name*

pipe {input|output} close

pipe input interval *milliseconds*:*10, 10000*

pipe input {pause|resume}

pipe output write *string*

Options

pipe_name	Specifies the name of the input or output pipe
interval	Specifies in milliseconds how often the input pipe is read from; the default is 250 and the range is 10-10000
pause / resume	Pauses or resumes reading the input pipe
write	Writes to the output pipe

Example

To create an input pipe named pipe_organ, enter the following.

```
pipe input create pipe_organ
```

To set the interval for an input pipe to 100 milliseconds, enter the following.

```
pipe input interval 100
```

Place

Use the Place command to place a component at a selected site. If the autorouting attribute is set to True, any nets connected to the component are routed.

Syntax

```
place
```

Example

To place a logic block, follow these steps.

1. Display the unplaced components list in the List window.
2. Select a component from the list.
3. Select a vacant site in the Array window.
4. Enter the following to place the component.

```
place
```

Playback

Plays back the commands in a script file.

Syntax

playback [-d][-r][-i][-p][-s] *file_name*.**scr**

Options

-d	Inhibits the redrawing of windows during script playback
-r	Ignores the editblock, getattr, null, pan, pause, post, and zoom commands during playback. Use this option to recover from an aborted FPGA Editor session.
-i	Runs the unalias -all and unbutton -all commands before script playback
-p	Inhibits the post command from opening any windows during script playback
-s	Displays each command in the history area as it is performed
file_name	Specifies the script file name

Example

To play back the myroute.scr script file, and display each command in the history area as it is being performed, enter the following.

```
playback -s myroute.scr
```

Post

Use the Post command to display a dialog box, window, or toolbar of the specified type.

Syntax

post attr [main]

post attr {net|comp|site|pin|layer|path|macro|wire} *name*

post {array|list|world}

post block [comp|site|sitetype *name*]

post {cmd|history|standard|user|view}

post {drc|find|new|open|macnew|macopen|addmacro|playback|probes|record|trace|tracesum|autorouteall|autoplaceall} *arg1 arg2 .....*

post traceerr *pcf_index:0, 32000*

post msg [-t][-c|-ok|-okcancel|-yesno|-yesnocancel]
[-defbutton1|-defbutton2|-defbutton3]
[-info|-information|-question|-exclamation|-stop]
message **[-newcc][***cmdstream1* **[***cmdstream2* **[***cmdstream3***]]]**

post [-m] saveas

post [-n] {cmd|exit}

Options

The allowable dialog box, property sheet, window, or toolbar name and key entries are listed in the following table.

name	Posts the dialog box for the object specified with this name
array	Creates a new instance of the Array window
list	Creates a new instance of the List window
world	Creates a new instance of the World window
block	Creates a new instance of the Block window for a selected component or site
cmd,history,standard, user, view	Posts the Command, History, Standard, User, or Layer Visibility toolbar
-m	Posts the Save As Macro dialog box
-n exit	Posts the Exit dialog box if you have unsaved changes. If you have not made any changes to your design, FPGA Editor terminates without posting the dialog box
-n cmd	Posts the command dialog box without buttons (OK, Apply, Cancel). Once a command is entered and the Return key is pressed, the command is executed and the command line dialog box is unposted.
pcf_index	Specifies the position of the constraint within the constraint file and the List window. For example, the first constraint listed is number 0. Value can be between 0 and 32,000.
msg	Specifies the message you enter with the post msg command.

cmd_stream Used with the post msg command to specify one of three optional command streams. The first is executed if the first button is pressed, the second when the second button is pressed, and so on.

The allowable dialog box, property sheet, or toolbar entries are described in the following table.

Table 6-3 Post Command Options

Dialog Box	Description
addmacro	Posts the Add Macro dialog box, which can be used to add a macro instance.
attr	Posts a property sheet for selected objects.
autoplaceall	Posts the Autoplace All Components dialog box, which allows you to select options when you autoplace your entire design.
autorouteall	Posts the Autoroute All Nets dialog box, which allows you to select options when you autoroute your entire design.
cmd	Posts the Command Line toolbar, which allows you to enter and execute FPGA Editor commands.
drc	Posts the DRC dialog box, which allows you to run a DRC (Design Rule Check) on selected nets, logic blocks.
exit	Posts the Exit dialog box, which allows you to close the main window and end your FPGA Editor session. If you have not made any changes since you last saved the design, the window will close without posting the Exit dialog box.
find	Posts the Find dialog box, which allows you to find a specified object.
list	Posts the List window, which displays a list of component, net, or layer names used in your design.
macnew	Posts the New Macro dialog box, which can be used to create a new macro.
macopen	Posts the Open Macro dialog box, which can be used to open an existing macro.

Table 6-3 Post Command Options

Dialog Box	Description
msg	Posts a Message dialog box containing text that you specify. The default message box includes an Ok button. Use -c or -okcancel to add a Cancel button; use -yesno to add a Yes and No button. Use -defbutton1, 2, or 3 to specify which button is the default button. Use -info, -exclamation, - stop to specify the type of icon that appears in the message box. Use \n with the message parameter to specify a new line. Use -newcc to execute the command stream in a new command context. Do not use this option if one of the command streams is "end."
new	Posts the New Design dialog box to create a new design.
open	Posts the Open Design dialog box to open an existing design.
playback	Posts the Script Playback dialog box, which allows you to play back a selected command script file.
record	Posts the Script dialog box, which allows you to record a command script. Optionally creates a script that, when played back, replicates the current design, macro, or routing.
saveas	Posts the Save As dialog box to save the design in the main window under a different name.
trace	Posts the TRACE dialog box.
tracesum	Posts the TRACE summary dialog box.
traceerr	Posts the TRACE Error dialog box; you must include a pcf_index value.
view	Posts the Layer Visibility toolbar, which allows you to control which objects appear in the Array window.

Table 6-4 Property Sheet Posted

Object Type	Name	Property Sheet Posted
main	N/A	Main Window Properties
net	net name	Net Properties
comp	comp name	Component Properties
site	site name	Site Properties

Table 6-4 Property Sheet Posted

Object Type	Name	Property Sheet Posted
pin	pin name	Pin Properties
layer	layer name	Layer Properties
path	path name	Path Properties
macro	macro name	Macro Properties

Example

Use this command to post the Main Properties property sheet.

```
post attr main
```

If there are no objects selected in your design, you can enter the following command to post the Main Properties property sheet.

```
post attr
```

To post the Net Properties property sheet for a net selected in the List window, enter.

```
post attr
```

To post the Net Properties property sheet for the Q1 net, enter.

```
post attr net Q1
```

Use this command to post a dialog box with the specified message and then post the Exit dialog box.

```
post msg “Warning: You've done something wrong!” “post exit”
```

Probe

Use the Probe command to define and add a probe to your design.

Syntax

probe add [*net_name***] [-pinname** *pin_name***] [-targetpins** *pin_number1 pin_number2***] [-usedpin** *pin_number***][-noroute]**

probe change [-pinname] *net_or_pin_name attr_name1 attr_value1 attr_name2 attr_value2*

probe {route|unroute|delete|list} [-pinname] *net_or_pin_name*

probe {route|unroute|delete|list] [-all]

probe save *probe_script_name*

Options

pinname	Specifies the IOB name; if not specified, the net name is used with a PROBE_ prefix
targetpins	Specifies the list of sites to try when routing the probe
usedpin	Route the probe to the specified pin
noroute	Probe is not routed

Example

probe add DATA7 -targetpins P121

probe add DATA6 -pinname C2.G1 -targetpins P122

Quit!

Use the Quit! command to exit the FPGA Editor without saving your design changes. You will not be prompted to save any design changes.

Syntax

quit!

Record

Use the Record command to record a series of commands into a script file. You can also use this command to create a script file that, when played back, replicates the current design or macro.

Syntax

record [-r][*scriptfile_name***]**

Options

-r	Writes routing commands into the script file
scriptfile_name	Specifies the script file name; if a file name is not specified, *design_name*.scr is used

Refresh

Use the Refresh command to redraw the main window and write the most recent commands into the command log file.

Syntax

```
refresh
```

Route

Use the Route command to route a series of specified connections.

Syntax

```
route
```

Example

To route a signal between Pin Y on LB1 and Pin O on LB2, follow these steps. Use the following figure as reference.

1. Use the Select command to select pin Y on LB1, local line C, local line I, and pin O on LB2.
2. Enter the following command.

   ```
   route
   ```

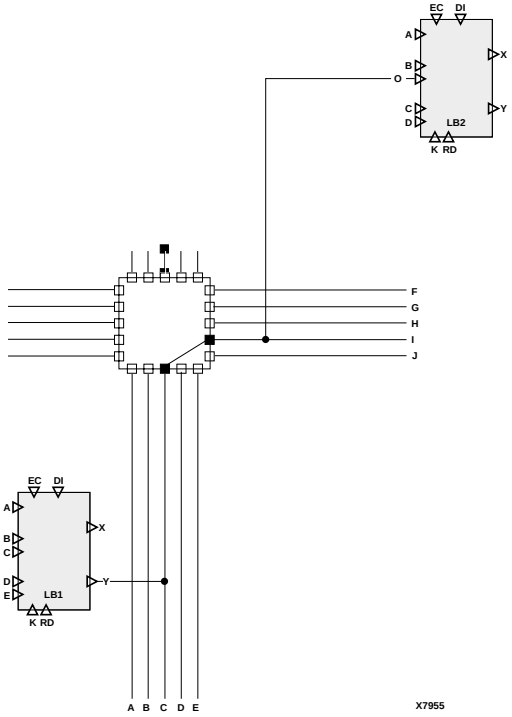


Figure 6-1 Routing Example

Save

Use the Save command to save your design or macro.

Syntax

save [*design_name* **[***pcffile_name***]]**

save design [*design_name pcffile_name***]]**

save macro [*macro_name***]**

Select

Use the Select command to select an object without using the mouse.

Syntax

select [-k][-id]{comp|pin|net|node|layer|path|macro|site|wire} *name*

select [-k] route *net_name xpos:-32000, 32000 ypos:-32000, 32000*

select [-k] *layer_name xpos:-32000, 32000 ypos:-32000, 32000 xpos:-32000, 32000 ypos:-32000, 32000*

select [-k] *layer_name name xpos:-32000, 32000 ypos:-32000, 32000*

Options

-k	Maintains the selection of an object that is already selected. If the -k option is not used, a previously selected object is unselected with the Select command.
name	Specifies the name of the object you want to select
layer_name	Specifies the name of the graphical layer you want to select
xpos, ypos	Specifies screen coordinates
-id	Specifies the id number of the component you want to select

Example

To select the LB1 component, enter the following.

```
select comp LB1
```

To select the site layer, enter the following.

```
select layer sites
```

Setattr

Use the Setattr command to set attributes for a specified object. You can specify more than one attribute name/value pair in a single command. Non-constraint attributes with two opposing values (for example, TRUE/FALSE) can be toggled with the TOGGLE option.

Syntax

Note: Attribute names and values are case insensitive, and dashes and underscores are interpreted as the same character.

`setattr` {**`main`** | **`find`** | **`list`**} *attrname1 attrvalue1 attrname2 attrvalue2*

`setattr` {**`net`** | **`comp`** | **`site`** | **`layer`** | **`path`** | **`pin`**} *name attrname1 attrvalue1 attrname2 attrvalue2*

`setattr` *attrname1 attrvalue1 attrname2 attrvalue2*

Options

name	Specifies the name of the object
attrname	Specifies the valid attribute name for the specified object
attrvalue	Specifies the appropriate value for the attribute name specified

Table 6-5 Attributes

Object	Name	Attribute Name	Value Expected
main	N/A	speed	Enter **`post new`** at the command line to display the New dialog box. Select the Part button to view the speed grades for a device.
		clknets_period	
		temperature	
		voltage	
		process	
		edit_mode	read-only | read-write | no-logic-changes
		flush_rate	*number_of_commands*

Table 6-5 Attributes

Object	Name	Attribute Name	Value Expected
		auto_deselect	true | false | toggle
		auto_hilite	true | false | toggle
		auto_post	true | false | toggle
		stub_trim	true | false | toggle
		auto_route	true | false | toggle
		enhanced_routing	true | false | toggle
		delay_based	true | false | toggle
		disable_draw	true | false | toggle
		lock_routing	on | off
		penalize_tilde	percentage | off
		allnets_maxdelay	nanoseconds | off
		clknets_period	nanoseconds | off
		clknets_maxskew	nanoseconds | off
		allpaths_maxdelay	nanoseconds | off
		asyncpaths_block	on | off
find	N/A	type	comp | net | site | pin
		name	text string
		auto_clear	true | false | toggle
		auto_pan	true | false | toggle
net	net_name	name	text string
		route_status	routed | unrouted
		number_of_pins	number
		pin_list	list
		lock	on | off
		block	on | off
		prioritize	0-100 | off
		maxdelay	nanoseconds | off
		maxskew	nanoseconds | off
		period	nanoseconds | off

Table 6-5 Attributes

Object	Name	Attribute Name	Value Expected
		paths	path name(s)
comp	comp_name	name	text string
		type	type name
		designator	site name
		lock	on | off
		locate	on | off
		paths	path names
		offset	on | off
		offset comp1	text string
		offset comp2	text string
		offset order	before | after
		offset direction	in | out
		offset time	nanoseconds
		base	F | FG | FGM | IO
		config	text string
		carry (XC4000 only) feqn geqn heqn (XC4000 only)	 text string text string text string
layer	layer name (for example, components, hilite, and so forth.)	color	black | blue | green | cyan | red | magenta | yellow | white | grey | dark blue | dark green | dark cyan | dark red | dark magenta | olive
		view	on | off | toggle
		block	on | off
		lock	on | off
		maxskew	nanoseconds | off

Table 6-5 Attributes

Object	Name	Attribute Name	Value Expected
		prioritize	1-100 | off
macro	*macro_name*	name lock locate	*text_string* on | off on | off

Note: Enter the following to set the global period attributes.

`setattr main clknets_period` *period* [**`:low`** | **`high:`** *duration*]

Period	Specifies the total period
low | high	Specifies whether the first pulse is low or high
duration	Specifies the duration of the first pulse in nanoseconds

Example

Use the following command to generate the PERIOD 50.000000 nS constraint.

```
setattr main clknets_period 50
```

Use the following command to generate the PERIOD 50.000000 nS LOW 10.000000 ns constraint.

```
setattr main clknets_period 50:low:10
```

Use the following syntax to set the period attribute for a selected net.

```
setattr period [: low | high : duration]
```

where:

- Period is the total period
- Low | high specifies whether the first pulse is low or high
- Duration is the duration of the first pulse

For example (assuming net “$1--T5” is selected), the following commands generate the following constraints.

setattr period 50

PERIOD NET “$1--T5” 50.000000 ns ;

setattr period 50:low:10

PERIOD NET “$1--T5” 50.000000 ns LOW 10.000000 ns ;

To set the main window Automatic Routing Option attribute to true, enter the following.

```
setattr main auto_route TRUE
```

To toggle the value for the main window Automatic Routing Option attribute, enter the following.

```
setattr main auto_route TOGGLE
```

The following command sets the priority to 3 and the locked attribute to FALSE for the net Q1.

```
setattr net Q1 priority 3 lock OFF
```

The following command sets the locked attribute to true for the component selected.

```
setattr lock ON
```

The following command sets the color and visibility attributes for the component layer.

```
setattr layer components color blue view on
```

Setwin

Use the Setwin command to set window related attributes, such as position and size.

Syntax

setwin [**-c**] *name attrname1 attrvalue1 attrname2 attrvalue2*

Options

-c	Use this option to create a new window
name	Specifies the name of a window as it appears in the window’s title bar

attrname	Specifies the valid attribute name for the window (x, y, w, or h)
attrvalue	Specifies the appropriate value for the specified attribute; for x, y, w, or h it must be between 0 and 100, inclusive. This is a percentage of the client or work space area (the main window area that includes the Array, List, and World windows) width or height.

Example

To move the List1 window to the left hand side of the client (or work space) area, enter the following.

```
setwin list1 x 0 y 0 w 50 h 100
```

To create an Array2 window on the right hand side of the client (or work space) area, enter the following.

```
setwin -c array2 x 50 y 0 w 50 h 100
```

Swap

Use the Swap command to change the placement of a selected component with that of another selected component. You can also use this command to swap two net pins on a component.

Syntax

```
swap
```

Example

- To move component LB1 to site CC, follow these steps.
  - Select LB1 and select site CC.
  - Enter the Swap command.

    ```
    swap
    ```
- To swap the placement of comp1 and comp2, perform the following steps.
  - Select comp1 and comp2.
  - Enter the Swap command.

swap

Trace

Use the Trace command to view a timing report in the history area for constraints you select in the List window.

Syntax

trace [-r][-e][-l *limit***]**

Options

-r	Prevents a timing report from being written to the history area
-e	Generates a timing error report for the selected constraints. If -e is not specified, a verbose report is issued
-l	Specifies a limit to the number of errors or verbose output for each selected constraint. Default is 5. The limit is from 0 to 32000

Example

The following command directs TRACE to do timing analysis on selected constraints and generate a timing error report. It limits the number of errors reported for each selected constraint.

trace -e -l 5

Unalias

Use the Unalias command to remove a defined command alias. You can use the Unalias command on more than one alias at a time.

Syntax

unalias [-all] *aliasname1* **[***aliasname2***]**

Options

-all	Removes all aliases
aliasname	Specifies the name of an existing alias

Example

The following command removes the two_in alias.

```
unalias two_in
```

Unbind

Use this command to separate macro components and nets from the selected macro.

Syntax

```
select macro foo
unbind
```

Unbutton

Use the Unbutton command to remove an existing User toolbar button. You can use the Unbutton command to remove more than one button at a time.

Syntax

unbutton [-all] *button_name1* **[***button_name2***]**

Options

-all	Removes all buttons
button_name	Specifies the name of the button to be removed

Unhilite

Use the Unhilite command to remove highlighting from currently selected objects or from objects specified in the Command Line toolbar.

Syntax

unhilite [-all]

unhilite traceerror *pcf_index error_index*

Options

-all	Specifies that all highlighted objects are to be unhighlighted
traceerror	Indicates an error discovered by TRACE
pcf_index	Position of the constraint within the constraint file and the List window. For example, the first constraint listed is number 0, and so on
error_index	Position of the error in the TRACE Error dialog box. The first error listed is number 0, and so on

Example

The following command removes highlighting from all highlighted objects.

unhilite -all

The following command removes highlighting from pin HG.K.

unhilite pin HG.K

Unplace

Use the Unplace command to remove some or all placed components and macros from their sites. If components are connected to routed nets, these nets are unrouted from the components before they are unplaced.

Syntax

unplace [**-all**]

Options

-all	Unplaces all placed components and macros except those that are locked

Example

To unplace comp1, enter the following.

```
unplace comp1
```

Unpost

Use the Unpost command to close all or some dialog boxes, property sheets, windows, or toolbars.

Syntax

unpost [**-all**]

unpost [**attr**] **main**

unpost [**attr**] {**net** | **comp** | **site** | **pin** | **layer** | **path** | **macro** | **wire**} *name*

unpost {**cmd** | **history** | **standard** | **status** | **user** | **view**}

unpost *window_name* [*key*]

Options

The allowable dialog box, property sheet, window, or toolbar name and key entries are listed in the following table.

Table 6-6 Unpost Command Options

Dialog Box Name	Description
addmacro	Closes and cancels the Add Macro dialog box.
autoplcp | autoplaceall	Closes and cancels the Autoplace All Components dialog box.

Table 6-6 Unpost Command Options

Dialog Box Name	Description
autortcp | autorouteall	Closes and cancels the Autoroute All Nets dialog box.
cmd	Closes and cancels the Command Line toolbar.
comp *comp_name*	Closes and cancels the Component Properties property sheet.
drcform | drc	Closes and cancels the DRC dialog box.
find	Closes and cancels the Find dialog box.
open	Closes and cancels the Open Design dialog box.
playback	Closes and cancels the Script Playback dialog box.
record	Closes and cancels the Script dialog box.
save	Closes and cancels the Save As dialog box.
layer *layer_name*	Closes and cancels the Layer Attributes dialog box.
macnew	Closes and cancels the New Macro dialog box.
macopen	Closes and cancels the Open Macro dialog box.
macro	Closes and cancels the Macro Properties property sheet.
macsave	Closes and cancels the Save As macro dialog box.
main	Closes and cancels the Main Window constraints dialog box.
net *net_name*	Closes and cancels the Net Properties property sheet.
new	Closes and cancels the New Design dialog box.
path *path_name*	Closes and cancels the Path Properties property sheet.
pin *pin_name*	Closes and cancels the Pin Properties property sheet; *pin_name* is site *pinname*
site *site_name*	Closes and cancels the Site Properties property sheet.
trace	Closes and cancels the TRACE dialog box.
tracesum	Closes and cancels the TRACE Summary dialog box.
traceerr	Closes and cancels all TRACE error dialog boxes.
view	Closes and cancels the Layer Visibility toolbar.
wire	Closes and cancels all Wire Properties property sheets.

The available selections for layer name are components, hilite, local lines, long lines, pinwires, pips, ratsnests, routes, select, sites, switch boxes, text.

The *variable_name* identifies the specific object within the layer.

Example

The following command closes the Main Properties property sheet.

```
unpost main
```

The following command closes the Component Properties property sheet for LB12.

```
unpost comp LB12
```

The following command closes all Component Properties property sheets.

```
unpost comp
```

The following command closes all dialog boxes.

```
unpost -all
```

Unroute

Use the Unroute command to unroute all or selected objects in your design except locked nets.

Syntax

```
unroute [-all]
```

Options

-all	Unroutes your entire design

Unselect

Use this command to unselect all or selected objects in your design.

Syntax

unselect [**-all**] | {**comp** | **pin** | **net** | **node** | **layer** | **path** | **macro** | **site** | **wire**} [**-id**] *name*

Options

-all	Unselects all selected objects in your design
-id	Specifies an index value for *name*
name	Specifies the name of the object; if the -id option is used, *name* is an index value

Zoom

Use the Zoom command to adjust the magnification of the display in the Array window. If you have more than one array view open at a time, the zoom command applies to the last activated one.

Syntax

zoom {in|out} [far][@cursor]

zoom {in|out}[*xpos:-32000, 32000 ypos:-32000, 32000***]**

zoom toggle [@cursor]

zoom toggle [*xpos:-32000, 32000 ypos:-32000, 32000***]**

zoom selection

Options

@cursor	Zooms the display centered around the spot in the window where you click the mouse button. If you do not specify this, the zoom takes place centered around the point in the center of the window.
far	Zooms all the way in or out.
selection	Zooms to the nearest setting that surrounds the selected object.

Chapter 7

Customizing the FPGA Editor

You can change many of the FPGA Editor default settings to customize the interface to suit your needs. This chapter includes the following sections.

- “Initializing the FPGA Editor”
- “Customizing the User Toolbar”
- “Customizing Mouse Buttons”
- “Customizing Colors”
- “Customizing Fonts”
- “Customizing with Command Aliases”
- “Customizing with Command Scripts”

Initializing the FPGA Editor

The fpga_editor.ini initialization file is installed in $XILINX/data when the FPGA Editor is installed on your system. This file is a text file containing a series of commands that are performed when the FPGA Editor is invoked. You can edit this file to include any of the commands described in the “Command Line Syntax” chapter.

When you invoke the FPGA Editor, it automatically finds the correct fpga_editor.ini file. The FPGA Editor looks for this file in the following order.

- Current working directory
- Your home directory
- $XILINX/data (a generic fpga_editor.ini file)

If you want to customize the fpga_editor.ini file to suit your needs, you can create a fpga_editor_user.ini file in your home directory. When the FPGA Editor is invoked, it reads the fpga_editor.ini file before the fpga_editor_user.ini file. You can also copy the fpga_editor.ini file to your working directory and edit it as well for your own use.

Customizing the User Toolbar

You can customize the User toolbar to include commands that you frequently use in your editing sessions. You can either edit the fpga_editor.ini (or fpga_editor_user.ini) file before you start the FPGA Editor, or you can make changes to the User toolbar during an editing session.

Before Starting the FPGA Editor

When the FPGA Editor is invoked, it reads the fpga_editor.ini file, as described in the "Initializing the FPGA Editor" section. One function of the fpga_editor.ini file is to set the default User toolbar commands that are displayed when the FPGA Editor window opens. You can change the default configuration by editing the fpga_editor.ini or fpga_editor_user.ini file.

During an Editing Session

You can also add or delete commands to the User toolbar during an editing session with the Button and Unbutton commands. Any command changes made during an editing session are not saved for later sessions. These commands are described in the "Command Line Syntax" chapter.

Customizing Mouse Buttons

You can program mouse buttons to run commands from the command line by clicking the appropriate mouse button. You can only program commands to mouse clicks; not to clicking and holding down the mouse button.

EPIC supported a three button mouse on the workstation, and a two button mouse on the PC. The FPGA Editor supports only the left and

right mouse buttons on the workstation. The following table includes some comparisons between EPIC and FPGA Editor mouse actions.

Table 7-1 Mouse Button Functions

Function	FPGA Editor on Workstation and PC	EPIC on Workstation	EPIC on PC
Zoom in	Control + Right Click	Middle Click	Right Click
Zoom out	Shift + Control + Right Click	Right Click	Shift + Right Click
Pan	Control + Right Drag	Right Drag	Right Drag
Select toolbar buttons, menus, menu commands, dialog box options, design objects	Left Click	N / A	N / A
Display a context-sensitive popup menu for the selected window area or design object. Use the right mouse button to select a command from this menu.	Right Click	N / A	N / A

To re-program mouse buttons, use the Alias command in the fpga_editor.ini or fpga_editor_user.ini file, as shown in the following lines from the default fpga_editor.ini file. For more information on the Alias command, see the “Alias” section of the “Command Line Syntax” chapter.

```
alias [LeftClick] "unselect -all; pick -order pin:etc"
alias [Control+LeftClick] "pick -order pin:etc"
```

The mouse aliases used in the default fpga_editor. ini file are shown in the following table. If you unalias a programmed mouse button, the FPGA Editor restores the default command to that button.

Mouse Button	Command Mapping
Left Click	unselect -all; pick -order *order_spec*
Control + Left Click	pick -order *order_spec*
Shift + Left Click	pick -k -order *order_spec*
Control + Shift + Left Click	pick -order *order_spec*
Control + Right Click	zoom in @cursor
Shift + Control + Right Click	zoom out @cursor
Left Double Click	post block

Customizing Colors

Areas in the FPGA Editor window (such as the User toolbar or the history area) are automatically assigned colors when the FPGA Editor window opens. These colors cannot be modified after an FPGA Editor session begins. Layers of objects in the Array window (for example, components, long lines, or selected objects) are also assigned colors when the FPGA Editor window opens. On a workstation or a PC, you can customize the layer colors that appear when you first open the FPGA Editor window, and you can modify these colors at any time during an FPGA Editor session.

Changing Window Colors on the Workstation

On the workstation, you can change the color of the FPGA Editor windows in your .Xdefaults file. You can use any of the colors from the full palette supported by the X Window System. See your X Window System documentation for more information.

Changing Window Colors on the PC

On the PC, the FPGA Editor windows use the standard system colors. You can change these colors by selecting the Display icon in the

Control Panel. The default colors for some of the areas in the FPGA Editor window are shown in the following table.

Window Area	Color
Background of Array window	Black
Background of World window	Black
Background of List window	White
Background of Menu bar	Standard System Colors
Background of History area toolbar	Standard System Colors
Background of User toolbar	Standard System Colors
Background of Command Line toolbar	Standard System Colors
Background of Status bar	Standard System Colors

Changing Object Colors on Workstation and PC

On a workstation or a PC, you can control the colors of layers of objects (such as sites, components, switchboxes) in the Array window. You can change the colors assigned when the FPGA Editor window opens, and also change colors during an editing session. When you change layer colors during an editing session, the changed colors are only valid for the current session.

When the FPGA Editor window opens, the system assigns default colors to object layers. You change these default colors by editing the fpga_editor.ini file. To change colors during an editing session, use the Command Line toolbar. Both of these procedures are described in this section.

Note: You can also modify a layer color by using a Layer Properties dialog box as described in the “Viewing and Changing Properties” section in the “Using the FPGA Editor” chapter.

Editing the FGPA_editor.ini File

1. Open the fpga_editor.ini file with a text editor.
2. Enter the following command for each layer color you want to modify.

   `setattr layer` *layer_name* **`color`** *color*

The *layer_name* variable specifies the name of a particular layer. Examples of types of layers are sites, components, switch boxes, pinwires, local lines, long lines, pips, routes, ratsnests, hilite, select, and text. Different layers are available for different device architectures.

The *color* variable specifies the color you want to use for a particular layer. Possible colors are black, blue, green, cyan, red, magenta, yellow, white, grey, dark blue, dark green, dark cyan, dark red, dark magenta, or olive.

Using the Command Line Toolbar

At any time during an FPGA Editor session, you can change the color assigned to a specified layer by entering the Setattr command in the Command Line toolbar.

`setattr layer` *layer_name* **`color`** *color*

The *layer_name* variable specifies the name of a particular layer. Examples of types of layers are sites, components, switch boxes, pinwires, local lines, long lines, pips, routes, ratsnests, hilite, select, and text. Different layers are available for different device architectures.

The *color* variable specifies the color you want to use for a particular layer. Possible colors are black, blue, green, cyan, red, magenta, yellow, white, grey, dark blue, dark green, dark cyan, dark red, dark magenta, or olive.

Customizing Fonts

You can change the fonts used in dialog boxes, menu bars, and other areas of the FPGA Editor window.

Changing Fonts on the Workstation

On the workstation, you can change the fonts used in the FPGA Editor in your .Xdefaults file. You can use any of the fonts supported by the X Window System. See your X Window System documentation for more information.

Changing Fonts on the PC

On the PC, the FPGA Editor windows use the standard system fonts. You can change these fonts by selecting the Display icon in the Control Panel.

Customizing with Command Aliases

You can use the Alias command to assign a name to an FPGA Editor command stream. You can then enter the alias name to perform the assigned commands. This is useful for abbreviating or renaming existing commands. Refer to the "Alias" section of the "Command Line Syntax" chapter for more information. Default aliases for the FPGA Editor are in the fpga_editor.ini file.

Defining Keyboard Shortcuts

Note: The keyboard shortcuts for the FPGA Editor pull-down menu commands are hard coded and cannot be used with the Alias command. For example, you cannot re-program the Control + O shortcut for the Open command to perform any other command.

For frequently used FPGA Editor commands, you can create keyboard shortcuts by programming one or more keys to execute any of the commands described in the "Command Line Syntax" chapter. After the shortcut keys are defined, you can invoke a command by pressing the appropriate key ("hot key") when the Array window has the keyboard focus instead of typing the command in the command line toolbar.

On PCs, you must click the left mouse button in a window to activate the commands applicable to that window. For example, if your active window is the List window, and you move the cursor to the Array window, and type a keyboard shortcut without first clicking in the Array window, the shortcut will not work.

The default aliases for the keys are contained in the fpga_editor.ini file. You can set up your own default aliases in the fpga_editor_user.ini file. On initialization, the FPGA Editor reads the fpga_editor.ini and fpga_editor_user.ini files in the following order.

1. Current working directory
2. Home directory

3. $XILINX/*architecture*/data directory
4. $XILINX/data directory

To view a list of the active keyboard shortcuts in the history area, enter the following in the command line toolbar.

```
alias
```

A listing similar to the following is displayed.

"0x111" ([UpArrow]) = "pan up 75"

"0x113" ([LeftArrow]) = "pan left 75"

The hexadecimal number represents the value for the key enclosed in brackets. The information following the equal sign is the FPGA Editor command represented by the key. For example, first alias listed uses the UpArrow key to pan up 75% of one window height.

The default shortcuts that you can customize are listed in the following table.

Table 7-2 Default Shortcuts

Key Name	Action
Left arrow (←)	Pan left 75 % of one window width
Right arrow (→)	Pan right 75 % of one window width
Up arrow (↑)	Pan up 75 % of one window height
Down arrow (↓)	Pan down 75 % of one window height
Shift + ←	Pan to left edge of device
Shift + →	Pan to right edge of device
Shift + ↑	Pan to upper edge of device
Shift + ↓	Pan to lower edge of device
Space bar	Center the window about the cursor
A,a	Posts the Command Line toolbar
C, c	Toggle the view of components
N, n	Toggle the view of ratsnest lines
Q, q	Display information about the object currently under the cursor
R, r	Toggle the view of routes

Table 7-2 Default Shortcuts

Key Name	Action
S, s	Toggle the view of sites
T, t	Toggle the view of text
X, x	Posts the Command Line toolbar
Z, z	Toggle the zoom

The following table lists the hard-coded shortcuts that cannot be customized.

Table 7-3 Hard-Coded Shortcuts

Key Name	Action
F1	Help
F2	Go to command line
Control + N	File → New
Control + U	Undo last action
Control + F6	Go to next window
Shift + Control + F6	Go to previous window
Control + C	Copy
Control + O	File → Open
Control + P	File → Print
Control + S	File → Save
Control + V	Paste text to the command line
Control + X	Cut text from the command line

You can define keyboard shortcuts either on the command line during an editing session, or in the initialization file. Shortcuts defined during an editing session can only be used for that session. Shortcuts defined in the .ini file can be used for all subsequent sessions.

Customizing with Command Scripts

A script is a series of commands that you can record and play back.

Recording a Script

Use the following steps to record a script.

1. If the script is going to be used on objects that will change each time you run the script, you must first select the objects you want the script to process.
2. Select the following commands to display the Script Record dialog box.

   Tools → Scripts → Begin Recording

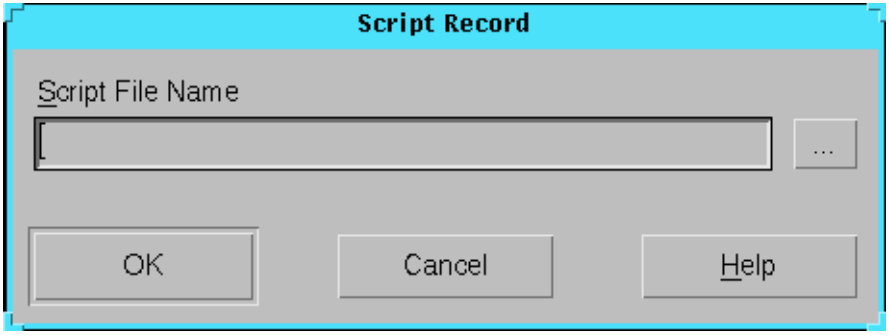


Figure 7-1 Script Record Dialog Box

3. Enter a name in the Script File Name field, or press the browse button and use the Save As dialog box to specify the name and directory. Script files use a .scr extension. If you do not include an extension, the system adds this extension to your file name.
4. Select **OK**.
5. Enter the series of commands that you want to record on the command line, from the pull-down menus, and so on.

Note: The Script Record dialog box does not allow nested scripts. If you attempt to record a script within a script using the Script Record dialog box, you will get an error message. However, you can manually edit a script file to use nested scripts.

6. To finish recording the script, select the following.

   Tools → Scripts → End Recording

Playing Back a Script

1. If the script commands are performed on selected objects, you must first select these objects.
2. Select the following to display the Script Playback dialog box.

   `Tools` → **`Scripts`** → **`Playback`**

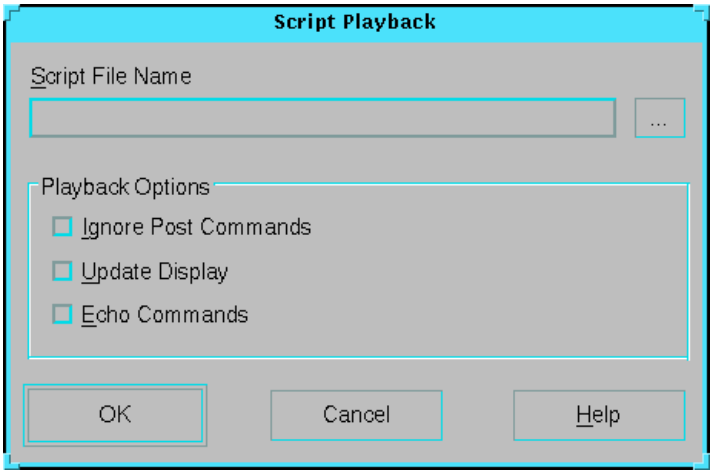


Figure 7-2 Script Playback Dialog Box

3. Enter the script file name in the Script File Name field, or press the browse button and use the Open dialog box to select the file.
4. Select the Playback Options to specify the following.
   - Ignore Post Commands

     Dialog boxes resulting from commands in the script are not posted as the script plays back. If you do not select this option, dialog boxes are posted and remain open after playback is finished. In either case, the commands invoked by the dialog boxes are performed.
   - Update Display

     This option updates the display in the FPGA Editor window every time a command that redraws the window is run by the script. If you do not select this option, the display is updated only after script playback is finished.

- Echo Commands

  The commands run by the script appear in the history area during playback. If you do not select this option, the only commands that appear in the history area are the commands indicating when the script playback starts and ends. This option is useful because you can scroll through the history area to view the commands.

5. Select **OK**.

   The commands in the script are performed on the selected objects.

Appendix A

Glossary

This appendix contains definitions and explanations for terms used in the FPGA Editor manual.

Definitions

array window

The Array window displays a graphical representation of the FPGA device. The device components and the interconnections (both logical and routed) between these components are displayed in this window. When you edit the internal logic of a programmable component such as a logic block, a schematic of the interior of the component is displayed in the Block window.

autoplace

The automatic placement (AutoPlace) is software that selects sites intelligently based on routability. You can automatically place selected components in your design.

autoroute

AutoRoute automatically routes the objects you specify.

bank shot

A bank shot is a way of indirectly connecting two switch box pins that cannot be connected directly. If you want to route a bank shot through a switch box, you must select (in the correct order) the local lines leading to all of the pins you want to connect.

block

A group consisting of one or more logic functions.

block window

The Block window is used to edit logic blocks. You can use only one Block window at a time for editing; however, you can have additional Block windows open for viewing.

carry logic

An architecture feature of the Xilinx XC4000 and XC5200 families. Carry logic is designed to speed-up and reduce the area of counters, adders, incrementers, decrementers, comparators, and subtractors. It is a special interconnect that speeds up the carry path of adders and counters from one CLB to another. This dedicated carry line runs along each column of CLBs as well as the top and bottom CLBs. FPGA Express can synthesize carry logic directly.

CLB

The CLB, or Configurable Logic Block, constitutes the basic FPGA cell. It consists of two 16-bit function generators (F or G), one 8-bit function generator (H), two registers (flip-flops or latches), and reprogrammable routing controls (multiplexors).

command line toobar

Use the Command Line toolbar to enter commands from the keyboard.

component

A component is an instantiation of a physical logic cell such as a CLB or IOB.

constraints

Constraints are specifications for the implementation process. There are several categories of constraints: routing, timing, area, mapping, and placement constraints.

Using attributes, you can force the placement of logic (macros) in CLBs, the location of CLBs on the chip, and the maximum delay between flip-flops. PAR does not attempt to change the location of constrained logic.

CLBs are arranged in columns and rows on the FPGA device. The goal is to place logic in columns on the device to attain the best possible placement from the point of view of performance and space.

constraints file

A constraints file specifies constraints (location and path delay) information in a textual form. You can also place constraints on a schematic.

delay calculator

This tool calculates and displays the delay associated with load pins and driver pins in a given net or path.

Design Rule Check (DRC)

Physical DRC is a series of tests to discover physical errors and some logic errors in your design.

device

A device is an integrated circuit or other solid-state circuit formed in semiconducting materials during manufacturing.

external pin

A macro pin used to connect the components in an instantiated macro to other components in your design (outside of the macro).

FPGA

An FPGA, or field programmable gate array, is a class of integrated circuits pioneered by Xilinx for which the logic function is defined by the customer using Xilinx development system software after the IC has been manufactured and delivered to the end user.

FPGA Editor

A graphical application for displaying and configuring Field Programmable Gate Arrays (FPGAs).

fpga_editor.ini File

Script that determines what FPGA Editor commands are performed when the FPGA Editor starts up.

fpga_editor_user.ini File

You can customize the fpga_editor.ini initialization file by creating an fpga_editor_user.ini file in your home directory. When the FPGA Editor is initialized, it reads the fpga_editor.ini file first and then the fpga_editor_user.ini file.

history area toolbar

The History toolbar is located below the Array window and displays commands and responses. All error messages, warnings, and command responses are written to the History toolbar. Information in the History toolbar is especially useful for deciphering unexpected command results.

IOB (input/output block)

An IOB is a collection or grouping of basic elements that implement the input and output functions of an FPGA device.

layer

An FPGA Editor layer contains all of one type of object (for example, all long lines in the device, or all components in the design database).

layer visibility toolbar

The Layer Visibility toolbar allows you to specify which objects are displayed in the Array window. Select the layers you want displayed and deselect the layers you want hidden.

list window

The List window displays a list of the components, nets, layers, paths, and macros in your design. Use the pull-down list box at the top of the window to specify the items you want displayed in the List window.

local line

Local lines usually span across multiple CLBs; typically they are between switch boxes. Local lines do not directly connect to site pins, such as direct connects, and they do not span across the entire length of the device, such as long lines.

locking

Lock placement applies a constraint to all placed components in your design. This option specifies that placed components cannot be unplaced, moved, or deleted.

log file

The log file is a command log file. This file records all FPGA Editor commands executed and output generated.

long line

A long line connects to a primary global net or to any secondary global net. Each CLB has four dedicated vertical longlines. These lines are very fast. Long lines usually span the entire width or height of the device.

look-up table (LUT)

A look-up table, or LUT, implements Boolean functions.

macro

See the “physical macros” section.

macro instance

A copy of a macro library file inserted in a design file. When you add a macro instance to a design you “instantiate” the macro. A design may contain multiple instances of the same library file, and each will receive a unique name. Since the library file is copied into the design file when you instantiate a macro, if you then change the library file the changes will not be reflected in the macro instantiated in the design file. In this User’s Guide, the word “macro” may be used instead of “macro instance.” A macro library file will always be referred to as a “macro library file.”

macro library file

A file containing the definition of a macro. Macro library files have an .nmc extension.

menu bar

The menu bar is located above the Array window. Most of the FPGA Editor commands are available in the pull-down menus of the FPGA Editor window after a design is loaded.

map

Mapping is the process of assigning a design’s logic elements to the specific physical elements that actually implement logic functions in a device.

NCD File

A NCD file is the output design file from the MAP program and represents the physical design.

net

1. A net is a logical connection between two or more symbol instance pins. After routing, the abstract concept of a net is transformed to a physical connection called a wire.

2. A net is an electronic connection between components or nets. It can also be a connection from a single component. It is the same as a wire or a signal.

net delay

Displays the delay for all pins in a net. You can either find the delay for all pins in the net or you find delays for specific pins.

NMC File

A NMC file contains a physical macro which can be created or viewed with the FPGA Editor.

package

A package is the physical packaging of a chip, for example, PG84, VQ100, and PC48.

path

A path is a connected series of nets and logic elements. A path has a start point and an end point that are different depending on the type of path. The time taken for a signal to propagate through a path is referred to as the path delay.

path delay

A path delay is the time taken for a signal to propagate through a path.

PCF File

The PCF file is an ASCII file containing physical constraints created by the MAP program as well as physical constraints entered by you. You can edit the PCF file in the FPGA Editor.

Physical Design Rule Check (DRC)

Physical Design Rule Check (DRC) is a series of tests to discover logical and physical errors in the design. Physical DRC is applied to the FPGA Editor and BITGEN. Results of the DRC are written into the history area.

physical macros

A physical macro is a logical function that has been created from components of a specific device family. Physical macros are stored in files with the extension .nmc.

pin

A pin is an attachment point on a site or a component. Nets can be attached to pins.

pinwire

Pinwires are wires which are directly tied to the pin of a site (i.e. CLB, IOB, etc.)

placing

Placing is the process of assigning physical device cell locations to the logic in a design.

property

Properties are instructions placed on symbols or nets in an FPGA or CPLD schematic to indicate their placement, implementation, naming, directionality, or other properties.

ratsnest

A ratsnest consists of lines that are point to point connections between unrouted pins on a given net.

reference component

A component in the macro library file used as a reference when a macro instance is placed, moved, or copied. Placement and routing of all other pre-placed macro components are determined relative to this component.

router

The router is the utility that connects all appropriate pins to create the design's nets.

routing

The process of assigning logical nets to physical wire segments in the FPGA that interconnect logic cells.

route-through

A route that can pass through an occupied or an unoccupied CLB site is called a route-through. You can manually do a route-through in the FPGA Editor. Route-throughs provide you with routing resources that would otherwise be unavailable.

site

A site is a programmable logic element (used or unused) location within the device, sites are potential locations for components and are displayed in the Array window as outlines of components.

speed

Speed is a function of net types, CLB density, switching matrices, and architecture.

status

The status bar appears at the bottom of the main window. When you select a menu command, a brief description of the command's function appears in the status bar.

switch box

A switch matrix is a collection of transistors located between CLB blocks that enables the connection of two interconnect lines. PPR uses the switch matrices and interconnects to connect CLB inputs and outputs. Switch matrices reduce some of the net delay. They have three possible directions: top, bottom, and left.

title bar

The title bar displays the program name and the name of the currently loaded design.

timing

Timing is the process that calculates the delays associated with each of the routed nets in the design.

TRACE

TRACE (Timing Reporter and Circuit Evaluator) is a program you can run within the FPGA Editor that provides static timing analysis of the physical design based on input timing constraints.

user toolbar

The User toolbar provides a convenient way to perform frequently used commands. To use a command, select the appropriate command button with the left mouse button.

wire

A wire is a net or a signal. See the “net” section.

world window

The World window shows the area of the device that is currently displayed in the Array window. As you pan and zoom the Array window, notice the corresponding changes in the size and position of the rectangle within the World window. Also, any objects selected in the Array window appear in the World window. You can drag the inner box with the mouse button to pan the display to the desired position. If you have multiple Array windows, the World window displays a rectangle for each Array window.

Appendix B

FPGA Editor Files

This appendix gives a listing of the files used by the FPGA Editor.

Name	Type	Produced By	Description
fpga_editor.ini	ASCII	Xilinx software	Script that determines what FPGA Editor commands are performed when FPGA Editor starts up.
fpga_editor_user.ini	ASCII	Xilinx software	A supplement to the *fpga_editor.ini* file used for modifying or adding to the *fpga_editor.ini* file.
.log	ASCII	FPGA Editor	FPGA Editor command log file. This file keeps a record of all FPGA Editor commands executed and output generated.
.ncd	Data	Mappers, Translators, PAR, FPGA Editor	A flat physical design database correlated to the physical side of the .ngd in order to provide coupling back to your original design.
.nmc	Binary	FPGA Editor	Xilinx physical macro library file. Contains a physical macro definition that can be instantiated into an FPGA Editor design.

Name	Type	Produced By	Description
.out	ASCII	FPGA Editor	The system keeps track of all commands performed on your design in the temporary command log file, *design_name*_fpga_editor.out. This file is erased when you end an editing session. If a session is unexpectedly terminated, the *design_name*_fpga_editor.out file remains in your current design directory, and the next time you start the FPGA Editor, the *design_name*_fpga_editor.out file is renamed *design_name*_fpga_editor.rcv.
.pcf	ASCII	Mapper, Translator, FPGA Editor	A file containing constraints specified during design entry (i.e., schematics) and constraints added by the user.
.rcv	ASCII	FPGA Editor	FPGA Editor recovery file.
.scr	ASCII	FPGA Editor	Command script file.

Window Manager Resources

On a UNIX workstation, you may also customize the appearance of the FPGA Editor by modifying the X window system configuration file,.Xdefaults. In addition, you may be able to customize your window manager to simplify access to the FPGA Editor and the graphic shells. This is done by modifying the window manager-specific resource files.

Appendix C

Configuring Xprinter

This appendix provides detailed instructions on configuring a printer so you can print from the Xilinx application. The information in this appendix applies only to workstation applications.

You must have the following Wind / U files installed correctly to print from your application.

- PPD (PostScript Printer Description)

  PPD files provide Wind / U with model-specific information like paper tray configuration, supported paper sizes, available ROM fonts, and so forth.

- AFM (Adobe Font Metric) and TFM (Tagged Font Metric)

  AFM and TFM files provide font metric information for all fonts in PostScript and PCL5 printers, respectively.

- Other files

  Various other files are copied to `$WUHOME/xprinter` and are required by Wind / U when printing. These include `xprinter.prolog` (PostScript prolog), `psstd.fonts` and `pclstd.fonts` (provide PostScript / PCL5 to X Window System font name mappings), and `rgb.txt`.

Make a complete, as-is copy of the directory `$WUHOME/xprinter` and include it in the installation for your product. None of the files from this directory require modifications in most environments.

Note: All of the files in $WUHOME / xprinter are the property of Bristol Technology and are licensed to you under the terms of the Wind / U license agreement. You can freely distribute these files as long as they are bundled with your application. Consult the Wind / U license agreement for further details.

Configuring .WindU

Once you have installed the required printer configuration files on your system, you must configure the .WindU file in your home directory (or SYS$LOGIN:WINDU.INI) for printing.

You can modify the .WindU file either by using a text editor or the Xprinter Printer Setup dialog box. Using the dialog box is recommended, because it reduces the risk of error. The instructions in this appendix describe how to edit the .WindU file, and then provide step-by-step instructions for performing the same task with the Printer Setup dialog box. These instructions are provided to help you configure your printer.

Printer Information

When you configure Wind/U to print, you need to know the following information for each printer you want to access.

- Name of the printer description (PPD) file
- The command used to send output to a printer

PPD Files

The Wind/U installation media includes the PPD files for most commonly used printers. To verify that the PPD file associated with your printer is included, look at the Printer Devices dialog (from the Printer Setup dialog, click Install and Add Printer). If your printer model is listed, Wind/U has a PPD file for your printer. If your printer model is not listed, contact your printer vendor to obtain the PPD file for your printer.

Unix Print Command

The command used to send output to a specific printer depends on the platform, the printer, and how the printer is connected to your system. For example, if a printer is connected directly to your system, the following might be valid print commands.

Unix	`lp -d ps -t$XPDOCNAME`
OpenVMS	`PRINT /QUEUE=OPTRA`

If your printer is connected to a different system on your network, your printer command will specify how to connect to that system. For example, if a printer is connected to the system bandit on your network, any of the following might be valid print commands

```
rsh bandit lp -d ps -t$XPDOCNAME
```

Note: In these examples, $XPDOCNAME represents the name of the output file sent to the printer with the specified command. If you use a multi-word file name, such as *a print file*, you must enclose the $XPDOCNAME in quotation marks as follows. You must escape the quotation marks in the remote command, because `rsh` strips them out if you do not.

Local Printer	`lp -d ps -t"$XPDOCNAME"`
Remote Printer	`rsh bandit lp -d ps -t\"$XPDOCNAME\"`

Configuring Wind/U for Printing

Once you know the name of the PPD file and the print command for each printer you want to direct output to, you can configure Wind/U to recognize those printers. To configure Wind/U to recognize a printer, you must do the following

1. Define a port, which is an alias for the print command.
2. Associate the port with the printer's PPD file.
3. Specify a default printer.
4. Set printer options.

Defining a Port

A printer port is an alias for the print command. It is defined in the [ports] section of $HOME/.WindU and appears as part of the Printer Name in the Printer Setup dialog box. For example, the following is the first Printer Name in the Printer Setup dialog box before you make any changes to $HOME/.WindU.

```
AppleLaserWriter v23.0 PostScript on FILE:
```

In this Printer Name, FILE: is the port name. Port entries in the [ports] section have the following format.

port=*print_command*

The print_command sends output to the printer port. For example, if you have two printers: ORION and SIRIUS, your [ports] section may look like the following example.

```
[ports]
ORION=rsh bandit lp -d ps -t\"$XPDOCNAME\"
SIRIUS=rsh bandit lp -d ps -T pcl5 -t\"$XPDOCNAME\"
```

In this example, both printers are connected to the system *bandit*, so the print command is a remote shell command executed on *bandit*. ORION is a PostScript printer, so the command `lp -d ps` is executed on *bandit* to print to ORION. SIRIUS, however, is a PCL5 printer, so the print command executed on *bandit* to print to SIRIUS is `lp -d ps -T pcl5`.

If you have a printer connected to your local system, you need to add an entry for it. For the local printer, add an entry similar to the following.

```
[ports]
ORION=rsh bandit lp -d ps -t\"$XPDOCNAME\"
SIRIUS=rsh bandit lp -d ps -T pcl5 -t\"$XPDOCNAME\"
LOCAL=lp -d ps -t$XPDOCNAME
```

Your printer port can be any name, except FILE:, which is the only reserved port name. It causes HyperHelp to create a print file formatted specifically for the specified printer type.

You must create an entry in the [ports] section for every printer you want to print to.

To Define a New Port

To define a new port using the Printer Setup dialog box, perform the following steps.

1. To display the Ports dialog box, from the Printer Setup dialog box, click **Install**, **Add Printer**, and **Define New Port**.
2. Type the port definition in the Edit Port edit box.
3. Click **Add/Replace**.

The new port is now included in the list of current port definitions.

4. Repeat steps 1–3 for each printer you want to print to.

Note: To create a printer port for each available printer queue on HP700 systems, click the Spooler button in the Ports dialog box. This command creates a default printer port for each available printer queue returned by the lpstat -a command.

To Modify an Existing Port

To modify an existing port using the Printer Setup dialog box, perform the following steps.

1. To display the Ports dialog box, from the Printer Setup dialog box, click **`Install`**, **`Add Printer`**, and **`Define New Port`**.
2. Select the port you want to modify and edit the port information in the Edit Port edit box.
3. Click **`Add/Replace`**.

   The modified port is now included in the list of current port definitions.

Matching a Printer Type to a Defined Port

After you define a port for each printer, specify the type of printer associated with each port. Device types are listed in the `[devices]` section of the `.WindU` file. Each entry in the `[devices]` section has the following format.

alias`=`*PPD_file driver*`,`*port*

Note: There must be a space between the *PPD_file* and *driver* and a comma between the *driver* and the *port*. The following table describes each part of this entry.

Field	Description
alias	The *alias* is a descriptive name that identifies the printer. It can be anything. The *alias* is the name of the printer that appears in the Printer Setup dialog box, such as, `HP LaserJet 4L PostScript`).

PPD_file	The *PPD_file* is the name of the printer description (PPD) file used by the printer, without the `.PPD` extension.
driver	The *driver* is the type of driver the printer uses. Valid values are `PostScript`, `PCL4`, and `PCL5`.
port	The *port* is the printer port listed in the `[ports]` section of the .WindU file. (ORION, SIRIUS, and LOCAL appear in the example `[ports]` section.)

Following is an example procedure for configuring three printers.

Port	Printer Type	Output Type
ORION	HP LaserJet 4LPostScript	PostScript
SIRIUS	HP LaserJet 4M PCL Cartridge	PCL
LOCAL	QMS-PS 2200 v52.3	PostScript

1. Choose an alias for each printer.

   To easily identify the printer you want to use from the Printer Setup dialog box, use these aliases.

   - HP LaserJet PS
   - HP LaserJet PCL
   - QMS PS

Note: If you use the Printer Setup dialog box to associate ports and PPD files, you cannot specify a printer alias. You must choose an alias from the predefined list that appears in the Printer Devices list box in the Add Printer dialog box. The corresponding PPD file is already associated with the printer aliases in this list box.

2. Identify the PPD file associated with each of these printers. In this example, the `[devices]` section of the `.WindU` file appears as follows.

   ```
   [devices]
   HP LaserJet PS=HP3SI523 PostScript,ORION
   HP LaserJet PCL=HP4M PCL,SIRIUS
   QMS PS=Q2200523 PostScript,LOCAL
   ```

   After you add these entries to your `.WindU` file, the following printer choices are available from the Printer Setup dialog box.

```
HP LaserJet PS on ORION
HP LaserJet PCL on SIRIUS
QMS PS on LOCAL
```

To Match a Printer Device to a Port

To match a printer device to a port using the Printer Setup dialog, perform the following steps.

1. To display the **`Add Printer`** dialog box, from the Printer Setup dialog box, click **`Install`** and **`Add Printer`**.
2. In the **`Printer Devices`** field, select the description that matches the printer you are installing.

   If no description matches your printer, contact your printer vendor for a printer description (PPD) file and install it in the `$WUHOME/xprinter/ppds` directory.
3. Select the desired port in the **`Current Port Definitions`** list box and click **`Add Selected`**.

   The new printer is now included in the list of currently installed printers.

To Remove an Installed Printer

To remove a printer device / port combination using the Printer Setup dialog box, perform the following steps.

1. To display the **`Printer Installation`** dialog box, from the Printer Setup dialog box, click **`Install`**.
2. In the **`Currently Installed Printers`** list box, select the printer you want to remove and click **`Remove Selected`**.

Specifying a Default Printer

After all available printers are configured, you can make one of them the default printer. To specify a default printer in the Printer Setup dialog box, add an entry in the following format to the `[windows]` section of the `.WindU` file.

```
[windows]
device=PPD_file,driver,port
```

Provide the same information that you used in the [devices] section. Only the format of the entry is different; there is a comma between the *PPD_file* and the *driver* instead of a space.

For example, if you want the default printer to be the printer at port ORION, your [windows] section appears as follows.

```
[windows]
device=HP4L,PostScript,ORION
```

The printing-related sections of your .WindU file look like the following.

```
[windows]
device=HP4L,PostScript,ORION

[ports]
ORION=rsh bandit "lp -d ps -t"
SIRUS=rsh bandit "lp -d ps -T pcl5"
LOCAL=lp -d ps

[devices]
HP LaserJet PS=HP4L PostScript,ORION
HP LaserJet PCL=HP4M PCL,SIRIUS
QMS PS=Q2200523 PostScript,LOCAL
```

Whenever you make and save a change with the Printer Setup dialog box, the changes are written to the .WindU file in your home directory.

In your default .WindU file, the [windows] entry appears as follows.

```
[windows]
device=NULL,PostScript,FILE:
```

Because no PPD file is listed (NULL), the default in the Printer Setup dialog box is to print generic PostScript to a file. You can specify the file name and change the type of output to PCL in the Printer Setup dialog box.

To Specify a Default Printer

To specify a default printer using the Printer Setup dialog box, do the following.

1. To display the **Options** dialog box, from the Printer Setup dialog, click **Options**.

2. From the **Printer Name** drop-down list, select the desired printer and click **OK**.
3. Click **Save** in the Printer Setup dialog box.

Setting Printer Options

Because printer options vary between printers, use the Printer Setup dialog box to set them. Xprinter reads the PPD file to identify the specific options available for each printer.

1. Display the Printer Setup Dialog box.
2. Set all fields to the desired values. The following table describes all printer setup fields.

Option	Description
Output Format	Specify whether to send output to a file or to a printer. If you choose Printer Specific, you can send output to any printer type/port combination configured in your `$HOME/.windU` file. If the port is FILE: (as in this example), Xprinter creates an output file specifically for the specified printer type. If you choose Generic (File Only), print output is sent to an Encapsulated PostScript or generic PCL file.
Printer	Appears only if you select **Output Format: Printer Specific**. It specifies the name of the default printer to send print output to. Click the **Options** button to specify a different printer.
File Name	Appears only if you select **Output Format: Generic (File Only)**. Type the name of the print file to create. To pipe print output to a command, type a **!** character as the first character, then specify the command to pipe output to. For example, to pipe output to the `lp` command, enter the following: **!lp -d ps**.
EPSF PCL4 PCL5	Appears only if you select **Output Format: Generic (File Only)**. Click this button to display a list of output file types and select the desired type. Available types are EPSF (Encapsulated PostScript), PCL4, and PCL5.
Orientation	Specify portrait or landscape.

Scale	To increase the size of the output, specify a value greater than 1.00. To reduce the size, specify a value less than 1.00. For example, a value of 2.00 doubles the size of the output; a value of 0.50 reduces it by half.
Copies	Specify the number of copies to print.

3. To set additional options, such as selecting a new printer or changing the page size, click **Options**.
4. Set all options to the desired values.The following table describes all printer options.

Option	Description
Printer Name	Changes the Printer in the Setup dialog box. Click the down arrow to display a list of configured printers.
Resolution	Specify printer resolution. Values vary.
Page Size	Specify paper size. Values vary.
Paper tray	Specify tray where paper is located. Values vary.

5. Click **Save** to apply your changes and make them the new default values.

Sending Output to a File

The default `$HOME/.windU` file contains many printer devices, including the following.

```
HP LaserJet 4L PostScript=HP4L PostScript,FILE:
HP LaserJet 4M PCL Cartridge PCL5=HP4M PCL,FILE:
```

In all of the default entries, the port is `FILE:`, which is the only reserved port name. If you specify `FILE:` as the *port*, Wind / U creates a print file instead of sending output to a printer. When you use a PPD file, you generate PostScript or PCL output that is specific to the printer. If you use Output Format: Generic (File Only), you generate generic Encapsulated PostScript or PCL output.

For example, the HP LaserJet 4L PostScript entry creates a PostScript file that includes the characteristics of the HP 4L PostScript printer. The HP LaserJet 4M PCL entry creates a PCL file that includes the characteristics of the HP LaserJet 4M PCL printer.

You can also print to a file instead of a printer by selecting the Output Format: Generic (file only) option in the Printer Setup dialog box, but doing so creates a generic EPS or PCL print file that does not take advantage of any special characteristics of your particular printer.

Solving Printing Problems

If you have problems printing, use the following hints.

- Start with just printing to a PostScript file. You can use PostScript previewers (on Sun's pageview), to see the file. Adding spooling and PCL support later is easy.
- Ensure that the $WUHOME/xprinter files are installed correctly.
- Ensure that you have .WindU in your home directory.
- Check that the `printing` sample application works with the configuration you are using with your application.
- Ensure that there is a PPD file for the printer you are using. Xprinter requires a PPD file that describes the attributes (paper size, resolution, color capabilities, paper trays, and so forth). for each printer device you want to use. Wind/U includes a number of PPD files for common printers; however, these do not represent all supported printers. If you have customer whose printer is not included in the PPD files supplied with Wind/U, try the following.
  - Contact the printer manufacturer for the PPD file.
  - Download the PPD file from the Adobe FTP site (ftp.adobe.com:/pub/adobe/PPDfiles).
  - Use the PPD file for a similar output device.

If you continue to have problems, submit an SPR to Bristol Technical Support. Be sure to include a copy of your printer output and your `.windU` file.