WD90C33

High Performance VGA Controller for PC/AT/ISA/EISA/VESA and PS/2 Systems

WESTERN DIGITAL

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1.0 INTRODUCTION

The Western Digital® WD90C33 High Performance VGA Controller is a 0.8 micron CMOS VLSI device that provides GUI for WINDOWS. The WD90C33 supports hardware BITBLT, line draw, cursor, while maintaining backward compatibility with previous standards such as MDA, EGA, CGA, Hercules, and AT&T 6300. Designs that use the WD90C33 controller are able to run applications requiring VGA hardware and BIOS compatibility and also EGA register level compatibility on analog, TTL, or multifrequency monitors, in interlace or non-interlace mode. The WD90C33 supports high resolution graphics with 1024 by 768 dot resolution and 256 colors. The WD90C33 also supports 132-column text mode and 6-16 pixel fonts.

This data sheet provides a functional overview, signal pin details, a block diagram, internal register descriptions, AC/DC characteristics, timing diagrams, VLSI package information and associated references.

1.1 FEATURES

The WD90C33 provides the following features:

- A full-function VGA controller optimized for windows.
- Built-in interface with 32-bit 386/486 local bus
- Built-in interface with VESA local bus
- Integrated bus interface for AT and Micro Channel with minimum external component support.
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- True 32-bit host-to-display memory data transfers in graphics modes
- Hardware BITBLT for 4-bit, 8-bit, and 16-bit color modes.
  - Pattern Fill
  - Raster Operations
  - Transparency
  - Color Expansion for Text Support
  - Filled Rectangles
  - 32-Bit Memory or I/O Port imaging transfer to or from host.
  - X/Y Addressing
- Hardware assisted Line Draw for 4-bit, 8-bit, and 16-bit color modes.
  - Bresenham Line Algorithm
  - Strip Line Algorithm
  - X/Y Addressing with Clipping
- Hardware assisted trapezoidal fill
- Hardware assisted rectangular clipping
- Command Buffer eight levels deep
- BITBLT pipeline 4 levels deep.
- True 24-bit color with limited BITBLT hardware support.
- Host BITBLT supports memory mapped 32-bit transfers through the write buffer.
- Allows the CPU to access the display memory while the drawing engine is active.
- Supports up to:
  - 1024 x 768 x 256 color
  - 640 x 480 x 64K color
  - 640 x 480 x 16 million color
  - 1280 x 1024 x 256 color interlaced
- Hardware Cursor.
  - 64 by 64 pixels or 32 by 32 pixels
  - Inversion and transparency
  - Two color and three color modes
- Provides a single chip video graphics solution for IBM AT and PS/2 compatible systems.
- Supports up to 2M bytes of display memory with two 64K by 16 DRAMs; four, eight, or sixteen 256K by 4 DRAMs; or one, two, or four 256K by 16 DRAMs
- Fully compatible with IBM's VGA and EGA with hidden register support

- Fully compatible with CGA, MDA, Hercules Graphics and AT&T Model 6300 standards
- Supports 132-column text
- Write buffer for zero wait state CPU write performance
- Provides 16-bit or 32-bit memory interface with fast page operations.
- Up to 80 MHz maximum video clock rate.
- Up to 50 MHz maximum memory clock rate.
- Up to four simultaneous displayable fonts.
- 6-16 pixel-wide fonts.
- A maximum of 16 fonts can be loaded.
- Provides adapter video BIOS ROM decoding.
- Eleven-bit vertical counter to support scan resolution of up to 2048 scan lines.
- Supports 16-bit I/O register transfer to index/ data register pairs.
- Adjustable internal display FIFO and fast page memory interface.
- 208-pin EAIJ MQFP (Metric Quad Flat Package)
- Integrated Feature connector interface and external RAMDAC support.
- Programmable memory mapping register to map WD90C33 into any CPU memory address space
- Separate host address and data to save external glue logic (For AT and CPU local bus.)
- True color, 24-bit hardware cursor.
- Supports 256Kx16 DRAM with four CAS strobes and one write strobe.

2.0 WD90C33 ARCHITECTURE

The WD90C33 contains six major internal modules, the CRT Controller, the Sequencer, the Drawing Engine Data Path, Hardware Cursor Controller, Drawing Engine Controller and the Attribute Controller. The WD90C33 also has four major interfaces: the CPU and BIOS ROM interface, the DRAM Display Buffer interface, the Video and RAMDAC interface and the Clock interface.

An internal write buffer is used to achieve fast memory write. A zero wait state may be achieved with a 32-bit video memory interface for most memory write operations.

An internal FIFO is used to achieve the video display bandwidth necessary to interleave CPU accesses and display refresh cycles.

The CRT Controller module maintains screen refresh functions for the various display modes defined by the BIOS ROM resident firmware. The CRT Controller module also generates a horizontal sync (HSYNC), vertical sync (VSYNC) and blanking signal for the display monitor.

The Sequencer functions as a timing generator for the display memory cycles. It provides the character clock in the alphanumeric mode and the dot clock in the graphics mode. The sequencer arbitrates between video display refresh, Drawing Engine memory cycle, memory refresh, and CPU access of the video memory. The sequencer also provides write buffer control.

The Drawing Engine Data Path manipulates the data flow between the CPU and the video memory for both CPU write and CPU read cycles. The datapath also manipulates display data by doing color compare, color expansion, and data rotation. It contains a 32-bit Arithmetic Logic Unit (ALU) for raster operations.

The Drawing Engine controller generates memory addresses, data masks, and control signals for BITBLT, Line Draw, pattern fill, and other graphics operations.

The Attribute Controller serializes the video memory data into video data stream according to different display formats. It controls blinking, underlining, cursor, pixel panning, reverse video and background or foreground color in all display modes.

The Hardware Cursor Controller reads in each line of the cursor pattern during the horizontal retrace immediately preceding the scan line on which that line of the cursor pattern is to be displayed. It then merges the cursor pattern into the video stream for the scan line.

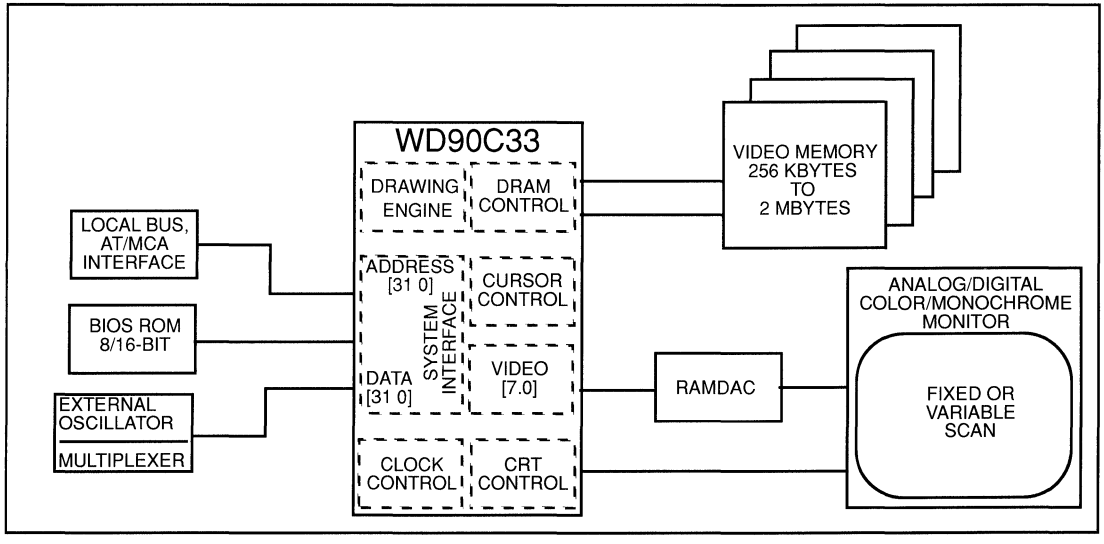

FIGURE 2-1 SYSTEM BLOCK DIAGRAM

3.0 WD90C33 INTERFACES

3.1 HOST INTERFACE

The WD90C33 is designed to interface directly with the 386/486 CPU 32-bit local bus. It also complies with the VESA local bus standard and provides the signals necessary to interface with the VESA connector. The WD90C33 also provides the interface for local bus RAMDAC, BIOS, and clock generator without using glue logic. While connected to the CPU local bus, the WD90C33 allows the user to choose whether to connect the RAMDAC to the local bus or to the system (AT) bus. The WD90C33 also supports RAMDAC write shadowing, and can interface with the video BIOS, which can be integrated with the system BIOS. Selection of the 32-bit local bus interface is determined by the state of Configuration register bit CNF(11) during power-on or system reset as described in Section 9.

The WD90C33 also operates in both the AT Bus and the PS/2 MicroChannel bus architecture configurations. The selection of the bus architecture determines the operating mode, and is selected by the state of Configuration Register bit CNF(2) during power-on or system reset as described in Section 9.

Whether configured for Local Bus, AT, or MicroChannel operation, the WD90C33 operates functionally in a manner that is compatible with the selected interface. The signal pins, memory maps and I/O ports all operate to optimize the selected interface with a minimum of external circuits.

The WD90C33 provides all the signals and decodes all the necessary memory and I/O addresses to interface with the Local bus, AT bus, or the MicroChannel bus in 8-bit or 16-bit data path modes. It also provides the necessary decoding of the adapter video BIOS ROM. Using the provided signals, it is possible to implement designs which operate in 8-bit or 16-bit mode and control an 8-bit or 16-bit BIOS ROM.

The I/O data path is programmable to be either 16-bit or 8-bit. Also, the CPU to display buffer data path can be eight or sixteen bits wide for all modes. $\overline{\text{ROM16}}$, $\overline{\text{IOCS16}}$, and $\overline{\text{MEMCS16}}$ signals are generated by the WD90C33 to indicate a 16-bit operation.

The WD90C33 has a display memory write buffer that holds the CPU write data until it can be transferred to the display memory, allowing the CPU to continue. This feature greatly reduces CPU wait states while writing to the video memory.

The WD90C33 provides the necessary wait states for CPU accesses to the video memory if necessary.

Special I/O ports such as 46E8h for the AT (or 03C3h for MicroChannel) for setup and 102h for VGA enable, have been implemented internally in the WD90C33.

3.2 DRAM INTERFACE

The WD90C33 has a flexible DRAM interface. It works with two or four 64K by 16 DRAMs with a 32-bit memory interface. It can also work with four 256 Kbyte by 4 DRAMs or one 256 Kbyte by 16 DRAM with a 16-bit memory interface. Other possible configurations are eight or sixteen 256 Kbyte by 4 DRAMS, and two or four 256 Kbyte by 16 DRAMS with a 32-bit memory interface. In all cases the WD90C33 uses the DRAM fast page mode to optimize performance.

The WD90C3 supports all standard IBM VGA modes with only two 64K by 16 DRAMs. Because it uses a 32-bit memory interface and has an internal write buffer, the WD90C33 can update the video memory without inserting wait states to the AT bus for most standard IBM VGA modes.

When additional DRAMs are installed the WD90C33 is capable of supporting high resolution color video modes (1024 by 768 with 256 colors, non-interlaced at 72 Hz vertical refresh rate).

The WD90C33 is designed to support 60 ns, 70 ns, 80 ns and 100 ns DRAMs with the dedicated MCLOCK, which can operate from 32 MHz to 50 MHz maximum.

The WD90C33 generates fast page DRAM timing for all BITBLT, cursor and CPU accesses, graphics display and text display. A choice of page mode and non-page mode operation is provided to access fonts in text modes.

The WD90C33 also generates CAS before RAS DRAM refresh for the display memory.

3.3 VIDEO INTERFACE

The WD90C33 is optimized to connect to an analog CRT monitor through a RAMDAC but it may also be used to drive other types of displays, such as TTL monitors. In interfacing to an analog monitor through an external RAMDAC, the WD90C33 provides all the necessary signals to interface to the video RAMDAC.

The video interface for a CRT is very dependent on the CRT requirements and the resolution and depth (bits/pixels) of the image desired. New monitors such as multifrequency monitors, are less stringent because of the many sync frequencies available. The WD90C33 can be programmed to directly generate all the CRT signals for up to eight bits/pixel (256 color) displays.

The MicroChannel Auxiliary Video Connector and the AT Feature Connector can be connected directly to the WD90C33. The WD90C33 also provides an input for a monitor type detection interface as done on the IBM VGA using comparators.

3.4 CLOCK INTERFACE

The WD90C33 has four clock input signals, Memory Clock, MCLK, which drives the DRAM and bus interface timing, and the three Video Clocks, VCLK0, VCLK1, and VCLK2, which drive the video timing. VCLK1 and VCLK2 can also be programmed as outputs to provide the option to externally control a multiplexer that supplies the video clock. MCLK can also be selected as a memory clock or video clock.

3.5 WD90C33 POWER-UP CONFIGURATION

The WD90C33 uses the memory data pins to configure an internal configuration register during power-on or system reset as described in Section 9. Configuration bit CNF(2) determines whether the WD90C33 will operate in AT or MicroChannel Architecture (MCA) implementation (AT or MicroChannel mode). Configuration bit CNF(11) determines whether the WD90C33 will operate in the Local Bus or AT bus mode. Other configuration (CNF) bits configured by the WD90C33 during power-on or system reset are used as status bits or for clock source control. For more information the WD90C33 configuration register, refer to Section 9.

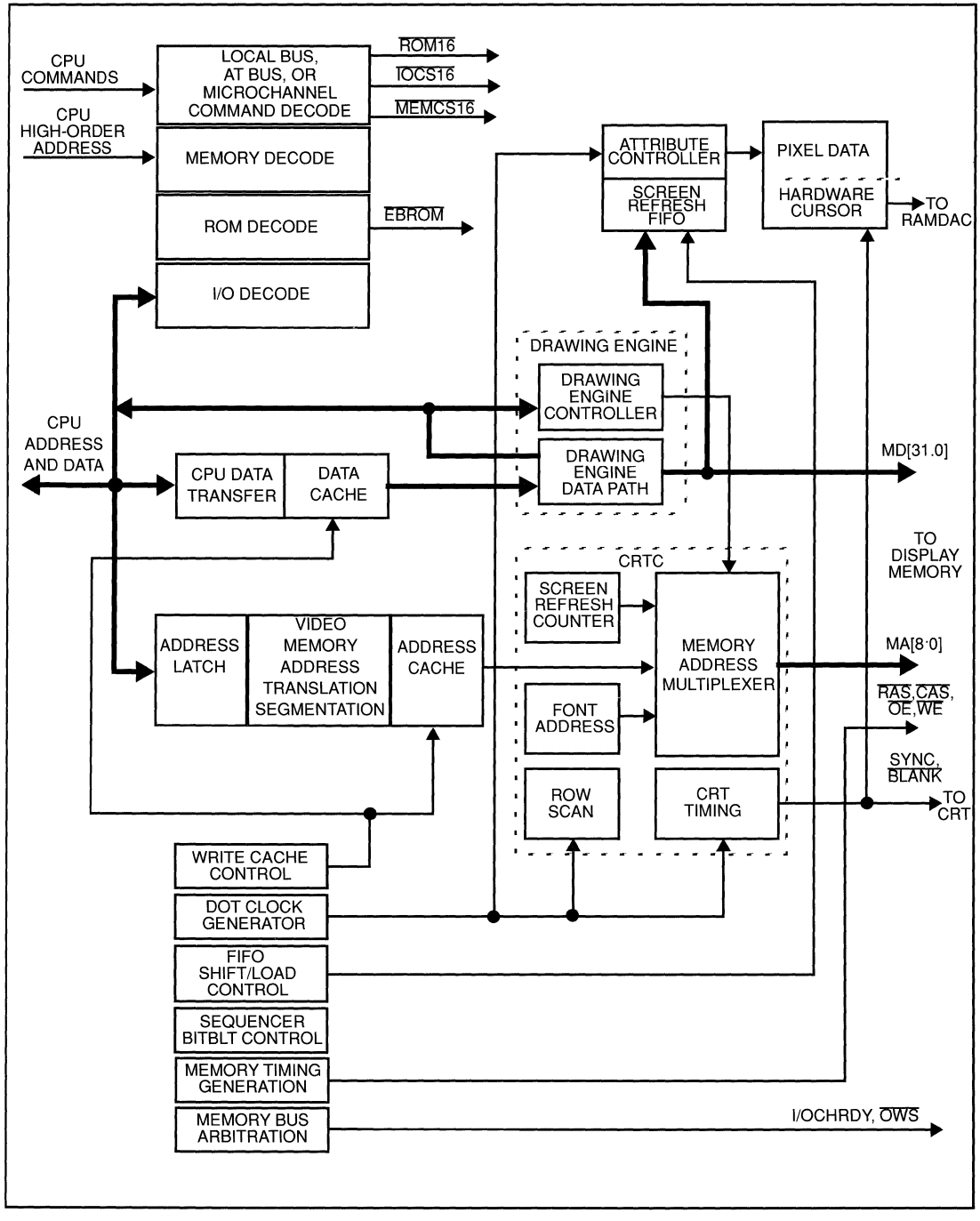

FIGURE 3-1 WD90C33 BLOCK DIAGRAM

4.0 SIGNAL DESCRIPTIONS

This section contains detailed information concerning signals and pin outs for the WD90C33 controller 208-pin package.

4.1 INTRODUCTION

This section contains the following information:

- Signal Mnemonic to Pin Location Table
- Signal and Pin Configuration Diagram
- Detailed Signal Descriptions
- Host Interface Pin Multiplexing

4.2 SIGNAL MNEMONIC TO PIN LOCATION

1. $\overline{RAS2}^1$	33. $MA1^1$	65. $A7^2$	97. D29
2. $\overline{WE1}^1/\overline{CAS1}^1$	34. $MA0^1$	66. GND^3	98. D28
3. MD15	35. $\overline{OE}^1$	67. $A8^2$	99. GND^3
4. MD14	36. GND^3	68. $A9^2$	100. D27
5. MD13	37. $\overline{OWS}^1$/ LDEVBUSY^1	69. $A10^2$	101. D26
6. MD12	38. $\overline{IOW}^2$/HRQ^2/ $\overline{CMD}^2$	70. $A11^2$	102. D25
7. GND^3	39. $EMEM^2$/ $CPURESET^2$	71. $A12^2$	103. D24
8. MD11	40. $\overline{EBROM}^1$	72. $A13^2$	104. VCC^3
9. MD10	41. $\overline{IOCS16}$/RDYIN/ $\overline{CDSETUP}$	73. $A14^2$	105. D23
10. MD9	42. VCC^3	74. $A15^2$	106. D22
11. MD8	43. $\overline{EIO}^2$/$LCLK^2$/ $3C3D0^2$	75. GND^3	107. D21
12. $\overline{WE0}^1/\overline{WE}^1$	44. $IRQ^1/\overline{IRQ}^1$	76. $A16^2$	108. D20
13. VCC^3	45. $ALE^2/\overline{ADS}^2/\overline{ALD}^2$	77. $A17^2$	109. VCC^3
14. MD7	46. IOCHRDY^1/ $\overline{VGARDY}^1$	78. $A18^2$	110. D19
15. MD6	47. $\overline{ROM16}/\overline{BOFF}$/ $\overline{CSFB}$	79. $A19^2$	111. D18
16. MD5	48. GND^3	80. VCC^3	112. D17
17. MD4	49. $\overline{MEMCS16}^1$/ $\overline{LDEV}^1/\overline{CDDS16}^1$	81. $A20^2$	113. D16
18. GND^3	50. $\overline{IOR}^2$/W/$\overline{R}^2/\overline{S1}^2$	82. $A21^2$	114. GND^3
19. MD3	51. $\overline{MRD}^2/\overline{MIO}^2$	83. $A22^2$	115. D15
20. MD2	52. $\overline{MWR}^2/\overline{DC}^2/\overline{S0}^2$	84. $A23^2$	116. D14
21. MD1	53. VCC^3	85. GND^3	117. D13
22. MD0	54. $\overline{SYSRESET}^2$/ $RSET^2$	86. $A24^2$	118. D12
23. $\overline{CAS}$	55. $\overline{BE3}^2$	87. $A25^2$	119. VCC^3
24. VCC^3	56. $A1^2/\overline{BE2}^2$	88. $A26^2$	120. D11
25. $MA8^1$	57. $\overline{BHE}^2/\overline{BE1}^2$	89. $A27^2$	121. D10
26. $MA7^1$	58. $A0^2/\overline{BE0}^2/\overline{BLE}^2$	90. $A28^2$	122. D9
27. $MA6^1$	59. GND^3	91. $A29^2$	123. D8
28. $MA5^1$	60. $A2^2$	92. $A30^2$	124. GND^3
29. $MA4^1$	61. $A3^2$	93. $A31^2$	125. D7
30. GND^3	62. $A4^2$	94. GND^3	126. D6
31. $MA3^1$	63. $A5^2$	95. D31	127. D5
32. $MA2^1$	64. $A6^2$	96. D30	128. D4

NOTE: Refer to notes at the end of this table.

TABLE 4-1 SIGNAL TO PIN LOCATION

129. VCC[3]	149. $\overline{WPLT}$[1]	169. VID5[1]	189. MD29
130. D3	150. $\overline{RPLT}$[1]	170. VID6[1]	190. MD28
131. D2	151. MDET[2]	171. VID7[1]	191. GND[3]
132. D1	152. $\overline{EXVID}$[2]	172. GND[3]	192. MD27
133. D0	153. No Connection	173. No Connection	193. MD26
134. GND[3]	154. No Connection	174. No Connection	194. MD25
135. VSYNC[1]	155. No Connection	175. No Connection	195. MD24
136. HSYNC[1]	156. No Connection	176. MCLOCK[2]	196. $\overline{WE2}$[1]/$\overline{CAS2}$[1]
137. BD0	157. No Connection.	177. GND[3]	197. VCC[3]
138. BD1	158. No Connection	178. VCLK0[2]	198. MD23
139. BD2	159. No Connection	179. VCLK1	199. MD22
140. BD3	160. GND[3]	180. VCLK2	200. MD21
141. VCC[3]	161. PCLK[1]	181. VCC[3]	201. MD20
142. BD4	162. $\overline{BLNK}$[1]	182. $\overline{EXPCLK}$[2]	202. GND[3]
143. BD5	163. VID0[1]	183. USR1[2]	203. MD19
144. BD6	164. VID1[1]	184. USR0[2]	204. MD18
145. BD7	165. VID2[1]	185. VCC[3]	205. MD17
146. GND[3]	166. VID3[1]	186. $\overline{WE3}$[1]/$\overline{CAS3}$[1]	206. MD16
147. BA1[1]	167. VCC[3]	187. MD31	207. $\overline{RAS}$[1]
148. BA0[1]	168. VID4[1]	188. MD30	208. VCC[3]

NOTES:

[1] Indicates output only signal names.

[2] Indicates input only signal names.

[3] Indicates power distribution pins.

Signal names not otherwise indicated are input/output.

The direction of signal flow is relative to the WD90C33 controller.

TABLE 4-1 SIGNAL TO PIN LOCATION

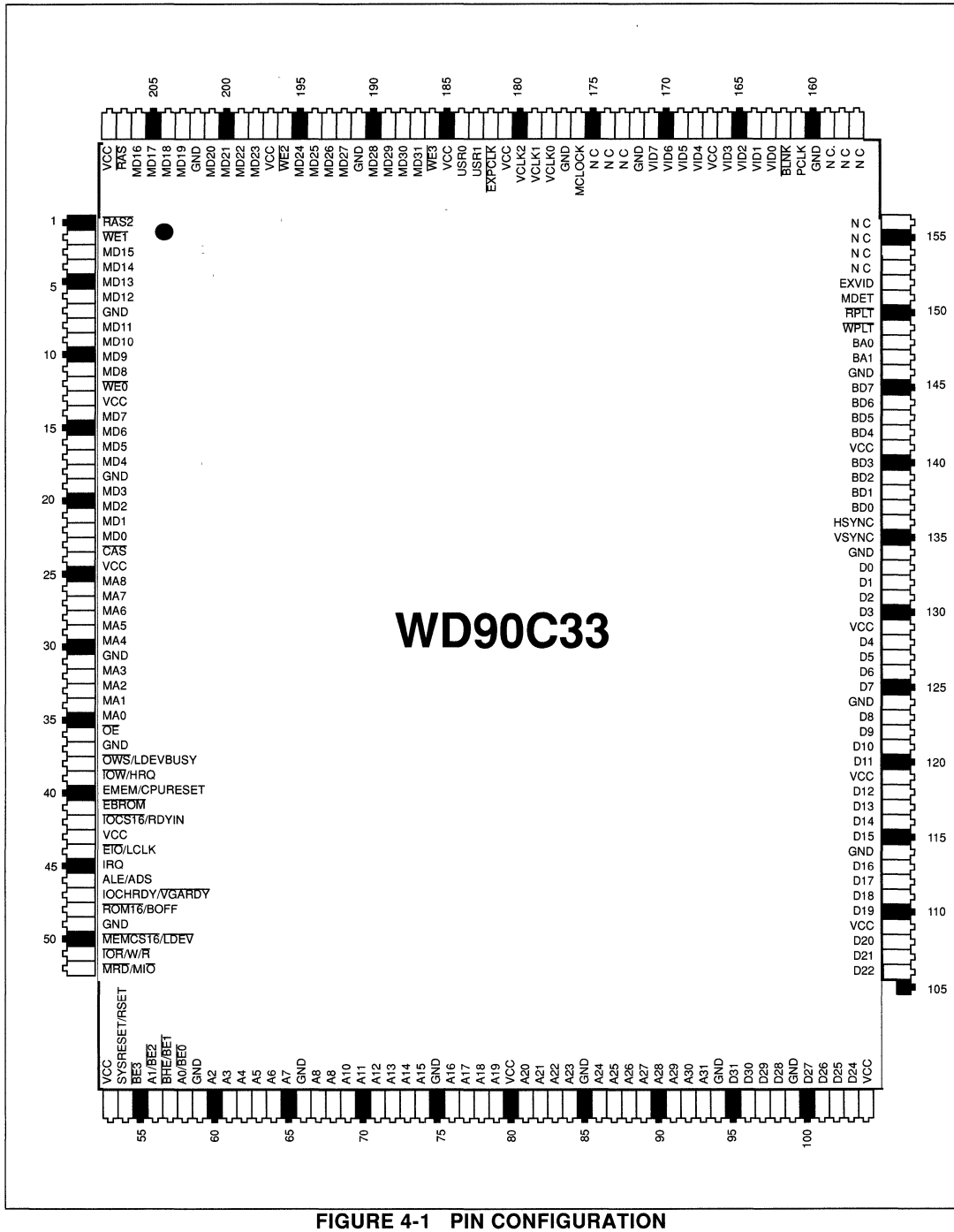

FIGURE 4-1 PIN CONFIGURATION

4.3 DETAILED SIGNAL DESCRIPTIONS

The following tables provide detailed signal descriptions for the WD90C33 controller 208-pin package. The signal descriptions are listed by the pin number and mnemonic given in Table 4-1. The definitions are listed in functional groups. The functional groups are listed below:

- Display Memory Interface
- RAMDAC Interface
- Clock Selection
- User Program
- Feature Connector
- CRT Control
- Host CPU Bus Interface
- Power Distribution
- Unused Connections

Where more than one signal name is indicated on the same pin, the signal names are separated by a virgule (/) in Table 4-1. The pin usage, as described in Table 4-2, changes for each signal name depending upon which bus interface is used as follows:

1. The letters AT in the bus column indicate an Industry Standard Architecture (ISA) bus compatible signal. The terms AT bus and ISA bus are used interchangeably unless otherwise indicated.
2. The letters MC in the bus column indicate an IBM MicroChannel bus compatible signal.
3. The letters LOC in the bus column indicate a local bus compatible signal.
4. Where no specific bus is indicated, the signals are used in all bus modes.

Table 4-2 lists and provides descriptions for the WD90C33 connector pins.

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
Display Memory Interface (49 Pins)				
207	$\overline{RAS}$	---	Active Low Output	**ROW ADDRESS STROBE** Strobe for the first 1 Mbyte of DRAM
1	$\overline{RAS}$2	---	Active Low Output	**ROW ADDRESS STROBE 2** Strobe for the second 1 Mbyte of DRAM, only if 2M of DRAM memory are used.
186	$\overline{WE}$[3] or $\overline{CAS}$[3]	---	Active Low Output	**WRITE ENABLE 3 or COLUMN ADDRESS STROBE 3** If CNF17 = 1, $\overline{WE}$[3] is the write enable signal for MD[31:24] If CNF17 = 0, $\overline{CAS}$[3] is the column address strobe for MD[31:24]
196	$\overline{WE}$[2] or $\overline{CAS}$[2]	---	Active Low Output	**WRITE ENABLE 2 or COLUMN ADDRESS STROBE 2** If CNF17 = 1, $\overline{WE}$[2] is the write enable signal for MD[23:16] If CNF17 = 0, $\overline{CAS}$[2] is the column address strobe for MD[23:16]
2	$\overline{WE}$[1] or $\overline{CAS}$[1]	---	Active Low Output	**WRITE ENABLE 1 or COLUMN ADDRESS STROBE 1** If CNF17 = 1, $\overline{WE}$[1] is the write enable signal for MD[15:8] If CNF17 = 0, $\overline{CAS}$[1] is the column address strobe for MD[15:8]
12	$\overline{WE}$[0] or $\overline{WE}$	---	Active Low Output	**WRITE ENABLE 0 or WRITE ENABLE** If CNF17 = 1, $\overline{WE}$[0] is the write enable signal for MD[7:0] If CNF17 = 0, $\overline{WE}$ is the write enable signal for MD[31:0]
23	$\overline{CAS}$ or $\overline{CAS0}$	---	Active Low Input/ Output	**COLUMN ADDRESS STROBE or COLUMN ADDRESS STROBE 0** If CNF17 = 1, $\overline{CAS}$ is the column address strobe for two, four, eight, and sixteen DRAM configurations If CNF17 = 0, $\overline{CAS}$[0] is the column address strobe for MD[7:0]
35	$\overline{OE}$	---	Active Low Output	**OUTPUT ENABLE** Output enable signal for two, four, eight, and sixteen DRAM configurations
25 MA8 26 MA7 27 MA6 28 MA5 29 MA4 31 MA3 32 MA2 33 MA1 34 MA0		---	Active High Output	**MEMORY ADDRESS** Display memory DRAM address. For testing, these pins can be tristated by setting PR4 register bit 4 to 1.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
187 188 189 190 192 193 194 195 198 199 200 201 203 204 205 206 3 4 5 6 8 9 10 11 14 15 16 17 19 20 21 22	MD31 MD30 MD29 MD28 MD27 MD26 MD25 MD24 MD23 MD22 MD21 MD20 MD19 MD18 MD17 MD16 MD15 MD14 MD13 MD12 MD11 MD10 MD9 MD8 MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0	---	Active High Input/ Output	**DISPLAY MEMORY DATA** These lines are the data bus for the video display DRAMS. These data lines are pulled up by internal 50 Kohm resistors, but may be pulled down by external 4.7 Kohm resistors to provide configuration information during power-on and system reset as follows: **MD FUNCTION REGISTER(BIT)** [31:30] $\overline{VIOR}/\overline{VIOW}$ High/Low Duration CNF[31:30]+ [29:28] $\overline{VMWR}/\overline{VMRD}$ High Duration CNF[29:28]+ [27:26] $\overline{VMWR}/\overline{VMRD}$ Low Duration CNF[27:26]+ 25 Set BIOS In Local Bus Mode CNF[25]+ 24 Connect RAMDAC In Local Bus Mode CNF[24]+ 23 Enable Local Bus Interface CNF[23]+ 22 Select Pulse Width High/Low Duration for RAMAC, IOR, and IOW; also Duration of $\overline{EBROM}$ MRD CNF[22]+ 21 Select 386/486 Local Bus Interface CNF[21]+ 20 Terminated Local Bus VGA Cycle CNF[20]+ 19 Reserved CNF[19]+ 18 Enable ROM16 as $\overline{EXBLANK}$ CNF[18]+ 17 Memory Write Control ($\overline{CAS}$ or $\overline{WE}$) CNF[17]+ 16 64K by 16 or 256K by 4 DRAM Select CNF[16]+ 15 EGA SW4/General Purpose CNF[15]+ 14 EGA SW3/General Purpose CNF[14]+ 13 EGA SW2/General Purpose CNF[13]+ 12 EGA SW1/General Purpose CNF[12]+ 11 Select AT/Local Bus Mode CNF[11]+ 10 Set 16-bit ROM CNF[10]* 9 Wakeup I/O Port 3C3h or 46E8h CNF[9]+ 8 Analog/TTL Display CNF[8]* 7 General Purpose CNF[7]* 6 General Purpose CNF[6]* 5 General Purpose CNF[5]* 4 General Purpose CNF[4]* 3 VCLK1, VCLK2 I/O CNF[3]+ 2 Select AT/ MicroChannel Mode CNF[2]+ 1 Select 1 ROM or 2 ROMs CNF[1]* 0 BIOS ROM Mapping CNF[0]* **NOTES:** + = Pulldown resistor sets these bits to 1. * = Pulldown resistor sets these bits to 0. CNF[30:20] have no effect unless Local bus mode is selected. For addition information, refer to the Configuration Register descriptions in Section 9.
RAMDAC Interface (22 Pins)				

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
148 147	BA0 BA1	---	Active High Output	**RAMDAC ADDRESS BUS** A 3-bit wide address bus to read/write the RAMDAC.
145 144 143 142 140 139 138 137	BD7 BD6 BD5 BD4 BD3 BD2 BD1 BD0	---	Active High Input/ Output	**RAMDAC DATA BUS** An 8-bit wide data bus to read/ write the RAMDAC.
171 170 169 168 166 165 164 163	VID7 VID6 VID5 VID4 VID3 VID2 VID1 VID0	---	Active High Output	**VIDEO** Pixel video data output to DAC and to Feature Connector. These lines can drive an up to 8 mA load.
150	$\overline{\text{RPLT}}$	---	Active Low Output	**READ PALETTE** Video DAC register and color palette read signal for an external RAMDAC. Active low during I/O read of addresses 3C6h, 3C8h, and 3C9h.
149	$\overline{\text{WPLT}}$	--	Active Low Output	**WRITE PALETTE** Video DAC register and color palette write signal for an external RAMDAC. Active low during I/O write of addresses 3C6h through 3C9h.
161	PCLK	---	Active High Output	**PIXEL CLOCK** Video pixel clock used by the DAC to latch video signals VID7 through VID0. Its source is one of the video clock inputs (VCLK0, VCLK1, or VCLK2) as selected by the Miscellaneous Output Register.
162	$\overline{\text{BLNK}}$	---	Active Low Output	**BLANK** Active low display monitor blanking pulse to external RAMDAC.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
Clock Selection (4 Pins)				
176	MCLK	---	Active High Input	**MEMORY CLOCK** Provides VGA DRAM and system interface control timing. Should be 37.5 MHz minimum for 80 ns DRAMS.
178	VCLK0	---	Active High Input	**VIDEO CLOCK 0** Provides video display clock for alphanumeric and graphics display modes. Typically, VCLK0 is 25.175 MHz to display 640 pixels per horizontal display line. VCLK0 is selected as the clock when VCLK1 and VCLK2 are used as inputs and Miscellaneous Output register bits 2 and 3 are both set to 0.
179	VCLK1	---	Active High Input/ Output	**VIDEO CLOCK 1** Provides a second video clock input or an output to an external clock selection module. The direction is determined at Reset by a pull-up or pull-down resistor on MD3. Typically, VCLK1 is 28.322 MHz to display 720 pixels per horizontal display line. As an output, VCLK1 is an active low pulse during I/O writes to port 3C2h, or reflects the contents of 3C2h (Miscellaneous Output Register, bit 2). For addition information, refer to the Configuration Register and PR15 register bit 5 descriptions.
180	VCLK2	---	Active High Input/ Output	**VIDEO CLOCK 2** Provides a third video clock input or an output to an external clock selection module. The direction is programmed simultaneously with VCLK1. VCLK2 performs as a user-defined external clock input, an output reflecting the state of PR2 register bit 1, or reflects the contents of port 3C2h (Miscellaneous Output Register, bit 2). For addition information, refer to the Configuration Register and PR15 register bit 5 descriptions.
User Program (2 Pins)				
183 184	USR1 USR0	---	Active High Output	**USER PROGRAMMABLE OUTPUTS** Either or both outputs may be used to control a system feature of special device.
Feature Connector (2 Pins)				
152	$\overline{\text{EXVID}}$	---	Active Low Input	**ENABLE EXTERNAL VIDEO DATA** A feature connector input. A low tristates video data lines VID7:0. An internal pullup resistor is provided.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
182	$\overline{\text{EXPCLK}}$	---	Active Low Input	**ENABLE EXTERNAL PIXEL CLOCK** A feature connector input. A low tristates the PLCK output. An internal pullup resistor is provided.
CRT Control (3 Pins)				
136	HSYNC	---	Active High Input/ Output	**HORIZONTAL SYNC** Display monitor horizontal synchronization pulse. Active high or low depending upon the Miscellaneous Output Register programming.
135	VSYNC	---	Active High Input/ Output	**VERTICAL SYNC** Display monitor vertical synchronization pulse. Active high or low depending upon the Miscellaneous Output Register programming.
151	MDET	---	Active High Input	**MONITOR DETECT** When the RAMDAC is external, MDET is used to determine the monitor type. MDET can be read at port 3C2h, bit 4.
Host CPU Bus Interface (80 Pins)				
93 92 91 90 89 88 87 86	A31 A30 A29 A28 A27 A26 A25 A24	LOC	Active High Input	**SYSTEM ADDRESS BUS BIT 31 THROUGH 24** Address Bus bits 31 through 24 for the 32-bit Local bus interface. These pins are not connected for either AT or MicroChannel bus compatible systems.
84 83 82 81 79 78 77	A23 A22 A21 A20 A19 A18 A17	LOC	Active High Input	**SYSTEM ADDRESS BUS BITS 23 THROUGH 17** Address Bus bits 23 through 17 for the 32-bit Local bus interface.
		AT		**SYSTEM ADDRESS BUS BITS 23 THROUGH 17** For the AT bus, A17 through A23 are connected to LA23 through LA17 to provide a 24-bit AT address bus.
		MC		**SYSTEM ADDRESS BUS BITS 23 THROUGH 17** For the MicroChannel bus, A17 through A23 are connected to SA23 through SA17 to provide a 24-bit MicroChannel address bus.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
76 74 73 72 71 70 69 68 67 65 64 63 62 61 60	A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2	---	Active High Input	**SYSTEM ADDRESS BUS BITS 16 THROUGH 2** Address Bus bits 16 through 2 for all bus operating modes.
56	A1	AT, MC	Active High Input	**SYSTEM ADDRESS BUS BIT 1** For AT and MicroChannel bus mode operation, A1 provides Address Bus bit 1.
	$\overline{BE2}$	LOC	Active Low Input	**BYTE ENABLE 2** In Local bus mode, $\overline{BE2}$ provides Byte Enable for data bits D23 through D16.
58	A0	AT	Active High Input	**SYSTEM ADDRESS BUS BIT 0** For AT bus mode operation, A0 provides Address Bus bit 0.
	$\overline{BLE}$	MC	Active Low Input	**BYTE LOW ENABLE** For MicroChannel bus mode operation, this line is connected to the $\overline{BLE}$ line from the CPU to enable the low byte for data transfers.
	$\overline{BE0}$	LOC	Active Low Input	**BYTE ENABLE 0** In Local bus mode, $\overline{BE0}$ provides Byte Enable for data bits D7 through D0.
57	$\overline{BE1}$	LOC	Active Low Input	**BYTE ENABLE 1** In Local bus mode, $\overline{BE1}$ provides Byte Enable for data bits D15 through 8.
	$\overline{BHE}$	AT, MC		**BYTE HIGH ENABLE** For AT and MicroChannel bus mode operation, this line is connected to the $\overline{BHE}$ line from the CPU to enable the high byte for data transfers.
55	$\overline{BE3}$	LOC	Active Low Input	**BYTE ENABLE 3** In Local bus mode, $\overline{BE2}$ provides Byte Enable for data bits D31 through D24. Not used in AT or MicroChannel modes.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
45	ADS	LOC	Active High Input	**ADDRESS DATA STROBE** Local bus address data strobe connected to the ADS pin on the CPU.
	ALE	AT		**ADDRESS LATCH ENABLE** In AT mode, A23 through A17 (LA23:LA17) are latched internally at the falling edge of ALE.
	ALD	MC		**ADDRESS LATCH** In MicroChannel mode, this signal is not used and should be tied high.
51	M/$\overline{IO}$	LOC, MC	Active High or Low Input	**MEMORY or I/O CYCLE** Indicator for memory or I/O cycle. Low indicates I/O cycle; high indicates memory cycle. In MicroChannel mode, indicator for memory or I/O cycle. Low indicates I/O cycle; high indicates memory cycle.
	$\overline{MRD}$	AT	Active Low Input	**MEMORY READ** In AT mode, $\overline{MRD}$ is the memory read strobe.
52	D/$\overline{C}$	LOC	Active High or Low Input	**DATA or COMMAND CYCLE** Data or command cycle indicator. Low indicates command cycle; high indicates a data cycle.
	$\overline{MWR}$	AT	Active Low Input	**MEMORY WRITE** In AT mode, $\overline{MWR}$ is the memory write strobe.
	$\overline{S0}$	MC	Active Low Input	**STATUS 0** In MicroChannel mode, $\overline{S0}$ is a channel status signal that indicates the start and type of a channel cycle. The $\overline{S0}$, $\overline{S1}$, M/$\overline{IO}$, and $\overline{CMD}$ signals are decoded to interpret I/O and memory commands.
50	W/$\overline{R}$	LOC	Active High or Low Input	**WRITE or READ CYCLE** Write or read cycle indicator. Low indicates a read cycle; high indicates a write cycle.
	$\overline{IOR}$	AT	Active Low Input	**I/O READ** **In AT mode, $\overline{IOR}$ provides an I/O read strobe.**
	$\overline{S1}$	MC	Active Low Input	**STATUS 1** In MicroChannel mode, $\overline{S1}$ is a channel status signal that indicates the start and type of a channel cycle. The $\overline{S0}$, $\overline{S1}$, M/$\overline{IO}$, and $\overline{CMD}$ signals are decoded to interpret I/O and memory commands.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
38	HRQ	LOC	Active High Input	**HOLD REQUEST** Indicates that a system bus request was received via a REFRESH, DMA, or MASTER signal. The processor responds by asserting a HOLD ACKNOWLEDGE after relinquishing the bus.
	$\overline{IOW}$	AT	Active Low Input	**I/O WRITE** In AT mode, $\overline{IOW}$ provides an I/O write strobe.
	$\overline{CMD}$	MC	Active Low Input	**COMMAND** In MicroChannel mode, $\overline{CMD}$ is the bus data strobe. $\overline{CMD}$ low indicates address bus validity and the rising edge of $\overline{CMD}$ indicate the end of a MicroChannel bus cycle.
43	LCLK	LOC	Active High Input	**PROCESSOR CLOCK** Normal clock input from 80486; for 80386, this is CPU-CLK2, which the WD90C33 divides internally to drive other logic.
	$\overline{EIO}$	AT	Active Low Input	**ENABLE I/O** In AT mode, $\overline{EIO}$ enables address decoding and is connected to AEN (address Enable).
	3C3D0	MC	Active High Input	**PORT 3C3h** In MicroChannel mode, when I/O port 3C3h bit 0 is set to 1, it enables video subsystem memory and I/O address decoding.
54	$\overline{SYSRESET}$	LOC	Active Low Input	**SYSTEM RESET** For local bus, MCLK and VCLK0 must be connected to initialize the WD90C33 during power-on and reset. Western Digital configuration bits are initialized at power-on and reset, based on the logic levels of display memory data bits MD31 through MD0 bus, as determined by pullup and pulldown resistors. The reset pulse width should be at least 10 MCLK clock periods.
	RSET	AT, MC	Active High Input	**SYSTEM RESET** For AT and MicroChannel bus operation, MCLK and VCLK0 must be connected to initialize the WD90C33 during power-on and reset. Western Digital configuration bits are initialized at power-on and reset, based on the logic levels of display memory data bits MD19 through MD0 bus, as determined by pullup and pulldown resistors. The reset pulse width should be at least 10 MCLK clock periods.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
95 96 97 98 100 101 102 103 105 106 107 108 110 111 112 113	D31 D30 D29 D28 D27 D26 D25 D24 D23 D22 D21 D20 D119 D18 D17 D16	LOC, AT	Active High Input/ Output	**DATA BUS BITS 31 THROUGH 16** System data lines connect to host CPU data bus D[31:16]. In AT mode, the BIOS EPROM can be connected to this bus. Then, the BIOS data will be sent to the host via D[15:0] D[31:16} are not used for MicroChannel bus operations.
115 116 117 118 120 121 122 123 125 126 127 128 130 131 132 133	D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	---	Active High Input/ Output	**DATA BUS BITS 15 THROUGH 0** System data lines connect to the host CPU or system data bus D[15:0].
49	LDEV	LOC	Active High Output	**LOCAL BUS VGA CYCLE** Active low to indicate a local bus VGA cycle. System controllers should not respond to this cycle.
	$\overline{\text{MEMCS16}}$	AT	Active Low Output	**MEMORY CHIP SELECT, 16 BITS** In AT mode, $\overline{\text{MEMCS16}}$ indicates to the host that the WD90C33 is ready to perform a requested 16-bit video memory data transfer.
	$\overline{\text{CDDS16}}$	MC	Active Low Input	**CHANNEL SELECT, 16 BITS** In MicroChannel mode, $\overline{\text{CDDS16}}$ indicates a 16-bit video memory or I/O access.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
47	BOFF	LOC	Active High Output	**BOFF** Connects to the 80486 BOFF# pin. When active low, the 80486 retracts its last cycle and enables other masters to control the local bus. Its operation is similar to a read cycle for the VGA when the write buffers are full.
	$\overline{\text{ROM16}}$	AT	Active Low Output	**BIOS ROM SELECT, 16 BITS** In AT mode, $\overline{\text{ROM16}}$ decodes ROM address (LA23-LA17) for space 0C0000h through 0DFFFFh. Also, it can be combined externally with A16 and A15 to control $\overline{\text{MEMCS16}}$ for address space C0000h through C7FFFh. If CNF(17) is set to at power-up/reset, the $\overline{\text{ROM16}}$ address decoding is disabled. Then, $\overline{\text{ROM16}}$ reflects the status of PR1 register bit 16.
	$\overline{\text{CSFB}}$	MC	Active Low Input	**CARD SELECT FEEDBACK** In Microchannel mode, $\overline{\text{CSFB}}$ acknowledges that the WD90C33 is present at the specified host address.
39	CPURESET	LOC	Active High Input	**CPU RESET** Provides a synchronous reset to the CPU, and is used to generate an internal CLK to maintain phase of CLK2 in sync with 80386dx and 80386sx CPUs.
	EMEM	AT, MC		**ENABLE MEMORY** In AT and MicroChannel mode, EMEM enables memory decoding. Normally it is connected to REFRESH.
37	LDEVBUSY	LOC	Active High Output	**VIDEO LOCAL BUS BUSY** When an external RAMDAC exists on the AT bus, or a monochrome interface card in installed on the AT bus, the writing cycle for these devices is passed to the AT bus. Then, the AT controller is expected to terminate the cycle. The write cycle is also sent to the local bus VGA, where LDEVBUSY is asserted until the write data are captured.
	$\overline{\text{0WS}}$	AT, MC	Active Low Output	**ZERO WAIT STATE** In AT and MicroChannel mode, $\overline{\text{0WS}}$ is asserted to generate a zero wait state. It is controlled by PR33 register bits 7 and 6. Refer to the PR33 description for additional information.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
46	$\overline{\text{VGARDY}}$	LOC	Active Low Output	**VGA READY** Ready signal to host CPU. This signal can be connected directly to the ready input of the CPU or connected in combination with other local bus slaves. When not active, this signal is tristated.
	IOCHRDY	AT, MC	Active High Output	**I/O CHANNEL READY** In AT and MicroChannel mode, IOCHRDY indicates to the host processor that the requested memory or I/O access is complete. When IOCHRDY is low, the video controller is not able to immediately complete a requested memory or I/O access and that causes the host processor to wait.
41	RDYIN	LOC	Active High Output	**READY INPUT** For Local bus mode, RDYIN provides the final CPURDY feedback to the WD90C33 to terminate its local bus cycle. The use of RDYIN is optional depending on the setting of Configuration register bit CNF20 as follows: If CNF20 = 0, a Local bus cycle is terminated when $\overline{\text{VGARDY}}$ is active, regardless of the state of RDYIN. If CNF20 = 1, a Local bus cycle is terminated when RDYIN provides the final CPURDY feedback.
	$\overline{\text{IOCS16}}$	AT	Active Low Output	**I/O CHIP SELECT, 16 BITS** In AT mode, $\overline{\text{IOCS16}}$ indicates to the host that the WD90C33 is ready to perform a requested 16-bit I/O accesses.
	$\overline{\text{CDSETUP}}$	MC	Active Low Input	**CHANNEL SETUP** In MicroChannel Mode, $\overline{\text{CDSETUP}}$ is driven by the host to individually select channel connector slots during system configuration.
40	$\overline{\text{EBROM}}$	---	Active Low Output	**ENABLE BIOS ROM** Active low to enable BIOS ROM (C0000h through C7FFFh) if enabled by PR1 register, bit 0. A write to WD90C33 internal I/O port 46E8h causes $\overline{\text{EBROM}}$ to be used as a write strobe for an external register used in BIOS ROM page mapping.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
44	$\overline{IRQ}$	LOC, AT	Active Low Output	**INTERRUPT REQUEST** For Local and AT bus modes, IRQ provides a programmable interrupt request to the host CPU. The interrupt request is enable by Vertical Retrace End Register, bit 5. When the end of vertical display occurs, this signal is active, requesting an interrupt, and it stays active until cleared by CRTC11 register bit 4.
	$\overline{IRQ}$	MC	Active Low Output	**INTERRUPT REQUEST** For MicroChannel bus mode, operation is the same as is Local and AT bus modes except that an active low IRQ is used.
Power Distribution				
13 24 42 53 80 104 109 119 129 141 167 181 185 197 208	VCC	---	---	**+5 VDC** Power supply pins.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
7 18 30 36 48 59 66 76 85 94 99 114 124 134 146 160 172 177 191 202	GND	---	---	**GR0UND** Power return pins.
Unused Connections (10 Pins)				
153 154 155 156 157 158 159 173 174 175	No Connection	---	---	These pins are not connected to internal circuits of the WD90C33 controller.

TABLE 4-2 SIGNAL DESCRIPTIONS

4.4 HOST INTERFACE PIN MULTIPLEXING

Table 4-3 lists the WD90C33 connector pins that have more than one signal mnemonic depending on the host system bus structure where the video controller is used.

PIN NO.	SIGNAL MNEMONICS		
	LOCAL BUS INTERFACE	AT BUS	MICROCHANNEL BUS
37	LDEVBUSY	$\overline{0WS}$	$\overline{0WS}$
38	HRQ	$\overline{IOW}$	$\overline{CMD}$
39	CPURESET	EMEM	EMEM
40	$\overline{EBROM}$,	$\overline{EBROM}$	$\overline{EBROM}$
41	RDYIN	$\overline{IOCS16}$	$\overline{CDSETUP}$
43	LCLK	$\overline{EIO}$	3C3D0
44	IRQ	IRQ	$\overline{IRQ}$
45	$\overline{ADS}$	ALE	$\overline{ALD}$
46	$\overline{VGARDY}$	IOCHRDY	IOCHRDY
47	$\overline{BOFF}$	$\overline{ROM16}$	$\overline{CSFB}$
49	$\overline{LDEV}$	$\overline{MEMCS16}$	$\overline{CDDS16}$
50	W/$\overline{R}$	$\overline{IOR}$	$\overline{S1}$
51	M/$\overline{IO}$	$\overline{MRD}$	M/$\overline{IO}$
52	D/$\overline{C}$	$\overline{MWR}$	$\overline{S0}$
54	$\overline{SYSRESET}$,	RSET	RSET
55	$\overline{BE}$3	Not Used	Not Used
56	$\overline{BE}$2	A1]	A1
57	$\overline{BE}$1	$\overline{BHE}$	$\overline{BHE}$
58	$\overline{BE}$0	A0	$\overline{BLE}$
76, 74-67, 65-60	A[31:24]	Not Used	Not Used
84-81, 79-77	A[23:2]	A[23:2]	A[23:2]
95-98, 100-101, 105-108,110-118	D[31:16]	D[31:16]	Not Used
115-118, 120-123, 125-128, 130-133	D[15:0]	D[15:0]	D[15:0]

TABLE 4-3 HOST INTERFACE PIN MULTIPLEXING