# *WD83C691A Manchester Encoder/ Decoder (MED)*

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# 1.0 INTRODUCTION

## 1.1 DESCRIPTION

The Manchester Encoder/Decoder (MED) consists of balanced drivers and receivers, an on-board crystal oscillator, a signal translator, and a diagnostic loopback circuit. Manufactured using CMOS silicon gate technology, the device is functionally compatible with the National DP8391 Serial Network Interface (SNI).

The WD83C691A is part of a three-device set that implements the complete IEEE 802.3-compatible network node electronics (see Figure 1-1). The WD83C690 Ethernet LAN Controller (ELC) and the WD83B692 Ethernet Transceiver (ET) comprise the other two devices in the set. The WD83C690 provides media access protocol functions and performs buffer management tasks, while the WD83B692 serves as a coaxial cable line driver/receiver and collision detector.

The WD83C691A Manchester Encoder/Decoder provides the interface between the WD83C690 ELC and the WD83B692 ET. When transmitting, the device converts non-return-to-zero (NRZ) data from the controller into Manchester encoded data, then sends the data to the transceiver. When receiving, the device reverses the process using an analog phase-locked loop that decodes 10 Mbit/sec signals with up to 18 nsec of jitter.

This document describes the operation of the WD83C691A Manchester Encoder/Decoder, and provides information on the following functional blocks:

- Oscillator
- Manchester Encoder and Differential Driver
- Manchester Decoder
- Collision Translator
- Loopback Capabilities

The appendices provide pin designations, electrical operating and switching characteristics, and timing and package diagrams.

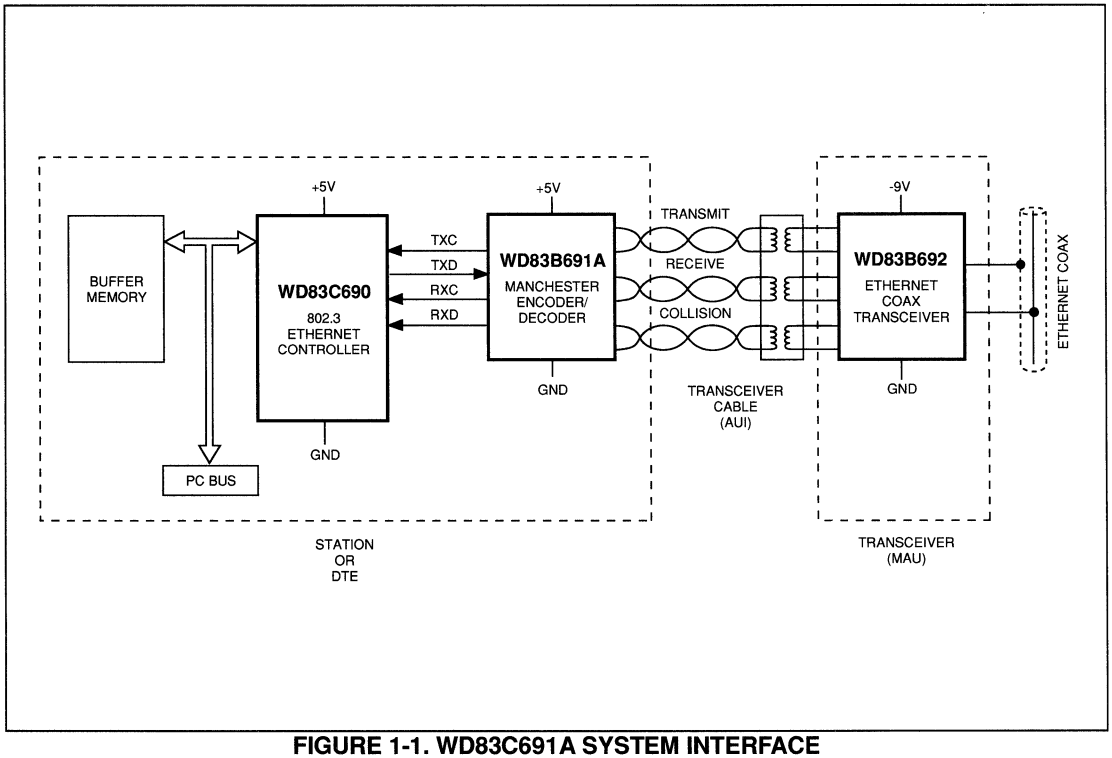


**FIGURE 1-1. WD83C691A SYSTEM INTERFACE**

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## 1.2 FEATURES

- Compatible with Ethernet II (10BASE5) and Cheapernet (10BASE2) IEEE 802.3 standards
- Incorporates low power, 1.25 CMOS technology
- Provides 10 Mbps Manchester encoding/ decoding with receive clock recovery
- Connects directly to the transceiver (AUI) cable
- Provides 16V fault protection at the transceiver interface
- TTL/MOS-compatible controller interface
- Features externally-selectable half- or full-step modes of operation at transmit output
- Incorporates squelch circuits at receive and collision inputs to reject noise
- Provides loopback capability for diagnostics

## 2.0 OPERATIONAL DESCRIPTION

This section describes the five basic components of the WD83C691A.

### 2.1 Oscillator

Control is provided either by a 20 MHz, parallel resonant crystal connected between X1 and X2, or by an external clock connected at X1. The oscillator's 20-MHz output is divided in half to generate the 10-MHz transmit clock for the Ethernet LAN controller and to provide the internal clock signals for the encoding and decoding circuits.

The IEEE 802.3 standard requires 0.01% absolute accuracy on the transmitted signal frequency. Stray capacitance, however, can shift the crystal's frequency out of range, causing it to exceed the 0.01% tolerance. To remedy this, you may need to add extra load capacitance.

To determine the amount of capacitance to add, measure the board capacitance and the capacitance between the X1 and X2 pins. Then add these values together, and subtract them from the crystal's required load capacitance. (Refer to Figure 2-2.)

### 2.2 Manchester Encoder/Differential Driver

Data encoding and transmission begin when the transmit enable input (TXE) goes high, and continue as long as the TXE remains high. It is essential that the transmit enable and transmit data inputs meet the setup and hold time requirements in relation to the rising edge of the transmit clock. Transmission ends when the transmit enable input goes low. The last transition occurs at the center of the bit cell if the last bit is one, or at the boundary of the bit cell if the last bit is zero.

The differential line driver, which has the ability to drive up to 50 meters of twisted pair AUI/ Ethernet transceiver cable, provides the emitter-coupled logic (ECL) level signals. The outputs consist of current drivers that must be loaded with external 1602 pull-down resistors.

With the SEL input, one of two modes can be selected, full-step or half-step. When SEL is low, TX+ is positive in relation to TX- in the idle state. When SEL is high, TX+ and TX- are equal in the idle state. Figures C1 through C3 illustrate transmit timing.

### 2.3 Manchester Decoder

Decoding is accomplished by a differential input receiver circuit and an analog phase-locked loop that separate the Manchester-encoded data stream into clock signals and NRZ data. With the standard 782 transceiver drop cable, the differential input must be externally terminated. This requirement can be satisfied by connecting two 392 resistors in series with one optional common mode bypass capacitor.

To prevent noise at the input from falsely triggering the decoder, a squelch circuit rejects signals with pulse widths less than 20 nsec (negative going), or with levels less than -175 mV. When the input exceeds the squelch requirements, the analog phase-locked loop locks onto the incoming signal and the WD83C691A decodes a data frame. The carrier sense (CRS) is activated, and the receive data (RXD) and receive clock (RXC) become available within five bit times. At the end of a frame, when the normal mid-bit transition on the differential input ceases, carrier sense is deactivated. The receive clock remains active for an additional six bit times before subsiding. Figures C-4 through C-6 illustrate receive timing.

### 2.4 Collision Translator

The Ethernet transceiver detects collisions on the coaxial cable and generates a 10-MHz signal, which is monitored by the WD83C691A through the collision detect pins. The presence of the signal activates the collision detect (CD) pin connected to the WD83C690, and causes the controller to stop transmitting. The collision detect output is deactivated within 350 nsec after the absence of the 10-MHz signal. (Figure C-7 illustrates the collision timing.) Make sure that the collision differential inputs are terminated in exactly the same manner as the receive inputs.

## 2.5 Loopback Functions

A logic "1" on the loopback input causes the WD83C691A to send serial data from the transmit data input through the encoder, and back through the phase-locked loop decoder to receive the output data. The transmit driver is in the idle state during loopback mode and the receiver circuitry is disabled.

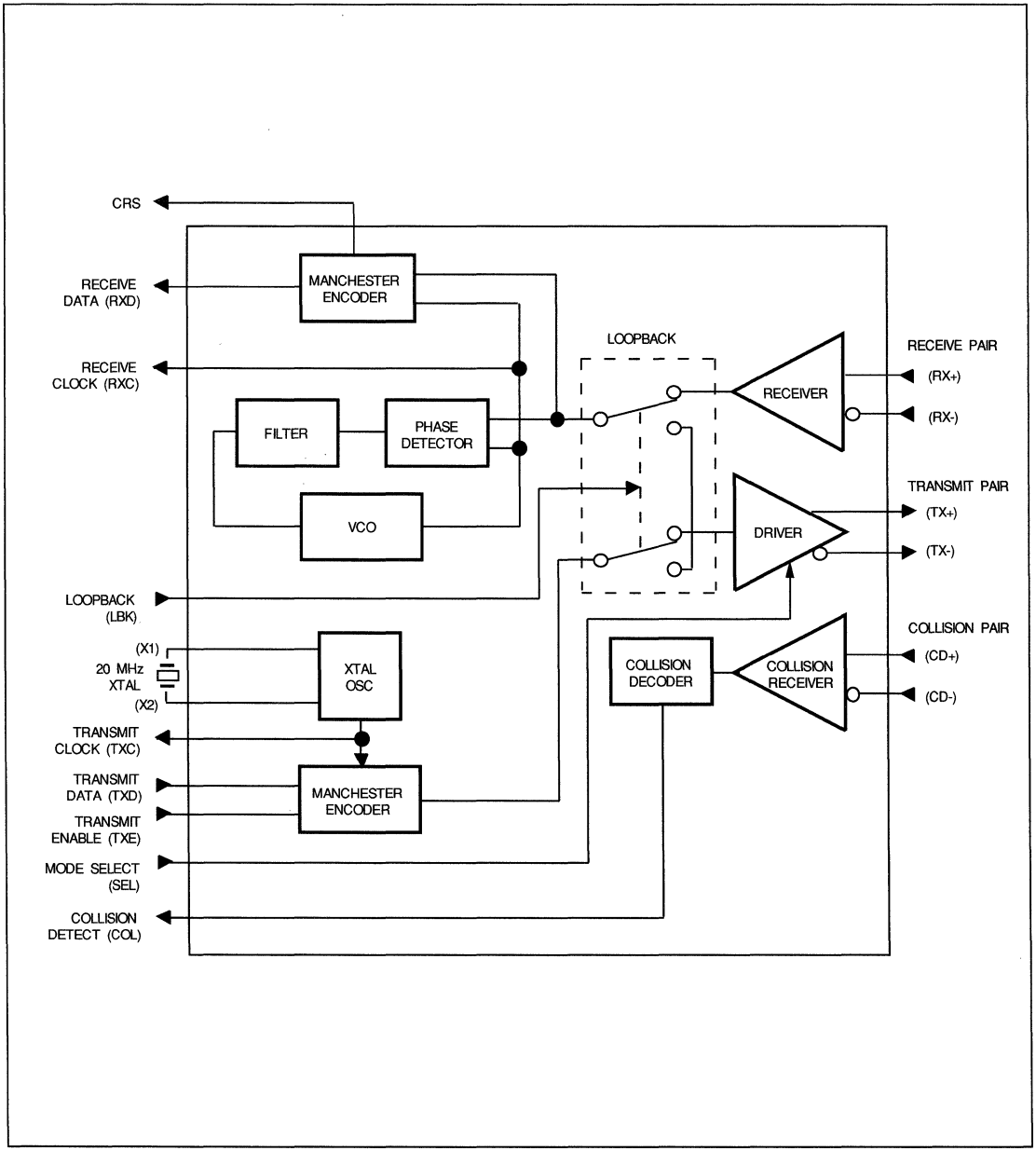
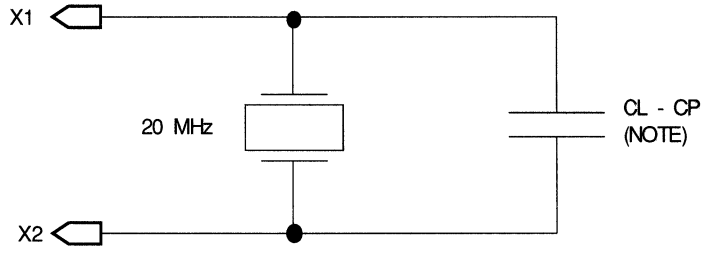



**FIGURE 2-1. WD83C691A GENERAL SYSTEM BLOCK DIAGRAM**

## 2.6 CRYSTAL SPECIFICATIONS

| | |
|---|---|
| Resonant Frequency: | 20 MHz |
| Overall Tolerance: | 0.005% at 25°C (77°F) |
| Type: | AT-Cut |
| Temperature Tolerance: | 0.005% 0°C (32°F) to 70°C (158°F) |
| Circuit Type: | Parallel resonance (refer to Figure 2-2 for crystal connection diagram). |




CL = Load capacitance specified by crystal manufacturer.

CP= Total parasitic capacitance including:
a) WD83C691A input capacitance between X1 and X2 (typically 5 pF).
b) PC board traces, plated through holes, socket capacitances.

NOTE:
No external shunt capacitance (CL) is required if the crystal capacitance plus the parasitic capacitance matches the capacitance required to stabilize the crystal frequency.

**FIGURE 2-2. CONNECTION DIAGRAM**

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## APPENDIX A -- PIN DESIGNATIONS

This Appendix provides information on the 24-Pin DIP and 28-Pin PLCC devices. Figures A-1 andA-2 depict the devices, and Table A-1 lists all pin designations.

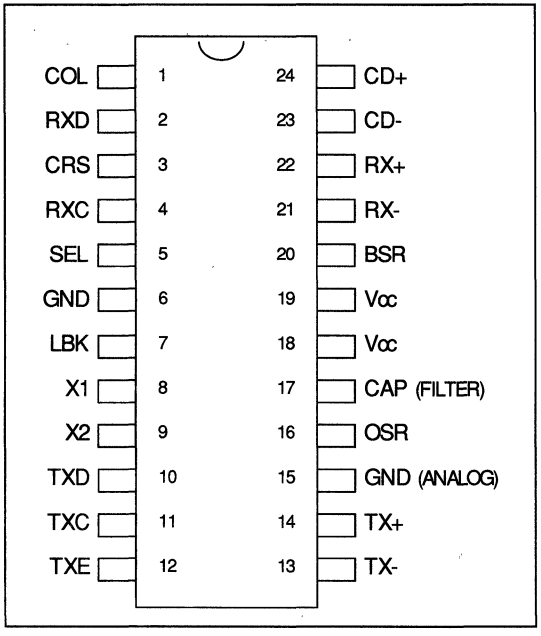


**FIGURE A-1. WD83C691-PG 24-Pin DIP Manchester Encoder/Decoder**

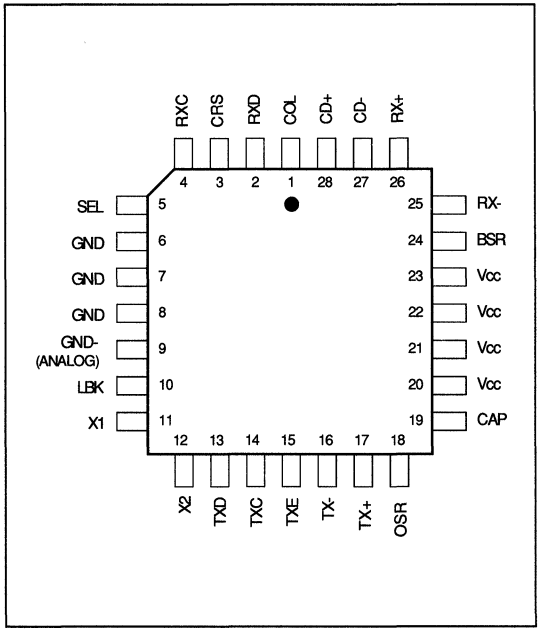


**FIGURE A-2. WD83C691-JH 28-Pin PLCC Manchester Encoder/Decoder**

| DIP PINS | PLCC PINS | MNEMONIC | SIGNAL NAME | DESCRIPTION/FUNCTION |
|---|---|---|---|---|
| 1 | 1 | COL | COLLISON DETECT OUTPUT | TTL/MOS level active high output. A 10-MHz signal at the collision input produces a logic high at COL output. When there is no signal at the collision input, COL output is low. |
| 2 | 2 | RXD | RECEIVE DATA OUTPUT | TTL/MOS level output. This is the NRZ data from the analog phase-locked loop. This signal is sampled by the controller at the rising edge of the receive clock. |
| 3 | 3 | CRS | CARRIER SENSE | TTL/MOS level active high output. The output is activated when there is valid data from the transceiver at the receive input. It is deactivated two bit times after the last bit at receive point. |
| 4 | 4 | RXC | RECEIVE CLOCK | TTL/MOS level recovered clock output. When the analog phase-locked loop locks to a valid incoming signal, a 10-MHz clock signal is activated on this output, which remains low during idle (5 bit times after activity ceases at receive input.) |
| 5 | 5 | SEL* | MODE SELECT | When high, the TX+ and TX- outputs have the same voltage in idle state, providing a "zero" differential. When low, TX+ is positive with respect to TX- in idle state. |
| 6 | 6-8 | GND | GROUND | |
| 7 | 10 | LBK | LOOPBACK | TTL/MOS level active high on this input enables the loopback mode. |
| 8 | 11 | X1 | CRYSTAL1 | Crystal or external frequency source input (TTL). |
| 9 | 12 | X2 | CRYSTAL FEEDBACK OUTPUT | This output is used only in the crystal connection, and must be left open when driving X1 with an external frequency source. |
| 10 | 13 | TXD | TRANSMIT DATA | TTL/MOS level input. When transmit enable input is high, this signal is sampled by the WD83C691A at the rising edge of the transmit clock. The WD83C691A combines transmit data and transmit clock signals to produce a Manchester-encoded bit stream, which is sent differentially to the transceiver. |

**TABLE A-1. PIN DESCRIPTIONS**

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| DIP PINS | PLCC PINS | MNEMONIC | SIGNAL NAME | DESCRIPTION/FUNCTION |
|---|---|---|---|---|
| 11 | 14 | TXC | TRANSMIT CLOCK | Derived from the 20-MHz oscillator, This TTL/MOS level 10-MHz clock output is always active. |
| 12 | 15 | TXE | TRANSMIT ENABLE | TTL/MOS level active high data encoder enable input, sampled by the WD83C691A at the rising edge of the transmit clock. |
| 13,14 | 16,17 | TX-,TX+ | TRANSMIT OUTPUT | These outputs are current drivers and require 160 ± 5.0% Ohm pull-down resistors to GND. |
| 15 | 9 | GND | GROUND | System analog ground. |
| 16 | 18 | OSR | VCO RESISTOR | A 31.6 ± 1.0% Kbyte, bias oscillator resistor connected between this pin and a VCC pin. |
| 17 | 19 | CAP | FILTER CAPACITOR | A ceramic capacitor must be connected from this output pin to ground as close to the part as possible. The capacitor must be .01μ F ± 10%. |
| 18,19 | 20-23 | VCC | VCC | +5V positive supply pins. A 0.1μ F ceramic decoupling capacitor must be connected across VCC and GND, as close to the device as possible. |
| 20 | 24 | BSR | BIAS RESISTOR | A 10.0 ± 1.0% Kbyte bias resistor connects beween this pin and a VCC pin. |
| 21,22 | 25,26 | RX-,RX+ | RECEIVE INPUT | Differential receive input pair from the transceiver. |
| 23,24 | 27,28 | CD-,CD+ | COLLISION OUTPUT | Differential collision input pair from transceiver. |

**TABLE A-1. PIN DESCRIPTIONS, Continued**

*SEL is not a TTL/MOS level input. The VCO frequency can be observed at RXC when SEL is forced to one-half Vcc (for test purposes).



## APPENDIX B -- ELECTRICAL OPERATING CHARACTERISTICS

Ta = 0°C (32°F) to 70°C (158°F), Vcc = +5V ±5% (Refer to note after table)

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage (TTL and X1) | 2.0 | - | V | |
| $V_{IH}$ | Input High Voltage (SEL) | 4.0 | - | V | - |
| $V_{IL}$ | Input Low Voltage (TTL and X1) | - | 0.8 | V | - |
| $V_{IL}$ | Input Low Voltage (SEL) | - | 1.0 | V | - |
| $I_{IH}$ | Input High Current (TTL)<br>Input High Current (RX±, CD±) | -<br>- | 10<br>10 | µA<br>µA | Vin = Vcc<br>Vin = Vcc |
| $I_{IL}$ | Input Low Current (TTL)<br>Input Low Current (RX±, CD±) | -<br>- | -10<br>-500 | µA<br>µA | Vin = 0.5V<br>Vin = 0.5V |
| $V_{CL}$ | Input Clamp Voltage (TTL) | - | -1.2 | V | Iin = -12mA |
| $V_{OH}$ | Output High Voltage (TTL/MOS) | 3.5 | - | V | Ioh = -100 µA |
| $V_{OL}$ | Output Low Voltage (TTL/MOS) | - | 0.5 | V | Iol = 8mA |
| $i_{CS}$ | Output Short Circuit Current (TTL/MOS) | -40 | -200 | mA | - |
| $V_{OD}$ | Differential Output Voltage (TX±) | ±450 | ±120 | mV | 78Ω termination and 200Ω from each to ground |
| $V_{OB}$ | Differential Output Voltage Imbalance (TX±) | - | ±40 | mV | 78Ω termination and 200Ω from each to ground |
| $V_{DS}$ | Differential Squelch Threshold (RX± CD±) | -175 | -300 | mV | - |
| $V_{CM}$ | Input Common Mode Voltage (RX± CD±) | 0 | 7.0 | V | - |
| $i_{CC}$ | Power Supply Current | - | 80 | mA | 10 Mbit/sec |

**TABLE B-1. ELECTRICAL OPERATING CHARACTERISTICS**

NOTE: All currents into device pins are positive. All currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

All typical values are given for Vcc = 5V and Ta = 25°C (77°F)

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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage (Vcc) | 6V |
| TTL Input Voltage | 0 - 5.5V |
| Differential Input Voltage | -5.5 - 16V |
| Differential Output Voltage | 0 - 16V |
| Differential Output Current | -40 mA |
| Storage Temperature | -65°C (-85°F) to 150° (302°F) |

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not recommended; operation should be limited to conditions specified under DC Operating Characteristics.

## RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| Supply Voltage (Vcc) | 5V ±5% |
| Ambient Temperature | 0°C (32°F) to 70°C (158°F) |

## APPENDIX C -- SWITCHING CHARACTERISTICS

Ta = 0°C (32°F) to 70°C (158°F), Vcc = +5V ±5% (Refer to note after table)

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **Oscillator Specification** | | | | | |
| $t_{XTH}$ | X1 to Transmit Clock High | 8 | - | 20 | nsec |
| $t_{XTL}$ | X1 to Transmit Clock Low | 8 | - | 20 | nsec |
| **Transmit Specification** | | | | | |
| $t_{TCD}$ | Transmit Clock Duty Cycle at 1.5V (10 MHz) | 42 | 50 | 58 | % |
| $t_{TCR}$ | Transmit Clock Rise Time (1.1V to 2.9V) | - | - | 10 | nsec |
| $t_{TCF}$ | Transmit Clock Fall Time (2.9V to 1.1V) | - | - | 10 | nsec |
| $t_{TDS}$ | Transmit Data Setup Time to Transmit Clock Rising Edge | 20 | - | - | nsec |
| $t_{TDH}$ | Transmit Data Hold Time from Transmit Clock Rising Edge | 0 | - | - | nsec |
| $t_{TES}$ | Transmit Enable Setup Time to Transmit Clock Rising Edge | 20 | - | - | nsec |
| $t_{TEH}$ | Transmit Enable Hold Time from Transmit Clock Rising Edge | 0 | - | - | nsec |
| $t_{TOD}$ | Transmit Output Delay from Transmit Clock Rising Edge | - | - | 40 | nsec |
| $t_{TOR}$ | Transmit Output Rise Time (20% to 80%) | - | - | 7 | nsec |
| $t_{TOF}$ | Transmit Output Fall Time (80% to 20%) | - | - | 7 | nsec |
| $t_{TOJ}$ | Transmit Output Jitter | - | ±0.25 | - | nsec |
| $t_{TOH}$ | Transmit Output High Before Idle in Half Step Mode | 200 | - | - | nsec |
| $t_{TOI}$ | Transmit Output Idle Time in Half Step Mode | - | - | 800 | nsec |
| **Receive Specification** | | | | | |
| $t_{RCD}$ | Receive Clock Duty Cycle at 1.5V (10 MHz) | 40 | 50 | 60 | % |
| $t_{RCR}$ | Receive Clock Rise Time (1.1V to 2.9V) | - | - | 10 | nsec |
| $t_{RCF}$ | Receive Clock Fall Time (2.9V to 1.1V) | - | - | 8 | nsec |

**TABLE C-1. SWITCHING CHARACTERISTICS**

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| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **Receive Specification, continued** | | | | | |
| $t_{RDR}$ | Receive Data Rise Time (20% to 80%) | - | - | 8 | nsec |
| $t_{RDF}$ | Receive Data Fall Time (80% to 20%) | - | - | 8 | nsec |
| $t_{RDS}$ | Receive Data Stable From Receive Clock Rising Edge | 40 | - | - | nsec |
| $t_{CSON}$ | Carrier Sense Turn on Delay | - | - | 50 | nsec |
| $t_{CSOFF}$ | Carrier Sense Turn off Delay | - | - | 160 | nsec |
| $t_{DAT}$ | Decoder Acquisition Time | - | - | 700 | nsec |
| $t_{DREJ}$ | Differential Inputs Rejection Pulse Width (Squelch) | 8 | - | 30 | nsec |
| $t_{RD}$ | Receive Throughout Delay | - | - | 150 | nsec |
| **Collision Specification** | | | | | |
| $t_{COLON}$ | Collision Turn On Delay | - | - | 50 | nsec |
| $t_{COLOFF}$ | Collision Turn Off Delay | - | - | 350 | nsec |
| **Loopback Specification** | | | | | |
| $t_{LBS}$ | Loopback Setup Time | 20 | - | - | nsec |
| $t_{LBH}$ | Loopback Hold Time | 0 | - | - | nsec |

**TABLE C-1. SWITCHING CHARACTERISTICS, Continued**

NOTE: All typical values are given for Vcc = 5V and Ta = 25°C (77°F).

## TIMING DIAGRAMS

Table C-2 lists all timing diagrams. Figures C-1 through C-9 illustrate all timings.

| Figure Number | Title |
|---|---|
| C-1 | Transmit Timing -- Start of Transmission |
| C-2 | Transmit Timing -- End of Transmission (last bit = 0) |
| C-3 | Transmit Timing -- End of Transmission (last bit = 1) |
| C-4 | Receive Timing -- Start of Packet |
| C-5 | Receive Timing -- End of Packet (last bit = 0) |
| C-6 | Receive Timing -- End of Packet (last bit = 1) |
| C-7 | Collision Timing |
| C-8 | Loopback Timing |
| C-9 | Test Loads |

**TABLE C-2. WD83C691A TIMING DIAGRAMS**

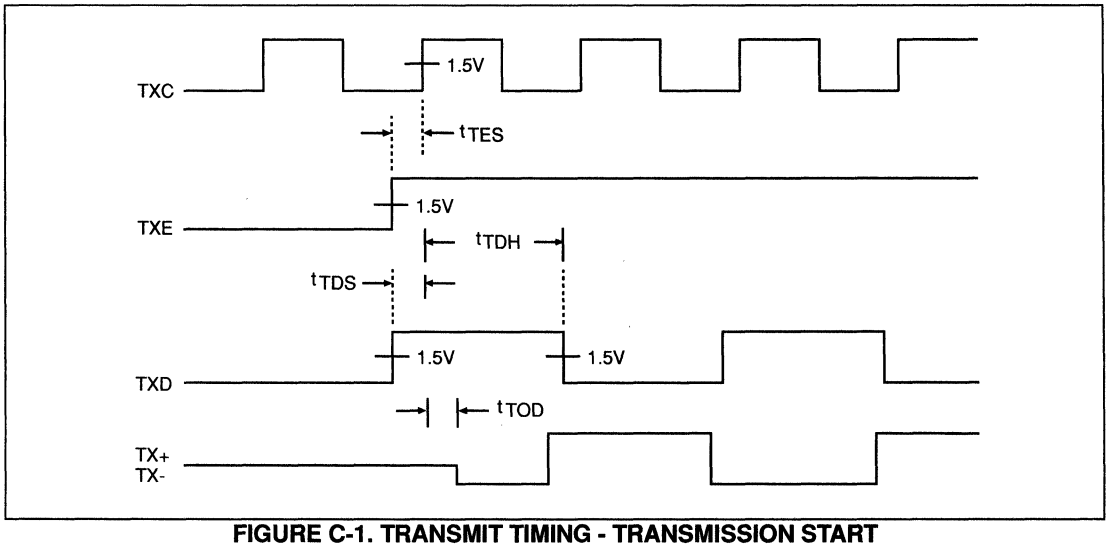


**FIGURE C-1. TRANSMIT TIMING - TRANSMISSION START**

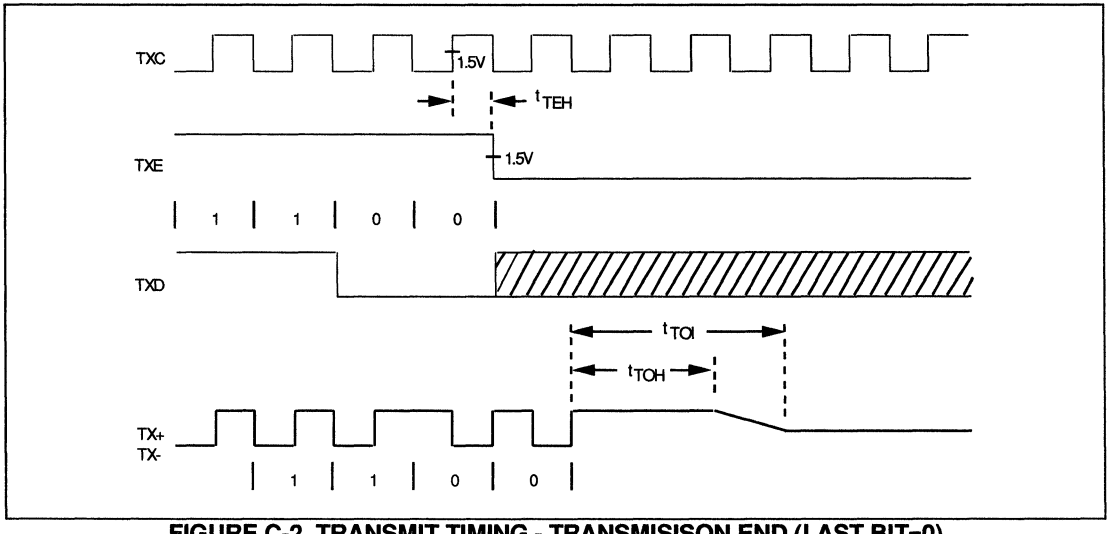


**FIGURE C-2. TRANSMIT TIMING - TRANSMISISON END (LAST BIT=0)**

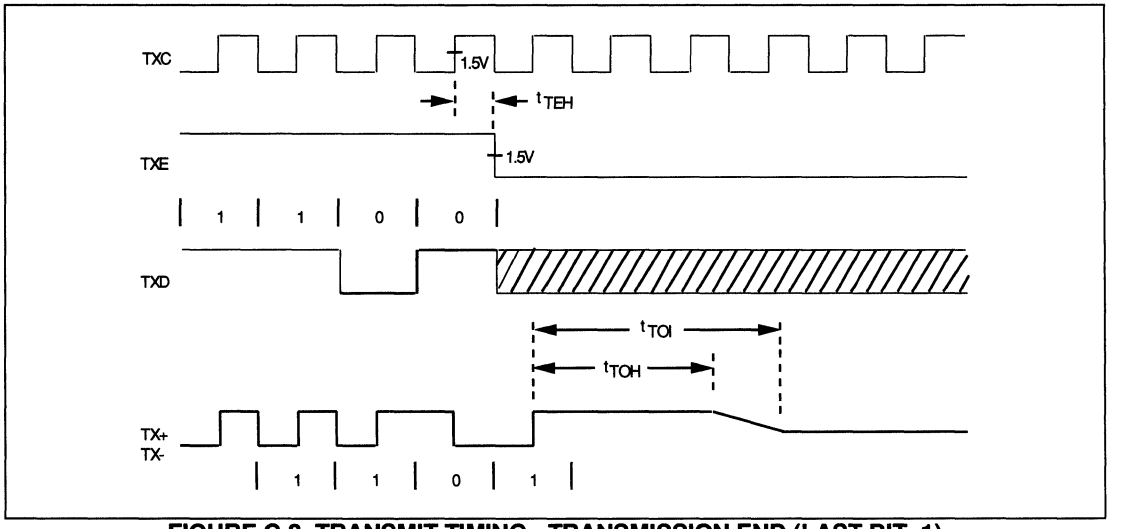


**FIGURE C-3. TRANSMIT TIMING - TRANSMISSION END (LAST BIT=1)**

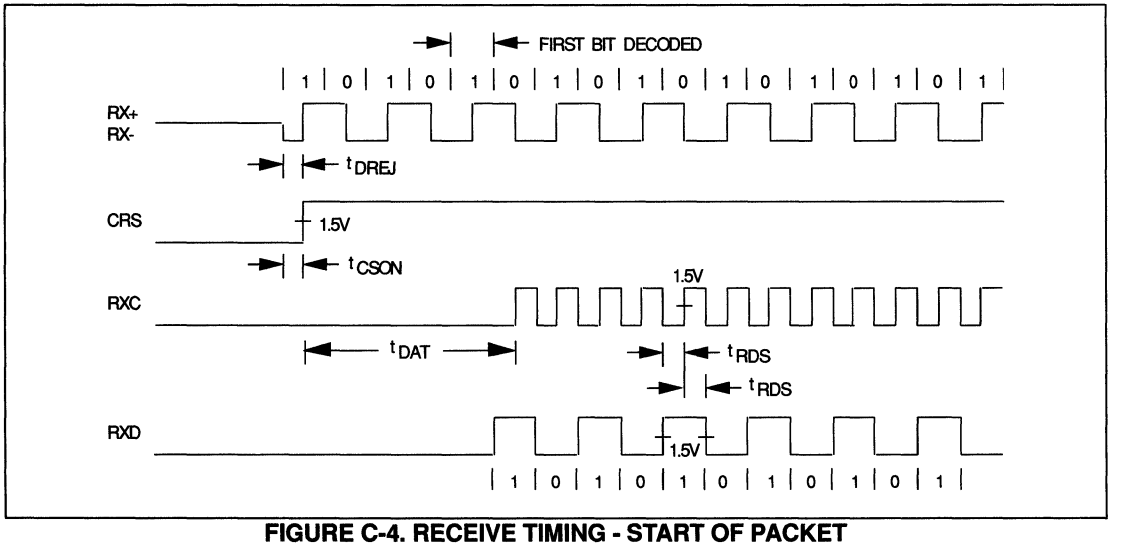


**FIGURE C-4. RECEIVE TIMING - START OF PACKET**

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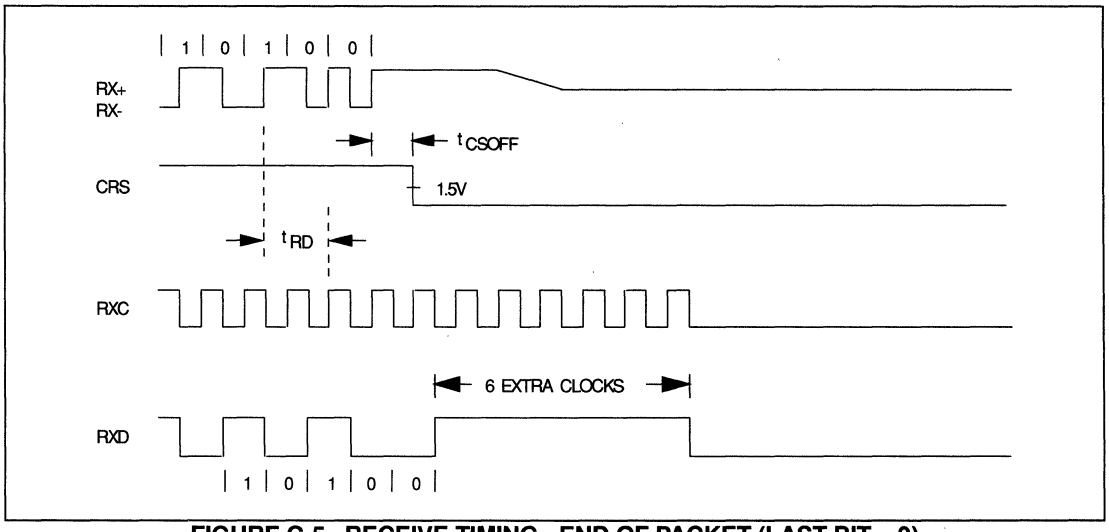


**FIGURE C-5. RECEIVE TIMING - END OF PACKET (LAST BIT = 0)**

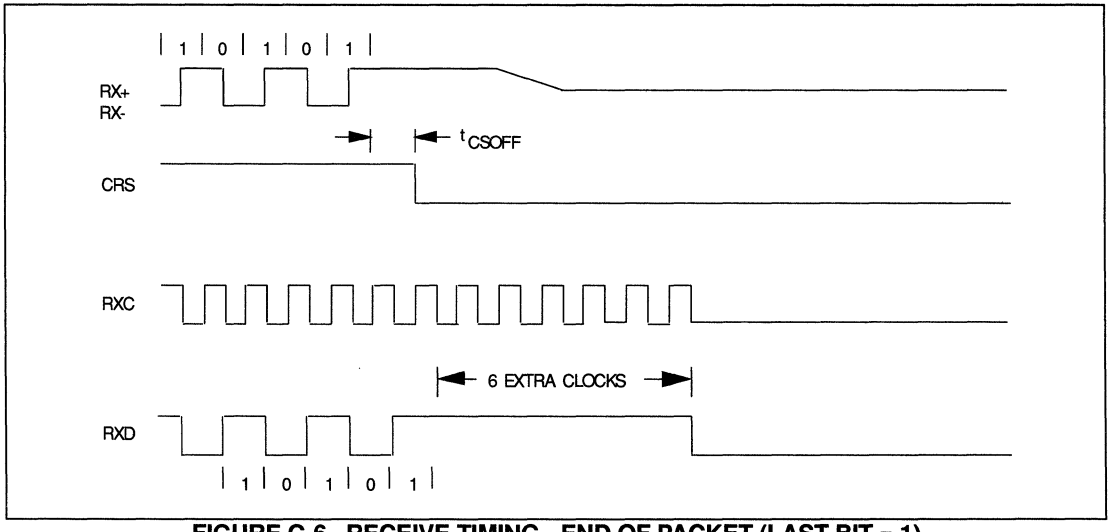


**FIGURE C-6. RECEIVE TIMING - END OF PACKET (LAST BIT = 1)**

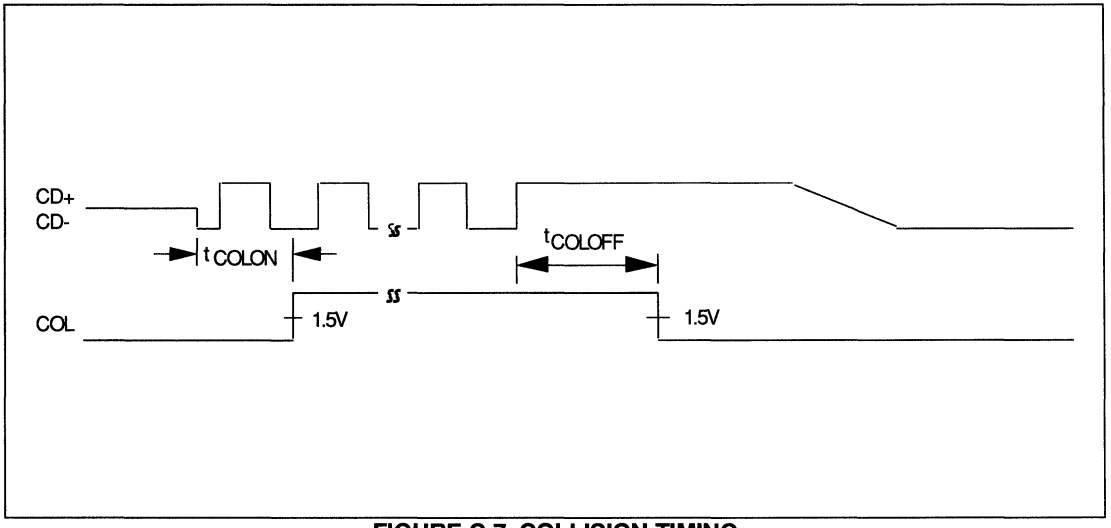


**FIGURE C-7. COLLISION TIMING**

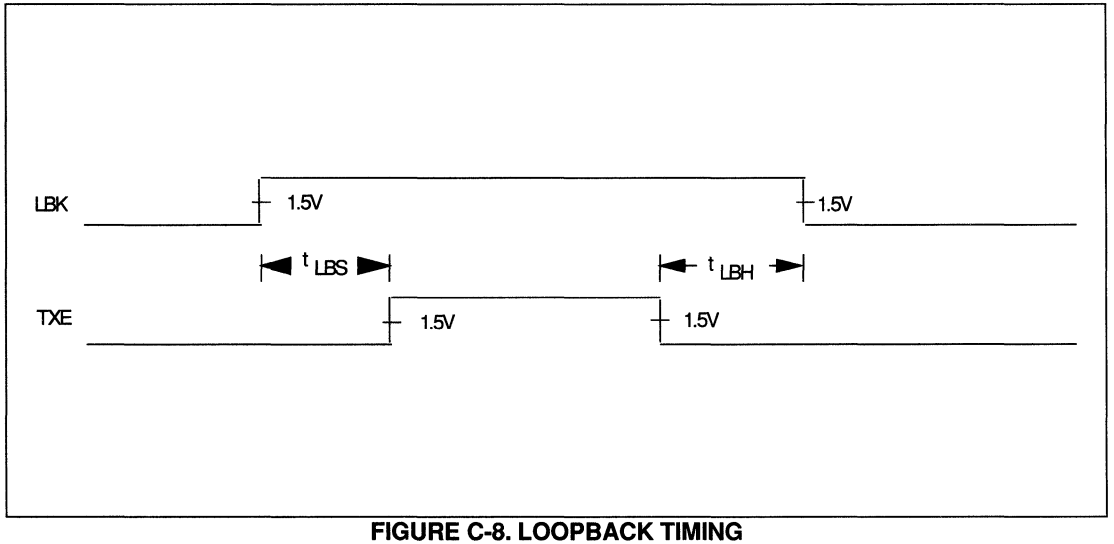


**FIGURE C-8. LOOPBACK TIMING**

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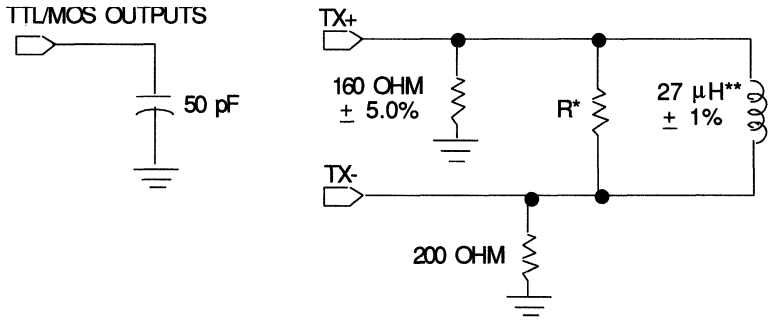


* R = 73 OHM ± 1% and
R = 83 OHM ± 1%

** 27 µH ± 1% inductor is used for test purposes. 100 µH transformers (Valor LT 1101, or Pulse Engineering 64103) are recommended for application use.

**FIGURE C-9. TEST LOADS**

## APPENDIX D - PACKAGE DIAGRAMS

Figures D-1 and D-2 are illustrations of the 24-Pin DIP and 28-Pin PLCC packages showing dimensions in inches.

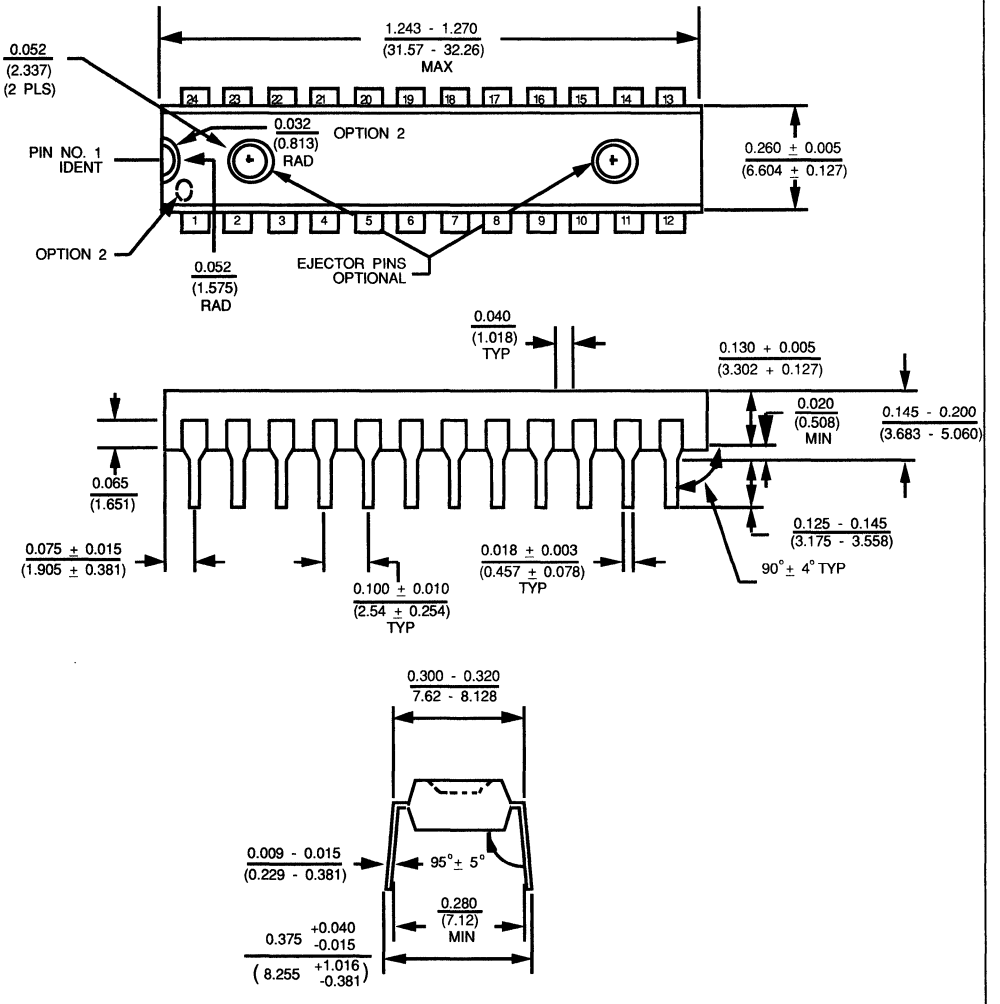


**FIGURE D-1. 24-PIN DIP PACKAGE DRAWING**

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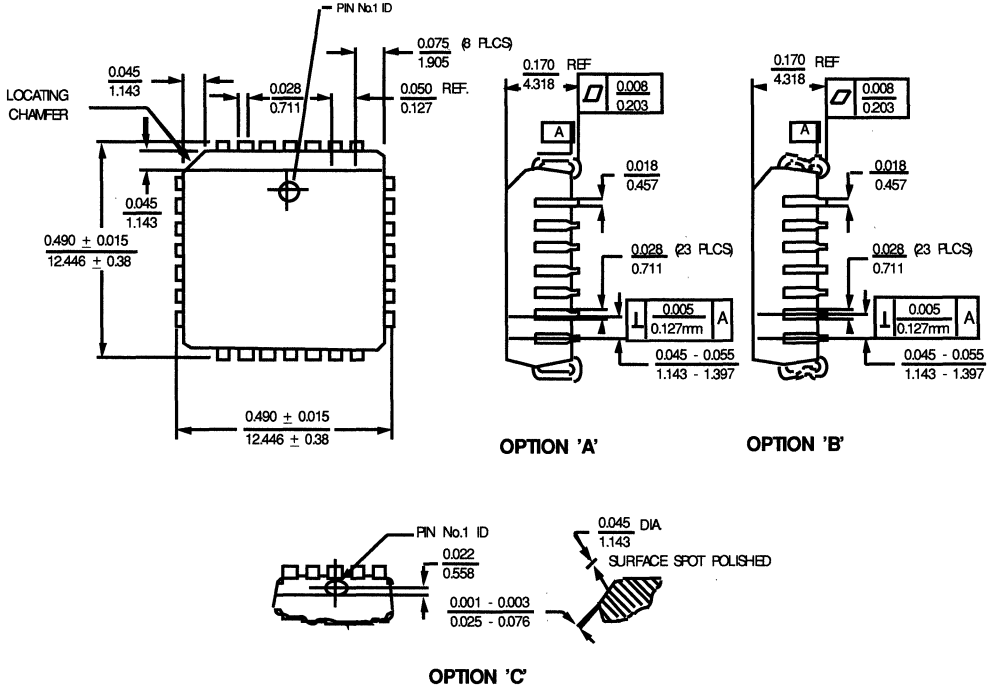


**FIGURE D-2. 28-PIN PLCC PACKAGE DRAWING**