

FE3010C
AT Peripheral
Control Device



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1.0 INTRODUCTION

1.1 DESCRIPTION

As part of the Western Digital® FE3600B and FE3600C chip sets, the FE3010C AT Peripheral Control Device allows designers to build PC/AT Bus compatible single board computers that will operate at speeds from 10 MHz to 20 MHz with an 80286, or 16 or 20 MHz with an 80386SX processor.

The FE3010C is typically used in conjunction with the FE3001 (AT CPU Control Device), the FE3021 (AT Address Buffer and Memory Control Device), and the FE3031 (Data Buffer Device). Doing so allows you to reduce the size of an 80286 or 80386SX-based PC/AT compatible system board by 80%, power by 70%, and component count by 62%.

The FE3010C contains the functional equivalent of two 8237 DMA Controllers in cascade mode. This block improves the performance of a system by allowing external devices to transfer data directly from the system's memory. The FE3010C also contains the functional equivalent of two

8259 interrupt controllers in cascade mode. Additional features include 15 interrupt channels, 3 timer channels, 7 DMA channels, DMA page registers, 8 MHz DMA, and TTL compatibility.

1.2 FEATURES

- Hardware and software compatible with the IBM AT
- 15 interrupt channels
- 3 timer channels
- 7 DMA channels
- TTL compatible
- DMA clock rate up to 8 MHz
- Refresh circuitry for 256 Kbyte or 1 Mbyte DRAMs
- DMA page registers
- 1.25 Micron HCMOS technology
- 84-Pin PLCC

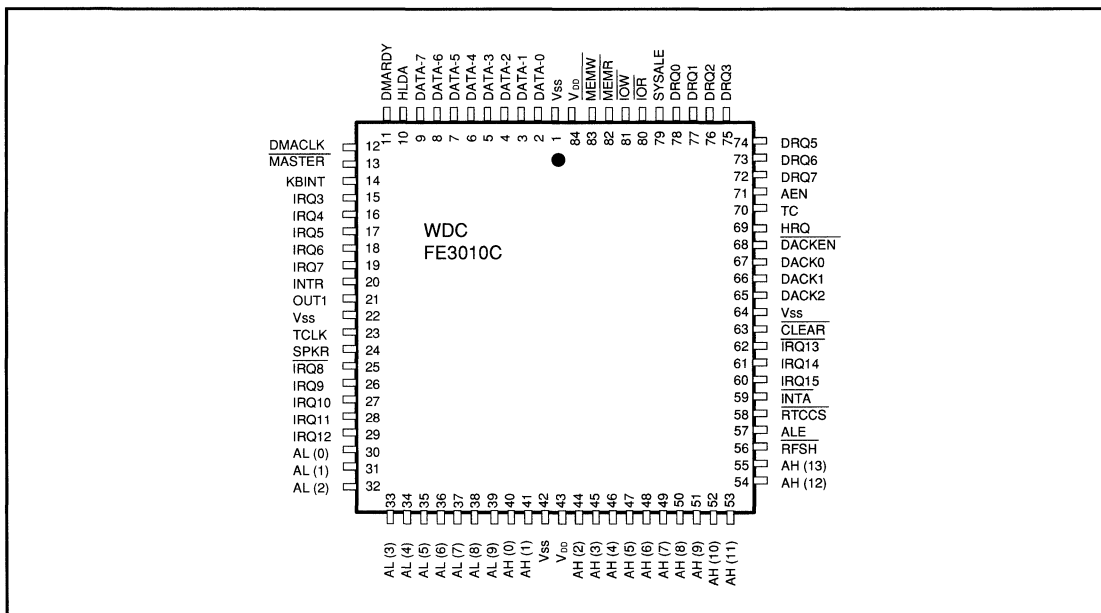


FIGURE 1-1. FE3010C PIN LOCATIONS



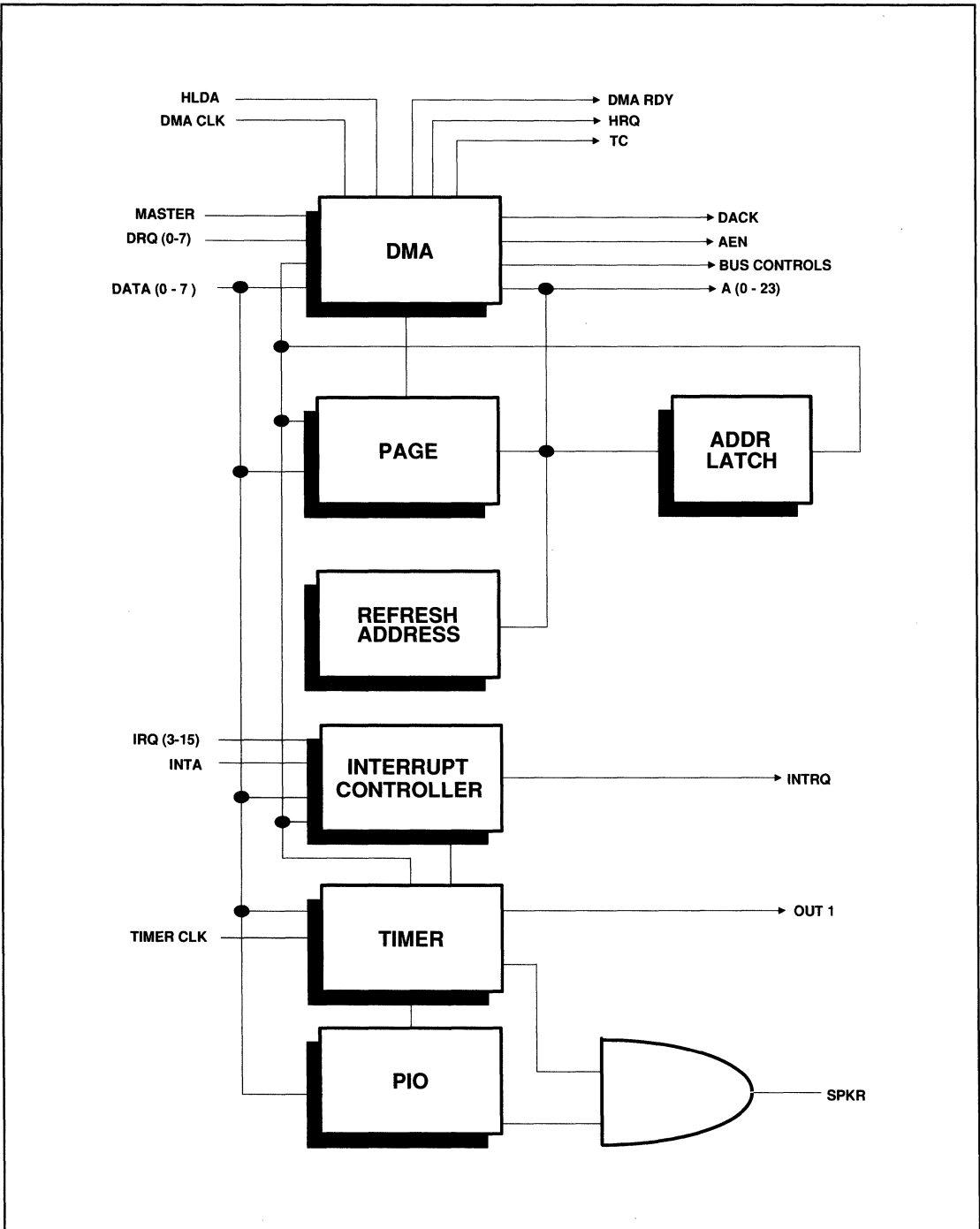


FIGURE 1-2. FE3010C FUNCTIONAL BLOCK DIAGRAM



PIN	TYPE	SYMBOL	FUNCTION
1		VSS	GROUND
2	I/O	DATA(0)	DATA BIT 0
3	I/O	DATA(1)	DATA BIT 1
4	I/O	DATA(2)	DATA BIT 2
5	I/O	DATA(3)	DATA BIT 3
6	I/O	DATA(4)	DATA BIT 4
7	I/O	DATA(5)	DATA BIT 5
8	I/O	DATA(6)	DATA BIT 6
9	I/O	DATA(7)	DATA BIT 7
10	I	HLDA	HOLD ACKNOWLEDGE Active high. Acknowledge from the CPU (80286) for a request for the bus from the DMA controller.
11	I	DMARDY	DMA READY Active high Signal to indicate that the DMA may complete its current cycle.
12	I	DMACLK	DMA CLOCK System clock/ DMACLK 6 MHz / 3 or 6 MHz 8 MHz / 4 or 8 MHz 10 MHz / 5 MHz
13	I	MASTER	BUS MASTER Active low Signal indicating a master on the expansion bus has bus control.
14	I	KBINT	KEYBOARD INTERRUPT Active high
15	I	IRQ3	INTERRUPT REQUEST 3 Active high
16	I	IRQ4	INTERRUPT REQUEST 4 Active high
17	I	IRQ5	INTERRUPT REQUEST 5 Active high
18	I	IRQ6	INTERRUPT REQUEST 6 Active high
19	I	IRQ7	INTERRUPT REQUEST 7 Active high
20	O	INTR	INTERRUPT REQUEST TO CPU (80286) Active high
21	O	OUT1	TIMER CHANNEL 1 OUTPUT
22		Vss	GROUND

TABLE 1-1. PIN ASSIGNMENT INFORMATION



PIN	TYPE	SYMBOL	FUNCTION
23	I	TCLK	TIMER CLOCK (1.19 MHz clock for timer)
24	O	SPKR	SPEAKER DATA
25	I	$\overline{\text{IRQ8}}$	INTERRUPT REQUEST 8 Active low
26	I	IRQ9	INTERRUPT REQUEST 9 Active high
27	I	IRQ10	INTERRUPT REQUEST 10 Active high
28	I	IRQ11	INTERRUPT REQUEST 11 Active high
29	I	IRQ12	INTERRUPT REQUEST 12 Active high
30-39	I/O	AL(0-9)	ADDRESS BIT 0-9
NOTE			
All addresses sent to the FE3010C during CPU cycles are latched with ALE except for A0. This allows compatibility for 16-bit writes to the FE3010C, although 8-bit accesses are preferred. A0 is latched in the FE3001, so no external latch on A0 is necessary if an FE3001 is used with the FE3010C.			
40	O	AH(0)	ADDRESS BIT 10
41	O	AH(1)	ADDRESS BIT 11
42		V _{SS}	GROUND
43		V _{DD}	+5 VOLTS SUPPLY
44	O	AH(2)	ADDRESS BIT 12
45	O	AH(3)	ADDRESS BIT 13
46	O	AH(4)	ADDRESS BIT 14
47	O	AH(5)	ADDRESS BIT 15
48	O	AH(6)	ADDRESS BIT 16
49	O	AH(7)	ADDRESS BIT 17
50	O	AH(8)	ADDRESS BIT 18
51	O	AH(9)	ADDRESS BIT 19
52	O	AH(10)	ADDRESS BIT 20
53	O	AH(11)	ADDRESS BIT 21
54	O	AH(12)	ADDRESS BIT 22

TABLE 1-1. PIN ASSIGNMENT INFORMATION, CONTINUED



PIN	TYPE	SYMBOL	FUNCTION
55	O	AH(13)	ADDRESS BIT 23
56	I	$\overline{\text{RFSH}}$	REFRESH ADDRESS Active low Signal to enable the refresh address to the address bus during a RAM refresh cycle.
57	I	ALE	ADDRESS LATCH ENABLE Active high
58	O	$\overline{\text{RTCCS}}$	REAL TIME CLOCK CHIP SELECT
59	I	$\overline{\text{INTA}}$	INTERRUPT ACKNOWLEDGE FROM CPU (80286) Active low Interrupt acknowledge to the interrupt controllers
60	I	IRQ15	INTERRUPT REQUEST 15 Active high
61	I	IRQ14	INTERRUPT REQUEST 14 Active high
62	I	$\overline{\text{IRQ13}}$	INTERRUPT REQUEST 13 Active low Error interrupt from (80287)
63	I	$\overline{\text{CLEAR}}$	SYSTEM CLEAR Active low
64		V _{ss}	GROUND
65	O	DACK2	DMA ACKNOWLEDGE BIT 2
DACK2	DACK1	DACK0	DMA Channel Acknowledge
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	illegal
1	0	1	5
1	1	0	6
1	1	1	7
66	O	DACK1	DMA ACKNOWLEDGE BIT 1
67	O	DACK2	DMA ACKNOWLEDGE BIT 0
68	O	DACKEN	DMA ACKNOWLEDGE ENABLE Active low Signal to enable DACK0, DACK1, and DACK2 decode.

TABLE 1-1. PIN ASSIGNMENT INFORMATION, CONTINUED



PIN	TYPE	SYMBOL	FUNCTION
69	O	HRQ	DMA REQUEST TO CPU (80286) Active high
70	O	TC	DMA END OF OPERATION Active high Signal to indicate the DMA controller has finished its cycle.
71	O	AEN	DMA AEN Active high Signal to indicate that the current bus is a DMA cycle.
72	I	DRQ7	CHANNEL 7 DMA REQUEST Active high
73	I	DRQ6	CHANNEL 6 DMA REQUEST Active high
74	I	DRQ5	CHANNEL 5 DMA REQUEST Active high
75	I	DRQ3	CHANNEL 3 DMA REQUEST Active high
76	I	DRQ2	CHANNEL 2 DMA REQUEST Active high
77	I	DRQ1	CHANNEL 1 DMA REQUEST Active high
78	I	DRQ0	CHANNEL 0 DMA REQUEST Active high
79	O	SYSALE	SYSTEM ALE Active high Signal to latch the address in the address latch.
80	I/O	$\overline{\text{IOR}}$	$\overline{\text{I/O READ COMMAND}}$ Active low
81	I/O	$\overline{\text{IOW}}$	$\overline{\text{I/O WRITE COMMAND}}$ Active low
NOTE			
Data must be valid before $\overline{\text{IOW}}$ to the FE3010C goes low because the leading edge of $\overline{\text{IOW}}$ is used to clock some registers in the FE3010C. This setup time (data valid to $\overline{\text{IOW}}$ active low) is specified at 30 ns minimum.			
82	O	$\overline{\text{MEMR}}$	$\overline{\text{MEMORY READ COMMAND}}$ Active low
83	O	$\overline{\text{MEMW}}$	$\overline{\text{MEMORY WRITE COMMAND}}$ Active low
84		V _{DD}	+5 VOLTS SUPPLY

TABLE 1-1. PIN ASSIGNMENT INFORMATION, CONTINUED



2.0 DMA CONTROL

2.1 OVERVIEW

The FE3010C contains two 8237 equivalent DMA controllers. DMA controller #1 is in the I/O address space from 000 to 00F and is used for 8-bit transfers. DMA controller #2 is in the I/O space from 0C0 to 0DE and is used for 16-bit transfers. Channel 0 of DMA controller #2 is used to cascade DMA controller #1.

AT Bus DMA Channel	DMA Controller	Transfer Type
0	#1 Channel 0	8-bit
1	#1 Channel 1	8-bit
2	#1 Channel 2	8-bit
3	#1 Channel 3	8-bit
4	#2 Channel 0	Cascade DMA Cont. #1
5	#2 Channel 1	16-bit
6	#2 Channel 2	16-bit
7	#2 Channel 3	16-bit

TABLE 2-1. DMA TRANSFER TYPES

2.2 TRANSFER MODES

Each DMA channel may be programmed in Single Transfer Mode, Block Transfer Mode, Demand Transfer Mode, or Cascade Mode.

2.2.1 Single Transfer Mode

In single transfer mode the channel will make one transfer for each request. The word count will be decremented, and the address will be incremented or decremented at the end of each transfer. When the word count goes from 0000 to FFFF, a terminal count (TC) will be generated. To start a transfer, the DRQ should be held active high until a DACK is received. If the DRQ is held active through the cycle, only one transfer will take place. The DRQ must go low and then high to start another transfer. The bus will be released between transfers.

2.2.2 Block Mode Transfer

A transfer is started in block mode by a DRQ and continues until a TC is reached. The DRQ should be held active until DACK becomes active. Block mode should be used with caution since refresh will be locked out. The address and word count behave as in single mode.

2.2.3 Demand Mode

In demand mode, a transfer will continue to take place until DRQ is inactive or a TC is reached. If the DRQ is dropped, the bus will be released. If DRQ is activated again, the transfer will resume. The address and word count behave as in single mode.

2.2.4 Cascade Mode

Cascade mode is used to cascade DMA controller #2 to DMA controller #1, and for bus master transfers. A channel in cascade mode will get the bus when a DRQ is active, but the word count and address are ignored. The IOR, IOW, MEMR, and MEMW signals must be generated by the bus master device. The addresses from the FE3010C are floated when the MASTER signal becomes active.

2.3 TRANSFER TYPES

There are three types of transfers: read, write, and verify.

Read

A read transfers data from memory to an I/O device.

Write

A write transfers data from an I/O device to memory.

Verify

A verify transfer is a pseudo transfer that does not generate IOR, IOW, MEMR, or MEMW signals.



2.4 AUTOINITIALIZE

A channel may be programmed to autoinitialize for any transfer type. In this mode when a TC is reached the channel is loaded with the original word count and address, and is ready to start another transfer.

2.5 PRIORITY

Each DMA controller has two types of priority, fixed and rotating. For fixed priority, channel 0 has the highest priority and channel 3 has the lowest. In rotating priority, the last channel to be serviced has the lowest priority. The DMA controller #2 has priority over the DMA controller #1.

2.6 EXTENDED WRITE

In normal timing the MEMR or IOR pulse is two clock cycles and the MEMW or IOW is one clock cycle. If extended write is selected, the MEMW or IOW will be the same as the MEMR or IOR.

2.7 BASE AND CURRENT ADDRESS REGISTERS

Each channel has a 16-bit base and current address register. The current address register is loaded from the base register when the base register is loaded or when in autoinitialize mode. The current address register is incremented or decremented during a transfer.

Addresses are driven to the bus while $\overline{\text{RFSH}}$ is low, indicating a refresh cycle. Only address bits A23-A16 (from the page register) and bits A10-A0 (from the refresh counter) are meaningful during refresh. The address counter gets incremented on the rising edge of $\overline{\text{RFSH}}$.

2.8 BASE AND CURRENT WORD COUNT

Each channel has a 16-bit base and current word count register. The current word count register is loaded from the base register when the base register is loaded or when in autoinitialize mode. The current word count is decremented during a transfer.

2.9 COMMAND REGISTER WRITE

This register is cleared by a reset or Master Clear command.

0-1	Unused
2	Controller Disable
3	Must be 0 for extended write, otherwise no effect
4	Rotating Priority
5	Extended Write
6-7	Unused

TABLE 2-2. COMMAND REGISTER WRITE FORMAT

2.10 STATUS REGISTER READ

Bits 0-3 are cleared by a reset, a Master Clear command or a status read.

0	Channel 0 has Reached TC
1	Channel 1 has Reached TC
2	Channel 2 has Reached TC
3	Channel 3 has Reached TC
4	Channel 0 DRQ Active
5	Channel 1 DRQ Active
6	Channel 2 DRQ Active
7	Channel 3 DRQ Active

TABLE 2-3. STATUS REGISTER READ FORMAT

2.11 REQUEST REGISTER WRITE

Each channel may be started by a software request. These request are not affected by the mask register. It is cleared by a reset or a Master Clear command.

0-1	Channel Number \Rightarrow	00	Channel 0
2	Request	01	Channel 1
3-7	Unused	10	Channel 2
		11	Channel 3

TABLE 2-4. REQUEST REGISTER WRITE FORMAT



2.12 MASK REGISTER WRITE

Each channel has a mask bit associated with it. If it is set, the channel is disabled. The bits may be set or cleared by software or set by a TC if the channel is not in autoinitialize mode. All the bits are set by a reset or a Master Clear Function.

SINGLE MASK	
0-1	Channel Select
2	Set/Clear Mask (0 = Clear, 1 = Set)
3-7	Unused
CLEAR MASK	
0-7	Unused
MASK ALL	
0	Channel 0 Mask
1	Channel 1 Mask
2	Channel 2 Mask
3	Channel 3 Mask
4-7	Unused

TABLE 2-5. MASK REGISTER WRITE FORMAT

2.13 MODE REGISTER WRITE

0-1	Channel Select ⇒	00 Channel 0
		01 Channel 1
		10 Channel 2
		11 Channel 3
2-3	Transfer Type ⇒	00 Verify
		01 Write
		10 Read
		11 Unused
4	Autoinitialize	
5	Address Decrement	
6-7	Mode ⇒	00 Demand
		01 Single
		10 Block
		11 Cascade

TABLE 2-6. MODE REGISTER WRITE

2.14 CLEAR POINTER WRITE

Each DMA controller has a pointer flip flop that indicates which half of the word count or address is being accessed. Each time a word count or address is written or read, the pointer is toggled. When the flip flop is cleared, bits 0-7 are accessed and when it is set, bits 8-15 are accessed. The pointer may be cleared by writing to the Clear Pointer. Any data is ignored.

2.15 MASTER CLEAR WRITE

A write to the Master Clear will:

1. Clear the Command Register
2. Clear the Status Register
3. Clear the Request Register
4. Set the Mask Register
5. Clear the Pointer Flip Flop

Any data will be ignored.



I/O Address	Read/Write	DMA Controller	Function
000	Read/Write	1	Channel 0 Address
001	Read/Write	1	Channel 0 Word Count
002	Read/Write	1	Channel 1 Address
003	Read/Write	1	Channel 1 Word Count
004	Read/Write	1	Channel 2 Address
005	Read/Write	1	Channel 2 Word Count
006	Read/Write	1	Channel 3 Address
007	Read/Write	1	Channel 3 Word Count
008	Read	1	Status
008	Write	1	Command Register
009	Write	1	Request Register
00A	Write	1	Single Mask
00B	Write	1	Mode Register
00C	Write	1	Clear Pointer
00D	Write	1	Master Clear
00E	Write	1	Clear Mask
00F	Write	1	Mask All
0C0	Read/Write	2	Channel 0 Address
0C2	Read/Write	2	Channel 0 Word Count
0C4	Read/Write	2	Channel 1 Address
0C6	Read/Write	2	Channel 1 Word Count
0C8	Read/Write	2	Channel 2 Address
0CA	Read/Write	2	Channel 2 Word Count
0CC	Read/Write	2	Channel 3 Address
0CE	Read/Write	2	Channel 3 Word Count
0D0	Read	2	Status
0D0	Write	2	Command Register
0D2	Write	2	Request Register
0D4	Write	2	Single Mask
0D6	Write	2	Mode Register
0D8	Write	2	Clear Pointer
0DA	Write	2	Master Clear
0DC	Write	2	Clear Mask
0DE	Write	2	Mask All

TABLE 2-7. DMA CONTROL FUNCTION MAP



3.0 DIFFERENCES BETWEEN THE FE3010C AND 8237

The FE3010C implementation is different from the Intel 8237 in two ways. The DMA address in the 8237 is valid during the entire DMA cycle, while the FE3010C multiplexes the address and transfer count on the address bus. Therefore, addresses A16-A0 from the FE3010C need to be latched with SYSALE coming out from the FE3010C. These latches are in the FE3021.

The second difference is in the cascade mode; the 8237 does not enable the address outputs, while the FE3010C does. Since the only way to use the cascade mode on an AT system is through Bus Master operation, this is not a problem, since the FE3010C disables its address outputs when the MASTER signal becomes active.



4.0 8259 INTERRUPT CONTROLLERS

The FE3010C contains two 8259 equivalent interrupt controllers. Interrupt controller #1 is in the I/O space of 020 to 021, and interrupt controller #2 is in the I/O space of 0A0 to 0A1. Interrupt 2 of interrupt controller #1 is used to cascade interrupt controller #2.

4.1 INTERRUPT SEQUENCE

1. When an interrupt arrives from a peripheral device, the interrupt may be programmed to be level or edge sensitive. In the level mode, the interrupt will keep occurring as long as the interrupt is kept high. In the edge mode, it must go low and high for each interrupt. The interrupt will set the appropriate bit in the Interrupt Request Register (IRR).

System Interrupt	Interrupt Controller	Use
0	#1 Level 0	Timer
1	#1 Level 1	Keyboard
2	#1 Level 2	Cascade
3-7	#1 Level 3 - 7	AT Bus
8	#2 Level 0	R.T.C.
9-12	#2 Level 1-4	AT Bus
13	#2 Level 5	Co-Processor
14-15	#2 Level 6-7	AT Bus

TABLE 4-1. INTERRUPT SEQUENCE FORMAT

2. If the interrupt has not been masked off, it is passed to the priority circuit. There are three types of priority.

Fixed

In fixed priority, interrupt 0 has the highest priority and interrupt 7 has the lowest.

Automatic Rotation

In automatic rotation, the last interrupt serviced has the lowest priority.

Specific Rotation

In this mode, the lowest priority interrupt can be set by software. The next interrupt will have the highest priority. For example if interrupt 4 is set to the lowest level, the priority will be 5, 6, 7, 0, 1, 2, 3, and 4.

3. The interrupt controller sends an IRQ to the CPU.

4. The CPU responds with an INTA cycle that freezes priority.

5. The CPU sends another INTA that causes the interrupt controller to send a vector to the CPU and set the appropriate bit in the Interrupt Service Register (ISR) and clear the corresponding bit in the IRR, if it is in the edge triggered mode. As long as the bit in the ISR is set, all interrupts at the same level or lower will be inhibited unless programmed for special mask mode.

6. An EOI is issued to end the interrupt. This clears the appropriate bit in the Interrupt Service Register. For the slave adapter (interrupt controller #2), two EOI's must be issued. There are three types of EOI's.

Specific

An EOI is issued by software for a specific interrupt.

Non-Specific

A non-specific EOI is issued by software. The hardware will generate a EOI for the highest level active interrupt.

Automatic

An automatic EOI is a non-specific EOI that is caused by the second INTA.

The interrupt controllers may also be operated in a polled mode. In this mode, the CPU is set to disable the interrupt input. In this case, software must issue a poll command. This takes the place of an INTA, and the software can then read the interrupt level to determine the interrupt to be serviced.

When cascading is used and the slave has issued an interrupt, other interrupts from the slave are locked out. If it is desired to preserve priority in the slave (i.e. allow higher interrupts to occur when a lower interrupt is being serviced), Special Fully Nested Mode should be programmed in the master. After a non-specific EOI has been sent to the slave, the ISR should be checked to see if any



other interrupts are active. If there are no interrupts active, a non-specific EOI should be sent to the master.

4.2 SETUP

The interrupt controllers are setup by writing a series of initialization command words (ICW). The sequence is started by writing ICW1 with data bit 4 = 1. ICW2 is then written followed by ICW3 and ICW4 if they are needed.

ICW1 Write	
0	ICW4 Needed
1	Not Cascade Mode
2	Unused
3	Level Triggered
4	1
5-7	Unused
ICW2 Write	
0-2	Unused
3-7	Interrupt Vector
ICW3 Write (Interrupt Controller #1 only)	
0-1	0
2	Interrupt 2 has slave
3-7	0
ICW3 Write (Interrupt Controller #2 only)	
0-2	Slave I/D
3-7	0
ICW4	
0	1
1	Auto EOI
2-3	0
4	Special Fully Nested Mode
5-7	0

TABLE 4-2. ICW FORMATS

4.3 OPERATION

Once the interrupt controllers are setup, they may be programmed by Operation Control Words (OCW).

OCW1	
0	Interrupt 0 Mask
1	Interrupt 1 Mask
2	Interrupt 2 Mask
3	Interrupt 3 Mask
4	Interrupt 4 Mask
5	Interrupt 5 Mask
6	Interrupt 6 Mask
7	Interrupt 7 Mask
OCW2	
0-2	Interrupt Level
3-4	0
5-7 ⇒ 001	Non-specific EOI
011	Specific EOI
111	Rotate on Specific EOI
101	Rotate on Non-Specific EOI
100	Select Rotate on Automatic EOI
000	Clear Rotate On Automatic EOI
110	Set Priority
010	Unused

TABLE 4-3. OCW FORMATS

4.3.1 OCW3

Bits 0, 1, and 2 of OCW3 determine what the next read of the interrupt controller will yield.

0-1 ⇒ 00	Unused
01	Unused
10	Select Read IRR
11	Select Read ISR
2	Poll Command
3	1
4	0
5-6 ⇒ 00	Unused
01	Unused
10	Reset Special Mask Mode
11	Set Special Mask Mode
7	0

TABLE 4-4. OCW3 FORMATS



Interrupt Controller	Address	Function	Read/Write
1	020	ICW1	Write
1	021	ICW2	Write
1	021	ICW3	Write
1	021	ICW4	Write
1	021	OCW1	Write
1	020	OCW2	Write
1	020	OCW3	Write
1	020	IRR	Read
1	020	ISR	Read
1	021	Mask	Read
1	020, 021	Interrupt Level	Read
2	0A0	ICW1	Write
2	0A1	ICW2	Write
2	0A1	ICW3	Write
2	0A1	ICW4	Write
2	0A1	OCW1	Write
2	0A0	OCW2	Write
2	0A0	OCW3	Write
2	0A0	IRR	Read
2	0A0	ISR	Read
2	0A1	Mask	Read
2	0A0, 0A1	Interrupt Level	Read

TABLE 4-5. INTERRUPT CONTROLLER FUNCTION MAP



5.0 8254 TIMER

The FE3010C contains an 8254 equivalent timer that contains three independent counters. All the timers run off a 1.19 MHz clock. The GATE0 and GATE1 signals are tied high. The GATE2 signal is tied to register 61, bit 0. The counters decrement when counting. The largest possible count is 0.

Each counter may be programmed for different counting modes and the count may be read back. To initialize a counter, the Control Word must be written followed by one or two bytes of count if needed. Each counter may be programmed to count in BCD or binary.

3

Timer Channel	Use
0	Time of Day (Interrupt)
1	Refresh Request
2	Speaker

I/O Address	Use	Read/Write
040	Timer 0 Count/Status	Read/Write
041	Timer 1 Count/Status	Read/Write
042	Timer 2 Count/Status	Read/Write
043	Control Word	Write

CONTROL WORD (FORMAT 1)			
0	CD		
1-3	Mode ⇒	000	Mode 0
		001	Mode 1
		X10	Mode 2
		X11	Mode 3
		100	Mode 4
		101	Mode 5
4-5	Function ⇒	00	Counter Latch Command
		01	Read/Write Low Byte
		10	Read/Write High Byte
		11	Read/Write Low Byte then High Byte
6-7	Counter ⇒	00	Counter 0
		01	Counter 1
		10	Counter 2
CONTROL WORD (FORMAT 2)			
0		0	
1			Select Counter 0
2			Select Counter 1
3			Select Counter 2
4			Latch Status
5			Latch Count
6-7		1	

TABLE 5-1. CONTROL WORD FORMAT



5.1 SETUP

Each counter may be set in one of 5 modes by writing a command word (format 1). The command word must specify the counter and the number of count bytes to be written. A new count may be written at any time.

5.1.1 Mode 0 Interrupt on Terminal Count

The counter starts when the count is loaded. When the count = 0, the counter will continue counting from FFFF in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting.

OUT will go low when the counter starts. It will go high when the count = 0, and stay high until a new count or mode is written.

If a new count is written while the counter is counting, it will be loaded on the next clock pulse.

5.1.2 Mode 1 Hardware Retriggerable One Shot

The counter starts when GATE goes from low to high. When the count = 0, the counter will continue counting from FFFF in binary mode or 9999 in BCD mode.

Any time GATE goes from low to high, the counter will be reloaded with the original count and the counter started.

OUT will go low when GATE goes from low to high. It will go high when the count = 0. If a new count is written while the counter is counting, it will be loaded the next time GATE goes from low to high.

5.1.3 Mode 2 Rate Generator

The counter starts when the count is loaded. When the count = 0, the counter is reloaded and the counter is started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded.

OUT will initially be high. When the count = 1, OUT will go low for one clock.

If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.1.4 Mode 3 Square Wave Generator

The counter starts when the count is loaded. When the count = 0, the counter is reloaded and the counter started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded.

When the counter starts, OUT will be high. When the count is half done, OUT will go low. If GATE goes low, then OUT will go high.

If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.1.5 Mode 4 Software Triggered Strobe

The counter starts when the count is loaded. When the count = 0, the counter will continue counting from FFFF in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. OUT will initially be high. When the count = 0, OUT will go low for one clock.

If a new count is written while the counter is counting, it will be loaded on the next clock pulse.

5.1.6 Mode 5 Hardware Triggered Strobe

The counter starts when the count is loaded. When the count = 0, the counter will continue counting from FFFF in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded. OUT will be high when the counter starts. When count = 0, OUT will go low for one clock. If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.



5.2 READING THE COUNTER

There are three ways of reading the counters:

1. The count is read directly. This mode can cause false readings due to fact that the counter may be changing while it is read.
2. The count may be read via a Counter Latch Command. (See COMMAND WORD format 1). This command latches the count so it may be read without changing.
3. The count may be read via a Read Back Command. (See COMMAND WORD format 2). This command is the equivalent of multiple Counter Latch Commands.

5.3 READING STATUS

The status of a counter may be read by issuing a Read Back Command with data bit 4 = 0. (See COMMAND WORD format 2). Bits 0-5 are the same as the command word for the counter. Bit 6 tells if the last count that was written has been loaded into the counter. Bit 7 reflects the state of the OUT pin.

STATUS WORD	
0	BCD
1-3	Mode
4-5	Function
6	New Count Written
7	Out Status

5.4 PAGE

The page register is an 8-bit by 16-byte dual-ported RAM. It is used to refresh cycles and to generate address bits 16 to 23 for 8-bit DMA transfers and address bits 17 to 23 for 16-bit DMA transfers. One port of the RAM is a read-only port for DMA or refresh cycles, and the other is a read/write port for the 80286 CPU.

5.5 REFRESH ADDRESS

This block contains an 11-bit counter that is used for the address during a refresh.

6.0 DECODE

Address	Decodes	Hex	
9 8 7 6 5 4 3 2 1 01			
0 0 0 0 0 X X X X X			DMA Controller 1 (Ch 0-3)0
0 0 0 0 1 X X X X X			Interrupt Controller Master
0 0 0 1 0 X X X X X			Timer
0 0 0 1 1 0 X X X 1			Port B (PIO)
0 0 0 1 1 1 X X X 1			Real Time Clock (RTCCS)
0 0 1 0 0 X X X X X			Page Register
0 0 1 0 1 X X X X X			Interrupt Controller Slave
0 0 1 1 0 X X X X X			DMA Controller 2 (Ch 4-7)

TABLE 6-1. DECODE ADDRESSES

6.1 PAGE REGISTER DECODES

Address	Decode
0087	DMA Channel 0
0083	DMA Channel 1
0081	DMA Channel 2
0082	DMA Channel 3
008B	DMA Channel 5
0089	DMA Channel 6

TABLE 6-2. PAGE REGISTER DECODES

Note: Page register data appears on address bits A23-A16 during refresh and 8-bit DMA cycles. For 16-bit DMA cycles (channels 5-7), the LSB of the page register does not appear; instead the 16-bit DMA address is shifted up one bit and A0 is floated in the FE3010C to be driven by external logic.

6.2 PIO

This block contains the control port to control the speaker and timer channel. It also contains circuitry to detect if refresh is running. This condition may be read back as bit 4. Bits 2 and 3 are read/write, but they do not perform any function. They are used for software compatibility with the IBM PC AT.

Port B (PIO) is an 8-bit control and status register on the AT. Bits 0 through 5 are defined in the FE3010C, while bits 6 and 7 are generated in the FE3001. During a read of Port B (address 0061), the FE3010C drives data bits 0-5 and tri-states bits 6 and 7. The FE3001, if used, will drive bits 6 and 7 indicating the parity error and channel check status. Bits 0 through 5 are described in the table below.

Bits 3 and 2 perform no function on the FE3010C; they are duplicated here to provide the read/write capability, but the actual enable functions are performed in the FE3001.

Bit	Function
5	OUT2 from timer channel 2 (read only)
4	Toggles on each refresh (read only)
3	Enable channel check (active low)
2	Enable parity check (active low)
1	Enable speaker (active high)
0	Gate for timer channel 2

TABLE 6-3. DECODE BIT FUNCTIONS



7.0 ABSOLUTE MAXIMUM RATINGS

T _A =+25 °C	
Power supply voltage, V _{DD} @ V _{SS} =0	7.0 V
Power dissipation, P _D MAX @V _{DD} =5.25V	300 mW
Current, I _{DD} @V _{DD} =5.25V	55 mA
Input voltage, V _I	0.0V to V _{DD} + 0.3V
Output voltage, V _O	0.0V to V _{DD} + 0.3V
Operating temperature, T _{OPT}	0° C to 70° C
Storage temperature, T _{STG}	-40° C to 125° C

* Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8.0 CAPACITANCE

(T _A =+25° C, V _{DD} = 0V)			
Parameter	Symbol	Max Limits	Test Condition
Input capacitance	C _I	10 pF	fc = 1 MHz unmeasured pins returned to 0V
I/O capacitance	C _{IO}	15 pF	

9.0 DC CHARACTERISTICS

T_A = 0° C to 70° C, V_{DD} = 5V ± 5%, these inputs have internal 50K Ω(min.) pullups.

[ALE, DMACLK, DMARDY, DRQ0, DRQ1, DRQ2, DRQ3, DRQ5, DRQ6, DRQ7, HLDA, IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, IRQ15, KBINT, CLEAR, INTA, IRQ13, MASTER, RFSH, TLCK, IRQ8]

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	V _{IL}	V _{SS}	0.8	V	V _{DD} = 5V ± 5%
Input high voltage	V _{IH}	2.0	V _{DD}	V	V _{DD} = 5V ± 5%
Input low current	I _{IL}	-10.0	-300.0	uA	V _{IN} = 0.0V
Input high current	I _{IH}		40.0	uA	V _{IN} = V _{DD}



[A(0), A(1), A(2), A(3), A(4), A(5), A(6), A(7), A(8), A(9), DATA(0), DATA(1), DATA(2), DATA(3), DATA(4), DATA(5), DATA(6), DATA(7), $\overline{\text{IOR}}$, $\overline{\text{IOW}}$]

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	V_{IL}	V_{SS}	0.8	V	$V_{DD} = 5V \pm 5\%$
Input high voltage	V_{IH}	2.0	V_{DD}	V	$V_{DD} = 5V \pm 5\%$
Input low current	I_{IL}		-10.0	μA	$V_{IN} = 0.0V$
Input high current	I_{IH}		10.0	μA	$V_{IN} = V_{DD}$
Output low voltage	V_{OL}		0.4	V	$I_{OL} = 4.0 \text{ mA}$
Output high voltage	V_{OH}	2.4		V	$I_{OH} = -4.0 \text{ mA}$
Output current	I_{OZ}	-10.0	10.00	μA	$0V < V_{OUT} < V_{DD}$

[AEN, DACK0, DACK1, DACK2, HRQ, INTR, $\overline{\text{DACKEN}}$, $\overline{\text{RTCCS}}$, OUT1, SPKR, SYSALE]

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	V_{OL}		0.4	V	$I_{OL} = 2.0 \text{ mA}$
Output high voltage	V_{OH}	2.4		V	$I_{OH} = -2.0 \text{ mA}$

[A(10), A(11), A(12), A(13), A(14), A(15), A(16), A(17), A(18), A(19), A(20), A(21), A(22), A(23), $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, TC]

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	V_{OL}		0.4	V	$I_{OL} = 4.0 \text{ mA}$
Output high voltage	V_{OH}	2.4		V	$I_{OH} = -4.0 \text{ mA}$
Output current	I_{OZ}	-10.0	10.00	μA	$0V < V_{OUT} < V_{DD}$



10.0 AC CHARACTERISTICS

TA = 0° C to +70° C, V_{DD} = +5V ±5% load capacitance = 85 pF, operating at 8 MHz.

Symbol	Parameter	Min	Max	Unit
t1	DRQ high setup time to DMACLK high	20		ns
t2	HRQ active high delay from DMACLK rising edge	10	49	ns
t3	HLDA high setup time to DMACLK rising edge	15		ns
t4	AEN active high delay from DMACLK falling edge	14	69	ns
t5	AEN inactive low delay from DMACLK rising edge	15	74	ns
t6	SYSALE active high delay from DMACLK rising edge	10	54	ns
t7	SYSALE inactive low delay from DMACLK rising edge	14	69	ns
t8	$\overline{\text{IOR}}$ and $\overline{\text{MEMR}}$ active low delay from DMACLK rising edge	12	60	ns
t9	$\overline{\text{IOW}}$ and $\overline{\text{MEMW}}$ active low delay from DMACLK rising edge	12	60	ns
t10	$\overline{\text{IOR}}$ and $\overline{\text{MEMR}}$ inactive high delay from DMACLK rising edge	11	52	ns
t11	$\overline{\text{IOW}}$ and $\overline{\text{MEMW}}$ inactive high delay from DMACLK rising edge	11	52	ns
t12	$\overline{\text{DACKEN}}$ active low delay from DMACLK falling edge	13	63	ns
t13	$\overline{\text{DACKEN}}$ inactive high delay from DMACLK falling edge	10	49	ns
t14	TC active high delay from DMACLK falling edge	11	58	ns
t15	TC inactive low delay from DMACLK falling edge	13	68	ns
t16	DMARDY high setup time delay to DMACLK rising edge	10	2	ns
t17	ADDR active delay from AEN rising edge	2	18	ns
t18a	ADDR valid delay from DMACLK rising edge		178	ns
t19	ADDR float delay from DMACLK falling edge		83	ns
t20	DATA valid delay from $\overline{\text{IOR}}$ falling edge	14	68	ns
t21	DATA float delay from $\overline{\text{IOR}}$ rising edge	11	51	ns
t22	ADDR valid setup time to SYSALE inactive low	71		ns
t23a	SYSALE inactive low to ADDR valid hold time	121		ns
t24	ADDR valid delay from $\overline{\text{RFSH}}$ falling edge	15	78	ns
t25	ADDR float delay from $\overline{\text{RFSH}}$ rising edge	10	60	ns
t26	SYSALE active high from delay $\overline{\text{RFSH}}$ falling edge	6	29	ns
t27	SYSALE inactive low delay from $\overline{\text{RFSH}}$ rising edge	8	40	ns



10.0 AC CHARACTERISTICS (CONTINUED)

Symbol	Parameter	Min	Max	Unit
t28	SYSALE active high delay from ALE rising edge	5	31	ns
t29	SYSALE inactive low delay from ALE falling edge	9	46	ns
t30	INTR (mstr) active high delay from IRQ rising edge	11	105	ns
t31	INTR (slave) active high from ALE rising edge	27	136	ns
t32	DATA valid delay from $\overline{\text{INTA}}$ falling edge	17	84	ns
t33	DATA float delay from $\overline{\text{INTA}}$ rising edge	9	45	ns
t34	RTCCS active low delay from ALE rising edge	13	66	ns
t35	RTCSS inactive high delay from ALE rising edge	9	46	ns
t36	OUT1 active high delay from TCLK falling edge	7	53	ns
t37	OUT1 inactive low delay from TCLK falling edge	10	63	ns
t38	DATA invalid time delay from DATA to $\overline{\text{IOW}}$ inactive high	30		ns
t39	DATA set-up time to $\overline{\text{IOW}}$ active low	30		ns



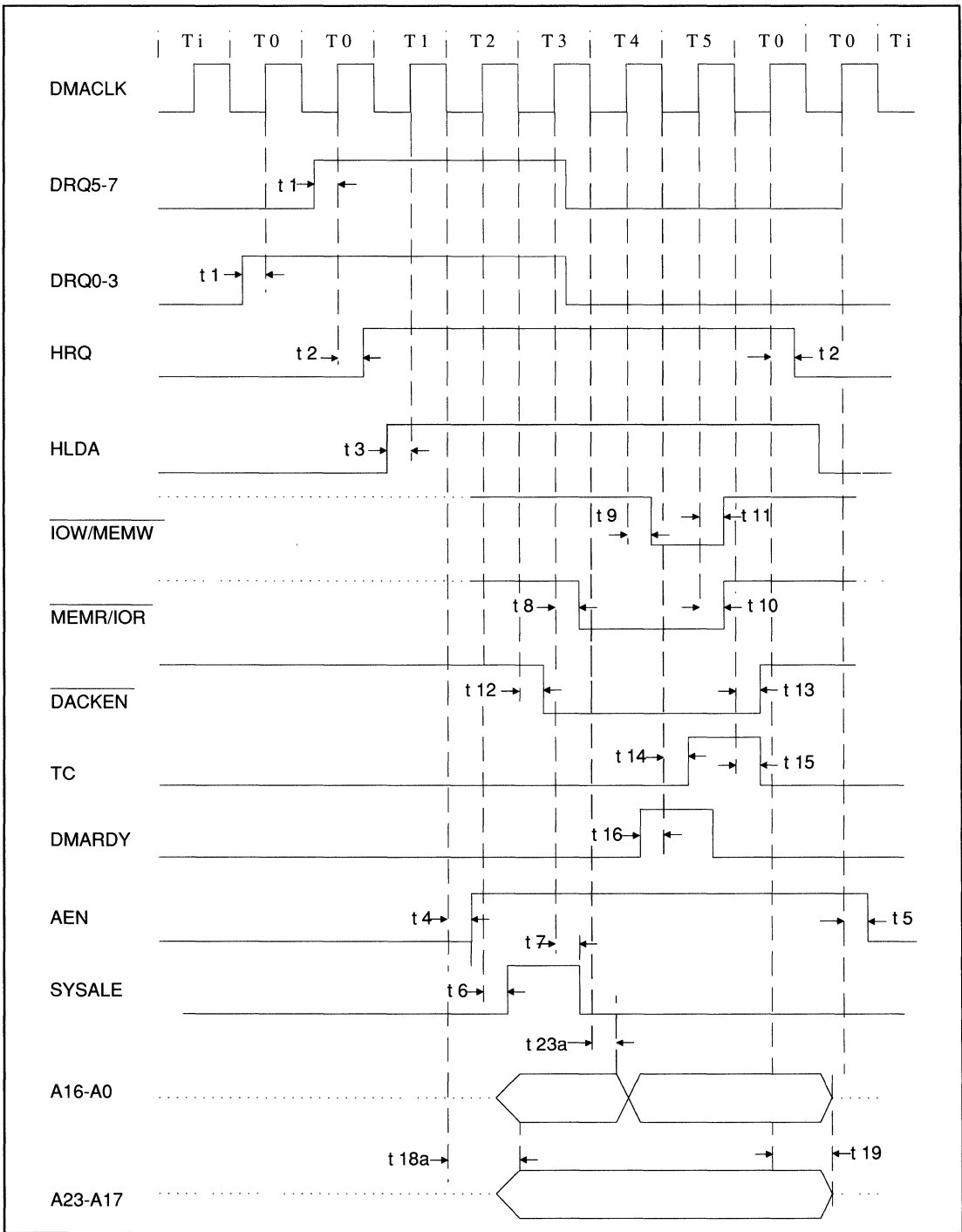


FIGURE 10-1. DMA CYCLE



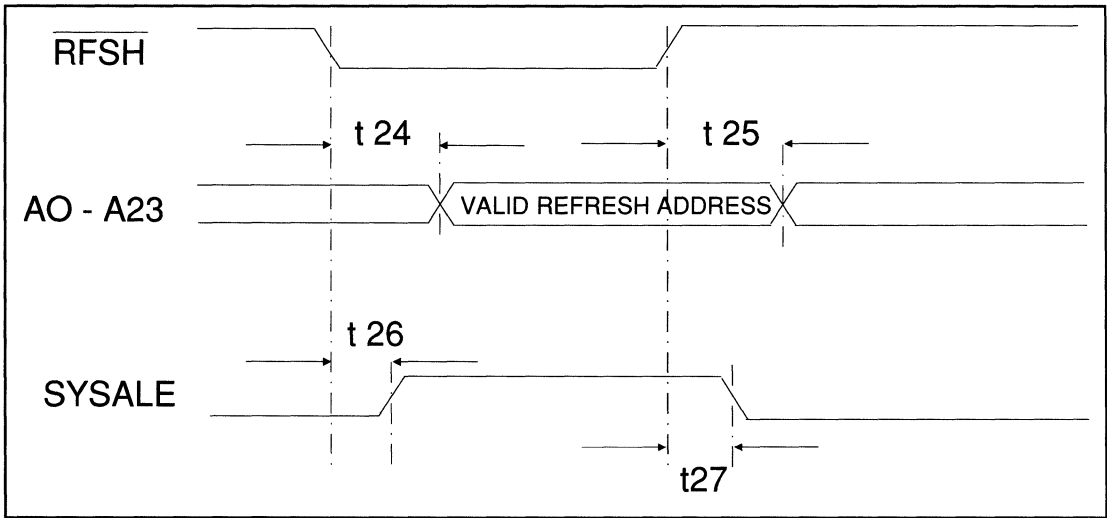


FIGURE 10-2. REFRESH CYCLE

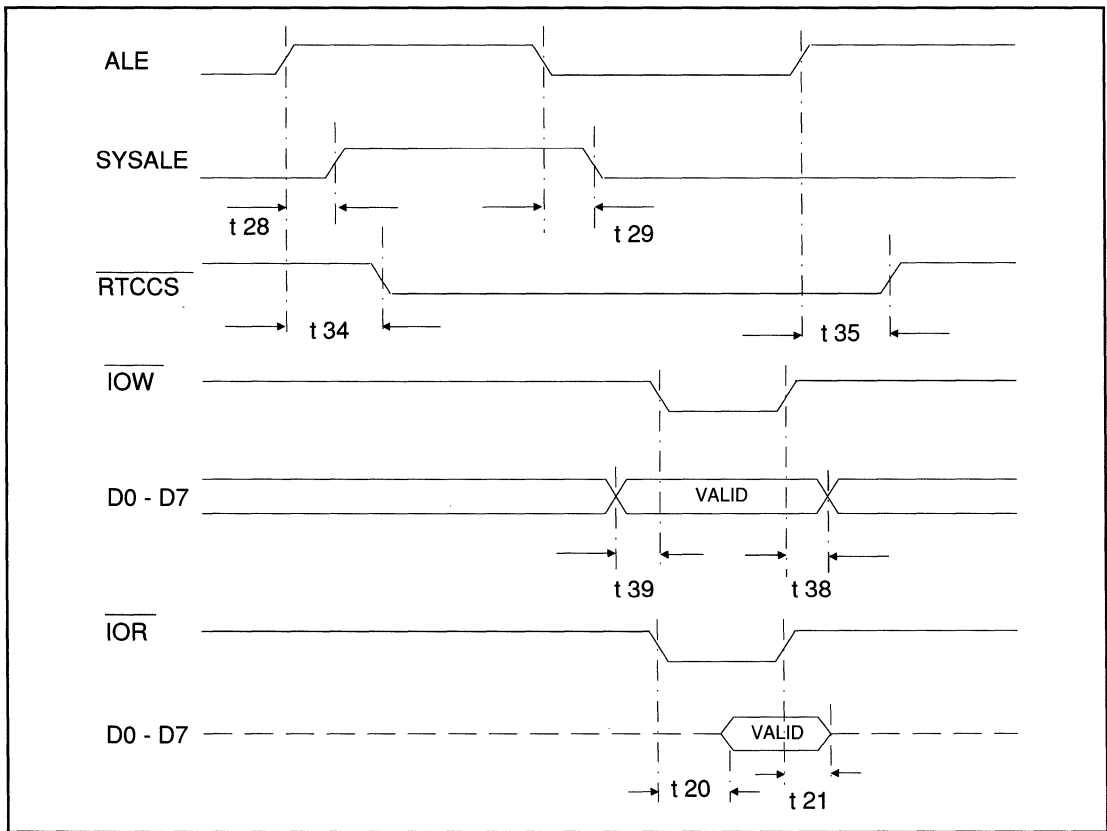


FIGURE 10-3. CPU CYCLE



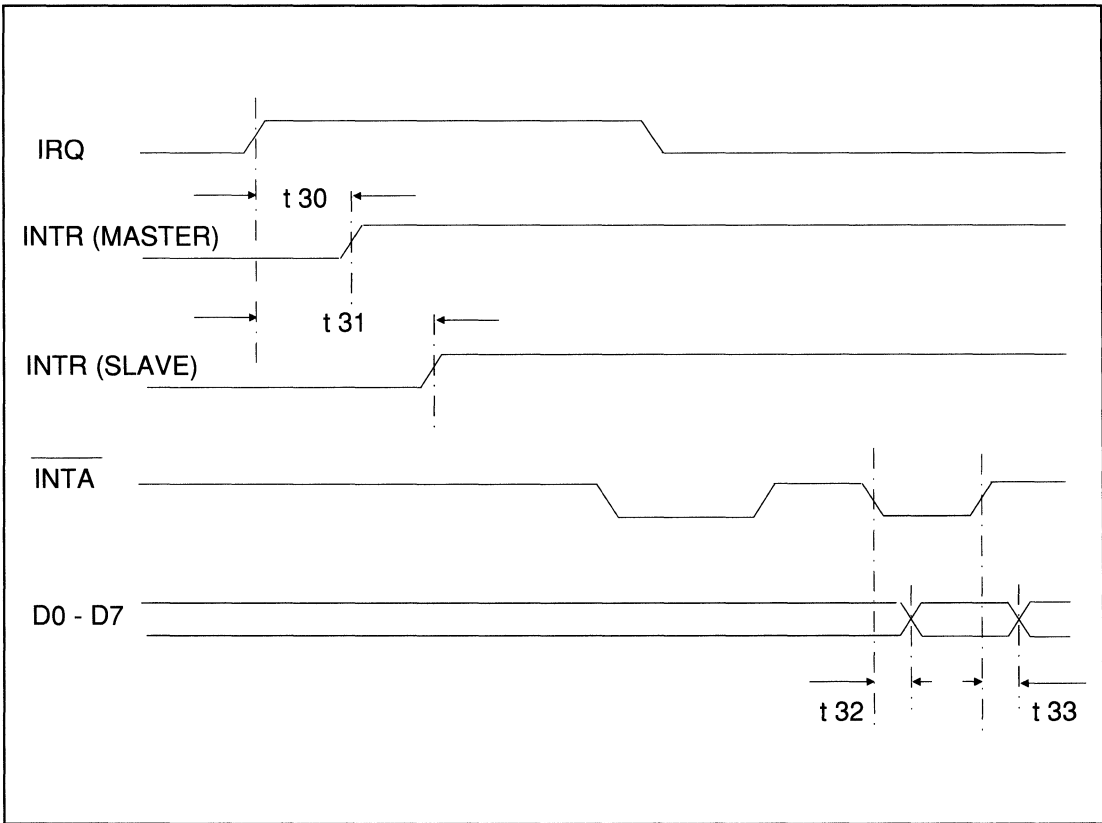


FIGURE 10-4. INTERRUPT CYCLE

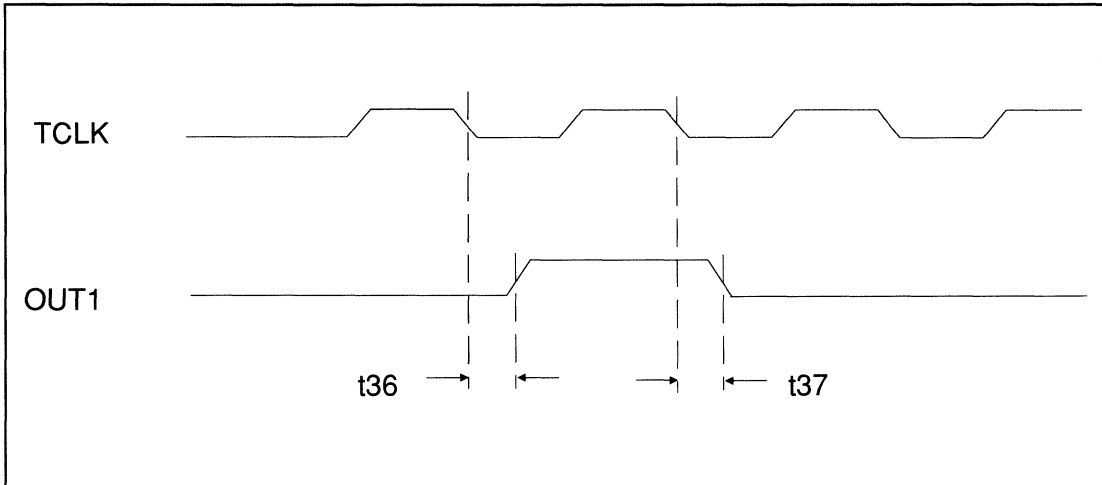


FIGURE 10-5. TIMER CYCLE

