TGC100 SERIES
1-μm CMOS GATE ARRAYS

RELEASE 2.0, REVISED OCTOBER 1988

- **Six Arrays with up to 16 758 Useable Gates**
- **Fast Prototype Turn-around Time**
- **Extensive Design Support**
  - **Design Libraries Compatible with Daisy and Mentor CAE Systems**
  - **TI Regional ASIC Design Centers**
  - **TI ASIC Distributor Design Centers**
- **Library Contains 222 Macros Including:**
  - **Register Files, Oscillators**
  - **Scan Flip–Flops/Latches**
  - **Clock Distribution Macros**
- **TGC100 1-μm EPIC™ CMOS Technology:**
  - **Double-Level Metal, Silicided-Poly**
  - **Typical Gate Delay 500 ps (FO = 3)**
  - **Flip-Flop Toggle Rates Up to 208 MHz**
  - **ESD and Latch-Up Protected I/Os**
  - **Outputs with Up to 20-mA Sink Current**
  - **di/dt Controlled or Full-Speed Outputs**

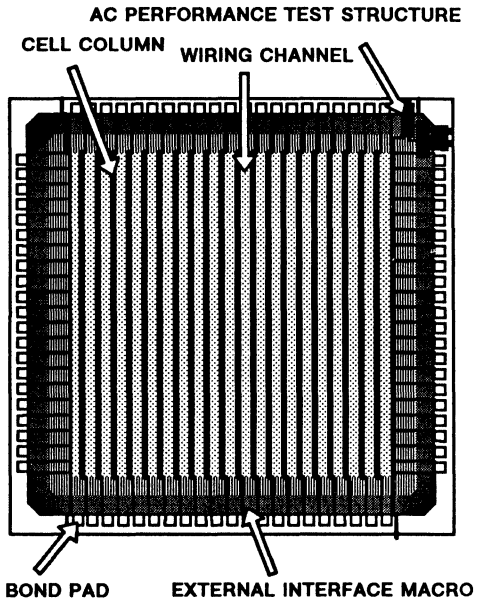

FIGURE 1. TGC103 CMOS GATE ARRAY

description

The Texas Instruments TGC100 Series comprises six gate arrays, each fabricated using TI's 1-μm advanced silicon-gate CMOS EPIC™ process. The process features two levels of copper-doped-aluminum metallization for interconnect. Silicided polysilicon gate, source, and drain elements further reduce internal resistance and enhance performance. N-channel and P-channel gate lengths are patterned at 1-μm. The six base gate-arrays, with their basic-cell and bond-pad configurations and production packages, are shown below.

GATE ARRAY TYPE	BASIC CELLS 2–INPUT GATES		TOTAL BOND PADS	PRODUCTION PACKAGES															
	TOTAL AVAILABLE	MAXIMUM USABLE		PLASTIC DIP		PLASTIC LEADED CHIP CARRIER				PLASTIC QFP See Note 1				PLASTIC PIN–GRID ARRAY					
				28	40	28	44	68	84	100	120	132	160	100	120	132	144	180	208
TGC103	3 200	2 880	84	✓	✓	✓	✓	✓	✓					✓					
TGC105	5 376	4 838	118	✓	✓		✓	✓	✓	✓●	●			✓	✓				
TGC108	8 896	8 006	142	✓	✓		✓	✓	✓	✓●	●	✓		✓	✓	✓	✓		
TGC112	12 654	11 389	196					✓	✓		●	✓	●	✓	✓	✓	✓	✓	
TGC115	15 580	14 022	216								●	✓	●			✓	✓	✓	✓
TGC118	18 620	16 758	216								●	✓	●			✓	✓	✓	✓

NOTE 1: For the quad-flat packages (QFP) ✓ = JEDEC and ● = EIAJ

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PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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The basic structure of the TGC100 Series 1-μm CMOS gate arrays consists of basic-cell columns separated by wiring channels. A perimeter of external interface macros are configurable as inputs, outputs, bidirectional I/Os, oscillators, or power pins. Each 4-transistor internal basic cell is equivalent to a 2-input NAND gate.

Each base array in the TGC100 Series incorporates an ac-performance test structure embedded in an otherwise unused corner of the array. Although not user-accessible from the I/O bond pads, this test structure is activated by TI during the wafer-probe stage of device fabrication. Measurements are made to verify that the ac performance of the finished gate array falls within the normal production range. For most applications, this ac performance verification, in conjunction with the standard 1-MHz functional testing and DC parametric testing, is sufficient to ensure correct device operation and performance.

library functions

The TGC100 Series gate array library includes basic gates, buffers, flip-flops, latches, registers, and MSI macros. Of the 222 macros offered, 195 are hardwired and 27 are software macros. The hardwired macros provide a broad selection of predesigned, fully characterized functions. The software macros provide popular TTL/CMOS-type MSI functions, which can be used as supplied or modified at the workstation to suit your design requirements. Additional user-defined software macros can be created using the TGC100 library macros. Library release 2.0 contains the following classes of macros:

- 2 Hardwired MegaModule™ Register Files and 27 MSI Software Macros
- 39 Register, Scan Flip-Flops/Latches, Delay Elements
- 75 Gate, Bus Buffers, and Macro Building Blocks
- 79 External Input, Output, Bidirectional Buffer and Oscillator Macros

A workstation library summary, showing essential performance data and basic-cell utilization, begins on page 14. A complete TGC100 Series Design Kit, supplied for the Daisy or Mentor CAE Systems, includes the following:

- TGC100 Series Data Manual
- CMOS Gate Array Design Manual
- Design Support Software User's Manual
- TGC100 Series Design Library

The Design Kit is arranged to accommodate new material as it is issued.

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design flow

User-defined semicustom integrated circuits, designed using TI's TGC100 Series Macro Function Library in conjunction with Daisy or Mentor CAE Systems, can be simulated and verified prior to creating the design database files. The database files generated are used to create the photomask tooling for fabrication. These files are also used by the test programs required for acceptance of the user-defined gate array prototypes. Figure 2 provides an overview of the design flow.

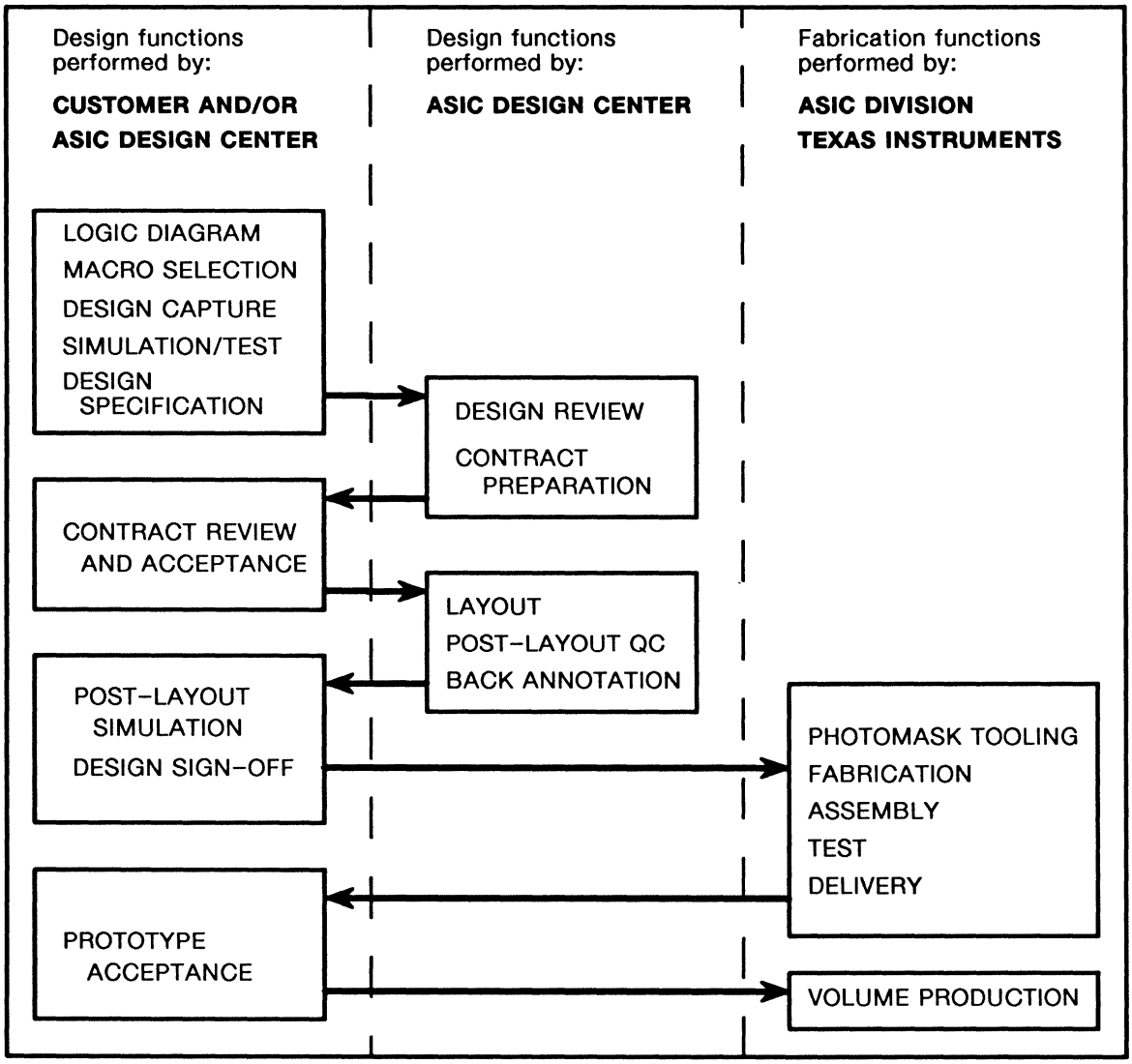

FIGURE 2. TGC100 SERIES DESIGN FLOW OVERVIEW

If desired, TGC100 Series gate array designs can be migrated easily to TI standard cell designs.

prototype and production

The standard TGC100 Series nonrecurring engineering (NRE) charge and prototype cycle-time quotation includes the following products and services:

- Initial Design Review
- Design Specification Generation
- Development Contract Preparation
- Design Layout (macro placement and routing)
- Post-Layout QC
- Delivery of Post-Layout Delay Files (back annotation)
- Photomask Tooling
- Fabrication, Assembly, and Test of Prototypes
- Delivery of Five (5) Prototypes (See Notes 2 and 3)

NOTES: 2. Prototypes are assembled in packages that are socket and footprint compatible with the package chosen for production units.
3. Prototypes are tested for functionality using customer-supplied test patterns at f = 1 MHz, V_{CC} = 5 V, and T_A = 25°C.

prototype and production testing

Standard testing that is performed on TGC100 Series products is enumerated in Table 1. The wafer probe tests use the 1 MHz test description language (TDL) pattern set and includes testing the ac performance of the die by exercising the ac-performance test structure. Specified logic-level thresholds are utilized to test output voltage (V_{OH}, V_{OL}), off-state output current (I_{OZ}), quiescent supply current (I_{CC}), and input current (I_{IL}, I_{IH}).

TABLE 1. TGC100 SERIES STANDARD TESTING

1-MHz TEST DESCRIPTION LANGUAGE (TDL) PATTERN SET	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE		DC PARA-METRICS	AC TEST STRUCTURE
	4.5 V	5 V	5.5 V	25°C	70°C		
Prototype Unit Tests		✓		✓			
Production Wafer Probe Tests	✓	✓	✓	✓		✓	✓
Production Unit Tests	✓	✓	✓		✓	✓	

options for prototype and production units

In addition to the standard TGC100 Series product and services previously outlined, the following options may be selected (at additional cost and cycle-time):

- Additional Prototypes
- Additional 1-MHz Test Vectors
- Prototype Devices Tested Over Temperature– and V_{CC}–Range Plus DC Parametrics
- Critical Path Delay Measurements (pin-to-pin)
- "At-Speed" Test Vectors
- NonStandard V_{CC} and Ground Pin Locations
- Operating Temperature Range Other Than 0°C to 70°C

For a quotation or further details of available options, please contact your local TI Sales Office or TI-Authorized ASIC Distributor.

macro naming summary

The logic function implemented by each of the TGC100 Series gate array macro functions is indicated by the macro name prefix. An index to the macro name prefixes is shown in Table 2. The LJ suffix appended to each macro name indicates 1-μm CMOS technology.

TABLE 2. INDEX TO MACRO FUNCTION PREFIXES

AD ..... Adder	LA ..... D-Type and S-R Latches
AN ..... AND Gates	LH ..... Latches
AO ..... AND-OR Gates	MU ..... Multiplexers
BF .. Multi-Stage AND, NAND, NOR, OR Gates	NA ..... NAND Gates
BU ..... Buffers	NO ..... NOR Gates
DE ..... Decoders/Demultiplexers	OP ..... Output Buffers
DF/DT ..... D-Type Flip-Flops	OR ..... OR Gates
DL ..... Delay Elements	OS ..... Oscillators
EN ..... Exclusive-NOR Gates	R ..... Registers
EX ..... Exclusive-OR Gates	RF ..... Register Files
IO ..... Bidirectional I/O Buffers	S ..... Software Macros
IP ..... Input Buffers	TA ..... Toggle Type Flip-Flops
IV ..... Inverters	TD ..... Scan Flip-Flops
JK ..... J-K Type Flip-Flops	TO ..... Hi- and Lo-Level Tie-Off Gate

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I . . . . . −0.5 V to 7 V
Output voltage range, V_O . . . . . −0.5 V to 7 V
Input clamp current‡ I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current§ I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current§ (V_O = 0 to V_{CC}) . . . . . ±25 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at or beyond the conditions indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
‡ Applies for external input and bidirectional buffers.
§ Applies for external bidirectional and output buffers.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage†	CMOS-compatible inputs	$0.7V_{CC}$			V
		TTL-compatible inputs	2			
V_{IL}	Low-level input voltage†	CMOS-compatible inputs			$0.2V_{CC}$	V
		TTL-compatible inputs			0.8	
V_I	Input voltage†‡		0		V_{CC}	V
V_{T+}	Positive-going threshold voltage‡	CMOS-compatible inputs	$0.7V_{CC}$			V
		TTL-compatible inputs	2			
V_{T-}	Negative-going threshold voltage‡	CMOS-compatible inputs			$0.2V_{CC}$	V
		TTL-compatible inputs			0.8	
V_{hys}	Hysteresis‡ ($V_{T+} - V_{T-}$)	CMOS-compatible inputs		1.7		V
		TTL-compatible inputs		0.4		
V_O	Output voltage§		0		V_{CC}	V
I_{OH}	High-level output current§		As specified on individual data sheets			mA
I_{OL}	Low-level output current§					
T_A	Operating temperature range		0		70	°C
t_t	Input transition time (rise and fall)†		0		25	ns

† Applies for external input and bidirectional buffers without hysteresis.
‡ Applies for external input buffers with hysteresis.
§ Applies for external bidirectional and output buffers.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage††	CMOS threshold	I_{OH} = Rated	3.7		V
		TTL threshold		2.4		
		Inputs without pull-up	I_{OH} = −20 μA, See Note 5	V_{CC}−0.1		
V_{OL}	Low-level output voltage##	CMOS threshold	I_{OL} = Rated		0.5	V
		TTL threshold			0.5	
		Inputs without pull-down	I_{OL} = 20 μA, See Note 5		0.1	
I_{CC}	Supply Current	TGC103	V_I = V_{CC} OR 0, See Note 6		225	μA
		TGC105			350	
		TGC108			450	
		TGC112			650	
		TGC115			750	
		TGC118			800	

†† Not applicable for N-channel open-drain output buffers.
Not applicable for P-channel open-drain output buffers.

NOTES: 5. These limits apply when all other outputs are open.
6. For external inputs and bidirectional I/O buffers with pull-up source VI = VCC and with pull-down source VI = 0, the remaining electrical and switching characteristics are summarized in the library listing beginning on page 14.

input, output, and bidirectional buffers

The TGC100 Series library contains a wide selection of input, output and bidirectional buffers that facilitate design trade-offs. The buffers include versions having active pull-up or pull-down terminators and N-channel and P-channel open-drains.

input buffers

Input buffers are available with CMOS-or TTL-level thresholds that feature inverting and noninverting versions with and without hysteresis. A guide to input buffer selection is shown in Table 3.

TABLE 3. INPUT BUFFER SELECTION GUIDE

INPUT THRESHOLD	INVERTING/ NONINVERTING	LOGIC TYPE AND OPTIONS	MACRO NAME
CMOS	Noninverting	Standard	IPI01LJ
		70-μA Pull-up	IPL01LJ
		70-μA Pull-down	IPU01LJ
	Inverting	Hysteresis	IPI06LJ
		Standard	IPI00LJ
TTL	Noninverting	Standard	IPI04LJ
		70-μA Pull-up	IPL04LJ
		70-μA Pull-down	IPU04LJ
		Hysteresis	IPI09LJ

These input buffers feature 2-pin crystal-controlled oscillator circuits embedded in an input design.

TABLE 4. CRYSTAL–CONTROLLED OSCILLATORS

FREQUENCY	MACRO NAME
55-to-75 MHz	OSI11LJ
35-to-55 MHz	OSI12LJ
20-to-35 MHz	OSI13LJ
1-to-20 MHz	OSI14LJ

Performance specifications for input buffers and crystal-controlled oscillators are contained in the workstation library summary section of this data sheet and also in the *TGC100 Series Data Manual.*

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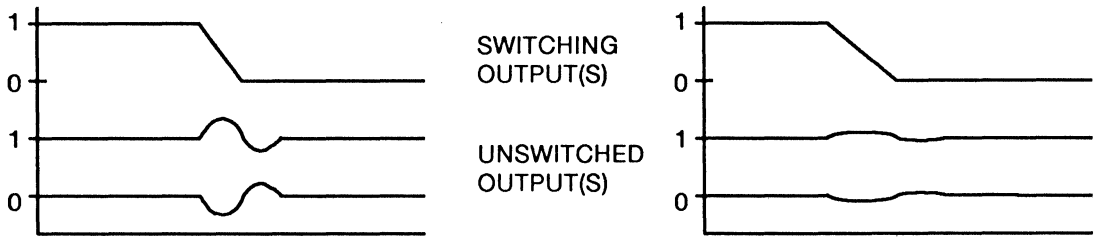
di/dt control

The rapid rate of change of current (di/dt) developed during high-speed logic-level transitions of output and bidirectional buffers creates unwanted voltage transients if the gate array is installed in a system having high V_{CC} and/or ground impedances (see Figure 3a). To assist in minimizing unwanted voltage transients, the TGC100 Series Gate Array library includes output and bidirectional buffers having integral di/dt control (see Figure 3b). Full-speed, non-di/dt-controlled versions are also offered for critical paths.



a. WITHOUT di/dt CONTROL

b. WITH di/dt CONTROL

FIGURE 3. TYPICAL EFFECTS OF di/dt CONTROL

When using non-di/dt-controlled output buffers, the following methods are some of the options used to minimize the di/dt related transients and reduce V_{CC} and ground trace impedances.

- Locate non-di/dt-controlled output and bidirectional buffers on low-inductance pins and adjacent to V_{CC} and ground pins.
- Minimize the number of simultaneously switching outputs.
- Increase the number of V_{CC} and ground pins.
- Increase the width of printed-circuit board's V_{CC} and ground traces, or use dedicated V_{CC} and ground planes.

Table 5 provides a selection guide for choosing the correct buffer based on the type of load driven, along with potential V_{CC} and ground pin requirements reduction.

TABLE 5. BUFFER SELECTION GUIDE

APPLICATION (TYPE OF LOAD DRIVEN)				CONSIDER USING BUFFER TYPE		POTENTIAL V_{CC}/GND PIN REDUCTION
CMOS/MOS LS	AC/ACT ALS/S/AS/F	TERMINATED LINES	CRITICAL PATHS	I/Os	OUTPUTS	
•	•	•		IO(K,N,W)XXLJ	OPKXXLJ	45%
	•	•	•	IO(I,L,U)XXLJ	OPIXXLJ	0

Detailed design guidelines on the selection of output and bidirectional buffers, and V_{CC} and ground pin requirements, are contained in the *CMOS Gate Array Design Manual.*

output and bidirectional I/O characteristics

The high-level and low-level output voltage characteristics of external outputs and bidirectional I/Os are common for all types of macros. The electrical characteristics table on page 6 provides the V_{OH} and V_{OL} parameters.

output buffers

Output buffers are available in totem-pole, 3-state, N-channel, or P-channel open-drain output configurations, with drive current ratings from 2 mA to 20 mA. Performance specifications are contained in the workstation library summary section of this data sheet and also in the *TGC100 Series Data Manual*. A guide to output buffer selection is shown in Table 6.

TABLE 6. OUTPUT BUFFER MACRO SELECTION GUIDE

OUTPUT CONFIGURATION (See Note 7)	OUTPUT CURRENT (Source/Sink) (mA)	MACRO NAME (and performance class)	
		WITH di/dt	WITHOUT di/dt
TOTEM–POLE	2/2	OPK20LJ	OPI20LJ
	4/4	OPK40LJ	OPI40LJ
	8/8	OPK80LJ	OPI80LJ
	12/12	OPKH0LJ	OPIH0LJ
	12/16	OPKA0LJ	OPIA0LJ
	12/20	OPKJ0LJ	OPIJ0LJ
OPEN–DRAIN N–Channel (See Note 8)	2	OPK21LJ	OPI21LJ
	4	OPK41LJ	OPI41LJ
	8	OPK81LJ	OPI81LJ
OPEN–DRAIN P–Channel (See Note 9)	2	OPK24LJ	OPI24LJ
	4	OPK44LJ	OPI44LJ
	8	OPK84LJ	OPI84LJ
3–STATE	2/2	OPK23LJ	OPI23LJ
	4/4	OPK43LJ	OPI43LJ
	8/8	OPK83LJ	OPI83LJ

NOTES: 7. All output buffers are noninverting.
8. N-channel open-drain outputs are for sink current.
9. P-channel open-drain outputs are for source current.

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bidirectional input/output buffers

Bidirectional I/O buffers are available in 3-state output configurations, with drive current ratings from 2 mA to 8 mA. Performance specifications are contained in the workstation library summary section of this data sheet and also in the *TGC100 Series Data Manual.* A guide to bidirectional buffer selection is shown in Table 7.

TABLE 7. BIDIRECTIONAL I/O BUFFER SELECTION GUIDE

OUTPUT CONFIGURATION (See Notes 10 and 11)	OUTPUT CURRENT (Source/Sink) (mA)	INPUT THRESHOLD	MACRO NAME (and performance class)	
			WITH di/dt	WITHOUT di/dt
STANDARD	2/2	CMOS	IOK21LJ	IOI21LJ
		TTL	IOK24LJ	IOI24LJ
	4/4	CMOS	IOK41LJ	IOI41LJ
		TTL	IOK44LJ	IOI44LJ
	8/8	CMOS	IOK81LJ	IOI81LJ
		TTL	IOK84LJ	IOI84LJ
WITH 70-μA PULL-UP	2/2	CMOS	ION21LJ	IOL21LJ
		TTL	ION24LJ	IOL24LJ
	4/4	CMOS	ION41LJ	IOL41LJ
		TTL	ION44LJ	IOL44LJ
	8/8	CMOS	ION81LJ	IOL81LJ
		TTL	ION84LJ	IOL84LJ
WITH 70-μA PULL-DOWN	2/2	CMOS	IOW21LJ	IOU21LJ
		TTL	IOW24LJ	IOU24LJ
	4/4	CMOS	IOW41LJ	IOU41LJ
		TTL	IOW44LJ	IOU44LJ
	8/8	CMOS	IOW81LJ	IOU81LJ
		TTL	IOW84LJ	IOU84LJ

NOTES: 10. All inputs are noninverting.
11. All outputs are 3-state and noninverting.

ALPHANUMERIC INDEX TO TGC100 MACROS

MACRO NAME	CELLS USED	PAGE
AD100LJ	9	16
AN210LJ	2	15
AN220LJ	2	15
AN310LJ	2	15
AN320LJ	3	15
AN410LJ	3	15
AN420LJ	3	15
AN510LJ	3	15
AN810LJ	5	15
AO220LJ	3	15
AO221LJ	2	15
AO241LJ	6	15
AO320LJ	4	15
AO421LJ	4	15
BF001LJ	2	17
BF006LJ	2	17
BF011LJ	3	17
BF022LJ	3	17
BF051LJ	2	17
BF053LJ	2	17
BF056LJ	2	17
BU130LJ	2	17
BU150LJ	3	17
CKD03LJ	40	17
CKD05LJ	48	17
CKD08LJ	64	17
CKD12LJ	74	17
CKD15LJ	82	17
CKD18LJ	98	17
CK120LJ	10	17
DE210LJ	3	18
DFB20LJ	12	19
DLD00LJ	2	20
DLE00LJ	3	20
DTB00LJ	8	19
DTB10LJ	9	19
DTB20LJ	10	19
DTC00LJ	7	19
DTC10LJ	8	19
DTC20LJ	9	19
DTN00LJ	6	19
DTN10LJ	7	19
DTN20LJ	8	19
DTP00LJ	7	19
DTP10LJ	8	19
DTP20LJ	9	19
EN210LJ	3	20
EX210LJ	3	20
EX220LJ	4	20
IOI21LJ	–	22
IOI24LJ	–	22
IOI41LJ	–	22
IOI44LJ	–	22
IOI81LJ	–	22
IOI84LJ	–	22
IOK21LJ	–	22
IOK24LJ	–	22
IOK41LJ	–	22
IOK44LJ	–	22
IOK81LJ	–	22
IOK84LJ	–	22
IOL21LJ	–	23
IOL24LJ	–	23
IOL41LJ	–	23
IOL44LJ	–	23
IOL81LJ	–	23
IOL84LJ	–	23
ION21LJ	–	23
ION24LJ	–	23
ION41LJ	–	23
ION44LJ	–	23
ION81LJ	–	23
ION84LJ	–	23
IOU21LJ	–	23
IOU24LJ	–	23
IOU41LJ	–	23
IOU44LJ	–	23
IOU81LJ	–	23
IOU84LJ	–	23
IOW21LJ	–	23
IOW24LJ	–	23
IOW41LJ	–	23
IOW44LJ	–	23
IOW81LJ	–	23
IOW84LJ	–	23
IPI00LJ	–	21
IPI01LJ	–	21
IPI04LJ	–	21
IPI06LJ	–	21
IPI09LJ	–	21
IPL01LJ	–	21
IPL04LJ	–	21
IPU01LJ	–	21
IPU04LJ	–	21
IV110LJ	1	24
IV120LJ	1	24
IV140LJ	2	24
IV211LJ	2	24
IV221LJ	4	24
IV241LJ	5	24
JKB20LJ	12	24
JKB21LJ	12	24
LAB20LJ	4	25
LAH12LJ	5	25
LAH13LJ	5	25
LAH14LJ	7	25
LAH20LJ	5	25
LAH22LJ	4	25
LH110LJ	4	25
LH400LJ	11	25
MU111LJ	3	25
MU220LJ	7	25
MU311LJ	13	25
NA210LJ	1	26
NA220LJ	2	26
NA310LJ	2	26
NA311LJ	2	26
NA320LJ	3	26
NA410LJ	2	26
NA420LJ	4	26

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MACRO NAME	CELLS USED	PAGE
NA510LJ	3	26
NA520LJ	5	26
NA810LJ	6	26
NA820LJ	6	26
NO210LJ	1	26
NO220LJ	2	26
NO310LJ	2	26
NO320LJ	3	26
NO410LJ	4	26
NO420LJ	4	26
NO510LJ	4	26
NO520LJ	5	26
NO810LJ	6	26
NO820LJ	6	26
OA220LJ	3	26
OA231LJ	3	26
OA241LJ	4	26
OPIA0LJ	–	27
OPIH0LJ	–	27
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OPI80LJ	–	27
OPI81LJ	–	28
OPI83LJ	–	27
OPI84LJ	–	28
OPKA0LJ	–	27
OPKH0LJ	–	27

MACRO NAME	CELLS USED	PAGE
OPKJ0LJ	–	27
OPK20LJ	–	27
OPK21LJ	–	28
OPK23LJ	–	27
OPK24LJ	–	28
OPK40LJ	–	27
OPK41LJ	–	28
OPK43LJ	–	27
OPK44LJ	–	28
OPK80LJ	–	27
OPK81LJ	–	28
OPK83LJ	–	27
OPK84LJ	–	28
OR210LJ	2	28
OR220LJ	2	28
OR310LJ	2	28
OR320LJ	3	28
OR410LJ	3	28
OR420LJ	3	28
OR510LJ	4	28
OR810LJ	5	28
OSI11LJ	–	29
OSI12LJ	–	29
OSI13LJ	–	29
OSI14LJ	–	29
RF400LJ	418	30
RF402LJ	462	30
R2401LJ	26	29
R2402LJ	27	29
R2403LJ	27	29
R2404LJ	31	29
R2405LJ	26	29
R2406LJ	28	29
S085LJ	58	16

MACRO NAME	CELLS USED	PAGE
S138LJ	25	18
S139LJ	26	18
S150LJ	122	25
S151LJ	40	25
S153LJ	26	25
S157LJ	18	25
S161ALJ	79	18
S163ALJ	81	18
S164LJ	88	31
S165ALJ	126	31
S173LJ	53	20
S175LJ	31	20
S180XLJ	21	16
S181LJ	125	16
S182LJ	35	16
S191LJ	98	18
S193LJ	87	18
S194ALJ	73	31
S244LJ	28	17
S273LJ	55	20
S283LJ	69	16
S373LJ	47	25
S374LJ	76	20
S375LJ	16	25
S686LJ	104	16
S688LJ	32	16
TAB20LJ	9	31
TDB10LJ	10	30
TDC11LJ	10	30
TDN11LJ	8	30
TDN12LJ	9	30
TDN13LJ	12	30
TDN22LJ	11	30
TO010LJ	2	31

– = 0, IOs, IPs, OPs, and OSs do not occupy basic-cell locations.

CMOS/TTL NUMERICAL CROSS–REFERENCE

CMOS OR TTL TYPE NUMBER	SIMILAR GATE ARRAY MACRO	PAGE
4002	NO410LJ NO420LJ	26
4072	OR410LJ OR420LJ	28
4078	OR310LJ OR320LJ	28
4078	NO810LJ NO820LJ	26
7400	NA210LJ NA220LJ	26
7402	NO210LJ NO220LJ	26
7404	IV110LJ IV120LJ IVI40LJ	24
7408	AN210LJ AN220LJ	15
7410	NA310LJ NA320LJ	26
7411	AN310LJ AN320LJ	15
7420	NA410LJ NA420LJ	26
7421	AN410LJ AN420LJ	15
7427	NO310LJ NO320LJ	26
7430	NA810LJ NA820LJ	26
7432	OR210LJ OR220LJ	28
7451	AO221LJ	15
7454	AO241LJ	15
7455	AO421LJ	15
7474	DFB20LJ DTB00LJ DTB10LJ DTB20LJ	19
7475	LAH20LJ LH400LJ	25
7482	AD100LJ	16
7485	SO85LJ	16
7486	EX210LJ EX220LJ	20

TTL TYPE NUMBER	SIMILAR GATE ARRAY MACRO	PAGE
74109	JKB20LJ	24
74116	LAH22LJ	25
74138	S138LJ	18
74139	S139LJ	18
74150	S150LJ	25
74151	MU311LJ	25
74151	S151LJ	25
74153	MU220LJ	25
74153	S153LJ	25
74157	MU111LJ	25
74157	S157LJ	25
74161A	S161ALJ	18
74163A	S163ALJ	18
74164	S164LJ	31
74165	S165ALJ	31
74173	S173LJ	20
74175	S175LJ	20
74180	S180XLJ	16
74181	S181LJ	16
74182	S182LJ	16
74191	S191LJ	18
74193	S193LJ	18
74194A	S194ALJ	31
74244	S244LJ	31
74260	NO510LJ NO520LJ	26
74266	EN210LJ	20
74273	S273LJ	20
74279	LAB20LJ	25
74283	S283LJ	16
74373	S373LJ	25
74374	S374LJ	20
74375	S375LJ	25
74686	S686LJ	16
74688	S688LJ	16

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AND, AND–OR, AND–NOR GATES

FUNCTION	MACRO NAME	NUMBER OF INPUTS	OUTPUT DRIVE	CELLS USED	CHARACTERISTICS							
					ELECTRICAL			SWITCHING (C_L = 0)				
									DELAY TIME		DELTA DELAY	
HARDWIRED						C_I (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
AND GATES	AN210LJ	2	1X	2	TYP	0.07	0.44	TYP	0.48	0.54	0.88	0.49
								MAX	0.89	1.07	1.72	0.88
	AN220LJ	2	2X	2	TYP	0.07	0.6	TYP	0.55	0.6	0.44	0.3
								MAX	1.02	1.19	0.88	0.56
	AN310LJ	3	1X	2	TYP	0.07	0.56	TYP	0.65	0.65	0.89	0.5
								MAX	1.33	1.36	1.72	0.94
	AN320LJ	3	2X	3	TYP	0.07	0.73	TYP	0.71	0.67	0.46	0.31
								MAX	1.42	1.43	0.92	0.59
	AN410LJ	4	1X	3	TYP	0.07	0.57	TYP	0.77	0.67	0.9	0.52
								MAX	1.66	1.46	1.76	0.98
	AN420LJ	4	2X	3	TYP	0.07	0.83	TYP	0.87	0.7	0.48	0.33
								MAX	1.86	1.54	0.97	0.65
	AN510LJ	5	1X	3	TYP	0.07	0.65	TYP	0.99	0.74	0.92	0.54
								MAX	2.27	1.67	1.83	1.03
	AN810LJ	8	1X	5	TYP	0.07	0.94	TYP	0.88	0.7	1.69	0.52
								MAX	1.89	1.54	3.41	0.98
AND–OR GATES	A0220LJ	4	2X	3	TYP	0.07	0.76	TYP	0.62	0.97	0.46	0.38
	$Y = (A \cdot B)+(C \cdot D)$							MAX	1.28	2.35	0.9	0.74
	A0320LJ	6	1X	4	TYP	0.07	0.6	TYP	0.8	1.06	0.89	0.63
	$Y = (A1 \cdot A2 \cdot A3)+(B1 \cdot B2 \cdot B3)$							MAX	1.82	2.84	1.78	1.22
AND–NOR GATES	A0221LJ	4	1X	2	TYP	0.07	0.28	TYP	0.5	0.38	1.68	0.75
	$Y = \overline{(A \cdot B)+(C \cdot D)}$							MAX	1.25	0.7	3.42	1.5
	A0241LJ	4	2X	6	TYP	0.07	0.4	TYP	1.23	0.92	0.44	0.3
	$Y = \overline{(A1 \cdot A2)+(B1 \cdot B2)+(C1 \cdot C2)+(D1 \cdot D2)}$							MAX	3.15	1.95	0.88	0.59
	A0421LJ	8	1X	4	TYP	0.07	0.38	TYP	0.72	0.62	1.67	1.3
	$Y = \overline{(A1 \cdot A2 \cdot A3 \cdot A4)+(B1 \cdot B2 \cdot B3 \cdot B4)}$							MAX	2.13	1.63	3.43	2.79

ARITHMETIC FUNCTIONS

FUNCTION					CHARACTERISTICS							
					ELECTRICAL			SWITCHING (C_L = 0)				
									DELAY TIME		DELTA DELAY	
ARITHMETIC OPERATORS (SOFTWARE)	MACRO NAME	WIDTH OR SIZE	OUTPUT DRIVE	CELLS USED		C_I (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
1-BIT FULL ADDER	AD100LJ	1-BIT	1X	9	TYP	0.34	1.72	TYP MAX	1.2 2.44	1.51 3.27	0.89 1.71	0.51 0.91
MAGNITUDE COMPARATOR	S085LJ	4-BITS	2X	58	TYP	MULTI	9.83	TYP MAX	4.6 8.9	5.5 10.8	0.44 0.84	0.32 0.44
PARITY TREE	S180XLJ	8-BITS	1X	21	TYP	0.17	5.32	TYP MAX	3.2 6.1	3.1 5.9	0.89 1.72	0.5 0.9
ALU with LOOK-AHEAD	S181LJ	4-BITS	1X	125	TYP	MULTI	24.01	TYP MAX	7.4 13.1	6.7 11.7	0.88 1.74	1.27 2.66
LOOK-AHEAD CARRY GEN.	S182LJ	4 STAGES	2X	35	TYP	MULTI	6.62	TYP MAX	2.5 4.3	2.3 4.1	1.68 3.42	0.75 1.5
RIPPLE ADDER	S283LJ	4-BITS	2X	69	TYP	MULTI	13.35	TYP MAX	3.8 6.9	3.4 6.5	0.44 0.84	0.32 0.44
MAGNITUDE COMPARATOR	S686LJ	8-BITS	2X	104	TYP	MULTI	23.51	TYP MAX	3.2 5.7	4.2 7.9	0.44 0.9	0.64 1.34
IDENTITY COMPARATOR	S688LJ	8-BITS	2X	32	TYP	MULTI	5.57	TYP MAX	2.5 4.4	3.2 6.3	0.44 0.84	0.32 0.44

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BOOLEANS, BUFFERS, CLOCK GENERATOR/DRIVERS

FUNCTION					CHARACTERISTICS							
					ELECTRICAL			SWITCHING (C_L = 0)				
									DELAY TIME		DELTA DELAY	
HARDWIRED	MACRO NAME	NUMBER OF INPUTS	OUTPUT DRIVE	CELLS USED		C_i (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
HARDWIRED MULTI-STAGE GATES	BF001LJ	3	1X	2	TYP	0.07	0.19	TYP	0.46	0.37	1.67	0.67
	$Y = \overline{A1+(B1 \cdot B2)}$							MAX	1.12	0.59	3.4	1.46
	BF006LJ	4	1X	2	TYP	0.07	0.18	TYP	0.6	0.36	2.49	0.64
	$Y = \overline{A1+A2+(B1 \cdot B2)}$							MAX	1.77	0.63	5.1	1.53
	BF011LJ	6	1X	3	TYP	0.07	0.34	TYP	0.8	0.42	2.5	0.76
	$Y = \overline{(A1 \cdot A2)+(B1 \cdot B2)+(C1 \cdot C2)}$							MAX	2.39	0.77	5.12	1.58
	BF022LJ	6	1X	3	TYP	0.07	0.31	TYP	1.19	0.53	2.49	1.05
	$Y = \overline{A1 \cdot A2+[B1 \cdot B2 \cdot (C1+C2)]}$							MAX	2.69	1.07	5.1	2.2
	BF051LJ	3	1X	2	TYP	0.07	0.27	TYP	0.49	0.33	1.41	0.73
	$Y = \overline{A1 \cdot (B1+B2)}$							MAX	1.07	0.58	3.4	1.48
	BF053LJ	4	1X	2	TYP	0.07	0.3	TYP	0.52	0.38	1.69	0.74
	$Y = \overline{(A1+A2) \cdot (B1+B2)}$							MAX	1.32	0.69	3.42	1.46
	BF056LJ	4	1X	2	TYP	0.07	0.26	TYP	0.48	0.41	1.28	1
	$Y = \overline{A1 \cdot A2 \cdot (B1+B2)}$							MAX	1.39	0.86	3.4	2.06
HARDWIRED BUFFER GATES	BU130LJ	1	3X	2	TYP	0.07	0.96	TYP	0.49	0.69	0.28	0.3
								MAX	0.82	1.27	0.58	0.56
	BU150LJ	1	5X	3	TYP	0.07	1.36	TYP	0.57	0.85	0.2	0.26
								MAX	0.99	1.66	0.38	0.47
SOFTWARE with 3-STATE OUTPUTS	S244LJ	1X8 BITS 2 EN	1X	28	TYP	MULTI	6.54	TYP	1.9	2.5	0.96	0.62
								MAX	2.6	3.2	1.9	1.26

FUNCTION					CHARACTERISTICS							
					ELECTRICAL			SWITCHING (C_L = 0)				
									DELAY TIME		DELTA DELAY	
CLOCK GENERATOR DRIVERS HARDWIRED	MACRO NAME	NUMBER OF INPUTS	OUTPUT DRIVE	CELLS USED		C_i (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
CLOCK GENERATOR	CK120LJ	TWO PHASE	1X	10	TYP	0.07	4.8	TYP	5.84	1.54	.55	.33
								MAX	12.69	3.82	1.14	.62
GATE ARRAY CLOCK DRIVERS	CKD03LJ	1	25pF	40	TYP	0.32	18.1	TYP	1.94	1.95	.020	.030
								MAX	3.05	3.12	.040	.040
	CKD05LJ	1	25 pF	48	TYP	0.32	24.1	TYP	2.18	2.21	.020	.020
								MAX	3.44	3.55	.030	.030
	CKD08LJ	1	25 pF	64	TYP	0.32	31.6	TYP	2.3	2.29	.010	.020
								MAX	3.64	3.7	.020	.030
	CKD12LJ	1	35 pF	74	TYP	0.32	36.6	TYP	2.36	2.41	.010	.010
								MAX	3.75	3.87	.020	.020
	CKD15LJ	1	35 pF	82	TYP	0.32	40.8	TYP	2.45	2.5	.010	.010
								MAX	3.88	4.03	.020	.020
	CKD18LJ	1	35 pF	98	TYP	0.32	40.8	TYP	2.45	2.5	.010	.010
								MAX	3.88	4.03	.020	.020

COUNTERS, DECODERS/DEMULTIPLEXERS

FUNCTION					CHARACTERISTICS							
					ELECTRICAL			SWITCHING (C_L = 0) (See Note 12)				
									DELAY TIME		DELTA DELAY	
COUNTERS (SOFTWARE)	MACRO NAME	TYPE OF CLEAR	OUTPUT DRIVE	CELLS USED		C_i (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
4-BIT BINARY	S161ALJ	ASYNC	1X RCO=2X	79	TYP	MULTI	18.58	TYP MAX	3.9 7.1	3.5 7.1	0.9 1.73	0.52 0.96
4-BIT BINARY	S163ALJ	SYNC	1X RCO=2X	81	TYP	MULTI	17.62	TYP MAX	3.9 7.1	3.5 7.1	0.9 1.73	0.52 0.96
4-BIT UP/DOWN BINARY	S191LJ	NONE	1X	98	TYP	MULTI	23	TYP MAX	4.7 9	3.9 7.5	0.88 1.72	0.99 2.04
4-BIT UP/DOWN BINARY	S193LJ	ASYNC	1X	87	TYP	MULTI	22.6	TYP MAX	3.8 7.4	3.7 7.2	0.88 1.76	1.56 3.3

NOTE 12: Specific timing data regarding pulse duration, setup time and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked functions embedded in the software macros. Evaluations of timing requirements made during prelayout simulation, produce workstation output used to identify and resolve each specific timing need.

FUNCTION					CHARACTERISTICS							
					ELECTRICAL			SWITCHING (C_L = 0)				
									DELAY TIME		DELTA DELAY	
DECODERS/ DEMULTI-PLEXERS	MACRO NAME	SIZE	OUTPUT DRIVE	CELLS USED		C_i (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
HARDWIRED	DE210LJ	2-TO-4	1X	3	TYP	0.23	1.52	TYP MAX	0.39 0.97	0.47 1.18	0.87 1.7	0.73 1.46
3-ENABLES (SOFTWARE)	S138LJ	3-TO-8	1X	25	TYP	MULTI	5.08	TYP MAX	1.6 2.5	2.7 5.3	0.88 1.74	1.27 2.66
1-ENABLE (SOFTWARE)	S139LJ	DUAL 2-TO-4	1X	26	TYP	MULTI	7.66	TYP MAX	1.3 2.1	1.4 2.4	0.88 1.72	0.99 2.04

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D–TYPE FLIP–FLOPS

FUNCTION				CHARACTERISTICS								REQUIREMENTS	
				ELECTRICAL			SWITCHING (C_L = 0) (CLK TO Q)					TIMING	
								DELAY TIME		DELTA DELAY		SETUP (MIN)	HOLD (MIN)
D-TYPE FLIP-FLOPS HARDWIRED (f_{clock})	MACRO NAME	OUTPUT DRIVE	CELLS USED		C_I (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)	t_{su} (ns)	t_h (ns)
115 MHz with CLR and PREZ	DFB20LJ	2X	12	TYP	0.12	2.06	TYP MAX	2 4.21	1.37 2.9	0.46 0.92	0.35 0.64	3	1
100MHz with CLR and PREZ	DTB00LJ	0.5X	8	TYP	0.07	1.9	TYP MAX	1.38 2.83	1.39 2.9	1.96 3.88	1.98 3.86	2	0
170MHz with CLR and PREZ	DTB10LJ	1X	9	TYP	0.07	2.1	TYP MAX	1.46 3.11	1.53 3.2	0.88 1.7	0.52 0.96	1.9	0
193 MHz with CLR and PREZ	DTB20LJ	2X	10	TYP	0.07	2.6	TYP MAX	1.68 3.64	1.65 3.53	0.42 0.84	0.32 0.6	2.1	0.6
100 MHz with CLR	DTC00LJ	0.5X	7	TYP	0.07	1.8	TYP MAX	1.29 2.57	1.33 2.76	1.92 3.82	1.86 3.58	2	0
185 MHz with CLR	DTC10LJ	1X	8	TYP	0.07	2.1	TYP MAX	1.44 3.02	1.54 3.21	0.9 1.72	0.52 0.96	1.5	0.7
208 MHz with CLR	DTC20LJ	2X	9	TYP	0.07	2.6	TYP MAX	1.63 3.46	1.64 3.45	0.44 0.86	0.32 0.62	1.6	0.7
100 MHz	DTN00LJ	0.5X	6	TYP	0.07	1.7	TYP MAX	1.23 2.48	1.26 2.55	1.6 3.06	1.84 3.6	2	0
179 MHz	DTN10LJ	1X	7	TYP	0.07	2	TYP MAX	1.32 2.75	1.43 2.99	0.88 1.68	0.52 0.92	0.7	0.6
208 MHz	DTN20LJ	2X	8	TYP	0.07	2.4	TYP MAX	1.49 3.19	1.56 3.24	0.44 0.82	0.3 0.6	0.7	0.6
95 MHz with PREZ	DTP00LJ	0.5X	7	TYP	0.07	1.9	TYP MAX	1.35 2.65	1.44 2.91	1.58 3.06	1.96 3.84	2	0
167 MHz with PREZ	DTP10LJ	1X	8	TYP	0.07	2.2	TYP MAX	1.34 2.75	1.55 3.19	0.88 1.7	0.52 0.92	1.6	0
200 MHz with PREZ	DTP20LJ	2X	9	TYP	0.07	2.5	TYP MAX	1.53 3.18	1.69 3.5	0.42 0.82	0.3 0.6	1.6	0

D–TYPE FLIP–FLOPS, DELAY ELEMENTS, EX–NOR AND EX–OR GATES

FUNCTION				CHARACTERISTICS							
				ELECTRICAL			SWITCHING (C_L = 0) (See Note 13)				
								DELAY TIME		DELTA DELAY	
D-TYPE FLIP-FLOPS (SOFTWARE)	MACRO NAME	OUTPUT DRIVE	CELLS USED		C_i (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
4-BIT 3-STATE with CLR	S173LJ	1X	53	TYP	MULTI	14.37	TYP MAX	2.3 4.5	2.5 5.1	0.96 1.9	0.64 1.26
4-BIT COMP OUTPUTS with CLR	S175LJ	1X	31	TYP	MULTI	9.18	TYP MAX	1.8 3.9	1.7 3.5	0.9 1.73	0.52 0.96
8-BIT with CLR	S273LJ	1X	55	TYP	MULTI	8.03	TYP MAX	1.4 2.8	1.6 3.4	0.89 1.72	0.51 0.95
8-BIT with 3-STATE	S374 LJ	1X	76	TYP	MULT	20.3	TYP MAX	2.3 4.5	2.5 5.1	0.96 1.9	0.64 1.26

NOTE 13: Specific timing data regarding pulse duration, setup time and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked functions embedded in the software macros. Evaluations of timing requirements made during prelayout simulation, produce workstation output used to identify and resolve each specific timing need.

FUNCTION					CHARACTERISTICS							
					ELECTRICAL			SWITCHING (C_L = 0)				
									DELAY TIME		DELTA DELAY	
DELAY ELEMENTS HARDWIRED	MACRO NAME	FUNCTION	OUTPUT DRIVE	CELLS USED		C_i (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
LEVEL RESTORER	DLD00LJ	LOGIC DRIVER	2X	2	TYP	0.17	0.64	TYP MAX	0.59 1.26	0.42 0.92	0.44 0.86	0.49 0.87
DELAY ELEMENT	DLE00LJ	2 ns TYP DELAY	DRIVES ONLY DLD00LJ or DLE00LJ	3	TYP	0.23	0.6	TYP MAX	1.58 3.73	1.92 4.45	2.55 5.19	1.24 2.57

FUNCTION					CHARACTERISTICS							
					ELECTRICAL			SWITCHING (C_L = 0)				
									DELAY TIME		DELTA DELAY	
EX-NOR, EX-OR GATES HARDWIRED	MACRO NAME	NUMBER OF INPUTS	OUTPUT DRIVE	CELLS USED		C_i (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
EX-NOR GATE	EN210LJ	2	1X	3	TYP	0.17	0.52	TYP MAX	0.57 1.09	0.85 2.02	0.89 1.72	0.57 1.06
EX-OR GATES	EX210LJ	2	1X	3	TYP	0.17	0.76	TYP MAX	0.81 1.6	0.75 1.48	0.89 1.72	0.5 0.9
	EX220LJ	2	2X	4	TYP	0.16	1.1	TYP MAX	0.86 1.75	0.81 1.61	0.45 0.88	0.3 0.56

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INPUT BUFFERS

FUNCTION			CHARACTERISTICS							
			ELECTRICAL			SWITCHING (C_L = 0)				
							DELAY TIME		DELTA DELAY	
INPUT BUFFERS (HARDWIRED)	MACRO NAME	INPUT THRESHOLD VOLTAGE		C_I (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
INVERTING	IPI00LJ	2.5 (CMOS)	TYP	3.79	2.63	TYP MAX	0.95 1.64	1.13 1.87	0.18 0.38	0.16 0.25
NONINVERTING	IPI01LJ	2.5 (CMOS)	TYP	3.79	1.8	TYP MAX	1.1 1.63	0.77 1.36	0.2 0.39	0.17 0.27
	IPI04LJ	1.3 (TTL)	TYP	3.79	2.18	TYP MAX	1.62 2.39	1.22 2.82	0.2 0.39	0.26 0.62
INVERTING with HYSTERESIS	IPI06LJ	0.9/3.85 (CMOS)	TYP	3.79	2.04	TYP MAX	2.22 2.8	2.31 3.05	0.81 1.48	0.92 1.7
NONINVERTING with HYSTERESIS	IPI09LJ	0.8/2 (TTL)	TYP	3.79	2.15	TYP MAX	1.74 2.59	2.71 5.27	0.24 0.45	0.44 0.83
WITH 70-μA PULL-UP CURRENT SOURCE	IPL01LJ	2.5 (CMOS)	TYP	3.79	1.82	TYP MAX	1.15 1.71	0.82 1.45	0.19 0.36	0.18 0.24
	IPL04LJ	1.3 (TTL)	TYP	3.79	2.31	TYP MAX	1.66 2.44	1.23 2.84	0.19 0.39	0.26 0.62
WITH 70-μA PULL-DOWN CURRENT SOURCE	IPU01LJ	2.5 (CMOS)	TYP	3.79	1.82	TYP MAX	1.16 1.7	0.8 1.4	0.19 0.36	0.14 0.25
	IPU04LJ	1.3 (TTL)	TYP	3.79	2.31	TYP MAX	1.68 2.47	1.29 3.01	0.19 0.37	0.26 0.64

BIDIRECTIONAL INPUT/OUTPUT BUFFERS

FUNCTION				OUTPUT CHARACTERISTICS								INPUT CHARACTERISTICS				
				ELECTRICAL			SWITCHING† (C_L = 15 pF)					ELEC-TRICAL	SWITCHING (C_L = 0 pF)			
								DELAY TIME		DELTA DELAY			DELAY TIME		DELTA DELAY	
I/O 3-STATE BIDIREC-TIONAL HARDWIRED	MACRO NAME	OUTPUT CURRENT (mA)	INPUT THRESH-OLD VOLTAGE		C_I (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)	CI (pF)	t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
	IOI21LJ	2	2.5 (CMOS)	TYP	0.23	11.5	TYP	4.29	5.04	0.16	0.14	7.1	1.09	0.79	0.22	0.14
							MAX	8.31	9.66	0.3	0.25		1.65	1.35	0.37	0.27
	IOI24LJ	2	1.3 (TTL)	TYP	0.23	11.4	TYP	4.31	5.03	0.16	0.14	7.1	1.63	1.32	0.2	0.29
							MAX	8.33	9.63	0.3	0.25		2.38	3.14	0.4	0.67
	IOI41LJ	4	2.5 (CMOS)	TYP	0.23	10.9	TYP	2.88	3.84	0.08	0.07	7.1	1.09	0.79	0.22	0.14
							MAX	5.72	7.7	0.15	0.13		1.65	1.35	0.37	0.27
	IOI44LJ	4	1.3 (TTL)	TYP	0.23	11.7	TYP	2.88	3.84	0.08	0.07	7.1	1.63	1.31	0.2	0.28
							MAX	5.72	7.69	0.15	0.13		2.38	3.09	0.4	0.66
	IOI81LJ	8	2.5 (CMOS)	TYP	0.23	12.6	TYP	2.56	3.58	0.04	0.05	7.1	1.09	0.79	0.22	0.14
							MAX	5.29	7.53	0.08	0.09		1.65	1.35	0.37	0.27
	IOI84LJ	8	1.3 (TTL)	TYP	0.23	13.4	TYP	2.56	3.58	0.04	0.05	7.1	1.63	1.29	0.2	0.26
							MAX	5.29	7.53	0.08	0.09		2.38	2.99	0.4	0.64
WITH dI/dt CONTROL	IOK21LJ	2	2.5 (CMOS)	TYP	0.23	10.4	TYP	5.21	7.88	0.16	0.15	7.13	1.1	0.79	0.21	0.14
							MAX	10.27	15.14	0.3	0.27		1.65	1.37	0.37	0.26
	IOK24LJ	2	1.3 (TTL)	TYP	0.23	12.6	TYP	5.22	7.86	0.16	0.15	7.13	1.64	1.33	0.2	0.29
							MAX	10.3	15.11	0.3	0.27		2.39	3.15	0.4	0.67
	IOK41LJ	4	2.5 (CMOS)	TYP	0.23	11.8	TYP	4.12	6.75	0.08	0.09	7.13	1.1	0.79	0.21	0.14
							MAX	8.38	13.41	0.16	0.17		1.65	1.37	0.37	0.26
	IOK44LJ	4	1.3 (TTL)	TYP	0.23	12.1	TYP	4.12	6.74	0.08	0.09	7.13	1.64	1.32	0.2	0.28
							MAX	8.39	13.4	0.16	0.17		2.39	3.11	0.4	0.66
	IOK81LJ	8	2.5 (CMOS)	TYP	0.23	13.2	TYP	4.17	6.82	0.05	0.07	7.13	1.1	0.79	0.21	0.14
							MAX	8.8	14.06	0.1	0.13		1.65	1.37	0.37	0.26
	IOK84LJ	8	1.3 (TTL)	TYP	0.23	13.4	TYP	4.18	6.81	0.05	0.07	7.13	1.64	1.29	0.2	0.26
							MAX	8.8	14.05	0.1	0.13		2.39	3	0.4	0.64

† CMOS threshold measurements are shown.

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BIDIRECTIONAL INPUT/OUTPUT BUFFERS

FUNCTION				OUTPUT CHARACTERISTICS								INPUT CHARACTERISTICS				
				ELECTRICAL			SWITCHING† (C_L = 15 pF)					ELEC-TRICAL	SWITCHING (C_L = 0 pF)			
								DELAY TIME		DELTA DELAY			DELAY TIME		DELTA DELAY	
I/O 3-STATE BIDIREC-TIONAL HARDWIRED	MACRO NAME	OUTPUT CURRENT (mA)	INPUT THRESH-OLD VOLTAGE		C_i (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)	CI (pF)	t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
WITH 70-μA PULL-UP	IOL21LJ	2	2.5 (CMOS)	TYP	0.23	19.3	TYP	4.28	5.08	0.16	0.14	7.1	1.15	0.83	0.19	0.17
							MAX	8.27	9.74	0.3	0.25		1.7	1.44	0.36	0.24
	IOL24LJ	2	1.3 (TTL)	TYP	0.23	19.3	TYP	4.29	5.07	0.16	0.14	7.1	1.64	1.34	0.2	0.29
							MAX	8.29	9.72	0.3	0.25		2.43	3.17	0.39	0.66
	IOL41LJ	4	2.5 (CMOS)	TYP	0.23	18.8	TYP	2.88	3.87	0.08	0.07	7.1	1.15	0.83	0.19	0.17
							MAX	5.71	7.75	0.15	0.13		1.7	1.44	0.36	0.24
	IOL44LJ	4	1.3 (TTL)	TYP	0.23	19.3	TYP	2.88	3.86	0.08	0.07	7.1	1.64	1.32	0.2	0.29
							MAX	5.71	7.74	0.15	0.13		2.43	3.12	0.39	0.66
	IOL81LJ	8	2.5 (CMOS)	TYP	0.23	20.4	TYP	2.56	3.6	0.04	0.05	7.1	1.15	0.83	0.19	0.17
							MAX	5.28	7.56	0.08	0.09		1.7	1.44	0.36	0.24
	IOL84LJ	8	1.3 (TTL)	TYP	0.23	21.3	TYP	2.56	3.59	0.04	0.05	7.1	1.64	1.3	0.2	0.27
							MAX	5.28	7.56	0.08	0.09		2.43	3.01	0.39	0.64
WITH di/dt CONTROL and 70-μA PULL-UP	ION21LJ	2	2.5 (CMOS)	TYP	0.23	18	TYP	5.19	7.93	0.16	0.15	7.13	1.15	0.82	0.19	0.18
							MAX	10.22	15.24	0.3	0.27		1.71	1.45	0.36	0.24
	ION24LJ	2	1.3 (TTL)	TYP	0.23	20	TYP	5.2	7.92	0.16	0.15	7.13	1.66	1.35	0.19	0.29
							MAX	10.25	15.21	0.3	0.27		2.44	3.19	0.39	0.66
	ION41LJ	4	2.5 (CMOS)	TYP	0.23	19.6	TYP	4.11	6.78	0.08	0.09	7.13	1.15	0.82	0.19	0.18
							MAX	8.36	13.47	0.16	0.17		1.71	1.45	0.36	0.24
	ION44LJ	4	1.3 (TTL)	TYP	0.23	19.7	TYP	4.11	6.78	0.08	0.09	7.13	1.66	1.33	0.19	0.29
							MAX	8.37	13.46	0.16	0.17		2.44	3.13	0.39	0.66
	ION81LJ	8	2.5 (CMOS)	TYP	0.23	21.6	TYP	4.17	6.84	0.05	0.07	7.13	1.15	0.82	0.19	0.18
							MAX	8.79	14.11	0.1	0.13		1.71	1.45	0.36	0.24
	ION84LJ	8	1.3 (TTL)	TYP	0.23	21	TYP	4.17	6.84	0.05	0.07	7.13	1.66	1.3	0.19	0.27
							MAX	8.79	14.09	0.1	0.13		2.44	3.03	0.39	0.64
WITH 70-μA PULL-DOWN	IOU21LJ	2	2.5 (CMOS)	TYP	0.23	16.8	TYP	4.33	5.02	0.16	0.14	7.1	1.16	0. 8	0.19	0.14
							MAX	8.37	9.61	0.3	0.25		1.7	1.39	0.36	0.25
	IOU24LJ	2	1.3 (TTL)	TYP	0.23	17.2	TYP	4.34	5	0.16	0.14	7.1	1.68	1.37	0.19	0.29
							MAX	8.4	9.59	0.3	0.25		2.45	3.3	0.38	0.67
	IOU41LJ	4	2.5 (CMOS)	TYP	0.23	16.5	TYP	2.89	3.84	0.08	0.07	7.1	1.15	0.8	0.19	0.14
							MAX	5.75	7.69	0.15	0.13		1.7	1.39	0.36	0.25
	IOU44LJ	4	1.3 (TTL)	TYP	0.23	17.3	TYP	2.89	3.83	0.08	0.07	7.1	1.68	1.36	0.19	0.26
							MAX	5.75	7.68	0.15	0.13		2.45	3.25	0.38	0.67
	IOU81LJ	8	2.5 (CMOS)	TYP	0.23	18.2	TYP	2.57	3.58	0.04	0.05	7.1	1.15	0.8	0.19	0.14
							MAX	5.3	7.53	0.08	0.09		1.7	1.39	0.36	0.25
	IOU84LJ	8	1.3 (TTL)	TYP	0.23	19.1	TYP	2.57	3.58	0.04	0.05	7.1	1.68	1.33	0.19	0.29
							MAX	5.3	7.52	0.08	0.09		2.45	3.15	0.38	0.67
WITH di/dt CONTROL and 70-μA PULL-DOWN	IOW21LJ	2	2.5 (CMOS)	TYP	0.23	16	TYP	5.24	7.84	0.16	0.15	7.13	1.16	0. 8	0.19	0.14
							MAX	10.33	15.06	0.3	0.27		1.71	1.39	0.36	0.25
	IOW24LJ	2	1.3 (TTL)	TYP	0.23	17.8	TYP	5.25	7.82	0.16	0.15	7.13	1.68	1.38	0.19	0.29
							MAX	10.36	15.03	0.3	0.27		2.47	3.32	0.37	0.67
	IOW41LJ	4	2.5 (CMOS)	TYP	0.23	17.4	TYP	4.13	6.73	0.08	0.09	7.13	1.16	0.8	0.19	0.14
							MAX	8.4	13.37	0.16	0.17		1.71	1.39	0.36	0.25
	IOW44LJ	4	1.3 (TTL)	TYP	0.23	17.7	TYP	4.13	6.73	0.08	0.09	7.13	1.68	1.37	0.19	0.29
							MAX	8.41	13.36	0.16	0.17		2.47	3.28	0.37	0.66
	IOW81LJ	8	2.5 (CMOS)	TYP	0.23	19.8	TYP	4.18	6.81	0.05	0.07	7.13	1.16	0.8	0.19	0.14
							MAX	8.82	14.04	0.1	0.13		1.71	1.39	0.36	0.25
	IOW84LJ	8	1.3 (TTL)	TYP	0.23	19	TYP	4.18	6.8	0.05	0.07	7.13	1.68	1.33	0.19	0.29
							MAX	8.81	14.02	0.1	0.13		2.47	3.17	0.37	0.67

† CMOS threshold measurements are shown.

INVERTERS, 3–STATE INVERTERS, J–K FLIP–FLOPS

FUNCTION					CHARACTERISTICS							
					ELECTRICAL			SWITCHING (C_L = 0)				
									DELAY TIME		DELTA DELAY	
HARDWIRED	MACRO NAME	NUMBER OF INPUTS	OUTPUT DRIVE	CELLS USED		C_I (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
INVERTERS	IV110LJ	1	1X	1	TYP	0.07	0.21	TYP MAX	0.26 0.36	0.28 0.41	0.86 1.68	0.5 0.82
	IV120LJ	1	2X	1	TYP	0.15	0.39	TYP MAX	0.24 0.32	0.19 0.36	0.44 0.84	0.32 0.44
	IV140LJ	1	4X	2	TYP	0.31	0.8	TYP MAX	0.2 0.34	0.13 0.28	0.26 0.4	0.22 0.3
3-STATE INVERTER	IV211LJ	2	1X	2	TYP	0.08	0.38	TYP MAX	0.45 0.77	0.43 0.66	0.96 1.9	0.64 1.26
	IV221LJ	2	2X	4	TYP	0.23	0.96	TYP MAX	0.38 0.62	0.33 0.58	0.45 0.88	0.31 0.61
	IV241LJ	2	4X	5	TYP	0.38	1.36	TYP MAX	0.33 0.52	0.29 0.58	0.26 0.52	0.25 0.48

FUNCTION				CHARACTERISTICS							REQUIREMENTS	
				ELECTRICAL			SWITCHING (C_L = 0) (CLK to Q)				TIMING	
								DELAY TIME		DELTA DELAY		
J–$\overline{K}$ FLIP-FLOPS HARDWIRED (f_{clock})	MACRO NAME	OUTPUT DRIVE	CELLS USED		C_I (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)	SETUP (MIN) t_{su} (ns)	HOLD (MIN) t_h (ns)
135 MHz with CLR and PREZ	JKB20LJ	2X	12	TYP	0.08	3	TYP MAX	2.13 4.45	2.07 4.34	0.44 0.86	0.34 0.64	4	0
135 MHz with CLR and PREZ	JKB21LJ (NEG EDGE CLOCK)	2X	12	TYP	0.08	3.2	TYP MAX	2.08 4.33	2.28 4.81	0.44 0.88	0.34 0.66	3	0

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LATCHES, MULTIPLEXERS

FUNCTION					CHARACTERISTICS								
					ELECTRICAL				SWITCHING (C_L = 0) (See Note 14)				
										DELAY TIME		DELTA DELAY	
LATCHES	MACRO NAME	WIDTH OR SIZE	OUTPUT DRIVE	CELLS USED		INPUT	C_i (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
HARDWIRED	LAB20LJ	1-BIT	2X	4	TYP	RZ SZ	0.07 0.07	1.6	TYP MAX	1.1 2.24	0.68 1.28	0.44 0.86	0.3 0.6
	LAH12LJ	1-BIT	1X	5	TYP	C D	0.15 0.07	1.48	TYP MAX	1.27 2.5	1.43 2.85	0.97 1.88	0.64 1.27
	LAH13LJ	1-BIT	1X	5	TYP	C D	0.15 0.07	1.48	TYP MAX	1.26 2.53	1.16 2.23	0.96 1.89	0.63 1.27
	LAH14LJ	1-BIT	1X	7	TYP	C D	0.15 0.07	1.8	TYP MAX	1.43 2.81	1.55 3.11	0.96 1.89	0.64 1.26
	LAH20LJ	1-BIT	2X	5	TYP	C D	0.17 0.07	2.2	TYP MAX	1.31 2.64	1.48 3.05	0.44 0.86	0.3 0.6
	LAH22LJ	1-BIT	2X	4	TYP	C D	0.15 0.07	0.8	TYP MAX	0.89 1.73	0.99 1.99	0.48 0.96	0.38 0.73
	LH110LJ	1-BIT	1X	4	TYP	I/O	0.56	0.76	TYP MAX	–	–	(0.56 pF)	(0.56 pF)
	LH400LJ	4-BIT	1X	11	TYP	C Dn	0.07 0.08	3.92	TYP MAX	1.35 2.73	1.51 3.07	1.59 3.09	1.85 3.61
SOFTWARE	S373LJ	8-BITS	1X	47	TYP	C Dn,OCZ	0.07 0.31	10.06	TYP MAX	1.8 3.4	2.3 4.4	0.96 1.9	0.64 1.26
	S375LJ	4-BITS	2X	16	TYP	ANY	0.07	3.52	TYP MAX	2 4.2	1.9 3.2	0.44 0.84	0.32 0.44

NOTE 14: Specific timing data regarding pulse duration, setup time and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked functions embedded in the software macros. Evaluations of timing requirements made during prelayout simulation, produce workstation output used to identify and resolve each specific timing need.

FUNCTION					CHARACTERISTICS							
					ELECTRICAL			SWITCHING (C_L = 0)				
									DELAY TIME		DELTA DELAY	
MULTIPLEXERS	MACRO NAME	SIZE	OUTPUT DRIVE	CELLS USED		C_i (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
HARDWIRED	MU111LJ	2-TO-1	1X	3	TYP	0.07 0.18	0.68	TYP MAX	0.62 1.36	0.81 1.87	0.89 1.72	0.57 1.1
	MU220LJ	4-TO-1	1X	7	TYP	0.07 0.24	1.4	TYP MAX	0.95 1.87	1.11 2.33	0.47 0.94	0.49 1
	MU311LJ	8-TO-1	1X	13	TYP	0.07 0.42	1.32	TYP MAX	1.28 2.61	1.5 3.27	0.91 1.81	0.88 1.8
SOFTWARE	S150LJ	16-TO-1	2X	122	TYP GZ	0.07 0.15	26.07	TYP MAX	4.3 8.2	4.5 9	0.44 0.84	0.32 0.44
	S151LJ	8-TO-1	2X	40	TYP GZ	0.07 0.15	7.82	TYP MAX	3.5 6.6	3.5 6.8	0.44 0.84	0.32 0.44
	S153LJ	DUAL 4-TO-1	1X	26	TYP	0.07	5.24	TYP MAX	2.4 4.1	2.2 3.9	0.88 1.74	1.27 2.66
	S157LJ	QUAD 2-TO-1	1X	18	TYP A/B	0.07 0.14	4.98	TYP MAX	2.5 4.1	2.4 3.9	0.87 1.7	0.72 1.44

NAND, NOR, OR–AND, OR–NAND GATES

FUNCTION					CHARACTERISTICS							
					ELECTRICAL			SWITCHING (C_L = 0)				
									DELAY TIME		DELTA DELAY	
HARDWIRED	MACRO NAME	NUMBER OF INPUTS	OUTPUT DRIVE	CELLS USED		C_I (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
NAND GATES	NA210LJ	2	1X	1	TYP	0.07	0.27	TYP	0.3	0.33	0.87	0.72
								MAX	0.52	0.47	1.7	1.44
	NA220LJ	2	2X	2	TYP	0.15	0.52	TYP	0.29	0.28	0.43	0.39
								MAX	0.5	0.46	0.84	0.72
	NA310LJ	3	1X	2	TYP	0.07	0.28	TYP	0.36	0.4	0.88	0.99
								MAX	0.73	0.72	1.72	2.04
	NA311LJ	3	1X	2	TYP	0.07	0.6	TYP	0.38	0.46	0.88	0.99
	$Y = (-A) \cdot B \cdot C$							MAX	0.78	1.09	1.72	2.05
	NA320LJ	3	2X	3	TYP	0.15	0.52	TYP	0.34	0.36	0.44	0.5
								MAX	0.65	0.61	0.86	1.04
	NA410LJ	4	1X	2	TYP	0.07	0.29	TYP	0.4	0.46	0.88	1.27
								MAX	0.82	0.95	1.74	2.66
	NA420LJ	4	2X	4	TYP	0.15	0.56	TYP	0.38	0.44	0.44	0.64
								MAX	0.77	0.92	0.9	1.34
	NA510LJ	5	1X	3	TYP	0.07	0.34	TYP	0.46	0.61	0.88	1.56
								MAX	1.01	1.43	1.76	3.3
	NA520LJ	5	2X	5	TYP	0.15	0.6	TYP	0.42	0.56	0.45	0.78
								MAX	0.89	1.26	0.92	1.66
	NA810LJ	8	1X	6	TYP	0.07	1.2	TYP	0.85	1.26	0.88	0.55
								MAX	1.86	2.75	1.72	1.02
	NA820LJ	8	2X	6	TYP	0.07	1.7	TYP	0.9	1.36	0.44	0.37
								MAX	1.97	3.04	0.86	0.7
NOR GATES	NO210LJ	2	1X	1	TYP	0.07	0.18	TYP	0.35	0.31	1.67	0.5
								MAX	0.67	0.49	3.4	0.82
	NO220LJ	2	2X	2	TYP	0.15	0.3	TYP	0.35	0.23	0.82	0.32
								MAX	0.62	0.43	1.72	0.45
	NO310LJ	3	1X	2	TYP	0.07	0.21	TYP	0.57	0.34	2.48	0.49
								MAX	1.45	0.51	5.1	0.88
	NO320LJ	3	2X	3	TYP	0.15	0.34	TYP	0.49	0.25	1.23	0.31
								MAX	1.22	0.47	2.58	0.45
	NO410LJ	4	1X	4	TYP	0.07	0.23	TYP	0.95	0.68	0.88	0.49
								MAX	1.95	1.47	1.71	0.88
	NO420LJ	4	2X	4	TYP	0.07	1.2	TYP	1.02	0.74	0.45	0.3
								MAX	2.15	1.61	0.87	0.59
	NO510LJ	5	1X	4	TYP	0.07	0.96	TYP	1.19	0.71	0.88	0.5
								MAX	3.12	1.5	1.7	0.9
	NO520LJ	5	2X	5	TYP	0.07	1.25	TYP	1.22	0.77	0.45	0.3
								MAX	3.08	1.66	0.88	0.58
	NO810LJ	8	1X	6	TYP	0.07	1.3	TYP	1.63	0.75	0.89	0.49
								MAX	4.23	1.56	1.72	0.9
	NO820LJ	8	2X	6	TYP	0.07	1.4	TYP	1.72	0.81	0.45	0.3
								MAX	4.49	1.7	0.9	0.56
OR-AND	OA220LJ	4	2X	3	TYP	0.07	0.6	TYP	0.63	0.99	0.45	0.39
	$Y = (A1+A2) \cdot (B1+B2)$							MAX	1.25	2.38	0.88	0.78
OR-NAND GATES	OA231LJ	6	1X	3	TYP	0.07	0.38	TYP	0.64	0.48	1.69	1
	$Y = \overline{(A1+A2) \cdot (B1+B2) \cdot (C1+C2)}$							MAX	1.78	1.03	3.42	2.07
	OA241LJ	8	1X	4	TYP	0.07	0.4	TYP	0.88	0.97	1.72	1.29
	$Y = \overline{(A1+A2) \cdot (B1+B2) \cdot (C1+C2) \cdot (D1+D2)}$							MAX	2.47	2.35	3.43	2.7

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TOTEM–POLE, 3–STATE OUTPUTS

FUNCTION OUTPUT TOTEM-POLE HARDWIRED	MACRO NAME	OUTPUT CURRENT (Source/Sink) (mA)	OUTPUT CHARACTERISTICS							
			ELECTRICAL			SWITCHING† (C_L = 15 pF)				
							DELAY TIME		DELTA DELAY	
				C_i (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ps/pF)	Δt_{PHL} (ps/pF)
	OPIA0LJ	12/16	TYP	0.41	13	TYP MAX	1.56 2.92	1.76 3.45	30 50	20 40
	OPIH0LJ	12/12	TYP	0.41	12.9	TYP MAX	1.56 2.91	1.78 3.42	30 50	30 50
	OPIJ0LJ	12/20	TYP	0.41	13.2	TYP MAX	1.57 2.92	1.8 3.6	30 50	10 30
	OPI20LJ	2/2	TYP	0.23	7.36	TYP MAX	3.91 7.36	4.01 7.28	160 300	140 250
	OPI40LJ	4/4	TYP	0.41	8.51	TYP MAX	2.24 4.17	2.36 4.28	80 150	70 120
	OPI80LJ	8/8	TYP	0.41	10.5	TYP MAX	1.63 3.02	1.86 3.5	40 70	40 70
WITH dI/dt CONTROL	OPKA0LJ	12/16	TYP	0.41	10.6	TYP MAX	3.73 7.7	5.66 11.6	40 80	50 90
	OPKH0LJ	12/12	TYP	0.41	10.3	TYP MAX	3.72 7.68	5.24 10.6	40 80	50 90
	OPKJ0LJ	12/20	TYP	0.41	10.9	TYP MAX	3.73 7.71	6.24 12.9	40 80	40 80
	OPK20LJ	2/2	TYP	0.23	7.44	TYP MAX	4.63 8.98	6.53 12.19	160 300	150 260
	OPK40LJ	4/4	TYP	0.41	8.28	TYP MAX	3.47 6.81	5.3 10.04	80 150	80 150
	OPK80LJ	8/8	TYP	0.41	9.36	TYP MAX	3.38 6.87	5.23 10.28	50 90	60 110

FUNCTION OUTPUT 3-STATE HARDWIRED	MACRO NAME	OUTPUT CURRENT (Source/Sink) (mA)	OUTPUT CHARACTERISTICS								
			ELECTRICAL				SWITCHING† (C_L = 15 pF)				
				A	GZ			DELAY TIME		DELTA DELAY	
				C_i (pF)	C_{pd} (pF)	Cpd (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ps/pF)	Δt_{PHL} (ps/pF)
	OPI23LJ	2/2	TYP	0.23	0.18	7.34	TYP MAX	4.14 8	4.91 9.41	160 300	140 250
	OPI43LJ	4/4	TYP	0.23	0.18	7.95	TYP MAX	2.81 5.57	3.77 7.56	80 150	70 140
	OPI83LJ	8/8	TYP	0.23	0.18	10.1	TYP MAX	2.52 5.2	3.53 7.43	40 80	50 90
WITH dI/dt CONTROL	OPK23LJ	2/2	TYP	0.23	0.18	7.56	TYP MAX	5.06 9.98	7.74 14.88	160 300	150 270
	OPK43LJ	4/4	TYP	0.23	0.18	8.16	TYP MAX	4.04 8.23	6.66 13.24	80 160	90 170
	OPK83LJ	8/8	TYP	0.23	0.18	9.04	TYP MAX	4.12 8.69	6.75 13.92	50 100	70 130

† CMOS threshold measurements are shown.

OPEN–DRAIN OUTPUTS, OR GATES

FUNCTION			OUTPUT CHARACTERISTICS							
			ELECTRICAL			SWITCHING† (C_L = 15 pF)				
							DELAY TIME		DELTA DELAY	
OUTPUT OPEN-DRAIN HARDWIRED	MACRO NAME	OUTPUT CURRENT (mA)		C_i (pF)	C_{pd} (pF)		t_{PZL} (ns)	t_{PZH} (ns)	Δt_{PZL} (ps/pF)	Δt_{PZH} (ps/pF)
N-CHANNEL (SINK CURRENT)	OPI21LJ	2	TYP	0.14	0.5	TYP MAX	3.95 7.51	– –	150 290	– –
	OPI41LJ	4	TYP	0.22	0.82	TYP MAX	2.26 4.17	– –	70 130	– –
	OPI81LJ	8	TYP	0.22	1.09	TYP MAX	1.77 3.35	– –	40 70	– –
N-CHANNEL with dI/dt CONTROL (SINK CURRENT)	OPK21LJ	2	TYP	0.14	0.53	TYP MAX	6.59 12.8	– –	160 290	– –
	OPK41LJ	4	TYP	0.23	0.76	TYP MAX	5.26 10.17	– –	90 160	– –
	OPK81LJ	8	TYP	0.23	1.04	TYP MAX	5.19 10.34	– –	60 110	– –
P-CHANNEL (SOURCE CURRENT)	OPI24LJ	2	TYP	0.14	0.62	TYP MAX	– –	4.1 8.26	– –	170 340
	OPI44LJ	4	TYP	0.24	1.16	TYP MAX	– –	2.25 4.29	– –	80 160
	OPI84LJ	8	TYP	0.24	1.74	TYP MAX	– –	1.61 3.01	– –	40 80
P-CHANNEL with dI/dt CONTROL (SOURCE CURRENT)	OPK24LJ	2	TYP	0.14	0.61	TYP MAX	– –	4.85 9.94	– –	170 340
	OPK44LJ	4	TYP	0.23	1.04	TYP MAX	– –	3.5 7.03	– –	80 160
	OPK84LJ	8	TYP	0.23	1.64	TYP MAX	– –	3.4 6.95	– –	50 90

† CMOS threshold measurements are shown.

FUNCTION					CHARACTERISTICS							
					ELECTRICAL			SWITCHING (CL = 0)				
									DELAY TIME		DELTA DELAY	
HARDWIRED	MACRO NAME	NUMBER OF INPUTS	OUTPUT DRIVE	CELLS USED		C_i (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
OR GATES	OR210LJ	2	1X	2	TYP	0.07	0.48	TYP MAX	0.39 0.78	0.71 1.47	0.88 1.7	0.55 1
	OR220LJ	2	2X	2	TYP	0.07	0.8	TYP MAX	0.46 0.83	0.82 1.72	0.44 0.86	0.36 0.7
	OR310LJ	3	1X	2	TYP	0.07	0.45	TYP MAX	0.43 0.84	1.04 2.44	0.88 1.73	0.64 1.21
	OR320LJ	3	2X	3	TYP	0.07	0.89	TYP MAX	0.52 0.93	1.2 2.88	0.44 0.87	0.42 0.83
	OR410LJ	4	1X	3	TYP	0.07	0.55	TYP MAX	0.46 0.85	1.34 3.43	0.89 1.75	0.72 1.39
	OR420LJ	4	2X	3	TYP	0.07	1.16	TYP MAX	0.51 0.91	1.53 3.98	0.45 0.89	0.49 0.97
	OR510LJ	5	1X	4	TYP	0.07	0.74	TYP MAX	0.46 0.97	0.97 2.49	0.89 1.73	0.79 1.6
	OR810LJ	8	1X	5	TYP	0.07	0.97	TYP MAX	0.5 0.98	1.43 3.83	0.89 1.76	0.9 1.92

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OSCILLATORS, REGISTERS

FUNCTION				CHARACTERISTICS								
				ELECTRICAL				SWITCHING† (C_L = 0 pF)				
									DELAY TIME		DELTA DELAY	
OSCILLATORS HARDWIRED	MACRO NAME	FREQUENCY RANGE (MHz)	PACKAGE PINS		C_I (pF)	C_{OUT} (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ps/pF)	Δt_{PHL} (ps/pF)
THIRD OVERTONE	OSI11LJ	55-tO-75	2	TYP	3.79	6.92	10.9	TYP MAX	2.52 4.2	2.33 4.04	160 350	160 340
THIRD OVERTONE	OSI12LJ	35-tO-55	2	TYP	3.79	6.89	10.3	TYP MAX	2.37 3.99	2.19 3.87	170 370	180 350
THIRD OVERTONE	OSI13LJ	20-tO-35	2	TYP	3.79	6.98	10.2	TYP MAX	2.29 3.89	2.13 3.78	180 370	180 350
FUNDAMENTAL	OSI14LJ	1-tO-20	2	TYP	3.79	6.9	10.1	TYP MAX	2.27 3.88	2.11 3.76	190 370	190 350

† CMOS output delay times are shown.

FUNCTION					CHARACTERISTICS								REQUIREMENTS	
					ELECTRICAL			SWITCHING (C_L = 0) (CLK to Q)					TIMING	
									DELAY TIME		DELTA DELAY		SETUP (MIN)	HOLD (MIN)
REGISTER/ FLIP-FLOPS HARDWIRED	MACRO NAME	f_{clock}	OUTPUT DRIVE	CELLS USED		C_I (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)	t_{su} (ns)	t_h (ns)
4-BIT,SER IN, CLR	R2401LJ	135 MHz	1X	26	TYP	MULTI	6.4	TYP MAX	1.38 2.77	1.59 3.21	0.89 1.73	0.51 0.95	2	0
4-BIT,SER IN, CLR, COMPLI-MENTARY OUTPUTS	R2402LJ	135 MHz	1X	27	TYP	MULTI	6.8	TYP MAX	1.49 3.07	1.66 3.43	0.89 1.74	0.55 1.01	2	0
4-BIT, PARALLEL IN	R2403LJ	135 MHz	1X	27	TYP	MULTI	6	TYP MAX	1.25 2.46	1.58 3.19	0.89 1.71	0.51 0.93	2	0
4-BIT, PARALLEL IN, COMPLI-MENTARY OUTPUT	R2404LJ	135 MHz	1X	31	TYP	MULTI	8	TYP MAX	1.26 2.48	1.58 3.22	0.89 1.72	0.51 0.94	2	0
4-BIT with CLR	R2405LJ	135 MHz	1X	26	TYP	MULTI	7.02	TYP MAX	1.42 2.85	1.63 3.33	0.89 1.72	0.51 0.95	2	0
4-BIT with CLR and COMPLI-MENTARY OUTPUTS	R2406LJ	135 MHz	1X	28	TYP	MULTI	8.17	TYP MAX	1.36 2.73	1.68 3.49	0.9 1.73	0.52 0.96	2	0

REGISTER FILES, SCAN FLIP–FLOPS/LATCHES

FUNCTION					CHARACTERISTICS								REQUIREMENTS	
					ELECTRICAL			ACCESS/CYCLE TIMES					TIMING	
3-PORT REGISTER FILES HARDWIRED (See Note 15)	MACRO NAME	ORGANI-ZATION (W X B)	OUTPUT DRIVE	CELLS USED		C_i (pF)	C_{pd} (pF)		WRITE CYCLE $t_c(W)$ (ns)	ADDRESS ACCESS $t_a(A)$ (ns)	ENABLE ACCESS t_{en} (ns)	DELTA DELAY Δt_a (ns/pF)	WRITE SETUP (MIN) t_{su} (ns)	WRITE HOLD (MIN) t_h (ns)
1 WRITE, 2 READ	RF400LJ	16 X 8	2X	418	TYP	0.19	48	TYP MAX	8	5.2 10.89	1.3 3.23	0.3 1.02	5	2
	RF402LJ	16 X 9	2X	462		0.19	53	TYP MAX	8	5.3 11.03	1.4 3.4	0.3 1.07	5	2

NOTE 15: RF400LJ and RF402LJ are for use on TGC112, TGC115, or TGC118 gate arrays only.

FUNCTION					CHARACTERISTICS								REQUIREMENTS	
					ELECTRICAL			SWITCHING (C_L = 0) (CLK to Q)					TIMING	
SCAN FLIP-FLOPS LATCHES HARDWIRED	MACRO NAME	OPERATING FRE-QUENCY f_{opr}	OUTPUT DRIVE	CELLS USED		C_i (pF)	C_{pd} (pF)		DELAY TIME t_{PLH} (ns)	DELAY TIME t_{PHL} (ns)	DELTA DELAY Δt_{PLH} (ns/pF)	DELTA DELAY Δt_{PHL} (ns/pF)	SETUP (MIN) t_{su} (ns)	HOLD (MIN) t_h (ns)
D-FF, with CLR	TDB10LJ	90MHz	1X	10	TYP	MULTI	4.6	TYP MAX	1.83 3.69	2.57 5.69	0.9 1.77	0.58 1.06	4 USE CK120LJ	0
M-S D-LATCH with CLR, COMP OUT	TDC11LJ	100MHz	1X	10	TYP	MULTI	3.99	TYP MAX	2.18 4.49	2.23 4.98	0.9 1.76	0.68 1.31	3 USE CK120LJ	0
M-S D-LATCH	TDN11LJ	100MHz	1X	8	TYP	MULTI	2.2	TYP MAX	1.67 3.69	1.95 4.3	0.89 1.76	0.51 0.94	3 USE CK120LJ	0
M-S D-LATCH with COMP OUT	TDN12LJ	100MHz	1X	9	TYP	MULTI	3.69	TYP MAX	1.89 4.23	2.17 4.84	0.91 1.77	0.54 0.95	3 USE CK120LJ	0
M-S D-LATCH with SLAVE D COMP OUT	TDN13LJ	100MHz	1X	12	TYP	MULTI	4	TYP MAX	1.99 4.41	2.31 5.07	0.91 1.77	0.54 0.98	3 USE CK120LJ	0
M-S D-LATCH	TDN22LJ	83MHz	2X	11	TYP	MULTI	5.8	TYP MAX	2.18 4.91	2.57 5.73	0.44 0.87	0.32 0.62	3 USE CK120LJ	0

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SHIFT REGISTERS, TOGGLE FLIP–FLOPS, TIE–OFF

FUNCTION					CHARACTERISTICS							
					ELECTRICAL			SWITCHING (See Note 16)				
									DELAY TIME		DELTA DELAY	
SHIFT REGISTERS SOFTWARE	MACRO NAME	LENGTH	OUTPUT DRIVE	CELLS USED		C_I (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
SIPO with CLR	S164LJ	8–BITS	2X	88	TYP	0.07	30.36	TYP MAX	2.5 4.7	2.5 4.7	0.44 0.84	0.32 0.44
PISO with CLKINH	S165ALJ	8–BITS	1X	126	TYP	MULTI	23.2	TYP MAX	3 6.4	2.4 4.9	0.46 0.92	0.34 0.65
PIPO BIDIRECTIONAL with CLR	S194ALJ	4–BITS	1X	73	TYP	NULTI	15.23	TYP MAX	1.8 3.7	1.9 3.8	0.89 1.72	0.51 0.95

NOTE 16: Specific timing data regarding pulse duration, setup time and hold time models are incorporated in most engineering workstation libraries. These models are for the clocked functions embedded in the software macros. Evaluations of timing requirements made during prelayout simulation, produce workstation output used to identify and resolve each specific timing need.

FUNCTION				CHARACTERISTICS							
				ELECTRICAL			SWITCHING (CLK TO Q OUT)				
								DELAY TIME		DELTA DELAY	
TOGGLE FLIP-FLOPS (f_{clock}) HARDWIRED	MACRO NAME	OUTPUT DRIVE	CELLS USED		C_I (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
131 MHz with CLR and PREZ	TAB20LJ	2X	9	TYP	0.2	3	TYP MAX	1.2 2.48	1.08 2.3	0.48 0.98	0.44 0.84

FUNCTION				CHARACTERISTICS							
				ELECTRICAL			SWITCHING				
								DELAY TIME		DELTA DELAY	
TIEOFF for UNUSED INPUTS HARDWIRED	MACRO NAME	OUTPUT DRIVE	CELLS USED		C_I (pF)	C_{pd} (pF)		t_{PLH} (ns)	t_{PHL} (ns)	Δt_{PLH} (ns/pF)	Δt_{PHL} (ns/pF)
HI/LO with ESD PROTECTION	TO010LJ	1X	2	TYP	NONE	NIL	TYP MAX	--	--	--	--

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