INTEGRATED CIRCUITS

NEW PRODUCT BULLETIN

This announcement provides preliminary engineering information on new Texas Instruments products. Definitive specifications are now being prepared for publication.

SOLID CIRCUIT®
SEMICONDUCTOR NETWORKS†

TYPE SN5474
DUAL D-TYPE EDGE TRIGGERED FLIP-FLOP

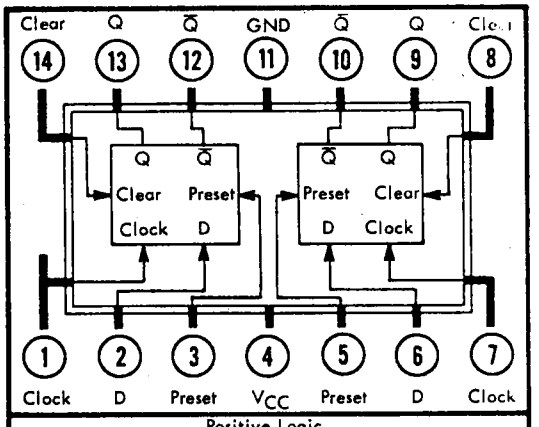
A HIGH-SPEED FLIP-FLOP
FOR GENERAL-PURPOSE DIGITAL APPLICATIONS

logic

TRUTH TABLE (Each F-F)

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\overline{Q}$
0	0	1
1	1	0

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.



Positive Logic
a. Low input to clear sets Q to logical 1.
b. Low input to preset sets $\overline{Q}$ to logical 1.
c. Clear or preset inputs dominate regardless of the state of clock and D inputs.

description

The SN5474 is a monolithic, dual, D-type, edge-triggered flip-flop featuring direct clear and preset inputs and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the Q output on the positive edge of the clock pulse.

Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed the data input (D) is locked out.

The SN5474 dual flip-flop has the same clocking characteristics as the SN5470 gated (edge-triggered) flip-flop and both are ideally suited for medium to high speed applications requiring toggle frequencies up to 25 MHz. The SN5474 can be used at a significant saving in system power dissipation and package count in applications where input gating is not required.

mechanical data

Mechanical data for the SN5474 is identical to that shown on the data sheet for Series 54 SOLID CIRCUIT® semiconductor networks.

absolute maximum ratings over free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 3) . . . . . 7 V
Input Voltage V_{in} (See Notes 3 and 4) . . . . . 5.5 V
Operating Free-Air Temperature Range . . . . . -55°C to 125°C
Storage Temperature Range . . . . . -65°C to 150°C

NOTES: 3. Voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

† Patented by Texas Instruments

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TYPE SN5474
DUAL D-TYPE EDGE TRIGGERED FLIP-FLOP

recommended operating conditions

Supply Voltage, V_{CC}	4.5 V to 5.5 V
Maximum Fan-Out From Each Output, N	10
Minimum Width of Clock Pulse t_p (clock)	20 ns
Toggle Frequency, f_{toggle}	0 to 25 MHz
Minimum Set-Up Time, t_{set-up}	20 ns
Minimum Hold Time, t_{hold}	10 ns
Minimum Preset Time, t_{preset}	25 ns
Minimum Clear Time, t_{clear}	25 ns

electrical characteristics, V_{CC} = 4.5 V to 5.5 V, T_A = −55°C to 125°C

PARAMETER		MIN	TYP	MAX	UNIT
V_{in} (1)	Logical 1 input voltage	2			V
V_{in} (0)	Logical 0 input voltage			0.8	V
V_{out} (1)	Logical 1 output voltage	2.4			V
V_{out} (0)	Logical 0 output voltage			0.4	V
$I_{in(0)}$	Logical 0 level input current at clear or D input			1.6	mA
$I_{in(0)}$	Logical 0 level input current preset or clock input			3.2	mA
I_{in} (1)	Logical 1 level input current at D input			40	μA
I_{in} (1)	Logical 1 level input current at clear or clock input			80	μA
I_{in} (1)	Logical 1 level input current at preset input			120	μA
I_{OS}	Short-circuit output current at either output‡	20		55	mA
I_{CC}	Supply current each flip-flop (D and clock inputs at GND)		8.5		mA

‡ Not more than one output should be shorted at a time

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		MIN	TYP	MAX	UNIT
t_{pd} (1)	Propagation delay time to logical 1		20	35	ns
t_{pd} (0)	Propagation delay time to logical 0		28	50	ns

schematic (each flip-flop)