

54/74 Family SSI Circuits

6

recommended operating conditions

	54 FAMILY	SERIES 54			SERIES 54H			SERIES 54L			SERIES 54LS			SERIES 54S			UNIT
	74 FAMILY	SERIES 74			SERIES 74H			SERIES 74L			SERIES 74LS			SERIES 74S			
		'00, '04, '10, '20, '30			'H00, 'H04, 'H10, 'H20, 'H30			'L00, 'L04, 'L10, 'L20, 'L30			'LS00, 'LS04, 'LS10, 'LS20, 'LS30			'S00, 'S04, 'S10, 'S20, 'S30, 'S133			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I _{OH}	54 Family	-400			-500			-100			-400			-1000			μA
	74 Family	-400			-500			-200			-400			-1000			
Low-level output current, I _{OL}	54 Family	16			20			2			4			20			mA
	74 Family	16			20			3.6			8			20			
Operating free-air temperature, T _A	54 Family	-55	125	-55	125	-55	125	-55	125	-55	125	-55	125	-55	125	125	°C
	74 Family	0	70	0	70	0	70	0	70	0	70	0	70	0	70	70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54	SERIES 54H	SERIES 54L	SERIES 54LS	SERIES 54S	UNIT						
			SERIES 74	SERIES 74H	SERIES 74L	SERIES 74LS	SERIES 74S							
			'00, '04, '10, '20, '30	'H00, 'H04, 'H10, 'H20, 'H30	'L00, 'L04, 'L10, 'L20, 'L30	'LS00, 'LS04, 'LS10, 'LS20, 'LS30	'S00, 'S04, 'S10, 'S20, 'S30, 'S133							
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage	1, 2		2		2		2		V					
V _{IL} Low-level input voltage	1, 2		0.8		0.8		0.7		V					
		54 Family	0.8		0.8		0.7							
		74 Family	0.8		0.8		0.7							
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = §	-1.5		-1.5		-1.5		V					
V _{OH} High-level output voltage	1	V _{CC} = MIN, V _{IL} = V _{IL} max, I _{OH} = MAX	54 Family	2.4	3.4	2.4	3.5	2.4	3.3	2.5	3.4	2.5	3.4	V
			74 Family	2.4	3.4	2.4	3.5	2.4	3.2	2.7	3.4	2.7	3.4	
V _{OL} Low-level output voltage	2	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = MAX	54 Family	0.2	0.4	0.2	0.4	0.15	0.3	0.25	0.4	0.25	0.4	V
			74 Family	0.2	0.4	0.2	0.4	0.2	0.4	0.25	0.5	0.25	0.5	
			Series 74LS							0.4				
I _I Input current at maximum input voltage	4	V _{CC} = MAX	V _I = 5.5 V		1		1		0.1		1		mA	
			V _I = 7 V						0.1					
I _{IH} High-level input current	4	V _{CC} = MAX	V _{IH} = 2.4 V		40		50		10		20		μA	
			V _{IH} = 2.7 V								50			
I _{IL} Low-level input current	5	V _{CC} = MAX	V _{IL} = 0.3 V						-0.18				mA	
			V _{IL} = 0.4 V		-1.6		-2				-0.4			
			V _{IL} = 0.5 V								-2			
I _{OS} Short-circuit output current*	6	V _{CC} = MAX	54 Family	-20	-55	-40	-100	-3	-15	-20	-100	-40	-100	mA
			74 Family	-18	-55	-40	-100	-3	-15	-20	-100	-40	-100	
I _{CC} Supply current	7	V _{CC} = MAX	See table on next page										mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ I_I = -12 mA for SN54/SN74*, -8 mA for SN54H/SN74H*, and -18 mA for SN54LS/SN74LS* and SN54S/SN74S*.

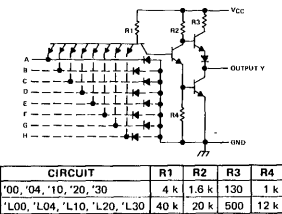
* Not more than one output should be shorted at a time, and for SN54H/SN74H*, SN54LS/SN74LS*, and SN54S/SN74S*, duration of short-circuit should not exceed 1 second.

supply current[†]

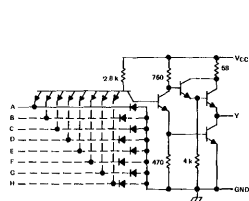
TYPE	I _{CCH} (mA) Total with outputs high		I _{CCL} (mA) Total with outputs low		I _{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'00	4	8	12	22	2
'04	6	12	18	33	2
'10	3	6	9	16.5	2
'20	2	4	6	11	2
'30	1	2	3	6	2
'H00	10	16.8	26	40	4.5
'H04	16	26	40	58	4.5
'H10	7.5	12.6	19.5	30	4.5
'H20	5	8.4	13	20	4.5
'H30	2.5	4.2	6.5	10	4.5
'L00	0.44	0.8	1.16	2.04	0.20
'L04	0.66	1.2	1.74	3.06	0.20
'L10	0.33	0.6	0.87	1.53	0.20
'L20	0.22	0.4	0.58	1.02	0.20
SN54L30	0.11	0.33	0.29	0.51	0.20
SN74L30	0.11	0.2	0.29	0.51	0.20
'LS00	0.8	1.6	2.4	4.4	0.4
'LS04	1.2	2.4	3.6	6.6	0.4
'LS10	0.6	1.2	1.8	3.3	0.4
'LS20	0.4	0.8	1.2	2.2	0.4
'LS30	0.35	0.5	0.6	1.1	0.48
'S00	10	16	20	36	3.75
'S04	15	24	30	54	3.75
'S10	7.5	12	15	27	3.75
'S20	5	8	10	18	3.75
'S30	3	5	5.5	10	4.25
'S133	3	5	5.5	10	4.25

[†]Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

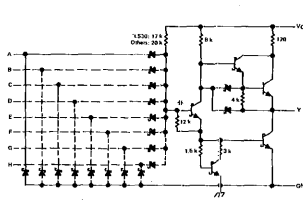
schematics (each gate)



'00, '04, '10, '20, '30
'L00, 'L04, 'L10, 'L20, 'L30, CIRCUITS
Input clamp diodes not on
SN54L/SN74L' circuits.

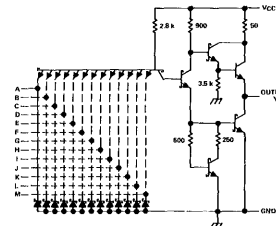


'H00, 'H04, 'H10, 'H20, 'H30 CIRCUITS



'LS00, 'LS04, 'LS10, 'LS20,
'LS30 CIRCUITS
*The 12-kΩ resistor is not on 'LS30.

Resistor values shown are nominal and in ohms.



'S00, 'S04, 'S10, 'S20,
'S30, 'S133 CIRCUITS

switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS#	t _{PLH} (ns) Propagation delay time, low-to-high-level output			t _{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'00, '10	C _L = 15 pF, R _L = 400 Ω	11	22		7	15	
'04, '20		12	22		8	15	
'30		13	22		8	15	
'H00	C _L = 25 pF, R _L = 280 Ω	5.9	10		6.2	10	
'H04		6	10		6.5	10	
'H10		5.9	10		6.3	10	
'H20	C _L = 50 pF, R _L = 4 kΩ	6	10		7	10	
'H30		6.8	10		8.9	12	
'L00, 'L04, 'L10, 'L20		35	60		31	60	
'L30	C _L = 15 pF, R _L = 2 kΩ	35	60		70	100	
'LS00, 'LS04 'LS10, 'LS20		9	15		10	15	
'LS30		8	15		13	20	
'S00, 'S04	C _L = 15 pF, R _L = 280 Ω	3	4.5		3	5	
'S10, 'S20		4.5			5		
'S30, 'S133	C _L = 15 pF, R _L = 280 Ω	4	6		4.5	7	
	C _L = 50 pF, R _L = 280 Ω	5.5			6.5		

#Load circuits and voltage waveforms are shown on pages 3-10 and 3-11.

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74			SERIES 54H SERIES 74H			SERIES 54L SERIES 74L			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT
		'01, '03, '05, '12, '22			'H01, 'H05, 'H22			'L01, 'L03			'LS01, 'LS03, 'LS05, 'LS12, 'LS22			'S03, 'S05, 'S22			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	54 Family 74 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
High-level output voltage, V _{OH}		5.5			5.5			5.5			5.5			5.5			V
Low-level output current, I _{OL}	54 Family 74 Family	16			20			2			4			20			mA
Operating free-air temperature, T _A	54 Family 74 Family	-55	125	70	-55	125	70	-55	125	70	-55	125	70	-55	125	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS [†]	SERIES 54 SERIES 74			SERIES 54H SERIES 74H			SERIES 54L SERIES 74L			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT
			'01, '03, '05, '12, '22			'H01, 'H05, 'H22			'L01, 'L03			'LS01, 'LS03, 'LS05, 'LS12, 'LS22			'S03, 'S05, 'S22			
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IH} High-level input voltage	1, 2		2			2			2			2			2			V
V _{IL} Low-level input voltage	1, 2		54 Family 74 Family			0.8 0.8			0.6 0.6			0.7 0.8			0.8 0.8			V
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = §	-1.5			-1.5						-1.5			-1.2			V
I _{OH} High-level output current	1	V _{CC} = MIN, V _{IL} = V _{IL} max, V _{OH} = 5.5 V	250			250			50			100			250			µA
V _{OL} Low-level output voltage	2	V _{CC} = MIN, V _{IH} = 2 V	54 Family 74 Family Series 74LS			0.2 0.4 0.2 0.4			0.15 0.3 0.2 0.4			0.25 0.4 0.35 0.5			0.5 0.5			V
I _I Input current at maximum input voltage	4	V _{CC} = MAX	V _I = 5.5 V V _I = 7 V			1 1			0.1			0.1			1			mA
I _{IH} High-level input current	4	V _{CC} = MAX	V _{IH} = 2.4 V V _{IH} = 2.7 V			40 50			10			20			50			µA
I _{IL} Low-level input current	5	V _{CC} = MAX	V _{IL} = 0.3 V V _{IL} = 0.4 V V _{IL} = 0.5 V			-1.6 -2			-0.18			-0.4			-2			mA
I _{CC} Supply current	7	V _{CC} = MAX	See table on next page															mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[§] I_I = -12 mA for SN54/SN74', -8 mA for SN54H/SN74H', and -18 mA for SN54LS/SN74LS' and SN54S/SN74S'.

supply current[¶]

TYPE	I _{CCH} (mA) Total with outputs high		I _{CCL} (mA) Total with outputs low		I _{CC} (mA) Average per Gate (50% duty cycle)
	TYP	MAX	TYP	MAX	
'01	4	8	12	22	2
'03	4	8	12	22	2
'05	6	12	18	33	2
'12	3	6	9	16.5	2
'22	2	4	6	11	2
'H01	6.8	10	26	40	4.1
'H05	16	26	40	58	4.67
'H22	3.4	5	13	20	4.1
'L01	0.44	0.8	1.16	2.04	0.20
'L03	0.44	0.8	1.16	2.04	0.20
'LS01	0.8	1.6	2.4	4.4	0.4
'LS03	0.8	1.6	2.4	4.4	0.4
'LS05	1.2	2.4	3.6	6.6	0.4
'LS12	0.7	1.4	1.8	3.3	0.42
'LS22	0.4	0.8	1.2	2.2	0.4
'S03	6	13.2	20	36	3.25
'S05	9	19.8	30	54	3.25
'S22	3	6.6	10	18	3.25

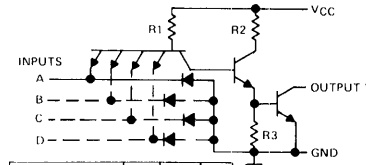
[¶] Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS [#]	t _{PLH} (ns) Propagation delay time, low-to-high-level output			t _{PHL} (ns) Propagation delay time, high-to-low-level output			
		MIN	TYP	MAX	MIN	TYP	MAX	
'01, '03	C _L = 15 pF, R _L = 4 kΩ for t _{PLH} , 400 Ω for t _{PHL}		35	45		8	15	
'05			40	55		8	15	
'12, '22			35	45		8	15	
'H01, 'H05, 'H22	C _L = 25 pF, R _L = 280 Ω		10	15		7.5	12	
'L01, 'L03	C _L = 50 pF, R _L = 4 kΩ		60	90		33	60	
'LS01, 'LS03, 'LS05, 'LS12, 'LS22	C _L = 15 pF, R _L = 2 kΩ		17	32		15	28	
'S03, 'S05, 'S22	C _L = 15 pF, R _L = 280 Ω		2	5	7.5	2	4.5	7
	C _L = 50 pF, R _L = 280 Ω			7.5			7	

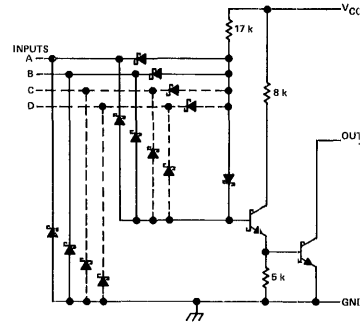
[#] Load circuits and voltage waveforms are shown on pages 3-10 and 3-11.

schematics (each gate)

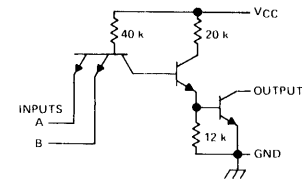


CIRCUITS	R1	R2	R3
'01, '03, '05, '12, '22	4 k	1.6 k	1 k
'H01, 'H05, 'H22	2.8 k	760	470

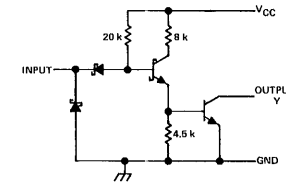
'01, '03, '05, '12, '22, 'H01, 'H05, 'H22 CIRCUITS



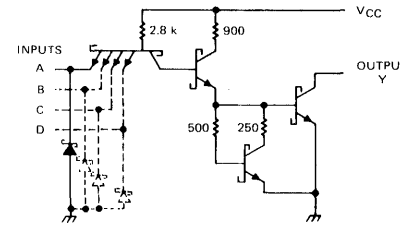
'LS01, 'LS03, 'LS12, 'LS22 CIRCUITS



'L01, 'L03 CIRCUITS



'LS05 CIRCUITS



'S03, 'S05, 'S22 CIRCUITS

Resistor values shown are nominal and in ohms.

POSITIVE-NAND GATES AND INVERTERS
WITH OPEN-COLLECTOR OUTPUTS

OPEN-COLLECTOR OUTPUT APPLICATION DATA

APPLICATION DATA

combined fan-out and wire-AND capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), may be paralleled with other similar TTL gates to perform the wire-AND function, and simultaneously, will drive from one to nine standard loads of its own series. When no other open-collector gates are paralleled, this gate may be used to drive ten loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and off current (through paralleled outputs) will be available while the output is high. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the low level even if only one of the paralleled outputs is sinking all the currents.

In both conditions (low and high level) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where V_{RL} is the voltage drop in volts, and I_{RL} is the current in amperes.

high-level (off-state) circuit calculations (see figure A)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the V_{OH} level required at the load:

$$V_{RL} = V_{CC} - V_{OH \text{ min}}$$

The total current through the load resistor (I_{RL}) is the sum of the load currents (I_{IH}) and off-state reverse currents (I_{OH}) through each of the wire-AND-connected outputs:

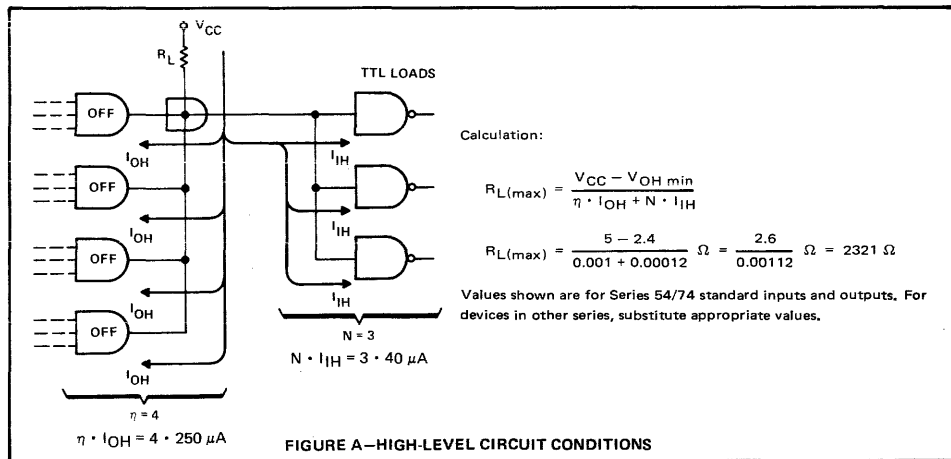
$$I_{RL} = \eta \cdot I_{OH} + N \cdot I_{IH} \text{ to TTL loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(\text{max})} = \frac{V_{CC} - V_{OH \text{ min}}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

where η = number of gates wire-AND-connected, and N = number of standard loads.

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OPEN-COLLECTOR OUTPUT APPLICATION DATA

APPLICATION DATA

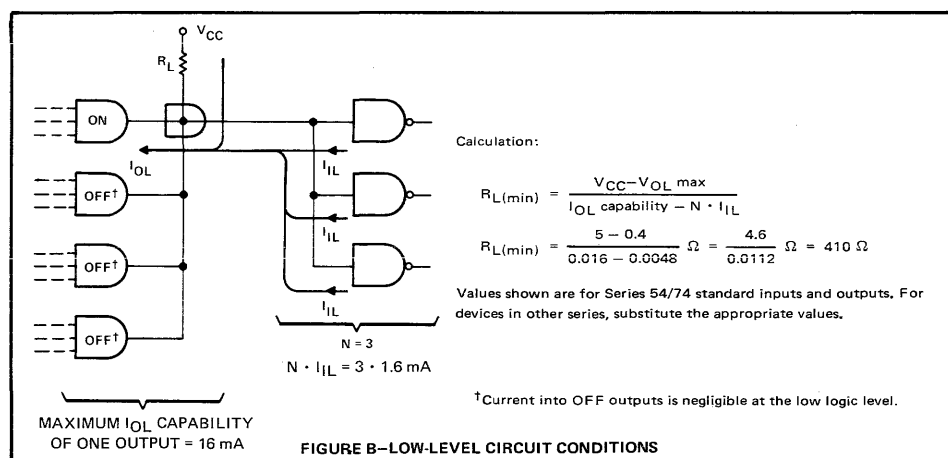
low-level (on-state) circuit calculations (see figure B)

The current through the resistor must be limited to the maximum sink current of one output transistor. Note that if several output transistors are wire-AND connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during low-level periods, the current must be limited to the recommended maximum I_{OL} , the maximum current which will ensure that the low-level output voltage, V_{OL} , will be below V_{OL} max.

Also, fan-out must be considered. Part of I_{OL} will be supplied from the inputs which are being driven. This reduces the amount of current which can be allowed through R_L .

Therefore, the equation used to determine the minimum value of R_L would be:

$$R_{L(\min)} = \frac{V_{CC} - V_{OL \max}}{I_{OL \text{ capability}} - N \cdot I_{IL}}$$



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recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74			SERIES 54L SERIES 74L			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT			
		'02			'25, '27			'L02			'LS02, 'LS27				'S02, 'S260		
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX		MIN	NOM	MAX
Supply voltage, V _{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I _{OH}	54 Family	-400			-800			-100			-400			-1000			μA
	74 Family	-400			-800			-200			-400			-1000			
Low-level output current, I _{OL}	54 Family	16			16			2			4			20			mA
	74 Family	16			16			3.6			8			20			
Operating free-air temperature, T _A	54 Family	-55 125			-55 125			-55 125			-55 125			-55 125			°C
	74 Family	0 70			0 70			0 70			0 70			0 70			

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54 SERIES 74		SERIES 54L SERIES 74L		SERIES 54LS SERIES 74LS		SERIES 54S SERIES 74S		UNIT	
			'02, '25, '27		'L02		'LS02, 'LS27		'S02, 'S260			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡		MAX
V _{IH} High-level input voltage	1, 2		2		2		2		2		V	
V _{IL} Low-level input voltage	1, 2	54 Family	0.8		0.7		0.7		0.8		V	
		74 Family	0.8		0.7		0.8		0.8			
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = §	-1.5				-1.5		-1.2		V	
V _{OH} High-level output voltage	1	V _{CC} = MIN, V _{IL} = V _{IL} max, I _{OH} = MAX	54 Family	2.4	3.4	2.4	3.3	2.5	3.4	2.5	3.4	V
		74 Family	2.4	3.4	2.4	3.2	2.7	3.4	2.7	3.4		
V _{OL} Low-level output voltage	2	V _{CC} = MIN, I _{OL} = MAX	54 Family	0.2	0.4	0.15	0.3	0.25	0.4		0.5	V
		74 Family	0.2	0.4	0.2	0.4	0.35	0.5		0.5		
		Series 74LS					0.25	0.4				
I _I Input current at maximum input voltage	4	V _{CC} = MAX	V _I = 5.5 V		1		0.1				mA	
			V _I = 7 V				0.1					
I _{IH} High-level input current	4	V _{CC} = MAX	V _{IH} = 2.4 V		40		10				μA	
			Strobe of '25		160							
			All inputs		V _{IH} = 2.7 V				20		50	
I _{IL} Low-level input current	5	V _{CC} = MAX	V _{IL} = 0.3 V		-0.18		-0.4				mA	
			Data inputs		V _{IL} = 0.4 V		-1.6					
			Strobe of '25		V _{IL} = 0.5 V		-6.4					
			All inputs						-2			
I _{OS} Short-circuit output current*	6	V _{CC} = MAX	54 Family	-20	-55	-3	-15	-20	-100	-40	-100	mA
			74 Family	-18	-55	-3	-15	-20	-100	-40	-100	
I _{CC} Supply current	7	V _{CC} = MAX	See table on next page									mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ I_I = -12 mA for SN54'/SN74' and -18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.

* Not more than one output should be shorted at a time, and for SN54LS'/SN74LS' and SN54S'/SN74S', duration of output short-circuit should not exceed one second.

supply current¹

TYPE	I _{CC} H (mA) Total with outputs high		I _{CC} L (mA) Total with outputs low		I _{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'02	8	16	14	27	2.75
'25	8	16	10	19	2.25
'27	10	16	16	26	4.34
'L02	0.8	1.6	1.4	2.6	0.275
'LS02	1.6	3.2	2.8	5.4	0.55
'LS27	2.0	4	3.4	6.8	0.9
'S02	17	29	26	45	5.38
'S260	17	29	26	45	10.75

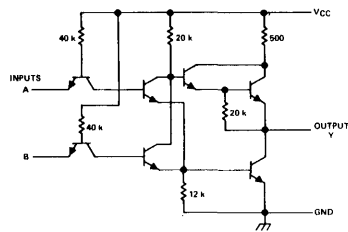
¹Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

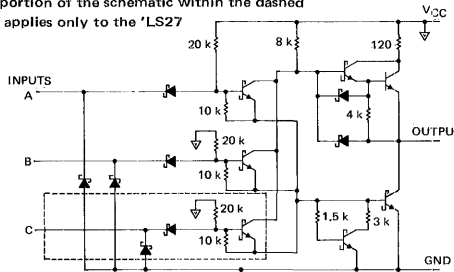
TYPE	TEST CONDITIONS#	t _{PLH} (ns) Propagation delay time, low-to-high-level output			t _{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
		'02	C _L = 15 pF, R _L = 400 Ω	12	15	8	15
'25	13	22		8	15		
'27	10	15		7	11		
'L02	C _L = 50 pF, R _L = 4 kΩ	31	60	35	60		
'LS02, 'LS27	C _L = 15 pF, R _L = 2 kΩ	10	15	10	15		
'S02	C _L = 15 pF, R _L = 280 Ω	3.5	5.5	3.5	5.5		
	C _L = 50 pF, R _L = 280 Ω	5		5			
'S260	C _L = 15 pF, R _L = 280 Ω	4	5.5	4	6		

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

The portion of the schematic within the dashed lines applies only to the 'LS27

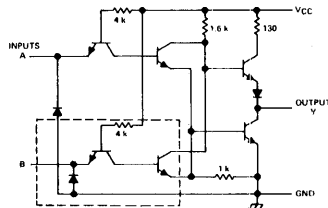


'L02 CIRCUITS



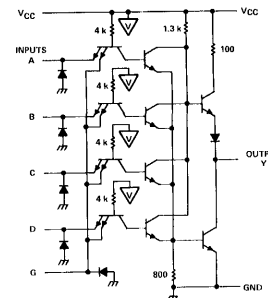
'LS02, 'LS27 CIRCUITS

schematics (each gate)



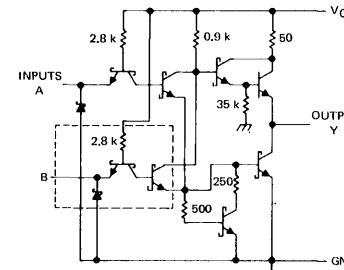
The portion of the schematic within the dashed lines is repeated for the C input of the '27.

'02, '27 CIRCUITS



'25 CIRCUITS

Resistor values are nominal and in ohms.



The portion of the schematic within the dashed lines is repeated for each additional input of the 'S260, and the 0.9-kΩ resistor is changed to 0.6 kΩ.

'S02, 'S260 CIRCUITS

POSITIVE-NOR GATES WITH TOTEM-POLE OUTPUTS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74			SERIES 54H SERIES 74H			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT
		'08,			'H11, 'H21			'LS08, 'LS11, 'LS21			'S08, 'S11			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}	54 Family 74 Family	4.5 4.75	5 5	5.5 5.25	4.5 4.75	5 5	5.5 5.25	4.5 4.75	5 5	5.5 5.25	4.5 4.75	5 5	5.5 5.25	V
High-level output current, I_{OH}				-800			-500			-400			-1000	μ A
Low-level output current, I_{OL}	54 Family 74 Family			16			20			4			20	mA
Operating free-air temperature, T_A	54 Family 74 Family	-55 0		125 70	-55 0		125 70	-55 0		125 70	-55 0		125 70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS [†]	SERIES 54 SERIES 74		SERIES 54H SERIES 74H		SERIES 54LS SERIES 74LS		SERIES 54S SERIES 74S		UNIT
			'08,		'H11, 'H21		'LS08, 'LS11, 'LS21		'S08, 'S11		
			MIN	TYP [‡] MAX	MIN	TYP [‡] MAX	MIN	TYP [‡] MAX	MIN	TYP [‡] MAX	
V_{IH} High-level input voltage	1, 2		2		2		2		2		V
V_{IL} Low-level input voltage	1, 2		54 Family 74 Family		0.8 0.8		0.7 0.8		0.8 0.8		V
V_{IK} Input clamp voltage	3	$V_{CC} = \text{MIN}, I_I = \frac{1}{2}$			-1.5		-1.5		-1.2		V
V_{OH} High-level output voltage	1	$V_{CC} = \text{MIN}, I_{OH} = \text{MAX}, V_{IH} = 2 \text{ V}$	54 Family 74 Family		2.4 3.4 2.4 3.4		2.5 3.4 2.7 3.4		2.5 3.4 2.7 3.4		V
V_{OL} Low-level output voltage	2	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}$	54 Family 74 Family		0.2 0.4 0.2 0.4		0.15 0.3 0.2 0.4		0.25 0.4 0.35 0.5		V
I_I Input current at maximum input voltage	4	$V_{CC} = \text{MAX}$	54 Family 74 Family		1 0.1		0.1 0.1		1 0.1		mA
I_{IH} High-level input current	4	$V_{CC} = \text{MAX}$	54 Family 74 Family		40 50		20 50		50 50		μ A
I_{IL} Low-level input current	5	$V_{CC} = \text{MAX}$	54 Family 74 Family		-1.6 -2		-0.4 -0.4		-2 -2		mA
I_{OS} Short circuit output current*	6	$V_{CC} = \text{MAX}$	54 Family 74 Family		-20 -55 -40 -100		-20 -100 -20 -100		-40 -100 -40 -100		mA
I_{CC} Supply current	7	$V_{CC} = \text{MAX}$					See table on next page				mA

[†]For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 25^{\circ}$ C.

[§] $I_I = -12$ mA for SN54/SN74, -8 mA for SN54H/SN74H, and -18 mA for SN54LS/SN74LS and SN54S/SN74S.

*Not more than one output should be shorted at a time, and for SN54H/SN74H, SN54LS/SN74LS and SN54S/SN74S, duration of output short circuit should not exceed one second.

supply current†

TYPE	I _{CCH} (mA) Total with outputs high		I _{CCL} (mA) Total with outputs low		I _{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'08	11	21	20	33	3.88
'H11	18	30	30	48	8
'H21	12	20	20	32	8
'LS08	2.4	4.8	4.4	8.8	0.85
'LS11	1.8	3.6	3.3	6.6	0.85
'LS21	1.2	2.4	2.2	4.4	0.85
'S08	18	32	32	57	6.25
'S11	13.5	24	24	42	6.25

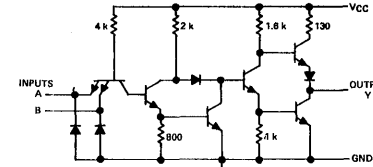
†Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

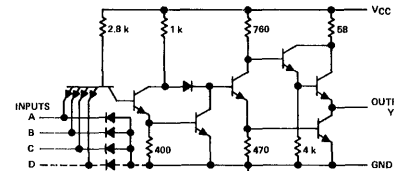
TYPE	TEST CONDITIONS#	t _{PLH} (ns) Propagation delay time, low-to-high-level output			t _{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'08	C _L = 15 pF, R _L = 400 Ω		17.5	27	12		19
'H11, 'H21	C _L = 25 pF, R _L = 280 Ω		7.6	12	8.8		12
'LS08, 'LS11 'LS21	C _L = 15 pF, R _L = 2 kΩ		8	15	10		20
'S08, 'S11	C _L = 15 pF, R _L = 280 Ω		4.5	7	5		7.5
	C _L = 50 pF, R _L = 280 Ω		6		7.5		

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

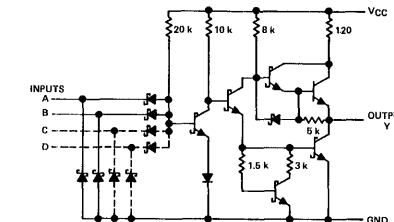
schematics (each gate)



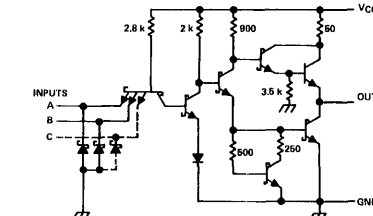
'08 CIRCUITS



'H11, 'H21 CIRCUITS



'LS08, 'LS11, 'LS21 CIRCUITS



'S08, 'S11 CIRCUITS

Resistor values shown are nominal and in ohms.

recommended operating conditions

	54 FAMILY	SERIES 54			SERIES 54H			SERIES 54LS			SERIES 54S			UNIT
	74 FAMILY	SERIES 74			SERIES 74H			SERIES 74LS			SERIES 74S			
		'09			'H15			'LS09, 'LS15			'S09, 'S15			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V _{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V _{OH}				5.5			5.5			5.5			5.5	V
Low-level output current, I _{OL}	54 Family			16			20			4			20	mA
	74 Family			16			20			8			20	
Operating free-air temperature, T _A	54 Family	-55		125	-55		125	-55		125	-55		125	°C
	74 Family	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54	SERIES 54H	SERIES 54LS	SERIES 54S	UNIT						
			SERIES 74	SERIES 74H	SERIES 74LS	SERIES 74S							
			'09	'H15	'LS09, 'LS15	'S09, 'S15							
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IH} High-level input voltage	1, 2		2		2		2		2			V	
V _{IL} Low-level input voltage	1, 2		54 Family	0.8	0.8		0.7		0.8			V	
			74 Family	0.8	0.8		0.8		0.8				
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = §		-1.5	-1.5		-1.5		-1.2			V	
I _{OH} High-level output current	1	V _{CC} = MIN, V _{IH} = 2 V, V _{OH} = 5.5 V,		250	250		100		250			μA	
V _{OL} Low-level output voltage	2	V _{CC} = MIN, V _{IH} = 2 V	I _{OL} = MAX	54 Family	0.2	0.4	0.15	0.3	0.25	0.4	0.5		V
			I _{OL} = 4 mA	74 Family	0.2	0.4	0.2	0.4	0.35	0.5	0.5		
				Series 74LS					0.25	0.4			
I _I Input current at maximum input voltage	4	V _{CC} = MAX	V _I = 5.5 V		1		0.1				1	mA	
			V _I = 7 V				0.1						
I _{IH} High-level input current	4	V _{CC} = MAX	V _{IH} = 2.4 V		40		50					μA	
			V _{IH} = 2.7 V					20		50			
I _{IL} Low-level input current	5	V _{CC} = MAX	V _{IL} = 0.4 V		-1.6		-2		-0.4			mA	
			V _{IL} = 0.5 V							-2			
I _{CC} Supply current	7	V _{CC} = MAX	See table on next page									mA	

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
 ‡ All typical values are at V_{CC} = 5 V, T_A = 25° C.
 § I_I = -12 mA for SN54/SN74, -8 mA for SN54H/SN74H, and -18 mA for SN54LS/SN74LS.

supply current[†]

TYPE	I _{CCH} (mA)		I _{CCL} (mA)		I _{CC} (mA)
	Total with outputs high		Total with outputs low		Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'09	11	21	20	33	3.88
'H15	15	25	30	48	7.5
'LS09	2.4	4.8	4.4	8.8	0.85
'LS15	1.8	3.6	3.3	6.6	0.85
'S09	18	32	32	57	6.25
'S15	10.5	19.5	24	42	5.75

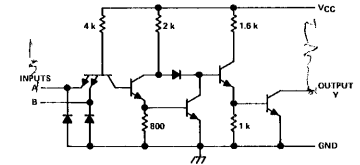
[†]Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

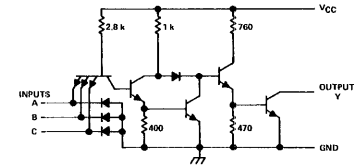
TYPE	TEST CONDITIONS [#]	t _{PLH} (ns)			t _{PHL} (ns)		
		Propagation delay time, low-to-high-level output			Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'09	C _L = 15 pF, R _L = 400 Ω		21	32		16	24
'H15	C _L = 25 pF, R _L = 280 Ω		12	18		9	13
'LS09, 'LS15	C _L = 15 pF, R _L = 2 kΩ		20	35		17	35
'S09	C _L = 15 pF, R _L = 280 Ω		6.5	10		6.5	10
	C _L = 50 pF, R _L = 280 Ω		9			9	
'S15	C _L = 15 pF, R _L = 280 Ω		5.5	8.5		6	9
	C _L = 50 pF, R _L = 280 Ω		8.5			8	

[#]Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

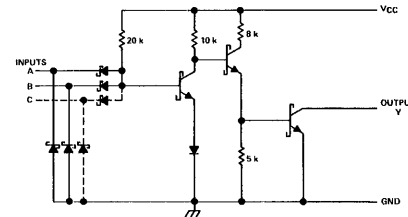
schematics (each gate)



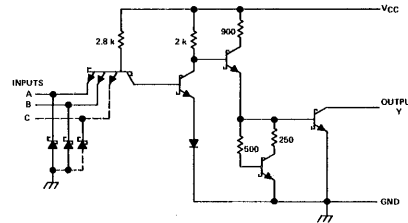
'09 CIRCUITS



'H15 CIRCUITS



'LS09, 'LS15 CIRCUITS



'S09, 'S15 CIRCUITS

Resistor values shown are nominal and in ohms.

POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS



recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74						SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT
		'13			'14, '132			'LS13, 'LS14, 'LS132			'S132			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
High level output current, I _{OH}		-800						-400			-1000			μA
Low-level output current, I _{OL}	54 Family	16						4			20			mA
	74 Family	16						8			20			
Operating free-air temperature, T _A	54 Family	-55						-55			-55			°C
	74 Family	0						0			0			

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54 SERIES 74						SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT
			'13			'14, '132			'LS13, 'LS14, 'LS132			'S132			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{T+} Positive-going threshold voltage	8	V _{CC} = 5 V	1.5	1.7	2	1.5	1.7	2	1.4	1.6	1.9	1.6	1.77	1.9	V
V _{T-} Negative-going threshold voltage	9	V _{CC} = 5 V	0.6	0.9	1.1	0.6	0.9	1.1	0.5	0.8	1	1.1	1.22	1.4	V
Hysteresis (V _{T+} -V _{T-})	8, 9	V _{CC} = 5 V	0.4	0.8		0.4	0.8		0.4	0.8		0.2	0.55		V
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = §	-1.5			-1.5			1.5			-1.2			V
V _{OH} High-level output voltage	9	V _{CC} = MIN, I _{OH} = MAX, V _I = V _{T- min}	54 Family	2.4	3.4		2.4	3.4		2.5	3.4		2.5	3.4	V
			74 Family	2.4	3.4		2.4	3.4		2.7	3.4		2.7	3.4	
V _{OL} Low-level output voltage	8	V _{CC} = MIN, V _I = V _{T+} max	I _{OL} = MAX	54 Family	0.2	0.4		0.2	0.4		0.25	0.4		0.5	V
			I _{OL} = 4 mA	74 Family	0.2	0.4		0.2	0.4		0.35	0.5		0.5	
				Series 74LS							0.25	0.4			
I _{T+} Input current at positive-going threshold	8	V _{CC} = 5 V, V _I = V _{T+}	-0.65			-0.43			-0.14			-0.9			mA
I _{T-} Input current at negative-going threshold	9	V _{CC} = 5 V, V _I = V _{T-}	-0.85			-0.56			-0.18			-1.1			mA
I _I Input current at maximum input voltage	4	V _{CC} = MAX	V _I = 5.5 V	1			1			1			mA		
			V _I = 7 V	40			40			0.1					
I _{IH} High-level input current	4	V _{CC} = MAX	V _I = 2.4 V	40			40			20			μA		
			V _I = 2.7 V	20			50			50					
I _{IL} Low-level input current	5	V _{CC} = MAX	V _I = 0.4 V	-1			-1.6			-0.4			mA		
I _{OS} Short-circuit output current*	6	V _{CC} = MAX	-18			-55			-18			-55			mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ I_I = -12 mA for SN54/SN74 and -18 mA for 'LS13, 'LS14, 'LS132, and 'S132.

* Not more than one output should be shorted at a time, and for SN54LS/SN74LS and 'S132, duration of output short-circuit should not exceed one second.

supply current[†]

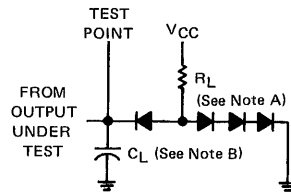
TYPE	I _{CC} H (mA) Total with outputs high		I _{CC} L (mA) Total with outputs low		I _{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'13	14	23	20	32	8.5
'14	22	36	39	60	5.1
'132	15	24	26	40	5.1
'LS13	2.9	6	4.1	7	1.75
'LS14	8.6	16	12	21	1.72
'LS132	5.9	11	8.2	14	1.76
'S132	28	44	44	68	9

[†]Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

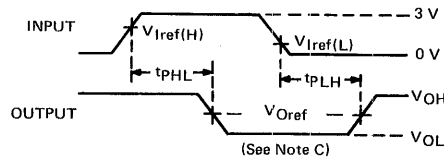
switching characteristics, V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS	t _{PLH} (ns) Propagation delay time, low-to-high-level output			t _{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'13	C _L = 15 pF, R _L = 400 Ω	18	27		15	22	
'14, '132		15	22		15	22	
'LS13	C _L = 15 pF, R _L = 2 kΩ	15	22		18	27	
'LS14		15	22		15	22	
'LS132		15	22		15	22	
'S132	C _L = 15 pF, R _L = 280 Ω	7	10.5		8.5	13	

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



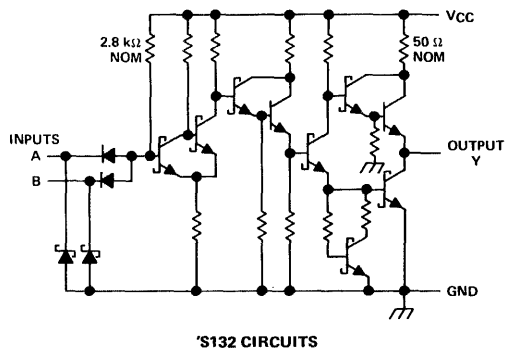
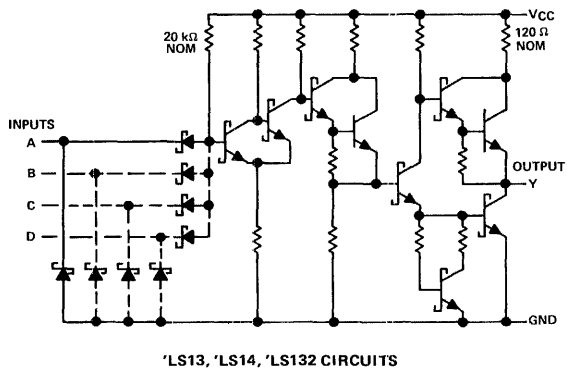
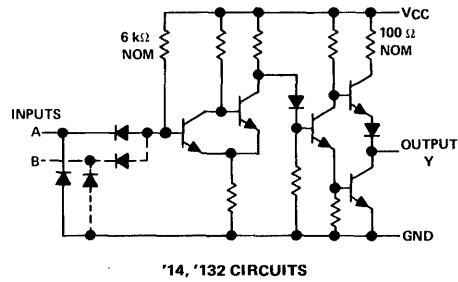
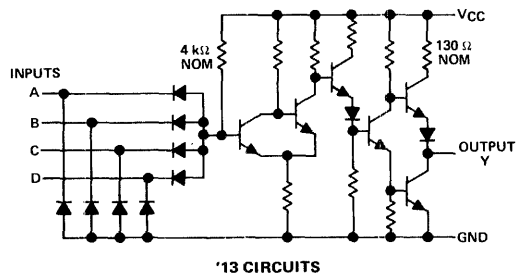
VOLTAGE WAVEFORMS

- NOTES: A. All diodes are 1N916 or 1N3064.
 B. C_L includes probe and jrg capacitance.
 C. Generator characteristics and reference voltages are:

	Generator Characteristics				Reference Voltages		
	Z _{out}	PRR	t _r	t _f	V _{Iref(H)}	V _{Iref(L)}	V _{Oref}
SN54/SN74 [*]	50 Ω	1 MHz	10 ns	10 ns	1.7 V	0.9 V	1.5 V
SN54LS/SN74LS [*]	50 Ω	1 MHz	15 ns	6 ns	1.6 V	0.8 V	1.3 V
'S132	50 Ω	1 MHz	2.5 ns	2.5 ns	1.8 V	1.2 V	1.5 V

**SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS
WITH TOTEM-POLE OUTPUTS**

schematics (each gate)



Resistor values shown are nominal.

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

TYPICAL CHARACTERISTICS OF '13, '14, AND '132 CIRCUITS†

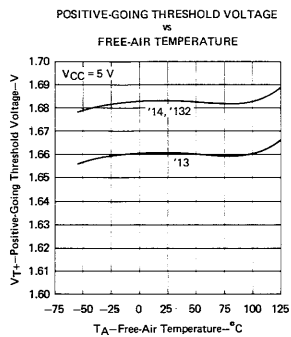


FIGURE 1

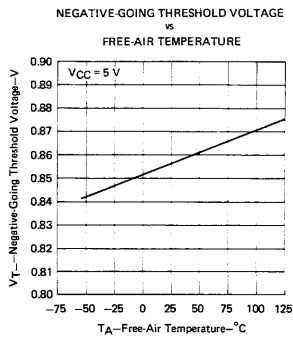


FIGURE 2

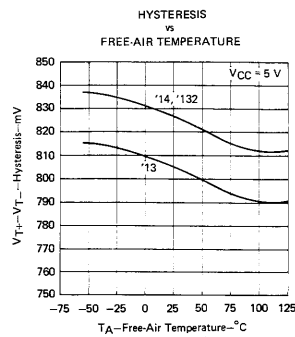


FIGURE 3

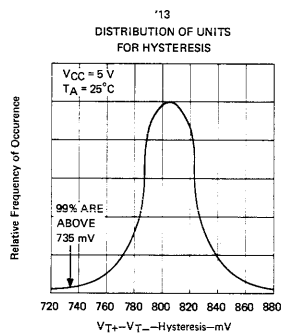


FIGURE 4

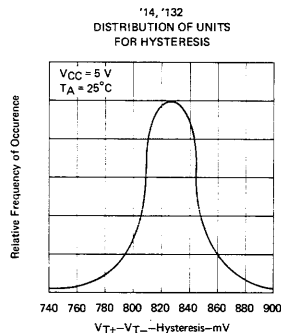


FIGURE 5

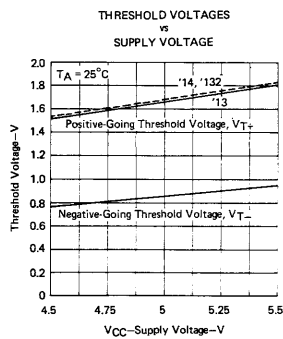


FIGURE 6

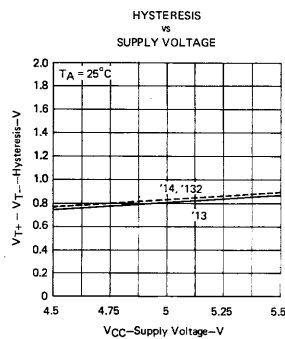


FIGURE 7

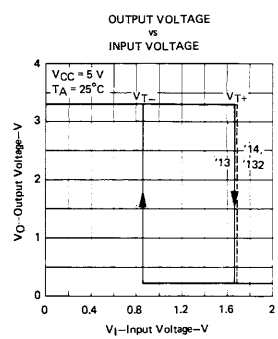
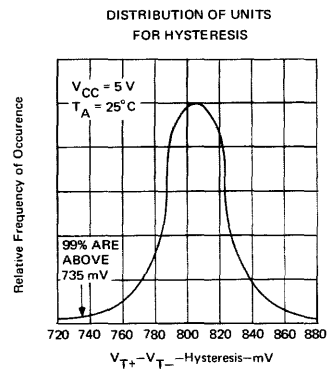
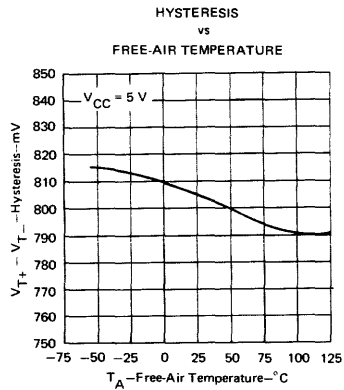
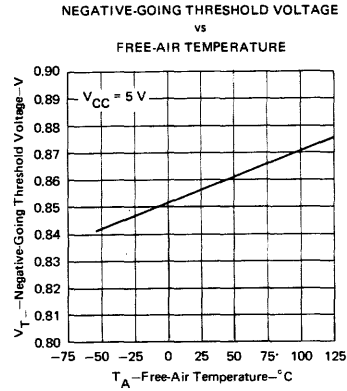
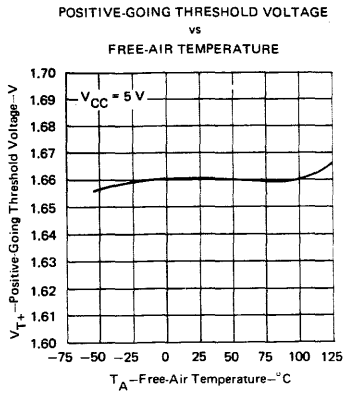


FIGURE 8

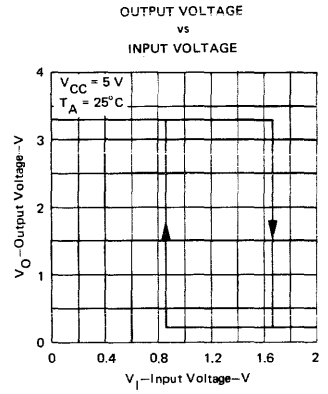
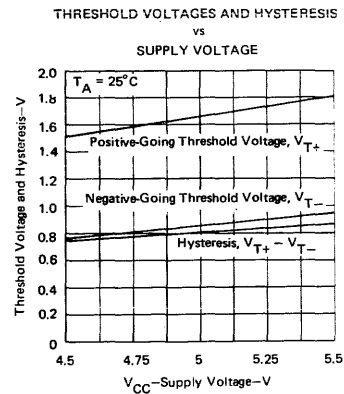
†Data for temperatures below 0°C and 70°C and supply voltages below 4.75V and above 5.25 V are applicable for SN5413, SN5414, and SN54132 only.

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

TYPICAL CHARACTERISTICS OF 'LS13, 'LS14, AND 'LS132 CIRCUITS†



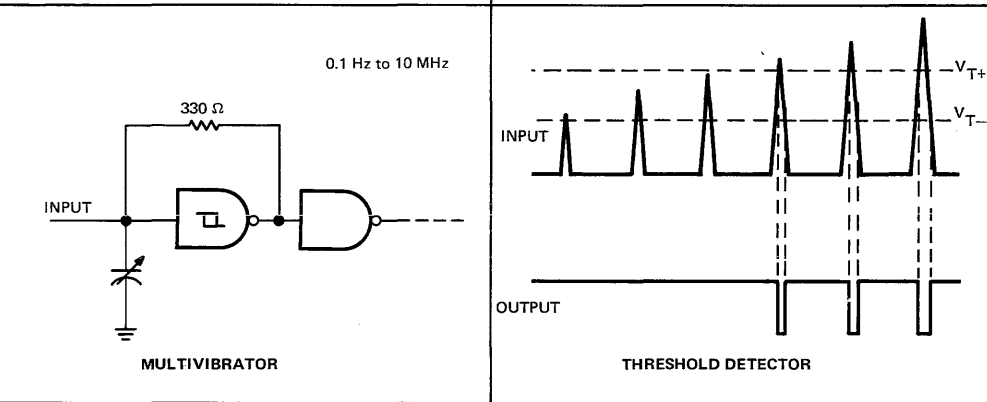
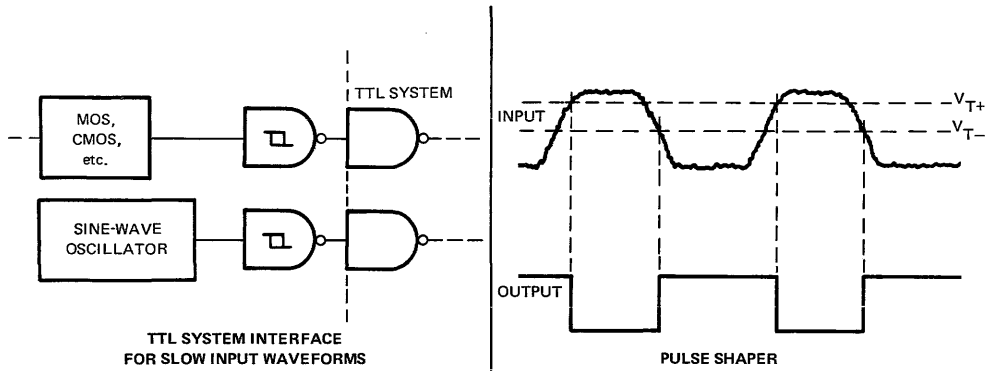
6



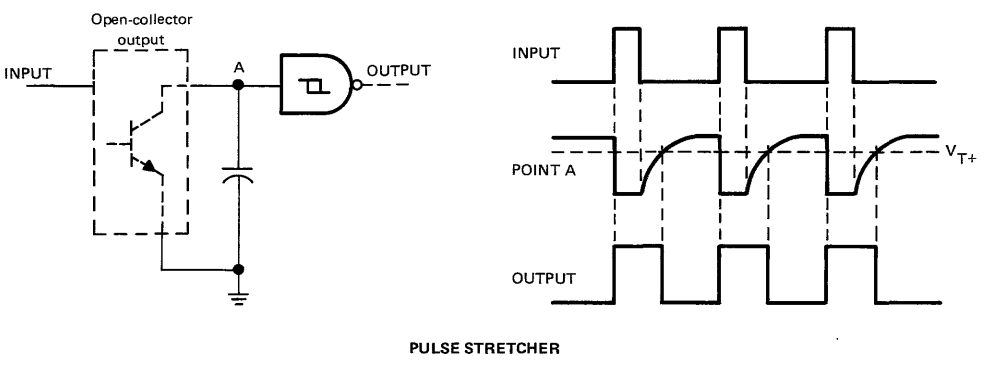
†Data for temperatures below 0°C and above 70°C and supply voltages below 4.75 V and above 5.25 are applicable for SN54LS13, SN54LS14, and SN54LS132 only.

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

TYPICAL APPLICATION DATA



6



recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74						SERIES 54H SERIES 74H			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT	
		'28		'37, '40				'H40			'LS28, 'LS37, 'LS40			'S37, 'S40				
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, V _{CC}	54 Family 74 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V	
High-level output current, I _{OH}		-2.4		-1.2				-1.5			-1.2			-3			mA	
Low-level output current, I _{OL}	54 Family 74 Family	48		48				60			12			60			mA	
Operating free-air temperature, T _A	54 Family 74 Family	-55	125	-55	125	-55	125	-55	125	-55	125	-55	125	-55	125	-55	125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54 SERIES 74						SERIES 54H SERIES 74H			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT															
			'28		'37, '40				'H40			'LS28, 'LS37, 'LS40			'S37, 'S40																		
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX																
V _{IH} High-level input voltage	1, 2		2		2				2			2			2			V															
V _{IL} Low-level input voltage	1, 2		0.8		0.8				0.8			0.7			0.8			V															
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = §	-1.5		-1.5				-1.5			-1.5			-1.2			V															
V _{OH} High-level output voltage	1	V _{CC} = MIN, V _{IL} = V _{IL} max, I _{OH} = MAX	2.4 3.4		2.4 3.3				2.4 3.4			2.5 3.4			2.5 3.4			V															
V _{OL} Low-level output voltage	2	V _{CC} = MIN, V _{IH} = 2 V	I _{OL} = MAX		0.2 0.4		0.2 0.4		0.15 0.3		0.25 0.4		0.5		0.5		V																
			I _{OL} = 12 mA		0.2 0.4		0.2 0.4		0.2 0.4		0.35 0.5		0.5																				
I _I Input current at maximum input voltage	4	V _{CC} = MAX	1		1				0.1			0.1			1			mA															
I _{IH} High-level input current	4	V _{CC} = MAX	40		40				100			20			100			µA															
I _{IL} Low-level input current	5	V _{CC} = MAX	V _{IL} = 0.4 V		-1.6		-1.6				-4			-0.4			-4			mA													
			V _{IL} = 0.5 V																														
I _{OS} Short-circuit output current*	6		-70		-180				-20			-70			-40			-125			-30			-130			-50			-225			mA
I _{CC} Supply current	7	V _{CC} = MAX	-70		-180				-18			-70			-40			-125			-30			-130			-50			-225			mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ I_I = -12 mA for SN54/SN74*, -8 mA for SN54H/SN74H*, and -18 mA for SN54LS/SN74LS* and SN54S/SN74S*.

* Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second for all of these circuits except 'S37 and 'S40, or 100 milli-seconds for 'S37 and 'S40.

See table on next page

supply current[†]

TYPE	I _{CCH} (mA) Total with outputs high		I _{CCL} (mA) Total with outputs low		I _{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'28	12	21	33	57	5.63
'37	9	15.5	34	54	5.38
'40	4	8	17	27	5.25
'H40	10.4	16	25	40	8.85
'LS28	1.8	3.6	6.9	13.8	1.09
'LS37	0.9	2	6	12	0.86
'LS40	0.45	1	3	6	0.86
'S37	20	36	46	80	8.25
'S40	10	18	25	44	8.75

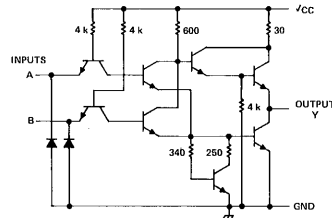
[†]Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

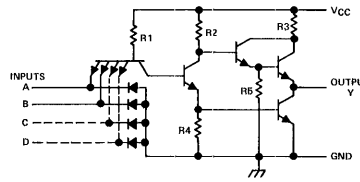
TYPE	TEST CONDITIONS#	t _{PLH} (ns) Propagation delay time, low-to-high-level output			t _{PHL} (ns) Propagation delay time, high-to-low output		
		MIN	TYP	MAX	MIN	TYP	MAX
		'28	C _L = 50 pF, R _L = 133 Ω	6	9	8	12
	C _L = 150 pF, R _L = 133 Ω	10	15	12	18		
'37	C _L = 45 pF, R _L = 133 Ω	13	22	8	15		
'40	C _L = 15 pF, R _L = 133 Ω	13	22	8	15		
'H40	C _L = 25 pF, R _L = 93 Ω	8.5	12	6.5	12		
'LS28		12	24	12	24		
'LS37	C _L = 45 pF, R _L = 667 Ω	12	24	12	24		
'LS40		12	24	12	24		
'S37	C _L = 50 pF, R _L = 93 Ω	4	6.5	4	6.5		
'S40	C _L = 150 pF, R _L = 93 Ω	6		6			

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

schematics (each gate)

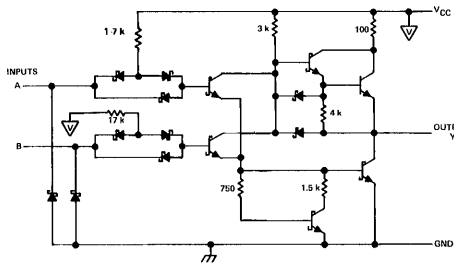


'28 CIRCUITS



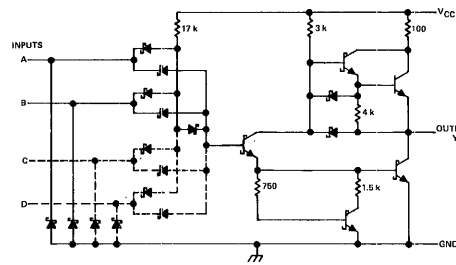
'37, '40, 'H40 CIRCUITS

	'37	'40	'H40
R1	4 k	4 k	1.4 k
R2	600	600	390
R3	100	100	45
R4	400	400	250
R5	4 k	4 k	2 k

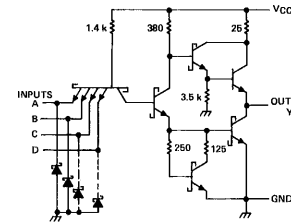


'LS28 CIRCUITS

Resistor values shown are nominal and in ohms.



'LS37, 'LS40 CIRCUITS



'S37, 'S40 CIRCUITS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74			SERIES 54S SERIES 74S			UNIT
		'128			'S140			
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family 74 Family	4.5 4.75	5 5	5.5 5.25	4.5 4.75	5 5	5.5 5.25	V
High-level output current, I_{OH}	54 Family 74 Family			-29 -42.4			-40 -40	mA
Low-level output current, I_{OL}				48			60	mA
Operating free-air temperature, T_A	54 Family 74 Family	-55 0		125 70	-55 0		125 70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54 SERIES 74		SERIES 54S SERIES 74S		UNIT	
			'128		'S140			
			MIN	TYP‡	MAX	MIN		TYP‡
V_{IH} High-level input voltage	1, 2		2		2		V	
V_{IL} Low-level input voltage	1, 2			0.8		0.8	V	
V_{IK} Input clamp voltage	3	$V_{CC} = \text{MIN}, I_I = §$			-1.5		-1.2	V
V_{OH} High-level output voltage	1	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -2.4 \text{ mA}$	54 Family	2.4	3.4			V
			74 Family	2.4	3.4			
		$V_{CC} = \text{MIN}, V_{IL} = 0.4 \text{ V}, I_{OH} = -13.2 \text{ mA}$		2.4				
			$V_{CC} = \text{MIN}, V_{IL} = 0.4 \text{ V}, I_{OH} = \text{MAX}$		2			
		$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -3 \text{ mA}$	54 Family			2.5	3.4	
			74 Family			2.7	3.4	
$V_{CC} = \text{MIN}, V_{IL} = 0.5 \text{ V}, R_O = 50 \Omega \text{ to GND}$				2				
V_{OL} Low-level output voltage	2	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = \text{MAX}$	0.26	0.4		0.5	V	
I_I Input current at maximum input voltage	4	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1		1	mA	
I_{IH} High-level input current	4	$V_{CC} = \text{MAX}$	$V_{IH} = 2.4 \text{ V}$		40		µA	
			$V_{IH} = 2.7 \text{ V}$			100		
I_{IL} Low-level input current	5	$V_{CC} = \text{MAX}$	$V_{IL} = 0.4 \text{ V}$		-1.6		mA	
			$V_{IL} = 0.5 \text{ V}$			-4		
I_{OS} Short-circuit output current*	6	$V_{CC} = \text{MAX}$	-70	-180	-50	-225	mA	
I_{CC} Supply current	Total, outputs high	7	$V_{CC} = \text{MAX}$	12	21	10	18	mA
	Total, outputs low			33	57	25	44	
	Average per gate			5.63		8.75		
		$V_{CC} = 5 \text{ V}, 50\% \text{ duty cycle}$						

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ $I_I = -12 \text{ mA}$ for '128 and -18 mA for 'S140.

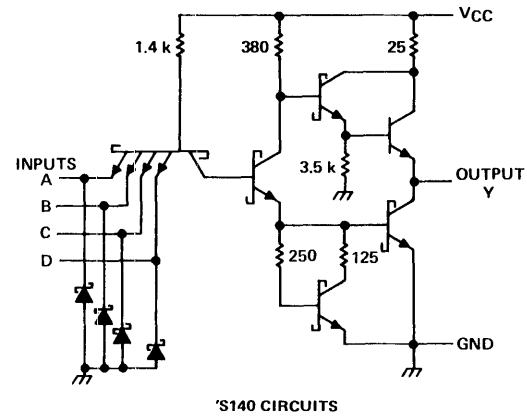
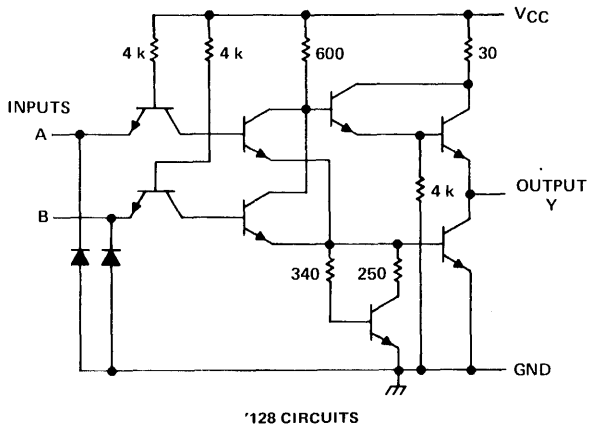
* Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second for '128 or 100 milliseconds for 'S140.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

TYPE	TEST CONDITIONS#	t _{PLH} (ns)			t _{PHL} (ns)		
		Propagation delay time, low-to-high-level output			Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'128	C _L = 50 pF, R _L = 133 Ω		6	9	8	12	
	C _L = 150 pF, R _L = 133 Ω		10	15	12	18	
'S140	C _L = 50 pF, R _L = 93 Ω		4	6.5	4	6.5	
	C _L = 150 pF, R _L = 93 Ω		6		6		

#Load circuit and voltage waveforms are shown on page 3-10.

schematics (each driver)



Resistor values shown are nominal and in ohms.

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54' SERIES 74'												UNIT
		'06, '07			'16, '17			'26			'33, '38			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V _{OH}				30			15			15			5.5	V
Low-level output current, I _{OL}	54 Family			30			30			16			48	mA
	74 Family			40			40			16			48	
Operating free-air temperature, T _A	54 Family	-55		125	-55		125	-55		125	-55		125	°C
	74 Family	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54' SERIES 74'												UNIT
			'06, '07			'16, '17			'26			'33, '38			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V _{IH} High-level input voltage	1, 2		2			2			2			2			V
V _{IL} Low-level input voltage	1, 2			0.8			0.8			0.8			0.8	V	
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = -12 mA			-1.5			-1.5			-1.5			-1.5	V
I _{OH} High-level output current	1	V _{CC} = MIN, V _I = ▲								50			250	μA	
		V _{OH} = 12 V			250			250		1000			250		
		V _{OH} = MAX													
V _{OL} Low-level output voltage	2	V _{CC} = MIN, V _I = ▲			0.4			0.4		0.4			0.4	V	
		I _{OL} = 16 mA			0.7			0.7		0.4			0.4		
		I _{OL} = MAX													
I _I Input current at maximum input voltage	4	V _{CC} = MAX, V _I = 5.5 V			1			1		1			1	mA	
I _{IH} High-level input current	4	V _{CC} = MAX, V _{IH} = 2.4 V			40			40		40			40	μA	
I _{IL} Low-level input current	5	V _{CC} = MAX, V _{IL} = 0.4 V			-1.6			-1.6		-1.6			-1.6	mA	
I _{CC} Supply current	7	V _{CC} = MAX												mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

▲ The input voltage is V_{IH} = 2 V or V_{IL} = V_{IL} max, as appropriate. See tables with test figures 1 and 2.

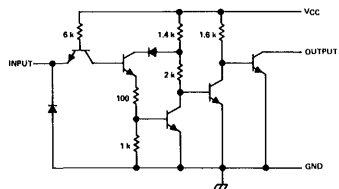
See table on next page

supply current[†]

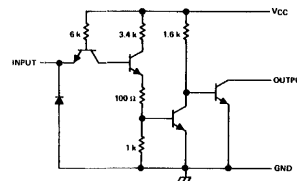
TYPE	I _{CC} H (mA) Total with outputs high		I _{CC} L (mA) Total with outputs low		I _{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'06, '16	30	48	32	51	5.17
'07, '17	29	41	21	30	4.17
'26	4	8	12	22	2.00
'33	12	21	33	57	5.63
'38	5	8.5	34	54	4.88

[†]Maximum values of I_{CC} shown are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

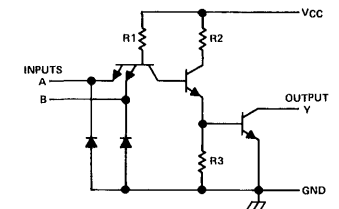
schematics (each gate)



'06, '16 CIRCUITS

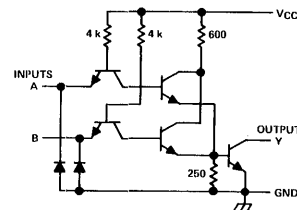


'07, '17 CIRCUITS



CIRCUITS	R1	R2	R3
'26	4 kΩ	1.6 kΩ	.1 kΩ
'38	4 kΩ	600 Ω	400 Ω

'26, '38 CIRCUITS



'33 CIRCUITS

switching characteristics, V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS#	t _{PLH} (ns) Propagation delay time, low-to-high-level output		t _{PHL} (ns) Propagation delay time, high-to-low-level output	
		TYP	MAX	TYP	MAX
		'06, '16	C _L = 15 pF, R _L = 110 Ω	10	15
'07, '17	6	10		20	30
'26	C _L = 15 pF, R _L = 1 kΩ	16	24	11	17
'33	C _L = 50 pF, R _L = 133 Ω	10	15	12	18
	C _L = 150 pF, R _L = 133 Ω	15	22	16	24
'38	C _L = 45 pF, R _L = 667 Ω	14	22	11	18

#Load circuit and voltage waveforms are shown on page 3-10.

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54LS' SERIES 74LS'									UNIT			
		'LS26			'LS33			'LS38				'S38		
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX		MIN	NOM	MAX
Supply voltage, V _{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
High-level output voltage, V _{OH}		15			5.5			5.5			5.5			V
Low-level output current, I _{OL}	54 Family	4			12			12			60			mA
	74 Family	8			24			24			60			mA
Operating free-air temperature, T _A	54 Family	-55			125			-55			125			°C
	74 Family	0			70			0			70			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54LS' SERIES 74LS'									UNIT						
			'LS26			'LS33			'LS38				'S38					
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX		MIN	TYP‡	MAX			
V _{IH} High-level input voltage	1, 2		2			2			2			2			V			
V _{IL} Low-level input voltage	1, 2		54 Family			0.7			0.7			0.8			V			
			74 Family			0.8			0.8			0.8			V			
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = §	-1.5			-1.5			-1.5			-1.2			V			
I _{OH} High-level output current	1	V _{CC} = MIN, V _I = ▲	V _{OH} = 12 V			50									μA			
			V _{OH} = MAX			1000			250			250			μA			
V _{OL} Low-level output voltage	2	V _{CC} = MIN, V _I = ▲	54 Family			0.25			0.4			0.25			0.4			V
		I _{OL} = MAX	74 Family			0.35			0.5			0.35			0.5			V
		I _{OL} = 4 mA	Series 74LS'			0.25			0.4									V
		I _{OL} = 12 mA				0.25			0.4									V
I _I Input current at maximum input voltage	4	V _{CC} = MAX	V _I = 5.5 V									1			mA			
			V _I = 7 V			0.1			0.1			0.1			mA			
I _{IH} High-level input current	4	V _{CC} = MAX	V _{IH} = 2.7 V			20			20			100			μA			
I _{IL} Low-level input current	5	V _{CC} = MAX	V _{IL} = 0.4 V			-0.4			-0.4			-0.4			mA			
			V _{IL} = 0.5 V									-4			mA			
I _{CC} Supply current	7	V _{CC} = MAX	See table on next page												mA			

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ I_I = -18 mA for SN54LS/SN74LS' and -12 mA for SN54S/SN74'.

▲ The input voltage is V_{IH} = 2 V or V_{IL} = V_{IL} max, as appropriate. See tables with test figures 1 and 2.

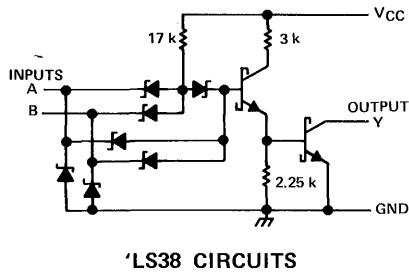
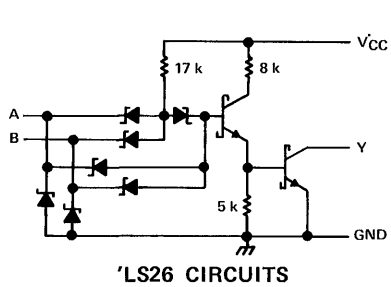
SERIES 54LS/74LS AND SERIES 54S/74S
BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

supply current[†]

TYPE	I _{CCH} (mA) Total with outputs high		I _{CCL} (mA) Total with outputs low		I _{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'LS26	0.8	1.6	2.4	4.4	0.4
'LS33	1.8	3.6	6.9	13.8	1.09
'LS38	0.9	2	6	12	0.86
'S38	20	36	46	80	8.25

[†]Maximum values of I_{CC} shown are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

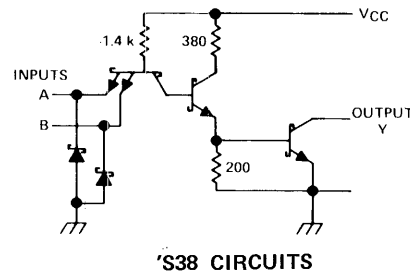
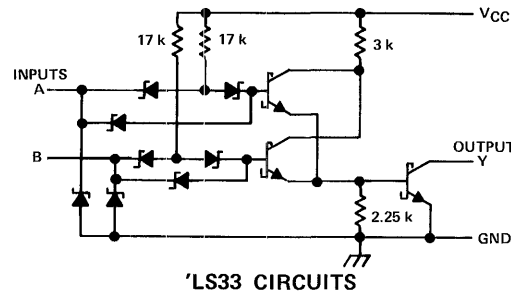
schematics (each gate)



switching characteristics, V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS [#]	t _{PLH} (ns) Propagation delay time, low-to-high-level output		t _{PHL} (ns) Propagation delay time, high-to-low-level output		
		TYP	MAX	TYP	MAX	
		'LS26	C _L = 15 pF, R _L = 2 kΩ	17	32	15
'LS33	C _L = 45 pF, R _L = 667 Ω	20	32	18	28	
'LS38		20	32	18	28	
'S38	R _L = 93 Ω	C _L = 50 pF	6.5	10	6.5	10
		C _L = 150 pF	9		8.5	

[#]Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.



SERIES 54LS/74LS AND SERIES 54S/74S
BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT
		'32			'LS32			'S32			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	54 Family 74 Family	4.5 4.75	5 5	5.5 5.25	4.5 4.75	5 5	5.5 5.25	4.5 4.75	5 5	5.25 5.25	V
High-level output current, I _{OH}				-800			-400			-1000	μA
Low-level output current, I _{OL}	54 Family 74 Family			16 16			4 8			20 20	mA
Operating free-air temperature, T _A	54 Family 74 Family	-55 0		125 70	-55 0		125 70	-55 0		125 70	C

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54 SERIES 74			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT	
			'32			'LS32			'S32				
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IH} High-level input voltage	1, 2		2			2			2			V	
V _{IL} Low-level input voltage	1, 2		0.8			0.7			0.8			V	
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = §	-1.5			-1.5			-1.2			V	
V _{OH} High-level output voltage	1	V _{CC} = MIN, V _{IH} = 2 V, I _{OH} = MAX	54 Family 74 Family			2.4 3.4 2.7 3.4			2.5 3.4 2.7 3.4			V	
V _{OL} Low-level output voltage	2	V _{CC} = MIN, V _{IL} = V _{IL max} , I _{OL} = MAX, I _{OL} = 4 mA	54 Family 74 Family Series 74LS			0.2 0.4 0.2 0.4 0.25 0.4			0.25 0.4 0.35 0.5 0.25 0.4			V	
I _I Input current at maximum input voltage	4	V _{CC} = MAX	V _I = 5.5 V V _I = 7 V			1 0.1			1			mA	
I _{IH} High-level input current	4	V _{CC} = MAX	V _{IH} = 2.4 V V _{IH} = 2.7 V			40			20 50			μA	
I _{IL} Low-level input current	5	V _{CC} = MAX	V _{IL} = 0.4 V V _{IL} = 0.5 V			-1.6 -0.4			-2 -2			mA	
I _{OS} Short-circuit output current*	6	V _{CC} = MAX	54 Family 74 Family			-20 -18			-55 -55 -20			-100 -40 -100 -100 -40 -100	mA
I _{CC} Supply current	7	Total, outputs high	15 22			3.1 6.2			18 32			mA	
Total, outputs low		23 38			4.9 9.8			38 68					
Average per gate		V _{CC} = 5 V, 50% duty cycle			4.75			1.0 7					

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

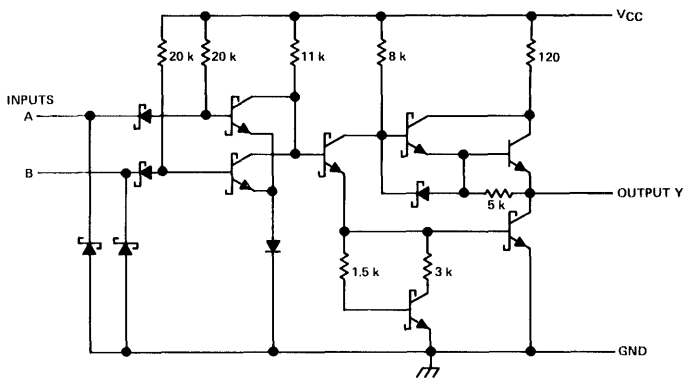
§ I_I = -12 mA for SN54/SN74' and -18 mA for SN54LS/SN74LS' and SN54S/SN74S'.

* Not more than one output should be shorted at a time, and for SN54LS/SN74LS' and SN54S/SN74S', duration of the short-circuit should be less than one second.

switching characteristics at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

TYPE	TEST CONDITIONS#	t _{PLH} (ns) Propagation delay time, low-to-high-level output			t _{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'32	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$	10	15		14	22	
'LS32	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$	14	22		14	22	
'S32	$C_L = 15\text{ pF}$, $R_L = 280\ \Omega$	4	7		4	7	
	$C_L = 50\text{ pF}$, $R_L = 280\ \Omega$	5			5		

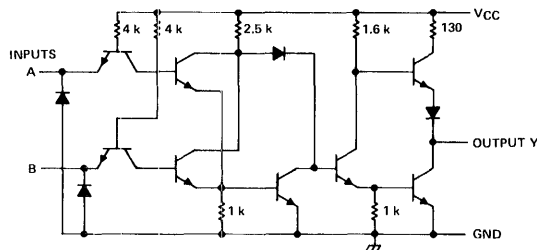
#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.



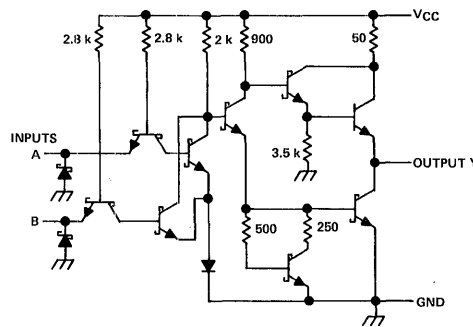
'LS32 CIRCUITS

Resistor values shown are nominal and in ohms.

schematics (each gate)



'32 CIRCUITS



'S32 CIRCUITS

POSITIVE-OR GATES WITH TOTEM-POLE OUTPUTS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74			SERIES 54H SERIES 74H			SERIES 54L SERIES 74L			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT
		'51, '54			'H51, 'H54			'L51, 'L54, 'L55			'LS51, 'LS54, 'LS55			'S51, 'S64			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	54 Family 74 Family	4.5 4.75	5 5	5.5 5.25	4.5 4.75	5 5	5.5 5.25	4.5 4.75	5 5	5.5 5.25	4.5 4.75	5 5	5.5 5.25	4.5 4.75	5 5	5.5 5.25	V
High-level output current, I _{OH}	54 Family 74 Family			-400			-500			-100			-400			-1000	μA
Low-level output current, I _{OL}	54 Family 74 Family			16			20			2			4			20	mA
Operating free-air temperature, T _A	54 Family 74 Family	-55 0		125 70	-55 0		125 70	-55 0		125 70	-55 0		125 70	-55 0		125 70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54 SERIES 74			SERIES 54H SERIES 74H			SERIES 54L SERIES 74L			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT	
			'51, '54			'H51, 'H54			'L51, 'L54, 'L55			'LS51, 'LS54, 'LS55			'S51, 'S64				
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IH} High-level input voltage	1, 2		2			2			2			2			2			V	
V _{IL} Low-level input voltage	1, 2		54 Family 74 Family			0.8 0.8			0.8 0.8			0.7 0.7			0.8 0.8			V	
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = §	-1.5			-1.5						-1.5			-1.2			V	
V _{OH} High-level output voltage	1	V _{CC} = MIN, V _{IL} = V _{IL max} , I _{OH} = MAX	74 Family			2.4 3.4			2.4 3.4			2.4 3.3			2.5 3.4			2.5 3.4	V
V _{OL} Low-level output voltage	2	V _{CC} = MIN, V _{IH} = 2 V	54 Family 74 Family Series 74LS			0.2 0.4 0.2 0.4			0.2 0.4 0.2 0.4			0.15 0.3 0.2 0.4			0.25 0.4 0.35 0.5			0.5 0.5	V
I _I Input current at maximum input voltage	4	V _{CC} = MAX	V _I = 5.5 V V _I = 7 V			1 1			0.1			0.1			1			mA	
I _{IH} High-level input current	4	V _{CC} = MAX	V _{IH} = 2.4 V V _{IH} = 2.7 V			40 50			10			20			50			μA	
I _{IL} Low-level input current	5	V _{CC} = MAX	V _{IL} = 0.3 V V _{IL} = 0.4 V V _{IL} = 0.5 V			-1.6 -2			-0.18			-0.4			-2			mA	
I _{OS} Short-circuit output current*	6	V _{CC} = MAX	54 Family 74 Family			-20 -18			-55 -55			-40 -40			-100 -100			-40 -40	mA
I _{CC} Supply current	7	V _{CC} = MAX	See table on next page															mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ I_I = -12 mA for SN54/SN74, -8 mA for SN54H/SN74H, and -18 mA for SN54L/SN74L and SN54S/SN74S.

◆ Not more than one output should be shorted at a time, and for SN54LS/SN74LS, SN54H/SN74H, and SN54S/SN74S, duration of the short-circuit should not exceed one second.

supply current†

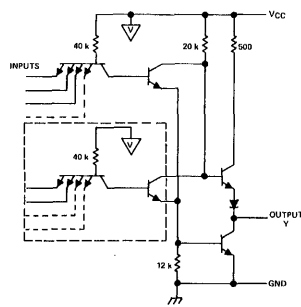
TYPE	I _{CC} H (mA) Total with outputs high		I _{CC} L (mA) Total with outputs low		I _{CC} (mA) Average per AOI gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'51	4	8	7.4	14	2.85
'54	4	8	5.1	9.5	4.55
'H51	8.2	12.8	15.2	24	5.85
'H54	7.1	11	9.4	14	8.25
'L51	0.44	0.8	0.76	1.3	0.30
'L54	0.39	0.8	0.60	0.99	0.50
'L55	0.22	0.4	0.38	0.65	0.30
'LS51	0.8	1.6	1.4	2.8	0.55
'LS54	0.8	1.6	1.0	2	0.9
'LS55	0.4	0.8	0.7	1.3	0.55
'S51	8.2	17.8	13.6	22	5.45
'S64	7	12.5	8.5	16	7.75

†Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25° C.

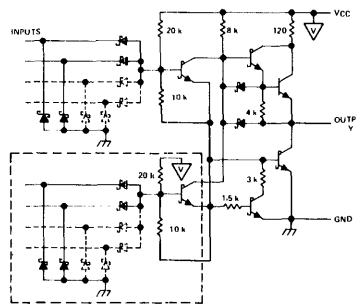
schematics (each gate)

The portion of the circuits within the dashed lines is repeated (with as many emitters or input diodes as applicable) for each additional AND section.

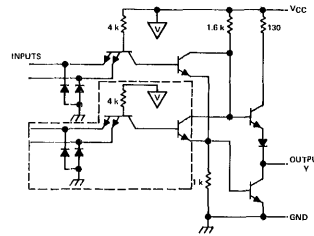
Resistor values shown are nominal and in ohms.



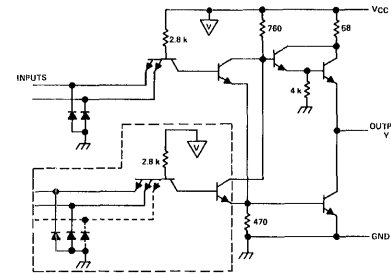
'L51, 'L54, 'L55 CIRCUITS



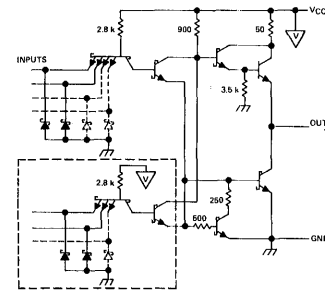
'LS51, 'LS54, 'LS55 CIRCUITS



'51, '54 CIRCUITS



'H51, 'H54 CIRCUITS



'S51, 'S64 CIRCUITS

switching characteristics at V_{CC} = 5 V, T_A = 25° C

TYPE	TEST CONDITIONS#	t _{PLH} (ns) Propagation delay time, low-to-high-level output			t _{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
		'51, '54	C _L = 15 pF, R _L = 400 Ω	13	22	8	15
'H51	C _L = 25 pF, R _L = 280 Ω	6.8	11	6.2	11		
'H54	C _L = 25 pF, R _L = 280 Ω	7	11	6.2	11		
'L51, 'L54, 'L55	C _L = 50 pF, R _L = 4 kΩ	50	90	35	60		
'LS51, 'LS55	C _L = 15 pF, R _L = 2 kΩ	12	20	12.5	20		
'LS54	C _L = 15 pF, R _L = 2 kΩ	12	20	12.5	20		
'S51, 'S64	C _L = 15 pF, R _L = 280 Ω	3.5	5.5	3.5	5.5		
	C _L = 50 pF, R _L = 280 Ω	5		5.5			

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

recommended operating conditions

	SN54S65			SN74S65			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}	5.5			5.5			V
Low-level output current, I_{OL}	20			20			mA
Operating free-air temperature, T_A	-55	125		0	70		$^{\circ}$ C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	'S65			UNIT	
			MIN	TYP‡	MAX		
V_{IH} High-level input voltage	1, 2		2			V	
V_{IL} Low-level input voltage	1, 2		0.8			V	
V_{IK} Input clamp voltage	3	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.2			V	
I_{OH} High-level output current	1	$V_{CC} = \text{MIN}, V_{IH} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$	250			μ A	
V_{OL} Low-level output voltage	2	$V_{CC} = \text{MIN}, V_{IL} = 2 \text{ V}, I_{OL} = 20 \text{ mA}$	0.5			V	
I_I Input current at maximum input voltage	4	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	1			mA	
I_{IH} High-level input current	4	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$	50			μ A	
I_{IL} Low-level input current	5	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$	-2			mA	
I_{CCH} Supply current, output high	7	$V_{CC} = \text{MAX}$	6			11	mA
I_{CCL} Supply current, output low	7	$V_{CC} = \text{MAX}$	8.5			16	mA

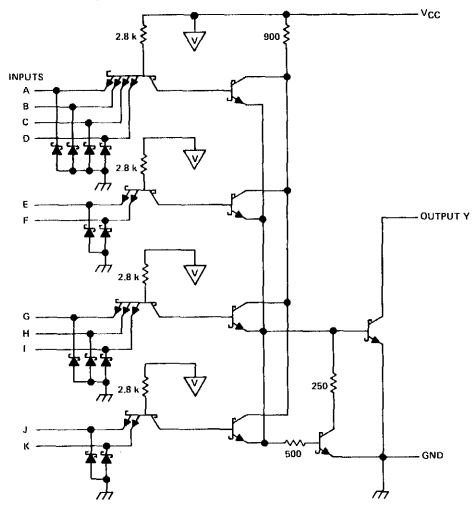
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ} \text{ C}$.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ} \text{ C}$

PARAMETER	TEST CONDITIONS#	'S65			UNIT
		MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}, R_L = 280 \Omega$	2	5	7.5	ns
	$C_L = 50 \text{ pF}, R_L = 280 \Omega$	8			ns
t_{PHL} Propagation delay time, high-to-low-level output	$C_L = 15 \text{ pF}, R_L = 280 \Omega$	2	5.5	8.5	ns
	$C_L = 50 \text{ pF}, R_L = 280 \Omega$	6.5			ns

#1 Load circuit and voltage waveforms are shown on page 3-10.

schematic



Resistor values shown are nominal and in ohms.

AND-OR-INVERT GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT	
		'126, '126, '426, '426			'LS126, 'LS126			'S134				
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, V _{CC}	54 Family 74 Family	4.5 4.75	5 5	5.5 5.25	4.5 4.75	5 5	5.5 5.25	4.5 4.75	5 5	5.5 5.25	V	
High-level output current, I _{OH}	54 Family 74 Family	-2 -5.2			-1 -2.6			-2 -6.5			mA	
Low-level output current, I _{OL}	54 Family 74 Family	16 16			8 16			20 20			mA	
Operating free-air temperature, T _A	54 Family 74 Family	-55 0			125 70			-55 0			125 70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54 SERIES 74		SERIES 54LS SERIES 74LS		SERIES 54S SERIES 74S		UNIT
			'126, '126, '426, '426		'LS126, 'LS126		'S134		
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage	1, 2		2		2		2		V
V _{IL} Low-level input voltage	1, 2		54 Family 74 Family		0.8 0.8		0.7 0.8		V
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = §			-1.5		-1.5		V
V _{OH} High-level output voltage	1	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = MAX	54 Family 74 Family		2.4 3.3 2.4		2.4 3.4		V
V _{OL} Low-level output voltage	2	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OL} = MAX	54 Family 74 Family		0.4 0.4		0.25 0.5 0.35 0.5		V
I _{OZ} Off-state (high-impedance state) output current	19	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OL} = 8 mA	V _O = 2.4 V V _O = 0.4 V V _O = 0.5 V		40 -40		20 -20		μA
I _I Input current at maximum input voltage	4	V _{CC} = MAX	V _I = 5.5 V V _I = 7 V		1		0.1		mA
I _{IH} High-level input current	4	V _{CC} = MAX	V _{IH} = 2.4 V V _{IH} = 2.7 V		40		20 50		μA
I _{IL} Low-level input current	5	V _{CC} = MAX	V _{IL} = 0.4 V V _{IL} = 0.5 V		-1.6		-0.4		mA
I _{OS} Short-circuit output current* I _{CC} Supply current	6 7	V _{CC} = MAX	54 Family 74 Family		-30 -28		-70 -70		mA
					-40 -40		-225 -225		mA
							-40 -40		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ I_I = -12 mA for SN54/SN74' and -18 mA for SN54LS/SN74LS' and SN54S/SN74S'.

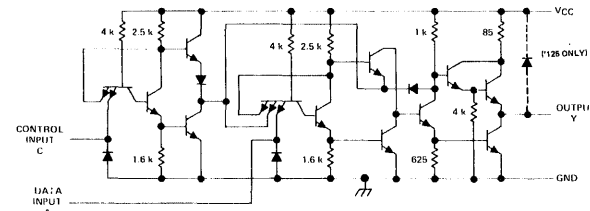
* Not more than one output should be shorted at a time, and for SN54LS/SN74LS' and SN54S/SN74S', duration of the short circuit should not exceed one second.

supply current[†]

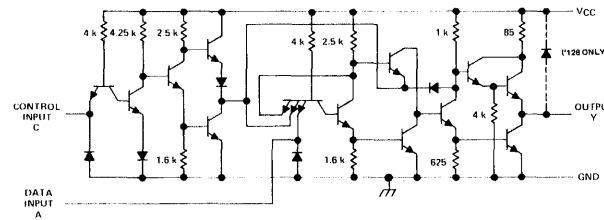
TYPE	TEST CONDITIONS		I _{CC} (mA)		
	DATA INPUTS	OUTPUT CONTROLS	MIN	TYP	MAX
'125, '425	0 V	4.5 V		32	54
'126, '426	0 V	0 V		36	62
'LS125	0 V	4.5 V		11	20
'LS126	0 V	0 V		12	22
'S134	0 V	0 V		7	13
	5 V	0 V		9	16
	5 V	5 V		14	25

[†]Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

schematics (each gate)



'125, '425 CIRCUITS



'126, '426 CIRCUITS

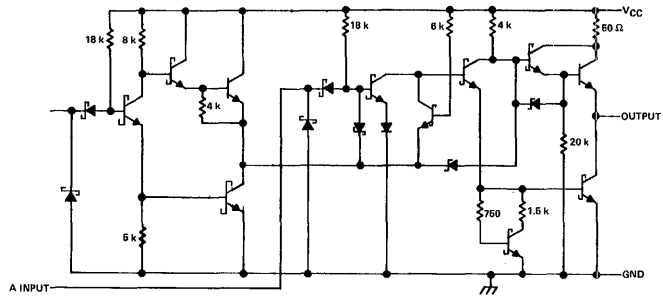
Resistor values shown are nominal and in ohms.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

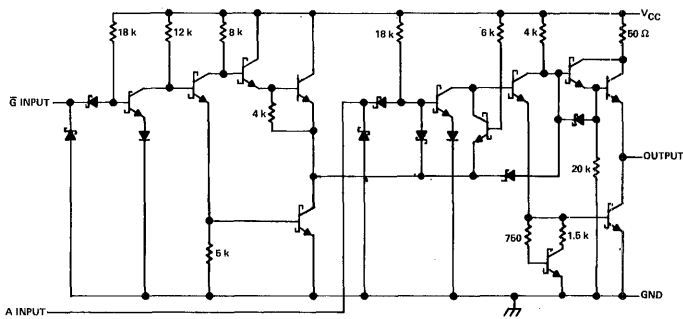
PARAMETER	SERIES 54/74				SERIES 54LS/74LS				SERIES 54S/74S		UNIT		
	TEST CONDITIONS#	'125, '425 TYP MAX	'126, '426 TYP MAX		TEST CONDITIONS#	'LS125 TYP MAX	'LS126 TYP MAX		'S134 TYP MAX				
t _{PLH} Propagation delay time, low-to-high-level output	C _L = 50 pF, R _L = 400 Ω	8	13	8	13	9	15	9	15	C _L = 15 pF, R _L = 280 Ω	4	6	ns
t _{PHL} Propagation delay time, high-to-low-level output		12	18	12	18	7	18	8	18	C _L = 50 pF, R _L = 280 Ω	5.5	7	
t _{PZH} Output enable time to high level	C _L = 5 pF, R _L = 400 Ω	11	17	11	18	12	20	16	25	C _L = 50 pF, R _L = 280 Ω	13	19.5	ns
t _{PZL} Output enable time to low level		16	25	16	25	15	25	21	35		14	21	
t _{PHZ} Output disable time from high level	C _L = 5 pF, R _L = 400 Ω	5	8	10	16	20	25	25	25	C _L = 5 pF, R _L = 280 Ω	5.5	8.5	ns
t _{PLZ} Output disable time from low level		7	12	12	18	20	25	25	25		9	14	

#Load circuit and voltage waveforms are shown on page 3-10.

schematics (each gate)

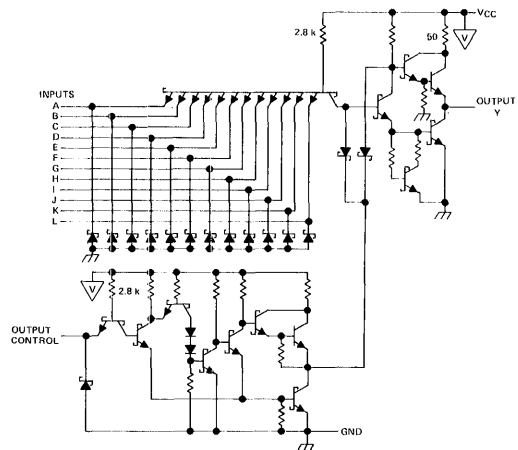


'LS125 CIRCUITS



'LS126 CIRCUITS

Resistor values shown are nominal and in ohms.



'S134 CIRCUITS

GATES WITH 3-STATE OUTPUTS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74			SERIES 54LS SERIES 74LS			UNIT
		'365A, '366A '367A, '368A			'LS365, 'LS366 'LS367, 'LS368			
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	54 Family 74 Family	4.5 4.75	5 5	5.5 5.25	4.5 4.75	5 5	5.5 5.25	V
High-level output current, I _{OH}	54 Family 74 Family			-2 -5.2			-1 -2.6	mA
Low-level output current, I _{OL}	54 Family 74 Family			32 32			8 16	mA
Operating free-air temperature, T _A	54 Family 74 Family	-55 0		125 70	-55 0		125 70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54 SERIES 74			SERIES 54LS SERIES 74LS			UNIT
			'365A, '366A '367A, '368A			'LS365, 'LS366 'LS367, 'LS368			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage	1, 2			2		2		V	
V _{IL} Low-level input voltage	1, 2		54 Family 74 Family		0.8 0.8		0.7 0.8	V	
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = §					-1.5	V	
V _{OH} High-level output voltage	1	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL max} , I _{OH} = MAX	54 Family 74 Family	2.4 2.4	3.3 3.1	2.4 2.4	3.3 3.1	V	
V _{OL} Low-level output voltage	2	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL max} , I _{OL} = MAX, I _{OL} = 8 mA	54 Family 74 Family Series 74LS		0.4 0.4		0.25 0.35 0.25	0.4 0.5 0.4	V
I _{OZ} Off-state (high-impedance state) output current	19	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{IL max}			40 -40		20 -20	µA	
I _I Input current at maximum input voltage	4	V _{CC} = MAX			1		0.1	mA	
I _{IH} High-level input current	4	V _{CC} = MAX			40		20	µA	
I _{IL} Low-level input current	A inputs	V _{CC} = MAX, V _I = 0.5 V, Either \bar{G} input at 2 V			-40		-20	µA	
		V _{CC} = MAX, V _I = 0.4 V, Both \bar{G} inputs at 0.4 V			-1.6		-0.4	mA	
I _{IL} Low-level input current	\bar{G} inputs	V _{CC} = MAX, V _I = 0.4 V			-1.6		-0.4	mA	
		V _{CC} = MAX			-40	-130	-40	-225	mA
I _{OS} Short-circuit output current*	6	V _{CC} = MAX			-40	-130	-40	-225	mA
I _{CC} Supply current	7	V _{CC} = MAX			See table on next page			mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
 ‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
 § I_I = -12 mA for SN54/SN74 and -18 mA for SN54LS/SN74LS, SN54S/SN74S.
 * Not more than one output should be shorted at a time, and for SN54LS/SN74LS and SN54S/SN74S, duration of output short-circuit should not exceed one second.

supply current[†]

TYPE	DATA INPUTS	OUTPUT CONTROLS	I _{CC} (mA)	
			TYP	MAX
'365A, '367A	0 V	4.5 V	65	85
'366A, '368A	0 V	4.5 V	59	77
'LS365, 'LS367	0 V	4.5 V	14	24
'LS366, 'LS368	0 V	4.5 V	12	21

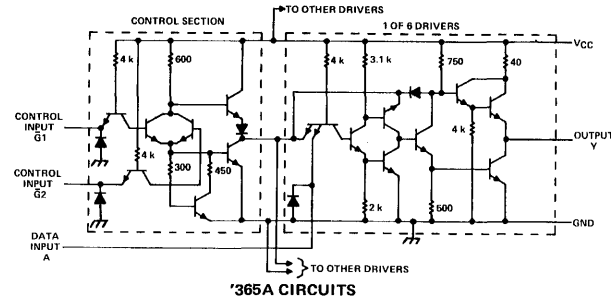
[†] Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 1

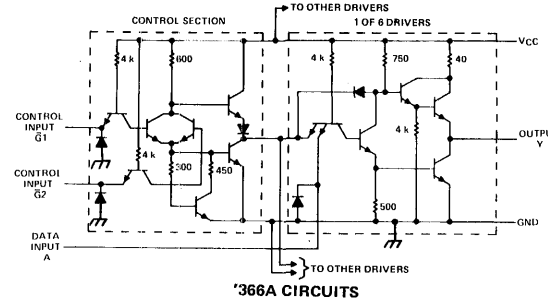
PARAMETER*	TEST CONDITIONS	SERIES 54/74				TEST CONDITIONS	SERIES 54LS/74LS			
		'365A, '367A		'366A, '368A			'LS365, 'LS367		'LS366, 'LS368	
		TYP	MAX	TYP	MAX		TYP	MAX	TYP	MAX
t _{PLH}	C _L = 50 pF, R _L = 400 Ω	16		17		10	16	7	15	
t _{PHL}		22		16		9	22	12	18	
t _{PZH}	C _L = 30 pF, R _L = 1 kΩ	35		35		19	35	18	35	
t _{PZL}		37		37		24	40	28	45	
t _{PHZ}	C _L = 5 pF, R _L = 400 Ω	11		11			30		32	
t _{PLZ}		27		27		35		35		

*t_{PLH} = Propagation delay time, low-to-high-level output
 t_{PHL} = Propagation delay time, high-to-low-level output
 t_{PZH} = Output enable time to high level
 t_{PZL} = Output enable time to low level
 t_{PHZ} = Output disable time from high level
 t_{PLZ} = Output disable time from low level
 NOTE 1: Load circuits and voltage waveforms are shown on pages 3-10 and 3-11.

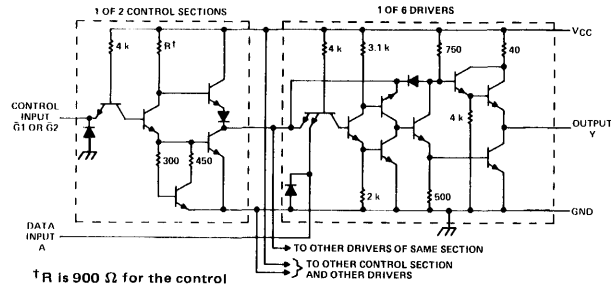
schematics



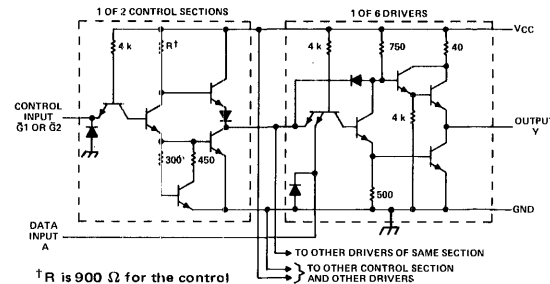
'365A CIRCUITS



'366A CIRCUITS



'367A CIRCUITS



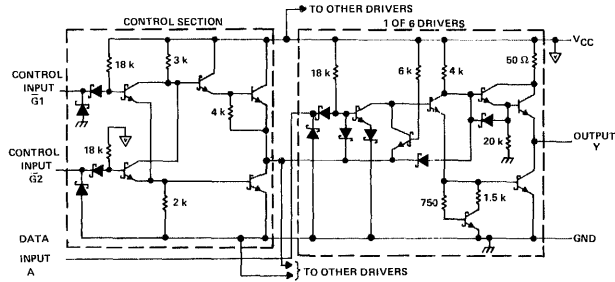
'368A CIRCUITS

[†] R is 900 Ω for the control section associated with G₁ and 600 Ω for the control section associated with G₂.

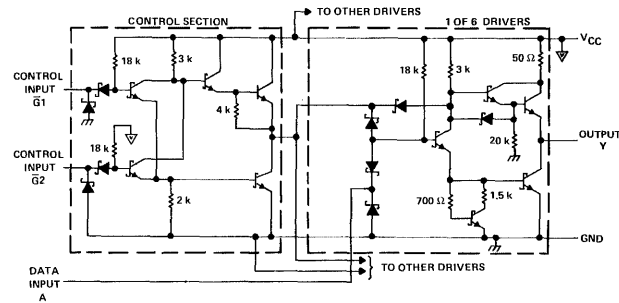
[†] R is 900 Ω for the control section associated with G₁ and 600 Ω for the control section associated with G₂.

Resistor values shown are nominal and in ohms.

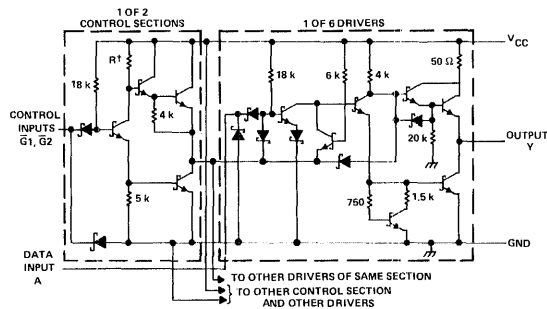
HEX BUS DRIVERS WITH 3-STATE OUTPUTS



'LS365 CIRCUITS

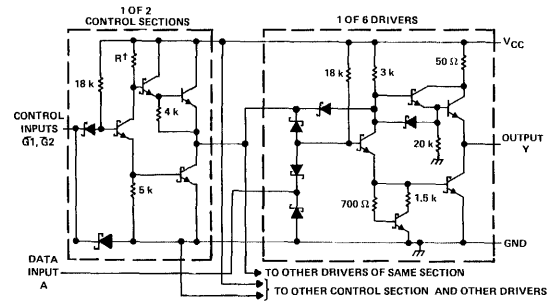


'LS366 CIRCUITS



'LS367 CIRCUITS

† R is 5 kΩ for the control section associated with G1 and 8 kΩ for the control section associated with G2.



'LS368 CIRCUITS

† R is 5 kΩ for the control section associated with G1 and 8 kΩ for the control section associated with G2.

Resistor values shown are nominal and in ohms

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74						SERIES 54H SERIES 74H			UNIT
		'23			'50, '53			'H50, 'H52, 'H53, 'H55			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}				-800			-400			-500	μ A
Low-level output current, I_{OL}	54 Family			16			16			20	mA
	74 Family			16			16			20	
Operating free-air temperature range, T_A	54 Family	-55		125	-55		125	-55		125	$^{\circ}$ C
	74 Family	0		70	0		70	0		70	

The '23, '50, and '53 are designed for use with up to four '60 expanders.

The 'H50, 'H53, and 'H55 are designed for use with up to four 'H60 expanders or one 'H62 expander.

The 'H52 is designed for use with up to six 'H61 expanders.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS [†]	SERIES 54 SERIES 74						SERIES 54H SERIES 74H			UNIT
			'23			'50, '53			'H50, 'H52, 'H53, 'H55			
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage	1, 2		2			2			2		V	
V_{IL} Low-level input voltage	1, 2			0.8		0.8				0.8	V	
V_{IK} Input clamp voltage	3	$V_{CC} = \text{MIN}, I_I = \S$		-1.5		-1.5				-1.5	V	
V_{OH} High-level output voltage	1	$V_{CC} = \text{MIN}, V_I = \blacktriangle, I_{OH} = \text{MAX}$	2.4	3.4		2.4	3.4		2.4	3.4	V	
V_{OL} Low-level output voltage	2	$V_{CC} = \text{MIN}, V_I = \blacktriangle, I_{OL} = \text{MAX}$	0.2	0.4		0.2	0.4		0.2	0.4	V	
I_I Input current at maximum input voltage	4	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1		1			1		mA	
I_{IH} High-level input current	Data input	$V_{CC} = \text{MAX}, V_{IH} = 2.4 \text{ V}$		40		40			50		μ A	
	Strobe of '23			160								
I_{IL} Low-level input current	Data inputs	$V_{CC} = \text{MAX}, V_{IL} = 0.4 \text{ V}$		-1.6		-1.6			-2		mA	
	Strobe of '23			-6.4								
I_{OS} Short-circuit output current [♦]		$V_{CC} = \text{MAX}$	54 Family	-20	-55	-20	-55	-40	-100		mA	
			74 Family	-18	-55	-18	-55	-40	-100			
I_{CC} Supply current	7	$V_{CC} = \text{MAX}$									mA	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

[§] $I_I = -12 \text{ mA}$ for SN54'/SN74' and -8 mA for SN54H'/SN74H'.

[♦]The input voltage is $V_{IH} = 2 \text{ V}$ or $V_{IL} = V_{IL \text{ max}}$, as appropriate. See tables with test figures 1 and 2.

[♦]Not more than one output should be shorted at a time, and for the SN54H'/SN74H', duration of short-circuit should not exceed one second.

electrical characteristics using expander inputs, $V_{CC} = \text{MIN}$, $T_A = \text{MIN}$ (unless otherwise noted)

TYPE	$I_{\bar{X}}$ (mA) (I_X for 'H52) Expander current			$V_{BE(Q)}$ (V) Base-emitter voltage of output transistor Q			V_{OH} (V) High-level output voltage			V_{OL} (V) Low-level output voltage		
	TEST CONDITIONS	MIN	TYP [‡] MAX	TEST CONDITIONS	MIN	TYP [‡] MAX	TEST CONDITIONS	MIN	TYP [‡] MAX	TEST CONDITIONS	MIN	TYP [‡] MAX
SN5423	$V_{\bar{X}} = 0.4 \text{ V}$,		-3.5	$I_X + I_{\bar{X}} = 410 \mu\text{A}$, $R_{\bar{X}X} = 0$, $I_{OL} = 16 \text{ mA}$, See Figure 11		1.1	$I_X = 150 \mu\text{A}$, $I_{\bar{X}} = -150 \mu\text{A}$, $I_{OH} = -400 \mu\text{A}$, See Figure 12	2.4	3.4	$I_X + I_{\bar{X}} = 300 \mu\text{A}$, $R_{\bar{X}X} = 138 \Omega$, $I_{OL} = 16 \text{ mA}$, See Figure 11	0.2	0.4
SN5450	$I_{OL} = 16 \text{ mA}$,		-2.9									
SN5453	See Figure 10		-2.9									
SN7423	$V_{\bar{X}} = 0.4 \text{ V}$,		-3.5	$I_X + I_{\bar{X}} = 620 \mu\text{A}$, $R_{\bar{X}X} = 0$, $I_{OL} = 16 \text{ mA}$, See Figure 11		1	$I_X = 270 \mu\text{A}$, $I_{\bar{X}} = -270 \mu\text{A}$, $I_{OH} = -400 \mu\text{A}$, See Figure 12	2.4	3.4	$I_X + I_{\bar{X}} = 430 \mu\text{A}$, $R_{\bar{X}X} = 130 \Omega$, $I_{OL} = 16 \text{ mA}$, See Figure 11	0.2	0.4
SN7450	$I_{OL} = 16 \text{ mA}$,		-3.1									
SN7453	See Figure 10		-3.1									
SN54H50, SN54H53, SN54H55	$V_{\bar{X}} = 1.4 \text{ V}$, $I_X = 0$, $I_{OL} = 0$, See Figure 10		-5.85	$I_X + I_{\bar{X}} = 700 \mu\text{A}$, $R_{\bar{X}X} = 0$, $I_{OL} = 20 \text{ mA}$, See Figure 11		1.1	$I_X = 320 \mu\text{A}$, $I_{\bar{X}} = -320 \mu\text{A}$, $I_{OH} = -500 \mu\text{A}$, See Figure 12	2.4	3.4	$I_X + I_{\bar{X}} = 470 \mu\text{A}$, $R_{\bar{X}X} = 68 \Omega$, $I_{OL} = 20 \text{ mA}$, See Figure 11	0.2	0.4
SN74H50, SN74H53, SN74H55	$V_{\bar{X}} = 1.4 \text{ V}$, $I_X = 0$, $I_{OL} = 0$, See Figure 10		-6.3									
SN54H52 SN74H52	$V_X = 1 \text{ V}$, $I_{OH} = -500 \mu\text{A}$, See Figure 13	-2.7	-4.5						2.4		3.4	$I_X = -300 \mu\text{A}$, $I_{OL} = 20 \text{ mA}$, $T_A = \text{MAX}$, See Figure 14
		-2.9	-5.35									

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

 supply current[¶]

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	
'23	8	16	10	19	4.5
'50	4	8	7.4	14	2.85
'53	4	8	5.1	9.5	4.55
'H50	8.2	12.8	15.2	24	5.85
'H52	20	31	15.2	24	17.6
'H53	7.1	11	9.4	14	8.25
'H55	4.5	6.4	7.5	12	6.00

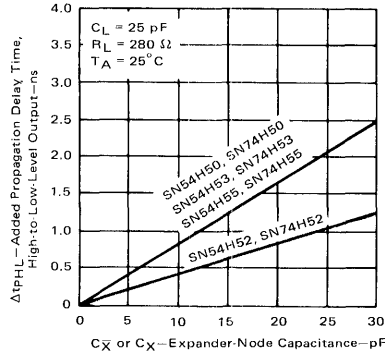
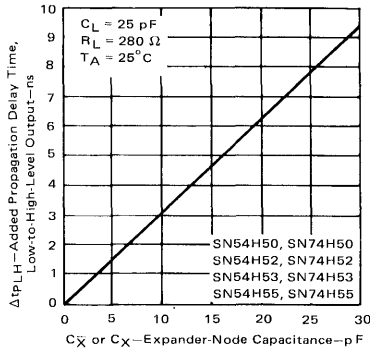
[¶]Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A ; typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

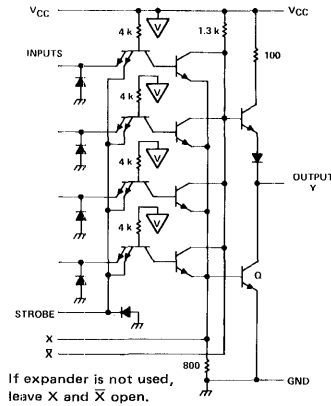
TYPE	TEST CONDITIONS#	t_{PLH} (ns)		t_{PHL} (ns)	
		Propagation delay time, low-to-high-level output		Propagation delay time, high-to-low-level output	
		TYP	MAX	TYP	MAX
'23, '50, '53	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$, Expander pins open	13	22	8	15
'50	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$, From input of '60 expander	15	30	10	20
'H50	$C_L = 25\text{ pF}$, $R_L = 280\ \Omega$, Expander pins open	6.8	11	6.2	11
'H52		10.6	15	9.2	15
'H53		7	11	6.2	11
'H55		7	11	6.5	11
'H50		$C_L = 25\text{ pF}$, $R_L = 280\ \Omega$,	11		7.4
'H52	$C = 15\text{ pF}$ (GND to X of	14.8		9.8	
'H53	'H50, 'H53, or 'H55; or	11.4		7.4	
'H55	to X of 'H52)	11.4		7.7	

#Load circuit and voltage waveforms are shown on page 3-10.

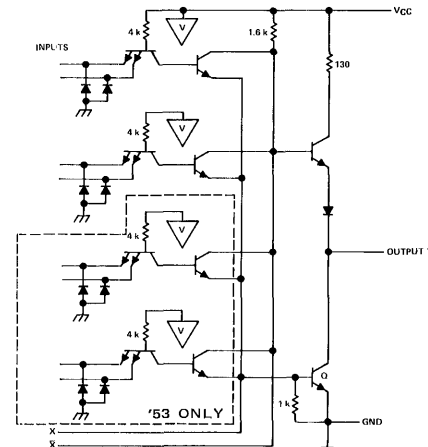
TYPICAL ADDED PROPAGATION DELAY TIME vs EXPANDER-NODE CAPACITANCE



schematics (each gate)



'23 CIRCUITS

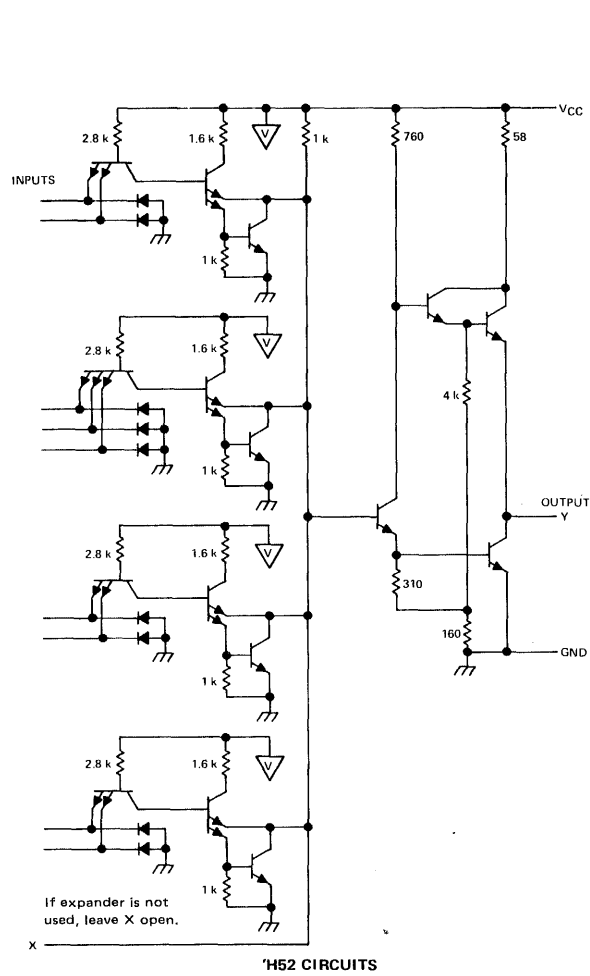


'50, '53 CIRCUITS

Resistor values shown are nominal and in ohms.

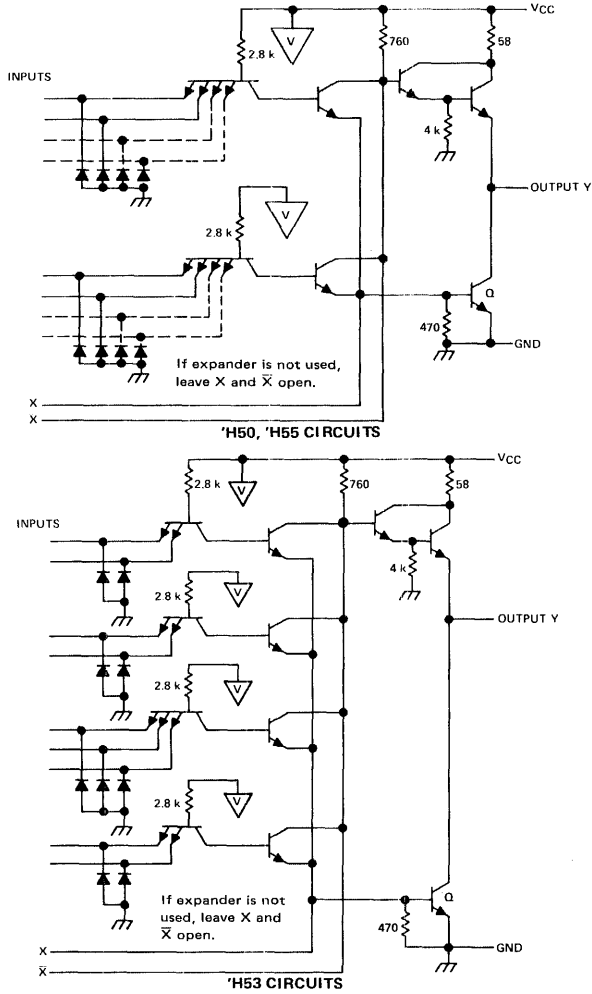
EXPANDABLE GATES

EXPANDABLE GATES



Resistor values shown are nominal and in ohms.

6



6-42

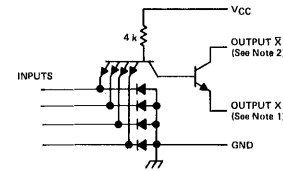
TEXAS INSTRUMENTS
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recommended operating conditions

	SN5460			SN7460			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	-55		125	0		70	°C

The '23, '50, and '53 are designed for use with up to four '60 expanders.

schematic (each gate)



'60 CIRCUITS

- NOTES: 1. Connect to X input of '23, '50, or '53 circuit.
2. Connect to X input of '23, '50, or '53 circuit.

Resistor value shown is nominal and in ohms.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	SN5460			SN7460			UNIT				
		TEST CONDITIONS			MIN	TYP [‡]	MAX		TEST CONDITIONS			MIN
V_{IH} High-level input voltage	15			2				2				V
V_{IL} Low-level input voltage	16					0.8					0.8	V
$V_{XX(on)}$ On-state voltage between expander outputs	15	$V_{CC} = 4.5\text{ V}$, $V_{IH} = 2\text{ V}$, $V_X = 1.1\text{ V}$, $I_{\bar{X}} = 3.5\text{ mA}$, $T_A = -55^\circ\text{C}$			0.4			$V_{CC} = 4.75\text{ V}$, $V_{IH} = 2\text{ V}$, $V_X = 1\text{ V}$, $I_{\bar{X}} = 3.5\text{ mA}$, $T_A = 0^\circ\text{C}$			0.4	V
$I_{X(on)}$ On-state expander current	15	$V_{CC} = 4.5\text{ V}$, $V_{IH} = 2\text{ V}$, $V_X = 1.1\text{ V}$, $I_{\bar{X}} = 0$, $T_A = -55^\circ\text{C}$		-0.3				$V_{CC} = 4.75\text{ V}$, $V_{IH} = 2\text{ V}$, $V_X = 1\text{ V}$, $I_{\bar{X}} = 0$, $T_A = 0^\circ\text{C}$		-0.43		mA
$I_{\bar{X}(off)}$ Off-state expander current	16	$V_{CC} = 4.5\text{ V}$, $V_{IL} = 0.8\text{ V}$, $V_{\bar{X}} = 4.5\text{ V}$, $R_X = 1.2\text{ k}\Omega$, $T_A = -55^\circ\text{C}$				150		$V_{CC} = 4.75\text{ V}$, $V_{IL} = 0.8\text{ V}$, $V_{\bar{X}} = 4.5\text{ V}$, $R_X = 1.2\text{ k}\Omega$, $T_A = 0^\circ\text{C}$			270	μA
I_I Input current at maximum input voltage	4	$V_{CC} = 5.5\text{ V}$, $V_I = 5.5\text{ V}$			1			$V_{CC} = 5.25\text{ V}$, $V_I = 5.5\text{ V}$			1	mA
I_{IH} High-level input current	4	$V_{CC} = 5.5\text{ V}$, $V_I = 2.4\text{ V}$			40			$V_{CC} = 5.25\text{ V}$, $V_I = 2.4\text{ V}$			40	μA
I_{IL} Low-level input current	5	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$			-1.6			$V_{CC} = 5.25\text{ V}$, $V_I = 0.4\text{ V}$			-1.6	mA
$I_{CC(on)}$ Supply current, expander on	7	$V_{CC} = 5.5\text{ V}$, $V_I = 4.5\text{ V}$, $V_X = 0.85\text{ V}$, $I_{\bar{X}} = 0$		1.2	2.5			$V_{CC} = 5.25\text{ V}$, $V_I = 4.5\text{ V}$, $V_X = 0.85\text{ V}$, $I_{\bar{X}} = 0$		1.2	2.5	mA
$I_{CC(off)}$ Supply current, expander off	7	$V_{CC} = 5.5\text{ V}$, $V_I = 0$, $V_X = 0.85\text{ V}$, $I_{\bar{X}} = 0$		2	4			$V_{CC} = 5.25\text{ V}$, $V_I = 0$, $V_X = 0.85\text{ V}$, $I_{\bar{X}} = 0$		2	4	mA

[‡]All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

recommended operating conditions

	SN54H60 SN54H62			SN74H60 SN74H62			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	-55		125	0		70	°C

See schematics
next page

The 'H50, 'H53, and 'H55 are designed for use with up to four 'H60 expanders or one 'H62 expander.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	SN54H60, SN54H62			SN74H60, SN74H62			UNIT		
		TEST CONDITIONS			TEST CONDITIONS					
V_{IH} High-level input voltage	15	2			2			V		
V_{IL} Low-level input voltage	16	0.8			0.8			V		
$V_{XX(on)}$ On-state voltage between expander outputs	15	$V_{CC} = 4.5\text{ V}$, $V_{IH} = 2\text{ V}$, $V_X = 1.1\text{ V}$, $I_{\bar{X}} = 5.85\text{ mA}$, $T_A = -55^\circ\text{C}$			$V_{CC} = 4.75\text{ V}$, $V_{IH} = 2\text{ V}$, $V_X = 1\text{ V}$, $I_{\bar{X}} = 6.3\text{ mA}$, $T_A = 0^\circ\text{C}$			V		
		$V_{CC} = 5.5\text{ V}$, $V_{IH} = 2\text{ V}$, $V_X = 1\text{ V}$, $I_{\bar{X}} = 7.85\text{ mA}$, $T_A = 125^\circ\text{C}$			$V_{CC} = 5.25\text{ V}$, $V_{IH} = 2\text{ V}$, $V_X = 1\text{ V}$, $I_{\bar{X}} = 7.4\text{ mA}$, $T_A = 70^\circ\text{C}$					
$I_{X(on)}$ On-state expander current	15	$V_{CC} = 4.5\text{ V}$, $V_{IH} = 2\text{ V}$, $V_X = 1.1\text{ V}$, $I_{\bar{X}} = 0$, $T_A = -55^\circ\text{C}$			-470	$V_{CC} = 4.75\text{ V}$, $V_{IH} = 2\text{ V}$, $V_X = 1\text{ V}$, $I_{\bar{X}} = 0$, $T_A = 0^\circ\text{C}$		-600	μA	
$I_{\bar{X}(off)}$ Off-state expander current	16	$V_{CC} = 4.5\text{ V}$, $V_{IL} = 0.8\text{ V}$, $V_{\bar{X}} = 4.5\text{ V}$, $R_X = 575\ \Omega$, $T_A = -55^\circ\text{C}$			320			570	μA	
I_I Input current at maximum input voltage	4	$V_{CC} = 5.5\text{ V}$, $V_I = 5.5\text{ V}$			1			1	mA	
I_{IH} High-level input current	4	$V_{CC} = 5.5\text{ V}$, $V_I = 2.4\text{ V}$			50			50	μA	
I_{IL} Low-level input current	5	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$			-2			-2	mA	
$I_{CC(on)}$ Supply current, expander on	'H60	$V_{CC} = 5.5\text{ V}$, $V_I = 4.5\text{ V}$, $V_X = 0.85\text{ V}$, $I_{\bar{X}} = 0$			1.9	3.5	$V_{CC} = 5.25\text{ V}$, $V_I = 4.5\text{ V}$, $V_X = 0.85\text{ V}$, $I_{\bar{X}} = 0$		1.9	3.5
	'H62				3.8	7			3.8	7
$I_{CC(off)}$ Supply current, expander off	'H60	$V_{CC} = 5.5\text{ V}$, $V_I = 0$, $V_X = 0.85\text{ V}$, $I_{\bar{X}} = 0$			3	4.5	$V_{CC} = 5.25\text{ V}$, $V_I = 0$, $V_X = 0.85\text{ V}$, $I_{\bar{X}} = 0$		3	4.5
	'H62				6	9			6	9
$C_{\bar{X}}$ Expander output capacitance	'H60	V_{CC} , inputs, and X open; $f = 1\text{ MHz}$			5.4			5.4	pF	
	'H62				6.0			6.0		

‡ All typical values are at $V_{CC} = 5\text{ V}$ (except $C_{\bar{X}}$), $T_A = 25^\circ\text{C}$.

recommended operating conditions

	SN54H61			SN74H61			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	-55		125	0		70	°C

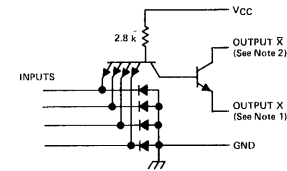
The 'H52 is designed for use with up to six 'H61 expanders.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

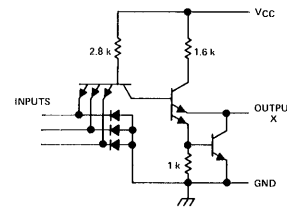
PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP [‡]	MAX	UNIT
V_{IH} High-level input voltage	17		2			V
V_{IL} Low-level input voltage	18				0.8	V
$V_{X(on)}$ On-state expander-output voltage	17	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_X = 4.5 \text{ mA}$ for SN54H61, 5.35 mA for SN74H61, $T_A = \text{MIN}$			1	V
$I_{X(off)}$ Off-state expander current	18	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, V_X = 2.2 \text{ V}, T_A = \text{MAX}$			50	μA
I_I Input current at maximum input voltage	4	$V_{CC} = 5.5 \text{ V}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	4	$V_{CC} = 5.5 \text{ V}, V_I = 2.4 \text{ V}$			50	μA
I_{IL} Low-level input current	5	$V_{CC} = 5.5 \text{ V}, V_I = 0.4 \text{ V}$			-2	mA
$I_{CC(on)}$ Supply current, expander on	7	$V_{CC} = 5.5 \text{ V}, V_I = 4.5 \text{ V}$		11	16	mA
$I_{CC(off)}$ Supply current, expander off	7	$V_{CC} = 5.5 \text{ V}, V_I = 0$		5	7	mA
C_X Expander output capacitance		V_{CC} and inputs open, $f = 1 \text{ MHz}$		5.4		pF

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡]All typical values are at $V_{CC} = 5 \text{ V}$ (except C_X), $T_A = 25^\circ\text{C}$.

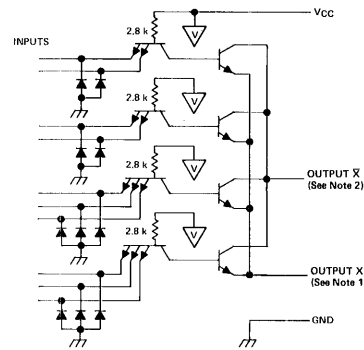
schematics (each gate)



'H60 CIRCUITS



'H61 CIRCUITS



'H62 CIRCUITS

- NOTES: 1. Connect to X input of 'H50, 'H53, or 'H55 circuit.
2. Connect to \bar{X} input of 'H50, 'H53, or 'H55 circuit.

Resistor values shown are nominal and in ohms.

recommended operating conditions

	SERIES 54/74	'70			'72, '73, '76, '107			'74			'109			'110			'111			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	Series 54	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	Series 74	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I _{OH}		-400			-400			-400			-800			-800			-800			μA
Low-level output current, I _{OL}		16			16			16			16			16			16			mA
Pulse width, t _w	Clock high	20			20			30			20			25			25			ns
	Clock low	30			47			37			20			25			25			
	Preset or clear low	25			25			30			20			25			25			
Input setup time, t _{su}		20†			0†			20†			10†			20†			0†			ns
Input hold time, t _h		5†			0‡			5†			6†			5†			30†			ns
Operating free-air temperature, T _A	Series 54	-55	125		-55	125		-55	125		-55	125		-55	125		-55	125		°C
	Series 74	0	70		0	70		0	70		0	70		0	70		0	70		

† The arrow indicates the edge of the clock pulse used for reference: † for the rising edge, ‡ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'70		'72, '73, '76, '107		'74		'109		'110		'111		UNIT
		MIN	TYP‡ MAX	MIN	TYP‡ MAX	MIN	TYP‡ MAX	MIN	TYP‡ MAX	MIN	TYP‡ MAX	MIN	TYP‡ MAX	
V _{IH} High-level input voltage		2		2		2		2		2		2		V
V _{IL} Low-level input voltage		0.8		0.8		0.8		0.8		0.8		0.8		V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -12 mA	-1.5		-1.5		-1.5		-1.5		-1.5		-1.5		V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = MAX	2.4	3.4	2.4	3.4	2.4	3.4	2.4	3.4	2.4	3.4	2.4	3.4	V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA	0.2	0.4	0.2	0.4	0.2	0.4	0.2	0.4	0.2	0.4	0.2	0.4	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V	1		1		1		1		1		1		mA
I _{IH} High-level input current	D, J, K, or K	40		40		40		40		40		40		μA
	Clear	80		80		120		160		160		80		
	Preset	80		80		80		80		160		80		
	Clock	40		80		80		80		40		120		
I _{IL} Low-level input current	D, J, K, or K	-1.6		-1.6		-1.6		-1.6		-1.6		-1.6		mA
	Clear *	-3.2		-3.2		-3.2		-4.8		-3.2		-3.2		
	Preset *	-3.2		-3.2		-1.6		-3.2		-3.2		-3.2		
	Clock	-1.6		-3.2		-3.2		-3.2		-1.6		-4.8		
I _{OS} Short-circuit output current*	Series 54	-20	-57	-20	-57	-20	-57	-30	-85	-20	-57	-20	-57	mA
	Series 74	-18	-57	-18	-57	-18	-57	-30	-85	-18	-57	-18	-57	
I _{CC} Supply current (Average per flip-flop)	V _{CC} = MAX, See Note 1	13	26	10	20	8.5	15	9	15	20	34	14	20.5	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

* Not more than one output should be shorted at a time.

* Clear is tested with preset high and preset is tested with clear high.

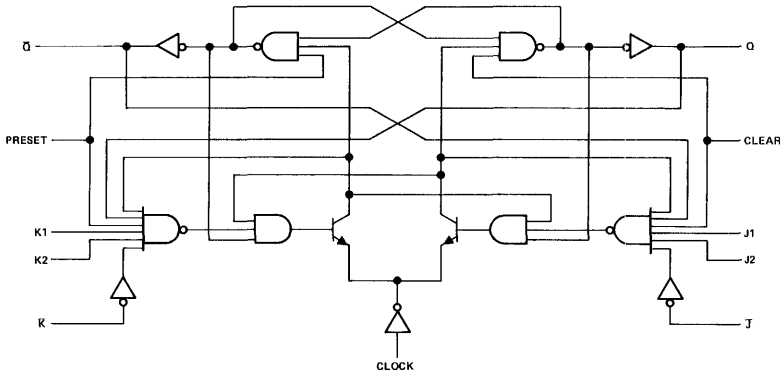
NOTE 1: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is at 4.5 V for the '70, '110, and '111; and is grounded for all the others.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

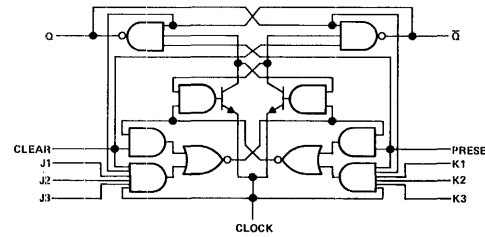
PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'70			'72, '73 '76, '107			'74			'109			'110			'111			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$, See Note 2	20	35		15	20		15	25		25	33		20	25		20	25	MHz	
t_{PLH}	Preset	Q				50		16	25			25		10	15		12	20		12	18	ns
t_{PHL}	(as applicable)	\bar{Q}				50		25	40			40		23	35		18	25		21	30	ns
t_{PLH}	Clear	\bar{Q}				50		16	25			25		10	15		12	20		12	18	ns
t_{PHL}	(as applicable)	Q				50		25	40			40		17	25		18	25		21	30	ns
t_{PLH}	Clock	Q or \bar{Q}				27		16	25			14		10	16		20	30		12	17	ns
t_{PHL}							18		25	40			20		18	28		13	20		20	30

[†] f_{max} = maximum clock frequency; t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output.
NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

functional block diagrams



'70-GATED J-K WITH CLEAR AND PRESET

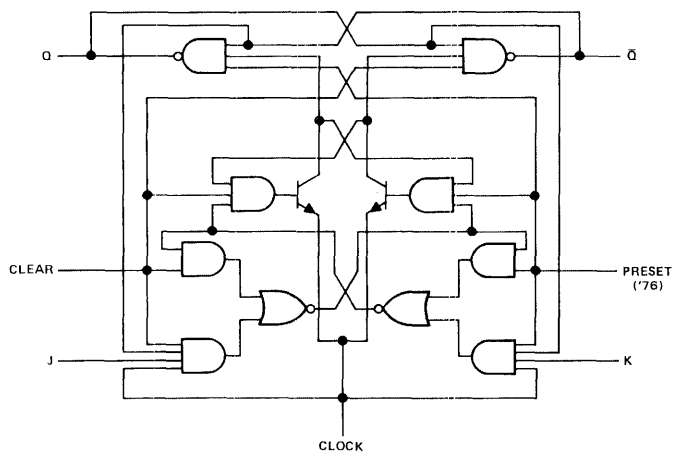


'72-GATED J-K WITH CLEAR AND PRESET

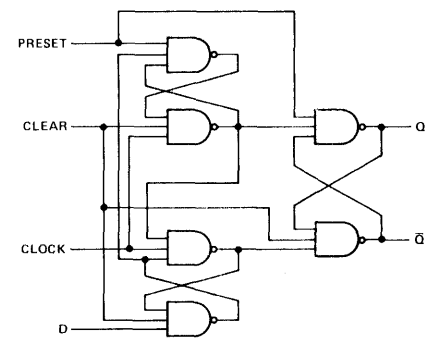
See following pages for:
'73-DUAL J-K WITH CLEAR
'74-DUAL D WITH CLEAR AND PRESET
'76-DUAL J-K WITH CLEAR AND PRESET
'107-DUAL J-K WITH CLEAR

'109-DUAL J-K WITH CLEAR AND PRESET
'110-GATED J-K WITH CLEAR AND PRESET
'111-DUAL J-K WITH CLEAR AND PRESET

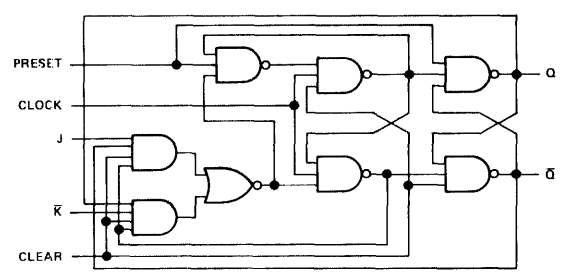
functional block diagrams (continued)



'73-DUAL J-K WITH CLEAR
'76-DUAL J-K WITH CLEAR AND PRESET
'107-DUAL J-K WITH CLEAR

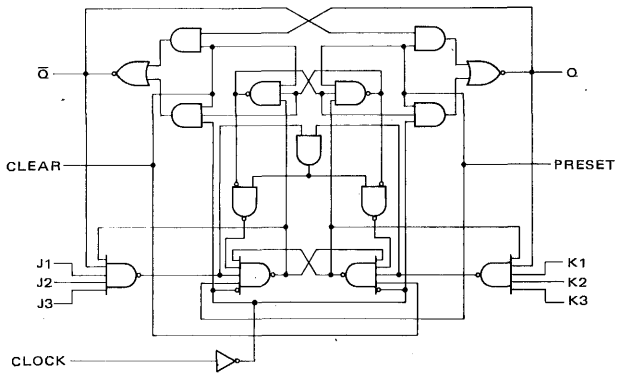


'74-DUAL D WITH CLEAR AND PRESET

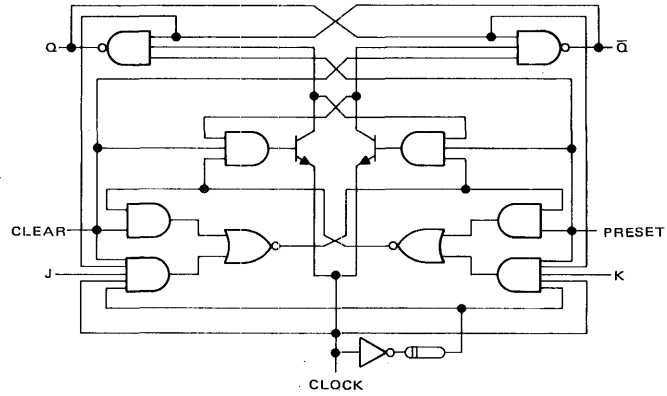


'109-DUAL J-K̄ WITH CLEAR AND PRESET

functional block diagrams (continued)

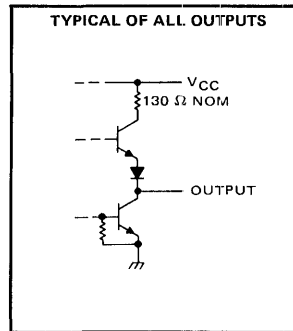
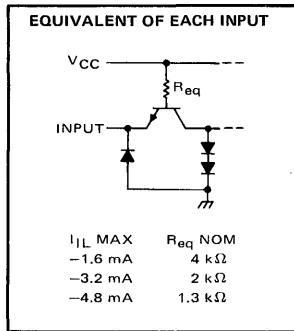


'110-GATED J-K WITH CLEAR AND PRESET



'111-DUAL J-K WITH CLEAR AND PRESET

schematics of inputs and outputs



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recommended operating conditions

	SERIES 54H/74H	'H71			'H72, 'H73, 'H76			'H74			'H78			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	Series 54H	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	Series 74H	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I _{OH}		-500			-500			-1000			-500			μA
Low-level output current, I _{OL}		20			20			20			20			mA
Pulse width, t _w	Clock high	12			12			15			12			ns
	Clock low	28			28			13.5			28			
	Clear or preset low	16			16			25			16			
Setup time, t _{su}	High-level data	0†			0†			10†			0†			ns
	Low-level data	0†			0†			15†			0†			
Hold time, t _h		0‡			0‡			5†			0‡			ns
Operating free-air temperature, T _A	Series 54H	-55	125		-55	125		-55	125		-55	125	°C	
	Series 74H	0	70		0	70		0	70		0	70		

† ‡ The arrow indicates the edge of the clock pulse used for reference: † for the rising edge, ‡ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'H71		'H72, 'H73, 'H76		'H74		'H78		UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	
V _{IH} High-level input voltage		2		2		2		2		V
V _{IL} Low-level input voltage		0.8		0.8		0.8		0.8		V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -8 mA	-1.5		-1.5		-1.5		-1.5		V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = MAX	2.4	3.4	2.4	3.4	2.4	3.4	2.4	3.4	V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA	0.2	0.4	0.2	0.4	0.2	0.4	0.2	0.4	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V	1		1		1		1		mA
I _{IH} High-level input current	D, J, or K	50		50		50		50		μA
	Clear	150		100		150		200		
	Preset	150		100		100		100		
	Clock	100		50		100		100		
I _{IL} Low-level input current	D, J, or K	-2		-2		-2		-2		mA
	Clear *	-4		-4		-4		-8		
	Preset *	-6		-4		-2		-4		
	Clock	-4		-2		-4		-4		
I _{OS} Short-circuit output current*	V _{CC} = MAX	-40	-100	-40	-100	-40	-100	-40	-100	mA
I _{CC} (Average per flip-flop)	Supply current	19 30		16 25		15 21		16 25		mA
	See Note 1	19 30		16 25		15 25		16 25		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

*Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

*Clear is tested with preset high and preset is tested with clear high.

NOTE 1: With all outputs open, I_{CC} is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

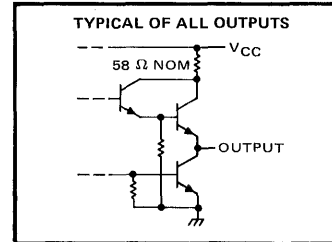
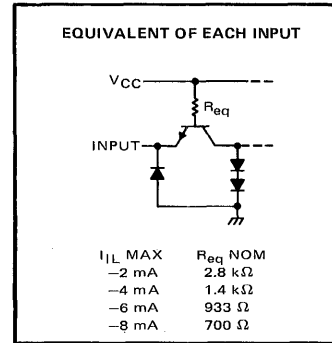
switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{ C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'H71, 'H72, 'H73, 'H76, 'H78			'H74			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			$C_L = 25\text{ pF}$, $R_L = 280\ \Omega$, See Note 2	25	30		35	43		MHz
t_{PLH}	Preset	Q		6	13			20		ns
t_{PHL}	(as applicable)	\bar{Q}		12	24			30		ns
t_{PLH}	Clear	\bar{Q}		6	13			20		ns
t_{PHL}	(as applicable)	Q		12	24			30		ns
t_{PLH}	Clock	Q or \bar{Q}		14	21			8.5	15	
t_{PHL}				22	27			13	20	

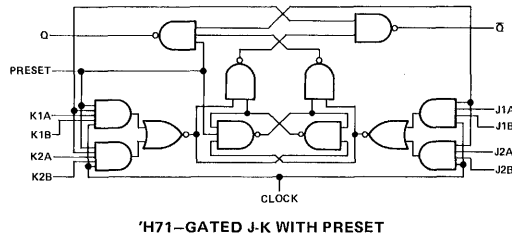
[†] f_{max} = maximum clock frequency; t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output.

NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

schematics of input and outputs

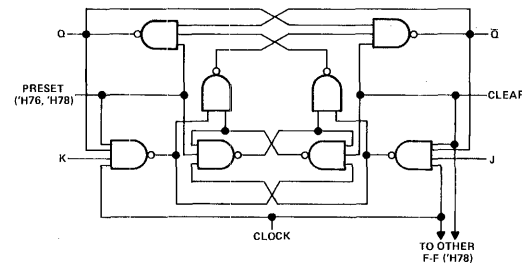
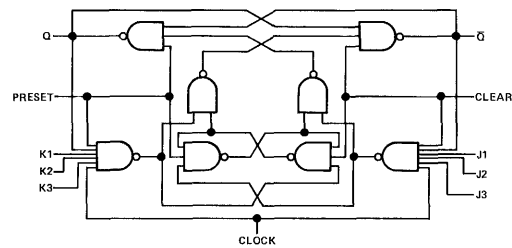


functional block diagrams



Same functional block diagram as for '74, see page 122.

'H74-DUAL D WITH CLEAR AND PRESET



SERIES 54H/74H PULSE-TRIGGERED J-K AND EDGE-TRIGGERED D-TYPE FLIP-FLOPS

recommended operating conditions

		SERIES 54H/74H	'H101			'H102, 'H106			'H103			'H108			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Series 54H	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V	
	Series 74H	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25		
High-level output current, I_{OH}			-500			-500			-500			-500			μ A
Low-level output current, I_{OL}			20			20			20			20			mA
Pulse width, t_w	Clock high		10			10			10			10			ns
	Clock low		15			15			15			15			
	Clear or preset low		16			16			16			16			
Setup time, t_{su}	High-level data		10 \downarrow			10 \downarrow			10 \downarrow			10 \downarrow			ns
	Low-level data		13 \downarrow			13 \downarrow			13 \downarrow			13 \downarrow			
Hold time, t_h			0 \downarrow			0 \downarrow			0 \downarrow			0 \downarrow			ns
Operating free-air temperature, T_A		Series 54H	-55	125		-55	125		-55	125		-55	125		$^{\circ}$ C
		Series 74H	0	70		0	70		0	70		0	70		

\downarrow The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	'H101		'H102, 'H106		'H103		'H108		UNIT		
			MIN	TYP [‡] MAX	MIN	TYP [‡] MAX	MIN	TYP [‡] MAX	MIN	TYP [‡] MAX			
V_{IH}	High-level input voltage		2		2		2		2		V		
V_{IL}	Low-level input voltage			0.8		0.8		0.8		0.8	V		
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -8 \text{ mA}$		-1.5		-1.5		-1.5		-1.5	V		
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -500 \mu\text{A}$	2.4	3.4	2.4	3.4	2.4	3.4	2.4	3.4	V		
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$	0.2	0.4	0.2	0.4	0.2	0.4	0.2	0.4	V		
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1		1		1		1	mA		
I_{IH}	High-level input current	Any J or K		50		50		50		50	μ A		
		Clear	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$		100		100		100	200			
		Preset		100	100	100	100						
		Clock		0	-1	0	-1	0	-1	0		-1	
I_{IL}	Low-level input current	Any J or K			-1	-2	-1	-2	-1	-2	-1	-2	mA
		Clear	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-1	-2	-1	-2	-1	-2	-2	-4	
		Preset		-1	-2	-1	-2	-1	-2	-1	-2		
		Clock		-3	-4.8	-3	-4.8	-3	-4.8	-6	-9.6		
I_{OS}	Short-circuit output current [♦]	$V_{CC} = \text{MAX}$		-40	-100	-40	-100	-40	-100	-40	-100	mA	
I_{CC}	Supply current (Average per flip-flop)	$V_{CC} = \text{MAX}, \text{ See Note 1}$		20	38		20	38		20	38	mA	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

[♦]Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.

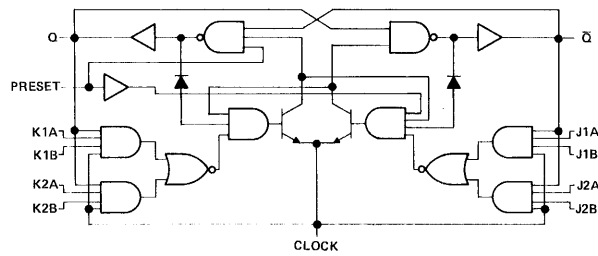
NOTE 1: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

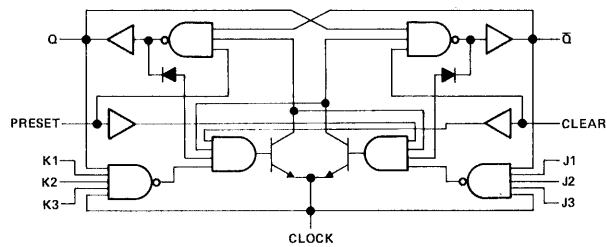
PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				40	50		MHz
t_{PLH}	Preset or clear	Q or \bar{Q}	$C_L = 25\text{ pF}$, $R_L = 280\ \Omega$, See Note 2		8	12	ns
t_{PHL}	Preset or clear (clock high)	\bar{Q} or Q			15	20	ns
	Preset or clear (clock low)				23	35	ns
t_{PLH}	Clock	Q or \bar{Q}			10	15	ns
t_{PHL}				16	20		ns

† f_{max} ≡ maximum clock frequency
 t_{PLH} ≡ propagation delay time, low-to-high-level output
 t_{PHL} ≡ propagation delay time, high-to-low-level output
 NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

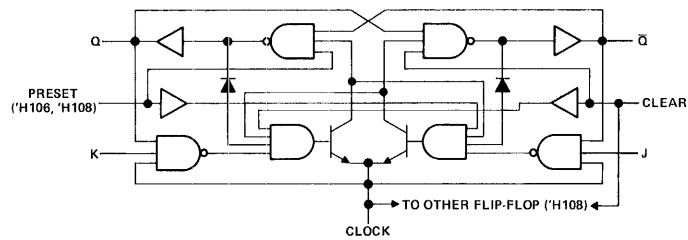
functional block diagrams



'H101-GATED J-K WITH PRESET

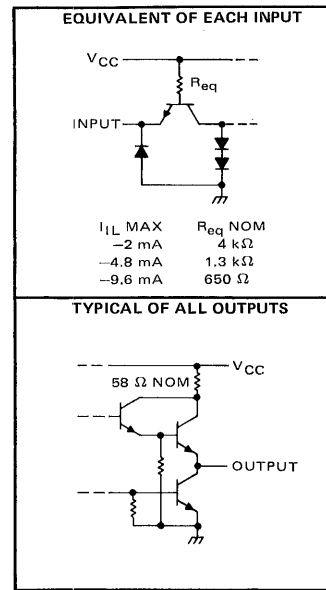


'H102-GATED J-K WITH CLEAR AND PRESET



'H103-DUAL J-K WITH CLEAR
 'H106-DUAL J-K WITH CLEAR AND PRESET
 'H108-DUAL J-K WITH PRESET, COMMON CLEAR,
 AND COMMON CLOCK

schematics of inputs and outputs



recommended operating conditions

	SERIES 54L/74L	'L71			'L72, 'L73			'L74			'L78			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	Series 54L	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	Series 74L	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I _{OH}	Series 54L	-100			-100			-100			-100			μA
	Series 74L	-200			-200			-200			-200			
Low-level output current, I _{OL}	Series 54L	2			2			2			2			mA
	Series 74L	3.6			3.6			3.6			3.6			
Pulse width, t _w	Clock high	200			200			200			200			ns
	Clock low	200			200			200			200			
	Clear or preset low	100			100			100			100			
Setup time, t _{su}		0†			0†			50†			0†			ns
Hold time, t _h		0‡			0‡			15†			0‡			ns
Operating free-air temperature, T _A	Series 54L	-55	125		-55	125		-55	125		-55	125		°C
	Series 74L	0	70		0	70		0	70		0	70		

† The arrow indicates the edge of the clock pulse used for reference: † for the rising edge, ‡ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'L71		'L72, 'L73		'L74		'L78		UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	
V _{IH} High-level input voltage		2		2		2		2		V
V _{IL} Low-level input voltage	Clock input	0.6		0.6		0.7		0.6		V
	All other inputs	0.7		0.7		0.7		0.7		
V _{OH} High-level output voltage	Series 54L	V _{CC} = MIN, V _{IH} = 2 V,		2.4 3.3		2.4 3.3		2.4 3.3		V
	Series 74L	V _{IL} = V _{IL} max, I _{OH} = MAX		2.4 3.2		2.4 3.2		2.4 3.2		
V _{OL} Low-level output voltage	Series 54L	V _{CC} = MIN, V _{IH} = 2 V,		0.15 0.3		0.15 0.3		0.15 0.3		V
	Series 74L	V _{IL} = V _{IL} max, I _{OL} = MAX		0.2 0.4		0.2 0.4		0.2 0.4		
I _I Input current at maximum input voltage	R, S, J, K, or D	100		100		100		100		μA
	Clear	200		200		300		400		
	Preset	200		200		200		200		
	Clock	200		200		200		400		
I _{IH} High-level input current	R, S, J, K, or D	10		10		10		10		μA
	Clear	20		20		30		40		
	Preset	20		20		20		20		
	Clock	-200		-200		20		-400		
I _{IL} Low-level input current	R, S, J, K, or D	-0.18		-0.18		-0.18		-0.18		mA
	Clear	-0.36		-0.36		-0.36		-0.72		
	Preset	-0.36		-0.36		-0.18		-0.36		
	Clock	-0.36		-0.36		-0.36		-0.72		
I _{OS} Short-circuit output current	V _{CC} = MAX	-3	-15	-3	-15	-3	-15	-3	-15	mA
I _{CC} Supply current (Average per flip-flop)	V _{CC} = MAX, See Note 1	0.76	1.44	0.76	1.44	0.8	1.5	0.76	1.44	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

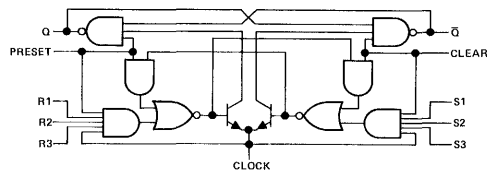
NOTE 1: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

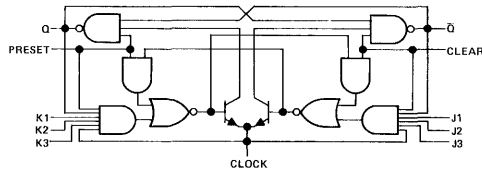
PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'L71, 'L72, 'L73, 'L78			'L74			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			$C_L = 50\text{ pF}$, $R_L = 4\text{ k}\Omega$, See Note 2	2.5	3		2.5	3		MHz
t_{PLH}	Preset or clear	Q or \bar{Q}		35	75		50	75		ns
t_{PHL}	Preset or clear (clock high)	\bar{Q} or Q		60	150		80	150		ns
	Preset or clear (clock low)			200		80	150			
t_{PLH}	Clock	Q or \bar{Q}		10	35	75	15	65	100	ns
t_{PHL}				10	60	150	15	65	150	

[†] f_{max} = maximum clock frequency
 t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output
 NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

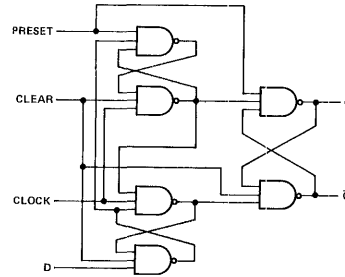
functional block diagrams



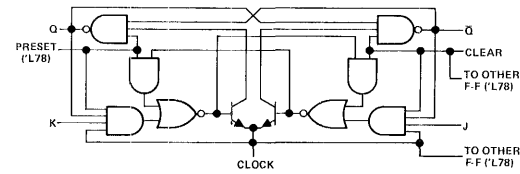
'L71-GATED R-S WITH CLEAR AND PRESET



'L72-GATED J-K WITH CLEAR AND PRESET

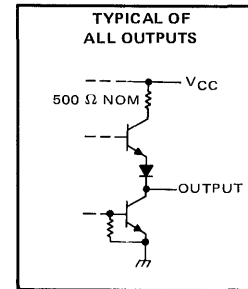
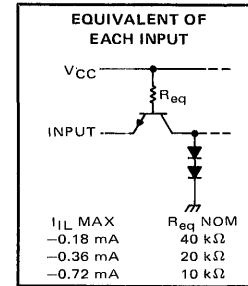


'L74-DUAL D WITH CLEAR AND PRESET



'L73-DUAL J-K WITH CLEAR
 'L78-DUAL J-K WITH PRESET, COMMON CLEAR,
 AND COMMON CLOCK

schematics of inputs and outputs



recommended operating conditions

	SERIES 54LS/74LS	'LS73, 'LS107, 'LS113			'LS74A			'LS76, 'LS112			'LS78, 'LS114			'LS109A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	Series 54LS	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	Series 74LS	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I _{OH}		-400			-400			-400			-400			-400			μA
Low-level output current, I _{OL}	Series 54LS	4			4			4			4			4			mA
	Series 74LS	8			8			8			8			8			
Clock frequency, f _{clock}		0	30	0	25	0	25	0	30	0	30	0	25	0	25	MHz	
Pulse width, t _w	Clock high	20			25			20			25			20			ns
	Preset or clear low	25			25			25			25			25			
Setup time, t _{su}	High-level data	20 ↓			25 ↑			20 ↓			20 ↓			20 ↑			ns
	Low-level data	20 ↓			20 ↑			20 ↓			20 ↓			20 ↑			
Hold time, t _h		0 ↓			5 ↑			0 ↓			0 ↓			5 ↑			ns
Operating free-air temperature, T _A	Series 54LS	-55	125	-55	125	-55	125	-55	125	-55	125	-55	125	-55	125	°C	
	Series 74LS	0	70	0	70	0	70	0	70	0	70	0	70	0	70		

↑ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'LS73, 'LS107, 'LS113			'LS74A			'LS76, 'LS112			'LS78, 'LS114			'LS109A			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IH}	High-level input voltage	2			2			2			2			2			V	
V _{IL}	Low-level input voltage	0.7			0.7			0.7			0.7			0.7			V	
	Series 54LS	0.8			0.8			0.8			0.8			0.8				
V _{IK}	Input clamp voltage	-1.5			-1.5			-1.5			-1.5			-1.5			V	
V _{OH}	High-level output voltage	2.5 3.4			2.5 3.4			2.5 3.4			2.5 3.4			2.5 3.4			V	
	Series 54LS	2.7 3.4			2.7 3.4			2.7 3.4			2.7 3.4			2.7 3.4				
V _{OL}	Low-level output voltage	0.25 0.4			0.25 0.4			0.25 0.4			0.25 0.4			0.25 0.4			V	
	Series 54LS	0.35 0.5			0.35 0.5			0.35 0.5			0.35 0.5			0.35 0.5				
I _I	Input current at maximum input voltage	D, J, K, or R		Clear		V _I = 7 V		0.1		0.1		0.1		0.1		0.1		mA
		D, J, K, or R		Preset		V _I = 7 V		0.3		0.2		0.3		0.6		0.2		
		D, J, K, or R		Clock		V _I = 7 V		0.3		0.2		0.3		0.3		0.2		
		D, J, K, or R		Clock		V _I = 7 V		0.4		0.1		0.4		0.8		0.1		
I _{IH}	High-level input current	D, J, K, or R		Clear		V _I = 2.7 V		20		20		20		20		20		μA
		D, J, K, or R		Preset		V _I = 2.7 V		60		40		60		120		40		
		D, J, K, or R		Preset		V _I = 2.7 V		60		40		60		60		40		
		D, J, K, or R		Clock		V _I = 2.7 V		80		20		80		160		20		
I _{IL}	Low-level input current	D, J, K, or R		Clear		V _I = 0.4 V		-0.4		-0.4		-0.4		-0.4		-0.4		mA
		D, J, K, or R		Preset		V _I = 0.4 V		-0.8		-0.8		-0.8		-1.6		-0.8		
		D, J, K, or R		Preset		V _I = 0.4 V		-0.8		-0.8		-0.8		-0.8		-0.8		
		D, J, K, or R		Clock		V _I = 0.4 V		-0.8		-0.4		-0.8		-1.6		-0.4		
I _{OS}	Short-circuit output current*	Series 54LS		Series 74LS		V _{CC} = MAX		-20 -100		-20 -100		-20 -100		-20 -100		mA		
I _{CC}	Supply current (Total)	Series 54LS		Series 74LS		V _{CC} = MAX, See Note 1		4 8		4 8		4 8		4 8		mA		

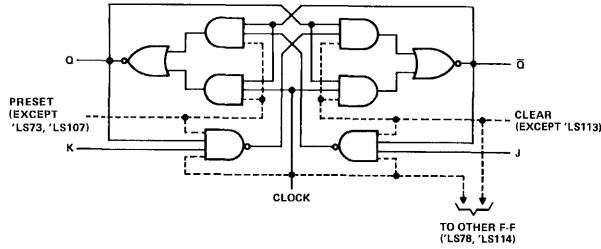
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
 ‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
 * Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.
 NOTE 1: With all outputs open, I_{CC} is measured with the Q and Q outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS73, 'LS76, 'LS78, 'LS107 'LS112, 'LS113, 'LS114			'LS74A, 'LS109A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			$C_L = 15\text{ pF}$,	30	45		25	33		MHz
t_{PLH}	Clear, preset, or	Q or \bar{Q}	$R_L = 2\text{ k}\Omega$,		11	20		13	25	ns
t_{PHL}	clock (as appropriate)		See Note 2		15	30		25	40	ns

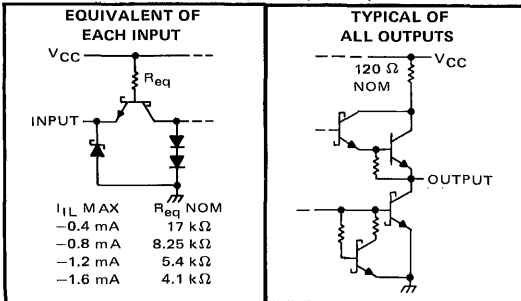
[†] f_{max} \equiv maximum clock frequency
 t_{PLH} \equiv propagation delay time, low-to-high-level output
 t_{PHL} \equiv propagation delay time, high-to-low-level output
 NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

functional block diagrams and schematics of inputs and outputs

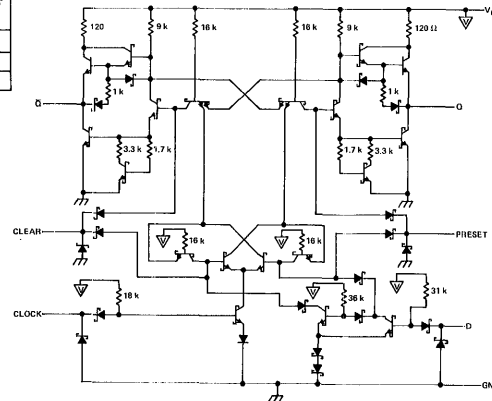


- 'LS73, 'LS107—DUAL J-K WITH CLEAR
- 'LS76, 'LS112—DUAL J-K WITH CLEAR AND PRESET
- 'LS78, 'LS114—DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK
- 'LS113—DUAL J-K WITH PRESET

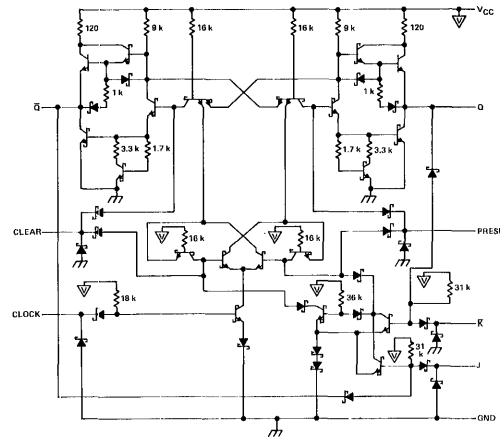
'LS73, 'LS76, 'LS78, 'LS112, 'LS113, 'LS114



schematics of 'LS74A and 'LS109A



'LS74A—DUAL D WITH CLEAR AND PRESET



'LS109A—DUAL J-K WITH CLEAR AND PRESET

SERIES 54LS/74LS FLIP-FLOPS

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recommended operating conditions

	SERIES 54S/74S	'S74			'S112			'S113			'S114			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Series 54S	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	Series 74S	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}				-1			-1			-1			-1	mA
Low-level output current, I_{OL}				20			20			20			20	mA
Pulse width, t_w	Clock high			6			6			6			6	ns
	Clock low			7.3			6.5			6.5			6.5	
	Clear or preset low			7			8			8			8	
Input setup time, t_{su}	High-level data			3†			3‡			3‡			3‡	ns
	Low-level data			3†			3‡			3‡			3‡	
Input hold time, t_h				2†			0‡			0‡			0‡	ns
Operating free-air temperature, T_A	Series 54S			-55			125			-55			125	°C
	Series 74S			0			70			0			70	

†‡ The arrow indicates the edge of the clock pulse used for reference: † for the rising edge, ‡ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'S74			'S112			'S113			'S114			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage				2			2			2			2	V
V_{IL} Low-level input voltage				0.8			0.8			0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2			-1.2			-1.2	V
V_{OH} High-level output voltage	Series 54S			$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$			2.5 3.4			2.5 3.4			2.5 3.4	V
	Series 74S			$V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$			2.7 3.4			2.7 3.4			2.7 3.4	
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5			0.5			0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1			1			1	mA
I_{IH} High-level input current	J, K, or D			50			50			50			50	µA
	Clear			150			100			100			200	
	Preset			100			100			100			100	
	Clock			100			100			100			200	
I_{IL} Low-level input current	J, K, or D			-2			-1.6			-1.6			-1.6	mA
	Clear *			-6			-7			-7			-14	
	Preset *			-4			-7			-7			-7	
	Clock			-4			-4			-4			-8	
I_{OS} Short-circuit output current*	$V_{CC} = \text{MAX}$			-40			-100			-40			-100	mA
I_{CC} Supply current (average per flip-flop)	$V_{CC} = \text{MAX}, \text{ See Note 1}$			15 25			15 25			15 25			15 25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

* Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.

* Clear is tested with preset high and preset is tested with clear high.

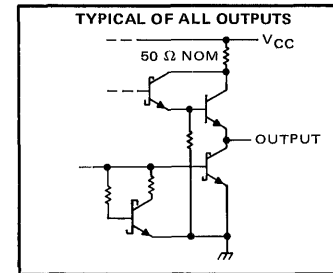
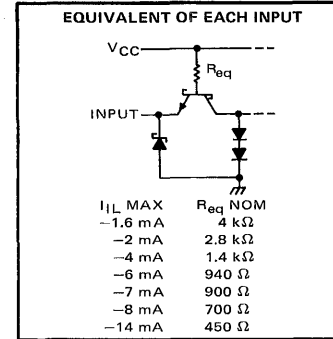
NOTE 1: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{ C}$

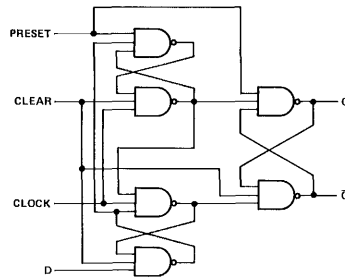
PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'S74			'S112, 'S113, 'S114			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}				75	110		80	125		MHz
t_{PLH}	Preset or clear	Q or \bar{Q}	$C_L = 15\text{ pF}$, $R_L = 280\ \Omega$, See Note 2	4	6		4	7		ns
t_{PHL}	Preset or clear (clock high)	Q or \bar{Q}		9	13.5		5	7		ns
t_{PLH}	Preset or clear (clock low)	Q or \bar{Q}		5	8		5	7		ns
t_{PHL}	Clock	Q or \bar{Q}		6	9		4	7		ns
t_{PHL}	Clock	Q or \bar{Q}		6	9		5	7		ns

† f_{max} ≡ maximum clock frequency
 t_{PLH} ≡ propagation delay time, low-to-high-level output
 t_{PHL} ≡ propagation delay time, high-to-low-level output
 NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

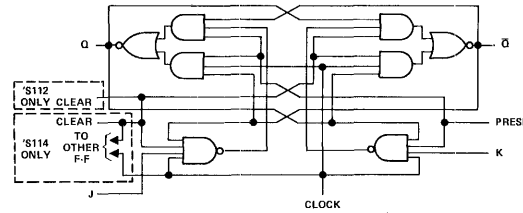
schematics of inputs and outputs



functional block diagrams



'S74—DUAL D WITH CLEAR AND PRESET



'S112—DUAL J-K WITH CLEAR AND PRESET
 'S113—DUAL J-K WITH PRESET
 'S114—DUAL J-K WITH PRESET, COMMON CLEAR,
 AND COMMON CLOCK

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recommended operating conditions

	54 FAMILY 74 FAMILY	SN54279 SN74279			SN54LS279 SN74LS279			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	54 Family 74 Family	4.5 4.75	5 5	5.5 5.25	4.5 4.5	5 5	5.5 5.25	V
High-level output current, I _{OH}				-800			-400	μA
Low-level output current, I _{OL}	54 Family			16			4	mA
	74 Family			16			8	
Operating free-air temperature, T _A	54 Family	-55		125	-55		125	°C
	74 Family	0		70	0		70	

electrical characteristics over recommended free-air operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54279 SN74279			SN54LS279 SN74LS279			UNIT		
		MIN	TYP‡	MAX	MIN	TYP‡	MAX			
V _{IH} High-level output voltage		2			2			V		
V _{IL} Low-level output voltage		54 Family			0.8			V		
		74 Family			0.8					
V _{IK} Input clamp voltage	V _{CC} = MAX, I _I = §				-1.5			V		
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = MAX	54 Family			2.4	3.4	2.5	3.4	V	
		74 Family			2.4	3.4	2.7	3.4		
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IL} = V _{IL} max, V _{IH} = 2 V	I _{OL} = MAX	54 Family			0.2	0.4	0.25	0.4	V
			74 Family			0.2	0.4	0.35	0.5	
		I _{OL} = 4 mA	Series 74LS			0.35			0.4	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5 V			1			mA		
		V _I = 7 V			0.1					
I _{IH} High-level input current	V _{CC} = MAX	V _I = 2.4 V			40			μA		
		V _I = 2.7 V			20					
I _{IL} Low-level input current	V _{CC} = MAX, V _I = 0.4 V				-1.6			-0.4	mA	
I _{OS} Short-circuit output current‡	V _{CC} = MAX	54 Family			-18	-55	-20	-100	mA	
		74 Family			-18	-57	-20	-100		
I _{CC} Supply current	V _{CC} = MAX, See note 1				18	30	3.8	7	mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ I_I = -12 mA for SN54/SN74 and -18 mA for SN54LS/SN74LS.

◆ Not more than one output should be shorted at a time, and for SN54LS/SN74LS, duration of the output short circuit should not exceed one second.

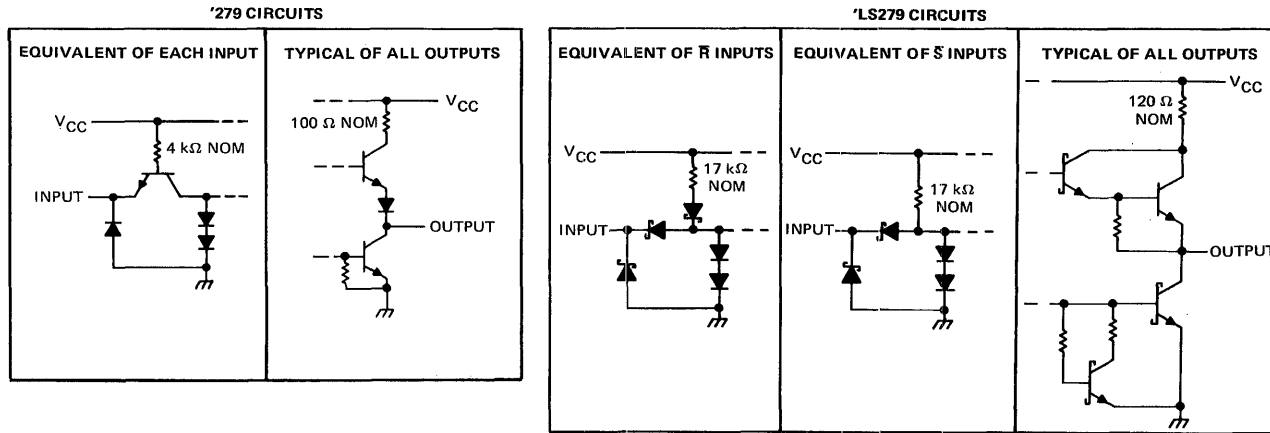
NOTE 1: I_{CC} is measured with all \bar{R} inputs grounded, all \bar{S} inputs at 4.5 V, and all outputs open.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output from \bar{S} input	$C_L = 15\text{ pF}$, See Notes 2 and 3		12	22	ns
t_{PHL} Propagation delay time, high-to-low-level output from \bar{S} input			9	15	
t_{PHL} Propagation delay time, high-to-low-level output from \bar{R} input			15	27	

NOTE 2: Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.
NOTE 3: $R_L = 400\ \Omega$ for '279, $R_L = 2\text{ k}\Omega$ for 'LS279.

schematics of inputs and outputs



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SN54LS63, SN74LS63 HEX CURRENT-SENSING INTERFACE GATES WITH TOTEM-POLE OUTPUTS

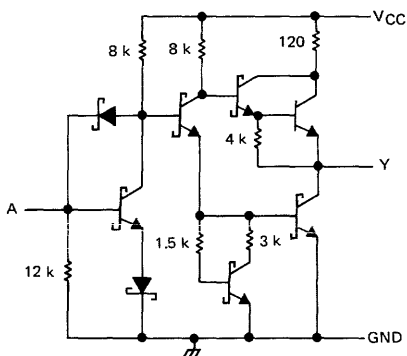
- Translates low-level input current to low-level output voltage
- Translates high-level input current to high-level output voltage
- Interfaces to PLA's or other logic elements that source current but do not sink current
- Operates from a single 5 V supply
- TTL compatible
- Low power dissipation . . .40 mW typical

description

Each of these Schottky-clamped interface gates is able to discriminate between low-level ($\leq 50 \mu\text{A}$) and high-level ($\geq 200 \mu\text{A}$) input currents.

The outputs are fabricated with standard Low-Power Schottky design rules and are compatible with all TTL families.

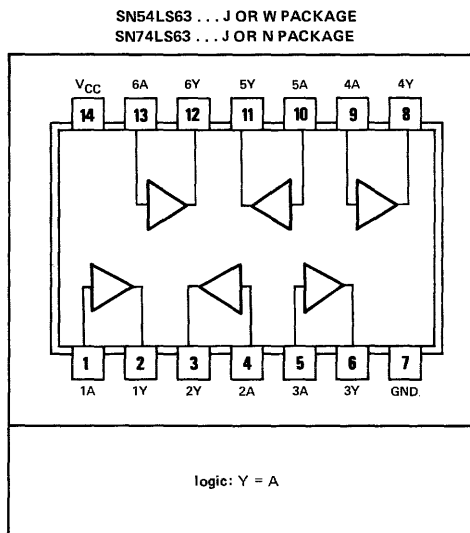
schematic (each gate)



Resistor values shown are nominal and in ohms.

recommended operating conditions

	SN54LS63			SN74LS63			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Input current, I_I			1			1	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}\text{C}$



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TYPES SN54LS63, SN74LS63 HEX CURRENT-SENSING INTERFACE GATES WITH TOTEM-POLE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS63			SN74LS63			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _I Input voltage	I _I = 50 μA, V _{CC} = MIN	0.35	1.05	1.75	0.6	1.05	1.6	V
	I _I = 200 μA, V _{CC} = MAX	0.6	1.30	2	0.85	1.30	1.8	
V _{OH} High-level output voltage	V _{CC} = MAX, I _I = 200 μA, I _{OH} = -400 μA	3.5	3.4		3.2	3.4		V
V _{OL} Low-level output voltage	V _{CC} = MIN, I _I = 50 μA	I _{OL} = 4 mA			0.25 0.4			V
		I _{OL} = 8 mA			0.35 0.5			
I _{OS} Short-circuit output current§	V _{CC} = MAX, I _I = 600 μA	-20	-100		-20	-100		mA
I _{CC} Supply current	V _{CC} = MAX, See Note 1	8 16			8 16			mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of output short circuit should not exceed one second.

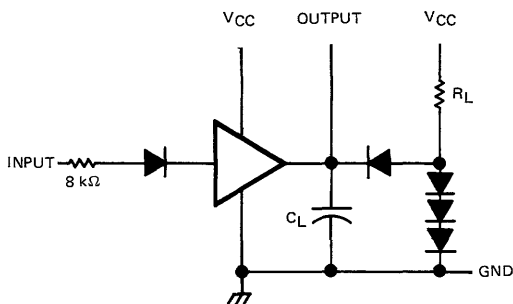
NOTE 1: I_{CC} is measured with inputs and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} Propagation delay time, low-to-high-level output	C _L = 15 pF,		27	45	ns
t _{PHL} Propagation delay time, high-to-low-level output	R _L = 2 kΩ	15	25		

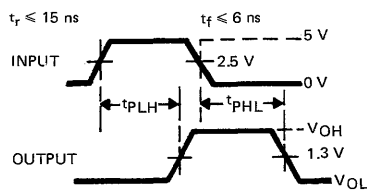
PARAMETER MEASUREMENT INFORMATION

6



NOTES: a. C_L includes probe and jig capacitance
b. All diodes are 1N916 or 1N3064

TEST CIRCUIT



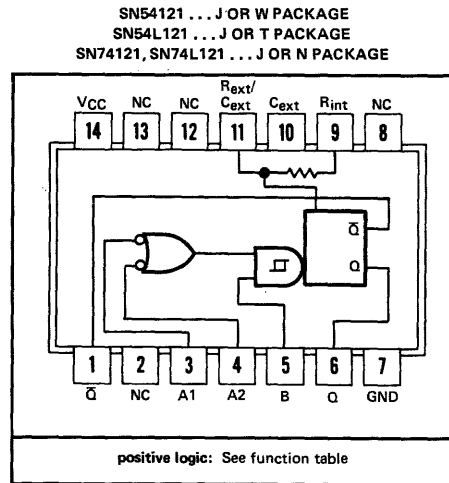
VOLTAGE WAVEFORMS

TYPES SN54121, SN54L121, SN74121, SN74L121 MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

- Programmable Output Pulse Width
With $R_{int} \dots 35 \text{ ns Typ}$
With $R_{ext}/C_{ext} \dots 40 \text{ ns to 28 Seconds}$
- Internal Compensation for Virtual
Temperature Independence
- Jitter-Free Operation up to 90%
Duty Cycle
- Inhibit Capability

FUNCTION TABLE				
INPUTS			OUTPUTS	
A1	A2	B	Q	\bar{Q}
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H		
↓	H	H		
↓	↓	H		
L	X	↑		
X	L	↑		

For explanation of function table symbols, see page 3-8.



NC—No internal connection

- NOTES:
1. An external capacitor may be connected between C_{ext} (positive) and R_{ext}/C_{ext} .
 2. To use the internal timing resistor, connect R_{int} to V_{CC} . For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.

description

6

These multivibrators feature dual negative-transition-triggered inputs and a single positive-transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

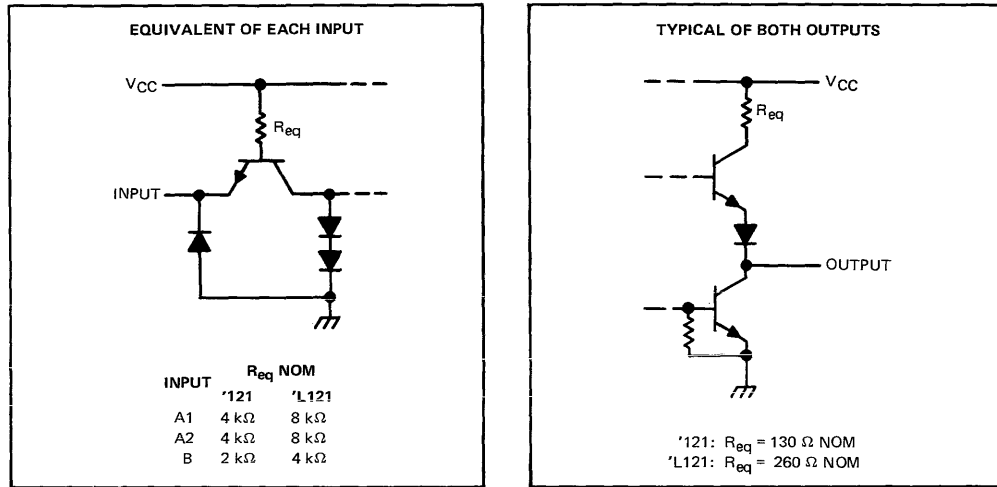
Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 40 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R_{int} connected to V_{CC} , C_{ext} and R_{ext}/C_{ext} open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μ F) and more than one decade of timing resistance (2 k Ω to 30 k Ω for the SN54121/SN54L121 and 2 k Ω to 40 k Ω for the SN74121/SN74L121). Throughout these ranges, pulse width is defined by the relationship $t_{w(out)} = C_{ext}R_T \ln 2 \approx 0.7 C_{ext}R_T$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μ F and timing resistance as low as 1.4 k Ω may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T . Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

TYPES SN54121, SN54L121, SN74121, SN74L121 MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

schematics of inputs and outputs



recommended operating conditions

	54 FAMILY	SN54121			SN54L121			UNIT
	74 FAMILY	SN74121			SN74L121			
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}				-400			-200	μ A
Low-level output current, I_{OL}				16			8	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt input, B	1			1			V/s
	Logic inputs, A1, A2	1			1			V/ μ s
Input pulse width, $t_{w(in)}$		50			100			ns
External timing resistance, R_{ext}	54 Family	1.4			30			k Ω
	74 Family	1.4			40			k Ω
External timing capacitance, C_{ext}		0			1000			μ F
Duty cycle	$R_T = 2 \text{ k}\Omega$	67			67			%
	$R_T = \text{MAX } R_{ext}$	90			90			%
Operating free-air temperature, T_A	54 Family	-55			125			$^{\circ}$ C
	74 Family	0			70			$^{\circ}$ C

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TYPES SN54121, SN54L121, SN74121, SN74L121 MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54121 SN74121		SN54L121 SN74L121		UNIT		
		MIN	TYP‡	MAX	MIN		TYP‡	MAX
V _{T+}	Positive-going threshold voltage at A input	V _{CC} = MIN		1.4	2	1.4	2	V
V _{T-}	Negative-going threshold voltage at A input	V _{CC} = MIN		0.8	1.4	0.8	1.4	V
V _{T+}	Positive-going threshold voltage at B input	V _{CC} = MIN		1.55	2	1.55	2	V
V _{T-}	Negative-going threshold voltage at B input	V _{CC} = MIN		0.8	1.35	0.8	1.35	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -12 mA				-1.5	-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, I _{OH} = MAX		2.4	3.4	2.4	3.4	V
V _{OL}	Low-level output voltage	V _{CC} = MIN, I _{OL} = MAX		0.2	0.4	0.2	0.4	V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V				1	1	mA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.4 V		A1 or A2		40	20	μA
				B		80	40	
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V		A1 or A2		-1.6	-0.8	mA
				B		-3.2	-1.6	
I _{OS}	Short-circuit output current*	V _{CC} = MAX		54 Family		-20	-55	mA
				74 Family		-18	-55	
I _{CC}	Supply current	V _{CC} = MAX		Quiescent		13	25	mA
				Triggered		23	40	
						7	12	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

* Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	'121			'L121			UNIT		
		MIN	TYP	MAX	MIN	TYP	MAX			
t _{PLH}	Propagation delay time, low-to-high-level Q output from either A input			45	70			140	ns	
t _{PLH}	Propagation delay time, low-to-high-level Q output from B input			35	55			110	ns	
t _{PHL}	Propagation delay time, high-to-low-level Q output from either A input			50	80			160	ns	
t _{PHL}	Propagation delay time, high-to-low-level Q output from B input			40	65			130	ns	
t _{w(out)}	Pulse width obtained using internal timing resistor	C _L = 15 pF, R _L = 400 Ω for '121, R _L = 800 Ω for 'L121, See Note 3		70	110	150	70	225	260	ns
t _{w(out)}	Pulse width obtained with zero timing capacitance			30	50			35	70	ns
t _{w(out)}	Pulse width obtained using external timing resistor			600	700	800	600	700	850	ns
				6	7	8	6	7	8	ms

NOTE 3: Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

TYPES SN54121, SN54L121, SN74121, SN74L121 MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

TYPICAL CHARACTERISTICS[§]

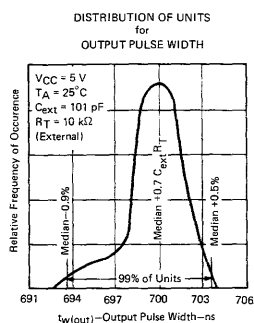


FIGURE 1

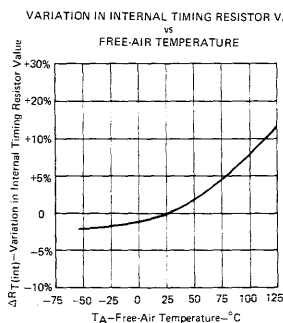


FIGURE 2

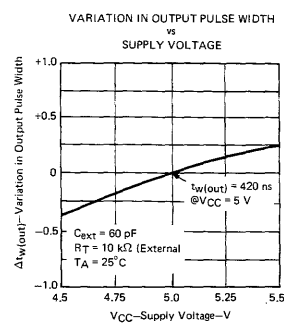


FIGURE 3

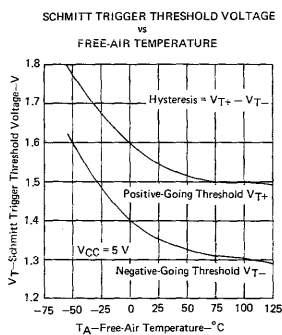


FIGURE 4

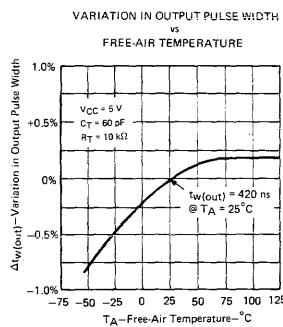


FIGURE 5

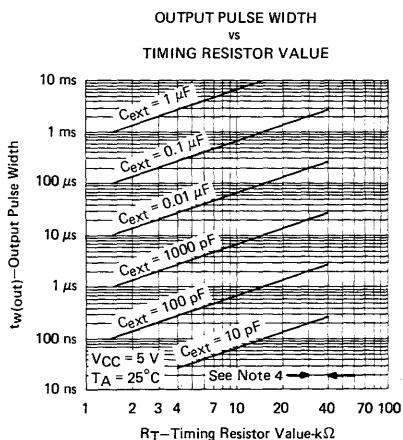


FIGURE 6

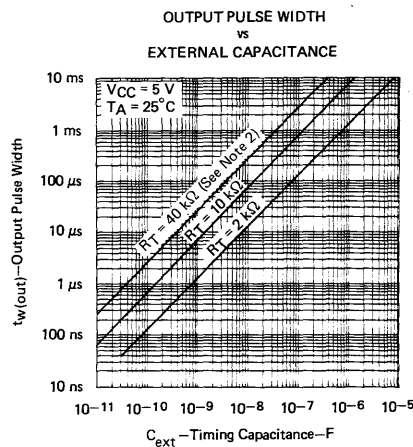


FIGURE 7

NOTE 4: These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54L121.
[§]Data for temperatures below 0°C and above 70°C are applicable for SN54121 and SN54L121.

TYPES SN54221, SN54LS221, SN74221, SN74LS221 DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

- SN54221, SN54LS221, SN74221 and SN74LS221 Are Dual Versions of Highly Stable SN54121, SN74121 One-Shots on a Monolithic Chip
- SN54221 and SN74221 Demonstrate Electrical and Switching Characteristics That Are Virtually Identical to the SN54121, SN74121 One-Shots
- Pin-Out Is Identical to the SN54123, SN74123, SN54LS123, SN74LS123
- Overriding Clear Terminates Output Pulse

TYPE	TYPICAL POWER DISSIPATION	MAXIMUM OUTPUT PULSE LENGTH
SN54221	130 mW	21 s
SN74221	130 mW	28 s
SN54LS221	23 mW	49 s
SN74LS221	23 mW	70 s

description

The '221 and 'LS221 are monolithic dual multivibrators with performance characteristics virtually identical to those of the '121. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

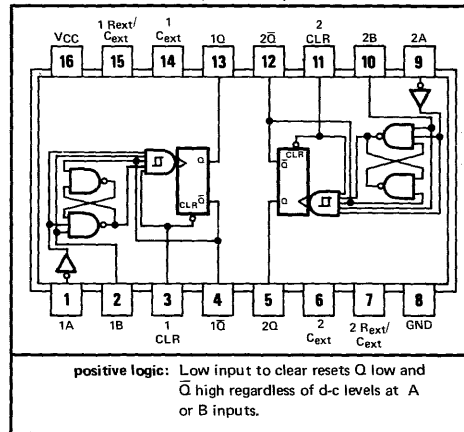
Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35 nanoseconds to the maximums shown in the above table by choosing appropriate timing components. With R_{ext} = 2 kΩ and C_{ext} = 0, an output pulse of typically 30 nanoseconds is achieved which may be used as a d-c-triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length. Typical triggering and clearing sequences are illustrated as a part of the switching characteristics waveforms.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 30 kΩ for the SN54221, 2 kΩ to 40 kΩ for the SN74221, 2 kΩ to 70 kΩ for the SN54LS221, and 2 kΩ to 100 kΩ for the SN74LS221). Throughout these ranges, pulse width is defined by the relationship: $t_w(\text{out}) = C_{\text{ext}}R_{\text{ext}} \ln 2 \approx 0.7 C_{\text{ext}}R_{\text{ext}}$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μF and timing resistance as low as 1.4 kΩ may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is

SN54221, SN54LS221 . . . J OR W PACKAGE
SN74221, SN74LS221 . . . J OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE
(EACH MONOSTABLE)

CLEAR	INPUTS		OUTPUTS	
	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑		
H	↓	H		
↑	L	H		

Also see description and switching characteristics

See explanation of function tables on page 3-8.

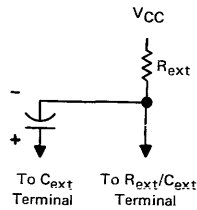
TYPES SN54221, SN54LS221, SN74221, SN74LS221 DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

description (continued)

held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T . Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

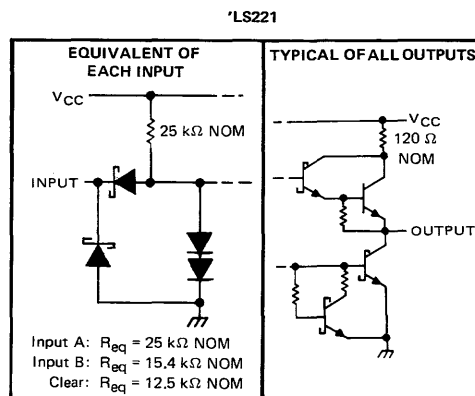
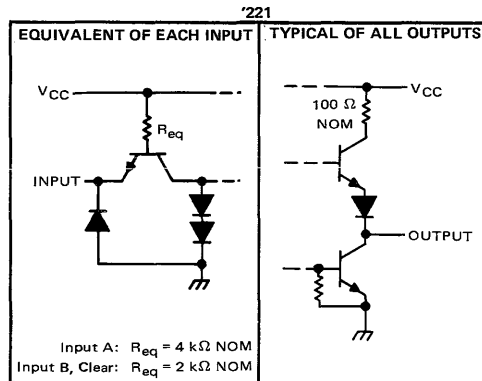
The variance in output pulse width from device to device is typically less than $\pm 0.5\%$ for given external timing components. An example of this distribution for the '221 is shown in Figure 2. Variations in output pulse width versus supply voltage and temperature for the '221 are shown in Figure 3 and 4, respectively.

Pin assignments for these devices are identical to those of the SN54123/SN74123 or SN54LS123/SN74LS123 so that the '221 or 'LS221 can be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext} .



TIMING COMPONENT CONNECTIONS

schematics of inputs and outputs



6

TYPES SN54221, SN74221 DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

recommended operating conditions

	SN54221			SN74221			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt input, B	1		1			V/s
	Logic input, A	1		1			V/ μ s
Input pulse width	A or B, $t_{w(in)}$	50		50			ns
	Clear, $t_{w(clear)}$	20		20			
Clear-inactive-state setup time, t_{su}		15		15			ns
External timing resistance, R_{ext}		1.4	30	1.4		40	k Ω
External timing capacitance, C_{ext}		0	1000	0		1000	μ F
Output duty cycle	$R_{ext} = 2\text{ k}\Omega$		67			67	%
	$R_{ext} = \text{MAX } R_{ext}$		90			90	
Operating free-air temperature, T_A		-55	125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V_{T+} Positive-going threshold voltage at A input	$V_{CC} = \text{MIN}$		1.4	2	V
V_{T-} Negative-going threshold voltage at A input	$V_{CC} = \text{MIN}$		0.8	1.4	V
V_{T+} Positive-going threshold voltage at B input	$V_{CC} = \text{MIN}$		1.55	2	V
V_{T-} Negative-going threshold voltage at B input	$V_{CC} = \text{MIN}$		0.8	1.35	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12\text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $I_{OH} = -800\text{ }\mu\text{A}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $I_{OL} = 16\text{ mA}$		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5\text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4\text{ V}$	Input A		40	μ A
		Input B, Clear		80	
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4\text{ V}$	Input A		-1.6	mA
		Input B, Clear		-3.2	
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$				mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$	Quiescent		26	50
		Triggered		46	80

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§]Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT	
t_{PLH}	A	Q	$C_L = 15\text{ pF}$, $R_L = 400\text{ }\Omega$, See Figure 1 and Note 2	$C_{ext} = 80\text{ pF}$, $R_{ext} = 2\text{ k}\Omega$		45	70	ns	
	B	Q				35	55		
t_{PHL}	A	\bar{Q}					50	80	ns
	B	\bar{Q}					40	65	
t_{PHL}	Clear	Q						27	ns
t_{PLH}	Clear	\bar{Q}						40	ns
$t_{w(out)}$	A or B	Q or \bar{Q}	$C_{ext} = 80\text{ pF}$, $R_{ext} = 2\text{ k}\Omega$		70	110	150	ns	
			$C_{ext} = 0$, $R_{ext} = 2\text{ k}\Omega$		20	30	50		
			$C_{ext} = 100\text{ pF}$, $R_{ext} = 10\text{ k}\Omega$		650	700	750		
			$C_{ext} = 1\text{ }\mu\text{F}$, $R_{ext} = 10\text{ k}\Omega$		6.5	7	7.5	ms	

[†] t_{PLH} \equiv Propagation delay time, low-to-high-level output

t_{PHL} \equiv Propagation delay time, high-to-low-level output

$t_{w(out)}$ \equiv Output pulse width

NOTE 2: Load circuit is shown on page 3-10.

TYPES SN54LS221, SN74LS221 DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

recommended operating conditions

		SN54LS221			SN74LS221			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		-400			-400			μ A
Low-level output current, I_{OL}		4			8			mA
Rate of rise or fall of input pulse, dv/dt	Schmitt, B	1			1			V/s
	Logic input, A	1			1			V/ μ s
Input pulse width	A or B, $t_w(\text{in})$	40			40			ns
	Clear, $t_w(\text{clear})$	40			40			
Clear-inactive-state setup time, t_{su}		15			15			ns
External timing resistance, R_{ext}		1.4			1.4			k Ω
External timing capacitance, C_{ext}		0			1000			μ F
Output duty cycle	$R_T = 2 \text{ k}\Omega$	67			67			%
	$R_T = \text{MAX } R_{ext}$	90			90			
Operating free-air temperature, T_A		-55			125			$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS221			SN74LS221			UNIT	
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX		
V_{T+}	Positive-going threshold voltage at A input $V_{CC} = \text{MIN}$	1.0 2			1.0 2			V	
V_{T-}	Negative-going threshold voltage at A input $V_{CC} = \text{MIN}$	0.7 1.0			0.8 1.0			V	
V_{T+}	Positive-going threshold voltage at B input $V_{CC} = \text{MIN}$	1.0 2			1.0 2			V	
V_{T-}	Negative-going threshold voltage at B input $V_{CC} = \text{MIN}$	0.7 0.9			0.8 0.9			V	
V_{IK}	Input clamp voltage $V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$	-1.5			-1.5			V	
V_{OH}	High-level output voltage $V_{CC} = \text{MIN}$, $I_{OH} = -400 \mu\text{A}$	2.5 3.4			2.7 3.4			V	
V_{OL}	Low-level output voltage $V_{CC} = \text{MIN}$	$I_{OL} = 4 \text{ mA}$			0.25 0.4			V	
		$I_{OL} = 8 \text{ mA}$			0.35 0.5				
I_I	Input current at maximum input voltage $V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$	0.1			0.1			mA	
I_{IH}	High-level input current $V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$	20			20			μ A	
I_{IL}	Low-level input current	Input A	-0.4			-0.4			mA
		Input B	-0.4			-0.4			
		Clear	-0.8			-0.8			
I_{OS}	Short-circuit output current [§] $V_{CC} = \text{MAX}$	-20 -100			-20 -100			mA	
I_{CC}	Supply current $V_{CC} = \text{MAX}$	Quiescent			4.7 11			mA	
		Triggered			19 27				

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§]Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

6

**TYPES SN54LS221, SN74LS221
DUAL MONOSTABLE MULTIVIBRATORS
WITH SCHMITT-TRIGGER INPUTS**

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER †	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH}	A	Q	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$, See Figure 1 and Note 3	$C_{ext} = 80\text{ pF}$, $R_{ext} = 2\text{ k}\Omega$	45	70	ns	
	B	Q			35	55		
t_{PHL}	A	\bar{Q}			50	80	ns	
	B	\bar{Q}			40	65		
t_{PHL}	Clear	Q			35	55	ns	
t_{PLH}	Clear	\bar{Q}			44	65	ns	
$t_{w(out)}$	A or B	Q or \bar{Q}		$C_{ext} = 80\text{ pF}$, $R_{ext} = 2\text{ k}\Omega$	70	120	150	ns
				$C_{ext} = 0$, $R_{ext} = 2\text{ k}\Omega$	20	47	70	
				$C_{ext} = 100\text{ pF}$, $R_{ext} = 10\text{ k}\Omega$	600	670	750	
				$C_{ext} = 1\text{ }\mu\text{F}$, $R_{ext} = 10\text{ k}\Omega$	6	6.7	7.5	

† t_{PLH} \equiv Propagation delay time, low-to-high-level output

t_{PHL} \equiv Propagation delay time, high-to-low-level output

$t_{w(out)}$ \equiv Output pulse width

NOTE 3: Load circuit is shown on page 3-11.

6

TYPES SN54221, SN54LS221, SN74221, SN74LS221
DUAL MONOSTABLE MULTIVIBRATORS
WITH SCHMITT-TRIGGER INPUTS

PARAMETER MEASUREMENT INFORMATION

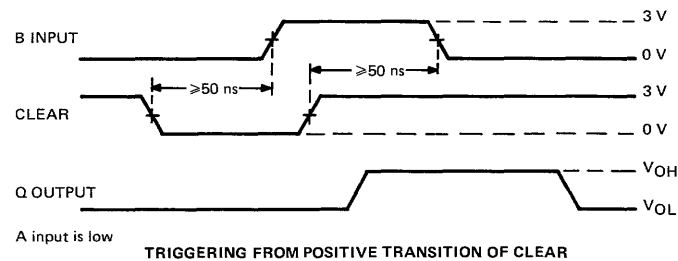
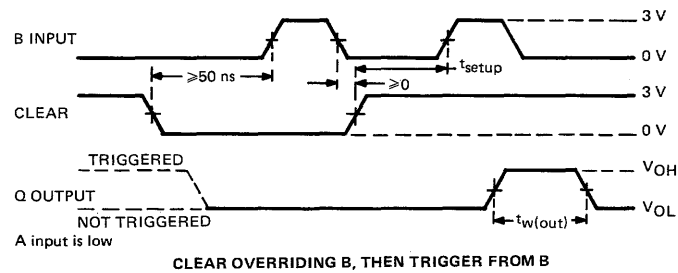
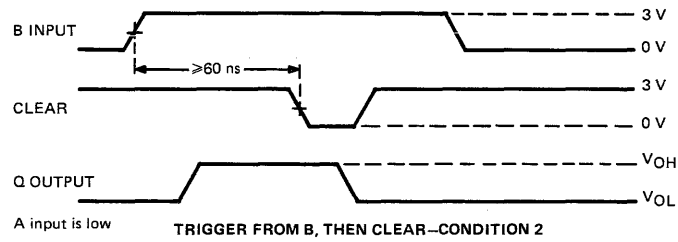
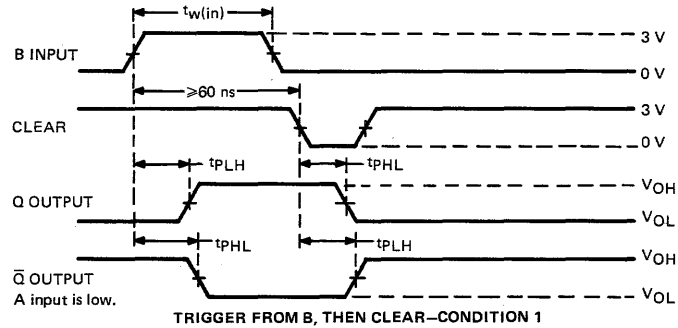
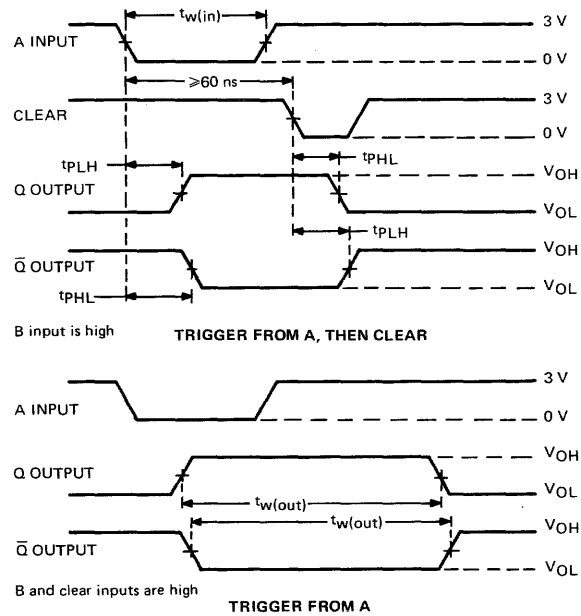


FIGURE 1—SWITCHING CHARACTERISTICS

6

TYPES SN54221, SN54LS221, SN74221, SN74LS221
DUAL MONOSTABLE MULTIVIBRATORS
WITH SCHMITT-TRIGGER INPUTS

PARAMETER MEASUREMENT INFORMATION



6

NOTES: A. Input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_{out} \approx 50 \Omega$; for '221, $t_r \leq 7$ ns, $t_f \leq 7$ ns, for 'LS221, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
 B. All measurements are made between the 1.5 V points of the indicated transitions for the '221 or between the 1.3 V points for the 'LS221.

FIGURE 1—SWITCHING CHARACTERISTICS (CONTINUED)

TYPES SN54221, SN74221 DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

TYPICAL CHARACTERISTICS ('221 ONLY)†

DISTRIBUTION OF UNITS
for
OUTPUT PULSE WIDTH

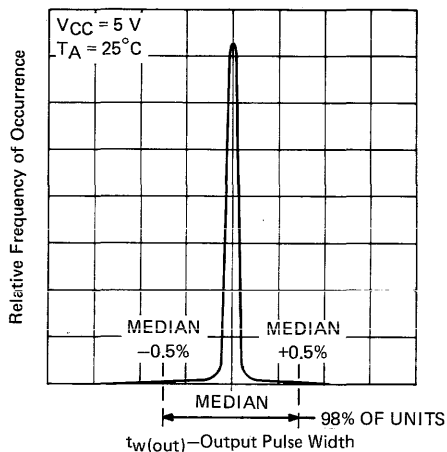


FIGURE 2

VARIATION IN OUTPUT PULSE WIDTH
vs
SUPPLY VOLTAGE

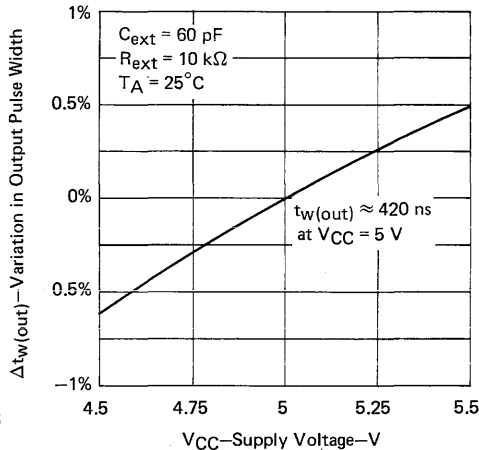


FIGURE 3

VARIATION IN OUTPUT PULSE WIDTH
vs
FREE-AIR TEMPERATURE

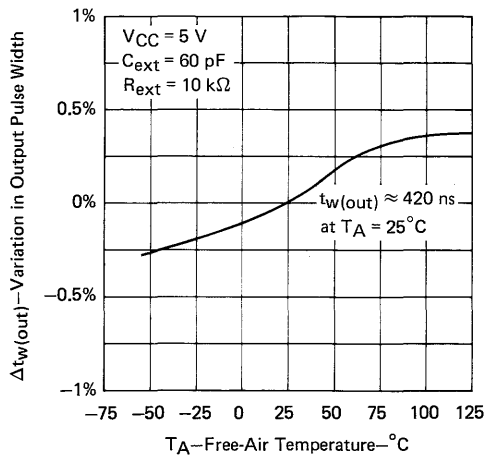


FIGURE 4

OUTPUT PULSE WIDTH
vs
TIMING RESISTOR VALUE

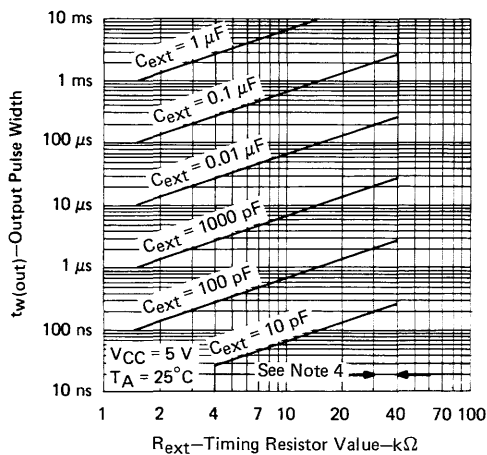


FIGURE 5

NOTE 4: These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54221.

†Data for temperatures below 0°C and above 70°C, and for supply voltages below 4.75 V and above 5.25 V are applicable for the SN54221 only.

6

TYPES SN54122, SN54123, SN54L122, SN54L123, SN54LS122, SN54LS123, SN74122, SN74123, SN74L122, SN74L123, SN74LS122, SN74LS123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

- D-C Triggered from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Compensated for VCC and Temperature Variations
- '122, 'L122, 'LS122 Have Internal Timing Resistors

'122, 'L122, 'LS122
FUNCTION TABLE

CLEAR	INPUTS				OUTPUTS	
	A1	A2	B1	B2	Q	\bar{Q}
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⌋	⌋
H	L	X	H	↑	⌋	⌋
H	X	L	↑	H	⌋	⌋
H	X	L	H	↑	⌋	⌋
H	H	↓	H	H	⌋	⌋
H	↓	↓	H	H	⌋	⌋
H	↓	H	H	H	⌋	⌋
↑	L	X	H	H	⌋	⌋
↑	X	L	H	H	⌋	⌋

'123, 'L123, 'LS123
FUNCTION TABLE

CLEAR	INPUTS		OUTPUTS	
	A	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⌋	⌋
H	↓	H	⌋	⌋
↑	L	H	⌋	⌋

See explanation of function tables on page 3-8.

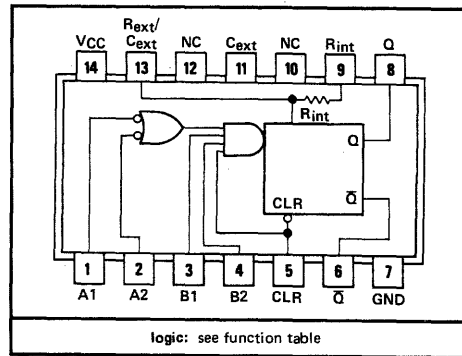
description

These d-c triggered multivibrators feature output pulse width control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The '122, 'L122, and 'LS122 have internal timing resistors that allow the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

The 'LS122 and 'LS123 are provided enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

- NOTES:
1. An external timing capacitor may be connected between C_{EXT} and R_{EXT}/C_{EXT} (positive).
 2. To use the internal timing resistor of '122, 'L122 or 'LS122, connect R_{INT} to V_{CC}.
 3. For improved pulse width accuracy and repeatability, connect an external resistor between R_{EXT}/C_{EXT} and V_{CC} with R_{INT} open-circuited.
 4. To obtain variable pulse widths, connect an external variable resistance between R_{INT} or R_{EXT}/C_{EXT} and V_{CC}.

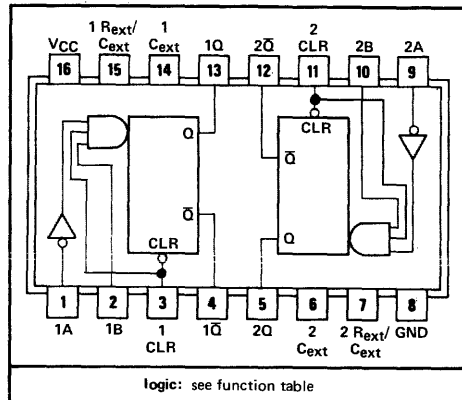
SN54122, SN54LS122 ... J OR W
SN54L122 ... J OR T
SN74122, SN74L122, SN74LS122 ... J OR N
(TOP VIEW) (SEE NOTES 1 THRU 4)



logic: see function table

NC—No internal connection.

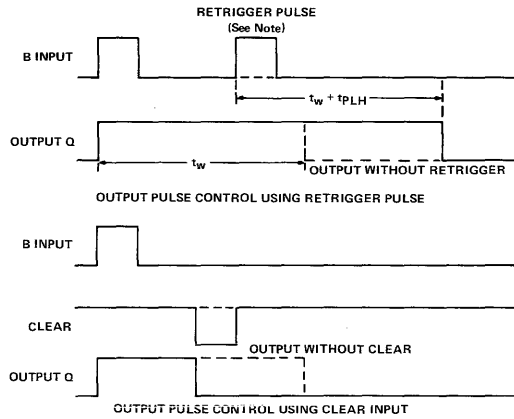
SN54123, SN54LS123 ... J OR W
SN54L123 ... J
SN74123, SN74L123, SN74LS123 ... J OR N
(TOP VIEW) (SEE NOTES 1 THRU 4)



logic: see function table

**TYPES SN54122, SN54123, SN54L122, SN54L123, SN54LS122, SN54LS123,
SN74122, SN74123, SN74L122, SN74L123, SN74LS122, SN74LS123
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS**

description (continued)

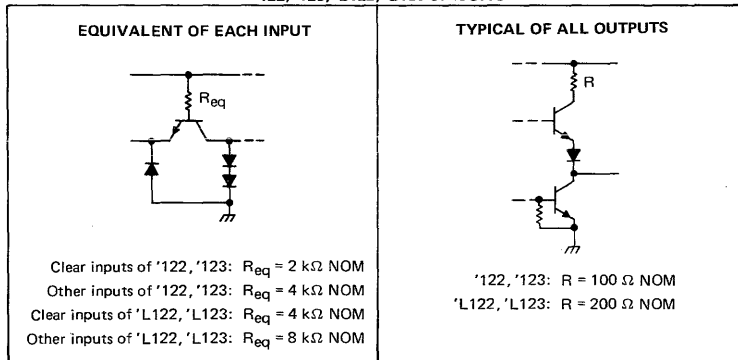


NOTE: Retrigger pulse must not start before $0.22 C_{ext}$ (in picofarads) nanoseconds after previous trigger pulse.

FIGURE 1—TYPICAL INPUT/OUTPUT PULSES

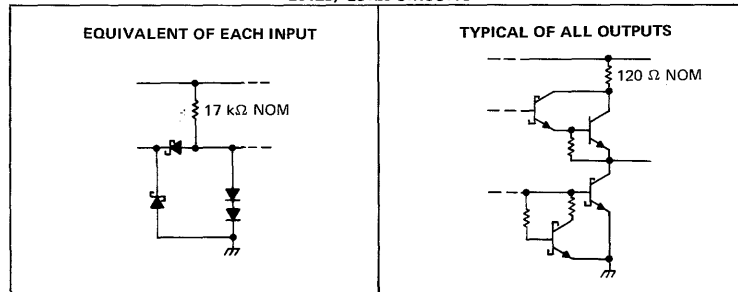
schematics of inputs and outputs

'122, '123, 'L122, 'L123 CIRCUITS



6

'LS122, 'LS123 CIRCUITS



TYPES SN54122, SN54123, SN74122, SN74123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

recommended operating conditions

	SN54'			SN74'			UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V	
High-level output current, I_{OH}	-800			-800			μA	
Low-level output current, I_{OL}	16			16			mA	
Pulse width, t_w	40			40			ns	
External timing resistance, R_{ext}	5			5			50 $k\Omega$	
External capacitance, C_{ext}	No restriction			No restriction				
Wiring capacitance at R_{ext}/C_{ext} terminal	50			50			pF	
Operating free-air temperature, T_A	-55			125			0	$^{\circ}C$

electrical characteristics over recommended free-air operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'122			'123			UNIT		
		MIN	TYP‡	MAX	MIN	TYP‡	MAX			
V_{IH} High-level input voltage		2			2			V		
V_{IL} Low-level input voltage		0.8			0.8			V		
V_{IK} Input clamp voltage		-1.5			-1.5			V		
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$, See Note 1	2.4	3.4		2.4	3.4		V		
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $I_{OL} = 16 \text{ mA}$, See Note 1	0.2	0.4		0.2	0.4		V		
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$	1			1			mA		
I_{IH} High-level input current	Data inputs	40			40			μA		
	Clear input	80			80					
I_{IL} Low-level input current	Data inputs	-1.6			-1.6			mA		
	Clear input	-3.2			-3.2					
I_{OS} Short-circuit output current*	$V_{CC} = \text{MAX}$, See Note 5	-10	-40		-10	-40		mA		
I_{CC} Supply current (quiescent or triggered)	$V_{CC} = \text{MAX}$, See Notes 6 and 7	23			28			46	66	mA

† For conditions shown as MIN or MAX, use the value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}C$.

* Not more than one output should be shorted at a time.

NOTES: 5. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at \bar{Q} , or I_{OS} at Q. C_{ext} is open to measure V_{OH} at \bar{Q} , V_{OL} at Q, or I_{OS} at \bar{Q} .

6. Quiescent I_{CC} is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, $C_{ext} = 0.02 \mu F$, and $R_{ext} = 25 \text{ k}\Omega$. R_{int} of '122 is open.

7. I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, $C_{ext} = 0.02 \mu F$, and $R_{ext} = 25 \text{ k}\Omega$. R_{int} of '122 is open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}C$, see note 8

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'122			'123			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	Q	$C_{ext} = 0$, $R_{ext} = 5 \text{ k}\Omega$, $C_L = 15 \text{ pF}$, $R_L = 400 \Omega$	22	33		22	33		ns
	B			19	28		19	28		
t_{PHL}	A	\bar{Q}		30	40		30	40		ns
	B			27	36		27	36		
t_{PHL}	Clear	Q		18	27		18	27		ns
t_{PLH}		\bar{Q}		30	40		30	40		
$t_{wQ}(\text{min})$	A or B	Q		45	65		45	65		ns
t_{wQ}	A or B	Q		3.08	3.42	3.76	2.76	3.03	3.37	μs

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output

t_{PHL} ≡ propagation delay time, high-to-low-level output

t_{wQ} ≡ width of pulse at output Q

NOTE 8: Load circuit and voltage waveforms are shown on page 3-10.

TYPES SN54L122, SN54L123, SN74L122, SN74L123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

recommended operating conditions

	SN54L'			SN74L'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	-400			-400			μ A
Low-level output current, I_{OL}	8			8			mA
Pulse width, t_w	50			50			ns
External timing resistance, R_{ext}	5			25			k Ω
External capacitance, C_{ext}	No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal	50			50			pF
Operating free-air temperature, T_A	-55			125			$^{\circ}$ C

electrical characteristics over recommended free-air operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'L122			'L123			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage		0.8			0.8			V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$	1.5			-1.5			V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, I_{OH} = -400 \mu\text{A}$, See Note 1	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, I_{OL} = 8 \text{ mA}$, See Note 1	0.2	0.4		0.2	0.4		V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	1			1			mA
I_{IH} High-level input current	Data inputs	20			20			μ A
	Clear input	40			40			
I_{IL} Low-level input current	Data inputs	-0.8			-0.8			mA
	Clear input	-1.6			-1.6			
I_{OS} Short-circuit output current*	$V_{CC} = \text{MAX}$, See Note 9	-5	-20		-5	-20		mA
I_{CC} Supply current (quiescent or triggered)	$V_{CC} = \text{MAX}$, See Notes 10 and 11	11	14		23	33		mA

† For conditions shown as MIN or MAX, use the value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

* Not more than one output should be shorted at a time.

NOTES: 9. Ground C_{ext} to measure V_{OH} at \bar{Q} , V_{OL} at \bar{Q} , or I_{OS} at \bar{Q} . C_{ext} is open to measure V_{OH} at \bar{Q} , V_{OL} at \bar{Q} , or I_{OS} at \bar{Q} .

10. Quiescent I_{CC} is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, $C_{ext} = 0.02 \mu\text{F}$, and $R_{ext} = 25 \text{ k}\Omega$. R_{int} of 'L122 is open.

11. I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, $C_{ext} = 0.02 \mu\text{F}$, and $R_{ext} = 25 \text{ k}\Omega$. R_{int} of 'L122 is open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$, see note 8

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'L122			'L123			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	Q	$C_{ext} = 0, R_{ext} = 5 \text{ k}\Omega,$ $C_L = 15 \text{ pF}, R_L = 800 \Omega$	44	66		44	66		ns
	B			38	56		38	56		
t_{PHL}	A	\bar{Q}		60	80		60	80		ns
	B			54	72		54	72		
t_{PHL}	Clear	Q		36	54		36	54		ns
t_{PLH}		\bar{Q}		60	80		60	80		
t_{wQ} (min)	A or B	Q		90	135		90	135		ns
t_{wQ}	A or B	Q		1.7	1.9	2.1	1.3		2.1	

‡ $t_{PLH} \equiv$ propagation delay time, low-to-high-level output

$t_{PHL} \equiv$ propagation delay time, high-to-low-level output

$t_{wQ} \equiv$ width of pulse at output Q

NOTE 8: Load circuit and voltage waveforms are shown on page 3-10.

TYPES SN54LS122, SN54LS123, SN74LS122, SN74LS123

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

recommended operating conditions

	SN54LS*			SN74LS*			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Pulse width, t_w	40			40			ns
External timing resistance, R_{ext}	5		180	5		260	k Ω
External capacitance, C_{ext}	No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal	50			50			pF
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}, I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$		0.25 0.4		0.25 0.4	0.35 0.5		V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short-circuit output current‡	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC} Supply current (quiescent or triggered)	$V_{CC} = \text{MAX},$ See Note 13			6 12	11 20		6 12	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTES: 12. To measure V_{OH} at Q, V_{OL} at \bar{Q} , or I_{OS} at Q, ground R_{ext}/C_{ext} , apply 2 V to B and clear, and pulse A from 2 V to 0 V.

13. With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$, see note 14

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	$C_{ext} = 0,$ $C_L = 15 \text{ pF},$ $R_{ext} = 5 \text{ k}\Omega,$ $R_L = 2 \text{ k}\Omega$		23	33	ns
	B	Q			23	44	
t_{PHL}	A	\bar{Q}			32	45	ns
	B	\bar{Q}			34	56	
t_{PLH}	Clear	Q	$C_{ext} = 1000 \text{ pF},$ $C_L = 15 \text{ pF},$ $R_{ext} = 10 \text{ k}\Omega,$ $R_L = 2 \text{ k}\Omega$		20	27	ns
t_{PLH}	Clear	\bar{Q}			28	45	
$t_{wQ}(\text{min})$	A or B	Q			116	200	ns
t_{wQ}	A or B	Q			4	4.5	

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{wQ} = width of pulse at output Q

NOTE 14: Load circuit and voltage waveforms are shown on page 3-11.

TYPES SN54122, SN74122, SN54123, SN74123 SN54L122, SN74L122, SN54L123, SN74L123, RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

TYPICAL APPLICATION DATA FOR '122, '123, 'L122, 'L123

For pulse widths when $C_{ext} \leq 1000$ pF, See Figures 4 and 5.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse width (t_w) is defined as:

$$t_w = K \cdot R_T \cdot C_{ext} \left(1 + \frac{0.7}{R_T} \right)$$

where

K is 0.32 for '122, 0.28 for '123,
0.37 for 'L122, 0.33 for 'L123

R_T is in $k\Omega$ (internal or external timing resistance).

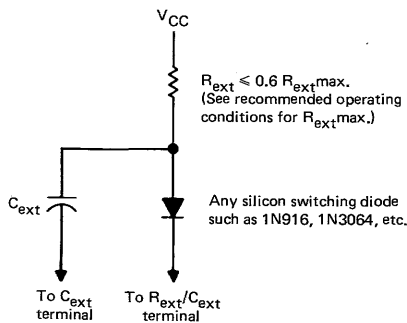
C_{ext} is in pF

t_w is in nanoseconds

To prevent reverse voltage across C_{ext} , it is recommended that the method shown in Figure 2 be employed when using electrolytic capacitors and in applications utilizing the clear function. In all applications using the diode, the pulse width is:

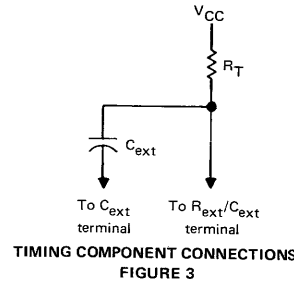
$$t_w = K_D \cdot R_T \cdot C_{ext} \left(1 + \frac{0.7}{R_T} \right)$$

K_D is 0.28 for '122, 0.25 for '123,
0.33 for 'L122, 0.29 for 'L123



TIMING COMPONENT CONNECTIONS WHEN
 $C_{ext} > 1000$ pF AND CLEAR IS USED
FIGURE 2

Applications requiring more precise pulse widths (up to 28 seconds) and not requiring the clear feature can best be satisfied with the '121 or 'L121.



TIMING COMPONENT CONNECTIONS
FIGURE 3

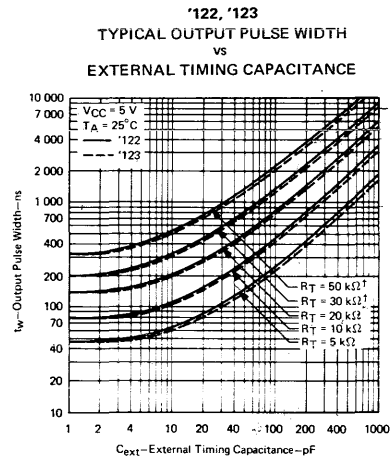


FIGURE 4

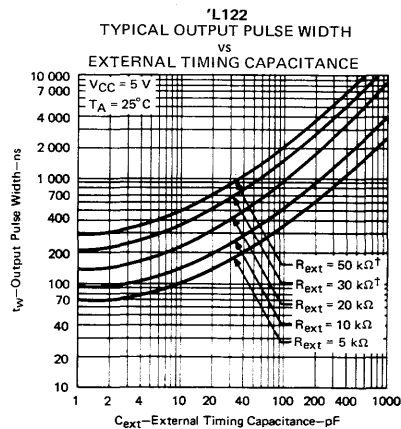


FIGURE 5

†These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54' and SN54L' circuits.

TYPES SN54LS122, SN74LS122, SN54LS123, SN74LS123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

TYPICAL APPLICATION DATA FOR 'LS122, 'LS123

The basic output pulse width is essentially determined by the values of external capacitance and timing resistance. For pulse widths when $C_{ext} \leq 1000$ pF, see Figure 7.

When $C_{ext} > 1000$ pF, the output pulse width is defined as:

$$t_w = 0.45 \cdot R_T \cdot C_{ext}$$

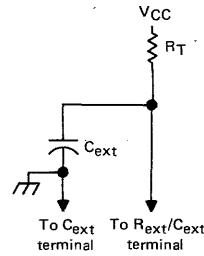
where

R_T is in $k\Omega$ (internal or external timing resistance.)

C_{ext} is in pF

t_w is in nanoseconds

For best results, system ground should be applied to the C_{ext} terminal. The switching diode is not needed for electrolytic capacitance applications.

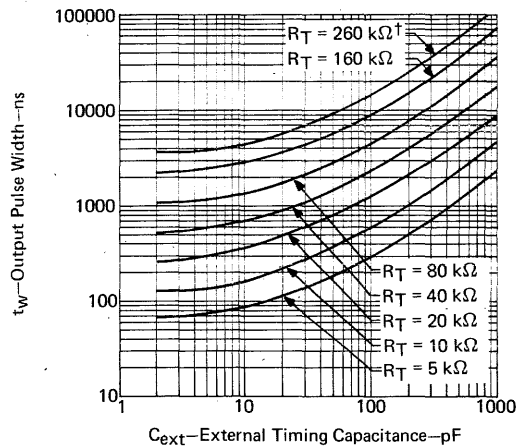


TIMING COMPONENT CONNECTIONS

FIGURE 6

6

'LS122, 'LS123 TYPICAL OUTPUT PULSE WIDTH vs EXTERNAL TIMING CAPACITANCE



† This value of resistance exceeds the maximum recommended for use over the full temperature range of the SN54LS circuits.

FIGURE 7

TYPES SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

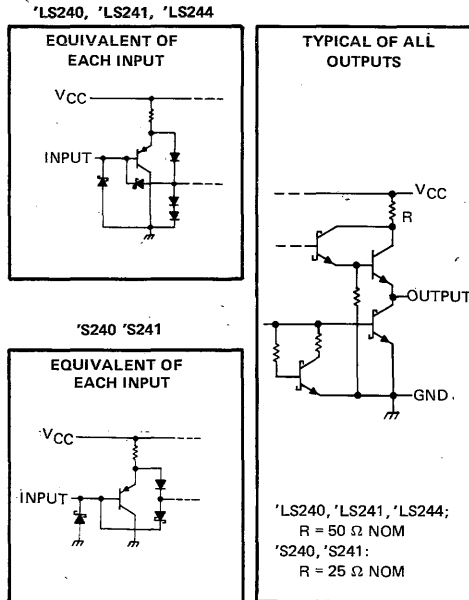
	Typical	Typical	Typical Propagation		Typical Enable/Disable Times	Typical Power Dissipation (Enabled)	
	I _{OL} (Sink Current)	I _{OH} (Source Current)	Inverting	Noninverting		Inverting	Noninverting
SN54LS*	12 mA	-12 mA	10.5 ns	12 ns	18 ns	130 mW	135 mW
SN74LS*	24 mA	-15 mA	10.5 ns	12 ns	18 ns	130 mW	135 mW
SN54S*	48 mA	-12 mA	4.5 ns	6 ns	9 ns	450 mW	538 mW
SN74S*	64 mA	-15 mA	4.5 ns	6 ns	9 ns	450 mW	538 mW

- 3-State Outputs Drive Bus Lines or Buffer-Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins

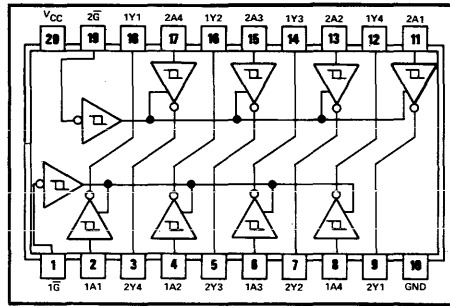
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical \bar{G} (active-low output control) inputs, and complementary G and \bar{G} inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise-margin. The SN74LS* and SN74S* can be used to drive terminated lines down to 133 ohms.

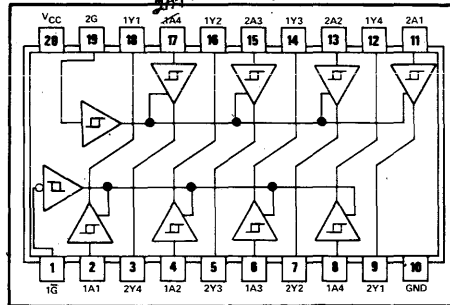
schematics of inputs and outputs



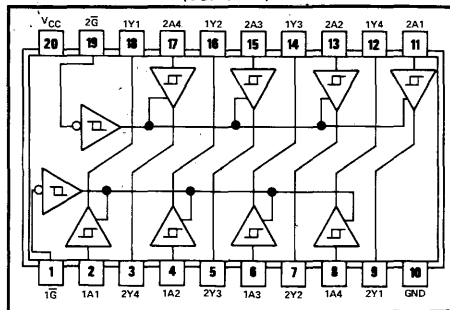
SN54LS240, SN54S240 ... J
SN74LS240, SN74S240 ... J OR N
(TOP VIEW)



SN54LS241, SN54S241 ... J
SN74LS241, SN74S241 ... J OR N
(TOP VIEW)



SN54LS244 ... J
SN74LS244 ... J OR N
(TOP VIEW)



6

**TYPES SN54LS240, SN54LS241, SN54LS244,
SN74LS240, SN74LS241, SN74LS244
BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

recommended operating conditions

PARAMETER	SN54LS*			SN74LS*			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-12			-15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT		
		MIN	TYP‡	MAX	MIN	TYP‡	MAX			
V_{IH} High-level input voltage		2			2			V		
V_{IL} Low-level input voltage			0.7			0.8		V		
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V		
Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$	0.2	0.4		0.2	0.4		V		
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$	2.4	3.4		2.4	3.4		V		
	$V_{CC} = \text{MIN}, V_{IL} = 0.5 \text{ V}, I_{OH} = \text{MAX}$	2			2			V		
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 12 \text{ mA}, V_{IL} = V_{IL\text{max}}$			0.4			0.4	V		
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 24 \text{ mA}, V_{IL} = V_{IL\text{max}}$						0.5	V		
I_{OZH} Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL\text{max}}$			20			20	μA		
I_{OZL} Off-state output current, low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL\text{max}}$			-20			-20	μA		
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA		
I_{IH} High-level input current, any input	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA		
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_{IL} = 0.4 \text{ V}$			-0.2			-0.2	mA		
I_{OS} Short-circuit output current*	$V_{CC} = \text{MAX}$	-50		-225	-50		-225	mA		
I_{CC} Supply current	Outputs high			13	23		13	23	mA	
	Outputs low			26	44		26	44		
	Outputs open	All			27	46		27		46
		'LS240, 'LS241, 'LS244			29	50		29		50
		'LS240, 'LS241, 'LS244			32	54		32		54

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

* Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER	TEST CONDITIONS	'LS240			'LS241, 'LS244			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 45 \text{ pF}, R_L = 667 \Omega,$ See Note 2		9	14		12	18	ns
t_{PHL} Propagation delay time, high-to-low-level output			12	18		12	18	ns
t_{PZL} Output enable time to low level	$C_L = 5 \text{ pF}, R_L = 667 \Omega,$ See Note 2		20	30		20	30	ns
t_{PZH} Output enable time to high level			15	23		15	23	ns
t_{PLZ} Output disable time from low level			15	25		15	25	ns
t_{PHZ} Output disable time from high level			10	18		10	18	ns

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

TYPES SN54S240, SN54S241, SN74S240, SN74S241 BUFFERS/LINE DRIVERS/LINE RECEIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	SN54S*			SN74S*			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-12			-15	mA
Low-level output current, I_{OL}			48			64	mA
Operating free-air temperature, T_A (see Note 3)	-55		125	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
 3. An SN54S241J operating at free-air temperature above 116°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 40°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'S240			'S241			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage		0.8			0.8			V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.2			-1.2			V
Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$	0.2	0.4		0.2	0.4	V	
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -3 \text{ mA}$	2.4	3.4		2.4	3.4	V	
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.5 \text{ V}, I_{OH} = \text{MAX}$	2			2			V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = \text{MAX}$	0.55			0.55			V
I_{OZH} Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_O = 2.4 \text{ V}$	50			50			μA
I_{OZL} Off-state output current, low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_O = 0.5 \text{ V}$	-50			-50			μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	1			1			mA
I_{IH} High-level input current, any input	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$	50			50			μA
I_{IL} Low-level input current	Any A	-400			-400			μA
	Any G	-2			-2			mA
I_{OS} Short-circuit output current*	$V_{CC} = \text{MAX}$	-50	-225		-50	-225	mA	
I_{CC} Supply current	Outputs high	SN54S*	80	123	95	147	mA	
		SN74S*	80	135	95	160		
	Outputs low	SN54S*	100	145	120	170		
		SN74S*	100	150	120	180		
	Outputs disabled	SN54S*	100	145	120	170		
		SN74S*	100	150	120	180		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

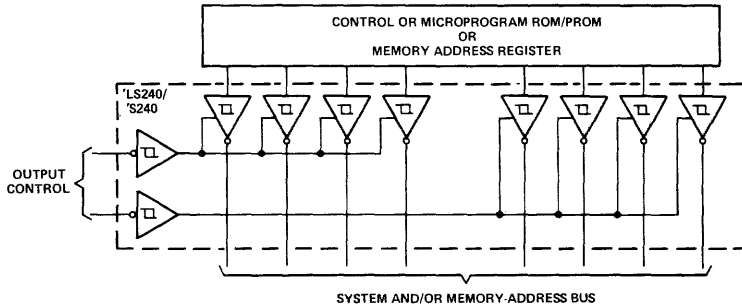
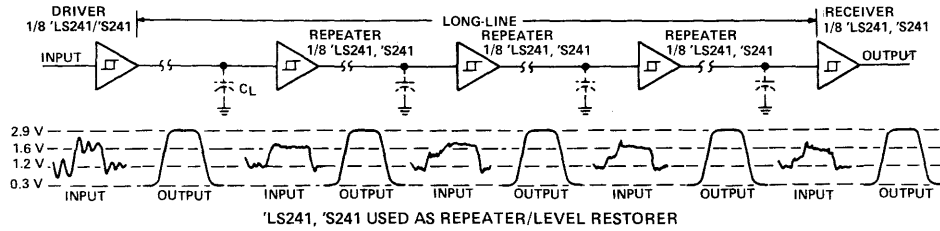
* Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER	TEST CONDITIONS	'S240			'S241			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 50 \text{ pF}, R_L = 90 \Omega,$ See Note 4	4.5		7	6		9	ns
t_{PHL} Propagation delay time, high-to-low-level output		4.5		7	6		9	ns
t_{PZL} Output enable time to low level		10		15	10		15	ns
t_{PZH} Output enable time to high level		6.5		10	8		12	ns
t_{PLZ} Output disable time from low level	$C_L = 5 \text{ pF}, R_L = 90 \Omega,$ See Note 4	10		15	10		15	ns
t_{PHZ} Output disable time from high level		6		9	6		9	ns

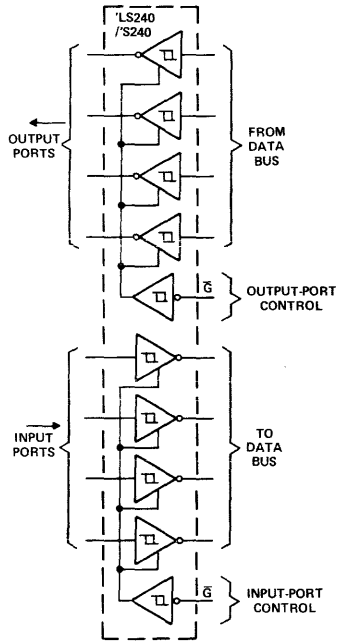
NOTE 4: Load circuit and voltage waveforms are shown on page 3-10.

**TYPES SN54LS240, SN54LS241,
SN54LS244, SN54S240, SN54S241, SN74LS240,
SN74LS241, SN74LS244, SN74S240, SN74S241
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

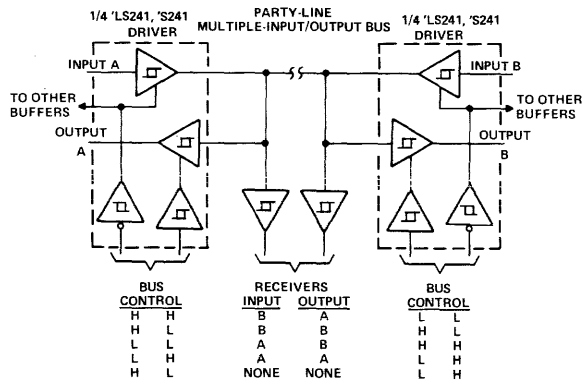


'LS241, 'S240 USED AS SYSTEM AND/OR MEMORY BUS DRIVER—4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD

6



INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



PARTY-LINE BUS SYSTEM WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS

TYPES SN54LS242, SN54LS243, SN74LS242, SN74LS243 QUADRUPLE BUS TRANSCEIVERS

- Two-Way Asynchronous Communication Between Data Buses
- P-N-P Inputs Reduce D-C Loading
- Hysteresis (Typically 400 mV) at Inputs Improves Noise Margin

description

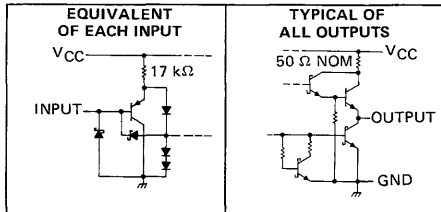
These four-data-line transceivers are designed for asynchronous two-way communications between data buses. The SN74LS' can be used to drive terminated lines down to 133 ohms.

FUNCTION TABLE (EACH TRANSCEIVER)

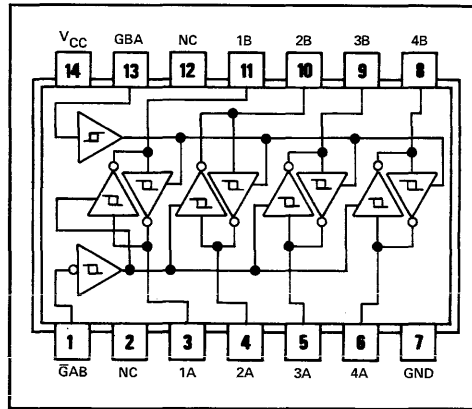
CONTROL INPUTS		'LS242 DATA PORT STATUS		'LS243 DATA PORT STATUS	
$\bar{G}AB$	GBA	A	B	A	B
H	H	\bar{O}	I	O	I
L	H	*	*	*	*
H	L	ISOLATED		ISOLATED	
L	L	I	\bar{O}	I	O

*Possibly destructive oscillation may occur if the transceivers are enabled in both directions at once.
I = Input, O = Output, \bar{O} = Inverting Output.

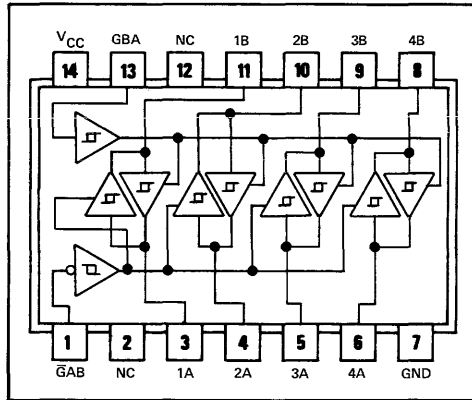
schematics of inputs and outputs



SN54LS242 ... J OR W
SN74LS242 ... J OR N
(TOP VIEW)



SN54LS243 ... J OR W
SN74LS243 ... J OR N
(TOP VIEW)



NC—No internal connection

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I _{OH}			-12			-15	mA
Low-level output current, I _{OL}			12			24	mA
Operating free-air temperature, T _A	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54LS242, SN54LS243, SN74LS242, SN74LS243 QUADRUPLE BUS TRANSCEIVERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS †	SN54LS*			SN74LS*			UNIT
			MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
	Hysteresis (V _{T+} - V _{T-})	V _{CC} = MIN	0.2	0.4		0.2	0.4		V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -3 mA	2.4	3.1		2.4	3.1		V
		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.5 V, I _{OH} = MAX	2			2			
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OL} = 24 mA					0.35	0.5	
I _{OZH}	Off-state output current, high-level voltage applied	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{IL} max, V _O = 2.7 V			20			20	μA
I _{OZL}	Off-state output current, low-level voltage applied	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{IL} max, V _O = 0.4 V			-200			-200	μA
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA
I _{IH}	High-level input current, any input	V _{CC} = MAX, V _I = 2.7 V			20			20	μA
I _{IL}	Low-level input current	A inputs	V _{CC} = MAX, V _I = 0.4 V, \bar{G} A and GBA at V _{IL} max		-0.2			-0.2	mA
		B inputs	V _{CC} = MAX, V _I = 0.4 V, \bar{G} A and GBA at 2 V		-0.2		-0.2		
		\bar{G} A or GBA	V _{CC} = MAX, V _I = 0.4 V		-0.2		-0.2		
I _{OS}	Short-circuit output current †	V _{CC} = MAX	-50	-225		-50	-225	mA	
I _{CC}	Supply current	Outputs high	V _{CC} = MAX, 'LS242, 'LS243	22	38		22	38	mA
		Outputs low	V _{CC} = MAX, 'LS242, 'LS243	29	50		29	50	
		All outputs open	V _{CC} = MAX, 'LS242	29	50		29	50	
		All outputs disabled	V _{CC} = MAX, 'LS243	32	54		32	54	

6

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

* Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with transceivers enabled in one direction only, or with all transceivers disabled.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	'LS242			'LS243			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX		
t _{PLH}	Propagation delay time, low-to-high-level output		9	14		12	18	ns	
t _{PHL}	Propagation delay time, high-to-low-level output	C _L = 45 pF, R _L = 667 Ω, See Note 3		12	18		12	18	ns
t _{PZL}	Output enable time to low level			20	30		20	30	ns
t _{PZH}	Output enable time to high level			15	23		15	23	ns
t _{PLZ}	Output disable time from low level	C _L = 5 pF, R _L = 667 Ω, See Note 3		15	25		15	25	ns
t _{PHZ}	Output disable time from high level			10	18		10	18	ns

NOTE 3: Load circuit and waveforms are shown on page 3-11.

TYPES SN54265, SN74265 QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

FOR SYMMETRICAL GENERATION OF COMPLEMENTARY TTL SIGNALS

- Switching Time Skew of the Complementary Outputs Is Typically 0.5 ns . . . Guaranteed to be No More than 3 ns at Rated Loading
- Full Fan-Out to 20 High-Level and 10 Low-Level 54/74 Loads
- Active Pull-Down Provides Square Transfer Characteristic

description

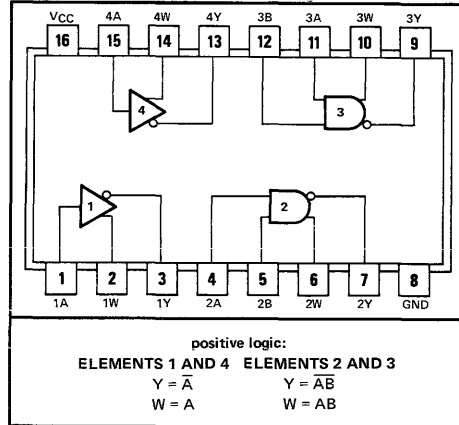
The SN54265 and SN74265 circuits feature complementary outputs from each logic element, which have virtually symmetrical switching time delays from the triggering input. They are designed specifically for use in applications such as:

- Symmetrical clock/clock generators
- Complementary input circuit for decoders and code converters
- Switch debouncing
- Differential line driver

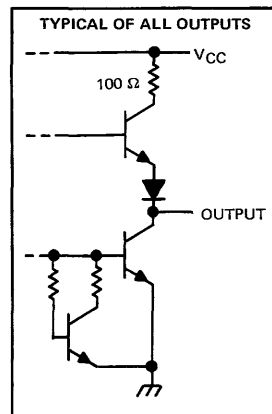
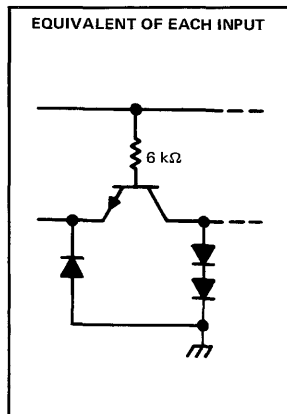
Examples of these four functions are illustrated in the typical application data.

The SN54265 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74265 is characterized for operation from 0°C to 70°C .

SN54265 . . . J OR W PACKAGE
SN74265 . . . J OR N PACKAGE
(TOP VIEW)



schematics of inputs and outputs



TYPES SN54265, SN74265 QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

recommended operating conditions

	SN54265			SN74265			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $I_{OH} = -800 \mu\text{A}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6	mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$, SN54265		-20	-57	mA
	SN74265		-18	-57	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 3		25	34	mA

6

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§]Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured with all outputs open and all inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}(W)$	A or B	W	$R_L = 400 \Omega$, $C_L = 15 \text{ pF}$, See Note 4		11.6	18	ns
$t_{PHL}(Y)$	(as applicable)	Y			11.3	18	
$t_{PHL}(W)$	A or B	W			9.8	18	ns
$t_{PLH}(Y)$	(as applicable)	Y			10.2	18	
$t_{PLH}(W) - t_{PHL}(Y)$	A or B	W with respect to Y			+0.3	+3	ns
$t_{PHL}(W) - t_{PLH}(Y)$	(as applicable)				-0.4	+3	

t_{PLH} \equiv Propagation delay time, low-to-high-level output.

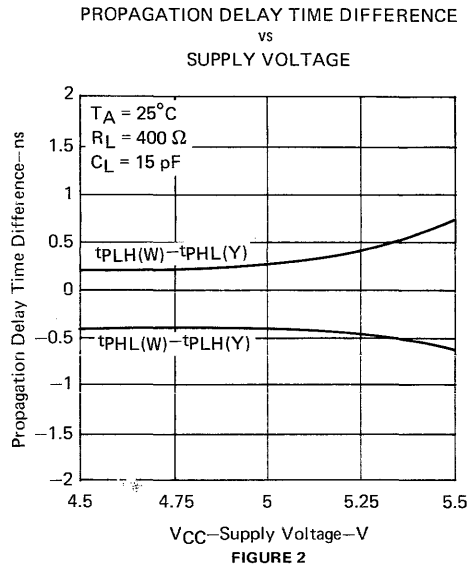
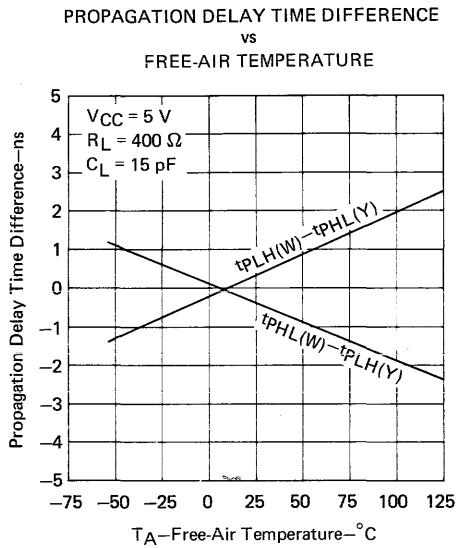
t_{PHL} \equiv Propagation delay time, high-to-low-level output.

$t_{PXX}(W) - t_{PXX}(Y)$ \equiv Difference in indicated propagation delay times at the W and Y outputs, respectively.

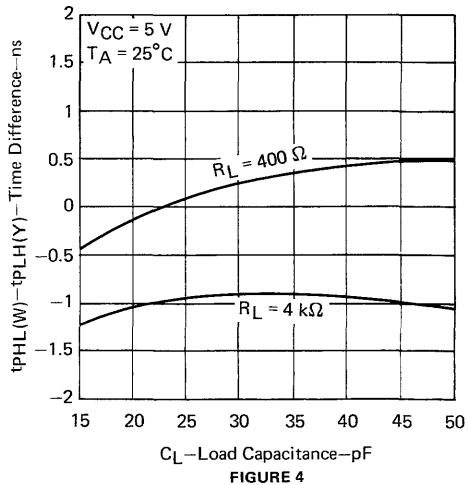
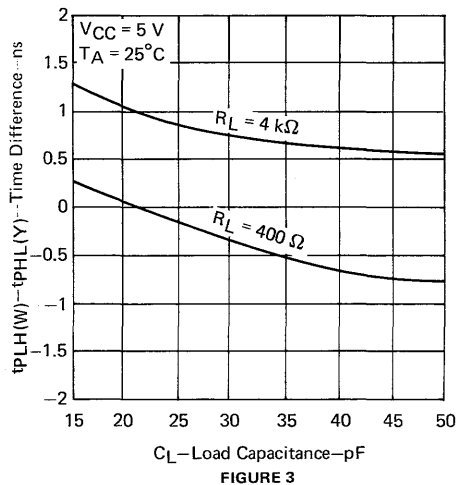
NOTE 4: Load circuit and voltage waveforms are shown on page 3-10.

TYPES SN54265, SN74265 QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

TYPICAL CHARACTERISTICS†



PROPAGATION DELAY TIME DIFFERENCE vs LOAD CAPACITANCE



6

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable for SN54265 only.

TYPES SN54265, SN74265
QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

TYPICAL APPLICATION DATA

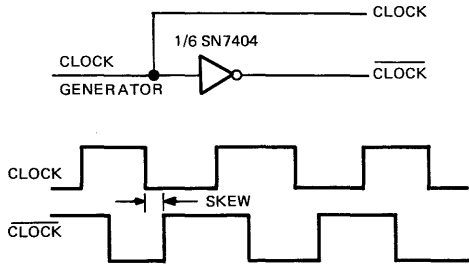


FIGURE A - TYPICAL CLOCK/ $\overline{\text{CLOCK}}$ GENERATOR CIRCUIT

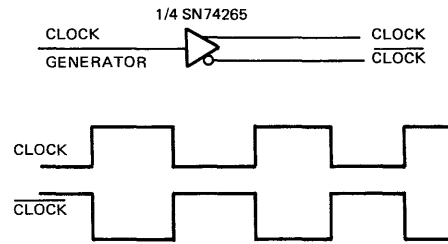


FIGURE B - SKEWLESS CLOCK/ $\overline{\text{CLOCK}}$ GENERATOR CIRCUIT

6

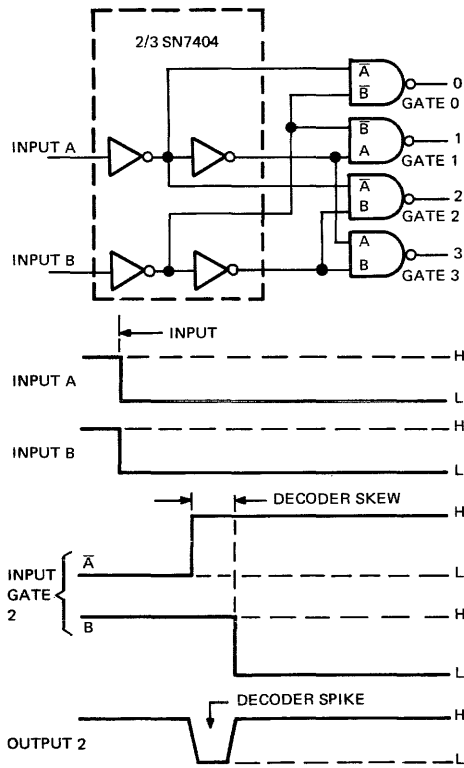


FIGURE C - TYPICAL DECODER/CODE CONVERTER

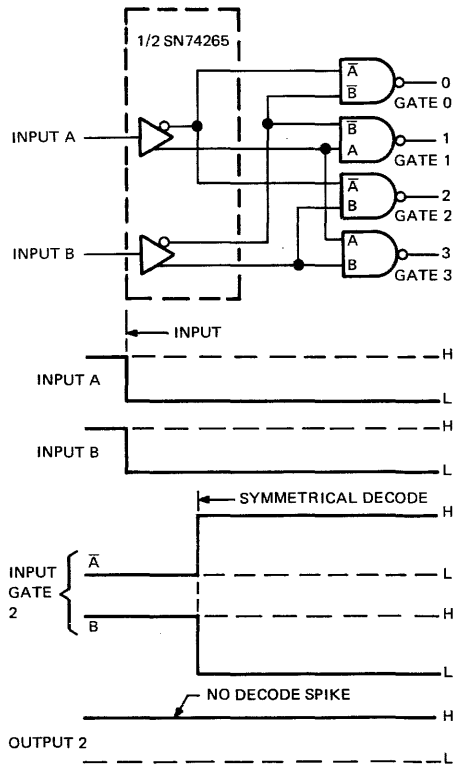


FIGURE D - SYMMETRICAL DECODER/CODE CONVERTER

TYPES SN54265, SN74265 QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

TYPICAL APPLICATION DATA

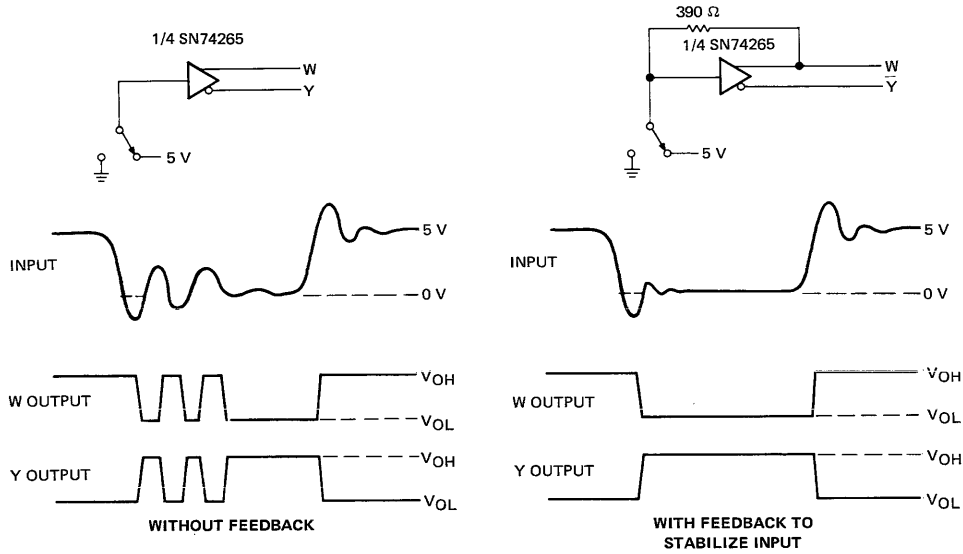
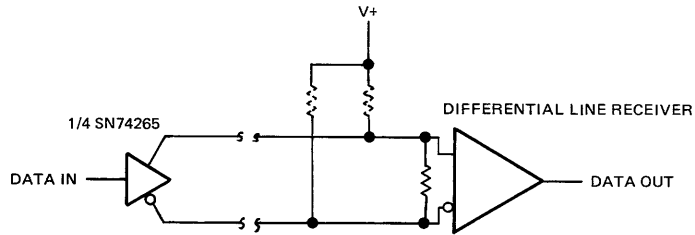


FIGURE E – SWITCH DEBOUNCER

6

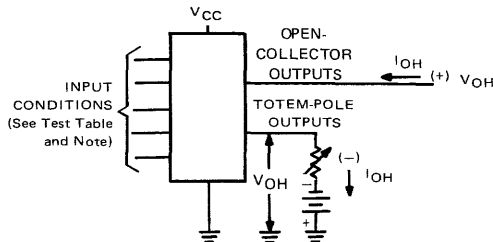


Noise immunity typically 3 V
for either high level or low level data

FIGURE F – DIFFERENTIAL LINE DRIVER

SERIES 54/74, 54H/74H, 54L/74L, 54LS/74LS, 54S/74S TRANSISTOR-TRANSISTOR LOGIC

PARAMETER MEASUREMENT INFORMATION

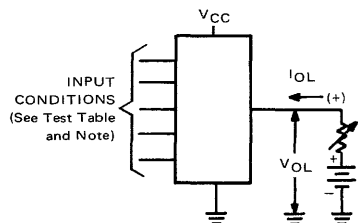


NOTE: For functions having three-state outputs, input conditions are maintained which will cause the outputs to be enabled (low-impedance).

FIGURE 1— V_{IH} , V_{IL} , V_{OH} , I_{OH}

TEST TABLE

FUNCTION	INPUT CONDITIONS
NAND	Input under test at V_{IL} max, all others at 4.5 V
AND	All inputs at V_{IH} min
NOR	All inputs at V_{IL} max
OR	Input under test at V_{IH} min, all others at GND
AND-OR-INVERT	Inputs under test (a set including one input of each AND gate) at V_{IL} max, all others at 4.5 V
AND-OR	All inputs of AND gate under test at V_{IH} min, all others at GND



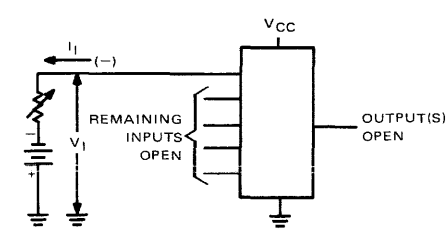
NOTE: For functions having three-state outputs, input conditions are maintained which will cause the outputs to be enabled (low-impedance).

FIGURE 2— V_{IH} , V_{IL} , V_{OL}

TEST TABLE

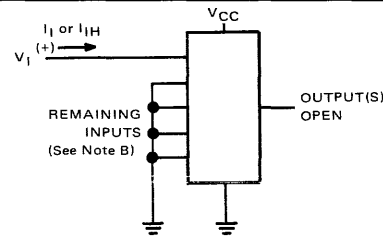
FUNCTION	INPUT CONDITIONS
NAND	All inputs at V_{IH} min
AND	Input under test at V_{IL} max, all others at 4.5 V
NOR	Input under test at V_{IH} min, others at GND
OR	All inputs at V_{IL} max
AND-OR-INVERT	All inputs of AND gate under test at V_{IH} min, all others at GND
AND-OR	Inputs under test (a set including one input of each AND gate) at V_{IH} min, all others at 4.5 V

6



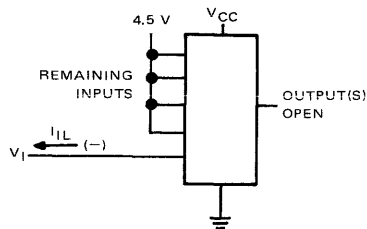
NOTE: Each input is tested separately.

FIGURE 3— V_{I1}



NOTES: A. Each input is tested separately.
B. When testing AND-OR-INVERT or AND-OR gates, each AND gate is tested separately with inputs of AND gates not under test open when testing I_{I1} and grounded when testing I_{IH} .

FIGURE 4— I_{I1} , I_{IH}

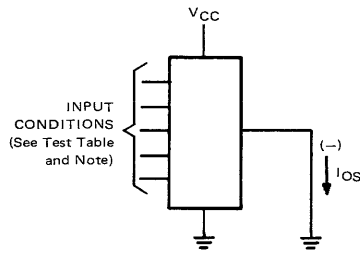


NOTES: A. Each input is tested separately.
B. When testing AND-OR-INVERT or AND-OR gates, each AND gate is tested separately with inputs of AND gates not under test open.

FIGURE 5— I_{I1L}

SERIES 54/74, 54H/74H, 54L/74L, 54LS/74LS, 54S/74S TRANSISTOR-TRANSISTOR LOGIC

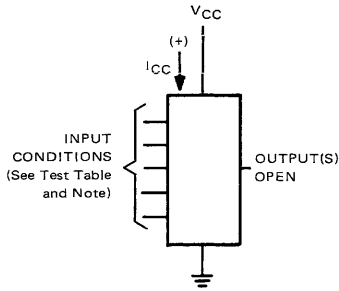
PARAMETER MEASUREMENT INFORMATION



TEST TABLE	
FUNCTION	INPUT CONDITIONS
NAND	All inputs at GND
AND	All inputs at 4.5 V
NOR	All inputs at GND
OR	All inputs at 4.5 V
AND-OR-INVERT	All inputs at GND
AND-OR	All inputs at 4.5 V

NOTE: For functions having three-state outputs, input conditions are maintained which will cause the outputs to be enabled (low-impedance).

FIGURE 6— I_{OS}



TEST TABLE		
FUNCTION	INPUT CONDITIONS FOR I_{CCH}	INPUT CONDITIONS FOR I_{CCL}
NAND	All inputs at GND	All inputs at 4.5 V
AND	All inputs at 4.5 V	All inputs at GND
NOR	All inputs at GND	One input at 4.5 V, all others at GND
OR	One input at 4.5 V, all others at GND	All inputs at GND
AND-OR-INVERT	All inputs at GND	All inputs of one AND gate at 4.5 V, all others at GND
AND-OR	All inputs of one AND gate at 4.5 V, all others at GND	All inputs at GND

NOTE: I_{CC} is measured simultaneously for all functions in a package. The average-per-gate values are calculated from the appropriate one of the following equations:

$$I_{CC}, I_{CCH}, \text{ or } I_{CCL} \text{ (average per gate or flip-flop)} = \frac{\text{total } I_{CC}, I_{CCH}, \text{ or } I_{CCL}}{\text{(number of gates or flip-flops in package)}}$$

$$I_{CC} \text{ (average per gate, 50\% duty cycle)} = \frac{I_{CCH} + I_{CCL}}{2 \text{ (number of gates in package)}}$$

FIGURE 7— I_{CC}

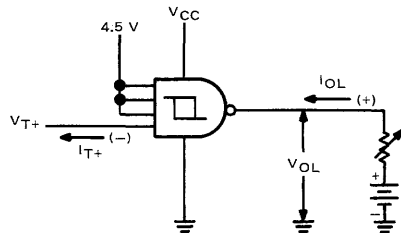


FIGURE 8— V_{T+} , I_{T+} , V_{OL} (FOR NAND SCHMITT TRIGGERS)

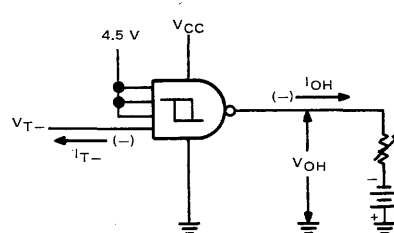
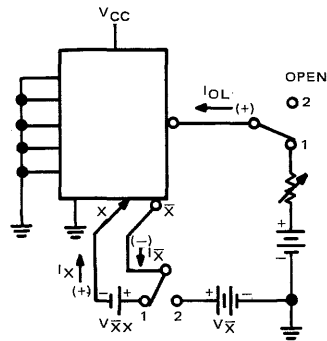


FIGURE 9— V_{T-} , I_{T-} , V_{OH} (FOR NAND SCHMITT TRIGGERS)

SERIES 54/74, 54H/74H, 54L/74L, 54LS/74LS, 54S/74S TRANSISTOR-TRANSISTOR LOGIC

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Switches are in position 1 for SN54'/SN74', position 2 for SN54H'/SN74H'.
- B. The $I_{\bar{X}}$ limit for SN54' and SN74' circuits may be verified by an alternate equivalent procedure. The $V_{\bar{X}X}$ source is replaced by a resistor (138 Ω for SN54', 130 Ω for SN74') in parallel with a voltmeter between the X and \bar{X} pins. If the measured voltage, $V_{\bar{X}X}$, is less than 0.4 V, the specified limit for $I_{\bar{X}}$ is met.

FIGURE 10— $I_{\bar{X}}$ (FOR EXPANDABLE GATES)

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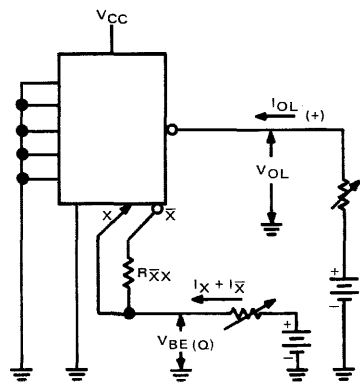


FIGURE 11— $V_{BE(Q)}$ (FOR EXPANDABLE GATES)

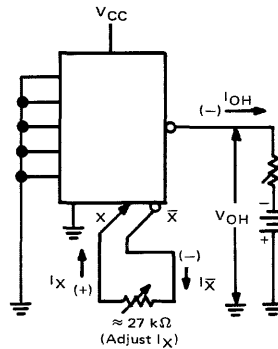


FIGURE 12— V_{OH} (FOR EXPANDABLE GATES)

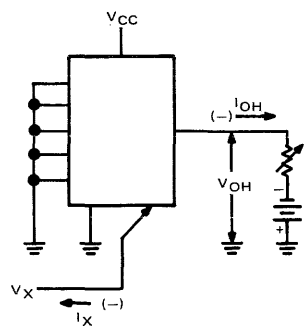


FIGURE 13— V_{OH} (FOR EXPANDABLE GATES)

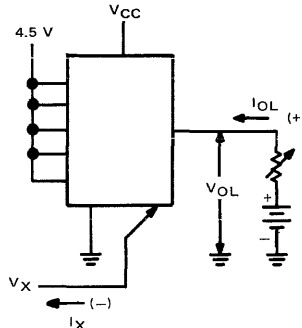


FIGURE 14— V_{OL} (FOR EXPANDABLE GATES)

**SERIES 54/74, 54H/74H, 54L/74L, 54LS/74LS, 54S/74S
TRANSISTOR-TRANSISTOR LOGIC**

PARAMETER MEASUREMENT INFORMATION

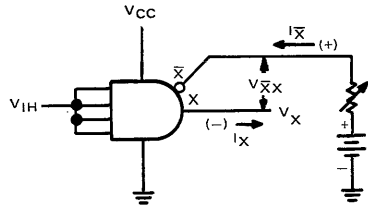


FIGURE 15—ON-STATE CHARACTERISTICS FOR EXPANDERS

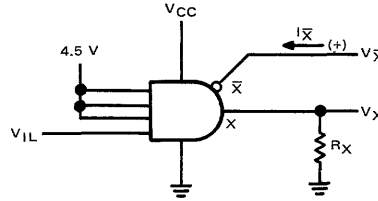


FIGURE 16—OFF-STATE CHARACTERISTICS FOR EXPANDERS

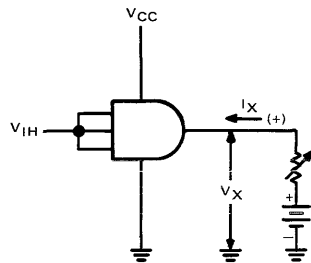


FIGURE 17—ON-STATE CHARACTERISTICS FOR EXPANDERS

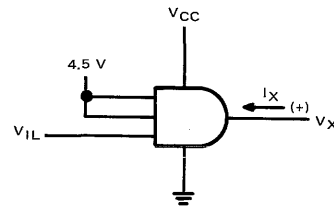
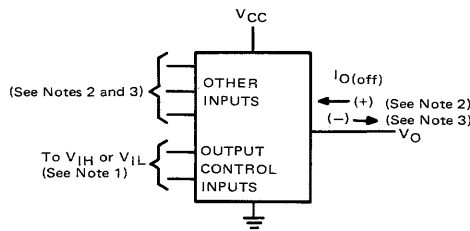


FIGURE 18—OFF-STATE CHARACTERISTICS FOR EXPANDERS

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- NOTES: 1. Input conditions are maintained which will ensure that the three-state output(s) is (are) disabled to the high-impedance state. See function table or logic for the particular device.
 2. When testing for current into the output with a high-level output voltage, input conditions are applied that would cause the output to be low if it were enabled.
 3. When testing for current out of the output with a low-level output voltage, input conditions are applied that would cause the output to be high if it were enabled.

FIGURE 19— $I_{O(off)}$ (THREE-STATE OUTPUTS)

SERIES 54/74 TRANSISTOR-TRANSISTOR LOGIC

TYPICAL CHARACTERISTICS†§

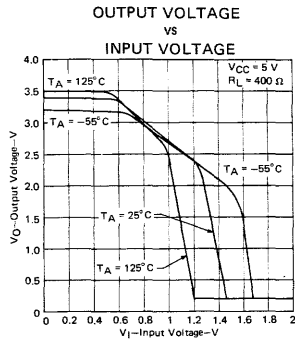


FIGURE A1

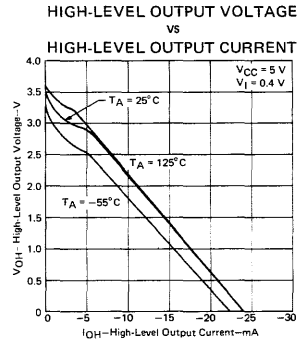


FIGURE A2

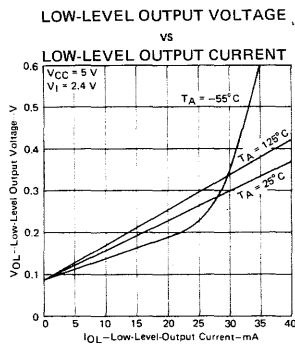


FIGURE A3

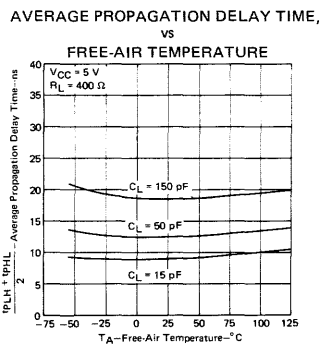


FIGURE A4

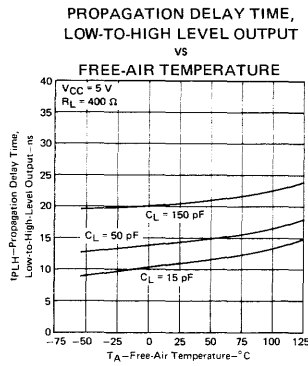


FIGURE A5

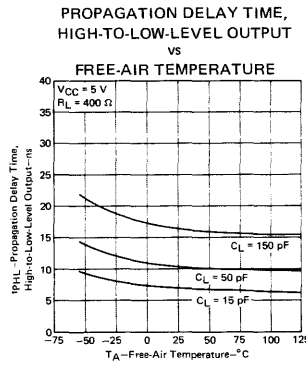


FIGURE A6

† Data for temperatures below 0°C and above 70°C are applicable for Series 54 circuits only.
§ Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

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SERIES 54H/74H

HIGH-SPEED TRANSISTOR-TRANSISTOR LOGIC

TYPICAL CHARACTERISTICS†§

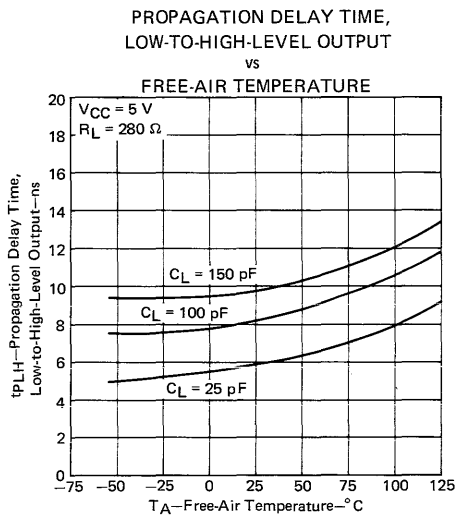


FIGURE B1

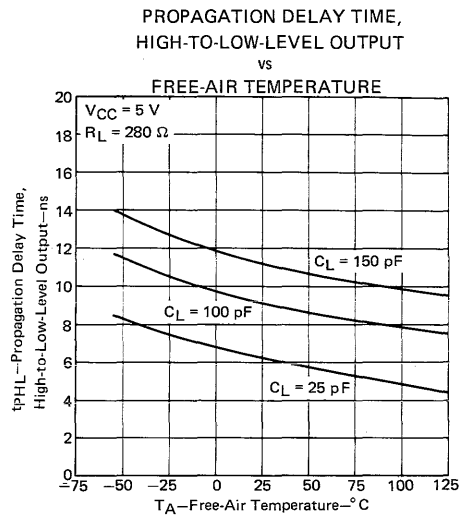


FIGURE B2

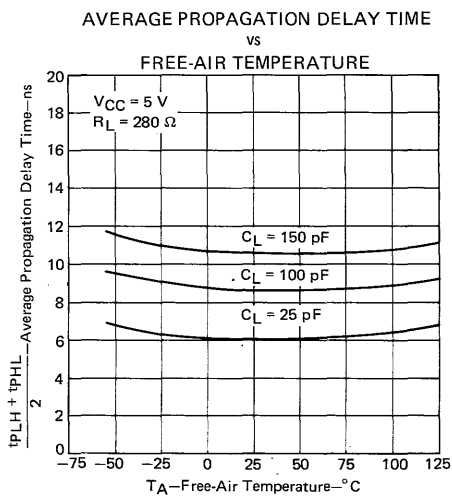


FIGURE B3

† Data for temperatures below 0°C and above 70°C are applicable for Series 54H circuits only.
§ Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

SERIES 54L/74L

LOW-POWER TRANSISTOR-TRANSISTOR LOGIC

TYPICAL CHARACTERISTICS†§

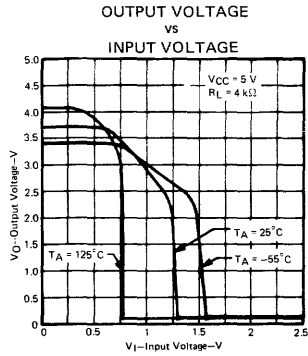


FIGURE C1

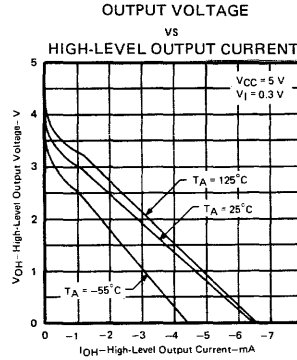


FIGURE C2

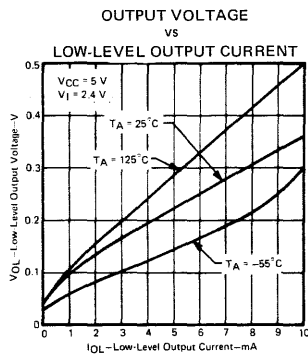


FIGURE C3

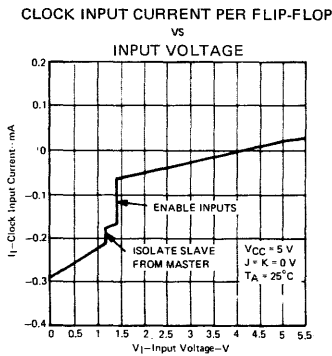


FIGURE C4

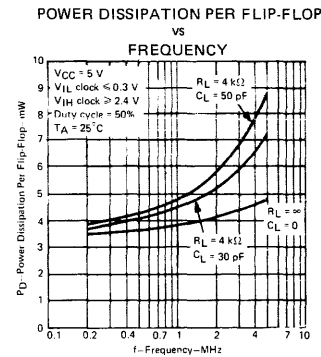


FIGURE C5

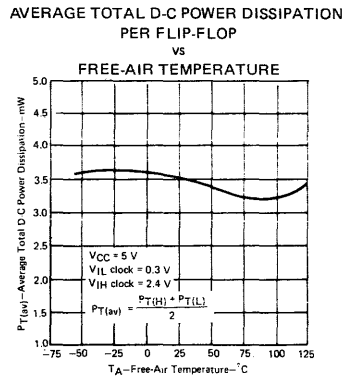


FIGURE C6

†Data for temperatures below 0°C and above 70°C are applicable for Series 54L circuits only.

§ Unless otherwise noted, data as shown are applicable specifically for the NAND gates with totem-pole outputs.

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SERIES 54L/74L LOW-POWER TRANSISTOR-TRANSISTOR LOGIC

TYPICAL CHARACTERISTICS†§

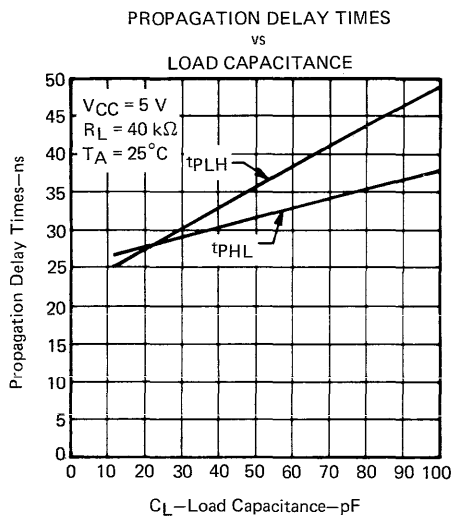


FIGURE C7

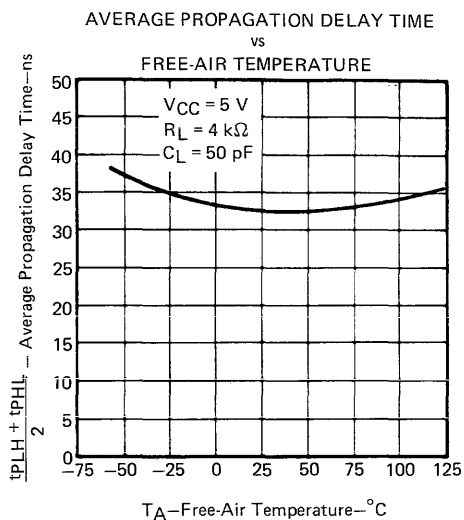


FIGURE C8

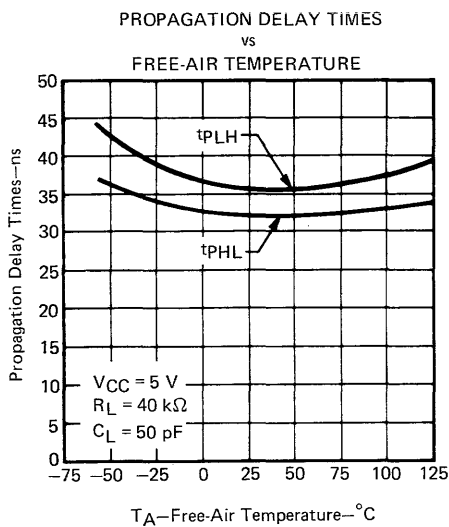


FIGURE C9

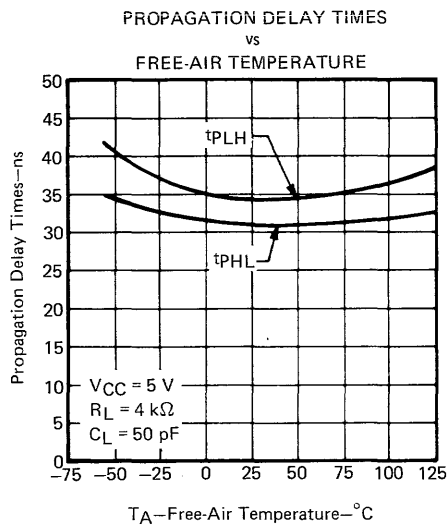


FIGURE C10

6

† Data for temperatures below 0°C and above 70°C are applicable for Series 54L circuits only.

§ Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

54LS/74LS SCHOTTKY-CLAMPED LOW-POWER TRANSISTOR-TRANSISTOR LOGIC

TYPICAL CHARACTERISTICS†§

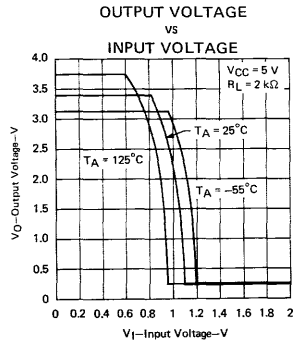


FIGURE D1

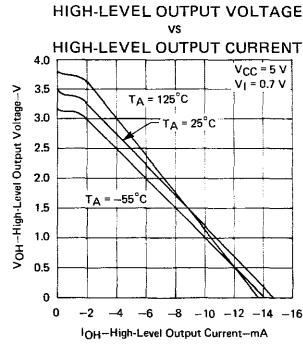


FIGURE D2

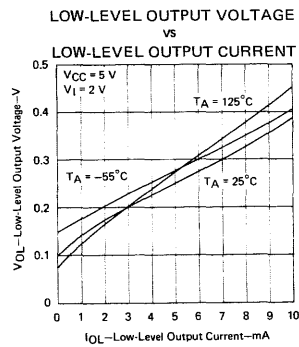


FIGURE D3

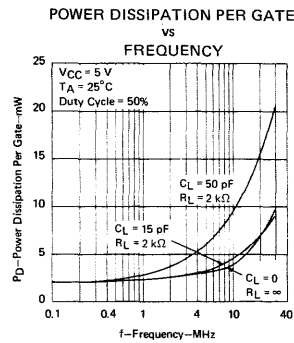


FIGURE D4

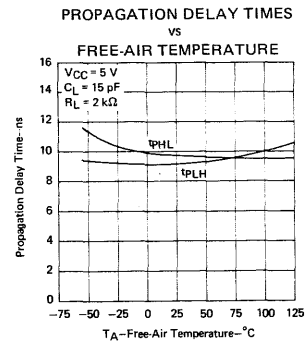


FIGURE D5

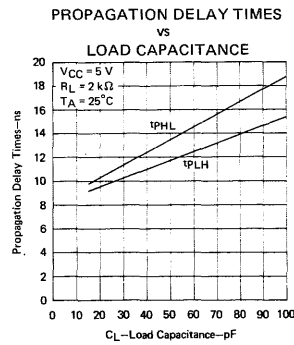


FIGURE D6

† Data for temperatures below 0°C and above 70°C are applicable for Series 54LS circuits only.
§ Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

6

SERIES 54S/74S

SCHOTTKY-CLAMPED TRANSISTOR-TRANSISTOR LOGIC

TYPICAL CHARACTERISTICS†§

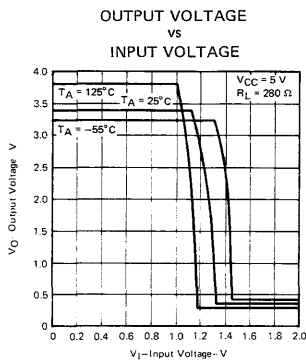


FIGURE E1

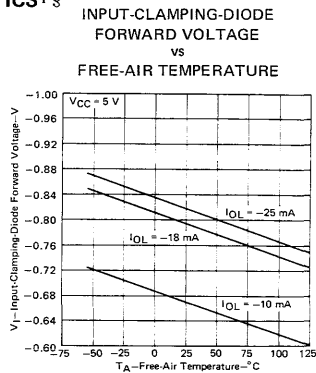


FIGURE E2

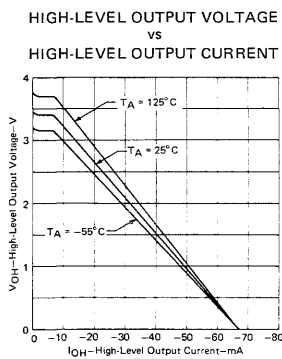


FIGURE E3

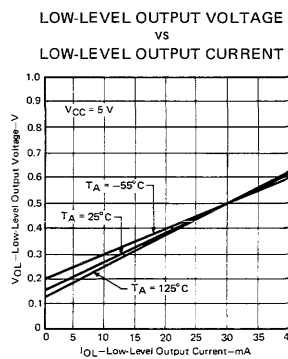


FIGURE E4

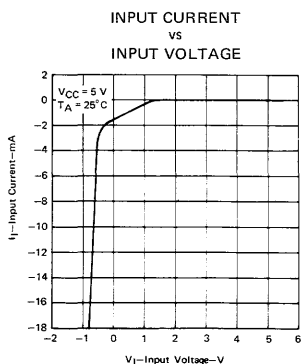


FIGURE E5

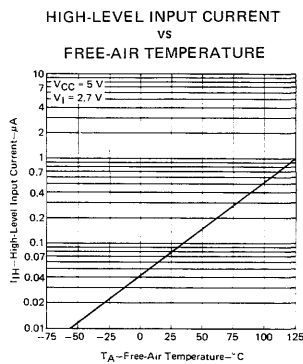


FIGURE E6

† Data for temperatures below 0°C and above 70°C are applicable for Series 54S circuits only.
§ Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

6

SERIES 54S/74S

SCHOTTKY-CLAMPED TRANSISTOR-TRANSISTOR LOGIC

TYPICAL CHARACTERISTICS†§

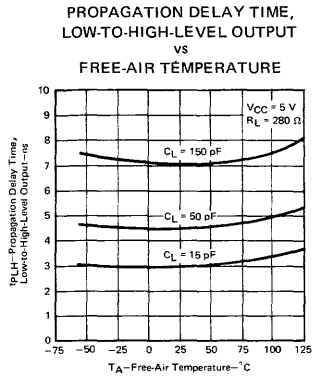


FIGURE E7

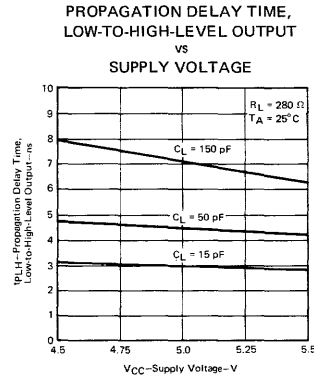


FIGURE E8

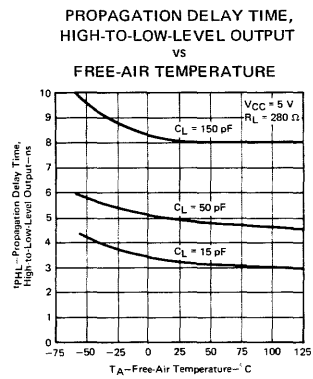


FIGURE E9

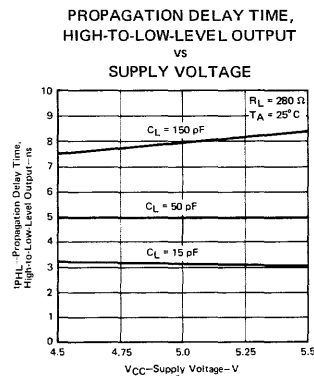


FIGURE E10

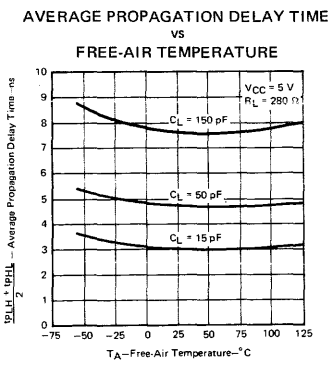


FIGURE E11

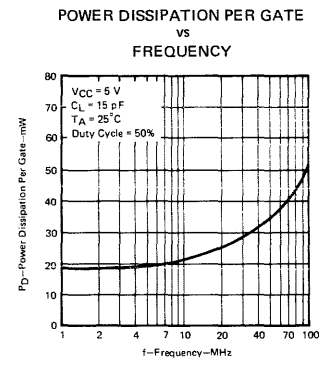


FIGURE E12

† Data for temperatures below 0°C and above 70°C are applicable for Series 54S circuits only.

§ Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

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SERIES 54S/74S SCHOTTKY-CLAMPED TRANSISTOR-TRANSISTOR LOGIC

TYPICAL CHARACTERISTICS FOR FLIP-FLOPS†

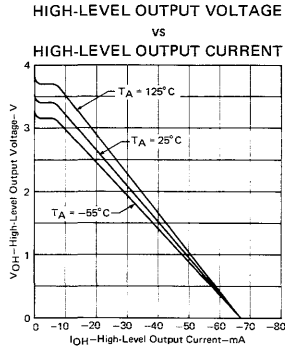


FIGURE E13

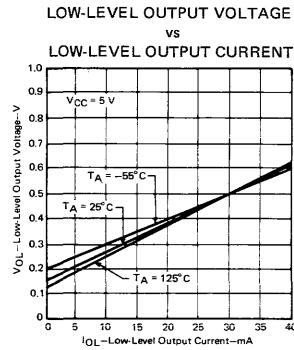


FIGURE E14

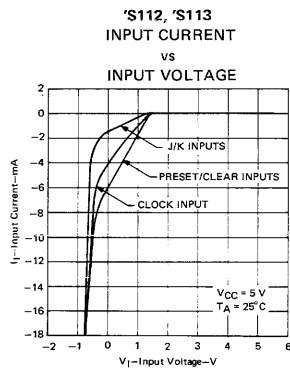


FIGURE E15

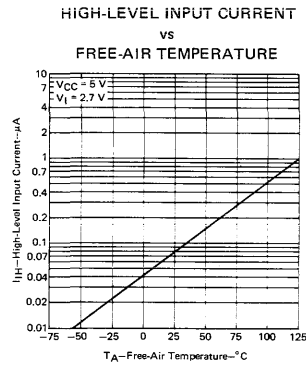


FIGURE E16

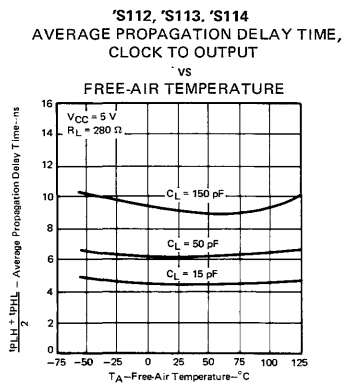


FIGURE E17

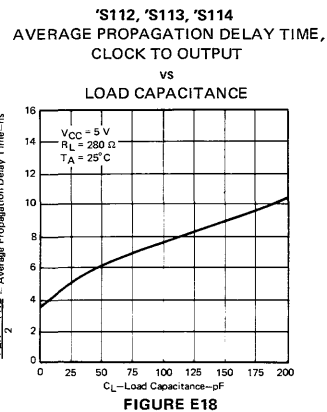


FIGURE E18

†Data for temperatures below 0°C and above 70°C are applicable for Series 54S circuits only.

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