STANDARD
MICROSYSTEMS
CORPORATION

PPC34C60

Parallel Port Interface Chip - Peripheral Side

FEATURES

- Creates PC/AT-Style Bus from Parallel Printer Port Signals
- Single Chip Interface to Any Bus Capable Peripheral
- Supports Standard, Bi-Directional, EPP, and ECP Parallel Ports
- Burst Mode for Improved Data Transfer Rates
- Adaptive Interface Optimizes Transfer Rates to Parallel Port Characteristics
- Digital Signal Filtering Increases Noise Immunity
- Allows Daisy-Chain of up to Eight Peripherals Including Standard Printer
- Provides Interrupt Sharing with Daisy-Chained Devices
- 16-Bit Product ID Support
- Peripheral Bus Clock Selectable at System Clock /2, /3, /5, or /6
- Interfaces to 8-Bit and/or 16-Bit Peripherals
- FIFO Operation Permits Overlapping Parallel Port and Peripheral Bus Cycles for Maximum Data Transfer Rate
- Flexible DRAM Buffer Support and DMA Capability
- Four Output Lines Individually Configurable as Chip Selects or General Purpose Outputs
- Three Output Lines Individually Configurable as Strobes or General Purpose Outputs
- Four Uncommitted Inputs
- Watchdog Monitors Host Computer Activity
- Low Battery Detect Input
- Direct Output for Piezo Transducer
- Support for Automatic Power Up/Down
- Prevents Host System Latchup with Powerback Control
- On Chip Crystal Oscillator

GENERAL DESCRIPTION

The PPC34C60 provides a means of re-generating an IBM® AT® style (ISA) bus from the PC printer port signals. In addition to Standard (Compatible) printer ports, the PPC34C60 supports PS/2® (bi-directional), EPP, and ECP ports. Up to eight peripherals may be daisy chained between the computer and the printer. Printer operation is unaffected.

The PPC34C60 performs as an intelligent data mux. It multiplexes the printer port signals between the daisy chain (pass-through) outputs and there-generated ISA bus. Furthermore, it handles breaking up 8- and 16-bit ISA data into 4- or 8-bit chunks for the parallel port.

The PPC34C60 also provides a piezo transducer driver for battery-powered systems. The transducer will signal low battery with two repeated beeps. If the cable to the computer is disconnected, or if the host is dormant for about a minute, the transducer will signal inactivity with four beeps. Additionally, a power-down signal can be provided to external circuitry to automatically shut down system power during inactivity.

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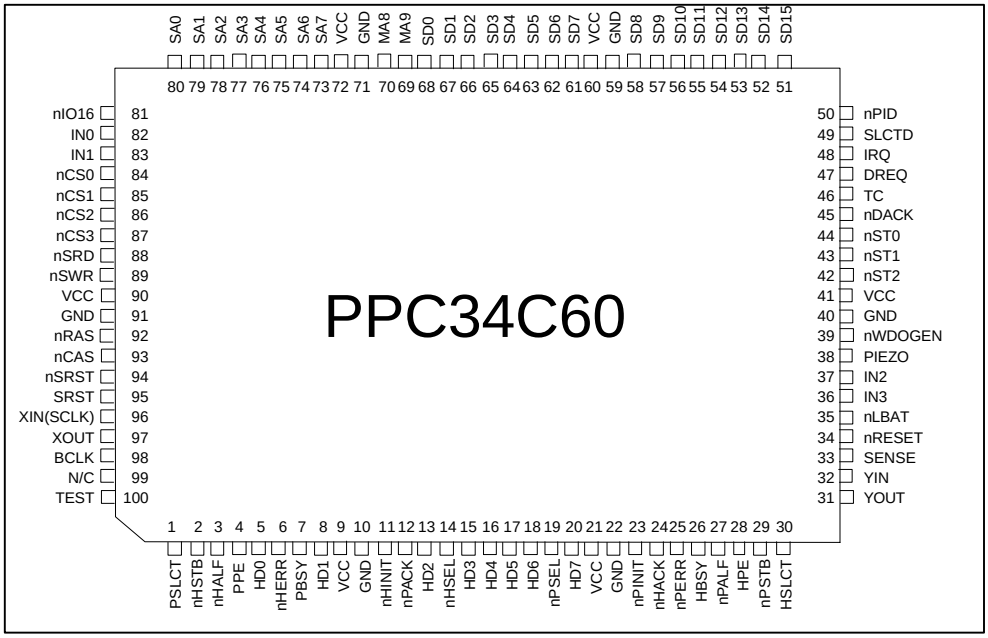
PIN CONFIGURATION



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
PARALLEL PORT HOST CONTROL AND COMMON DATA BUS INTERFACE				
2	nHost:Strobe	nHSTB	I,PU	An active low pulse on this input is used to strobe printer data into the printer. Refer to Section 4 of the IEEE STD 1284 (Reference 1) for use of this pin in ECP and EPP modes.
3	nHost:Auto Line Feed	nHALF	I,PU	This input goes low to cause the printer to automatically feed one line after each line is printed. Connects to AUTOFD output from Host. Refer to Section 4 of the IEEE STD 1284 (Reference 1) for use of this pin in ECP and EPP modes.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
14	nHost:SelectIn	nHSEL	I	This active low input is driven by the host to select the printer. Connects to SELECT IN output from Host. Refer to Section 4 of the IEEE STD 1284 (Reference 1) for use of this pin in ECP and EPP modes. (See Note 1 on Page 11.)
11	nHost:Initiate	nHINIT	I	This active low input initiates the printer when low. Connects to INIT output from Host. Refer to Section 4 of the IEEE STD 1284 (Reference 1) for use of this pin in ECP and EPP modes. (See Note 1 on Page 11.)
24	nHost: Acknowledge	nHACK	O16	This active low output from the printer is used to indicate that the printer has received the data and is ready to accept new data. Connects to the ACK input to the Host. Refer to Section 4 of the IEEE STD 1284 (Reference 1) for use of this pin in ECP and EPP modes.
26	Host:Busy	HBSY	O16	This status output, generated by the printer, goes high to indicate that it is not ready to receive new data from the host. Connects to the BUSY input to the Host. Refer to Section 4 of the IEEE STD 1284 (Reference 1) for use of this pin in ECP and EPP modes.
28	Host:Paper End	HPE	O16	This status output, generated by the printer, goes high to indicate that the printer is out of paper. Connects to the PERROR input to the Host. Refer to Section 4 of the IEEE STD 1284 (Reference 1) for use of this pin in ECP and EPP modes.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
30	Host:Printer Selected	HSLCT	O16	This status output, generated by the printer, goes high to indicate that the printer is selected. Connects to the SELECT input to the Host. Refer to Section 4 of the IEEE STD 1284 (Reference 1) for use of this pin in ECP and EPP modes.
6	nHost:Printer Error	nHERR	O16	This status output, generated by the printer, goes low to indicate an error condition at the printer. Connects to the ERROR input to the Host. Refer to Section 4 of the IEEE STD 1284 (Reference 1) for use of this pin in ECP and EPP modes.
5,8,13,15 -18, 20	Host:Data[0:7]	HD[0:7]	I/O16, PU	Parallel port bi-directional data bus connected to host system is used by SPP, ECP and EPP to transfer data between the host CPU and peripherals. Refer to Section 4 of the IEEE STD 1284 (Reference 1) for use of this pin in ECP and EPP modes.
PARALLEL PORT PASS-THROUGH INTERFACE PINS				
29	nPass-Through: Strobe	nPSTB	O16	An active low pulse on this output is used to strobe printer data into the printer. Connects to the STROBE input on the next device along the chain. Refer to Section 4 of the IEEE STD 1284 (Reference 1) for use of this pin in ECP and EPP modes.
27	nPass-Through: Auto Line Feed	nPALF	O16	This output goes low to cause the printer to automatically feed one line after each line is printed. Connects to the AUTOFD input on the next device along the chain. Refer to Section 4 of the IEEE STD 1284 (Reference 1) for use of this pin in ECP and EPP modes.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
19	nPass-Through: SelectIn	nPSEL	O16	This active low output selects the printer. Connects to the SELECT IN input on the next device along the chain. Refer to Section 4 of the IEEE STD 1284 (Reference 1) for use of this pin in ECP and EPP modes.
23	nPass-Through: Initiate	nPINIT	O16	This active low output initiates the printer when low. Connects to the INIT input on the next device along the chain. Refer to Section 4 of the IEEE STD 1284 (Reference 1) for use of this pin in ECP and EPP modes.
12	nPass-Through: Acknowledge	nPACK	I, PU	This active low input from the printer is used to indicate that the printer has received the data and is ready to accept new data. Connects to the ACK output from the next device along the chain. Refer to Section 4 of the IEEE STD 1284 (Reference 1) for use of this pin in ECP and EPP modes.
7	Pass-Through: Busy	PBSY	I, PU	This status input, generated by the printer goes high to indicate that it is not ready to receive new data from the Pass-Through. Connects to the BUSY output from the next device along the chain. Refer to Section 4 of the IEEE STD 1284 (Reference 1) for use of this pin in ECP/EPP modes.
4	Pass-Through: Paper End	PPE	I, PU	This status input, generated by the printer, goes high to indicate that the printer is out of paper. Connects to the PERROR output from the next device along the chain. Refer to Section 4 of the IEEE STD 1284 (Reference 1) for use of this pin in ECP and EPP modes.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Pass-Through: Printer Selected	PSLCT	I, PU	This status input, generated by the printer, goes high to indicate that the printer is selected. Connects to the SELECT output from the next device along the chain. Refer to Section 4 of the IEEE STD 1284 (Reference 1) for use of this pin in ECP/EPP modes.
25	nPass-Through: Printer Error	nPERR	I, PU	This status output, generated by the printer, goes low to indicate an error condition at the printer. Connects to the ERROR output from the next device along the chain. Refer to Section 4 of the IEEE STD 1284 (Reference 1) for use of this pin in ECP and EPP modes.
SYSTEM (REGENERATED ISA PERIPHERAL) INTERFACE				
96 97	System Clock/Crystal	XIN (SCLK) XOUT	I O8	XIN may be connected to a ttl peripheral system clock or a crystal may be placed across XIN/XOUT (typically 24MHz). This is used to derive the internal clock (BUSCLK) used for all system interface timing.
80-73	System Address [0:7]	SA[0:7]	O8	These lower eight address bits are presented to the system bus directly by the PPC34C60 during bus and DRAM access. Upper address bits, if needed, should be latched through use of the PPC34C60's strobe lines prior to generating bus accesses.
70,69	Memory Address [8,9]	MA[8:9]	O8	These address bits are appended to SA[0:7] to create a 10-bit row or column address for DRAM access.
68-61, 58-51	System Data [0:15]	SD[0:15]	I/O8, PU	These bi-directional pins are used to transfer data during bus or DRAM cycles to or from the system.
88	nSystem Read	nSRD	O8	This indicates that a bus read cycle is occurring, similar to an ISA MEMR signal.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
89	nSystem Write	nSWR	O8	This indicates that a bus write cycle is occurring, similar to an ISA MEMW signal.
81	n16-Bit I/O	nIO16	I, PU	This signal is asserted by the remote system to indicate whether or not the address being accessed is capable of a 16-bit transfer.
48	Interrupt Request	IRQ	I, PU	This rising edge activated signal indicates an interrupt request from the System.
94	nSystem Reset	nSRST	O8	This low going signal can be used to reset the System. This signal is asserted for 16 SCLKs.
95	System Reset	SRST	O8	This high going signal can be used to reset the System. This signal is asserted for 16 SCLKs.
92	nRow Address Strobe	nRAS	O8	This low going strobe signal is used by the DRAM to latch the row address, present on the SA[0:7] and MA[8:9] pins. This output drives the DRAM directly, however a series resistor is recommended on this line.
93	nColumn Address Strobe	nCAS	O8	This low going strobe signal is used by the DRAM to latch the column address, present on the SA[0:7] and MA[8:9] pins. This output drives the DRAM directly, however a series resistor is recommended on this line.
45	nDMA Acknowledge	nDACK	O8	This active low output signal is issued to inform the System that data is to be transferred using DMA transfer cycles.
46	Terminal Count	TC	O8	This active high output is asserted with the last DMA data transfer to indicate to the System that the DMA data transfer is complete. TC is asserted in conjunction with DACK.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
47	DMA Request	DREQ	I, PD	The remote system indicates that it is ready to perform DMA transfers by driving this line high. This signal is asserted as long as the System is ready to receive or send data and is deasserted on the last byte of the data transfer.
MISCELLANEOUS				
39	nWatchdog Enable	nWDOGEN	I, PU	Pulling this line low enables the watchdog. The watchdog will generate four beeps on the piezo driver if there are no transitions on the host port lines for a minute. This circuitry can also automatically power down the system when the watchdog "barks". This feature requires software to tickle the port every 30 seconds.
34	nReset Chip	nRESET	I, PU	Pulling this line low for two SYSCLKs will reset the PPC34C60 to its initial state. This will reset all internal registers to their default values.
35	nLow Battery Indicator	nLBAT	I, PU	A low level on this input line signals that the battery power is low and the PPC34C60 will generate low battery tones. It is the responsibility of the remote system to monitor battery power and generate this input signal.
82,83, 37,36	General Purpose Inputs [0:3]	IN[0:3]	I, PU	The host may obtain the level at these pins by reading the Internal Input Register.
38	Piezo Crystal Drive	PIEZO	O24	This high current output can be directly hooked up to a piezo speaker to provide audio tones.
44,43, 42	nStrobes[0:2] (special function)	nST[0:2]	O8	These pins are individually configured as general purpose outputs or as strobe outputs as programmed in the Output Configuration Register. ST2 may also be programmed as the Auto-Power pin.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
84-87	nChip Selects[0:3] (special function)	nCS[0:3]	O8	These pins are individually configured as general purpose outputs or as chip select outputs as programmed in the Output Configuration Register.
32 31	Oscillator Input Oscillator Output	YIN YOUT	I 08	A parallel resonant crystal or RC network may be placed across YIN and YOUT. This nominal 32KHz clock (32.768KHz) is used by the internal piezo driver and watchdog timer.
49	Selected Device	SLCTD	O8	This signal is an active high output that indicates that the device is the active device on the daisy chain. This may be used for debug purposes, to enable drivers, or to qualify signals.
50	nProduct ID	PID	O8	This signal is an active low output asserted when the host performs a request for the peripheral's Product ID. This function is used by the daisy chain and multiplexor protocols.
33	Sense VCC	SENSE	I, PD	When pulled high, this input will enable all output drivers of the PPC34C60. When low, all outputs are tri-stated. This resolves the back-power problem inherent in parallel port peripherals. Isolate the chip's VCC from the rest of the peripheral's VCC using a schottky diode. The SENSE input should be tied to the peripheral's VCC and the anode of the diode. In this manner, when the peripheral's power is off, the sense input will shut down all outputs, preventing the chip from driving into a low impedance load and consequently damaging the chip's input protection diodes.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
100	Test Counters	TEST	I, PD	This is an active high signal that allows access to some large counter chains that are normally buried within the chip. For normal operation this input should be left unconnected, or tied to ground. For more information on the test mode contact the factory.
98	BUSCLK	BCLK	O8	BUSCLK is the SCLK divided by the value programmed in the Configuration Register.
99	Reserved	RESERVED		Leave floating, no connection
9,21, 41,60, 72,90	Power	VCC		+5 Volt supply pins.
10,22, 40,59, 71,91	Ground	GND		Ground pins

Note 1: By pulling both these lines low (illegal state), the PPC34C60's output ports can be disabled.

BUFFER TYPE DESCRIPTIONS

BUFFER TYPE	DESCRIPTION
I	Input, Schmitt Trigger
I/O8	Input, Schmitt Trigger/8mA Output
I/O16	Input, Schmitt Trigger/16mA Output
O8	8mA Output
O16	16mA Output
O24	24mA Output
PU	Pull Up, nominal 100K
PD	Pull Down, nominal 100K

GENERAL CONVENTIONS

Throughout this document, the following various terms and conventions will be used:

Compatible = "Centronics"

SPP = "Standard Bi-Directional Parallel Port" (PS/2)

EPP = "Enhanced Parallel Port"

ECP = "Extended Capabilities Port"

REFERENCE DOCUMENTS

1. IEEE STD 1284, February 2, 1993.
2. The Enhanced Parallel Port, an Introduction; FarPoint Communications.
3. Daisy Chain Specification, Rev. 1.1, September 16, 1993; Disctec Corporation.
4. Enhanced Parallel Port BIOS Specification, Rev 3, February 12, 1993; FarPoint Communications.
5. ECP: Specification Kit, Rev 1.03, February 10, 1993; Microsoft Corporation.

FUNCTIONAL DESCRIPTION

PPC34C60 BLOCK DESCRIPTION

The PPC34C60 can be broken down into eight functional blocks as shown in Figure 1.

The PPC34C60 implements and complies with the Daisy Chain Specification (Reference 3) through the Daisy Chain Protocol block. Under the Daisy Chain protocol, the PPC34C60 operates in either Pass-Through or Selected mode. Pass-Through mode is the power up default, and is electrically transparent to devices further down the chain. When in Pass-Through mode, the Data Switch gates the control and status lines of the parallel port to the Pass-Through port. Selected mode connects the System Interface bus to the parallel port. When in Selected mode, the Data Switch gates the control and status lines to the PPC34C60's Protocol Translator functional block.

The Protocol Translator block gives the PPC34C60 its capability to communicate with the parallel port in either SPP, EPP, or ECP mode. The Protocol Translator interprets the Multiport Access Protocol (MAP) packets described in the Daisy Chain Specification (Reference 3). The MAP packets and command codes are described in the Daisy Chain Command Protocol. The Protocol Translator also decodes the type of parallel port transfer (ie. Address Write/Data Read_Write Cycle) and provides the proper control of the data to the Registers and Control block and to the Bus Interface block. The PPC34C60's internal registers, contained in the Register and Control block, control the operation of the chip's internal DRAM Controller, DMA Controller, and Watchdog Controller. The Bus Interface block controls data transfers between the Parallel Port and the peripheral's System Interface Bus. The MUX block routes data and control signals to the System Interface.

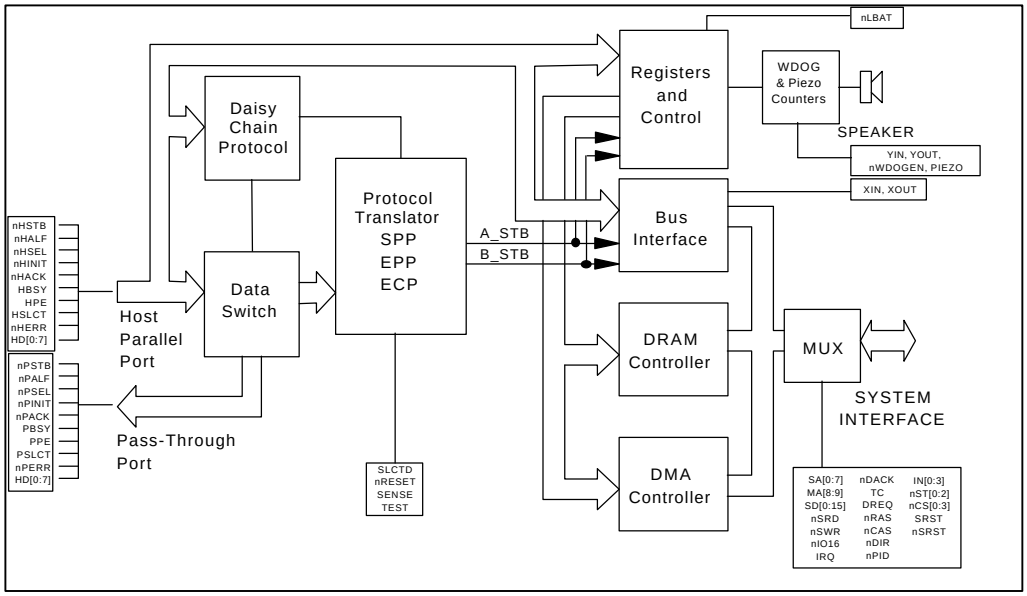


FIGURE 1 – INTERNAL BLOCK DIAGRAM

DAISY CHAIN COMMAND PROTOCOL

The daisy chain protocol is used to select the mode of each device and to allow connection of up to eight devices on one parallel port. The daisy chain commands use the Multiport Access Protocol (MAP) to access the devices. The format of the MAP packets is as follows:

The command byte in the MAP packet represents a code and possibly an address as well. The currently defined codes are:

(00-07)	**0000 0aaa**	Assign address aaa to the current device
(08-0F)	**0000 1aaa**	Query Interrupt from device aaa
(10-17)	**0001 0aaa**	Query Product ID from device aaa
(20-27)	**0010 0aaa**	Select device aaa in EPP mode
(30)	**0011 xxxx**	De-select all devices
(40)	**0100 0xxx**	Disable Daisy Chain Interrupts
(48)	**0100 1xxx**	Enable Daisy Chain Interrupts
(50-57)	**0101 0aaa**	Clear Interrupt Latches on device aaa
(58-5F)	**0101 1aaa**	Set Interrupt Latch on device aaa
(D0-D7)	**1101 0aaa**	Select device aaa in ECP mode
(E0-E7)	**1110 0aaa**	Select device aaa in Compatible Mode - SPP

aaa = Device Address

xxx = Undefined - set to zero

Refer to the Daisy Chain Specification (Reference 3) for more information.

PERIPHERAL SYSTEM DESIGN

The PPC34C60 simplifies the design of a peripheral to exploit the benefits of IEEE STD 1284, Standard Signaling for a Bi-Directional Parallel Port (Reference 1). Figure 2 depicts a high-level System Block Diagram which shows the peripheral chip's three primary data paths.

Note that the Parallel Port Data Bus is not switched through the PPC34C60; this allows all daisy chained devices to receive a special "out of band" Control Packet as defined in the Distec Daisy Chain Specification (Reference 3).

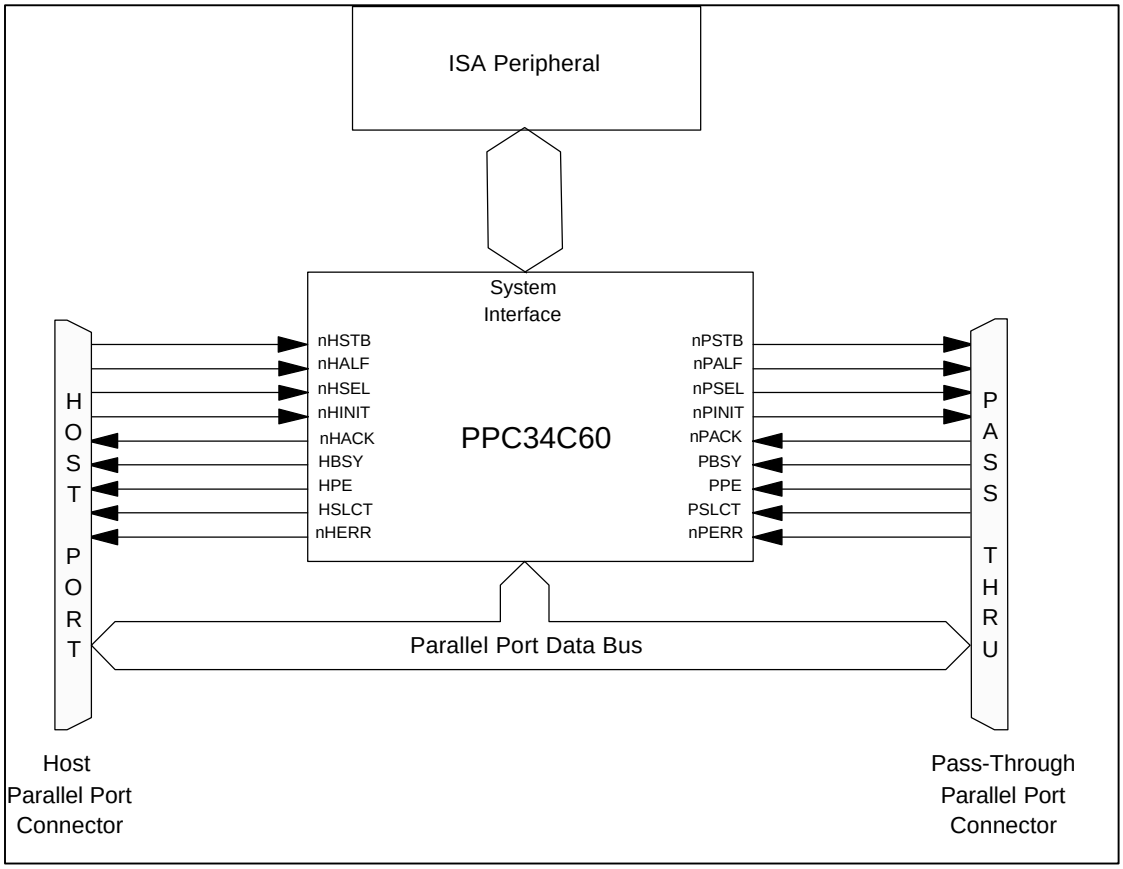


FIGURE 2 – SYTEM BLOCK DIAGRAM

DESIGN EXAMPLE

Figure 3 shows a simple system design that uses most of the PPC34C60's interface functions. This example shows:

1) A DRAM interface.

2) An 8Kx8 NV-memory device interface using nStrobe Output 0 to latch the upper address bits and nChip Select Output 0 to enable the device.

3) An interface to SMSC's FDC37C662 Super I/O Floppy Disk Controller. This section of the design illustrates how the PPC34C60 can handle a direct memory access interface, four interrupts, and an additional chip select output configured as a standard output pin. The SRST (reset output) is used to reset the floppy disk controller.

4) The use of 10K bias resistors to implement a product ID code.

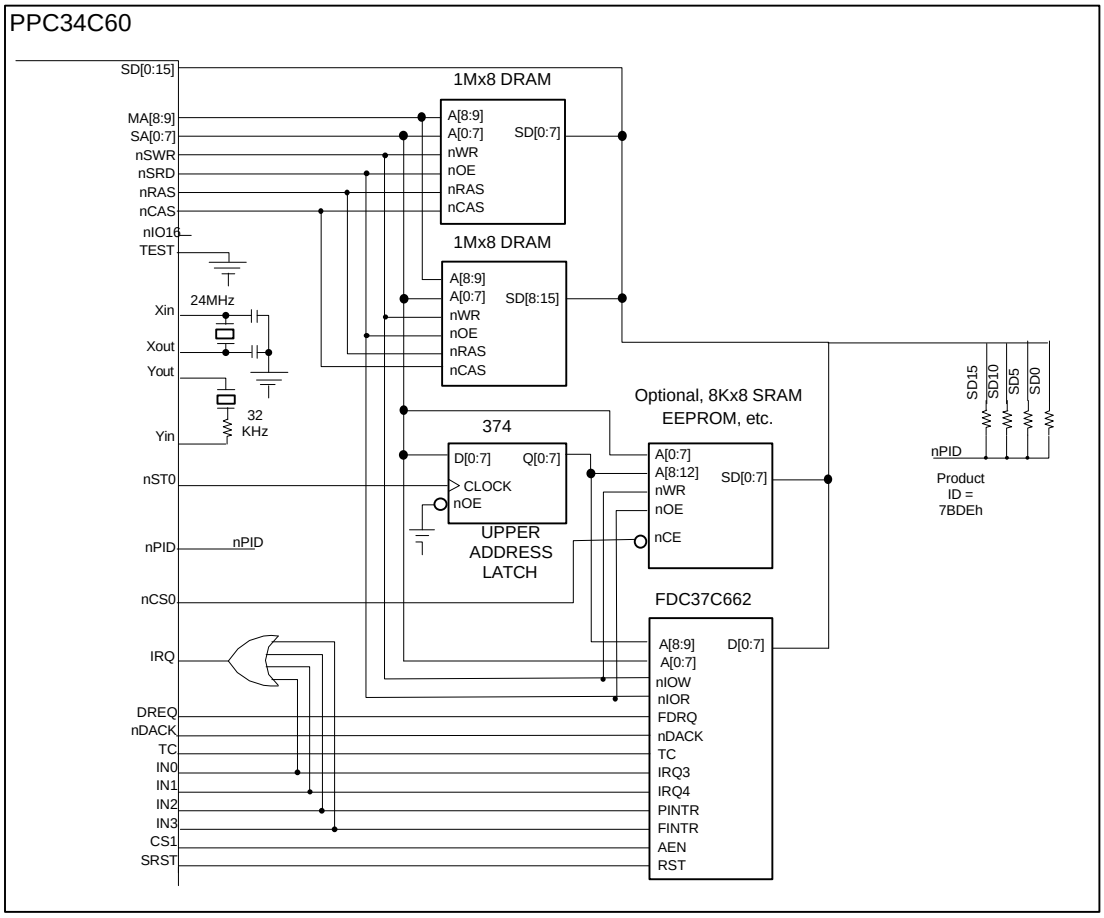


FIGURE 3 – TYPICAL SYSTEM INTERFACE

DEVICE ADDRESSING

The Bi-Directional Parallel Peripheral Interface protocol, defined by the IEEE STD 1284 (Reference 1), describes two basic types of 8-bit information transfers: data read/write operations and address read/write operations. The PPC34C60's bus and internal registers are accessed via data read/write operations.

The PPC34C60's address mode is set through an SPP, EPP, or ECP address write operation. Table 1 specifies the control signals used by each protocol to perform Address and Data Cycles and to indicate reverse data flow. Refer to the IEEE STD 1284 (Reference 1) for further information.

Table 1 - Key Address/Data Cycle Signals

SIGNAL	SPP	EPP	ECP
Address Strobe	SEL	SEL	STB(ALF=0)
Data Strobe	STB	ALF	STB(ALF=1)
Reverse Channel Signal	INIT=0	IMPLICIT	INIT = 0

The Parallel Port provides a byte-wide parallel data path. Figure 4 defines the data bits of this parallel port data path during an address write operation to the PPC34C60.

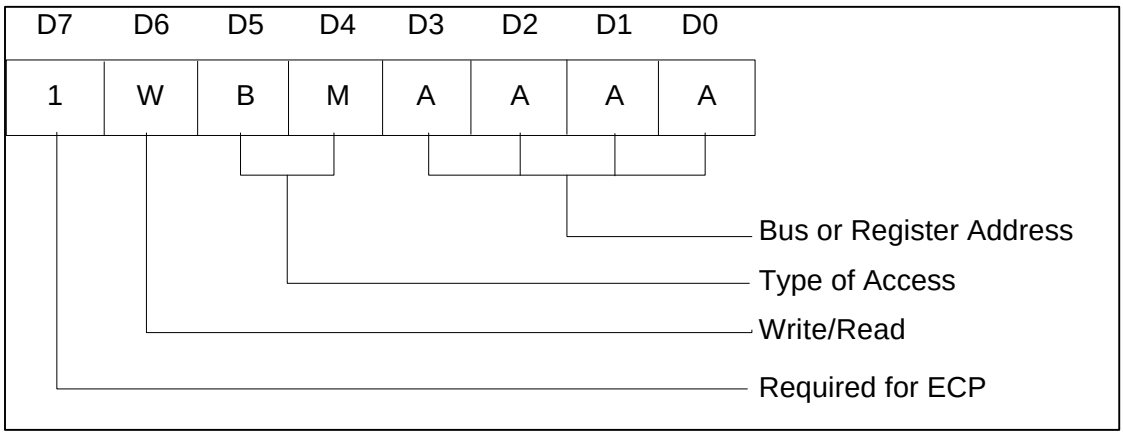


FIGURE 4 – PARALLEL PORT ADDRESS WRITE AND DATA BITS

An address write cycle is used to select the PPC34C60's address mode for subsequent data write cycles. Table 2 shows ten types of Address Modes into which the PPC34C60 may be placed. The address write data byte required for each mode is encoded as '1WBMA3A2A1A0'.

Table 2 also illustrates three separate System Data Bus addressing modes along with DRAM and Internal Registers addressing.

When the Host Address Write data is 1X100XXX, the PPC34C60 provides unrestricted System Data Bus access for all subsequent Host Parallel Port data exchanges.

Unrestricted System Data Bus access can also occur following Address Write operations where 1WBMA3A2A1A0 = 1X00(A3-A0), except that in this short hand addressing mode A3-A0 is also written to the least significant four bits of the PPC34C60 internal Address Register. Address Write operations where 1WBMA3A2A1A0 = 1X01(A3-A0) provides block count limited System Data Bus access with shorthand addressing.

For example, an Address Write operation in which B = 1, M = 0, and A3A2A1A0 = 0000 selects System Data Bus access but does not alter the value of the PPC34C60 Address Bus, SA[0:7].

Table 2 - Address Mode Operations

1WBM	A3A2A1A0	Access Type	W=1(Write)	W=0(Read)
1X00	(A3-A0)	SYSTEM DATA BUS	Unrestricted Bus Write (Shorthand Mode)	Unrestricted Bus Read (Shorthand Mode)
1X01	(A3-A0)		Block Restricted Bus Write (Shorthand Mode)	Block Restricted Bus Read (Shorthand Mode)
1X10	0XXX (BUS)		Unrestricted Bus Write Access	Unrestricted Bus Read Access
1X10	1XXX (DRAM)	DRAM	DRAM Write Access	DRAM Read Access
1X11	RRRR	INTERNAL REGISTERS	Write Internal Register RRRR	Read Internal Register RRRR

W = Write
B = Bus
M = Max Count
A3A2A1A0 = Address Selector
RRRR = Register Selector

INTERNAL REGISTER MAP

The internal registers of the PPC34C60 are selected by performing an Address Write Cycle with bits B and M (bits 5 and 4) set to 1,1 (see Table 2). The desired register is selected by the binary value of A3A2A1A0 (bits-3:0), also shown as RRRR. Internal register RRRR is made available for Read or Write based on the bit value of W (bit 6) as shown below. All internal registers are eight bits wide.

Table 3 - Internal Register Map

W*	BM	RRRR	REGISTER DESCRIPTION	DEFAULTS
X	11	0000	Address Register	00
X	11	0001	Output Configuration Reg	10
X	11	0010	Output Register	80
1	11	0011	Sound Register	NA
0	11	0011	Input Register	SF
X	11	0100	Operation Register	00
X	11	0101	DRAM Buffer Size Register	0C
X	11	0110	Host DRAM Buffer Pointer	00
X	11	0111	DMA DRAM Buffer Pointer	00
X	11	1000	Host Max Block Count - Low	00
X	11	1001	Host Max Block Count - High	10
X	11	1010	DMA Byte Count - Low	00
X	11	1011	DMA Byte Count - High	00
X	11	1100	Configuration Register	04
0	11	1101	Chip Revision Level	00
1	11	1110	Port Test Register	NA
0	11	1110	Port Test Register	00
X	11	1111	Data Transfer Control Register	01

*W
X = Read/Write
1 = Write
0 = Read

REGISTER DESCRIPTIONS

ADDRESS REGISTER - 0000 (Read/Write)

The value in the Address Register represents the current address presented to the Bus Address lines SA[0:7]. The primary method of updating this value is the following sequence. First the Address Register is selected to be written to by performing an Address Write operation (XWBMA3A2A1A0=x1110000). Next a Data Write operation is issued to write A<0:7> as a group equal to the value presented on the parallel port host data lines HD[0:7].

A shorthand mode is also provided to allow the Address to be modified and Bus Operation to be selected in one Address Write operation. If B = 0, then bus operation is selected and A3A2A1A0 is written to A<0-3>; A<4-7> are unaffected. In this mode, if M = 1, then the bus access will be limited by the Host Max Block Count Register. Any attempts to read more data will return invalid data. The PPC34C60 contains an integrated FIFO to enhance performance by reading the Bus one or two bytes ahead of the Host Port. As an example, some devices such as IDE hard drives expect data to be read in a fixed block length (sector). Set MAXCNT (Configuration Register bit 6) and set the value of Host Max Block Count Register to the length of the IDE data block to read only the desired amount of data (1 sector) from the peripheral.

If M = 0, then the current setting of MAXCNT and Host Max Block Count are ignored. This allows polling of a status register without limiting the number of times the register may be accessed.

The PPC34C60 directly provides eight address lines. If more than eight bits of address are necessary, three strobe lines are available which may be used with external circuitry to latch higher-order address bits off of SA[0:7]. For example, the address register can be written with higher order address bits and latched with one or more of the three programmable strobe lines. The address register is then written with A0-A7, and normal bus reads/writes follow. This scheme may be extended to any size address bus needed.

An auto-increment option may be activated by setting AUTOINC (bit 4 in the Operation Register, RRRR=0100) which will increment A<0:7> after each bus access.

OUTPUT CONFIGURATION REGISTER - 0001 (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SP1	SP0	SO1	SO0	CO3	CO2	CO1	CO0

The Output Configuration Register defines the operation of the bits in the Output Register.

The PPC34C60 has eight independent output lines. The functionality of seven of these output lines is selected through the Output Configuration Register. All eight output lines are then controlled or activated through the Output Register (RRRR=0010).

The seven programmable output lines controlled by Output Register bits 0-6 can be selected to operate as either general purpose output pins (inverting), or as special function output pins. The special functions are: Chip Select, Strobe, and Auto-Power.

The eighth (non-programmable) output line is controlled by Output Register bit 7. This output line is defined as "Bus Reset", but it is simply an output bit. It may be used for other purposes if a Bus Reset signal is not required or generated elsewhere. This bit is present on two pins (95 and 94) in both normal and inverted polarities.

Bits 0-3:
SPECIAL FUNCTIONS FOR PROGRAMMABLE OUTPUT LINES 0-3:

Programmable output lines 0-3 can be individually configured as General Purpose (inverting) outputs or as chip select outputs. Chip selects are generated by the bus cycle state machine.

During a bus cycle, the chip select goes low at the start of the cycle and remains low until the end of the cycle.

Output line N (N = 0...3) is controlled through Output Register Bit N. Output line N, configured as a General Purpose output, will present the inverted value written to Output Register bit N. Output line N, configured as a Chip Select, will follow the bus chip select if Output Register bit N is a 1.

Bit 0:CO0 - Chip Select 0/Standard Output 0	
0	Select Output line 0 (Pin 84) as a General Purpose inverting output.
1	Select Output line 0 (Pin 84) as a Chip Select output.

Bit 1:CO1 - Chip Select 1/Standard Output 1	
0	Select Output line 1 (Pin 85) as a General Purpose inverting output.
1	Select Output line 1 (Pin 85) as a Chip Select output.

Bit 2:CO2 - Chip Select 2/Standard Output 2	
0	Select Output line 2 (Pin 86) as a General Purpose inverting output.
1	Select Output line 2 (Pin 86) as a Chip Select output.

Bit 3:CO3 - Chip Select 3/Standard Output 3	
0	Select Output line 3 (Pin 87) as a General Purpose inverting output.
1	Select Output line 3 (Pin 87) as a Chip Select output.

Bits 4-7:
SPECIAL FUNCTIONS FOR PROGRAMMABLE OUTPUT LINES 4-6

Programmable Output lines 4-6 can be individually configured as general purpose (inverting) outputs or as strobe outputs. These strobe signals may be used to clock any edge-triggered flip-flop or register. Additionally, Programmable Output line 6 may be programmed as an Auto-Power pin. This signal allows a peripheral to automatically control its power on state, so that a separate power switch is not necessary. The external circuitry necessary for this passively pulls down the INIT line from the host. The power supply is turned on when the INIT line rises to a high logic level. The PPC34C60 will then monitor the host, and will bring the Auto-Power pin to a logic low level when the power can be shut off.

Output line N, configured as a Strobe signal, is normally high and pulses low momentarily when a 1 is written to Output Register bit N.

Bit 4:SO0 - Strobe 0/Standard Output 4	
0	Select Output line 4 (Pin 44) as a General Purpose inverting output.
1	Select Output line 4 (Pin 44) as a Strobe output.

Bit 5:SO1 - Strobe 1/Standard Output 5	
0	Select Output line 5 (Pin 43) as a General Purpose inverting output.
1	Select Output line 5 (Pin 43) as a Strobe output.

Bit 6,7:SP0,SP1 - Auto-Power/Strobe 2/Standard Output 6	
0,x	Select Output line 6 (Pin 42) as an Auto-Power Pin.
1,0	Select Output line 6 (Pin 42) as a General Purpose inverting output.
1,1	Select Output line 6 (Pin 42) as a Strobe output.

OUTPUT REGISTER - 0010 (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BRESET	nOP6 nPWR STB2	nOP5 STB1	nOP4 STB0	nOP3 CS3	nOP2 CS2	nOP1 CS1	nOP0 CS0

Each Output Register bit independently controls the operation of its respective Output pin. The function of each output pin, except for BRST (Pins 94 and 95), is determined by the data stored in the Output Configuration Register.

CHIP SELECT OUTPUTS

Output lines 0-3 (Pins 84-87) are programmable as Chip Selects (CS0-CS3) via the Output Configuration Register. When programmed as a Chip Select, the output pin will go low during bus operations if its associated bit in the Output Register is set. If the associated bit is not set in this register, the output pin will remain high.

STROBE OUTPUTS

Output lines 4-6 (Pins 44-42), when programmed as strobes (STB0-STB2) via the Output Configuration Register, will pulse low for two BUSCLK periods when the associated bit is set. The strobes recover and may be re-written at any time. Note: the strobe Output Register bits are reset automatically after the strobe is generated.

AUTO-POWER OUTPUT

Output line 6 (Pin 42), when programmed as Auto-Power (nPWR), via the Output Configuration Register, will remain at a high level as long as host activity is detected. When the chip determines that power may be shut off, this pin will go low.

There are two mechanisms driving this output. The first mechanism monitors the levels on the host port. If the port assumes the terminated levels or all low levels for 16 to 20 seconds, then the host is presumed off (or disconnected). The second mechanism monitors Host port activity (signal transitions). After a one minute period of inactivity (given that the WDOGEN pin is tied low) the watchdog will be triggered sending four beeps to the piezo driver. After completion of the tones the Auto-Power pin will go low.

GENERAL PURPOSE OUTPUTS

Bit 7 (BRESET) and any other bits that are programmed through the Output Configuration Register as general purpose output bits are inverted and passed to the associated output pin.

SOUND REGISTER - 0011 (Write Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FREQ	LTONE	STONE	SQULCH	rsvrd	rsvrd	rsvrd	rsvrd

These bits allow the piezo driver to generate tones under program control.

Bits 0-3:rsvrd
These bits are reserved and should be written as zeros.

Bit 4:SQULCH
Setting this bit terminates currently active low battery tones. If the low battery input (Pin 35) goes high, and then low again after this bit is set, low battery tones will resume. In order to squelch these low battery tones, this bit simply needs to be re-written with a logic "1".

Bit 5:STONE
Setting this bit generates a 1/8 second tone. This bit self-clears after the tone is generated and when set again will generate another 1/8 second tone.

Bit 6:LTONE
Setting this bit generates a 1/2 second tone. This bit self-clears after the tone is generated and when set again will generate another 1/2 second tone.

Bit 7:FREQ
This bit selects the Nominal frequency for the piezo driver circuit. 0 selects 2KHz, 1 selects 4 KHz .

INPUT REGISTER - 0011 (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LOBATT	IRQ	IRQ LATCH	QIC-80	IN3	IN2	IN1	IN0

The PPC34C60 has six Input pins, of which two are dedicated and four are uncommitted. The Input Register provides the Host with bit access to each of these input pins. Bit 4 is a special purpose bit useful for QIC-80 tape drive peripherals.

Bit 0:IN0 (Pin 82)
This bit represents the current state of the uncommitted input pin IN0.

Bit 1:IN1 (Pin 83)
This bit represents the current state of the uncommitted input pin IN1.

Bit 2:IN2 (Pin 37)
This bit represents the current state of the uncommitted input pin IN2.

Bit 3:IN3 (Pin 36)
This bit represents the current state of the uncommitted input pin IN3.

Bit 4:QIC-80
This bit will be set if more than 2.5ms have passed since the last rising edge of IRQ (pin 48). This function is designed for QIC-80 tape drives that require 2.5ms between the completion of one command and the start of a subsequent command.

Bit 5:IRQ LATCH
This bit is used to latch an interrupt request event and is enabled by setting INTEN (bit 6 of the Operation Register). When enabled this bit is set by a rising edge on the IRQ pin (Pin 48), and cleared by setting INTCLR (bit 7of the Operation Register), or by following a Clear Interrupt command from the Daisy Chain control packet (see the Daisy Chain Specification - Reference 3).

Bit 6:IRQ (Pin 48)
This bit represents the current state of the IRQ pin.

Bit 7:LOBATT (Pin 35)
This bit represents the current state of the LOBATT input. When low, the piezo driver circuitry will provide a "low battery beep."

OPERATION REGISTER - 0100 (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTCLR	INTEN	AUTO-INC	PDMA	DIREC	DMAEN	D16	F16

The bits in this register control the operation of the PPC34C60.

Bit 0:F16
Setting this bit overrides Pin 81 (nIO16), forcing all bus accesses to 16-bit. Use this bit to access a 16-bit peripheral which does not generate nIO16.

Bit 1:D16
This bit controls the bus width of the DMA cycles. 1 selects 16-bit, 0 selects 8-bit. nIO16 and F16 are ignored during DMA cycles.

Bit 2:DMAEN
This bit must be set for the DMA state machine to recognize DREQs. This bit will be automatically cleared when the DMA is complete.

Bit 3:DIREC
This bit controls the direction of DRAM - BUS DMA cycles. 1 selects a write from DRAM to BUS, 0 selects a read from BUS to DRAM.

Bit 4:PDMA
Setting this bit enables the psuedo-DMA mode. In the PDMA mode DMA functions are performed, but CS is used instead of DACK to qualify the bus cycles. Use the PDMA mode to DMA to or from a device which does not explicitly support DMA.

Bit 5:AUTOINC
Setting this bit causes the bus address (A0-A7) to increment after every bus access.

Bit 6:INTEN
Setting this bit enables the interrupt latch.

Bit 7:INTCLR
Writing a 1 to this bit will clear any pending interrupt. This bit always reads 0.

DRAM BUFFER SIZE REGISTER - 0101 (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DMA DRAM BUFFER SIZE				HOST DRAM BUFFER SIZE			

This register determines the size of the DRAM buffers, both for DMA DRAM and Host DRAM accesses. The buffer sizes are encoded as follows:

0001	=	2	Bytes	1001	=	512	Bytes
0010	=	4	Bytes	1010	=	1 K	Bytes
0011	=	8	Bytes	1011	=	2 K	Bytes
0100	=	16	Bytes	1100	=	4 K	Bytes
0101	=	32	Bytes	1101	=	8 K	Bytes
0110	=	64	Bytes	1110	=	16 K	Bytes
0111	=	128	Bytes	1111	=	32 K	Bytes
1000	=	256	Bytes	0000	=	64 K	Bytes

HOST DRAM BUFFER POINTER REGISTER - 0110 (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HOST DRAM BUFFER POINTER (0-255)							

This register sets the Host's DRAM pointer to the selected buffer. The DRAM address is calculated using this pointer, the DRAM Buffer Size Register, and the DRAM bus width from the Configuration Register. If MAXCNT is set during the Host to DRAM transfer, then this register is incremented upon reaching maximum count, and the DRAM address is recalculated for the next buffer.

A maximum of 256 buffers are available in this register. The actual number of buffers depends on the DRAM loaded, and the buffer size selected. If the pointer is incremented past the last buffer, it will wrap back around to the first buffer. No active buffer count is maintained; the driver software must prevent overwriting existing buffers.

DMA DRAM BUFFER POINTER REGISTER - 0111 (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DMA DRAM BUFFER POINTER (0-255)							

This register sets the DMA DRAM pointer to the selected buffer. Its operation is similar to the Host DRAM Buffer Pointer Register. This register is incremented upon completion of a DMA transfer and the DRAM address is recalculated for the next buffer.

HOST MAX BLOCK BYTE-COUNT LOW REGISTER - 1000 (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HOST MAX BLOCK BYTE-COUNT LOW (HBC[7:0])							

This register sets the low byte of the counter for Host block transfers. It is used in conjunction with MAXCNT in the Configuration register to limit external DRAM and bus read accesses. The counter is reloaded with this value at every Address Write cycle.

HOST MAX BLOCK BYTE-COUNT HIGH REGISTER - 1001 (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HOST MAX BLOCK BYTE-COUNT HIGH (HBC[15:8])							

This register sets the high byte of the counter for Host block transfers. It is used in conjunction with MAXCNT in the Configuration register to limit external DRAM and bus read accesses. The counter is reloaded with this value at every Address Write cycle.

DMA BYTE-COUNT LOW REGISTER - 1010 (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DMA BYTE-COUNT LOW (DBC[7:0])							

This register sets the low byte of the 16-bit byte counter used for terminating DMA transfers.

Subsequent DMA transfers with the same byte count can be kicked off by resetting the DMA Enable bit in the Operation Register.

DMA BYTE-COUNT HIGH REGISTER - 1011 (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DMA BYTE-COUNT HIGH (DBC[15:8])							

This register sets the high byte of the 16-bit byte counter used for terminating DMA transfers.

Subsequent DMA transfers with the same byte count can be kicked off by resetting the DMA Enable bit in the Operation Register.

CONFIGURATION REGISTER - 1100 (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RST	MAXCNT	SFIFO	rsvrd	RAMSZ1	RAMSZ0	CKSEL1	CKSEL0

The bits in this register define the configuration of the system.

Bit 7:RST
Setting this bit resets the storage elements in the chip.

Bit 6:MAXCNT
When this bit is set, the Max Block Count Registers are used to limit the bus and DRAM accesses.

Bit 5:SFIFO
This bit selects the operating mode of the Read FIFO. Setting this bit causes the internal Read FIFO to operate as a single-word read-ahead. If this bit is clear, the Read FIFO will operate as a two-word read-ahead.

Bit 4:rsvrd
This bit is reserved and should be written as zeros.

Bits[3:2]:RAMSZ[1:0]

RAMSZ1	RAMSZ0	DRAM BUS WIDTH
0	0	Selects DRAM data width of 4 bits.
0	1	Selects DRAM data width of 8 bits.
1	X	Selects DRAM data width of 16 bits.

Bits[1:0]:CKSEL[1:0]

CKSEL1	CKSEL0	BUS CYCLE (BUSCLK)
0	0	Bus Cycle (BUSCLK) = System Clock / 2
0	1	Bus Cycle (BUSCLK) = System Clock / 3
1	0	Bus Cycle (BUSCLK) = System Clock / 5
1	1	Bus Cycle (BUSCLK) = System Clock / 6

BUSCLK clocks the Bus Interface State Machine responsible for generating Bus Access, DRAM access, and DRAM Refresh timing. BUSCLK is also responsible for Output Strobe timing. System Clock is the SCLK input (pin 96) and is typically 24MHz.

CHIP REVISION LEVEL REGISTER - 1101 (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TYPE ID					REVISION		

It is expected that the PPC34C60 will be used in various designs at different integration levels. This register provides a means of determining which type of chip is in use. The most significant five bits are reserved for a Type ID; The least significant three bits may be used to identify different masks and/or process types. This document refers to chips with Revision Level values:

0000 0000

PORT TEST WRITE REGISTER - 1110 (Write Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INCREMENTING WRITE TEST PATTERN							

The Port Test Write Register is used to determine the highest reliable printer port data transfer rate. An interface test must be performed at various speeds until data integrity can be assured. To enable this test, select the Port Test Write Register with an Address Write cycle. After being selected, the register looks for an incrementing pattern starting at 00. If data is written out of sequence, or if a communications error occurs, the ERR bit in the Data Transfer Control Register will be set.

PORT TEST READ REGISTER - 1110 (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INCREMENTING READ TEST PATTERN							

The Port Test Read Register verifies the read data transfer rate. To enable this test, select the Port Test Read Register with an Address Write cycle. After being selected, this Register reads 00 when first addressed, and increments with every access. The ERR bit in the Data Transfer Control Register is not affected by the Port Test Read.

DATA TRANSFER CONTROL REGISTER - 1111 (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ERR	rsvrd	rsvrd	rsvrd	rsvrd	rsvrd	BURST	8BIT

Bits 0 and 1 of this register provide options to regulate data transfer on non-enhanced ports. Bit 7 provides data transfer rate status information as described in the Port Test Write Register.

Bit 7:ERR
This bit is set if an error occurs writing to the Port Test Write Register. It is cleared by selecting the Port Test Register with an Address Write cycle.

Bits 6-2:rsvrd
These bits are reserved and should be written as zeros.

Bit 1:BURST
This bit is valid if the PPC34C60 is selected for Compatibility mode. Burst mode applies for reads and writes in Byte mode and reads in Nibble mode (see IEEE STD 1284 - Reference 1). Setting this bit maximizes data transfer by minimizing handshaking requirements. Data is latched on each edge of the Burst strobe as shown in Figure 5.

Bit 0:8BIT
This bit is only valid with a bi-directional port in Compatibility mode. Setting this bit selects Reverse Transfer Byte mode. Clearing this bit selects Reverse Transfer Nibble mode (see IEEE STD 1284 - Reference 1).

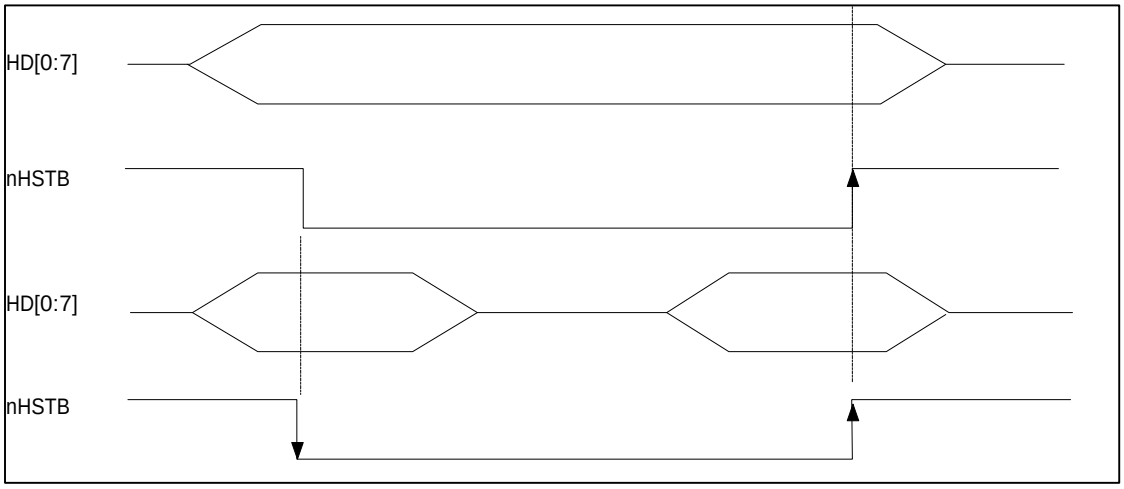


FIGURE 5 – BURST MODE

DRAM BUFFER OPERATION

The PPC34C60 provides support for a DRAM buffer with DMA capability. DRAM bus widths of 4, 8, or 16 bits may be used, with linear 20 bit addressing. DMA to and from the DRAM may be either 8 or 16 bit cycles. The PPC34C60 will take care of matching the bus widths between the DMA Controller and the DRAM. If multiple DRAM accesses are necessary for a DMA cycle, they will use fast page mode.

DRAM refresh is automatic, and uses a CAS before RAS refresh method. The DRAM is addressed as a number of buffers. The buffer size is programmable to 'power of 2' sizes between 2 and 64K bytes. A byte counter is used to control the DRAM access. It may be programmed to any value from 1 up to the buffer size. To prevent overwriting data, the byte counter should not be set to a value exceeding the buffer size.

The DRAM may be independently accessed by the host and the DMA Controller. There are separate buffer and byte counters for each. When a DRAM transfer is complete, the buffer number is incremented, and further DRAM access is blocked.

DRAM Linear Address Mapping

	MA9	MA8	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
ROW	A19	A17	A15	A14	A13	A12	A11	A10	A9	A8
COL	A18	A16	A7	A6	A5	A4	A3	A2	A1	A0

64K x N

256K x N

1M x N

DRAM PHYSICAL ADDRESSING

Users access the PPC34C60 DRAM through the Host and DMA logical addressing controls found in the Internal Registers. The system automatically calculates the physical DRAM addresses based on the values stored in these registers and the width of the system data paths.

The logical addressing controls are the 4-bit encoded Host and DMA DRAM buffer size controls in the DRAM Buffer Size Register (0101h) and the 8-bit DRAM buffer pointers in the Host DRAM Buffer Pointer Register (0110h) and the DMA DRAM Buffer Pointer Register (0111h). The DRAM Data Bus width is determined by RAMSZ0 and RAMSZ1, bits 2 and 3, in the Configuration Register (1100h). The System DMA Data Bus width is determined by D16, bit 1 in the Operation Register (0100h). Host access is always eight bits.

The PPC34C60 determines physical DRAM addresses by calculating the buffer start address and adjusting this value for bus width. The buffer start address is the buffer pointer multiplied by the buffer size. If the DRAM Bus width is greater than or equal to the System Bus width then the buffer start address is the physical DRAM address, otherwise the physical DRAM address is the buffer start address multiplied by the System Bus width divided by the DRAM Bus width as shown in the Figure 6 below.

HOST/DMA Bus Width Greater Than DRAM Bus Width

Physical Address = Buffer Ptr * Buffer Size * System Bus Width / DRAM Bus Width

HOST/DMA Bus Width Less Than or Equal to DRAM Bus Width

Physical Address = Buffer Ptr * Buffer Size

For example, during a DMA transfer where;

1. the DRAM data bus width is four bits,
2. the DMA device data bus width is sixteen bits,
3. the DMA Buffer Size is 4096 bytes (1000h),
4. the DRAM Buffer Pointer is 2,

the Physical DRAM Address for the start of this transfer will be 32768 (8000h)

FIGURE 6 - DRAM PHYSICAL ADDRESSING

SYSTEM DATA BUS CYCLES

The System Data Bus is controlled by an internal state machine with seven states as shown below in Figure 7. The state machine is clocked by the BUSCLK which is software- programmable as SCLK divided by 2, 3, 5, or 6.

Three types of operations are performed by the bus interface: a Bus Cycle, a DRAM Access, and a DRAM Refresh. Refer to Tables 4-6 for the state flow description for each operation. The bus controller normally sits in the idle state. When a bus interface operation is kicked off, it advances to state 1. It then advances to the next state at every BUSCLK cycle. After state 7, the controller returns to idle.

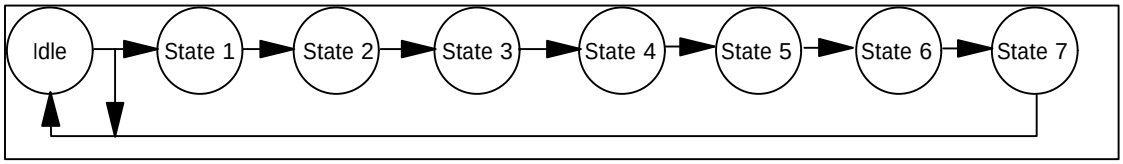


FIGURE 7 - GENERIC SYSTEM DATA BUS CYCLE

BUS CYCLE TIMING

When an Address Write cycle selects a bus write, the next data received is written to the bus. The interface must, however, know whether to expect an 8 or 16 bit bus address. To determine the bus width, a bus cycle is started from the Address Write cycle. This "pre-write" cycle asserts chip select and samples and latches nIO16. The write cycle is initiated after the first byte received for 8 bit writes, or after the second byte of data for 16 bit writes.

Table 4 - Bus Cycle State Flow Description

IDLE	Write: Data bus drivers are disabled, nRAS and nCAS are inactive.
STATE 1	Read: If necessary, data advances to next element in the FIFO buffer. nCAS goes active for first refresh.
STATE 2	Write: Data is latched into bus latches. nRAS goes active for first refresh.
STATE 3	Chip Select goes active.
STATE 4	nIO16 is sampled. Read: nRD goes active. Write: If nIO16 is sampled low and this is the first byte received, then nWR remains inactive. If nIO16 is sampled high or if nIO16 is sampled low and this is the second byte received, then nWR goes active and data bus drivers are enabled. nRAS and nCAS go inactive.
STATE 5	Wait for data bus to stabilize, nCAS goes active for second refresh.
STATE 6	Read: Data is latched, nRD goes inactive. Write: nWR goes inactive. nRAS goes active for second refresh.
STATE 7	Chip select goes inactive. Read: Data advances to next element if possible. Write: Data bus drivers are disabled.

Table 5 - DRAM Access State Flow Description

IDLE	nRAS and nCAS go inactive.
STATE 1	Row Address output.
STATE 2	nRAS goes active. Read: nRD goes active. Write: nWR goes active.
STATE 3	Column Address output Write: Data bus drivers enabled.
STATE 4	nCAS goes active.
STATE 5	Column Address incremented. Read: Data is latched. Write: Data bus drivers disabled. (If multiple accesses are needed, States 3-5 are repeated)
STATE 6	nRAS, nCAS, nRD, nWR go inactive.
STATE 7	nRAS precharge time.

Table 6 - DRAM Refresh State Flow Description*

IDLE	nRAS and nCAS go inactive.
STATE 1	nCAS goes active for first refresh.
STATE 2	nRAS goes active for first refresh.
STATE 3	
STATE 4	nRAS and nCAS go inactive.
STATE 5	nCAS goes active for second refresh.
STATE 6	nRAS goes active for second refresh.
STATE 7	

*For SCLK = 24 MHz, a DRAM Refresh Cycle is performed every 30μS. Bus cycles have built-in DRAM refresh which reset the 30μS refresh timer.

POWERING THE PPC34C60

The PPC34C60 has a built-in mechanism to insure against damage when the peripheral is powered down and the host is powered up. Figure 8 shows how to incorporate this protection feature into your peripheral's power and return design. Isolate the chip's VCC from the rest of the peripheral's VCC using a Schottky diode. The SENSE input should be tied to the peripheral's VCC and the anode of the diode. When the peripheral's power is off, the SENSE input will go low, tri-stating all outputs. This prevents the PPC34C60 from driving into a low impedance load and damaging its input protection diodes. When the peripheral's power is turned on, the SENSE line will be pulled high and all output drivers of the PPC34C60 will be enabled.

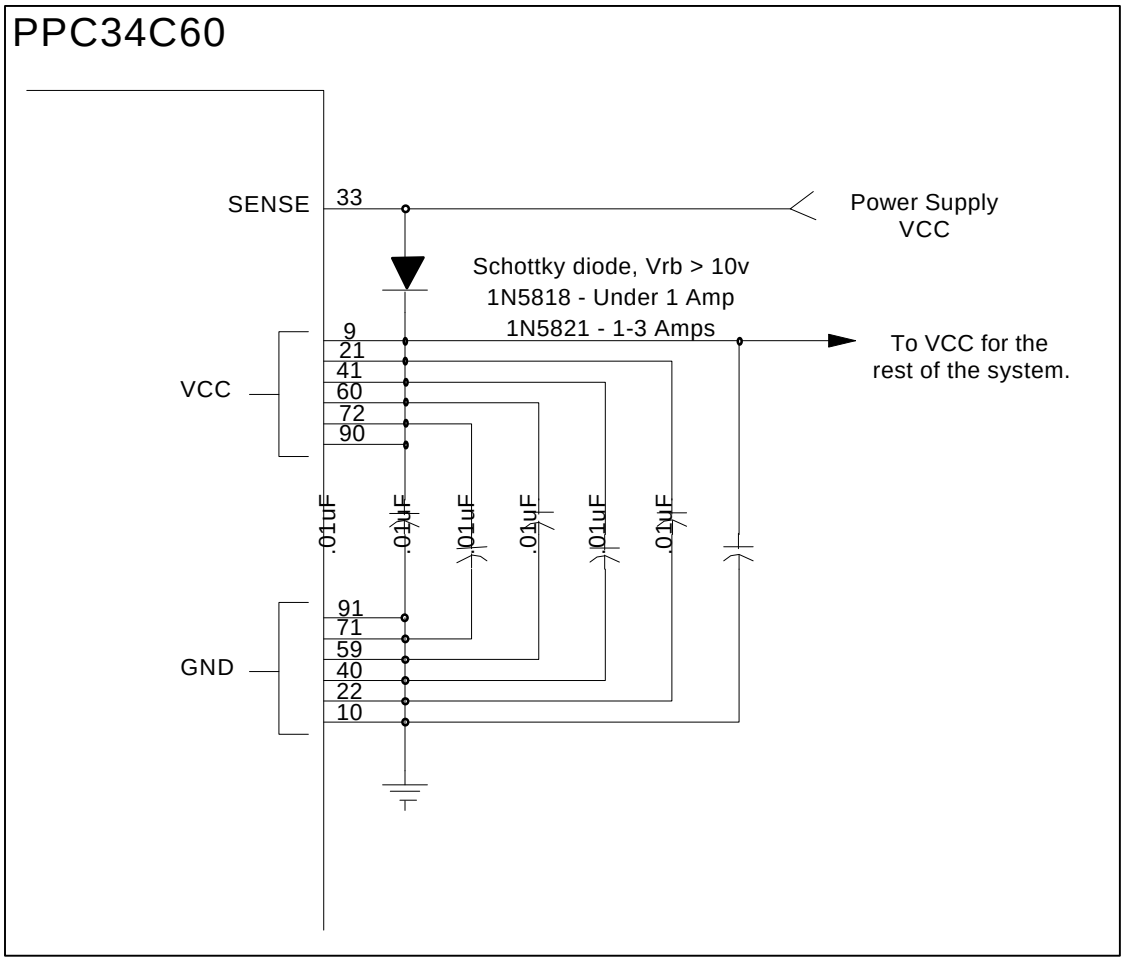


FIGURE 8 - SUGGESTED PP

SUGGESTED OSCILLATOR CIRCUITS

The PPC34C60 requires two frequency sources. The 24MHz clock is supplied with a parallel resonant 24MHz crystal oscillator connected as shown in Figure 9. It is important that the board designer place the crystal oscillator close to the PPC34C60 maintaining the shortest possible traces. The 24MHz clock is used by much of the internal circuitry and provides the time base used by the Bus Interface circuitry.

The second clock source is provided by an RC circuit and should be connected as shown in Figure 10. This clock is used primarily by the Watch Dog Timer and Piezo Driver functional blocks.

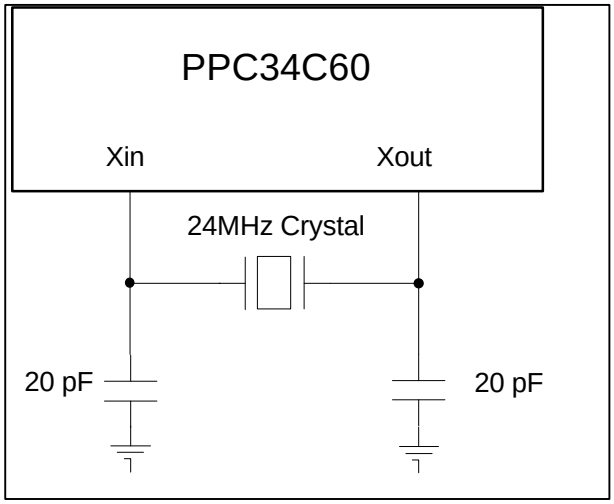


FIGURE 9 - SUGGESTED 24 MHz OSCILLATOR CIRCUIT

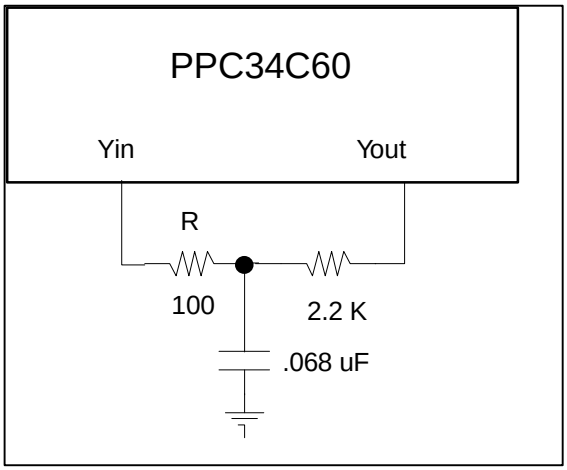


FIGURE 10 - SUGGESTED 32 KHz OSCILLATOR CIRCUIT

OPERATIONAL DESCRIPTION

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0^{o}C to $+70^{o}$C
Storage Temperature Range..... -55^{o} to $+150^{o}$C
Lead Temperature Range (soldering, 10 seconds)..... $+325^{o}$C
Positive Voltage on any pin, with respect to Ground..... VCC+0.3V
Negative Voltage on any pin, with respect to Ground ..... -0.3V
Maximum VCC..... +7V

*Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS (TA = 0^{o}C - 70^{o}C, VCC = +5.0 V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILIS}			0.8	V	Schmitt Trigger
High Input Level	V_{IHIS}	2.2			V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		250		mV	
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.4	V	
High Input Level	V_{IHCK}	3.0			V	
Input Leakage (All I and IS buffers)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	$V_{IN} = V_{CC}$
Pull Up Current	I_{OH}		75	150	µA	V_{IN} = 0
Pull Down Current	I_{OL}			200	µA	V_{IN} = 5

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I/O8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
I/O16 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 16 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -12 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
O8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
O16 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 16 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -12 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
O24 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 24 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -12 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
Supply Current Active	I_{CC}			80	mA	All outputs open.

CAPACITANCE $T_A = 25^oC$; fc = 1MHz; V_{CC} = 5V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

TIMING DIAGRAMS

The PPC34C60 supports three communications cycles: Address Write, Data Write, and Data Read. The signalling for these cycles in Standard, EPP, and ECP modes is discussed below.

ADDRESS WRITE

An Address Write cycle must be issued before any Data cycles, since this tells the PPC34C60 whether the following Data cycles are write/read, and where the data should go/come from.

Standard Mode

The host places the address information on the parallel port data lines, then strobes the address into the PPC34C60 by pulsing Select In (HSEL) low with a minimum 200 ns pulse width. The PPC34C60 will always accept the Address Write cycle, there is no Busy hold off.

EPP Mode

The host sends address information by writing to the EPP Address Register (base+3). The EPP interface chip places this data on the parallel port data lines, then brings Select In (HSEL) low. The PPC34C60 latches the information, then acknowledges the transfer by raising Busy (HBSY). The EPP interface chip may terminate the cycle when it sees Busy go high.

ECP Mode

The host sends address information by writing to the ECP Address FIFO (base+0). The ECP interface chip places this data on the parallel port data lines, sets Auto LF (HALF) low to indicate address information, then sets Strobe (HSTB) low to start the transfer. The PPC34C60 acknowledges the cycle by raising Busy (HBSY). The ECP chip then raises Strobe. The PPC34C60 latches the information, then sets Busy low.

DATA WRITE

The data write cycle is used to send data to the PPC34C60 registers, DRAM, or the remote system. A previous Address Write cycle must have been sent to the PPC34C60 selecting Write, and the target of the write.

Standard Mode

If the PPC34C60 can accept data, busy (HBSY) will be low. The host places the data on the parallel port data lines, then strobes the data into the PPC34C60 by pulsing Strobe (HSTB) low with a minimum 200 ns pulse width. If the PPC34C60 is operating in the Burst Mode, then Strobe should only change state instead of pulsing low.

EPP Mode

If the PPC34C60 can accept data, Busy (HBSY) will be low. The host sends data by writing to the EPP Data Registers (base+4 - base+7). The EPP interface chip places the data on the parallel port data lines, then lowers Auto LF (HALF). The PPC34C60 latches the data, then raises Busy to acknowledge the transfer. The EPP interface chip may terminate the cycle when it sees Busy go high.

ECP Mode

If the PPC34C60 can accept data, Busy (HBSY) will be low. The host sends data by writing to the ECP Data FIFO (base+400h). The ECP interface chip places this data on the parallel port data lines, sets Auto LF (HALF) high to indicate data cycle, then lowers Strobe (HSTB) to start the transfer. The PPC34C60 acknowledges the cycle by raising Busy. The ECP chip then raises Strobe. The PPC34C60 latches the data, then sets Busy low.

DATA READ

A Data Read cycle is used to get data from the PPC34C60 registers, DRAM, or the remote system. A previous Address Write cycle must have been sent to the PPC34C60 selecting Read, and the source of the read.

Standard Mode

If the PPC34C60 has data ready, Busy (HBSY) will be low. If the PPC34C60 is in 4 bit mode, the host reads the low nibble from the status lines Ack (HACK), PError (HPE), Slct (HSLCT), Error (HERR). The host then pulses Strobe (HSTB) low to acknowledge the low nibble. The PPC34C60 then places the high nibble on the same status lines, the host reads the high nibble, then pulses Strobe to signal receipt of the data. If the PPC34C60 is in 8 bit mode, then the host disables it's data drivers, floating the parallel port data lines. The host enables the PPC34C60 bus drivers by lowering Init (HINIT), reads the data from the data lines, then pulses Strobe low to acknowledge the transfer.

If the PPC34C60 is operating in Burst Mode, then the Strobe only changes State instead of pulsing low in the above description.

EPP Mode

If the PPC34C60 has data ready, Busy (HBSY) will be low. The host gets data from the PPC34C60 by reading the EPP Data Registers (base+4-base+7). The EPP interface chip disables the port drivers, then lowers Auto LF (HALF). At this point, the PPC34C60 drives data onto the data lines, then raises Busy. The EPP Chip then latches the data, and raises Auto LF to terminate the cycle.

ECP Mode

The ECP interface requests a reverse transfer by disabling the data line drivers, then lowering Inet (HINIT). The PPC34C60 acknowledges the reverse transfer by lowering PError (HPE), and driving the data lines. When the PPC34C60 has data ready, it will lower Ack (HACK). The ECP chip will respond by raising Auto LF (HALF). The PPC34C60 then raises Ack, signalling the ECP chip to latch the data. The ECP chip then terminates the cycle by lowering Auto LF.

TIMING SYMBOL	PPC34C60 PIN NAME	PIN NUMBER
HD[0:7]	HD[0:7]	5,8,13,15-18,20
nSTB	nHSTB	2
nALF	nHALF	3
nSEL	nHSEL	14
nINIT	nHINIT	11
BSY	HBSY	26
nACK	nHACK	24
PE	HPE	28
SLCT	HSLCT	30
nERR	nHERR	6

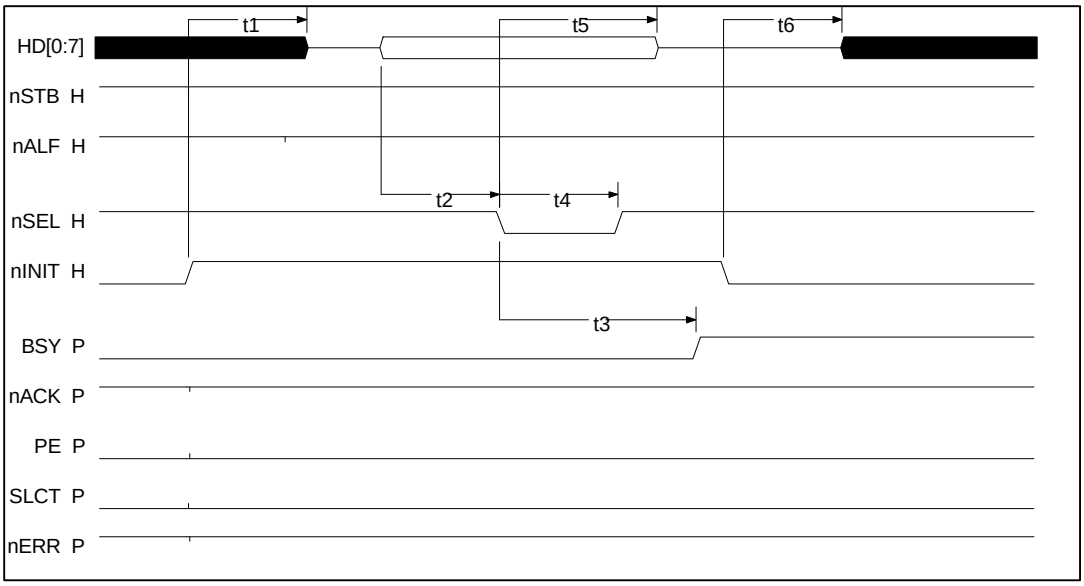


FIGURE 11 - SPP ADDRESS WRITE TIMING (PARALLEL PORT SIGNALS)

All timing for SCLK = 24MHz.

This signaling sequence pertains to a device that has been previously selected to communicate via SPP Mode. This timing sequence is not specified in the P1284 specification; it should not violate the P1284 spec.

See Page 46 for SPP Address Write Timing Parameters.

SPP ADDRESS WRITE TIMING (PARALLEL PORT SIGNALS)

	Parameter	min	typ	max	units
t1	nINIT controls the direction of the parallel port when in SPP mode. nINIT deasserted to HD[0:7] released to high impedance by the PPC34C60.	84 [2 SCLK]		125 [3 SCLK]	ns
t2	The Host can now drive HD[0:7] with an address byte and then strobe it into the PPC34C60 by asserting the nSEL signal. This time represents the address setup time required by the PPC34C60.	125 [3 SCLK]			ns
t3	Typically the address written to the PPC34C60 is an instruction detailing the type of transfer to follow (i.e., Data Read/Write to DRAM, Bus, Register). Thus, once this address is received by the PPC34C60, it asserts the BSY signal to indicate that it is preparing for the upcoming transfer. This time represents the time for BSY to assert from the assertion of nSEL.	167 [4 SCLK]		208 [5 SCLK]	ns
t4	nSEL pulse width. This time represents the duration that nSEL must be asserted in order for the PPC34C60 to recognize an edge.	125 [3 SCLK]			ns
t5	The Host is required to hold the address valid for this amount of time following assertion of the nSEL line.	167 [4 SCLK]			ns
t6	nINIT controls the direction of the parallel port when in SPP mode. nINIT may be asserted anytime after the address hold time (t5) has been satisfied. This time represents the time from nINIT asserted to HD[0:7] driven by the PPC34C60.	84 [2 SCLK]		125 [3 SCLK]	ns

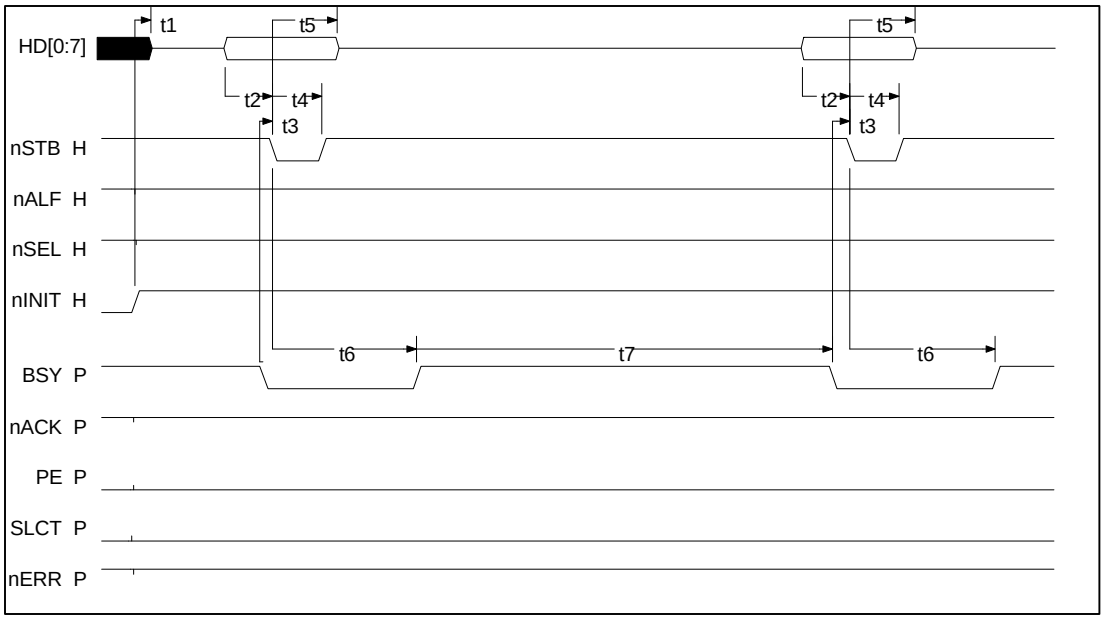


FIGURE 12 - SPP DATA WRITE TIMING (PARALLEL PORT SIGNALS)

This signaling sequence pertains to a device that has been previously selected to communicate via SPP Mode.

SPP DATA WRITE TIMING (PARALLEL PORT SIGNALS)

	Parameter	min	typ	max	units
t1	nINIT controls the direction of the parallel port when in SPP mode. nINIT deasserted to HD[0:7] released to high impedance by the PPC34C60.	84 [2 SCLK]		125 [3 SCLK]	ns
t2	Valid data on HD[0:7] to nSTB asserted edge.	125 [3 SCLK]			ns
t3	BSY deasserted (low) to nSTB asserted edge.	0			ns
t4	nSTB asserted pulse width.	125 [3 SCLK]			ns
t5	Valid data hold from nSTB deasserted edge.	125 [3 SCLK]			ns
t6	nSTB asserted edge to BSY asserted edge.	333 [8 SCLK]		375 [9 SCLK]	ns
t7	BSY asserted pulse width. These values are based on BCLK = 2 SCLK.	0		1,084 [13 BCLK]	ns

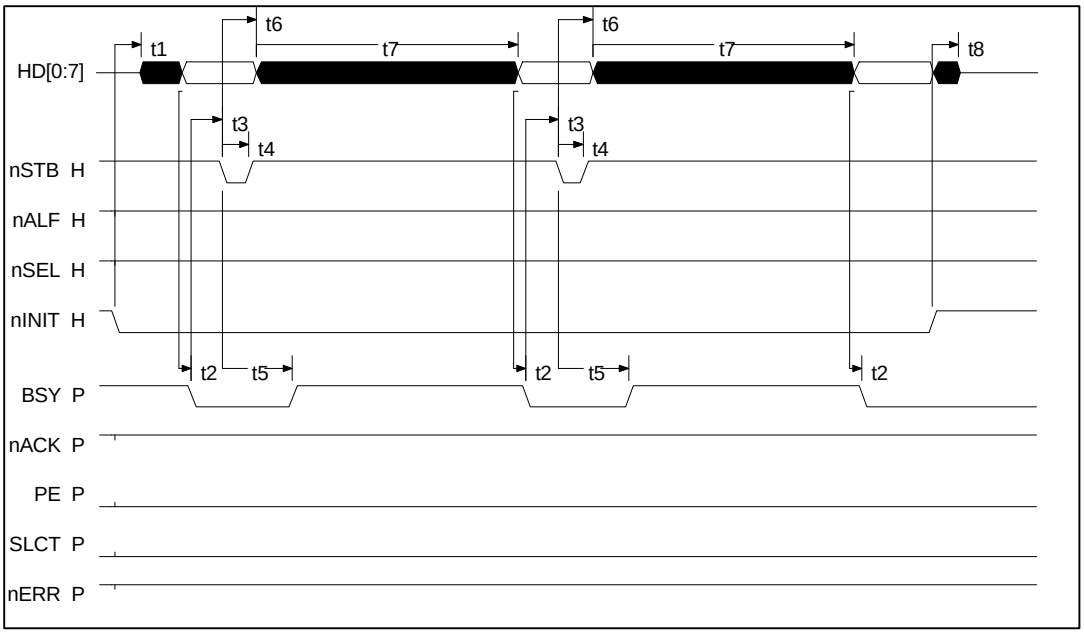


FIGURE 13 - SPP DATA READ TIMING (PARALLEL PORT SIGNALS)

This signaling sequence pertains to a device that has been previously selected to communicate via SPP Mode. The timing sequence shows three bytes being read from the 34C60.

See Page 49 for SPP Data Read Timing Parameters.

SPP DATA READ TIMING

	Parameter	min	typ	max	units
t1	nINIT controls the direction of the parallel port when in SPP mode. When nINIT is asserted the data port is driven by the PPC34C60 and read by the Host. This time represents the time from nINIT asserted to HD[0:7] driven by the PPC34C60. Note: data is not necessarily valid.	84 [2 SCLK]		125 [3 SCLK]	ns
t2	As soon as the PPC34C60 places valid data onto the HD[0:7] port lines, the BSY signal is deasserted by the PPC34C60 to inform the Host that data is now valid.	0		20	ns
t3	This time is determined by the host, the PPC34C60 places no restriction on this time. This time represents the time it takes the Host to recognize and latch the valid data on HD[0:7].	n/a		n/a	
t4	nSTB pulse width. This time represents the duration that nSEL must be asserted in order for the PPC34C60 to recognize an edge.	125 [3 SCLK]			ns
t5	Once the Host has latched the Data on HD[0:7] it asserts the nSTB signal to inform the PPC34C60 to fetch another byte of data. If the PPC34C60 has to perform a DRAM or BUS cycle it may have to assert the BSY signal until it has completed the cycle and has placed valid data on HD[0:7]. This time represents the time from the assertion of nSTB to the assertion of BSY when appropriate.	334 [8 SCLK]		375 [9 SCLK]	ns
t6	Once the Host has latched the Data on HD[0:7] it asserts the nSTB signal to inform the PPC34C60 to fetch another byte of data. This time represents the time that the HD[0:7] data will remain valid from the assertion of nSTB.	84 [2 SCLK]		125 [3 SCLK]	ns
t7	This time (+t6) represents the time it takes the PPC34C60 to fetch and present the next valid data byte on the HD[0:7] lines. This time will vary significantly based on the type of access and the BCLK currently selected. These values are based on BCLK = 2 SCLK.	250 [6 SCLK]		1,292 [5 SCLK] + [13 BCLK]	ns
t8	nINIT controls the direction of the parallel port when in SPP mode. nINIT deasserted to HD[0:7] released to high impedance by the PPC34C60.	84 [2 SCLK]		125 [3 SCLK]	ns

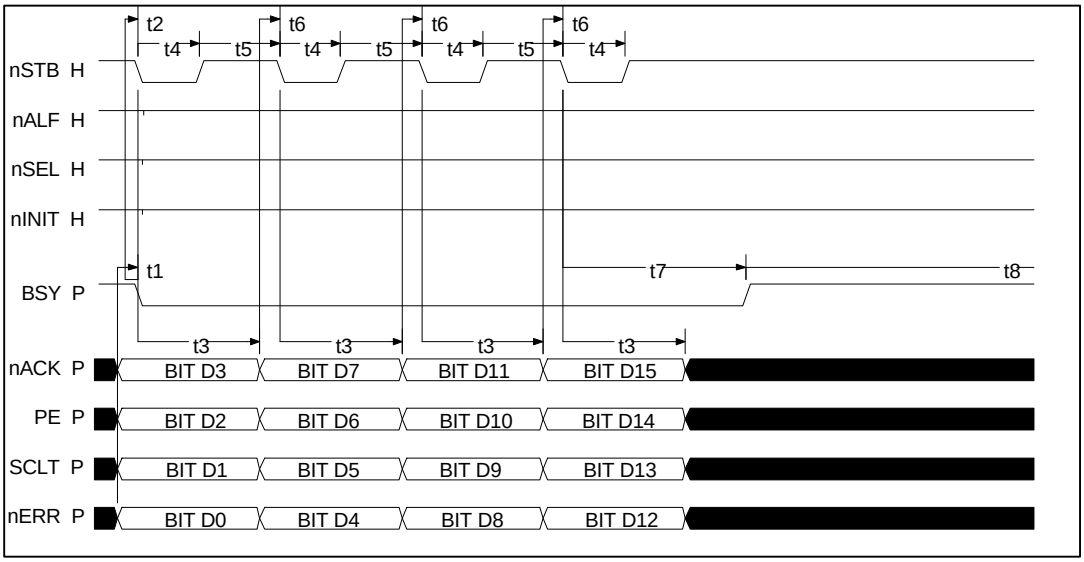


FIGURE 14 - SPP NIBBLE READ (PARALLEL PORT SIGNALS)

This signaling sequence pertains to a device that has been previously selected to communicate via SPP Mode. This timing sequence deviates from that specified in the P1284 specification. It is implemented in a way that requires less host software overhead and therefore affords higher bandwidth.

The timing shown is for a nibble read of a 16 bit wide resource (DRAM or peripheral BUS). See Page 51 for SPP Nibble Read Timing parameters.

SPP NIBBLE READ (PARALLEL PORT SIGNALS)

	Parameter	min	typ	max	units
t1	The PPC34C60 assembles a nibble of data and places it on the status lines. The PPC34C60 then deasserts the BSY signal to inform the Host that a valid nibble is available.			42 [SCLK]	ns
t2	Once the Host senses that the BSY line is deasserted it will then internally latch the nibble and then assert nSTB to tell the PPC34C60 to get the next nibble.	0			ns
t3	It will take the PPC34C60 this amount of time to fetch and present the next nibble of data.			250 [6 SCLK]	ns
t4	nSTB asserted pulse width	125 [3 SCLK]			ns
t5	nSTB deasserted pulse width	125 [3 SCLK]			ns
t6	Once the PPC34C60 has placed the next nibble, this is the time for the Host to latch the nibble and then assert nSTB to tell the PPC34C60 to get the next nibble.	42 [SCLK]			ns
t7	Once the Host has latched the last nibble it asserts the nSTB signal to inform the PPC34C60 to fetch another more data. If the PPC34C60 has to perform a DRAM or BUS cycle it may have to assert the BSY signal until it has completed the cycle and has placed a valid nibble on the status lines. This time represents the time from the assertion of nSTB to the assertion of BSY when appropriate.	334 [8 SCLK]		375 [9 SCLK]	ns
t8	This time represents the time it takes the PPC34C60 to fetch and present the next valid nibble on the status lines. This time will vary significantly based on the type of access and the BCLK currently selected. These values are based on BCLK = 2 SCLK.	0		1,084 [13 BCLK]	ns

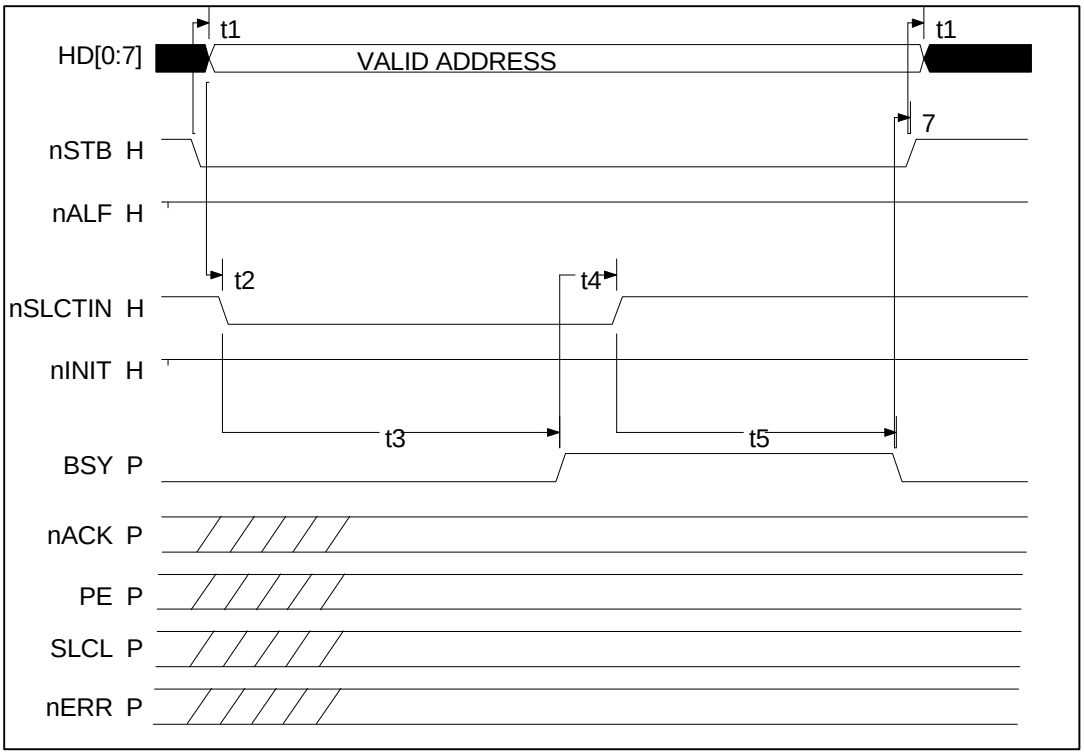


FIGURE 15 - EPP ADDRESS WRITE (PARALLEL PORT SIGNALS)

EPP timing is IEEE P1284 compatible except the PPC34C60:

1) Does not use nINIT to terminate EPP Mode (return to compatibility mode)
2) Does not support using nACK to generate interrupts to the Host while selected.

See Page 53 for EPP Address Write Timing Parameters.

EPP ADDRESS WRITE (PARALLEL PORT SIGNALS)

	Parameter	min	typ	max	units
t1	The Host asserts nSTB. At the same time the Host places the address byte on HD[0:7]. This specifies the jitter between nSTB being asserted and an address appearing on HD[0:7]. The PPC34C60 does not rely on nSTB.	0		50	ns
t2	The nSLCTIN signal is asserted coincident with the above events to indicate that an EPP address cycle is to take place. This time represents the jitter margin between nSLCTIN asserted and the above two events.	0		50	ns
t3	The PPC34C60 will detect the assertion of nSLCTIN and will assert BSY to indicate that it has latched the address on HD[0:7].	250 [6 SCLK]		10,000	ns
t4	After the PPC34C60 asserts BSY the Host will then indicate that the cycle is complete by deasserting nSLCTIN. This represents the response time requirements put on the Host.	42 [SCLK]			ns
t5	Seeing that the Host has indicated that the cycle is complete, the PPC34C60 will then deassert the BSY line as soon as it is ready for another EPP transfer.			209 [5 SCLK]	ns
t6	As soon as the PPC34C60 deasserts BSY the Host may initiate another EPP transfer. This time represents the time between the PPC34C60 deasserting BSY to the Host starting a new transfer cycle.	0			ns

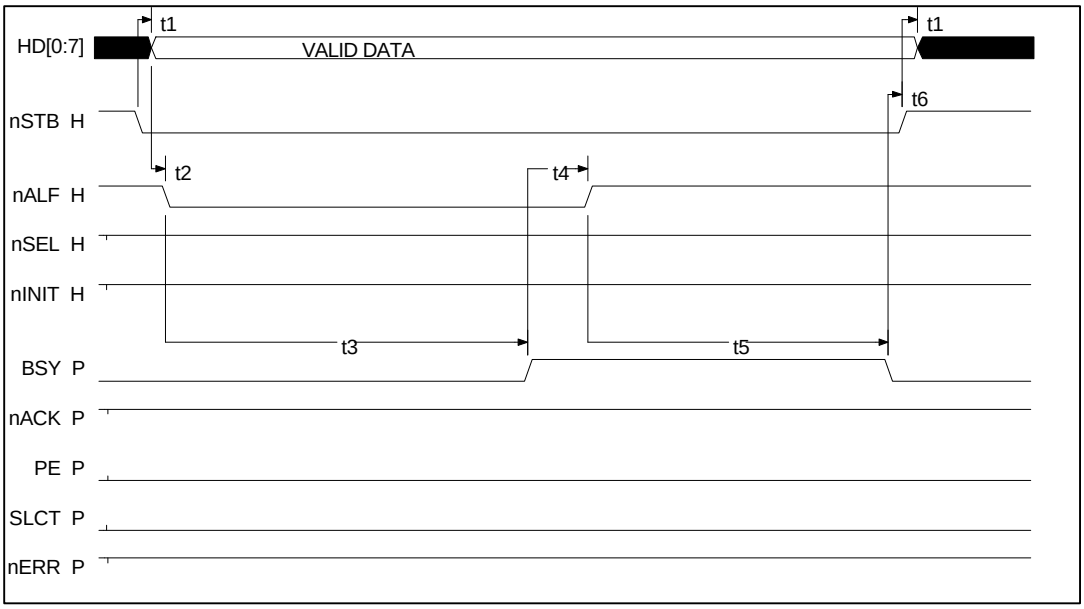


FIGURE 16 - EPP DATA WRITE TIMING (PARALLEL PORT SIGNALS)

See Page 55 for EPP Data Write Timing parameters.

EPP DATA WRITE TIMING (PARALLEL PORT SIGNALS)

	Parameter	min	typ	max	units
t1	The Host asserts nSTB to indicate that the forthcoming transfer is a write cycle. At the same time or soon after the Host places the address byte on HD[0:7]. This specifies the time between nSTB being asserted and an address appearing on HD[0:7]. The PPC34C60 does not rely on nSTB.	0			ns
t2	After placing an address on HD[0:7], the Host then asserts nALF to inform the PPC34C60 that a data cycle is taking place.	0			ns
t3	The PPC34C60 will detect the assertion of nALF and will assert BSY to indicate that it has latched the data on HD[0:7].	250 [6 SCLK]		10,000	ns
t4	After the PPC34C60 asserts BSY the Host will then indicate that the cycle is complete by deasserting nALF. This represents the response time requirements put on the Host.	42 [SCLK]			
t5	Seeing that the Host has indicated that the cycle is complete, the PPC34C60 will then deassert the BSY line as soon as it is ready for another EPP transfer.			209 [5 SCLK]	ns
t6	As soon as the PPC34C60 deasserts BSY the Host may initiate another EPP transfer. This time represents the time between the PPC34C60 deasserting BSY to the Host starting a new transfer cycle.	0			ns

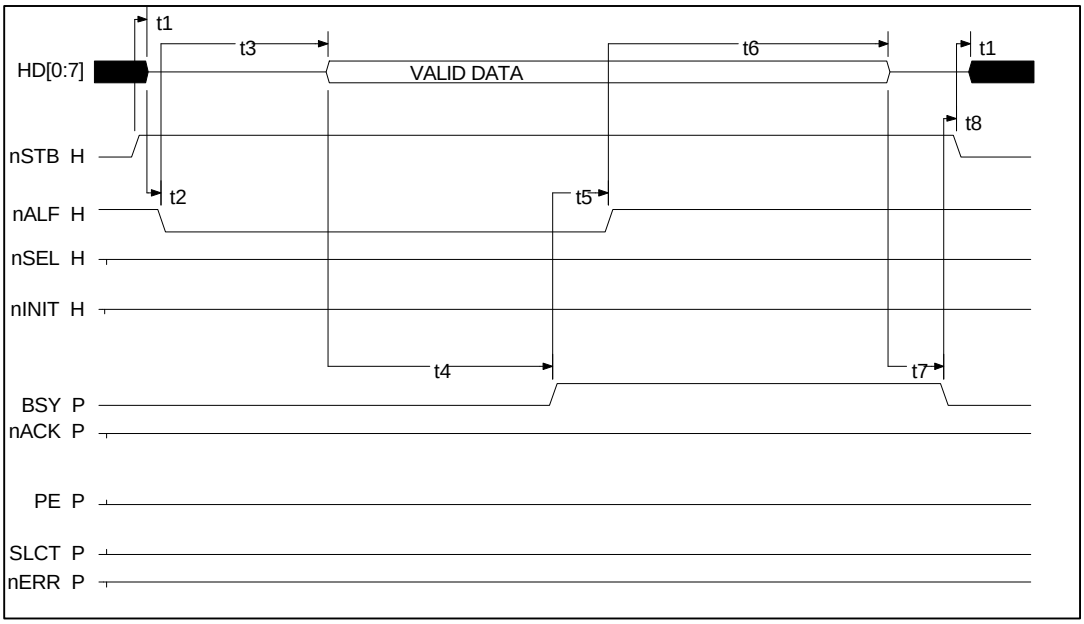


FIGURE 17 - EPP DATA READ TIMING (PARALLEL PORT SIGNALS)

See Page 57 for EPP Data Read Timing Parameters.

EPP DATA READ TIMING (PARALLEL PORT SIGNALS)

	Parameter	min	typ	max	units
t1	The Host deasserts nSTB to indicate that the forthcoming transfer is a read cycle. At the same time or soon after the Host will release the Parallel port data lines HD[0:7] to a high impedance state. This specifies the time between nSTB being asserted and an address appearing on HD[0:7].The PPC34C60 does not rely on nSTB.	0			
t2	After tri-stating the HD[0:7] lines, the Host then asserts nALF to inform the PPC34C60 that a data cycle is taking place.	0			
t3	The PPC34C60 will respond by placing data on HD[0:7].	125 [3 SCLK]		1,084 [13 BCLK]	ns
t4	Then the PPC34C60 will assert the BSY line to inform the Host that it has placed a valid byte of data on the parallel port data lines HD[0:7].	125 [3 SCLK]		167 [4 SCLK]	ns
t5	Next, the Host latches the data on HD[0:7] and deasserts nALF to inform the PPC34C60 that the cycle is complete.	42 [SCLK]			ns
t6	In response, the PPC34C60 tri-states the parallel port data lines HD[0:7].			209 [5 SCLK]	ns
t7	After tri-stating HD[0:7] the PPC34C60 deassert BSY to indicate that it is now ready for the next EPP transfer.			42 [SCLK]	ns
t8	As soon as the PPC34C60 deasserts BSY the Host may initiate another EPP transfer. This time represents the time between the PPC34C60 deasserting BSY to the Host starting a new transfer cycle.	0			ns

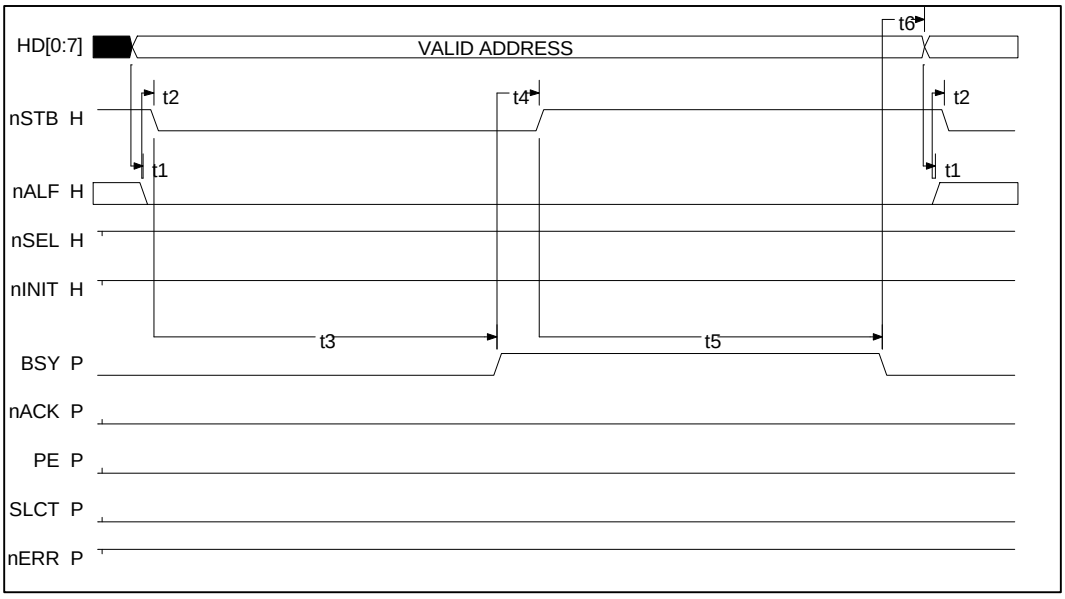


FIGURE 18 - ECP FORWARD COMMAND TRANSFER TIMING
(ECP ADDRESS WRITE, PARALLEL PORT SIGNALS)

See Page 59 for ECP Forward Command Transfer Timing Parameters

ECP FORWARD COMMAND TRANSFER TIMING
(ECP ADDRESS WRITE, PARALLEL PORT SIGNALS)

	Parameter	min	typ	max	units
t1	The Host places data on HD[0:7] and at the same time asserts nALF to indicate that this is a Command transfer. (the PPC34C60 supports Address commands, not RLE commands)	0			ns
t2	After placing data on HD[0:7] and asserting nALF, the host is required to meet this setup time before asserting nSTB. Assetion of nSTB informs the PPC34C60 that valid data is on HD[0:7] and that nALF is valid.	0			ns
t3	The peripheral acknowledges by asserting BSY.	334 [8 SCLK]			ns
t4	Once the peripheral has sent its acknowledgement the Host deasserts nSTB to continue the handshake. The PPC34C60 latches the address data on this rising edge of nSTB.	42 [SCLK]			ns
t5	As soon as the PPC34C60 has accepted the data and is ready to accept another byte it deasserts the BSY signal.	334 [8 SCLK]			ns
t6	Once the PPC34C60 has indicated it is ready to receive another byte of data from the Host, the Host if and when ready will place another byte on HD[0:7]. This time is the time required between the deassertion of BSY and new valid data on HD[0:7].	42 [SCLK]			ns

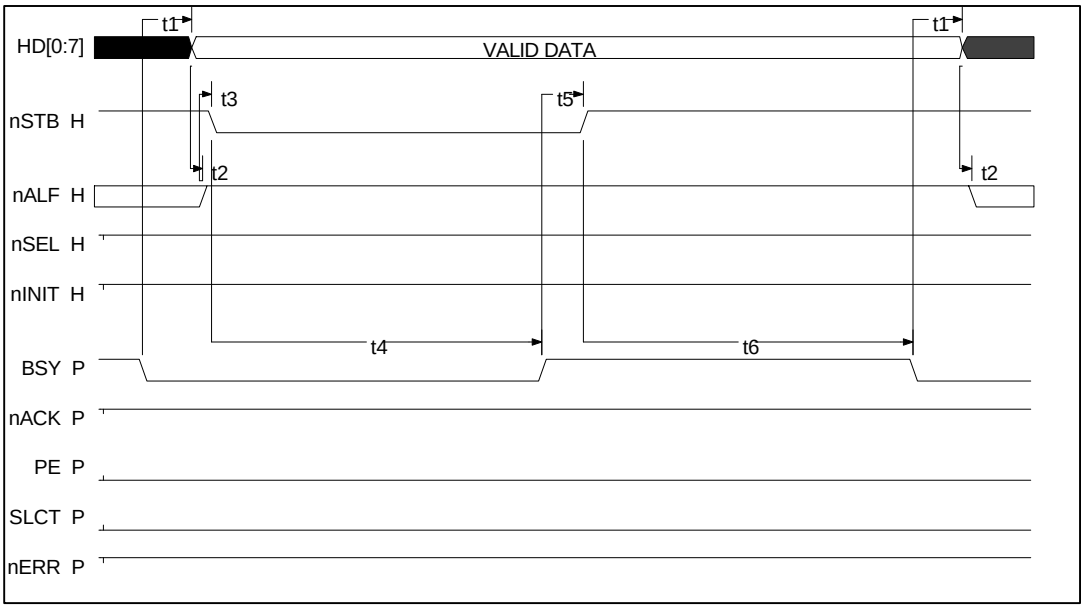


FIGURE 19 - ECP FORWARD DATA TRANSFER TIMING
(ECP DATA WRITE, PARALLEL PORT SIGNALS)

See Page 61 for ECP Forward Data Transfer Timing Parameters

ECP FORWARD DATA TRANSFER TIMING
(ECP DATA WRITE, PARALLEL PORT SIGNALS)

	Parameter	min	typ	max	units
t1	The PPC34C60 indicates it is ready to receive another byte of data from the Host by deasserting BSY. The Host if and when ready will place a byte on HD[0:7]. This time is the time required between the deassertion of BSY and data on HD[0:7].	42 [SCLK]			ns
t2	The Host places data on HD[0:7] and at the same time deasserts nALF to indicate that this is a Data transfer.	0			ns
t3	After placing data on HD[0:7] and deasserting nALF, the host is required to meet this setup time before asserting nSTB. Assetion of nSTB informs the PPC34C60 that valid data is on HD[0:7] and that nALF is valid.	0			ns
t4	The peripheral acknowledges by asserting BSY.	334 [8 SCLK]			ns
t5	Once the peripheral has sent its acknowledgement the Host deasserts nSTB to continue the handshake. The PPC34C60 latches the data on this rising edge of nSTB.	42 [SCLK]			ns
t6	As soon as the PPC34C60 has accepted the data and is ready to accept another byte it deasserts the BSY signal.	334 [8 SCLK]			ns

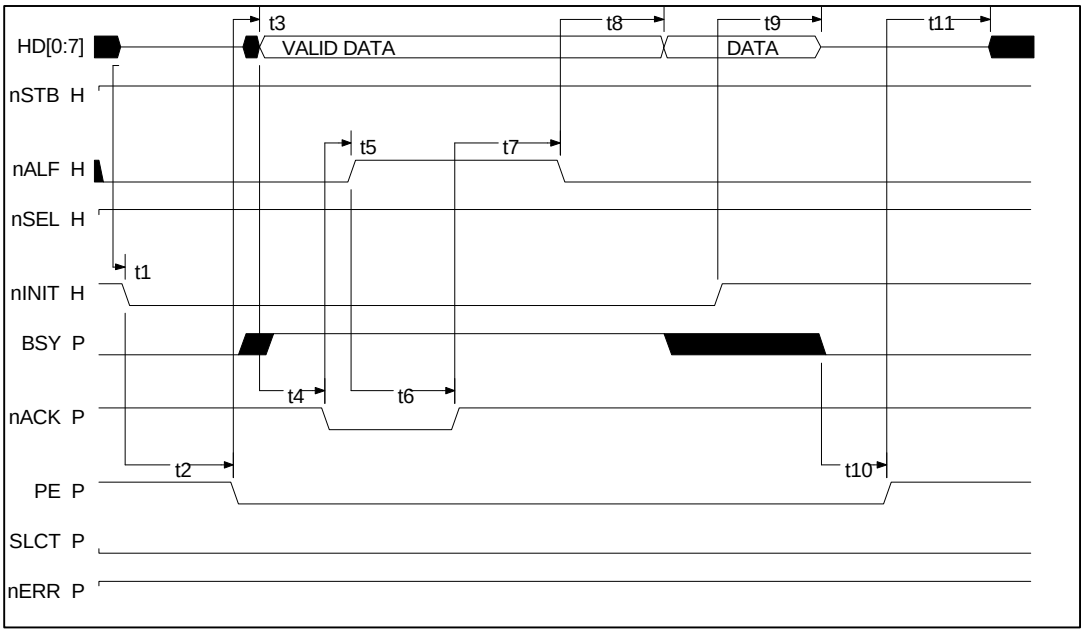


FIGURE 20 - ECP REVERSE DATA TRANSFER TIMING
(ECP DATA READ, PARALLEL PORT SIGNALS)

Note: The optional use of the nERR (nFAULT) line to "hint" to the Host that the peripheral has data to send to the Host is not supported in the PPC34C60. The driver should ignore any activity on this line. The PPC34C60 supports reverse data transfers only (not reverse command transfers) and, therefore, always asserts the BSY (nCMD) signal during reverse transfers.

See Page 63 for ECP Reverse Data Transfer Timing Parameters.

ECP REVERSE DATA TRANSFER TIMING (ECP DATA READ, PARALLEL PORT SIGNALS)

	Parameter	min	typ	max	units
t1	To prepare for an ECP reverse channel transfer the Host tri-states the parallel data lines HD[0:7] and asserts nALF at the same time. Next the Host asserts nINIT to initiate an ECP bus reversal. The PPC34C60 requires this amout of time between these events.	0			ns
t2	The PPC34C60 acknowledges the bus reversal by deasserting the PE signal. At this point in time the parallel port bus is in the reverse idle state.	208 [5 SCLK]		334 [8 SCLK]	ns
t3	Along with deasserting the PE signal the PPC34C60 takes control of the parallel port data bus HD[0:7]. The data on this bus remains undefined until the PPC34C60 has accessed and placed a data byte on the bus. Along with driving the data lines with valid data, the PPC34C60 asserts BSY to indicate that this is a data transfer.	0		1,084 [13 BCLK]	ns
t4	After placing data on the parallel port data lines the PPC34C60 asserts nACK to inform the Host that valid data is available.	125 [3 SCLK]		167 [4 SCLK]	ns
t5	Next, the Host will acknowledge that it is ready for the data by deasserting nALF.	50		infinite	ns
t6	Now the PPC34C60 will deassert nACK in response to the Host. The Host will latch the data on HD[0:7] on this rising edge of nACK.	125 [3 SCLK]		167 [4 SCLK]	ns
t7	The Host completes the ECP reverse transfer, acknowledging that it has accepted the data byte by asserting nALF.	50ns		1s	
t8	At the completion of the ECP reverse transfer cycle the PPC34C60 either places another valid data byte on the data lines or if it has no more data to send goes into the idle state driving undefined data onto the parallel port bus lines. As long as the port is in the reverse transfer mode, the PPC34C60 will always return data when a byte is requested. Once HOST MAX BLOCK byte-count has been reached, the PPC34C60 will present "pad" bytes to the host. The Host will discard any extra bytes received. The extra "pad" bytes are useful to provide alignment to wider buses.	125 [3 SCLK]		167 [4 SCLK]	ns
t9	The Host requests that the parallel port be placed back into the forward direction by deasserting nINIT, and in response to this the PPC34C60 will terminate any ongoing data transfer and place the data bus HD[0:7] in a high impedance state and deassert the BSY line.	125 [3 SCLK]		167 [4 SCLK]	ns
t10	After releasing the bus, the PPC34C60 acknowledges that it has relinquished the bus by asserting the PE signal.	0		125 [3 SCLK]	ns
t11	After the PPC34C60 has indicated that it has relinquished the bus, the Host may drive the data bus.	0	500		ns

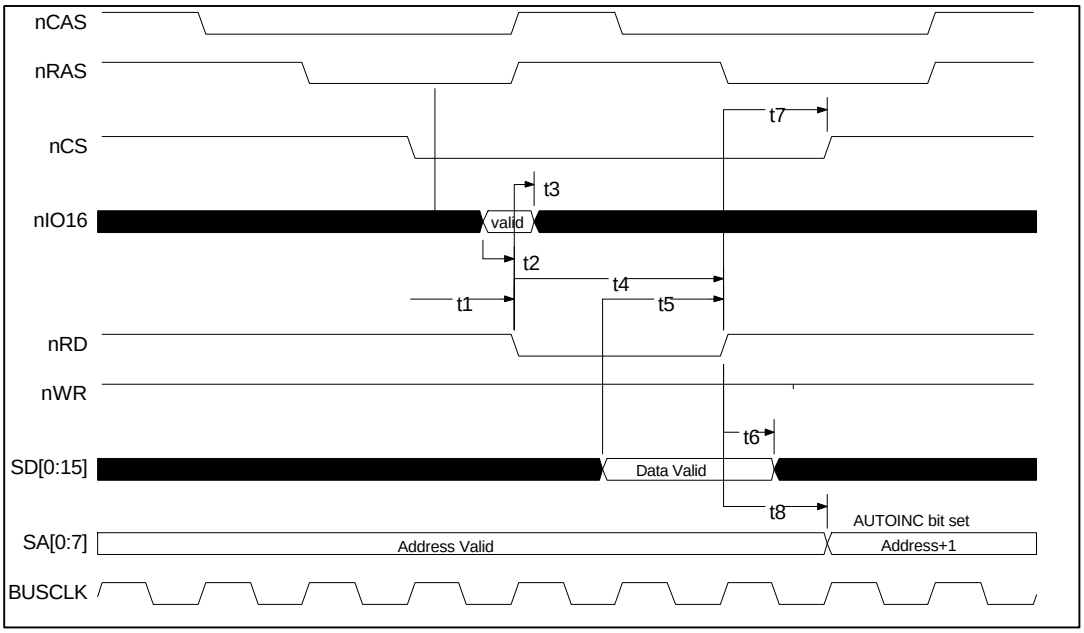


FIGURE 21 - PERIPHERAL BUS READ CYCLE TIMING

	Parameter	min	typ	max	units
t1	nCS asserted to nWR asserted. This applies to any and all of the general purpose output pins that have been configured to operate as "special function" Chip Select pins. This feature saves the designer from having to implement costly address decoders.	74 [1 BCLK -10]	84 [1 BCLK]	94 [1BCLK +10]	ns
t2	nIO16 setup required to the assertion of nRD.	15			ns
t3	nIO16 hold time required from the assertion of nRD.	10			ns
t4	nRD asserted pulse width.	158 [2 BCLK - 10]	168 [2 BCLK]	178 [2 BCLK +10]	ns
t5	Data valid setup time required to deassertion of nRD.	15			ns
t6	Data valid hold time required from deassertion of nRD.	10			ns
t7	nRD deasserted to nCS deasserted.	74 [1 BCLK -10]	84 [1 BCLK]	94 [1BCLK +10]	ns
t8	nRD deasserted to the address incremented (this is valid only if the AUTOINC bit is set).	74 [1 BCLK -10]	84 [1 BCLK]	94 [1BCLK +10]	ns

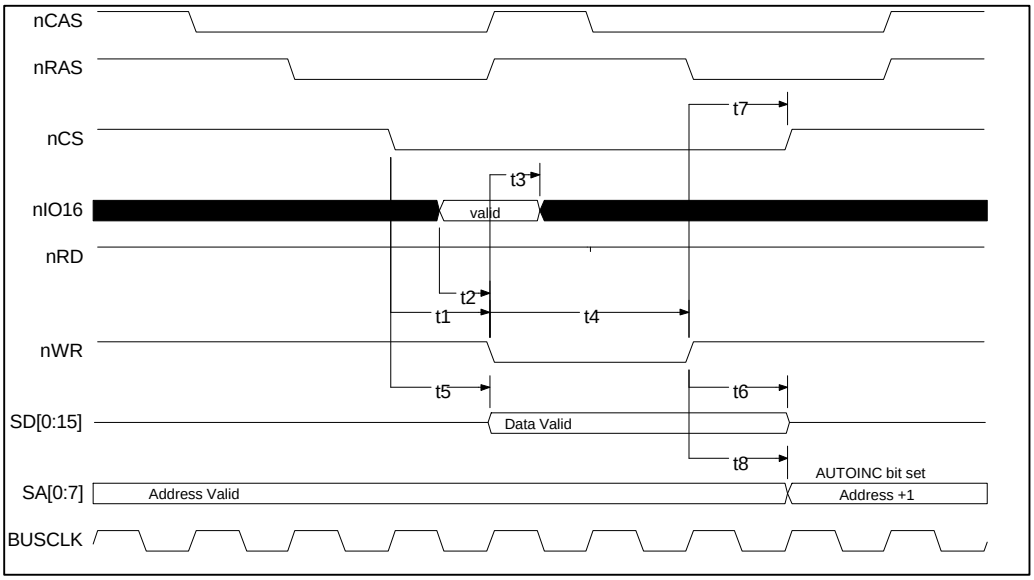


FIGURE 22 - PERIPHERAL BUS WRITE CYCLE TIMING

	Parameter	min	typ	max	units
t1	nCS asserted to nWR asserted. This applies to any and all of the general purpose output pins that have been configured to operate as "special function" Chip Select pins. This feature saves the designer from having to implement costly address decoders.	74 [1 BCLK-10]	84 [1 BCLK]	94 [1BCLK+10]	ns
t2	nIO16 setup required to the assertion of nWR.	15			ns
t3	nIO16 hold time required from the assertion of nWR.	10			ns
t4	nWR asserted pulse width.	158 [2 BCLK-10]	168 [2 BCLK]	178 [2BCLK+10]	ns
t5	Write data valid from the assertion of nCS.	74 [1 BCLK-10]	84 [1 BCLK]	94 [1BCLK+10]	ns
t6	Write data valid hold time from the deassertion of nWR.	74 [1 BCLK-10]	84 [1 BCLK]	94 [1BCLK+10]	ns
t7	nWR deasserted to nCS deasserted.	74 [1 BCLK-10]	84 [1 BCLK]	94 [1BCLK+10]	ns
T8	nWR deasserted to the address incremented (this is valid only if the AUTOINC bit is set).	74 [1 BCLK-10]	84 [1 BCLK]	94 [1BCLK+10]	ns

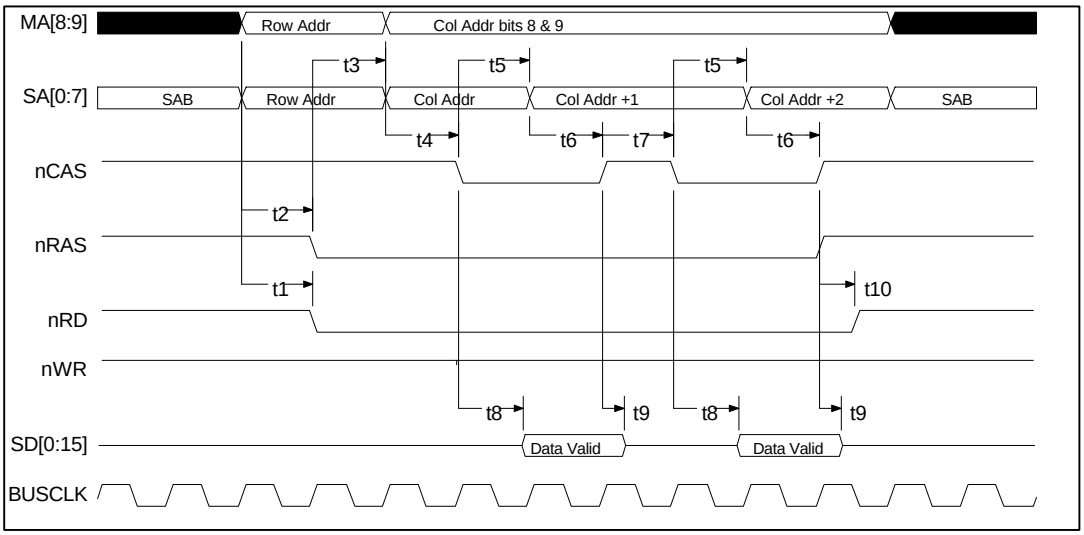


FIGURE 23 – DRAM READ CYCLE TIMING

When the DRAM bus width (4, 8 or 16 bits) is narrower than the Host bus (always 8-bits) or the Peripheral bus (8 or 16 bits) than the PPC34C60 will implement fast page mode DRAM cycles to complete the data transfer. These page mode transfers are performed for DMA as well as Host DRAM access.

See Page 67 for DRAM Read Cycle Timing Parameters.

DRAM READ CYCLE TIMING

	Parameter	min	typ	max	units
t1	10-bit DRAM row address valid to nRD asserted.	74 [1 BCLK -10]	84 [1 BCLK]	94 [1BCLK +10]	ns
t2	10-bit DRAM row address valid to nRAS asserted.	74 [1 BCLK -10]	84 [1 BCLK]	94 [1BCLK +10]	ns
t3	nRAS asserted to valid 10-bit DRAM column address.	74 [1 BCLK -10]	84 [1 BCLK]	94 [1BCLK +10]	ns
t4	10-bit DRAM column address valid to nCAS asserted.	74 [1 BCLK -10]	84 [1 BCLK]	94 [1BCLK +10]	ns
t5	10-bit DRAM column address incremented and at the same time the data is latched into the PPC34C60 following nCAS asserted.	74 [1 BCLK -10]	84 [1 BCLK]	94 [1BCLK +10]	ns
t6	nCAS deasserted after the column address has been updated and the data has been latched by the PPC34C60.	74 [1 BCLK -10]	84 [1 BCLK]	94 [1BCLK +10]	ns
t7	nCAS deasserted pulse width during page mode accesses.	74 [1 BCLK -10]	84 [1 BCLK]	94 [1BCLK +10]	ns
t8	nCAS asserted to valid data, i.e., maximum acceptable DRAM access time.	0		74 [1BCLK -10]	ns
t9	nCAS deasserted to DRAM releasing data from the bus.	0		74 [1BCLK -10]	ns
t10	nCAS and nRAS both deasserted to nRD deasserted.	0		42 [1 SCLK]	ns

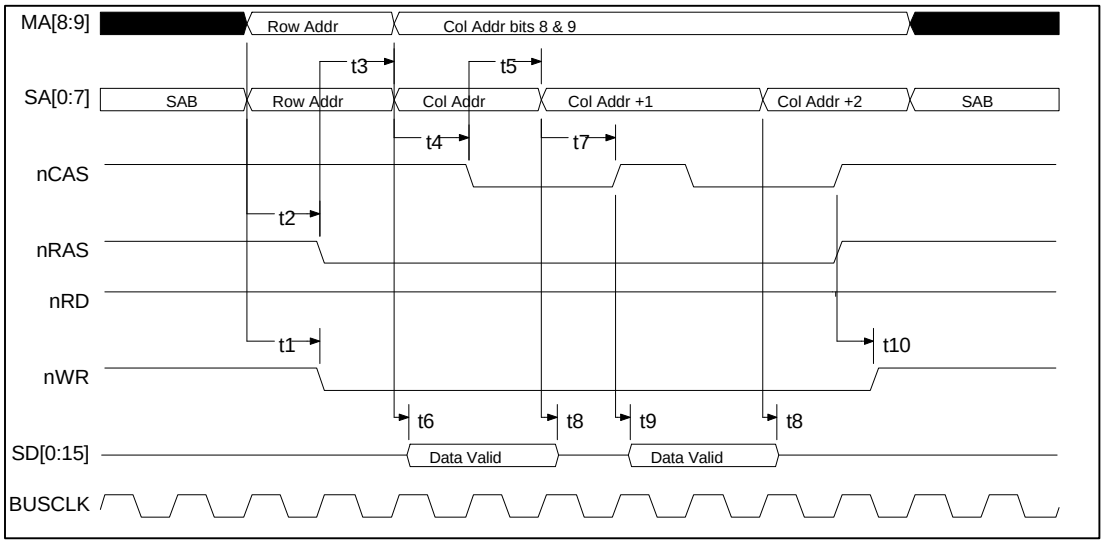


FIGURE 24 - DRAM WRITE CYCLE TIMING

When the DRAM bus width (4, 8 or 16 bits) is narrower than the Host bus (always 8-bits) or the Peripheral bus (8 or 16 bits) than the PPC34C60 will implement fast page mode DRAM cycles to complete the data transfer. These page mode transfers are performed for DMA as well as Host DRAM access.

See Page 69 for DRAM Write Cycle Timing parameters.

DRAM WRITE CYCLE TIMING

	Parameter	min	typ	max	units
t1	10-bit DRAM row address valid to nWR asserted.	74 [1 BCLK -10]	84 [1 BCLK]	94 [1BCLK +10]	ns
t2	10-bit DRAM row address valid to nRAS asserted.	74 [1 BCLK -10]	84 [1 BCLK]	94 [1BCLK +10]	ns
t3	nRAS asserted to valid 10-bit DRAM column address.	74 [1 BCLK -10]	84 [1 BCLK]	94 [1BCLK +10]	ns
t4	10-bit DRAM column address valid to nCAS asserted.	74 [1 BCLK -10]	84 [1 BCLK]	94 [1BCLK +10]	ns
t5	10-bit DRAM column address incremented following nCAS asserted.	74 [1 BCLK -10]	84 [1 BCLK]	94 [1BCLK +10]	ns
t6	Valid write data in relation to the 10-bit column address presented by the PPC34C60.	0		10	ns
t7	DRAM column address incremented to nCAS deasserted.	74 [1 BCLK -10]	84 [1 BCLK]	94 [1BCLK +10]	ns
t8	Valid write data in relation to the 10-bit column address presented by the PPC34C60.	0		10	ns
t9	nCAS deasserted to valid data placed on the data bus.	0		10	ns
t10	nCAS and nRAS both deasserted to nWR deasserted.	0		42 [1 SCLK]	ns

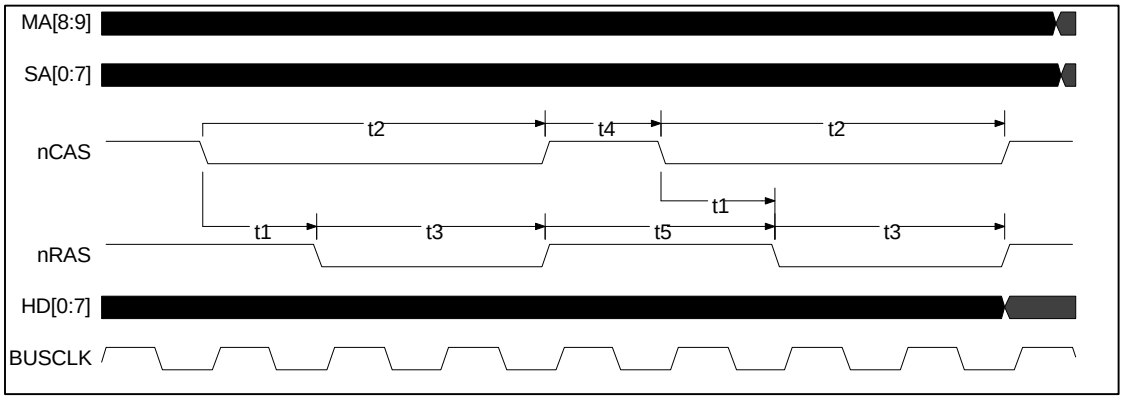


FIGURE 25 – DRAM WRITE REFRESH CYCLE

	Parameter	min	typ	max	units
t1	nCAS asserted to nRAS asserted.	74 [1 BCLK -10]	84 [1 BCLK]	94 [1BCLK +10]	ns
t2	nCAS asserted pulse width	242 [3 BCLK -10]	252 [3 BCLK]	262 [3 BCLK +10]	ns
t3	nRAS asserted pulse width	158 [2 BCLK -10]	168 [2 BCLK]	178 [2 BCLK +10]	ns
t4	nCAS deasserted pulse width	74 [1 BCLK -10]	84 [1 BCLK]	94 [1 BCLK +10]	ns
t5	nRAS deasserted pulse width	158 [2 BCLK -10]	168 [2 BCLK]	178 [2 BCLK +10]	ns

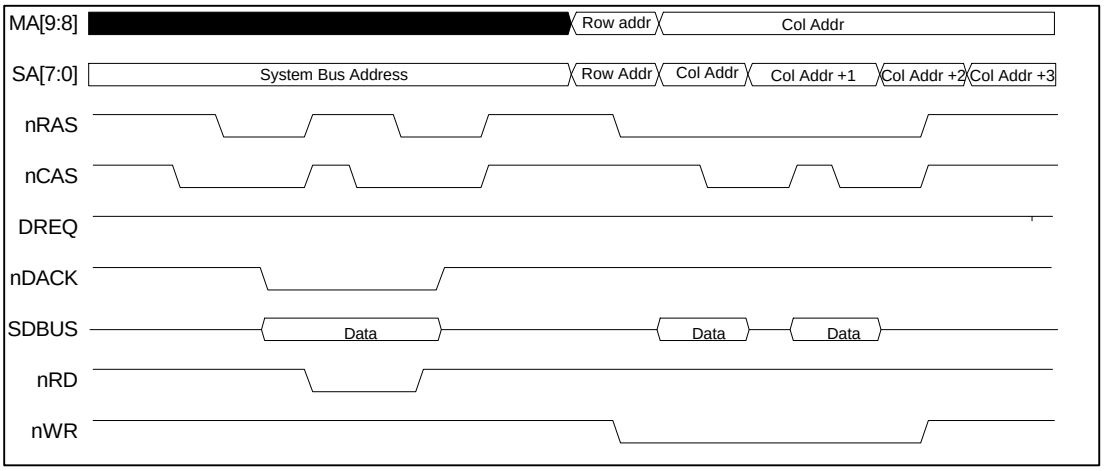


FIGURE 26 - DMA TRANSFER CYCLE TIMING

[8-bit peripheral system bus to 4-bit DRAM], (D16=0, RAMSZ[1:0]=[0,0])
[16-bit peripheral system bus to 8-bit DRAM], (D16=1, RAMSZ[1:0]=[0,1])

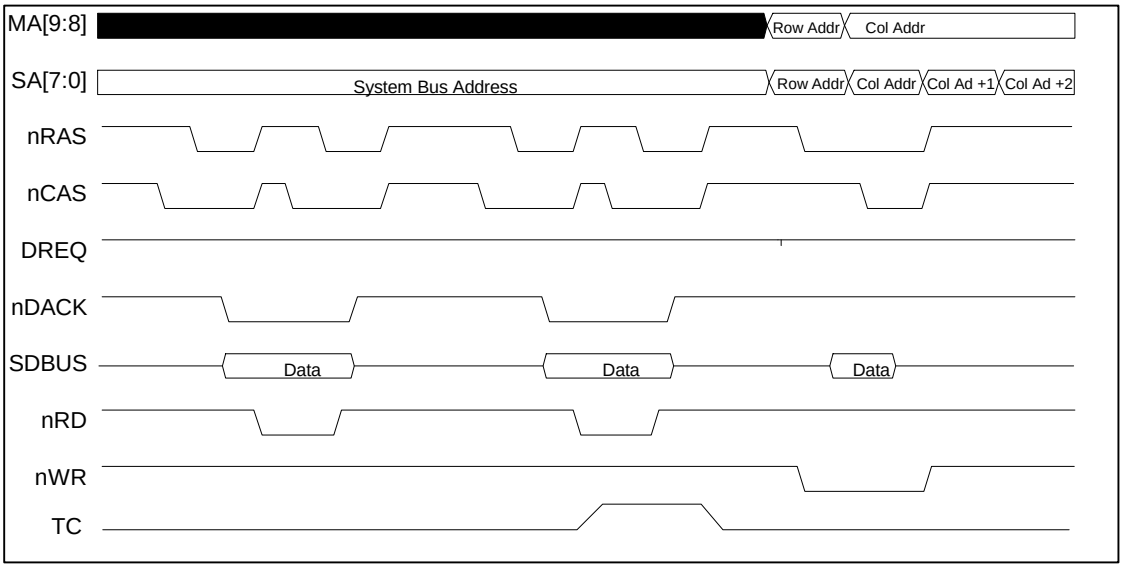


FIGURE 27 - DMA TRANSFER CYCLE TIMING

[8-bit peripheral system bus to 16-bit DRAM], (D16=0, RAMSZ[1:0]=[1,X]). DMA Tern=minal Count goes high coincident with nDACK for last transfer. See Page 72 for DMA Transfer Cycle Timing Parameters.

DMA TRANSFER CYCLE TIMING

DMA Transfer Type (peripheral bus <--> DRAM)		DMA Transfer Cycle	DMA Transfer Rate
Peripheral Bus Width	DRAM Width		
8	8	1,333 [16 BCLK]	750 KB/S
8	4	1,583 [19 BCLK]	631,578 KB/S
16	16	1,333 [16 BCLK]	1.5 MB/S
16	8	1,583 [19 BCLK]	1.263 MB/S
16	4	2,083 [25 BCLK]	960 KB/S

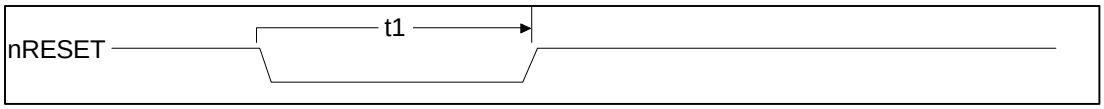


FIGURE 28 – RESET TIMING

	Parameter	min	typ	max	units
t1	Reset pulse width	84 [2 SCLK]			ns

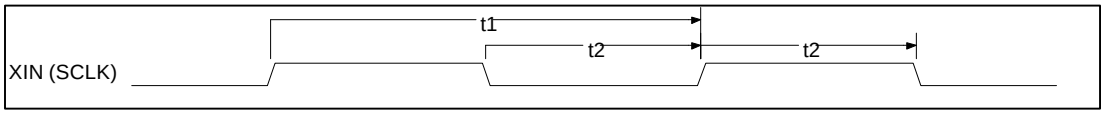
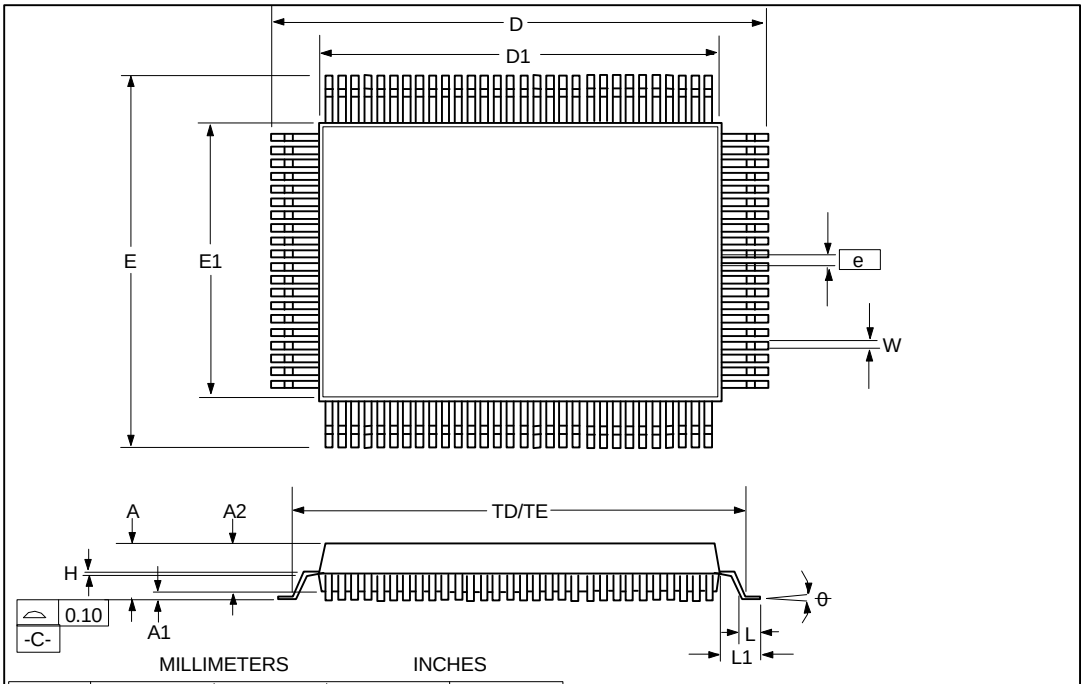


FIGURE 29 – CLOCK TIMING

	Parameter	min	typ	max	units
t1	Clock Period (max SCLK=25MHz)	40	41.67		ns
t2	Clock active high or low	14			ns
tr	Clock Rise time (Vin = 0.4 to 3.0 V)			5	ns
tf	Clock Fall time (Vin = 3.0 to 0.4 V)			5	ns



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.15	.110	.124
A1	0.1	0.45	.004	.018
A2	2.57	2.87	.101	.113
D	23.4	24.15	.921	.951
D1	19.9	20.1	.783	.791
E	17.4	18.15	.685	.715
E1	13.9	14.1	.547	.555
H	0.1	0.2	.004	.008
L	0.65	0.95	.026	.037
L1	1.8	2.6	.071	.102
e	0.65 BSC		.0256 BSC	
θ	0°	12°	0°	12°
W	.2	.4	.008	.016
TD(1)	21.8	22.2	.858	.874
TE(1)	15.8	16.2	.622	.638
TD(2)	22.21	22.76	.874	.896
TE(2)	16.27	16.82	.641	.662

Notes:

1) Coplanarity is 0.100mm (.004") maximum.

2) Tolerance on the position of the leads is 0.200mm (.008") maximum.

3) Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25mm (.010").

4) Dimensions TD and TE are important for testing by robotic handler. Only above combinations of (1) or (2) are acceptable.

5) Controlling dimension: millimeter. Dimensions in inches for reference only and not necessarily accurate.

FIGURE 30 - 100 PIN QFP PACKAGE OUTLINES

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