

AN 8.9

LAN91C96 Motorola 68000 Bus Mode

1 Introduction

The LAN91C96 is the most recent device in the LAN9000 family of fully integrated 10BaseT Ethernet controllers targeted for PC, mobile and embedded networking applications. Because of the LAN9000 family's broad use in embedded applications, the LAN91C96 implements a subset of the Motorola 68000 interface, allowing bus connections to Motorola 68000 family processors which also sees popular success in embedded applications. This application note provides details of the LAN91C96 Motorola 68000 interface, targeting developers with an understanding of ISA or Motorola 68000 bus interfaces. The application note begins with an overview of the LAN91C96 Ethernet controller followed by Motorola 68000 bus limitations of the LAN91C96. Pin functionality differences between ISA and Motorola 68000 bus modes are consolidated into easily read tables for quick reference. Configurations with popular Motorola 68000 processors provide a means of easy application integration. Finally, known LAN91C96 Motorola 68000 interface anomalies are detailed.

2 LAN91C96 Features

The LAN91C96 is an Ethernet controller implementing all MAC and physical layer functions required for 10BASE-T operation. By combining ISA, PCMCIA and Motorola 680000 bus interfaces, the LAN91C96 provides a cross platform solution with a flexible on board RAM and a flat memory structure. Advanced power management features and Magic Packet[™] conserve power, while an AUI interface expands physical media compatibility through the use of external 10BASE5, 10BASE2, and 10BASE-F transceivers. The LAN91C96 is pin and software compatible with the LAN91C94 and LAN91C92 allowing an easy upgrade path for earlier generation applications. Full duplex operation maximizes network performance. With serial EEPROM and ROM or Flash ROM interfaces, the LAN91C96 provides jumper less setup for ISA, PCMCIA or Motorola 68000 buses.



Figure 2.1 LAN91C96 SYSTEM BLOCK DIAGRAM



2.1 Motorola 68000 Bus Mode on the LAN91C96

When Motorola 68000 mode is entered (refer to section titled "Motorola 68000 Bus Mode Entry / Exit Sequence" for mode entry requirements), the functions of key ISA bus pins are replaced with Motorola 68000 signal functions. However, the LAN91C96 incorporates only a subset of the Motorola 68000 bus interface. The following limitations exist in Motorola 68000 bus mode:

Address Bus

The Motorola 68000 family of processors supports up to 16MB of byte addressable space. The LAN91C96 can only support word addressing in Motorola 68000 mode. For this reason, the A[0] pin should be tied low to limit all data accesses to 16-bit words. Additionally, the LAN91C96 uses only address lines A[15:0] for decode into the register space, limiting the device to the lower 32KB of addressable space.

Asynchronous Bus Control

The 16-bit processors in the Motorola 68000 family of processors implement the Lower Data Strobe (nLDS) and Upper Data Strobe (nUDS) signals. The LAN91C96 implements only one input, xDS, to replace these signals. Because the LAN91C96 bus interface is limited to 16-bit accesses, the signal xDS should be connected to nLDS on 16-bit processors. <u>The LAN91C96 will not work with 8-bit processors such as the MC68008</u>.

Data Bus

The LAN91C96 does not swap the low and high bytes of the data bus in Motorola 68000 mode. It is the responsibility of the user to wire the pins as needed (Little Endian or Big Endian ordering).

Bus Arbitration Control

Motorola 68000 family processors support bus arbitration for master and slave devices. Bus arbitration is not supported with the LAN91C96. As a result, the LAN91C96 should be implemented as a slave device. If no other devices exist in the system, the Motorola 68000 Bus Arbitration signals must be dealt with accordingly through the use of 10K pull-ups on nBR and nBGACK.

Interrupt Control

Interrupt control on a Motorola 68000 processor uses an encoded bit scheme. The LAN91C96 does not directly support and encoded interrupt scheme. Instead, a single interrupt pin is provided (INTR) that can be connected to any one of the available Motorola 68000 interrupt lines (IPL[2:0]) The remaining two interrupt lines should be encoded to zero through 10K pull-downs. When INTR is low, the Motorola 68000 will view the value on IPL[2:0] as no interrupt. When INTR is high, the Motorola 68000 will view the value on IPL[2:0] as an encoded interrupt where 7 is the highest priority.

System Reset

The Motorola 68000 family of processors defines reset as an active low state. The LAN91C96 defines reset as an active high state. In order to correctly wire the reset circuit, the reset signal from the Motorola 68000 processor must first be inverted.



2.2 ISA and Motorola 68000 Bus Mode Differences

The LAN91C96 supports asynchronous bus operation in ISA and Motorola 68000 bus. When the LAN91C96 is configured for ISA or Motorola 68000 bus mode, pin signal definitions change. Table 1 below details pin function differences between the two modes.

SIGNAL DESCRIPTION SIGNAL DESCRIPTION A[19:1] Input Address Bus A[19:1] Input Address Bus Address Bus A[0] Input Address Bus Low Bit Not Used Pull-down pin D[15:0] Input Data Bus D[15:0] Input Data Bus D[15:0] Input Data Bus Address Strobe Signifies a valid address is on the address bus nAS Address Strobe nIORD O Space Read xDS Data Strobe Signifies a valid address on the address bus nIOWR IO Space Write Cycle R/nW Read / Write Signifies a read cycle if high or a write cycle if low NBMEM Byte High Enable Input Not Used Pull-down pin Signifies a read cycle if high or a write cycle if low NBHE Byte High Enable Input Not Used Float pin Pull-down pin Signifies cycle is a ROM Memory Read Not Used Float pin Float pin Output Optionally used to extend host cycles if wait states required cycles if wait states required Not Used Float pin Output Orbin Select Not Used Float pin	ISA BUS MODE		MOTOROLA 68000 BUS MODE	
A119:11 InputAddress BusA119:11 InputAddress BusA[0] InputAddress Bus Low BitNot UsedPull-down pinA[0] InputData BusD[15:0] Input/ OutputData BusPull-down pinInput/ OutputSignifies a valid address is on the address busInput / OutputData BusNOR Do Signifies excle is a IO ReadNASAddress StrobeSignifies a valid address on the address busnIORDIO Space ReadXDSData StrobeInputSignifies cycle is a IO Read CycleNot UsedRead / Write Signifies a read cycle if high or a write cycle if lownIORDIO Space Write Signifies cycle is a IO Write CycleRinWRead / Write Signifies a read cycle if high or a write cycle if lownBHE InputByte High Enable Low value indicates valid data on the upper data byteNot UsedPull-down pinnMEMR InputExternal ROM Memory Read Signifies cycle is a ROM Memory ReadNot UsedPull-up pinInputFalling edge latches address and nSBHENot UsedFloat pinIOCHRDY OutputIO Channel Ready Cycles if wait states requiredNot UsedFloat pinIOCHRDY OutputIO Channel Ready Asserted when A[15:4] decoded to the value in the Base AddressNot UsedFloat pinINTR1 OutputInterrupt 0INT Single line interruptInputInputINTR3 OutputInterrupt 3nDTACK01Data Transfer Acknowledge Indicates data transfer complete.INTR3 Output<	SIGNAL	DESCRIPTION	SIGNAL	DESCRIPTION
Input Input Input A(0) Address Bus Low Bit Not Used Pull-down pin DpUt / Output Data Bus D[15:0] Data Bus Input / Output Address Enable nAS Address Strobe Input / Output Signifies a valid address is on the address bus NAS Data Strobe NIORD IO Space Read xDS Data Strobe Signifies address bus NIOWR IO Space Write RinW Signifies a log address address and and a bus signifies aread cycle is a ROM Memory Read Input Input Address Strobe Not Used Float pin Input Gotionally used to extend host cycles if wait states required Not Used Float pin Output Ortionally used to extend host ortion inthe address index address Regigiter Not	A[19:1]	Address Bus	A[19:1]	Address Bus
A[0] Input Address Bus Low Bit Not Used Pull-down pin D[15:0] Input / Output Data Bus D[15:0] Input / Output Data Bus AER Address Enable nAS Address Strobe Input Signifies a valid address is on the address bus nAS Address Strobe Input Signifies cycle is a IO Read Cycle xDS Data Strobe Input Signifies cycle is a IO Write Cycle NDW Signifies a valid address bus Input Signifies cycle is a IO Write Cycle RinW Signifies a valid obta on data bus NOWR IO Space Write Cycle Not Used Pull-down pin Input Signifies cycle is a IO Write Cycle Not Used Pull-down pin Input Signifies cycle is a ROM Memory Read Not Used Pull-down pin INMEMR External ROM Memory Read Signifies cycle is a ROM Memory Read Not Used Float pin Input Signifies cycle is a ROM Memory Read Not Used Float pin Output Othannel Ready Optionally used to extend host cycles if wait states required Not Used Float pin Output	Input		Input	
D15:01 Input / Output Data Bus D15:01 Input / Output Data Bus AKH Address Enable nAS Address Strobe Signifies a valid address is on the address bus Address Strobe Signifies a valid address on the address bus nIORD IO Space Read xDS Data Strobe Signifies valid data on data bus nIOWR IO Space Write R/nW Signifies valid data on data bus Signifies valid data on data bus nIOWR IO Space Write R/nW Signifies a read cycle if high or a write cycle if low Signifies a read cycle if high or a write cycle if low nBHE Byte High Enable Not Used Pull-down pin Float pin Input Signifies cycle is a ROM Memory Read Not Used Float pin Float pin Input Signifies cycle is a ROM Memory Read Not Used Float pin Float pin IOCHRDY Ochannel Ready Output Optionally used to extend host cycles if wait states required Not Used Float pin INCCS16 IOCHRDY Othe value in the Base Address Register Not Used Float pin INTR0 Interrupt 0 INT Int	A[0] Input	Address Bus Low Bit	Not Used	Pull-down pin
Input / Output Input / Output AEN Input Address Enable Signifies a valid address is on the address bus nAS Address Strobe NIORD IO Space Read Cycle xDS Data Strobe Input Signifies cycle is a IO Read Cycle xDS Data Strobe NIOWR IO Space Write Signifies cycle is a IO Write Cycle R/nW Read / Write Signifies a read cycle if high or a write cycle if low nSBHE Byte High Enable Low value indicates valid data on the upper data byte Not Used Float pin Input Signifies cycle is a ROM Memory Read Not Used Float pin Input Signifies cycle is a ROM Memory Read Not Used Pull-up pin Input Faling edge latches address and nSBHE Not Used Float pin IOCHRDY IO Channel Ready Output Not Used Float pin Output Asserted when A[15:4] decoded to the value in the Base Address Register Not Used Float pin Notuput Single line interrupt Output Unencoded interrupt tied to IPL0, IPL1 or IPL2 NTR1 Interrupt 1 Not Used Float pin Output <	D[15:0]	Data Bus	D[15:0]	Data Bus
AEN InputAddress Enable Signifies a valid address is on the address busnAS InputAddress Strobe Signifies a valid address on the address busnIORDIO Space Read CyclexDSData StrobeInputSignifies cycle is a IO Read CycleInputSignifies valid data on data bus CyclenIOWRIO Space Write CycleR/NWRead / WriteInputSignifies cycle is a IO Write CycleNot UsedRead / WritenBBHE InputByte High Enable Low value indicates valid data on the upper data byteNot UsedPull-down pinnMEMR InputExternal ROM Memory Read Signifies cycle is a ROM Memory ReadNot UsedFloat pinInputSignifies cycle is a address and nSBHENot UsedPull-up pinInputFiling edge latches address and cycles if wait states requiredNot UsedFloat pinIOCHRDY OutputIO Channel Ready Optionally used to extend host cycles if wait states requiredNot UsedFloat pinOutputIO Chip Select InputNot UsedFloat pinOutputSingle line interruptNot UsedFloat pinINTR0 OutputInterrupt 1 Single line interruptNot UsedFloat pinINTR1 OutputInterrupt 2 Single line interruptNot UsedFloat pinINTR2 OutputInterrupt 3 Single line interruptNot UsedFloat pinINTR3 OutputInterrupt 3 Single line interruptNot UsedFloat pinINTR3 OutputInterrupt 3 Sing	Input / Output		Input / Output	
Input Signifies a valid address is on the address bus Input Signifies a valid address on the address bus nIORD IO Space Read xDS Data Strobe Input Signifies cycle is a IO Read Cycle xDS Data Strobe nIOWR IO Space Write R/nW Read / Write Signifies cycle is a IO Write Cycle R/nW Read / Write Signifies aread cycle if high or a write cycle if high or a write cycle if low nSBHE Input Byte High Enable Low value indicates valid data on the upper data byte Not Used Pull-down pin nMEMR Input External ROM Memory Read Signifies cycle is a ROM Memory Read Not Used Float pin BALE Input Input Address Strobe Falling edge latches address and nSBHE Not Used Pull-up pin IOCHRDY Output IO Channel Ready cycles if wait states required Not Used Float pin IOCS16 Output IO Chip Select Not Used Float pin NITR0 Output Interrupt 0 INT Interrupt Not Used Float pin Interrupt Not Used Float pin Interrupt Output Single line interrupt	AEN	Address Enable	nAS	Address Strobe
nIORD InputIO Space Read Signifies cycle is a IO Read CyclexDS InputData Strobe Signifies valid data on data busnIOWR InputIO Space Write Signifies cycle is a IO Write CycleR/nW InputRead / Write Signifies a read cycle if high or a write cycle if lownSBHE InputByte High Enable Low value indicates valid data on the upper data byteNot UsedRead / Write Signifies cycle is a ROM Memory ReadNot UsedPull-down pinnMEMR InputExternal ROM Memory Read Signifies cycle is a ROM Memory ReadNot UsedFloat pinBALE InputInput Address Strobe Faling edge latches address and nSBHENot UsedPull-up pinIOC+IRDY OutputIO Channel Ready Optionally used to extend host cycles if wait states requiredNot UsedFloat pinIOCS16 OutputIO Chip Select Asserted when A[15:4] decoded to the value in the Base Address RegisterNot UsedFloat pinRESET OutputChip Reset Active highInput Input Active lowChip Reset Float pinChip Reset Float pinNTR0 OutputInterrupt 0INT Interrupt 0INT InterruptInterrupt OutputData Transfer Acknowledge Indicates data transfer complete. If processor is reading data is Iatched. If processor is writing, bus cycle is terminated.INTR3 OutputInterrupt 3nDTACK/1 OutputData Transfer Acknowledge Indicates data transfer complete. If proces	Input	Signifies a valid address is on the address bus	Input	Signifies a valid address on the address bus
Input Signifies cycle is a IO Read Cycle Input Signifies valid data on data bus NOWR IO Space Write Signifies cycle is a IO Write Cycle R/nW Read / Write Signifies a read cycle if high or a write cycle if low nSBHE Byte High Enable Input Not Used Pull-down pin Input Signifies cycle is a ROM Memory Read Not Used Float pin Input Signifies cycle is a ROM Memory Read Not Used Float pin Input External ROM Memory Read Signifies cycle is a ROM Memory Read Not Used Float pin Input Falling edge latches address and nSBHE Not Used Pull-up pin IOC HRDY O Channel Ready Output Not Used Float pin Output O Chip Select to the value in the Base Address Register Not Used Float pin RESET Chip Reset Input Reset Active low Interrupt Unencoded interrupt tied to IPL0, IPL1 or IPL2 Output Interrupt 1 Not Used Float pin Float pin INTR1 Interrupt 2 Not Used Float pin Interrupt Output Single line interrupt No	nIORD	IO Space Read	xDS	Data Strobe
nIOWR InputIO Space Write Signifies cycle is a IO Write CycleRhW InputRead / Write Signifies a read cycle if high or a write cycle if lownSBHE InputByte High Enable Low value indicates valid data on the upper data byteNot UsedPull-down pinnMEMR InputExternal ROM Memory Read Signifies cycle is a ROM Memory ReadNot UsedFloat pinBALE InputInput Address Strobe Falling edge latches address and nSBHENot UsedFloat pinIOC HRDY OutputOptionally used to extend host cycles if wait states requiredNot UsedFloat pinIOCS16 OutputIO Channel Ready Optionally used to extend host cycles if wait states requiredNot UsedFloat pinNIDCS16 OutputIO Chip Select Asserted when A[15:4] decoded to the value in the Base Address RegisterNot UsedFloat pinINTR0 OutputInterrupt 0INT Unencoded interrupt tied to IPL0, IPL1 or IPL2InterruptINTR1 OutputInterrupt 1 Single line interruptNot UsedFloat pinINTR2 OutputInterrupt 2 Single line interruptnDTACK/0 OutputData Transfer Acknowledge Indicates data transfer complete. If processor is writing, bus cycle is terminated.INTR3 OutputInterrupt 3 Single line interruptnDTACK/1 OutputData Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated.	Input	Signifies cycle is a IO Read Cycle	Input	Signifies valid data on data bus
Input Signifies cycle is a IO Write Cycle Input Input Signifies a read cycle if high or a write cycle if low NSBHE Input Byte High Enable Low value indicates valid data on the upper data byte Not Used Pull-down pin nMEMR Input External ROM Memory Read Signifies cycle is a ROM Memory Read Not Used Float pin BALE Input Input Address Strobe Falting edge latches address and nSBHE Not Used Pull-up pin IOCHRDY Output Optionally used to extend host cycles if wait states required Not Used Float pin IOCS16 Output IO Chip Select Not Used Float pin Output Active high Input Float pin INTR0 Output Interrupt 0 INT Interrupt upt ied to IPL0, IPL1 or IPL2 INTR1 Output Interrupt 1 Not Used Float pin Output Single line interrupt Output Data Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated. INTR3 Output Interrupt 3 nDTACK/1 Output Data Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated.	nIOWR	IO Space Write	R/nW	Read / Write
nSBHE InputByte High Enable Low value indicates valid data on the upper data byteNot UsedPull-down pin nMEMR InputExternal ROM Memory Read Signifies cycle is a ROM Memory ReadNot UsedFloat pin BALE InputInput Address Strobe Faling edge latches address and nSBHENot UsedPull-up pin IOCHRDY Output IO Channel Ready OutputNot UsedFloat pin IOCS16 Output IO Chip Select ot the value in the Base Address RegisterNot UsedFloat pin RESET Input Chip Reset Active highNot UsedFloat pin INTR0 OutputInterrupt 0 Single line interruptINT OutputInterruptINTR2 OutputInterrupt 2 Single line interruptNot UsedFloat pinINTR2 OutputInterrupt 3 Single line interruptNot UsedFloat pinINTR3 OutputInterrupt 3 Single line interruptNot UsedData Transfer Acknowledge Indicates data transfer complete. If processor is writing, bus cycle is terminated.INTR3 OutputInterrupt 3 Single line interruptNDTACK/1 OutputData Transfer Acknowledge Indicates data transfer complete. If processor is writing, bus cycle is terminated.	Input	Signifies cycle is a IO Write Cycle	Input	Signifies a read cycle if high or a write cycle if low
Input Low value indicates valid data on the upper data byte Not Used Float pin nMEMR Input External ROM Memory Read Not Used Float pin BALE Input Input Address Strobe Falling edge latches address and nSBHE Not Used Pull-up pin IOC HRDY Output IO Channel Ready Optionally used to extend host cycles if wait states required Not Used Float pin IOCS16 Output IO Chip Select Not use address Register Not Used Float pin RESET Chip Reset Active high Not Used Float pin INTR0 Interrupt 0 INT Interrupt Unencoded interrupt tied to IPL0, IPL1 or IPL2 INTR1 Interrupt 1 Not Used Float pin Output Single line interrupt Output Output INTR2 Interrupt 2 Not Used Float pin INTR3 Output Interrupt 3 Not Used Float pin INTR3 Output Interrupt 3 nDTACK/I Data Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated.	nSBHE	Byte High Enable	Not Used	Pull-down pin
nMEMR InputExternal ROM Memory Read Signifies cycle is a ROM Memory ReadNot UsedFloat pinBALE InputInput Address Strobe Faling edge latches address and nSBHENot UsedPull-up pinIOC HRDY OutputIO Channel Ready Optionally used to extend host cycles if wait states requiredNot UsedFloat pinIOCS16 OutputIO Chip Select Asserted when A[15:4] decoded to the value in the Base Address RegisterNot UsedFloat pinRESET InputChip Reset Active highRESET InputChip Reset Active lowResetINTR0 OutputInterrupt 0 Single line interruptINT OutputInterrupt 1 OutputNot UsedINTR1 OutputInterrupt 2 Single line interruptNot UsedFloat pinINTR2 OutputInterrupt 3 Single line interruptNot UsedFloat pinINTR3 OutputInterrupt 3 Single line interruptNot UsedFloat pinINTR3 OutputInterrupt 3 Single line interruptNot UsedInterasfer complete. Indicates data transfer complete. If processor is reading data is latched. If processor is reading	Input	Low value indicates valid data on the upper data byte		
Input Read Signifies cycle is a ROM Memory Read Not Used Pull-up pin BALE Input Falling edge latches address and nSBHE Not Used Pull-up pin IOC HRDY Output IO Channel Ready Optionally used to extend host cycles if wait states required Not Used Float pin IOCS16 Output IO Chip Select Asserted when A[15:4] decoded to the value in the Base Address Register Not Used Float pin RESET Chip Reset Input Active high Input Active low INTR0 Interrupt 0 INT Interrupt Unencode interrupt tied to IPL0, IPL1 or IPL2 INTR1 Interrupt 1 Not Used Float pin Output Single line interrupt Not Used Float pin INTR2 Interrupt 0 INT Interrupt tied to IPL0, IPL1 or IPL2 INTR1 Interrupt 2 Not Used Float pin Output Single line interrupt Output Data Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated. INTR3 Interrupt 3 NDTACK/1 Data Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is reading data is latched. If processor is writing, bus cycle is termina	nMEMR	External ROM Memory Read	Not Used	Float pin
BALE InputInput Address Strobe Falling edge latches address and nSBHENot UsedPull-up pinIOC HRDY OutputIO Channel Ready Optionally used to extend host cycles if wait states requiredNot UsedFloat pinnIOCS16 OutputIO Chip Select Asserted when A[15:4] decoded to the value in the Base Address RegisterNot UsedFloat pinRESET InputChip Reset Active highRESET InputChip Reset Active lowChip Reset Interrupt 0INTR0 OutputInterrupt 0 Single line interruptINT OutputInterrupt do Single line interruptINT Interrupt 0INTR1 OutputInterrupt 1 Single line interruptNot Used Interrupt 2Data Transfer Acknowledge Indicates data transfer complete. If processor is reading data is Iatched. If processor is writing, bus cycle	Input	Signifies cycle is a ROM Memory Read		
Input Falling edge latches address and nSBHE Not Used Float pin IOC HRDY IO Channel Ready Not Used Float pin Output Optionally used to extend host cycles if wait states required Not Used Float pin nIOCS16 IO Chip Select Not Used Float pin Output Asserted when A[15:4] decoded to the value in the Base Address Register Not Used Float pin RESET Chip Reset RESET Chip Reset Active low INTR0 Interrupt 0 INT Interrupt Un encoded interrupt tied to IPL0, IPL1 or IPL2 INTR1 Interrupt 1 Not Used Float pin Output Single line interrupt Not Used Float pin INTR2 Interrupt 2 Not Used Float pin Output Single line interrupt Output Data Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated. Output Single line interrupt Output Data Transfer Acknowledge Indicates data transfer complete	BALE	Input Address Strobe	Not Used	Pull-up pin
IOC HRDY OutputIO Channel Ready Optionally used to extend host cycles if wait states requiredNot UsedFloat pinnIOCS16 OutputIO Chip Select Asserted when A[15:4] decoded to the value in the Base Address RegisterNot UsedFloat pinRESET Input OutputChip Reset Active highRESET Input Active highRESET Input OutputChip Reset Interrupt 0RESET Interrupt OutputChip Reset Interrupt OutputINTR0 OutputInterrupt 0 Single line interruptINT OutputInterrupt Unencoded interrupt tied to IPL0, IPL1 or IPL2INTR1 OutputInterrupt 1 Single line interruptNot UsedFloat pinINTR2 OutputInterrupt 2 Single line interruptNot UsedData Transfer Acknowledge Indicates data transfer complete. If processor is writing, bus cycle is terminated.INTR3 OutputInterrupt 3 Single line interruptnDTACK/1 OutputData Transfer Acknowledge Indicates data transfer complete. If processor is writing, bus cycle is terminated.	Input	Falling edge latches address and nSBHE		
OutputOptionally used to extend host cycles if wait states requiredNot UsednIOCS16 OutputIO Chip Select Asserted when A[15:4] decoded to the value in the Base Address RegisterNot UsedFloat pinRESET Input OutputChip Reset Active highRESET Input Active highChip Reset Input OutputChip Reset Interrupt 0INTR0 OutputInterrupt 0 Single line interruptINT OutputInterrupt Unencoded interrupt tied to IPL0, IPL1 or IPL2INTR1 OutputInterrupt 1 Single line interruptNot UsedFloat pinINTR2 OutputInterrupt 2 Single line interruptNot UsedData Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated.INTR3 OutputInterrupt 3 Single line interruptnDTACK/1 OutputData Transfer Acknowledge Indicates data transfer complete. If processor is writing, bus cycle is terminated.	IOCHRDY	IO Channel Ready	Not Used	Float pin
NIOCS16 OutputIÓ Chip Select Asserted when A[15:4] decoded to the value in the Base Address RegisterNot UsedFloat pinRESET InputChip Reset Active highRESET InputChip Reset Active lowINTR0 OutputInterrupt 0 Single line interruptINT OutputInterrupt Unencoded interrupt tied to IPL0, IPL1 or IPL2INTR1 OutputInterrupt 1 Single line interruptNot UsedFloat pinINTR2 OutputInterrupt 2 Single line interruptNot UsedData Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated.INTR3 OutputInterrupt 3 Single line interruptnDTACK/1 OutputData Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated.	Output	Optionally used to extend host cycles if wait states required		
Output Asserted when A[15:4] decoded to the value in the Base Address Register Reset Chip Reset Reset Input Active high Input Active low Input Active low INTR0 Interrupt 0 INT Interrupt Output Single line interrupt Output Interrupt 1 Output INTR1 Interrupt 1 Not Used Float pin Output Single line interrupt Not Used Data Transfer Acknowledge INTR2 Interrupt 2 NDTACK/0 Data Transfer Acknowledge Output Single line interrupt Output Data Transfer Acknowledge INTR3 Interrupt 3 NDTACK/1 Data Transfer Acknowledge Indicates data transfer complete. If processor is writing, bus cycle is terminated. INTR3 Interrupt 3 NDTACK/1 Data Transfer Acknowledge Indicates data transfer complete. If processor is writing, bus cycle is terminated. Interrupt Output Single line interrupt Output	nIOCS16	IÓ Chip Select	Not Used	Float pin
to the value in the Base Address RegisterRESET InputChip Reset Active highRESET InputChip Reset Active lowINTR0 OutputInterrupt 0 Single line interruptINT OutputInterrupt Unencoded interrupt tied to IPL0, IPL1 or IPL2INTR1 OutputInterrupt 1 Single line interruptNot UsedFloat pinINTR2 OutputInterrupt 2 Single line interruptnDTACK/0 OutputData Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated.INTR3 OutputInterrupt 3 Single line interruptnDTACK/1 OutputData Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated.INTR3 OutputInterrupt 3 Single line interruptnDTACK/1 OutputData Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated.	Output	Asserted when A[15:4] decoded		
RegisterRESET InputChip Reset Active highRESET InputChip Reset Active lowINTR0 OutputInterrupt 0 Single line interruptINT OutputInterrupt OutputINT OutputINTR1 OutputInterrupt 1 Single line interruptNot UsedFloat pinINTR2 OutputInterrupt 2 Single line interruptNot UsedData Transfer Acknowledge Indicates data transfer complete. If processor is reading data is Iatched. If processor is writing, bus cycle is terminated.INTR3 OutputInterrupt 3 Single line interruptnDTACK/1 OutputData Transfer Acknowledge Indicates data transfer complete. If processor is reading data is Iatched. If processor is writing, Indicates data transfer complete. If processor is reading data is Iatched. If processor is writing, Indicates data transfer complete. If processor is reading data is Iatched. If processor is writing, Indicates data transfer complete.		to the value in the Base Address		
RESET InputChip Reset Active highRESET InputChip Reset Active lowINTR0 OutputInterrupt 0 Single line interruptINT OutputInterrupt Unencoded interrupt tied to IPL0, IPL1 or IPL2INTR1 OutputInterrupt 1 Single line interruptNot UsedFloat pinINTR2 OutputInterrupt 2 Single line interruptNDTACK/0 OutputData Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated.INTR3 OutputInterrupt 3 Single line interruptNDTACK/1 OutputData Transfer Acknowledge Indicates data transfer complete. If processor is writing, bus cycle is terminated.INTR3 OutputInterrupt 3 Single line interruptNDTACK/1 OutputData Transfer Acknowledge Indicates data transfer complete. If processor is writing, bus cycle is terminated.INTR3 OutputInterrupt 3 Single line interruptNDTACK/1 OutputData Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is reading data is latched. If processor is writing, bus cycle is terminated		Register		
InputActive highInputActive lowINTR0Interrupt 0INTInterruptOutputSingle line interruptOutputUn encoded interrupt tied to IPL0, IPL1 or IPL2INTR1Interrupt 1Not UsedFloat pinOutputSingle line interruptNot UsedInterrust from singleINTR2Interrupt 2NDTACK/0Data Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated.INTR3Interrupt 3NDTACK/1Data Transfer Acknowledge Indicates data transfer complete. If processor is writing, bus cycle is terminated.INTR3Interrupt 3NDTACK/1 OutputData Transfer Acknowledge Indicates data transfer complete. If processor is writing, bus cycle is terminated.	RESET	Chip Reset	RESET	Chip Reset
INTR0 OutputInterrupt 0INT Single line interruptInterrupt OutputUnencoded interrupt tied to IPL0, IPL1 or IPL2INTR1 OutputInterrupt 1Not UsedFloat pinINTR2 OutputInterrupt 2NDTACK/0 Single line interruptData Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated.INTR3 OutputInterrupt 3 Single line interruptNDTACK/1 OutputData Transfer Acknowledge Indicates data transfer complete. If processor is writing, bus cycle is terminated.	Input	Active high	Input	Active low
OutputSingle line interruptOutputUnencoded interrupt tied to IPL0, IPL1 or IPL2INTR1 OutputInterrupt 1 Single line interruptNot UsedFloat pinINTR2 OutputInterrupt 2 Single line interruptnDTACK/0 OutputData Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated.INTR3 OutputInterrupt 3 Single line interruptnDTACK/1 OutputData Transfer Acknowledge Indicates data transfer complete. If processor is writing, bus cycle is terminated.INTR3 OutputInterrupt 3 Single line interruptnDTACK/1 OutputData Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated.	INTR0	Interrupt 0	INT	Interrupt
INTR1 Interrupt 1 Not Used Float pin Output Single line interrupt NDTACK/0 Data Transfer Acknowledge INTR2 Interrupt 2 NDTACK/0 Data Transfer Acknowledge Output Single line interrupt Output Data Transfer Acknowledge INTR3 Interrupt 3 Output NDTACK/1 Data Transfer Acknowledge INTR3 Interrupt 3 NDTACK/1 Data Transfer Acknowledge Indicates data transfer complete. If processor is writing, bus cycle is terminated. INTR3 Interrupt 3 NDTACK/1 Data Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is reading data is latched. If processor is writing, bus cycle is terminated.	Output	Single line interrupt	Output	Unencoded interrupt tied to IPL0,
INTR1 Interrupt 1 Not Used Float pin Output Single line interrupt nDTACK/0 Data Transfer Acknowledge INTR2 Interrupt 2 Output Data Transfer Acknowledge Output Single line interrupt Output Data Transfer Acknowledge INTR3 Interrupt 3 Output Output NTR3 Interrupt 3 Single line interrupt Output INTR3 Single line interrupt Output Data Transfer Acknowledge Indicates data transfer complete. If processor is writing, bus cycle is terminated. INTR3 Interrupt 3 Single line interrupt Output Single line interrupt Output Data Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. Indicates data transfer complete. If processor is reading data is latched. Is processor is writing, bus cycle is terminated. Indicates data transfer complete.				IPL1 or IPL2
Output Single line interrupt INTR2 Output Interrupt 2 Single line interrupt nDTACK/0 Output Data Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated. Interrupt 3 Single line interrupt nDTACK/1 Output Data Transfer Acknowledge INTR3 Output Interrupt 3 Single line interrupt nDTACK/1 Output Data Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated Data Transfer Acknowledge	INTR1	Interrupt 1	Not Used	Float pin
INTR2 Output Interrupt 2 Single line interrupt nDTACK/0 Output Data Transfer Acknowledge NTR3 Output Single line interrupt 3 Output Interrupt 3 Interrupt 3 NDTACK/1 Output Data Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated. INTR3 Output Interrupt 3 NDTACK/1 Single line interrupt Data Transfer Acknowledge Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated. Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated	Output	Single line interrupt		
Output Single line interrupt Output Indicates data transfer complete. Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated. INTR3 Interrupt 3 nDTACK/1 Data Transfer Acknowledge Output Single line interrupt Output Indicates data transfer complete. Is processor is reading data is latched. Indicates data transfer Acknowledge Indicates data transfer complete. Output Single line interrupt Output Indicates data transfer complete.	INTR2	Interrupt 2	nDTACK/0	Data Transfer Acknowledge
INTR3 Interrupt 3 nDTACK/1 Data Transfer Acknowledge Output Single line interrupt Output Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated. Data Transfer Acknowledge Indicates data transfer complete. Indicates data transfer complete. If processor is writing, bus cycle is terminated. Indicates data transfer complete.	Output	Single line interrupt	Output	Indicates data transfer complete.
INTR3 Interrupt 3 nDTACK/1 Data Transfer Acknowledge Output Single line interrupt Output Indicates data transfer complete. If processor is writing, bus cycle is terminated. Indicates data transfer complete. If processor is writing, bus cycle is terminated.				IT processor is reading data is
INTR3 Interrupt 3 nDTACK/1 Data Transfer Acknowledge Output Single line interrupt Output Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated. Indicates data transfer complete.				hus evelo is terminated
Output Single line interrupt Output Dirack/1 Data Transfer Acknowledge Output Single line interrupt Output Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated		Interrupt 2		Dus cycle is terminated.
If processor is reading data is latched. If processor is writing,	Output	Single line interrupt		Indicatos data transfer complete
latched. If processor is writing,	Juipui		Juput	If processor is reading data is
bus even is tormated				latched If processor is writing
				bus cycle is terminated.

Table 2.1 Bus Interface Signal Cross Reference



It is important to note that all other LAN91C96 signals retain the same function in all bus modes. Some of these signals can effect operation of the controller in Motorola 68000 bus mode and must be correctly wired. Table 2 details signals that have uses in ISA bus mode, but will negatively impact operation when configured for the Motorola 68000 bus mode.

SIGNAL	ISA BUS MODE USE	WIRING FOR MOTOROLA 68000 BUS MODE
nEN16 Input	When low, the LAN91C96 is performs 16-bit operations. When high, the LAN91C96 is performs for 8-bit operations.	Provide 10K Pull-down
nROM Input / Output	If this pin is sampled low at the end of RESET the bus interface is configured in PCMCIA mode. In ISA mode, the pin is used as a ROM chip select output.	Float pin
nDTACK/0 and nDTACK/1 Output	These pins represent interrupts. When not selected through the INTSEL0 and INTSEL1 bits these pins are tri-stated.	Provide 10K pull-ups

Table 2.2 Noteworthy Controller Signals In Motorola 68000 Bus Mode

2.3 MOTOROLA 68000 BUS MODE ENTRY / EXIT SEQUENCE

Entering Motorola 68000 bus mode requires a specific sequence. Once entered, only a hard reset will take the part out of Motorola 68000 bus mode.

2.3.1 Bus Mode Entry

- 1. **Power device up in ISA 16-Bit Bus Mode**. To configure the LAN91C96 up in ISA 16-Bit Bus Mode, nEN16 must be low and nROM must float when samples at the end of reset (RESET signal's falling edge). Table 2 details the pin configuration necessary to accomplish this.
- 2. **Assert nIORD and nIOWR simultaneously**. After reset, assert nIORD and nIOWR (both driven low) simultaneously to configure the device in Motorola 68000 Bus Mode. Executing a Motorola 68000 bus write sequence is an easy way to accomplish this.
- 3. Write to the LAN91C96 using a Motorola 68000 bus write cycle. The first access to the device after assertion of nIORD and nIOWR must be a Motorola 68000 write cycle. This allows the device to verify the bus mode. Executing a second Motorola 68000 bus write sequence will accomplish this.

2.3.2 Bus Mode Exit

1. Assert RESET. Pulling RESET low will reset the device and allow reconfiguration of the bus operating mode.



2.4 MOTOROLA 68000 BUS MODE SOFTWARE CONSIDERATIONS

When configured in Motorola 68000 bus mode, use of the device is the same as in ISA mode, that is all features of the LAN91C96 remain active. Although the ability to access all registers remains, functions related to the system bus must be carefully handled. The following functions need to be considered whenever accessing the device:

PCMCIA Register Functions

The Ethernet Configuration Option Register (8000h) and Ethernet Configuration and Status Register (8002h) are reserved for PCMCIA functions. These registers should be left in the reset state and not changed when operating in Motorola 68000 bus mode.

16-Bit Data Accesses

The Configuration Register 16BIT bit (Bank 1, Offset 0, Bit 7) controls the data bus width. Out-of-reset this bit will reflect the inverted value on the nEN16 pin. When correctly configured for Motorola 68000 bus mode, the bit will read as a high, reflecting a pull-down on the nEN16 bit. This bit should only be written with a high value.

Wait States

The Configuration Register NOWAIT bit (Bank 1, Offset 0, Bit 12) controls whether or not the LAN91C96 will request ISA bus wait states. The default value of zero will negate the IOCHRDY signal for two or three 20MHz clocks on any cycle to the LAN91C96. Writing a one to this bit will prevent the LAN91C96 from requesting wait states. Because the IOCHRDY is not used in Motorola 68000 bus mode, this bit can be ignored.

Interrupts

The Configuration Register INTSEL1 and INTSEL0 bits (Bank 1, Offset 0, Bits 2 and 1) define which interrupt pin (INTR0, INTR1, INTR2 or INTR3) to use when requesting service. Because only INTR0 is used for Motorola 68000 bus mode, these bits should both be written to zero.

Little Endian / Bit Endian

The LAN91C96 does not swap the lower and upper bytes of the data bus when in Motorola 68000 bus mode. This means any access to the device must consider byte ordering. It is up to the application and hardware layout as to whether the bytes should or should not be swapped.

Boot ROM

The Base Address Register ROMSIZE bits (Bank 1, Offset 2, Bits 6 and 7) define the size of the external boot ROM and the address lines to use for decode. The nMEMR signal is also required when using an external boot ROM. Because the Motorola 68000 bus interface does not support I/O and Memory cycles, the ROMSIZE bits should always be programmed low to disable address decoding to an external ROM. Address lines A[19:16] will then be ignored and the chip select output nROM will remain high through the internal pull-up.



2.5 BUS CONFIGURATIONS WITH POPULAR M68000 PROCESSORS



other peripheral controls are independent of the bus interface.

Figure 2.2 - MC68000, MC68HC000, AND MC680 10 (16-BIT PROCESSORS)





Figure 2.3 MC68HC001 (8-/16 BIT PROCESSOR)





Figure 2.4 - MC68EC000 (8-/16-BIT PROCESSOR)



2.6 MOTOROLA 68000 BUS MODE ANOMALIES

2.6.1 nDTACK/0 and nDTACK/1 Do Not Acknowledge Data Transfers

2.6.2 Problem

nDTACK/0 and nDTACK/1 are specified as data transfer acknowledgment pins. These are output pins from the LAN91C96 that communicate the status of data on the data bus to the host Motorola 68000 processor. For read and write operations these signals are specified to have the following meaning:

2.6.3 Read Operation

During a read operation the LAN91C96 places valid data on the D[15:0] pins. When this data is valid, the LAN91C96 lowers the nDTACK/0 and nDTACK/1 pins to signify to the host processor that data is valid and read to be latched.

2.6.4 Write Operation

During a write operations, the LAN91C96 reads data into its registers. When the data on the data bus has been latched within the LAN91C96, nDTACK/0 and nDTACK/1 are lowered to signify to the host processor that the data has been read and the write cycle can be terminated.

2.6.5 Actual Behavior

All aspects of a read and write operation work except for the nDTACK/0 and nDTACK/1 response. These pins do not go low as expected and as a result the LAN91C96 can not feedback to the host processor that a data transfer has completed.

2.6.6 Solution

The LAN91C96 does not require wait states for read and write operations so the use of nDTACK/0 and nDTACK/1 is not required. These pins can be wired as specified and will not interfere with normal operation.