

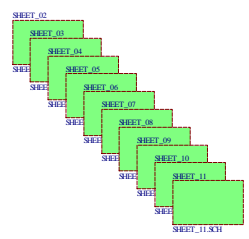
RDCLIENT

STPC CLIENT REFERENCE DESIGN

REV 1.3

SAA00022AAXX

SEPTEMBER 8th, 1999



BOARD DESCRIPTION:

- Motherboard in ATX format.
- STPC Client interfaces:
 - * Standard Spec VGA monitor output.
 - * 3 PCI slot.
 - * 3 ISA slots.
 - * Primary and Secondary EIDE.
 - * Video Input Port.
 - * Digital TV Output.
- Memory:
 - * 4 DRAM SMM Sockets.
- SUPER I/O:
 - * 1 Parallel port.
 - * 2 Serial ports.
 - * Keyboard/Mouse interface.
 - * 1 Floppy Disk interface.
- Other:
 - * NISCPAL Encoder.
 - * ATX Power supply.
 - * Reset and Power on switch.
 - * Speaker.

FILENAME	SHEET DESCRIPTION
RDCLIENT.SCH	COVER
SHEET_02.SCH	STPC CLIENT
SHEET_03.SCH	DRAM 0,1,2,3
SHEET_04.SCH	VGA, VIDEO INPUT PORT
SHEET_05.SCH	NTSC/PAL ENCODER
SHEET_06.SCH	ROM BIOS, CONFIGURATIONS STRAPS
SHEET_07.SCH	PCI SLOTS A, B, C
SHEET_08.SCH	3 ISA SLOTS + IRQ, DRQ, DACK MUX
SHEET_09.SCH	SIO, PARALLEL AND SERIAL PORT, KBD, MOUSE
SHEET_10.SCH	FLOPPY, EIDE CONNECTORS
SHEET_11.SCH	RESET, POWER SUPPLY AND SPEAKER

THE INFORMATION CONTAINED IN THESE SCHEMATIC SHEETS IS PRELIMINARY AND SUBJECT TO CHANGE WITHOUT NOTICE. STMicroelectronics BEARS NO RESPONSIBILITY FOR ANY ERRORS IN THESE SCHEMATIC SHEETS.

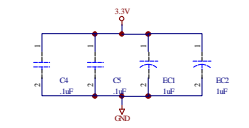
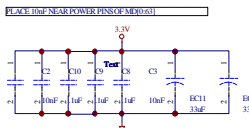
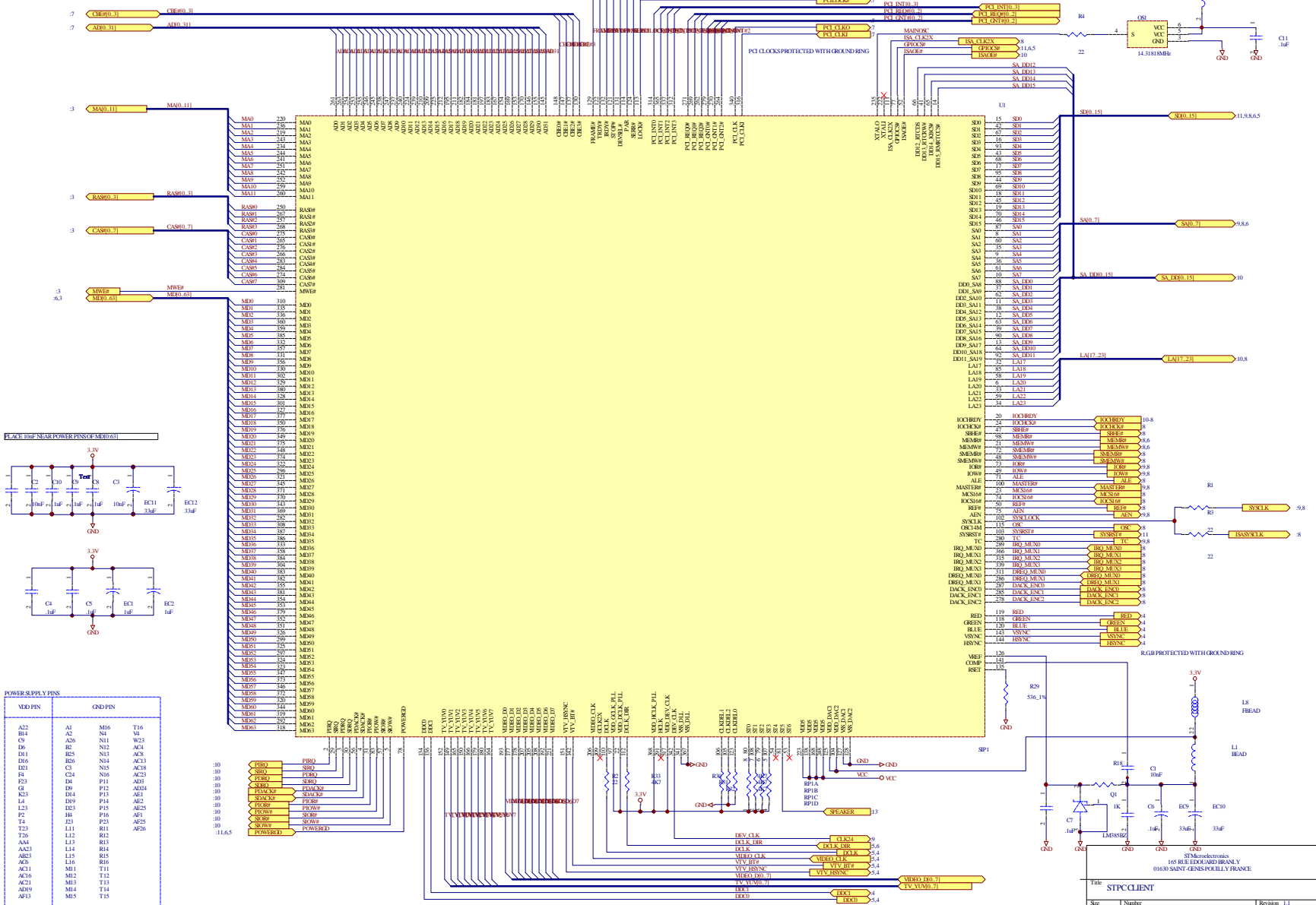
REVISION HISTORY	
REV 0.1:	Initial release
REV 1.0:	
REV 1.1:	07/22/1999
REV 1.2:	06/18/1999
REV 1.3:	09/08/1999

NOTES

* The text with no border are for misc and layout informations.
 Comments about the schematics are with dashed lines border.
 The Config straps is necessary to config the STPC during the reset.

STMicroelectronics 165 RUE EDUGARD BRANLY 91630 SAINT GENES POUALLY FRANCE			
Title: COVER			
Size	Number	Revision 1/0	
Orical C:			
Date: 14 Sep 1999	Sheet 1	of 11	
File: C:\A\REV02\STPC\REV1_0\PROJ01\RDCLIENT.SCH			

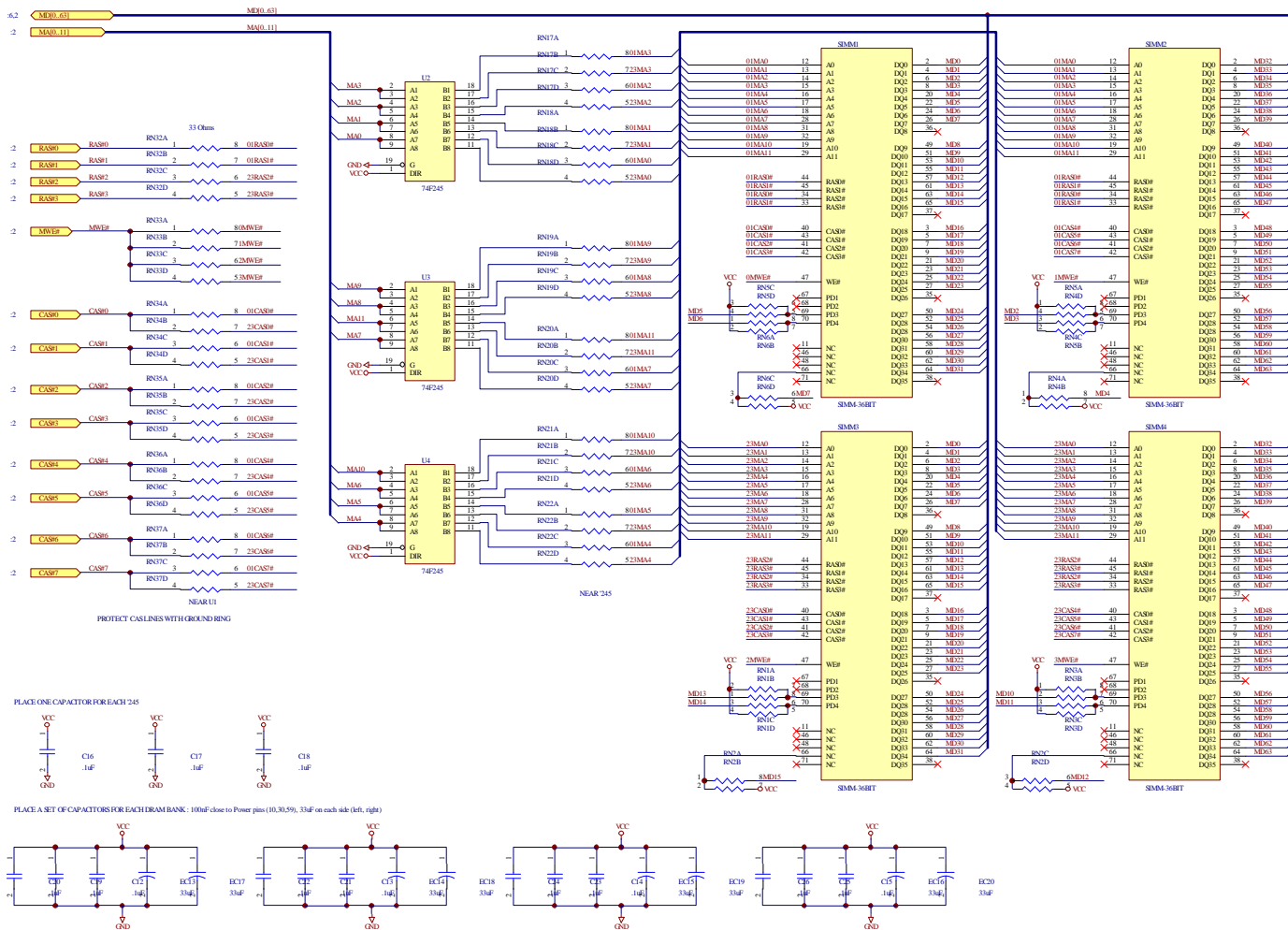
STPC Client



MID PIN	GND PIN
A22	A1
B14	A2
C9	A26
D6	B2
D11	B25
D16	B24
D21	C3
F4	C24
F23	D4
G1	D9
K23	H4
L4	D19
L23	D23
P2	H4
T4	J23
T23	L11
T26	L12
A04	L13
AA23	L14
AC3	L15
AC9	L16
AC11	M1
AC16	M2
AC21	M1
AD09	M4
AP13	M15
M16	T16
N6	W2
N2	AC8
N4	AC13
N15	AC18
N16	AC23
P11	AD3
P12	AD24
P13	AE1
P14	AE2
P15	AE3
P16	AF1
P17	AF2
R1	AF20
R2	
R3	
R4	
R5	
R6	
R7	
R8	
R9	
R10	
R11	
R12	
R13	
R14	
R15	
R16	
R17	
R18	
R19	
R20	
R21	
R22	
R23	
R24	
R25	
R26	
R27	
R28	
R29	
R30	
R31	
R32	
R33	
R34	
R35	
R36	
R37	
R38	
R39	
R40	
R41	
R42	
R43	
R44	
R45	
R46	
R47	
R48	
R49	
R50	
R51	
R52	
R53	
R54	
R55	
R56	
R57	
R58	
R59	
R60	
R61	
R62	
R63	
R64	
R65	
R66	
R67	
R68	
R69	
R70	
R71	
R72	
R73	
R74	
R75	
R76	
R77	
R78	
R79	
R80	
R81	
R82	
R83	
R84	
R85	
R86	
R87	
R88	
R89	
R90	
R91	
R92	
R93	
R94	
R95	
R96	
R97	
R98	
R99	
R100	

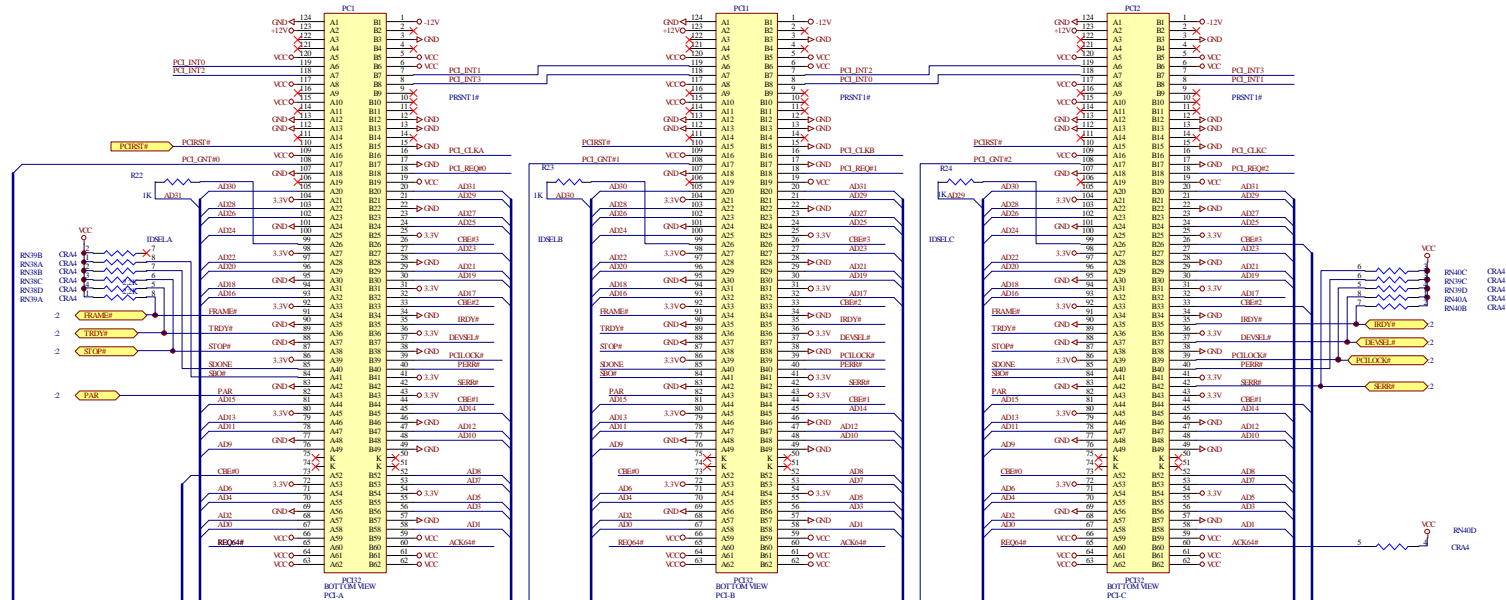
STPC CLIENT	
Size	Number
14-Sep-1999	Sheet 2 of 11
STMicroelectronics 165 RUE EDGAR BELLAIR 91060 SAINT-GENES-POUILLEY FRANCE	

DRAM 0,1,2,3

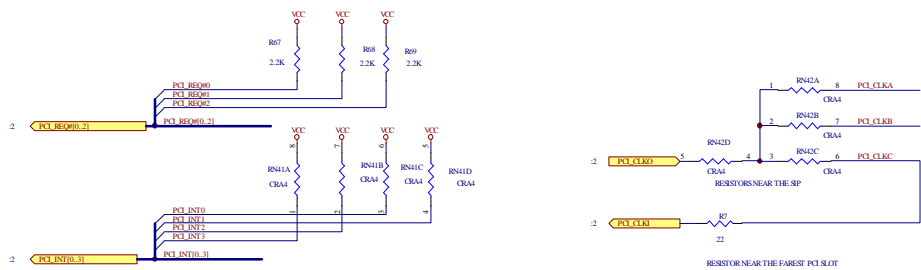


STMicroelectronics 165 RUE EDGARDE BRANLY 91630 SAINT GENES PULLY FRANCE	
Title: DRAM 0, 1, 2, 3	
Size: 0x0x0	Number: Revision: 1/0
Date: 14-Sep-1999	Sheet: 1 of 11
File: C:\A810\WP\1\MP\B\CL1\090113\DR01_03.XM	

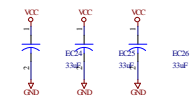
PCI SLOTS A, B, C



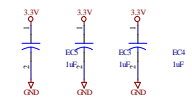
2 PCI_CNT#0_31 PCI_CNT#0_21



ONE CAPACITOR FOR EACH PCI SLOT



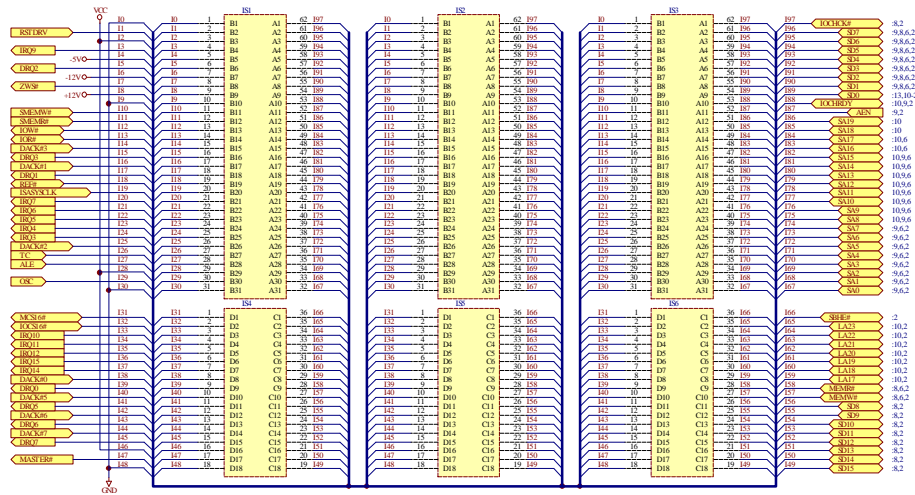
ONE CAPACITOR FOR EACH PCI SLOT



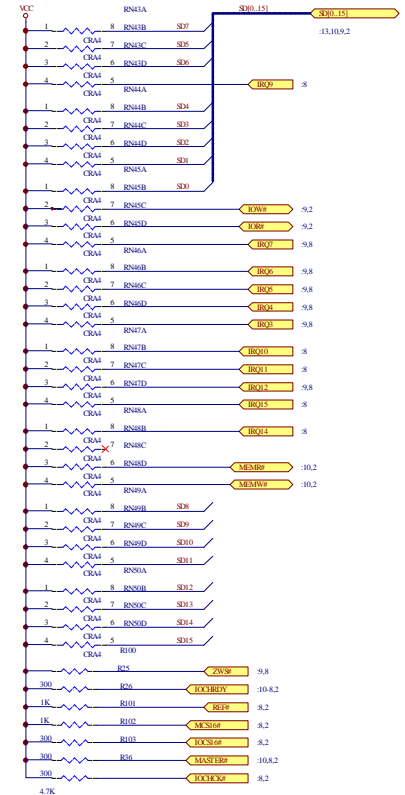
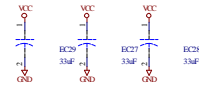
RESISTOR NEAR THE FAREST PCI SLOT

STMicroelectronics 165 RUE EDGARDE BRANLY 91630 SAINT GENES POUILLY FRANCE		
Title: PCI SLOTS A, B, C		
Size:	Number:	Revision: 2/0
Date: 14-Sep-1999	Sheet: 1	of: 11
File: C:\A\B\TOP\PC1\PC1_1\PC1_SLOT_A_B_C.DWG		

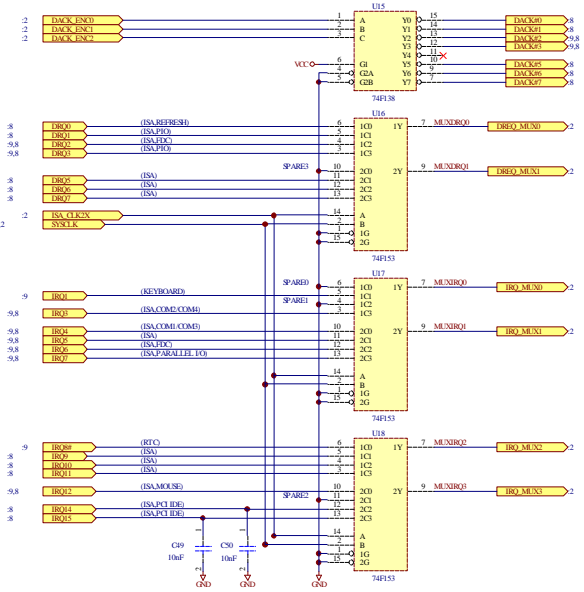
3 ISA SLOTS



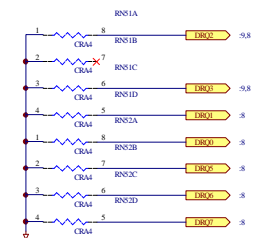
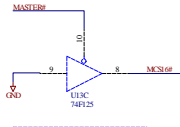
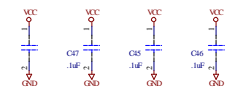
ONE CAPACITOR FOR EACH ISA SLOT



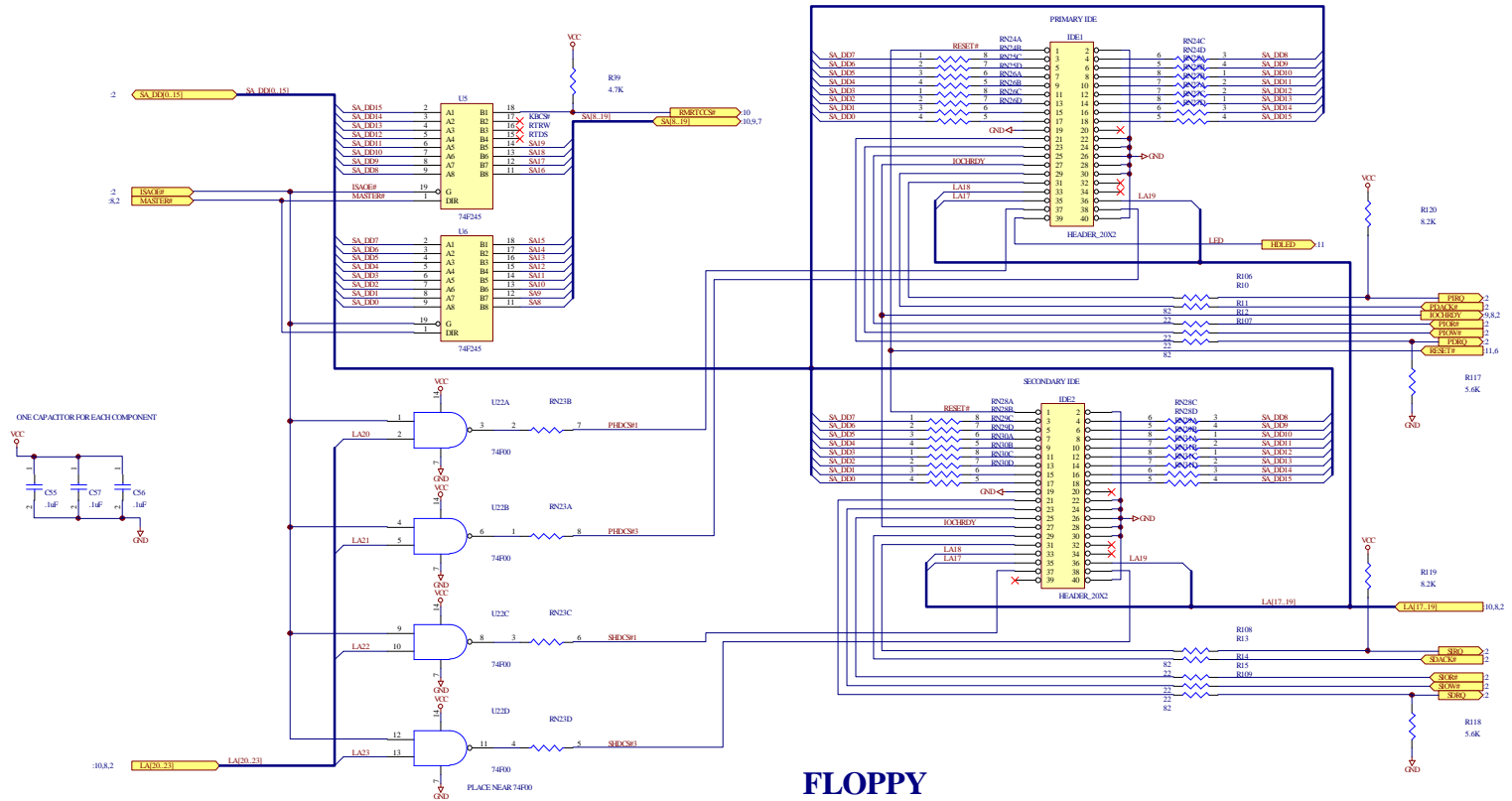
IRQ, DRQ, DACK MUX



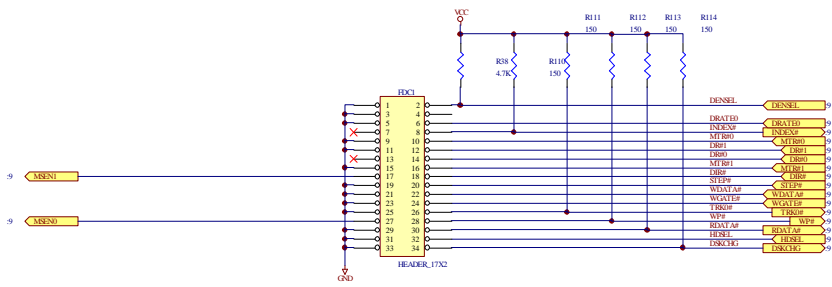
ONE CAPACITOR FOR EACH COMPONENT



EIDE CONNECTORS



FLOPPY



Media Sense and DRATE Options
 Determined by Floppy Drive Model
 and Preference of System Designer

STMicroelectronics 165 RUE EDGARDE BRANLY 91630 SAINT GENIS POUILLY FRANCE		
Title: FLOPPY, EIDE CONNECTORS		
Size:	Number:	Revision: 1/0
OrCAD:	Sheet 10 of 11	
Date: 14-Sep-1999	File: C:\A:\BENCH\1\MP\BENCH1\09011001\SUBE1.DOC	

