Signetics

AN12
Low Cost Programmer for PLD 20-Pin Series

Application Note

Application Specific Products

INTRODUCTION

The Low Cost Programmer (LCP) is designed to provide the user with a low cost alternative to program Signetics' PLD 20-pin series programmable logic devices. This system is a peripheral device which is to be controlled by a computer running Signetics software, AMAZE, or by a terminal. The LCP is connected to the host computer via the RS232 interface and will accept ASCII codes. The data transfer rate can be either 9600 or 4800 baud. The LCP system clock is 4800 baud. The basic measure of time in the system is in units of 13μs. After every fuse is programmed, the LCP will automatically perform a verification cycle and feed data back to the computer. The system can be set to TEST mode which causes the outputs to cycle through the fusing sequence in an endless loop.

THEORY OF OPERATION

A block diagram of the LCP is shown in Figure 1. U1 generates the 9600 baud clock for U3 (UART) and the 4800 baud clock for the rest of the system. When data is transferred into U3, it is put on the system bus. U1 generates IDAV which enables the rest of the system to react to the input. Since each device can decode the input instruction, very few controls are necessary.

Figure 2 shows the system instruction set. Each consists of seven bits with the upper 3 bits being the instruction code and the lower 4 bits being data or finer resolution of the instruction code. Figures 2 and 3 of Appendix 1 show the fuse address tables of PLS153 and PLS159, respectively. Note that the Variable Addresses have seven bits (3 upper bits and 4 lower bits), whereas the Term Addresses have six bits (2 upper bits and 4 lower bits). Therefore, it takes up to four nibbles to define a fuse address. Once an address is defined, the Variable Address generator will increment automatically to generate the subsequent fuse addresses for the same Term Address. Loading a Term Address in the Term Address generator will always reset the Variable Address generator. Therefore, the Term Address should be entered first and then the Variable Address. The last entry is the fusing data in a 4-bit nibble. The system will automatically increment the Variable Address generator to program four fuses. Once the 4-bit fusing data is loaded, the system goes into an internal mode until the fusing cycle for the four fuses are completed.

The following illustrates the sequence of programming operation:

1. Switch LCP to ON-LINE
2. Input 010 0000 – reset LCP
3. Input 010 0001 – put LCP "ON-LINE"

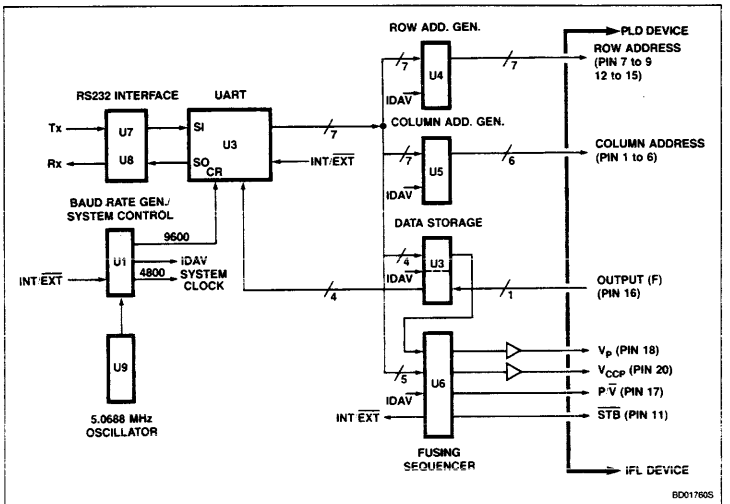

Figure 1. Block Diagram

C2 (D6)	C1 (D5)	C0 (D4)	D3	D2	D1	D0	FUNCTION
0	0	0	X	X	X	X	System internal use
0	0	1	X	X	X	X	System internal use
0	1	0	0	0	0	0	System reset
0	1	0	0	0	0	1	Set system ON-LINE
0	1	0	0	0	1	0	Set system OFF-LINE
0	1	1	4-bit data				Load fusing data
1	0	0	4-bit data				Load 4-bit lower TERM ADD.
1	0	1	2-bit data				Load 2-bit upper TERM ADD.
1	1	0	4-bit data				Load 4-bit upper VAR ADD.
1	1	1	3-bit data				Load 3-bit upper VAR ADD.

NOTE:
The upper and lower VARIABLE ADDRESSES will be reset to zero if upper or lower TERM ADDRESS is loaded into the LCP.

Figure 2. LCP Instruction Set

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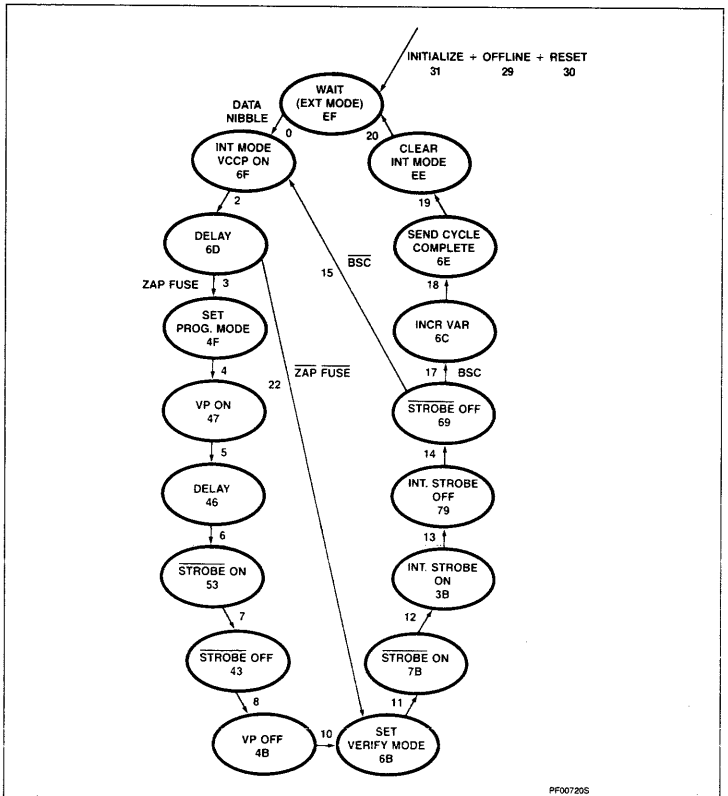
4. Input 100 — – load 4-bit lower TERM ADDRESS
5. Input 101 00– – load 2-bit upper TERM ADDRESS
6. Input 110— – load 4-bit lower VARIABLE ADDRESS
7. Input 111 0— – load 3-bit upper VARIABLE ADDRESS
8. Input 011— – load 4-bit fusing data, a "1" causes a fuse to be blown
9. U6, the fusing sequencer, causes the system to go into INTERN mode
10. Fusing sequence starts. See Figures 3 and 4
11. Fusing cycle completed. Input next address:
    a. If next TERM ADDRESS is different from the previous one, go to (4)
    b. If next address is in sequence with the previous VARIABLE ADDRESS and in the same TERM, go to (8)
    c. The Variable Address generator will always reset to 0 if TERM ADDRESS is loaded.

Figure 3 shows the sequence of fusing operation while the system is in internal mode. Figure 4 shows the timing diagram and voltage waveform of the fusing sequence of four consecutive fuses.

Analog Drivers:

V_P — This signal is current limited to 325mA. It is 1.25V to 1.75V when not fusing (idle). During the fusing cycle it takes on a value of 14.25V to 14.75V for a short time. The leading edge is slew rate limited to about 10μs.

V_{CCP} — This signal is the programming power supply. It can source up to 1A. It has a value of 1.1V to 1.3V when not fusing (idle).



NOTES:
1. State numbers in hex.
2. State changes on every clock.
3. 13μs cycle time.

Figure 3. State Diagram Fusing Sequence and Control PLD U6

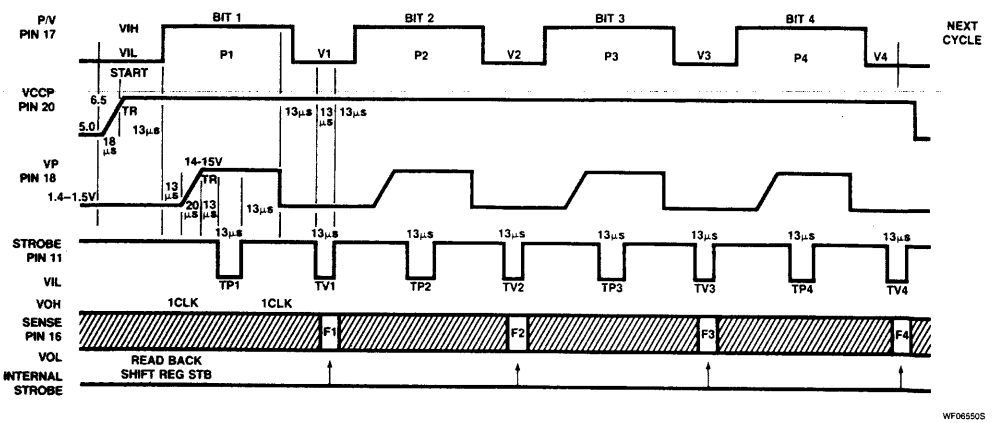


Figure 4. Timing Diagram and Voltage Waveforms

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During the fusing cycle it assumes a value of 8.25V to 8.75V for the duration of the entire cycle (four fusing pulses – See Figure 4).

V_P Driver Circuitry — The V_P signal is toggled by the Fusing Sequencer, U6, Pin 15. This TTL signal is buffered up by the switching transistor, Q3, and its associated resistors, R6 and R9. Transistor Q4 inverts the signal to achieve the correct phase relationship. It also performs the following circuit functions:

1. It clamps the base of the Darlington transistor, Q5, to near ground through the R10 resistor.
2. Transistor Q4 discharges the slew rate time constant capacitor, C1, through the resistor, R10, and shunts the current from the current source, VR2, to near ground. This prepares the circuit for the next controlled slew rate edge at the beginning of the next fuse blowing cycle.
3. It provides a current sinking path to pull current out of the fusing socket enable line, thus creating a rapidly falling V_{CCP} trailing edge. The diode, D2, provides sourcing isolation while the resistor, R11, limits inrush currents. A ferrite bead on the R11 lead slows down this path. This prevents large currents from flowing through transistor Q4 at the low level switching transition time.

The voltage regulator, VR1, forms the 325mA current limit circuit in conjunction with the voltage dropping resistor, R8.

The controlled slew rate of the leading edge and the final level of the enable high output voltage V_P are generated in the following manner:

1. A 10mA current source is formed by the voltage regulator, VR2, and the dropping resistor, R7.
2. This current is shunted to ground through Q4 when the enable pulse is low.
3. At the instant when Q4 turns off, the 10mA current is diverted into the slew rate control capacitor, C1. The capacitor, C1, will continue to charge linearly until the voltage across it reaches the value of the zener diode stack D1A and D1B.
4. The current is then shunted down the zener diodes until Q4 is turned back on.
5. The base of the Darlington transistor, Q5, follows the voltage across the capacitor, C1, and draws very little current due to its very high current gain. Since the Q5 transistor is configured as an emitter follower, the voltage seen on the fusing socket enable line will be about 1V lower than the base of transistor Q5. Resistor R12 stabilizes the value of the V_{BE} on transistor Q5 by pulling a small amount of current early in the ramp.

V_{CCP} Driver Circuitry — V_{CCP} is toggled by the internal/external signal from the Fusing Sequencer, U6. Again, the signal is buffered and inverted twice by transistors Q1 and Q2 along with resistors R4 and R3.

Low Voltage (Idle)
Resistor R2 is shorted to ground through transistor Q2 in order to generate the 1.1V to 1.3V low output level. This is an intrinsic value generated by the internal reference of the voltage regulator.

High Voltage (V_{CCP})
When transistor Q2 is turned off, the output voltage ramps to the 8.25V to 8.75V level. This value is determined by the ratio of resistors R1 and R2 in conjunction with the actual value of the voltage regulator's internal reference.

Power Supply Consideration

1. The Low Cost Programmer circuitry draws about 1A.
2. The Enable and V_{CCP} currents may reach about 1.4A.
3. The Enable signal is about 15V and needs at least 5V of head room.
4. The RS232 drivers require ± 12V at about 60mA.

In a bridge circuit, a rule of thumb says that the transformer's current rating should be from 1.2 to 1.6 times the load current. Using this rule, the secondary of the transformer that supplies V_{CC} and ± 12V should be rated at 18V center tapped at about 1.6A.

The transformer that supplies the Enable and V_{CCP} circuits should have an 18V secondary at about 2.2A.

PROGRAMMING THE LCP

The addresses and fusing data can be generated by the host computer using AMAZE or a terminal nibble by nibble. The fuse address of each PLD 20-pin device is available in the Signetics PLD data manual. Copies of the fuse address tables of PLS153 and PLS159 are included in Appendix A Tables A-1 and A-2. These fuse addresses, together with the 3-bit instruction code, form a 7-bit instruction which can be represented by a single ASCII character. Table 1 is a table of ASCII characters.

The following example illustrates the conversion of program table entries into fuse addresses and fusing data. Table 2 shows a simple entry in an PLS153 program table. To keep things simple, only four entries are made. The first entry is term 3, variable I7. The fuse of the non-inverting buffer is to remain intact, whereas the fuse to be blown is the inverting buffer, I7. For this entry, from Table A-1 of Appendix A, the Term Address is 03hex or 00 0011b, the Variable Addresses of the two buffers are 0Ehex or 000 1110b, and 0Fhex or 000 1111. The fusing data is 01. The second entry is Term 3, I6. The fuse of the inverting buffer is to be kept intact while that of the non-inverting buffer will be blown. The Term Address is the same as the previ-

Table 1. ASCII Character Table

		0000	0001	0010	0011	0100	0101	0110	0111
		0	1	2	3	4	5	6	7
0000	0	NUL	DLE	SP	0	•	P	·	p
0001	1	SOH	DC1	!	1	A	Q	a	q
0010	2	STX	DC2	"	2	B	R	b	r
0011	3	ETX	DC3	#	3	C	S	c	s
0100	4	EOT	DC4	$	4	D	T	d	t
0101	5	ENQ	NAK	%	5	E	U	e	u
0110	6	ACK	SYN	&	6	F	V	f	v
0111	7	BEL	ETB	'	7	G	W	g	w
1000	8	BS	CAN	(	8	H	X	h	x
1001	9	HT	EM	)	9	I	Y	i	y
1010	A	LF	SUB	*	:	J	Z	j	z
1011	B	VT	ESC	+	;	K	[	k	{
1100	C	FF	FS	,	<	L	^	l	:
1101	D	CR	GS	—	=	M	]	m	}
1110	E	SO	RS	.	>	N		n	~
1111	F	SI	US	/	?	O	÷	o	DEL

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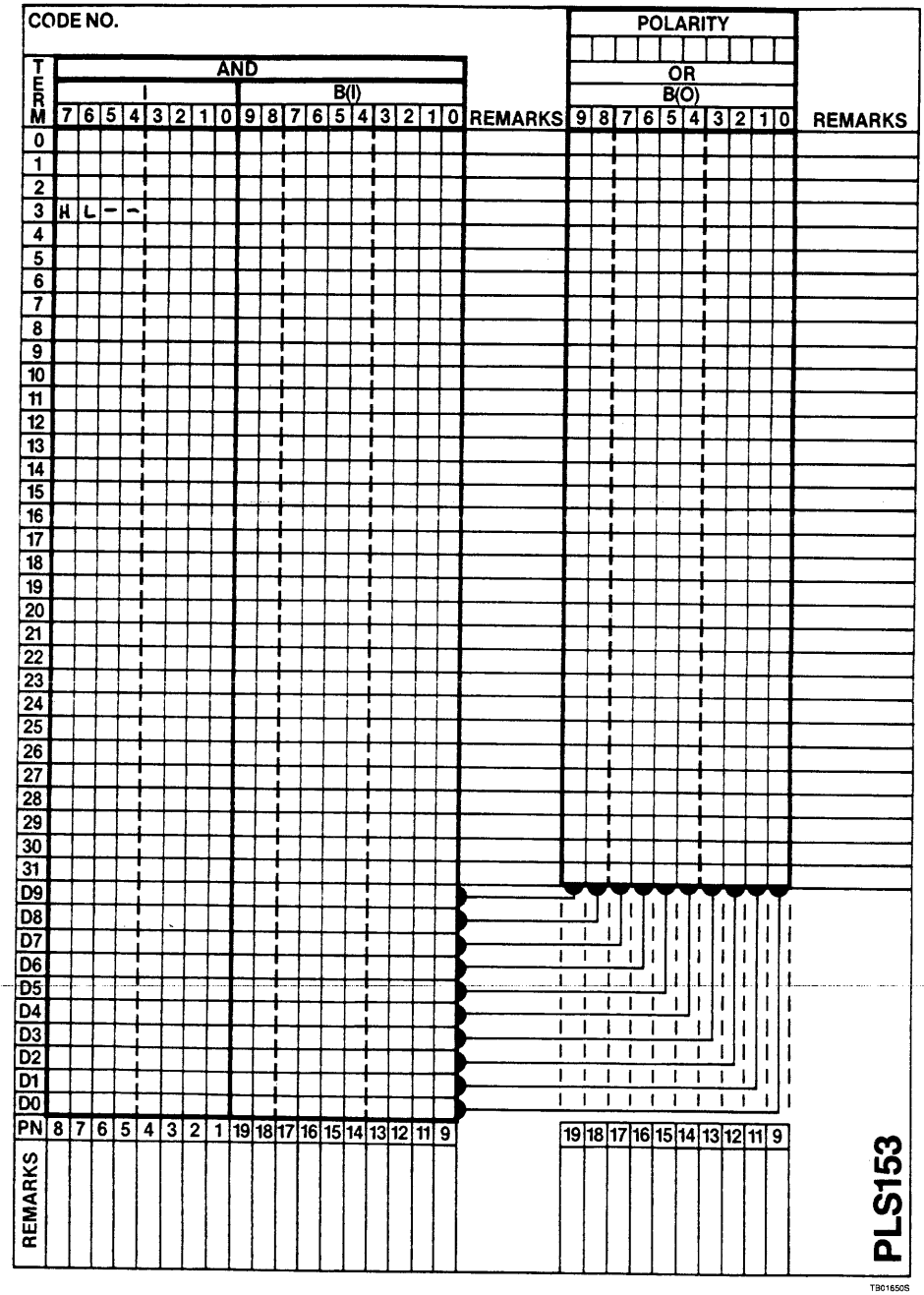
Table 2. FPLA Program Table



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ous entry; the Variable Addresses of the two buffers are 0Chex or 000 1100b and 0Dhex or 000 1101b. The fusing data is 10. The four fusing data can be combined into one nibble (0110) since the two entries are in sequence. Only the first address has to be loaded (Term Address 03hex and Variable Address 0F). The next two entries are in sequence with the first two, therefore only fusing data nibble 1111 has to be loaded.

The instruction and data nibbles can be loaded into the LCP in ASCII characters (see Table 1).

LCP CHECK OUT AND CALIBRATION

This section deals with the check out and calibration of the Low Cost Programmer.

The voltage regulator, VR4, dissipates a lot of heat. It should be mounted on a metal chassis with an isolation mount.

Notice that the fusing socket, P1, has three columns of pads. Use the left set if the socket is to be mounted on the component side of the PCB. Use the right set if the socket is to be placed on the blank side of the PCB. The LEDs may also be mounted on the blank side, allowing for very easy panel mounting of the finished LCP.

Power Supplies

1. $+10V_{DC}$ to $+14V_{DC}$ at the positive side of C4.
2. $-10V_{DC}$ to $-14V_{DC}$ at the negative side of C3.
3. $+4.75V_{DC}$ to $+5.25V_{DC}$ at the $+5V_{DC}$ input pad of the PCB.
4. $+20V_{DC}$ to $+26V_{DC}$ at the positive side of C2.

Turn off the LCP and insert ICs U1 through U5, U7 and U8. Do not insert U6 yet.

Turn on the LCP and repeat steps 1 through 4 above.

Driver Calibration

The Fusing Sequencer, U6, must not be in the LCP for the following steps:

Measure $1.25V_{DC}$ to $1.75V_{DC}$ at Pin 18 of P1. (The fusing socket.)

2. Place a clip lead from the U6 Pin 15 end of resistor R6 to V_{CC} ($+5V_{DC}$).
3. Measure $14.0V_{DC}$ to $15.0V_{DC}$ at Pin 18 of P1.
4. Momentarily place a 75Ω 3W resistor from Pin 18 of P1 to ground and observe the voltage to still read $14.0V_{DC}$ to $15.0V_{DC}$.
5. Disconnect the clip lead between R6 and V_{CC}.
6. Measure the voltage at Pin 18 of P1 to once again be 1.25 to $1.75V_{DC}$.
7. Place a jumper from the U6 Pin 19 side of resistor R4 to ground.
8. Measure the voltage at Pin 20 of P1. It should be $1.10V_{DC}$ to $1.30V_{DC}$.
9. Place a jumper from the U6 Pin 19 side of resistor R4 to V_{CC}.
10. The voltage should be from $8.25V_{DC}$ to $8.75V_{DC}$ at Pin 20 of P1.
11. Place a 30Ω 3W load resistor momentarily from Pin 20 of P1 to ground and measure the voltage. It should remain within the $8.25V_{DC}$ to $8.75V_{DC}$ range. The value of R2 may have to be selected in order to give the correct voltage reading.
12. Reconnect the jumper from R4 to ground.
13. The voltage at Pin 20 of P1 should be $1.10V_{DC}$ to $1.30V_{DC}$.
14. Turn off power and insert U6 into its socket.

Baud Rate Generation

1. Using an oscilloscope, look at the waveform on Pin 17 of the Baud Rate Generator, U1. This signal should swing from < 450mV to > 2.4V and have about a 50% duty cycle.
2. The frequency at this pin should be 153.6kHz. This results in a period of 6.51μs.
3. Repeat Steps 1 and 2 for Pin 18 of U1. The frequency should be 76.8kHz, resulting in a period of 13.0μs.

Control Functions

Connect an ASCII RS232 terminal to the computer connector, C1, on the LCP. The set up should be:

1. 9600 baud.
2. 8 bits.
3. 1 Stop bit.
4. No parity.
5. Terminal Tx to Pin 3 of the LCP C1 connector.
6. Terminal Rx to Pin 2 of the LCP C1 connector.

The following steps send ASCII characters to the LCP, which it should interpret as instructions. It will not echo the characters sent, but it should perform the instructions. Refer to Figure 5 for the ASCII equivalent instruction characters.

1. Turn on the LCP.
2. Set the ON-LINE/OFF-LINE switch to ON-LINE.
3. Type ".
4. Type !. The ON-LINE LED should illuminate. If the ON-LINE LED does not light at this point, check for the correct interfacing of Pins 2 and 3 on the RS232 terminal connector.
5. Type ". The ON-LINE LED should go back off.

TERM ADDRESS GENERATION

The purpose of this section is to test the ability of the LCP to uniquely load the bits of the term address. This is done by sending ASCII characters to the LCP and then checking the term address pins of P1.

Send the following lines of characters and check the P1 pins after each.

CHAR	1	2	3	4	5	6
!	On-Line — Address at Previous State					
SO	H	H	H	H	H	H
space	L	L	L	L	L	L
A	L	L	L	L	L	L
B	L	L	L	L	H	H
D	L	L	L	H	L	L
H	L	L	H	L	L	L
@Q	L	H	L	L	L	L
R	H	L	L	L	L	L
SO	H	H	H	H	H	H
N	H	H	H	H	H	L
M	H	H	H	H	L	H
K	H	H	H	L	H	H
G	H	H	L	H	H	H
OR	H	L	H	H	H	H
Q	L	H	H	H	H	H
S	H	H	H	H	H	H
@ P	L	L	L	L	L	L
	Off-Line — Address Not Altered					

VARIABLE ADDRESS GENERATION

The purpose of this section is to test the ability of the LCP to uniquely load and increment the bits of the Variable Address. This is done by sending the appropriate ASCII characters to the LCP and then checking the Term Address pins of P1.

Send each line of characters and check the specified P1 pins after each.

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CHAR	7	8	9	12	13	14	15
!	On-Line — Address Same as Previous						
wo	H	H	H	H	H	H	H
space	L	L	L	L	L	L	L
a	L	L	L	L	L	L	H
b	L	L	L	L	L	H	L
d	L	L	L	L	H	L	L
h	L	L	L	H	L	L	L
space q	L	L	H	L	L	L	L
r	L	H	L	L	L	L	L
t	H	L	L	L	L	L	L
ow	H	H	H	H	H	H	H
n	H	H	H	H	H	H	L
m	H	H	H	H	H	L	H
k	H	H	H	H	L	H	H
g	H	H	H	L	H	H	H
ov	H	H	L	H	H	H	H
u	H	L	H	H	H	H	H
s	L	H	H	H	H	H	H
w	H	H	H	H	H	H	H
A	L	L	L	L	L	L	L
owQ	L	L	L	L	L	L	L
1	L	L	L	L	H	L	L
1	L	L	L	H	L	L	L
2	L	L	L	H	H	L	L
2	L	L	H	L	L	L	L
I2	L	H	L	L	L	L	L
Is2	H	L	L	L	L	L	L
	Off-Line — Address Not Altered						

Fusing Cycle/Test Mode

Place a jumper from U1 Pin 3 to ground. This enables test mode. Send any data character and the LCP will continuously loop through the fusing sequence. Verify the voltages and timing per Figure 4.

Remove the jumper.

Pass Through

Turn the LCP ON-LINE/OFF-LINE switch to OFF-LINE.

Connect the Host Computer to the C1 connector of the LCP and the Terminal to T1 of the LCP. Make certain the Tx and Rx signals of both are associated with the correct LCP RS232 pins on the respective connectors.

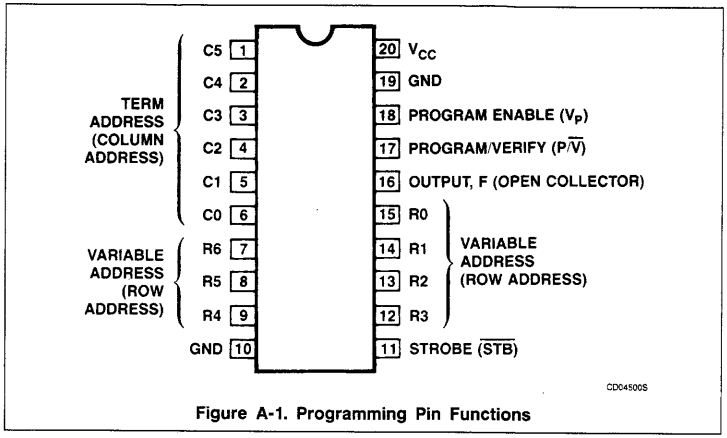

Figure A-1. Programming Pin Functions

Type on the terminal keyboard. The computer should behave normally – usually with an echo.

This completes the LCP calibration and checkout.

APPENDIX A

HOW TO PROGRAM PLD 20-PIN SERIES DEVICES

An PLD device is basically a group of logic functions interconnected to each other by fuses which can be blown to open a circuit, or left intact to make a connection. Each fuse can be identified by its own unique address which consists of a 7-bit Variable Address (ROW ADDRESS) and a 6-bit Term Address (COLUMN ADDRESS). The programming pin function is the same throughout the 20-pin series see Figure A-1). Tables A-1 and A-2 are fuse address tables of the PLS153 and PLS159, respectively.

The programming cycle can be separated into four stages:

Set-Up

1. Set Program Enable (V_P) to GND
2. Apply Column and Row Address to pins 1-6 and 7-9, 11-15
3. Set STROBE (STB) to V_{IH}
4. Set PROGRAM/VERIFY (P/V) to V_{IL}
5. Wait 1-50μs
6. Set V_{CCP} to 8.5V

To Blow a Fuse

1. Wait 1-10μs
2. Set P/V to V_{IH}
3. Wait 1-50μs
4. Set V_P to 14.5V
5. Wait 1-5μs
6. Pulse STB to V_{IL} for 10μs
7. Wait 1-5μs
8. Set V_P to GND
9. Wait 1-5μs
10. Set P/V to V_{IL}

To Verify

1. Wait 1-5μs
2. Pulse STB to V_{IL} for 1-10μs
3. While STB is LOW, OUTPUT (F) will be V_{IL} for a fuse intact and 2-8.75V for a blown fuse (note: F is an open-collector, a pull-up circuit may be needed)

Go To Set-Up for Next Fuse

Table A-1. Program Cycle Row/Column Fuse Addressing

PLS153

Variable Select Table[1]

ROW HEX ADDRESS		SELECTED VARIABLE	
$I_6I_7B_0$	$B_2B_3B_4B_5$		
0	0	AND Array	$\overline{I_0}$
0	1		I_0
0	2		$\overline{I_1}$
0	3		I_1
0	4		$\overline{I_2}$
0	5		I_2
0	6		$\overline{I_3}$
0	7		I_3
0	8		$\overline{I_4}$
0	9		I_4
0	A		$\overline{I_5}$
0	B		I_5
0	C		$\overline{I_6}$
0	D		I_6
0	E		$\overline{I_7}$
0	F		I_7
1	0		$\overline{B_9}$
1	1		B_9
1	2		$\overline{B_8}$
1	3		B_8
1	4		$\overline{B_7}$
1	5		B_7
1	6		$\overline{B_6}$
1	7		B_6
1	8		$\overline{B_5}$
1	9		B_5
1	A		$\overline{B_4}$
1	B		B_4
1	C		$\overline{B_3}$
1	D		B_3
1	E		$\overline{B_2}$
1	F		B_2
1	0		$\overline{B_1}$
1	1		B_1
1	2		$\overline{B_0}$
1	3		B_0

ROW HEX ADDRESS		SELECTED VARIABLE	
$I_6I_7B_0$	$B_2B_3B_4B_5$		
2 ↓	4 ↓	Empty Address Space	
2	F		
3	0	OR Array	9
3	1		8
3	2		7
3	3		6
3	4		5
3	5		4
3	6		3
3	7		2
3	8		1
3	9		0
3	A	Polarity Enable	
3 ↓	B ↓	Empty Address Space	
3	F		

Term Select Table[2]

COLUMN HEX ADDRESS		SELECTED PRODUCT TERM	
I_0I_1	$I_2I_3I_4I_5$		
0	0	Logic Terms	0
0	1		1
0	2		2
0	3		3
0	4		4
0	5		5
0	6		6
0	7		7
0	8		8
0	9		9
0	A		10
0	B		11
0	C		12
0	D		13
0	E		14
0	F		15
1	0		16
1	1		17
1	2		18
1	3		19
1	4		20
1	5		21
1	6		22
1	7		23
1	8		24
1	9		25
1	A		26
1	B		27
1	C		28
1	D		29
1	E		30
1	F		31
2	0	Control Terms	0
2	1		1
2	2		2
2	3		3
2	4		4
2	5		5
2	6		6
2	7		7
2	8		8
2	9		9
2	A	Polarity Terms	0
2	B		1
2	C		2
2	D		3
2	E		4
2	F		5
3	0		6
3	1		1
3	2		8
3	3		9

NOTES:
1. A row address identifies a particular variable coupled to all product terms.
2. With a variable selected by the row address the column address further selects a coupling fuse for each term.

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Table A-2. Program Cycle Row/Column Fuse Addressing (Continued)

PLS159

Variable Select Table[1]

ROW HEX ADDRESS		SELECTED VARIABLE	
$B_1B_2B_3$	$F_0F_1F_2F_3$		
0	0	AND Array	$\overline{B}_3$
0	1		B_3
0	2		$\overline{B}_2$
0	3		B_2
0	4		$\overline{B}_1$
0	5		B_1
0	6		$\overline{B}_0$
0	7		B_0
0	8		$\overline{I}_3$
0	9		I_3
0	A		$\overline{I}_2$
0	B		I_2
0	C		$\overline{I}_1$
0	D		I_1
0	E		$\overline{I}_0$
0	F		I_0
2	0		$\overline{F}_0$
2	1		F_0
2	2		$\overline{F}_1$
2	3		F_1
2	4		$\overline{F}_2$
2	5		F_2
2	6		$\overline{F}_3$
2	7		F_3
2	8		$\overline{F}_4$
2	9		F_4
2	A		$\overline{F}_5$
2	B		F_5
2	C		$\overline{F}_6$
2	D		F_6
2	E		$\overline{F}_7$
2	F		F_7
4	F		C_N

ROW HEX ADDRESS		SELECTED VARIABLE	
$B_1B_2B_3$	$F_0F_1F_2F_3$		
5	0	Flip-flop Control Terms	F_7 J
5	1		F_7 K
5	2		F_6 J
5	3		F_6 K
5	4		F_5 J
5	5		F_5 K
5	6		F_4 J
5	7		F_4 K
5	8		F_3 J
5	9		F_3 K
5	A		F_2 J
5	B		F_2 K
5	C		F_1 J
5	D		F_1 K
5	E		F_0 J
5	F		F_0 K
6	0	J-K/D Option	F_7
6	1		F_6
6	2		F_5
6	3		F_4
6	4		F_3
6	5		F_2
6	6		F_1
6	7		F_0
7	1	OR Array	B_3
7	2		B_2
7	3		B_1
7	4		B_0
7	5	C-Array	C_N
7	6	OE	EA
7	8	Polarity Terms	B_0
7	A		B_1
7	D		B_2
7	F		B_3

Term Select Table[2]

COLUMN HEX ADDRESS		SELECTED TERM	
$CLKI_0$	$I_1I_2I_3B_0$		
0	0	Transition Term	0
0	1		1
0	2		2
0	3		3
0	4		4
0	5		5
0	6		6
0	7		7
0	8		8
0	9		9
0	A		10
0	B		11
0	C		12
0	D		13
0	E		14
0	F		15
1	0		16
1	1		17
1	2		18
1	3		19
1	4		20
1	5		21
1	6		22
1	7		23
1	8		24
1	9		25
1	A		26
1	B		27
1	C		28
1	D		29
1	E		30
1	F		31
2	1	Control Term	PA
2	2		PB
2	3		RA
2	4		RB
2	5		LA
2	6		LB
2	7		FC
2	8	Output Enable	EA
2	9		EB
2	C		A EA
2	A		A EB
2	D		Polarity
2	E	Direction Control	D_0
2	F		D_1
3	0		D_2
3	1		D_3
2	0		Test Col. 2
3	2		Test Col. 1

NOTES:
1. A row address identifies a particular variable coupled to all product terms.
2. With a variable selected by the row address the column address further selects a coupling fuse for each term.

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APPENDIX B

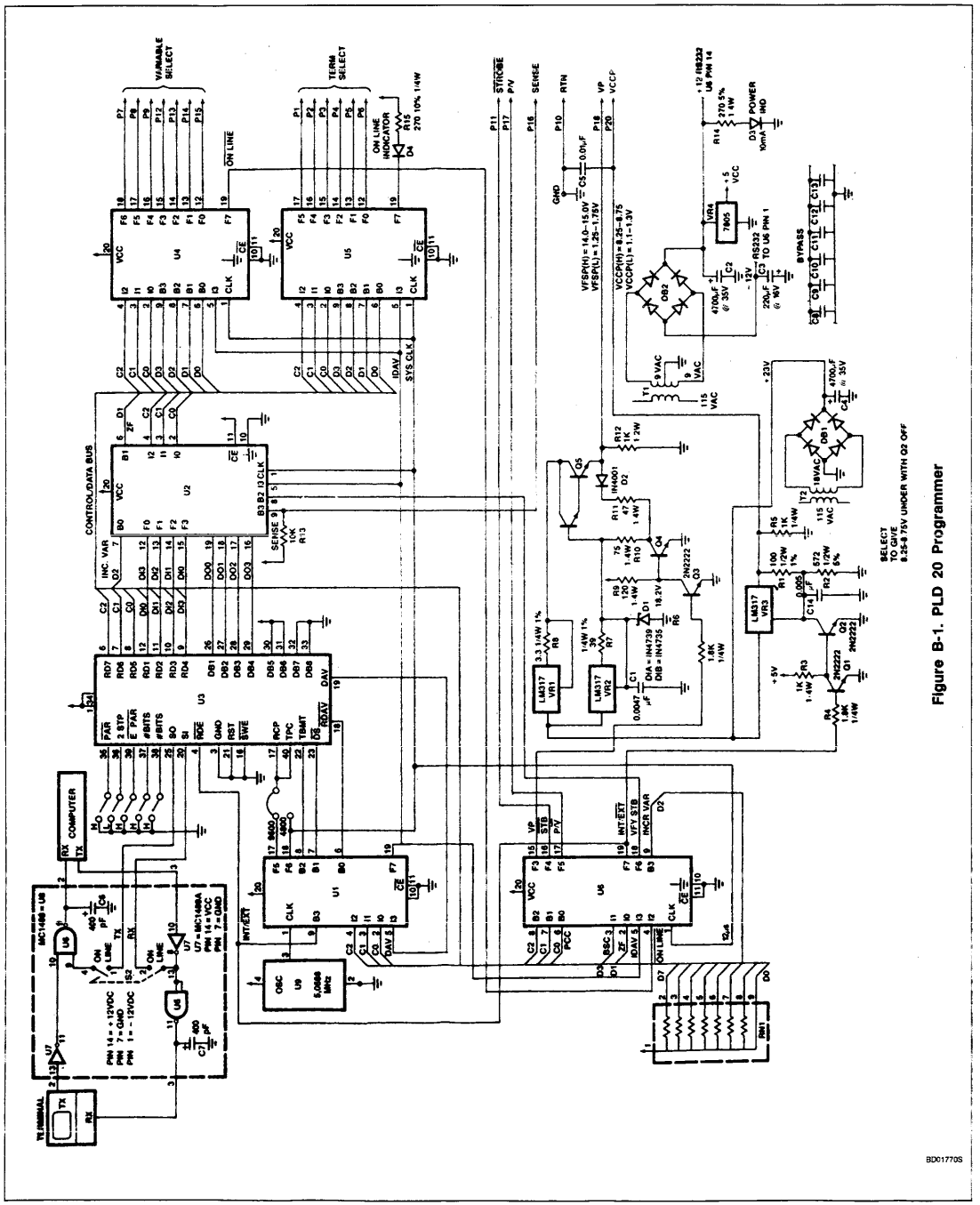

Figure B-1. PLD 20 Programmer

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Table B-1. Baud Rate Generation and UART Control PLD U1 Revision "B" Adds Test Mode

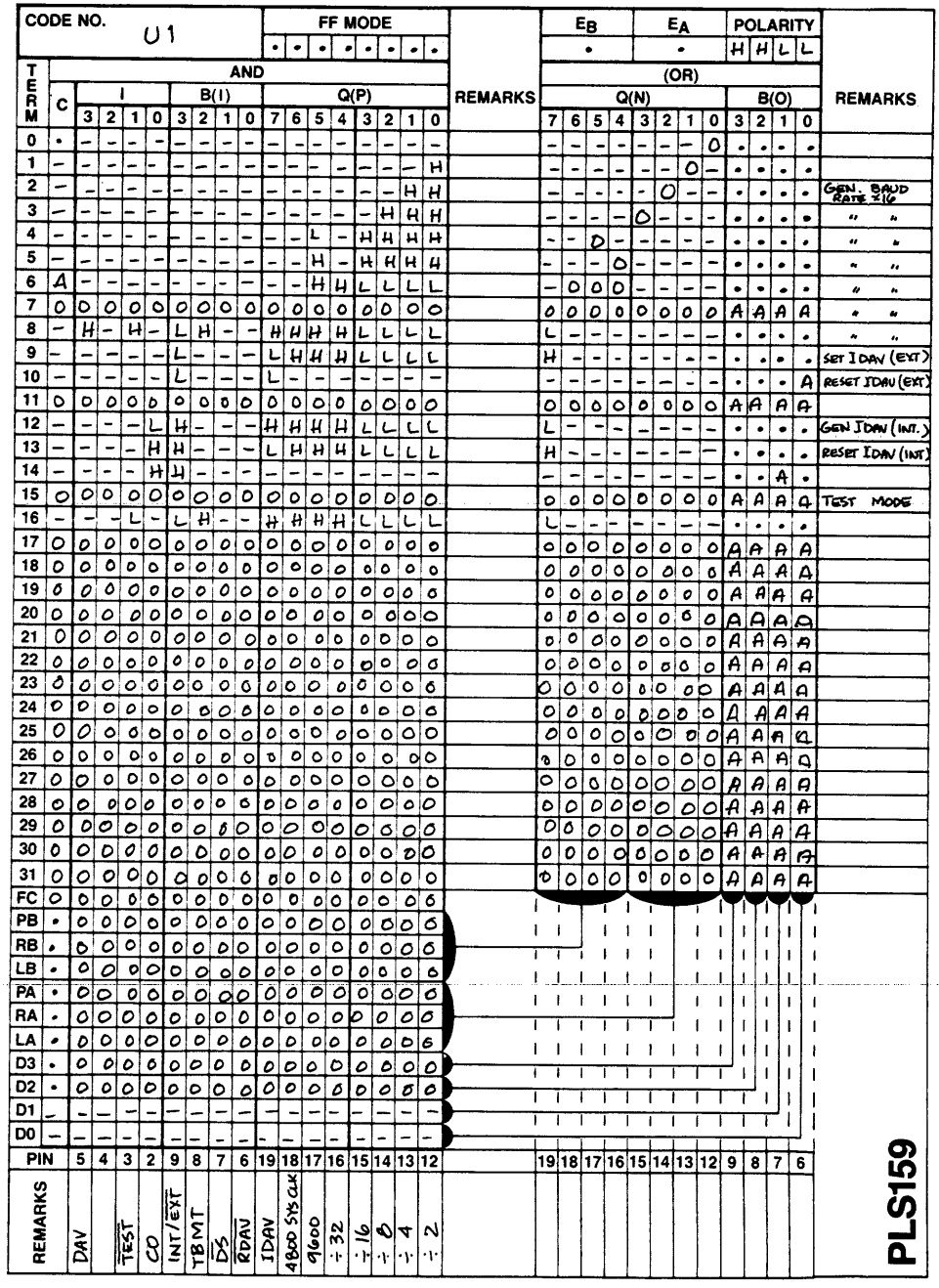

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Table B-2. Low Cost Programmer PLD #U4 Variable Address Generator

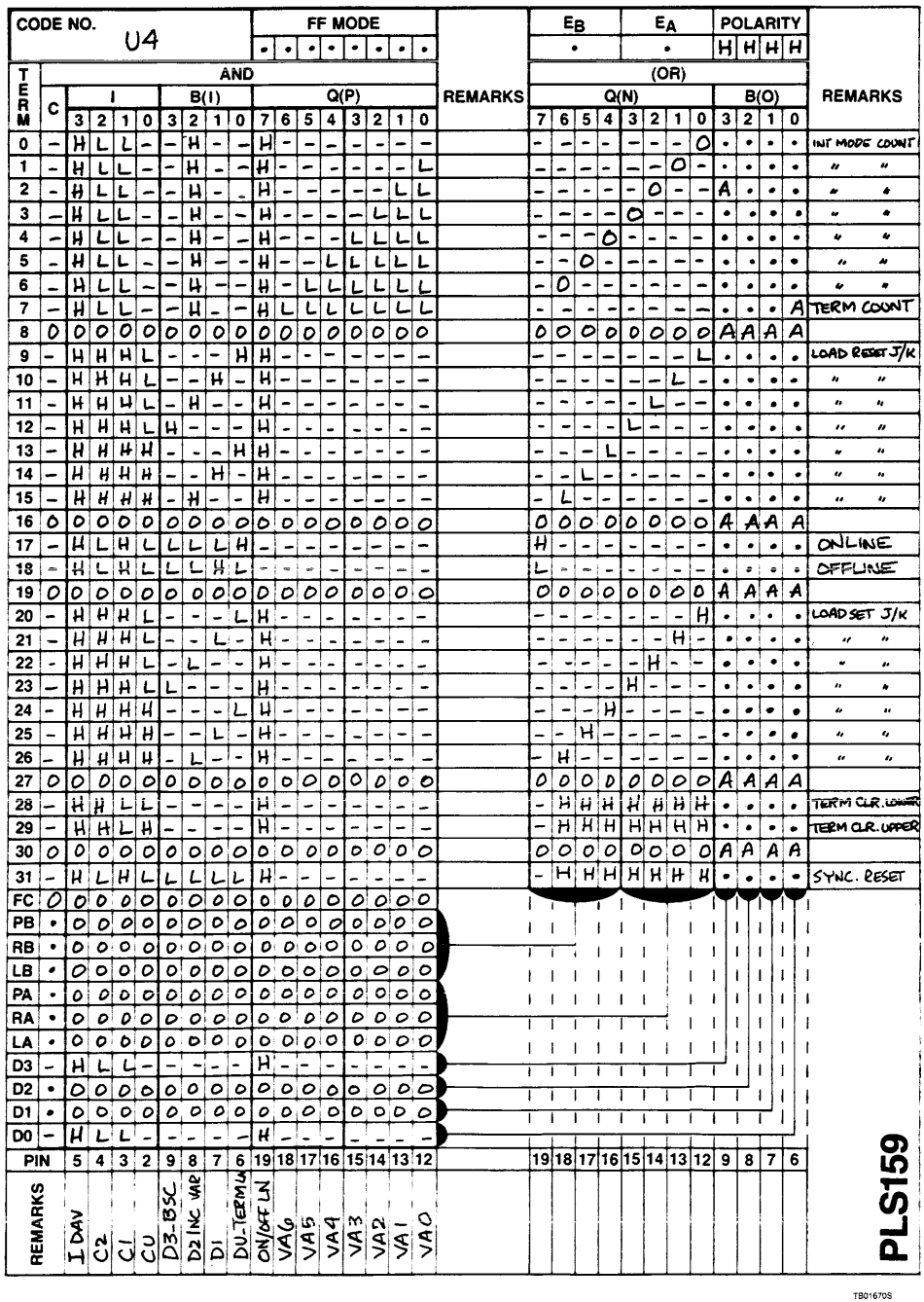

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Table B-3. Low Cost Programmer PLD #U4 Variable Address Generator

CODE NO. U5		FF MODE								REMARKS	E_B	E_A	POLARITY				REMARKS
		•	•	•	•	•	•	•	•		•	•	H	H	H	H	
TERM	AND										(OR)						
	C	I				B(I)					Q(P)									Q(N)								B(O)				
		3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	3	2	1	0	
0	–	H	L	L	–	–	–	–	H	H	–	–	–	–	–	–	0		–	–	–	–	–	–	–	0	•	•	•	•	INT. MODE CNT.
1	–	H	L	L	–	–	–	–	–	H	–	–	–	–	–	–	L		–	–	–	–	–	–	–	–	•	•	•	•	NOT USED
2	–	H	L	L	–	–	–	–	–	H	–	–	–	–	–	L	L		–	–	–	–	–	–	–	–	•	•	•	•	" "
3	–	H	L	L	–	–	–	–	–	H	–	–	–	–	L	L	L		–	–	–	–	–	–	–	–	•	•	•	•	" "
4	–	H	L	L	–	–	–	–	–	H	–	–	–	L	L	L	L		–	–	–	–	–	–	–	–	•	•	•	•	" "
5	–	H	L	L	–	–	–	–	–	H	–	–	L	L	L	L	L		–	–	–	–	–	–	–	–	•	•	•	•	" "
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
7	–	H	H	L	L	–	–	–	H	H	–	–	–	–	–	–	L		–	–	–	–	–	–	–	L	•	•	•	•	LOAD SET
8	–	H	H	L	L	–	–	H	–	H	–	–	–	–	–	L	–		–	–	–	–	–	–	L	–	•	•	•	•	" "
9	–	H	H	L	L	–	H	–	–	H	–	–	–	–	–	–	–		–	–	–	–	–	L	–	–	•	•	•	•	" "
10	–	H	H	L	L	H	–	–	–	H	–	–	–	–	–	–	–		–	–	–	–	L	–	–	–	•	•	•	•	" "
11	–	H	H	L	H	–	–	–	H	H	–	–	–	–	–	–	–		–	–	–	L	–	–	–	–	•	•	•	•	" "
12	–	H	H	L	H	–	–	H	–	H	–	–	–	–	–	–	–		–	–	L	–	–	–	–	–	•	•	•	•	" "
13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
14	–	H	L	H	L	L	L	L	H	–	–	–	–	–	–	–	–		H	–	–	–	–	–	–	–	•	•	•	•	ON LINE
15	–	H	L	H	L	L	L	H	L	–	–	–	–	–	–	–	–		L	–	–	–	–	–	–	–	•	•	•	•	OFF LINE
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
17	–	H	H	L	L	–	–	–	L	H	–	–	–	–	–	–	H		–	–	–	–	–	–	–	H	•	•	•	•	LOAD RESET
18	–	H	H	L	L	–	–	L	–	H	–	–	–	–	–	H	–		–	–	–	–	–	–	H	–	•	•	•	•	" "
19	–	H	H	L	L	–	L	–	–	H	–	–	–	–	–	–	–		–	–	–	–	–	H	–	–	•	•	•	•	" "
20	–	H	H	L	L	L	–	–	–	H	–	–	–	–	–	–	–		–	–	–	–	H	–	–	–	•	•	•	•	" "
21	–	H	H	L	H	–	–	–	L	H	–	–	–	–	–	–	–		–	–	–	H	–	–	–	–	•	•	•	•	" "
22	–	H	H	L	H	–	–	L	–	H	–	–	–	–	–	–	–		–	–	H	–	–	–	–	–	•	•	•	•	" "
23	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
24	–	H	L	L	–	–	–	–	H	H	–	–	–	–	–	–	L		–	–	–	–	–	–	0	–	•	•	•	•	INT. MODE COUNT
25	–	H	L	L	–	–	–	H	–	H	–	–	–	–	–	L	–		–	–	–	–	–	0	–	–	•	•	•	•	" "
26	–	H	L	L	–	–	–	H	–	H	–	–	–	–	L	L	–		–	–	–	–	0	–	–	–	•	•	•	•	" "
27	–	H	L	L	–	–	–	H	–	H	–	–	–	L	L	L	L		–	–	–	0	–	–	–	–	•	•	•	•	" "
28	–	H	L	L	–	–	–	H	H	–	–	L	L	L	L	L			–	–	0	–	–	–	–	–	•	•	•	•	" "
29	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	" "
30	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
31	–	H	L	H	L	L	L	L	L	H	–	–	–	–	–	–	–		–	H	H	H	H	H	H	H	•	•	•	•	SYNC. RESET
FC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0														
PB	•	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0														
RB	•	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0														
LB	•	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0														
PA	•	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0														
RA	•	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0														
LA	•	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0														
D3	•	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0														
D2	•	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0														
D1	•	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0														
D0	•	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0														
PIN		5	4	3	2	9	8	7	6	19	18	17	16	15	14	13	12		19	18	17	16	15	14	13	12	9	8	7	6	
REMARKS		IDAV	C2	C1	C0	D3	D2	D1	D0 TERM CNT.	ON/OFF LN.	N/A	TA5	TA4	TA3	TA2	TA1	TA0														

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Table B-4. Low Cost Programmer PLD #U2B Revision "3" Data Register

CODE NO. U2B										FF MODE								REMARKS	E_B	E_A	POLARITY				REMARKS
										A	A	A	A	A	A	A	A		•	A	H	H	H	H	
TERM	C	AND																	(OR)							
		I				B(I)				Q(P)									Q(N)				B(O)			
		3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	
0	–	–	–	–	–	–	–	–	–	–	–	–	–	L	–	–	–		–	–	–	–	–	–	–	–	A	B1+Ø OUT
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
2	–	H	L	L	–	–	–	H	–	–	H	–	–	–	–	–	–		H	–	–	–	–	–	–	–	•	•	•	•	SHIFT DOWN
3	–	H	L	L	–	–	–	H	–	–	–	H	–	–	–	–	–		–	H	–	–	–	–	–	–	•	•	•	•	" "
4	–	H	L	L	–	–	–	H	–	–	–	–	H	–	–	–	–		–	–	H	–	–	–	–	–	•	•	•	•	" "
5	–	H	L	L	–	–	–	H	–	H	–	–	–	–	–	–	–		–	–	–	H	–	–	–	–	•	•	•	•	" "
6	–	H	L	L	–	–	–	H	–	–	–	–	–	–	H	–	–		–	–	–	–	H	–	–	–	•	•	•	•	" "
7	–	H	L	L	–	–	–	H	–	–	–	–	–	–	–	H	–		–	–	–	–	–	H	–	–	•	•	•	•	" "
8	–	H	L	L	–	–	–	H	–	–	–	–	–	–	–	–	H		–	–	–	–	–	–	H	–	•	•	•	•	" "
9	–	H	L	L	–	–	–	H	–	–	–	–	–	H	–	–	–		–	–	–	–	–	–	–	H	•	•	•	•	" "
10	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	" "
11	–	H	L	L	–	H	H	L	–	–	–	–	–	–	–	–	–		L	–	–	–	–	–	–	–	•	•	•	•	VARIFY IN
12	–	H	L	L	–	L	H	L	–	–	–	–	–	–	–	–	–		H	–	–	–	–	–	–	–	•	•	•	•	" "
13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
14	A	H	L	L	–	–	–	H	–	–	–	–	–	–	–	–	–		–	–	–	–	–	–	–	–	•	•	•	•	SHIFT ENABLE
15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
17	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
18	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
19	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
20	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
21	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
22	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
23	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
24	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
25	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
26	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
27	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
28	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
29	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
30	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	A	A	A	A	
31	–	H	L	H	L	–	–	–	–	–	–	–	–	–	–	–	–		H	H	H	H	H	H	H	H	•	•	•	•	SYNE RESET
FC	•	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–														
PB	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0														
RB	•	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0														
LB	•	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0														
PA	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0														
RA	•	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0														
LA	–	H	L	H	H	–	–	–	–	–	–	–	–	–	–	–	–														
D3	•	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0														
D2	•	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0														
D1	•	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0														
D0	–	H	L	L	–	–	–	–	–	–	–	–	–	–	–	–	–														
PIN		5	4	3	2	9	8	7	6	19	18	17	16	15	14	13	12		19	18	17	16	15	14	13	12	9	8	7	6	
REMARKS																															

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Table B-5. Low Cost Programmer PLD #U6 Revision "B" Results in New Timing Figures

CODE NO. U6		FF MODE								REMARKS	E_B	E_A	POLARITY				REMARKS
TERM	C	AND I				B(I)					(OR) Q(N)						REMARKS
		3	2	1	0	3	2	1	0		7 6 5 4 3 2 1 0		3	2	1	0	
0	–	H	L	–	–	–	L	H	H		H H H L H H H H	L – – – – – – –	•	•	•	•	SET INT. MODE
1	–	–	L	–	–	–	–	–	–		L – – – – – – –	– – – – – – – –	•	A	A	•	SEND INT. MD. C4, C2
2	–	–	L	–	–	–	–	–	–		L H H L H H H H	– – – – – – L –	•	•	•	•	DELAY
3	–	H	L	–	H	–	–	–	–		L H H L H H L H	– – L – – – H –	•	•	•	•	SET PRD. MD. 2ND FSS
4	–	–	L	–	–	–	–	–	–		L H L L H H H H	– – – – L – – –	•	•	•	•	VSP ON
5	–	–	L	–	–	–	–	–	–		L H L L L H H H	– – – – – – – L	•	•	•	•	DELAY
6	–	–	L	–	–	–	–	–	–		L H L L L H H L	– – – H – L – H	•	•	•	•	STROBE ON & DOWN
7	–	–	L	–	–	–	–	–	–		L H L H L L H H	– – – L – – – –	•	•	•	•	STROBE OFF
8	–	–	L	–	–	–	–	–	–		L H L L L L H H	– – – – H – – –	•	•	•	•	VP OFF
9	0	0	0	0	0	0	0	0	0		0 0 0 0 0 0 0 0	A A A A	A	A	A	A	
10	–	–	L	–	–	–	–	–	–		L H L L H L H H	– – H – – – – –	•	•	•	•	SET VERIFY MODE
11	–	–	L	–	–	–	–	–	–		L H H L H L H H	– – – H – – – –	•	•	•	•	STROBE ON
12	–	–	L	–	–	–	–	–	–		L H H H H L H H	– L – – – – – –	•	•	•	•	INT. STROBE ON
13	–	–	L	–	–	–	–	–	–		L L H H H L H H	– H – – – – L –	•	•	•	•	INT. STROBE OFF
14	–	–	L	–	–	–	–	–	–		L H H H H L L H	– – – L – – – –	•	•	•	•	STROBE OFF
15	–	–	L	L	–	–	–	–	–		L H H L H L L H	– – – – – H H –	A	•	•	•	INCR. VAR ($\overline{ESC}$)
16	0	0	0	0	0	0	0	0	0		0 0 0 0 0 0 0 0	A A A A	A	A	A	A	
17	–	–	L	H	–	–	–	–	–		L H H L H L L H	– – – – – H – L	A	•	•	•	BAIL OUT
18	A	–	L	–	–	–	–	–	–		L H H L H L L L	– – – – – – H –	•	•	•	•	SEND CYCLE COMP.
19	–	–	L	–	–	–	–	–	–		L H H L H H H L	H – – – – – – –	•	•	•	•	CLEAR INT. MODE
20	–	–	L	–	–	–	–	–	–		H H H L H H H L	– – – – – – – H	•	•	•	•	WAIT (EXT. MODE)
21	0	0	0	0	0	0	0	0	0		0 0 0 0 0 0 0 0	A A A A	A	A	A	A	
22	–	H	L	–	L	–	–	–	–		L H H L H H L H	– – – – – L H –	•	•	•	•	SET VFY (ZAP)
23	0	0	0	0	0	0	0	0	0		0 0 0 0 0 0 0 0	A A A A	A	A	A	A	
24	•	–	L	–	–	–	–	–	–		L – – – – – – –	– – – – – – – –	•	•	•	A	SEND INT MD (C0)
25	0	0	0	0	0	0	0	0	0		0 0 0 0 0 0 0 0	A A A A	A	A	A	A	
26	0	0	0	0	0	0	0	0	0		0 0 0 0 0 0 0 0	A A A A	A	A	A	A	
27	0	0	0	0	0	0	0	0	0		0 0 0 0 0 0 0 0	A A A A	A	A	A	A	
28	0	0	0	0	0	0	0	0	0		0 0 0 0 0 0 0 0	A A A A	A	A	A	A	
29	–	–	H	–	–	–	–	–	–		H H H L H H H H	• • • •	•	•	•	•	OFFLINE INITIAL
30	–	H	L	–	–	–	L	H	L		– H H L H H H H	• • • •	•	•	•	•	COMPUTER INITIAL
31	–	–	–	–	–	–	–	–	–		H H H – H H H H	• • • •	•	•	•	•	PWR UP INITIAL
FC	0	0	0	0	0	0	0	0	0								
PB	•	0	0	0	0	0	0	0	0								
RB	•	0	0	0	0	0	0	0	0								
LB	•	0	0	0	0	0	0	0	0								
PA	•	0	0	0	0	0	0	0	0								
RA	•	0	0	0	0	0	0	0	0								
LA	•	0	0	0	0	0	0	0	0								
D3	–	–	–	–	–	–	–	–	–								
D2	–	–	–	–	–	–	–	–	–								
D1	–	–	–	–	–	–	–	–	–								
D0	–	–	–	–	–	–	–	–	–								
PIN		5	4	3	2	9	8	7	6	19	18	17	16	15	14	13	12
REMARKS		DAY	ONLINE	D3-BSC	D1-ZF	D2 INC. VAR.	C2	C1	C0	INT/EXT	VEY S B	MODE P/V	$\overline{EN}$	VFSP	UP-DOWN	TDI	TDO

19	18	17	16	15	14	13	12	9	8	7	6

PLS159

TB01700S

Low Cost Programmer for PLD 20-Pin Series AN12

Table B-6. Low Cost Programmer Parts List

REF. DES.	QUANT.	DESCRIPTION	RADIO SHACK#
Resistors			
R1	1	100Ω 1/4W 5%	
R2	1	620Ω 1/4W 5%	
R3, R5	2	1KΩ 1/4W 5%	271-1421
R14, R15	2	270Ω 1/4W 5%	
R4, R6	2	1.8KΩ 1/4W 5%	271-1324
R7	1	39Ω 1/4W 5%	
R8	1	3.3Ω 1/4W 5%	
R9	1	120Ω 1/4W 5%	
R10	1	75Ω 1/4W 5%	
R11	1	47Ω 1/4W 5%	271-1307
R12*	1	1KΩ 1/4W 5%	271-023
R13	1	10KΩ 1/4W 5%	
RN1	1	10KΩ 1/4W 5% 8-Pin SIP	
Capacitors			
C1	1	0.047μF	
C2, C4	2	4700μF Elec. 35V Axial	272-1022
C3	1	220μF Elec. 35V Axial	272-1017
C6, C7	2	470μF	
C5, C8 – C13	7	0.01μF	
Diodes			
D1A	1	6.2V Zener 1N4735	276-561
D1B	1	9.1V Zener 1N4739	276-563
D2	1	1N4001	276-1101
D3, D4	2	10mA Red LED	276-041
DB1, DB2	2	1.4A Full-Wave Bridge	276-1151
Voltage regulators			
VR1 – VR3	3	LM317 TO-220	276-1778
VR4	1	7805 TO-3	
Integrated circuits			
U1, U2, U4 – U6	5	PLS159IFL — Codes Req'd	
U3	1	AY-3-1015 UART	276-1794
Transformers			
T1, T2	2	18.0VAC CT, 2A	273-1515
FB1	1	Ferrite Bead FB-75B-01 Amidon Associates	
Transistors			
Q1 – Q4	4	2N2222 Transistors	276-2009
Q5	1	TIP 120 Power Dar.	

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Low Cost Programmer for PLD 20-Pin Series

AN12

APPENDIX C

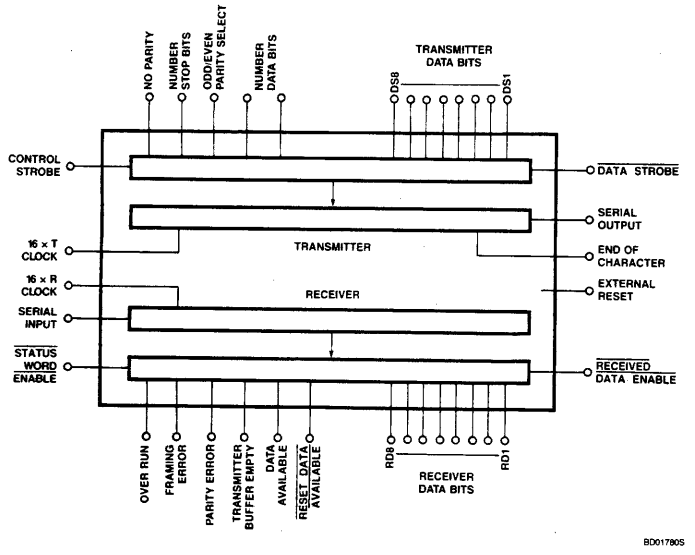

Figure C-1. Block Diagram

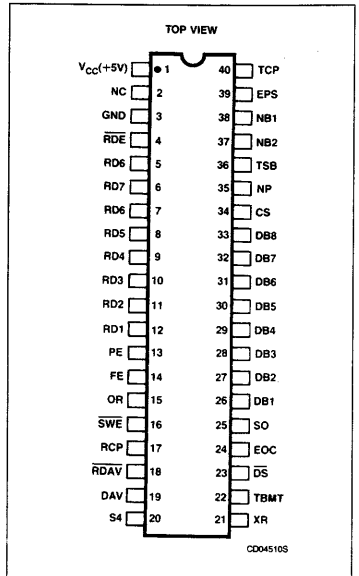

Figure C-2