

TTL Programmable Delay Lines

16-pin DIP

For delay adjustments via BCD programming. Simplifies minor adjustments and adds flexibility. Although indicated below that programmable modules are available up to 3-bit, 6-bit modules are available through a simple combination of modules (see next page).

- 5 to 500 ns delays available.
- 3-bit binary (1, 2, 4) programming gives 7 equal step delays.
- Low on \overline{E} enables output.
- **■** Complimentary output available.
- Available in 19 step delays from 1 to 64 ns.
- **■** Designed for leading-edge timing.
- Low inherent delay from:

Input to output = 6.0 ± 1.5 ns. Input to $\overline{\text{output}} = 3.0 \pm 1.5 \text{ ns.}$

E to output = 10.0 ns maximum

 S_n to output = 13.0 ns maximum

- Transfer molded reliable. Contact factory for other logic specifications.
- Military models with temperature range of -55 to +125°C and ceramic package IC to meet MIL-STD-883C, add suffix "M" to part number.
- Military models as "M" above, but with ceramic package IC screened to MIL-STD -883C, add suffix "MX" to part number.
- Military models as "MX" above, but with in-house burn-in and thermal shock, add suffix "MY" to part number.
- Specifications are for Schottky TTL only.

MODEL HTTLDL ACTIVE TTL DELAY LINES

TECHNITROL PART NO.	Step Delay ns ± ns	Max. Delay ns ± ns	Output Rise Time (ns)
TTLPG301	$1.0 \pm .4$	13.0 ± 2.0	2.0
TTLPG302	$2.0 \pm .6$	20.0 ± 2.0	2.0
TTLPG303	3.0 ± 1.0	27.0 ± 2.0	2.0
TTLPG304	4.0 ± 1.0	34.0 ± 2.0	2.0
TTLPG305	5.0 ± 1.5	41.0 ± 2.0	2.0
TTLPG306	6.0 ± 1.5	48.0 ± 2.0	2.0
TTLPG307	7.0 ± 1.5	55.0 ± 2.5	2.0
TTLPG308	8.0 ± 1.5	62.0 ± 2.5	2.0
TTLPG309	9.0 ± 1.5	69.0 ± 3.0	2.0
TTLPG310	10.0 ± 1.5	76.0 ± 3.5	2.0
TTLPG315	15.0 ± 1.5	111.0 ± 5.0	2.0
TTLPG320	20.0 ± 1.5	146.0 ± 7.0	2.0
TTLPG325	25.0 ± 1.5	181.0 ± 9.0	2.0
TTLPG330	30.0 ± 2.0	216.0 ± 11.0	2.0
TTLPG335	35.0 ± 2.0	251.0 ± 12.0	2.0
TTLPG340	40.0 ± 2.5	286.0 ± 14.0	2.0
TTLPG345	45.0 ± 3.0	321.0 ± 16.0	2.0
TTLPG350	50.0 ± 3.5	356.0 ± 17.0	2.0
TTLPG364	64.0 ± 4.0	454.0 ± 23.0	2.0

Delay Characteristics measured at $V_{CC} = 5.0V$ and $T_a = 25$ °C, no load.

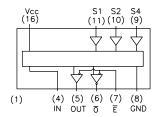
Delay time measured at 1.5V level.

Rise Time measured @ 0.8V to 2.0V levels.

For minimum input pulse width -- contact factory.



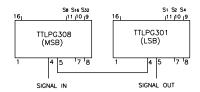
SCHEMATIC



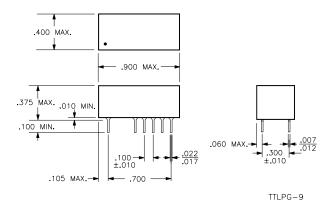
TTLPG 16-pin DIP

CASCADE EXAMPLE

Example of 6-bit cascade with 63 steps of 1.0 ns delay with an inherent (or reference) delay of 12.0 ns (2×6.0 ns).



MECHANICAL OUTLINE



Notes

- Only the pins specified in the schematics are provided with each package.
- Pin numbers shown are for reference only and are not necessarily marked on unit.
- Lead material is electro tin plated (alloy 42) or solder dipped.
- All specifications are subject to change without notice.

Delay Characteristics measured at $V_{CC} = 5.0V$, 25°C, no load. Delay Tolerance ± 2 ns or 5%, whichever is greater. Rise time measured @ 0.8V to 2.0V levels. For minimum input pulse width -- contact factory.