1986

PMI Linear and Conversion Applications

Linear and Conversion Applications Handbook

1986

Precision Monolithics Inc.

- Operational Amplifiers
- Instrumentation Amplifiers
- Voltage Followers/ Buffers
- Voltage Comparators
- Matched Transistors
- Voltage References
- Digital-to-Analog Converters
- Analog-to-Digital Converters
- Analog Switches/ Multiplexers
- Sample-and-Hold Amplifiers
- Special Functions
- Communications Circuits

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Linear and Conversion Applications Handbook

1986

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Note to the Reader:
To make it easier to locate applications information within this book, the contents have been indexed three ways on the pages indicated above. Some examples include:

- Major Topics —
  amplifiers, communications circuits
- Subjects —
  current monitors, isolation amplifiers
- PMI Part Numbers —
  ADC-910, MAT-04

Additional applications data and complete product specifications may be found in PMI's 1986 Data Book which is available upon request.

Author Acknowledgments

This handbook was prepared by the engineering staff of Precision Monolithics Inc. and contributing authors. It reflects the combined efforts of many people. We gratefully acknowledge each author's contribution.

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INDEX BY MAJOR TOPIC

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Amplifiers

A/D And D/A Converter Circuits

Refer to PMI's 1986 Data Book for additional applications.

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INDEX BY MAJOR TOPIC

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Signal Conditioning And Measurement

Analog Signal Processing Circuits

Signal Switching Circuits

Communication Circuits

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AB-1

STROBING THE DAC-08 UNDER LOGIC CONTROL

Precision Monolithics Inc.

APPLICATION BRIEF 1

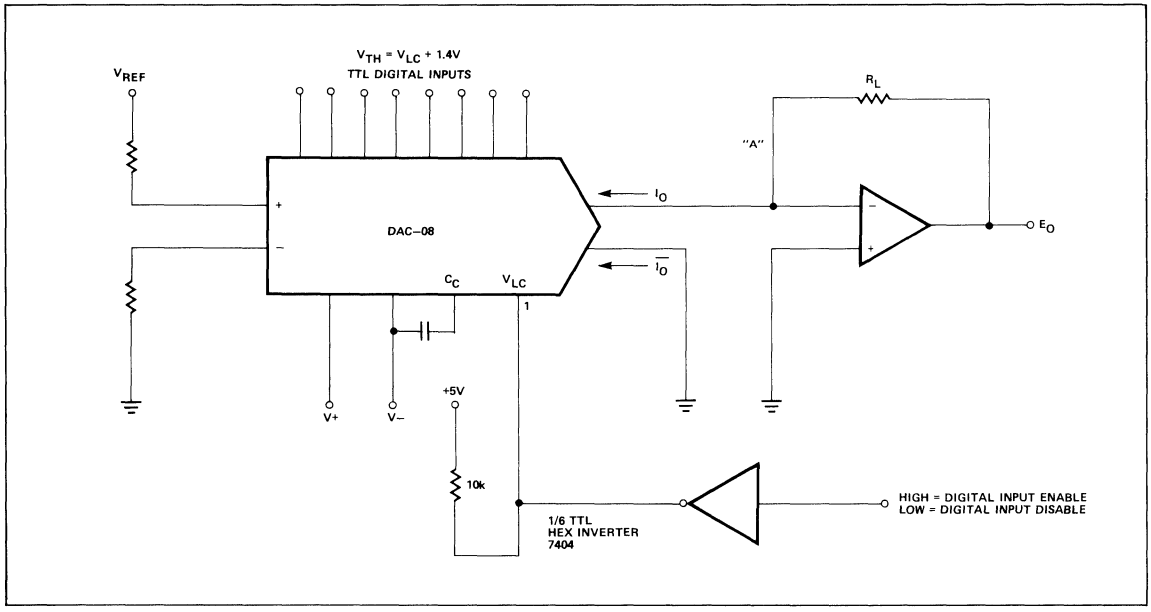
FEATURES

- Digital inputs are treated as all zeros by increasing the logic threshold to +6.4V.
- Single Line Logic Control
- Handy in Multiplying Applications
- When more than one DAC is connected to point "A" —party line connection — strobing is simple.
- Higher speed and greater simplicity when compared to the alternative method of disabling which is accomplished by reducing V_{REF} to zero.

GENERAL DESCRIPTION

Since the PMI DAC-08 has a variable logic input threshold, strobing the output is easily accomplished using the circuit below. Normally, for TTL thresholds, Pin 1 (V_{LC}) is grounded; but if it is connected instead to a hex inverter with a pullup resistor to +5V, all digital inputs effectively become zeros. When the hex inverter's output is high, no current flows in I_O no matter what the digital input code may be. When the hex inverter's output is low, normal TTL input logic threshold and operation is restored.

NOTE:
Recovery when logic inputs are enabled may be slower when DAC is on ±5V supply due to bias line saturation. This should be checked in the actual application.



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AB-2

OP-10 INSTRUMENTATION AMPLIFIER CMRR vs FREQUENCY IMPROVEMENT

Precision Monolithics Inc.

APPLICATION BRIEF 2

FEATURES

- Addition of one selected capacitor improves CMRR at 400Hz to >95dB.
- OP-10 Side "A" and Side "B" bandwidths are matched.
- Circuit uses existing nulling pins as frequency compensation connections.
- Added capacitor is in the range of 5pF to 100pF.

CAPACITOR SELECTION PROCEDURE

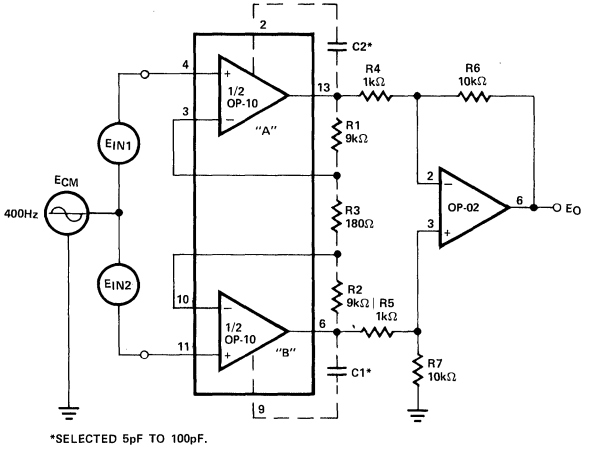
1. Connect E_{IN1} to E_{IN2} and to a 400Hz ±10V signal source.
2. While observing E_O with an oscilloscope, try different values of C1 or C2 until E_O is at a minimum.
3. Permanently install the selected capacitor.

GENERAL DESCRIPTION

Common mode rejection ratio (CMRR) versus frequency of the familiar three op-amp instrumentation amplifier can be optimized by matching the frequency responses of the input differentially-connected pair of op amps. The circuit shown uses one selected capacitor (to reduce the frequency response of the faster op amp) which is connected between an output and one of the pins usually used for nulling ΔV_{OS}.

Eight devices were tested in this connection. Improvement to greater than 95dB @ 400Hz was achieved on all devices, an improvement of 1 to 20dB over performance without the selected capacitor.

TRIPLE OP-AMP INSTRUMENTATION AMPLIFIER CIRCUIT



*SELECTED 5pF TO 100pF.

NOTES:

1. $E_O = (E_{IN1} - E_{IN2})\,A_{VCL}$
2. $A_{VCL} = \left(1 + \frac{R1 + R2}{R3}\right)\left(\frac{R6}{R4}\right) = 1000$
3. $CMRR = 20 \text{ LOG } \frac{E_{CM}\,(A_{VCL})}{E_O}$ @ DC
4. IF $\frac{R6}{R4} = \frac{R7}{R5}$, CMRR @ DC ≅ 120dB
5. AT 400Hz, CMRR IS A FUNCTION OF THE DIFFERENCE IN FREQUENCY RESPONSE OF SIDE "A" AND SIDE "B".
6. USE OF C1 OR C2, SELECTED USING THE PROCEDURE DESCRIBED, MATCHES THE FREQUENCY RESPONSE OF SIDE "A" AND SIDE "B", THEREBY MAXIMIZING CMRR AT 400Hz.

AB-3

DIGITAL NULLING OF PRECISION OP AMPS

Precision Monolithics Inc.

APPLICATION BRIEF 3

FEATURES

- Digitally-controlled offset nulling is achieved by imbalancing the first stage collector currents of a precision op amp.
- Greater than 1.5mV of offset voltage may be nulled to zero with 5μV resolution at 25° C.
- This application is especially useful in microprocessor-controlled systems where stringent error budgets exist.
- Circuit uses the nulling terminals with a DAC-08 substituted for the conventional nulling potentiometer.

GENERAL DESCRIPTION

The input offset voltage of a precision op amp (OP-05, OP-07, OP-77) may be nulled to <5μV using the complementary current outputs of a DAC-08 to change the ratio of collector currents in the first stage. With V_{OS} being defined as the voltage which must be applied between the input terminals to force V_{OUT} to zero and assuming all errors to be in the first stage, V_{OS} may be expressed as:

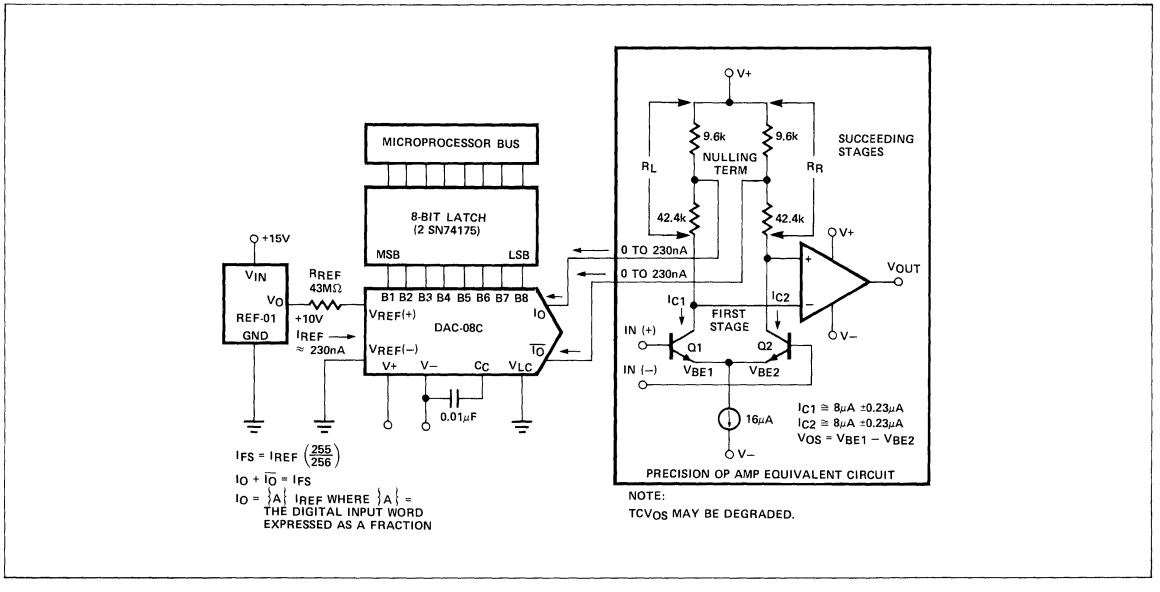
1) $$V_{OS} = \frac{kT}{q} \log_e \frac{I_{C1}}{I_{C2}} \cdot \frac{I_{S2}}{I_{S1}}$$

where:

k = Boltzmann's constant = 1.38 x 10^{-23} joules/° K
T = Absolute temperature, ° K
q = Charge of an electron = 1.6 x 10^{-19} coulomb
I_S = Theoretical reverse-saturation current
I_C = Collector Current

Changing the ratio I_{C1}/I_{C2} over a ±3% range results in an input offset voltage nulling range of greater than 1.5mV at 25° C.

CIRCUIT



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AB-4

REF-02
TEMPERATURE CONTROLLER

Precision Monolithics Inc.

APPLICATION BRIEF 4

FEATURES

- **Variable Temperature Control**
- **Adjustable Hysteresis**
- **12V To 32V Power Supply**
- **2 IC Design**
- **Low Cost**

SETPOINT DETERMINATION

With $R2 = 1.5k\Omega$, the value of R1 may be found for any desired temperature using the following procedure:

$$E_1 \cong (\text{Desired Temp} - 25°C)\,(2.1mV/°C) + 630mV$$

$$R1 \cong R2\left(\frac{5 - E_1}{E_1}\right)$$

DESCRIPTION

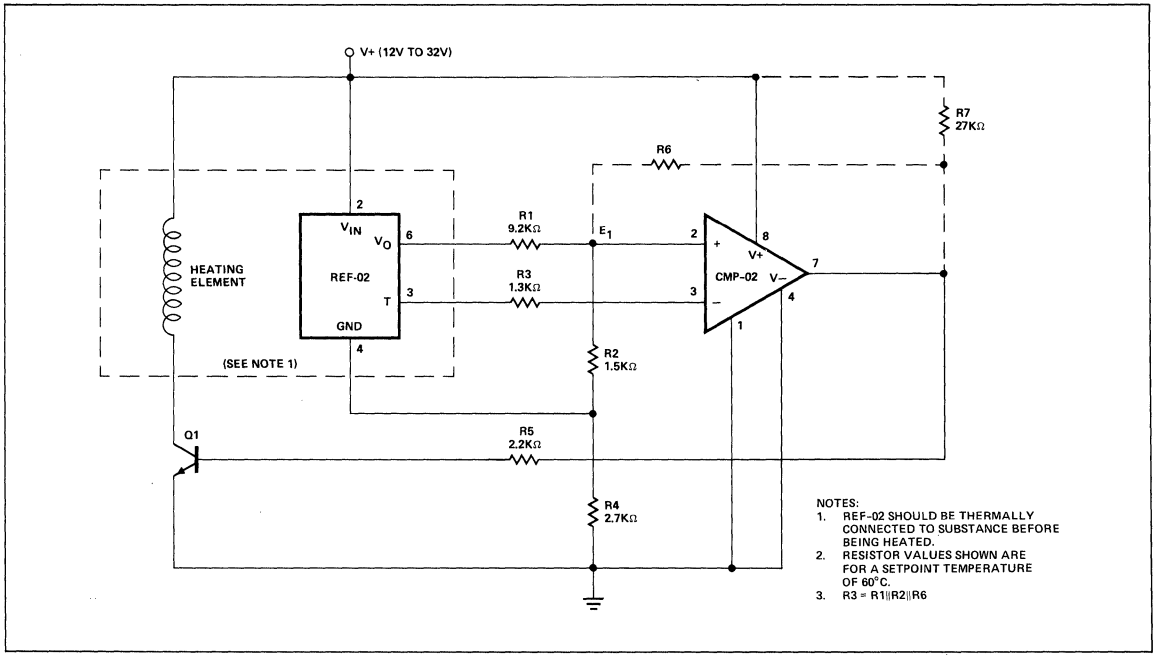
In the circuit below, temperature control is achieved using the REF-02 +5V Reference/Thermometer and a CMP-02 Precision Low Input Current Comparator. The CMP-02 turns on a heating element driver (Q1) whenever the present temperature drops below a setpoint temperature determined by the ratio of R1 to R2. The circuit also provides adjustable hysteresis and single supply operation.

HYSTERESIS DETERMINATION

R6 and R7 set hysteresis. With $R7 = 27k\Omega$, R6 may be calculated:

$$R6 \cong \frac{\left[(V+) - 4V\right]}{(2.1mV/°C)\ (\text{Hysteresis width in } °C)}$$

CIRCUIT



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AB-6

SINGLE SUPPLY OPERATION OF THE DAC-08 AND DAC-20

Precision Monolithics Inc.

APPLICATION BRIEF 6

FEATURES

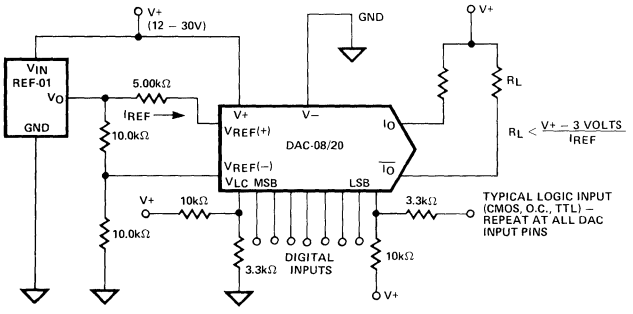
- **Simple Interface**
- **Compatible with CMOS and Open Collector TTL**
- **No Degradation in Performance**

GENERAL DESCRIPTION

The DAC-08 may be operated from a single supply when properly biased. This circuit will allow the use of a single power supply, or battery, and still realize the premium performance of these high speed DACs.

The resistive voltage divider inputs to V_{LC} and logic inputs provide the necessary voltage levels for operation from CMOS and Open Collector TTL logic.

CIRCUIT



AB-9
DUAL PRECISION VOLTAGE REFERENCE

Precision Monolithics Inc.

APPLICATION BRIEF 9

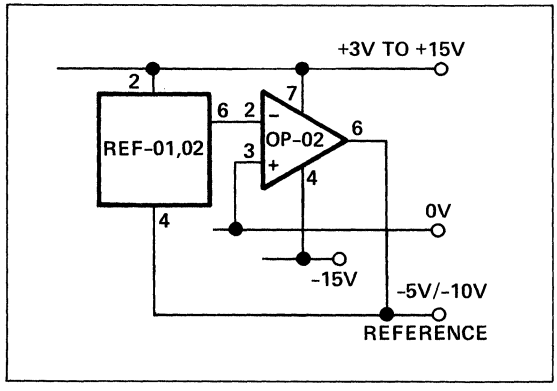
FEATURES

- **Dual Outputs** ..... **±10V**
- **Temperature Coefficient** ..... **3.3ppm/° C**
- **Positive Output Tracks Negative Output**
- **Load Regulation** **0.0005%/mA**
- **Line Regulation** **0.0005%/Volt**

GENERAL DESCRIPTION

Three-terminal voltage references like the REF-01 and REF-02 are easily configured to provide a negative output voltage with the addition of a single op-amp, (see Figure 1). The op-amp specs are not critical, offset voltage drift being the important parameter. TCV_{OS} of 10μV/° C adds approximately 1ppm/° C drift to the references own TC for a −10V output and 2ppm/° C for a −5V output. Performance can be improved by replacing the OP-02 with an OP-07.

FIGURE 1

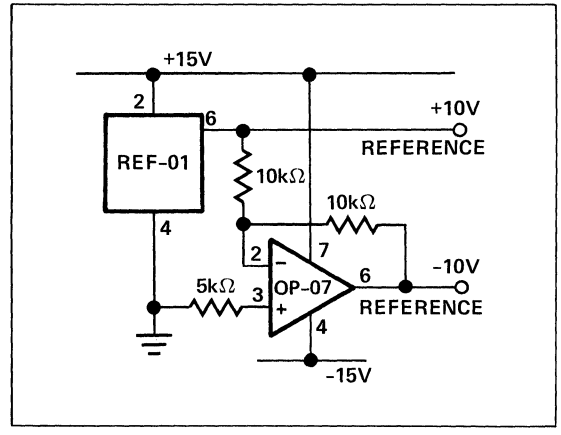


Line regulation is virtually the same as for the reference itself. Load regulation is improved by a factor of 2 for an output change of 0 to −5mA. Output current is provided by the op-amp so this is the limiting factor for output drive.

DUAL PRECISION REFERENCE

The conventional dual reference, shown in Figure 2, uses a REF-01 and an op-amp connected as a unity gain inverter.

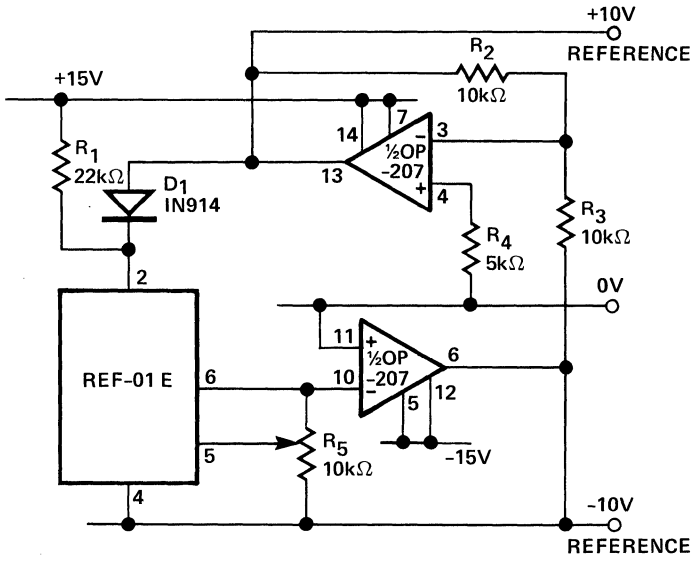
FIGURE 2



The circuit gives excellent performance but can be improved by reconfiguring and adding another op-amp, (see Figure 3).

The main advantage is improved line regulation. This is achieved by powering the REF-01 from the +10 volt stabilized output. This makes both reference outputs virtually independent of supply variations, temperature coefficient of the reference contributing most of the remaining error.

FIGURE 3



Components R_1 and D_1 ensure correct circuit start-up and R_5 adjusts the negative output. The positive output tracks the negative with an accuracy determined by the inverting amplifier and resistors R_2 and R_3. Positive output drift relative to negative has two components; 2 X TCV_{OS} caused by the inverting amplifier (approx. 0.2ppm/° C error), and the ratio TC match of R_2 and R_3. Therefore, for best performance R_2 and R_3 must be ratio matched for resistance value and temperature coefficient.

Load and line regulation are typically 0.0005% for this improved reference configuration. Temperature coefficients are typically 3.3ppm/° C for a REF-01E used with an OP-207F. Guaranteed long term stability can be specified by replacing the REF-01 with a REF-10 (max. 50ppm/1000 hours).

AB-101
PRECISION AUDIO SWITCH

Precision Monolithics Inc.

APPLICATION BRIEF 101

APPLICATIONS:

- **Professional Audio Equipment**
- **Electronic Music**
- **Satellite Communications**
- **Speech Synthesis**

FEATURES

- **Total Harmonic Distortion** **0.003%**
- **Slew Rate** **17V/μs**
- **Feedthrough Attenuation** ..... **>95dB**
- **Signal-to-Noise Ratio** **118dB**
- **Drive Capability** **600Ω**

GENERAL DESCRIPTION

The technology of High Fidelity Sound Reproduction has experienced continued emphasis in digitization, control, and processing of audio signals. The ability to switch analog signals at high speed predominates the manufacturing of professional audio equipment. The precision audio switch is an electronic solution. This application uses a SW-06 JFET analog switch and an OP-37 low-noise operational amplifier to achieve unequalled performance with a minimum of components.

ANALOG SWITCHING

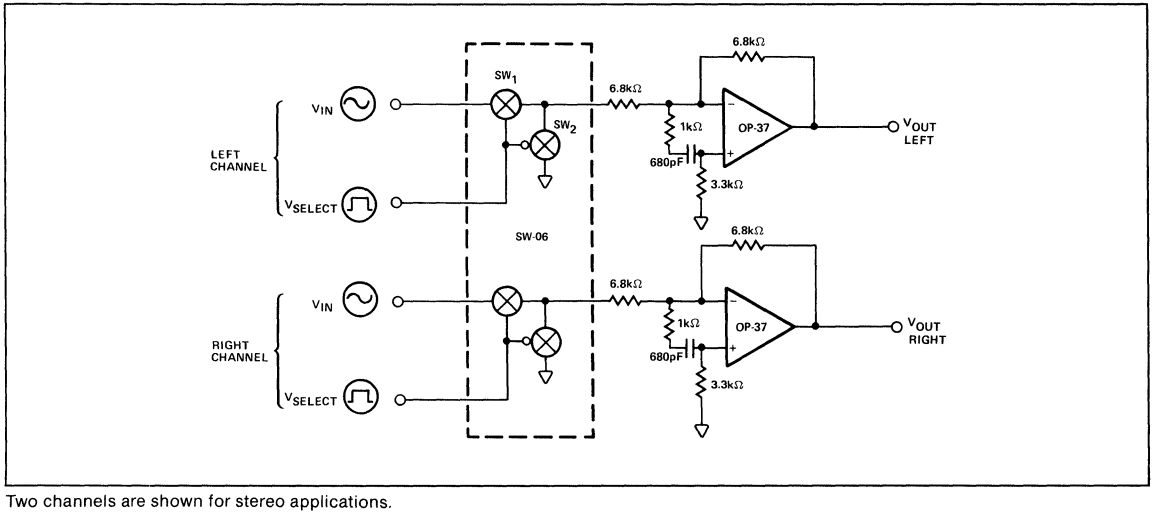
Mechanical switches have rapidly become obsolete due to the increased complexity of multi-channel matrix switchers and the extensive use of high-resolution converters and microprocessor interfacing. In addition, contact wear and contamination degrade instrument performance with age.

The circuit illustrated below virtually eliminates mechanical switching effects and achieves fast switching speeds without introducing any significant errors. The precision audio switch features a total harmonic distortion of 0.003% and a slew rate of 17V/μs, making it ideal for use in conjunction with 16-bit conversion systems. In the OFF state the feedthrough attenuation is greater than −95dB over the full audio range. Intermodulation distortion (CCIF method) is less than 0.02%. Switching and settling time is approximately 1μs.

CIRCUIT OPERATION

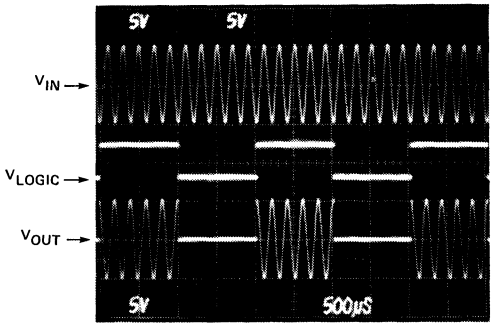
The decompensated OP-37, normally used in gains of five or more, accurately achieves stability in a unity-gain configuration. This design takes advantage of the components' speed and superb noise characteristics. The logic configuration in the SW-06 allows two of the four switches to be combined to yield one SPDT switch. When the circuit is enabled (logic "1"), switch #1 is ON and #2 is OFF, allowing the input signal to pass through the switch. Upon receipt of a logic "0", switch #1 opens and at the same moment switch #2 is biased into an ON condition effectively grounding the input node of the amplifier. In stereo applications, the remaining two devices can be connected to make a second switch. In this case crosstalk between channels should remain below −90dB.

SCHEMATIC



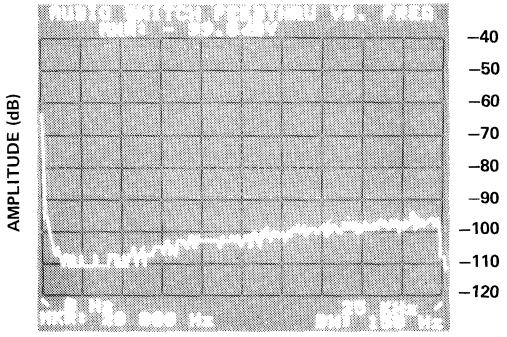
Two channels are shown for stereo applications.

DYNAMIC SWITCHING



True TTL compatibility is accomplished by the audio switch. The output returns to ground during logic "0".

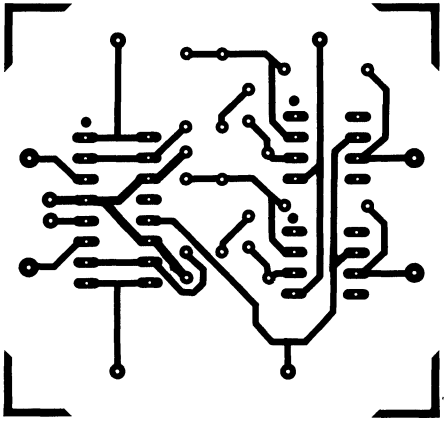
FEEDTHROUGH ATTENUATION RATIO

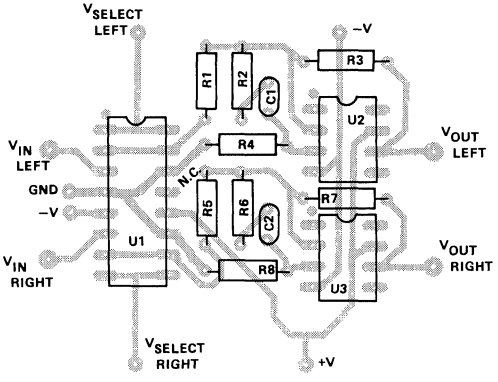


In the "OFF"state the audio switch input is swept and the output displayed on a high-resolution Audio Spectrum Analyzer. Vert. = 10dB/Div., Horz. = 0 to 25kHz, 2.5kHz/Div., 150Hz B.W.

AB-101

PRINTED CIRCUIT AND COMPONENT LAYOUT





P.C. board artwork and component layout are shown above. Good solid grounds should be employed as well as star grounding techniques. All supplies should be well bypassed with 0.1µF mono-caps and 10µF tantalums.

Parts List:

U1 — SW-06GP
U2, U3 — OP-37GP
R1, R3, R5, R7 — 6.8kΩ
R2, R6 — 1kΩ
R4, R8 — 3.3kΩ
C1, C2 — 680pF (mica)

Note: Artwork is not to scale.

AB-102

12-BIT 4 QUADRANT MULTIPLYING D/A CONVERTER

Precision Monolithics Inc.

APPLICATION BRIEF 102

FEATURES

- **4 Quadrant Multiplication — ±5V Analog Input Range, Offset Binary Coding, ±2.5V Analog Output Range**
- **Faster Settling Time Than CMOS Converters**
- **Accepts Differential, Inverting Single-Ended, or Noninverting Single-Ended Analog Input Voltages**

GENERAL DESCRIPTION

The transfer function of this circuit is:

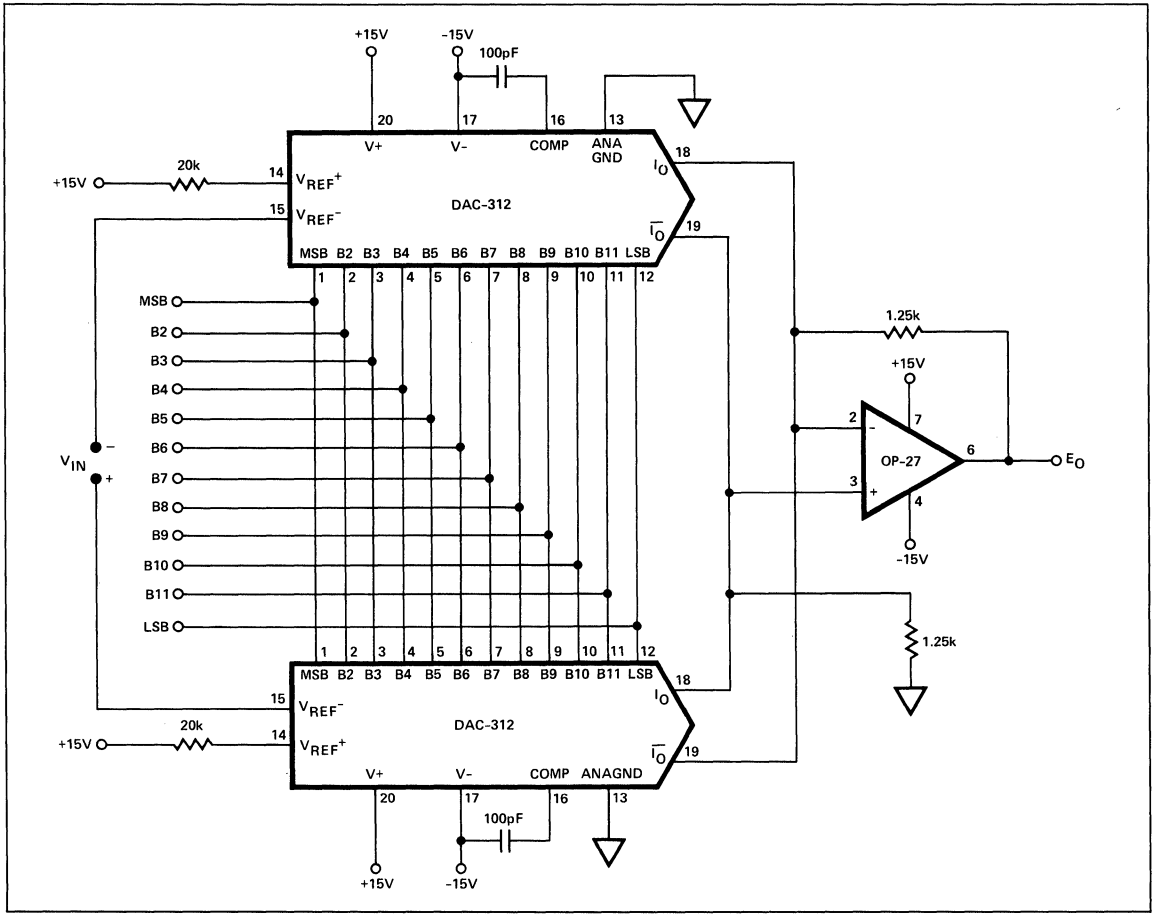
$$V_{OUT} = D \times \frac{(V_{IN+} - V_{IN-})}{2}$$

$$\text{where } D = \frac{\text{Digital Input Code}}{1111\ 1111\ 1111}$$

The circuit uses differentially cross-connected DAC-312 outputs driving a differential current to single-ended voltage converter. Current to voltage conversion is achieved using an OP-27 and two matched resistors.

For single-ended analog input voltages, connect the input signal to either the inverting or noninverting input, and ground the unused input.

4 QUADRANT MULTIPLYING D/A CONVERTER



AB-103

LOW-DRIFT MICROPOWER INSTRUMENTATION AMPLIFIER

Precision Monolithics Inc.

APPLICATION BRIEF 103

The MAT-04, followed by a programmable micropower op amp, is used to make an instrumentation amplifier that has very low power consumption. The MAT-04 monolithic quad is optimized for operation at only 10μA collector current. Gain is set by one resistor, R_0, and CMRR is primarily determined by the resistor matching of the R_1 and R_3 resistor sets.

To analyze the circuit, assume an input voltage of $V_{CM} + 1/2\ V_d$ at +IN and $V_{CM} - 1/2 V_d$ at -IN. This is a common-mode voltage of V_{CM} and a differential voltage of V_d. Defining I_2 as the current through each R_2, and I_3 as the current through each R_3, then summing currents at each side of R_0 yields:

$$\left(V_{CM} - \frac{1}{2}V_d - V_{BE}\right)\frac{1}{R_1} + I_3 = \frac{1}{R_0}V_d + I_2$$

$$\left(V_O - V_{CM} - \frac{1}{2}V_d + V_{BE}\right)\frac{1}{R_1} + I_2 = \frac{1}{R_0}V_d + I_3$$

Adding these two equations together results in:

$$V_O = \left(1 + \frac{2R_1}{R_0}\right)V_d$$

Gain is set by resistor R_0. If R_1 is 500kΩ and a gain range of 10 to 100 is needed, then R_0 would range from 110kΩ to 10.1kΩ. Input resistance is beta dependent and is given by:

$$R_{IN} = \beta\frac{2\,R_0\,R_1}{R_0 + 2R_1}$$

Collector currents are set by the R_4, R_5 divider and R_3. For example, a divider of 100kΩ, 100kΩ and a V- of -9V would result in a base voltage of approximately -4.5V. This would provide 3.9V if V_{BE} were 0.6V, thus an R_3 of approximately 390kΩ is needed to generate a collector current of 10μA. The common-mode variation does change the currents through the input pair, so common-mode range should be limited to about ±1V.

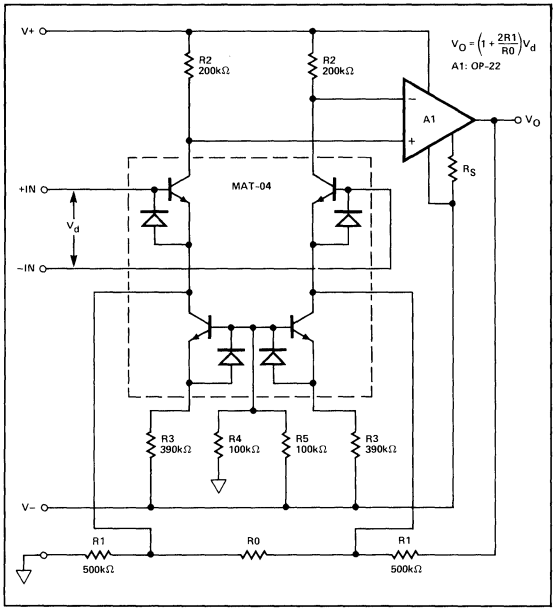
The amplifier can be designed to operate with ±15V supply; the voltage divider resistor R_5 should be changed to 230kΩ.

CMRR is primarily a function of the matching of the R_1 pair and R_2 pair, although input transistor dynamic emitter resistance also is a factor. Neglecting second-order effects, the CMRR is approximately:

$$CMRR \simeq \frac{A_d}{\frac{\Delta r_E}{R_1}A_d + \frac{\Delta R_1}{R_1} + \frac{\Delta R_2}{R_2}}$$

where A_d is the differential gain $(1 + 2R_1/R_0)$. CMRR of over 100dB is achievable for gains of 10 to 1000 by trimming the ratio of the two R_1 resistors. The maximum input voltage of the OP-22 needs to be at least 1.5V below the positive supply. If we choose to have a nominal value of 2V across the R_2 resistors, then $R_2 = 2V/10\mu A = 200k\Omega$. To operate the OP-22 at 20μA supply current, make R_S approximately 12MΩ. Total supply drain is nominally 40μA when operating at ±9V.

This circuit has the advantages of very low input offset voltage drift, low power consumption, and a practical gain range of 10 to 1000. Frequency response is easily varied by trimming of R_S.



PMI

AB-104

SINGLE-SUPPLY MICROPOWER INSTRUMENTATION AMPLIFIER

Precision Monolithics Inc.

APPLICATION BRIEF 104

The OP-220 dual op amp has a wide input voltage range and operates from very low supply currents (125μA max at 5V for OP-220B/F). These characteristics, combined with low input offset voltage drift and high open-loop gain, make the OP-220 ideal for use in this single-supply, two-op-amp instrumentation amplifier.

Consider an input of V_{CM} −1/2 V_d at the −IN terminal and V_{CM} +1/2 V_d at the +IN terminal. This corresponds to a common-mode input V_{CM} and a differential input of V_d. The currents at the inverting input of each op amp can be summed to form two equations:

$$\left(V_B - V_{CM} + \frac{1}{2}V_d\right)\frac{1}{2R_1} + \frac{V_d}{R_0} + \left(V_1 - V_{CM} + \frac{1}{2}V_d\right)\frac{1}{R_1}$$

$$= \left(V_{CM} - \frac{1}{2}V_d\right)\frac{1}{2R_1}$$

$$\left(V_1 - V_{CM} - \frac{1}{2}V_d\right)\frac{1}{R_1} + \left(V_O - V_{CM} - \frac{1}{2}V_d\right)\frac{1}{R_1} = \frac{V_d}{R_0}$$

Combining these two equations gives

$$V_O = 2\left(1 + \frac{R_1}{R_0}\right)V_d + \frac{1}{2}V_B$$

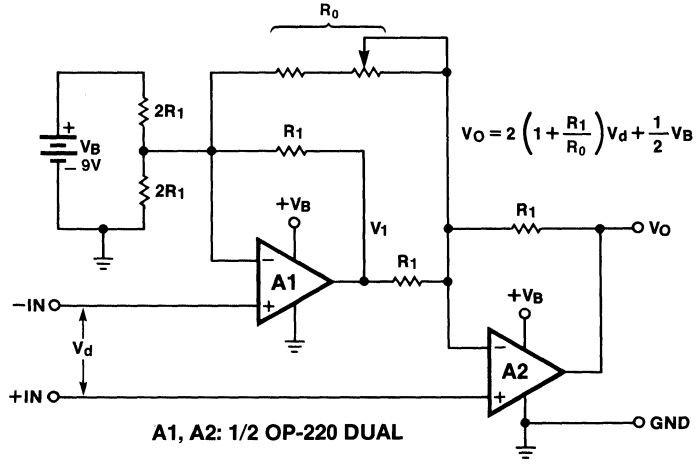
The common-mode input (V_{CM}) has been rejected. The differential gain is adjustable by varying the single resistor R_0. Matching the R_1 resistors assures high CMRR.

The OP-220 has an input range that goes from negative supply to within 1.5V of positive rail, and an output range of approximately 0.8V from the negative rail to within 1.0V of the positive rail. Operating from a 9V battery (assume 8V minimum), then an input range of zero to 6V is easily accommodated. The outputs of both A1 and A2 must be kept within their linear range (1V to 6V is conservative).

$$V_1 = -\left(1 + \frac{R_1}{R_0}\right)V_d - \frac{V_B}{2} + 2V_{CM},\ 1V \le V_1 \le 6V$$

$$V_O = 2\left(1 + \frac{R_1}{R_0}\right)V_d + \frac{1}{2}V_B,\ 1V \le V_O \le 6V$$

A value of 100kΩ is recommended for R_1. A gain range of 1 to 1000 is practical for this circuit. Using the OP-220E, supply current will be less than 122μA at 25°C. This instrumentation amplifier offers a wide gain range, low power consumption, and single-supply operation. Slew-rate is approximately 0.04V/μs; the OP-221 is recommended for the same circuit if higher speed is needed.



A1, A2: 1/2 OP-220 DUAL

AB-105

LOW INPUT-CURRENT OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

APPLICATION BRIEF 105

A low-current JFET dual combined with an OP-22 programmable micropower op amp provides exceptionally low input bias current, high open-loop gain, and very low power consumption. This simple circuit is ideal for high gain, inverting-mode operation where very low input currents are converted to a voltage. Battery operation is practical; quiescent current drain is approximately 80μA when operating from ±9V and with R_S = 12MΩ. Performance is comparable to many electrometer and picoammeter instruments.

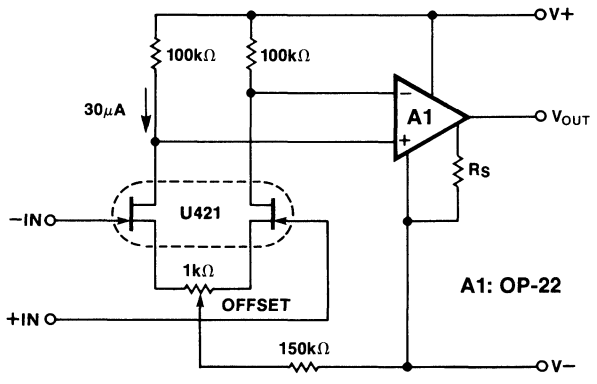
The Siliconix U421 used for the input stage is optimized for operation at drain currents of 30μA. The input gate current with I_D of 30μA and V_{DG} of 10V is a maximum of 0.1pA for the U421. Assuming ±9V supplies, the source resistor needs to be about 9V/60μA = 150kΩ to have 30μA per side. The drop from positive supply to op amp inputs needs to be at least 1.5V; drain resistors of 100kΩ provide 3V drop at I_D of 30μA. Input stage gain is approximately $g_{fs} \times R_D$, which for the U421 is 200μmho × 100kΩ = 20, or 26dB.

The OP-22 is operated with R_S of 12MΩ to obtain a set current of 1.4μA. This sets the quiescent supply current to approximately 20μA. The wide input range, low offset current, low offset voltage, and high gain of the OP-22 are valuable characteristics for this circuit.

The high gain of this circuit causes phase margin to be low, so some form of compensation is generally needed for operation at low closed-loop gains. Stability can be enhanced by reducing the supply current of the OP-22 or by adding an RC network across the inputs. Also, the common-mode input range must be limited to ±1V to avoid modulation of the drain currents. Common-mode range can easily be extended by adding some sort of constant current source.

The amplifier can operate to ±15V supply. At this voltage, the input stage operates at about 50μA per side. If the 30μA operating current is to be retained, the 150kΩ source resistor should be increased to 250kΩ.

This straight-forward circuit has less than 1pA input bias current, very high open-loop gain (over 120dB), and low quiescent supply drain (80μA at V_S = ±9V, R_S = 12MΩ). These features are particularly useful for electrometer circuits where very small currents must be accurately amplified.



PMI

AB-106
TRANSIMPEDANCE AMPLIFIER

Precision Monolithics Inc.

APPLICATION BRIEF 106

Accurate measurement of very low currents is a challenging instrumentation problem. Insulation testers, capacitor leakage test instruments, and pH meters all need amplifiers that can accurately convert currents from the sub-picoamp level to a DC voltage. This circuit, using a siliconix U421 JFET dual for the input stage, achieves less than 2pA input bias current. Input current noise is very low. The OP-22 second stage provides high gain at a very low quiescent current. Current-sensing amplifiers often need protection at the input, but conventional diodes have far more leakage than the input FET pair. The solution is to use two low-leakage JFETs connected as diodes across the op amp input. The Siliconix DPAD series provides two FET diodes in a single package with leakages as low as 1pA at 20V.

A divider circuit at the output is used to raise the closed-loop gain. The feedback is attenuated by a factor β which is $R_2/(R_1+R_2)$. If R_2 is much less than R_1, then the output V_O will be:

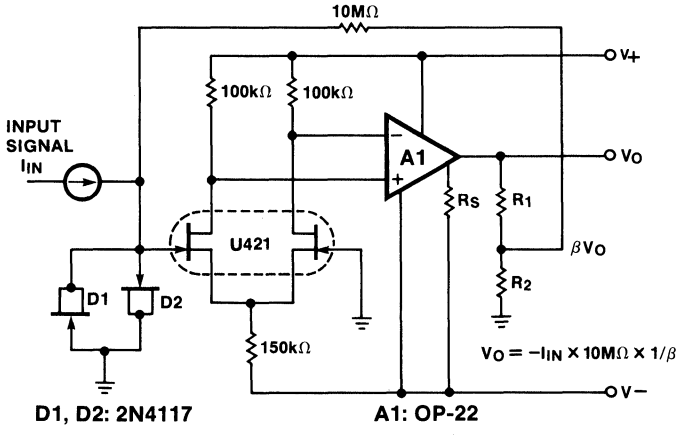
$$V_O = -I_{IN} \times 10M\Omega \times \frac{1}{\beta}$$

Typical values would be 10kΩ for R_2 and 90kΩ for R_1 to obtain a gain of 10. The output would then be:

$$V_O = -I_{IN} \times 10^8\Omega$$

A −1V output would correspond to an input of 1nA.

Quiescent current of the OP-22 is set by the external resistor R_S. A value of 12MΩ will set the current at about 1.4μA when operating from ±9V supplies, and this will result in approximately 20μA of supply drain for the OP-22. The amplifier also works well at a supply voltage of ±15V. Slew-rate and quiescent current can be traded off; the 20μA supply current corresponds to a slew-rate of approximately 0.005V/μs. A range of 3MΩ to 33MΩ is practical for R_S.



AB-107

TWO-WIRE, 4-20mA CURRENT TRANSMITTER

Precision Monolithics Inc.

APPLICATION BRIEF 107

This two-wire current transmitter provides an output of 4mA to 20mA that is proportional to an input voltage V_{IN} plus an offset. Current loops are particularly useful in process control systems where remote analog signal conditioners must be interfaced to a central location. The loop can be powered by an inexpensive, unregulated DC voltage. The low supply current needs of the OP-22 programmable op amp and REF-02 bandgap reference allow for "floating" operation. The transmitter circuit uses less than 2mA and can therefore supply up to 2mA at 5V as a transducer reference or bridge supply without exceeding the minimum loop current of 4mA. The OP-22 and REF-02 can be operated over a wide supply range. With a load resistor R_L of 50Ω and a sense resistor R_S of 100Ω, the maximum voltage from Ground to Signal Common is 150Ω × 20mA, or 3V. The REF-02 minimum limit is 7V, therefore V_S needs to be above 10V.

The OP-22 regulates the output I_O to satisfy the current summation at the noninverting mode:

$$\frac{V_{IN}}{R_1} + \frac{5V}{R_2} - \frac{I_O R_S}{R_3} = 0$$

$$I_O = \frac{1}{R_S}\left(\frac{R_3}{R_1} V_{IN} + \frac{R_3}{R_2} 5V\right)$$

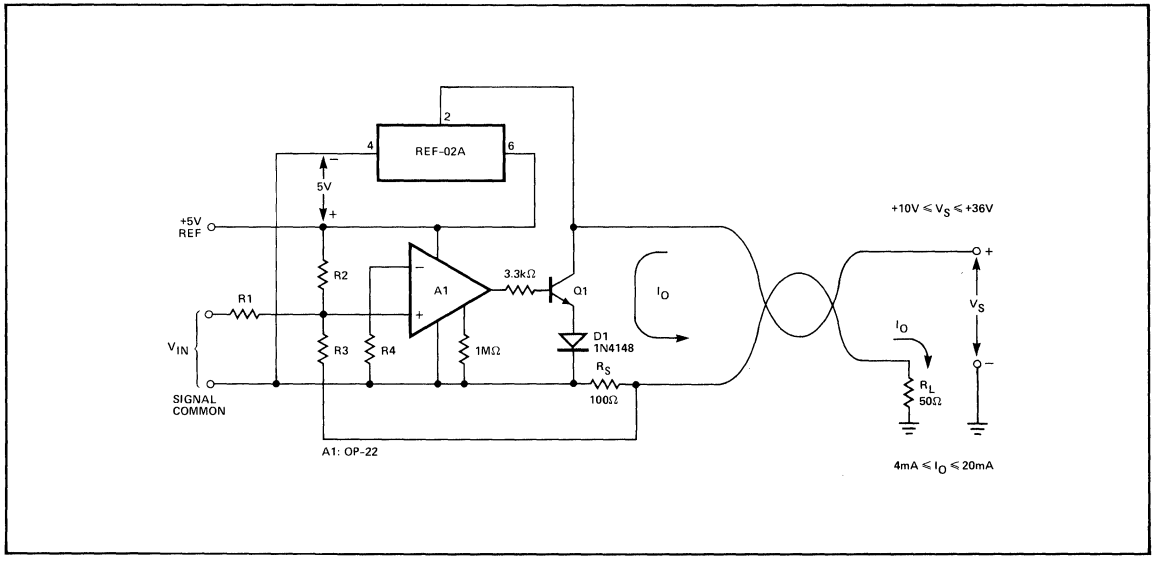
As a design example, consider a system need for:

$$I_O = \frac{16V_{IN}}{100\Omega} + 4mA$$

This would provide an output span of 4mA to 20mA for an input range of zero to 100mV. This requires a ratio of 16 for R_3/R_1, and a ratio of 0.08 for R_3/R_2. Choosing R_1 to be 5kΩ, then we need $R_3 = 80k\Omega$ and $R_2 = 1M\Omega$. Drift due to input bias current of the OP-22 can be minimized by making R_4 equal to the parallel combination of R_1, R_2, and R_3.

Designing for other input ranges or other values of R_S and R_L is straightforward. The sense resistor R_S does have an upper limit that is not obvious; the voltage drop across R_S at turn-on can pull the OP-22 noninverting input negative relative to its own negative supply rail. This can cause the OP-22 op amp output to go for the positive limit which drives Q1 into saturation and a possible latching condition. This is prevented by limiting the negative voltage at the noninverting input or by limiting the maximum drop across R_S.

This current transmitter has excellent linearity, operates well with very low supply currents, and is easily adaptable to a wide range of input signal levels.



AB-108

A MICROPOWER SINGLE-SUPPLY PRECISION RECTIFIER

Precision Monolithics Inc.

APPLICATION BRIEF 108

This precision full-wave rectifier circuit accepts AC inputs of up to ±3V, yet operates from a single +5V supply voltage. Quiescent supply drain is only 320μA. Rectifier gain is unity with the gain accuracy almost entirely dependent on the match between resistors $2R_1$ and $2R_1$. Frequency range is approximately DC to 2kHz. The single supply operation at very low, quiescent current drain makes this circuit particularly useful for battery-powered equipment.

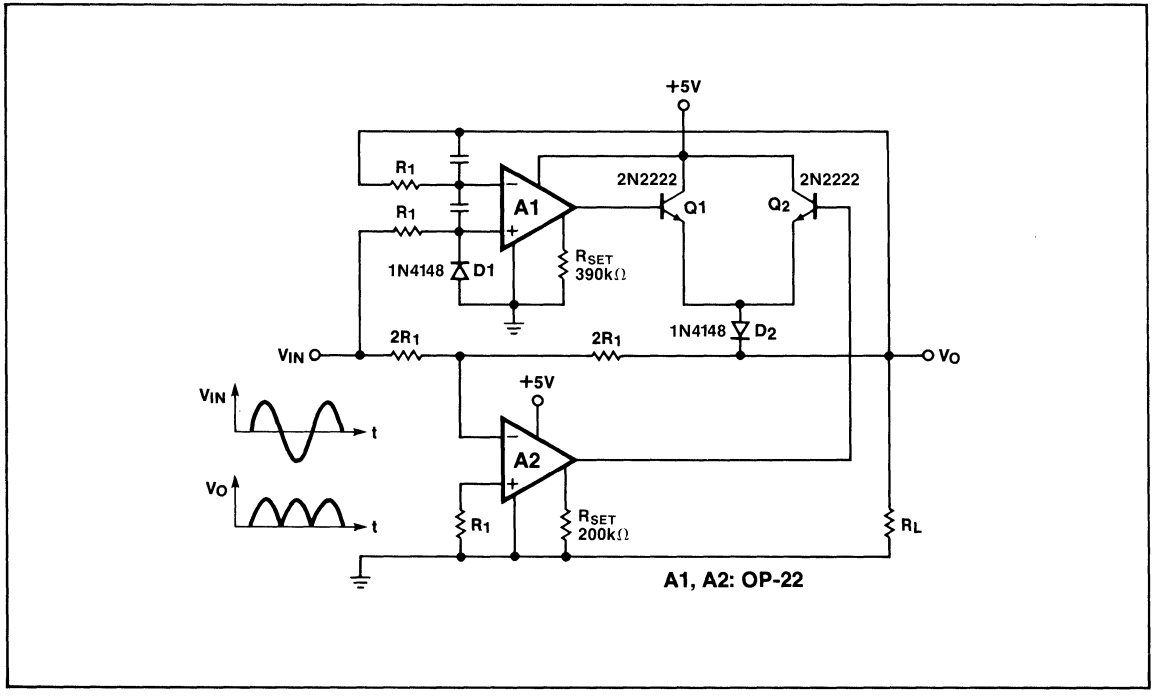
For positive input voltage ($V_{IN} > 0$), A1 will drive Q1 and D2 to make the output voltage V_O equal to the input voltage. Output swing at V_O is approximately three diode drops below the supply voltage, thus the peak output voltage is near +3V. Amplifier A2 output goes to negative saturation, which is approximately +0.8V, and Q2 will therefore be back-biased and OFF.

For negative input voltage ($V_{IN} < 0$), A1 output goes into negative saturation and Q1 is thereby gated OFF. Amplifier A2 will serve as a unity-gain inverter. Since V_O will be equal to V_{IN} in magnitude, but opposite in polarity, V_O will be equal to the absolute value of V_{IN}.

Quiescent current drain is determined by the set current I_{SET}. With a 5V supply the set current will be $3.7V/R_{SET}$. Slew rate and bandwidth vary directly with the set current. Amplifier A1 essentially operates with unity-gain feedback, while A2 operates with a feedback gain of 0.5. The closed-loop gain-bandwidth is therefore made equal, and the frequency response symmetrical, by making the set current of A2 twice that of A1. Amplifier A2 has a set current of 3.7V/200k, which is 18.5μA, and amplifier A1 has a set current of 3.7V/390k, which is 9.5μA. These set currents will result in quiescent currents of 100μA for amplifier A1 and 220μA for amplifier A2.

The OP-22 input stage is a PNP Darlington, thus a negative input voltage can forward bias the collector-base junction of the input transistor. This potential problem is prevented by adding resistor R1 and diode D1 at the A1 input to limit the negative input voltage.

This simple circuit provides precise, unity-gain rectification of AC signals of up to ±3V in the frequency range of DC to 2kHz. It operates from a single +5V supply voltage with quiescent current drain of only 320μA.



AB-109
HIGH SPEED PRECISION RECTIFIER

Precision Monolithics Inc.

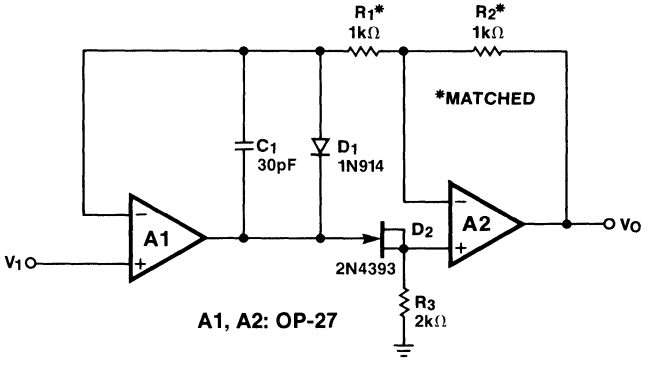
APPLICATION BRIEF 109

The low offsets and excellent load driving capability of the OP-27 are key advantages in this precision rectifier circuit. The summing impedances can be as low as 1KΩ which helps to reduce the effects of stray capacitance.

For positive inputs, D2 conducts and D1 is biased OFF. Amplifiers A1 and A2 act as a follower with output-to-input feedback and the R1 resistors are not critical. For negative inputs, D1 conducts and D2 is biased OFF. A1 acts as a follower and A2 serves as a precision inverter. In this mode, matching of the two R_1 resistors is critical to gain accuracy.

Typical component values are 30pF for C_1 and 2kΩ for R_3. The drop across D1 must be less than the drop across the FET diode D2. A 1N914 for D1 and a 2N4393 for the JFET were used successfully.

The circuit provides full-wave rectification for inputs of up to ±10V and up to 20kHz in frequency. To assure frequency stability, be sure to decouple the power supply inputs and minimize any capacitive loading. An OP-227, which is two OP-27 amplifiers in a single package, can be used to improve packaging density.



AB-110
LOGARITHMIC CONVERTER

Precision Monolithics Inc.

APPLICATION BRIEF 110

The logarithmic relationship between the collector current and base-emitter voltage of a transistor is used to obtain logarithmic signal compression. The MAT-02 monolithic transistor pair has excellent matching and logarithmic characteristics. Amplifiers A1 and A2 need low input bias currents, so the FET-input OP-41 is recommended.

Collector current I_1 is V_1/R_1 and collector current I_2 is V_R/R_2. The voltage at the base of Q2 is V_O attenuated by the R_3, R_4 divider. The output voltage V_O is

$$V_O = \frac{R_3 + R_4}{R_4} (V_{BE2} - V_{BE1})$$

For matched transistors,

$$\Delta V_{BE} = \frac{kT}{q} \ln \left[\frac{I_1}{I_2} \right]$$

where k is Boltzman's constant, T is temperature, and q is the charge of an electron. Therefore;

$$V_O = \frac{kT}{q} \left[\frac{R_3 + R_4}{R_4} \right] \left[\ln \frac{V_1}{V_R} \frac{R_2}{R_1} \right]$$

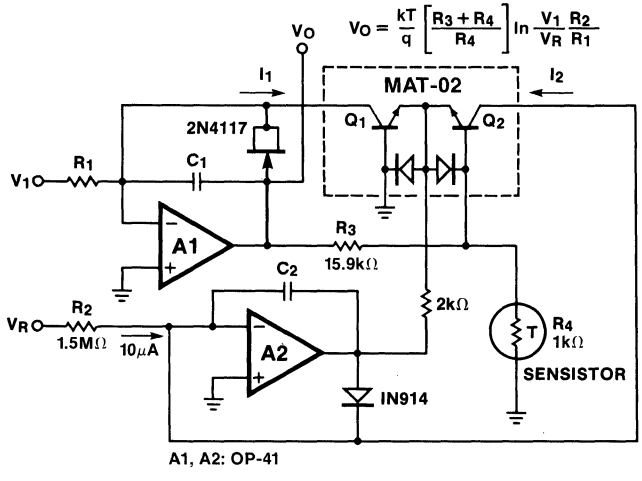
The R_3, R_4 divider sets the gain and the current V_R/R_2 sets the zero.

If a regulated 15V supply is available for V_R, then just make R_2 a 1.5MΩ resistor and I_2 will then be 10μA. A divider of 15.9kΩ for R_3 and 1kΩ for R_4 will provide gain of 16.9. Since kT/q is approximately 25.7mV at 25°C, a gain of 16.9 will provide a scale factor of 1V/decade. This scale factor varies directly with temperature, but a temperature-sensitive resistor in the R_4 position can approximately cancel this known drift if it has a positive coefficient of +0.35%/°C. These component values provide a temperature-compensated output of

$$V_O = 1V \times \log_{10} \left(\frac{V_1}{R_1} \frac{1}{10\mu A} \right)$$

The output is zero for an input current of 10μA, and it varies in logarithmic fashion by 1V/decade about this zero.

Frequency compensation is difficult to analyze due to the transistor being in the feedback loop. Typical values for C_1 and C_2 are in the 50pF to 250pF range. This amplifier configuration is very versatile and can easily be adapted to a wide range of log converter applications. A range of three to four decades is easily obtained and up to six decades is feasible if the amplifier offsets are trimmed and the temperature range is limited.



A1, A2: OP-41

AB-111
SINGLE-SUPPLY WIEN-BRIDGE OSCILLATOR

Precision Monolithics Inc.

APPLICATION BRIEF 111

Wien-bridge oscillators have the advantage of requiring only one op amp, and this advantage is particularly important for battery-operated applications. This oscillator circuit operates from a single 9V battery.

The conditions for Wien-bridge oscillation are

$1 - R_1 R_2 C_1 C_2 \omega_O^2 = 0$ and

$$\frac{R_2 C_1}{R_1 C_1 + R_2 C_2 + R_2 C_1} = \beta$$

where β is the ratio of output voltage feedback to the inverting input. If $R_1 = R_2$ and $C_1 = C_2$, then ω_O is 1/RC and β is 1/3.

This oscillator should be set to just diverge in amplitude. Diodes are used to obtain a nonlinear feedback characteristic which will limit the divergence without causing too much distortion. The condition for oscillation is

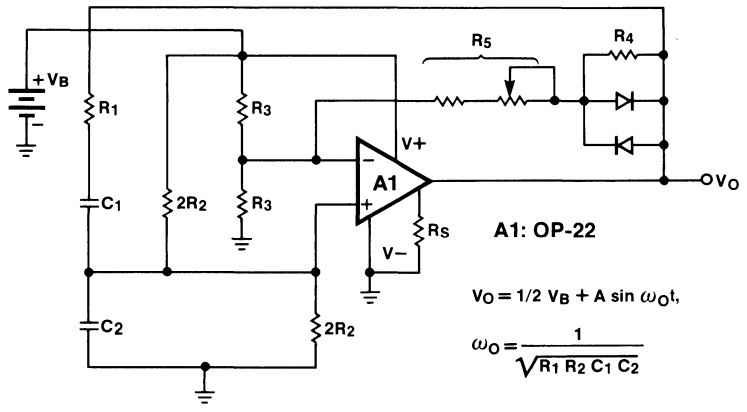
$$\frac{R_3}{R_3 + 2\,(R_5 + R_4')} = \frac{1}{3}, \quad R_4' = \text{Parallel combination of } R_4 \text{ and diodes}$$

As a design example, consider

$C_1 = C_2 = 0.01\mu F$	$R_4 = 10k\Omega$
$R_1 = 15.8k\Omega$	$R_5 = 40k\Omega$ nominally
$2R_2 = 31.8$	Diodes = 1N914 or 1N4148
$R_3 = 50k\Omega$	$R_S = 1M\Omega$

Using these component values, f_O will be 1004Hz. Resistor R_5 must be adjusted for best amplitude stability. If R_5 is too low, the oscillation might converge; if too large, then the oscillation will diverge until the output clips. An oscillation output of 6V peak-to-peak when operating from a 9V battery is recommended. Resistor R_5 needs to be a nominal 40kΩ with a ±2.5kΩ adjustment range.

The OP-22 is operated with a 1MΩ set resistor for a set current of 7.8μA which corresponds to a supply current of approximately 100μA. Gain-bandwidth product and slew-rate vary directly with the set current, so R_S should be optimized for the specific oscillation frequency. Supply drain can be reduced for lower frequencies. The OP-22 works well for frequencies in the range of 100Hz to 1kHz; the OP-27 is recommended for higher frequencies.



AB-112

SINGLE-RESISTOR CONTROLS WIEN-BRIDGE OSCILLATOR FREQUENCY

Precision Monolithics Inc.

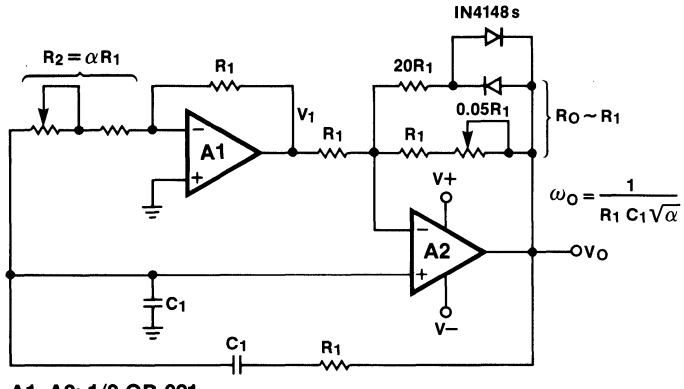
APPLICATION BRIEF 112

Frequency control can be added to the conventional Wien-bridge circuit by adding an op amp inverter (A1 in the diagram). The low-power OP-221 dual works well in this circuit. Center frequency ω_O is $1/R_1 C_1$ multiplied by a variable term $1/\sqrt{\alpha}$. The inverter gain is $1/\alpha$, where α is nominally unity.

The center frequency is given by

$$\omega_O = \frac{1}{R_1 C_1 \sqrt{\alpha}}$$

This circuit adds tuning capability to the Wien-bridge oscillator circuit.



A1, A2: 1/2 OP-221

PMI

AB-113
PRECISION RAMP GENERATOR

Precision Monolithics Inc.

APPLICATION BRIEF 113

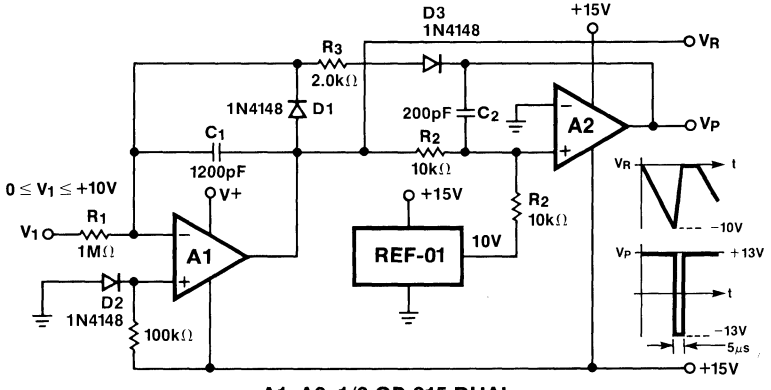
Precision ramps with well-controlled repetition rate and amplitude are generated by this circuit. Repetition rate is controlled by a DC input voltage (V_1). This circuit can also be used as a simple voltage-to-frequency converter over a limited input range.

Just after resetting, the A1 op amp generates a negative ramp with a slope proportional to I_1, which is $(V_1 - V_{D2})/R_1$. The slope is $-C_1 dV_R/dt$ and the A2 output is sitting at the positive limit. When the A1 output reaches −10V, the output of A2 flips to the negative limit. This transition is given regenerative action through capacitor C_2. The negative pulse from A2 discharges C_1 through diode D3 and drives it positive until diode D1 conducts. Since D2 sets the A1 inputs to −0.6V and D1 has an equal drop when it conducts, the integrator will be reset to zero volts. After the integrator reaches zero volts and C_2 has discharged, amplifier A2 flips back to positive saturation and D3 is again back-biased. A key feature of this circuit is the amplitude stability; the REF-01 output of +10V is very stable and the reset zero is temperature compensated by the matching of D1 and D2. Thus the ramp amplitude of 10V is very accurate and stable over a wide range of operating conditions.

Exact circuit values and op amp choices depend on the desired operating range. For a range of 10Hz to 1kHz, the OP-215 can be used with the following values:

$R_1 = 1M\Omega$
$C_1 = 1200pF$
$R_2 = 10k\Omega$
$R_3 = 2.0k\Omega$
$C_2 = 200pF$

With these component values and using the OP-215 dual, we will have a reset time interval of approximately 5μs. The minimum ramp interval, assuming a maximum input voltage of 11.4V and 0.6V diode drop, is 1200pF × 10V/12μA = 1msec which corresponds to a 1kHz repetition rate. The ramp amplitude of zero to −10V is very accurate and stable over a range of 10Hz to 1kHz. The output of A2 is a 5μs pulse of approximately ±13V amplitude.



A1, A2: 1/2 OP-215 DUAL

PMI

AB-114
PRECISION CURRENT REGULATOR

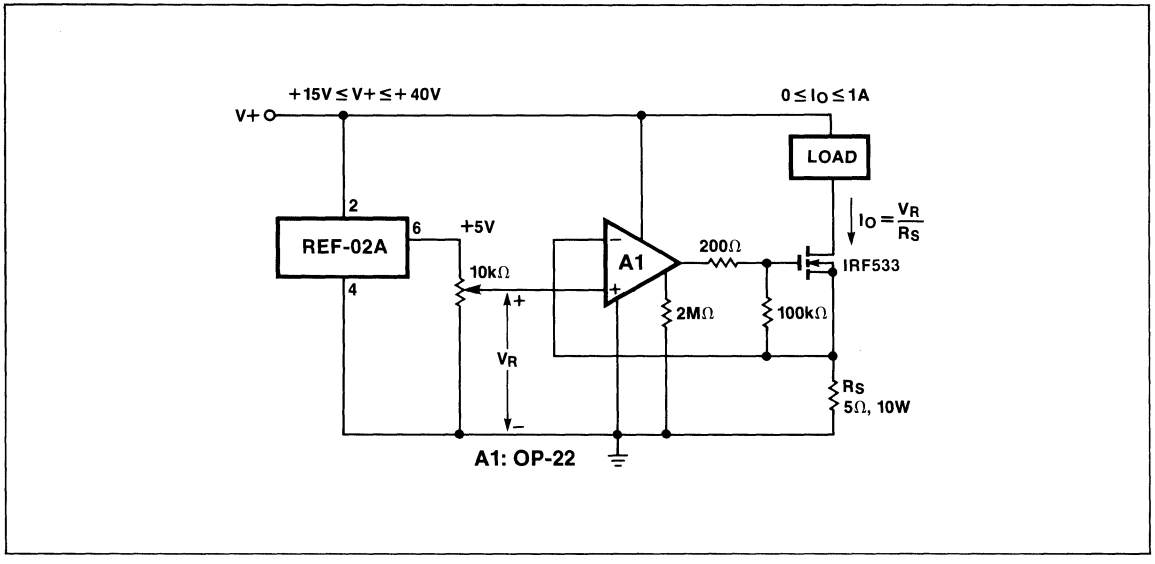
Precision Monolithics Inc.

APPLICATION BRIEF 114

The wide input and output voltage range of the OP-22 programmable micropower op amp is very useful for driving power MOSFET devices. This simple circuit provides a very stable and accurate current source that operates over a range of 15V to 40V and up to 1A of current. The REF-02 and OP-22 both operate from the +15V to +40V supply voltage. The REF-02 output is a stable +5V that is divided down to drive the input voltage (V_R) to the current amplifier. The op amp drives the power MOSFET to make $I_O R_S = V_R$. A sense resistor of 5Ω provides a range of zero to 1A for an input range of zero to +5V. The high open-loop gain assures excellent current regulation.

While the nominal V_{GS} for the IRF533 is 2V to 4V and the OP-22 output will go to within 1.5V of the negative rail, there is a possible difficulty in swinging low enough at the OP-22 output to assure cut-off of the IRF533 over the full temperature range. Selecting the power MOSFET for minimum V_{GS} of 2V over the temperature range will provide a good safety margin. In any case, the IRF533 will require an adequate heat sink if operated over the full zero to 1A range.

The 200Ω resistor should be located near the gate; its purpose is to prevent any spurious parasitic oscillations in the power FET. The 100kΩ resistor is non-critical and just serves as a resistive load in parallel with the gate-to-source capacitance. If desired, a signal source can be used in place of the REF-02 to dynamically control I_O. Slew-rate is approximately 0.07V/μs at 20V supply voltage. Also, other power FET devices can be used in this circuit and other current ranges accommodated by simply changing the sense resistor R_S as needed.



Most bandgap references require at least 1mA of quiescent operating current. This circuit takes advantage of a PMI programmable micropower op amp, the OP-22, which provides high gain even at low quiescent currents. It has a further advantage of wide supply voltage range. Total quiescent current for this 1.23V reference is only 20μA and the input voltage range is +3V to +30V.

A bandgap reference is generated by summing a V_{BE} drop that has a negative tempco with a fraction of a ΔV_{BE} that has a positive tempco. The summation that gives zero tempco is the energy bandgap of silicon (1.205V) plus kT/q (~25mV at 25°C) for a total of 1.230V. This varies slightly with processing, but the zero tempco point will be very close to 1.23V.

In this circuit, a ΔV_{BE} is generated by the imbalance in collector resistance.

$$\Delta V_{BE} = \frac{kT}{q} \ln \frac{I_{C1}}{I_{C2}}$$

$$= 25.7\text{mV} \times \ln \frac{R_2}{R_1}$$

$$= 25.7\text{mV} \times \ln \frac{2.2\text{M}}{360\text{k}\Omega}$$

$$= 46.5\text{mV at } 25°\text{C}$$

The ΔV_{BE} is impressed across R_3, a 68kΩ resistor, and the resulting current of 0.684μA is summed with I_{C1}. This total current I_T is

$$I_T = I_{C1} + \frac{1}{R_3} \Delta V_{BE}$$

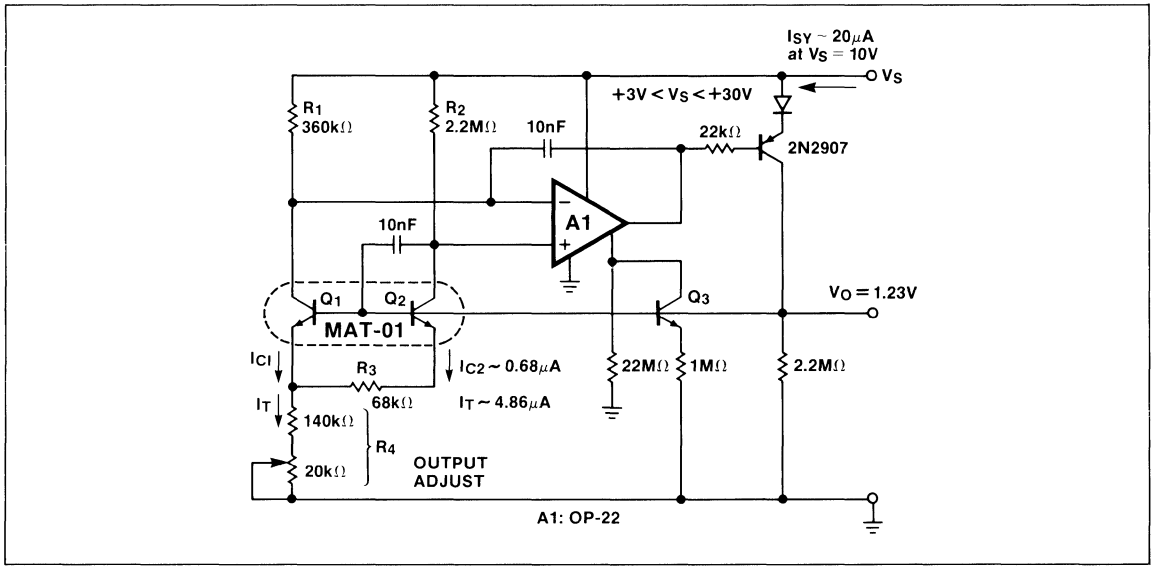
$$= \frac{\Delta V_{BE}}{R_3} \times \frac{R_1 + R_2}{R_1}$$

$$= 4.863\mu\text{A}$$

This current across a nominal 150kΩ for R_4 causes a voltage of 729mV. This 729mV adds to a V_{BE} of 500mV to generate the desired total of 1.230V at the base of Q1. Tempco of this 1.230V bandgap output will be low, typically 20ppm/°C over a 0°C to 70°C range.

The OP-22 op amp, followed by a 2N2907 PNP transistor, makes the collector voltages of Q1 and Q2 equal and regulates the output voltage. Line regulation is approximately 0.01%/V and load regulation is 0.001%/mA. Quiescent current for the OP-22 is set by the Q3 constant-current source. Set current for the OP-22 is 0.73V/1M which corresponds to a quiescent supply current of approximately 7μA to 12μA over the supply range of +3V to +30V.

This bandgap reference provides excellent stability and regulation at very low quiescent operating current, approximately 20μA at a 10V supply level.



PMI

AN-6

A LOW-COST, HIGH-PERFORMANCE TRACKING A/D CONVERTER

Precision Monolithics Inc.

APPLICATION NOTE 6

INTRODUCTION

The availability of low-cost IC D/A converters, comparators and up/down counters makes possible construction of tracking A/D converters having high performance and reliability despite their small size and low cost. These A/D converters are suitable for a wide range of applications such as transducer and audio digitizing, infinite sample and holds, and servo-control loops. This paper describes an 8-bit tracking A/D converter that can be built using Precision Monolithics, Inc., DAC-100 CCQ3 D/A converter, CMP-01CJ Fast Precision Comparator and 4-bit MSI up/down counters.

TYPES OF A/D CONVERTERS

There are several popular styles of A/D converters (ADC) based on using a D/A converter in a feedback configuration. The three most common are: ramp or count-up, tracking or servo, and successive approximation.

Ramp types produce one conversion per each 2^N clock counts for an "N" bit converter and are suitable only for very slowly changing analog data; additionally, the data can be taken out only at the end of the conversion period. Successive approximation types are quite fast, requiring only "N + 1" clock counts for conversion. They are capable of encoding fast-moving analog signals if an external sample-and-hold circuit is used to stop the analog data; again, the digital output is true only at the end of the conversion period.

For many applications, tracking ADCs can provide adequate speed while costing approximately the same as simple ramp types. Additional advantages are that no sample-and-hold circuit is required and that the digital data is continuously available at the output.

BASIC OPERATION

The tracking A/D is a relatively simple system, both in concept and in practice. The basic design requires three major elements: an up/down counter, a current output D/A converter, and a voltage comparator (see Figure 1). The voltage at the comparator's input will be the result of the analog input voltage minus the DAC output sink current times R_{IN} ($V_O = V_{IN} - I_1 \cdot R_{IN}$). Assuming a perfect comparator, if the output voltage (V_O) is above ground, the comparator's output will be low, causing the up/down counter to increase the DAC's output sink current by one LSB. (The counter actually counts down one count; this results from the DAC's utilization of complementary logic, i.e., an all-zero input produces maximum DAC output current.) The comparator continues to examine the voltage for polarity, and always drives the counter's code in the direction which causes the output voltage to approach zero. Once a balance is achieved, the loop is "locked," and tracks the analog input signal so long as the loop slew rate is not exceeded. When the loop is balanced, the converter's output is the binary-coded equivalent of the analog input.

When encoding a DC input signal, the digital output will "dither" or alternate between the two adjacent states which span the theoretically correct output value. This is of little consequence as all A/D converters have a similar error, known as the "quantizing" error.

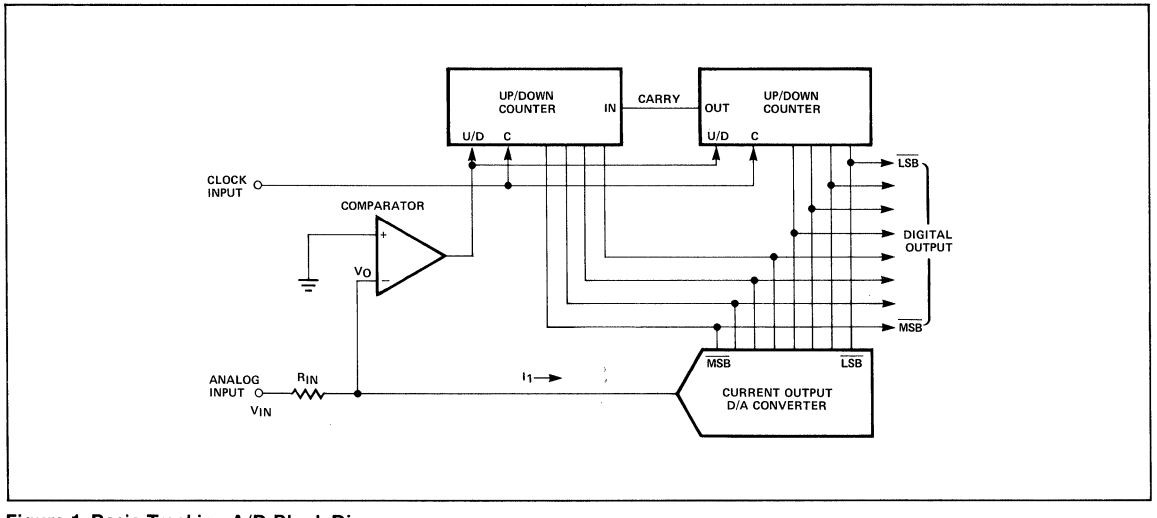


Figure 1. Basic Tracking A/D Block Diagram

In the actual circuit design, a "type-D" flip-flop is inserted between the comparator and the counter's up/down input. This is to insure adequate set-up time between the comparator's output change and the counter's next stage change.

Loop timing can be seen in Figure 2. After the positive clock transition, the counter changes to its next state and drives the DAC to its new output. After the DAC has settled and the comparator has come to its final state, the next positive clock transition loads the comparator's new state into the flip-flop and the cycle repeats.

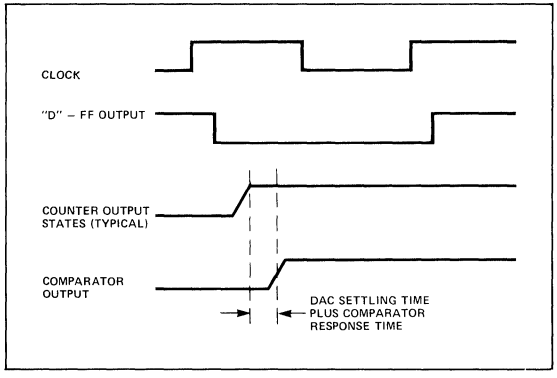


Figure 2. System Timing Diagram

FINAL CIRCUIT DESIGN

The completed 8-bit tracking A/D design is shown in Figure 3. The digital output is available in complemented form, as the DAC-100 utilizes complementary logic. Diode clamps insure the DAC output remains near zero despite input and turn-on transients. For this 8-bit design, the two least significant bit inputs of the 10-bit DAC are not required and are connected to +5V, thus turning them off. Diodes are also used to insure that a positive voltage is applied to the V+ pin (Pin 14) as soon as the +5V supply comes up. The clock, although extremely simple, is quite stable over a wide range of temperatures and supply voltages. Several layouts were tried, with no perceptible differences in performance.

TRIMMING

The circuit requires only one trimming operation. The full-scale output current of the DAC is adjusted to produce proper encoding at full scale input. Although several schemes are possible, the simplest is to place +10.0V at the input, and trim the 200Ω Full Scale Adjust pot to produce a low output at the seven most significant bits with the LSB alternating states (dithering) at the clock frequency.

VOLTAGE OUTPUT APPLICATIONS

The basic tracking A/D uses a "current-comparison" technique; the analog voltage is not reconstructed at the comparator's input, thus eliminating the need for an op amp to convert the DAC-100's current output to a voltage. For applications such as infinite (no-droop) analog sample-and-hold circuits, the OP-01CJ, a low-cost, fast slewing, fast settling op amp with internal compensation can be added as in Figure 4. This configuration also provides very high input impedances, without requiring an extra buffer amplifier. The reconstructed analog voltage is available at the output of the op amp; gating the counter "off" stores the data in analog form.

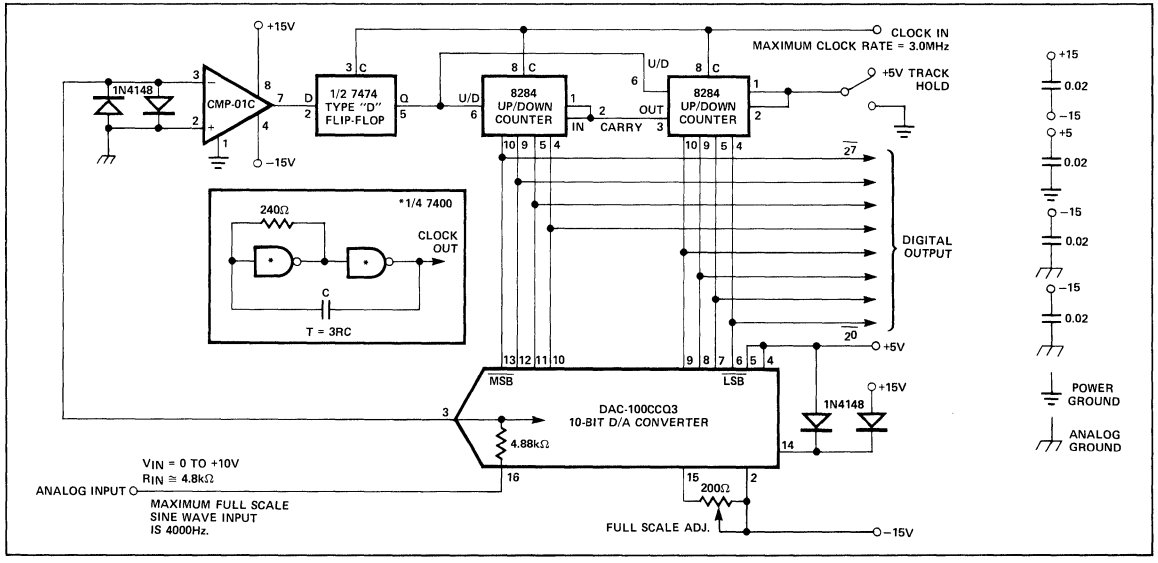


Figure 3. Complete Schematic — 8-Bit Tracking A/D Converter

BIPOLAR OPERATION

Bipolar operation (±5V) can be obtained by injecting a current equal to 1/2 the full scale current into the DAC-100 sum line. This can be accomplished by applying +6.4V to the internal bipolar resistor of the DAC-100 (Pin 1) — a 500Ω symmetry-trim-pot to produce a high output at all bits, with the normal "dither" in the LSB only. Next, ground the input and adjust the Full Scale trimpot to produce an output which alternates between 10000000 and 01111111.

0 TO +5V OPERATION

Operation with 5 volt full scale inputs (0V to +5V or ±2.5V) can be obtained by specifying the DAC-100CCQ4.

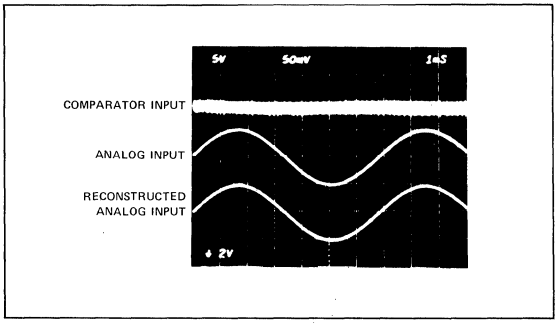
0.05% APPLICATIONS

Applications requiring 10 bits of resolution with 0.05% linearity can be implemented by adding a third up/down counter and utilizing all 10 inputs of a DAC-100ACQ3 (or Q4). See Figure 4.

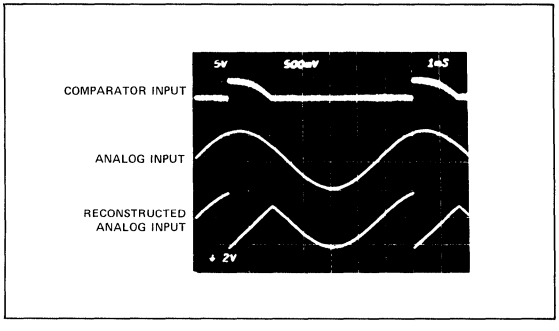
TRACKING A/D CONVERTER WAVEFORMS

These scope photos were taken to indicate the waveforms observed at the comparator input during normal and abnormal operation of the converter. The output analog voltage trace was generated by applying the encoded digital output to a second D/A converter.

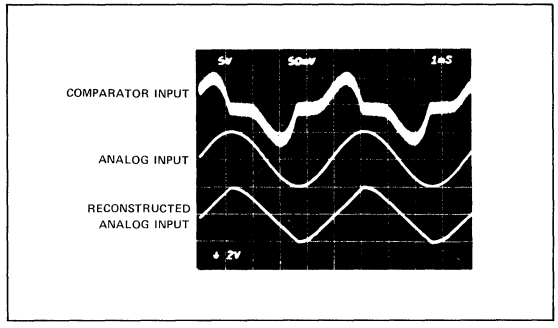
NORMAL OPERATION



INPUT OVER-RANGE



SLEW RATE LIMITING



PERFORMANCE

Performance of the completed converter is quite impressive despite the low cost and small size. Using clock rates of 3.0MHz, 10 V_{p-p} signals can be accurately tracked to frequencies of about 4.0kHz; higher frequencies can be accommodated by reducing the peak-to-peak amplitude.

Fully monotonic operation is obtained from 0° to 70° C; this is achieved because the DAC-100CQ3 is guaranteed to have ±1/2 LSB linearity to 8 bits (0.2%) over this temperature range, and the DAC-100ACQ3 has ±1/2 LSB linearity to 10 bits (0.05%).

All D.C. static errors can be attributed to the analog components only; the comparator makes no contribution to linearity errors, but its V_{OS} and V_{OS} drift with temperature are a consideration in the zero scale and full scale performance, and especially so in bipolar applications. The worst case DAC-100 zero error over 0° C to 70° C is 0.6mV; adding to this the 3.5mV maximum V_{OS} of the CMP-01C results in a worst case zero scale error of 4.1mV, which is acceptably small compared to the value of 1/2 LSB (19.5mV) for the 8-bit A/D.

Because the V_{OS} drift of the CMP-01C is typically only 1.8μV/° C even without offset triming, the full scale drift will be almost entirely a function of the DAC-100CC tempco —60ppm/° C maximum.

For 10-bit applications, the comparator V_{OS} becomes significant; the CMP-01C can be nulled, or the 0.8V maximum V_{OS} CMP-01E can be utilized without nulling. Nulling of the comparator is not required in bipolar applications; this is accomplished by the bipolar symmetry trimming.

Other performance characteristics of the completed converter are listed in Table 1.

MILITARY TEMPERATURE RANGE OPERATION

Operation over wider temperature ranges can be obtained by simply specifying appropriate temperature range components. The simplicity of the all IC design coupled with the compatibility with MIL-M-38510 processing assures high reliability in military applications.

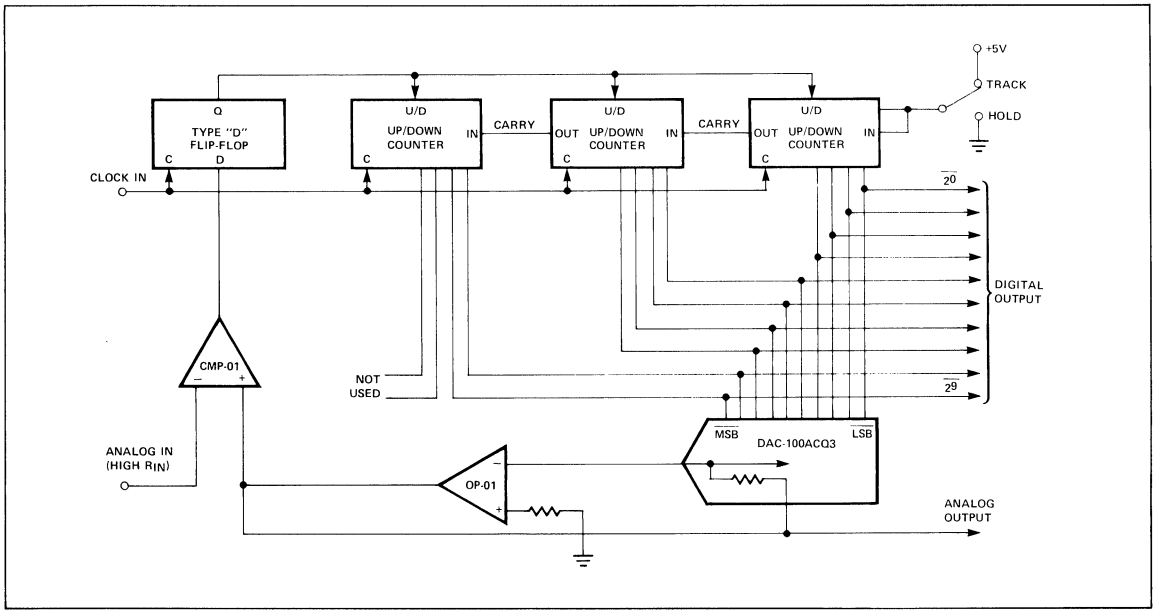


Figure 4. 10-Bit Voltage Output A/D Converter Block Diagram

CONCLUSION

Extremely compact, low power consumption, all IC tracking A/D converters are made possible by combining Precision Monolithics, Inc. DAC-100 series 10-bit D/A converter, CMP-01 series comparator, and commerically available MSI up/down counters. Layout, construction and adjustment are noncritical. The simplicity and low cost of the tracking A/D converter invites usage in many new applications, including single channel digitizing at remote transducer locations.

TABLE 1. PERFORMANCE DATA

	8-BIT	10-BIT
Nonlinearity (0°C to +70°C)	0.2% Maximum	0.05% Maximum
Full Scale Tempco (0°C to +70°C)	60ppm Maximum	60ppm Maximum
Zero Scale Error (0°C to +70°C)	0.10 LSB Maximum	0.20 LSB Maximum*
Zero Scale Error Comparator Trimmed (0°C to +70°C)	0.02 LSB	0.08 LSB
Full Scale Voltages	0V to +10V, ±5V 0V to +5V, ±2.5V	0V to +10V, ±5V 0V to +5V, ±2.5V
Power Supply Rejection (0°C to +70°C)	0.02% per % Maximum	0.02% per % Maximum
Power Consumption (V_S = ±15V, +5V)	1.4W Maximum	1.77W Maximum

*Untrimmed CMP-01E

APPENDIX — USEFUL DATA AND FORMULAE

	10V Full Scale	5V Full Scale
LSB — 8 Bits	39.1mV	19.5mV
10 Bits	9.85mV	4.92mV

Loop Slew Rate = Clock Frequency X V_{LSB} = f_c X V_{LSB}

Maximum Clock Frequency = $1/(T_A + T_B + T_C + T_D + T_E)$

WHERE: T_A = Flip-Flop Propagation Delay

T_B = Minimum Counter Set-Up Time

T_C = Counter Propagation Delay

T_D = D/A converter Settline Time (to n-bits)

T_E = Comparator Response Time

$$\text{Minimum Clock Frequency} = \frac{\pi \cdot V_{IN_{p\text{-}p}} \cdot f_{IN}\,\text{max}}{V_{LSB}}$$

AN-6

PMI

AN-11

A LOW-COST, EASY-TO-BUILD SUCCESSIVE APPROXIMATION A/D CONVERTER

Precision Monolithics Inc.

APPLICATION NOTE 11

Successive Approximation Analog-to-Digital Converters have often been considered to be complex, expensive and troublesome circuits to produce. This application note describes a high-speed 8-bit successive approximation A/D easily constructed using only three readily available ICs. Precision Monolithics' DAC-100 Digital-to-Analog Converter, CMP-01 Fast Precision Voltage Comparator, a Successive Approximation Register plus a handful of discrete components complete the design. Despite the simplicity, the A/D is capable of 8-bit conversions in 6μsec, and can easily be expanded to 10-bit resolution operation.

FEEDBACK A/D CONVERTERS

Most popular A/D converters built today use a digital-to-analog converter as part of a feedback or servo loop. Three of the most common types are the Ramp, Tracking, and Successive-Approximation; these differ primarily in the type of programming logic circuitry used to drive the D/A converter. All three types perform a comparison between the analog input and the output of a D/A converter; the logic changes the D/A output so that it approaches the analog input —when they are equal, the input to the DAC is the correct digitally encoded number (Figure 1).

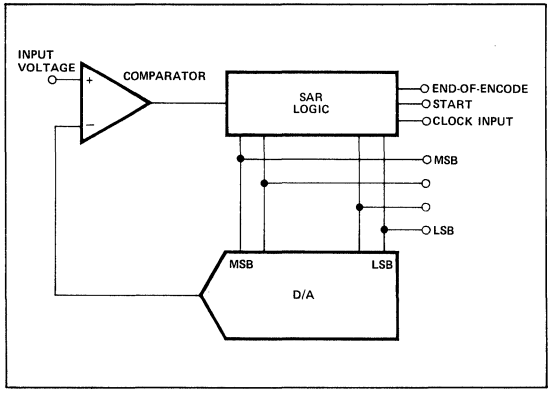


Figure 1. Basic Feedback A/D Converter

The Ramp or Count-up type ADC uses up-counters for the programming logic. A start command clears the counters which then count up until the comparator output changes. The user must allow 2^N clock periods to insure a complete conversion; therefore only very slowly varying data may be converted.

Tracking A/D converters use up/down counters for the programming logic; the comparator output forces the counters to "track" the changes in the analog input. Once initial "lock" is acquired the correct digital output is continuously available, and the converter may be capable of encoding fairly fast-moving input signals without requiring a sample and hold circuit. (Complete details on the construction of this type of converter are available in Precision Monolithics Application Note 6, "A Low-Cost, High-Performance Tracking A/D Converter.")

Tracking ADCs are at their best when used to encode a single signal with a well-behaved maximum slew rate; multiplexed or video signals have large discontinuities which cause large errors while the tracking loop moves to acquire a new "lock" on the signal.

Successive Approximation A/D Converters are attractive for their rapid conversion rates and have found wide acceptance in video and multiplexed data systems. Recently-announced ICs provide the three basic converter building blocks in integrated form, reducing the cost and complexity of this approach to a figure at or below that of the ramp and tracking types. The great advantage of the SA ADC is that complete "N"-bit conversions can be accomplished typically in N+1 clock periods — for a 10-bit converter this would be a speed improvement of about 100 times over the ramp type.

BASIC SUCCESSIVE APPROXIMATION A/D CONVERSION

An SA ADC operates by comparing the analog input to a series of "trial" conversions; the first trial compares the input to the value of the most significant bit (MSB) or half of full scale. Figure 2 shows the progression of trials for a 3-bit converter. If the input is greater than the MSB value, the MSB is retained and the converter moves on to "trying" the next most significant bit, or three-quarters full scale. If the input had been less than the MSB, the logic would have turned the MSB off before going on to the next most significant bit, or one-quarter full scale. This "branching" continues until each successively smaller bit has been tried, with the entire process taking "N+1" trials.

To implement the logic for the successive approximation algorithm, a configuration similar to Figure 3 may be employed wherein a start command places a "one" in the first bit of a shift register. This sets the first latch to "one," and turns on the DAC's MSB. If the comparator output remains slow, the "one" will remain in the latch; if not, the latch will be reset to zero before the next bit trial begins. The next clock cycle causes the shift register to place a "one" in the second bit and

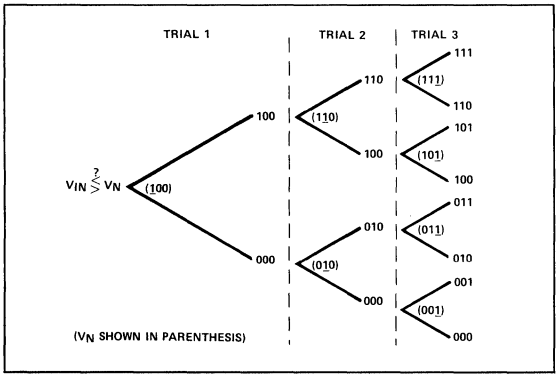


Figure 2. Flow Diagram for 3-Bit Successive Approximation A/D Conversion

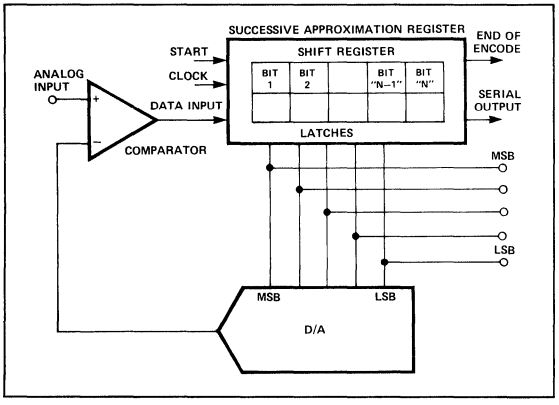


Figure 3. Successive Approximation A/D Converter

a similar process continues until all bits have been tried. After the last bit's trial, the end-of-encode output changes state indicating the parallel data is ready to be used. A useful feature of successive approximation conversion is that the correctly converted data is also available in serial form; this is handy for transmission of data on a single bus.

The complete sequence of events is demonstrated in the timing diagram of Figure 4. Note that "negative true" logic is shown; the DAC-100 employs a complementary binary code and the AM2502 produces a "low" output during each bit's trial, thus producing the standard successive approximation routine starting with the MSB trial and working towards the LSB trial. All events are initiated during positive-going clock transitions; the conversion process starts when the S input is held low, which also causes the CC (Conversion Completed) output to go high. After all bits have been tried, the last positive clock transition returns the CC to a low state, indicating the conversion has completed.

"CURRENT" COMPARISON

The previous discussion has indicated that the function of the comparator was to perform a comparison between the

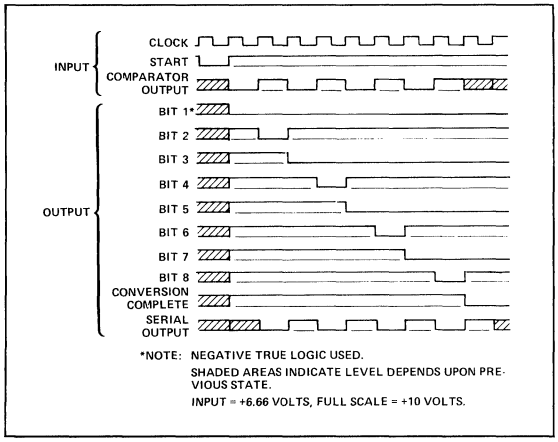


Figure 4. Timing Diagram

analog input voltage and the output voltage of the D/A converter. Higher speed conversions may be achieved by using the output of a fast current output DAC directly. This may be implemented as shown in Figure 5, where the comparator examines the polarity of ($V_{IN} - I_{IN} R_{IN}$). The "current comparison" method eliminates the need for a current-to-voltage converting op amp which is by far the slowest element in most D/A converters.

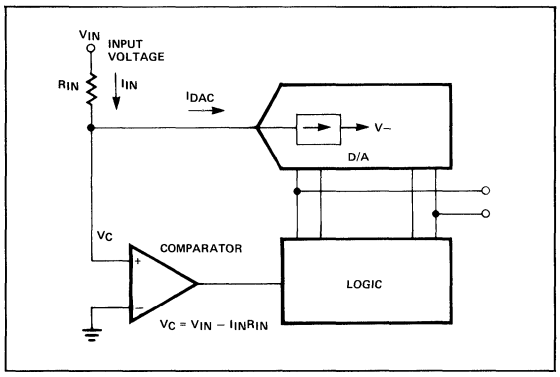


Figure 5. "Current Comparison" A/D Input

COMPLETE CIRCUIT

The schematic for the complete 8-bit A/D converter is shown in Figure 6. It is seen that the complete circuit adds very few components to the basic three ICs of the block diagram. A 200Ω potentiometer is used to adjust the full scale output and R1 is used to inject a +1/2 LSB value current into the sum node. This insures that adjacent code point transitions occur at 1/2 LSB points for minimum overall error. The clamp diodes minimize settling time and prevent large inputs from damaging the DAC output. For an 8-bit, 10 volt system the CMP-01CJ's maximum offset voltage is less than 1/10 LSB and should not require nulling.

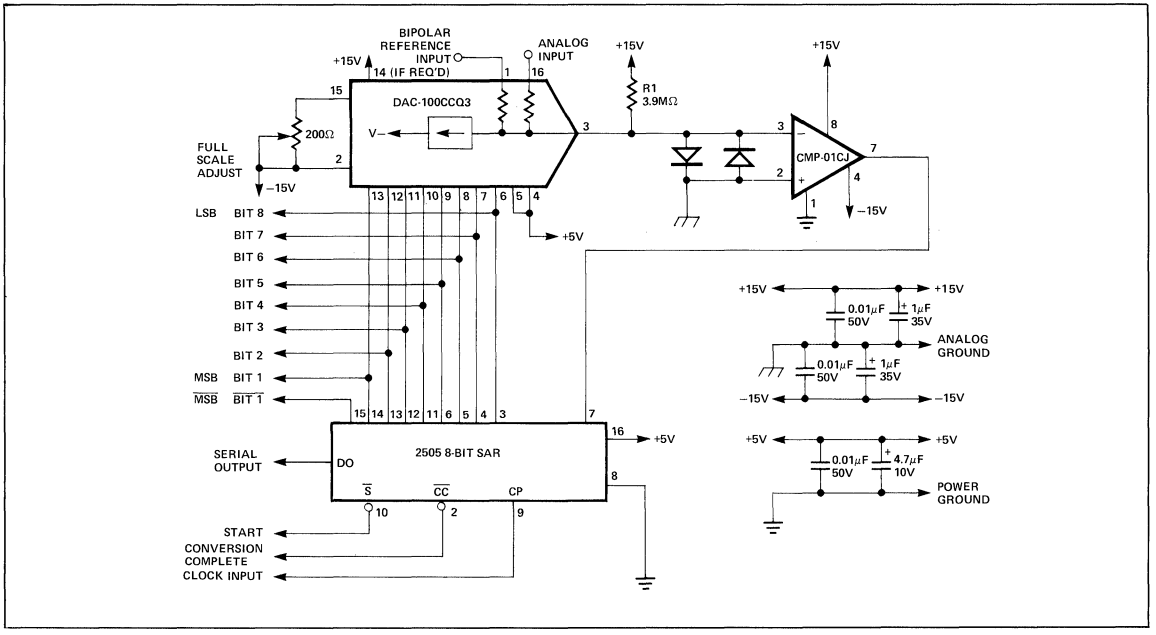


Figure 6. Complete 8-Bit A/D Schematic

GROUNDING

For optimum noise rejection, digital (power) ground currents should not flow in signal input ground return lines. Analog and power grounds should be connected as close as possible to the A/D converter input connector. Figure 7 illustrates a typical system installation showing the ground connections.

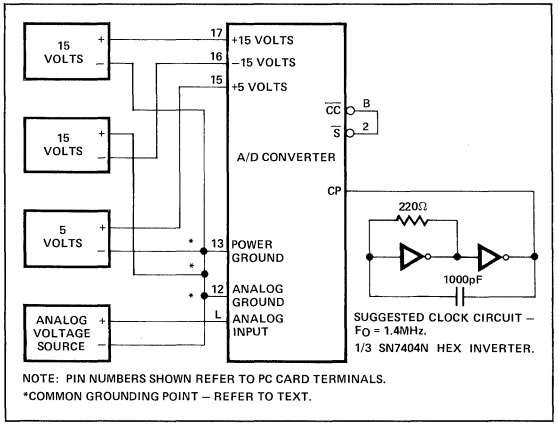


Figure 7. Grounding and Supply Hookup

LAYOUT

A suggested layout for an 8-bit converter is shown in Figure 8. This layout demonstrates some of the basic rules of good A/D converter practice: analog wiring is kept as short as possible and is separated from digital lines; the DAC output trace is especially short and directly connected to the comparator input and clamping diodes. Generous power supply bypassing has been employed using both disc and electrolytic capacitors. Other layouts can be easily designed because of the extreme simplicity of this circuit.

SERIAL OUTPUT

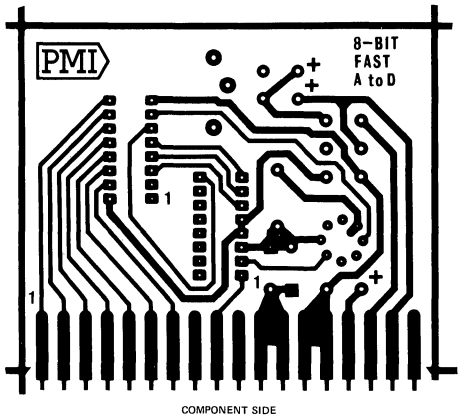
The digital output is available in serial NRZ (non-return-to-zero) format at the data output (DO) shortly after each positive-going clock transition. Serial output is especially convenient in applications where system wiring must be minimized, such as in one A/D per channel systems. Performing the A/D conversion process in close proximity to the signal source has the advantage of reducing errors associated with transmission of low level analog signals; instead, digitally encoded signals are transmitted with their inherent low error rates and ease of multiplexing.

BIPOLAR OPERATION

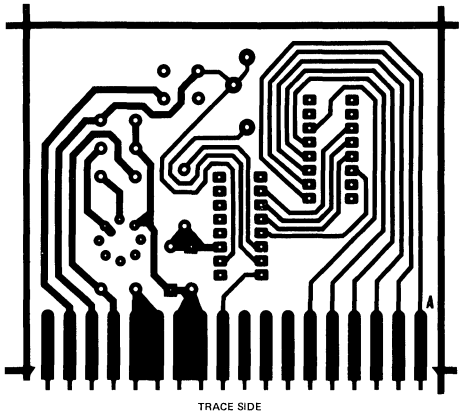
Bipolar operation can be obtained by injecting a current equal to 1/2 full scale into the sum node. This can be accomplished by applying +6.4 volts through a 500 ohm potentiometer to the internal bipolar resistor of the DAC-100. Both Bit 1 and $\overline{\text{Bit 1}}$ are available so 2's complement or offset binary coding may be obtained as desired.

0 TO +5V, ±2.5V OPERATION

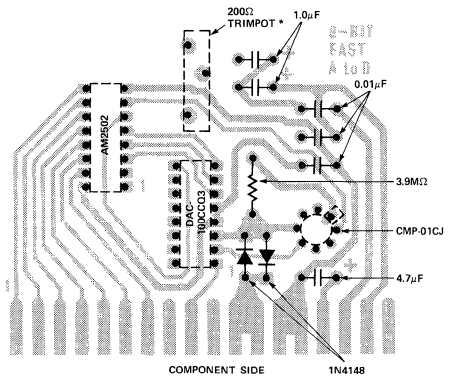
Operation with 5V full scale inputs (0 to +5V, ±2.5V) may be obtained by specifying DAC-100 models with a Q4 suffix.



COMPONENT SIDE



TRACE SIDE



COMPONENT SIDE

CONNECTOR PIN CONNECTIONS

18	N.C.	V	N.C.
17	+15 VOLTS	U	+15 VOLTS
16	−15 VOLTS	T	−15 VOLTS
15	+5 VOLTS	S	+5 VOLTS
14	POWER GROUND	R	POWER GROUND
13	POWER GROUND	P	POWER GROUND
12	ANALOG GROUND	N	ANALOG GROUND
11	ANALOG GROUND	M	ANALOG GROUND
10	N.C.	L	ANALOG INPUT
9	BIPOLAR REFERENCE VOLTAGE INPUT	K	N.C.
8	N.C.	J	N.C.
7	BIT 1	H	N.C.
6	BIT 1	F	BIT 5
5	BIT 2	E	BIT 6
4	BIT 3	D	BIT 7
3	BIT 4	C	BIT 8
2	S START	B	CC CONVERSION COMPLETED
1	CLOCK INPUT	A	DO SERIAL OUTPUT

Figure 8. 8-Bit A/D Layout

CALIBRATION

For unipolar, 8-bit, 10 volt full scale calibration apply +9.941 volts (full scale -3/2 LSB) to the input. Adjust the gain potentiometer until the digital output is alternating between "0000 0000" and "0000 0001". This calibrates the converter at a transition point insuring correct outputs over the analog input range. No zero adjust is necessary due to the low comparator input offset voltage (V_{OS}), virtually zero output offset of the DAC and the correct +1/2 LSB bias established by R1.

For 8-bit, ±5 volt full scale offset binary operation, first perform the unipolar calibration as described above with the bipolar reference removed. Next connect the +6.4 volt bipolar reference through the 500 ohm potentiometer to the bipolar input resistor. With -5.000 volts as an analog input, adjust the 500 ohm potentiometer until the digital output is alternating between "1111 1111" and "1111 1110". For calibration at lower bit resolutions refer to Table 1.

PERFORMANCE

Performance of the completed converter for 6, 7 and 8-bit resolution applications is shown in Table 2. To assure fully monotonic operation in 8-bit applications the DAC-100CC grade with its maximum nonlinearity of 0.2% from 0° to 70° C should be specified. Applications requiring 8-bit resolution with 0.3% or less linearity may utilize the lower cost DAC-100DD types.

All D.C. static errors can be attributed to the analog components only; the comparator makes no contribution to nonlinearity, but its 25° C V_{OS} and V_{OS} drift with temperature are a consideration in the zero scale and full scale performance, and especially so in bipolar applications. The worst case DAC-100 zero error over 0° to 70° C is 0.6mV; adding to this the 3.5mV maximum V_{OS} of the CMP-01C results in a worst case zero scale error of 4.1mV, which is acceptably small compared to the value of 1/2 LSB (19.5mV) for the 8-bit A/D.

*TRIMPOT is a registered trademark of Bourns, Inc.

Table 1. Reduced Resolution Application Data

Resolution Desired		Offset Current Value (1/2 LSB)	Conversion Complete Indicator	Full Scale Calibration Point	LSB (10VFS)
8 Bits	3.9MΩ	3.9μA	CC	9.941V	39mV
7 Bits	2MΩ	7.8μA	Bit 8	9.883V	78mV
6 Bits	1MΩ	15.6μA	Bit 7	9.766V	156mV
5 Bits	470kΩ	31.3μA	Bit 6	9.531V	313mV
4 Bits	240kΩ	62.5μA	Bit 5	9.163V	625mV

Table 2. Performance Data

Resolution D/A	6 Bits DAC-100DDQ3	7 Bits DAC-100DDQ3	8 Bits DAC-100CCQ3
0° to 70°C Maximum Nonlinearity	±0.3%	±0.3%	±0.2%
0° to 70°C Full Scale Tempco Maximum	120ppm/°C	120ppm/°C	60ppm/°C
Zero Scale Error Maximum	±0.05 LSB	±0.1 LSB	±0.2 LSB
Conversion Time 1.5MHz Clock	4.7μs	5.3μs	6.0μs
Unipolar Reference		Internal	
Bipolar Reference		External +6.4 Volts	
Input Impedance (+10V or ±5V Scale)		5kΩ Nominal	
Input Impedance (+5V or ±2.5V Scale)		2.5kΩ Nominal	
Quantizing Error		±1/2 LSB	
Output Code Unipolar		Complementary Binary	
Output Code Bipolar		Complementary Offset Binary	
Clock		External	
Logic Output Drive Capability		6 TTL Loads	
Analog Power Supply Range		±6V to ±18V	
Digital Power Supply Range		+5V ±5%	
Power Consumption ±15V and +5V Supplies		935mW Maximum	

Because the V_{OS} drift of the CMP-01C is typically only 1.8μV/°C even without offset trimming, the full scale drift will be almost entirely a function of the DAC-100CC tempco —60ppm/°C maximum. (Tempco of DAC-100DD models is 120ppm/°C.)

REDUCED RESOLUTION APPLICATIONS

Encoding time may be reduced in applications not requiring the full 8-bit resolution. In convert-on-command applications, the negative-going transition of the (N+1) bit may be used as the Conversion Completed (CC) signal; the register will continue to step through the remaining bits so the CC level will be present for one clock period only. For continuous conversion applications, the register may be truncated by applying a low level to the S input; however, caution must be observed to prevent possible stalling on power-up: the S input should be generated by either the CC or bit (N+1) going to a low state. Figure 9 demonstrates a 6-bit, continuous-encoding application. Since reducing the resolution increases the size of the LSB, the value of R1 and the full scale calibration point should be changed accordingly, as shown in Table 1. Additional speed in reduced resolution applications may be achieved by increasing the clock frequency.

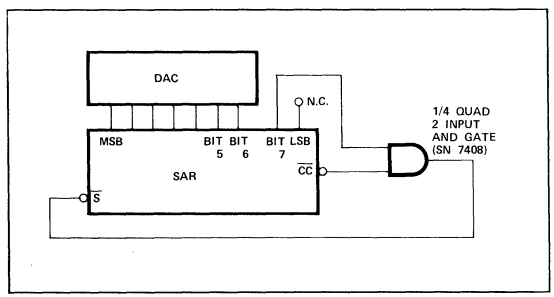


Figure 9A. Short-Cycled Continuous Coding (6 Bits Shown)

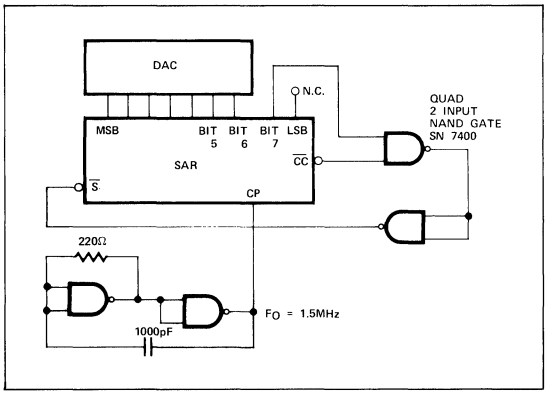


Figure 9B. Short-Cycled Continuous Encoding (Alternate Method Including Clock)

10-BIT APPLICATIONS

The basic 8-bit converter may easily be expanded to 10 bits by using a 2504 12-bit Successive Approximation Register; it may be allowed to step through all 12 bits or short-cycled as described above (Figures 9A, 9B). All DAC-100 Series devices have 10-bit resolution; for applications requiring 10-bit monotonic performance the DAC-100ACQ3 or Q4 grades with maximum nonlinearity of ±0.05% (0° to 70° C) should be specified; for less demanding applications the ±0.1% DAC-100BCQ3 (Q4) grades are recommended. Due to the 10mV LSB size, comparator V_{OS} can provide significant zero error. This can be eliminated in unipolar applications by nulling the CMP-01CJ or specifying the 0.8mV offset CMP-01EJ. No initial V_{OS} improvement is required in bipolar applications, as this error will be eliminated during the bipolar calibration procedure. The offsetting resistor (R1) should be 15MΩ for 10-bit applications, with the full scale calibration voltage of +9.985 for unipolar applications.

SYSTEM CONSIDERATIONS

When integrating the A/D Converter into a system, consideration must be given to several factors to assure best performance. First, the analog signal to be encoded should not change more than 1/2 LSB during the encoding process; a sample-and-hold circuit should be used if required to hold changes to 1/2 LSB or preferably, much less (Figure 11). Second, proper grounding of the system is essential to prevent errors due to system noise. The preferred method is to connect the analog signal ground and digital power ground together at only one point, right at the A/D's connector. This will insure that digital ground currents do not flow in the analog ground line.

LOWER POWER CONSUMPTION

Power consumption may easily be reduced from 935mW maximum to about 310mW with two minor design changes. The D/A and comparator power supplies can be reduced from ±15 volts to ±6 volts and low power TTL AM25LO2PC logic function may be specified. Digital output fanout is reduced to three standard TTL loads. The value of R1 must also be lowered accordingly to maintain the same +1/2 LSB bias current to the sum node.

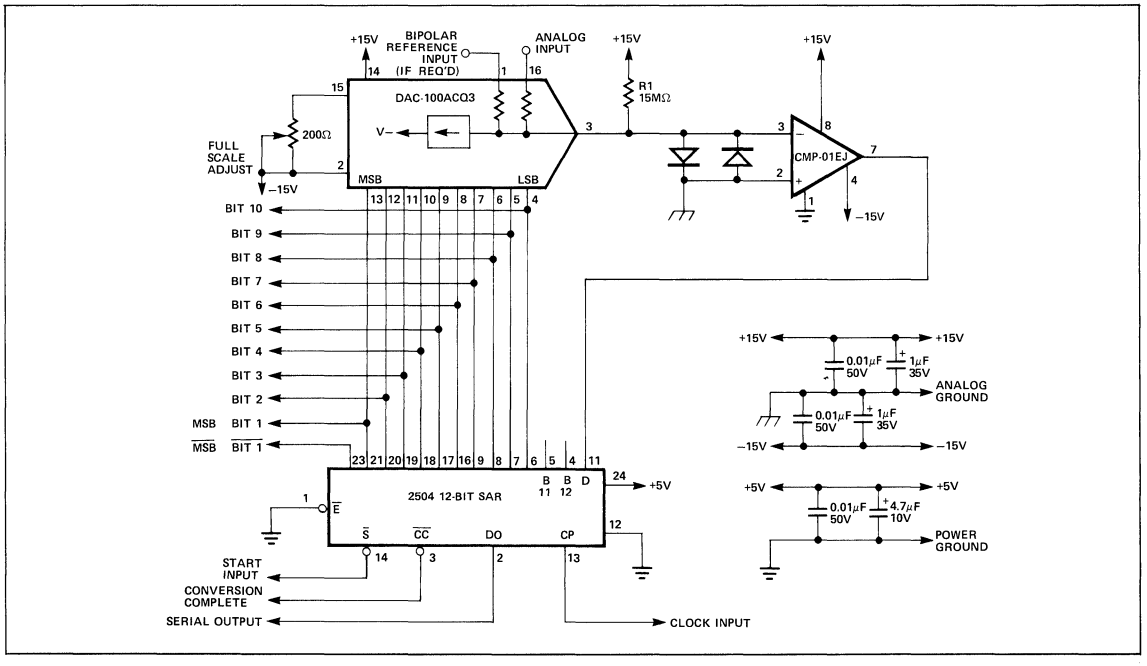


Figure 10. Complete 10-Bit A/D Schematic

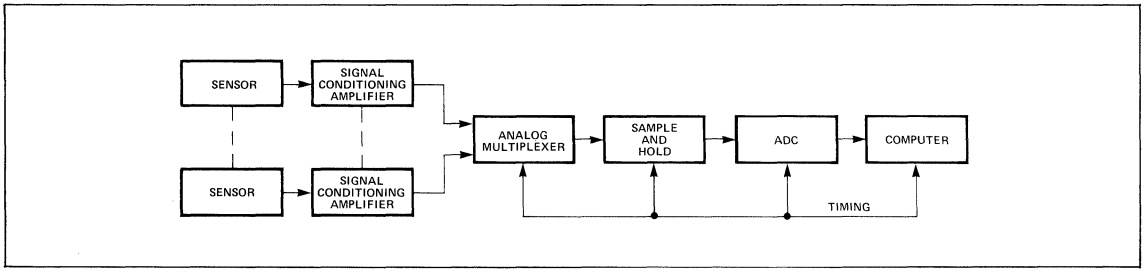


Figure 11. Typical Multiplexed Data Acquisition System

MILITARY TEMPERATURE RANGE OPERATION

Operation over wider temperature ranges can be obtained by simply specifying appropriate temperature range components. The simplicity of the three IC designs coupled with the compatibility of the devices with MIL-STD-883B processing assures high reliability in military applications.

CONCLUSION

Extremely compact, rugged, low power consumption successive approximation A/D converters are made possible by combining three ICs: PMI's DAC-100 Series 10-bit D/A, CMP-01 comparator, and a Successive Approximation Register. This simple, low cost design opens up new applications such as one A/D per channel operation in data acquisition systems.

PARTS LIST FOR 8-BIT A/D CONVERTER

±0.3% maximum nonlinearity, FS tempco 120ppm/°C	
1	DAC-100DDQ3 (or Q4)
1	CMP-01CJ
1	AMP2502PC (Advanced Micro Devices) or Equivalent
1	Pot-200Ω Bourns #3006P-1-201
1	4.7μF CAP-Mallory #TDC475M010EL
2	1.0μF CAP-Mallory #TDC105M035EL
2	Diode, 1N4148
3	.01μF CAP-Centralab #CK-103
1	PC Board
1	Resistor 3.9MΩ 5% 1/4W
For ±0.2% maximum nonlinearity, FS tempco 60ppm/°C use DAC-100CCQ3 (or Q4)	

PARTS LIST FOR 10-BIT A/D CONVERTER

±0.1% maximum nonlinearity, FS tempco 60ppm/°C	
1	DAC-100BCQ3 (or Q4)
1	CMP-01EJ
1	AM2504PC (Advanced Micro Devices) or Equivalent
1	Pot-200Ω Bourns #3006P-1-201
1	4.7μF CAP-Mallory #TDC475M010EL
2	1.0μF CAP-Mallory #TDC105M035EL
2	Diode, 1N4148
3	.01μF CAP-Centralab #CK-103
1	PC Board
1	Resistor 15MΩ 5% 1/4W
For ±0.05% maximum nonlinearity, FS tempco 60ppm/°C use DAC-100ACQ3 (or Q4)	

PMI

AN-12

TEMPERATURE MEASUREMENT METHOD BASED ON MATCHED TRANSISTOR PAIR REQUIRES NO REFERENCE

Precision Monolithics Inc.

APPLICATION NOTE 12

Most remote temperature measurements are made with thermistors or thermocouples as the sensing elements. This article shows how the function can be accomplished by using the intrinsic properties of a well-matched monolithic transistor pair. The method is attractive for its simplicity, accuracy, and long-term stability. Of particular utility is the fact the output is inherently linear and is directly useable without special linearizing circuitry.

Thermocouples can require both linearizing circuitry and reference junction making them difficult to apply. Linear outputs may be achieved with composite thermistor-resistor networks but long-term stability is diffult to predict. Ordinary silicon diodes, when operated as temperature sensors, require constant current drive and extensive calibration. The matched transistor pair method has none of these drawbacks.

BASIC THEORY

Matched transistor pairs have predictable relationships which make temperature measurements possible. To develop these relationships, let us consider the fundamental properties of a single transistor. The well known relationship between collector current and base-emitter voltage for a single transistor is:

$$1.\ V_{BE} = \frac{kT}{q} \log_e \left(\frac{I_C}{I_S}\right) \text{ provided } I_C/I_S >> 1$$

where

k = Boltzmann's constant = 1.38×10^{-23} joules/°K
T = absolute temperature, °K
q = charge of an electron = 1.6×10^{-19} coulomb
I_S = theoretical reverse-saturation current $\cong 1.87 \times 10^{-14}$A
I_C = collector current

Consider the difference in base-emitter voltages, ΔV_{BE}, of two transistors operated at the same temperature:

$$2.\ \Delta V_{BE} = \frac{kT}{q} \log_e \left(\frac{I_{C1}}{I_{S1}}\right) - \frac{kT}{q} \log_e \left(\frac{I_{C2}}{I_{S2}}\right)$$

This expression may be rewritten to:

$$3.\ \Delta V_{BE} = \frac{kT}{q} \log_e \left(\frac{I_{C1}}{I_{C2}}\right) - \frac{kT}{q} \log_e \left(\frac{I_{S1}}{I_{S2}}\right)$$

The values of I_{S1} and I_{S2} are a strong function of processing and geometry variables, and are very nearly identical in a well-matched monolithic transistor pair. As I_{S1} and I_{S2} approach equality ($\log_e 1 = 0$), the second term can be eliminated. For an ideal pair the expression becomes:

$$4.\ \Delta V_{BE} = \frac{kT}{q} \log_e \left(\frac{I_{C1}}{I_{C2}}\right)$$

Note that if the ratio of collector currents I_{C1} to I_{C2} is made constant, ΔV_{BE} will be proportional to absolute temperature alone. No absolute values of current are required because only a stable current ratio must be maintained. For a fixed ratio of 2 to 1 the expression is:

$$5.\ \frac{\Delta V_{BE}}{\Delta T} = 5.973 \times 10^{-5} = 59.73 \mu V/°K$$

This predictable differential base-emitter voltage relationship allows a matched transistor pair to be used as a temperature sensor. A complete temperature measuring system can be built with a matched pair, two constant current sources, and a differential amplifier as shown in Figure 1.

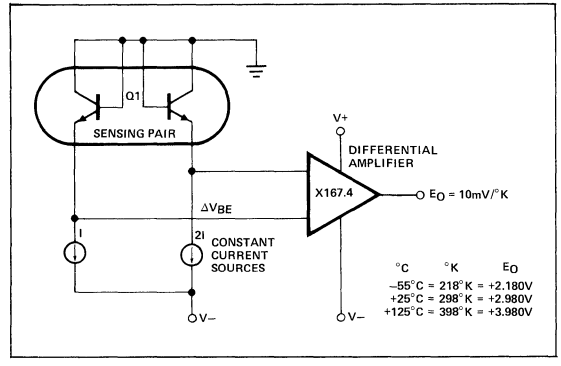


Figure 1. Basic Temperature Sensor

SYSTEM DESIGN CONSIDERATIONS

To illustrate this concept, let us design a system to provide accurate temperature mesurement over the range of −55°C to +125°C (218°K to 398°K). Other goals are: ease of calibration, long-term stability, standard resistor values, and small physical size. In addition, the system should be capable of operation with the sensing matched pair located up to 100 feet from the current sources and differential amplifier. A system achieving these goals is detailed below.

SENSING MATCHED PAIR

Any mismatch will cause performance to deviate from the ideal case shown in Equation 4, the most critical parameter

being average offset voltage drift (TCV_{OS}). This quantity, multiplied by the largest temperature excursion (100°K) and the differential amplifier gain (167.4), will be the output error and is shown in Table 1 for typical TCV_{OS} specifications.

Clearly, system accuracy is directly related to the degree of matching of the sensing pair. A Precision Monolithics MAT-01H with its typical TCV_{OS} of 0.15μV/°C was specified in order to minimize this error factor.

Table 1.

TCV_{OS}	Error in °K over 100°
0.15μV/°C	0.251°K
0.5μV/°C	0.837°K
1.0μV/°C	1.67°K
2.0μV/°C	3.34°K
2.5μV/°C	4.19°K
5.0μV/°C	8.37°K
10μV/°C	16.7°K

CONSTANT CURRENT SOURCES

Two currents of a precise 2 to 1 ratio are provided by this section. Several considerations make 5μA and 10μA good choices as nominal operating currents for I_{C2} and I_{C1} respectively. Most monolithic matched transistor pairs are specified at $I_C = 10\mu A$. Input bias currents associated with the differential amplifier can be ignored because 5μA is three orders of magnitude larger. Resistor values are small enough to keep physical size and cost reasonable. Finally, the quiescent currents do not develop significant voltage drops in 100 feet of ordinary shielded-pair cable.

The two most important current source transistor matching characteristics required are h_{FE} and V_{OS} long-term stability, assuming that this part of the circuit is not subjected to wide temperature variations. If the system is to have good power supply and ripple rejection, the h_{FE} match must be maintained over a range of operating currents. These characteristics will insure a constant 2 to 1 ratio of I_{C1} to I_{C2} is maintained.

With the circuit as shown in Figure 2, the total system has measured power supply rejection of 1°K/volt. Once calibrated, long-term changes in V_{OS} will change the current ratio, and, in turn, the output. A Precision Monlithics MAT-01GH was selected for Q2 because it has the desired combination of specified long-term stability (0.2μV/month) and close h_{FE} matching, typically 1%.

DIFFERENTIAL AMPLIFIER

The sensing pair and constant current sources provide a differential voltage (ΔV_{BE}) which is directly proportional to absolute temperature. The amplifier must acquire this voltage difference in the presence of common mode voltages, amplify it by 167.4, and change it from a differential to a single-ended signal. Excellent performance is obtained using the circuit of Figure 3.

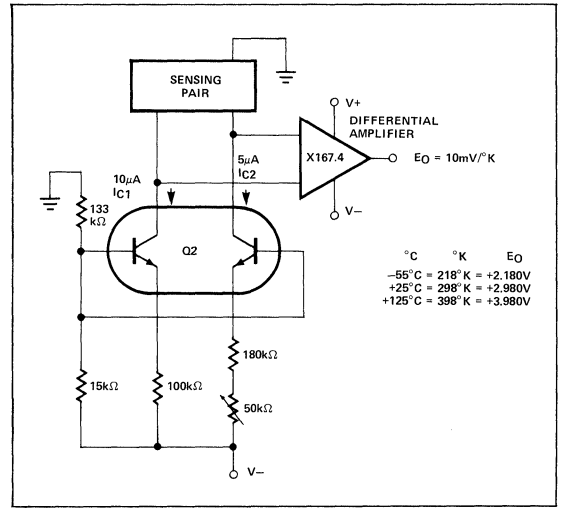


Figure 2. Basic Temperature Sensor

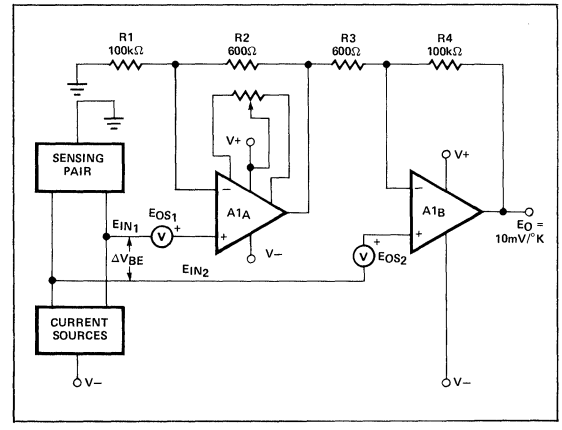


Figure 3. Differential Amplifier Design

The two op-amp differential amplifier configuration is widely used wherever high input impedance and fixed gain are required. This amplifier uses a dual matched instrumentation operational amplifier designed and specified for differential applications, the Precision Monolithics OP-10CY.

GENERAL DESIGN CONSIDERATIONS

Assuming ideal amplifiers, the expression for output voltage is:

$$6.\ E_o = \left[E_{IN_1}\left(1 + \frac{R2}{R1}\right)\frac{R4}{R3}\right] + E_{IN_2}\left(\frac{R4}{R3} + 1\right)$$

With ideal resistors this simplifies to:

$$7.\ E_o = (E_{IN_2} - E_{IN_1})\left(\frac{R4}{R3} + 1\right) \text{ provided } \frac{R1}{R2} = \frac{R4}{R3}$$

In this system, (E_{IN1} — E_{IN2}) has been previously defined as ΔV_{BE}. The actual expression for E_o may be written as:

8. $E_o = \Delta V_{BE} \left(\frac{R4}{R3} + 1\right)$ but $\frac{\Delta V_{BE}}{\Delta T} = 5.973 \times 10^{-5}$ (Eq. 5)

Therefore, the ideal overall system output expression is:

9. $E_o = (5.973 \times 10^{-5}) \left(\frac{R4}{R3} + 1\right) T$

COMMON MODE REJECTION

At 25°C (298°K), ΔV_{BE} is 17.8mV while the individual sensing pair base-emitter voltages are about 520mV. There is a need to reject the 520mV common mode input voltage while accurately amplifying the differential input voltage, ΔV_{BE}. At −55°C (218°K), the situation becomes more difficult with ΔV_{Be} of 13mV and 396mV of common mode voltage. Keeping in mind that this is a best case disregarding any extraneous cable pickup, it can be observed that the requirement for high common mode rejection is very real.

Because the dual op amp has a specified 117dB common mode rejection ratio match, the ability to reject common mode inputs becomes primarily a function of resistor ratio matching. This device eliminates the need for special op amp selections in this stringent differential amplifier application.

Resistor selections can be avoided by using readily available 0.01% tolerance precision resistors, resulting in a worst-case ratio match of 0.04%. This ratio match, a combination with the dual op amp's performance, results in greater than 100dB common mode rejection at the amplifier's input.

Long term stability of the resistors must approach the initial ratio match or degradation of common mode rejection can occur over time. The resistors chosen are specified at ±50ppm/3 years and ±5ppm/°C thereby assuring stability versus time and temperature.

DIFFERENTIAL OFFSET VOLTAGE

The amplifier's differential input offset voltage (E_{OS1} — E_{OS2}) will be the major error factor. If the individual input offset voltages are of equal magnitude and polarity they appear as a common mode input and are rejected. The OP-10CY provides the additional convenience that only a single

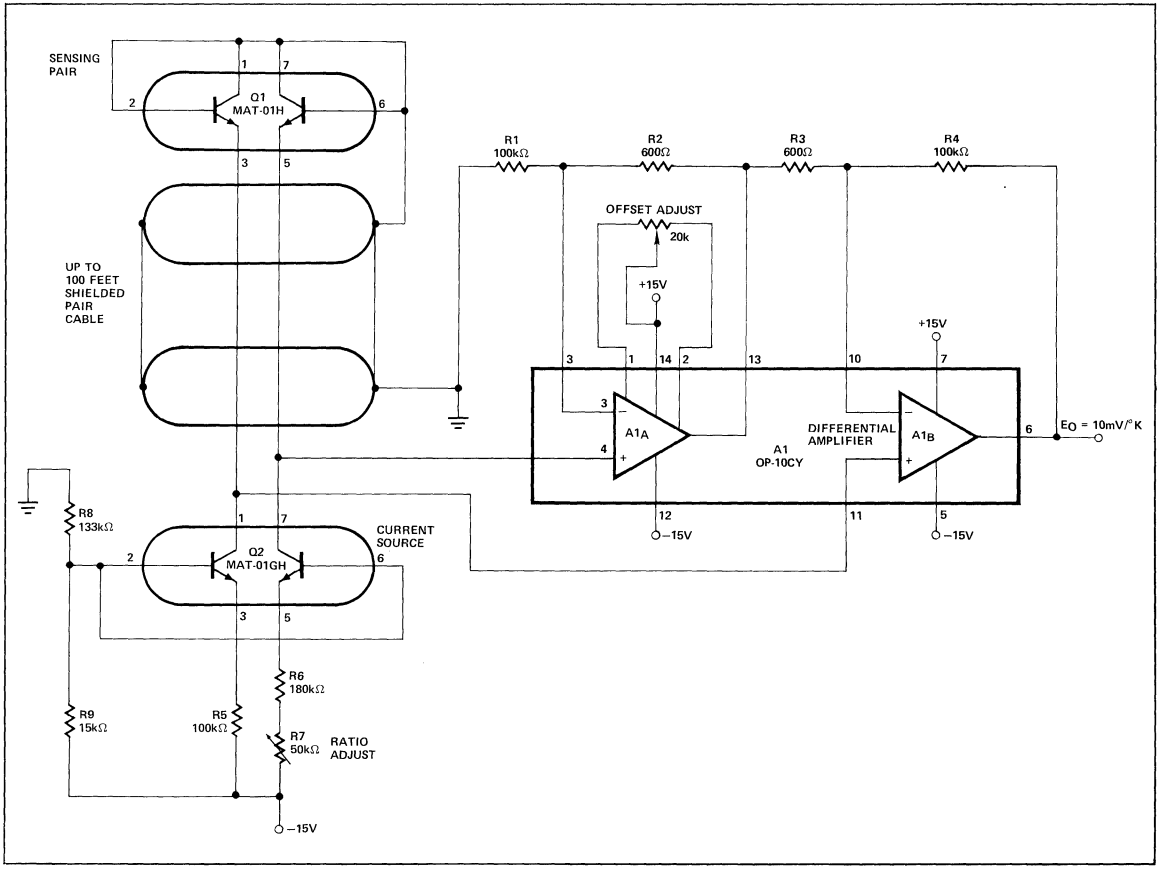


Figure 4. Complete Schematic

offset adjustment is necessary to provide the required ΔV_{OS} match; this adjustment at the same time provides a minimum $TC\Delta V_{OS}$ of the differential amplifier.

INSTALLATION

Ordinary shielded pair cable, with #22 or larger conductors, is satisfactory for most remote temperature measuring applications. Good thermal conductivity from the sensing pair's case to the environment being measured is essential to avoid incorrect readings. When this circuit is used for temperature control, thermally-conductive epoxy works especially well in attaching the sensing pair to the device being controlled.

CALIBRATION PROCEDURE

This is an easy two-step procedure. First, short the differential amplifier inputs and adjust the offset potentiometer until the output reads zero volts. Remove the input short. Second, with the sensing pair at a known temperature (room temperature is suitable), adjust the ratio potentiometer for a correct differential amplifier output reading. Having the capability of room temperature calibration makes this circuit much more convenient to calibrate than other types.

OVERALL ACCURACY

This circuit, with the components as specified, is capable of ±1°k accuracy over the full military temperature range of −55°C to +125°C (218°k to 398°k). Optimum accuracy is obtained with the differential amplifier and constant current sources in a controlled environment remote from the sensing pair. Maintenance of high accuracy over long periods of time is achieved because all components used in this design have long-term stability specified.

APPLICATIONS

The circuit's output, as measured by a 10-volt full scale digital panel meter, makes a digital thermometer. DPMs with BCD outputs may be used in applications requiring simultaneous direct readout and digital outputs for control purposes.

CONCLUSIONS

Accurate temperature measurement and control sysems are easily and economically built using the predictable characteristics of modern monolithic matched transistor pairs. This method offers long-term stability, excellent linearity, simple calibration, and high performance in severe environments.

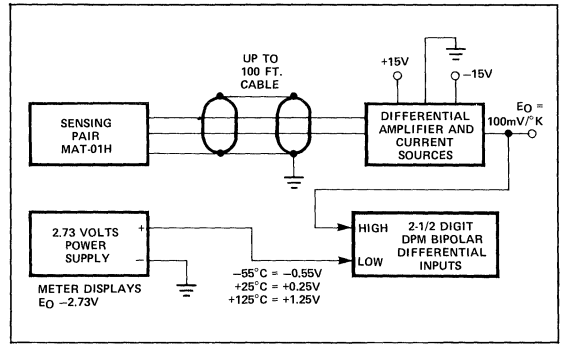


Figure 6. Digital Thermometer with Readout in °C

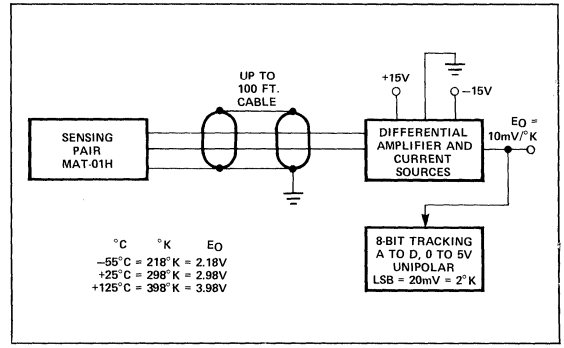


Figure 7. Binary-Coded Temperature Readings with 2° Resolution

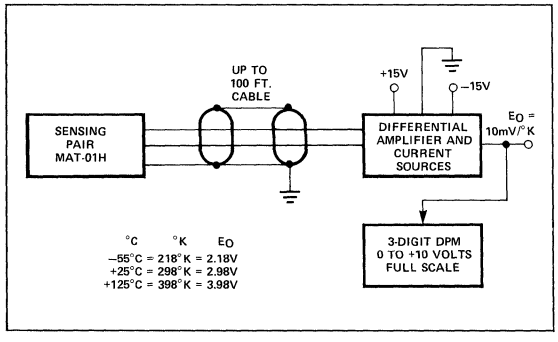


Figure 5. Basic Digital Thermometer with Readout in Degrees Kelvin (°k)

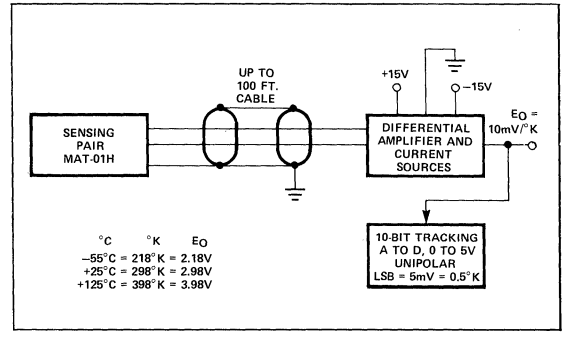


Figure 8. Binary-Coded Temperature Readings with 5° Resolution

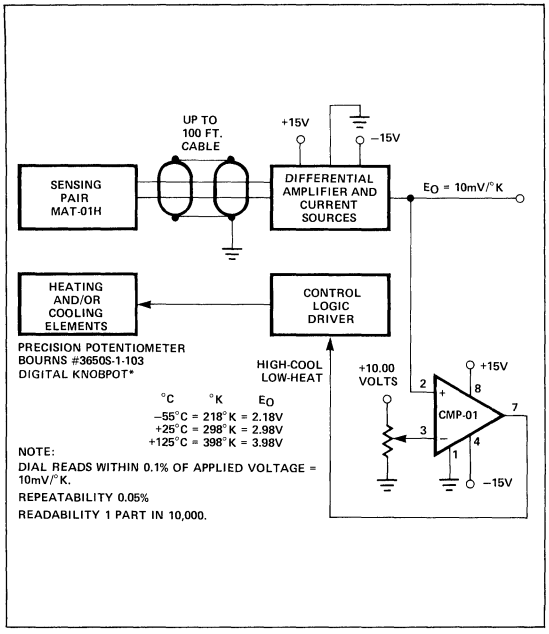


Figure 9. Temperature Controller — Digital Dial Controlled

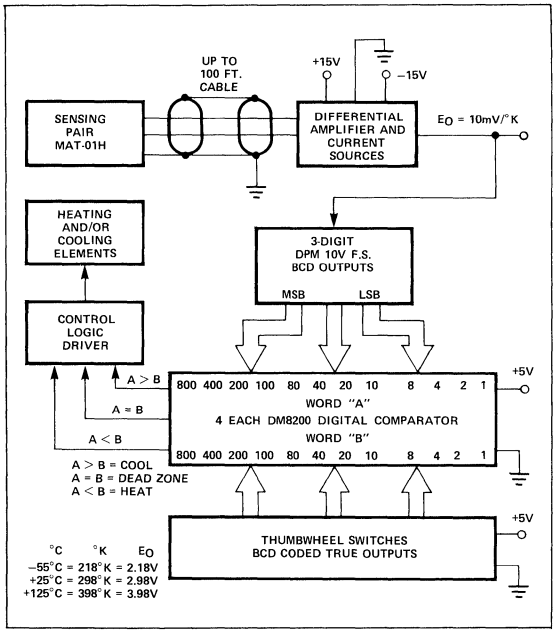


Figure 10. Temperature Controller — Digital Thermometer

PARTS LIST

1.	Q1	MAT-01H, Matched Transistor Pair Precision Monolithics, Inc.
2.	Q2	MAT-01GH, Matched Transistor Pair Precision Monolithics, Inc.
3.	A1	OP-10CY, Dual Instrumentation Op Amp Precision Monolithics, Inc.
4.	R1, R4	Resistor, 600Ω, 0.01% General Resistance Econister
5.	R2, R3	Resistor, 100kΩ, 0.01% General Resistance Econister
6.	R5	Resistor, 100kΩ, 0.1% General Resistance Econistor
7.	R6	Resistor, 180kΩ, 0.1% General Resistance Econistor
8.	R7	Potentiometer, 50kΩ, 10% Bourns #3006P-1-503
9.	R8	Resistor, 133kΩ, 1% RN55C1333F
10.	R9	Resistor, 15kΩ, 1% RN55C1502F
11.	R10	Potentiometer, 20kΩ, 10% Bourns #3006P-1-203

*KNOBPOT is a registered trademark of Bourns, Inc.

PMI

AN-13

THE OP-07 ULTRA-LOW OFFSET VOLTAGE OP AMP — A BIPOLAR OP AMP THAT CHALLENGES CHOPPERS, ELIMINATES NULLING

Precision Monolithics Inc.

APPLICATION NOTE 13

Note to readers: This article was written prior to the introduction of the OP-77, a highly improved direct descendant of the OP-07. The OP-77 is recommended for all new designs and as a direct, higher performance replacement in existing OP-07 circuit designs.

INTRODUCTION

The OP-07, a new bipolar-input monolithic operational amplifier, provides chopper-stabilized amplifier performance at bipolar prices. Input offset voltage, the major error contribution in most designs, is reduced to a maximum of 25μV by a new computer-controlled on-chip trimming technique. Such low V_{OS} eliminates the nulling potentiometer requirement of most op amp circuits, greatly reducing system complexity while improving reliability. A description of this amplifier's design and performance is given, followed by an applications section showing how superior input specifications can simplify high-accuracy analog design.

IMPORTANCE OF LOW INPUT OFFSET VOLTAGE

In many applications, the initial input offset voltage of operational amplifiers causes more inaccuracy than all other error factors combined. The other significant error parameters, such as bias and offset currents, open-loop gain, and common mode rejection, have come closer to theoretically ideal performance than has V_{OS}. For this reason, most operational amplifiers, monolithic and modular, are provided with terminals to allow the user to adjust this offset voltage to zero — a costly and potentially unreliable procedure, which in many cases degrades performance of TCV_{OS}. Monolithic op amp manufacturers have constantly strived for improvement in V_{OS} from μA709 and μA741 at 5000μV, to the μA725 at 1000μV in 1969, to the OP-05A at 150μV in 1972. The OP-07A at 25μV maximum V_{OS} is a significant milestone in monolithic bipolar operational amplifier design.

Temperature stability is also important since the benefits of low initial V_{OS} are quickly lost if a small change in operating temperature causes substantial V_{OS} drift. Good long-term V_{OS} stability is required to avoid periodic re-calibrations and degradation of system performance over time. Until now, chopper-stabilized or externally-nulled monolithic op amps have been the usual choices despite the disadvantages of high noise and/or external components. The OP-07 design achieves the desired combination of low V_{OS}, low TCV_{OS}, long-term V_{OS} stability, low bias current, and low noise. It provides performance comparable to chopper-stabilized amplifiers with the further advantages of freedom from chopper-frequency noise and external component requirements.

LOW V_{OS} AMPLIFIERS

Some of the more common methods for optimizing V_{OS} performance have been chopper-stabilized amplifiers, bipolar amplifiers nulled to zero initial V_{OS}, and combinational amplifiers constructed with a matched transistor pair followed by a standard bipolar op amp. Each approach to the V_{OS} problem is a compromise between allowable error, reliability and price. The purpose of this discussion is to show how the OP-07 provides superior performance, higher reliability, and reduced size at a lower overall cost.

CHOPPER-STABILIZED AMPLIFIERS

In the past, designers have been forced to use chopper-stabilized amplifiers in applications requiring less than 100μV initial V_{OS}. The OP-07 is a cost-effective alternative, providing chopper-type performance with 741 ease-of-application. Use of a bipolar input op amp eliminates the usual chopper problems of high noise, large physical size, and limited common-mode input voltage range.

Low initial offset voltage specifications lose their significance if noise and long-term drift are of the same magnitude. Although the monolithic choppers have lower average input bias currents, the chopping action produces very large spikes in the input currents and prevents their use with large or unbalanced source resistors. For this reason, most chopper manufacturers carefully avoid specifying noise currents above 10Hz. The input bias current, remains below 4nA over the full military temperature range, and being free from chopper spikes, enables use in high impedance circuitry.

Another chopper-related problem is that input signals often interact with chopping frequency components and their harmonics. This interaction can cause errors due to intermodulation, producing slowly varying offset voltages usually below 20Hz. Chopper frequency switching transients can also cause electromagnetic interference frequently requiring special shielding and input guarding methods to protect adjacent circuitry. Modular choppers can have input overload recovery times as high as five seconds and require up to ten external components to effectively eliminate this problem. Monolithic choppers require expensive, large external components, such as two 0.1μF teflon dielectric capacitors, for wide temperature range operation. These problems are eliminated by the OP-07.

NULLED BIPOLAR AMPLIFIERS

The major disadvantage of most high performance bipolar op amps is that their high initial V_{OS} must be adjusted to zero with a nulling potentiometer or trimming resistors. In certain amplifiers, this is also a requirement in order to optimize TCV_{OS} performance. Selected or adjusted components require special test labor, take up much-needed space, decrease reliability, and add to system complexity. "Maintainability" is poor — field replacements or renulling due to long-term V_{OS} and resistance changes must be performed by a skilled technician with sophisticated test equipment. Use of an internally-nulled OP-07 avoids all of these problems since it is a complete, fully-interchangeable device, and does not require zeroing to optimize TCV_{OS}.

COMBINATIONAL AMPLIFIERS

This is one of the oldest methods, usually implemented with a heated-substrate matched transistor pair in a differential-input gain stage followed by a conventional op amp. This method requires four precision resistors, a nulling potentiometer, external frequency compensation, and up to 360mW of heater power. TCV_{OS} is only about $2\mu V/°C$ despite the temperature control for the input pair. The OP-07 provides improved performance in all parameters as well as lower cost, elimination of calibration labor, lower noise and a tremendous reduction in total power consumption.

CIRCUIT DESCRIPTION

The three-stage design concept of previous Precision Monolithics' instrumentation quality op amps was retained for the OP-07 because, using this design, nulling of V_{OS} simultaneously optimizes TCV_{OS}. (This relationship is not the case for the more commonly used two-stage "741"-type amplifier.) There are additional advantages of high gain, low noise, and predictable long-term stability. Low input bias current is achieved by bias current cancellation; i.e., currents are generated equal in magnitude but opposite in direction to the base currents of the input transistors Q1 and Q2 in the simplified schematic of Figure 1.

and Q3 are h_{FE}-matched transistors operating at similar collector currents and, therefore, the base current of Q1 is approximately equal to the base current of Q3. Q3's base current is supplied by Q7, a diode-connected PNP transistor closely matched to Q5. Together Q5 and Q7 form a current mirror (turnaround) and the collector current of Q5 will equal

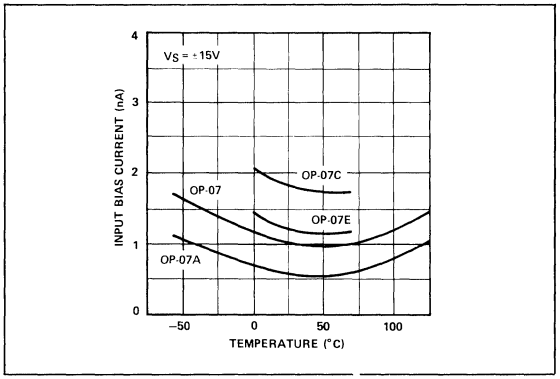


Figure 2. Input Bias Current vs Tempe.ature

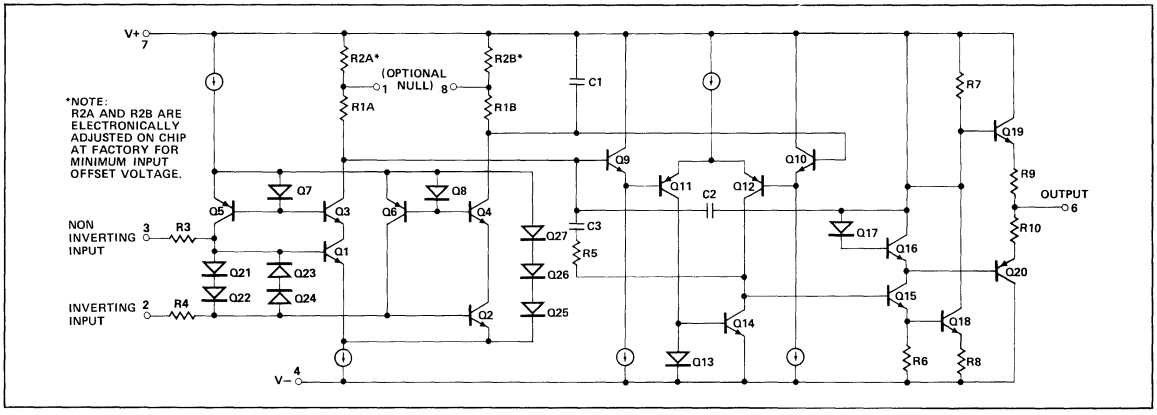


Figure 1. OP-07 Simplified Schematic

INPUT STAGE

To achieve lowest initial V_{OS}, TCV_{OS} and noise, a simple differential input pair, Q1 and Q2, was chosen. V_{OS} nulling resistors R2A and R2B are electronically adjusted and will be covered separately in the trimming discussion. R3 and R4, in conjunction with Q21-Q24, provide input differential overvoltage protection.

The symmetry of the input stage allows examination of only one side to demonstrate bias current cancellation. Base drive for the input transistor, Q1, is provided by Q5 and the external circuitry; the difference between Q5's collector current and Q1's base current being the input bias current. Q1 the base current of Q3. In this manner almost all base current for Q1 is provided by Q5 and precise bias current cancellation is achieved. Careful design has enabled this cancellation to be effective over a wide temperature range. (Figure 2.)

FOLLOWING STAGES

The first stage output is buffered by emitter followers Q9 and Q10, and applied to a high-gain differential stage, Q11 and Q12. Its output, the junction of Q12, Q14, Q15, and R5, drives a short-circuit-protected complementary emitter follower power output stage.

COMPENSATION

Frequency compensation of the OP-07 is accomplished using three capacitors. Feedforward capacitor C3 bypasses the second stage lateral pnp's at high frequencies and, therefore, the excessive phase-shift normally associated with these transistors is circumvented. The dominant pole of the amplifier is set by C_2 which feed back around the second and driver stages and rolls off the open loop response at 20dB decade. The presence of C_1 ensures that the high frequency signal path is single-ended by rolling off the response of one side of the input stage. The total internal capacitance on the 100 X 53 mil chip is 210pF, a remarkable amount for a monolithic device.

LAYOUT

The circuit layout has thermal symmetry, a concept which has been used quite extensively on precision amplifier designs since its inception in 1969.[1] Variations in power dissipation in the driver and output stages, and the resultant thermal gradients affect the critical input transistors identically, thereby preventing offset voltage changes at the input.

INTERNAL NULLING TECHNIQUE

To understand the nulling technique some fundamental relationships should be examined using the equivalent circuit of Figure 3. (Errors caused by the second stage are effectively divided by the first stage gain and will be neglected in this discussion.) V_{OS} is defined as the voltage which must be applied between the input terminals to obtain zero voltage at the amplifier's output. Referring to Figure 3:

1. $V_{OS} = V_{be1} - V_{be2}$, V_{OUT} = zero

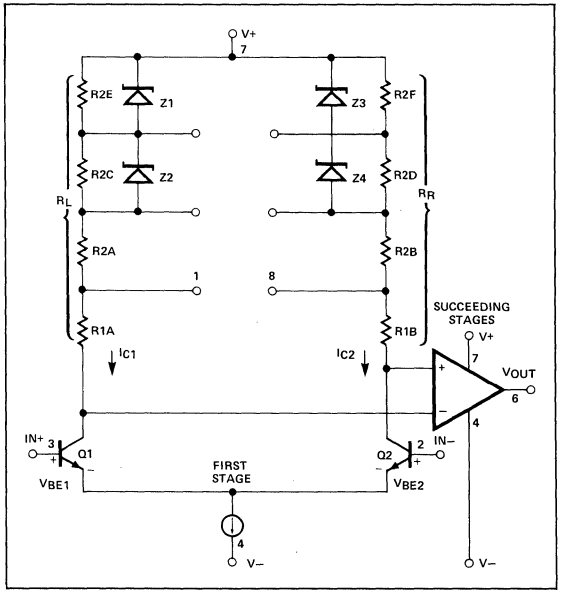


Figure 3. Offset Nulling Circuit

With an error free second stage it may be assumed that the input transistor collectors are equal in potential.

2. $I_{C1}R_L = I_{C2}R_R$ and $\frac{I_{C1}}{I_{C2}} = \frac{R_R}{R_L}$

3. $V_{be} = \frac{kT}{q} \log_e \left(\frac{I_{C1}}{I_{S1}}\right)$, $V_{be2} = \frac{kT}{q} \log_e \left(\frac{I_{C2}}{I_{S2}}\right)$,

   Provided $I_C/I_S >> 1$.

Substituting in Equation 1:

4. $V_{OS} = \frac{kT}{q} \log_e \left(\frac{I_{C1}}{I_{S1}}\right) - \frac{kT}{q} \log_e \left(\frac{I_{C2}}{I_{S2}}\right)$

Rewriting:

5. $V_{OS} = \frac{kT}{q} \log_e \left(\frac{I_{C1}}{I_{C1}} \cdot \frac{I_{S2}}{I_{S1}}\right)$

Substituting from Equation 2:

6. $V_{OS} = \frac{kT}{q} \log_e \left(\frac{R_R}{R_L} \cdot \frac{I_{S2}}{I_{S1}}\right)$

For V_{OS} = zero:

7. $\frac{R_R}{R_L} \cdot \frac{I_{S2}}{I_{S1}} = 1$

Where:

k = Boltzmann's constant = 1.38 X 10^{-23} joules/°K

T = Absolute temperature, °K

q = Charge of an electron = 1.6 X 10^{-19} coulomb

I_S = Theoretical reverse-saturation current

I_C = Collector Current

Therefore, by adjusting the ratio of $\frac{R_R}{R_L}$ the inherent processing-related differences in I_{S1} and I_{S2} which cause V_{be} differentials may be cancelled. Earlier amplifier designs achieved the adjustment of collector resistance by an external nulling potentiometer between Pin 1 and Pin 8 with its wiper connected to Pin 7 (Figure 1).

In the OP-07, permanent nulling is accomplished by shorting out a small percentage of R_R or R_L as determined by a computer programmed with Equation 6 and a lookup table. This is done by reading V_{OS} before trimming, comparing its magnitude and polarity with a lookup table value, and shorting out one of the normally nonconducting zener diodes. The short is created by passing a high current pulse through the selected zener, fusing its metal contacts into the silicon as shown in Figure 4. High volume production is achieved through automation, with initial device testing at wafer probe including V_{OS} trimming requiring less than one second.

Through this technique, V_{OS} of the entire "raw" OP-07 distribution can be nulled to less than 150μV, with the majority being under 75μV. Prime grade yields are high, providing adequate numbers of OP-07A devices with a V_{OS} maximum of 25μV.

PERFORMANCE

The specifications in Table 1 and curves of Figure 5 show noise, initial V_{OS}, and long-term stability performance unsurpassed by any other monolithic op amp. This device is free of

[1] **Editor's note:** This concept was originally introduced by George Erdi during employment at Fairchild Semiconductor Research and Development.

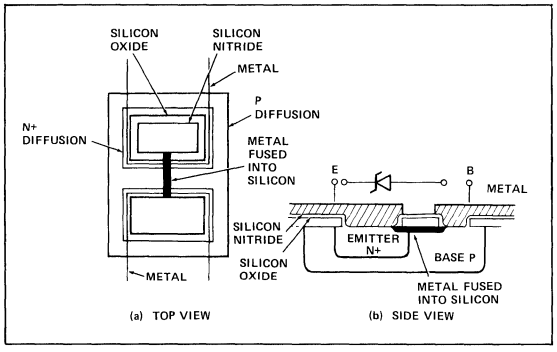


Figure 4. Short-Circuiting of Zener Diodes

Table 1. OP-07A Performance

OP-07 Performance @ V_S = ±15V, T_A = 25°C			
Parameter	**Typical**	**Min/Max**	**Units**
Offset Voltage, V_{OS}	10	25	μV
Drift with Temperature	0.2	0.6	μV/°C
Drift with Time	0.2	1.0	μV/mo
Offset Current, I_{OS}	0.3	2.0	nA
Drift with Temperature	5	25	pA/°C
Input bias current, I_B	±0.7	±2.0	nA
Noise Voltage 0.1Hz to 10Hz	0.35	0.6	μV_{p-p}
Noise Current 0.1Hz to 10Hz	14	30	pA_{p-p}
Input Resistance — Differential	80	30	MΩ
Input Resistance — Common Mode	200	—	GΩ
Common-Mode Rejection	126	110	dB
Power Supply Rejection	110	100	dB
Voltage Gain	500	300	V/mV
Slew Rate	0.25	—	V/μs
Unity Gain Bandwidth	1.2	—	MHz

the common problems of latchup, noise, compensation capacitors, and narrow power supply limitations. Power supply rejection ratio (PSRR) exceeds 100dB over the unusually wide range of ±3 to ±18 volts. Common-mode rejection is specified over a full ±13 volt input range allowing small signal amplification in high noise environments and use in inverting, non-inverting, and differential applications. The amplifier is completely self-contained — no external compensation or protection components are required. It is an excellent replacement for chopper-stabilized amplifiers where reductions in cost, noise, size, and power consumption are desired, and for monolithic op amps where elimination of the offset nulling potentiometer is desirable.

The pinout of the OP-07 allows direct replacement of 725, 108, and OP-05 types without circuit changes while 741 devices may be replaced by removal of the nulling potentiometer. HA-2900 series chopper-stabilized amplifiers may be replaced by removing the two 0.1μF capacitors and the 1500pF capacitor whenever cost or noise reductions are required. Table 2 is included to show comparative performance in wide temperature range applications.

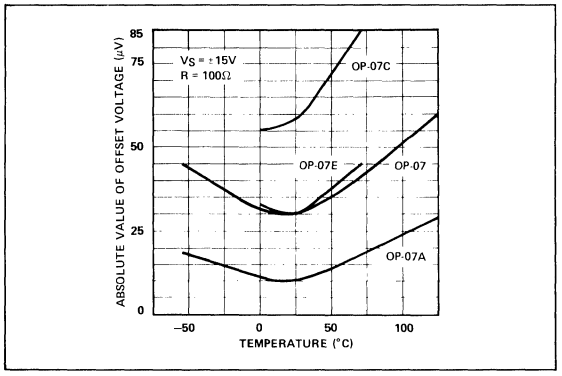


Figure 5A. Untrimmed Offset Voltage vs Temperature

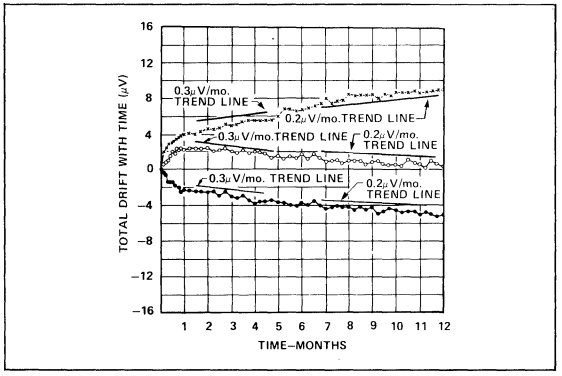


Figure 5B. Offset Voltage Stability vs Time

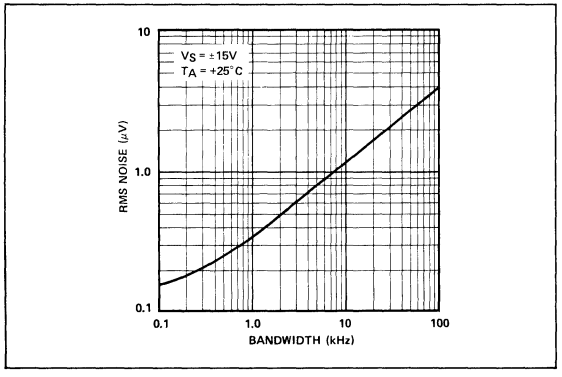


Figure 5C. Input Wideband Noise vs Bandwidth (0.1Hz to Frequency Indicated)

Table 3 compares various OP-07 versions with competitive op amps and over the 0°/70°C temperature range. An absence of noise and long-term stability specifications for

some amplifiers should caution potential users of possible deficiencies in those areas. This same comment would apply to "typical-only" specifications since accurate predictions of circuit performance can only be made with a fully specified device.

PERFORMANCE

The low frequency noise photograph in Figure 6A shows $0.35\mu V_{p-p}$ input voltage noise (0.1Hz to 10Hz), the best performance available in an instrumentation op amp at this writing. The wideband voltage noise comparison photograph (Figure 7A) shows relative performance of a OP-07 and a monolithic chopper in the same X100 configuration; the chopper is seen to have at least $200\mu V_{p-p}$ noise referred to the input. Clearly, low V_{OS} specifications are not very meaningful if input voltage noise is the predominant error factor.

Chopper-frequency noise is a common mode current noise occurring at the chopping frequency due to switching transients. The effect of a 500kΩ source mismatch is shown in the wideband curent noise photograph comparing a OP-07 with a monolithic chopper in the non-inverting buffer application (Figure 7B). High source impedance circuits require low

Table 2. Military Temperature Range Performance Comparison

Manufacturer's Part Number	V_{OS} Maximum −55°/+125°C	TCV_{OS} Maximum −55°/+125°C (Unnulled)	Voltage Noise Typical F = 10Hz	Current Noise Typical F = 10Hz	I_{Bias} Maximum −55°/+125°C	Long-Term Drift Typical
OP-07A	60μV	0.6μV/°C	10.3nV/√Hz	0.32pA/√Hz	4nA	0.2μV/mo
OP-07	200μV	1.3μV/°C	10.3nV/√Hz	0.32pA/√Hz	6nA	0.2μV/mo
HA-2900	60μV	0.6μV/°C	900nV/√Hz	Not Specified (Chopper)	1nA	Not Specified
OP-05A	240μV	0.9μV/°C	10.3nV/√Hz	0.32pA √Hz	4nA	0.2μV/mo
OP-05	700μV	2.0μV/°C	10.3nV/√Hz	0.32pA/√Hz	6nA	0.2μV/mo
μA725	1500μV	5.0μV/°C	15nV/√Hz	1.0pA/√Hz	200nA	Not Specified
LM108A	1000μV	5.0μV/°C	43nV/√Hz	Not Specified	3nA	Not Specified

Table 3. Commercial Temperature Range Performance Comparison

Manufacturer's Part Number		V_{OS} Maximum 0°/70°C	Long Term Drift Typical	Long Term Typical Maximum	Voltage Noise Maximum 0.1Hz to 10Hz	Voltage Noise Maximum 0.1Hz to 10Hz
OP-07A	(M)	45μV	0.2μV/mo	1.0μV/mo	$0.35\mu V_{p-p}$	$0.6\mu V_{p-p}$
OP-07	(M)	130μV	0.2μV/mo	1.0μV/mo	$0.35\mu V_{p-p}$	$0.6\mu V_{p-p}$
OP-07E	(C)	130μV	0.3μV/mo	1.5μV/mo	$0.35\mu V_{p-p}$	$0.6\mu V_{p-p}$
OP-07C	(C)	250μV	0.4μV/mo	2.0μV/mo	$0.38\mu V_{p-p}$	$0.65\mu V_{p-p}$
LM108A	(M)	725μV	Not Specified	Not Specified	Not Specified	Not Specified
HA-2900 Chopper-Stabilized	(M)	60μV	Not Specified	Not Specified	$35\mu V_{p-p}$	Not Specified
HA-2905 Chopper-Stabilized	(C)	80μV	Not Specified	Not Specified	$35\mu V_{p-p}$	Not Specified
AD504M	(C)	545μV	10μV/mo	Not Specified	Not Specified	$0.6\mu V_{p-p}$
AD508L	(C)	612μV	Not Specified	10μV/mo	$1.0\mu V_{p-p}$	Not Specified
Typical Inverting-Only Chopper Module	(C)	95μV	2.0μV/mo	Not Specified	$1.7\mu V_{p-p}$	Not Specified

M = 55°/+125°C Range Device
C = 0°/+70°C Range Device

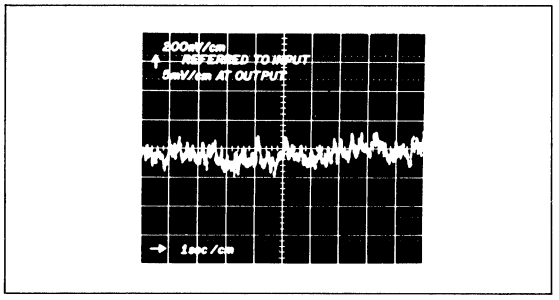


Figure 6A. Low Frequency Noise

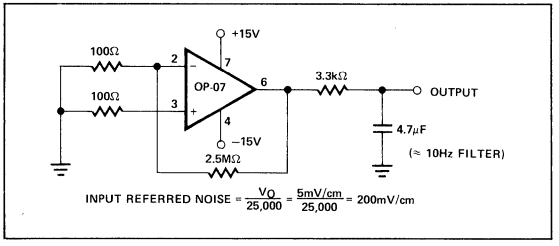


Figure 6B. Low Frequency Noise Test Circuit

input noise currents, which as the photograph illustrates, can be larger than input bias current with certain operational amplifiers.

LONG-TERM V_{OS} DRIFT

Input offset voltage drift over time has three components: warmup drift, first month drift, and trend line stability.

Warmup drift is a change in V_{OS} occurring in the first few minutes of operation. In order to produce high volumes of OP-07s, V_{OS} is measured 0.5 seconds after application of power using automated test equipment. The pass limits are "guardbanded" or made small enough with respect to V_{OS} maximum specification to compensate for not having directly observed warmup drift.

The first month stability, defined as changes in V_{OS} from one hour to 30 days, is typically 2.5μV. Even with closely maintained equipment, individual measurements with time can suffer from inaccuracies on the order of a half-microvolt due to low frequency noise and slight temperature variations. Fortunately, over a large number of measurements, these errors tend to integrate out, and an accurate trend line can be defined.

The trend line is defined as the drift per month averaged over the month one to month twelve period, and is generally an order of magnitude better than the first month drift (Figure 5B). Over 1.7 million device hours of testing and characterization have been logged in order to accurately specify long-term V_{OS} stability. Results indicate an average trend line drift of 0.2μV/month-outstanding stability performance for any amplifier, regardless of its technological approach.

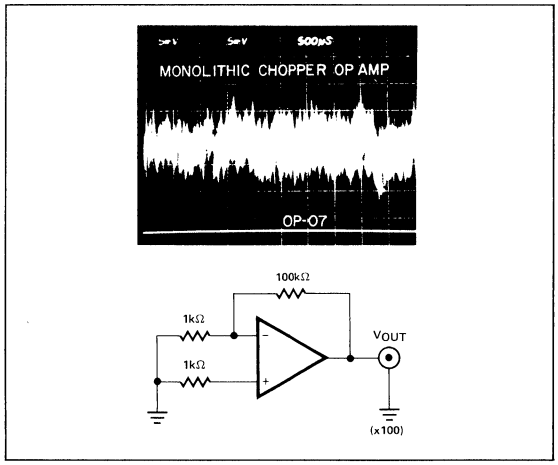


Figure 7A. Wideband Voltage Noise vs Chopper

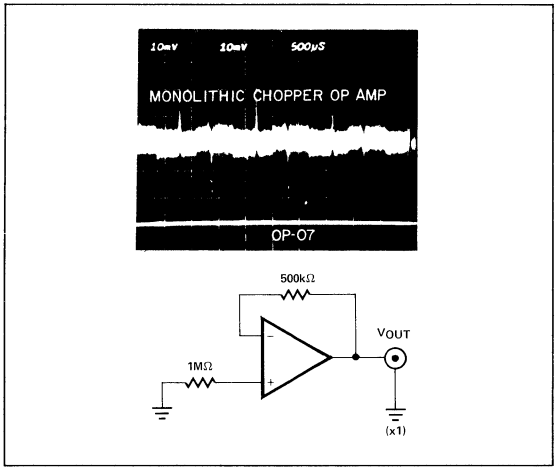


Figure 7B. Wideband Current Noise vs Chopper

LONG-TERM V_{OS} TESTING CONDITIONS

The deceptively simple circuit of Figure 8 is used for long-term V_{OS} stability testing. Three absolutely essential conditions must exist for accurate measurements: still air, power supply accuracy, and long-term temperature control.

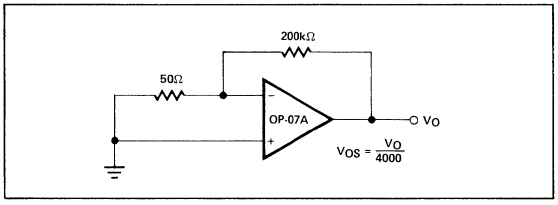


Figure 8. Long-Term Offset Voltage Test Circuit

All components, including sockets and solder joints, are enclosed in a metal box to eliminate air movement and temperature gradients. Thermoelectric error voltages may be generated if the dissimilar metal junctions formed by solder joints and socket contacts are at different temperatures. This effect is minimized by using "low thermal" solder (70% Cadmium, 30% Tin) and nonmetallic flux, such as Kester #1544, to avoid ionic contamination.

Although the power supply rejection ratio (PSRR) of the OP-07 is extremely high, nevertheless it should be considered as a potential error factor in long-term V_{OS} testing. The power supplies are verified to be at ±10mV before each set of weekly readings. This removes any possible significant errors due to the PSRR specification of 110dB (3μV/Volt).

All long-term V_{OS} testing is performed in a controlled laboratory environment of 30° C to eliminate TCV_{OS}, 0.2μV/° C, as an error possibility.

APPLICATIONS OF OP-07

HIGH STABILITY VOLTAGE REFERENCE

The simple bootstrapped voltage reference of Figure 9 provides a precise 10 volts virtually independent of changes in power supply voltage, ambient temperature, and output loading. Correct zener operating current of exactly 2mA is maintained by R1, a selected 5ppm/° C resistor, connected to the regulated output. Accuracy is primarily determined by three factors: the 5ppm/° C temperature coefficient of D1, 1ppm/° C ratio tracking of R2 and R3, and operational amplifier V_{OS} errors.

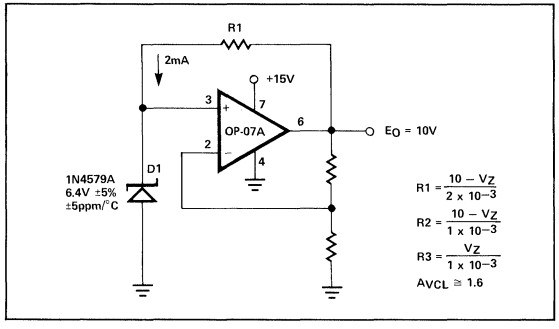


Figure 9. High Stability Voltage Reference

V_{OS} errors, amplified by 1.6 (A_{VCL}), appear at the output and can be significant with most monolithic amplifiers. For example: an ordinary amplifier with TCV_{OS} of 5μV/° C contributes 0.8ppm/° C of output error while the OP-07 at 0.3μV/° C (0.5ppm/° C) effectively eliminates TCV_{OS} as an error consideration.

Perhaps the most easily overlooked accuracy requirement in this and many other critical circuits is long-term V_{OS} stability. In this circuit, a 741 drifting at 100μV/mo would cause 200ppm/year of output drift — a very large amount. This type of problem is particularly troublesome in potted subassemblies where periodic recalibration is impossible. Use of the OP-07 at 1μV/mo maximum avoids this potentially troublesome condition.

LARGE SIGNAL BUFFER — 0.005% WORST-CASE ACCURACY

Unity gain large-signal buffers are one of the most common applications of operational amplifiers. The low V_{OS} and high CMRR of the OP-07 provide high accuracy, and small physical size is achieved due to the complete absence of external components. Performance over the appropriate temperature range is shown for the various OP-07 selections. Note that the errors on Table 4 are absolute worst-case numbers, a combination that would be extremely unlikely in actual practice. A figure closer to expected overall performance based on the RMS sum of typical errors is also included. Typical

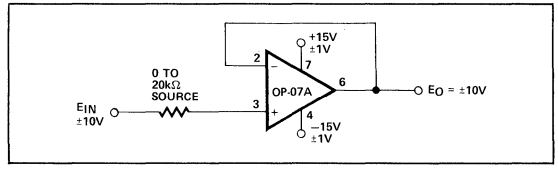


Figure 10. Large Signal Voltage Buffer

Table 4. Large Signal Voltage Buffer Error Analysis

Error Source	OP-07A -55°/+125°		OP-07 -55°/+125°		OP-07E 0°/+70°		OP-07C 0°/+70°	
	Min/Max	Typical	Min/Max	Typical	Min/Max	Typical	Min/Max	Typical
V_{OS}[1]	60μV	25μV	200μV	60μV	130μV	45μV	250μV	85μV
I_{Bias}[1]	80μV	20μV	120μV	40μV	110μV	30μV	180μV	44μV
CMRR[1]	50μV	7μV	50μV	7μV	70μV	7μV	141μV	10μV
PSRR[1]	40μV	10μV	40μV	10μV	63μV	13μV	100μV	20μV
Gain[1]	50μV	25μV	67μV	25μV	56μV	22μV	100μV	25μV
ΔV_{OS} 5 Years	60μV	12μV	60μV	12μV	90μV	18μV	120μV	24μV
Total	340μV	44μV*	537μV	78μV*	519μV	63μV*	891μV	104μV*
Percent Full Scale	0.0034%	0.0005%*	0.0054%	0.0008%*	0.0052%	0.0006%*	0.009%	0.001%*

*RMS Calculation

[1]Full operating temperature range specification.

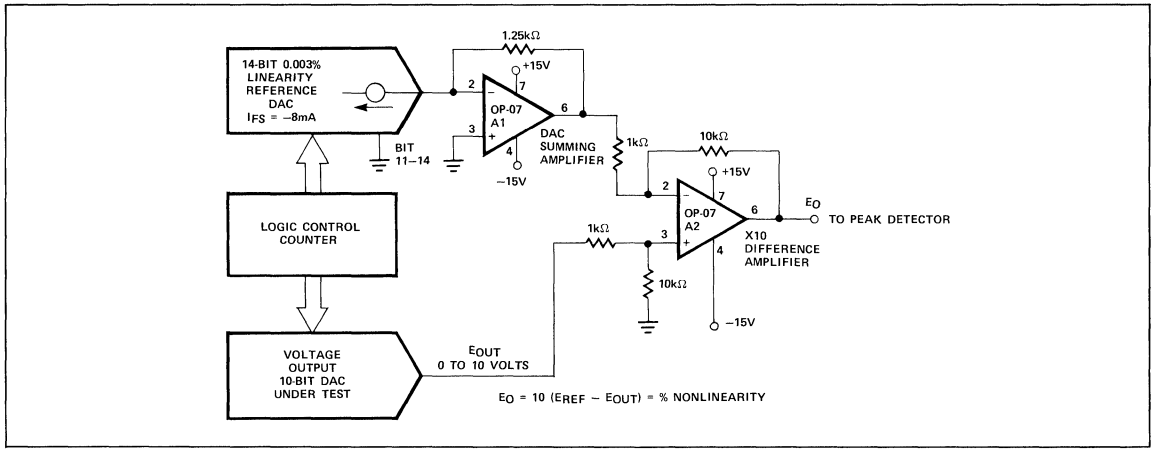


Figure 11. D/A Converter Test System

military temperature range error for the OP-07A is 44μV —far smaller than most other amplifiers' input offset voltage error alone.

CALIBRATION-FREE DAC SYSTEM

The circuit of Figure 11 is part of an automated test system used for measuring 6-bit to 10-bit DAC nonlinearity at each possible digital input code combination. It detects the largest difference between a 14-bit linear reference DAC and a unit under test, and generates an output voltage that is directly proportional to nonlinearity as a percentage of full scale.

Reference DACs are frequently supplied having current-output only, with selection of a summing amplifier left up to the user. Summing amplifier characteristics must not cause degradation of reference DAC linearity, full-scale, or zero scale performance or erroneous testing could occur. In addition, V_{OS} errors are direct zero scale output errors, so both long-term V_{OS} stability and drift over temperature are important. Using a OP-07, total E_{REF} errors due to op amp performance are estimated at less than 100μV or 0.2 LSB on a 14-bit base, permanently eliminating zero calibration while maintaining test system accuracy. Summing amplifier applications requiring higher speed should use the composite amplifier of Figure 12.

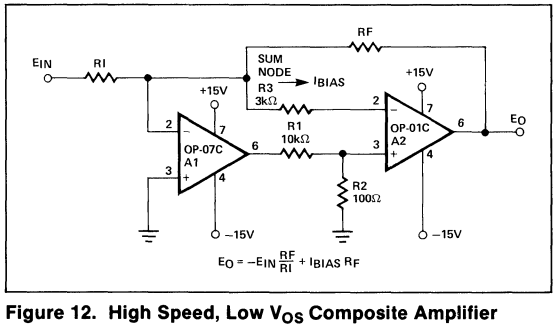


Figure 12. High Speed, Low V_{OS} Composite Amplifier

Another 0P-07 is used in the dfference amplifier for high common mode rejection and V_{OS} stability. This op amp is well-suited for critical test system circuits, providing accurate measurements, high reliability, and calibration-free operation.

COMPOSITE SUMMING AND AMPLIFIER WITH HIGH SLEW RATE AND LOW V_{OS}

The circuit configuration of Figure 12 is a method for obtaining a 18V/μs slew rate with OP-07 V_{OS} characteristics. V_{OS} of A2 (3mV) is continuously nulled by forcing the sum node to equal V_{OS} of A1 through a secondary feedback loop formed by R1, R2, A2's input stage, and R3. An error due to I_{Bias} of A2 limits practical values of feedback resistances to a maximum of 5kΩ in most applications; a fast FET input op amp could be used as A2 to reduce the circuit's bias current to approximately 2nA. The circuit is also good as a current-output DAC summing amplifier because zero scale offset adjustments are not required and high speed is preserved. Composite connections such as this are generally quite cost-effective compared to single op amps having both high slew rate and good V_{OS} specifications.

ABSOLUTE VALUE CIRCUIT WITH MINIMUM ERROR

This circuit provides precise full-wave rectification by inverting negative-polarity input voltages and operating as a unity-gain buffer for positive-polarity inputs. It is useful for conditioning inputs to unipolar A to D's, positive peak detectors, single quadrant multipliers, and magnitude-only measurement systems. A polarity indication for sign plus magnitude applications is present at the output of A1.

For a positive input, the circuit operates as two stages of inverting unity-gain amplification. As the input goes positive, the output of A1 becomes negative, turning D2 off and D1 on, placing the junction of R3 and R4 at $-E_{IN}$. V_A is at zero volts because D2 is off and only insignificant A2 bias current flows in R2. A2 operates as a second inverting unity-gain stage and E_O equals E_{IN}.

For negative inputs, the first stage gain to point V_A is -2/3 because D2 is on, D1 is off, and 1/3 of the input current, $E_{IN}/R1$, flows in R3 and R4. The second stage is operated in a non-inverting gain of 1.5 configuration with V_A as its input, giving an over-all circuit gain of -1.

Using conventional op amps, input offset voltage is usually the predominent error factor because it is doubled and added to E_{IN}. For example, with E_{IN} of 100mV, only 0.5mV of V_{OS} will cause 1% output error. Clearly, A1 and A2 must be low V_{OS} op amps to achieve high accuracy over the full input voltage range. By using a OP-07, performance is mainly a function of resistor ratio matching and diode leakages. Gain errors due to resistor matching will typically be less than 0.3% when R2-R4 are within 0.01% of R1's value. Low leakage diodes should be used to prevent errors from reverse current flow in R2 or R3 which would appear as V_{OS} error of A2.

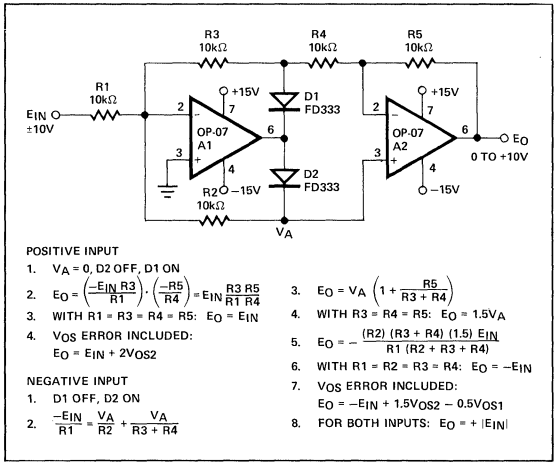


Figure 13. Precision Absolute Value Circuit

PRECISION SUMMING AMPLIFIER WITH NO ADJUSTMENTS

Figure 14 shows the basic op amp connection for analog computation, a precision summing amplifier. Analog computers use several of these stages connected in combinations to produce continuous outputs that are a function of multiple input variables. Single-stage accuracy is important because errors accumulate throughout a system and determine its over-all performance. Some analog computers require time-consuming and annoying recalibration of each stage at weekly or monthly intervals to compensate for long-term V_{OS} drift. This circuit, with 1μV to 2μV per month maximum change in V_{OS}, completely eliminates periodic calibration while insuring long-term accuracy.

Single-stage maximum full scale errors contributed by the op amp range from 0.001% for a OP-07A to 0.004% for a OP-07C. This makes resistor-related errors of ratio matching and temperature tracking the major accuracy considerations. Instrumentation quality operational amplifiers with ultra-low V_{OS} allow simple construction of high performance summing and differencing amplifiers.

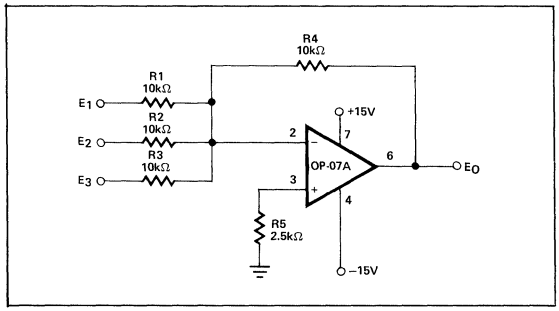


Figure 14. Adjustment-Free Precision Summing Amplifier

INSTRUMENTATION AMPLIFIERS FOR THERMOCOUPLES

Thermocouples are very low voltage output temperature transducers requiring differential DC amplification before linearization and display. Typical full scale outputs are under 50mV with some types having as low as 5μV/°C sensitivity.

These very small input signals often have sizable common mode voltages present because the thermocouples are frequently located in high-noise industrial environments. The single op-amp instrumentation amplifier of Figure 15 has the high common mode rejection and long-term accuracy required for this stringent application.

The amplifier achieves about 100dB of common mode voltage rejection over a full ±13 volt range when the ratios of R2/R1 and R4/R3 are matched within 0.01%. R1B and R3B are usually around 1kΩ, a value large in respect to line resistance but small enough to make voltage drops from input bias currents negligible. Input voltages and V_{OS} are both amplified by 200 so V_{OS} changes, either long-term or due to temperature, can cause direct output error. For example, with a 5μV/°C thermocouple, the OP-07A holds this error factor to 0.05°C/year and 1°C for an amplifier operating temperature range of 100°C (-25°C to +75°C) — a typical industrial environment. For 0°C to 70°C applications, the low-cost OP-07C holds output error due to a change in V_{OS} below 1°C/year and 2°C over the full commercial operating temperature range.

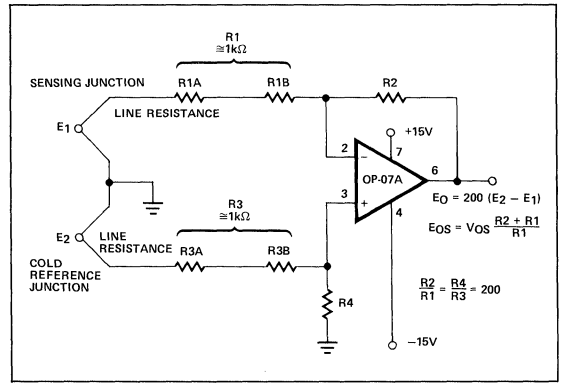


Figure 15. High Stability Thermocouple Amplifier

The circuit is useful whenever small differential signals from low-impedance sources must be accurately amplified in the presence of large common mode voltages.

CONCLUSIONS

The OP-07 Ultra-Low Offset Voltage Operational Amplifier is a cost-effective monolithic alternative to the chopper-stabilized amplifier and is suitable for a wide variety of critical applications. An internal trimming procedure achieves significant improvements over previous bipolar designs in offset voltage, noise levels, and long-term stability at a moderate cost. For the first time, a complete precision IC op amp is available requiring no external components whatsoever for general application, thus increasing reliability by decreasing system complexity. The adjustment-free, fully interchangeable device allows tremendous simplification of calibration and field servicing procedures. This is a most powerful and cost-effective design tool — chopper-type performance and bipolar prices with 741 ease-of-operation.

REFERENCES

1. *Minimizing Offset Voltage Drift with Temperature in Monolithic Operational Amplifiers,* G. Erdi, Proceedings of the National Electronic Conference, Volume 25, 1969
2. *A Low Drift, Low Noise Monolithic Operational Amplifier for Low Level Signal Processing,* G. Erdi, Fairchild Semiconductor Application Brief #136, July 1969

PMI

AN-14

INTERFACING BIPOLAR TECHNOLOGY D/A CONVERTERS WITH CMOS LOGIC

Precision Monolithics Inc.

APPLICATION NOTE 14

The rise in popularity of CMOS logic has created a demand for digital-to-analog converters with CMOS-compatible logic inputs. PMI DACs incorporate bipolar technology but are designed to allow simple CMOS interfacing in most applications. Since interfacing is easily achieved, the proven advantages of low-cost and high speed are available to both TTL and CMOS system designers. Typical TTL input logic levels of bipolar DACs provide about 1.2 volts of noise margin. In order to increase this noise margin, this application note discusses interfacing methods and rules for both voltage and current output types and describes several typical CMOS system applications.

INTERFACING THE DAC-08/20

The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V– = –15V, the logic inputs may swing between –10V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-08 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V– plus (I_{REF} · 1kΩ) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic control pin (Pin 1, V_{LC}). It should be noted that Pin 1 will source approximately 100μA; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when Pin 1 sees a low impedance. If Pin 1 is connected to a resistive divider, as in Figure 1, it should be bypassed to ground by a 0.1μF capacitor.

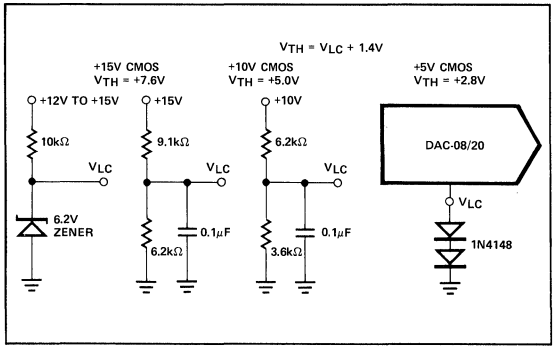


Figure 1. DAC-08/20 CMOS Interfacing with True CMOS Threshold

INTERFACING THE DAC-86/88/89

These companding D/A converters are similar to the DAC-08 in that the input logic threshold is two diode drops positive with respect to the logic control pin. However, more current flows into the logic control pin requiring active current sourcing as shown below.

V_{LC} (Pin 10) is placed as a potential which is 1.4V below the desired logic input switching threshold. However, this voltage source must be capable of sourcing and sinking a changing current at Pin 10. The negative voltage at the logic inputs must be limited to +10V with respect to V– (Pin 13).

INTERFACING THE DAC-210

Use the same circuit as in Figure 2 except connect to Digital Ground, Pin 11. Input logic threshold will be 1.4V above the potential at Pin 11.

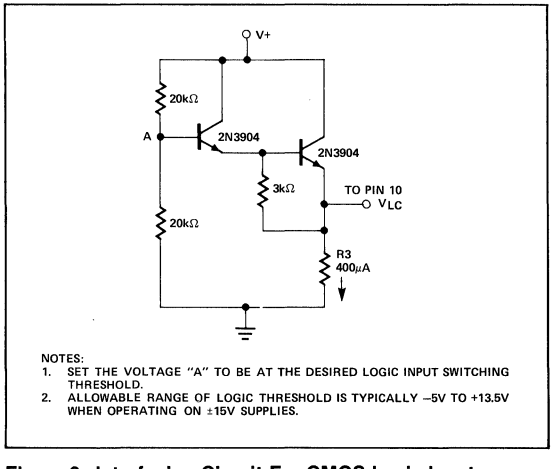


Figure 2. Interfacing Circuit For CMOS Logic Inputs

INTERFACING THE DAC-02/03/05/06

Five complete voltage output monolithic DACs are described in this section: the DAC-02/05 and DAC-03, 10-bit plus sign devices, and the DAC-06 10-bit two's complement coded converter. These DACs are well-suited to use in CMOS systems as their complete, internal temperature-compensated references eliminate the external reference voltage requirement, a major source of power dissipation, drift, and cost in some CMOS compatible designs.

These DACs have logic input stages which require about 1μA and are capable of operation with inputs between −5 volts and V+ less 0.7 volt. This wide input voltage range allows direct CMOS interfacing in many applications, the exception being where the CMOS logic and D/A converter must use the same power supply.

In this special case, the diode should be placed in series with the CMOS driving device's V_{DD} lead as shown in Figure 3. The diode limits V_{DD} to V+ less 0.7 volt — since the output from the CMOS device cannot exceed this value, the DAC's maximum input voltage rule is satisfied. Summarizing: in all applications, these high-speed DACs require either no interfacing components, or, at most, a single inexpensive diode for full CMOS compatibility.

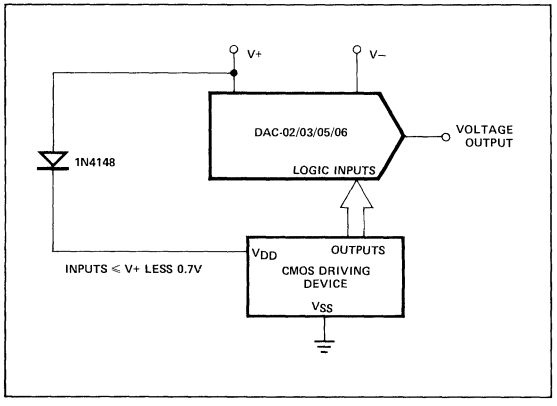


Figure 3. DAC-02/03/05/06 CMOS Interfacing

INTERFACING THE DAC-100 AND DAC-01

The DAC-100, a complete 10-bit monolithic fast current output DAC is available in a wide range of electrical grades and packages. This device requires only about 1μA of input current into each logic stage. Similar logic input stages are used in the DAC-01, a complete voltage output 6-bit DAC. One rule must be observed when interfacing these DACs with CMOS inputs: logic input voltages should not exceed 6.5 volts or V+, whichever is smaller. To provide an understanding of this rule, it is necessary to discuss the logic input stage design.

DAC-100 LOGIC INPUT STAGE DESIGN

For simplicity, only one of the ten identical input circuits is shown in Figure 4. The DAC-100 uses a fast current-steering technique that switches a bit-weighted current between the positive supply (V+) and the analog output, which is usually constrained to be at zero volts (virtual ground) by an external summing amplifier.

Switching is accomplished by forward biasing Q4, a diode-connected transistor, for the bit "ON" condition and back biasing Q4 in the "OFF" condition. For the "ON" condition

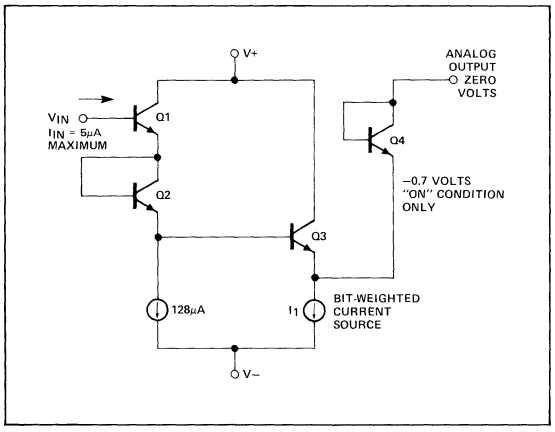


Figure 4. DAC-100 Logic Input Stage

($V_{IN} \leq 0.7$ volts), Q3 is "OFF" — all of the bit-weighted current, I_1, flows from the analog output through Q4 and ultimately to V−. In the "OFF" condition ($V_{IN} \leq 2.1$ volts), Q3 is "ON", Q4 is back biased, and the bit-weighted current is sourced from the positive power supply instead of the analog output.

If V_{IN} is too high, Q4's emitter-base junction will experience reverse breakdown and a fault condition will occur. Equation 1 describes this condition:

1. $BV_{IH} = V_{BE1} + V_{BE2} + V_{BE3} + BV_{EB4} \cong 7.7$ volts

Using this relationship, it can be seen that a conservative input voltage limit would be around 6.5 volts. When the 6.5V input limited is observed, DAC-100 operation with CMOS inputs is easily achieved as demonstrated in the following applications section.

CMOS COMPATIBLE OPERATION OF DAC-100 WITH ±6 VOLT POWER SUPPLIES

This is the most convenient method of interfacing a DAC-100 with CMOS logic. At ±6 volts, DAC-100 power dissipation is only 80mW, which is very small considering the inclusion of a complete internal reference. No interfacing components are required with ±5% power supplies, and the CMOS logic and DAC-100 can use the same +6 volt power supply. In this application the device is directly CMOS compatible.

HIGH LEVEL CMOS INTERFACING

The block diagram in Figure 5 illustrates a convenient method for interfacing CMOS input levels between 6.5 volts and 15 volts with a DAC-100. Inexpensive and readily available CMOS hex buffer/converters step down the high-level inputs to TTL levels that cannot exceed 5 volts — clearly satisfying the input stage voltage rule.

In addition to level shifting, buffer/converters provide input coding flexibility since they are available as inverting

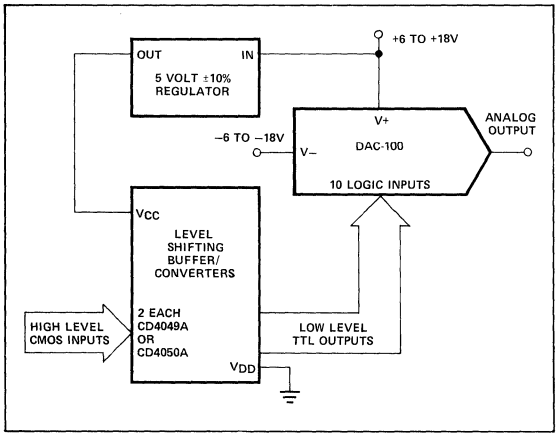


Figure 5. Block Diagram — CMOS to DAC-100 Interface

(CD4049A) or noninverting (CD4050A) devices. This gives the user a choice between negative-true and positive-true binary coding and allows the same basic DAC-100-to-CMOS interfacing method to be used in either type of application.

Since buffer/converter power consumption is very low, the required +5 volts can be provided by a simple regulator or even a resistive divider in some applications. In a multi-DAC system, one central, inexpensive 3-terminal IC regulator can supply several level shifting devices. Next, we will examine a complete circuit using all of these concepts in a high-speed CMOS compatible DAC.

COMPLETE CMOS COMPATIBLE DAC

The complete, 10-bit, voltage output DAC in Figure 6 has CMOS input compatibility, high speed, and low-cost. Current output from the DAC-100 is accurately converted to a voltage by the Precision Monolithics OP-01, a high speed op amp which has been specifically designed for the DAC summing amplifier application. Input offset voltage of this op amp is typically 2mV, eliminating the requirement for zero scale adjustment.

COMPLETE CMOS COMPATIBLE DAC DYNAMIC PERFORMANCE

The dynamic performance, as shown in the photograph, is quite good. Slew rate is 18V/μs while settling time to ±0.5% of full scale requires less than 1.5μs. DC performance is also

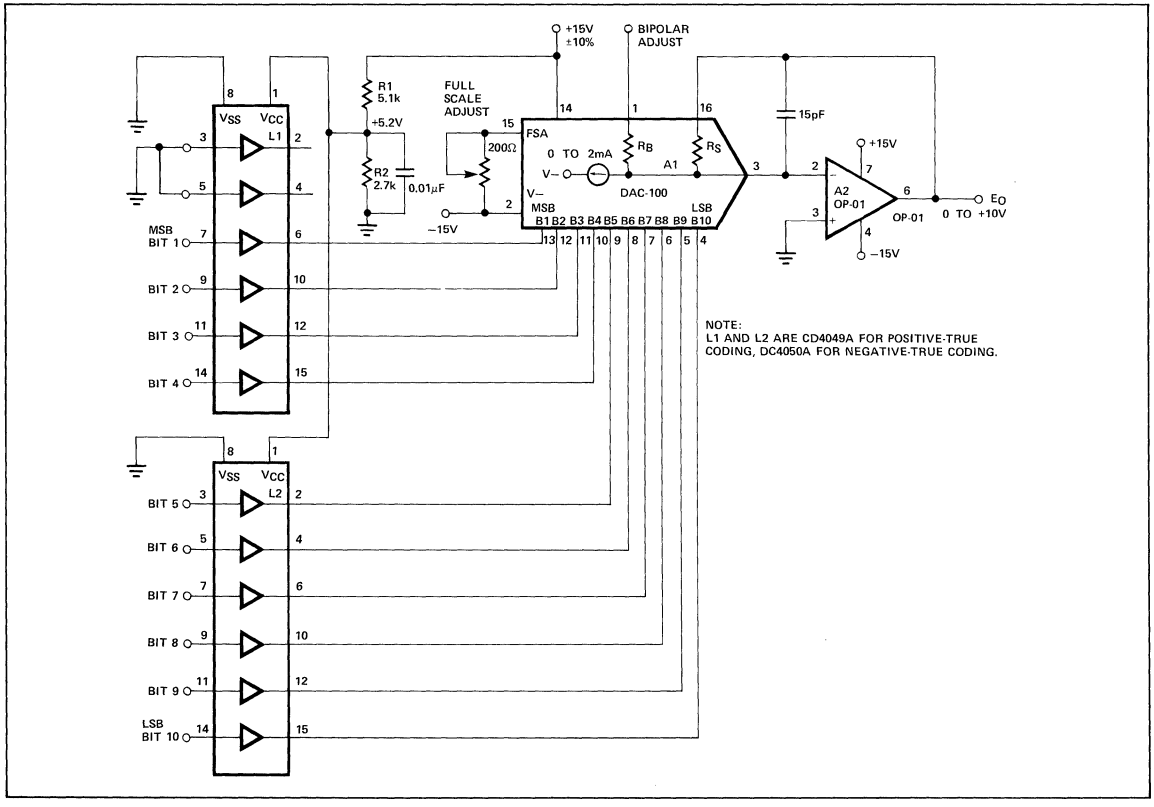
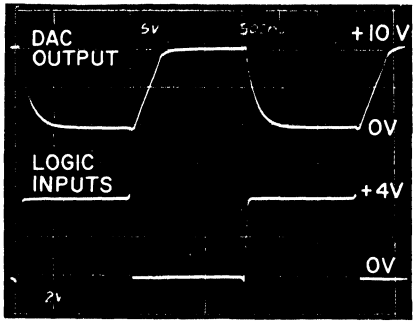


Figure 6. Interfacing DAC-100 with ±15 Volt CMOS Systems



good since DAC-100 nonlinearity is specified over the entire temperature range. In addition, the internal temperature-compensated voltage reference provides minimum full scale drift and decreases overall circuit complexity.

LOW COST THREE IC CMOS COMPATIBLE A/D CONVERTER

The diagram in Figure 7 is a modification of a previously published application note circuit substituting CMOS logic for TTL. All necessary logic for A to D conversion is contained in L1, a MC14559 CMOS successive approximation register. A conversion sequence is initiated by applying a positive pulse, with a width greater than one clock cycle, to the "Start Conversion" input. The analog input, applied to R_S and converted to a current, is compared successively to 1/2 scale, then 1/4 scale, and the remaining binarily-decreasing bit weights until it has been resolved within ±1/2LSB. At this time, "End of Conversion" changes to a logic "1" and the parallel answer is present in negative-true, binary-coded format at the register outputs.

Tracking A/D's may be similarly constructed using CD4029A up/down counters, a DAC-100, and a CMP-01 fast precision comparator.

CONCLUSION

Precision Monolithics D/A converters may be easily incorporated into CMOS systems. Low current logic input stage designs allow simple interfacing with a minimum of external components. The low power dissipation, high speed output and low cost make this line of monolithic DACs attractive in CMOS system designs.

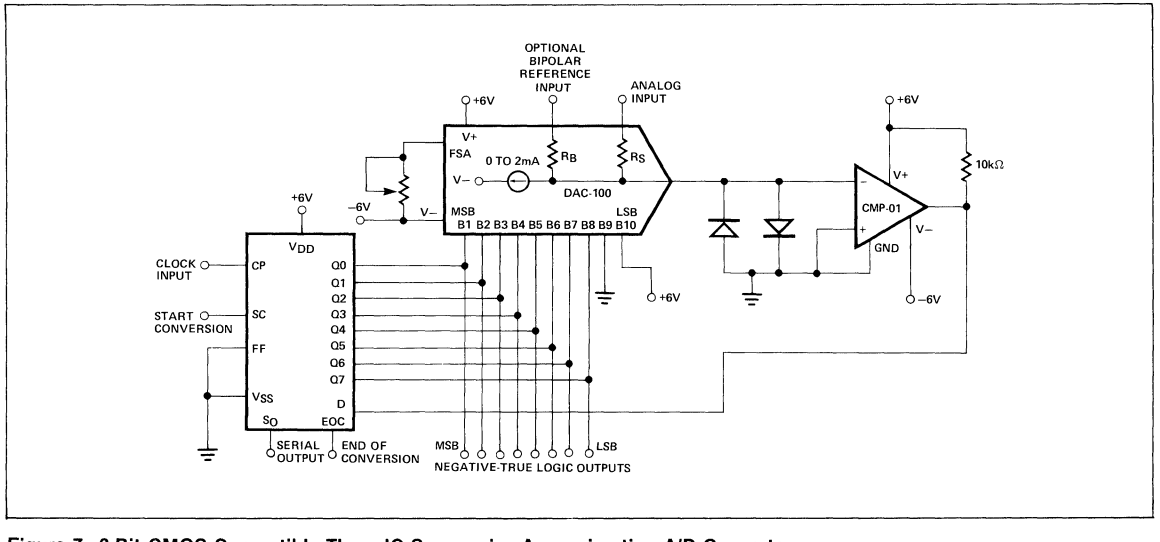


Figure 7. 8-Bit CMOS Compatible Three IC Successive Approximation A/D Converter

MINIMIZATION OF NOISE IN OPERATIONAL AMPLIFIER APPLICATIONS

Precision Monolithics Inc.

APPLICATION NOTE 15

INTRODUCTION

Since operational amplifier specifications such as Input Offset Voltage and Input Bias Current have improved tremendously in the past few years, noise is becoming an increasingly important error consideration. To take advantage of today's high performance op amps, an understanding of the noise mechanisms affecting op amps is required. This paper examines noise contributions, both internal and external to an op amp, and provides practical methods for minimizing their effects.

BASIC NOISE PROPERTIES

Noise, for purposes of this discussion, is defined as any signal appearing in an op amp's output that could not have been predicted by DC and AC input error analysis. Noise can be random or repetitive, internally or externally generated, current or voltage type, narrowband or wideband, high frequency or low frequency; whatever its nature, it can be minimized.

The first step in minimizing noise is source identification in terms of bandwidth and location in the frequency spectrum; some of the more common sources are shown in Figure 1, an 11-decade frequency spectrum chart. Some preliminary observations can be made: noise is present from DC to VHF from sources which may be identified in terms of bandwidth and frequency. Noise source bandwidths overlap, making noise a composite quantity at any given frequency. Most externally caused noise is repetitive rather than random and can be found at a definite frequency. Noise effects from external sources must be reduced to insignificant levels to realize the full performance available from a low noise op amp.

EXTERNAL NOISE SOURCES

Since noise is a composite signal, the individual sources must be identified to minimize their effects. For example, 60Hz power line pickup is a common interference noise appearing at an op amp's output as a 16ms sine wave. In this and most other situations, the basic tool for external noise source frequency characterization is the oscilloscope sweep rate setting. Recognizing the oscilloscope's potential in this area, Tektronix® manufactures an oscilloscope vertical amplifier with variable upper and lower −3dB points, which allows quick noise source frequency identification. Another basic identification tool is the simple low pass filter as shown in Figure 2, where the bandpass is calculated by:

$$(1)\quad f_O \cong \frac{1}{2\pi RC}$$

With such a filter, measurement bandpass can be changed from 10Hz to 100kHz (C = 4.7μF to 470pF), attenuating higher frequency components while passing frequencies of interest. Once identified, noise from an external source may be minimized by the methods outlined in Table 1—the external noise source chart.

Tektronix® is a registered trademark of Tektronix, Inc., Oregon.

FIGURE 1: Frequency Spectrum of Noise Sources Affecting Operational Amplifier Performance

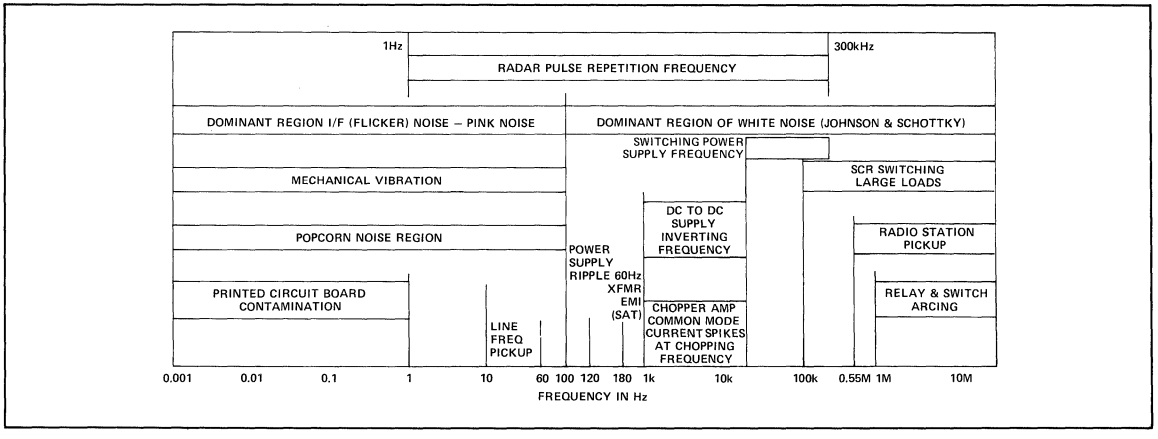


TABLE 1: External Noise Source Chart

Source	Nature	Causes	Minimization Methods
60Hz	Repetitive Interference	Powerlines physically close to op amp inputs. Poor CMRR at 60Hz. Power transformer primary-to-secondary capacitive coupling.	Reorientation of power wiring. Shielded transformers. Single point grounding. Battery power.
120Hz Ripple	Repetitive	Full wave rectifier ripple on op amp's supply terminals. Inadequate ripple consideration. Poor PSRR at 120Hz.	Thorough design to minimize ripple. RC decoupling at the op amp. Battery power.
180Hz	Repetitive EMI	180Hz radiated from saturated 60Hz transformers.	Physical reorientation of components. Shielding. Battery power.
Radio Stations	Standard AM Broadcast Through FM	Antenna action anyplace in system.	Shielding. Output filtering. Limited circuit bandwidth.
Relay and Switch Arcing	High Frequency Burst At Switching Rate	Proximity to amplifier inputs, power lines, compensation terminals, or nulling terminals.	Filtering of HF components. Shielding. Avoidance of ground loops. Arc suppressors at switching source.
Printed Circuit Board Contamination	Random Low Frequency	Dirty boards or sockets.	Thorough cleaning at time of soldering followed by a bakeout and humidity sealant.
Radar Transmitters	High Frequency Gated At Radar Pulse Repetition Rate	Radar transmitters from long range surface search to short range navigational—especially near airports.	Shielding. Output filtering of frequencies ≫ PRR.
Mechanical Vibration	Random < 100Hz	Loose connections, intermittent contact in mobile equipment.	Attention to connectors and cable conditions. Shock mounting in severe environments.
Chopper Frequency Noise	Common Mode Input Current At Chopping Frequency	Abnormally high noise chopper amplifier in system.	Balanced source resistors. Use bipolar input op amps instead. Use premium low noise chopper.
Switching Power Supply	Repetitive High Frequency Glitches In Supply And Ground	Improper ground return. Radiated noise from switching circuit.	Analog ground return to AC return. Shield power supply. Liberal power supply bypass at the op amp.

FIGURE 2: Noise Frequency Analysis RC Low Pass Filter

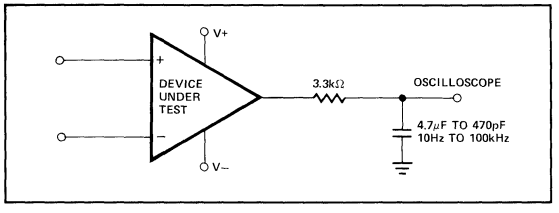
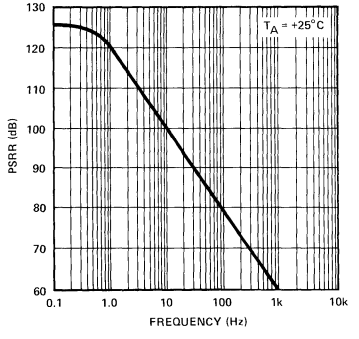


FIGURE 3: PSRR vs Frequency (OP-77)



Power Supply Ripple

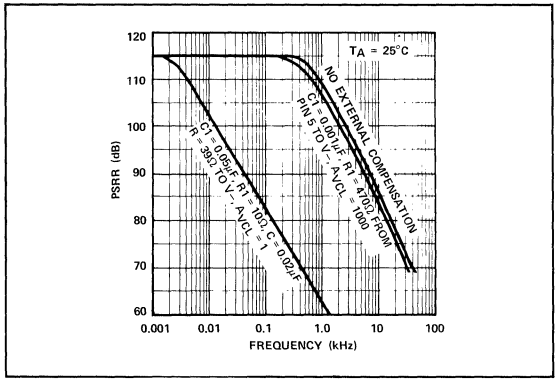
Power supply ripple at 120Hz is not usually thought of as a noise, but it should be. In an actual op amp application, it is quite possible to have a 120Hz noise component that is equal in magnitude to all other noise sources combined, and, for this reason, it deserves a special discussion.

To be negligible, 120Hz ripple noise should be between 10nV and 100nV referred to the input of an op amp. Achieving these low levels requires consideration of three factors: the op amp's 120Hz power supply rejection ratio (PSRR), the regulator's ripple rejection ratio, and finally, the regulator's input capacitor size.

PSRR at 120Hz for a given op amp may be found in the manufacturer's data sheet curves of PSRR versus frequency as shown in Figure 3. For the amplifier shown, 120Hz PSRR is about 76dB, and to attain a goal of 100nV referred to the input, ripple at the power terminals must be less than 0.6mV. Today's IC regulators provide about 60dB of ripple rejection; in this case the regulator input capacitor must be made large enough to limit input ripple to 0.6V.

Externally-compensated low noise op amps can provide improved 120Hz PSRR in high closed-loop gain configurations. The PSRR versus frequency curves of such an op amp are shown in Figure 4. When compensated for a closed-loop gain of 1000, 120Hz PSRR is 115dB. PSRR is still excellent at much higher frequencies allowing low ripple-noise operation in exceptionally severe environments.

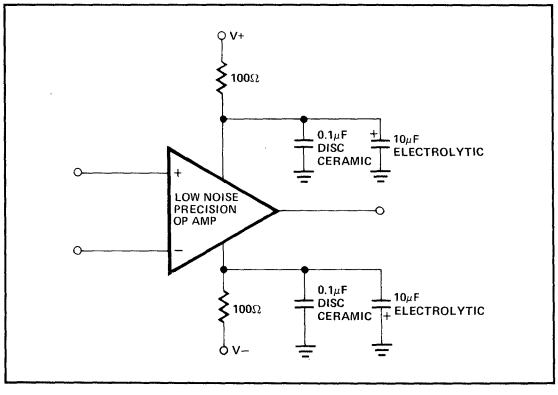
FIGURE 4: PSRR vs Frequency (OP-06)



Power Supply Bypassing

Usually, 120Hz ripple is not the only power supply associated noise. Series regulator output typically contain at least 150µV of noise in the 100Hz to 100kHz range; switching types contain even more. Unpredictable amounts of induced noise can also be present on power leads from many sources. Since high frequency PSRR decreases at 20dB/decade, these higher frequency supply noise components must not be allowed to reach the op amp's power terminals. RC decoupling, as shown in Figure 5, will adequately filter most wideband noise. Some caution must be exercised with this type of decoupling, as load current changes will modulate the voltage at the op amp's supply pins.

FIGURE 5: RC Decoupling



Power Supply Regulation

Any change in power supply voltage will have a resultant effect referred to an op amp's inputs. For the op amp of Figure 3, PSRR at DC is 126dB (0.5µV/V) which may be considered as a potential low frequency noise source. Power supplies for low noise op amp applications should, therefore, be both low in ripple and well-regulated. Inadequate supply regulation is often mistaken to be low frequency op amp noise.

When noise from external sources has been effectively minimized, further improvements in low noise performance are obtained by specifying the right op amp and through careful selection and application of the associated components.

OPERATIONAL AMPLIFIER INTERNAL NOISE

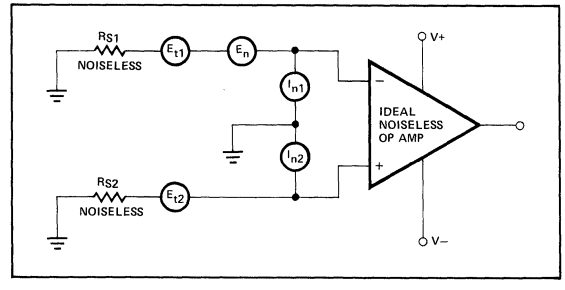
Most completely specified low-noise op amp data sheets specify current and voltage noises in a 1Hz bandwidth centered on 10Hz, 100Hz, and 1kHz, as well as low frequency noise over a range of 0.1Hz to 10Hz. To minimize total noise, a knowledge of the derivation of these specifications is useful. In this section, the reader is provided with an explanation of basic op amp-associated random noise mechanisms and introduced to a simplified method for calculating total input-referred noise in typical applications.

Op amp-associated noise currents and voltages are random in nature. They are aperiodic and uncorrelated to each other; and typically have Gaussian amplitude distributions, with the highest noise amplitudes having the lowest probability. There is a statistical relationship between the peak-to-peak value of random noise and its rms value. Where the amplitude distribution is Gaussian, the rms value may be multiplied by six to yield a peak-to-peak value that will not be exceeded 99.73% of the time (this is a handy rule-of-thumb for noise calculations).

Noise Model of Op Amps

In the calculation of op amp circuit noise, it is customary to refer all noise to the input. Figure 6 completely models the input-referred noise sources. In the model, the internal white and flicker noise sources are combined into three equivalent input noise generators, E_n, I_{n1}, and I_{n2}. The noise current generators produce noise voltage drops across their respective source resistors, R_{S1} and R_{S2}. The source resistors themselves generate thermal noise voltages, E_{t1} and E_{t2}. Total rms input-referred voltage noise, over a given bandwidth, is the square root of the sum of the squares of the five noise voltage generators over that bandwidth.

FIGURE 6: Op Amp Noise Model



(2) $E_n(f_H, f_L) = \sqrt{E_n^2 + (I_{n1} \cdot R_{S1})^2 + (I_{n2} \cdot R_{S2})^2 + E_{t1}^2 + E_{t2}^2}$

Equation 2 describes, in total, all noise sources of an op amp circuit. It will be used throughout this application note.

Minimization of total noise requires an understanding of the mechanisms involved in each of the five generators. First, the white noise mechanisms, thermal and shot, are discussed, followed by other low frequency noise mechanisms, flicker and popcorn.

Noise Mechanisms of Op Amps

The two basic types of op amp-associated noises are white noise and flicker noise (1/f). White noise contains equal amounts of power in each hertz of bandwidth. Flicker noise is different in that it contains equal amounts of power in each decade of bandwidth. This is best illustrated by spectral noise density plots such as in Figures 7 and 8. Above a certain corner frequency, white noise dominates; below that frequency, flicker (1/f) noise is dominant. Low noise corner frequencies in conjunction with a low white noise magnitude distinguish low noise op amps from general purpose devices.

FIGURE 7: OP-77 Noise Voltage

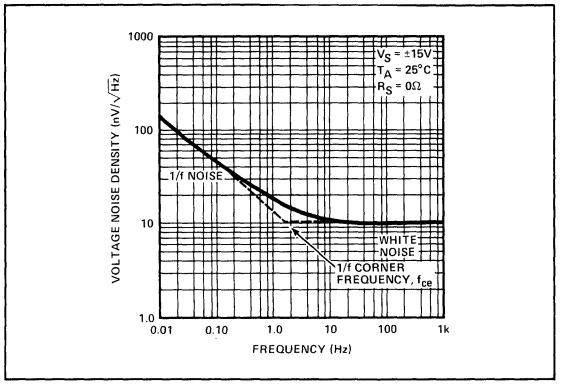
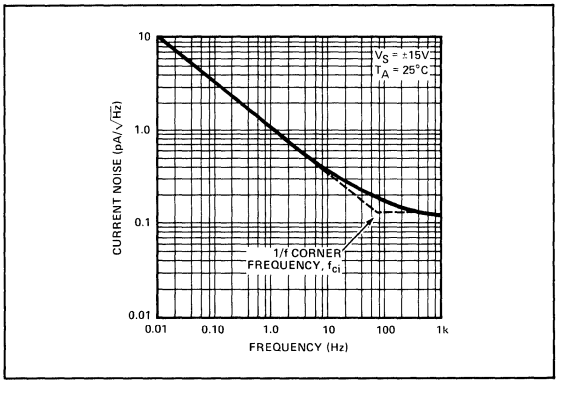


FIGURE 8: OP-77 Noise Current



Mathematically, noise spectral density may be expressed as:

(3a) $e_n^2 = \frac{E_n^2}{\Delta f}$ (3b) $i_n^2 = \frac{I_n^2}{\Delta f}$

Where: e_n, i_n = Spectral noise density of voltage and current, respectively

E_n, I_n = Total rms voltage and current noise in a frequency band, respectively

Δf = Bandwidth of 1Hz

From Equation 3, the total rms noise in a frequency band from f_L to f_H is then,

(4a) $E_n^2 = \int_{f_L}^{f_H} e_n^2 \, df$ (4b) $I_n^2 = \int_{f_L}^{f_H} i_n^2 \, df$

Where: f_H = Upper frequency limit of interest

f_L = Lower frequency limit of interest

Equation 4 means that three things must be known to evaluate total voltage noise (E_n) or current noise (I_n): f_H, f_L, and a knowledge of noise behavior over frequency.

White Noise

White noise contains many frequency components and is so named in analogy to white light which is made up of many colors. The important point to remember is that white noise has equal noise power in each hertz of bandwidth. In other words, the noise spectral density of white noise is **constant** with varying frequency. Thus, Equation 4 may be rewritten to describe white noise over a frequency band.

(5a) $E_{nW} = e_{nW}\sqrt{f_H - f_L}$ (5b) $I_{nW} = i_{nW}\sqrt{f_H - f_L}$

When $f_H \geq 10\,f_L$, the white noise expressions may be reduced to:

(6a) $E_{nW} = e_{nW}\sqrt{f_H}$ (6b) $I_{nW} = i_{nW}\sqrt{f_H}$

Flicker Noise

Unlike white noise, flicker (1/f) noise is not constant with respect to frequency, but has a power spectral density that is inversely proportional (K_e, K_i) to the frequency of interest as described in Equation 7.

(7a) $e_{nF}^2(f) = \frac{K_e^2}{f}$ (7b) $i_{nF}^2(f) = \frac{K_i^2}{f}$

or,

(8a) $e_{nF}(f) = \frac{K_e}{\sqrt{f}}$ (8b) $i_{nF}(f) = \frac{K_i}{\sqrt{f}}$

Where: K_e, K_i are constants of proportionality.

The constants of proportionality depend on a number of parameters internal to the amplifier. It will be shown later that the constants will drop out mathematically.

In order to calculate total voltage and current noise, the concept of corner frequency is useful. Referring to the graphs of e_n or i_n versus frequency as in Figures 7 and 8, we can see that it is a composite of a zero-slope line (white noise) summed with a line

of slope −1/2 (1/f noise, or flicker noise). The projected intersection of these lines occurs where the two noise powers are equal, at a frequency called the *corner frequency*. Therefore, it follows that at the corner frequency, f_{ce} or f_{ci},

(9a) $e_{nW}^2 = e_{nF}^2(f_{ce}) = \frac{K_e^2}{f_{ce}}$ (9b) $i_{nW}^2 = i_{nF}^2(f_{ci}) = \frac{K_i^2}{f_{ci}}$

rearranging,

(10a) $K_e^2 = e_{nW}^2 \cdot f_{ce}$ (10b) $K_i^2 = i_{nW}^2 \cdot f_{ci}$

substituting in Equation 7,

(11a) $e_{nF}^2(f) = e_{nW}^2 \cdot \frac{f_{ce}}{f}$ (11b) $i_{nF}^2(f) = i_{nW}^2 \cdot \frac{f_{ci}}{f}$

or,

(12a) $e_{nF}(f) = e_{nW}\sqrt{\frac{f_{ce}}{f}}$ (12b) $i_{nF}(f) = i_{nW}\sqrt{\frac{f_{ci}}{f}}$

We can find the rms flicker noise in a band as follows:

(13a) $E_{nF}^2 = \int_{f_L}^{f_H} e_{nF}^2(f)\, df$

$= e_{nW}^2 \cdot f_{ce} \cdot \ln\left(\frac{f_H}{f_L}\right)$

(13b) $I_{nF}^2 = \int_{f_L}^{f_H} i_{nF}^2(f)\, df$

$= i_{nW}^2 \cdot f_{ci} \cdot \ln\left(\frac{f_H}{f_L}\right)$

Typical bipolar op amp corner frequencies for voltage noise are in the range of 1 to 20Hz; and for current noise, 10 to 1,000Hz. In comparison, FET input op amps have voltage noise corner frequencies in the range of 100Hz to 500Hz. Still higher are CMOS op amps whose corner frequencies are typically on the order of 1kHz.

Now that we have the mathematical expressions describing white noise and flicker noise, we can sum (by root-sum-square method) the two components to yield a total spectral density expression.

(14a) $e_n^2 = e_{nW}^2 + e_{nF}^2(f)$ (14b) $i_n^2 = i_{nW}^2 + i_{nF}^2(f)$

substituting from Equation 11,

(15a) $e_n = e_{nW}\sqrt{1 + \frac{f_{ce}}{f}}$ (15b) $i_n = i_{nW}\sqrt{1 + \frac{f_{ci}}{f}}$

Equation 15 is an expression frequently used to describe noise (voltage and current) curves seen in op amp data sheets.

The rms noise in a band is then:

(16) $E_n(f_H, f_L) = e_{nW}\sqrt{f_{ce} \cdot \ln\left(\frac{f_H}{f_L}\right) + (f_H - f_L)}$

(17) $I_n(f_H, f_L) = i_{nW}\sqrt{f_{ci} \cdot \ln\left(\frac{f_H}{f_L}\right) + (f_H - f_L)}$

Where: e_{nW} = White noise voltage spectral density
i_{nW} = White noise current spectral density
f_{ce} = Voltage noise corner frequency
f_{ci} = Current noise corner frequency
f_H = Upper frequency limit of interest
f_L = Lower frequency limit of interest

The two most important internally-generated noise minimization rules are derived from Equation 16 and 17: a) limit the circuit bandwidth, and b) use operational amplifiers with low white noise specifications in conjunction with low corner frequencies. So far we have derived the noise voltage (E_n) and noise current (I_n) components (Equations 16 and 17) for the first three terms of Equation 2, which is reproduced below.

(2) $E_n(f_H, f_L) = \sqrt{E_n^2 + (I_{n1} \cdot R_{S1})^2 + (I_{n2} \cdot R_{S2})^2 + E_{t1}^2 + E_{t2}^2}$

In the next section, the last two terms of the equation, which are the thermal noise voltages generated by the external source resistances, are derived.

Thermal Noise

Thermal (Johnson) noise is a white noise voltage generated by random movement of thermally-charged carriers in a resistance; in op amp circuits, this is the type of noise produced by the source resistances in series with each input. Its rms value over a given bandwidth is calculated by:

(18) $E_t = \sqrt{4kTR \cdot (f_H - f_L)}$

Where: k = Boltzmann's constant = 1.38×10^{-23} joules/K
T = Absolute temperature, kelvin
R = Resistance in ohms
f_H = Upper frequency limit in hertz
f_L = Lower frequency limit in hertz

At room temperature, Equation 18 simplifies to:

(19) $E_t = 1.28 \times 10^{-10}\sqrt{R \cdot (f_H - f_L)}$

To minimize thermal noise (E_{t1} and E_{t2}) from R_{S1} and R_{S2}, large source resistors and excessive system bandwidth should be avoided.

Thermal noise is also generated inside the op amp, principally from r_{bb}', the base-spreading resistances in the input stage transistors. These noises are included in E_n, the total equivalent input voltage noise generator.

All the component noise sources of Equation 2 have now been derived. Total noise of an op amp circuit may be easily calculated using the equation. In the next sections, examples using several precision op amps will be calculated to illustrate the noise minimization techniques as well as to contrast the different noise performance of these devices.

TOTAL NOISE CALCULATION

With data sheet curves and specifications, and a knowledge of source resistance values, total input-referred noise may be calculated for a given application. To illustrate the method, noise information from the Precision Monolithics OP-77A and OP-27A data sheets are reproduced in Figure 9. The first step is to determine the current and voltage noise corner frequencies so that the E_n and I_n terms of Equation 2 may be calculated using Equations 16 and 17.

Corner Frequency Determination

In the input spot noise versus frequency curves of Figure 9, it may be seen that voltage noise ($R_S = 0$) begins to rise at about 3Hz. Lines projected from the horizontal (white noise) portion and the sloped (flicker noise) portion intersect at 2Hz, the voltage noise corner frequency (f_{ce}). In the center curve, excluding thermal noise from the source resistance, current noise multiplied by 200kΩ is plotted as a voltage noise. Lines projected from the horizontal portion and sloped portions intersect at 80Hz, the current noise corner frequency (f_{ci}).

FIGURE 9A: OP-77 Input Spot Noise Voltage vs Frequency

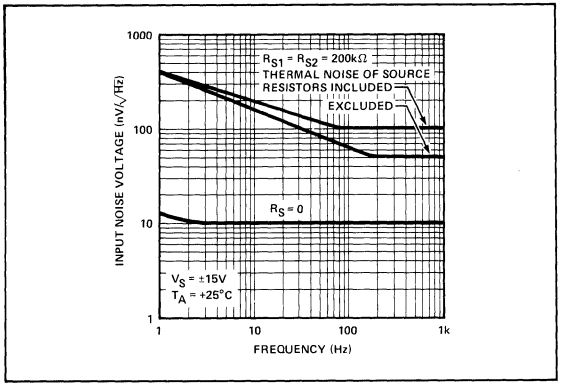


FIGURE 9B: OP-77/OP-27 Ultra-Low Offset Voltage Op Amps

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $T_A = 25°C$, unless otherwise noted.

			OP-77A			OP-27A			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.35	0.6	—	0.08	0.18	μV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz	—	10.3	18.0	—	3.5	5.5	$nV/\sqrt{Hz}$
		f_O = 100Hz	—	10.0	13.0	—	3.1	4.5	
		f_O = 1000Hz	—	9.6	11.0	—	3.0	3.8	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	14	30	—	—	—	pA_{p-p}
Input Noise Current Density	i_n	f_O = 10Hz	—	0.32	0.80	—	1.7	4.0	$pA/\sqrt{Hz}$
		f_O = 100Hz	—	0.14	0.23	—	1.0	2.3	
		f_O = 1000Hz	—	0.12	0.17	—	0.4	0.6	
Input Offset Voltage	V_{OS}		—	10	25	—	10	25	μV
Input Offset Voltage Drift	TCV_{OS}	$-55°C \leq T_A \leq +125°C$	—	0.1	0.3	—	0.2	0.6	$\mu V/°C$
Long Term Input Offset Voltage Stability	V_{OS}/Time		—	0.2	1.0	—	0.2	1.0	$\mu V/Mo$
Input Offset Current	I_{OS}		—	0.3	1.5	—	7	35	nA
Input Bias Current	I_B		—	±1.2	±2.0	—	±10	±40	nA

INPUT NOISE VOLTAGE (e_{np-p})
The peak-to-peak noise voltage in a specified frequency band.

INPUT NOISE VOLTAGE DENSITY(e_n)
The rms noise voltage in a 1Hz band surrounding a specified value of frequency.

INPUT NOISE CURRENT (i_{np-p})
The peak-to-peak noise current in a specified frequency band.

INPUT NOISE CURRENT DENSITY (i_n)
The rms noise current in a 1Hz band surrounding a specified value of frequency.

Equations 16 and 17 also require e_{nW} and i_{nW} for calculation of E_n and I_n. To find e_{nW} and i_{nW}, use the data sheet specifications a decade or more above the respective corner frequencies; in the case of the OP-77A, e_{nW} is $9.6V/\sqrt{Hz}$ (1,000Hz), and i_{nW} is $0.12pA/\sqrt{Hz}$ (1,000Hz). At this time, it should be noted that the noise current, $0.12pA/\sqrt{Hz}$, is a value that has been incorrectly derived from the standardized, commonly-used test method on virtually ALL commercially available op amps. The value is off by a factor of $\sqrt{2}$. Therefore, in order to calculate the correct total noise, the data sheet current noise value should be multiplied by a correction factor of $\sqrt{2}$. Thus, for the noise calculation of the OP-77A, the value e_{nW} is $9.6nV/\sqrt{Hz}$ (1,000Hz), and i_{nW} should be $0.17pA/\sqrt{Hz}$ (1,000Hz).

OP-77 Bandwidth of Interest

To be summed correctly, each of the five noise quantities must be expressed over the same bandwidth, f_H to f_L. For calculation purposes, assume f_H to be the highest frequency component that must be amplified without distortion. Note that e_n, i_n, corner frequencies are independent of actual circuit component values. When doing noise calculations for a large number of circuits using the same op amp, these numbers only have to be calculated once.

OP-77 Typical Application Example

Figure 10A shows a typical ×10 gain stage with a 10kΩ source resistance. In Figure 10B, the circuit is redrawn to show five noise voltage sources. To evaluate total input-referred noise, the values of each of the five sources must be determined.

FIGURE 10A: Noise Analysis Circuit

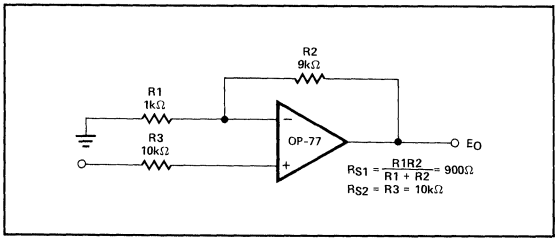
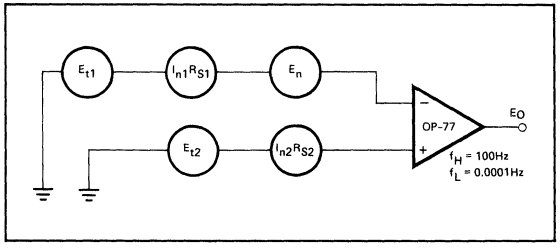


FIGURE 10B: Noise Analysis Equivalent Circuit



Using Equation 19: $E_t = 1.28 \times 10^{-10} \sqrt{R \cdot (f_H - f_L)}$

$E_{t1} = 1.28 \times 10^{-10} \sqrt{(900\Omega)\ (100Hz)} = 0.04\mu Vrms$

$E_{t2} = 1.28 \times 10^{-10} \sqrt{(10k\Omega)\ (100Hz)} = 0.128\mu Vrms$

Next, calculate I_n using Equation 17:

$$I_n = i_n \sqrt{f_{ci} \cdot \ln\left(\frac{f_H}{f_L}\right) + f_H - f_L}$$

$$= 0.17pA \sqrt{80 \cdot \ln\left(\frac{100Hz}{0.0001Hz}\right) + 100 - 0.0001}$$

$$= 5.9pArms$$

and:

$$I_{n1} \cdot R_{S1} = 5.9pA \cdot (900\Omega) = 0.0053\mu Vrms$$

$$I_{n2} \cdot R_{S2} = 5.9pA \cdot (10k\Omega) = 0.059\mu Vrms$$

Finally, E_n from Equation 16:

$$E_n = e_n \sqrt{f_{ce} \cdot \ln\left(\frac{f_H}{f_L}\right) + f_H - f_L}$$

$$= 9.6nV \sqrt{2 \cdot \ln\left(\frac{100Hz}{0.0001Hz}\right) + 100 - 0.0001}$$

$$= 0.108\mu Vrms$$

Substituting in Equation 2:

$$E_n(f_H - f_L) = \sqrt{E_n^2 + I_{n1}^2 R_{S1}^2 + I_{n2}^2 R_{S2}^2 + E_{t1}^2 + E_{t2}^2}$$

$$= \sqrt{(0.108\mu V)^2 + (0.0053\mu V)^2 + (0.059\mu V)^2 + (0.04\mu V)^2 + (0.128\mu V)^2}$$

$$= 0.18\mu Vrms$$

Total input-referred noise = 1.08μV peak-to-peak (0.0001Hz to 100Hz).

Notice that of the five terms in the equation, the first and the last terms dominate. Since the first term is the total rms noise voltage inherent of the amplifier, nothing can be done by the system designer to lower its noise other than to choose a device having inherently low noise characteristics. As can be seen in Equation 16, two key parameters determine the total rms noise of an amplifier—low white noise density and low noise corner frequency.

Notice that the thermal noise voltage (last term) of Equation 2 is determined by the 10kΩ value selected for R3. Had the value been reduced to 1kΩ, the thermal noise voltage would have been 0.04μVrms instead of 0.128μVrms. As a result, total rms noise voltage would have become 0.122μV, a remarkable 32% reduction in total noise.

Indeed, low noise design requires the system designer not only to choose an amplifier with low noise characteristics, but also to pay close attention in selecting appropriately low source resistances in the input circuit.

741 Calculation Example

The preceding calculation determined total noise in a given bandwidth using a low noise op amp. To place this level of performance into perspective, a calculation using the industry-standard 741 op amp in the circuit of Figure 10 is useful. Once again the starting point is corner frequency determination, using the data sheet curves of Figure 11: $f_{ce} = 200Hz$; $f_{ci} = 2kHz$; $e_n = 20nV/\sqrt{Hz}$; $i_n = (\sqrt{2}) \cdot (0.5pA/\sqrt{Hz}) = 0.71pA/\sqrt{Hz}$.

Using these corner frequencies and noise magnitudes, E_n and I_n are calculated to be 1.07μVrms and 118pArms respectively. Multiplying this noise current by the source resistance gives terms 2 and 3 of Equation 2 as shown below:

$$(2)\quad E_n(f_H, f_L) = \sqrt{E_n^2 + I_{n1}^2 R_{S1}^2 + I_{n2}^2 R_{S2}^2 + E_{t1}^2 + E_{t2}^2}$$

substituting in the equation:

$$E_n(f_H, f_L) = \sqrt{(1.07\mu V)^2 + (0.106\mu V)^2 + (1.18\mu V)^2 + (0.04\mu V)^2 + (0.128\mu V)^2}$$

$$= 1.6\mu Vrms$$

Total input-referred noise = 9.6μV peak-to-peak (0.0001Hz to 100Hz). This is more than 8 times that of the low noise OP-77 example. Notice further in this example, the third term of the equation becomes an additional dominant term. It is due to a higher noise current flow in the 10kΩ source resistance.

The calculation examples illustrate four rules for minimizing noise in operational amplifier applications:

Rule 1. Use an op amp with low noise characteristics.

Rule 2. Use an op amp with low noise corner frequencies.

Rule 3. Keep source resistances as low as practical.

Rule 4. Limit circuit bandwidth to signal bandwidth.

FIGURE 11A: Input Noise Voltage as a Function of Frequency

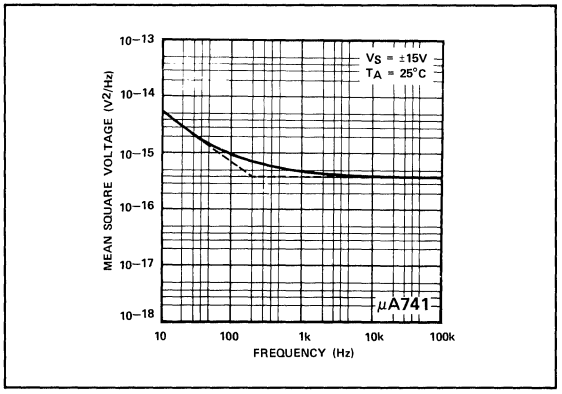
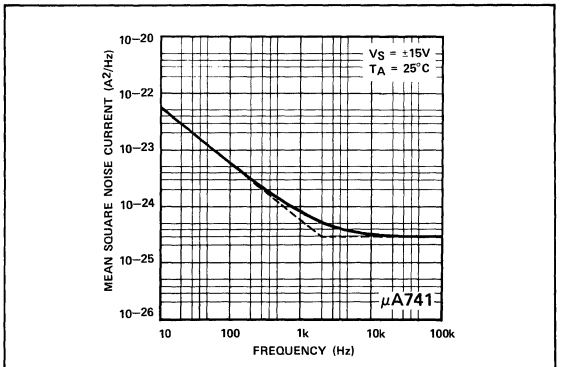
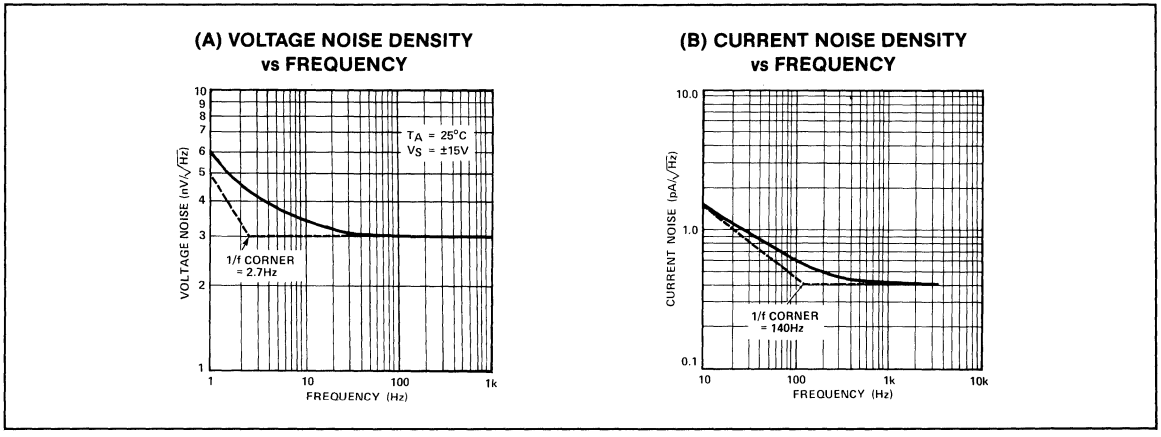


FIGURE 11B: Input Noise Current as a Function of Frequency



AN-15

FIGURE 12: OP-27, OP-37, and OP-227 Noise Voltage and Current as a Function of Frequency



OP-27/OP-227/OP-37 Noise Optimization Design

In this example, a low noise, high speed op amp is examined. Using the circuits in Figures 10A and 10B, and using the data sheet curves of Figures 12A and 12B:

$f_{ce} = 2.7Hz$; $f_{ci} = 140Hz$; $e_n = 3.0nV/\sqrt{Hz}$;
$i_n = (\sqrt{2}) \cdot (0.4pA/\sqrt{Hz}) = 0.57pA/\sqrt{Hz}$

Using these corner frequencies and noise magnitudes, E_n and I_n are calculated to be 0.035μVrms and 25.7pArms, respectively. Multiplying the noise currents by the source resistances yield terms 2 and 3 of Equation 2 as shown below:

$$E_n(f_H, f_L) = \sqrt{E_n^2 + I_{n1}^2 R_{S1}^2 + I_{n2}^2 R_{S2}^2 + E_{t1}^2 + E_{t2}^2}$$

$$= \sqrt{(0.035\mu V)^2 + (0.023\mu V)^2 + (0.257\mu V)^2 + (0.04\mu V)^2 + (0.128\mu V)^2}$$

$$= 0.293\mu Vrms$$

Total input-referred noise = 1.76μV peak-to-peak (0.0001Hz to 100Hz).

Contrary to expectation, these supposedly lower noise amplifiers produce a circuit that has higher total noise than the previous OP-77 design. A closer analysis reveals again that the 10kΩ source resistance is the primary contributor to the two dominant terms (terms 3 and 5) of the total noise equation. The resulting noise generated swamped the excellent noise performance of these devices.

For the purpose of noise optimization, the 10kΩ source resistance is reduced to a balanced 910Ω resistance to preserve the inherently low input offset error of the amplifier. Recalculating Equation 2,

$$E_n(f_H, f_L) = \sqrt{(0.035\mu V)^2 + (0.023\mu V)^2 + (0.023\mu V)^2 + (0.04\mu V)^2 + (0.04\mu V)^2}$$

$$= 0.074\mu Vrms$$

Total input-referred noise is now a respectable 0.44μV peak-to-peak (0.0001Hz to 100Hz).

It is clear from this optimization that the system designer can achieve both a balance of low noise and low input offset voltage performance with these amplifiers. It is also obvious that one can optimize noise further by using, say, a 10Ω source resistance; in which case, the resulting total rms noise voltage is now 0.058μV, and a peak-to-peak noise is 0.35μV. This translates to a net noise reduction of 20% compared to the design using 1kΩ balance source resistance.

LIMITING BANDWIDTH TO MINIMIZE NOISE

Effective circuit bandwidth must not be much greater than signal bandwidth or amplification of undesirable high frequency noise components will occur. Throughout the preceding calculations, an assumption of "bandwidth-of-interest" was made, while in actual application the amplifier's bandwidth must be considered.

In Figure 13, the OP-77 frequency response curves show a rolloff of 20dB/decade; integration of the area under the curve will show the effective circuit noise bandwidth to be 1.57 times the 3dB bandwidth. In most closed-loop gain configurations, the amplifier's bandwidth may be greater than required, and output filtering, such as in Figure 14, could be used. As an alternate to output filtering, an integrating capacitor may be connected across the feedback resistor. Bandwidth may also be limited in some applications by overcompensating an externally-compensated low noise op amp, such as the OP-06.

FIGURE 13A: OP-77 Open-Loop Frequency Response

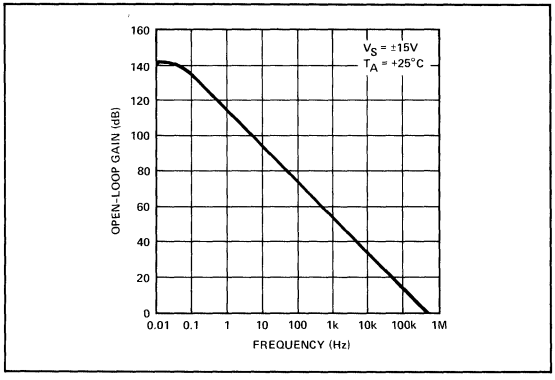


FIGURE 13B: OP-77 Closed-Loop Response for Various Gain Configurations

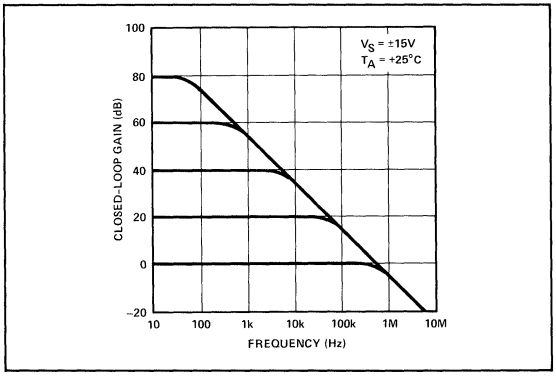
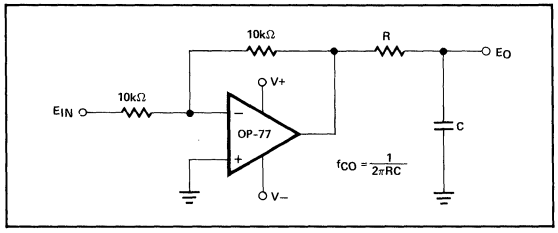


FIGURE 14: Output Filtering



MISCELLANEOUS NOISE MINIMIZATION METHODS

Certain other noise mechanisms merit consideration: use metal film resistors; carbon resistors exhibit "excess noise," with both 1/f and white noise content being related to DC applied voltage. The use of balanced source resistors, while sometimes good for DC error purposes, will increase noise; the balancing resistor is not required for op amps such as the OP-07 and OP-77, since $I_{OS} \cong I_B$. Keep noise in its proper perspective; minimize it without introducing additional DC errors. Use low noise op amps with overall DC specifications that will satisfy the application.

OTHER NOISES

Shot noise (Schottky noise) is a white noise current associated with the fact that current flow is actually a movement of discrete charged particles (electrons) across a potential barrier, such as a PN junction of a transistor or diode. Shot noise is a component of i_n, and indirectly, e_n. In Figure 6, I_{n1} and I_{n2}, above the 1/f frequency, are shot noise currents which are related to the amplifier's DC input bias currents:

$$(20)\quad I_{sh} = \sqrt{2qI_{DC}(f_H - f_L)}$$

Where: I_{sh} = rms shot noise value in amps

q = Charge of an electron = 1.602×10^{-19} C

I_{DC} = DC bias current in amps

f_H = Upper frequency limit in hertz

f_L = Lower frequency limit in hertz

At room temperature Equation 20 simplifies to:

$$(21)\quad I_{sh} = 5.66 \times 10^{-10} \sqrt{I_{DC}(f_H - f_L)}$$

Shot noise currents also flow in the input-stage emitter dynamic resistances (r_e), producing input noise voltages. These voltages, along with the r_{bb}' thermal noise, make up the white noise portion of E_n; the total equivalent input noise voltage generator.

Shot noise can also be generated from external sources such as PIN photodiodes, zener diodes, and other semiconductor junction devices. Noise current from these sources may be calculated using Equation 20 or 21.

In limited bandwidth, very low frequency applications, *flicker* (1/f) noise is the most critical noise source. An op amp designer minimizes flicker noise by keeping current noise components in the input and second stages from contributing to input voltage noise. Equation 22 illustrates this relationship:

$$(22)\quad \frac{i_{n\ \text{second stage}}}{g_{m\ \text{first stage}}} = e_{n\ \text{input}}$$

Another critical factor is corner frequency. For minimum noise, the current and voltage noise corner frequencies must be low; this is crucial. As shown in Figure 15, low-noise corner frequencies distinguish low-noise op amps from ordinary industry-standard 741 types.

The photograph in Figure 16, taken using the test circuit of Figure 17, illustrates the flicker noise performance of the OP-77. This device demonstrates proper attention to low noise circuit design and wafer processing and achieves a remarkable 0.35μV peak-to-peak input voltage noise in the 0.1Hz to 10Hz bandwidth.

FIGURE 15: Noise Voltage Comparison

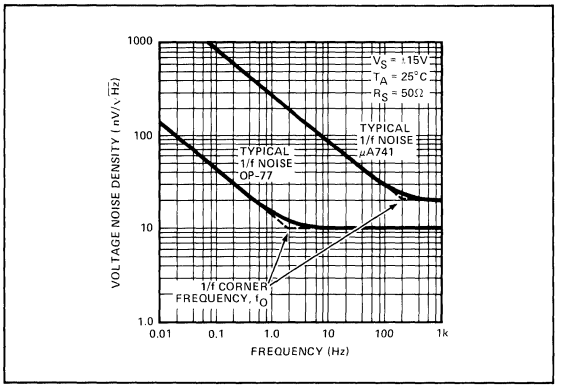


FIGURE 16: OP-77 Low Frequency Noise

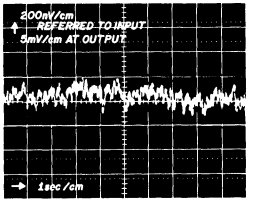
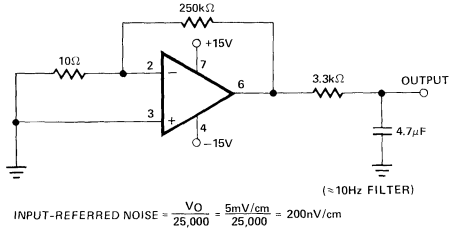


FIGURE 17: Low Frequency Noise Test Circuit

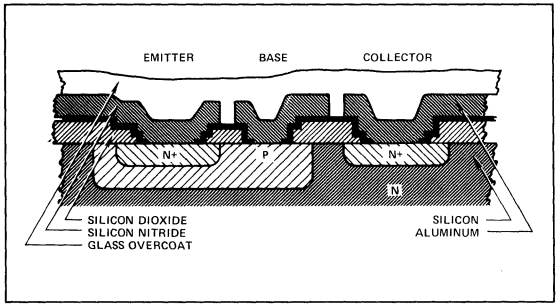


Popcorn noise (burst noise) is a momentary change in input bias current usually occurring below 100Hz, and is caused by imperfect semiconductor surface conditions incurred during wafer processing. Precision Monolithics minimizes this problem through careful surface treatment, general cleanliness, and a special three-step process known as "Triple Passivation."

To begin the process, a specially-treated thermal silicon dioxide layer is grown. This protects the junctions and also attracts any residual ionic impurities to the top surface of the oxide, where they are held fixed. Next, a layer of silicon nitride is applied to prevent the entry of any potential contamination or impurities.

The third step is the thick glass overcoat which leaves only the bonding pads exposed. A cutaway view of a finished device is shown in Figure 18.

FIGURE 18: Triple Passivated Integrated Circuit Process



Op amp manufacturers face a difficult decision in dealing with popcorn noise. Through careful low noise processing, it can be eliminated from almost all devices; alternatively, the processing may be relaxed, and finished devices must be individually tested for this parameter. Special noise testing takes valuable labor time, adds significant amounts to manufacturing cost, and ultimately increases the price a customer has to pay. At Precision Monolithics, the low noise process alternative is used to manufacture high volumes of cost-effective low noise op amps.

SUMMARY

A summary of the major points to consider is as follows:

1. Minimize externally-generated noise.
2. Choose an amplifier with low noise characteristics and low 1/f noise corner frequencies.
3. Limit the circuit bandwidth to signal bandwidth.
4. Eliminate excessive resistance in the input circuit.

CONCLUSION

Recent improvements in IC op amp DC specifications have made noise an important error consideration. From data sheet information and source resistance values, total input-referred noise over a given bandwidth can be easily calculated. Total noise can be minimized by a thorough understanding of the various noise-generation mechanisms.

NOISE BIBLIOGRAPHY

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PMI

AN-16

LOW-COST, HIGH-SPEED A/D CONVERSION WITH THE DAC-08

Precision Monolithics Inc.

APPLICATION NOTE 16

Today's fast computer and microprocessor-controlled systems frequently require A/D converters which will complete a conversion in one cycle time.

Until now, these high speed A/D converters have been expensive and difficult to build. Most designers have therefore chosen to purchase modular A/D converters typically ranging in price from $100 to $400. This application note describes three less costly A/D designs, with total conversion times of 4μs, 2μs, and 1μs. These designs are implemented with the DAC-08, a recently announced high speed monolithic digital-to-analog converter. A discussion of basic successive approximation is given, followed by practical circuit designs.

SUCCESSIVE APPROXIMATION A/D ADVANTAGES

Successive approximation A/D conversion is the most popular choice in many systems today because it achieves high conversion rates at very low cost. Other methods, such as Tracking (Servo) or Staircase (Ramp), require up to "2^n" clock cycles per conversion, where "n" is the number of bits of resolution, while successive approximation requires only "n + 1" clock cycles. Finally, a designer can easily construct his A/D with readily available standard ICs.

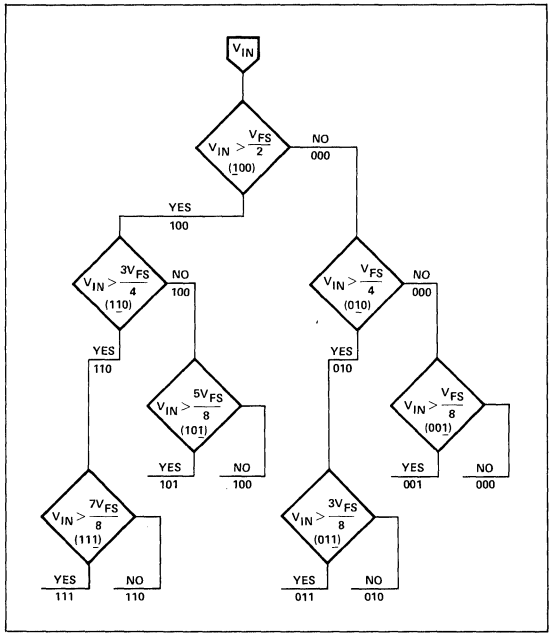


Figure 1. Flow Diagram for 3-Bit Successive Approximation A/D Conversion

BASIC SUCCESSIVE APPROXIMATION A/D CONVERSION

A successive approximation A/D converter operates by comparing the analog input to a series of "trial" conversions; the first trial compares the input to the value of the most significant bit (MSB) or half of full scale. Figure 1 shows the progression of trials for a 3-bit converter. If the input is greater than the MSB value, the MSB is retained and the converter moves on to "trying" the next most significant bit, or three-quarters full scale. If the input had been less than the MSB, the logic would have turned the MSB off before going on to the next most significant bit, or one-quarter full scale. This "branching" continues until each successively smaller bit has been tried, with the entire process taking "n" trials.

To implement the logic for the successive approximation algorithm, a configuration similar to Figure 2 may be employed, wherein a start command places a "one" in the first bit of a shift register. This sets the first latch to "one" and turns on the DAC's MSB. If the comparator output remains low, the "one" will remain in the latch; if not, the latch will be reset to zero before the next bit trial begins. The next clock cycle causes the shift register to place a "one" in the second bit, and a similar process continues until all bits

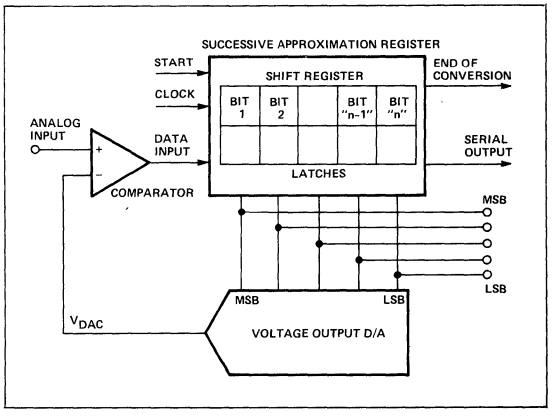


Figure 2. Successive Approximation A/D Converter

have been tried. After the last bit's trial, the end-of-conversion output changes state indicating the parallel data is ready to be used.

CURRENT COMPARISON

The previous discussion indicated that the function of the comparator was to perform a comparison between the analog input **voltage** and the output **voltage** of the DAC. Higher speed conversions may be achieved by using the output of a fast current output DAC directly. This may be implemented as shown in Figure 3, where the comparator examines the polarity of ($V_{IN} - I_{DAC}R_{IN}$). Current comparison eliminates the need for a current-to-voltage converting op amp which is by far the slowest element in most D/A converters.

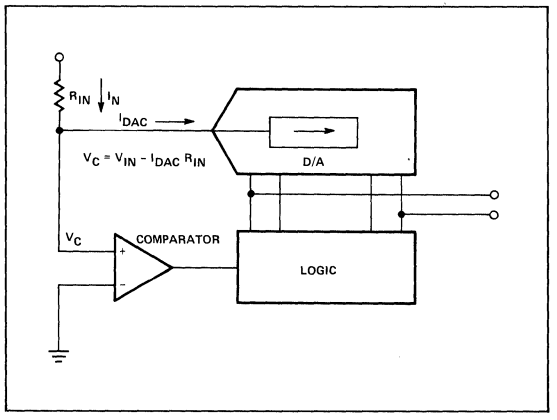


Figure 3. Current Comparison A/D Input

DYNAMIC CONSIDERATIONS

The time required to complete an 8-bit successive approximation A/D conversion is determined by the length of 8 trials and their associated comparator decisions, plus one clock cycle. To minimize these periods, three dynamic considerations must be made:

1. DAC output current settling time to ±1/2LSB.
2. Comparator propagation delay with the available overdrive.
3. Logic propagation delay and setup time requirements.

For example, with a 500ns DAC, a 500ns comparator, and 100nsec of logic delay, each of these cycles would require 1.1μs. An 8-bit conversion would take nine clock periods, or 10μs. To design a fast A/D, each of these delays must be made as short as possible. In the next few paragraphs, practical methods of minimizing these delays are discussed.

DAC CURRENT SETTLING TIME

The DAC-08 is a low cost monolithic current output DAC with 85ns full scale settling time and is ideal for use in high speed A/D converter designs. The internal logic switch design enables propagation delays of 35ns for each of the 8 bits. Settling time of the LSB to within ±1/2LSB of final value is therefore 35ns, with each successively more significant bit taking progressively longer. The MSB settles in 85ns; it is the dominant factor of full scale settling time. This performance is illustrated in the scope photo of Figure 4, taken at the output of the test circuit of Figure 5.

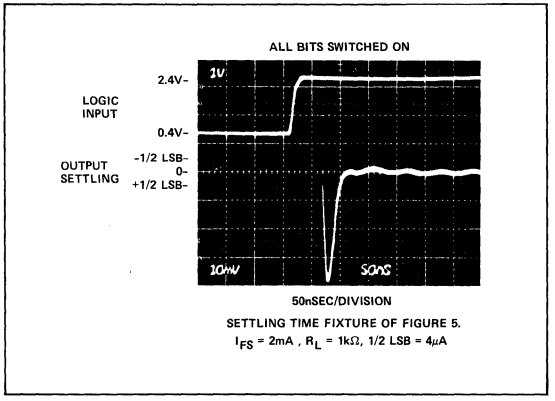


Figure 4. Output Settling Time

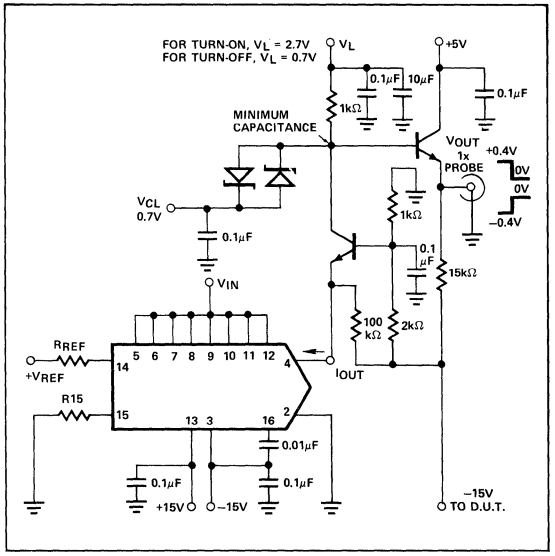


Figure 5. Settling Time Measurement

A major factor affecting settling time is the RC time constant formed by the load resistance (R_L) and the DAC output capacitance (C_O) plus any stray capacitance present at the summing node. Settling to within ±1/2LSB at 8 bits (±0.2%

full scale) requires 6.2 RC time constants. For the DAC-08, the output capacitance is 15pF; as a result the output RC time constant is a major factor influencing settling time when R_L is greater than 500Ω and dominates when R_L exceeds 900Ω.

This situation produces difficult requirements. Optimum DAC settling time occurs when $R_L \leq 500\Omega$, but for full scale currents of 2mA, 1/2LSB is only 4μA. Thus, with a 500Ω equivalent resistance, the voltage at the DAC output corresponding to 1/2LSB is only 2mV and is inadequate for high speed operation of many comparators. For this reason, R_L is usually larger than 500Ω, which is a necessary compromise between DAC settling time and comparator input overdrive requirements.

COMPARATOR CONSIDERATIONS

All comparators respond fastest to large differential input voltages (high overdrive). This phenomenon is shown in Figure 6, a graph of response time vs input voltage for the Precision Monolithics' CMP-01. This low cost comparator provides DC characteristics compatible with 10 and 12-bit A/D converters and has adequate speed for 4μs 8-bit converters.

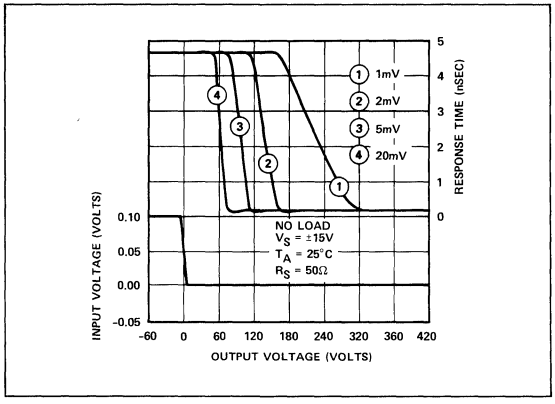


Figure 6. Response Time For 100mV Step and Various Input Overdrives

For 2μs and 1μs designs, the AM686 was selected. It provides 12ns propagation with 2.5mV overdrive, Schottky TTL outputs, and DC input specifications adequate for an 8-bit A/D. Ultra-high speed requires considerable power. Maximum supply currents are 42mA from the +5V supply and 34mA from the −5V supply.

LOGIC CONSIDERATIONS

A single DIP package, the AM2502 Successive Approximation Register, contains the logic for 8-bit A/D converters operating at 2μs or greater conversion times. (Detailed descriptions of A/Ds constructed with the AM2502 and Precision Monolithics DACs are contained in AN-11.) A 1μs A/D requires special logic design using Schottky TTL and will be described in the detailed circuit description.

PRACTICAL 3 IC A/Ds

When the required conversion time is ≥2μs, the DAC-08's fast settling time enables very simple and low cost designs. A 4μs design is shown in Figure 7. At additional cost and increased power dissipation, changing the comparator to an AM686 results in a 2μs A/D. Every nanosecond counts in a 1μs A/D, and the circuit necessarily increases in complexity. However, with the DAC-08, Schottky TTL logic, and attention to layout, a 1μs A/D can be constructed at low cost.

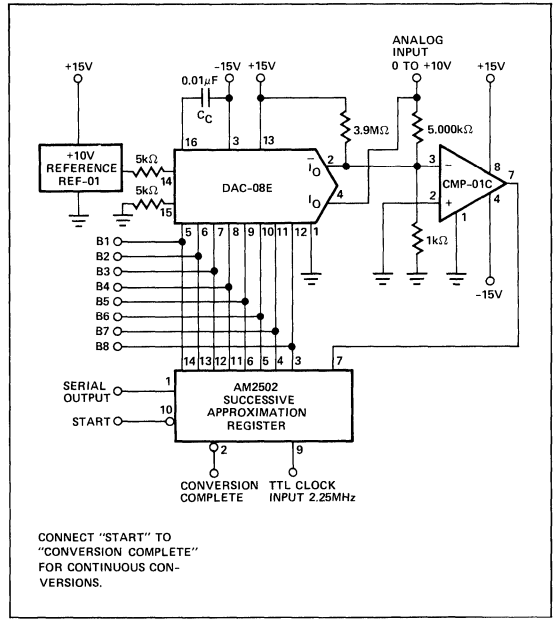


Figure 7. 3 IC Low Cost A/D Converter

ANALOG DESIGN

The DAC-08AQ is useful in this design for several reasons. Its output full scale current is guaranteed to be 1.992mA ±8μA, when a 10.000V reference is connected to a 5.000kΩ resistor in series with Pin 14. In this design, the 5kΩ is split to allow bypassing without capacitively loading the 10 volt source. For slightly higher speed, the total resistance may be reduced to 2.5kΩ, thereby increasing I_O full scale to 3.984mA, allowing a lower sum node resistance and lower RC time constant. (The DAC itself does not settle faster at 4mA full scale current.) The DAC-08A maximum nonlinearity of ±0.1% full scale enables faster settling time to within ±1/2LSB (±0.2% full scale) for each bit trial than would be the case using a DAC with ±0.2% nonlinearity. Using the ±0.2% nonlinearity DAC-08 or DAC-08E provides cost sav-

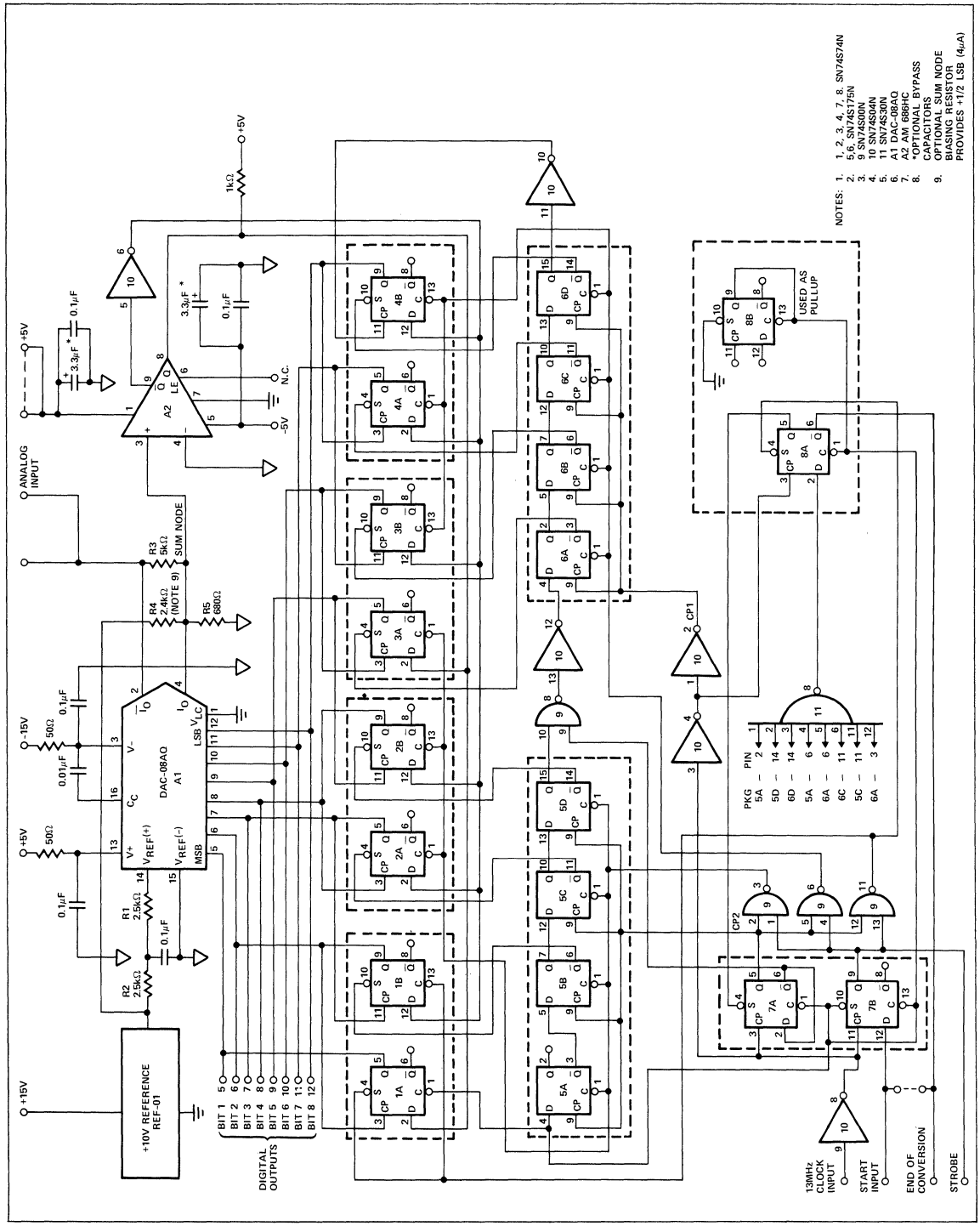


Figure 8. Complete Schematic 8-Bit, 1μs A/D

ings at an overall increase in conversion time. Both true and complementary current outputs are provided, and their summation is always $I_{full\ scale}$. In this design, I_O is connected to the analog input. Since $I_O + \overline{I_O}$ is constant, and $\overline{I_O}$ flows in R3, the DC input current is constant. Holding the A/D input current constant reduces buffer amplifier output impedance requirements. The buffer amplifier used in this application must have sufficient bandwidth to hold V_{IN} constant during a 1μs A/D conversion.

CALIBRATION AND ACCURACY

In many applications calibration is not required. With a 10.000V reference and ±0.05% tolerance resistors, the worst case full scale error is ±0.15%. The zero scale error is totally dependent upon comparator input offset voltage and input bias current, and, in most cases, it may be tolerated. If the errors are not tolerable, then the following calibration procedure may be used.

Calibration of the A/D is done first at zero scale, then at full scale. The zero transition is set by R4, a resistor connected to the +10 volt reference. For 10V full scale, the desired transition point between a code of 0000 0000 and 0000 0001 is at +20mV (+1/2LSB). With an ideal comparator, R4 would be 2.56mΩ (10 volts/3.9μA). Since comparators are less than ideal, R4 must also cancel out the comparator's input offset errors. With +20mV applied at the analog input and using a low clock rate, select R4 to cause the output code to fluctuate between 0000 0000 and 0000 0001. (Do not install a pot for R2 or R4 since it will increase capacitance and inductance at the sum node.) Full scale is calibrated by applying +9.940V to the analog input and trimming R2 until the output code fluctuates between 1111 1110 and 1111 1111. Alternatively, the reference voltage source may be adjusted for the same effect. This will be a small adjustment due to the DAC-08A's tight output full scale current relationship with the reference voltage. Once calibrated, accuracy is a function of temperature-induced drifts only.

A TYPICAL CONVERSION CYCLE

A conversion is initiated by a high level at the Start input when the input 13mHz clock makes a low to high transition. Approximately 9ns later, the control logic generates a clear and reset pulse (Strobe) which causes several events: the 8 output flip-flops are cleared except for the MSB flip-flop 1 which is set to a "one"; both shift registers are cleared; the DAC has Bit 1 turned on, all others are off. The conditions for the first trial at half scale are now established.

As the DAC output settles, the comparator continuously examines the polarity at its noninverting input. For this case, with zero volts at the analog input, the comparator finds a negative voltage present; its output therefore is low. This low is applied to the "D" inputs of all 8 output flip-flops. Recall that 74S74 flip-flop outputs won't change until they are clocked by a positive transition at their CP inputs. At the time labeled 1 on the CP1 waveform, the reset and clear pulse, Strobe, returns high.

Shift Register Number 1 waits for a positive-going transition of CP2. At 2 time CP2 goes high, transferring a "one" from 9A-Q to 9B-Q; 9B-Q goes low, setting 2-Q high and clocking the comparator's "zero" into the Bit 1 flip-flop. The other six flip-flops do nothing, because they are not clocked. Bit 1's answer is now latched, and Bit 2, 1/4 full scale, is being tried. The process continues with the shift register causing each bit to be tried from Bit 2 to Bit 8. After the Bit 8 decision, the EOC output goes high, indicating that the answer in parallel format is available at the 8-bit outputs.

OUTPUT INTERFACING

In continuous conversion operation, the most common connection, EOC is connected to the Start input. While the answer is available whenever EOC is high, it is convenient to use the positive-going edge of the Strobe output as a clock for two 74S175 quad "D" flip-flops used as an 8-bit storage latch. Since Strobe goes high before another conversion cycle begins, there is ample setup time for the latch; the answer has been steady for over 35ns.

OVERALL DESIGN

Due to the bit settling time range of the DAC-08 from 85ns for Bit 1 to 35ns for Bit 8, progressively decreasing trial-and-decision periods would be ideal. Practically, such a timing sequence is difficult to generate at low cost, so a compromise was made: The first four bits allow 160ns for each trial-and-decision, while the last four bits allow 80ns. This may be seen in the waveforms of Figure 9. The timing sequence is generated by shifting a "one" through two shift registers with in-phase clocks, one at 6.5mHz derived from the other at 13mHz.

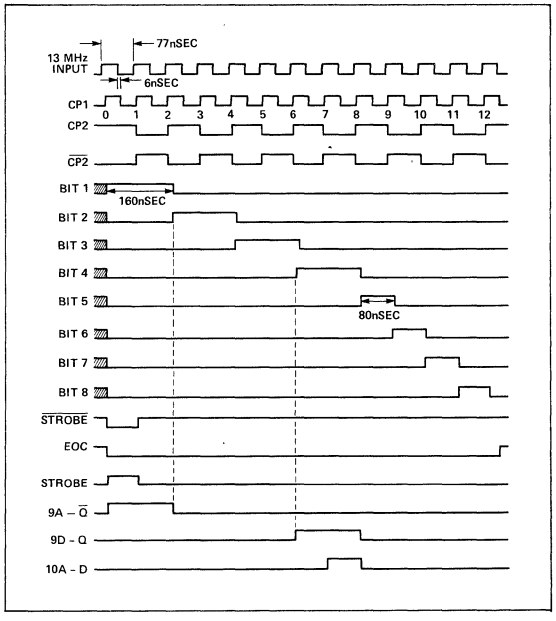


Figure 9. Timing Waveforms with Zero Volts Input

Standard 74 Schottky TTL logic was selected for speed, compatibility with the AM686 comparator, ready availability, and price.

A useful characteristic of the DAC-08 is its capability to directly interface with all popular logic families including TTL, CMOS, and ECL. For this design the DAC-08's logic control pin (Pin 1) is grounded to provide the proper TTL logic threshold. A design utilizing ECL could provide slightly faster conversion time at increased power consumption.

LOGIC DESIGN

The primary logic design element is the 74S series positive-edge-triggered "D" flip-flop. This type of flip-flop is useful in A/D designs because of several properties:

1. The propagation delay from Set to Q going high is only 3ns.
2. The information on the D input is transferred to the Q output only at a positive-going edge of CP.
3. Changes at the D input (comparator settling changes) are ignored when CP is in a steady state.

74S74 dual "D" flip-flops are used for the 8 output latches and for the control logic, and 74S175 quad "D" flip-flops are used for the two shift registers.

Flip-flops 2 through 8 in the simplified schematic (Figure 10) perform two functions. Typical operation can be understood by examining the operation of Flip-Flop 2. When set by an input from Shift Register Number 1, the Q output of Flip-Flop Number 2 goes high, which starts the trial of Bit 2 and acts as a clock which is the result of Trial 1, to Q of Flip-Flop 1. This basic connection, using the beginning of a new trial to clock the previous bit trial, is used on all eight output flip-flops. The start of each bit trial is precisely coincident with

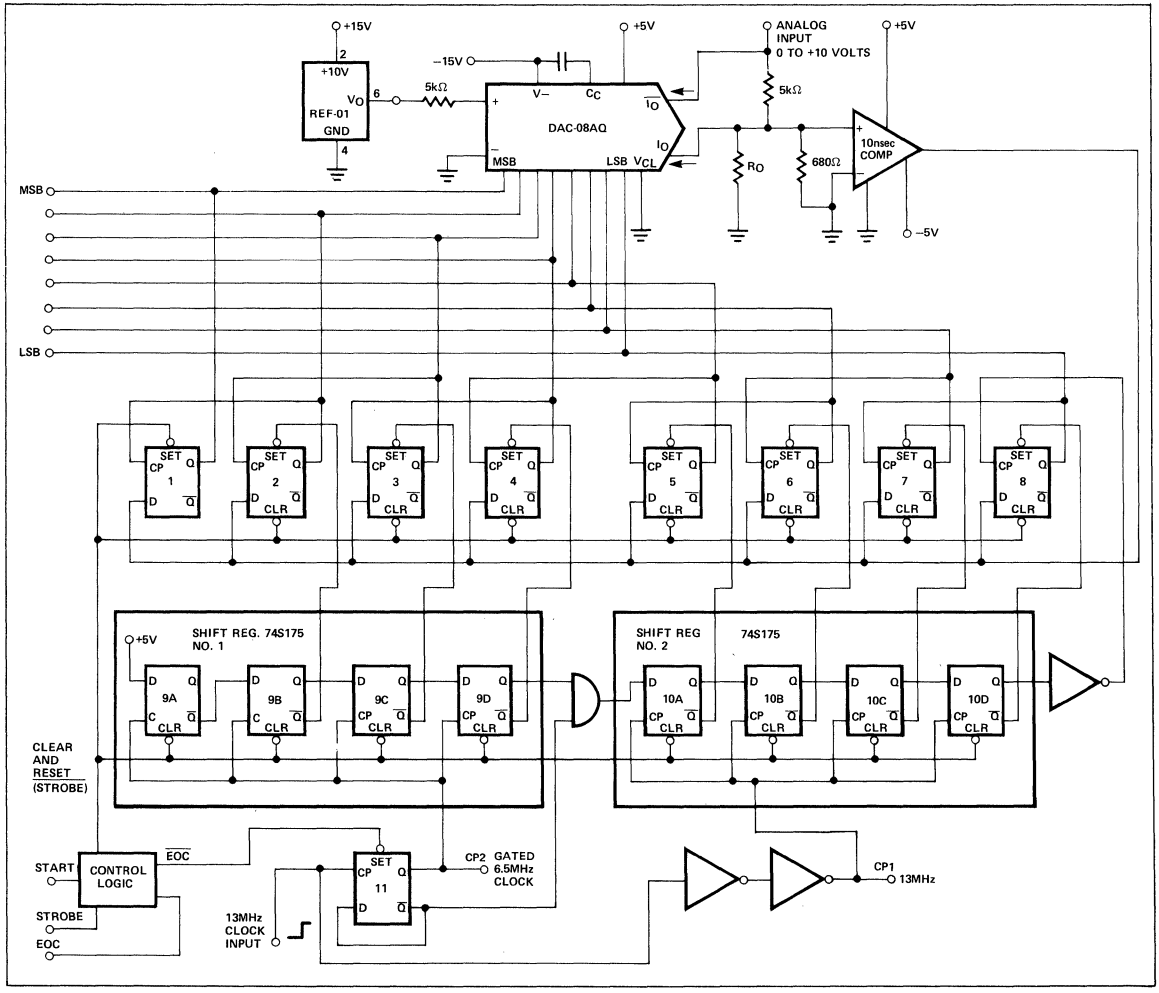


Figure 10. Simplified Schematic 1μs A/D

clocking of the previous bit answer; so no time is wasted, and logic delays are reduced to setup times only.

PRINTED CIRCUIT BOARD LAYOUT RULES

For A/D designs generally, and high speed designs in particular, layout is important. Some of the more important rules are listed below:

1. Digital ground must be separated from analog ground; they must meet at only one common point.
2. Digital traces should not cross or be routed near sensitive analog areas; this is especially important near the sum node.
3. With Schottky TTL logic, the digital ground and V_{CC} traces should be large and contain provisions for generous bypassing.
4. The trace from the DAC output to comparator input (sum node) should be short, and it should be guarded by analog ground.
5. All analog components should be located as close as possible to the edge connector so that the input analog traces will be short.
6. The comparator's outputs should be routed away from its inputs, to minimize capacitive coupling and possible oscillation.

SYSTEM CONSIDERATIONS

Typical system connections ar shown in Figure 11. Digital grounds and analog grounds meet at one point only keeping large power supply return currents away from the sensitive analog ground portion of the A/D system. Start is connected to EOC for continuous conversions, and Strobe is used to clock the parallel answer into an output register at the end of each conversion.

CONCLUSION

The DAC-08 High Speed Monolithic D/A Converter greatly simplifies construction of high speed A/D converters. Designs using only three ICs achieve 2μs conversions, and 1μs conversion can be attained with additional logic. Techniques have been presented which allow the user to construct low cost, high speed A/D converters.

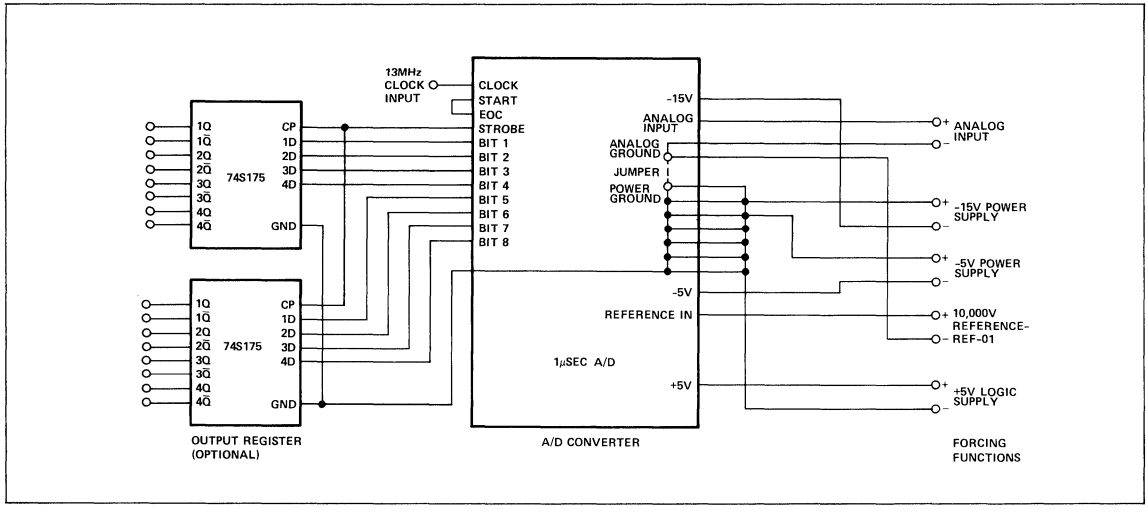


Figure 11. Typical System Connection

APPLICATION NOTE 17

GENERAL DESCRIPTION

There has been a trend in recent years toward providing totally dedicated digital-to-analog converters with limited applications versatility. This application note describes a new type of monolithic DAC designed for an extremely broad range of applications, the Precision Monolithics DAC-08.

Several unique design features of this low-cost DAC combine to provide total applications flexibility. Principal among them are: dual complementary, true current outputs; universal logic inputs capable of interfacing with any logic family; 85ns settling time; high-speed multiplying capability; and finally, the ability to use any standard system power supply voltages. A description of these features is given followed by specific applications using each feature.

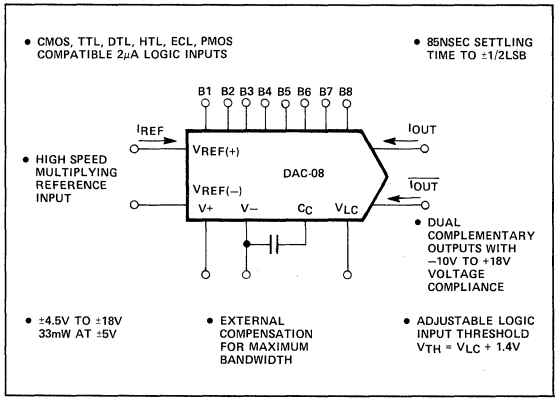


Figure 1. The Flexible D/A Converter

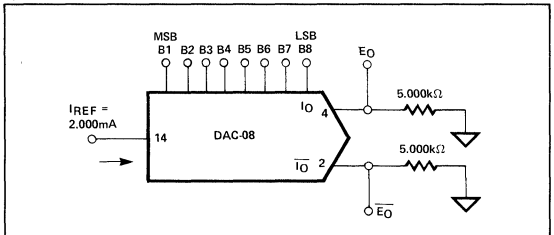
OUTPUT

HIGH VOLTAGE COMPLIANCE CURRENT OUTPUTS

Many older current-output DACs actually have resistive outputs which must be terminated in a virtual ground. The DAC-08, however, is a true digitally-controlled current source with an output impedance typically exceeding 20MΩ.

Its outputs can swing between −10V and +18V with little or no effect on full-scale current or linearity. Some of the applications that require high output voltage compliance include:

1. Precise current transmission over long distances.
2. Programmable current sources.
3. Analog meter movement driving.
4. Resistive termination for a voltage output without an op amp.
5. Capacitive termination for digitally-controlled integrators.
6. Inductive termination with balanced transformers, transducers and headsets.



	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	E_O
FULL SCALE −1LSB	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	0.000
FULL SCALE −2LSB	1	1	1	1	1	1	1	0	1.984	0.008	−9.920	− 0.40
HALF SCALE +LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
HALF SCALE	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
HALF SCALE −LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
ZERO SCALE +LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
ZERO SCALE	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

Figure 2. Basic Unipolar Negative Operation

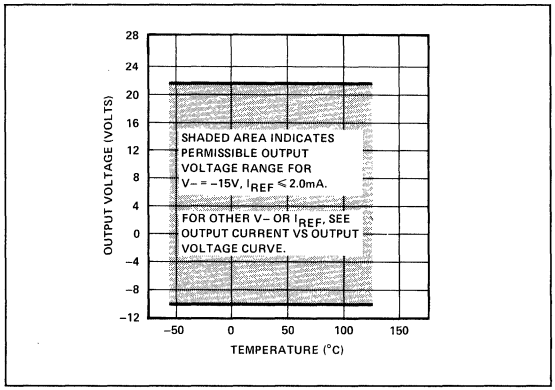


Figure 3. Output Voltage Compliance vs Temperature

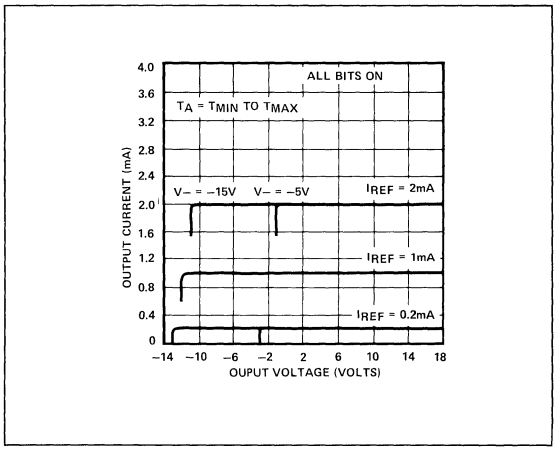
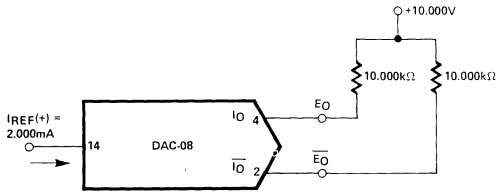
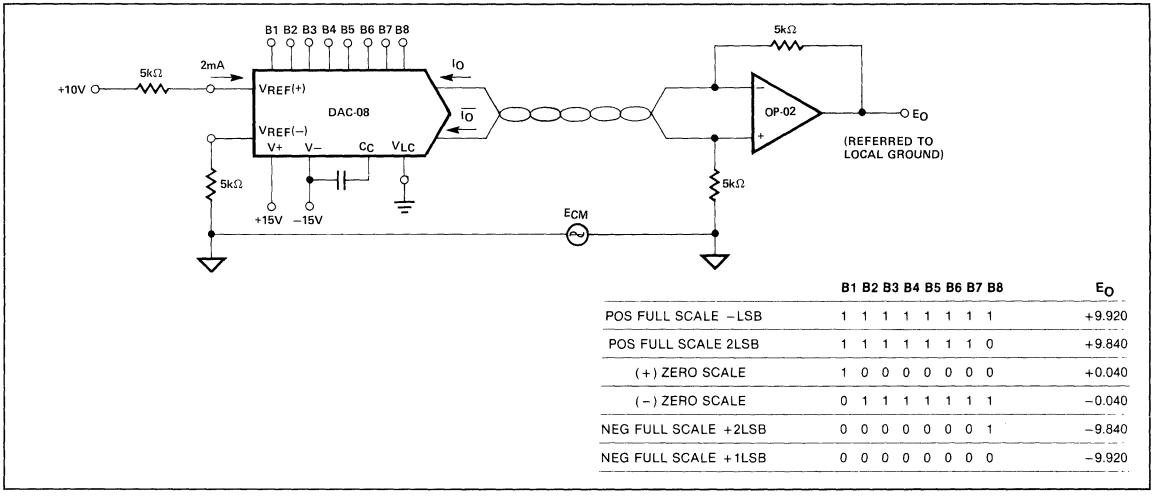


Figure 4. Output Current vs Output Voltage (Output Voltage Compliance)



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	E_O
POS FULL SCALE –LSB	1	1	1	1	1	1	1	1	– 9.920	+10.000
POS FULL SCALE 2LSB	1	1	1	1	1	1	1	0	– 9.840	+ 9.920
ZERO SCALE +LSB	1	0	0	0	0	0	0	1	– 0.080	+ 0.160
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	+ 0.080
ZERO SCALE –LSB	0	1	1	1	1	1	1	1	+ 0.080	0.000
NEG FULL SCALE +LSB	0	0	0	0	0	0	0	1	+ 9.920	– 9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	+10.000	– 9.920

Figure 5. Basic Bipolar Output Operation



	B1	B2	B3	B4	B5	B6	B7	B8	E_O
POS FULL SCALE –LSB	1	1	1	1	1	1	1	1	+9.920
POS FULL SCALE 2LSB	1	1	1	1	1	1	1	0	+9.840
(+) ZERO SCALE	1	0	0	0	0	0	0	0	+0.040
(–) ZERO SCALE	0	1	1	1	1	1	1	1	–0.040
NEG FULL SCALE +2LSB	0	0	0	0	0	0	0	1	–9.840
NEG FULL SCALE +1LSB	0	0	0	0	0	0	0	0	–9.920

Figure 6. High Noise Immunity Current to Voltage Conversion

DUAL COMPLEMENTARY OUTPUTS

Convertional DACs have a single output, so they cannot drive balanced loads and are limited to a single input code polarity. The DAC-08 was designed to overcome these limitations.

Input coding of positive binary or complementary binary is obtained by a choice of outputs, I_O for positive-true or $\overline{I_O}$ for negative-true. In many applications both are used either independently or in combination. Dual comlementary outputs allow some very unusual and useful DAC applications:

1. CRT display driving without transformers.
2. Differential transducer control systems.
3. Differential line driving.
4. High-speed waveform generation.
5. Digitally controlled offset nulling of op amps.

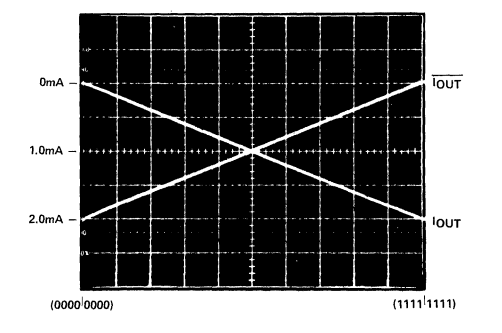


Figure 7. True and Complementary Output Operation

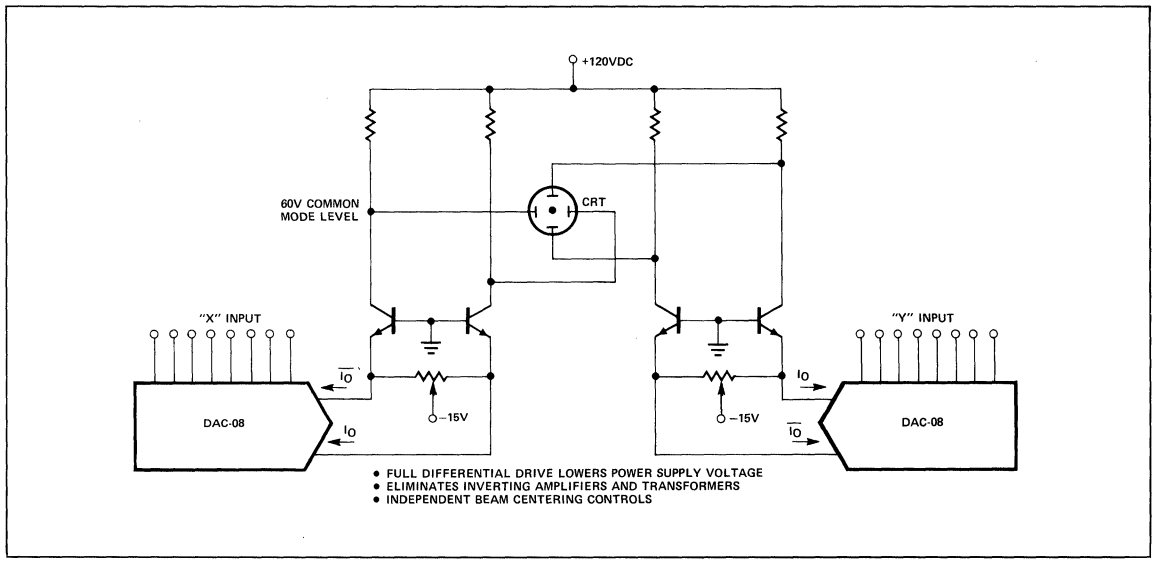


Figure 8. CRT Display Driver

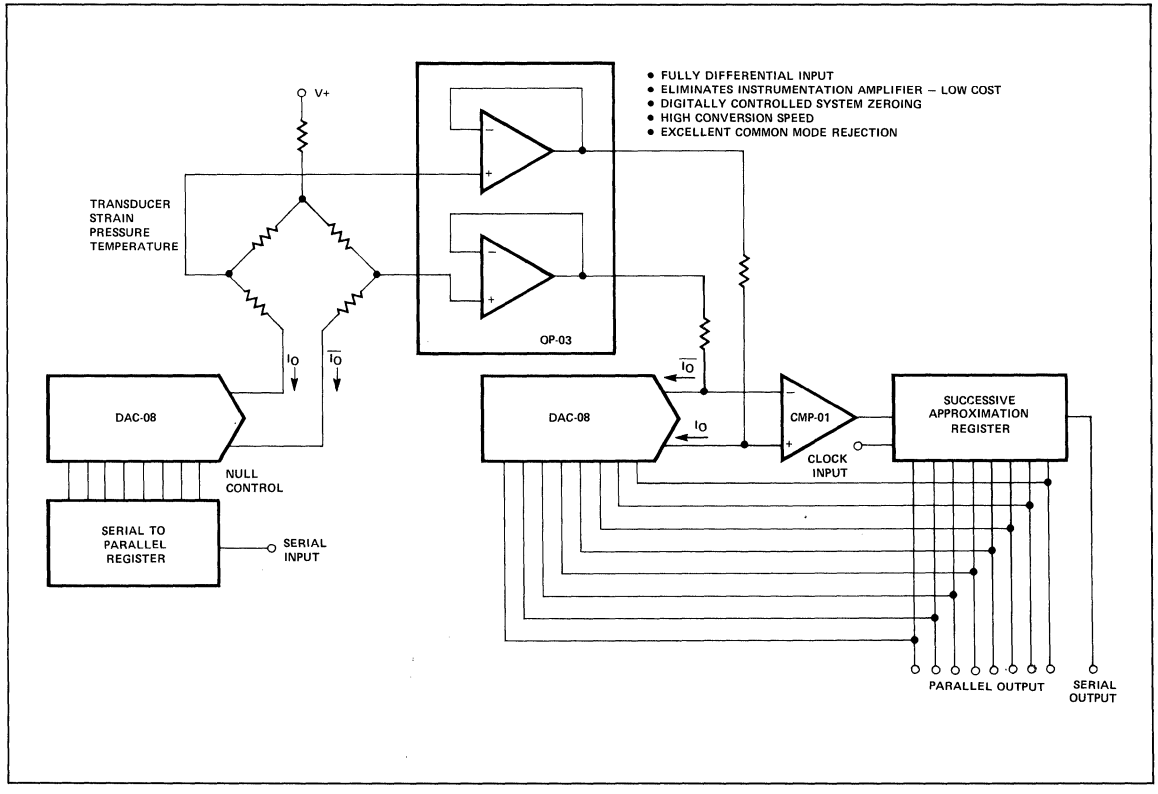


Figure 9. Bridge Transducer Control System with Full Differential Input

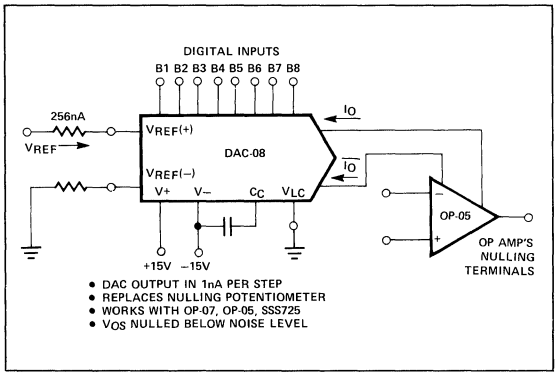


Figure 10. Digitally Controlled Offset Nulling

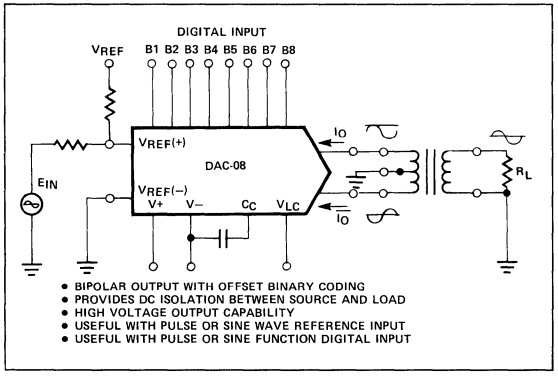


Figure 11. Balanced Transformer Drive

HIGH SPEED

Sub-microsecond settling times are common in current-output DACs. Many DACs settle in 500ns; 300ns is not unusual. But 85ns settling time for a low-cost DAC is exceptional, and this characteristic allows the use of the DAC-08 in formerly difficult and expensive-to-build applications:

1. 1μs, 2μs and 4μs A/Ds. (These are completely described in AN-16.)
2. 15MHz Tracking A/Ds.
3. ECL compatible applications.
4. Video displays requiring a low-glitch DAC.
5. Radar pulse height analysis system.

LOGIC INPUTS

ADJUSTABLE INPUT LOGIC THRESHOLD

Most DACs have TTL or CMOS compatible inputs which require complicated interfaces for use with ECL, PMOS, NMOS or HTL logic. By contrast, the DAC-08, with typical logic input current of 2μA and an adjustable input logic threshold, interfaces easily with any logic family in use today. The logic input threshold is 1.4V positive with respect to Pin 1; for TTL Pin 1 is therefore grounded; for other families Pin 1 is connected as shown in the interfacing figure. An adjustable threshold and a −10V to +18V input range greatly simplify system design especially with other-than-TTL logic. The circuits shown in c and d provide a $2V_{BE}$ V_{LC} compensation to minimize temperature drift.

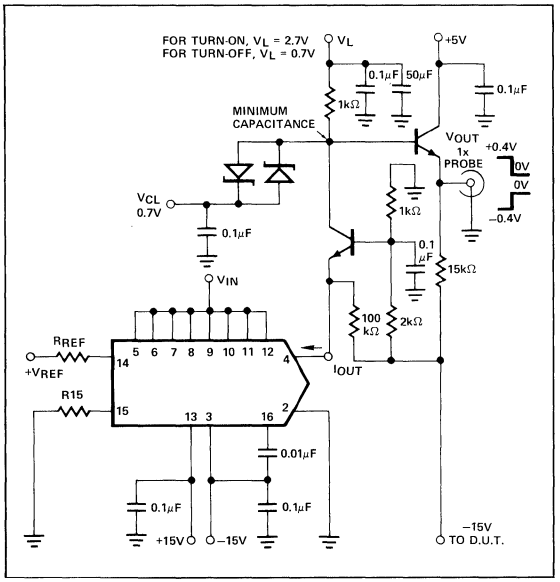


Figure 12. Settling Time Measurement Circuit

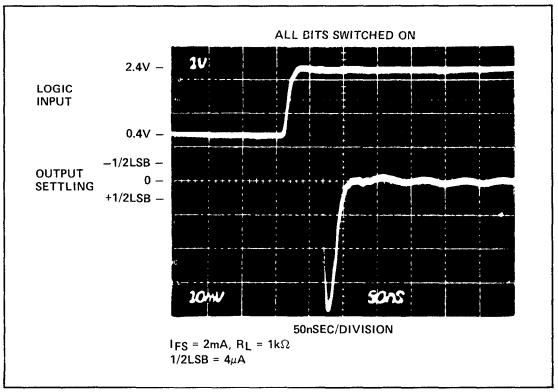


Figure 13. Full Scale Settling Time

1. ECL applications without level translators.
2. Direct interfaces with Hi-Z RAM outputs.
3. CMOS applications without static discharge considerations.
4. HTL or HNIL applications without level translators.
5. System size, weight, and cost reduction.

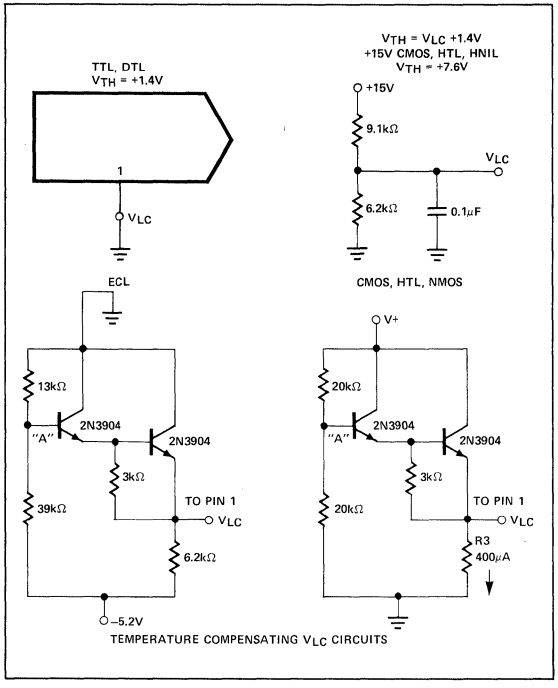


Figure 14. Interfacing with Various Logic Families ($V_{TH} = V_{LC} + 1.4V$)

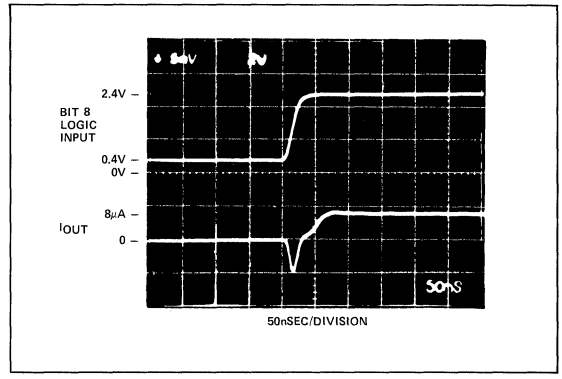


Figure 16. LSB Switching

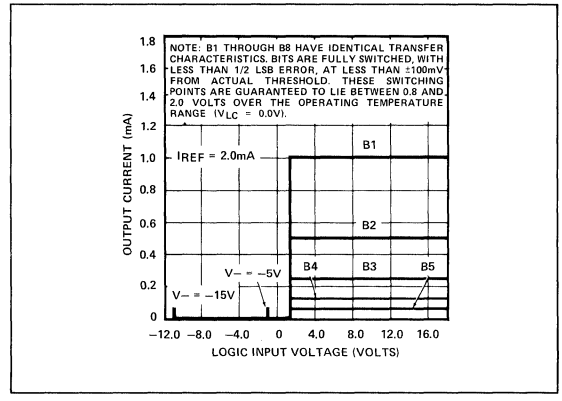


Figure 17. Bit Transfer Characteristics

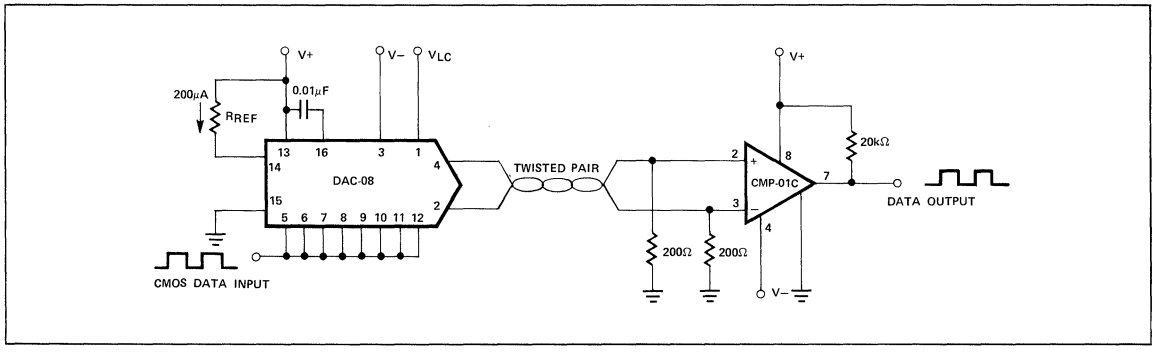


Figure 15. CMOS Differential Line Driver/Receiver

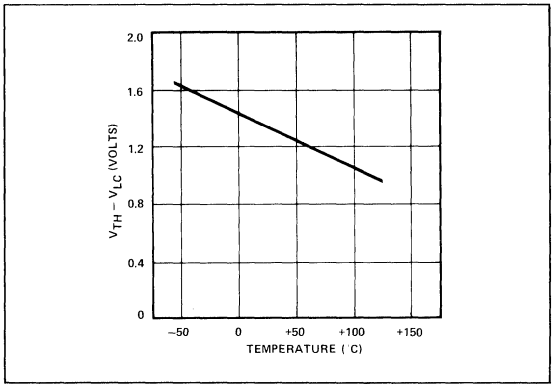


Figure 18. $V_{TH} - V_{LC}$ vs Temperature

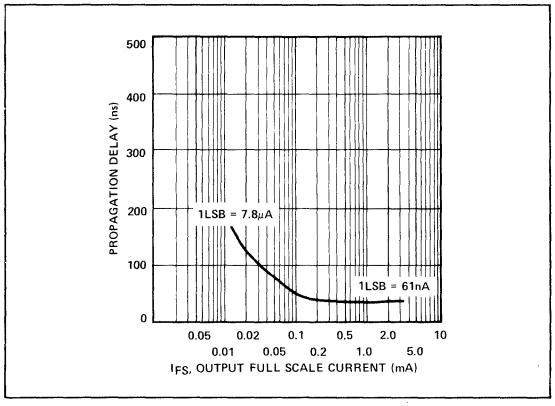


Figure 19. LSB Propogation Delay vs I_{FS}

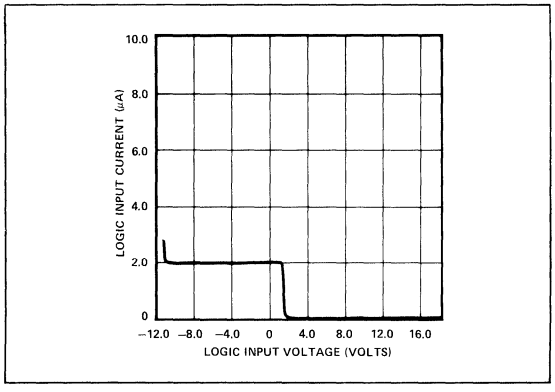


Figure 20. Logic Input Current vs Input Voltage

REFERENCE INPUTS

MULTIPLYING CAPABILITY

Fixed internal references are included in many DACs, but they limit the user to non-multiplying, single-polarity reference applications and do not allow a single-system reference. To achieve the design goals of low cost and total applications flexibility, the DAC-08 uses an external reference. Positive or negative references may be applied over a wide common-mode voltage range. In addition, the full-scale current is matched to the reference current eliminating calibration in most applications.

1. Digitally controlled full-scale calibration.
2. 8 x 8 multiplication of two digital words.
3. Digital Attenuators/Programmable gain amplifiers.
4. Modem transmitters to 1MHz.
5. Remote shutdown and party line DAC applications.

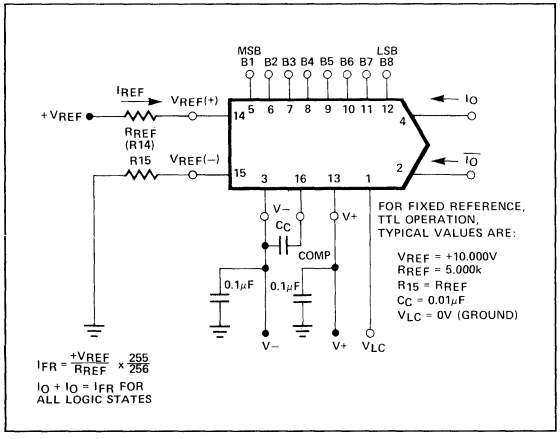


Figure 21. Basic Positive Reference Operation

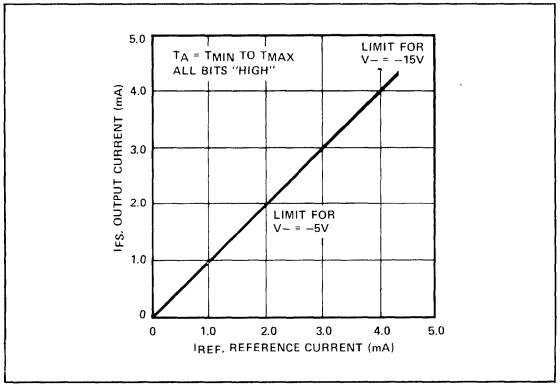


Figure 22. Full-Scale Current vs Reference Current

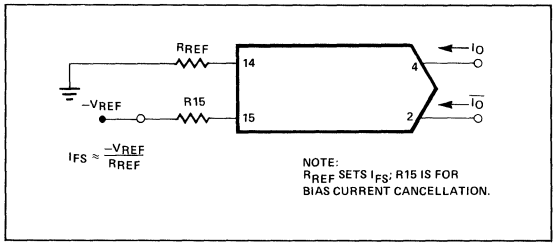


Figure 23. Basic Negative Reference Operation

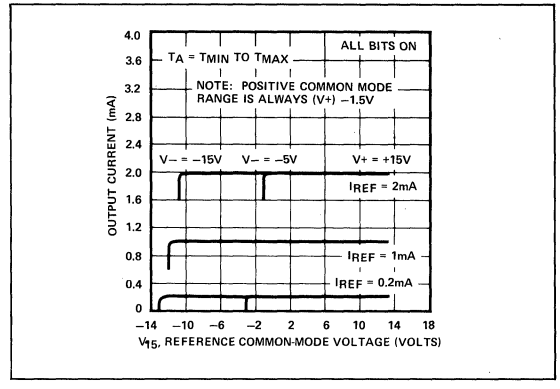


Figure 24. Reference Amp Common-Mode Range

HIGH SPEED

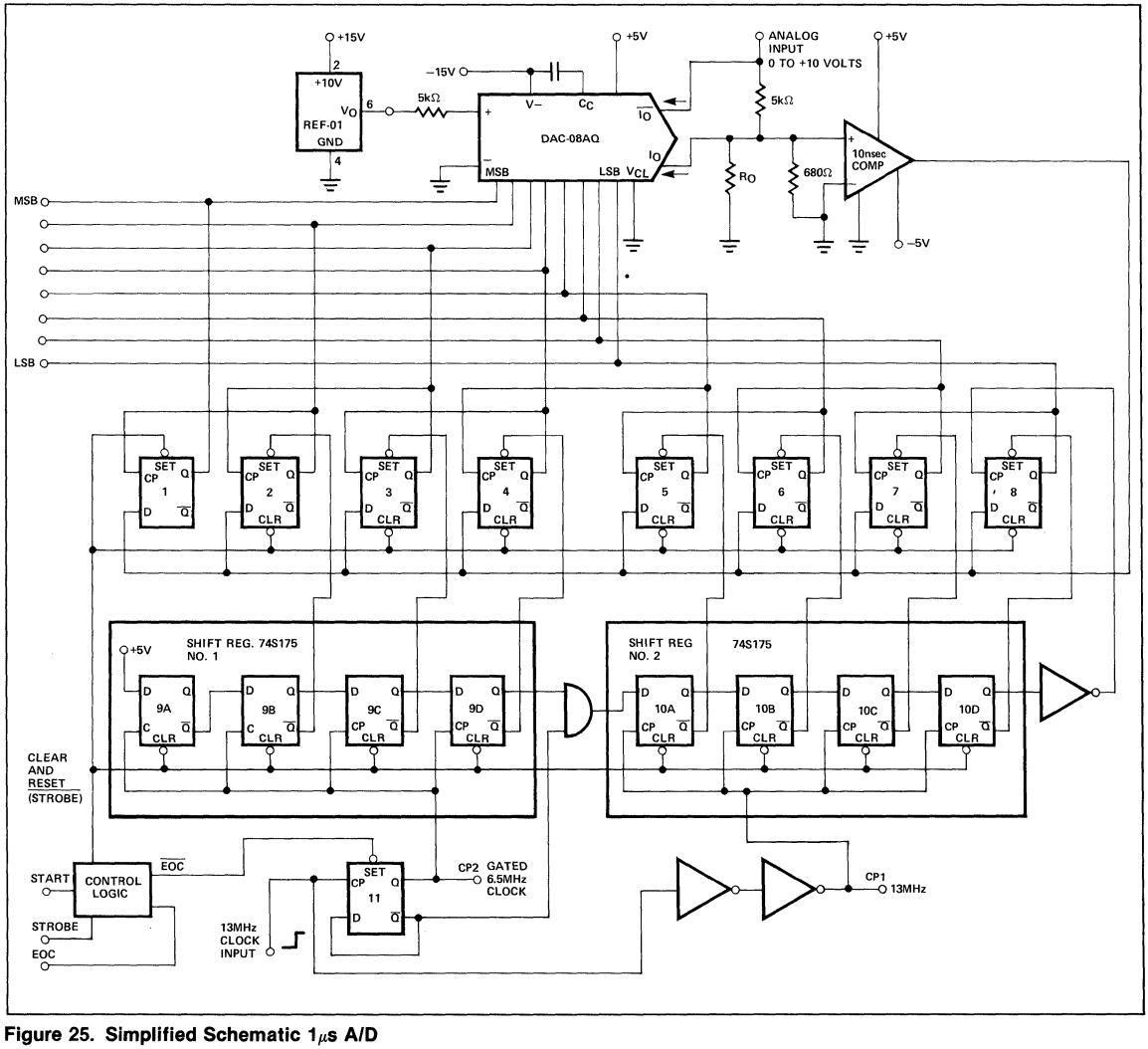
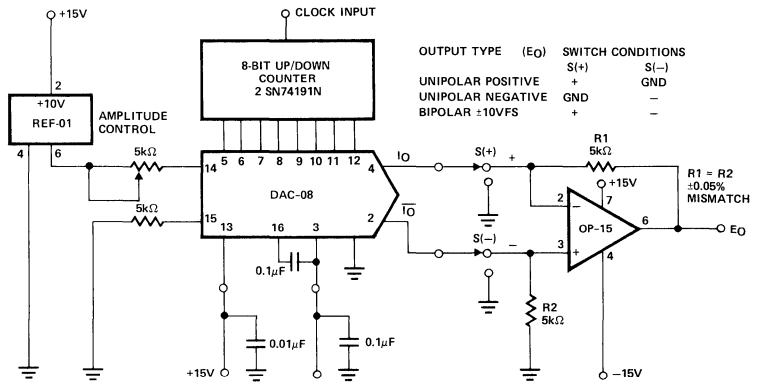


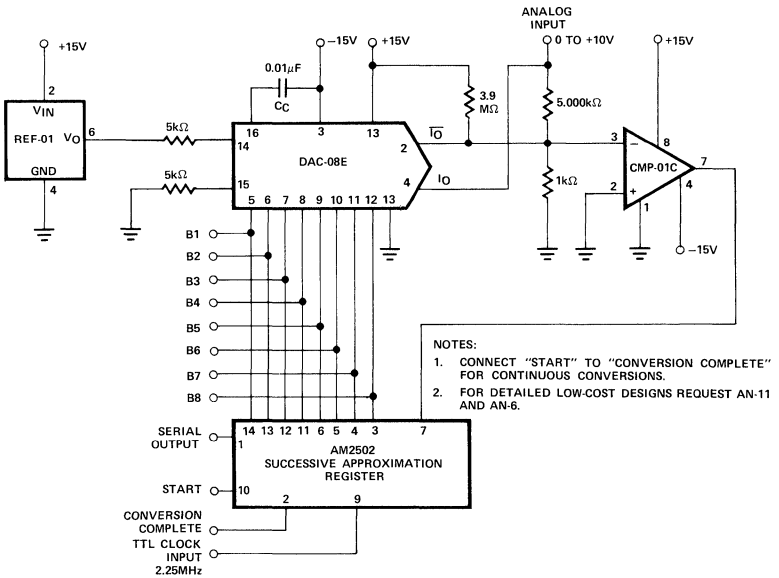
Figure 25. Simplified Schematic 1μs A/D



NOTES:

1. BIPOLAR OUTPUT IS SYMMETRICAL AROUND ZERO. ADJUSTABLE PEAK-TO-PEAK AMPLITUDE.
2. FOR TRIANGLE WAVE, COUNT UP TO FULL REVERSE AND COUNT DOWN.
3. FOR POSITIVE-GOING SAWTOOTH, COUNT UP TO FULL CLEAR, REPEAT.
4. FOR NEGATIVE-GOING SAWTOOTH, COUNT DOWN. CLEAR REPEAT.
5. FOR OTHER WAVEFORMS, USE A ROM PROGRAMMED WITH THE DESIRED FUNCTION.
6. 85nSEC SETTLING TIME PERMITS WAVEFORM PERIOD OF 25.6μSEC OR 39kHz REPETITION RATE IN THE UNIPOLAR POSITIVE MODE.

Figure 26. High-Speed Waveform Generator



NOTES:

1. CONNECT "START" TO "CONVERSION COMPLETE" FOR CONTINUOUS CONVERSIONS.
2. FOR DETAILED LOW-COST DESIGNS REQUEST AN-11 AND AN-6.

Figure 27. Four IC Low-Cost A/D Converter

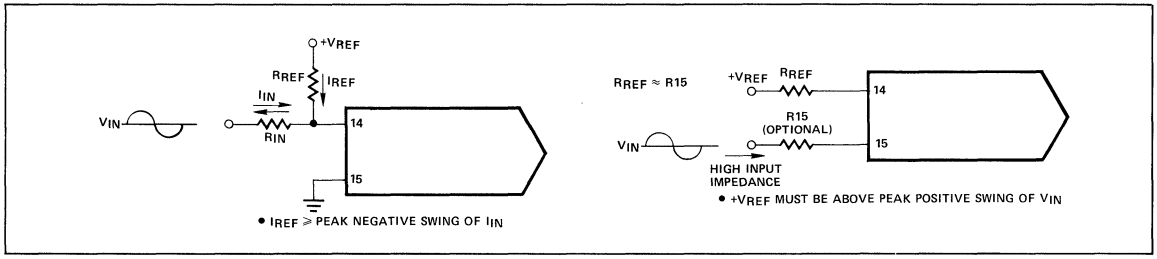


Figure 28. Accommodating Bipolar References

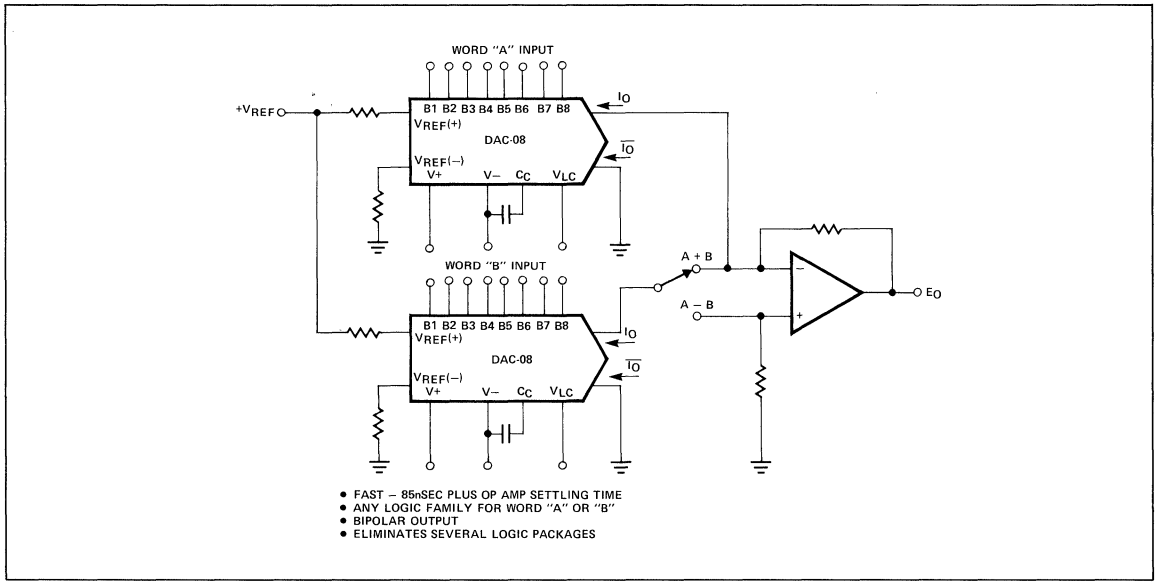


Figure 29. Digital Addition or Subtraction with Analog Output

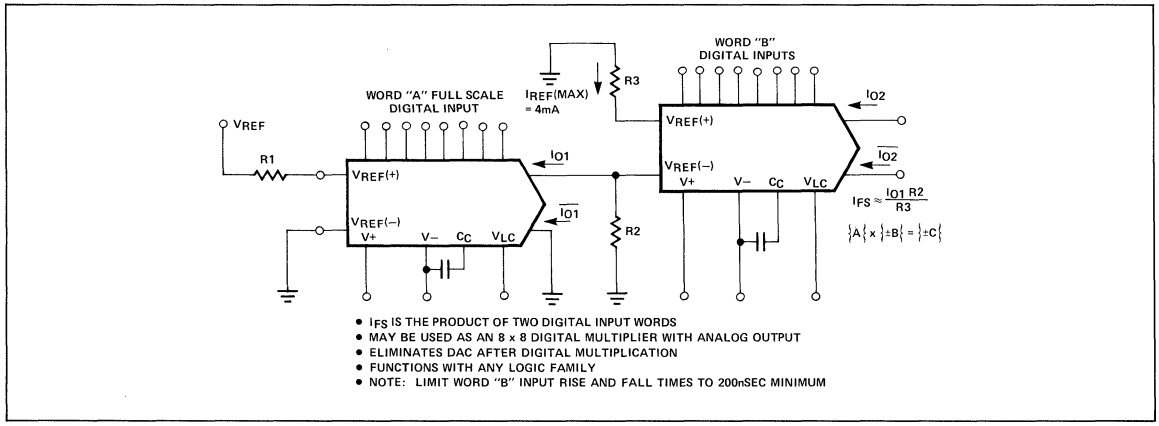


Figure 30. Digitally Controlled Full-Scale Calibration (Multiplier)

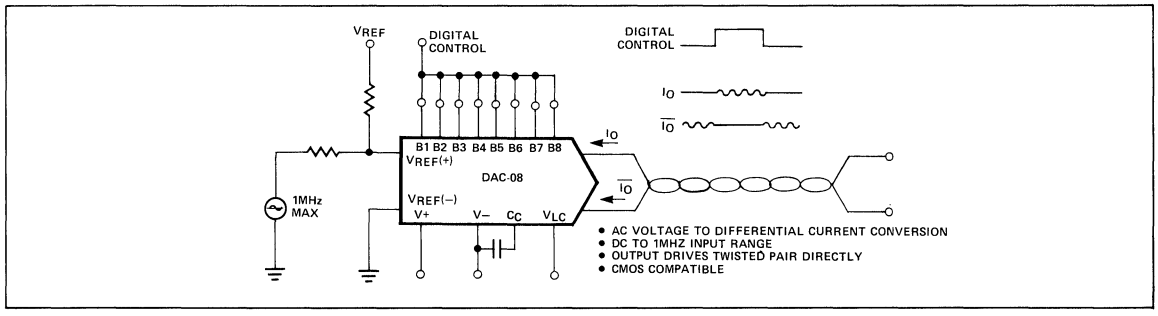


Figure 31. Modem Transmitter

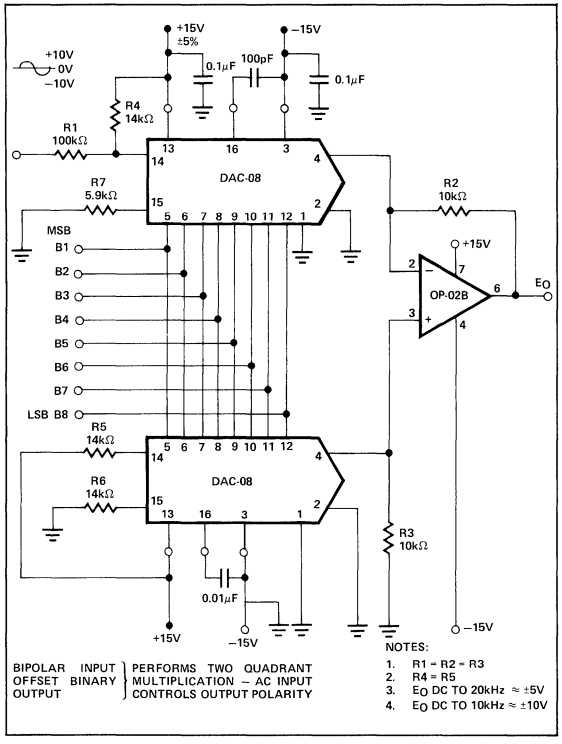


Figure 32. DC-Coupled Digital Attenuator/ Programmable Gain Amplifier

POWER SUPPLIES

POWER SUPPLY REQUIREMENTS

The DAC-08 works with ±4.5V to ±18V supplies allowing use with all standard digital and analog system supply voltages plus most battery voltages. With only 33mW of power dissipation at ±5V and 85ns settling time, it has a lower speed power product than CMOS DACs. Power dissipation is almost constant over temperature, and bypassing is accomplished with 0.01μF capacitors — no large electrolytics are required. These power supply requirements allow:

1. Battery operation.
2. Use of unregulated or poorly regulated power supplies.
3. Use in space-limited areas due to small bypass capacitors.
4. Use in constant power dissipation applications.
5. Common digital and analog power supplies.

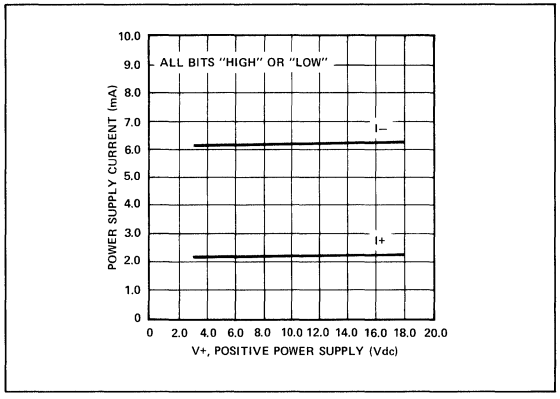


Figure 33. Power Supply Current vs V+

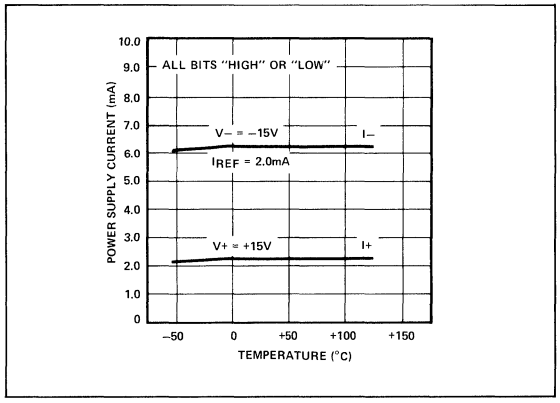


Figure 34. Power Supply Current vs Temperature

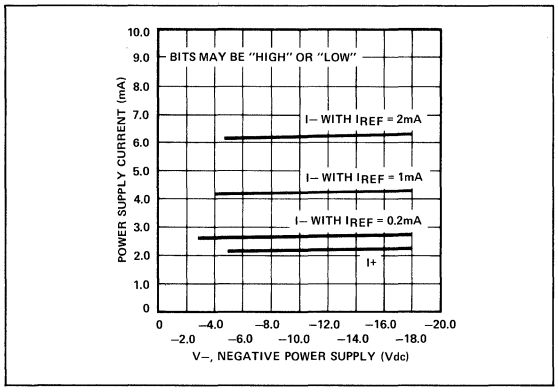


Figure 35. Power Supply Current vs V–

OTHER APPLICATIONS

MICROPROCESSOR APPLICATIONS

The ability to use μP power supply voltages and the ability to interface with any logic family make the DAC-08 especially useful in μP applications:

1. Tracking A/D converters.
2. Successive approximation A/D converters.
3. Direct drive from Hi-Z MOS RAM outputs.

By programming the ROMs with the successive approximation or the tracking A/D algorithm, all of the logic for A/D conversion is contained in the μP. This is a very inexpensive approach, since there is no need for the usual A/D conversion logic packages.

CONCLUSION

High voltage compliance complementary current outputs, universal logic inputs and multiplying capability make the Precision Monolithics DAC-08 the most versatile monolithic high-speed DAC available today.

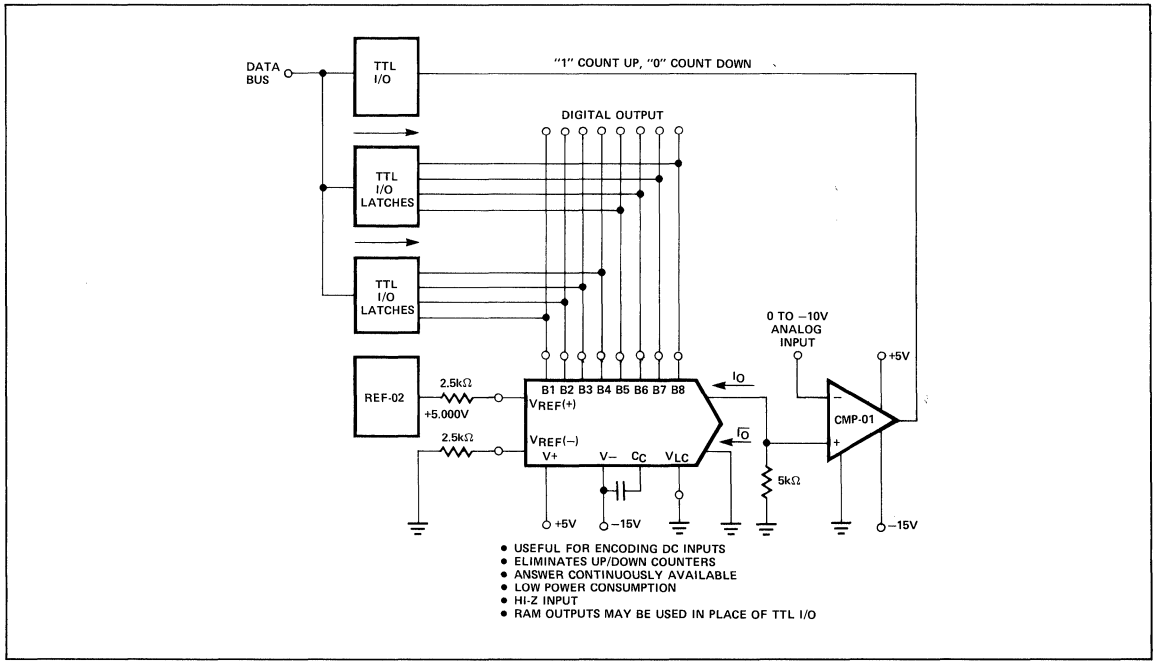


Figure 36. Microprocessor Controlled Tracking A/D Converter

INTRODUCTION

This application note describes electronic thermometer applications of the REF-02 +5V Voltage Reference where the voltage output is a direct measurement of temperature in °C or in °F. These applications use the predictable 2.1mV/°C TEMP output voltage temperature coefficient of the REF-02, a byproduct of a bandgap voltage reference design. Thermometer applications are described first followed by a discussion of bandgap voltage reference theory.

THERMOMETER ESSENTIALS

In addition to a highly linear temperature sensitive component, electronic thermometers should have the following characteristics:

1. Convenient scaling such as 10mV/°C, 100mV/°C, or 10mV/°F.
2. Direct voltage readings such as −0.55V at −55°C, 0V at 0°C, and +1.25V at +125°C.
3. Room temperature calibration.

BASIC CIRCUIT IMPLEMENTATION

The simplified schematic in Figure 1 shows the basic thermometer connections. An operational amplifier, three resistors, and the +5.000V output of the REF-02 function together to level shift and amplify V_{TEMP} allowing V_{OUT} to read in the desired manner. The expression for V_{OUT} is:

$$\text{EQ 1. } V_{OUT} = \left(1 + \frac{R_c}{R_a \| R_b}\right) V_{TEMP} - \frac{R_c}{R_a} (V_{REF})$$

The first term is the gain of the circuit with V_{REF} equal to 0V; the second term is the gain of the circuit with V_{TEMP} equal to 0V. Differentiating Equation 1 with respect to temperature gives the slope, S, of the output-versus-temperature curve:

$$\text{EQ 2. } \frac{dV_{OUT}}{dT} = S = m\left(1 + \frac{R_c}{R_a \| R_b}\right)$$

$$= 2.1\text{mV/°C}\left(1 + \frac{R_c}{R_a \| R_b}\right)$$

$$\text{where } m = TCV_{TEMP}$$

Thus, the ratio of R_c to $R_a \| R_b$ sets the slope of V_{OUT}, and the ratio of R_c to R_a and V_{REF} set the initial output value at 25°C. Table 1 lists typical scaling ratios for different output scales.

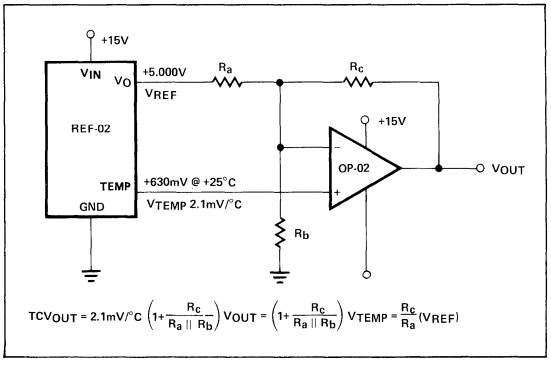


Figure 1. Simplified Schematic

Table 1. Temperature Scaling Ratios

$V_{REF} = 5.000V, V_{TEMP} = 630mV @ 25°C, TCV_{TEMP} = 2.1mV/°C$

V_{OUT} @ 25°C (77°F)	TCV_{OUT} (Slope)	$\frac{R_c}{R_a}$	$\frac{R_c}{R_a \| R_b}$
250mV	10mV/°C	0.55	3.76
2.5V	100mV/°C	5.50	46.6
770mV	10mV/°F	0.926	7.57

COMPLETE CIRCUIT

Two potentiometers, R_p and R_{bp}, have been added to the circuit for precise calibration and to allow for the ±1% resistor tolerances. V_{REF} is adjusted by R_p to set the V_{OUT} value at +25°C (77°F); the ratio of R_c to $R_a \| R_b$ is adjusted by R_{bp} to set the slope of V_{OUT} versus temperature. Resistor values for typical output scales are shown in Table 2.

Table 2. Resistor Values

TCV_{OUT} SLOPE(S)	10mV/°C	100mV/°C	10mV/°F
TEMPERATURE RANGE	−55° to +125°C	−55° to +125°C	−67°F to +257°F
OUTPUT VOLTAGE RANGE	−0.55V to +1.25V	−5.5V to +12.5V*	−0.67V to +2.57V
ZERO SCALE	0V@0°C	0V@0°C	0V@0°F
R_a (±1% resistor)	9.09kΩ	15kΩ	8.25kΩ
R_{b1} (±1% resistor)	1.5kΩ	1.82kΩ	1.0kΩ
R_{bp} (potentiometer)	200Ω	500Ω	200Ω
R_c (±1% resistor)	5.11kΩ	84.5kΩ	7.5kΩ

*For 125°C operation, the op amp output must be able to swing to +12.5V; increase V_{IN} to +18V from +15V if this is a problem.

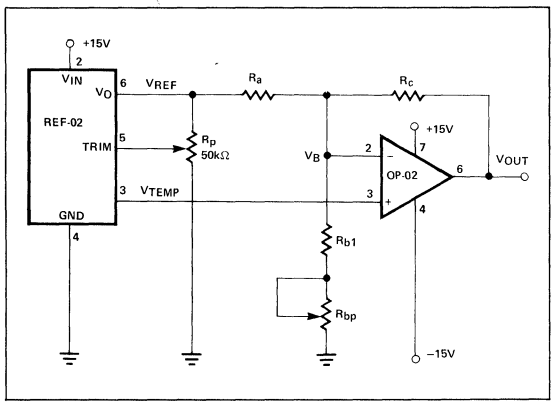


Figure 2. Complete Schematic

CALIBRATION CONDITIONS

All calibration is conducted in free air. Heatsinking of the REF-02 is unnecessary and is undesirable. The small (2°C) rise in chip temperature of the REF-02 above ambient temperature serves as an error-cancelling factor of some second order effects internal to the REF-02 design. The calibration procedure which follows assumes free air — no heatsinking — calibration.

CALIBRATION PROCEDURE

Calibration is performed at ambient temperature with two adjustments using the following procedure:

Step 1: Measure and record V_{TEMP} and T_A in °C.

Step 2: Calculate the calibration ratio "r" using Equation 3:

EQ 3. $$r \equiv \frac{R_a \| R_b}{R_c + R_a \| R_b} = \frac{V_{TEMP} \text{ in mV}}{S(T_A + 273)}$$

Where S = TCV_{OUT}, T_A = ambient temperature in °C

Step 3: Turn power off, short V_{REF} terminal to ground, and apply a precise 100mV to the V_{OUT} terminal.

Step 4: Adjust R_{bp} so that $V_B = r(100mV)$; remove short.

Step 5: Turn power on; adjust R_p so that V_{OUT} equals the correct value at ambient temperature.

The system is now calibrated.

CALIBRATION EXAMPLE

Here is an example at $T_A = 25°C$, $S = 10mV/°C$, and $V_{TEMP} = 632mV$:

Step 1: $V_{TEMP} = 632mV$, $T_A = 25°C$.

Step 2: Using Equation 3:

$$r = \frac{V_{TEMP}}{S(T_A + 273)} = \frac{632}{10(25 + 273)} = \frac{632}{2980} = 0.2121$$

Step 3: Apply 100.00mV to V_{OUT} with power off and V_{REF} connected to ground.

Step 4: Adjust R_{bp} so that $V_B = r(100mV) = 21.21mV$.

Step 5: Turn power on and adjust R_p so that V_{OUT} equals +0.25V.

The system is now calibrated.

TRANSDUCER ERROR FACTORS

Error terms are threefold:

1. Slope errors — Deviations from nominal slope. For example, if the slope is 10.04mV/°C instead of 10.00mV/°C, the accuracy due to the slope error is 0.4%.
2. Linearity errors — Deviations in V_{TEMP} versus temperature from straight line performance, a change in V_{TEMP} slope with temperature.
3. Offset error — V_{OUT} deviations due to changes in V_{REF} with temperature.

Since these errors are grade dependent, Table 3 is provided as an aid in specifying the correct combination of components for a given application. Offset error can be eliminated by using one REF-02 as a temperature sensor only and another REF-02 (operated at a constant temperature) as V_{REF}.

Table 3. Typical Transducer Performance vs Grade

GRADE / PARAMETER	REF-02A	REF-02	REF-02E	REF-02H	REF-02C
TEMPERATURE RANGE	−55° to +125°C	−55° to +125°C	0° to +70°C	0° to +70°C	0° to +70°C
SLOPE ERROR	±0.30%	±0.40%	±0.25%	±0.35%	±0.45%
TCV_{TEMP} ERROR	±0.10%	±0.12%	±0.08%	±0.10%	±0.15%
OFFSET ERROR	±0.15%	±0.40%	±0.10%	±0.30%	±0.60%
RMS ERROR SUM	±0.35%	±0.58%	±0.28%	±0.47%	±0.76%
TYPICAL ACCURACY	0.50%	0.75%	0.40%	0.60%	0.90%
OP-02 GRADE RECOMMENDED	OP-02A	OP-02	OP-02E	OP-02C	OP-02C

TRANSDUCER PERFORMANCE

Typical system accuracy is ±0.5% over the −55° to +125°C range of a REF-02A. For example, when calibrated at +25°C, the reading of V_{OUT} at +105°C may be 105.4°C, a deviation of 0.5% of the 80° temperature change (+25°C to +105°C).

Although the REF-02 is guaranteed to perform over the −55° to +125°C range only, operation beyond those limits is possible. A large number of devices were measured and found to be functioning satisfactorily over the −150°C to +170°C range, and there was only a slight degradation in accuracy.

REMOTE APPLICATIONS

In many applications, the sensor must be located some distance away from the measurement circuitry. One precaution must be taken with the REF-02: a 1.5kΩ resistor should be connected between Pin 3 (TEMP) and its associated cable conductor to isolate this pin from cable capacitances.

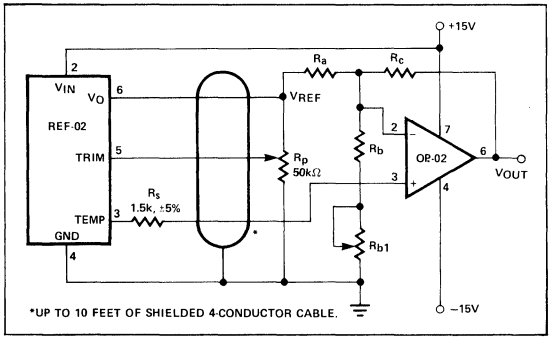


Figure 3. Precision Temperature Transducer with Remote Sensor

Remote application of the transducer is illustrated in Figure 3 with R_S, the isolation resistor.

TRANSDUCER SUMMARY

The accuracies indicated compare quite favorably to traditional temperature measurement methods such as thermocouples and thermistors. Ease-of-use, low cost, and high accuracy make this new bandgap method of temperature measurement attractive in a wide range of applications.

The following section describes the bandgap principle in theory and its use in the internal REF-02 design.

BANDGAP REFERENCE THEORY

Bandgap voltage references (1), (2), (3), use predictable relationships from semiconductor physics to generate a constant voltage. The base-emitter voltage of a transistor (V_{BE}) has a processing and current density dependent **negative** temperature coefficient of about −2.1mV/°C. Another well-known relationship with a **positive** temperature coefficient is the difference between base-emitter voltages of two transistors operated at different current densities:

EQ 4. $$\Delta V_{BE} = \frac{kT}{q} \log_e \left(\frac{J2}{J1}\right), \text{ where}$$

k = Boltzmann's constant = 1.38 x 10^{-23} joules/°K

T = absolute temperature, °K

q = charge of an electron = 1.6 x 10^{-19} coulomb

J = current density

When ΔV_{BE} is amplified and added to V_{BE}, a voltage reference with zero temperature coefficient results if the sum (V_Z) of these two terms equals the linearly-extrapolated bandgap voltage of silicon (V_{go}) at 0°K or −273°C, V_{go} = 1.205V. A more exact calculation, see reference 2, will show that V_Z will have zero temperature coefficient if:

EQ 5. $$V_Z = V_{go} + \frac{kT}{q} = 1.230V @ +25°C$$

The circuit in Figure 4 generates a ΔV_{BE} of 72mV at 25°C by making the current density of Q2 16 times greater than Q1. Q2 has four times the current of Q1, and Q1 has four times the emitter area of Q2. A ΔV_{BE} of 72mV appears across R1

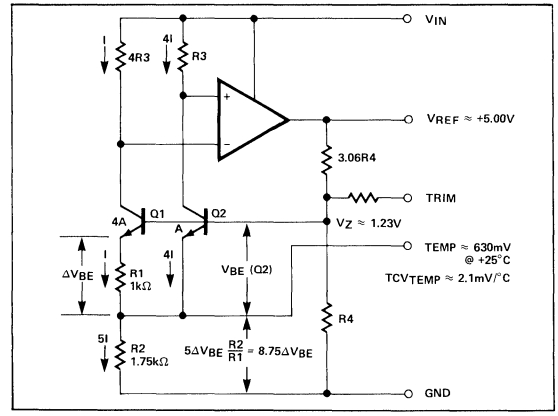


Figure 4. REF-02 Simplified Schematic

Table 4. REF-02 Typical Nodal Voltages

VOLTAGE \ TEMPERATURE	T_A = −75°C (T_J = 200°K)	T_A = +25°C (T_J = 300°K)	T_A = +125°C (T_J = 400°K)
$\Delta V_{BE} = \frac{kT}{q} \log_e 16$	48mV	72mV	96mV
$V_{TEMP} = 8.75\ \Delta V_{BE}$	420mV	630mV	840mV
$V_{BE}(Q2)$	810mV	600mV	390mV
$V_{REF} \approx V_{BE} + V_{TEMP}$	1.23V	1.23V	1.23V
$V_{REF} \approx 1 + \frac{3.06R4}{R4}$ $\approx 4.06V_Z$	5.00V	5.00V	5.00V

and is amplified by 8.75 (becoming the TEMP output) and is added to V_{BE} (Q2) to produce a nearly constant V_Z of 1.23V. The −2.1mV/°C of TCV_{BE} is cancelled by the +2.1mV/°C of TCV_{TEMP}; and V_Z is amplified by 4.06 to produce an output of V_{REF} of 5.000V.

CONCLUSION

The REF-02, by using a bandgap design, provides both a stable +5V reference voltage output and an additional output voltage directly proportional to temperature. Accurate electronic thermometers reading in °C or in °F can be constructed at low cost for a wide variety of temperature monitoring and controlling applications.

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2. "A Precision Reference Voltage Source"
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IEEE Journal of Solid-State Circuits
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INTRODUCTION

The introduction of low-cost monolithic D/A converters has simplified data acquisition and control system design. This application note describes several new applications using the multiplying capability and dual complementary current outputs of the Precision Monolithics DAC-08.

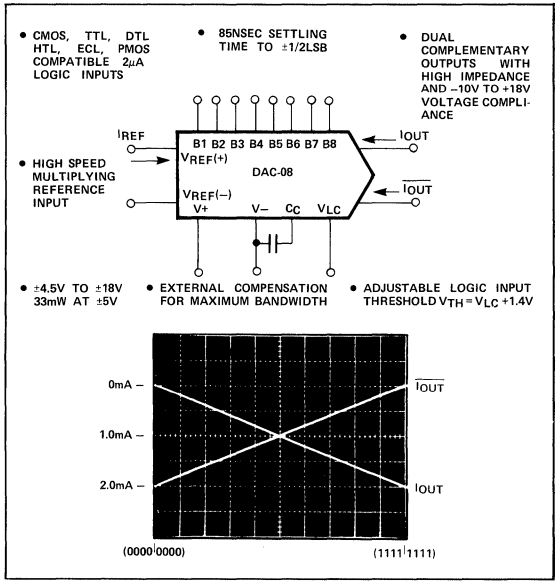


Figure 1. The Universal DAC

MULTIPLYING DAC BASICS

A multiplying DAC has an analog output which is the product of a digital input word and a reference voltage and can be expressed as:

$$(1.)\ E_O = E_{REF}\left(\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right)$$

For a current reference, current output DAC, the expression becomes:

$$(2.)\ I_O = I_{REF}\left(\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right)$$

The DAC-08 has complementary/differential current outputs, and I_O has a complement expressed as:

(3.) $\overline{I_O} = I_{FS} - I_O$ for all input logic states.

The relationship of I_{REF} to I_O and $\overline{I_O}$ is illustrated in Figure 2 and in Figure 3, the basic DC reference connections. References may be either positive or negative, and a bipolar output voltage may be achieved using the high compliance current outputs alone or with an output operational amplifier. The simplest form of a multiplying DAC accepts a unipolar varying reference input.

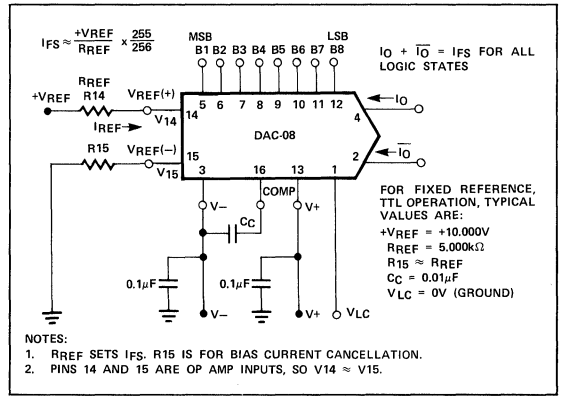


Figure 2. Positive Reference Connection

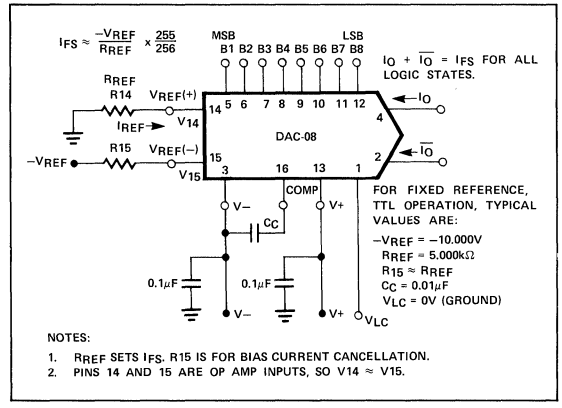


Figure 3. Negative Reference Connection

BIPOLAR REFERENCES

Operation with bipolar references is achieved by modulating I_{REF} as shown in Figure 5. To aid in understanding bipolar operation, see the equivalent circuit in Figure 4. The reference inputs of the DAC-08 are op amp inputs — $V_{REF}(+)$ being the inverting input and $V_{REF}(-)$ being the noninverting input. Excellent gain linearity of the reference amplifier allows multiplying operation over a range of I_{REF} of 4μA to 4mA with monotonic operation from less than 100μA to 4mA.

REFERENCE AMPLIFIER COMPENSATION

AC reference applications will require the reference amplifier to be compensated using a capacitor from Pin 16 to V–. The value of this capacitor depends on the impedance presented to Pin 14: for R_{IN} values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37, and 75pF. Larger values of R_{IN} require proportionately increased values of C_C for proper phase margin.

FAST PULSED OPERATION

For fastest multiplying response, low values of R_{IN} enabling small C_C values should be used. For R_{IN} = 1kΩ and C_C = 15pF, the reference amplifier slews at 4mA/μs enabling a transition from I_{REF} = 0 to I_{REF} = 2mA in 500ns. If R_{IN} or the parallel equivalent resistance at Pin 14 is less than 200Ω, no compensation capacitor is necessary, and a full-scale transition requires only 16ns.

TWO-QUADRANT MULTIPLICATION

There are two forms of two-quadrant multiplication: bipolar digital, where the digital input word controls output polarity, and bipolar analog, where the analog reference input controls output polarity.

Bipolar digital two-quadrant mutliplication is shown in Figure 6 with the output polarity being controlled by an offset-binary-coded digital input word.

Bipolar analog two-quadrant multiplication is shown in Figure 7. A bipolar reference voltage is connected to the upper DAC-08 and modulates the reference current by ±1.0mA around a quiescent current of 1.1mA. The lower DAC-08 also has a reference current of 1.1mA; due to the parallel digital inputs, the lower DAC-08 effectively subtracts out the quiescent 1.1mA of the upper DAC-08's reference current at all in-

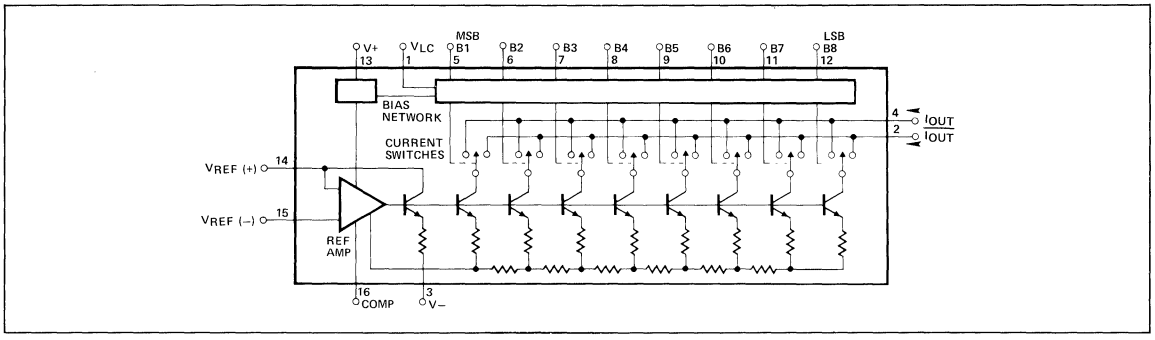


Figure 4. DAC-08 Equivalent Circuit

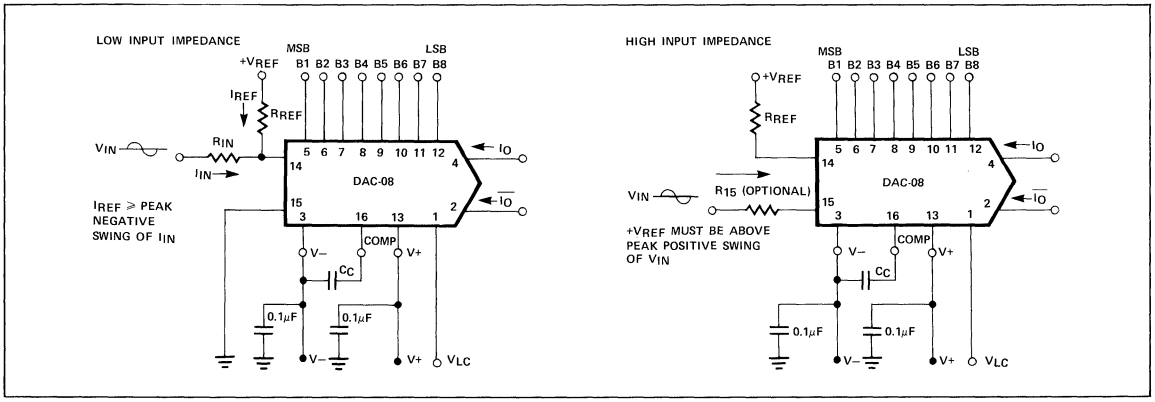
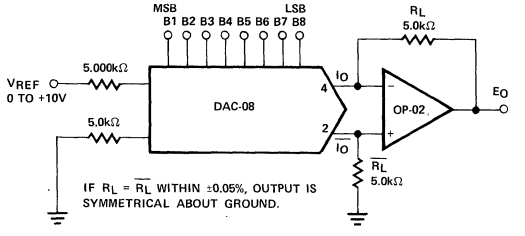


Figure 5. Bipolar Reference Connections

put codes, since the voltage across R3 varies between −10V and 0V. Thus, the output voltage, E_O, is a product of a digital input word and a bipolar analog reference voltage.



	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O (V)
POS. FULL SCALE	1	1	1	1	1	1	1	1	1.992	0.000	+9.96
POS. FULL SCALE − LSB	1	1	1	1	1	1	1	0	1.984	0.008	+9.88
(+) ZERO SCALE	1	0	0	0	0	0	0	0	1.000	0.992	+0.040
(−) ZERO SCALE	0	1	1	1	1	1	1	1	0.992	1.000	−0.040
NEG. FULL SCALE + LSB	0	0	0	0	0	0	0	1	0.008	1.984	−9.88
NEG. FULL SCALE	0	0	0	0	0	0	0	0	0.000	1.992	−9.96

Figure 6. Bipolar Digital Two-Quadrant Multiplication (Symmetrical Offset Binary)

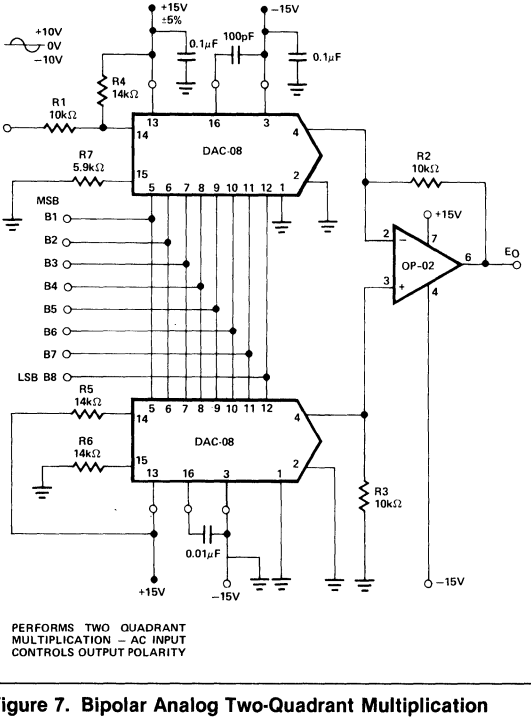


Figure 7. Bipolar Analog Two-Quadrant Multiplication (DC-Coupled Digital Attenuator)

FOUR-QUADRANT MULTIPLICATION

Four-quadrant multiplication combines the two forms of two-quadrant multiplication. Output analog polarity is controlled by either the analog input reference or by the offset binary digital input word. One implementation of this function with the DAC-08 is shown in Figure 8 with output current values listed in Table 1.

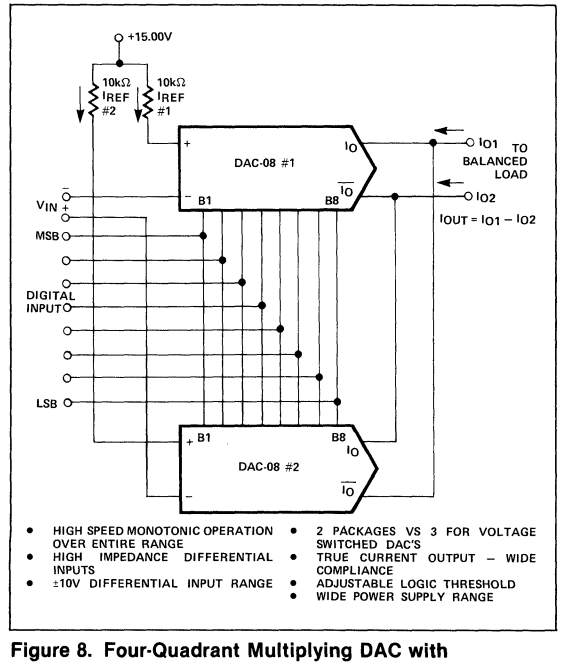


Figure 8. Four-Quadrant Multiplying DAC with with Impedance Input

The four-quadrant multiplying DAC circuit shown accepts a differential voltage input and produces a differential current output. An output op amp is not shown because it is not always required; many applications are more suited for high output compliance (−10V to +18V) differential current outputs. Typical balanced loads include transformers, transducers, transmission lines, bridges and servos.

Operation of the four-quadrant multiplier may be more easily visualized by considering that if either $V_{IN} = 0V$ or the offset binary digital input code is at midscale (corresponding to zero), then a change in the other input will not affect the output. Zero multiplied by any number equals zero.

A common mode current will be present at the output and must be accommodated by the balanced load. A pair of matched resistors may be used at the outputs to shunt most of the common mode current to ground, thus reducing the common mode voltage swing at the output.

Table 1. Four-Quadrant Multiplying Current Values in Figure 8.

DIGITAL INPUT	$V_{IN}(+)$	$V_{IN}(-)$	V_{IN} DIFF.	I_{REF} #1 (mA)	I_{REF} #2 (mA)	I_O#1 (mA)	I_O#2 (mA)	I_{O1} (mA)	I_O#2 (mA)	I_O#1 (mA)	I_{O2} (mA)	I_{OUT} DIFF.
1111 1111	+5V	−5V	+10V	2.000	1.000	1.992	0	1.992	0.996	0	0.996	0.996mA
1000 0000	+5V	−5V	+10V	2.000	1.000	1.000	0.496	1.496	0.500	0.992	1.492	0.004mA
0111 1111	+5V	−5V	+10V	2.000	1.000	0.992	0.500	1.492	0.496	1.000	1.496	−0.004mA
0000 0000	+5V	−5V	+10V	2.000	1.000	0	0.996	0.996	0	1.992	1.992	−0.996mA
1111 1111	0V	0V	0V	1.500	1.500	1.494	0	1.494	1.494	0	1.494	0.000mA
1000 0000	−10V	−10V	0V	2.500	2.500	1.250	1.240	2.490	1.250	1.240	2.490	0.000mA
0111 1111	+10V	+10V	0V	0.500	0.500	0.248	0.250	0.498	0.248	0.250	0.498	0.000mA
0000 0000	0V	0V	0V	1.500	1.500	0	1.494	1.494	0	1.494	1.494	0.000mA
1111 1111	−5V	+5V	−10V	1.000	2.000	0.996	0	0.996	1.992	0	1.992	−0.996mA
1000 0000	−5V	+5V	−10V	1.000	2.000	0.500	0.992	1.492	1.000	0.496	1.496	−0.004mA
0111 1111	−5V	+5V	−10V	1.000	2.000	0.496	1.000	1.496	0.992	0.500	1.492	0.004mA
0000 0000	−5V	+5V	−10V	1.000	2.000	0	1.992	1.992	0	0.996	0.996	0.996mA

HIGHEST SPEED FOUR-QUADRANT MULTIPLYING CONSIDERATIONS

The configuration shown in Figure 10 makes use of the DAC-08's ability to operate in a fast-pulsed reference mode without compensation capacitors. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ($I_{REF} = 0$) condition. This connection yields a reference slew rate of 16mA/μs which is relatively independent of R_{IN} and V_{IN} values.

Input resistances are not limited to 10kΩ. For example, 100kΩ resistors for R_{IN1} and R_{IN2} allow ±100V reference voltage inputs making this connection especially useful in high common mode voltage environments. Except for different reference treatment, operation and digital input coding are identical in the circuits shown in Figure 8 and in Figure 10; both have the transfer function shown in Figure 9.

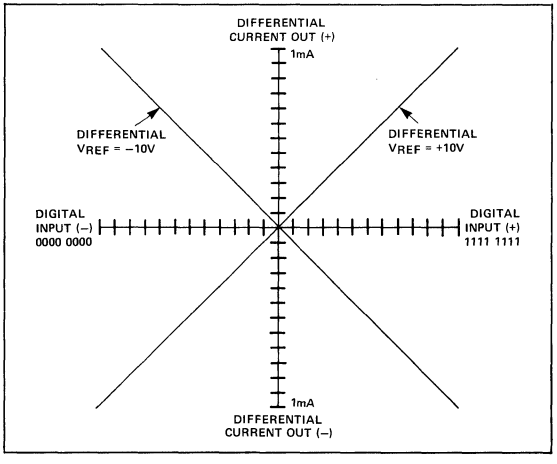


Figure 9. Four-Quadrant Multiplying DAC Transfer Function

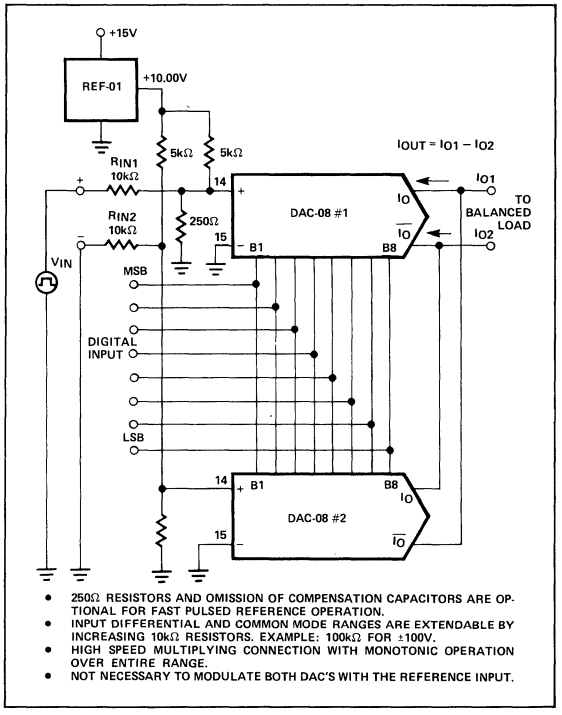


Figure 10. Four-Quadrant Multiplying DAC with Extendable Input Range and Highest Speed

AC-COUPLED MULTIPLICATION

Some multiplying DAC applications are more easily achieved with AC coupling. At the same time, a high impedance input is often required to avoid loading a relatively high source impedance. Both requirements are met by the circuits shown in Figure 11 and Figure 12 which use the compensation

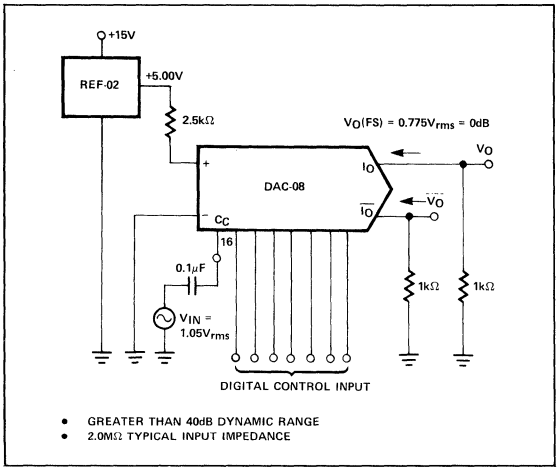


Figure 11. High Input Impedance AC-Coupled Multiplication (Audio Frequency Digital Attenutor)

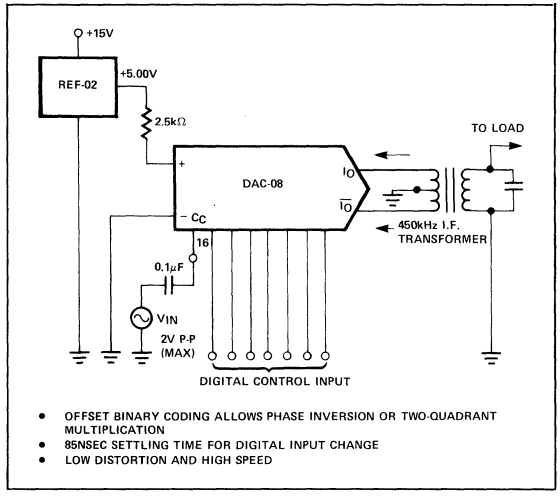


Figure 12. High Input Impedance AC-Coupled Multiplication (I.F. Amplifier/Digital Attenuator)

capacitor terminal (C_C) as an input. This is possible because C_C is the base of a transistor whose emitter is one diode drop (0.7V) away from the R-2R ladder network common baseline internal to the DAC-08.

With a full-scale input code the output, V_O, is flat to >200kHz and is 3dB down at approximately 1.0MHz making this type of multiplying connection useful even beyond the audio frequency range. Such a connection is illustrated in Figure 12 operating at 455kHz, the highest recommended operating frequency in this connection.

DIFFERENTIAL AND RATIOMETRIC A/D CONVERSION

Complementary/differential current-source outputs and multiplying capability allow the DAC-08 to be used in differential and ratiometric A/D converter designs directly without signal conditioning amplifiers. This group of applications begins with the basic differential A/D converter and ratiometric A/D converter connections followed by more specific applications.

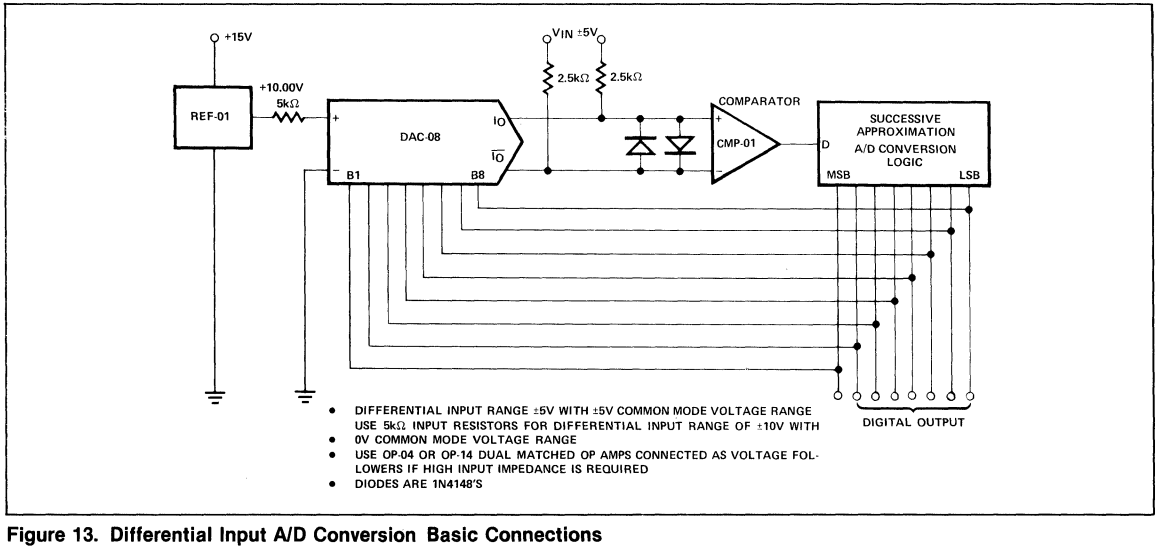


Figure 13. Differential Input A/D Conversion Basic Connections

These are extremely cost-effective designs due to their low parts count and simplicity. Alternative designs performing identical functions require instrumentation amplifiers for the differential-to-single-ended input signal conditioning and analog multipliers or dividers for the arithmetic functions.

DIFFERENTIAL A/D CONVERSION

The circuit in Figure 13 uses the high voltage compliance current output capability of the DAC-08 and the high common mode voltage rejection of the CMP-01 to construct a differential input ADC without input signal conditioning.

A successive approximation ADC is constructed with four ICs: a REF-01 +10V reference, a 2502-type successive approximation register, a CMP-01 precision voltage comparator, and a DAC-08. As shown, the circuit converts an analog input in less than 2.0μs. For lower speed requirements, the A/D conversion logic can be the tracking or servo type consisting of up/down counters.

FOUR-QUADRANT RATIOMETRIC A/D CONVERSION

Ratiometric A/D conversion with fully differential X and Y inputs is accomplished with the circuit in Figure 14. Here, one set of inputs, V_X, is connected in a manner similar to the circuit in Figure 13, and the other set of inputs V_Y, is connected in a multiplying fashion. Operation is as follows: I_{REF} for both the upper and the lower DAC-08 is modulated between 1mA and 3mA; and the resulting output currents are differentially transformed into voltages by the 5kΩ resistors at the comparator's inputs and compared with the V_X differential input. When the conversion process is complete (comparator inputs differentially nulled to less than 1/2 LSB) a digital output is available which corresponds to the quotient of V_X/V_Y. Thus, four-quadrant ratiometric A/D conversion is achieved with four ICs and without instrumentation amplifiers.

BRIDGE TRANSDUCER NULL

In many control systems, bridges must be nulled, and a digital representation of the bridge's error must be provided for computer monitoring and control. The circuit in Figure 15 accomplishes both tasks by using the DAC-08 complementary/differential current outputs to null the bridge with the DAC-08 connected in a tracking differential A/D converter configuration. The REF-02 reference voltage source provides both the bridge excitation voltage and the positive reference voltage for the DAC-08. Some of the advantages of this circuit are listed at the bottom of Figure 15.

POWER MONITOR

Another differential current-input ADC is shown in Figure 16 with a transformer-coupled input. An up/down counter, a precision high-speed comparator, and the DAC-08 form a tracking A/D converter which continuously monitors the analog input. Two precautions must be observed: the common mode voltage at the comparator's inputs must not ex-

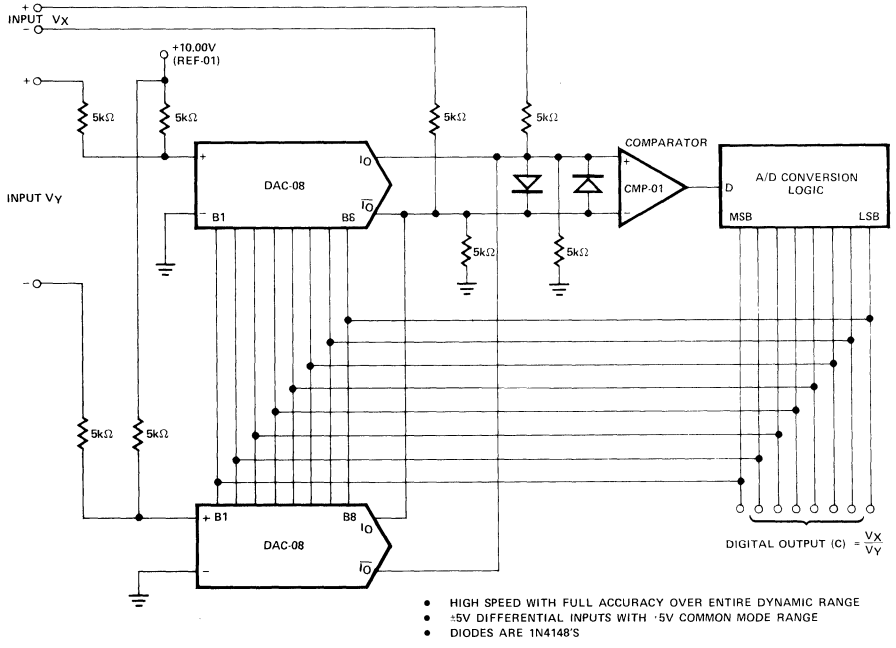


Figure 14. Four-Quadrant Ratiometric A/D Conversion Basic Connections

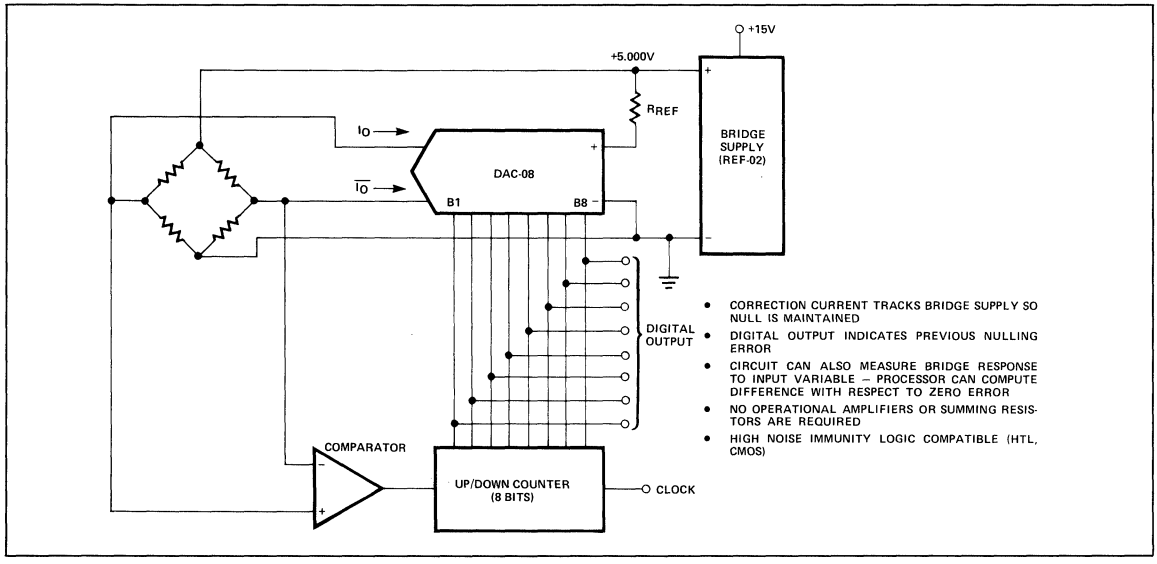


Figure 15. Bridge Transducer Null

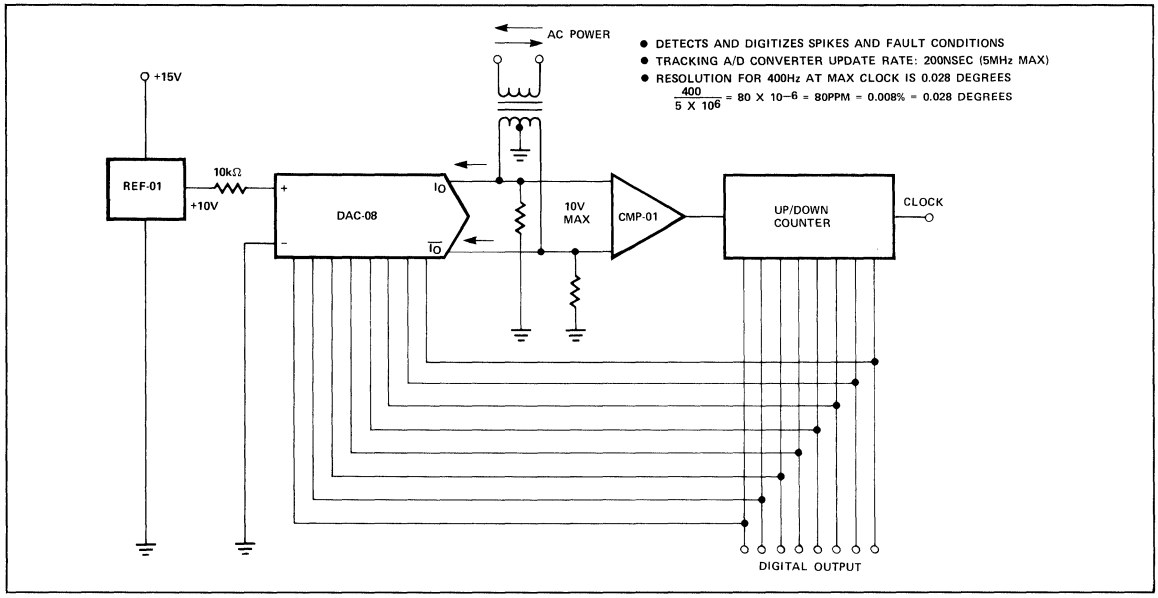


Figure 16. Power Fault Monitor and Detector

ceed ±10V; and the differential voltage must not exceed 11V. Voltage-limiting resistors at the comparator's inputs are recommended.

ALGEBRAIC DIGITAL COMPUTATION

Frequently, a digital arithmetic operation (addition, subtraction, multiplication, or division) must be performed, and an analog output must be provided. Traditionally, the arithmetic operations are performed with several ICs, and the output drives a D/A converter. This section decribes applications of the DAC-08 as an arithmetic building block, new design approaches that reduce the number of packages required in many applications. Today's low cost, versatile DACs merit a designer's consideration as arithmetic elements.

One benefit is not immediately apparent and deserves special mention. In all of these applications, the digital input words can be CMOS, TTL, DTL, NMOS, or MECL, because the DAC-08 interfaces with all of those logic families. In fact, the two input words may even be from different logic families to eliminate special level translators or interface circuitry. (See AN-17 "DAC-08 Applications Collection.")

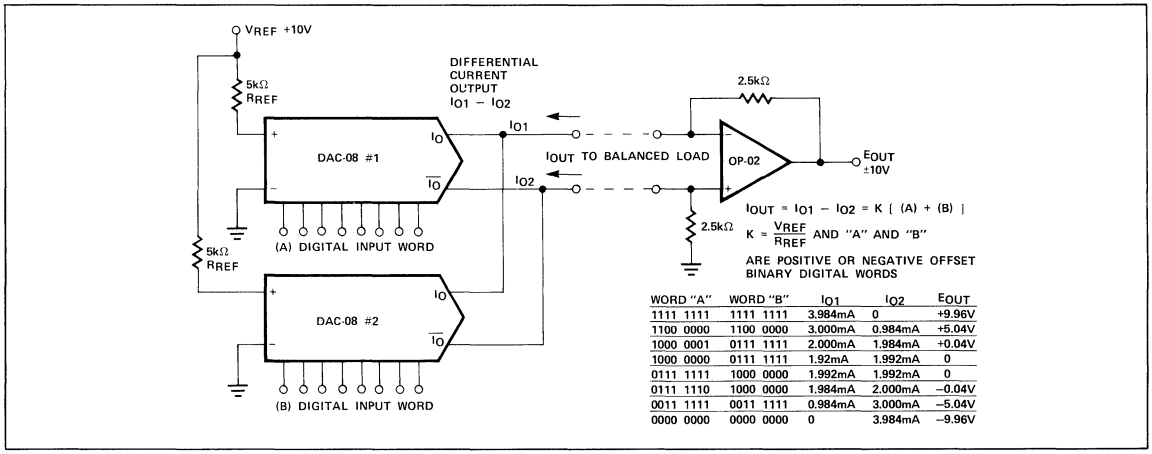
The first arithmetic application is shown in Figure 17. Two DAC-08s perform a fast algebraic summation with a direct analog output. The circuit works by paralleling the outputs of two DAC-08s and summing their currents while driving a balanced load. The output is the algebraic sum of word "A" and word "B" in all four quadrants.

FOUR-QUADRANT DIGITAL MULTIPLICATION

High-speed multiplication of two 8-bit digital words with an analog output usually requires several logic packages and a D/A converter. The circuit in Figure 18 performs this function using only three ICs.

In Figure 18 DAC-08 number 1 and number 2 are connected as previously shown, and DAC-08 number 3 provides the analog reference inputs to DAC-08 number 1 and number 2. Those reference inputs are determined by digital input word "A." The circuit's output, I_{01}-I_{02}, is a differential current output which may be used to drive a balanced load.

Four-quadrant multiplication is thus performed by adding one more DAC-08 to the basic four-quadrant multiplying connection.



WORD "A"	WORD "B"	IO1	IO2	EOUT
1111 1111	1111 1111	3.984mA	0	+9.96V
1100 0000	1100 0000	3.000mA	0.984mA	+5.04V
1000 0001	0111 1111	2.000mA	1.984mA	+0.04V
1000 0000	0111 1111	1.92mA	1.992mA	0
0111 1111	1000 0000	1.992mA	1.992mA	0
0111 1110	1000 0000	1.984mA	2.000mA	–0.04V
0011 1111	0011 1111	0.984mA	3.000mA	–5.04V
0000 0000	0000 0000	0	3.984mA	–9.96V

Figure 17. Four-Quadrant Algebraic Digital Computation

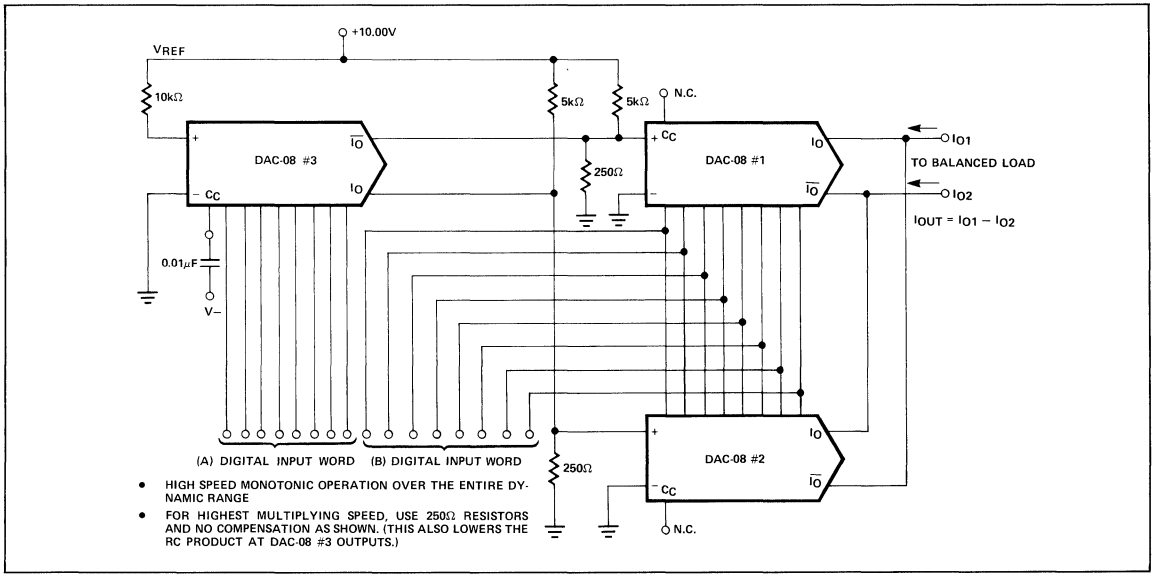


Figure 18. Four-Quadrant 8-Bit × 8-Bit Digital Multiplier

PMI

AN-20

EXPONENTIAL DIGITALLY CONTROLLED OSCILLATOR USING DAC-86

Precision Monolithics Inc.

APPLICATION NOTE 20

Here is a four-IC, microprocessor-controlled oscillator with a 8159 to 1 frequency range covering 2.5Hz to 20kHz. An exponential, current output IC DAC functioning as a programmable current source alternately charges and discharges a capacitor between precisely-controlled upper and lower limits. This circuit features instantaneous frequency change, operates with +5V ±1V and −15V ±3V supplies, and provides monotonic frequency changes over a 78dB range — the dynamic range of a 13-bit DAC.

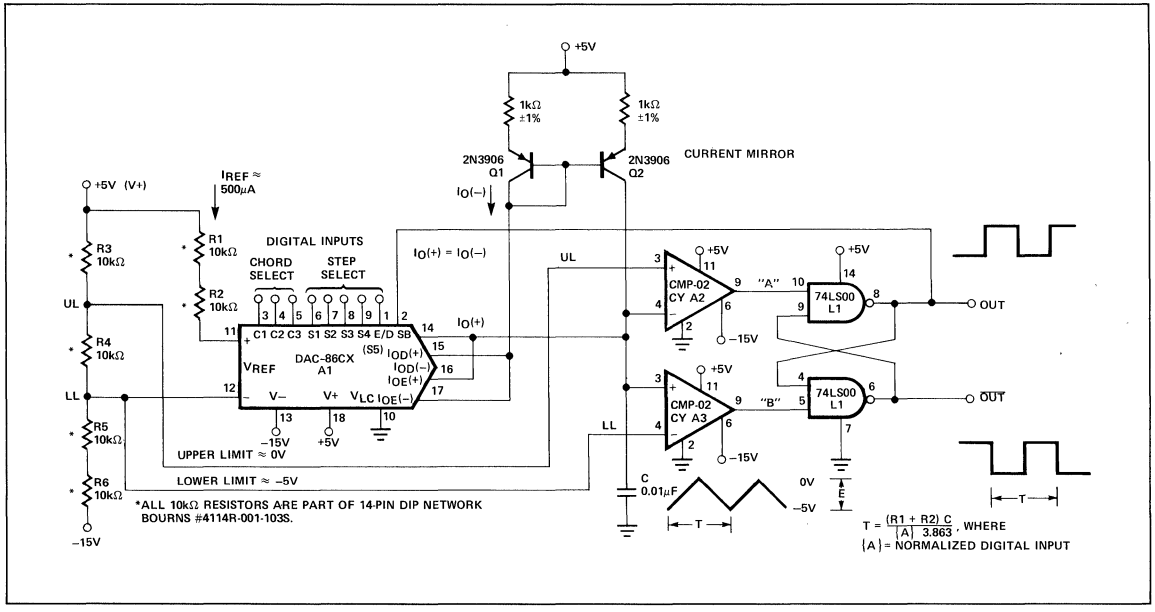
BASIC OPERATION

Connected as shown below, the output of the exponential DAC is an eight-chord (or segment) current ranging between 250nA and 2.0mA. The three most significant bits select 1 of 8 binarily-related chords; and the five least significant bits select 1 of 32 linear steps within each chord. This current is switched between the $I_O(+)$ output and the $I_O(-)$ output under the control of a pin labeled SB (Pin 2).

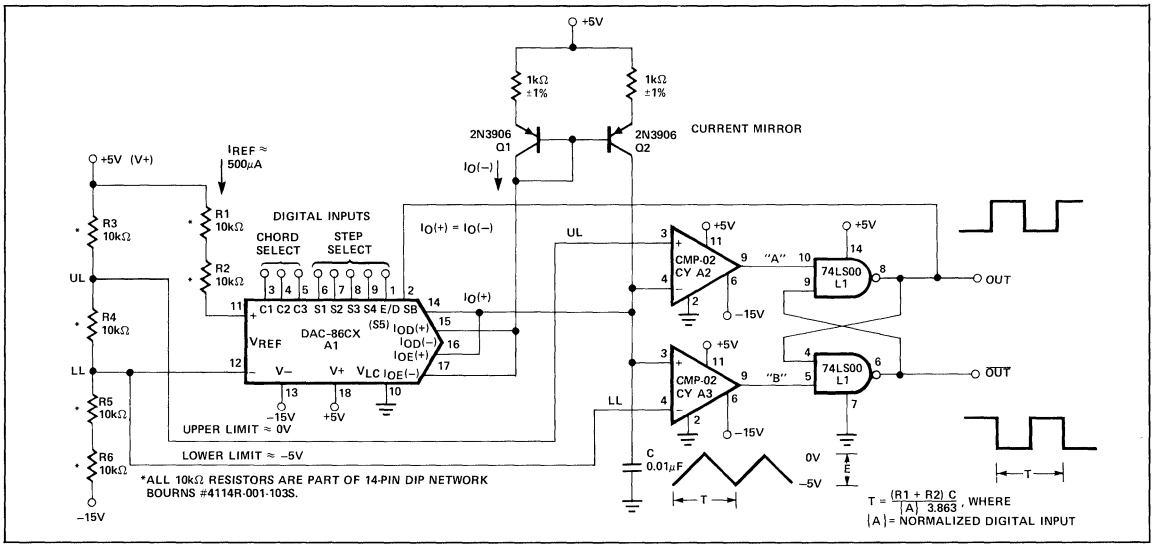
When SB is low, $I_O(-)$ is selected, and the DAC's output current drives a current mirror which ramps the timing capacitor in a positive direction until an upper limit of 0V is sensed by A2. At this time the set-resist flip-flop (L1) is set, SB becomes a "1", and the DAC's output current is switched to the $I_O(+)$ output. Now the capacitor is charged to a lower limit of −5V, the flip-flop is reset, and the cycle repeats itself.

REFERENCE SETUP

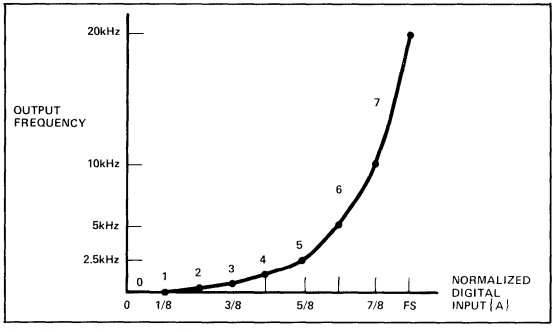
The multiplying relationship between the reference current, I_{REF}, and the full-scale output of the DAC is 3.863. I_{REF} is set by the voltage between V+ and the lower limit divided by R1 + R2. This is so because Pin 12, $V_{REF}(-)$, is a high-impedance input, namely the noninverting input of an op amp internal to the DAC. Since both I_{REF} and the upper and lower limits are derived by dividing down the power supply voltages, operation (frequency of oscillation) is independent of power supply changes. (See Appendix for a complete derivation of the timing formula.)



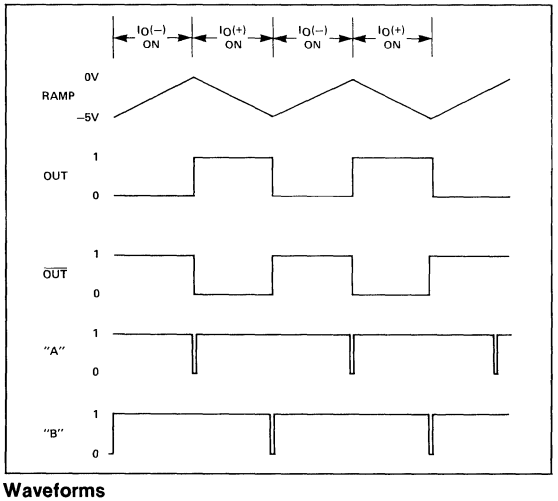
Circuit Diagram Exponential Digitally-Controlled Oscillator



Circuit Diagram Exponential Digitally-Controlled Oscillator



Oscillator Transfer Function



Waveforms

Table 1. Ideal Output Frequency

CHORD (SEGMENT)	DIGITAL INPUT CODE	NORMALIZED DIGITAL INPUT |A|	OUTPUT FREQUENCY	AVERAGE STEP SIZE
0	000 00001	$\frac{1}{8159}$	2.45Hz	2.3Hz
	000 01000	$\frac{8}{8159}$	19.6Hz	
	000 11111	$\frac{31}{8159}$	76.0Hz	
1	001 00000	$\frac{33}{8159}$	80.9Hz	4.8Hz
	001 11111	$\frac{95}{8159}$	233Hz	
2	010 00000	$\frac{99}{8159}$	243Hz	9.5Hz
	010 11111	$\frac{223}{8159}$	547Hz	
3	011 00000	$\frac{231}{8159}$	566Hz	19Hz
	011 11111	$\frac{479}{8159}$	1.17kHz	
4	100 00000	$\frac{495}{8159}$	1.21kHz	38Hz
	100 11111	$\frac{991}{8159}$	2.43kHz	
5	101 00000	$\frac{1023}{8159}$	2.51kHz	76Hz
	101 11111	$\frac{2015}{8159}$	4.94kHz	
6	110 00000	$\frac{2079}{8159}$	5.09kHz	152Hz
	110 11111	$\frac{4063}{8159}$	9.96kHz	
7	111 00000	$\frac{4191}{8159}$	10.3kHz	303Hz
	111 11111	$\frac{8159}{8159}$ = FS	20.0kHz	

FREQUENCY SELECTION

Table 1 lists ideal output frequencies at the lowest and highest codes of each chord and the average change in frequency produced by a one-step change (LSB change) within each chord. For highest accuracy in Chord 0, especially between 2.5Hz and 19.6Hz, comparators with low input current are recommended. The CMP-02CY comparators typically have 35nA of input current; at the lowest code point (000 00001) the DAC output is 250nA; so low input current comparators are essential for best operation. Above 000 01000 (4μA or 19.6Hz) the comparator input currents become less critical.

CONCLUSION

A microprocessor-controlled oscillator has been shown which achieves a 13-bit dynamic range with only 8 bits of control. Monotonic frequency steps over 2.5Hz to 20kHz are provided in a four-IC low-cost design.

REFERENCE

"Eight-bit Frequency Source Suited for μP Control" by Albert Helfrick, **EDN**, September 20, 1976, pp. 116-118.

APPENDIX

TIMING EQUATION DERIVATIONS

One of the best features of this design is its insensitivity to power supply changes. The equation derivations are shown to explain how V+ and V− drop out as timing determinations.

With a constant current drive the charge on C changes linearly over a range (E) between an upper limit (UL) and a lower limit (LL) dependent upon the DAC's digital input code, the DAC's output current, and the value of the timing capacitor (C).

Equation 1. $T = 2\left(\frac{CE}{I}\right)$ where:

C = timing capacitor value

E = upper limit — lower limit

I = DAC output current, $I_O(+)$ or $I_O(-)$

T = period

Equation 2. E = UL − LL where: UL = upper limit
LL = lower limit

Equation 3. $UL = \frac{R4+R5+R6}{R3+R4+R5+R6}\left[(V+)-(V-)\right]+(V-)$

where: V+ = positive power supply and V− = negative power supply

but: R3 = R4 = R5 = R6

$\therefore UL = \frac{3(V+)+(V-)}{4}$

Equation 4. $LL = \frac{R5+R6}{R3+R4+R5+R6}\left[(V+)-(V-)\right]+(V-)$

$LL = \frac{(V+)+(V-)}{2}$

Substituting 3 and 4 into 2 and solving for E:

Equation 5. $E = \frac{(V+)-(V-)}{4}$

Rewriting Equation 1 and substituting 5:

Equation 6. $\frac{T}{2C} = \frac{\left[(V+)-(V-)\right]I}{4}$

The expression for I is:

Equation 7. $I = 3.863\ |A|\ I_{REF}$

where: 3.863 is a constant derived from the ratio of I_{REF} to $I_{FULL\ SCALE}$ of the DAC
A = the normalized digital input code
I_{REF} = the reference current

Equation 8. $I_{REF} = \frac{(V+)-LL}{R1+R2}$

Substituting 4 into 8:

Equation 9. $I_{REF} = \frac{(V+)-\left[\frac{(V+)+(V-)}{2}\right]}{R1+R2}$

$= \frac{(V+)-(V-)}{2(R1+R2)}$

Substituting 9 and 7 into 6:

Equation 10. $\frac{T}{2C} = \frac{\frac{(V+)-(V-)}{4}}{3.863\ |A|\left[\frac{(V+)-(V-)}{2(R1+R2)}\right]}$

Multiplying by |A| 3.863:

Equation 11. $\frac{|A|\ 3.863T}{2C} = \frac{\frac{(V+)-(V-)}{4}}{\frac{(V+)-(V-)}{2(R1+R2)}}$

$\frac{|A|\ 3.863T}{2C} = \frac{R1+R2}{2}$

So V+ and V− have dropped out as timing considerations. Solving for T:

Equation 12. $T = \frac{C(R1+R2)}{3.863\ |A|}$ but: $C = 0.01\mu F$
$R1 = R2 = 10k\Omega$

Equation 13. $T = \frac{5.177 \times 10^{-5}}{|A|}$

Finally, the simplified expressions:

Equation 14. $T \cong \frac{50\mu s}{|A|}$

Equation 15. f (frequency) $\cong \frac{|A|}{50 \times 10^{-6}} \cong$ 20kHz full scale

OTHER DAC APPLICATIONS

The combination of high voltage compliance complementary current outputs, universal logic inputs, and multiplying capability in a low-cost DAC enables widespread application. Consider the following partial list:

A/D CONVERTERS

Tracking (Servo)
Successive Approximation
Ramp (Staircase)
Microprocessor Controlled
Ratiometric (Bridge Balancing)

TEST SYSTEMS

Transistor Tester (Force I_B and I_C)
Resistor Matching (Use both outputs)
Programmable Power Supplies
Programmable Pulse Generators
Programmable Current Source
Function Generators (ROM Drive)

ARITHMETIC OPERATIONS

Analog Division by a Digital Word
Analog Quotient of Two Digital Words
Analog Product of Two Digital Words — Squaring
Addition and Subtraction with Analog Output
Magnitude Comparison of Two Digital Words
Digital Quotient of Two Analog Variables
Arithmetic Operations with Words from Different Logic Families

GRAPHICS AND DISPLAYS

Polar to Rectangular Conversion
CRT Character Generation
Chart Recorder Driver
CRT Display Driver

DATA TRANSMISSION

Modem Transmitter
Differential Line Driver
Party Line Multiplexing of Analog Signals
Multi-Level 2-Wire Data Transmission
Secure Communications (Constant Power Dissipation)

CONTROL SYSTEMS

Reference Level Generator for Setpoint Controllers
Positive Peak Detector
Negative Peak Detector
Disc Drive Head Positioner
Microfilm Head Positioner

AUDIO SYSTEMS

Digital AVC and Reverberation
Music Distribution
Organ Tone Generator
Audio Tracking A/D

CONCLUSION

Differential and multiplying applications have been described which use the high-voltage compliance, complementary-current outputs and the high-speed multiplying inputs of the Precision Monolithics DAC-08.

BIBLIOGRAPHY

1. *"DAC-08 Applications Collection"*, Precision Monolithics Application Note 17
2. *"Low Cost, High-Speed Analog-to-Digital Conversion with the DAC-08"*, Precision Monolithics Application Note 16
3. *"Differential and Multiplying Use of Digital-to-Analog Converters"*, Donn Soderquist and John Schoeff, **E.E. Times** article, June 21, 1976, pp. 40-47

AN-21

4 - 20mA DIGITAL TO PROCESS CURRENT TRANSMITTER

Precision Monolithics Inc.

APPLICATION NOTE 21

This application note describes a three IC, 4-20mA process current, digital-to-analog converter that can be constructed at low cost. It operates from a −5V ±1V negative power supply and a +23V ±7V positive power supply, has 24V output voltage compliance, and occupies less than 4 square inches of printed circuit board space. Other significant features include TTL logic input compatibility, 8-bit binary coding, 0° to +70°C operation, and 5μs full scale settling time into a 500Ω load.

THEORY OF OPERATION

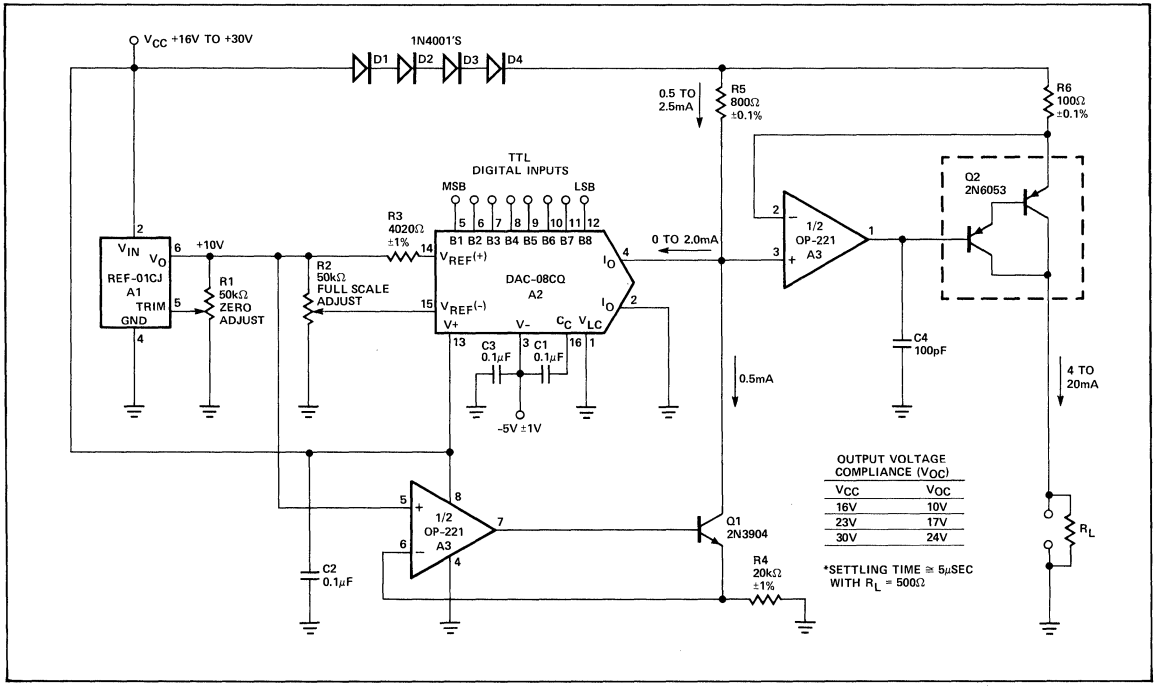
A fixed current of 0.5mA is added to a DAC's output current varying between 0 and 2.0mA and the resulting total current is multiplied by a factor of 8 to produce an output current of 4.0 to 20mA.

In the schematic, first note the REF-01CJ, a +10V adjustable reference. Its output goes to the noninverting input of one half of A3, a dual precision op amp. The inverting input is within a feedback loop forcing +10V to appear at the top of R4, a 20kΩ resistor; a 0.5mA current will flow in R4 through Q1, a high h_{FE} transistor. The same +10V is applied to R3, the reference input resistor of a multiplying IC D/A converter, the DAC-08. Full scale output current of the DAC will be the difference in voltage between the +10V reference and Pin 14 of the DAC divided by R3; Pin 15 will be at the same voltage as Pin 14 because it is a high impedance point, the noninverting input of an op amp internal to the DAC. After calibration a current of 0 to 2mA (depending on the digital input code) will flow into the DAC's output, Pin 4.

Both the DAC's output current and the fixed 0.5mA flow in R5, a 800Ω precision resistor. The voltage developed by that current is applied to the noninverting input of the other half of A3 and will also appear across R6, a 100Ω precision resistor. Thus, eight times the 0.5 to 2.5mA current in R5 flows in R6, or 4 to 20mA. Almost all of this current appears at the output because the 2N6053 is a high h_{FE} device, a power darlington transistor.

Some other components need explanation. C1 provides frequency compensation of the DAC's reference amplifier; C2

SCHEMATIC DIAGRAM



and C3 are power supply decoupling (bypass) capacitors; C4 prevents high frequency oscillations. D1 through D4 insure at least 2.5V differential between the op amp's inputs and its positive power supply under all conditions. R1 and R2 are zero scale and full scale adjustments respectively.

CALIBRATION PROCEDURE

Apply +23V ±7V and −5V ±1V to the converter with a current-measuring meter connected between the output and ground. Make the digital inputs all zeros, < +0.8V. Adjust R1 until the output current is 4.0mA. Now change the digital inputs to all ones, > +2.0V. Adjust R2 until the output current is 20mA. Calibration is now completed.

OUTPUT VOLTAGE COMPLIANCE

Output voltage compliance is V_{CC} −6V. For example, at V_{CC} = +16V, the output may go to a maximum of +10V without affecting output current. Thus, a 500Ω resistor would be the maximum load resistor at V_{CC} = +30V, V_{OC} = 24V, and R_L Maximum = 1.2kΩ.

SCALE MODIFICATION

Although the values shown are for the more common 4-20mA requirement, operation at 1-5mA or 10-50mA may be achieved by changing some components. For 10-50mA, change R6 to 40Ω; this makes the multiplying factor 20 instead of 8. For 1-5mA, replace the 2N6053 with a 2N5087, and change R6 to 400Ω.

CONCLUSION

A simple, low-cost process current converter has been shown with wide application in the controls industry. The design is tolerant of wide power supply variations, has high voltage compliance, and is easily calibrated. Reliability and cost are optimized by using only three integrated circuits, the Precision Monolithics DAC-08, REF-01, and OP-14, plus a few readily available discrete components.

REFERENCE

Crowley, B., "Circuit Converts Voltages to 4-20mA For Industrial Control Loops," **Electronic Design**, Jan. 5, 1976, page 116.

PARTS LIST

Circuit Symbol(s)	Description
A1	+10V Reference, PMI REF-01CJ
A2	8-Bit DAC, PMI DAC-08CQ
A3	Dual Op Amp, PMI OP-221
C1-C3	0.1μF +80%/−20% 50V, Type CK-104
C4	100pF ±5% Mica, DM100ED101J03
D1-D4	Power Diode, 1N4001
Q1	NPN Transistor, 2N3904
Q2	PNP Power Darlington, Motorola 2N6053
R1-R2	50kΩ Potentiometer, Bourns #3006P-1-503
R3	4020Ω ±1%, RN55C4021F
R4	20kΩ ±1#, RN55C2002F
R5	800Ω ±0.1%, GR#8E16D800
R6	100Ω ±0.1%, GR#8E16D100

PMI

AN-23

D/A CONVERTER GENERATES HYPERBOLIC FUNCTIONS

Precision Monolithics Inc.

APPLICATION NOTE 23

Measurement and control systems frequently require fine resolution around a setpoint with wide dynamic ranging capability. This can be satisfied by systems designs which use a high resolution, strictly linear approach; but this is costly and often unnecessary. Nonlinear function fitting using multiplying digital-to-analog converters (DAC's) offers a desirable alternative by being both simpler and more cost-effective. This application note describes how extended range hyperbolic functions of the type A/X or —A/X (where "A" indicates an analog constant, while "X" represents a decimally-expressed digital divisor) are easily generated by just two lowcost I.C.'s; an operational amplifier and a multiplying DAC. Circuit configurations are provided for each polarity output along with dynamic performance photographs and general design guidelines for either binary or BCD-coded divisors.

THEORY OF OPERATION (A/X)

Figure 1a shows the A/X function circuit which uses a two-digit BCD-coded DAC, the DAC-20EX, and a decompensated, wide-bandwidth op-amp, the OP-17. A constant current, I constant, equal to the value of one least significant bit (LSB), flows into the DAC output terminal, I_O. Simultaneous adjustment of the scale factor and output amplifier offset voltage is enabled by a multi-turn, low tempco potentiometer, R5, which adjusts current $-I_R$ producing voltage $-V_R$ across R2. The LSB value (scale factor) equals $-V_R/R1$.

Zener diode, D_Z, provides a stable reference voltage source. Because feedback for the op amp is through the DAC, capacitors C1 and C2 are added to provide proper phase compensation. Reference resistor R3 is determined by the scale factor and the maximum current allowed into the DAC reference input V_R+. Bias

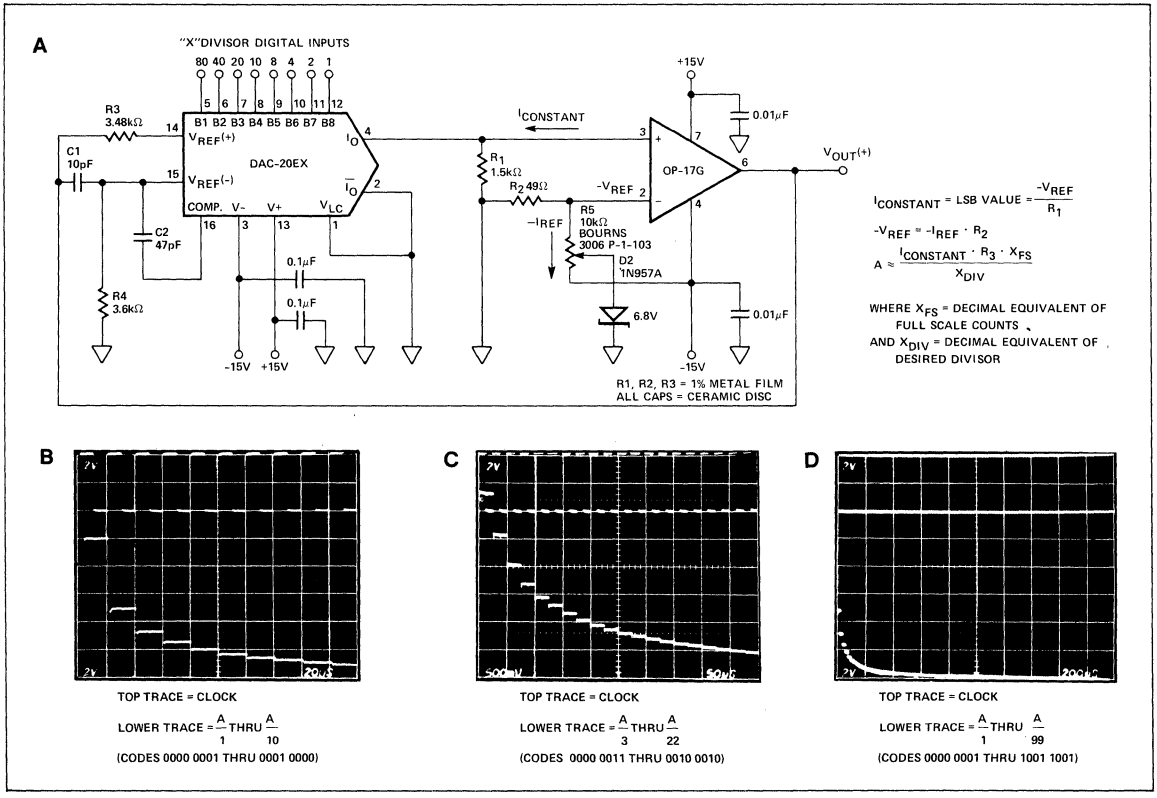


Figure 1. A/X Function Generator

current compensation for the DAC reference amplifier is accomplished by R4.

Figures 1b, 1c, and 1d show dynamic performance of circuit 1a when the digital inputs are swept by an external BCD up-counter with codes of 0000 0001 through 1001 1001 (division by zero is not allowed).

THEORY OF OPERATION (—A/X)

The circuit configuration for the —A/X function is shown in Figure 2a. It is quite similar to that of Figure 1a with both the DAC reference amplifier and output amplifier terminals reversed. Capacitors C1 and C2 provide phase compensation. Figures 2b, 2c, and 2d show dynamic performance of circuit 2a.

DESIGN CONSIDERATIONS

1. Circuit speed and settling time are dictated by output op amp slew rate, scale factor, and compensation. Use of slower amplifiers considerably increases the illustrated settling times. Effective slew rate of circuit 1a is 3V/μs, while circuit 2a slews 0.6V/μs.
2. Layout and breadboarding of high gain, wide-bandwidth devices necessitates considerable care with a ground plane with single point grounding being highly desirable. Decoupling capacitors located close to the devices' supply inputs are essential.
3. Accuracy of the circuit is within 1% over the 0°C to +70°C temperature range with 1% metal film resistors R1, R2 and R3. DAC linearity becomes an important factor as the divisor decreases; for this reason 1/4 LSB linear DACs are recommended.
4. Binary coding may be accomplished by substituting an 8-bit binary-coded DAC-08EX for the two-digit BCD-coded DAC-20EX. In addition to adjusting circuit values however, a higher performance op amp such as the OP-17F is desirable because the output amplifier's input offset voltage drift becomes a more significant error source for overall scale factor stability over temperature. This is due to the increased resolution of the binary coding.

AN-23

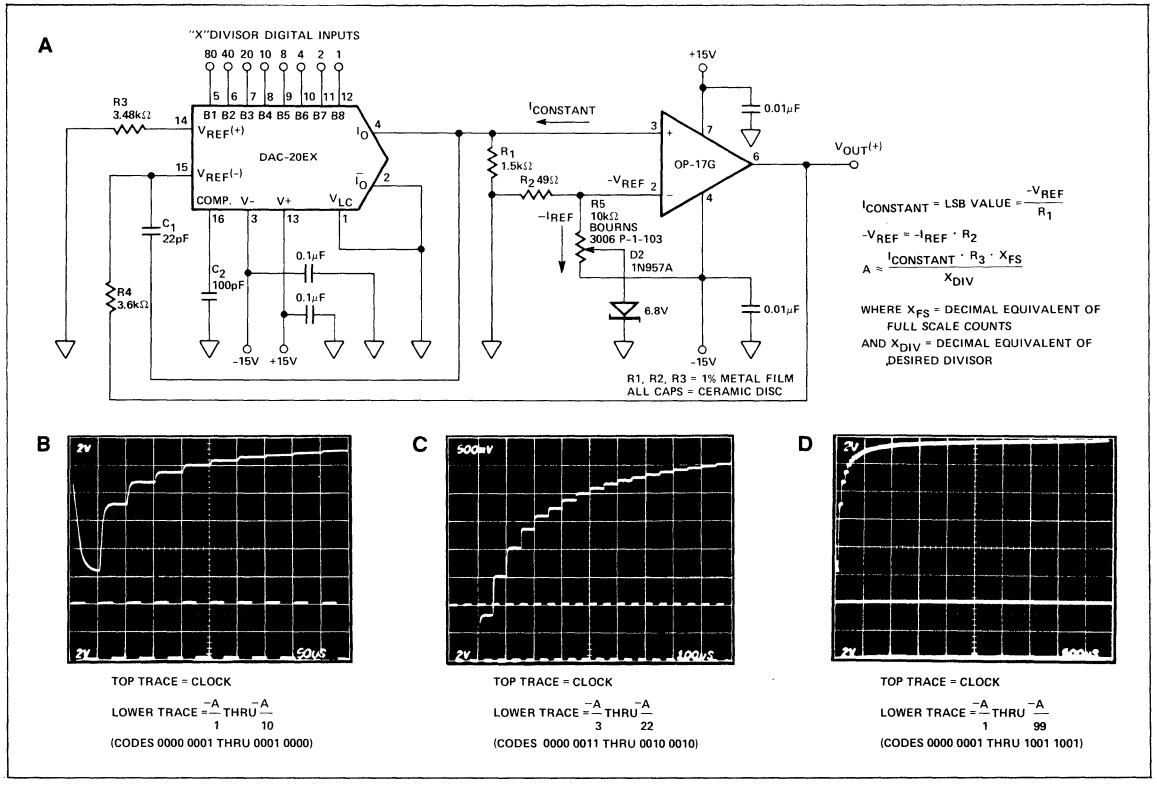


Figure 2. -A/X Function Generator

This application note shows how to make high speed, voltage output D/A converters using the DAC-08 and OP-15/16/17 precision FET-input op amps. Designs are optimized for highest speed (OP-17), lowest drift (OP-16) and for lowest power (OP-15). Although the DAC-08 is used as an example, the same configurations work with DAC-20 and DAC-86.

Converting the current output of a fast IC DAC to a voltage while maintaining fast settling time is difficult. The full scale current of the DAC-08 settles in 85ns. It can be terminated with a load resistance, as shown in Figure 1, to give a 10V output. However, in this configuration the settling time will be dominated by the RC time constant of R_1 and the DAC-08's output capacitance ($T = R_1C_O = 5k\Omega \times 15pF = 75ns$). It requires 6.2 time-constants to settle within 0.2% of full scale (1/2 least significant bit of an 8-bit converter). Therefore, the settling time is 500ns including the DAC-08's 35ns propagation delay.

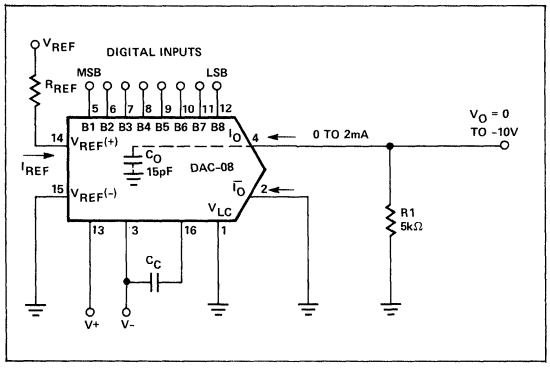


Figure 1. DAC-08 with Resistive Termination Settling Time = 500ns for 0 to -10V

Due to this RC time constant, current-to-voltage conversion is usually accomplished with a transimpedance amplifier as shown in Figure 2. The output's response is now limited by the amplifier's slew rate and settling time. However, an additional pole is introduced at $\frac{1}{2\pi R2C1}$, where C1 is the sum of the DAC's output capacitance and the op amp's input capacitance. The frequency of this pole is likely to be at an inopportune location for fast amplifiers, creating an underdamped response or even oscillation.

The circuit of Figure 3 resolves this problem. It can be shown that if R1C1 = R2C2, the effect of the two capacitors is

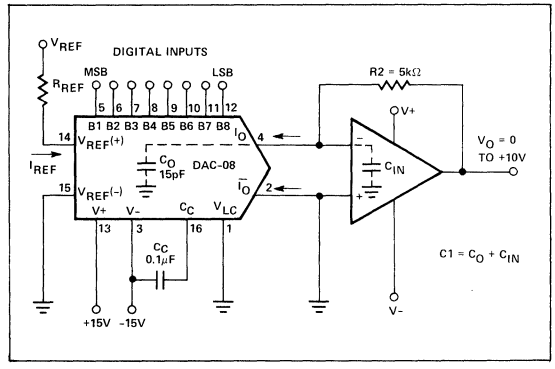


Figure 2. Voltage Output DAC with Transimpedance Amplifier

completely cancelled, and the overall settling will be determined by the amplifier's behavior only. In addition, C2 can be varied to fine tune the system's response and minimize settling time to compensate for the op amp's possibly underdamped or overdamped characteristics. The disadvantage of this circuit compared to that of Figure 2 is that all input errors, and in particular input offset voltage (V_{OS}), are amplified by the factor $\left(1+\frac{R2}{R1}\right)$.

The optimum speed is obtained — at low cost — by using the OP-17, fast, precision, JFET-input op amp, stable only at closed-loop gains of five or more. Therefore, the R2/R1 ratio

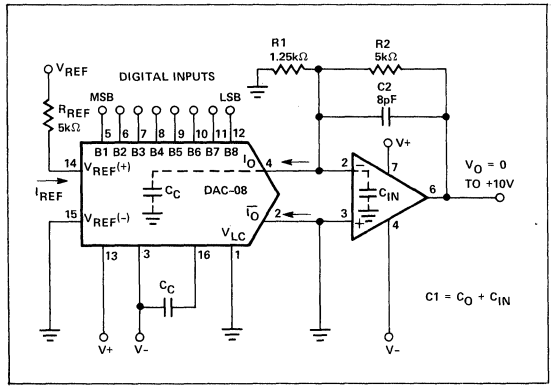


Figure 3. Voltage Output DAC with Response Shaping

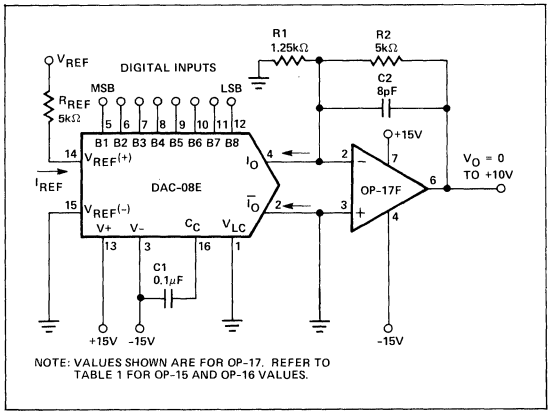


Figure 4. 0 to +10V Connection, Settling Time = 380ns

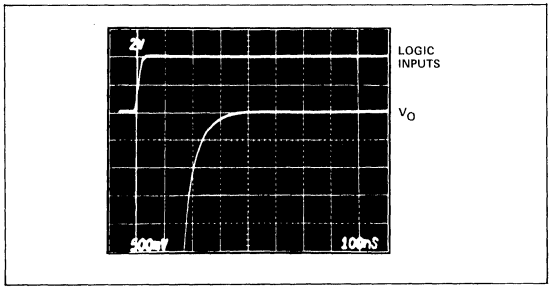


Figure 5. Settling Time of Figure 4 Circuit Using OP-17

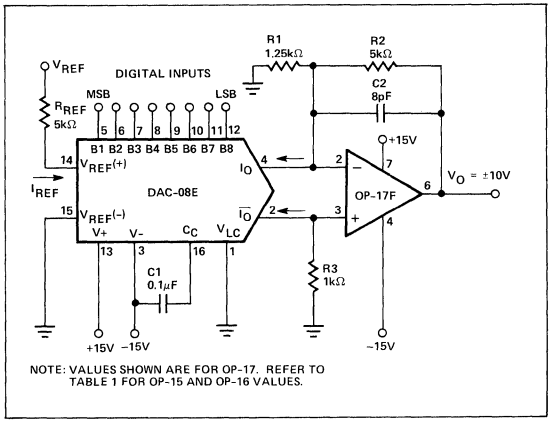


Figure 6. ±10V Connection, Settling Time = 450ns

is set at four (Figure 4). Settling time to 0.2% is 380ns with all bits turning ON (0 to 10V), or all bits turning OFF (10V to 0). The last 2.5 volts of the rising waveform are shown in the photograph of Figure 5. The three grades of the OP-17 are specified at V_{OS} = 0.5mV maximum (OP-17E), 1.0mV maximum (OP-17F), and 3.0mV maximum (OP-17G). Even though V_{OS} is multiplied five times its effect is still less than 0.2% or 20mV. The OP-17E's contribution will be only 1/4 LSB even on a 10-bit system. The offset voltage can also be trimmed to zero, then the TCV_{OS}, at 2 to 4μV/°C, typically, will be the limiting factor. The complementary output of the DAC-08 can be used for a -10V to +10V system as depicted in Figure 6. Settling time is only slightly increased because of the time required to slew the additional ten volts. Since 1/2 LSB is now 40mV, the non-slew portion is decreased by 70ns.

The OP-16 is slower than the OP-17 but it is stable in unity gain. Therefore, improved output-referred error can be traded off for increased settling time. The OP-15 is a lower power dissipation model, but again this improvement is obtained at the expense of settling time. Table 1 summarizes the resistor and capacitor values for the various amplifiers in the circuits of Figure 4 and Figure 6, the settling times obtained in these circuits, and the output-referred offset errors.

Table 1. OP-17/16/15 Performance as Output Op Amp for DAC-08

	OP-17		OP-16		OP-15	
	0 to 10V Figure 4	**-10 to +10V Figure 6**	**0 to 10V Figure 4**	**-10 to +10V Figure 6**	**0 to 10V Figure 4**	**-10 to +10V Figure 6**
R_1	1.25kΩ	1.25kΩ	10kΩ	10kΩ	10kΩ	10kΩ
R_2	5kΩ	5kΩ	5kΩ	5kΩ	5kΩ	5kΩ
R_3	—	1kΩ	—	3.3kΩ	—	3.3kΩ
C_2	8pF	8pF	25pF	40pF	30pF	50pF
Settling time to ±0.2%	380ns	450ns	750ns	1100ns	900ns	1350ns
Slew Time	150ns	290ns	400ns	800ns	590ns	1170ns
1/2 LSB = 0.2%	20mV	40mV	20mV	40mV	20mV	40mV
Closed Loop Gain	5	5	1.5	1.5	1.5	1.5
Offset Error at Output						
E Grade Maximum	2.5mV	2.5mV	0.75mV	0.75mV	0.75mV	0.75mV
F Grade Maximum	5.0mV	5.0mV	1.5mV	1.5mV	1.5mV	1.5mV
G Grade Maximum	15.0mV	15.0mV	4.5mV	4.5mV	4.5mV	4.5mV
Supply Current Maximum	7mA	7mA	7mA	7mA	4mA	4mA

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AN-25

APPLYING THE OP-06 OP AMP AS A HIGH PRECISION COMPARATOR

Precision Monolithics Inc.

APPLICATION NOTE 25

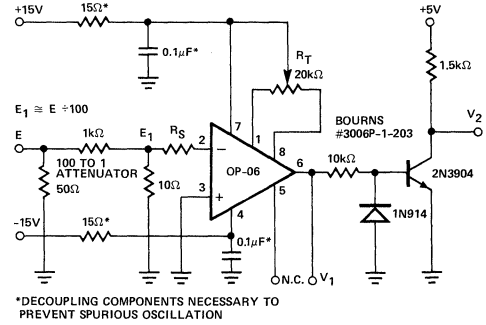
INTRODUCTION

The Precision Monolithics OP06 op amp makes an excellent comparator. In fact, for submillivolt signals, there is simply no comparator that performs as well. Using an external nulling potentiometer, the offset drift is typically 0.6μV/° C. With its high open loop gain of 1 million, only 30μV is required at the input to drive the output from one saturation level to the other. A 50° C change in temperature produces a 30μV change in V_{OS}; thus a *total* error band of 100μV *including temperature effects* is quite conservative. This performance is an order of magnitude better than other comparators. 100μV sensitivity is nice to have in 12-bit A/D converters, but it is essential in 14-bit converters. Where preamplifiers are typically needed with thermocouples and strain gauges, the OP06's sensitivity allows *direct* comparison of these low-level outputs. As a result system costs decrease, and reliability increases.

LOW-LEVEL PERFORMANCE MEASUREMENTS

The low-level capabilities of the OP06 comparator are graphically illustrated in Figures 1 and 2 using the test circuit below. Comparator voltage input, applied through a 100 to 1 attenuator, is 100μV_{p-p} in Figure 1 and 40μV_{p-p} in Figure 2. Note that the op amp output still reaches both positive and negative saturation.

TEST CIRCUIT



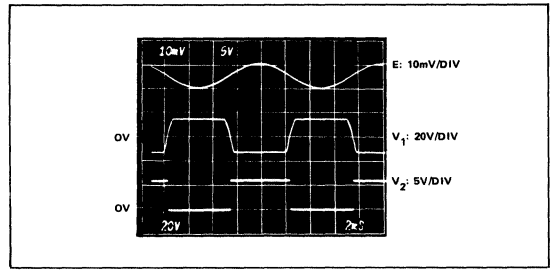


Figure 1. 100μV_{p-p} Sine Wave Response (R_S: 100Ω)

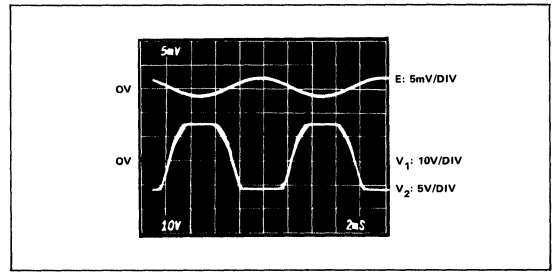


Figure 2. 40μV_{p-p} Sine Wave Response (R_S: 100Ω)

COMPARATOR RESPONSE TIME

While most comparators are specified for 2mV to 5mV overdrive, the OP06 operates very reliably with only 0.5mV overdrive. Figures 3 and 4 show the response times for both positive going and negative going inputs with 500μV and 5mV overdrives as measured at the logic output.

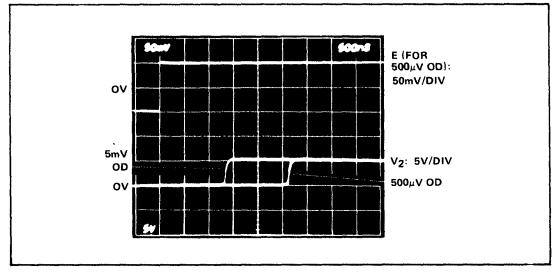


Figure 3. Positive Going Response Time (5mV and 500μV Overdrives)

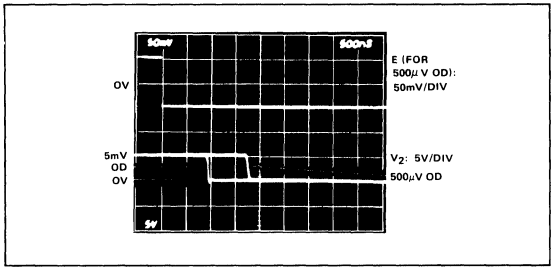


Figure 4. Negative Going Response Time (5mV and 500μV Overdrives)

OP AMP RESPONSE TIME

Primarily, the very high open loop gain (A_{VO}) of the OP06 — over one million — is responsible for its success as a comparator. The DC gain, as specified on op amp data sheets, is important for comparison sensitivity (V_{DET}). However, it is the shape of the gain curve with frequency that dictates how fast the op amp will switch as it passes through its linear region. When operated as a comparator the OP06 spends most of its time in either positive or negative saturation (see Figures 5 and 6). Saturation effects are discussed later; but for now notice the difference in slew rates for the overdrive levels.

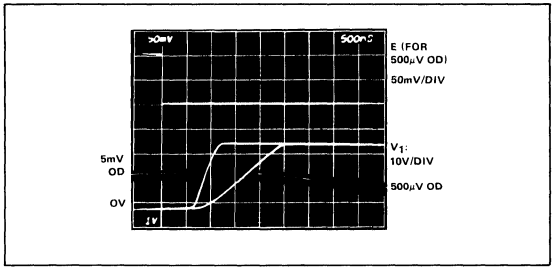


Figure 5. Positive Going Op Amp Response Time vs Overdrive

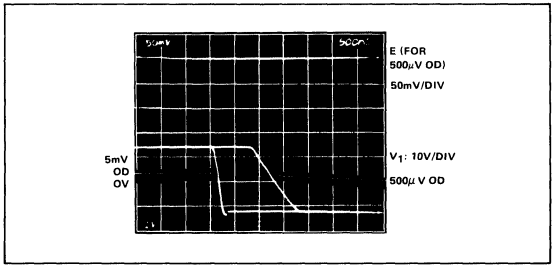


Figure 6. Negative Going Op Amp Response Time vs Overdrive

OP06 DYNAMIC PERFORMANCE CHARACTERISTICS

There is another factor which has a significant effect on slew rates — the way in which the AC gain is rolled off versus frequency. If we refer to Figure 7 we see gain compensation curves for closed loop gains from 1 to 10,000. Figure 8 relates the slew rate to these frequency response curves. These curves point out one of the tradeoffs between good op amp performance and good comparator performance. For example, if an OP06 has a gain compensation for $A_V = 10$, then its slew rate would be 0.08V/μs. This would result in a rise time (20 volt swing) of 250μs. The fact that a designer needs no compensation with the OP06 — when operated as a comparator — allows the rise times observed in Figures 5 and 6.

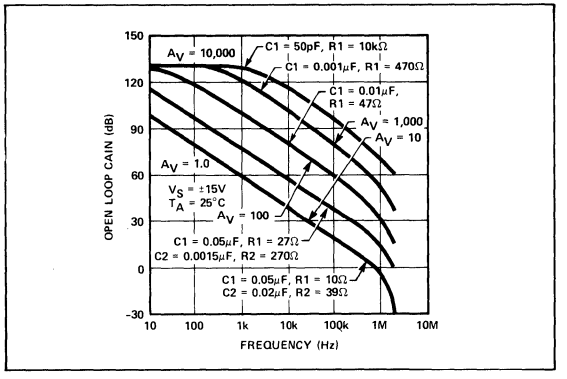


Figure 7. Open Loop Response for Values of Compensation

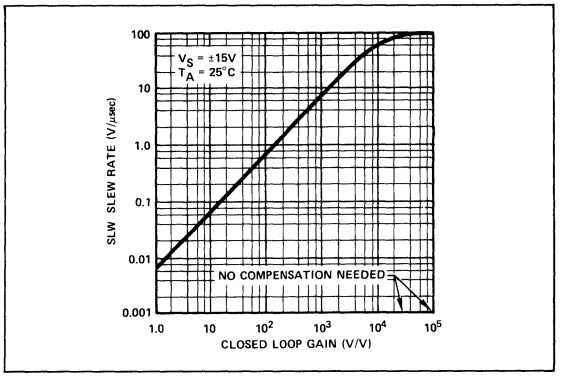


Figure 8. Slew Rate Using Recommended Compensation Networks

COMPARATOR, OP AMP SIMILARITIES

In an op amp, the offset voltage is that voltage which must be applied to the input to drive the output to zero volts. In a comparator this definition is modified to a *specified voltage range* at the output. In ths way the required voltage "window" includes the normal offset voltage of op amps and the signal voltage needed to move the output by some ΔV. Since most

op amps operate in ±15 volt systems, an output voltage range of ±15 volts (or a ΔV of 30 volts) has been chosen. Using this range assures saturation at both the positive and negative extremes (−14 volts and +12 volts for the OP06). Low offset voltage and high gain combine to produce the comparator "detector window."

OTHER FACTORS AFFECTING SPEED

To gain further insight into the relation between overdrive and the various switching times, the graph in Figure 9 was generated from measurements on the OP06 "comparator." To further characterize the OP06 performance, delay times were measured versus source resistance (R_S) with a fixed 5mV overdrive. This curve is shown in Figure 10. Since the rise and fall times were essentially constant with R_S variations, they were not plotted. The delay times are the main contributors to total comparator response time. Since the OP06 was not designed as a comparator, individual gain stages will go into saturation when the output voltage is driven to one of its limits. One of the differences between designing op amps and comparators is the addition of clamp diodes to prevent the above mentioned saturation.

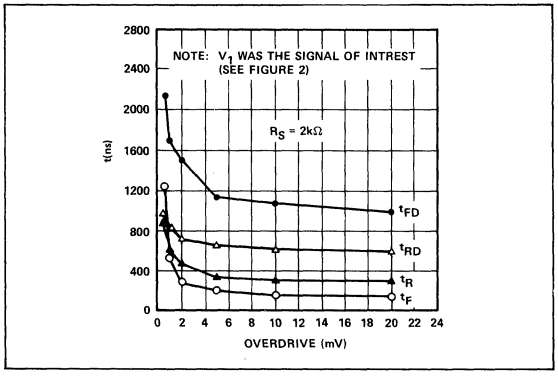


Figure 9. Rise, Fall and Delay Times vs Overdrive Signal

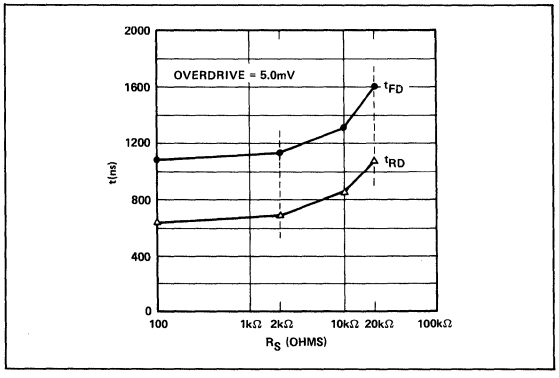


Figure 10. Delay Times vs Source Resistance (R_S)

NOISE AND POWER SUPPLY REJECTION

When dealing with sub-millivolt signals, noise referred to the comparator input becomes an important factor. Basically, the noise comes from two sources:

1) Normal input noise of an op amp;

2) Noise induced by power supply ripple.

Figure 11 shows the wideband noise-on an RMS basis-vs. system bandwidth. What is more important is the RMS to peak conversion factor. Table I shows the crest factors for gaussian noise. Note in particular that the crest factor is less than four 99.99% of the time, and less than five 99.9999% of the time. Thus the RMS noise is 1μV for 10kHz bandwidth and this yields a "worst case" of 5μV peak or 10μV peak-to-peak.

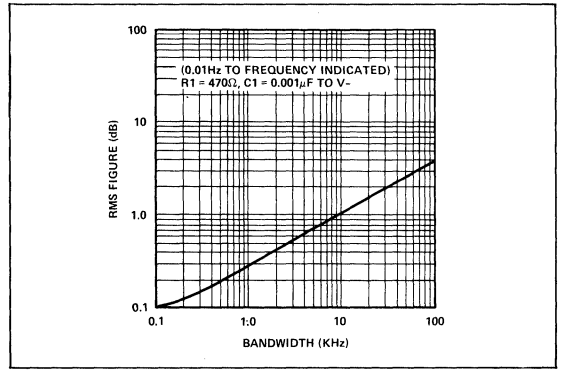


Figure 11. Input Wideband Noise vs Bandwidth

Table 1. Crest Factors for Gaussian Noise (1)

% OF TIME PEAK IS EXCEEDED	PEAK RMS	PEAK FACTOR IN dB = 20 $\log_{10}$ PEAK RMS
10.0	1.645	4.32
1.0	2.576	8.22
0.1	3.291	10.35
0.01	3.890	11.80
0.001	4.417	12.90
0.0001	4.892	13.79

The other source of noise comes from the power supplies. Looking at Figure 12 note that the power supply rejection ratio (PSRR) is 115dB (1.8μV/V) out to 300Hz. For example a power supply which had 1 volt (peak-to-peak) ripple would only produce 1.8μV peak-to-peak "noise." Thus it becomes obvious that the total noise performance of the OP06 is indeed outstanding.

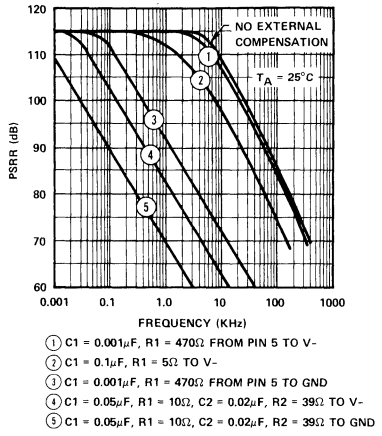


Figure 12. PSRR vs Frequency

CONCLUSION

The combination of ±30V input overvoltage protection, gain of 1 million, low noise, low drift and external compensation allow operation of the OP06 op amp as a low-level comparator. Low-level performance is unsurpassed by any presently available comparator.

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Four ICs are used in this design to give positive or negative peak detection and reset levels over a ±10V range. A precision voltage comparator, a sample-and-hold amplifier, an open-collector exclusive-OR gate package, and a quad analog switch used as two SPDT switches are the principal components required.

BLOCK DIAGRAM

Figure 1 shows the basic circuit and the 4 modes of operation. A comparator continuously examines the difference between the present analog input voltage and a voltage peak held by the sample and hold (S/H) amplifier. If the present value exceeds the held value, the S/H is placed in the "Track" condition and acquires a new peak value returning to a "Hold" condition when coincidence is reached. The comparator's output is inverted or non-inverted depending on the polarity selected by POS/$\overline{\text{NEG}}$ SELECT. This same TTL control signal connects the appropriate voltage-programmed reset voltage to the S/H input during the RESET modes. In RESET the S/H is forced to a "Track" condition by the PEAK DETECT/$\overline{\text{RESET SELECT}}$ digital input. Figure 2 shows typical waveforms.

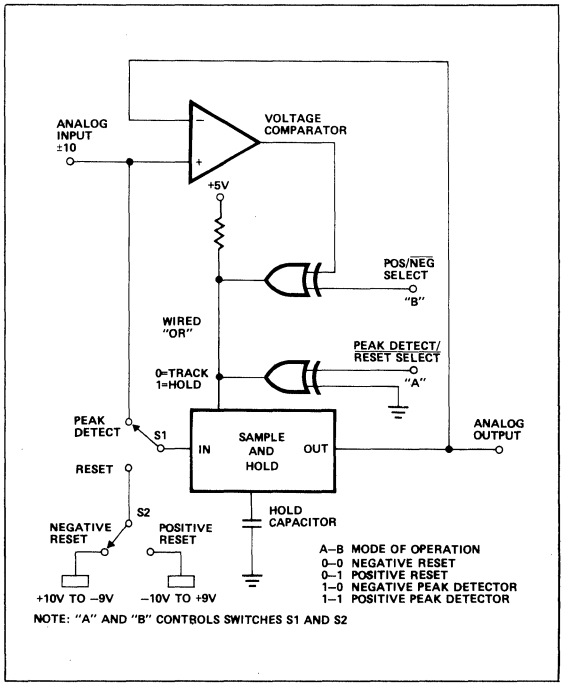

Figure 1. Programmable Peak Detector Block Diagram

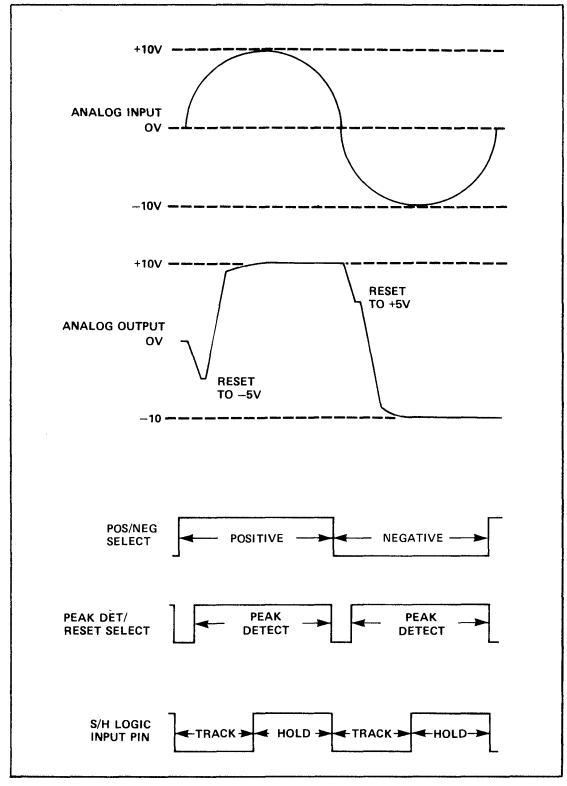

Figure 2. Programmable Peak Detector Waveforms

DETAILED CIRCUIT DESCRIPTION

In Figure 3, the SMP-11FY S/H is specified for three reasons: low cost, 2.5mV (Maximum) zero-scale error, and its 10V/μs slew rate. Together with the CMP-01CJ precision voltage comparator, system unadjusted DC accuracy is within 5mV at zero-scale and 10mV at full-scale. Comparator input overvoltage protection resistors and diodes are required as shown.

A SW-01 Quad Analog Switch connected at 2 SPDT switches connects the proper analog inputs to the S/H during the 4 modes of operation. 200 ohm current-limiting resistors are used as recommended by the switch manufacturer. Logic drive to the switch is provided by 1/2 of a SN74LS136 quad exclusive-OR gate used as 2 inverters.

Bypassing as shown is strongly recommended — 0.1μF ceramic dieletric capacitors for the comparator and the S/H, plus 10μF solid tantalum bypass capacitors physically close to the S/H. In addition the use of a ground plane is recommended to minimize ground path resistances. A 0.01μF hold capacitor is used to minimize overshoot when tracking high frequency analog inputs.

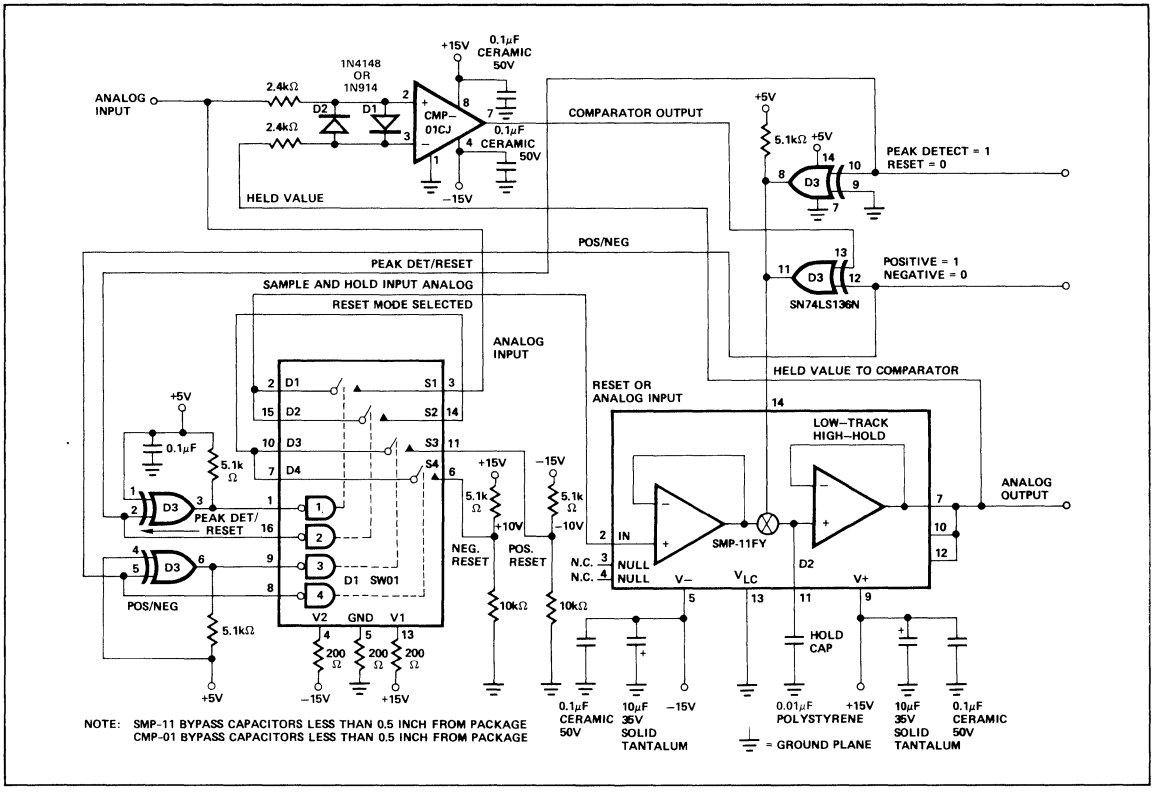

Figure 3. Programmable Peak Detector Complete Schematic

PMI

AN-28

AUDIO APPLICATIONS FOR THE DAC-86 COMPANDING D/A CONVERTER

Precision Monolithics Inc.

APPLICATION NOTE 28

The DAC-86*, with its 12-bit linear equivalent dynamic range capability in a 7-bit + sign format, has opened up new applications possibilities in data conversion and related areas of signal processing. Like multiplying D/A predecessors as the DAC-08, it has logic programmability, wide linear range reference operation, wide voltage compliance, and true current source outputs. In addition it has sign control and multiplex output options.

These features, combined with the exponential coding, make the DAC-86 a very useful design block for audio systems, where decibel weighted scaling is often the rule. Such applications are generally characterized by accuracy relative to reading, rather than full scale, and it is for such uses that the DAC-86 is intended.

This application note discusses the multiplying and control characteristics of the DAC-86 with regard to AC inputs in some detail, as an aid to optimization of high performance digitally-controlled gain circuits. These and other different types of audio circuits are illustrated, with wide ranges of applicability. Not discussed in this note are basic details of DAC-86 operation; for these, the data sheet may be consulted.

DAC-86 REFERENCE MODULATION CONSIDERATIONS

For use as a multiplying D/A converter with a modulated (AC) reference, the DAC-86 is an attractive device for two basic reasons — its wide control dynamic range capability, and the fidelity of the reference channel in audio performance terms. The device is capable of either 72 or 78dB control ranges with quasi-exponential coding (dB scaled), and noise and distortion components are on the order of 0.01% of full scale.

Modulation of the reference channel can be accomplished in either of two basic ways, shown in Figures 1 and 2. Method (a) is a low input impedance method, with an input impedance equal to R_{IN}; to scale I_{IN} to a value less than V_{REF}/R_{REF}, the DC current in R_{REF}. Method (b) is a high impedance connection, analogous to an op amp voltage follower. This mode has less inherent freedom of operation, because of the lack of independence between AC and DC current inputs and the practical common mode restrictions of the reference inputs. Basic design equations for both methods are shown. Method (a) is fairly straightforward, but method (b) requires some comment.

For small AC voltage inputs using method (b), it may not be possible to achieve high percentages of reference modulation with a single resistor, such as R_{REF}. For such cases an additional resistor (R_X) can be used, chosen for the desired equivalent impedance at the (+) input. The AC term of I_{REF} will be equal to V_{IN} divided by the parallel resistance of R_{REF} and R_X.

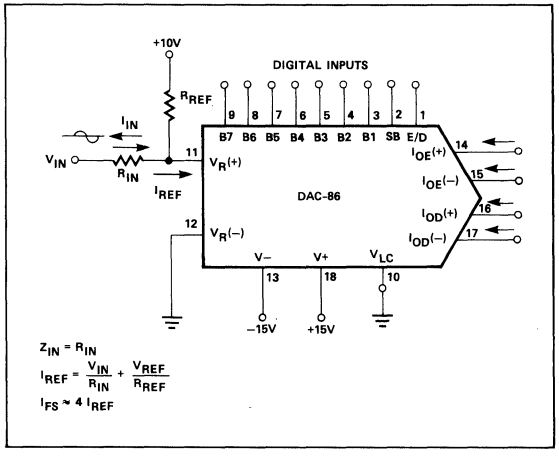

Figure 1. Low Input Impedance Connection

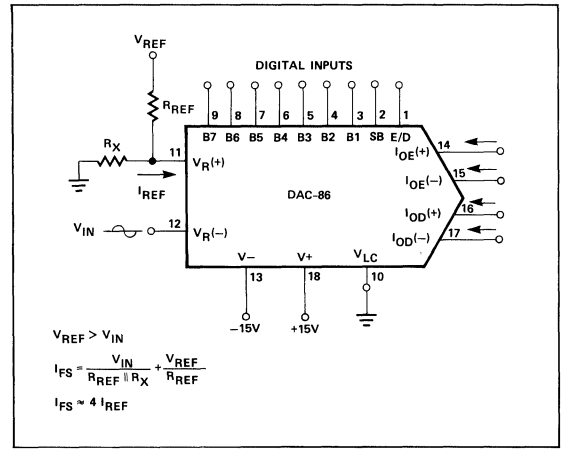

Figure 2. High Input Impedance Connection

*Manufactured under one or more of the following U.S. patents: 4055773, 4056740, 4088905.

MULTIPLYING PERFORMANCE AND DISTORTION

While the DAC-86's reference channel performance is generally quite good, it can vary, dependent upon the percent of modulation, the method used, and relative impedances. Typical data is shown in Figure 4, which was taken in the test circuit of Figure 3.

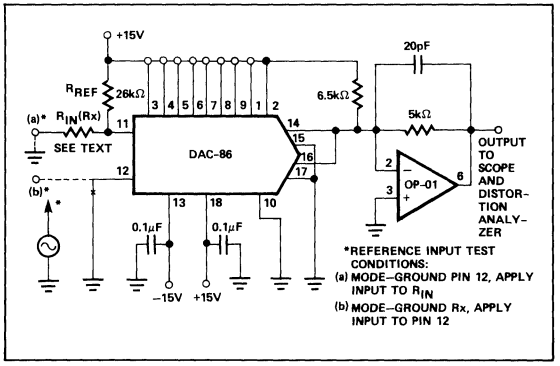

Figure 3. Reference Linearity Test Circuit

Figure 3 is a test circuit which operates the DAC-86 at a full scale current output of 2.5mA (fixed for test purposes), into a current-to-voltage converter using a high slew rate op amp, the OP-01. This minimizes error contributions due to DAC-86 output compliance and linearity at voltage dynamic range extremes. The method of reference modulation can be varied between (a) and (b) for modulator levels to more than 85% of I_{REF}'s DC level. The results are shown in Figure 4.

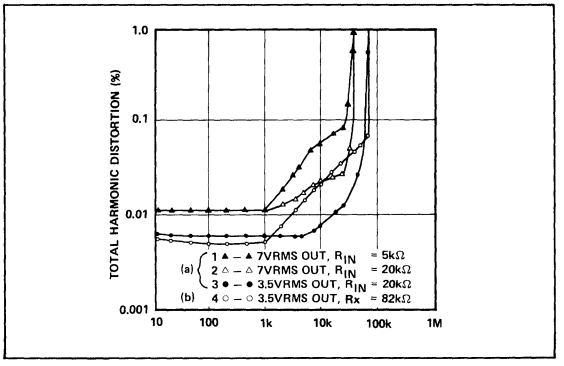

Figure 4. Total Harmonic Distortion vs Frequency

Curve numbers 1, 2 and 3 are for method (a) with 7VRMS output level and two different R_{IN} values. For these two curves, it can be noted in the region of 1 to 20kHz the 20kΩ R_{IN} value gives better performance because of the higher loop gain it permits in the reference channel op amp. For both of these conditions, slew limiting of the DAC-86 is reached at 30kHz. Curve 3 shows data for the (a) method, but using a 20kΩ R_{IN} and an output level of 3.5V. Slew limiting is pushed out to 60kHz, and below 15kHz THD is 0.01% or less. This curve represents close to full realization of DAC-86 performance potential.

Curve 4 shows performance for method (b) with a 3.5VRMS input, and output level THD is higher than method (a) for comparable level conditions because of reference channel common mode nonlinearities. Maximum input level for method (b) and the conditions shown is ±5V (3.5VRMS).

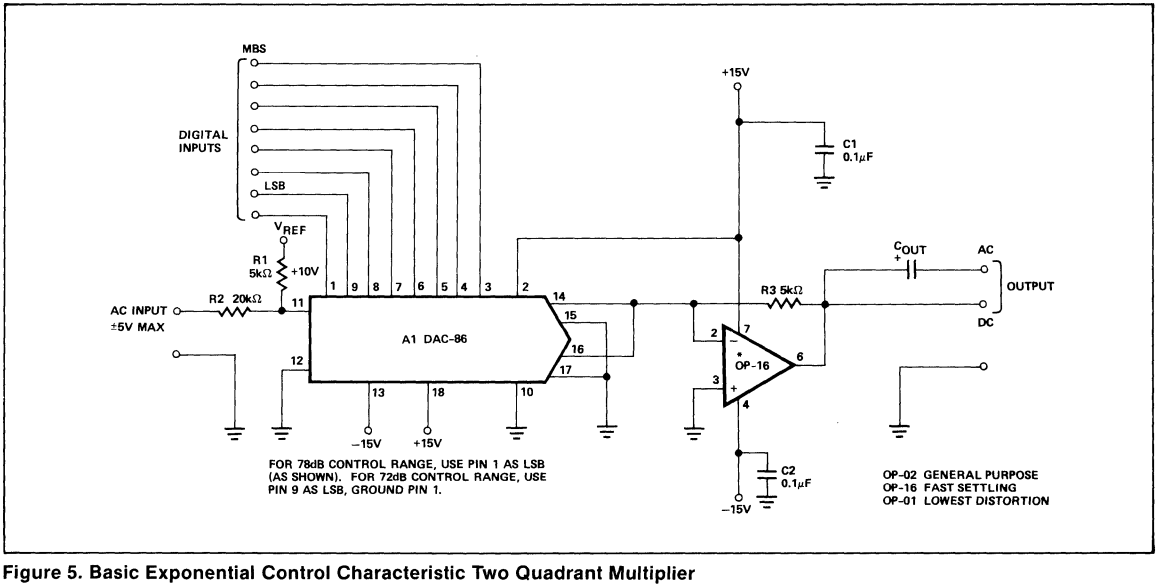

Figure 5. Basic Exponential Control Characteristic Two Quadrant Multiplier

From the above, it can be seen that reference modulation method (a) is preferred from a linearity standpoint, and linearity can generally be optimized by maintaining R_{IN} (or R_X) high in value, and also by using low percentages of modulation, where possible. Output modulation levels and signal frequencies should be used such that slew limiting is avoided in both the DAC-86 and subsequent amplifier as slew induced distortion (SID) can be troublesome in audio circuits (2, 3). The DAC-86's typical reference current slew rate is 0.25mA/μs; this is equivalent to 1.25V/μs when operating into a 5kΩ load.

DAC-86 GAIN CONTROL CIRCUITS

As an audio gain control, the DAC-86 is highly advantageous, because its audio signal level control is an exponential, or decibel weighted control law characteristic. Such a performance characteristic matches the natural human ear loudness sensitivity and provides greater useful dynamic range from a given device, as opposed to more common linear control scaling. The DAC-86's exponential coding and two quadrant multiplying capability allow it to perform the audio control level function with a control law accuracy of 1dB or less, over a 50dB or more gain range, with a total control span of 72 or 78dB, and a nominal 0.3 to 0.15dB/step gain resolution. The 8-bit word control input is readily interfaced with standard TTL compatible microprocessor buss systems; thus the device is a natural interface control element.

Figure 5 shows a DAC-86 gain control circuit to illustrate the basic operation. In this circuit reference modulation method (a) is used, and the input is scaled for a +5V max level by R2. Reference current is 270μA, as determined by R1 and the reference voltage. Full scale (DC) output current for the circuit is 1mA; thus R3 is chosen to bias A2's output to +5V. Signal output swing is $\pm$5V maximum, for full (all 1's) gain. The circuit can be used for either 78 or 72dB range control. By use of the E/D input pin as the LSB, it achieves a 78dB control range with 8 bits of control. With the E/D pin grounded range is 72dB with 7 control bits.

Figures 6 and 7 illustrate the control characteristic of the DAC-86 for these two modes of operation. This data shows the relative step differences in dB over the range of control which each form of the circuit possesses. Figure 6 shows the entire characteristic of the decode output (72dB range) circuit. As can be noted, over the first 50dB of range the change is close to 0.3dB/step, varying within each chord and more gradually from chord to chord. Note that the step size is maintained quite low up to chord 0, or over about 50dB of range. Because of the greater dynamic range implicit to the decode/encode mode of use (78dB) only the salient portions of this characteristic are shown in Figure 7. Each chord has 16 steps which encompass 6dB of range with a lower nominal resolution, 0.15dB/step. As can be noted from chords 7 and 6, the general error pattern is similar, but more gradual. The 1dB step limit for this circuit does not occur until chord 0 at a level corresponding to 59dB of control range.

Either of these basic operating options can be attractive for a control, as well as many other uses, because of the high dynamic range with relatively low control resolution.

An inherent disadvantage of the circuit of Figure 5 is the fact that the desired AC output rides atop a DC level, which varies with code changes. Although the static DC can be blocked with a coupling capacitor such as C_O, large and/or rapid gain changes will produce annoying output transients, which can be as high as 1/2 full scale. Generally, such a behavior is not tolerable in an active audio channel for quality use, so a means of suppression is described next: "Clickless" Attenuator/Amplifier (5).

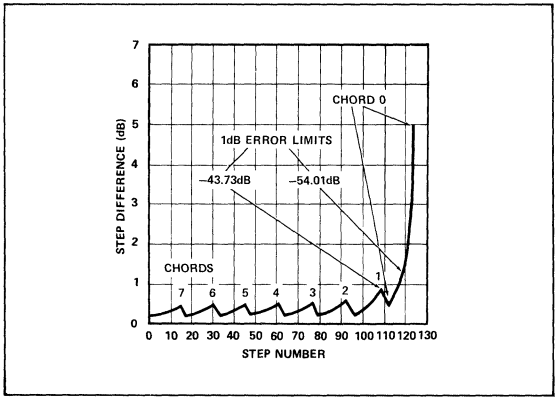

Figure 6. DAC-86 Decode Output Attenuation Characteristics Step Difference (dB) vs Relative Step Number

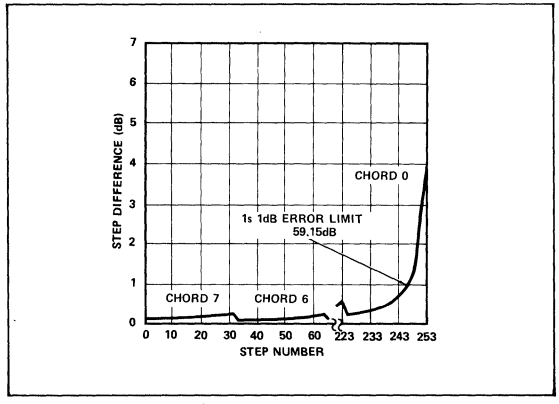

Figure 7. DAC-86 Decode/Encode Output Attenuation Characteristics Step Difference (dB) vs Relative Step Number

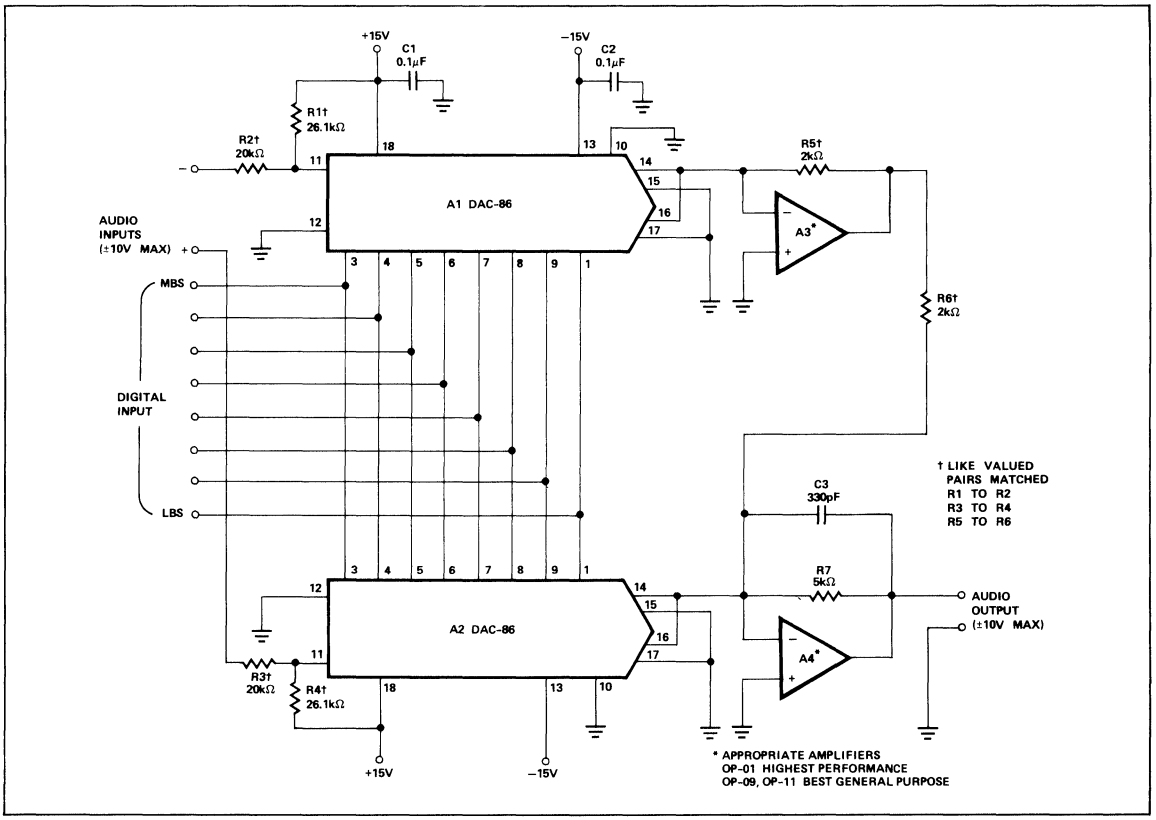

Figure 8. "Clickless" Attenuator/Amplifier

"CLICKLESS" ATTENUATOR

The "Clickless" attenuator circuit of Figure 8 is optimized for the audio level control function, as it features transient-free gain-change operation. This circuit utilizes two DAC-86s operating differentially, to minimize the gain change transient. Consequently it may be completely DC-coupled from input to output with differential signal inputs as well.

Signal handling capability is up to ±10V at either input and output, and distortion is quite low, generally 0.02% or less over much of the audio range, and independent of programmed gain state. S/N is 80dB or better, referred to 1V out. Overall performance is to some extent governed by the output op amp used, and the indicated types are suggested for cost/performance optimization. Lowest high level, high frequency distortion and minimum SID effects will be realized with high slew rate devices (5V/μs or more), such as the feedforward type OP-01 (2,3,4). For lower ouput levels, lower slew rate devices such as the OP-09 and OP-11 types can be used, with packaging advantages. The signal inputs may be used either singly or differentially, as may be desired. Distortion is comparably low through either input, as is demonstrated by Figure 9. This graph, a curve of 1kHz THD versus output level, is also an indicator of noise performance. Below 1V, performance is largely limited by noise and an S/N ratio of better than 80dB is implied by this data. Small signal bandwidth of the circuit can be adjusted by means of C3; for the value shown bandwidth is approximately 100kHz.

With circuit values as shown in the figure, the maximum (all 1's) gain is unity (0dB) from either input to the output, while

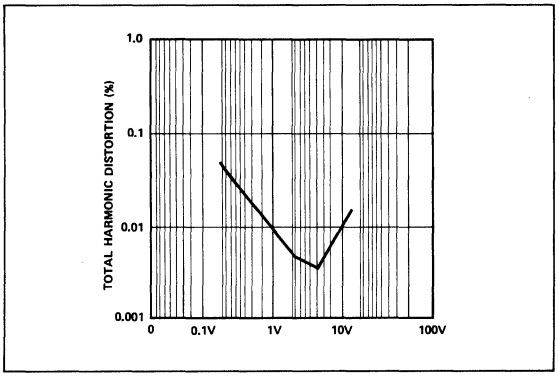

Figure 9. DAC-86 "Clickless" Attenuator 1kHz THD vs Output Level (All 1's) Unity Gain

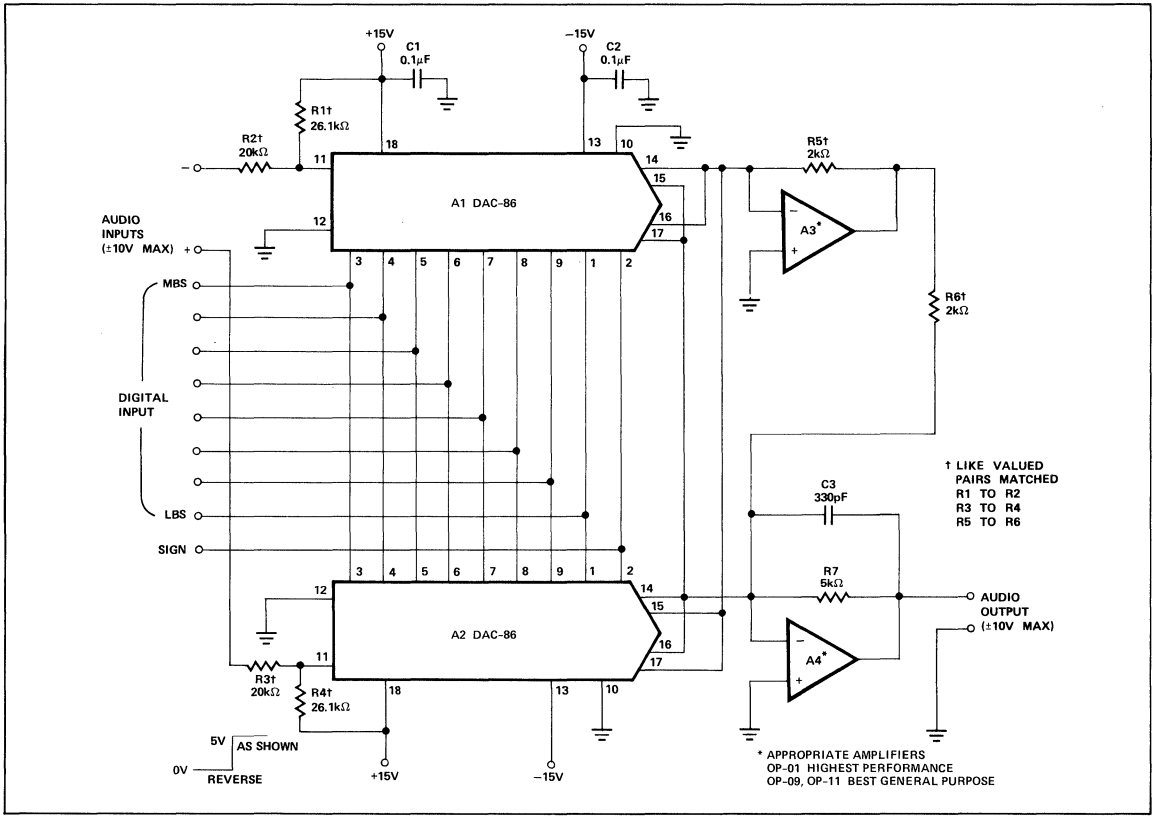

Figure 10. Sign + 3 Magnitude "Clickless" Attenuator/Amplifier

differential input to output gain is +6dB. Overall gain may be scaled by adjustment of R7, if necessary, yielding maximum gains either above or less than unity. Although a 78dB control range configuration is shown, the circuit may also be operated for a 72dB range, as shown in Figure 5. For best results the indicated pairs of resistors should be matched.

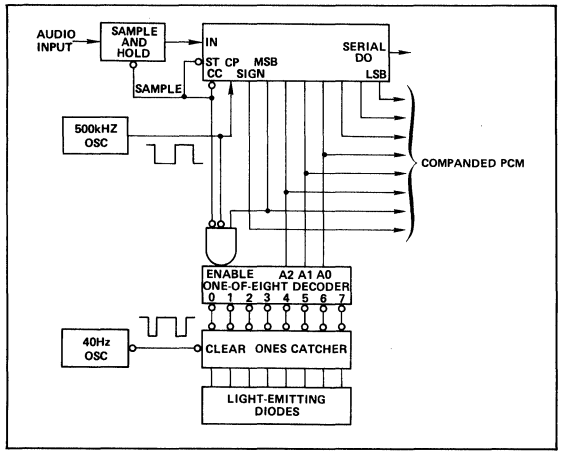

Figure 11. Peak-Reading VU Indicator Block Diagram

SIGN + MAGNITUDE "CLICKLESS" ATTENUATOR/AMPLIFIER

Not only is the circuit of Figure 8 highly useful in its basic form, it can also be easily adapted into other useful variations. One of these, a sign + magnitude clickless attenuator, is shown in Figure 10.

This circuit is essentially the same as Figure 8, except that the previously unused $I_{OE}(-)$ and $I_{OD}(-)$ outputs are lifted from ground, and cross connected to the opposite summing amplifier. With the sign input high, the circuit operates like Figure 8; with the sign input low the output phase is reversed. The circuit is useful as a programmed rectifier or absolute value amplifier with exponential gain control.

PEAK READING VU INDICATOR (6)

A very interesting audio application where the DAC-86's exponential coding is used to good advantage is a peak reading LED VU indicator, with logarithmic weighting. With the DAC-86's exponential coding, this allows log "thermometer" type lamp displays to be easily and accurately implemented. The block diagram of the system is shown in Figure

11, and the detailed schematic in Figure 12. Input audio is converted by the DAC-86, CMP-01 and 2502 SA A/D, after being sampled by the sample and hold. The A/D is clocked at a 500kHz rate, and completes a conversion every 18μs, sufficiently fast to track audio range signals.

The converted data appearing at the SAR outputs is in log form, since the DAC-86 has an exponential characteristic, and is within a feedback path. The four most significant magnitude bits drive a 1 of 8 decoder, which is enabled by the MSB. The resulting 8 classified levels are separated by 3dB increments, and drive an 8-bit R-S latch. This latch is updated every 25ms by the 40Hz display multiplex clock. Table 1

Table 1. Display Levels

INDICATION	INPUT VOLTAGE RANGE (RMS)
+3dB	$2.7 < V_{IN}$
0dB	$1.8 < V_{IN} \leq 2.7$
−3dB	$1.4 < V_{IN} \leq 1.8$
−6dB	$0.9 < V_{IN} \leq 1.4$
−9dB	$0.\overline{7} < V_{IN} \leq 0.9$
−12dB	$0.4 < V_{IN} \leq 0.7$
−15dB	$0.3 < V_{IN} \leq 0.4$
−18dB	$0.2 < V_{IN} \leq 0.3$
NONE	$0 \leq V_{IN} \leq 0.2$

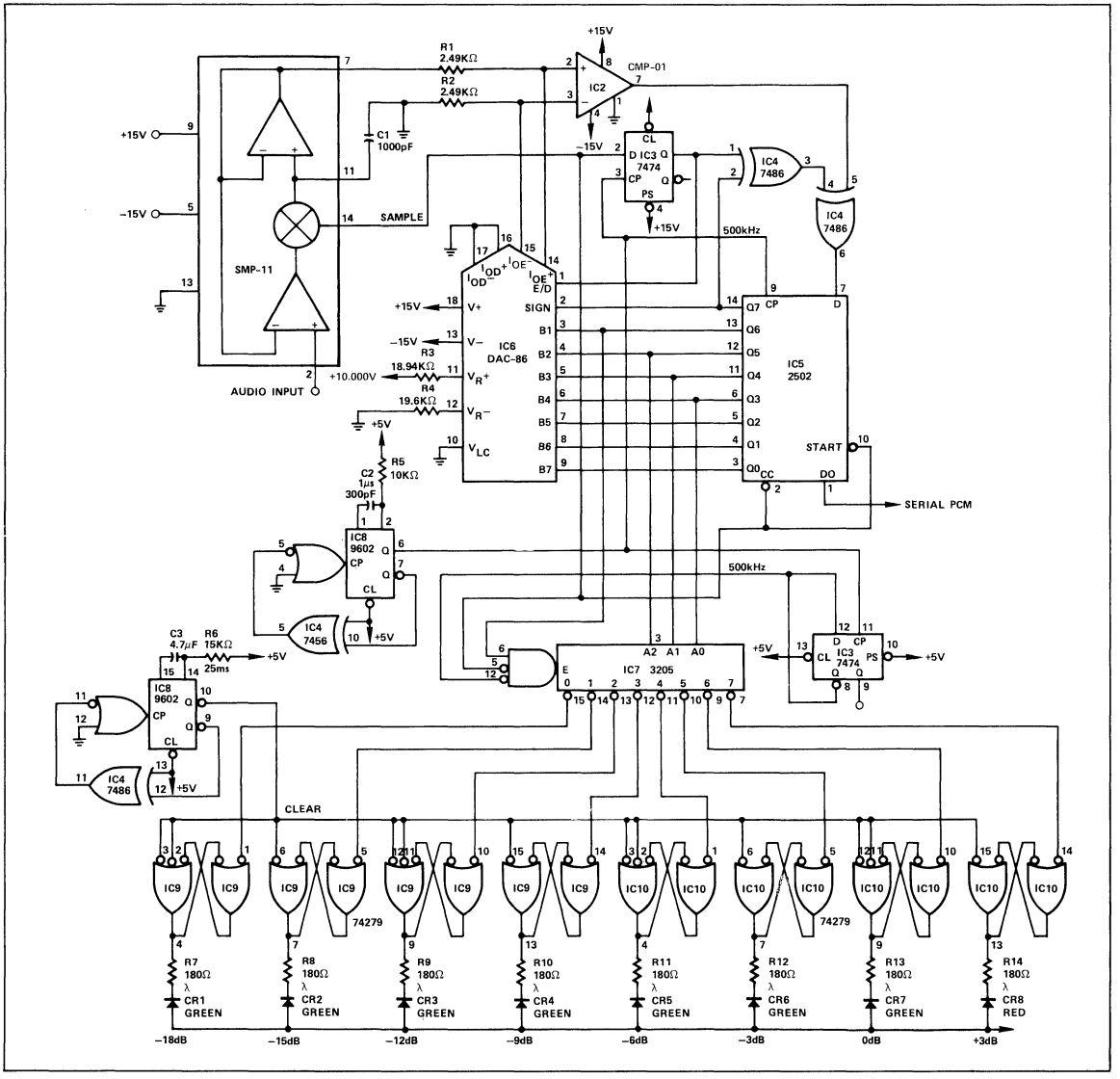

Figure 12. Peak-Reading VU Indicator Complete Schematic

summarizes the input levels associated with the respective dB levels. As can noted, 0dB corresponds to $2.15V_{RMS}$. These levels can be scaled upward or downward if desired, by configuring the S/H for gain, or by adding an input attenuator. Greater range, resolution, and more display levels can be realized by adding additional decode logic. Since the DAC-86's resolution and accuracy for the upper portion of the dynamic range is a fraction of a dB (see Figure 6), the possibilities for expansion are considerable.

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AN-31

SUCCESSIVE APPROXIMATION REGISTER DESIGN FOR MULTI-CHANNEL CODECs

Precision Monolithics Inc.

APPLICATION NOTE 31

INTRODUCTION

This Application Note describes a low cost, high speed Successive Approximation Register (SAR) design for use with 24-channel or 32-channel encoders. It is implemented with standard MSI functions which are available in several processes: T^2L, Low Power Schottky, CMOS, etc. The system is optimized for use with PMI COMDAC® DAC-86/89 D/A converter in conjunction with the CMP-01 precision voltage comparator and REF-01 voltage reference. This design offers a low-cost alternative to the 2502 LSI SAR by sharing a common system timing circuit over all the encoders (usually 2 or 3) used in a 24 or 32 channel system.

First, the traditional encoding procedure using the 2502 LSI SAR is explained. Next, the improved method described here will be discussed and compared with the 2502 method.

TRADITIONAL ENCODING METHOD

An encoding sequence begins with the sign bit comparison and decision. During this time the comparator is a polarity detector only. The Encode/Decode (E/D) input is held at a logic "0". Therefore, no current flows into the encode outputs, and the comparator is effectively disconnected from the DAC. Once the input polarity has been determined, the E/D input is changed to a logic "1", allowing current to flow into $I_{OE}(+)$ or $I_{OE}(-)$ depending upon the sign bit answer.

For positive inputs, current flows into $I_{OE}(+)$ through R_1, and the comparator's output will be entered as the answer for each successive decision. For negative inputs current flows into $I_{OE}(-)$ through R_2, developing a negative voltage which is compared with the analog input. An exclusive-OR gate inverts the comparator output during negative trials to maintain the proper logic coding, all ones for full scale and all zeros for zero scale. However, the exclusive-OR gate must not invert the signal during the sign bit decision, hence the need for the second exclusive-OR gate and the additional D flip flop in the 2502 LSI SAR encoder.

The successive removal technique requires the first decision to be made at the code 01111111, sequentially turning off all bits until all decisions have been made.

Traditional encoding systems begin the encode cycle by setting the binary input at 01111111. This is because LSI SARs are not designed to accommodate a DAC that is implemented in a sign-magnitude configuration.

IMPROVED ENCODING METHOD

For the sign-magnitude configuration such as the COMDAC® DAC-86/89 system, the initial setting of 10111111 performed by the SAR described here allows the DAC to settle for one additional clock cycle and requires no logic circuitry to prevent the exclusive-OR gate from inverting during the sign bit trial. The theory of operation follows.

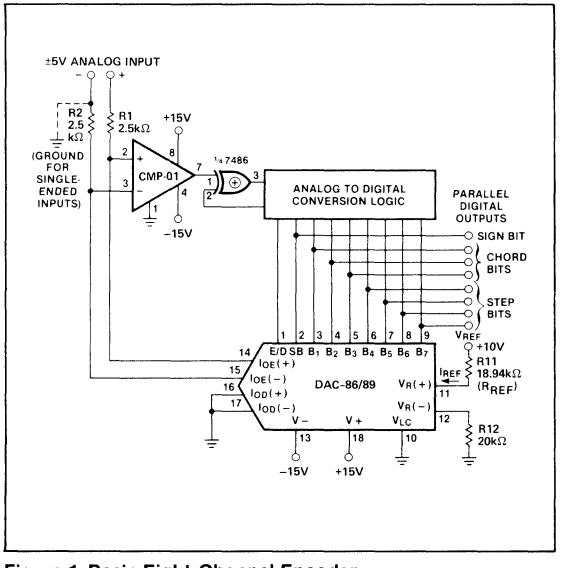


Figure 1. Basic Eight-Channel Encoder

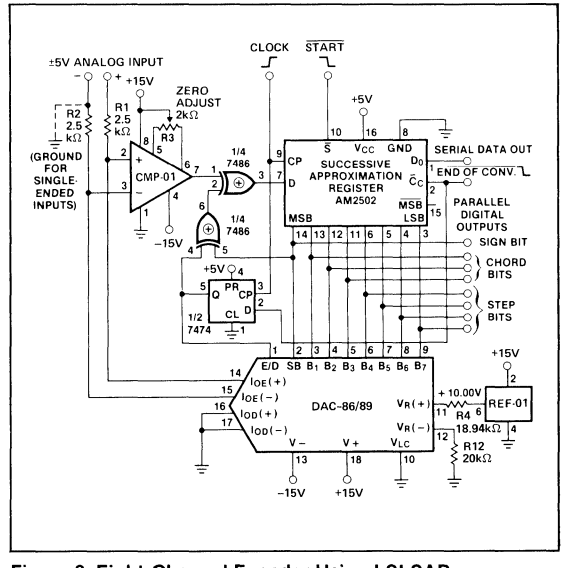


Figure 2. Eight-Channel Encoder Using LSI SAR

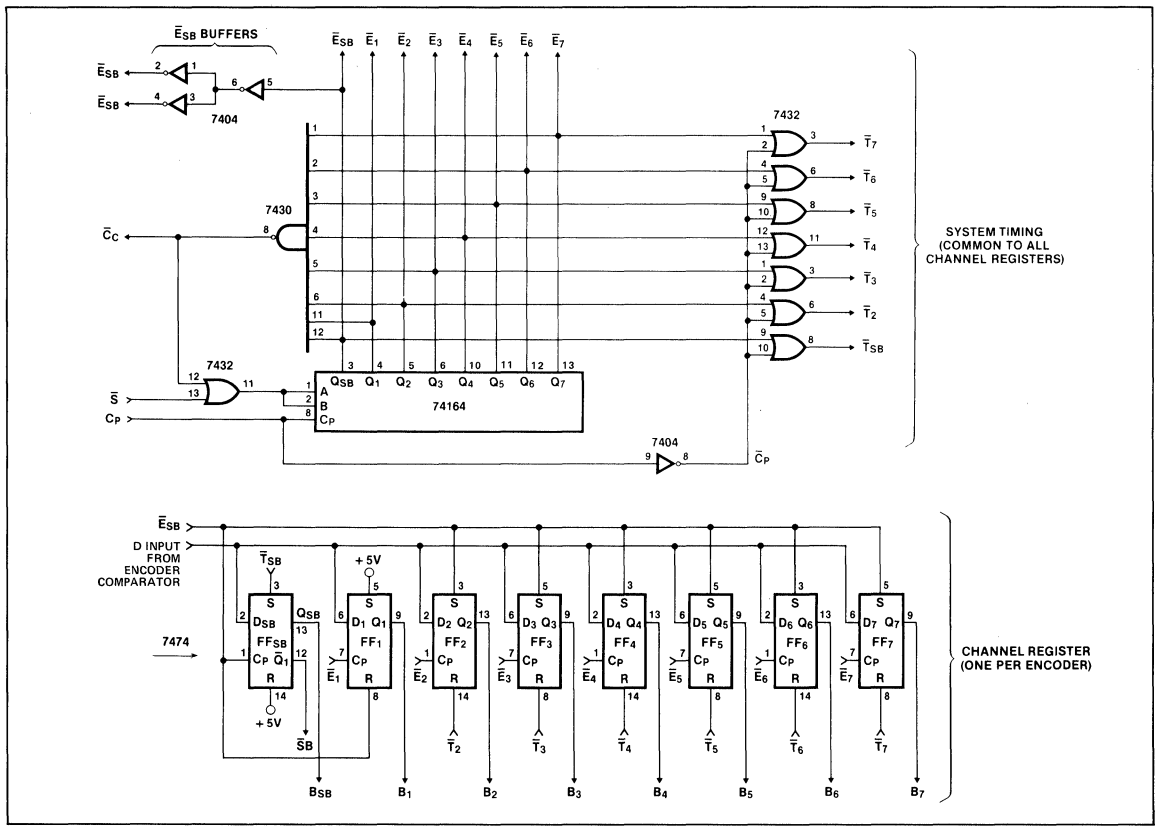


Figure 3. Successive Approximation Register

The start conversion pulse $\overline{S}$ occurs just before positive-going clock edge $C_{\overline{S}}$ as shown on the SAR waveforms. The 74164 shift register will have all Q outputs at the 1.0 level so long as the circuit has been operating for eight or more clock pulses. With $\overline{S}$ high the OR gate will continue to input a logic one into the shift register on every pulse. With all inputs at logic one the 7430 eight input NAND gate will have a zero output, thus the $\overline{S}$ signal going low will cause the next clock pulse $C_{\overline{S}}$ to clock a zero into the shift register output Q_{SB} which becomes the leading edge of negative-going pulse $\overline{E}_{SB}$. Now one input lead to the 7430 is a zero and the output of the NAND gate goes to logic one. The zero propagates down the shift register appearing on outputs Q_{SB} to Q_7 in succession, keeping the NAND gate output at logic one. Because of the OR gate this logic one is clocked repeatedly into the shift register outputs from Q_{SB} to Q_7. The cycle will not repeat if $\overline{S}$ is not held low for longer than 8 clock cycles; however, the actual duration of the $\overline{S}$ pulse is not important so long as it does not cause the circuit to recycle. The S pulse need not be synchronized with the clock. $\overline{C}_C$ stays high for 8 clock cycles.

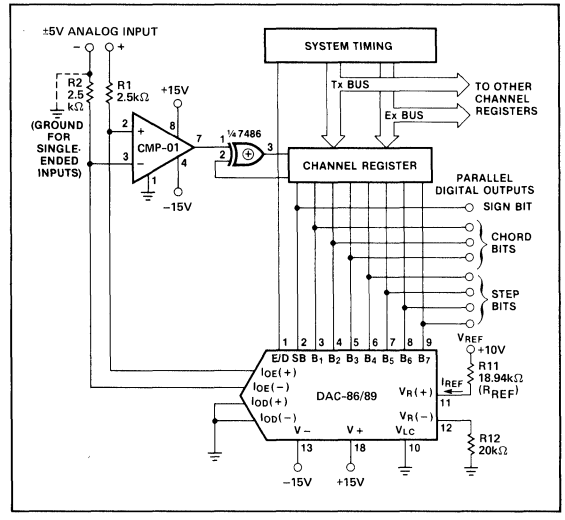


Figure 4. Eight-Channel Encoder with Improved Design SAR

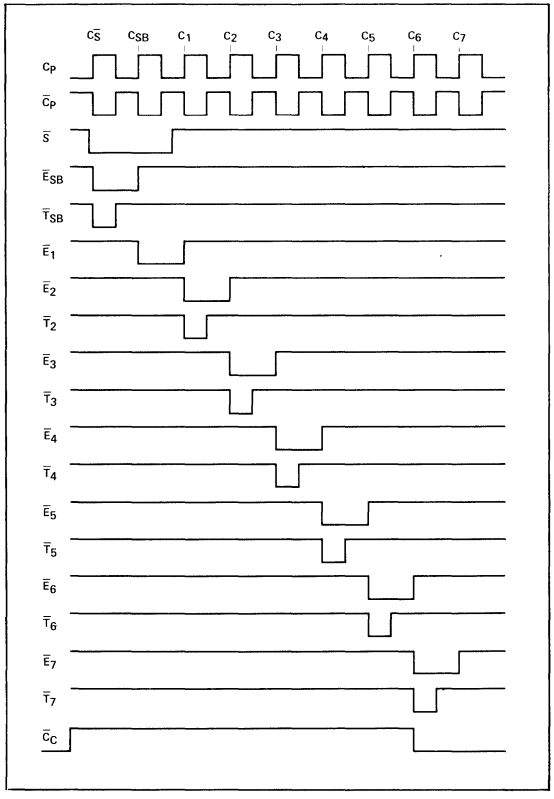


Figure 5. SAR Waveforms

As E_{SB} goes to zero it resets FF_1 and sets FF_2 through FF_7. When the circuit is used with the encoder circuit shown here, $\overline{E}_{SB}$ is used to keep the DAC in the decode mode for the duration of $\overline{E}_{SB}$. $\overline{T}_{SB}$, which is logically $\overline{E} + \overline{C}_P$, occurs at the leading edge of $\overline{E}_{SB}$ and sets FF_{SB} to SB = 1. Thus, on the first clock edge after $\overline{S}$ goes low the SAR is set to 10111111. The trailing edge of $\overline{E}_{SB}$ is used as a clock for FF_{SB} so that the comparator output, which represents the sign bit so long as the DAC is being held in the decode mode, is clocked into FF_{SB}. The $\overline{Q}$ output of FF_{SB} becomes the SB signal which drives the control input of the exclusive-OR gate.

By forcing this signal to a zero during the Sign Bit trial the exclusive-OR gate is in the proper non-invert mode while the sign bit is generated. $\overline{E}_1$ goes low just as $\overline{E}_{SB}$ goes high. No $\overline{T}_1$ signal is needed since FF_1 was set low during the initial setting. The rising edge of $\overline{E}_{SB}$ puts the DAC-86/89 back into the encode mode. The DAC internal circuit has been settling to the X0111111 magnitude output since the first clock after $\overline{S}$ went low, so the rising edge of $\overline{E}_1$ will clock the most significant bit of the quantized signal into FF_1. The remainder of the conversion proceeds as follows: $\overline{T}_2$ resets FF_2 and the rising edge of $\overline{E}_2$ clocks the second most significant bit into FF_2. $\overline{T}_3$ resets FF_3 and the rising edge of $\overline{E}_3$ clocks the second most significant bit into FF_3 and so on through $\overline{T}_7$ and $\overline{E}_7$.

E_{SB} BUFFERS

The implementation of this SAR requires a package count of 4 for the system timing which can then be shared over 3 channel registers, provided the $\overline{E}_{SB}$ buffers are properly used to prevent excessive fan-out on the $\overline{E}_{SB}$ line.

CONCLUSION

A low cost, alternative method of successive approximation register design has been shown which is optimized for use with multi-channel encoders for PCM systems.

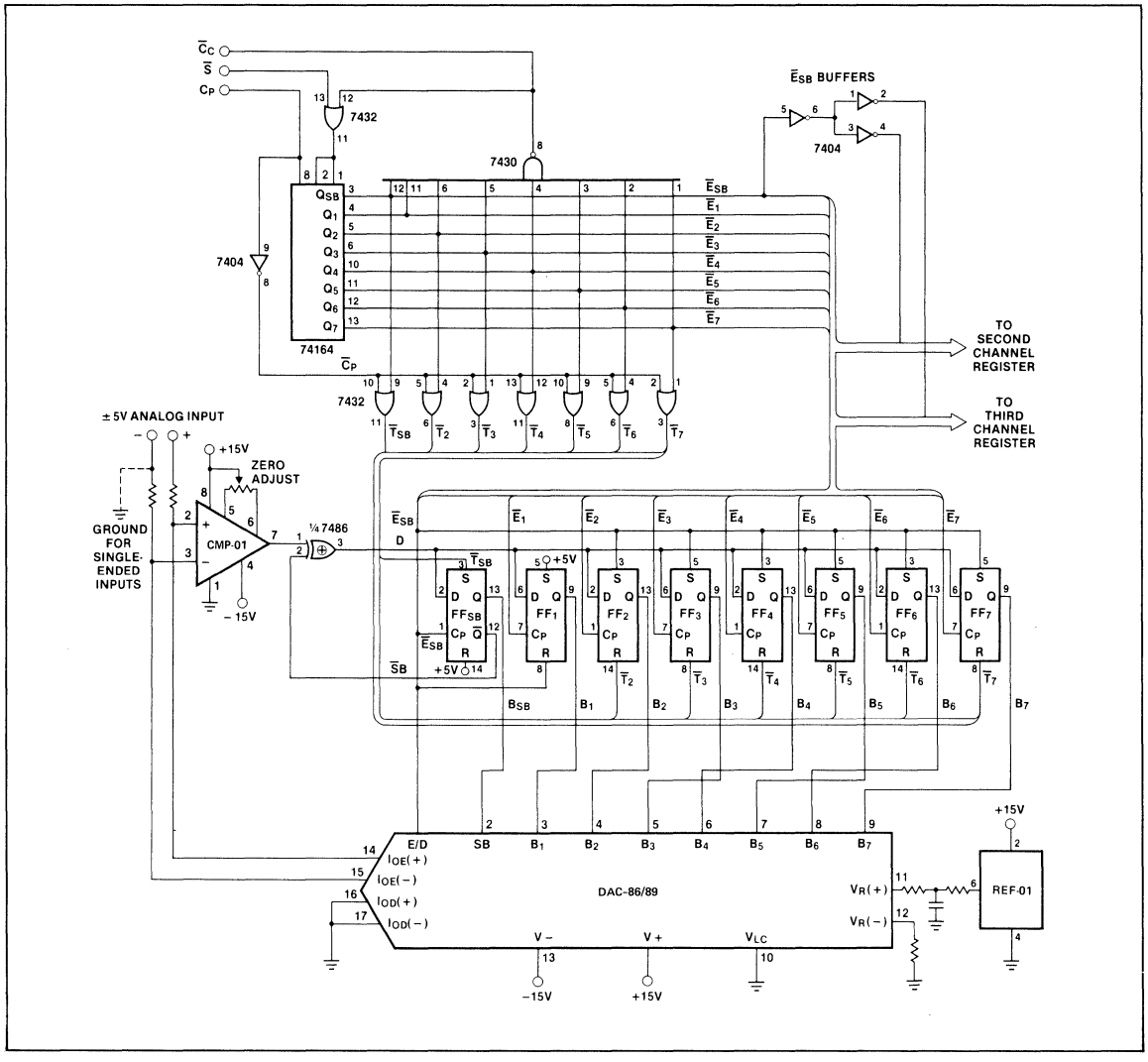


Figure 6. Improved Eight-Channel Encoder Complete Schematic

INTRODUCTION

In addition to normal operation (+/− supplies), the PMI family of JFET multiplexers (MUX-08/88, MUX-24, MUX-16, and MUX-28) performs quite well in single supply systems. This Application Note explains single supply operation as it applies to JFET and CMOS multiplexers. Common requirements are in battery-operated systems and in microprocessor-based, single supply data acquisition systems. JFET and CMOS devices are compared for R_{ON} variation versus power supply voltage (V_S), then settling times.

CONNECTIONS FOR SINGLE SUPPLY OPERATION

Figure 1 shows single supply connections for the entire PMI JFET multiplexer family. Each multiplexer handles 0 to +10V signals with a +15V supply. The signal range is conservatively rated to be (V_S − 4V) as a maximum, and zero volt as a minimum.

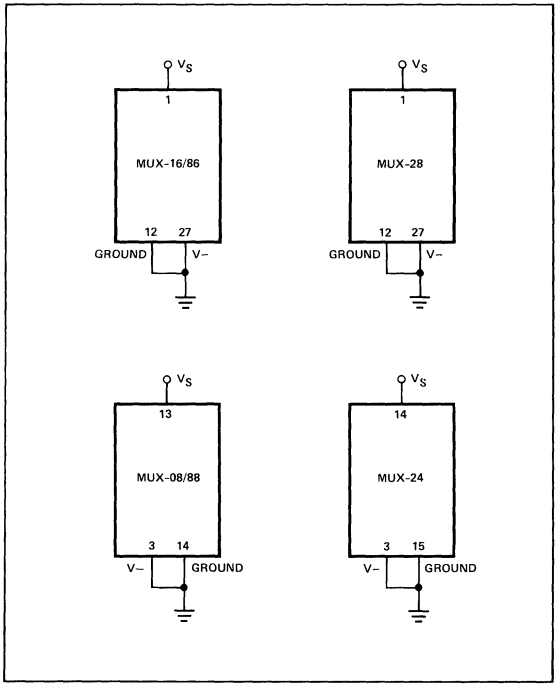


Figure 1. JFET Multiplexer Single Supply Connections

JFET VARIATION OF R_{ON} WITH V_S (MUX-08)

Figure 2 shows the test circuit and defines the test conditions (MUX-08). Figure 3 shows the performance of a MUX-08 driving a 1kΩ load. The positive voltage should be 1.10V and the negative voltage should be −0.4V. The reason for the output voltages being less (magnitude) than the above is due to the R_{ON} of the multiplexer switches. Curves 1 and 2 show that R_{ON} does not vary as V_S varies from +5V to +15V.

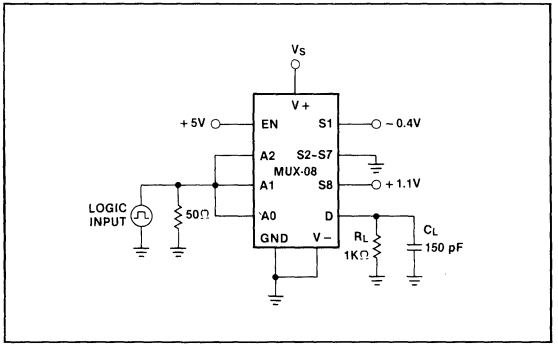


Figure 2. Test Circuit

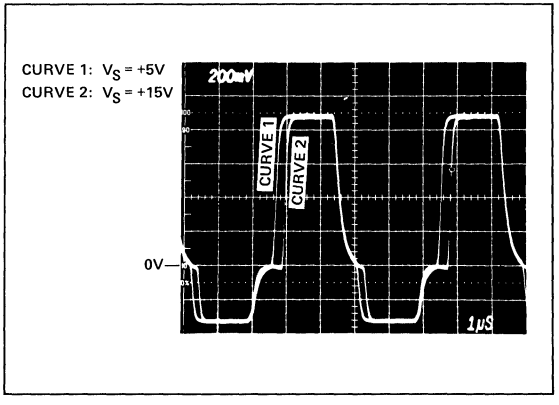


Figure 3. JFET Variation of R_{ON} with V_S

CMOS VARIATION OF R_{ON} WITH V_S (508 Pin-Compatible Device)

The CMOS multiplexer (connected as shown in Figure 4) **does** show a variation in R_{ON} as V_S is varied from +6V to +15V. This is evidenced by the curves shown in Figure 5. Note that while the positive peak voltages in Figure 3 are the same for both curves, the peaks differ in Figure 5.

One very important consideration when choosing a multiplexer is the nonlinearity (or distortion) introduced by the switch when it is ON. What is important is the **change** in R_{ON} which occurs because of external variations such as power supplies. In particular, the variation in R_{ON} shown in Figure 3 is 148 ohms. The R_{ON} at $V_S = +6V$ is 1000 ohms, while its value at $V_S = +15V$ is only 852 ohms. A change of 148 ohms represents a 1.48% error if the load resistor is 10,000 ohms. In battery-operated systems (which is what a lot of single supply applications are), distortion due to power supply variations is generally not acceptable.

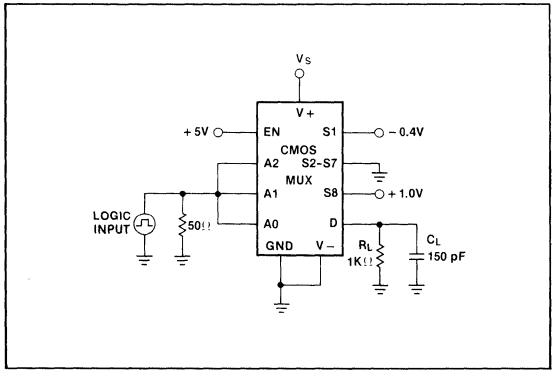


Figure 4. Test Circuit

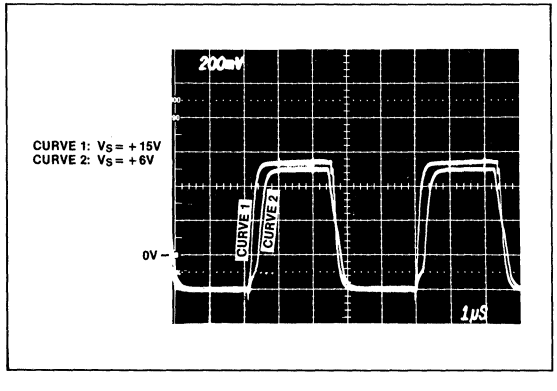


Figure 5. CMOS Variation of R_{ON} with V_S

CMOS vs JFET — EFFECT OF R_{ON} ON SETTLING TIME

Figure 6 defines the test conditions used for the JFET and CMOS multiplexer curves shown in Figure 7. In this case, R_L is large enough so that the output voltages will reach the input voltage levels. Note that MUX-08 does just that, while the CMOS multiplexer does not reach the final value.

The problem is settling time, and occurs because the R_{ON} of the CMOS device is considerably larger than the MUX-08 (852 ohms as opposed to 250 ohms). A final note concerns the fact that the multiplexers are switching signals at 400mV more negative than the negative supply voltage without appreciable distortion. In no circumstances should the input exceed one diode voltage below the negative supply voltage.

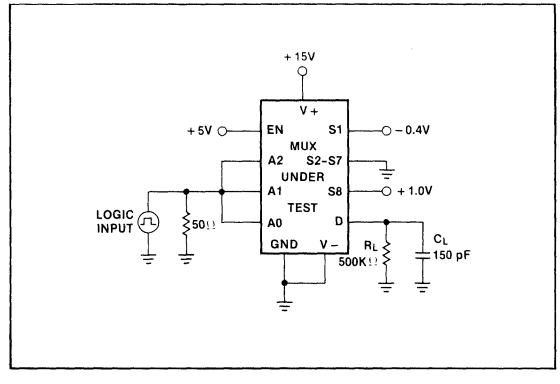


Figure 6. Test Circuit

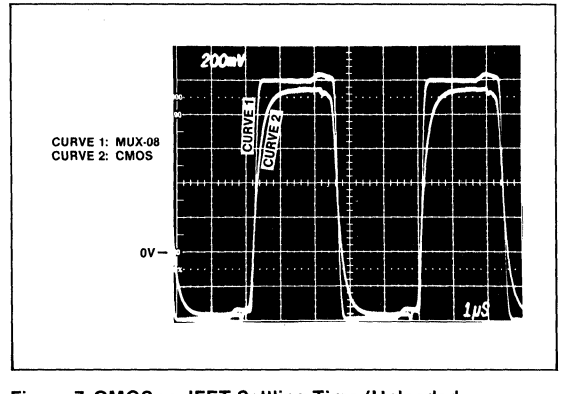


Figure 7. CMOS vs JFET Settling Time (Unloaded Output Voltage)

CONCLUSION

The information presented has shown how JFET multiplexers handle analog inputs in single supply systems, with R_{ON} independent of power supply variations, and with fast settling time.

AN-35
UNDERSTANDING CROSSTALK IN ANALOG MULTIPLEXERS

Precision Monolithics Inc.

APPLICATION NOTE 35

INTRODUCTION

One of the most troublesome errors in analog multiplexers is crosstalk. Various schemes have been devised to reduce its effects. One designer will terminate the multiplexer in a 10kΩ resistive impedance. Another will short the multiplexer node to ground between address changes with an analog switch. A third engineer will terminate the multiplexer node in 1MΩ because he doesn't want to live with the attenuation which comes about with any lower impedance. What is confounding about these three situations is that the solution is correct in each case. THE CORRECT SOLUTION IS DICTATED BY THE APPLICATION.

To understand why the solution is application dependent, it is necessary to dig rather deeply into what crosstalk really is. When this is done, crosstalk is found to have not one, but three components in a multiplexer. To differentiate the components one from the other, it is convenient to give them names:

1. Static crosstalk (CT)
2. Dynamic crosstalk (DCT)
3. Adjacent Channel crosstalk (ACCT)

This application note explains the three crosstalk components qualitatively and quantitatively. The qualitative discussion tells what component(s) should be considered in various applications. The quantitative discussion uses both theoretical and empirical information to arrive at conclusions about what performance should be expected.

STATIC CROSSTALK (CT)

To introduce the concept of crosstalk, Figure 1 is helpful. A basic analog switch may be constructed with a FET (JFET or CMOS) and a suitable driver which switches it OFF and ON, as shown in Figure 1a. The equivalent circuit, as shown in Figure 1b, models the analog switch such that when the ideal switch (SW) is closed, the switch has an ON resistance R_{ON}. When SW is open, the OFF impedance is determined by C_{EQ}. A two-channel multiplexer circuit, made up of two analog switches connected as shown in Figure 1c, shows how signals from one channel can be coupled into the other channel. Theoretically, V_{OUT} consists of e_1 modified by the resistor divider formed by R_{ON1} and R_L (assumes reactance of C_L is $\gg R_L$). However, the capacitance of switch number two (C_{EQ2}) does couple some portion of e_2 into V_{OUT}. This is the simplest example of crosstalk.

The model which explains static crosstalk is relatively simple and may be derived from the OFF isolation model. Figure 2a shows the OFF isolation model as capacitive coupling from the input to the output of an OFF switch. This condition may be duplicated in Figure 1c by opening SW_1 and setting $e_2 = 0$. Coupling from input to output is accomplished through C_{EQ},

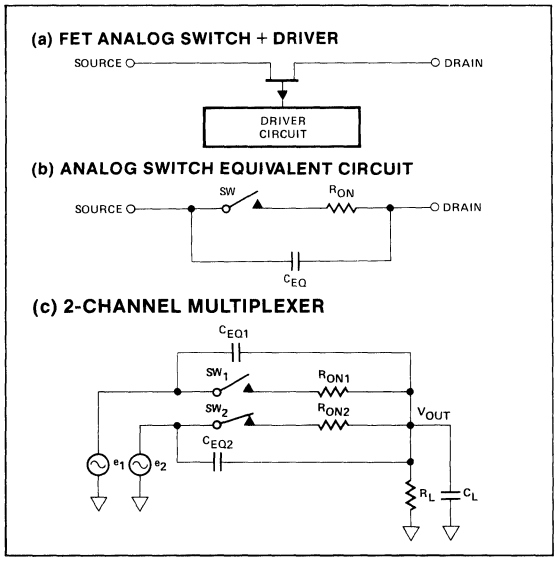


Figure 1. Essentials of an Analog Multiplexer

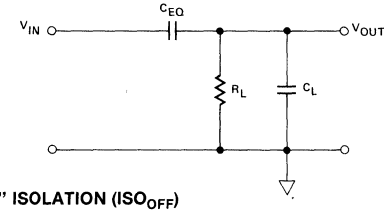
and this parameter may be computed from measurements of V_{IN}, V_{OUT}, and frequency. In the case of static crosstalk, C_{EQ} is shown coupling into a parallel combination of R_{ON} with R_L and C_L (Figure 2b). The two channel multiplexer shown in Figure 1c reduces to the circuit in Figure 2b, where $e_1 = 0$, $e_2 = V_{IN}$, and C_{EQ} is the coupling capacitance from e_2 to V_{OUT}.

Since R_L is generally 10kΩ or more, and typical analog switches are less than 1kΩ, static crosstalk is much smaller than OFF isolation. The crosstalk and OFF isolation numbers quoted on analog multiplexer data sheets are derived from the models shown in Figure 2. Unfortunately the one component of crosstalk specified is the least troublesome of the three. However the crosstalk figures on data sheets will alert the designer to those devices which absolutely will not satisfy his requirements.

There are applications where the static crosstalk specification given on data sheets is adequate. When the multiplexer is being used as a one-of-many switch, and is not being cycled through all channels on an automatic basis, then the static crosstalk component will give accurate prediction of the actual performance. Examples of such applications are:

1. Audio/Video Selector Switch
2. Programmable Gain Amplifier
3. Programmable Power Supply

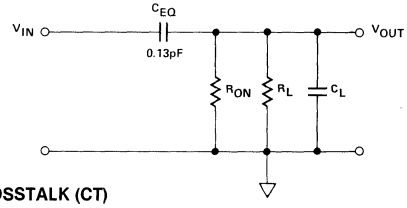
(a) OFF ISOLATION EQUIVALENT CIRCUIT



"OFF" ISOLATION (ISO_{OFF})

The proportionate amount of a high frequency analog input signal which is coupled through the channel of an "OFF" device. This feedthrough is transmitted through $C_{DS(OFF)}$ to a load comprised of $C_{D(OFF)}$ in parallel with an external load. Isolation generally decreases by 6dB/octave with increasing frequency.

(b) STATIC CROSSTALK EQUIVALENT CIRCUIT



CROSSTALK (CT)

The proportionate amount of cross-coupling from an "OFF" analog input channel to the output of another "ON" output channel.

Figure 2. Model for Static Crosstalk

DYNAMIC CROSSTALK (DCT)

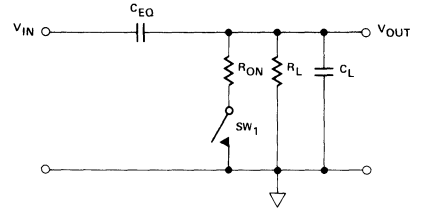
The dynamic crosstalk model can be derived from Figure 3. The switch SW_1 represents one condition on the multiplexer node (SW_1 is open). Actually SW_1 is continually switching between OFF and ON. This is represented in Figure 3b. In order to reduce crosstalk, multiplexers are designed to have break-before-make switching so that no two channels are addressed at the same time. The finite open time of SW_1 (shown in Figure 3b) represents the break-before-make action. There are two "open" conditions on the multiplexer node per cycle of the clock; thus the equivalent nodal resistance (R_{EQ}) may be computed as given in Figure 3b. Table I shows some typical values of static and dynamic crosstalk. Static crosstalk values are given in lines 1 and 12. There is a change in crosstalk as the clock frequency (f_{CLK}) is varied. Starting at line 4 notice the variation in crosstalk as R_L is varied from 10kΩ to 100kΩ while f_{CLK} remains constant at 100kHz. While Table I yields some theoretical values which give insight into the operation of dynamic crosstalk, a working multiplexer will have different values of f_{CLK} with respect to the maximum value of f_{SIG}. The real world situation will be analyzed in a later section of this paper.

Examples of multiplexer applications which are dynamic in nature are:

1. Industrial Process Control
2. Telephony
3. Data Acquisition Systems
4. Telemetry

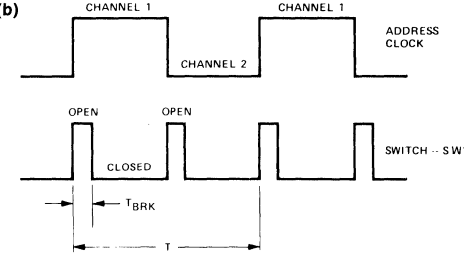
Each one of the above applications are a form of Time Division Multiplexing. In other words, these are sampled-data

(a) DYNAMIC CROSSTALK EQUIVALENT CIRCUIT



NOTE: SWI is a time dependent switch. Its characteristic is shown in Figure 3b.

(b)



T ≡ Period of address clock

T_{BRK} ≡ Break-Before-Make Time

$$\text{If } R_L \gg R_{ON},\ R_{EQ} \cong \frac{R_{ON}(T - 2T_{BRK}) + 2R_L T_{BRK}}{T}$$

Figure 3. Model for Dynamic Crosstalk

Table 1. Computed Values of Static and Dynamic Crosstalk

LINE NO.	f_{SIG} Hz	f_{CLK} Hz	T μsec	T_{BRK} μsec	R_{ON} OHMS	R_L OHMS	R_{EQ} OHMS	C_{EQ} pF	CROSS-TALK dB
1	10K	0	—	0.80	300	10K	291	0.30	105
2	10K	20K	50	0.80	300	10K	602	0.30	99
3	10K	40K	25	0.80	300	10K	913	0.30	95
4	10K	100K	10	0.80	300	10K	1845	0.30	89
5	10K	100K	10	0.80	300	20K	3448	0.30	84
6	10K	100K	10	0.80	300	40K	6650	0.30	78
7	10K	100K	10	0.80	300	100K	16.25K	0.30	70
8	20K	50K	20	0.80	300	10K	1068	0.30	88
9	20K	50K	20	0.80	300	20K	1872	0.30	83
10	20K	50K	20	0.80	300	40K	3474	0.30	78
11	20K	50K	20	0.80	300	100K	8275	0.30	70
12	20K	0	—	0.80	300	100K	291	0.30	99

systems where each channel is being continuously sampled and the information for a given channel is contained in a given time slot. In these applications, the static crosstalk is almost meaningless, since the wrong choice of R_L (or f_{CLK}) can be disastrous.

ADJACENT CHANNEL CROSSTALK (ACCT)

Adjacent channel crosstalk is the most confusing component of crosstalk. In addition to its confusing nature, in some cases, it is the most dominant component. While both static and dynamic crosstalk are capacitive in nature, i.e., they vary with frequency at 6dB/octave, the adjacent channel crosstalk is **invariant with frequency**. In other words, it is possible to have crosstalk **when multiplexing DC signals** such as the outputs of thermocouples, pressure transducers, etc. The parameters which must be dealt with are R_L, C_L, R_{ON}, and f_{CLK}. In addition, the break-before-make time ($=T_{BRK}$) of the multiplexer is of importance. Before diving into the details of this component of crosstalk, it will be helpful to define what is meant by ACCT.

The term "adjacent" refers to time only. In other words, channel two is adjacent to channel one if channel two **immediately** follows channel one in time slots. Since the channel following is the "adjacent" channel, then channel one is not adjacent to channel two, but rather the other way around. Figure 4 illustrates the concept of adjacent channels. Assuming the multiplexer had, say, 1V on channel one, 2V on channel two, etc., then the output would look like the curve labeled "channel addressed." What is important about the waveforms in Figure 4 is the way the adjacent channel (in time) is shown. Note that while channel two is adjacent to channel one, channel one is itself adjacent to channel eight.

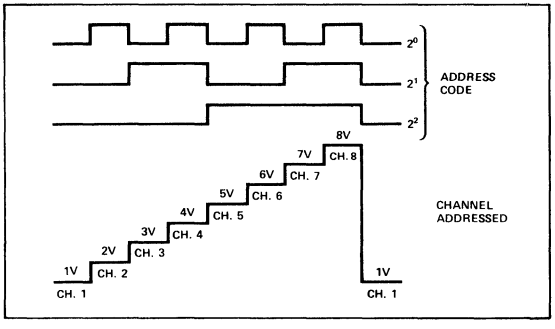


Figure 4. Adjacent Channel Concept

The fact that information is "carried forward" from one channel to the next (in time) suggests a storage mechanism as causing ACCT. Thus the multiplexer nodal capacitance becomes the prime suspect. Figure 5 illustrates how information is carried forward from one channel to the next as the addresses are changed. The address code is shown in Figure 5a, while Figure 5b shows the theoretical multiplexer output. Note that the even numbered channels have zero volt on them, while the odd channels have their channel number in volts. This arrangement best illustrates how the

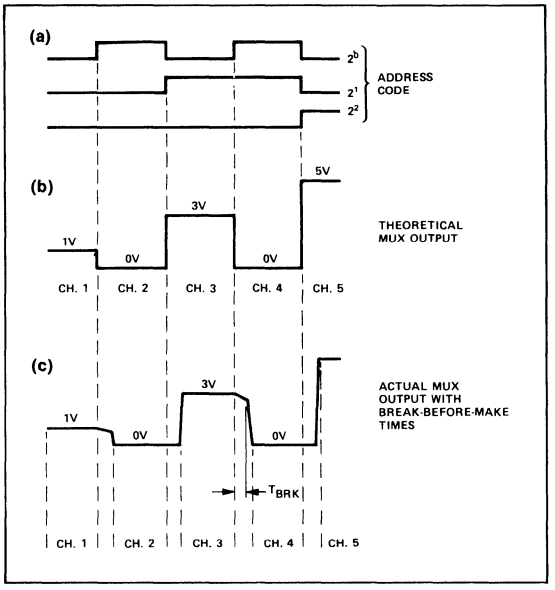


Figure 5. Adjacent Channel Crosstalk

information is transferred to the adjacent channel (as shown in Figure 5c). While the theoretical MUX output switches from channel three (3 volts) to channel four (0 volt) at the moment of the address change, note the delay in the actual MUX output caused by T_{BRK}. During this time the MUX node discharges along an RC curve determined by the load capacitance (C_L), and the load resistance (R_L). When the break-before-make time (T_{BRK}) is over, channel four is turned ON and the RC product is suddenly reduced to $R_{ON}C_L$. A curve which details how this all takes place is shown in Figure 6. Before leaving Figure 5, the arrangement suggests a method of avoiding adjacent channel crosstalk. In other words, the alternate grounding of channels prevents channel one signals from reaching channel three... channel three from reaching channel five, etc.

The curve in Figure 6a shows a typical nodal discharge for a set of real world conditions. The curve is normalized and T_{BRK} is chosen to be 900nsec. An accepted method of measuring T_{BRK} is from the 50% point of the channel which has been turned OFF to the 50% point of the channel which is being turned ON. This concept is illustrated in Figure 6b. In this case (Figure 6a) T_{BRK} is measured from the moment of the address change. While this is not totally correct, the agreement between theoretical and actual results is good enough to justify the simpler model which is derived. Since most designers are interested in crosstalk which is less than the resolution of the discharge curve, the ACCT vs. time graph gives crosstalk down to 90dB. In other words, the ACCT is down 90dB in less than 1.25μsec.

Adjacent channel crosstalk is a problem in every application where dynamic crosstalk must be considered; however there are techniques to minimize its effects. A popular way to diminish adjacent channel crosstalk is to short the

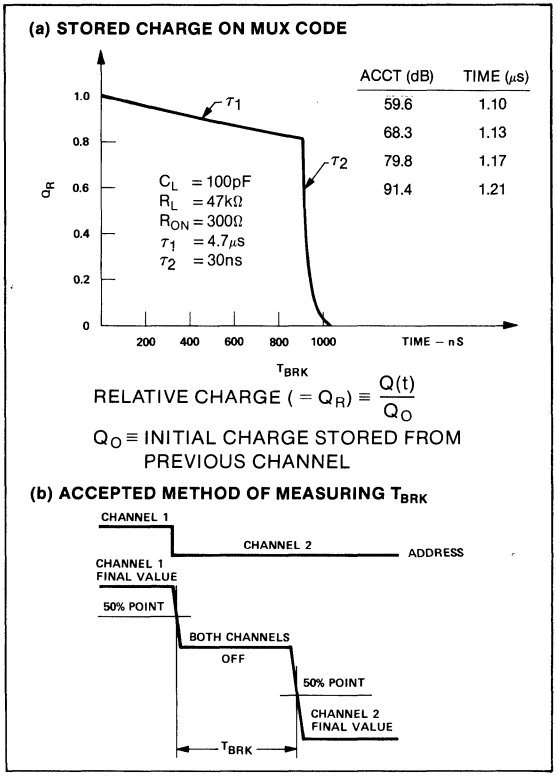


Figure 6. Stored Charge Decay and Definition of T_{BRK}

multiplexer node to ground between address changes. Tnis requires an additional analog switch which should be fast and have low R_{ON}. An alternative approach to reducing adjacent channel crosstalk is to ground every other channel in a multiplexer. This technique was illustrated in Figure 5.

MEASUREMENT OF STATIC CROSSTALK

Figures 7 and 8 give the element values for a typical PMI JFET MUX-08 on channel three. In the case shown, the OFF isolation was first measured and found to be 75dB. With R_L and f_{SIG} known, then C_{EQ} was calculated. Once C_{EQ} is known, then R_{EQ} may be calculated from the static crosstalk measurement made in Figure 8. R_{EQ} is the parallel combination of R_L and R_{ON}; thus it is possible to compute R_{ON} and this value is also shown in Figure 8. The measurements thus far are relatively simple and only require a voltmeter which is capable of measuring signals which are 100dB below the reference signal. On the other hand, the measurement of dynamic crosstalk is a bit more involved, and requires a more complex system.

MEASUREMENT OF DYNAMIC CROSSTALK

The crosstalk measuring system shown in Figure 9 is to be used for measuring dynamic crosstalk. The signal from M_5 is fed into M_1 where it is multiplexed onto the OUT terminal.

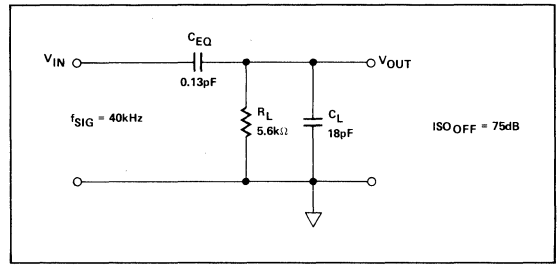


Figure 7. Typical OFF Isolation Element Values

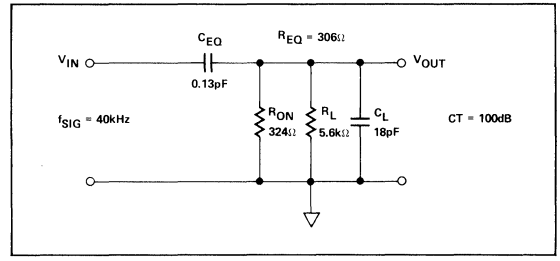


Figure 8. Typical Static Crosstalk Element Values

M_1 contains the multiplexer under test and a decoding circuit. The decoding circuit allows the selection of any two channels to be used as a two channel multiplexer. M_2 is a high-speed buffer used for driving the IN terminal of M_3. M_3 contains a multiplexer operated in a demultiplexer mode, along with decoding circuitry to allow several combinations of two channel demultiplexing. The signal which appears on S_{3A} is fed through M_4 (high-speed buffer) to M_8 for spectrum analysis. In short, if no errors are introduced by the multiplexer-demultiplexer system, the output should be the same as the input.

Since the system in Figure 9 is capable of measuring dynamic crosstalk, a good check of its performance is to repeat the static crosstalk measurements. M_3 is set to have IN connected to S_{3A} at all times. M_1 is set to have S_3 connected to OUT, and the signal thus measured is taken as the reference signal. Static crosstalk is measured by connecting S_1 (or S_8) to OUT, with V_{IN} still applied to S_3, and again measuring V_{OUT}. The relative signal levels represent static crosstalk. This measuring technique was used to verify the accuracy of the system.

The measurement of dynamic crosstalk leaves M_3 exactly as in the static case. With V_{IN} connected to S_3, M_1 is switched between S_1 and S_8. The signal frequency (f_{SIG}) was 40kHz and f_{CLK} was 100kHz (see Figure 10). From the crosstalk measured, the equivalent resistance (R_{EQ}) is computed to be 1150Ω (see Figure 10a). To verify the validity of this measurement, R_{EQ} was calculated using the formula in Figure 10c (T_{BRK} was measured separately). Since there is very good agreement between these two independently derived values, both the measurement technique and the dynamic crosstalk model are valid.

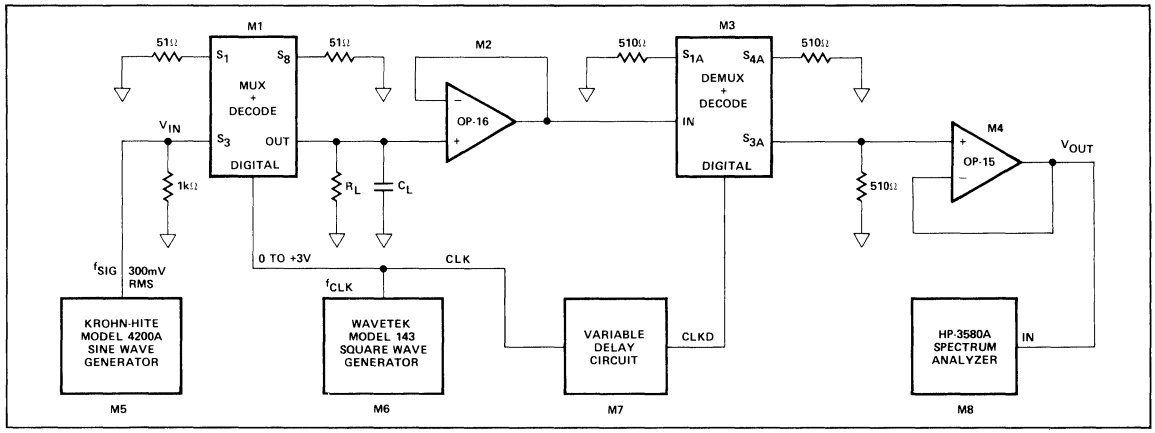
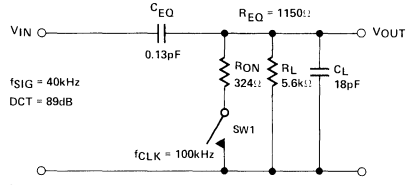


Figure 9. Dynamic Crosstalk Measuring System

(a) TYPICAL DYNAMIC CROSSTALK ELEMENT VALUES

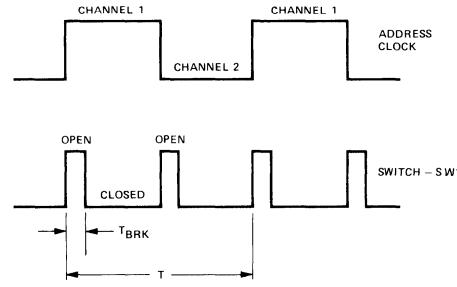


NOTE: SWI is a time dependent switch. Its characteristic is shown in Figure 10c.

(b) SYSTEM DYNAMIC CROSSTALK

f_{SIG}	f_{CLK}	R_L	R_{EQ}	DCT (C_{EQ} = 0.13pF)	DCT (C_{EQ} = 0.5pF)
Hz	HZ	Ω	Ω	dB	dB
10K	100K	10K	1718	97.1	85.4
10K	100K	22K	3463	91.0	79.3
10K	100K	33K	5059	87.7	76.0
10K	100K	47K	7090	84.7	73.0
10K	100K	100K	14.78K	78.4	66.7

(c)



$T = 5\mu s$
$T_{BRK} = 725ns$
$R_{EQ} = 1089\Omega$
T ≡ Period of Address Clock
T_{BRK} ≡ Break-Before-Make Time

$$\text{If } R_L \gg R_{ON},\ R_{EQ} \cong \frac{R_{ON}\,(T - 2T_{BRK}\ (+\ 2R_L\ T_{BRK})}{T}$$

Figure 10. Computed Dynamic Crosstalk for Actual Multiplexer

The numbers shown in Figure 10 apply to the measurement system, but are unlikely in a real multiplexer. To satisfy sampling theory limitations, f_{SIG} must be less than one-half the sampling frequency. Assuming f_{CLK} = 200kHz then each channel in a multiplexer is addressed for 5μsec. This means that it takes 40μsec to sample all channels of an eight channel multiplexer. In other words, **each channel** is sampled at a 25kHz rate. Thus the maximum value of f_{SIG} would be 12.5kHz. Figure 10b gives values of dynamic crosstalk (DCT) which would be experienced if the values of R_{ON} and T_{BRK} shown in Figures 10a and 10b were used. The first DCT column lists the values for a C_{EQ} of 0.13pF (measured value of channel three). The second DCT column shows the performance for C_{EQ} = 0.5pF. The purpose for the second column is to point out how critical minimizing stray capacitance is to good crosstalk performance.

MEASUREMENT OF ADJACENT CHANNEL CROSSTALK

The system shown in Figure 11 was used to measure adjacent channel crosstalk (ACCT). M_1 drives the address lines of the MUX system and the gating input of M_4. By setting the period of M_4 (T_2) to 10μsec, the pulse rate out of M_4 is controlled by the pulse rate of M_1 (40μsec) coming into the gate input of M_4. The output of M_4 is in the complement mode

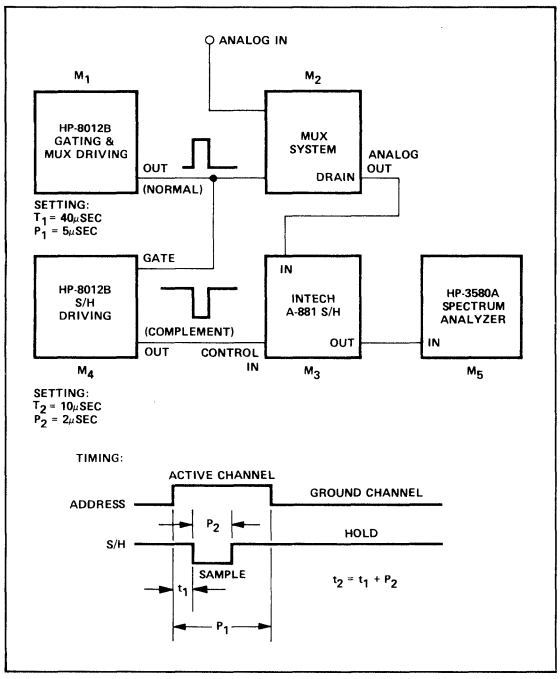
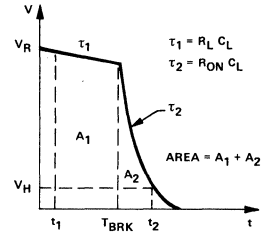


Figure 11. Adjacent Channel Crosstalk Measuring System

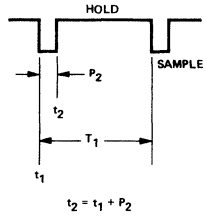
because the control input to M_3 causes the S/H to HOLD when the input is high (1). Thus the sample period occurs during the time P_2. M_4 also can delay its pulse relative to the pulse out of M_1, thereby allowing measurements of crosstalk versus t_1 (start of the sample time). This information is valuable because in many systems, a sample/hold is used with a successive approximation ADC to encode the analog output of the MUX. As will be shown, the ACCT can be made negligible if a sufficient time elapses before going to the HOLD mode for encoding the data. Since "time is money," the term "sufficient time" becomes important.

The nature of sample/holds and the nature of spectrum analyzers can cause some apparent discrepancies in the data observed by this measurement system. It is important to note the spectrum analyzer "sees" the average of **everything** that is presented to its input terminals. While it is true the sample/hold holds the last value it "saw," the spectrum analyzer also looks at the signal present during the sample/hold's sample time. Thus the equation which expresses the signal level present as a function of time must also account for the true averaging of the spectrum analyzer. Figure 12 shows the equations (12c) and the definitions of the terms used in the equations (12a and 12b). The term N_O is the **relative** signal level which the spectrum analyzer measures. If the model of the signal decay shown in Figure 12a is the correct one to explain the ACCT, then the computed value of N_O should correspond to the measured values. As will be shown in Figure 14, the agreement does in fact justify the model; however it was necessary to choose the measurement conditions **very carefully.**

(a) VOLTAGE DECAY ON MUX OUTPUT



(b) SAMPLE/HOLD



(c)

EQUATIONS:

1. $$\frac{V_O}{V_R} \equiv N_O = \frac{N_H(T_1 - P_2) + S_1 + S_2}{T_1}\text{; Where}$$

2. $$\frac{V_H}{V_R} \equiv N_H = EXP\left[\frac{-t}{\tau_1}\right],\ t \le T_{BRK}$$

$$= EXP\left[\frac{-T_{BRK}}{\tau_1}\right] EXP\left[\frac{T_{BRK} - t}{\tau_2}\right],\ t \ge T_{BRK}$$

3. $$\frac{A_1}{V_R} \equiv S_1 = \tau_1\left[EXP\left(\frac{-t_1}{\tau_1}\right) - EXP\left(\frac{-T_{BRK}}{\tau_1}\right)\right]$$

4. $$\frac{A_2}{V_R} \equiv S_2 = \tau_2\, EXP\left[\frac{-T_{BRK}}{\tau_1}\right]\left[1 - EXP\left(\frac{T_{BRK} - t_2}{\tau_2}\right)\right]$$

Figure 12. Predicting the Measurement System Response

In order to get good correlation between lab data and theoretical predictions, it was necessary to use fairly long time constants ($R_L = 22k\Omega$ and $C_L = 1000pF$). With $R_L = 22k\Omega$ and $C_L = 50pF$ ($R_{ON} = 300\Omega$), the theoretical plot of ACCT (as measured on the spectrum analyzer) vs. t_1 is shown in Figure 13. Note that the data is plotted between 900nsec and 1025nsec. The curve shows that a **10nsec error in t_1 can cause a 6dB error** in reading on the spectrum analyzer. The results shown in Figure 14 confirm the necessity of using large capacitances to obtain predictable results. The theoretical curve tracks the actual data well in both cases; however the 1000pF curve is better than the 300pF curve. Notice that there is good agreement both at DC and at 4kHz.

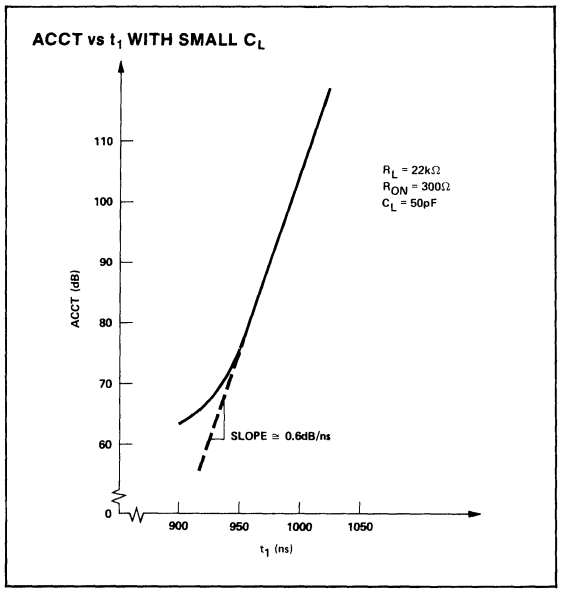


Figure 13. Measurement Errors Due To Small C_L

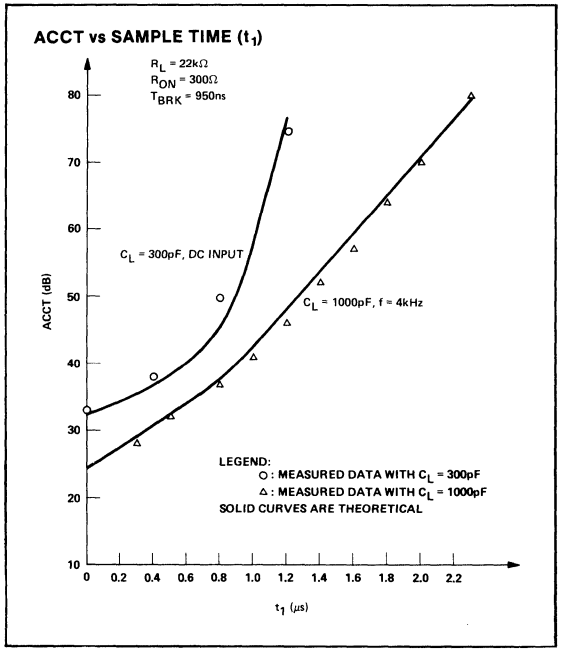


Figure 14. Agreement Between Measured and Computed ACCT

PREDICTING AND CONTROLLING ADJACENT CHANNEL CROSSTALK

The equations in Figure 12c can be used to predict how much adjacent channel crosstalk one might expect in an actual system. An all analog system will follow the MUX with a

A. Multiplexer-Demultiplexer System:

$N_H \equiv 0$ Therefore

1. $N_O = \dfrac{S_1 + S_2}{T_1}$, Where $T_1 = \dfrac{1}{f_{CLK}}$ x (No. of Channels)

2. $S_1 = \tau_1 \left[EXP\left(\dfrac{-t_1}{\tau_1}\right) - EXP\left(\dfrac{-T_{BRK}}{\tau_1}\right)\right]$

3. $S_2 = \tau_2 \ EXP\left[\dfrac{T_{BRK}}{\tau_1}\right]\left[1 - EXP\left(\dfrac{T_{BRK} - t_2}{\tau_2}\right)\right]$

Where $t_1 = T_D$ (Break-Before-Make Time of DEMUX)

$$t_2 = \frac{1}{f_{CLK}} - T_D$$

B. Multiplexer — Sample/Hold System

$S_1 = S_2 = P_2 \equiv 0$

4. $N_O = N_H = EXP\left[\dfrac{-t}{\tau_1}\right] \quad t \le T_{BRK}$

$$= EXP\left[\frac{-T_{BRK}}{\tau_1}\right] EXP\left[\frac{T_{BRK} - t}{\tau_2}\right], \quad t \ge T_{BRK}$$

Where: $t = t_H$ (Hold Command for Sample/Hold as measured from Address Change Time)

Figure 15. Predicting Adjacent Channel Crosstalk

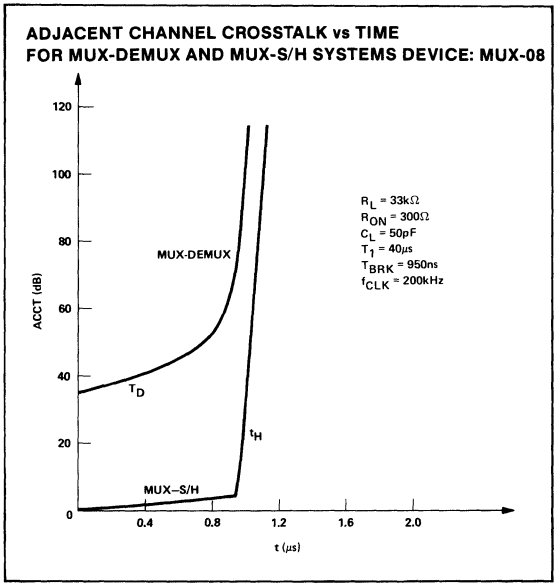


Figure 16. Computed ACCT vs Time for MUX-DEMUX and MUX-S/H Systems

demultiplexer, which will have its own break-before-make delay. An analog to digital system will have a sample/hold amplifier in front of the A/D converter. Since the equations which apply to these situations are different, they will be discussed separately. Figure 15 summarizes the conditions and the equations which apply to them.

Since there is no held voltage, then $N_H = 0$ in the multiplexer-demultiplexer system. This reduces N_O to the simple form shown in equation (1). S_1 and S_2 follow in equations (2) and (3). Since $t_1 = T_D$ (break-before-make time of the DEMUX), that time will have a significant effect on ACCT. The MUX-sample/hold system imposes the condition $S_1 = S_2 = P_2 = 0$; thus $N_O = N_H$. It will be instructive to compare the levels of ACCT in these two systems versus their appropriate times.

Figure 16 looks at a "typical" system which will give approximately one percent transmission error (33kΩ R_L and 300Ω R_{ON}), and has 50pF C_L. The value of C_L is somewhat on the high side (20pF being typical for MUX-08 connected to a buffer amp), but it does give a conservative value for analysis. What Figure 16 shows is rather startling. The adjacent channel crosstalk, while inherent in the multiplexer itself, can be eliminated in **both** systems by the proper timing. In the case of the sample/hold it is only necessary to delay the hold command for approximately 1.2μsec to have the ACCT vanish completely. This is no problem, since most sample/holds need at least 2μsec to accurately acquire the signal (this is particularly true of monolithic devices). The plot for the MUX-DEMUX system relates to T_D, which is **not adjustable** for a given DEMUX. What is possible is to add some delay to the address change for the DEMUX. In this way, the DEMUX will not "look" at the MUX output until the charge from the previous channel has had a chance to dissipate.

CONCLUSION

Table II summarizes the forms of crosstalk and lists ways of coping with them. Reduction of R_{ON} is helpful in all three cases. While T_{BRK} should be minimized as much as possible, it is important that no two channels are ON at the same time. In some cases, T_{BRK} is chosen such that even over temperature extremes, the break-before-make feature is maintained. Since all three components of crosstalk are present in a dynamic multiplexer, the "careful circuit board layout" is important even though it is not listed in the ACCT section.

Table 2. How to Handle Crosstalk

Crosstalk Component	Variation with f_{SIG}	Ways to Minimize Effects
Static	**6dB/octave**	• **Minimize R_{ON}** • **Reduce stray capacitance (C_{EQ}) by careful circuit board layout.**
Dynamic	**6dB/octave**	• **Minimize R_{ON}** • **Minimize f_{CLK}** • **Minimize T_{BRK}, but $T_{BRK} > 0$ is needed to prevent shorting channels together.** • **Minimize R_L** • **Reduce stray capacitance (C_{EQ}) by careful circuit board layout.**
Adjacent Channel	**NONE**	• **Minimize R_{ON}** • **Minimize f_{CLK}** • **Minimize T_{BRK}, but $T_{BRK} > 0$ is needed to prevent shorting channels together.** • **Minimize R_L and C_L** • **WAIT before allowing sample/hold or DEMUX to measure MUX output.**

This paper has pointed out the fact that static crosstalk (given on multiplexer data sheets) is only **one** of the **three** components of crosstalk. The models for static and dynamic crosstalk are relatively simple and were discussed to show how they are related. The most troublesome component of crosstalk (adjacent channel crosstalk) was shown not to be quite so straight-forward. For one thing, adjacent channel crosstalk (ACCT) is **not signal frequency dependent** as are CT and DCT. The mechanism which governs this form of crosstalk is stored charge on the MUX node. While CT and DCT must be minimized by careful layout and once present in the multiplexer cannot be reduced, such is not the case with ACCT. Even though ACCT is present in the multiplexer, the proper timing of demultiplexer or sample/hold commands can effectively eliminate ACCT from the total system.

PMI

AN-36
DAC-08 CONTROL OF 555 TIMERS

Precision Monolithics Inc.

APPLICATION NOTE 36

INTRODUCTION

This application note describes a digitally or microprocessor controlled one-shot and an astable multivibrator using two of the industry's most widely used low cost building blocks, the PMI DAC-08 8 bit DAC and the 555 timer. Digital control ranges of 255 to 1 and 510 to 1 are shown for one-shot and astable applications allowing periods of 18μsec to 1.4 seconds and frequencies of 1 Hz to 60 KHz. The circuit is presented in Figure 1.

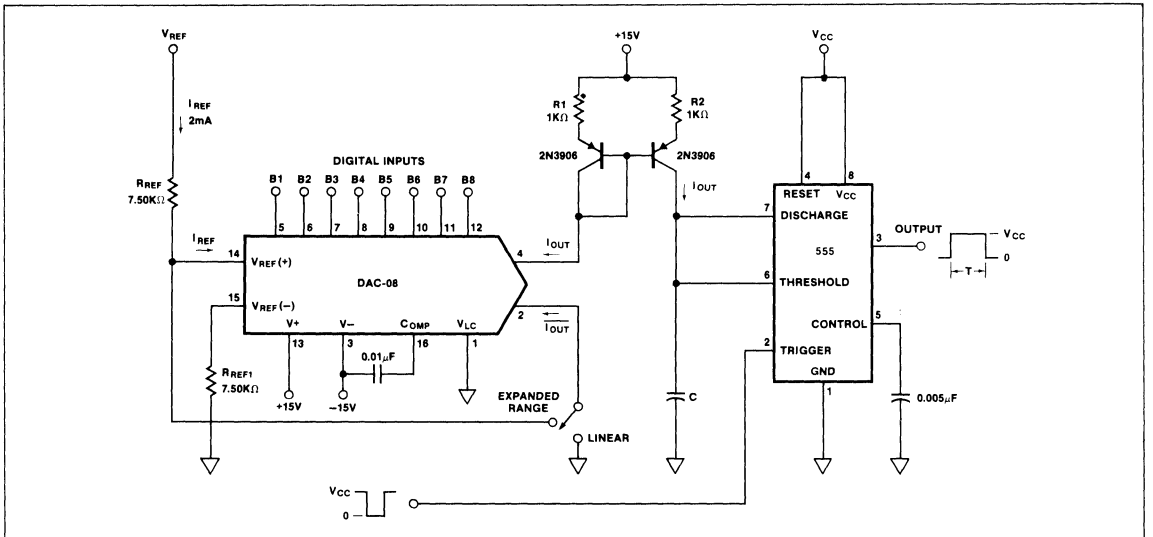
ONE-SHOT LINEAR MODE OPERATION

In the one-shot mode of operation, the time delay or the one-shot period is determined by a constant current source and a capacitor. A digitally programmable constant current source is made using the DAC-08 and two PNP transistors. The DAC-08 is a current sink; the two PNP transistors are used as a current mirror which reverses the direction of the DAC's sink current forming a current source. The current source charges the timing capacitor C, causing the voltage across the capacitor to increase linearly at the rate of $\left(\frac{I_{OUT}}{C}\right)$ volts per second from approximately zero volts to $\frac{2}{3}$ V_{CC} of the 555 timer.

The one-shot's period, T, is basically an RC product with two other control factors. The R is fixed and represented by R_{REF} which sets up the correct I_{REF} current for the DAC. With the fixed R_{REF}, the one-shot period is directly proportional to the value of the timing capacitor C (see Table 1). The other two controlling factors are the DAC's digital inputs and the ratio of the timer's V_{CC} to the DAC's V_{REF}. The one-shot period is inversely proportional to the normalized digital input value and directly proportional to the V_{CC} to V_{REF} ratio as illustrated in Fig. 2. When operated in the linear mode, a 255 to 1 control range of the one-shot's period is achieved.

BASIC DESIGN

As shown in Fig. 1, this design involves a series of conversions from a digital input to an analog current to a threshold voltage and finally to a time delay or a frequency. A DAC-08 converts the digital input to an analog current



$$\text{ONE-SHOT PERIOD, } T = \frac{2}{3} \frac{R_{REF}C}{D} \frac{V_{CC}}{V_{REF}} \text{ FOR LINEAR MODE, D = NORMALIZED DIGITAL CODE INPUT}$$

$$\text{ONE-SHOT PERIOD, } T = \frac{2}{3} R_{REF}C \frac{V_{CC}}{V_{REF}} \left[\frac{2-D}{D}\right] \text{ FOR EXPANDED MODE}$$

Figure 1. Digitally Controlled One-Shot

Table 1. One-Shot Linear Mode Timing Table

	ONE-SHOT PERIOD (ms)					
	V_{CC} = 15, V_{REF} = 15V			V_{CC} = 5V, V_{REF} = 15V		
Input Digital Code	C = 1μF	C = 0.1μF	C = 0.01μF	C = 1μF	C = 0.1μF	C = 0.01μF
11 11 11 11	5.2	0.505	0.049	1.72	0.160	0.0176
00 00 00 01	1440	134	13.8	455	43	4.8

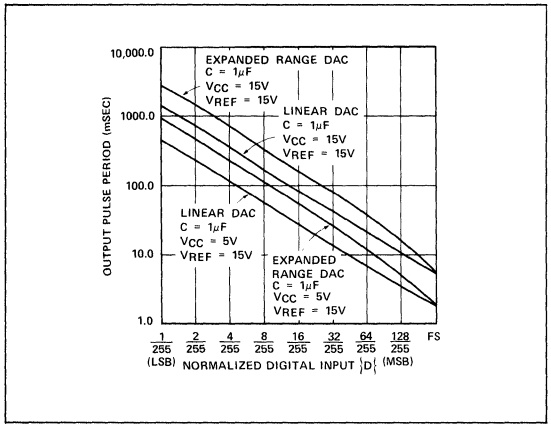


Figure 2. One-Shot Period vs Digital Input

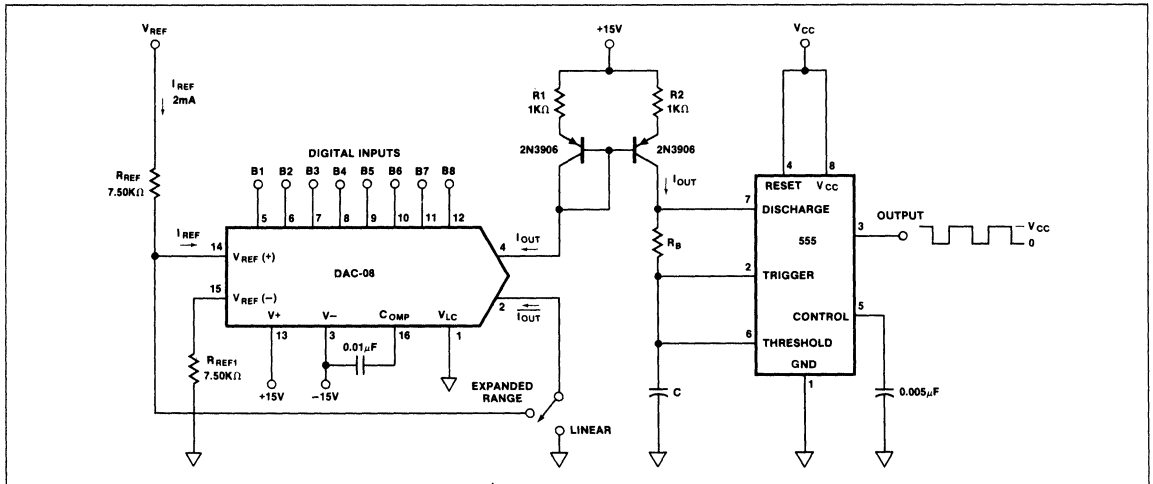
which is then converted to a voltage by a two transistor current source and a capacitor. The voltage is then converted to a time delay or frequency by a timing capacitor and the 555 timer.

ONE-SHOT EXPANDED MODE OPERATION

Range is doubled to 510 to 1 by operating the DAC in the expanded range mode with the DAC's I_{OUT} fed forward from the reference input node of the DAC. Expanded range mode timing is shown in Table 2 and in the graph of Fig. 2.

ASTABLE MODE OPERATION

An astable multivibrator is made in a similar fashion in Fig. 3. A DAC-08 and two PNP's form a current source driving the timing capacitor (C) and a discharge resistor (R_B). The timing capacitor is charged linearly by the current source and discharged exponentially through R_B. Once again, the



$$\text{FREQUENCY, } f = \frac{1}{\frac{1}{3}\frac{R_{REF}C}{D}\frac{V_{CC}}{V_{REF}} + 0.695\,R_BC} \quad \text{FOR LINEAR MODE}$$

$$\text{FREQUENCY, } f = \frac{1}{\frac{1}{3}R_{REF}C\frac{V_{CC}}{V_{REF}}\left[\frac{2-D}{D}\right] + 0.695\,R_BC} \quad \text{FOR EXPANDED MODE}$$

Figure 3. Digitally Controlled Astable Multivibrator

digital DAC input and the ratio of the timer V_{CC} to the DAC's V_{REF} provide additional control on the multivibrator's frequency. The digital input has directly proportional control while the V_{CC} to V_{REF} ratio has an inversely proportional control of frequency.

Frequency range is not fully 255 to 1 as expected but approximately 220 to 1, because the discharge time (output low) of a cycle is invariable for any digital input being determined by the product of R_B and C. Frequency is shown in Table 3 and in Fig. 4. Expanded range operation doubles frequency range as it did in the one-shot application. Frequency is shown in Table 4.

MICROPROCESSOR CONTROL

Both the one-shot and the astable multivibrator can be microprocessor controlled. Fig. 5 shows the implementation of a microprocessor controlled one-shot. The eight bit latch (74LS377) is used to interface between the data bus and the DAC. Stable data is latched in by a positive going edge of an address coincident pulse. After the data is latched, a buffered negative going address coincident pulse can be used to trigger the one-shot. The astable multivibrator is implimented similarily except for elimination of the buffer and the trigger pulses which are not required.

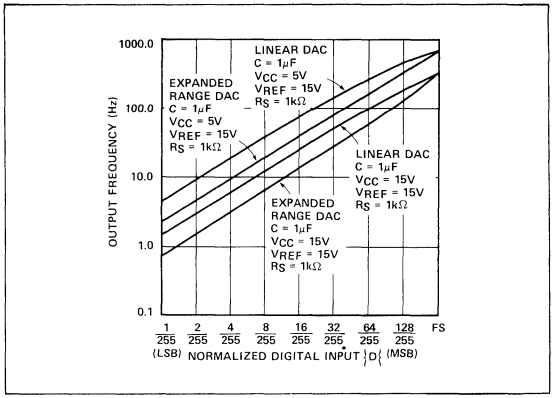


Figure 4. Multivibrator Frequency vs Digital Input

CONCLUSION

Digitally controlled one-shot and astable multivibrator with a wide range of outputs have been implemented. The one-shot has a 255 to 1 (8 Bit dynamic) time period range and the astable multivibrator a 220 to 1 frequency range. When the DAC is operated in the expanded modes, these ranges are doubled.

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Table 2. One-Shot Expanded Mode Timing Table

	ONE-SHOT PERIOD (ms)					
	V_{CC} = 15V, V_{REF} = 15V			V_{CC} = 5V, V_{REF} = 15V		
Input Digital Code	C = 1μF	C = 0.1μF	C = 0.01μF	C = 1μF	C = 0.1μF	C = 0.01μF
11 11 11 11	5.2	0.495	0.049	1.72	0.160	0.0176
00 00 00 01	2900	280	26	970	87	8.4

Table 3. Astable Linear Mode Frequency Table

	ASTABLE MULTIVIBRATOR FREQUENCY (Hz)					
	R_B = 1kΩ, V_{CC} = 15V, V_{REF} = 15V			R_B = 1kΩ, V_{CC} = 5V, V_{REF} = 15V		
Input Digital Code	C = 1μF	C = 0.1μF	C = 0.01μF	C = 1μF	C = 0.1μF	C = 0.01μF
00 00 00 01	1.49	14.7	156	4.86	49.8	433
11 11 11 11	328	3,279	33,333	717	7,273	60,241

Table 4. Astable Expanded Mode Frequency Table

	ASTABLE MULTIVIBRATOR FREQUENCY (Hz)					
	R_B = 1kΩ, V_{CC} = 15V, V_{REF} = 15V			R_B = 1kΩ, V_{CC} = 5V, V_{REF} = 10V		
Input Digital Code	C = 1μF	C = 0.10μF	C = 0.01μF	C = 1μF	C = 0.1μF	C = 0.01μF
00 00 00 01	0.74	7.69	79.9	2.42	24.7	217
11 11 11 11	328	3,279	33,333	714	7,299	60,241

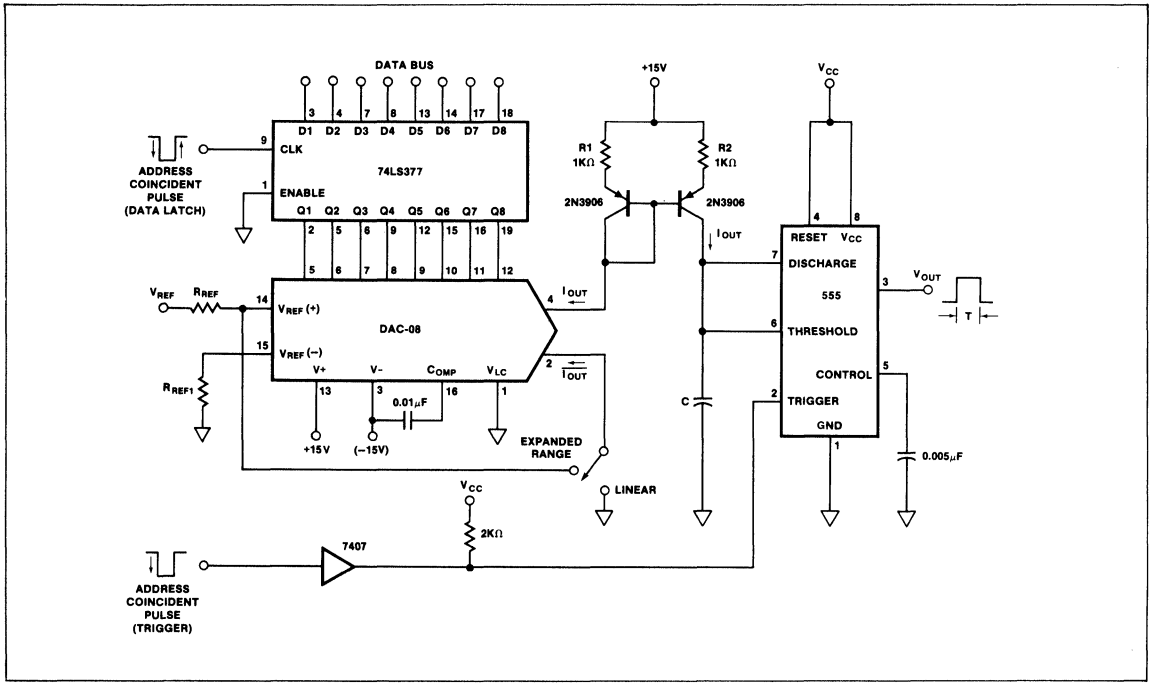


Figure 5. Microprocessor Controlled One-Shot

Precision Monolithics Inc. has developed a CODEC system for the purpose of demonstrating its use in a shared-channel system. These circuits provide a working digital transmission system incorporating eight analog input channels digitally interfacing to eight output channels. The circuit design was completed so that a single analog printed circuit board could be used either for encoding eight channels or decoding eight channels. A single digital timing and interface board is used to provide system clocks and the parallel digital data bus from transmitter to receiver. The design uses pluggable connections so that, if desired, the encoding portion or the decoding portion of the system can be tested separately. The user need only provide three voltage supplies (±15VDC, +5VDC), the appropriate filters and any applicable transmission test equipment.

HARDWARE

The entire eight-channel system consists of twenty-one integrated circuits mounted on three printed circuit boards. Two of the boards, as mentioned, are a common layout which is used for the analog functions of the system. The analog board used for the encoder (analog-to-digital conversion) requires the addition of a COMDAC® (DAC-86, 89), a MUX-88, a SMP-81, a CMP-01, and a REF-02. The other analog board is used for the decoder (digital-to-analog conversion) with the addition of a DAC-86, MUX-88, REF-02, and an OP-16. The general schematic and parts list for the analog boards are shown in Figures 1 and 2.

The control board is a TTL circuit of twelve devices designed to provide three basic functions: a) the seccessive approximation register with interface circuit to the DAC-86, b) the

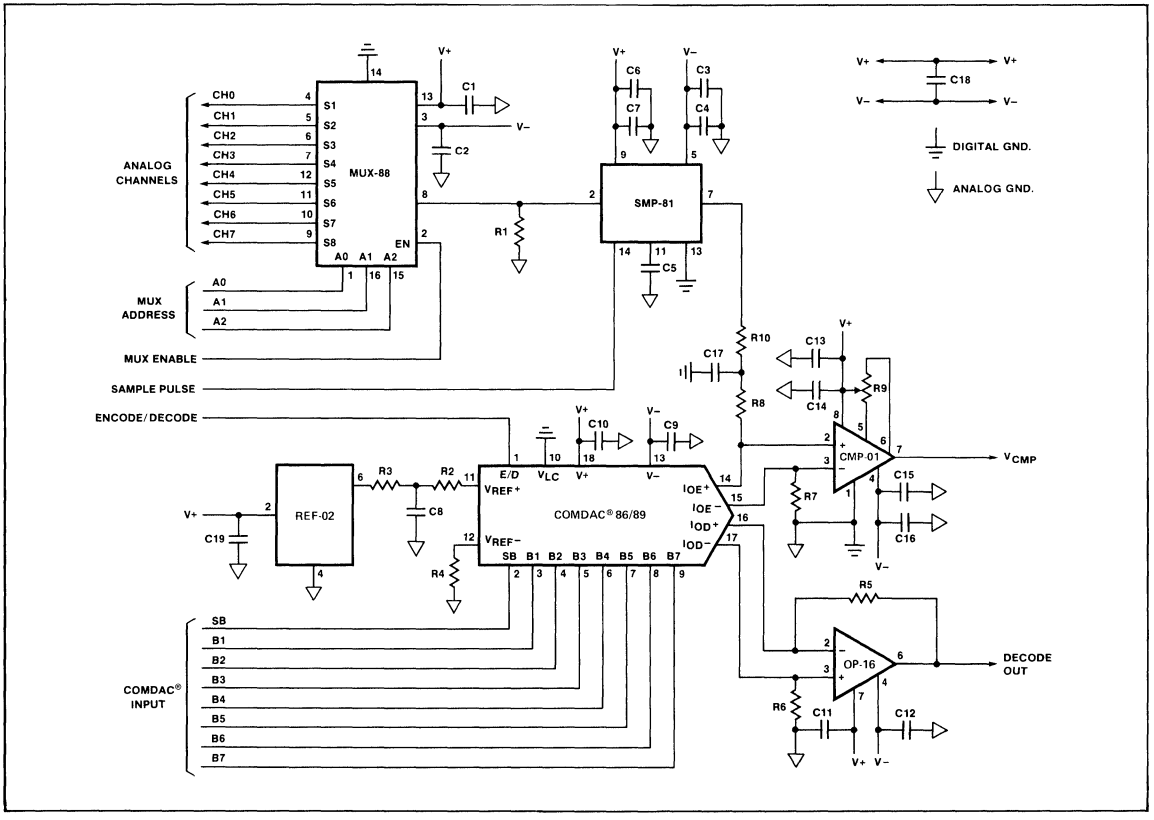


Figure 1. COMDAC® Encoder/Decoder Analog Circuit Board

TRANSMIT (Eight-Channel Encoder)	RECEIVE (Eight-Channel Decoder)
MUX-88	MUX-88
SMP-81FY	COMDAC® DAC-86EX (89)
COMDAC® DAC-86EX (89)	OP-16F
CMP-01EJ	REF-02
REF-02	

RESISTORS

R1 — 20kΩ	R6 — 2.49kΩ
R2 — 330Ω	R7 — 2.49kΩ
R3 — 9.1kΩ	R8 — 1.5kΩ
R4 — 10kΩ	R9 — 2kΩ (POT)
R5 — 2.49kΩ	R10 — 1.0kΩ

CAPACITORS

C1, C2, C4, C7, C8, C9, C10, C11, C12, C13, C15, C18, C19	0.1μF
C3, C6, C14, C16	10μF
C5	5000pF
C17	100pF

Figure 2. Parts List — Analog Board

clock for the encoder circuit, and c) the digital interface between the encode and decode sections. The encoder clock design is a multiple frequency clock, the usefulness of which is treated in a later section, generated from a programmable read-only memory frequency divider. The PROM was used to provide flexibility in changing the clock waveforms if the user so wishes. The resultant clock waveforms are also described later; the circuit schematic is shown in Figures 3a and 3b. The PROM data is listed in Figure 4. The digital interface is provided by using a standard 8-bit, parallel-in, parallel-out latch updated as the successive approximation process is completed for each input channel. The remainder of the circuit consists of the SAR and the multiplexer address counters. A parts list for the circuit is shown in Figure 5. A complete circuit schematic for the digital board is shown in Appendix A.

The boards are interconnected by use of four mini-dip connectors and cables, a 16-pin and 14-pin from each analog board to the controller. The lead designations of the two connectors are shown in Figure 6. The input and output channels are accessible through "banana"-type plugs; this allows optional connections from the transmission line in order to try different types of filters and line interface circuits. The two analog boards require ±15VDC and "banana" plugs are provided to interface to the appropriate supplies. The control board requires +5VDC only. The entire system layout is shown in block diagram in Figure 7.

SYSTEM OPERATION AND DESIGN

To achieve a workable system configuration, the encoding and decoding operations were approached as two separate designs. The entire transmission link was then connected to complete the end-to-end tests.

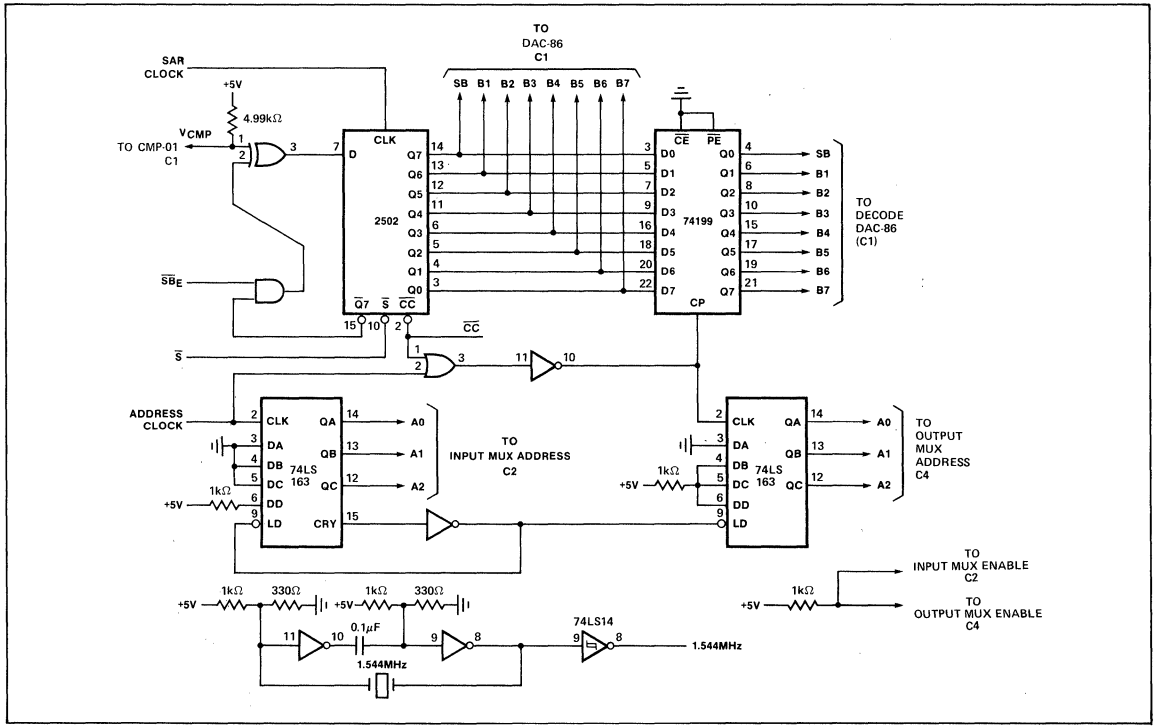


Figure 3A. Encoder/Decoder Controller

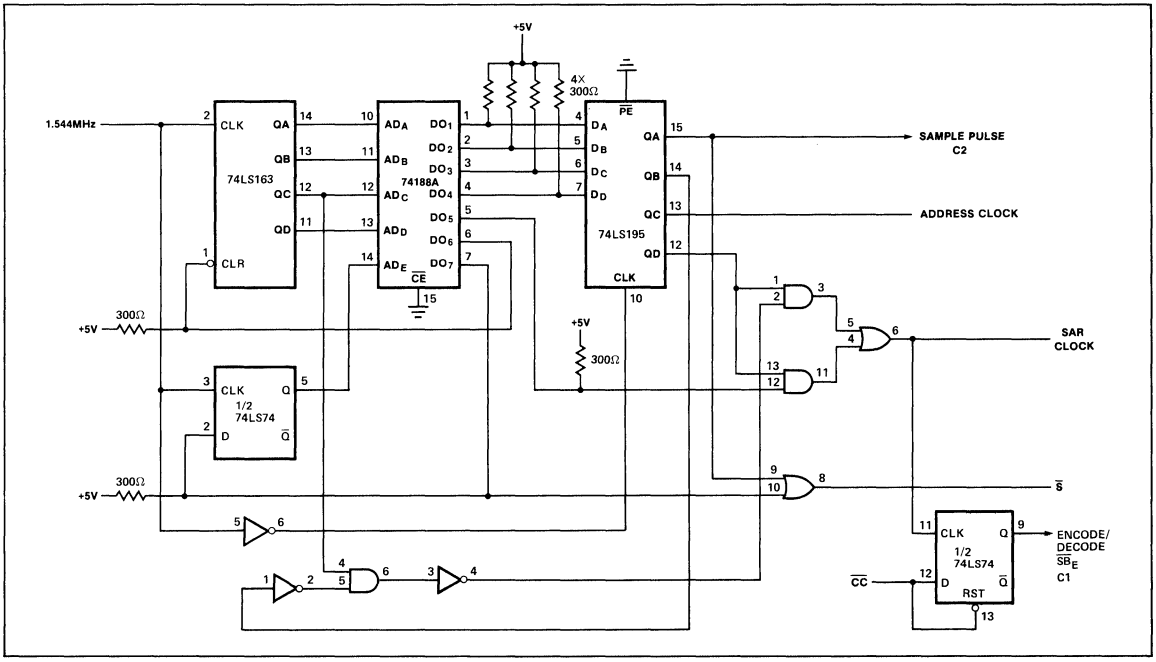


Figure 3B. Encode Clock

ADDRESS	DATA (MSB—LSB)	ADDRESS	DATA (MSB—LSB)
00	20	0C	27
01	28	0D	27
02	20	0E	2F
03	21	0F	6F
04	39	10	67
05	2B	11	67
06	23	12	6F
07	2B	13	6F
08	23	14	67
09	2B	15	67
0A	23	16	6E
0B	2F	17	0E

MSB = $D0_8$
LSB = $D0_1$
Address 18 — 1F — Unused.

Figure 4. PROM-Based Clock

PARTS			
74LS04	2	74LS163	3
74LS08	1	74188A	1
74LS14	1	74LS195	1
74LS32	1	74199	1
74LS74	1	2502	1
74LS86	1	1.544MHz Crystal	

Figure 5. Parts List — Controller

CONNECTORS		
PIN #	C1 (C3)	C2 (C4)
1	+5	+5 GND
2	+5	Sample Pulse
3	+5	MUX Enable
4	VC MP	A0 — Address
5	+5 GND	+5 GND
6	+5 GND	A2 — MUX Address
7	+5 GND	A1 — MUX Address
8	B7 — LSB	+5 GND
9	B6	+5 GND
10	B5	+5 GND
11	B4	+5 GND
12	B3	+5 GND
13	B2	+5 GND
14	B1	+5 GND
15	SB — MSB	+5 GND
16	Encode/Decode	+5 GND

*C2 is 14 Pin — C1 is 16 Pin

Figure 6. Pin Designations — System Connectors

The accuracy of the encoder, the analog-to-digital converter, is dependent upon several factors. The first, and most significant, is the speed (settling time) of the companding DAC in conjunction with the comparator. Other factors are switching time of the multiplexer, acquisition time of the sample-and-hold, hold-step settling time of the sample-and-hold, and output noise of the sample-and-hold and

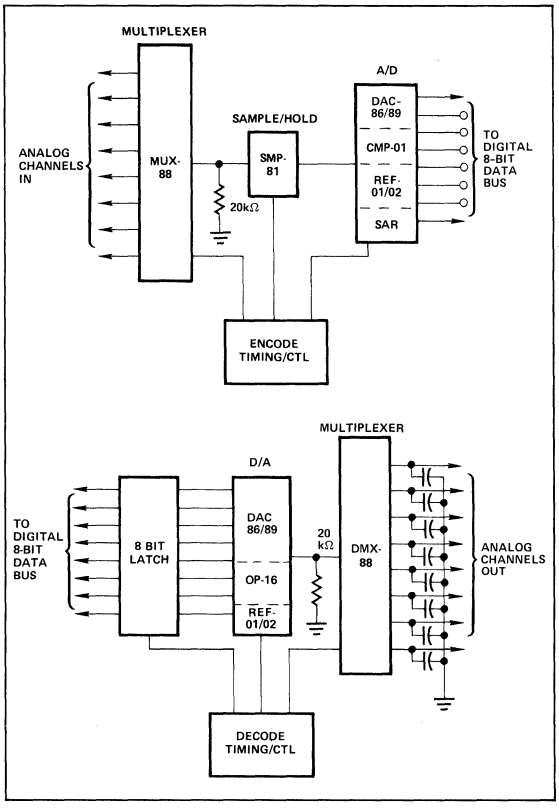


Figure 7. Eight-Channel System Layout

multiplexer. All of these characteristics had to be considered while developing the encoder circuit.

In a companded A/D conversion, using a successive approximation method, different digital bits require different settling times. There is a constant increase in the settling time required as one goes from the sign bit to the chord bits and then to the step bits. This increase in settling time is partially caused by the scaled current sources used to design a companding D/A and is most affected by the magnitude of the voltage level being converted. So as the output currents of the DAC-86 become smaller (at smaller voltage levels), the comparator is less responsive. Also as the less significant bits are clocked in, the situation becomes more critical since progressively smaller current changes are provided to force the comparator to change output state. The encoder clock waveforms, shown in Figure 8, depict a system approach to accommodate these timing characteristics. The governing design criteria was that a limited amount of time is available to complete the successive approximation of the analog signal (for eight channels, with a sampling frequency of 8kHz, this means 15.6μs) and the optimum clock must fit within this period. All functions (including sampling, encoding, switching) must therefore be completed with an acceptable accuracy, within this time constraint. To achieve accurate data acquisition with the sample-and-hold, a sam-

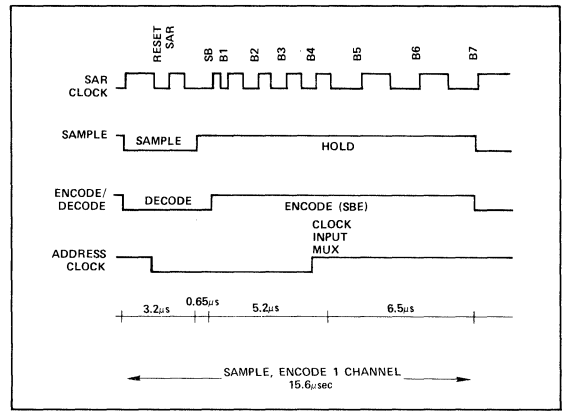


Figure 8. Encoder Timing Waveforms

ple pulse of 3.2μs was used. Once the pulse goes from sample to hold, there is a waiting time required to allow the sample-and-hold output to settle to the "held" value, 650ns is the time added. Since the sign bit is the fastest transition, the basic system clock (1.544MHz) is used for the first SAR clock period. The clock frequency is then halved to clock in the chord bits (B1, B2, B3), the next "slowest" transitions. Finally, the clock frequency is halved again to allow for the step bits (B4-B7), a frequency of 386kHz. The times required for the different bit conversions are shown in Figure 8. The SAR is reset during the sampling period and once the sample circuit has entered the hold mode, the input multiplexer's address is changed. This provides ample time for the MUX to switch to the next analog input with little effect on the adjacent waveforms. In addition, to further minimize interchannel crosstalk, a 20kΩ resistor to ground is added to the multiplexer output.

To provide sufficient noise immunity from the sample-and-hold to the comparator, a simple filtering circuit using a 100pF capacitor is added. A 4.9kΩ resistor to +5V from the comparator output aids in increasing the DAC-86 and comparator speed. In order to test the encoder without adding a decoder, a high-precision voltage source (DC levels) was used as an input to one or more channels of the A/D circuit. The data output (one byte every 15.6μs) was sampled and stored in a logic analyzer. By reviewing the samples for each channel, and comparing the data from all channels of the eight channel system, the effects of changes in the clock on the accuracy of the design could be observed. By inputting a steady-state value, the data out would not only demonstrate the "consistency" of the A/D conversion but also make obvious any adjacent channel effects that were produced.

The analyzer sampling also presents a method of initializing the system components. By grounding all inputs and digitally sampling the data bus output, the zero level can be set so as to produce an alternating series of data bytes equivalent to 0 volts (10000000 and 00000000).

A similar design approach was used in developing an eight-channel decoder. In this case, the response time of the DAC-86 and op amp offers little problem since an eight-

channel decoder is relatively slow. However, the accuracy of the devices does become important. The design considerations become, therefore, the nonlinearity of the DAC-86 in conjunction with the switching time and charge injection of the multiplexer. The DAC-86 is manufactured to strict linear specifications, which assures both excellent decoding linearity and absolute accuracy. The multiplexer is used both as a switch to demultiplex the output waveforms and as a holding circuit by adding capacitance to the output leads. One effect seen in the multiplexer is that as a channel is switched off, there is a charge injected onto the output. This charge is not normally obvious in a MUX design, however, when working into a high impedance (such as a filter) and with capacitors on the source leads (outputs), the charge can add an offset to the waveform. To minimize the effect, a large capacitor (0.1μF or greater) is added. Since the charge pulse is a short duration signal, the signal on the larger capacitor will be less affected by the charge than if a smaller component was used.

In terms of a system decoder design, this circuit could be used for more than eight channels. The op amp and DAC-86 are both capable of responding to more output channels. An eight-channel system was incorporated to remain compatible with the analog board that is used in the demonstrator. In order to decode more channels (>12), the output capacitance on the demultiplexer would need to be reduced. The other circuit components would remain the same.

The decoding circuitry can be tested separately by adding a series of data bytes and monitoring the output channels. The CCITT recommendation for testing PCM systems includes a method of testing a decoder by introducing a standard sequence of digital data words in order to produce a 1kHz sinusoid at a nominal level of 0dBm0.* This method proved useful in "debugging" the circuit design prior to attempting the end-to-end tests.

SYSTEM TESTS

Once the encoder and decoder were functioning separately, the entire system was connected with the appropriate interfacing to allow for full-system transmission tests. The measurements taken were the standard set of PCM specifications observed in the majority of data sheets for telecommunication oriented products. These tests included signal-to-total distortion, gain tracking, intelligible crosstalk, and idle channel noise.

There are two different methods of performing the tests. For the U.S. standards, a sinusoid signal is used as the channel input and the measurements are taken around the base (test) frequency. For the European tests, a pseudo-random or "white" noise source is preferred as the input signal. The test results discussed here were obtained with the U.S. testing procedures; similar test results have been achieved using European test methods.

The test set-up for signal-to-total distortion and gain tracking measurements is shown in Figure 9. The results are plotted in Figures 10 and 11. As is seen, each test was performed with both the C-Message Weighting and the 3kHz Flat response terminating configurations. The results using the μ-law parts (DAC-86) are represented. In terms of signal-to-total distortion, the system exceeds the recommended standard at all input levels by 2dB or greater. The system is also well within the recommended gain tracking limits for both terminations.

The crosstalk and idle channel noise measurements are given in Figure 12. One consideration of the system design, in terms of performance, was that the most difficult characteristic for a shared-channel system to minimize is the intelligible crosstalk specification. The design is directed

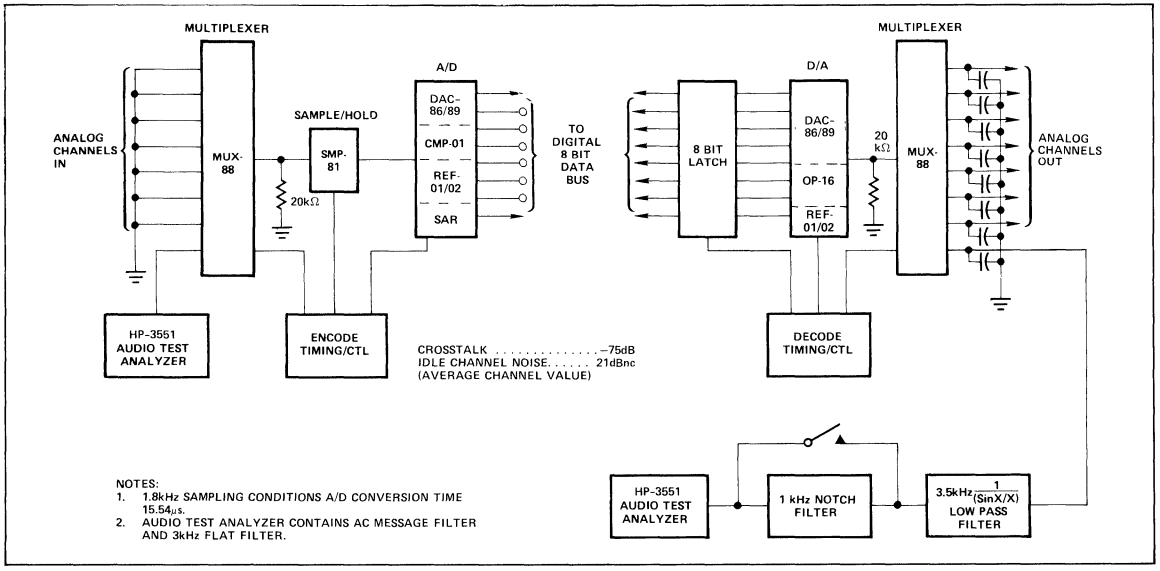


Figure 9. Eight-Channel Test Configuration

*Reference — CCITT Sixth Plenary Assembly (1976), Orange Book Vol. III-2

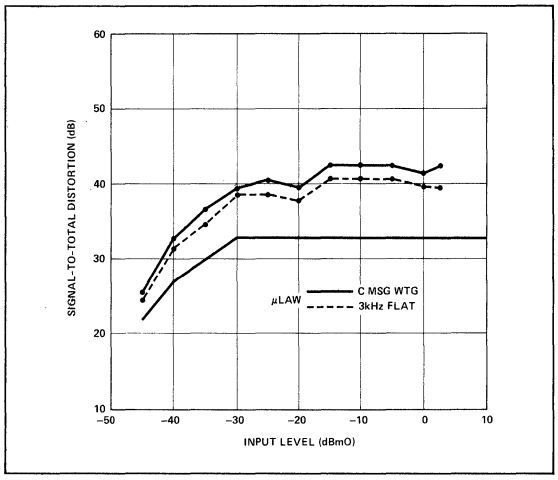


Figure 10. Signal-To-Quantizing Distortion vs. Input Level

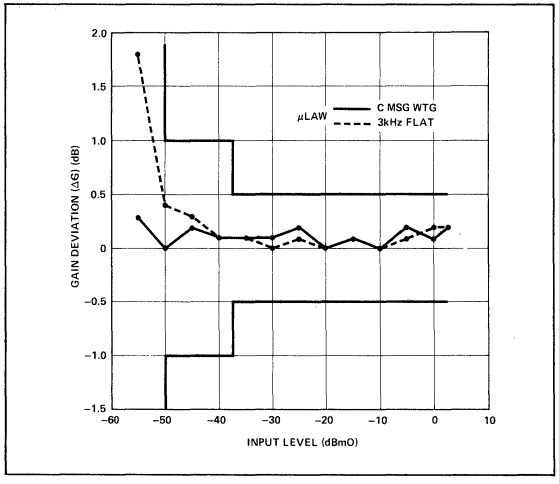


Figure 11. Gain Tracking

IDLE CHANNEL NOISE

CHANNEL	NOISE (dBm0)	CHANNEL	NOISE (dBm0)
1	−66.9	5	−62.6
2	−67.6	6	−65.3
3	−67.0	7	−67.0
4	−67.2	8	−61.8

CROSSTALK

FREQUENCY	INTELLIGIBLE CROSSTALK
300 — 2900Hz	≤ −78dBm0
2900 — 3400Hz	≤ −70dBm0

Figure 12. Idle Channel Noise and Crosstalk

toward optimizing this measurement. The idle channel noise is at the system recommended level when measured without output filtering. It is further reduced by adding a PCM receive filter on the decoder multiplexer.

CONCLUSIONS

The circuitry just discussed is meant to represent one approach to designing an eight-channel, shared CODEC system. It is not meant to be the only design, but provides a working system upon which to base further engineering development. It should be noted that in terms of transmission testing, the design is an end-to-end system. The configuration presents the users with a complete circuit enabling them to observe the individual device characteristics significant in producing a shared-channel design.

The design provides a starting point from which most characteristics important to both shared-channel and single-channel designs can be manipulated to allow for improvements in transmission quality. To be able to develop a realistic transmission design, the system engineer needs to consider more than just the coder/decoder devices. A complete multiple-channel system, such as the one presented here, allows the user to observe the complete system performance as it is affected by the individual system components.

APPENDIX A

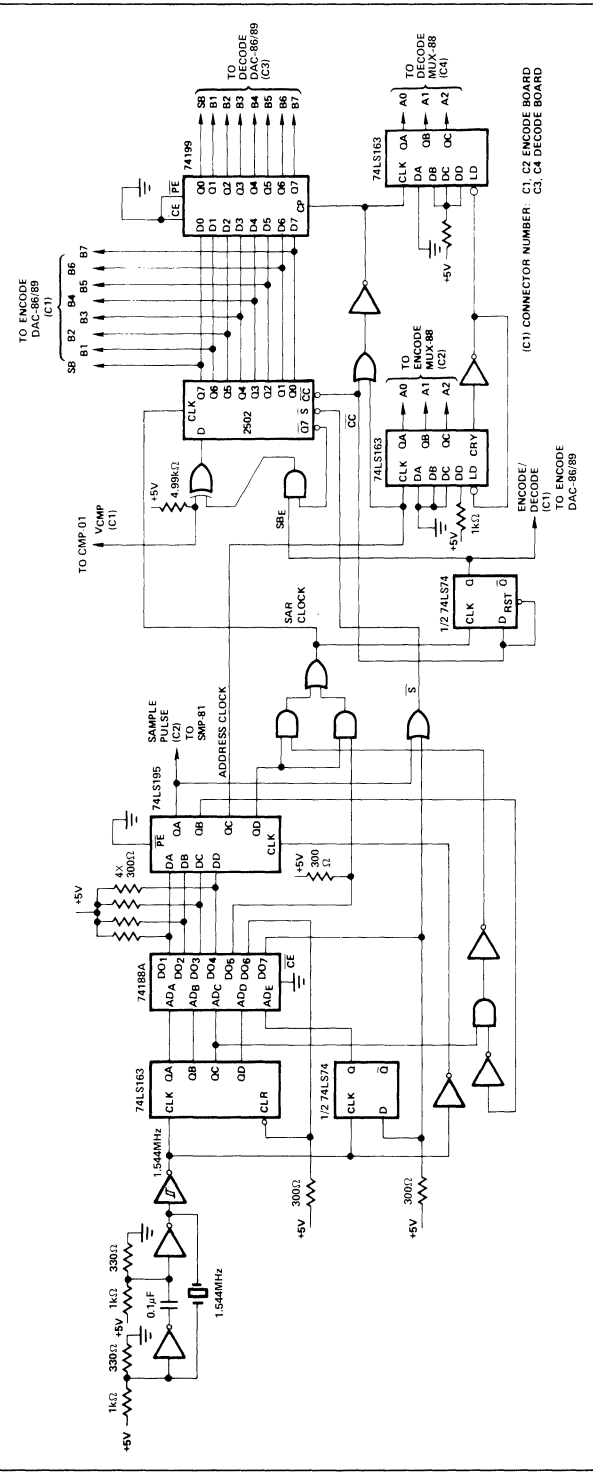


Figure A-1. Circuit Schematic

APPLICATION NOTE 38

FOUR-CHANNEL SHARED CODEC

A four-channel CODEC assembled from LSI components is a cost-effective digital transmission system requiring a relatively small number of devices. The system makes use of a single COMDAC® companded DAC-86 or DAC-89 digital-to-analog converter for both encoding and decoding (see Figure 1). The timing of the circuitry is compatible with ATT and CCITT system specifications.

Each channel is sampled at the standard 8kHz rate. With four channels this allows approximately 31.2μs to encode the sampled analog input and to decode the received digital signal for the same channel. To simplify the timing system requirements equal amounts of time were allowed for encoding and decoding, thus permitting 15.6μs for the more critical encode portion of the cycle. The encode/decode clocking scheme for this CODEC was incorporated directly from a successful eight-channel CODEC system which has been published as PMI Application Note 37. One original feature of the four-channel design was the use of dual eight-channel multiplexer ICs to switch the four channels. This results in a system whose interchannel crosstalk is practically negligible. Crosstalk figures of −85dB have been observed. This article describes the design procedure and reviews the transmission characteristics of the completed system.

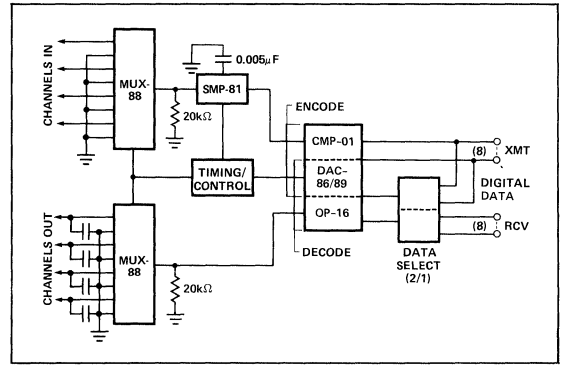


Figure 1. Four-Channel CODEC

CIRCUIT DESIGN

The analog circuitry required for a four-channel system is shown in Figure 2. The circuit uses the same printed circuit card as the transmit or receive sections of the eight-channel CODEC design (with the addition of a second multiplexer). The analog inputs all connect at the input multiplexer(MUX-88) using alternating inputs, the output (drain) of the MUX

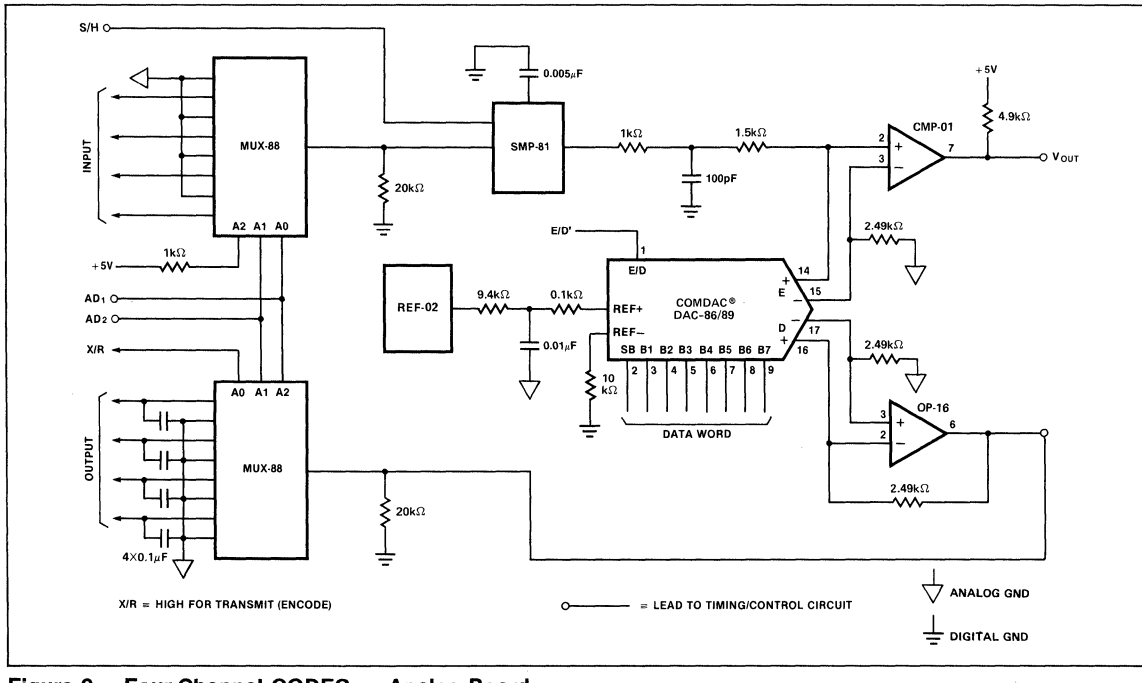


Figure 2. Four-Channel CODEC — Analog Board

drives the SMP-81 sample-and-hold device. Once the input level is held, the COMDAC® (DAC-86 or 89), in conjunction with the comparator (CMP-01), begins the analog-to-digital conversion sequence. A successive approximation encode procedure is used; this generates, within the allotted conversion time (15.6μs), an eight-bit digital approximation of the analog level. The data byte is available at the successive approximation register output for the next 15.6μs time frame. During this time the CODEC decodes the incoming digital signals.

The decode cycle begins as soon as the encode cycle is completed. The DAC-86 is switched to the decode mode and an eight-bit data word is presented at its input leads, presumably from some distant analog-to-digital converter through a switching matrix. As the DAC-86 is switched to decode, the operational amplifier (OP-16) converts the output current of the DAC-86 into the appropriate voltage level. The output multiplexer is switched to the proper analog port as the decode procedure is initiated. On the output leads of the "de"-multiplexer, a hold capacitor is used to provide an output holding function. The "staircase" waveform is then available for filtering and the final subcriber interface.

As shown in the Figure 2, several circuit precautions were taken to reduce the internal noise levels. Foremost among these is the ample use of grounding throughout the analog circuit. All power supply inputs to the ICs are bypassed with capacitance (0.1μF) to ground. In addition, any spare land area of the board is filled with ground paths. The various voltage return paths are kept separate except for one common location on the board at the supply input leads. For further noise protection, a 20kΩ resistor to ground is connected to the drain leads (the common output or input) of both multiplexers. This reduces the multiplexer output noise and any crosstalk voltage feedthroughs. Also, in terms of the multiplexers, the output MUX is addressed to a grounded terminal (source connection) in between the active channels. This aids in minimizing the mutiplexer injection phenomena (discussed in detail in Application Note 37, describing the eight-channel CODEC design) and helps to further reduce the device crosstalk. The significance of using two multiplexers in this design is to allow unused channels of the output MUX to be connected to ground. The active channels are then alternated, in terms of addressing, with the grounded terminals. Addressing the multiplexers requires only two of the address leads to be controlled by a binary counter for data selection. The third address input is either held active (as in the input MUX), or can follow the system transmit and receive control signal (lead X/R, as in the output MUX). The address sequence for the input MUX is repeated through ports 4 to 7 (100 to 111), the most significant bit is held high and the two lower bits are counter outputs. This scheme allows maximum settling time for the MUX since the next channel to be encoded is selected more than 16μs prior to the conversion. For the output MUX, the two **most** significant bits of the address are the counter output leads, the least significant bit is the transmit/receive lead (X/R). As is shown in Figure 3, the address sequence alternates from active output port (even addresses) to

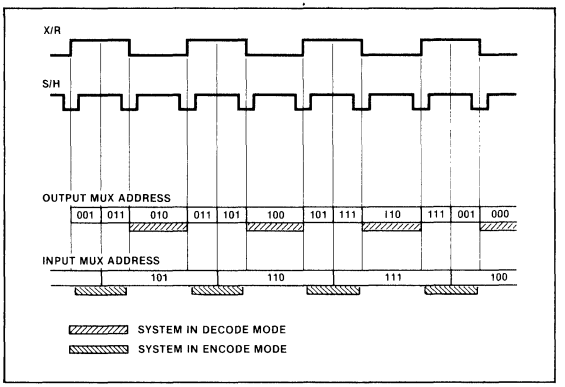


Figure 3. Four-Channel CODEC — Multiplexer Sequencing

grounded ports (odd addresses). The counter is changed while the MUX is selecting an unused (grounded) channel. This type of sequencing reduces the interchannel interference of the MUX and greatly adds to the system's measured performance.

To minimize sample-and-hold noise, a simple filter circuit is added to the output terminal of the device. A similar approach was used in the eight-channel design. Another feature in common with the eight-channel system is the use of a 4.9kΩ resistor pull-up from +5V to the output of the comparator; this decreases the switching time of the device for the encode procedure.

The timing waveforms generated for the four-channel system are based on the encoder clock used in the eight-channel CODEC. This clock circuit is shown in Figure 4. In a companded A/D conversion, using a successive approximation method, different digital bits require different settling times. There is a constant increase in the settling time required as one goes from the sign bit to the chord bits and then to the step bits. This increase in settling time is partially caused by the scaled current sources used to design a companding D/A and is most affected by the magnitude of the voltage level being converted. So that, as, the output currents of the DAC-86 become smaller (at smaller voltage levels), the comparator is less responsive. As the less significant bits are clocked in, the situation becomes more critical since progressively smaller current changes are provided to drive the comparator. A multi-frequency clock will take advantage of these timing variations; such a clocking scheme is shown in Figure 5. The governing design criteria is that a limited amount of time is available to complete the successive approximation of the analog signal and the optimum clock must fit within this period. All functions (including sampling, encoding, switching) must be completed, therefore, with an acceptable accuracy, within this time constraint. To achieve accurate data acquisition with the sample-and-hold, a sample pulse of 3.2μs was used. Once the pulse goes from sample to hold, there is a waiting time required to allow the sample-and-hold output to settle to the "held" value; 650ns is the time added. Since the sign bit is

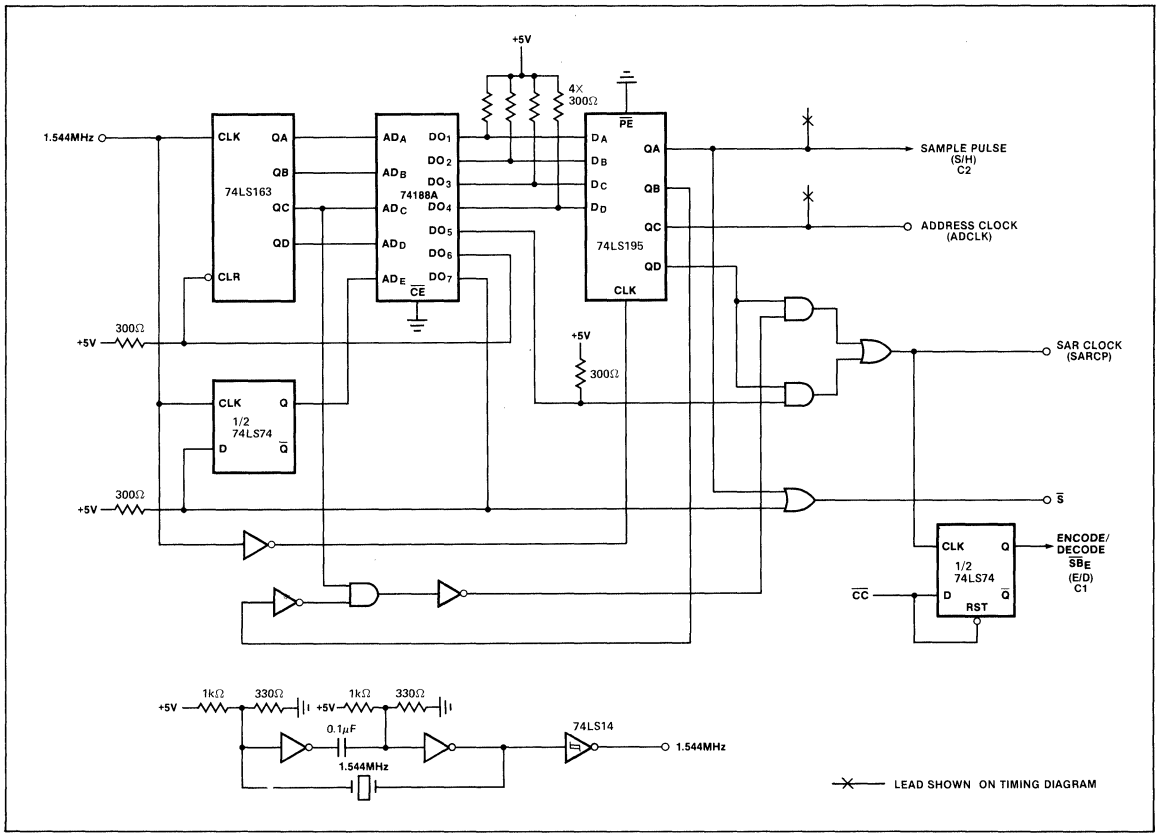


Figure 4. PROM Based System Clock

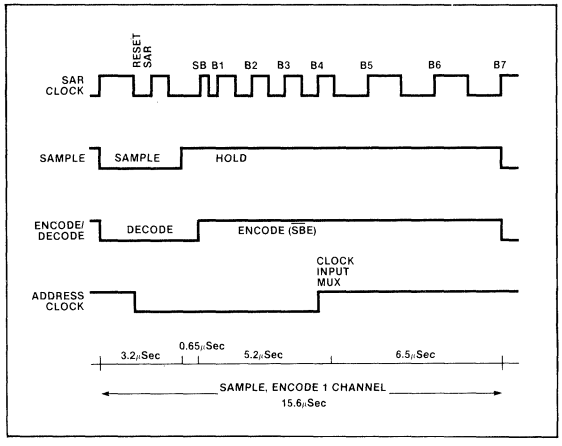


Figure 5. Four-Channel CODEC — Encoder Timing

the fastest transition, the basic system clock (1.544MHz) is used for the first SAR clock period. The clock frequency is then halved to clock in the chord bits (B1, B2, B3), the next "slowest" transitions. Finally, the clock frequency is halved again to allow for the step bits (B4-B7), a frequency of 386KHz. The SAR is reset during the sampling period and once the sample circuit has entered the hold mode, the input multiplexer's address is changed. This provides ample time for the MUX to switch to the next analog input with little effect on the adjacent waveforms.

Using this timing pattern as the starting point, the original eight-channel system was converted to a four-channel bidirectional design. The only additional control functions to be added were the timing signals needed to switch the DAC-86 between the encoding and decoding modes, to operate the output multiplexer, and to select the proper data inputs for the DAC-86. The DAC-86 mode select and the multiplexer address leads, as mentioned previously, are generated from a single system transmit/receive control (shown as X/R in Figure 6). The lead is the system monitor of the mode in which the CODEC is operating. When active (logic "1"), the DAC-86 and associated parts are in the encode mode. In the encode mode: the successive approximation register clock is enabled, the encode/decode lead to the DAC-86 (E/D) is enabled, the data input selector directs the SAR output back toward the DAC-86 for the feedback needed in successive approximation, and the output MUX connects the OP-16 to a grounded (unused) channel. The

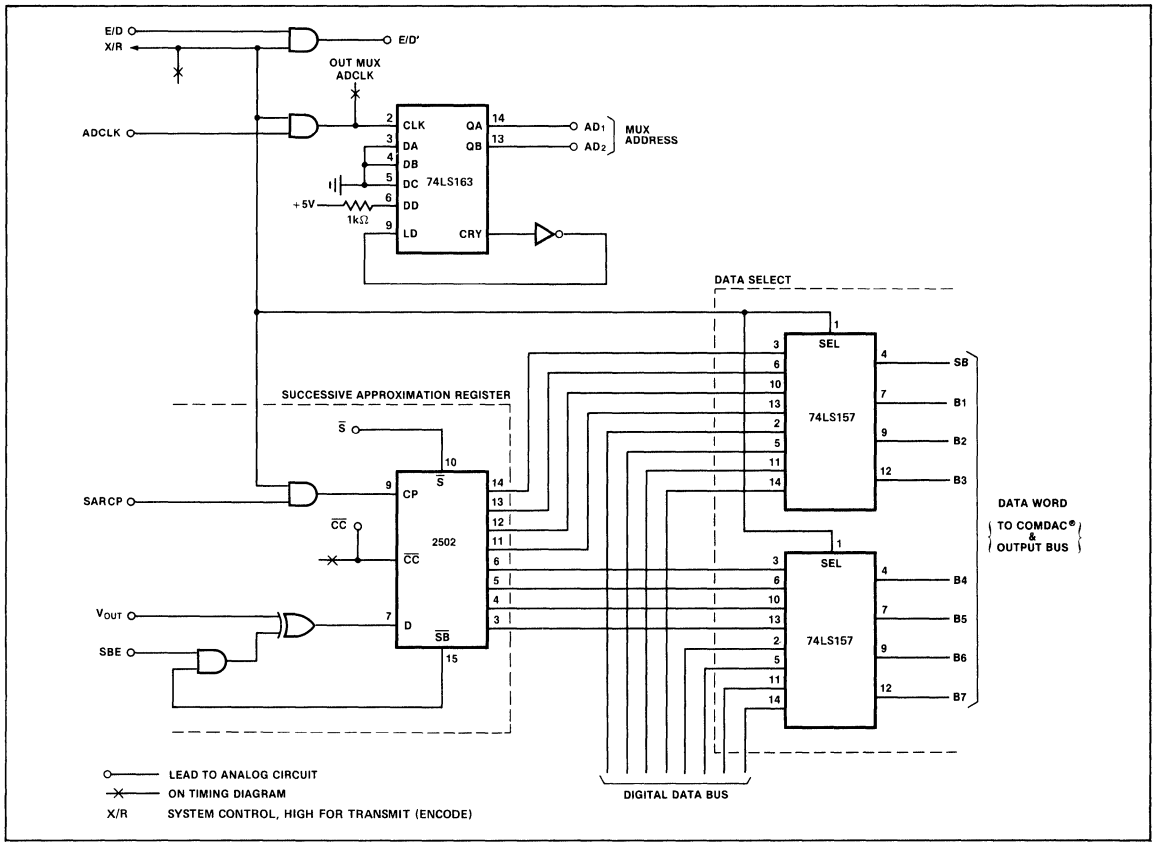


Figure 6. Four-Channel CODEC — Control Board

X/R lead remains at logic "1" until encoding is completed, then goes to ground (logic "0"), the decode state. To decode a data byte, the DAC-86 is held in the decode mode (E/D is low), the output MUX is addressed to an active output port, and the SAR clock is disabled (this register will hold the last encoded data word throughout the decode cycle — it is not cleared until a new input signal is to be encoded). The data selector is directed to the digital system bus and the decoding of the byte on the bus begins. As described, the address leads of the multiplexers are programmed such that the input MUX will always be directed toward the next active channel, once the previous analog sample has been held. But the output MUX does not connect to an active channel until the decode cycle begins; during the encode cycle only unused (grounded) ports are addressed.

SYSTEM TESTS

The system as configured in the block diagram (Figure 7) is a complete four-channel CODEC. To perform the transmission tests, it was decided to use a single CODEC circuit and transmit data in a "loopback" configuration. As was mentioned earlier, the only signal required from an external controller is the X/R lead. This is generated for the test circuit by halving the inverted ADCLK lead from the prom-based clock.

The system waveforms that result are shown in Figure 8. These clock patterns can be correlated to the encode clock waveforms in Figure 5 by comparing the ADCLK or the S/H leads. Since the successive approximation register is not

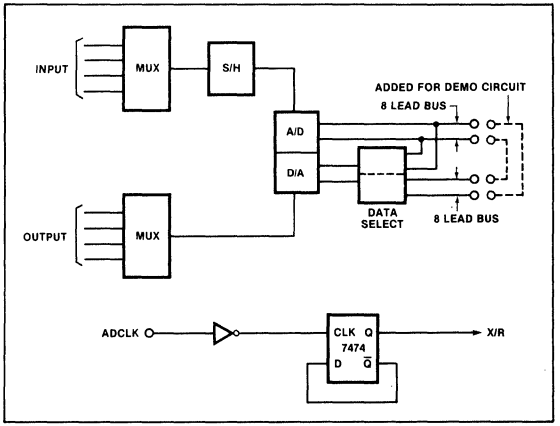


Figure 7. Four-Channel CODEC — Demonstrator Layout

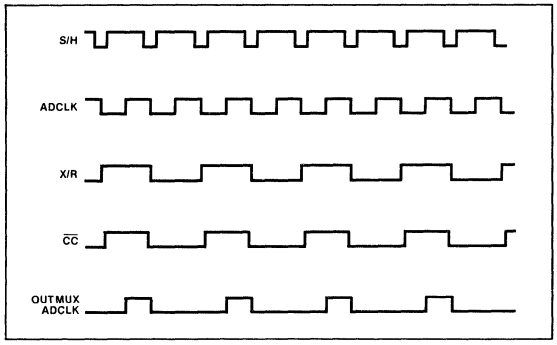


Figure 8. Four-Channel CODEC — Demonstrator Timing

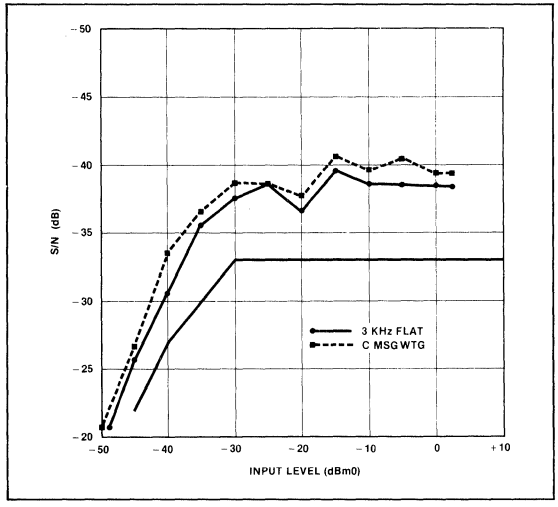


Figure 9. Signal-To-Total Distortion (Four-Channel)

cleared until after the decode cycle, an external register is not necessary to hold the data for the decoding process.

The transmission tests that were completed were the typical telephone network tests as described in the eight-channel application information. The tests include signal-to-total distortion, gain tracking, intelligible crosstalk and idle channel noise. Again the test method used for the first two tests was based on a sinusoidal input signal, as is common in the AT&T specifications, at a frequency between 400 and 3400Hz using a frequency-selective wave analyser. The results of all testing are shown in Figures 9 through 11.

It is of some interest to compare this data with the test results of the eight-channel CODEC design. In particular, the idle channel noise and the crosstalk measurements are improved. This can be partially explained by the different manipulations of the output multiplexer. This does however, tend to point to the fact that the output MUX can be a significant source of noise and cross channel interference. Further data is certainly necessary, but these results do point out an area of concentration for the system designer wanting to improve system performance.

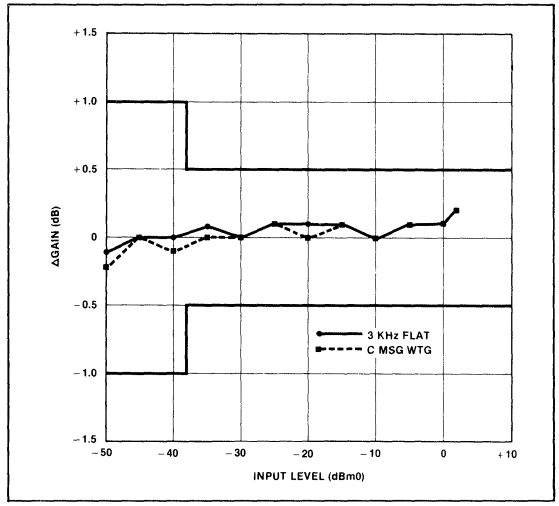


Figure 10. Gain Deviation (Four-Channel)

IDLE CHANNEL NOISE

Channel	
1	
2	no channel
3	had noise
4	level > 2dBrnc

INTELLIGIBLE CROSSTALK

f_{input}	Level
400-3400Hz	≤ −85dBmO

Figure 11. Transmission Measurements (Four-Channel)

In terms of signal-to-total distortion and gain tracking, the four-channel results compare favorably with the eight-channel data and both systems exceed the AT&T requirements. Overall, the transmission tests point out that using a single DAC-86 for four-channel transmitting and receiving is a realistic approach and can comply with all " system" standards.

CONCLUSIONS

The testing described in the preceding pages demonstrates the feasibility of encoding and decoding four channels with a single DAC-86. The system has several advantages: 1) a smaller number of devices are required to complete the CODEC function than were necessary for the eight-channel design, 2) the clock circuitry (PROM-based timing generator) is common to all encoders, so only a single such circuit is needed for multiple CODECs. Both of these factors contribute to reduced printed circuit board area for multiple transmission channels. The devices needed for a four-channel CODEC are listed in Figure 12. In terms of package sizes, only one device is larger than sixteen pins (the DAC-86/89 is 18 pins) and three of the components are only eight pins. This should make system layout fairly simple and allow relatively dense component packing. If chan-

PARTS (CODEC + CLOCK)

Analog

MUX-88 E (2)
* SMP-81 FY
* DAC-86 EX
* CMP-01 EJ
* OP-16 FJ
* REF-02 EJ

Digital

* 74LS04 (2)
* 74LS08 (2)
74LS14
74LS32
74LS74
* 74LS86
74LS157 (2)
* 74LS163 (2)
74188A
74LS195
* 2502
+1.544MHz Crystal

* Parts for CODEC

Figure 12. Four-Channel CODEC — Parts

nel monitoring is incorporated, then a single supervision circuit could administer several circuit packs in a system lineup. The number of external leads is reduced in a four-channel CODEC and the design is easily added to a bus-structure data switching system.

The price per channel is still less than that being quoted by single-channel CODEC designers although slightly more than the eight-channel approach. The sacrifice made in price-per-channel is offset by the gains in system architecture and board layout offered by a four-channel shared CODEC. The shared channel CODEC approach is a viable solution to producing a digital transmission system. AN-37 shows designs at even lower per channel cost.

INTRODUCTION

A companding digital-to-analog converter (DAC) is the key component in PCM CODEC systems. (CODEC is an acronym for coder-decoder.) A CODEC performs the coding functions which consist of an analog-to-digital conversion (ADC) of the input analog (voice) signal and decoding, which consists of a digital-to-analog conversion (DAC) of the received digital input.

The DAC is used for both encoding and decoding; it is in a feedback loop to generate the ADC functions. Voice signals in telephony require a system with a very large dynamic range. The dynamic range (DR) of a CODEC is defined as the ratio of the largest resolvable signal to the smallest signal which can be encoded. The dynamic range of the CODEC is the same as that of the DAC used in either the decode mode or in the feedback loop of the successive approximation type ADC. The dynamic range of a DAC is simply the ratio of its output for a linear input of one least significant bit (LSB) to that of the largest, all "1s," input. This ratio is usually expressed in decibels using the equation:

$$DR = 20 \log_{10} \frac{I_{MAX.}}{I_{LSB}}$$

where for a current output DAC I_{MAX} is the output current for all "1s" input and I_{LSB} is the output current for one LSB input. Using this equation a linear bit DAC can be shown to resolve a ratio of 2^n:1 therefore:

$$DR = 20 \log_{10} \frac{2^n}{1} \approx 6^n$$

The wide dynamic range requirements of a telephone system require the equivalent dynamic range of a 12-bit system or 72dB. However, this system would not be satisfactory for telephone voice transmission because of its excessive bandwidth requirements. With present day T1 type transmission systems a 64kbits/sec data rate is required to transmit each voice channel. The use of the linear system would increase this bit rate to 96kbits/sec. This would provide more accuracy than is needed at the expense of excessive bandwidth.

For voice systems the most important criterion is the signal-to-noise ratio. In a PCM system noise is due almost entirely to quantizing distortion. Thus, a non-linear DAC has a non-linear transfer characteristic to compress the analog signal into a digital word and a complementary transfer characteristic to expand the digital words into analog signals with a wide dynamic range. For a telephone system a CODEC requires a fairly uniform signal-to-distortion ratio over its entire dynamic range. Achieving this uniform signal-to-distortion ratio over a wide dynamic range requires the use of non-uniform coding. A non-uniform CODEC is a coder-decoder pair whose input amplitude range is divided into steps of unequal widths, such that the width of the quantizing steps increase in proportion to the amplitude of the signal. To achieve uniform signal to distortion performance a logarithmic transfer function is required. The word compand, (compand is an acronym for compress — expand) was borrowed from analog systems to describe this non-uniform coding system where quantizing and coding is such that step size depends on the input amplitude.

COMPANDING PRINCIPLES

Companding requirements differ for different signal distributions. As mentioned above, voice signals require constant S/D performance over a wide dynamic range. In order to accomplish this the distortion must be proportional to the signal level. This feat is best achieved by the use of a logarithmic compression law. However, a truly logarithmic assignment of code words is not physically possible since this implies an infinite number of codes. Two methods for generating practical implementations of logarithmic transfer functions have been derived which have become industry standards. These methods are generally known by their transfer functions which are called μ-law and A-law respectively. Both of these transfer functions are normally implemented with eight-bit non-linear DACs to achieve a 72dB dynamic range. This is the equivalent dynamic range of a twelve-bit linear DAC. The μ-law and the A-law transfer functions are described by the following equations:

$$\mu\text{-law} \quad Y = \frac{\ln(1 + \mu|X|)}{\ln(1 + \mu)} \operatorname{sgn} X \quad \text{for } -1 \le X \le +1$$

$$\text{A-law} \quad Y = \frac{1 + \ln A|X|}{1 + \ln A} \operatorname{sgn} X \quad \text{for } 1/A \le X \le 1$$

$$Y = \frac{A|X|}{1 + \ln A} \operatorname{sgn} X \quad \text{for } 0 \le X \le 1/A$$

These laws have unique signal-to-distortion characteristics for each value of μ and A respectively. At present ATT has settled on a value of μ equal to 255 and CCITT specifications use a value of A equal to 87.6. Substituting these constants into the original equation above obtain:

$$\mu\text{-law} \quad Y = 0.18 \ln(1 + \mu|X|) \quad \operatorname{sgn} X \text{ for } -1 \le X \le 1$$

$$\text{A-law} \quad Y = 0.18 \ln(1 + \ln|X|) \quad \operatorname{sgn} X \text{ for } 1/A \le |X| \le 1$$

$$Y = 0.18\, A|X| \quad \operatorname{sgn} X \text{ for } 0 \le |X| = 1/A$$

The wideband (unfiltered) signal-to-distortion ratio over the useable dynamic range of voice transmissions is shown in Figure 1. This plot does not represent actual system performance; it is instead, a measure of the distortion which would be caused by an ideal quantizer.

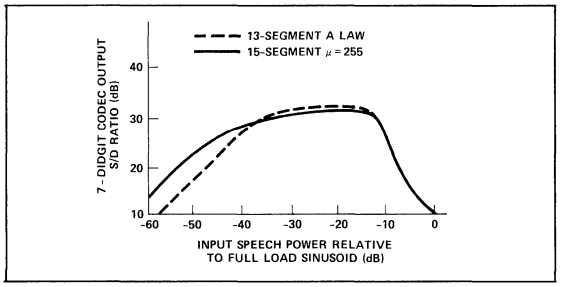


Figure 1. Input Speech Power Relative to Full Load Sinusoid (dB)

The practical implementation of the two transfer functions is accomplished by standardized piece-wise linear approximations. The transfer functions are implemented in chords or segments where the transfer function within any one chord is a linear staircase. Each chord has sixteen steps and the size of the step in each succeeding chord is double the size of the step in the preceeding chord. There are normally eight chords numbered zero through seven in both μ-law and A-law characteristics. For the A-law function the first two chords on either side of the origin have equal step sizes, whereas, for the μ-law function, the second chord after the origin has a step size which is double that of the first. For all remaining chords the steps double in size for each succeeding chord. This applies to both the μ-law and A-law functions. For the A-law function the four chords about the origin can be considered as a single segment so that the A-law characteristic is sometimes referred to as being a "13-segment" code. The A-law characteristic also differs from the μ-law characteristic in the manner in which the transfer function crosses the origin. The X-axis origin for the μ-law is at "mid-step" while the X-axis origin for the A-law is coincident with a "riser". This can be understood better from the "blow-ups" about the origin of Figures 2 and 3.

In order to obtain the best implementations of the transfer function, companded DACs are constructed such that encode and decode functions are offset by one-half step. With this technique the quantizing band for the encode DAC will be centered about the decode value. This can be seen in Figure 4, where the μ-law characteristics about the origin are shown. (The A-law characteristics would be identical except for the "mid-riser" phenomena at the origin.) As an example suppose that, for Figure 4, an analog input whose amplitude lies between levels 2 and 4 is being encoded. The best quantizing code to assign to this entire quantizing band is its mean value of 3. Thus the DAC used in the suc-

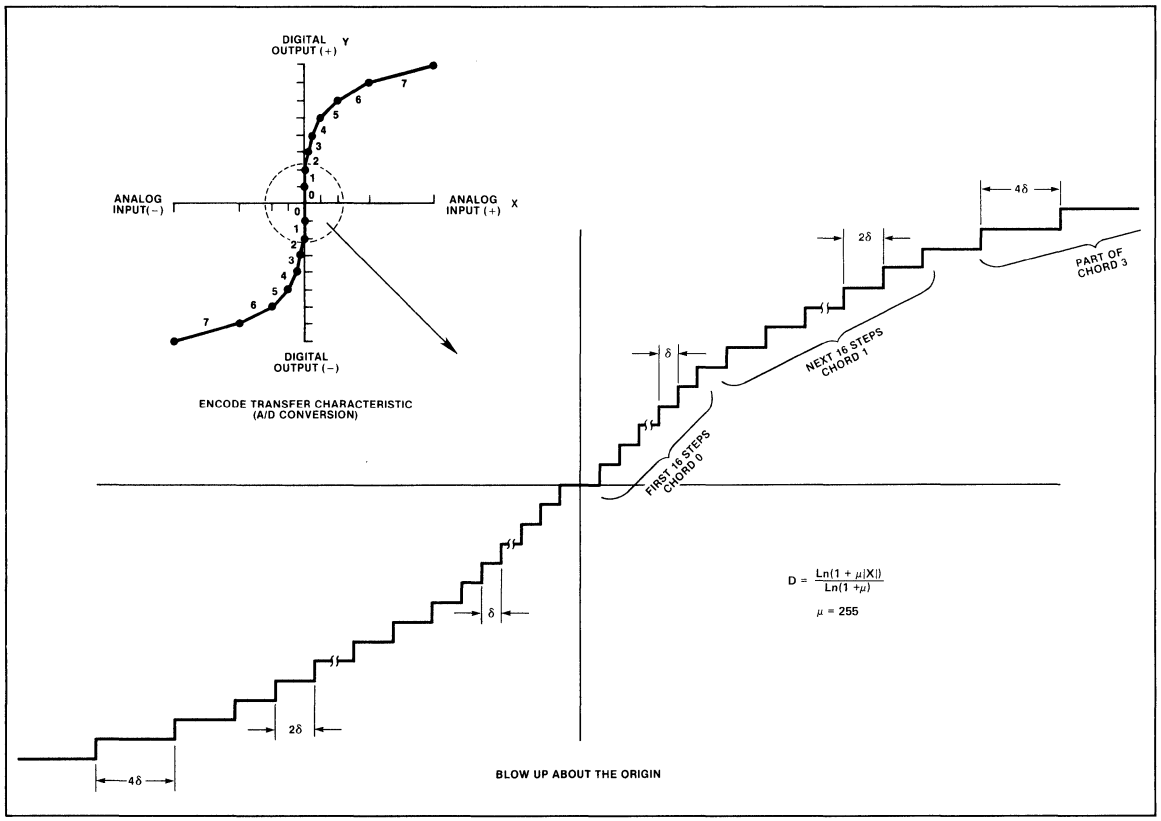


Figure 2. μ-Law Transfer Function

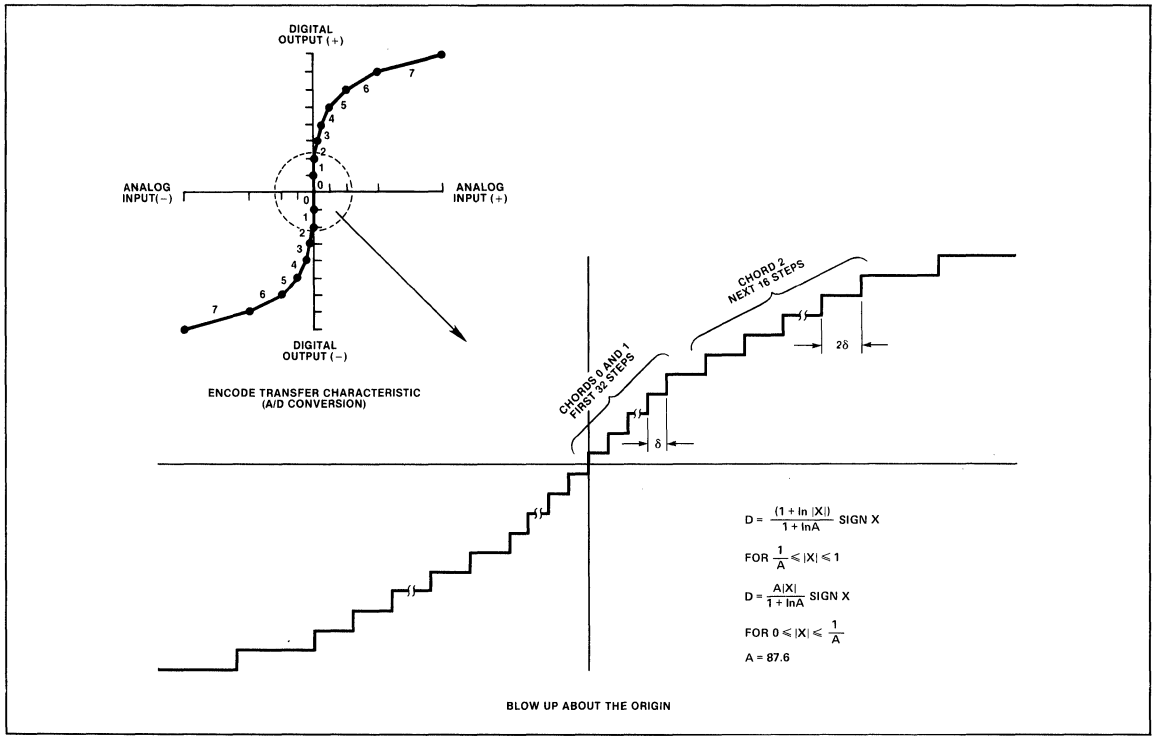


Figure 3. A-Law Transfer Function

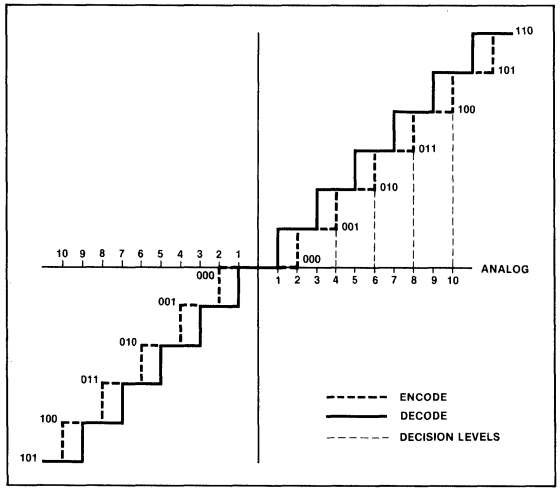


Figure 4. μ-Law Encode/Decode Characteristics About the Origin

cessive approximation feedback loop of the encode has output levels which represent the quantizing band edges. These can be referred to as decision levels. On the other hand the DAC for the decoder has output levels which represent the mean values of the quantizing bands which must, of necessity, be centered about the decoder output values. The end result is that a DAC used for decoding must be offset one-half step from the DAC used for encoding. This situation must exist over the entire range of the CODEC. A transmission system implemented with companding DACs is shown in Figure 5.

COMDAC® SYSTEM DESCRIPTION

A block diagram of PMI's companding DAC is shown in Figure 6. A single current output DAC is used to generate outputs for either the encode or decode mode of operation.

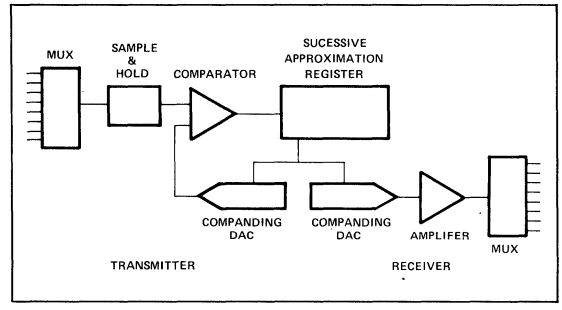


Figure 5. Transmission System Implemented with Companding DAC

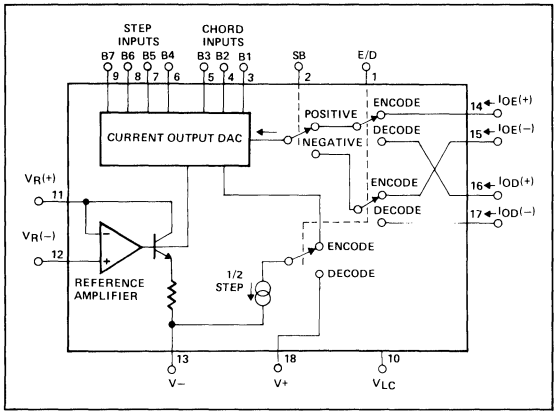


Figure 6. Equivalent Circuit and Pin Connection Diagram

Each companding DAC can be programmed to operate as either an encoder or a decoder by properly programming the E/D pin. The encode mode is offset one-half step from the decode mode by means of the current generator which is switched in during the encode mode. The reference amplifier establishes the current reference for the current output DAC. The sign bit pin (SB) controls the positive-negative switch which directs the output of the current output DAC.

This output will eventually end up at the positive (I_{OE+} or I_{OD+}) outputs or the negative (I_{OE-} or I_{OD-}) outputs depending on whether the SB pin is programmed to a binary "1" or a binary "0". The encode-decode switch E/D determines whether the DAC output shall be directed to the encode or decode terminations as shown in Figure 6. In addition, this same switch introduces the one-half step of offset current required during encode.

A better understanding of the COMDAC® circuitry is obtained by reviewing the previously discussed piece-wise linear approximation of the companding DAC transfer function to the desired μ-law or A-law transfer functions. Each chord or segment consists of 16 steps numbered from 0 to 15. The size of the steps double in size from one chord to the next as the number of the chord increases. The chords are numbered 0 to 7. In order to smooth out the characteristics during the transition from one chord to the next, the step current for step 0 of each chord is 1-1/2 times larger than the current of the highest step of the chord immediately preceding it. The succeeding 15 steps (steps 1 to 15) are then two times the size of the steps of this previous chord. These characteristics can be examined in Figure 7.

To implement the transfer function, the first chord (N = 0) uses 16 equal steps each of whose size, I_0 is 1/16 of chord current source I_{C0} for A-law, or 1/16.5 of current source I_{C0} for μ-law. The next chord, N = 1, must begin at $I_{C0} + 1.5I_0$ for both A-law or μ-law. Another way of saying this is that chord

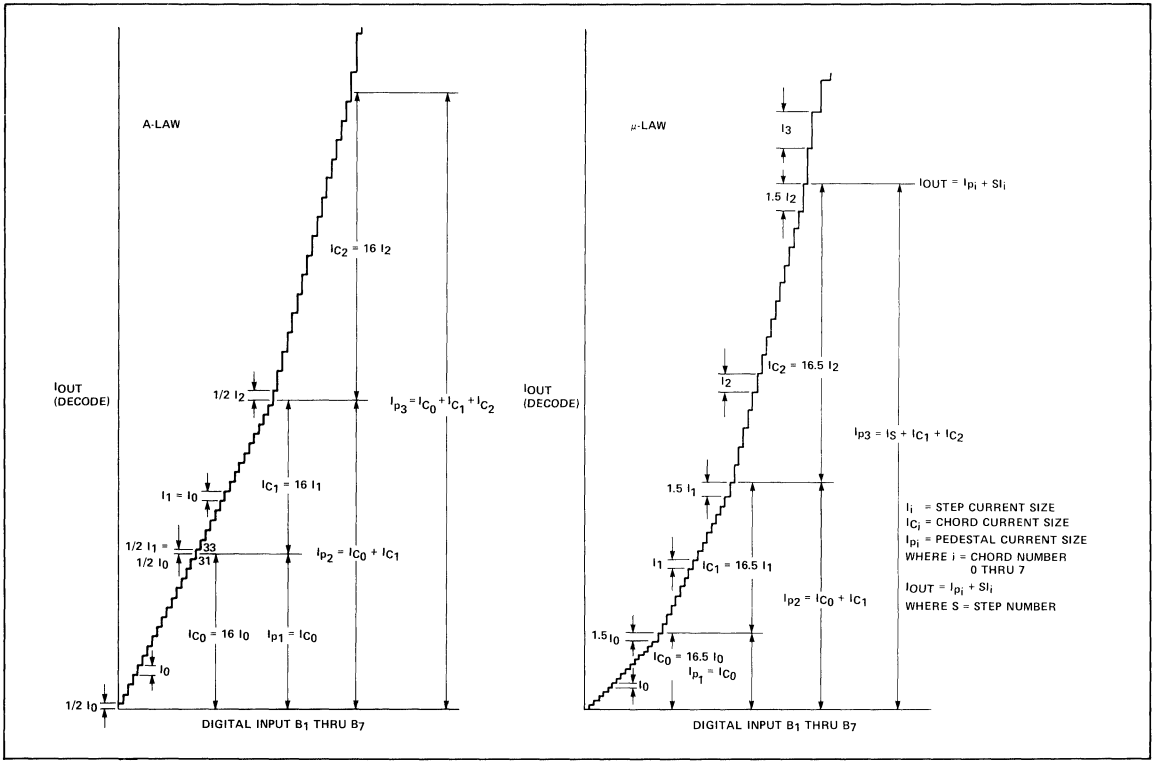


Figure 7. Construction of the Companding DAC Transfer Function

$N = 1$ begins 16.5 steps from the origin. In order to accomplish this a pedestal current must be directed toward the output whose magnitude is equal to $I_{C0} + 1.5I_0$. Chord C2 begins at $I_{C0} + 1.5I_0 + I_{C1} + 1.5I_1$ and ends at $I_{C0} + 1.5I_0 + I_{C1} + 1.5I_1 + I_{C2} + 1.5I_2$ and so forth. This process continues with pedestal currents for each chord number N described by the equation:

$$I_{PN} = \sum_{i=0}^{N-1} (I_{Ci} + 1.5I_i) = 16.5 \sum_{i=0}^{N-1} I_i$$

note that $I_{PO} = 0$.

A functional diagram of a companding DAC which implements the proper transfer function discussed above is shown in Figure 8, which operates in the following manner:

16.5 step currents (16.0 steps for A-law) where a step current is equal to the current step caused by changing the least significant bit in the chord of interest. Note that this satisfies the requirement of the equation for pedestal current I_{PN}. The step generator has the ability to sum current I_E into the output mode to provide the one-half step offset required when the system is operating in the encode mode. This one-half step offset current is controlled by the E/D pin. The system is in the encode mode when the E/D pin is biased to a binary "1".

DETAILED CIRCUIT DESCRIPTION

All of the single pole double throw switches in Figure 8 are constructed of bipolar emitter coupled transistors. One such switch is shown as an example in Figure 9. When the

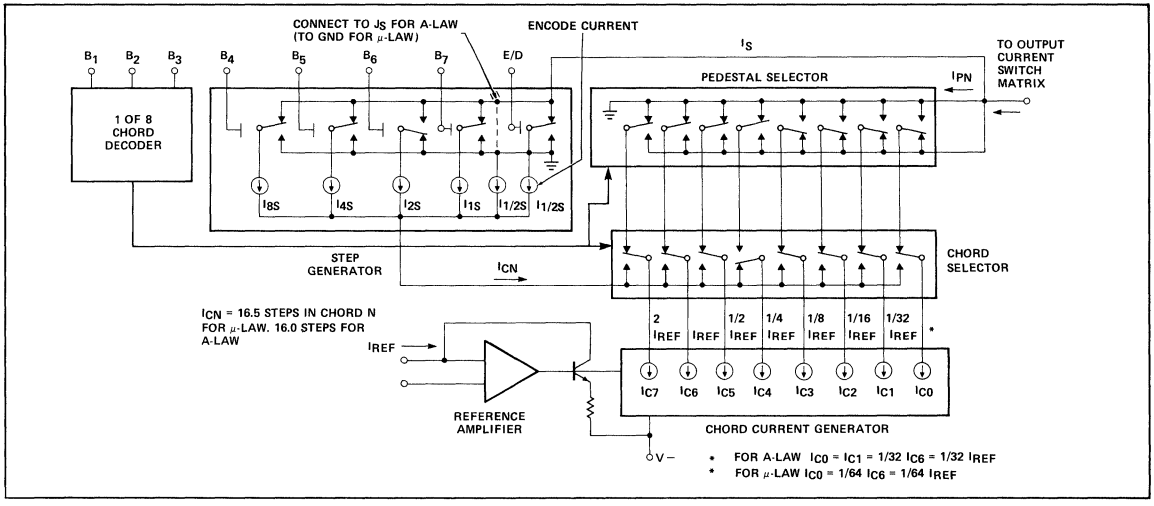


Figure 8. COMDAC® Companding DAC Functional Diagram

the reference amplifier sets the bias current for the chord generator by means of I_{C7} which is a current mirror whose output is equal to $2I_{REF}$. Next, due to the operation of an R–2R ladder which is described in a following paragraph, I_{C6} is made equal to one-half I_{C7} and is therefore equal to I_{REF}. I_{C5} is made equal to one-half I_{C6} and so forth. From I_{C3} down to I_{C0} a slave ladder is used rather than an R–2R ladder but the results are the same. The chord currents double in size progressing from I_{C0} to I_{C7} respectively (for A-law however $I_{C1} = I_{C0}$). The chord selector is programmed from the 1 of 8 decoder so that the chord identified by binary chord number N on leads B_1 to B_3 will switch I_{CN} to the step generator. All other chord currents are switched to the pedestal selector. The pedestal selector is programmed from the same 1 of 8 chord decoder such that chords I_0 to I_{N-1} are switched to the pedestal selector output in order to generate pedestal current I_{PN}. All other chord currents are switched to ground so that a pedestal current equal to the sum of the chord currents from I_{C0} to $I_{C(N-1)}$ will be directed to the output current switch matrix as I_{PN}. The I_{CN} flowing into the chord selector from the step generator is equal to

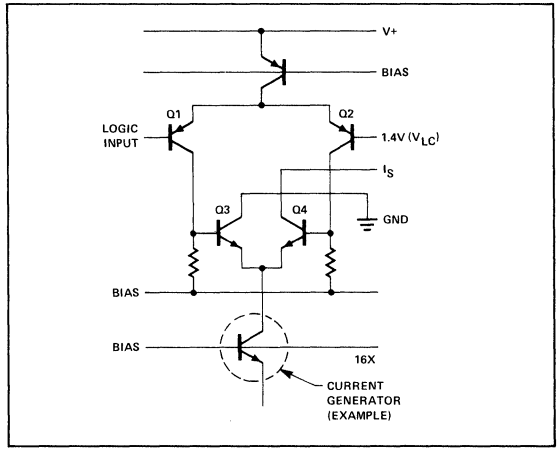


Figure 9. Double-Pole Double-Throw Switch Implemented with Emitter Coupled Transistors

logic input exceeds the logic level bias V_{LC} Q_1 is turned off and Q_2 is turned on. In turn Q_3 is turned off and Q_4 is turned on thus effectively switching the current generator, shown as an example, from the ground to I_S. Conversely, lowering the logic level input below V_{LC} will switch the current from I_S to ground. The V_{LC} Control permits the circuit to interface with a large range of logic levels.

The chord current generator circuit is shown in Figure 10. This circuit is the implementation of the chord current generator previously discussed. Q_0 is forced to operate at the reference input current I_{REF} and Q_1, with an emitter resistor one-half the size of the emitter resistor of Q_0, will then operate at $2I_{REF}$. Q_2 through Q_4 will operate at progressively smaller currents where each transistor operates at one-half the current of the transistor to its immediate left. To review this normal R–2R current-ladder function notice that Q_{4A} and Q_{4B} operate at equal currents and that the sum of their currents is equal to that of one transistor with an emitter resistor equal to R. When the series resistor R is added to the junction of the emitter resistors of Q_{4A} and Q_{4B} the current of Q_3 will be forced to equal the sum of the Q_{4A} and Q_{4B} currents. Thus Q_{4A} current equals one-half the Q_3 current. Now the current from Q_{4A}, Q_{4B} and Q_3 must all flow through the next series resistor R. This current is equal to twice that of Q_3; therefore it is easy to compute that the Q_2 current is twice that of the Q_3. The same reasoning may be used to proceed down the ladder to show that each transistor in the ladder sinks twice the current of the transistor on its immediate right. The slave ladder consisting of Q_5 through Q_{8A} and Q_{8B} continues to halve currents for each transistor proceeding to the right. However this part of the chord current generator uses scaled resistors instead of the R–2R ladder technique. Since Q_{4B} sinks constant current from the slave ladder, and since all the current must flow through the scaled emitter resistors, then the curent through each transistor must be inversely proportional to the size of its emitter resistor. By examination of the slave ladder it can be seen that each transistor proceeding to the right sinks one-half the current of the transistor to its immediate left. For the μ-law chord current generator Q_{8B} is simply diode connected such that the chord current for chord C_0 is roughly one-half the current of chord C_1. For the A-law chord current generator, however, the collectors of transistors Q_{8A} and Q_{8B} are tied together so that I_{C0} is exactly equal to I_{C1}. The currents flow to the chord current generator from an array of bipolar single pole double throw switches labeled "chord selector" in Figure 8. The actual switches are not shown in this paper.

The Step Current Generator is shown in Figure 11. Again the single pole double throw switches which connect the step generator to the output current matrix as shown in the companding DAC functional diagram are not represented. The step generator is connected to the chord selector which sinks I_{CN}. Ratioed emitters are used to divide the current. The largest emitter is 16 times the size of the smallest emitter and therefore sinks 16 times the current. The A-law step generator differs from the μ-law step generator in that each chord begins with a riser instead of a step. This also applies to the origin, therefore one-half step of current flows (decode mode) even when the binary input to the step generator is "0". Step switches controlled directly by the binary code connect the appropriate collectors of the step current generator transistors to the output current matrix. For both A-law and μ-law devices I_{CN} is one of the pedestal currents. The difference is that for the A-law device the pedestal current is equal to 16 steps whereas, for the μ-law, the pedestal current is equal to 16.5 steps.

NORMALIZED COMPANDING DAC OUTPUTS

It is convenient to generate tables of normalized values which correspond exactly to the CCITT (Consultative Committee for International Telephone and Telegraph) specifications. The following tables are normalized to the smallest DAC output which is equivalent to one-half step.

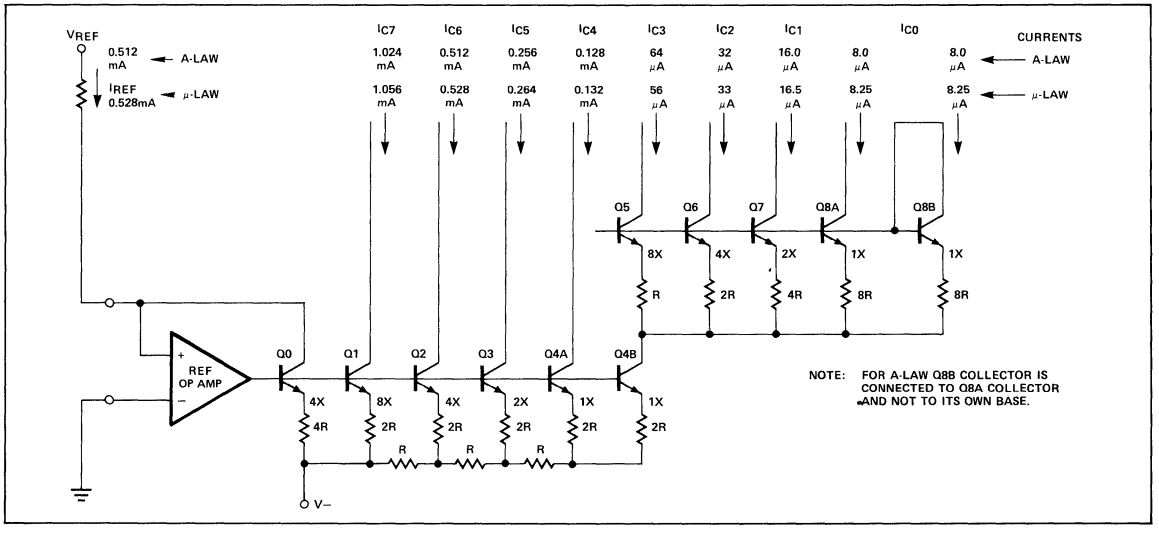


Figure 10. Chord Current Generator Diagram

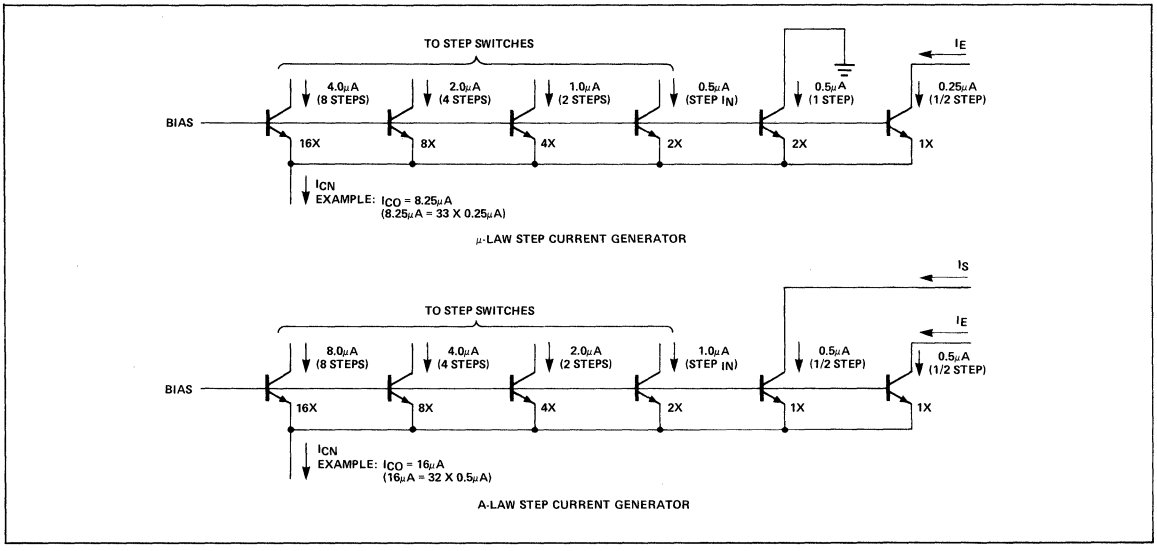


Figure 11. A-Law and μ-Law Step Current Generators

μ-Law Normalized Table

NORMALIZED DECODE OUTPUT (SIGN BIT EXCLUDED) $I_{C,S} = 2[2^C (S + 16.5) - 16.5]$

C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	33	99	231	495	1023	2079	4191
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	211	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
STEP SIZE		2	4	8	16	32	64	128	256

μ-Law Normalized Table

NORMALIZED ENCODE LEVEL (SIGN BIT EXCLUDED) $I_{C,S} = 2[2^C (S + 17) - 16.5]$

C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	1	35	103	239	511	1055	2143	4319
1	0001	3	39	111	255	543	1119	2271	4575
2	0010	5	43	119	271	575	1183	2399	4831
3	0011	7	47	127	287	607	1247	2527	5087
4	0100	9	51	135	303	639	1311	2655	5343
5	0101	11	55	143	319	671	1375	2783	5599
6	0110	13	59	151	335	703	1439	2911	5855
7	0111	15	63	159	351	735	1503	3039	6111
8	1000	17	67	167	367	767	1567	3167	6367
9	1001	19	71	175	383	799	1631	3295	6623
10	1010	21	75	183	399	831	1695	3423	6879
11	1011	23	79	191	415	863	1759	3551	7135
12	1100	25	83	199	431	895	1823	3679	7391
13	1101	27	87	207	447	927	1887	3807	7647
14	1110	29	91	215	463	959	1951	3935	7903
15	1111	31	95	223	479	991	2015	4063	8159
STEP SIZE		2	4	8	16	32	64	128	256

A-Law Normalized Table

NORMALIZED DECODE OUTPUT (SIGN BIT EXCLUDED)

$I_{CS} = 2^{N-1} (33 + 2S)$ For $N > 0$
$I_{CS} = 2S + 1$ For $N = 0$

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	1	33	66	132	264	528	1056	2112
1	0001	3	35	70	140	280	560	1120	2240
2	0010	5	37	74	148	296	592	1184	2368
3	0011	7	39	78	156	312	624	1248	2496
4	0100	9	41	82	164	328	656	1312	2624
5	0101	11	43	86	172	344	688	1376	2752
6	0110	13	45	90	180	360	720	1440	2880
7	0111	15	47	94	188	376	752	1504	3008
8	1000	17	49	98	196	392	784	1568	3136
9	1001	19	51	102	204	408	816	1632	3264
10	1010	21	53	106	212	424	848	1696	3392
11	1011	23	55	110	220	440	880	1760	3520
12	1100	25	57	114	228	456	912	1824	3648
13	1101	27	59	118	236	472	944	1888	3776
14	1110	29	61	122	244	488	976	1952	3904
15	1111	31	63	126	252	504	1008	2016	4032
STEP SIZE		2	2	4	8	16	32	64	128

A-Law Normalized Table

NORMALIZED ENCODE DECISION LEVELS (SIGN BIT EXCLUDED)

$I_{CS} = 2^{N-1}(34 + 2S)$ For $N > 0$
$I_{CS} = 2S + 2$ For $S = 0$

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	2	34	68	136	272	544	1088	2176
1	0001	4	36	72	144	288	576	1152	2304
2	0010	6	38	76	152	304	608	1216	2432
3	0011	8	40	80	160	320	640	1280	2560
4	0100	10	42	84	168	336	672	1344	2688
5	0101	12	44	88	176	352	704	1408	2816
6	0110	14	46	92	184	368	736	1472	2944
7	0111	16	48	96	192	384	768	1536	3072
8	1000	18	50	100	200	400	800	1600	3200
9	1001	20	52	104	208	416	832	1664	3328
10	1010	22	54	108	216	432	864	1728	3456
11	1011	24	56	112	224	448	896	1792	3584
12	1100	26	58	116	232	464	928	1856	3712
13	1101	28	60	120	240	480	960	1920	3840
14	1110	30	62	124	248	496	992	1984	3968
15	1111	32	64	128	256	512	1024	2048	*4096
STEP SIZE		2	2	4	8	16	32	64	128

The numbers in these tables are directly proportional to the input reference current. However the exact relationship is somewhat complicated. A reference current of 528μA for the μ-law DAC will produce a step size of 0.5μA; thus, for the μ-law device driven by a reference current of 528μA, it is only necessary to multiply all the numbers in the normalized tables by one-half step or 0.25μA to obtain the output in μA. The table tabulated below corresponds to a 528μA reference.

μ-Law Current Output Table

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS (SIGN BIT EXCLUDED)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	8.25	24.75	57.75	123.75	255.75	519.75	1047.75
1	0001	0.5	9.25	26.75	61.75	131.75	271.75	551.75	1111.75
2	0010	1	10.25	28.75	65.75	139.75	287.75	583.75	1175.75
3	0011	1.5	11.25	30.75	69.75	147.75	303.75	615.75	1239.75
4	0100	2	12.25	32.75	73.75	155.75	319.75	647.75	1303.75
5	0101	2.5	13.25	34.75	77.75	163.75	335.75	679.75	1367.75
6	0110	3	14.25	36.75	81.75	171.75	351.75	711.75	1431.75
7	0111	3.5	15.25	38.75	85.75	179.75	367.75	743.75	1495.75
8	1000	4	16.25	40.75	89.75	187.75	383.75	775.75	1559.75
9	1001	4.5	17.25	42.75	93.75	195.75	399.75	807.75	1623.75
10	1010	5	18.25	44.75	97.75	203.75	415.75	839.75	1687.75
11	1011	5.5	19.25	46.75	101.75	211.75	431.75	871.75	1751.75
12	1100	6	20.25	48.75	105.75	219.75	447.75	903.75	1815.75
13	1101	6.5	21.25	50.75	109.75	227.75	463.75	935.75	1879.75
14	1110	7	22.25	52.75	113.75	235.75	479.75	967.75	1943.75
15	1111	7.5	23.25	54.75	117.75	243.75	495.75	999.75	2007.75
STEP SIZE		.50	1	2	4	8	16	32	64

*Virtual Decision Level

A similar exercise will yield a corresponding table for the A-law part. Multiplying all the numbers in the normalized A-law table, for instance, will produce a table of currents for a reference input of 512μA. A table based on 512μA reference current will have a step size of 1.0μA and is tabulated in the μ-law current output table.

A-Law Current Output Table

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS (SIGN BIT EXCLUDED)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0.5	16.5	33	66	132	264	528	1056
1	0001	1.5	17.5	35	70	140	280	560	1120
2	0010	2.5	18.5	37	74	148	286	592	1184
3	0011	3.5	19.5	39	78	156	312	624	1248
4	0100	4.5	20.5	41	82	164	328	656	1312
5	0101	5.5	21.5	43	86	172	344	688	1376
6	0110	6.5	22.5	45	90	180	360	720	1440
7	0111	7.5	23.5	47	94	188	376	752	1504
8	1000	8.5	24.5	49	98	196	392	784	1568
9	1001	9.5	25.5	51	102	204	408	816	1632
10	1010	10.5	26.5	53	106	212	424	848	1696
11	1011	11.5	27.5	55	110	220	440	880	1760
12	1100	12.5	28.5	57	114	228	456	912	1824
13	1101	13.5	29.5	59	118	236	472	944	1888
14	1110	14.5	30.5	61	122	244	488	976	1952
15	1111	15.5	31.5	63	126	252	504	1008	2016
STEP SIZE		1	1	2	4	8	16	32	64

Reviewing the companding DAC functional diagram Figure 8 demonstrates the relationship between step size and I_{REF}. For a μ-law device I_{C0} equals 16.5 chord zero steps and for an A-law device I_{C0} equals 16 chord zero steps. I_{C6} is always equal to I_{REF} in either system. I_{C6} is then equal to 64 times I_{C0} for a μ-law system, and 32 times I_{C0} for an A-law system. The step size can then be related to I_{REF} by the following equations:

$$\text{step size} = I_{REF}/64 \times 16.5 = I_{REF}/1056 \text{ (μ-law)}$$
$$\text{step size} = I_{REF}/32 \times 16 = I_{REF}/512 \text{ (A-law)}$$

Now for a reference current of 528μA the step size for a μ-law system is 528/1056 or 0.5μA. For a reference current of 512μA the step size for an A-law system is 512/512 or 1.0μA. These values concur with those used to generate the tables.

In the design of the PMI DAC-89 the biasing resistors were not scaled to exactly integer values. This was done deliberately to standardize somewhat on 528μA input reference current for both A-law and μ-law parts. The performance of the device is not affected, however the actual scaling is somewhat complicated and will not be discussed in this paper.

Finally if encode output tables were desired for current output they could be obtained by scaling to proper step size the normalized encode tables or adding one-half step to each value in the decode table, where the step size depends on the chord number.

DAC ACCURACY

Companding DACs must be manufactured to satisfy a unique set of parameters. The performance of a companded DAC used for telephony must satisfy the requirements of a communication system on an end-to-end basis. A voice channel is first encoded by one CODEC then decoded by a second CODEC such that the system performance can be measured on an audio-in-audio-out basis. The CODEC performance will be almost completely dominated by the Gain Tracking requirement.

GAIN TRACKING

Gain Tracking refers to the ability of a system to track its input power level. The test is normally made with a system such as that shown in Figure 12.

Gain Tracking is measured by monitoring the input and output levels in decibels. At an input level of −10Bm0 the output is recorded as the output reference level. For ideal Gain Tracking, any change (in dB) of the input level must be matched exactly by the same change in the output level.

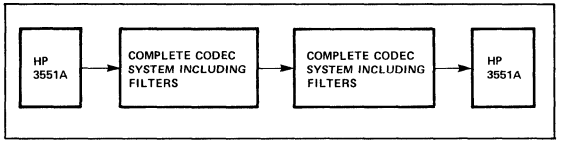


Figure 12. Gain Tracking or S/N Test

This condition is monitored over all input power levels of interest. The extent to which these power level changes differ (again in dB) is a measure of Gain Tracking, also referred to as gain deviation. The ATT/D3 Gain Tracking specification is show in Figure 13.

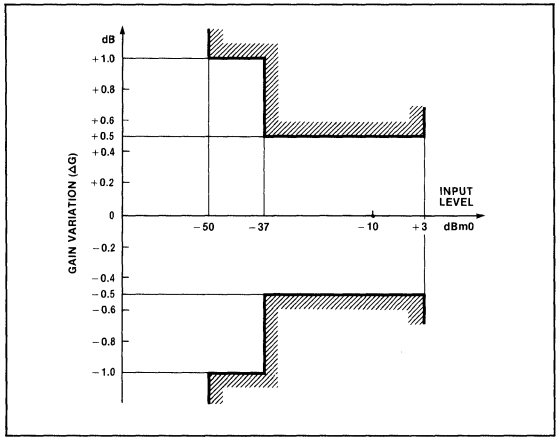


Figure 13. ATT/D3 Gain Tracking Specification

CCITT publishes two separate specifications for Gain Tracking. The apparatus used for making either of these tests is basically the same as that used in Figure 13 except that for the first part of the "method one" test the HP3551A would be replaced with a suitable white noise source at the input and an RMS reading voltmeter at the output. Gain Tracking masks equivalent to those found in CCITT publications are shown in Figure 14.

POWER LEVELS

For PCM channel performance measurements, power levels are characteristically expressed in dBm0. A reference level of 0dBm0 is established by referencing to a code in the **digital** transmission. The binary code pattern required to establish a reference level of 0dBm0 can be found in the CCITT publications. This pattern is reproduced in the PMI Telecommunications Handbook for the readers convenience. The constant repetition of these binary numbers at the normal sampling rate of 8kHz will produce a 1kHz sinusoid at a 0dBm0 reference level. Starting with this definition it can then be shown that a sinusoid whose peak value is just at the system saturation level (all "1s" PCM output) will have a power level of 3.14 and 3.17dBm0 for A-law and μ-law respectively.

SIGNAL-TO-DISTORTION MEASUREMENTS

Signal-to-Distortion is a measure of the total distortion a system will exhibit on an end-to-end basis. As with Gain Tracking this measurement is normally performed on an audio-to-audio basis. A typical setup for measuring Signal-to-Distortion is shown in Figure 15. A wideband (3kHz) filter may be substituted for the C-Message filter shown for some tests.

Figure 16 shows the ATT/D3 specification mask with the performance of a PMI demonstration COMDAC® based shared CODEC system superimposed. This method of measuring Signal-to-Distortion is applicable to either CCITT or ATT specifications.

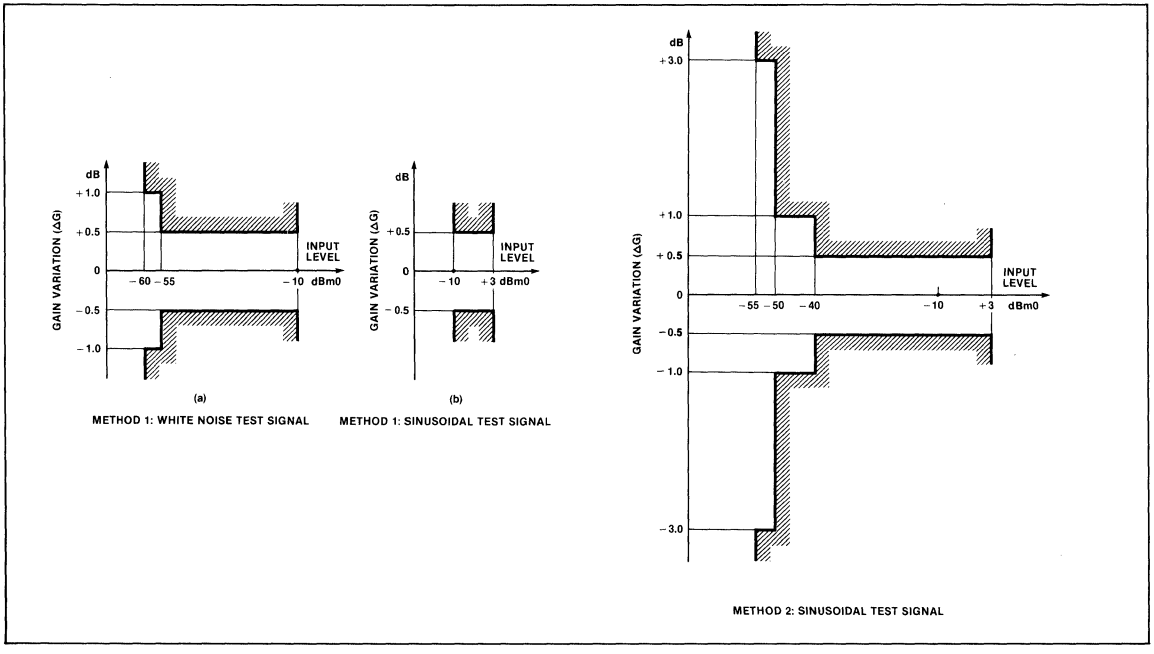


Figure 14. CCIT Gain Tracking Specification

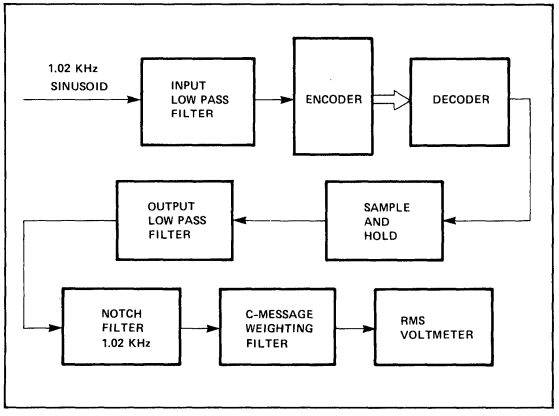


Figure 15. Signal-to-Distortion Test Setup

DAC ACCURACY VERSUS GAIN TRACKING AND SIGNAL-TO-DISTORTION RATIO

The analog portions of a PCM system usually make only a minor contribution to either Gain Tracking or Signal-to-Distortion errors. Thus, the major contribution to error is the inability of the companding DAC to accurately follow the encoding format. The process of quantizing and coding will cause some deviation from the ideal, however the errors made by the ideal CODEC system will be well within telephony specifications. To conform to the required Gain Tracking and Signal-to-Distortion specifications the DAC output currents must conform as closely as possible to the ideal transfer function as tabulated in the normalized tables. This corresponds to a specification of absolute error on the DAC output current with respect to its binary inputs. The DAC-86/89 companded DACs are guaranteed to plus or minus one-fourth step from ideal values in chord zero and to plus or minus one-half step elsewhere. This information can be transformed into tabular form by adding the allowable error to the DAC tables. Either the normalized tables or the current output tables can be used as a basis for this exercise.

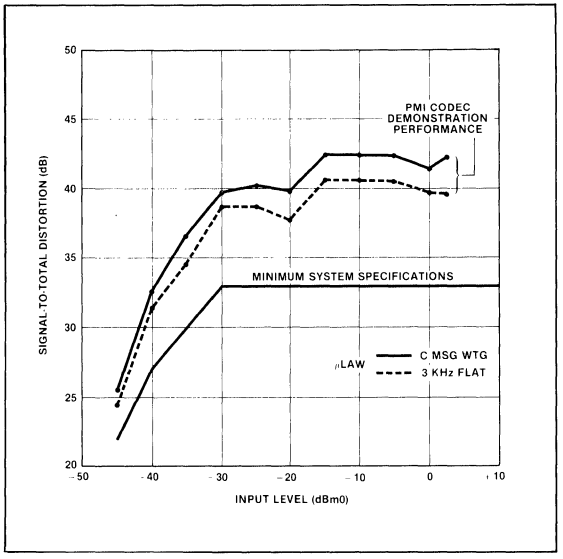


Figure 16. ATT/D3 Signal-to-Distortion Mask

APPLICATION NOTE 40

INTRODUCTION

This Application Note consists of a collection of circuits which use buffer amplifiers in a variety of applications. As will be shown, buffers may be used to make filters, current sources, cable drivers, sample and holds, line drivers for multiplexers, current boosters, and high speed voltage output DACs.

INDUCTORS AND FILTERS

The active inductor in Figure 1 is realized with an eight-lead IC, two carbon resistors, and a small capacitor. A commercial inductor of 50 henries may occupy up to five cubic inches.

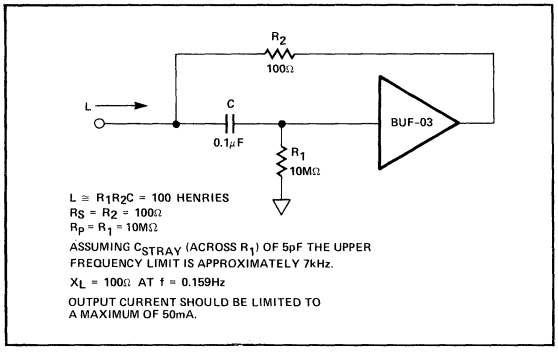


Figure 1. Active Inductor

The tuned circuit shown in Figure 2 uses the simulated inductor of Figure 1 (R_1, R_2, C_1) and C_2. Depending upon whether the circuit is driven at E_1 or E_2 the responses of Figures 3 or 4 result. The resonant response in both cases is

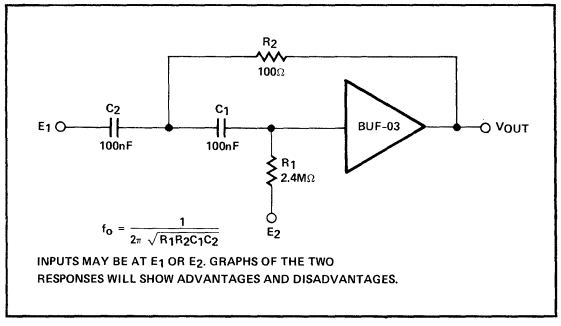


Figure 2. Tuned Circuit

+38dB at 103Hz. The Figure 3 response is +2.5dB at 200Hz and −10dB at 50Hz. On the other hand, the Figure 4 response is −9dB at 200Hz and +2.5dB at 50Hz.

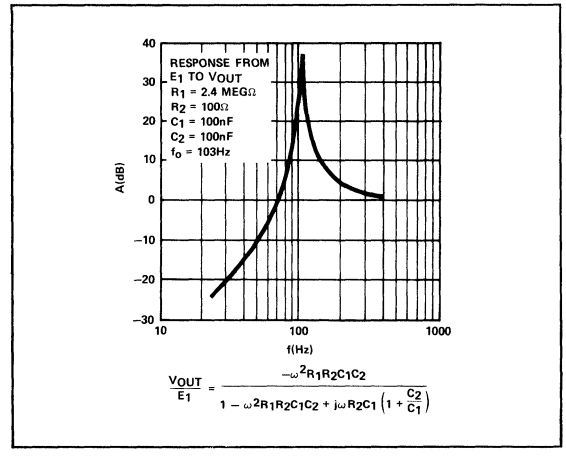


Figure 3. Response from E_1 to V_{OUT}

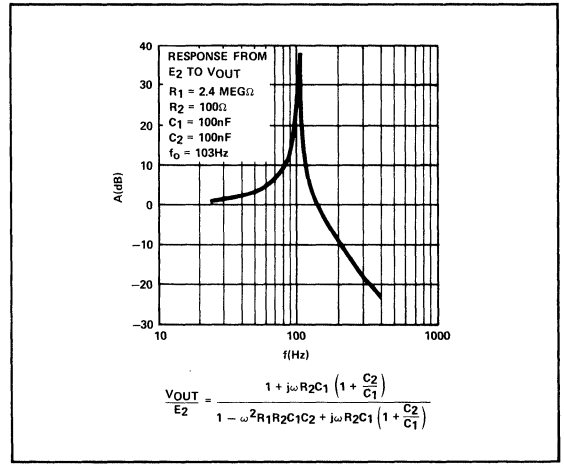


Figure 4. Response from E_2 to V_{OUT}

Figure 5 shows a low pass filter realized for f_0 of 1MHz. What is remarkable about this filter is most ICs do not have the full power bandwidth to handle 1MHz signals in the 5 to 10 Volt range, while the BUF-03 has a greater than 4MHz full power bandwidth for a $20V_{p-p}$ sinewave. Similar comments apply to the filter in Figure 6. In other words, the outstanding bandwidth of the BUF-03 extends the bandwidth capability of certain classes of active filters.

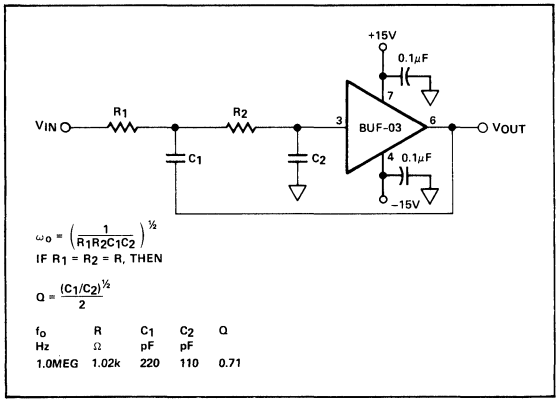


Figure 5. Low Pass Filter (High Frequency)

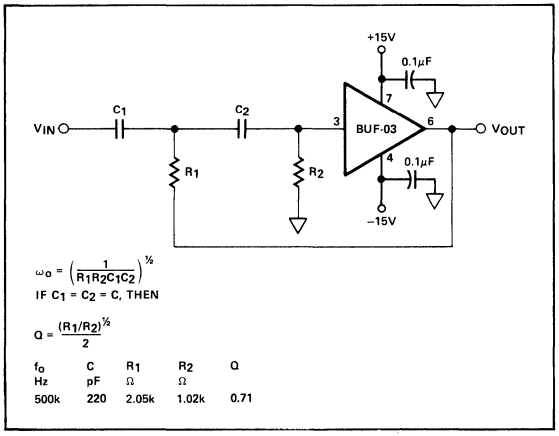


Figure 6. High Pass Filter (High Frequency)

The BUF-03 can be used to make a 4.5MHz trap for use in TV. This circuit is shown in Figure 7, and the elements are chosen such that no capacitor is less than 100pF.

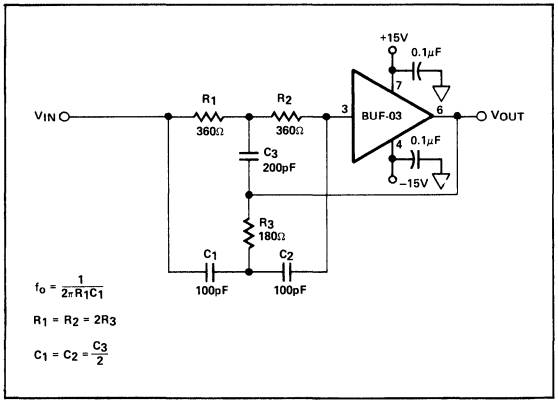


Figure 7. Notch Filter at 4.5MHz

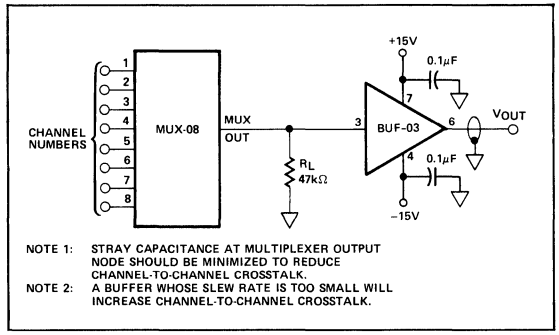


Figure 8. High Speed Line Driver for Multiplexers

The BUF-03 can be used as a data line driver because of its speed and current drive capabilities. The connection for this application is shown in Figure 8. The realization of a high speed sample and hold is possible using the BUF-03 and suitable analog switches. The circuit shown in Figure 9 provides the highest speed because there are no feedback loops to slow down the settling times. Typically the sample and hold is followed by a successive approximation analog-to-digital converter (ADC). The final application involves the BUF-03 and the DAC-08 (digital-to-analog converter). Figure 10 shows how it is possible to develop both V_{OUT} and $\overline{V_{OUT}}$. The output capacitance of the DAC-08 is approximately 15pF, thus as R_0 increases in value, so does the settling time for V_{OUT} (and $\overline{V_{OUT}}$).

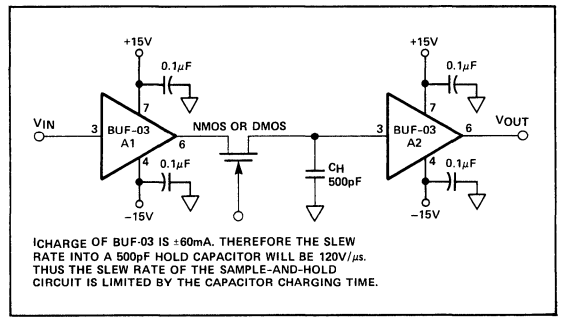


Figure 9. High Speed Sample and Hold

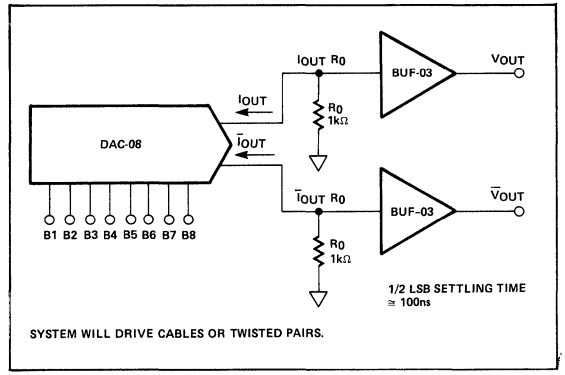


Figure 10. High Speed Voltage Output DAC

LINE DRIVER APPLICATIONS

If your FET "line driver" has the speed but not the stability or the current capability to drive coaxial cables, its output may be buffered with a BUF-03 as shown in Figure 11. Figure 12 shows an alternative connection when better accuracy and high current capability is needed. Note that the limitation on R_L being greater than 1kΩ does not apply in this case since the added error caused by lower impedances is imbedded inside the feedback loop of the op amp.

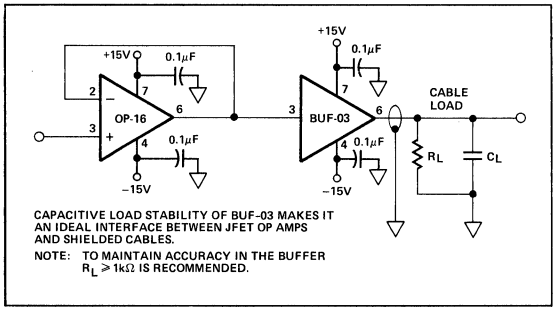


Figure 11. Convert FET Op Amp Into Cable Driver

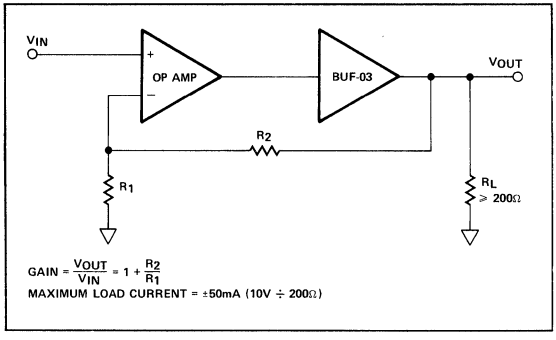


Figure 12. Current Booster

MISCELLANEOUS USES OF BUFFERS

Single supply applications can be realized using the BUF-03 as shown in Figure 13. The input is DC biased to +10V such that the BUF-03 operates in the linear region. Signal is AC coupled to the input and also AC coupled to the output load resistor.

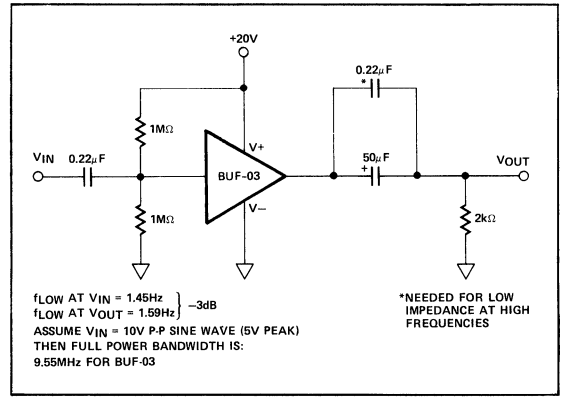


Figure 13. Single Supply AC Buffer (High Speed)

CONCLUSION

While the list is by no means all inclusive, this application note has attempted to point out some of the myriad of uses for the IC buffer. In particular, the BUF-03 makes possible a whole new class of high frequency filters and high speed current sources. Many problems in data acquisition systems can be solved by the use of buffers. In addition, the BUF-03 is useful in providing increased drive current, as well as the ability to drive long cables without instability. Finally, the versatility of the reference zener can be increased by using buffers, and for AC applications the buffer can be used on single power supplies.

PMI

AN-41

IMPROVED SHARED-CHANNEL CODEC DESIGN WITH PMI's COMPANDING DACs

Precision Monolithics Inc.

APPLICATION NOTE 41

DESIGNERS FACE CHOICE

Designers of telecommunications systems are faced with a fundamental design decision; they must base the design of digital voice transmission systems on either the use of a CODEC shared over several analog channels or on the use of one CODEC per channel.

Since 1976, users of PMI's shared-channel approach point to the economical advantages of a system that incorporates an encoder and a decoder capable of accommodating multiple voice channels. Proponents of single-CODEC-per-channel systems generally cite the straight-forward techniques involved in implementing this concept as the motivation for its selection.

The use of the shared-CODEC configuration is appealing because fewer integrated circuits per channel are required and less circuit board area per channel is needed. Because of its lower cost per channel and lower total system cost, the shared-channel CODEC concept looms as the logical choice for designers provided it can meet the performance needs of their systems.

Recently, new telecommunication components were introduced by Precision Monolithics Incorporated that improve the performance that can be obtained from a shared-CODEC system; the availability of these devices could influence future design decisions in favor of the shared CODEC concept over the single-CODEC approach. These newly developed devices, including the DAC-88 and the DAC-89 COMDAC® companding D/A converters, and the DMX-88 demultiplexer, not only provide performance which is superior to previously existing products, they are also easier to apply.

The degree of improvement offered by these devices and the present capabilities of a shared-CODEC system can be demonstrated using the circuit configuration shown in Figure 1. This configuration, an eight-channel digital transmission system, was designed and breadboarded by PMI as a vehicle for measuring the analog-input to analog-output transmission parameters commonly used to specify CODEC performance regardless of the particular system configuration.

Two of the components employed in the transmission system shown in Figure 1, the companding digital-to-analog converter and the analog multiplexer represent improved versions of previously existing products and are key contributors to the superior performance the system demonstrates over previous versions.

In the redesign of the companding DAC, it was felt that the best results would be achieved by improving the device's response within chord 0. Two design goals were set: to establish a reasonable settling time within chord 0 and to provide a guaranteed better than ±1/4 step linearity within that chord. Excellent results were obtained for both μ-law and A-law devices.

The new version of the companding DAC typically settles within 500ns, thus overcoming a restriction that had previously reduced the maximum number of channels for encoding. The IC's nominally settle to within ±1/8 step of the theoretical level in chord 0 and are 100% tested to be no worse than ±1/4 step.

Because of testing time restrictions, the settling time is given as a nominal specification. The guaranteed linearity specifi-

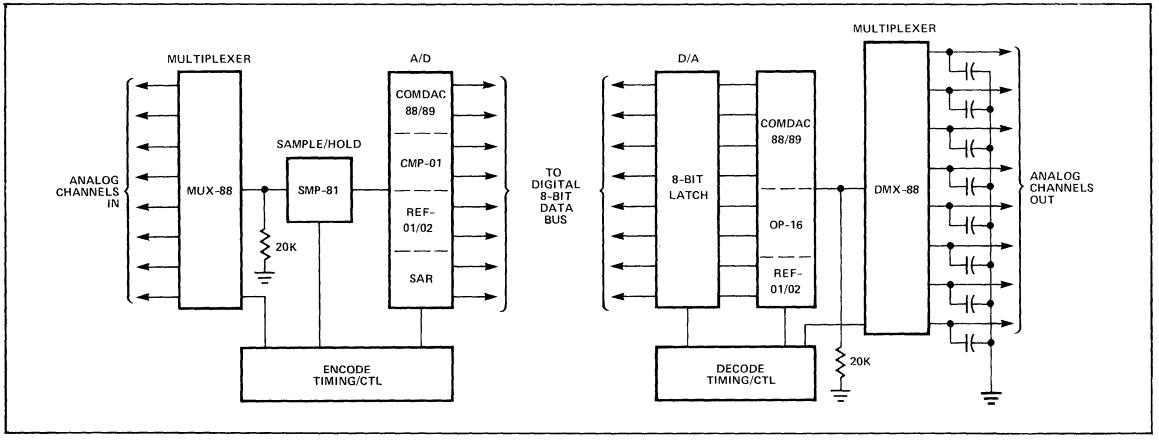


Figure 1. Eight-Channel Test Configuration

cation, in conjunction with the nominal settling time data, can provide the designer with the data needed to determine if the performance needs of his system can be satisfied.

When the earlier version of the output multiplexer was used as a sample-and-hold and switch, it was found that certain characteristics of the device caused idle channel noise and transmission degradation. An analysis showed that reduction of the charge injected during the switch turn-off would enhance the performance of the device. The effect of the charge injection becomes important because of the capacitance added to the MUX output. This output drives a high-impedance load (the PCM filter) and without a discharge path, the charge adds to the analog output being switched through the multiplexer. Because of the use of an improved JFET switch structure, the new multiplexer exhibits a discharged only 1/4 of 1/5 of the value for the previous device. Tests reveal that the idle channel noise is reduced by several dB when the DMX-88 is used as the output switch and sample-and-hold. In addition, the reduced amount of charge permits the use of a smaller value capacitor and thus increases the number of output channels that can be decoded.

DEMONSTRATOR MODIFICATIONS

The most obvious system improvement provided by the eight-channel system depicted in Figure 1, compared to an earlier design developed by PMI (described in the PMI application note AN-37), is a simplified encoder clocking scheme. In the original circuit, additional settling time was required because of the slower changing bits.

The new version of the clocking circuitry still employs a programmable read-only memory (PROM) for flexibility in performing future modifications and experimentation. However, the clock pattern is markedly changed. The new SAR clock timing diagram is shown in Figure 2. As can be seen, bit clocking is accomplished with a set 772 kHz clock. This

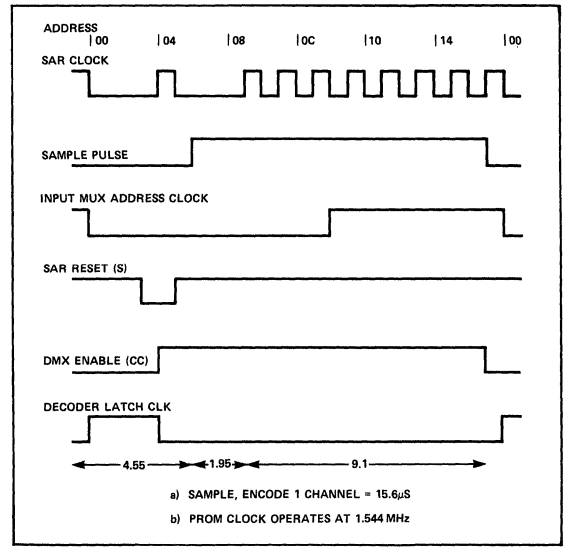


Figure 2. Encode Timing: DMX Control

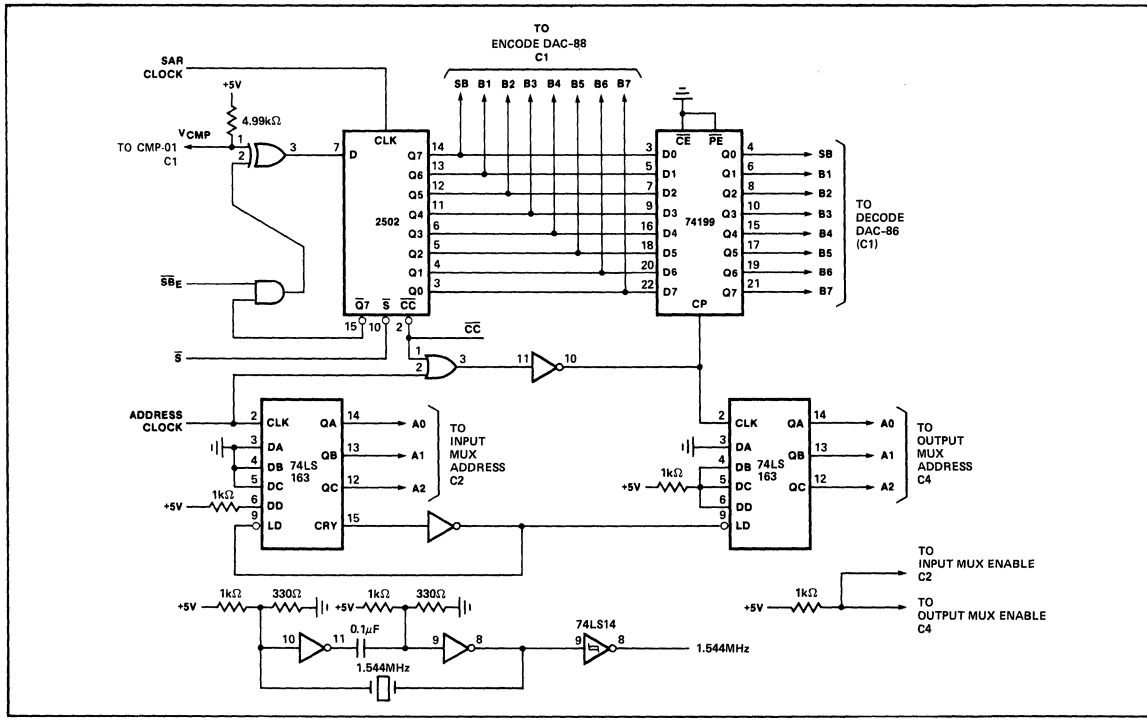


Figure 2A. Encode/Decode Controller

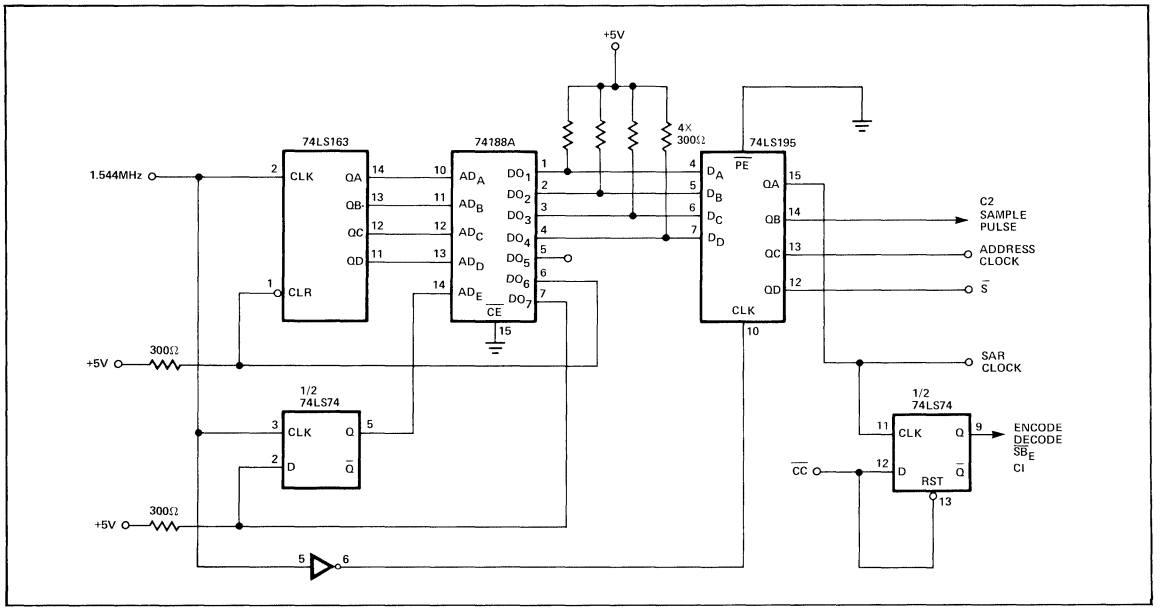


Figure 2B. Encode Clock

allows 9.1 μs (eight-channel rate) for encoding; the remaining cycle time (6.5 μs) is used for sampling the analog signal and holding the level to be encoded. The remaining cycle time is divided as follows: sample period, 4.55 μs; transition time between the hold signal and the sign bit acquisition, 1.95 μs.

The sampling time for the new clocking scheme is longer than it was for the old design (4.5 μs as compared to 3.2 μs) and the hold settling time has increased from 0.65 to 1.95 μs. As a result, the values measured for gain tracking differential (linearity) at low input levels (−55 dBm0) provide an indication of the improved response.

Since the clocking pattern has been simplified, the number of TTL gates needed is less than had been required by the original configuration. An even simpler clocking scheme can be designed by replacing the PROM, address counter and data latch with a "D" flip-flop and some additional gates. The use of a programmable clock generator, however, was advantageous in demonstrating the effects of various circuit components on the overall transmission performance. For example, by increasing the sample time and thereby reducing the hold settling time (keeping the SAR clock the same frequency), the system tends to show different characteristics. The gain tracking stays within spec, but signal-to-total distortion increases at levels below −40dBm0. The crosstalk performance (adjacent channel) also deteriorates. Apparently both of these effects are results of the output settling of the sample-and-hold device. The point is that by designing with a system consisting of individual devices the user can more precisely determine those components that have the greatest effect on system characteristics. The design can then be adapted to maximize certain performance attributes in lieu of other, less-important characteristics. The system as finalized in these notes is a compromise system, one aimed at providing adequate performance in various applicaitons. The final design modifications are left up to the individuals responsible for the specific systems.

The DAC-88 and DAC-89 have idle currents present on the selected output leads; these currents are equal on both the positive and negative outputs and are normally around 10μA. The DAC-89EX is specified at a lower reference current than the DAC-88. The new reference is 16μA less than the original value. The tests described here were performed with constant reference current for both the DAC-88 and the DAC-89. The effect on the A-law measurements means the full-scale output is 2079μA instead of 2016μA. Although all steps are slightly expanded, for the purpose of the data collected here the reference current difference is negligible.

The normal testing configuration used was to provide a test signal input in one channel and monitor the output of that channel (or adjacent channels for crosstalk) with a PCM receive filter and the prescribed receiver. The test diagram is shown in Figure 3. It becomes important to ground all unused encoder inputs to provide the proper termination. It also is very important when laying out system boards to generate sufficient ground planes and proper isolation between analog and digital ground areas. The common point of these ground areas should be as close to the power supply as possible. Also "daisy-chaining" of ground returns should be avoided. Careful consideration of grounding can help improve all system parameters.

The transmission test results collected with this system are shown in Figures 4 through 6. An example of results with a different clock pattern is also presented.

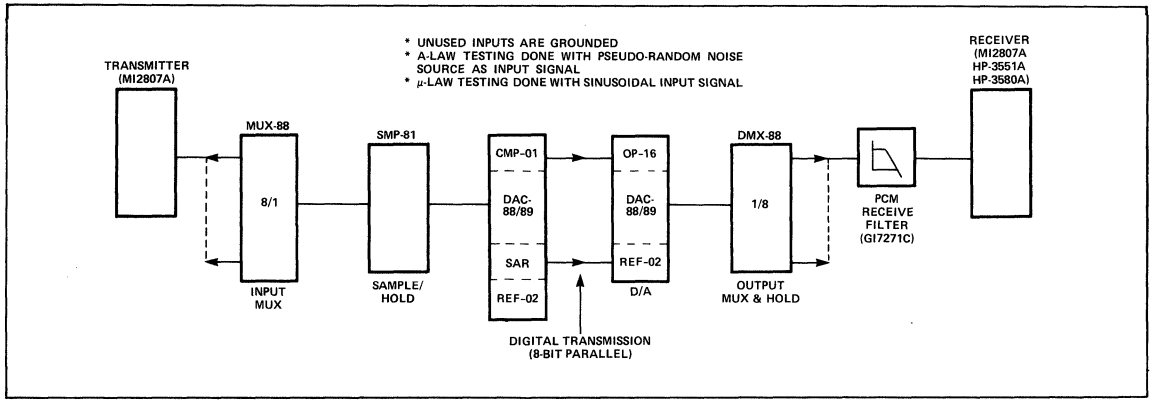


Figure 3. Test Configuration

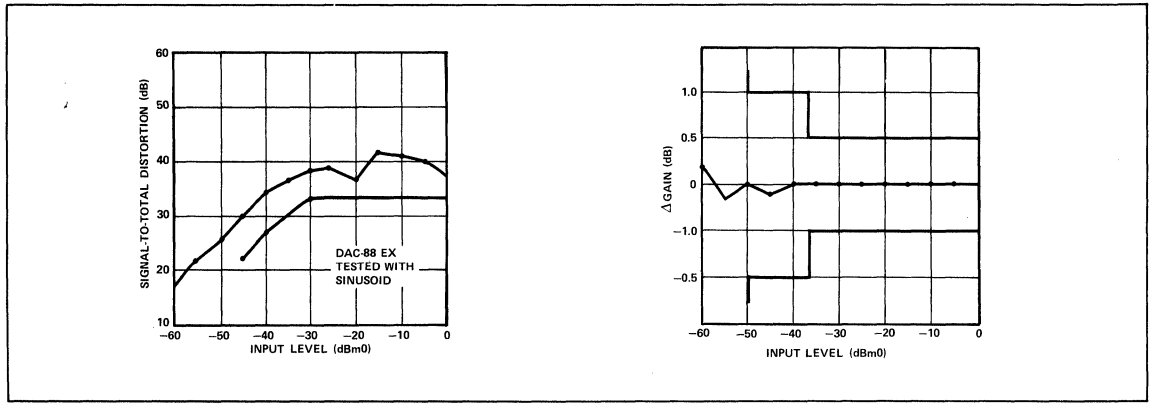


Figure 4. DAC-88EX Tested with Sinusoid

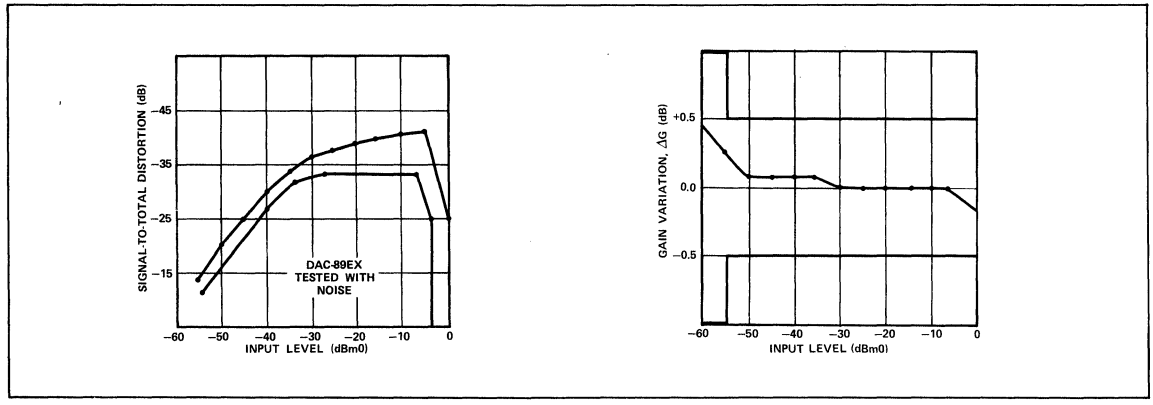


Figure 5. DAC-89EX Tested with Noise Source

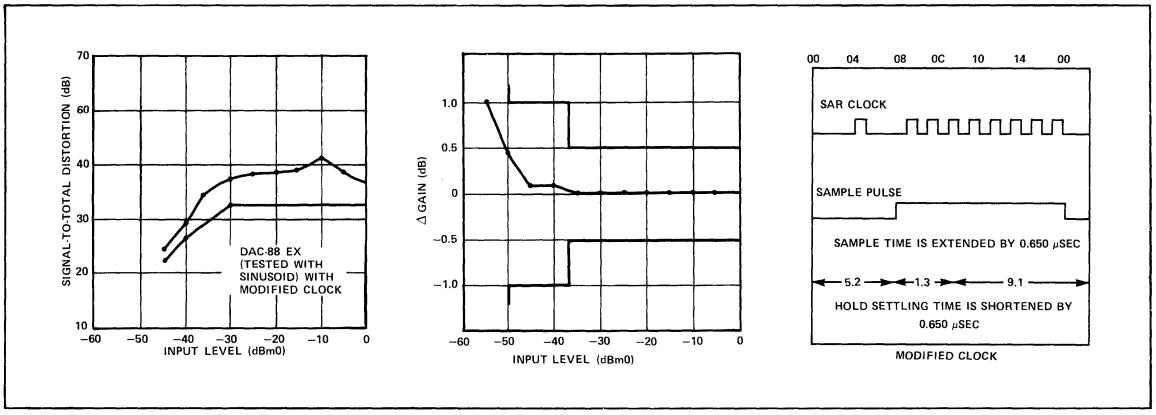


Figure 6. DAC-88EX with Altered Encode Clock (Reduced Hold Settling Time)

Comparisons of idle channel noise measurements using the MUX-88 and the DMX-88 are shown in Figures 7 and 8. It is important to notice that these measurements were made at the input to the PCM output filter. Collecting data at the filter output is not feasable because the noise values are too low for the equipment being used. To show the difference between the new and old components, a measurement was made that yielded some data. However, for both devices the idle channel noise is well within the normal system guidelines. The test data shows the difference due to reduced device charge injection of the DMX. Using a 10,000pF hold capacitor produces at least a 10dB improvement for the DMX and when the hold capacitor is reduced, the improvement is even more obvious. The smaller hold capacitor allows the D/A circuit to drive more channels. Since the current capability of the multiplexer switch is limited, a smaller capacitor means less charge-up time is required and a faster settling time is possible. The "demultiplexer" allows the user the option of reducing the hold capacitance without affecting the idle channel noise performance.

	CHANNEL MEASURED	IDLE CHANNEL NOISE	HOLD CAP
MUX-88	1	-60.8	10000pf
	2	-61.1	10000pf
	3	-60.3	10000pf
	4	-61.1	10000pf
	5	-60.9	10000pf
	6	-61.3	10000pf
	7	-61.2	10000pf
	8	-60.0	10000pf
DMX-88	1	All Values <-70dB	10000pf
	2		10000pf
	3		10000pf
	4		10000pf
	5		10000pf
	6		10000pf
	7		10000pf
	8		10000pf

NOTE: VALUES MEASURED BEFORE PCM OUTPUT FILTER WITH HP-3551A (-70dB IS LOWEST MEASUREMENT)

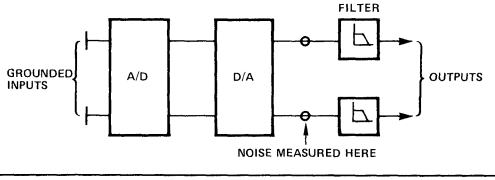


Figure 7. Idle Channel Noise

	CHANNEL MEASURED	IDLE CHANNEL NOISE	HOLD CAP
MUX-88	1	-57.2	1000pf
	2	-57.2	1000pf
	3	-57.2	1000pf
	4	-57.2	1000pf
	5	-57.2	1000pf
	6	-57.2	4300pf
	7	-57.2	4300pf
	8	-57.2	4300pf
DMX-88	1	-68.6	1000pf
	2	-68.6	1000pf
	3	-68.6	1000pf
	4	-68.6	1000pf
	5	-68.6	1000pf
	6	<-70	4300pf
	7	<-70	4300pf
	8	-69.9	4300pf

NOTE: MEASURED AS SHOWN IN PREVIOUS FIGURE.

Figure 8. Idle Channel Noise

Another demonstrator design change was added to show how additional reduction of crosstalk is possible through proper control of the output multiplexer. The first design did not make use of the enable function of the output switch. As a new digital word was latched to the decode circuit, the output MUX address was switched. The timing involved in these two sequences is such that some signal feedthrough is seen due to the data latch and D/A circuit (DAC-88/89 and OP-16) settling more quickly than the MUX switch can open. Performance is improved by the MUX being disabled prior to the analog channel being switched. This assures, by using lead CC, that the MUX is completely open while the new decoder output is settling. The MUX address is then switched and the MUX enabled. The timing of these signals is shown with the SAR clock in Figure 2. The crosstalk measurements are shown in Figure 9.

INPUT CHANNEL	MEASURED CHANNELS	CROSSTALK (1.02KHz)
1	4	-72
	3	-80
	2	-80
	8	-85
	7	-85
	6	-85
	5	-78
2	8	-72
	7	-80
	6	-85
	5	-85
	1	-85
	4	-84
	3	-85
3	2	-70
	8	-80
	7	-85
	6	-85
	1	-85
	4	-74
4	3	-72
	2	-78
	8	-82
	7	-85
	6	-85
	5	-80
	1	-75

- CHANNEL NUMBERS AS SHOWN ON ENCODER & DECODER BOARDS.
- INPUT LEVEL = 0dBm0
- MEASURED WITH HP3580A SPECTRUM ANALYSER.

Figure 9. Crosstalk

CONCLUSIONS

Thanks to the use of newly developed components, the PMI eight-channel CODEC demonstrator reveals the performance possible with a multiple channel digital transmission system. As illustrated by the test results, the transmission performance has been improved from that shown in AN-37. Moreover, the design is simpler and even more economical. Working with an eight-channel system allows the designer to investigate additional improvements in and advantages of the multiple-channel approach. Because of this, PMI makes a set of boards available (encoder, decoder, controller) to any customer interested in investigating the advantages to a shared-channel design.

The system is still the basic design presented in AN-37 and the work described in that note has aided in continuing improvement of PMI components. A complete demonstration system schematic is shown in Figure 10.

PMI is committed to providing telecommunication components capable of meeting and exceeding all requirements for digital switching and transmission systems. We feel the shared-channel approach provides economic and space advantages over the use of single-channel CODEC's in many designs. It has also been seen by several of our customers, that since our designs use individual components, by properly specifying these parts, the overall system performance can be guaranteed. This can provide savings in component and board-level testing costs. The system designer needs only to evaluate the PMI approach to become aware of the possibilities it holds in terms of digital transmission system design.

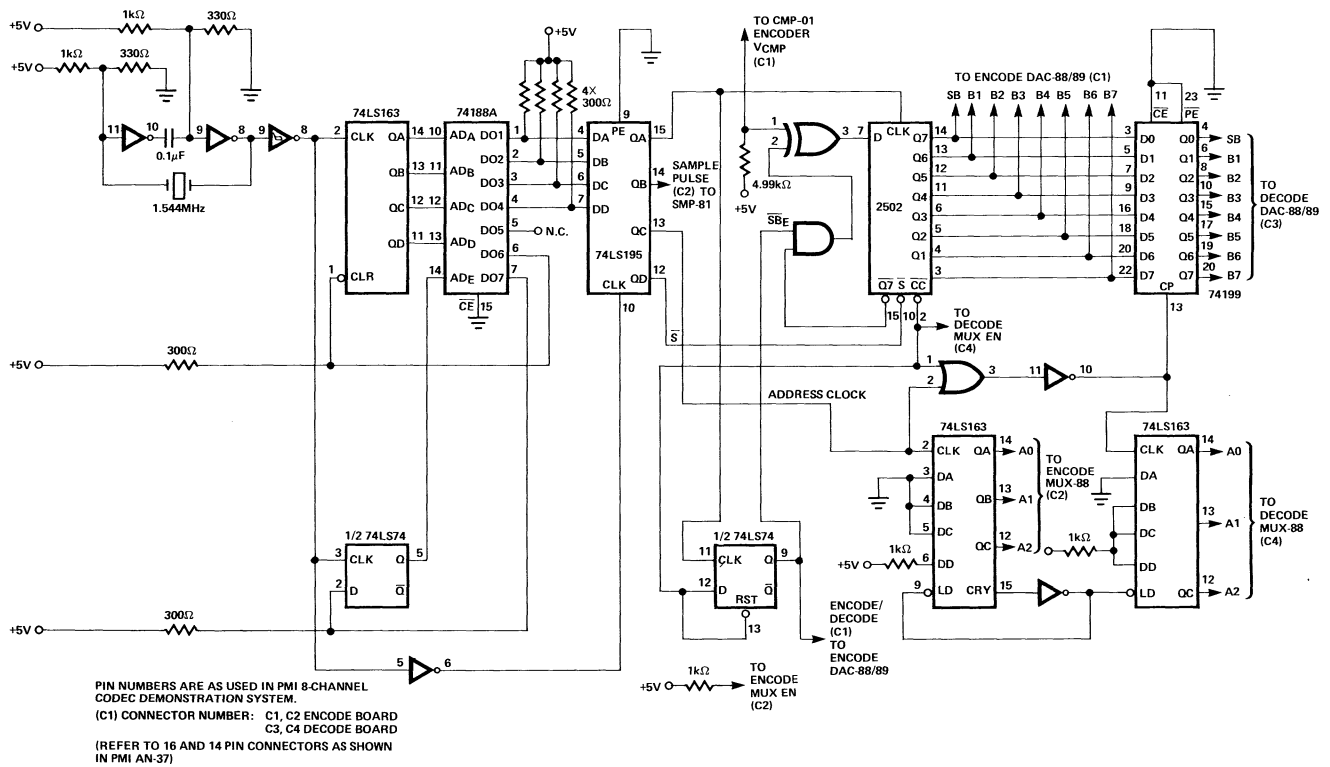


Figure 10A. CODEC Demonstration System Digital Control Board

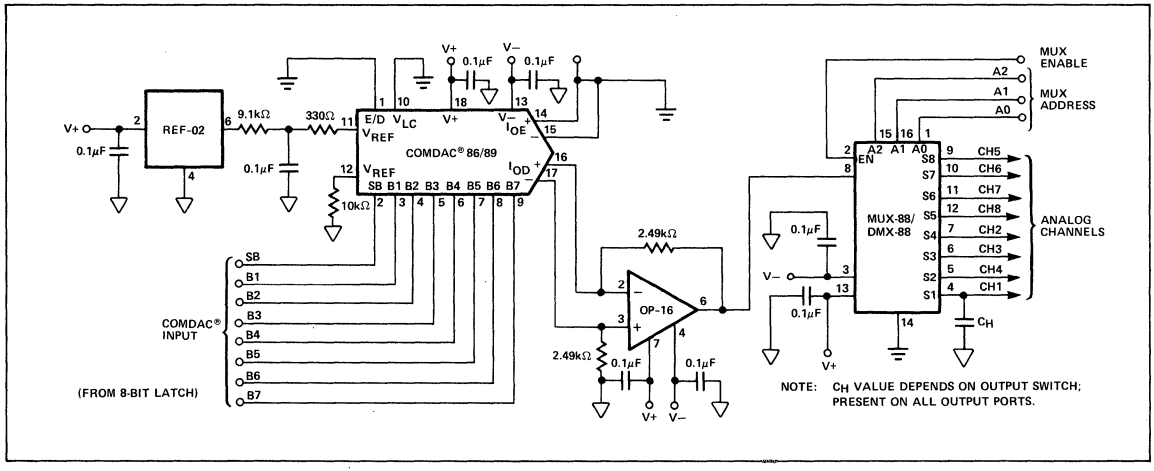


Figure 10B. Demo System Decode Board

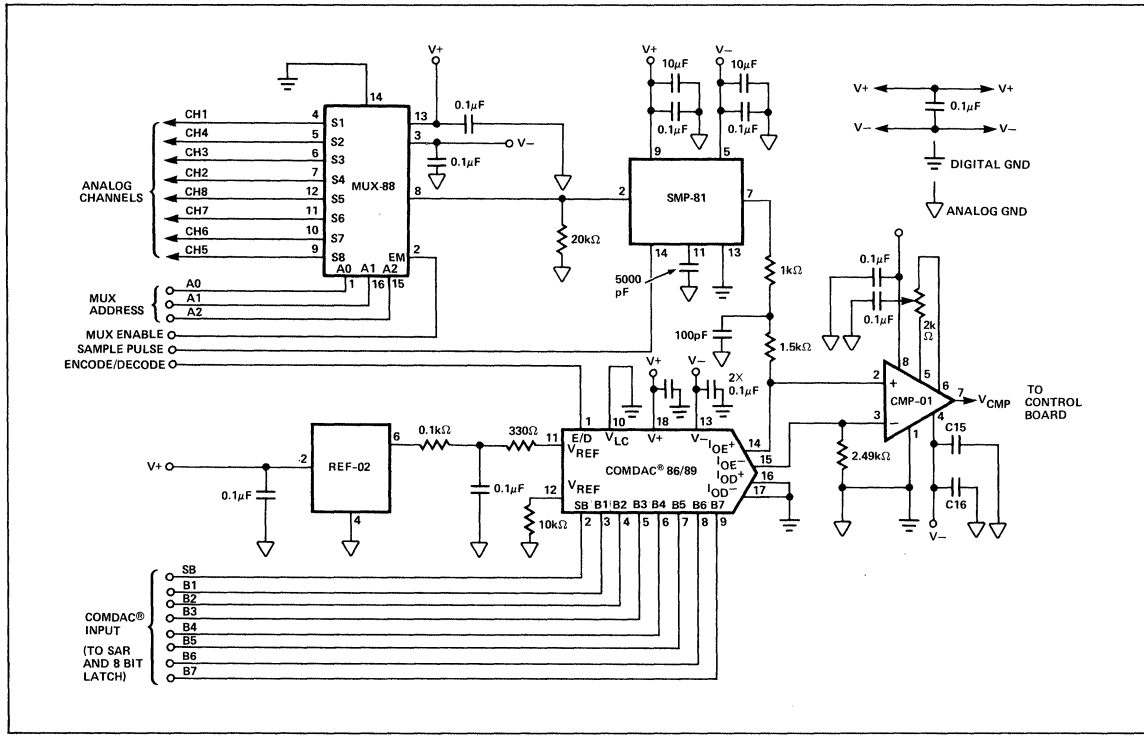


Figure 10C. Demo System Encode Board

The CCITT standards concerning line transmission include a specification demonstrating the relationship between the encoding laws (A-law or μ-law) and a standard audio signal level. The relationship is such that when a specific periodic sequence of character signals are applied to the appropriate decoder, the output will be a sine-wave signal at 1kHz with a nominal level of 0dBm0. The prescribed digital characters are those represented in Tables 1 and 2.

While developing the multiple-channel CODEC systems, it became useful to test the encoder and decoder portions of the circuit separately. To complete such tests, a CCITT-standard signal generator was produced. The generator consists of five TTL packages and is driven by an 8kHz signal. The required digital sequence is simple to implement as four of the outputs are constant values. For the remaining active bits, a four bit-binary counter was used to produce an appropriate sequence. As is shown in the schematic (Figure 3), the counter clocks from 0101 to 1100 and then repeats. This sequence directly provides the output for bits 4 and 6 and the inverted bit 8. With additional logic, the remaining bit, bit 1, is also available.

The usefulness of such a generator is seen first of all in trouble shooting any preliminary CODEC designs. Secondly, for PMI, it provided a small, easily transportable signal source to be used in PMI's eight-channel CODEC demonstration unit. Using the digital signal generator in conjunction with a PMI DAC-88 or 89 and an OP-16 provides a analog driver capable of producing the CCITT standard transmission signal. The completed signal generator schematic is shown in Figure 4.

Table 1. A-Law

Character Signals								Transmitted Characters*							
B1	B2	B3	B4	B5	B6	B7	B8	B1	B2	B3	B4	B5	B6	B7	B8
0	0	1	1	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	0	0	0	0	1	0	1	1	1	0	1	0	0
0	0	1	0	0	0	0	1	0	1	1	1	0	1	0	0
0	0	1	1	0	1	0	0	0	1	1	0	0	0	0	1
1	0	1	1	0	1	0	0	1	1	1	0	0	0	0	1
1	0	1	0	0	0	0	1	1	1	1	1	0	1	0	0
1	0	1	0	0	0	0	1	1	1	1	1	0	1	0	0
1	0	1	1	0	1	0	0	1	1	1	0	0	0	0	1

*Transmitted Characters for A-LAW are obtained by inverting even bits of Character Signals.

Table 2. μ-Law

Character Signals								Transmitted Characters*							
B1	B2	B3	B4	B5	B6	B7	B8	B1	B2	B3	B4	B5	B6	B7	B8
0	0	0	1	1	1	1	0	1	1	1	0	0	0	0	1
0	0	0	0	1	0	1	1	1	1	1	1	0	1	0	0
0	0	0	0	1	0	1	1	1	1	1	1	0	1	0	0
0	0	0	1	1	1	1	0	1	1	1	0	0	0	0	1
1	0	0	1	1	1	1	0	0	1	1	0	0	0	0	1
1	0	0	0	1	0	1	1	0	1	1	1	0	1	0	0
1	0	0	0	1	0	1	1	0	1	1	1	0	1	0	0
1	0	0	1	1	1	1	0	0	1	1	0	0	0	0	1

*Transmitted Characters for μ-LAW, all bits are inverted.

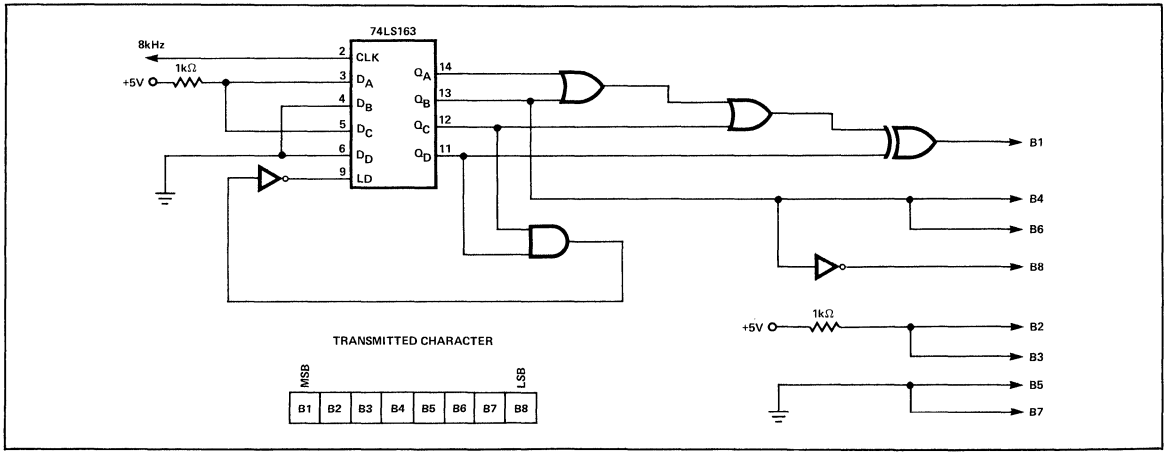


Figure 3. Character Generator

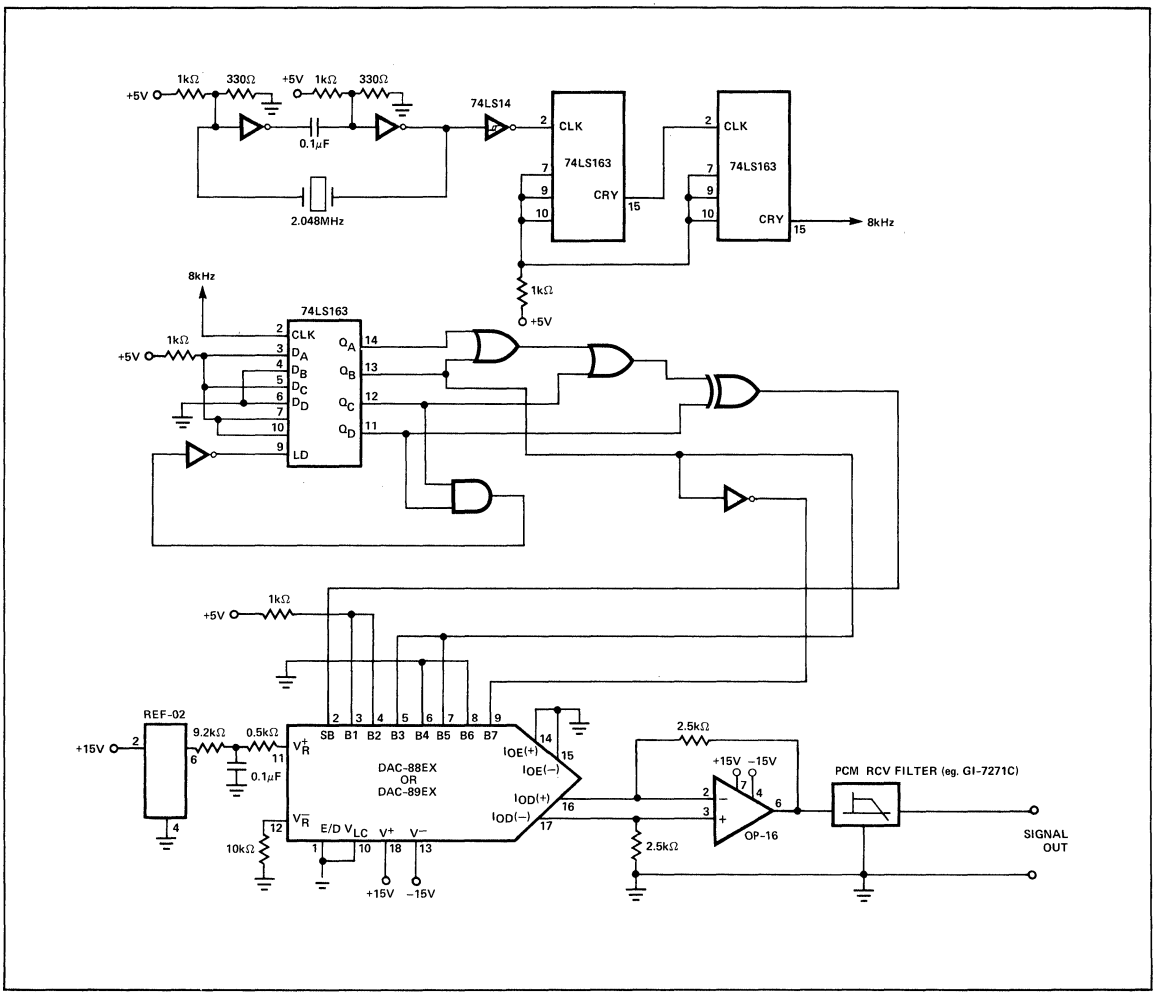


Figure 4. 1kHz, 0dBm0 Sine-Wave Generator

PMI

AN-47

BCD DAC MAKES PROGRAMMING OF FUNCTION GENERATOR SIMPLE

Precision Monolithics Inc.

APPLICATION NOTE 47

Providing analog instrumentation and signal processing systems with the capability to be digitally programmed is becoming increasingly important for two reasons. The first is compatibility with automated digital control systems using microprocessors or general-purpose interface Bus systems. The second reason, unrelated to automation, is the need to reduce errors that result from operator adjustments of equipment.

A conceptional view of analog control (using a potentiometer) and digital control (using a digital-to-analog IC) is depicted in Figure 1. Linear control of the analog function can be achieved through control of absolute voltage, differential voltage or current. Configurations for each of these control modes are shown in Figure 2. For maximum flexibility in applying digital control to a system, a current output DAC, such as the popular DAC-08, or the BCD DAC-20 should be used.

Use of a DAC in analog conditioning or signal processing systems can be a problem if the linear output of the DAC elicits a nonlinear response from the system. To add digital programmability to the system, the designer must begin with a linear system unless, of course, a log or other nonlinear response is desired.

An instrument that can be significantly enhanced by the inclusion of a BCD DAC in its circuitry is the ubiquitous function generator. A single-chip function generator, such as the 8038, can provide sine, triangle, and square-wave outputs at very low cost. The 8038 can operate over the 0.001Hz to over 100kHz range and through three outputs can deliver square, triangular and sine waveforms simultaneously.

In conjunction with a DAC-20 (a two-digit BCD DAC) and a few additional components, the 8038 can be used to design a function generator having 2% frequency linearity and providing both digitally programmable output and logarithmic sweep.

At first glance, the circuit shown in Figure 3 appears to provide the designer with digital control capability. In this circuit, the 8038 is programmed by the voltage differential between V_{CC} and V_{IN}. Unfortunately, the performance of the 8038 is not sufficiently linear to allow this simple interface arrangement to work. A linearization circuit must be added.

The linearization requirements of the 8038 can best be grasped by examining and understanding the way it functions. Initially, the 8038 generates a triangular wave which is then used in the derivation of the sine and square waveforms. The triangular wave is formed by two voltage-controlled current sources (VCCS), equal to I_1 and $2I_2$. One of the current sources (I_1) is always on; the other one ($2I_2$) is switched, so that an external capacitor is alternately charged and discharged.

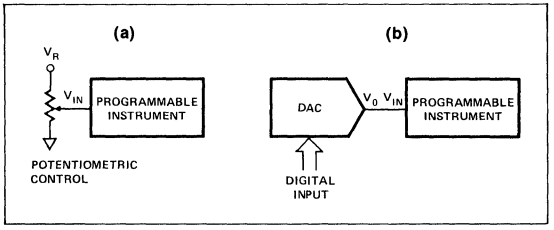


Figure 1. Simplified Representation of Analog and Digital Control: (a) Potentiometric Control; (b) Digital Control.

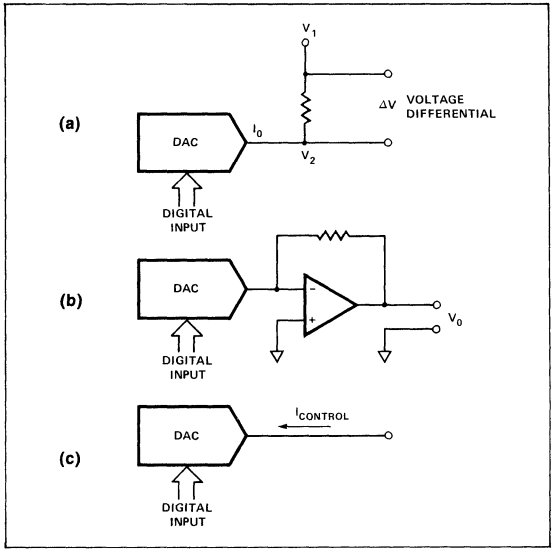


Figure 2. Control Configurations: (a) Differential Voltage Control; (b) Ground-Referenced Voltage Control; (c) Current Control.

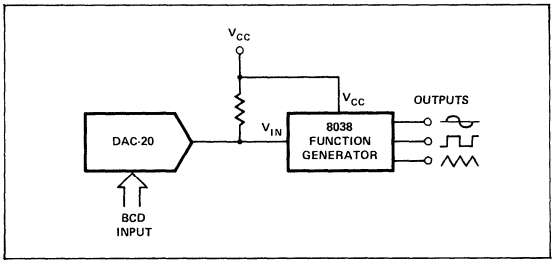


Figure 3. Basic Digital Control Configuration Using DAC-20 and 8038 Function Generator IC.

A simplified circuit diagram for the 8038 VCCS is shown in Figure 4. The VCCS output is given by:

$$I_1 = \frac{V_{IN} + V_{BEQ1} - V_{BEQ2}}{R_A} \quad (1)$$

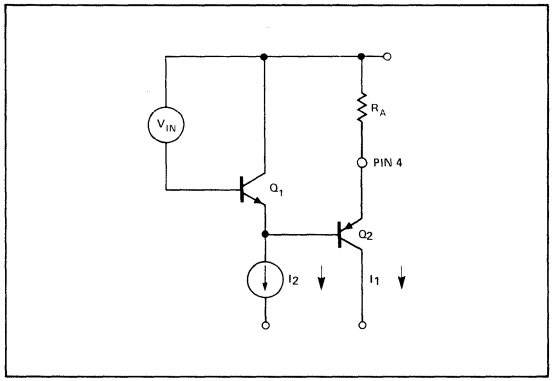


Figure 4. Simplified Circuit Diagram for the 8038's Voltage-Controlled Current Source.

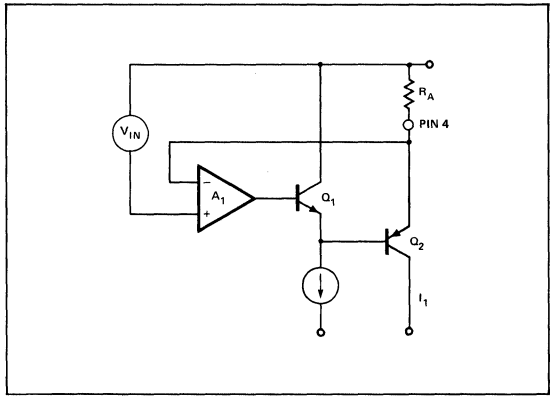


Figure 5. Improved VCCS with Added Feedback Amplifier.

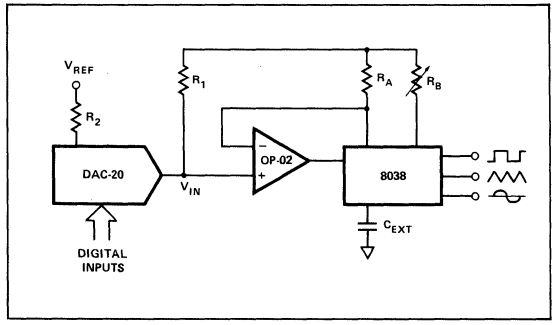


Figure 6. Digitally Controlled 8038.

This current source is not linear enough for the digital programming because V_{BEQ2} varies with I_1 while V_{BEQ1} does not. Adding a feedback amplifier to the VCCS, as shown in Figure 5, makes the output very linear by forcing the voltage at Pin 4 to equal V_{IN}, so that the VCCS output is simply:

$$I_1 = \frac{V_{IN}}{R_A} \quad (2)$$

The excellent linearity of the current source permits the output frequency (f_{out}) of the 8038 to be controlled by the DAC as shown in Figure 6. The digital inputs to the DAC set the voltage at point V_{IN}, and thereby control the output frequency of the 8038. R_A and C_{EXT} set the frequency range of the 8038 and R1 and R2 set the increment at which the frequency changes (although there are two current sources, the lowest sine wave distortion is obtained when $I_1 = I_2$; therefore, only R_A need be considered in calculating f_{out}).

The internal comparators of the 8038 limit the triangle wave amplitude to 1/3 V_{CC}. If $I_1 = I_2$ so that rise time = fall time, and $I_1 = V_{IN}/R_A$, then

$$f_{out} = \frac{-V_{IN}}{2/3\ V_{CC}\ R_A\ C_{EXT}} \quad (3)$$

The voltage at the output of the DAC-20 is given by:

$$V_{DAC} = V_{IN} = \frac{V_{REF}}{(R2)} \times \frac{N}{100 \times R1,} \quad (4)$$

where N is a two-digit BCD number. The most significant digit of the DAC-20 (comprised of four binary bits) can overrange to hexadecimal F (equivalent to decimal 15) so that N can range from 1 to 159.

The complete function generator schematic is shown in Figure 7. The component values listed will control the 8038 output from 100Hz to 15,900Hz, which covers almost all of the audio range. (Note that a 00 input should halt the generator; however, leakages and offsets keep the generator operating — in a bread-board version, the output was 19Hz.)

S_1 and S_2 are hexadecimal and decimal thumbwheel switches, respectively, for setting the desired frequency. Frequency linearity is excellent with f_{out} within 2% of programmed value over the entire frequency range. Sine wave distortion can be adjusted to less than 1%, and varies less than ±0.2% over the output range.

The Precision Monolithics REF-02 supplies a very stable reference voltage to R3, which sets the DAC-20 full scale current at 3.18mA. R1 converts the DAC output current to a voltage at the noninverting input of the OP-02, which then sets the f_{out} of the 8038. D1 and R6 protect the 8038 input from transients during power supply turn-on and C1-R5 roll off the op amp loop.

Since the DAC-20 has a high-compliance current source output, an external voltage source can be applied at V_{IN} if external control of f_{out} is desired. A modulating voltage can also be capacitively coupled into V_{IN} to provide a frequency-modulated output. Another way of modulating would be to apply the external signal to the DAC reference input to modulate the reference voltage.

Calibration of the generator is straightforward. Since the 8038 symmetry adjustments affect frequency, these are performed first. With a digital word of F9 (HEX) applied to the DAC, RB2 is adjusted for one 50% duty cycle square wave output and R13 and R14 adjusted for lowest distortion sine wave. Then, with a DAC input of 01, R11 is adjusted for a 50% duty cycle square wave and R7 for f_{out} = 100Hz. Finally, with a DAC input of A0, R2 is adjusted for f_{out} = 10kHz and the calibration is complete.

For audio testing, a generator with logarithmic sweep is very desirable. The addition of only 3 IC's provides log sweep as well as programmable counters on the input of the DAC-20. When S3 is open the oscillator will produce 16 cycles at each frequency step, producing a logarithmically related sweep. The log nature of the sweep is shown by the controlling equation for the counter.

$$\text{Count} = \int \frac{f_O}{16}\, dt$$

but the frequency out, f_O, is proportional to the count

$$f_O = 100 \text{ count}$$

$$\frac{f_O}{100} = \int \frac{f_O}{16}\, dt \quad \text{or} \quad f_O = \frac{16}{100}\,\frac{df_O}{dt}$$

When S3 is closed, the 74192 and 74193 counters act as transparent latches, so that thumbwheel switches S1 and S2 can be used to program f_{out}.

Microprocessor control of the generator is very simple since the DAC-20 is compatible with all logic families. Any CMOS, NMOS, or bipolar output device will drive the DAC-20, or a memory write pulse can be used to latch data into the counters (Figure 9). If the counters are used with µp control one bit of an I/O port or an external switch must be used to select swept or programmed output.

The "intelligence" added to this instrument by DAC control allows operation from µp or thumbwheel switches and permits easy interface to the IEEE 488 bus with the popular GPIB chips.

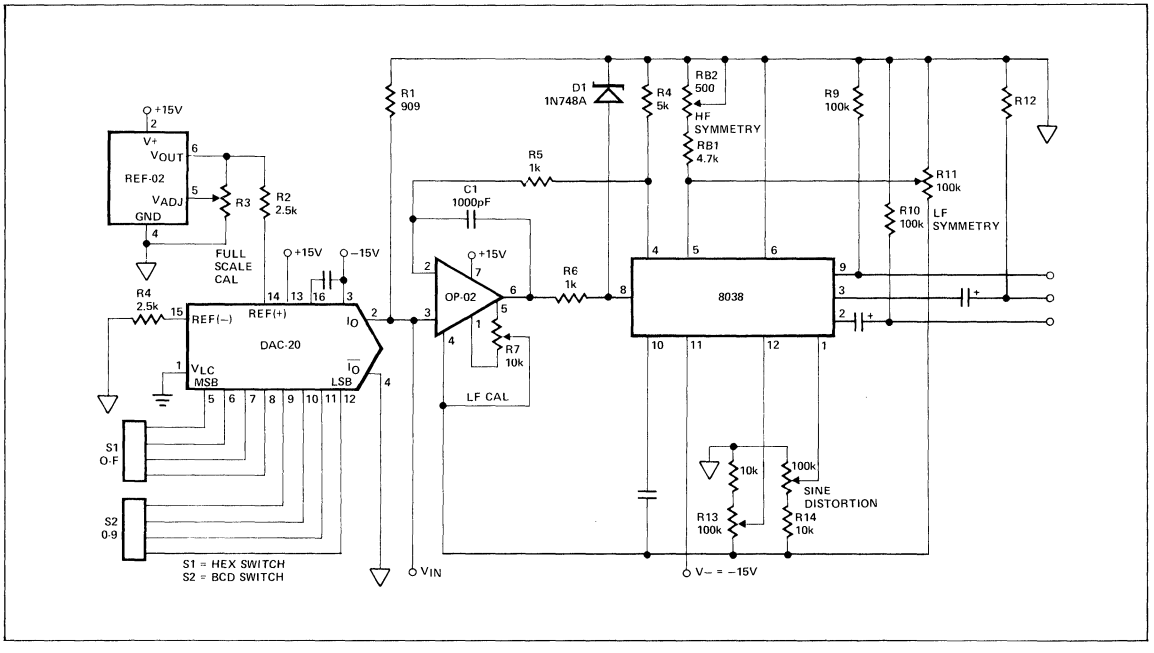


Figure 7. Complete Circuit Diagram for Programmed Function Generator.

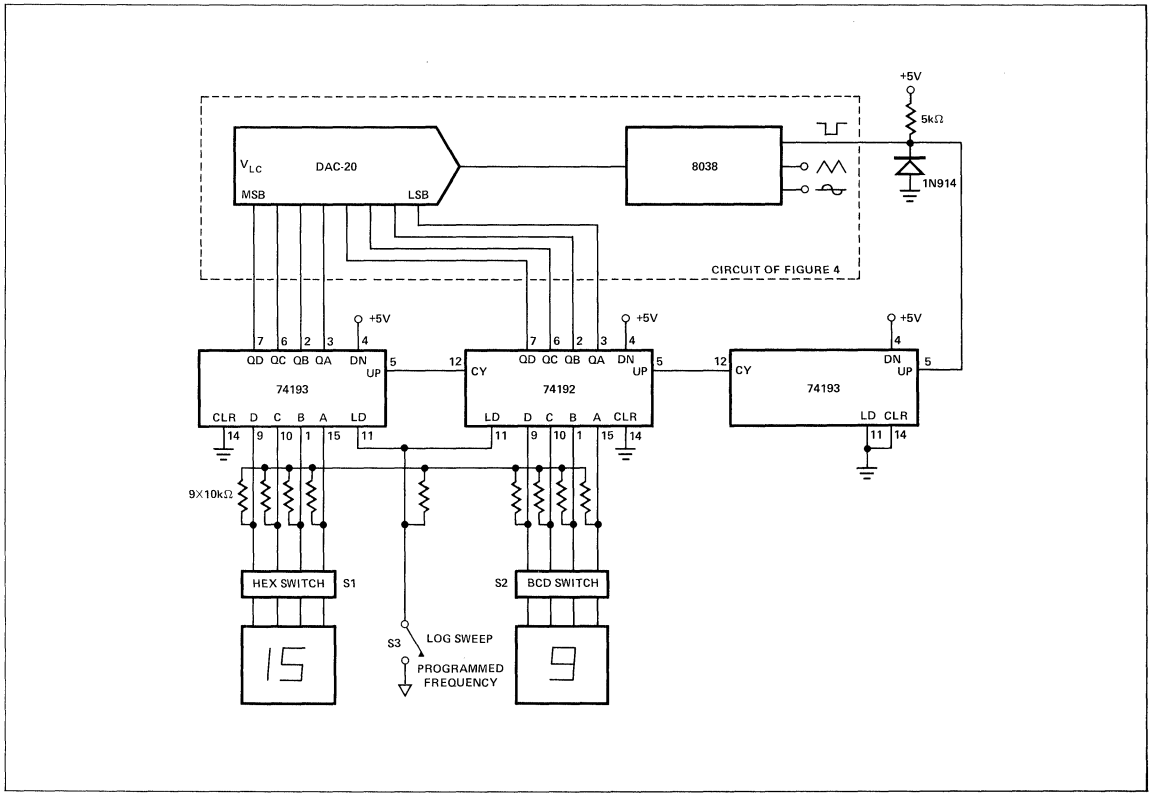


Figure 8. Log Sweep Modification of Programmable Function Generator.

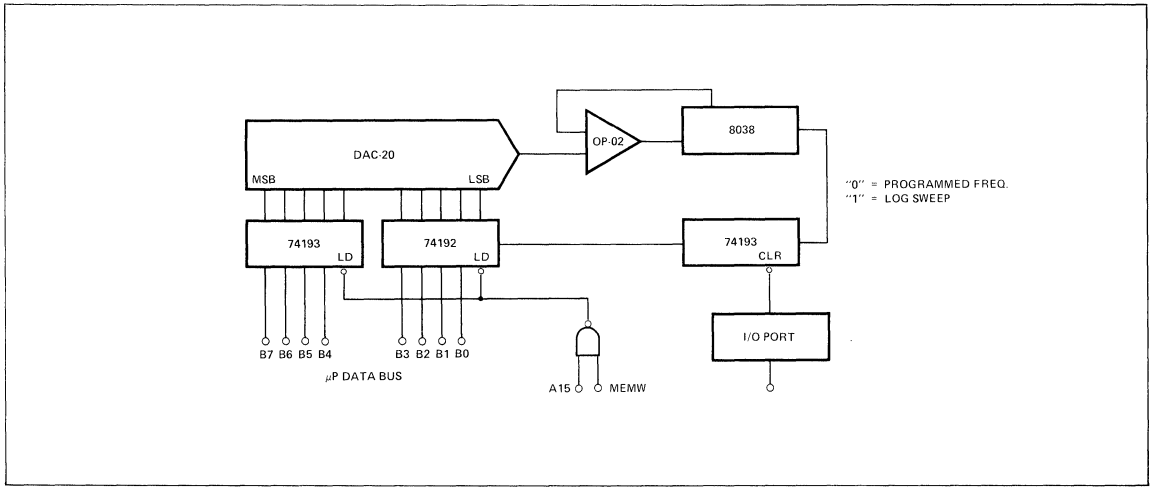


Figure 9. Microprocessor Interface to Function Generator with Software Selectable Sweep.

AN-48

DESIGNING DIGITAL REPEATERS WITH ICs

Precision Monolithics Inc.

APPLICATION NOTE 48

This note describes the use of the RPT-82 and the RPT-83, PCM carrier repeater integrated circuits, which perform all of the active functions required for a regenerative repeater operating at 1.544-2.048 Megabits per second (Mbps) data rates on PCM lines.

Most of the problems in digital voice transmission are caused by the transmission medium itself rather than by the transmit or receive hardware.

This is particularly true for the most commonly used medium, twisted-pair cable designed to carry analog voice-frequency signals in the 300- to 3700-Hz frequency range.

As more and more transmission routes are called upon to accommodate digital data, it becomes important, in terms of system cost and installation time, to use existing cable interchanges. As a result, audio-frequency-grade cable is called upon to transmit high-speed digital data. This was made possible through the development of digital regenerators.

A digital regenerator consists of two repeaters, one in each transmission direction. Repeaters receive digital data streams and retransmit them to the next receiver position. Current integrated-circuit repeaters eliminate the loading coils that were originally used to introduce a flat-band response over the voice band. A T1 repeater (the U.S. standard) can accept a degraded signal, regenerate it, retime the pulse stream, and transmit it over another 6000 feet of twisted-pair cable. The action taking place in the regenerative repeater stage is depicted within the dashed-line portion of Figure 1. When digital carrier repeater circuits are installed, the operating error rate for carrier systems with audio-grade cable pairs is well within the limits necessary for adequate voice communication.

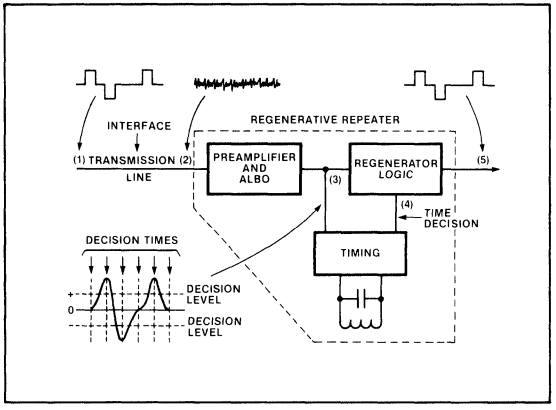


Figure 1: The functional elements of a regenerative repeater section are shown within the dashed line. The results being a re-shaping of the incoming pulses, which in turn enables a re-timed and regenerated data stream.

Several different integrated circuits are being used in the latest generation of repeater equipment. These circuits have cut the number of components required to build a digital regenerator while improving its capabilities and performance.

To grasp the concepts concerning use of the devices, it is helpful to first examine some of the basic theories relating to practical digital transmission.

The present T1 carrier uses bipolar or mark inversion digital format shown in Figure 2. There are several specific advantages provided by this coding system.

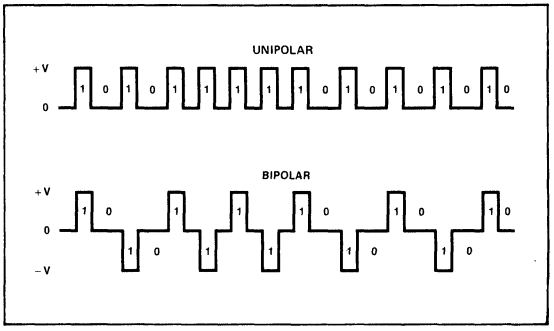


Figure 2: In the bipolar (alternate mark inversion) digital format, alternate 1 bits are inverted in polarity.

First, the maximum energy of the waveform is found at one-half of the bandwidth (data-transmission rate) of the system. For a binary code (see Figure 3), the most significant frequency is found at the zero level rather than the mid-frequency. This means that the energy spectrum encompasses double the bandwidth (3.088 MHz) of the transmission rate for the T1 rate. The bipolar scheme keeps the spectrum within the 1.544-MHz bandwidth of the transmission system.

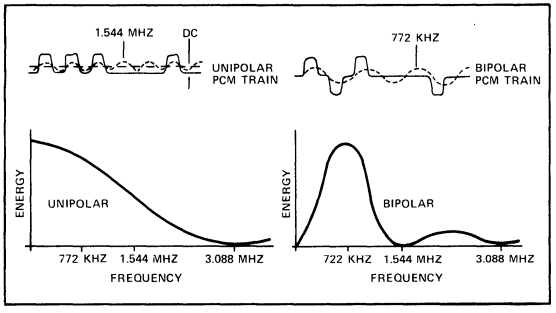


Figure 3: The (alternate mark inversion) bipolar digital format keeps the spectrum within the 1.544MHz bandwidth of the transmission system. The average dc component on the transmission pair is zero.

Another important characteristic of a bipolar code is that the average dc component on the transmission pair is zero. This is important in regenerator development because it allows the same channel to be used for data transmission and power supply. An advantage of this design approach is that extra pairs for powering a repeater location are not necessary with a simplex power arrangement.

Still another advantage provided by bipolar code is the capability to detect single-bit errors within the transmitted data. Since the sequence of pulses has alternating polarity, the absence of a pulse will be received as a bipolar violation. Though error bursts could produce incorrect error counts, it has been purported that the difference between the true error rate and measured error rate is negligible in high-error channels.

If the error rate is low enough to show differences for burst-error occurrences versus single-error counts, the channel will probably be performing well enough to make the difference unimportant.

There are also some problems associated with bipolar coding. For example, since retiming depends on the incoming pulse stream, a long series of zeroes will have a very low energy content. Some oscillator-resonant circuit designs may then damp out completely and fail to restart. This will depend on the Q of the circuit.

Some carrier designs have moved to different coding schemes to restrict the number of zeroes possible in a legal transmission. In European systems especially, the HDB3 code (high-density bipolar with no more than three zeroes in succession) has often been incorporated. In this discussion, however, the straight bipolar coding scheme will be considered when determining the relationship of the active components within the repeater.

The functional components of a repeater integrated circuit are illustrated in Figure 4. The repeater amplifies the incoming signal and equalizes the received signal to compensate for attenuation distortion and phase distortion. The analog amplifier also has a feedback loop that provides for a variable amplification dependent on the threshold detected for the incoming pulses (either positive or negative). Either of two methods can be used to obtain equalization: in the first approach, a fixed value of cable attenuation is provided; in the second approach, automatic equalization can be used with constant modification taking place to handle variable line lengths in that transmission section. The monolithic approach provides an equalization network and variable line matching circuitry.

The repeater must provide a timing-recovery circuit to extract the data transmission clock from the incoming pulse train. The recovery circuit will normally comprise a resonant circuit tuned to the peak energy level of the incoming signal. The resonant circuit is "energized" by the transitions at the received channel with the resonant frequency dependent on the Q of the circuit. A higher Q can allow the circuit to remain active through longer periods of zero signals levels. The recovered timing pattern is then used in the reproduction of the incoming series of pulses.

The repeater must be capable of differentiating between a data pulse and channel noise. The noise due to adjacent channel pairs or interference due to signals in adjacent time slots must not negate the reception of the proper incoming pulse sequence. Jitter due to timing variations from repeater section to repeater section can disrupt the signal detection

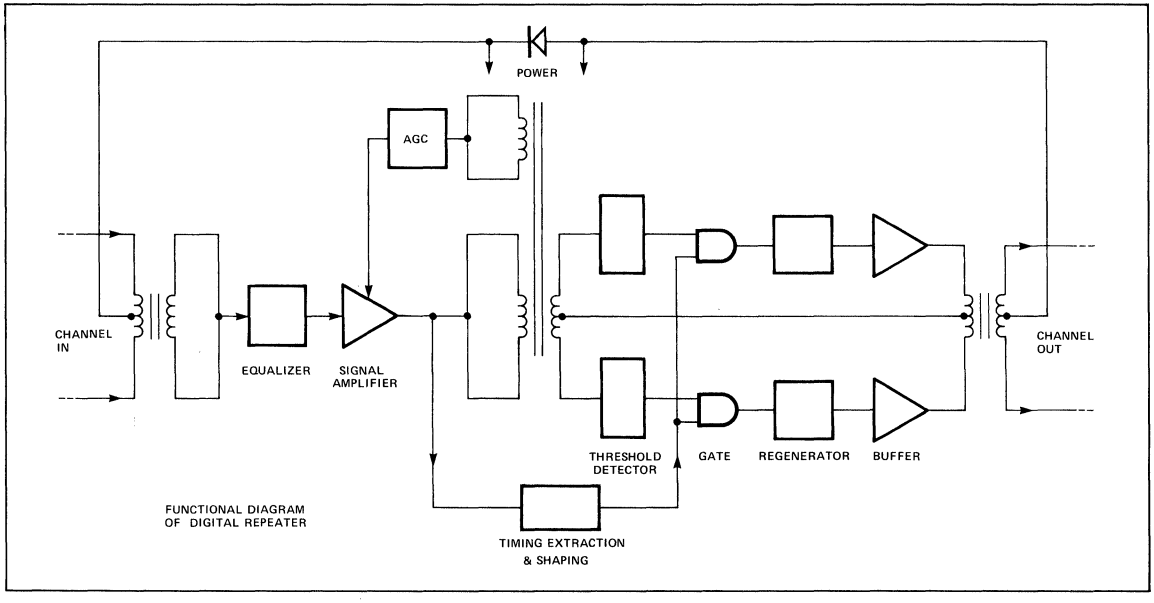


Figure 4: Functional diagram of a repeater integrated circuit shows the equalizer (to compensate for attenuation and phase distortion) and analog amplifier with feedback to provide variable amplification dependent on the detected threshold.

by causing pulse thresholds to be measured at the improper intervals. Pulse detection is accomplished by the detection of proper threshold levels and correct timing intervals. The repeater then will retime the detected levels to provide for a new pulse train. It is important when retiming the waveform that the input from the threshold detector precede the timing strobe. This ensures that the output pulse will follow the reconstructed timing, reducing the jitter components.

The final functional block necessary for the complete repeater function involves the regeneration of the output pulses. The buffer stages drive the output transformer to produce a posi-

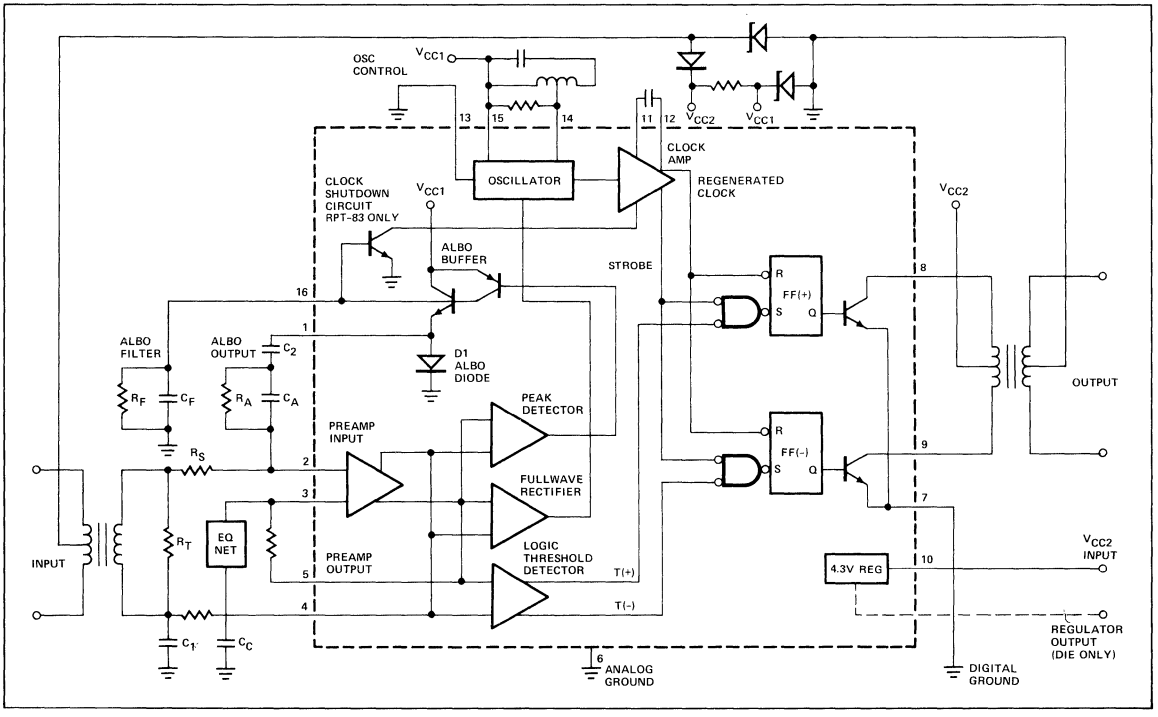


Figure 5: In PMI's RPT-82 and RPT-83, equalization and amplification of the incoming pulse train takes place through an amplifier with an external network controlled by feedback.

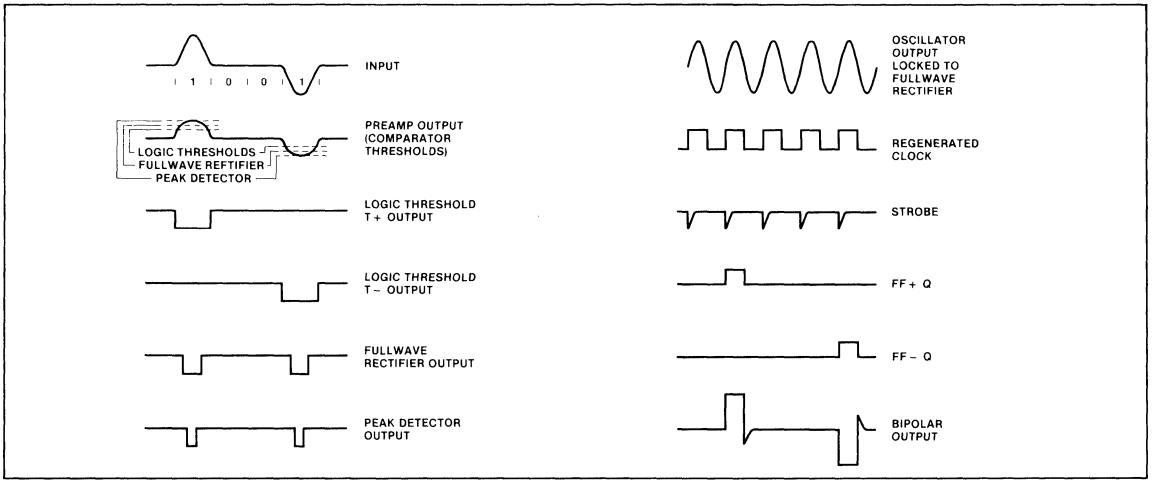


Figure 5A: Voltage waveforms at the outputs of the various functional blocks within the RPT-83 integrated circuit. The output pulses of the amplifier trip some combination of the level-detecting comparators.

tive or negative signal on the channel output pair. The design is such that, in most instances (U.S. and European), the generated signals are nominally square pulses. Different theories as to improving performance by band-limiting the output stage have been discussed and, in some instances, implemented. However, the majority opinion still seems to favor the square-wave components.

The repeater can be considered a combination of discrete yet interrelated functions. The overall function of the repeater is the shaping of incoming pulses, the retiming of these pulses, and the generation of an equivalent output stream.

IC APPROACH

In PMI's RPT-82 and RPT-83, the equalization and amplification of the incoming pulse train is achieved through a bipolar amplifier with an external equalization network controlled by feedback from the amplifier outputs (Figure 5). The result is that the pulses peak so the majority of the pulse amplitude is restricted to its own time slot.

The automatic attenuation of the pulses is done by an ALBO (automatic line build-out) circuit actuated through a buffer circuit on chip. The output pulses of the amplifier will trip one or all of the three level-detecting comparators. In terms of the ALBO feature, if the incoming pulses exceed a specified peak-reference value, the comparator generates current pulses that flow into the ALBO filter external to the chip and charge capacitor C_F.

The voltage at the ALBO filter is applied, in turn, to the base of the internal ALBO buffer transistor. The buffer will turn on when its base voltage exceeds approximately 1.7 volts. This 'ON voltage' is also specified in the electrical characteristics of both the RPT-82 and RPT-83. The ALBO diode acts as a series impedance, normally much larger, and therefore the dominant factor, than the shunt impedance of the external network. As the current increases at the buffer, the diode impedance decreases and the shunt impedance becomes dominant.

The overall effect is to increase the ALBO attenuation as the filter voltage level increases. The result is that the feedback loop will adjust itself until the pulses out of the preamplifier are equal to the fixed reference. The references for the other level detector and rectifier are set at fixed ratios of this peak reference. Therefore, their thresholds are fixed with respect to the pulse shape and relative amplitude.

On the RPT-83 (not the RPT-82), a clock shutdown circuit, which is activated by the current levels from the ALBO buffer, is also provided. This shutdown circuit turns off the clock amplifier at low input levels, thus neither the regenerated clock nor the strobe outputs are enabled at the output buffer flip-flops. The circuit was incorporated to prevent random-noise pulses from being reproduced as valid output pulses. The problem, however, can be that at long line lengths the correct signals are too low in energy to activate the clock circuit. Presently, PMI has customers using both schemes in their repeater designs.

The timing of the circuit is based upon the pulsing of a resonant tank circuit. The full-wave-rectifier comparator output pulses the tank network. The pulses try to "force" the oscillator circuit to phase lock to the incoming pulse waveform, while the tank attempts to resonate at its preset (with external components) frequency. The result of the two factors is a clock circuit that runs at an average bit rate for the incoming waveforms.

Again, the value of Q for the tank circuit will help determine the oscillator accuracy. If the Q is high, the resonant frequency dominates and it is more difficult to phase-lock to the incoming pulse rate. A high Q circuit also changes considerably with the temperature and long-term component drift. A Q value that is too low will cause adverse affects on the oscillator circuit by the jitter present in the pulse stream. This means the jitter will then also be transferred to the output pulse train as well. For both the RPT-82 and RPT-83, Qs of greater than 75 are recommended.

The logic-threshold comparator provides the detection function for incoming pulses. For positive received pulses, a negative pulse is generated on the T+ line; for incoming negative pulses, a pulse is sent on the T– line. The clock amplifier "squares" the timing waveform from the oscillation circuit and produces a square clock signal and a negative strobe pulse. The strobe pulses are 'ANDed' with the logic outputs (T+ or T–) to set the output buffer flip-flops.

The strobe is coincident with the positive edge of the clock signal generated by the tank circuit. Once the appropriate flip-flop is set by the combination of the logic output and the strobe pulse, the output driver stage causes current to flow through the proper half of the output transformer, thus regenerating the received bipolar pulse. The falling (negative) edge of the internal clock signal serves to reset the output flip-flops and thereby terminate the output pulse. This is important to prevent the regenerated waveform from following the data threshold instead of the clocking circuit.

One option is made available to users of both the RPT-82 and the RPT-83. The internal clock oscillator can operate in either an injection-locked mode or a pulsed-tank mode. By grounding a pin on the device, the oscillator is free-running but is phase-locked to the full-wave rectified output. With the pin open, the oscillator will only operate when pulsed by an incoming signal. The circuit then "rings" until the next incoming pulse is received from the rectifier. In both cases, the overall effect is to phase-lock the resonant circuit to the average frequency of the pulse train.

The completed T1 repeater may look something like Figure 6 in a typical configuration. The input transformer provides a two-to-one step-up from the 100-ohm characteristic impedance of the line. The matching impedance, in this case, is doubled to approximately 400 ohms. A fixed attenuation is added to provide a fixed line build-out of approximately 6dB. The automatic build-out then provides a varying attenuation for line lengths up to 36dB.

The equalization network is added to give the preamplifier higher gains at higher frequencies. This compensates for the roll-off characteristics of the preamp and the transmission line.

The oscillator tank circuit provides the resonant frequency for the oscillator. It is controlled by current pulses generated as the incoming waveform is received.

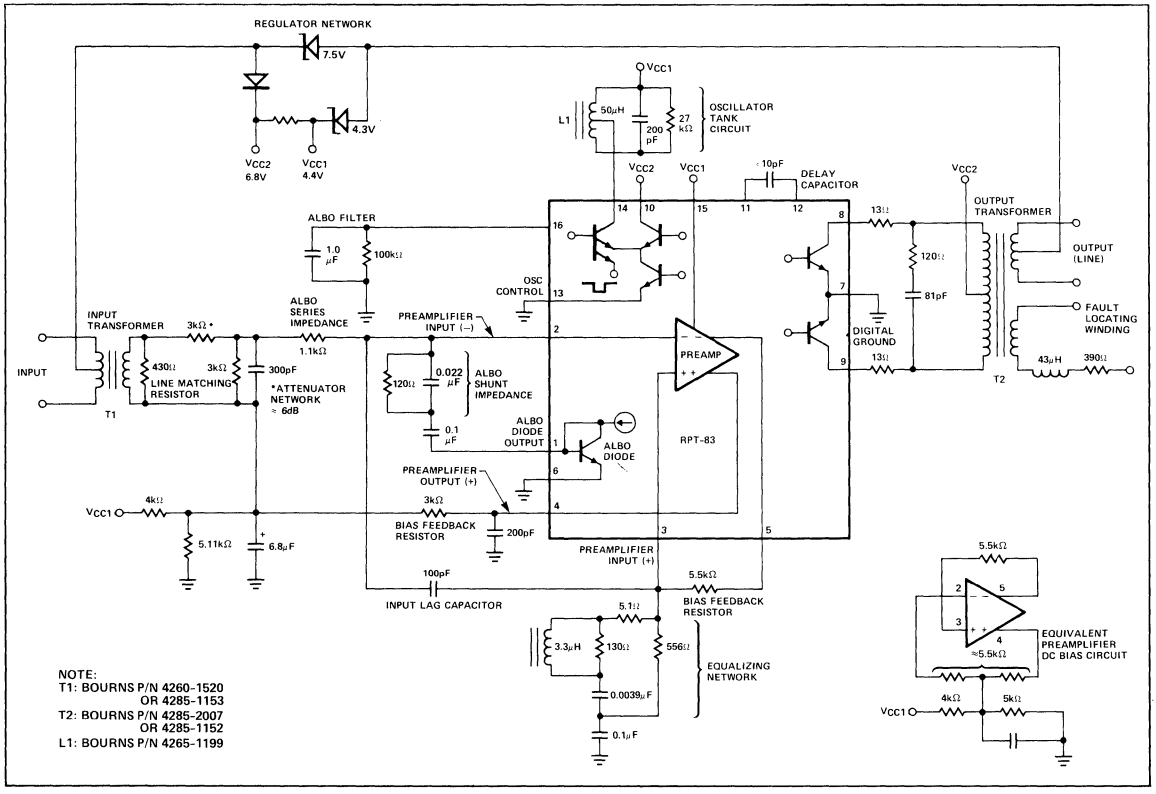


Figure 6: The complete T1 repeater system (1.544MHz) using the RPT-83 integrated circuit. The input transformer provides a 2:1 step-up from the 100 ohm line impedance.

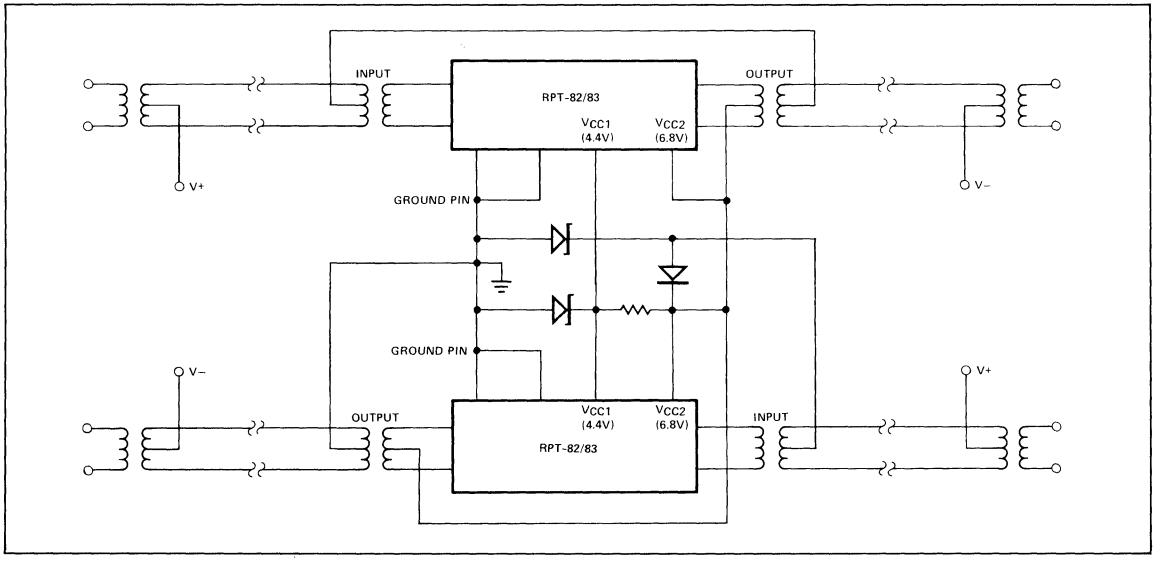


Figure 7: The simplex power supply design consists of two zener diodes and a diode float connected to the center taps of the line transformers. Nominal voltages are 4.4 and 6.8V.

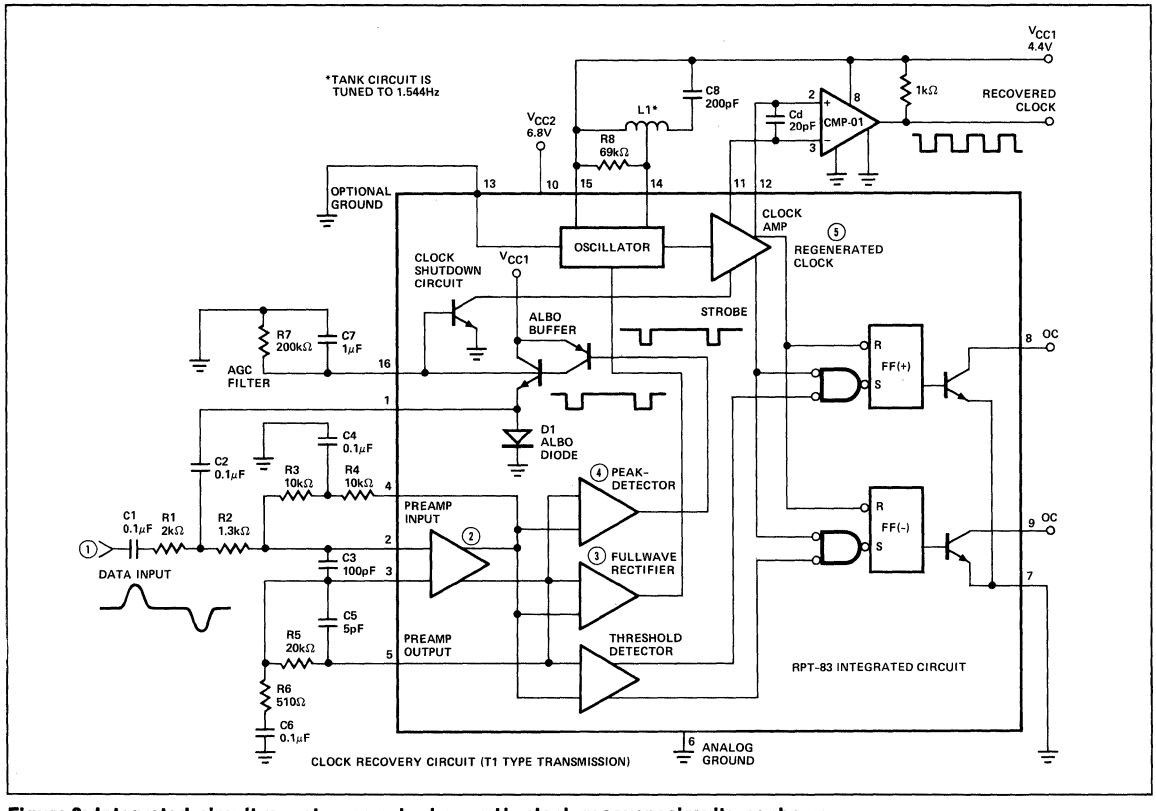


Figure 8: Integrated-circuit repeaters can also be used in clock-recovery circuits, as shown.

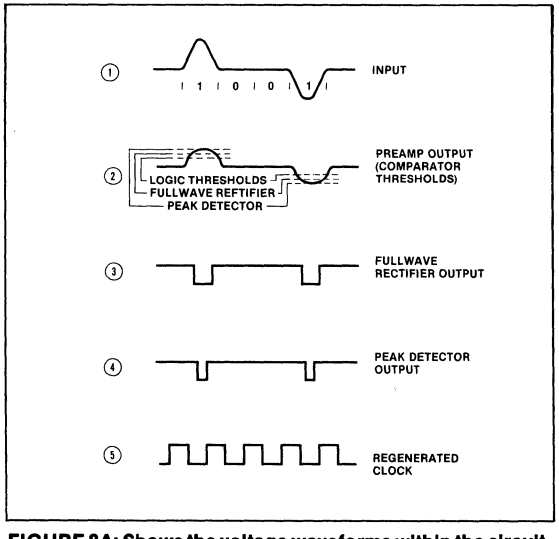


FIGURE 8A: Shows the voltage waveforms within the circuit.

The ALBO filter aids in integrating the pulse output of the detector. As the voltage increases, more current flows through the ALBO diode, and the line build-out is characteristic of longer line lengths.

The power-supply current is available over the signal pair. The simplex power design consists of two zener diodes and a diode float connected to the center taps of the line transformers (Figure 7). The nominal voltage values required are 4.4 and 6.8V.

This design meets the specifications called for in a T1 carrier repeater. The integrated circuit uses less than 13mA total current (both voltage supplies). This means the maximum output current for the total repeater circuit will be under 50mA at worst-case conditions (all ones output signal).

A final application of the integrated circuits is the use of the repeater device in a clock recovery circuit. Data transmission is becoming more important in areas other than long-distance digitized audio. In these instances, the capability of recovering clocking from the data stream can be advantageous. This can mean single-pair connections that can transfer data without additional wiring for timing and clock signals.

Using the RPT-83 in conjunction with a precision comparator, such as the PMI CMP-01, will provide a recovery scheme capable of reproducing a clock waveform from input levels as low as 35mV peak-to-peak. Any system that requires clock retrieval from a data signal and synchronization to that signal can use a circuit similar to this design shown in Figure 8.

The test circuit was operated with an AMI incoming code at frequencies from 64kHz up to 1.544MHz. In the published design, the incoming data waveform is capacitively coupled to an input attenuator using fixed external components and the internal ALBO diode. Since the impedance at pin 1 of the device varies inversely with the amplitude of the input signal, the voltage at the preamplifier input (through resistor R2) will be held to less than 100mV peak-to-peak amplitude. This gives the design an input dynamics range of greater than 45dB while still producing a constant output waveform.

In the circuit shown in Figure 8, tests show none of the external component values to have critical tolerances. The design can be used to recover clocking from an incoming data stream—again a capability that has proven advantageous for designers of data interfaces in many areas other than telecom carrier exchanges.

PMI

AN-50

A VARIABLE-FREQUENCY, CLOCK-RECOVERY CIRCUIT USING THE RPT-82 OR RPT-83

Precision Monolithics Inc.

APPLICATION NOTE 50

This note describes a high-performance clock-recovery circuit, employing an RPT-83 repeater IC and a CMP-01 IC comparator, which helps derive a clock pulse from, and synchronizes it with, an incoming data signal. The circuit accepts a low-level bipolar pulse train (35mV peak-to-peak, minimum) while producing a usable recovered clock signal. Since the circuit also accepts high-level inputs (10V peak-to-peak, minimum), it can attain a 49-dB dynamic range.

The RPT-83 chip is conventionally connected, except that input and output transformers are not required and the (internal) output transistors are left as an open circuit (Figure 1). The recovered clock signal is picked off the RPT-83's clock amplifier (pins 11 and 12) by the CMP-01 comparator.

The comparator's output is basically a square wave at the data rate frequency (which, for this example, is the T1 transmission frequency of 1.544 Mbits/s).

Clock recovery can be best understood by referring to a more detailed diagram of the RPT-83's oscillator section and external tuned circuit (Figure 2). Grounding pin 13 creates a "locked oscillator" operating mode. Floating pin 13 creates a "pulsed tank" operating mode.

In the pulsed-tank mode, the external tuned circuit is stimulated each time the full-wave rectifier demands a current pulse. Between pulses, the tank circuit "rings" at its resonant frequency, damped only by R8 and the on-chip transistor collector resistor R.

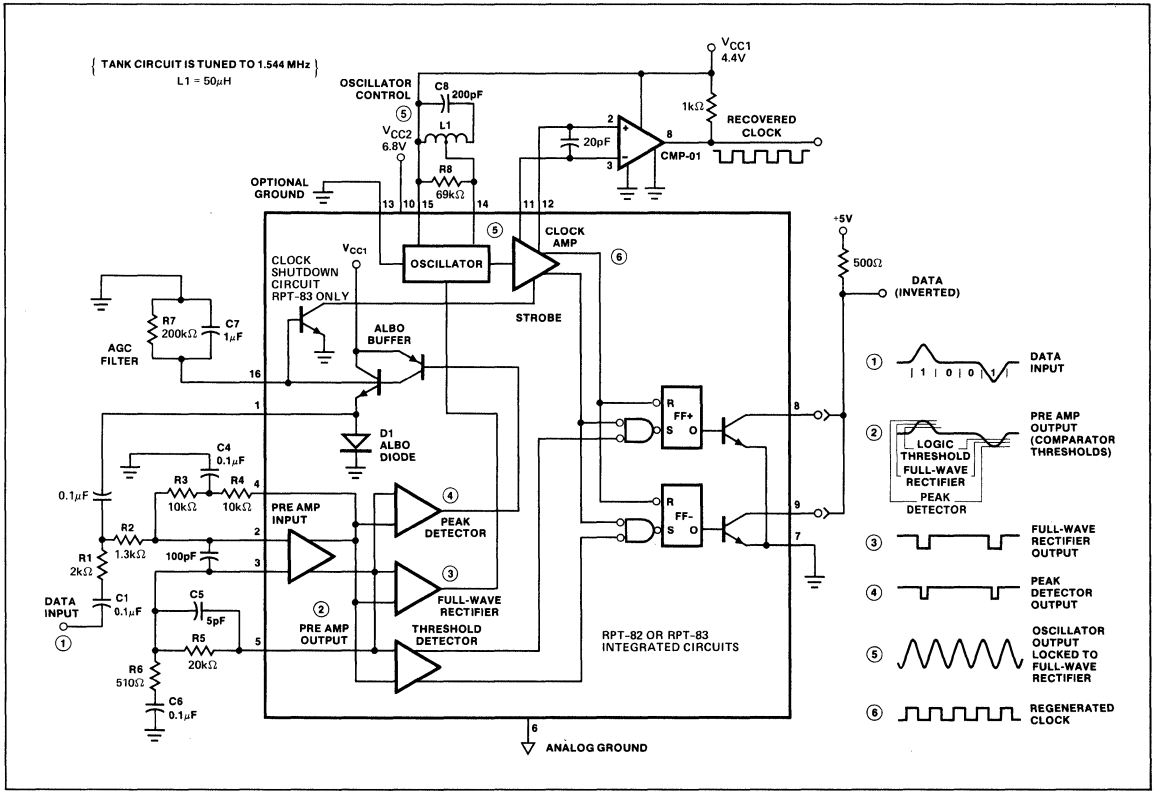


Figure 1: The clock-recovery circuit shown above will accept a 35mV peak-to-peak (minimum) bipolar pulse train and produce recovered clock pulses at the data rate frequency (1.544Mbits/s for this example). Key waveforms, shown in correct timing relationship, illustrate the circuit's operation. Comparator CMP-01 provides amplification and offset for a good TTL interface.

In the locked-oscillator mode, the oscillator runs continuously. It is injection-locked to the full-wave rectifier pulses by the second emitter of on-chip transistor Q. The oscillator circuit drives a buffer emitter follower, which in turn drives a clock amplifier. The clock amplifier has a differential output (pins 11 and 12) and squares the sinusoidal oscillations orginating at pin 14.

Since the clock amplitude at pins 11 and 12 is only 1Vp-p around a common-mode dc level of 4.5V, the CMP-01 comparator provides a good interface to TTL or other logic. A small capacitor, C_4, may be connected across pins 11 and 12 to delay the clock relative to the data.

The circuit shown in Figure 1 does not make use of the data outputs of the repeater IC. However, if a data waveform is required in addition to the clocking pattern, the change in circuit configuration required is minor. By tieing the output leads of the two flip-flops together (pins 8 and 9) and adding a 500ohm pull-up resistor to +5V, an inverted data waveform is made available.

How "pulsed-tank" and "locked-oscillator" modes are selected is shown in Figure 2. Pickoff points for a regenerated clock signal (within the clock amplifier) are also evident in the diagram.

The circuit described in this note was designed and tested only with alternate-mark-inversion (AMI) codes. However, the system should work equally well with any return-to-zero code and would suit any of the many AMI-code variants. It can handle data rates up to 2.0 Mbits/s.

Designs have been tested at frequencies from 64kHz up to 1.544MHz by simply modifying the tank circuit. In all cases, performance met desired expectations.

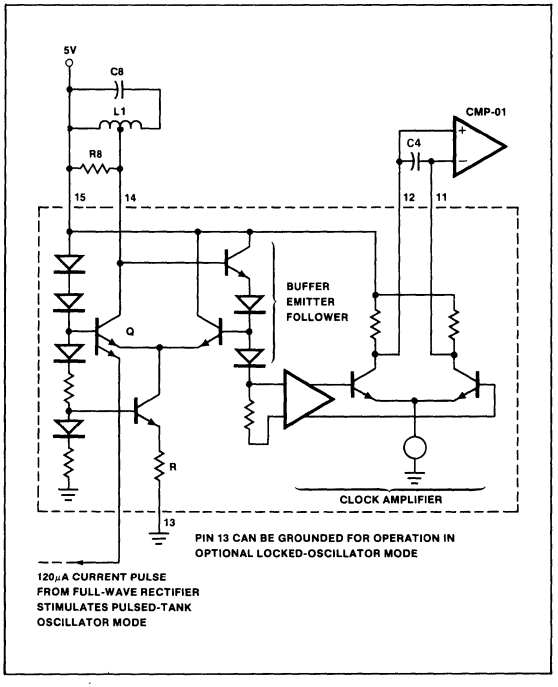


Figure 2: Detailed view of the RPT-83's oscillator and clock amplifier shows how "pulsed-tank" and "locked-oscillator" modes are selected. Pickoff points for a regenerated clock signal (within the clock amplifier) are also evident.

PMI

AN-53

SAMPLE/HOLD CIRCUIT MONITORS TWO INPUT SIGNALS AND TRACKS THE SMALLER OR LARGER SIGNAL

Precision Monolithics Inc.

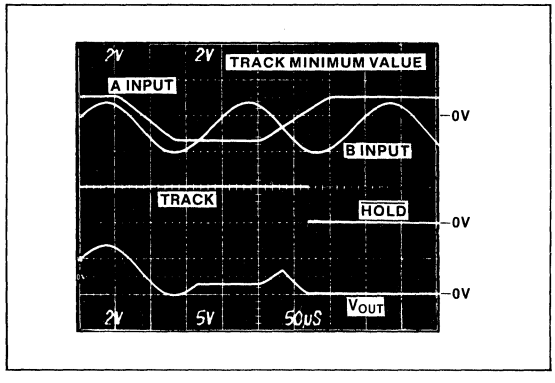
APPLICATION NOTE 53

INTRODUCTION

In control applications involving two sensors it may be necessary to select the smaller or larger of the two sensor signals for control purposes. Possible applications include electronic automobile antiskid control, depth measurement and temperature monitoring. Automatic selection of the signal of interest eliminates the wasteful and expensive hardware and software duplication needed to monitor, digitize and evaluate the two signals.

The circuit described provides a two channel sample-and-hold amplifier that automatically tracks the larger or smaller (user programmed) of two input signals. It is implemented with only one integrated circuit which can replace up to three IC packages that would be necessary (dual switch, comparator, quad op amp) in other implementations. This IC, the GAP-01, contains a comparator and two transconductance input amplifiers (A & B), whose outputs are switched by internal current mode switches into the voltage follower output buffer(C). Two digitally selectable signal paths through the device are possible via the Channel A, Channel B control signals.

Circuit operation is straight forward. In Figure 1, the signal paths through Channel A and Channel B are configured for gains of +1. The comparator monitors the input signals relative magnitudes. With the MIN/MAX control in the "Minimum Track" position (MAXIMUM/$\overline{\text{MINIMUM}}$ = "0"), and the system in "TRACK" (TRACK/$\overline{\text{HOLD}}$ = "1"). The minimum or smaller of the two input signals, A or B, is present at the GAP-01 output (Photograph 1). A "1" comparator output indicates input B is less than input A.



Photograph 1. Minimum Value Track/Hold

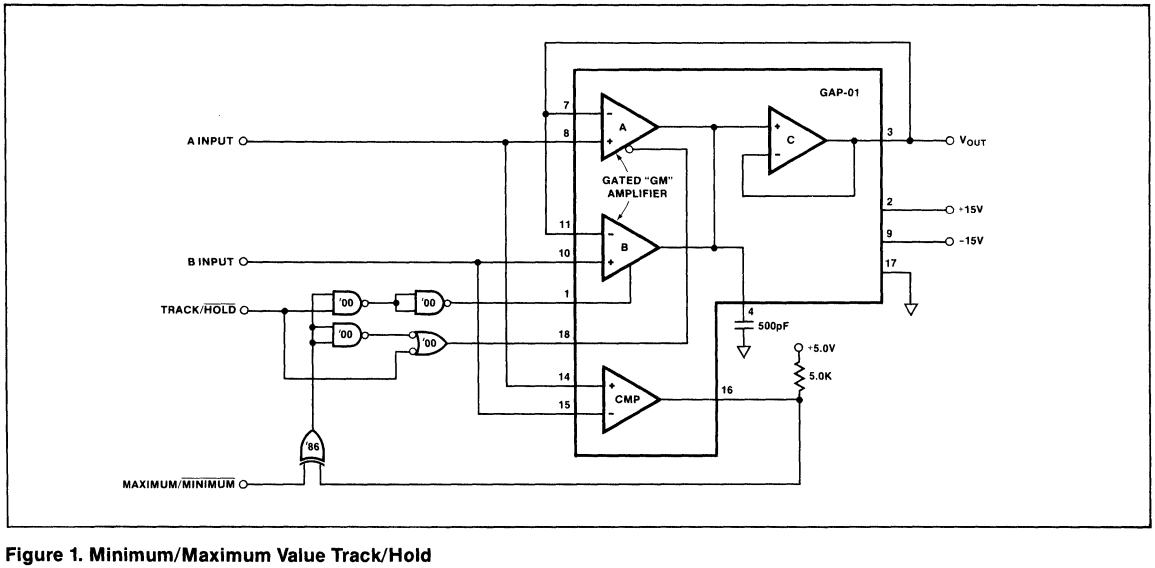
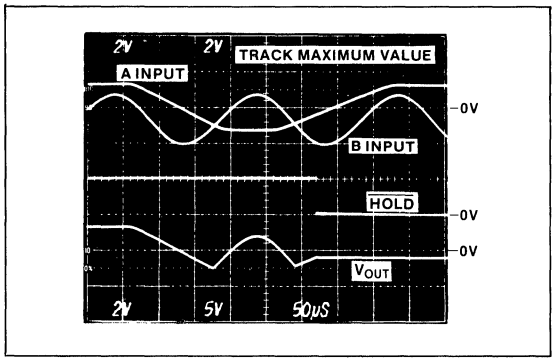


Figure 1. Minimum/Maximum Value Track/Hold

By setting MAXIMUM/$\overline{\text{MINIMUM}}$ to "1" the larger of the two input signals is tracked (Photograph 2). The exclusive "OR" gate simply inverts the comparator output.



Photograph 2. Maximum Value Track/Hold

Gains other than +1 are achievable by changing the GAP-01 feedback ratio as shown in Figure 2.

By setting the TRACK/$\overline{\text{HOLD}}$ control to "0" both the A and B amplifier outputs are disconnected from the output buffer amplifier input, thus putting the system into "hold" and maintaining the last output stored on the external capacitor C_H. This capacitor serves both as a loop compensation and hold, or storage, capacitor (Photographs 1 and 2). Droop rates of 0.2mV/msec are typical.

This powerful minimum/maximum track and hold system is easily constructed from the versatile GAP-01.

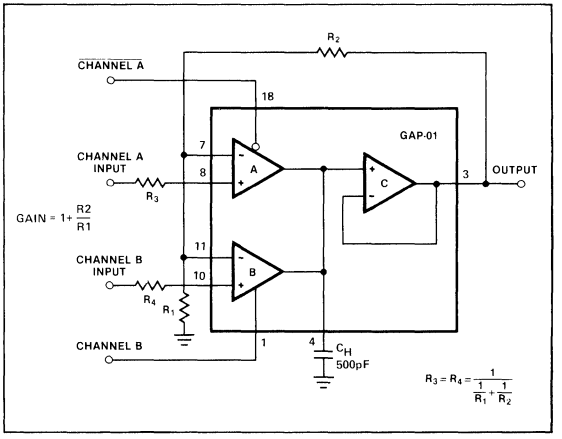


Figure 2. Alternate Gain Configuration

PMI

AN-101

CROSS-PLOT GENERATOR ALLOWS QUICK A/D CONVERTER EVALUATION

Precision Monolithics Inc.

APPLICATION NOTE 101

INTRODUCTION

The testing of analog-to-digital converters (ADCs) can be a difficult and time consuming process. The cross-plot generator described here provides a quick, low-cost way to evaluate ADCs.

ADCs AND THEIR TESTING

Analog-to-digital converters generate a digital code for each discrete value of analog input voltage. The number of codes is a function of resolution. For example, an 8-bit device has 256 codes. The resolution is equal to 1/256 of the full-scale analog voltage. 12-bit converters have 4096 codes and can resolve to 1/4096 of the full-scale voltage. The number of codes can be expressed as 2^n where n = number of bits.

Testing ADCs can be a difficult task. Modern high-resolution devices tax the speed and accuracy of measurement equipment. Linearity tests are highly data-intensive and dynamic measurements require complex and costly test apparatus.

CROSS-PLOT GENERATOR

The cross-plot generator is a simple approach to ADC evaluation. The system uses basic test equipment, simple logic and timing, and is compatible with converters of any resolution.

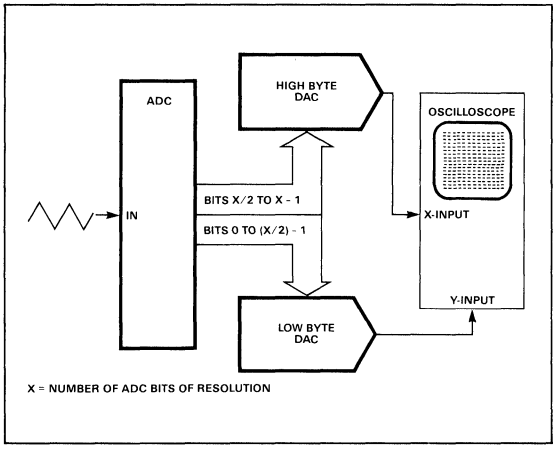
The test circuit (see Figure 1) consists of two D/A converters (DACs) which reconstruct the digitized information and display the data in a dot-matrix format (see Matrix Photos). This format allows the user to view the entire transfer function in real time.

Each dot in the matrix represents one digital code. Missing or narrow codes are identified as missing or dim dots in the displayed matrix.

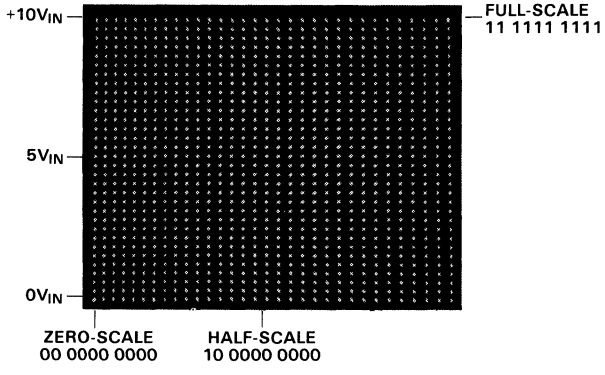
This test method yields four types of data:

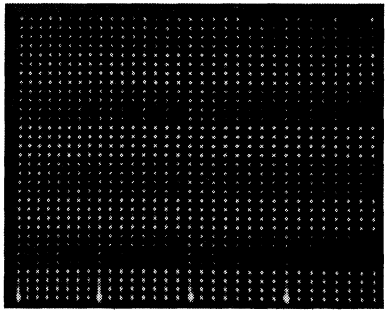
1. Missing code identification
2. Dynamic response (conversion speed)
3. Converter code-width
4. System noise

FIGURE 1: Block Diagram



CROSS-PLOT MATRIX





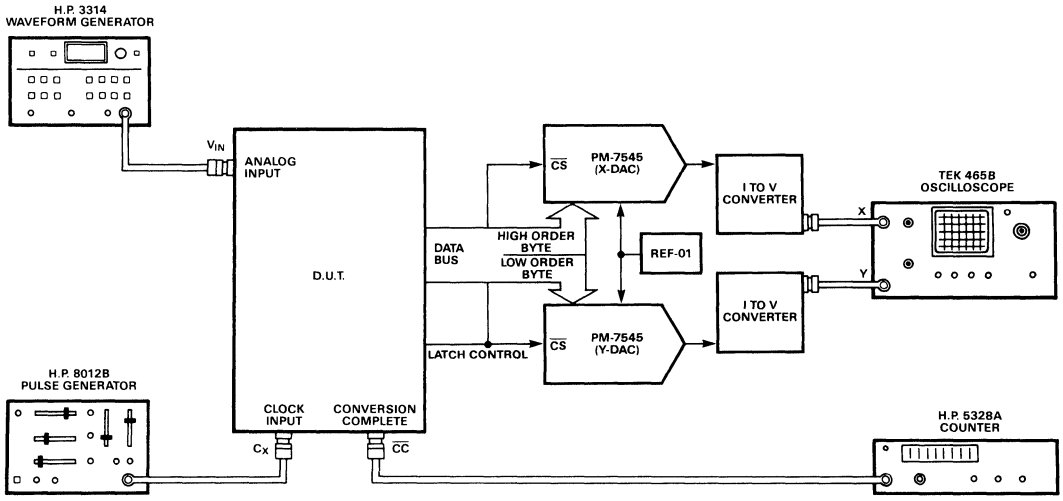
The dot-matrix field for a 10-bit converter is pictured above. The photo illustrates a 32 × 32 dot-matrix or 1024 dots.

The DUT is an ADC-910 operating with a nominal 6μs conversion time. The inputs are a 10Hz, 0 to 10V triangle wave and a 1MHz clock pulse train. These inputs result in approximately three conversions per code.

As illustrated in the photo above, missing and narrow codes are clearly visible as weak or absent dots in the array.

In this case, as conversion speed is increased beyond the ADC's capability, missing codes are observed.

FIGURE 2: Block Diagram



The cross-plot test set-up is shown above. The equipment required is: a waveform generator, pulse generator (used as an external clock), oscilloscope with X-Y function, and a frequency counter or second oscilloscope (to determine clock frequency and conversion time).

The ADC is configured in a free running (continuous conversion) mode. An input triangle wave and clock are applied to the ADC (see Timing Diagram). The ADC executes a conversion and presents the data to the Data Bus. The data is then divided into higher and lower order bytes and latched into the DACs by the latch control line. Following current to voltage conversion, the DAC outputs drive the oscilloscope (higher order driving the X-input, lower order driving the Y-input), creating the dot-matrix field.

MISSING CODES

One form of converter malfunction occurs when some digital codes are absent or missing. Missing codes can cause serious problems in systems level applications. These missing codes can be identified as holes in the dot-matrix field.

DYNAMIC TESTING

Conversion speeds can be measured with the cross-plot generator. A slow triangle wave is applied to the ADC's input. The waveform's voltage is adjusted to sweep from just below zero-scale to just above full-scale. The triangle-wave test frequency should be chosen so that the analog input remains within 1/2 LSB during the converter's conversion time. The conversion clock frequency is then increased until conversion codes (dots in the array) first begin dropping out. A frequency counter is used to determine the clock frequency and conversion time. Alternately, a second oscilloscope may be used, monitoring the ADC's Conversion Complete line, to determine directly the minimum conversion time.

CODE WIDTH

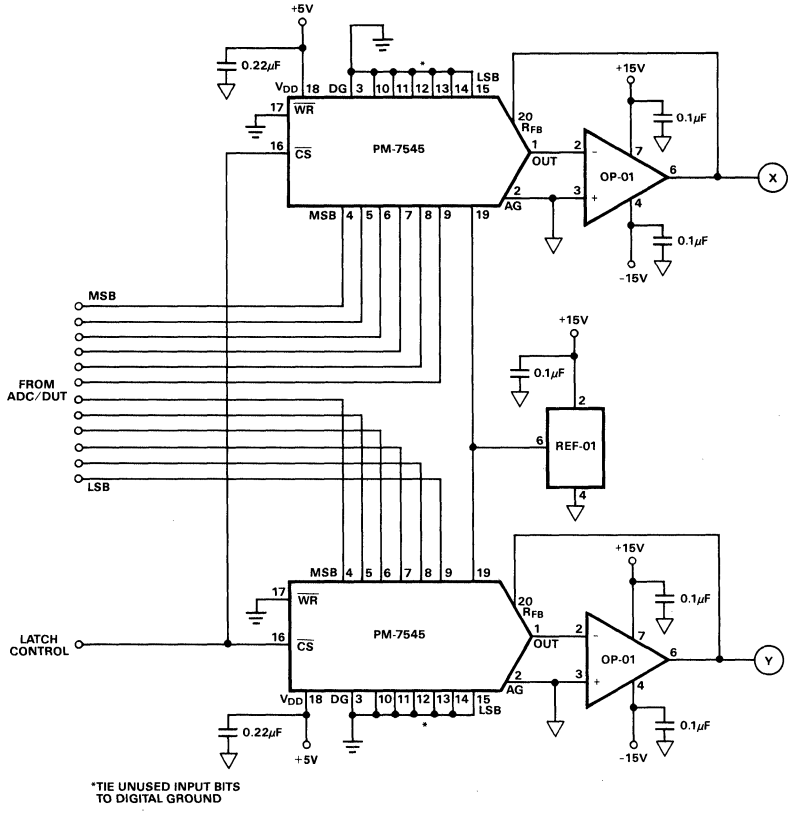
Code-width, or differential nonlinearity, is a measure of the width of the converter's quantizing bands. Each band or code-step has a finite value. As the input voltage is slowly swept, several conversions take place for each code value. Since the number of conversions is dependent upon code-width, shorter codes produce fewer conversions. The intensity of each dot displayed in the matrix is a direct function of the number of conversions and hence the code-width. Dimmer dots, therefore, denote narrower codes and higher differential nonlinearities. Narrow code-widths are depicted in the dot-matrix photograph.

SYSTEM NOISE

The cross-plot generator can be used to determine the repeatability of ADCs. By slowing down the input triangle wave frequency to 0.1Hz, the oscilloscope should ideally display one dot at a time when the input voltage is between code transitions. As the input voltage approaches a code transition, two dots will appear on the oscilloscope screen. Once the input voltage moves to the next code, a single dot will again appear on the oscilloscope screen. If the ADC system has noise problems, either due to layout or the ADC itself, the oscilloscope display will show two, three, or more dots simultaneously. This is an indication of undesirable noise in the system causing multiple output codes for a single analog input voltage.

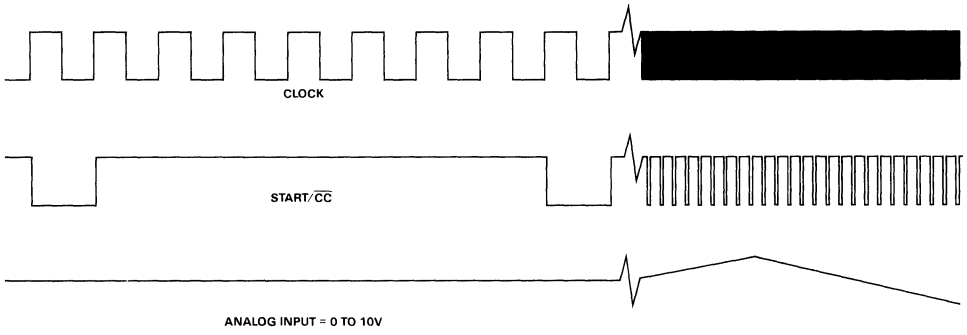
Checking prototype circuits with this test can help quickly identify the noise level and source. Proper location of bypass capacitors, central analog ground, and digital signal lines can be easily determined, speeding the system debugging process.

FIGURE 3: Schematic



The cross-plot schematic is shown above. A pair of PM-7545s are driven directly by the ADC's outputs. The DACs drive the X-Y inputs of the oscilloscope after current-to-voltage conversion by the OP-01s. Reference voltage for the converters is provided by a REF-01.

FIGURE 4: Timing Diagram



A typical timing diagram for a 10-bit successive approximation conversion system (ADC-910) is shown above. The analog input is a slow triangle wave sweeping the full input range of the converter (shown here as a unipolar 10V range).

The clock provides a time base for the converter and is several orders of magnitude faster than the input frequency. This high clock frequency, relative to the analog input, insures that the analog voltage changes less than 1/2 LSB during the conversion time.

The START/$\overline{CC}$ signal (sometimes termed $\overline{BUSY}$) is generated by the ADC and can function as a data-load pulse for the DACs.

PMI

AN-102
VERY LOW NOISE OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

APPLICATION NOTE 102

APPLICATIONS

- **High Precision Instrumentation**
- **Microphone Preamplifier**
- **Tape-Head Preamplifier**
- **Strain-Gage Amplifier**

FEATURES

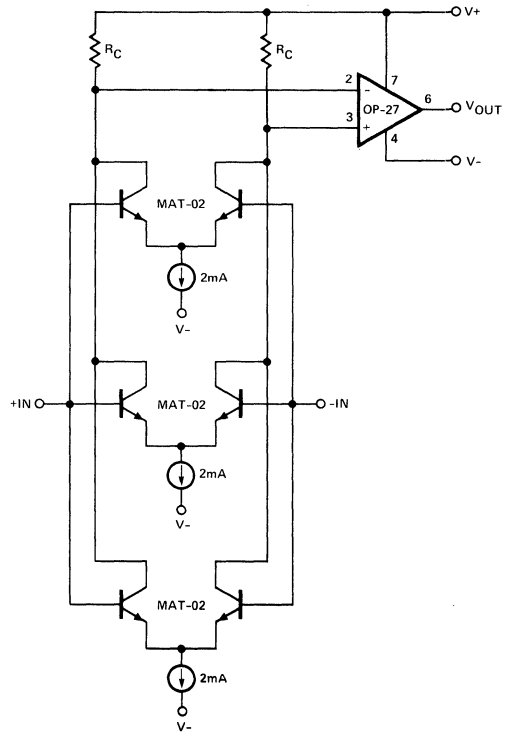
- **Very Low Voltage Noise** ..... **500pV/$\sqrt{Hz}$**
- **High Gain-Bandwidth Product** **150MHz**
- **High Open-Loop Gain** ..... **3×10^7**
- **High CMRR** **130dB**
- **Very Low Offset Voltage Drift** ..... **<0.1μV/°C**

GENERAL DESCRIPTION

In situations where low output, low-impedance transducers are used, amplifiers must have very low voltage noise to maintain a good signal-to-noise ratio. The design presented in this application note is an operational amplifier with only 500pV/$\sqrt{Hz}$ of broadband noise. The front end uses MAT-02 low-noise dual transistors to achieve this exceptional performance. The op amp has superb DC specifications compatible with high-precision transducer requirements, and AC specifications suitable for professional audio work.

PRINCIPLE OF OPERATION

The design configuration in Figure 1 uses an OP-27 op amp (already a low-noise design) preceded by an amplifier consisting of three parallel-connected MAT-02 dual transistors. Base spreading resistance (R_{bb}) generates thermal noise which is reduced by a factor of $\sqrt{3}$ when the input transistors are parallel connected. Schottky noise, the other major noise-generating mechanism, is minimized by using a relatively high collector current (1mA per device). High current ensures a low dynamic emitter resistance, but does increase the base current and its associated current noise. Higher current noise is relatively unimportant when low-impedance transducers are used.



Simplified Schematic for Very-Low-Noise Operational Amplifier

Figure 1: Simplified Schematic

CIRCUIT DESCRIPTION

The detailed circuit is shown in Figure 2. A total input-stage emitter current of 6mA is provided by Q4. The transistor acts as a true current source to provide the highest possible common-mode rejection. R_1, R_2, and R_3 ensure that this current splits equally among the three input pairs. The constant current in Q4 is set by using the forward voltage of a GaAsP light-emitting diode as a reference. The difference between this voltage and the base-emitter voltage of a silicon transistor is predictable and constant (to within a few percent) over the military temperature range. The voltage difference, approximately 1V, is impressed across the emitter resistor R_{12} which produces a temperature-stable emitter current.

R_6 and C_1 provide phase compensation for the amplifier and are sufficient to ensure stability at gains of ten and above.

R_7 is an input offset trim that provides approximately $\pm 300\mu V$ trim range. The very low drift characteristics of the MAT-02 make it possible to obtain drifts of less than $0.1\mu V/°C$ when the offset is nulled close to zero. If this trim is not required, the R_4, R_7, and R_8 network should be omitted and R_5/R_9 connected directly to V+.

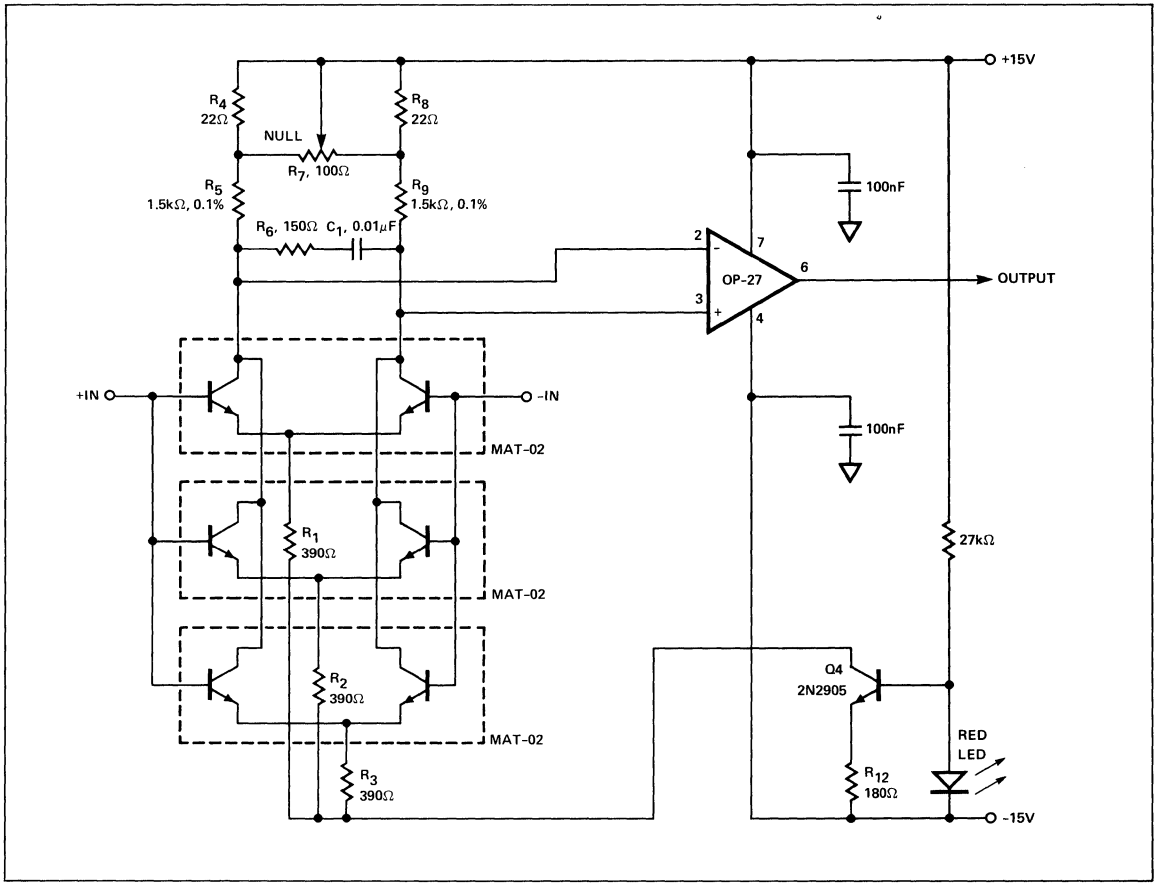


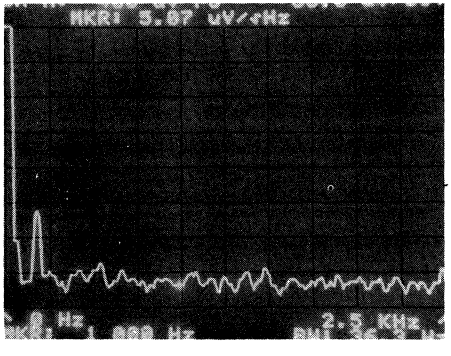
Figure 2: Complete Amplifier Schematic

AMPLIFIER PERFORMANCE

The measured performance of the op amp is summarized in Table 1. Figure 3 shows the broadband noise spectrum which is flat at about 500pV/$\sqrt{Hz}$. Figure 4 shows the low-frequency spectrum which illustrates the low 1/f noise corner at 1.5Hz. The low-frequency characteristic in the time domain from 0.1Hz to 10 Hz is shown in Figure 5; peak-to-peak amplitude is less than 40nV.

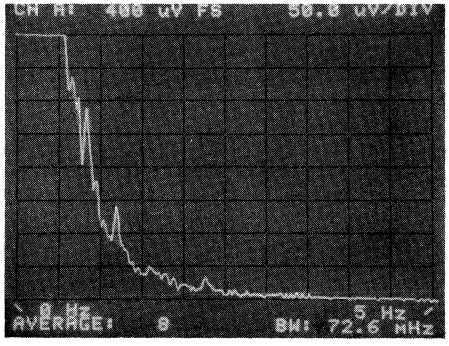
Table 1: Measured Performance of the Op Amp

Input Noise Voltage Density at 1kHz		500pV/$\sqrt{Hz}$
Input Noise Voltage from 0.1Hz to 10Hz		40nV$_{p-p}$
Input Noise Current at 1kHz		1.5pA/$\sqrt{Hz}$
Gain-Bandwidth	G = 10	3MHz
	G = 100	600kHz
	G = 1000	150kHz
Slew Rate		2V/μs
Open-Loop Gain		3×10^7
Common-Mode Rejection		130dB
Input Bias Current		3μA
Supply Current		10mA
Nulled TCV$_{OS}$		0.1μV/°C Max
T.H.D. at 1kHz	G = 1000	0.002%



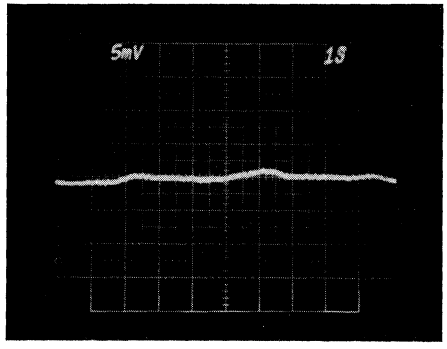
Spectrum analyzer display of broadband noise with a gain of 10,000.
Horizontal axis = 0 to 2.5kHz.
Normalized vertical axis = 830pV/$\sqrt{Hz}$ R.T.I.
e_n = 507pV/$\sqrt{Hz}$ at 1kHz.

Figure 3: Spectrum Analyzer Display — Broadband



Low frequency noise spectrum at a gain of 10,000 showing a low 1.5Hz noise corner.

Figure 4: Spectrum Analyzer Display — Low Frequency



Peak-to-peak noise from 0.1 to 10Hz.
Overall gain is 100,000.

Figure 5: Oscilloscope Display

CONCLUSION

Using MAT-02 matched transistor pairs operating at a high current level, it is possible to construct a high-performance, low-noise operational amplifier. The circuit uses a minimum of components and achieves performance levels impractical with monolithic amplifiers.

Take the guesswork out of settling-time measurements

By building an oscilloscope input amplifier and a step generator, you can use off-the-shelf laboratory oscilloscopes to make precise measurements of the settling times of fast linear circuits.

Because linear circuits are getting faster and faster, it's becoming increasingly difficult to accurately measure such circuits' dynamic performance. Available test equipment is inadequate to measure the dynamic performance of these circuits, which have settling times as fast as 100 nsec. Such equipment either lacks the requisite sensitivity or has poor overload characteristics, which mask the effects you're trying to observe (see **box**, "Sources of error in fast-linear-IC measurement").

To test a device accurately, you must use test equipment that has much better resolution than the device under test will ever require. To test fast linear circuits, you have to observe small effects superimposed on a very large signal change. But if you increase oscilloscope sensitivity enough so you can see these small effects, you will almost certainly produce overload conditions in the oscilloscope. Off-the-shelf oscilloscopes do not provide the resolution you need at the extreme ends of a large step signal, and they won't be able to handle the overload conditions.

To make an accurate determination of settling time—especially for op amps and fast D/A converters—you need to build two items of special test equipment: a step-function generator (**Fig 1**) and an oscilloscope input amplifier (**Fig 2**).

Fig 1's step-function generator lets you evaluate the recovery characteristics of the available oscilloscopes. Further, by providing a reference signal that has precisely known characteristics, the generator will eliminate guesswork in settling-time measurement.

The oscilloscope input amplifier in **Fig 2** provides a resolution to 200 μV/div on a voltage-input range of ±10V, or 200 nA/div on a current-input range of ±10 mA. This input amplifier will allow you to make 0.01% settling determinations without having to estimate the magnitude of small and questionable oscilloscope images. This test system provides settling-time measurements to 50 nsec for 8-bit measurements and will allow you to perform dynamic tests on 12-bit devices at full operating speeds.

Test fixture removes sources of error

Fig 2 shows the complete test fixture. This test fixture, which will eliminate most sources of error, consists for the most part of discrete components and CA3127 transistor arrays. The main amplifier chain consists of cascaded differential amplifiers IC_1 through IC_4, with emitter followers between each stage to

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Off-the-shelf scopes don't provide the resolution you need at the ends of a large step signal.

perform buffering and level shifting. Although these amplifiers overload in the presence of large inputs, they do not saturate, and they recover from overload within approximately 15 nsec.

It's essential that you place each amplifier section in a separate, well-shielded compartment. If the shielding is not adequate, the entire amplifier chain may oscillate at several hundred megahertz.

The V_{IN} path has a gain of 0.5 between the input terminal and the summing junction. IC_1 and IC_2 provide most of the system gain; you set the product of their gains to a value between 4 and 100 by varying the bias currents fed into the differential amplifiers. IC_3 and IC_4 together form a linear output driver with a gain of 2 and a differential output swing of no more than ±160 mV; thus, an oscilloscope set for an A+B display of vertical inputs with B inverted and a sensitivity of 20 mV/div needs to handle only two screens' worth of signal; this small input range does not overload the oscilloscope input circuitry. All signals are measured relative to ground, not to some bias point.

The offset voltage is provided by transistors Q_1 through Q_7 and their related components. Transistor Q_2, the offset voltage source, operates at a bias of 25 mA to reduce its output impedance, and it has a feedback loop to reduce the output impedance still further at high frequencies. Transistor Q_8 acts as a buffer between Q_2 and amplifier IC_9, which, with three analog switches of IC_7, constitutes an S/H amplifier that stores the offset level.

The test fixture has an autozero feature, which offsets the final output value of the device under test so that it falls on the oscilloscope baseline. The test fixture cycles continuously through the four time states shown

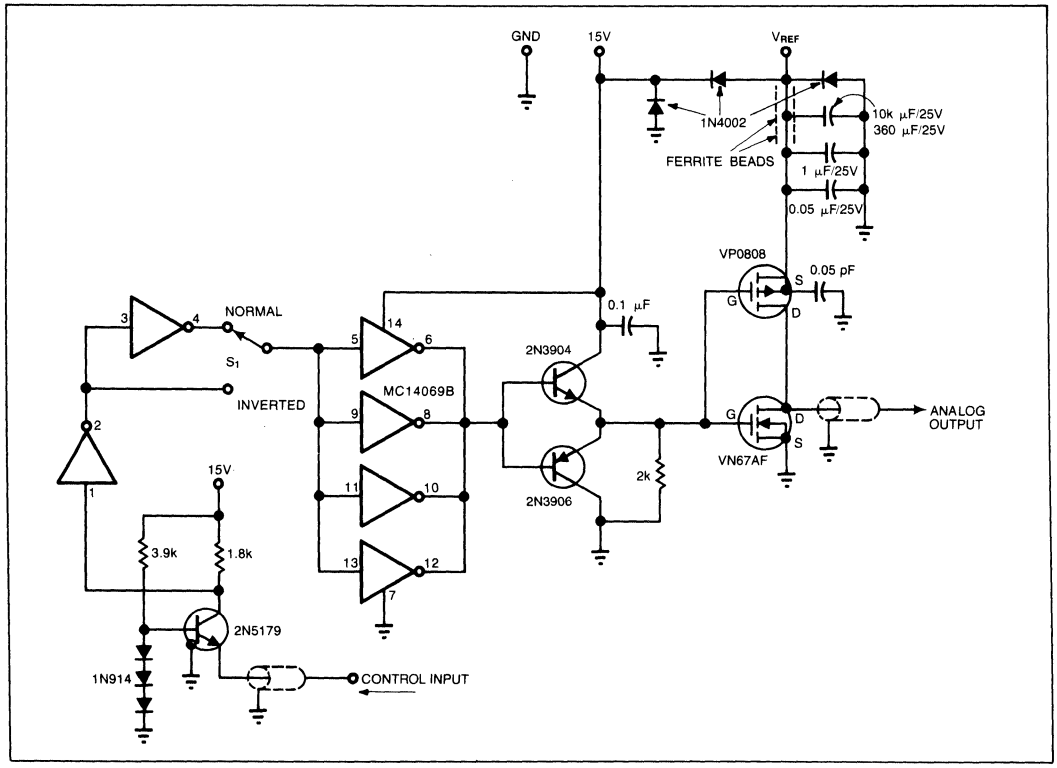


Fig 1—Use this perfect-step generator *for checking your oscilloscope. Output power VMOS transistors Q_4 and Q_5 exhibit no saturation effects and switch the analog output cleanly to ground or to V_{REF} (nominally 10V). The step rate is greater than 1500 V/µsec.*

Sources of error in fast-linear-IC measurement

It's often difficult to measure the performance of fast linear ICs, mainly because off-the-shelf laboratory oscilloscopes either can't handle the sensitivity you require or mask the effects you're trying to observe.

When you use off-the-shelf equipment to measure the performance of a fast linear circuit, your measurements may be inaccurate because such equipment doesn't allow you to see the actual shape of a waveform. And you can't accurately estimate the actual shape of a waveform by assuming that it follows an exponential curve; if you do so, your estimation may be wildly inaccurate.

Although many components of analog waveforms are exponential—overshoot, ringing, and the response produced by feed-forward compensation fall into this category—waveshapes are often composed of components that are not exponential, although they may seem to be. Overload recovery, for example, is almost never exponential, and thermal tails can have almost any shape.

Fig A shows the difference between an actual waveform and an expected exponential curve. The lower diagram in **Fig A** shows an analog signal moving from some initial value to a higher level and then settling toward a final value. The area within the dashed lines is expanded by a factor of 2000 in the upper diagram. You'll see that overshoot and recovery components cause the waveform to have a tail that crosses the lines representing the ±1-mV acceptable settling window more than once.

The time that elapses between the start of the rising edge and the last entry into the settling window is called T_{SETTLE}. The dashed curve in **Fig A** approximates the sum of all exponential components of the waveform; if the real waveform followed this exponential curve, you could easily determine settling time.

However, most electronic circuits exhibit, after slewing, a slow-settling component that's not exponential. One of the most troublesome components of this kind is the tail generated by a device input stage that's driven into overload by a step function. It's hard to determine the difference the tail makes, because a wide range of overloads will produce the same recovery characteristics—for example, a 10V step and a 20V step might both produce an identical 1-mV settling component, which would appear as a 0.01% tail on the 10V step, but a 0.005% tail on the 20V step.

Although a 0.005% tail on the 20V step appears to indicate better system performance, the performance is actually unchanged. Other causes of tails are thermal changes, the destabilization of a power supply or of bias, and the characteristics of a device that's recovering from saturation; tails due to these causes are not symmetrical for input steps of opposite slope.

The pole/zero pairs in op amps that use feed-forward compensation are particularly troublesome. Many such amplifiers have settling times of 1 μsec or less for settling accuracies of 1 or 0.1%. However, when these amplifiers must settle to an accuracy of 0.01%, the settling time increases to 3 μsec or more.

This phenomenon is significant in oscilloscope probes that attenuate, because such probes often use pole/zero pairs to smooth out response aberrations over a wide frequency range, but in the process they produce linear tails of 1% or more.

Noise, too, can be a source of confusion. Noise peaks that constantly cross the settling window may make you think the device under test hasn't settled, even when the device's contribution to the waveform is constant. Actually, 16-bit D/A converters never really do settle; to estimate their performance, you just have to smooth the output wave and ignore the noise.

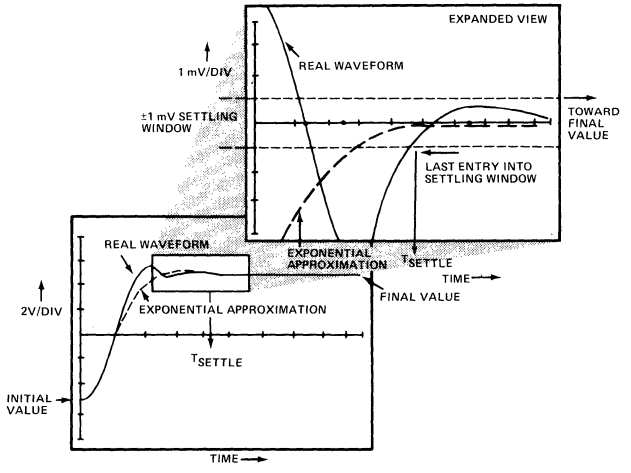


Fig A—This typical settling waveform *shows what you can expect to see on a low-sensitivity oscilloscope (bottom) and an expanded view (top) of the details that are difficult to measure.*

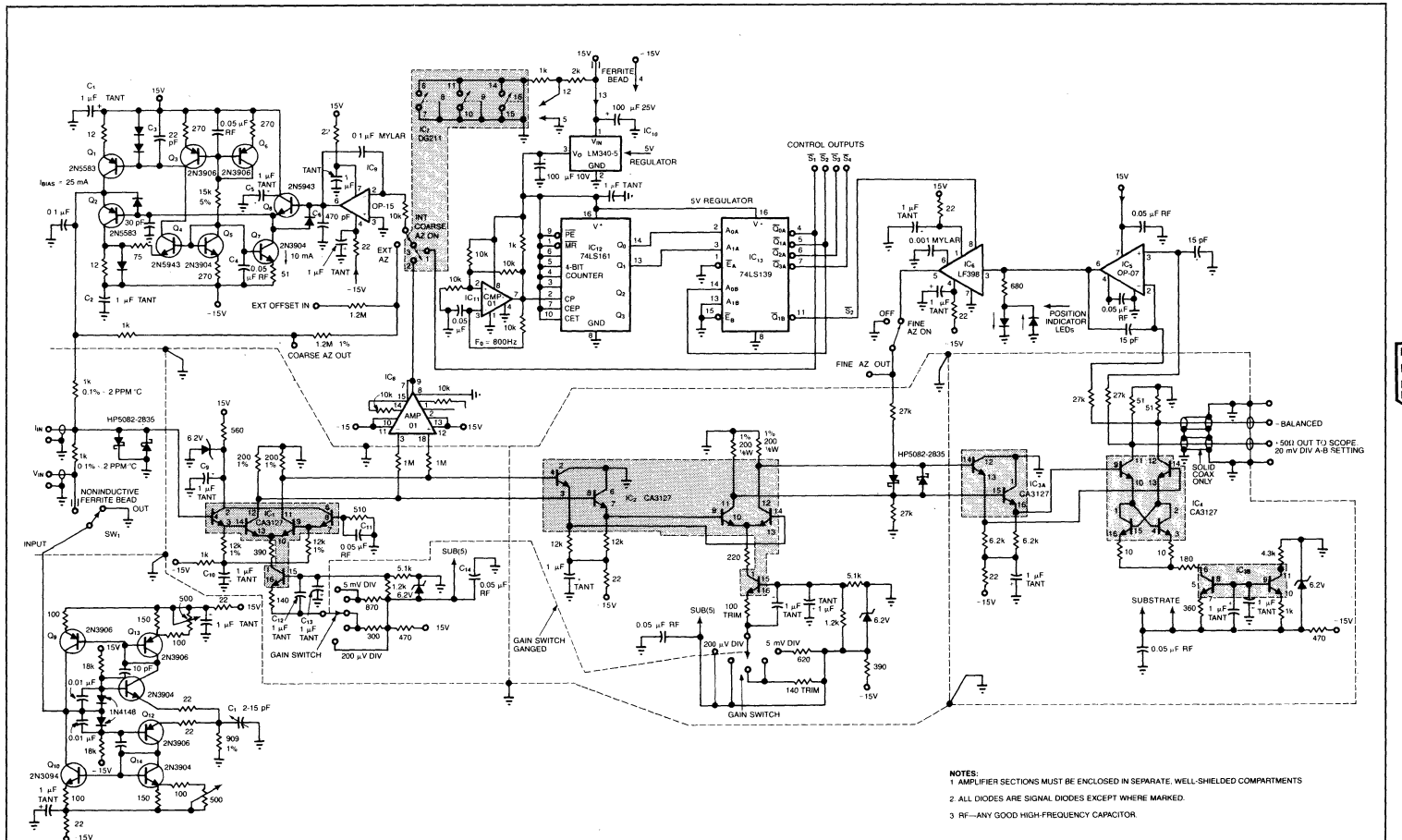


Fig 2—This settling-time test fixture *has an autozero feature, which ensures that the final output of the device under test will fall on the oscilloscope baseline. The fixture has special protection against overloading of the oscilloscope input circuits.*

If you assume that settling tails too small to see clearly are exponential, your estimate may be wildly inaccurate.

in **Table 1.** Comparator IC_{11} acts as an 800-Hz clock oscillator that generates the time states with the aid of IC_{12}, a 4-bit counter, and IC_{13}, a decoder. IC_{12} divides and squares the clock signal; IC_{13} provides four nonoverlapping but closely synchronized state signals.

The repetition rate of the complete cycle (S_1 through S_4) is set at approximately 200 Hz to allow the oscilloscope to develop sufficient brightness. During the first state (S_1), when the device under test is at its final value, IC_8 measures the unbalance of amplifier IC_1.

The output of IC_8 drives IC_9 (an S/H amplifier) to change the offset voltage in the direction that tends to rebalance IC_1. This coarse autozero voltage settles toward the end of time state S_1. Exactly at the end of S_1, IC_9 (in conjunction with IC_7) samples and holds the voltage on capacitor C_7 (C_7 is in IC_9's feedback loop). This voltage acts as a reference voltage for the succeeding time states.

TABLE 1—TIME STATES AND ACTIONS FOR AUTOZERO FUNCTION

TIME →

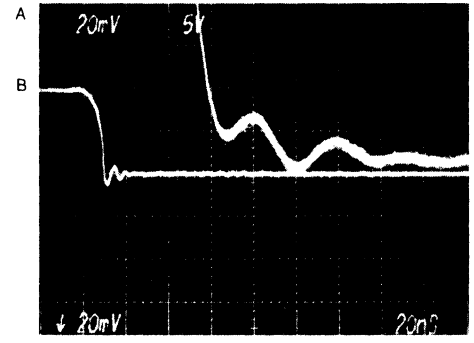
STATE	S_1	S_2	S_3	S_4
VALUE FOR DEVICE UNDER TEST	FINAL	FINAL	INITIAL	FINAL
SYSTEM FUNCTION	COARSE AUTOZERO	FINE AUTOZERO	STARTING MARK (TEST FIXTURE IS OVERLOADED)	DISPLAY SETTLING CHARACTERISTIC

↑ SCOPE TRIGGER

Although it's stable to several tens of microvolts, the coarse autozero voltage is not accurate enough to ensure that the final output value of the device under test will be offset onto the oscilloscope baseline. The largest error occurs when the fourth analog switch of IC_7 disconnects IC_8 from IC_9, delivering a charge from the switch to the integrator input and causing a step of approximately 1 mV. To correct for the effects of this step, IC_5 and IC_6 force IC_3 and IC_4 to come to balance during state S_2 by injecting feedback. At the end of state S_2, IC_6 samples and holds the voltage that brought the fixture output to balance; input baseline variations of ±10V cause less than 20 μV of output baseline shift.

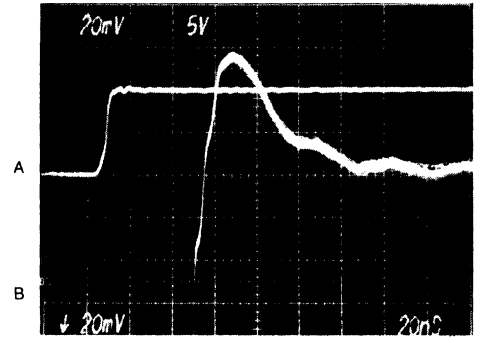
In state S_3, the fixture sends the device under test to its initial value; at this time, the amplifiers of the fixture will probably be overloaded, but will recover rapidly. In state S_4, the device under test settles back toward its final value and the oscilloscope is triggered so that you can observe the settling event through the fixture.

The test fixture accepts either a current input (connected directly to the summing junction) or a voltage input (connected via a 1000Ω resistor). The effective



(a)

TRACE	VERTICAL	HORIZONTAL
A	1 mV/DIV	20 nSEC/DIV
B	5V/DIV	20 nSEC/DIV



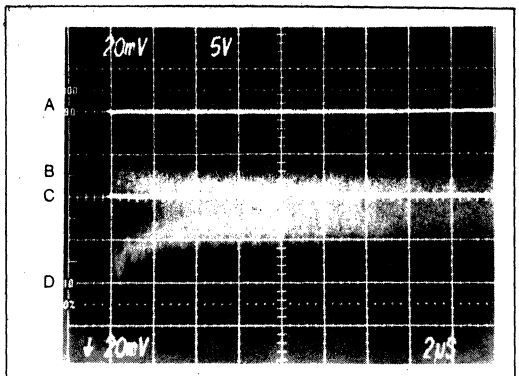
(b)

TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	20 nSEC/DIV
B	1 mV/DIV	20 nSEC/DIV

***Fig 3—The step-function generator settles to 0.01%** within 70 nsec toward ground **(a)** and toward 10 V **(b)**. These scope photos show settling times of the step generator and the test fixture alone.*

impedance of R_{IN} and R_{OFF} in parallel is 500Ω, and the time constant is approximately 7 nsec. (A lower impedance would improve settling speed, but some sources, which have difficulty in driving even the 1000Ω input impedance at the voltage input, would not tolerate any decrease.)

Transistors Q_9 through Q_{14} alleviate this difficulty by simulating a negative resistance of −1000Ω, which can be switched in parallel with the 1000Ω voltage-input resistor. When actuated, the negative-resistance simulator raises the impedance at the voltage input to approximately 30,000Ω and provides whatever current is needed to assist the device under test in placing its normal output current through the input resistor.



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	2 μSEC/DIV
B	200 μV/DIV	2 μSEC/DIV
C	5V/DIV	2 μSEC/DIV
D	200 μV/DIV	2 μSEC/DIV

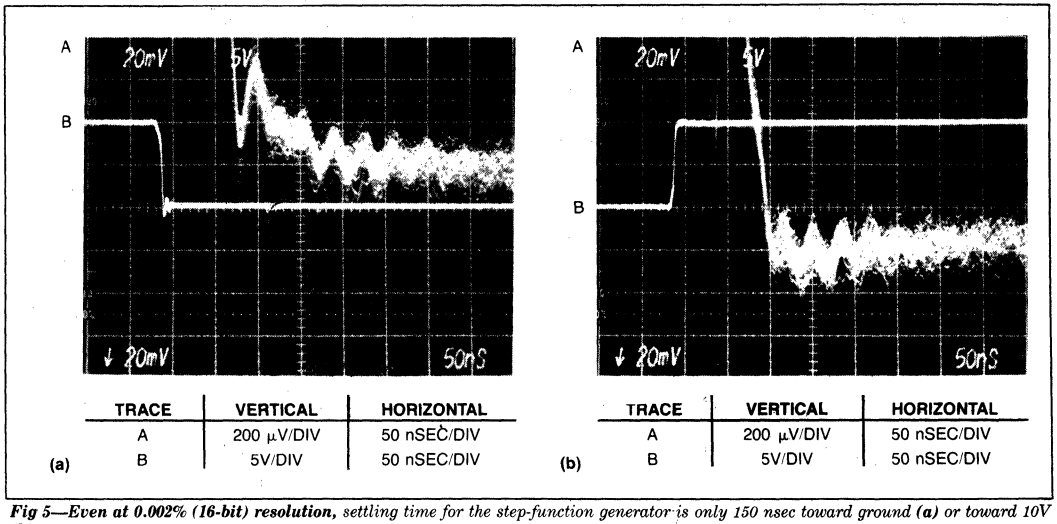
Fig 4—The long-term step-generator tail is approximately 80 μV when settling to ground and approximately 300 μV when settling to 10V.

Determine settling times accurately

Fig 3 shows the settling times—both toward 10V and toward ground—that you obtain when the edge generator is driving the test fixture. The combined settling time of both units to within 0.01% of 10V is 70 nsec or less, measured from the point where ringing is no longer visible after slewing (at the second major division on curve A) to the last crossing of the 1-mV division (curve B). It's difficult to know what each unit actually contributes to the combined settling time; however, it seems probable that the fixture settles within 50 nsec, and that, beyond the 40-nsec mark, the display shows the real settling tail of the edge generator plus a small, slow, thermal response from the fixture.

The size of the tail, as you can see from **Fig 4,** is approximately 80 μV when the signal is settling to ground and 300 μV when it's settling to 10V. A supply-voltage glitch occurs on each transition of the output, so the edge generator probably creates some of the tail.

When you're applying a large signal to the input of the test fixture, you may find that the signal source develops a long settling tail in driving the 1-kΩ resistors. In that case, switch in the negative-resistance simulator.



	TRACE	VERTICAL	HORIZONTAL
(a)	A	200 μV/DIV	50 nSEC/DIV
	B	5V/DIV	50 nSEC/DIV

	TRACE	VERTICAL	HORIZONTAL
(b)	A	200 μV/DIV	50 nSEC/DIV
	B	5V/DIV	50 nSEC/DIV

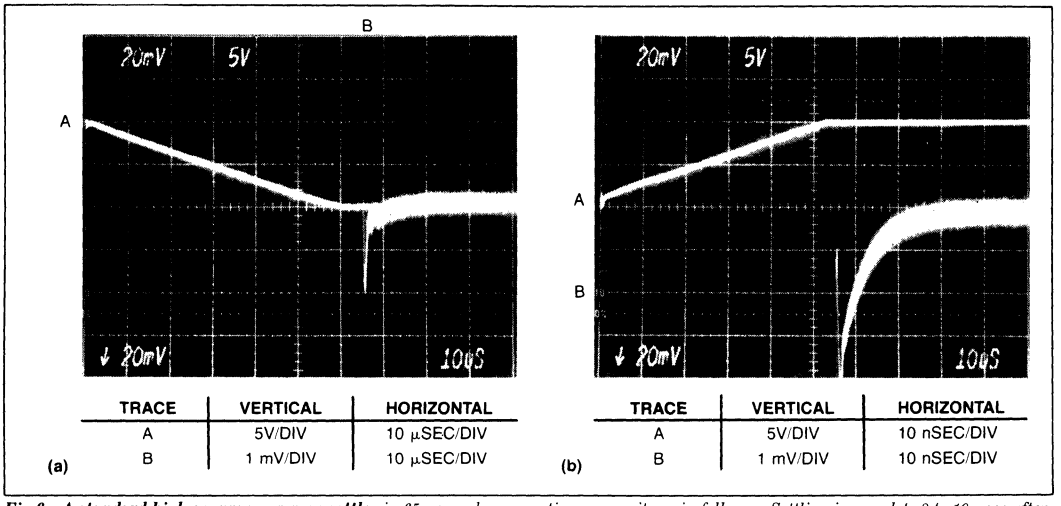
Fig 5—Even at 0.002% (16-bit) resolution, *settling time for the step-function generator is only 150 nsec toward ground* ***(a)*** *or toward 10V* ***(b).***

Overload recovery is almost never exponential.

When it's driven by a fast signal source, the negative-resistance-simulator circuit can cause short-term ringing. Thus, when you're testing very fast devices, you may have to use the normal 1000Ω input for the short-term measurements and then switch in the impedance buffer for an accurate display of the long-term effects. **Fig 5**'s photos, which were taken with the negative-resistance simulator inactive, show that even with 16-bit resolution, the test system's settling time is less than 150 nsec.

You can use **Fig 2**'s test fixture to test op amps as well as D/A converters. The scope photos in **Figs 6** and **7** show the settling times of a standard, high-accuracy op amp (OP-07) and a fast FET op amp (OP-16). **Fig 8** shows the settling times of two 565A 12-bit D/A converter devices from different manufacturers.

The 565A devices require a special test setup, because their full-scale output is only −2 mA, in contrast with the fixture's ±10-mA input range. This sensitivity penalty degrades the signal-to-noise ratio. You should ground the feedback and offset resistor of the 565A devices to prevent their capacitance from slowing the



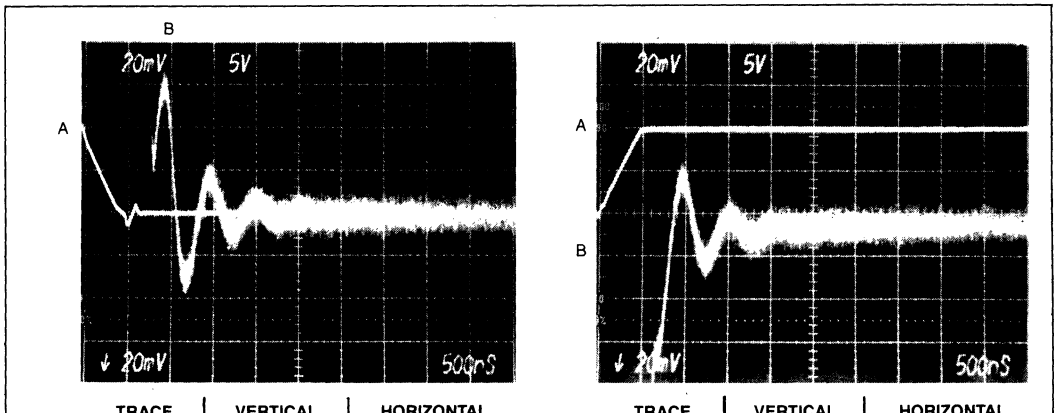
(a)

TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	10 μSEC/DIV
B	1 mV/DIV	10 μSEC/DIV

(b)

TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	10 nSEC/DIV
B	1 mV/DIV	10 nSEC/DIV

***Fig 6—A standard high-accuracy op amp settles** in 65 μsec when operating as a unity-gain follower. Settling is complete 8 to 10 μsec after slewing is finished.*



(a)

TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	500 nSEC/DIV
B	1 mV/DIV	500 nSEC/DIV

(b)

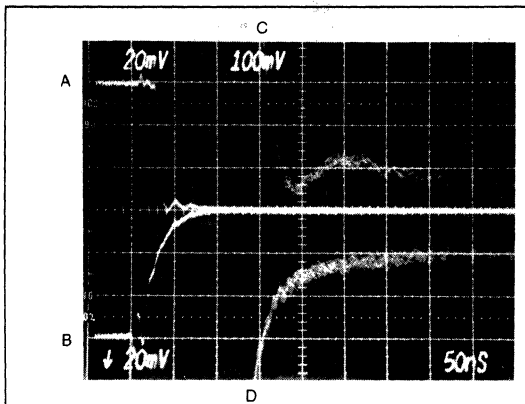
TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	500 nSEC/DIV
B	20 mV/DIV	500 nSEC/DIV

***Fig 7—A fast FET op amp settles to 0.01%** within 1.5 μsec toward ground **(a)** and toward 10V **(b)**. The last ringing peak that grazes the ±1 major vertical division is taken as the 0.01% settling point.*

It's essential that you place each amplifier section in a separate, well-shielded compartment.

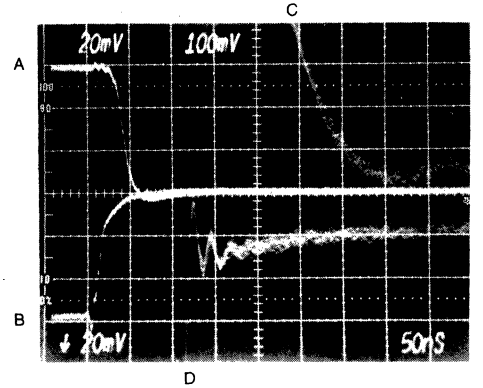
settling. You should also bypass the reference output with a 1-μF tantalum capacitor to prevent the reference from destabilizing.

To measure current, ground the voltage input terminal of the fixture, or terminate it with a 50Ω resistor, and connect the converter output to the current-input terminal of the fixture. The input impedance is now 500Ω, but by reckoning it as 1000Ω, you can maintain the calibration of the gain switch. Thus, 1 mV/div on the gain switch equals 1 μA/div of input, or approximately 2 LSB of the converter output. The first device seems to settle within its 250-nsec specification, even though it has a slow tail (approximately ±1 LSB) (**Fig 8a**). This tail is probably real, but you should, of course, always be suspicious of any measurements at these speeds and sensitivities. The second device exhibits a large glitch on the off-to-on transition (**Fig 8b**); this glitch is probably caused by destabilization of the device's reference input amplifier. **Fig 8c** shows a compression of **Fig 8b**'s glitch so that the whole glitch is visible. **EDN**



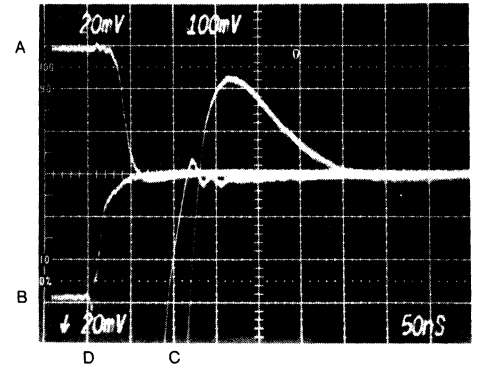
TRACE	VERTICAL	HORIZONTAL
A	0.5 mV/DIV	50 nSEC/DIV
B	0.5 mV/DIV	50 nSEC/DIV
C	0.5 mV/DIV	50 nSEC/DIV
D	0.5 mV/DIV	50 nSEC/DIV

(a)



TRACE	VERTICAL	HORIZONTAL
A	0.5 mV/DIV	50 nSEC/DIV
B	0.5 mV/DIV	50 nSEC/DIV
C	0.5 mV/DIV	50 nSEC/DIV
D	0.5 mV/DIV	50 nSEC/DIV

(b)



TRACE	VERTICAL	HORIZONTAL
A	2 mV/DIV	50 nSEC/DIV
B	2 mV/DIV	50 nSEC/DIV
C	2 mV/DIV	50 nSEC/DIV
D	2 mV/DIV	50 nSEC/DIV

(c)

***Fig 8—Two 565A D/A converters (a and b)** exhibit similar settling times but one **(b)** generates a large glitch at the off-to-on transition. A compression of the glitch appears in **c**.*

PMI

AN-104

RADIATION EFFECTS OF LINEAR INTEGRATED CIRCUITS

Precision Monolithics Inc.

APPLICATION NOTE 104

INTRODUCTION

In the years ahead, the understanding of radiation effects and the radiation hardening of integrated circuits will take on an increasingly important priority. Precision Monolithics Inc. has been actively participating in many programs that require radiation-hard ICs. Through years of involvement and characterization, a good amount of useful radiation hardness data on PMI's products has been generated and is available. This application note is intended to be an introduction to the different radiation environments and their effects on linear integrated circuits. It summarizes the radiation hardness characteristics of a selection of PMI's products. For more in-depth discussions of this important topic, additional sources are referenced in the bibliography.

Many electronic systems may encounter exposure to various radiation environments such as in a nuclear power plant, nuclear explosion, and natural sources. It is vital for these systems to withstand a sufficiently high radiation level and still remain fully functional. The primary effects of radiation are on semiconductor components. The effects range from a mild but recoverable disturbance, or an intermittent failure, to a catastrophic destruction of the components (and therefore the system). Consequently, the system designer must anticipate the worst case radiation environments under which the system must operate; select the appropriate radiation-hard components that can withstand the anticipated environment; and provide some safeguards in the event the worst case is exceeded.

RADIATION ENVIRONMENTS

There are three basic classes of radiation environments which electronic systems are exposed to. The most prominent class is that of very high radiation levels for a very short period of time (nanoseconds to microseconds), such as a nuclear event. Survivability in such environments is crucial for many military systems. The second class is environments which have low levels of natural electron and proton radiation. Spacecraft systems and satellites fall into this category. These types of equipment are required to withstand low-rate cosmic environments for years without suffering appreciable degradation. Although, certain satellites require hardening to survive nuclear events as well. The third class is an environment where there is steady-state gamma and neutron irradiation for a long period of time. This environment is most prevalent in nuclear power generation and fuel reprocessing systems.

In the following sections, three types of radiation will be discussed. They are transient dose radiation, neutron radiation, and total dose radiation. Each type of radiation has markedly different effects on linear integrated circuits. Therefore, the radiation hardening techniques are also different. Several techniques will be presented along with a summary of radiation tolerance of a selection of PMI products.

TRANSIENT DOSE RADIATION

The primary example of transient dose radiation is that which is produced by a nuclear event. It consists of intense pulses of x-rays or gamma rays lasting for up to one microsecond. This form of radiation is also called prompt gamma radiation and is typically measured in rad/sec, where a rad is 100 ergs/gm energy deposited in a specific material. In the case of silicon semiconductors, the units are then rad (Si)/sec.

When gamma rays are absorbed in semiconductor materials, ionization interaction occurs. The high energy absorption separates electrons from their parent atoms and produces large quantities of positive ions and free electrons. The normally minority-carrier dominant semiconductor junctions become highly enhanced with excess charge carriers. With an electric field applied, large amounts of photocurrents flow across the P-N junctions. At light to moderate radiation levels, circuits can be upset or saturated. At higher levels, triggering of parasitic P-N-P-N structures through the substrate can occur. This type of high current latchup may result in device burn-out if adequate protection is not provided (Ref. 4, Ref. 10, Ref. 11). At the extreme dose level, the excess carrier population approaches the doping levels of the semiconductor materials, destroying the semiconductor junction and transforming it into a resistive element. If the power supply currents are not externally limited, large amounts of currents will conduct, which may fuse bond wires or burn-out metal interconnections on the semiconductor circuit.

Linear bipolar ICs tend to be more sensitive than digital MOS ICs. The most sensitive device parameters affecting linear bipolar ICs are leakage current and transistor beta. Furthermore, linear ICs have a much longer recovery time (in hundreds of microseconds) after photocurrents dissipate, compared to digital ICs. CMOS ICs, on the other hand, have inherent P-N-P-N structures which are prone to latchup under irradiation.

TRANSIENT DOSE RADIATION HARDENING TECHNIQUES

The potentially destructive high current saturation under irradiation is prevalent and difficult to prevent. The most important hardening technique from a system designer's perspective is to provide sufficient current limiting for the circuit. Current flowing through a linear IC should be limited to less than one-half ampere, or at a level that burn out will not result. It is prudent to select high frequency part types to allow for bandwidth degradation. In addition, these devices have small geometries, thus limiting the ionization process, reducing photocurrent generation. Indeed, one should select ICs that are inherently radiation hard. These devices tend to have a higher survivability rate and can recover quickly. System designs must take into account the long recovery time (on the order of hundreds of microseconds) of linear ICs after irradiation. Finally, it should be noted that stored charge in an external capacitor can also sustain a large peak current flow in a momentarily saturated, active device. Selection of capacitor values should be chosen to store less than 10μJ of energy.

NEUTRON RADIATION

Neutron bombardment from a nuclear event is the primary cause of this type of radiation. It is measured in fluence of neutrons/cm^2. The uncharged neutrons, when colliding with atoms in the semiconductor lattice, cause permanent displacement, or damage, to the crystal lattice and therefore degrade performance characteristics. The damage decreases minority carrier lifetime and carrier concentration, resulting in beta degradation of transistors in linear ICs. Defects in the lattice structure also increases reverse leakage currents across device junctions. Furthermore, bulk resistance rises dramatically. The beta degradation exhibits some ability to recover. The transient part, and usually the majority, of the degradation anneals out within milliseconds to a second after exposure. The permanent part remains and can only be partially restored by high temperature annealing. But the bulk resistivity changes are essentially permanent.

Once the transistor carrier lifetime and mobilities are degenerated, the f_T (gain-bandwidth) of transistors also suffers. The amount of degradation varies, depending upon the specific process and geometry of the transistors. Neutron radiation has the greatest degradation effect on lateral PNP devices in ICs. Gain and bandwidth usually suffer the most damage.

For operational amplifiers, the main parameters that are most susceptible are the open-loop gain, A_{VOL}; input bias current, I_B; input offset current, I_{OS}; input offset voltage, V_{OS}; and slew rate, SR. Low power op amps which operate on low current levels are particularly sensitive to damage under neutron irradiation environments.

NEUTRON RADIATION HARDENING TECHNIQUES

The degree of hardening required depends on the anticipated amount of radiation exposure a system is designed to withstand. In general, the system designer should choose high frequency components in anticipation of bandwidth degradation. The design should tolerate degradation of I_B, I_{OS}, V_{OS}, A_{VOL}, BW, SR, and Z_{IN} parameters. Where gain parameter drift is critical, use closed-loop design to minimize error. Avoid low power devices where failures are critically disruptive. Finally, shielding should be provided where practical.

TOTAL DOSE RADIATION

This type of radiation refers to a steady state, continuous exposure of gamma rays and x-rays. The primary effect is a cumulative build-up of trapped charges on the surface layers of integrated circuits. Total dose refers to the total dose absorbed over time, which is measured in rads (Si) absorbed. This type of radiation is typically found in spacecraft environments and nuclear power plants.

At low dose levels, the trapped charges within the dielectric layers can cause surface channeling and high surface recombination velocities. The results are increased leakage currents and reduced gain. Depending on the design, various op amps will exhibit degraded input parameters such as input offset voltage, input bias current, and input offset current. Similarly, the open-loop gain and output drive capability also suffer degradation. Typically, a total dose of less than 10 krad (Si) causes no appreciable changes in parameters in bipolar operational amplifiers and comparators. At high dose levels, bulk damage due to silicon displacement can occur with severe and permanent degradation of device parameters.

CMOS integrated circuits are generally more sensitive to total dose radiation. Charges that are trapped in gates and field oxide cause shifts in threshold voltage and device transconductance. Failures may include malfunction and out-of-specification parametric changes.

TOTAL DOSE RADIATION HARDENING TECHNIQUES

Radiation hardening techniques for total dose are very similar to neutron radiation due to the similarity of the degradation effects. Basically, a design should provide sufficient tolerance for degradation in operating parameters of linear ICs. Where practical, extensive shielding should be used.

PMI PRODUCT PERFORMANCE

PMI has been actively involved in performing product radiation characterization using the Scanning Electron Microscope (SEM). SEM has been demonstrated to be an effective tool for predicting the total dose sensitivity of a device. Carefully controlled test sequences have been conducted on separate CO^{60} and SEM sample devices from common wafers. Test data compiled indicated high correlation between the two radiation sources.

The basic methodology for using the SEM as a total dose radiation source has been reported and well-documented in a number of scientific journals over the past several years. The SEM method is currently being used at PMI to identify wafer lots suitable for radiation screening. Table 1 summarizes the relative radiation tolerance of various PMI products. It should be understood that when reviewing the information, the rankings are based on functionality and should serve only as a guide. The suitability of any particular product depends on the application, the expected environment, and the shielding level under consideration. Once the environmental condition is known, the selected device should undergo further evaluation and/or testing to assure its critical parameters will meet the performance requirements of the system involved.

(Note: PMI does not have the in-house capability of performing CO^{60} total dose or neutron irradiations. These tests are performed in conjunction with end users at remote facilities. PMI actively participates in supplying devices into radiation-sensitive applications, but must separately consider each application to supply devices which have been individually or lot screened for radiation hardness. Consult PMI factory to discuss specific requirements and PMI capabilities.)

TABLE 1: Ranking of Radiation Tolerance of Selected PMI Products

Radiation Tolerance Category	Maximum Radiation Level (Rad)	Product/Description
Excellent Performance	Greater than 1 Meg	CMP-01, Fast comparator CMP-02, Fast comparator DAC-08, 8-bit D/A converter DAC-100, 10-bit D/A converter OP-15, High-speed FET-input op amp OP-16, High-speed FET-input op amp OP-17, High-speed FET-input op amp REF-01, +10V precision reference REF-02, +5V precision reference SW-01, Quad analog switch SW-02, Quad analog switch SW-05, Dual analog switch SW-06, Quad analog switch SW-201, Quad analog switch SW-202, Quad analog switch
Good Performance	500k—1 Meg	AMP-01, Precision instrumentation amp MAT-01, Matched transistor pair OP-01, High-speed op amp OP-02, High-speed op amp OP-05, Low-noise precision op amp OP-06, Low-noise precision op amp OP-07, Low-noise precision op amp OP-08, Low-input-current op amp OP-12, Low-input-current op amp OP-27, High-speed, low-noise precision op amp OP-37, High-speed, low-noise precision op amp PM-108, Low-input-current op amp
Moderately Sensitive	250k—500k	CMP-404, Quad low-power comparator MUX-08, Analog multiplexer PM-111, Precision comparator PM-139, Quad low-power comparator
Sensitive	100k—250k	CMP-04, Low-power comparator OP-20/21, Low-power op amps OP-22/32, Programmable low-power op amps OP-220/221, Dual low-power op amps OP-420/421, Quad low-power op amps

PMI continues to collect radiation tolerance data on its product line. The following summarizes the critically affected parameters of each product and its radiation tolerance level. Its intent is to provide a relative point of reference to the system designer. The ratings are based on collected radiation data available at the time of this printing. From time to time, products undergo design improvements which may impact the relative radiation tolerance of these devices. Designers are urged to consult PMI factory for additional information.

D/A Converters

DAC-08, 8-Bit D/A Converter

Excellent radiation performance. Survives 3×10^6 rads total dose. Widely used as an industry-standard device in military and space applications.

DAC-100, 10-Bit D/A Converter

Excellent radiation performance. Virtually no degradation at 1×10^6 rads total dose. Industry-standard device in military and space applications.

Operational Amplifiers

OP-01/02, High-Speed Op Amps

Good radiation performance. I_B increases 20 times (20X), A_{VO} decreases 10X, minimal V_{OS} degradation to 1×10^6 rads.

OP-05/06/07, Low-Noise Precision Op Amps

Good radiation performance. I_B increases 200X, A_{VO} decreases 10X, minimal V_{OS} degradation to 1×10^6 rads.

OP-08/OP-12/PM-108, Low-Input-Current Op Amps

Good radiation performance. Very lot-process dependent. I_B degradation ranges from 20X to 70X depending on production lot. V_{OS} shows some degradation at 1×10^6 rads and A_{VO} degrades 50X to 100X depending on the lot. Output drive capability degrades significantly at 1×10^6 rads.

OP-09/11, Quad General-Purpose Op Amps

Good radiation performance. I_B and A_{VO} degradation range 15X to 30X at 1×10^6 rads. Some V_{OS} sensitivity.

OP-15/16/17, High-Speed, FET-Input Op Amps

Excellent radiation performance. Very little degradation on all precision parameters at 1×10^6 rads. I_B shows some sensitivity to junction leakages at 1×10^6 rads, but still performs well.

OP-20/21/22/32/220/221/420/421, Low-Power Op Amps

Sensitive devices. Low-power device family operates at low current which makes them susceptible to radiation damage. Good performance at low level radiation (<100 krads range).

OP-27/37, High-Speed, Low-Noise Op Amps

Good radiation performance. Minimal V_{OS} degradation, A_{VO} degrades 2X, and I_B increases 250X at 1×10^6 rads. Good high-gain, low V_{OS} device in radiation environment.

OP-77, Low-Noise Precision Op Amp

Excellent radiation performance. Virtually no V_{OS} degradation, A_{VO} remains greater than 1 million, I_B increases 100X at 1×10^6 rads. Excellent post radiation op amp characteristics.

Comparators

CMP-01/02, Fast Comparators

Excellent radiation performance. Low V_{OS}, V_{SAT} drift, minimal change in response time, and I_B increases 15X to 20X at 1×10^6 rads.

CMP-04, Quad Low-Power Comparator

Sensitive device. Production lot dependent. Some V_{OS} sensitivity, I_B increases 30X at 250 krads. Device non-functional at greater than 250 krad. Good comparator for low level radiation applications.

CMP-404, Quad Low-Power Comparator

Moderately sensitive device. V_{OS} maintains low values up to 100 krads. I_B increases 15X to 30X at 250 krads. Device becomes non-functional above 500 krads. Good for low level radiation environments.

PM-111/211, Precision Comparators

Moderately sensitive device. Good performance up to 500 krads. Becomes non-functional above 500 krads. Good comparator for moderate radiation levels.

PM-139, Quad Low-Power Comparator

Moderately sensitive device. Good performance up to 500 krads. Has proven track-record in many military and space programs.

Other Linear Devices

AMP-01, Low-Noise Instrumentation Amp

Good radiation performance. Maintains high-gain and low V_{OS} above 1×10^6 rads. I_B increases 200X to 300X at 1×10^6 rads.

REF-01/02, Precision References

Excellent radiation performance. No degradation in line regulation; load regulation degrades by 2X at above 1×10^6 rads.

SW-01/02/05/06/201/202, Analog Switches

Excellent radiation performance. Very little degradation at 1×10^6 rads. Used in a number of military and space programs.

MUX-08/24, Analog Multiplexers

Moderately sensitive device. Input logic current increases 30X to 40X at 500 krads. Maintains functionality up to 500 krads. Good performance at less than 500 krads.

MAT-01, Matched Transistor Pair

Good radiation performance. Maintains high breakdown voltage; beta degrades 2X at high current levels and 10X at lower current levels at 1×10^6 rads.

CONCLUSION

Radiation environments create a myriad of challenges for the system designers. Since the primary impact of radiation on a system is performance degradation in semiconductor devices, then, appropriately, radiation hardening begins at the component level. The hardness of a linear IC depends largely on its fabrication process, circuit topology, and circuit layout. Each device type must be characterized under irradiated test conditions, in order that the designer can select the appropriate devices to minimize the impact which a radiation environment will have on the system. A fundamental design philosophy should be one of designing into the system adequate allowance for component degradation and still perform the intended function. This implies the system designers should select components with the optimum trade-off between the best initial specifications and a set of acceptable post-radiation specifications, provide safe current limiting protection in the event dangerously high radiation levels persist, and finally, provide sufficient radiation shielding.

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APPLICATION NOTE 105

The MAT-04 is a monolithic device containing four low-noise, tightly matched transistors, which dramatically improves the performance of many amplifier and analog computational circuits. This note describes several of these designs which capitalize on the superior characteristics and dynamic range of the MAT-04. These applications include a low-distortion voltage-controlled attenuator, a very low-noise ($1.2nV/\sqrt{Hz}$) high-speed instrumentation amplifier, a $900pV/\sqrt{Hz}$ ultra-low noise audio preamplifier, a vector summing amplifier, a squaring amplifier, and a square-root amplifier.

Discrete circuit designers repeatedly run into the problem of circuit component mismatches that limit performance. Passive component mismatching can be reduced by using tighter tolerance components, but active components present a more difficult problem. Discrete transistors exhibit poor beta and $V_{BE(ON)}$ matching, even within single transistor families, which severely degrade amplifier performance. Most available transistor arrays however, were developed to save board space rather than to provide accurate parametric matching. Only a few are designed to have tight matching tolerance.

The MAT-04 uses advanced layout and process techniques to guarantee that the offset voltage between **any** two transistors in the device will be no more than $200\mu V$, and beta mismatch will not exceed 2%. Additionally, the MAT-04 transistors are designed for high beta (400 minimum) and 40V minimum breakdown. It exhibits a low 0.4Ω bulk resistance, which is important in logarithmic circuit applications. The MAT-04 uses a symmetrical quad transistor pinout (Figure 1) which allows incorrect orientation of pin 1 without damage. The base-emitter junctions are internally diode-protected against reverse zener breakdown, which protects against degradation of beta and matching characteristics.

VOLTAGE-CONTROLLED ATTENUATOR

A useful MAT-04 application is the Voltage-Controlled Attenuator (VCA) of Figure 2. This circuit, widely used in professional audio applications, is difficult to implement using discrete transistors due to distortion induced by transistor mismatching. The MAT-04 offers excellent matching which

FIGURE 1: Pin Connections

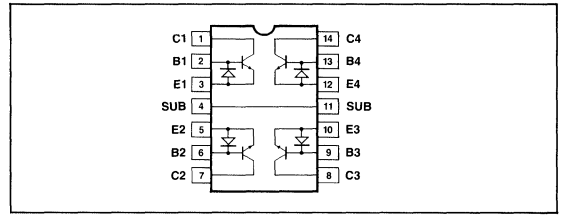
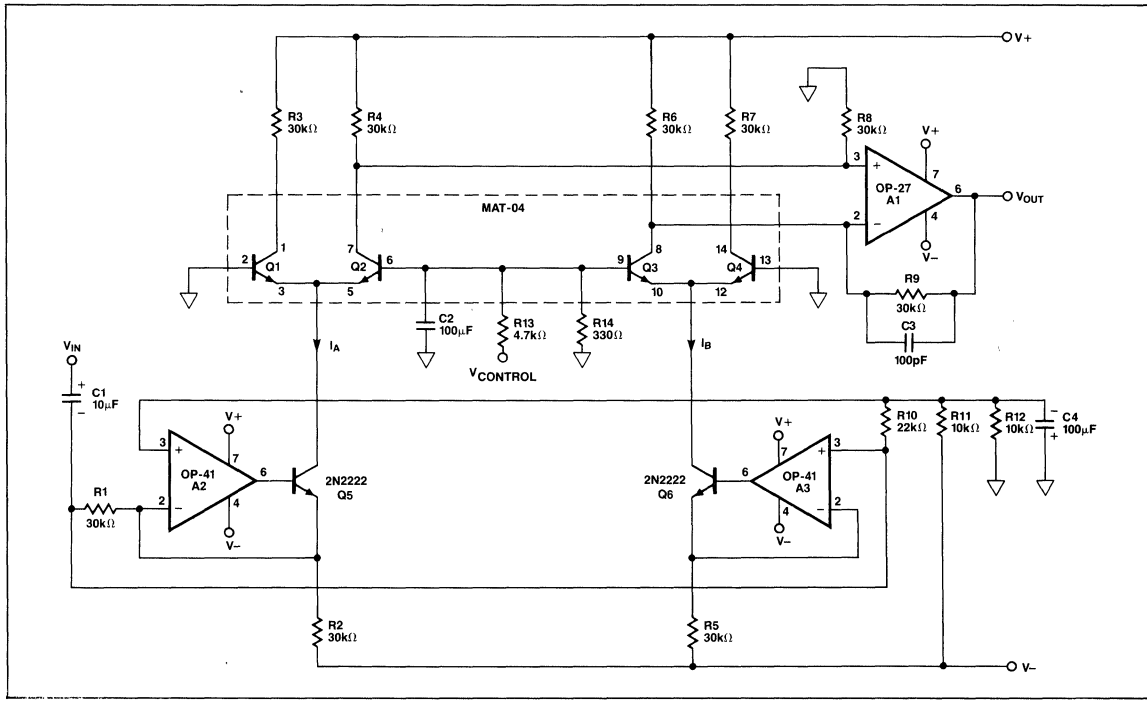


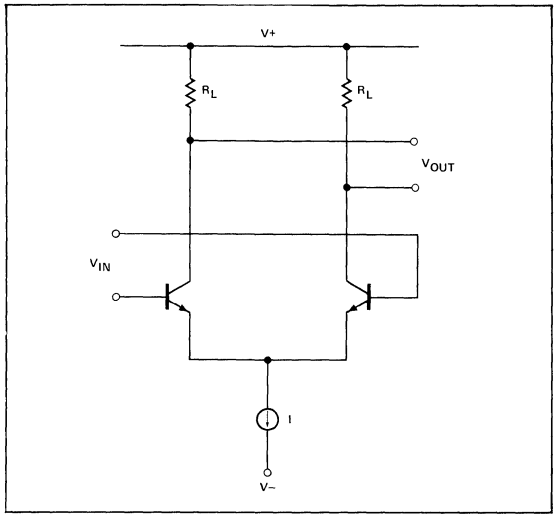
FIGURE 2: Voltage-Controlled Attenuator



dramatically reduces distortion. The VCA provides low-distortion attenuation over a wide range of control voltages, and can be used as a low-distortion gain control in an audio amplifier.

The VCA design is based upon the amplifying characteristics of a differential pair. Figure 3 shows the classic differential pair. With zero volts between the inputs (V_{IN} = 0V), the current in each side of the differential pair is equal and therefore the output voltage equals zero. Small changes in V_{IN} unbalance the currents flowing in each side of the differential pair and produce an amplified differential output. The total stage current (I) of the differential pair is constant regardless of the input voltage. Matching of the transistors in a differential pair is critical, as any device mismatch will cause DC errors and upset linearity.

FIGURE 3: Classic Differential Pair



In the Voltage-Controlled Attenuator, the input signal modulates the stage currents of the two differential amplifier stages. Op amps A2 and A3, in conjunction with transistors Q5 and Q6, form two voltage-to-current converters that transform a single input voltage into differential currents, which form the stage currents I_A and I_B (see Figure 2) of each differential pair. The transfer function of the voltage-to-current converter is:

$$(1)\quad I_A = \frac{-V_{IN}}{R2}$$

$$(2)\quad I_B = \frac{V_{IN}}{R5}$$

Low-cost unmatched transistors can be used for Q5 and Q6, since they are inside the feedback loop of op amps A2 and A3. Their beta mismatch has minimal effect on output offset.

If all the bases of the MAT-04 are at ground potential, then the stage currents of each differential pair split equally among each transistor. The output is taken from one side of each differential pair (Q2 and Q3) and converted to a single-ended signal by op amp A1 which has a stage gain of 1. The gain of the overall circuit with the bases of the MAT-04 at ground potential is:

(3)

$$\frac{V_{OUT}}{V_{IN}} = \left[\left(\frac{1}{2}\right)(V_{IN})\left(\frac{R6}{R5}\right)\right] - \left[\left(-\frac{1}{2}\right)(V_{IN})\left(\frac{R4}{R2}\right)\right]$$

$$= V_{IN}\,\frac{(R2 \cdot R6 + R4 \cdot R5)}{(2R2 \cdot R5)}$$

and since R2 = R4 = R5 = R6, $\frac{V_{OUT}}{V_{IN}} = 1$

When a positive control voltage is applied, most of the stage current is diverted into transistors Q2 and Q3, resulting in an increase in circuit gain. However, when a negative control voltage is applied, most of the stage current is diverted through transistors Q1 and Q4, with a subsequent decrease in circuit gain.

The ideal transfer function for the Voltage-Controlled Attenuator is:

$$(4)\quad \frac{V_{OUT}}{V_{IN}} = \frac{2}{1+\exp\left[\dfrac{(-V_{CONTROL})\left(\dfrac{R14}{R13+R14}\right)}{\left(\dfrac{kT}{q}\right)}\right]}$$

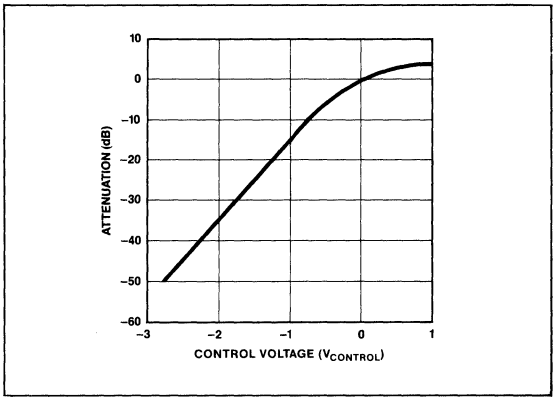
where k = Boltzmann constant = $\frac{1.38 \times 10^{-23}\ J}{°K}$

T = temperature in °K

q = electronic charge = 1.602×10^{-19} C

From the transfer function, it can be seen that the maximum gain of the circuit is 2 (6dB). Figure 4 shows the increase in attenuation as the control voltage becomes more negative.

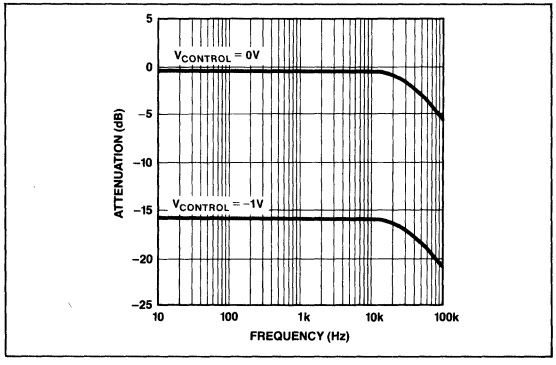
FIGURE 4: Voltage-Controlled Attenuator, Attenuation vs Control Voltage at 1kHz, 25°C



The Voltage-Controlled Attenuator accepts a 3Vrms input and easily handles the full 20Hz — 20kHz audio bandwidth as indicated in Figure 5. Distortion typically runs under 0.03% and the noise level is more than 110dB below maximum output.

To insure best performance, resistors R2 through R7 should be 1% metal film resistors. Since capacitor C2 can see a small amount of reverse bias when the control voltage is positive, a nonpolarized tantalum capacitor or two polarized capacitors connected back-to-back should be used.

FIGURE 5: Voltage-Controlled Attenuator, Attenuation vs Frequency



A LOW-NOISE, HIGH-SPEED INSTRUMENTATION AMPLIFIER

The circuit of Figure 6 has performance characteristics which make it ideal for use in high precision transducer and professional audio applications. The circuit uses a high-speed op amp, the OP-17, preceded by an input amplifier consisting of a precision matched dual transistor, the MAT-02, and a MAT-04. The arrangement of the MAT-04 is known as a "linearized cross quad" and acts as a voltage-to-current converter to provide feedback to the input stage. The OP-17 acts as an overall nulling amplifier to complete the feedback loop. Resistor pair R1 and R2, and resistor pair R3 and R4 form voltage dividers that attenuate the output feedback due to the limited input range of the "cross quad" arrangement. Biasing for the input stage is set by zener diode Z1. At low currents, the effective zener voltage is about 3.3V due to the soft knee characteristic of the zener diode. This results in a bias current of 530μA per side for the input stage.

The gain of the instrumentation amplifier, with the values shown in Figure 6, is:

$$(5)\quad \frac{V_{OUT}}{V_{IN}} = \frac{33{,}000}{R_G}$$

FIGURE 6: Low-Noise, High-Speed Instrumentation Amplifier

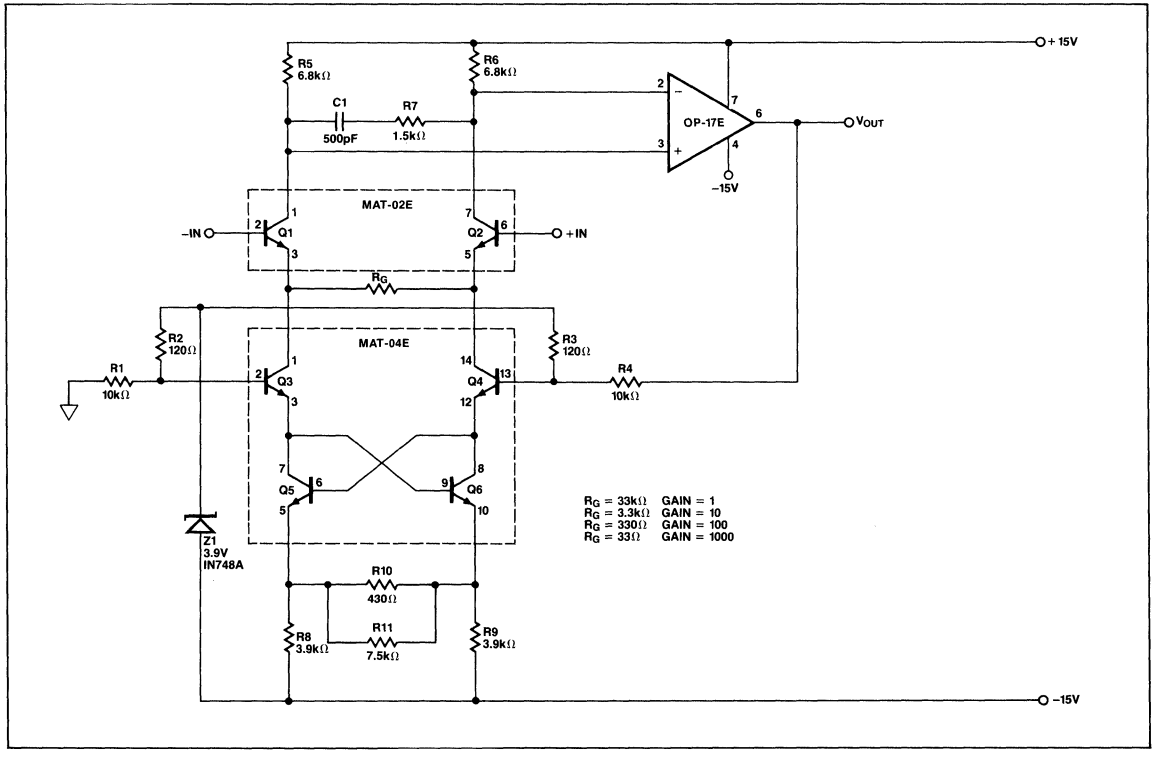


TABLE 1

Input Noise Voltage Density	G = 1000 G = 100 G = 10	1.2nV/$\sqrt{Hz}$ 3.6nV/$\sqrt{Hz}$ 30nV/$\sqrt{Hz}$
Bandwidth	G = 500 G = 100 G = 10	400kHz 1MHz 1.2MHz
Slew Rate		40V/μs
Common-Mode Rejection	G = 1000	130dB
Distortion	G = 100 f = 20Hz to 20kHz	0.03%
Settling Time	G = 1000	10μs
Power Consumption		350mW

FIGURE 7: Spot Noise of Discrete Instrumentation Amplifier at Gain = 1000 from 0 to 25kHz

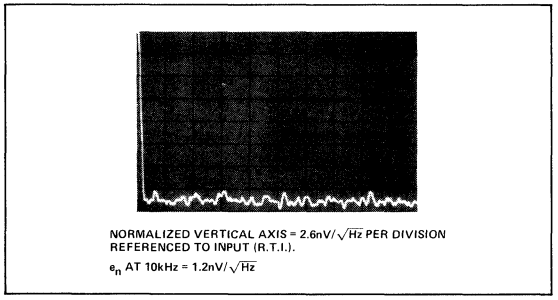
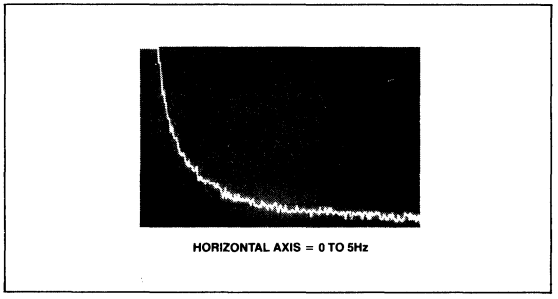


FIGURE 8: Low Frequency Noise Spectrum Showing Low 2Hz Noise Corner; Gain = 1000



The performance of the amplifier is summarized in Table 1. Figure 7 shows the input-referred spot noise to be flat at about 1.2nV/$\sqrt{Hz}$ over the 0 — 25kHz bandwidth. Figure 8 shows the low frequency noise spectrum which highlights the low 1/f noise corner at 2Hz.

In situations where small output, low impedance transducers are used, such as strain gages, amplifiers must have low voltage noise to maintain a good signal-to-noise ratio. The low voltage noise of 1.2nV/$\sqrt{Hz}$ suits this instrumentation amplifier for use in many low impedance transducer applications.

A LOW-NOISE HI-FI QUALITY PREAMPLIFIER

The AC-coupled preamplifier of Figure 9 exhibits an input-referred noise voltage density of only 900pV/$\sqrt{Hz}$ at a gain of 200. Preamplifier noise is minimized by using a single-ended input stage consisting of three transistors of a MAT-04 connected in parallel. This technique lowers the effective base-spreading resistance, reducing thermal noise from this source by a factor of $\sqrt{3}$. Tight matching of the three paralleled transistors is a critical requirement. If the matching is poor, one transistor will steal most of the stage current, effectively removing the two other transistors from the circuit. Noise reduction, achieved by paralleling the transistors, would therefore be lost. Schottky noise, or shot noise, is minimized by using a relatively high stage current of 2mA.

The fourth transistor (Q1) of the MAT-04 is used to bias the input stage. Op amp A1 forces the voltages across R1 and R2 to be equal, setting the bias current at 2mA. Overall feedback for the preamplifier is provided by resistors R7 and R8. Gain for this circuit is:

$$(6)\quad \frac{V_{OUT}}{V_{IN}} = \frac{R8 + 5\Omega}{5\Omega}$$

The circuit is characterized with the gain of 200. Compensation components R3 and C2 may need to be optimized for other values of gain. Open-loop gain of the preamplifier is over 10 million.

Figure 10 illustrates the wide bandwidth of the preamplifier. Figure 11 shows the broadband noise spectrum (0 — 25kHz) to be flat at 900pV/$\sqrt{Hz}$. Distortion of the preamplifier is 0.035% at $V_{OUT} = 10V_{p-p}$, f = 10kHz.

FIGURE 9: Low-Noise AC Preamplifier

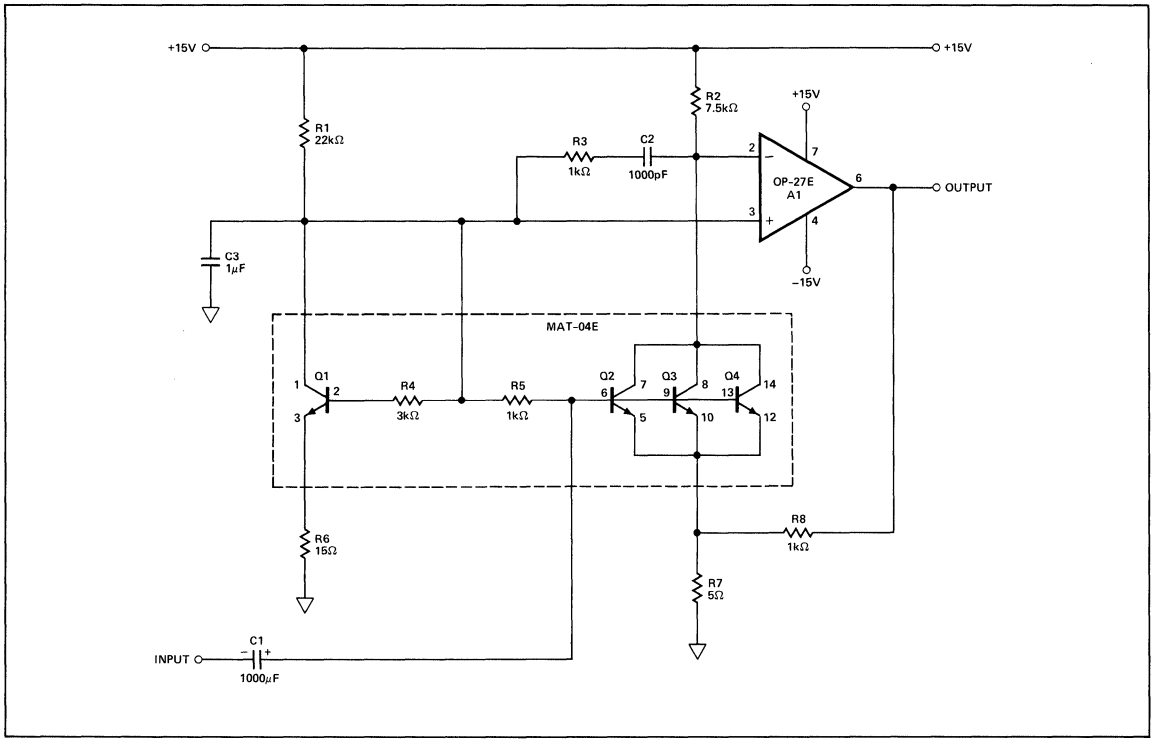


FIGURE 10: Low-Noise AC Preamplifier, Gain vs Frequency

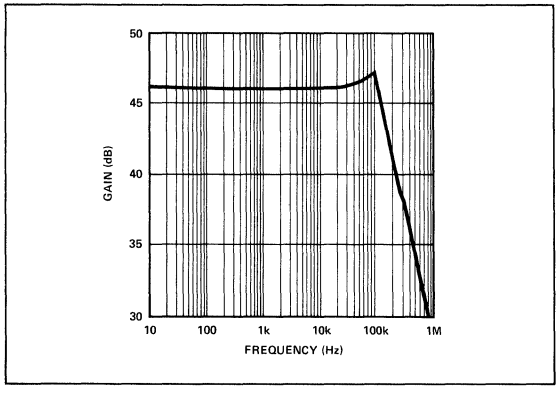
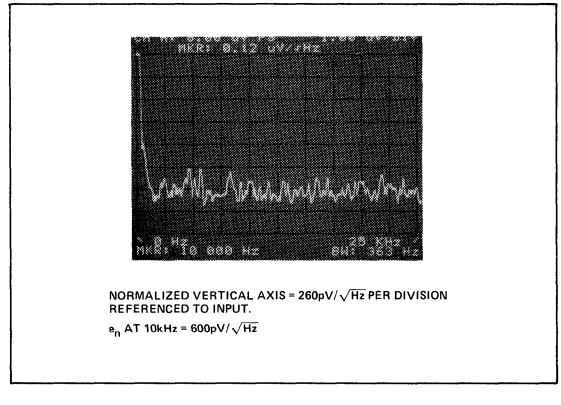


FIGURE 11: Spot Noise of AC Preamplifier at Gain = 200 from 0 to 25kHz



NONLINEAR CIRCUIT APPLICATIONS

Another application area where precision matched transistors are a powerful tool is in the generation of nonlinear functions. These are based upon the transistor's logarithmic property which has the following form:

$$(7)\quad V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$$

where: $V_T = \frac{kT}{q}$

I_S = saturation current

The circuit of Figure 12 is a vector summing amplifier that has the following generalized transfer function:

(8) $V_{OUT} = k\sqrt{V_A^2 + V_B^2}$

where k is a scale factor

The circuit (see Figure 12) consists of two log amplifiers each using two transistors and an op amp. The voltage across the series transistors Q1 and Q2 is equal to the voltage across Q3 and the base-emitter of Q4. Summing this voltage loop leads to:

(9) $V_{T1}\ln\left(\frac{I_1}{I_{S1}}\right) + V_{T2}\ln\left(\frac{I_2}{I_{S2}}\right) = V_{T3}\ln\left(\frac{I_A}{I_{S3}}\right) + V_{T4}\ln\left(\frac{I_{OUT}}{I_{S4}}\right)$

All transistors are precisely matched and at the same temperature, therefore the I_S and V_T terms cancel. Equation 9 is simplified to:

(10) $2\ln I_1 = \ln I_A + \ln I_O = \ln(I_A \cdot I_O)$

Exponentiating both sides yields:

(11) $I_1^2 = I_A \cdot I_O$

Similar analysis for transistors Q7, Q6, Q5, and Q4 leads to:

(12) $I_2^2 = I_B \cdot I_O$

Summing the currents at the emitter of Q4 gives:

(13) $I_O = I_A + I_B$

Solving equations (11) and (12) for I_A and I_B, and substituting into equation (13) yields:

(14) $I_O = \frac{I_1^2}{I_O} + \frac{I_2^2}{I_O} = \sqrt{I_1^2 + I_2^2}$

Op amp A3 forms a current-to-voltage converter giving $V_{OUT} = I_O \cdot R2$,

(15) $V_{OUT} = R2\sqrt{\left(\frac{V_A}{R1}\right)^2 + \left(\frac{V_B}{R3}\right)^2}$

For the circuit of Figure 12, R1 = R3, and $R2 = \frac{R1}{\sqrt{2}}$,

(16) $V_{OUT} = \left(\frac{1}{\sqrt{2}}\right)\sqrt{V_A^2 + V_B^2}$

A value of $R1/\sqrt{2}$ for resistor R2 builds in a scale factor of $1/\sqrt{2}$, which allows +10V to be applied to both inputs simultaneously without the danger of V_{OUT} exceeding the output range of op amp A3. The built-in protection diodes on the MAT-04 allow the input voltages to go negative without damaging the MAT-04. Under this condition, the output voltage is zero. The interconnections of the two MAT-04s in the circuit reduce errors due to inherent mismatching and temperature-induced differences between the two matched quad transistors. The accuracy of the vector summing amplifier is better than 0.5% over an input range of 10mV to 10V.

The MAT-04 can also be used to implement other nonlinear functions such as the square and square-root circuits shown in Figures 13 and 14 respectively. Similar to the vector summing amplifier, the analysis begins by summing the voltages across transistors Q1, Q2, Q3, and Q4 of the squaring circuit shown in Figure 13;

(17) $V_{T1}\ln\left(\frac{I_{IN}}{I_{S1}}\right) + V_{T2}\ln\left(\frac{I_{IN}}{I_{S2}}\right)$

$= V_{T3}\ln\left(\frac{I_O}{I_{S3}}\right) + V_{T4}\ln\left(\frac{I_{REF}}{I_{S4}}\right)$

FIGURE 12: Vector-Summing Amplifier

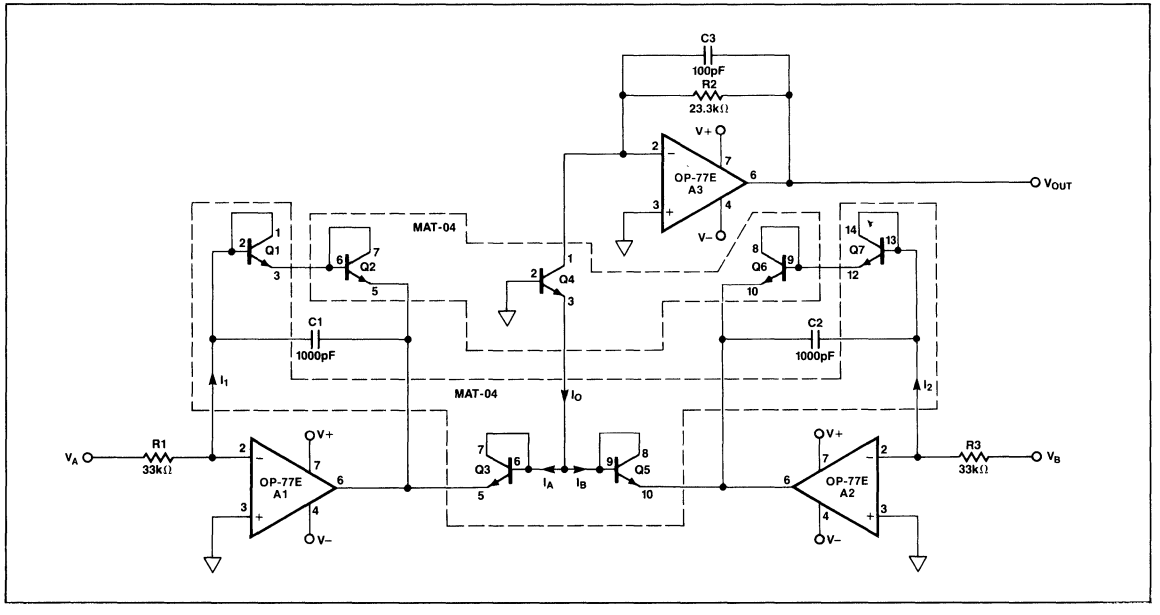


FIGURE 13: Squaring Amplifier

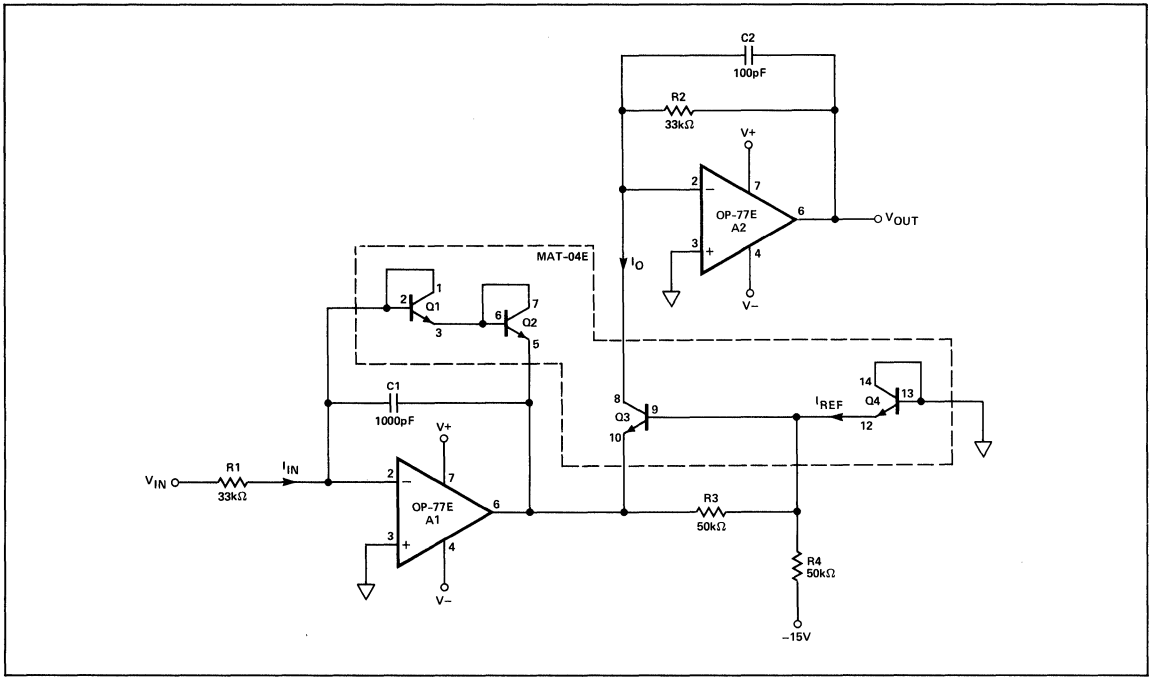
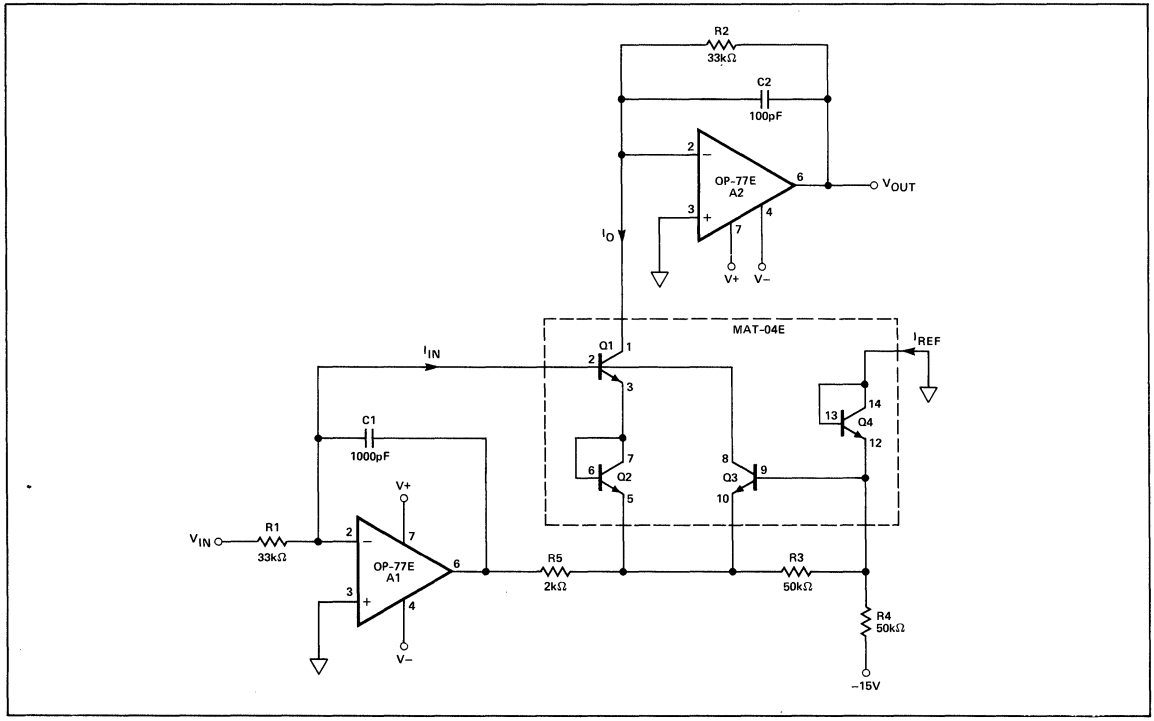


FIGURE 14: Square-Root Amplifier



Once again, all the transistors are precisely matched and at the same temperature, so the I_S and V_T terms cancel giving:

$$(18)\quad 2\ln I_{IN} = \ln I_O + \ln I_{REF} = \ln(I_O \cdot I_{REF})$$

Exponentiating both sides of the equation leads to:

$$(19)\quad I_O = \frac{(I_{IN})^2}{I_{REF}}$$

Op amp A2 forms a current-to-voltage converter which gives $V_{OUT} = R2 \cdot I_O$. Substituting $(V_{IN}/R1)$ for I_{IN} and equation (19) for I_O yields:

$$(20)\quad V_{OUT} = \left(\frac{R2}{I_{REF}}\right)\left(\frac{V_{IN}}{R1}\right)^2$$

A similar analysis made for the square-root circuit of Figure 14 leads to its transfer function:

$$(21)\quad V_{OUT} = R2\sqrt{\frac{(V_{IN})(I_{REF})}{R1}}$$

In these circuits, I_{REF} is a function of the negative power supply. To maintain accuracy, the negative supply should be well regulated. For applications where very high accuracy is required, a voltage reference may be used to set I_{REF}. An important consideration for the squaring circuit is that a sufficiently large input voltage can force the output beyond the operating range of the output op amp. Resistor R4 can be changed to scale I_{REF}, or R1 and R2 can be varied to keep the output voltage within the usable range.

Unadjusted accuracy of the square-root circuit is better than 0.1% over an input voltage range of 100mV to 10V. For a similar input voltage range, the accuracy of the squaring circuit is better than 0.5%.

In summary, the accuracy of nonlinear circuits depends heavily upon the logarithmic conformance of the transistors used in the circuit. Extrinsic resistances and the Early effect cause a deviation from the ideal logarithmic transistor behavior. For small values of V_{CB}, the collector-base voltage, these effects can be lumped together as an effective bulk resistance, r_{BE}. The logarithmic transistor relationship of equation (7) changes to:

$$(22)\quad V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) + (I_C\, r_{BE})$$

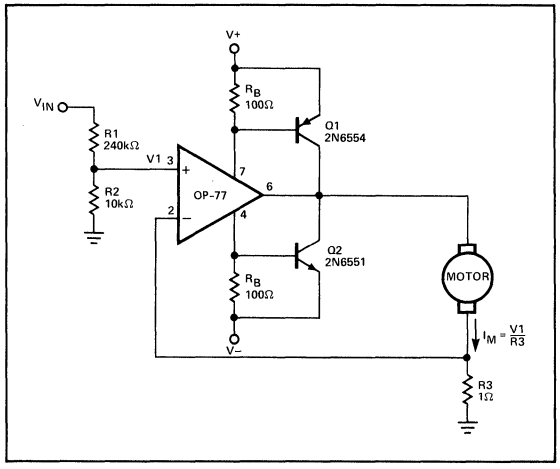
An obvious way to reduce r_{BE}-induced error in nonlinear circuits is to reduce the maximum collector currents, but the op amp offsets and leakage currents become a limiting factor at low input levels. An operating range of 10μA to 1mA is recommended. The MAT-04, which is specifically designed to have a low bulk resistance of 0.4Ω, further reduces r_{BE}-induced error in nonlinear circuits.

APPLICATION NOTE 106

This note examines some of the numerous and widely-used applications of the operational amplifier. While not attempting to list every possible application, it presents several basic circuit configurations that can be modified to suit applications other than those listed. In each case, significant op amp or circuit characteristics are discussed to aid the user in adapting the circuit to a particular need. Table 1 provides an index to the applications contained in this note.

TABLE 1: Op Amp Circuit Applications

FIGURE 1: ±200mA Servo Motor Amplifier



R_B sets the bias point for transistors Q1 and Q2. Because $V_{BE(ON)}$ varies greatly with temperature, a guardband is required to prevent Q1 and Q2 from conducting simultaneously. R_B should be selected such that the transistors do not conduct until I_M equals the op amp quiescent supply current, I_{SY}. The transistors will begin to conduct at about $V_{BE\,(ON)} = 0.5V$.

In this design,

$$R_B = \frac{V_{BE(ON)}}{I_{SY} + I_M} = \frac{0.5}{0.0025 + 0.0025} = 100\Omega$$

To maximize voltage swing across the motor, V1 must be minimized. If at full load V1 = 0.2V with V+ = 15V and V_{BE1} = 0.8V, the voltage across the motor will be:

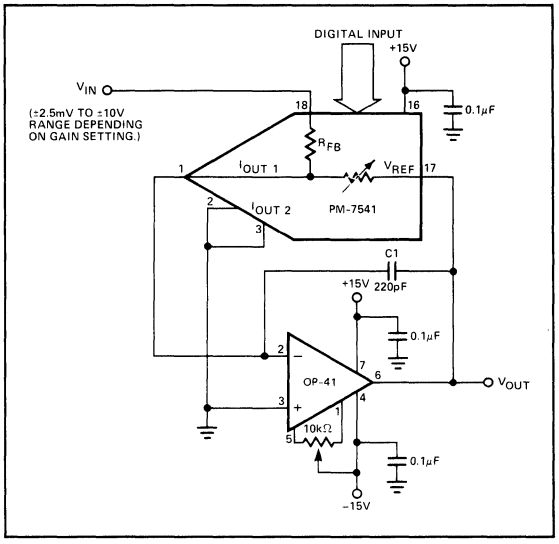
$$V_M = (V^+ - 2) - V_{BE1} - V1 = (15 - 2) - 0.8 - 0.2$$
$$= 12.0V$$

V_{IN} may be scaled with a resistive divider as:

$$\frac{V_{IN}}{V1} = \frac{R1 + R2}{R2}$$

With R1 = 240kΩ and R2 = 10kΩ, V_{IN} = 5V will produce I_M = 200mA.

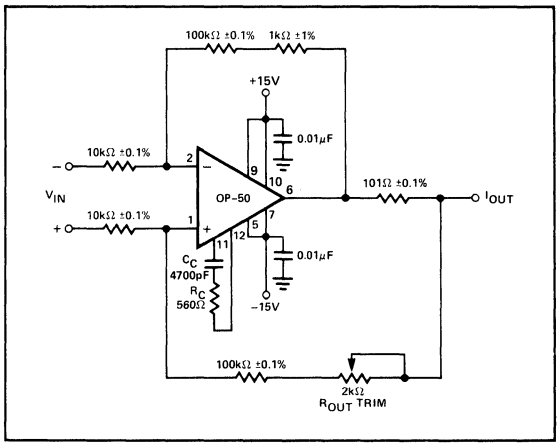
FIGURE 2: Precision Programmable Gain Amplifier



The digitally programmable gain has 12-bit accuracy over the range of −1 to −1024 and 10-bit accuracy to −4096. The low bias current of the OP-41's JFET input maintains this accuracy, while C1 limits the noise voltage bandwidth allowing accurate measurement down to microvolt levels.

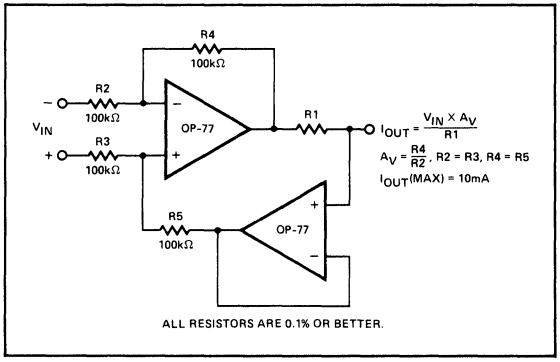
DIGITAL IN	GAIN (A_V)
4095	−1.00024
2048	−2
1024	−4
512	−8
256	−16
128	−32
64	−64
32	−128
16	−256
8	−512
4	−1024
2	−2048
1	−4096
0	OPEN LOOP

FIGURE 3: Bilateral Current Source



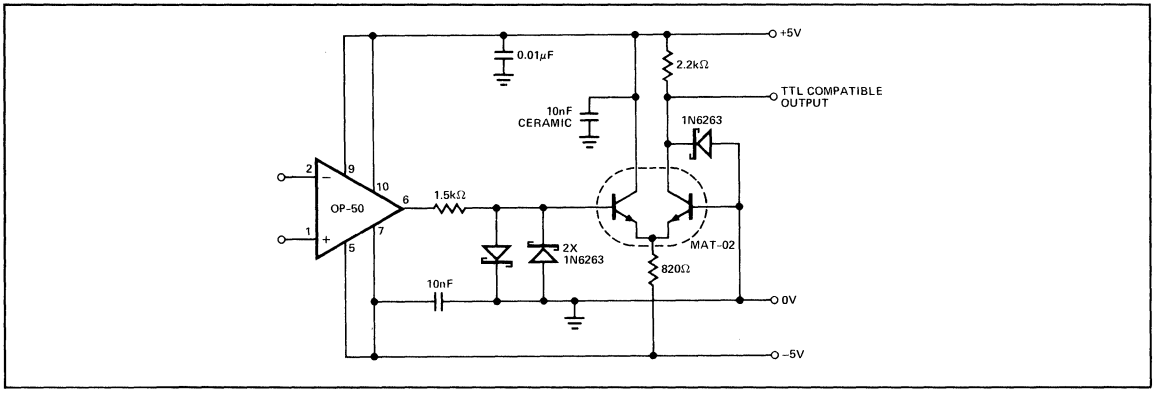
Compliance is better than ±11V at an output current of 20mA, and the trimmed output resistance is typically 2MΩ with $R_L \leq 500\Omega$. For the resistor values shown, the maximum V_{IN} is 200mV.

FIGURE 4: Precision Current Pump



Accuracy of I_{OUT} is improved by using a noninverting voltage-follower in the feedback loop. To maximize voltage compliance of I_{OUT}, R1 should be minimized.

FIGURE 5: High-Sensitivity Voltage Comparator



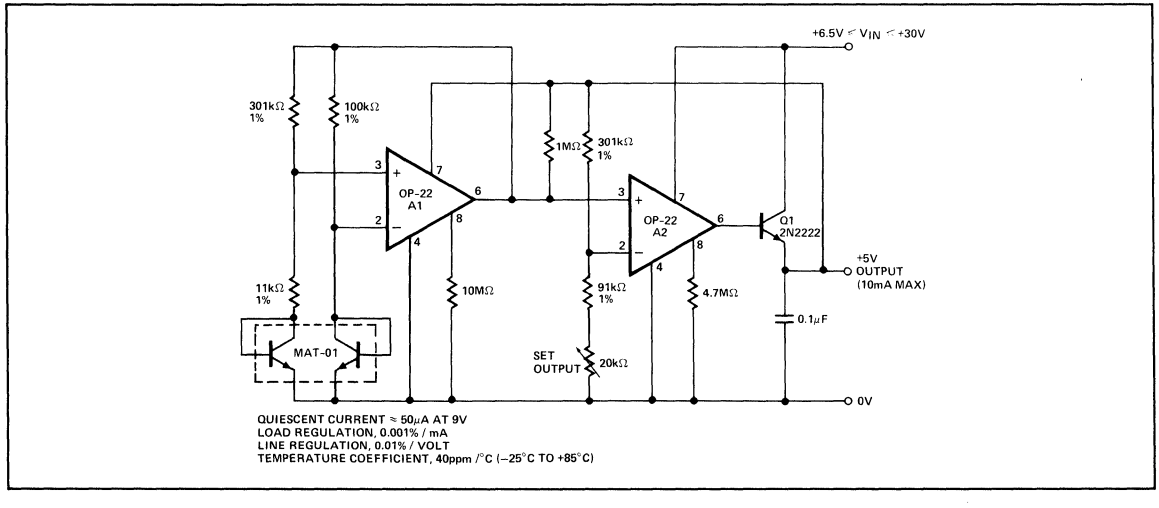
This comparator circuit is capable of resolving a submicrovolt difference signal. The OP-50, operating without feedback, drives a second gain stage which generates a TTL-compatible output signal. Schottky-clamp diodes prevent overdriving of the long-tailed transistor pair and stop saturation of the output transistor. Power supply voltage is set to ±5V to lower the quiescent power dissipation and minimize thermal feedback due to output stage dissipation. Operating from ±5V supplies also reduces the OP-50 rise and fall times as the output slews over a reduced voltage range. This, in turn, reduces the output response time.

It is common practice with voltage comparators to ground one input terminal and to use a single-ended input. The historic reason is poor common-mode rejection on the input stage. In contrast, the OP-50 has very high common-mode rejection and is capable of detecting microvolt level differences in the presence of large common-mode signals.

The comparator is not fast, but it is very sensitive and can detect signal differences as low as 0.3μV. With large input overdrives, the circuit responds in approximately 3μs. If sharp transitions are needed, the use of a TTL Schmitt-trigger input is recommended. A table of Response Time vs. Input Overdrive is shown below.

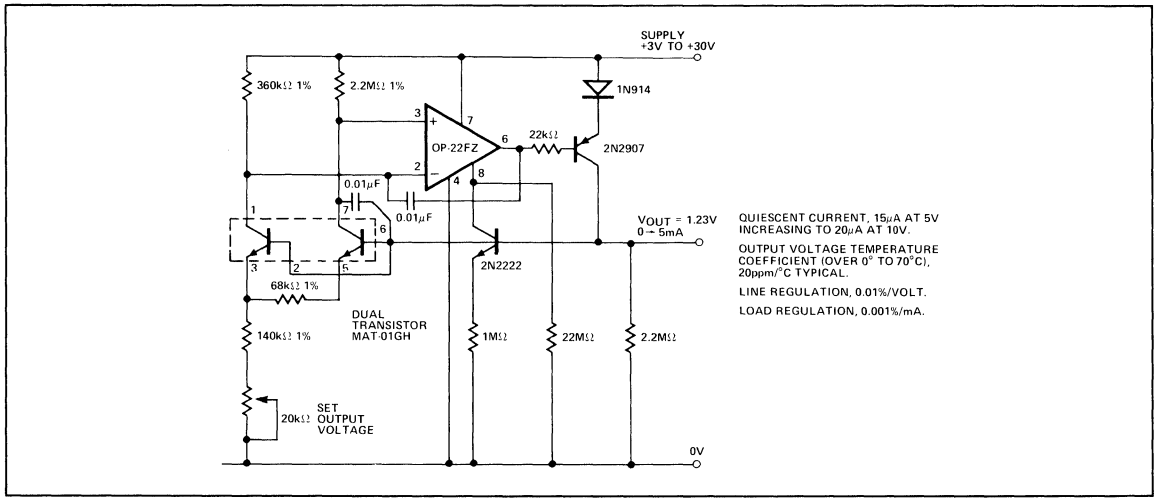
INPUT OVERDRIVE	100mV	10mV	1mV	100μV	10μV
Positive Output Delay	3.2μs	5μs	40μs	340μs	2.4ms
Negative Output Delay	1.8μs	5μs	50μs	380μs	4.5ms

FIGURE 6: Micropower 5V Regulator



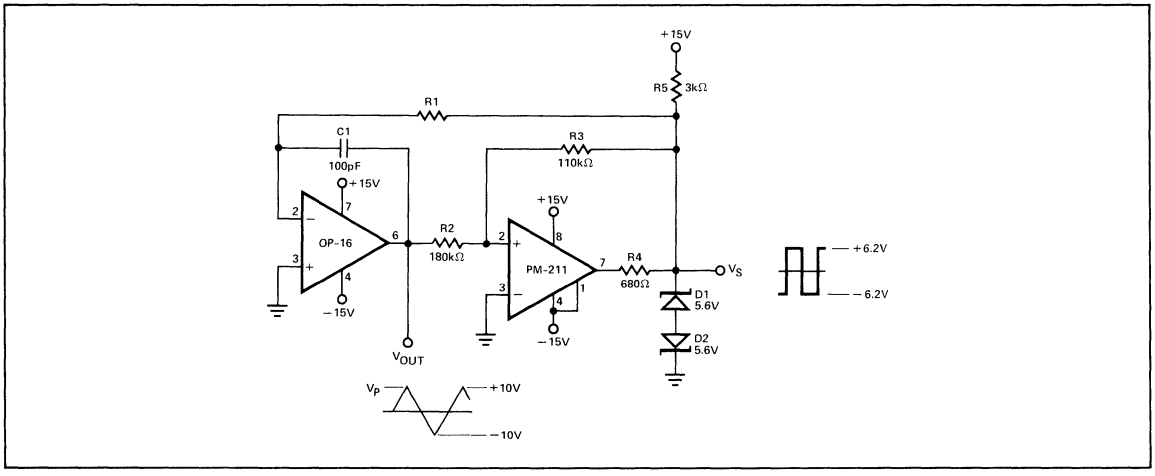
This 5V regulator is ideal for instrumentation requiring good power efficiency. Low-power 3-terminal IC regulators typically draw 2mA to 5mA quiescent current compared to only 50μA with this discrete implementation. Maximum load current is 10mA as shown, and can be increased by changing Q1 to a power transistor and proportionately increasing the set current of A2.

FIGURE 7: Micropower 1.23V Bandgap Reference



A micropower bandgap voltage reference operating at a quiescent current of 15μA may be constructed using an OP-22 and a MAT-01 dual transistor. The circuit provides a 1.23V reference with better performance than micropower IC shunt regulators and has the advantages of being a series regulator.

FIGURE 8: Versatile Triangular Wave Generator



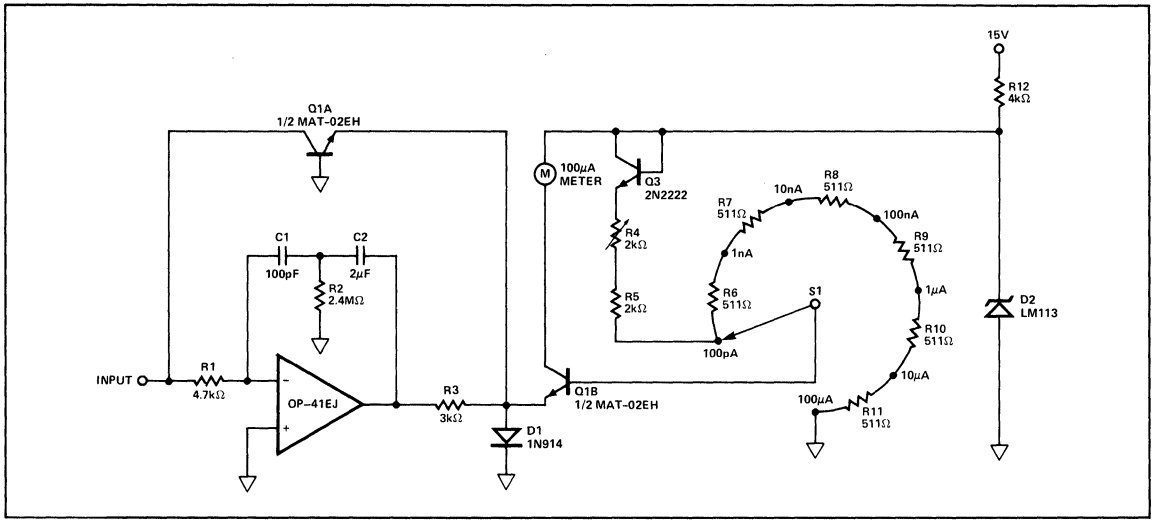
Triangular waveshapes of ±10V from 100Hz to 500kHz are obtained with values of R1 from 15MΩ to 3kΩ as given by:

$$R1 = \frac{V_S}{4V_P \cdot f_O \cdot C1}, \; V_S = 6.2V, \; V_P = 10V$$

The amplitude of the triangle wave may be adjusted via R2 as:

$$R2 = \frac{V_P \cdot 110k\Omega}{6.2V}$$

FIGURE 9: Wide Range, Low Current Ammeter

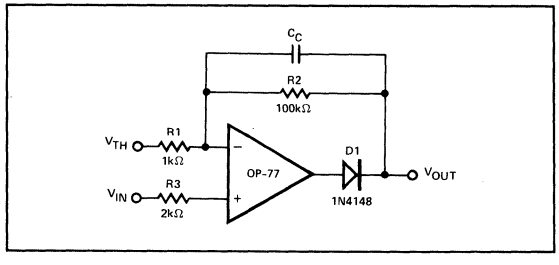


This ammeter can measure currents from 100pA to 100μA without the use of high value resistors. Accuracy is better than 1% over most of the range, depending upon the accuracy of the divider resistor and the input bias current of the op amp. Using the OP-41 as the input amplifier allows low end measurement down to a few pA due to the 5pA input bias current. Because the voltage across the inputs of the inverting amplifier is forced to virtually zero, the current meter's effective series voltage drop is less than 500μV at any current level.

Calibration is simple, requiring only one adjustment. R4 is used to adjust full scale deflection with a 1μA input current. This will give maximum accuracy over the operating range of currents.

The low V_{OS} and exceptionally good log conformance of the MAT-02 assure high accuracy over the full 6 decade operating range.

FIGURE 10: Precision Threshold Detector/Amplifier



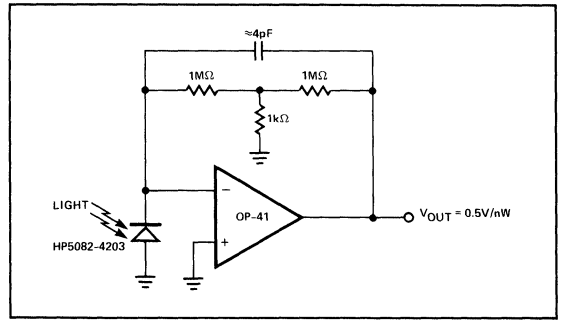
When $V_{IN} < V_{TH}$, the amplifier output swings negative, reverse biasing diode D1. Therefore $V_{OUT} = V_{TH}$.

When $V_{IN} \geq V_{TH}$, the loop closes, and

$$V_{OUT} = V_{TH} + (V_{IN} - V_{TH})\left(1 + \frac{R2}{R1}\right)$$

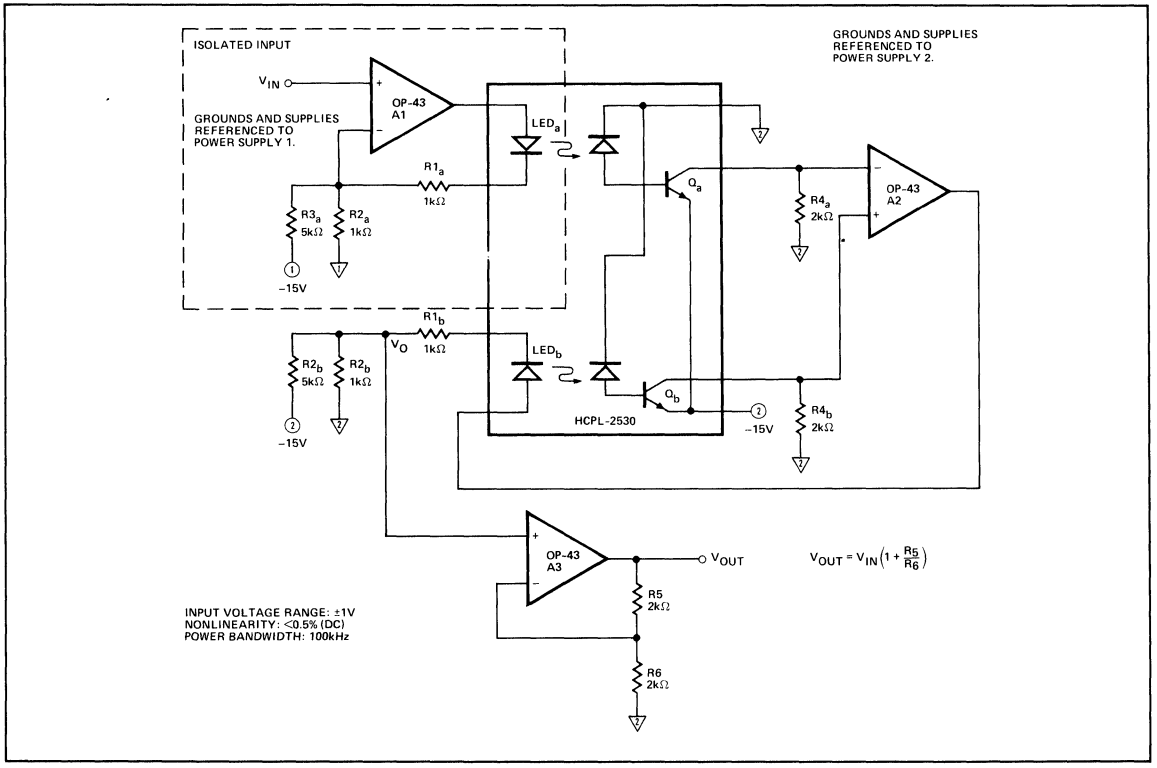
C_C is selected to smooth the loop response.

FIGURE 11: Wide-Dynamic-Range Light Detector



This circuit produces an output voltage proportional to light input over a 60dB range. The 5pA input bias current of the OP-41 assures a low output voltage offset.

FIGURE 12: Isolation Amplifier



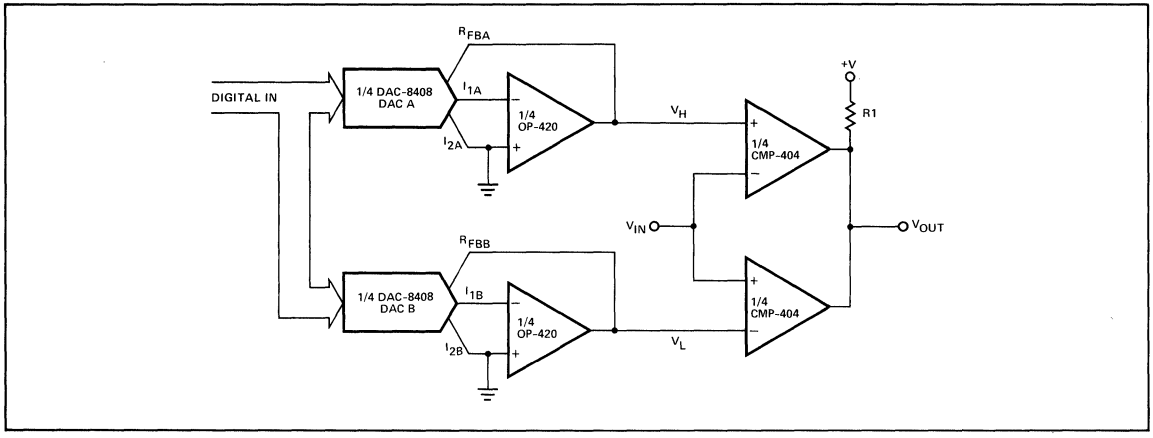
In conjunction with two optocouplers, or a dual optocoupler such as the Hewlett-Packard HCPL-2530, three OP-43's can be combined to create an isolation amplifier. In this sort of amplifier, the input and the output operate on separate power supplies, allowing extremely high common-mode voltages to be dealt with. In industrial applications, an isolation amplifier protects instrumentation from high voltages at the sensing site. When interfacing with a computing system, an isolation amplifier will protect the rest of the system from a sensor which accidentally becomes shorted to a high voltage.

The isolation amplifier operates on the principle that the nonlinearities of one optocoupler will be tracked by the nonlinearities of another, if they are well matched. By using an optocoupler in the feedback loop of A2, nonlinearities of the isolating optocoupler will be cancelled. V_O will equal V_{IN} plus an offset created by imperfect matching between a and b side resistors and optocouplers.

A3 is an output buffer for the isolation amplifier. The low bias current ensures that it does not affect the voltage it is amplifying. Gain is realized in this stage, and any offsets induced in the previous stages may be corrected by offsetting this op amp. Although shown in the circuit as a simple gain stage, this output amplifier may take any form desired. It may be configured as a filter or other waveshaping circuit as needed. The only requirement is that the buffer not disturb the currents in the optocoupler feedback circuit, thus noninverting amplifier configurations are preferred. For highest linearity, the currents in the two LEDs should track as closely as possible.

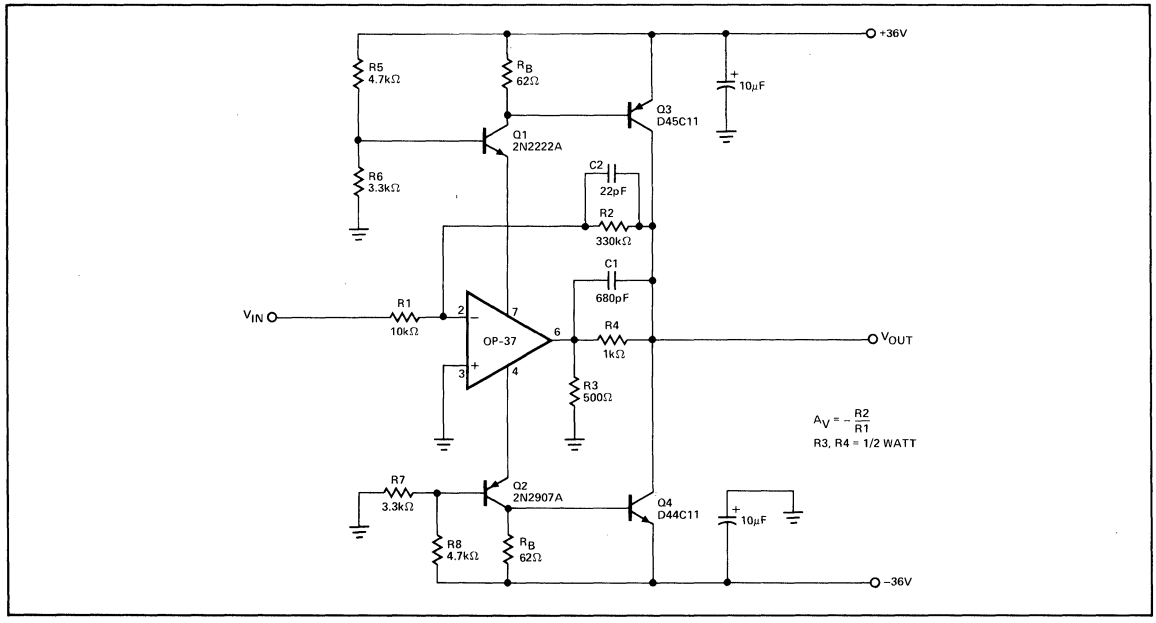
With stable supplies, the circuit has excellent reponse and displays less than 0.5% DC nonlinearity with a $2V_{p-p}$ signal. The high speed of the OP-43 gives the circuit a power bandwidth of 100kHz, while the majority of the power budget is consumed in biasing the LEDs. The dual optocoupler provides isolation against 600VDC common-mode voltages. Higher isolations may be achieved using two separate optocouplers, such as HP's 6N136.

FIGURE 13: Dual Programmable Window Comparator



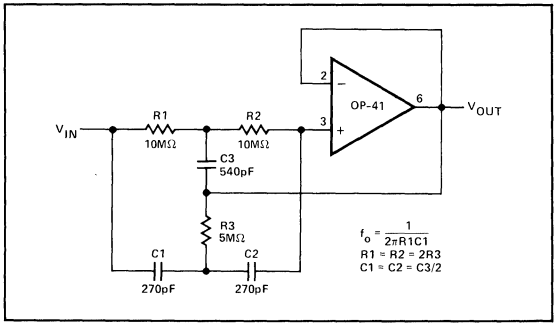
Only three ICs are required to fully implement two independent programmable window comparators. The quad, latched, 8-bit CMOS DAC-8408 together with the quad micropower OP-420 provide digitally-programmable HIGH and LOW thresholds to the CMP-404, quad low-power comparator. The outputs of the threshold comparators are wire-ORed with a common pull-up resistor producing $V_{OUT} = +V$ only when $V_L < V_{IN} < V_H$. Total supply current for the full circuit is less than 2mA.

FIGURE 14: ±36V Low Noise Operational Amplifier



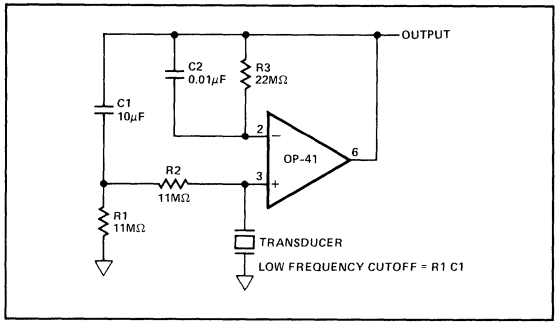
An OP-37 provides a low-noise front end for this amplifier which is capable of delivering over ±200mA to a load with a 70V peak-to-peak output swing. Transistors Q1 and Q2 are series regulators stepping down the supply voltage for the OP-37 to ±15V, while transistors Q3 and Q4 provide the high current output drive. R3 and R4 form an output voltage gain stage whose gain, $A_V = 3$, is reduced to unity at high frequencies by C1 to maintain stability.

FIGURE 15: High Q Notch Filter



The low bias current and high input impedance of the OP-41 enable small value capacitors and large resistors to be used in this 60Hz notch filter. The 5pA bias current only develops 100μV across R1 and R2.

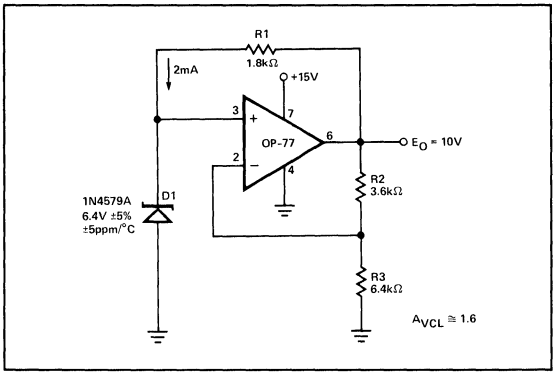
FIGURE 16: Piezoelectric Transducer Amplifier



Piezoelectric transducers often require a high-input-resistance amplifier. The OP-41 can provide input resistance in the range of $10^{12}\Omega$, however, a DC return for bias current is needed. To maintain a high R_{IN}, large value resistors above 22MΩ are often required. These may not be practicable.

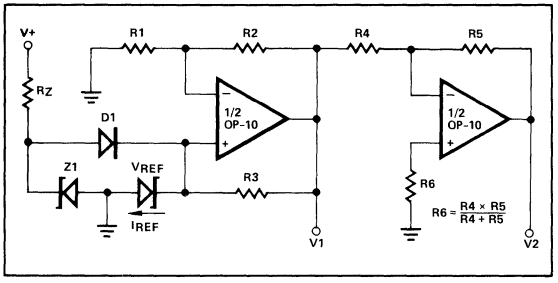
Using this circuit, input resistances that are orders of magnitude greater than the values of the DC return resistors can be obtained. This is accomplished by bootstrapping the resistors to the output. With this arrangement, the lower cutoff frequency is determined more by the RC product of R1 and C1 that it is by resistor values and the equivalent capacitance of the transducer.

FIGURE 17: High Stability Voltage Reference



The simple bootstrapped voltage reference provides a precise 10V virtually independent of changes in power supply voltage, ambient temperature, and output loading. Correct zener operating current of exactly 2mA is maintained by R1, a selected 5ppm/°C resistor, connected to the regulated output. Accuracy is primarily determined by three factors: the 5ppm/°C temperature coefficient of D1, 1ppm/°C ratio tracking of R2 and R3, and operational amplifier V_{OS} errors. The OP-77, with TCV_{OS} of 0.3μV/°C, contributes only 0.05ppm/°C of output error, thus effectively eliminating TCV_{OS} as an error consideration.

FIGURE 18. Precision Dual Tracking Voltage References



Precision dual tracking voltage references using a single reference source are easily constructed using OP-10. These references exhibit excellent stability vs. temperature/time, low noise, and excellent power supply rejection.

In the circuit shown, R3 should be adjusted to set I_{REF} to operate V_{REF} at its minimum temperature coefficient current. Proper circuit start-up is assured by R_Z, Z1, and D1.

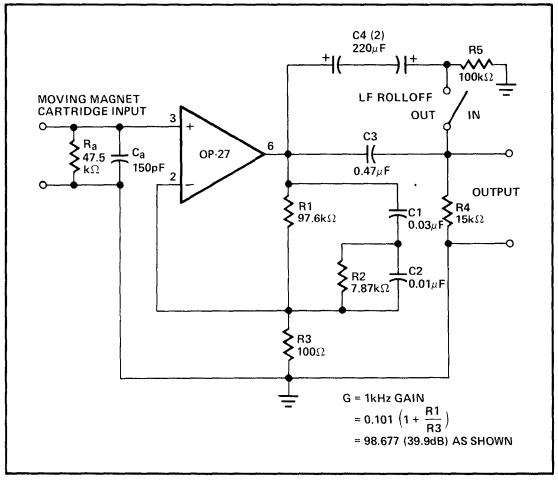
$$V_{Z1} \leq V_{REF} \qquad V1 = V_{REF}\left(1 + \frac{R2}{R1}\right)$$

$$R3 = \frac{(V1 - V_{REF})}{I_{REF}} \qquad V2 = V1\left(\frac{-R5}{R4}\right)$$

Output Impedance (ΔI_L:1.0mA—5.0mA) ..... $0.25 \times 10^{-3}\Omega$

AN-106

FIGURE 19: RIAA Phone Pre-Amplifier



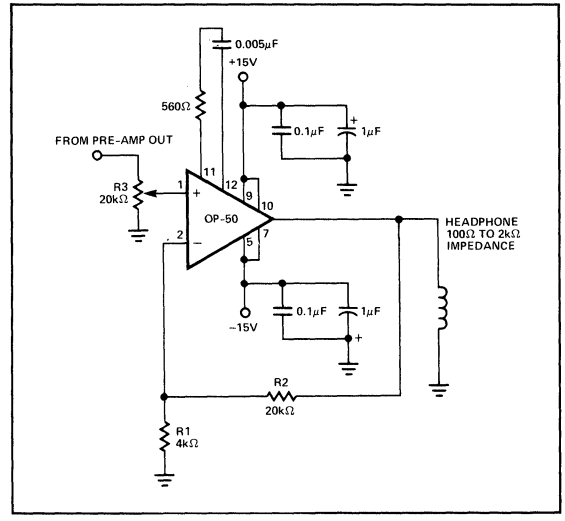
The OP-27 is used in this phono pre-amplifier circuit because of its low noise characteristics. It contributes only $3.2nV/\sqrt{Hz}$ voltage noise and $0.45pA/\sqrt{Hz}$ current noise to the circuit. To minimize noise from other sources, R3 is set to 100Ω. This generates additional voltage noise of only $1.3nV/\sqrt{Hz}$. With a 1kΩ source, the circuit noise measures 63dB below a 1mV reference level, unweighted, in a 20kHz bandwidth.

R1, R2, C1, and C2 form a very accurate RIAA network with standard component values providing the necessary time constants of 3180, 318, and 75μsec. For initial equalization accuracy and stability, precision metal-film resistors and film capacitors of polystyrene or polypropylene are recommended since they have low voltage coefficients, dissipation factors, and dielectric absorption. (High-K ceramic capacitors should be avoided here, though low-K ceramics—such as NPO types, which have excellent dissipation factors, and somewhat lower dielectric absorption—can be considered for small values.)

Capacitor C3 and resistor R4 form a simple −6dB-per-octave rumble filter, with a corner at 22Hz. As an option, the switch-selected shunt capacitor C4, a nonpolarized electrolytic, bypasses the low-frequency rolloff. Placing the rumble filter's high-pass action after the pre-amp has the desirable result of discriminating against the RIAA-amplified low-frequency noise components and pickup-produced low-frequency disturbances.

This circuit is capable of very low distortion over its entire range, generally below 0.01% at levels up to 7Vrms. At 3V output levels, it will produce less than 0.03% total harmonic distortion at frequencies up to 20kHz.

FIGURE 20: Headphone Amplifier



For low level Pre-Amp Out signals, the amplifier gain may be increased by reducing R1 according to:

$$R1 = \frac{20k\Omega}{A_V - 1}$$

Note that two amplifiers are required for stereo applications.

Performance: ($V_{OUT} = 6V_{RMS}$, R1 = 4kΩ)

T.H.D @ 100Hz = 0.0025%

@ 1kHz = 0.003%

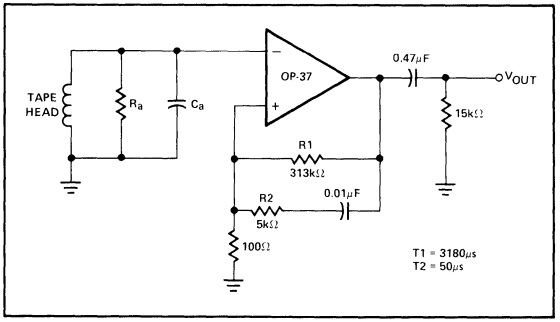
@ 10kHz = 0.011%

Signal-to-Noise Ratio ≥ 80dB

Response Flatness = ±0.4dB from 10Hz to 20kHz

Bandwidth = −3dB @ 56kHz

FIGURE 21: NAB Tape Head Pre-Amplifier



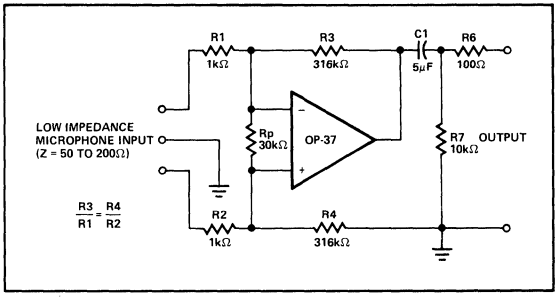
A pre-amplifier for NAB tape playback is similar to an RIAA phono pre-amp, though more gain is typically demanded, along with equalization requiring a heavy low-frequency boost.

The network values of this configuration yield a 50dB gain at 1kHz, and a DC gain greater than 70dB. Thus, the worst-case output offset is just over 500mV. The DC resistance of the tape head will add to this a bias-current-induced offset voltage. To minimize this contribution, the head's DC resistance should be low, preferably below 1kΩ. A single 0.47μF output capacitor can block the final output offset without affecting the dynamic range.

The tape head can be coupled directly to the amplifier input, since the worst-case bias current of 80nA with a 400mH, 100μin. head (such as the PRB2H7K) will not be troublesome.

One potential tape head problem is presented by amplifier bias current transients at power-up or power-down which can magnetize a head. Although the OP-37 is free of these bias current transients, it is always good design practice to control the speed of power supply rise and fall to eliminate transients.

FIGURE 22: Microphone Pre-Amplifier

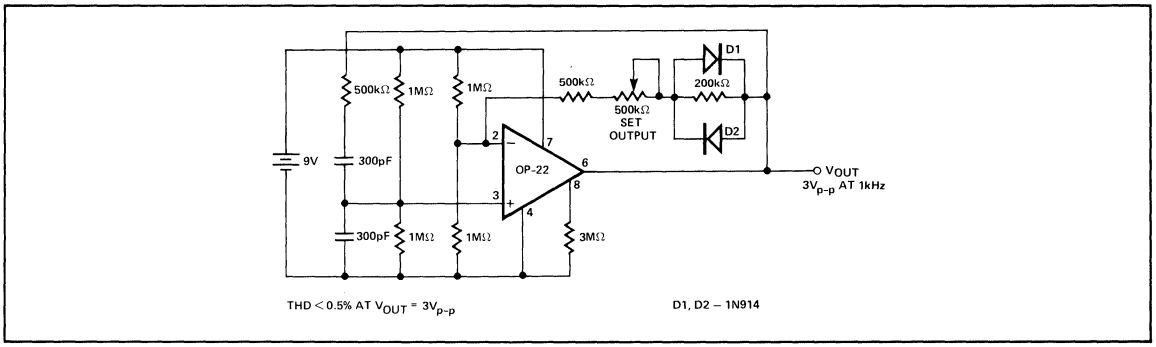


This simple, but effective, fixed-gain transformerless microphone pre-amp amplifies differential signals from low-impedance microphones by 50dB, and has an input impedance of 2kΩ. Because of the high working gain of the circuit, an OP-37 helps to preserve bandwidth, which will be 110kHz. As the OP-37 is a decompensated device (minimum stable gain of 5), a dummy resistor, R_p, may be necessary, if the microphone is to be unplugged. Otherwise the 100% feedback from the open input may cause the amplifier to oscillate.

Common-mode input-noise rejection will depend upon the match of the bridge-resistor ratios. Either close-tolerance (0.1%) types should be used, or R4 should be trimmed for best CMRR. All resistors should be metal-film types for best stability and low noise.

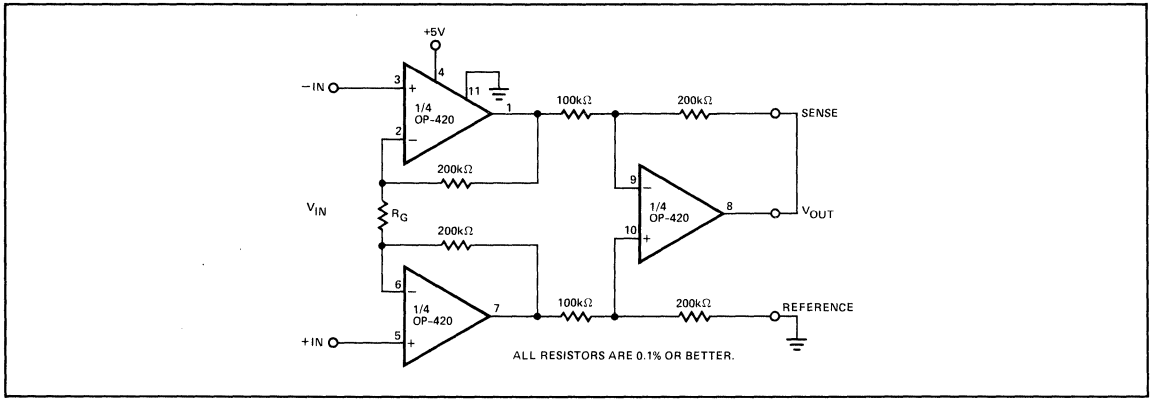
Noise performance of this circuit is limited more by the input resistors R1 and R2 than by the op amp, as R1 and R2 each generate a $4nV/\sqrt{Hz}$ noise, while the op amp generates a $3.2nV/\sqrt{Hz}$ noise. The rms sum of these predominant noise sources will be about $6nV/\sqrt{Hz}$, equivalent to 0.9μV in a 20kHz noise bandwidth, or nearly 61dB below a 1mV input signal. Measurements confirm this predicted performance.

FIGURE 23: Micropower Wien-Bridge Oscillator ($P_d < 500\mu W$)



Requiring less than 60μA of supply current, this micropower Wien-bridge oscillator is ideal for battery-powered instrumentation. Output level is controlled by nonlinear elements D1 and D2. When adjusted for $3V_{p-p}$ output, the distortion level is below 0.5% at 1kHz.

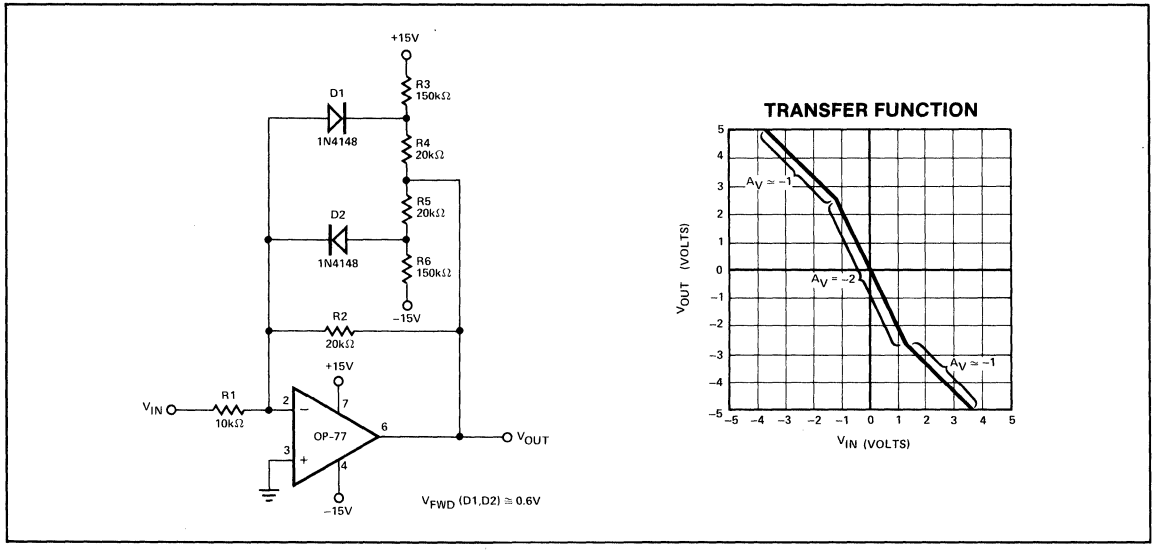
FIGURE 24: Micropower Instrumentation Amplifier



This instrumentation amplifier requires only 200μA total quiescent current (V_{CM} = 0V) and operates on single voltage supplies from +1.6V to +36V. Input and output voltage range is 0V to (V^+ − 1.5) volts with CMRR above 100dB. Differential gain, A_V, is adjusted with a single resistor, R_G, as given by:

$$R_G = \frac{800k\Omega}{A_V - 2}$$

FIGURE 25: Piecewise-Linear Amplifier (Decreasing Gain)



This circuit is useful in linearizing a nonlinear input signal or creating a nonlinear output function from a linear input. At V_{OUT} = 0V, both D1 and D2 are reverse biased, and V_{OUT}/V_{IN} = −R2/R1. As V_{IN} goes positive, V_{OUT} becomes negative according to that gain until a threshold is reached, $-(V_{OUT} + V_{FWD})/R4 = 15V/R3$, where D1 becomes forward biased. For more positive values of V_{IN}, the gain is:

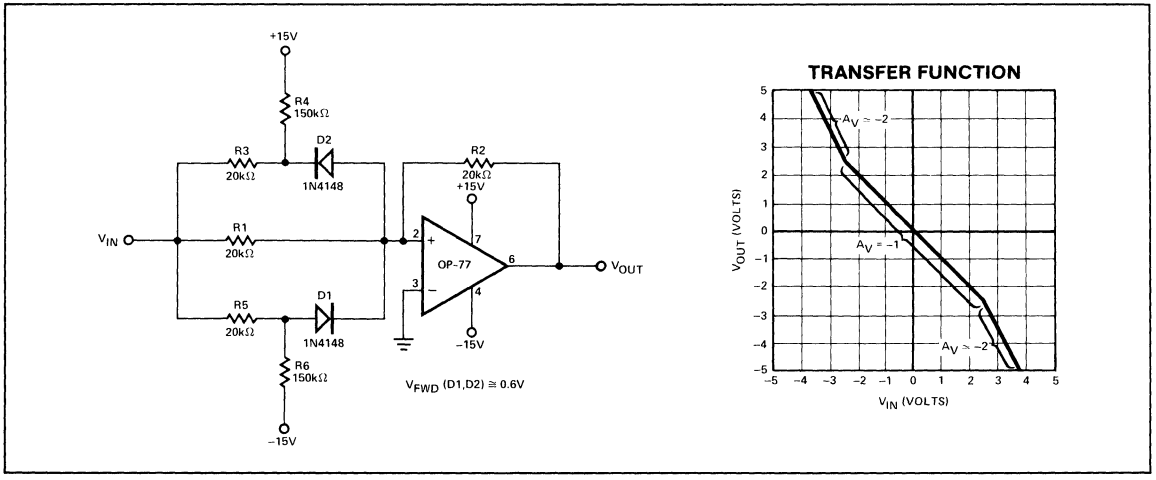
$$\frac{V_{OUT}}{V_{IN}} = -\frac{(R2 \cdot R4)}{(R2 + R4)R1} - \frac{R2 \cdot V_{FWD}}{(R2 + R5)V_{IN}}$$

A similar action occurs as V_{IN} goes negative. Beyond the point where D2 becomes forward biased, $(V_{OUT} - V_{FWD})/R5 = 15V/R6$, the gain is:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{(R2 \cdot R5)}{(R2 + R5)R1} - \frac{R2 \cdot V_{FWD}}{(R2 + R5)V_{IN}}$$

Additional diode/resistor combinations can be added to further contour the gain.

FIGURE 26: Piecewise-Linear Amplifier (Increasing Gain)



This circuit performs the linear-to-nonlinear or nonlinear-to-linear transformation by increasing gain beyond fixed thresholds. At $V_{IN} = 0V$, both D1 and D2 are reverse biased, and $V_{OUT}/V_{IN} = -R2/R1$. As V_{IN} goes positive beyond the threshold, $(V_{IN} - V_{FWD})/R5 = 15V/R6$, D1 conducts, and the gain becomes:

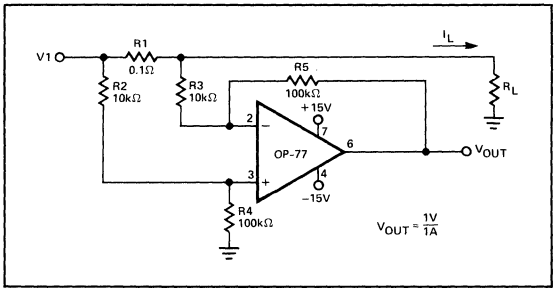
$$\frac{V_{OUT}}{V_{IN}} = -\frac{R2(R1 + R5)}{(R1 \cdot R5)} + \frac{V_{FWD} \cdot R2}{V_{IN} \cdot R5}$$

As V_{IN} goes negative beyond the threshold, $-(V_{IN} + V_{FWD})/R3 = 15V/R4$, D2 conducts, and the gain becomes:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R2(R1 + R3)}{(R1 \cdot R3)} + \frac{V_{FWD} \cdot R2}{V_{IN} \cdot R3}$$

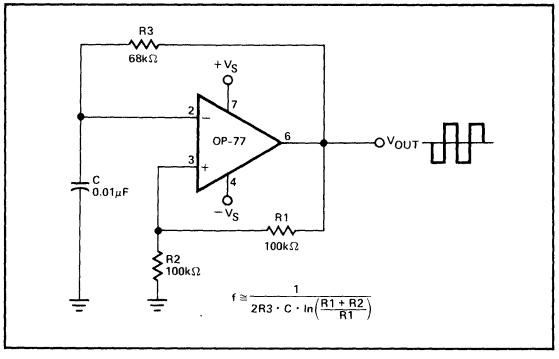
Additional diode/resistor combinations can be added to further contour the gain.

FIGURE 27: Current Monitor Circuit



This versatile monitor circuit can typically sense current at any point between the ±15V supplies ($|V1| < 14.3V$ guaranteed). This makes it ideal for sensing current in applications such as full bridge drivers where bi-directional current is associated with large common-mode voltage changes. The 120db CMRR of the OP-77 makes the amplifier's contribution to common-mode error negligible, leaving only the error due to the resistor ratio inequality. Ideally, R2/R4 = R3/R5. This is best trimmed via R4.

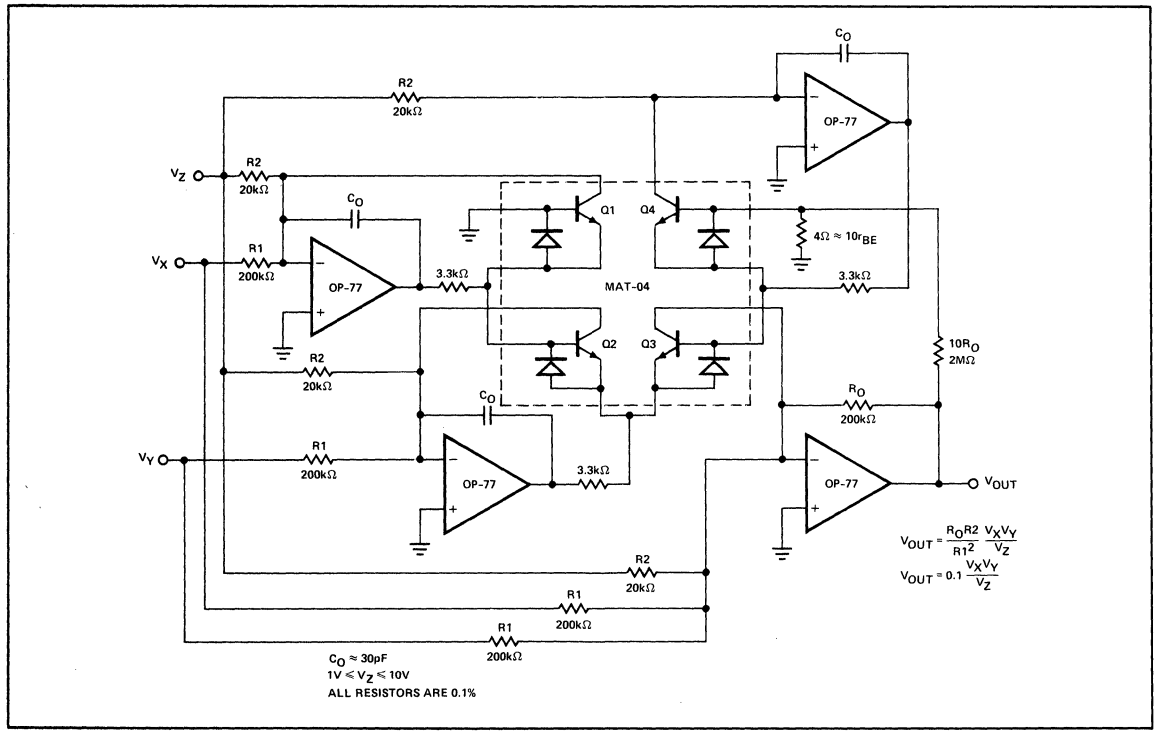
FIGURE 28: Free-Running Square-Wave Oscillator



This simple oscillator creates a square-wave output of ±(V_S − 2V) at 1kHz for the values shown.

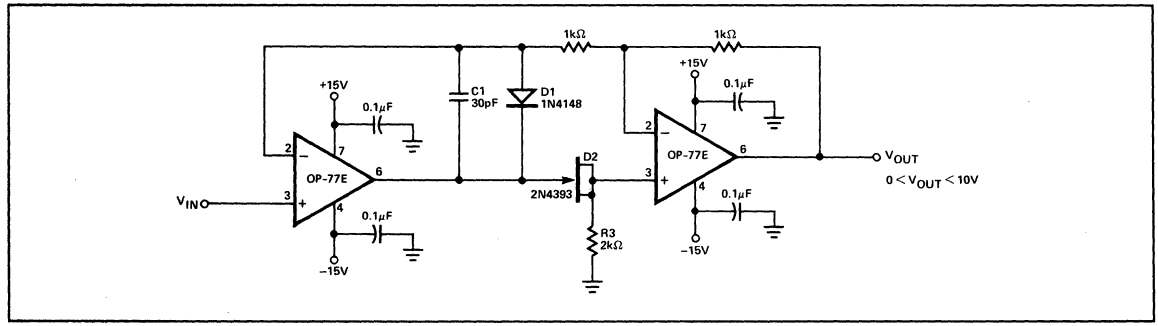
AN-106

FIGURE 29: Precision Analog Multiplier/Divider



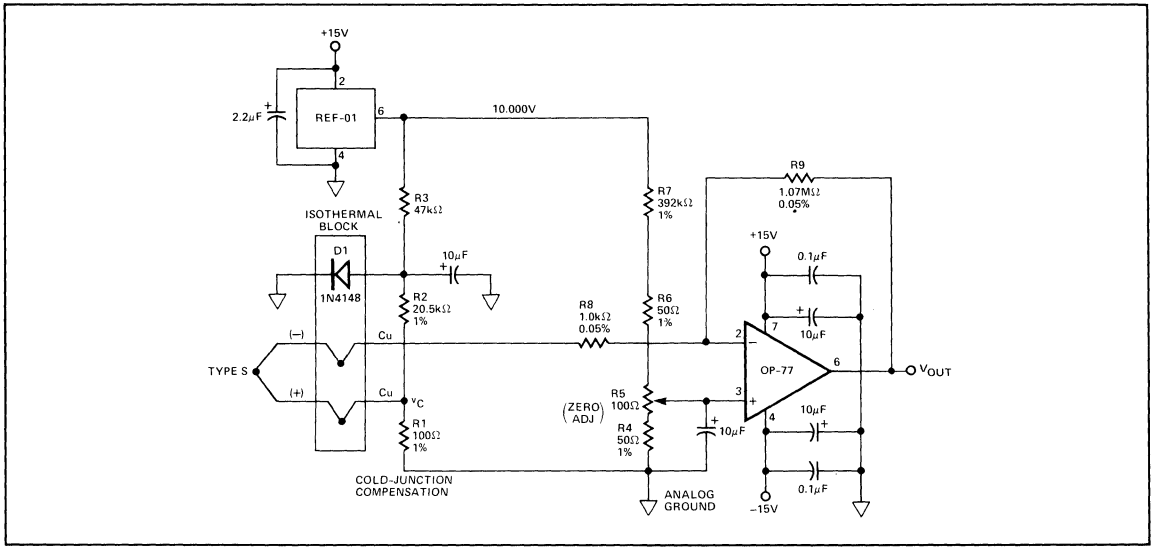
This multiplier/divider achieves its excellent performance through the low emitter resistance, r_{BE}, and superior V_{OS} matching of MAT-04 quad transistor array. In this circuit, linearity error due the transistors is less than ±0.1%. The OP-77 helps maintain accuracy with a V_{OS} less than 25μV. For even higher accuracy the offset voltages may be nulled.

FIGURE 30: Precision Absolute Value Amplifier



The high gain and low TCV_{OS} assure accurate operation with inputs from microvolts to volts. In this circuit, the signal always appears as a common-mode signal to the op amps. The OP-77E CMRR of 1μV/V assures errors of less than 2ppm.

FIGURE 31: Thermocouple Amplifier With Cold-Junction Compensation



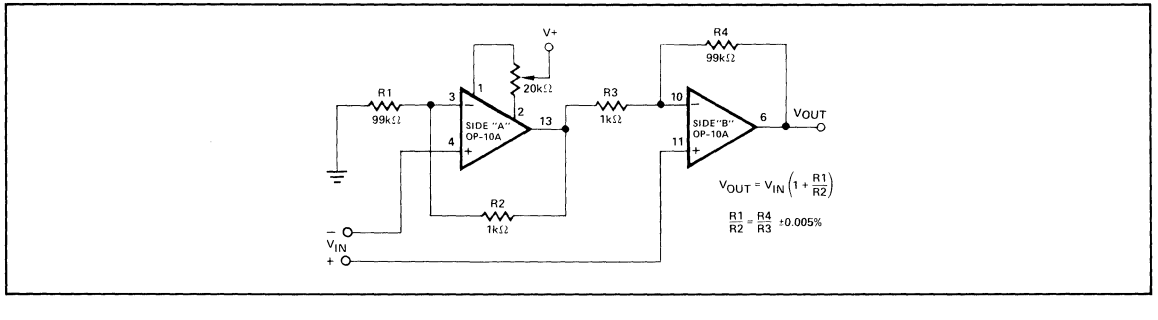
The high gain, low noise, and low offset drift of the OP-77 can be used to create a thermocouple amplifier with superb linearity. They combine to give a total accuracy typically better than ±0.5°C.

Cold-junction compensation is performed by R1, R2, and D1 which is mounted isothermally with the thermocouple terminating junctions. Calibration is done using R5 after the circuit has stabilized for about 15 minutes. A copper wire short is applied across the terminating junctions simulating a zero °C ice point. R5 is then adjusted for 0.000V output. The short is then removed, and the amplifier is ready for use.

This amplifier can be used for type S, J, and K thermocouples with the appropriate resistor values as shown below. R9 is chosen to give a +10.000V output for a 1,000°C measurement.

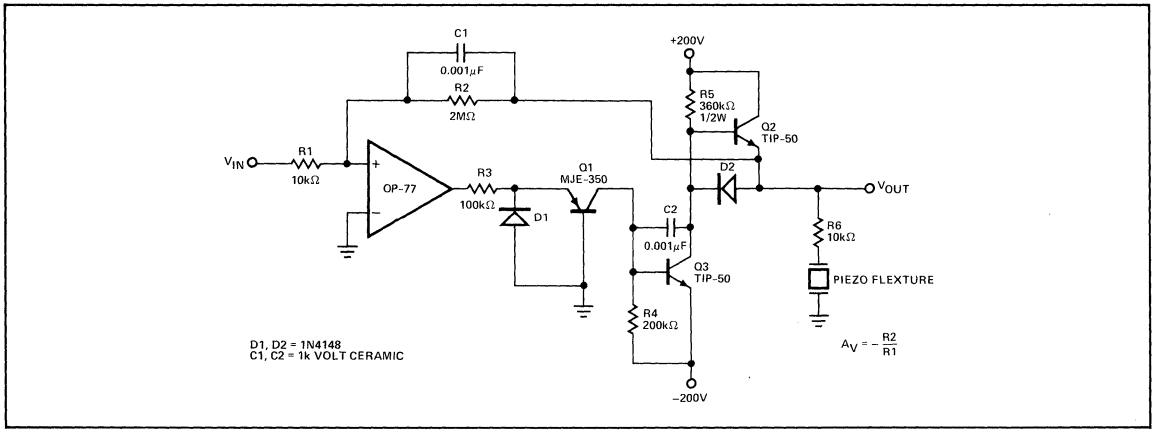
TYPE	SEEBECK COEFFICIENT, α	R1	R2	R7	R9
K	39.2μV/°C	110Ω	5.76kΩ	102kΩ	269kΩ
J	50.2μV/°C	100Ω	4.02kΩ	80.6kΩ	200kΩ
S	10.3μV/°C	100Ω	20.5kΩ	392kΩ	1.07MΩ

FIGURE 32: Instrumentation Amplifier (2 Op Amp Design)



This differential amplifier offers high input impedance and a power supply rejection ratio greater than 100dB. Because the high circuit gain occurs in Side "B"; Side "A" offset should be adjusted with respect to V_{OUT}. This simultaneously corrects for Side "B" offset voltage. For the circuit values given, $A_V = 100$.

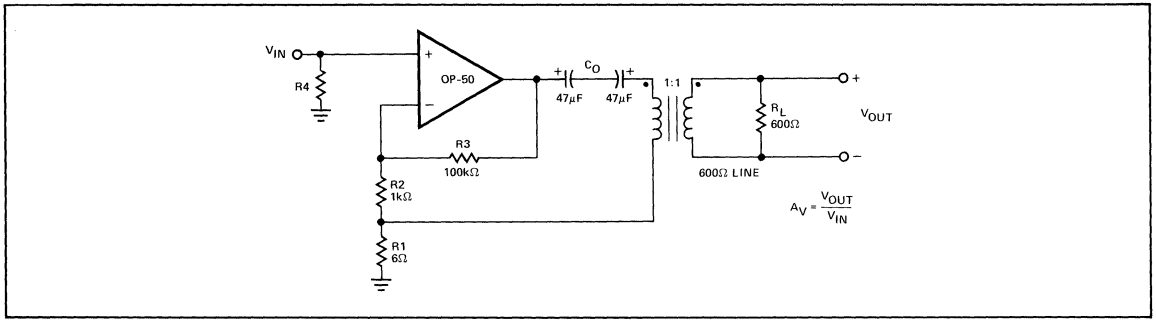
FIGURE 33: ±200V Low Offset Operational Amplifier



The OP-77 is the heart of this high voltage amplifier designed to drive piezo flexture elements in precise positioning applications. The high gain and low offset voltage of the OP-77 produce an accurate, stable drive voltage to the piezo device allowing predictable, repeatable sub-micron movements to be easily controlled.

The output of the OP-77 creates a proportional current drive through the common-base connected Q1 to the base of Q3. Q3 forms a Class A amplifier with bias resistor R5, and transistor Q2 is simply an emitter-follower used for output current boost. R6 is necessary to prevent oscillation caused by the capacitive loading of the piezo device on the output of the amplifier.

FIGURE 34: Impedance Transforming Amplifier



This is an efficient, flexible circuit simulating a source impedance equal to the load impedance. By definition, if $R_S = R_L$, then,

$$A_V = \frac{A_{V(UNLOADED)}}{2}$$

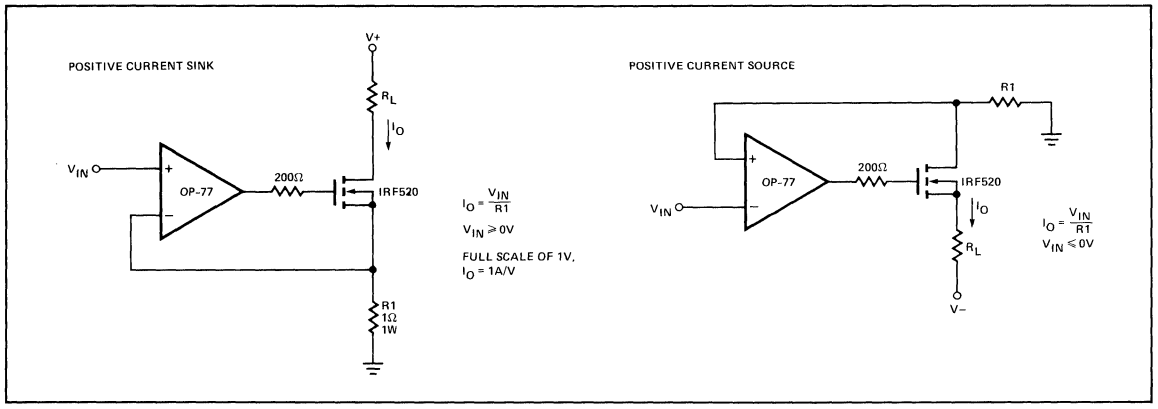
The unloaded gain is roughly R3/R2. When the output is loaded, a second feedback loop is closed whose gain, $A_V \simeq R_L/R1$, combines in parallel with $A_{V(UNLOADED)}$ to give:

$$A_{V(LOADED)} = \frac{A_{V(UNLOADED)} \cdot A_V}{A_{V(UNLOADED)} + A_V}$$

If R3/R2 = R_L/R1, then $A_{V(LOADED)} = \frac{A_{V(UNLOADED)}}{2}$

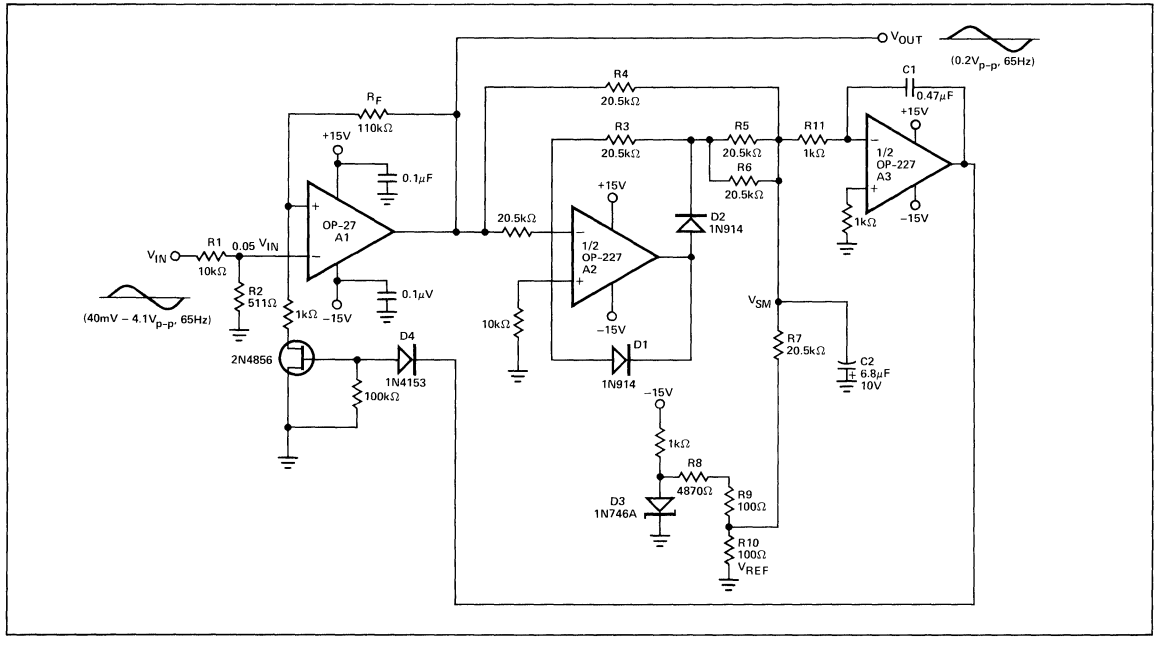
These approximations assume that R1 ≪ R2 and R2 ≪ R3. The OP-50 requires no compensation for the circuit values shown and can easily drive the 600Ω line.

FIGURE 35: Precision Current Sinks



These simple high-current sinks require that the load float between the power supply and the sink. In these circuits, OP-77's high gain, high CMRR, and low TCV_{OS} assure high accuracy.

FIGURE 36: Low Noise AGC Amplifier

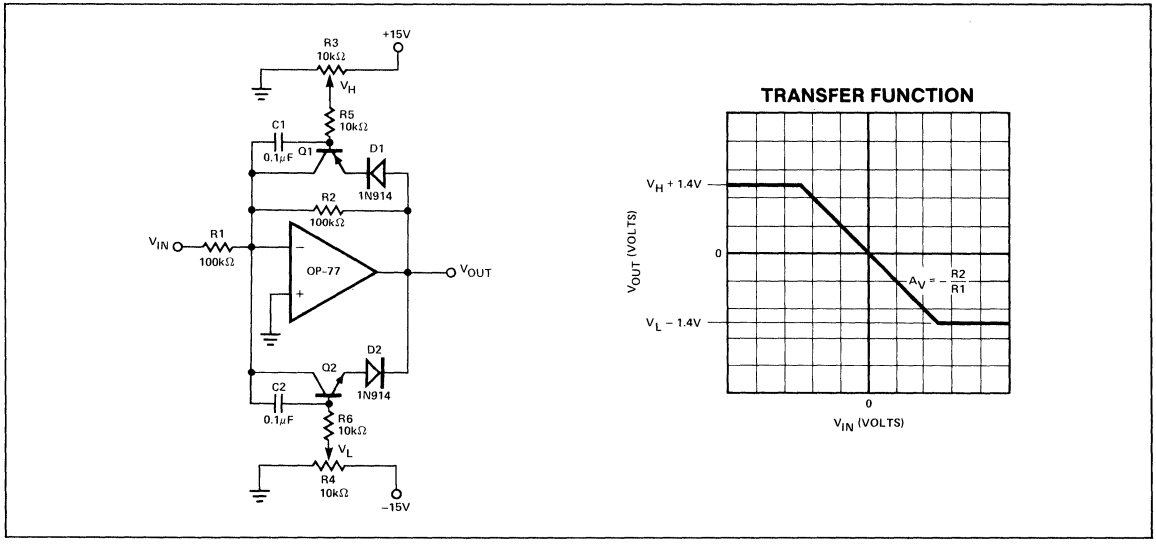


In this circuit, a JFET transistor is used to control the gain of the low-noise OP-27 amplifier over a two-decade input voltage range. For inputs from 40mV to 4.1V peak-to-peak, the AGC maintains a 0.2V peak-to-peak output.

Amplifier A2 performs an absolute-value operation on V_{OUT} and sums the result with a −0.2V reference on capaciator C2. The deviation of this sum, V_{SM}, from zero is amplified by A3 and controls the gate of the JFET. If the peak-to-peak amplitude of V_{OUT} exceeds 0.2V, V_{SM} becomes positive and drives the JFET gate negative. This increases the JFET's channel resistance lowering the gain of the A1. The reverse of this occurs if V_{OUT} falls below 0.2V peak-to-peak.

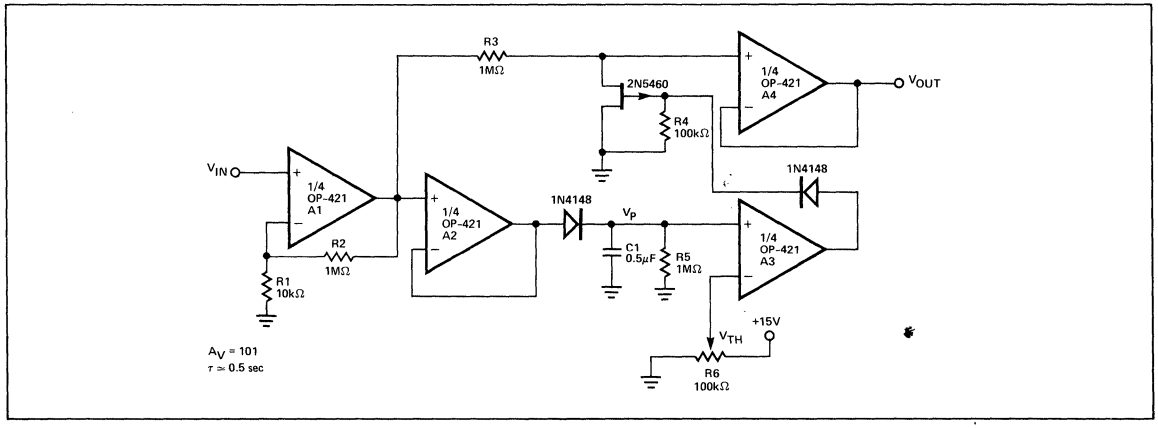
The values of C1 and C2 are chosen to optimize the circuits response time for a given input voltage frequency. This example was designed for a 65Hz signal. Higher frequencies would justify lower values for C1 and C2 to speed the AGC response.

FIGURE 37: Amplifier with Active Output Clipping



This configuration allows adjustment of the op amp's maximum output voltage. Below the clipping levels, circuit gain is $A_V = -R2/R1$. As V_{OUT} rises above ($V_H + 1.4V$), the base/emitter of Q1 becomes forward biased, allowing collector current to flow to the summing node, thus clamping V_{OUT}. A similar action occurs as V_{OUT} goes below ($V_L - 1.4V$) and is clamped by Q2.

FIGURE 38: Low Power Amplifier With Squelch



The OP-421 is the heart of this variable squelch amplifier which requires less than 2mA of supply current ($R_L = \infty$). A1 provides a high impedance input amplifier with $A_V = 1 + R2/R1$. Its output drives a unity gain output buffer, A4, and a peak detector with a time constant set by C1 and R5. When the output of the peak detector, V_P, exceeds the adjustable threshold, V_{TH}, the comparator, A3, drives the gate of the P-channel FET high, turning it OFF. At lower input signal levels, V_P falls below V_{TH}, and the FET turns ON, clamping the input of A4 to ground.

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