FireLink USB

82C862/82C863
Dual Controller
PCI-USB Host Bridge

Data Book

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Revision 1.1
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1.0 Features

The OPTi 82C862 and 82C863 FireLink USB devices are high performance USB host controllers. Both products share the same dual transfer engine design, the only difference being that the 82C862 product implements four USB ports, while the 82C863 product implements two ports.

Their shared feature set is as follows.

- Compliant with USB rev. 1.1 specification
- Compliant with PCI rev 2.2 specification
- Implements complete USB Open Host Controller Interface (OHCI) specification
- Two independent host controllers (implemented as a multi-function PCI device)
- Two USB ports (82C862) or one USB port (82C863) per controller
- Second host controller can be disabled if not used to save power
- Clock input can be derived from either a 12MHz crystal or a 48MHz oscillator
- Clocks can be turned off when not in use to save power
- Core operates at 3.3V; PCI inputs are 5V-tolerant
- Incorporates PCI Power Management, supporting very low power standby modes
- Implements CLKRUN# pin to support hardware-enforced power-down
- Packaged as 100-pin LQFP (Low-profile Quad Flat Pack)
- Supported by Windows 98, Windows Me, Windows 2000, Windows XP, Windows CE, Apple Mac OS, Linux

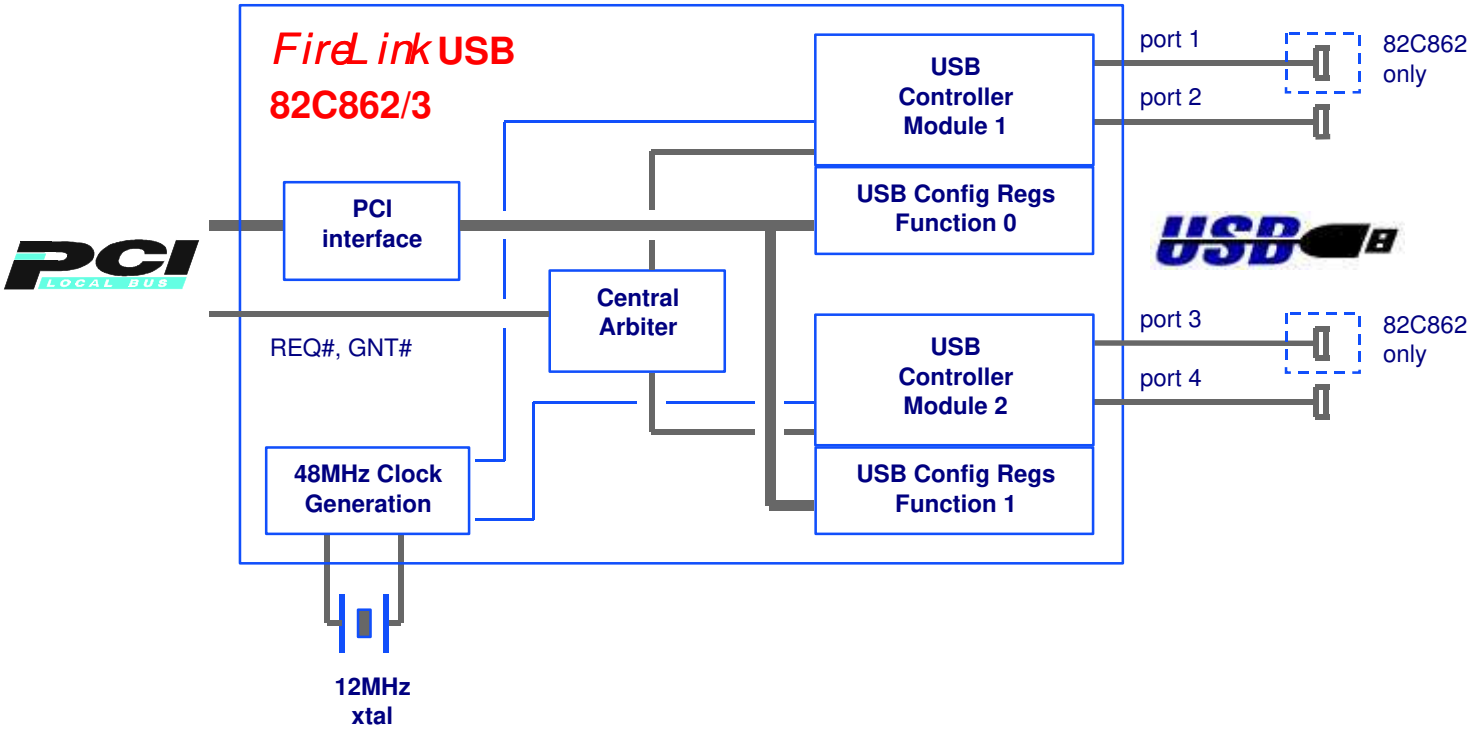
1.1 Overview

This document describes the OPTi FireLink USB 82C862/82C863 controller.

This PCI-to-USB bridge is unique in that it consists of two independent dual-port controllers, each sharing only the common PCI bus connection. This arrangement allows for a total Universal Serial Bus bandwidth of 24Mbps, divided into 12Mbps for each pair of ports (or 12Mbps per port in the case of the 82C863).

Figure 1 provides a block diagram of the overall functionality of the chip.

Figure 1. FireLink USB Block Diagram



2.0 Signal Definitions

2.1 Terminology/Nomenclature Conventions

The "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used extensively. This is done to avoid confusion when working with a mixture of active low and active high signals. The term assert, or assertion indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation indicates that a signal is inactive.

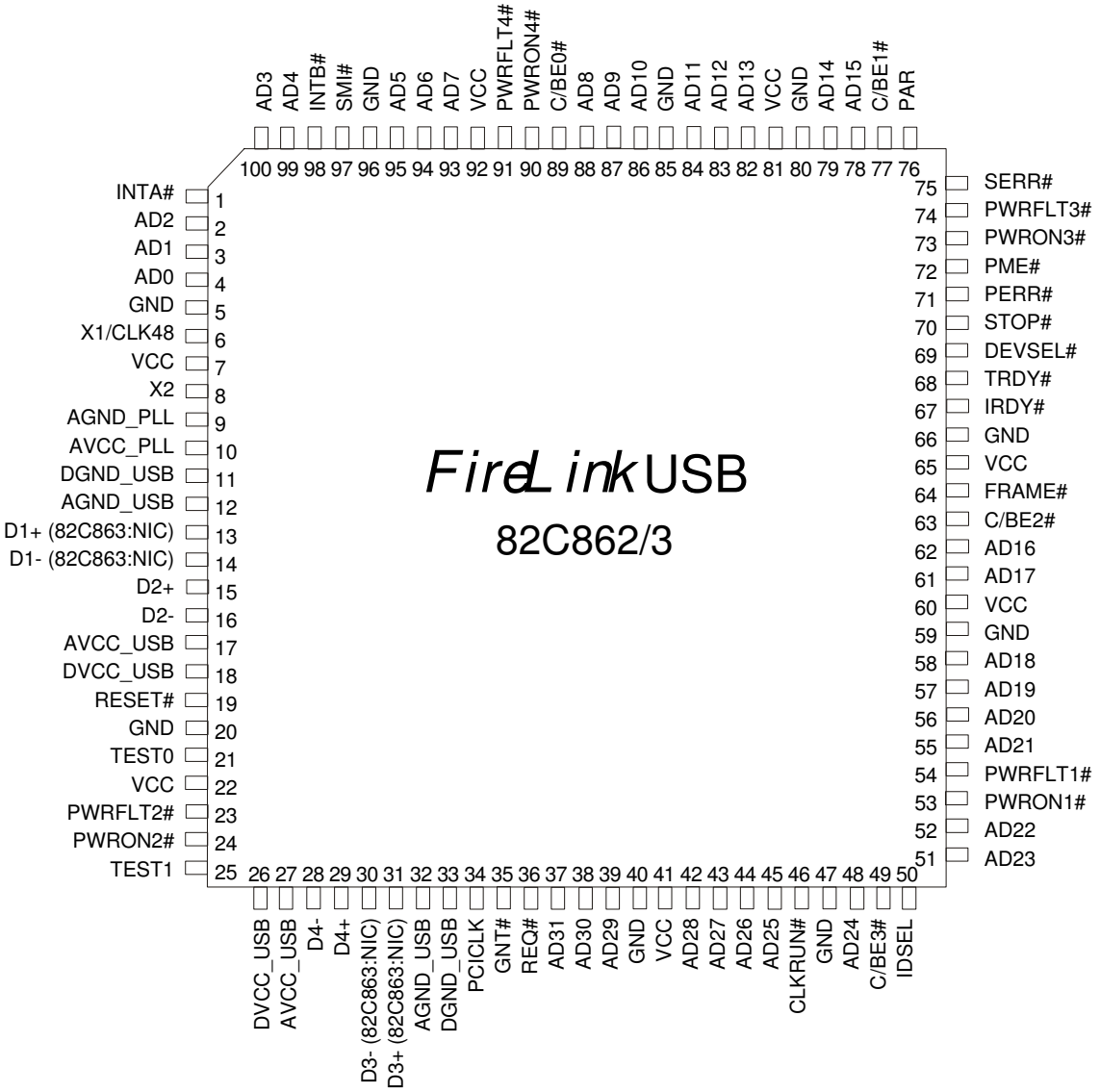
The tables in this section use several common abbreviations. Table 1 lists the mnemonics and their meanings. Note that TTL/CMOS/Schmitt-trigger levels pertain to inputs only. Outputs are driven at CMOS levels.

Table 1. Signal Definitions Legend

Mnemonic	Description
Analog	Analog-level compatible
CMOS	CMOS-level compatible
Dcdr	Decoder
Diff	Differential signal pair
Ext	External
G	Ground
I	Input
Int	Internal
I/O	Input/Output
Mux	Multiplexer
NIC	No Internal Connection
O	Output
OD	Open drain
P	Power
PD	Pull-down resistor
PU	Pull-up resistor
S	Schmitt-trigger
S/T/S	Sustain Tristate
TTL	TTL-level compatible

Figure 2. LQFP Pin Diagram (Note)

Note: Figure 2 shows a pin diagram of the 82C862/3 packaged in an LQFP (Low-profile Quad Flat Pack, square). Refer to the "Mechanical Package Outlines" section for details regarding packaging.



NOTE: NIC = No Internal Connection

2.2 Numerical Pin Cross-Reference List

Pin No.	Signal Name	Power Plane
1	INTA#	VCC
2	AD2	
3	AD1	
4	AD0	
5	GND	
6	X1/CLK48	
7	VCC	
8	X2	
9	AGND_PLL	AVCC_PLL
10	AVCC_PLL	
11	DGND_USB	DVCC_USB
12	AGND_USB	AVCC_USB
13	82C862: D1+ 82C863: NIC	
14	82C862: D1- 82C863: NIC	
15	D2+	
16	D2-	
17	AVCC_USB	
18	DVCC_USB	DVCC_USB
19	RESET#	VCC
20	GND	
21	TEST0	
22	VCC	
23	PWRFLT2	
24	PWRON2	
25	TEST1	
26	DVCC_USB	DVCC_USB
27	AVCC_USB	AVCC_USB
28	D4-	
29	D4+	
30	82C862: D3- 82C863: NIC	
31	82C862: D3+ 82C863: NIC	
32	AGND_USB	

Pin No.	Signal Name	Power Plane
33	DGND_USB	DVCC_USB
34	PCICLK	VCC
35	GNT#	
36	REQ#	
37	AD31	
38	AD30	
39	AD29	
40	GND	
41	VCC	
42	AD28	
43	AD27	
44	AD26	
45	AD25	
46	CLKRUN#	
47	GND	
48	AD24	
49	C/BE3#	
50	IDSEL	
51	AD23	
52	AD22	
53	PWRON1#	
54	PWRFLT1#	
55	AD21	
56	AD20	
57	AD19	
58	AD18	
59	GND	
60	VCC	
61	AD17	
62	AD16	
63	C/BE2#	
64	FRAME#	
65	VCC	
66	GND	

Pin No.	Signal Name	Power Plane
67	IRDY#	VCC
68	TRDY#	
69	DEVSEL#	
70	STOP#	
71	PERR#	
72	PME#	
73	PWRON3#	
74	PWRFLT3#	
75	SERR#	
76	PAR	
77	C/BE1#	
78	AD15	
79	AD14	
80	GND	
81	VCC	
82	AD13	
83	AD12	
84	AD11	
85	GND	
86	AD10	
87	AD9	
88	AD8	
89	C/BE0#	
90	PWRON4#	
91	PWRFLT4#	
92	VCC	
93	AD7	
94	AD6	
95	AD5	
96	GND	
97	SMI#	
98	INTB#	
99	AD4	
100	AD3	

2.3 Signal Descriptions

2.3.1 Clock and Reset Interface Signals

Signal Name	Pin No.	Pin Type	Signal Description
PCICLK	34	I	**PCI Clock:** This input provides timing for all cycles on the host PCI bus; normally 33MHz. All other PCI signals are sampled on the rising edge of PCLK (timing parameters refer to this edge).
X1/CLK48 X2	6 8	I O	**USB Clock:** The CLK48 input provides timing for USB data signals; this clock must be 48MHz for proper USB operation. As an option, a 12MHz crystal can be connected across X1 and X2, in which case an internal PLL will develop the 48MHz signal. Refer to the TEST0-TEST1 strap options for selecting the mode of operation.
RESET#	19	I	**Reset:** If RESET# is asserted for a minimum of 1µs while PCICLK is stable at 33MHz, it causes the logic to enter its default state (all registers are set to their default values). AD[31:0], C/BE[3:0]#, and PAR are always driven low by the logic synchronously from the leading edge of RESET# and are always tristated from the trailing edge of RESET#. FRAME#, IRDY#, TRDY#, STOP#, and DEVSEL# are tristated from the leading edge of RESET# and remain so until driven as either a master or slave. RESET# may be asynchronous to PCICLK when asserted or negated, however, negation must occur with a clean, bounce-free edge.

2.3.2 PCI Bus Interface Signals

Signal Name	Pin No.	Pin Type	Signal Description
AD[31:0]	37:39, 42:45, 49, 51, 55:58, 61:62, 78:79, 82:84, 86:88, 93:95, 99:100, 2:1	I/O	**Address and Data Lines 31 through 0:** This bus carries the address and/or data during a PCI bus cycle. A PCI bus cycle has two phases - an address phase which is followed by one or more data phases. During the initial clock of the bus cycle, the AD bus contains a 32-bit physical byte address. AD[7:0] is the least significant byte (LSB) and AD[31:24] is the most significant byte (MBS). After the first clock of the cycle, the AD bus contains data. When the chip is the target, AD[31:0] are inputs during the address phase. For the data phase(s) that follow, the chip may supply data on AD[31:0] in the case of a read or accept data in the case of a write. When the chip is the master, it drives a valid address on AD[31:2] during the address phase, and drives write or accepts read data on AD[31:0] during the data phase. As a master, the chip always drives AD[1:0] low.
C/BE[3:0]#	49, 63, 77, 89	I/O	**Bus Command and Byte Enables 3 through 0:** These signals provide the command type information during the address phase and carry the byte enable information during the data phase. C/BE0# corresponds to byte 0, C/BE1# to byte 1, C/BE2# to byte 2, and C/BE3# to byte 3. If the chip is the initiator of a PCI bus cycle, it drives C/BE[3:0]#. When it is the target, it samples C/BE[3:0]#.

Signal Name	Pin No.	Pin Type	Signal Description
PAR	76	O	**Even Parity:** The logic calculates PAR for both the address and data phases of PCI cycles. PAR is valid one PCI clock after the associated address or data phase, but may or may not be valid for subsequent clocks. It is calculated based on 36 bits - AD[31:0] plus C/BE[3:0]#. "Even" parity means that the sum of the 36 bit values plus PAR is always an even number, even if one or more bits of C/BE[3:0]# indicate invalid data.
FRAME#	64	I/O (s/t/s)	**Cycle Frame:** This signal is driven by the current PCI bus master to indicate the beginning and duration of an access. The master asserts FRAME# at the beginning of a bus cycle, sustains the assertion during data transfers, and then negates FRAME# in the final data phase. FRAME# is an input when the chip is the target and an output when it is the initiator. FRAME# is tristated from the leading edge of RESET# and remains tristated until driven as either a master or slave.
IRDY#	67	I/O (s/t/s)	**Initiator Ready:** IRDY#, along with TRDY#, indicates whether the chip is able to complete the current data phase of the cycle. IRDY# and TRDY# are both asserted when a data phase is completed. During a write, the chip asserts IRDY# to indicate that it has valid data on AD[31:0]. During a read, the chip asserts IRDY# to indicate that it is prepared to accept data. IRDY# is an input when the chip is a target and an output when it is the initiator. IRDY# is tristated from the leading edge of RESET# and remains tristated until driven as either a master or a slave by the chip.
TRDY#	68	I/O (s/t/s)	**Target Ready:** TRDY#, along with IRDY#, indicates whether the chip is able to complete the current data phase of the cycle. TRDY# and IRDY# are both asserted when a data phase is completed. When the chip is acting as the target during read and write cycles, it performs in the following manner: 1. During a read, the chip asserts TRDY# to indicate that it has placed valid data on AD[31:0]. 2. During a write, the chip asserts TRDY# to indicate that is prepared to accept data. TRDY# is an input when the chip is the initiator and an output when it is the target. TRDY# is tristated from the leading edge of RESET# and remains so until driven as either a master or a slave by the chip.
STOP#	70	I/O (s/t/s)	**Stop:** STOP# is an output when the chip is the target and an input when it is the initiator. As the target, the chip asserts STOP# to request that the master stop the current cycle. As the master, the assertion of STOP# by a target forces the chip to stop the current cycle. STOP# is tristated from the leading edge of RESET# and remains so until driven by the chip acting as a slave.

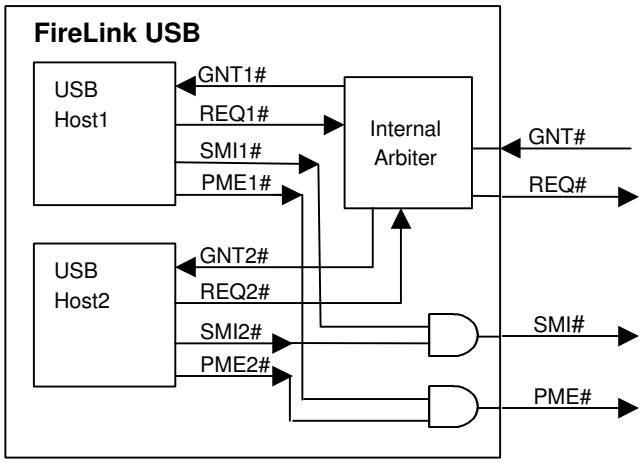
Signal Name	Pin No.	Pin Type	Signal Description
DEVSEL#	69	I/O (s/t/s)	**Device Select:** The chip claims a PCI cycle via positive decoding by asserting DEVSEL#. As an output, the chip drives DEVSEL# for two different reasons: 1. If the chip samples IDSEL active in configuration cycles, DEVSEL# is asserted. 2. When the chip decodes an internal address or when it subtractively decodes a cycle, DEVSEL# is asserted When DEVSEL# is an input, it indicates the target response to an chip master-initiated cycle. DEVSEL# is tristated from the leading edge of RESET# and remains so until driven by the chip acting as a slave.
IDSEL	50	I	**Initialization Device Select:** This signal is the "chip select" during configuration read and write cycles. IDSEL is sampled by the chip during the address phase of a cycle. If IDSEL is found to be active and the bus command is a configuration read or write, the chip claims the cycle with DEVSEL#.
PERR#	71	I/O	**Parity Error:** The chip uses this line to report data parity errors during any PCI cycle except a Special Cycle.
SERR#	75	I	**System Error:** The chip uses this line to report address parity errors and data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
REQ#	36	O	**Bus Request:** REQ# is asserted by the chip to request ownership of the PCI bus.
GNT#	35	I	**Bus Grant:** GNT# is sampled by the chip for an active low assertion, which indicates that it has been granted use of the PCI bus.
CLKRUN#	46	I/O	**Clock Run:** The CLKRUN# function is available on this pin and can be used to reduce chip power consumption during idle periods. It is an I/O sustained tristate signal and follows the PCI 2.1 defined protocol.
GPIO2			**General Purpose I/O pin 2:** These pins can be written or read by specific application software. Refer to PCICFG 53-55h for information.
INTB#	98	O	**PCI Interrupt B:** This signal can be connected to a PCI Interrupt line.

2.3.3 USB Interface Signals

Signal Name	Pin No.	Pin Type	Signal Description
D1+ D1-	13 14	diff	**USB Port 1 Differential Data Pair:** This pair comes from the first controller. These pins have no internal connection on the 82C863 part.
D2+ D2-	15 16	diff	**USB Port 2 Differential Data Pair:** This pair comes from the first controller.
D3+ D3-	28 29	diff	**USB Port 3 Differential Data Pair:** This pair comes from the second controller. These pins have no internal connection on the 82C863 part.
D4+ D4-	30 31	diff	**USB Port 4 Differential Data Pair:** This pair comes from the second controller.
PWRON1# PWRON2# PWRON3# PWRON4#	53 24 73 90	O	**Power On Lines 1, 2, 3 and 4:** These outputs are used to switch port VCC for the respective USB port. The controlled VCC is used only by the device connected to the port, and is not used by the chip. PWRON1# and PWRON3# are not used for the 82C863 part and can be left unconnected.
PWRFLT1# PWRFLT2# PWRFLT3# PWRFLT4#	54 23 74 91	I	**Power Fault Lines 1, 2, 3 and 4:** These inputs indicate that an over-current fault has occurred on the respective USB port. Their polarity can be both strap- and software-controlled: Refer to the Strap Options section for details. PWRFLT1# and PWRFLT3# should be tied to GND for the 82C863 part.

2.3.4 Host Controller shared signals: PME#, SMI#, REQ#, GNT#

Several other signals are shared by both host controllers in addition to the bused PCI signals. The shared signals are all active low. The diagram below best explains the internal connections of the chip.



2.3.5 Legacy and Interrupt Interface Signals

Signal Name	Pin No.	Pin Type	Signal Description
SMI#	97	O	**System Management Interrupt:** This signal is used to request a System Management Mode (SMM) interrupt. It can be connected to a spare EPMI pin on the host chipset.
GPIO4			**General Purpose I/O pin 4:** These pins can be written or read by specific application software. Refer to PCICFG 53-55h for information.
PME#	72	special	**Power Management Event:** This signal is used to wake up the system from a PCI Power Management (PCI/PM) power saving mode. This pin is normally tri-stated and is driven low when active. **Note:** When unpowered, the PME# driver output circuit will not be damaged if PME# is powered from another source. Moreover, once power is removed from the chip, this pin does not present a current path to ground.
GPIO3			**General Purpose I/O pin 3:** These pins can be written or read by specific application software. Refer to PCICFG 53-55h for information.
INTA#	1	O	**PCI Interrupt A:** This signal can be connected to a PCI interrupt line.
TEST0	21	I/O	**TEST Pin 0:** This pin is sampled by the chip at reset time to put the logic into a test mode if needed. See the STRAP OPTIONS section for details.
GPIO0			**General Purpose I/O pin 0:** These pins can be written or read by specific application software. Refer to PCICFG 53-55h for information.
TEST1	25	I/O	**TEST Pin 1:** This pin is sampled by the chip at reset time to put the logic into a test mode if needed. See the STRAP OPTIONS section for details.
GPIO1			**General Purpose I/O pin 1:** These pins can be written or read by specific application software. Refer to PCICFG 53-55h for information.

2.3.6 Power and Ground Pins

Signal Name	Pin No.	Pin Type	Signal Description
VCC	7, 22, 41, 60, 65, 81, 92,	P	**3.3V Power Connection:** Core voltage is always 3.3V. However, the PCI interface can be 5V as the PCI inputs are 5V-tolerant.
AVCC_PLL	10	P	**PLL Analog Power:** Connect to low-noise 3.3V.
AVCC_USB	17, 27	P	**USB I/O Analog Power:** Connect to low-noise 3.3V.
DVCC_USB	18, 26	P	**USB I/O Digital Power:** Connect to 3.3V.
GND	20,40,47, 59,66,80, 85,96	G	**Core Digital Ground:** Connect to board ground.
AGND_PLL	9	G	**PLL Analog Ground:** Connect to same board ground as GND.
AGND_USB	12, 32	G	**USB I/O Analog Ground:** Connect to same board ground as GND.
DGND_USB	11, 33	G	**USB I/O Digital Ground:** Connect to same board ground as GND.

2.3.7 Strap Options

The 82C862/3 component offers several operating mode choices at power-up time. These choices are selected through a strap resistor that pulls the related pin either up or down to the required level. A 4.7k ohm resistor is recommended.

Table 2. Strap Selected Options

Pin		Mode
PWRON3#		**Enable/Disable Second Host**
1		Enable Second USB Host Controller (Function 1) [DEFAULT]
0		Disable Second USB Host Controller. All clocks going to the logic for the second host are stopped to reduce power consumption.
TEST0	**TEST1**	**Mode Operation**
0	0	PLL Operational Mode using 12 MHz crystal on X1 and X2 [DEFAULT]
0	1	48 MHz clock Operation Mode. X1 connects to 48 MHz clock, X2 no-connect.
1	1	NAND Tree test mode
1	0	Tristate test mode
SMI#		**PCI Power Management PME# function / Reference USB clock**
0		PME# becomes 48 MHz reference clock output from PLL. Used for testing PLL. Also disables PCI power management, PCICFG 06h[4] = 0.
1		Enables PME# function and PCI power management, PCICFG 06h[4]=1. [DEFAULT]
PWRON2#		**Global/Individual Power Control**
1		Individual PWRON# and PWRFLT# for each port: [DEFAULT] HcRhDescA NoPowerSwitching=0 (MEMOFST 49h[1]) HcRhDescA PowerSwitchingMode=1 (MEMOFST 49h[0]) HcRhDescB PortPowerControlMask bit1,bit2=1,1 (MEMOFST4Eh[1,2]) HcRhDescA NoOvercurrentProtection=0 (MEMOFST 49h[4]) HcRhDescA OvercurrentProtectionMode=1 (MEMOFST 49h[3]])
0		Global PWRON# and PWRFLT# for each port: HcRhDescA NoPowerSwitching=0 (MEMOFST 49h[1]) HcRhDescA PowerSwitchingMode=0 (MEMOFST 49h[0]) HcRhDescB PortPowerControlMask bit1,bit2=0,0 (MEMOFST4Eh[1,2]) HcRhDescA NoOvercurrentProtection=0 (MEMOFST 49h[4]) HcRhDescA OvercurrentProtectionMode=0 (MEMOFST 49h[3]])

3.0 Functional Description

3.1 Universal Serial Bus (USB)

The 82C862/3 controller supports a PCI-based implementation of Universal Serial Bus utilizing the OpenHCI core developed by Compaq. The logic core consists of two USB host controller modules (making the part a multi-function PCI device), and a PCI interface controller.

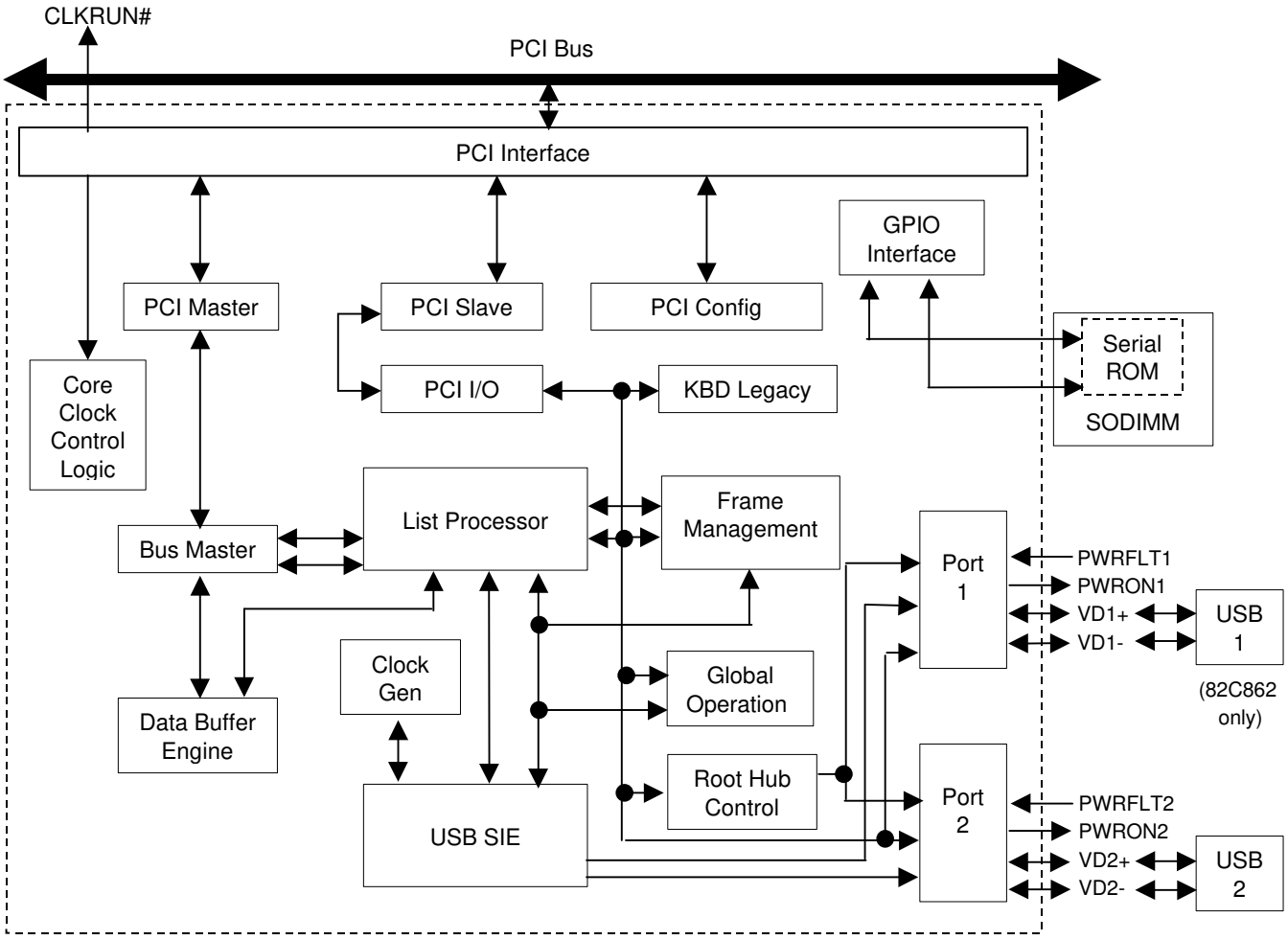
Each USB host controller module contains an integrated root hub that supports one (82C863) or two (82C862) downstream USB hubs or devices. Keyboard and mouse legacy support are also included for DOS compatibility with USB devices. This legacy support operates in conjunction with the primary host controller module as described later in this document.

This document must be used along with the following public domain reference documents to get the complete functional description of the USB core implementation.

- USB Specification, Revision 1.1
- OpenHCI Specification, Revision 1.0a
- PCI Specification, Version 2.2

A functional block diagram of one of the two USB controller modules is given in Figure 3. The other is identical.

Figure 3. USB Functional Block Diagram



3.2 PCI Controller

The PCI controller interfaces the host controller to the PCI bus. As a master, the PCI controller is responsible for running cycles on the PCI bus on behalf of the host controller. As a target, the PCI controller monitors the cycles on the PCI bus and determines when to respond to these cycles. A USB host controller module is a PCI target when it decodes cycles to its internal PCI configuration registers or to its internal PCI memory mapped I/O registers. The PCI controller asserts DEVSEL# in medium decode timing to claim a PCI transaction.

Since two PCI-interfaced USB controller modules reside on-chip, the logic includes an internal arbiter to select between the two modules when one or both make a bus mastering request.

The PCI configuration space of the primary USB host controller module is accessed as Device #X, Function #0, where Device #X depends on which AD line is connected to the IDSEL input. For the secondary USB host controller module, PCI configuration register space is accessed as Function #1 instead. PCI configuration space is hereafter referred to as PCICFG.

Table 3 gives a register map of the PCICFG register space (duplicated for each of the two functions). Refer to the "PCICFG Register Space" section for detailed bit information.

Table 3. PCI Controller Register Map

PCICFG	R/W	Register Name
00h-01h	RO	Vendor ID
02h-03h	RO	Device ID
04h-05h	R/W	Command
06h-07h	R/W	Status
08h	RO	Revision ID
09h-0Bh	RO	Class Code
0Ch	R/W	Cache Line Size
0Dh	R/W	Master Latency Timer
0Eh	RO	Header Type
0Fh	--	Reserved
10h-13h	R/W	Base Address Register 0
14h-2Bh	--	Reserved
2Ch-2Dh	RO	Subsystem Vendor
2Eh-2Fh	RO	Subsystem ID
30h-3Bh	--	Reserved
3Ch	R/W	Interrupt Line
3Dh	R/W	Interrupt Pin
3Eh	R/W	Minimum Grant

PCICFG	R/W	Register Name
3Fh	R/W	Maximum Latency
40h-45h	--	Reserved for factory test
46h-4Bh	--	Reserved
4Ch	R/W	Interrupt Pin Selection
4Dh	R/W	Miscellaneous Control
4Eh-4Fh	--	Reserved
50h	R/W	PCI Host Feature Control
51h	--	Reserved
52h	R/W	Strap Option Override
53h	R/W	GPIO Select
54h	R/W	GPIO Output Enable
55h	R/W	GPIO Data
56h-7Bh	--	Reserved
7Ch-7Fh	R/W	Subsystem ID Restore
80h-EFh	--	Reserved
F0h-F5h	R/W	PCI Power Management
F6h-FFh	--	Reserved

3.3 Clock Generation

The USB core requires an accurate 48MHz internal clock for proper operation. This clock can be obtained either by connecting an external 48MHz oscillator, or by connecting a 12MHz crystal.

To use the external 48MHz clock, connect the clock source to the X1 pin and strap TEST1 high. The X2 pin is not used in this configuration and must be left floating. This clock must be accurate to +/- 0.2%, or 2000ppm. Jitter must be less than +/- 1ns.

To use a 12MHz crystal, connect it to the X1 and X2 pins and strap TEST1 low. An internal PLL develops the required 48MHz clock. This PLL can be powered down when not in use through the PCI Power Management registers. Since the 12MHz clock generated is used to develop 48MHz internally, the crystal accuracy must be within +/- 0.05%, or 500ppm.

3.4 Power Management Features

FireLink USB implements new power management features which can reduce the overall power consumed in mobile USB applications. Key features are as follows.

The OS can put each USB controller module individually into USBSuspend state.

Once in USBSuspend state, the BIOS can turn off the USB I/O cells on each port for further power savings.

The external PCI clock can be stopped if system hardware is designed to use the CLKRUN# pin from the chip, which can also be used to awaken the system.

The external 48MHz USB clock can also be stopped along with the PCICLK when the system will be put into a Standby mode.

USB clocks to each of the internal modules can be stopped independently through the PCI power management registers.

Each of these features is described in the sections below.

3.4.1 Putting FireLink into USBSuspend State

Before a host system goes into a suspend state, the operating system should put the OHCI USB controller into USBSuspend mode by writing to register MEMOFST 04h[7:6] = 11.

3.4.2 Powering Down the USB I/O Cells

Once in USBSuspend state, the USB I/O cells can be disabled to reduce power by setting PCICFG 50h[1:0] = 11. If this feature is used, the I/O cells should be disabled by the BIOS before going into system-level Suspend, and re-enabled by the BIOS before giving control back to the operating system.

3.4.3 Stopping the 48MHz USB Clock

After the controller is put into USBSuspend state, still another step can be taken to further reduce power consumption: stop the 48MHz USB clock. If this route is taken, the USB clock must be stopped and started in a glitch free manner. The usual means of effecting this control would be through software control of the system clock generator circuit.

Once the USB clock is stopped, the system can be awakened by using PME#, which will be asserted on a USB wake up event (resume signalling, connect, disconnect). This system event should be designed to restart the 48MHz clock to the USB controller.

3.4.4 Using CLKRUN#

The CLKRUN# pin is always operational in the part; no enabling is required. The PCI Mobile Design Guide, available from the PCISIG, describes the operation of CLKRUN# in detail. Briefly, connected devices monitor this pin to see if it goes high, indicating that the host wants to stop the system PCICLKs. If the line goes high, connected devices are allowed to momentarily drive the pin low. The host will then take over driving this pin low until it wants to try again to stop the clocks.

The host system uses CLKRUN# to determine whether or not the USB controller requires a PCI clock by releasing CLKRUN#, which is always pulled high with a resistor. The USB controller power management logic will drive this pin low again as

required by the CLKRUN# specification if the controller is using the clock, i.e. whenever a USB device is attached. If the controller does not drive the clock low, the system is free to slow or stop the PCI clock.

3.4.5 Stopping the Internal USB Clocks

The chip is equipped with PCI Power Management registers. When either function is set to D3hot mode, its internal USB clock is switched off to effect a significant reduction in power consumption. Returning the system to D0 will restart the internal USB clock.

3.4.6 Power Control Modes

The chip pinout includes the following signals for controlling and monitoring USB power for the respective USB port:

- PWRON1-4# are active-low outputs to turn USB power on.
- PWRFLT1-4# are active-low inputs to detect over current.

At design time, it must be decided whether these control and monitoring signals will be used independently on a per-port basis (ideal situation), or paired together (for lower component cost). Consequently, the chip can strap into one of two power control modes:

- Individual PWRON# and PWRFLT# - entered when PWRON2# is sensed high at reset
- Global PWRON# and PWRFLT# - entered when PWRON2# is sensed low at reset.

The part supports two modes for turning on power to the respective USB ports: Global and Individual (per-port). This logic is contained in the Root Hub partition of each USB controller module, and consists of a portion for the Root Hub itself as well as portions for each individual port. The operation of Global and Individual power switching is explained below.

Global Power Switching is the mode that is supported in the original 82C861 design. In this mode either PWRON1# or PWRON2# can be used to turn on power for both ports on USB Host 1, and either PWRON3# or PWRON4# can be used to turn on power for both ports USB Host 2. When supporting this mode the following registers are of significance:

Register	Field	Value or Function
HcRhDescriptorA	NoPowerSwitching MEMOFST 49h[1]	0: Ports are power switched
HcRhDescriptorA	PowerSwitchingMode MEMOFST 49h[0]	0: All ports are powered at the same time
HcRhDescriptorB	PortPowerControlMask MEMOFST 4Eh[2:1]	Not Used
HcRhStatus	ClearGlobalPower (write) MEMOFST 50h[0]	This bit is written to ‘1’ to turn OFF power to all ports.
HcRhStatus	SetGlobalPower (write) MEMOFST 52h[0]	This bit is written to ‘1’ to turn ON power to all ports.
HcRhPort1Status HcRhPort2Status	PortPowerStatus (read) MEMOFST 55h[0] port 1 MEMOFST 59h[0] port 2	0=port power is off 1=port power is on Only Set/ClearGlobalPower controls this bit

Individual Power Switching is the mode in which the power to the USB ports can be controlled individually by using the Port Status registers for each port, or can also be controlled globally depending on the value in the PowerControlMask register. When strapping into this mode, the PowerControlMask registers will be set. All four signals, PWRON1#, PWRON2#, PWRON3#, and PWRON4# will be used to turn on the respective USB ports power and will be independently controlled. When supporting this mode the following registers are of significance:

Register	Field	Value or Function
HcRhDescriptorA	NoPowerSwitching MEMOFST 49h[1]	0: Ports are power switched
HcRhDescriptorA	PowerSwitchingMode MEMOFST 49h[0]	1: Each port is powered individually. This mode allows the port to be either global or individual controlled depending on value in PortPowerControlMask.
HcRhDescriptorB	PortPowerControlMask MEMOFST 4Eh[2:1]	This register determines if the ports power is controlled individually by the Port Status register, or globally by the Root Hub Status register. 0=port uses global Set/ClearGlobalPower 1=port uses per-port Set/ClearPortPower
HcRhStatus	ClearGlobalPower (write) MEMOFST 50h[0]	This bit is written to '1' to turn off power to ports whose PortPowerControlMask=0.
HcRhStatus	SetGlobalPower (write) MEMOFST 52h[0]	This bit is written to '1' to turn on power to ports whose PortPowerControlMask=0.
HcRhPort1Status HcRhPort2Status	PortPowerStatus (read) MEMOFST 55h[0] port 1 MEMOFST 59h[0] port 2	0=port power is off 1=port power is on If per-port switching is enabled for this port, then only Set/ClearPortPower affect this bit. If global mode is enabled, then Set/ClearGlobalPower control this bit.
HcRhPort1Status HcRhPort2Status	SetPortPower (write) MEMOFST 55h[0] port 1 MEMOFST 59h[0] port 2	1: sets PortPowerStatus Only valid if port is enabled for per-port switching.
HcRhPort1Status HcRhPort2Status	ClearPortPower (write) MEMOFST 55h[1] port 1 MEMOFST 59h[1] port 2	1: clear PortPowerStatus Only valid if port is enabled for per-port switching.

The logic also supports both Global and per-port overcurrent detection as follows.

Global overcurrent mode – either PWRFLT1# or PWRFLT2# can be used to detect an overcurrent condition on any port on USB Host 1, and either PWRFLT3# or PWRFLT4# can be used to detect an overcurrent condition on any port on USB Host 2. For example, if PWRFLT1# is asserted, it means an overcurrent condition exists on USB Host 1, resulting in power shutoff for both ports on USB Host 1, and setting of the appropriate global overcurrent indicator bits.

Register	Field	Value or Function
HcRhDescriptorA	NoOvercurrentProtection MEMOFST 49h[4]	0: Over-current status is reported
HcRhDescriptorA	OverCurrentProtectionMode MEMOFST 49h[3]	0: Global - Over-current reported collectively for all ports
HcRhStatus	OverCurrentIndicator MEMOFST 50h[1]	1: Global over-current exists 0: power operations normal
HcRhStatus	OverCurrentIndicatorChange MEMOFST 52h[1]	Set by hardware when OverCurrentIndicator bit changes. Write a '1' to clear this bit.
HcRhPort1Status HcRhPort2Status	PortOverCurrentIndicator MEMOFST 54h[3] port 1 MEMOFST 58h[3] port 2	Not used, set to '0' for global over-current.
HcRhPort1Status HcRhPort2Status	PortOverCurrentIndicatorChange MEMOFST 56h[3] port 1 MEMOFST 5Ah[3] port 2	Not used, set to '0' for global over-current.

Per-Port overcurrent mode – PWRFLT1 #, PWRFLT2#, PWRFLT3#, and PWRFLT4# are all used to monitor each port individually. If an overcurrent condition exists on one port, power is only shut off to that port.

Register	Field	Value or Function
HcRhDescriptorA	NoOvercurrentProtection MEMOFST 49h[4]	0: Over-current status is reported
HcRhDescriptorA	OverCurrentProtectionMode MEMOFST 49h[3]	1: Over-current is reported on a per-port basis
HcRhStatus	OverCurrentIndicator MEMOFST 50h[1]	Not used, always '0' for per-port over-current mode.
HcRhStatus	OverCurrentIndicatorChange MEMOFST 52h[1]	Not used, always '0' for per-port over-current mode.
HcRhPort1Status HcRhPort2Status	PortOverCurrentIndicator MEMOFST 54h[3] port 1 MEMOFST 58h[3] port 2	0: no over-current condition 1: over-current condition exists
HcRhPort1Status HcRhPort2Status	PortOverCurrentIndicatorChange MEMOFST 56h[3] port 1 MEMOFST 5Ah[3] port 2	Set by hardware when PortOverCurrentIndicator bit changes. Write a '1' to clear this bit.

3.5 Host Controller

This block is the operational control block in the USB core. It is responsible for the host controller operational states (Suspend, Disabled, Enabled), special USB signaling (Reset, Resume), status, interrupt control, and host controller configuration information.

The host controller (HC) interface registers are PCI memory mapped I/O, hereafter referred to as MEMOFST. Table 4 gives a register map for the MEMOFST register space. Refer to the "Host Controller Register Space" section for detailed bit information.

Table 4. Host Controller Register Map

MEMOFST	R/W	Register Name
00h-03h	RO	HcRevision
04h-07h	R/W	HcControl
08h-0Bh	R/W	HcCommandStatus
0Ch-0Fh	R/W	HcInterruptStatus
10h-13h	R/W	HcInterrupt Enable
14h-17h	R/W	HcInterrupt Disable
18h-1Bh	R/W	HcHCCA
1Ch-1Fh	R/W	HcPeriodCurrentED
20h-23h	R/W	HcControlHeadED
24h-27h	R/W	HcControlCurrentED
28h-2Bh	R/W	HcBulkHeadED
2Ch-2Fh	R/W	HcBulkCurrentED
30h-33h	R/W	HcDoneHead
34h-37h	R/W	HcFmInterval
38h-3Bh	R/W	HcFrameRemaining
3Ch-3Fh	R/W	HcFmNumber
40h-43h	R/W	HcPeriodicStart
44h-47h	R/W	HcLSThreshold
48h-4Bh	R/W	HcRhDescriptorA
4Ch-4Fh	R/W	HcRhDescriptorB
50h-53h	R/W	HcRhStatus
54h-57h	R/W	HcRhPort1Status
58h-5Bh	R/W	HcRhPort2Status

3.5.1 Legacy Support

Four registers are provided for legacy support:

1. HceControl
- - Used to enable and control the emulation hardware and report various status information.

2. HceInput
- - Emulation side of the legacy Input Buffer register.

3. HceOutput
- - Emulation side of the legacy Output Buffer register where keyboard and mouse data is to be written by software.

4. HceStatus
- - Emulation side of the legacy Status register.

These registers are located in the Host Controller Register Space; from MEMOFST 100h through 10Fh. Table 5 shows a register map of these registers. Refer to the "Legacy Support Registers" section for detailed bit information.

Table 5. Legacy Support Register Map

MEMOFST	R/W	Register Name
100h-103h	R/W	HceControl
104h-107h	R/W	HceInput
108h-10Bh	R/W	HceOutput
10Ch-10Fh	R/W	HceStatus

3.5.2 Intercept Port 60h and 64h Accesses

The HceStatus, HceInput, and HceOutput registers are accessible at I/O Ports 60h and 64h when emulation is enabled. Reads and writes to these registers using the I/O Ports do have some side effects as shown in Table 6. However, accessing these registers directly through their memory address produces no side effects.

When emulation is enabled, I/O accesses of Ports 60h and 64h must be handled by the Host Controller (HC). The HC must be positioned in the system so that it can do a positive decode of accesses to Ports 60h and 64h on the PCI bus. If a keyboard controller is present in the system, it must either use subtractive decode or have provisions to disable its decode of Ports 60h and 64h. If the legacy keyboard controller uses positive decode and is turned off during emulation, it must be possible for the emulation code to quickly re-enable and disable the legacy keyboard controller Port 60h and 64h decode. This is necessary to support a mixed operating environment.

Table 6. Emulated Registers and Side Effects

Register Contents Accessed/Modified	Side Effect
HceOutput	• A read from Port 60h will set the Output Full bit (MEMOFST 10Ch[0]) to 0.
HceInput	• A write to Port 60h will set the Input Full bit (MEMOFST 10Ch[1]) to 1 and the Cmd Data bit (MEMOFST 10Ch[3]) to 0. • A write to Port 64h will set the: Input Full bit (MEMOFST 10Ch[1]) to 0 and the Cmd Data bit (MEMOFST 10Ch[3]) to 1.
HceStatus	• A read from Port 64h returns the current value of the HceStatus register.

3.6 General Purpose Pins

The strap pins TEST0, TEST1, CLKRUN#, PME#, and SMI# are multifunction pins that offer general purpose I/O (GPIO) functionality.

At reset time these pins are always input pins. After being sampled at reset to determine strap selections for the chip logic, these pins can be programmatically selected to be GPIO signals. TEST0 and TEST1 are automatically available as GPIO pins after reset is de-asserted, since they have no other assigned functions. The other pins must be specifically enabled for GPIO if their primary function assignment is not needed. The PIO mapping is as follows.

Signal	PIO signal mapped to
TEST0	PIO0
TEST1	PIO1
CLKRUN#	PIO2
PME#	PIO3
SMI#	PIO4

Refer to PCICFG 53h, 54h, and 55h for information on selection and direction of PIO pins. Note that PIO pins can be used along with host CPU software to generate I2C interface signaling; contact OPTi for details or sample code.

4.0 Register Descriptions

The chip has three types of register spaces:

1. PCI Configuration Register Space
2. Host Controller Register Space
3. I/O Register Space

The subsections that follow detail the locations and access mechanisms for the registers located within these register spaces.

Notes: 1. All bits/registers are read/write and their default value is 0 unless otherwise specified.

2. All reserved bits/registers MUST be written to 0 unless otherwise specified.

4.1 PCICFG Register Space

FireLink USB implements a multi-function PCI device.

Function 0: Primary USB host controller module

Function 1: Secondary USB host controller module.

The two USB controller modules each have their own PCI configuration space. The configuration space of both USB controllers are similar except for the value in the Interrupt Pin register (PCICFG 3Dh) and the Interrupt Pin Selection register (PCICFG 4Ch), because the controllers are assigned different interrupt pins by default.

The configuration space of each PCI USB controller module is referred to as PCICFG. The bit formats for these registers are described in the following section.

4.1.1 Programming Differences from 82C861 Component

While the physical device part number of this chip is 82C862 or 82C863, the USB controller modules identify themselves as 82C861 to maintain backward software compatibility with the previous OPTi chip. Software can differentiate between the chips by reading the Revision ID of 20h in PCICFG 08h (previous revisions read back 10h or lower).

Additional revision 20h changes that relate to the programming interface are as follows.

- The 82C862/3 component adds PCI power management, reflected in changes in PCICFG 06h and the addition of PCICFG 34h, 4Dh, and F0-F5h.
- The 82C862/3 part provides a way to restore the Subsystem Vendor ID and Subsystem ID values in a single-step process, necessary for proper context restoration after the chip is powered down during OS Suspend operations. This new approach is reflected in the deletion of PCICFG 50h[3] and the addition of PCICFG 7C-7Fh.
- The limited-functionality "I2C" general purpose I/O pins of the 82C861 part have been replaced by true GPIO pins, resulting in the deletion of PCICFG 4Eh.
- The IRQ Driveback feature is no longer supported, resulting in the deletion of PCICFG 51h and 54-57h.
- Changes to the chip pinout result in major changes to the PCICFG 52h bit definitions.
- PCICFG 4Ch has been added to allow both USB controller modules to share a single PCI interrupt.
- All bits of MEMOFST 4Bh are now read/writeable (previous chip versions allowed only bits [1:0] to be written).

4.1.2 PCICFG 00h-FFh

7	6	5	4	3	2	1	0
PCICFG 00h			**Vendor Identification Register (RO)**				**Default = 45h**
PCICFG 01h							**Default = 10h**
PCICFG 02h			**Device Identification Register (RO)**				**Default = 61h**
PCICFG 03h							**Default = C8h**
PCICFG 04h			**Command Register - Byte 0**				**Default = 00h**
Wait cycle control: USB core does not need to insert a wait state between address and data on the AD lines. This bit is always 0.	PERR# (response) detection enable bit: 0 = PERR# not asserted 1 = USB core can assert PERR# if it is the receiving data agent and detects a data parity error.	VGA palette snooping: This bit is always 0.	Postable memory write command: Not used when USB core is a master. This bit is always 0.	Special Cycles: USB core does not run Special Cycles on PCI. This bit is always 0.	USB core can run PCI master cycles: 0 = Disable 1 = Enable	USB core responds as a target to memory cycles. 0 = Disable 1 = Enable	USB core responds as a target to I/O cycles: 0 = Disable 1 = Enable
PCICFG 05h			**Command Register - Byte 1**				**Default = 00h**
Reserved: These bits are always 0.						Back-to-back enable: USB core only acts as a master to a single device, so this functionality is not needed. This bit is always 0.	SERR# (response) detection enable bit: 0 = SERR# not asserted 1 = USB core asserts SERR#
PCICFG 06h			**Status Register - Byte 0**				**Default = 90h**
Fast back-to-back capability: USB core supports fast back-to-back transactions when they are not to same agent. This bit is always 1.	Reserved		Capabilities bit (RO): 0=No PCI Power Management 1=PCI Power Management Available See note.	Reserved			

Note: Bit [4] enables extended PCI capabilities. This bit =1 by default, enabling PCI power management capabilities. PCI power management is enabled/disabled by a strap option, which can be overridden by writing PCICFG 4Dh[1]=0 to disable PCI PM, or writing PCICFG 4Dh[1]=1 to enable PCI PM.

7	6	5	4	3	2	1	0
PCICFG 07h			**Status Register - Byte 1**				**Default = 02h**
Detected parity error: This bit is set to 1 whenever the USB core detects a parity error, even if PCICFG 04h[6] is disabled. Write 1 to clear.	SERR# status: This bit is set to 1 whenever the USB core detects a PCI address parity error. Write 1 to clear.	Received master abort status: Set to 1 when the USB core, acting as a PCI master, aborts a PCI bus memory cycle. Write 1 to clear.	Received target abort status: This bit is set to 1 when a USB core generated PCI cycle (USB core is the PCI master) is aborted by a PCI target. Write 1 to clear.	Signaled target abort status: This bit is set to 1 when the USB core signals target abort. Write 1 to clear.	DEVSEL timing (RO): Indicates DEVSEL# timing when performing a positive decode. Since DEVSEL# is asserted to meet the medium timing, these bits are encoded as 01.		Data parity reported: Set to 1 if PCICFG 04h[6] is set and the USB core detects PERR# asserted while acting as PCI master (whether PERR# was driven by USB core or not.)
PCICFG 08h			**Revision Identification Register (RO)**				**Default = 20h**
PCICFG 09h			**Class Code Register (RO)**				**Default = 10h**
PCICFG 0Ah							**Default = 03h**
PCICFG 0Bh							**Default = 0Ch**
PCICFG 0Ch			**Cache Line Size Register**				**Default = 00h**
PCICFG 0Dh			**Master Latency Timer Register**				**Default = 00h**
PCICFG 0Eh			**Header Type Register (RO)**				**Default = 80h**
Multi-function device: 1=Yes (always)	Layout type = 00h (no special layout)						
PCICFG 0Fh			**Reserved**				**Default = 00h**
PCICFG 10h-13h			**Base Address Register 0**				**Default = 00h**

This register identifies the base address of a contiguous memory space in main memory. POST will write all 1s to this register, then read back the value to determine how big of a memory space is requested. After allocating the requested memory, POST will write the upper bytes with the base address.

Bits [31:0] correspond to: 10h = [7:0], 11h = [15:8], 12h = [23:16], 13h = [31:24].

- Bit [0] - Indicates that the operational registers are mapped into memory space. Always = 0.
- Bits [2:1] - Indicates that the base register is 32 bits wide and can be placed anywhere in 32-bit memory space. Always = 0.
- Bit [3] - Indicates no support for prefetchable memory. Always = 0.
- Bits [11:4] - Indicates a 4K byte address range is requested, Always = 0.
- Bits [31:12] - Base Address: Post writes the value of the memory base address to this register.

PCICFG 14h-2Bh	**Reserved**	**Default = 00h**
PCICFG 2Ch	**Subsystem Vendor ID Register (RO) - Byte 0**	**Default = 45h**
The Subsystem Vendor ID register is read-only but its value can be changed through PCICFG 7Dh:7Ch.		
PCICFG 2Dh	**Subsystem Vendor ID Register (RO) - Byte 1**	**Default = 10h**
PCICFG 2Eh	**Subsystem ID Register (RO) Byte 0**	**Default = 61h**
The Subsystem ID register is read-only but its value can be changed through PCICFG 7Fh:7Eh.		
PCICFG 2Fh	**Subsystem ID Register (RO) Byte 1**	**Default = C8h**
PCICFG 30h-33h	**Reserved**	**Default = 00h**

7	6	5	4	3	2	1	0

PCICFG 34h — **Capabilities Pointer Register (RO)** — **Default = F0h**

This register provides the offset into the PCI Configuration Space of the USB controller for the location of the PCI Power Management register block. This location is PCICFG F0h

PCICFG 35h-3Bh — **Reserved** — **Default = 00h**

PCICFG 3Ch — **Interrupt Line Register** — **Default = 00h**

This register identifies the system interrupt controller line to which the interrupt pin of this USB controller module is connected. The value of this register is used by device drivers and has no direct meaning to the USB core.

PCICFG 3Dh — **Interrupt Pin Register** — **Primary Default = 01h**, **Secondary Default = 02h**

This register identifies the interrupt pin a device uses. The primary USB controller module uses INTA#, so this value reads 01h by default; the secondary USB controller module uses INTB#, so this value reads 02h by default. The interrupt pin used by each USB controller module can be changed via the respective PCICFG 4Ch[1:0].

PCICFG 3Eh — **Minimum Grant Register (RO)** — **Default = 00h**

Reserved

PCICFG 3Fh — **Maximum Latency Register (RO)** — **Default = 00h**

Reserved

PCICFG 40h-44h — **Reserved** — **Default = 00h**

These registers are for internal testing purposes. Do not write to these registers.

PCICFG 45h — **Reserved** — **Default = 00h**

This register is for internal testing purposes. Do not write to this register.

Reserved	Reserved	SIE Pipelining 0=Enable 1=Disable

PCICFG 46h-4Bh — **Reserved** — **Default = 00h**

PCICFG 4Ch — **Interrupt Pin Selection Register** — **Function 0 Default = 00h**, **Function 1 Default = 01h**

Reserved	USB controller interrupt pin: 00 = PCIRQ0# (INTA#) 01 = PCIRQ1# (INTB#) 10 = PCIRQ2# (INTC#) 11 = PCIRQ3# (INTD#) The interrupt pin selected will be reflected in PCICFG 3Dh.

PCICFG 4Dh — **Miscellaneous Control Register** — **Default = 00h**

Reserved	State of Capabilities bit: 0 = Force PCICFG 06h[4] = 0 1 = Force PCICFG 06h[4] = 1	Reserved

PCICFG 4E-4Fh — **Reserved** — **Default = 00h**

7	6	5	4	3	2	1	0
PCICFG 50h			**PCI Host Feature Control Register**				**Default = 00h**
Reserved			Reserved, formerly CLKRUN# mode control	Reserved, formerly Subsystem Vendor ID write enable control	Reserved, formerly CLKRUN# enable control	Port 2 output: 0 = Enable 1 = Disable (Controls USB I/O cells to save power)	Port 1 output: 0 = Enable 1 = Disable (Controls USB I/O cells to save power)
PCICFG 51h			**Reserved**				**Default = 00h**
PCICFG 52h			**Strap Option Override**				**Default = 03h**
Reserved	Read/write factory test mode 0=Disable 1=Enable	TEST0 Strap Value 0 = Low (Operational) 1 = High (Test Mode)	TEST1 Strap Value 0 = Low - use 12MHz crystal and PLL 1 = High - use external 48MHz	PWRON3# Strap Value – Secondary Controller Mode 0 = Disable 1 = Enable	SMI# Strap Selection 0 = PME# used as 48MHz output 1 = PME# pin functional	PWRFLT Polarity: 0 = High 1 = Low	PWRON polarity: 0 = High 1 = Low
PCICFG 53h			**GPIO Select Register**				**Default = 00h**
PIO4 Direction 0=Input 1=Output	PIO3 Direction 0=Input 1=Output	PIO2 Direction 0=Input 1=Output	PIO1 Direction 0=Input 1=Output	PIO0 Direction 0=Input 1=Output	SMI# / PIO4 Select 0=SMI# (default) 1=PIO4	PME# / PIO3 Select 0=PME# (default) 1=PIO3	CLKRUN# / PIO2 Select 0=CLKRUN# (default) 1=PIO2
PCICFG 54h			**GPIO Output Enable Register**				**Default = 00h**
Reserved			PIO4 Buffer 0=Disable 1=Enable	PIO3 Buffer 0=Disable 1=Enable	PIO2 Buffer 0=Disable 1=Enable	PIO1 Buffer 0=Disable 1=Enable	PIO0 Buffer 0=Disable 1=Enable
These bits control buffer driving for those GPIO pins selected to be outputs.							
PCICFG 55h			**GPIO Data Register**				**Default = 00h**
Reserved			PIO4 Data 0=Low 1=High	PIO3 Data 0=Low 1=High	PIO2 Data 0=Low 1=High	PIO1 Data 0=Low 1=High	PIO0 Data 0=Low 1=High
For input pins these bits return the value presently being driven onto the pins; for output pins these bits select the level that will be driven.							
PCICFG 56h-7Bh			**Reserved**				**Default = 00h**
PCICFG 7Ch			**Subsystem Vendor ID Restore Register - Byte 0**				**Default = 45h**
The register is used to program the value of the Subsystem Vendor ID register at PCICFG 2Dh:2Ch.							
PCICFG 7Dh			**Subsystem Vendor ID Restore Register - Byte 1**				**Default = 10h**
PCICFG 7Eh			**Subsystem ID Restore Register - Byte 0**				**Default = 61h**
The register is used to program the value of the Subsystem ID register at PCICFG 2Fh:2Eh.							
PCICFG 7Fh			**Subsystem ID Restore Register - Byte 1**				**Default = C8h**
PCICFG 80h - EFh			**Reserved**				**Default = 00h**

7	6	5	4	3	2	1	0
PCICFG F0h			**CAP_ID Register (RO)**				**Default = 01h**
This register returns a value of 01h to identify the Capabilities list item as being the PCI Power Management Register Block.							
PCICFG F1h			**Next_Item_Ptr Register (RO)**				**Default = 00h**
This register returns a value of 00h to indicate that there are no additional items in the Capabilities list.							
PCICFG F2h			**PMC Register (RO) - Byte 0**				**Default = 01h**
Reserved		Device Specific Initialization (DSI): 0 = DSI is not required	Reserved	PME Clock: 0 = PME# clock not required to generate PME#	Version: 001 = This function complies with Revision 1.0 of the PCI PowerManagement Interface Specification.		
PCICFG F3h			**PMC Register (RO) - Byte 1**				**Default = 40h**
PME Support: 01000 = The PCI USB controller supports PME# generation from $D3_{hot.}$					D2 device state support: 0 = No	D1 device state support: 0 = No	Reserved
PCICFG F4h			**PMCSR Register - Byte 0**				**Default = 00h**
Reserved							PowerState (R/W): 00 = D0 01 = D1 (Not Supported) 10 = D2 (Not Supported) 11 = D3hot This field is used both to determine the current power state and to set a new power state. Unsupported states will be ignored when written to.
PCICFG F5h			**PMCSR Register - Byte 1**				**Default = 00h**
PME Status (R/W): This bit is set when a PME event is generated. Write 1 to clear.	Data_Scale (RO): 00 = Data register is not supported		Data_Select (RO): 0000 = Data register is not supported				PME_En (R/W): 0 = PME# assertion is disabled 1 = PME# is asserted when PME_ Status = 1
PCICFG F6h - FFh			**Reserved**				**Default = 00h**

4.2 Host Controller Register Space

This register space is the operational control block in the USB core. It is responsible for the host controller operational states (Suspend, Disabled, Enabled), special USB signaling (Reset, Resume), status, interrupt control, and host controller configuration information.

The host controller (HC) interface registers are PCI memory mapped I/O, hereafter referred to as MEMOFST. The bit formats for these registers are described below.

4.2.1 MEMOFST 00h-5Ch

7	6	5	4	3	2	1	0

MEMOFST 00h — **HcRevision Register (RO)** — **Default = 10h**

MEMOFST 01h-03h — **Default = 000001h**

Bits [31:0] correspond to: 00h = [7:0], 01h = [15:8], 02h = [23:16], 03h = [31:24]

- Bits [7:0] Revision - Indicates the Open HCI Specification revision number implemented by hardware (X.Y = XYh). FireLink support Specification 1.0.
- Bits [31:8] Reserved

MEMOFST 04h — **HcControl Register - Byte 0** — **Default = 00h**

HC Functional State:	Processing of Bulk List:	Processing of Control List:	Disable Isochronous List when Periodic List is enabled:(1)	Processing of Periodic (interrupt and isochronous) List:	Control Bulk Service Ratio:
00 = USB Reset 01 = USB Resume 10 = USB Operational 11 = USB Suspend The HC may force a state change from USB Suspend to USB Resume after detecting resume signaling from a downstream port.	0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Yes 1 = No	0 = Disable 1 = Enable The HC checks this bit prior to attempting any periodic transfers in a frame.	Specifies the number of control endpoints serviced for every bulk endpoint. Encoding is NÐ1 where N is the number of control endpoints (i.e., 00 = 1 control endpoint; 11 = 4 control endpoints).

(1) Disabling the Isochronous List when the Periodic List is enabled allows interrupt endpoint descriptors to be serviced. While processing the Period List, the HC will check bit 3 when it finds an isochronous endpoint descriptor.

MEMOFST 05h — **HcControl Register - Byte 1** — **Default = 00h**

Reserved	Remote Wakeup Connected Enable:	Remote Wakeup Connected (RO):	Interrupt Routing:
	If a remote wakeup signal is supported, this bit is used to enable that operation. Since there is no remote wakeup signal supported, this bit is ignored.	Indicates whether the HC supports a remote wakeup signal. This implementation does not support any such signal. The bit is hardcoded to 0.	0 = Interrupts routed to normal interrupt mechanism (INTA#) 1 = Interrupts routed to SMI

MEMOFST 06h-07h — **HcControl Register - Bytes 2 & 3** — **Default = 00h**

Reserved

7	6	5	4	3	2	1	0
MEMOFST 08h			**HcCommandStatus Register - Byte 0**				**Default = 00h**
Reserved				Ownership Change Request: When set by software, this bit sets the Ownership Change bit (MEMOFST 0Fh[6]). Cleared by software.	Bulk List has an active endpoint descriptor?(1) 0 = No 1 = Yes	Control List has an active endpoint descriptor?(1) 0 = No 1 = Yes	HC Reset: Writing a 1 initiates a software reset. This bit is cleared by the HC upon completion of reset operation.
(1) The bit may be set by either software or the HC. It is cleared by the HC each time it begins processing the head of the list (Bulk List for bit 2, Control List for bit 1)							
MEMOFST 09h			**HcCommandStatus Register - Byte 1**				**Default = 00h**
Reserved							
MEMOFST 0Ah			**HcCommandStatus Register - Byte 2**				**Default = 00h**
Reserved						Schedule Overrun Count: This field increments every time the Scheduling Overrun bit (MEMOFST 0Ch[0] is set. The count wraps from 11 to 00.	
MEMOFST 0Bh			**HcCommandStatus Register - Byte 3**				**Default = 00h**
Reserved							
MEMOFST 0Ch			**HcInterrupt Status Register - Byte 0***				**Default = 00h**
Reserved	Root Hub Status Change: This bit is set when the content of HcRh Status (50h-53h) or the content of any HcRhPort Status Register (54h-5Bh) has changed.	Frame Number Overflow: This bit is set when MEMOFST 3Ch[15] (Frame Number Register) changes from 0-to-1 or from 1-to-0.	Unrecoverable Error: This event is not implemented and is hardcoded to 0. All writes are ignored.	Resume Detected: This bit is set when the HC detects resume signaling on a downstream port.	Start of Frame: This bit is set when the Frame Management block signals a "Start of Frame" event.	Writeback Done Head: This bit is set after the Host Controller has written HcDoneHead to HccaDoneHead .	Scheduling Overrun occurred? 0 = No 1 = Yes
MEMOFST 0Dh-0Eh			**HcInterruptStatus Register - Bytes 1 & 2**				**Default = 00h**
Reserved							

7	6	5	4	3	2	1	0
MEMOFST 0Fh			**HcInterruptStatus Register - Byte 3***				**Default = 00h**
Reserved	Ownership Change: This bit is set when the Ownership Change Request bit (MEMOFST 08h[3]) is set.	Reserved					
* Writing a 1 to a bit in this register clears the corresponding bit, while writing a 0 leaves the bit unchanged.							
MEMOFST 10h			**HcInterruptEnable Register - Byte 0***				**Default = 00h**
Reserved	Allow interrupt generation due to Root Hub Status Change: 0 = Ignore 1 = Enable	Allow interrupt generation due to Frame Number Overflow: 0 = Ignore 1 = Enable	Reserved All writes to this bit are ignored.	Allow interrupt generation due to Resume Detected: 0 = Ignore 1 = Enable	Allow interrupt generation due to Start of Frame: 0 = Ignore 1 = Enable	Allow interrupt generation due to Writeback Done Head: 0 = Ignore 1 = Enable	Allow interrupt generation due to Scheduling Overrun: 0 = Ignore 1 = Enable
MEMOFST 11h-12h			**HcInterruptEnable Register - Bytes 1 & 2**				**Default = 00h**
Reserved							
MEMOFST 13h			**HcInterruptEnable Register - Byte 3***				**Default = 00h**
Master interrupt generation: 0 = Ignore 1 = Allows all interrupts to be enabled in 10h-13h.	Allow interrupt generation due to Ownership Change: 0 = Ignore 1 = Enable	Reserved					
* Writing a 1 to a bit in this register sets the corresponding bit, while writing a 0 leaves the bit unchanged.							
MEMOFST 14h			**HcInterruptDisable Register - Byte 0***				**Default = 00h**
Reserved	Allow interrupt generation due to Root Hub Status Change: 0 = Ignore 1 = Disable	Allow interrupt generation due to Frame Number Overflow: 0 = Ignore 1 = Disable	Reserved All writes to this bit are ignored.	Allow interrupt generation due to Resume Detected: 0 = Ignore 1 = Disable	Allow interrupt generation due to Start of Frame: 0 = Ignore 1 = Disable	Allow interrupt generation due to Writeback Done Head: 0 = Ignore 1 = Disable	Allow interrupt generation due to Scheduling Overrun: 0 = Ignore 1 = Disable
MEMOFST 15h-16h			**HcInterruptDisable Register - Bytes 1 & 2**				**Default = 00h**
Reserved							

7	6	5	4	3	2	1	0
MEMOFST 17h			**HcInterruptDisable Register - Byte 3***				**Default = 00h**
Master interrupt generation: 0 = Ignore 1 = Allows all interrupts to be disabled in 10h-13h.	Allow interrupt generation due to Ownership Change: 0 = Ignore 1 = Disable	Reserved					
* Writing a 1 to a bit in this register clears the corresponding bit, while writing a 0 leaves the bit unchanged.							

MEMOFST 18h-1Bh **HcHCCA Register** **Default = 00h**

Bits [31:0] correspond to: 18h = [7:0], 19h = [15:8], 1Ah = [23:16], 1Bh = [31:24].

- Bits [7:0] Reserved
- Bits [31:8] Pointer to HCCA base address

MEMOFST 1Ch-1Fh **HcPeriodCurrentED Register** **Default = 00h**

Bits [31:0] correspond to: 1Ch = [7:0], 1Dh = [15:8], 1Eh = [23:16], 1Fh = [31:24].

- Bits [3:0] Reserved
- Bits [31:4] Pointer to current Periodic List End Descriptor

MEMOFST 20h-23h **HcControlHeadED Register** **Default = 00h**

Bits [31:0] correspond to: 20h = [7:0], 21h = [15:8], 22h = [23:16], 23h = [31:24].

- Bits [3:0] Reserved
- Bits [31:4] Pointer to current Control List Head End Descriptor

MEMOFST 24h-27h **HcControlCurrent ED** **Default = 00h**

Bits [31:0] correspond to: 24h = [7:0], 25h = [15:8], 26h = [23:16], 27h = [31:24].

- Bits [3:0] Reserved
- Bits [31:4] Pointer to current End Descriptor in Control List

MEMOFST 28h-2Bh **HcBulkHeadED Register** **Default = 00h**

Bits [31:0] correspond to: 28h = [7:0], 29h = [15:8], 2Ah = [23:16], 2Bh = [31:24].

- Bits [3:0] Reserved
- Bits [31:4] Pointer to current Bulk List Head End Descriptor in Control List

MEMOFST 2Ch-2Fh **HcBulkCurrentED Register** **Default = 00h**

Bits [31:0] correspond to: 2Ch = [7:0], 2Dh = [15:8], 2Eh = [23:16], 2Fh = [31:24].

- Bits [3:0] Reserved
- Bits [31:4] Pointer to current Bulk List End Descriptor

MEMOFST 30h-33h **HcDoneHead Register** **Default = 00h**

Bits [31:0] correspond to: 30h = [7:0], 31h = [15:8], 32h = [23:16], 33h = [31:24].

- Bits [3:0] Reserved
- Bits [31:4] Pointer to current Done List Head End Descriptor

7	6	5	4	3	2	1	0

MEMOFST 34h-37h **HcFmInterval Register** **Default = xxxx2EDFh**

Bits [31:0] correspond to: 34h = [7:0], 35h = [15:8], 36h = [23:16], 37h = [31:24].

- Bits [13:0] Frame Interval - These bits specify the length of a frame as (bit times - 1). For 12,000 bit times in a frame, a value of 11,999 is stored here.
- Bits [15:14] Reserved
- Bits [30:16] FS Largest Data Packet: These bits specify a value which is loaded into the Largest Data Packet Counter at the beginning of each frame.
- Bit 31 Frame Interval Toggle - This bit is toggled by HCD whenever it loads a new value into the Frame Interval bits (bits [13:0]).

MEMOFST 38h-3Bh **HcFrameRemaining Register** **Default = 00h**

Bits [31:0] correspond to: 38h = [7:0], 39h = [15:8], 3Ah = [23:16], 3Bh = [31:24].

- Bits [13:0] Frame Remaining (RO) - This 14-bit decrementing counter is used to time a frame. When the HC is in the USB Operational state, the counter decrements each 12MHz clock period. When the count reaches 0, the end of a frame has been reached. The counter reloads with Frame Interval (MEMOFST 34h[13:0]) at that time. In addition, the counter loads when the HC transitions into the USB Operational state.
- Bits [30:14] Reserved
- Bit 31 Frame Remaining Toggle (RO) - This bit is loaded with Frame Interval Toggle (MEMOFST 34h[31]) when Frame Remaining (bits [13:0]) is loaded.

MEMOFST 3Ch-3Fh **HcFmNumber Register** **Default = 00h**

Bits [31:0] correspond to: 3Ch = [7:0], 3Dh = [15:8], 3Eh = [23:16], 3Fh = [31:24].

- Bits [15:0] Frame Number (RO) - This 16-bit incrementing counter is incremented coincident with the load of Frame Remaining (MEMOFST 38h[13:0]). The count will roll over from FFFh to 0h.
- Bits [31:16] Reserved

MEMOFST 40h-43h **HcPeriodicStart Register** **Default = 00h**

Bits [31:0] correspond to: 40h = [7:0], 41h = [15:8], 42h = [23:16], 43h = [31:24].

- Bits [13:0] Periodic Start - These bits are used by the List Processor to determine where in a frame the Periodic List processing must begin.
- Bits [31:14] Reserved

MEMOFST 44h-47h **HcLSThreshold Register** **Default = 00h**

Bits [31:0] correspond to: 44h = [7:0], 45h = [15:8], 46h = [23:16], 47h = [31:24].

- Bits [11:0] LS Threshold - These bits contain a value used by the Frame Management Block to determine whether or not a low speed transaction can be started in the current frame.
- Bits [31:12] Reserved

MEMOFST 48h **HcRhDescriptorA Register - Byte 0 (RO)** **Default = 02h**

Number Downstream Ports - The USB core supports two downstream ports.

7	6	5	4	3	2	1	0
MEMOFST 49h			**HcRhDescriptorA Register - Byte 1**				**Default = 09h**
Reserved			No Over-current Protection:(1) 0 = Over-current status is reported 1 = Over-current status is not reported	Over-current Protection Mode: 0 = Global over-current 1 = Individual Over-Current This bit is only valid when bit 4 is cleared. This bit should be written to 0.	Device Type (RO): The USB core is not a compound device.	No Power Switching:(1) 0 = Ports are powered switched 1 = Ports are always powered on	Power Switching Mode: 0 = Global switching 1 = Individual switching This bit is only valid when bit 1 is cleared. This bit should be written to 0.
(1) Bits 4 and 1 should be written to support the external system port over-current and switching implementations.							
MEMOFST 4Ah			**HcRhDescriptorA Register - Byte 2**				**Default = 00h**
Reserved							
MEMOFST 4Bh			**HcRhDescriptorA Register - Byte 3**				**Default = 01h**
Power-On to Power-Good Time - The USB core power switching is effective within 2ms. The field value is represented as the number of 2ms intervals. This field should be written to support the system implementation. This field should always be written to a non-zero value.							
MEMOFST 4Ch-4Dh			**HcRhDescriptorB Register - Bytes 0 & 1**				**Default = 00h**
Bits [15:0] correspond to: 4Ch = [7:0], 4Dh = [15:8]. - Bit 0 Reserved - Bits [15:1] Device Removable - USB core ports default to removable devices: 0 = Device not removable 1 = Device removable Bit 15 corresponds to Port 15, Bit 14 corresponds to Port 14, the remaining bits follow suit. Unimplemented ports are reserved.							
MEMOFST 4Eh-4Fh			**HcRhDescriptorB Register- Bytes 2 & 3**				**Default = 00h**
Bits [15:0] correspond to: 4Eh = [7:0], 4Fh = [15:8]. - Bit 0 Reserved - Bits [15:1] Port Power Control Mask: Bit 15 corresponds to Port 15, Bit 14 corresponds to Port 14, the remaining bits follow suit. Unimplemented ports are reserved. 0 = Device not removable 1 = Global power mask This field is only valid if No Power Switching bit (MEMOFST 49h[1]) is cleared and Power Switching Mode Bit (MEMOFST 49h[0]) is set (individual port switching). When set, the port only responds to individual port power switching commands (Set/ClearPortPower, MEMOFST 54h[1:0] and 58h[1:0]). When cleared, the port only responds to global power switching commands (Set/ClearGlobalPower, MEMOFST 52h[0] and 50h[0]).							

7	6	5	4	3	2	1	0
MEMOFST 50h			**HcRhStatus Register - Byte 0**				**Default = 00h**
Reserved						Over-current Indicator (RO):(1) Reflects state of OVCR pin. 0 = No over-current condition 1 = Over-current condition	Read: Local Power Status Not supported. Always read 0. Write: Clear Global Power 0 = No effect 1 = Issue Clear Global Power command to ports
(1) Bit 1 is only valid if the No Over-current Protection (MEMOFST 49h[4]) and Over-current Protection Mode (MEMOFST 49h[3]) bits are cleared.							
MEMOFST 51h			**HcRhStatus Register - Byte 1**				**Default = 00h**
Read: Device Remote Wake-up Enable(1) 0 = Disabled 1 = Enabled Write: Set Remote Wake-up Enable 0 = No effect 1 = Sets Device Remote Wakeup Enable	Reserved						
(1) Allows port Connect Status Change Bit (MEMOFST 56h[0] for Port 1 and MEMOFST 59h[0] for Port 2) as a remote wakeup event.							
MEMOFST 52h			**HcRhStatus Register - Byte 2**				**Default = 00h**
Reserved						Over-current Indicator Change This bit is set when the Over-current Indicator bit (MEMOFST 50h[1]) changes. Write 1 to clear	Read: Local Power Status Change Not supported. Always read 0 Write: Set Global Power 0 = No effect 1 = Issue Set Global Power command to ports

7	6	5	4	3	2	1	0
MEMOFST 53h			**HcRhStatus Register - Byte 3**				**Default = 00h**
Clear Remote Wakeup Enable (WO) 0 = No effect 1 = Clear Device Remote Wakeup Enable bit (MEMOFST 51h[7])	Reserved						
MEMOFST 54h			**HcRhPort1Status Register - Byte 0**				**Default = 00h**
Reserved			Read: Port Reset Status 0 = Port reset status signal not active 1 = Port reset signal active Write: Set Port Reset 0 = No effect 1 = Sets Port Reset Status	Read: Port Over-current Indicator(1) 0 = No over-current condition 1 = Over-current condition Write: Clear Port Suspend 0 = No effect 1 = Initiates selective resume sequence for the port	Read: Port Suspend Status 0 = Port is not suspended 1 = Port is selectively suspended Write: Set Port Suspend 0 = No effect 1 = Sets Port Suspend Status	Read: Port Enable Status 0 = Port disabled 1 = Port enabled Write: Set Port Enable 0 = No effect 1 = Sets Port Enable Status	Read: Current Connect Status 0 = No device connected 1 = Device connected.(2) Write: Clear Port Enable 0 = No effect 1 = Clears Port Enable Status bit (bit 1)

(1) The USB core supports global over-current reporting. This bit reflects the state of the OVRCUR pin dedicated to this port. This bit is only valid if the No Over-current Protection (MEMOFST 49h[4]) bit is cleared and Over-current Protection Mode (MEMOFST 49h[3]) bit is set.

(2) If the Device Removable bits (MEMOFST 4Ch[15:0]) are set (not removable), bit 0 is always 1.

MEMOFST 55h			**HcRhPort1Status Register - Byte 1**				**Default = 00h**
Reserved						Read: Low Speed Device Attached(1) 0 = Full speed device 1 = Low speed device Write: Clear Port Power 0 = No effect 1 = Clears Port Power Status (bit 0)	Read: Port Power Status(2) 0 = Port power is off 1 = Port power is on Write: Set Port Power 0 = No effect 1 = Sets Port Power Status

(1) Bit 1 defines the speed (and bus idle) of the attached device. It is only valid when Current Connect Status (MEMOFST 54h[0]) bit is set.

(2) Bit 0 reflects the power state of the port regardless of the power switching mode. If the No Power Switching (MEMOFST 49h[1]) bit is set, bit 0 is always read as 1.

7	6	5	4	3	2	1	0
MEMOFST 56h			**HcRhPort1Status Register - Byte 2**				**Default = 00h**
Reserved			Port Reset Status Change 0 = Port reset is not complete 1 = Port reset is complete	Port Over-current Indicator Change This bit is set when the Over-current Indicator (MEMOFST 50h[1]) bit changes. Write 1 to clear	Port Suspend Status Change Indicates the completion of the selective resume sequence for the port. 0 = Port is not resumed 1 = Port resume is complete	Port Enable Status Change Indicates that the port has been disabled due to a hardware event (cleared Port Enable Status, MEMOFST 54h[1]). 0 = Port has not been disabled 1 = Port Enable Status has been cleared	Connect Status Change Indicates a connect or disconnect event has been detected. 0 = No connect/disconnect event 1 = Hardware detection of connect/disconnect event(1) Write 1 to clear
(1) If the Device Removable Bits (MEMOFST 4Ch[15:1]) are set, bit 0 resets to 1.							
MEMOFST 57h			**HcRhPort1Status Register - Byte 3**				**Default = 00h**
Reserved							
MEMOFST 58h			**HcRhPort2Status Register - Byte 0**				**Default = 00h**
Reserved			Read: Port Reset Status 0 = Port reset status signal not active 1 = Port reset signal active Write: Set Port Reset 0 = No effect 1 = Sets Port Reset Status	Read: Port Over-current Indicator(1) 0 = No over-current condition 1 = Over-current condition Write: Clear Port Suspend 0 = No effect 1 = Initiates selective resume sequence for the port	Read: Port Suspend Status 0 = Port is not suspended 1 = Port is selectively suspended Write: Set Port Suspend 0 = No effect 1 = Sets Port Suspend Status	Read: Port Enable Status 0 = Port disabled 1 = Port enabled Write: Set Port Enable 0 = No effect 1 = Sets Port Enable Status	Read: Current Connect Status 0 = No device connected 1 = Device connected.(2) Write: Clear Port Enable 0 = No effect 1 = Clears Port Enable Status bit (bit 1)
(1) The USB core supports global over-current reporting. This bit reflects the state of the OVRCUR pin dedicated to this port. This bit is only valid if the No Over-current Protection (MEMOFST 49h[4]) bit is cleared and Over-current Protection Mode (MEMOFST 49h[3]) bit is set. (2) If the Device Removable bits (MEMOFST 4Ch[15:0]) are set (not removable), bit 0 is always 1.							

7	6	5	4	3	2	1	0
MEMOFST 59h			**HcRhPort2Status Register - Byte 1**				**Default = 00h**
Reserved						Read: Low Speed Device Attached(1) 0 = Full speed device 1 = Low speed device Write: Clear Port Power 0 = No effect 1 = Clears Port Power Status (bit 0)	Read: Port Power Status(2) 0 = Port power is off 1 = Port power is on Write: Set Port Power 0 = No effect 1 = Sets Port Power Status
(1) Bit 1 defines the speed (and bus idle) of the attached device. It is only valid when Current Connect Status (MEMOFST 54h[0]) bit is set. (2) Bit 0 reflects the power state of the port regardless of the power switching mode. If the No Power Switching (MEMOFST 49h[1]) bit is set, bit 0 is always read as 1.							
MEMOFST 5Ah			**HcRhPort2Status Register - Byte 2**				**Default = 00h**
Reserved			Port Reset Status Change 0 = Port reset is not complete 1 = Port reset is complete	Port Over-current Indicator Change This bit is set when the Over-current Indicator (MEMOFST 50h[1]) bit changes. Write 1 to clear	Port Suspend Status Change Indicates the completion of the selective resume sequence for the port. 0 = Port is not resumed 1 = Port resume is complete	Port Enable Status Change Indicates that the port has been disabled due to a hardware event (cleared Port Enable Status, MEMOFST 54h[1]). 0 = Port has not been disabled 1 = Port Enable Status has been cleared	Connect Status Change Indicates a connect or disconnect event has been detected. 0 = No connect/disconnect event 1 = Hardware detection of connect/disconnect event(1) Write 1 to clear
(1) If the Device Removable Bits (MEMOFST 4Ch[15:1]) are set, bit 0 resets to 1.							
MEMOFST 5Bh			**HcRhPort2 Status Register - Byte 3**				**Default = 00h**
Reserved							

4.2.2 Legacy Support Registers

Four registers are provided for legacy support:

1. HceControl
- - Used to enable and control the emulation hardware and report various status information.

2. HceInput
- - Emulation side of the legacy Input Buffer register.

3. HceOutput
- - Emulation side of the legacy Output Buffer register where keyboard and mouse data is to be written by software.

4. HceStatus
- - Emulation side of the legacy Status register.

These registers are located in the Host Controller Register Space; from MEMOFST 100h through 10Fh. The bit formats for these registers are described below.

Refer to "Legacy Support" section for information when accessing these registers when emulation is enabled.

4.2.3 MEMOFST 100h-1Fh (Legacy Support Registers)

7	6	5	4	3	2	1	0
MEMOFST 100h			**HceControl Register - Byte 0**				**Default = 00h**
IRQ12 Active Indicates that a positive transition of IRQ12 from kybrd controller has occurred. Writing a 1 clears this bit, while writing a 0 leaves it unchanged.	IRQ1 Active Indicates that a positive transition of IRQ1 from kybrd controller has occurred. Writing a 1 clears this bit, while writing a 0 leaves it unchanged.	GateA20 Sequence Set by HC when a data value of D1h is written to Port 64h. Cleared by HC on write to Port 64h of any value other than D1h.	External IRQEn IRQ1 and IRQ12 from kybrd controller causes emulation interrupt: 0 = Disable 1 = Enable This bit is independent of the Emulation Enable bit (bit 0) setting.	IRQEn If the Output Full bit (MEMOFST 10Ch[0]) = 1, HC generates IRQ1 or IRQ12. If the Aux Output Full bit (MEMOFST 10Ch[5]) = 0, HC generates IRQ1; if = 1, HC generates IRQ12. 0 = Disable 1 = Enable	Character Pending HC generates emulation interrupt when the Output Full bit (MEMOFST 10Ch[0]) = 0. 0 = Disable 1 = Enable	Emulation Interrupt (RO) A static decode of the emulation interrupt condition.	Emulation Enable HC is enabled for legacy emulation? 0 = No 1 = Yes(1)
(1) The HC decodes accesses to Ports 60h/64h and generates IRQ1 and/or IRQ12 when appropriate. Additionally, the HC generates an emulation interrupt at appropriate times to invoke the emulation software.							
MEMOFST 101h			**HceControl Register - Byte 1**				**Default = 00h**
Reserved							A20 State: Indicates current state of Gate A20 on kybrd controller. Used to compare against value written to Port 60h when GateA20 Sequence is active.

7	6	5	4	3	2	1	0

MEMOFST 102h-103h — **HceControl Register - Bytes 2 & 3** — **Default = 00h**

Reserved

MEMOFST 104h — **HceInput Register - Bytes 0** — **Default = 00h**

Input Data:

- I/O data that is written to Ports 60h and 64h is captured in this register.

Note: Refer to "Emulated Registers and Side Effects" if emulation is enabled.

MEMOFST 105h-107h — **HceInput Register - Bytes 1-3** — **Default = 00h**

Reserved

MEMOFST 108h — **HceOutput Register - Bytes 0** — **Default = 00h**

Output Data:

- This register hosts data that is returned when an I/O read of Port 60h is performed by application software.

Note: Refer to "Emulated Registers and Side Effects" if emulation is enabled.

MEMOFST 109h-10Bh — **HceOutput Register - Bytes 1-3** — **Default = 00h**

Reserved

MEMOFST 10Ch — **HceStatus Register - Byte 0** — **Default = 00h**

Parity	Time-out	Aux Output Full	Inhibit Switch	Cmd Data	Flag	Input Full	Output Full
Indicates parity error on keyboard/mouse data.	Used to indicate a time-out	Assert IRQ12 if Output Full bit (MEMOFST 10Ch[0]) = 1 and IRQEn bit (MEMOFST 100h[3]) = 1? 0 = No 1 = Yes	Reflects state of the keyboard inhibit switch: 0 = Inhibited 1 = Not inhibited	HC sets this bit on I/O writes to Ports 60h and 64h: 0 = Port 60h 1 = Port 64h	Nominally used as a system flag by software to indicate a warm or cold boot.	HC sets this bit to 1 on an I/O write to Port 60h or 64h except for the case of a GateA20 Sequence. While set to 1 and emulation is enabled (MEMOFST 100h[0] = 1), an emulation interrupt condition exists.	HC sets this bit to 0 on a read of Port 60h. While this bit is 0 and the Character Pending bit (MEMOFST 100h[2]) = 1, an emulation interrupt condition exists. Setting this bit to 1 will generate either IRQ1 or IRQ12 under certain conditions(1).

(1) If the IRQEn bit (MEMOFST 100h[3]) = 1 and Aux Output Full bit (MEMOFST 10Ch[5]) = 0: IRQ1 is generated.
If the IRQEn bit (MEMOFST 100h[3]) = 1 and Aux Output Full bit (MEMOFST 10Ch[5]) = 1: IRQ12 is generated.

Note: Refer to "Emulated Registers and Side Effects if emulation is enabled.

MEMOFST 10Dh-10Fh — **HceStatus Register - Bytes 1-3** — **Default = 00h**

Reserved

5.0 Electrical Ratings

Stresses above those listed in the following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied.

5.1 Absolute Maximum Ratings

Symbol	Parameter	5.0 Volt		3.3 Volt		Unit
		Min	Max	Min	Max	
V_{CC}	Supply Voltage	not allowed	not allowed		+4.0	V
V_I	Input Voltage	–0.5	V_{CC} + 0.5	–0.5	V_{CC} + 0.5	V
V_O	Output Voltage	–0.5	V_{CC} + 0.5	–0.5	V_{CC} + 0.5	V
T_{OP}	Operating Temperature	0	+70	0	+70	degrees C
T_{STG}	Storage Temperature	–40	+125	–40	+125	degrees C

5.2 DC Characteristics:

V_{CC} = 3.3V ±5%, T_A = 0C to +70C

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input low Voltage	–0.5	+0.8	V	
V_{IH}	Input high Voltage	+2.0	+5.5	V	
V_{OL}	Output low Voltage		+0.4	V	I_{OL} = 4.0mA
V_{OH}	Output high Voltage	+2.4		V	I_{OH} = –1.6mA
I_{IL}	Input Leakage Current		+10.0	µA	V_{IN} = V_{CC}
I_{OZ}	Tristate Leakage Current		+10.0	µA	
C_{IN}	Input Capacitance		+10.0	pF	
C_{OUT}	Output Capacitance		+10.0	pF	
I_{CC}	Power Supply Current: 3.3V Core	50mA max during operation, 1mA max during Standby (all clocks stopped)			

5.3 AC Characteristics (Preliminary)

5.3.1 PCI Bus AC Timings

Sym	Parameter	Min	Max	Unit	Figure
t100	C/BE[3:0]#, AD[31:0], FRAME#, IRDY#, TRDY#, STOP#, DEVSEL#, LOCK#, PAR, SERR#, PERR# setup time to PCICLK rising	7		ns	4
t101	C/BE[3:0]#, AD[31:0], FRAME#, IRDY#, TRDY#, STOP#, DEVSEL#, LOCK#, PAR, SERR#, PERR# hold time from PCICLK rising	0		ns	5
t102	C/BE[3:0]#, AD[31:0], FRAME#, IRDY#, TRDY#, STOP#, DEVSEL#, LOCK#, PAR, SERR#, PERR# valid delay from PCICLK rising	2	11	ns	6
t103	REQ# setup time to PCICLK rising	12		ns	4
t104	REQ# hold time from PCICLK rising	0		ns	5
t105	GNT# valid delay from PCICLK rising	2	12	ns	6

Figure 4. Setup Timing Waveform

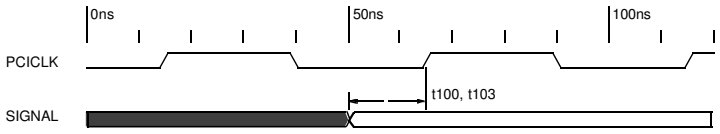


Figure 5. Hold Timing Waveform

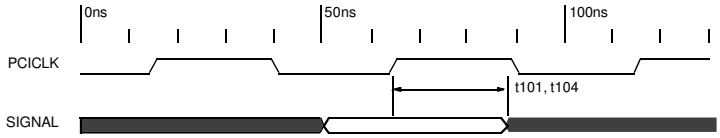
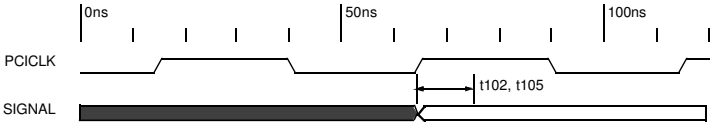


Figure 6. Output Delay Timing Waveform



5.3.2 USB AC Timings: Full Speed Source

Sym	Parameter	Min	Max	Unit	Figure	Condition (Notes 1, 2, and 3)
Driver Characteristics						
	Transition Time:					CL = 50pF, Notes 5 and 6
tR	Rise Time	4	20	ns		
tF	Fall Time	4	20	ns		
tRFM	Rise/Fall Time Matching	90	110	%		(tR/tF)
vCRS	Output Signal Crossover Voltage	1.3	2.0	V		
zDRV	Driver Output Resistance	28	43	ohm		Steady state drive
Data Source Timings						
tDRATE	Full Speed Data Rate	11.97	12.03	Mbps		Average bit rate = 12Mbps ±0.25%
tFRAME	Frame Interval	0.9995	1.0005	ms		1.0ms ±0.05%
	Source Differential Driver Jitter:					Notes 7 and 8
tDJ1	To Next Transition	–3.5	3.5	ns		
tDJ2	For Paired Transitions	–4.0	4.0	ns		
tEOPT	Source EOP Width	160	175	ns		Note 8
tDEOP	Differential to EOP Transition Skew	–2	5	ns		Note 8
	Receiver Data Jitter Tolerance:					Note 8
tJR1	To Next Transition	–18.5	18.5	ns		
tJR2	For Paired Transitions	–9	9	ns		
	EOP Width at Receiver:					Note 8
tEOPR1	Must Reject at EOP	40		ns		
tEOPR2	Must Accept as EOP	82		ns		

5.3.3 USB AC Timings: Low Speed Source

Sym	Parameter	Min	Max	Unit	Figure	Condition (Notes 1, 2, and 4)
Driver Characteristics						
	Transition Time:					Notes 5 and 6
tR	Rise Time	75	300	ns		Min# measured with: CL = 50pF
tF	Fall Time	75	300	ns		Max# measured with: CL = 350pF
tRFM	Rise/Fall Time Matching	80	120	%		(tR/tF)
vCRS	Output Signal Crossover Voltage	1.3	2.0	V		
Data Source Timings						
tDRATE	Low Speed Data Rate	1.4775	1.5225	Mbps		Average bit rate = 1.5Mbps ±1.5%
	Source Differential Driver Jitter, At Host (Downstream):				7	Notes 7 and 8
tDDJ1	To Next Transition	–75	75	ns		
tDDJ2	For Paired Transitions	–45	45	ns		
	Source Differential Driver Jitter, At Function (Upstream):				7	Notes 7 and 8
tUDJ1	To Next Transition	–95	95	ns		
tUDJ2	For Paired Transitions	–150	150	ns		
tEOPT	Source EOP Width	1.25	150	µs	8	Note 8
tDEOP	Differential to EOP Transition Skew	–40	100	ns	8	Note 8
	Receiver Data Jitter Tolerance, At Host (Upstream):				9	
tUJR1	To Next Transition	–152	152	ns		
tUJR2	For Paired Transitions	–200	200	ns		
	Receiver Data Jitter Tolerance, At Function (Downstream):				9	
tDJR1	To Next Transition	–75	75	ns		
tDJR2	For Paired Transitions	–45	45	ns		
	EOP Width at Receiver:				9	Note 8
tEOPR1	Must Reject at EOP	330		ns		
tEOPR2	Must Accept as EOP	675		ns		

Notes:
1. All voltages measured from the local ground potential, unless otherwise specified.
2. All timings use a capacitive load (CL) to ground of 50pF, unless otherwise specified.
3. Full speed timings have a 1.5 kohm pull-up to 2.8V on the D+ data line.
4. Low speed timings have a 1.5 kohm pull-up to 2.8V on the D– line.
5. Measured from 10% to 90% of the data signal.
6. The rising and falling edges should be smoothly transitioning (monotonic).
7. Timing difference between the differential data signals.
8. Measured at crossover point of differential data signals.
9. The maximum load specification is the maximum effective capacitive load allowed that meets the target hub Vbus droop of 330mV.

Figure 7. Differential Data Jitter

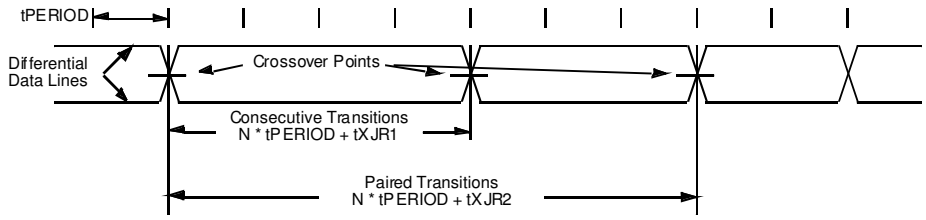


Figure 8. Differential to EOP Transition Skew and EOP Width

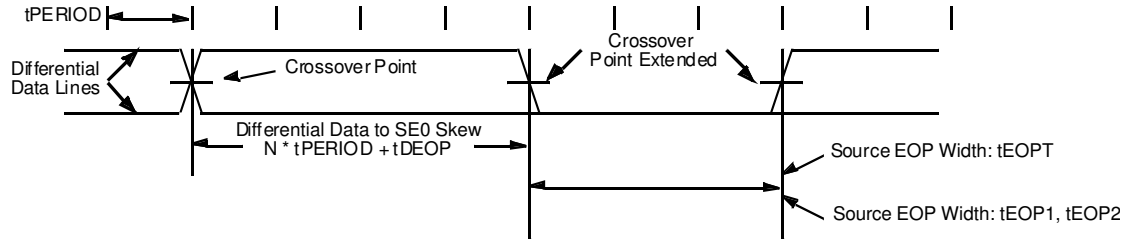
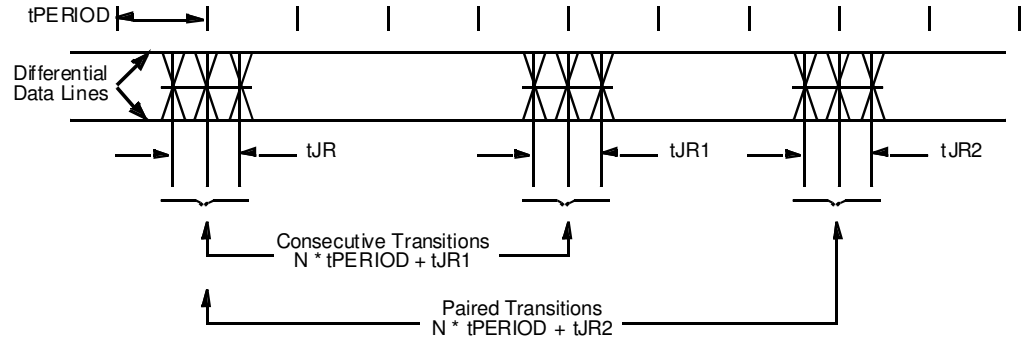


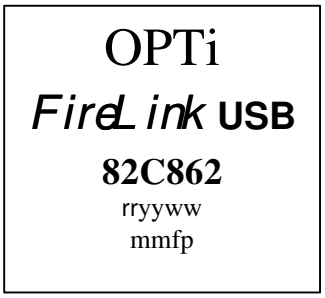
Figure 9. Receiver Jitter Tolerance



6.0 Marking and Order Information

6.1 Package Marking

82C862. Specific marking for the production 82C862 silicon, LQFP package, is as follows (not to scale):

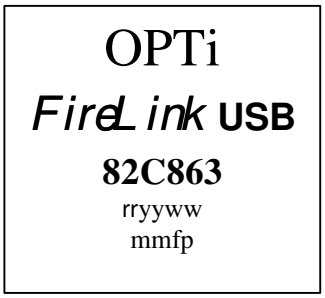


(generic)

(1st prod. rev.)

(2nd prod. rev.)

82C863. Specific marking for the production 82C863 silicon, LQFP package, is as follows (not to scale):



(generic)

(1st prod. rev.)

(2nd prod. rev.)

For both products:
– rr indicates OPTi netlist revision
– yy indicates the year of production
– ww indicates the week of production (1-52)
– mm indicates foundry mask revision
– f indicates the foundry (M identifies the foundry as WSMC, now part of TSMC; U identifies the foundry as UMC)
– p indicates the packaging house (E identifies the assembly house as ASE).

6.2 Order Number and Shipping Box Information

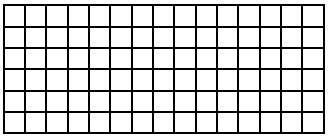
Specific marking for the box in which the 82C862/3 silicon is shipped is as follows:

QT0086202XME-002 – Identifies that the box contains **82C862** LQFP packaged parts. The -002 marking indicates a normal production run; initial production parts meeting the same stringent requirements are marked -999. 02XME indicates the same as the 02ME on the chip marking; the "X" indicates no particular speed grading.
2nd revision: QT0086203XUE-002 – same product, but re-engineered for UMC foundry.

QT0086302XME-002 – Identifies that the box contains **82C863** LQFP packaged parts. The -002 marking indicates a normal production run; initial production parts meeting the same stringent requirements are marked -999. 02XME indicates the same as the 02ME on the chip marking; the "X" indicates no particular speed grading.
2nd revision: QT0086303XUE-002 – same product, but re-engineered for UMC foundry.

These are also the numbers used to order parts from OPTi.

Packing Options. All packing is done in trays only (tape and reel are not available). Trays measure 13.5mm x 32.2mm for LQFP. Tray organization: 90 parts per tray (configured as shown below); 10 trays per box.



Baking method: 125°C for 12 hours.

6.3 Package Specifications

Package Thermal Specifications. For LQFP package, worst-case values are as follows:

– θ_{JA} = 40 °C/W at no air flow

– θ_{JC} = 5 °C/W

– Max power output = 1.5W at 25 °C.

Packaging Details.

– LEAD FRAME: C7025 (Cu)

– SOLDER: Sn/Pb = 85/15

– WIRE BOND: Gold Wire (99.99% Au)

– Resistance to flow, spot, or IR reflow soldering heat: 255°C for 5s max.

– EPOXY: ABLESTIK 8361H

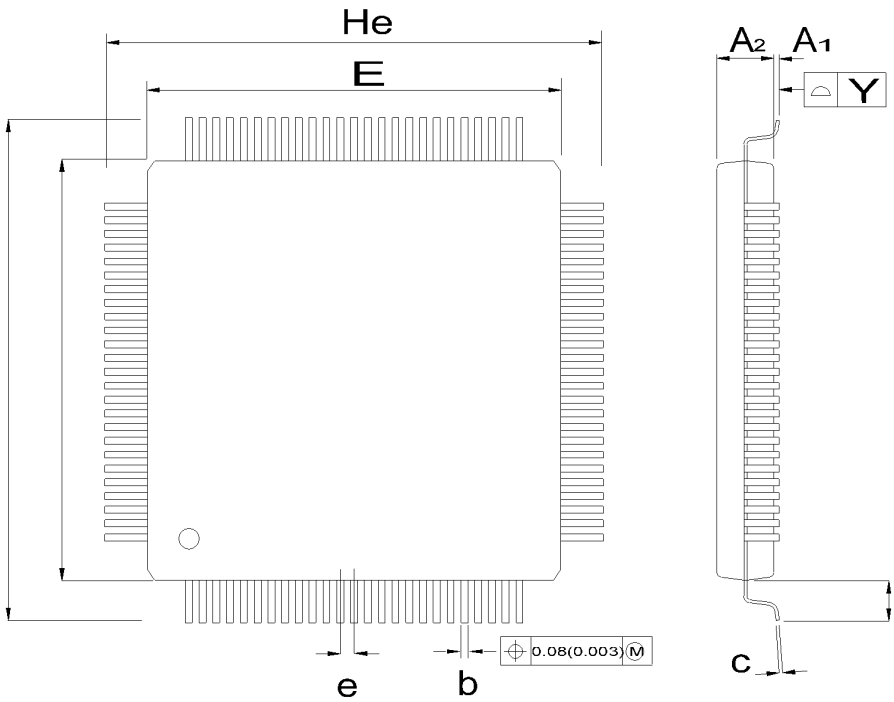
– MOLDING COMPOUND: Sumitomo EME-7320A(R)

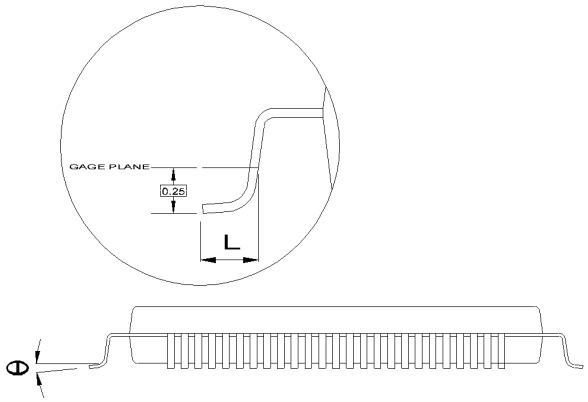
Environmental Details.

– Electrostatic Discharge (ESD) Tolerance: 2000V

7.0 Mechanical Package Outlines

Figure 10. 100-Pin Low-Profile Quad Flat Pack (LQFP)





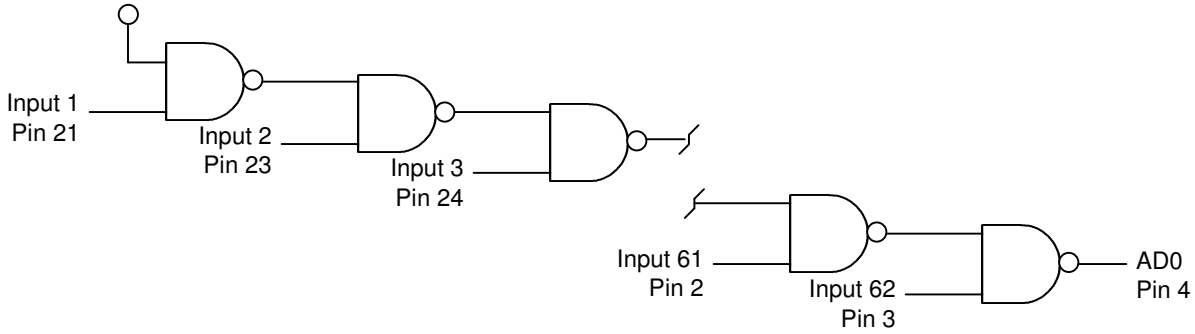
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A_1	0.05	0.10	0.15	0.002	0.004	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.090		0.200	0.004		0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	13.90	14.00	14.10	0.547	0.551	0.555
e		0.50			0.020	
Hd	15.90	16.00	16.10	0.626	0.630	0.634
He	15.90	16.00	16.10	0.626	0.630	0.634
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1		1.00			0.039	
Y			0.08			0.003
θ	0		7	0		7

Dwg. No.:	AS100TQFP-001	
Dwg. Rev.:	A0	Unit: MM / INCH

8.0 NAND Tree Test Mode

The NAND Tree test mode is a convenient method of testing all digital signal pins on the chip for connectivity. By sequentially inverting each input and observing the output, proper connections are assured. The logic structure is shown in Figure 11.

Figure 11. NAND Tree Logic



The NAND tree mode tests both input and bi-directional pins that are part of the NAND tree chain. The NAND tree chain starts at pin 21 (TEST0) while the output of the chain is at pin 4 (AD0). RESET# and PCICLK# are not included in the NAND tree chain.

To enable the NAND tree test mode, strap FireLink USB by pulling up the following pins during the rising edge of RESET#: Pin 25 (TEST1) and Pin 21 (TEST0). For reliable strapping, toggle PCICLK at least two times after RESET# goes low, and at least two times after RESET# goes high. After that strapping sequence, set both RESET# and PCICLK high. Do not toggle RESET# and PCICLK during the NAND tree test.

Testing involves the following steps.

1. Drive all signal inputs initially high.
2. Note the signal state on the AD0 pin (pin 4).
3. Drive the first NAND tree signal input pin (pin 21) low.
4. The signal state on the OUT pin will invert.
5. Drive the next input pin in the sequence (pin 23) low.
6. The signal state on the OUT pin will again invert.
7. Continue this sequence until reaching the final pin (pin 3), ensuring that the AD0 pin toggles each time.