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DP8344 Data Sheet Reference

Introduction

This document supplements the current revision of the data sheet. It is provided as an aid to the design engineer in understanding the status of the data sheet, plans for future data sheet releases, and how the information provided relates to the current revision of the product.

The product currently being shipped is marked DP8344V (sometimes referred to as rev. A2). A revision of this product is planned, to be marked DP8344AV (previously referred to as rev. B). Since the 'V' suffix on the part number is a package designation, signifying that the product is packaged in a plastic leaded chip carrier (PLCC) and does not hold any relevance to the functionality of the product, this suffix is not used either in the data sheet or in this reference document. All references to DP8344 therefore refer to the product currently available (rev. A2) and all references to DP8344A refer to the planned new revision (rev. B).

The DP8344 does not function exactly as indicated in the current revision of the data sheet. This is because some "bugs" still exist which must be worked around, and some features listed in the data sheet are not yet available. The DP8344A will fix all known bugs and provide some additional features.

The data sheet reflects the functionality of the DP8344A. Those items which are not available on the DP8344, due to bugs or new features not yet implemented, are listed in this document. Recommended work-arounds to minimize the effect of bugs, are provided wherever possible.

The DP8344A compatibility guide is also included. This provides guidance on the design of systems and the preparation of software using the DP8344 to minimize any compatibility problems between the two revisions of silicon.

The DP8344 is now available as a full production product. This product is capable of being used in a wide range of applications; all bugs can be efficiently coded around. No additional hardware is required.

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DP8344 Bug List

The items listed below comprise all problems known at this time for the DP8344.

- Instruction address generation may not operate correctly at the desired maximum CPU clock speed of 20 MHz. Correct operation has, however, been verified at 10 MHz (CPU clock set to CLK/2 using a 20 MHz crystal), over the full temperature and supply voltage range of 0 - 70 °C, 5 V ± 10%.

- The LCALL Rs, p, s, nn instruction (formerly CALLB Rs, s, p, n) is not available.

- The interrupt circuitry will not operate correctly when single stepping.

- The Non-Maskable Interrupt (NMI) is not available when any other interrupt is unmasked. It does, however, operate correctly if no other interrupts are used concurrently.

- In 5250 modes, the receiver will flag a loss of mid-bit error if a transition is seen on the selected input within 3 µsec after the last valid fill bit. This will inhibit the Line Turn Around (LTA) interrupt. It is suggested that software be used to determine the end of the message and then reset the transceiver to clear any erroneous loss of mid-bit transition errors.

- In the non-promiscuous 5250 mode, the receiver will continue to monitor all frames of the message for errors even if there was not a valid address match. It is suggested that the promiscuous mode, with a software address comparison, be used in place of the non-promiscuous mode.

- The Global Interrupt Enable [GIE], bit 0 in the Auxiliary Control Register {ACR}, may not be cleared by writing to {ACR} if an interrupt occurs during that instruction. It is suggested that the EXX instruction with the clear [GIE] option be used instead. If the present banks are selected in the EXX instruction, its only affect will be that of clearing [GIE]. Alternatively, if the Non Maskable Interrupt (NMI) is not being used, [GIE] can be cleared by first masking all interrupts via the Interrupt Control Register {ICR} and then writing to [GIE].

- The value of the Remote Interface Configuration Register {RIC} will be incorrect when read by a remote processor if the remote access causes a BCP data memory access to be waited.

- The output $\overline{\text{LCL}}$ may go high one T-state early when the remote processor's access is waited by a BCP data memory access (a local access).

- The Transmit FIFO Full flag [TFF], bit 7 in the Transceiver Status Register {TSR}, is not available. It is suggested that the Transmit FIFO Empty flag [TFE], bit 7 in the Network Command Flag Register {NCF}, or the TFE interrupt be used instead. Note, however, that less than one frame time is available to reload the transmitter FIFO to continue a multi-byte transmission after the [TFE] flag is set or the TFE interrupt occurs.

- The number of instruction wait states of the instruction currently being executed by the BCP may be as much as doubled by a remote access of the Remote Interface Control Register {RIC} if at the time bit 0 of {RIC} was a "1". If no instruction wait states are used, the problem does not occur.

- The transmitter does not generate pre-emphasis on the first half bit of the first of the five line quiesces unless the Transmitter Serial Data Output Invert [TIN] bit is set and it is the first transmission after the transceiver was reset.

- ICLK will be asserted on either the third or fourth rising edge of the signal driving X1 after starting the BCP following a reset. This may cause problems with automated testing operations. There will be no effect in normal applications.

DP8344A Features not available in DP8344

The items listed below are features to be provided by the DP8344A that are not available in the DP8344. The data sheet provides a detailed description of how these features work.

- Line Turn Around flag [LTA], bit 4 in the Network Command Flag Register {NCF}.
- Data Error or End of Message flag [DEME], bit 3 in the Network Command Flag Register {NCF}.
- Receive Line Quiesce [RLQ] bit, bit 7 in the Transceiver Control Register {TCR}. The DP8344 receiver is hard-wired to require a minimum of three line quiesce pulses to recognize the beginning of a message.
- The transmitter line hold function, selected by bits 3-7 in the Auxiliary Transceiver Register {ATR} (formerly {NAR}). In 5250 modes, the DP8344 transmitter de-asserts TX-ACT after the last fill bit at the end of a message.
- The option to clear the Line Turn Around flag [LTA], bit 4 in the Network Command Flag Register {NCF}, or the Line Turn Around interrupt, LTA, by writing a "1" to bit 4 in the {NCF} register. In the DP8344, the LTA interrupt is cleared by asserting transceiver reset [TRES], bit 7 of the Transceiver Mode Register {TMR}, or by loading the transmitter FIFO. The [LTA] flag is not available in the DP8344.
- The CLK-OUT Disable bit [COD], bit 2 in the Auxiliary Control Register {ACR}.
- The Advance Transmitter Active [ATA] function, controlled by bit 4 in the Transceiver Control Register {TCR}. In the DP8344, this bit is designated Delay Transmitter Active [DTA]. Setting this bit delays the transmitter active signal, TX-ACT, one half bit time instead of advancing it. Therefore, the transmitter sends 4-1/2 line quiesce pulses instead of the intended 5-1/2. In the DP8344A, setting [ATA] advances TX-ACT one half bit time.

DP8344A Compatibility Guide

The DP8344A will correct all bugs on the DP8344, and provide some additional features to enhance the flexibility and ease of use of the BCP. Because of this, some care must be taken when designing a system with the DP8344 to ensure that it will function the same with the DP8344A. This section addresses those hardware and software issues.

First a general statement: Whenever possible, keep all reserved bits low at all times, except where indicated below.

New Control bits:

On the DP8344A, some of the bits in the special function registers have been re-defined or new ones added. If these bits are read only, they should not be used when designing with the DP8344. If they are writable, then care must be taken to avoid writing arbitrary values to these bits because it will have an effect on the operation of the DP8344A. A list of the bits and their suggested treatment is as follows:

- **[LTA]** Bit 4 in {NCF} will be changed from Receiver Active [RA] to Line Turn Around [LTA]. {NCF} is read only on the DP8344, but [LTA] will be reset if a "1" is written to it on the DP8344A. Therefore, when using the DP8344, do not use bit 4 of {NCF} as the [RA] flag (use bit 4 of {TSR} instead), and do not write to {NCF}.

- **[DEME]** Bit 3 in {NCF} will be changed from Address Match [ADM] to Data Error or End of Message [DEME]. Both [ADM] and [DEME] are read only. Therefore, to ensure compatibility, do not use bit 3 of {NCF}.

- **[RLQ]** Bit 7 in {TCR} is reserved on the DP8344. It will be Receive Line Quiesce [RLQ] on the DP8344A. This bit, when cleared, will cause the receiver to only require two line quiesces at the beginning of a message instead of three as on the DP8344. Therefore, this bit must be set when writing code for the DP8344 if the DP8344A receiver is to operate identically.

- **{ATR}** Bits 3-7 of {NAR} are don't cares in 5250 mode on the DP8344. On the DP8344A these bits will control the time TX-ACT stays asserted after the last fill bit in 5250 mode. This is an additional function for this register, bits 0-2 retain their DP8344 functionality and there are no changes to the functionality of the other bits other than in 5250 modes. If you want the DP8344A to operate identically to the DP8344 in 5250 mode, you must write a zero to bits 3-7 in the {NAR} register before transmitting. The name of this register is being changed from Network Address Register {NAR} to Auxiliary Transceiver Register {ATR} on the DP8344A to reflect this additional function.

- **[ATA]** Bit 4 of {TCR} will be changed from Delay Transmitter Active [DTA] on the DP8344 to Advance Transmitter Active [ATA] on the DP8344A. If this bit is set on the DP8344, the transmitter will generate 4-1/2 line quiesces. If it is set on the DP8344A the transmitter will generate 5-1/2 line quiesces, and therefore add one bit time to the starting sequence operation. If the bit is not set the transmitter will generate 5 line quiesces on both the DP8344 and the DP8344A. Therefore, to ensure compatibility this bit should not be set.

- **[COD]** Bit 2 of {ACR} is reserved on the DP8344. It will be CLK-OUT Disable [COD] on the DP8344A and, if set, will put the CLK-OUT output into TRI-STATE. Therefore, to ensure compatibility between the DP8344 and the DP8344A, do not write a "1" to this bit.

DP8344A Compatibility Guide (continued)

Processor Hardware Modifications

There are three subtle hardware differences between the DP8344 and the DP8344A that the user should be aware of and plan for accordingly.

- **CLK-OUT:** The CLK-OUT output drive will be reduced from 4 mA to 1 mA. Therefore, depending on the fan out required, this output may need to be externally buffered.

- **$\overline{\text{LCL}}$:** On the DP8344, this output goes high one T-state early if the remote processor is waited by a the BCP data memory access. This will cause $\overline{\text{LCL}}$ to go high at approximately the same time as the the BCP's $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ strobes are de-asserted, eliminating a one T-state pad before the remote processor comes on the bus. This will not happen on the DP8344A. The interface circuitry must be able to handle either case.

- **ICLK:** On the DP8344, ICLK will be asserted on either the third or fourth rising edge of the signal driving X1, after starting the the BCP following a reset. A change will be made on the DP8344A to ensure that ICLK is always asserted on the fourth rising edge of the signal driving X1, after starting the the BCP following RESET being de-asserted for the second time, i.e. RESET must be pulsed low twice. This is to simplify automated testing, it will have no effect on normal operation.

Transceiver Hardware Modifications

The major definition change between the DP8344A and the DP8344 is related to how the BCP's transmitter and receiver operate in the 5250 protocol.

- **Transmitter Output Pre-emphasis:** On the DP8344, the first line quiesce pulse sent at the beginning of a message does not have pre-emphasis on the first half bit in all modes. For the transmitter to generate pre-emphasis on the first half bit [TIN] must be asserted and the transceiver must have been reset prior to each transmission. In the DP8344A, with [TIN] either asserted or de-asserted, regardless of whether the transceiver was reset prior to the transmission or not, the transmitter will always generate pre-emphasis on the first half bit of the five line quiesce pulses.

- **TX-ACT Extension:** The DP8344A will have the ability to extend TX-ACT from 0 to 15.5 µs after the last fill bit. This can be used to continue driving one of the twinax phases after transmitting a message to suppress ringing and reflections on the twinax cable. Because the DP8344 does not support this feature, bits 3-7 of {NAR} (now called {ATR}) should be set to zero to ensure identical operation between the DP8344 and the DP8344A.

- **5250 End of Message:** The manner in which the receiver detects the end of a message in the 5250 mode will be changed. On the DP8344, the receiver flags a loss of mid-bit error if a transition due to noise or reflections is seen on the selected input less than 3 µs after the last fill bit. This inhibits the Line Turn Around [LTA] interrupt. It is suggested that the user determine the end of the message and then reset the transceiver to clear any erroneous loss of mid-bit errors. This can be done in software by checking to see that the Data Available [DAV] flag is de-asserted after the error is cleared, by decoding the message to determine that another frame is not expected, and then by checking to see that the Line Active [LA] flag is de-asserted 2 µs later. In the DP8344A, when a loss of synchronization is detected, i.e. a loss of mid-bit transition, during the fill bits, the receiver will not recognize an error unless transitions on the line continue for more that 11 µs or resemble a valid sync bit of a multi-frame transmission. If transitions are still seen after 11 µs, or a valid sync bit is detected without a complete frame, the loss of mid-bit error [LMBT] will be asserted. If transitions of the line are not seen for at least 2 µs in the 11 µs window, the receiver will reset and assert [LTA]. To be compatible between DP8344 and DP8344A, the suggested DP8344 software work-around should be used.

Upcoming Data Sheet Releases

The schedule for future releases of the data sheet is as follows:

Rev.	Date Available	Contents	Comments
3.7	Now	Pinout Electrical Spec. Instruction Set CPU Registers Remote Interface Transceiver	Production Release data sheet with full electrical specification. General outline description (front sheet), Pinout, Transceiver, Remote Interface, Instruction Set sections now complete and in their final form. CPU registers in outline form.
3.8	5/31/88	Pinout Electrical Spec. Instruction Set CPU Registers Remote Interface Transceiver	Will include a full description of the CPU functionality, incorporating the CPU Register Section.

The information provided in the comments column is the minimum planned for that revision of the data sheet. More information may be provided if available at publication.

IBM Documentation List

To aid in the design of products for the IBM 3270 and 5250 environments, additional documentation is available from IBM. To obtain this information contact your local IBM Marketing Representative or write to:

IBM Industry Relations Department
2000 Purchase Street
Purchase, NY 10577
Phone: (914)697-7227

Following is a list of suggested documents:

- **3270 Coax Literature:**

  1. Introduction to the IBM 3270 Information Display System (GA27-2739-21)
  2. IBM 3174/3274 Control Unit to Device Product Attachment Information (Oct. 16, 1986 or later)
  3. IBM 3274 Control Unit to Distributed Function Device Product Attachment Information (June 1985 or later)

- **5250 Twinax Literature:**

  1. IBM 5250 Information Display System Planning and Site Preparation Guide (GA21-9337-7)
  2. 5250 Information Display System to System/36 and System/38 System Units Product Attachment Information (November 1986 or later)
  3. System/36 Internals (G-360-1009)

- **SNA Literature:**

  1. Systems Network Architecture Concepts and Products (GC30-3072-1)
  2. An Introduction to Advanced Program-to-Program Communication (APPC) (GG24-1584-01)

- **General Literature:**

  1. IBM Cabling System Planning and Installation Guide (GA27-3361-6)