## LS/S/TTL Logic

## Databook

## LS/S/TTL <br> Logic <br> Databook

1989

Introduction to Bipolar Logic
Low Power Schottky
Schottky
TTL
TTL - Low Power
Physical Dimensions

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Introduction to Bipolar Logic

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## Guide to Bipolar Logic Device Families

Since the introduction of the first saturating logic bipolar integrated circuit family (DM54/DM74), there have been many developments in the process and manufacturing technologies as well as circuit design techniques which have produced new generations (families) of bipolar logic devices. Each generation had advantages and disadvantages over the previous generations. Today National provides seven bipolar logic families.

## TTL

(DM54/DM74)
Low Power TTL
Low Power Schottky
Advanced Low Power Schottky Schottky
Advanced Schottky
FAST

## TTL LOGIC (DM54/DM74) and (54xx)

TTL logic was the first saturating logic integrated circuit family introduced, thus setting the standard for all the future families. It offers a combination of speed, power consumption, output source and sink capabilities suitable for most applications. This family offers the greatest variety of logic functions. The basic gate (see Figure 1) features a multipleemitter input configuration for fast switching speeds, active pull-up output to provide a low driving source impedance which also improves noise margin and device speed. Typical device power dissipation is 10 mW per gate and the typical propagation delay is 10 ns when driving a 15 $\mathrm{pF} / 400 \Omega$ load.

## LOW POWER TTL (DM54L)

The low power family has essentially the same circuit configuration as the TTL devices. The resistor values, however, are increased by nearly tenfold, which results in tremendous reduction of power dissipation to less than $1 / 10$ of the TTL family. Because of this reduction of power, the device speed


FIGURE 1. DM5400/DM7400
is sacrificed. The propagation delays are increased threefold. These devices have a typical power dissipation of 1 mW per gate and typical propagation delay of 33 ns , making this family ideal for applications where power consumption and heat dissipation are the critical parameters.

## LOW POWER SCHOTTKY (DM54LS/DM74LS and 54LS)

The low power Schottky family features a combined fivefold reduction in current and power when compared to the TTL family. Gold doping commonly used in the TTL devices reduces switching times at the expense of current gain. The LS process overcomes this limitation by using a surface barrier diode (Schottky diode) in the baker clamp configuration between the base and collector junction of the transistor. In this way, the transistor is never fully saturated and recovers quickly when base drive is interrupted. Using shallower diffusion and soft-saturating Schottky diode clamped transistors, higher current gains and faster turn-on times are obtained. The National LS circuits and a majority of the former Fairchild LS circuits do not use the multi-emitter inputs. They use diode-transistor inputs which are faster and give increased input breakdown voltage; the input threshold is $\sim 0.1 \mathrm{~V}$ lower than TTL. A few of the former Fairchild LS circuits use the traditional emitter inputs and thus have input breakdown ratings of 5.5 V . These circuits are the open-collector gate types 'LS03, 'LS05, 'LS22 and 'LS136; flip-flop types 'LS74, 'LS109, 'LS112 and 'LS113; and the clock inputs of the 'LS490. Another commonly used input is the vertical substrate PNP transistor. In addition to fast switching, it exhibits very high impedance at both the high and low input states, and the transistor's current gain ( $\beta$ ) significantly reduces input loading and provides better output performance. The output structure is also modified with a Darlington transistor pair to increase speed and improve drive capability. An active pull-down transistor (Q3) is incorporated to


TL/F/5534-7

FIGURE 2. DM54L00
yield a symmetrical transfer characteristic (squaring network). This family achieves circuit performance exceeding the standard TTL family at fractions of its power consumption. The typical device power dissipation is 2 mW per gate and typical propagation delay is 10 ns while driving a $15 \mathrm{pF} /$ $2 \mathrm{k} \Omega$ load.

## SCHOTTKY (DM54S/DM74S)

This family features the high switching speed of unsaturated bipolar emitter-coupled logic, but consumes more power than standard TTL devices. To achieve this high speed, the Schottky barrier diode is incorporated as a clamp to divert the excess base current and to prevent the transistor from reaching deep saturation. The Schottky gate input and internal circuitry resemble the standard TTL gate except the resistor values are about one-half the TTL value. The output section has a Darlington transistor pair for pull-up and an active pull-down squaring network. This family has power dissipation of 20 mW per gate and propagation delays three times as fast as TTL devices with the average time of 3 ns while driving $15 \mathrm{pF} / 280 \Omega$ load.

## ADVANCED LOW POWER SCHOTTKY (DM54ALS/DM74ALS)

The advanced low power Schottky family is one of the most advanced TTL families. It delivers twice the data handling efficiency and still provides up to $50 \%$ reduction in power consumption compared to the LS family. This is possible because of a new fabrication process where components are isolated by a selectively grown thick-oxide rather than the P-N junction used in conventional processes. This refined process, coupled with improved circuit design techniques, yields smaller component geometries, shallower diffusions, and lower junction capacitances. This enables the devices to have increased $f_{T}$ in excess of 5 GHz and improved switching speeds by a factor of two, while offering much lower operating currents.


TL/F/5534-3
FIGURE 3. DM54LS00/DM74LS00

In addition to the pin-to-pin compatibility of the ALS family, a large number of MSI and LSI functions are introduced in the high density 24 -pin 300 mil DIP. These devices offer the designers greater cost effectiveness with the advantages of reduced component count, reduced circuit board real-estate, increased functional capabilities per device and improved speed-power perfomance.
The basic ALS gate schematic is quite similar to the LS gate. It consists of either the PNP transistor or the diode inputs, Darlington transistor pair pull-up and active pulldown (squaring network) at the output. Since the shallower diffusions and thinner oxides will cause ALS devices to be more susceptible to damage from electro-static discharge, additional protection via a base-emitter shorted transistor is included at the input for rapid discharge of high voltage static electricity. Furthermore, the inputs and outputs are clamped by Schottky diodes to prevent them from swinging excessively below ground level. A buried $\mathrm{N}^{+}$guard ring around all input and output structures prevents crosstalk. The ALS family has a typical power dissipation of 1 mW per gate and typical propagation delay time of 4 ns into a $50 \mathrm{pF} / 2 \mathrm{k} \Omega$ load.

## ADVANCED SCHOTTKY (DM54AS/DM74AS)

This family of devices is designed to meet the needs of the system designers who require the ultimate in speed. Utilizing Schottky barrier diode clamped transistors with shallower diffusions and advanced oxide-isolation fabrication techniques, the AS family achieves the fastest propagation delay that bipolar technology can offer. The AS family has virtually the same circuit configuration as the ALS family. It has PNP transistor or diode inputs with electrostatic protection base-emitter shorted transistors. The output totem-pole consists of a Darlington pair transistor pull-up and an active


FIGURE 3a. 54/74LS00
pull-down squaring network. The inputs and outputs are Schottky clamped to attenuate critical transmission line reflections. In addition, the circuit contains the "Miller Killer" network at the output section to improve output rise time and reduce power consumption during switching at high repetition rates. The AS family yields typical power dissipation of 7 mW per gate and propagation delay time of 1.5 ns when driving a $50 \mathrm{pF} / 2 \mathrm{k} \Omega$ load.

## FAST® TECHNOLOGY

FAST (Fairchild Advanced Schottky TTL) circuits are made with the advanced isoplanar II process, which produces transistors with very high, well-controlled switching speeds, extremely small parasitic capacitances and $\mathrm{f}_{\mathrm{T}}$ in excess of 5 GHz . Isoplanar is an established National process, used for years in the manufacture of bipolar memories. CMOS, subnanosecond ECL and ${ }^{3}$ LTM (Isoplanar Integrated Injection Logic) LSI devices.
In the isoplanar process, components are isolated by a selectively grown thick oxide rather than the $p^{+}$isolation region used in the planar process. Since this oxide needs no separation from the base-collector regions, component and
chip sizes are substantially reduced. The base and emitter ends terminate in the oxide wall; masks can thus overlap the device area into the isolation oxide. This overlap feature eliminates the extremely close tolerances normally required for base and emitter masking, and the standard photolithographic processes can be used.

## SELECTING A FAMILY

Two factors shoud be considered when choosing a logic family for application, speed and power consumption. New logic families were created to improve the speed or lower the power consumption of the previous families. The following tables rate each family.

| Speed |  |  | Power Consumption |
| :---: | :---: | :---: | :---: |
| Fastest | AS/F | Low | L |
|  | S |  | ALS |
|  | $\downarrow$ | ALS |  |
|  | LS | $\downarrow$ | LS |
|  | TTL |  | F |
|  |  |  | AS |
|  | Slowest | L | High |



FIGURE 6. DM54AS00/DM74AS00

# Consolidation of National Semiconductor and Fairchild Semiconductor 

The combination of National Semiconductor and Fairchild Semiconductor provides the largest selection of Bipolar Logic Devices available anywhere. Recognizing that two of the major product lines overlap-Low Power Schottky and Standard TTL—both the Mil/Aero and Commercial products were consolidated so as to have the least impact on their customers.

## Military/Aerospace Products

All of the Mil/Aero MIL-STD-883 devices were maintained for both National and Fairchild. In other words, the same mask set, fab processes and electrical tests and specifications were continued for all devices previously made by Fairchild Semiconductor as well as National Semiconductor, whether there was duplication of a device or not. For exam-
ple, the QUAD 2-INPUT NAND Gates, DM54LS00 and 54LS00 are both available. The former's performance is described by RET's (Reliability Electrical Test specifications); and the latter's by a Table I. This is done to prevent considerable inconvenience to our customers who would have had to modify their Source Control Drawings were a change made to the device or its name.
While the datasheets in this databook do not describe the full performance of the Mil/Aero devices, the Table I and/or the RET's do, and may be obtained through your local Field Sales Offices or Representatives.
In terms of nomenclature, National Semiconductor uses the prefix "DM" to represent all National-origin Mil/Aero devices. The Fairchild-origin Mil/Aero devices uses no "DM" prefix. Ordering information is included as well.


MIL-STD-883/C Military

Package Outline
D = Ceramic Dual-In-Line Package
F = Ceramic Flat Package
$\mathrm{L}=$ Ceramic Leadless Chip Carrier Package

Device Number

Military Device Family

## Commercial Products

The majority of products in the Low Power Schottky, Schottky and TTL logic families produced by National and Fairchild are nearly identical in performance and considerably over!ap in portfolio size. All of the sole source functions were retained after the consolidation to minimize the impact
to our customers. Fairchild devices that remain in the logic family portfolios are now designated by the National nomenclature. Where a Fairchild device was named 74LS373PC, it will now be referenced to as a DM74LS373N. Please refer to the ordering format below.


## IC Device Testing

Understanding the intent and practice of IC device testing is vital to insuring both the quality and proper usage of integrated circuits. All National Semiconductor data sheets list the AC and DC parameters with min and/or max limits, along with forcing functions. Understanding when a part fails the limit, and which forcing functions are really tighter, is critical when determining if an IC device is good or bad.
All of National's databook parameters are defined and guaranteed for "worst-case testing." Input loading currents (fanin) are tested at the input and $\mathrm{V}_{\mathrm{CC}}$ levels that most increase that loading, while the output drive capability (fan-out) is tested at the input and $\mathrm{V}_{\mathrm{CC}}$ levels that most decrease that capability. ICC is tested with the input conditions and $V_{C C}$ level that yield the greatest lCc value, and VCLAMP is tested such that the negative voltage is maximized for the given clamp current. The fan-in and fan-out specs are contained in the $I_{I_{H},} l_{O H}, l_{I L}$ and $l_{O L}$ values. To guarantee these fan-in and fan-out limits at 10, the lol must be at least 10 times the $I_{I L}$ and the $I_{O H}$ must be at least 10 times the $I_{I H}$. Be aware that the fan-in and fan-out specifications are valid only within a given device family. The standard input loading and output drives are shown in Table I.
Notice that the $\mathrm{l}_{\mathrm{OL}}$ is at least 10 times the $\mathrm{I}_{\mathrm{IL}}$ and that the $\mathrm{l}_{\mathrm{OH}}$ is greater than 10 times the $\mathrm{I}_{\mathrm{IH}}$. Also notice that these are "standard" drive and load currents for single sink outputs and inputs. Certain devices may have multiple load inputs where the input line goes to several input structures and has, say, 2 or 3 times the normal $\mathrm{I}_{\mathrm{IL}}$ and $\mathrm{I}_{\mathrm{IH}}$ loading.

Certain other devices will have "triple sink" outputs that can drive 3 times the standard $\mathrm{I}_{\mathrm{OL}}$ and $\mathrm{I}_{\mathrm{OH}}$ currents. These devices are generally bus drivers, or drivers intended to drive highly capacitive loads. Finally, there are certain devices that have PNP inputs that reduce the I/L loading to typically $-200 \mu \mathrm{~A}$, thus allowing an increased DC fan-in of 20. One must therefore be careful when interfacing many different types of devices, even in the same family, and not simply go the "fan-out of 10 " rule.
When dealing with any kind of device specification, it is important to note that there exists a pair of test conditions that define that test: the forcing function and the limit. Forcing functions appear under the column labeled "Conditions" and define the external operating constraints placed upon the device tested. The actual test limit defines how well the device responds to these constraints. For example, take the parameter $\mathrm{V}_{\mathrm{OH}(\min )}$ for the DM74LSOO. It is tested at $\mathrm{V}_{\mathrm{CC}(\text { min })}=4.75 \mathrm{~V}$ commercial, using an $\mathrm{IOH}_{\mathrm{OH}}=-400 \mu \mathrm{~A}$. If we required an $\mathrm{I}_{\mathrm{OH}}=-800 \mu \mathrm{~A}$, this would be a "tighter" test, as the output voltage drops with increased $\mathrm{IOH}_{\mathrm{OH}}$. Hence, a device that would pass the $-800 \mu \mathrm{~A} \mathrm{I}_{\mathrm{OH}}$ would also pass the $-400 \mu \mathrm{~A} \mathrm{lOH}$, but not necessarily the other way around. Futhermore, $\mathrm{V}_{\mathrm{OH}}$ tracks with $\mathrm{V}_{\mathrm{CC}}$, which is why $\mathrm{V}_{\mathrm{CC}(\text { min })}$ is the worst-case testing, and not $\mathrm{V}_{\mathrm{CC}(\max )}$. Finally, forcing inputs to threshold represents the most difficult testing because this puts those inputs as close as possible to the actual switching point and guarantees that the device will meet the $\mathrm{V}_{\mathrm{IH}} / \mathrm{V}_{\mathrm{IL}}$ spec.

TABLE I. Fan-In/Fan-Out

| Device Family | Input Loading | Output Drive |
| :--- | :--- | :--- |
| TTL | $I_{\mathrm{IL}}=-1.6 \mathrm{~mA}$ | $\mathrm{I}_{\mathrm{OL}}=16 \mathrm{~mA}$ |
|  | $I_{\mathrm{IH}}=40 \mu \mathrm{~A}$ | $\mathrm{I}_{\mathrm{OH}}=-400 \mu \mathrm{~A}$ |
| Low Power | $I_{\mathrm{IL}}=-400 \mu \mathrm{~A}$ | $\mathrm{I}_{\mathrm{OL}}=4 \mathrm{~mA}(\mathrm{Mil})$ |
| Schottky |  | $I_{\mathrm{OL}}=8 \mathrm{~mA}(\mathrm{Com})$ |
|  | $I_{\mathrm{IH}}=20 \mu \mathrm{~A}$ | $\mathrm{I}_{\mathrm{OH}}=-400 \mu \mathrm{~A}$ |
| Schottky | $I_{I L}=-2 \mathrm{~mA}$ | $\mathrm{I}_{\mathrm{OL}}=20 \mathrm{~mA}$ |
|  | $I_{I H}=50 \mu \mathrm{~A}$ | $I_{\mathrm{OH}}=-1 \mathrm{~mA}$ |

Tables II and III show the "direction" of the looser/tighter testing for most common DC parameters. Notice that one can tighten either the forcing function or the limit, or both. Tightening either one is sufficient to insure a tighter test. Also notice the difference between max and min limits. For IOS (double-ended limits), even though -20 mA is more positive than -100 mA , and is mathematically the max limit,
the magnitude of the number is the determining factor when deciding which is the max limit. The negative sign simply implies the direction that the current is going, with a negative current leaving the device, and a positive current entering the device. Table II shows the direction of tighter forcing functions, while Table III shows the direction of tighter limits.

TABLE II. Looser/Tighter Forcing Functions Example: DM74LS00

| Condition | Test | Looser | Nominal | Tighter | Units |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{IK}}$ | $\mathrm{V}_{\mathrm{IK}}$ | -17 | -18 | -19 | mA |
| $\mathrm{I}_{\mathrm{OH}}$ | $\mathrm{V}_{\mathrm{OH}}$ | -350 | -400 | -450 | $\mu \mathrm{~A}$ |
| $\mathrm{I}_{\mathrm{OL}}$ | $\mathrm{V}_{\mathrm{OL}}$ | 3 | 4 | 5 | mA |
| $\mathrm{~V}_{\mathrm{I}}$ | $\mathrm{I}_{\mathrm{I}}$ | 6.5 | 7 | 7.5 | V |
| $\mathrm{~V}_{\mathrm{IH}}$ | $\mathrm{I}_{\mathrm{IH}}$ | 2.6 | 2.7 | 2.8 | V |
| $\mathrm{~V}_{\mathrm{IL}}$ | $\mathrm{I}_{\mathrm{IL}}$ | 0.5 | 0.4 | 0.3 | V |
| $\mathrm{~V}_{\mathrm{O}}$ | $\mathrm{I}_{\mathrm{OS}}$ | 0.1 | 0.0 | -0.1 | V |
| $\mathrm{~V}_{\mathrm{CC}}$ | $\mathrm{I}_{\mathrm{CC}}$ | 5.0 | 5.5 | 6.0 | V |

TABLE III. Looser/Tighter Test Limits Example: DM74L.S00

| Parameter | Looser | Nominal | Tighter | Units |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{IH} \text { (min) }}$ | 2.1 | 2.0 | 1.9 | V |
| $\mathrm{V}_{\mathrm{IL} \text { (max) }}$ | 0.7 | 0.8 | 0.9 | V |
| $V_{\text {IK (max) }}$ | -1.6 | -1.5 | -1.4 | V |
| $\mathrm{V}_{\mathrm{OH}(\text { min }}$ | 2.6 | 2.7 | 2.8 | V |
| $\mathrm{V}_{\text {OL(max) }}$ | 0.6 | 0.5 | 0.4 | V |
| $1 /$ min) | 6.5 | 7.0 | 7.5 | V |
| $\mathrm{IIH}_{(\text {max }}$ | 50 | 40 | 30 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {IL(max }}$ | -450 | -400 | -390 | $\mu \mathrm{A}$ |
| loS (max) | -110 | -100 | -90 | mA |
| los(min) | -10 | -20 | -30 | mA |
| $\mathrm{I}^{\text {CCH }}$ (max) | 1.7 | 1.6 | 1.5 | mA |
| $\mathrm{I}_{\text {CCL }}($ max $)$ | 4.5 | 4.4 | 4.3 | mA |

Following are the test set-ups that are used to test the DC parametrics. In each case, the gate connection, equivalent circuit schematic and resultant voltage/current plot are shown.

The indicated graphs are typical of LS products and are similiar to other bipolar logic families. The schematics shown are for single inversion devices and represent generalized circuits.

## OUTPUT VOLTAGE LOW LEVEL (VOL)

Both inputs are connected to logic " 1 " values (assuming an inverting gate) and forced at the $\mathrm{V}_{\mathrm{iH}}$ specs. $\mathrm{V}_{\mathrm{CC}}$ minimum is used, and $\mathrm{l}_{\mathrm{OL}}$ is forced on the output. The resulting $\mathrm{V}_{\mathrm{OL}}$ is



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measured. For typical LS products, the military and commercial test points are indicated on the $\mathrm{V}_{\mathrm{OL}}$ vs loL graph. In each case, the device must not exceed the $\mathrm{V}_{\mathrm{OL}}$ spec when the lol current is being forced.

## OUTPUT VOLTAGE HIGH LEVEL ( $\mathbf{V}_{\mathbf{O H}}$ )

One input is tied high (any value above 2.0 V ) and the other input is forced at the $\mathrm{V}_{\mathrm{IL}}$ threshold (assuming a single inversion gate). The minimum $V_{C C}$ value is used. Each input is tested independently and the $\mathrm{I}_{\mathrm{OH}}$ current is forced. The resulting $\mathrm{V}_{\mathrm{OH}}$ is measured. The $\mathrm{V}_{\mathrm{OH}}$ vs $\mathrm{I}_{\mathrm{OH}}$ graph shows the military and commercial $\mathrm{V}_{\mathrm{OH}} / \mathrm{IOH}_{\mathrm{OH}}$ test points for standard LS products.



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## INPUT CURRENT HIGH LEVEL (IH)

$I_{I H}$ tests the input leakage in the high state. For MET, diode, and PNP input, the test set-up consists of all inputs except the one under test tied high (greater than $\mathrm{V}_{\mathrm{IH}}$ ). The remaining input has the $\mathrm{V}_{1 \mathrm{H}}$ value forced upon it, and the resultant $l_{I H}$ is measured. This test checks for emitter-to-collector inverse transistor action for MET inputs, and reverse bias leakage for diode and PNP inputs.
For MET inputs, there is also an additional set-up for $I_{1 H}$ testing that checks for emitter-to-emitter transistor action. This is done with all the other inputs tied to ground.

## MAXIMUM INPUT CURRENT (l)

$I_{I}$ or $B V_{I N}$ testing is the same as the emitter-to-collector leakage test ( $l_{H}$ ) and guarantees that the input will not pass more than the specified current at the stated specification ( $100 \mu \mathrm{~A}$ at 7 V for LS).


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## INPUT CURRENT LOW LEVEL (ILL)

One input at a time is tested with the other inputs tied to a solid " 1 " value. $V_{C C}$ is set to the maximum value and the $V_{I L}$ value is forced. $I_{I L}$ is then measured.

$$
\begin{aligned}
& I_{I L}=\frac{\left[V_{C C}-\left(V_{I L}+V_{B E}\right)\right]}{R 1} \text { Standard Inputs. } \\
& I_{I L}=\frac{\left[V_{C C}-\left(V_{I L}+V_{S H}\right)\right]}{R 1} \text { Diode Inputs } \\
& I_{I L}=\frac{\left[V_{C C}-\left(V_{I L}+V_{B E}\right)\right]}{R 1 \times \beta} \text { PNP Inputs }
\end{aligned}
$$

$I_{I L}$ is intended to measure the value of the base pull-up resistor on the input, and to guarantee the maximum input load an IC presents.


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TL/F/6731-10


TL/F/6731-12

## OUTPUT SHORT CIRCUIT CURRENT (los)

los is measured with $\mathrm{V}_{\mathrm{CC}}$ (max) and the OV forced on the output while it is in the high state. The resultant current is measured. The purpose of this is to check the los resistor that forms the Darlington's collector pull-up. This parameter is important as it reflects both the maximum current the device will draw and the maximum drive it will provide when it is switching from low to high.
Caution must be taken when measuring TTL, LS and S outputs as the power dissipated on the die will be substantial. los shorts should not be maintained in excess of one second or damage to the device may result.


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SUPPLY CURRENT HIGH LEVEL (Iссн) AND SUPPLY CURRENT LOW LEVEL (Iccl)
Both $\mathrm{I}_{\mathrm{CCH}}$ and $\mathrm{I}_{\mathrm{CCL}}$ are tested using the $\mathrm{V}_{\mathrm{CC}}$ maximum value. The inputs are set to the values necessary to achieve the output in the desired state. All outputs are left open, neither sourcing nor sinking current. The goal of this test is to guarantee the maximum quiescent operating power that the device will draw.


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INPUT CLAMP VOLTAGE (VIC OR $\mathbf{V}_{\mathbf{I K}}$ )
$V_{C L A M P}\left(V_{\text {IK }}\right)$ is measured with all but one input tied high and the $I_{I K}$ current forced on the remaining input. $V_{C C}$ is set to the minimum and the $\mathrm{V}_{\mathrm{IK}}$ voltage is measured.

OUTPUT TRI-STATE CURRENT HIGH LEVEL (IOZH) AND OUTPUT TRI-STATE CURRENT LOW LEVEL (lozL)
TRI-STATE® I $_{\text {SINK }}$ and ISOURCE are measured with the output control input tied to the appropriate threshold value (usually $\mathrm{V}_{\mathrm{IL}}=0.8 \mathrm{~V}$ ) and with $\mathrm{V}_{\mathrm{CC}(\max )}$. This is to insure that

Vclamp Vs lclamp
Typical LS Device Curve




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the output will have the greatest drive capability and the TRI-STATE control can effectively "turn off" the output under these conditions.
TRI-STATE ISINK: Output is set in the high state and then TRI-STATE mode. $\mathrm{V}_{\text {OZL }}=0.4 \mathrm{~V}$ is then applied. The current drawn out of the device is then measured.
TRI-STATE ISOURCE: Output is set in the low state and then TRI-STATE mode. $\mathrm{V}_{\mathrm{OZH}}=2.7 \mathrm{~V}$ is then applied. The current drawn into the device is then measured.


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## HIGH LEVEL OUTPUT CURRENT (OPEN-COLLECTOR DEVICES ONLY)

ICEX is tested with the output in the high state. $\mathrm{V}_{C C}$ is set to 5.0 V and the specified voltage ( 5.5 V for LS ) is applied to the output. The inputs are at the threshold values ( 0.8 V and 2.0 V , depending upon the logic to put output in the high state) and the resulting ICEX leakage current is measured.


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TL/F/6731-25


## AC SWITCHING CHARACTERISTICS

The AC switching characteristics are generally measured in units of time (commonly in nanoseconds), and define how long it takes for the signal to propagate from the input to the output. The definitions used in determining the pass/fail status of each limit are not the same for AC as they are for DC. The distinction lies in the fact that for DC operation there exists one characteristic V-I curve on which the device must operate. Devices are good if they operate on the correct side of the limit, and bad if they operate on the wrong side of the limit. When dealing with certain AC parameters ( $f_{\text {MAX }}, t_{\text {SET-UP, }} \mathrm{t}_{\text {HOLD }}, \mathrm{t}_{\text {RELEASE, }} \mathrm{t}_{\text {PW }}$ ), the device can, and usually does, operate on both sides of the databook limit. The limit really implies a boundary that all devices are guaranteed to exceed. Depending upon the parameter, the device will either operate at all values above and some below the limit, or it will operate at all values below and some above the limit. In each case, the device is only guaranteed to operate for all values on one side of the limit. Although the device will also operate beyond the limit, it is not guaranteed to. Furthermore, device operation beyond the limit is not considered a failure. For instance, take the $f_{\text {MAX }}$ parameter with a min limit of 25 MHz . All devices are guaranteed to operate at all frequencies below 25 MHz and will operate in excess of 25 MHz , although this is not guaranteed. Now, take the example of tSET-UP with a minimum limit of 25 ns . All of the devices are guaranteed to operate with a set-up time of 25 ns and longer, and will operate with set-up times below 25 ns , although this is not guaranteed either. Be aware that both of these specifications are listed in the minimum column in the databook, but the interpretation of what is failing differs significantly.
Propagation delays (called prop delays and denoted by the symbols $t_{P H L}$ and $\left.t_{P L H}\right)$ are specified as maximum limits, and guarantee the maximum time one must wait to insure that the correct data has appeared at the device's output. Each propagation delay is specified from one input to one output only.
Input set-up and hold times (including treLEASE) specify how long one input must be stable at a particular logic level prior to an action occurring at another input. For example, take the DM54/74LS74 positive-edge-triggered D flip-flop. The "set-up 1" specification defines how long a logic " 1 " must be present and stable at the DATA input prior to the positive edge of the CLOCK to insure that the device will recognize that data as a " 1 ". There also exists a "hold 1" specification which specifies how long a logic " 1 " must be held after the active edge of CLOCK for the device to recognize that logic " 1 ". Both the set-up and hold times must always be met or the device will not necessarily bring in the proper data. Set-up times are generally positive, while hold
times may be either positive or negative, usually negative. The meaning of a negative hold time is that the data may be removed from the input prior to the active edge of CLOCK, and the CLOCK will still bring in the desired data. Set-up and hold times are specified as minimum values, since this defines the minimum time data must be stable prior to any change at the CLOCK input. Removing the data sooner than the minimum time may cause improper action on the part of the device.
$t_{\text {release }}$ is specified on devices where there is an input that must be set inactive prior to the active edge of CLOCK. Such inputs are usually overriding inputs like CLEAR and PRESET. With CLEAR active, it will prevent the device from switching on the CLOCK signal. treLEASE is defined as the time it takes for the CLEAR input to "release" the device for clocking action, and is specified as a minimum. This represents the maximum delay required between CLEAR going inactive and the active edge of CLOCK to insure proper device operation.
All devices that have a CLOCK input also have a specification that defines the maximum speed that the CLOCK can be driven, called $f_{\text {MAX }}$. This specification is defined as a minimum specification and states that all of the devices will
be able to operate at frequencies up to 25 MHz . For the DM54/74LS74 with an $f_{\text {MAX }}$ of 25 MHz , all of the devices are guaranteed to operate at all clock frequencies, up to and including 25 MHz . Although no devices are guaranteed to operate above $f_{\text {MAX }}$ (only below it), most devices will operate beyond the maximum specification. The minimum limit does not state that the device will not operate below $f_{\text {MAX }}$ or that any devices that do are bad, but rather that all the devices will operate up to the limit.
Table IV shows the direction of the tighter testing for the more common AC parameters. All prop dealys (those AC parameters that have the symbols $\mathrm{t}_{\mathrm{LLH}}$ or $\mathrm{t}_{\mathrm{PHL}}$ ) have simple $\mathrm{min} / \mathrm{max}$ limits. The device is guaranteed to operate within the bounds of the $\mathrm{min} / \mathrm{max}$ limits, and any operation outside these limits denotes a device failure. tset-up, thold, fmax, and trelease parameters have limits that denote guaranteed operation boundaries (i.e., the device is guaranteed to operate up to the boundary) but no guarantee is made concerning the device operation (or lack of it) beyond the boundary.
For detailed information on the AC waveforms, please see the test waveforms in this section.

TABLE IV. Looser/Tighter AC Test Limits Example: DM74LS74

| Test | From | Looser | Nominal | Tighter | Units |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{f}_{\max (\min )}$ |  | 24 | 25 | 26 | MHz |
| $t_{\text {PLH }}(\max )$ | CLR, PRE, CLK | 26 | 25 | 24 | ns |
| $t_{\text {PHL(max) }}$ | CLR, PRE, CLK | 31 | 30 | 29 | ns |
| $t_{W(\min )}$ | CLOCK HIGH | 21 | 20 | 19 | ns |
| $t_{W(\min )}$ | PRE, CLR LOW | 26 | 25 | 24 | ns |
| $t_{S E T-U P(\min )}$ | DATA HIGH | 21 | 20 | 19 | ns |
| $t_{S E T-U P(\min )}$ | DATA LOW | 21 | 20 | 19 | ns |
| $t_{\text {HOLD }(\min )}$ | All DATA | 1 | 0 | -1 | ns |


|  | tional <br> micon | C |  | thm | Op | tors |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Function/Description |  | Type | Technology |  |  |  |  |  |  |  | No. of Blts | No. of Pins |
|  |  | STD <br> TTL | L |  | S |  | LS |  |  |  |
|  |  | 54 | 74 | 54 | 74 | 54 | 74 | 54 | 74 |  |  |
| Adder/Binary 4-Bit with Fast Carry |  |  | '83 | X |  |  |  |  |  | X | X | 4 | 16 |
|  |  | '283 | X | X |  |  | X | x | X | X | 4 | 16 |
| ALU with Carry Look Ahead |  |  | '181 | X |  |  |  | X | X | X | X | 4 | 24 |
|  |  | '381 |  |  |  |  |  | X |  |  | 4 | 20 |
|  |  | 93541 |  |  |  |  |  | X |  |  | 4 | 24 |
| Binary to BCD Converter |  | '185 |  | X |  |  |  |  |  |  | 6 | 16 |
| BCD to Binary Converter |  | '184 |  | X |  |  |  |  |  |  | 6 | 16 |
| Lookahead Carry Generator |  | '182 |  |  |  |  | X | $x$ |  |  |  | 16 |
| Multiplier/Twos Complement |  | 93543 |  |  |  |  |  | X |  |  | $4 \times 2$ | 24 |
| 9-Bit Parity Generator/Checker |  | '180 | X | X |  |  |  |  |  |  | 9 | 14 |
|  |  | '280 |  |  |  |  | X | x |  |  | 9 | 14 |
|  |  | 93562 |  |  |  |  |  | X |  |  | 9 | 14 |
| 12-Bit Parity Generator/Checker |  | 9348 | X |  |  |  |  |  |  |  | 12 | 16 |
| Comparator | 4-Bit Magnitude with Expander | '85 | X | X |  |  |  |  | X | X | 4 | 16 |
|  | 5-Bit Magnitude | 9324 | X | X | X |  |  |  |  |  | 5 | 16 |
|  | Hi-Speed 6-Bit Identity with Expander | 93546 |  |  |  |  |  | X |  |  | 6 | 16 |
|  | Hi-Speed 6-Bit Identity with OC* | $93 S 47$ |  |  |  |  |  | X |  |  | 6 | 16 |
|  | 6-Bit Unified Bus with OC* | 7136 | X |  |  |  |  |  |  |  | 6 | 16 |
|  | 6-Bit Magnitude with OC* | 7160 | X |  |  |  |  |  |  |  | 6 | 16 |
|  | 10-Bit <br> Magnitude with $O C^{*}$ | 7130 | X |  |  |  |  |  |  |  | 10 | 24 |
| 6-Bit Binary Rate Multiplier |  | '97 | X | X |  |  |  |  |  |  | 64 | 16 |
| *OC : Open Collector |  |  |  |  |  |  |  |  |  |  |  |  |


| Function/Description | Type | Technology |  |  |  |  |  |  |  | Up/Down | Clock <br> Edge | No. of Pins |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | STDTTL |  | L |  | S |  | LS |  |  |  |  |
|  |  | 54 | 74 | 54 | 74 | 54 | 74 | 54 | 74 |  |  |  |
| 4-Bit Binary Counter | '93 | X | X | X |  |  |  |  | X |  | $\checkmark$ | 14 |
|  | '293 |  |  |  |  |  |  |  | X |  | $\checkmark$ | 14 |
| Synchronous Modulo 64-Bit Rate Multiplier | '97 | X | x |  |  |  |  |  |  |  | $\sim$ | 16 |
| Asynchronous Decade Counter | '90 | X | X |  |  |  |  | X | x |  | $\checkmark$ | 14 |
| Synchronous 4-Bit Binary Counter with Asynchronous Clear | '161 | X | X |  |  | x | X | x | X |  | $\checkmark$ | 16 |
| Synchronous Presettable BCD Decade Counter | '160 | X |  |  |  |  |  | X | X |  | $\Omega$ | 16 |
| Synchronous 4-Bit Binary Counter with Synchronous Clear | '163 | X | X |  |  | x | X | X | X |  | $\widetilde{ }$ | 16 |
| Synchronous Presettable BCD Decade Counter | '162 |  |  |  |  |  |  | X | X |  | $\sim$ | 16 |
| Synchronous Bidirectional BCD Decade Counter | '168 |  |  |  |  |  |  | X |  | X | $\Omega$ | 16 |
| Synchronous 4-Bit Up/Down Binary Counter | '169 |  |  |  |  |  |  | x | X | X | $\widetilde{ }$ | 16 |
| Synchronous Up/Down Decade Counter with Mode Control | '190 |  |  |  |  |  |  | X | X | X | $\widetilde{ }$ | 16 |
| Synchronous 4-Bit Up/Down Binary Counter with Mode Control | '191 | X | X |  |  |  |  | X | X | X | $\Omega$ | 16 |
| Synchronous 4-Bit Up/Down Binary Counter with Dual Clock | '193 | X |  |  |  |  |  | X | X | X | $\sim$ | 16 |
| Asynchronous Presettable Decade Counter | '196 |  |  |  |  |  |  |  | X |  | $\checkmark$ | 14 |
| Asynchronous Presettable Binary Counter | '197 |  | X |  |  |  |  |  | X |  | $\checkmark$ | 14 |
| BCD Decade Counter/4-Bit | 9310 |  |  | $x$ |  |  |  |  |  |  | $\Omega$ | 16 |
| Binary Counter | 9316 | x | X | X |  |  |  |  |  |  | $\sim$ | 16 |
| TRI-STATE® Programmable 4-Bit Binary Counter | 7556 | X |  |  |  |  |  |  |  |  | $\Omega$ | 16 |
| Decade Counter with Separate Up/Down Clocks | '192 |  |  |  |  |  |  | X | X | X | $\Omega$ | 16 |
| Decade Counter | '290 |  |  |  |  |  |  |  | X |  | 2 | 14 |
| Dual Decade (Bi-Quinary) Counter | '390 |  |  |  |  |  |  |  | X |  | $\checkmark$ | 16 |
| Dual 4-Bit Binary Counter | '393 |  |  |  |  |  |  |  | X |  | $\checkmark$ | 14 |
| Dual Decade Counter | '490 |  |  |  |  |  |  | X | X |  | $\checkmark$ | 16 |


| Decoders/Demultiplexers |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Function/Description | Type | Technology |  |  |  |  |  |  |  | Address Input | Active Low <br> Enable | Active Low Outputs | No. of Pins |
|  |  | STD <br> TTL |  | L |  | S |  | LS |  |  |  |  |  |
|  |  | 54 | 74 | 54 | 74 | 54 | 74 | 54 | 74 |  |  |  |  |
| Dual 1 of 4 | 9321 | X | X | X |  |  |  |  |  | $2+2$ | 1+1 | $4+4$ | 16 |
|  | '139 |  |  |  |  | X | X | X | x | 2+1 | 1+1 | $4+4$ | 16 |
|  | '155 | X | X |  |  |  |  | X | X | 2 | $2+1$ | $4+4$ | 16 |
|  | '156 |  |  |  |  |  |  | X | X | 2 | 2+1 | $4+4$ | 16 |
| 1 of 8 | 9301 | x | X |  | X |  |  |  |  | 3 | 1 | 8 | 16 |
|  | '45 | x | x |  |  |  |  |  |  | 3 | 1 | 8 | 16 |
|  | '42 | X | X |  |  |  |  | X | $x$ | 3 | 1 | 8 | 16 |
|  | '138 |  |  |  |  | X | x | X | X | 3 | 2 | 8 | 16 |
|  | '145 | X | X |  |  |  |  |  |  | 3 | 1 | 8 | 16 |
| 1 of 10 | 9301 | X | X | X |  |  |  |  |  | 4 (BCD) |  | 10 | 16 |
|  | '45 | X | X |  |  |  |  |  |  | 4 (BCD) |  | 10 | 16 |
|  | '42 | X | X |  |  |  |  | X | X | 4 (BCD) |  | 10 | 16 |
|  | '145 | x | x |  |  |  |  |  |  | 4 (BCD) |  | 10 | 16 |
| 1 of 16 | 9311 | X | X |  |  |  |  |  |  | 4 | 2 | 16 | 24 |
|  | '154 | X | X |  |  |  |  | X | x | 4 | 2 | 16 | 24 |
| 8 to 3-Line Priority Encoder | 9318 | X | X |  |  |  |  |  |  | 8 |  |  | 16 |
|  | '148 | X |  |  |  |  |  |  |  | 8 |  |  | 16 |


| Flip Fiops-Single \& Dual |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Function/Description | Type | Technology |  |  |  |  |  |  |  | Inputs | Clock <br> Edge | Direct Set | Direct Clear | No. of Pins |
|  |  | STD <br> TTL |  | L |  | S |  | LS |  |  |  |  |  |  |
|  |  | 54 | 74 | 54 | 74 | 54 | 74 | 54 | 74 |  |  |  |  |  |
| Dual JK | '73 | X | X | X |  |  |  | X | X | J, K | $\checkmark$ |  | X | 14 |
|  | '76 | X | X |  |  |  |  |  |  | J, K | $\checkmark$ | X | X | 16 |
|  | '107 | X |  |  |  |  |  | X | X | J, K | $\checkmark$ |  | X | 14 |
|  | '109 | X |  |  |  |  | X | $x$ | $x$ | $J, \bar{K}$ | $\Omega$ | X | X | 16 |
|  | '112 |  |  |  |  | X | X | X | X | J, K | $\checkmark$ | X | X | 16 |
|  | '113 |  |  |  |  | X | X | X |  | J, K | 2 | X* |  | 14 |
|  | '114 |  |  |  |  |  |  | X |  | J, K | $\checkmark$ | X | X | 14 |
|  | '72 |  |  | $x$ |  |  |  |  |  | J, K | $\checkmark$ | X | X | 14 |
| Dual D | '74 | X | X | X |  | X | X | X | X | D | $\checkmark$ | X | X | 14 |

*Does not apply to LS.

Filip Flops-Multiple

| Function/Description | Type | Technology |  |  |  |  |  |  |  | Data Inputs | Clock Inputs | Broadside Pinout | TRI-STATE Output | No. of Pins |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | STD <br> TTL |  | L |  | S |  | LS |  |  |  |  |  |  |
|  |  | 54 | 74 | 54 | 74 | 54 | 74 | 54 | 74 |  |  |  |  |  |
| 4-Bit D Flip Flop | '175 | X | X |  |  | X | X | X | X | $4 \times$ D | $\Gamma$ |  |  | 16 |
| 6-Bit D Flip Flop | '174 | X | X |  |  | X | X | X | X | $6 \times \mathrm{D}$ | $\Gamma$ |  | X | 16 |
| 8-Bit D Flip Flop | '374 |  |  |  |  | X | X | x | x | $8 \times \mathrm{D}$ | $\Gamma$ |  | X | 20 |
|  | '377 |  |  |  |  |  |  | X | x | $8 \times \mathrm{D}$ | $\sim$ |  |  | 20 |
|  | '534 |  |  |  |  |  |  |  | X | $8 \times D$ | $\Omega$ |  | X | 20 |
|  | '574 |  |  |  |  |  |  |  | x | $8 \times \mathrm{D}$ | $\Omega$ | X | X | 20 |
|  | '564 |  |  |  |  |  |  |  | X | $8 \times D$ | $\checkmark$ | X |  | 20 |
|  | '373 |  |  |  |  | X | X | X | X | $8 \times \mathrm{D}$ | $\Omega$ |  | X | 20 |
| 8-Bit Multiple Port Register | 9338 | X | X | X |  |  |  |  |  | $1 \times \mathrm{D}$ | L |  |  | 16 |
| Quad 2-Port Register | '298 | X |  |  |  |  |  | X | X | $2 \times 4 \times \mathrm{D}$ | $\checkmark$ |  |  | 16 |


| Gates |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Function/Descriptlon |  | Type | Technology |  |  |  |  |  |  |  | No. of Pins |
|  |  | STD <br> TTL | L |  | S |  | LS |  |  |
|  |  | 54 | 74 | 54 | 74 | 54 | 74 | 54 | 74 |  |
| NAND | Quad 2-Input NAND |  | '00 | X | X | X |  | X | X | X | $\times$ | 14 |
|  | Quad 2-Input NAND with $\mathrm{OC}^{*}$ |  | '01 | X | X |  |  |  |  |  |  | 14 |
|  |  | '03 | X | X |  |  |  | X | $x$ | X | 14 |
|  | Triple 3-Input NAND | '10 | X | X | X |  | X | X | $x$ | X | 14 |
|  | Triple 3-Input NAND with OC* | '12 |  |  |  |  |  |  | X | X | 14 |
|  | Dual 4-Input Schmitt Trigger | '13 |  |  |  |  |  |  | X | X | 14 |
|  | Dual 4-Input NAND | '20 | X | X |  |  | X | X | $x$ | X | 14 |
|  | Dual 4-Input NAND with OC* | '22 |  |  |  |  |  |  | X | X | 14 |
|  | 8-Input NAND Gate | '30 | $x$ | $x$ |  |  | X | X | X | X | 14 |
|  | Quad 2-Input Schmitt Trigger NAND | '132 | X | X |  |  |  | X | X | X | 14 |
|  | 13-Input NAND | '133 |  |  |  |  | X | X | $x$ | X | 16 |
| NOR | Quad 2-Input NOR | '02 | X | X | X |  | X | X | X | X | 14 |
|  | Dual 4-Input NOR with Strobe | '25 | X | X |  |  |  |  |  |  | 14 |
|  | Triple 3-Input NOR | '27 |  | X |  |  |  |  | X | X | 14 |
|  | Dual 5-Input NOR | '260 |  |  |  |  |  |  | X | X | 14 |
| AND | Quad 2-Input AND | '08 | x | X |  |  | X | X | X | X | 14 |
|  | Quad 2-Input AND with OC* | '09 | X | X |  |  |  | X | X | x | 14 |
|  | Triple 3-Input AND | '11 |  | X |  |  | X | X | X | X | 14 |
|  | Triple 3-Input AND with OC* | '15 |  |  |  |  |  |  | X | X | 14 |
|  | Dual 4-Input AND | '21 |  |  |  |  |  |  | X | X | 14 |
| Exclusive-OR | Quad Ex-OR | '86 | X | X |  |  | X | X | X | X | 14 |
|  | Quad 2-Input Ex-OR with OC* | '136 |  |  |  |  |  |  | X | X | 14 |
| OR | Quad 2-Input OR/ | '32 | X | X |  |  | X | X | X | X | 14 |
| Exclusive-NOR | $\begin{aligned} & \text { 4-Bit Quad Ex-NOR } \\ & \text { with OC* } \end{aligned}$ | 9386 |  | X |  |  |  |  |  |  | 14 |
|  | Quad 2-Input ExNOR with OC* | '266 |  |  |  |  |  |  | X | X | 14 |
| AND <br> OR <br> Gates Invert | Expandable Dual 2-Wide 2-Input | '50 |  | X |  |  |  |  |  |  | 14 |
|  | Dual 2-Wide 2-Input | '51 | X | X |  |  |  | X | X | X | 14 |
|  | 4-Wide 2-Input | '54 |  |  |  |  |  |  | X | X | 14 |
|  | 2-Wide 4-Input | '55 |  |  |  |  |  |  | X | X | 14 |
|  | 4-Wide | '64 |  |  |  |  | X | X |  |  | 14 |
| Inverters | Hex Inverters | '04 | X | X | X |  | X | X | X | $x$ | 14 |
|  | Hex Inverter with OC* | '05 | $x$ | X |  |  |  | X | X | X | 14 |
|  | Hex Schmitt Trigger Inverter | '14 | X | X |  |  |  |  | X | X | 14 |
| *OC : Open Collector |  |  |  |  |  |  |  |  |  |  |  |


| Latches |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Function | Type | Technology |  |  |  |  |  |  |  | Data Inputs | Enable Inputs (Level) | TRI-STATE Outputs | No. of Pins |
|  |  | STD <br> TTL |  | L |  | S |  | LS |  |  |  |  |  |
|  |  | 54 | 74 | 54 | 74 | 54 | 74 | 54 | 74 |  |  |  |  |
| 4-Bit D Latch | '75 | X | X |  |  |  |  | x | x | $4 \times$ D | 2(H) |  | 16 |
|  | '375 |  |  |  |  |  |  | X | X | $4 \times D$ | 2(H) |  | 16 |
| Dual 4-Bit D Latch | 9308 | X | X | X |  |  |  |  |  | $8 \times$ D | $\begin{aligned} & 2 \times 2 \\ & \text { AND } \end{aligned}$ |  | 24 |
| 4-Bit D Latch | 9314 | X | X | X |  |  |  |  |  | $4 \times D$ | 1(L) |  | 16 |
| 8-Bit D Latch | '373 |  |  |  |  | X | X | X | $x$ | $8 \times{ }^{*}$ | 1(H) | X | 20 |
|  | '533 |  |  |  |  |  |  |  | X | $8 \times D$ | 1(H) | X | 20 |
|  | '563 |  |  |  |  |  |  |  | X | $8 \times \mathrm{D}$ | 1(H) | X | 20 |
|  | '573 |  |  |  |  |  |  |  | X | $8 \times D$ | 1(L) | X | 20 |
| 8-Bit Addressable Latch | 9334 | X | X | X |  |  |  |  |  | $1 \times \mathrm{D}$ | 1(L) |  | 16 |
|  | '259 |  |  |  |  |  |  | X | X | $1 \times \mathrm{D}$ | 1(L) |  | 16 |
| Dual 4-Bit <br> Addressable Latch | '256 |  |  |  |  |  |  | X | X | $8 \times$ D | 2(L) |  | 16 |
| 4-Bit RS Latch | '279 | X | X |  |  |  |  | X | X | $4 \times(\overline{\mathrm{R}} \overline{\mathrm{S}})$ |  |  | 16 |

""D" only for SKY.

| Line and Bus Drivers/Transceivers/Receivers |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Function/Description | Type | Technology |  |  |  |  |  |  |  | No. of Pins |
|  |  | $\begin{aligned} & \text { STD } \\ & \text { TTL } \end{aligned}$ |  | L |  | S |  | LS |  |  |
|  |  | 54 | 74 | 54 | 74 | 54 | 74 | 54 | 74 |  |
| Quad 2 NAND Buffer | '37 | X | X |  |  |  |  | X | X | 14 |
| Quad 2 NAND Buffer with OC* | '26 | X | X |  |  |  |  | X | X | 14 |
|  | '38 | X | X |  |  |  |  | X | X | 14 |
|  | '39 |  | X |  |  |  |  |  |  | 14 |
|  | '96101 |  | X |  |  |  |  |  |  | 14 |
| Dual 4 NAND Buffer | '40 | X | X |  |  | $x$ | X | X | X | 14 |
|  | '140 |  |  |  |  | X | X |  |  | 14 |
| Quad 2 NOR Buffer | '28 |  |  |  |  |  |  | X | X | 14 |
| Quad 2 NOR Buffer with OC* | '33 |  |  |  |  |  |  | X | X | 14 |
| Quad TRI-STATE Buffer | '125 | X | X |  |  |  |  | X | X | 14 |
|  | '126 |  |  |  |  |  |  | X | X | 14 |
| Hex Buffer/Driver with High Voltage OC* | '07 | X | X |  |  |  |  |  |  | 14 |
|  | '17 | X | X |  |  |  |  |  |  | 14 |
| Hex Inverting Buffer/Driver with High Voltage OC* | '06 | X | X |  |  |  |  |  |  | 14 |
|  | '16 | X | X |  |  |  |  |  |  | 14 |
| Hex TRI-STATE Buffer/Bus Driver | '365 | X |  |  |  |  |  | X | X | 16 |
|  | '367 | X |  |  |  |  |  | X | X | 16 |
| Hex Inverting TRI-STATE Buffer/Bus Driver | '368 | X |  |  |  |  |  | X | X | 16 |
|  | '366 |  |  |  |  |  |  | X | X | 16 |
| Octal Buffer/Line Driver with TRI-STATE Outputs | '540 |  |  |  |  |  |  |  | X | 20 |
| Octal TRI-STATE Buffer/Bus Driver | '465 |  |  |  |  |  |  |  | X | 20 |
|  | '467 |  |  |  |  |  |  |  | X | 20 |
| Octal TRI-STATE Inverting Buffer/Bus Driver | '466 |  |  |  |  |  |  |  | X | 20 |
|  | '468 |  |  |  |  |  |  |  | X | 20 |
| Octal TRI-STATE Buffer/Line Driver/Line Receiver | '241 |  |  |  |  | X | X | X | X | 20 |
|  | '244 |  |  |  |  | X | X | X | X | 20 |
| Octal TRI-STATE Inverting Buffer/Line Driver/Line Receiver | '240 |  |  |  |  | X | X | X | X | 20 |
|  | '243 |  |  |  |  |  |  |  | X | 14 |
| Octal TRI-STATE Bus Transceiver | '245 |  |  |  |  |  |  | X | X | 20 |
|  | '645 |  |  |  |  |  |  |  | X | 20 |


| Monostables (One-Shots) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Function/Description | Type | Technology |  |  |  |  |  |  |  | No. of Inputs |  | Resettable |  | No. of Pins |
|  |  | $\begin{aligned} & \text { STD } \\ & \text { TTL } \end{aligned}$ |  | L |  | S |  | LS |  |  |  |  |  |  |
|  |  | 54 | 74 | 54 | 74 | 54 | 74 | 54 | 74 | Pos. | Neg. |  |  |  |
| Single Retriggerable | 9601 | X | X |  |  |  |  |  |  | 2 | 2 |  | 50 | 14 |
|  | '122 | X | X |  |  |  |  |  |  | 2 | 2 | X | 45 | 14 |
|  | '122 |  |  |  |  |  |  |  | X | 2 | 2 |  | 40 | 14 |
| Single NonRetriggerable | '121 | X | X |  |  |  |  |  |  | 1 | 2 |  | 40 | 14 |
| Dual Retriggerable | 9602 | X | X | X |  |  |  |  |  | 1 | 1 | X | 72 | 16 |
|  | 96S02 |  |  |  |  |  | X |  |  | 1 | 1 | X | 27 | 16 |
|  | 96LS02 |  |  |  |  |  |  | X | X | 1 | 1 | X | 35 | 16 |
|  | '123 | X | X |  |  |  |  |  |  | 1 | 1 | X | 45 | 16 |
|  | '123 |  |  |  |  |  |  |  | X | 1 | 1 | X | 40 | 16 |
| Dual NonRetriggerable | '221 |  |  |  |  |  |  |  | X | 1 | 1 | X | 40 | 16 |

Multiplexers

| Function/Description | Type | Technology |  |  |  |  |  |  |  | Enable Inputs | True Outputs | Complementary Outputs | No. of Pins |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\begin{aligned} & \text { STD } \\ & \text { TTL } \end{aligned}$ |  | L |  | S |  | LS |  |  |  |  |  |
|  |  | 54 | 74 | 54 | 74 | 54 | 74 | 54 | 74 |  |  |  |  |
| Quad 2-Input | 9322 | X | X | X |  |  |  |  |  | 1 | x |  | 16 |
|  | '157 | X | X |  |  | X | X | X | X | 1 | X |  | 16 |
|  | '158 |  |  |  |  | X | X | X | X | 1 |  | X | 16 |
|  | '257 |  |  |  |  | X | X | X | - X | 1 | TRI-STATE |  | 16 |
|  | '258 |  |  |  |  | X | X | X | X | 1 |  | TRI-STATE | 16 |
|  | '298 | $x$ |  |  |  |  |  | X | X | Clocked | $x$ |  | 16 |
| Dual 4-Input | '153 | X | X |  |  | X | x | X | x | 2 | X |  | 16 |
|  | '253 |  |  |  |  | X | X | $x$ | $x$ | 2 | TRI-STATE |  | 16 |
|  | '352 |  |  |  |  |  |  | X | X | 2 |  | X | 16 |
|  | '353 |  |  |  |  |  |  | X | X | 2 |  | TRI-STATE | 16 |
|  | 9309 | X | X | X |  |  |  |  |  |  | X | X | 16 |
| 8-Input | '151 | X | X |  |  | x | X | X | X | 1 | X | X | 16 |
|  | '251 |  |  |  |  | X | X | X | X | 1 | TRI-STATE | TRI-STATE | 16 |
|  | '152 |  |  |  |  |  |  | X |  |  |  | X | 14 |
|  | 9312 | X | X | X |  |  |  |  |  | 1 | X | X | 16 |
| Quad 2-Input TRI-STATE | 7123 | X |  |  |  |  |  |  |  | 1 | X |  | 16 |
| 16-Input | '150 | X | X |  |  |  |  |  |  | 1 |  | X | 24 |


| Registers |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Function/Description |  | Type | Technology |  |  |  |  |  |  |  | No. of Bits | Serial <br> Entry | Parallel Entry No. of Bits | Clock Edge | No. of Pins |
|  |  | $\begin{aligned} & \text { STD } \\ & \text { TTL } \end{aligned}$ | L |  | S |  | LS |  |  |  |  |  |  |
|  |  | 54 | 74 | 54 | 74 | 54 | 74 | 54 | 74 |  |  |  |  |  |
| Parallel In/Parallel Out Shift Right |  |  | 9300 | X | X | X |  |  | X |  |  | 4 | J, $\bar{K}$ | 4S | $\sim$ | 16 |
|  |  | '95 | X | X | X |  |  |  | X | X | 4 | D | 4S | $\checkmark$ | 14 |
|  |  | '195 |  |  |  |  | x | X | x | x | 4 | J, $\bar{K}$ | 4S | $\checkmark$ | 16 |
| Parallel In/Parallel Out Shift Right (TRI-STATE) |  |  | '295 |  |  |  |  |  |  | X | X | 4 | D | 4S | $\checkmark$ | 14 |
|  |  | '395 |  |  |  |  |  |  | X | X | 4 | D | 4S | 入 | 16 |
| Parallel In/Parallel Out <br> Bidirectional |  | '194 | X |  |  |  | x | X | X | X | 4 | DR, DL | 4S | $\sim$ | 16 |
| Quad D |  | '173 | X | X |  |  |  |  | X | X | 4 |  | 4S | $\checkmark$ | 16 |
|  |  | '379 |  |  |  |  |  |  | x | X | 4 |  | 4S | $\checkmark$ | 16 |
| Quad 2 Port Register |  | '298 | X |  |  |  |  |  | X | X | 4 |  | 2 D (Mux) | $\checkmark$ | 16 |
| Parallel D Register |  | '378 |  |  |  |  |  |  | X | X | 6 |  | 6 S | $\sim$ | 16 |
| Multiport Register |  | 9338 | X | X |  |  |  |  |  |  | 8 | D |  | $\Omega$ | 16 |
| Serial/Parallel In, Parallel, Serial Out, Shift Right |  | '322 |  |  |  |  |  |  | x | X | 8 | 2D | 8 S | $\checkmark$ | 20 |
| Serial In/Parallel Out, Shift Right |  | '164 | X | X |  |  |  |  | X | X | 8 | 2D |  | $\sim$ | 14 |
| Parallel/Serial In, Serial Out, Shift Right |  | '165 | x | X |  |  |  |  | X | X | 8 | D | 8A | $\checkmark$ | 16 |
|  |  | '166 | X |  |  |  |  |  |  | X | 8 | D | 8 S | $\Gamma$ | 16 |
| Successive Approx. Register |  | '502 |  |  |  |  |  |  | X | X | 8 | D |  | $\Omega$ | 16 |
|  |  | '503 |  |  |  |  |  |  | X | X | 8 | D |  | $\Gamma$ | 16 |
|  |  | 2503 | X |  |  |  |  |  |  |  | 8 | D |  | $\sim$ | 16 |
| Parallel In/Parallel Out Bidirectional <br> (TRI-STATE) |  | '299 |  |  |  |  |  | X | X | X | 8 | DR, DL | 8 S | $\Gamma$ | 20 |
|  |  | '323 |  |  |  |  |  |  | X | X | 8 | DR, DL | 8 8 | $\checkmark$ | 20 |
| Serial In/Serial Out, Shift Right |  | 9328 | x | x | X |  |  |  |  |  | $2 \times 8$ | $2 \times 2 \mathrm{D}$ <br> Mux |  | $\Gamma$ | 16 |
| Octal D Register |  | '273 |  |  |  |  |  |  | X | X | 8 |  | 8 S | $\checkmark$ | 20 |
| Register File | (OC*) | '170 | X | X |  |  |  |  | X | X | $4 \times 4$ |  | 4A | $\sim$ | 16 |
|  | (TRI-STATE) | '670 |  |  |  |  |  |  | X | X | $4 \times 4$ |  | 4A | $\checkmark$ | 16 |
| 8-Bit Shift Register (TRI-STATE) |  | '952 |  |  |  |  |  |  |  | X | 8 |  |  | $\checkmark$ | 18 |
|  |  | '962 |  |  |  |  |  |  |  | X | 8 |  |  | $\Gamma$ | 18 |
| Data Selector/Storage Register |  | '98 |  |  | X |  |  |  |  |  | 4 |  | 2 D (Mux) | $\checkmark$ | 16 |
| *S = Synchronous, A = Asynchronous, OC : Open Collector |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## DC Operating Conditions and Characteristics

## GENERAL DEFINITIONS

I: Current is the flow of electric charge from one potential to another through a conductor. The unit of measure is the Ampere, or Amp, abbreviated A. One Amp is equal to the current flowing through one ohm of resistance when one volt is applied across that resistance. Common units found in the semiconductor industry are the milliampere, abbreviated mA , equal to 0.001 A and the microampere, abbreviated $\mu \mathrm{A}$, equal to 0.000001 A . Negative current is defined as current flowing out of a device terminal and positive current is defined as current flowing into a device terminal.
V: Voltage, or the electromotive force which causes current to flow through a conductor. One Ampere of current flowing through one ohm of resistance develops a potential difference of one volt across that resistance. The unit of measure is the Volt, abbreviated V , and a common unit is the millivolt, abbreviated mV , equal to 0.001 V .

## INPUT CURRENT PARAMETERS

I, Maximum High Level Input Current: Current flowing into an input when that input has the maximum voltage specified for the family applied to it. This test is used to guarantee the minimum reverse breakdown voltage of the input structure.
$I_{\text {IH }}$ High Level Input Current: The current flowing into an input when that input has a high level voltage equal to the minimum high level output voltage specified for the family. This test is used to check the emitter-to-emitter leakage and the inverse transistor action of a multi-emitter transistor input, the input leakage of a diode, PNP transistor, or C-B short type of input, and to guarantee the fan-in specified for the family.
$I_{\text {IK }}$ Input Clamp Current: The current flowing out of an input when that input is pulled below ground. This test is used to guarantee the integrity of the input clamp diode. The input clamp diode is used to limit the voltage swings on the input by clamping the negative excursions to a level equal to one diode drop below ground. This serves to reduce ringing on an incoming signal. Pulling the input below ground for an extended length of time can cause parasitic transistor action to occur between adjacent tanks on the die which can cause erroneous data to occur on the outputs of the device. To prevent this, voltages on the inputs during operation (other than high speed ringing) should be limited to no more than 0.5 V below ground at all times.
IIL Low Level Input Current: The current flowing out of an input when a low level voltage equal to the maximum low level output voltage specified for the family is applied to the input. This test is used to check the input pullup resistor on an MET or a diode input and to guarantee the specified fanin of the family.
$\mathbf{I}_{\mathbf{T}}+$ Current at Positive-Going Threshold Point: The current flowing out of a transition-operated (Schmitt trigger) input when a voltage equal to the positive going threshold voltage is applied to the input.
$\mathbf{I}_{\mathbf{T}}$ - Current at Negative-Going Threshold Point: The current flowing out of a transition-operated (Schmitt trigger) input when a voltage equal to the negative going threshold voltage is applied to the input.

## OUTPUT CURRENT PARAMETERS

ICEX Output Leakage Current: The current flowing into an open collector output when input conditions have been applied that, according to the product specification, will cause the output to be in the logic high state. This test checks the reverse breakdown of the output transistor.
$\mathrm{I}_{\mathrm{O}}$ (off) Off-State Output Current: The current flowing into an output with input conditions applied that, according to the product specification, will cause the output switching element to be in the off state.
NOTE: This parameter is usually specified for open collector outputs intended to drive devices other than logic circuits, such as displays. Any leakage current applied to a display may cuase the display to be activated.
$\mathbf{I O H}$ High Level Output Current: The current flowing out of an output with input conditions applied that, according to the product specification, will establish a logic high level at the output. This test guarantees the current sourcing (drive) capability of the output and the fan-out specified for the family.
IOL Low Level Output Current: The current flowing into an output with input conditions applied that, according to the product specification, will establish a logic low level at the output. This test guarantees the current sinking capability of the output and the fan-out specified for the family.
Ios Output Short-Circuit Current: The current out of an output when that output is shorted to ground, or another specified potential, with input conditions applied that, according to the product specification, will establish a logic high level at the output.
Ioz High-Impedance State Output Current: These tests guarantee that the device will not excessively load a bus line when the device output is put into the TRI-STATE ${ }^{\text {® }}$ mode.
$I_{\text {OZH }}$ (or ISINK): The current flowing into an output with input conditions applied to the output control pin such that the output is in the high impedance state and input conditions applied to the other inputs that, according to the product specification, will establish a logic low level at the output.
lozl(or ISOURCE): The current flowing out of an output with input conditions applied to the output control pin such that the output is in the high impedance state and input conditions applied to the other inputs that, according to the product specification, will establish a logic high level at the output.

## SUPPLY CURRENT PARAMETERS

$I_{\text {CCH }}$ Supply Current (outputs in the high state): The current flowing into the $V_{C C}$ terminal of a device with input conditions applied that, according to the product specification, will establish a logic high level at the output(s).
ICCL Supply Current (outputs in the low state): The current flowing into the $V_{C C}$ terminal of a device with input conditions applied that, according to the product specification, will establish a logic low level at the output(s).

## DC Operating Conditions and Characteristics (Continued)

Iccz Supply Current (outputs in the high-impedance state): The current flowing into the $\mathrm{V}_{\mathrm{CC}}$ terminal of a device with input conditions applied that, according to the product specification, will establish a high impedance state at the output.

## INPUT VOLTAGE PARAMETERS

$\mathrm{BV}_{\text {IN }}$ Input Breakdown Voltage: The maximum voltage that the device is guaranteed to be able to withstand without exceeding the maximum input current specification.
$\mathbf{V}_{\mathbf{F}}$ Input Forward Voltage: The voltage applied to the input of a device that causes the input structure to become forward biased; usually equal to the maximum output low voltage specified for the family.
$\mathbf{V}_{\mathbf{I H}}$ High Level Input Voltage: The minimum positive voltage level that can be applied to an input terminal of a device and be recognized as a logic high level.
$V_{\text {IK }}$ Input Clamp Voltage: The input clamp voltage specification checks the quality of the input diode whose purpose is to damp out ringing. This is not intended to be an operating condition and if this voltage is allowed to persist for any length of time, parasitic transistor action will occur between adjacent geometry tanks and circuit performance will be degraded, in some cases to the point of failure.
$\mathbf{V}_{\mathrm{IL}}$ Low Level Input Voltage: The maximum positive voltage level that can be applied to an input terminal of a device and be recognized as a logic low level.
$\mathbf{V}_{\mathbf{R}}$ Input Reverse Voltage: The voltage applied to an input of a device that causes the input structure to become reverse biased; usually equal to the minimum high level output voltage specified for the family.
$\mathbf{V}_{\mathbf{T}}+$ Positive-Going Threshold Voltage: The voltage level at a transition-operated (Schmitt trigger) input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, $\mathrm{V}_{\mathrm{T}}-$.
$\mathbf{V}_{\mathbf{T}}$ - Negative-Going Threshold Voltage: The voltage level at a transition-operated (Schmitt trigger) input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, $\mathrm{V}_{\mathrm{T}}+$.

## OUTPUT VOLTAGE PARAMETERS

$V_{\text {OH }}$ High Level Output Voltage: The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.
Vol Low Level Output Voltage: The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.
Vo(off) Off-State Output Voltage: The voltage at an output terminal with input conditions applied that, according to the product specification, will cause the output switching element to be in the off state.
NOTE: This characteristic is usually specified only for outputs without internal pull-up elements intended for driving devices other than logic circuits.
$V_{0}(o n)$ On-State Output Voltage: The voltage at an output terminal with input conditions applied that, according to the product specification, will cause the output switching element to be in the on state.
NOTE: This characteristic is usually specified only for outputs without internal pull-up elements intended for driving devices other than logic circuits.

## AC Operating Conditions and Characteristics

## INPUT PARAMETERS

$f_{\text {max }}$ Maximum Clock Frequency: The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic levels at the output with input conditions established that should cause changes of output logic level in accordance with the specification. Unless otherwise specified, this test is performed with no restrictions on input rise and fall times or duty cycle.
NOTE: A minimum value is specified that is the highest frequency at which all devices are guaranteed to function correctly.
$t_{H}$ Hold Time: The interval during which a signal must be maintained at a given data input after an active transition at another given input.
NOTE: A minimum value is specified that is the smallest time interval above which all devices are guaranteed to function correctly.
$\mathbf{t}_{\mathbf{W}}$ Pulse Width: The time interval between specified voltage reference points on the leading and trailing edges of a pulse waveform.
NOTE: A minimum value is specified that is the smallest time interval at which correct operation of the logic element is guaranteed.
$\mathbf{t}_{\text {REC }}$ Recovery Time: The time interval needed to switch a memory-type device from a write mode to a read mode and to obtain valid data signals at the output.
NOTE: A minimum value is specified that is the smallest time interval at which correct operation of the device is guaranteed.
$t_{\text {REL }}$ Release Time: The time interval between one control input going inactive and another input going active after which the inactive input no longer has any influence on the device operation.
NOTE: A minimum value is specified that is the smallest time interval at which correct operation of the logic element is guaranteed.
ts $_{\text {S }}$ Set-Up Time: The time interval during which a stable signal must be maintained at a specified input terminal before an active transition at another specified input terminal.
NOTE: A minimum value is specified that is the smallest time interval at which correct operation of the logic element is guaranteed.
$\mathbf{t}_{\mathbf{R}}$ Rise Time: The time interval between a specified lowlevel voltage and a specified high-level voltage on a waveform that is changing from a defined low level to a defined high level. Common defined levels are from $10 \%$ of the signal amplitude to $90 \%$ of the signal amplitude.
$\mathbf{t}_{\mathbf{F}}$ Fall Time: The time interval between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from a defined high level to a defined low level. Common defined levels are from $90 \%$ of the signal amplitude to $10 \%$ of the signal amplitude.

## OUTPUT PARAMETERS

tpzH $^{\text {Pr }}$ Output Enable Time to a High Logic Level: The propagation delay time between the specified voltage reference points on the input and output waveforms with a TRISTATE output changing from a high impedance (off) state to the defined high state.
$t_{\text {PzL }}$ Output Enable Time to a Low Logic Level: The propagation delay time between the specified voltage reference points on the input and output waveforms with a TRI-STATE output changing from a high impedance (off) state to the defined low state.
$t_{\text {Phz }}$ Output Disable Time from a High Logic Level: The propagation delay time between the specified voltage reference points on the input and output waveforms with a TRISTATE output changing from the defined high state to the high impedance (off) state .
$t_{p L z}$ Output Disable Time from a Low Logic Level: The propagation delay time between the specified voltage reference points on the input and output waveforms with a TRISTATE output changing from the defined low state to the high impedance (off) state .
$\mathbf{t}_{\text {wout }}$ Output Pulse Width: The time interval between specified voltage reference points on the leading and trailing edges of an output waveform.
NOTE: This is usually only specified for monostable elements.
$t_{\text {PLH }}$ Propagation Time, Low to High: The time between the specified voltage reference points on the input and output waveforms with the output changing from a low logic level to a high logic level.
$t_{\text {phL }}$ Propagation Delay, High to Low: The time between the specified voltage reference points on the input and output waveforms with the output changing from a high logic level to a low logic level.
$\mathbf{t}_{\text {TLH }}, \mathbf{t}_{\mathbf{r}}$ Transition Time, or Rise Time: The time interval between a specified low-level voltage and a specified highlevel voltage on a waveform that is changing from a defined low level to a defined high level. Common defined levels are from $10 \%$ of the signal amplitude to $90 \%$ of the signal amplitude, or from 0.6 V to 2.6 V .
$\boldsymbol{t}_{\mathbf{T H L}}, \mathrm{t}_{\mathbf{f}}$ Transition Time, or Fall Time: The time interval between a specified high-level voltage and a specified lowlevel voltage on a waveform that is changing from a defined high level to a defined low level. Common defined levels are from $90 \%$ of the signal amplitude to $10 \%$ of the signal amplitude, or from 2.6 V to 0.6 V .
Note A: All AC Specifications are for one output switching at a time.

## EXPLANATION OF DEVICE FUNCTIONS

## Circuit Complexity

SSI: Small Scale Integration; the lowest level of complexity in integrated circuits.
MSI: Medium Scale Integration; small subsystems integrated into a single microcircuit.
LSI: Large Scale Integration; large subsystems or small systems integrated into a single microcircuit.

## FUNCTIONAL DESCRIPTIONS

Buffer: A logic gate with high output drive capability, or fanout. Buffers are used where a single circuit must drive a large number of loads.
Comparator: A logic circuit that will compare two separate input signals and produce an output based on that comparison. A simple comparator is the Exclusive-NOR gate, which produces a high level output only when its two inputs are identical.
Counter: A logic circuit that counts the number of input pulses it receives. Counters can be used for frequency division, counting, and sequencing digital operations. Common counter configurations are Binary, where the device counts from 0 to 15 and Decade, where the device counts from 0 to 9 .

## AC Operating Conditions and Characteristics (Continued)

Data Selector/Multiplexer: A logic circuit that will select one of several input signals and feed that signal onto a common bus line. It can be thought of as a multipole, multiposition switch with each switch pole representing one output and each switch position representing one input.
Decoder/Demultiplexer: A logic circuit that is the complement of the Data Selector/Multiplexer; that is, this circuit takes an input signal and feeds it to any one of several output lines depending on the information placed on its steering, or control, inputs.
Driver: Same as Buffer, above.
Flip-Flop: A logic circuit that is used to store information. A flip-flop is called "bistable" since it has two stable states.
Gate: The basic building block of all logic circuits; an element whose output is a Boolean function of its inputs. The basic functions are the AND, OR, and NOT. By combining these functions, NAND, NOR, and Exclusive-OR and Exclu-sive-NOR gates are built.
Latch: A bistable element that latches, or holds, data which is present at its input at the time the Enable input goes to its inactive state. When the Enable input is active, the data, present at the input, is passed directly to the output, similar to the operation of a gate.
One-Shot: Monostable multivibrator; a flip-flop that only has one stable state. When triggered by an input transient, it flips to its unstable state for a time period determined by an external R-C network connected to its timing inputs, and then returns to its stable state.
Shift Register: A series of flip-flops in which the data signal is shifted out of one flip-flop and into the succeeding flip-flop during an active transition on the clock input.
Transceiver: A logic circuit that can transmit data onto a bus line and receive data off of the bus line using the same terminal as an input and output. The direction of signal flow is determined by logic levels present at a Direction Control input.

## OTHER TERMS

Asynchronous: A mode of operation that does not require any specific timing relationship between different control inputs.
Open Collector: Output configuration that has no internal pullup. This configuration enables outputs that are connected together (wired-OR) to assume opposite states without incurring damage.
Schmitt Trigger: An input configuration that has a different threshold point depending on whether the input signal is rising or falling. This is especially useful in electrically noisy environments.
Synchronous: A mode of operation where specific timing requirements must be met between control inputs before an indicated action can occur.
Totem Pole: An output configuration that contains an internal pullup structure, usually a transistor pullup allowing higher output drive capability than is available with open collector outputs.

TRI-STATE: A registered trademark for a circuit configuration in which the device can be switched 'off' during which time the output presents a very high impedance to the bus it is connected to. This allows multiple outputs to be connected to a bus line while only one output drives the line, the other outputs being switched into their high impedance states.

## EXPLANATION OF FUNCTION TABLES

The following symbols are used in the function tables found in NSC data sheets:

| H | = high logic level (steady state) |
| :---: | :---: |
| L | = low logic level (steady state) |
| $\uparrow$ | = transition from low to high logic level |
| $\downarrow$ | $=$ transition from high to low logic level |
| X | = irrelevant (any level, including transitions) |
| Z | $=$ off (high impedance) state of a TRI-STATE output |
|  | $=$ the level of steady state inputs at inputs $A$ through H respectively |
| $Q_{0}$ | $=$ the level of $Q$ before the indicated steady state input conditions were established |
| $\bar{Q}_{0}$ | $=$ complement of $Q_{0}$ or level of $Q$ before the indicated steady state input conditons were established |
| $Q_{n}$ | $=$ level of $Q$ before the most recent active transition indicated by $\uparrow$ or $\downarrow$ |
| $\Omega$ | $=$ one high level pulse |
|  | = one low level pulse |

toggle $=$ each output changes to the complement of its previous level on each active transition indicated by $\uparrow$ or $\downarrow$
If, in the input columns, a row contains only the symbols H , $L$, and/or $X$, this means the indicated output is valid whenever the input configuration is achieved regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.
If, in the input columns, a row contains $\mathrm{H}, \mathrm{L}$, and/or X together with $\uparrow$ and/or $\downarrow$, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady state levels. If the output is shown as a level $\left(H, L, Q_{0}\right.$, or $\bar{Q}_{0}$ ), it persists so long as the steady state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect on the output. If the output is shown as a pulse, $\Omega$ or $\tau$, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.
Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. As an example, Figure 1 is the function table for a 4-bit bidirectional universal shift register, similar to the DM54LS194.
The first line of the table represents "asynchronous" clearing of the register and indicates that if CLEAR is low, all four outputs will be reset low regardless of the states of the other inputs. In the succeeding lines, CLEAR is inactive (high) and consequently has no effect.

## AC Operating Conditions and Characteristics (Continued)

The second line indicates that so long as the CLOCK input remains low (while CLEAR is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of CLEAR high and CLOCK low was established. Since on all the other lines of the table only the rising edge of the CLOCK is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the CLOCK remains high or on the high-to-low transition of the CLOCK.
The third line of the table represents "synchronous" parallel loading of the register and indicates that if S1 and S0 are both high, then regardless of the levels at the SERIAL inputs, the data present at A will transfer to QA, the data present at B will transfer to QB, and so forth, following a low-to-high transition on CLOCK.
The fourth and fifth lines represent the "synchronous" loading of high and low level data, respectively, from the SHIFT RIGHT SERIAL input and the shifting one bit to the right of previously entered data; data previously at QA is now at QB, data previously at QB and QC is now at QC and QD respec-
tively, and the data previously at QD has been shifted out of the register. This entry of data and shifting takes place on the low-to-high level transition of CLOCK when S1 is low and $S 0$ is high and as shown, the levels at the PARALLEL inputs, A through D, have no effect.
The sixth and seventh lines represent the "synchronous" loading of high and low level data respectively, from the SHIFT LEFT SERIAL input and the shifting one bit to the left of previously entered data; data previously at QD is now at QC, data previously at QC and QB is now at QB and QA respectively, and the data previously at QA has been shifted out of the register. This entry of serial data and shifting to the left takes place on the low-to-high level transition of CLOCK when S1 is high and S0 is low and as seen, the levels at the PARALLEL inputs, $A$ through $D$, have no effect. The last line indicates that so long as both MODE inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady state combination of CLEAR high and both MODE inputs low was established.

| Clear | Mode |  | Inputs |  |  |  |  |  |  | Outputs |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Clock | Serial |  | Parallel |  |  |  |  |  |  |  |
|  | S1 | So |  | Left | Right | A | B | C | D | $\mathbf{Q}_{\mathbf{A}}$ | $\mathbf{Q}_{\mathbf{B}}$ | $Q_{C}$ | $\mathbf{Q}_{\mathbf{D}}$ |
| L | X | X | X | X | $X$ | X | X | X | $x$ | L | L | L | L |
| H | X | X | L | X | X | X | $x$ | X | X | $Q_{A O}$ | $Q_{B 0}$ | $Q_{\text {co }}$ | $Q_{\text {Do }}$ |
| H | H | H | $\uparrow$ | X | X | a | b | c | d | a | b | c | d |
| H | L | H | $\uparrow$ | X | H | X | X | X | X | H | $Q_{\text {An }}$ | $Q_{B n}$ | $Q_{C n}$ |
| H | L | H | $\uparrow$ | X | L | X | X | X | X | L | $Q_{\text {An }}$ | $Q_{B n}$ | $Q_{C n}$ |
| H | H | L | $\uparrow$ | H | X | X | X | X | X | $Q_{B n}$ | $Q_{C n}$ | $Q_{D n}$ | H |
| H | H | L | $\uparrow$ | L | $x$ | X | X | X | X | $Q_{B n}$ | $Q_{C n}$ | $Q_{D n}$ | L |
| H | L | L | X | X | X | X | X | X | X | $Q_{A 0}$ | $\mathrm{Q}_{\mathrm{BO}}$ | $Q_{C 0}$ | $Q_{\text {D0 }}$ |

FIGURE 1. Function Table

## DM54/74, 54S/74S Test Waveforms

Parameter Measurement Information


Note A: $\mathrm{C}_{\mathrm{L}}$ includes probe and jig capacitance.
Note B: All diodes are 1N916 or 1N3064.


$$
\begin{aligned}
& 54 / 74 \mathrm{t}_{\mathrm{r}} \leq 7 \mathrm{~ns} ; \mathrm{t}_{\mathrm{f}} \leq 7 \mathrm{~ns} \\
& 54 \mathrm{~S} / 74 \mathrm{~S} \mathrm{t}_{\mathrm{r}} \leq 2.5 \mathrm{~ns}, \mathrm{t}_{\mathrm{f}} \leq 2.5 \mathrm{~ns} \\
& \text { Generator: } Z_{\text {OUT }} \approx 50 \Omega \\
& \quad \text { PRR } \leq 1 \mathrm{MHz}
\end{aligned}
$$



Voltage Waveforms Propagation Delay Times


TL/X/0003-7


TL/X/0003-8
Note C: Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
Note D: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
Note E: When measuring propagation delay times of TRI-STATE outputs, switches S1 and S2 are closed.

## DM54L/DM54LS/74LS Test Waveforms

Parameter Measurement Information


Note $A: C_{L}$ includes probe and jig capacitance.
Note B: All diodes are 1N916 or 1N3064.
Note C: C1 ( 30 pF ) is used for testing Series 54L/74L devices only.

## Input Waveform



54LS/74LS: $\mathrm{t}_{\mathrm{r}} \leq 6 \mathrm{~ns}, \mathrm{t}_{\mathrm{f}} \leq 6 \mathrm{~ns}$
54 L gates and inverters: $\mathrm{t}_{\mathrm{r}} \leq 60 \mathrm{~ns}, \mathrm{t}_{\mathrm{f}} \leq 60 \mathrm{~ns}$
54 L flip-flops and MSI: $\mathrm{t}_{\mathrm{r}} \leq 25 \mathrm{~ns}, \mathrm{t}_{\mathrm{f}} \leq 25 \mathrm{~ns}$
Generator: Z OUT $\approx 50 \Omega$ PRR $\leq 1 \mathrm{MHz}$


DM54L/DM54LS/74LS Test Waveforms (Continued)
Parameter Measurement Information (Continued)

Voltage Waveforms Propagation Delay Times


TL/X/0003-16

Voltage Waveforms Enable and Disable Times, TRI-STATE Outputs


TL/X/0003-17
Note D: Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
Note E: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
Note F: When measuring propagation delay times of TRI-STATE outputs, switches S1 and S2 are closed.

Section 2
Low Power Schottky

## Section 2-Low Power Schottky

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## 54LS00/DM54LS00/DM74LS00

Quad 2-Input NAND Gates

## General Description

This device contains four independent gates each of which performs the logic NAND function.

## Features

- Alternate Military/Aerospace device (54LSOO) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.


## Connection Diagram

Dual-In-Line Package


TL/F/6439-1
Order Number 54LS00DMQB, 54LS00FMQB, 54LS00LMQB, DM54LS00J, DM54LS00W, DM74LS00M or DM74LS00N See NS Package Number E20A, J14A, M14A, N14A or W14B
Function Table
$\mathbf{Y}=\overline{\mathbf{A} \mathbf{B}}$

| Inputs |  | Output |
| :---: | :---: | :---: |
| $\mathbf{A}$ | $\mathbf{B}$ | $\mathbf{Y}$ |
| L | L | H |
| L | H | H |
| H | L | H |
| H | $H$ | L |

$H=$ High Logic Level
$\mathrm{L}=$ Low Logic Level

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.


## Recommended Operating Conditions

| Symbol | Parameter | DM54LS00 |  |  | DM74LS00 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| IOH | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| IOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & V_{C C}=M i n, I_{O H}=M a x, \\ & V_{I L}=M a x \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\text {OL }}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max}, \\ & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{IOL}=4 \mathrm{~mA}$, | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $\mathrm{V}_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
|  | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.36 | mA |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & (\text { Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICCH | Supply Current with Outputs High | $V_{C C}=$ Max |  |  | 0.8 | 1.6 | mA |
| $\mathrm{I}_{\text {CCL }}$ | Supply Current with Outputs Low | $V_{C C}=$ Max |  |  | 2.4 | 4.4 | mA |

Switching Characteristics at $\mathrm{V}_{C C}=5 V_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $C_{L}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| tplH | Propagation Delay Time Low to High Level Output | 3 | 10 | 4 | 15 | ns |
| tPHL | Propagation Delay Time High to Low Level Output | 3 | 10 | 4 | 15 | ns |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

## 54LS02/DM54LS02/DM74LS02 <br> Quad 2-Input NOR Gates

## General Description

This device contains four independent gates each of which performs the logic NOR function.

## Features

- Alternate Military/Aerospace device (54LS02) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications


## Connection Diagram

Dual-In-LIne Package


Order Number 54LS02DMQB, 54LS02FMQB, 54LS02LMQB, DM54LS02J, DM54LS02W, DM74LS02M or DM74LS02N See NS Package Number E20A, J14A, M14A, N14A or W14B

## Function Table

$$
\mathbf{Y}=\overline{\mathbf{A}+\mathbf{B}}
$$

| Inputs |  | Output |
| :---: | :---: | :---: |
| $\mathbf{A}$ | $\mathbf{B}$ | $\mathbf{Y}$ |
| L | L | $H$ |
| L | $H$ | L |
| $H$ | L | L |
| $H$ | $H$ | L |

$H=$ High Logic Level
$L=$ Low Logic Level

```
Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for avallabllity and specifications.
Supply Voltage
Input Voltage
7V
Operating Free Air Temperature Range
```

DM54LS and 54LS
DM74LS
Storage Temperature Range

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS02 |  |  | DM74LS02 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{C C}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| $\mathrm{IOH}^{\text {l }}$ | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | $\begin{gathered} \text { Typ } \\ \text { (Note 1) } \end{gathered}$ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| VOL | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\ & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 |  |
|  |  |  | DM74 |  | 0.35 | 0.5 | V |
|  |  | $\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{I}_{\mathrm{H}}$ | High Level Input Current | $V_{C C}=\operatorname{Max}, V_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| ILL | Low Level Input Current | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.40 | mA |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=\text { Max } \\ & \text { (Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| $\mathrm{I}_{\mathrm{CCH}}$ | Supply Current with Outputs High | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 1.6 | 3.2 | mA |
| ICCL | Supply Current with Outputs Low | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 2.8 | 5.4 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output |  | 13 |  | 18 | ns |
| tpHL | Propagation Delay Time High to Low Level Output |  | 10 |  | 15 | ns |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

## 54LS03/DM54LS03/DM74LS03 <br> Quad 2-Input NAND Gates with Open-Collector Outputs

## General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

## Features

- Alternate Military/Aerospace device (54LSO3) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.


## Pull-Up Resistor Equations

$R_{\text {MAX }}=\frac{V_{C C}(M i n)-V_{O H}}{N_{1}\left(I_{O H}\right)+N_{2}\left(I_{H}\right)}$
$R_{\text {MIN }}=\frac{V_{C C}(M a x)-V_{O L}}{I_{O L}-N_{3}\left(I_{L L}\right)}$
Where: $\mathrm{N}_{1}\left(\mathrm{IOH}_{\mathrm{OH}}\right)=$ total maximum output high current for all outputs tied to pull-up resistor
$\mathrm{N}_{2}\left(\mathrm{l}_{I H}\right)=$ total maximum input high current for all inputs tied to pull-up resistor
$N_{3}\left(I_{1 L}\right)=$ total maximum input low current for all inputs tied to pull-up resistor

## Connection Diagram

Dual-In-Line Package


TL/F/6344-1
Order Number 54LS03DMQB, 54LS03FMQB, 54LS03LMQB, DM54LS03J, DM54LS03W, DM74LS03M or DM74LS03N See NS Package Number E20A, J14A, M14A, N14A or W14B

## Function Table

| Absolute Maximum Ratings (Note) |
| :--- |
| If Military/Aerospace specified devices are required, |
| please contact the National Semiconductor Sales |
| Office/Distributors for availability and specifications. |
| Supply Voltage |
| Input Voltage |
| Output Voltage |
| Operating Free Air Temperature Range |
| DM54LS and 54LS |
| DM74LS |
| Storage Temperature Range |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS03 |  |  | DM74LS03 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $V_{C C}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| VOH | High Level Output Voltage |  |  | 5.5 |  |  | 5.5 | V |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | $\begin{gathered} \text { Typ } \\ \text { (Note 1) } \\ \hline \end{gathered}$ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $I_{\text {cex }}$ | High Level Output Current | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{V}_{\mathrm{O}}=5.5 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max} \end{aligned}$ |  |  |  | 100 | $\mu \mathrm{A}$ |
| VoL | Low Level Output Voltage | $\begin{aligned} & V_{C C}=\operatorname{Min}, \operatorname{IOL}=\text { Max }, \\ & V_{I H}=\operatorname{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 |  |
|  |  |  | DM74 |  | 0.35 | 0.5 | v |
|  |  | $\mathrm{l}_{\mathrm{LL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{I}_{\mathrm{H}}$ | High Level Input Current | $\mathrm{V}_{C C}=$ Max, $\mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| ILI | Low Level Input Current | $\mathrm{V}_{C C}=$ Max, $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.36 | mA |
| ICCH | Supply Current with Outputs High | $V_{\text {CC }}=$ Max |  |  | 0.8 | 1.6 | mA |
| lCCL | Supply Current with Outputs Low | $V_{\text {CC }}=$ Max |  |  | 2.4 | 4.4 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | 6 | 20 | 20 | 45 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | 3 | 15 | 4 | 20 | ns |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.

## 54LS04/DM54LS04/DM74LS04 Hex Inverting Gates

## General Description

This device contains six independent gates each of which performs the logic INVERT function.

## Features

- Alternate Military/Aerospace device (54LSO4) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.


## Connection Diagram



TL/F/6345-1
Order Number 54LS04DMQB, 54LS04FMQB, 54LS04LMQB, DM54LS04J, DM54LS04W, DM74LS04M or DM74LS04N See NS Package Number E20A, J14A, M14A, N14A or W14B

## Function Table

| $\mathbf{Y}=\overline{\mathbf{A}}$ |  |
| :---: | :---: |
| Input | Output |
| $\mathbf{A}$ | $\mathbf{Y}$ |
| L | H |
| H | L |

$H=$ High Logic Level
$L=$ Low Logic Level

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS04 |  |  | DM74LS04 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\mathrm{IL}}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| $\mathrm{IOH}^{\text {r }}$ | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ <br> (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & V_{C C}=\operatorname{Min}, I_{O H}=M a x, \\ & V_{I L}=M a x \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\ & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{LL}}$ | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.36 | mA |
| los | Short Circuit Output Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ <br> (Note 2) | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | $-20$ |  | -100 |  |
| ICCH | Supply Current with Outputs High | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 1.2 | 2.4 | mA |
| $\mathrm{I}_{\text {CCL }}$ | Supply Current with Outputs Low | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 3.6 | 6.6 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $C_{L}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | 3 | 10 | 4 | 15 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | 3 | 10 | 4 | 15 | ns |

[^0]
## 54LS05/DM54LS05/DM74LS05 Hex Inverters with Open-Collector Outputs

## General Description

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

## Features

- Alternate Military/Aerospace device (54LSO5) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.


## Pull-Up Resistor Equations

$$
\begin{aligned}
R_{\text {MAX }} & =\frac{V_{\mathrm{CC}}(\mathrm{Min})-V_{\mathrm{OH}}}{N_{1}\left(l_{\mathrm{OH}}\right)+N_{2}\left(I_{\mathrm{IH}}\right)} \\
R_{\text {MIN }} & =\frac{V_{\mathrm{CC}}(\mathrm{Max})-V_{\mathrm{OL}}}{I_{\mathrm{OL}}-N_{3}\left(I_{\mathrm{IL}}\right)}
\end{aligned}
$$

Where: $\mathrm{N}_{1}(\mathrm{I} \mathrm{OH})=$ total maximum output high current for all outputs tied to pull-up resistor
$N_{2}\left(l_{1 H}\right)=$ total maximum input high current for all inputs tied to pull-up resistor
$N_{3}\left(I_{L}\right)=$ total maximum input low current for all inputs tied to pull-up resistor

## Connection Diagram

Dual-In-Line Package


TL/F/6346-1
Order Number 54LS05DMQB, 54LS05FMQB, DM54LS05J, DM54LS05W, DM74LS05M or DM74LS05N See NS Package Number E20A, J14A, M14A, N14A or W14B

## Function Table

$$
\mathbf{Y}=\overline{\mathbf{A}}
$$

| Input | Output |
| :---: | :---: |
| $\mathbf{A}$ | $\mathbf{Y}$ |
| L | $H$ |
| $H$ | L |

[^1]L = Low Logic Level

| Absolute Maximum Ratings (Note) |  |
| :--- | ---: |
| Af Milltary/Aerospace specified devices are required, |  |
| please contact the National Semiconductor Sales |  |
| Office/Distributors for availability and specifications. |  |
| Supply Voltage | 7 V |
| Input Voltage | 7 V |
| Output Voltage | 7 V |
| Operating Free Air Temperature Range | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| DM54LS and 54LS | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| DM74LS | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS05 |  |  | DM74LS05 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage |  |  | 5.5 |  |  | 5.5 | V |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | $\begin{gathered} \text { Typ } \\ \text { (Note 1) } \end{gathered}$ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| ICEX | High Level Output Current | $\begin{aligned} & V_{\mathrm{CC}}=M \mathrm{Min}, \mathrm{~V}_{\mathrm{O}}=5.5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ |  |  |  | 100 | $\mu \mathrm{A}$ |
| V OL | Low Level Output Voltage | $\begin{aligned} & V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\ & V_{I H}=\operatorname{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 |  |
|  |  |  | DM74 |  | 0.35 | 0.5 | V |
|  |  | $\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $V_{C C}=M a x, V_{1}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{I}_{\mathrm{H}}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| IIL | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.36 | mA |
| ICCH | Supply Current with Outputs High | $V_{C C}=M a x$ |  |  | 1.2 | 2.4 | mA |
| ICCL | Supply Current with Outputs Low | $V_{C C}=M a x$ |  |  | 3.6 | 6.6 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $C_{L}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | 6 | 20 | 20 | 45 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | 3 | 15 | 4 | 20 | ns |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.

## 54LS08/DM54LS08/DM74LS08 Quad 2-Input AND Gates

## General Description

This device contains four independent gates each of which performs the logic AND function.

## Features

Alternate Military/Aerospace device (54LSO8) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

## Connection Diagram



Order Number 54LS08DMQB, 54LS08FMQB, 54LS08LMQB, DM54LS08J, DM54LS08W, DM74LS08M or DM74LS08N See NS Package Number E20A, J14A, M14A, N14A or W14B

## Function Table

| $Y=A B$ |  |  |
| :---: | :---: | :---: |
| Inputs  Output <br> $\mathbf{A}$ $B$ $Y$ <br> $L$ $L$ $L$ <br> $L$ $H$ $L$ <br> $H$ $L$ $L$ <br> $H$ $H$ $H$ |  |  |

[^2]```
Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for availability and specifications.
Supply Voltage
7V
Input Voltage
\(7 V\)
Operating Free Air Temperature Range
    DM54LS and 54LS
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    DM74LS
        \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
Storage Temperature Range
\(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
```

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS08 |  |  | DM74LS08 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $V_{C C}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| ${ }_{\mathrm{OH}}$ | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\ & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| VOL | Low Level Output Voltage | $\begin{aligned} & V_{C C}=\text { Min, } I_{O L}=\text { Max } \\ & V_{I L}=M a x \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{IOL}^{2}=4 \mathrm{~mA}$, | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| IIL | Low Level Input Current | $V_{C C}=M a x, V_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.36 | mA |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & \text { (Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICCH | Supply Current with Outputs High | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 2.4 | 4.8 | mA |
| ICCL | Supply Current with Outputs Low | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 4.4 | 8.8 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | 4 | 13 | 6 | 18 | ns |
| tPHL | Propagation Delay Time High to Low Level Output | 3 | 11 | 5 | 18 | ns |

Note 1: All typicals are at $V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

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## 54LS09/DM54LS09/DM74LS09

## Quad 2-Input AND Gates with Open-Collector Outputs

## General Description

This device contains four independent gates each of which performs the logic AND function. The open-collector outputs require external pull-up resistors for proper logical operation.

## Features

- Alternate Military/Aerospace device (54LS09) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.


## Pull-Up Resistor Equations

$$
\begin{aligned}
R_{M A X} & =\frac{V_{C C}(M i n)-V_{O H}}{N_{1}\left(l_{O H}\right)+N_{2}\left(I_{H}\right)} \\
R_{M I N} & =\frac{V_{C C}(M a x)-V_{O L}}{I_{O L}-N_{3}\left(I_{I L}\right)}
\end{aligned}
$$

Where: $\mathrm{N}_{1}\left(\mathrm{l}_{\mathrm{OH}}\right)=$ total maximum output high current for all outputs tied to pull-up resistor
$\mathrm{N}_{2}\left(\mathrm{l}_{\mathrm{H}}\right)=$ total maximum input high current for all inputs tied to pull-up resistor
$N_{3}\left(l_{\mathrm{IL}}\right)=$ total maximum input low current for all inputs tied to pull-up resistor

## Connection Diagram

## Dual-In-Line Package



TL/F/6348-1
Order Number 54LS09DMQB, 54LS09FMQB, DM54LS09J, DM54LS09W, DM74LS09M or DM74LS09N See NS Package Number E20A, J14A, M14A, N14A or W14B
Function Table

| $\mathrm{Y}=\mathbf{A B}$ |  |  |
| :---: | :---: | :---: |
| Inputs |  | Output |
| $\mathbf{A}$ | $\mathbf{B}$ | Y |
| $L$ | L | L |
| L | $H$ | $L$ |
| $H$ | $L$ | $L$ |
| $H$ | $H$ | $H$ |

[^3]```
Absolute Maximum Ratings (Note)
If Military/Aerospace speclfied devices are required,
please contact the National Semiconductor Sales
Office/Distributors for avallability and specifications.
Supply Voltage
\(7 V\)
Input Voltage
\(7 V\)
Output Voltage
7V
Operating Free Air Temperature Range
\begin{tabular}{lr} 
DM54LS and 54LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}
```

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS09 |  |  | DM74LS09 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| VCC | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage |  |  | 5.5 |  |  | 5.5 | V |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{C C}=\mathrm{Min}, l_{l}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| ICEX | High Level Output Current | $\begin{aligned} & V_{C C}=\operatorname{Min}, V_{O}=5.5 \mathrm{~V} \\ & V_{I H}=\operatorname{Min} \end{aligned}$ |  |  |  | 100 | $\mu \mathrm{A}$ |
| VoL | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{IIH}^{\text {H}}$ | High Level Input Current | $V_{C C}=\operatorname{Max}, V_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| I/L | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.36 | mA |
| ICCH | Supply Current With Outputs High | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 2.4 | 4.8 | mA |
| ICCL | Supply Current With Outputs Low | $\mathrm{V}_{C C}=\mathrm{Max}$ |  |  | 4.4 | 8.8 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $C_{L}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| ${ }_{\text {tpLH }}$ | Propagation Delay Time Low to High Level Output | 5 | 20 | 8 | 45 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | 4 | 15 | 6 | 27 | ns |

[^4]
## General Description

This device contains three independent gates each of which performs the logic NAND function.

## Features

- Alternate Military/Aerospace device (54LS10) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.


## Connection Diagram

Dual-In-Line Package


TL/F/6349-1
Order Number 54LS10DMQB, 54LS10FMQB, 54LS10LMQB, DM54LS10J, DM54LS10W, DM74LS10M or DM74LS10N
See NS Package Number E20A, J14A, M14A, N14A or W14B
Function Table

$$
\mathbf{Y}=\overline{\mathbf{A B C}}
$$

| Inputs |  |  | Output |
| :---: | :---: | :---: | :---: |
| A | B | C | Y |
| X | X | L | H |
| X | L | X | H |
| L | X | X | H |
| H | H | H | L |

$H=$ High Logic Level
L = Low Logic Level

| Absolute Maximum Ratings (Note) |  |
| :--- | ---: |
| Ab Military/Aerospace specified devices are required, |  |
| please contact the National Semiconductor Sales |  |
| Office/Distributors for availability and specifications. |  |
| Supply Voltage | 7 V |
| Input Voltage | 7 V |
| Operating Free Air Temperature Range | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| DM54LS and 54LS | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| DM74LS | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS10 |  |  | DM74LS10 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\text {CC }}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| $\mathrm{IOH}^{\text {l }}$ | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | $\begin{gathered} \text { Typ } \\ \text { (Note 1) } \end{gathered}$ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| VOH | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| VOL | Low Level Output Voltage | $\begin{aligned} & V_{C C}=\operatorname{Min}, I_{O L}=M a x, \\ & V_{I H}=M i n \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| IIL | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.36 | mA |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & \text { (Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICCH | Supply Current with Outputs High | $\mathrm{V}_{C C}=\mathrm{Max}$ |  |  | 0.6 | 1.2 | mA |
| $\mathrm{I}_{\text {CCL }}$ | Supply Current with Outputs Low | $V_{C C}=M a x$ |  |  | 1.8 | 3.3 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=\mathbf{2 k} \boldsymbol{R}$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| $t_{\text {pLH }}$ | Propagation Delay Time Low to High Level Output | 3 | 10 | 4 | 15 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | 3 | 10 | 4 | 15 | ns |

Note 1: All typicals are at $V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

## 54LS11/DM54LS11/DM74LS11 Triple 3-Input AND Gates

## General Description

This device contains three independent gates each of which performs the logic AND function.

## Features

■ Alternate military/aerospace device (54LS11) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

## Connection Diagram

Dual-In-Line Package


Order Number 54LS11DMQB, 54LS11FMQB, 54LS11LMQB, DM54LS11J, DM54LS11W, DM74LS11M or DM74LS11N
See NS Package Number E20A, J14A, M14A, N14A or W14B

## Function Table

$\mathrm{Y}=\mathrm{ABC}$

| Inputs |  |  | Output |
| :---: | :---: | :---: | :---: |
| A | B | C | Y |
| X | X | L | L |
| X | L | X | L |
| L | X | X | L |
| H | H | H | H |

$H=$ High Logic Level
$L=$ Low Logic Level
$X=$ Either Low or High Logic Level

| Absolute Maximum Ratings (Note) |
| :--- |
| If Military/Aerospace specified devices are required, |
| please contact the National Semiconductor Sales |
| Office/Distributors for availability and specifications. |
| Supply Voltage |
| Input Voltage |
| Operating Free Air Temperature Range |
| DM54LS and 54LS |
| DM74LS |
| Storage Temperature Range |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS11 |  |  | DM74LS11 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $V_{C C}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\mathrm{IL}}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| $\mathrm{IOH}^{\text {l }}$ | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOH}_{\mathrm{OH}}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{I}_{\mathrm{H}}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| IIL | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.36 | mA |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & \text { (Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICCH | Supply Current with Outputs High | $\mathrm{V}_{C C}=\mathrm{Max}$ |  |  | 1.8 | 3.6 | mA |
| $\mathrm{I}_{\text {CCL }}$ | Supply Current with Outputs Low | $V_{C C}=M a x$ |  |  | 3.3 | 6.6 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| tpLH | Propagation Delay Time Low to High Level Output | 4 | 13 | 6 | 18 | ns |
| ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | 3 | 11 | 5 | 18 | ns |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

## DM54LS12/DM74LS12 Triple 3-Input NAND Gates with Open-Collector Outputs

## General Description

This device contains three independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations
$R_{M A X}=\frac{V_{C C}(\mathrm{Min})-V_{\mathrm{OH}}}{N_{1}\left(I_{\mathrm{OH}}\right)+\mathrm{N}_{2}\left(\mathrm{I}_{\mathrm{H}}\right)}$
$R_{\text {MIN }}=\frac{V_{C C}(M a x)-V_{O L}}{l_{O L}-N_{3}\left(I_{L}\right)}$
Where: $\mathrm{N}_{1}(\mathrm{l} \mathrm{OH})=$ total maximum output high current for all outputs tied to pull-up resistor
$\mathrm{N}_{2}\left(l_{\mathrm{IH}}\right)=$ total maximum input high current for all inputs tied to pull-up resistor
$N_{3}\left(l_{I L}\right)=$ total maximum input low current for all inputs tied to pull-up resistor

## Connection Diagram

Dual-In-LIne Package


Order Number DM54LS12J, DM54LS12W, DM74LS12M or DM74LS12N
See NS Package Number J14A, M14A, N14A or W14B

## Function Table

$$
Y=\overline{A B}
$$

| Inputs |  |  | Output |
| :---: | :---: | :---: | :---: |
| A | B | C | Y |
| X | X | L | H |
| X | L | X | H |
| L | X | X | H |
| H | $H$ | $H$ | L |

$H=$ High Logic Level
L = Low Logic Level
$X=$ Either Low or High Logic Level

| Absolute Maximum RatingS (Note) |  |
| :--- | ---: |
| If Milltary/Aerospace specified devices are required, |  |
| please contact the National Semiconductor Sales |  |
| Office/Distributors for availability and specifications. |  |
| Supply Voltage | 7 V |
| Input Voltage | 7 V |
| Output Voltage | 7 V |
| Operating Free Air Temperature Range |  |
| DM54LS | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| DM74LS | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS12 |  |  | DM74LS12 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\text {CC }}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage |  |  | 5.5 |  |  | 5.5 | V |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $I_{\text {cex }}$ | High Level Output Current | $\begin{aligned} & V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{O}}=5.5 \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ |  |  |  | 100 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}_{\mathrm{OL}}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 |  |
|  |  |  | DM74 |  | 0.35 | 0.5 | V |
|  |  | $\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| ${ }_{1 / \mathrm{H}}$ | High Level Input Current | $V_{C C}=\operatorname{Max}, V_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| ILL | Low Level Input Current | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.36 | mA |
| ICCH | Supply Current with Outputs High | $V_{C C}=\operatorname{Max}$ |  |  | 0.7 | 1.4 | mA |
| ICCL | Supply Current with Outputs Low | $V_{C C}=M a x$ |  |  | 1.8 | 3.3 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | $C_{L}=50 \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | 6 | 20 | 20 | 45 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | 3 | 15 | 4 | 20 | ns |

[^5]
## 54LS13/DM74LS13 <br> Dual 4-Input Schmitt Trigger

## General Description

This device contains two independent gates each of which perform the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing jitter free output.

## Connection Diagram



TL/F/10166-1
Order Number 54LS13DMQB, 54LS13FMQB, 54LS13LMQB, DM74LS13M or DM74LS13N See NS Package Number E20A, J14A, M14A, N14A or W14B

| Absolute Maximum Ratings (Note) |  |
| :---: | :---: |
| please contact the National Semiconductor Sales Office/Distributors for avallability and specifications. |  |
| Supply Voltage | 7 V |
| Input Voltage | 7 |
| Operating Free Air Temperature Range |  |
| 54LS | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| DM74LS | - |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to +15 |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | 54LS13 |  |  | DM74LS13 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $V_{\text {CC }}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| IOH | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ <br> (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{I}_{\mathrm{I}}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| V OH | High Level Output Voltage | $\begin{aligned} & V_{C C}=\operatorname{Min}, I_{O H}=M a x, \\ & V_{\mathrm{IL}}=M a x \end{aligned}$ | 54LS | 2.5 |  |  | V |
|  |  |  | DM74 | 2.7 |  |  |  |
| V OL | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\text { Max, } \\ & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | 54LS |  |  | 0.4 |  |
|  |  |  | DM74 |  |  | 0.5 | V |
|  |  | $\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  |  | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{C C}=$ Max, $\mathrm{V}_{1}=10 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| IIH | High Level Input Current | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| $1 / 2$ | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.4 | mA |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=\text { Max } \\ & \text { (Note 2) } \end{aligned}$ | 54LS | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICCH | Supply Current with Outputs High | $\begin{aligned} & V_{C C}=\operatorname{Max} \\ & V_{I N}=\mathrm{GND} \\ & \hline \end{aligned}$ |  |  |  | 6.0 | mA |
| ICCL | Supply Current with Outputs Low | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\ & \mathrm{~V}_{\text {IN }}=\mathrm{OPEN} \end{aligned}$ |  |  |  | 7.0 | mA |
| $\mathrm{V}_{\text {T }+}$ | Positive-Going Threshold Voltage | $\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}$ |  | 1.5 |  | 2.0 | V |
| $\mathrm{V}_{\text {T- }}$ | Negative-Going Threshold Voltage | $\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}$ |  | 0.6 |  | 1.1 | V |
| $\mathrm{V}_{T+}-\mathrm{V}_{\text {T- }}$ | Hysteresis Voltage | $\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}$ |  | 0.4 |  |  | V |
| $\mathrm{I}_{\mathrm{T}+}$ | Input Current at PositiveGoing Threshold | $\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{T}+}$ |  | -0.14* |  |  | mA |
| $I_{T-}$ | Input Current at NegativeGoing Threshold | $V_{C C}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{T}}$ |  | -0.18* |  |  | mA |

[^6]Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

| Switching Characteristics <br> $\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (See Section 1 for test waveforms and output load) |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  |  |  | Units |
|  |  | 54LS |  | DM74 |  |  |
|  |  | Min | Max | Min | Max |  |
| tple | Propagation Delay Time Low to High Level Output |  | 22 |  | 25 | ns |
| ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output |  | 27 |  | 30 | ns |

$\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (See Section 1 for test waveforms and output load)

## 54LS14/DM74LS14 Hex Inverters with Schmitt Trigger Inputs

## General Description

This device contains six independent gates each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

## Connection Diagram

Dual-In-Line Package


Order Number 54LS14DMQB, 54LS14FMQB,
54LS14LMQB, DM74LS14M or DM74LS14N
See NS Package Number E20A, J14A, M14A, N14A or W14B

## Function Table

| $\mathbf{Y}=\overline{\mathbf{A}}$ |  |
| :---: | :---: |
| Input | Output |
| $\mathbf{A}$ | $\mathbf{Y}$ |
| L | H |
| H | L |

$H=$ High Logic Level
L = Low Logic Level

| Absolute Maximum Ratings (Note) |  |
| :---: | :---: |
| please contact the National Semiconductor Sales |  |
|  |  |
| Office/Distributors for availability | specifica |
| Supply Voltage | 7 V |
| Input Voltage | V |
| Operating Free Air Temperature Range |  |
| 54LS | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| DM74LS | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | 54LS14 |  |  | DM74LS14 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $V_{C C}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{T}+}$ | Positive-Going Input <br> Threshold Voltage (Note 1) | 1.5 | 1.6 | 2.0 | 1.4 | 1.6 | 1.9 | V |
| $\mathrm{V}_{\mathrm{T}}$ - | Negative-Going Input Threshold Voltage (Note 1) | 0.6 | 0.8 | 1.1 | 0.5 | 0.8 | 1 | V |
| HYS | Input Hysteresis (Note 1) | 0.4 | 0.8 |  | 0.4 | 0.8 |  | V |
| IOH | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 2) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | 54LS | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\ & \mathrm{V}_{1 \mathrm{H}}=\operatorname{Min} \end{aligned}$ | 54LS |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| IT+ | Input Current at Positive-Going Threshold | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~V}$ | DM74 |  | -0.14 |  | mA |
| ${ }_{1}$ - | Input Current at Negative-Going Threshold | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~V}$ | DM74 |  | -0.18 |  | mA |
| 1 | Input Current @ Max Input Voltage | $V_{C C}=$ Max, | DM74 |  |  | 0.1 | mA |
|  |  | $V_{C C}=M a x$, | 54LS |  |  |  |  |
| $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| ILL | Low Level Input Current | $V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.4 | mA |
| los | Short Circuit Output Current | $V_{C C}=M a x$ <br> (Note 3) | 54LS | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICCH | Supply Current with Outputs High | $\mathrm{V}_{C C}=\mathrm{Max}$ |  |  | 8.6 | 16 | mA |
| ICCL | Supply Current with Outputs Low | $V_{C C}=M a x$ |  |  | 12 | 21 | mA |

Note 1: $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$.
Note 2: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $C_{L}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | 5 | 22 | 8 | 25 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | 5 | 22 | 10 | 33 | ns |

## General Description

This device contains three independent gates, each of which perform the logic AND function. The outputs are open-collector.

## Connection Diagram

## Dual-In-Line Package



Order Number 54LS15DMQB, 54LS15FMQB,
DM74LS15M or DM74LS15N
See NS Package Number J14A, M14A, N14A or W14B

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
Operating Free Air Temperature Range

| 54LS | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| :--- | ---: |
| DM74LS | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions at $\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{v}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$

| Symbol | Parameter | 54LS15 |  |  | DM74LS15 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\text {CC }}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage |  |  | 5.5 |  |  | 5.5 | V |
| 1 OL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & V_{\mathrm{CC}}=\text { Min, } \mathrm{I}_{\mathrm{OL}}=\text { Max } \\ & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | 54LS |  |  | 0.4 | V |
|  |  |  | DM74 |  |  | 0.5 |  |
|  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  |  | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $V_{C C}=M a x, V_{1}=10 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{I}_{\mathrm{H}}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| 112 | Low Level Input Current | $V_{C C}=M a x, V_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.4 | mA |
| lOH | High Level Output Current | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{O}}=5.5 \mathrm{~V}$ |  |  |  | 100 | $\mu \mathrm{A}$ |
| ICCH | Supply Current with Outputs High | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{IN}}=$ OPEN |  |  |  | 3.6 | mA |
| ICCL | Supply Current with Outputs Low | $\mathrm{V}_{\mathrm{IN}}=\mathrm{GND}$ |  |  |  | 6.6 | mA |

Note 1: All typicals are at $V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.

Switching Characteristics
$\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (See Section 1 for test waveforms and output load)

| Symbol | Parameter | $\begin{aligned} & R_{L}=2 \mathrm{k} \Omega \\ & C_{\mathrm{L}}=15 \mathrm{pF} \\ & \hline \end{aligned}$ |  | Units |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Max |  |  |
|  |  | 54LS | DM74 |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | 24 | 20 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | 18 | 14 | ns |

## 54LS20/DM54LS20/DM74LS20 Dual 4-Input NAND Gates

## General Description

This device contains two independent gates each of which performs the logic NAND function.

## Features

- Alternate Military/Aerospace device (54LS20) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications


## Connection Diagram



Function Table

$$
\mathbf{Y}=\overline{\mathbf{A B C D}}
$$

| Inputs |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Output |  |  |  |  |
| A | B | C | D | Y |
| X | X | X | L | H |
| X | X | L | X | H |
| X | L | X | X | H |
| L | X | X | X | H |
| H | H | H | H | L |

$$
H=\text { High Logic Level }
$$

L = Low Logic Level
X = Either Low or High Logic Level


Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & V_{C C}=M i n, I_{O H}=M a x, \\ & V_{\mathrm{IL}}=M a x \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\text {OL }}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\text { Min, } \mathrm{I}_{\mathrm{OL}}=\text { Max, } \\ & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| ${ }_{1 / H}$ | High Level Input Current | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| $1 / 1$ | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.36 | mA |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & (\text { Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICCH | Supply Current with Outputs High | $\mathrm{V}_{C C}=$ Max |  |  | 0.4 | 0.8 | mA |
| ICCL | Supply Current with Outputs Low | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 1.2 | 2.2 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $C_{L}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | 3 | 10 | 4 | 15 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | 3 | 10 | 4 | 15 | ns |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

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## 54LS21/DM54LS21/DM74LS21 Dual 4-Input AND Gates

## General Description

This device contains two independent gates each of which performs the logic AND function.

## Features

- Alternate Military/Aerospace device (54LS21) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.


## Connection Diagram

## Dual-In-Line Package



Order Number 54LS21DMQB, 54LS21FMQB, 54LS21LMQB, DM54LS21J, DM54LS21W, DM74LS21M or DM74LS21N See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$$
\mathbf{Y}=\mathbf{A B C D}
$$

| Inputs |  |  |  | Output |
| :---: | :---: | :---: | :---: | :---: |
| A | B | C | D | Y |
| X | X | X | L | L |
| X | X | L | X | L |
| X | L | X | X | L |
| L | X | X | X | L |
| H | H | H | H | H |

$H=$ High Logic Level
$\mathrm{L}=$ Low Logic Level
X = Either Low or High Logic Level

# Absolute Maximum Ratings (Note) <br> If Military/Aerospace specified devices are required, <br> please contact the National Semiconductor Sales <br> Office/Distributors for availability and specifications. <br> Supply Voltage <br> $7 V$ <br> Input Voltage <br> $7 V$ <br> Operating Free Air Temperature Range <br> DM54LS and 54LS <br> $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ <br> DM74LS <br> Storage Temperature Range 

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS21 |  |  | DM74LS21 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{1 H}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| IOH | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | $-1.5$ | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\ & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & V_{C C}=M i n, I_{O L}=M a x, \\ & V_{\mathrm{IL}}=M a x \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{l} \mathrm{OL}=4 \mathrm{~mA}$, | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| 112 | Low Level Input Current | $\mathrm{V}_{\text {CC }}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}$ |  |  |  | -0.36 | mA |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & \text { (Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICCH | Supply Current with Outputs High | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 1.2 | 2.4 | mA |
| $\mathrm{I}_{\text {CCL }}$ | Supply Current with Outputs Low | $V_{C C}=$ Max |  |  | 2.2 | 4.4 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=\mathbf{2 k} \mathrm{s}$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | 4 | 13 | 6 | 18 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | 3 | 11 | 5 | 18 | ns |

Note 1: All typicals are at $V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

## 54LS22/DM74LS22 <br> Dual 4-Input NAND Gate <br> (with Open-Collector Output)

## General Description

The 'LS22 contains two independent NAND gates, each with four data inputs.

## Connection Diagram



TL/F/10168-1
Order Number 54LS22DMQB, 54LS22FMQB,
DM74LS22M or DM74LS22N
See NS Package Number J14A, M14A, N14A or W14B

| Absolute Maximum Ratings (Note) |  |
| :---: | :---: |
| If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and speclfications. |  |
|  |  |
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Operating Free Air Temperature Range |  |
| 54LS | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| DM74LS | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | 54LS22 |  |  | DM74LS22 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $V_{C C}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $V_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage |  |  | 5.5 |  |  | 5.5 | mA |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ <br> (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| ICEX | High Level Output Current | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{O}}=5.5 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ |  |  |  | 100 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & V_{C C}=\text { Min, } \mathrm{IOL}^{\prime}=\text { Max }, \\ & V_{I H}=\operatorname{Min} \end{aligned}$ | 54LS |  |  | 0.4 |  |
|  |  |  | DM74 |  |  | 0.5 | V |
|  |  | $\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  |  | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{IIH}^{\text {H}}$ | High Level Input Current | $V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| $1 / 12$ | Low Level Input Current | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.4 | mA |
| ICCH | Supply Current Outputs High | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{IN}}=\mathrm{GND}$ |  |  |  | 0.8 | mA |
| ICCL | Supply Current Outputs Low | $V_{C C}=M a x, V_{\text {IN }}=$ Open |  |  |  | 2.2 | mA |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | Units |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output |  | 22 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output |  | 24 | ns |

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## 54LS26/DM74LS26 Quad 2-Input NAND Gates with High Voltage Open-Collector Outputs

## General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.
These gates feature high-voltage output ratings (up to 15 V ) for interfacing with 12 V systems. Although the outputs are rated for 15 V , the device supply is still rated for 5 V .

## Pull-Up Resistor Equations

$$
\begin{gathered}
R_{\text {MAX }}=\frac{V_{\mathrm{O}}(\mathrm{Min})-V_{\mathrm{OH}}}{N_{1}\left(l_{\mathrm{OH}}\right)+\mathrm{N}_{2}\left(I_{\mathrm{IH}}\right)} \\
\mathrm{R}_{\mathrm{MIN}}=\frac{V_{\mathrm{O}}(\mathrm{Max})-V_{\mathrm{OL}}}{I_{\mathrm{OL}}-N_{3}\left(l_{\mathrm{IL}}\right)} \\
\text { Where: } \begin{array}{l}
N_{1}\left(l_{\mathrm{OH}}\right)=\text { total maximum output high current for } \\
\text { all outputs tied to pull-up resistor } \\
N_{2}\left(I_{\mathrm{IH}}\right)=\text { total maximum input high current for all } \\
\text { inputs tied to pull-up resistor } \\
N_{3}\left(I_{I L}\right)=\text { total maximum input low current for all } \\
\text { inputs tied to pull-up resistor }
\end{array}
\end{gathered}
$$

| Absolute Maximum Ratings (Note) |  |
| :---: | :---: |
| If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. |  |
| Supply Voltage | 7 V |
| Input Voitage | 7 V |
| Output Voltage | 15V |
| Operating Free Air Temperature Range |  |
| 54LS | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| DM74LS | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ}$ |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | 54LS26 |  |  | DM74LS26 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $V_{C C}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage |  |  | 15 |  |  | 15 | V |
| loL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $I_{\text {CEX }}$ | High Level Output Current | $\begin{aligned} & V_{C C}=M i n \\ & V_{\mathrm{IL}}=M a x \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}=15 \mathrm{~V}$ |  |  | 1000 | $\mu \mathrm{A}$ |
|  |  |  | $\mathrm{V}_{\mathrm{O}}=12 \mathrm{~V}$ |  |  | 50 |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}_{\mathrm{OL}}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | 54LS |  |  | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=5.5 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{I}_{\mathrm{IH}}$ | High Level Input Current | $V_{C C}=$ Max, $V_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| IIL | Low Level Input Current | $V_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ | 54LS |  |  | $-0.40$ | mA |
|  |  |  | DM74 |  |  | -0.36 |  |
| $\mathrm{I}_{\mathrm{CCH}}$ | Supply Current with Outputs High | $V_{C C}=M a x$ |  |  | 0.8 | 1.6 | mA |
| ICCL | Supply Current with Outputs Low | $V_{C C}=\operatorname{Max}$ |  |  | 2.4 | 4.4 | mA |

Switching Characteristics at $\mathrm{V}_{C C}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $R_{L}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | Units |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Max |  |  |
|  |  | 54LS | DM74 |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | 27 | 32 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | 18 | 28 | ns |

[^7]
## 54LS27/DM54LS27/DM74LS27 Triple 3-Input NOR Gates

## General Description

This device contains three independent gates each of which performs the logic NOR function.

## Features

- Alternate Military/Aerospace device (54LS27) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.


## Connection Diagram

Dual-In-Line Package


TL/F/6359-1
Order Number 54LS27DMQB, 54LS27FMQB, 54LS27LMQB, DM54LS27J, DM54LS27W, DM74LS27M or DM74LS27N See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

| $\mathbf{Y}=\overline{\mathbf{A}+\mathbf{B}}$ |  |  |
| :---: | :---: | :---: |
| Inputs |  | Output |
| A | B | $\mathbf{Y}$ |
| L | L | H |
| L | $H$ | L |
| H | L | L |
| H | H | L |

H = High Logic Level
$L=$ Low Logic Level

Absolute Maximum Ratings（Note）
If Military／Aerospace specified devices are required， please contact the National Semiconductor Sales Office／Distributors for availability and specifications．
Supply Voltage
Input Voltage
Operating Free Air Temperature Range

DM54LS and 54LS
DM74LS
Storage Temperature Range
$-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
$0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

Note：The＂Absolute Maximum Raings＂ beyond which the safety of the device cont： teed．The device should not be operated al ith parametric values defined in the＂Electricali table are not guaranteed at the absolute fin， The＂Recommended Operating Concfilion：＂，＂ the conditions for actual device opermitis．

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS27 |  |  | DM74LS？ |  |  |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5 |
| $\mathrm{~V}_{\mathrm{IH}}$ | High Level Input Voltage | 2 |  |  | 2 |  |  |
| $\mathrm{~V}_{\mathrm{IL}}$ | Low Level Input Voltage |  |  | 0.7 |  |  |  |
| $\mathrm{I}_{\mathrm{OH}}$ | High Level Output Current |  |  | -0.4 |  |  |  |
| $\mathrm{I}_{\mathrm{OL}}$ | Low Level Output Current |  |  | 4 |  |  |  |
| $\mathrm{~T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  |  |

Electrical Characteristics

| Symbol | Parameter | Conditions |  | Min | Typ （Note 1） | ；＇．．． |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{l}}=-18 \mathrm{~mA}$ |  |  |  | $\ldots$ |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | DM54 | 2.5 | 3.4 |  |
|  |  |  | DM74 | 2.7 | 3.4 |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & V_{C C}=\operatorname{Min}, I_{O L}=M a x, \\ & V_{I H}=M i n \end{aligned}$ | DM54 |  | 0.25 | 0.1 |
|  |  |  | DM74 |  | 0.35 | 0.1 |
|  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | $0 \ldots$ |
| 1 | Input Current＠Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}$ |  |  |  | 0.1 |
| $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 9 |
| $1 / 2$ | Low Level Input Current | $\mathrm{V}_{\text {CC }}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}$ |  |  |  | 0.0 |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & (\text { Note 2) } \end{aligned}$ | DM54 | －20 |  | －－1t？ |
|  |  |  | DM74 | －20 |  | －109 |
| ICCH | Supply Current with Outputs High | $\mathrm{V}_{\text {CC }}=\mathrm{Max}$ |  |  | 2 | ¢ |
| ICCL | Supply Current with Outputs Low | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 3.4 | 8.6 |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$（See Section 1 for Test Waveforms and（ -H

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pr}$ |  |
|  |  | Min | Max | Min | M⿴囗十 |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | 3 | 13 | 5 | 18 |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | 3 | 10 | 4 | 15 |

Note 1：All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ．
Note 2：Not more than one output should be shorted at a time，and the duration should not exceed one second．

54LS28/DM74LS28

## Quad 2-Input NOR Buffer

## General Description

The 'LS28 contains four independent gates each of which perform the logic NOR function.

## Connection Diagram



TL/F/10169-1
Order Number 54LS28DMQB, 54LS28FMQB, 54LS28LMQB, DM74LS28M or DM74LS28N
See NS Package Number E20A, J14A, M14A, N14A or W14B
Absolute Maximum Ratings (Note)
If Milltary/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage | 7 V |
| :--- | ---: |
| Input Voltage | 7 V |
| Operating Free Air Temperature Range |  |
| 54 LS | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| DM74LS | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | 54LS28 |  |  | DM74LS28 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| lOH | High Level Output Current |  |  | -1.2 |  |  | -1.2 | mA |
| lOL | Low Level Output Current |  |  | 12 |  |  | 24 | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $V_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\text { Max, } \\ & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | 54LS | 2.5 |  |  | V |
|  |  |  | DM74 | 2.7 |  |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\ & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | 54LS |  |  | 0.4 | V |
|  |  |  | DM74 |  |  | 0.5 |  |
|  |  | $\mathrm{I}_{\mathrm{OL}}=12 \mathrm{~mA}$ | DM74 |  |  | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=10 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{IIH}^{\text {H}}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| 1 LL | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.4 | mA |
| los | Short Circuit Output Current | $V_{C C}=M a x$ <br> (Note 2) | 54LS | $-30$ |  | -130 | mA |
|  |  |  | DM74 | $-30$ |  | -130 |  |
| ICCH | Supply Current with Outputs High | $\mathrm{V}_{C C}=\mathrm{Max}$ |  |  |  | 3.6 | mA |
| ICCL | Supply Current with Outputs Low | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  |  | 13.8 | mA |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

## Switching Characteristics

at $\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (See Section 1 for test waveforms and output load)

| Symbol | Parameter | $\begin{aligned} & R_{L}=2 \mathrm{k} \Omega \\ & C_{L}=15 \mathrm{pF} \\ & \hline \end{aligned}$ |  | Units |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output |  | 20 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output |  | 20 | ns |

## 54LS30/DM54LS30/DM74LS30 <br> 8-Input NAND Gate

## General Description

This device contains a single gate which performs the logic NAND function.

## Features

■ Alternate Military/Aerospace device (54LS30) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

## Connection Diagram



TL/F/6360-1
Order Number 54LS30DMQB, 54LS30FMQB,
54LS30LMQB, DM54LS30J, DM54LS530W, DM74LS30M or DM74LS30N
See NS Package Number E20A, J14A, M14A, N14A or W14B

## Function Table

$$
\mathbf{Y}=\overline{\mathbf{A B C D E F G H}}
$$

| Inputs | Output |
| :---: | :---: |
| $\mathbf{A}$ thru $\mathbf{H}$ | $\mathbf{Y}$ |
| All Inputs $H$ <br> One or More <br> Input $L$ | $\mathbf{L}$ |

$H=$ High Logic Level
$L=$ Low Logic Level


Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS30 |  |  | DM74LS30 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| ${ }^{1} \mathrm{OH}$ | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}_{\mathrm{OL}}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $I_{1 H}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| IIL | Low Level Input Current | $\mathrm{V}_{\text {CC }}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.4 | mA |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & (\text { Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICCH | Supply Current with Outputs High | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 0.35 | 0.5 | mA |
| ICCL | Supply Current with Outputs Low | $V_{C C}=$ Max |  |  | 0.6 | 1.1 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $C_{L}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | 4 | 12 | 5 | 18 | ns |
| ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | 4 | 15 | 5 | 20 | ns |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

## 54LS32/DM54LS32/DM74LS32 <br> Quad 2-Input OR Gates

## General Description

This device contains four independent gates each of which performs the logic OR function.

## Features

- Alternate Military/Aerospace device (54LS32) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.


## Connection Diagram

Dual-In-Line Package


TL/F/6361-1
Order Number 54LS32DMQB, 54LS32FMQB, 54LS32LMQB, DM54LS32J, DM54LS32W, DM74LS32M or DM74LS32N
See NS Package Number E20A, J14A, M14A, N14A or W14B
Function Table

| Inputs |  | Output |
| :---: | :---: | :---: |
| $A$ | $B$ | $Y$ |
| $L$ | $L$ | $L$ |
| L | $H$ | $H$ |
| $H$ | $L$ | $H$ |
| $H$ | $H$ | $H$ |

$H=$ High Logic Level
$L=$ Low Logic Level

| Absolute Maximum Ratings (Note) |
| :--- |
| If Military/Aerospace specified devices are required, |
| please contact the National Semiconductor Sales |
| Office/Distributors for availability and specifications. |
| Supply Voltage |
| Input Voltage |
| Operating Free Air Temperature Range |
| DM54LS and 54 LS |
| DM74LS |
| Storage Temperature Range |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS32 |  |  | DM74LS32 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $V_{C C}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\mathrm{IL}}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| IOH | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | $-55$ |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}$, | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{I}_{\mathrm{H}}$ | High Level Input Current | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{IL}}$ | Low Level Input Current | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.36 | mA |
| los | Short Circuit Output Current | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\ & \text { (Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICCH | Supply Current with Outputs High | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 3.1 | 6.2 | mA |
| $\mathrm{I}_{\text {CCL }}$ | Supply Current with Outputs Low | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 4.9 | 9.8 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $C_{L}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| tPLH | Propagation Delay Time Low to High Level Output | 3 | 11 | 4 | 15 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | 3 | 11 | 4 | 15 | ns |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

## 54LS33/DM74LS33 <br> Quad 2-Input NOR Buffer with Open-Collector Outputs

## General Description

This device contains four independent gates each of which perform the logic NOR function. Outputs are open-collector.

## Connection Diagram



Mviculam Patings (Note)
we specified devices are required, tit National Semiconductor Sales .: ior availability and specifications.
.i. Whperature Range

$$
\begin{array}{r}
-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\
0^{\circ} \mathrm{C} \text { to }+70^{\circ} \mathrm{C}
\end{array}
$$

. ic Fiange

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Operating Conditions

| Parameter | 54LS33 |  |  | DM74LS33 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Min | Nom | Max | Min | Nom | Max |  |
| ! 4 , V Vollage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| Shl evel Input Voltage | 2 |  |  | 2 |  |  | V |
|  |  |  | 0.7 |  |  | 0.8 | V |
| igh Level Output Voltage |  |  | 5.5 |  |  | 5.5 | V |
| 1 6 w level Output Current |  |  | 12 |  |  | 24 | mA |
| $\therefore$ Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Whentoteristics over recommended operating free air temperature range (unless otherwise noted)

| danmer | Conditions |  | Min | $\begin{gathered} \text { Typ } \\ \text { (Note 1) } \end{gathered}$ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| infui Clamp Voltage | $V_{C C}=\operatorname{Min}, l_{I}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| A shi Level Output Bament | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{O}}=5.5 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ |  |  |  | 100 | $\mu \mathrm{A}$ |
| -... ! avcl Output | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\ & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | 54LS |  |  | 0.4 |  |
|  |  | DM74 |  |  | 0.5 | V |
|  | $\mathrm{I}_{\mathrm{OL}}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  |  | 0.4 |  |
| Cument @ Max <br> .! M, Vilage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\therefore$ acllnput Current | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| (:) Level lnput Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}$ |  |  |  | -0.4 | mA |
| : Current with nt: H High | $\begin{aligned} & V_{C C}=M a x \\ & V_{I N}=G N D \end{aligned}$ |  |  |  | 3.6 | mA |
| J. Current with <br> us Low | $\begin{aligned} & V_{C C}=\text { Max } \\ & V_{I N}=\text { Open } \end{aligned}$ |  |  |  | 13.8 | mA |

$V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{A}=25^{\circ} \mathrm{C}$.
Texacteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Parameter | $\mathbf{R}_{\mathrm{L}}=\mathbf{2 k} \mathbf{k}$ <br> $\mathbf{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | Units |
| :---: | :---: | :---: | :---: |
|  | Min | Max |  |
| Propagation Delay Time <br> Low to High Level Output |  | 22 | ns |
| Propagation Delay Time <br> High to Low Level Output | 22 | ns |  |

## 54LS37/DM74LS37 <br> Quad 2-Input NAND Buffers

## General Description

This device contains four independent buffer gates each of which performs the logic NAND function.

## Connection Diagram



TL/F/6362-1
Order Number 54LS37DMQB, 54LS37FMQB, 54LS37LMQB, DM74LS37M or DM74LS37N
See NS Package Number E20A, J14A, M14A, N14A or W14B

## Function Table

| $\mathbf{Y}=\overline{\mathbf{A B}}$ |  |  |
| :---: | :---: | :---: |
| Inputs |  | Output |
| A | $\mathbf{B}$ | $\mathbf{Y}$ |
| L | L | H |
| L | $H$ | H |
| H | L | H |
| H | H | L |

[^8]| Absolute Maximum Ratings (Note) |  |
| :---: | :---: |
| If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avallability and specifications. |  |
| Supply Voltage |  |
| Input Voltage |  |
| Operating Free Air Temperature Range |  |
| 54LS | $-55^{\circ} \mathrm{C}$ to +12 |
| DM74LS | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to +15 |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | 54LS37 |  |  | DM74LS37 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $V_{C C}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\mathrm{IL}}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| IOH | High Level Output Current |  |  | -1.2 |  |  | -1.2 | mA |
| $\mathrm{lOL}^{\text {l }}$ | Low Level Output Current |  |  | 12 |  |  | 24 | mA |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $V_{C C}=\operatorname{Min}, l_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\ & V_{I L}=\operatorname{Max} \end{aligned}$ | 54LS | 2.5 |  |  | V |
|  |  |  | DM74LS | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | 54LS |  |  | 0.4 | V |
|  |  |  | DM74LS |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{IOL}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ |  |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\begin{aligned} V_{C C}=M a x, & V_{1} \end{aligned}=10 \mathrm{~V}(54 \mathrm{LS}), ~(\mathrm{VM} 74 \mathrm{LS})$ |  |  |  | 0.1 | mA |
| 1 IH | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| IIL | Low Level Input Current | $\mathrm{V}_{C C}=\operatorname{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ | 54LS |  |  | -0.40 | mA |
|  |  |  | DM74LS |  |  | -0.36 |  |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & \text { (Note 2) } \end{aligned}$ | 54LS | -30 |  | $-130$ | mA |
|  |  |  | DM74LS | -20 |  | -100 |  |
| ICCH | Supply Current with Outputs High | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 0.9 | 2 | mA |
| ICCL | Supply Current with Outputs Low | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 6 | 12 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | 54LS |  | DM74LS |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}$ |  | $\begin{aligned} & C_{L}=150 \mathrm{pF}, \\ & R_{\mathrm{L}}=667 \Omega \\ & \hline \end{aligned}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output |  | 20 | 4 | 18 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output |  | 20 | 4 | 21 | ns |

Note 1: All typicals are at $V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

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## 54LS38/DM54LS38/DM74LS38 Quad 2-Input NAND Buffers with Open-Collector Outputs

## General Description

This device contains four independent gates, each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

## Features

- Alternate Military/Aerospace device (54LS38) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

Pull-Up Resistor Equations
$R_{\text {MAX }}=\frac{V_{\mathrm{CC}}(\mathrm{Min})-\mathrm{V}_{\mathrm{OH}}}{\mathrm{N}_{1}\left(\mathrm{I}_{\mathrm{OH}}\right)+\mathrm{N}_{2}\left(\mathrm{I}_{\mathrm{I}}\right)}$
$R_{\text {MIN }}=\frac{V_{C C}(\text { Max })-V_{O L}}{I_{O L}-N_{3}\left(I_{\mathrm{IL}}\right)}$
Where: $\mathrm{N}_{1}\left(\mathrm{l}_{\mathrm{OH}}\right)=$ total maximum output high current for all outputs tied to pull-up resistor
$\mathrm{N}_{2}\left(\mathrm{I}_{\mathrm{H}}\right)=$ total maximum input high current for all inputs tied to pull-up resistor
$N_{3}\left(l_{1 L}\right)=$ total maximum input low current for all inputs tied to pull-up resistor

## Connection Diagram



TL/F/6363-1
Order Number 54LS38DMQB, 54LS38FMQB, 54LS38LMQB, DM54LS38J, DM74LS38M or DM74LS38N
See NS Package Number E20A, J14A, M14A, N14A or W14B

## Function Table

$$
\mathbf{Y}=\overline{\mathbf{A B}}
$$

| Inputs |  | Output |
| :---: | :---: | :---: |
| A | B | $\mathbf{Y}$ |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

[^9]
## Absolute Maximum Ratings (Note)

If Military/Aerospace specifled devices are required, please contact the National Semiconductor Sales Office/Distributors for avallablity and specifications.
Supply Voltage
Input Voltage
Output Voltage
Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.
Operating Free Air Temperature Range

DM54LS and 54LS
$-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
DM74LS
Storage Temperature Range

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS38 |  |  | DM74LS38 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage |  |  | 5.5 |  |  | 5.5 | V |
| loL | Low Level Output Current |  |  | 12 |  |  | 24 | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | $\begin{aligned} & \text { Typ } \\ & \text { (Note 1) } \end{aligned}$ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| ${ }^{\text {ICEX }}$ | High Level Output Current | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{O}}=5.5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ |  |  |  | 250 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 |  |
|  |  |  | DM74 |  | 0.35 | 0.5 | V |
|  |  | $\mathrm{IOL}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| ${ }_{1 / \mathrm{H}}$ | High Level Input Current | $V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| IIL | Low Level Input Current | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | $-0.36$ | mA |
| ICCH | Supply Current with Outputs High | $V_{C C}=$ Max |  |  | 0.9 | 2 | mA |
| ICCL | Supply Current with Outputs Low | $\mathrm{V}_{C C}=\mathrm{Max}$ |  |  | 6 | 12 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=667 \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{C}_{\mathrm{L}}=45 \mathrm{pF}$ |  | $C_{L}=150 \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output |  | 22 |  | 48 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output |  | 22 |  | 29 | ns |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.

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## 54LS40/DM74LS40 <br> Dual 4-Input NAND Buffer

## General Description

This device contains two independent gates each of which perform the logic NAND function.

## Connection Diagrams



If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage

Operating Free Air Temperature Range

54LS
DM74LS
Storage Temperature Range

$$
\begin{array}{r}
-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\
0^{\circ} \mathrm{C} \text { to }+70^{\circ} \mathrm{C} \\
-65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C}
\end{array}
$$

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | 54LS40 |  |  | DM74LS40 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $V_{C C}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| IOH | High Level Output Current |  |  | -1.2 |  |  | -1.2 | mA |
| lOL | Low Level Output Current |  |  | 12 |  |  | 24 | mA |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $V_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\text { Max, } \\ & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | 54LS | 2.5 |  |  | V |
|  |  |  | DM74 | 2.7 |  |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\ & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | 54LS |  |  | 0.4 | V |
|  |  |  | DM74 |  |  | 0.5 |  |
|  |  | $\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  |  | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=10 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| ILL | Low Level Input Current | $V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -1.6 | mA |
| los | Short Circuit Output Current | $V_{C C}=M a x$ <br> (Note 2) | 54LS | $-30$ |  | -130 | mA |
|  |  |  | DM74 | $-30$ |  | -130 |  |
| ICCH | Supply Current with Outputs High | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{IN}}=\mathrm{GND}$ |  |  |  | 1.0 | mA |
| ICCL | Supply Current with Outputs Low | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\text {IN }}=$ OPEN |  |  |  | 6.0 | mA |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Note more than one output should be shorted at a time, and the duration should not exceed one second.

## Switching Characteristics

$V_{C C}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (See Section 1 for test wate:.

| Symbol | Parameter |
| :---: | :---: |
| tPLH | Propagation Delay Time <br> Low to High Level Outpue |
| tPHL | Propagation Delay Time <br> High to Low Level Outpui |

## 54LS42/DM54LS42/DM74LS42 BCD/Decimal Decoders

## General Description

These BCD-to-decimal decoders consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of input logic ensures that all outputs remain off for all invalid $(10-15)$ input conditions.

## Features

- Diode clamped inputs

■ Also for applications as 4-line-to-16-line decoders; 3-line-to-8-line decoders

- All outputs are high for invalid input conditions
- Alternate Military/Aerospace device (54LS42) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

Connection Diagram


TL/F/6365-1
Order Number 54LS42DMQB, 54LS42FMQB, DM54LS42J, DM54LS42W, DM74LS42M or DM74LS42N
See NS Package Number J16A, M16A, N16E or W16A

Function Table

| No. | BCD Inputs |  |  |  | Decimal Outputs |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0 | L | L | L | L | L | H | H | H | H | H | H | H | H | H |
| 1 | L | L | L | H | H | L | H | H | H | H | H | H | H | H |
| 2 | L | L | H | L | H | H | L | H | H | H | H | H | H | H |
| 3 | L | L | H | H | H | H | H | L | H | H | H | H | H | H |
| 4 | L | H | L | L | H | H | H | H | L | H | H | H | H | H |
| 5 | L | H | L | H | H | H | H | H | H | L | H | H | H | H |
| 6 | L | H | H | L | H | H | H | H | H | H | L | H | H | H |
| 7 | L | H | H | H | H | H | H | H | H | H | H | L | H | H |
| 8 | H | L | L | L | H | H | H | H | H | H | H | H | L | H |
| 9 | H | L | L | H | H | H | H | H | H | H | H | H | H | L |
| 1 | H | L | H | L | H | H | H | H | H | H | H | H | H | H |
| N | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| A | H | H | L | L | H | H | H | H | H | H | H | H | H | H |
| A | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| L | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| D | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

$H=$ High Level
L = Low Level

## Logic Diagram



Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
7 V
Operating Free Air Temperature Range

DM54LS and 54LS
DM74LS
$-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
$0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$
Storage Temperature Range

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS42 |  |  | DM74LS42 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| ${ }_{\mathrm{OH}}$ | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\text {OL }}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{IOL}=4 \mathrm{~mA}$, | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| IIL | Low Level Input Current | $V_{C C}=M a x, V_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.4 | mA |
| los | Short Circuit Output Current | $V_{C C}=M a x$ <br> (Note 2) | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICC | Supply Current | $V_{C C}=\operatorname{Max}$ (Note 3) |  |  | 7 | 13 | mA |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: ICC is measured with all outputs open and all inputs grounded.

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From (Input) To (Output) | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  |  | Min | Max | Min | Max |  |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | A, B, C, or D (2 Levels of Logic) to Output |  | 25 |  | 30 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | A, B, C, or D (3 Levels of Logic) to Output |  | 30 |  | 35 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | A, B, C, or D (2 Levels of Logic) to Output |  | 25 |  | 30 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | A, B, C, or D (3 Levels of Logic) to Output |  | 30 |  | 35 | ns |

## 54LS47/DM74LS47 <br> BCD to 7-Segment Decoder/Driver

## General Description

The 'LS47 accepts four lines of BCD (8421) input data, generates their complements internally and decodes the data with seven AND/OR gates having open-collector outputs to drive indicator segments directly. Each segment output is guaranteed to sink 24 mA in the ON (LOW) state and withstand 15 V in the OFF (HIGH) state with a maximum leakage current of $250 \mu \mathrm{~A}$. Auxiliary inputs provided blanking, lamp test and cascadable zero-suppression functions. Also see the 'LS47 data sheet.

## Features

- Open-collector outputs
- Drive indicator segments directly
- Cascadable zero-suppression capability
- Lamp test input


## Connection Diagram



TL/F/9817-1
Order Number 54LS47DMQB, 54LS47FMQB, DM74LS47M or DM74LS47N
See NS Package Number J16A, M16A, N16E or W16A

| Pin Names | Description |
| :--- | :--- |
| A0-A3 | BCD Inputs |
| $\overline{\text { RBI }}$ | Ripple Blanking Input (Active LOW) |
| $\overline{\text { LT }}$ | Lamp Test Input (Active LOW) |
| $\overline{\mathrm{BI} / R B O}$ | Blanking Input (Active LOW) or |
| $\overline{\mathrm{a}}-\overline{\mathrm{g}}$ | Ripple Blanking Output (Active LOW) |
|  | *Segment Outputs (Active LOW) |

[^10]Absolute Maximum Ratings (Note)
If Military/Aerospace specifled devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage | 7 V |
| :--- | ---: |
| Input Voltage | 7 V |
| Operating Free Air Temperature Range |  |
| 54 LS | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| DM74LS | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | 54LS47 |  |  | DM74SL47 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| IOH | High Level Output Current @ $15 \mathrm{~V}=\mathrm{V}_{\mathrm{OH}}{ }^{*}$ |  |  | -50 |  |  | -250 | $\mu \mathrm{A}$ |
| lOL | Low Level Output Current |  |  | 12 |  |  | 24 | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

*OFF state at $\overline{\mathrm{a}}-\overline{\mathrm{g}}$.

## Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | 54LS | 2.4 |  |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max}, \\ & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | 54LS |  |  | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $V_{C C}=M a x, V_{1}=10 \mathrm{~V}$ |  |  |  | 100 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{H}}$ | High Level Input Current | $V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| IIL | Low Level Input Current | $V_{C C}=M a x, V_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.4 | mA |
| los | Short Circuit Output Current | $V_{C C}=\operatorname{Max}$ <br> (Note 2), los at $\overline{\mathrm{BI} / \mathrm{RBO}}$ | 54LS | -0.3 |  | -2.0 | mA |
|  |  |  | DM74 | -0.3 |  | -2.0 |  |
| ICC | Supply Current | $\mathrm{V}_{C C}=$ Max |  |  |  | 13 | mA |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$

| Symbol | Parameter | Conditions | $\begin{aligned} & R_{L}=665 \Omega \\ & C_{L}=15 \mathrm{pF} \end{aligned}$ |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |
|  |  |  | Min | Max |  |
| tpLH $\mathrm{t}_{\mathrm{PHL}}$ | Propagation Delay <br> An to $\bar{a}-\bar{g}$ |  |  | $\begin{aligned} & 100 \\ & 100 \\ & \hline \end{aligned}$ | ns |
| $t_{\text {PLH }}$ <br> $\mathrm{t}_{\mathrm{PHL}}$ | Propagation Delay $\overline{\text { RBI }}$ to $\overline{\mathrm{a}}-\overline{\mathrm{g}}^{*}$ |  |  | $\begin{aligned} & 100 \\ & 100 \\ & \hline \end{aligned}$ | ns |

${ }^{*} \overline{L T}=H I G H, A O-A 3=L O W$

## Functional Description

The 'LS47 decodes the input data in the pattern indicated in the Truth Table and the segment identification illustration. If the input data is decimal zero, a LOW signal applied to the $\overline{\text { RBI blanks the display and causes a multidigit display. For }}$ example, by grounding the $\overline{\mathrm{RBI}}$ of the highest order decoder and connecting its $\overline{\mathrm{BI} / R B O}$ to RBI of the next lowest order decoder, etc., leading zeros will be suppressed. Similarly, by grounding $\overline{\text { RBI }}$ of the lowest order decoder and connecting its BI/RBO to RBI of the next highest order decoder, etc., trailing zeros will be suppressed. Leading and trailing zeros can be suppressed simultaneously by using external gates, i.e.: by driving $\overline{\mathrm{RBI}}$ of a intermediate decoder from an OR
gate whose inputs are $\overline{\mathrm{BI} / \text { RBO }}$ of the next highest and lowest order decoders. $\overline{\mathrm{BI} / \mathrm{RBO}}$ also serves as an unconditional blanking input. The internal NAND gate that generates the $\overline{R B O}$ signal has a resistive pull-up, as opposed to a totem pole, and thus BI/RBO can be forced LOW by external means, using wired-collector logic. A LOW signal thus applied to BI/RBO turns off all segment outputs. This blanking feature can be used to control display intensity by varying the duty cycle of the blanking signal. A LOW signal applied to LT turns on all segment outputs, provided that $\overline{\mathrm{BI} / \mathrm{RBO}}$ is not forced LOW.

## Logic Diagram



TL/F/9817-3
Numerical Designations-Resultant Displays

$$
0 \text { D23456789cITEE }
$$

$$
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Pin} 16 \\
& \mathrm{GND}=\operatorname{Pin} 8
\end{aligned}
$$

Truth Table

| Decimal or Function | Inputs |  |  |  |  |  |  | Outputs |  |  |  |  |  |  | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\overline{\text { LT }}$ | RBI | A3 | A2 | A1 | AO | BI/RBO | $\overline{\mathrm{a}}$ | $\overline{\text { b }}$ | $\overline{\mathbf{c}}$ | $\bar{d}$ | $\overline{\mathbf{e}}$ | $\bar{f}$ | $\overline{\mathbf{g}}$ |  |
| 0 | H | H | L | L | L | L | H | L | L | L | L | L | L | H | 1 |
| 1 | H | X | L | L | L | H | H | H | L | L | H | H | H | H | 1 |
| 2 | H | X | L | L | H | L | H | L | L | H | L | L | H | L |  |
| 3 | H | X | L | L | H | H | H | L | L | L | L | H | H | L |  |
| 4 | H | $x$ | L | H | L | L | H | H | L | L | H | H | L | L |  |
| 5 | H | X | L | H | L | H | H | L | H | L | L | H | L | L |  |
| 6 | H | X | L | H | H | L | H | H | H | L | L | L | L | L |  |
| 7 | H | X | L | H | H | H | H | L | L | L | H | H | H | H |  |
| 8 | H | X | H | L | L | L | H | L | L | L | L | L | L | L |  |
| 9 | H | X | H | L | L | H | H | L | L | L | H | H | L | L |  |
| 10 | H | X | H | L | H | L | H | H | H | H | L | L | H | L |  |
| 11 | H | X | H | L | H | H | H | H | H | L | L | H | H | L |  |
| 12 | H | X | H | H | L | L | H | H | L | H | H | H | L | L |  |
| 13 | H | X | H | H | L | H | H | L | H | H | L | H | L | L |  |
| 14 | H | $x$ | H | H | H | L | H | H | H | H | L | L | L | L |  |
| 15 | H | X | H | H | H | H | H | H | H | H | H | H | H | H |  |
| BI | X | X | X | X | X | X | L | H | H | H | H | H | H | H | 2 |
| $\overline{\text { RBI }}$ | H | L | L | L | L | L | L | H | H | H | H | H | H | H | 3 |
| $\overline{\text { LT }}$ | L | X | X | X | X | X | H | L | L | L | L | L | L | L | 4 |

Note 1: $\overline{\mathrm{BI} / \mathrm{RBO}}$ is wire-AND logic serving as blanking input ( $\overline{\mathrm{BI}}$ ) and/or ripple-blanking output ( $\overline{\mathrm{RBO}}$ ). The blanking out ( $\overline{\mathrm{BI}}$ ) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ( $\overline{\mathrm{RBI})}$ ) must be open or at a HIGH level if blanking or a decimal 0 is not desired. $\mathrm{X}=$ input may be HIGH or LOW.
Note 2: When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a HIGH level regardless of the state of any other input condition.
Note 3: When ripple-blanking input ( $\overline{\mathrm{RBI}})$ and inputs A0, A1, A2 and A3 are LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ( $\overline{\mathrm{RBO}}$ ) goes to a LOW level (response condition).
Note 4: When the blanking input/ripple-blanking output ( $\overline{\mathrm{BI} / \mathrm{RBO}})$ is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.
driver transistors. Auxiliary inputs provide lamp test, blanking and cascadable zero-suppression functions.
the 'LS48 decodes the input data in the pattern indicated in ins Truth Table and the segment identification illustration.


TL/F/10172-1
SM@B, DM74LS48M, or DM74LS48N
) $\mathfrak{A}$, M16A, N16E or W16A

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
$7 V$
Operating Free Air Temperature Range
54LS
$-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
DM74LS
Storage Temperature Range

## Recommended Operating Conditions

| Symbol | Parameter | 54LS48 |  |  | DM74LS48 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\mathrm{IL}}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| IOH | High Level Output Current |  |  | -50 |  |  | -50 | $\mu \mathrm{A}$ |
| lOL | Low Level Output Current |  |  | 2.0 |  |  | 6.0 | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ <br> (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & V_{\mathrm{CC}} \operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | 54LS | 2.4 |  |  | V |
|  |  |  | DM74 | 2.4 |  |  |  |
| IOFF | Output High Current Segment Outputs | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{V}_{\mathrm{O}}=0.85 \mathrm{~V}$ |  | -1.3 |  |  | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\ & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | 54LS |  |  | 0.4 | V |
|  |  |  | DM74 |  |  | 0.5 |  |
|  |  | $\mathrm{IOL}=2.0 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  |  | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $V_{C C}=M a x, V_{l}=10 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{I}_{\mathrm{H}}$ | High Level Input Current | $V_{C C}=$ Max, $V_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| 1 lL | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.4 | mA |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x, V_{O}=0 V \\ & \text { at } \overline{\mathrm{B} / / R B O}(\text { Note 2 }) \end{aligned}$ | 54LS | -0.3 |  | -2 | mA |
|  |  |  | DM74 | -0.3 |  | -2 |  |
| ICCH | Supply Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{IN}}=4.5 \mathrm{~V}$ |  |  |  | 38 | mA |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $C_{L}=15 \mathrm{pF}$ |  | Units |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max |  |
| $\begin{aligned} & \mathrm{t}_{\mathrm{PLH}} \\ & \mathrm{t}_{\mathrm{PHL}} \\ & \hline \end{aligned}$ | Propagation Delay Time $A_{n}$ to a-g |  | $\begin{aligned} & 100 \\ & 100 \\ & \hline \end{aligned}$ | ns |
| $\mathrm{t}_{\mathrm{PLH}}$ $\mathrm{t}_{\mathrm{PHL}}$ | Propagation Delay Time $\overline{\text { RBI }}$ to $a-f$ |  | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ | ns |
| Note: [T $=$ HIGH, $A_{0}-\mathrm{A}_{3}=$ HIGH. |  |  |  |  |

## Truth Table

| Decimal Or <br> Function | Inputs |  |  |  |  |  | Outputs |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\overline{\mathbf{L T}}$ | $\overline{\text { RBI }}$ | $\mathrm{A}_{3}$ | $\mathrm{A}_{2}$ | $\mathrm{A}_{1}$ | $A_{0}$ | BI/RBO | a | b | c | d | e | $f$ | $g$ |
| 0 (Note 1) | H | H | L | L | L | L | H | H | H | H | H | H | H | L |
| 1 (Note 1) | H | X | L | L | L | H | H | L | H | H | L | L | L | L |
| 2 | H | X | L | L | H | L | H | H | H | L | H | H | L | H |
| 3 | H | X | L | L | H | H | H | H | H | H | H | L | L | H |
| 4 | H | $x$ | L | H | L | L | H | L | H | H | L | L | H | H |
| 5 | H | X | L | H | L | H | H | H | L | H | H | L | H | H |
| 6 | H | X | L | H | H | L | H | L | L | H | H | H | H | H |
| 7 | H | $x$ | L | H | H | H | H | H | H | H | L | L | L | L |
| 8 | H | X | H | L | L | L | H | H | H | H | H | H | H | H |
| 9 | H | X | H | L | L | H | H | H | H | H | L | L | H | H |
| 10 | H | X | H | L | H | L | H | L | L | L | H | H | L | H |
| 11 | H | X | H | L | H | H | H | L | L | H | H | L | L | H |
| 12 | H | X | H | H | L | L | H | L | H | L | L | L | H | H |
| 13 | H | X | H | H | L | H | H | H | L | L | H | L | H | H |
| 14 | H | $x$ | H | H | H | L | H | L | L | L | H | H | H | H |
| 15 | H | X | H | H | H | H | H | L | L | L | L | L | L | L |
| $\overline{\text { BI ( }}$ (Note 2) | X | X | X | X | X | X | L | L | L | L | L | L | L | L |
| RBI (Note 3) | H | L | L | L | L | L | L | L | L | L | L | L | L | L |
| LT (Note 4) | L | $X$ | X | X | X | X | H | H | H | H | H | H | H | H |

Note 1: $\overline{\mathrm{BI} / \mathrm{RBO}}$ is wired-AND logic serving as blanking input ( $\overline{\mathrm{BI}})$ and/or ripple-blanking output ( $\overline{\mathrm{RBO}}$ ). The blanking out ( $\overline{\mathrm{BI}}$ ) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ( $\overline{\mathrm{RBI}})$ must be open or at a HIGH level if blanking of a decimal 0 is not desired. $X=$ input may be HIGH or LOW.
Note 2: When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level, regardless of the state of any other input condition.
Note 3: When ripple-blanking input ( $\overline{\mathrm{RBI}}$ ) and inputs $A_{0}, A_{1}, A_{2}$, and $A_{3}$ are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a LOW level and the ripple-blanking output ( $\overline{\mathrm{RBO}}$ ) goes to a LOW level (response condition).
Note 4: When the blanking input/ripple-blanking output ( $\overline{\mathrm{BI} / \mathrm{RBO}})$ is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a HIGH level.

## Logic Symbol




## 54LS49 BCD to 7-Segment Decoder

## General Description

The 54LS49 translates four lines of BCD (8421) input data into the 7 -segment numeral code as shown in the Function Table. It has open-collector outputs and is logically the 14pin verson of the '48, without the lamp test and ripple blanking features. Also see the 'LS249 data sheet.

## Connection Diagram



TL/F/10204-1
Order Number 54LS49DMQB or 54LS49FMQB See NS Package Number J14A or W14B

## Logic Symbol



TL/F/10204-2

$$
V_{C C}=\operatorname{Pin} 14
$$

$$
\text { GND }=\operatorname{Pin} 7
$$

| Pin Names | Description |
| :--- | :--- |
| $\mathrm{AO}-\mathrm{A} 3$ | BCD Inputs |
| $\overline{\mathrm{BI}}$ | Blanking Input (Active LOW) |
| $\mathrm{a}-\mathrm{g}$ | Segment Outputs (Active HIGH) |

Numerical Designations-Resultant Displays


Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter |  | 54LS49 |  | Units |
| :--- | :--- | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | V |
| $\mathrm{~V}_{\mathrm{IH}}$ | High Level Input Voltage | 2 |  |  | V |
| $\mathrm{~V}_{\mathrm{IL}}$ | Low Level Input Voltage |  |  | 0.7 | V |
| $\mathrm{I}_{\mathrm{OH}}$ | High Level Output Current |  |  | 250 | $\mu \mathrm{~A}$ |
| $\mathrm{I}_{\mathrm{OL}}$ | Low Level Output Current |  |  | 4 | mA |
| $\mathrm{~T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ <br> (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{\mathrm{l}}=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\ & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | 2.5 |  |  | V |
| VOL | Low Level Output Voltage | $\begin{aligned} & V_{C C}=\text { Min, } I_{O L}=\text { Max }, \\ & V_{\mathrm{IH}}=\text { Min, } V_{\mathrm{IL}}=\operatorname{Max} \end{aligned}$ |  |  | 0.4 | V |
| 1 | Input Current @ Max Input Voltage | $V_{C C}=$ Max, $V_{1}=10.0 \mathrm{~V}$ |  |  | 0.1 | mA |
| ${ }_{1 / H}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  | 20 | $\mu \mathrm{A}$ |
| $1 / 2$ | Low Level Input Current | $V_{C C}=M a x, V_{1}=0.4 \mathrm{~V}$ |  |  | -0.4 | mA |
| ICC | Supply Current | $V_{C C}=M a x$ |  |  | 15 | mA |

Note 1: All typicals are at $V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Switching Characteristics $\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (See Section 1 for waveforms and output load)

| Symbol | Parameter | 54LS |  | Units |
| :---: | :---: | :---: | :---: | :---: |
|  |  | $C_{L}=15 \mathrm{pF}$ |  |  |
|  |  | Min | Max |  |
| $t_{\text {PLH }}$ $\mathrm{t}_{\mathrm{PHL}}$ | $\begin{aligned} & \text { Propagation Delay; } R_{L}=2 \mathrm{k} \Omega \\ & A_{n} \text { to } a-g \end{aligned}$ |  | $\begin{aligned} & 100 \\ & 100 \\ & \hline \end{aligned}$ | ns |
| tplH <br> tpHL | Propagation Delay; $R_{L}=6 \mathrm{k} \Omega$ $\overline{B I}$ to $\mathrm{a}-\mathrm{g}$ |  | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ | ns |

Function Table

| Decimal or Function | Inputs |  |  |  |  | Outputs |  |  |  |  |  |  | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | A3 | A2 | A1 | A0 | BI | a | b | c | d | e | $f$ | g |  |
| 0 | L | L | L | L | H | H | H | H | H | H | H | L | 1 |
| 1 | L | L | L | H | H | L | H | H | L | L | L | L |  |
| 2 | L | L | H | L | H | H | H | L | H | H | L | H |  |
| 3 | L | L | H | H | H | H | H | H | H | L | L | H |  |
| 4 | L | H | L | L | H | L | H | H | L | L | H | H |  |
| 5 | L | H | L | H | H | H | L | H | H | L | H | H |  |
| 6 | L | H | H | L | H | L | L | H | H | H | H | H |  |
| 7 | L | H | H | H | H | H | H | H | L | L | L | L |  |
| 8 | H | L | L | L | H | H | H | H | H | H | H | H |  |
| 9 | H | L | L | H | H | H | H | H | L | L | H | H |  |
| 10 | H | L | H | L | H | L | L | L | H | H | L | H |  |
| 11 | H | L | H | H | H | L | L | H | H | L | L | H |  |
| 12 | H | H | L | L | H | L | H | L | L | L | H | H |  |
| 13 | H | H | L | H | H | H | L | L | H | L | H | H |  |
| 14 | H | H | H | L | H | L | L | L | H | H | H | H |  |
| 15 | H | H | H | H | H | L | L | L | L | L | L | L |  |
| BI | X | X | X | X | L | L | L | L | L | L | L | L | 2 |

Note 1: The blanking input must be open or held at a HIGH level when output functions 0 through 15 are desired.
Note 2: When a LOW level is applied to the blanking input all segment outputs go to a LOW level regardless of the state of any other input condition. $\mathrm{X}=$ Input may be HIGH or LOW.
$H=$ HIGH Voltage Level
$L=$ LOW Voltage Level
$X=$ Immaterial

## Logic Diagram



TL/F/10204-4

National
Semiconductor

## 54LS51/DM74LS51 Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-INVERT Gates

## General Description

This device contains two independent combinations of gates each of which performs the logic AND-OR-INVERT function. Each package contains one 2-wide 2-input and one 2 -wide 3 -input AND-OR-INVERT gates.

## Connection Diagram



## Function Table

$$
Y 1=\overline{(A 1)(B 1)(C 1)+(D 1)(E 1)(F 1)}
$$

| Inputs |  |  |  |  |  | Output |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A1 | B1 | C1 | D1 | E1 | F1 | Y1 |
| H | H | H | X | X | X | L |
| X | X | X | H | H | H | L |
| Other Combinations |  |  |  |  |  |  |

Y2 $=\overline{((A 2)(B 2)+(C 2)(D 2))}$

| Inputs |  |  |  | Output |
| :---: | :---: | :---: | :---: | :---: |
| A2 | B2 | C2 | D2 | Y2 |
| H | H | X | X | L |
| X | X | H | H | L |
| Other combinations |  |  |  |  |

$H=$ High Logic Level
$L=$ Low Logic Level
$X=$ Either Low or High Logic Level

```
Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for availability and specifications.
Supply Voltage
7V
Input Voltage
7V
Operating Free Air Temperature Range
\begin{tabular}{lr}
54 LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}
```

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | 54LS51 |  |  | DM74LS51 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| ${ }_{\mathrm{OH}}$ | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| IOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\text { Max, } \\ & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | 54LS | 2.5 |  |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\text {OL }}$ | Low Level Output Voltage | $\begin{aligned} & V_{\mathrm{CC}}=\operatorname{Min}, I_{O L}=\operatorname{Max}, \\ & \mathrm{V}_{\mathbb{I H}}=\operatorname{Min} \end{aligned}$ | 54LS |  |  | 0.4 |  |
|  |  |  | DM74 |  | 0.35 | 0.5 | V |
|  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ |  |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $V_{C C}=M a x, V_{1}=10 \mathrm{~V}$ (54LS) |  |  |  | 0.1 | mA |
| $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| IIL | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ | 54LS |  |  | -0.40 | mA |
|  |  |  | DM74 |  |  | -0.36 |  |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & \text { (Note 2) } \end{aligned}$ | 54LS | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICCH | Supply Current with Outputs High | $V_{C C}=\operatorname{Max}$ |  |  | 0.8 | 1.6 | mA |
| ICCL | Supply Current with Outputs Low | $\mathrm{V}_{C C}=\operatorname{Max}$ |  |  | 1.4 | 2.8 | mA |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | 54LS51 |  | DM74LS51 |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\begin{aligned} & C_{L}=15 \mathrm{pF}, \\ & R_{\mathrm{L}}=2 \mathrm{k} \Omega \\ & \hline \end{aligned}$ |  | $\begin{aligned} & C_{L}=50 \mathrm{pF}, \\ & R_{\mathrm{L}}=2 \mathrm{k} \Omega \end{aligned}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| tplH | Propagation Delay Time Low to High Level Output |  | 20 | 4 | 18 | ns |
| ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output |  | 20 | 3 | 15 | ns |

## General Description

This device contains a combination of four, two input AND
gates whose outputs are connected to a four input NOR
Gate.

## Connection Diagram



TL/F/10173-1
Order Number 54LS54DMQB, 54LS54FMQB, DM74LS54M or DM74LS54N
See NS Package Number J14A, M14A, N14A or W14B
Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
Operating Free Air Temperature Range
54LS
DM74LS
Storage Temperature Range
Sto

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | 54LS54 |  |  | DM74LS54 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\text {CC }}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| $\mathrm{lOH}^{\text {l }}$ | High Level Output Voltage |  |  | -0.4 |  |  | -0.4 | mA |
| 1 OL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Tyр <br> (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\text { Max, } \\ & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | 54LS | 2.5 |  |  | V |
|  |  |  | DM74LS | 2.7 |  |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\text { Max, } \\ & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | 54LS |  |  | 0.4 | V |
|  |  |  | DM74LS |  |  | 0.5 |  |
|  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}$, | DM74LS |  |  | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $V_{C C}=M a x, V_{1}=10 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| 1 IH | High Level Input Current | $\mathrm{V}_{C C}=$ Max, $\mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| ILL | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.4 | mA |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=\text { Max } \\ & \text { (Note 2) } \end{aligned}$ | 54LS | -20 |  | -100 | mA |
|  |  |  | DM74LS | -20 |  | -100 |  |
| ICCH | Supply Current with Outputs High | $\begin{aligned} & V_{C C}=M a x \\ & V_{I N}=G N D \end{aligned}$ |  |  |  | 1.6 | mA |
| ICCL | Supply Current with Outputs Low | $\begin{aligned} & V_{C C}=M a x \\ & V_{\mathbb{I N}}=O p e n \\ & \hline \end{aligned}$ |  |  |  | 2.0 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $C_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  | Units |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output |  | 15 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output |  | 15 | ns |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

## General Description

This device contains a combination of AND-OR-INVERT functions. The internal gates are configured as two, four-input AND gates with their outputs connected to a two-input NOR gate.

## Connection Diagram

Dual-In-Line Package


TL/F/10174-1
Order Number 54LS55DMQB, 54LS55FMQB,
DM74LS55M or DM74LS55N
See NS Package Number J14A, M14A, N14A or W14B

| bsolute Maximum Ratings (Note) |  |
| :---: | :---: |
| please contact the National Semiconductor Sales Office/Distributors for availability and specifications. |  |
| Supply Voltage | 7 |
| Input Voltage |  |
| Operating Free Air Temperature Range |  |
| 54LS | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| DM74LS | $0^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | 54LS55 |  |  | DM74LS55 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $V_{C C}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| $\mathrm{lOH}^{\text {l }}$ | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unloss otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{1}$ | Input Clamp Voltage | $V_{C C}=\operatorname{Min}, I_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | 54LS | 2.5 |  |  | V |
|  |  |  | DM74 | 2.7 |  |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\text { Max }, \\ & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | 54LS |  |  | 0.4 | V |
|  |  |  | DM74 |  |  | 0.5 |  |
|  |  | $\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  |  | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $V_{C C}=M a x, V_{l}=10 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{I}_{\mathrm{IH}}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {IL }}$ | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.4 | mA |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & (\text { Note 2) } \end{aligned}$ | 54LS | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICCH | Supply Current with Outputs High | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{IN}}=\mathrm{GND}$ |  |  |  | 0.8 | mA |
| ICCL | Supply Current with Outputs Low | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\text {IN }}=$ Open |  |  |  | 1.3 | mA |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

## Switching Characteristics

$\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  | Units |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max |  |
| $t_{\text {PLH }}$ <br> $t_{\text {PHL }}$ | Propagation Delay Time |  | $\begin{aligned} & 15 \\ & 15 \\ & \hline \end{aligned}$ | ns |

# DM54LS73A/DM74LS73A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Clear and Complementary Outputs 

## General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The $J$ and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. The data on the J
and K inputs is allowed to change while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the clear input will reset the outputs regardless of the levels of the other inputs.

## Connection Diagram

Dual-In-Line Package


TL/F/6372-1
Order Number DM54LS73AJ, DM54LS73AW, DM74LS73AM or DM74LS73AN
See NS Package Number J14A, M14A, N14A or W14B

## Function Table

| Inputs |  |  |  | Outputs |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CLR | CLK | J | K | Q | $\overline{\mathbf{Q}}$ |
| L | X | X | X | L | H |
| H | $\downarrow$ | L | L | $Q_{0}$ | $\bar{Q}_{0}$ |
| $H$ | $\downarrow$ | $H$ | $L$ | $H$ | L |
| H | $\downarrow$ | L | $H$ | L | $H$ |
| $H$ | $\downarrow$ | $H$ | $H$ | Toggle |  |
| $H$ | $H$ | X | X | $Q_{0}$ | $\bar{Q}_{0}$ |

$H=$ High Logic Level
L = Low Logic Level
$X=$ Either Low or High Logic Level
$\downarrow=$ Negative going edge of pulse.
$Q_{0}=$ The output logic level before the indicated input conditions were established.
Toggle $=$ Each output changes to the complement of its previous level on each falling edge of the clock pulse.

[^11]Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The 'Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter |  | DM54LS73A |  |  | DM74LS73A |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage |  | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  |  | 0.7 |  |  | 0.8 | V |
| IOH | High Level Output Current |  |  |  | -0.4 |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  |  | 4 |  |  | 8 | mA |
| $\mathrm{f}_{\mathrm{CLK}}$ | Clock Frequency (Note 2) |  | 0 |  | 30 | 0 |  | 30 | MHz |
| $\mathrm{f}_{\mathrm{CLK}}$ | Clock Frequency (Note 3) |  | 0 |  | 25 | 0 |  | 25 | MHz |
| tw | Pulse Width (Note 2) | Clock High | 20 |  |  | 20 |  |  | ns |
|  |  | Preset Low | 25 |  |  | 25 |  |  |  |
|  |  | Clear Low | 25 |  |  | 25 |  |  |  |
| ${ }^{\text {t }}$ W | Pulse Width (Note 3) | Clock High | 25 |  |  | 25 |  |  | ns |
|  |  | Preset Low | 30 |  |  | 30 |  |  |  |
|  |  | Clear Low | 30 |  |  | 30 |  |  |  |
| tsu | Setup Time (Notes 1 and 2) |  | $20 \downarrow$ |  |  | 20 $\downarrow$ |  |  | ns |
| tsu | Setup Time (Notes 1 and 3) |  | 25 $\downarrow$ |  |  | 25 $\downarrow$ |  |  | ns |
| $t_{H}$ | Hold Time (Notes 1 and 2) |  | 0】 |  |  | 0 $\downarrow$ |  |  | ns |
| $\mathrm{t}_{\mathrm{H}}$ | Hold Time (Notes 1 and 3) |  | 5 $\downarrow$ |  |  | 5 $\downarrow$ |  |  | ns |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature |  | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Note 1: The symbol $(\downarrow)$ indicates the falling edge of the clock pulse is used for reference.
Note 2: $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$.
Note 3: $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| VOH | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\begin{aligned} & V_{C C}=M a x \\ & V_{1}=7 V \end{aligned}$ | J, K |  |  | 0.1 | mA |
|  |  |  | Clear |  |  | 0.3 |  |
|  |  |  | Clock |  |  | 0.4 |  |
| ${ }_{1 / \mathrm{H}}$ | High Level Input Current | $\begin{aligned} & V_{C C}=M a x \\ & V_{I}=2.7 V \end{aligned}$ | J, K |  |  | 20 | $\mu \mathrm{A}$ |
|  |  |  | Clear |  |  | 60 |  |
|  |  |  | Clock |  |  | 80 |  |
| IIL | Low Level Input Current | $\begin{aligned} & V_{C C}=M a x \\ & V_{I}=0.4 V \end{aligned}$ | J, K |  |  | -0.4 | mA |
|  |  |  | Clear |  |  | -0.8 |  |
|  |  |  | Clock |  |  | -0.8 |  |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & \text { (Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICC | Supply Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ (Note 3) |  |  | 4 | 6 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From (Input) To (Output) | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $C_{L}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  |  | Min | Max | Min | Max |  |
| ${ }_{\text {f MAX }}$ | Maximum Clock Frequency |  | 30 |  | 25 |  | MHz |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | $\begin{aligned} & \text { Clear } \\ & \text { to } \mathrm{Q} \end{aligned}$ |  | 20 |  | 28 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $\begin{aligned} & \text { Clear } \\ & \text { to } \bar{Q} \end{aligned}$ |  | 20 |  | 24 | ns |
| tPLH | Propagation Delay Time Low to High Level Output | Clock to Q or $\bar{Q}$ |  | 20 |  | 24 | ns |
| ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | Clock to Q or $\bar{Q}$ |  | 20 |  | 28 | ns |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state, an equivalent test may be performed where $\mathrm{V}_{\mathrm{O}}=2.25 \mathrm{~V}$ and 2.125 V for DM 54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.
Note 3: With all outputs open, ICC is measured with the $Q$ and $\bar{Q}$ outputs high in turn. At the time of measurement, the clock is grounded.

## 54LS74/DM54LS74A/DM74LS74A

## Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

## General Description

This device contains two independent positive-edge-triggered $D$ flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not
violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

## Features

- Alternate military/aerospace device (54LS74) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.


## Connection Diagram



TL/F/6373-1
Order Number 54LS74DMQB, 54LS74FMQB, 54LS74LMQB, DM54LS74AJ, DM54LS74AW, DM74LS74AM or DM74LS74AN See NS Package Number E20A, J14A, M14A, N14A or W14B

## Function Table

| Inputs |  |  |  |  | Outputs |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PR | CLR | CLK | D | Q | $\overline{\text { Q }}$ |  |
| L | $H$ | X | X | $H$ | L |  |
| H | L | X | X | L | $H$ |  |
| L | L | X | X | $H^{*}$ | $H^{*}$ |  |
| $H$ | $H$ | $\uparrow$ | $H$ | $H$ | L |  |
| $H$ | $H$ | $\uparrow$ | L | L | $H$ |  |
| $H$ | $H$ | L | X | $Q_{0}$ | $\bar{Q}_{0}$ |  |

[^12]* $=$ This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (high) level.
$Q_{0}=$ The output logic level of $Q$ before the indicated input conditions were established.


## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

## Supply Voltage

Input Voltage
Operating Free Air Temperature Range

DM54LS and 54LS
$-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
$0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$
Storage Temperature Range
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

| Symbol | Parameter |  | DM54LS74A |  |  | DM74LS74A |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{C C}$ | Supply Voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage |  | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  |  | 0.7 |  |  | 0.8 | V |
| ${ }_{\mathrm{OH}}$ | High Level Output Current |  |  |  | -0.4 |  |  | -0.4 | mA |
| $\mathrm{lOL}^{2}$ | Low Level Output Current |  |  |  | 4 |  |  | 8 | mA |
| $\mathrm{f}_{\mathrm{CLK}}$ | Clock Frequency (Note 2) |  | 0 |  | 25 | 0 |  | 25 | MHz |
| $\mathrm{f}_{\mathrm{CLK}}$ | Clock Frequency (Note 3) |  | 0 |  | 20 | 0 |  | 20 | MHz |
| tw | Pulse Width (Note 2) | Clock High | 18 |  |  | 18 |  |  | ns |
|  |  | Preset Low | 15 |  |  | 15 |  |  |  |
|  |  | Clear Low | 15 |  |  | 15 |  |  |  |
| tw | Pulse Width (Note 3) | Clock High | 25 |  |  | 25 |  |  | ns |
|  |  | Preset Low | 20 |  |  | 20 |  |  |  |
|  |  | Clear Low | 20 |  |  | 20 |  |  |  |
| tsu | Setup Time (Notes 1 and 2) |  | $20 \uparrow$ |  |  | $20 \uparrow$ |  |  | ns |
| $\mathrm{t}_{\text {SU }}$ | Setup Time (Notes 1 and 3) |  | $25 \uparrow$ |  |  | $25 \uparrow$ |  |  | ns |
| $\mathrm{t}_{\mathrm{H}}$ | Hold Time (Note 1 and 4) |  | $0 \uparrow$ |  |  | $0 \uparrow$ |  |  | ns |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature |  | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Note 1: The symbol $(\uparrow)$ indicates the rising edge of the clock pulse is used for reference.
Note 2: $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, and $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$.
Note 3: $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, and $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$.
Note 4: $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| VOH | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\ & V_{I L}=\operatorname{Max}, V_{I H}=M i n \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @Max Input Voltage | $\begin{aligned} & V_{C C}=M a x \\ & V_{1}=7 V \end{aligned}$ | Data |  |  | 0.1 | mA |
|  |  |  | Clock |  |  | 0.1 |  |
|  |  |  | Preset |  |  | 0.2 |  |
|  |  |  | Clear |  |  | 0.2 |  |
| $\mathrm{IIH}^{\text {H}}$ | High Level Input Current | $\begin{aligned} & V_{C C}=M a x \\ & V_{1}=2.7 V \end{aligned}$ | Data |  |  | 20 | $\mu \mathrm{A}$ |
|  |  |  | Clock |  |  | 20 |  |
|  |  |  | Clear |  |  | 40 |  |
|  |  |  | Preset |  |  | 40 |  |
| IIL | Low Level Input Current | $\begin{aligned} & V_{\mathrm{CC}}=\mathrm{Max} \\ & V_{\mathrm{I}}=0.4 \mathrm{~V} \end{aligned}$ | Data |  |  | -0.4 | mA |
|  |  |  | Clock |  |  | -0.4 |  |
|  |  |  | Preset |  |  | -0.8 |  |
|  |  |  | Clear |  |  | -0.8 |  |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & (\text { Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| Icc | Supply Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ (Note 3) |  |  | 4 | 8 | mA |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where $\mathrm{V}_{\mathrm{O}}=2.25 \mathrm{~V}$ and 2.125 V for DM 54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.
Note 3: With all outputs open, $I_{C C}$ is measured with CLOCK grounded after setting the $Q$ and $\bar{Q}$ outputs high in turn.
Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From (Input) To (Output) | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $C_{L}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  |  | Min | Max | Min | Max |  |
| $\mathrm{f}_{\text {MAX }}$ | Maximum Clock Frequency |  | 25 |  | 20 |  | MHz |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | Clock to Q or $\bar{Q}$ |  | 25 |  | 35 | ns |
| ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | Clock to Q or $\bar{Q}$ |  | 30 |  | 35 | ns |
| tpLH | Propagation Delay Time Low to High Level Output | Preset <br> to Q |  | 25 |  | 35 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | Preset to $\bar{Q}$ |  | 30 |  | 35 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $\begin{aligned} & \text { Clear } \\ & \text { to } \bar{Q} \end{aligned}$ |  | 25 |  | 35 | ns |
| ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | $\begin{aligned} & \text { Clear } \\ & \text { to } Q \end{aligned}$ |  | 30 |  | 35 | ns |

## DM54LS75/DM74LS75 Quad Latches

## General Description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data ( $D$ ) input is transferred to the $Q$ output when the enable is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low,
the information (that was present at the data input at the time the transition occured) is retained at the Q output until the enable is permitted to go high.
These latches feature complementary Q and $\overline{\mathrm{Q}}$ outputs from a 4-bit latch, and are available in 16-pin packages.

Function Table (Each Latch)

| Inputs |  | Outputs |  |
| :---: | :---: | :---: | :---: |
| $\mathbf{D}$ | Enable | $\mathbf{Q}$ | $\overline{\mathbf{Q}}$ |
| L | $H$ | L | H |
| $H$ | $H$ | $H$ | L |
| X | L | $\mathrm{Q}_{0}$ | $\overline{\mathrm{Q}}_{0}$ |

$H=$ High Level, $L=$ Low Level, $X=$ Don't Care
$Q_{0}=$ The Level of $Q$ Before the High-to-Low Transition of ENABLE

| Absolute Maximum Ratings (Note) |  |
| :--- | ---: |
| If Milltary/Aerospace specified devices are required, |  |
| please contact the National Semiconductor Sales |  |
| Office/Distributors for availability and specifications. |  |
| Supply Voltage | 7 V |
| Input Voltage | 7 V |
| Operating Free Air Temperature Range | $-55^{\circ} \mathrm{C}$ o $+125^{\circ} \mathrm{C}$ |
| DM54LS | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| DM74LS | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS75 |  |  | DM74LS75 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $V_{C C}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| ${ }_{\mathrm{OH}}$ | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| $\mathrm{lOL}^{\text {l }}$ | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| tw | Enable Pulse Width (Note 4) | 20 |  |  | 20 |  |  | ns |
| tsu | Setup Time (Note 4) | 20 |  |  | 20 |  |  | ns |
| $\mathrm{t}_{\mathrm{H}}$ | Hold Time (Note 4) | 0 |  |  | 0 |  |  | ns |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ <br> (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{I}}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | DM54 | 2.5 | 3.5 |  | V |
|  |  |  | DM74 | 2.7 | 3.5 |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}$ | D |  |  | 0.1 | mA |
|  |  |  | Enable |  |  | 0.4 |  |
| ${ }_{1 / H}$ | High Level Input Current | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ | D |  |  | 20 | $\mu \mathrm{A}$ |
|  |  |  | Enable |  |  | 80 |  |
| IIL | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=0.4 \mathrm{~V}$ | D |  |  | -0.4 | mA |
|  |  |  | Enable |  |  | -1.6 |  |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & \text { (Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICC | Supply Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ (Note 3) |  |  | 6.3 | 12 | mA |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: $I_{C C}$ is measured with all outputs open and all inputs grounded.
Note 4: $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$.

| Symbol | Parameter | From (Input) <br> To (Output) | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}$ |  |  |
|  |  |  | Min | Max | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $\begin{gathered} D \text { to } \\ \mathrm{Q} \end{gathered}$ |  | 27 |  | 30 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | $\begin{gathered} \mathrm{D} \text { to } \\ \mathrm{Q} \\ \hline \end{gathered}$ |  | 17 |  | 25 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $D \text { to }$ $\overline{\mathrm{Q}}$ |  | 20 |  | 25 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | $\begin{gathered} \mathrm{D} \text { to } \\ \overline{\mathrm{Q}} \\ \hline \end{gathered}$ |  | 15 |  | 20 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | Enable to Q |  | 27 |  | 30 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | Enable to $\mathrm{Q}$ |  | 25 |  | 30 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | Enable to $\bar{Q}$ |  | 30 |  | 30 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | Enable to $\bar{Q}$ |  | 15 |  | 20 | ns |

## 54LS83A/DM54LS83A/DM74LS83A 4-Bit Binary Adders with Fast Carry

## General Description

These full adders perform the addition of two 4-bit binary numbers. The sum ( $\Sigma$ ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial lookahead performance at the economy and reduced package count of a ripple-carry implementation.
The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

## Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times

Two 8-bit words 25 ns
Two 16-bit words 45 ns

- Typical power dissipation per 4-bit adder 95 mW
- Alternate Military/Aerospace device (54LS83A) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.


## Connection Diagram



TL/F/6378-1
Order Number 54LS83ADMQB, 54LS83AFMQB, DM54LS83AJ, DM54LS83AW, DM74LS83AWM or DM74LS83AN See NS Package Number J16A, M16B, N16E or W16A

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage | 7 V |
| :--- | ---: |
| Input Voltage | 7 V |
| Operating Free Air Temperature Range |  |
| DM54LS and 54LS | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| DM74LS | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS83A |  |  | DM74LS83A |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| ${ }^{\mathrm{OH}}$ | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating tree air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| VOL | Low Level Output Voltage | $\begin{aligned} & V_{C C}=\operatorname{Min}, \mathrm{IOL}_{\mathrm{O}}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\begin{aligned} & V_{C C}=M a x \\ & V_{1}=7 V \end{aligned}$ | A or B |  |  | 0.2 | mA |
|  |  |  | CO |  |  | 0.1 |  |
| $\mathrm{IIH}^{\text {H}}$ | High Level Input Current | $\begin{aligned} & V_{C C}=M a x \\ & V_{1}=2.7 V \end{aligned}$ | A or B |  |  | 40 | $\mu \mathrm{A}$ |
|  |  |  | C0 |  |  | 20 |  |
| IIL | Low Level Input Current | $\begin{aligned} & V_{C C}=M a x \\ & V_{1}=0.4 V \end{aligned}$ | A or B |  |  | -0.8 | mA |
|  |  |  | CO |  |  | -0.4 |  |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & \text { (Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| $\mathrm{ICC1}$ | Supply Current | $\mathrm{V}_{C C}=\operatorname{Max}$ (Note 3) |  |  | 19 | 34 | mA |
| ICC2 | Supply Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ (Note 4) |  |  | 22 | 39 | mA |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: $\mathrm{I}_{\mathrm{C} 1}$ is measured with all outputs open, all B inputs low and all other inputs at 4.5 V , or all inputs at 4.5 V .
Note 4: $I_{\mathrm{CC} 2}$ is measured with all outputs open and all inputs grounded.

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From (Input) To (Output) | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $C_{L}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}$ |  |  |
|  |  |  | Min | Max | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $\begin{gathered} \mathrm{CO} \text { to } \\ \Sigma 1 \text { or } \Sigma 2 \end{gathered}$ |  | 24 |  | 28 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | $\begin{gathered} \mathrm{CO} \text { to } \\ \Sigma 1 \text { or } \Sigma 2 \end{gathered}$ |  | 24 |  | 30 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $\begin{gathered} \mathrm{CO} \text { to } \\ \Sigma 3 \\ \hline \end{gathered}$ |  | 24 |  | 28 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | $\begin{gathered} \mathrm{C} 0 \text { to } \\ \Sigma 3 \end{gathered}$ |  | 24 |  | 30 | ns |
| tple | Propagation Delay Time Low to High Level Output | $\begin{gathered} \mathrm{CO} \text { to } \\ \Sigma 4 \\ \hline \end{gathered}$ |  | 24 |  | 28 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | $\begin{gathered} \mathrm{C} 0 \text { to } \\ \Sigma 4 \\ \hline \end{gathered}$ |  | 24 |  | 30 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $\begin{aligned} & A_{i}, B_{i} \\ & \text { to } \Sigma_{i} \end{aligned}$ |  | 24 |  | 28 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | $\begin{aligned} & A_{i}, B_{i} \\ & \text { to } \Sigma_{i} \end{aligned}$ |  | 24 |  | 30 | ns |
| $\mathrm{t}_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $\begin{gathered} \mathrm{C} 0 \text { to } \\ \mathrm{C} 4 \\ \hline \end{gathered}$ |  | 17 |  | 24 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | $\begin{gathered} \mathrm{C} 0 \text { to } \\ \mathrm{C} 4 \\ \hline \end{gathered}$ |  | 17 |  | 25 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $\begin{aligned} & \mathrm{A}_{\mathrm{i}}, \mathrm{~B}_{\mathrm{i}} \\ & \text { to } \mathrm{C} 4 \end{aligned}$ |  | 17 |  | 24 | ns |
| tPHL | Propagation Delay Time High to Low Level Output | $\begin{aligned} & \mathrm{A}_{\mathrm{i}}, \mathrm{~B}_{\mathrm{i}} \\ & \text { to } \mathrm{C} 4 \\ & \hline \end{aligned}$ |  | 17 |  | 26 | ns |

## Truth Table

(

Note: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs $\Sigma 1$ and $\Sigma 2$ and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs $\Sigma 3, \Sigma 4$, and C 4 .


TL/F/6378-2

## 54LS85/DM54LS85/DM74LS85 4-Bit Magnitude Comparators

## General Description

These 4-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two, 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The $A>B, A<B$, and $A=B$ outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must
have a high-level voltage applied to the $A=B$ input. The cascading path is implemented with only a two-gate-level delay to reduce overall comparison times for long words.

## Features

- Typical power dissipation 52 mW
- Typical delay (4-bit words) 24 ns
- Alternate Military/Aerospace device (54LS85) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.


## Connection Diagram



Order Number 54LS85DMQB, 54LS85FMQB, 54LS85LMQB, DM54LS85J, DM54LS85W, DM74LS85M or DM74LS85N See NS Package Number E20A, J16A, M16A, N16E or W16A

## Function Table

| Comparing Inputs |  |  |  | Cascading Inputs |  |  | Outputs |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A3, B3 | A2, B2 | A1, B1 | AO, B0 | A $>$ B | $\mathbf{A}<\mathbf{B}$ | $A=B$ | A $>$ B | A<B | $\mathbf{A}=\mathbf{B}$ |
| A3 $>$ B3 | X | X | X | X | X | X | H | L | L |
| A3 < B3 | X | X | X | X | X | X | L | H | L |
| $A 3=B 3$ | $\mathrm{A} 2>\mathrm{B} 2$ | X | X | X | X | X | H | L | L |
| A3 $=$ B3 | $\mathrm{A} 2<\mathrm{B} 2$ | X | X | X | X | X | L | H | L |
| $A 3=B 3$ | $\mathrm{A} 2=\mathrm{B} 2$ | A1 > B1 | X | X | X | X | H | L | L |
| $A 3=B 3$ | $\mathrm{A} 2=\mathrm{B} 2$ | A1 < B1 | X | X | X | X | L | H | L |
| $A 3=B 3$ | $\mathrm{A} 2=\mathrm{B} 2$ | $A 1=B 1$ | $\mathrm{AO}>\mathrm{BO}$ | X | X | X | H | L | L |
| $\mathrm{A} 3=\mathrm{B} 3$ | $\mathrm{A} 2=\mathrm{B} 2$ | $A 1=B 1$ | $\mathrm{AO}<\mathrm{BO}$ | X | X | X | L | H | L |
| $A 3=B 3$ | $\mathrm{A} 2=\mathrm{B} 2$ | $A 1=B 1$ | $A O=B 0$ | H | L | L | H | L | L |
| $A 3=B 3$ | $\mathrm{A} 2=\mathrm{B} 2$ | $A 1=B 1$ | $A O=B O$ | L | H | L | L | H | L |
| $A 3=B 3$ | $\mathrm{A} 2=\mathrm{B} 2$ | $A 1=B 1$ | $A O=B 0$ | L | L | H | L | L | H |
| $A 3=B 3$ | $\mathrm{A} 2=\mathrm{B} 2$ | $A 1=B 1$ | $A 0=B 0$ | X | X | H | L | L | H |
| $A 3=B 3$ | $\mathrm{A} 2=\mathrm{B} 2$ | $\mathrm{A} 1=\mathrm{B1}$ | $A 0=B 0$ | H | H | L | L | L | L |
| $\mathrm{A} 3=\mathrm{B} 3$ | $\mathrm{A} 2=\mathrm{B} 2$ | $\mathrm{A} 1=\mathrm{B1}$ | $A 0=B 0$ | L | L | L | H | H | L |

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
Operating Free Air Temperature Range

DM54LS and 54LS
$-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
$0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$
Storage Temperature Range

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

| Symbol | Parameter | DM54LS85 |  |  | DM74LS85 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\mathrm{IL}}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| IOH | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ <br> (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\text {OL }}$ | Low Level Output Voltage | $\begin{aligned} & V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\ & V_{I L}=M a x, V_{I H}=\operatorname{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\begin{aligned} & V_{\mathrm{CC}}=\mathrm{Max} \\ & V_{1}=7 \mathrm{~V} \end{aligned}$ | $A<B$ |  |  | 0.1 | mA |
|  |  |  | $A>B$ |  |  | 0.1 |  |
|  |  |  | Others |  |  | 0.3 |  |
| $\mathrm{IIH}_{\mathrm{H}}$ | High Level Input Current | $\begin{aligned} & V_{C C}=M a x \\ & V_{1}=2.7 V \end{aligned}$ | $A<B$ |  |  | 20 | $\mu \mathrm{A}$ |
|  |  |  | $A>B$ |  |  | 20 |  |
|  |  |  | Others |  |  | 60 |  |
| IIL | Low Level Input Current | $\begin{aligned} & V_{C C}=\operatorname{Max} \\ & V_{1}=0.4 V \end{aligned}$ | $A<B$ |  |  | -0.4 | mA |
|  |  |  | A $>$ B |  |  | -0.4 |  |
|  |  |  | Others |  |  | -1.2 |  |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=\text { Max } \\ & \text { (Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICC | Supply Current | $\mathrm{V}_{C C}=\operatorname{Max}$ (Note 3) |  |  | 10 | 20 | mA |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: ICC is measured with all outputs open, $A=B$ grounded and all other inputs at 4.5 V .

Switching Characteristics at $\mathrm{V}_{C C}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From Input | To Output | Number of Gate Levels | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  |  |  |  | Min | Max | Min | Max |  |
| ${ }^{\text {PLLH }}$ | Propagation Delay Time Low-to-High Level Output | Any A or B Data Input | $\begin{aligned} & A<B, \\ & A>B \end{aligned}$ | 3 |  | 36 |  | 42 | ns |
|  |  |  | $A=B$ | 4 |  | 40 |  | 40 |  |
| tPHL | Propagation Delay Time High-to-Low Level Output | Any A or B Data Input | $\begin{aligned} & A<B, \\ & A>B \end{aligned}$ | 3 |  | 30 |  | 40 | ns |
|  |  |  | $\mathrm{A}=\mathrm{B}$ | 4 |  | 30 |  | 40 |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low-to-High Level Output | $\begin{gathered} A<B \\ \text { or } A=B \end{gathered}$ | A > B | 1 |  | 22 |  | 26 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High-to-Low Level Output | $\begin{gathered} A<B \\ \text { or } A=B \end{gathered}$ | A > B | 1 |  | 17 |  | 26 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low-to-High Level Output | $A=B$ | $\mathrm{A}=\mathrm{B}$ | 2 |  | 20 |  | 25 | ns |
| tPHL | Propagation Delay Time High-to-Low Level Output | $A=B$ | $A=B$ | 2 |  | 17 |  | 26 | ns |
| ${ }_{\text {tpLH }}$ | Propagation Delay Time Low-to-High Level Output | $\begin{gathered} A>B \\ \text { or } A=B \end{gathered}$ | $\mathrm{A}<\mathrm{B}$ | 1 |  | 22 |  | 26 | ns |
| tPHL | Propagation Delay Time High-to-Low Level Output | $\begin{gathered} A>B \\ \text { or } A=B \end{gathered}$ | A < B | 1 |  | 17 |  | 26 | ns |

## Logic Diagram



TL/F/6379-2

## DM54LS86/DM74LS86

## Quad 2-Input Exclusive-OR Gates

## General Description

This device contains four independent gates each of which performs the logic exclusive-OR function.

## Connection Diagram



TL/F/6380-1
Order Number DM54LS86J, DM54LS86W, DM74LS86M or DM74LS86N See NS Package Number J14A, M14A, N14A or W14B

Function Table

$$
\mathbf{Y}=\mathbf{A} \oplus \mathbf{B}=\overline{\mathbf{A}} \mathbf{B}+\mathbf{A} \overline{\mathbf{B}}
$$

| Inputs |  | Output |
| :---: | :---: | :---: |
| $\mathbf{A}$ | $\mathbf{B}$ | $\mathbf{Y}$ |
| $L$ | $L$ | $L$ |
| $L$ | $H$ | $H$ |
| $H$ | $L$ | $H$ |
| $H$ | $H$ | $L$ |

$$
H=\text { High Logic Level }
$$

L = Low Logic Level

| Absolute Maximum Ratings (Note) |
| :--- |
| If Military/Aerospace specified devices are required, |
| please contact the National Semiconductor Sales |
| Office/Distributors for availability and specifications. |
| Supply Voltage |
| Input Voltage |
| Operating Free Air Temperature Range |
| DM54LS |
| DM74LS |
| Storage Temperature Range |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS86 |  |  | DM74LS86 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $V_{\text {CC }}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| IOH | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & V_{C C}=M i n, I_{O L}=M a x \\ & V_{I L}=M a x, V_{I H}=M i n \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{IOL}=4 \mathrm{~mA}$, | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}$ |  |  |  | 0.2 | mA |
| $\mathrm{I}_{\mathrm{H}}$ | High Level Input Current | $V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 40 | $\mu \mathrm{A}$ |
| 111 | Low Level Input Current | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.6 | mA |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & (\text { Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICCH | Supply Current with Outputs High | $\begin{aligned} & V_{\mathrm{CC}}=M a x \\ & \text { (Note 3) } \\ & \hline \end{aligned}$ |  |  | 6.1 | 10 | mA |
| ${ }^{\text {ICCL }}$ | Supply Current with Outputs Low | $\begin{aligned} & V_{\mathrm{CC}}=\mathrm{Max} \\ & (\text { Note 4) } \end{aligned}$ |  |  | 9 | 15 | mA |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3 : $\mathrm{I}_{\mathrm{CCH}}$ is measured with all outputs open, one input at each gate at 4.5 V , and the other inputs grounded.
Note 4: ICCL is measured with all outputs open and all inputs grounded.

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | Condilions | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $C_{L}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}$ |  |  |
|  |  |  | Min | Max | Min | Max |  |
| tPLH | Propagation Delay Time Low to High Level Output | Other Input Low |  | 18 |  | 23 | ns |
| ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output |  |  | 17 |  | 21 | ns |
| tpLH | Propagation Delay Time Low to High Level Output | Other <br> Input High |  | 10 |  | 15 | ns |
| ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output |  |  | 12 |  | 15 | ns |

## DM74LS90/DM74LS93 <br> Decade and Binary Counters

## General Description

Each of these monolithic counters contains four masterslave flip-flops and additional gating to provide a divide-bytwo counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 'LS90 and divide-by-eight for the 'LS93.
All of these counters have a gated zero reset and the LS90 also has gated set-to-nine inputs for use in BCD nine's complement applications.
To use their maximum count length (decade or four bit bina$r y$ ), the $B$ input is connected to the $Q_{A}$ output. The input
count pulses are applied to input $A$ and the outputs are as described in the appropriate truth table. A symmetrical di-vide-by-ten count can be obtained from the 'LS90 counters by connecting the $Q_{D}$ output to the $A$ input and applying the input count to the $B$ input which gives a divide-by-ten square wave at output $Q_{A}$.

## Features

- Typical power dissipation 45 mW
- Count frequency 42 MHz


## Connection Diagrams (Dual-In-Line Packages)



TL/F/6381-1
Order Number DM74LS90M or DM74LS90N See NS Package Number M14A or N14A


TL/F/6381-2
Order Number DM74LS93M or DM74LS93N See NS Package Number M14A or N14A

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

| Symbol | Parameter |  | DM74LS90 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Nom | Max |  |
| $V_{C C}$ | Supply Voltage |  | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{H}}$ | High Level Input Voltage |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  |  | 0.8 | V |
| IOH | High Level Output Current |  |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  |  | 8 | mA |
| $f_{\text {fle }}$ | Clock Frequency (Note 1) | $A$ to $Q_{A}$ | 0 |  | 32 | MHz |
|  |  | $B$ to $Q_{B}$ | 0 |  | 16 |  |
| ${ }_{\text {f CLK }}$ | Clock Frequency (Note 2) | $A$ to $Q_{A}$ | 0 |  | 20 | MHz |
|  |  | $B$ to $Q_{B}$ | 0 |  | 10 |  |
| tw | Pulse Width (Note 1) | A | 15 |  |  | ns |
|  |  | B | 30 |  |  |  |
|  |  | Reset | 15 |  |  |  |
| tw | Pulse Width (Note 2) | A | 25 |  |  | ns |
|  |  | B | 50 |  |  |  |
|  |  | Reset | 25 |  |  |  |
| $t_{\text {REL }}$ | Reset Release Time (Note 1) |  | 25 |  |  | ns |
| $t_{\text {REL }}$ | Reset Release Time (Note 2) |  | 35 |  |  | ns |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature |  | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Note 1: $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$.
Note 2: $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$.

## 'LS90 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ <br> (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\ & V_{\mathrm{IL}}=\operatorname{Max}, V_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ |  | 2.7 | 3.4 |  | V |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & V_{C C}=M i n, I_{O L}=M a x \\ & V_{I L}=M a x, V_{I H}=M i n \\ & \text { (Note 4) } \end{aligned}$ |  |  | 0.35 | 0.5 | V |
|  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ |  |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}$ | Reset |  |  | 0.1 | mA |
|  |  | $\begin{aligned} & V_{C C}=M a x \\ & V_{1}=5.5 V \end{aligned}$ | A |  |  | 0.2 |  |
|  |  |  | B |  |  | 0.4 |  |


| 'LS90 Electrical Characteristics <br> over recommended operating free air temperature range (unless otherwise noted) (Continued) |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Parameter | Conditions |  | Min | Typ <br> (Note 1) | Max | Units |
| $\mathrm{IIH}^{\text {H}}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ | Reset |  |  | 20 | $\mu \mathrm{A}$ |
|  |  |  | A |  |  | 40 |  |
|  |  |  | B |  |  | 80 |  |
| IIL | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ | Reset |  |  | -0.4 | mA |
|  |  |  | A |  |  | -2.4 |  |
|  |  |  | B |  |  | $-3.2$ |  |
| los | Short Circuit Output Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ (Note 2) |  | -20 |  | -100 | mA |
| ICC | Supply Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ (Note 3) |  |  | 9 | 15 | mA |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I ICC is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5 V and all other inputs grounded.
Note 4: $Q_{A}$ outputs are tested at $I_{O L}=$ Max plus the limit value of $l_{L L}$ for the $B$ input. This permits driving the $B$ input while maintaining full fan-out capability.

## 'LS90 Switching Characteristics

at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From (Input) To (Output) | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $C_{L}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}$ |  |  |
|  |  |  | Min | Max | Min | Max |  |
| $f_{\text {MAX }}$ | Maximum Clock Frequency | A to $Q_{A}$ | 32 |  | 20 |  | MHz |
|  |  | $B$ to $Q_{B}$ | 16 |  | 10 |  |  |
| tpLH | Propagation Delay Time Low to High Level Output | A to $Q_{A}$ |  | 16 |  | 20 | ns |
| ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | $A$ to $Q_{A}$ |  | 18 |  | 24 | ns |
| $\mathrm{t}_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | A to $Q_{D}$ |  | 48 |  | 52 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | A to $Q_{D}$ |  | 50 |  | 60 | ns |
| ${ }_{\text {tPLH }}$ | Propagation Delay Time Low to High Level Output | $B$ to $Q_{B}$ |  | 16 |  | 23 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | $B$ to $Q_{B}$ |  | 21 |  | 30 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $B$ to $Q_{C}$ |  | 32 |  | 37 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | $B$ to $Q_{C}$ |  | 35 |  | 44 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $B$ to $Q_{D}$ |  | 32 |  | 36 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | $B$ to $Q_{D}$ |  | 35 |  | 44 | ns |
| ${ }_{\text {PLLH }}$ | Propagation Delay Time Low to High Level Output | SET-9 to $Q_{A}, Q_{D}$ |  | 30 |  | 35 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | SET-9 to $\mathrm{Q}_{\mathrm{B}}, \mathrm{Q}_{\mathrm{C}}$ |  | 40 |  | 48 | ns |
| ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | SET-0 to Any Q |  | 40 |  | 52 | ns |

Recommended Operating Conditions

| Symbol | Parameter |  | DM74LS93 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Nom | Max |  |
| $V_{C C}$ | Supply Voltage |  | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  |  | 0.8 | V |
| IOH | High Level Output Current |  |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  |  | 8 | mA |
| ${ }_{\text {f CLK }}$ | Clock Frequency (Note 1) | $A$ to $Q_{A}$ | 0 |  | 32 | MHz |
|  |  | $B$ to $Q_{B}$ | 0 |  | 16 |  |
| ${ }_{\text {f CLK }}$ | Clock Frequency (Note 2) | $A$ to $Q_{A}$ | 0 |  | 20 |  |
|  |  | $B$ to $Q_{B}$ | 0 |  | 10 |  |
| tw | Pulse Width (Note 1) | A | 15 |  |  | ns |
|  |  | B | 30 |  |  |  |
|  |  | Reset | 15 |  |  |  |
| tw | Pulse Width (Note 2) | A | 25 |  |  | ns |
|  |  | B | 50 |  |  |  |
|  |  | Reset | 25 |  |  |  |
| $t_{\text {REL }}$ | Reset Release Time (Note 1) |  | 25 |  |  | ns |
| $\mathrm{t}_{\text {REL }}$ | Reset Release Time (Note 2) |  | 35 |  |  | ns |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature |  | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Note 1: $C_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$.
Note 2: $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$.

## 'LS93 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\text {OH }}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOH}_{=}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ |  | 2.7 | 3.4 |  | V |
| $\mathrm{V}_{\text {OL }}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\text { Min } \\ & \text { (Note 4) } \end{aligned}$ |  |  | 0.35 | 0.5 | V |
|  |  | $\mathrm{IOL}^{\text {a }}=4 \mathrm{~mA}, \mathrm{~V}_{\text {CC }}=\mathrm{Min}$ |  |  | 0.25 | 0.4 |  |
| 1 | Input Current @Max Input Voltage | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}$ | Reset |  |  | 0.1 |  |
|  |  | $\begin{aligned} & V_{c c}=\operatorname{Max} \\ & V_{1}=5.5 \mathrm{~V} \end{aligned}$ | A |  |  | 0.2 | mA |
|  |  |  | B |  |  | 0.4 |  |
| $\mathrm{IIH}^{\text {H}}$ | High Level Input Current | $\begin{aligned} & V_{C C}=M a x \\ & V_{1}=2.7 V \end{aligned}$ | Reset |  |  | 20 |  |
|  |  |  | A |  |  | 40 | $\mu \mathrm{A}$ |
|  |  |  | B |  |  | 80 |  |

## 'LS93 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ILL | Low Level Input Current | $V_{C C}=\operatorname{Max}, V_{1}=0.4 \mathrm{~V}$ | Reset |  |  | -0.4 | mA |
|  |  |  | A |  |  | -2.4 |  |
|  |  |  | B |  |  | -1.6 |  |
| los | Short Circuit Output Current | $\mathrm{V}_{\text {CC }}=\mathrm{Max}($ Note 2) |  | -20 |  | -100 | mA |
| Icc | Supply Current | $\mathrm{V}_{\text {CC }}=\mathrm{Max}$ (Note 3) |  |  | 9 | 15 | mA |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: ICC is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5 V and all other inputs grounded.
Note 4: $Q_{A}$ outputs are tested at $l_{\mathrm{OL}}=$ max plus the limit value of $\mathrm{I}_{\mathrm{IL}}$ for the B input. This permits driving the $B$ input while maintaining full fan-out capability.

## 'LS93 Switching Characteristics

at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From (Input) To (Output) | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  |  | Min | Max | Min | Max |  |
| $f_{\text {MAX }}$ | Maximum Clock Frequency | $A$ to $Q_{A}$ | 32 |  | 20 |  | MHz |
|  |  | $B$ to $Q_{B}$ | 16 |  | 10 |  |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | A to $Q_{A}$ |  | 16 |  | 20 | ns |
| ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | A to $Q_{A}$ |  | 18 |  | 24 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | A to $Q_{D}$ |  | 70 |  | 85 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | $A$ to $Q_{D}$ |  | 70 |  | 90 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $B$ to $Q_{B}$ |  | 16 |  | 23 | ns |
| ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | $B$ to $Q_{B}$ |  | 21 |  | 30 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $B$ to $Q_{C}$ |  | 32 |  | 37 | ns |
| ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | $B$ to $Q_{C}$ |  | 35 |  | 44 | ns |
| $t_{\text {PL }}$ | Propagation Delay Time Low to High Level Output | $B$ to $Q_{D}$ |  | 51 |  | 60 | ns |
| ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | $B$ to $Q_{D}$ |  | 51 |  | 70 | ns |
| ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | SET-0 to Any Q |  | 40 |  | 52 | ns |

Function Tables

| LS90 BCD Count Sequence (See Note A) |  |  |  |  | $\begin{gathered} \text { LS90 } \\ \text { Bi-Quinary (5-2) } \\ \text { (See Note B) } \\ \hline \end{gathered}$ |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Count | Output |  |  |  | Count | Output |  |  |  |
|  | $Q_{D}$ | $Q_{C}$ | $\mathbf{Q}_{B}$ | $\mathbf{Q}_{\mathbf{A}}$ |  | $\mathbf{Q}_{\mathbf{A}}$ | $Q_{D}$ | $Q_{C}$ | $\mathbf{Q}_{\mathbf{B}}$ |
| 0 | L | L | L | L | 0 | L | L | L | L |
| 1 | L | L | L | H | 1 | L | L | L | H |
| 2 | L | L | H | L | 2 | L | L | H | L |
| 3 | L | L | H | H | 3 | L | L | H | H |
| 4 | L | H | L | L | 4 | L | H | L | L |
| 5 | L | H | L | H | 5 | H | L | L | L |
| 6 | L | H | H | L | 6 | H | L | L | H |
| 7 | L | H | H | H | 7 | H | L | H | L |
| 8 | H | L | L | L | 8 | H | L | H | H |
| 9 | H | L | L | H | 9 | H | H | L | L |

LS93 Count Sequence
(See Note C)

| Count | Output |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | $Q_{D}$ | $Q_{C}$ | $Q_{B}$ | $\mathbf{Q}_{\mathbf{A}}$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

LS90
Reset/Count Truth Table

| Reset Inputs |  |  |  |  | Output |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| R0(1) | R0(2) | R9(1) | R9(2) | $\mathbf{Q}_{\mathbf{D}}$ | $\mathbf{Q}_{\mathbf{C}}$ | $\mathbf{Q}_{\mathbf{B}}$ | $\mathbf{Q}_{\mathbf{A}}$ |  |
| H | H | L | X | L | L | L | L |  |
| H | H | X | L | L | L | L | L |  |
| X | X | H | H | H | L | L | H |  |
| X | L | X | L |  | COUNT |  |  |  |
| L | X | L | X |  | COUNT |  |  |  |
| L | X | X | L |  | COUNT |  |  |  |
| X | L | L | X |  | COUNT |  |  |  |

LS93
Reset/Count Truth Table

| Reset Inputs |  | Output |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| RO(1) | RO(2) | $\mathbf{Q}_{\mathbf{D}}$ | $\mathbf{Q}_{\mathbf{C}}$ | $\mathbf{Q}_{\mathbf{B}}$ | $\mathbf{Q}_{\mathbf{A}}$ |
| H | H | L | L | L | L |
| L | X |  | COUNT |  |  |
| X | L | COUNT |  |  |  |

Note $A$ : Output $Q_{A}$ is connected to input $B$ for $B C D$ count.
Note B: Output $Q_{D}$ is connected to input $A$ for bi-quinary count.
Note C: Output $Q_{A}$ is connected to input $B$.
Note D: $\mathrm{H}=$ High Level, $\mathrm{L}=$ Low Level, $\mathrm{X}=$ Don't Care.


## 54LS95B/DM74LS95B

## 4-Bit Right/Left Shift Register

## General Description

The 'LS95B is a 4-bit shift register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel $D$ inputs to the Q outputs synchronous with the HIGH-to-LOW transition of the appropriate clock input.

## Features

■ Synchronous, expandable shift right

- Synchronous shift left capability
- Synchronous parallel load
- Separate shift and load clock inputs


## Connection Diagram

Dual-In-Line Package


Logic Symbol


TL/F/10175-2
$V_{C C}=\operatorname{Pin} 14$
GND $=\operatorname{Pin} 7$

TL/F/10175-1
Order Number 54LS95BDMQB, 54LS95BFMQB,
DM74LS95BM or DM74LS95BN
See NS Package Number J14A, M14A, N14A or W14B

| Pin Names | Description |
| :--- | :--- |
| $\overline{\mathrm{CP}} 1$ | Serial Clock Input (Active Falling Edge) |
| $\overline{\mathrm{CP}} 2$ | Parallel Clock Input (Active Falling Edge) |
| D | Serial Data Input |
| P0-P3 | Parallel Data Inputs |
| PE | Parallel Enable Input (Active HIGH) |
| Q0-Q3 | Parallel Outputs |

Absolute Maximum Ratings (Note)

If Milltary/Aerospace specifled devices are required, please contact the Natlonal Semiconductor Sales Office/Distributors for avallability and specifications.
Supply Voltage
Input Voltage
Operating Free Air Temperature Range

| 54LS | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| :--- | ---: |
| DM74LS | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions $\mathrm{v}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$

| Symbol | Parameter | 54LS95 |  |  | DM74LS95 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $V_{C C}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| IOH | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |
| $\begin{aligned} & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\ & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \end{aligned}$ | Setup Time HIGH or LOW Ds or Pn to $\overline{\mathrm{CP}} \mathrm{n}$ | $\begin{aligned} & 20 \\ & 20 \\ & \hline \end{aligned}$ |  |  | $\begin{aligned} & 20 \\ & 20 \\ & \hline \end{aligned}$ |  |  | ns |
| $\begin{aligned} & t_{h}(H) \\ & t_{h}(L) \end{aligned}$ | Hold Time HIGH or LOW $\mathrm{D}_{\mathrm{S}}$ or Pn to $\overline{\mathrm{CP}} \mathrm{n}$ | $\begin{aligned} & 10 \\ & 10 \\ & \hline \end{aligned}$ |  |  | $\begin{aligned} & 10 \\ & 10 \\ & \hline \end{aligned}$ |  |  | ns |
| $t_{w}(H)$ | $\overline{\text { CPn Pulse Width HIGH }}$ | 20 |  |  | 20 |  |  | ns |
| $t_{\text {en }}(\mathrm{L})$ | Enable Time LOW, PE to $\overline{\mathrm{CP}} 1$ | 25 |  |  | 25 |  |  | ns |
| $t_{\text {inh }}(H)$ | Inhibit Time HIGH, PE to CP1 | 20 |  |  | 20 |  |  | ns |
| $t_{\text {en }}(H)$ | Enable Time HIGH, PE to $\overline{\mathrm{CP}} 2$ | 25 |  |  | 25 |  |  | ns |
| $\mathrm{t}_{\text {inh }}(\mathrm{L})$ | Inhibit Time LOW, PE to $\overline{\mathrm{CP}} 2$ | 20 |  |  | 20 |  |  | ns |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| VOH | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\text { Max, } \\ & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max} \end{aligned}$ | 54LS | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| VOL | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\ & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | 54LS |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $V_{C C}=M a x, V_{1}=10 \mathrm{~V}$ |  |  |  | 0.1 | mA |
|  | PE Input | $V_{C C}=M a x, V_{1}=10 \mathrm{~V}$ |  |  |  | 200 | $\mu \mathrm{A}$ |
| ${ }_{1 / \mathrm{H}}$ | High Level Input Current | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
|  | PE Input | $V_{C C}=M a x, V_{1}=2.7 V$ |  |  |  | 40 | $\mu \mathrm{A}$ |
| IIL | Low Level Input Current | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.4 | mA |
|  | PE Input | $\mathrm{V}_{C C}=\operatorname{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.8 | mA |
| los | Short Circuit Output Current | $V_{C C}=M a x$ <br> (Note 2) | 54LS | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | $-100$ |  |
| ICC | Supply Current | $\mathrm{V}_{\mathrm{CC}}=$ Max |  |  |  | 21 | mA |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Switching Characteristics
$\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $\begin{aligned} & R_{L}=2 \mathrm{k} \Omega \\ & \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\ & \hline \end{aligned}$ |  | Units |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output |  | 27 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output |  | 27 | ns |
| $f_{\text {max }}$ | Maximum Shift Frequency | 30 |  | MHz |

## Functional Description

The '95 is a 4-bit shift register with serial and parallel synchronous operating modes. It has a Serial ( $\mathrm{D}_{\mathrm{S}}$ ) and four Parallel (P0-P3) Data inputs and four Parallel Data outputs (Q0-Q3). The serial or parallel mode of operation is controlled by a Parallel Enable input (PE) and two Clock inputs, $\overline{\mathrm{CP}} 1$ and CP 2 . The serial (right-shift) or parallel data transfers occur synchronous with the HIGH-to-LOW transition of the selected clock input.
When PE is HIGH, $\overline{\mathrm{CP}} 2$ is enabled. A HIGH-to-LOW transition on enabled $\overline{\mathrm{CP}} 2$ transfers parallel data from the P0P3 inputs to the Q0-Q3 outputs. When PE is LOW, $\overline{\mathrm{CP}} 1$ is
enabled. A HIGH-to-LOW transition on enabled CP1 transfers the data from Serial input ( $\mathrm{D}_{\mathrm{S}}$ ) to Q0 and shifts the data in Q0 to Q1, Q1 to Q2, and Q2 to Q3 respectively (rightshift). A left-shift is accomplished by externally connecting Q3 to P2, Q2 to P1, and Q1 to P0, and operating the ' 95 in the parallel mode ( $\mathrm{PE}=\mathrm{HIGH}$ ). For normal operation, PE should only change states when both Clock inputs are LOW. However, changing PE from LOW to HIGH while CP2 is HIGH, or changing PE from HIGH to LOW while $\overline{\mathrm{CP}} 1$ is HIGH and $\overline{\mathrm{CP}} 2$ is LOW will not cause any changes on the register outputs.

I = LOW Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.
$h=$ HIGH Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.
$\mathrm{pn}=$ Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.
H = HIGH Voltage Level
L = LOW Voltage Level
$X=$ Immaterial


TL/F/10175-3
FIGURE A

## Logic Diagram



## DM54LS107A/DM74LS107A Dual Negative-EdgeTriggered Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

## General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The $J$ and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. The data on the J
and K inputs may change while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the clear input will reset the outputs regardless of the logic levels of the other inputs.

## Connection Diagram

Dual-In-Line Package


Order Number DM54LS107AJ, DM54LS107AW, DM74LS107AM or DM74LS107AN See NS Package Number J14A, M14A, N14A or W14B

Function Table

| Inputs |  |  |  | Outputs |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CLR | CLK | J | K | Q | $\overline{\mathbf{Q}}$ |
| L | X | X | X | L | H |
| H | $\downarrow$ | L | L | $Q_{0}$ | $\bar{Q}_{0}$ |
| $H$ | $\downarrow$ | $H$ | $L$ | $H$ | L |
| $H$ | $\downarrow$ | L | $H$ | L | $H$ |
| $H$ | $\downarrow$ | $H$ | $H$ | Toggle |  |
| H | $H$ | X | X | Q $_{0}$ | $\bar{Q}_{0}$ |

[^13]| Absolute Maximum Ratings (Note) |  |
| :--- | ---: |
| If Milltary/Aerospace specified devices are required, |  |
| please contact the National Semiconductor Sales |  |
| Office/Distributors for availability and specifications. |  |
| Supply Voltage | 7 V |
| Input Voltage | 7 V |
| Operating Free Air Temperature Range | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| DM54LS | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| DM 74 S | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter |  | DM54LS107A |  |  | DM74LS107A |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage |  | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  |  | 0.7 |  |  | 0.8 | V |
| $\mathrm{IOH}^{\text {l }}$ | High Level Output Current |  |  |  | -0.4 |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  |  | 4 |  |  | 8 | mA |
| fCLK | Clock Frequency (Note 2) |  | 0 |  | 30 | 0 |  | 30 | MHz |
| fCLK | Clock Frequency (Note 3) |  | 0 |  | 25 | 0 |  | 25 | MHz |
| tw | Pulse Width (Note 2) | Clock High | 20 |  |  | 20 |  |  | ns |
|  |  | Clear Low | 25 |  |  | 25 |  |  |  |
| tw | Pulse Width (Note 3) | Clock High | 25 |  |  | 25 |  |  | ns |
|  |  | Clear Low | 30 |  |  | 30 |  |  |  |
| tsu | Setup Time (Notes 1 \& 2) |  | 20 $\downarrow$ |  |  | 20 $\downarrow$ |  |  | ns |
| tsu | Setup Time (Notes 1 \& 3) |  | 25 $\downarrow$ |  |  | 25 $\downarrow$ |  |  | ns |
| $t_{H}$ | Hold Time (Notes 1 \& 2) |  | 0】 |  |  | 0 $\downarrow$ |  |  | ns |
| $\mathrm{t}_{\mathrm{H}}$ | Hold Time (Notes 1 \& 3) |  | 5 $\downarrow$ |  |  | 5 $\downarrow$ |  |  | ns |
| TA | Free Air Operating Temperature |  | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Note 1: The symbol $(\downarrow)$ indicates the falling edge of the clock pulse is used for reference.
Note 2: $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$.
Note 3: $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | $\begin{gathered} \text { Typ } \\ \text { (Note 1) } \end{gathered}$ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| VOH | High Level Output Voltage | $\begin{aligned} & V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\ & V_{I L}=\operatorname{Max}, V_{I H}=\operatorname{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}$ | J, K |  |  | 0.1 | mA |
|  |  |  | Clear |  |  | 0.3 |  |
|  |  |  | Clock |  |  | 0.4 |  |

Electrical Characteristics
over recommended operating free air temperature range (unless otherwise noted) (Continued)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }_{1 / H}$ | High Level Input Current | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\ & \mathrm{~V}_{1}=2.7 \mathrm{~V} \end{aligned}$ | J, K |  |  | 20 | $\mu \mathrm{A}$ |
|  |  |  | Clear |  |  | 60 |  |
|  |  |  | Clock |  |  | 80 |  |
| ILL | Low Level Input Current | $\begin{aligned} & V_{C C}=M a x \\ & V_{1}=0.4 V \end{aligned}$ | J, K |  |  | -0.4 | mA |
|  |  |  | Clear |  |  | -0.8 |  |
|  |  |  | Clock |  |  | -0.8 |  |
| los | Short Circuit Output Current | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\ & \text { (Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICC | Supply Current | $\mathrm{V}_{\text {CC }}=\mathrm{Max}$ (Note 3) |  |  | 4 | 6 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From (Input) To (Output) | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $C_{L}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}$ |  |  |
|  |  |  | Min | Max | Min | Max |  |
| $\mathrm{f}_{\text {MAX }}$ | Maximum Clock Frequency |  | 30 |  | 25 |  | MHz |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | Preset to Q |  | 20 |  | 24 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | Preset to $\bar{Q}$ |  | 20 |  | 28 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $\begin{aligned} & \text { Clear } \\ & \text { to } \overline{\mathrm{Q}} \end{aligned}$ |  | 20 |  | 24 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | $\begin{aligned} & \text { Clear } \\ & \text { to } \mathrm{Q} \\ & \hline \end{aligned}$ |  | 20 |  | 28 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | Clock to Q or $\bar{Q}$ |  | 20 |  | 24 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | Clock to Q or $\bar{Q}$ |  | 20 |  | 28 | ns |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where $\mathrm{V}_{\mathrm{O}}=2.25 \mathrm{~V}$ and 2.125 V for DM 54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.
Note 3: With all inputs open, $I_{C C}$ is measured with the $Q$ and $\bar{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

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## 54LS109/DM54LS109A/DM74LS109A Dual Positive-Edge-Triggered J-K Flip-Flops with Preset, Clear, and Complementary Outputs

## General Description

This device contains two independent positive-edge-triggered J-K flip-flops with complementary outputs. The J and $\overline{\mathrm{K}}$ data is accepted by the flip-flop on the rising edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the $J$ and $\bar{K}$ inputs may be changed while the clock is high or low as long as setup and hold times are not violated. A low logic level on the preset or
clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

## Features

- Alternate Military/Aerospace device (54LS109) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications


## Connection Diagram

## Dual-In-Line Package



TL/F/6368-1
Order Number 54LS109DMQB, 54LS109FMQB, DM54LS109AJ, DM54LS109AW, DM74LS109AM or DM74LS109AN See NS Package Number J16A, M16A, N16E or W16A

## Function Table

| Inputs |  |  |  |  |  | Outputs |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PR | CLR | CLK | J | $\bar{K}$ | $\mathbf{Q}$ | $\overline{\mathbf{Q}}$ |  |
| L | $H$ | $X$ | $X$ | $X$ | $H$ | L |  |
| $H$ | $L$ | $X$ | $X$ | $X$ | $L$ | $H$ |  |
| $L$ | $L$ | $X$ | $X$ | $X$ | $H^{*}$ | $H^{*}$ |  |
| $H$ | $H$ | $\uparrow$ | $L$ | $L$ | $L$ | $H$ |  |
| $H$ | $H$ | $\uparrow$ | $H$ | $L$ | Toggle |  |  |
| $H$ | $H$ | $\uparrow$ | $L$ | $H$ | $Q_{0}$ | $\bar{Q}_{0}$ |  |
| $H$ | $H$ | $\uparrow$ | $H$ | $H$ | $H$ | $L$ |  |
| $H$ | $H$ | $L$ | $X$ | $X$ | $Q_{0}$ | $\bar{Q}_{0}$ |  |

$H=$ High Logic Level
L = Low Logic Level
$X=$ Either Low or High Logic Level
$\uparrow=$ Rising Edge of Pulse

* = This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) state.
$Q_{0}=$ The output logic level of $Q$ before the indicated input conditions were established.

Toggle $=$ Each output changes to the complement of its previous level on each active transition of the clock pulse.

| Absolute Maximum Ratings (Note) |  |
| :---: | :---: |
| If Military/Aerospace specified devic please contact the National Semi Office/Distributors for availability and | es are required, conductor Sales specifications. |
| Supply Voltage | V |
| Input Voltage | 7V |
| Operating Free Air Temperature Range |  |
| DM54LS and 54LS | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| DM74LS | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter |  | DM54LS109A |  |  | DM74LS109A |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Nom | Max | Min | Nom | Max |  |
| $V_{C C}$ | Supply Voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage |  | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  |  | 0.7 |  |  | 0.8 | V |
| IOH | High Level Output Current |  |  |  | -0.4 |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  |  | 4 |  |  | 8 | mA |
| fCLK | Clock Frequency (Note 2) |  | 0 |  | 25 | 0 |  | 25 | MHz |
| $\mathrm{f}_{\mathrm{CLK}}$ | Clock Frequency (Note 3) |  | 0 |  | 20 | 0 |  | 20 | MHz |
| tw | Pulse Width (Note 2) | Clock High | 18 |  |  | 18 |  |  | ns |
|  |  | Preset Low | 15 |  |  | 15 |  |  |  |
|  |  | Clear Low | 15 |  |  | 15 |  |  |  |
| tw | Pulse Width (Note 3) | Clock High | 25 |  |  | 25 |  |  | ns |
|  |  | Preset Low | 20 |  |  | 20 |  |  |  |
|  |  | Clear Low | 20 |  |  | 20 |  |  |  |
| tsu | Setup Time (Notes 1 \& 2) | Data High | $30 \uparrow$ |  |  | $30 \uparrow$ |  |  | ns |
|  |  | Data Low | $20 \uparrow$ |  |  | $20 \uparrow$ |  |  |  |
| tsu | Setup Time <br> (Notes 1 \& 3) | Data High | $35 \uparrow$ |  |  | $35 \uparrow$ |  |  | ns |
|  |  | Data Low | $25 \uparrow$ |  |  | $25 \uparrow$ |  |  |  |
| ${ }_{\text {t }}^{\text {H }}$ | Hold Time (Note 4) |  | $0 \uparrow$ |  |  | $0 \uparrow$ |  |  | ns |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature |  | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Note 1: The symbol ( $\uparrow$ ) indicates the rising edge of the clock pulse is used for reference.
Note 2: $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$.
Note 3: $C_{L}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, T_{A}=25^{\circ} \mathrm{C}$ and $V_{C C}=5 \mathrm{~V}$.
Note 4: $T_{A}=25^{\circ} \mathrm{C}$ and $V_{C C}=5 \mathrm{~V}$.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ <br> (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOH}_{\mathrm{H}}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & V_{C C}=M i n, I_{O L}=M a x \\ & V_{I L}=M a x, V_{I H}=\operatorname{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\begin{aligned} & V_{\mathrm{CC}}=\mathrm{Max} \\ & V_{1}=7 \mathrm{~V} \end{aligned}$ | J, $\bar{K}$ |  |  | 0.1 | mA |
|  |  |  | Clock |  |  | 0.1 |  |
|  |  |  | Preset |  |  | 0.2 |  |
|  |  |  | Clear |  |  | 0.2 |  |
| $\mathrm{IIH}^{\text {H}}$ | High Level Input Current | $\begin{aligned} & V_{\mathrm{CC}}=\mathrm{Max} \\ & \mathrm{~V}_{1}=2.7 \mathrm{~V} \end{aligned}$ | J, $\bar{K}$ |  |  | 20 | $\mu \mathrm{A}$ |
|  |  |  | Clock |  |  | 20 |  |
|  |  |  | Preset |  |  | 40 |  |
|  |  |  | Clear |  |  | 40 |  |
| IIL | Low Level Input Current | $\begin{aligned} & V_{\mathrm{CC}}=\mathrm{Max} \\ & V_{1}=0.4 \mathrm{~V} \end{aligned}$ | J, $\overline{\mathrm{K}}$ |  |  | -0.4 | mA |
|  |  |  | Clock |  |  | -0.4 |  |
|  |  |  | Preset |  |  | -0.8 |  |
|  |  |  | Clear |  |  | -0.8 |  |
| los | Short Circuit Output Current | $\begin{aligned} & V_{\mathrm{CC}}=\mathrm{Max} \\ & \text { (Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICC | Supply Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ (Note 3) |  |  | 4 | 8 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From (Input) To (Output) | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  |  | Min | Max | Min | Max |  |
| $\mathrm{f}_{\text {MAX }}$ | Maximum Clock Frequency |  | 25 |  | 20 |  | MHz |
| tplH | Propagation Delay Time Low to High Level Output | Clock to Q or $\bar{Q}$ |  | 25 |  | 35 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | Clock to Q or $\bar{Q}$ |  | 30 |  | 35 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $\begin{aligned} & \text { Clear } \\ & \text { to } \overline{\mathrm{Q}} \end{aligned}$ |  | 25 |  | 35 | ns |
| tPHL | Propagation Delay Time High to Low Level Output | $\begin{aligned} & \hline \text { Clear } \\ & \text { to } \mathrm{Q} \\ & \hline \end{aligned}$ |  | 30 |  | 35 | ns |
| tpLH | Propagation Delay Time Low to High Level Output | Preset to Q |  | 25 |  | 35 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | Preset to Q |  | 30 |  | 35 | ns |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where $\mathrm{V}_{\mathrm{O}}=2.25 \mathrm{~V}$ and 2.125 V for DM 54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.
Note 3: $I_{C C}$ is measured with all outputs open, with CLOCK grounded after setting the $Q$ and $\bar{Q}$ outputs high in turn.

## 54LS112/DM54LS112A/DM74LS112A <br> Dual Negative-Edge-Triggered Master-Slave <br> J-K Flip-Flops with Preset, Clear, and Complementary Outputs

## General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flop on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the falling edge of the clock pulse. Data on the J and K inputs may be changed while the clock is high or low without affecting the outputs as long as the setup and hold times are not
violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

## Features

■ Alternate Military/Aerospace device (54LS112) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

## Connection Diagram



Order Number 54LS112DMQB, 54LS112FMQB,
54LS112LMQB, DM54LS112AJ, DM54LS112AW, DM74LS112AM or DM74LS112AN See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

| Inputs |  |  |  |  | Outputs |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PR | CLR | CLK | J | K | Q | $\overline{\mathbf{Q}}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | $\mathrm{H}^{*}$ | $\mathrm{H}^{*}$ |
| H | H | $\downarrow$ | L | L | $Q_{0}$ | $\bar{Q}_{0}$ |
| H | H | $\downarrow$ | H | L | H | L |
| H | H | $\downarrow$ | L | H | L | H |
| H | H | $\downarrow$ | H | H |  |  |
| H | H | H | X | X | $Q_{0}$ | $\bar{Q}_{0}$ |

$H=$ High Logic Level
L = Low Logic Level
$X=$ Either Low or High Logic Level
$\downarrow=$ Negative Going Edge of Pulse

* = This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) level.
$Q_{0}=$ The output logic level before the indicated input conditions were established.
Toggle $=$ Each output changes to the complement of its previous level on each falling edge of the clock pulse.


## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
Operating Free Air Temperature Range

DM54LS and 54LS
$-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
$0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$
Storage Temperature Range

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter |  | DM54LS112A |  |  | DM74LS112A |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage |  | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  |  | 0.7 |  |  | 0.8 | V |
| IOH | High Level Output Current |  |  |  | -0.4 |  |  | -0.4 | mA |
| lOL | Low Level Output Current |  |  |  | 4 |  |  | 8 | mA |
| $\mathrm{f}_{\mathrm{CLK}}$ | Clock Frequency (Note 2) |  | 0 |  | 30 | 0 |  | 30 | MHz |
| $\mathrm{f}_{\mathrm{CLK}}$ | Clock Frequency (Note 3) |  | 0 |  | 25 | 0 |  | 25 | MHz |
| tw | Pulse Width (Note 2) | Clock High | 20 |  |  | 20 |  |  | ns |
|  |  | Preset Low | 25 |  |  | 25 |  |  |  |
|  |  | Clear Low | 25 |  |  | 25 |  |  |  |
| tw | Pulse Width (Note 3) | Clock High | 25 |  |  | 25 |  |  | ns |
|  |  | Preset Low | 30 |  |  | 30 |  |  |  |
|  |  | Clear Low | 30 |  |  | 30 |  |  |  |
| tsu | Setup Time (Notes 1 and 2) |  | $20 \downarrow$ |  |  | $20 \downarrow$ |  |  | ns |
| tsu | Setup Time (Notes 1 and 3) |  | 25 $\downarrow$ |  |  | 25 $\downarrow$ |  |  | ns |
| $\mathrm{t}_{\mathrm{H}}$ | Hold Time (Notes 1 and 2) |  | 0 $\downarrow$ |  |  | $0 \downarrow$ |  |  | ns |
| $t_{H}$ | Hold Time (Notes 1 and 3) |  | 5 $\downarrow$ |  |  | $5 \downarrow$ |  |  | ns |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature |  | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Note 1: The symbol $(\downarrow)$ indicates the falling edge of the clock pulse is used for reference.
Note 2: $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, T_{A}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$.
Note 3: $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | $\begin{gathered} \text { Typ } \\ \text { (Note 1) } \end{gathered}$ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & V_{C C}=M i n, I_{O H}=\operatorname{Max} \\ & V_{\mathrm{IL}}=\operatorname{Max}, V_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| VOL | Low Level Output Voltage | $\begin{aligned} & V_{C C}=M i n, I_{O L}=\operatorname{Max} \\ & V_{I L}=M a x, V_{I H}=\operatorname{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}$ | J, K |  |  | 0.1 | mA |
|  |  |  | Clear |  |  | 0.3 |  |
|  |  |  | Preset |  |  | 0.3 |  |
|  |  |  | Clock |  |  | 0.4 |  |

Electrical Characteristics
over recommended operating free air temperature range (unless otherwise noted) (Continued)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }_{1 / H}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ | J, K |  |  | 20 | $\mu \mathrm{A}$ |
|  |  |  | Clear |  |  | 60 |  |
|  |  |  | Preset |  |  | 60 |  |
|  |  |  | Clock |  |  | 80 |  |
| IIL | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}$ | J, K |  |  | -0.4 | mA |
|  |  |  | Clear |  |  | -0.8 |  |
|  |  |  | Preset |  |  | -0.8 |  |
|  |  |  | Clock |  |  | -0.8 |  |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & (\text { Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICC | Supply Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ (Note 3) |  |  | 4 | 6 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From (Input) To (Output) | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}$ |  |  |
|  |  |  | Min | Max | Min | Max |  |
| $\mathrm{f}_{\text {MAX }}$ | Maximum Clock Frequency |  | 30 |  | 25 |  | MHz |
| ${ }_{\text {tplH }}$ | Propagation Delay Time Low to High Level Output | Preset to Q |  | 20 |  | 24 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | $\begin{aligned} & \text { Preset } \\ & \text { to } \bar{Q} \end{aligned}$ |  | 20 |  | 28 | ns |
| ${ }_{\text {tPLH }}$ | Propagation Delay Time Low to High Level Output | $\begin{aligned} & \text { Clear } \\ & \text { to } \bar{Q} \end{aligned}$ |  | 20 |  | 24 | ns |
| ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | Clear $\text { to } Q$ |  | 20 |  | 28 | ns |
| ${ }_{\text {tPLH }}$ | Propagation Delay Time Low to High Level Output | Clock to $Q$ or $\bar{Q}$ |  | 20 |  | 24 | ns |
| ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | Clock to Q or $\bar{Q}$ |  | 20 |  | 28 | ns |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where $\mathrm{V}_{\mathrm{O}}=2.25 \mathrm{~V}$ and 2.125 V for DM 54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.
Note 3: With all outputs open, ICC is measured with the $Q$ and $\bar{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

## 54LS113

## Dual JK Edge-Triggered Flip-Flop

## General Description

The 54LS113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is HIGH and the bistable will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

## Connection Diagram



TL/F/10205-1
Order Number 54LS113DMQB, 54LS113FMQB or 54LS113LMQB
See NS Package Number E20A, J14A or W14B

## Logic Symbol



TL/F/10205-2
$V_{\mathrm{CC}}=\operatorname{Pin} 14$
$\mathrm{GND}=\operatorname{Pin} 7$

## Truth Table

| Inputs |  | Output |
| :---: | :---: | :---: |
| $@ t_{n}$ |  | $@ t_{n}+1$ |
| $J$ | $K$ | $Q$ |
| $L$ | $L$ | $Q_{n}$ |
| $L$ | $H$ | $L$ |
| $H$ | $L$ | $H$ |
| $H$ | $H$ | $\bar{Q}_{n}$ |

$\mathrm{t}_{\mathrm{n}}=$ Bit Time before Clock Pulse
$t_{\mathrm{n}}+1=$ Bit Time after Clock Pulse
H = HIGH Voltage Level
L = LOW Voltage Level
Asynchronous Input:
Low input to $\bar{S}_{D}$ sets $Q$ to HIGH level
Set is independent of clock

| Pin Names | Description |
| :--- | :--- |
| $\mathrm{J} 1, \mathrm{~J} 2, \mathrm{~K} 1, \mathrm{~K} 2$ | Data Inputs |
| $\overline{\mathrm{CP}} 1, \overline{\mathrm{CP}} 2$ | Clock Pulse Inputs (Active Falling Edge) |
| $\overline{\mathrm{SD} 1, \overline{\mathrm{~S}} 2} 2$ | Direct Set Inputs (Active LOW) |
| Q1, Q2, $\overline{\mathrm{Q} 1, \overline{\mathrm{Q} 2}}$ | Outputs |



| Supply Voltage | 7 V |
| :---: | :---: |
| Input Voltage | 5.5 V |
| Operating Free Air Temperature Range |  |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

## Recommended Operating Conditions

| Symbol | Parameter | 54LS113 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max |  |
| $V_{C C}$ | Supply Voltage | 4.5 | 5 | 5.5 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 | V |
| $\mathrm{IOH}^{2}$ | High Level Output Current |  |  | -0.4 | mA |
| $\mathrm{IOL}^{\text {l }}$ | Low Level Output Current |  |  | 4 | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | ${ }^{\circ} \mathrm{C}$ |
| $\begin{aligned} & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\ & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\ & \hline \end{aligned}$ | Setup Time $J_{n} \text { or } K_{n} \text { to } \overline{C P}_{n}$ | $\begin{aligned} & 20 \\ & 20 \end{aligned}$ |  |  | ns |
| $\begin{aligned} & t_{\mathrm{t}}(H) \\ & \mathrm{t}_{\mathrm{h}}(\mathrm{~L}) \end{aligned}$ | Hold Time $J_{n} \text { or } K_{n} \text { to } \overline{C P}_{n}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ |  |  | ns |
| $\begin{aligned} & t_{w}(H) \\ & t_{w}(L) \\ & \hline \end{aligned}$ | $\overline{C P}_{n}$ Pulse Width | $\begin{aligned} & 20 \\ & 15 \\ & \hline \end{aligned}$ |  |  | ns |
| $\mathrm{t}_{\mathrm{w}}(\mathrm{L})$ | $\bar{S}_{\text {Dn }}$ Pulse Width LOW | 15 |  |  | ns |

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ <br> (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $V_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\ & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ |  | 2.5 |  |  | V |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & V_{C C}=M i n, I_{O L}=\operatorname{Max}, \\ & V_{I H}=\operatorname{Min}, V_{I L}=M a x \end{aligned}$ |  |  |  | 0.4 | V |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}$ | J, K |  |  | 0.1 | mA |
|  |  |  | SD |  |  | 0.3 |  |
|  |  |  | CP |  |  | 0.4 |  |
| $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ | J, K |  |  | 20 | $\mu \mathrm{A}$ |
|  |  |  | SD |  |  | 60 |  |
|  |  |  | CP |  |  | 80 |  |
| IIL | Low Level Input Current | $V_{C C}=M a x, V_{1}=0.5 \mathrm{~V}$ | J, K | -30 |  | -400 | $\mu \mathrm{A}$ |
|  |  |  | CP, SD | -60 |  | -800 |  |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & \text { (Note 2) } \end{aligned}$ |  | -20 |  | -100 | mA |
| $\mathrm{I}_{\mathrm{CC}}$ | Supply Current | $\mathrm{V}_{C C}=\operatorname{Max}$ (Note 3) |  |  |  | 8 | mA |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: $l_{C C}$ is measured with all outputs open and all inputs grounded.

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual operation.

Switching Characteristics $\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (See Section 1 for test waveforms and output load)

| Symbol | Parameter | 54LS113 |  | Units |
| :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  |  |
|  |  | Min | Max |  |
| $f_{\text {max }}$ | Maximum Clock Frequency | 30 |  | MHz |
| $t_{\text {PLH }}$ $t_{\mathrm{PHL}}$ | Propagation Delay $\overline{C P}_{n}$ to $Q_{n}$ or $\bar{Q}_{n}$ |  | $\begin{array}{r} 16 \\ 24 \\ \hline \end{array}$ | ns |
| $t_{\text {PLH }}$ $\mathrm{t}_{\mathrm{PHL}}$ | Propagation Delay $\bar{S}_{D n}$ to $Q_{n}$ or $\bar{Q}_{n}$ |  | $\begin{array}{r} 16 \\ 24 \\ \hline \end{array}$ | ns |

Logic Diagram (one half shown)


## 54LS114

## Dual JK Negative Edge-Triggered Flip-Flop with Common Clocks and Clears

## General Description

The 'LS114 features individual J, K and set inputs and common clock and common clear inputs. When the clock goes HIGH the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change
when the Clock Pulse is HIGH and the bistable will perform according to the truth table as long as the minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

## Connection Diagram

Dual-In-Line Package


TL/F/10176-1

## Logic Symbol



TL/F/10176-2
$V_{C C}=\operatorname{Pin} 14$
GND $=\operatorname{Pin} 7$

| Pin Names | Description |
| :--- | :--- |
| $\mathrm{J} 1, \mathrm{~J} 2, \mathrm{~K} 1, \mathrm{~K} 2$ | Data Inputs |
| $\overline{\mathrm{CP}}$ | Clock Pulse Input (Active Falling Edge) |
| $\overline{\mathrm{C} D}$ | Direct Clear Input (Active LOW) |
| $\overline{\mathrm{S} D 1, \bar{S} D 2}$ | Direct Set Inputs (Active LOW) |
| $\mathrm{Q} 1, \mathrm{Q} 2, \overline{\mathrm{Q}} 1, \overline{\mathrm{Q} 2}$ | Outputs |

[^14]\textrm{C}\mathrm{ to }+7\mp@subsup{0}{}{\circ}\textrm{C
-65}\mp@subsup{}{}{\circ}\textrm{C}\mathrm{ to }+15\mp@subsup{0}{}{\circ}\textrm{C

```

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multirow{2}{|c|}{ Parameter } & \multicolumn{2}{|c|}{ DM93S47 } & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Current & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Current & & & 0.8 & V \\
\hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -1 & mA \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 20 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) }
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\) & & & \(-1.2\) & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & 2.7 & 3.4 & & V \\
\hline VOL & Low Level Output Voltage & \[
\begin{aligned}
& V_{C C}=\text { Min, } I_{O H}=\text { Max, } \\
& V_{I H}=\operatorname{Min}
\end{aligned}
\] & & 0.35 & 0.5 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \({ }_{1 / \mathrm{H}}\) & High Level Input Current & \(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\) & & & 50 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \(V_{C C}=\operatorname{Max}, V_{1}=0.5 \mathrm{~V}\) & & & -2.0 & mA \\
\hline los & Short Circuit Output Current & \(V_{C C}=\operatorname{Max}\) (Note 2) & -40 & & -100 & mA \\
\hline ICC & Supply Current & \(\mathrm{V}_{C C}=\) Max & & & 65 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for Waveforms and Load Configurations)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Conditions} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \begin{tabular}{l}
\(t_{\text {PLH }}\) \\
\(t_{\text {PHL }}\)
\end{tabular} & Propagation Delay
\[
A_{n} \text { or } B_{n} \text { to } A=B
\] & \(\overline{\mathrm{E}}=\mathrm{GND}\), Other Inputs \(=4.5 \mathrm{~V}\), Test Each Input Individually & \[
\begin{aligned}
& 5.0 \\
& 5.0
\end{aligned}
\] & \[
\begin{aligned}
& 17 \\
& 17
\end{aligned}
\] & ns \\
\hline \begin{tabular}{l}
\(t_{\text {PLH }}\) \\
\(t_{\text {PHL }}\)
\end{tabular} & Propagation Delay
\[
A_{n} \text { or } B_{n} \text { to } A=B
\] & \(\overline{\mathrm{E}}=\mathrm{GND}\), Other Inputs \(=\) GND, Test Each Input Individually & \[
\begin{aligned}
& 4.0 \\
& 4.0 \\
& \hline
\end{aligned}
\] & \[
\begin{aligned}
& 14 \\
& 15 \\
& \hline
\end{aligned}
\] & ns \\
\hline \begin{tabular}{l}
\(t_{\text {PLH }}\) \\
\(t_{\text {PHL }}\)
\end{tabular} & Propagation Delay \(\bar{E}\) to \(A=B\) & \(A_{n} \neq B_{n}\) & \[
\begin{aligned}
& 3.0 \\
& 3.0
\end{aligned}
\] & \[
\begin{aligned}
& 10 \\
& 10
\end{aligned}
\] & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The DM93S47 is a very high speed 6-bit identity comparator. When enabled ( \(\bar{E}\) input LOW), the \(A=B\) output is HIGH if the two 6 -bit words are equal. When disabled ( \(\bar{E}\) input HIGH), the \(A=B\) output is forced HIGH. Equality is determined by Exclusive-NOR circuits which individually compare the equivalent bits from each word. Since the \(A=B\) output state is determined by the equality of each pair of inputs, the equivalent \(A_{n}\) and \(B_{n}\) pins can be interchanged to facilitate board layout or wiring. The active LOW Enable ( \(\overline{\mathrm{E}}\) ) can be used as a high speed strobe. When the Enable is HIGH, the \(A=B\) output is forced HIGH. This allows devices tied to a common wired-OR (actually wired-AND) node to be strobed individually or in groups. Only the enabled devices will determine the state of the output node.
\[
\begin{aligned}
(A=B)= & \bar{E}+(\overline{\mathrm{A} 0 \oplus \mathrm{~B} 0}) \bullet(\overline{\mathrm{A} 1 \oplus \mathrm{~B} 1}) \bullet(\overline{\mathrm{A} 2 \oplus \mathrm{~B} 2}) \bullet \\
& (\overline{\mathrm{A} 3 \oplus(\mathrm{~B} 3}) \cdot(\overline{\mathrm{A} 4 \oplus \mathrm{~B} 4}) \bullet(\overline{\mathrm{A} 5 \oplus \mathrm{~B} 5})
\end{aligned}
\]

\section*{Logic Diagram}


\section*{DM93S62}

\section*{9-Input Parity Checker/Generator}

\section*{General Description}

The DM93S62 is a very high speed 9-Input parity checker/ generator for use in error detection and error correction applications. The DM93S62 provides odd and even parity for up to nine data bits. The even parity output (PE) is HIGH if
an even number of inputs are HIGH and \(\bar{E}\) is LOW. The odd parity output (PO) will be HIGH if an odd number of inputs are HIGH and \(\bar{E}\) is LOW. A HIGH level on the Enable ( \(\bar{E}\) ) input forces both outputs LOW.

\section*{Connection Diagram}


Order Number DM93S62N NS Package Number N14A

\section*{Logic Symbol}

\begin{tabular}{|l|l|}
\hline Pin Name & \multicolumn{1}{c|}{ Description } \\
\hline \(10-18\) & Data Inputs \\
\(\bar{E}\) & Output Enable (Active Low) \\
PO & Odd Parity Output \\
PE & Even Parity Output \\
\hline
\end{tabular}

\section*{Truth Table ( \(\bar{E}=\) Low)}
\begin{tabular}{|c|c|c|}
\hline \multirow{2}{*}{\begin{tabular}{c} 
Number of Inputs \\
I0-18 that are HIGH
\end{tabular}} & \multicolumn{2}{|c|}{ Outputs } \\
\cline { 2 - 3 } & PO & PE \\
\hline \(1,3,5,7,9\) & \(H\) & L \\
\(0,2,4,6,8\) & L & H \\
\hline
\end{tabular}

\footnotetext{
\(H=H I G H\) Voltage Level
L = LOW Voltage Level
}

\section*{Absolute Maximum Ratings (Note)}

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
\begin{tabular}{lr} 
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \\
DM93S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multirow{2}{|c|}{ Parameter } & \multicolumn{3}{|c|}{ DM93S62 } & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -1 & mA \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 20 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ
(Note 1) & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}^{\prime}=-18 \mathrm{~mA}\) & & & -1.2 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & 2.7 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\] & & 0.35 & 0.5 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{C C}=\operatorname{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\) & & & 50 & \(\mu \mathrm{A}\) \\
\hline \multirow[t]{2}{*}{ILL} & \multirow[t]{2}{*}{Low Level Input Current} & \(V_{C C}=M a x, V_{1}=0.5 \mathrm{~V}, 10-18\) & & & -1.6 & \multirow[t]{2}{*}{mA} \\
\hline & & \(V_{C C}=\) Max, \(V_{1}=0.5 \mathrm{~V}\), E Only & & & -3.2 & \\
\hline los & Short Circuit Output Current & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\text { Max } \\
& \text { (Note 2) } \\
& \hline
\end{aligned}
\] & -40 & & -100 & mA \\
\hline ICC & Supply Current & \(V_{C C}=\) Max & & & 65 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

\section*{Switching Characteristics}
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\(C_{L}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay 10-17 to PE & & \[
\begin{aligned}
& 26 \\
& 22 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
t_{\text {PLH }}
\]
\[
t_{\mathrm{PHL}}
\] & Propagation Delay 18 to PE & & \[
\begin{aligned}
& 12 \\
& 9.0
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay 10-17 to PO & & \[
\begin{array}{r}
26 \\
26 \\
\hline
\end{array}
\] & ns \\
\hline tpLH
\[
\mathrm{t}_{\mathrm{PHL}}
\] & Propagation Delay 18 to PO & & \[
\begin{aligned}
& 13 \\
& 13 \\
& \hline
\end{aligned}
\] & ns \\
\hline \begin{tabular}{l}
tpLH \\
tpHL
\end{tabular} & Propagation Delay \(\bar{E}\) to PE & & \[
\begin{aligned}
& 7.0 \\
& 7.0
\end{aligned}
\] & ns \\
\hline \begin{tabular}{l}
\(t_{\text {PLH }}\) \\
tpHL
\end{tabular} & Propagation Delay \(\bar{E}\) to PO & & \[
\begin{aligned}
& 7.0 \\
& 7.0 \\
& \hline
\end{aligned}
\] & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The DM93S62 is a very high speed 9-input parity checker or generator. It is intended primarily for error detection in systems which transmit data in 8 -bit bytes, but it can be expanded to any number of data inputs. Both even and odd parity outputs are available to allow maximum flexibility for both parity generation and parity checking. When the device is enabled ( \(\bar{E}=\) LOW), the Even Parity output (PE) is HIGH when an even number of inputs is HIGH, and the Odd Parity output (PO) is HIGH when an odd number of inputs is HIGH. The active LOW Enable ( \(\overline{\mathrm{E}}\) ) controls the state of both outputs; when the Enable ( \(\overline{\mathrm{E}}\) ) is HIGH, both outputs will be LOW. The Enable may be used to strobe the outputs at very high speeds to synchronize or inhibit the parity data.
The DM93S62 has been designed with two sections using Exclusive-NOR comparison techniques. Eight data inputs

10-17 represent one section which will generate a parity bit in 16 ns to 20 ns . The ninth input (18) bypasses three levels of logic and switches the outputs in 6.0 ns to 9.0 ns . This feature may be used to compensate for delayed arrival of the parity bit, allowing faster system cycle times (Figure a). The fast I8 input is also useful when more than nine bits are to be checked. The output of one DM93S62 drives the 18 input of a second DM93S62, providing a 17-bit parity check in 29 ns (typ).
When some inputs of the DM93S62 are not used, such as for words of less than nine bits or when using parallel expansion techniques, there is an optimum delay scheme for termination of the unused inputs (see Table II). In essence, if one of the inputs of any Exclusive-NOR stays HIGH, the delay from the other input to the output is minimized.

TABLE II. Termination Recommendations for Less than Nine Bits
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \begin{tabular}{c} 
Number of \\
Data Inputs
\end{tabular} & \(\mathbf{1 0}\) & \(\mathbf{1 1}\) & \(\mathbf{1 2}\) & \(\mathbf{1 3}\) & \(\mathbf{1 4}\) & \(\mathbf{1 5}\) & \(\mathbf{1 6}\) & \(\mathbf{1 7}\) & \(\mathbf{1 8}\) \\
\hline 3 & D0 & L & D 1 & L & D 2 & L & L & L & L \\
4 & D 0 & L & D 1 & L & D 2 & L & D 3 & L & L \\
5 & D 0 & L & D 1 & L & D 2 & L & D 3 & L & D 4 \\
& & & & & & & \\
7 & D 0 & D 1 & D 2 & D 3 & D 4 & L & D 5 & L & L \\
7 & D 0 & D 1 & D 2 & D 3 & D 4 & L & D 5 & L & D 6 \\
8 & D 0 & D 1 & D 2 & D 3 & D 4 & D 5 & D 6 & D 7 & L \\
\hline
\end{tabular}


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FIGURE a. Fast Input 18 allows Higher System Speed

Logic Diagram

\[
\begin{aligned}
& P O=(10 \oplus 11 \oplus 12 \oplus 13 \oplus 14 \oplus 15 \oplus 16 \oplus 17 \oplus 18) \cdot \bar{E} \\
& P E=(10 \oplus 11 \oplus I 2 \oplus 13 \oplus 14 \oplus 15 \oplus 16 \oplus 17 \oplus 18) \cdot \bar{E}
\end{aligned}
\]

TL/F/9809-4

\section*{DM96S02}

Dual Retriggerable Resettable
Monostable Multivibrator

\section*{General Description}

The DM96S02 is a dual retriggerable and resettable monostable multivibrator. This one-shot provides exceptionally wide delay range, pulse width stability, predictable accuracy and immunity to noise. The pulse width is set by an external

\section*{Connection Diagram}

Dual-In-Line Package


Order Number DM96S02N See NS Package Number N16E
resistor and capacitor. Resistor values up to \(2.0 \mathrm{M} \Omega\) for the DM96S02 reduce required capacitor values. Hysteresis is provided on the positive trigger input of the DM96S02 for increased noise immunity.

\section*{Logic Symbol}


TL/F/9810-2
(13) 3
\(V_{C C}=\operatorname{Pin} 16\)
GND \(=\operatorname{Pin} 8\)
Triggering Truth Table
\begin{tabular}{|ccc|l|}
\hline 5(11) & \begin{tabular}{c} 
Pin Number \\
4(12)
\end{tabular} & 3(13) & Operation \\
\hline\(H \rightarrow L\) & \(L\) & \(H\) & Trigger \\
\(H\) & \(L \rightarrow H\) & \(H\) & Trigger \\
\(X\) & \(X\) & \(L\) & Reset \\
\hline
\end{tabular}

\footnotetext{
\(\mathrm{H}=\mathrm{HIGH}\) Voltage Level \(\geq \mathrm{V}_{\mathrm{IH}}\)
\(\mathrm{L}=\) LOW Voltage Level \(\leq \mathrm{V}_{\mathrm{IL}}\)
\(X=\) Immaterial (either \(H\) or \(L\) )
\(H \rightarrow L=H I G H\) to LOW Voltage Level transition
\(L \rightarrow H=\) LOW to HIGH Voltage Level transition
}

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Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Nom & Max & Units \\
\hline \(V_{C C}\) & Supply Voltage & & & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & & & 2 & V & & \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & & & -1 & mA \\
\hline lOL & Low Level Output Current & & & & & 20 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & & & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline \(\mathrm{V}_{\mathrm{T}+}\) & Positive-Going Threshold Voltage, \(I_{0}, I_{1}\) & \(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}\) & & & & 2.0 & V \\
\hline \(\mathrm{V}_{\mathrm{T}}\) - & Negative-Going Threshold Voltage, \(\bar{I}_{0}, I_{1}\) & \(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}\) & & 0.8 & & & V \\
\hline \(V_{C X}\) & \begin{tabular}{l}
Capacitor Voltage \\
Pin 1 (15) Referenced \\
to Pin 2 (14)
\end{tabular} & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=4.75 \mathrm{~V} \\
& \text { to } 5.25 \mathrm{~V}
\end{aligned}
\] & \[
\begin{aligned}
& R_{X}=1.0 \mathrm{k} \Omega, \\
& R_{X} \geq 10 \mathrm{k} \Omega, \\
& R_{X}>1.0 \mathrm{~m} \Omega
\end{aligned}
\] & \[
\begin{gathered}
-0.85 \\
-0.5 \\
-0.4
\end{gathered}
\] & \[
\begin{aligned}
& 3.0 \\
& 3.0 \\
& 3.0
\end{aligned}
\] & & V \\
\hline
\end{tabular}

\section*{Electrical Characteristics}

Over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\) & & & -1.2 & V \\
\hline V OH & High Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=-1.0 \mathrm{~mA}, \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & 2.7 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\text { Max }, \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\] & & 0.35 & 0.5 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline 1 H & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\) & & & 20 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -1.0 & mA \\
\hline los & Short Circuit Output Current & \begin{tabular}{l}
\[
V_{C C}=M a x
\] \\
(Note 2)
\end{tabular} & -40 & & -100 & mA \\
\hline ICC & Supply Current & \(V_{C C}=\) Max & & & 75 & mA \\
\hline
\end{tabular}

\section*{Switching Characteristics}
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Conditions} & \multicolumn{2}{|c|}{\(C_{L}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay io to Q & \multirow[t]{9}{*}{Figure a} & & 15 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay io to \(\bar{Q}\) & & & 19 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay 11 to Q & & & 19 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay 11 to \(\bar{Q}\) & & & 20 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay \(\bar{C}_{D}\) to \(Q\) & & & 20 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay \(\overline{\mathrm{C}}_{\mathrm{D}}\) to \(\overline{\mathrm{Q}}\) & & & 14 & ns \\
\hline \(t_{w}(L)\) & İO Pulse Width LOW & & 8.0 & & ns \\
\hline \(t_{w}(H)\) & 11 Pulse Width HIGH & & 12 & & ns \\
\hline \(t_{w}(L)\) & \(\overline{\mathrm{C}}_{\mathrm{D}}\) Pulse Width LOW & & 7.0 & & ns \\
\hline \(t_{w}(\mathrm{H})\) & Minimum Q Pulse Width HIGH & \[
R_{X}=1.0 \mathrm{k} \Omega, C_{X}=10 \mathrm{pF}
\] Including Jig and Stray & 30 & 45 & ns \\
\hline \(t_{w}\) & Q Pulse Width & \(\mathrm{R}_{\mathrm{X}}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{X}}=1000 \mathrm{pF}\) & 5.2 & 5.8 & \(\mu \mathrm{s}\) \\
\hline \(\mathrm{R}_{\mathrm{X}}\) & Timing Resistor Range* & \[
\begin{aligned}
& \mathrm{T}_{\mathrm{A}}=-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\
& V_{\mathrm{CC}}=4.5 \mathrm{~V} \text { to } 5.5 \mathrm{~V}
\end{aligned}
\] & 1.0 & 2000 & k \(\boldsymbol{\Omega}\) \\
\hline \(t \Delta_{t}\) & Change in Q Pulse Width over Temperature & \(\mathrm{RXX}^{\prime}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{X}}=1000 \mathrm{pF}\) & & 1.0 & \% \\
\hline \(t \Delta v\) & Change in Q Pulse Width over VCC Range & \[
\begin{aligned}
& \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{~V}_{\mathrm{CC}}=4.75 \mathrm{~V} \text { to } \\
& 5.25 \mathrm{~V}, \mathrm{R}_{\mathrm{X}}=10 \mathrm{k} \Omega, \\
& \mathrm{C}_{\mathrm{X}}=1000 \mathrm{pF} \\
& \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{~V}_{\mathrm{CC}}=4.5 \mathrm{~V} \text { to } \\
& 5.5 \mathrm{~V}, \mathrm{RX}_{\mathrm{X}}=10 \mathrm{k} \Omega, \\
& \mathrm{C}_{\mathrm{X}}=1000 \mathrm{pF}
\end{aligned}
\] & & 1.0 & \% \\
\hline
\end{tabular}
*Applies only over commercial \(\mathrm{V}_{\mathrm{CC}}\) and \(\mathrm{T}_{A}\) range for DM96S02.
Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\)
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

\section*{Switching Waveforms}


Figure a.

\section*{Logic Diagram}


\section*{Typical Performance Characteristics}






TL/F/9810-7

\section*{Functional Description}

The 96S02 dual retriggerable resettable monostable multivibrator has two DC coupled trigger inputs per function, one active LOW (İO) and one active HIGH (11). The I1 input utilizes an internal Schmitt trigger with hysteresis of 0.3 V to provide increased noise immunity. The use of active HIGH and LOW inputs allows either rising or falling edge triggering and optional non-retriggerable operation. The inputs are DC coupled making triggering independent of input transition times. When input conditions for triggering are met the \(\mathbf{Q}\) output goes HIGH and the external capacitor is rapidly discharged and then allowed to recharge. An input trigger
which occurs during the timing cycle will retrigger the circuit and result in \(Q\) remaining HIGH. The output pulse may be terminated ( \(Q\) to the LOW state) at any time by setting the Direct Clear input LOW. Retriggering may be inhibited by tying the \(\bar{Q}\) output to \(\overline{1} 0\) or the \(Q\) output to I1. Differential sensing techniques are used to obtain excellent stability over temperature and power supply variations and a feedback Darlington capacitor discharge circuit minimizes pulse width variation from unit to unit. Schottky TTL output stages provide high switching speeds and output compatibility with all TTL logic families.

\section*{Operation Notes}

\section*{timing}
1. An external resistor ( \(\mathrm{R}_{\mathrm{X}}\) ) and an external capacitor ( \(\mathrm{C}_{\mathrm{X}}\) ) are required as shown in the Logic Diagram. The value of \(R_{X}\) may vary from \(1.0 \mathrm{k} \Omega\) to \(2.0 \mathrm{M} \Omega\) (DM96S02).
2. The value of \(C_{X}\) may vary from 0 to any necessary value available. If, however, the capacitor has significant leakage relative to \(V_{C C} / R_{X}\) the timing equations may not represent the pulse width obtained.
3. Polarized capacitors may be used directly. The (+) terminal of a polarized capacitor is connected to pin 1(15), the \((-)\) terminal to pin 2(14) and RX. Pin 1(15) will remain positive with respect to pin 2(14) during the timing cycle. However, during quiescent (non-triggered) conditions, pin 1(15) may go negative with respect to pin 2(14) depending on values of \(R_{X}\) and \(V_{C C}\). For values of \(R_{X} \geq 10 \mathrm{k} \Omega\) the maximum amount of capacitor reverse polarity, pin 1 (15) negative with respect to pin 2(14) is 500 mV . Most tantalum electrolytic capacitors are rated for safe reverse bias operation up to \(5 \%\) of their working forward voltage rating; therefore, capacitors having a rating of 10 WVdc or higher should be used with the DM96S02 when \(\mathrm{R}_{\mathrm{X}} \geq\) \(10 \mathrm{k} \Omega\).
4. The output pulse width \(t_{w}\) for \(R_{X} \geq 10 \mathrm{k} \Omega\) and \(C_{X} \geq\) 1000 pF is determined as follows:
\(t_{w}=0.55 R_{X} C_{X}\)
Where \(R_{X}\) is in \(k \Omega, C_{X}\) is in \(p F, t\) is in ns or \(R T_{X}\) is in \(k \Omega\), \(C_{X}\) is in \(\mu \mathrm{F}, \mathrm{t}\) is in ms .
5. The output pulse width for \(\mathrm{R}_{\mathrm{X}}<10 \mathrm{k} \Omega\) or \(\mathrm{C}_{\mathrm{X}}<1000 \mathrm{pF}\) should be determined from pulse width versus \(\mathrm{C}_{\mathrm{x}}\) or \(\mathrm{R}_{\mathrm{X}}\) graphs.
6. To obtain variable pulse width by remote trimming, the following circuit is recommended:

7. Under any operating condition, \(\mathrm{C}_{X}\) and \(\mathrm{R}_{X}\) (Min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
8. \(V_{C C}\) and ground wiring should conform to good high frequency standards so that switching transients on \(V_{C C}\) and ground leads do not cause interaction between one shots. Use of a \(0.01 \mu \mathrm{~F}\) to \(0.1 \mu \mathrm{~F}\) bypass capacitor between \(V_{C C}\) and ground located near the circuit is recommended.

\section*{TRIGGERING}
1. The minimum negative pulse width into \(\overline{0} 0\) is 8.0 ns ; the minimum positive pulse width into 11 is 12 ns .
2. Input signals to the DM96S02 exhibiting slow or noisy transitions should use the positive trigger input 11 which contains a Schmitt trigger. Input signals to the 96LS02 exhibiting slow or noisy transitions can use either trigger as both are Schmitt triggers.
3. When non-retriggerable operation is required, i.e., when input triggers are to be ignored during quasi-stable state, input latching is used to inhibit retriggering.
4. An overriding active LOW level direct clear is provided on each multivibrator. By applying a LOW to the clear, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW. A LOW-to-HIGH transition on \(\overline{\mathrm{C}}_{\mathrm{D}}\) will not trigger the DM96S02. If the \(\overline{\mathrm{C}}_{\mathrm{D}}\) input goes HIGH coincident with a trigger transition, the circuit will respond to the trigger.



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Section 4 TTL

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\section*{5400/DM5400/DM7400 \\ Quad 2-Input NAND Gates}

\section*{General Description}

This device contains four independent gates each of which performs the logic NAND function.

\section*{Features}
- Alternate Military/Aerospace device (5400) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Connection Diagram}

\section*{Dual-In-Line Package}


TL/F/6613-1
Order Number 5400DMQB, 5400FMQB, DM5400J, DM5400W or DM7400N See NS Package Number J14A, N14A or W14B

Function Table
\begin{tabular}{|c|c|c|}
\multicolumn{3}{c|}{\(\mathbf{Y}=\overline{\mathbf{A B}}\)} \\
\hline \multicolumn{2}{|c|}{ Inputs } & Output \\
\hline \(\mathbf{A}\) & \(\mathbf{B}\) & \(\mathbf{Y}\) \\
\hline L & L & H \\
L & H & H \\
H & L & H \\
H & \(H\) & L \\
\hline
\end{tabular}
\(H=\) High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
\begin{tabular}{lr} 
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \\
DM54 and 54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5400} & \multicolumn{3}{|c|}{DM7400} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \({ }^{\mathrm{OH}}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
\hline \(\mathrm{lOL}^{\text {l }}\) & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
(Note 1) & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline I/L & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=M a x
\] \\
(Note 2)
\end{tabular}} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 4 & 8 & mA \\
\hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & 12 & 22 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|c|c|c|c|c}
\hline Symbol & \multicolumn{1}{c|}{ Parameter } & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{l}
\(C_{\mathrm{L}}=15 \mathrm{pF}\) \\
\(\mathrm{R}_{\mathrm{L}}=400 \Omega\)
\end{tabular} & & 22 & ns \\
\cline { 1 - 2 } & & & & 15 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

National Semiconductor

\section*{DM5401/DM7401 Quad 2-Input NAND Gates with Open-Collector Outputs}

\section*{General Description}

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

\section*{Pull-Up Resistor Equations}
\(R_{\mathrm{MAX}}=\frac{\mathrm{V}_{\mathrm{CC}}(\mathrm{Min})-\mathrm{V}_{\mathrm{OH}}}{\mathrm{N}_{1}\left(\mathrm{I}_{\mathrm{OH}}\right)+\mathrm{N}_{2}\left(\mathrm{I}_{\mathrm{H}}\right)}\)
\(R_{\mathrm{MIN}}=\frac{\mathrm{V}_{\mathrm{CC}}(\mathrm{Max})-\mathrm{V}_{\mathrm{OL}}}{\mathrm{l}_{\mathrm{OL}}-\mathrm{N}_{3}\left(\mathrm{l}_{\mathrm{L}}\right)}\)
Where: \(\mathrm{N}_{1}\left(\mathrm{I}_{\mathrm{OH}}\right)=\) total maximum output high current for all outputs tied to pull-up resistor
\(\mathrm{N}_{2}\left(\mathrm{l}_{\mathrm{IH}}\right)=\) total maximum input high current for all inputs tied to pull-up resistor
\(N_{3}\left(l_{L}\right)=\) total maximum input low current for all inputs tied to pull-up resistor

\section*{Connection Diagram}

\section*{Dual-In-Line Package}


\section*{Function Table}
\[
\mathbf{Y}=\overline{\mathbf{A B}}
\]
\begin{tabular}{|c|c|c|}
\hline \multicolumn{2}{|c|}{ Inputs } & Output \\
\hline A & B & Y \\
\hline L & L & \(H\) \\
L & \(H\) & \(H\) \\
\(H\) & L & \(H\) \\
\(H\) & \(H\) & L \\
\hline
\end{tabular}

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage 5.5 V

Output Voltage
Operating Free Air Temperature Range
\begin{tabular}{lr} 
DM54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5401} & \multicolumn{3}{|c|}{DM7401} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline VOH & High Level Output Voltage & & & 5.5 & & & 5.5 & V \\
\hline IOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) }
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline ICEX & High Level Output Current & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{O}}=5.5 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & & & 250 & \(\mu \mathrm{A}\) \\
\hline VOL & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{OL}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\] & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \(V_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline ICCH & Supply Current with Outputs High & \(V_{C C}=\) Max & & 4 & 8 & mA \\
\hline ICCL & Supply Current with Outputs Low & \(V_{C C}=\) Max & & 12 & 22 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Max & Units \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \multirow[t]{2}{*}{\[
\begin{aligned}
& C_{L}=15 \mathrm{pF} \\
& R_{L}=4 \mathrm{k} \Omega\left(t_{P L H}\right) \\
& R_{L}=400 \Omega\left(t_{P H L}\right)
\end{aligned}
\]} & & 45 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & & & 15 & ns \\
\hline
\end{tabular}

\footnotetext{
Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
}

\section*{5402/DM5402/DM7402 \\ Quad 2-Input NOR Gates}

\section*{General Descriptlon}

This device contains four Independent gates each of which performs the logic NOR function.

\section*{Features}
- Alternate Military/Areospace device (5402) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Connection Dlagram}


TL/F/6492-1
Order Number 5402DMQB, 5402FMQB, DM5402J, DM5402W or DM7402N See NS Package Number J14A, N14A or W14B

Function Table
\begin{tabular}{|c|c|c|}
\multicolumn{3}{c|}{\(\mathbf{Y}=\overline{\mathbf{A}+\mathbf{B}}\)} \\
\hline \multicolumn{2}{|c|}{ Inputs } & Output \\
\hline \(\mathbf{A}\) & \(\mathbf{B}\) & \(\mathbf{Y}\) \\
\hline L & L & \(H\) \\
L & \(H\) & L \\
\(H\) & \(L\) & L \\
\(H\) & \(H\) & L \\
\hline
\end{tabular}
\(H=\) High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
5.5V

Operating Free Air Temperature Range
DM54 and 54
\(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
DM74 \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
Storage Temperature Range
\(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5402} & \multicolumn{3}{|c|}{DM7402} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{1}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics}
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
(Note 1) & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\text { Min, } \mathrm{IOL}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline \(1 / 1\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=M a x
\] \\
(Note 2)
\end{tabular}} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 8 & 16 & mA \\
\hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 14 & 27 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Max & Units \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \multirow[t]{2}{*}{\[
\begin{aligned}
& C_{L}=15 \mathrm{pF} \\
& R_{\mathrm{L}}=400 \Omega
\end{aligned}
\]} & & 22 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & & & 15 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{DM5403/DM7403 Quad 2-Input NAND Gates with Open-Collector Outputs}

\section*{General Description}

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

\section*{Pull-Up Resistor Equations}
\(R_{M A X}=\frac{V_{\mathrm{CC}}(\mathrm{Min})-\mathrm{V}_{\mathrm{OH}}}{N_{1}\left(l_{\mathrm{OH}}\right)+\mathrm{N}_{2}\left(I_{\mathrm{I}}\right)}\)
\(R_{\text {MIN }}=\frac{V_{C C}(\text { Max })-V_{O L}}{I_{\mathrm{OL}}-N_{3}\left(I_{I L}\right)}\)
Where: \(\mathrm{N}_{1}\left(\mathrm{I}_{\mathrm{OH}}\right)=\) total maximum output high current for all outputs tied to pull-up resistor
\(\mathrm{N}_{2}\left(\mathrm{I}_{\mathrm{H}}\right)=\) total maximum input high current for all inputs tied to pull-up resistor
\(N_{3}\left(l_{L}\right)=\) total maximum input low current for all inputs tied to pull-up resistor

\section*{Connection Diagram}


\section*{Function Table}
\[
Y=\overline{A B}
\]
\begin{tabular}{|c|c|c|}
\hline \multicolumn{2}{|c|}{ Inputs } & Output \\
\hline A & B & Y \\
\hline L & L & H \\
L & H & H \\
H & L & H \\
H & H & L \\
\hline
\end{tabular}
\(\mathrm{H}=\) High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avallabllity and specifications.


Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5403} & \multicolumn{3}{|c|}{DM7403} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline VCC & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline V OH & High Level Output Voltage & & & 5.5 & & & 5.5 & V \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics}
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(V_{C C}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline ICEX & High Level Output Current & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{V}_{\mathrm{O}}=5.5 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & & & 250 & \(\mu \mathrm{A}\) \\
\hline VOL & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\] & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline 1 H & High Level Input Current & \(V_{C C}=M a x, V_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline 1 LL & Low Level Input Current & \(V_{C C}=M a x, V_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline I'CH & Supply Current with Outputs High & \(V_{C C}=\operatorname{Max}\) & & 4 & 8 & mA \\
\hline ICCL & Supply Current with Outputs Low & \(V_{C C}=M a x\) & & 12 & 22 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|c|c|c|c|c}
\hline Symbol & \multicolumn{1}{|c|}{ Parameter } & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{l}
\(C_{L}=15 \mathrm{pF}\) \\
\(R_{L}=4 \mathrm{k} \Omega\left(t_{P L H}\right)\) \\
\(\mathrm{R}_{\mathrm{L}}=400 \Omega\left(\mathrm{t}_{\mathrm{PHL}}\right)\)
\end{tabular} & 45 & ns \\
\hline & \begin{tabular}{l} 
Propagation Delay Time \\
High to Low Level Output
\end{tabular} & & & 15 & ns \\
\hline
\end{tabular}

\footnotetext{
Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
}

\section*{5404/DM5404/DM7404}

Hex Inverting Gates

\section*{General Description}

This device contains six independent gates each of which performs the logic INVERT function.

\section*{Features}
- Alternate Military/Aerospace device (5404) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Connection Diagram}

Dual-In-Line Package


Order Number 5404DMQB, 5404FMQB, DM5404J, DM5404W, DM7404M or DM7404N
See NS Package Number J14A, M14A, N14A or W14B

\section*{Function Table}
\begin{tabular}{|c|c|}
\multicolumn{2}{c|}{\(\mathbf{Y}=\overline{\mathbf{A}}\)} \\
\hline Inputs & Output \\
\hline \(\mathbf{A}\) & \(\mathbf{Y}\) \\
\hline L & H \\
\(H\) & L \\
\hline
\end{tabular}
\(H=\) High Logic Level
\(L=\) Low Logic Level

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
Operating Free Air Temperature Range
\begin{tabular}{lr} 
DM54 and 54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5404} & \multicolumn{3}{|c|}{DM7404} & \multirow{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
\hline IOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics}
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
(Note 1) & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline VOH & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOH}_{\mathrm{O}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline ILL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=M a x
\] \\
(Note 2)
\end{tabular}} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 6 & 12 & mA \\
\hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 18 & 33 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|c|c|c|c|c}
\hline Symbol & Parameter & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{l}
\(C_{L}=15 \mathrm{pF}\) \\
\(R_{L}=40 \Omega\)
\end{tabular} & 22 & ns \\
\hline tpHL & \begin{tabular}{l} 
Propagation Delay Time \\
High to Low Level Output
\end{tabular} & & & 15 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{DM5405/DM7405 Hex Inverters with Open-Collector Outputs}

\section*{General Description}

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations
\(R_{\text {MAX }}=\frac{V_{\mathrm{CC}}(\mathrm{Min})-\mathrm{V}_{\mathrm{OH}}}{\mathrm{N}_{1}\left(\mathrm{l}_{\mathrm{OH}}\right)+\mathrm{N}_{2}\left(\mathrm{I}_{\mathrm{H}}\right)}\)
\(R_{\text {MIN }}=\frac{V_{C C}(\text { Max })-V_{O L}}{l_{\mathrm{OL}}-N_{3}\left(l_{\mathrm{IL}}\right)}\)
Where: \(\mathrm{N}_{1}(\mathrm{IOH})=\) total maximum output high current for all outputs tied to pull-up resistor
\(\mathrm{N}_{2}\left(\mathrm{I}_{\mathrm{H}}\right)=\) total maximum input high current for all inputs tied to pull-up resistor
\(N_{3}\left(l_{L L}\right)=\) total maximum input low current for all inputs tied to pull-up resistor

\section*{Connection Diagram}

\section*{Dual-In-Line Package}


TL/F/6495-1
Order Number DM5405J, DM5405W or DM7405N
See NS Package Number J14A, N14A or W14B

\section*{Function Table}
\begin{tabular}{|c|c|}
\hline \multicolumn{2}{c|}{\(\mathbf{Y}=\overline{\mathbf{A}}\)} \\
\hline Input & Output \\
\hline \(\mathbf{A}\) & \(\mathbf{Y}\) \\
\hline L & \(H\) \\
\(H\) & L \\
\hline
\end{tabular}
\(H=\) High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avallability and specifications.
Supply Voltage
Input Voltage
Output Voltage
7 V

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Operating Free Air Temperature Range
\begin{tabular}{cr} 
DM54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5405} & \multicolumn{3}{|c|}{DM7405} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & & & 5.5 & & & 5.5 & V \\
\hline lol & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics}
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(I_{\text {CEX }}\) & High Level Output Current & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{O}}=5.5 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & & & 250 & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\] & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(V_{C C}=\) Max, \(V_{l}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{I}_{1}\) & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline ICCH & Supply Current with Outputs High & \(V_{C C}=M a x\) & & 6 & 12 & mA \\
\hline ICCL & Supply Current with Outputs Low & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) & & 18 & 33 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Max & Units \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\
& \mathrm{R}_{\mathrm{L}}=4 \mathrm{k} \Omega\left(\mathrm{t}_{\mathrm{PLH}}\right) \\
& \left.\mathrm{R}_{\mathrm{L}}=400 \Omega \text { (tpHL}\right)
\end{aligned}
\]} & & 55 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & & & 15 & ns \\
\hline
\end{tabular}

\footnotetext{
Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
}

\section*{DM5406/DM7406 Hex Inverting Buffers with High Voltage Open-Collector Outputs}

\section*{General Description}

This device contains six independent buffers each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations
\(R_{M A X}=\frac{V_{\mathrm{O}}(\mathrm{Min})-\mathrm{V}_{\mathrm{OH}}}{\mathrm{N}_{1}\left(\mathrm{l}_{\mathrm{OH}}\right)+\mathrm{N}_{2}\left(I_{\mathrm{IH}}\right)}\)
\(R_{\text {MIN }}=\frac{V_{O}(\text { Max })-V_{O L}}{I_{O L}-N_{3}\left(I_{\mathrm{IL}}\right)}\)
Where: \(\mathrm{N}_{1}\left(\mathrm{I}_{\mathrm{OH}}\right)=\) total maximum output high current for all outputs tied to pull-up resistor
\(N_{2}\left(l_{\mid H}\right)=\) total maximum input high current for all inputs tied to pull-up resistor
\(N_{3}\left(I_{L L}\right)=\) total maximum input low current for all inputs tied to pull-up resistor

\section*{Connection Diagram}

\section*{Dual-In-Line Package}


TL/F/6496-1
Order Number DM5406J, DM5406W, DM7406M or DM7406N
See NS Package Number J14A, M14A, N14A or W14B

Function Table
\begin{tabular}{|c|c|}
\hline \multicolumn{1}{c|}{\(\mathbf{Y}=\overline{\mathbf{A}}\)} \\
\hline Input & Output \\
\hline \(\mathbf{A}\) & \(\mathbf{Y}\) \\
\hline L & H \\
\(H\) & L \\
\hline
\end{tabular}
\(H=\) High Logic Level
\(L=\) Low Logic Level
\begin{tabular}{lr} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for avallability and specifications. \\
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Output Voltage & 30 V \\
Operating Free Air Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM54 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
DM74 & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5406} & \multicolumn{3}{|c|}{DM7406} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{1}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & & & 30 & & & 30 & V \\
\hline loL & Low Level Output Current & & & 30 & & & 40 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(V_{C C}=\) Min, \(I_{I}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline ICEX & High Level Output Current & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{O}}=30 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & & & 250 & \(\mu \mathrm{A}\) \\
\hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\] & & & 0.7 & \multirow[t]{2}{*}{V} \\
\hline & & \(\mathrm{IOL}=16 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & & & 0.4 & \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \(V_{C C}=M a x, V_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline 1 IL & Low Level Input Current & \(V_{C C}=M a x, V_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline \(\mathrm{I}_{\mathrm{CCH}}\) & Supply Current with Outputs High & \(V_{C C}=\operatorname{Max}\) & & 30 & 48 & mA \\
\hline \(I_{\text {CCL }}\) & Supply Current with Outputs Low & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) & & 27 & 51 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|c|c|c|c|c}
\hline Symbol & Parameter & Conditions & Min & Max & Units \\
\hline tpLH & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{c}
\(C_{L}=15 \mathrm{pF}\) \\
\(R_{\mathrm{L}}=110 \Omega\)
\end{tabular} & 15 & ns \\
\hline tPHL & \begin{tabular}{l} 
Propagation Delay Time \\
High to Low Level Output
\end{tabular} & & & 23 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).

\section*{DM5407/DM7407 Hex Buffers with \\ High Voltage Open-Collector Outputs}

\section*{General Description}

This device contains six independent gates each of which performs a buffer function. The open-collector outputs require external pull-up resistors for proper logical operation.

\section*{Pull-Up Resistor Equations}
\(R_{\text {MAX }}=\frac{V_{\mathrm{O}}(\mathrm{Min})-\mathrm{V}_{\mathrm{OH}}}{\mathrm{N}_{1}\left(\mathrm{l}_{\mathrm{OH}}\right)+\mathrm{N}_{2}\left(\mathrm{I}_{\mathrm{H}}\right)}\)
\(\mathrm{R}_{\mathrm{MIN}}=\frac{\mathrm{V}_{\mathrm{O}}(\mathrm{Max})-\mathrm{V}_{\mathrm{OL}}}{\mathrm{I}_{\mathrm{OL}}-\mathrm{N}_{3}\left(\mathrm{I}_{\mathrm{LL}}\right)}\)
Where: \(\mathrm{N}_{1}\left(\mathrm{l}_{\mathrm{OH}}\right)=\) total maximum output high current for all outputs tied to pull-up resistor
\(\mathrm{N}_{2}\left(I_{\mathrm{IH}}\right)=\) total maximum input high current for all inputs tied to pull-up resistor
\(N_{3}\left(I_{1 L}\right)=\) total maximum input low current for all inputs tied to pull-up resistor

\section*{Connection Diagram}

\section*{Dual-In-Line Package}


TL/F/6497-1
Order Number DM5407J, DM5407W, DM7407M or DM7407N See NS Package Number J14A, M14A, N14A or W14B

\section*{Function Table}
\begin{tabular}{|c|c|}
\multicolumn{2}{c|}{\(\mathbf{Y}=\mathbf{A}\)} \\
\hline Input & Output \\
\hline \(\mathbf{A}\) & \(\mathbf{Y}\) \\
\hline L & L \\
\(H\) & \(H\) \\
\hline
\end{tabular}
\(H=\) High Logic Level
\(\mathrm{L}=\) Low Logic Level
\begin{tabular}{lr} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Output Voltage & 30 V \\
Operating Free Air Temperature Range & \\
DM54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5407} & \multicolumn{3}{|c|}{DM7407} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(V_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline VOH & High Level Output Voltage & & & 30 & & & 30 & V \\
\hline lOL & Low Level Output Current & & & 30 & & & 40 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & \begin{tabular}{l}
Typ \\
(Note 1)
\end{tabular} & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(V_{C C}=\operatorname{Min}, l_{1}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline ICEX & High Level Output Current & \[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{O}}=30 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\] & & & 250 & \(\mu \mathrm{A}\) \\
\hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \[
\begin{aligned}
& V_{C C}=\operatorname{Min}, I_{O L}=M a x \\
& V_{I L}=M a x
\end{aligned}
\] & & & 0.7 & \multirow[t]{2}{*}{V} \\
\hline & & \(\mathrm{I}_{\mathrm{OL}}=16 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & & & 0.4 & \\
\hline 1 & Input Current @ Max Input Voltage & \(V_{C C}=\) Max, \(V_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \(V_{C C}=\) Max, \(V_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline lCCH & Supply Current with Outputs High & \(V_{C C}=M a x\) & & 29 & 41 & mA \\
\hline ICCL & Supply Current with Outputs Low & \(V_{C C}=M a x\) & & 21 & 30 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|c|c|c|c|c}
\hline Symbol & Parameter & Conditions & Min & Max & Units \\
\hline tpLH \(^{\text {tPHL }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{l}
\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\) \\
\(\mathrm{R}_{\mathrm{L}}=110 \Omega\)
\end{tabular} & & 10 & ns \\
\cline { 1 - 1 } & \begin{tabular}{l} 
Propagation Delay Time \\
High to Low Level Output
\end{tabular} & & 30 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).

\section*{5408/DM5408/DM7408}

Quad 2-Input AND Gates

\section*{General Description}

This device contains four independent gates each of which performs the logic AND function.

\section*{Features}
- Alternate Military/Aerospace device (5408) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Connection Diagram}


TL/F/6498-1
Order Number 5408DMQB, 5408FMQB, DM5408J, DM5408W or DM7408N See NS Package Number J14A, N14A or W14B

\section*{Function Table}
\begin{tabular}{|c|c|c|}
\multicolumn{3}{c|}{\(Y=A B\)} \\
\hline \multicolumn{2}{|c|}{ Inputs } & Output \\
\hline \(\mathbf{A}\) & \(\mathbf{B}\) & \(\mathbf{Y}\) \\
\hline\(L\) & \(L\) & \(L\) \\
\(L\) & \(H\) & \(L\) \\
\(H\) & \(L\) & \(L\) \\
\(H\) & \(H\) & \(H\) \\
\hline
\end{tabular}

\footnotetext{
\(H=\) High Logic Level
L = Low Logic Level
}

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
5.5 V

Operating Free Air Temperature Range
\[
\begin{aligned}
& \text { DM54 and } 54 \\
& \text { DM74 } \\
& \text { Storage Temperature Range }
\end{aligned}
\]

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5408} & \multicolumn{3}{|c|}{DM7408} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \begin{tabular}{l}
Typ \\
(Note 1)
\end{tabular} & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline VOH & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \({ }_{1 / \mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& \text { (Note 2) }
\end{aligned}
\]} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 11 & 21 & mA \\
\hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 20 & 33 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|c|c|c|c|c}
\hline Symbol & Parameter & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{c}
\(C_{L}=15 \mathrm{pF}\) \\
\(R_{\mathrm{L}}=400 \Omega\)
\end{tabular} & 27 & ns \\
\hline t \(_{\text {PHL }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
High to Low Level Output
\end{tabular} & & & 19 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{5409/DM7409 Quad 2-Input AND Gates with Open-Collector Outputs}

\section*{General Description}

This device contains four independent gates each of which performs the logic AND function. The open-collector outputs require external pull-up resistors for proper logical operation.

\section*{Pull-Up Resistor Equations}
\(R_{\text {MAX }}=\frac{V_{\mathrm{CC}}(\mathrm{Min})-\mathrm{V}_{\mathrm{OH}}}{N_{1}\left(\mathrm{l}_{\mathrm{OH}}\right)+\mathrm{N}_{2}\left(\mathrm{I}_{\mathrm{H}}\right)}\)
\(R_{\text {MIN }}=\frac{V_{C C}(M a x)-V_{O L}}{I_{O L}-N_{3}\left(I_{\mathrm{IL}}\right)}\)
Where: \(\mathrm{N}_{1}\left(\mathrm{I}_{\mathrm{OH}}\right)=\) total maximum output high current for all outputs tied to pull-up resistor
\(\mathrm{N}_{2}\left(\mathrm{I}_{\mathrm{IH}}\right)=\) total maximum input high current for all inputs tied to pull-up resistor
\(N_{3}\left(I_{I L}\right)=\) total maximum input low current for all inputs tied to pull-up resistor

\section*{Connection Diagram}


Order Number 5409DMQB, 5409FMQB or DM7409N See NS Package Number J14A, N14A or W14B

Function Table
\[
Y=A B
\]
\begin{tabular}{|c|c|c|}
\hline \multicolumn{2}{|c|}{ Inputs } & Output \\
\hline A & B & Y \\
\hline L & L & L \\
L & \(H\) & L \\
\(H\) & L & L \\
H & \(H\) & \(H\) \\
\hline
\end{tabular}

\footnotetext{
H = High Logic Level
L = Low Logic Level
}
\begin{tabular}{lr} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Output Voltage & 7 V \\
Operating Free Air Temperature Range & \\
54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{5409} & \multicolumn{3}{|c|}{DM7409} & \multirow{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & & & 5.5 & & & 5.5 & V \\
\hline \(\mathrm{lOL}^{\text {l }}\) & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline ICEX & High Level Output Current & \[
\begin{aligned}
& V_{C C}=\operatorname{Min}, V_{O}=5.5 \mathrm{~V} \\
& V_{I H}=\operatorname{Min}
\end{aligned}
\] & & & 250 & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{I}_{\text {LL }}\) & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline ICCH & Supply Current with Outputs High & \(V_{C C}=\operatorname{Max}\) & & 11 & 21 & mA \\
\hline ICCL & Supply Current with Outputs Low & \(V_{C C}=\operatorname{Max}\) & & 20 & 33 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|c|c|c|c|c}
\hline Symbol & \multicolumn{1}{c|}{ Parameter } & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{l}
\(C_{L}=15 \mathrm{pF}\) \\
\(\mathrm{R}_{\mathrm{L}}=40 \Omega\)
\end{tabular} & 32 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
High to Low Level Output
\end{tabular} & & 24 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).

\section*{5410/DM5410/DM7410 \\ Triple 3-Input NAND Gates}

\section*{General Description}

This device contains three independent gates each of which performs the logic NAND function.

\section*{Features}
- Alternate Military/Aerospace device (5410) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Connection Diagram}


Order Number 5410DMQB, 5410FMQB, DM5410J, DM5410W or DM7410N See NS Package Number J14A, N14A or W14B

\section*{Function Table}
\[
\mathbf{Y}=\overline{\mathbf{A B C}}
\]
\begin{tabular}{|c|c|c|c|}
\hline \multicolumn{3}{|c|}{ Inputs } & Output \\
\hline A & B & C & Y \\
\hline\(X\) & \(X\) & \(L\) & H \\
\(X\) & L & \(X\) & H \\
L & X & X & H \\
\(H\) & \(H\) & \(H\) & L \\
\hline
\end{tabular}
\(H=\) High Logic Level
L = Low Logic Level
\(X=\) Either Low or High Logic Level

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
Operating Free Air Temperature Range

DM54 and 54
DM74
Storage Temperature Range

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The 'Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5410} & \multicolumn{3}{|c|}{DM7410} & \multirow{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(V_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOH}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=\operatorname{Max}
\] \\
(Note 2)
\end{tabular}} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 3 & 6 & mA \\
\hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 9 & 16.5 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|l|c|c|c|c}
\hline Symbol & \multicolumn{1}{c|}{ Parameter } & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{l}
\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\) \\
\(\mathrm{R}_{\mathrm{L}}=400 \Omega\)
\end{tabular} & 22 & ns \\
\hline \(\mathrm{t}_{\mathrm{PHL}}\) & \begin{tabular}{l} 
Propagation Delay Time \\
High to Low Level Output
\end{tabular} & & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{DM7411}

\section*{Triple 3-Input AND Gate}

\section*{General Description}

This device contains three independent gates with three data inputs each which perform the logic AND function.

\section*{Connection Diagram}


Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage 5.5 V

Operating Free Air
Temperature Range (DM74)
Storage Temperature Range

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operations.

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multirow{2}{*}{ Parameter } & \multicolumn{2}{|c|}{ DM7411 } & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & Typ & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -0.4 & mA \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 16 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline VOH & High Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \[
\begin{aligned}
& V_{C C}=\operatorname{Min}, I_{O L}=M a x, \\
& V_{I H}=\operatorname{Min}
\end{aligned}
\] & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \(V_{C C}=M a x, V_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline ILL & Low Level Input Current & \(V_{C C}=\) Max, \(V_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline los & Short Circuit Output Current & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\text { Max } \\
& \text { (Note 2) } \\
& \hline
\end{aligned}
\] & -18 & & -57 & mA \\
\hline ICCH & Supply Current with Outputs High & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) & & & 15 & mA \\
\hline ICCL & Supply Current with Outputs Low & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) & & & 24 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|l|c|c|c|c}
\hline Symbol & \multicolumn{1}{|c|}{ Parameter } & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{l}
\(C_{L}=15 \mathrm{pF}\), \\
\(R_{L}=400 \Omega\)
\end{tabular} & 27 & ns \\
\cline { 1 - 1 } & & & & 19 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{DM5414/DM7414 Hex Inverter with Schmitt Trigger Inputs}

\section*{General Description}

This device contains six independent gates each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

\section*{Connection Diagram}

Dual-In-Line Package


Order Number DM5414J, DM5414W or DM7414N
See NS Package Number J14A, N14A or W14B
Function Table
\begin{tabular}{|c|c|}
\multicolumn{1}{c}{\(\mathbf{Y}=\overline{\mathbf{A}}\)} \\
\hline Input & Output \\
\hline \(\mathbf{A}\) & \(\mathbf{Y}\) \\
\hline L & \(H\) \\
\(H\) & L \\
\hline
\end{tabular}
\(\mathrm{H}=\) High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)
If Milltary/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
Operating Free Air Temperature Range
\begin{tabular}{cr} 
DM54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5414} & \multicolumn{3}{|c|}{DM7414} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{T}+}\) & \begin{tabular}{l}
Positive-Going Input \\
Threshold Voltage (Note 1)
\end{tabular} & 1.5 & 1.7 & 2 & 1.5 & 1.7 & 2 & V \\
\hline \(\mathrm{V}_{\text {T- }}\) & Negative-Going Input Threshold Voltage (Note 1) & 0.6 & 0.9 & 1.1 & 0.6 & 0.9 & 1.1 & V \\
\hline HYS & Input Hysteresis (Note 1) & 0.4 & 0.8 & & 0.4 & 0.8 & & V \\
\hline \(\mathrm{l}^{\mathrm{OH}}\) & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline loL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics}
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \begin{tabular}{l}
Typ \\
(Note 2)
\end{tabular} & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{T}-\mathrm{Min}}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{T}+} \mathrm{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline \({ }^{T}+\) & Input Current at Positive-Going Threshold & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~V}_{1}=\mathrm{V}_{\mathrm{T}+}\)} & & -0.43 & & mA \\
\hline \({ }_{1}\) - & Input Current at Negative-Going Threshold & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~V}_{1}=\mathrm{V}_{\mathrm{T}-}\)} & & -0.56 & & mA \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.2 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=\operatorname{Max}
\] \\
(Note 3)
\end{tabular}} & DM54 & -18 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 22 & 36 & mA \\
\hline \({ }^{\text {ICCL }}\) & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & 39 & 60 & mA \\
\hline
\end{tabular}

Note 1: \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\)
Note 2: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 3: Not more than one output should be shorted at a time.

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Max & Units \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & \multirow[t]{2}{*}{\[
\begin{aligned}
& C_{L}=15 \mathrm{pF} \\
& R_{L}=400 \Omega
\end{aligned}
\]} & & 22 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & & & 22 & ns \\
\hline
\end{tabular}

\section*{DM5416/DM7416 Hex Inverting Buffers with High Voltage Open-Collector Outputs}

\section*{General Description}

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

\section*{Pull-Up Resistor Equations}
\(R_{M A X}=\frac{V_{O}(\mathrm{Min})-V_{\mathrm{OH}}}{N_{1}\left(I_{\mathrm{OH}}\right)+N_{2}\left(I_{\mathrm{IH}}\right)}\)
\(R_{\text {MIN }}=\frac{V_{\mathrm{O}}(\mathrm{Max})-\mathrm{V}_{\mathrm{OL}}}{\mathrm{I}_{\mathrm{OL}}-\mathrm{N}_{3}\left(\mathrm{I}_{\mathrm{IL}}\right)}\)
Where: \(\mathrm{N}_{1}\left(\mathrm{l}_{\mathrm{OH}}\right)=\) total maximum output high current for all outputs tied to pull-up resistor
\(\mathrm{N}_{2}\left(l_{\mid H}\right)=\) total maximum input high current for all inputs tied to pull-up resistor
\(N_{3}\left(I_{\mathrm{IL}}\right)=\) total maximum input low current for all inputs tied to pull-up resistor

\section*{Connection Diagram}


Function Table
\begin{tabular}{|c|c|}
\multicolumn{2}{c|}{\(\mathbf{Y}=\overline{\mathbf{A}}\)} \\
\hline Input & Output \\
\hline \(\mathbf{A}\) & \(\mathbf{Y}\) \\
\hline L & \(H\) \\
\(H\) & L \\
\hline
\end{tabular}
\(H=\) High Logic Level
\(L=\) Low Logic Level

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
7 V
Input Voltage
5.5 V

Output Voltage 15 V
Operating Free Air Temperature Range
\begin{tabular}{cr} 
DM54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5416} & \multicolumn{3}{|c|}{DM7416} & \multirow{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & & & 15 & & & 15 & V \\
\hline lOL & Low Level Output Current & & & 30 & & & 40 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ
(Note 1) & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \(V_{C C}=M i n, l_{1}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline ICEX & High Level Output Current & \[
\begin{aligned}
& V_{C C}=\operatorname{Min}, V_{O}=15 V \\
& V_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\] & & & 250 & \(\mu \mathrm{A}\) \\
\hline \multirow[t]{2}{*}{VOL} & \multirow[t]{2}{*}{Low Level Output Voltage} & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{I H}=\operatorname{Min}
\end{aligned}
\] & & & 0.7 & \multirow[t]{2}{*}{V} \\
\hline & & \(\mathrm{I}_{\mathrm{OL}}=16 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & & & 0.4 & \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \({ }_{1 / \mathrm{H}}\) & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline \(1 / 2\) & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline ICCH & Supply Current with Outputs High & \(V_{C C}=\operatorname{Max}\) & & 30 & 48 & mA \\
\hline ICCL & Supply Current with Outputs Low & \(V_{C C}=\operatorname{Max}\) & & 27 & 51 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|c|c|c|c|c}
\hline Symbol & \multicolumn{1}{|c|}{ Parameter } & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{c}
\(C_{L}=15 \mathrm{pF}\) \\
\(R_{L}=110 \Omega\)
\end{tabular} & 15 & ns \\
\hline \cline { 1 - 1 } & & & 23 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).

DM5417/DM7417 Hex Buffers with
High Voltage Open-Collector Outputs

\section*{General Description}

This device contains six independent gates each of which performs a buffer function. The open-collector outputs require external pull-up resistors for proper logical operation.

\section*{Pull-Up Resistor Equations}
\(R_{M A X}=\frac{V_{\mathrm{O}}(\mathrm{Min})-\mathrm{V}_{\mathrm{OH}}}{N_{1}\left(\mathrm{I}_{\mathrm{OH}}\right)+\mathrm{N}_{2}\left(\mathrm{I}_{\mathrm{IH}}\right)}\)
\(R_{\text {MIN }}=\frac{V_{\mathrm{O}}(\mathrm{Max})-V_{\mathrm{OL}}}{l_{\mathrm{OL}}-\mathrm{N}_{3}\left(I_{\mathrm{IL}}\right)}\)
Where: \(\mathrm{N}_{1}(\mathrm{l} \mathrm{OH})=\) total maximum output high current for all outputs tied to pull-up resistor
\(\mathrm{N}_{2}\left(\mathrm{I}_{\mathrm{H}}\right)=\) total maximum input high current for all inputs tied to pull-up resistor
\(N_{3}\left(I_{L}\right)=\) total maximum input low current for all inputs tied to pull-up resistor

\section*{Connection Diagram}

\section*{Dual-In-Line Package}


Order Number DM5417J, DM5417W or DM7417N
See NS Package Number J14A, N14A or W14B

\section*{Function Table}
\begin{tabular}{|c|c|}
\multicolumn{2}{c|}{\(\mathbf{Y}=\mathbf{A}\)} \\
\hline Input & Output \\
\hline \(\mathbf{A}\) & \(\mathbf{Y}\) \\
\hline L & L \\
H & H \\
\hline
\end{tabular}

\footnotetext{
H = High Logic Level
L = Low Logic Level
}

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
\begin{tabular}{lr} 
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Output Voltage & 15 V \\
Operating Free Air Temperature Range & \\
DM54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5417} & \multicolumn{3}{|c|}{DM7417} & \multirow{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & & & 15 & & & 15 & V \\
\hline loL & Low Level Output Current & & & 30 & & & 40 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{I}}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline ICEX & High Level Output Current & \[
\begin{aligned}
& V_{C C}=\operatorname{Min}, V_{O}=15 \mathrm{~V} \\
& V_{I H}=\operatorname{Min}
\end{aligned}
\] & & & 250 & \(\mu \mathrm{A}\) \\
\hline \multirow[t]{2}{*}{\(\mathrm{V}_{\text {OL }}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & & & 0.7 & \multirow[t]{2}{*}{V} \\
\hline & & \(\mathrm{l}_{\mathrm{OL}}=16 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & & & 0.4 & \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline \({ }^{\text {CCH }}\) & Supply Current with Outputs High & \(V_{C C}=\operatorname{Max}\) & & 29 & 41 & mA \\
\hline \(I_{\text {CCL }}\) & Supply Current with Outputs Low & \(V_{C C}=\operatorname{Max}\) & & 21 & 30 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Max & Units \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \multirow[t]{2}{*}{\[
\begin{aligned}
& C_{\mathrm{L}}=15 \mathrm{pF} \\
& \mathrm{R}_{\mathrm{L}}=110 \Omega
\end{aligned}
\]} & & 10 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & & & 30 & ns \\
\hline
\end{tabular}

\footnotetext{
Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
}

National Semiconductor

\section*{5420/DM5420/DM7420}

Dual 4-Input NAND Gates

\section*{General Description}

This device contains two independent gates each of which performs the logic NAND function.

\section*{Features}

Alternate Military/Aerospace device (5420) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Connection Diagram}


TL/F/6506-1
Order Number 5420DMQB, 5420FMQB, DM5420J, DM5420W or DM7420N See NS Package Number J14A, N14A or W14B

Function Table
\begin{tabular}{|c|c|c|c|c|}
\multicolumn{5}{c|}{\(\mathbf{Y}=\overline{\mathbf{A B C D}}\)} \\
\hline \multicolumn{4}{|c|}{ Inputs } & Output \\
\hline A & B & C & D & Y \\
\hline X & X & X & L & H \\
X & X & L & X & H \\
X & L & X & X & H \\
L & X & X & X & H \\
H & H & H & H & L \\
\hline
\end{tabular}
\(H=\) High Logic Level
L = Low Logic Level
\(X=\) Either Low or High Logic Level
Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for availability and specifications. \begin{tabular}{l} 
Note: The "Absolute Maximum Ratings" are those values \\
beyond which the safety of the device cannot be guaran- \\
teed. The device should' not be operated at these limits. The
\end{tabular}

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5402} & \multicolumn{3}{|c|}{DM7402} & \multirow{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
(Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline I/L & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& \text { (Note 2) }
\end{aligned}
\]} & DM54 & \(-20\) & & -55 & \multirow{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & 2 & 4 & mA \\
\hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & 6 & 11 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|c|c|c|c|c}
\hline Symbol & \multicolumn{1}{c|}{ Parameter } & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{l}
\(C_{L}=15 \mathrm{pF}\) \\
\(R_{L}=400 \Omega\)
\end{tabular} & & 22 & ns \\
\hline\(t_{\text {PHL }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
High to Low Level Output
\end{tabular} & & 15 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{5425/DM7425 \\ Dual 4-Input NOR Gate (with Strobe)}

\section*{General Description}

This device contains two, 4-input gates that perform the logic NOR function. The output of each NOR gate is gated (strobed) by pin 3 and pin 11 by positive true logic i.e., logic "1" equals output on.

\section*{Connection Diagram}



Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{2}{*}{\(I_{1 H}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=2.4 V
\end{aligned}
\]} & Strobe & & & 160 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Inputs & & & 40 & \\
\hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x, \\
& V_{1}=0.4 V \\
& \hline
\end{aligned}
\]} & Strobe & & & -6.4 & \multirow[t]{2}{*}{mA} \\
\hline & & & Inputs & & & -1.6 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=M a x
\] \\
(Note 2)
\end{tabular}} & 54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -57 & \\
\hline \({ }^{\text {CCH }}\) & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(V_{C C}=M a x\)} & & & 16 & mA \\
\hline \(\mathrm{I}_{\mathrm{CCL}}\) & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & & 19 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(V_{C C}=5 V, T_{A}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|c|c|c|c|c}
\hline Symbol & Parameter & Conditions & Min & Max & Units \\
\hline t \(_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{c}
\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\) \\
\(\mathrm{R}_{\mathrm{L}}=400 \Omega\)
\end{tabular} & 22 & ns \\
\hline t \begin{tabular}{c} 
PHL
\end{tabular} & \begin{tabular}{l} 
Propagation Delay Time \\
High to Low Level Output
\end{tabular} & & 15 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{DM5426/DM7426 Quad 2-Input NAND Gates with High Voltage Open-Collector Outputs}

\section*{General Description}

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

\section*{Pull-Up Resistor Equations}
\(R_{M A X}=\frac{V_{\mathrm{O}}(\mathrm{Min})-\mathrm{V}_{\mathrm{OH}}}{N_{1}\left(I_{\mathrm{OH}}\right)+N_{2}\left(I_{\mathrm{IH}}\right)}\)
\(R_{\text {MIN }}=\frac{V_{\mathrm{O}}(\mathrm{Max})-\mathrm{V}_{\mathrm{OL}}}{\mathrm{IOL}_{\mathrm{OL}}-\mathrm{N}_{3}\left(\mathrm{I}_{\mathrm{LL}}\right)}\)
Where: \(\mathrm{N}_{1}\left(\mathrm{l}_{\mathrm{OH}}\right)=\) total maximum output high current for all outputs tied to pull-up resistor
\(\mathrm{N}_{2}\left(\mathrm{I}_{\mathrm{IH}}\right)=\) total maximum input high current for all inputs tied to pull-up resistor
\(N_{3}\left(I_{L}\right)=\) total maximum input low current for all inputs tied to pull-up resistor

\section*{Connection Diagram}

\section*{Dual-In-Line Package}


TL/F/6508-1
Order Number DM5426J or DM7426N
See NS Package Number J14A or N14A
Function Table
\begin{tabular}{|c|c|c|}
\multicolumn{3}{c|}{\(\mathbf{Y}=\overline{\mathbf{A B}}\)} \\
\hline \multicolumn{2}{|c|}{ Inputs } & Output \\
\hline \(\mathbf{A}\) & \(\mathbf{B}\) & \(\mathbf{Y}\) \\
\hline L & L & \(H\) \\
L & \(H\) & \(H\) \\
\(H\) & L & \(H\) \\
\(H\) & \(H\) & L \\
\hline
\end{tabular}

\footnotetext{
\(H=\) High Logic Level
L = Low Logic Level
}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{9}{|l|}{Absolute Maximum Ratings (Note)} \\
\hline \multicolumn{3}{|l|}{If Military/Aerospace specified devices are required please contact the National Semiconductor Sale Office/Distributors for availability and specifications.} & \multicolumn{6}{|l|}{\multirow[t]{4}{*}{Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.}} \\
\hline \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Supply Voltage Input Voltage}} & 7V & & & & & & \\
\hline & & 5.5 V & & & & & & \\
\hline Output & & 15 & & & & & & \\
\hline \multicolumn{2}{|l|}{\begin{tabular}{ll} 
DM54 \\
DM74 & \(-55^{\circ}\)
\end{tabular}} & \(125^{\circ} \mathrm{C}\)
\(+70^{\circ} \mathrm{C}\) & & & & & & \\
\hline \multicolumn{2}{|l|}{Storage Temperature Range} & \(50^{\circ} \mathrm{C}\) & & & & & & \\
\hline \multicolumn{9}{|l|}{Recommended Operating Conditions} \\
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5426} & \multicolumn{3}{|c|}{DM7426} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & & & 15 & & & 15 & V \\
\hline loL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics}
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) }
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \multirow[t]{2}{*}{ICEX} & \multirow[t]{2}{*}{High Level Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min} \\
& V_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & \(\mathrm{V}_{\mathrm{O}}=15 \mathrm{~V}\) & & & 1000 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & \(\mathrm{V}_{\mathrm{O}}=12 \mathrm{~V}\) & & & 50 & \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\text { Min, } I_{O L}=M a x \\
& V_{I H}=M i n
\end{aligned}
\]} & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline 1 IL & Low Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\) Max, \(V_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \({ }^{\text {ICCH }}\) & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & 4 & 8 & mA \\
\hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 12 & 22 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|c|c|c|c|c}
\hline Symbol & \multicolumn{1}{c|}{ Parameter } & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{c}
\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\) \\
\(R_{L}=1 \mathrm{k} \Omega(\mathrm{tPLH})\)
\end{tabular} & 24 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
High to Low Level Output
\end{tabular} & & & 17 & ns \\
\hline
\end{tabular}

\footnotetext{
Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
}

\section*{DM7427 Triple 3-Input NOR Gates}

\section*{General Description}

This device contains three independent gates each of which performs the logic NOR function.

\section*{Connection Diagram}


Function Table
\begin{tabular}{|c|c|c|c|}
\hline \multicolumn{3}{|c|}{ Inputs } & Output \\
\hline A & B & C & Y \\
\hline L & L & L & H \\
X & X & H & L \\
X & H & X & L \\
H & X & X & L \\
\hline
\end{tabular}
\(H=\) High Logic Level
L = Low Logic Level
\(X=\) Either High or Low Logic Level

Absolute Maximum Ratings (Note)
\begin{tabular}{lr} 
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \\
\(\quad\) DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{l|l|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multirow{2}{*}{ Parameter } & \multicolumn{2}{c|}{ DM7427 } & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -0.8 & mA \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 16 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ
(Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{I}}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\] & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline 1 IL & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline los & Short Circuit Output Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 2) & -18 & & -57 & mA \\
\hline ICCH & Supply Current with Outputs High & \(\mathrm{V}_{\text {CC }}=\mathrm{Max}\) & & 10 & 16 & mA \\
\hline ICCL & Supply Current with Outputs Low & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) & & 16 & 26 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|c|c|c|c|c}
\hline Symbol & \multicolumn{1}{|c|}{ Parameter } & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{l}
\(C_{L}=15 \mathrm{pF}\) \\
\(R_{L}=400 \Omega\)
\end{tabular} & & 11 & ns \\
\cline { 1 - 1 } & & & & 15 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{5430/DM5430/DM7430 \\ 8-Input NAND Gate}

\section*{General Description}

This device contains a single gate which performs the logic NAND function.

Alternate Military/Aerospace device (5430) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Connection Diagram}

Dual-In-Line Package


TL/F/6510-1
Order Number 5430DMBQ, 5430FMQB, DM5430J, DM5430W or DM7430N See NS Package Number J14A, N14A or W14B

\section*{Function Table}
\begin{tabular}{|c|c|}
\hline \(\mathbf{Y}=\overline{\text { ABCDEFGH }}\) \\
\hline Inputs & Output \\
\hline A thru H & \(\mathbf{Y}\) \\
\hline All Inputs H & L \\
One or More & H \\
Input L & \\
\hline
\end{tabular}
\(H=\) High Logic Level
\(L=\) Low Logic Level

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
Operating Free Air Temperature Range
DM54 and 54
DM74
\(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
\(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
Storage Temperature Range

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5430} & \multicolumn{3}{|c|}{DM7430} & \multirow{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
(Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min}, I_{O L}=M a x \\
& V_{I H}=\operatorname{Min}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\) Max, \(V_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{I}_{\mathrm{LL}}\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=\operatorname{Max}
\] \\
(Note 2)
\end{tabular}} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\)} & & 1 & 2 & mA \\
\hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 3 & 6 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{l|l|c|c|c|c}
\hline Symbol & Parameter & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{l}
\(C_{L}=15 \mathrm{pF}\) \\
\(R_{L}=400 \Omega\)
\end{tabular} & 22 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
High to Low Level Output
\end{tabular} & & & 15 & ns \\
\hline
\end{tabular}

\footnotetext{
Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
}

\section*{5432/DM5432/DM7432 \\ Quad 2-Input OR Gates}

\section*{General Description}

This device contains four independent gates each of which performs the logic OR function.

\section*{Features}
- Alternate Military/Aerospace device (5432) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Connection Diagram}


TL/F/6511-1
Order Number 5432DMQB, 5432FMQB, DM5432J, DM5432W or DM7432N See NS Package Number J14A, N14A or W14B

Function Table
\begin{tabular}{|c|c|c|}
\multicolumn{3}{c|}{\(\mathbf{Y}=\mathbf{A}+\mathbf{B}\)} \\
\hline \multicolumn{2}{|c|}{ Inputs } & Output \\
\hline \(\mathbf{A}\) & \(\mathbf{B}\) & \(\mathbf{Y}\) \\
\hline L & L & L \\
L & \(H\) & \(H\) \\
\(H\) & L & \(H\) \\
\(H\) & \(H\) & \(H\) \\
\hline
\end{tabular}
\(H=\) High Logic Level
\(L=\) Low Logic Level
\begin{tabular}{lr} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM54 and 54 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
DM74 & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5432} & \multicolumn{3}{|c|}{DM7432} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline TA & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics}
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
(Note 1) & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=M a x
\] \\
(Note 2)
\end{tabular}} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline \({ }^{\text {ICCH }}\) & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 15 & 22 & mA \\
\hline \({ }^{\text {ICCL }}\) & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}\)} & & 23 & 38 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Max & Units \\
\hline tplH & Propagation Delay Time Low to High Level Output & \multirow[t]{2}{*}{\[
\begin{aligned}
& C_{L}=15 \mathrm{pF} \\
& R_{\mathrm{L}}=400 \Omega
\end{aligned}
\]} & & 15 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & & & 22 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{5437/DM5437/DM7437}

\section*{Quad 2-Input NAND Buffers}

\section*{General Description}

This device contains four independent gates each of which performs the logic NAND function.

\section*{Features}
- Alternate Military/Aerospace device (5437) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Connection Diagram}


TL/F/6512-1
Order Number 5437DMQB, 5437FMQB, DM5437J, DM5437W or DM7437N See NS Package Number J14A, N14A or W14B

\section*{Function Table}
\begin{tabular}{|c|c|c|}
\hline \multicolumn{3}{c|}{\(Y=\overline{\mathbf{A B}}\)} \\
\hline \multicolumn{2}{|c|}{ Inputs } & Output \\
\hline \(\mathbf{A}\) & \(\mathbf{B}\) & \(\mathbf{Y}\) \\
\hline\(L\) & \(L\) & \(H\) \\
\(L\) & \(H\) & \(H\) \\
\(H\) & \(L\) & \(H\) \\
\(H\) & \(H\) & \(L\) \\
\hline
\end{tabular}
\(H=\) High Logic Level
L = Low Logic Level
\begin{tabular}{lr} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \\
DM54 and 54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM 74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5437} & \multicolumn{3}{|c|}{DM7437} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -1.2 & & & -1.2 & mA \\
\hline lol & Low Level Output Current & & & 48 & & & 48 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics}
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
(Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & 2.4 & 3.3 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline 1 IH & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, V_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& \text { (Note 2) }
\end{aligned}
\]} & DM54 & -20 & & -70 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -70 & \\
\hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 9 & 15.5 & mA \\
\hline \({ }^{\text {I CCL }}\) & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 34 & 54 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|c|c|c|c|c}
\hline Symbol & \multicolumn{1}{|c|}{ Parameter } & Conditions & Min & Max & Units \\
\hline tpLH \(^{t_{P H L}}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{l}
\(\mathrm{C}_{\mathrm{L}}=45 \mathrm{pF}\) \\
\(\mathrm{R}_{\mathrm{L}}=133 \Omega\)
\end{tabular} & 22 & ns \\
\cline { 1 - 1 } & \begin{tabular}{l} 
Propagation Delay Time \\
High to Low Level Output
\end{tabular} & & 15 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{DM5438/DM7438 Quad 2-Input NAND Buffers with Open-Collector Outputs}

\section*{General Description}

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations
\(R_{\text {MAX }}=\frac{V_{\mathrm{CC}}(\mathrm{Min})-\mathrm{V}_{\mathrm{OH}}}{\mathrm{N}_{1}\left(\mathrm{l}_{\mathrm{OH}}\right)+\mathrm{N}_{2}\left(\mathrm{I}_{\mathrm{I}}\right)}\)
\(R_{\mathrm{MIN}}=\frac{\mathrm{V}_{\mathrm{CC}}(\mathrm{Max})-\mathrm{V}_{\mathrm{OL}}}{\mathrm{l}_{\mathrm{OL}}-\mathrm{N}_{3}\left(\mathrm{IIL}^{2}\right)}\)
Where: \(\mathrm{N}_{1}\left(\mathrm{l}_{\mathrm{OH}}\right)=\) total maximum output high current for all outputs tied to pull-up resistor
\(\mathrm{N}_{2}\left(\mathrm{I}_{1 H}\right)=\) total maximum input high current for all inputs tied to pull-up resistor
\(N_{3}\left(l_{1 L}\right)=\) total maximum input low current for all inputs tied to pull-up resistor

\section*{Connection Diagram}

Dual-In-LIne Package


Order Number DM5438J, DM5438W, DM7438M or DM7438N See NS Package Number J14A, M14A, N14A or W14B

\section*{Function Table}
\[
\mathbf{Y}=\overline{\mathbf{A B}}
\]
\begin{tabular}{|c|c|c|}
\hline \multicolumn{2}{|c|}{ Inputs } & Output \\
\hline A & \(\mathbf{B}\) & \(\mathbf{Y}\) \\
\hline L & L & \(H\) \\
L & \(H\) & \(H\) \\
\(H\) & L & \(H\) \\
\(H\) & \(H\) & L \\
\hline
\end{tabular}
\(H=\) High Logic Level
L = Low Logic Level
Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
\begin{tabular}{lr} 
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Output Voltage & 7 V \\
Operating Free Air Temperature Range & \\
DM54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5438} & \multicolumn{3}{|c|}{DM7438} & \multirow{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & & & 5.5 & & & 5.5 & V \\
\hline lOL & Low Level Output Current & & & 48 & & & 48 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics}
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ
(Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(I_{\text {cex }}\) & High Level Output Current & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{V}_{\mathrm{O}}=5.5 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & & & 250 & \(\mu \mathrm{A}\) \\
\hline VoL & Low Level Output Voltage & \[
\begin{aligned}
& V_{C C}=\operatorname{Min}, I_{O L}=M a x \\
& V_{I H}=\operatorname{Min}
\end{aligned}
\] & & & 0.4 & V \\
\hline 1 & Input Current @Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\) Max, \(\mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline IL & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\) Max, \(\mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline ICCH & Supply Current with Outputs High & \(\mathrm{V}_{\mathrm{CC}}=\) Max & & 5 & 8.5 & mA \\
\hline ICCL & Supply Current with Outputs Low & \(\mathrm{V}_{\mathrm{CC}}=\) Max & & 34 & 54 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|l|c|c|c|c}
\hline Symbol & \multicolumn{1}{|c|}{ Parameter } & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{c}
\(C_{L}=45 \mathrm{pF}\) \\
\(R_{\mathrm{L}}=133 \Omega\)
\end{tabular} & 22 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
High to Low Level Output
\end{tabular} & & & 18 & ns \\
\hline
\end{tabular}

\footnotetext{
Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
}

\section*{DM7439 Quad 2-Input NAND Buffer with Open-Collector Output}

\section*{General Description}

This device contains four independent gates with two data inputs, each which performs the logic NAND function.

\section*{Connection Diagram}



Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline VOH & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=250 \mu \mathrm{~A} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \multirow[t]{3}{*}{VOL} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min} \\
& V_{I H}=2.0 \mathrm{~V}
\end{aligned}
\]} & \(\mathrm{IOL}=48 \mathrm{~mA}\) & & 0.2 & 0.4 & \\
\hline & & & \(\mathrm{l}_{\mathrm{OL}}=60 \mathrm{~mA}\) & & & 0.5 & V \\
\hline & & & \(\mathrm{l} \mathrm{OL}=80 \mathrm{~mA}\) & & & 0.6 & \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, V_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline 1 IL & Low Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 2)} & -18 & & -57 & mA \\
\hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & & 8.5 & mA \\
\hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & & 54 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|c|c|c|c|c}
\hline Symbol & Parameter & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{l}
\(C_{L}=15 \mathrm{pF}\) \\
\(R_{L}=400 \Omega\)
\end{tabular} & 22 & ns \\
\hline tpHL & \begin{tabular}{l} 
Propagation Delay Time \\
High to Low Level Output
\end{tabular} & & & 18 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{5440/DM7440 Dual 4-Input NAND Buffer}

\section*{General Description}

This device contains two, 4 input gates that perform the Logic NAND function. Outputs have 48 mA loL.

\section*{Connection Diagrams}


TL/F/9777-2
Order Number 5440FMQB See NS Package Number W14B


\section*{Electrical Characteristics}

Over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(I_{1 H}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=\operatorname{Max}
\] \\
(Note 2)
\end{tabular}} & 54 & -20 & & -70 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -70 & \\
\hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(V_{C C}=M a x\)} & & & 8 & mA \\
\hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & & 27 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Max & Units \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \multirow[t]{2}{*}{\[
\begin{aligned}
& C_{L}=15 \mathrm{pF} \\
& R_{\mathrm{L}}=400 \Omega
\end{aligned}
\]} & & 22 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & & & 15 & ns \\
\hline
\end{tabular}

5442A/DM5442A/DM7442A BCD to Decimal Decoders

\section*{General Description}

These BCD-to-decimal decoders consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of input logic ensures that all outputs remain off for all invalid (10-15) input conditions.

\section*{Features}
- Diode clamped inputs
- Also for application as 4 -line-to-16-line decoders; 3-line-to-8-line decoders
- All outputs are high for invalid input conditions
- Typical power dissipation 140 mW
- Typical propagation delay 17 ns
- Alternate Military/Aerospace device (5442A) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

Connection Diagram


TL/F/6516-1
Order Number 5442ADMQB, 5442AFMQB, DM5442AJ, DM5442AW or DM7442AN See NS Package Number J16A, N16E or W16A

\section*{Function Table}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{No.} & \multicolumn{4}{|c|}{BCD Input} & \multicolumn{10}{|c|}{Decimal Output} \\
\hline & D & C & B & A & 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 \\
\hline 0 & L & L & L & L & L & H & H & H & H & H & H & H & H & H \\
\hline 1 & L & L & L & H & H & L & H & H & H & H & H & H & H & H \\
\hline 2 & L & L & H & L & H & H & L & H & H & H & H & H & H & H \\
\hline 3 & L & L & H & H & H & H & H & L & H & H & H & H & H & H \\
\hline 4 & L & H & L & L & H & H & H & H & L & H & H & H & H & H \\
\hline 5 & L & H & L & H & H & H & H & H & H & L & H & H & H & H \\
\hline 6 & L & H & H & L & H & H & H & H & H & H & L & H & H & H \\
\hline 7 & L & H & H & H & H & H & H & H & H & H & H & L & H & H \\
\hline 8 & H & L & L & L & H & H & H & H & H & H & H & H & L & H \\
\hline 9 & H & L & L & H & H & H & H & H & H & H & H & H & H & L \\
\hline 1 & H & L & H & L & H & H & H & H & H & H & H & H & H & H \\
\hline \(N\) & H & L & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline V & H & H & L & L & H & H & H & H & H & H & H & H & H & H \\
\hline A & H & H & L & H & H & H & H & H & H & H & H & H & H & H \\
\hline L & H & H & H & L & H & H & H & H & H & H & H & H & H & H \\
\hline 1 & H & H & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline D & & & & & & & & & & & & & & \\
\hline
\end{tabular}

\footnotetext{
\(\mathrm{H}=\) High Level
L = Low Level
}

\section*{Absolute Maximum Ratings (Note)}

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
7 V
Input Voltage
5.5 V

Operating Free Air Temperature Range
DM54 and 54
\(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
DM74
\(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
Storage Temperature Range
\(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5442A} & \multicolumn{3}{|c|}{DM7442A} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \({ }^{\mathrm{IOH}}\) & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline lol & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) } \\
\hline
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=M i n, I_{O L}=M a x \\
& V_{I H}=M i n, V_{I L}=M a x
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline \(1 / 1\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{\mathrm{CC}}=M a x \\
& \text { (Note 2) }
\end{aligned}
\]} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline \multirow[t]{2}{*}{Icc} & \multirow[t]{2}{*}{Supply Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& \text { (Note 3) }
\end{aligned}
\]} & DM54 & & 28 & 41 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & & 28 & 56 & \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: ICC is measured with all outputs open and all inputs grounded.

Switching Characteristics at \(\mathrm{V}_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Max & Units \\
\hline tpHL & Propagation Delay Time High to Low Level Output from A, B, C or D through 2 Levels of Logic & \multirow[t]{4}{*}{\[
\begin{aligned}
& C_{L}=15 \mathrm{pF} \\
& R_{L}=400 \Omega
\end{aligned}
\]} & & 25 & ns \\
\hline tPHL & Propagation Delay Time High to Low Level Output from A, B, C or D through 3 Levels of Logic & & & 30 & ns \\
\hline tPLH & Propagation Delay Time Low to High Level Output from A, B, C or D through 2 Levels of Logic & & & 25 & ns \\
\hline tPLH & Propagation Delay Time Low to High Level Output from A, B, C or D through 3 Levels of Logic & & & 30 & ns \\
\hline
\end{tabular}

\section*{Logic Diagram}


National Semiconductor

\section*{DM5445/DM7445 BCD to Decimal Decoders/Drivers}

\section*{General Description}

These BCD-to-decimal decoders/drivers consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of BCD input logic ensures that all outputs remain off for all invalid (10-15) binary input conditions. These decoders feature high-performance, NPN output transistors designed for use as indicator/relay drivers, or as open-collector logic-circuit drivers. The high-breakdown output transistors are compatible for interfacing with most MOS integrated circuits.

\section*{Connection Diagram}

\section*{Features}
- Full decoding of input logic
- 80 mA sink-current capability
- All outputs are off for invalid BCD input conditions


TL/F/6517-1
Order Number DM5445J, DM5445W or DM7445N See NS Package Number J16A, N16E or W16A

445N

Function Table
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{No.} & \multicolumn{4}{|c|}{Inputs} & \multicolumn{10}{|c|}{Outputs} \\
\hline & D & C & B & A & 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 \\
\hline 0 & L & L & L & L & L & H & H & H & H & H & H & H & H & H \\
\hline 1 & L & L & L & H & H & L & H & H & H & H & H & H & H & H \\
\hline 2 & L & L & H & L & H & H & L & H & H & H & H & H & H & H \\
\hline 3 & L & L & H & H & H & H & H & L & H & H & H & H & H & H \\
\hline 4 & L & H & L & L & H & H & H & H & L & H & H & H & H & H \\
\hline 5 & L & H & L & H & H & H & H & H & H & L & H & H & H & H \\
\hline 6 & L & H & H & L & H & H & H & H & H & H & L & H & H & H \\
\hline 7 & L & H & H & H & H & H & H & H & H & H & H & L & H & H \\
\hline 8 & H & L & L & L & H & H & H & H & H & H & H & H & L & H \\
\hline 9 & H & L & L & H & H & H & H & H & H & H & H & H & H & L \\
\hline 1 & H & L & H & L & H & H & H & H & H & H & H & H & H & H \\
\hline N & H & L & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline V & H & H & L & L & H & H & H & H & H & H & H & H & H & H \\
\hline A & H & H & L & H & H & H & H & H & H & H & H & H & H & H \\
\hline L & H & H & H & L & H & H & H & H & H & H & H & H & H & H \\
\hline 1 & H & H & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline D & & & & & & & & & & & & & & \\
\hline
\end{tabular}
\(H=\) High Level (Off), L = Low Level (On)
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{9}{|l|}{Absolute Maximum Ratings (Note)} \\
\hline \multicolumn{3}{|l|}{If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.} & \multicolumn{6}{|l|}{\multirow[t]{4}{*}{Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.}} \\
\hline \multicolumn{2}{|l|}{\multirow[t]{3}{*}{Supply Voltage Input Voltage}} & 7 V & & & & & & \\
\hline & & 5.5 V & & & & & & \\
\hline & & 30 & & & & & & \\
\hline Operating DM54 DM74 & Air Temperature Range & \(125^{\circ} \mathrm{C}\)
\(+70^{\circ} \mathrm{C}\) & & & & & & \\
\hline \multicolumn{2}{|l|}{Storage Temperature Range} & \(150^{\circ} \mathrm{C}\) & & & & & & \\
\hline \multicolumn{9}{|l|}{Recommended Operating Conditions} \\
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5445} & \multicolumn{3}{|c|}{DM7445} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline VOH & High Level Output Voltage & & & 30 & & & 30 & V \\
\hline \(\mathrm{IOL}^{\text {l }}\) & Low Level Output Current & & & 20 & & & 20 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \begin{tabular}{l}
Typ \\
(Note 1)
\end{tabular} & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Min}, l_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline ICEX & High Level Output Current & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=M i n, V_{O}=30 V \\
& V_{\mathrm{IL}}=M a x, V_{I H}=M i n
\end{aligned}
\]} & & & 250 & \(\mu \mathrm{A}\) \\
\hline \multirow[t]{2}{*}{\(\mathrm{V}_{\text {OL }}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline & & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{l}_{\mathrm{OL}}=80 \mathrm{~mA} \\
& \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min} \\
& \hline
\end{aligned}
\]} & & 0.5 & 0.9 & \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{Icc} & \multirow[t]{2}{*}{Supply Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& (\text { Note 2) }
\end{aligned}
\]} & DM54 & & 43 & 62 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & & 43 & 70 & \\
\hline
\end{tabular}

Switching Characteristics
at \(V_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{A}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|c|c|c|c|c}
\hline Symbol & \multicolumn{1}{c}{ Parameter } & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{l}
\(C_{L}=15 \mathrm{pF}\) \\
\(R_{L}=100 \Omega\)
\end{tabular} & & 49.5 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
High to Low Level Output
\end{tabular} & & 49.5 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: ICC is measured with all inputs grounded and all outputs open.


TL/F/6517-2

National Semiconductor

\section*{DM7446A, DM5447A/DM7447A}

BCD to 7-Segment Decoders/Drivers

\section*{General Description}

The 46A and 47A feature active-low outputs designed for driving common-anode LEDs or incandescent indicators directly. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown on a following page. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.
All of the circuits incorporate automatic leading and/or trail-ing-edge, zero-blanking control (RBI and RBO). Lamp test (LT) of these devices may be performed at any time when the BI/RBO node is at a high logic level. All types contain
an overriding blanking input (BI) which can be used to control the lamp intensity (by pulsing) or to inhibit the outputs.

\section*{Features}
- All circuit types feature lamp intensity modulation capability
- Open-collector outputs drive indicators directly
- Lamp-test provision

■ Leading/trailing zero suppression

\section*{Connection Diagram}


Order Number DM5447AJ, DM7446AN or DM7447AN
See NS Package Number J16A or N16E
\begin{tabular}{lr} 
Absolute Maximum Ratings (Note) \\
Af Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM54 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
DM74 & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM7446A} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage (a thru g) & & & 30 & V \\
\hline IOH & High Level Output Current (BI/RBO) & & & -0.2 & \(\mu \mathrm{A}\) \\
\hline lOL & Low Level Output Current (a thru g) & & & 40 & mA \\
\hline lOL & Low Level Output Current (BI/RBO) & & & 8 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{'46A Electrical Characteristics}
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
(Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage (BI/RBO) & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min} \\
& I_{O H}=\mathrm{Max}
\end{aligned}
\]} & 2.4 & 3.7 & & V \\
\hline ICEX & High Level Output Current (a thru g) & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Max}, V_{O}=30 V \\
& V_{I L}=M a x, V_{I H}=\operatorname{Min}
\end{aligned}
\]} & & & 250 & \(\mu \mathrm{A}\) \\
\hline VOL & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{lOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & 0.3 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Max}, V_{1}=5.5 \mathrm{~V} \\
& \text { (Except BI/RBO) }
\end{aligned}
\]} & & & 1 & mA \\
\hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\begin{tabular}{l}
\[
V_{C C}=\operatorname{Max}, V_{1}=2.4 V
\] \\
(Except BI/RBO)
\end{tabular}} & & & 40 & \(\mu \mathrm{A}\) \\
\hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=0.4 V
\end{aligned}
\]} & BI/RBO & & & -4 & \multirow[t]{2}{*}{mA} \\
\hline & & & Others & & & -1.6 & \\
\hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}(\mathrm{BI} / \mathrm{RBO})\)} & & & -4 & mA \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\begin{tabular}{l}
\[
V_{C C}=M a x
\] \\
(Note 2)
\end{tabular}} & & 60 & 103 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: ICC is measured with all outputs open and all inputs at 4.5 V .
'46A Switching Characteristics
at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{l|l|c|c|c|c}
\hline Symbol & Parameter & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{l}
\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\) \\
\(\mathrm{R}_{\mathrm{L}}=120 \Omega\)
\end{tabular} & & 100 & ns \\
\cline { 1 - 1 } & & & 100 & ns \\
\hline
\end{tabular}

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5447A} & \multicolumn{3}{|c|}{DM7447A} & \multirow{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage (a thru g) & & & 15 & & & 15 & V \\
\hline IOH & High Level Output Current (BI/RBO) & & & -0.2 & & & -0.2 & \(\mu \mathrm{A}\) \\
\hline loL & Low Level Output Current (a thru g) & & & 40 & & & 40 & mA \\
\hline IOL & Low Level Output Current (BI/RBO) & & & 8 & & & 8 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{'47A Electrical Characteristics}
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|r|}{Conditions} & Min & Typ
(Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage (BI/RBO) & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min} \\
& \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
& \hline
\end{aligned}
\]} & 2.4 & 3.7 & & V \\
\hline ICEX & High Level Output Current (a thru g) & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Max}, V_{O}=15 \mathrm{~V} \\
& V_{\mathrm{IL}}=\operatorname{Max}, V_{I H}=\operatorname{Min}
\end{aligned}
\]} & & & 250 & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & 0.3 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=0.4 V
\end{aligned}
\]} & BI/RBO & & & -4 & \multirow[t]{2}{*}{mA} \\
\hline & & & Others & & & -1.6 & \\
\hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}(\mathrm{BI} / \mathrm{RBO})\)} & & & -4 & mA \\
\hline \multirow[t]{2}{*}{Icc} & \multirow[t]{2}{*}{Supply Current} & \multirow[t]{2}{*}{\[
V_{C C}=\operatorname{Max}
\]
(Note 2)} & DM54 & & 60 & 85 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & & 60 & 103 & \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: \(\mathrm{I}_{\mathrm{CC}}\) is measured with all outputs open and all inputs at 4.5 V .

\section*{'47A Switching Characteristics}
at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{l|l|c|c|c|c}
\hline Symbol & Parameter & Conditions & Min & Max & Units \\
\hline tPLH & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{c}
\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\) \\
\(\mathrm{R}_{\mathrm{L}}=120 \Omega\)
\end{tabular} & & 100 & ns \\
\cline { 1 - 3 } & & & & 100 & ns \\
\hline
\end{tabular}

\section*{Function Table}

46A, 47A
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Decimal or Function} & \multicolumn{6}{|c|}{Inputs} & \multirow[t]{2}{*}{\begin{tabular}{l}
BI/RBO \\
(Note 1)
\end{tabular}} & \multicolumn{7}{|c|}{Outputs} & \multirow[t]{2}{*}{Note} \\
\hline & LT & RBI & D & C & B & A & & a & b & c & d & e & \(f\) & g & \\
\hline 0 & H & H & L & L & L & L & H & L & L & L & L & L & L & H & \multirow{16}{*}{(2)} \\
\hline 1 & H & X & L & L & L & H & H & H & L & L & H & H & H & H & \\
\hline 2 & H & X & L & L & H & L & H & L & L & H & L & L & H & L & \\
\hline 3 & H & X & L & L & H & H & H & L & L & L & L & H & H & L & \\
\hline 4 & H & X & L & H & L & L & H & H & L & L & H & H & L & L & \\
\hline 5 & H & X & L & H & L & H & H & L & H & L & L & H & L & L & \\
\hline 6 & H & X & L & H & H & L & H & H & H & L & L & L & L & L & \\
\hline 7 & H & X & L & H & H & H & H & L & L & L & H & H & H & H & \\
\hline 8 & H & X & H & L & L & L & H & L & L & L & L & L & L & L & \\
\hline 9 & H & X & H & L & L & H & H & L & L & L & H & H & L & L & \\
\hline 10 & H & X & H & L & H & L & H & H & H & H & L & L & H & L & \\
\hline 11 & H & X & H & L & H & H & H & H & H & L & L & H & H & L & \\
\hline 12 & H & X & H & H & L & L & H & H & L & H & H & H & L & L & \\
\hline 13 & H & X & H & H & L & H & H & L & H & H & L & H & L & L & \\
\hline 14 & H & x & H & H & H & L & H & H & H & H & L & L & L & L & \\
\hline 15 & H & X & H & H & H & H & H & H & H & H & H & H & H & H & \\
\hline BI & X & X & X & X & X & X & L & H & H & H & H & H & H & H & (3) \\
\hline RBI & H & L & L & L & L & L & L & H & H & H & H & H & H & H & (4) \\
\hline LT & L & X & X & X & X & X & H & L & L & L & L & L & L & L & (5) \\
\hline
\end{tabular}

Note 1: BI/RBO is a wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).
Note 2: The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
Note 3: When a low logic level is applied directly to the blanking input (BI), all segment outputs are high regardless of the level of any other input.
Note 4: When ripple-blanking input (RBI) and inputs \(A, B, C\), and \(D\) are at a low level with the lamp test input high, all segment outputs go \(H\) and the rippleblanking output (RBO) goes to a low level (response condition).
Note 5: When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are L . \(H=\) High level, \(L=\) Low level, \(X=\) Don't Care

\section*{DM7450 Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate}

\section*{General Description}

This device contains two independent combinations of gates, each of which perform the logic AND-OR-INVERT function. One set of gates has an expander node.

\section*{Connection Diagram}



Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multirow{2}{*}{ Parameter } & \multicolumn{2}{|c|}{ DM7450 } & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & Nom & Max & \\
\hline\(V_{\text {CC }}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{~V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -0.4 & mA \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 16 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics}

Over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ (Note 1) & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \(V_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=-400 \mu \mathrm{~A} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Max}
\end{aligned}
\] & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline IX & Expander Current & \[
\begin{aligned}
& \mathrm{V} 1=0.4 \mathrm{~V}, \mathrm{I}_{\mathrm{OL}}=16 \mathrm{~mA} \\
& \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~T}_{\mathrm{A}}=\mathrm{Min}
\end{aligned}
\] & & & 3.1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline \(1 / 12\) & Low Level Input Current & \(V_{C C}=\) Max, \(\mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline los & Short Circuit Output Current & \(\mathrm{V}_{\mathrm{CC}}=\operatorname{Max}\) (Note 2) & -18 & & -57 & mA \\
\hline ICCH & Supply Current with Outputs High & \(\mathrm{V}_{C C}=\mathrm{Max}\) & & & 8 & mA \\
\hline ICCL & Supply Current with Outputs Low & \(\mathrm{V}_{C C}=\mathrm{Max}\) & & & 14 & mA \\
\hline \(V_{B E(Q)}\) & Base-Emitter Voltage of Output Transistor Q & \[
\begin{aligned}
& \mathrm{I} 1=0.62 \mathrm{~mA} \\
& \mathrm{I}_{\mathrm{OL}}=16 \mathrm{~mA} \\
& \mathrm{R}_{1}=0 \Omega
\end{aligned}
\] & & & 1.0 & V \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|l|c|c|c|c}
\hline Symbol & \multicolumn{1}{|c|}{ Parameter } & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{l}
\(C_{L}=15 \mathrm{pF}\) \\
\(R_{\mathrm{L}}=400 \Omega\)
\end{tabular} & & 22 & ns \\
\hline & & & & 15 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 V, T_{A}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{5451/DM7451}

\section*{Dual 2-Wide, 2-Input AOI Gate}

\section*{General Description}

This device contains two independent combinations of gates, each of which perform the logic AND-OR-INVERT
function.

\section*{Connection Diagram}

Absolute Maximum Ratings (Note)
\begin{tabular}{lr} 
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage \\
Input Voltage & 7 V \\
Operating Free Air Temperature Range \\
54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for acutual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{5451} & \multicolumn{3}{|c|}{DM7451} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & . & & -0.8 & & & -0.4 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|r|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline VOH & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\) Max, \(V_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\) Max, \(V_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline \(1 / 2\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& (\text { Note 2) }
\end{aligned}
\]} & 54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -57 & \\
\hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(V_{C C}=M a x\)} & & & 8 & mA \\
\hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & & 14 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|c|c|c|c|c}
\hline Symbol & \multicolumn{1}{|c|}{ Parameter } & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{c}
\(C_{L}=15 \mathrm{pF}\) \\
\(R_{L}=40 \Omega\)
\end{tabular} & 22 & ns \\
\cline { 1 - 1 } & & & 15 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, T_{A}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{5473/DM5473/DM7473 \\ Dual Master-Slave J-K Flip-Flops with Clear and Complementary Outputs}

\section*{General Description}

This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The \(J\) and K data is processed by the flip-flops after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high the \(J\) and \(K\) inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic states of the J and K inputs must not be allowed to change while the clock is high. Data
transfers to the outputs on the falling edge of the clock pulse. A low logic level on the clear input will reset the outputs regardless of the logic states of the other inputs.

\section*{Features}
- Alternate Military/Aerospace device (5473) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Connection Diagram}

\section*{Dual-In-Line Package}


TL/F/6525-1
Order Number 5473DMQB, 5473FMQB, DM5473J, DM5473W or DM7473N
See NS Package Number J14A, N14A or W14B

\section*{Function Table}
\begin{tabular}{|c|c|c|c|cc|}
\hline \multicolumn{4}{|c|}{ Inputs } & \multicolumn{2}{c|}{ Outputs } \\
\hline CLR & CLK & J & K & Q & \(\overline{\mathbf{Q}}\) \\
\hline\(L\) & X & X & X & L & \(H\) \\
\(H\) & \(\Omega\) & \(L\) & \(L\) & \(Q_{0}\) & \(\bar{Q}_{0}\) \\
\(H\) & \(\Omega\) & \(H\) & \(L\) & \(H\) & \(L\) \\
\(H\) & \(\Omega\) & \(L\) & \(H\) & \(L\) & \(H\) \\
\(H\) & \(\Omega\) & \(H\) & \(H\) & \multicolumn{2}{|c|}{ Toggle } \\
\hline
\end{tabular}
\(\mathrm{H}=\) High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
\(\Omega=\) Positive pulse data. the J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.
\(Q_{0}=\) The output logic level before the indicated input conditions were established.
Toggle \(=\) Each output changes to the complement of its previous level on each high level clock pulse.
\begin{tabular}{|c|c|}
\hline \multicolumn{2}{|l|}{Absolute Maximum Ratings (Note)} \\
\hline \multicolumn{2}{|l|}{please contact the National Semiconductor Sales Office/Distributors for availability and specifications.} \\
\hline Supply Voltage & \\
\hline Input Voltage & 5.5 \\
\hline Operating Free Air Temperature Rang & \\
\hline DM54 and 54 & \(-55^{\circ} \mathrm{C}\) \\
\hline DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
\hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \\
\hline
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM5473} & \multicolumn{3}{|c|}{DM7473} & \multirow{2}{*}{Units} \\
\hline & & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{IOH}^{\text {O }}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & & & -0.4 & mA \\
\hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & & & 16 & mA \\
\hline fCLK & \multicolumn{2}{|l|}{Clock Frequency (Note 5)} & 0 & & 15 & 0 & & 15 & MHz \\
\hline \multirow[t]{3}{*}{tw} & \multirow[t]{3}{*}{Pulse Width (Note 5)} & Clock High & 20 & & & 20 & & & \multirow{3}{*}{ns} \\
\hline & & Clock Low & 47 & & & 47 & & & \\
\hline & & Clear Low & 25 & & & 25 & & & \\
\hline tsu & \multicolumn{2}{|l|}{Input Setup Time (Note 1 \& 5)} & \(0 \uparrow\) & & & \(0 \uparrow\) & & & ns \\
\hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Input Hold Time (Note 1 \& 5)} & 0 \(\downarrow\) & & & 0 \(\downarrow\) & & & ns \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics}
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 2) } \\
\hline
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, l_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\
& V_{I L}=\operatorname{Max}, V_{I H}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}_{\mathrm{O}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\) Max, \(V_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{3}{*}{1 H} & \multirow[t]{3}{*}{High Level Input Current} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=2.4 V
\end{aligned}
\]} & J, K & & & 40 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Clock & & & 80 & \\
\hline & & & Clear & & & 80 & \\
\hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=0.4 V
\end{aligned}
\]} & J, K & & & -1.6 & \multirow{3}{*}{mA} \\
\hline & & & Clock & & & -3.2 & \\
\hline & & & Clear & & & -3.2 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
& (\text { Note 3) }
\end{aligned}
\]} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\) Max, (Note 4)} & & 18 & 34 & mA \\
\hline
\end{tabular}

Note 1: The symbol ( \(\uparrow, \downarrow\) ) indicates the edge of the clock pulse is used for reference: ( \(\uparrow\) ) for rising edge, ( \(\downarrow\) ) for falling edge.
Note 2: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 3: Not more than one output should be shorted at a time.
Note 4: With all outputs open, ICc is measured with the \(Q\) and \(\bar{Q}\) outputs high in turn. At the time of measurement the clock input grounded.
Note 5: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|c|}{\[
\begin{aligned}
& \mathrm{R}_{\mathrm{L}}=400 \Omega \\
& \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}
\end{aligned}
\]} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 15 & & MHz \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
Clear \\
to Q
\end{tabular} & & 40 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
\begin{aligned}
& \text { Clear } \\
& \text { to } \bar{Q}
\end{aligned}
\] & & 25 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Q or \(\bar{Q}\) & & 40 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to \(Q\) or \(\bar{Q}\) & & 25 & ns \\
\hline
\end{tabular}

\section*{5474/DM5474/DM7474}

\section*{Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs}

\section*{General Description}

This device contains two independent positive-edge-triggered \(D\) flip-flops with complementary outputs. The information on the \(D\) input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the \(D\) input may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not
violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

\section*{Features}
- Alternate Military/Aerospace device (5474) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Connection Diagram}


Order Number 5474DMQB, 5474FMQB, DM5474J, DM5474W, DM7474M or DM7474N See NS Package Number J14A, M14A, N14A or W14B

Function Table
\begin{tabular}{|c|c|c|c|cc|}
\hline \multicolumn{5}{|c|}{ Inputs } & \multicolumn{2}{c|}{ Outputs } \\
\hline PR & CLR & CLK & D & Q & \(\overline{\mathbf{Q}}\) \\
\hline L & H & X & X & H & L \\
H & L & X & X & L & H \\
L & L & X & X & \(H^{*}\) & \(H^{*}\) \\
H & \(H\) & \(\uparrow\) & \(H\) & \(H\) & L \\
H & \(H\) & \(\uparrow\) & L & L & \(H\) \\
\(H\) & \(H\) & H & X & \(Q_{0}\) & \(\bar{Q}_{0}\) \\
\hline
\end{tabular}

H = High Logic Level
\(X=\) Either Low or High Logic Level
\(L=\) Low Logic Level
\(\uparrow=\) Positive-going transition of the clock.
* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (high) level.
\(Q_{0}=\) The output logic level of \(Q\) before the indicated input conditions were established.

Absolute Maximum Ratings (Note)
If Milltary/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
\(\begin{array}{lr}\text { Operating Free Air Temperature Range } & \\ \text { DM54 and } 54 & -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\ \text { DM74 } & 0^{\circ} \mathrm{C} \text { to }+70^{\circ} \mathrm{C} \\ \text { Storage Temperature Range } & -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C}\end{array}\)
\begin{tabular}{lr} 
DM54 and 54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM5474} & \multicolumn{3}{|c|}{DM7474} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{\text {CC }}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{1}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
\hline \({ }_{\mathrm{IOH}}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & & & -0.4 & mA \\
\hline l OL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & & & 16 & mA \\
\hline \(\mathrm{f}_{\text {CLK }}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & & 15 & 0 & & 15 & MHz \\
\hline \multirow[t]{4}{*}{tw} & \multirow[t]{4}{*}{Pulse Width (Note 2)} & Clock High & 30 & & & 30 & & & \multirow{4}{*}{ns} \\
\hline & & Clock Low & 37 & & & 37 & & & \\
\hline & & Clear Low & 30 & & & 30 & & & \\
\hline & & Preset Low & 30 & & & 30 & & & \\
\hline tsu & \multicolumn{2}{|l|}{Input Setup Time (Notes 1 \& 2)} & \(20 \uparrow\) & & & \(20 \uparrow\) & & & ns \\
\hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Input Hold Time (Notes 1 \& 2)} & \(5 \uparrow\) & & & \(5 \uparrow\) & & & ns \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Note 1: The symbol \((\uparrow)\) indicates the rising edge of the clock pulse is used for reference.
Note 2: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min &  & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Min}, \_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{VOH}^{\text {O }}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{4}{*}{\({ }_{1} \mathrm{H}\)} & \multirow[t]{4}{*}{High Level Input Current} & \multirow[t]{4}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{I}=2.4 V
\end{aligned}
\]} & D & & & 40 & \multirow{4}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Clock & & & 80 & \\
\hline & & & Clear & & & 120 & \\
\hline & & & Preset & & & 40 & \\
\hline \multirow[t]{4}{*}{IIL} & \multirow[t]{4}{*}{Low Level Input Current} & \multirow[t]{4}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
& \mathrm{~V}_{1}=0.4 \mathrm{~V} \\
& \text { (Note } 6 \text { ) }
\end{aligned}
\]} & D & & & -1.6 & \multirow{4}{*}{mA} \\
\hline & & & Clock & & & -3.2 & \\
\hline & & & Clear & & & -3.2 & \\
\hline & & & Preset & & & -1.6 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& \text { (Note 4) }
\end{aligned}
\]} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\operatorname{Max}\) (Note 5)} & & 17 & 30 & mA \\
\hline
\end{tabular}

Note 3: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 4: Not more than one output should be shorted at a time.
Note 5: With all outputs open, ICC is measured with the \(Q\) and \(\bar{Q}\) outputs high in turn. At the time of measurement the clock is grounded.
Note 6: Clear is tested with preset high and preset is tested with clear high.
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|c|}{\[
\begin{aligned}
& \mathrm{R}_{\mathrm{L}}=400 \Omega \\
& \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}
\end{aligned}
\]} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(f_{\text {max }}\) & Maximum Clock Frequency & & 15 & & MHz \\
\hline \({ }^{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Preset to \(\bar{Q}\) & & 40 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Preset to Q & & 25 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
\begin{aligned}
& \text { Clear } \\
& \text { to } Q
\end{aligned}
\] & & 40 & ns \\
\hline tple & Propagation Delay Time Low to High Level Output & \[
\begin{aligned}
& \text { Clear } \\
& \text { to } \bar{Q}
\end{aligned}
\] & & 25 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Q or \(\bar{Q}\) & & 40 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Q or \(\bar{Q}\) & & 25 & ns \\
\hline
\end{tabular}

5475/DM5475/DM7475

\section*{Quad Latches}

\section*{General Description}

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the \(Q\) input when the enable \((G)\) is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the \(Q\) output until the enable is permitted to go high.

These latches feature complementary \(Q\) and \(\bar{Q}\) outputs from a 4-bit latch and are available in 16-pin packages.

\section*{Features}
- Alternate Military/Aerospace device (5475) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Connection Diagram}

\section*{Dual-In-Line Package}


Order Number 5475DMQB, 5475FMQB, DM5475J, DM5475W or DM7475N
See NS Package Number J16A, N16E or W16A

\section*{Function Table (Each Latch)}
\begin{tabular}{|c|c|c|c|}
\hline \multicolumn{2}{|c|}{ Inputs } & \multicolumn{2}{c|}{ Outputs } \\
\hline D & \(\mathbf{G}\) & \(\mathbf{Q}\) & \(\overline{\mathbf{Q}}\) \\
\hline L & H & L & H \\
H & H & H & L \\
X & L & \(\mathrm{Q}_{0}\) & \(\overline{\mathrm{Q}}_{0}\) \\
\hline
\end{tabular}

H = High Level, L = Low Level, X = Don't Care, \(Q_{0}=\) The Level of \(Q\) Before the High-to-Low Transition of \(G\)

Logic Diagram (Each Latch)

\begin{tabular}{ll} 
Absolute Maximum Ratings (Note) & \\
If Military/Aerospace specified devices are required, & Note: The "Absolute Maximum Ratings" are those values \\
please contact the National Semiconductor Sales & \begin{tabular}{l} 
beyond which the safety of the device cannot be guaran- \\
Office/Distributors for avallablility and specifications. \\
teed. The device should not be operated at these limits. The
\end{tabular} \\
Supply Voltage & 7 V
\end{tabular} \begin{tabular}{l} 
parametric values defined in the "Electrical Characteristics" \\
table are not guaranteed at the absolute maximum ratings.
\end{tabular}

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5475} & \multicolumn{3}{|c|}{DM7475} & \multirow{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \({ }_{\mathrm{OH}}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
\hline lol & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(t_{W}\) & Enable Pulse Width (Note 4) & 20 & & & 20 & & & ns \\
\hline tsu & Setup Time (Note 4) & 20 & & & 20 & & & ns \\
\hline \(\mathrm{t}_{\mathrm{H}}\) & Hold Time (Note 4) & 5 & & & 5 & & & ns \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 80 & \(\mu \mathrm{A}\) \\
\hline I/L & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -3.2 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& (\text { Note 2) }
\end{aligned}
\]} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline \multirow[t]{2}{*}{Icc} & \multirow[t]{2}{*}{Supply Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=\text { Max } \\
& \text { (Note 3) }
\end{aligned}
\]} & DM54 & & 32 & 46 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & & 32 & 50 & \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: Icc is measured with all inputs grounded and all outputs open.
Note 4: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|c|}{\[
\begin{aligned}
& R_{\mathrm{L}}=400 \Omega \\
& \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}
\end{aligned}
\]} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & D to Q & & 25 & ns \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & D to Q & & 30 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & D to \(\overline{\mathrm{Q}}\) & & 15 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \(D\) to \(\bar{Q}\) & & 40 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & G to Q & & 15 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & G to Q & & 30 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & G to \(\overline{\mathbf{Q}}\) & & 15 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & G to \(\overline{\mathbf{Q}}\) & & 30 & ns \\
\hline
\end{tabular}

\section*{5476/DM5476/DM7476 \\ Dual Master-Slave J-K Flip-Flops with Clear, Preset, and Complementary Outputs}

\section*{General Description}

This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flop after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high the J and K inputs are disabled. On the negative transition of the clock, the data from the master is trans-

Connection Diagram


Order Number 5476DMQB, 5476FMQB, DM5476J, DM5476W or DM7476N
See NS Package Number J16A, N16E or W16A
ferred to the slave. The logic state of J and K inputs must not be allowed to change while the clock is high. The data is transfered to the outputs on the falling edge of the clock pulse. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

\section*{Features}
- Alternate Military/Aerospace device (5476) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Function Table}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multicolumn{5}{|c|}{Inputs} & \multicolumn{2}{|r|}{Outputs} \\
\hline PR & CLR & CLK & J & K & Q & \(\overline{\mathbf{Q}}\) \\
\hline L & H & X & X & X & H & L \\
\hline H & L & X & X & X & L & H \\
\hline L & L & X & X & X & \(\mathrm{H}^{*}\) & \(\mathrm{H}^{*}\) \\
\hline H & H & \(\Omega\) & L & L & Q & \(\bar{Q}_{0}\) \\
\hline H & H & \(\Omega\) & H & L & H & L \\
\hline H & H & \(\Omega\) & L & H & L & H \\
\hline H & H & \(\Omega\) & H & H & & \\
\hline
\end{tabular}

H = High Logic Level
L = Low Logic Level
\(X=\) Either Low or High Logic Level
\(\Omega=\) Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transfered to the outputs on the falling edge of the clock pulse.
* = This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.
\(Q_{0}=\) The output logic level before the indicated input conditions were established.
Toggle \(=\) Each output changes to the complement of its previous level on each complete active high level clock pulse.

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
5.5 V

Operating Free Air Temperature Range
DM54 and 54
DM74
\[
\begin{array}{r}
-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\
0^{\circ} \mathrm{C} \text { to }+70^{\circ} \mathrm{C}
\end{array}
\]
Storage Temperature Range

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM5476} & \multicolumn{3}{|c|}{DM7476} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
\hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & & & -0.4 & mA \\
\hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & & & 16 & mA \\
\hline fcLK & \multicolumn{2}{|l|}{Clock Frequency (Note 6)} & 0 & & 15 & 0 & & 15 & MHz \\
\hline \multirow[t]{4}{*}{tw} & \multirow[t]{4}{*}{Pulse Width (Note 6)} & Clock High & 20 & & & 20 & & & \multirow{4}{*}{ns} \\
\hline & & Clock Low & 47 & & & 47 & & & \\
\hline & & Preset Low & 25 & & & 25 & & & \\
\hline & & Clear Low & 25 & & & 25 & & & \\
\hline tsu & \multicolumn{2}{|l|}{Input Setup Time (Notes 1 \& 6)} & \(0 \uparrow\) & & & \(0 \uparrow\) & & & ns \\
\hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Input Hold Time (Notes 1 \& 6)} & 0 \(\downarrow\) & & & \(0 \downarrow\) & & & ns \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \begin{tabular}{l}
Typ \\
(Note 2)
\end{tabular} & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{4}{*}{\({ }_{1} \mathrm{H}\)} & \multirow[t]{4}{*}{High Level Input Current} & \multirow[t]{4}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
& \mathrm{~V}_{1}=2.4 \mathrm{~V}
\end{aligned}
\]} & J, K & & & 40 & \multirow{4}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Clock & & & 80 & \\
\hline & & & Clear & & & 80 & \\
\hline & & & Preset & & & 80 & \\
\hline \multirow[t]{4}{*}{IIL} & \multirow[t]{4}{*}{Low Level Input Current} & \multirow[t]{4}{*}{\[
\begin{gathered}
V_{C C}=M a x \\
V_{1}=0.4 V \\
(\text { Note } 5)
\end{gathered}
\]} & J, K & & & -1.6 & \multirow{4}{*}{mA} \\
\hline & & & Clock & & & -3.2 & \\
\hline & & & Clear & & & -3.2 & \\
\hline & & & Preset & & & -3.2 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=\text { Max } \\
& \text { (Note 3) }
\end{aligned}
\]} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline Icc & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}\) (Note 4)} & & 18 & 34 & mA \\
\hline
\end{tabular}

Note 1: The symbol ( \(\uparrow, \downarrow\) ) indicates the edge of the clock pulse is used for reference ( \(\uparrow\) ) for rising edge, ( \(\downarrow\) ) for falling edge.
Note 2: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 3: Not more than one output should be shorted at a time.
Note 4: With all outputs open, Icc is measured with the \(Q\) and \(\bar{Q}\) outputs high in turn. At the time of measurement the clock input is grounded.
Note 5: Clear is measured with preset high and preset is measured with clear high.
Note 6: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|c|}{\[
\begin{aligned}
& \mathrm{R}_{\mathrm{L}}=400 \Omega \\
& \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}
\end{aligned}
\]} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 15 & & MHz \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Preset to \(\bar{Q}\) & & 40 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Preset to Q & & 25 & ns \\
\hline tPHL & Propagation Delay Time High to Low Level Output & \[
\begin{aligned}
& \text { Clear } \\
& \text { to } Q
\end{aligned}
\] & & 40 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
\begin{aligned}
& \text { Clear } \\
& \text { to } \overline{\mathrm{Q}}
\end{aligned}
\] & & 25 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Q or \(\overline{\mathrm{Q}}\) & & 40 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \begin{tabular}{l}
Clock to \\
Q or \(\overline{\mathrm{Q}}\)
\end{tabular} & & 25 & ns \\
\hline
\end{tabular}

\section*{5483A}

\section*{4-Bit Binary Full Adder with Fast Carry}

\section*{General Description}

The '83A high speed 4-bit binary full adders with internal carry lookahead accept two 4-bit binary words ( \(\mathrm{A}_{0}-\mathrm{A}_{3}, \mathrm{~B}_{0}-\) \(\mathrm{B}_{3}\) ) and a Carry input ( \(\mathrm{C}_{0}\) ). They generate the binary Sum outputs \(\left(\mathrm{S}_{0}-\mathrm{S}_{3}\right)\) and the Carry output \(\left(\mathrm{C}_{4}\right)\) from the most
significant bit. They operate with either HIGH or active LOW operands (positive or negative logic). The '283 is recommended for new designs since it features standard corner power pins.

\section*{Connection Diagram}

\section*{Dual-In-LIne Package}


TL/F/9613-1
Order Number 5483ADMQB or 5483AFMQB
See NS Package Number J16A or W16A
\begin{tabular}{|l|l|}
\hline Pin Names & Description \\
\hline\(A_{0}-A_{3}\) & A Operand Inputs \\
\(B_{0}-B_{3}\) & B Operand Inputs \\
\(C_{0}\) & Carry Input \\
\(S_{0}-S_{3}\) & Sum Ouputs \\
\(C_{4}\) & Carry Ouput \\
\hline
\end{tabular}

\section*{Truth Table}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{} & \multicolumn{9}{|c|}{Inputs} & \multicolumn{5}{|c|}{Outputs} \\
\hline & \(\mathrm{C}_{0}\) & \(\mathrm{A}_{0}\) & \(\mathrm{A}_{1}\) & \(\mathrm{A}_{2}\) & \(\mathrm{A}_{3}\) & \(\mathrm{B}_{0}\) & \(\mathrm{B}_{1}\) & \(\mathrm{B}_{2}\) & \(\mathrm{B}_{3}\) & \(\mathrm{S}_{0}\) & \(\mathrm{S}_{1}\) & \(\mathrm{S}_{2}\) & \(\mathrm{S}_{3}\) & \(\mathrm{C}_{4}\) \\
\hline Logic Levels & L & L & H & L & H & H & L & L & H & H & H & L & L & H \\
\hline Active HIGH & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 1 \\
\hline Active LOW & 1 & 1 & 0 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 0 \\
\hline
\end{tabular}
\[
\begin{aligned}
& (10+9=19) \\
& (\text { carry }+5+6=12)
\end{aligned}
\]

\footnotetext{
H = HIGH Voltage Level
}
\(\mathrm{L}=\) LOW Voltage Level

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
\begin{tabular}{lr} 
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \\
DM54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{5483A} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & V \\
\hline \(\mathrm{IOH}^{\text {O}}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.8 & mA \\
\hline \multirow[t]{2}{*}{IOL} & \multirow[t]{2}{*}{Low Level Output Current} & \(\mathrm{S}_{\mathrm{n}}\) & & & 16 & \multirow[t]{2}{*}{mA} \\
\hline & & \(\mathrm{C}_{4}\) & & & 8 & \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) }
\end{gathered}
\] & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{Ios} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\operatorname{Max}\) (Note 2)} & Outputs & \(-20\) & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & \(\mathrm{C}_{4}\) & -20 & & -70 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & & 99 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics \(\mathrm{v}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\[
\begin{aligned}
& \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\
& \mathrm{R}_{\mathrm{L}}=400 \Omega \\
& \hline
\end{aligned}
\]} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \[
t_{\text {PLH }}
\]
\[
\mathrm{t}_{\mathrm{PHL}}
\] & Propagation Delay \(\mathrm{C}_{0}\) to \(\mathrm{S}_{\mathrm{n}}\) & & \[
\begin{aligned}
& 21 \\
& 21
\end{aligned}
\] & ns \\
\hline \(t_{\text {PLH }}\)
\[
\mathrm{t}_{\mathrm{PHL}}
\] & \begin{tabular}{l}
Propagation Delay \\
\(A_{n}\) or \(B_{n}\) to \(S_{n}\)
\end{tabular} & & \[
\begin{aligned}
& 24 \\
& 24 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay \(\mathrm{C}_{0}\) to \(\mathrm{C}_{4}\) & & \[
\begin{aligned}
& 14 \\
& 16 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}}
\end{aligned}
\] & \begin{tabular}{l}
Propagation Delay \\
\(A_{n}\) or \(B_{n}\) to \(C_{4}\)
\end{tabular} & & \[
\begin{aligned}
& 14 \\
& 16 \\
& \hline
\end{aligned}
\] & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The '83A adds two 4-bit binary words (A and B) plus the incoming carry. The binary sum appears on the sum outputs ( \(\mathrm{S}_{0}-\mathrm{S}_{3}\) ) and outgoing carry \(\left(\mathrm{C}_{4}\right)\) outputs.
\(C_{0}+\left(A_{0}+B_{0}\right)+2\left(A_{1}+B_{1}\right)+4\left(A_{2}+B_{2}\right)+8\left(A_{3}+\right.\) \(\left.B_{3}\right)=S_{0}+2 S_{1}+4 S_{2}+8 S_{3}+16 C_{4}\)

Where: \((+)=\) plus

Due to the symmetry of the binary add function the '83A can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry In can not be left open, but must be held LOW when no carry in is intended.
Interchanging inputs of equal weight does not affect the operation, thus \(\mathrm{C}_{0}, \mathrm{~A}_{0}, \mathrm{~B}_{0}\) can be arbitrarily assigned to pins \(10,11,13\), etc.

\section*{Logic Diagram}


TL/F/9613-3

\section*{5485/DM5485/DM7485 \\ 4-Bit Magnitude Comparators}

\section*{General Description}

These 4-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The \(A>B, A<B\), and \(A=B\) outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must
have a high-level voltage applied to the \(\mathrm{A}=\mathrm{B}\) input. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words.

\section*{Features}
- Typical power dissipation 275 mW
- Typical delay (4-bit words) 23 ns
© Alternate Military/Aerospace device (5485) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

\begin{tabular}{|c|c|}
\hline \multicolumn{2}{|l|}{Absolute Maximum Ratings (Note)} \\
\hline \multicolumn{2}{|l|}{please contact the National Semiconductor Sales Office/Distributors for availability and specifications.} \\
\hline Supply Voltage & V \\
\hline Input Voltage & 5.5 V \\
\hline Operating Free Air Temperature Range & \\
\hline DM54 and 54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ}\) \\
\hline DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
\hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to + \\
\hline
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5485} & \multicolumn{3}{|c|}{DM7485} & \multirow{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
(Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline V OH & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & & & V \\
\hline VOL & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & 0.4 & V \\
\hline 4 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{3}{*}{\(\mathrm{IIH}^{\text {H}}\)} & \multirow[t]{3}{*}{High Level Input Current} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=2.4 V
\end{aligned}
\]} & \(A<B\) & & & 40 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & \(A>B\) & & & 40 & \\
\hline & & & Others & & & 120 & \\
\hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{l}}=0.4 \mathrm{~V}
\end{aligned}
\]} & \(A<B\) & & & -1.6 & \multirow{3}{*}{mA} \\
\hline & & & A \(>\) B & & & -1.6 & \\
\hline & & & Others & & & -4.8 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=M a x
\] \\
(Note 2)
\end{tabular}} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline Icc & Supply Current & \multicolumn{2}{|l|}{\begin{tabular}{l}
\[
V_{C C}=M a x
\] \\
(Note 3)
\end{tabular}} & & 55 & 88 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: ICC is measured with all outputs open, \(\mathrm{A}=\mathrm{B}\) input grounded and all other inputs at 4.5 V .
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From Input} & \multirow[t]{2}{*}{To Output} & \multirow[t]{2}{*}{Number of Gate Levels} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{R}_{\mathrm{L}}=400 \Omega \\
& \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}
\end{aligned}
\]} & \multirow[t]{2}{*}{Units} \\
\hline & & & & & Min & Max & \\
\hline \multirow[t]{2}{*}{\(t_{\text {PLH }}\)} & \multirow[t]{2}{*}{Propagation Delay Time Low-to-High Level Output} & \multirow[t]{2}{*}{Any A or B Data Input} & \[
\begin{aligned}
& A<B \\
& A>B
\end{aligned}
\] & 3 & & 26 & \multirow[t]{2}{*}{ns} \\
\hline & & & \(A=B\) & 4 & & 35 & \\
\hline \multirow[t]{2}{*}{\({ }_{\text {tPHL }}\)} & \multirow[t]{2}{*}{Propagation Delay Time High-to-Low Level Output} & \multirow[t]{2}{*}{Any A or B Data Input} & \[
\begin{aligned}
& A<B \\
& A>B
\end{aligned}
\] & 3 & & 30 & \multirow[t]{2}{*}{ns} \\
\hline & & & \(A=B\) & 4 & & 30 & \\
\hline \({ }^{\text {PLLH }}\) & Propagation Delay Time Low-to-High Level Output & \[
\begin{gathered}
A<B \\
\text { or } A=B
\end{gathered}
\] & A \(>\) B & 1 & & 11 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High-to-Low Level Output & \[
\begin{gathered}
A<B \\
\text { or } A=B
\end{gathered}
\] & \(A>B\) & 1 & & 17 & ns \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low-to-High Level Output & \(A=B\) & \(A=B\) & 2 & & 20 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High-to-Low Level Output & \(A=B\) & \(A=B\) & 2 & & 17 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low-to-High Level Output & \[
\begin{gathered}
A>B \\
\text { or } A=B
\end{gathered}
\] & \(A<B\) & 1 & & 11 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High-to-Low Level Output & \[
\begin{gathered}
A>B \\
\text { or } A=B
\end{gathered}
\] & \(A<B\) & 1 & & 17 & ns \\
\hline
\end{tabular}

\section*{Function Table}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{4}{|c|}{Comparing Inputs} & \multicolumn{3}{|c|}{Cascading Inputs} & \multicolumn{3}{|c|}{Outputs} \\
\hline A3, B3 & A2, B2 & A1, B1 & A0, BO & A \(>\) B & A<B & \(\mathbf{A}=\mathbf{B}\) & A \(>\) B & A<B & \(A=B\) \\
\hline A3 \(>\) B3 & X & X & X & \(X\) & X & X & H & L & L \\
\hline A3 < B3 & X & X & X & X & X & X & L & H & L \\
\hline \(A 3=B 3\) & A2 > B2 & X & X & X & X & X & H & L & L \\
\hline \(\mathrm{A} 3=\mathrm{B} 3\) & \(\mathrm{A} 2<\mathrm{B} 2\) & X & X & X & X & X & L & H & L \\
\hline \(\mathrm{A} 3=\mathrm{B} 3\) & \(\mathrm{A} 2=\mathrm{B} 2\) & A1 > B1 & X & X & X & X & H & L & L \\
\hline \(\mathrm{A} 3=\mathrm{B} 3\) & \(\mathrm{A} 2=\mathrm{B} 2\) & \(A 1<B 1\) & X & X & X & X & L & H & L \\
\hline \(A 3=B 3\) & \(\mathrm{A} 2=\mathrm{B} 2\) & \(\mathrm{A} 1=\mathrm{B} 1\) & \(\mathrm{AO}>\mathrm{BO}\) & X & X & X & H & L & L \\
\hline \(A 3=B 3\) & \(\mathrm{A} 2=\mathrm{B} 2\) & \(\mathrm{A} 1=\mathrm{B} 1\) & \(\mathrm{AO}<\mathrm{BO}\) & X & X & X & L & H & L \\
\hline \(A 3=B 3\) & \(\mathrm{A} 2=\mathrm{B} 2\) & \(\mathrm{A} 1=\mathrm{B} 1\) & \(A 0=B 0\) & H & L & L & H & L & L \\
\hline \(A 3=B 3\) & \(\mathrm{A} 2=\mathrm{B} 2\) & \(A 1=B 1\) & \(A 0=B 0\) & L & H & L & L & H & L \\
\hline A3 \(=\) B3 & \(\mathrm{A} 2=\mathrm{B} 2\) & \(A 1=B 1\) & \(A 0=B 0\) & L & L & H & L & L & H \\
\hline A3 \(=\) B3 & \(\mathrm{A} 2=\mathrm{B} 2\) & \(A 1=B 1\) & \(A 0=B 0\) & X & X & H & L & L & H \\
\hline \(\mathrm{A} 3=\mathrm{B} 3\) & \(\mathrm{A} 2=\mathrm{B} 2\) & \(A 1=B 1\) & \(A 0=B 0\) & H & H & L & L & L & L \\
\hline \(\mathrm{A} 3=\mathrm{B} 3\) & \(\mathrm{A} 2=\mathrm{B} 2\) & \(\mathrm{A} 1=\mathrm{B} 1\) & \(A 0=B 0\) & L & L & L & H & H & L \\
\hline
\end{tabular}

\footnotetext{
\(H=\) High Level, L = Low Level, \(X=\) Don't Care
}

Logic Diagram


\section*{5486/DM5486/DM7486}

\section*{Quad 2-Input Exclusive-OR Gates}

\section*{General Description}

This device contains four independent gates each of which performs the logic exclusive-OR function.

\section*{Features}

■ Alternate Military/Aerospace device (5486) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Connection Diagram}


Order Number 5486DMQB, 5486FMQB, DM5486J, DM5486W or DM7486N See NS Package Number J14A, N14A or W14B

\section*{Function Table}
\begin{tabular}{|c|c|c|}
\multicolumn{3}{c|}{\(\mathbf{Y}=\mathbf{A} \oplus \mathbf{B}\)} \\
\hline \multicolumn{2}{|c|}{ Inputs } & Output \\
\hline \(\mathbf{A}\) & \(\mathbf{B}\) & \(\mathbf{Y}\) \\
\hline\(L\) & \(L\) & \(L\) \\
\(L\) & \(H\) & \(H\) \\
\(H\) & \(L\) & \(H\) \\
\(H\) & \(H\) & \(L\) \\
\hline
\end{tabular}
\(H=\) High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
7V
Input Voltage
5.5 V

Operating Free Air Temperature Range
\begin{tabular}{lr} 
DM54 and 54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM5486} & \multicolumn{3}{|c|}{DM7486} & \multirow{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics}
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
(Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\)} & & & \(-1.5\) & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\) Max, \(\mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=\operatorname{Max} \\
& (\text { Note 2) }
\end{aligned}
\]} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline \multirow[t]{2}{*}{ICCH} & \multirow[t]{2}{*}{Supply Current with Outputs High} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=M a x
\] \\
(Note 3)
\end{tabular}} & DM54 & & 30 & 43 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & & 30 & 50 & \\
\hline \(\mathrm{I}_{\text {CCL }}\) & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 4)} & & 36 & 57 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=\cdot 5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: I ICCH is measured with all outputs open, one input of each gate at 4.5V, and the other inputs grounded.
Note 4: ICCL is measured with all outputs open, and all inputs at ground.

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Conditions} & \multicolumn{2}{|c|}{\[
\begin{aligned}
& C_{L}=15 \mathrm{pF} \\
& R_{L}=400 \Omega \\
& \hline
\end{aligned}
\]} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline tplH & Propagation Delay Time Low to High Level Output & \multirow{2}{*}{Other Input Low} & & 23 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & & & 17 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \multirow[t]{2}{*}{Other Input High} & & 30 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & & & 22 & ns \\
\hline
\end{tabular}

\section*{5490/DM5490A/DM7490A, DM5493A/DM7493A Decade, and Binary Counters}

\section*{General Description}

Each of these monolithic counters contains four masterslave flip-flops and additional gating to provide a divide-bytwo counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 90A and divide-by-eight for the 93A.
All of these counters have a gated zero reset and the 90A also has gated set-to-nine inputs for use in BCD nine's complement applications.
To use their maximum count length (decade or four-bit binary ), the B input is connected to the \(\mathrm{Q}_{\mathrm{A}}\) output. The input count pulses are applied to input \(A\) and the outputs are as described in the appropriate truth table. A symmetrical di-vide-by-ten count can be obtained from the 90A counters by
connecting the \(Q_{D}\) output to the \(A\) input and applying the input count to the \(B\) input which gives a divide-by-ten square wave at output \(Q_{A}\).

\section*{Features}
- Typical power dissipation -90A 145 mW —93A 130 mW
- Count frequency 42 MHz
- Alternate Military/Aerospace device (5490) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Connection Diagrams}

\section*{Dual-In-LIne Package}


Order Number 5490DMQB, 5490FMQB, DM5490AJ, DM5490AW or DM7490AN See NS Package Number J14A, N14A or W14B

Dual-In-Line Package


TL/F/6533-2
Order Number DM5493AJ, DM5493AW or DM7493AN
See NS Package Number J14A, N14A or W14B

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
5.5 V

Operating Free Air Temperature Range
DM54 and 54
\(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
DM74 \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
Storage Temperature Range

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|r|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM5490A} & \multicolumn{3}{|c|}{DM7490A} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{IOH}^{\text {I }}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.8 & & & -0.8 & mA \\
\hline IOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & & & 16 & mA \\
\hline \multirow[t]{2}{*}{\(\mathrm{f}_{\mathrm{CLK}}\)} & \multirow[t]{2}{*}{Clock Frequency (Note 5)} & A & 0 & & 32 & 0 & & 32 & \multirow[t]{2}{*}{MHz} \\
\hline & & B & 0 & & 16 & 0 & & 16 & \\
\hline \multirow[t]{3}{*}{tw} & \multirow[t]{3}{*}{Pulse Width (Note 5)} & A & 15 & & & 15 & & & \multirow{3}{*}{ns} \\
\hline & & B & 30 & & & 30 & & & \\
\hline & & Reset & 15 & & & 15 & & & \\
\hline \(t_{\text {REL }}\) & \multicolumn{2}{|l|}{Reset Release Time (Note 5)} & 25 & & & 25 & & & ns \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{'90A Electrical Characteristics}
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
(Note 1) & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}(\text { Note } 4)
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{3}{*}{\({ }_{I H}\)} & \multirow[t]{3}{*}{High Level Input Current} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=2.7 V
\end{aligned}
\]} & A & & & 80 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Reset & & & 40 & \\
\hline & & & B & & & 120 & \\
\hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=0.4 V
\end{aligned}
\]} & A & & & -3.2 & \multirow{3}{*}{mA} \\
\hline & & & Reset & & & -1.6 & \\
\hline & & & B & & & -4.8 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& \text { (Note 2) }
\end{aligned}
\]} & DM54 & -20 & & -57 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -57 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}(\) Note 3)} & & 29 & 42 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: ICC is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5 V , and all other inputs grounded.
Note 4: \(Q_{A}\) outputs are tested at \(l_{O L}=\) Max plus the limit value of \(l_{I L}\) for the \(B\) input. This permits driving the \(B\) input while maintaining full fan-out capability.
Note 5: \(T_{A}=25^{\circ} \mathrm{C}\) and \(V_{C C}=5 \mathrm{~V}\).

\section*{'90A Switching Characteristics}
at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|c|}{\[
\begin{aligned}
& \mathrm{R}_{\mathrm{L}}=400 \Omega \\
& \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\
& \hline
\end{aligned}
\]} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \multirow[t]{2}{*}{\(\mathrm{f}_{\text {MAX }}\)} & \multirow[t]{2}{*}{Maximum Clock Frequency} & \(A\) to \(Q_{A}\) & 32 & & \multirow[t]{2}{*}{MHz} \\
\hline & & \(B\) to \(Q_{B}\) & 16 & & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & A to \(Q_{A}\) & & 16 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & A to \(Q_{A}\) & & 18 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \(A\) to \(Q_{D}\) & & 48 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & A to \(Q_{D}\) & & 50 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \(B\) to \(Q_{B}\) & & 16 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & \(B\) to \(Q_{B}\) & & 21 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \(B\) to \(Q_{C}\) & & 32 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & \(B\) to \(Q_{C}\) & & 35 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \(B\) to \(Q_{D}\) & & 32 & ns \\
\hline tPHL & Propagation Delay Time High to Low Level Output & \(B\) to \(Q_{D}\) & & 35 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & SET-9 to \(Q_{A}, Q_{D}\) & & 30 & ns \\
\hline tPHL & Propagation Delay Time High to Low Level Output & SET-9 to
\[
Q_{B}, Q_{C}
\] & & 40 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
SET-0 \\
Any Q
\end{tabular} & & 40 & ns \\
\hline
\end{tabular}

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|r|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM5493A} & \multicolumn{3}{|c|}{DM7493A} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{IOH}^{\text {l }}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.8 & & & -0.8 & mA \\
\hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & & & 16 & mA \\
\hline \multirow[t]{2}{*}{\({ }_{\text {f CLK }}\)} & \multirow[t]{2}{*}{Clock Frequency (Note 5)} & A & 0 & & 32 & 0 & & 32 & \multirow[t]{2}{*}{MHz} \\
\hline & & B & 0 & & 16 & 0 & & 16 & \\
\hline \multirow[t]{3}{*}{tw} & \multirow[t]{3}{*}{Pulse Width (Note 5)} & A & 15 & & & 15 & & & \multirow{3}{*}{ns} \\
\hline & & B & 30 & & & 30 & & & \\
\hline & & Reset & 15 & & & 15 & & & \\
\hline \(t_{\text {REL }}\) & \multicolumn{2}{|l|}{Reset Release Time (Note 5)} & 25 & & & 25 & & & ns \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{'93A Electrical Characteristics}
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) } \\
\hline
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{J}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}(\text { Note } 4)
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\) Max, \(\mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{3}{*}{\(\mathrm{IIH}^{\text {H}}\)} & \multirow[t]{3}{*}{High Level Input Current} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=2.4 V
\end{aligned}
\]} & Reset & & & 40 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & A & & & 80 & \\
\hline & & & B & & & 80 & \\
\hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=\operatorname{Max} \\
& V_{1}=0.4 V
\end{aligned}
\]} & Reset & & & -1.6 & \multirow{3}{*}{mA} \\
\hline & & & A & & & -3.2 & \\
\hline & & & B & & & -3.2 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& \text { (Note 2) }
\end{aligned}
\]} & DM54 & -20 & & -57 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -57 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}\) (Note 3)} & & 26 & 39 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: ICC is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5 V and all other inputs grounded.
Note 4: \(Q_{A}\) outputs are tested at \(I_{O L}=\) Max plus the limit value of \(I_{L L}\) for the \(B\) input. This permits driving the \(B\) input while maintaining full fan-out capability.
Note 5: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).


Function Tables (Note D)

90A
\(B C D\) Count Sequence
(See Note A)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Count} & \multicolumn{4}{|c|}{Outputs} \\
\hline & \(Q_{D}\) & \(Q_{C}\) & \(Q_{B}\) & \(Q_{\text {A }}\) \\
\hline 0 & L & L & L & L \\
\hline 1 & L & L & L & H \\
\hline 2 & L & L & H & L \\
\hline 3 & L & L & H & H \\
\hline 4 & L & H & L & L \\
\hline 5 & L & H & L & H \\
\hline 6 & L & H & H & L \\
\hline 7 & L & H & H & H \\
\hline 8 & H & L & L & L \\
\hline 9 & H & L & L & H \\
\hline
\end{tabular}

90A
BCD Bi-Quinary (5-2)
(See Note B)
\begin{tabular}{|c|cccc|}
\hline \multirow{2}{*}{ Count } & \multicolumn{4}{|c|}{ Outputs } \\
\cline { 2 - 5 } & \(\mathbf{Q}_{\mathbf{A}}\) & \(\mathbf{Q}_{\mathbf{D}}\) & \(\mathbf{Q}_{\mathbf{C}}\) & \(\mathbf{Q}_{\mathbf{B}}\) \\
\hline 0 & L & L & L & L \\
1 & L & L & L & H \\
2 & L & L & H & L \\
3 & L & L & H & H \\
4 & L & H & L & L \\
5 & H & L & L & L \\
6 & H & L & L & H \\
7 & H & L & H & L \\
8 & \(H\) & L & H & H \\
9 & H & H & L & L \\
\hline
\end{tabular}

93A
Count Sequence
(See Note C)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Count} & \multicolumn{4}{|c|}{Outputs} \\
\hline & \(\mathbf{Q}_{\mathbf{D}}\) & \(\mathrm{Q}_{\mathrm{C}}\) & \(\mathbf{Q}_{\mathbf{B}}\) & \(\mathbf{Q}_{\mathbf{A}}\) \\
\hline 0 & L & L & L & L \\
\hline 1 & L & L & L & H \\
\hline 2 & L & L & H & L \\
\hline 3 & L & L & H & H \\
\hline 4 & L & H & L & L \\
\hline 5 & L & H & L & H \\
\hline 6 & L & H & H & L \\
\hline 7 & L & H & H & H \\
\hline 8 & H & L & L & L \\
\hline 9 & H & L & L & H \\
\hline 10 & H & L & H & L \\
\hline 11 & H & L & H & H \\
\hline 12 & H & H & L & L \\
\hline 13 & H & H & L & H \\
\hline 14 & H & H & H & L \\
\hline 15 & H & H & H & H \\
\hline
\end{tabular}

90A
Reset/Count Function Table
\begin{tabular}{|cccc|cccc|}
\hline \multicolumn{4}{|c|}{ Reset Inputs } & \multicolumn{4}{c|}{ Outputs } \\
\hline R0(1) & R0(2) & R9(1) & R9(2) & \(\mathbf{Q}_{\mathbf{D}}\) & \(\mathbf{Q}_{\mathbf{C}}\) & \(\mathbf{Q}_{\mathbf{B}}\) & \(\mathbf{Q}_{\mathbf{A}}\) \\
\hline H & H & L & X & L & L & L & L \\
H & H & X & L & L & L & L & L \\
X & X & H & H & H & L & L & H \\
X & L & X & L & & COUNT & \\
L & X & L & X & & COUNT & \\
L & X & X & L & & COUNT & \\
X & L & L & X & & COUNT \\
\hline
\end{tabular}

93A
Reset/Count Function Table
\begin{tabular}{|cc|cccc|}
\hline \multicolumn{2}{|c|}{ Reset Inputs } & \multicolumn{4}{c|}{ Outputs } \\
\hline \(\mathbf{R O}(1)\) & \(\mathbf{R O}(2)\) & \(\mathbf{Q}_{\mathbf{D}}\) & \(\mathbf{Q}_{\mathbf{C}}\) & \(\mathbf{Q}_{\mathbf{B}}\) & \(\mathbf{Q}_{\mathbf{A}}\) \\
\hline H & H & L & L & L & L \\
L & X & & COUNT & \\
X & L & \multicolumn{4}{|c|}{ COUNT } \\
\hline
\end{tabular}

Note \(A\) : Output \(Q_{A}\) is connected to input \(B\) for \(B C D\) count.
Note \(B\) : Output \(Q_{D}\) is connected to input \(A\) for bi-quinary count.
Note C: Output \(Q_{A}\) is connected to input \(B\).
Note D: \(H=\) High Level, L = Low Level, \(X=\) Don't Care.

\section*{Logic Diagrams}


93A


TL/F/6533-4

The J and K inputs shown without connection are for reference only and are functionally at a high level.

\section*{5495A/DM7495}

\section*{4-Bit Parallel Access Shift Registers}

\section*{General Description}

These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation.

Parallel (broadside) load
Shift right (the direction \(Q_{A}\) toward \(Q_{D}\) )
Shift left (the direction \(Q_{D}\) toward \(Q_{A}\) )
Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.
Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the
mode control is high by connecting the output of each flipflop to the parallel input of the previous flip-flop ( \(Q_{D}\) to input C , etc.) and serial data is entered at input D . The clock input may be applied simultaneously to clock 1 and clock 2 if both modes can be clocked from the same source.
Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the truth table will also ensure that register contents are protected.

\section*{Features}
- Typical maximum clock frequency 36 MHz
n Typical power dissipation 250 mW

\section*{Connection Diagram}


TL/F/6534-1
Order Number 5495ADMQB, 5495AFMQB or DM7495N See NS Package Number J14A, N14A or W14B

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
7 V
Input Voltage
5.5 V

Operating Free Air Temperature Range
\(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
DM74
Storage Temperature Range

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{5495A} & \multicolumn{3}{|c|}{DM7495} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
\hline \({ }^{\mathrm{l}} \mathrm{H}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.8 & & & -0.8 & mA \\
\hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & & & 16 & mA \\
\hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 4)} & 0 & & 25 & 0 & & 25 & MHz \\
\hline tw & \multicolumn{2}{|l|}{Clock Pulse Width (Note 4)} & 15 & 11 & & 15 & & & ns \\
\hline tsu & \multicolumn{2}{|l|}{Data Setup Time (Note 4)} & 20 & 10 & & 20 & 10 & & ns \\
\hline \multirow[t]{2}{*}{ten} & \multirow[t]{2}{*}{Time to Enable Clock (Note 4)} & Clock 1 & 20 & & & 20 & & & ns \\
\hline & & Clock 2 & 15 & & & 15 & & & \\
\hline \(t_{H}\) & \multicolumn{2}{|l|}{Data Hold Time (Note 4)} & 0 & \(-10\) & & 0 & -10 & & ns \\
\hline \(\mathrm{t}_{\mathrm{IN}}\) & \multicolumn{2}{|l|}{Time to Inhibit Clock 1 or Clock 2 (Note 4)} & 10 & & & 10 & & & ns \\
\hline \(T_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{2}{*}{\({ }_{1 / H}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=2.4 V
\end{aligned}
\]} & Mode & & & 80 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Others & & & 40 & \\
\hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Max} \\
& V_{1}=0.4 \mathrm{~V}
\end{aligned}
\]} & Mode & & & -3.2 & \multirow[t]{2}{*}{mA} \\
\hline & & & Others & & & -1.6 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& (\text { Note 2) }
\end{aligned}
\]} & DM54 & -18 & & -57 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -57 & \\
\hline Icc & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\) (Note 3)} & & 50 & 75 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: \(I_{C C}\) is measured with all outputs and serial input open; \(A, B, C\), and \(D\) inputs grounded: Mode Control at 4.5 V : and a momentary 3 V , then ground, applied to both clock inputs.
Note 4: \(T_{A}=25^{\circ} \mathrm{C}\) and \(V_{C C}=5 \mathrm{~V}\).

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(f_{\text {MAX }}\) & Maximum Clock Frequency & & 25 & & MHz \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Output & & 35 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Output & & 35 & ns \\
\hline
\end{tabular}

Function Table
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{8}{|c|}{Inputs} & \multicolumn{4}{|c|}{Outputs} \\
\hline \multirow[t]{2}{*}{Mode Control} & \multicolumn{2}{|c|}{Clocks} & \multirow[t]{2}{*}{Serlal} & \multicolumn{4}{|c|}{Parallel} & \multirow[t]{2}{*}{\(\mathbf{Q}_{\mathbf{A}}\)} & \multirow[t]{2}{*}{\(Q_{B}\)} & \multirow[t]{2}{*}{\(Q_{C}\)} & \multirow[t]{2}{*}{\(Q_{D}\)} \\
\hline & 2(L) & 1(R) & & A & B & c & D & & & & \\
\hline H & H & X & X & X & X & X & X & \(Q_{A 0}\) & \(Q_{B 0}\) & \(Q_{\text {co }}\) & \(Q_{\text {DO }}\) \\
\hline H & \(\downarrow\) & X & X & a & b & c & d & a & b & c & d \\
\hline H & \(\downarrow\) & X & X & \(\mathrm{Q}_{\mathrm{B} \dagger}\) & \(Q_{C+}\) & \(Q_{D \dagger}\) & d & \(Q_{B n}\) & \(Q_{\text {cn }}\) & \(Q_{\text {Dn }}\) & d \\
\hline L & L & H & X & X & X & X & X & \(Q_{A 0}\) & \(Q_{B 0}\) & \(Q_{C 0}\) & \(Q_{\text {DO }}\) \\
\hline L & \(X\) & \(\downarrow\) & H & X & \(x\) & X & \(x\) & H & \(Q_{\text {An }}\) & \(Q_{B n}\) & \(Q_{C n}\) \\
\hline L & X & \(\downarrow\) & L & X & \(X\) & X & \(x\) & L & \(Q_{\text {An }}\) & \(Q_{B n}\) & \(Q_{C n}\) \\
\hline \(\uparrow\) & L & L & X & X & X & X & X & \(\mathrm{Q}_{\text {AO }}\) & \(Q_{B 0}\) & \(Q_{C 0}\) & \(Q_{D 0}\) \\
\hline \(\downarrow\) & L & L & X & X & X & X & X & \(Q_{\text {A0 }}\) & \(Q_{B 0}\) & \(Q_{\text {co }}\) & \(Q_{D 0}\) \\
\hline \(\downarrow\) & L & H & X & X & X & X & \(x\) & \(\mathrm{Q}_{\text {A0 }}\) & \(\mathrm{Q}_{\mathrm{BO}}\) & \(Q_{\text {co }}\) & \(Q_{D 0}\) \\
\hline \(\uparrow\) & H & L & X & X & X & X & X & \(Q_{A 0}\) & \(Q_{B 0}\) & \(Q_{\text {co }}\) & \(Q_{\text {DO }}\) \\
\hline \(\uparrow\) & H & H & X & X & X & X & X & \(\mathrm{Q}_{\text {AO }}\) & \(\mathrm{Q}_{\mathrm{BO}}\) & \(Q_{C 0}\) & \(Q_{D 0}\) \\
\hline
\end{tabular}
\(\dagger\) Shifting left requires external connection of \(Q_{B}\) to \(A, Q_{C}\) to \(B, Q_{D}\) to \(C\). Serial data is entered at input \(D\).
\(H=\) High Level (Steady State), L = Low Level (Steady State), \(X=\) Don't Care (Any input, including transitions)
\(\downarrow=\) Transition from high to low level, \(\uparrow=\) Transition from low to high level
\(a, b, c, d=\) The level of steady, state input at inputs \(A, B, C\), or \(D\), respectively.
\(Q_{A 0}, Q_{B 0}, Q_{C 0}, Q_{D 0}=\) The level of \(Q_{A}, Q_{B}, Q_{C}, Q_{D}\), respectively, before the indicated steady state input conditions were established.
\(Q_{A n}, Q_{B n}, Q_{C n}, Q_{D n}=\) The level of \(Q_{A}, Q_{B}, Q_{C}, Q_{D}\), respectively, before the most recent \(\downarrow\) transition of the clock.

\section*{Logic Diagram}


TL/F/6534-2

\section*{5497/DM7497 \\ Synchronous Modulo-64 Bit Rate Multiplier}

\section*{General Description}

The ' 97 contains a synchronous 6 -stage binary counter and six decoding gates that serve to gate the clock through to the output at a sub-multiple of the input frequency. The output pulse rate, relative to the clock frequency, is determined by signals applied to the Select (S0-S5) inputs. Both true and complement outputs are available, along with an enable input for each. A Count Enable input and a Terminal Count output are provided for cascading two or more packages. An asynchronous Master Reset input prevents counting and resets the counter.

\section*{Connection Diagram}

Dual-In-Line Package


\section*{Logic Symbol}


TL/F/9780-2
\(V_{C C}=\operatorname{Pin} 16\)
GND \(=\operatorname{Pin} 8\)

Order Number 5497DMQB, 5497FMQB or DM7497N See NS Package Number J16A, N16E or W16A
\begin{tabular}{|c|c|}
\hline Pin Names & Description \\
\hline S0-S5 & Rate Select Inputs \\
\hline \(\bar{E}_{Z}\) & \(\overline{\mathrm{O}}_{\mathrm{Z}}\) Enable Input (Active LOW) \\
\hline EY & OY Enable Input \\
\hline \(\overline{C E}\) & Count Enable Input (Active LOW) \\
\hline CP & Clock Pulse Input (Active Rising Edge) \\
\hline MR & Asynchronous Master Reset Input (Active HIGH) \\
\hline \(\bar{O}_{z}\) & Gated Clock Output (Active LOW) \\
\hline Oy & Complement Output (Active HIGH) \\
\hline TC & Terminal Count Output (Active LOW) \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{9}{|l|}{Absolute Maximum Ratings (Note)} \\
\hline \multicolumn{3}{|l|}{If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.} & \multicolumn{6}{|l|}{\multirow[t]{4}{*}{Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for acutual device operation.}} \\
\hline \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Supply Voltage}} & 7 V & & & & & & \\
\hline & & 5.5 V & & & & & & \\
\hline \begin{tabular}{l}
Operating 54 \\
DM74
\end{tabular} & Air Temperature Range & \(125^{\circ} \mathrm{C}\) & & & & & & \\
\hline \multicolumn{2}{|l|}{Storage Temperature Range \(\quad-65^{\circ} \mathrm{C}\)} & \(150^{\circ} \mathrm{C}\) & & & & & & \\
\hline \multicolumn{9}{|l|}{Recommended Operating Conditions} \\
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{5497} & \multicolumn{3}{|c|}{DM7497} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \({ }^{\mathrm{IOH}}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
\hline \(\mathrm{lOL}^{\text {l }}\) & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline \(\mathrm{t}_{\mathrm{s}}(\mathrm{L})\) & Setup Time LOW, \(\overline{\mathrm{CE}}\) to CP Rising & 25 & & & 25 & & & ns \\
\hline \(t_{h}(\mathrm{H})\) & Hold Time HIGH, \(\overline{\text { CE }}\) to CP Rising & 0 & & & 0 & & & ns \\
\hline \(t_{\text {h }}(\mathrm{L})\) & Hold Time LOW, \(\overline{\text { CE }}\) to CP Falling & 0 & & & 0 & & & ns \\
\hline \(\mathrm{t}_{\mathrm{w}}(\mathrm{H})\) & CP Pulse Width HIGH & 20 & & & 20 & & & ns \\
\hline \(t_{w}(\mathrm{~L})\) & CP Pulse Width LOW & 20 & & & & & & ns \\
\hline \(\mathrm{t}_{\mathrm{w}}(\mathrm{H})\) & MR Pulse Width HIGH & 15 & & & 15 & & & ns \\
\hline
\end{tabular}

Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \begin{tabular}{l}
Typ \\
(Note 1)
\end{tabular} & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline V OH & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{2}{*}{\({ }_{1} \mathrm{H}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=\operatorname{Max}, V_{1}=2.4 V
\] \\
Clock Inputs
\end{tabular}} & DM74 & & & 40 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & 54 & & & 80 & \\
\hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=M a x, V_{1}=0.4 V
\] \\
Clock Inputs
\end{tabular}} & DM74 & & & -1.6 & \multirow[t]{2}{*}{mA} \\
\hline & & & 54 & & & -3.2 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=\text { Max } \\
& (\text { Note 2) }
\end{aligned}
\]} & 54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline \({ }^{\text {ICC }}\) & Supply Current With Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}\)} & & & 120 & mA \\
\hline
\end{tabular}

\section*{Switching Characteristics}
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow{3}{*}{Symboi} & \multirow{3}{*}{Parameter} & \multicolumn{2}{|c|}{5497} & \multicolumn{2}{|c|}{DM7497} & \multirow{3}{*}{Units} \\
\hline & & \multicolumn{2}{|c|}{\[
\begin{aligned}
& C_{L}=15 \mathrm{pF} \\
& R_{\mathrm{L}}=400 \Omega
\end{aligned}
\]} & \multicolumn{2}{|c|}{\[
\begin{aligned}
& C_{\mathrm{L}}=15 \mathrm{pF} \\
& \mathrm{R}_{\mathrm{L}}=400 \Omega
\end{aligned}
\]} & \\
\hline & & Min & Max & Min & Max & \\
\hline \(f_{\text {max }}\) & Maximum Clock Frequency & 25 & & 25 & & MHz \\
\hline \begin{tabular}{l}
\(t_{\text {PLH }}\) \\
\(\mathrm{t}_{\mathrm{PHL}}\)
\end{tabular} & Propagation Delay \(\bar{E}_{Z}\) to \(\bar{O}_{Z}\) & & \[
\begin{array}{r}
18 \\
23 \\
\hline
\end{array}
\] & & \[
\begin{aligned}
& 18 \\
& 23 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay \(\mathrm{E}_{\mathrm{Z}}\) to \(\mathrm{O}_{\mathrm{Y}}\) & & \[
\begin{array}{r}
30 \\
33 \\
\hline
\end{array}
\] & & \[
\begin{array}{r}
30 \\
33 \\
\hline
\end{array}
\] & ns \\
\hline \begin{tabular}{l}
\(t_{\text {PLH }}\) \\
\(t_{\text {PHL }}\)
\end{tabular} & Propagation Delay Ey to OY & & \[
\begin{aligned}
& 14 \\
& 10 \\
& \hline
\end{aligned}
\] & & \[
\begin{array}{r}
14 \\
10 \\
\hline
\end{array}
\] & ns \\
\hline tpLH
\(t_{\text {PHL }}\) & Propagation Delay \(\mathrm{S}_{\mathrm{n}}\) to \(\mathrm{O}_{\mathrm{Y}}\) & & \[
\begin{aligned}
& 23 \\
& 23 \\
& \hline
\end{aligned}
\] & & \[
\begin{aligned}
& 23 \\
& 23 \\
& \hline
\end{aligned}
\] & ns \\
\hline \(t_{\text {tp }}\) \(t_{\text {PHL }}\) & Propagation Delay \(\mathrm{S}_{\mathrm{n}}\) to \(\overline{\mathrm{O}}_{\mathrm{Z}}\) & & \[
\begin{aligned}
& 14 \\
& 14
\end{aligned}
\] & & \[
\begin{aligned}
& 14 \\
& 14
\end{aligned}
\] & ns \\
\hline \begin{tabular}{l}
\({ }^{\text {tpLH }}\) \\
\(t_{\text {PHL }}\)
\end{tabular} & Propagation Delay CP to OY & & \[
\begin{aligned}
& 39 \\
& 30
\end{aligned}
\] & & \[
\begin{aligned}
& 39 \\
& 30
\end{aligned}
\] & ns \\
\hline \begin{tabular}{l}
\(t_{\text {PLH }}\) \\
\(t_{\text {PHL }}\)
\end{tabular} & Propagation Delay CP to \(\mathrm{O}_{\mathrm{z}}\) & & \[
\begin{array}{r}
18 \\
26 \\
\hline
\end{array}
\] & & \[
\begin{array}{r}
18 \\
26 \\
\hline
\end{array}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay CP to TC & & \[
\begin{aligned}
& 35 \\
& 33 \\
& \hline
\end{aligned}
\] & & \[
\begin{aligned}
& 30 \\
& 33 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay \(\overline{\mathrm{CE}}\) to \(\overline{\mathrm{TC}}\) & & \[
\begin{aligned}
& 25 \\
& 21 \\
& \hline
\end{aligned}
\] & & \[
\begin{aligned}
& 20 \\
& 21 \\
& \hline
\end{aligned}
\] & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay MR to \(\mathrm{O}_{\mathrm{Y}}\) & & 43 & & 36 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay MR to \(\overline{\mathrm{O}}_{\mathrm{Z}}\) & & 34 & & 23 & ns \\
\hline
\end{tabular}

\section*{Timing Diagrams}



TL/F/9780-6

\section*{Functional Description}

The '97 contains six JK flip-flops connected as a synchronous modulo-64 binary counter. A LOW signal on the Count Enable ( \(\overline{\mathrm{CE}}\) ) input permits counting, with all state changes initiated simultaneously by the rising edge of the clock. When the count reaches maximum (63), with all Qs HIGH, the Terminal Count ( \(\overline{\mathrm{TC}}\) ) output will be LOW if \(\overline{\mathrm{CE}}\) is LOW. A HIGH signal on Master Reset (MR) resets the flip-flops and prevents counting, although output pulses can still occur if the clock is running, \(\bar{E}_{Z}\) is LOW and S5 is HIGH.
The flip-flop outputs are decoded by a 6 -wide AND-OR-INVERT gate. Each AND gate also contains the buffered and inverted \(C P\) and \(Z\)-enable ( \(\bar{E}_{Z}\) ) functions, as well as one of the Select ( \(\mathrm{S} 0-\mathrm{S} 5\) ) inputs. The Z output, \(\overline{\mathrm{O}}_{\mathrm{Z}}\) is normally HIGH and goes LOW when CP and \(\bar{E}_{Z}\) are LOW and any of the AND gates has its other inputs HIGH. The AND gates are enabled by the counter at different times and different rates relative to the clock. For example, the gate to which S5 is connected is enabled during every other clock period, assuming S5 is HIGH. Thus, during one complete cycle of the counter ( 64 clocks) the S 5 gate is enabled 32 times and can therefore gate 32 clocks per cycle to the output. The S4 gate is enabled 16 times per cycle, the S3 gate 8 times per cycle, etc. The output pulse rate thus depends on the clock rate and which of the SO-S5 inputs is HIGH.
\[
\begin{gathered}
f_{\text {out }}=\frac{m}{64} \bullet f_{\text {in }} \\
\text { Where: } m=S 5 \bullet 2^{5}+S 4 \bullet 2^{4}+S 3 \bullet 2_{3}+S 2 \bullet 2^{2}+S 1 \\
\bullet 2^{1}+S 0 \bullet 2^{0}
\end{gathered}
\]

Thus by appropriate choice of signals applied to the S0-S5 inputs, the output pulse rate can range from \(1 / 64\) to \(63 / 64\) of the clock rate, as suggested in Rate Select Table. There is no output pulse when the counter is in the "all ones" condition. When \(m\) is \(1,2,4,8,16\) or 32, the output pulses are evenly spaced, assuming that the clock frequency is constant. For any other value of \(m\) the output pulses are not evenly spaced, since the pulse train is formed by interleav-
ing pulses passed by two or more of the AND gates. The Pulse Pattern Table indicates the output pattern for several values of m . In each row, a one means that the \(\overline{\mathrm{O}}_{\mathrm{Z}}\) output will be HIGH during that entire clock period, while a zero means that \(\overline{\mathrm{O}}_{\mathrm{Z}}\) will be LOW when the clock is LOW in that period. The first column in the output field coincides with the "all zeroes" condition of the counter, while the last column represents the "all ones" condition. The pulse pattern for any particular value of m can be deduced by factoring it into the sum of appropriate powers of two (e.g. \(19=16+2+\) 1) and combining the pulses (i.e., the zeroes) shown for each for the relevant powers of two (e.g. for \(m=16,2\) and 1).

The \(Y\) output \(O_{Y}\) is the complement of \(\bar{O}_{Z}\) and is thus normally LOW. A LOW signal on the \(Y\)-enable input, EY, disables \(\mathrm{O}_{\mathrm{y}}\). To expand the multiplier to 12 -bit rate select, two packages can be cascaded as shown in Figure A. Both circuits operate from the basic clock, with the TC output of the first acting to enable both counting and the output pulses of the second package. Thus the second counter advances at only \(1 / 64\) the rate of the first and a full cycle of the two counters combined requires 4096 clocks. Each rate select input of the first package has 64 times the weight of its counterpart in the second package.
\[
\begin{gathered}
\mathrm{f}_{\text {out }}=\frac{\mathrm{m}_{1}+\mathrm{m}_{2}}{64 \bullet 64} \cdot \mathrm{f}_{\text {in }} \\
\text { Where: } \mathrm{m}_{1}=\mathrm{S} 5 \bullet 2^{11}+\mathrm{S} 4 \bullet 2^{10}+\mathrm{S} 3 \bullet 2^{9}+\mathrm{S} 2 \bullet 2^{8}+ \\
\mathrm{S} 1 \cdot 2^{7}+\mathrm{S} 0 \cdot 2^{6} \text { (first package) } \\
\mathrm{m}_{2}=\mathrm{S} 5 \cdot 2^{5}+\mathrm{S} 4 \cdot 2^{4}+\mathrm{S} 3 \cdot 2^{3}+\mathrm{S} 2 \cdot 2_{2}+ \\
\mathrm{S} 1 \cdot 2^{1}+\mathrm{S} 0 \cdot 2^{0} \text { (second package) }
\end{gathered}
\]

Combined output pulses are obtained in Figure \(A\) by letting the Z output of the first circuit act as the Y -enable function for the second, with the interleaved pulses obtained from the \(Y\) output of the second package being opposite in phase to the clock.


FIGURE A. Cascading for 12-Bit Rate Select

Functional Description (Continued)
Mode and Rate Select Table (Note 1)
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{9}{|c|}{Inputs} & \multirow[t]{2}{*}{\begin{tabular}{l}
Clock \\
Pulses
\end{tabular}} & \multicolumn{4}{|c|}{Outputs} & \multirow[t]{2}{*}{Notes} \\
\hline MR & \(\overline{C E}\) & \(\bar{E}_{\mathbf{z}}\) & S5 & S4 & S3 & S 2 & S1 & So & & Ey & OY & \(\mathrm{O}_{\mathrm{z}}\) & \(\overline{\text { TC }}\) & \\
\hline H & X & H & X & X & X & X & X & X & X & H & L & H & H & 2 \\
\hline L & \(L\) & L & L & L & L & L & L & L & 64 & H & L & H & 1 & 3 \\
\hline L & L & L & L & L & L & L & L & H & 64 & H & 1 & 1 & 1 & 3 \\
\hline L & L & L & L & L & L & L & H & L & 64 & H & 2 & 2 & 1 & 3 \\
\hline L & \(L\) & L & L & L & L & H & L & L & 64 & H & 4 & 4 & 1 & 3 \\
\hline L & L & L & L & L & H & L & L & L & 64 & H & 8 & 8 & 1 & 3 \\
\hline \(L\) & L & L & L & H & L & L & L & L & 64 & H & 16 & 16 & 1 & 3 \\
\hline L & L & L & H & L & L & L & L & L & 64 & H & 32 & 32 & 1 & 3 \\
\hline L & L & \(L\) & H & H & H & H & H & H & 64 & H & 63 & 62 & 1 & 3 \\
\hline L & L & L & H & H & H & H & H & H & 64 & L & H & 63 & 1 & 4 \\
\hline L & L & L & H & L & L & L & L & L & 64 & H & 40 & 40 & 1 & 5 \\
\hline
\end{tabular}
\(H=H I G H\) Voltage Level
\(L=\) LOW Voltage Level
\(X=\) Immaterial
Note 1: Numerals indicate number of pulses per cycle.
Note 2: This is a simplified illustration of the clear function. CP and \(\bar{E}_{Z}\) also affect the logic level of \(O_{Y}\) and \(\bar{O}_{Z}\). A LOW signal on EY will cause \(O_{Y}\) to remain HIGH.
Note 3: Each rate illustrated assumes S0-S5 are constant throughout the cycle; however, these illustrations in no way prohibit variablerate operation.
Note 4: \(\mathrm{E}_{\mathrm{Y}}\) is used to inhibit output Y .
Note 5: \(f_{\text {out }}=m \bullet \frac{f_{\text {in }}}{64}=\frac{(32+8) f_{\text {in }}}{64}=\frac{40 f_{\text {in }}}{64}=0.625 f_{\text {in }}\)

Pulse Pattern Table
\begin{tabular}{|c|c|}
\hline m & Output Pulse Pattern at \(\overline{\mathbf{O}}_{\mathbf{z}}\) \\
\hline 1 & 11111111111111111111111111111110111111111111111111111111111111 \\
\hline 2 & 1111111111111110111111111111111111111111111111101111111111111111 \\
\hline 3 & 1111111111111110111111111111111011111111111111101111111111111111 \\
\hline 4 & 1111111011111111111111101111111111111110111111111111111011111111 \\
\hline 5 & 1111111011111111111111101111111011111110111111111111111011111111 \\
\hline 6 & 1111111011111110111111101111111111111110111111101111111011111111 \\
\hline 8 & 1110111111101111111011111110111111101111111011111110111111101111 \\
\hline 10 & 1110111111101111111011111110111111101111111011101110111111101111 \\
\hline 12 & 1110111011101111111011101110111111101110111011111110111011101111 \\
\hline 14 & 1110111011101110111011101110111111101110111011101110111011101111 \\
\hline 16 & 1011101110111011101110111011101110111011101110111011101110111011 \\
\hline 20 & 1011101010111011101110101011101110111010101110111011101110111011 \\
\hline 24 & 1010101110101011101010111010101110101011111010111010101110101011 \\
\hline 28 & 1010101010101011101010101010101110101010101010111010101010101011 \\
\hline 32 & \(010101 \ldots\). . 0101 \\
\hline
\end{tabular}


TL/F/9780-4

\section*{DM54107 Dual Master-Slave J-K Flip-Flops with Clear and Complementary Outputs}

\section*{General Description}

This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high the J and K inputs are disabled. On the nega-
tive transition of the clock, the data from the master is transferred to the slave. The logic states of the J and K inputs must not be allowed to change while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse. A low logic level on the clear input will reset the output regardless of the logic states of the other inputs.

\section*{Connection Diagram}

Dual-In-Line Package


Order Number DM54107J
See NS Package Number J14A
Function Table
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multicolumn{4}{|c|}{ Inputs } & \multicolumn{2}{c|}{ Outputs } \\
\hline CLR & CLK & J & K & Q & \(\overline{\mathbf{Q}}\) \\
\hline L & X & X & X & L & \(H\) \\
\(H\) & \(\Omega\) & \(L\) & \(L\) & \(Q_{0}\) & \(\bar{Q}_{0}\) \\
\(H\) & \(\Omega\) & \(H\) & \(L\) & \(H\) & \(L\) \\
\(H\) & \(\Omega\) & \(L\) & \(H\) & \(L\) & \(H\) \\
\cline { 5 - 7 } & H & L & \(H\) & \(H\) & \multicolumn{2}{|c|}{ Toggle } \\
\hline
\end{tabular}
\(H=\) High Logic Level
X = Either Low or High Logic Level
L = Low Logic Level
\(\Omega\) = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.
\(Q_{0}=\) The output logic level of \(Q\) before the indicated input conditions were established.

Toggle \(=\) Each output changes to the complement of its previous level on each complete positive clock pulse.

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
\begin{tabular}{lr} 
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \\
DM54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54107} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & V \\
\hline \(\mathrm{IOH}^{\mathrm{l}}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & mA \\
\hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & mA \\
\hline fCLK & \multicolumn{2}{|l|}{Clock Frequency (Note 5)} & 0 & 20 & 15 & MHz \\
\hline \multirow[t]{3}{*}{tw} & \multirow[t]{3}{*}{Pulse Width (Note 5)} & Clock High & 20 & & & \multirow{3}{*}{ns} \\
\hline & & Clock Low & 47 & & & \\
\hline & & Clear Low & 25 & & & \\
\hline tsu & \multicolumn{2}{|l|}{Input Setup Time (Notes 1 \& 5)} & \(0 \uparrow\) & & & ns \\
\hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Input Hold Time (Notes 1 \& 5)} & 0 \(\downarrow\) & & & ns \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 2) } \\
\hline
\end{gathered}
\] & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{3}{*}{\(\mathrm{IIH}^{\text {H}}\)} & \multirow[t]{3}{*}{High Level Input Current} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=2.4 V
\end{aligned}
\]} & J, K & & & 40 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Clock & & & 80 & \\
\hline & & & Clear & & & 80 & \\
\hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=0.4 V
\end{aligned}
\]} & J, K & & & -1.6 & \multirow{3}{*}{mA} \\
\hline & & & Clock & & & -3.2 & \\
\hline & & & Clear & & & -3.2 & \\
\hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 3)} & -20 & & -55 & mA \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\) Max, (Note 4)} & & 18 & 34 & mA \\
\hline
\end{tabular}

Note 1: The symbols \((\uparrow, \downarrow)\) indicate the edge of the clock pulse is used for reference: \((\uparrow)\) for rising edge, \((\downarrow)\) for falling edge.
Note 2: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 3: Not more than one output should be shorted at a time.
Note 4: With all outputs open, Icc is measured with the \(Q\) and \(\bar{Q}\) outputs high in turn. At the time of measurement the clock input is grounded.
Note 5: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|c|}{\[
\begin{aligned}
& \mathrm{R}_{\mathrm{L}}=400 \Omega \\
& \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}
\end{aligned}
\]} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 15 & & MHz \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
Clear \\
to Q
\end{tabular} & & 40 & ns \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & \[
\begin{aligned}
& \text { Clear } \\
& \text { to } \bar{Q}
\end{aligned}
\] & & 25 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Q or \(\bar{Q}\) & & 40 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Q or \(\bar{Q}\) & & 25 & ns \\
\hline
\end{tabular}

\section*{DM54109 Dual Positive-Edge-Triggered J-K Flip-Flops with Preset, Clear, and Complementary Outputs}

\section*{General Description}

This device contains two independent positive-edge-triggered J-K flip-flops with complementary outputs. The J and \(\overline{\mathrm{K}}\) data is accepted by the flip-flop on the rising edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of
the clock. The data on the \(J\) and \(\bar{K}\) inputs may be changed while the clock is high or low as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

\section*{Connection Diagram}


Function Table
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multicolumn{5}{|c|}{Inputs} & \multicolumn{2}{|r|}{Outputs} \\
\hline PR & CLR & CLK & J & \(\overline{\mathbf{K}}\) & Q & \(\overline{\mathbf{Q}}\) \\
\hline L & H & X & X & X & H & L \\
\hline H & L & X & X & X & L & H \\
\hline L & L & X & X & X & \(\mathrm{H}^{*}\) & \(\mathrm{H}^{*}\) \\
\hline H & H & 「 & L & L & L & H \\
\hline H & H & \(\uparrow\) & H & L & & \\
\hline H & H & \(\uparrow\) & L & H & Q & \(\bar{Q}_{0}\) \\
\hline H & H & \(\uparrow\) & H & H & H & L \\
\hline H & H & L & X & X & \(Q_{0}\) & \(\bar{Q}_{0}\) \\
\hline
\end{tabular}
\(H=\) High Logic Level
L = Low Logic Level
\(\uparrow=\) Rising Edge of Pulse.
* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.
\(Q_{0}=\) The output logic level of \(Q\) before the indicated input conditions were established.
Toggle \(=\) Each output changes to the complement of its previous level on each active transition of the clock pulse.
\begin{tabular}{lr} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM54 & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54109} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & \\
\hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & V \\
\hline \(V_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & V \\
\hline \(\mathrm{IOH}^{2}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -1.2 & mA \\
\hline \(\mathrm{lOL}^{2}\) & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & mA \\
\hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 6)} & 0 & & 30 & MHz \\
\hline \multirow[t]{4}{*}{\(t_{W}\)} & \multirow[t]{4}{*}{Pulse Width (Note 6)} & Clock High & 20 & & & \multirow{4}{*}{ns} \\
\hline & & Clock Low & 20 & & & \\
\hline & & Preset Low & 20 & & & \\
\hline & & Clear Low & 20 & & & \\
\hline tsu & \multicolumn{2}{|l|}{Input Setup Time (Notes 1 \& 6)} & \(15 \uparrow\) & & & ns \\
\hline \(t_{H}\) & \multicolumn{2}{|l|}{Input Hold Time (Notes 1 \& 6)} & \(10 \downarrow\) & & & ns \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unloss otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \begin{tabular}{l}
Typ \\
(Note 2)
\end{tabular} & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{I}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOH}_{\mathrm{OH}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{4}{*}{\(\mathrm{IIH}^{\text {H }}\)} & \multirow[t]{4}{*}{High Level Input Current} & \multirow[t]{4}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=2.4 V
\end{aligned}
\]} & J, \(\overline{\mathrm{K}}\) & & & 40 & \multirow{4}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Preset & & & 80 & \\
\hline & & & Clock & & & 80 & \\
\hline & & & Clear & & & 160 & \\
\hline \multirow[t]{4}{*}{IIL} & \multirow[t]{4}{*}{Low Level Input Current} & \multirow[t]{4}{*}{\[
\begin{gathered}
\mathrm{V}_{\mathrm{cc}}=\operatorname{Max} \\
\mathrm{V}_{1}=0.4 \mathrm{~V} \\
(\text { Note } 5)
\end{gathered}
\]} & J, \(\overline{\mathrm{K}}\) & & & -1.6 & \multirow{4}{*}{mA} \\
\hline & & & Preset & & & -3.2 & \\
\hline & & & Clock & & & -3.2 & \\
\hline & & & Clear & & & -4.8 & \\
\hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\operatorname{Max}(\) Note 3)} & -30 & & -85 & mA \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 4)} & & 20 & 30 & mA \\
\hline
\end{tabular}

Note 1: The symbol ( \(\uparrow\) ) indicates the rising edge of the clock pulse is used for reference.
Note 2: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 3: Not more than one output should be shorted at a time.
Note 4: With all outputs open, lCC is measured with the \(Q\) and \(\bar{Q}\) outputs high in turn. At the time of measurement the clock input grounded.
Note 5: Clear is tested with preset high and preset is tested with clear high.
Note 6: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|c|}{\[
\begin{aligned}
& R_{\mathrm{L}}=400 \Omega \\
& C_{\mathrm{L}}=15 \mathrm{pF}
\end{aligned}
\]} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 30 & & MHz \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Preset to Q & & 14 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Preset to \(\bar{Q}\) & & 29 & ns \\
\hline tplH & Propagation Delay Time Low to High Level Output & \[
\begin{aligned}
& \text { Clear } \\
& \text { to } \bar{Q}
\end{aligned}
\] & & 14 & ns \\
\hline \(\mathrm{t}_{\mathrm{PHL}}\) & Propagation Delay Time High to Low Level Output & \[
\begin{aligned}
& \text { Clear } \\
& \text { to } \mathrm{Q}
\end{aligned}
\] & & 25 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Q or \(\bar{Q}\) & & 18 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Qor \(\bar{Q}\) & & 28 & ns \\
\hline
\end{tabular}

\section*{54121/DM54121/DM74121 One-Shot with Clear and Complementary Outputs}

\section*{General Description}

The DM54/74121 is a monostable multivibrator featuring both positive and negative edge triggering with complementary outputs. An internal \(2 \mathrm{k} \Omega\) timing resistor is provided for design convenience minimizing component count and layout problems. This device can be used with a single external capacitor. Inputs (A) are active-low trigger transition inputs and input ( B ) is an active-high transition Schmitt-trigger input that allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second. A high immunity to \(\mathrm{V}_{\mathrm{cc}}\) noise of typically 1.5 V is also provided by internal circuitry at the input stage.
To obtain optimum and trouble free operation please read operating rules and NSC one-shot application notes carefully and observe recommendations.

\section*{Features}
- Triggered from active-high transition or active-low transition inputs
- Variable pulse width from 30 ns to 28 seconds
- Jitter free Schmitt-trigger input
- Excellent noise immunity typically 1.2 V
- Stable pulse width up to \(90 \%\) duty cycle
- TTL, DTL compatible
- Compensated for \(V_{C C}\) and temperature variations
- Input clamp diodes
- Alternate Military/Aerospace device (54121) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

\section*{Functional Description}

The basic output pulse width is determined by selection of an internal resistor \(\mathrm{R}_{\text {INT }}\) or an external resistor ( \(\mathrm{R}_{\mathrm{X}}\) ) and capacitor ( \(\mathrm{C}_{\mathrm{X}}\) ). Once triggered the output pulse width is independent of further transitions of the inputs and is a function of the timing components. Pulse width can vary from a few nano-seconds to 28 seconds by choosing appropriate \(R_{X}\) and \(C_{X}\) combinations. There are three trigger inputs from the device, two negative edge-triggering (A) inputs, one positive edge Schmitt-triggering (B) input.

\section*{Function Table}
\begin{tabular}{|c|c|c|c|c|}
\hline \multicolumn{3}{|c|}{ Inputs } & \multicolumn{3}{c|}{ Outputs } \\
\hline A1 & A2 & B & Q & \(\overline{\mathbf{Q}}\) \\
\hline L & X & H & L & H \\
X & L & H & L & H \\
X & X & L & L & H \\
H & H & X & L & H \\
H & \(\downarrow\) & H & \(\Omega\) & U \\
\(\downarrow\) & H & H & \(\Omega\) & U \\
\(\downarrow\) & \(\downarrow\) & H & \(\Omega\) & U \\
L & X & \(\uparrow\) & \(\Omega\) & I \\
X & L & \(\uparrow\) & \(\Omega\) & U \\
\hline
\end{tabular}

H = High Logic Level
L = Low Logic Level
X = Can Be Either Low or High
\(\uparrow=\) Positive Going Transition
\(\downarrow=\) Negative Going Transition
\(\Omega=A\) Positive Pulse
U = A Negative Pulse

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage 7V
Input Voltage 5.5 V

Operating Free Air Temperature Range
DM54
\(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
\(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
Storage Temperature Range
\(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54121} & \multicolumn{3}{|c|}{DM74121} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\text {CC }}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{T}+}\) & \multicolumn{2}{|l|}{Positive-Going Input Threshold Voltage at the A Input ( \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}\) )} & & 1.4 & 2 & & 1.4 & 2 & V \\
\hline \(\mathrm{V}_{\mathrm{T}-}\) & \multicolumn{2}{|l|}{Negative-Going Input Threshold Voltage at the A Input ( \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}\) )} & 0.8 & 1.4 & & 0.8 & 1.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{T}+}\) & \multicolumn{2}{|l|}{Positive-Going Input Threshold Voltage at the B Input ( \(V_{\mathrm{CC}}=\mathrm{Min}\) )} & & 1.5 & 2 & & 1.5 & 2 & V \\
\hline \(\mathrm{V}_{\mathrm{T}-}\) & \multicolumn{2}{|l|}{Negative-Going Input Threshold Voltage at the B Input ( \(\left.V_{C C}=\mathrm{Min}\right)\)} & 0.8 & 1.3 & & 0.8 & 1.3 & & V \\
\hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & & & -0.4 & mA \\
\hline \(\mathrm{lOL}^{\text {l }}\) & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & & & 16 & mA \\
\hline tw & \multicolumn{2}{|l|}{Input Pulse Width (Note 1)} & 40 & & & 40 & & & ns \\
\hline dV/dt & \multicolumn{2}{|l|}{Rate of Rise or Fall of Schmidt Input (B) (Note 1)} & & & 1 & & & 1 & V/s \\
\hline dV/dt & \multicolumn{2}{|l|}{Rate of Rise or Fall of Logic Input (A) (Note 1)} & & & 1 & & & 1 & \(\mathrm{V} / \mu \mathrm{s}\) \\
\hline REXT & \multicolumn{2}{|l|}{External Timing Resistor (Note 1)} & 1.4 & & 30 & 1.4 & & 40 & \(\mathrm{k} \Omega\) \\
\hline \(\mathrm{C}_{\text {EXT }}\) & \multicolumn{2}{|l|}{External Timing Capacitance (Note 1)} & 0 & & 1000 & 0 & & 1000 & \(\mu \mathrm{F}\) \\
\hline \multirow[t]{2}{*}{DC} & \multirow[t]{2}{*}{Duty Cycle (Note 1)} & \(\mathrm{R}_{\mathrm{T}}=2 \mathrm{k} \Omega\) & & & 67 & & & 67 & \% \\
\hline & & \(\mathrm{R}_{\mathrm{T}}=\mathrm{R}_{\mathrm{EXT}}\) (Max) & & & 90 & & & 90 & \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Note 1: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) }
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=M i n, I_{O L}=\operatorname{Max}, \\
& V_{I H}=M i n, V_{I L}=M a x
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{2}{*}{\(\mathrm{I}_{\mathrm{H}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=2.4 V
\end{aligned}
\]} & A1, A2 & & & 40 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & B & & & 80 & \\
\hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Max} \\
& V_{1}=0.4 \mathrm{~V}
\end{aligned}
\]} & A1, A2 & & & -1.6 & \multirow[t]{2}{*}{mA} \\
\hline & & & B & & & -3.2 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
& \text { (Note 2) }
\end{aligned}
\]} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline \multirow[t]{2}{*}{ICC} & \multirow[t]{2}{*}{Supply Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & Quiescent & & 13 & 25 & \multirow[t]{2}{*}{mA} \\
\hline & & & Triggered & & 23 & 40 & \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

Switching Characteristics
at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Outout Load)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & From (Input) To (Output) & Conditions & Min & Max & Units \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
\begin{gathered}
\text { A1, A2 } \\
\text { to Q }
\end{gathered}
\] & \multirow[t]{4}{*}{\[
\begin{aligned}
& C_{E X T}=80 \mathrm{pF} \\
& \mathrm{R}_{\text {INT }} \text { to } V_{C C} \\
& C_{\mathrm{L}}=15 \mathrm{pF} \\
& \mathrm{R}_{\mathrm{L}}=400 \Omega
\end{aligned}
\]} & & 70 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
\begin{gathered}
B \text { to } \\
\mathrm{Q} \\
\hline
\end{gathered}
\] & & & 55 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
\begin{aligned}
& \mathrm{A} 1, \mathrm{~A} 2 \\
& \text { to } \overline{\mathrm{Q}}
\end{aligned}
\] & & & 80 & ns \\
\hline \(\mathrm{t}_{\mathrm{PHL}}\) & Propagation Delay Time High to Low Level Output & \[
\text { to } \bar{Q}
\] & & & 65 & ns \\
\hline \({ }^{\text {tw }}\) (OUT) & Output Pulse Width Using the Internal Timing Resistor & \[
\begin{aligned}
& \mathrm{A} 1, \mathrm{~A} 2 \text { or } \mathrm{B} \\
& \text { to } \mathrm{Q}, \overline{\mathrm{Q}}
\end{aligned}
\] & \[
\begin{aligned}
& \mathrm{C}_{\text {EXT }}=80 \mathrm{pF} \\
& \mathrm{R}_{\text {INT }} \text { to } \mathrm{V}_{\mathrm{CC}} \\
& \mathrm{R}_{\mathrm{L}}=400 \Omega \\
& \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\
& \hline
\end{aligned}
\] & 70 & 150 & ns \\
\hline \({ }^{\text {tw(OUT }}\) ) & Output Pulse Width Using Zero Timing Capacitance & \[
\begin{aligned}
& \mathrm{A} 1, \mathrm{~A} 2 \\
& \text { to } \mathrm{Q}, \overline{\mathrm{Q}}
\end{aligned}
\] & \[
\begin{aligned}
& \mathrm{C}_{E X T}=0 \mathrm{pF} \\
& \mathrm{R}_{\text {INT }} \text { to } \mathrm{V}_{\mathrm{CC}} \\
& \mathrm{R}_{\mathrm{L}}=400 \Omega \\
& \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\
& \hline
\end{aligned}
\] & & 50 & ns \\
\hline \multirow[t]{2}{*}{\({ }^{\text {tw }}\) (OUT)} & \multirow[t]{2}{*}{Output Pulse Width Using External Timing Resistor} & \[
\begin{aligned}
& \mathrm{A} 1, \mathrm{~A} 2 \\
& \text { to } \mathrm{Q}, \overline{\mathrm{Q}}
\end{aligned}
\] & \[
\begin{aligned}
& C_{E X T}=100 \mathrm{pF} \\
& \mathrm{R}_{\text {INT }}=10 \mathrm{k} \Omega \\
& \mathrm{R}_{\mathrm{L}}=400 \Omega \\
& \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}
\end{aligned}
\] & 600 & 800 & ns \\
\hline & & \[
\begin{aligned}
& \mathrm{A} 1, \mathrm{~A} 2 \\
& \text { to } \mathrm{Q}, \overline{\mathrm{Q}}
\end{aligned}
\] & \[
\begin{aligned}
& \mathrm{C}_{\mathrm{EXT}}=1 \mu \mathrm{~F} \\
& \mathrm{R}_{\mathrm{INT}}=10 \mathrm{k} \Omega \\
& \mathrm{R}_{\mathrm{L}}=400 \Omega \\
& \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\
& \hline
\end{aligned}
\] & 6 & 8 & ms \\
\hline
\end{tabular}

\section*{Operating Rules}
1. To use the internal \(2 \mathrm{k} \Omega\) timing resistor, connect the \(\mathrm{R}_{\mathrm{INT}}\) pin to \(V_{C C}\).
2. An external resistor ( \(\mathrm{R}_{\mathrm{X}}\) ) or the internal resistor (2 \(\mathrm{k} \Omega\) ) and an external capacitor ( \(C_{X}\) ) are required for proper operation. The value of \(C_{X}\) may vary from 0 to any necessary value. For small time constants use high-quality mica, glass, polypropylene, polycarbonate, or polystyrene capacitors. For large time constants use solid tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
3. The pulse width is essentially determined by external timing components \(\mathrm{R}_{\mathrm{X}}\) and \(\mathrm{C}_{\mathrm{X}}\). For \(\mathrm{C}_{\mathrm{X}}<1000 \mathrm{pF}\) see Figure 1 design curves on \(T_{W}\) as function of timing components value. For \(\mathrm{C}_{X}>1000 \mathrm{pF}\) the output is defined as:
\(t_{W}=K R_{X} C_{X}\)
where [ \(\mathrm{R}_{\mathrm{X}}\) is in Kilo-ohm]
[ \(C_{X}\) is in pico Farad]
[ \(T_{W}\) is in nano second]
[ \(\mathrm{K} \approx 0.7\) ]


FIGURE 1
4. If \(C_{X}\) is an electrolytic capacitor a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current (Figure 2).


TL/F/6538-3
FIGURE 2

\section*{Operating Rules (Continued)}
5. Output pulse width versus \(\mathrm{V}_{\mathrm{CC}}\) and operation temperatures: Figure 3 depicts the relationship between pulse width variation versus \(\mathrm{V}_{\mathrm{CC}}\). Figure 4 depicts pulse width variation versus ambient temperature.


FIGURE 3


TL/F/6538-5
FIGURE 4
6. The " \(K\) " coefficient is not a constant, but varies as a function of the timing capacitor Cx. Figure 5 details this characteristic.


TL/F/6538-6
FIGURE 5
7. Under any operating condition \(C_{X}\) and \(R_{X}\) must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce \(I \times R\) and Ldi/dt voltage developed along their connecting paths. If the lead length from \(C_{X}\) to pins (10) and (11) is greater than 3 cm , for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of \(\mathrm{C}_{X}\) in each cycle of its operation so that the output pulse width will be accurate.
8. \(\mathrm{V}_{\mathrm{CC}}\) and ground wiring should conform to good high-frequency standards and practices so that switching transients on the \(V_{C C}\) and ground return leads do not cause interaction between one-shots. \(\mathrm{A} 0.01 \mu \mathrm{~F}\) to \(0.10 \mu \mathrm{~F}\) bypass capacitor (disk ceramic or monolithic type) from \(V_{C C}\) to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the \(\mathrm{V}_{\mathrm{CC}}{ }^{-}\) pin as space permits.
For further detailed device characteristics and output performance please refer to the NSC one-shot application note, AN-366.

National Semiconductor

\section*{54122/DM74122}

\section*{Retriggerable Resettable Multivibrator}

\section*{General Description}

The '122 features positive and negative DC level triggering inputs, complementary outputs, an optional \(10 \mathrm{k} \Omega\) internal timing resistor and an overriding Direct Clear ( \(\overline{\mathrm{C}}_{\mathrm{D}}\) ) input. When the circuit is in the quasi-stable (delay) state, another trigger applied to the inputs (per Truth Table) will cause the delay period to start again, without disturbing the outputs. This process can be repeated indefinitely and thus the output pulse period (Q HIGH, \(\bar{Q}\) LOW) can be made as long as desired. Alternatively, a delay period can be terminated
by a LOW signal applied to \(\overline{\mathrm{C}}_{\mathrm{D}}\), which also prevents triggering. An internal connection from \(\overline{\mathrm{C}}_{\mathrm{D}}\) to the input gate makes it possible to trigger the circuit by a positive-going signal on \(\bar{C}_{D}\), as shown in the Truth Table. For timing capacitor values greater than 1000 pF , the output pulse width is defined as follows:
\[
t_{w}=0.32 R_{X} C_{X}\left(1.0+0.7 / R_{X}\right)
\]

Where \(t_{w}\) is in \(n s, R_{x}\) is in \(k \Omega\) and \(C_{x}\) is in \(p F\).

\section*{Logic Symbol}


TL/F/10212-2
\(V_{C C}=\operatorname{Pin} 14\)
GND \(=\operatorname{Pin} 7\)
NC \(=\) Pins 10 and 12

Order Number \(54122 \mathrm{DMQB}, 54122\) FMQB or DM74122N
See NS Package Number J14A, N14A or W14B
\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{c|}{ Description } \\
\hline\(\overline{\mathrm{A}}_{1}, \overline{\mathrm{~A}}_{2}\) & Trigger Inputs (Active Falling Edge) \\
\(\mathrm{B}_{1}, \mathrm{~B}_{2}\) & Trigger Inputs (Active Rising Edge) \\
\(\overline{\mathrm{C}}_{\mathrm{D}}\) & Direct Clear Inputs (Active LOW) \\
\(\mathrm{Q}, \overline{\mathrm{Q}}\) & Outputs \\
\hline
\end{tabular}
\begin{tabular}{lr} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range \\
54 & \\
DM74 & \\
Storage Temperature Range & \(0^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
Sm \(+70^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multicolumn{2}{|c|}{ Parameter } & \multicolumn{3}{|c|}{54122} & \multicolumn{3}{c|}{ DM74122 } \\
\cline { 3 - 7 } & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.5 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & -55 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Recommended Operating Conditions \(\mathrm{v}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Parameter}} & \multirow[t]{2}{*}{Conditions} & \multicolumn{2}{|c|}{DM74} & \multirow[t]{2}{*}{Units} \\
\hline & & & & Min & Max & \\
\hline \(t_{w}\) & \multicolumn{2}{|l|}{Trigger Pulse Width} & \multirow{4}{*}{Over Operating \(\mathrm{V}_{\mathrm{CC}}\) and Temperature Range} & 40 & & ns \\
\hline \multirow[t]{2}{*}{RX} & \multirow[t]{2}{*}{External Timing Resistor} & XC & & 5.0 & 50 & \multirow[t]{2}{*}{k \(\Omega\)} \\
\hline & & XM & & 5.0 & 25 & \\
\hline \(C_{X}\) & \multicolumn{2}{|l|}{External Timing Capacitor} & & \multicolumn{2}{|l|}{No Restrictions} & pF \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) }
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{I}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, I_{\mathrm{OH}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}\)} & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{2}{*}{\(I_{1 H}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & Inputs & & & 40 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Clear & & & 80 & \\
\hline \multirow[t]{2}{*}{IIL.} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}\)} & Inputs & & & -1.6 & \multirow[t]{2}{*}{mA} \\
\hline & & & Clear & & & -3.2 & \\
\hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 2)} & -10 & & -40 & mA \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & & 28 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

\section*{Switching Characteristics}
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 3 for waveforms and load configurations)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{Conditions} & \multicolumn{2}{|c|}{54/74} & \multirow{3}{*}{Units} \\
\hline & & & \multicolumn{2}{|c|}{\[
\begin{aligned}
& C_{L}=15 \mathrm{pF} \\
& R_{\mathrm{L}}=400 \Omega
\end{aligned}
\]} & \\
\hline & & & Min & Max & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay B to Q & \multirow{4}{*}{\begin{tabular}{l}
\[
C_{X}=0 \mathrm{pF}, \mathrm{R}_{\mathrm{X}}=5 \mathrm{k} \Omega
\] \\
Figure 3-1, Figure a
\end{tabular}} & & 28 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay \(\bar{A}\) to \(Q\) & & & 33 & ns \\
\hline \({ }_{\text {PPLH }}\) & Propagation Delay \(B\) to \(\bar{Q}\) & & & 36 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay \(\bar{A}\) to \(\bar{Q}\) & & & 40 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay \(\bar{C}_{D}\) to \(\bar{Q}\) & \multirow[t]{2}{*}{\begin{tabular}{l}
\(C_{X}=0 \mathrm{pF}, \mathrm{R}_{\mathrm{X}}=5 \mathrm{k} \Omega\) \\
Figure 3-1, Figure 3-10
\end{tabular}} & & 40 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay \(\bar{C}_{D}\) to \(Q\) & & & 27 & ns \\
\hline \(t_{\text {w }}\) (out) & Pulse Width at Q with Zero Timing Capacitor & \begin{tabular}{l}
\[
C_{X}=0 \mathrm{pF}, \mathrm{R}_{\mathrm{X}}=5 \mathrm{k} \Omega
\] \\
Figure 3-1, Figure a
\end{tabular} & & 65 & ns \\
\hline \(t_{\text {w }}\) (out) & Pulse Width with External Timing Components & \begin{tabular}{l}
\[
C_{X}=1000 \mathrm{pF}, R_{X}=10 \mathrm{k} \Omega
\] \\
Figure 3-1, Figure a
\end{tabular} & 3.08 & 3.76 & \(\mu \mathrm{S}\) \\
\hline
\end{tabular}

\section*{Triggering Truth Table}
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multicolumn{5}{|c|}{Inputs*} & \multirow{2}{*}{Response} \\
\hline \(\bar{C}_{\text {D }}\) & \(\bar{A}_{1}\) & \(\bar{A}_{2}\) & \(\mathrm{B}_{1}\) & \(\mathrm{B}_{2}\) & \\
\hline L & X & X & X & X & No Trigger \\
\hline X & V & L & X & X & No Trigger \\
\hline X & \(\checkmark\) & X & L & X & No Trigger \\
\hline H & \(\checkmark\) & H & H & H & Trigger \\
\hline X & X & X & \(\checkmark\) & L & No Trigger \\
\hline X & H & H & \(\checkmark\) & X & No Trigger \\
\hline H & L & X & \(\checkmark\) & H & Trigger \\
\hline - & L & X & H & H & Trigger \\
\hline
\end{tabular}

H \(=\) HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
*Input pins 1 and 2 are logically interchangeable, as are input pins 3 and 4.


\section*{54123/DM74123 Dual Retriggerable One-Shot with Clear and Complementary Outputs}

\section*{General Description}

The '123 is a dual retriggerable monostable multivibrator capable of generating output pulses from a few nano-seconds to extremely long duration up to \(100 \%\) duty cycle. Each device has three inputs permitting the choice of either leading-edge or trailing edge triggering. Pin \((A)\) is an activelow transition trigger input and pin \((B)\) is an active-high transition trigger input. The clear (CLR) input terminates the output pulse at a predetermined time independent of the timing components.
National's '123 device features a unique logic realization not implemented by other manufacturers. The "Clear" input will not trigger the device, a design tailored for applications where it shall only terminate or reduce a timing pulse.
To obtain the best and trouble free operation from this device please read the operating rules as well as the NSC one-shot application notes carefully and observe recommendations.

\section*{Features}
- DC triggered from active-high transition or active-low transition inputs
- Retriggerable to \(100 \%\) duty cycle
- Direct reset terminates output pulse
- Compensated for \(V_{C C}\) and temperature variations
- DTL, TTL compatible
- Input clamp diodes

\section*{Functional Description}

The basic output pulse width is determined by selection of an external resistor ( \(\mathrm{R}_{\mathrm{X}}\) ) and capacitor ( \(\mathrm{C}_{\mathrm{X}}\) ). Once triggered, the basic pulse width may be extended by retriggering the gated active-low transition or active-high transition inputs or be reduced by use of the active-low transition clear input. Retriggering to \(100 \%\) duty cycle is possible by application of an input pulse train whose cycle time is shorter than the output cycle time such that a continuous "HIGH" logic state is maintained at the " \(Q\) " output.

\section*{Connection Diagram}


H = HIGH Voltage Level
\(\mathrm{L}=\) LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
7V
Input Voltage
5.5 V

Operating Free Air Temperature Range
\begin{tabular}{lr}
54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{54123} & \multicolumn{3}{|c|}{DM74123} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voitage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
\hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.8 & & & -0.8 & mA \\
\hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & & & 16 & mA \\
\hline \multirow[t]{3}{*}{\(t_{W}\)} & \multirow[t]{3}{*}{Pulse Width (Note 5)} & A or B High & & & & 40 & & & \multirow{3}{*}{ns} \\
\hline & & A or B Low & & & & 40 & & & \\
\hline & & Clear Low & & & & 40 & & & \\
\hline TWQ (Min) & Minimum Width of Pulse at Q (Note 5) & A or B & & & 80 & & & 65 & ns \\
\hline REXT & \multicolumn{2}{|l|}{External Timing Resistor} & & & & 5 & & 50 & \(\mathrm{k} \Omega\) \\
\hline \(\mathrm{C}_{\text {EXT }}\) & \multicolumn{2}{|l|}{External Timing Capacitance} & & & & \multicolumn{3}{|c|}{No Restriction} & \(\mu \mathrm{F}\) \\
\hline CWIRE & \multicolumn{2}{|l|}{Wiring Capacitance at \(\mathrm{R}_{\mathrm{EXT}} / \mathrm{C}_{\mathrm{EXT}}\) Terminal (Note 5)} & & & & & & 50 & pF \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) } \\
\hline
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 54 & 2.4 & \multirow[t]{2}{*}{3.4} & & \multirow[t]{2}{*}{V} \\
\hline & & & DM74 & 2.5 & & & \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\) & & & & 1 & mA \\
\hline \multirow[t]{2}{*}{IIH} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{I}}=2.4 \mathrm{~V}
\end{aligned}
\]} & Data & & & 40 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Clear & & & 80 & \\
\hline \multirow[t]{2}{*}{ILL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}\)} & Clear & & & -3.2 & \multirow[t]{2}{*}{mA} \\
\hline & & & Data & & & -1.6 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& (\text { Note 2) }
\end{aligned}
\]} & 54 & -10 & & -40 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -10 & & -40 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}(\) Notes 3 and 4)} & & 46 & 66 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: Quiescent \(\mathrm{I}_{\mathrm{CC}}\) is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, \(\mathrm{C}_{\mathrm{EXT}}=0.02 \mu \mathrm{~F}\), and \(\mathrm{R}_{\mathrm{EXT}}=\) \(25 \mathrm{~K} \Omega\).
Note 4: \(\mathrm{I}_{\mathrm{CC}}\) is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, \(\mathrm{C}_{\mathrm{EXT}}=0.02 \mu \mathrm{~F}\), and \(\mathrm{R}_{\mathrm{EXT}}=25 \mathrm{k} \Omega\).
Note 5: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{From (Input) To (Output)} & \multicolumn{2}{|c|}{54123} & \multicolumn{2}{|c|}{DM74123} & \multirow{3}{*}{Units} \\
\hline & & & \multicolumn{2}{|l|}{\[
\begin{gathered}
C_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=400 \Omega \\
\mathrm{C}_{\mathrm{EXT}}=0 \mathrm{pF}, \mathrm{R}_{\mathrm{EXT}}=5 \mathrm{k} \Omega \\
\hline
\end{gathered}
\]} & \multicolumn{2}{|l|}{\[
\begin{gathered}
\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=400 \Omega \\
\mathrm{C}_{\mathrm{EXT}}=1000 \mathrm{pF}, \mathrm{R}_{\mathrm{EXT}}=10 \mathrm{~K} \Omega \\
\hline
\end{gathered}
\]} & \\
\hline & & & Min & Max & Min & Max & \\
\hline tpLH & Propagation Delay Time Low to High Level Output & \(\bar{A}\) to \(Q\) & & 33 & & 33 & ns \\
\hline tpLH & Propagation Delay Time Low to High Level Output & \(B\) to \(Q\) & & 28 & & 28 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \(\bar{A}\) to \(\bar{Q}\) & & 40 & & 40 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \(B\) to \(\bar{Q}\) & & 36 & & 36 & ns \\
\hline tpLH & Propagation Delay Time Low to High Level Output & Clear to \(\overline{\mathbf{Q}}\) & & 40 & & 40 & ns \\
\hline \({ }^{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & \(\overline{\text { Clear to } Q}\) & & 27 & & 27 & ns \\
\hline tw(out) & Output Pulse Width* & A or B to Q & 3.08 & 3.76 & 3.08 & 3.76 & \(\mu \mathrm{S}\) \\
\hline
\end{tabular}
\({ }^{*} \mathrm{C}_{\mathrm{ECT}}=1000 \mathrm{pF}, \mathrm{R}_{\mathrm{EXT}}=10 \mathrm{k} \Omega\)

\section*{Operating Rules}
1. An external resistor ( \(R_{X}\) ) and external capacitor ( \(C_{X}\) ) are required for proper operation. The value of \(\mathrm{C}_{\mathrm{X}}\) may vary from 0 to any necessary value. For small time constants high-grade mica, glass, polypropylene, polycarbonate, or polystyrene material capacitors may be used. For large time constants use tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
2. When an electrolytic capacitor is used for \(\mathrm{C}_{X}\) a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current (Figure 2). However, its use in general is not recommended with retriggerable operation.
3. The output pulse width ( \(T_{W}\) ) for \(\mathrm{C}_{X}>1000 \mathrm{pF}\) is defined as follows:
\(T_{W}=K R_{X} C_{X}\left(1+0.7 / R_{X}\right)\)
where [ \(R_{X}\) is in Kilo-ohm]
\[
\begin{aligned}
& {\left[C_{X}\right. \text { is in pico Farad] }} \\
& {\left[T_{W} \text { is in nano second }\right]} \\
& {[K \approx 0.34]}
\end{aligned}
\]
4. The multiplicative factor \(K\) is plotted as a function of \(C_{X}\) below for design considerations:


TL/F/6539-2


TL/F/6539-3
FIGURE 2
5. For \(C_{X}<1000 \mathrm{pF}\) see Figure 3 for \(T_{W}\) vs \(C_{X}\) family curves with \(\mathrm{RX}_{\mathrm{X}}\) as a parameter:


TL/F/6539-4
FIGURE 3
6. To obtain variable pulse width by remote trimming, the following circuit is recommended:


TL/F/6539-5
Note: "Rremote" should be as close to the one-shot as possible.
FIGURE 4

\section*{Operating Rules (Continued)}
7. The retriggerable pulse width is calculated as shown below:
\[
T=T_{W}+t_{P L H}=K \times R_{X} \times C_{X}+t_{P L H}
\]

The retriggered pulse width is equal to the pulse width plus a delay time period (Figure 5).


FIGURE 5
8. Output pulse width versus \(\mathrm{V}_{\mathrm{CC}}\) and Temperatures: Figure 6 depicts the relationship between pulse width variation versus operating \(\mathrm{V}_{\mathrm{cc}}\). Figure 7 depicts pulse width variation versus ambient temperatures.


TL/F/6539-7
FIGURE 6


FIGURE 7
9. Under any operating condition \(C_{X}\) and \(R_{X}\) must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce \(I \times R\) and \(\mathrm{Ldi} / \mathrm{dt}\) voltage developed along their connecting paths. If the lead length from \(\mathrm{C}_{X}\) to pins (6) and (7) or pins (14) and (15) is greater than 3 cm , for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of \(C_{X}\) in each cycle of its operation so that the output pulse width will be accurate.
10. The \(\mathrm{C}_{\text {EXT }}\) pins of this device are internally connected to the internal ground. For optimum system performance they should be hard wired to the system's return ground plane.
* However, it should be noted that although the 74221 series one-shot is pin-for-pin compatiable with the ' 123 device, its CEXT \(^{\text {pin }}\) is not an internal connection to ground. Hence, if substitution of an '221 on to an '123 design layout whose C EXT pin is wired to the ground is attempted, the ' 221 device will not function!
11. \(\mathrm{V}_{\mathrm{CC}}\) and ground wiring should conform to good high-frequency standards and practices so that switching transients on the \(\mathrm{V}_{\mathrm{CC}}\) and ground return leads do not cause interaction between one-shots. A \(0.01 \mu \mathrm{~F}\) to \(0.10 \mu \mathrm{~F}\) bypass capacitor (disk ceramic or monolithic type) from \(V_{C C}\) to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the \(V_{C C}\) pin as space permits.
*For further detailed device characteristics and output performance please refer to the NSC one-shot application note, AN-366.

\section*{54125/DM54125/DM74125 \\ Quad TRI-STATE \({ }^{\circledR}\) Buffers}

\section*{General Description}

This device contains four independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard TTL output with additional drive capability at the high Logic level to permit the driving of bus lines without external pull-up resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

\section*{Features}
- Alternate Military/Aerospace device (54125) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

\section*{Connection Diagram}

\section*{Dual-In-Line Package}


TL/F/6540-1
Order Number 54125DMQB, 54125FMQB, DM54125J, DM54125W or DM74125N See NS Package Number J14A, N14A or W14B

\section*{Function Table}
\begin{tabular}{|c|c|c|}
\hline \multicolumn{3}{|c|}{\(\mathbf{Y}=\mathbf{A}\)} \\
\hline \multicolumn{2}{|c|}{ Inputs } & Output \\
\hline \(\mathbf{A}\) & \(\mathbf{C}\) & \(\mathbf{Y}\) \\
\hline L & L & L \\
H & L & H \\
X & H & Hi-Z \\
\hline
\end{tabular}

\footnotetext{
H = High Logic Level
L = Low Logic Level
\(X=\) Either Low or High Logic Level
\(\mathrm{Hi}-\mathrm{Z}=\) TRI-STATE (Outputs are disabled)
}

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
\begin{tabular}{lr} 
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \\
\(\quad\) DM54 and 54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM 74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54125} & \multicolumn{3}{|c|}{DM74125} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -2 & & & -5.2 & mA \\
\hline \(\mathrm{lOL}^{\text {l }}\) & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics}
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) } \\
\hline
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.3 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline IIZL & Off-State Input Current with Low Level Input Voltage Applied & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -40 & \(\mu \mathrm{A}\) \\
\hline lozh & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Max}, V_{O}=2.4 V \\
& V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
\end{aligned}
\]} & & & 40 & \(\mu \mathrm{A}\) \\
\hline lozl & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Max}, V_{O}=0.4 V \\
& V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
\end{aligned}
\]} & & & -40 & \(\mu \mathrm{A}\) \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=\text { Max } \\
& \text { (Note 2) }
\end{aligned}
\]} & DM54 & -30 & & -70 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -28 & & -70 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}(\) Note 3)} & & 36 & 54 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: \(\mathrm{I}_{\mathrm{CC}}\) is measured with the output control \((\mathrm{C})\) inputs at 4.5 V , the data inputs grounded, and the outputs open.

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega\)} & \multirow{3}{*}{Units} \\
\hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
\hline & & Min & Max & Min & Max & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & & & & 15 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & & & & 18 & ns \\
\hline \(t_{\text {PZH }}\) & Output Enable Time to High Level Output & & & & 18 & ns \\
\hline tpzL & Output Enable Time to Low Level Output & & & & 25 & ns \\
\hline \(t_{\text {PHZ }}\) & Output Disable Time from High Level Output & & 8 & & & ns \\
\hline \(t_{\text {PLZ }}\) & Output Disable Time from Low Level Output & & 14 & & & ns \\
\hline
\end{tabular}

\section*{DM54132/DM74132 Quad 2-Input NAND Gates with Schmitt Trigger Inputs}

\section*{General Description}

This device contains four independent gates each of which performs the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter-free output.

\section*{Connection Diagram}


Function Table
\begin{tabular}{|c|c|c|}
\multicolumn{3}{c|}{\(\mathbf{Y}=\overline{\mathbf{A B}}\)} \\
\hline \multicolumn{2}{|c|}{ Inputs } & Output \\
\hline \(\mathbf{A}\) & \(\mathbf{B}\) & \(\mathbf{Y}\) \\
\hline L & L & \(H\) \\
L & \(H\) & \(H\) \\
\(H\) & L & \(H\) \\
\(H\) & \(H\) & L \\
\hline
\end{tabular}
\(H=\) High Logic Level
\(L=\) Low Logic Level
\begin{tabular}{lr} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM54 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
DM74 & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54132} & \multicolumn{3}{|c|}{DM74132} & \multirow{2}{*}{Units} \\
\hline & & Min & Typ & Max & Min & Typ & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{T}+}\) & \begin{tabular}{l}
Positive-Going Input \\
Threshold Voltage (Note 1)
\end{tabular} & 1.5 & 1.7 & 2 & 1.5 & 1.7 & 2 & V \\
\hline \(\mathrm{V}_{\mathrm{T}-}\) & Negative-Going Input Threshold Voltage (Note 1) & 0.6 & 0.9 & 1.1 & 0.6 & 0.9 & 1.1 & V \\
\hline HYS & Input Hysteresis (Note 1) & 0.4 & 0.8 & & 0.4 & 0.8 & & V \\
\hline IOH & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating tree air temperature (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 2) }
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{I}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\text { Max } \\
& \mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{T}-\mathrm{Min}}
\end{aligned}
\]} & DM54 & 2.4 & 3.4 & & \multirow[t]{2}{*}{V} \\
\hline & & & DM74 & 2.4 & 3.4 & & \\
\hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{T}+} \mathrm{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline \({ }_{1}+\) & Input Current at Positive-Going Threshold & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~V}_{1}=\mathrm{V}_{T+}\)} & & -0.43 & & mA \\
\hline \(1 T_{\text {- }}\) & Input Current at Negative-Going Threshold & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{T}-}\)} & & -0.56 & & mA \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & -0.8 & -1.2 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& (\text { Note 3) }
\end{aligned}
\]} & DM54 & -18 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(V_{C C}=\) Max} & & 15 & 24 & mA \\
\hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(V_{C C}=\) Max} & & 26 & 40 & mA \\
\hline
\end{tabular}

Note 1: \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
Note 2: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 3: Not more than one output should be shorted at a time.

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\[
\begin{aligned}
& \mathrm{R}_{\mathrm{L}}=400 \Omega \\
& \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}
\end{aligned}
\]} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & & 22 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & & 22 & ns \\
\hline
\end{tabular}

\section*{DM54145/DM74145}

BCD to Decimal Decoders/Drivers

\section*{General Description}

These BCD-to-decimal decoders/drivers consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of BCD input logic ensures that all outputs remain off for all invalid (1015) binary input conditions. These decoders feature highperformance, NPN output transistors designed for use as indicator/relay drivers, or as open-collector logic-circuit drivers. The high-breakdown output transistors are compatible for interfacing with most MOS integrated circuits.

\section*{Features}
- Full decoding of input logic
- 80 mA sink-current capability
- All outputs are off for invalid BCD input conditions

Connection Diagram
Dual-In-Line Package


TL/F/6544-1
Order Number DM54145J, DM54145W or DM74145N See NS Package Number J16A, N16E or W16A

\section*{Function Table}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{No.} & \multicolumn{4}{|c|}{Inputs} & \multicolumn{10}{|c|}{Outputs} \\
\hline & D & C & B & A & 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 \\
\hline 0 & L & L & L & L & L & H & H & H & H & H & H & H & H & H \\
\hline 1 & L & L & L & H & H & L & H & H & H & H & H & H & H & H \\
\hline 2 & L & L & H & L & H & H & L & H & H & H & H & H & H & H \\
\hline 3 & L & L & H & H & H & H & H & L & H & H & H & H & H & H \\
\hline 4 & L & H & L & L & H & H & H & H & L & H & H & H & H & H \\
\hline 5 & L & H & L & H & H & H & H & H & H & L & H & H & H & H \\
\hline 6 & L & H & H & L & H & H & H & H & H & H & L & H & H & H \\
\hline 7 & L & H & H & H & H & H & H & H & H & H & H & L & H & H \\
\hline 8 & H & L & L & L & H & H & H & H & H & H & H & H & L & H \\
\hline 9 & H & L & L & H & H & H & H & H & H & H & H & H & H & L \\
\hline 1 & H & L & H & L & H & H & H & H & H & H & H & H & H & H \\
\hline N & H & L & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline V & H & H & L & L & H & H & H & H & H & H & H & H & H & H \\
\hline A & H & H & L & H & H & H & H & H & H & H & H & H & H & H \\
\hline L & H & H & H & L & H & H & H & H & H & H & H & H & H & H \\
\hline 1 & H & H & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline D & & & & & & & & & & & & & & \\
\hline
\end{tabular}
\(H=\) High Level (Off), L = Low Level (On)

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage 7 V
Input Voltage
Operating Free Air Temperature Range
\begin{tabular}{lr} 
DM54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54145} & \multicolumn{3}{|c|}{DM74145} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & & & 15 & & & 15 & V \\
\hline lOL & Low Level Output Current & & & 20 & & & 20 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
(Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(I_{\text {cex }}\) & High Level Output Current & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{V}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & & & 250 & \(\mu \mathrm{A}\) \\
\hline \multirow[t]{2}{*}{\(\mathrm{V}_{\text {OL }}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & & 0.4 & V \\
\hline & & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{IOL}=80 \mathrm{~mA} \\
& \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}
\end{aligned}
\]} & & 0.5 & 0.9 & \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline ILL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{Icc} & \multirow[t]{2}{*}{Supply Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& (\text { Note 2) }
\end{aligned}
\]} & DM54 & & 43 & 62 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & & 43 & 70 & \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Max & Units \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \multirow[t]{2}{*}{\[
\begin{aligned}
& C_{L}=15 \mathrm{pF} \\
& R_{L}=100 \Omega
\end{aligned}
\]} & & 30 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & & & 30 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: ICC is measured with all outputs open and all inputs grounded.


TL/F/6544-2

\section*{DM54148 Priority Encoder}

\section*{General Description}

This TTL encoder features priority decoding of the input data to ensure that only the highest-order data line is encoded. The DM54148 encodes eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input E1 and enable output E0) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level.

\section*{Features}
- Encodes 8 data lines to 3 -line binary (octal)
- Applications include:

N -bit encoding
Code converters and generators

\section*{Connection Diagram}

Dual-In-Line Package


Order Number DM54148J or DM54148W See NS Package Number J16A or W16A

\section*{Function Table}

DM54148
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{9}{|c|}{Inputs} & \multicolumn{5}{|c|}{Outputs} \\
\hline E1 & 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & A2 & A1 & AO & GS & E0 \\
\hline H & X & X & X & X & X & X & X & X & H & H & H & H & H \\
\hline L & H & H & H & H & H & H & H & H & H & H & H & H & L \\
\hline L & X & X & X & X & X & X & X & L & L & L & L & L & H \\
\hline L & X & X & X & X & X & X & L & H & L & L & H & L & H \\
\hline L & X & X & X & X & X & L & H & H & L & H & L & L & H \\
\hline L & X & X & X & X & L & H & H & H & L & H & H & L & H \\
\hline L & X & X & X & L & H & H & H & H & H & L & L & L & H \\
\hline L & X & X & L & H & H & H & H & H & H & L & H & L & H \\
\hline L & X & L & H & H & H & H & H & H & H & H & L & L & H \\
\hline L & L & H & H & H & H & H & H & H & H & H & H & L & H \\
\hline
\end{tabular}

\footnotetext{
\(H=\) High Logic Level, L \(=\) Low Logic Level, \(X=\) Don't Care
}

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
\begin{tabular}{|c|c|}
\hline Supply Voltage & 7V \\
\hline Input Voltage & 5.5 V \\
\hline Operating Free Air Temperature Range DM54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
\hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multirow{2}{*}{ Parameter } & \multicolumn{2}{c|}{ DM54148 } & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline \(\mathrm{IOH}_{\mathrm{OH}}\) & High Level Output Current & & & -0.8 & mA \\
\hline \(\mathrm{IOL}_{\mathrm{OL}}\) & Low Level Output Current & & & 16 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\
& V_{I L}=\operatorname{Max}, V_{I H}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & & & V \\
\hline V OL & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & 0.4 & V \\
\hline 1 & Input Current @Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{2}{*}{\(\mathrm{I}_{\mathrm{H}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{I}}=2.4 \mathrm{~V}
\end{aligned}
\]} & 0 Input & & & 40 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Others & & & 80 & \\
\hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=0.4 V
\end{aligned}
\]} & 0 Input & & & -1.6 & \multirow[t]{2}{*}{mA} \\
\hline & & & Others & & & -3.2 & \\
\hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}(\) Note 2)} & -35 & & -85 & mA \\
\hline ICCl & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\operatorname{Max}\) (Note 3)} & & 40 & 60 & mA \\
\hline ICC2 & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\) (Note 4)} & & 35 & 55 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: \(\mathrm{I}_{\mathrm{CC}} 1\) is measured with inputs E1 and 7 grounded, other inputs and outputs open.
Note 4: ICC2 is measured with all inputs and all outputs open.
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multicolumn{7}{|l|}{Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)} \\
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multirow[t]{2}{*}{Waveform} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & & Min & Max & \\
\hline \({ }_{\text {tpLH }}\) & Propagation Delay Time Low to High Level Output & \[
\begin{gathered}
0 \text { thru } 7 \\
\text { to } \mathrm{AO}, 1,2
\end{gathered}
\] & \multirow{2}{*}{In-Phase Output} & & 15 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & \[
\begin{gathered}
0 \text { thru } 7 \\
\text { to } A 0,1,2
\end{gathered}
\] & & & 14 & ns \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & \[
\begin{gathered}
0 \text { thru } 7 \\
\text { to } \mathrm{AO}, 1,2 \\
\hline
\end{gathered}
\] & \multirow[t]{2}{*}{Out-of-Phase Output} & & 19 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & \[
\begin{gathered}
0 \text { thru } 7 \\
\text { to } \mathrm{AO}, 1,2 \\
\hline
\end{gathered}
\] & & & 19 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \begin{tabular}{l}
0 thru 7 \\
to EO
\end{tabular} & \multirow[t]{2}{*}{Out-of-Phase Output} & & 10 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & 0 thru 7 to E0 & & & 25 & ns \\
\hline \({ }_{\text {tpLH }}\) & Propagation Delay Time Low to High Level Output & 0 thru 7 to GS & \multirow[t]{2}{*}{In-Phase Output} & & 30 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & 0 thru 7 to GS & & & 25 & ns \\
\hline \({ }^{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & \[
\begin{gathered}
\text { E1 to } \\
\text { AO, 1, } 2
\end{gathered}
\] & \multirow[t]{2}{*}{In-Phase Output} & & 16 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & E1 to AO, 1, 2 & & & 15 & ns \\
\hline \({ }_{\text {tpLH }}\) & Propagation Delay Time Low to High Level Output & E1 to GS & \multirow[t]{2}{*}{In-Phase Output} & & 13 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & E1 to GS & & & 15 & ns \\
\hline \({ }_{\text {tpLH }}\) & Propagation Delay Time Low to High Level Output & E1 to E0 & \multirow[t]{2}{*}{In-Phase Output} & & 15 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & E1 to E0 & & & 30 & ns \\
\hline
\end{tabular}


\section*{54150/DM54150/DM74150, 54151A/DM54151A/DM74151A \\ Data Selectors/Multiplexers}

\section*{General Description}

These data selectors/multiplexers contain full on-chip decoding to select the desired data source. The 150 selects one-of-sixteen data sources; the 151A selects one-of-eight data sources. The 150 and 151A have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high and the \(Y\) output (as applicable) low.
The 151A features complementary W and Y outputs, whereas the 150 has an inverted (W) output only.
The 151A incorporates address buffers which have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the 151A outputs are enabled (i.e., strobe low).

\section*{Features}
- 150 selects one-of-sixteen data lines
- 151A selects one-of-eight data lines
- Performs parallel-to-serial conversion
- Permits multiplexing from N lines to one line
- Also for use as Boolean function generator
- Typical average propagation delay time, data input to W output
\[
\begin{array}{lr}
150 & 11 \mathrm{~ns} \\
151 \mathrm{~A} & 9 \mathrm{~ns}
\end{array}
\]
- Typical power dissipation
 151A 135 mW
■ Alternate Military/Aerospace device (54150, 54151A) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Connection Diagrams}


TL/F/6546-1
Order Number 54150DQMB, 54150FMQB,
DM54150J or DM74150N
See NS Package Number J24A, N24A or W24C


TL/F/6546-2
Order Number 54151ADMQB, 54151AFMQB, DM54151AJ, DM54151AW or DM74151AN See NS Package Number J16A, N16E or W16A

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54150} & \multicolumn{3}{|c|}{DM74150} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{1 \mathrm{H}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{IOH}^{\text {l }}\) & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline \(\mathrm{lOL}^{\text {l }}\) & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{'150 Electrical Characteristics}
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \begin{tabular}{l}
Typ \\
(Note 1)
\end{tabular} & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min}, \mathrm{IOL}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \({ }_{1 / H}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\) Max, \(V_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=\operatorname{Max}
\] \\
(Note 2)
\end{tabular}} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\) Max, (Note 3)} & & 40 & 68 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: ICC is measured with the strobe and data select inputs at 4.5V, all other inputs and outputs open.
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{9}{|l|}{\begin{tabular}{l}
'150 Switching Characteristics \\
at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\end{tabular}} \\
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{\begin{tabular}{l}
From (Input) \\
To (Output)
\end{tabular}}} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & & \multicolumn{2}{|c|}{Min} & \multicolumn{2}{|l|}{Max} & \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & \multicolumn{2}{|c|}{Select to W} & & & \multicolumn{2}{|l|}{35} & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & \multicolumn{2}{|c|}{Select to W} & & & 33 & & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \multicolumn{2}{|c|}{Strobe to W} & & & 24 & & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \multicolumn{2}{|c|}{Strobe to W} & & & \multicolumn{2}{|l|}{30} & ns \\
\hline tpLH & Propagation Delay Time Low to High Level Output & \multicolumn{2}{|c|}{\[
\begin{gathered}
\mathrm{EO}-\mathrm{E} 15 \\
\text { to } \mathrm{W}
\end{gathered}
\]} & & & \multicolumn{2}{|l|}{20} & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & \multicolumn{2}{|c|}{\[
\begin{gathered}
\mathrm{EO}-\mathrm{E} 15 \\
\text { to } \mathrm{W}
\end{gathered}
\]} & & & \multicolumn{2}{|l|}{14} & ns \\
\hline \multicolumn{9}{|l|}{Recommended Operating Conditions} \\
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54151A} & \multicolumn{3}{|c|}{DM74151A} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline \(\mathrm{lOL}^{2}\) & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{'151A Electrical Characteristics}
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \begin{tabular}{l}
Typ \\
(Note 1)
\end{tabular} & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, l_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=M i n, I_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & 0.4 & V \\
\hline 11 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\) Max, \(\mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline 1 lL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}
\] \\
(Note 2)
\end{tabular}} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\) Max, (Note 3)} & & 27 & 48 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: \(I_{C C}\) is measured with the strobe and data select inputs at 4.5 V , all other inputs and outputs open.
'151A Switching Characteristics
at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Select (4 Levels) to \(Y\) & & 38 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
Select \\
(4 Levels) to \(Y\)
\end{tabular} & & 30 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Select (3 Levels) to W & & 26 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Select (3 Levels) to W & & 30 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Strobe to \(Y\) & & 33 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Strobe to \(Y\) & & 30 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Strobe to W & & 21 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Strobe to W & & 25 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
\begin{aligned}
& \text { DO-D7 } \\
& \text { to } \mathrm{Y}
\end{aligned}
\] & & 24 & ns \\
\hline tPHL & Propagation Delay Time High to Low Level Output & \[
\begin{aligned}
& \text { D0-D7 } \\
& \text { to } \mathrm{Y}
\end{aligned}
\] & & 24 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
\begin{gathered}
\text { D0-D7 } \\
\text { to W }
\end{gathered}
\] & & 14 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
\begin{aligned}
& \text { D0-D7 } \\
& \text { to W }
\end{aligned}
\] & & 14 & ns \\
\hline
\end{tabular}

\section*{Logic Diagrams}



Function Tables

54150/74150
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multicolumn{5}{|c|}{Inputs} & \multirow{3}{*}{Outputs W} \\
\hline \multicolumn{4}{|c|}{Select} & \multirow[t]{2}{*}{Strobe S} & \\
\hline D & C & B & A & & \\
\hline X & X & X & X & H & H \\
\hline L & L & L & L & L & EO \\
\hline L & L & L & H & L & E1 \\
\hline L & L & H & L & L & E2 \\
\hline L & L & H & H & L & E3 \\
\hline L & H & L & L & L & E4 \\
\hline L & H & L & H & L & E5 \\
\hline L & H & H & L & L & E6 \\
\hline L & H & H & H & L & E7 \\
\hline H & L & L & L & L & E8 \\
\hline H & \(L\) & L & H & L & E9 \\
\hline H & L & H & L & L & E10 \\
\hline H & L & H & H & L & E11 \\
\hline H & H & L & L & L & \(\overline{E 12}\) \\
\hline H & H & L & H & L & E13 \\
\hline H & H & H & L & L & E14 \\
\hline H & H & H & H & L & \(\overline{\text { E15 }}\) \\
\hline
\end{tabular}
\(H=\) High Level, \(L=\) Low Level, \(X=\) Don't Care
\(\overline{\mathrm{E} 0}, \overline{\mathrm{E} 1} \ldots \overline{\mathrm{E} 15}=\) the complement of the level of the respective E input

54151A/75151A
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multicolumn{4}{|c|}{ Inputs } & \multicolumn{2}{c|}{ Outputs } \\
\hline \multicolumn{3}{|c|}{ Select } & Strobe & Y & W \\
\hline C & B & A & S & & \\
\hline X & X & X & H & L & H \\
L & L & L & L & D0 & \(\overline{D 0}\) \\
L & L & H & L & D1 & \(\overline{D 1}\) \\
L & H & L & L & D2 & \(\overline{\text { D2 }}\) \\
L & H & H & L & D3 & \(\overline{\text { D3 }}\) \\
H & L & L & L & D4 & \(\overline{D 4}\) \\
H & L & H & L & D5 & \(\overline{\text { D5 }}\) \\
H & H & L & L & D6 & \(\overline{\text { D6 }}\) \\
H & H & H & L & D7 & \(\overline{D 7}\) \\
\hline
\end{tabular}
\(H=\) High Level, \(L=\) Low Level, \(X=\) Don't Care \(D 0, D 1 \ldots D 7=\) the level of the respective \(D\) input

\section*{54153/DM54153/DM74153 Dual 4-Line to 1-Line Data Selectors/Multiplexers}

\section*{General Description}

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

\section*{Features}

四 Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe (enable) line provided for cascading ( N lines to \(n\) lines)
. High fan-out, low-impedance, totem-pole outputs
- Typical average propagation delay times

From data 11 ns
From strobe 18 ns
From select 20 ns
■ Typical power dissipation 170 mW
\(\square\) Alternate Military/Aerospace device (54153) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

\section*{Function Table}
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \begin{tabular}{c} 
Select \\
Inputs
\end{tabular} & \multicolumn{5}{|c|}{ Data Inputs } & Strobe & Output \\
\hline B & A & Co & C1 & C2 & C3 & G & Y \\
\hline X & X & X & X & X & X & H & L \\
L & L & L & X & X & X & L & L \\
L & L & H & X & X & X & L & H \\
L & H & X & L & X & X & L & L \\
L & H & X & H & X & X & L & H \\
H & L & X & X & L & X & L & L \\
H & L & X & X & H & X & L & H \\
H & H & X & X & X & L & L & L \\
H & H & X & X & X & H & L & H \\
\hline
\end{tabular}

Select inputs \(A\) and \(B\) are common to both sections.
\(H=\) High Level, \(L=\) Low Level, \(X=\) Don't Care

\section*{Connection Diagram}

Order Number 54153DMQB, 54153FMQB, DM54153J, DM54153W or DM74153N
See NS Package Number J16A, N16E or W16A

\begin{tabular}{lr} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM54 and 54 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
DM74 & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54153} & \multicolumn{3}{|c|}{DM74153} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \begin{tabular}{l}
Typ \\
(Note 1)
\end{tabular} & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline V OH & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\
& V_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.2 & & V \\
\hline VOL & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\
& V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(I_{\text {IH }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& \text { (Note 2) }
\end{aligned}
\]} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -57 & \\
\hline \multirow[t]{2}{*}{Icc} & \multirow[t]{2}{*}{Supply Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=M a x
\] \\
(Note 3)
\end{tabular}} & DM54 & & 34 & 52 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & & 34 & 60 & \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: ICC is measured with the outputs open and all inputs grounded.

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=30 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & Data to Y & & 18 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to \(Y\) & & 23 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Select to Y & & 34 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Select to Y & & 34 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Strobe to \(Y\) & & 30 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Strobe to Y & & 23 & ns \\
\hline
\end{tabular}

\section*{Logic Diagram}


TL/F/6547-2

\section*{54154/DM54154/DM74154 \\ 4-Line to 16-Line Decoders/Demultiplexers}

\section*{General Description}

Each or these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

\section*{Features}
- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical propagation delay 3 levels of logic 19 ns Strobe 18 ns
- Typical power dissipation 170 mW
- Alternate Military/Aerospace device (54154) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

\section*{Connection Diagram}

\section*{Dual-In-Line Package}


TL/F/6548-1
Order Number 54154DMQB, 54154FMQB, DM54154J or DM74154N
See NS Package Number J24A, N24A or W24C

\section*{Absolute Maximum Ratings (Note)}
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If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for avallability and specifications.
Supply Voltage
Operating Free Air Temperature Range

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\section*{DM54 and 54}

DM74
Storage Temperature Range
\[
\begin{array}{r}
-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\
0^{\circ} \mathrm{C} \text { to }+70^{\circ} \mathrm{C} \\
-65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C}
\end{array}
\]

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54154} & \multicolumn{3}{|c|}{DM74154} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \({ }_{\mathrm{OH}}\) & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) }
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.2 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=M i n, I_{O L}=\operatorname{Max} \\
& V_{I H}=\operatorname{Min}, V_{I L}=M a x
\end{aligned}
\]} & & 0.25 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{I}_{\mathrm{I}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
& \text { (Note 2) }
\end{aligned}
\]} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -57 & \\
\hline \multirow[t]{2}{*}{ICC} & \multirow[t]{2}{*}{Supply Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\text { Max } \\
& \text { (Note 3) }
\end{aligned}
\]} & DM54 & & 34 & 49 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & & 34 & 56 & \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: ICC is measured with all outputs open and all inputs grounded.
Switching Characteristics at \(\mathrm{V}_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Data to Output & & 36 & ns \\
\hline tPHL & Propagation Delay Time High to Low Level Output & Data to Output & & 33 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Strobe to Output & & 30 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Strobe to Output & & 27 & ns \\
\hline
\end{tabular}

Function Table
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{6}{|c|}{Inputs} & \multicolumn{16}{|c|}{Outputs} \\
\hline G1 & G2 & D & C & B & A & 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12 & 13 & 14 & 15 \\
\hline L & L & L & L & L & L & L & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline \(L\) & L & L & L & L & H & H & L & H & H & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline L & L & L & L & H & L & H & H & L & H & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline L & \(L\) & \(L\) & L & H & H & H & H & H & L & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline L & L & \(L\) & H & \(L\) & L & H & H & H & H & L & H & H & H & H & H & H & H & H & H & H & H \\
\hline \(L\) & L & \(L\) & H & L & H & H & H & H & H & H & L & H & H & H & H & H & H & H & H & H & H \\
\hline \(L\) & L & \(L\) & H & H & L & H & H & H & H & H & H & L & H & H & H & H & H & H & H & H & H \\
\hline L & L & L & H & H & H & H & H & H & H & H & H & H & L & H & H & H & H & H & H & H & H \\
\hline L & L & H & L & L & L & H & H & H & H & H & H & H & H & L & H & H & H & H & H & H & H \\
\hline L & L & H & L & L & H & H & H & H & H & H & H & H & H & H & L & H & H & H & H & H & H \\
\hline L & L & H & L & H & L & H & H & H & H & H & H & H & H & H & H & L & H & H & H & H & H \\
\hline L & \(L\) & H & L & H & H & H & H & H & H & H & H & H & H & H & H & H & L & H & H & H & H \\
\hline L & \(L\) & H & H & L & L & H & H & H & H & H & H & H & H & H & H & H & H & L & H & H & H \\
\hline \(L\) & L & H & H & L & H & H & H & H & H & H & H & H & H & H & H & H & H & H & L & H & H \\
\hline L & L & H & H & H & L & H & H & H & H & H & H & H & H & H & H & H & H & H & H & L & H \\
\hline L & L & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H & L \\
\hline L & H & X & X & X & X & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline H & L & X & \(X\) & \(X\) & \(X\) & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline H & H & X & X & X & X & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline
\end{tabular}
\(\mathrm{H}=\) High Level, \(L=\) Low Level, \(X=\) Don't Care

\section*{Logic Diagram}


TL/F/6548-2

\section*{DM54155/DM74155 Dual 2-Line to 4-Line Decoders/Demultiplexers}

\section*{General Description}

These TTL circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4 -bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied at C2 is true through its outputs. The inverter following the C 1 data input permits use as a 3-to-8-line decoder, or 1-to-8-line demultiplexer, without external gating.

Input clamping diodes are provided on these circuits to minimize transmission-line effects and simplify system design.

\section*{Features}
- Applications:

Dual 2-to-4-line decoder
Dual 1-to-4-line demultiplexer
3-to-8-line decoder
1-to-8-line demultiplexer
- Individual strobes simplify cascading for decoding or demultiplexing larger words
- Input clamping diodes simplify system design

Connection Diagram and Function Tables


TL/F/6549-1
Order Number DM54155J, DM54155W or DM74155N See NS Package Number J16A, N16A or W16A
†C = inputs C1 and C2 connected together
\(\ddagger \mathrm{G}=\) inputs G 1 and G 2 connected together
\(H=\) high level, \(L=\) low level, \(X=\) don't care

2-Line-to-4-Line Decoder or 1-Line-to-4-Line Demultiplexer
\begin{tabular}{|cc|c|c|cccc|}
\hline \multicolumn{4}{|c|}{ Inputs } & \multicolumn{4}{c|}{ Outputs } \\
\cline { 1 - 4 } Select & Strobe & Data & & & & \\
\cline { 1 - 3 } B & A & G1 & C1 & 1Yo & 1Y1 & 1Y2 & 1Y3 \\
\cline { 1 - 7 } X & X & H & X & H & H & H & H \\
L & L & L & H & L & H & H & H \\
L & H & L & H & H & L & H & H \\
H & L & L & H & H & H & L & H \\
H & H & L & H & H & H & H & L \\
X & X & X & L & H & H & H & H \\
\hline
\end{tabular}
\begin{tabular}{|cc|c|c|cccc|}
\hline \multicolumn{4}{|c|}{ Inputs } & \multicolumn{4}{c|}{ Outputs } \\
\cline { 1 - 3 } Select & Strobe & Data & & & & \\
\cline { 1 - 3 } B & A & G2 & C2 & 2Yo & 2Y1 & 2Y2 & 2Y3 \\
\cline { 1 - 7 } X & X & H & X & H & H & H & H \\
L & L & L & L & L & H & H & H \\
L & H & L & L & H & L & H & H \\
H & L & L & L & H & H & L & H \\
H & H & L & L & H & H & H & L \\
X & X & X & H & H & H & H & H \\
\hline
\end{tabular}

3-Line-to-8-Line Decoder or 1-Line-to-8-Line Demultiplexer
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{2}{|l|}{Inputs} & \multicolumn{8}{|c|}{Outputs} \\
\hline Select & Strobe Or Data & (0) & (1) & (2) & (3) & (4) & (5) & (6) & (7) \\
\hline \(\mathbf{C} \dagger\) B A & G \(\ddagger\) & 2 YO & 2Y1 & 2 Y 2 & 2 Y 3 & 1 YO & 1Y1 & 1Y2 & 1 Y 3 \\
\hline X \(\times \mathrm{X}\) & H & H & H & H & H & H & H & H & H \\
\hline L L L & L & L & H & H & H & H & H & H & H \\
\hline L L H & L & H & L & H & H & H & H & H & H \\
\hline L HL & L & H & H & L & H & H & H & H & H \\
\hline L H H & L & H & H & H & L & H & H & H & H \\
\hline H L L & L & H & H & H & H & L & H & H & H \\
\hline H L H & L & H & H & H & H & H & L & H & H \\
\hline H H L & L & H & H & H & H & H & H & L & H \\
\hline HHH & L & H & H & H & H & H & H & H & L \\
\hline
\end{tabular}
\begin{tabular}{lr} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage & 7 V \\
Input Voltage & \(5.5^{2} \mathrm{~V}\) \\
Operating Free Air Temperature Range & \\
DM54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54155} & \multicolumn{3}{|c|}{DM74155} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline loL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
(Note 1) & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline V OH & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{l}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& \text { (Note 2) }
\end{aligned}
\]} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline \multirow[t]{2}{*}{Icc} & \multirow[t]{2}{*}{Supply Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=\text { Max } \\
& \text { (Note 3) }
\end{aligned}
\]} & DM54 & & 25 & 35 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & & 25 & 40 & \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, T_{A}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: \(\mathrm{I}_{\mathrm{CC}}\) is measured with the outputs open, \(\mathrm{A}, \mathrm{B}\), and C 1 inputs at 4.5 V , and \(\mathrm{C} 2, \mathrm{G} 1\), and G 2 inputs grounded.

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
\begin{gathered}
\mathrm{A}, \mathrm{~B}, \mathrm{C} 2, \mathrm{G} 1 \\
\text { or } \mathrm{G} 2 \text { to } \mathrm{Y}
\end{gathered}
\] & & 20 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
\begin{aligned}
& \mathrm{A}, \mathrm{~B}, \mathrm{C} 2, \mathrm{G} 1 \\
& \text { or } \mathrm{G} 2 \text { to } \mathrm{Y}
\end{aligned}
\] & & 27 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \(A\) or \(B\) to \(Y\) & & FSC & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & A or B to \(Y\) & & 32 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
\begin{aligned}
& \mathrm{C} 1 \\
& \text { to } \mathrm{Y}
\end{aligned}
\] & & 24 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
\begin{aligned}
& \mathrm{C} 1 \\
& \text { to } \mathrm{Y}
\end{aligned}
\] & & 27 & ns \\
\hline
\end{tabular}

Logic Diagram


TL/F/6549-2

National Semiconductor

\section*{54157/DM54157/DM74157}

Quad 2-Line to 1-Line Data Selectors/Multiplexers

\section*{General Description}

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs.

\section*{Applications}
- Expand any data input point
- Multiplex dual data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

\section*{Features}
- Buffered inputs and outputs
- Typical propagation time 9 ns
- Typical power dissipation 150 mW
- Alternate Military/Aerospace device (54157) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

\section*{Connection Diagram}


TL/F/6550-1
Order Number 54157DMQB, 54157FMQB, DM54157J, DM54157W or DM74157N See NS Package Number J16A, N16E or W16A

\section*{Function Table}
\begin{tabular}{|c|c|c|c|c|}
\hline \multicolumn{5}{|c|}{ Inputs } \\
\multirow{2}{*}{ Output Y } \\
\hline Strobe & Select & A & B & \\
\hline H & X & X & X & L \\
L & L & L & X & L \\
L & L & H & X & H \\
L & H & X & L & L \\
L & H & X & H & H \\
\hline
\end{tabular}

\footnotetext{
\(H=\) High Level, L = Low Level, X = Don't Care
}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{9}{|l|}{Absolute Maximum Ratings (Note)} \\
\hline \multicolumn{4}{|l|}{If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.} & \multicolumn{5}{|l|}{Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The} \\
\hline \multicolumn{2}{|l|}{Supply Voltage} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{7V par}} & \multicolumn{5}{|l|}{\multirow[t]{2}{*}{parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define}} \\
\hline \multicolumn{2}{|l|}{Input Voltage} & & & & & & & \\
\hline \multicolumn{2}{|l|}{DM54 and 54
DM74} & \(+125^{\circ}\)
\(+70^{\circ}\) & \multicolumn{6}{|r|}{the conditions for actual device operation.} \\
\hline \multicolumn{2}{|l|}{Storage Temperature Range} & \(+150^{\circ}\) & & & & & & \\
\hline \multicolumn{9}{|l|}{Recommended Operating Conditions} \\
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54157} & \multicolumn{3}{|c|}{DM74157} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline TA & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{I}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline IIH & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline 1 l & Low Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& (\text { Note } 2)
\end{aligned}
\]} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 3)} & & 30 & 48 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: ICC is measured with 4.5 V applied to all inputs and all outputs open.

Switching Characteristics at \(\mathrm{V}_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \({ }_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output & Data to \(Y\) & & 14 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to \(Y\) & & 14 & ns \\
\hline tplH & Propagation Delay Time Low to High Level Output & Strobe to \(Y\) & & 20 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Strobe to \(Y\) & & 21 & ns \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & Select to \(Y\) & & 23 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Select to \(Y\) & & 27 & ns \\
\hline
\end{tabular}

\section*{Logic Diagram}


National Semiconductor

\section*{54161/DM54161A/DM74161A DM54163A/DM74163A Synchronous 4-Bit Counters}

\section*{General Description}

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 161A and 163A are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flipflops clocked simultaneously so that the outputs change coincident with each other when so instructed by the countenable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.
These counters are fully programmable; that is. the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable input. Low-to-high transitions at the load input of the 161A and 163A are perfectly acceptable, regardless of the logic levels on the clock or enable inputs. The clear function for the 161A is asynchronous; and a low level at the clear input sets all four of the flip-flop outputs low, regardless of the levels of clock, load, or enable inputs. The clear function for the 163A is synchronous; and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate out-
put is connected to the clear input to synchronously clear the counter to all low outputs. Low-to-high transitions at the clear input of the 163A are also permissible, regardless of the logic levels on the clock, enable, or load inputs.
The carry look-ahead circuitry provides for cascading counters for \(n\)-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both countenable inputs ( \(P\) and \(T\) ) must be high to count, and input \(T\) is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the \(Q_{A}\) output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable \(P\) or \(T\) inputs of the 161A through 163A may occur, regardless of the logic level on the clock.

\section*{Features}
- Synchronously programmable

Internal look-ahead for fast counting
(0arry output for n-bit cascading
■ Synchronous counting
- Load control line
. Diode-clamped inputs
( Alternate Military/Aerospace device (54161) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

\section*{Connection Diagram}


TL/F/6551-1
Order Number 54161DMQB, 54161FMQB, DM54161AJ, DM54161AW, DM54163AJ, DM54163AW, DM74161AN or DM74163AN See NS Package Number J16A, N16E or W16A
\begin{tabular}{lr} 
Absolute Maximum Ratings（Note） \\
If Military／Aerospace specified devices are required， \\
please contact the National Semiconductor Sales \\
Office／Distributors for availability and specification． \\
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM54 and 54 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
DM74 & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note：The＂Absolute Maximum Ratings＂are those values beyond which the safety of the device cannot be guaran－ teed．The device should not be operated at these limits．The parametric values defined in the＂Electrical Characteristics＂ table are not guaranteed at the absolute maximum ratings． The＂Recommended Operating Conditions＂table will define the conditions for actual device operation．

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|l|}{DM54161A and 163A} & \multicolumn{3}{|l|}{DM74161A and 163A} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
\hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & －0．8 & & & －0．8 & mA \\
\hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & & & 16 & mA \\
\hline \({ }^{\text {f CLK }}\) & \multicolumn{2}{|l|}{Clock Frequency（Note 6）} & 0 & & 25 & 0 & & 25 & MHz \\
\hline \multirow[t]{2}{*}{\(t_{W}\)} & \multirow[t]{2}{*}{Pulse Width （Note 6）} & Clock & 25 & & & 25 & & & \multirow[t]{2}{*}{ns} \\
\hline & & Clear & 20 & & & 20 & & & \\
\hline \multirow[t]{4}{*}{tsu} & \multirow[t]{4}{*}{Setup Time （Note 6）} & Data & 20 & & & 20 & & & \multirow{4}{*}{ns} \\
\hline & & Enable P & 34 & & & 34 & & & \\
\hline & & Load & 25 & & & 25 & & & \\
\hline & & Clear（Note 5） & 20 & & & 20 & & & \\
\hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Hold Time（Note 6）} & 0 & & & 0 & & & ns \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & －55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics}

Over recommended operating free air temperature range（unless otherwise noted）
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ （Note 1） & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & －1．5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current＠Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{3}{*}{\(I_{1 H}\)} & \multirow[t]{3}{*}{High Level Input Current} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=2.4 V
\end{aligned}
\]} & Enable T & & & 80 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Clock & & & 80 & \\
\hline & & & Others & & & 40 & \\
\hline \multirow[t]{3}{*}{ILL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=\operatorname{Max} \\
& V_{1}=0.4 V
\end{aligned}
\]} & Enable T & & & －3．2 & \multirow{3}{*}{mA} \\
\hline & & & Clock & & & －3．2 & \\
\hline & & & Others & & & －1．6 & \\
\hline
\end{tabular}

\section*{Electrical Characteristics}

Over recommended operating free air temperature range (unless otherwise noted) (Continued)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \begin{tabular}{l}
Symbol \\
los
\end{tabular} & \begin{tabular}{l}
Parameter \\
Short Circuit Output Current
\end{tabular} & \multicolumn{2}{|c|}{Conditions} & \multirow[t]{2}{*}{\[
\begin{gathered}
\text { Min } \\
\hline-20 \\
\hline
\end{gathered}
\]} & \multirow[t]{2}{*}{Typ (Note 1)} & \multirow[t]{2}{*}{\[
\frac{\text { Max }}{-57}
\]} & Units \\
\hline \multirow[t]{2}{*}{} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& (\text { Note 2) }
\end{aligned}
\]} & DM54 & & & & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -20 & & -57 & \\
\hline ICCH & Supply Current & \[
\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}
\] & DM54 & & 59 & 85 & mA \\
\hline & ts High & (Note 3) & DM74 & & 59 & 94 & \\
\hline ICCL & Supply Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) & DM54 & & 63 & 91 & A \\
\hline & with Outputs Low & (Note 4) & DM74 & & 63 & 101 & \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: \(I_{C C H}\) is measured with the LOAD high, then again with the LOAD low, with all inputs high and all outputs open.
Note 4: ICCL is measured with the CLOCK high, then again with the CLOCK input low, with all inputs low and all outputs open.
Note 5: Applies to '163A which has synchronous clear inputs.
Note 6: \(T_{A}=25^{\circ} \mathrm{C}\) and \(V_{C C}=5 \mathrm{~V}\).
Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 25 & & MHz \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Ripple Carry & & 27 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Ripple Carry & & 24 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock (Load High) to Q & & 20 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock (Load High) to Q & & 32 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock (Load Low) to Q & & 21 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock (Load Low) to Q & & 32 & ns \\
\hline \({ }^{\text {PLLH }}\) & Propagation Delay Time Low to High Level Output & Enable T to Ripple Carry & & 16 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Enable T to Ripple Carry & & 16 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
\begin{gathered}
\text { Clear (Note 7) } \\
\text { to } \mathrm{Q} \\
\hline
\end{gathered}
\] & & 36 & ns \\
\hline
\end{tabular}

Note 7: Propagation delay for clearing is measured from the clear input for the 161A or from the clock input transition for the 163A.

Logic Diagrams




\section*{Parameter Measurement Information}


TL/F/6551-6
Note A: The input pulses are supplied by generators having the following characteristics: PRR \(\leq 1 \mathrm{MHz}\), duty cycle \(\leq 50 \%\), \(\mathrm{Z}_{\mathrm{OUT}} \approx 50 \Omega\). For 161 A and 163 A , \(\mathrm{t}_{\mathrm{r}} \leq 10 \mathrm{~ns}, \mathrm{t}_{\mathrm{f}} \leq 10 \mathrm{~ns}\). Vary PRR to measure \(f_{\text {max }}\).
Note B: Outputs \(Q_{D}\) and carry are tested at \(t_{n+16}\) for \(161 A, 163 A\) where \(t_{n}\) is the bit time when all outputs are low.
Note C: For 161A and 163A, \(V_{\text {REF }}=1.5 \mathrm{~V}\).

\section*{Parameter Measurement Information (Continued)}


TL/F/6551-7
Note A: The input pulses are supplied by generators having the following characteristics: PRR \(\leq 1 \mathrm{MHz}\), duty cycle \(\leq 50 \%\), Zout \(\approx 50 \Omega\). For 161 A and \(163 A, t_{f} \leq 10 \mathrm{~ns}, \mathrm{t}_{\mathrm{f}} \leq 10 \mathrm{~ns}\). Vary PRR to measure \(f_{\text {max }}\).
Note B: Enable \(P\) and enable \(T\) setup times are measured at \(t_{n+0}\).
Note C: For 161A and 163A, \(V_{\text {REF }}=1.5 \mathrm{~V}\).

\section*{54164/DM74164}

\section*{8-Bit Serial In/Parallel Out Shift Registers}

\section*{General Description}

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either serial input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

\section*{Connection Diagram}


TL/F/6552-1
Order Number 54164DMQB, 54164FMQB or DM74164N See NS Package Number J14A, N14A or W14B

\section*{Features}
(1) Gated (enable/disable) serial inputs

国 Fully buffered clock and serial inputs
- Asynchronous clear
- Typical clock frequency 36 MHz
- Typical power dissipation 185 mW

Function Table
\begin{tabular}{|c|c|cc|cccc|}
\hline \multicolumn{5}{|c|}{ Inputs } & \multicolumn{5}{c|}{ Outputs } \\
\hline Clear & Clock & \(\mathbf{A}\) & \(\mathbf{B}\) & \(\mathbf{Q}_{\mathbf{A}}\) & \(\mathbf{Q}_{\mathbf{B}}\) & \(\ldots\) & \(\mathbf{Q}_{\boldsymbol{H}}\) \\
\hline L & X & X & X & L & L & \(\ldots\) & L \\
H & L & X & X & \(\mathrm{Q}_{\mathrm{AO}}\) & \(\mathrm{Q}_{\mathrm{B} 0}\) & \(\ldots\) & \(\mathrm{Q}_{\mathrm{H} 0}\) \\
H & \(\uparrow\) & H & H & H & \(\mathrm{Q}_{\mathrm{An}}\) & \(\ldots\) & \(\mathrm{Q}_{\mathrm{Gn}}\) \\
\(H\) & \(\uparrow\) & L & X & L & \(\mathrm{Q}_{\mathrm{An}}\) & \(\ldots\) & \(\mathrm{Q}_{\mathrm{Gn}}\) \\
H & \(\uparrow\) & X & L & L & \(\mathrm{Q}_{\mathrm{An}}\) & \(\ldots\) & \(\mathrm{Q}_{\mathrm{Gn}}\) \\
\hline
\end{tabular}
\(H=\) High Level (steady state), L = Low Level (steady state)
\(X=\) Don't Care (any input, including transitions)
\(\uparrow=\) Transition from low to high level
\(Q_{A 0}, Q_{B 0}, Q_{H 0}=\) The level of \(Q_{A}, Q_{B}\), or \(Q_{H}\), respectively, before the indicated steady-state input conditions were established.
\(Q_{A n}, Q_{G n}=\) The level of \(Q_{A}\) or \(Q_{G}\) before the most recent \(\uparrow\) transition of the clock; indicates a one-bit shift.
\begin{tabular}{lr} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \\
54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{54164} & \multicolumn{3}{|c|}{DM74164} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
\hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & & & -0.4 & mA \\
\hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 8 & & & 8 & mA \\
\hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 4)} & & & 25 & 0 & & 25 & MHz \\
\hline \multirow[t]{2}{*}{tw} & \multirow[t]{2}{*}{Pulse Width (Note 4)} & Clock & 20 & & & 20 & & & \multirow[t]{2}{*}{ns} \\
\hline & & Clear & 20 & & & 20 & & & \\
\hline tsu & \multicolumn{2}{|l|}{Data Setup Time (Note 4)} & 15 & & & 15 & & & ns \\
\hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Data Hold Time (Note 4)} & 0 & & & 5 & & & ns \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|r|}{Conditions} & Min & Typ
(Note 1) & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Min}, l_{1}=-14 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.2 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=M i n, I_{O L}=M a x \\
& V_{I H}=M i n, V_{I L}=M a x
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline  & Low Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& (\text { Note 2) }
\end{aligned}
\]} & 54 & -10 & & -27.5 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -9 & & -27.5 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 3)} & & 37 & 54 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: \(\mathrm{I}_{\mathrm{CC}}\) is measured with all outputs open, SERIAL inputs grounded, the CLOCK input at 2.4 V , and a momentary ground, then 4.5 V , applied to the CLEAR input. Note 4: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{C}}=5 \mathrm{~V}\).

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=\mathbf{8 0 0 \Omega}\)} & \multirow{3}{*}{Units} \\
\hline & & & \multicolumn{2}{|r|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}\)} & \\
\hline & & & Min & Max & Min & Max & \\
\hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 25 & & & & MHz \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Output & & 27 & & 30 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Output & & 32 & & 37 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clear to Output & & 36 & & 42 & ns \\
\hline
\end{tabular}

\section*{Logic Diagram}


\section*{Timing Diagram}


National Semiconductor

\section*{54165/DM74165}

\section*{8-Bit Parallel-to-Serial Converter}

\section*{General Description}

The '165 is an 8-bit parallel load or serial-in register with complementary outputs available from the last stage. Parallel inputting occurs asynchronously when the Parallel Load ( \(\overline{\mathrm{PL}}\) ) input is LOW. With \(\overline{\text { PL HIGH, serial shifting occurs on }}\)
the rising edge of the clock; new data enters via the Serial Data (DS) input. The 2-input OR clock can be used to combine two independent clock sources, or one input can act as an active LOW clock enable.

\section*{Connection Diagram}

Dual-In-Line-Package


Logic Symbol


Order Number 54165DMQB, 54165FMQB or DM74165N See NS Package Number J16A, N16E or W16A
\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
\hline CP1, CP2 & Clock Pulse Inputs (Active Rising Edge) \\
\(\mathrm{D}_{\mathbf{S}}\) & Serial Data Input \\
\(\overline{\text { PL }}\) & Asynchronous Parallel Load Input \\
& (Active LOW) \\
P0-P7 & Parallel Data Inputs \\
Q7 & Serial Output from Last Stage \\
Q7 & Complementary Output \\
\hline
\end{tabular}


\section*{Electrical Characteristics}

Over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) } \\
\hline
\end{gathered}
\] & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{OH}}=\mathrm{Max}, \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}\)} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{V}_{I H}=\mathrm{Min}\)} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{2}{*}{\({ }_{1} \mathrm{H}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=2.4 \mathrm{~V}\)} & PL & & & 80 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Inputs & & & 40 & \\
\hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & \(\overline{\text { PL }}\) & & & -3.2 & \multirow[t]{2}{*}{mA} \\
\hline & & & Inputs & & & -1.6 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& (\text { Note 2) }
\end{aligned}
\]} & 54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=M a x, \overline{P L}=V \\
& P_{n}=\neg, C P_{1}, C P_{2}=4.5 \mathrm{~V}
\end{aligned}
\]} & & & 63 & mA \\
\hline
\end{tabular}

Switching Characteristics
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\[
\begin{aligned}
& C_{L}=15 \mathrm{pF} \\
& R_{L}=400 \Omega
\end{aligned}
\]} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \(f_{\text {max }}\) & Maximum Clock Frequency & 20 & & MHz \\
\hline \[
t_{P L H}
\]
\[
\mathrm{t}_{\mathrm{PHL}}
\] & Propagation Delay \(\overline{\text { PL to }}\) Q7 or \(\overline{\text { Q }} 7\) & & \[
\begin{aligned}
& 31 \\
& 40 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& t_{\mathrm{PLH}} \\
& t_{\mathrm{PHL}}
\end{aligned}
\] & Propagation Delay CP1 to Q7 or Q7 & & \[
\begin{aligned}
& 24 \\
& 31 \\
& \hline
\end{aligned}
\] & ns \\
\hline \begin{tabular}{l}
\(t_{\text {PLH }}\) \\
\(t_{\text {PHL }}\)
\end{tabular} & Propagation Delay P7 to Q7 & & \[
\begin{aligned}
& 17 \\
& 36
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLLH}} \\
& \mathrm{t}_{\mathrm{PHL}}
\end{aligned}
\] & Propagation Delay P7 to \(\bar{Q} 7\) & & \[
\begin{aligned}
& 27 \\
& 27 \\
& \hline
\end{aligned}
\] & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{Functional Description}

The '165 contains eight clocked master/slave RS flip-flops connected as a shift register with auxiliary gating to provide overriding asynchronous parallel entry. Parallel data enters when the \(\overline{\mathrm{PL}}\) signal is LOW. The parallel data can change while \(\overline{\mathrm{PL}}\) is LOW provided that the recommended setup and hold times are observed.
For clocked operation, \(\overline{\text { PL }}\) must be HIGH. The two clock inputs perform identically; one can be used as a clock inhibit
by applying a HIGH signal. To avoid double clocking, however, the inhibit signal should only go HIGH while the clock is HIGH. Otherwise, the rising inhibit signal will cause the same response as a rising clock edge. The flip-flops are edge-triggered for serial operations. The serial input data can change at any time, provided only that the recommended setup and hold times are observed, with respect to the rising edge of the clock.

\section*{Truth Table}
\begin{tabular}{|l|cc|cccccccc|l|}
\hline \multirow{2}{*}{ PL } & \multicolumn{2}{|c|}{ CP } & \multicolumn{8}{|c|}{ Contents } & \multirow{2}{*}{ Response } \\
\cline { 2 - 10 } & \(\mathbf{1}\) & 2 & Q0 & Q1 & Q2 & Q3 & Q4 & Q5 & Q6 & Q7 & \\
\hline L & X & X & P0 & P1 & P2 & P3 & P4 & P5 & P6 & P7 & Parallel Entry \\
H & L & - & DS & Q0 & Q1 & Q2 & Q3 & Q4 & Q5 & Q6 & Right Shift \\
H & H & - & Q0 & Q1 & Q2 & Q3 & Q4 & Q5 & Q6 & Q7 & No Change \\
H & - & L & DS & Q0 & Q1 & Q2 & Q3 & Q4 & Q5 & Q6 & Right Shift \\
H & - & H & Q0 & Q1 & Q2 & Q3 & Q4 & Q5 & Q6 & Q7 & No Change \\
\hline
\end{tabular}
\(H=\) HIGH Voltage Level
L = LOW Voltage Level
\(X=\) Immaterial
\(\Omega=\) Positive Rising Edge

\section*{Logic Diagram}


TL/F/9782-3

\section*{DM54166}

\section*{8-Bit Parallel In/Serial Out Shift Registers}

\section*{General Description}

These parallel-in or serial-in, serial-out shift registers feature gated clock inputs and an overriding clear input. All inputs are buffered to lower the drive requirements to one normalized load, and input clamping diodes minimize switching transients to simplify system design. The load mode is established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on
the low-to-high-level edge of the clock pulse through a twoinput NOR gate, permitting one input to be used as a clockenable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be freerunning, and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

\section*{Connection Diagram}


\section*{Function Table}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{6}{|c|}{Inputs} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Internal Outputs}} & \multirow[b]{3}{*}{} \\
\hline \multirow[t]{2}{*}{Clear} & \multirow[t]{2}{*}{Shift/ Load} & \multirow[t]{2}{*}{Clock Inhiblt} & \multirow[t]{2}{*}{Clock} & \multirow[t]{2}{*}{Serial} & Parallel & & & \\
\hline & & & & & A...H & \(\mathbf{Q}_{\mathbf{A}}\) & \(\mathrm{Q}_{\mathrm{B}}\) & \\
\hline L & X & X & X & X & X & L & L & L \\
\hline H & X & L & L & \(x\) & X & \(Q_{A 0}\) & \(Q_{B 0}\) & Q HO \\
\hline H & L & \(L\) & \(\uparrow\) & X & a...h & a & b & h \\
\hline H & H & \(L\) & \(\uparrow\) & H & X & H & \(Q_{\text {An }}\) & \(Q_{G n}\). \\
\hline H & H & \(L\) & \(\uparrow\) & L & X & L & \(Q_{\text {An }}\) & \(Q_{G n}\) \\
\hline H & X & H & 个 & X & X & \(Q_{A O}\) & \(Q_{B O}\) & \(Q_{H 0}\) \\
\hline
\end{tabular}

\footnotetext{
\(H=\) High Level (steady state), L = Low Level (steady state)
\(X=\) Don't Care (any input, including transitions)
\(\uparrow=\) Transition from Low to High Level
a \(. . . h=\) The level of stead-state input at inputs \(A\) through \(H\), respectively
\(Q_{A O}, Q_{B O}, Q_{H O}=\) The level of \(Q_{A}, Q_{B}, Q_{H}\), respectively, before the indicated steady-state input conditions were established
\(Q_{A n}, Q_{G n}=\) The level of \(Q_{A}, Q_{G}\), respectively, before the most recent \(\uparrow\) transition of the clock
}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54166} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & \\
\hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & V \\
\hline \(\mathrm{lOH}^{2}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.8 & mA \\
\hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & mA \\
\hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 4)} & 0 & & 25 & MHz \\
\hline \multirow[t]{2}{*}{tw} & \multirow[t]{2}{*}{Pulse Width (Note 4)} & Clock & 24 & & & \multirow[t]{2}{*}{ns} \\
\hline & & Clear & 20 & & & \\
\hline \multirow[t]{2}{*}{tsu} & \multirow[t]{2}{*}{Setup Time (Note 4)} & Mode & 30 & & & \multirow[t]{2}{*}{ns} \\
\hline & & Data & 20 & & & \\
\hline \(t_{H}\) & \multicolumn{2}{|l|}{Data Hold Time (Note 4)} & 0 & & & ns \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOH}_{\mathrm{OH}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\] & 2.4 & & & V \\
\hline VOL & Low Level Output Voltage & \[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(V_{C C}=\) Max, \(\mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{I}_{\mathrm{IL}}\) & Low Level Input Current & \(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline los & Short Circuit Output Current & \(V_{C C}=\operatorname{Max}\) (Note 2) & -20 & & -57 & mA \\
\hline Icc & Supply Current & \(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 3) & & 72 & 104 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: With all outputs open, 4.5 V applied to the SERIAL input, all other inputs except CLOCK grounded, ICc is measured after a momentary ground, then 4.5 V , is applied to the CLOCK.
Note 4: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).


Logic Diagram


Timing Diagram
Typical Clear, Shift, Load, Inhibit, and Shift Sequences


TL/F/6554-3

\section*{Parameter Measurement Information}

\section*{Voltage Waveforms}


TL/F/6554-4
Test Table for Synchronous Inputs
\begin{tabular}{|c|c|c|}
\hline \begin{tabular}{c} 
Data Input \\
For Test
\end{tabular} & Shift/Load & \begin{tabular}{c} 
Output Tested \\
(See Note C)
\end{tabular} \\
\hline\(H\) & 0 V & \(Q_{H}\) at \(T_{N}+1\) \\
Serial Input & 4.5 V & \(Q_{H}\) at \(T_{N}+8\) \\
\hline
\end{tabular}

Note A: The clock pulse has the following characteristics:
\(t_{W}\) (clock) \(\geq 20 \mathrm{~ns}\) and PRR \(=1 \mathrm{MHz}\).
The clear pulse has the following characteristics:
\(t_{W \text { (clear) }} \geq 20 \mathrm{~ns}\) and \(\mathrm{t}_{\text {HOLD }}=0 \mathrm{~ns}\).
When testing \(\mathrm{f}_{\mathrm{MAX}}\), vary the clock PRR.
Note B: A clear pulse is applied prior to each test.
Note C: Propagation delay times ( \(t_{\text {PLH }}\) and \(t_{\text {PHL }}\) ) are measured at \(t_{n}+1\). Proper shifting of data is verified at \(t_{n}+8\) with a functional test.
Note \(\mathbf{D}: \mathrm{t}_{\mathrm{n}}=\) bit time before clocking transition.
\(t_{n+1}=\) bit time after one clocking transition.
\(t_{n}+8=\) bit time after eight clocking transitions.
Note E: \(\mathrm{V}_{\mathrm{REF}}=1.5 \mathrm{~V}\) for 166.

\section*{54170/DM74170}

\section*{\(4 \times 4\) Register File}

\section*{with Open-Collector Outputs}

\section*{General Description}

The '170 contains 16 high speed, low power, transparent D-type latches arranged as four words of four bits each, to function as a \(4 \times 4\) register file. Separate read and write inputs, both address and enable, allow simultaneous read and write operation. Open-collector outputs make it possible to connect up to 128 outputs in a wired-AND configuration to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an \(n\)-bit length.

\section*{Connection Diagram}


Logic Symbol


TL/F/9783-2
\(V_{C C}=\operatorname{Pin} 16\)
GND \(=\operatorname{Pin} 8\)

TL/F/9783-1
Order Number 54170DMQB, 54170FMQB or DM74170N See NS Package Number J16A, N16E and W16A
\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
\hline D1-D4 & Data Inputs \\
WA0, WA1 & Write Address Inputs \\
\(\overline{W E}\) & Write Enable Input (Active LOW) \\
RA0-RA1 & Read Address Inputs \\
\(\overline{R E}\) & Read Enable Input (Active LOW) \\
\(O 1-O 4\) & Data Outputs \\
\hline
\end{tabular}
\begin{tabular}{|c|c|}
\hline \begin{tabular}{l}
Absolute Maximum Ratin \\
If Military/Aerospace specified devic please contact the National Semi Office/Distributors for availability and
\end{tabular} & \begin{tabular}{l}
ngs \\
ces are required, conductor Sales specifications.
\end{tabular} \\
\hline Supply Voltage & V \\
\hline Input Voltage & 5.5 V \\
\hline Operating Free Air Temperature Range & \\
\hline 54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
\hline DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
\hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ}\) \\
\hline
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{54170} & \multicolumn{3}{|c|}{DM74170} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & & & 5.5 & & & & V \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline \(\mathrm{t}_{\text {s }}\) & Setup Time HIGH or LOW \(\mathrm{D}_{\mathrm{n}}\) to Rising \(\overline{\mathrm{WE}}\) & 10 & & & 10 & & & ns \\
\hline \(t_{h}\) & Hold Time HIGH or LOW \(D_{n}\) to Rising \(\overline{W E}\) & 15 & & & 15 & & & ns \\
\hline \(t_{s}\) & Setup Time HIGH or LOW \(W A_{n}\) to Falling \(\overline{W E}\) & 15 & & & 15 & & & ns \\
\hline \(t_{n}\) & Hold Time HIGH or LOW \(W A_{n}\) to Rising \(\overline{W E}\) & 5.0 & & & 5.0 & & & ns \\
\hline \(t_{w}(L)\) & \(\overline{\text { WE }}\) or \(\overline{R E}\) Pulse Width LOW & 25 & & & 25 & & & ns \\
\hline
\end{tabular}

\section*{Electrical Characteristics}

Over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \begin{tabular}{l}
Typ \\
(Note 1)
\end{tabular} & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline IOH & High Level Output Current & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{V}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & & 30 & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min}, I_{O L}=M a x \\
& V_{I H}=\operatorname{Min}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{I}_{\mathrm{LL}}\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{Icc} & \multirow[t]{2}{*}{Supply Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x, R A_{n}=0 V \\
& D_{n}, \overline{W E}, \overline{R E}=4.5 \mathrm{~V}
\end{aligned}
\]} & 54 & & & 140 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & & & 150 & \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
\begin{tabular}{|c|c|c|c|c|}
\hline \multicolumn{5}{|l|}{\begin{tabular}{l}
Switching Characteristics \\
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 2 for waveforms and load configurations)
\end{tabular}} \\
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{\[
\begin{gathered}
\text { 54/DM74 } \\
\hline C_{L}=15 \mathrm{pF} \\
\mathrm{R}_{\mathrm{L}}=400 \Omega
\end{gathered}
\]}} & \multirow{3}{*}{Units} \\
\hline & & & & \\
\hline & & Min & Max & \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{pLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay* \(\mathrm{RA}_{0}\) or \(\mathrm{RA}_{1}\) to \(\mathrm{O}_{\mathrm{n}}\) & & \[
\begin{aligned}
& 35 \\
& 40
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay \(\overline{R E}\) to \(\mathrm{O}_{\mathrm{n}}\) & & \[
\begin{aligned}
& 15 \\
& 30 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay \(\overline{W E}\) to \(\mathrm{O}_{\mathrm{n}}\) & & \[
\begin{array}{r}
40 \\
45 \\
\hline
\end{array}
\] & ns \\
\hline \[
\begin{aligned}
& t_{\mathrm{PLH}} \\
& t_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay
\[
\mathrm{D}_{\mathrm{n}} \text { to } \mathrm{O}_{\mathrm{n}}
\] & & \[
\begin{aligned}
& 30 \\
& 45 \\
& \hline
\end{aligned}
\] & ns \\
\hline
\end{tabular}
*Measured at least 25 ns after entry of new data at selected location.

\section*{Timing Waveforms}


\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{4}{|c|}{Write Function Table} & \multicolumn{4}{|c|}{Read Function Table} \\
\hline \multicolumn{3}{|c|}{Write Inputs} & \multirow[t]{2}{*}{D Inputs To} & & ad In & & Outputs From \\
\hline \(\overline{W E}\) & \(W^{W} A_{1}\) & WA0 & & \(\overline{R E}\) & \(\mathrm{RA}_{1}\) & RA \({ }_{0}\) & \\
\hline L & L & L & Word 0 & L & L & L & Word 0 \\
\hline L & L & H & Word 1 & L & L & H & Word 1 \\
\hline L & H & L & Word 2 & L & H & L & Word 2 \\
\hline L & H & H & Word 3 & L & H & H & Word 3 \\
\hline H & X & X & None (Hold) & H & X & X & None (HIGH Z) \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{H}=\mathrm{HIGH}\) Voltage Level} & - LOW Voltage Level & & erial & \\
\hline
\end{tabular}

\section*{54173/DM54173/DM74173 TRI-STATE \({ }^{\circledR}\) Quad D Registers}

\section*{General Description}

These four-bit registers contain D-type flip-flops with totempole TRI-STATE outputs, capable of driving highly capacitive or low-impedance loads. The high-impedance state and increased high-logic-level drive provide these flip-flops with the capability of driving the bus lines in a bus-organized system without need for interface or pull-up components.
Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flipflops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

\section*{Features}
- TRI-STATE outputs interface directly with system bus
- Gated output control lines for enabling or disabling the outputs
mully independent clock elminates restrictions for operating in one of two modes: Parallel load Do nothing (hold)
민 For application as bus buffer registers
(1) Typical propagation delay 18 ns
- Typical frequency 30 MHz
- Typical power dissipation 250 mW
© Alternate Military/Aerospace device (54173) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

Function Table
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multicolumn{5}{|c|}{Inputs} & \multirow{3}{*}{Output Q} \\
\hline \multirow[b]{2}{*}{Clear} & \multirow[b]{2}{*}{Clock} & \multicolumn{2}{|l|}{Data Enable} & \multirow[t]{2}{*}{Data D} & \\
\hline & & G1 & G2 & & \\
\hline H & X & X & X & X & L \\
\hline L & L & X & X & X & \(Q_{0}\) \\
\hline L & \(\uparrow\) & H & X & X & \(Q_{0}\) \\
\hline L & \(\uparrow\) & X & H & X & \(Q_{0}\) \\
\hline L & \(\uparrow\) & L & L & L & L \\
\hline L & \(\uparrow\) & L & L & H & H \\
\hline
\end{tabular}

When either \(M\) or \(N\) (or both) is (are) high the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.
\(\mathrm{H}=\) high level (steady state)
\(\mathrm{L}=\) low level (steady state)
\(\uparrow=\) low-to-high level transition
\(X=\) don't care (any input including transitions)
\(Q_{0}=\) the level of \(Q\) before the indicated steady state input conditions were established

\section*{Connection Diagram}


TL/F/6556-1
Order Number 54173DMQB, 54173FMQB, DM54173J, DM54173W or DM74173N
See NS Package Number J16A, N16E or W16A
```

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
Operating Free Air Temperature Range

| DM54 and 54 | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| :--- | ---: |
| DM74 | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| rage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

```

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54173} & \multicolumn{3}{|c|}{DM74173} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
\hline \({ }_{\mathrm{OH}}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -2 & & & -5.2 & mA \\
\hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & & & 16 & mA \\
\hline \(\mathrm{f}_{\text {cLK }}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 4)} & 0 & & 25 & 0 & & 25 & MHz \\
\hline \multirow[t]{2}{*}{tw} & \multirow[t]{2}{*}{Pulse Width (Note 4)} & Clock & 20 & & & 20 & & & \multirow[t]{2}{*}{ns} \\
\hline & & Clear & 20 & & & 20 & & & \\
\hline \multirow[t]{2}{*}{tsu} & \multirow[t]{2}{*}{Setup Time (Note 4)} & Enable & 17 & & & 17 & & & \multirow[t]{2}{*}{ns} \\
\hline & & Data & 10 & & & 10 & & & \\
\hline \multirow[t]{2}{*}{\(\mathrm{t}_{\mathrm{H}}\)} & \multirow[t]{2}{*}{Hold Time (Note 4)} & Enable & 2 & & & 2 & & & \multirow[t]{2}{*}{ns} \\
\hline & & Data & 10 & & & 10 & & & \\
\hline \(t_{\text {REL }}\) & \multicolumn{2}{|l|}{Clear Release Time (Note 4)} & 10 & & & 10 & & & ns \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
\begin{aligned}
& \text { Typ } \\
& \text { (Note 1) }
\end{aligned}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}_{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{I}_{\mathrm{L}}\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline lozh & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Max}, V_{O}=2.4 \mathrm{~V} \\
& V_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IozL & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & -40 & \(\mu \mathrm{A}\) \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& (\text { Note 2) }
\end{aligned}
\]} & DM54 & \(-30\) & & -70 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -30 & & -70 & \\
\hline \(\mathrm{I}_{\mathrm{CC}}\) & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\operatorname{Max}\) (Note 3)} & & 50 & 72 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: \(\mathrm{I}_{\mathrm{CC}}\) is measured with all outputs open, CLEAR grounded after a momentary connection to 4.5 V : \(\mathrm{N}, \mathrm{G} 1, \mathrm{G} 2\) and all DATA inputs grounded: and the CLOCK input and \(M\) input at 4.5 V .
Note 4: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega\)} & \multirow{3}{*}{Units} \\
\hline & & & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
\hline & & & Min & Max & Min & Max & \\
\hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & & & 25 & & MHz \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Output & & & & 25 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Output & & & & 28 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Clear to Output & & & & 27 & ns \\
\hline \(t_{\text {PZH }}\) & Output Enable Time to High Level Output & Output Control to Q & & & 7 & 30 & ns \\
\hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level Output & Output Control to Q & & & 7 & 30 & ns \\
\hline \(t_{\text {PHZ }}\) & Output Disable Time from High Level Output & Output Control to Q & 3 & 14 & & & ns \\
\hline \(t_{\text {PLZ }}\) & Output Disable Time from Low Level Output & Output Control to Q & 3 & 20 & & & ns \\
\hline
\end{tabular}


TL/F/6556-2

\section*{54174／DM54174／DM74174，54175／DM54175／DM74175 Hex／Quad D Flip－Flops with Clear}

\section*{General Description}

These positive－edge triggered flip－flops utilize TTL circuitry to implement D－type flip－flop logic．All have a direct clear input，and the quad（175）version features complementary outputs from each flip－flop．
Information at the D inputs meeting the setup and hold time requirements is transferred to the \(Q\) outputs on the positive－ going edge of the clock pulse．Clock triggering occurs at a particular voltage level and is not directly related to the tran－ sition time of the positive－going pulse．When the clock input is at either the high or low level，the D input signal has no effect at the output．

\section*{Features}
－ 174 contains six flip－flops with single－rail outputs
－ 175 contains four flip－flops with double－rail outputs
－Buffered clock and direct clear inputs
－Individual data input to each flip－flop
－Applications include：
Buffer／storage registers
Shift registers
Pattern generators
－Typical clock frequency 40 MHz
－Typical power dissipation per flip－flop 38 mW
■ Alternate Military／Aerospace device \((54174,54175)\) is available．Contact a National Semiconductor Sales Of－ fice／Distributor for specifications．

\section*{Connection Diagrams}

Dual－In－Line Package


Order Number 54174DMQB，54174FMQB，DM54174J， DM54174W or DM74174N
See NS Package Number J16A，N16E or W16A

\section*{Dual－In－Line Package}


Order Number 54175DMQB，54175FMQB，DM54175J， DM54175W or DM74175N See NS Package Number J16A，N16E or W16A

Function Table（Each Flip－Flop）
\begin{tabular}{|c|c|c|c|c|}
\hline \multicolumn{3}{|c|}{ Inputs } & \multicolumn{2}{c|}{ Outputs } \\
\hline Clear & Clock & D & Q & \(\overline{\mathbf{Q}} \dagger\) \\
\hline L & X & X & L & \(H\) \\
\(H\) & \(\uparrow\) & \(H\) & \(H\) & L \\
\(H\) & \(\uparrow\) & L & L & \(H\) \\
\(H\) & L & \(X\) & \(Q_{0}\) & \(\bar{Q}_{0}\) \\
\hline
\end{tabular}

\footnotetext{
\(H=\) High Level（steady state）
\(L=\) Low Level（steady state）
X＝Don＇t Care
\(\uparrow=\) Transition from low to high level
\(Q_{0}=\) The level of \(Q\) before the indicated steady－state input conditions were established．
\(\dagger=175\) only
}

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avallability and specifications.
\begin{tabular}{lr} 
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \\
DM54 and 54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54174} & \multicolumn{3}{|c|}{DM74174} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\text {CC }}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{IOH}^{\text {l }}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.8 & & & -0.8 & mA \\
\hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & & & 16 & mA \\
\hline \(\mathrm{fcLK}^{\text {chen }}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 4)} & 0 & & 30 & 0 & & 30 & MHz \\
\hline \multirow[t]{3}{*}{tw} & \multirow[t]{3}{*}{Pulse Width (Note 4)} & Clock Low & 25 & & & 25 & & & \multirow{3}{*}{ns} \\
\hline & & Clock High & 10 & & & 10 & & & \\
\hline & & Clear & 20 & & & 20 & & & \\
\hline tsu & \multicolumn{2}{|l|}{Data Setup Time (Note 4)} & 20 & & & 20 & & & ns \\
\hline \(t_{H}\) & \multicolumn{2}{|l|}{Data Hold Time (Note 4)} & 0 & & & 0 & & & ns \\
\hline \(t_{\text {REL }}\) & \multicolumn{2}{|l|}{Clear Release Time (Note 4)} & 30 & & & 30 & & & ns \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{'174 Electrical Characteristics}
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOH}_{\mathrm{OH}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, V_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, V_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=\operatorname{Max} \\
& \text { (Note 2) }
\end{aligned}
\]} & DM54 & -20 & & -57 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -57 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\operatorname{Max}\) (Note 3)} & & 45 & 65 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: With all outputs open and all DATA and CLEAR inputs at 4.5 V , ICC is measured after a momentary ground, then 4.5 V applied to the CLOCK input.
Note 4: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{C}}=5 \mathrm{~V}\).
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multicolumn{6}{|l|}{\begin{tabular}{l}
'174 Switching Characteristics \\
at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\end{tabular}} \\
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{\begin{tabular}{l}
From (Input) \\
To (Output)
\end{tabular}} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 30 & & MHz \\
\hline \({ }_{\text {tpLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Any Q & & 25 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
Clock to \\
Any Q
\end{tabular} & & 25 & ns \\
\hline \({ }_{\text {trHL }}\) & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
Clear to \\
Any Q
\end{tabular} & & 40 & ns \\
\hline
\end{tabular}

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54175} & \multicolumn{3}{|c|}{DM74175} & \multirow{2}{*}{Units} \\
\hline & & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\mathrm{IL}}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{lOH}^{\text {l }}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.8 & & & -0.8 & mA \\
\hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & & & 16 & mA \\
\hline \({ }_{\text {f CLK }}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 1)} & 0 & & 30 & 0 & & 30 & MHz \\
\hline \multirow[t]{3}{*}{tw} & \multirow[t]{3}{*}{Pulse Width (Note 1)} & Clock Low & 25 & & & 25 & & & \multirow{3}{*}{ns} \\
\hline & & Clock High & 10 & & & 10 & & & \\
\hline & & Clear & 20 & & & 20 & & & \\
\hline tsu & \multicolumn{2}{|l|}{Data Setup Time (Note 1)} & 20 & & & 20 & & & ns \\
\hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Data Hold Time (Note 1)} & 0 & & & 0 & & & ns \\
\hline \(t_{\text {REL }}\) & \multicolumn{2}{|l|}{Clear Release Time (Note 1)} & 30 & & & 30 & & & ns \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Note 1: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
'175 Electrical Characteristics
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & 2.4 & & & V \\
\hline VOL & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline I/L & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=M a x
\] \\
(Note 2)
\end{tabular}} & DM54 & -20 & & -57 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -57 & \\
\hline \(\mathrm{I}_{\mathrm{CC}}\) & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\) (Note 3)} & & 30 & 45 & mA \\
\hline
\end{tabular}
'175 Switching Characteristics
at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{\begin{tabular}{l}
From (Input) \\
To (Output)
\end{tabular}} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 30 & & MHz \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Any Q or \(\bar{Q}\) & & 25 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Any Q or \(\bar{Q}\) & & 25 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \begin{tabular}{l}
Clear to \\
Any \(\bar{Q}\)
\end{tabular} & & 25 & ns \\
\hline tPHL & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
Clear to \\
Any Q
\end{tabular} & & 40 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: With all outputs open and 4.5 V applied to all DATA and CLEAR inputs, ICc is measured after a momentary ground then 4.5 V applied to the CLOCK.

\section*{Logic Diagrams}


\section*{DM54180/DM74180 9-Bit Parity Generators/Checkers}

\section*{General Description}

These universal 9-bit (8 data bits plus 1 parity bit) parity generators/checkers feature odd/even outputs and control inputs to facilitate operation in either odd or even parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd input can be utilized as the parity or 9th-bit input. The word-length capability is easily expanded by cascading.

Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs at a low logic level. A fan-out to 20 normalized loads is provided at a high logic level to facilitate the connection of unused inputs to used inputs.

\section*{Connection Diagram}


TL/F/6559-1
Order Number DM54180J, DM54180W or DM74180N
See NS Package Number J14A, N14A or W14B

\section*{Function Table}
\begin{tabular}{|c|c|c|c|c|}
\hline \multicolumn{3}{|c|}{ Inputs } & \multicolumn{2}{c|}{ Outputs } \\
\hline \begin{tabular}{c}
\(\Sigma\) of H's at \\
A thru H
\end{tabular} & Even & Odd & \begin{tabular}{c}
\(\Sigma\) \\
Even
\end{tabular} & \begin{tabular}{c}
\(\Sigma\) \\
Odd
\end{tabular} \\
\hline Even & H & L & H & L \\
\hline Odd & H & L & L & H \\
\hline Even & L & H & L & H \\
\hline Odd & L & H & H & L \\
\hline X & H & H & L & L \\
\hline X & L & L & H & H \\
\hline
\end{tabular}

H = High Level, L = Low Level, X = Don't Care


Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \begin{tabular}{l}
Typ \\
(Note 1)
\end{tabular} & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M i n, l_{l}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, I_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{2}{*}{\(I_{1 H}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=2.4 V
\end{aligned}
\]} & Odd or Even & & & 80 & \multirow{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Data & & & 40 & \\
\hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{I}=0.4 V
\end{aligned}
\]} & Odd or Even & & & -3.2 & \multirow[t]{2}{*}{mA} \\
\hline & & & Data & & & -1.6 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& (\text { Note 2) }
\end{aligned}
\]} & DM54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -55 & \\
\hline \multirow[t]{2}{*}{ICC} & \multirow[t]{2}{*}{Supply Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=\operatorname{Max}
\] \\
(Note 3)
\end{tabular}} & DM54 & & 34 & 49 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & & 34 & 56 & \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: ICC is measured with EVEN and ODD inputs at 4.5V, all other inputs and outputs open.

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & From (Input) To (Output) & Conditions & Min & Max & Units \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Data to \(\Sigma\) Even & \multirow[t]{4}{*}{\[
\begin{aligned}
& \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\
& \mathrm{R}_{\mathrm{L}}=400 \Omega \\
& \text { Odd Input Low }
\end{aligned}
\]} & & 60 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to \(\Sigma\) Even & & & 68 & ns \\
\hline \({ }_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output & Data to \(\Sigma\) Odd & & & 48 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to \(\Sigma\) Odd & & & 38 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Data to \(\Sigma\) Even & \multirow[t]{4}{*}{\begin{tabular}{l}
\[
\begin{aligned}
& \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\
& \mathrm{R}_{\mathrm{L}}=400 \Omega
\end{aligned}
\] \\
Odd Input High
\end{tabular}} & & 48 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to \(\Sigma\) Even & & & 38 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Data to \(\Sigma\) Odd & & & 60 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to \(\Sigma\) Odd & & & 68 & ns \\
\hline tplH & Propagation Delay Time Low to High Level Output & \begin{tabular}{l}
Even or Odd to \\
\(\Sigma\) Even or \(\Sigma\) Odd
\end{tabular} & \multirow[t]{2}{*}{\[
\begin{aligned}
& C_{\mathrm{L}}=15 \mathrm{pF} \\
& \mathrm{R}_{\mathrm{L}}=400 \Omega
\end{aligned}
\]} & & 20 & ns \\
\hline \({ }^{\text {PPHL }}\) & Propagation Delay Time High to Low Level Output & Even or Odd to \(\Sigma\) Even or \(\Sigma\) Odd & & & 10 & ns \\
\hline
\end{tabular}

Logic Diagram


\section*{DM54181}

Arithmetic Logic Unit/Function Generators

\section*{General Description}

These arithmetic logic units (ALU)/function generators perform 16 binary arithmetic operations on two 4-bit words, as shown in Tables I and II. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is available in these devices for fast, simultaneous carry generation by means of two cascade-outputs ( \(P\) and \(G\) ) for the four bits in the package. When used in conjunction with the DM54S182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown below illustrate how little time is required for addition of longer words, when full carry look-ahead is employed. The method of cascading 182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the DM54S182.
(Continued)

\section*{Features}
a Arithmetic operating modes: Addition Subtraction Shift operand A one position Magnitude comparison Plus twelve other arithmetic operations
- Logic function modes:

EXCLUSIVE-OR
Comparator AND, NAND, OR, NOR Plus ten other logic operations
m Full look-ahead for high-speed operations on long words

\section*{Connection Diagram}

Dual-In-Line Package


TL/F/6560-1
Order Number DM54181J See NS Package Number J24A

Pin Designations
\begin{tabular}{|c|c|c|}
\hline Designation & Pin Nos. & Function \\
\hline A3, A2, A1, A0 & \(19,21,23,2\) & Word A Inputs \\
\hline B3, B2, B1, B0 & \(18,20,22,1\) & Word B Inputs \\
\hline S3, S2, S1, S0 & \(3,4,5,6\) & \begin{tabular}{c} 
Function-Select \\
Inputs
\end{tabular} \\
\hline C \(_{n}\) & 7 & Inv. Carry Input \\
\hline M & 8 & \begin{tabular}{c} 
Mode Control \\
Input
\end{tabular} \\
\hline F3, F2, F1, F0 & \(13,11,10,9\) & Function Outputs \\
\hline A = B & 14 & Comparator Output \\
\hline P & 15 & \begin{tabular}{c} 
Carry Propagate \\
Output
\end{tabular} \\
\hline C \(_{n}+4\) & 16 & Inv. Carry Output \\
\hline G & 17 & \begin{tabular}{c} 
Carry Generate \\
Output
\end{tabular} \\
\hline V \(C C^{\text {GND }}\) & 24 & Supply Voltage \\
\hline & 12 & Ground \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Number of Bits} & \multirow[t]{2}{*}{Typical Addition Times} & \multicolumn{2}{|r|}{Package Count} & \multirow[t]{2}{*}{Carry Method Between ALU's} \\
\hline & & Arithmetic/ Logic Units & Look Ahead Carry Generators & \\
\hline 1 to 4 & 20 ns & 1 & 0 & None \\
\hline 5 to 8 & 30 ns & 2 & 0 & Ripple \\
\hline 9 to 16 & 30 ns & 3 or 4 & 1 & Full Look-Ahead \\
\hline 17 to 64 & 50 ns & 5 to 16 & 2 to 5 & Full Look-Ahead \\
\hline
\end{tabular}

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage 5.5 V

Output Voltage ( \(\mathrm{A}=\mathrm{B}\) Output) 5.5 V

Operating Free Air Temperature Range DM54
\(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
Storage Temperature Range
\(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{c|l|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multicolumn{2}{|c|}{ Parameter } & \multicolumn{2}{|c|}{ DM54181 } & \multirow{2}{*}{ Units } \\
\cline { 3 - 5 } & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline \(\mathrm{~V}_{\mathrm{OH}}\) & \begin{tabular}{l} 
High Level Output \\
Voltage (A = B Output)
\end{tabular} & & & 5.5 & V \\
\hline \(\mathrm{IOH}_{\mathrm{OH}}\) & \begin{tabular}{l} 
High Level Output \\
Current (All Except \(\mathrm{A}=\mathrm{B})\)
\end{tabular} & & & -800 & \(\mu \mathrm{~A}\) \\
\hline IOL & Low Level Output Current & & & 16 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & \begin{tabular}{l} 
Free Air Operating \\
Temperature
\end{tabular} & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \begin{tabular}{l}
Typ \\
(Note 1)
\end{tabular} & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(I_{\text {CEX }}\) & High Level Output Current ( \(\mathrm{A}=\mathrm{B}\) Output) & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{V}_{\mathrm{O}}=5.5 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & & & 250 & \(\mu \mathrm{A}\) \\
\hline V OH & High Level Output Voltage (All Except A = B) & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOH}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{4}{*}{\(\mathrm{IIH}^{\text {H }}\)} & \multirow[t]{4}{*}{High Level Input Current} & \multirow[t]{4}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=2.4 V
\end{aligned}
\]} & Mode & & & 40 & \multirow{4}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & A or B & & & 120 & \\
\hline & & & S & & & 160 & \\
\hline & & & Carry & & & 200 & \\
\hline \multirow[t]{4}{*}{IIL} & \multirow[t]{4}{*}{Low Level Input Current} & \multirow[t]{4}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=0.4 V
\end{aligned}
\]} & Mode & & & -1.6 & \multirow{4}{*}{mA} \\
\hline & & & A or B & & & -4.8 & \\
\hline & & & S & & & -6.4 & \\
\hline & & & Carry & & & -8 & \\
\hline los & \begin{tabular}{l}
Short Circuit Output \\
Current (All Except A = B)
\end{tabular} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=2.4 V
\end{aligned}
\]} & -20 & & -55 & mA \\
\hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=M a x \\
& \text { (Note 3) } \\
& \hline
\end{aligned}
\]} & & 88 & 127 & mA \\
\hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=M a x \\
& (\text { Note 4) } \\
& \hline
\end{aligned}
\]} & & 92 & 135 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: \(\mathrm{I}_{\mathrm{CCH}}\) is measured with SO through \(\mathrm{S} 3, \mathrm{M}\), and A inputs at 4.5 V , all other inputs grounded and all outputs open.
Note 4: \(I_{C C L}\) is measured with \(S 0\) through \(S 3\) and \(M\) inputs at 4.5 V , all other inputs grounded and all outputs open.
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[b]{3}{*}{From (Input)} & \multirow[b]{3}{*}{To (Output)} & \multirow{3}{*}{Conditions} & \multicolumn{2}{|c|}{DM54181} & \multirow{3}{*}{Units} \\
\hline & & & & & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \\
\hline & & & & & Min & Max & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{\(C_{n}\)} & \multirow[t]{2}{*}{\(\mathrm{C}_{\mathrm{n}}+4\)} & & & 18 & \multirow[t]{2}{*}{ns} \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 19 & \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{Any A or B} & \multirow[t]{2}{*}{\(C_{n}+4\)} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{M}=0 \mathrm{~V}, \mathrm{SO}= \\
& \mathrm{S} 3=4.5 \mathrm{~V} \\
& \mathrm{~S} 1=\mathrm{S} 2=0 \mathrm{~V} \\
& (\overline{\mathrm{SUM}} \text { mode })
\end{aligned}
\]} & & 30 & \multirow[t]{2}{*}{ns} \\
\hline \({ }^{\text {PrHL }}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 33 & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{Any A or B} & \multirow[t]{2}{*}{\(C_{n}+4\)} & \multirow[t]{2}{*}{\[
\begin{aligned}
& M=O V, S 0= \\
& S 3=O V \\
& S 1=S 2=4.5 \mathrm{~V} \\
& \text { (DIFF mode) }
\end{aligned}
\]} & & 30 & \multirow[t]{2}{*}{ns} \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 33 & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{\(\mathrm{C}_{\mathrm{n}}\)} & \multirow[t]{2}{*}{Any F} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
\mathrm{M}=0 \mathrm{~V}
\] \\
(SUM or DIFF mode)
\end{tabular}} & & 19 & \multirow[t]{2}{*}{ns} \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 18 & \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{Any A or B} & \multirow[t]{2}{*}{G} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{M}=0 \mathrm{~V}, \mathrm{SO}= \\
& \mathrm{S} 3=4.5 \mathrm{~V} \\
& \mathrm{~S} 1=\mathrm{S} 2=0 \mathrm{~V} \\
& (\mathrm{SUM} \text { mode })
\end{aligned}
\]} & & 19 & \multirow[t]{2}{*}{ns} \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 19 & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{Any A or B} & \multirow[t]{2}{*}{G} & \multirow[t]{2}{*}{\[
\begin{aligned}
& M=O V, S 0= \\
& S 3=O V \\
& S 1=S 2=4.5 \mathrm{~V} \\
& \text { (DIFF mode) }
\end{aligned}
\]} & & 20 & \multirow[t]{2}{*}{ns} \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 25 & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{Any A or B} & \multirow[t]{2}{*}{P} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
\begin{aligned}
& M=0 \mathrm{~V}, \mathrm{SO}= \\
& \mathrm{S} 3=4.5 \mathrm{~V} \\
& \mathrm{~S} 1=\mathrm{S} 2=0 \mathrm{~V}
\end{aligned}
\] \\
(SUM mode)
\end{tabular}} & & 19 & \multirow[t]{2}{*}{ns} \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 25 & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{Any A or B} & \multirow[t]{2}{*}{P} & \multirow[t]{2}{*}{\[
\begin{aligned}
& M=O V, S 0= \\
& S 3=O V \\
& S 1=S 2=4.5 \mathrm{~V} \\
& \text { (DIFF mode) }
\end{aligned}
\]} & & 25 & \multirow[t]{2}{*}{ns} \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 25 & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{\(\mathrm{A}_{i}\) or \(\mathrm{B}_{i}\)} & \multirow[t]{2}{*}{\(\mathrm{F}_{\mathrm{i}}\)} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{M}=0 \mathrm{~V}, \mathrm{~S} 0= \\
& \mathrm{S} 3=4.5 \mathrm{~V} \\
& \mathrm{~S} 1=\mathrm{S} 2=0 \mathrm{~V} \\
& (\mathrm{SUM} \text { mode })
\end{aligned}
\]} & & 30 & \multirow[t]{2}{*}{ns} \\
\hline \({ }^{\text {PrHL }}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 30 & \\
\hline \({ }_{\text {tplH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{\(\mathrm{A}_{\mathrm{i}}\) or \(\mathrm{B}_{i}\)} & \multirow[t]{2}{*}{\(\mathrm{F}_{\mathrm{i}}\)} & \multirow[t]{2}{*}{\[
\begin{aligned}
& M=0 \mathrm{~V}, \mathrm{~S} 0= \\
& \mathrm{S} 3=0 \mathrm{~V} \\
& \mathrm{~S} 1=\mathrm{S} 2=4.5 \mathrm{~V} \\
& \text { (DIFF mode) }
\end{aligned}
\]} & & 24 & \multirow[t]{2}{*}{ns} \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 24 & \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{\(\mathrm{A}_{\mathrm{i}}\) or \(\mathrm{B}_{\mathrm{i}}\)} & \multirow[t]{2}{*}{\(\mathrm{F}_{\mathrm{i}}\)} & \multirow[t]{2}{*}{\[
\begin{aligned}
& M=4.5 \mathrm{~V} \\
& (\text { logic mode })
\end{aligned}
\]} & & 28 & \multirow[t]{2}{*}{ns} \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 30 & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{Any A or B} & \multirow[t]{2}{*}{\(A=B\)} & \multirow[t]{2}{*}{\[
\begin{aligned}
& M=O V, S 0= \\
& S 3=O V \\
& S 1=S 2=4.5 \mathrm{~V} \\
& \text { (DIFF mode) }
\end{aligned}
\]} & & 40 & \multirow[t]{2}{*}{ns} \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 40 & \\
\hline
\end{tabular}

\section*{General Description (Continued)}

If high speed is not important, a ripple-carry input \(\left(\mathrm{C}_{n}\right)\) and a ripple-carry output ( \(\mathrm{C}_{n}+4\) ) are available. However, the rip-ple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.
These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below. Subtraction is accomplished by 1 's complement addition, where the 1's complement of the subtrahend is generated internally. The resultant output is \(\mathrm{A}-\mathrm{B}-1\), which requires an end-around or forced carry to provide A-B.
The 181 can also be utilized as a comparator. The \(A=B\) output is internally decoded from the function outputs (FO, F1, F2, F3) so that when two words of equal magnitude are applied at the \(A\) and \(B\) inputs, it will assume a high level to indicate equality \((A=B)\). The ALU should be in the subtract mode with \(\mathrm{C}_{\mathrm{n}}=\mathrm{H}\) when performing this comparison. The A \(=B\) output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output ( \(C_{n}+4\) ) can also be used to supply
relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.
These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusiveOR, NAND, AND, NOR, and OR functions.

\section*{ALU SIGNAL DESIGNATIONS}

The DM54181 can be used with the signal designations of either Figure 1 or Figure 2.
The logic functions and arithmetic operations obtained with signal designations as in Figure 1 are given in Table I; those obtained with the signal designations of Figure 2 are given in Table II.
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline Pin Number & \(\mathbf{2}\) & \(\mathbf{1}\) & \(\mathbf{2 3}\) & \(\mathbf{2 2}\) & \(\mathbf{2 1}\) & \(\mathbf{2 0}\) & \(\mathbf{1 9}\) & \(\mathbf{1 8}\) & \(\mathbf{9}\) & \(\mathbf{1 0}\) & \(\mathbf{1 1}\) & \(\mathbf{1 3}\) & \(\mathbf{7}\) & \(\mathbf{1 6}\) & \(\mathbf{1 5}\) & \(\mathbf{1 7}\) \\
\hline Active-High Data (Table I) & A 0 & B 0 & A 1 & B 1 & A 2 & B 2 & A 3 & B 3 & F 0 & F 1 & F 2 & F 3 & \(\overline{\mathrm{C}}_{\mathrm{n}}\) & \(\overline{\mathrm{C}}_{n}+4\) & X & Y \\
\hline Active-Low Data (Table II) & \(\overline{\mathrm{A} 0} 0\) & \(\overline{\mathrm{~B}} 0\) & \(\overline{\mathrm{~A}} 1\) & \(\overline{\mathrm{~B}} 1\) & \(\overline{\mathrm{~A}} 2\) & \(\overline{\mathrm{~B}} 2\) & \(\overline{\mathrm{~A}} 3\) & \(\overline{\mathrm{~B}} 3\) & \(\overline{\mathrm{~F}} 0\) & \(\overline{\mathrm{~F}} 1\) & \(\overline{\mathrm{~F}} 2\) & \(\overline{\mathrm{~F}} 3\) & \(\mathrm{C}_{\mathrm{n}}\) & \(\mathrm{C}_{n}+4\) & \(\overline{\mathrm{P}}\) & \(\overline{\mathrm{G}}\) \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|c|}
\hline \begin{tabular}{c} 
Input \\
\(\mathbf{C}_{\boldsymbol{n}}\)
\end{tabular} & \begin{tabular}{c} 
Output \\
\(\mathrm{C}_{\boldsymbol{n}}+\mathbf{4}\)
\end{tabular} & \begin{tabular}{c} 
Active-High Data \\
(Figure 1)
\end{tabular} & \begin{tabular}{c} 
Active-Low Data \\
(Figure 2)
\end{tabular} \\
\hline\(H\) & \(H\) & \(A \leq B\) & \(A \geq B\) \\
\(H\) & \(L\) & \(A>B\) & \(A<B\) \\
\(L\) & \(H\) & \(A<B\) & \(A>B\) \\
\(L\) & \(L\) & \(A \geq B\) & \(A \leq B\) \\
\hline
\end{tabular}


FIGURE 1


FIGURE 2

TABLE I
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multicolumn{4}{|c|}{\multirow[t]{2}{*}{Selection}} & \multicolumn{3}{|c|}{Active High Data} \\
\hline & & & & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
\mathbf{M}=\mathbf{H}
\] \\
Logic Functions
\end{tabular}} & \multicolumn{2}{|r|}{\(\mathrm{M}=\mathrm{L}\); Arithmetic Operations} \\
\hline S3 & S2 & S1 & S0 & & \(\mathrm{C}_{\mathrm{n}}=\mathrm{H}\) ( no carry) & \(\mathrm{C}_{\mathrm{n}}=\mathrm{L}\) (with carry) \\
\hline L & L & L & L & \(F=\bar{A}\) & \(F=A\) & \(F=A\) Plus 1 \\
\hline L & L & L & H & \(F=\overline{A+B}\) & \(F=A+B\) & \(F=(A+B)\) Plus 1 \\
\hline L & L & H & L & \(F=\bar{A} B\) & \(F=A+\bar{B}\) & \(F=(A+\bar{B})\) Plus 1 \\
\hline L & L & H & H & \(\mathrm{F}=0\) & \(\mathrm{F}=\) Minus 1 (2's Compl) & \(F=\) Zero \\
\hline L & H & L & L & \(F=\overline{A B}\) & \(F=A\) Plus \(A \bar{B}\) & \(F=A\) Plus \(A \bar{B}\) Plus 1 \\
\hline L & H & L & H & \(\mathrm{F}=\overline{\mathrm{B}}\) & \(F=(A+B)\) Plus \(A \bar{B}\) & \(F=(A+B)\) Plus \(A \bar{B}\) Plus 1 \\
\hline L & H & H & L & \(F=A \oplus B\) & \(F=A\) Minus \(B\) Minus 1 & \(F=A\) Minus \(B\) \\
\hline L & H & H & H & \(F=A \bar{B}\) & \(F=A \bar{B}\) Minus 1 & \(F=A \bar{B}\) \\
\hline H & L & L & L & \(F=\bar{A}+B\) & \(F=A\) Plus \(A B\) & \(F=A\) Plus AB Plus 1 \\
\hline H & L & L & H & \(F=\overline{A \oplus B}\) & \(F=A\) Plus \(B\) & \(F=A\) Plus \(B\) Plus 1 \\
\hline H & L & H & L & \(F=B\) & \(F=(A+\bar{B})\) Plus \(A B\) & \(F=(A+\bar{B})\) Plus \(A B\) Plus 1 \\
\hline H & L & H & H & \(F=A B\) & \(F=A B\) Minus 1 & \(F=A B\) \\
\hline H & H & L & L & \(F=1\) & \(F=A\) Plus \(A^{*}\) & \(F=A\) Plus A Plus 1 \\
\hline H & H & L & H & \(F=A+\bar{B}\) & \(F=(A+B)\) Plus \(A\) & \(F=(A+B)\) Plus A Plus 1 \\
\hline H & H & H & L & \(F=A+B\) & \(F=(A+\bar{B})\) Plus \(A\) & \(F=(A+\bar{B})\) Plus \(A\) Plus 1 \\
\hline H & H & H & H & \(F=A\) & \(F=A\) Minus 1 & \(F=A\) \\
\hline
\end{tabular}
*Each bit is shifted to the next more significant position.

TABLE II
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multicolumn{4}{|c|}{\multirow[t]{2}{*}{Selection}} & \multicolumn{3}{|c|}{Active Low Data} \\
\hline & & & & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
M=H
\] \\
Logic Functions
\end{tabular}} & \multicolumn{2}{|r|}{M = L; Arithmetic Operations} \\
\hline S3 & S2 & S1 & So & & \(\mathrm{C}_{\mathrm{n}}=\mathrm{L}\) ( no carry) & \(\mathrm{C}_{\mathrm{n}}=\mathrm{H}\) (with carry) \\
\hline L & L & L & L & \(\mathrm{F}=\overline{\mathrm{A}}\) & \(F=A\) Minus 1 & \(F=A\) \\
\hline L & L & L & H & \(F=\overline{A B}\) & \(F=A B\) Minus 1 & \(F=A B\) \\
\hline L & L & H & L & \(F=\bar{A}+B\) & \(F=A \bar{B}\) Minus 1 & \(F=A \bar{B}\) \\
\hline L & L & H & H & \(F=1\) & \(\mathrm{F}=\) Minus 1 (2's Compl) & \(F=\) Zero \\
\hline L & H & L & L & \(F=\overline{A+B}\) & \(\mathrm{F}=\mathrm{A}\) Plus \((\mathrm{A}+\overline{\mathrm{B}}\) ) & \(F=A\) Plus \((A+\bar{B})\) Plus 1 \\
\hline L & H & L & H & \(\mathrm{F}=\overline{\mathrm{B}}\) & \(F=A B\) Plus \((A+B)\) & \(F=A B\) Plus \((A+\bar{B})\) Plus 1 \\
\hline L & H & H & L & \(F=\overline{A \oplus B}\) & \(F=A\) Minus \(B\) Minus 1 & \(F=A\) Minus \(B\) \\
\hline L & H & H & H & \(F=A+\bar{B}\) & \(F=A+\bar{B}\) & \(F=(A+\bar{B})\) Plus 1 \\
\hline H & L & L & L & \(F=\bar{A} B\) & \(F=A\) Plus \((A+B)\) & \(F=A\) Plus \((A+B)\) Plus 1 \\
\hline H & L & L & H & \(F=A \oplus B\) & \(F=A\) Plus B & \(F=A\) Plus \(B\) Plus 1 \\
\hline H & L & H & L & \(F=B\) & \(F=A \bar{B}\) Plus \((A+B)\) & \(F=A \bar{B}\) Plus \((A+B)\) Plus 1 \\
\hline H & L & H & H & \(F=A+B\) & \(F=A+B\) & \(F=(A+B)\) Plus 1 \\
\hline H & H & L & L & \(\mathrm{F}=0\) & \(F=\) A Plus \({ }^{*}\) & \(\mathrm{F}=\mathrm{A}\) Plus A Plus 1 \\
\hline H & H & L & H & \(F=A \bar{B}\) & \(F=A B\) Plus \(A\) & \(F=A B\) Plus A Plus 1 \\
\hline H & H & H & L & \(F=A B\) & \(F=A \bar{B}\) Plus \(A\) & \(F=A \bar{B}\) Plus A Plus 1 \\
\hline H & H & H & H & \(F=A\) & \(F=A\) & \(\mathrm{F}=\mathrm{A}\) Plus 1 \\
\hline
\end{tabular}
"Each bit is shifted to the next more significant position.

\section*{Parameter Measurement Information}

Logic Mode Test Table
Function Inputs: \(\mathbf{S 1}=\mathbf{S 2}=\mathbf{M}=\mathbf{4 . 5 V}, \mathbf{S 0}=\mathbf{S 3}=\mathbf{O V}\)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{\begin{tabular}{l}
Input \\
Under \\
Test
\end{tabular}} & \multicolumn{2}{|c|}{Other Input Same Bit} & \multicolumn{2}{|r|}{Other Data Inputs} & \multirow[t]{2}{*}{\begin{tabular}{l}
Output \\
Under \\
Test
\end{tabular}} & \multirow[t]{2}{*}{Output Waveform} \\
\hline & & Apply 4.5V & Apply GND & Apply 4.5V & Apply GND & & \\
\hline \(t_{\text {tPLH }}{ }_{\text {tPHL }}\) & \(\mathrm{A}_{\mathrm{i}}\) & \(B_{i}\) & None & None & Remaining \(A\) and \(B, C_{n}\) & \(\mathrm{F}_{\mathrm{i}}\) & Out-of-Phase \\
\hline \({ }_{\text {tPLH }}^{\text {tPHL }}\) & \(\mathrm{B}_{i}\) & \(\mathrm{A}_{\mathrm{i}}\) & None & None & \begin{tabular}{l}
Remaining \\
\(A\) and \(B, C_{n}\)
\end{tabular} & \(\mathrm{F}_{\mathrm{i}}\) & Out-ot-Phase \\
\hline
\end{tabular}

SUM Mode Test Table
Function Inputs: \(\mathbf{S O}=\mathbf{S 3}=\mathbf{4 . 5 V}, \mathbf{S 1}=\mathbf{S 2}=\mathbf{M}=\mathbf{O V}\)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Input Under Test} & \multicolumn{2}{|c|}{Other Input Same Bit} & \multicolumn{2}{|r|}{Other Data Inputs} & \multirow[t]{2}{*}{\begin{tabular}{l}
Output \\
Under \\
Test
\end{tabular}} & \multirow[t]{2}{*}{Output Waveform} \\
\hline & & Apply 4.5V & Apply GND & Apply 4.5V & Apply GND & & \\
\hline \[
\frac{t_{\text {PLH }}}{t_{\text {PHL }}}
\] & \(A_{i}\) & \(\mathrm{B}_{\mathrm{i}}\) & None & Remaining \(A\) and \(B\) & \(\mathrm{C}_{\mathrm{n}}\) & \(\mathrm{F}_{\mathrm{i}}\) & In-Phase \\
\hline \[
\frac{t_{\text {PLH }}}{t_{\text {PHL }}}
\] & \(\mathrm{B}_{\mathrm{i}}\) & \(A_{i}\) & None & Remaining \(A\) and \(B\) & \(\mathrm{C}_{\mathrm{n}}\) & \(\mathrm{F}_{\mathrm{i}}\) & In-Phase \\
\hline \[
\frac{t_{\text {PLH }}}{t_{\text {PHL }}}
\] & \(A_{i}\) & \(\mathrm{B}_{\mathrm{i}}\) & None & None & \begin{tabular}{l}
Remaining \\
\(A\) and \(B, C_{n}\)
\end{tabular} & P & In-Phase \\
\hline \(\mathrm{t}_{\text {PLH }}\) & \(\mathrm{B}_{i}\) & \(A_{i}\) & None & None & \begin{tabular}{l}
Remaining \\
\(A\) and \(B, C_{n}\)
\end{tabular} & P & In-Phase \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{8}{|l|}{Parameter Measurement Information (Continued)} \\
\hline \multicolumn{8}{|c|}{\begin{tabular}{l}
डUM Mode Test Table \\
Function Inputs: S0 = S3 \(=\mathbf{4 . 5 V}, \mathbf{S 1}=\mathbf{S 2}=\mathbf{M}=\mathbf{O V}\) (Continued)
\end{tabular}} \\
\hline \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Input Under Test} & \multicolumn{2}{|c|}{Other Input Same Bit} & \multicolumn{2}{|l|}{Other Data Inputs} & \multirow[t]{2}{*}{Output Under Test} & \multirow[t]{2}{*}{Output Waveform} \\
\hline & & Apply 4.5V & Apply GND & Apply
\[
4.5 \mathrm{~V}
\] & Apply GND & & \\
\hline \(\mathrm{tpLH}^{\text {tpHL }}\) & \(A_{i}\) & None & \(\mathrm{B}_{\mathrm{i}}\) & Remaining B & Remaining \(\mathrm{A}, \mathrm{C}_{\mathrm{n}}\) & G & In-Phase \\
\hline \(t_{\text {PLH }}\) & \(\mathrm{B}_{\mathrm{i}}\) & None & \(A_{i}\) & Remaining
B & \[
\begin{aligned}
& \text { Remaining } \\
& \qquad A, C_{n}
\end{aligned}
\] & G & In-Phase \\
\hline \[
\frac{\mathrm{t}_{\mathrm{PLH}}}{\mathrm{t}_{\mathrm{PHL}}}
\] & \(C_{n}\) & None & None & \[
\begin{gathered}
\text { All } \\
\text { A }
\end{gathered}
\] & \[
\begin{gathered}
\text { All } \\
\text { B }
\end{gathered}
\] & \[
\begin{gathered}
\text { Any F } \\
\text { or } \mathrm{C}_{n}+4
\end{gathered}
\] & In-Phase \\
\hline \[
\frac{t_{\mathrm{PLH}}}{\mathrm{t}_{\mathrm{PHL}}}
\] & \(A_{i}\) & None & \(\mathrm{B}_{\mathrm{i}}\) & Remaining B & Remaining A, \(\mathrm{C}_{\mathrm{n}}\) & \(\mathrm{C}_{\mathrm{n}}+4\) & Out-of-Phase \\
\hline \(\mathrm{tpLH}_{\text {tPHL }}\) & \(\mathrm{B}_{\mathrm{i}}\) & None & \(A_{i}\) & Remaining B & Remaining \(A, C_{n}\) & \(\mathrm{C}_{\mathrm{n}}+4\) & Out-of-Phase \\
\hline
\end{tabular}

DIFF Mode Test Table
Function Inputs: S1 \(=\mathbf{S} 2=4.5 \mathrm{~V}, \mathrm{SO}=\mathbf{S 3}=\mathrm{M}=\mathbf{O V}\)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Input Under Test} & \multicolumn{2}{|c|}{Other Input Same Bit} & \multicolumn{2}{|r|}{Other Data Inputs} & \multirow[t]{2}{*}{\begin{tabular}{l}
Output \\
Under \\
Test
\end{tabular}} & \multirow[t]{2}{*}{Output Waveform} \\
\hline & & Apply
\[
4.5 \mathrm{~V}
\] & Apply GND & Apply
\[
4.5 \mathrm{~V}
\] & Apply GND & & \\
\hline \[
\frac{t_{\mathrm{PLH}}}{\mathrm{t}_{\mathrm{PHL}}}
\] & \(\mathrm{A}_{\mathrm{i}}\) & None & \(\mathrm{B}_{\mathrm{i}}\) & Remaining
A & \[
\begin{aligned}
& \text { Remaining } \\
& B, C_{n}
\end{aligned}
\] & \(\mathrm{F}_{\mathrm{i}}\) & In-Phase \\
\hline \[
\frac{t_{\mathrm{PLH}}}{t_{\mathrm{PHL}}}
\] & \(\mathrm{B}_{\mathrm{i}}\) & \(\mathrm{A}_{\mathrm{i}}\) & None & \begin{tabular}{l}
Remaining \\
A
\end{tabular} & \[
\begin{aligned}
& \text { Remaining } \\
& B, C_{n}
\end{aligned}
\] & \(\mathrm{F}_{\mathrm{i}}\) & Out-of-Phase \\
\hline \[
\frac{t_{\mathrm{PLH}}}{t_{\mathrm{PHLL}}}
\] & \(A_{i}\) & None & \(\mathrm{B}_{\mathrm{i}}\) & None & Remaining \(A\) and \(B, C_{n}\) & P & In-Phase \\
\hline \[
\frac{t_{\text {PLH }}}{t_{\text {PHL }}}
\] & \(\mathrm{B}_{\mathrm{i}}\) & \(\mathrm{A}_{\mathrm{i}}\) & None & None & Remaining \(A\) and \(B, C_{n}\) & P & Out-of-Phase \\
\hline \[
\frac{\mathrm{t}_{\mathrm{PLH}}}{\mathrm{t}_{\mathrm{PHL}}}
\] & \(A_{i}\) & \(\mathrm{B}_{\mathrm{i}}\) & None & None & Remaining \(A\) and \(B, C_{n}\) & G & In-Phase \\
\hline \[
\frac{t_{\mathrm{PLH}}}{\mathrm{t}_{\mathrm{PHL}}}
\] & \(\mathrm{B}_{\mathrm{i}}\) & None & \(\mathrm{A}_{\mathrm{i}}\) & None & Remaining \(A\) and \(B, C_{n}\) & G & Out-of-Phase \\
\hline \({ }_{\text {tPLH }}\) & \(A_{i}\) & None & \(B_{i}\) & \[
\begin{gathered}
\text { Remaining } \\
\text { A }
\end{gathered}
\] & \[
\begin{aligned}
& \text { Remaining } \\
& B, C_{n}
\end{aligned}
\] & \(A=B\) & In-Phase \\
\hline \({ }_{\text {tPLH }}\) & \(\mathrm{B}_{\mathrm{i}}\) & \(A_{i}\) & None & \[
\begin{gathered}
\text { Remaining }
\end{gathered}
\] & \[
\begin{aligned}
& \text { Remaining } \\
& B, C_{n}
\end{aligned}
\] & \(A=B\) & Out-of-Phase \\
\hline \(\mathrm{tpLH}^{\text {tpHL }}\) & \(C_{n}\) & None & None & All \(A\) and \(B\) & None & \begin{tabular}{l}
\[
C_{n}+4
\] \\
or any F
\end{tabular} & In-Phase \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & \(A_{i}\) & \(\mathrm{B}_{\mathrm{i}}\) & None & None & Remaining \(A, B, C_{n}\) & \(\mathrm{C}_{n}+4\) & Out-of-Phase \\
\hline \({ }_{\text {tpLH }}\) & \(\mathrm{B}_{\mathrm{i}}\) & None & \(A_{i}\) & None & Remaining \(A, B, C_{n}\) & \(C_{n}+4\) & In-Phase \\
\hline
\end{tabular}

\(V_{C C}=\) PIN 24
GND \(=\) PIN 12

\section*{DM74184/DM74185A}

BCD-to-Binary and Binary-to-BCD Converters

\section*{General Description}

These monolithic converters are derived from the 256-bit read only memories, DM5488, and DM7488. Emitter connections are made to provide direct read-out of converted codes at outputs Y8 through Y1, as shown in the function tables. These converters demonstrate the versatility of a read only memory in that an unlimited number of reference tables or conversion tables may be built into a system. Both of these converters comprehend that the least significant bits (LSB) of the binary and BCD codes are logically equal, and in each case the LSB bypasses the converter as illustrated in the typical applications. This means that a 6 -bit converter is produced in each case. Both devices are cascadable to N bits.
An overriding enable input is provided on each converter which when taken high inhibits the function, causing all outputs to go high. For this reason, and to minimize power consumption, unused outputs Y 7 and Y 8 of the 185A and all "don't care" conditions of the 184 are programmed high. The outputs are of the open-collector type.

\section*{DM74184 BCD-TO-BINARY CONVERTERS}

The 6-bit BCD-to-binary function of the DM74184 is analogous to the algorithm:
a. Shift BCD number right one bit and examine each decade. Subtract three from each 4-bit decade containing a binary value greater than seven.
b. Shift right, examine, and correct after each shift until the least significant decade contains a number smaller than eight and all other converted decades contain zeros.
In addition to BCD-to-binary conversion, the DM74184 is programmed to generate BCD 9's complement or BCD 10's complement. Again, in each case, one bit of the complement code is logically equal to one of the BCD bits; therefore, these complements can be produced on three lines. As outputs \(\mathrm{Y} 6, \mathrm{Y} 7\) and Y 8 are not required in the BCD-to-binary conversion, they are utilized to provide these complement codes as specified in the function table when the devices are connected as shown.

\section*{DM74185A BINARY-TO-BCD CONVERTERS}

The function performed by these 6 -bit binary-to-BCD converters is analogous to the algorithm:
a. Examine the three most significant bits. If the sum is greater than four, add three and shift left one bit.
b. Examine each BCD decade. If the sum is greater than four, add three and shift left one bit.
c. Repeat step \(b\) until the least-significant binary bit is in the least-significant BCD location.
(Continued)

\section*{Connection Diagram}


\section*{Absolute Maximum Ratings (Note)}

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
\begin{tabular}{lr} 
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Output Voltage & 7 V \\
Operating Free Air Temperature & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c}
\hline Symbol & Parameter & Min & Nom & Max & Units \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline \(\mathrm{~V}_{\mathrm{OH}}\) & High Level Output Voltage & & & 5.5 & V \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 12 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{'184 and '185A Electrical Characteristics}
over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline ICEX & High Level Output Current & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{O}}=5.5 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\] & & & 100 & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline 1 IH & High Level Input Current & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 25 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -1 & mA \\
\hline \({ }^{\text {ICCH }}\) & Supply Current with Outputs High & \(\mathrm{V}_{\text {CC }}=\) Max & & 65 & 95 & mA \\
\hline \({ }^{\text {I CCL }}\) & Supply Current with Outputs Low & \(V_{C C}=\operatorname{Max}\) & & 80 & 99 & mA \\
\hline
\end{tabular}

\section*{'184 and '185A Switching Characteristics}
at \(V_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\[
\begin{gathered}
R_{\mathrm{L} 1}=400 \Omega, R_{\mathrm{L} 2}=600 \Omega \\
\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \text { (See Test Circuit) }
\end{gathered}
\]} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & Enable G to Output & & 35 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Enable G to Output & & 35 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Binary Select to Output & & 35 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Binary Select to Output & & 35 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).

\section*{General Description (Continued)}

DM74184 BCD-to-Binary
TABLE I. Package Count and Delay Times for BCD-to-Binary Conversion
\begin{tabular}{|c|c|c|c|}
\hline \multirow{2}{*}{\begin{tabular}{c} 
Input \\
(Decades)
\end{tabular}} & \multirow{2}{|c|}{\begin{tabular}{c} 
Packages \\
Required
\end{tabular}} & \multicolumn{2}{|c|}{ Total Delay Times (ns) } \\
\cline { 3 - 4 } & & Typ & Max \\
\hline 2 & 2 & 56 & 80 \\
3 & 6 & 140 & 200 \\
4 & 12 & 196 & 280 \\
5 & 19 & 280 & 400 \\
6 & 28 & 364 & 520 \\
\hline
\end{tabular}

BCD 9's Complement Converter


TL/F/6561-3

DM74185A Binary-to-BCD

TABLE II. Package Count and Delay Times
for Binary-to-BCD Conversion
\begin{tabular}{|c|c|c|c|}
\hline \multirow{2}{*}{\begin{tabular}{c} 
Input \\
(Bits)
\end{tabular}} & \multirow{2}{*|}{\begin{tabular}{c} 
Packages \\
Required
\end{tabular}} & \multicolumn{2}{|c|}{ Total Delay Times (ns) } \\
\cline { 3 - 4 } & & Typ & Max \\
\hline 4 to 6 & 1 & 25 & 40 \\
7 or 8 & 3 & 50 & 80 \\
9 & 4 & 75 & 120 \\
10 & 6 & 100 & 160 \\
11 & 7 & 125 & 200 \\
12 & 8 & 125 & 200 \\
13 & 10 & 150 & 240 \\
14 & 12 & 175 & 280 \\
15 & 14 & 175 & 280 \\
16 & 16 & 200 & 320 \\
17 & 19 & 225 & 360 \\
18 & 21 & 225 & 360 \\
19 & 24 & 250 & 400 \\
20 & 27 & 275 & 440 \\
\hline
\end{tabular}


TL/F/6561-4

\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{2}{|r|}{\multirow[t]{3}{*}{Binary Words}} & \multicolumn{6}{|c|}{Inputs} & \multicolumn{8}{|c|}{Outputs} \\
\hline & & \multicolumn{5}{|c|}{Binary Select} & \multirow[t]{2}{*}{Enable G} & \multirow[b]{2}{*}{Y8} & \multirow[b]{2}{*}{Y7} & \multirow[b]{2}{*}{Y6} & \multirow[b]{2}{*}{Y5} & \multirow[b]{2}{*}{Y4} & \multirow[b]{2}{*}{Y3} & \multirow[b]{2}{*}{Y2} & \multirow[b]{2}{*}{Y1} \\
\hline & & E & D & C & B & A & & & & & & & & & \\
\hline 0 & 1 & L & L & L & L & L & L & H & H & L & L & L & L & L & L \\
\hline 2 & 3 & L & L & L & L & H & L & H & H & L & L & L & L & L & H \\
\hline 4 & 5 & L & L & L & H & L & L & H & H & L & L & L & L & H & L \\
\hline 6 & 7 & L & L & L & H & H & L & H & H & L & L & L & L & H & H \\
\hline 8 & 9 & L & L & H & L & L & L & H & H & L & L & L & H & L & L \\
\hline 10 & 11 & L & L & H & L & H & L & H & H & L & L & H & L & L & L \\
\hline 12 & 13 & L & L & H & H & L & L & H & H & L & L & H & L & L & H \\
\hline 14 & 15 & L & L & H & H & H & L & H & H & L & L & H & L & H & L \\
\hline 16 & 17 & L & H & L & L & L & L & H & H & L & L & H & L & H & H \\
\hline 18 & 19 & L & H & L & L & H & L & H & H & L & L & H & H & L & L \\
\hline 20 & 21 & L & H & L & H & L & L & H & H & L & H & L & L & L & L \\
\hline 22 & 23 & L & H & L & H & H & L & H & H & L & H & L & L & L & H \\
\hline 24 & 25 & L & H & H & L & L & L & H & H & L & H & L & L & H & L \\
\hline 26 & 27 & L & H & H & L & H & L & H & H & L & H & L & L & H & H \\
\hline 28 & 29 & L & H & H & H & L & L & H & H & L & H & L & H & L & L \\
\hline 30 & 31 & L & H & H & H & H & L & H & H & L & H & H & L & L & L \\
\hline 32 & 33 & H & L & L & L & L & L & H & H & L & H & H & L & L & H \\
\hline 34 & 35 & H & L & L & L & H & L & H & H & L & H & H & L & H & L \\
\hline 36 & 37 & H & L & L & H & L & L & H & H & L & H & H & L & H & H \\
\hline 38 & 39 & H & L & L & H & H & L & H & H & L & H & H & H & L & L \\
\hline 40 & 41 & H & L & H & L & L & L & H & H & H & L & L & L & L & L \\
\hline 42 & 43 & H & L & H & L & H & L & H & H & H & L & L & L & L & H \\
\hline 44 & 45 & H & L & H & H & L & L & H & H & H & L & L & L & H & L \\
\hline 46 & 47 & H & L & H & H & H & L & H & H & H & L & L & L & H & H \\
\hline 48 & 49 & H & H & L & L & L & L & H & H & H & L & L & H & L & L \\
\hline 50 & 51 & H & H & L & L & H & L & H & H & H & L & H & L & L & L \\
\hline 52 & 53 & H & H & L & H & L & L & H & H & H & L & H & L & L & H \\
\hline 54 & 55 & H & H & L & H & H & L & H & H & H & L & H & L & H & L \\
\hline 56 & 57 & H & H & H & L & L & L & H & H & H & L & H & L & H & H \\
\hline 58 & 59 & H & H & H & L & H & L & H & H & H & L & H & H & L & L \\
\hline 60 & 61 & H & H & H & H & L & L & H & H & H & H & L & L & L & L \\
\hline 62 & 63 & H & H & H & H & H & L & H & H & H & H & L & L & L & H \\
\hline \multicolumn{2}{|c|}{All} & X & X & X & X & X & H & H & H & H & H & H & H & H & H \\
\hline
\end{tabular}

Function Tables (Continued)
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{13}{|c|}{BCD-to-Binary Converter} & \multicolumn{10}{|c|}{BCD 9's or BCD 10's Complement Converter} \\
\hline \multicolumn{2}{|l|}{\multirow[t]{2}{*}{\begin{tabular}{l}
BCD \\
Words
\end{tabular}}} & \multicolumn{5}{|c|}{Inputs (See Note A)} & \multicolumn{6}{|c|}{Outputs (See Note B)} & \multirow[t]{2}{*}{\begin{tabular}{l}
BCD \\
Word
\end{tabular}} & \multicolumn{6}{|c|}{Inputs (See Note C)} & \multicolumn{3}{|l|}{Outputs (See Note D)} \\
\hline & & & C & C B & A & G & Y5 & Y 4 & 4 & Y3 & Y2 & Y1 & & \(\mathrm{E} \dagger\) & D & C & B & A & G & Y8 & Y7 & Y6 \\
\hline 0 & 1 & & L & L L & L & L & L & & & L & L & L & 0 & L & L & L & L & L & L & H & L & H \\
\hline 2 & 3 & & L & L L & H & L & L & & & & L & H & 1 & L & L & L & L & H & L & H & L & L \\
\hline 4 & 5 & & L & L H & H L & L & L & L & L & L & H & L & 2 & L & L & L & H & L & L & L & H & H \\
\hline 6 & 7 & L & L & L H & H H & L & L & L & L & L & H & H & 3 & L & L & L & H & H & L & L & H & L \\
\hline 8 & 9 & L & H & H L & L & L & L & L & L & H & L & L & 4 & L & L & H & L & L & L & L & H & H \\
\hline 10 & 11 & & H L & L L & L & L & L & & & H & L & H & 5 & L & L & H & L & H & L & L & H & L \\
\hline 12 & 13 & L & H & L L & H & L & L & L & L & H & H & L & 6 & L & L & H & H & L & L & L & L & H \\
\hline 14 & 15 & L & L & L H & H L & L & L & L & L & H & H & H & 7 & L & L & H & H & H & L & L & L & L \\
\hline 16 & 17 & L & L & L H & H & L & L & H & H & L & L & L & 8 & L & H & L & L & L & L & L & L & H \\
\hline 18 & 19 & L & H & H L & L & L & L & H & H & L & L & H & 9 & L & H & L & L & H & L & L & L & L \\
\hline 20 & 21 & & L & L L & L & L & L & & H & L & H & L & 0 & H & L & L & L & L & L & L & L & L \\
\hline 22 & 23 & H & L & L L & H & L & L & H & H & L & H & H & 1 & H & L & L & L & H & L & H & L & L \\
\hline 24 & 25 & H & L & L H & H L & L & L & H & H & H & L & L & 2 & H & L & L & H & L & L & H & L & L \\
\hline 26 & 27 & H & L & L H & H H & L & L & H & H & H & L & H & 3 & H & L & L & H & H & L & L & H & H \\
\hline 28 & 29 & H & H & H L & L & L & L & H & H & H & H & L & 4 & H & L & H. & L & L & L & L & H & H \\
\hline 30 & 31 & H & H L & L L & L & L & L & H & H & H & H & H & 5 & H & L & H & L & H & L & L & H & L \\
\hline 32 & 33 & H & H L & L L & - H & L & H & L & L & L & L & L & 6 & H & L & H & H & L & L & L & H & L \\
\hline 34 & 35 & H & H L & L H & H L & L & H & L & L & L & L & H & 7 & H & L & H & H & H & L & L & L & H \\
\hline 36 & 37 & H & H & L H & H & L & H & & L & L & H & L & 8 & H & H & L & L & L & L & L & L & H \\
\hline 38 & 39 & H & H & H L & L L & L & H & L & L & L & H & H & 9 & H & H & L & L & H & L & L & \(L\) & L \\
\hline & & X & \(\times \times\) & \(\times \times\) & \(\times \times\) & H & H & H & H & H & H & H & Any & X & X & X & X & X & H & H & H & H \\
\hline
\end{tabular}
\(H=\) High Level, \(L=\) Low Level, \(X=\) Don't Care
Note A: Input Conditions other than those shown produce highs at outputs Y 1 through Y5.
Note B: Output Y6, Y7, and Y8 are not used for BCD-to-Binary conversion.
Note \(C\) : Input conditions other than those shown produce highs at outputs \(Y 6, Y 7\), and \(Y 8\).
Note D: Outputs Y1 through Y5 are not used for BCD 9's or BCD 10's complement conversion.
\(\dagger\) When these devices are used as complement converters, input E is used as a mode control. With this input low, the BCD 9's complement is generated; when it is high, the BCD 10's complement is generated.

\section*{Test Circuit}


TL/F/6561-6
\(C_{\text {L includes probe and jig capacitance }}\)

\section*{Typical Applications}


TL/F/6561-7
FIGURE 1. BCD-to-Binary Converter for Two BCD Decades
MSD-Most significant decade
LSD-Least significant decade
Each rectangle represents a DM74184


FIGURE 2. BCD-to-Binary Converter for Six BCD Decades
MSD-Most significant decade
LSD-Least significant decade
Each rectangle represents a DM74184

Typical Applications (Continued)


TL/F/6561-8
FIGURE 3. BCD-to-Binary Converter for Three BCD Decades
MSD-Most significant decade
LSD-Least significant decade
Each rectangle represents a DM74184


TL/F/6561-11
FIGURE 5. 8-Bit Binary-to-BCD Converter
MSD-Most significant decade
LSD-Least significant decade
Note A: Each rectangle represents a DM74185A.
Note B: All unused E inputs are grounded.


FIGURE 4. 6-Bit Binary-to-BCD Converter
MSD-Most significant decade
LSD-Least significant decade
Note A: Each rectangle represents a DM74185A.
Note B: All unused E inputs are grounded.


TL/F/6561-12
FIGURE 6. 9-Bit Binary-to-BCD Converter
MSD-Most significant decade
LSD-Least significant decade
Note A: Each rectangle represents a DM74185A.
Note B: All unused E inputs are grounded.


FIGURE 7. 12-Bit Binary-to-BCD Converter (See Note B)


FIGURE 8. 16-Bit Binary-to-BCD Converter (See Note B)

MSD—Most significant decade
LSD-Least significant decade
Note A: Each rectangle represents a DM74185A.
Note B: All unused E inputs are grounded.

\section*{54191/DM54191/DM74191 Synchronous Up/Down 4-Bit Binary Counter with Mode Control}

\section*{General Description}

This circuit is a synchronous, reversible, up/down counter. The 191 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.
The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/ up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.
This counter is fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs. The clock, down/up, and load inputs are buffered to lower the drive requirement; which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

\section*{Features}
- Single down/up count control line
- Count enable control input
- Ripple clock output for cascading
- Asynchronously presettable with load control
- Parallel outputs
- Cascadable for n -bit applications
- Alternate Military/Aerospace device (54191) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

\section*{Connection Diagram}



Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54191} & \multicolumn{3}{|c|}{DM74191} & \multirow{2}{*}{Units} \\
\hline & & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\text {CC }}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
\hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.8 & & & -0.8 & mA \\
\hline IOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & & & 16 & mA \\
\hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 4)} & 0 & & 20 & 0 & & 20 & MHz \\
\hline \multirow[t]{2}{*}{tw} & \multirow[t]{2}{*}{Pulse Width (Note 4)} & Clock & 25 & & & 25 & & & \\
\hline & & Load & 35 & & & 35 & & & \\
\hline \({ }_{\text {tSu }}\) & \multicolumn{2}{|l|}{Data Setup Time (Note 4)} & 28 & & & 28 & & & ns \\
\hline \(t_{H}\) & \multicolumn{2}{|l|}{Hold Time (Note 4)} & 0 & & & 0 & & & ns \\
\hline \(\mathrm{t}_{\text {REL }}\) & \multicolumn{2}{|l|}{Load Release Time (Note 4)} & 30 & & & 30 & & & ns \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{2}{*}{\(\mathrm{I}_{\mathrm{H}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Max} \\
& V_{1}=2.4 \mathrm{~V}
\end{aligned}
\]} & Enable & & & 120 & \multirow{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Others & & & 40 & \\
\hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{c C}=M a x \\
& V_{1}=0.4 V
\end{aligned}
\]} & Enable & & & -4.8 & \multirow[t]{2}{*}{mA} \\
\hline & & & Others & & & -1.6 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=\text { Max } \\
& \text { (Note 2) }
\end{aligned}
\]} & DM54 & -20 & & -65 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -65 & \\
\hline \multirow[t]{2}{*}{ICC} & \multirow[t]{2}{*}{Supply Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=M a x
\] \\
(Note 3)
\end{tabular}} & DM54 & & 65 & 99 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & & 65 & 105 & \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: I ICC is measured with all inputs grounded and all outputs open.
Note 4: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

Switching Characteristics at \(\mathrm{V}_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(f_{\text {MAX }}\) & Maximum Clock Frequency & & 20 & & MHz \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Load to Any Q & & 33 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Load to Any Q & & 70 & ns \\
\hline \(t_{\text {PLLH }}\) & Propagation Delay Time Low to High Level Output & \begin{tabular}{l}
Data to \\
Any Q
\end{tabular} & & 22 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to Any Q & & 70 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Ripple Carry & & 20 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Ripple Carry & & 24 & ns \\
\hline \({ }_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output & Clock to Any Q & & 24 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Any Q & & 36 & ns \\
\hline tplH & Propagation Delay Time Low to High Level Output & Clock to Max/Min & & 42 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Max/Min & & 52 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Down/Up to Ripple Carry & & 45 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Down/Up to Ripple Carry & & 45 & ns \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & Down/Up to Max/Min & & 33 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Down/Up to Max/Min & & 33 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Enable G to Ripple Carry & & 24 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Enable G to Ripple Carry & & 24 & ns \\
\hline
\end{tabular}

191 Binary Counter


191 Decade Counter
Typical Load, Count, and Inhibit Sequences


TL/F/6562-3

\section*{DM54193 Synchronous Up/Down 4-Bit Binary Counter with Dual Clock}

\section*{General Description}

This circuit is a synchronous up/down 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.
The outputs of the four master-slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed, while the other count input is held high.
This counter is fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is low. The output will change independently of the count pulses. This feature allows the counter to be used as modulo-N divider by simply modifying the count length with the preset inputs.
A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

This counter was designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up and down counting functions. The borrow output produces a pulse equal in width to the count down input when the counter underflows. Similarly , the carry output produces a pulse equal in width to the count up input when an overflow condition exists. The counter can then be easily cascaded by feeding the borrow and carry outputs to the count down and count up inputs respectively of the succeeding counter.

\section*{Features}
- Fully independent clear input
- Synchronous operation
- Cascading circuitry provided internally
- Individual preset each flip-flop

\section*{Connection Diagram}


TL/F/6563-1
Order Number DM54193J or DM54193W
See NS Package Number J16A or W16A
```

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for availability and specifications.
Supply Voltage
7V
Input Voltage
5.5V
Operating Free Air Temperature
Range -
Storage Temperature Range -65'C to +150 %

```

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & \multicolumn{2}{|c|}{Parameter} & Min & Nom & Max & Units \\
\hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & V \\
\hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & mA \\
\hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & mA \\
\hline fCLK & \multicolumn{2}{|l|}{Clock Frequency (Note 4)} & 0 & 25 & 20 & MHz \\
\hline \multirow[t]{2}{*}{tw} & \multirow[t]{2}{*}{Pulse Width (Note 4)} & Clock Low & 30 & & & \\
\hline & & Clock, Clear High Load Low & 20 & & & ns \\
\hline tsu & \multicolumn{2}{|l|}{Data Setup Time (Note 4)} & 20 & & & ns \\
\hline \(t_{H}\) & \multicolumn{2}{|l|}{Hold Time (Note 4)} & 0 & & & ns \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOH}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\] & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\] & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \(V_{C C}=\) Max, \(\mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline los & Short Circuit Output Current & \(V_{C C}=\operatorname{Max}\) (Note 2) & \(-20\) & & -55 & mA \\
\hline ICC & Supply Current & \(V_{C C}=\operatorname{Max}\) (Note 3) & & 65 & 89 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: ICC is measured with all outputs open, CLEAR and LOAD inputs grounded, and all other inputs at 4.5 V .
Note 4: \(T_{A}=25^{\circ} \mathrm{C}\) and \(V_{C C}=5 \mathrm{~V}\).

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 20 & & MHz \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & Count Up to Carry & & 26 & ns \\
\hline tPHL & Propagation Delay Time High to Low Level Output & Count Up to Carry & & 24 & ns \\
\hline tple & Propagation Delay Time Low to High Level Output & Count Down to Borrow & & 24 & ns \\
\hline tpHL & Propagation Delay Time High to Low Level Output & Count Down to Borrow & & 24 & ns \\
\hline tplH & Propagation Delay Time Low to High Level Output & \[
\begin{gathered}
\text { Either Count } \\
\text { to Q } \\
\hline
\end{gathered}
\] & & 38 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Either Count
\[
\text { to } Q
\] & & 47 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
\begin{aligned}
& \text { Load } \\
& \text { to } Q
\end{aligned}
\] & & 40 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
Load \\
to Q
\end{tabular} & & 40 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
\begin{aligned}
& \text { Clear } \\
& \text { to Q }
\end{aligned}
\] & & 35 & ns \\
\hline
\end{tabular}


193 Binary Counter
Typical Clear, Load, and Count Sequences


TL/F/6563-3

Note A: Clear overrides load, data, and count inputs.
Note B: When counting up, count-down input must be high, when counting down, count-up input must be high.

\section*{DM54194}

\section*{4-Bit Bidirectional Universal Shift Registers}

\section*{General Description}

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register; it features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

\section*{Parallel (broadside) load}

Shift right (in the direction \(Q_{A}\) toward \(Q_{D}\) )
Shift left (in the direction \(Q_{D}\) toward \(Q_{A}\) )
Inhibit clock (do nothing)
Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data is loaded into the associated flipflops and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.
Shift right is accomplished synchronously with the rising edge of the clock pulse when S 0 is high and S 1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left syn chronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls of the DM54194/ DM74194 should be changed only while the clock input is high.

\section*{Features}
- Parallel inputs and outputs
- Four operating modes:

Synchronous parallel load
Right shift
Left shift
Do nothing
圖 Positive edge-triggered clocking
(1) Direct overriding clear

国 Typical clock frequency 36 MHz
- Typical power dissipation 195 mW

\section*{Connection Diagram}


Order Number DM54194J or DM54194W See NS Package Number J16A or W16A
\begin{tabular}{lr} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the Natlonal Semliconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
\begin{tabular}{lr} 
Operating Free Air Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM54 & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular} Storage Temperature Range &
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54194} & \multirow{2}{*}{Units} \\
\hline & & & Min & Nom & Max & \\
\hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & V \\
\hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.8 & mA \\
\hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & mA \\
\hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 4)} & 0 & 36 & 25 & MHz \\
\hline \multirow[t]{2}{*}{\(t_{W}\)} & \multirow[t]{2}{*}{Pulse Width (Note 4)} & Clock & 20 & & & \multirow[t]{2}{*}{ns} \\
\hline & & Clear & 20 & & & \\
\hline \multirow[t]{2}{*}{tsu} & \multirow[t]{2}{*}{Setup Time (Note 4)} & Mode & 30 & & & \multirow[t]{2}{*}{ns} \\
\hline & & Data & 20 & & & \\
\hline \(t_{H}\) & \multicolumn{2}{|l|}{Hold Time (Note 4)} & 0 & & & ns \\
\hline \(t_{\text {REL }}\) & \multicolumn{2}{|l|}{Clear Release Time (Note 4)} & 25 & & & ns \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) }
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\text {CC }}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\] & 2.4 & 3.4 & & V \\
\hline VOL & Low Level Output Voltage & \[
\begin{aligned}
& V_{C C}=\operatorname{Min}, \mathrm{l}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\] & & 0.2 & 0.4 & V \\
\hline \(\|\) & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{IIH}_{\mathrm{H}}\) & High Level Input Current & \(V_{C C}=M a x, V_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline los & Short Circuit Output Current & \(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 2) & -20 & & -57 & mA \\
\hline Icc & Supply Current & \(V_{C C}=\operatorname{Max}\) (Note 3) & & 39 & 63 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{A}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: With all outputs open, inputs A through D grounded, and 4.5 V applied to SO, S1, CLEAR and the serial inputs, ICC is tested with a momentary ground, then 4.5 V applied to CLOCK.

Note 4: \(T_{A}=25^{\circ} \mathrm{C}\) and \(V_{C C}=5 \mathrm{~V}\).

Switching Characteristics at \(\mathrm{V}_{C C}=5 V_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 25 & & MHz \\
\hline \({ }_{\text {tpLH }}\) & Propagation Delay Time Low to High Level Output & \[
\begin{aligned}
& \text { Clock } \\
& \text { to Q }
\end{aligned}
\] & & 22 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Q & & 26 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
\begin{aligned}
& \text { Clear } \\
& \text { to } \mathrm{Q}
\end{aligned}
\] & & 30 & ns \\
\hline
\end{tabular}

Function Table
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{10}{|c|}{Inputs} & \multicolumn{4}{|c|}{Outputs} \\
\hline \multirow[t]{2}{*}{Clear} & \multicolumn{2}{|c|}{Mode} & \multirow[t]{2}{*}{Clock} & \multicolumn{2}{|c|}{Serial} & \multicolumn{4}{|c|}{Parallel} & \multirow[t]{2}{*}{\(Q_{A}\)} & \multirow[t]{2}{*}{\(Q_{B}\)} & \multirow{2}{*}{\(Q_{C}\)} & \multirow[t]{2}{*}{\(Q_{D}\)} \\
\hline & S1 & so & & Left & Right & A & B & c & D & & & & \\
\hline L & x & X & X & x & X & X & X & x & X & L & L & L & L \\
\hline H & X & X & L & X & X & X & X & X & X & \(Q_{A 0}\) & \(Q_{B 0}\) & \(Q_{c o}\) & \(Q_{\text {Do }}\) \\
\hline H & H & H & \(\uparrow\) & x & X & a & b & c & d & a & b & & d \\
\hline H & L & H & \(\uparrow\) & X & H & x & x & x & x & H & \(\mathrm{Q}_{\text {An }}\) & \(\mathrm{Q}_{\mathrm{Bn}}\) & \(Q_{C n}\) \\
\hline H & L & H & \(\uparrow\) & x & L & X & x & x & X & L & \(\mathrm{Q}_{\text {An }}\) & \(\mathrm{Q}_{\mathrm{Bn}}\) & \(\mathrm{Q}_{\mathrm{c}}\) \\
\hline H & H & L & \(\uparrow\) & H & X & X & x & X & x & \(\mathrm{Q}_{\mathrm{Bn}}\) & \(Q_{\mathrm{Cn}}\) & QDn & H \\
\hline H & H & L & \(\uparrow\) & & x & x & x & x & x & \(\mathrm{Q}_{\mathrm{Bn}}\) & \(Q_{\text {cn }}\) & \(Q_{\text {Dn }}\) & L \\
\hline H & L & L & X & X & X & x & x & x & x & \(\mathrm{Q}_{\text {A0 }}\) & \(\mathrm{Q}_{\text {B0 }}\) & \(\mathrm{Q}_{\mathrm{co}}\) & \(Q_{D 0}\) \\
\hline
\end{tabular}
\(\mathrm{H}=\) High Level (steady state), \(\mathrm{L}=\) Low Level (steady state), \(\mathrm{X}=\) Don't Care (any input, including transitions)
\(\uparrow=\) Transition from low to high level; \(a, b, c, d=\) The level of steady state input at inputs \(A, B, C\), or \(D\), respectively
\(Q_{A 0}, Q_{B 0}, Q_{C 0}, Q_{D 0}=\) The level of \(Q_{A}, Q_{B}, Q_{C}\), or \(Q_{D}\), respectively, before the indicated steady state input conditions were established.
\(Q_{A n}, Q_{B n}, Q_{C n}, Q_{D n}=\) The level of \(Q_{A}, Q_{B}, Q_{C}\), respectively, before the most recent \(\uparrow\) transition of the clock.


\section*{Timing Diagram}

Typical Clear, Load, Right-Shift, Left-Shift, Inhibit and Clear Sequences


TL/F/6564-3

\section*{DM74197}

\section*{Presettable Binary Counters}

\section*{General Description}

The '197 ripple counter contains divide-by-two and divide-by-eight sections which can be combined to form a modulo16 binary counter. State changes are initiated by the falling edge of the clock. The ' 197 has a Master Reset ( \(\overline{\mathrm{MR}}\) ) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input ( \(\overline{\mathrm{PL}}\) ) overrides
clocked operations and asynchronously loads the data on the Parallel Data inputs \(\left(P_{n}\right)\) into the flip-flops. This preset feature makes the circuit usable as a programmable counter. The circuit can also be used as a 4-bit latch, loading data from the Parallel Data inputs when \(\overline{P L}\) is LOW and storing the data when PL is HIGH.

\section*{Connection Diagram}

\begin{tabular}{|c|c|}
\hline Pin Names & Description \\
\hline \(\overline{\mathrm{CP}}\) & \(\div 2\) Section Clock Input (Active Falling Edge) \\
\hline \(\overline{\mathrm{CP}} 1\) & \(\div 8\) Section Clock Input (Active Falling Edge) \\
\hline \(\overline{\mathrm{MR}}\) & Asynchronous Master Reset Input (Active LOW) \\
\hline P0-P3 & Parallel Data Inputs \\
\hline \(\overline{\mathrm{PL}}\) & Asynchronous Parallel Load Input (Active LOW) \\
\hline Q0 & \(\div 2\) Section Output* \\
\hline Q1-Q3 & \(\div 8\) Section Outputs \\
\hline
\end{tabular}
*Q0 output is guaranteed to drive the full rated fan-out plus the \(\overline{\mathrm{CP}} 1\) input.

\section*{Absolute Maximum Ratings}

If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
7V
Input Voltage
5.5 V

Operating Free Air Temperature Range
DM74
Storage Temperature Range

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM74197} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline \(\mathrm{IOH}^{\text {l }}\) & High Level Output Current & & & -0.25 & mA \\
\hline IOL & Low Level Output Current & & & 16 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
& \mathrm{t}_{\mathrm{s}}(\mathrm{~L})
\end{aligned}
\] & Setup Time HIGH or LOW \(P_{n}\) to \(\overline{P L}\) & \[
\begin{aligned}
& 10 \\
& 15
\end{aligned}
\] & & & ns \\
\hline \[
\begin{aligned}
& t_{h}(H) \\
& t_{h}(L) \\
& \hline
\end{aligned}
\] & Hold Time HIGH or LOW \(P_{n}\) to \(\overline{P L}\) & \[
\begin{aligned}
& 0 \\
& 0
\end{aligned}
\] & & & ns \\
\hline \(t_{w}(\mathrm{H})\) & \(\overline{\mathrm{CP}} 0\) Pulse Width HIGH & 20 & & & ns \\
\hline \(t_{w}(H)\) & \(\overline{\text { CP1 Pulse Width HIGH }}\) & 30 & & & ns \\
\hline \(t_{w}(L)\) & PL Pulse Width LOW & 20 & & & ns \\
\hline \(t_{w}(L)\) & \(\overline{M R}\) Pulse Width LOW & 15 & & & ns \\
\hline \(t_{\text {rec }}\) & Recovery Time \(\overline{\mathrm{PL}}\) to \(\overline{\mathrm{CP}}_{n}\) & 20 & & & ns \\
\hline \(\mathrm{t}_{\text {rec }}\) & Recovery Time \(\overline{\mathrm{MR}}\) to \(\overline{\mathrm{CP}}_{\mathrm{n}}\) & 20 & & & ns \\
\hline
\end{tabular}

\section*{Electrical Characteristics}

Over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\] & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \multirow[t]{2}{*}{\(\mathrm{I}_{\mathrm{H}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \(V_{C C}=M a x, V_{1}=5.5 \mathrm{~V}, \overline{C P}_{1}\) & & & 1 & mA \\
\hline & & \(V_{C C}=\) Max, \(V_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline los & Short Circuit Output Current & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
& \text { (Note 2) } \\
& \hline
\end{aligned}
\] & -18 & & -57 & mA \\
\hline ICC & Supply Current & \(\mathrm{V}_{\mathrm{CC}}=\) Max, All Inputs \(=\) GND & & & 59 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

Switching Characteristics
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{3}{*}{Symbol} & \multirow[t]{3}{*}{Parameter} & \multicolumn{2}{|c|}{\(C_{L}=15 \mathrm{pF}\)} & \multirow[t]{3}{*}{Units} \\
\hline & & \multicolumn{2}{|c|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega\)} & \\
\hline & & Min & Max & \\
\hline \(f_{\text {max }}\) & \begin{tabular}{l}
Maximum Count \\
Frequency at \(\overline{\mathrm{CP}} 0\)
\end{tabular} & 50 & & MHz \\
\hline \(\mathrm{f}_{\text {max }}\) & \begin{tabular}{l}
Maximum Count \\
Frequency at \(\overline{\mathrm{CP}} 1\)
\end{tabular} & 25 & & MHz \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay \(\overline{\mathrm{CPO}}\) to Q0 & & \[
\begin{aligned}
& 12 \\
& 15 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay \(\overline{\mathrm{CP}} 1\) to Q1 & & \[
\begin{aligned}
& 18 \\
& 21
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}}
\end{aligned}
\] & Propagation Delay \(\overline{\mathrm{CP}} 1\) to Q2 & & \[
\begin{aligned}
& 36 \\
& 42 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay \(\overline{\mathrm{CP}} 1\) to Q3 & & \[
\begin{aligned}
& 54 \\
& 63
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay
\[
P_{n} \text { to } Q_{n}
\] & & \[
\begin{aligned}
& 24 \\
& 38 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay \(\overline{P L}\) to \(Q_{n}\) & & \[
\begin{aligned}
& 33 \\
& 36 \\
& \hline
\end{aligned}
\] & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay \(\overline{\mathrm{MR}}\) to \(Q_{n}\) & & 37 & ns \\
\hline
\end{tabular}

\section*{Logic Symbol}


TL/F/9784-2
\(V_{C C}=\operatorname{Pin} 14\)
\(\mathrm{GND}=\operatorname{Pin} 7\)
\begin{tabular}{|c|c|c|l|}
\hline \multicolumn{4}{|c|}{ Mode Selection Table } \\
\hline \multicolumn{3}{|c|}{ Inputs } & \multirow{2}{*}{ Response } \\
\hline\(\overline{\mathbf{M R}}\) & \(\overline{\mathbf{P L}}\) & \(\overline{\mathbf{C P}}\) & \\
\hline L & X & X & \multicolumn{2}{|c|}{\(\mathrm{Q}_{\mathrm{n}}\) Forced LOW } \\
H & L & X & \(\mathrm{P}_{\mathrm{n}} \rightarrow \mathrm{Q}_{\mathrm{n}}\) \\
H & H & - & Count Up \\
\hline
\end{tabular}
\(H=H I G H\) Voltage Level
L = LOW Voltage Level
\(\mathrm{X}=\) Immaterial


\section*{Logic Diagram}


TL/F/9784-4

\section*{54279/DM74279 Quad Set-Reset Latch}

\section*{General Description}

This device contains four independent set-reset type flipflops with one Q output each.

\section*{Connection Diagram}


TL/F/9785-1
Order Number 54279DMQB, 54279FMQB or DM74279N NS Package Number J16A, N16E or W16A
\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{c|}{ Description } \\
\hline\(R_{n}\) & Reset Inputs (Active Low) \\
\(S_{n}\) & Set Inputs (Active Low) \\
\(Q\) & Outputs \\
\hline
\end{tabular}

Truth Table
\begin{tabular}{|ccc|c|}
\hline & \begin{tabular}{c} 
Inputs \\
\(\overline{\mathbf{S}} \mathbf{1}\)
\end{tabular} & \(\overline{\mathbf{R}}\) & \begin{tabular}{c} 
Output \\
Q
\end{tabular} \\
\hline L & L & L & h \\
L & X & H & H \\
X & L & H & H \\
H & H & L & L \\
H & H & H & No Change \\
\hline
\end{tabular}
\(H=H I G H\) Voltage Level
L = LOW Voltage Level
\(X=\) Immaterial
\(h=\) The output is HIGH as long as \(\overline{\mathrm{S}} 1\) or \(\overline{\mathrm{S}} 2\) is LOW. If all inputs go HIGH simultaneously, the output state is indeterminate; otherwise, it follows the Truth Table.
Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
Operating Free Air Temperature Range
\begin{tabular}{lr}
54 & \\
DM74 & \\
Storage Temperature Range & \(55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
& \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
& \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{54279} & \multicolumn{3}{|c|}{DM74279} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline loL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics}
over Recommended Operating Free Air Temperature Range (Unless Otherwise Noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|r|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) }
\end{gathered}
\] & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=M i n, I_{\mathrm{OH}}=M a x, \\
& V_{\mathrm{IL}}=M a x
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\mathrm{Max}, \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Max} \\
& (\text { Note 2) }
\end{aligned}
\]} & 54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -57 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \overline{\mathrm{R}}=0 \mathrm{~V}\)} & & & 30 & mA \\
\hline
\end{tabular}

\section*{Switching Characteristics}
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{54/DM74} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \[
t_{P L H}
\]
\[
\mathrm{t}_{\mathrm{PHL}}
\] & Propagation Delay \(\bar{S}\) to \(Q\) & & \[
\begin{aligned}
& 22 \\
& 15 \\
& \hline
\end{aligned}
\] & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay \(\overline{\mathrm{R}}\) to \(Q\) & & 27 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, T_{A}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{54283/DM74283}

\section*{4-Bit Binary Full Adder (with Fast Carry)}

\section*{General Description}

The '283 high speed 4-bit binary full adders with internal carry lookahead accept two 4-bit binary words (AO-A3, B0B3) and a Carry input (C0). They generate the binary Sum outputs (SO-S3) and the Carry output (C4) from the most significant bit. They operate with either active HIGH or active LOW operands (positive or negative logic).

\section*{Connection Diagram}


Order Number 54283DMQB, 54283FMQB or DM74283N See NS Package Number J16A, N16E or W16A
\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
\hline A0-A3 & A Operand Inputs \\
BO-B3 & B Operand Inputs \\
C0 & Carry Input \\
S0-S3 & Sum Outputs \\
C4 & Carry Output \\
\hline
\end{tabular}
\begin{tabular}{lr} 
Absolute Maximum Ratings (Note) \\
If Milltary/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage & 7 V \\
Input Voltage & \(5.5^{2}\) \\
Operating Free Air Temperature Range \\
54 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{54283} & \multicolumn{3}{|c|}{DM74283} & \multirow{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{1 H}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \({ }^{\mathrm{OH}}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics}

Over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|r|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Min}, \mathrm{l}_{\mathrm{l}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline \(1 / 1\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current at \(\mathrm{S}_{\mathrm{n}}\)} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{\mathrm{CC}}=M a x \\
& (\text { Note 2) }
\end{aligned}
\]} & 54 & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -20 & & -55 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current at C4} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& (\text { Note 2) }
\end{aligned}
\]} & 54 & -20 & & -70 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -18 & & -70 & \\
\hline \multirow[t]{2}{*}{ICCH} & \multirow[t]{2}{*}{Supply Current with Outputs High} & \multirow[t]{2}{*}{\(V_{C C}=M a x\)} & 54 & & & 99 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & & & 110 & \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{Switching Characteristics}
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=400 \Omega\)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}}
\end{aligned}
\] & Propagation Delay CO or \(\mathrm{S}_{\mathrm{n}}\) & & \[
\begin{aligned}
& 21 \\
& 21 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay \(A_{n}\) or \(B_{n}\) to \(S_{n}\) & & \[
\begin{aligned}
& 24 \\
& 24
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}}
\end{aligned}
\] & Propagation Delay C0 to C4 & & \[
\begin{aligned}
& 14 \\
& 16 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}}
\end{aligned}
\] & Propagation Delay \(A_{n}\) or \(B_{n}\) to \(C 4\) & & \[
\begin{aligned}
& 14 \\
& 16 \\
& \hline
\end{aligned}
\] & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The '283 adds two 4-bit binary words (A plus B) plus the incoming carry CO . The binary sum appears on the Sum (S0-S3) and outgoing carry (C4 outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.
\[
\begin{aligned}
& 2^{0}(A 0+B 0+C 0)+2^{1}(A 1+B 1)+2^{2}(A 2+B 2)+ \\
& 2^{3}(A 3+B 3)=S 0+2 S 1+4 S 2+8 S 3+16 C 4 \\
& \text { Where }(+)=\text { plus }
\end{aligned}
\]

Interchanging inputs of equal weight does not affect the operation. Thus CO, AO, BO can be arbitrarily assigned to pins 5,6 and 7 . Due to the symmetry of the binary add function, the '283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that if CO is not used it must be tied LOW for active HIGH logic or tied HIGH for active LOW logic.

\section*{Example:}
\begin{tabular}{|l|l|l|l|l|}
\hline C0 & A0 A1 A2 A3 & B0 B1 B2 B3 & S0 S1 S2 S3 & C4 \\
\hline
\end{tabular}
\begin{tabular}{|l|l|llll|llll|lll|l|}
\hline Logic Levels & L & L & \(H\) & L & H & \(H\) & L & L & \(H\) & \(H\) & \(H\) & \(L\) & \(L\) \\
\(H\) \\
\hline Active HIGH & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 1 & 0 & 0 \\
1 \\
Active LOW & 1 & 1 & 0 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 1
\end{tabular} 0.

Active HIGH: \(0+10+9=3+16\) Active LOW: \(1+5+6=12+0\)


TL/F/9786-3
FIGURE a. 3-Bit Adder

Due to pin limitations, the intermediate carries of the '283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. Figure a shows a way of making a 3-bit adder. Tying the operand inputs of the fourth adder (A3, B3) LOW makes S3 dependent ony on, and equal to, the carry from the third adder. Using somewhat the same principle,Figure \(b\) shows a way of dividing the '283 into a 2-bit and a 1-bit adder. The third stage adder (A2, B2, S2) is used merely as a means of getting a carry (C10) signal into the fourth stage (via A2 and B 2 ) and bringing out the carry from the second stage on S2. Note that as long as A2 and B2 are the same, whether HIGH or LOW, they do not infuence S2. Similarly, when A2 and B2 are the same the carry into the third stage does not influence they carry out of the third stage. Figure \(c\) shows a method of implementing a 5 -input encoder, where the inputs are equally weighted. The outputs \(\mathrm{S} 0, \mathrm{~S} 1\) and S 2 present a binary number equal to the number of inputs \(11-15\) that are true. Figure \(d\) shows one method of implementing a 5 -input majority gate. When three or more of the inputs \(11-15\) are true, the output M5 is true.


TL/F/9786-4
FIGURE b. 2-Bit and 1-Bit Adders

Functional Description (Continued)


TL/F/9786-5
FIGURE c. 5-Input Encoder


TL/F/9786-6
FIGURE d. 5-Input Majority Gate

\section*{Logic Symbol}


TL/F/9786-2

\section*{Logic Diagram}


TL/F/9786-7

\section*{54298}

\section*{Quad 2-Port Register (Multiplexer With Storage)}

\section*{General Description}

The '298 is a quad 2-port register. It is the logical equivalent of a quad 2 -input multiplexer followed by a quad 4-bit edgetriggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register synchronous with the HIGH-to-LOW transition of the Clock input.

\section*{Features}
- Select from two data sources
- Fully edge-triggered operation

\section*{Connection Diagram}


TL/F/10215-1
Order Number 54298DMQB or 54298FMQB See NS Package Number J16A or W16A

\section*{Logic Symbol}


TL/F/10215-2
\(V_{C C}=P i n 16\)
GND \(=\operatorname{Pin} 8\)
\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
\hline S & Common Select Input \\
\(\overline{\mathrm{CP}}\) & Clock Pulse Input (Active Falling Edge) \\
10a-10d & Source 0 Data Inputs \\
11a-I1d & Source 1 Data Inputs \\
Qa, Qd & Flip-Flop Outputs \\
\hline
\end{tabular}
Absolute Maximum Ratings (Note)
If Milltary/Aerospace speclfied devices are required,
please contact the National Semiconductor Sales
Office/Distributors for availability and specifications.
\begin{tabular}{l} 
Supply Voltage \\
Input Voltage
\end{tabular}
\begin{tabular}{lr} 
Operating Free Air Temperature & 7 V \\
Range & \\
Storage Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
R & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{54298} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & \\
\hline \(V_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.8 & mA \\
\hline lOL & Low Level Output Current & & & 16 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
& \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
& \hline
\end{aligned}
\] & Setup Time HIGH or LOW \(S\) to \(\overline{\mathrm{CP}}\) & \[
\begin{array}{r}
25 \\
25 \\
\hline
\end{array}
\] & & & ns \\
\hline \[
\begin{aligned}
& t_{h}(H) \\
& t_{h}(L)
\end{aligned}
\] & Hold Time HIGH or LOW \(S\) to \(\overline{\mathrm{CP}}\) & \[
\begin{aligned}
& 0 \\
& 0
\end{aligned}
\] & & & ns \\
\hline \[
\begin{aligned}
& t_{s}(H) \\
& t_{s}(L) \\
& \hline
\end{aligned}
\] & Setup Time HIGH or LOW \(\mathrm{I}_{0 \times}\) or \(\mathrm{I}_{1 \mathrm{x}}\) to \(\overline{\mathrm{CP}}\) & \[
\begin{array}{r}
15 \\
15 \\
\hline
\end{array}
\] & & & ns \\
\hline \[
\begin{aligned}
& t_{h}(H) \\
& t_{h}(L) \\
& \hline
\end{aligned}
\] & Hold Time HIGH or LOW \(\mathrm{I}_{0 \times}\) or \(\mathrm{I}_{1 \mathrm{x}}\) to \(\overline{\mathrm{CP}}\) & \[
\begin{aligned}
& 5.0 \\
& 5.0 \\
& \hline
\end{aligned}
\] & & & ns \\
\hline \[
\begin{aligned}
& t_{w}(H) \\
& t_{w}(L) \\
& \hline
\end{aligned}
\] & \(\overline{\text { CP }}\) Pulse Width HIGH or LOW & \[
\begin{aligned}
& 20 \\
& 20
\end{aligned}
\] & & & ns \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ
(Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\] & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \({ }_{1 / 1}\) & High Level Input Current & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline los & Short Circuit Output Current & \[
\begin{aligned}
& V_{C C}=\text { Max } \\
& (\text { Note 2) }
\end{aligned}
\] & -20 & & -57 & mA \\
\hline ICC & Supply Current & \(V_{C C}=\operatorname{Max}\) (Note 3) & & & 65 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: ICC is measured with all outputs open and all inputs grounded.

Switching Characteristics \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for test waveforms and output load)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\[
\begin{aligned}
& C_{L}=15 \mathrm{pF} \\
& \mathrm{R}_{\mathrm{L}}=400 \Omega
\end{aligned}
\]} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \begin{tabular}{l}
\({ }^{\text {tpLH }}\) \\
tpHL
\end{tabular} & Propagation Delay, \(\overline{\mathrm{CP}}\) to \(\mathrm{Q}_{\mathrm{n}}\) & & \[
\begin{aligned}
& 27 \\
& 32 \\
& \hline
\end{aligned}
\] & ns \\
\hline
\end{tabular}

\section*{Functional Description}

This device is a high speed quad 2-port register. It selects four bits of data from two sources (ports) under the control of a Common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the Clock input ( \(\overline{\mathrm{CP}}\) ). The 4-bit output register is fully edge-triggered. The Data inputs ( \(\mathrm{I}_{\mathrm{nx}}\) ) and Select input (S) need be stable only one setup time prior to the HIGH-to-LOW transition of the clock for predictable operation.

\section*{Truth Table}
\begin{tabular}{|ccc|c|}
\hline \multicolumn{3}{|c|}{ Inputs } & Output \\
\hline \(\mathbf{S}\) & \(\mathbf{I}_{\mathbf{0 x}}\) & \(\mathbf{I}_{\mathbf{1 x}}\) & \(\mathbf{Q}_{\mathbf{x}}\) \\
\hline I & I & X & L \\
I & h & X & H \\
h & X & I & L \\
h & X & h & H \\
\hline
\end{tabular}
\[
\begin{aligned}
I= & \text { LOW Voltage Level one setup time prior to the HIGH-to-LOWclock } \\
& \text { transition. } \\
h= & \text { HIGH Voltage Level one setup time prior to the HIGH-to-LOW clock } \\
& \text { transition. } \\
H= & \text { HIGH Voltage level } \\
L= & \text { LOW Voltage level } \\
X= & \text { Immaterial }
\end{aligned}
\]

\section*{Logic Diagram}


\section*{DM54365 Hex TRI-STATE® Buffers}

\section*{General Description}

This device contains six independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard TTL output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the
output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

\section*{Connection Diagram}


TL/F/6570-1
Order Number DM54365J or DM54365W
See NS Package Number J16A or W16A

\section*{Function Table}
\begin{tabular}{|c|c|c|c|}
\hline \multicolumn{3}{|c|}{Input} & Output \\
\hline \(\overline{\mathbf{G} 1}\) & \(\overline{\mathrm{G}} 2\) & A & Y \\
\hline L & L & L & L \\
\hline L & L & H & H \\
\hline H & X & X & \(\mathrm{Hi}-\mathrm{Z}\) \\
\hline X & H & X & \(\mathrm{Hi}-\mathrm{Z}\) \\
\hline
\end{tabular}

\footnotetext{
\(H=\) High Logic Level
L = Low Logic Level
\(X=\) Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)
}
\begin{tabular}{|c|c|c|}
\hline \multicolumn{3}{|l|}{Absolute Maximum Ratings (Note)} \\
\hline If Milltary/Aerospace specifle please contact the Nationa Office/Distributors for availab & ces are required, conductor Sales specifications. & \multirow[t]{2}{*}{beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics"} \\
\hline Supply Voltage & 7 V & \\
\hline Input Voltage & 5.5 V & table are not guaranteed at the absolute maximum ratings. \\
\hline Operating Free Air Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) & the conditions for actual device operation. \\
\hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) & \\
\hline
\end{tabular}

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multirow{2}{|c|}{ Parameter } & \multicolumn{2}{c|}{ DM54365 } & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -2 & mA \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 32 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min &  & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.1 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min}, l_{O L}=\operatorname{Max} \\
& V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline \multirow[t]{3}{*}{ILL} & \multirow[t]{3}{*}{Low Level Input Current} & \[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=0.5 \mathrm{~V}(\text { Note } 4)
\end{aligned}
\] & A & & & -40 & \multirow{3}{*}{mA} \\
\hline & & \[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=0.4 V \text { (Note 5) }
\end{aligned}
\] & A & & & -1.6 & \\
\hline & & \[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=0.4 V
\end{aligned}
\] & \(\overline{\mathrm{G}}\) & & & -1.6 & \\
\hline lozh & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & 40 & \(\mu \mathrm{A}\) \\
\hline Iozl & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Max}, V_{O}=0.4 V \\
& V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
\end{aligned}
\]} & & & -40 & \(\mu \mathrm{A}\) \\
\hline los & Short Circuit Output Current & \(\mathrm{V}_{\text {CC }}=\mathrm{Max}\) (Note 2) & & -40 & & -115 & mA \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}\) (Note 3)} & & 59 & 85 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: IcC is measured with the data inputs grounded, and the output controls at 4.5 V .
Note 4: Both \(\bar{G}\) inputs are at 2 V .
Note 5: Both \(\overline{\mathcal{G}}\) inputs are at 0.4 V .

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega\)} & \multirow{3}{*}{Units} \\
\hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(C_{L}=50 \mathrm{pF}\)} & \\
\hline & & Min & Max & Min & Max & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & & & & 16 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & & & & 22 & ns \\
\hline \(t_{\text {PZH }}\) & Output Enable Time to High Level Output & & & & 35 & ns \\
\hline \(t_{P Z L}\) & Output Enable Time to Low Level Output & & & & 37 & ns \\
\hline \(t_{\text {PHZ }}\) & Output Disable Time from High Level Output & & 11 & & & ns \\
\hline \(t_{\text {PLZ }}\) & Output Disable Time from Low Level Output & & 27 & & & ns \\
\hline
\end{tabular}

\section*{General Description}

This device contains six independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard TTL output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the
output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a signficant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

\section*{Connection Diagram}

\section*{Dual-In-Line Package}


TL/F/6572-1
Order Number DM54367J or DM54367W See NS Package Number J16A or W16A

\section*{Function Table}
\begin{tabular}{|c|c|c|}
\hline \multicolumn{2}{|c|}{ Input } & Output \\
\hline\(\overline{\mathbf{G}}\) & \(\mathbf{A}\) & \(\mathbf{Y}\) \\
\hline L & L & L \\
L & H & H \\
H & X & \(\mathrm{Hi}-Z\) \\
\hline
\end{tabular}
\(H=\) High Logic Level
L = Low Logic Level
\(X=\) Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{l|l|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multicolumn{2}{|c|}{ Parameter } & \multicolumn{2}{|c|}{ DM54367 } & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -2 & mA \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 32 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) } \\
\hline
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M i n, l_{l}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=M i n, I_{O H}=\operatorname{Max} \\
& V_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.1 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline \multirow[t]{3}{*}{ILL} & \multirow[t]{3}{*}{Low Level Input Current} & \[
\begin{aligned}
& V_{C C}=\operatorname{Max} \\
& V_{1}=0.5 \mathrm{~V} \text { (Note 4) }
\end{aligned}
\] & A & & & -40 & \multirow{3}{*}{mA} \\
\hline & & \[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=0.4 \mathrm{~V}(\text { Note } 5)
\end{aligned}
\] & A & & & -1.6 & \\
\hline & & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{I}}=0.4 \mathrm{~V} \\
& \hline
\end{aligned}
\] & \(\overline{\mathrm{G}}\) & & & -1.6 & \\
\hline lozh & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & 40 & \(\mu \mathrm{A}\) \\
\hline lozl & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{O}^{\prime}}=0.4 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & -40 & \(\mu \mathrm{A}\) \\
\hline los & Short Circuit Output Current & \(\mathrm{V}_{\text {CC }}=\operatorname{Max}\) (Note 2) & & -40 & & -115 & mA \\
\hline Icc & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\) Max (Note 3)} & & 65 & 85 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: ICC is measured with the data inputs grounded and the output controls at 4.5 V .
Note 4: Both \(\overline{\mathrm{G}}\) inputs are at 2 V .
Note 5: Both \(\overline{\mathrm{G}}\) inputs are at 0.4 V .

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega\)} & \multirow{3}{*}{Units} \\
\hline & & \multicolumn{2}{|c|}{\(C_{L}=5 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
\hline & & Min & Max & Min & Max & \\
\hline tpLH & Propagation Delay Time Low to High Level Output & & & & 16 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & & & & 22 & ns \\
\hline tpzH & Output Enable Time to High Level Output & & & & 35 & ns \\
\hline tpzL & Output Enable Time to Low Level Output & & & & 37 & ns \\
\hline tphz & Output Disable Time from High Level Output & & 11 & & & ns \\
\hline tplz & Output Disable Time from Low Level Output & & 27 & & & ns \\
\hline
\end{tabular}

\section*{DM54368 Hex TRI-STATE® Inverting Buffers}

\section*{General Description}

This device contains six independent gates each of which performs an inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard TTL output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the
output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Connection Diagram

Dual-In-Line Package


TL/F/6573-1
Order Number DM54368J or DM54368W See NS Package Number J16A or W16A

Function Table
\begin{tabular}{|c|c|c|}
\hline \multicolumn{3}{|c|}{\(Y=\overline{\mathbf{A}}\)} \\
\hline \multicolumn{2}{|c|}{ Inputs } & Output \\
\hline\(\overline{\mathbf{G}}\) & \(\mathbf{A}\) & \(\mathbf{Y}\) \\
\hline\(L\) & L & H \\
L & H & L \\
\(H\) & X & \(\mathrm{Hi}-\mathrm{Z}\) \\
\hline
\end{tabular}

H = High Logic Level
L = Low Logic Level
\(X=\) Either Low or High Logic Level
\(\mathrm{Hi}-\mathrm{Z}=\) TRI-STATE (Outputs are disabled)
\begin{tabular}{l} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
\begin{tabular}{l} 
Supply Voltage \\
Input Voltage \\
Operating Free Air Temperature \\
Range \\
Storage Temperature Range \\
R \\
R
\end{tabular}\(\quad-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{c|c|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multicolumn{2}{|c|}{ Parameter } & \multicolumn{2}{|c|}{ DM54368 } & \multirow{2}{*}{ Units } \\
\cline { 3 - 5 } & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -2 & mA \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 32 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characterisťics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ
(Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.1 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \[
\begin{aligned}
& V_{C C}=M a x \\
& \left.V_{1}=0.5 \mathrm{~V} \text { (Note } 4\right)
\end{aligned}
\] & A & & & -40 & \multirow{3}{*}{mA} \\
\hline & & \[
\begin{aligned}
& V_{\mathrm{CC}}=M a x \\
& V_{1}=0.4 \mathrm{~V}(\text { Note } 5)
\end{aligned}
\] & A & & & -1.6 & \\
\hline & & \[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=0.4 V
\end{aligned}
\] & \(\overline{\mathrm{G}}\) & & & -1.6 & \\
\hline lozh & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Max}, V_{O}=2.4 V \\
& V_{\mathrm{IH}}=\operatorname{Min}, V_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & 40 & \(\mu \mathrm{A}\) \\
\hline lozl & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Max}, V_{O}=0.4 V \\
& V_{\mathrm{IH}}=\operatorname{Min}, V_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & -40 & \(\mu \mathrm{A}\) \\
\hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\) (Note 2)} & -40 & & \(-115\) & mA \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\) (Note 3)} & & 59 & 77 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: ICC is measured with the data inputs grounded, and the output controls at 4.5 V .
Note 4: Both \(\overline{\mathrm{G}}\) inputs are at 2V.
Note 5: Both \(\overline{\mathrm{G}}\) inputs are at 0.4 V .
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega\)} & \multirow{3}{*}{Units} \\
\hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
\hline & & Min & Max & Min & Max & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & & & & 17 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & & & & 16 & ns \\
\hline \(t_{\text {tPZ }}\) & Output Enable Time to High Level Output & & & & 35 & ns \\
\hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level Output & & & & 37 & ns \\
\hline \(t_{\text {PHZ }}\) & Output Disable Time from High Level Output & & 11 & & & ns \\
\hline \(t_{\text {PLL }}\) & Output Disable Time from Low Level Output & & 27 & & & ns \\
\hline
\end{tabular}

\section*{DM7123 Quad 2-Input}

\section*{Data Selectors/Multiplexers}

\section*{General Description}

This device contains four 2-input multiplexers with common input select logic and common output disable circuitry. The DM7123 provides TRI-STATE \({ }^{\circledR}\) outputs. When the enable/ strobe input is at a low logic level, the outputs of all devices are conventional TTL. However, when the enable/strobe input is raised to a high logic level, the outputs of the DM7123 go to the high-impedance third state. This device provides the designer with TRI-STATE and/or low power pin/pin replacements for the popular DM9322 and DM54/DM74157 multiplexers.

\section*{Features}

■ Pin equivalents popular DM9322 and DM54/DM74157 multiplexers
- Both conventional TTL and TRI-STATE outputs available
- Typical propagation delay 9.5 ns
- Typical power dissipation 200 mW

\section*{Connection Diagram}


TL/F/6574-1
Order Number DM7123J or DM7123W
See NS Package Number J16A or W16A

Function Table
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow{2}{*}{ Enable } & \multirow{2}{*}{ Select } & \multicolumn{2}{|c|}{ Inputs } & \multirow{2}{*}{\begin{tabular}{c} 
Outputs \\
\cline { 3 - 4 } \\
\end{tabular}} \\
& A & B & Y \\
\hline L & L & L & X & L \\
L & L & H & X & H \\
L & H & X & L & L \\
L & H & X & H & H \\
H & X & X & X & Hi-Z \\
\hline
\end{tabular}

\footnotetext{
L = Low Logic Level, \(H=\) High Logic Level
\(X=\) Either Low or High Logic Level
\(\mathrm{Hi}-\mathrm{Z}=\) TRI-STATE (Outputs are disabled)
}
Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for availability and specifications.
\begin{tabular}{lr} 
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM71 & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular} Storage Temperature Range

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multirow{2}{*}{ Parameter } & \multicolumn{2}{|c|}{ DM7123 } & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & Nom & Max & \\
\hline\(V_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline \(\mathrm{IOH}_{\mathrm{OH}}\) & High Level Output Current & & & -2 & mA \\
\hline \(\mathrm{IOL}_{\mathrm{OL}}\) & Low Level Output Current & & & 16 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) }
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\] & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline lozh & Off-State Output Current with High Level Output Voltage Applied & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{O}}=2.4 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\] & & & 40 & \(\mu \mathrm{A}\) \\
\hline lozL & Off-State Output Current with Low Level Output Voltage Applied & \[
\begin{aligned}
& V_{C C}=\operatorname{Max}, V_{\mathrm{O}}=0.4 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\] & & & -40 & \(\mu \mathrm{A}\) \\
\hline los & Short Circuit Output Current & \[
\begin{aligned}
& V_{\mathrm{CC}}=\text { Max } \\
& \text { (Note 2) } \\
& \hline
\end{aligned}
\] & -30 & & -70 & mA \\
\hline ICC & Supply Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 3) & & 40 & 51 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: ICC is measured with the inputs grounded, and all outputs open.

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega\)} & \multirow{3}{*}{Units} \\
\hline & & & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
\hline & & & Min & Max & Min & Max & \\
\hline \(t_{\text {PLL }}\) & Propagation Delay Time Low to High Level Output & Data to Output & & & 4 & 15 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to Output & & & 5 & 18 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Select to Output & & & 5 & 23 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Select to Output & & & 8 & 24 & ns \\
\hline \(t_{\text {PZH }}\) & Output Enable Time to High Level Output & Enable to Q & & & 9 & 25 & ns \\
\hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level Output & Enable to Q & & & 10 & 30 & ns \\
\hline \({ }_{\text {tPHZ }}\) & Output Disable Time from High Level Output & Enable to Q & 4 & 11 & & & ns \\
\hline \(t_{\text {PLZ }}\) & Output Disable Time from Low Level Output & Enable to Q & 9 & 27 & & & ns \\
\hline
\end{tabular}

Logic Diagram


TL/F/6574-2

\section*{DM7130 Magnitude Comparators}

\section*{General Description}

This device offers comparisons to determine equality between two binary words. The DM7130 compares two ten-bit words. A strobe override is provided. When the strobe is taken to a high logic level, the output is forced to a high logic level. The device also features open collector outputs for expansion.

\section*{Features}
- Typical propagation delay 21 ns
- Typical power dissipation 240 mW
- Open-collector outputs for expansion

\section*{Connection Diagram}

\section*{Dual-In-Line Package}


\section*{Function Table}
\begin{tabular}{|c|c|c|}
\hline Condition & \begin{tabular}{c} 
STROBE \\
\(\mathbf{S}\)
\end{tabular} & \begin{tabular}{c} 
Output \\
\(\mathbf{Y}\)
\end{tabular} \\
\hline\(A=B, A \neq B\) & \(H\) & \(H\) \\
\(A=B\) & \(L\) & \(H\) \\
\(A \neq B\) & \(L\) & \(L\) \\
\hline
\end{tabular}

H = High Logic Level
L = Low Logic Level
```

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
7 V
Input Voltage
5.5 V
Operating Free Air Temperature Range
DM71
Storage Temperature Range

```

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multicolumn{2}{|c|}{ Parameter } & \multicolumn{2}{|c|}{ DM7130 } & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline \(\mathrm{~V}_{\mathrm{OH}}\) & High Level Output Voltage & & & 5.5 & V \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 16 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) }
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(V_{C C}=M i n, l_{I}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline ICEX & High Level Output Current & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{O}}=5.5 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\] & & & 100 & \(\mu \mathrm{A}\) \\
\hline V OL & Low Level Output Voltage & \[
\begin{aligned}
& V_{C C}=M i n, I_{O L}=\operatorname{Max} \\
& V_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\] & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline 1 IH & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline ILL & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline ICC & Supply Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 2) & & 48 & 70 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & Data to Output & & 25 & ns \\
\hline tPHL & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
Data to \\
Output
\end{tabular} & & 40 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Strobe to Output & & 18 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Strobe to Output & & 30 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: ICC is measured with all inputs grounded and all outputs open.

\section*{DM7136 6-Bit Unified Bus Comparator with Open-Collector Outputs}

\section*{General Description}

The DM7136 compares two binary words of two-to-six bits in length and indicates matching (bit-for-bit) of the two words. Inputs for one word are 54/74 series-compatible TTL inputs, whereas those of the second word are high-impedance receivers driven by a terminated data bus. These bus inputs include 0.65 V typical hysteresis which provides 1.4 V noise immunity. The DM7136 has open-collector outputs which go to the high state upon equality and is expandable to \(n\) bits by collector-ORing. The device has an output latch which is strobe controlled.
The transfer of information to the output occurs when the STROBE input goes from a logic " 1 " to a logic " 0 " state. Inputs may be changed while the \(\overline{\text { STROBE }}\) is at the logic " 1 " level, without affecting the state of the output. These devices are useful as address comparators in computer systems utilizing unified data bus organization.

\section*{Features}

■ Low bus input current \(15 \mu \mathrm{~A}\) typ
- High bus input noise immunity 1.4 V typ
- Bus inputs comply with IEEE 488-1975
- TTL-compatible output
- Output latch provision

\section*{Connection Diagram}

Dual-In-Line Package

(BUS INPUT) (TTL INPUT)
TL/F/6577-1
Order Number DM7136J or DM7136W See NS Package Number J16A or W16A

Function Table
\begin{tabular}{|c|c|c|}
\hline \multirow{2}{*}{ Condition } & STROBE & Output \\
\cline { 3 - 3 } & & DM71/8136 \\
\hline \(\mathrm{T}=\mathrm{B}, \mathrm{T} \neq \mathrm{B}\) & H & \(\mathrm{Q}_{\mathrm{N}-1^{*}}\) \\
\(\mathrm{~T}=\mathrm{B}\) & L & \(H\) \\
\(\mathrm{~T} \neq \mathrm{B}\) & L & L \\
\hline
\end{tabular}
*Latched in previous state.
\(H=\) High Logic Level
L = Low Logic Level
\begin{tabular}{|c|c|}
\hline \multicolumn{2}{|l|}{Absolute Maximum Ratings (Note)} \\
\hline If Military/Aerospace specified dev please contact the National Sem Office/Distributors for availability and & ces are required, conductor Sales specifications. \\
\hline Supply Voltage & 7 V \\
\hline Input Voltage & 5.5 V \\
\hline Operating Free Air Temperature Range & \\
\hline DM71 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
\hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multicolumn{1}{|c|}{ Parameter } & \multicolumn{3}{|c|}{ DM7136 } & \multirow{2}{*}{ Units } \\
\cline { 3 - 5 } & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{~V}_{\mathrm{T}+}\) & \begin{tabular}{l} 
Positive-Going Input \\
Thrieshold Voltage for \\
Bus Inputs (Note 1)
\end{tabular} & 1.4 & 1.75 & 2 & V \\
\hline \(\mathrm{~V}_{\mathrm{T}-}\) & \begin{tabular}{l} 
Negative-Going Input \\
Threshold Voltage for \\
Bus Inputs (Note 1)
\end{tabular} & 2.9 & 1.1 & 1.35 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & \begin{tabular}{l} 
High Level Input \\
Voltage for TTL \\
and Strobe Inputs
\end{tabular} & \begin{tabular}{l} 
Low Level Input \\
Voltage for TTL \\
and Strobe Inputs
\end{tabular} & & & V \\
\hline \(\mathrm{V}_{\mathrm{IL}}\) & High Level Output Voltage & & & 0.8 & V \\
\hline \(\mathrm{~V}_{\mathrm{OH}}\) & Low Level Output Current & & & 5.5 & V \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & \begin{tabular}{l} 
Free Air Operating Temperature
\end{tabular} & -55 & & 16 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
\begin{aligned}
& \text { Typ } \\
& \text { (Note 2) }
\end{aligned}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline ICEX & High Level Output Current & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min}, V_{O}=5.5 \mathrm{~V} \\
& V_{I L}=\operatorname{Max}, V_{I H}=M i n
\end{aligned}
\]} & & & 250 & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min}, \mathrm{l}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & 0.4 & V \\
\hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current @ Max Input Voltage} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=5.5 V
\end{aligned}
\]} & TTL & & & 1 & \multirow[t]{2}{*}{mA} \\
\hline & & & Strobe & & & 2 & \\
\hline \multirow[t]{2}{*}{\(\mathrm{IIH}^{\text {H}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=2.4 V
\end{aligned}
\]} & TTL & & & 40 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Strobe & & & 80 & \\
\hline \multirow[t]{2}{*}{IIL.} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=0.4 V
\end{aligned}
\]} & TTL & & & -1.6 & \multirow[t]{2}{*}{mA} \\
\hline & & & Strobe & & & -2.4 & \\
\hline \multirow[t]{2}{*}{IN} & \multirow[t]{2}{*}{Bus input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{1}=4 \mathrm{~V}\)} & \(\mathrm{V}_{C C}=\mathrm{Max}\) & & 15 & 50 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & \(\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V}\) & & 1 & 50 & \\
\hline Icc & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}\) (Note 3)} & & 50 & 74 & mA \\
\hline
\end{tabular}

Note 1: \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
Note 2: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 3: ICC is measured with all inputs grounded and all outputs open.

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{\begin{tabular}{l}
From (Input) \\
To (Output)
\end{tabular}} & \multicolumn{2}{|c|}{\[
\begin{aligned}
& \mathrm{R}_{\mathrm{L}}=400 \Omega \\
& \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}
\end{aligned}
\]} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & TTL to Output & & 30 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & TTL to Output & & 30 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Bus to Output & & 45 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Bus to Output & & 45 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Strobe to Output & & 30 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Strobe to Output & & 30 & ns \\
\hline
\end{tabular}

\section*{Logic Diagram}


TL/F/6577-2

National

\section*{DM7160 Magnitude Comparator}

\section*{General Description}

This device offers comparisons to determine equality between two binary words. The DM7160 compares two six-bit words. A strobe override is provided. When the strobe is taken to a high logic level, the output is forced to a high logic level. The device also features open-collector outputs for expansion.

\section*{Features}
- Typical propagation delay 21 ns
- Typical power dissipation 205 mW
- Open-collector outputs for expansion

\section*{Connection Diagram}


Function Table
\begin{tabular}{|c|c|c|}
\hline Condition & \begin{tabular}{c} 
STROBE \\
S
\end{tabular} & \begin{tabular}{c} 
Output \\
\(\mathbf{Y}\)
\end{tabular} \\
\hline\(A=B, A \neq B\) & \(H\) & \(H\) \\
\(A=B\) & \(L\) & \(H\) \\
\(A \neq B\) & \(L\) & \(L\) \\
\hline
\end{tabular}

\footnotetext{
\(H=\) High Logic Level
L = Low Logic Level
}
\begin{tabular}{lr} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
\begin{tabular}{lr} 
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM71 & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular} Storage Temperature Range &
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{l|l|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multirow{2}{|c|}{ Darameter } & \multicolumn{2}{c|}{ DM160 } & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline \(\mathrm{~V}_{\mathrm{OH}}\) & High Level Output Voltage & & & 5.5 & V \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 16 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & \begin{tabular}{l}
Typ \\
(Note 1)
\end{tabular} & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline ICEX & High Level Output Current & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{O}}=5.5 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & & & 100 & \(\mu \mathrm{A}\) \\
\hline VOL & Low Level Output Voltage & \[
\begin{aligned}
& V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\
& V_{I H}=\operatorname{Min}
\end{aligned}
\] & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{IH}^{\text {H }}\) & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline ILL & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline ICC & Supply Current & \(\mathrm{V}_{\mathrm{CC}}=\operatorname{Max}\) (Note 2) & & 41 & 60 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \({ }_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output & Data to Output & & 25 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to Output & & 40 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Strobe to Output & & 18 & ns \\
\hline tpHL & Propagation Delay Time High to Low Level Output & Strobe to Output & & 30 & ns \\
\hline
\end{tabular}

\footnotetext{
Note 1: All typicals are at \(V_{C C}=5 V, T_{A}=25^{\circ} \mathrm{C}\).
Note 2: \(\mathrm{I}_{\mathrm{CC}}\) is measured with all inputs grounded and all outputs open.
}

\section*{\(\cdots\) National Semiconductor \\ 9300/DM9300 4-Bit Parallel-Access Shift Register}

\section*{General Description}

The 9300 4-bit registers feature parallel inputs, parallel outputs, \(\sqrt{\bar{K}}\) serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation: parallel (broadside) load and shift (in direction \(Q_{A}\) toward \(\left.Q_{D}\right)\).
Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flops, and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.
Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the \(J \bar{K}\) inputs. These inputs permit the first stage to perform as a \(\sqrt{\mathrm{K}}, \mathrm{D}\) or T -type flip-flop as shown in the function table.

These shift registers are fully compatible with most other TTL and DTL families. All inputs, including the clock, are buffered to lower the drive requirements to one normalized Series 54/74 load.

\section*{Features}
© Fully buffered inputs
- Direct overriding clear
- Synchronous parallel load
- Parallel inputs and outputs from each flip-flop
m Positive edge-triggered clocking
- \(J\) and \(\bar{K}\) inputs to first stage
- Typical shift frequency- 39 MHz

\section*{Connection Diagram}

Dual-In-Line Package


Order Number 9300DMQB, 9300FMQB or DM9300N See NS Package Number J16A, N16E or W16A

\section*{Function Table}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{9}{|c|}{Inputs} & \multicolumn{5}{|c|}{Outputs} \\
\hline \multirow[t]{2}{*}{Clear} & \multirow[t]{2}{*}{Shift/ Load} & \multirow[t]{2}{*}{Clock} & \multicolumn{2}{|r|}{Serial} & \multicolumn{4}{|c|}{Parallel} & \multirow[t]{2}{*}{\(\mathbf{Q}_{\mathbf{A}}\)} & \multirow[t]{2}{*}{\(Q_{B}\)} & \multirow[t]{2}{*}{\(Q_{C}\)} & \multirow[t]{2}{*}{\(Q_{D}\)} & \multirow[t]{2}{*}{\(\overline{\mathbf{Q}}_{\mathbf{D}}\)} \\
\hline & & & \(J\) & \(\overline{\mathbf{K}}\) & PO & P1 & P2 & P3 & & & & & \\
\hline L & X & X & X & X & X & X & X & X & L & L & L & L & H \\
\hline H & L & \(\uparrow\) & X & X & a & b & c & d & a & b & c & d & \(\bar{d}\) \\
\hline H & H & L & X & X & X & X & X & X & \(Q_{A 0}\) & \(\mathrm{Q}_{\mathrm{B0}}\) & \(Q_{C 0}\) & \(Q_{\text {Do }}\) & \(\bar{Q}_{\text {D0 }}\) \\
\hline H & H & \(\uparrow\) & L & H & X & X & X & X & \(Q_{A 0}\) & \(Q_{\text {AO }}\) & \(\mathrm{Q}_{\mathrm{Bn}}\) & \(Q_{C n}\) & \(\bar{Q}_{\text {Q }}\) \\
\hline H & H & \(\uparrow\) & L & L & X & X & X & X & L & \(Q_{\text {An }}\) & \(Q_{B n}\) & \(Q_{C n}\) & \(\bar{Q}_{\text {Cn }}\) \\
\hline H & H & \(\uparrow\) & H & H & X & X & X & X & H & \(Q_{A n}\) & \(\mathrm{Q}_{\mathrm{Bn}}\) & \(\mathrm{Q}_{\mathrm{Cn}}\) & \(\bar{Q}_{\text {Q }} \mathrm{n}\) \\
\hline H & H & \(\uparrow\) & H & L & X & X & X & X & \(\bar{Q}_{A n}\) & \(Q_{A n}\) & \(Q_{B n}\) & \(Q_{B n}\) & \(\bar{Q}_{C n}\) \\
\hline
\end{tabular}

\footnotetext{
H \(=\) High Level (Steady State)
L = Low Level (Steady State)
\(\mathrm{X}=\) Don't Care
\(\uparrow=\) Transition from low-to-high level
\(\mathrm{a}, \mathrm{b}, \mathrm{c}, \mathrm{d},=\) The level of steady state input at P0, P1, P2, or P3 respectively.
\(Q_{A 0}, Q_{B 0}, Q_{C 0}, Q_{D 0}=\) The level of \(Q_{A}, Q_{B}, Q_{C}\), or \(Q_{D}\), respectively before the indicated steady state input conditions were established.
\(Q_{A n}, Q_{B n}, Q_{C n}=\) The level of \(Q_{A}, Q_{B}, Q_{C}\), respectively, before the most recent \(\uparrow\) transition of the clock.
}
```

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for availability and specifications.
Supply Voltage
7V
Input Voltage 5.5V
Storage Temperature Range -65'C to +150 C
Operating Free Air Temperature Range
Military }r=-5\mp@subsup{5}{}{\circ}\textrm{C}\mathrm{ to }+12\mp@subsup{5}{}{\circ}\textrm{C

```

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{IOH}^{\text {I }}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.48 & & & -0.8 & mA \\
\hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 9.6 & & & 16 & mA \\
\hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 5)} & 0 & & 30 & 0 & & 30 & MHz \\
\hline \multirow[t]{2}{*}{tw} & \multirow[t]{2}{*}{Pulse Width (Note 5)} & Clock & 17 & & & 16 & 11 & & \multirow[t]{2}{*}{ns} \\
\hline & & Clear & 25 & & & 30 & 15 & & \\
\hline \multirow[t]{3}{*}{tsu} & \multirow[t]{3}{*}{Setup Time (Note 5)} & S/L & 36 & & & 30 & 13 & & \multirow{3}{*}{ns} \\
\hline & & Data & 18 & & & 20 & 13 & & \\
\hline & & Clear & 36 & & & 30 & 13 & & \\
\hline \(t_{H}\) & \multicolumn{2}{|l|}{Data Hold Time (Note 5)} & 0 & & & 0 & -11 & & ns \\
\hline \(\mathrm{t}_{\text {REL }}\) & \multicolumn{2}{|l|}{S/L Release Time (Notes 1 and 5)} & 10 & & & 10 & & & ns \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 2) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & & & V \\
\hline VOL & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}_{\mathrm{CL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{3}{*}{IIH} & \multirow[t]{3}{*}{High Level Input Current} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=M a x, \\
& V_{I}=2.4 V
\end{aligned}
\]} & Input & & & 40 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & CP Input & & & 80 & \\
\hline & & & \(\overline{\text { PE Input }}\) & & & 92 & \\
\hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{\mathrm{I}}=0.4 \mathrm{~V}
\end{aligned}
\]} & Input & & & -1.6 & \multirow{3}{*}{mA} \\
\hline & & & CP Input & & & -3.2 & \\
\hline & & & \(\overline{\text { PE Input }}\) & & & -3.7 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& \text { (Note 3) }
\end{aligned}
\]} & MIL & -20 & & -80 & \multirow[t]{2}{*}{mA} \\
\hline & & & COM & -18 & & -55 & \\
\hline \multirow[t]{2}{*}{Icc} & \multirow[t]{2}{*}{Supply Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=\text { Max } \\
& \text { (Note 4) }
\end{aligned}
\]} & MIL & & & 86 & \multirow[t]{2}{*}{mA} \\
\hline & & & COM & & & 92 & \\
\hline
\end{tabular}

Note 1: RELEASE TIME: treLEASE is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.

Note 2: All typicais are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 3: Not more than one output should be shorted at a time.
Note 4: With all outputs open, SHIFT/LOAD grounded, and 4.5 V applied to \(\mathrm{J}, \mathrm{K}\), and data inputs, ICC is measured by applying momentary ground, then 4.5 V to CLEAR, and then to CLOCK.
Note 5: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{\begin{tabular}{l}
From (Input) \\
To (Output)
\end{tabular}} & \multicolumn{2}{|c|}{Military} & \multicolumn{2}{|c|}{Commercial} & \multirow{3}{*}{Units} \\
\hline & & & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \\
\hline & & & Min & Max & Min & Max & \\
\hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 30 & & 30 & & MHz \\
\hline \({ }^{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Output & & 20 & & 22 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Output & & 24 & & 26 & ns \\
\hline \({ }^{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Clear to Output & & 37 & & 30 & ns \\
\hline
\end{tabular}


\section*{National \\ Semiconductor}

\section*{9301/DM9301}

\section*{1-of-10 Decoders}

\section*{General Description}

These BCD-to-decimal decoders consist of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain "OFF" for all invalid input conditions.
These circuits provide familiar TTL inputs and outputs which are compatible for use with other TTL and DTL circuits. DC noise margins are typically 1 V and power dissipation is typically 125 mW . The diode-clamped, buffered inputs represent only one normalized Series 54/74 load.

\section*{Connection Diagram}


TL/F/6601-1
Order Number 9301DMQB, 9301FMQB or DM9301N See NS Package Number J16A, N16E or W16A

\section*{Features}

■ Direct replacement for Signetics 8252
- Diode-clamped inputs
- All outputs are high for invalid BCD input conditions
- Typical power dissipation 125 mW
- Typical propagation delay 20 ns


Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commerclal} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{1 \mathrm{H}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{IOH}^{\text {l }}\) & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|r|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & & & V \\
\hline VoL & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, V_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\) Max, \(\mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline \(1 / 2\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\text { Max } \\
& \text { (Note 2) }
\end{aligned}
\]} & MIL & -20 & & -70 & \multirow[t]{2}{*}{mA} \\
\hline & & & COM & -20 & & -55 & \\
\hline \multirow[t]{2}{*}{Icc} & \multirow[t]{2}{*}{Supply Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& \text { (Note 3) }
\end{aligned}
\]} & MIL & & & 44 & \multirow[t]{2}{*}{mA} \\
\hline & & & COM & & 25 & 41 & \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Conditions} & \multicolumn{2}{|c|}{Military} & \multicolumn{2}{|l|}{Commercial} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & Min & Max & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \multirow[t]{2}{*}{\[
\begin{aligned}
& C_{\mathrm{L}}=15 \mathrm{pF} \\
& \mathrm{R}_{\mathrm{L}}=400 \Omega
\end{aligned}
\]} & & 35 & & 30 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & & & 30 & & 30 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: ICC is measured with the outputs open and all inputs grounded.

\section*{Logic Diagram}


\section*{9308/DM9308 Dual 4-Bit Latch}

\section*{General Description}

The 9308 is a dual 4-bit D-type latch designed for general purpose storage applications in digital systems. Each latch contains both an active LOW Master Reset input an active LOW Enable inputs. The 74116 is a pin for pin equivalent of the 9308.

\section*{Connection Diagram}

\section*{Logic Symbol}


\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Pin} 24 \\
& \mathrm{GND}=\operatorname{Pin} 12
\end{aligned}
\]
\begin{tabular}{|c|c|}
\hline Pin Names & Description \\
\hline \[
\left.\begin{array}{l}
D_{0 a}-D_{3 a} \\
D_{0 b}-D_{3 b}
\end{array}\right\}
\] & Parallel Latch Inputs \\
\hline \(\bar{E}_{0 a}, \bar{E}_{1 a}, \bar{E}_{0 b}, \bar{E}_{1 b}\) & AND Enable Inputs (Active LOW) \\
\hline \(\overline{M R}_{a}, \overline{M R}_{b}\) & Master Reset Inputs (Active LOW) \\
\hline \[
\left.\begin{array}{l}
\bar{Q}_{0 a}-\bar{Q}_{3 a} \\
\bar{Q}_{0 b}-\bar{Q}_{3 b}
\end{array}\right\}
\] & Parallel Latch Outputs \\
\hline
\end{tabular}

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
\begin{tabular}{lr} 
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \\
MIL & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
COM & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{Milltary} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(V_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline \(\mathrm{t}_{\mathrm{s}}(\mathrm{H})\) & Setup Time HIGH, \(\mathrm{D}_{\mathrm{n}}\) to \(\bar{E}_{n}\) & 6 & & & 10 & & & ns \\
\hline \(t_{n}(H)\) & Hold Time HIGH, \(\mathrm{D}_{\mathrm{n}}\) to \(\bar{E}_{n}\) & 4 & & & -2.0 & & & ns \\
\hline \(\mathrm{t}_{\mathrm{s}}(\mathrm{L})\) & Setup Time LOW, \(\mathrm{D}_{\mathrm{n}}\) to \(\bar{E}_{\mathrm{n}}\) & 10 & & & 12 & & & ns \\
\hline \(t_{\text {h }}(L)\) & Hold Time LOW, \(\mathrm{D}_{\mathrm{n}}\) to \(\mathrm{E}_{\mathrm{n}}\) & 4 & & & 8 & & & ns \\
\hline \(t_{w}(L)\) & \(\bar{E}_{n}\) Pulse Width LOW & 18 & & & 18 & & & ns \\
\hline \(t_{w}(L)\) & \(\overline{M R}\) Pulse Width LOW & 18 & & & 18 & & & ns \\
\hline \(\mathrm{t}_{\text {rec }}\) & Recovery Time, \(\overline{\mathrm{MR}}\) to \(\overline{\mathrm{E}}_{\mathrm{n}}\) & 10 & & & 8 & & & ns \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) } \\
\hline
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{VOH}^{\text {O }}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{Ios} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& \text { (Note 2) }
\end{aligned}
\]} & MIL & -20 & & -70 & \multirow[t]{2}{*}{mA} \\
\hline & & & COM & -20 & & -57 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 3)} & & & 100 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I ICC is measured with all outputs open and all inputs grounded.

\section*{Functional Description}

Data can be entered into the latch when both of the enable inputs are LOW. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes HIGH, the data present in the latch at that time is held in the latch and is no longer affected by data input. The master reset overrides all other input conditions and forces the outputs of all the latches LOW when a LOW signal is applied to the Master Reset input.

\section*{Truth Table}
\begin{tabular}{|l|cc|c|c|l|}
\hline\(\overline{\text { MR }}\) & \multicolumn{1}{c}{ E0 } & \multicolumn{1}{c|}{ E1 } & \multicolumn{1}{c|}{ D } & Qn & Operation \\
\hline H & L & L & L & L & Data Entry \\
H & L & L & H & H & Data Entry \\
H & L & H & X & Qn-1 & Hold \\
H & H & L & X & Qn-1 & Hold \\
H & H & H & X & Qn-1 & Hold \\
L & X & X & X & L & Reset \\
\hline
\end{tabular}

\footnotetext{
\(Q_{n-1}=\) Previous Output State
\(Q_{n}=\) Present Output State
\(H=\) HIGH Voltage Level
L = LOW Voltage Level
\(\mathrm{X}=\) Immaterial
}

\section*{Logic Diagram}


TL/F/10208-3

Switching Characteristics \(\mathrm{v}_{\mathrm{CC}}=+5.0 \mathrm{v}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for test waveforms and output load.)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{2}{|c|}{9308} & \multirow{3}{*}{Units} \\
\hline & & \multicolumn{2}{|c|}{\[
\begin{aligned}
& C_{L}=15 \mathrm{pF} \\
& R_{\mathrm{L}}=400 \Omega
\end{aligned}
\]} & \\
\hline & & Min & Max & \\
\hline \begin{tabular}{l}
\(t_{\text {PLH }}\) \\
tpHL
\end{tabular} & Propagation Delay En to Qn & & \[
\begin{aligned}
& 30 \\
& 22 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
t_{\text {PLH }}
\]
\[
\mathrm{t}_{\mathrm{PHL}}
\] & Propagation Delay Dn to Qn & & \[
\begin{aligned}
& 15 \\
& 18 \\
& \hline
\end{aligned}
\] & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay \(\overline{M R}\) to Qn & & 22 & ns \\
\hline
\end{tabular}

National Semiconductor

\section*{9309/DM9309 Dual 4-Bit Data Selectors/Multiplexers}

\section*{General Description}

These data selectors/multiplexers contain inverter/drivers to supply full complementary, on-chip, binary decoded data selection.
The 9309/DM9309 contains two separate 4-bit multiplexers with complementary Y and \(\overline{\mathrm{Y}}\) outputs; however, the two sections have common address select inputs.

Features
- Complementary outputs
- Dual one-of-four data selectors

\section*{Connection Diagram}


\section*{Function Table}
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{6}{|c|}{ Inputs } & \multicolumn{3}{c|}{ Outputs } \\
\hline \multicolumn{2}{|c|}{ Select } & \multicolumn{4}{c|}{ Data } & Y & \(\bar{Y}\) \\
\hline B & A & C0 & C1 & C2 & C3 & & \\
\hline L & L & L & X & X & X & L & H \\
L & L & H & X & X & X & H & L \\
L & H & X & L & X & X & L & H \\
L & H & X & H & X & X & H & L \\
H & L & X & X & L & X & L & H \\
H & L & X & X & H & X & H & L \\
H & H & X & X & X & L & L & H \\
H & H & X & X & X & H & H & L \\
\hline
\end{tabular}

Select inputs A and B are common to both sections.
\(H=\) High Level, \(L=\) Low Level, \(X=\) Don't Care.
```

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for availability and specifications.
Supply Voltage
7V
Input Voltage
5.5V
Operating Free Air Temperature Range

| Military | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| :--- | ---: |
| Commercial | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
|  | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

```

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multicolumn{2}{|c|}{ Parameter } & \multicolumn{3}{|c|}{ Milltary } & \multicolumn{3}{c|}{ Commercial } \\
\cline { 3 - 8 } & & \multirow{2}{*}{ Units } \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & 5 & 5.5 & 4.75 & 5 & 5.25 \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 2 & & V \\
\hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & 0.8 & & & V \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & -0.8 & & & 0.8 & V \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & & 16 & & & -0.8 \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
(Note 1) & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, l_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \({ }_{1 /}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=M a x
\] \\
(Note 2)
\end{tabular}} & MIL & -20 & & -70 & \multirow[t]{2}{*}{mA} \\
\hline & & & COM & \(-30\) & & -85 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 3)} & & 27 & 44 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: \(\mathrm{ICC}_{\mathrm{CC}}\) is measured with the outputs open and all inputs at 4.5 V .

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{2}{|c|}{Military} & \multicolumn{2}{|l|}{Commercial} & \multirow{3}{*}{Units} \\
\hline & & & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \\
\hline & & & Min & Max & Min & Max & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Select to \(Y\) & & 29 & & 40 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Select to \(Y\) & & 27 & & 36 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Select to \(\bar{Y}\) & & 21 & & 24 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Select to \(\bar{Y}\) & & 21 & & 29 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Data to \(Y\) & & 20 & & 27 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to \(Y\) & & 21 & & 34 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Data to \(\bar{Y}\) & & 12 & & 21 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to \(\bar{Y}\) & & 13 & & 13 & ns \\
\hline
\end{tabular}

\section*{Logic Diagram}


TL/F/6602-2

\section*{9311/DM9311 4-Line to 16-Line Decoders/Demultiplexers}

\section*{General Description}

Each of these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

\section*{Features}
- Pin for pin with popular DM54154/74154
- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs

■ Typical propagation delay 19 ns
- Typical power dissipation 170 mW
- Alternate Military/Aerospace device (9311) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram
Dual-In-Line Package
inputs
OUTPUTS


TL/F/6604-1
Order Number 9311DMQB, 9311FMQB, DM9311J or DM9311N See NS Package Number J24A, N24A or W24C

\section*{Absolute Maximum Ratings (Note)}

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avallability and specifications.
Supply Voltage
Input Voltage
Operating Free Air Temperature Range

Military
\(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
Commercial \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
Storage Temperature Range
\[
-65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C}
\]

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Min}, l_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & 0.25 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{\mathrm{CC}}=M a x \\
& \text { (Note 2) }
\end{aligned}
\]} & MIL & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & COM & -18 & & -57 & \\
\hline \multirow[t]{2}{*}{ICC} & \multirow[t]{2}{*}{Supply Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=M a x
\] \\
(Note 3)
\end{tabular}} & MIL & & 34 & 49 & \multirow[t]{2}{*}{mA} \\
\hline & & & COM & & 34 & 56 & \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: ICC is measured with all inputs grounded and all outputs open.

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Data to Output & & 27 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to Output & & 30 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Strobe to Output & & 25 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Strobe to Output & & 27 & ns \\
\hline
\end{tabular}

\section*{Function Table}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{6}{|c|}{Inputs} & \multicolumn{16}{|c|}{Outputs} \\
\hline G1 & G2 & D & C & B & A & 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12 & 13 & 14 & 15 \\
\hline L & L & L & L & L & L & L & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline L & L & L & L & L & H & H & L & H & H & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline L & L & L & L & H & L & H & H & L & H & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline L & L & L & L & H & H & H & H & H & L & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline L & L & L & H & L & L & H & H & H & H & L & H & H & H & H & H & H & H & H & H & H & H \\
\hline L & L & L & H & L & H & H & H & H & H & H & L & H & H & H & H & H & H & H & H & H & H \\
\hline L & L & L & H & H & L & H & H & H & H & H & H & L & H & H & H & H & H & H & H & H & H \\
\hline L & L & L & H & H & H & H & H & H & H & H & H & H & L & H & H & H & H & H & H & H & H \\
\hline L & L & H & L & L & L & H & H & H & H & H & H & H & H & L & H & H & H & H & H & H & H \\
\hline L & L & H & L & L & H & H & H & H & H & H & H & H & H & H & L & H & H & H & H & H & H \\
\hline L & L & H & L & H & L & H & H & H & H & H & H & H & H & H & H & L & H & H & H & H & H \\
\hline L & L & H & L & H & H & H & H & H & H & H & H & H & H & H & H & H & L & H & H & H & H \\
\hline L & L & H & H & L & L & H & H & H & H & H & H & H & H & H & H & H & H & L & H & H & H \\
\hline L & L & H & H & L & H & H & H & H & H & H & H & H & H & H & H & H & H & H & L & H & H \\
\hline L & L & H & H & H & L & H & H & H & H & H & H & H & H & H & H & H & H & H & H & L & H \\
\hline L & L & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H & L \\
\hline L & H & X & X & X & X & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline H & L & X & x & X & X & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline H & H & X & X & X & \(x\) & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline
\end{tabular}

\footnotetext{
\(\mathrm{H}=\) High Level, \(\mathrm{L}=\) Low Level, \(\mathrm{X}=\) Don't Care.
}


\section*{9312/DM9312 One of Eight Line Data Selectors/Multiplexers}

\section*{General Description}

These data selectors/multiplexers contain inverter/drivers to supply full complementary, on-chip, binary decoded data selection.
The 9312 is a single 8 -bit multiplexer with complementary outputs and a strobe control. When the strobe is low, the function is enabled. When a high logic level is applied to the strobe, the output is forced to the logic zero state regardless of the logic level of the data inputs.

\section*{Features}
- Selects one-of-eight data sources

■ Performs parallel to serial conversion
- Strobe controlled outputs

■ Complementary outputs

\section*{Connection Diagram}

Dual-In-Line Package


Order Number 9312DMQB, 9312FMQB or DM9312N See NS Package Number J16A, N16E or W16A

Function Table
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multicolumn{4}{|c|}{ Inputs } & \multicolumn{2}{c|}{ Outputs } \\
\hline \multicolumn{3}{|c|}{ Select } & Strobe & \multirow{2}{*}{ Y } & \(\overline{\text { Y }}\) \\
\hline C & B & A & G & & \\
\hline X & X & X & H & L & H \\
L & L & L & L & D0 & \(\overline{\text { D0 }}\) \\
L & L & H & L & D1 & \(\overline{\text { D1 }}\) \\
L & H & L & L & D2 & \(\overline{\text { D2 }}\) \\
L & H & H & L & D3 & \(\overline{\text { D3 }}\) \\
H & L & L & L & D4 & \(\overline{\text { D4 }}\) \\
H & L & H & L & D5 & \(\overline{\text { D5 }}\) \\
H & H & L & L & D6 & \(\overline{\text { D6 }}\) \\
H & H & H & L & D7 & \(\overline{\text { D7 }}\) \\
\hline
\end{tabular}

\footnotetext{
H = High Level, L = Low Level, X = Don't Care.
D0, D1 \(\ldots\) D7 \(=\) The level of the respective \(D\) input.
}
\begin{tabular}{l} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage \\
Input Voltage \\
Operating Free Air Temperature Range \\
Military \\
Commercial \\
Storage Temperature Range \\
Sr \\
\hline
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline \({ }_{\mathrm{OL}}\) & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|r|}{Conditions} & Min & Typ
(Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{l}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=M a x
\] \\
(Note 2)
\end{tabular}} & MIL & -20 & & \(-70\) & \multirow[t]{2}{*}{mA} \\
\hline & & & COM & -30 & & -85 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\) Max, (Note 3)} & & 27 & 44 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: ICC is measured with the STROBE and DATA SELECT inputs 4.5 V and all other inputs and outputs open.

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{2}{|c|}{Military} & \multicolumn{2}{|r|}{Commercial} & \multirow{3}{*}{Units} \\
\hline & & & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \\
\hline & & & Min & Max & Min & Max & \\
\hline \({ }_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output & Selectz to \(Y\) & & 34 & & 33 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Select to \(Y\) & & 34 & & 35 & ns \\
\hline \({ }^{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & Select to \(\bar{Y}\) & & 24 & & 28 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Select to \(\bar{Y}\) & & 26 & & 25 & ns \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & Data to \(Y\) & & 24 & & 23 & ns \\
\hline \({ }_{\text {tpHL }}\) & Propagation Delay Time High to Low Level Output & Data to \(Y\) & & 24 & & 25 & ns \\
\hline \({ }_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output & Data to \(\bar{Y}\) & & 14 & & 13 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Data
\[
\text { to } \bar{Y}
\] & & 16 & & 13 & ns \\
\hline \(\mathrm{tplH}^{\text {l }}\) & Propagation Delay Time Low to High Level Output & Strobe to \(Y\) & & 30 & & 33 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Strobe to \(Y\) & & 30 & & 32 & ns \\
\hline \({ }_{\text {tpLH }}\) & Propagation Delay Time Low to High Level Output & Strobe to \(\bar{Y}\) & & 20 & & 19 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Strobe to \(\bar{Y}\) & & 23 & & 21 & ns \\
\hline
\end{tabular}


\section*{9314/DM9314 Quad Latch}

\section*{General Description}

The '9314 is a multifunctional 4-bit latch designed for general purpose storage applications in high speed digital systems. All outputs have active pull-up circuitry to provide high capacitance drive and to provide low impedance in both logic states for good noise immunity.

\section*{Connection Diagram}

\section*{Logic Symbol}

\section*{Dual-In-Line Package}


TL/F/9788-2
\(V_{C C}=P\) in 16
TL/F/9788-
Order Number 9314DMQB, 9314FMQB or DM9314N
See NS Package Number J16A, N16E or W16A
\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{c|}{ Description } \\
\hline\(\overline{\mathrm{E}}\) & Enable Input (Active LOW) \\
\(\mathrm{DO}-\mathrm{D} 3\) & Data Inputs \\
\(\overline{\mathrm{S}} 0-\overline{\mathrm{S} 3}\) & Set Inputs (Active LOW) \\
\(\overline{\mathrm{MR}}\) & Master Reset Input (Active LOW) \\
\(\mathrm{QO}-\mathrm{Q} 3\) & Latch Outputs \\
\hline
\end{tabular}
```

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for availability and specifications.
Supply Voltage
7V
Input Voltage
5.5V
Operating Free Air Temperature Range

| Military | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| :--- | ---: |
| Commercial | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

```

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{IOH}^{\text {l }}\) & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline \[
\begin{aligned}
& t_{s}(H) \\
& t_{s}(\mathrm{~L}) \\
& \hline
\end{aligned}
\] & Setup Time HIGH or LOW \(D_{n}\) to \(\bar{E}\) & \[
\begin{array}{r}
5.0 \\
18 \\
\hline
\end{array}
\] & & & \[
\begin{array}{r}
5.0 \\
18 \\
\hline
\end{array}
\] & & & ns \\
\hline \[
\begin{aligned}
& t_{h}(H) \\
& t_{h}(\mathrm{~L})
\end{aligned}
\] & Hold Time HIGH or LOW \(D_{n}\) to \(\bar{E}\) & \[
\begin{gathered}
0 \\
5.0
\end{gathered}
\] & & & \[
\begin{gathered}
0 \\
5.0 \\
\hline
\end{gathered}
\] & & & ns \\
\hline \(\mathrm{t}_{\mathrm{s}}(\mathrm{H})\) & Setup Time HIGH, \(\mathrm{D}_{\mathrm{n}}\) to \(\bar{S}_{\mathrm{n}}\) & 8.0 & & & 8.0 & & & ns \\
\hline \(t_{h}(L)\) & Hold Time LOW, \(\mathrm{D}_{\mathrm{n}}\) to \(\bar{S}_{\mathrm{n}}\) & 8.0 & & & 8.0 & & & ns \\
\hline \(t_{w}(L)\) & \(\bar{E}\) Pulse Width LOW & 18 & & & 18 & & & ns \\
\hline \(t_{w}(L)\) & \(\overline{M R}\) Pulse Width LOW & 18 & & & 18 & - & & ns \\
\hline \(\mathrm{t}_{\text {rec }}\) & Recovery Time, \(\overline{\mathrm{MR}}\) to \(\overline{\mathrm{E}}\) & 0 & & & 0 & & & ns \\
\hline
\end{tabular}

\section*{Electrical Characteristics}

Over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{I}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline VOL & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{2}{*}{\(\mathrm{IIH}^{\text {H }}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline & & \multicolumn{2}{|l|}{Data Inputs} & & & 60 & \\
\hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline & & \multicolumn{2}{|l|}{Data Inputs} & & & -2.7 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& \text { (Note 2) }
\end{aligned}
\]} & MIL & -20 & & -70 & \multirow[t]{2}{*}{mA} \\
\hline & & & COM & -20 & & -70 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & & 55 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

Switching Characteristics \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\)（See Section 1 for waveforms and load configurations）
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline tpLH
\[
\mathrm{t}_{\mathrm{PHL}}
\] & Propagation Delay \(\bar{E}\) to \(Q_{n}\) & & \[
\begin{aligned}
& 24 \\
& 24 \\
& \hline
\end{aligned}
\] & ns \\
\hline \begin{tabular}{l}
\(t_{\text {PLH }}\) \\
\(\mathrm{t}_{\mathrm{PHL}}\)
\end{tabular} & Propagation Delay \(D_{n}\) to \(Q_{n}\) & & \[
\begin{aligned}
& 12 \\
& 24 \\
& \hline
\end{aligned}
\] & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay \(\overline{M R}\) to \(Q_{n}\) & & 18 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay \(\bar{S}_{n}\) to \(Q_{n}\) & & 24 & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The＇9314 consists of four latches with a common active LOW Enable input and active LOW Master Reset input． When the Enable goes HIGH，data present in the latches is stored and the state of the latch is no longer affected by the \(\bar{S}_{n}\) and \(D_{n}\) inputs．The Master Reset when activated over－ rides all other input conditions forcing all latch outputs LOW． Each of the four latches can be operated in one of two modes：
D－TYPE LATCH—For D－type operation the \(\overline{\mathrm{S}}\) input of a latch is held LOW．While the common Enable is active the latch output follows the D input．Information present at the latch output is stored in the latch when the Enable goes HIGH．
SET／RESET LATCH－During set／reset operation when the common Enable is LOW a latch is reset by a LOW on the D input，and can be set by a LOW on the \(\overline{\mathrm{S}}\) input if the D input is HIGH．If both \(\overline{\mathrm{S}}\) and D inputs are LOW，the D input will dominate and the latch will be reset．When the Enable goes HIGH，the latch remains in the last state prior to disable－ ment．The two modes of latch operation are shown in the Truth Table．

\section*{Truth Table}
\begin{tabular}{|c|c|c|c|c|l|}
\hline\(\overline{\mathbf{M R}}\) & \(\overline{\mathbf{E}}\) & \(\mathbf{D}\) & \(\overline{\mathbf{S}}\) & \(\mathbf{Q}_{\boldsymbol{n}}\) & Operation \\
\hline\(H\) & \(L\) & \(L\) & \(L\) & \(L\) & D Mode \\
\(H\) & \(L\) & \(H\) & \(L\) & \(H\) & \\
\(H\) & \(H\) & \(X\) & \(X\) & \(Q_{\boldsymbol{n}-1}\) & \\
\hline\(H\) & \(L\) & \(L\) & \(L\) & \(L\) & R／S Mode \\
\(H\) & \(L\) & \(H\) & \(L\) & \(H\) & \\
\(H\) & \(L\) & \(L\) & \(H\) & \(L\) & \\
\(H\) & \(L\) & \(H\) & \(H\) & \(Q_{\boldsymbol{n}-1}\) & \\
\(H\) & \(H\) & \(X\) & \(X\) & \(Q_{n-1}\) & \\
\hline\(L\) & \(X\) & \(X\) & \(X\) & \(L\) & Reset \\
\hline
\end{tabular}

\footnotetext{
H＝HIGH Voltage Level
L＝LOW Voltage Level
\(X=\) Immaterial
\(Q_{n-1}=\) Previous Output State
\(Q_{n}=\) Present Output State
}


\section*{9316/DM9316 Synchronous 4-Bit Counters}

\section*{General Description}

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 9316 is a 4-bit binary counter. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enables inputs and internal gating. This mode of operating eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.
These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input. Low-to-high transitions at the load input are perfectly acceptable regardless of the logic levels on the clock or enable inputs. The clear function is asynchronous and a low level at the clear input sets of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs.

The carry look-ahead circuitry provides for cascading counters for \(n\)-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both countenable inputs ( \(P\) and \(T\) ) must be high to count, and input \(T\) is fed-forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the \(Q_{A}\) output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs may occur regardless of the logic level in the clock.

\section*{Features}
- Internal look-ahead for fast counting
- Carry output for n-bit cascading

■ Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical clock frequency 35 MHz
- Pin-for-pin replacements popular 54/74 counters 5416A/7416A (binary)
- Alternate Military/Aerospace device (9316) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Connection Diagram}


Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
5.5 V

Operating Free Air Temperature Range
\begin{tabular}{lr} 
Military & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
Commercial & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\text {CC }}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{IOH}^{\text {l }}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.8 & & & -0.8 & mA \\
\hline \(\mathrm{l}_{\mathrm{OL}}\) & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & & & 16 & mA \\
\hline \(\mathrm{f}_{\text {CLK }}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 6)} & 0 & & 25 & 0 & & 25 & MHz \\
\hline \multirow[t]{2}{*}{\(t_{W}\)} & \multirow[t]{2}{*}{Pulse Width (Note 6)} & Clock & 25 & & & 25 & & & \multirow[t]{2}{*}{ns} \\
\hline & & Clear & 20 & & & 20 & & & \\
\hline \multirow[t]{4}{*}{\({ }^{\text {t }}\) U} & \multirow[t]{4}{*}{Setup Time (Note 6)} & Data & 20 & & & 20 & & & \multirow{4}{*}{ns} \\
\hline & & Enable P & 20 & & & 20 & & & \\
\hline & & Load & 25 & & & 25 & & & \\
\hline & & Clear & 20 & & & 20 & & & \\
\hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Any Hold Time (Notes 1 \& 6)} & 0 & & & 0 & & & ns \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 2) }
\end{gathered}
\] & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline V OH & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}_{2}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{3}{*}{\(\mathrm{IIH}^{\text {H }}\)} & \multirow[t]{3}{*}{High Level Input Current} & \multirow[t]{3}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
& \mathrm{~V}_{1}=2.4 \mathrm{~V}
\end{aligned}
\]} & Clock & & & 80 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Enable T & & & 80 & \\
\hline & & & Other & & & 40 & \\
\hline \multirow[t]{3}{*}{ILL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=0.4 V
\end{aligned}
\]} & Clock & & & -3.2 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Enable T & & & -3.2 & \\
\hline & & & Other & & & -1.6 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{cc}}=\mathrm{Max} \\
& \text { (Note 3) }
\end{aligned}
\]} & MIL & -20 & & -57 & \multirow[t]{2}{*}{mA} \\
\hline & & & COM & -18 & & -57 & \\
\hline \multirow[t]{2}{*}{\(\mathrm{I}_{\mathrm{CCH}}\)} & \multirow[t]{2}{*}{Supply Current with Outputs High} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{Cc}}=\mathrm{Max} \\
& \text { (Note 4) }
\end{aligned}
\]} & MIL & & 59 & 85 & \multirow[t]{2}{*}{mA} \\
\hline & & & COM & & 59 & 94 & \\
\hline \multirow[t]{2}{*}{ICCL} & \multirow[t]{2}{*}{Supply Current with Outputs Low} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{\mathrm{Cc}}=M a x \\
& \text { (Note 5) }
\end{aligned}
\]} & MIL & & 63 & 91 & \multirow[t]{2}{*}{mA} \\
\hline & & & COM & & 63 & 101 & \\
\hline
\end{tabular}

Note 1: The minimum HOLD time is as specified or as long as the CLOCK input takes to rise from 0.8 V to 2 V , whichever is longer.
Note 2: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 3: Not more than one output should be shorted at a time.
Note 4: ICCH is measured with the LOAD input high, then again with the LOAD input low, with all other inputs high and all outputs open.
Note 5: ICCL is measured with the CLOCK input high, then again with the CLOCK input low, with all other inputs low and all outputs open.
Note 6: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

Switching Characteristics at \(\mathrm{V}_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 25 & & MHz \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to RC & & 27 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to RC & & 24 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Q & & 20 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
\begin{aligned}
& \text { Clock } \\
& \text { to } Q
\end{aligned}
\] & & 23 & ns \\
\hline tpLH & Propagation Delay Time Low to High Level Output & Clock to Q & & 21 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Q & & 25 & ns \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & \[
\begin{aligned}
& \text { ENT } \\
& \text { to RC }
\end{aligned}
\] & & 15 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
\begin{aligned}
& \text { ENT } \\
& \text { to RC }
\end{aligned}
\] & & 16 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
\begin{aligned}
& \text { Clear } \\
& \text { to } Q
\end{aligned}
\] & & 36 & ns \\
\hline
\end{tabular}


9316 Synchronous Binary Counters Typical Clear, Preset, Count and Inhibit Sequences


TL/F/6606-3
Sequence:
(1) Clear outputs to zero.
(2) Preset to binary twelve.
(3) Count to thirteen, fourteen, fifteen, zero, one, and two.
(4) Inhibit


TL/F/6606-4
Note A: The input pulses are supplied by a generator having the following characteristics: PRR \(\leq 1 \mathrm{MHz}\), duty cycle \(\leq 50 \%, Z_{\text {OUT }} \approx 50 \Omega, \mathrm{t}_{\mathrm{r}} \leq 10 \mathrm{~ns}, \mathrm{t}_{\mathrm{f}} \leq 10 \mathrm{~ns}\). Vary PRR to measure f MAX.
Note B: Outputs \(Q_{D}\) and carry are tested at \(t_{n}+16\) for \(9316 / 8316\), where \(t_{n}\) is the bit time when all outputs are low.
Note C: \(\mathrm{V}_{\text {REF }}=1.5 \mathrm{~V}\).

\section*{Parameter Measurement Information (Continued)}

\section*{Switching Time Waveforms}


TL/F/6606-5
Note \(A\) : The input pulses are supplied by generators having the following characteristics: PRR \(\leq 1 \mathrm{MHz}\), duty cycle \(\leq 50 \%, Z_{\text {OUT }} \approx 50 \Omega, \mathrm{t}_{\mathrm{r}} \leq 10 \mathrm{~ns}, \mathrm{t}_{\mathrm{f}} \leq 10 \mathrm{~ns}\). Note B: Enable P and Enable T setup times are measured at \(t_{n}+16\) for 8316/9316.
Note C: \(\mathrm{V}_{\text {REF }}=1.5 \mathrm{~V}\).

\section*{DM9318 Priority Encoders}

\section*{General Description}

These TTL encoders feature priority decoding of the input data to ensure that only the highest-order data line is encoded. All inputs are buffered to represent one normalized Series 54/74 load. The DM9318 and DM8318 encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input E1 and enable output E0) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level.

\section*{Features}
- Pin for pin with popular DM54148/74148
- Encodes 8 data lines to 3 -line binary (octal)
- Applications include:

N -bit encoding
Code converters and generators
m Typical data delay 10 ns
- Typical power dissipation 190 mW

\section*{Connection Diagram}


Order Number DM9318J, DM9318N or DM9318W See NS Package Number J16A, N16E or W16A

Function Table
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{9}{|c|}{Inputs} & \multicolumn{5}{|c|}{Outputs} \\
\hline E1 & 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & A2 & A1 & A0 & GS & EO \\
\hline H & X & X & X & X & X & X & X & X & H & H & H & H & H \\
\hline L & H & H & H & H & H & H & H & H & H & H & H & H & L \\
\hline L & X & X & X & X & X & X & X & L & L & L & L & L & H \\
\hline L & X & X & X & X & X & X & L & H & L & L & H & L & H \\
\hline L & X & X & X & X & X & L & H & H & L & H & L & L & H \\
\hline L & X & X & X & X & L & H & H & H & L & H & H & L & H \\
\hline L & X & X & X & L & H & H & H & H & H & L & L & L & H \\
\hline L & X & X & L & H & H & H & H & H & H & L & H & L & H \\
\hline L & X & L & H & H & H & H & H & H & H & H & L & L & H \\
\hline L & L & H & H & H & H & H & H & H & H & H & H & L & H \\
\hline
\end{tabular}

\footnotetext{
\(H=\) High Logic Level, \(L=\) Low Logic Level, \(X=\) Don't Care
}
\begin{tabular}{lr} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for avallability and specifications. \\
Supply Voltage & 7 V \\
Input Voltage & \(5.5^{2} \mathrm{~V}\) \\
Operating Free Air Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
Military & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Commercial & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, I_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & & & V \\
\hline VOL & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{2}{*}{IH} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{I}=2.4 V
\end{aligned}
\]} & 0 Input & & & 40 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Others & & & 80 & \\
\hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{I}}=0.4 \mathrm{~V}
\end{aligned}
\]} & 0 Input & & & -1.6 & \multirow[t]{2}{*}{mA} \\
\hline & & & Others & & & -3.2 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{\mathrm{CC}}=M a x \\
& \text { (Note 2) }
\end{aligned}
\]} & MIL & -35 & & -85 & \multirow[t]{2}{*}{mA} \\
\hline & & & COM & -35 & & -85 & \\
\hline \(\mathrm{lCC1}\) & Supply Current Condition 1 & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max},(\) Note 3)} & & 35 & 55 & mA \\
\hline lcc2 & Supply Current Condition 2 & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max},(\) Note 4)} & & 40 & 60 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: \(I_{C C 1}\) is measured with all inputs and outputs open.
Note 4: \(\mathrm{ICC}_{\mathrm{C}}\) is measured with inputs 7 and El grounded and outputs open.

Switching Characteristics at \(\mathrm{V}_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & 0 thru 7 to ABCD In Phase & & 15 & ns \\
\hline tPHL & Propagation Delay Time High to Low Level Output & 0 thru 7 to ABCD In Phase & & 14 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
\begin{aligned}
& 0 \text { thru } 7 \text { to } \\
& \text { ABCD Out of Phase }
\end{aligned}
\] & & 19 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & 0 thru 7 to ABCD Out of Phase & & 19 & ns \\
\hline tpLH & Propagation Delay Time Low to High Level Output & 0 thru 7 to E0 Out of Phase & & 9 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & 0 thru 7 to E0 Out of Phase & & 21 & ns \\
\hline \(\mathrm{tpLH}^{\text {l }}\) & Propagation Delay Time Low to High Level Output & 0 thru 7 to GS In Phase & & 27 & ns \\
\hline tPHL & Propagation Delay Time High to Low Level Output & 0 thru 7 to GS In Phase & & 21 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \begin{tabular}{l}
El to AO, 1, 2 \\
In Phase
\end{tabular} & & 15 & ns \\
\hline tPHL & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
El to AO, 1, 2 \\
In Phase
\end{tabular} & & 15 & ns \\
\hline tPLH & Propagation Delay Time Low to High Level Output & \begin{tabular}{l}
El to GS \\
In Phase
\end{tabular} & & 12 & ns \\
\hline tPHL & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
El to GS \\
In Phase
\end{tabular} & & 15 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \begin{tabular}{l}
El to EO \\
In Phase
\end{tabular} & & 15 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
El to E0 \\
In Phase
\end{tabular} & & 26 & ns \\
\hline
\end{tabular}


\section*{National Semiconductor}

\section*{9321/DM9321}

\section*{Dual 1-of-4 Decoder}

\section*{General Description}

The 9321 consists of two independent multipurpose decoders, each designed to accept two inputs and provide four mutually exclusive outputs. In addition an active LOW enable input, which gives demultiplexing capability, is provided for each decoder.

\section*{Features}
- Multifunction capability
- Mutually exclusive outputs
- Demultiplexing capability
- Active low enable for each decoder

\section*{Connection Diagram}

\section*{Dual-In-Line Package}


TL/F/10209-1

\section*{Logic Symbol}

\(V_{C C}=\operatorname{Pin} 16\)
GND \(=\operatorname{Pin} 8\)

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(V_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \begin{tabular}{l}
Typ \\
(Note 1)
\end{tabular} & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-10 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline VOH & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\text { Max }, \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, V_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{l}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \({ }_{1 /}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, V_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& \text { (Note 2) }
\end{aligned}
\]} & MIL & -20 & & -70 & mA \\
\hline & & & COM & -1.3 & & -3.7 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 3)} & & & 50 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: ICC is measured with all outputs open and all inputs grounded.
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \begin{tabular}{l}
\(t_{\text {PLH }}\) \\
\(\mathrm{t}_{\mathrm{PHL}}\)
\end{tabular} & Propagation Delay, An to \(\bar{O} \mathrm{n}\) & & \[
\begin{array}{r}
20 \\
21 \\
\hline
\end{array}
\] & ns \\
\hline \begin{tabular}{l}
\(t_{\text {PLH }}\) \\
\(\mathrm{t}_{\mathrm{PHL}}\)
\end{tabular} & Propagation Delay, \(\overline{\mathrm{E}}\) to \(\overline{\mathrm{O}} \mathrm{n}\) & & \[
\begin{aligned}
& 14 \\
& 18
\end{aligned}
\] & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The 9321 consists of two separate decoders each designed to accept two binary weighted inputs and provide four mutually exclusive active LOW outputs as shown in the logic symbol. Each decoder can be used as a 4-output demultiplexer by using the enable as a data input.

Truth Table (Each Decoder)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|c|}{Inputs} & \multicolumn{4}{|c|}{Outputs} \\
\hline \(\bar{E}\) & AO & A1 & \(\overline{0} 0\) & \(\overline{0} 1\) & \(\overline{\mathbf{O} 2}\) & \(\overline{0} 3\) \\
\hline L & L & L & L & H & H & H \\
\hline L & H & L & H & L & H & H \\
\hline L & L & H & H & H & L & H \\
\hline L & H & H & H & H & H & L \\
\hline H & X & X & H & H & H & H \\
\hline
\end{tabular}

H = HIGH Voltage Level
L = LOW Voltage Level
\(X=\) Immaterial

\section*{Logic Diagram}



\section*{9322/DM9322 Quad 2-Line to 1-Line Data Selectors/Multiplexers}

\section*{General Description}

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. True data is presented at the outputs.

\section*{Features}

■ Pin-for-pin with popular DM54157/74157
- Buffered inputs and outputs

\section*{Applications}
- Expand any data input point
- Multiplex dual-data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters
- Alternate Military/Aerospace device (9322) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Connection Diagram}


Order Number 9322DMQB, 9322FMQB, DM9322J,
DM9322W or DM8322N
See NS Package Number J16A, N16E or W16A

\section*{Function Table}
\begin{tabular}{|c|c|c|c|c|}
\hline \multicolumn{5}{|c|}{ Inputs } \\
\multirow{2}{*}{ Output } \\
\cline { 1 - 4 } Strobe & Select & A & B & Y \\
\hline H & X & X & X & L \\
L & L & L & X & L \\
L & L & H & X & H \\
L & H & X & L & L \\
L & H & X & H & H \\
\hline
\end{tabular}
\(H=\) High Level, \(L=\) Low Level, \(X=\) Don't Care.
\begin{tabular}{|c|c|}
\hline \multicolumn{2}{|l|}{Absolute Maximum Ratings (Note)} \\
\hline If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. & Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The \\
\hline Supply Voltage 7V & parametric values defined in the "Electrical Characteristics" \\
\hline Input Voltage 5.5V & \begin{tabular}{l}
table are not guaranteed at the absolute maximum ratings. \\
The "Recommended Operating Conditions" table will define
\end{tabular} \\
\hline \begin{tabular}{lr} 
Operating Free Air Temperature Range & \\
Military & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
Commercial & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
\end{tabular} & the conditions for actual device operation. \\
\hline Storage Temperature Range \(\quad-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) & \\
\hline
\end{tabular}

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline lOH & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline VOL & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.4 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=\operatorname{Max}
\] \\
(Note 2)
\end{tabular}} & MIL & -20 & & -55 & \multirow[t]{2}{*}{mA} \\
\hline & & & COM & -18 & & -55 & \\
\hline lcc & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 3)} & & 30 & 48 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: ICC is measured with 4.5 V applied to all inputs and all outputs open.

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(t_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output & Data to Output & & 14 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to Output & & 14 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Strobe to Output & & 20 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Strobe to Output & & 21 & ns \\
\hline \({ }_{\text {tpLH }}\) & Propagation Delay Time Low to High Level Output & Select to Output & & 23 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Select to Output & & 27 & ns \\
\hline
\end{tabular}

\section*{Logic Diagram}


\section*{General Description}

The 9324 expandable comparators provide comparison between two 5-bit words and give three outputs-"less than", "greater than" and "equal to". A HIGH on the active LOW
Enable Input forces all three outputs LOW.

\section*{Connection Diagram}


TL/F/9792-1
Order Number 9324DMQB, 9324FMQB, or DM9324N
See NS Package Number J16A, N16E or W16A
\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
\hline \(\bar{E}\) & Enable Input (Active LOW) \\
AO-A4 & Word A Parallel Inputs \\
B0-B4 & Word B Parallel Inputs \\
\(A<B\) & A Less than B Output (Active HIGH) \\
\(A>B\) & A Greater than B Output (Active HIGH) \\
\(A=B\) & A Equal to B Output (Active HIGH) \\
\hline
\end{tabular}
\begin{tabular}{|c|c|}
\hline \multicolumn{2}{|l|}{Absolute Maximum Ratings (Note)} \\
\hline If Military/Aerospace specified d please contact the National Se Office/Distributors for availability & ces are required, iconductor Sales d specifications. \\
\hline Supply Voltage & V \\
\hline Input Voltage & 5.5 V \\
\hline Operating Free Air Temperature Range & \\
\hline Military & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
\hline Commercial & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
\hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) }
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, l_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline VOL & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.4 \mathrm{~V}\)} & & & 80 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -3.2 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Max} \\
& (\text { Note 2) }
\end{aligned}
\]} & MIL & -20 & & -70 & \multirow[t]{2}{*}{mA} \\
\hline & & & COM & -20 & & -70 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x\)} & & & 81 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{Switching Characteristics}
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay \(\bar{E}\) to \(A=B\) & & \[
\begin{aligned}
& 14 \\
& 14 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay \(A_{n}, B_{n}\) to \(A>B\) & & \[
\begin{array}{r}
25 \\
22 \\
\hline
\end{array}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}}
\end{aligned}
\] & Propagation Delay
\[
A_{n}, B_{n} \text { to } A<B
\] & & \[
\begin{array}{r}
26 \\
21 \\
\hline
\end{array}
\] & ns \\
\hline \begin{tabular}{l}
\(t_{\text {PLH }}\) \\
tphL
\end{tabular} & Propagation Delay \(A_{n}, B_{n}\) to \(A=B\) & & \[
\begin{aligned}
& 30 \\
& 32 \\
& \hline
\end{aligned}
\] & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The '24 5-bit comparators use combinational circuitry to directly generate " \(A\) greater than \(B\) " and " \(A\) less than \(B\) " outputs. As evident from the logic diagram, these outputs are generated in only three gate delays. The "A equals B" output is generated in one additional gate delay by decoding the " \(A\) neither less than nor greater than \(B\) " condition with a NOR gate. All three outputs are activated by the active LOW Enable Input ( E ).
Tying the \(\mathrm{A}>\mathrm{B}\) output from one device into an A input on another device and the \(A<B\) output into the corresponding \(B\) input permits easy expansion.

Truth Table
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multicolumn{3}{|c|}{Inputs} & \multicolumn{3}{|c|}{Outputs} \\
\hline E & \(A_{n}\) & \(B_{n}\) & A \(<\) B & A \(>\) B & \(\mathbf{A}=\mathbf{B}\) \\
\hline H & X & X & L & L & L \\
\hline L & Word & d B & L & L & H \\
\hline L & Word & d B & L & H & L \\
\hline L & Word & d A & H & L & L \\
\hline
\end{tabular}
\(H=\) HIGH Voltage Level
L = LOW Voltage Level
\(X=\) Immaterial

The A4 and B4 inputs are the most significant inputs and AO, B0 the least significant. Thus if A4 is HIGH and B4 is LOW, the \(A>B\) output will be HIGH regardless of all other inputs except \(\overline{\mathrm{E}}\).

\section*{Logic Symbol}


\section*{9328/DM9328 Dual 8-Bit Shift Register}

\section*{General Description}

The '9328 is a high speed serial storage element providing 16 bits of storage in the form of two 8 -bit registers. The multifunctional capability of this device is provided by several features: 1) additional gating is provided at the input to both shift registers so that the input is easily multiplexed between two sources; 2) the clock of each register may be provided separately or together; 3) both the true and complementary outputs are provided from each 8-bit register, and both registers may be master cleared from a common input.

\section*{Connection Diagram}


TL/F/9793-1
Order Number 9328DMQB, 9328FMQB or DM9328N See NS Package Number J16A, N16E or W16A

\section*{Logic Symbol}

\(V_{C C}=\operatorname{Pin} 16\)
GND \(=\operatorname{Pin} 8\)
\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{c|}{ Description } \\
\hline S & Data Select Input \\
D0, D1 & Data Inputs \\
CP & Clock Pulse Input (Active HIGH) \\
& Common (Pin 9) \\
& Separate (Pins 7 and 10) \\
\(\overline{M R}\) & Master Reset Input (Active LOW) \\
Q7 & Last Stage Output \\
\(\overline{\text { Q }}\) & Complementary Output \\
\hline
\end{tabular}
\begin{tabular}{|c|c|}
\hline \multicolumn{2}{|l|}{} \\
\hline \multicolumn{2}{|l|}{\begin{tabular}{l}
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specifled devices are required, please contact the National Semiconductor Sales Office/Distributors for avallability and specifications.
\end{tabular}} \\
\hline Supply Voltage & \\
\hline Input Voltage & 5.5 \\
\hline Operating Free Air Temperature Range & \\
\hline Military & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ}\) \\
\hline Commercial & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ}\) \\
\hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \\
\hline
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{IOH}^{2}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
& \mathrm{t}_{\mathrm{s}}(\mathrm{~L})
\end{aligned}
\] & Setup Time HIGH or LOW
\[
D_{n} \text { to } C P
\] & \[
\begin{aligned}
& 20 \\
& 20
\end{aligned}
\] & & & \[
\begin{aligned}
& 20 \\
& 20
\end{aligned}
\] & & & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{h}}(\mathrm{H}) \\
& \mathrm{t}_{\mathrm{h}}(\mathrm{~L})
\end{aligned}
\] & Hold Time HIGH or LOW
\[
D_{n} \text { to } C P
\] & \[
\begin{aligned}
& 0 \\
& 0
\end{aligned}
\] & & & \[
\begin{aligned}
& 0 \\
& 0
\end{aligned}
\] & & & ns \\
\hline \[
\begin{aligned}
& t_{w}(H) \\
& t_{w}(L)
\end{aligned}
\] & Clock Pulse Width HIGH or LOW & \[
\begin{array}{r}
25 \\
25 \\
\hline
\end{array}
\] & & & \[
\begin{array}{r}
25 \\
25 \\
\hline
\end{array}
\] & & & ns \\
\hline \(t_{w}(L)\) & \(\overline{\text { MR }}\) Pulse Width with CP HIGH & 30 & & & 30 & & & ns \\
\hline \(t_{w}(L)\) & \(\overline{M R}\) Pulse Width with CP LOW & 40 & & & 40 & & & ns \\
\hline \(t_{\text {rec }}\) & Recovery Time \(\overline{M R}\) to CP & 33 & & & 33 & & & ns \\
\hline
\end{tabular}

\section*{Electrical Characteristics}

Over Recommended Operating Free Air Temperature Range (Unless Otherwise Noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ
(Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\] & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\] & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(V_{C C}=M a x, V_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \multirow[t]{4}{*}{\(\mathrm{IIH}^{\text {H }}\)} & \multirow[t]{4}{*}{High Level Input Current} & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{l}}=2.4 \mathrm{~V} \\
& \mathrm{MR}, \mathrm{D}_{\mathrm{n}} \text { Inputs }
\end{aligned}
\] & & & 40 & \multirow{4}{*}{\(\mu \mathrm{A}\)} \\
\hline & & CP Inputs & & & 60 & \\
\hline & & \(S\) Inputs & & & 80 & \\
\hline & & CP (COM) Inputs & & & 120 & \\
\hline \multirow[t]{4}{*}{IIL} & \multirow[t]{4}{*}{Low Level Input Current} & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{~V}_{1}=0.4 \mathrm{~V} \\
& \mathrm{MR}, \mathrm{D}_{\mathrm{n}} \text { Inputs }
\end{aligned}
\] & & & -1.6 & \multirow{4}{*}{mA} \\
\hline & & CP Inputs & & & -2.4 & \\
\hline & & \(S\) Inputs & & & -3.2 & \\
\hline & & CP (COM) Input & & & -4.8 & \\
\hline
\end{tabular}

Electrical Characteristics
Over Recommended Operating Free Air Temperature Range (Unless Otherwise Noted) (Continued)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) }
\end{gathered}
\] & Max & Units \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& \text { (Note 2) }
\end{aligned}
\]} & MIL & -20 & & -70 & \multirow[t]{2}{*}{mA} \\
\hline & & & COMM & -20 & & -70 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x\)} & & & 77 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Switching Characteristics
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\[
\begin{aligned}
& C_{L}=15 \mathrm{pF} \\
& R_{\mathrm{L}}=400 \Omega \\
& \hline
\end{aligned}
\]} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \(\mathrm{f}_{\text {max }}\) & Maximum Shift Right Frequency & 20 & & MHz \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay CP to Q7 or \(\bar{Q} 7\) & & \[
\begin{aligned}
& 20 \\
& 35 \\
& \hline
\end{aligned}
\] & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay \(\overline{\text { MR }}\) to Q7 & & 50 & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The two 8-bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 and 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master/slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flops in parallel. When the two clock inputs (the separate and the common) to the OR gate are LOW, the slave latches are steady, but data can enter the master latches via the R and S input. During the first LOW-to-HIGH transition of either, or both simultaneously, of the two clock inputs, the data inputs ( R and S ) are inhibited so that a later change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain HIGH. During the HIGH-to-LOW transition of the last remaining HIGH clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state. The data inputs ( \(R\) and \(S\) ) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic HIGH signal.

Each 8-bit shift register has a 2 -input multiplexer in front of the serial data input. The two data inputs D0 and D1 are controlled by the data select input (S) following the Boolean expression:
Serial data in: \(S_{D}=\) SDO + SD1
An asynchronous master reset is provided which, when activated by a LOW logic level, will clear all 16 stages independently of any other input signal.

Shift Select Table
\begin{tabular}{|ccc|c|}
\hline \multicolumn{3}{c|}{ INPUTS } & OUTPUT \\
\hline S & DO & D1 & Q7 ( \(\left.\mathbf{t}_{n}+8\right)\) \\
\hline\(L\) & \(L\) & \(X\) & \(L\) \\
\(L\) & \(H\) & \(X\) & \(H\) \\
\(H\) & \(X\) & \(L\) & \(L\) \\
\(H\) & \(X\) & \(H\) & \(H\) \\
\hline
\end{tabular}
\(H=\) HIGH Voltage Level
L = LOW Voltage Level
\(X=\) Immaterial
\(n+8=\) indicates state after eight clock pulse


\section*{9334/DM9334 8-Bit Addressable Latch}

\section*{General Description}

The DM9334 is a high speed 8-bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level high outputs. The device also incorporates an active level low common clear for resetting all latches, as well as an active level low enable.
The DM9334 has four modes of operation which are shown in the mode selection table. In the addressable latch mode, data on the data line ( D ) is written into the addressed latch. The addressed latch will follow the data input with all nonaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs.
In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the \(D\) input with all other inputs in the low state. In the clear mode all outputs are low and unaffected by the address and data inputs.

When operating the device as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.
The function tables summarize the operation of the product.

\section*{Features}
- Common clear
- Easily expandable
- Random (addressable) data entry
- Serial to parallel capability
- 8 bits of storage/output of each bit available
- Active high demultiplexing/decoding capability
- Alternate Military/Aerospace device (9334) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Connection Diagram}


TL/F/6609-1

\section*{Order Number 9334DMQB, 9334FMQB, DM9334J or DM9334N \\ See NS Package Number J16A, N16E or W16A}

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage 5.5 V

Operating Free Air Temperature Range
\begin{tabular}{lr} 
Military & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
Commercial & \(0^{\circ}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{MIllitary} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
\hline \({ }^{\mathrm{IOH}}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.8 & & & -0.8 & mA \\
\hline 1 loL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & & & 16 & mA \\
\hline tw & \multicolumn{2}{|l|}{ENABLE Pulse Width (Fig. 1) (Note 4)} & 19 & 13 & & 19 & 13 & & ns \\
\hline \multirow[t]{3}{*}{tsu} & \multirow[t]{3}{*}{Setup Time (Note 4)} & Data 1 (Fig. 4) & 20 & 13 & & 20 & 13 & & \multirow{3}{*}{ns} \\
\hline & & Data 0 (Fig. 4) & 20 & 14 & & 20 & 14 & & \\
\hline & & Address (Fig. 6) (Note 1) & 10 & 5 & & 10 & 5 & & \\
\hline \multirow[t]{2}{*}{\(\mathrm{t}_{\mathrm{H}}\)} & \multirow[t]{2}{*}{Hold Time (Note 4)} & Data 1 (Fig. 4) & 0 & -10 & & 0 & -10 & & \multirow[t]{2}{*}{ns} \\
\hline & & Data 0 (Fig. 4) & 0 & -13 & & 0 & -13 & & \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 2) } \\
\hline
\end{gathered}
\] & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & 2.4 & 3.6 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{2}{*}{\(\mathrm{I}_{\mathrm{H}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=2.4 V
\end{aligned}
\]} & \(\bar{E}\) Input & & & 60 & \multirow{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Others & & & 40 & \\
\hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=0.4 V
\end{aligned}
\]} & \(\bar{E}\) Input & & & -2.4 & \multirow[t]{2}{*}{mA} \\
\hline & & & Others & & & -1.6 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& (\text { Note 3) }
\end{aligned}
\]} & MIL & \(-30\) & & -100 & \multirow[t]{2}{*}{mA} \\
\hline & & & COM & -30 & & -100 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\) Max} & & 56 & 86 & mA \\
\hline
\end{tabular}

Note 1: The ADDRESS setup time is the time before the negative ENABLE transition that the ADDRESS must be stable so that the correct latch is addressed without affecting the other latches.
Note 2: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 4: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

Switching Characteristics at \(\mathrm{V}_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline tplH & Propagation Delay Time Low to High Level Output & Enable to Output, Fig. 1 & & 28 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Enable to Output, Fig. 1 & & 27 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Data to Output, Fig. 2 & & 35 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to Output, Fig. 2 & & 28 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Address to Output, Fig. 3 & & 35 & ns \\
\hline tPHL & Propagation Delay Time High to Low Level Output & Address to Output, Fig. 3 & & 35 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clear to Output, Fig. 5 & & 31 & ns \\
\hline
\end{tabular}

\section*{Function Tables}
\begin{tabular}{|l|l|l|}
\hline\(\overline{\mathbf{E}}\) & \(\overline{\mathbf{C}}\) & \multicolumn{1}{|c|}{ Mode } \\
\hline L & H & Addressable Latch \\
\(H\) & \(H\) & Memory \\
L & L & \begin{tabular}{l} 
Active High Eight \\
\\
\(H\)
\end{tabular} \\
L Channel Demultiplexer \\
& Clear \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{6}{|c|}{Inputs} & \multicolumn{8}{|c|}{Present Output States} & \multirow{2}{*}{Mode} \\
\hline \(\overline{\mathrm{C}}\) & \(\bar{E}\) & D & A0 & A1 & A2 & Q0 & Q1 & Q2 & Q3 & Q4 & Q5 & Q6 & Q7 & \\
\hline L & H & X & X & X & X & L & L & L & L & L & L & L & L & Clear \\
\hline L & L & L & L & L & L & L & L & L & L & L & L & L & L & \\
\hline L & L & H & L & L & L & H & L & L & L & L & L & L & L & \\
\hline L & L & L & H & L & L & L & L & L & L & L & L & L & L & \\
\hline L & L & H & H & L & L & L & H & L & L & L & L & L & L & \\
\hline - & \(\bigcirc\) & \(\bigcirc\) & & - & & & & & - & & & & & Demultiplex \\
\hline - & - & - & & - & & & & & - & & & & & \\
\hline L & L & H & H & H & H & L & L & L & L & L & L & L & H & \\
\hline H & H & X & X & X & X & \(Q_{N-1}\) & & & & & & & & Memory \\
\hline H & L & L & L & L & L & L & \(Q_{N-1}\) & \(Q_{N-1}\) & \(Q_{N-1}\) & & & & & \\
\hline H & L & H & L & L & L & H & \(Q_{N-1}\) & \(Q_{N-1}\) & & & & & & \\
\hline H & L & L & H & L & L & \(Q_{N-1}\) & L & \(Q_{N-1}\) & & & & & & \\
\hline H & L & H & H & L & L & \(Q_{N-1}\) & H & \(Q_{N-1}\) & & & & & & Addressable \\
\hline - & - & - & & - & & & & - & & & & & & Latch \\
\hline - & \(\bigcirc\) & \(\bigcirc\) & & - & & & & - & & & & & & \\
\hline - & - & - & & - & & & & - & & & & & & \\
\hline H & L & L & H & H & H & \(Q_{N-1}\) & & & & & & \(Q_{N-1}\) & L & \\
\hline H & L & H & H & H & H & \(Q_{N-1}\) & & & & & & \(Q_{N-1}\) & H & \\
\hline
\end{tabular}
\(\mathrm{X}=\) Don't Care Condition
L = Low Voltage Level
\(H=\) High Voltage Level
\(Q_{N-1}=\) Previous Output State


\section*{Switching Time Waveforms}


TL/F/6609-4
Other Conditions: \(\bar{E}=L, \bar{C}=H, A=\) Stable
Figure 2
TL/F/6609-3
Other Conditions: \(C=H, A=\) Stable
Figure 1


TL/F/6609-5
Other Conditions: \(\bar{E}=L, \bar{C}=L, D=H\)
Figure 3


Figure 5
Other Conditons: \(\overline{\mathrm{E}}=\mathrm{H}\)


Other Conditions: \(C=H, A=\) Stable
Figure 4


Figure 6
Note: The shaded areas indicate when the inputs are permitted to change for predictable output performance.

\section*{National Semiconductor \\ 9338/DM9338 8-Bit Multiple Port Register}

\section*{General Description}

The DM9338 is an 8-bit multiple port register designed for high speed random access memory applications where the ability to simultaneously read and write is desirable. A common use would be as a register bank in a three address computer. Data can be written into any one of the eight bits and read from any two of the eight bits simultaneously.

\section*{Connection Diagrams}


TL/F/9794-1
Order Number 9338DMQB, 9338FMQB or DM9338N See NS Package Number J16A, N16E or W16A
\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
\hline\(A 0-A 2\) & Write Address Inputs \\
\(D_{A}\) & Data Input \\
B0-B2 & B Read Address Inputs \\
CO-C2 & C Read Address Inputs \\
\(C P\) & Clock Pulse Input (Active Rising Edge) \\
\(\overline{S L E}\) & Slave Enable Input (Active LOW) \\
\(Z_{B}\) & B Output \\
\(Z_{C}\) & C Output \\
\hline
\end{tabular}
\begin{tabular}{lr} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
Military & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Commercial & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -0.8 & & & -0.8 & mA \\
\hline lOL & Low Level Output Current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
& \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
& \hline
\end{aligned}
\] & Setup Time HIGH or LOW \(\mathrm{D}_{\mathrm{A}}\) to CP & \[
\begin{aligned}
& 20 \\
& 12 \\
& \hline
\end{aligned}
\] & & & \[
\begin{aligned}
& 20 \\
& 12 \\
& \hline
\end{aligned}
\] & & & ns \\
\hline \[
\begin{aligned}
& t_{h}(H) \\
& t_{h}(L) \\
& \hline
\end{aligned}
\] & Hold Time HIGH or LOW \(D_{A}\) to CP & \[
\begin{gathered}
0 \\
-8.0 \\
\hline
\end{gathered}
\] & & & \[
\begin{gathered}
0 \\
-8.0 \\
\hline
\end{gathered}
\] & & & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
& \mathrm{t}_{\mathrm{s}}(\mathrm{~L})
\end{aligned}
\] & Setup Time HIGH or LOW
\[
A_{n} \text { to } C P
\] & \[
\begin{aligned}
& 10 \\
& 10
\end{aligned}
\] & & & \[
\begin{aligned}
& 10 \\
& 10
\end{aligned}
\] & & & ns \\
\hline \[
\begin{aligned}
& t_{h}(H) \\
& t_{h}(L) \\
& \hline
\end{aligned}
\] & Hold Time HIGH or LOW
\[
A_{n} \text { to } C P
\] & \[
\begin{aligned}
& 0 \\
& 0
\end{aligned}
\] & & & \[
\begin{aligned}
& 0 \\
& 0
\end{aligned}
\] & & & ns \\
\hline \[
\begin{aligned}
& t_{w}(H) \\
& t_{w}(L)
\end{aligned}
\] & CP Pulse Width HIGH or LOW & \[
\begin{aligned}
& 23 \\
& 13
\end{aligned}
\] & & & \[
\begin{aligned}
& 23 \\
& 13
\end{aligned}
\] & & & ns \\
\hline
\end{tabular}

\section*{Electrical Characteristics}

Over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{I}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline VOL & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=2.4 \mathrm{~V}\)} & & & 27 & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{I}_{1 /}\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.1 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& (\text { Note 2) }
\end{aligned}
\]} & MIL & -10 & & -70 & \multirow[t]{2}{*}{mA} \\
\hline & & & COM & -10 & & -70 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & & 135 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{Switching Characteristics}
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow{3}{*}{Units} \\
\hline & & \multicolumn{2}{|c|}{9338 (MIL)} & \multicolumn{2}{|r|}{DM9338 (COM)} & \\
\hline & & Min & Max & Min & Max & \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{pLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay \(B_{n}\) or \(C_{n}\) to \(Z_{n}\) & & \[
\begin{array}{r}
40 \\
35 \\
\hline
\end{array}
\] & \[
\begin{array}{r}
13 \\
18 \\
\hline
\end{array}
\] & \[
\begin{array}{r}
40 \\
35 \\
\hline
\end{array}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}}
\end{aligned}
\] & Propagation Delay \(D_{A}\) to \(Z_{n}\) & & \[
\begin{array}{r}
45 \\
50 \\
\hline
\end{array}
\] & \[
\begin{aligned}
& 25 \\
& 25 \\
& \hline
\end{aligned}
\] & \[
\begin{array}{r}
45 \\
50 \\
\hline
\end{array}
\] & ns \\
\hline \(t_{\text {pLH }}\)
\[
\mathrm{t}_{\mathrm{PHL}}
\] & Propagation Delay CP to \(Z_{n}\) & & \[
\begin{aligned}
& 35 \\
& 30
\end{aligned}
\] & \[
\begin{array}{r}
18 \\
13 \\
\hline
\end{array}
\] & \[
\begin{aligned}
& 35 \\
& 30
\end{aligned}
\] & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The 93388 -bit multiple port register can be considered a 1 bit slice of eight high speed working registers. Data can be written into any one and read from any two of the eight locations simultaneously. Master/slave operation eliminates all race problems associated with simultaneous read/write activity from the same location. When the clock input (CP) is LOW data applied to the data input line ( \(\mathrm{D}_{\mathrm{A}}\) ) enters the selected master. This selection is accomplished by coding the three write input select lines (AO-A2) appropriately. Data is stored synchronously with the rising edge of the clock pulse.
The information for each of the two slaved (output) latches is selected by two sets of read address inputs ( \(\mathrm{BO}-\mathrm{B} 2\) and C0-C2). The information enters the slave while the clock is HIGH and is stored while the clock is LOW. If Slave Enable is LOW (SLE), the slave latches are continuously enabled. The signals are available on the output pins ( \(Z_{B}\) and \(Z_{C}\) ). The input bit selection and the two output bit selections can be accomplished independently or simultaneously. The data flows into the device, is demultiplexed according to the state of the write address lines and is clocked into the selected latch. The eight latches function as masters and store the input data. The two output latches are slaves and hold the
data during the read operation. The state of each slave is determined by the state of the master selected by its associated set of read address inputs.
The method of parallel expansion is shown in Figure a. One 9338 is needed for each bit of the required word length. The read and write input lines should be connected in common on all of the devices. This register configuration provides two words of \(n\)-bits each at one time, where \(n\) devices are connected in parallel.

\section*{Logic Symbol}


TL/F/9794-2
\(V_{C C}=\operatorname{Pin} 16\)
GND \(=\operatorname{Pin} 8\)


TL/F/9794-4
FIGURE a. Parallel Expansion

Logic Diagram


\section*{9348}

\section*{12-Input Parity Checker/Generator}

\section*{General Description}

The 9348 is a 12 -input parity checker/generator generating odd and even parity outputs. It can be used in high speed error detection applications.

\section*{Connection Diagram}

\section*{Logic Symbol}

Dual-In-Line Package


TL/F/9795-2
\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Pin} 16 \\
& \mathrm{GND}=\operatorname{Pin} 8
\end{aligned}
\]

TL/F/9795-1
Order Number 9348DMQB or 9348FMQB
See NS Package Number J16A or W16A
\begin{tabular}{|l|l|}
\hline Pin Names & Description \\
\hline \(10-111\) & Parity Inputs \\
PO & Odd Parity Output \\
PE & Even Parity Output \\
\hline
\end{tabular}
\begin{tabular}{|c|c|}
\hline \multicolumn{2}{|l|}{Absolute Maximum Ratings} \\
\hline If Military/Aerospace specified devic please contact the National Semi Office/Distributors for availability and & ices are required, iconductor Sales d specifications. \\
\hline Supply Voltage & 7 V \\
\hline Input Voltage & 5.5 V \\
\hline Operating Free Air Temperature Range Military & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
\hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multicolumn{2}{|c|}{ Parameter } & \multicolumn{2}{|c|}{9348} & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -0.8 & mA \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 16 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics}

Over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) }
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}\) & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\mathrm{Max}, \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}\) & & & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \(V_{C C}=M a x, V_{1}=2.4 V\) & & & 80 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -3.2 & mA \\
\hline los & Short Circuit Output Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 2) & -20 & & -70 & mA \\
\hline ICC & Supply Current & \(V_{C C}=\operatorname{Max}\) & & & 82 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Switching Characteristics
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configuration)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Conditions} & \multicolumn{2}{|c|}{\[
\begin{aligned}
& \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\
& \mathrm{R}_{\mathrm{L}}=400 \Omega
\end{aligned}
\]} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\text {PLH }} \\
& \mathrm{t}_{\mathrm{PH}} \\
& \hline
\end{aligned}
\] & Propagation Delay 14 to PO & \(\mathrm{I} 2, \mathrm{I}, \mathrm{I} 7,18=\) GND; Other Inputs (except 14) HIGH & & \[
\begin{aligned}
& 46 \\
& 42 \\
& \hline
\end{aligned}
\] & ns \\
\hline \begin{tabular}{l}
\({ }^{\text {tpLH }}\) \\
\(t_{\text {PHL }}\)
\end{tabular} & Propagation Delay 14 to PE & \(12,13,17,18=\) GND; Other Inputs (except 14) HIGH & & \[
\begin{aligned}
& 51 \\
& 48
\end{aligned}
\] & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay 13 to PO & \(17=\) HIGH; Other Inputs (except 13 ) = GND & & 27 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay 14 to PO & All Inputs (except 14) = GND & & 25 & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The 9348 is a 12 -input parity generator. It provides odd and even parity for up to 12 data bits. The Even Parity output (PE) will be HIGH if an even number of logic ones are present on the inputs. The Odd Parity output (PO) will be HIGH if an odd number of logic ones are present on the inputs. The logic equations for the outputs are shown below.

Note: Less through delay is encountered from the \(10, I 1\), I2 and 13 inputs than 14 thru I11 inputs. Therefore, if some signals are slower than others, the slower signals should be applied to these four inputs for maximum speed.

\section*{Truth Table}
\begin{tabular}{|l|l|c|c|}
\hline \multicolumn{2}{|c|}{ Inputs } & \multicolumn{2}{c|}{ Outputs } \\
\hline \multicolumn{2}{|c|}{ I0-I11 } & PO & PE \\
\hline All Twelve & Inputs LOW & L & H \\
Any One & Inputs HIGH & H & L \\
Any Two & Inputs HIGH & L & H \\
Any Three & Inputs HIGH & H & L \\
Any Four & Inputs HIGH & L & H \\
Any Five & Inputs HIGH & H & L \\
Any Six & Inputs HIGH & L & H \\
Any Seven & Inputs HIGH & H & L \\
Any Eight & Inputs HIGH & L & H \\
Any Nine & Inputs HIGH & H & L \\
Any Ten & Inputs HIGH & L & H \\
Any Eleven & Inputs HIGH & H & L \\
Any Twelve & Inputs HIGH & L & H \\
\hline
\end{tabular}

H = HIGH Voltage Level
L = LOW Voltage Level

\section*{Logic Diagram}


\section*{DM9368 7-Segment Decoder/Driver/Latch with Constant Current Source Outputs}

\section*{General Description}

The DM9368 is a 7 -segment decoder driver incorporating input latches and constant current output circuits to drive common cathode type LED displays directly.

\section*{Connection Diagram}

\begin{tabular}{|l|l|}
\hline Pin Name & \multicolumn{1}{|c|}{ Description } \\
\hline A0-A3 & Address (Data) Inputs \\
\(\overline{\text { RBO }}\) & Ripple Blanking Output (Active Low) \\
\(\overline{\mathrm{RBI}}\) & Ripple Blanking Input (Active Low) \\
\(\mathrm{a}-\mathrm{g}\) & Segment Drivers-Outputs \\
\(\overline{\mathrm{LE}}\) & Latch Enable Input (Active Low) \\
\hline
\end{tabular}
```

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for availability and specifications.
Supply Voltage 7V
Input Voltage 5.5 V
Operating Free Air Temperature Range $\quad 0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$
Storage Temperature Range $\quad-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

```

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM9368} & \multirow{2}{*}{Units} \\
\hline & & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline IOH & High Level Output Current & & -80 & & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{lOL}^{\text {l }}\) & Low Level Output Current & & & 16 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline \(\mathrm{t}_{\mathrm{s}}(\mathrm{H})\) & Setup Time High \(A_{n}\) to \(\overline{L E}\) & 30 & & & ns \\
\hline \(t_{h}(\mathrm{H})\) & Hold Time HIGH \(A_{n}\) to \(\overline{L E}\) & 0 & & & ns \\
\hline \(\mathrm{t}_{\mathrm{s}}(\mathrm{L})\) & Setup Time LOW \(A_{n}\) to \(\overline{\text { LE }}\) & 20 & & & ns \\
\hline \(t_{\text {f }}(\mathrm{L})\) & Hold Time LOW \(A_{n}\) to \(\overline{L E}\) & 0 & & & ns \\
\hline \(t_{w}(\mathrm{~L})\) & LE Pulse Width LOW & 45 & & & ns \\
\hline IOH & Segment Output HIGH Current & -16 & & -22 & mA \\
\hline lOL & Segment Output LOW Current & -250 & & 250 & \(\mu \mathrm{A}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics}

Over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & \begin{tabular}{l}
Typ \\
(Note 1)
\end{tabular} & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(V_{C C}=\operatorname{Min}, l_{l}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\text { Max, } \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
\begin{aligned}
& V_{C C}=M i n, I_{O L}=M a x, \\
& V_{I H}=M i n
\end{aligned}
\] & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \(V_{C C}=M a x, V_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \(V_{C C}=M a x, V_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline los & Short Circuit Output Current & \[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Max} \\
& (\text { Note 2) } \\
& \hline
\end{aligned}
\] & -18 & & -57 & mA \\
\hline ICC & Supply Current & \begin{tabular}{l}
\(V_{C C}=\) Max, Outputs Open, \\
Data \& Latch Inputs \(=0 \mathrm{~V}\)
\end{tabular} & & & 67 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{Switching Characteristics}
\(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Waveforms and Load Configuations)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\[
\begin{aligned}
& C_{\mathrm{L}}=15 \mathrm{pF} \\
& \mathrm{R}_{\mathrm{L}}=100 \Omega
\end{aligned}
\]} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \[
t_{\text {PLH }}
\]
\[
\mathrm{t}_{\mathrm{PHL}}
\] & Propagation Delay \(A_{n}\) to a-g & & \[
\begin{aligned}
& 40 \\
& 70 \\
& \hline
\end{aligned}
\] & ns \\
\hline \begin{tabular}{l}
tpLH \\
\(\mathrm{t}_{\mathrm{PHL}}\)
\end{tabular} & Propagation Delay \(\overline{L E}\) to \(a-g\) & & \[
\begin{aligned}
& 70 \\
& 90
\end{aligned}
\] & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The '68 is a 7 -segment decoder driver designed to drive 7 segment common cathode LED displays. The ' 68 drives any common cathode LED display rated at a nominal 20 mA at 1.7V per segment without need for current limiting resistors. This device accepts a 4-bit binary code and produces output drive to the appropriate segments of the 7 -segment display. It has a hexadecimal decode format which produces numeric codes " 0 " thru " 9 " and alpha codes " \(A\) " through " \(F\) " using upper and lower case fonts.
Latches on the four data inputs are controlled by an active LOW latch enable \(\overline{L E}\). When the \(\overline{L E}\) is LOW, the state of the outputs is determined by the input data. When the \(\overline{L E}\) goes HIGH, the last data present at the inputs is stored in the latches and the outputs remain stable. The LE pulse width necessary to accept and store data is typically 30 ns which allows data to be strobed into the '68 at normal TTL speeds. This feature means that data can be routed directly from high speed counters and frequency dividers into the display without slowing down the system clock or providing intermediate data storage.
Another feature of the '68 is that the unit loading on the data inputs is very low ( \(-100 \mu \mathrm{~A}\) Max) when the latch enable is

HIGH. This allows '68s to be driven from an MOS device in multiplex mode without the need for drivers on the data lines.
The '68 also has provision for automatic blanking of the leading and/or trailing edge zeros in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03 . Leading edge zero suppression is obtained by connecting the Ripple Blanking Output ( \(\overline{\mathrm{RBO}}\) ) of a decoder to the Ripple Blanking Input ( \(\overline{\mathrm{RBI}}\) ) of the next lower stage device. The most significant decoder stage should have the RBI input grounded; and since suppression of the least significant integer zero in a number is not usually desired, the \(\overline{\text { RBI }}\) input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeros. The RBO terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL or DTL gates.

\section*{Logic Symbol}


\section*{Truth Table}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{BINARY STATE} & \multicolumn{7}{|c|}{INPUTS} & \multicolumn{9}{|c|}{OUTPUTS} & \multirow[b]{2}{*}{DISPLAY} \\
\hline & \multicolumn{7}{|l|}{\(\overline{L E} \overline{\mathrm{RBI}}\) A3 A2 A1 AO} & a & b & b & c & d & e & \(f\) & g & RBO & \\
\hline - & H & * & X & X & X & X & X & & & & S & TABL & E & & \(\rightarrow\) & H & STABLE \\
\hline 0 & L & L & L & L & L & L & L & L & & L & L & L & L & L & L & L & BLANK \\
\hline 0 & L & H & L & L & L & L & L & H & & H & H & H & H & H & L & H & \% \\
\hline 1 & L & \(X\) & L & L & L & L & H & L & & H & H & L & L & L & L & H & ; \\
\hline 2 & L & \(x\) & L & L & H & H & L & H & & H & L & H & H & L & H & H & \% \\
\hline 3 & L & X & L & L & H & H & H & H & & H & H & H & L & L & H & H & 3 \\
\hline 4 & L & X & L & H & L & L & L & L & & H & H & L & L & H & H & H & \(\because\) \\
\hline 5 & L & \(x\) & L & H & L & & H & H & & L & H & H & L & H & H & H & 5 \\
\hline 6 & L & \(X\) & L & H & H & H & L & H & & L & H & H & H & H & H & H & 6 \\
\hline 7 & L & \(x\) & L & H & H & H & H & H & & H & H & L & L & L & L & H & ; \\
\hline 8 & L & X & H & L & L & L & L & H & & H & H & H & H & H & H & H & 8 \\
\hline 9 & L & \(X\) & H & L & L & L & H & H & & H & H & L & L & H & H & H & 9 \\
\hline 10 & L. & \(x\) & H & L & H & H & L & H & & H & H & L & H & H & H & H & 8 \\
\hline 11 & L & \(x\) & H & L & H & H & H & L & & L & H & H & H & H & H & H & 6 \\
\hline 12 & L & X & H & H & L & L & L & H & & L & L & H & H & H & L & H & \(\bigcirc\) \\
\hline 13 & L & X & H & H & L & L & H & L & & H & H & H & H & L & H & H & \(\theta\) \\
\hline 14 & L & \(x\) & H & H & H & H & L & H & & L & L & H & H & H & H & H & E \\
\hline 15 & L & \(x\) & H & H & H & H & H & H & & L & L & L & H & H & H & H & \(:\) \\
\hline X & X & \(X\) & \(X\) & \(X\) & X & X & X & L & & L & L & L & L & L & L & L** & BLANK \\
\hline
\end{tabular}

TL/F/9796-4

TL/F/9796-8
*The \(\overline{\mathrm{RBI}}\) will blank the display only if a binary zero is stored in the latches.
**The \(\overline{\mathrm{RBO}}\) used as an input overrides all other input conditions.
H \(=\) HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

\section*{Logic Diagram}


TL/F/9796-3

Numerical Designations
\begin{tabular}{|c|}
\hline  \\
\hline
\end{tabular}

\section*{Parallel Data Display System with Ripply Blanking}


\section*{Display Demultiplexing System with Ripple Blanking}


Note: Digit address data must be non-overlapping. Standard TTL decoders like the 9301, 9311, 7442 or 74155 must be strobed, since the address decoding glitches could cause erroneous data to be strobed into the latches.

\section*{DM9370 7-Segment Decoder/Driver/Latch with Open-Collector Outputs}

\section*{General Description}

The DM9370 is a 7 -segment decoder driver incorporating input latches and output circuits to directly drive incandescent displays. It can also be used to drive common anode LED displays in either a multiplexed mode or directly with the aid of external current limiting resistors.

\section*{Connection Diagram}
Dual-in-Line Package
Order Number DM9370N
See NS Package Number N16E
\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
\hline A0-A3 & Address Inputs \\
\(\overline{\text { LE }}\) & Latch Enable Input (Active LOW) \\
\(\overline{\text { RBI }}\) & Ripple Blanking Input (Active LOW) \\
\(\overline{\text { RBO }}\) & Ripple Blanking as Output (Active LOW) \\
& \(\quad\) as Input (Active LOW) \\
\(\overline{\mathrm{a}}-\overline{\mathrm{g}}\) & Segment Outputs (Active LOW) \\
\hline
\end{tabular}
\begin{tabular}{l} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage \\
Input Voltage \\
Operating Free Air Temperature Range \\
Commercial \\
Storage Temperature Range \\
\hline
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The devic should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM9370} & \multirow{2}{*}{Units} \\
\hline & & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline IOH & High Level Output Current & & & -80 & \(\mu \mathrm{A}\) \\
\hline lOL & Low Level Output Current & & & 3.2 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
& \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
& \hline
\end{aligned}
\] & Setup Time HIGH or LOW \(A_{n}\) to \(\overline{L E}\) & & & \[
\begin{aligned}
& 30 \\
& 20 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& t_{h}(H) \\
& t_{h}(\mathrm{~L}) \\
& \hline
\end{aligned}
\] & Hold Time HIGH or LOW \(A_{n}\) to \(\overline{L E}\) & & & \[
\begin{aligned}
& 0 \\
& 0
\end{aligned}
\] & ns \\
\hline \(\mathrm{t}_{\mathrm{w}}(\mathrm{L})\) & LE Pulse Width LOW & & & 45 & ns \\
\hline
\end{tabular}

\section*{Electrical Characteristics}

Over recommended operating free air temperature range (unless otherwise noted)

\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\[
\begin{aligned}
& C_{\mathrm{L}}=15 \mathrm{PF} \\
& \mathbf{R}_{\mathrm{L}}=500 \Omega
\end{aligned}
\]} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay \(A_{n}\) to \(\bar{a}-\bar{g}\) & & \[
\begin{aligned}
& 75 \\
& 50 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}}
\end{aligned}
\] & Propagation Delay \(\overline{\mathrm{LE}}\) to \(\overline{\mathrm{a}}-\overline{\mathrm{g}}\) & & \[
\begin{aligned}
& 90 \\
& 70
\end{aligned}
\] & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The '70 has active LOW outputs capable of sinking in excess of 25 mA which allows it to drive a wide variety of 7-segment incandescent displays directly. It may also be used to drive common anode LED displays, multiplexed or directly with the aid of suitable current limiting resistors. This device accepts a 4-bit binary code and produces output drive to the appropriate segments of the 7 -segment display. It has a hexadecimal decode format which produces numeric codes " 0 " through " 9 " and alpha codes " \(A\) " through " \(F\) " using upper and lower case fonts.
Latches on the four data inputs are controlled by an active LOW latch enable \(\overline{L E}\). When the \(\overline{L E}\) is LOW, the state of the outputs is determined by the input data. When the \(\overline{L E}\) goes HIGH, the last data present at the inputs is stored in the latches and the outputs remain stable. The \(\overline{L E}\) pulse width necessary to accept and store data is typically 30 ns which allows data to be strobed into the '70 at normal TTL speeds. This feature means that data can be routed directly from high speed counters and frequency dividers into the display without slowing down the system clock or providing intermediate data storage.
The latch/decoder combination is a simple system which drives incandescent displays with multiplexed data inputs from MOS time clocks, DVMs, calculator chips, etc. Data inputs are multiplexed while the displays are in static mode. This lowers component and insertion costs since several circuits-seven diodes per display, strobe drivers, a sepa-
rate display voltage source, and clock failure detect cir-cuits-traditionally found in incandescent multiplexed display systems are eliminated. It also allows low strobing rates to be used without display flicker.
Another ' 70 feature is the reduced loading on the data inputs when the Latch Enable is HIGH (only \(10 \mu \mathrm{~A}\) typ). This allows many ' 70 s to be driven from a MOS device in multiplex mode without the need for drivers on the data lines. The ' 70 also provides automatic blanking of the leading and/or trailing-edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an 8 -digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03 . Leadingedge zero suppression is obtained by connecting the Ripple Blanking Output ( \(\overline{\mathrm{RBO}}\) ) of a decoder to the Ripple Blanking Input ( \(\overline{\mathrm{RBI}}\) of the next lower stage device. The most significant decoder stage should have the \(\overline{\text { RBI }}\) input grounded; and since suppression of the least significant integer zero in a number is not usually desired, the RBI input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing-edge zeroes. The RBO terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL or DTL gates.

Logic Symbol


\section*{Truth Table}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{\begin{tabular}{l}
BINARY \\
STATE
\end{tabular}} & \multicolumn{5}{|c|}{INPUTS} & \multicolumn{9}{|c|}{OUTPUTS} & \multirow[b]{2}{*}{DISPLAY} \\
\hline & \(\overline{L E} \overline{\mathrm{RBI}}\) & A3 & A2 & A1 & AO & \(\bar{a}\) & \(\bar{b}\) & & \(\bar{c}\) & \(\bar{d}\) & \(\bar{\theta}\) & \(\bar{f}\) & \(\overline{\mathrm{g}}\) & \(\overline{\text { RBO }}\) & \\
\hline -- & \(\mathrm{H}^{*}\) & X & \(X\) & X & X & & & & ST & ABL & E & & \(\rightarrow\) & H & STABLE \\
\hline 0 & L L & & L & L & L & H & H & & H & H & H & H & H & L & BLANK \\
\hline 0 & L H & L & L & L & L & L & L & & L & L & L & L & H & H & \(\theta\) \\
\hline 1 & L \(X\) & L & L & L & H & H & L & & L & H & H & H & H & H & ; \\
\hline 2 & \(L X\) & L & L & H & L & L & L & & H & L & L & H & L & H & \(\because\) \\
\hline 3 & \(L \quad X\) & L & L & H & H & L & L & & L & L & H & H & L & H & 3 \\
\hline 4 & \(L X\) & L & H & L & L & H & L & & L & H & H & L & L & H & \(\because\) \\
\hline 5 & \(L X\) & L & H & L & H & L & H & & L & L & H & L & L & H & 5 \\
\hline 6 & L X & & H & H & L & L & & & L & L & L & L & L & H & 6 \\
\hline 7 & \(L \quad X\) & L & H & H & H & L & L & & L & H & H & H & H & H & \(i\) \\
\hline 8 & \(L \quad X\) & H & L & L & L & L & L & & L & L & L & L & L & H & 8 \\
\hline 9 & \(L X\) & H & L & L & H & L & L & & L & H & H & L & L & H & 9 \\
\hline 10 & \(L \quad X\) & H & L & H & L & L & L & & L & H & L & L & L & H & A \\
\hline 11 & \(L X\) & H & L & H & H & H & H & & L & L & L & L & L & H & \(\square\) \\
\hline 12 & \(L X\) & H & H & L & L & L & H & & H & L & L & L & H & H & : \\
\hline 13 & \(L \quad X\) & H & H & L & H & H & L & & L & L & L & H & L & H & 8 \\
\hline 14 & \(L \quad X\) & H & H & H & L & L & H & & H & L & L & L & L & H & \(\varepsilon\) \\
\hline 15 & L X & H & H & H & H & L & H & & H & H & L & L & L & H & \(:\) \\
\hline X & X X & X & X & \(X\) & X & H & H & H & H & H & H & H & H & L** & BLANK \\
\hline
\end{tabular}

TL/F/9797-4

Numerical Designation



\section*{DM9374 7-Segment Decoder/Driver/Latch with Constant Current Sink Outputs}

\section*{General Description}

The '74 is a 7 -segment decoder driver incorporating input latches and output circuits to directly drive common anode LED displays.

\section*{Connection Diagram}

\section*{Logic Symbol}


Order Number DM9374N
See NS Package Number N16E
\begin{tabular}{|l|l|}
\hline \begin{tabular}{c} 
Pin \\
Names
\end{tabular} & \multicolumn{1}{c|}{ Description } \\
\hline A0-A3 & Address (Data Inputs) \\
\(\overline{\mathrm{LE}}\) & Latch Enable Input (Active LOW) \\
\(\overline{\mathrm{RBI}}\) & Ripple Blanking Input (Active LOW) \\
\(\overline{\mathrm{RBO}}\) & Ripple Blanking as Output (Active LOW) \\
& as Input (Active LOW) \\
\(\overline{\mathrm{a}}-\overline{\mathrm{g}}\) & Constant Current Outputs (Active LOW) \\
\hline
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & \multicolumn{2}{|c|}{Parameter} & Min & Nom & Max & Units \\
\hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.75 & 5 & 5.25 & V \\
\hline \multirow[t]{2}{*}{V OUT} & \multirow[t]{2}{*}{Output Voltage Applied} & OFF & & & & V \\
\hline & & ON & & & (Figure A) & \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & V \\
\hline IOH & \multicolumn{2}{|l|}{High Level Output Current, \(\overline{\mathrm{a}}-\overline{\mathrm{g}}, \mathrm{V}_{\text {OUT }}=5.5 \mathrm{~V}\)} & & & 250 & \(\mu \mathrm{A}\) \\
\hline loL & \multicolumn{2}{|l|}{Low Level Output Current, \(\overline{\mathrm{a}}-\overline{\mathrm{g}}, \mathrm{V}_{\mathrm{OL}}=3.0 \mathrm{~V}\)} & 12 & & 18 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline \[
\begin{aligned}
& t_{\mathrm{s}}(\mathrm{H}) \\
& \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
& \hline
\end{aligned}
\] & \multicolumn{2}{|l|}{Setup Time HIGH or LOW An to \(\overline{L E}\)} & \[
\begin{aligned}
& 75 \\
& 30 \\
& \hline
\end{aligned}
\] & & & ns \\
\hline \[
\begin{aligned}
& t_{h}(H) \\
& t_{h}(L) \\
& \hline
\end{aligned}
\] & \multicolumn{2}{|l|}{Hold Time HIGH or LOW An to \(\overline{L E}\)} & \[
\begin{aligned}
& 0 \\
& 0
\end{aligned}
\] & & & ns \\
\hline \(t_{w}(L)\) & \multicolumn{2}{|l|}{LE Pulse Width LOW} & 85 & & & ns \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ
(Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}\) & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\mathrm{Max}, \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}\) & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \(V_{C C}=\) Max, \(V_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline ILL & Low Level Input Current & \(V_{C C}=\) Max, \(V_{1}=0.4 \mathrm{~V}\) & & & -1.6 & mA \\
\hline los & Short Circuit Output Current & \(\mathrm{V}_{C C}=\mathrm{Max}\) (Note 2) & -18 & & -57 & mA \\
\hline ICCH & Supply Current & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IN}}=0 \mathrm{~V}, \\
& \mathrm{~V}_{\mathrm{OUT}}=3.0 \mathrm{~V}
\end{aligned}
\] & & & 50 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{Switching Characteristics}
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for test waveforms and output load)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\[
\begin{aligned}
\mathrm{C}_{\mathrm{L}} & =15 \mathrm{pF} \\
\mathrm{R}_{\mathrm{L}} & =1 \mathrm{k} \Omega
\end{aligned}
\]} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \[
t_{\text {PLH }}
\]
\[
\mathrm{t}_{\mathrm{PHL}}
\] & \begin{tabular}{l}
Propagation Delay \\
An to \(\overline{\mathrm{a}}-\overline{\mathrm{g}}\)
\end{tabular} & & \[
\begin{aligned}
& 140 \\
& 140 \\
& \hline
\end{aligned}
\] & ns \\
\hline \begin{tabular}{l}
\({ }^{\text {tpLH }}\) \\
\(\mathrm{t}_{\mathrm{PHL}}\)
\end{tabular} & Propagation Delay \(\overline{\text { LE }}\) to \(\overline{\mathrm{a}}-\overline{\mathrm{g}}\) & & \[
\begin{aligned}
& 140 \\
& 140 \\
& \hline
\end{aligned}
\] & ns \\
\hline
\end{tabular}


TL/F/10210-9
FIGURE A. Output Voltage Safe Operating Area


TL/F/10210-10
FIGURE B. Typical Constant Segment Current Versus Output Voltage

Another ' 74 feature is the reduced loading on the data inputs when the Latch Enable is HIGH (only \(10 \mu \mathrm{~A}\) typ). This allows many ' 74 s to be driven from a MOS device in multiplex mode without the need for drivers on the data lines. The '74 also provides automatic blanking of the leading and/or trailing-edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an 8 -digit mixed integer fraction decimal representation, using the automatic blanking capability 0060.0300 would be displayed as 60.03 . Leading-edge zero suppression is obtained by connecting the Ripple Blanking Output ( \(\overline{\mathrm{RBO}}\) ) of a decoder to the Ripple Blanking Input ( \(\overline{\mathrm{RBI}})\) of the next lower stage device. The most significant decoder stage should have the \(\overline{\mathrm{RIB}}\) input grounded; and since suppression of the least significant integer zero in a number is not usually desired, the RBI input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing-edge zeroes. The RBO terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL or DTL gates.

\section*{Functional Description}

The '9374 is a 7 -segment decoder/driver with latches on the address inputs and active LOW constant current outputs to drive LEDs directly. This device accepts a 4-bit binary code and produces output drive to the appropriate segments of the 7 -segment display. It has a decode format which produces numeric codes " 0 " through " 9 " and other codes.
Latches on the four data inputs are controlled by an active LOW Latch Enable, \(\overline{L E}\). When \(\overline{L E}\) is LOW, the state of the outputs is determined by the input data. When \(\overline{L E}\) goes HIGH, the last data present at the inputs is stored in the latches and the outputs remain stable. The \(\overline{L E}\) pulse width necessary to accept and store data is typically 50 ns , which allows data to be strobed into the ' 74 at normal TTL speeds. This feature means that data can be routed directly from high speed counters and frequency dividers into the display without slowing down the system clock or providing intermediate data storage.
The latch/decoder combination is a simple system which drives LED displays with multiplexed data inputs from MOS time clocks, DVMs, calculator chips, etc. Data inputs are multiplexed while the displays are in static mode. This lowers component and insertion costs, since several circuitsseven resistors per display, strobe drivers, a separate display voltage source, and clock failure detect circuits-traditionally found in multiplexed display systems are eliminated. It also allows low strobing rates to be used without display flicker.

\section*{Logic Diagram}


\section*{Truth Table}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Binary State} & \multicolumn{6}{|c|}{Inputs} & \multicolumn{8}{|c|}{Outputs} & \multirow[t]{2}{*}{Display} \\
\hline & \(\overline{\text { LE }}\) & RBI & A3 & A2 & A1 & A0 & \(\overline{\mathbf{a}}\) & \(\overline{\text { b }}\) & \(\overline{\mathbf{c}}\) & d & \(\overline{\mathbf{e}}\) & \(\overline{\mathbf{f}}\) & \(\overline{\mathbf{g}}\) & RBO & \\
\hline - & H & * & X & X & X & X & \(\leftarrow\) & & & ABL & & & \(\rightarrow\) & H & Stable \\
\hline 0 & L & L & L & L & L & L & H & H & H & H & H & H & H & L & Blank \\
\hline 0 & L & H & L & L & L & L & L & L & L & L & L & L & H & H & 0 \\
\hline 1 & L & X & L & L & L & H & H & L & L & H & H & H & H & H & 1 \\
\hline 2 & L & X & L & L & H & L & L & L & H & L & L & H & L & H & 2 \\
\hline 3 & L & X & L & L & H & H & L & L & L & L & H & H & L & H & 3 \\
\hline 4 & L & X & L & H & L & L & H & L & L & H & H & L & L & H & 4 \\
\hline 5 & L & X & L & H & L & H & L & H & L & L & H & L & L & H & 5 \\
\hline 6 & L & \(x\) & L & H & H & L & L & H & L & L & L & L & L & H & 6 \\
\hline 7 & L & X & L & H & H & H & L & L & L & H & H & H & H & H & 7 \\
\hline 8 & L & X & H & L & L & L & L & L & L & L & L & L & L & H & 8 \\
\hline 9 & L & X & H & L & L & H & L & L & L & L & H & L & L & H & 9 \\
\hline 10 & L & X & H & L & H & L & H & H & H & H & H & H & L & H & - \\
\hline 11 & L & X & H & L & H & H & L & H & H & L & L & L & L & H & E \\
\hline 12 & L & X & H & H & L & L & H & L & L & H & L & L & L & H & H \\
\hline 13 & L & X & H & H & L & H & H & H & H & L & L & L & H & H & L \\
\hline 14 & L & X & H & H & H & L & L & L & H & H & L & L & L & H & P \\
\hline 15 & L & X & H & H & H & H & H & H & H & H & H & H & H & H & BLANK \\
\hline X & X & X & X & X & X & X & H & H & H & H & H & H & H & L** & BLANK \\
\hline
\end{tabular}

*The \(\overline{\mathrm{RBI}}\) will blank the display only if a binary zero is stored in the latches.
**RBO used as an input overrides all other input conditions.
\(H=\) HIGH Voltage Level
L = LOW Voltage Level
\(X=\) Immaterial

Numerical Designations


\section*{Applications}

It is possible with common anode 7 -segment LED displays and constant current sink decoder drivers to save substantial amounts of power by carefully choosing operating points on display supply voltage. First, examine the power used in the normal display driving method where the display and decoder driver are both operated from a +5.0 V regulated supply ( \(\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{S}}\) ).
The power dissipated by the LED and the driver outputs is ( \(V_{C C} \times I_{\text {seg }} \times n\) Segments). The total power dissipated with a 15 mA LED displaying an eight (8) would be:
\(\mathrm{P}_{\mathrm{TOT}}=5.0 \mathrm{~V} \times 15 \mathrm{~mA} \times 7\)
\(=525 \mathrm{~mW}\)
Of this 525 mW , the power actually required to drive the LED is dependent on the \(\mathrm{V}_{\mathrm{F}}\) drop of each segment. Most GaAsP LEDs exhibit either a 1.7 V or a 3.4 V forward voltage drop. Therefore, the required total power for seven segments would be:
\(P_{(1.7)}=1.7 \mathrm{~V} \times 15 \mathrm{~mA} \times 7\)
\(=178.5 \mathrm{~mW}\)
\(P_{(3.4)}=3.4 \mathrm{~V} \times 15 \mathrm{~mA} \times 7\)
\(=357 \mathrm{~mW}\)
The remaining power is dissipated by the driver outputs which are maintaining the 15 mA constant current required by the LEDs. Most of this power is wasted, since the driver
can maintain approximately 15 mA with as little as 0.5 V across the output device. By using a separate power source ( \(V_{\text {S }}\), Figure \(C\) ) for the LEDs, which is set to the LED V \(\mathrm{V}_{\mathrm{F}}\) plus the offset voltage of the driver, as much as 280 mW can be saved per digit. i.e.,
\(V_{S}=V_{F}(\) Max \()+V_{\text {offset }}\)
\(=2.0 \mathrm{~V}+0.5 \mathrm{~V}\)
\(=2.5 \mathrm{~V}\)
\(\mathrm{P}_{\mathrm{T}}=2.5 \mathrm{~V} \times 14 \mathrm{~mA}\) (from Figure \(B\) ) \(\times 7\)
\(=245 \mathrm{~mW}\)
These figures show that using a separate supply to drive the LEDs can offer significant display power savings. In battery powered equipment, two rechargeable nickle-cadmium cells in series would be sufficient to drive the display, while four such cells would be needed to operate the logic units.
Another method to save power is to apply intensity modulation to the displays (Figure D). It is well known that LED displays are more efficient when operated in pulse mode. There are two reasons: one, the quantum efficiency of the LED material is better; secondly the eye tends to peak detect. Typically a \(20 \%\) off duty cycle to displays (GaAsP) will produce the same brightness as operating under dc conditions.


FIGURE C. Separate Supply for LED Displays


INVERTER CAN BE
IMPLEMENTED WITH
ONE TRANSISTOR AND
A RESISTOR FOR
EACH DECADE
TL/F/10210-6
All Inverters are DTL 9936 or Open Collector TTL 7405

\section*{FIGURE D. Intensity Control by \(\overline{\text { RBO }}\) Pulse Duty Cycle}

Low Power, Low Cost Display Power Sources-In small line operated systems using TTL/MSI and LED or incandescent displays, a significant portion of the total dc power is consumed to drive the displays. Since it is irrelevant whether displays are driven from unfiltered dc or pulsed dc (at fast rates), a dual power system can be used that makes better utilization of transformer rms ratings. The system utilizes a full wave rectified but unsmoothed dc voltage to provide the displays with 120 Hz pulsed power while the reset of the system is driven by a conventional dc power circuit. The frequency of 120 Hz is high enough to avoid display flicker problems. The main advantages of this system are:
- Reduced transformer rating
- Much smaller smoothing capacitor
- Increased LED light output due to pulsed operation

With the standard capacitor filter circuit, the rms current (full wave) loading of the transformer is approximately twice the dc output. Most commercial transformer manufacturers rate transformers with capacitive input filters as follows:
Full Wave Bridge Rectifier Circuit
Transformer rms current \(=1.8 \times\) dc current required
Full Wave Center Tapped Rectifier Circuit
Transformer rms current \(=1.2 \times\) dc current required

Therefore, the removal of a large portion of the filtered dc current requirement (display power) substantially reduces the transformer loading.
There are two basic approaches. First (Figure E) is the direct full wave rectified unregulated supply to power the displays. The '74 decoder driver constant current feature maintains the specified segment current after the LED diode drop and 0.5 V saturation voltage has been reached ( \(\cong 2.2 \mathrm{~V}\) ). Care must be exercised not to exceed the '74 power ratings and the maximum voltage that the decoder driver sees in both the "on" and "off" modes.
The second approach (Figure F) uses a 3-terminal voltage regulator such as the 7805 to provide dc pulsed power to the display with the peak dc voltage limited to +5.0 V . This approach allows easier system thermal management by heat sinking the regulator rather than the display or display drivers. When this power source is used with an intensity modulation scheme or with a multiplexed display system, the frequencies must be chosen such that they do not beat with the 120 Hz full wave rectified power frequency.


TL/F/10210-7
FIGURE E. Direct Unregulated Display Supply


FIGURE F. Pulsed Regulated Display Supply

DM9386 4-Bit Quad Exclusive-NOR with Open-Collector Outputs

\section*{General Description}

The DM9386 consists of four independent Exclusive-NOR gates with open-collector outputs. Single 1-bit comparisons may be made with each gate, or multiple bit comparisons may be made by connecting the outputs of the four gates together. Typical power dissipation is 170 mW . The DM9386 is equivalent to the 8242.

\section*{Connection Diagram}

\section*{Dual-In-Line Package}


TL/F/9798-1
Order Number DM9386N
See NS Package Number N14A
\begin{tabular}{|l|l|}
\hline Pin Names & Description \\
\hline A0, B0 & Gate 0 Inputs \\
A1, B1 & Gate 1 Inputs \\
A2, B2 & Gate 2 Inputs \\
A3, B3 & Gate 3 Inputs \\
O0-O3 & Gate Outputs \\
\hline
\end{tabular}
```

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for availability and specifications.

| Supply Voltage | 7 V |
| :--- | ---: |
| Input Voltage | 5.5 V |
| Operating Free Air Temperature Range |  |
| Commercial | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

```

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c}
\hline Symbol & Parameter & Min & Nom & Max & Units \\
\hline\(V_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline \(\mathrm{IOH}_{\mathrm{OH}}\) & High Level Output Current & -0.150 & & -0.150 & mA \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 25 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics}

Over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & \begin{tabular}{l}
Typ \\
(Note 1)
\end{tabular} & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& V_{C C}=\operatorname{Min}, I_{O H}=\text { Max }, \\
& V_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\] & 2.4 & 3.4 & & V \\
\hline VOL & Low Level Output Voltage & \[
\begin{aligned}
& V_{C C}=\operatorname{Min}, I_{O L}=M a x, \\
& V_{I H}=M \operatorname{Min}
\end{aligned}
\] & & 0.2 & 0.4 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \(V_{C C}=M a x, V_{1}=2.4 V\) & & & 80 & \(\mu \mathrm{A}\) \\
\hline ILL & Low Level Input Current & \(V_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -3.2 & mA \\
\hline los & Short Circuit Output Current & \[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Max} \\
& \text { (Note 2) }
\end{aligned}
\] & -18 & & -57 & mA \\
\hline Icc & Supply Curent & \[
\begin{aligned}
& V_{C C}=M a x, \\
& V_{I N}(A), V_{I N}(B)=0.4 V
\end{aligned}
\] & & & 47.5 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|c|c|c|c|c}
\hline Symbol & Parameter & Condltions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{c}
\(\mathrm{C}_{\mathrm{L}}=30 \mathrm{pF}\) \\
\(\mathrm{R}_{\mathrm{L}}=530 \Omega\)
\end{tabular} & 25 & ns \\
\hline \(\mathrm{t}_{\mathrm{PHL}}\) & \begin{tabular}{l} 
Propagation Delay Time \\
High to Low Level Output
\end{tabular} & & 25 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.


Truth Table
\begin{tabular}{|c|c|c|}
\hline \multicolumn{2}{|c|}{ Inputs } & Output \\
\hline An & Bn & On \\
\hline L & L & H \\
H & L & L \\
L & \(H\) & L \\
H & \(H\) & \(H\) \\
\hline
\end{tabular}
\(H=\) HIGH Voltage Level
L = LOW Voltage Level

TL/F/9798-2
\(V_{C C}=\operatorname{Pin} 14\)
\(\mathrm{GND}=\operatorname{Pin} 7\)

\section*{Logic Diagram}


TL/F/9798-3

\section*{9601/DM9601 Retriggerable One Shot}

\section*{General Description}

These retriggerable one shots provide the designer with four inputs; two active high and two active low. This permits a choice of either leading-edge or trailing-edge triggering, independent of input transition times. When input conditons for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge again. The retriggerable feature allows for output pulse widths to be expanded. In fact a continuous true output can be maintained by having an input cycle time which is shorter than the output cycle time. Retriggering may be inhibited by tying the \(\bar{Q}\) output to an active low input.

\section*{Features}

■ High speed operation-input repetition rate \(>10 \mathrm{MHz}\)
- Flexibility of operation-optional retriggering/lock-out capability
- Output pulse width range- 50 ns to \(\infty\)
- Leading or trailing edge triggering
- Complementary outputs/inputs
- Input clamping diodes
- DTL/TTL compatible logic levels
- Alternate Military/Aerospace device (9601) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Connection Diagram}


Order Number 9601DMQB, 9601FMQB, DM9601J, DM9601W or DM9601N
See NS Package Number J14A, N14A or W14B

\section*{Function Table}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multicolumn{4}{|c|}{Inputs} & \multicolumn{2}{|l|}{Outputs} & \multirow[b]{3}{*}{\(\mathrm{H}=\) High Logic Level} \\
\hline A1 & A2 & B1 & B2 & Q & \(\overline{\mathbf{Q}}\) & \\
\hline H & H & X & X & L & H & \\
\hline x & X & L & X & L & H & L = Low Logic Level \\
\hline X & X & X & L & L & H & \[
\begin{array}{ll}
X= & \text { Either Low or } \\
& \text { High Logic Level }
\end{array}
\] \\
\hline L & \(x\) & H & H & L & H & \(\uparrow=\) Low to High Level \\
\hline L & \(x\) & \(\uparrow\) & H & \(\Omega\) & 工 & Transition \\
\hline L & X & H & \(\uparrow\) & \(\Omega\) & U & \(\downarrow=\) High to Low Level \\
\hline X & L & H & H & L & H & Transition \\
\hline X & L & \(\uparrow\) & H & \(\Omega\) & Ч & \(\Omega\) = Positive Pulse \\
\hline X & L & H & \(\uparrow\) & \(\Omega\) & Ч & U = Negative Pulse \\
\hline H & \(\downarrow\) & H & H & \(\Omega\) & Ч & \\
\hline \(\downarrow\) & \(\downarrow\) & H & H & \(\Omega\) & & \\
\hline \(\downarrow\) & H & H & H & \(\Omega\) & 凹 & \\
\hline
\end{tabular}
\begin{tabular}{lr} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
年lease contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
Military & \(0^{\circ}\) to \(+70^{\circ} \mathrm{C}\) \\
Commercial & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{Milltary} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & Min & Nom & Max & \\
\hline Vcc & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \multirow[t]{5}{*}{\(\mathrm{V}_{\mathrm{IH}}\)} & \multirow[t]{5}{*}{High Level Input Voltage} & \(\mathrm{T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}\) & 2 & & & & & & \multirow{5}{*}{V} \\
\hline & & \(\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}\) & & & & 1.9 & & & \\
\hline & & \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) & 1.7 & & & 1.8 & & & \\
\hline & & \(\mathrm{T}_{\mathrm{A}}=75^{\circ} \mathrm{C}\) & & & & 1.6 & & & \\
\hline & & \(\mathrm{T}_{\mathrm{A}}=125^{\circ} \mathrm{C}\) & 1.5 & & & & & & \\
\hline \multirow[t]{5}{*}{\(\mathrm{V}_{\text {IL }}\)} & \multirow[t]{5}{*}{Low Level Input Voltage} & \(\mathrm{T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}\) & & & 0.85 & & & & \multirow{5}{*}{V} \\
\hline & & \(\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}\) & & & & & & 0.85 & \\
\hline & & \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) & & & 0.9 & & & 0.85 & \\
\hline & & \(\mathrm{T}_{\mathrm{A}}=75^{\circ} \mathrm{C}\) & & & & & & 0.85 & \\
\hline & & \(\mathrm{T}_{\mathrm{A}}=125^{\circ} \mathrm{C}\) & & & 0.85 & & & & \\
\hline lOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.72 & & & -0.96 & mA \\
\hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 10 & & & 12.8 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions (Note 3)} & Min & Typ (Note 1) & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min}, \mathrm{IOH}_{\mathrm{O}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min},(\text { Note } 4)
\end{aligned}
\]} & 2.4 & & & V \\
\hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\text { Min } \\
& \text { (Note 4) }
\end{aligned}
\]} & MIL & & & 0.4 & \multirow[b]{2}{*}{V} \\
\hline & & & COM & & & 0.45 & \\
\hline \({ }_{1 / H}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=4.5 \mathrm{~V}\)} & & & 60 & \(\mu \mathrm{A}\) \\
\hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\(V_{C C}=\operatorname{Max}\)} & MIL \(\mathrm{V}_{\text {IN }}=0.40 \mathrm{~V}\) & & & -1.6 & \multirow[t]{2}{*}{mA} \\
\hline & & & COM \(\mathrm{V}_{\mathrm{IN}}=0.45 \mathrm{~V}\) & & & -1.6 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C C}=M a x
\] \\
(Notes 2 and 4)
\end{tabular}} & MIL & -10 & & -40 & \multirow[t]{2}{*}{mA} \\
\hline & & & COM & -10 & & -40 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x\)} & & & 25 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: Unless otherwise noted, \(\mathrm{R}_{\mathrm{X}}=10 \mathrm{k}\) between PIN 13 and \(\mathrm{V}_{\mathrm{CC}}\) on all tests.
Note 4: Ground PIN 11 for \(V_{O L}\) test on PIN 6, \(V_{O H}\) and los tests on PIN 8. Open PIN 11 for \(V_{O L}\) test on PIN 8, \(V_{O H}\) and los tests on PIN 6.

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \begin{tabular}{l}
From (Input) \\
To (Output)
\end{tabular} & Conditions & Min & Max & Units \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \begin{tabular}{l}
Negative Trigger Input to \\
True Output
\end{tabular} & \multirow[t]{3}{*}{\[
\begin{aligned}
& C_{L}=15 \mathrm{pF} \\
& C_{X}=0 \\
& R_{X}=5 \mathrm{k} \Omega
\end{aligned}
\]} & & 40 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \multirow[t]{6}{*}{Negative Trigger Input to Complement Output} & & & 40 & ns \\
\hline \(t_{\text {PW(MIN }}\) ) & Minimum True Output Pulse Width & & & & 65 & ns \\
\hline tpW & Pulse Width & & \[
\begin{aligned}
& \mathrm{RX}_{\mathrm{X}}=10 \mathrm{k} \Omega \\
& \mathrm{C}_{\mathrm{X}}=1000 \mathrm{pF}
\end{aligned}
\] & 3.08 & 3.76 & \(\mu \mathrm{s}\) \\
\hline \(\mathrm{C}_{\text {StRAY }}\) & Maximum Allowable Wiring Capacitance & & Pin 13 to GND & & 50 & pF \\
\hline \(\mathrm{R}_{\mathrm{X}}\) & External Timing Resistor & & DM96 & & 25 & \(\mathrm{k} \Omega\) \\
\hline \(\mathrm{R}_{\mathrm{X}}\) & External Timing Resistor & & DM86 & & 50 & \(\mathrm{k} \Omega\) \\
\hline
\end{tabular}

\section*{Operating Rules}
1. An external resistor \(R_{X}\) and an external capacitor \(C_{X}\) are required for operation. The value of \(R_{X}\) can vary between the limits shown in switching characteristics. The value of \(C_{X}\) is optional and may be adjusted to achieve the required output pulse width.
2. Output pulse width tpw may be calculated as follows:
\(t_{P W}=K R_{X} C_{X}\left[1+\frac{0.7}{R_{X}}\right]_{K \approx 0.34}^{\left(\text {for } C_{X}>10^{3} p F\right)}\)
\(R_{X}\) in \(k \Omega, C_{X}\) in \(p F\) and \(t_{P W}\) in \(n s\).
(For \(\mathrm{C}_{\mathrm{X}}<10^{3} \mathrm{pF}\), see curve.)
3. \(R_{X}\) and \(C_{X}\) must be kept as close as possible to the circuit in order to minimize stray capacitance and noise pickup. If remote trimming is required, \(\mathrm{R}_{\mathrm{X}}\) may be split up such that at least \(\mathrm{RX}_{\mathrm{X}(\mathrm{MIN})}\) must be as close as possible to the circuit and the remote portion of the trimming resistor \(R<R_{X(M A X)}-R_{X}\).
4. Set-up time \(\left(\mathrm{t}_{1}\right)\) for input trigger pulse must be \(>40 \mathrm{~ns}\). (See Figure 1).
Release time ( \(\mathrm{t}_{2}\) ) for input trigger pulse must be \(>40 \mathrm{~ns}\). (See Figure 2).


TL/F/6610-2
FIGURE 1


TL/F/6610-3
FIGURE 2
5. Retrigger pulse width (see Figure 3) is calculated as follows:
\[
t_{W}=t_{P W}+t_{P L H}=K R_{X} C_{X}\left[1+\frac{0.7}{R_{X}}\right]+t_{P L H}
\]


TL/F/6610-4
FIGURE 3
Typical "K" Coefficient Variation vs Timing Capacitance The multiplicative factor " \(K\) " varies as a function of the timing capacitor, \(\mathrm{C}_{\mathrm{X}}\). The graph below details this characteristic:


TL/F/6610-5
*For further detailed device characteristics and output performance, please refer to the NSC one-shot application note, AN-366.

\section*{Typical Performance Characteristics}


Normalized Output
Pulse Width vs


Normalized Output
Pulse Width vs Ambient
Temperature


Pulse Width vs Timing Resistance


Output Pulse Width vs Ambient Temperature


TL/F/6610-6
Schematic Diagram


TL/F/6610-7

\section*{National Semiconductor \\ 9602/DM9602 Dual Retriggerable, Resettable One Shots}

\section*{General Description}

These dual resettable, retriggerable one shots have two inputs per function; one which is active high, and one which is active low. This allows the designer to employ either lead-ing-edge or trailing-edge triggering, which is independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is allowed to rapidly discharge and then charge again. The retriggerable feature permits output pulse widths to be extended. In fact a continuous true output can be maintained by having an input cycle time which is shorter than the output cycle time. The output pulse may then be terminated at any time by applying a low logic level to the RESET pin. Retriggering may be inhibited by either connecting the \(Q\) output to an active high input, or the \(\bar{Q}\) output to an active low input.

\section*{Features}
n 70 ns to \(\infty\) output width range
. Resettable and retriggerable-0\% to 100\% duty cycle
- TTL input gating-leading or trailing edge triggering
- Complementary TTL outputs
- Optional retrigger lock-out capability
- Pulse width compensated for \(\mathrm{V}_{\mathrm{CC}}\) and temperature variations
- Alternate Military/Aerospace device (54xxx) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

\section*{Connection Diagram}


TL/F/6611-1
Order Number 9602DMQB, 9602FMQB or DM9602N
See NS Package Number J16A, N16E or W16A
Function Table
\begin{tabular}{|c|c|c|c|}
\hline \multicolumn{3}{|c|}{ Pin No's. } & \multirow{2}{*}{ Operation } \\
\cline { 1 - 3 } \(\mathbf{A}\) & B & CLR & \\
\hline\(H \rightarrow\) L & L & \(H\) & Trigger \\
\(H\) & \(L \rightarrow H\) & \(H\) & Trigger \\
\(X\) & \(X\) & L & Reset \\
\hline
\end{tabular}

\footnotetext{
\(H=\) High Voltage Level
\(\mathrm{L}=\) Low Voltage Level
X = Don't Care
}

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
7 V
Input Voltage 5.5 V

Operating Free Air Temperature Range
Military
\(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
Commercial
\(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
Storage Temperature Range
\(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \multirow[t]{5}{*}{\(\mathrm{V}_{\mathrm{IH}}\)} & \multirow[t]{5}{*}{High Level Input Voltage} & \(\mathrm{T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}\) & 2 & & & & & & \multirow{5}{*}{V} \\
\hline & & \(\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}\) & & & & 1.9 & & & \\
\hline & & \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) & 1.7 & & & 1.8 & & & \\
\hline & & \(\mathrm{T}_{\mathrm{A}}=75^{\circ} \mathrm{C}\) & & & & 1.65 & & & \\
\hline & & \(\mathrm{T}_{\mathrm{A}}=125^{\circ} \mathrm{C}\) & 1.5 & & & & & & \\
\hline \multirow[t]{5}{*}{\(\mathrm{V}_{\mathrm{IL}}\)} & \multirow[t]{5}{*}{Low Level Input Voltage} & \(\mathrm{T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}\) & & & 0.85 & & & & \multirow{5}{*}{V} \\
\hline & & \(\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}\) & & & & & & 0.85 & \\
\hline & & \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) & & & 0.9 & & & 0.85 & \\
\hline & & \(\mathrm{T}_{\mathrm{A}}=75^{\circ} \mathrm{C}\) & & & & & & 0.85 & \\
\hline & & \(\mathrm{T}_{\mathrm{A}}=125^{\circ} \mathrm{C}\) & & & 0.85 & & & & \\
\hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.8 & & & -0.8 & mA \\
\hline loL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions (Note 3)} & Min & Typ (Note 1) & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{l}}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \\
& \text { (Note 4) }
\end{aligned}
\]} & 2.4 & & & V \\
\hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min} \\
& \text { (Note 4) }
\end{aligned}
\]} & MIL & & & 0.4 & \multirow[b]{2}{*}{V} \\
\hline & & & COM & & & 0.45 & \\
\hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=4.5 \mathrm{~V}\)} & & & 60 & \(\mu \mathrm{A}\) \\
\hline \multirow[t]{4}{*}{IIL} & \multirow[t]{4}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\(V_{C C}=\) Max} & \(\mathrm{MIL} \mathrm{V}_{1}=0.40 \mathrm{~V}\) & & & -1.6 & \multirow{4}{*}{mA} \\
\hline & & & COM \(\mathrm{V}_{1}=0.45 \mathrm{~V}\) & & & -1.6 & \\
\hline & & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}\)} & MIL \(\mathrm{V}_{1}=0.40 \mathrm{~V}\) & & & -1.24 & \\
\hline & & & COM \(\mathrm{V}_{1}=0.45 \mathrm{~V}\) & & & -1.41 & \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x, V_{O U T}=1 V \\
& (\text { Notes } 2 \text { and } 4)
\end{aligned}
\]} & MIL & & & -25 & \multirow[b]{2}{*}{mA} \\
\hline & & & COM & & & -35 & \\
\hline \multirow[t]{2}{*}{Icc} & \multirow[t]{2}{*}{Supply Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{C C}=\mathrm{Max}\)} & MIL & & 39 & 45 & \multirow{2}{*}{mA} \\
\hline & & & COM & & 39 & 50 & \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: Unless otherwise noted, \(\mathrm{R}_{\mathrm{X}}=10 \mathrm{k}\) for all tests.
Note 4: Ground PIN 1(15) for \(\mathrm{V}_{\mathrm{OL}}\) on PIN 7(9) or \(\mathrm{V}_{\mathrm{OH}}\) and \(\mathrm{l}_{\mathrm{OS}}\) on PIN 6(10) and apply momentary ground to PIN 4(12). Open PIN 1(15) for \(\mathrm{V}_{\mathrm{OL}}\) on PIN 6(10) or \(\mathrm{V}_{\mathrm{OH}}\) and los on PIN 7(9).
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Parameter}} & \multirow[t]{2}{*}{Conditions} & \multicolumn{2}{|c|}{Military} & \multicolumn{2}{|l|}{Commercial} & \multirow[t]{2}{*}{Units} \\
\hline & & & & Min & Max & Min & Max & \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time, Low-to-High Level Output & Negative Trigger Input to True Output & \multirow{4}{*}{\[
\begin{aligned}
& \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\
& \mathrm{C}_{\mathrm{X}}=0 \\
& \mathrm{R}_{\mathrm{X}}=5 \mathrm{k} \Omega
\end{aligned}
\]} & & 35 & & 40 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time, High-to-Low Level Output & Negative Trigger Input To Complement Output & & & 43 & & 48 & ns \\
\hline \multirow[t]{2}{*}{\(t_{\text {PWW }}\) (MIN)} & Minimum True Output Pulse Width & & & & 90 & & 100 & \multirow[b]{2}{*}{ns} \\
\hline & Minimum Complement Pulse Width & & & & 100 & & 110 & \\
\hline tpW & Pulse Width & & \[
\begin{aligned}
& \mathrm{RXX}_{\mathrm{X}}=10 \mathrm{k} \Omega \\
& \mathrm{C}_{\mathrm{X}}=1000 \mathrm{pF} \\
& \hline
\end{aligned}
\] & 3.08 & 3.76 & 3.08 & 3.76 & \(\mu \mathrm{S}\) \\
\hline Cstray & Maximum Allowable Wiring Capacitance & & Pins 2, 14 to GND & & 50 & & 50 & pF \\
\hline \(\mathrm{R}_{\mathrm{X}}\) & External Timing Resistor & & & 5 & 25 & 5 & 50 & k \(\Omega\) \\
\hline
\end{tabular}

\section*{Logic Diagrams}


TL/F/6611-2

\section*{Operating Rules}
1. An external resistor ( \(R_{X}\) ) and external capacitor ( \(C_{X}\) ) are required as shown in the Logic Diagram.
2. The value of \(C_{X}\) may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching \(3.0 \mu \mathrm{~A}\) or if stray capacitance from either terminal to ground is more than 50 pF , the timing equations may not represent the pulse width obtained.
3. The output pulse with ( t ) is defined as follows:
\[
t=K R_{X} C_{X}\left[1+\frac{1}{R_{X}}\right] \quad \begin{aligned}
& \text { for } C_{X}>10^{3} \mathrm{pF} \\
& K \approx 0.34
\end{aligned}
\]
where: \(\quad R_{X}\) is in \(k \Omega, C_{X}\) is in \(p F\)
\(t\) is in ns
for \(\mathrm{C}_{\mathrm{X}}<10^{3} \mathrm{pF}\), see Figure 1.
for \(K\) vs \(C_{X}\) see Figure 6.


TL/F/6611-3

4. If electrolytic type capacitors are to be used, the following three configurations are recommended:
A. Use with low leakage capacitors:

The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 V is less than \(3 \mu \mathrm{~A}\), and the inverse capacitor leakage at 1.0 V is less than \(5 \mu \mathrm{~A}\) over the operational temperature range.

B. Use with high inverse leakage current electrolytic capacitors:
The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor. The use of this configuration is not recommended with retriggerable operation.

(14)


TL/F/6611-5
C. Use to obtain extended pulse widths:

This configuration can be used to obtain extended pulse widths, because of the larger timing resistor allowed by beta multiplication. Electrolytics with high inverse leakage currents can be used.
\(R<R_{X}(0.7)\left(h_{F E}\right.\) Q1) or \(<2.5 \mathrm{M} \Omega\), whichever is the lesser
\(R_{X}(\min )<R_{Y}<R_{X}\) (max)
( \(5 \mathrm{k} \Omega \leq R_{Y} \leq 10 \mathrm{k} \Omega\) is recommended)
Q1: NPN silicon transistor with \(h_{\text {FE }}\) requirements of above equations, such as 2N5961 or 2N5962.


TL/F/6611-6
This configuration is not recommended with retriggerable operation.
5. To obtain variable pulse width by remote trimming, the following circuit is recommended:


TL/F/6611-7
6. Under any operating condition, \(\mathrm{C}_{X}\) and \(\mathrm{R}_{X}(\mathrm{~min})\) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
7. Input Trigger Pulse Rules (See Triggering Truth Table)


TL/F/6611-8
Input to \(\operatorname{Pin} 5(11)\),
\[
(\operatorname{Pin} 3(13)=H I G H)
\]

Pin 4(12) \(=\) LOW
\(t_{1}, t_{3}=\) Min. Positive Input Pulse Width \(>40 \mathrm{~ns}\)
\(\mathrm{t}_{2}, \mathrm{t}_{4}=\) Min. Negative Input Pulse Width \(>40 \mathrm{~ns}\)


TL/F/6611-9
Input to Pin 4(12)
\((\operatorname{Pin} 3(13)=\mathrm{HIGH})\)
Pin 5(11) \(=\mathrm{HIGH}\)
8. The retriggerable pulse width is calculated as shown below:
\(t_{W}=t+t_{P L H}=K R_{X} C_{X}\left(1+\frac{1}{R_{X}}\right)+t_{P L H}\)


The retrigger pulse width is equal to the pulse width (t) plus a delay time. For pulse widths greater than \(500 \mathrm{~ns}, \mathrm{t}_{\mathrm{w}}\) can be approximated as t . Retriggering will not occur if the retrigger pulse comes within \(\approx 0.3 \mathrm{C}_{\mathrm{X}}\) (ns) after the initial trigger pulse (i.e., during the discharge cycle).
9. Reset Operation-An overriding clear (active LOW level) is provided on each one shot. By applying a LOW to the reset, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW.

10. \(\mathrm{V}_{\mathrm{CC}}\) and Ground wiring should conform to good high frequency standards so that switching transients on \(V_{C C}\) and Ground leads do not cause interaction between one shots. Use of a 0.01 to \(0.1 \mu \mathrm{~F}\) bypass capacitor between \(\mathrm{V}_{\mathrm{CC}}\) and Ground located near the DM9602 is recommended.
*For further detailed device characteristics and output performance, please refer to the NSC one-shot application note, AN-366.


FIGURE 1. Output Pulse Width vs Timing Resistance and Capacitance for \(\mathrm{C}_{\mathrm{X}}<10^{3} \mathrm{pF}\)


TL/F/6611-14
FIGURE 3. Pulse Width vs Timing Resistor


TL/F/6611-16
FIGURE 5. Minimum Output Pulse Width vs Ambient Temperature


TL/F/6611-13
FIGURE 2. Normalized Output Pulse Width vs Ambient Temperature


TL/F/6611-15
FIGURE 4. Normalized Output Pulse Width vs Supply Voltage


FIGURE 6. Typical "K" Coefficient Variation vs Timing Capacitance

\section*{DM96101}

\section*{Quad 2-Input Positive NAND Buffer with Open-Collector Output}

\section*{General Description}

The DM96101 is similar to the \(54 / 7439\), except that the outputs are specified at three levels of lol; in the HIGH state the \(\mathrm{l}_{\mathrm{OH}}\) current is specified at two levels of \(\mathrm{V}_{\mathrm{OH}}\). During switching transitions, output current change rate is typically \(4.0 \mathrm{~mA} / \mathrm{ns}\).

\section*{Connection Diagram}

\begin{tabular}{l} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage \\
Input Voltage \\
Operating Free Air Temperature Range \\
Storage Temperature Range \\
\hline
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{c|l|c|c|c|c}
\hline Symbol & Parameter & Min & Nom & Max & Units \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
\hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -0.05 & mA \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 16 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics}

Over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
(Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-12 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline VOH & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOH}_{\mathrm{O}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=M i n \\
& V_{\mathbb{I H}}=V_{I N}
\end{aligned}
\]} & \(\mathrm{l}_{\mathrm{OL}}=48 \mathrm{~mA}\) & & & 0.4 & \multirow{3}{*}{V} \\
\hline & & & \(\mathrm{lOL}=60 \mathrm{~mA}\) & & & 0.5 & \\
\hline & & & \(\mathrm{loL}=80 \mathrm{~mA}\) & & & 0.6 & \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{2}{*}{\(\mathrm{I}_{\mathrm{H}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\(V_{C C}=\operatorname{Max}\)} & \(\mathrm{V}_{\mathrm{IN}}=2.4 \mathrm{~V}\) & & & 40 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & \(\mathrm{V}_{\mathrm{IN}}=5.5 \mathrm{~V}\) & & & 1000 & \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{IN}}=0.4 \mathrm{~V}\)} & & & -1.6 & mA \\
\hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\text { Max } \\
& \text { (Note 2) }
\end{aligned}
\]} & -18 & & -57 & mA \\
\hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{I N}=0 V\)} & & & 8.5 & mA \\
\hline \(\mathrm{I}_{\mathrm{CCL}}\) & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{\text {IN }}=\) Open} & & & 54 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|c|c|c|c|c}
\hline Symbol & \multicolumn{1}{|c|}{ Parameter } & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{l}
\(C_{L}=45 \mathrm{pF}\) \\
\(R_{L}=120 \Omega\)
\end{tabular} & 22 & ns \\
\cline { 1 - 1 } & & & & 25 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

Section 5
TTL - Low Power
Section 5—TTL - Low Power
TTL (Low Power)-Mil/Aero
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\section*{DM54L00}

\section*{Quad 2-Input NAND Gates}

\section*{General Description}

This device contains four independent gates each of which performs the logic NAND function.

Connection Diagram


Order Number DM54L00J or DM54L00W
See NS Package Number J14A or W14B

\section*{Function Table}
\begin{tabular}{|c|c|c|}
\hline \multicolumn{3}{c|}{\(\mathbf{Y}=\overline{\mathbf{A B}}\)} \\
\hline \multicolumn{2}{|c|}{ Inputs } & Output \\
\hline A & B & Y \\
\hline L & L & H \\
L & H & H \\
H & L & H \\
H & H & L \\
\hline
\end{tabular}
\(\mathrm{H}=\) High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avaliability and specifications.
Supply Voltage
8V
Input Voltage
5.5 V

Operating Free Air Temperature Range
\(\begin{array}{ll}\text { DM57L } & -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\ \text { Storage Temperature Range } & -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C}\end{array}\)

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{c|c|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multirow{2}{|c|}{ Parameter } & \multicolumn{2}{c|}{ DM54L00 } & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.7 & V \\
\hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -0.2 & mA \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 2 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ
(Note 1) & Max & Units \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Ouput Voltage & \[
\begin{aligned}
& V_{C C}=\operatorname{Min}, I_{O H}=M a x \\
& V_{I L}=M a x
\end{aligned}
\] & 2.4 & 3.3 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\] & & 0.15 & 0.3 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 0.1 & mA \\
\hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=2.4 \mathrm{~V}\) & & & 10 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=0.3 \mathrm{~V}\) & & & -0.18 & mA \\
\hline los & Short Circuit Output Current & \[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Max} \\
& \text { (Note 2) }
\end{aligned}
\] & -3 & & -15 & mA \\
\hline ICCH & Supply Current with Outputs High & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) & & 0.44 & 0.8 & mA \\
\hline \(\mathrm{I}_{\text {CCL }}\) & Supply Current with Outputs Low & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) & & 1.16 & 2.04 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one should be shorted at a time.
Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|l|c|c|c|c}
\hline Symbol & \multicolumn{1}{|c|}{ Parameter } & Conditions & Min & Max & Units \\
\hline \(\mathrm{t}_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay \\
Low to High Level Output
\end{tabular} & \begin{tabular}{l}
\(R_{L}=4 \mathrm{k} \Omega\) \\
\(C_{L}=50 \mathrm{pF}\)
\end{tabular} & 60 & ns \\
\cline { 1 - 1 } & & & 60 & ns \\
\hline
\end{tabular}

\section*{DM54L02 Quad 2-Input NOR Gates}

\section*{General Description}

This device contains four independent gates each of which performs the logic NOR function.

\section*{Connection Diagram}


Function Table
\begin{tabular}{|c|c|c|}
\multicolumn{3}{c|}{\(\mathbf{Y}=\overline{\mathbf{A}+\mathbf{B}}\)} \\
\hline \multicolumn{2}{|c|}{ Inputs } & Output \\
\hline \(\mathbf{A}\) & \(\mathbf{B}\) & \(\mathbf{Y}\) \\
\hline L & L & \(H\) \\
L & \(H\) & L \\
\(H\) & L & L \\
\(H\) & \(H\) & L \\
\hline
\end{tabular}
\(H=\) High Logic Level
\(L=\) Low Logic Level

\footnotetext{
Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
5.5 V

Operating Free Air Temperature Range
\begin{tabular}{cl} 
DM54L & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}
}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{c|c|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multirow{2}{|c|}{ Parameter } & \multicolumn{2}{|c|}{ DM54L02 } & \multirow{2}{*}{ Units } \\
\cline { 3 - 5 } & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.7 & V \\
\hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -0.2 & mA \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 2 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ
(Note 1) & Max & Units \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & 2.4 & 3.3 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}_{\mathrm{OL}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\] & & 0.15 & 0.3 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=5.5 \mathrm{~V}\) & & & 0.1 & mA \\
\hline \(\mathrm{I}_{\mathrm{IH}}\) & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 10 & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{I}_{\text {IL }}\) & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.3 \mathrm{~V}\) & & & -0.18 & mA \\
\hline los & Short Circuit Output Current & \[
\begin{aligned}
& V_{\mathrm{CC}}=M a x \\
& \text { (Note 2) } \\
& \hline
\end{aligned}
\] & -3 & & -15 & mA \\
\hline \(\mathrm{I}_{\mathrm{CCH}}\) & Supply Current with Outputs High & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) & & 0.8 & 1.6 & mA \\
\hline \(\mathrm{I}_{\text {CCL }}\) & Supply Current with Outputs Low & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) & & 1.4 & 2.6 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|c|c|c|c|c}
\hline Symbol & \multicolumn{1}{|c|}{ Parameter } & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{l}
\(R_{L}=4 \mathrm{k} \Omega\) \\
\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)
\end{tabular} & 60 & ns \\
\hline tPHL & \begin{tabular}{l} 
Propagation Delay Time \\
High to Low Level Output
\end{tabular} & & & 60 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{DM54L04 Hex Inverting Gate}

\section*{General Description}

This device contains six independent gates each of which performs the logic INVERT function.

\section*{Connection Diagram}


Function Table
\begin{tabular}{|c|c|}
\hline Input & Output \\
\hline \(\mathbf{A}\) & \(\mathbf{Y}\) \\
\hline L & \(H\) \\
\(H\) & L \\
\hline
\end{tabular}

\footnotetext{
\(H=\) High Logic Level
\(L=\) Low Logic Level
}

\section*{Absolute Maximum Ratings (Note)}

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
5.5 V

Operating Free Air Temperature Range
DM54L \(\quad-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
Storage Temperature Range \(\quad-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multirow{2}{|c|}{ Parameter } & \multicolumn{2}{c|}{ DM54L04 } & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & Nom & Max & \\
\hline\(V_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.7 & V \\
\hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -0.2 & mA \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 2 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ (Note 1) & Max & Units \\
\hline V OH & High Level Output Voltage & \[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOH}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & 2.4 & 3.3 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min} \\
& \mathrm{IOL}_{\mathrm{OL}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\] & & 0.15 & 0.3 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 0.1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 10 & \(\mu \mathrm{A}\) \\
\hline \(1 / 2\) & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.3 \mathrm{~V}\) & & & -0.18 & mA \\
\hline los & Short Circuit Output Current & \[
\begin{aligned}
& V_{\mathrm{CC}}=\text { Max } \\
& \text { (Note 2) } \\
& \hline
\end{aligned}
\] & -3 & & -15 & mA \\
\hline ICCH & Supply Current with Outputs High & \(\mathrm{V}_{\mathrm{CC}}=\) Max & & 0.6 & 1.2 & mA \\
\hline ICCL & Supply Current with Outputs Low & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) & & 1.7 & 3.06 & mA \\
\hline
\end{tabular}

Switching CharacteristicS at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Max & Units \\
\hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{R}_{\mathrm{L}}=4 \mathrm{k} \Omega \\
& \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}
\end{aligned}
\]} & & 60 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & & & 60 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{DM54L10}

\section*{Triple 3-Input NAND Gates}

\section*{General Description}

This device contains three independent gates each of which performs the logic NAND function.

\section*{Connection Diagram}

\section*{Dual-In-Line Package}


TL/F/6619-1
Order Number DM54L10J or DM54L10W See NS Package Number J14A or W14B

\section*{Function Table}
\[
\mathbf{Y}=\overline{\mathbf{A B C}}
\]
\begin{tabular}{|c|c|c|c|}
\hline \multicolumn{3}{|c|}{ Inputs } & Output \\
\hline A & B & C & Y \\
\hline\(X\) & \(X\) & L & H \\
X & L & \(X\) & \(H\) \\
L & X & X & H \\
\(H\) & \(H\) & \(H\) & L \\
\hline
\end{tabular}
\(H=\) High Logic Level
L = Low Logic Level
\(X=\) Either Low or High Logic Level

\section*{Absolute Maximum Ratings (Note) \\ If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. \\ Supply Voltage \\ Input Voltage \\ Operating Free Air Temperature Range \\ DM54L \\ \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\ Storage Temperature Range \\ \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multirow{2}{*}{ Parameter } & \multicolumn{2}{c|}{ DM54L10 } & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & Nom & Max & \\
\hline\(V_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.7 & V \\
\hline IOH & High Level Output Current & & & -0.2 & mA \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 2 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ
(Note 1) & Max & Units \\
\hline V OH & High Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & 2.4 & 3.3 & & V \\
\hline VOL & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{lOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\] & & 0.15 & 0.3 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 0.1 & mA \\
\hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=2.4 \mathrm{~V}\) & & & 10 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=0.3 \mathrm{~V}\) & & & -0.18 & mA \\
\hline los & Short Circuit Output Current & \[
\begin{aligned}
& V_{C C}=\text { Max } \\
& \text { (Note 2) }
\end{aligned}
\] & -3 & & -15 & mA \\
\hline ICCH & Supply Current with Outputs High & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) & & 0.33 & 0.6 & mA \\
\hline ICCL & Supply Current with Outputs Low & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) & & 0.87 & 1.53 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{c|c|c|c|c|c}
\hline Symbol & \multicolumn{1}{c}{ Parameter } & Conditions & Min & Max & Units \\
\hline\(t_{\text {PLH }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
Low to High Level Output
\end{tabular} & \begin{tabular}{c}
\(R_{L}=4 \mathrm{k} \Omega\), \\
\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)
\end{tabular} & & 60 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & \begin{tabular}{l} 
Propagation Delay Time \\
High to Low Level Output
\end{tabular} & & 60 & ns \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.

\section*{National Semiconductor}

\section*{DM54L72 AND-Gated Master-Slave J-K Flip-Flop with Preset, Clear and Complementary Outputs}

\section*{General Description}

This device contains a positive pulse triggered master-slave J-K flip-flop with complementary outputs. Multiple J and K inputs are ANDed together to produce the internal \(J\) and \(K\) function for the flip-flop. The J and K data is processed by the flip-flop after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the AND gates is transferred to the master. While the clock is high the AND gate
inputs are disabled. On the negative transition of the clock the data from the master is transferred to the slave. The logic state of the \(J\) and \(K\) inputs must not be allowed to change while the clock is in the high state. Data is transferred to the outputs on the falling edge of the clock pulse. A low logic level on the preset or clear inputs sets or resets the outputs regardless of the logic levels of the other inputs.

\section*{Connection Diagram}

Dual-In-Line Package


Order Number DM54L72J or DM54L72W
See NS Package Number J14A or W14B

Function Table
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multicolumn{5}{|c|}{Inputs} & Outputs \\
\hline PR & CLR & CLK & (Note 1) & \[
\begin{gathered}
\text { K } \\
\text { (Note 1) }
\end{gathered}
\] & Q \(\overline{\mathbf{Q}}\) \\
\hline L & H & X & X & X & H L \\
\hline H & L & X & X & X & L H \\
\hline L & L & X & X & X & \(\mathrm{H}^{*} \mathrm{H}^{*}\) \\
\hline H & H & \(\Omega\) & L & L & \(\mathrm{Q}_{0} \quad \bar{Q}_{0}\) \\
\hline H & H & \(\Omega\) & H & L & H L \\
\hline H & H & \(\Omega\) & L & H & L H \\
\hline H & H & \(\Omega\) & H & H & Toggle \\
\hline
\end{tabular}

Note 1: \(\mathrm{J}=(\mathrm{J} 1)(\mathrm{J} 2)(\mathrm{J} 3), \mathrm{K}=(\mathrm{K} 1)(\mathrm{K} 2)(\mathrm{K} 3)\)
\(\mathrm{H}=\) High Logic Level
\(X=\) Either Low or High Logic Level
\(\mathrm{L}=\) Low Logic Level
\(\Omega=\) Positive pulse. The \(J\) and \(K\) inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.
\(Q_{0}=\) The output logic level before the indicated input conditions were established.
* \(=\) This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.
Toggle \(=\) Each output changes to the complement of its previous level on each complete high level clock pulse.

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
\begin{tabular}{lr} 
Supply Voltage & 8 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \\
DM54L & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guarateed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54L72} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & V \\
\hline \multirow[t]{2}{*}{\(V_{\text {IL }}\)} & \multirow[t]{2}{*}{Low Level Input Voltage} & Clock & & & 0.6 & \multirow[t]{2}{*}{V} \\
\hline & & Others & & & 0.7 & \\
\hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.2 & mA \\
\hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 2 & mA \\
\hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & & 6 & MHz \\
\hline \multirow[t]{4}{*}{\(\mathrm{t}_{\mathrm{w}}\)} & \multirow[t]{4}{*}{Pulse Width (Note 2)} & Clock High & 100 & & & \multirow{4}{*}{ns} \\
\hline & & Clock Low & 100 & & & \\
\hline & & Preset Low & 100 & & & \\
\hline & & Clear Low & 100 & & & \\
\hline \(\mathrm{t}_{\text {SU }}\) & \multicolumn{2}{|l|}{Input Setup Time (Notes 1 \& 2)} & \(0 \uparrow\) & & & ns \\
\hline \(t_{H}\) & \multicolumn{2}{|l|}{Input Hold Time (Notes 1 \& 2)} & \(0 \downarrow\) & & & ns \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Note 1: The symbols ( \(\uparrow, \downarrow\) ) indicate the edge of the clock pulse used for reference: \(\uparrow\) for rising edge, \(\downarrow\) for falling edge.
Note 2: \(T_{A}=25^{\circ} \mathrm{C}\) and \(V_{C C}=5 \mathrm{~V}\).

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.3 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & & 0.15 & 0.3 & V \\
\hline \multirow[t]{4}{*}{1} & \multirow[t]{4}{*}{Input Current @ Max Input Voltage} & \multirow[t]{4}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=5.5 \mathrm{~V}
\end{aligned}
\]} & J, K & & & 100 & \multirow{4}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Clear & & & 200 & \\
\hline & & & Preset & & & 200 & \\
\hline & & & Clock & & & 200 & \\
\hline \multirow[t]{4}{*}{\({ }_{1} \mathrm{H}\)} & \multirow[t]{4}{*}{High Level Input Current} & \multirow[t]{4}{*}{\[
\begin{aligned}
& V_{C C}=\operatorname{Max} \\
& V_{1}=2.4 V
\end{aligned}
\]} & J, K & & & 10 & \multirow{4}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Clear & & & 20 & \\
\hline & & & Preset & & & 20 & \\
\hline & & & Clock & & & -200 & \\
\hline \multirow[t]{4}{*}{ILL} & \multirow[t]{4}{*}{Low Level Input Current} & \multirow[t]{4}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=0.3 V
\end{aligned}
\]} & J, K & & & -0.18 & \multirow{4}{*}{mA} \\
\hline & & & Clear & & & -0.36 & \\
\hline & & & Preset & & & -0.36 & \\
\hline & & & Clock & & & -0.36 & \\
\hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\)} & -3 & & -15 & mA \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 2)} & & 0.76 & 1.44 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, T_{A}=25^{\circ} \mathrm{C}\).
Note 2: With all outputs open, Icc is measured with the \(Q\) and \(\bar{Q}\) outputs high in turn. At the time of measurement the clock input is grounded.
Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{Symbol} & \multirow[b]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=4 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \multirow[b]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 6 & & MHz \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Preset to Q & & 75 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Preset to \(\bar{Q}\) & & 150 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Level Output Low to High Level Output & \[
\begin{aligned}
& \text { Clear } \\
& \text { to } \overline{\mathrm{Q}}
\end{aligned}
\] & & 75 & ns \\
\hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & \[
\begin{aligned}
& \text { Clear } \\
& \text { to } Q
\end{aligned}
\] & & 150 & ns \\
\hline \({ }_{\text {PLLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Q or \(\bar{Q}\) & 10 & 75 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Q or \(\bar{Q}\) & 10 & 150 & ns \\
\hline
\end{tabular}

\section*{DM54L73 Dual Master-Slave J-K Flip-Flops with Clear and Complementary Outputs}

\section*{General Description}

This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high, the data from the J and K inputs are
disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic states of the \(J\) and \(K\) inputs must not be allowed to change while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse. A low logic level on the clear input will reset the outputs regardless of the logic states of the other inputs.

\section*{Connection Diagram}

\section*{Dual-In-Line Package}


TL/F/6630-1
Order Number DM54L73J or DM54L73W See NS Package Number J14A or W14B

Function Table
\begin{tabular}{|c|c|c|c|cc|}
\hline \multicolumn{4}{|c|}{ Inputs } & \multicolumn{2}{c|}{ Outputs } \\
\hline CLR & CLK & J & K & Q & \(\overline{\mathbf{Q}}\) \\
\hline\(L\) & X & X & X & L & \(H\) \\
\(H\) & \(\Omega\) & \(L\) & \(L\) & \(Q_{O}\) & \(\bar{Q}_{O}\) \\
\(H\) & \(\Omega\) & \(H\) & \(L\) & \(H\) & \(L\) \\
\(H\) & \(\Omega\) & \(L\) & \(H\) & L & \(H\) \\
\(H\) & \(\Omega\) & \(H\) & \(H\) & \multicolumn{2}{|c|}{ Toggle } \\
\hline
\end{tabular}
\(H=\) High Logic Level
X = Either Low or High Logic Level
L = Low Logic Level
\(\Omega=\) Positive pulse data. The \(J\) and \(K\) inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.
\(Q_{0}=\) The output logic level before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each complete high level clock pulse.
```

Absolute Maximum Ratings
(Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for availability and specifications.

| Supply Voltage | 8 V |
| :--- | ---: |
| Input Voltage | 5.5 V |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Operating Free Air Temperature Range |  |
| DM54L | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |

```

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54L73} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & \\
\hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & V \\
\hline \multirow[t]{2}{*}{\(\mathrm{V}_{\text {IL }}\)} & \multirow[t]{2}{*}{Low Level Input Voltage} & Clock & & & 0.6 & \multirow{2}{*}{V} \\
\hline & & Others & & & 0.7 & \\
\hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.2 & mA \\
\hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 2 & mA \\
\hline \(\mathrm{f}_{\text {CLK }}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & & 6 & MHz \\
\hline \multirow[t]{3}{*}{tw} & \multirow[t]{3}{*}{Pulse Width (Note 2)} & Clock High & 100 & & & \multirow{3}{*}{ns} \\
\hline & & Clock Low & 100 & & & \\
\hline & & Clear Low & 100 & & & \\
\hline tsu & \multicolumn{2}{|l|}{Input Setup Time (Notes 1 \& 2)} & \(0 \uparrow\) & & & ns \\
\hline \(t_{H}\) & \multicolumn{2}{|l|}{Input Hold Time (Notes 1 \& 2)} & \(0 \downarrow\) & & & ns \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Note 1: The symbols ( \(\uparrow, \downarrow\) ) indicate the edge of the clock pulse used for reference: \(\uparrow\) for rising edge, \(\downarrow\) for falling edge.
Note 2: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{C}}=5 \mathrm{~V}\).

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.3 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Voltage Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & & 0.15 & 0.3 & V \\
\hline \multirow[t]{3}{*}{1} & \multirow[t]{3}{*}{Input Current @ Max Input Voltage} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{I}=5.5 V
\end{aligned}
\]} & J, K & & & 100 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Clear & & & 200 & \\
\hline & & & Clock & & & 200 & \\
\hline \multirow[t]{3}{*}{\(\mathrm{IIH}^{\text {H}}\)} & \multirow[t]{3}{*}{High Level Input Current} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=2.4 V
\end{aligned}
\]} & J, K & & & 10 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Clear & & & 20 & \\
\hline & & & Clock & & & -200 & \\
\hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=0.3 V
\end{aligned}
\]} & J, K & & & -0.18 & \multirow{3}{*}{mA} \\
\hline & & & Clear & & & -0.36 & \\
\hline & & & Clock & & & -0.36 & \\
\hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\(V_{C C}=\) Max} & -3 & & -15 & mA \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\) (Note 2)} & & 1.5 & 2.88 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: With all outputs open, ICC is measured with the \(Q\) and \(\bar{Q}\) outputs high in turn. At the time of measurement, the clock is grounded.
Switching Characteristics \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{\begin{tabular}{l}
From (Input) \\
To (Output)
\end{tabular}} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=\mathbf{4 k} \Omega, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 6 & & MHz \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clear to Q & & 150 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clear to \(\bar{Q}\) & & 75 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Q or \(\bar{Q}\) & 10 & 75 & ns \\
\hline tPHL & Propagation Delay Time High to Low Level Output & Clock to Q or \(\overline{\mathrm{Q}}\) & 10 & 150 & ns \\
\hline
\end{tabular}

\section*{DM54L74 Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear, and Complementary Outputs}

\section*{General Description}

This device contains two independent positive-edge-triggered \(D\) flip-flops with complementary outputs. The information on the \(D\) input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the \(D\) input
may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

\section*{Connection Diagram}


TL/F/6631-1
Order Number DM54L74J or DM54L74W
See NS Package Number J14A or W14B

\section*{Function Table}
\begin{tabular}{|c|c|c|c|cc|}
\hline \multicolumn{5}{|c|}{ Inputs } & \multicolumn{2}{c|}{ Outputs } \\
\hline PR & CLR & CLK & D & Q & Q \\
\hline L & \(H\) & X & X & \(H\) & L \\
\(H\) & L & X & X & L & \(H\) \\
L & L & X & X & \(H^{*}\) & \(H^{*}\) \\
\(H\) & \(H\) & \(\uparrow\) & \(H\) & \(H\) & \(L\) \\
\(H\) & \(H\) & \(\uparrow\) & L & L & \(H\) \\
\(H\) & \(H\) & L & X & \(Q_{O}\) & Q \(_{\text {O }}\) \\
\hline
\end{tabular}
\(H=\) High Logic Level
\(X=\) Either Low or High Logic Level
\(L=\) Low Logic Level
\(\uparrow=\) Positive-going transition.
\(Q_{O}=\) The output logic level of \(Q\) before the indicated input conditions were established.
* \(=\) This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs returned to their inactive (high) level.
\begin{tabular}{|c|c|}
\hline \multicolumn{2}{|l|}{Absolute Maximum Ratings (Note)} \\
\hline If Military/Aerospace specified dev please contact the National Sem Office/Distributors for availability an & ces are required, conductor Sales specifications. \\
\hline Supply Voltage & 8 V \\
\hline Input Voltage & 5.5 V \\
\hline Operating Free Air Temperature Range DM54L & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
\hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54L74} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & \\
\hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.7 & V \\
\hline \(\mathrm{IOH}^{\text {l }}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.2 & mA \\
\hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 2 & mA \\
\hline fCLK & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & & 6 & MHz \\
\hline \multirow[t]{4}{*}{tw} & \multirow[t]{4}{*}{Pulse Width (Note 2)} & Clock High & 75 & & & \multirow{4}{*}{ns} \\
\hline & & Clock Low & 75 & & & \\
\hline & & Preset Low & 75 & & & \\
\hline & & Clear Low & 75 & & & \\
\hline tsu & \multicolumn{2}{|l|}{Input Setup Time (Notes 1 \& 2)} & \(50 \uparrow\) & & & ns \\
\hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Input Hold Time (Notes 1 \& 2)} & \(15 \uparrow\) & & & ns \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Note 1: The symbol ( \(\uparrow\) ) indicates the rising edge of the clock pulse is used for reference.
Note 2: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \begin{tabular}{l}
Typ \\
(Note 1)
\end{tabular} & Max & Units \\
\hline V OH & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOH}_{\mathrm{OH}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & 2.4 & 3.3 & & V \\
\hline VoL & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}^{2}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & & 0.15 & 0.3 & V \\
\hline \multirow[t]{4}{*}{11} & \multirow[t]{4}{*}{Input Current © Max Input Voltage} & \multirow[t]{4}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=5.5 \mathrm{~V}
\end{aligned}
\]} & D & & & 100 & \multirow{4}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Clear & & & 300 & \\
\hline & & & Preset & & & 200 & \\
\hline & & & Clock & & & 200 & \\
\hline \multirow[t]{4}{*}{\({ }_{1 / 4}\)} & \multirow[t]{4}{*}{High Level Input Current} & \multirow[t]{4}{*}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Max} \\
& \mathrm{~V}_{1}=2.4 \mathrm{~V}
\end{aligned}
\]} & D & & & 10 & \multirow{4}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Clear & & & 30 & \\
\hline & & & Preset & & & 20 & \\
\hline & & & Clock & & & 20 & \\
\hline \multirow[t]{4}{*}{ILL} & \multirow[t]{4}{*}{Low Level Input Current} & \multirow[t]{4}{*}{\[
\begin{aligned}
& V_{c \mathrm{cc}}=\operatorname{Max} \\
& \mathrm{V}_{1}=0.3 \mathrm{~V}
\end{aligned}
\]} & D & & & -0.18 & \multirow{4}{*}{mA} \\
\hline & & & Clear & & & -0.36 & \\
\hline & & & Preset & & & -0.18 & \\
\hline & & & Clock & & & -0.36 & \\
\hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\) Max} & -3 & & -15 & mA \\
\hline Icc & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\operatorname{Max}\) (Note 2)} & & 1.6 & 3 & mA \\
\hline
\end{tabular}


Switching Characteristics at \(\mathrm{VCC}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Lood)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=4 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 6 & & MHz \\
\hline \({ }_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output & Preset to Q & & 60 & ns \\
\hline tPHL & Propagation Delay Time High to Low Level Output & Preset to \(\bar{Q}\) & & 120 & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
\begin{aligned}
& \text { Clear } \\
& \text { to } \overline{\mathrm{Q}}
\end{aligned}
\] & & 60 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
\begin{aligned}
& \hline \text { Clear } \\
& \text { to } Q \\
& \hline
\end{aligned}
\] & & 120 & ns \\
\hline tpLH & Propagation Delay Time Low to High Level Output & Clock to Q or \(\bar{Q}\) & 10 & 90 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Q or \(\bar{Q}\) & 10 & 120 & ns \\
\hline
\end{tabular}

\section*{DM54L93}

\section*{Decade, Divide-by-12, and Binary Counters}

\section*{General Description}

Each of these monolithic counters contains four masterslave flip-flops and additional gating to provide a divide-bytwo counter and a three-stage binary counter for which the count cycle length is divide-by-eight.
To use their maximum count length (decade, divide-bytwelve, or four-bit binary), the \(B\) input is connected to the \(Q_{A}\) output. The input count pulses are applied to input \(A\) and the outputs are as described in the appropriate truth table.

\section*{Features}
- Typical power dissipation 16 mW

■ Count frequency 15 MHz

\section*{Connection Diagram}

Dual-In-Line Package


TL/F/6637-1
Order Number DM54L93J or DM54L93W
See NS Package Number J14A or W14B

\section*{Function Tables}

COUNT SEQUENCE
(See Note A)
\begin{tabular}{|c|cccc|}
\hline \multirow{2}{*}{ Count } & \multicolumn{4}{|c|}{ Output } \\
\cline { 2 - 5 } & \(\mathbf{Q}_{\mathbf{D}}\) & \(\mathbf{Q}_{\mathbf{C}}\) & \(\mathbf{Q}_{\mathbf{B}}\) & \(\mathbf{Q}_{\mathbf{A}}\) \\
\hline 0 & L & L & L & L \\
1 & L & L & L & H \\
2 & L & L & \(H\) & L \\
3 & L & L & \(H\) & H \\
4 & L & \(H\) & L & L \\
5 & L & \(H\) & L & \(H\) \\
6 & L & \(H\) & \(H\) & L \\
7 & L & \(H\) & \(H\) & \(H\) \\
8 & \(H\) & L & L & L \\
9 & \(H\) & L & L & \(H\) \\
10 & \(H\) & L & \(H\) & L \\
11 & \(H\) & L & \(H\) & \(H\) \\
12 & \(H\) & \(H\) & L & L \\
13 & \(H\) & \(H\) & L & \(H\) \\
14 & \(H\) & \(H\) & \(H\) & L \\
15 & \(H\) & \(H\) & \(H\) & \(H\) \\
\hline
\end{tabular}

RESET/COUNT TRUTH TABLE (Note B)
\begin{tabular}{|cc|cccc|}
\hline \multicolumn{2}{|c|}{ Reset Inputs } & \multicolumn{4}{|c|}{ Output } \\
\hline Ro(1) & R0(2) & \(\mathbf{Q}_{\mathbf{D}}\) & \(\mathbf{Q}_{\mathbf{C}}\) & \(\mathbf{Q}_{\mathbf{B}}\) & \(\mathbf{Q}_{\mathbf{A}}\) \\
\hline H & H & L & L & L & L \\
L & X & & COUNT & \\
X & L & & COUNT \\
\hline
\end{tabular}

Note \(A\) : Output \(Q_{A}\) is connected to input \(B\)
Note B: \(\mathrm{H}=\) High Level, \(L=\) Low Level, \(X=\) Don't Care.

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and speclfications.
\begin{tabular}{lr} 
Supply Voltage & 8 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \\
DM54L & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54L93} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & \\
\hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.7 & V \\
\hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.2 & mA \\
\hline \(\mathrm{lOL}^{2}\) & \multicolumn{2}{|l|}{Low Level Output Current} & & & 2 & mA \\
\hline \(\mathrm{f}_{\text {CLK }}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 5)} & 0 & & 6 & MHz \\
\hline \multirow[t]{3}{*}{\(\mathrm{t}_{\mathrm{W}}\)} & \multirow[t]{3}{*}{Pulse Width (Note 5)} & A & 90 & & & \multirow{3}{*}{ns} \\
\hline & & B & 90 & & & \\
\hline & & Reset & 200 & & & \\
\hline \(t_{\text {REL }}\) & \multicolumn{2}{|l|}{Reset Release time (Note 5)} & 200 & & & ns \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min} \\
& \text { (Note 4) }
\end{aligned}
\]} & & 0.15 & 0.3 & V \\
\hline \multirow[t]{3}{*}{1} & \multirow[t]{3}{*}{Input Current @ Max Input Voltage} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=5.5 V
\end{aligned}
\]} & Reset & & & 0.1 & \multirow{3}{*}{mA} \\
\hline & & & A & & & 0.2 & \\
\hline & & & B & & & 0.2 & \\
\hline \multirow[t]{3}{*}{\(\mathrm{IIH}^{\text {H}}\)} & \multirow[t]{3}{*}{High Level Input Current} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=2.4 V
\end{aligned}
\]} & Reset & & & 10 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & A & & & 20 & \\
\hline & & & B & & & 20 & \\
\hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=0.3 V
\end{aligned}
\]} & Reset & & & -0.18 & \multirow{3}{*}{mA} \\
\hline & & & A & & & -0.36 & \\
\hline & & & B & & & -0.36 & \\
\hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\text { Max } \\
& \text { (Note 2) } \\
& \hline
\end{aligned}
\]} & -3 & & -15 & mA \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}\) (Note 3)} & & & 5.5 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time.
Note 3: ICC is measured with all outputs open, RO inputs grounded following momentary connection to 4.5 V and all other inputs grounded.
Note 4: \(Q_{A}\) outputs are tested at \(I_{O L}=\) max plus the limit value of \(I_{I L}\) for the \(B\) input. This permits driving the \(B\) input while maintaining full fan-out capability.
Note 5: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

Switching CharacteristicS at \(\mathrm{V}_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{\begin{tabular}{l}
From (Input) \\
To (Output)
\end{tabular}} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=4 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & \(A\) to \(Q_{A}\) & 6 & & MHz \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & A to \(Q_{D}\) & & 400 & ns \\
\hline tPHL & Propagation Delay Time High to Low Level Output & \(A\) to \(Q_{D}\) & & 400 & ns \\
\hline
\end{tabular}

\section*{Logic Diagram}


TL/F/6637-2
The \(J\) and \(K\) inputs shown without connection are for reference only and are functionally at a high level.

\section*{DM54L95 4-Bit Parallel Access Shift Registers}

\section*{General Description}

These 4-bit registers feature parallel and serial inputs, parallel output, mode control, and two clock inputs. The registers have three modes of operation.

Parallel (broadside) load
Shift right (the direction \(Q_{A}\) toward \(Q_{D}\) )
Shift left (the direction \(Q_{D}\) toward \(Q_{A}\) )
Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.
Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the
mode control is high by connecting the output of each flipflop to the parallel input of the previous flip-flop ( \(Q_{D}\) to input C , etc.) and serial data is entered at input D . The clock input may be applied simultaneously to clock 1 and clock 2 if both modes can be clocked from the same source.
Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the truth table will also ensure that register contents are protected.

\section*{Features}

■ Typical maximum clock frequency 14 MHz
- Typical power dissipation mW

\section*{Connection Diagram}


Order Number DM54L95J or DM54L95W
See NS Package Number J14A or W14B

\section*{Function Table}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{8}{|c|}{Inputs} & \multicolumn{4}{|c|}{Outputs} \\
\hline \multirow[t]{2}{*}{Mode Control} & \multicolumn{2}{|r|}{Clocks} & \multirow[t]{2}{*}{Serial} & \multicolumn{4}{|c|}{Parallel} & \multirow{2}{*}{\(Q_{A}\)} & \multirow[t]{2}{*}{\(Q_{B}\)} & \multirow[t]{2}{*}{\(Q_{C}\)} & \multirow[t]{2}{*}{\(Q_{D}\)} \\
\hline & 2 (L) & 1 (R) & & A & B & C & D & & & & \\
\hline H & H & X & X & X & X & X & X & \(Q_{A O}\) & \(Q_{B O}\) & Q \({ }_{\text {co }}\) & \(Q_{\text {DO }}\) \\
\hline H & \(\downarrow\) & X & X & a & b & c & d & a & b & c & d \\
\hline H & \(\downarrow\) & X & X & \(\mathrm{Q}_{\mathrm{B}}{ }^{\dagger}\) & \(Q_{C}{ }^{\dagger}\) & QD \({ }^{\dagger}\) & d & \(Q_{B n}\) & \(Q_{\text {cn }}\) & \(Q_{\text {Dn }}\) & d \\
\hline L & L & H & X & X & X & X & X & QAO & \(Q_{B O}\) & Qco & \(Q_{\text {DO }}\) \\
\hline L & X & \(\downarrow\) & H & X & X & X & X & H & \(Q_{\text {An }}\) & \(Q_{\text {Bn }}\) & \(Q_{C n}\) \\
\hline L & X & \(\downarrow\) & L & X & X & X & X & L & \(Q_{\text {An }}\) & \(Q_{B n}\) & \(Q_{C n}\) \\
\hline \(\uparrow\) & L & L & X & X & X & X & X & \(Q_{\text {AO }}\) & \(\mathrm{Q}_{\mathrm{Bn}}\) & Qco & \(Q_{\text {DO }}\) \\
\hline \(\downarrow\) & L & L & X & X & X & X & X & \(Q_{A O}\) & \(\mathrm{Q}_{\mathrm{BO}}\) & Qco & \(Q_{D O}\) \\
\hline \(\downarrow\) & L & H & \(x\) & \(x\) & \(x\) & X & X & \(Q_{A O}\) & \(\mathrm{Q}_{\text {BO }}\) & Qco & QDO \\
\hline \(\uparrow\) & H & L & X & X & X & X & X & \(Q_{A O}\) & \(\mathrm{Q}_{\mathrm{BO}}\) & Qco & QDO \\
\hline \(\uparrow\) & H & H & \(X\) & X & X & X & X & \(Q_{A O}\) & \(\mathrm{Q}_{\mathrm{BO}}\) & \(Q_{\text {co }}\) & \(Q_{\text {DO }}\) \\
\hline
\end{tabular}

\footnotetext{
\(\dagger\) Shifting left requires external connection of \(Q_{B}\) to \(A, Q_{C}\) to \(B, Q_{D}\) to \(C\). Serial data is entered at input \(D\).
}
\(H=\) High Level (Steady State), \(L=\) Low Level (Steady State), \(X=\) Don't Care (Any input, including transitions).
\(\downarrow=\) Transition from high to low level. \(\uparrow=\) Transition from low to high level.
\(a, b, c, d,=\) The level of steady state input at inputs \(A, B, C\), or \(D\), respectively.
\(Q_{A O}, Q_{B O}, Q_{C O}, Q_{D O}=\) The level of \(Q_{A}, Q_{B}, Q_{C}\), or \(Q_{D}\), respectively, before the indicated steady state input conditions were established. \(Q_{A n}, Q_{B n}, Q_{C n}, Q_{D n}=\) The level of \(Q_{A}, Q_{B}, Q_{C}\), or \(Q_{D}\), respectively, before the most recent \(\downarrow\) transition of the clock.

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
8 V
Input Voltage
5.5V

Operating Free Air Temperature Range
\(\begin{array}{ll}\text { DM54L } & -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\ \text { Storage Temperature Range } & -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C}\end{array}\)

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54L95} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & \\
\hline \(V_{\text {cc }}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & V \\
\hline \(V_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.7 & V \\
\hline \(\mathrm{IOH}^{\text {l }}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.2 & mA \\
\hline loL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 2 & mA \\
\hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 1)} & 0 & & 6 & MHz \\
\hline \(t_{\text {W }}\) (CLK) & \multicolumn{2}{|l|}{Pulse Width of Clock (Note 1)} & 90 & & & ns \\
\hline \(\mathrm{t}_{\text {SU }}\) & \multicolumn{2}{|l|}{Data Setup Time (Note 1)} & 50 & & & ns \\
\hline \multirow[t]{2}{*}{\(t_{\text {EN }}\)} & \multirow[t]{2}{*}{Time to Enable Clock (Note 1)} & Clock 1 & 120 & & & ns \\
\hline & & Clock 2 & 100 & & & ns \\
\hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Data Hold Time (Note 1)} & 0 & & & ns \\
\hline \(\mathrm{t}_{\mathrm{IN}}\) & \multicolumn{2}{|l|}{Time to Inhibit Clock 1 or Clock 2 (Note 1)} & 0 & & & ns \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Note 1: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline V OH & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.1 & & V \\
\hline VOL & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=M i n, I_{O L}=M a x \\
& V_{I L}=M a x, V_{I H}=M i n
\end{aligned}
\]} & & 0.13 & 0.3 & V \\
\hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current © Max Input Voltage} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=5.5 \mathrm{~V}
\end{aligned}
\]} & Mode & & & 0.2 & \multirow[t]{2}{*}{mA} \\
\hline & & & Others & & & 0.1 & \\
\hline \multirow[t]{2}{*}{\(I_{1 H}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=2.4 V
\end{aligned}
\]} & Mode & & & 20 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & Others & & & 10 & \\
\hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& V_{1}=0.3 V
\end{aligned}
\]} & Mode & & & -0.36 & \multirow[t]{2}{*}{mA} \\
\hline & & & Others & & & -0.18 & \\
\hline los & Short Circuit Output Current & \[
\begin{aligned}
& V_{C C}=\text { Max } \\
& \text { (Note 2) } \\
& \hline
\end{aligned}
\] & & -3 & & -15 & mA \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 3)} & & 4.8 & 8 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}} 25^{\circ} \mathrm{C}\)
Note 2: Not more than one output should be shorted at a time.
Note 3: \(\mathrm{I}_{\mathrm{Cc}}\) is measured with all outputs and serial input open; \(\mathrm{A}, \mathrm{B}, \mathrm{C}\), and D inputs grounded; mode control at 4.5 V ; and a momentary 3 V , then ground, applied to both clock inputs.
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=4 \Omega, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 6 & & MHz \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Output & & 90 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Output & & 90 & ns \\
\hline
\end{tabular}

\section*{Logic Diagram}


TL/F/6638-2

\section*{DM54L98 4-Bit Storage Register}

\section*{General Description}

This data selector/storage register is composed of four S-R master-slave flip-flops, four AND-OR INVERT gates, one buffer, and six inverter/drivers.
When the word select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high level input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is shifted to the output terminals on the nega-tive-going edge of the clock pulse.
Typical clock frequency is 12 MHz .

\section*{Absolute Maximum Ratings (Note)}

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
8 V
Input Voltage 5.5 V
Operating Free Air Temperature Range
DM54L
\(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
Storage Temperature Range \(\quad-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Connection Diagram}


TL/F/6639-1
Order Number DM54L98J or DM54L98W See NS Package Number J16A or W16A

Logic Diagram


Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54L98} & \multirow{2}{*}{Units} \\
\hline & & & Min & Nom & Max & \\
\hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.7 & V \\
\hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.2 & mA \\
\hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 2 & mA \\
\hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 4)} & 0 & & 6 & MHz \\
\hline tw & \multicolumn{2}{|l|}{Clock Pulse Width (Note 4)} & 100 & 65 & & ns \\
\hline \multirow[t]{4}{*}{tsu} & \multirow[t]{4}{*}{Setup Time (Note 4)} & Data High & 100 & & & \multirow{4}{*}{ns} \\
\hline & & Data Low & 120 & & & \\
\hline & & Select High & 150 & & & \\
\hline & & Select Low & 100 & & & \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ (Note 1) & Max & Units \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\] & 2.4 & & & V \\
\hline V OL & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\] & & 0.15 & 0.3 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 0.1 & mA \\
\hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \(V_{C C}=M a x, V_{1}=2.4 \mathrm{~V}\) & & & 10 & \(\mu \mathrm{A}\) \\
\hline ILL & Low Level Input Current & \(V_{C C}=\operatorname{Max}, V_{1}=0.3 \mathrm{~V}\) & & & \(-0.18\) & mA \\
\hline los & Short Circuit Output Current & \(V_{C C}=\operatorname{Max}\) (Note 3) & -3 & & -15 & mA \\
\hline ICC & Supply Current & \(V_{C C}=\operatorname{Max}\) (Note 2) & & 6 & 8 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: ICC is measured with all outputs open and all inputs grounded.
Note 3: Not more than one output should be shorted at a time.
Note 4: \(T_{A}=25^{\circ} \mathrm{C}\) and \(V_{C C}=5 \mathrm{~V}\).
Switching Characteristics at \(\mathrm{V}_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{Symbol} & \multirow[b]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=\mathbf{4 k}\), \(\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}\)} & \multirow[b]{2}{*}{Units} \\
\hline & & & Min & Max & \\
\hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 6 & & MHz \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Output & & 80 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Output & & 100 & ns \\
\hline
\end{tabular}

\section*{93L00}

\section*{4-Bit Universal Shift Register}

\section*{General Description}

The 93L00 is a 4-bit universal shift register. As a high speed multifunctional sequential logic block, it is useful in a wide variety of register and counter applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallelserial, and parallel-parallel data register transfers.

\section*{Connection Diagram}


\section*{Logic Symbol}

TL/F/9576-1
Order Number 93L00DMQB or 93L00FMQB
See NS Package Number J16A or W16A
\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
\hline\(\overline{\mathrm{PE}}\) & Parallel Enable Input (Active LOW) \\
PO-P3 & Parallel Inputs \\
J & First Stage J Input (Active HIGH) \\
\(\overline{\mathrm{K}}\) & First Stage K Input (Active LOW) \\
CP & Clock Pulse Input (Active Rising Edge) \\
\(\overline{\mathrm{MR}}\) & Master Reset Input \\
\(\mathrm{Q} 0-\mathrm{Q3}\) & Parallel Outputs \\
\(\overline{\mathrm{Q} 3}\) & Complementary Last Stage Output \\
\hline
\end{tabular}
```

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for availability and specifications.
Supply Voltage 7V
Input Voltage 5.5 V
Operating Free Air Temperature Range
MIL $\quad-65^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$

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Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{93L00 (MIL)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.7 & V \\
\hline IOH & High Level Output Voltage & & & -0.4 & mA \\
\hline \(\mathrm{lOL}^{\text {L }}\) & Low Level Output Current & & & 4.8 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline \[
\begin{aligned}
& t_{s}(H) \\
& t_{s}(L)
\end{aligned}
\] & Setup Time HIGH or LOW, \(\mathrm{J}, \overline{\mathrm{K}}\) and PO-P3 to CP & \[
\begin{aligned}
& 60 \\
& 60 \\
& \hline
\end{aligned}
\] & & & ns \\
\hline \[
\begin{aligned}
& t_{h}(H) \\
& t_{h}(L) \\
& \hline
\end{aligned}
\] & Hold Time HIGH or LOW, \(J, \bar{K}\) and PO-P3 to CP & \[
\begin{aligned}
& 0 \\
& 0 \\
& \hline
\end{aligned}
\] & & & ns \\
\hline \[
\begin{aligned}
& t_{s}(H) \\
& t_{s}(L)
\end{aligned}
\] & Setup Time HIGH or LOW, \(\overline{\text { PE to }} \mathrm{CP}\) & \[
\begin{aligned}
& 68 \\
& 68 \\
& \hline
\end{aligned}
\] & & & ns \\
\hline \[
\begin{aligned}
& t_{h}(H) \\
& t_{h}(L)
\end{aligned}
\] & Hold Time HIGH or LOW, \(\overline{\text { PE to CP }}\) & \[
\begin{aligned}
& 0 \\
& 0
\end{aligned}
\] & & & ns \\
\hline \[
\begin{aligned}
& t_{w}(H) \\
& t_{w}(L) \\
& \hline
\end{aligned}
\] & CP Pulse Width HIGH or LOW & \[
\begin{aligned}
& 38 \\
& 38
\end{aligned}
\] & & & ns \\
\hline \(t_{w}(\mathrm{~L})\) & \(\overline{M R}\) Pulse Width LOW & 53 & & & ns \\
\hline \(t_{\text {rec }}\) & Recovery Time, \(\overline{\text { MR }}\) to CP & 70 & & & ns \\
\hline
\end{tabular}

\section*{Electrical Characteristics}

Over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) }
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-10 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=M i n, I_{O H}=\operatorname{Max}, \\
& V_{\mathrm{IL}}=\operatorname{Max}, V_{I H}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & 0.3 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{3}{*}{\(\mathrm{IIH}^{\text {H}}\)} & \multirow[t]{3}{*}{High Level Input Current} & \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & Inputs & & & 20 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & CP & & & 40 & \\
\hline & & & \(\overline{\text { PE }}\) & & & 46 & \\
\hline \multirow[t]{3}{*}{I/L} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.3 \mathrm{~V}\)} & Inputs & & & -400 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & CP & & & -800 & \\
\hline & & & \(\overline{\text { PE }}\) & & & -920 & \\
\hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\text { Max } \\
& \text { (Note 2) } \\
& \hline
\end{aligned}
\]} & -2.5 & & -25 & mA \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x\)} & & & 23 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

\section*{Switching Characteristics}
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{2}{|c|}{93L} & \multirow{3}{*}{Units} \\
\hline & & \multicolumn{2}{|c|}{\(C_{L}=15 \mathrm{pF}\)} & \\
\hline & & Min & Max & \\
\hline \(f_{\text {max }}\) & Maximum Shift Frequency & 10 & & MHz \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay CP to \(Q_{n}\) & & \[
\begin{aligned}
& 35 \\
& 51
\end{aligned}
\] & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay, \(\overline{M R}\) to \(Q_{n}\) & & 60 & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The Logic Diagrams and Truth Table indicate the functional characteristics of the 93L00 4-bit shift register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers.
The 93L00 has two primary modes of operation, shift right \((\mathrm{QO} \rightarrow \mathrm{Q1})\) and parallel load, which are controlled by the state of the Parallel Enable (PE) input. When the \(\overline{P E}\) input is HIGH, serial data enters the first flip-flop Q0 via the J and \(\overline{\mathrm{K}}\) inputs and is shifted one bit in the direction Q0 \(\rightarrow\) Q1 \(\rightarrow\) Q2 \(\rightarrow\) Q3 following each LOW-to-HIGH clock transition. The \(\sqrt{\bar{K}}\) inputs provide the flexibility of the JK type input for special applications, and the simple D-type input for general applications by tying the two pins together.

When the \(\overline{\mathrm{PE}}\) input is LOW, the 93L00 appears as four common clocked \(D\) flip-flops. The data on the parallel inputs P0-P3 is transferred to the respective Q0-Q3 outputs following the LOW-to-HIGH clock transition. Shift left operation (Q3 \(\rightarrow\) Q2) can be achieved by tying the Qn outputs to the \(\mathrm{Pn}-1\) inputs and holding the \(\overline{\mathrm{PE}}\) input LOW.
All serial and parallel data transfers are synchronous, occuring after each LOW-to-HIGH clock transition. Since the 93 LOO utilizes edge triggering, there is no restriction on the activity of the J, \(\overline{\mathrm{K}}, \mathrm{Pn}\) and \(\overline{\mathrm{PE}}\) inputs for logic operation-except for the setup and release time requirements. A LOW on the asynchronous Master Reset ( \(\overline{\mathrm{MR}}\) ) input sets all Q outputs LOW, independent of any other input condition.

\section*{Truth Table}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Operating Mode} & \multicolumn{7}{|c|}{Inputs ( \(\overline{\mathrm{MR}}=\mathrm{H}\) )} & \multicolumn{5}{|c|}{Outputs @ \(\mathrm{t}_{\mathrm{n}+1}\)} \\
\hline & \(\overline{\text { PE }}\) & J & \(\overline{\mathbf{K}}\) & P0 & P1 & P2 & P3 & Q0 & Q1 & Q2 & Q3 & Q3 \\
\hline \multirow{4}{*}{Shift Mode} & H & L & L & X & X & X & X & L & Q0 & Q1 & Q2 & Q2 \\
\hline & H & L & H & X & X & X & X & Q0 & Q0 & Q1 & Q2 & Q2 \\
\hline & H & H & L & X & X & X & X & Q0 & Q0 & Q1 & Q2 & Q2 \\
\hline & H & H & H & X & X & X & X & H & Q0 & Q1 & Q2 & Q2 \\
\hline Parallel & L & X & X & L & L & L & L & L & L & L & L & H \\
\hline Entry Mode & L & X & X & H & H & H & H & H & H & H & H & L \\
\hline
\end{tabular}

\footnotetext{
\({ }^{*} \mathrm{t}_{\mathrm{n}+1}=\) Indicates state after next LOW-to-HIGH clock transition.
\(H=H I G H\) Voltage Level
\(L=\) LOW Voltage Level
\(\mathrm{X}=\) Immaterial
}

\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{c|}{ Description } \\
\hline \(\mathrm{A} 0-\mathrm{A} 3\) & Address Inputs \\
\(\overline{\mathrm{O}} 0-\overline{\mathrm{O} 9}\) & Decoder Outputs (Active LOW) \\
\hline
\end{tabular}
\begin{tabular}{|c|c|}
\hline \begin{tabular}{l}
Absolute Maximum Rati \\
If Military/Aerospace specified devi please contact the National Sem Office/Distributors for avallability and
\end{tabular} & ngs (Note) ces are required conductor Sales specifications. \\
\hline Supply Voltage & \\
\hline Input Voltage & 5.5 V \\
\hline Operating Free Air Temperature Range MIL & \\
\hline ure & \(-65^{\circ}\) \\
\hline
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multirow{2}{|c|}{ Parameter } & \multicolumn{2}{c|}{ 93L01 (MIL) } & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.7 & V \\
\hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -400 & \(\mathrm{\mu A}\) \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 4.8 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(V_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-10 \mathrm{~mA}\) & & & -1.5 & V \\
\hline V OH & High Level Output Voltage & \[
\begin{aligned}
& V_{\mathrm{CC}}=\text { Min, }, I_{O H}=\text { Max }, \\
& V_{\mathrm{IL}}=M a x, V_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\] & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
\begin{aligned}
& V_{C C}=\operatorname{Min}, \mathrm{IOL}=\text { Max }, \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & & & 0.3 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\text {CC }}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \({ }_{I N}\) & High Level Input Current & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 20 & \(\mu \mathrm{A}\) \\
\hline ILL & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.3 \mathrm{~V}\) & & & -400 & \(\mu \mathrm{A}\) \\
\hline los & Short Circuit Output Current & \[
\begin{aligned}
& V_{C C}=M a x \\
& \text { (Note 2) }
\end{aligned}
\] & -2.5 & & -25 & mA \\
\hline ICC & Supply Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 3) & & & 13 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: \(\mathrm{I}_{\mathrm{CC}}\) is measured with all outputs open and all inputs grounded.

\section*{Switching Characteristics}
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 3 for waveforms and load configurations)
\begin{tabular}{c|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multirow{2}{*}{ Parameter } & \multicolumn{2}{|c|}{\(\mathbf{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & Max & \\
\hline\(t_{\text {PLH }}\) & Propagation Delay & & 36 & \multirow{2}{*}{ns} \\
\(t_{\text {PHL }}\) & An to \(\bar{O} \mathrm{n}\) & & 36 & \\
\hline
\end{tabular}

\section*{Functional Description}

The 93L01 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with active LOW input enables. The logic design of the 93L01 ensures that all out-
puts are HIGH when binary codes greater than nine are applied to the inputs. The most significant input A3 produces a useful inhibit function when the 93L01 is used as a 1 -of-8 decoder.

\section*{Truth Table}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{4}{|c|}{Inputs} & \multicolumn{10}{|c|}{Outputs} \\
\hline A0 & A1 & A2 & A3 & O0 & \(\overline{0} 1\) & \(\overline{0} 2\) & \(\overline{0} 3\) & \(\overline{0} 4\) & \(\overline{0} 5\) & \(\overline{0} 6\) & \(\overline{0} 7\) & \(\overline{0} 8\) & \(\overline{0} 9\) \\
\hline L & L & L & L & L & H & H & H & H & H & H & H & H & H \\
\hline H & L & L & L & H & L & H & H & H & H & H & H & H & H \\
\hline L & H & L & L & H & H & L & H & H & H & H & H & H & H \\
\hline H & H & L & L & H & H & H & L & H & H & H & H & H & H \\
\hline L & L & H & L & H & H & H & H & L & H & H & H & H & H \\
\hline H & L & H & L & H & H & H & H & H & L & H & H & H & H \\
\hline L & H & H & L & H & H & H & H & H & H & L & H & H & H \\
\hline H & H & H & L & H & H & H & H & H & H & H & L & H & H \\
\hline L & L & L & H & H & H & H & H & H & H & H & H & L & H \\
\hline H & L & L & H & H & H & H & H & H & H & H & H & H & L \\
\hline L & H & L & H & H & H & H & H & H & H & H & H & H & H \\
\hline H & H & L & H & H & H & H & H & H & H & H & H & H & H \\
\hline L & L & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline H & L & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline L & H & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline H & H & H & H & H & H & H & H & H & H & H & H & H & H \\
\hline
\end{tabular}
\[
\begin{aligned}
& H=H I G H \text { Voltage Level } \\
& L=\text { LOW Voltage Level }
\end{aligned}
\]

\section*{Logic Diagram}


TL/F/9583-3

\section*{93L08}

\section*{Dual 4-Bit Latch}

\section*{General Description}

The 93L08 is a dual 4-bit D-type latch designed for general purpose storage applications in digital systems. Each latch contains both an active LOW Master Reset input and active LOW Enable inputs.

\section*{Connection Diagram}

\section*{Logic Symbol}

\[
V_{C C}=\operatorname{Pin} 24
\]


TL/F/9594-1
Order Number 93L08DMQB or 93L08FMQB
See NS Package Number J24A or W24C
\[
\mathrm{GND}=\operatorname{Pin} 12
\]
\begin{tabular}{|c|c|}
\hline Pin Names & Description \\
\hline \[
\left.\begin{array}{l}
\text { D0a-D3a } \\
\text { DOb-D3b }
\end{array}\right\}
\] & Parallel Latch Inputs \\
\hline E'0a, E1a, E0b, E1b, & AND Enable Inputs (Active LOW) \\
\hline \(\overline{\mathrm{MRa}}, \overline{\mathrm{MR}} \mathrm{b}\) & Master Reset Inputs (Active LOW) \\
\hline Q0a-Q3a \(\}\) & \\
\hline Q0b-Q3b & Parallel Latch Outputs \\
\hline
\end{tabular}

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
Operating Free Air Temperature Range
MIL
\(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
Storage Temperature Range \(\quad-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|}
\hline Symbol & Parameter & Min & Nom & Max & Units \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & V \\
\hline IOH & High Level Output Current & & & -400 & \(\mu \mathrm{A}\) \\
\hline l OL & Low Level Output Current & & & 4.8 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline \(t_{\text {s }}(\mathrm{H})\) & Setup Time HIGH, \(\mathrm{D}_{\mathrm{n}}\) to \(\bar{E}_{n}\) & 8 & & & ns \\
\hline \(t_{h}(H)\) & Hold Time HIGH, \(\mathrm{D}_{\mathrm{n}}\) to \(\bar{E}_{n}\) & 1 & & & ns \\
\hline \(t_{s}(L)\) & Setup Time LOW, \(\mathrm{D}_{\mathrm{n}}\) to \(\bar{E}_{n}\) & 18 & & & ns \\
\hline \(t_{h}(L)\) & Hold Time LOW, \(\mathrm{D}_{\mathrm{n}}\) to \(\bar{E}_{\mathrm{n}}\) & 4 & & & ns \\
\hline \(t_{w}(L)\) & \(\bar{E}_{\mathrm{n}}\) Pulse Width LOW & 32 & & & ns \\
\hline \(t_{w}(L)\) & \(\overline{\text { MR }}\) Pulse Width LOW & 30 & & & ns \\
\hline \(t_{\text {rec }}\) & Recovery Time, \(\overline{\mathrm{MR}}\) to \(\overline{\mathrm{E}}_{\mathrm{n}}\) & 10 & & & ns \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) }
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-10 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=\operatorname{Min}, I_{O L}=M a x, \\
& V_{I H}=M i n, V_{I L}=M a x
\end{aligned}
\]} & & & 0.3 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{2}{*}{\(\mathrm{IIH}^{\text {H}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & Inputs & & & 20 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & \(\mathrm{D}_{\mathrm{n}}\) & & & 30 & \\
\hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.3 \mathrm{~V}\)} & Inputs & & & -400 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & \(\mathrm{D}_{\mathrm{n}}\) & & & -640 & \\
\hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 2)} & -2.5 & & -25 & mA \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\) (Note 3)} & & & 29 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: ICC is measured with all outputs open and all inputs grounded.

\section*{Switching Characteristics}
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 3 for waveforms and load configurations)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\(C_{L}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay En to Qn & & \[
\begin{aligned}
& 45 \\
& 38 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay Dn to Qn & & \[
\begin{array}{r}
27 \\
29 \\
\hline
\end{array}
\] & ns \\
\hline tPHL & Propagation Delay \(\overline{M R}\) to \(Q n\) & & 30 & ns \\
\hline
\end{tabular}

\section*{Functional Description}

Data can be entered into the latch when both of the enable inputs are LOW. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes HIGH, the data present in the latch at that time is held in the latch and is no longer affected by data input. The master reset overrides all other input conditions and forces the outputs of all the latches LOW when a LOW signal is applied to the Master Reset input.

Truth Table
\begin{tabular}{|l|c|c|c|c|l|}
\hline\(\overline{\text { MR }}\) & E0 & E1 & D & Qn & Operation \\
\hline H & L & L & L & L & Data Entry \\
H & L & L & H & L & Data Entry \\
H & L & H & X & Qn-1 & Hold \\
H & H & L & X & Qn-1 & Hold \\
H & H & H & X & Qn-1 & Hold \\
L & X & X & X & L & Reset \\
\hline
\end{tabular}
\(Q_{n-1}=\) Previous Output State
\(Q_{n}=\) Present Output State
\(H=\) HIGH Voltage Level
\(\mathrm{L}=\) LOW Voltage Level
\(\mathrm{X}=\) Immaterial

\section*{Logic Diagram}


TL/F/9594-3

\section*{93L09}

\section*{Dual 4-Input Multiplexer}

\section*{General Description}

The 93L09 monolithic dual 4-input digital multiplexers consist of two multiplexing circuits with common input select logic. Each circuit contains four inputs and fully buffered complementary outputs. In addition to multiplexer operation, the 93L09 can generate any two functions of three variables. Active pullups in the outputs ensure high drive and high speed performance. Because of its high speed performance and on-chip select decoding, the 93L09 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output bus.

\section*{Features}
- Multifunction capability
- On-chip select logic decoding
- Fully buffered complementary outputs

\section*{Connection Diagram}


\section*{Logic Symbol}


TL/F/9602-2
\(V_{C C}=\operatorname{Pin} 16\)
\(\mathrm{GND}=\operatorname{Pin} 8\)

TL/F/9602-1
Order Number 93L09DMQB or 93L09FMQB See NS Package Number J16A or W16A
\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
\hline \(\mathrm{SO}, \mathrm{S} 1\) & Common Select Inputs \\
\(10 \mathrm{a}-13 \mathrm{a}\) & Multiplexer A Inputs \\
Za & Multiplexer A Output \\
\(\overline{\mathrm{Za}}\) & Complementary Multiplexer A Output \\
\(\mathrm{IOb}-13 \mathrm{~b}\) & Multiplexer B Inputs \\
Zb & Multiplexer B Output \\
\(\overline{\mathrm{Zb}}\) & Complementary Multiplexer B Output \\
\hline
\end{tabular}

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avallability and specifications.
Supply Voltage 7V

Input Voltage
Operating Free Air Temperature Range
\begin{tabular}{ll} 
MIL & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multirow{2}{|c|}{ Parameter } & \multicolumn{2}{c|}{ 93L09 (MIL) } & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.7 & V \\
\hline \(\mathrm{l}_{\mathrm{OH}}\) & High Level Output Current & & & -400 & \(\mu \mathrm{~A}\) \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 4.8 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) }
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{II}=-10 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\] & 2.4 & & & V \\
\hline VOL & Low Level Output Voltage & \[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & & & 0.3 & V \\
\hline II & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline IIH & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 20 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \(V_{C C}=\) Max, \(V_{1}=0.3 \mathrm{~V}\) & & & -400 & \(\mu \mathrm{A}\) \\
\hline los & Short Circuit Output Current & \(V_{C C}=\operatorname{Max}\) (Note 2) & -10 & & -40 & mA \\
\hline ICC & Supply Current & \(V_{C C}=\operatorname{Max}\) & & & 11.5 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay \(\mathrm{S}_{0}\) to \(\mathrm{Z}_{\mathrm{a}}\) & & \[
\begin{aligned}
& 70 \\
& 60 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay \(\mathrm{S}_{0}\) to \(\overline{\mathrm{Z}}_{\mathrm{a}}\) & & \[
\begin{aligned}
& 55 \\
& 50 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay
\[
I_{0} \text { to } Z_{a}
\] & & \[
\begin{aligned}
& 70 \\
& 65
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay \(\mathrm{S}_{0}\) to \(\overline{\mathrm{Z}}_{\mathrm{a}}\) & & \[
\begin{aligned}
& 40 \\
& 60
\end{aligned}
\] & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The 93L09 dual 4-input multiplexers are able to select two bits of either HIGH or LOW data or control from up to four sources, in one package. The 93L09 is the logical implementation of two-pole, four-position switch, with the position of the switch being set by the logic levels supplied to the two select inputs. Both assertion and negation outputs are provided for both multiplexers. The logic equations for the outputs are shown below:
\[
\begin{aligned}
& \mathrm{Za}=10 \mathrm{a} \cdot \mathrm{~S}_{1} \cdot \overline{\mathrm{~S}} 0+11 \mathrm{a} \cdot \overline{\mathrm{~S}} 1 \cdot \mathrm{~S} 0+12 \mathrm{a} \cdot \mathrm{~S} 1 \cdot \overline{\mathrm{~S}} 0+13 \mathrm{a} \cdot \mathrm{~S} 1 \cdot \mathrm{~S} 0 \\
& \mathrm{Zb}=10 \mathrm{~b} \cdot \overline{\mathrm{~S}} 1 \cdot \overline{\mathrm{~S}} 0+11 \mathrm{~S} \cdot \overline{\mathrm{~S}} 1 \cdot \mathrm{~S} 0+12 \mathrm{a} \cdot \mathrm{~S} 1 \cdot \overline{\mathrm{~S}} 0+13 \mathrm{~b} \cdot \mathrm{~S} 1 \cdot \mathrm{~S} 0
\end{aligned}
\]

The 93L09 is frequently used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the select inputs. A less obvious application is as a function generator. The 93L09 can generate two functions of three variables. This is useful for implementing random gating functions.

\section*{Truth Table}
\begin{tabular}{|cc|cccc|cc|}
\hline \multicolumn{2}{|c|}{\begin{tabular}{c} 
Select \\
Inputs
\end{tabular}} & \multicolumn{4}{c|}{\begin{tabular}{c} 
Inputs \\
(a or b)
\end{tabular}} & & \multicolumn{2}{c|}{\begin{tabular}{c} 
Outputs \\
(a or b)
\end{tabular}} \\
\hline S0 & S1 & 10 & I1 & 12 & I3 & Z & Z \\
\hline L & L & L & X & X & X & L & H \\
L & L & H & X & X & X & H & L \\
H & L & X & L & X & X & L & H \\
H & L & X & H & X & X & H & L \\
L & H & X & X & L & X & L & H \\
L & H & X & X & H & X & H & L \\
H & H & X & X & X & L & L & H \\
H & H & X & X & X & H & H & L \\
\hline
\end{tabular}
\(H=\) HIGH voltage level
\(\mathrm{L}=\) LOW voltage level
\(\mathrm{X}=\) Immaterial

\section*{Logic Diagram}


TL/F/9602-3

\section*{93L10/93L16 BCD Decade Counter/4-Bit Binary Counter}

\section*{General Description}

The 93L10 is a high speed synchronous BCD decade counter and the 93L16 is a high speed synchronous 4-bit binary counter. They are synchronously presettable, multifunctional MSI building blocks useful in a large number of counting, digital integration and conversion applications. Several states of synchronous operation are obtainable with no external gating packages required through an internal carry lookahead counting technique.

\section*{Features}

■ Synchronous counting and parallel entry
- Decoded terminal count
- Built-in Carry Circuitry
- Easy interfacing with DTL, LPDTL, and TTL families

\section*{Connection Diagram}


Order Number 93L10DMQB, 93L10FMQB, 93L16DMQB or 93L16FMQB
See NS Package Number J16A or W16A

Logic Symbol


TL/F/9603-2
\(V_{C C}=\operatorname{Pin} 16\)
GND \(=\operatorname{Pin} 8\)
\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{|c|}{\(\quad\) Description } \\
\hline CEP & Count Enable Parallel Input \\
CET & Count Enable Trickle Input \\
CP & Clock Pulse Input (Active Rising Edge) \\
\(\overline{M R}\) & Asynchronous Master \\
& Reset Input (Active LOW) \\
PO-P3 & Parallel Data Inputs \\
\(\overline{P E}\) & Parallel Enable Input (Active LOW) \\
Q0-Q3 & Flip-Flop Outputs \\
TC & Terminal Count Output \\
\hline
\end{tabular}
\begin{tabular}{|c|c|}
\hline \multicolumn{2}{|l|}{Absolute Maximum Ratings (Note)} \\
\hline If Milltary/Aerospace specifled devi please contact the National Sem Office/Distributors for availability and & ces are required conductor Sale specifications. \\
\hline Supply Voltage & \\
\hline Input Voltage & \\
\hline Operating Free Air Temperature Range & \(-55^{\circ} \mathrm{C}\) to + \\
\hline rage Temperature Range & \(-65^{\circ} \mathrm{C}\) to +150 \\
\hline
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{93L10/93L 16 (MIL)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(V_{\text {IH }}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & V \\
\hline l OH & High Level Output Voltage & & & -400 & \(\mu \mathrm{A}\) \\
\hline lOL & Low Level Output Current & & & 4.8 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathbf{s}}(\mathrm{H}) \\
& \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
& \hline
\end{aligned}
\] & Setup Time HIGH or LOW \(P_{n}\) to CP & \[
\begin{aligned}
& 75 \\
& 75 \\
& \hline
\end{aligned}
\] & & & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{h}}(\mathrm{H}) \\
& \mathrm{t}_{\mathrm{h}}(\mathrm{~L}) \\
& \hline
\end{aligned}
\] & Hold Time HIGH or LOW
\[
P_{n} \text { to } C P
\] & \[
\begin{aligned}
& 10 \\
& 10 \\
& \hline
\end{aligned}
\] & & & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
& \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
& \hline
\end{aligned}
\] & Setup Time HIGH or LOW \(\overline{\text { PE to CP }}\) & (Note 2)
53 & & & ns \\
\hline \[
\begin{aligned}
& t_{h}(H) \\
& t_{h}(L) \\
& \hline
\end{aligned}
\] & Hold Time HIGH or LOW \(\overline{\text { PE to } C P ~}\) & \[
\begin{gathered}
7.0 \\
\text { (Note 2) } \\
\hline
\end{gathered}
\] & & & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
& \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
& \hline
\end{aligned}
\] & Setup Time HIGH or LOW CEP or CET to CP & \[
\begin{gathered}
26 \\
\text { (Note 1) } \\
\hline
\end{gathered}
\] & & & ns \\
\hline \[
\begin{aligned}
& t_{h}(H) \\
& t_{h}(\mathrm{~L}) \\
& \hline
\end{aligned}
\] & Hold Time HIGH or LOW CEP or CET to CP & (Note 1) 10 & & & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{w}}(\mathrm{H}) \\
& \mathrm{t}_{\mathrm{w}}(\mathrm{~L}) \\
& \hline
\end{aligned}
\] & CP Pulse Width & \[
\begin{aligned}
& 25 \\
& 25
\end{aligned}
\] & & & ns \\
\hline \(t_{w}(L)\) & \(\overline{M R}\) Pulse Width LOW & 65 & & & ns \\
\hline \(\mathrm{t}_{\text {rec }}\) & Recovery Time, \(\overline{\text { MR }}\) to CP & 30 & & & ns \\
\hline
\end{tabular}

Note 1: The Setup Time " \(\mathrm{t}_{\mathrm{s}}(\mathrm{L})\) " and Hold Time "th \((\mathrm{H})\) " between the Count Enable (CEP and CET) and the Clock (CP) indicate that the HIGH-to-LOW transition of the CEP and CET must occur only while the Clock is HIGH for conventional operation.
Note 2: The Setup Time " \(\mathrm{t}_{\mathrm{s}}(\mathrm{H})\) " and Hold Time " \(\mathrm{t}_{\mathrm{h}}(\mathrm{L})\) " between the Parallel Enable ( \(\overline{\mathrm{PE}}\) ) and Clock (CP) indicate that the LOW-to-HIGH transition of the \(\overline{\mathrm{PE}}\) must occur only while the Clock is HIGH for conventional operation.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \begin{tabular}{l}
Typ \\
(Note 1)
\end{tabular} & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-10 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\mathrm{Max}, \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & & 0.3 & V \\
\hline 11 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{3}{*}{\({ }_{1 / \mathrm{H}}\)} & \multirow[t]{3}{*}{High Level Input Current} & \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & Inputs & & & 20 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & CET, CP, PE & & & 40 & \\
\hline & & & \(\mathrm{P}_{\mathrm{n}}\) & & & 13.3 & \\
\hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.3 \mathrm{~V}\)} & Inputs & & & -400 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & CET, CP, PE & & & -800 & \\
\hline & & & \(\mathrm{P}_{\mathrm{n}}\) & & & -267 & \\
\hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 2)} & -2.5 & & -25 & mA \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x\)} & & & 27.5 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

\section*{Switching Characteristics}
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\(C_{L}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \(f_{\text {max }}\) & Maximum Count Frequency & 13 & & MHz \\
\hline \begin{tabular}{l}
\(t_{\text {PLH }}\) \\
tpHL
\end{tabular} & Propagation Delay \(C P\) to \(Q\) & & \[
\begin{aligned}
& 32 \\
& 39
\end{aligned}
\] & ns \\
\hline \begin{tabular}{l}
\(t_{\text {PLH }}\) \\
\(t_{\text {PHL }}\)
\end{tabular} & Propagation Delay CP to TC & & \[
\begin{aligned}
& 66 \\
& 30 \\
& \hline
\end{aligned}
\] & ns \\
\hline \(t_{\text {PLH }}\)
\[
t_{\mathrm{PHL}}
\] & Propagation Delay CET to TC & & \[
\begin{aligned}
& 35 \\
& 30
\end{aligned}
\] & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay, \(\overline{\mathrm{MR}}\) to Q & & 72 & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The 93L10 counts modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) it increments to state 0 (LLLL). The 93L16 counts modulo-16 in binary sequence. From state 15 (HHHH) it increments to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset, parallel load, count-up and hold. Four control inputs-Master Reset (MR), Parallel Enable ( \(\overline{\mathrm{PE}}\) ), Count Enable Parallel (CEP) and Count Enable Trickle (CET)-determine the mode of operation, as shown in the Mode Select Table. A LOW signal on MR overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on \(\overline{\text { PE }}\) overrides counting and allows information on the Parallel Data \(\left(P_{n}\right)\) inputs to be loaded into the flip-flops on the next rising edge of CP. With \(\overline{P E}\) and \(\overline{M R}\) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.
The 93L10 and 93L16 contain masterslave flip-flops which are "next-state catching" because of the JK feedback. This means that when CP is LOW, information that would change the state of a flip-flop, whether from the counting logic or the parallel entry logic if either mode is momentarily enabled, enters the master and is locked in. Thus to avoid inadvertently changing the state of a master latch, and the subsequent transfer of the erroneous information to the slave when the clock rises, it is necessary to insure that neither the counting mode, nor the parallel entry mode is momentarily enabled while CP is LOW.
The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in its maximum count state ( 9 for the decade counters, 15 for the binary counters-fully decoded in both types). To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. These two schemes are shown in Figures \(a\) and \(b\). The TC output is subject to decoding
spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the state diagrams.

\section*{MULTISTAGE COUNTING}

The '10/‘'16 counters may be cascaded to provide multistage synchronous counting. Two methods commonly used to cascade these counters are shown in Figures \(a\) and \(b\).
In multistage counting, all less significant stages must be at their terminal count before the next more significant counter is enabled. The ' \(10 /\) ' 16 internally decodes the terminal count condition and "ANDs" it with the CET input to generate the terminal count (TC) output. This arrangement allows one to perform series enabling by connecting the TC output (enable signal) to the CET input of the following stage, Figure \(a\). The setup requires very few interconnections, but has the following drawback: since it takes time for the enable to ripple through the counter stages, there is a reduction in maximum counting speed. To increase the counting rate, it is necessary to decrease the propagation delay of the TC signal, which is done in the second method.
The scheme illustrated in Figure \(b\) permits multistage counting, limited by the fan-out of the terminal count. The CEP input of the ' \(10 /\) ' 16 is internally "ANDed" with the CET input and as a result, both must be HIGH for the counter to be enabled. The CET inputs are connected as before except for the second stage. There the CET input is left floating and is therefore HIGH. Also, all CEP inputs are connected to the terminal output of the first stage. The advantage of this method is best seen by assuming all stages except the second and last are in their terminal condition. As the second stage advances to its terminal count, an enable is allowed to trickle down to the last counter stage, but has the full cycle time of the first counter to reach it. Then as the TC of the first stage goes active (HIGH), all CEP inputs are activated, allowing all stages to count on the next clock.


93L16

\begin{tabular}{|c|c|c|c|c|c|}
\hline \multicolumn{5}{|c|}{Inputs} & \multirow[t]{2}{*}{Response} \\
\hline \(\overline{M R}\) & \(\overline{\text { PE }}\) & CEP & CET & CP & \\
\hline L & X & \(X\) & X & X & Clear; All Outputs LOW \\
\hline H & L & X & X & \(\checkmark\) & Parallel Load; \(P_{n} \rightarrow Q_{n}\) \\
\hline H & H & L & X & X & Hold \\
\hline H & H & X & L & X & Hold; TC = LOW \\
\hline H & H & H & H & \(\checkmark\) & Count Up \\
\hline
\end{tabular}
\(H=H I G H\) Voltage Level
\(L=\) LOW Voltage Level
\(X=\) Immaterial
Logic Equations
Count Enable \(=\) MR \(\bullet\) PE \(\cdot \mathrm{CEP} \cdot \mathrm{CET}\)
Terminal Count \(=\) CET \(\bullet\) Q0 \(\bullet\) Q1 \(\cdot\) Q2 \(\bullet\) Q3 ('16)
Terminal Count \(=\mathrm{CET} \cdot \mathrm{Q} 0 \bullet \overline{\mathrm{Q}} 1 \cdot \overline{\mathrm{Q}} 2 \cdot \mathrm{Q} 3(' 10)\)

\section*{State Diagrams}


\section*{93L12}

\section*{8-Input Multiplexer}

\section*{General Description}

The 93 L 12 is a monolithic, high speed, 8 -input digital multiplexer circuit. It provides, in one package, the ability to select one bit of data from up to eight sources. The 93L12 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

\section*{Connection Diagram}


TL/F/9610-1

\section*{Logic Symbol}

\(V_{C C}=\operatorname{Pin} 16\)
GND \(=\operatorname{Pin} 8\)

Order Number 93L12DMQB or 93L12FMQB
See NS Package Number J16A or W16A
\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
\hline S0-S2 & Select Inputs \\
\(\overline{\mathrm{E}}\) & Enable Input (Active LOW) \\
\(10-17\) & Multiplexer Inputs \\
\(\mathbf{Z}\) & Multiplexer Output \\
\(\overline{\mathbf{Z}}\) & Complementary Multiplexer Output \\
\hline
\end{tabular}

Absolute Maximum Ratings (Note)
If Milltary/Aerospace specifled devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
Operating Free Air Temperature Range
MIL
\(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
Storage Temperature Range \(\quad-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multirow{2}{|c|}{9} & \multicolumn{2}{|c|}{93 Parameter (MIL) } & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.7 & V \\
\hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -400 & \(\mu \mathrm{~A}\) \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 4.8 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) }
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-10 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\] & 2.4 & 3.4 & & V \\
\hline V \({ }_{\text {OL }}\) & Low Level Output Voltage & \[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\] & & & 0.3 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 20 & \(\mu \mathrm{A}\) \\
\hline 1 l & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.3 \mathrm{~V}\) & & & -400 & \(\mu \mathrm{A}\) \\
\hline los & Short Circuit Output Current & \(\mathrm{V}_{C C}=\operatorname{Max}\) ( Note 2) & -2.5 & & -25 & mA \\
\hline ICC & Supply Current & \(\mathrm{V}_{\text {CC }}=\operatorname{Max}\) (Note 3) & & & 13.3 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: ICC is measured with all outputs open and all inputs grounded.

\section*{Switching Characteristics}
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay S0 to Z & & \[
\begin{aligned}
& 60 \\
& 75 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay SO to Z & & \[
\begin{aligned}
& 70 \\
& 50 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& t_{\text {PLH }} \\
& t_{\text {tPHL }}
\end{aligned}
\] & Propagation Delay Eto Z & & \[
\begin{aligned}
& 60 \\
& 75 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
t_{P L H}
\]
\[
t_{\mathrm{PHL}}
\] & Propagation Delay \(\overline{\mathrm{E}}\) to \(\overline{\mathrm{Z}}\) & & \[
\begin{array}{r}
70 \\
45 \\
\hline
\end{array}
\] & ns \\
\hline \[
\begin{aligned}
& t_{\text {PLH }} \\
& t_{\text {PHL }} \\
& \hline
\end{aligned}
\] & Propagation Delay In to Z & & \[
\begin{aligned}
& 70 \\
& 65
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \text { tpLH } \\
& \mathrm{t}_{\mathrm{pHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay In to \(\overline{\mathbf{Z}}\) & & \[
\begin{aligned}
& 55 \\
& 55 \\
& \hline
\end{aligned}
\] & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The 93L12 is a logical implementation of a single pole, eight position switch with the switch position controlled by the state of three Select inputs, S0, S1, S2. Both assertion and negation outputs are provided. The Enable input ( E ) is active LOW. When it is not activated the negation output is HIGH and the assertion output is LOW, regardless of all other inputs. The logic function provided at the output is:
\(Z=E \cdot(10 \cdot \overline{\mathrm{~S} 0} \cdot \overline{\mathrm{~S}} 1 \bullet \overline{\mathrm{~S}} 2+\mathrm{I} 1 \cdot \mathrm{~S} 0 \cdot \overline{\mathrm{~S}} 1 \cdot \overline{\mathrm{~S}} 2\)
\[
\begin{aligned}
& +12 \cdot \overline{\mathrm{~S} 0 \cdot \mathrm{~S} 1 \bullet \overline{\mathrm{~S}} 2+13 \cdot \mathrm{~S} 0 \cdot \mathrm{~S} 1 \cdot \overline{\mathrm{~S} 2}} \begin{array}{l}
+14 \cdot \overline{\mathrm{~S} 0} \cdot \overline{\mathrm{~S}} 1 \cdot \mathrm{~S} 2+15 \cdot \mathrm{~S} 0 \cdot \overline{\mathrm{~S}} 1 \cdot \mathrm{~S} 2 \\
+16 \cdot \overline{\mathrm{~S} 0} \mathrm{~S} 1 \cdot \mathrm{~S} 2 \\
+17 \cdot \mathrm{~S} 0 \cdot \mathrm{~S} 1 \cdot \mathrm{~S} 2) .
\end{array}
\end{aligned}
\]

\section*{Truth Table}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{12}{|c|}{Inputs} & \multicolumn{2}{|l|}{Outputs} \\
\hline \(\bar{E}\) & S2 & S1 & so & 10 & 11 & 12 & 13 & 14 & 15 & 16 & 17 & \(\overline{\mathbf{Z}}\) & Z \\
\hline H & X & X & X & X & X & X & X & X & X & X & X & H & L \\
\hline L & L & L & L & L & X & X & X & X & X & X & X & H & L \\
\hline L & L & L & L & H & X & X & X & X & X & X & X & L & H \\
\hline L & L & \(L\) & H & X & L & X & X & X & X & X & X & H & L \\
\hline L & L & L & H & X & H & X & X & X & X & X & X & L & H \\
\hline L & L & H & L & X & X & L & X & X & X & X & X & H & L \\
\hline L & L & H & L & X & X & H & X & X & X & X & X & L & H \\
\hline L & L & H & H & X & X & X & L & X & X & X & X & H & L \\
\hline L & L & H & H & X & X & \(x\) & H & X & X & X & \(x\) & L & H \\
\hline L & H & L & L & X & X & X & X & L & X & X & X & H & L \\
\hline L & H & L & L & X & X & X & X & H & X & X & X & L & H \\
\hline L & H & L & H & X & X & X & X & \(x\) & L & X & X & H & L \\
\hline L & H & L & H & X & \(x\) & \(x\) & X & \(x\) & H & X & X & L & H \\
\hline L & H & H & L & X & X & X & X & \(x\) & X & L & X & H & L \\
\hline L & H & H & L & X & X & X & X & X & X & H & X & L & H \\
\hline L & H & H & H & X & X & X & X & \(x\) & X & X & L & H & L \\
\hline L & H & H & H & X & X & X & X & X & X & X & H & L & H \\
\hline
\end{tabular}

\footnotetext{
\(\mathrm{H}=\mathrm{HIGH}\) Voltage Level
\(L=\) LOW Voltage Level
\(\mathrm{X}=\) Immaterial
}


\section*{93L14 Quad Latch}

\section*{General Description}

The 93L14 is a multifunctional 4-bit latch designed for general purpose storage applications in high speed digital systems. All outputs have active pull-up circuitry to provide high capacitance drive and to provide low impedance in both logic states for good noise immunity.

\section*{Features}
- Can be used as single input D latches or set/reset latches
- Active low enable gate input
- Overriding master reset

\section*{Connection Diagram}

\section*{Dual-In-Line Package}


\section*{Logic Symbol}


TL/F/9612-1
Order Number 93L14DMQB or 93L14FMQB
See NS Package Number J16A or W16A
\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{c|}{ Description } \\
\hline \(\bar{E}\) & Enable Input (Active LOW) \\
D0-D3 & Data Inputs \\
\(\bar{S} 0-\overline{S 3} 3\) & Set Inputs (Active LOW) \\
\(\overline{M R}\) & Master Reset Input (Active LOW) \\
Q0-Q3 & Latch Outputs \\
\hline
\end{tabular}
```

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for availability and specifications.
Supply Voltage 7V
Input Voltage 5.5V
Operating Free Air Temperature Range
MIL $\quad-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
Storage Temperature Range $\quad-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

```

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{93 L 14 (MIL)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.7 & V \\
\hline \(\mathrm{IOH}^{\text {l }}\) & High Level Output Voltage & & & -400 & \(\mu \mathrm{A}\) \\
\hline lOL & Low Level Output Current & & & 4.8 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
& \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
& \hline
\end{aligned}
\] & Setup Time HIGH or LOW \(D_{n}\) to \(\bar{E}\) & \[
\begin{aligned}
& 10 \\
& 20 \\
& \hline
\end{aligned}
\] & & & ns \\
\hline \[
\begin{aligned}
& t_{h}(H) \\
& t_{h}(L) \\
& \hline
\end{aligned}
\] & Hold Time HIGH or LOW \(D_{n}\) to \(\bar{E}\) & \[
\begin{gathered}
0 \\
10 \\
\hline
\end{gathered}
\] & & & ns \\
\hline \(t_{s}(\mathrm{H})\) & Setup Time HIGH, \(\mathrm{D}_{\mathrm{n}}\) to \(\bar{S}_{n}\) & 15 & & & ns \\
\hline \(t_{n}(L)\) & Hold Time LOW, \(\mathrm{D}_{\mathrm{n}}\) to \(\bar{S}_{\mathrm{n}}\) & 5 & & & ns \\
\hline \(t_{w}(L)\) & E Pulse Width LOW & 30 & & & ns \\
\hline \(t_{w}(L)\) & \(\overline{M R}\) Pulse Width LOW & 25 & & & ns \\
\hline \(t_{\text {rec }}\) & Recovery Time, \(\overline{\mathrm{MR}}\) to \(\overline{\mathrm{E}}\) & 5 & & & ns \\
\hline
\end{tabular}

Electrical Characteristics
Over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, l_{1}=-10 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=M i n, I_{O H}=M a x, \\
& V_{I L}=M a x, V_{I H}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & & & V \\
\hline VOL & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\]} & & & 0.3 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{2}{*}{\(\mathrm{I}_{\mathrm{H}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & Inputs & & & 20 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & \(\mathrm{D}_{\mathrm{n}}\) & & & 30 & \\
\hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\(V_{C C}=M a x, V_{1}=0.3 V\)} & Inputs & & & -400 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & \(\mathrm{D}_{\mathrm{n}}\) & & & -600 & \\
\hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Max} \\
& \text { (Note 2) }
\end{aligned}
\]} & -2.5 & & -25 & mA \\
\hline lcc & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\) (Note 3)} & & & 16.5 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: Icc is measured with all outputs open and all inputs grounded.

\section*{Switching Characteristics}
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\(C_{L}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \[
t_{\text {PLH }}
\]
\[
\mathrm{t}_{\mathrm{PHL}}
\] & Propagation Delay \(\bar{E}\) to \(Q_{n}\) & & \[
\begin{aligned}
& 45 \\
& 36 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay
\[
D_{n} \text { to } Q_{n}
\] & & \[
\begin{aligned}
& 30 \\
& 30 \\
& \hline
\end{aligned}
\] & ns \\
\hline \(t_{\text {PLH }}\) & Propagation Delay, \(\overline{M R}\) to \(Q_{n}\) & & 30 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay, \(\bar{S}_{n}\) to \(Q_{n}\) & & 33 & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The 93L14 consists of four latches with a common active LOW Enable input and active LOW Master Reset input. When the Enable goes HIGH, data present in the latches is stored and the state of the latch is no longer affected by the \(\bar{S}_{n}\) and \(D_{n}\) inputs. The Master Reset when activated overrides all other input conditions forcing all latch outputs LOW. Each of the four latches can be operated in one of two modes:
D-TYPE-LATCH-For D-type operation the \(\overline{\mathrm{S}}\) input of a latch is held LOW. While the common Enable is active the latch output follows the D input. Information present at the latch output is stored in the latch when the Enable goes HIGH.
SET/RESET LATCH—During set/reset operation when the common Enable is LOW a latch is reset by a LOW on the D input, and can be set by a LOW on the \(\overline{\mathrm{S}}\) input if the D input is HIGH. If both \(\bar{S}\) and \(D\) inputs are LOW, the \(D\) input will dominate and the latch wil be reset. When the Enable goes HIGH, the latch remains in the last state prior to disablement. The two modes of latch operation are shown in the Truth Table.

Truth Table
\begin{tabular}{|l|c|c|c|c|l|}
\hline\(\overline{M R}\) & \(\overline{\mathbf{E}}\) & \(\mathbf{D}\) & \(\overline{\mathbf{S}}\) & \(\mathbf{Q}_{\mathbf{n}}\) & Operation \\
\hline\(H\) & \(L\) & \(L\) & \(L\) & \(L\) & D Mode \\
\(H\) & \(L\) & \(H\) & \(L\) & \(L\) & \\
\(H\) & \(H\) & \(X\) & \(X\) & \(Q_{\mathrm{n}-1}\) & \\
\hline\(H\) & \(L\) & \(L\) & \(L\) & \(L\) & R/S Mode \\
\(H\) & \(L\) & \(H\) & \(L\) & \(H\) & \\
\(H\) & \(L\) & \(L\) & \(H\) & \(L\) & \\
\(H\) & \(L\) & \(H\) & \(H\) & \(Q_{n-1}\) & \\
\(H\) & \(H\) & \(X\) & \(X\) & \(Q_{n-1}\) & \\
\hline\(L\) & \(X\) & \(X\) & \(X\) & \(L\) & RESET \\
\hline
\end{tabular}
\(H=H I G H\) Voltage Level
L = LOW Voltage Leve!
\(x=\) Immaterial
\(Q_{n-1}=\) Previous Output State
\(Q_{n}=\) Present Output State

\section*{Logic Diagram}


\section*{93L21}

\section*{Dual 1-of-4 Decoder}

\section*{General Description}

The 93L21 consists of two independent multipurpose decoders, each designed to accept two inputs and provide four mutually exclusive outputs. In addition an active LOW enable input, which gives demultiplexing capability, is provided for each decoder.

\section*{Features}
- Multifunction capability
- Mutually exclusive outputs
- Demultiplexing capability
- Active low enable for each decoder

\section*{Logic Symbol}

\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Pin} 16 \\
& \mathrm{GND}=\operatorname{Pin} 8
\end{aligned}
\]


TL/F/10197-1
Order Number 93L21DMQB or 93L21FMQB
See NS Package Number J16A or W16A
\begin{tabular}{|c|c|}
\hline Pin Names & Description \\
\hline Ea, Eb & Enable Inputs (Active LOW) \\
\hline A0a, A1a, A0b, A1b & Address Inputs \\
\hline \[
\overline{0} 0 a-\overline{0} 3 a\}
\] & Decoder Outputs (Active LOW) \\
\hline
\end{tabular}

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
7V
Input Voltage
5.5 V

Operating Free Air Temperature Range
\(\begin{array}{cl}\text { MIL } & -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\ \text { Storage Temperature Range } & -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C}\end{array}\)

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{93 L 12 (MIL)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & V \\
\hline IOH & High Level Output Current & & & -400 & \(\mu \mathrm{A}\) \\
\hline lOL & Low Level Output Current & & & 4.8 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(V_{C C}=M i n, I I=-10 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\] & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\text { Max }, \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & & & 0.3 & V \\
\hline II & Input Current @ Max Input Voltage & \(\mathrm{V}_{\text {CC }}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline IIH & High Level Input Current & \(V_{C C}=M a x, V_{l}=2.4 \mathrm{~V}\) & & & 20 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \(V_{C C}=M a x, V_{1}=0.3 V\) & & & -400 & \(\mu \mathrm{A}\) \\
\hline los & Short Circuit Output Current & \[
\begin{aligned}
& V_{C C}=\text { Max } \\
& \text { (Note 2) }
\end{aligned}
\] & -2.5 & & -25 & mA \\
\hline ICC & Supply Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 3) & & & 13.2 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: ICC is measured with all outputs open and all inputs grounded.

\section*{Functional Description}

The 93L21 consists of two separate decoders each designed to accept two binary weighted inputs and provide four mutually exclusive active LOW outputs as shown in the logic symbol. Each decoder can be used as a 4-output demultiplexer by using the enable as a data input.

Truth Table (Each Decoder)
\begin{tabular}{|c|cc|cccc|}
\hline \multicolumn{3}{|c|}{ Inputs } & \multicolumn{4}{c|}{ Outputs } \\
\hline\(\overline{\text { E }}\) & A0 & A1 & \(\overline{\mathbf{O} 0}\) & \(\overline{\mathbf{O} 1}\) & \(\overline{\mathbf{O} 2}\) & \(\overline{\mathbf{O} 3}\) \\
\hline L & L & L & L & H & H & H \\
L & H & L & H & L & H & H \\
L & L & H & H & H & L & H \\
L & H & H & H & H & H & L \\
H & X & X & H & H & H & H \\
\hline
\end{tabular}
\(H=H I G H\) Voltage Level
L = LOW Voltage Level
\(X=\) Immaterial

\section*{Logic Diagram}


Switching Characteristics \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for test waveforms and output load.)
\begin{tabular}{c|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multirow{2}{*}{ Parameter } & \multicolumn{2}{|c|}{\(\mathbf{C}_{\mathbf{L}}=15 \mathrm{pF}\)} & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & \multirow{2}{*}{ Max } & \multirow{2}{*}{ns} \\
\hline tPLH & Propagation Delay & & 50 & 65 \\
tPHL & An to \(\overline{\mathrm{O}} \mathrm{n}\) & & 40 & \multirow{2}{*}{ns} \\
\hline tPLH & Propagation Delay & & 52 & \\
\hline tPHL & En to \(\overline{\mathrm{O}} \mathrm{n}\) & & \\
\hline
\end{tabular}

\section*{93L22}

\section*{Quad 2-Input Multiplexer}

\section*{General Description}

The 93L22 quad 2-input digital multiplexers consist of four multiplexing circuits with common select and enable logic; each circuit contains two inputs and one output.

\section*{Connection Diagram}


Features
- Multifunction capability

■ On-chip select logic decoding
- Fully buffered outputs

\section*{Logic Symbol}


TL/F/10198-2
\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Pin} 16 \\
& \mathrm{GND}=\operatorname{Pin} 8
\end{aligned}
\]

\section*{Truth Table}
\begin{tabular}{|c|c|c|c|c|}
\hline \multicolumn{5}{|c|}{ Inputs } \\
\hline E & S & IOn & IIn & Zn \\
\hline H & X & X & X & L \\
L & H & X & L & L \\
L & H & X & H & H \\
L & L & L & X & L \\
L & L & H & X & H \\
\hline
\end{tabular}

\footnotetext{
H \(=\) HIGH Voltage Level
L = LOW Voltage Level
\(X=\) Immaterial
}
\begin{tabular}{l} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage \\
Input Voltage \\
Operating Free Air Temperature Range \\
MIL \\
Storage Temperature Range \\
R \\
\hline
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{93 L 22 (MIL)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & V \\
\hline \(\mathrm{IOH}^{\text {l }}\) & High Level Output Current & & & -400 & \(\mu \mathrm{A}\) \\
\hline lOL & Low Level Output Current & & & 4.8 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ
(Note 1) & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \(V_{C C}=\operatorname{Min}, l_{l}=-10 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\] & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
\begin{aligned}
& V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max}, \\
& V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
\end{aligned}
\] & & & 0.3 & V \\
\hline II & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline IIH & High Level Input Current & \(V_{C C}=\) Max, \(V_{1}=2.4 \mathrm{~V}\) & & & 20 & \(\mu \mathrm{A}\) \\
\hline \(1 / 2\) & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.3 \mathrm{~V}\) & & & -400 & \(\mu \mathrm{A}\) \\
\hline los & Short Circuit Output Current & \(\mathrm{V}_{\text {CC }}=\) Max, (Note 2) & -2.5 & & -25 & mA \\
\hline ICC & Supply Current & \(V_{C C}=\operatorname{Max}\) & & & 13.2 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

\section*{Switching Characteristics}
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for test waveforms and output load)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \begin{tabular}{l}
tPLH \\
tPHL
\end{tabular} & Propagation Delay S to Zn & & \[
\begin{aligned}
& 36 \\
& 49
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{tPLH} \\
& \mathrm{tPHL}
\end{aligned}
\] & Propagation Delay 10 or l1 to Zn & & \[
\begin{aligned}
& 30 \\
& 22
\end{aligned}
\] & ns \\
\hline \begin{tabular}{l}
tPLH \\
tPHL
\end{tabular} & Propagation Delay \(\bar{E}\) to Zn & & \[
\begin{aligned}
& 27 \\
& 27
\end{aligned}
\] & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The 93L22 quad 2-input multiplexer provides the ability to select four bits of either data or control from two sources, in one package. The Enable input ( \(\overline{\mathrm{E}}\) ) is active LOW. When not activated all outputs \(\left(Z_{n}\right)\) are LOW regardless of all other inputs.
The 93L22 quad 2-input multiplexer is the logical implementation of a four-pole, two position switch, with the position of the switch being set by the logic levels supplied to the one select input. The logic equations for the outputs are shown below:
\(\mathrm{Za}=\mathrm{E} \cdot(11 \mathrm{a} \bullet \mathrm{S}+10 \mathrm{a} \bullet \overline{\mathrm{S}}) \quad \mathrm{Zb}=\mathrm{E} \bullet(11 \mathrm{~b} \cdot \mathrm{~S}+10 \mathrm{~b} \bullet \overline{\mathbf{S}})\)
\(\mathrm{Zc}=\mathrm{E} \bullet(11 \mathrm{c} \bullet \mathrm{S}+10 \mathrm{c} \bullet \overline{\mathrm{S}}) \quad \mathrm{Zd}=\mathrm{E} \bullet(11 \mathrm{~d} \bullet \mathrm{~S}+10 \mathrm{~d} \bullet \overline{\mathrm{~S}})\)

A common use of the 93L22 is the moving of data from a group of registers to four common output busses. The particular register from which the data comes is determined by the state of the select input. A less obvious use is as a function generator. The 93L22 can generate four functions of two variables with one variable common. This is useful for implementing random gating functions.

\section*{Logic Diagram}


TL/F/10198-3

National Semiconductor

\section*{93L24}

\section*{5-Bit Comparator}

\section*{General Description}

The 93L24 expandable comparator provides comparison between two 5 -bit words and gives three outputs-'less than", "greater than" and "equal to". A HIGH on the active LOW Enable Input forces all three outputs LOW.

\section*{Connection Diagram}


\section*{Logic Symbol}

\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Pin} 16 \\
& \mathrm{GND}=\operatorname{Pin} 8
\end{aligned}
\]

TL/F/10199-1
Order Number 93L24DMQB or 93L24FMQB
See NS Package Number J16A or W16A
\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
\hline \(\bar{E}\) & Enable Input (Active LOW) \\
AO-A4 & Word A Parallel Inputs \\
B0-B4 & Word B Parallel Inputs \\
A \(<B\) & A Less than B Output (Active HIGH) \\
\(A>B\) & A Greater than B Output (Active HIGH) \\
\(A=B\) & A Equal to B Output (Active HIGH) \\
\hline
\end{tabular}

\section*{Truth Table}
\begin{tabular}{|ccc|ccc|}
\hline \multicolumn{3}{|c|}{ Inputs } & \multicolumn{3}{c|}{ Outputs } \\
\hline \(\bar{E}\) & An & Bn & A < B & A>B & A=B \\
\hline H & X & X & L & L & L \\
L & Word A \(=\) Word B & L & L & H \\
L & Word A > Word B & L & H & L \\
L & Word B \(~\) Word A & H & L & L \\
\hline
\end{tabular}

\footnotetext{
H \(=\) HIGH Voltage Level
\(L=\) LOW Voltage Level
\(X=\) Immaterial
}

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Input Voltage
5.5 V

Operating Free Air Temperature Range
\(\begin{array}{cl}\text { MIL } & -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\ \text { Storage Temperature Range } & -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C}\end{array}\)

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multirow{2}{|c|}{ Parameter } & \multicolumn{2}{c|}{ 93L24 (MIL) } & \multirow{2}{*}{ Units } \\
\cline { 3 - 4 } & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.7 & V \\
\hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -400 & mA \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 4.8 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & \begin{tabular}{l}
Typ \\
(Note 1)
\end{tabular} & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(V_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-10 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\] & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & & & 0.3 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{I}_{\mathrm{IH}}\) & High Level Input Current & \(V_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
\hline I/L & Low Level Input Current & \(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=0.3 \mathrm{~V}\) & & & -0.8 & mA \\
\hline los & Short Circuit Output Current & \(V_{C C}=\operatorname{Max}\) (Note 2) & -2.5 & & -25 & mA \\
\hline ICC & Supply Current & \(V_{C C}=\operatorname{Max}\) & & & 21 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

\section*{Switching Characteristics}
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for test waveforms and output load)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& t_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & \begin{tabular}{l}
Propagation Delay \\
\(\bar{E}\) to \(A=B ; \bar{E}\) to \(A<B, A>B\)
\end{tabular} & & \[
\begin{aligned}
& 32 \\
& 35 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & \begin{tabular}{l}
Propagation Delay \\
An to A>B;Bn to A>B
\end{tabular} & & \[
\begin{aligned}
& 54 \\
& 75 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & \begin{tabular}{l}
Propagation Delay \\
An to A<B;Bn to A \(<B\)
\end{tabular} & & \[
\begin{aligned}
& 70 \\
& 77 \\
& \hline
\end{aligned}
\] & ns \\
\hline \(t_{\text {PLH }}\) \(t_{\text {PHL }}\) & Propagation Delay An or \(B n\) to \(A=B\) & & \[
\begin{aligned}
& 100 \\
& 102
\end{aligned}
\] & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The 93L24 5-bit comparators use combinational circuitry to directly generate "A greater than \(B\) " and " \(A\) less than \(B\) " outputs. As evident from the logic diagram, these ouptuts are generated in only three gate delays. The "A equals \(B\) " output is generated in one additional gate delay by decoding the "A neither less than nor greater than B " condition with a NOR gate. All three outputs are activated by the active LOW Enable Input ( \(\overline{\mathrm{E}}\) ).

Tying the \(A>B\) output from one device into an \(A\) input on another device and the \(A<B\) output into the corresponding \(B\) input permits easy expansion.
The A4 and B4 inputs are the most significant inputs and AO, B0 the least significant. Thus if A4 is HIGH and B4 is LOW, the \(A>B\) output will be HIGH regardless of all other inputs except \(\bar{E}\).

\section*{Logic Diagram}


TL/F/10199-3

\section*{National Semiconductor}

\section*{93L28}

\section*{Dual 8－Bit Shift Register}

\section*{General Description}

The 93L28 is a high speed serial storage element providing 16 bits of storage in the form of two 8 －bit registers．The multifunctional capability of this device is provided by sever－ al features：1）additional gating is provided at the input to both shift registers so that the input is easily multiplexed between two sources；2）the clock of each register may be provided separately or together；3）both the true and com－ plementary outputs are provided from each 8 －bit register， and both registers may be master cleared from a common input．

\section*{Connection Diagram}


TL／F／10200－1
Order Number 93L28DMQB or 93L28FMQB See NS Package Number J16A or W16A

\section*{Features}
－2－input multiplexer provided at data input of each register
－Gated clock input circuitry
凹 Both true and complementary outputs provided from last bit of each register
四 Asynchronous master reset common to both registers
 Logic Symbol


TL／F／10200－2
\(V_{C C}=\operatorname{Pin} 16\)
GND \(=\operatorname{Pin} 8\)
\begin{tabular}{|l|l|}
\hline \begin{tabular}{c} 
Pin \\
Names
\end{tabular} & \multicolumn{1}{c|}{ Description } \\
\hline S & Data Select Input \\
D0，D1 & Data Inputs \\
CP & Clock Pulse Input（Active HIGH） \\
& Common（Pin 9） \\
& Separate（Pins 7 and 10） \\
\(\overline{\text { MR }}\) & Master Reset Input（Active LOW） \\
Q7 & Last Stage Output \\
\(\overline{\text { Q } 7 ~}\) & Complementary Output \\
\hline
\end{tabular}
```

Absolute Maximum Ratings (Note)
If Milltary/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for avallability and specifications.
Supply Voltage
Input Voltage 5.5V
Operating Free Air Temperature Range
MIL - 55 ' to +125}\mp@subsup{}{}{\circ}\textrm{C
Storage Temperature Range -65 C to +150 %

```

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{\(93 \mathrm{L28}\) (MIL)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & \\
\hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & V \\
\hline \({ }_{\mathrm{OH}}\) & High Level Output Current & & & -400 & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{lOL}^{\text {L }}\) & Low Level Output Current & & & 4.8 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
& \mathrm{t}_{\mathrm{s}}(\mathrm{~L})
\end{aligned}
\] & Setup Time HIGH or LOW \(D_{n}\) to CP & \[
\begin{aligned}
& 30 \\
& 30 \\
& \hline
\end{aligned}
\] & & & ns \\
\hline \[
\begin{aligned}
& t_{h}(H) \\
& t_{h}(\mathrm{~L}) \\
& \hline
\end{aligned}
\] & Hold Time HIGH or LOW
\[
D_{n} \text { to } C P
\] & \[
\begin{aligned}
& 0 \\
& 0 \\
& \hline
\end{aligned}
\] & & & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{w}}(\mathrm{H}) \\
& \mathrm{t}_{\mathrm{w}}(\mathrm{~L}) \\
& \hline
\end{aligned}
\] & Clock Pulse Width HIGH or LOW & \[
\begin{aligned}
& 55 \\
& 55 \\
& \hline
\end{aligned}
\] & & & ns \\
\hline \(t_{w}(L)\) & \(\overline{\text { MR Pulse Width with CP HIGH }}\) & 60 & & & ns \\
\hline \(t_{\text {w }}(\mathrm{L})\) & \(\overline{M R}\) Pulse Width with CP LOW & 70 & & & ns \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M i n, l_{I}=-10 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\text { Max }, \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & & & 0.3 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{4}{*}{\(\mathrm{IIH}^{\text {H}}\)} & \multirow[t]{4}{*}{HIGH Level Input Current} & \multirow[t]{4}{*}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & MR, Dx & & & 20 & \multirow{4}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & \(C P(7,10)\) & & & 30 & \\
\hline & & & S & & & 40 & \\
\hline & & & CP Com & & & 60 & \\
\hline \multirow[t]{4}{*}{IIL} & \multirow[t]{4}{*}{LOW Level Input Current} & \multirow[t]{4}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.3 \mathrm{~V}\)} & \(\overline{\mathrm{MR}}, \mathrm{Dx}\) & & & -400 & \multirow{4}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & \(C P(7,10)\) & & & -600 & \\
\hline & & & S & & & -800 & \\
\hline & & & CP Com & & & -1200 & \\
\hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=M a x \\
& \text { (Note 2) } \\
& \hline
\end{aligned}
\]} & -2.5 & & -25 & mA \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & & 25.3 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Switching Characteristics
\(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for test waveforms and output load)
\begin{tabular}{c|l|c|c|c}
\hline \multirow{2}{*}{ Symbol } & \multicolumn{2}{|c|}{ Parameter } & \multicolumn{2}{|c}{\(\mathrm{C}_{\mathrm{L}}=\mathbf{1 5 F}\)} \\
\cline { 3 - 4 } & & Min & \multirow{2}{*}{ Units } \\
\hline \(\mathrm{f}_{\text {max }}\) & Maximum Shift Right Frequency & 5.0 & & \\
\hline \(\mathrm{t}_{\mathrm{PLH}}\) & Propagation Delay & & 45 & MHz \\
\(\mathrm{t}_{\mathrm{PHL}}\) & CP to \(\mathrm{Q}_{7}\) or \(\bar{Q}_{7}\) & & 80 & ns \\
\hline \(\mathrm{t}_{\mathrm{PHL}}\) & Propagation Delay \(\overline{\mathrm{MR}}\) to \(\mathrm{Q}_{7}\) & & 110 & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The two 8 -bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 and 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master/slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flops in parallel. When the two clock inputs (the separate and the common) to the OR gate are LOW, the slave latches are steady, but data can enter the master latches via the \(R\) and \(S\) input. During the first LOW-to-HIGH transition of either, or both simultaneously, of the two clock inputs, the data inputs ( R and S ) are inhibited so that a later change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain HIGH. During the HIGH-to-LOW transition of the last remaining HIGH clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state. The data inputs ( R and S ) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic HIGH signal.

Each 8-bit shift register has a 2-input multiplexer in front of the serial data input. The two data inputs D0 and D1 are controlled by the data select input ( S ) following the Boolean expression:
Serial data in: \(S_{D}=\) SD0 + SD1
An asynchronous master reset is provided which, when activated by a LOW logic level, will clear all 16 stages independently of any other input signal.

Shift Select Table
\begin{tabular}{|c|c|c|c|}
\hline \multicolumn{3}{|c|}{ Inputs } & Output \\
\hline S & DO & D1 & Q7 ( \(\left.t_{n+8}\right)\) \\
\hline L & L & X & L \\
L & H & X & H \\
H & X & L & L \\
H & X & H & H \\
\hline
\end{tabular}

\footnotetext{
\(\mathrm{H}=\mathrm{HIGH}\) Voltage Level
L = LOW Voltage Level
\(\mathrm{X}=\) Immaterial
\(\mathrm{n}+8=\) Indicates state after eight clock pulse
}

\section*{Logic Diagram}


\section*{93L34}

\section*{8-Bit Addressable Latch}

\section*{General Description}

The 93L34 is an 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level HIGH outputs. The device also incorporates an active LOW common clear for resetting all latches, as well as, an active LOW enable.

\section*{Features}

■ Serial to parallel capability
■ Eight bits of storage with output of each bit available
- Random (addressable) data entry

龱 Active high demultiplexing or decoding capability
- Easily expandable
- Common conditional clear

\section*{Connection Diagram}

Dual-In-Line Package


\section*{Logic Symbol}


TL/F/10201-2
\[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Pin} 16 \\
& \mathrm{GND}=\operatorname{Pin} 8
\end{aligned}
\]

Order Number 93L34DMQB or 93L34FMQB
See NS Package Number J16A or W16A
\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
\hline A0-A3 & Address Inputs \\
\(\bar{D}\) & Data Input \\
\(\bar{E}\) & Enable Input (Active LOW) \\
\(\overline{C L}\) & Clear Input (Active LOW) \\
Q0-Q7 & Parallel Latch Outputs \\
\hline
\end{tabular}
\begin{tabular}{|c|c|}
\hline \multicolumn{2}{|l|}{Absolute Maximum Ratings (Note)} \\
\hline If Military/Aerospace specified device please contact the National Sem Office/Distributors for availability and & ces are required, conductor Sales specifications. \\
\hline Supply Voltage & \\
\hline Input Voltage & 5.5 V \\
\hline Operating Free Air Temperature Range Military & \(-55^{\circ} \mathrm{C}\) to +125 \\
\hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to + \\
\hline
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{93 L 34 (Mil)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & V \\
\hline IOH & High Level Output Voltage & & & -400 & \(\mu \mathrm{A}\) \\
\hline lOL & Low Level Output Current & & & 4.8 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline \(\mathrm{t}_{\mathrm{s}}(\mathrm{H})\) & Setup Time HIGH, D to \(\bar{E}\) & 45 & & & ns \\
\hline \(t_{h}(H)\) & Hold Time HIGH, D to \(\bar{E}\) & -5 & & & ns \\
\hline \(t_{\text {s }}(\mathrm{L})\) & Setup Time LOW, D to \(\bar{E}\) & 45 & & & ns \\
\hline \(t_{h}(L)\) & Hold Time LOW, D to E & -7 & & & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
& \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
& \hline
\end{aligned}
\] & Setup Time HIGH or LOW \(A_{n}\) to \(\bar{E}\) & \[
\begin{aligned}
& 10 \\
& 10 \\
& \hline
\end{aligned}
\] & & & ns \\
\hline \(t_{w}(L)\) & Ė Pulse Width LOW & 26 & & & ns \\
\hline \(t_{w}(L)\) & \(\overline{\text { CL Pulse Width LOW }}\) & 35 & & & ns \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-10 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & 2.4 & & & V \\
\hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
\begin{aligned}
& V_{C C}=M i n, I_{O L}=M a x, \\
& V_{I H}=M i n, V_{I L}=M a x
\end{aligned}
\]} & & & 0.3 & V \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
\hline \multirow[t]{2}{*}{\(\mathrm{I}_{\mathrm{H}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{C C}=\) Max, \(\mathrm{V}_{1}=2.4 \mathrm{~V}\)} & Inputs & & & 20 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & E & & & 30 & \\
\hline \multirow[t]{2}{*}{I/L} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.3 \mathrm{~V}\)} & Inputs & & & -0.4 & \multirow[t]{2}{*}{mA} \\
\hline & & & E & & & -0.6 & \\
\hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 2)} & -2.5 & & -25 & mA \\
\hline Icc & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\) (Note 3)} & & & 21 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: Icc is measured with all outputs open and all inputs grounded.

Switching Characteristics \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \[
\begin{aligned}
& t_{\mathrm{pLH}} \\
& t_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay \(\bar{E}\) to \(Q_{n}\) & & \[
\begin{aligned}
& 45 \\
& 42 \\
& \hline
\end{aligned}
\] & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay \(D\) to \(Q_{n}\) & & \[
\begin{aligned}
& 65 \\
& 45 \\
& \hline
\end{aligned}
\] & ns \\
\hline \begin{tabular}{l}
\(t_{\text {PLH }}\) \\
\(t_{\text {PHL }}\)
\end{tabular} & Propagation Delay \(A_{n}\) to \(Q_{n}\) & & \[
\begin{aligned}
& 66 \\
& 66
\end{aligned}
\] & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay \(\overline{C L}\) to \(Q_{n}\) & & 55 & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The 93L34 has four modes of operation which are shown in the Mode Select Table. In the addressable latch mode, data on the data line ( D ) is written into the addressed latch. The addressed latch will follow the Data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the Enable should be held HIGH while the Address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the state of the \(D\) input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs. When operating the 93L34 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.
\begin{tabular}{|l|l|l|}
\multicolumn{3}{c|}{ Mode Select Table } \\
\hline \(\bar{E}\) & \(\overline{C L}\) & \multicolumn{1}{|c|}{ Mode } \\
\hline L & H & Addressable Latch \\
\(H\) & H & Memory \\
L & L & Active HIGH 8-Channel Demultiplexer \\
\(H\) & L & Clear \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{5}{|c|}{Inputs} & \multicolumn{8}{|c|}{Outputs} & \multirow[t]{2}{*}{Mode} \\
\hline \(\overline{C L}\) & \(\bar{E}\) & A0 & A1 & A2 & Q0 & Q1 & Q2 & Q3 & Q4 & Q5 & Q6 & Q7 & \\
\hline L & H & X & X & X & L & L & L & L & L & L & L & L & Clear \\
\hline L & L & L & L & L & D & L & L & L & L & L & L & L & Demultiplex \\
\hline L & L & H & L & L & L & D & L & L & L & L & L & L & \\
\hline L & L & L & H & L & L & L & D & L & L & L & L & L & \\
\hline - & - & - & \(\bullet\) & - & \(\bullet\) & - & - & - & - & - & - & - & \\
\hline \(\bullet\) & \(\bullet\) & \(\bullet\) & \(\bullet\) & \(\bullet\) & \(\bullet\) & \(\bullet\) & \(\bullet\) & \(\bullet\) & \(\bullet\) & \(\bullet\) & \(\bullet\) & \(\bullet\) & \\
\hline L & L & H & H & H & L & L & L & L & L & L & L & L & \\
\hline H & H & X & X & X & Qt-1 & Qt-1 & Qt-1 & Qt-1 & Qt-1 & Qt-1 & Qt-1 & Qt-1 & Memory \\
\hline H & L & L & L & L & D & Qt-1 & Qt-1 & Qt-1 & Qt-1 & Qt-1 & Qt-1 & Qt-1 & Addressable \\
\hline H & L & H & L & L & Qt-1 & D & Qt-1 & Qt-1 & Qt-1 & Qt-1 & Qt-1 & Qt-1 & Latch \\
\hline H & L & L & H & L & Qt-1 & Qt-1 & D & Qt-1 & Qt-1 & Qt-1 & Qt-1 & Qt-1 & \\
\hline - & - & - & - & - & \(\bullet\) & - & - & & - & - & & & \\
\hline - & - & \(\bullet\) & \(\bullet\) & \(\bullet\) & \(\bullet\) & - & - & - & - & - & & - & \\
\hline H & L & H & H & H & Qt-1 & Qt-1 & Qt-1 & Qt-1 & Qt-1 & Qt-1 & Qt-1 & D & \\
\hline
\end{tabular}

\section*{Logic Diagram}


\section*{93L38}

\section*{8-Bit Multiple Port Register}

\section*{General Description}

The 93L38 is an 8-bit multiple port register designed for high speed random access memory applications where the ability to simultaneously read and write is desirable. A common use would be as a register bank in a three address computer. Data can be written into any one of the eight bits and read from any two of the eight bits simultaneously. The circuit uses TTL technology and is compatible with all TTL families.

\section*{Features}
- Master/slave operation permitting simultaneous write/ read without race problems
- Simultaneously read two bits and write one bit in any one of eight bit positions
- Readily expandable to allow for larger word sizes

\section*{Connection Diagram}


TL/F/10202-
Order Number 93L38DMQB or 93L38FMQB
See NS Package Number J16A or W16A

\section*{Logic Symbol}


TL/F/10202-2
\(V_{C C}=\operatorname{Pin} 16\)
GND \(=\operatorname{Pin} 8\)
\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
\hline AO-A2 & Write Address Inputs \\
DA & Data Input \\
BO-B2 & B Read Address Inputs \\
CO-C2 & C Read Address Inputs \\
CP & Clock Pulse Input (Active Rising Edge) \\
SLE & Slave Enable Input (Active LOW) \\
ZB & B Output \\
ZC & C Output \\
\hline
\end{tabular}
Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for availability and specifications.
\begin{tabular}{lr} 
Supply Voltage & 7 V \\
Input Voltage & 5.5 V \\
Operating Free Air Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
Military & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular} Storage Temperature Range

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{93 L 38 (MIL)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & v \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & V \\
\hline \(\mathrm{IOH}^{\text {O }}\) & High Level Output Current & & & -400 & \(\mu \mathrm{A}\) \\
\hline loL & Low Level Output Current & & & 4.8 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
& \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
& \hline
\end{aligned}
\] & \[
\begin{aligned}
& \text { Setup Time HIGH or LOW } \\
& \mathrm{D}_{\mathrm{A}} \text { to } \mathrm{CP}
\end{aligned}
\] & \[
\begin{array}{r}
30 \\
22 \\
\hline
\end{array}
\] & & & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{h}}(\mathrm{H}) \\
& \mathrm{th}_{\mathrm{h}}(\mathrm{~L}) \\
& \hline
\end{aligned}
\] & Hold Time HIGH or LOW
\[
D_{A} \text { to } C P
\] & \[
\begin{gathered}
0 \\
-4.0 \\
\hline
\end{gathered}
\] & & & ns \\
\hline \[
\begin{aligned}
& \mathbf{t}_{\mathbf{s}}(H) \\
& \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
& \hline
\end{aligned}
\] & Setup Time HIGH or LOW \(A_{n}\) to CP & \[
\begin{aligned}
& 0 \\
& 0
\end{aligned}
\] & & & ns \\
\hline \[
\begin{aligned}
& t_{h}(H) \\
& t_{n}(L) \\
& \hline
\end{aligned}
\] & Hold Time HIGH or LOW
\[
A_{n} \text { to } C P
\] & \[
\begin{aligned}
& 0 \\
& 0
\end{aligned}
\] & & & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{w}}(\mathrm{H}) \\
& \mathrm{t}_{\mathrm{w}}(\mathrm{~L}) \\
& \hline
\end{aligned}
\] & CP Pulse Width HIGH or LOW & \[
\begin{aligned}
& 40 \\
& 30 \\
& \hline
\end{aligned}
\] & & & ns \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature (unless othewise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Typ (Note 1) & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{I}}=-10 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\] & 2.4 & & & V \\
\hline VOL & Low Level Output Voltage & \[
\begin{aligned}
& V_{\mathrm{CC}}=\operatorname{Min} \mathrm{IOL}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\] & & & 0.3 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(V_{C C}=\) Max, \(V_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \(V_{C C}=\) Max, \(V_{1}=2.4 \mathrm{~V}\) & & & 50 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=0.3 \mathrm{~V}\) & & & -2 & mA \\
\hline los & Short Circuit Output Current & \[
\begin{aligned}
& V_{C C}=\text { Max } \\
& \text { (Note 2) }
\end{aligned}
\] & -2.5 & & -25 & mA \\
\hline Icc & Supply Current & \(V_{C C}=\operatorname{Max}\) (Note 3) & & & 70 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: \(\mathrm{I}_{\mathrm{CC}}\) is measured with all outputs open and all input grounded.

Switching Characteristics \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Max & \\
\hline \begin{tabular}{l}
\(t_{\text {PLH }}\) \\
tpHL
\end{tabular} & Propagation Delay \(B_{n}\) or \(C_{n}\) or \(Z_{n}\) & & \[
\begin{aligned}
& 68 \\
& 95
\end{aligned}
\] & ns \\
\hline \begin{tabular}{l}
\(t_{\text {PLH }}\) \\
\(t_{\text {PHL }}\)
\end{tabular} & Propagation Delay \(D_{A}\) to \(Z_{n}\) & & \[
\begin{aligned}
& 70 \\
& 92
\end{aligned}
\] & ns \\
\hline \begin{tabular}{l}
\(t_{\text {PLH }}\) \\
\(t_{\text {PHL }}\)
\end{tabular} & Propagation Delay CP to \(Z_{n}\) & & \[
\begin{aligned}
& 65 \\
& 57
\end{aligned}
\] & ns \\
\hline
\end{tabular}

\section*{Functional Description}

The 93L38 8-bit multiple port register can be considered a 1-bit slice of eight high speed working registers. Data can be written into any one and read from any two of the eight locations simultaneously. Master/slave operation eliminates all race problems associated with simultaneous read/write activity from the same location. When the clock input (CP) is LOW data applied to the data input line ( \(D_{A}\) ) enters the selected master. This selection is accomplished by coding the three write input select lines (A0-A2) appropriately. Data is stored synchronously with the rising edge of the clock pulse.
The information for each of the two slaved (output) latches is selected by two sets of read address inputs ( \(\mathrm{B} 0-\mathrm{B} 2\) and \(\mathrm{CO}-\mathrm{C} 2\) ). The information enters the slave while the clock is HIGH and is stored while the clock is LOW. If Slave Enable is LOW ( \(\overline{\mathrm{SLE}}\) ), the slave latches are continuously enabled.

The signals are available on the output pins ( \(Z_{B}\) and \(\left.Z_{C}\right)\). The input bit selection and the two output bit selections can be accomplished independently or simultaneously. The data flows into the device, is demultiplexed according to the state of the write address lines and is clocked into the selected latch. The eight latches function as masters and store the input data. The two output latches are slaves and hold the data during the read operation. The state of each slave is determined by the state of the master selected by its associated set of read address inputs.
The method of parallel expansion is shown in Figure A. One 93 L 38 is needed for each bit of the required word length. The read and write input lines should be connected in common on all of the devices. This register configuration provides two words of \(n\)-bits each at one time, where \(n\) devices are connected in parallel.


FIGURE A. Parallel Expansion
Logic Diagram


\section*{96L02}

\section*{Dual Retriggerable Resettable Monostable Multivibrator}

\section*{General Description}

The 96L02 is a dual TTL monostable multivibrator with trigger mode selection, reset capability, rapid recovery, internally compensated reference levels and high speed capability. Output pulse duration and accuracy depend on external timing components, and are therefore under user control for each application. It is well suited for a broad variety of applications, including pulse delay generators, square wave generators, long delay timers, pulse absence detectors, frequency detectors, clock pulse generators and fixed-frequency dividers. Each input is provided with a clamp diode to limit undershoot and minimize ringing induced by fast fall times acting on system wiring impedances.

\section*{Features}
- Retriggerable, \(0 \%\) to \(100 \%\) duty cycle
- DC level triggering, insensitive to transition times
- Leading or trailing-edge triggering
- Complementary outputs with active pull-ups

■ Pulse width compensation for \(\Delta \mathrm{V}_{\mathrm{CC}}\) and \(\Delta \mathrm{T}_{\mathrm{A}}\)
- 50 ns to \(\infty\) output pulse width range
- Optional retrigger lock-out capability
- Resettable, for interrupt operations

\section*{Connection Diagram}

\section*{Dual-In-Line Package}


TL/F/10203-1
Order Number 96L02DMQB or 96L02FMQB See NS Package Number J16A or W16A

\section*{Logic Symbol}


TL/F/10203-2
\(V_{C C}=\operatorname{Pin} 16\)
\(\mathrm{GND}=\operatorname{Pin} 8\)
\begin{tabular}{|l|l|}
\hline Pin Names & \multicolumn{1}{c|}{ Description } \\
\hline\(\overline{1} 0\) & Trigger Input (Active Falling Edge) \\
11 & Trigger Input (Active Rising Edge) \\
\(\overline{\mathrm{C}}_{\mathrm{D}}\) & Direct Clear Input (Active LOW) \\
Q & Positive Pulse Output \\
\(\overline{\mathrm{Q}}\) & Complementary Pulse Output \\
\hline
\end{tabular}

Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for avallability and specifications.
Supply Voltage
Input Voltage
5.5 V

Operating Free Air Temperature Range

Military
\(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
Storage Temperature Range
Recommended Operating Conditions

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multirow{2}{*}{Conditions} & \multicolumn{3}{|c|}{96 L 02 (MII)} & \multirow{2}{*}{Units} \\
\hline & & & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voitage & & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & & 0.7 & V \\
\hline IOH & High Level Output Current & & & & 0.36 & mA \\
\hline lOL & Low Level Output Current & & & & 4.8 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
\hline \[
\begin{aligned}
& t_{w}(L) \\
& t_{w}(H)
\end{aligned}
\] & Minimum Input Pulse Width, 11, īo & \(V_{C C}=5.0 \mathrm{~V}\) & & & 50 & ns \\
\hline \(t_{w}(\min )\) & Minimum Output Pulse Width at \(\mathrm{Q}, \overline{\mathrm{Q}}\) & \[
\begin{aligned}
& V_{C C}=5.0 \mathrm{~V}, R_{X}=20 \mathrm{k} \Omega \\
& C_{X}=0, C_{L}=15 \mathrm{pF}
\end{aligned}
\] & 10 & & 300 & ns \\
\hline \(t_{w}\) & Output Pulse Width, Q, \(\bar{Q}\) & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{RXX}=39 \mathrm{k} \Omega \\
& \mathrm{C}_{\mathrm{X}}=1000 \mathrm{pF}
\end{aligned}
\] & 11.5 & & 14.2 & \(\mu \mathrm{S}\) \\
\hline \(\mathrm{R}_{\mathrm{X}}\) & Timing Resistor Range & & & & 100 & \(k \Omega\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Condltions & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) }
\end{gathered}
\] & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{l}}=-10 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
\begin{aligned}
& V_{C C}=M i n, I_{O H}=M a x, \\
& V_{I L}=M a x, V_{I H}=M i n
\end{aligned}
\] & 2.4 & & & V \\
\hline VOL & Low Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{l}_{\mathrm{OL}}=\text { Max }, \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
\end{aligned}
\] & & & 0.3 & V \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\) & & & 1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \(V_{C C}=M a x, V_{1}=2.4 \mathrm{~V}\) & & & 20 & \(\mu \mathrm{A}\) \\
\hline 1 LL & Low Level Input Current & \(V_{C C}=M a x, V_{1}=0.3 \mathrm{~V}\) & & & -0.4 & mA \\
\hline los & Short Circuit Output Current & \(V_{C C}=\operatorname{Max}\) (Note 2) & -2.0 & & \(-13.0\) & mA \\
\hline ICC & Supply Current & \(V_{C C}=\operatorname{Max}\) (Note 3) & & & 16 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: ICC is measured with all outputs open and all inputs grounded.

Switching Characteristics \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\)
\begin{tabular}{|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min & Max & Units \\
\hline \(t_{\text {PLH }}\) & Propagation Delay \(\overline{1} 0\) to \(Q\), 11 to Q & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{R}_{\mathrm{X}}=20 \mathrm{k} \Omega \\
& \mathrm{C}_{\mathrm{X}}=0, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}
\end{aligned}
\] & & 75 & ns \\
\hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay \(\overline{1} 0\) to \(\bar{Q}\), 11 to \(\bar{Q}\) & \[
\begin{aligned}
& V_{C C}=5.0 V, R_{X}=20 \mathrm{k} \Omega \\
& C_{X}=0, C_{L}=15 \mathrm{pF}
\end{aligned}
\] & & 62 & ns \\
\hline \[
\begin{aligned}
& \mathrm{t}_{\mathrm{PLLH}} \\
& \mathrm{t}_{\mathrm{PHL}} \\
& \hline
\end{aligned}
\] & Propagation Delay \(\overline{\mathrm{CD}}\) to \(\overline{\mathrm{Q}}\), \(\overline{\mathrm{CD}}\) to Q & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{R}_{\mathrm{X}}=39 \mathrm{k} \Omega \\
& \mathrm{C}_{\mathrm{X}}=1000 \mathrm{pF}
\end{aligned}
\] & & 100 & ns \\
\hline
\end{tabular}

\section*{Functional Block Diagram}


TL/F/10203-3

\section*{Operation Notes}
1. TRIGGERING-can be accomplished by a positive-going transition on pin 4 (12) or a negative-going transition on pin 5 (11). Triggering begins as a signal crosses the input \(\mathrm{V}_{\mathrm{IL}}: \mathrm{V}_{\mathrm{IH}}\) threshold region; this activates an internal latch whose unbalanced cross-coupling causes it to assume a preferred state. As the latch output goes LOW it disables the gates leading to the Q output and, through an inverter, turns on the capacitor discharge transistor. The inverted signal is also fed back to the latch input to change its state and effectively end the triggering action; thus the latch and its associated feed-back perform the function of a differentiator.
The emitters of the latch transistors return to ground through an enabling transistor which must be turned off between successive triggers in order for the latch to proceed through the proper sequence when triggering is desired. Pin 5 (11) must be HIGH in order to trigger at pin 4 (12); conversely, pin 4 (12) must be LOW in order to trigger at pin 5 (11).
2. RETRIGGERING-In a normal cycle, triggering initiates a rapid discharge of the external timing capacitor, followed by a ramp voltage run-up at pin 2 (14). The delay will time out when the ramp voltage reaches the upper trigger point of a Schmitt circuit, causing the outputs to revert to the quiescent state. If another trigger occurs before the ramp voltage reaches the Schmitt threshold, the capacitor will be discharged and the ramp will start again without having disturbed the output. The delay period can there-
fore be extended for an arbitrary length of time by insuring that the interval between triggers is less than the delay time, as determined by the external capacitor and resistor.
3. NON-RETRIGGERABLE OPERATION-Retriggering can be inhibited logically, by connecting pin 6 (10) back to pin 4 (12) or by connecting pin 7 (9) back to pin 5 (11). Either hook-up has the effect of keeping the latch-enabling transistor turned on during the delay period, which prevents the input latch from cycling as discussed above in the section on triggering.
4. OUTPUT PULSE WIDTH—An external resistor Rx and an external capacitor \(C_{x}\) are required, as shown in the functional block diagram. To minimize stray capacitance and noise pickup, \(\mathrm{R}_{\mathrm{X}}\) and \(\mathrm{C}_{\mathrm{X}}\) should be located as close as possible to the circuit. In applications which require remote trimming of the pulse width, as with a variable resistor, Rx should consist of a fixed resistor in series with the variable resistor; the fixed resistor should be located as close as possible to the circuit. The output pulse width \(t_{w}\) is defined as follows, where \(\mathrm{R}_{\mathrm{X}}\) is in \(\mathrm{k} \Omega, \mathrm{C}_{\mathrm{X}}\) is in pF and \(t_{w}\) is in ns.
\[
t_{w}=0.33 R_{x} C_{X}\left(1+3 / R_{x}\right) \text { for } C_{x} \geq 10^{3} p F
\]
\[
20 \mathrm{k} \Omega \leq \mathrm{R}_{\mathrm{X}} \leq 100 \mathrm{k} \Omega \text { for }-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C}
\]
\(\mathrm{C}_{\mathrm{X}}\) may vary from 0 to any value. For pulse widths with \(\mathrm{C}_{\mathrm{X}}\) less than \(10^{3} \mathrm{pF}\) see Figure \(a\).

\section*{Operation Notes (Continued)}
5. SETUP AND RELEASE TIMES-The setup times listed below are necessary to allow the latch-enabling transistor to turn off and the node voltages within the input latch to stabilize, thus insuring proper cycling of the latch when the next trigger occurs. The indicated release times (equivalent to trigger duration) allow time for the input latch to cycle and its signal to propagate.


TL/F/10203-4
Input to Pin 5 (11)
Pin 4 (12) \(=\mathrm{L}\)
\(\operatorname{Pin} 3(13)=\mathrm{H}\)


TL/F/10203-5

Input to Pin 4 (12)
Pins 5 (11) and \(3(13)=\mathrm{H}\)
6. RESET OPERATION-A LOW signal on \(\overline{\mathrm{C}}_{\mathrm{D}}\), pin 3 (13), will terminate an output pulse, causing \(Q\) to go LOW and \(\overline{\mathrm{Q}}\) to go HIGH. As long as \(\overline{\mathrm{C}}_{\mathrm{D}}\) is held LOW, a delay period cannot be initiated nor will attempted triggering cause spikes at the outputs. A reset pulse duration, in the LOW state, of 25 ns is sufficient to insure resetting. If the reset input goes LOW at the same time that a trigger transition occurs, the reset will dominate and the outputs will not respond to the trigger. If the reset input goes HIGH coincident with a trigger transition, the circuit will respond to the trigger.

\section*{96L02 Pulse Width vs \(\mathrm{R}_{\mathrm{X}}\) and \(\mathrm{C}_{\mathrm{X}}\)}



FIGURE a


\section*{Section 6}

\section*{Physical Dimensions}

\section*{Section 6-Physical Dimensions}

Physical Dimensions
Data Bookshelf
Sales and Distribution Offices

\section*{20 Terminal Ceramic Leadless Chip Carrier (E) NS Package Number E20A}


\section*{14 Lead Ceramic Dual-In-Line Package (J) NS Package Number J14A}


\section*{16 Lead Ceramic Dual-In-Line Package (J)} NS Package Number J16A


\section*{20 Lead Ceramic Dual-In-Line Package (J) NS Package Number J20A}


\section*{24 Lead Ceramic Dual-In-Line Package (J) NS Package Number J24A}


\section*{24 Lead Ceramic Dual-In-Line Package (J) NS Package Number J24F}


J24F(REV G)

\section*{14 Lead (0.150" Wide) Molded Small Outline Package (M)} NS Package Number M14A


\section*{14 Lead (0.300" Wide) Molded Small Outline Package (M) \\ NS Package Number M14B}


M14B (REV D)

\section*{16 Lead (0.150" Wide) Molded Small Outline Package (M) NS Package Number M16A}


16 Lead ( \(0.300^{\prime \prime}\) Wide) Molded Small Outline Package (M) NS Package Number M16B


20 Lead (0.300" Wide) Molded Small Outline Package (M) NS Package Number M20B


24 Lead ( \(0.300^{\prime \prime}\) Wide) Molded Small Outline Package (M) NS Package Number M24B


\section*{14 Lead Molded Dual-In-Line Package (N)} NS Package Number N14A


\section*{16 Lead Molded Dual-In-Line Package (N) NS Package Number N16A}


\section*{16 Lead Molded Dual-In-Line Package (N) NS Package Number N16E}


OPTION 01


\section*{18 Lead Molded Dual-In-Line Package (N) NS Package Number N18A}


\section*{20 Lead Molded Dual-In-Line Package (N) NS Package Number N20A}


\section*{24 Lead Molded Dual-In-Line Package (N) NS Package Number N24A}


N24A (REV E)

24 Lead (0.300" Wide) Dual-In-Line Package (N) NS Package Number N24C


\section*{28 Lead Plastic Chip Carrier (V) NS Package Number V28A}


\section*{14 Lead Ceramic Package (W)} NS Package Number W14B


\section*{16 Lead Ceramic Package (W) NS Package Number W16A}



DETAIL A

20 Lead Ceramic Package (W)
NS Package Number W20A


\section*{24 Lead Ceramic Package (W) \\ NS Package Number W24C}


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[^0]:    Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

[^1]:    H = High Logic Level

[^2]:    H = High Logic Level
    L = Low Logic Level

[^3]:    $H=$ High Logic Level
    $L=$ Low Logic Level

[^4]:    Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.

[^5]:    Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.

[^6]:    *Typical Value

[^7]:    Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.

[^8]:    $\mathrm{H}=$ High Logic Level
    L = Low Logic Level

[^9]:    $H=$ High Logic Level
    L = Low Logic Level

[^10]:    *OC-Open Collector

[^11]:    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

    | Supply Voltage | 7 V |
    | :--- | ---: |
    | Input Voltage | 7 V |
    | Operating Free Air Temperature Range |  |
    | DM54LS | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
    | DM74LS | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
    | Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

[^12]:    $\mathrm{H}=$ High Logic Level
    $X=$ Either Low or High Logic Level
    $\mathrm{L}=$ Low Logic Level
    $\uparrow=$ Positive-going Transition

[^13]:    $H=$ High Logic Level
    $X=$ Either Low or High Logic Level
    L = Low Logic Level
    $\downarrow=$ Negative going edge of pulse.
    $Q_{0}=$ The output logic level before the indicated input conditions were established.
    Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

[^14]:    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

    | Supply Voltage | $V$ |
    | :---: | :---: |
    | Input Voltage | V |
    | Operating Free Air Temperature Range |  |
    | 54LS | $-55^{\circ} \mathrm{C}$ to $+125^{\circ}$ |
    | Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ}$ |

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    ## Recommended Operating Conditions

    | Symbol | Parameter | 54LS114 |  |  | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: |
    |  |  | Min | Nom | Max |  |
    | $V_{C C}$ | Supply Voltage | 4.5 | 5 | 5.5 | V |
    | $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | V |
    | $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 | V |
    | $\mathrm{IOH}^{\text {l }}$ | High Level Output Current |  |  | -0.4 | mA |
    | $\mathrm{lOL}^{\text {l }}$ | Low Level Output Current |  |  | 4 | mA |
    | $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | ${ }^{\circ} \mathrm{C}$ |
    | $\begin{aligned} & t_{s}(H) \\ & t_{s}(L) \\ & \hline \end{aligned}$ | Setup Time Jn or Kn to $\overline{\mathrm{CP}}$ | $\begin{aligned} & 20 \\ & 20 \\ & \hline \end{aligned}$ |  |  | ns |
    | $\begin{aligned} & t_{h}(H) \\ & t_{h}(\mathrm{~L}) \\ & \hline \end{aligned}$ | Hold Time Jn or Kn to $\overline{C P}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ |  |  | ns |
    | $\begin{aligned} & t_{w}(H) \\ & t_{w}(L) \end{aligned}$ | $\overline{\text { CP Pulse Width }}$ | $\begin{aligned} & 20 \\ & 15 \\ & \hline \end{aligned}$ |  |  | ns |
    | $t_{\text {w }}$ | $\overline{\mathrm{C}} \mathrm{D}$ or $\overline{\text { S }}$ Dn Pulse Width | 15 |  |  | ns |

    Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)

    | Symbol | Parameter | Conditions | Min | Typ (Note 1) | Max | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    | $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
    | $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, I_{\mathrm{OH}}=\mathrm{Max}, \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | 2.5 |  |  | V |
    | VOL | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max}, \\ & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ |  |  | 0.4 | V |
    |  |  |  |  |  | 0.5 |  |
    | 1 | Input Current @ Max Input Voltage | $V_{C C}=M a x, V_{I}=10 \mathrm{~V} ; \mathrm{Jn}, \mathrm{Kn}$ Inputs SD1, SD2 Inputs <br> CD Input <br> CP Input |  |  | $\begin{aligned} & 0.1 \\ & 0.3 \\ & 0.6 \\ & 0.8 \end{aligned}$ | mA <br> mA <br> mA <br> mA |
    | ${ }_{I H}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=2.7 \mathrm{~V} ; \mathrm{Jn}, \mathrm{Kn}$ Inputs SD1, SD2 Inputs <br> CD Input <br> CP Input |  |  | $\begin{gathered} 20 \\ 60 \\ 120 \\ 160 \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \\ & \mu \mathrm{~A} \\ & \mu \mathrm{~A} \end{aligned}$ |

    Electrical Characteristics (Continued)
    Over recommended operating free air temperature range (unless otherwise noted)

    | Symbol | Parameter | Conditions | Min | $\begin{gathered} \text { Typ } \\ \text { (Note 1) } \end{gathered}$ | Max | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    | IIL | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V} \mathrm{Jn}, \mathrm{Kn}$ Inputs <br> SD1, SD2 Inputs <br> CD Input <br> CP Input |  |  | $\begin{gathered} -0.4 \\ -0.8 \\ -1.6 \\ -1.44 \end{gathered}$ | mA <br> mA <br> mA <br> mA |
    | los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & \text { (Note 2) } \end{aligned}$ | -20 |  | -100 | mA |
    | ICC | Supply Current | $V_{C C}=M a x, V_{C P}=0 V$ |  |  | 8.0 | mA |

    Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    ## Switching Characteristics

    $\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

    | Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=\mathbf{2 k}, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | Units |
    | :---: | :---: | :---: | :---: | :---: |
    |  |  | Min | Max |  |
    | $f_{\text {max }}$ | Maximum Count Frequency | 30 |  | MHz |
    | $\begin{aligned} & \text { tpLH } \\ & \mathrm{t}_{\mathrm{PHL}} \\ & \hline \end{aligned}$ | Propagation Delay $\overline{\mathrm{CP}}$ to Q or $\overline{\mathrm{Q}}$ |  | $\begin{array}{r} 16 \\ 24 \\ \hline \end{array}$ | ns |
    | $\begin{aligned} & \mathrm{t}_{\mathrm{PLH}} \\ & \mathrm{t}_{\mathrm{PHL}} \\ & \hline \end{aligned}$ | Propagation Delay $\overline{\mathrm{CD}}$ or $\overline{\mathrm{SD}} \mathrm{n}$ to Q or $\overline{\mathrm{Q}}$ |  | $\begin{aligned} & 16 \\ & 24 \\ & \hline \end{aligned}$ | ns |

    ## Truth Table

    Asynchronous Inputs:
    LOW input to $\overline{\text { S }}$ D sets $Q$ to HIGH level
    LOW input to $\bar{C} D$ sets $Q$ to LOW level
    Clear and Set are independent of clock
    Simultaneous LOW on $\overline{\mathrm{C}}$ and $\overline{\mathrm{S}} \mathrm{D}$
    makes both $Q$ and $\bar{Q}$ HIGH
    H = HIGH Voltage Level
    L = LOW Voltage Level
    $t_{n}=$ Bit time before clock pulse.
    $t_{n+1}=$ Bit time after clock pulse.
    

    ## DM74LS122 Retriggerable One－Shot with Clear and Complementary Outputs

    ## General Description

    The DM74LS122 is a retriggerable monostable multivibrator featuring both positive and negative edge triggering with complementary outputs．An internal $10 \mathrm{k} \Omega$ timing resistor is provided for design convenience minimizing component count and layout problems．This device can be used with a single external capacitor．The＇LS122 has two active－low transition triggering inputs（A），two active－high transition trig－ gering inputs $(B)$ ，and a CLEAR input that terminates the output pulse width at a predetermined time independent of the timing components．The clear（CLR）input also serves as a trigger input when it is pulsed with a low level pulse transition（ㄷ）．To obtain optimum and trouble free opera－ tion please read operating rules and NSC one－shot applica－ tion notes carefully and observe recommendations．
    －Retriggerable to $100 \%$ duty cycle
    －Over－riding clear terminates output pulse
    －Internal $10 \mathrm{k} \Omega$ timing resistor
    －TTL，DTL compatible
    －Compensated for $V_{C C}$ and temperature variations
    －Input clamp diodes

    ## Functional Description

    The basic output pulse width is determined by selection of the internal resistor RINT or an external resistor（ $\mathrm{R}_{\mathrm{X}}$ ）and capacitor（ $C_{X}$ ）．Once triggered，the output pulse width may be extended by retriggering the gated active－low（A）tran－ sition inputs or the active－high transition（B）inputs or the CLEAR input．The output pulse width can be reduced or terminated by overriding it with the active－low CLEAR input．

    ## Features

    ■ DC triggered from active－high transition or active－low transition inputs

    ## Connection Diagram

    

    Order Number DM74LS122M or DM74LS122N See NS Package Number M14A or N14A

    ## Function Table

    | Inputs |  |  |  |  | Outputs |  |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    | CLEAR | A1 | A2 | B1 | B2 | Q | $\overline{\mathbf{Q}}$ |
    | L | X | X | X | X | L | H |
    | X | H | H | X | X | L | H |
    | X | X | X | L | X | L | H |
    | X | X | X | X | L | L | H |
    | H | L | X | $\uparrow$ | H | $\Omega$ | ־ |
    | H | L | X | H | $\uparrow$ | $\Omega$ | ป |
    | H | X | L | $\uparrow$ | H | $\Omega$ | Ч |
    | H | X | L | H | $\uparrow$ | $\Omega$ | 凹 |
    | H | H | $\downarrow$ | H | H | $\Omega$ | Ч |
    | H | $\downarrow$ | $\downarrow$ | H | H | $\Omega$ | Ч |
    | H | $\downarrow$ | H | H | H | $\Omega$ | Ч |
    | $\uparrow$ | L | X | H | H | $\Omega$ | 凹 |
    | $\uparrow$ | X | L | H | H | $\Omega$ | Ч |

    $H=$ High Logic Level
    L＝Low Logic Level
    X＝Can Be Either Low or High
    $\uparrow=$ Positive Going Transition
    $\downarrow=$ Negative Going Transition
    $\Omega=$ A Positive Pulse
    $\Psi=A$ Negative Pulse
    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    DM74LS
    Storage Temperature
    $l r$

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    Recommended Operating Conditions

    | Symbol | Parameters |  | Min | Nom | Max | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    | $V_{C C}$ | Supply Voltage |  | 4.75 | 5 | 5.25 | V |
    | $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage |  | 2 |  |  | V |
    | $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  |  | 0.8 | V |
    | IOH | High Level Output Current |  |  |  | -0.4 | mA |
    | lOL | Low Level Output Current |  |  |  | 8 | mA |
    | tw | Pulse Width (Note 6) | A or B High | 40 |  |  | ns |
    |  |  | A or B Low | 40 |  |  |  |
    |  |  | Clear Low | 40 |  |  |  |
    | $\mathrm{R}_{\text {EXT }}$ | External Timing Resistor |  | 5 |  | 260 | $k \Omega$ |
    | $\mathrm{C}_{\text {EXT }}$ | External Timing Capacitance |  | No Restriction |  |  | $\mu \mathrm{F}$ |
    | $C_{\text {WIRE }}$ | Wiring Capacitance at $\mathrm{R}_{\mathrm{EXT}} / \mathrm{C}_{\text {EXT }}$ Terminal |  |  |  | 50 | pF |
    | $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature |  | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

    | Symbol | Parameter | Conditions | Min | Typ (Note 1) | Max | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    | $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
    | $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\ & V_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | 2.7 | 3.4 |  | V |
    | V ${ }_{\text {OL }}$ | Low Level Output Voltage | $\begin{aligned} & V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ |  | 0.35 | 0.5 | V |
    |  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ |  | 0.25 | 0.4 |  |
    | 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}$ |  |  | 0.1 | mA |
    | $\mathrm{IIH}^{\text {H}}$ | High Level Input Current | $V_{C C}=\operatorname{Max}, V_{1}=2.7 \mathrm{~V}$ |  |  | 20 | $\mu \mathrm{A}$ |
    | $\mathrm{I}_{1}$ | Low Level Input Current | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  | -0.4 | mA |
    | los | Short Circuit Output Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ <br> (Note 2) | -20 |  | -100 | mA |
    | ICC | Supply Current | $\mathrm{V}_{\mathrm{CC}}=\operatorname{Max}($ Notes 3, 4 and 5) |  | 6 | 11 | mA |


    | Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load) |  |
    | :---: | :---: |

    ## Operating Rules

    1. To use the internal $10 \mathrm{k} \Omega$ timing resistor, connect the $\mathrm{R}_{\text {INT }}$ pin to $\mathrm{V}_{\mathrm{CC}}$.
    2. An external resistor ( $\mathrm{R}_{\mathrm{X}}$ ) or the internal resistor ( $10 \mathrm{k} \Omega$ ) and an external capacitor ( $C_{\mathrm{x}}$ ) are required for proper operation. The value of $C_{X}$ may vary from 0 to any necessary value. For small time constants use high-quality mica, glass, polypropylene, polycarbonate, or polystyrene capacitors. For large time constants use solid tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
    3. The pulse width is essentially determined by external timing components $\mathrm{R}_{\mathrm{X}}$ and $\mathrm{C}_{\mathrm{X}}$. For $\mathrm{C}_{\mathrm{X}}<1000 \mathrm{pF}$ see Figure 1; design curves on $T_{W}$ as function of timing components value. For $\mathrm{C}_{\mathrm{X}} \gg 1000 \mathrm{pF}$ the output is defined as:

    $$
    T_{W}=K R_{X} C_{X}
    $$

    where [ $R_{X}$ is in $k \Omega$ ]

    $$
    \text { [ } \mathrm{C}_{\mathrm{X}} \text { is in } \mathrm{pF} \text { ] }
    $$

    [ $T_{W}$ is in $n s$ ]

    $$
    K \approx 0.37
    $$

    

    TL/F/6385-2

    FIGURE 1

    The K factor is not a constant, but, varies with $\mathrm{C}_{\mathrm{X}}$. See Figure 2.
    

    TL/F/6385-3
    FIGURE 2
    4. The switching diode required for most TTL one-shots when using an electrolytic timing capacitor is not needed for the 'LS122 and should not be used.
    5. To obtain variable pulse width by remote trimming, the following circuit is recommended:
    

    TL/F/6385-4
    Note: "R remote" should be as close to the device pins as possible.

    ## FIGURE 3

    6. The retriggerable pulse width is calculated as shown below:

    $$
    T=T_{W}+t_{P L H}=0.50 \times R_{X} \times C_{X}+T_{P L H}
    $$

    The retriggered pulse width is equal to the pulse width plus a delay time period (Figure 4).
    

    FIGURE 4
    7. Output pulse width variation versus $V_{C C}$ and operation temperatures: Figure 5 depicts the relationship between pulse width variation versus $\mathrm{V}_{\mathrm{CC}}$; and Figure 6 depicts pulse width variation versus temperatures.
    

    TL/F/6385-6
    FIGURE 5
    

    FIGURE 6
    8. Under any operating condition $\mathrm{C}_{X}$ and $\mathrm{R}_{X}$ must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce $\mathrm{I}-\mathrm{R}$ and $\mathrm{Ldi} / \mathrm{dt}$ voltage developed along their connecting paths. If the lead length from $\mathrm{C}_{X}$ to pins (13) and (11) is greater than 3 cm , for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of $C_{X}$ in each cycle of its operation so that the output pulse width will be accurate.
    9. $\mathrm{V}_{\mathrm{CC}}$ and ground wiring should conform to good high-frequency standards and practices so that switching transients on the $V_{C C}$ and ground return leads do not cause interaction between one-shots. $\mathrm{A} 0.01 \mu \mathrm{~F}$ to $0.10 \mu \mathrm{~F}$ bypass capacitor (disk ceramic or monolithic type) from $V_{C C}$ to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the $\mathrm{V}_{\mathrm{CC}}$ pin as space permits.

    For further detailed device characteristics and output performance please refer to the NSC one-shot application note AN-366.

    National
    Semiconductor

    ## DM74LS123 Dual Retriggerable One-Shot with Clear and Complementary Outputs

    ## General Description

    The DM74LS123 is a dual retriggerable monostable multivibrator capable of generating output pulses from a few nanoseconds to extremely long duration up to $100 \%$ duty cycle. Each device has three inputs permitting the choice of either leading edge or trailing edge triggering. Pin $(A)$ is an activelow transition trigger input and pin (B) is an active-high transition trigger input. The clear (CLR) input terminates the output pulse at a predetermined time independent of the timing components. The clear input also serves as a trigger input when it is pulsed with a low level pulse transition (乙). To obtain the best trouble free operation from this device please read the operating rules as well as the NSC one-shot application notes carefully and observe recommendations.

    ## Features

    - DC triggered from active-high transition or active-low transition inputs
    . Retriggerable to $100 \%$ duty cycle


    ## Connection Diagram

    

    Order Number DM74LS123M or DM74LS123N
    See NS Package Number M16A or N16E

    - Compensated for $V_{C C}$ and temperature variations
    - Triggerable from CLEAR input
    - DTL, TTL compatible
    - Input clamp diodes


    ## Functional Description

    The basic output pulse width is determined by selection of an external resistor ( $R_{X}$ ) and capacitor ( $C_{X}$ ). Once triggered, the basic pulse width may be extended by retriggering the gated active-low transition or active-high transition inputs or be reduced by use of the active-low or CLEAR input. Retriggering to $100 \%$ duty cycle is possible by application of an input pulse train whose cycle time is shorter than the output cycle time such that a continuous "HIGH" logic state is maintained at the " $Q$ " output.
    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage

    | Operating Free Air Temperature Range | 7 V |
    | :--- | ---: |
    | Storage Temperature | 7 V |
    | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |  |$\quad-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    ## Recommended Operating Conditions

    | Symbol | Parameter |  | Min | Nom | Max | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    | $V_{C C}$ | Supply Voltage |  | 4.75 | 5 | 5.25 | V |
    | $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage |  | 2 |  |  | V |
    | $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  |  | 0.8 | V |
    | IOH | High Level Output Current |  |  |  | -0.4 | mA |
    | lOL | Low Level Output Current |  |  |  | 8 | mA |
    | tw | Pulse Width (Note 6) | A or B High | 40 |  |  | ns |
    |  |  | A or B Low | 40 |  |  |  |
    |  |  | Clear Low | 40 |  |  |  |
    | $\mathrm{R}_{\text {EXT }}$ | External Timing Resistor |  | 5 |  | 260 | k $\Omega$ |
    | $\mathrm{C}_{\text {EXT }}$ | External Timing Capacitance |  | No Restriction |  |  | $\mu \mathrm{F}$ |
    | CWIRE | Wiring Capacitance at $\mathrm{R}_{\mathrm{EXT}} / \mathrm{C}_{\mathrm{EXT}}$ Terminal |  |  |  | 50 | pF |
    | $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature |  | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

    | Symbol | Parameter | Conditions | Min | $\begin{gathered} \text { Typ } \\ \text { (Note 1) } \end{gathered}$ | Max | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    | $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
    | $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | 2.7 | 3.4 |  | V |
    | $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\ & V_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ |  | 0.35 | 0.5 | V |
    |  |  | $\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ |  | 0.25 | 0.4 |  |
    | 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}$ |  |  | 0.1 | mA |
    | $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $V_{C C}=\operatorname{Max}, V_{1}=2.7 \mathrm{~V}$ |  |  | 20 | $\mu \mathrm{A}$ |
    | IIL | Low Level Input Current | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  | -0.4 | mA |
    | los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & \text { (Note 2) } \\ & \hline \end{aligned}$ | -20 |  | -100 | mA |
    | ICC | Supply Current | $\mathrm{V}_{\text {CC }}=\operatorname{Max}$ (Notes 3,4 and 5) |  | 12 | 20 | mA |

    Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: Quiescent ICC is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, $\mathrm{C}_{\mathrm{EXT}}=0.02 \mu \mathrm{~F}$, and $R_{E X T}=25 \mathrm{k} \Omega$.
    Note 4: $\mathrm{I}_{\mathrm{CC}}$ is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, $\mathrm{C}_{\mathrm{EXT}}=0.02 \mu \mathrm{~F}$, and $\mathrm{R}_{\mathrm{EXT}}=25 \mathrm{k} \Omega$.
    Note 5: With all outputs open and 4.5 V applied to all data and clear inputs, Icc is measured after a momentary ground, then 4.5 V is applied to the clock.
    Note 6: $T_{A}=25^{\circ} \mathrm{C}$ and $V_{C C}=5 \mathrm{~V}$.

    ## Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

    | Symbol | Parameters | From (Input) <br> To (Output) | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    |  |  |  | $\begin{gathered} \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\ \mathrm{C}_{\mathrm{EXT}}=0 \mathrm{pF}, \mathrm{R}_{\mathrm{EXT}}=5 \mathrm{k} \Omega \end{gathered}$ |  | $\begin{gathered} C_{\mathrm{L}}=15 \mathrm{pF} \\ C_{\mathrm{EXT}}=1000 \mathrm{pF}, \mathrm{R}_{\mathrm{EXT}}=10 \mathrm{~K} \Omega \end{gathered}$ |  |  |
    |  |  |  | Min | Max | Min | Max |  |
    | tply | Propagation Delay Time Low to High Level Output | A to Q |  | 33 |  |  | ns |
    | tPLH | Propagation Delay Time Low to High Level Output | $B$ to Q |  | 44 |  |  | ns |
    | ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | A to $\bar{Q}$ |  | 45 |  |  | ns |
    | ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | $B$ to $\bar{Q}$ |  | 56 |  |  | ns |
    | ${ }_{\text {tPLH }}$ | Propagation Delay Time Low to High Level Output | Clear to $\bar{Q}$ |  | 45 |  |  | ns |
    | $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | Clear to Q |  | 27 |  |  | ns |
    | $t_{\text {WQ(Min) }}$ | Minimum Width of Pulse at Output Q | $A$ or B to Q |  | 200 |  |  | ns |
    | ${ }^{\text {tw }}$ (out) | Output Pulse Width | A or B to Q |  |  | 4 | 5 | $\mu \mathrm{S}$ |

    ## Operating Rules

    1. An external resistor ( $R_{X}$ ) and an external capacitor ( $C_{X}$ ) are required for proper operation. The value of $C_{x}$ may vary from 0 to any necessary value. For small time constants high-grade mica, glass, polypropylene, polycarbonate, or polystyrene material capacitors may be used. For large time constants use tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
    2. When an electrolytic capacitor is used for $C_{X}$ a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current. This switching diode is not needed for the 'LS123 one-shot and should not be used. In general the use of the switching diode is not recommended with retriggerable operation.
    3. For $C_{X} \gg 1000 \mathrm{pF}$ the output pulse width ( $T_{W}$ ) is defined as follows:
    $T_{W}=K R_{X} C_{X}$
    where [ $R_{X}$ is in $k \Omega$ ]

    $$
    \begin{aligned}
    & {\left[C_{X} \text { is in } p F\right]} \\
    & {\left[T_{W} \text { is in } n s\right]} \\
    & K \approx 0.37
    \end{aligned}
    $$

    4. The multiplicative factor $K$ is plotted as a function of $C_{X}$ below for design considerations:
    

    TL/F/6386-2
    FIGURE 1

    ## Operating Rules (Continued)

    5. For $C_{X}<1000 \mathrm{pF}$ see Figure 2 for $\mathrm{T}_{\mathrm{W}}$ vs $\mathrm{C}_{\mathrm{X}}$ family curves with $\mathrm{R}_{\mathrm{X}}$ as a parameter:
    

    TL/F/6386-3
    FIGURE 2
    6. To obtain variable pulse widths by remote trimming, the following circuit is recommended:
    

    TL/F/6386-4
    FIGURE 3
    Note: "Rremote" should be as close to the device pin as possible.
    7. The retriggerable pulse width is calculated as shown below:

    $$
    T=T_{W}+t_{P L H}=K \times R_{X} \times C_{X}+t_{P L H}
    $$

    The retriggered pulse width is equal to the pulse width plus a delay time period (Figure 4).
    

    FIGURE 4
    8. Output pulse width variation versus $V_{C C}$ and temperatures: Figure 5 depicts the relationship between pulse width variation versus $V_{C C}$, and Figure 6 depicts pulse width variation versus temperatures.
    

    TL/F/6386-6
    FIGURE 5
    

    TL/F/6386-7
    FIGURE 6
    9. Under any operating condition $C_{X}$ and $R_{X}$ must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I-R and Ldi/dt voltage developed along their connecting paths. If the lead length from $\mathrm{C}_{\mathrm{X}}$ to pins (6) and (7) or pins (14) and (15) is greater than 3 cm , for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of $C_{X}$ in each cycle of its operation so that the output pulse width will be accurate.
    10. The $\mathrm{C}_{\text {EXT }}$ pins of this device are internally connected to the internal ground. For optimum system performance they should be hard wired to the system's return ground plane.
    11. $\mathrm{V}_{\mathrm{CC}}$ and ground wiring should conform to good high-frequency standards and practices so that switching transients on the $\mathrm{V}_{\mathrm{CC}}$ and ground return leads do not cause interaction between one-shots. A $0.01 \mu \mathrm{~F}$ to $0.10 \mu \mathrm{~F}$ bypass capacitor (disk ceramic or monolithic type) from $V_{C C}$ to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the $\mathrm{V}_{\mathrm{CC}}$-pin as space permits.
    For further detalled device characteristics and output performance please refer to the NSC one-shot application note AN-336.

    ## 54LS125A/DM54LS125A/DM74LS125A

    ## Quad TRI-STATE® Buffers

    ## General Description

    This device contains four independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility
    that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

    ## Features

    - Alternate Military/Aerospace device (54LS125) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.


    ## Connection Diagram

    

    Order Number 54LS125ADMQB, 54LS125AFMQB, 54LS125ALMQB, DM54LS125AJ, DM54LS125AW, DM74LS125AM or DM74LS125AN See NS Package Number E20A, J14A, M14A, N14A or W14B

    ## Function Table

    | $\mathbf{Y}=\mathbf{A}$ |  |  |
    | :---: | :---: | :---: |
    | Inputs |  | Output |
    | $\mathbf{A}$ | $\mathbf{C}$ | $\mathbf{Y}$ |
    | $L$ | $L$ | L |
    | $H$ | $L$ | $H$ |
    | $X$ | $H$ | $H i-Z$ |

    $H=$ High Logic Level
    L = Low Logic Level
    $X=$ Either Low or High Logic Level
    $\mathrm{Hi}-\mathrm{Z}=$ TRI-STATE (Outputs are disabled)

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

    | Supply Voltage | 7 V |
    | :--- | ---: |
    | Input Voltage | 7 V |
    | Operating Free Air Temperature Range |  |
    | DM54LS and 54LS | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
    | DM74LS | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
    | Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    ## Recommended Operating Conditions

    | Symbol | Parameter | DM54LS125A |  |  | DM74LS125A |  |  | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    |  |  | Min | Nom | Max | Min | Nom | Max |  |
    | $V_{C C}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
    | $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
    | $\mathrm{V}_{\mathrm{IL}}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
    | IOH | High Level Output Current |  |  | -1 |  |  | -2.6 | mA |
    | lOL | Low Level Output Current |  |  | 12 |  |  | 24 | mA |
    | $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

    | Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    | $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
    | $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ |  | 2.4 | 3.4 |  | V |
    | VOL | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I} \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \\ & \mathrm{I}_{\mathrm{OL}}=12 \mathrm{~mA} \\ & \hline \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
    |  |  |  | DM74 |  | 0.35 | 0.5 |  |
    |  |  |  | DM74 |  | 0.25 | 0.4 |  |
    | 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
    | ${ }_{\mathrm{I}}^{\mathrm{H}}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
    | IIL | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=0.4 \mathrm{~V}$ |  |  |  | -0.4 | mA |
    | lozh | Off-State Output Current with High Level Output Voltage Applied | $\begin{aligned} & V_{\mathrm{CC}}=\operatorname{Max}, V_{\mathrm{O}}=2.4 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max} \end{aligned}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
    | lozl | Off-State Output Current with Low Level Output Voltage Applied | $\begin{aligned} & V_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max} \end{aligned}$ |  |  |  | -20 | $\mu \mathrm{A}$ |
    | los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & (\text { Note 2) } \end{aligned}$ | DM54 | -20 |  | $-100$ | mA |
    |  |  |  | DM74 | -20 |  | -100 |  |
    | Icc | Supply Current | $\mathrm{V}_{\mathrm{CC}}=\operatorname{Max}$ (Note 3) |  |  | 11 | 20 | mA |

    Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: ICC is measured with the data control (C) inputs at 4.5 V and the data inputs grounded.

    | Symbol | Parameter | $R_{L}=667 \Omega$ |  |  |  | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    |  |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=150 \mathrm{pF}$ |  |  |
    |  |  | Min | Max | Min | Max |  |
    | $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output |  | 15 |  | 21 | ns |
    | ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output |  | 18 |  | 22 | ns |
    | tPZH | Output Enable Time to High Level Output |  | 25 |  | 35 | ns |
    | tPZL | Output Enable Time to Low Level Output |  | 25 |  | 40 | ns |
    | $t_{\text {PHZ }}$ | Output Disable Time from High Level Output (Note 1) |  | 20 |  |  | ns |
    | $t_{\text {PLI }}$ | Output Disable Time from Low Level Output (Note 1) |  | 20 |  |  | ns |

    National Semiconductor

    ## 54LS126/DM74LS126A Quad TRI-STATE® Buffers

    ## General Description

    This device contains four independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the
    output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

    ## Connection Diagram

    

    Order Number 54LS126DMQB, 54LS126FMQB, DM74LS126AM or DM74LS126AN See NS Package Number M14A, N14A or W14B

    ## Function Table

    | $\mathbf{Y}=\mathbf{A}$ |  |  |
    | :---: | :---: | :---: |
    | Inputs |  | Output |
    | $\mathbf{A}$ | $\mathbf{C}$ | $\mathbf{Y}$ |
    | L | $H$ | L |
    | $H$ | $H$ | $H$ |
    | $X$ | L | Hi-Z |

    $H=$ High Logic Level
    L = Low Logic Level
    X = Either Low or High Logic Level
    $\mathrm{Hi}-\mathrm{Z}=$ TRI-STATE (Outputs are disabled)

    ```
    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    \begin{tabular}{lr}
    54 LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    orage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}
    ```

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    ## Recommended Operating Conditions

    | Symbol | Parameter | 54LS126 |  |  | DM74LS126A |  |  | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    |  |  | Min | Nom | Max | Min | Nom | Max |  |
    | $V_{C C}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
    | $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
    | $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
    | IOH | High Level Output Current |  |  | -1 |  |  | -2.6 | mA |
    | $\mathrm{lOL}^{\text {l }}$ | Low Level Output Current |  |  | 12 |  |  | 24 | mA |
    | $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

    | Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    | $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
    | $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\ & V_{I H}=\operatorname{Min} \end{aligned}$ |  | 2.4 |  |  | V |
    | V OL | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | 54LS |  |  | 0.4 |  |
    |  |  |  | DM74 |  | 0.35 | 0.5 | V |
    |  |  | $\mathrm{l}_{\mathrm{OL}}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ |  |  | 0.25 | 0.4 |  |
    | 1 | Input Current @ Max Input Voltage | $\begin{aligned} V_{C C}=M a x, V_{1} & =10 \mathrm{~V}(54 \mathrm{LS}) \\ V_{1} & =7 \mathrm{~V}(\mathrm{DM} 74) \end{aligned}$ |  |  |  | 0.1 | mA |
    | $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
    | IIL | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}$ |  |  |  | -0.4 | mA |
    | l OZH | Off-State Output Current with High Level Output Voltage Applied | $\begin{aligned} & V_{C C}=M a x, V_{O}=2.4 V \\ & V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max} \end{aligned}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
    | lozL | Off-State Output Current with Low Level Output Voltage Applied | $\begin{aligned} & V_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max} \end{aligned}$ |  |  |  | -20 | $\mu \mathrm{A}$ |
    | los | Short Circuit Output Current | $\begin{aligned} & V_{\mathrm{CC}}=M a x \\ & \text { (Note 2) } \end{aligned}$ | 54LS | -30 |  | -130 | mA |
    |  |  |  | DM74 | -20 |  | -100 |  |
    | ICC | Supply Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ (Note 3) | DM74 |  | 12 | 22 | mA |
    | $\mathrm{I}_{\mathrm{CCL}}$ | Supply Current | $\mathrm{V}_{1}=0 \mathrm{~V}$ | 54LS |  |  | 24 | mA |
    | ICCH | Supply Current | $\mathrm{V}_{1}=4.5 \mathrm{~V}$ | 54LS |  |  | 20 | mA |

    Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: ICC is measured with both the output control and data inputs grounded.

    Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

    | Symbol | Parameter | 54LS |  | DM74LS |  | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    |  |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  | $\begin{aligned} & C_{L}=150 \mathrm{pF}, \\ & R_{\mathrm{L}}=667 \Omega \end{aligned}$ |  |  |
    |  |  | Min | Max | Min | Max |  |
    | $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output |  | 15 |  | 21 | ns |
    | tPHL | Propagation Delay Time High to Low Level Output |  | 18 |  | 22 | ns |
    | $t_{\text {PZH }}$ | Output Enable Time to High Level Output |  | 30 |  | 36 | ns |
    | $t_{\text {PZL }}$ | Output Enable Time to Low Level Output |  | 20 |  | 42 | ns |
    | $t_{\text {PHZ }}$ | Output Disable Time from High Level Output (Note 1) |  | 30 |  |  | ns |
    | $t_{\text {PLZ }}$ | Output Disable Time from Low Level Output (Note 1) |  | 30 |  |  | ns |

    Note 1: $C_{L}=5 \mathrm{pF}$.

    ## DM54LS132/DM74LS132 Quad 2-Input NAND Gates with Schmitt Trigger Inputs

    ## General Description

    This device contains four independent gates each of which performs the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

    ## Connection Diagram

    

    TL/F/6389-1
    Order Number DM54LS132J, DM54LS132W, DM74LS132M or DM74LS132N See NS Package Number J14A, M14A, N14A or W14B

    Function Table

    | $\mathbf{Y}=\overline{\mathbf{A B}}$ |  |  |
    | :---: | :---: | :---: |
    | Inputs |  | Output |
    | $\mathbf{A}$ | $\mathbf{B}$ | $\mathbf{Y}$ |
    | L | L | $H$ |
    | L | $H$ | $H$ |
    | $H$ | L | $H$ |
    | $H$ | $H$ | L |

    $H=$ High Logic Level
    $L=$ Low Logic Level
    Absolute Maximum Ratings (Note)
    Af Military/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    DM54LS
    DM74LS
    Storage Temperature Range
    Sto

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    ## Recommended Operating Conditions

    | Symbol | Parameter | DM54LS132 |  |  | DM74LS132 |  |  | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    |  |  | Min | Nom | Max | Min | Nom | Max |  |
    | $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
    | $\mathrm{V}_{\mathrm{T}+}$ | Positive-Going Input <br> Threshold Voltage (Note 1) | 1.4 | 1.6 | 1.9 | 1.4 | 1.6 | 1.9 | V |
    | $\mathrm{V}_{\mathrm{T}-}$ | Negative-Going Input Threshold Voltage (Note 1) | 0.5 | 0.8 | 1 | 0.5 | 0.8 | 1 | V |
    | HYS | Input Hysteresis (Note 1) | 0.4 | 0.8 |  | 0.4 | 0.8 |  | V |
    | IOH | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
    | lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
    | $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

    | Symbol | Parameter | Conditions |  | Min | $\begin{aligned} & \text { Typ } \\ & \text { (Note 2) } \end{aligned}$ | Max | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    | $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
    | $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\text { Max, } \\ & \mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{T}-\mathrm{Min}} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
    |  |  |  | DM74 | 2.7 | 3.4 |  |  |
    | $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & V_{C C}=\text { Min, } I_{O L}=\text { Max, } \\ & V_{I}=V_{T}+\text { Max } \end{aligned}$ | DM54 |  | 0.25 | 0.4 |  |
    |  |  |  | DM74 |  | 0.35 | 0.5 | V |
    |  |  | $\mathrm{lOL}=4 \mathrm{~mA}$, | DM74 |  | 0.25 | 0.4 |  |
    | $\mathrm{I}_{\mathrm{T}+}$ | Input Current at Positive-Going Threshold | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{l}}=\mathrm{V}_{\mathrm{T}+}$ |  |  | -0.14 |  | mA |
    | $\mathrm{I}_{\mathbf{T}-}$ | Input Current at Negative-Going Threshold | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{l}}=\mathrm{V}_{\mathrm{T}-}$ |  |  | -0.18 |  | mA |
    | 1 | Input Current @ Max Input Voltage | $V_{C C}=M a x, V_{1}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
    | $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
    | ILL | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.4 | mA |
    | los | Short Circuit Output Current | $V_{C C}=M a x$ <br> (Note 3) | DM54 | -20 |  | -100 | mA |
    |  |  |  | DM74 | -20 |  | -100 |  |
    | ICCH | Supply Current with Outputs High | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 5.9 | 11 | mA |
    | ICCL | Supply Current with Outputs Low | $V_{C C}=$ Max |  |  | 8.2 | 14 | mA |

    ## Note 1: $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$

    Note 2: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
    Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    Switching Characteristics at $\mathrm{V}_{\mathrm{CC}} 5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

    | Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    |  |  | $C_{L}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
    |  |  | Min | Max | Min | Max |  |
    | $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | 5 | 22 | 8 | 25 | ns |
    | $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | 5 | 22 | 10 | 33 | ns |

    ## 54LS133/DM74LS133 <br> 13-Input NAND Gate

    ## General Description

    This device contains one, 13 -input gate that performs the logic NAND functions.

    ## Connection Diagram

    

    TL/F/9818-1
    Order Number 54LS133DMQB, 54LS133FMQB, 54LS133LMQB, DM74LS133M or DM74LS133N See NS Package Number E20A, J16A, M16A, N16E or W16A

    ## Absolute Maximum Ratings (Note)

    

    ## Recommended Operating Conditions

    | Symbol | Parameter | 54LS133 |  |  | DM74LS133 |  |  | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    |  |  | Min | Nom | Max | Min | Nom | Max |  |
    | $V_{C C}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
    | $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
    | $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
    | $\mathrm{l}_{\mathrm{OH}}$ | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
    | lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
    | $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

    Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)

    | Symbol | Parameter | Conditions |  | Min | $\begin{gathered} \text { Typ } \\ \text { (Note 1) } \end{gathered}$ | Max | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    | $V_{1}$ | Input Clamp Voltage | $V_{C C}=\mathrm{Min}, \mathrm{l}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
    | VOH | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | 54LS | 2.5 |  |  | V |
    |  |  |  | DM74 | 2.7 | 3.4 |  |  |
    | V OL | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | 54LS |  |  | 0.4 | V |
    |  |  |  | DM74 |  | 0.35 | 0.5 |  |
    |  |  | $\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
    | 1 | Input Current @ Max Input Voltage | $V_{C C}=M a x, V_{1}=10 \mathrm{~V}$ |  |  |  | 0.1 | mA |
    | $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
    | ILL | Low Level Input Current | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.4 | mA |
    | los | Short Circuit Output Current | $V_{C C}=\operatorname{Max}$ <br> (Note 2) | 54LS | $-20$ |  | -100 | mA |
    |  |  |  | DM74 | -20 |  | -100 |  |
    | ICCH | Supply Current with Outputs High | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{IN}}=\mathrm{GND}$ |  |  |  | 0.5 | mA |
    | ICCL | Supply Current with Outputs Low | $V_{C C}=M a x, V_{\text {IN }}=$ Open |  |  |  | 1.1 | mA |

    Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

    | Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | Units |
    | :---: | :---: | :---: | :---: | :---: |
    |  |  | Min | Max |  |
    | $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output |  | 15 | ns |
    | $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output |  | 38 | ns |

    ## 54LS136/DM54LS136/DM74LS136 Quad 2-Input Exclusive-OR Gate with Open-Collector Outputs

    ## General Description

    This device contains four independent gates, each of which performs the logic exclusive-OR function.

    ## Features

    - Alternate Military/Aerospace device (54LS136) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.


    ## Connection Diagram

    

    TL/F/9819-1
    Order Number 54LS136DMQB, 54LS136FMQB, DM54LS136J, DM54LS136W, DM74LS136M or DM74LS136N See NS Package Number J14A, M14A, N14A or W14B

    Truth Table

    | Inputs |  | Output |
    | :---: | :---: | :---: |
    | A B |  | Z |
    | L | L | L |
    | L | H | H |
    | H | L | H |
    | H | H | L |

    $H=$ HIGH Voltage Level
    L = LOW Voltage Level

    | Absolute Maximum Ratings (Note) |
    | :--- |
    | If Military/Aerospace specified devices are required, |
    | please contact the National Semiconductor Sales |
    | Office/Distributors for availability and specifications. |
    | Supply Voltage |
    | Input Voltage |
    | Operating Free Air Temperature Range |
    | DM54LS and 54LS |
    | DM74LS |
    | Storage Temperature Range |

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    ## Recommended Operating Conditions

    | Symbol | Parameter | DM54LS136 |  |  | DM74LS136 |  |  | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    |  |  | Min | Nom | Max | Min | Nom | Max |  |
    | $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
    | $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
    | $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
    | lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
    | $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

    Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)

    | Symbol | Parameter | Conditions |  | Min | Typ <br> (Note 1) | Max | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    | $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
    | $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
    |  |  |  | DM74 |  | 0.35 | 0.5 |  |
    |  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
    | 1 | Input Current @ Max Input Voltage | $V_{C C}=M_{\text {ax }}, V_{1}=10 \mathrm{~V}$ |  |  |  | 0.2 | mA |
    | $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 40 | $\mu \mathrm{A}$ |
    | IIL | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.6 | mA |
    | ICC | Supply Current | $V_{C C}=M a x$ |  |  |  | 10 | mA |

    Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

    | Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  | Units |
    | :---: | :---: | :---: | :---: | :---: |
    |  |  | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  |  |
    |  |  | Min | Max |  |
    | $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output |  | 23 | ns |
    | $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output |  | 23 | ns |

    ## 54LS138/DM54LS138/DM74LS138, 54LS139/DM54LS139/DM74LS139 Decoders/Demultiplexers

    ## General Description

    These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.
    The LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24 -line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.
    The LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.
    All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance

    Schottky diodes to suppress line-ringing and simplify system design.

    ## Features

    - Designed specifically for high speed: Memory decoders Data transmission systems
    - LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
    - LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
    - Schottky clamped for high performance
    - Typical propagation delay (3 levels of logic)

    $$
    \begin{array}{ll}
    \text { LS138 } & 21 \mathrm{~ns} \\
    \text { LS139 } & 21 \mathrm{~ns}
    \end{array}
    $$

    - Typical power dissipation

    LS138 32 mW LS139 34 mW

    - Alternate Military/Aerospace devices (54LS138, 54LS139) are available. Contact a National Semiconductor Sales Office/Distributor for specifications.


    ## Connection Diagrams

    

    Order Number 54LS138DMQB, 54LS138FMQB, 54LS138LMQB, DM54LS138J, DM54LS138W, DM74LS138M or DM74LS138N
    See NS Package Number E20A, J16A, M16A, N16E or W16A
    

    TL/F/6391-2
    Order Number 54LS139DMQB, 54LS139FMQB, 54LS139LMQB, DM54LS139J, DM54LS139W, DM74LS139M or DM74LS139N
    See NS Package Number E20A, J16A, M16A, N16E or W16A

    ```
    Absolute Maximum Ratings (Note)
    If Milltary/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for avallability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    ```

    DM54LS and 54LS
    $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
    DM74LS
    $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$
    Storage Temperature Range

    $$
    -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C}
    $$

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    ## Recommended Operating Conditions

    | Symbol | Parameter | DM54LS138 |  |  | DM74LS138 |  |  | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    |  |  | Min | Nom | Max | Min | Nom | Max |  |
    | $V_{C C}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
    | $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
    | $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
    | IOH | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
    | lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
    | $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

    ## 'LS138 Electrical Characteristics

    over recommended operating free air temperature range (unless otherwise noted)

    | Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    | $V_{1}$ | Input Clamp Voltage | $V_{C C}=\operatorname{Min}, l_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
    | $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\ & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
    |  |  |  | DM74 | 2.7 | 3.4 |  |  |
    | $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max}, \\ & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
    |  |  |  | DM74 |  | 0.35 | 0.5 |  |
    |  |  | $\mathrm{lOL}=4 \mathrm{~mA}$, | DM74 |  | 0.25 | 0.4 |  |
    | 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
    | $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
    | $\mathrm{IIL}^{\text {L }}$ | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | $-0.36$ | mA |
    | los | Short Circuit Output Current | $V_{C C}=M a x$ <br> (Note 2) | DM54 | -20 |  | -100 | mA |
    |  |  |  | DM74 | -20 |  | -100 |  |
    | ICC | Supply Current | $\mathrm{V}_{\mathrm{CC}}=\operatorname{Max}($ Note 3) |  |  | 6.3 | 10 | mA |

    Note 1: All typicals are at $V_{C C}=5 \mathrm{~V}, T_{A}=25^{\circ} \mathrm{C}$.
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: ICC is measured with all outputs enabled and open.
    'LS138 Switching Characteristics
    at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

    | Symbol | Parameter | From (Input) To (Output) | Levels of Delay | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    |  |  |  |  | $C_{L}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
    |  |  |  |  | Min | Max | Min | Max |  |
    | ${ }_{\text {tPLH }}$ | Propagation Delay Time Low to High Level Output | Select to Output | 2 |  | 18 |  | 27 | ns |
    | ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | Select to Output | 2 |  | 27 |  | 40 | ns |
    | $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | Select to Output | 3 |  | 18 |  | 27 | ns |
    | ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | Select to Output | 3 |  | 27 |  | 40 | ns |
    | $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | Enable to Output | 2 |  | 18 |  | 27 | ns |
    | ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | Enable to Output | 2 |  | 24 |  | 40 | ns |
    | ${ }_{\text {tPLH }}$ | Propagation Delay Time Low to High Level Output | Enable to Output | 3 |  | 18 |  | 27 | ns |
    | ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | Enable to Output | 3 |  | 28 |  | 40 | ns |

    Recommended Operating Conditions

    | Symbol | Parameter | DM54LS139 |  |  | DM74LS139 |  |  | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    |  |  | Min | Nom | Max | Min | Nom | Max |  |
    | $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
    | $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
    | $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
    | IOH | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
    | lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
    | $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

    
    

    LS139
    

    TL/F/6391-4

    ## National Semiconductor <br> 54LS151/DM54LS151/DM74LS151 Data Selector/Multiplexer

    ## General Description

    This data selector/multiplexer contains full on-chip decoding to select the desired data source. The 'LS151 selects one-of-eight data sources. The 'LS151 has a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output low.
    The 'LS151 features complementary $W$ and $Y$ outputs.

    ## Features

    ■ Select one-of-eight data lines

    - Performs parallel-to-serial conversion
    - Permits multiplexing from N lines to one line
    - Also for use as Boolean function generator
    - Typical average propagation delay time data input to $W$ output 12.5 ns
    - Typical power dissipation 30 mW
    - Alternate Military/Aerospace device (54LS151) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.
    

    TL/F/6392-1

    Order Number 54LS151DMQB, 54LS151FMQB, 54LS151LMQB, DM54LS151J, DM54LS151W, DM74LS151M or DM74LS151N See NS Package Number E20A, J16A, M16A, N16E or W16A

    ## Truth Table

    | Inputs |  |  |  | Outputs |  |
    | :---: | :---: | :---: | :---: | :---: | :---: |
    |  | Select | Strobe | Y | W |  |
    | C | B | A | S |  |  |
    | X | X | X | H | L | H |
    | L | L | L | L | D0 | $\overline{\text { D0 }}$ |
    | L | L | H | L | D1 | $\overline{\text { D1 }}$ |
    | L | H | L | L | D2 | $\overline{\text { D2 }}$ |
    | L | H | H | L | D3 | $\overline{\text { D3 }}$ |
    | H | L | L | L | D4 | $\overline{\text { D4 }}$ |
    | H | L | H | L | D5 | $\overline{\text { D5 }}$ |
    | H | H | L | L | D6 | $\overline{\text { D6 }}$ |
    | H | H | H | L | D7 | $\overline{\text { D7 }}$ |


    ## Absolute Maximum Ratings (Note)

    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    7 V
    Operating Free Air Temperature Range

    DM54LS and 54LS
    DM74LS
    Storage Temperature Range
    $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
    $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$
    $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    ## Recommended Operating Conditions

    | Symbol | Parameter | DM54LS151 |  |  | DM74LS151 |  |  | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    |  |  | Min | Nom | Max | Min | Nom | Max |  |
    | $V_{C C}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
    | $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
    | $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
    | lOH | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
    | lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
    | $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

    | Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    | $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  |  | $-1.5$ | V |
    | $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\ & V_{I L}=M a x, V_{I H}=\operatorname{Min} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
    |  |  |  | DM74 | 2.7 | 3.4 |  |  |
    | $\mathrm{V}_{\text {OL }}$ | Low Level Output Voltage | $\begin{aligned} & V_{C C}=\operatorname{Min}, \mathrm{lOL}_{\mathrm{C}}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
    |  |  |  | DM74 |  | 0.35 | 0.5 |  |
    |  |  | $\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
    | 1 | Input Current @ Max Input Voltage | $V_{C C}=M a x, V_{1}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
    | $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $V_{C C}=\operatorname{Max}, V_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
    | I/L | Low Level Input Current | $\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.4 | mA |
    | los | Short Circuit Output Current | $V_{C C}=M a x$ <br> (Note 2) | DM54 | -20 |  | -100 | mA |
    |  |  |  | DM74 | -20 |  | -100 |  |
    | ICC | Supply Current | $\mathrm{V}_{C C}=\operatorname{Max}$ (Note 3) |  |  | 6 | 10 | mA |

    Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: ICC is measured with all outputs open, strobe and data select inputs at 4.5 V , and all other inputs open.
    

    ## 54LS152

    8-Input Multiplexer

    ## General Description

    The 54LS152 is a high speed 8 -input digital multiplexer. It provides, in one package, the ability to select one line of data from up to eight sources. The 54LS152 can be used as a universal function generator to generate any logic function of four variables. It is supplied in Flatpak only; for Dual-InLine Package applications use the 'LS151.

    ## Connection Diagram

    Dual-In-Line Package
    

    Order Number 54LS152FMQB See NS Package Number W14B

    ## Logic Symbol

    

    TL/F/10206-2
    TL/F/10206-1

    $$
    V_{C C}=\operatorname{Pin} 14
    $$

    $$
    \text { GND }=\operatorname{Pin} 7
    $$

    Truth Table

    |  | Inputs |  | Output |
    | :---: | :---: | :---: | :---: |
    | S2 | S1 | S0 | $\overline{\text { Z }}$ |
    | L | L | L | $\bar{I} 0$ |
    | L | L | H | $\bar{I} 1$ |
    | L | H | L | $\bar{I} 2$ |
    | L | $H$ | $H$ | $\overline{1} 3$ |
    | H | L | L | $\overline{1} 4$ |
    | H | L | $H$ | $\bar{I} 5$ |
    | H | H | L | $\bar{I} 6$ |
    | H | H | H | $\bar{I} 7$ |

    $H=$ HIGH Voltage Level
    $\mathrm{L}=$ LOW Voltage Level
    

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

    | Symbol | Parameter | Conditions | Min | Typ (Note 1) | Max | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    | $V_{1}$ | Input Clamp Voltage | $V_{C C}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
    | $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\text { Max }, \\ & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | 2.5 | 3.4 |  | V |
    | $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\operatorname{Max}, \\ & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ |  |  | 0.4 | V |
    | 1 | Input Current @ Max Input Voltage | $V_{C C}=M a x, V_{1}=10.0 \mathrm{~V}$ |  |  | 0.1 | mA |
    | $\mathrm{IIH}^{\text {H}}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  | 20 | $\mu \mathrm{A}$ |
    | IIL | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}$ | -30 |  | -400 | $\mu \mathrm{A}$ |
    | los | Short Circuit Output Current | $\begin{aligned} & V_{\mathrm{CC}}=\mathrm{Max} \\ & \text { (Note 2) } \\ & \hline \end{aligned}$ | -20 |  | -100 | mA |
    | ICC | Supply Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ (Note 3) |  |  | 9 | mA |

    Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Switching Characteristics $\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (See Section 1 for test waveforms and output load)

    | Symbol | Parameter | $C_{L}=15 \mathrm{pF}$ |  | Units |
    | :---: | :---: | :---: | :---: | :---: |
    |  |  | Min | Max |  |
    | $\begin{aligned} & \text { tpLH } \\ & \text { tpHL } \\ & \hline \end{aligned}$ | Propagation Delay, Sn to $\overline{\mathrm{Z}}$ |  | $\begin{aligned} & 23 \\ & 32 \\ & \hline \end{aligned}$ | ns |
    | $\begin{aligned} & \mathrm{t}_{\mathrm{PLLH}} \\ & \mathrm{t}_{\mathrm{PHL}} \end{aligned}$ | Propagation Delay, In to $\overline{\mathbf{Z}}$ |  | $\begin{aligned} & 21 \\ & 20 \end{aligned}$ | ns |

    ## Functional Description

    The 54LS152 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, $\mathrm{S} 0, \mathrm{~S} 1, \mathrm{~S} 2$. The logic function provided at the output is:

    $$
    \begin{aligned}
    & +14 \bullet \overline{\mathrm{~S}} 0 \cdot \overline{\mathrm{~S}} 1 \cdot \mathrm{~S} 2+\mathrm{I} 5 \cdot \mathrm{~S} 0 \cdot \overline{\mathrm{~S}} 1 \cdot \mathrm{~S} 2+\mathrm{I} 6 \bullet \mathrm{~S} 0 \cdot \mathrm{~S} 1 \cdot \mathrm{~S} 2+\mathrm{I} \cdot \bullet \mathrm{~S} 0 \cdot \mathrm{~S} 1 \cdot \mathrm{~S} 2) .
    \end{aligned}
    $$

    The 54LS152 provides the ability, in one package, to select from eight sources of data or control information.

    ## Logic Diagram

    

    TL/F/10206-3

    ## 54LS153/DM54LS153/DM74LS153

    ## Dual 4-Line to 1-Line Data Selectors/Multiplexers

    ## General Description

    Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

    ## Features

    - Permits multiplexing from N lines to 1 line

    ■ Performs at parallel-to-serial conversion

    ## Connection Diagram

    

    TL/F/6393-1

    ## Logic Diagram

    

    Order Number 54LS153DMQB, 54LS153FMQB, 54LS153LMQB, DM54LS153J, DM54LS153W, DM74LS153M or DM74LS153N See NS Package Number E20A, J16A, M16A, N16E or W16A

    ## Function Table

    | Select <br> Inputs | Data Inputs |  |  |  |  | Strobe | Output |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    | B | A | C0 | C1 | C2 | C3 | G | Y |
    | X | X | X | X | X | X | H | L |
    | L | L | L | X | X | X | L | L |
    | L | L | H | X | X | X | L | H |
    | L | H | X | L | X | X | L | L |
    | L | H | X | H | X | X | L | H |
    | H | L | X | X | L | X | L | L |
    | H | L | X | X | H | X | L | H |
    | H | H | X | X | X | L | L | L |
    | H | H | X | X | X | H | L | H |

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage 7V
    Operating Free Air Temperature Range
    DM54LS and 54LS
    $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
    DM74LS
    $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$
    Storage Temperature Range

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    ## Recommended Operating Conditions

    | Symbol | Parameter | DM54LS153 |  |  | DM74LS153 |  |  | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    |  |  | Min | Nom | Max | Min | Nom | Max |  |
    | $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
    | $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
    | $\mathrm{V}_{\mathrm{IL}}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
    | IOH | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
    | lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
    | $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

    | Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    | $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
    | $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
    |  |  |  | DM74 | 2.7 | 3.4 |  |  |
    | $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & V_{C C}=M i n, I_{O L}=\operatorname{Max} \\ & V_{I L}=M a x, V_{I H}=\operatorname{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
    |  |  |  | DM74 |  | 0.35 | 0.5 |  |
    |  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
    | 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
    | $\mathrm{I}_{\mathrm{H}}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
    | ILL | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.36 | mA |
    | los | Short Circuit Output Current | $V_{C C}=M a x$ <br> (Note 2) | DM54 | -20 |  | -100 | mA |
    |  |  |  | DM74 | -20 |  | -100 |  |
    | ICC | Supply Current | $V_{C C}=\operatorname{Max}$ (Note 3) |  |  | 6.2 | 10 | mA |

    Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: ICC is measured with all outputs open and all other inputs grounded.

    Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

    | Symbol | Parameter | From (Input) to (Output) | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    |  |  |  | $C_{L}=15 \mathrm{pF}$ |  | $C_{L}=50 \mathrm{pF}$ |  |  |
    |  |  |  | Min | Max | Min | Max |  |
    | ${ }_{\text {tpLH }}$ | Propagation Delay Time Low to High Level Output | Data to $Y$ |  | 15 |  | 20 | ns |
    | tPHL | Propagation Delay Time High to Low Level Output | Data to $Y$ |  | 26 |  | 35 | ns |
    | $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | Select to Y |  | 29 |  | 35 | ns |
    | $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | Select to $Y$ |  | 38 |  | 45 | ns |
    | $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | Strobe to Y |  | 24 |  | 30 | ns |
    | $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | Strobe to Y |  | 32 |  | 40 | ns |

    ## DM54LS154/DM74LS154 4-Line to 16-Line Decoders/Demultiplexers

    ## General Description

    Each of these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

    ## Features

    - Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
    - Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
    - Input clamping diodes simplify system design
    - High fan-out, low-impedance, totem-pole outputs
    - Typical propagation delay

    3 levels of logic 23 ns
    Strobe 19 ns

    - Typical power dissipation 45 mW


    ## Connection and Logic Diagrams

    

    TL/F/6394-2

    ```
    Absolute Maximum Ratings
    (Note)
    If Milltary/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for availability and specifications.
    Supply Voltage 7V
    Input Voltage
    7V
    Operating Free Air Temperature Range
    \begin{tabular}{lr} 
    DM54LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54LS154} & \multicolumn{3}{|c|}{DM74LS154} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{l}_{\mathrm{OH}}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, l_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{VOL} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline IIH & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\) Max, \(\mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\text { Max } \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 3)} & & 9 & 14 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: ICC is measured with all outputs open and all inputs grounded.
    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Data to Output & & 30 & & 35 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to Output & & 30 & & 35 & ns \\
    \hline \({ }_{\text {PPLH }}\) & Propagation Delay Time Low to High Level Output & Strobe to Output & & 20 & & 25 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Strobe to Output & & 25 & & 35 & ns \\
    \hline
    \end{tabular}

    \section*{7 National Semiconductor}

    \section*{54LS155/DM54LS155/DM74LS155, 54LS156/DM54LS156/DM74LS156 Dual 2-Line to 4-Line Decoders/Demultiplexers}

    \section*{General Description}

    These TTL circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied at C2 is true through its outputs. The inverter following the C1 data input permits use as a 3 -to- 8 -line decoder, or 1-to-8-line demultiplexer, without external gating. Input clamping diodes are provided on these circuits to minimize transmission-line effects and simplify system design.

    \section*{Features}
    - Applications:

    Dual 2-to-4-line decoder
    Dual 1-to-4-line demultiplexer
    3-to-8-line decoder
    1-to-8-line demultiplexer
    - Individual strobes simplify cascading for decoding or demultiplexing larger words
    - Input clamping diodes simplify system design
    - Choice of outputs: Totem-pole (LS155) Open-collector (LS156)
    - Alternate Military/Aerospace device (54LS155/156) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

    \section*{Connection Diagram and Function Tables}

    \section*{Dual-In-Line Package}
    

    TL/F/6395-1
    3-Line-to-8-Line Decoder or 1-Line-to-8-Line Demultiplexer
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{2}{|r|}{Inputs} & \multicolumn{8}{|c|}{Outputs} \\
    \hline Select & Strobe Or Data & (0) & (1) & (2) & (3) & (4) & (5) & (6) & (7) \\
    \hline C \(\dagger\) B A & G \(\ddagger\) & 2 YO & 2Y1 & 2 Y 2 & 2Y3 & 1 YO & 1Y1 & 1Y2 & 1 Y 3 \\
    \hline X \(\times\) X & H & H & H & H & H & H & H & H & H \\
    \hline L L L & L & L & H & H & H & H & H & H & H \\
    \hline L L H & L & H & L & H & H & H & H & H & H \\
    \hline L H L & L & H & H & L & H & H & H & H & H \\
    \hline L H H & L & H & H & H & L & H & H & H & H \\
    \hline H L L & L & H & H & H & H & L & H & H & H \\
    \hline H L H & L & H & H & H & H & H & L & H & H \\
    \hline H H L & L & H & H & H & H & H & H & L & H \\
    \hline H H H & L & H & H & H & H & H & H & H & L \\
    \hline
    \end{tabular}

    Order Number 54LS155DMQB, 54LS155FMQB, 54LS155LMQB, DM54LS155J, DM54LS155W, DM74LS155M, DM74LS155N, 54LS156DMQB, 54LS156FMQB, DM54LS156J, DM54LS156W, DM74LS156M or DM74LS156N
    See NS Package Number E20A, J16A, M16A, N16E or W16A

    2-Line-to-4-Line Decoder or 1-Line-to-4-Line Demultiplexer
    \begin{tabular}{|cc|c|c|cccc|}
    \hline \multicolumn{4}{|c|}{ Inputs } & \multicolumn{4}{c|}{ Outputs } \\
    \cline { 1 - 4 } Select & Strobe & Data & & & & \\
    \cline { 1 - 3 } B & A & G1 & C1 & 1Yo & 1Y1 & 1Y2 & 1Y3 \\
    \cline { 1 - 7 } X & X & H & X & H & H & H & H \\
    L & L & L & H & L & H & H & H \\
    L & H & L & H & H & L & H & H \\
    H & L & L & H & H & H & L & H \\
    H & H & L & H & H & H & H & L \\
    X & X & X & L & H & H & H & H \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{4}{|c|}{Inputs} & \multicolumn{4}{|c|}{Outputs} \\
    \hline \multicolumn{2}{|l|}{Select} & Strobe & Data & & & & \\
    \hline B & A & G2 & C2 & 2 YO & 2Y1 & 2Y2 & 2 Y 3 \\
    \hline X & X & H & X & H & H & H & H \\
    \hline L & L & L & L & L & H & H & H \\
    \hline L & H & L & L & H & L & H & H \\
    \hline H & L & L & L & H & H & L & H \\
    \hline H & H & L & L & H & H & H & L \\
    \hline X & X & X & H & H & H & H & H \\
    \hline
    \end{tabular}
    †C \(=\) inputs \(C 1\) and \(C 2\) connected together
    \(\ddagger \mathrm{G}=\) inputs G 1 and G 2 connected together
    \(H=\) high level, \(L=\) low level, \(X=\) don't care

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avallabillty and specifications.

    \section*{Supply Voltage}

    Input Voltage
    Operating Free Air Temperature Range
    DM54LS and 54LS
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    Storage Temperature Range
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{l|l|c|c|c|c|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multirow{2}{*}{ Parameter } & \multicolumn{3}{|c|}{ DM54LS155 } & \multicolumn{3}{c|}{ DM74LS155 } & \multirow{2}{*}{ Units } \\
    \cline { 3 - 9 } & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{~V}_{\mathrm{OH}}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    \section*{'LS155 Electrical Characteristics}
    over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\
    & V_{I L}=\operatorname{Max}, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\text {OL }}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, \mathrm{IOL}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{lOL}=4 \mathrm{~mA}\), & DM74 & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{l}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\) Max, \(V_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \(1 / 2\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.36 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\text { Max } \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline lCC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}\) (Note 3)} & & 6.1 & 10 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: Icc is measured with all outputs open, \(\mathrm{A}, \mathrm{B}\), and C 1 inputs at 4.5 V , and \(\mathrm{C} 2, \mathrm{G} 1\), and G 2 inputs grounded.
    'LS155 Switching Characteristics
    at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{\begin{tabular}{l}
    From (Input) \\
    To (Output)
    \end{tabular}} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    \mathrm{A}, \mathrm{~B}, \mathrm{C} 2, \mathrm{G} 1 \\
    \text { or G2 to Y }
    \end{gathered}
    \] & & 18 & & 22 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \mathrm{A}, \mathrm{~B}, \mathrm{C} 2, \mathrm{G} 1 \\
    \text { or } \mathrm{G} 2 \text { to } \mathrm{Y}
    \end{gathered}
    \] & & 27 & & 35 & ns \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & \(A\) or \(B\) to \(Y\) & & 18 & & 24 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \(A\) or \(B\) to \(Y\) & & 27 & & 35 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{aligned}
    & \mathrm{C} 1 \\
    & \text { to } \mathrm{Y}
    \end{aligned}
    \] & & 20 & & 24 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{aligned}
    & \mathrm{C} 1 \\
    & \text { to } \mathrm{Y}
    \end{aligned}
    \] & & 27 & & 35 & ns \\
    \hline
    \end{tabular}

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54LS156} & \multicolumn{3}{|c|}{DM74LS156} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline VOH & High Level Output Voltage & & & 5.5 & & & 5.5 & V \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    \section*{'LS156 Electrical Characteristics}
    over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline ICEX & High Level Output Current & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, V_{O}=5.5 \mathrm{~V} \\
    & V_{I L}=\operatorname{Max}, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & & & 100 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\text {OL }}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\) Max, \(V_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \(1 / 2\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.36 & mA \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 2)} & & 6.1 & 10 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: ICC is measured with all outputs open, A, B, and C1 inputs at 4.5 V , and \(\mathrm{C} 2, \mathrm{G} 1\), and G 2 grounded.
    'LS156 Switching Characteristics
    at \(V_{C C}=5 \mathrm{~V}\) and \(T_{A}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    A, B, C 2, G 1 \\
    \text { or } \mathrm{G} 2 \text { to } Y
    \end{gathered}
    \] & & 28 & & 53 & ns \\
    \hline tPHL & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \mathrm{A}, \mathrm{~B}, \mathrm{C} 2, \mathrm{G} 1 \\
    \text { or } \mathrm{G} 2 \text { to } \mathrm{Y}
    \end{gathered}
    \] & & 33 & & 43 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & A or B to \(Y\) & & 28 & & 53 & ns \\
    \hline tPHL & Propagation Delay Time High to Low Level Output & A or B to \(Y\) & & 33 & & 43 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{aligned}
    & \mathrm{C1} \\
    & \text { to } \mathrm{Y}
    \end{aligned}
    \] & & 28 & & 53 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{aligned}
    & \mathrm{C} 1 \\
    & \text { to } \mathrm{Y}
    \end{aligned}
    \] & & 34 & & 43 & ns \\
    \hline
    \end{tabular}

    \section*{Logic Diagram}
    

    TL/F/6395-2

    \section*{54LS157／DM54LS157／DM74LS157， 54LS158／DM54LS158／DM74LS158 Quad 2－Line to 1－Line Data Selectors／Multiplexers}

    \section*{General Description}

    These data selectors／multiplexers contain inverters and drivers to supply full on－chip data selection to the four out－ put gates．A separate strobe input is provided．A 4－bit word is selected from one of two sources and is routed to the four outputs．The LS157 presents true data whereas the LS158 presents inverted data to minimize propagation delay time．

    \section*{Applications}
    －Expand any data input point
    －Multiplex dual data buses
    －Generate four functions of two variables（one variable is common）
    －Source programmable counters

    Features
    四 Buffered inputs and outputs
    图 Typical Propagation Time LS157 9 ns LS158 7 ns
    田 Typical Power Dissipation LS157 49 mW LS158 24 mW
    （ Alternate Military／Aerospace device（54LS157， 54LS158）is available．Contact a National Semiconduc－ tor Sales Office／Distributor for specifications．

    \section*{Connection Diagrams}
    

    TL／F／6396－1
    Order Number 54LS157DMQB，54LS157FMQB， 54LS157LMQB，DM54LS157J，DM54LS157W， DM74LS157M or DM74LS157N
    See NS Package Number E20A，J16A， M16A，N16E or W16A
    

    TL／F／6396－2
    Order Number 54LS158DMQB，54LS158FMQB， 54LS158LMQB，DM54LS158J，DM54LS158W， DM74LS158M or DM74LS158N
    See NS Package Number E20A，J16A， M16A，N16E or W16A

    Function Table
    \begin{tabular}{|c|c|cc|c|c|}
    \hline \multicolumn{4}{|c|}{ Inputs } & \multicolumn{3}{c|}{ Output Y } \\
    \hline Strobe & Select & A & B & LS157 & LS158 \\
    \hline H & X & X & X & L & H \\
    L & L & L & X & L & H \\
    L & L & H & X & H & L \\
    L & H & X & L & L & H \\
    L & H & X & H & H & L \\
    \hline
    \end{tabular}

    \footnotetext{
    \(H=\) High Level，\(L=\) Low Level，\(X=\) Don＇t Care
    }

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54LS157} & \multicolumn{3}{|c|}{DM74LS157} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{lOH}^{\mathrm{O}}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    \section*{'LS157 Electrical Characteristics}
    over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{VOH} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\
    & V_{I L}=M a x, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\
    & V_{I L}=\operatorname{Max}, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current @ Max Input Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=7 V
    \end{aligned}
    \]} & S or G & & & 0.2 & \multirow[t]{2}{*}{mA} \\
    \hline & & & A or B & & & 0.1 & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{IIH}^{\text {H}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=2.7 V
    \end{aligned}
    \]} & Sor G & & & 40 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & A or B & & & 20 & \\
    \hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=0.4 V
    \end{aligned}
    \]} & Sor G & & & \(-0.8\) & \multirow[t]{2}{*}{mA} \\
    \hline & & & A or B & & & -0.4 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=M a x
    \] \\
    (Note 2)
    \end{tabular}} & DM54 & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\) (Note 3)} & & 9.7 & 16 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: Icc is measured with 4.5 V applied to all inputs and all outputs open.
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{9}{|l|}{\begin{tabular}{l}
    'LS157 Switching Characteristics \\
    at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \end{tabular}} \\
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{2}{|l|}{\multirow[t]{3}{*}{From (Input) To (Output)}} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & & \multicolumn{2}{|l|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & & Min & Max & Min & Max & \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & Data to \(Y\) & & & 14 & & 18 & ns \\
    \hline tpHL & Propagation Delay Time High to Low Level Output & Data to \(Y\) & & & 14 & & 23 & ns \\
    \hline tplH & Propagation Delay Time Low to High Level Output & Strobe to \(Y\) & & & 20 & & 24 & ns \\
    \hline tpHL & Propagation Delay Time High to Low Level Output & Strobe to \(Y\) & & & 21 & & 30 & ns \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & \[
    \begin{aligned}
    & \text { Select } \\
    & \text { to } Y
    \end{aligned}
    \] & & & 23 & & 28 & ns \\
    \hline tpHL & Propagation Delay Time High to Low Level Output & Select to Y & & & 27 & & 32 & ns \\
    \hline \multicolumn{9}{|l|}{Recommended Operating Conditions} \\
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54LS158} & \multicolumn{3}{|c|}{DM74LS158} & Units \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\text {cc }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline lol & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    \section*{'LS158 Electrical Characteristics}
    over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOH}_{\mathrm{OH}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{VOL} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\text { Min, } \mathrm{IOL}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{v} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current @ Max Input Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=7 \mathrm{~V}
    \end{aligned}
    \]} & S or G & & & 0.2 & \multirow[t]{2}{*}{mA} \\
    \hline & & & A or B & & & 0.1 & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{IIH}^{\text {H}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\text { Max } \\
    & V_{1}=2.7 \mathrm{~V}
    \end{aligned}
    \]} & S or G & & & 40 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & A or B & & & 20 & \\
    \hline \multirow[t]{2}{*}{ILL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max} \\
    & V_{1}=0.4 \mathrm{~V}
    \end{aligned}
    \]} & S or G & & & -0.8 & \multirow[t]{2}{*}{mA} \\
    \hline & & & A or B & & & -0.4 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline Icc & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 3)} & & 4.8 & 8 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: ICC is measured with 4.5 V applied to all inputs and all outputs open.
    'LS158 Switching Characteristics
    at \(V_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline tplH & Propagation Delay Time Low to High Level Output & \[
    \begin{aligned}
    & \text { Data } \\
    & \text { to } Y
    \end{aligned}
    \] & & 12 & & 18 & ns \\
    \hline tPHL & Propagation Delay Time High to Low Level Output & Data to Y & & 12 & & 21 & ns \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & Strobe to \(Y\) & & 17 & & 23 & ns \\
    \hline tPHL & Propagation Delay Time High to Low Level Output & Strobe to \(Y\) & & 18 & & 28 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Select to \(Y\) & & 20 & & 24 & ns \\
    \hline tPHL & Propagation Delay Time High to Low Level Output & Select to \(Y\) & & 24 & & 36 & ns \\
    \hline
    \end{tabular}

    \section*{Logic Diagrams}
    

    TL/F/6396-3
    

    TL/F/6396-4

    \section*{54LS160A/DM74LS160A, 54LS162A/DM74LS162A Synchronous Presettable BCD Decade Counters}

    \section*{General Description}

    The 'LS160 and 'LS162 are high speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'LS160 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'LS162 has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock.

    \section*{Features}
    - Synchronous counting and loading
    - High speed synchronous expansion
    - Typical count rate of 35 MHz
    - Fully edge triggered

    \section*{Connection Diagram}

    Dual-In-Line Package
    

    Order Number 54LS160ADMQB, 54LS160AFMQB, 54LS160ALMQB, 54LS162ADMQB, 54LS162AFMQB, 54LS162ALMQB, DM74LS160AM, DM74LS160AN, DM74LS162AM or DM74LS162AN See NS Package Number E20A, J16A, M16A, N16E or W16A
    \begin{tabular}{|l|l|}
    \hline \multicolumn{1}{|c|}{\begin{tabular}{c} 
    Pin \\
    Names
    \end{tabular}} & \multicolumn{1}{c|}{ Description } \\
    \hline CEP & Count Enable Parallel Input \\
    CET & Count Enable Trickle Input \\
    CP & Clock Pulse Input (Active Rising Edge) \\
    \(\overline{M R}(' 160)\) & Asynchronous Master Reset \\
    & Input (Active LOW) \\
    \(\overline{\text { SR ('162) }}\) & Synchronous Reset \\
    & Input (Active LOW) \\
    P0-P3 & Parallel Data Inputs \\
    \(\overline{\text { PE }}\) & Parallel Enable Input \\
    & (Active LOW) \\
    Q0-Q3 & Flip-Flop Outputs \\
    TC & Terminal Count Output \\
    \hline
    \end{tabular}

    Logic Symbol
    

    TL/F/10177-2

    \footnotetext{
    \(V_{C C}=\operatorname{Pin} 16 * \overline{M R}\) for 'LS160
    GND \(=\) Pin \(8 \quad * \overline{S R}\) for 'LS162
    }
    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required,
    please contact the Natlonal Semiconductor Sales
    Office/Distributors for avallablity and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    54LS
    DM74LS
    Storage Temperature Range

    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avallability and specifications.

    Input Voltage
    Operating Free Air Temperature Range

    DM74LS
    Storage Temperature Range

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    Recommended Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS160A/162A} & \multicolumn{3}{|c|}{DM74LS160A/162A} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{1 \mathrm{H}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L})
    \end{aligned}
    \] & Setup Time, HIGH or LOW
    \[
    P_{n} \text { to } C P
    \] & \[
    \begin{aligned}
    & 20 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 20 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L)
    \end{aligned}
    \] & Hold Time, HIGH or LOW
    \[
    P_{n} \text { to } C P
    \] & \[
    \begin{aligned}
    & 0.0 \\
    & 0.0 \\
    & \hline
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 0.0 \\
    & 0.0 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Setup Time, HIGH or LOW \(\overline{P E}\) to CP & \[
    \begin{aligned}
    & 20 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 20 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L) \\
    & \hline
    \end{aligned}
    \] & Hold Time, HIGH or LOW \(\overline{P E}\) to CP & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Setup Time, HIGH or LOW CEP, CET or \(\overline{\text { SR }}\) to CP & \[
    \begin{aligned}
    & 20 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 20 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(\mathrm{~L})
    \end{aligned}
    \] & Hold Time, HIGH or LOW CEP, CET or \(\overline{\mathrm{SR}}\) to CP & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{w}(H) \\
    & t_{w}(L)
    \end{aligned}
    \] & CP Pulse Width, HIGH or LOW & \[
    \begin{array}{r}
    15 \\
    25 \\
    \hline
    \end{array}
    \] & & & \[
    \begin{aligned}
    & 15 \\
    & 25
    \end{aligned}
    \] & & & ns \\
    \hline \(t_{w}(L)\) & \(\overline{\text { MR }}\) Pulse Width LOW ('160) & 15 & & & 15 & & & ns \\
    \hline \(\mathrm{t}_{\text {rec }}\) & Recovery Time \(\overline{\mathrm{MR}}\) to CP ('160) & 20 & & & 20 & & & ns \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \begin{tabular}{l}
    Typ \\
    (Note 1)
    \end{tabular} & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & 54LS & 2.5 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & & 0.5 & \\
    \hline & & \(\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & & 0.4 & \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{8}{|l|}{\begin{tabular}{l}
    Electrical Characteristics \\
    over recommended operating free air temperature range (unless otherwise noted) (Continued)
    \end{tabular}} \\
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \begin{tabular}{l}
    Typ \\
    (Note 1)
    \end{tabular} & Max & Units \\
    \hline 1 & Input Current © Max Input Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M a x, V_{1}=10 \mathrm{~V} \text { Inputs } \\
    & \text { PE, CET Inputs }
    \end{aligned}
    \]} & & & \[
    \begin{aligned}
    & 0.1 \\
    & 0.2
    \end{aligned}
    \] & mA \\
    \hline \(\mathrm{IIH}^{\prime}\) & High Level Input Current & \multicolumn{2}{|l|}{\[
    V_{C C}=M a x, V_{1}=2.7 \mathrm{~V} \text { Inputs }
    \]
    PE, CET Inputs} & & & \[
    \begin{aligned}
    & 20 \\
    & 40 \\
    & \hline
    \end{aligned}
    \] & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\) Max, \(\mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}\) Inputs} & 54LS & & & -0.4 & \multirow{2}{*}{mA} \\
    \hline & & & DM74 & & & -1.6 & \\
    \hline & & \(\overline{\text { PE, CET Inputs }}\) & & & & -0.8 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline \({ }^{\text {CCCH }}\) & Supply Current with Outputs HIGH & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \overline{\mathrm{PE}}=\mathrm{GND} \\
    & \mathrm{CP}=\widetilde{\mathrm{O}}, \text { Other Inputs }=4.5 \mathrm{~V}
    \end{aligned}
    \]} & & & 31 & mA \\
    \hline \({ }^{\text {cCL }}\) & Supply Current with Outputs LOW & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IN}}=\mathrm{GND} \\
    & \mathrm{CP}=\Omega
    \end{aligned}
    \]} & & & 31 & mA \\
    \hline
    \end{tabular}

    \section*{Switching Characteristics \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\)}
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\[
    \begin{aligned}
    & \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \\
    & \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\
    & \hline
    \end{aligned}
    \]} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \(\mathrm{f}_{\text {max }}\) & Maximum Clock Frequency & 25 & & MHz \\
    \hline \[
    \begin{aligned}
    & t_{\text {PLL }} \\
    & t_{\text {PHLL }}
    \end{aligned}
    \] & Propagation Delay CP to TC & & \[
    \begin{aligned}
    & 25 \\
    & 21
    \end{aligned}
    \] & ns \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLL }}\) \\
    tpHL
    \end{tabular} & Propagation Delay CP to \(Q_{n}\) & & \[
    \begin{aligned}
    & 20 \\
    & 27 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{tPLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay CP to \(Q_{n}\) & & \[
    \begin{aligned}
    & 24 \\
    & 27 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & t_{\text {PLH }} \\
    & t_{\text {PHLL }}
    \end{aligned}
    \] & Propagation Delay CET to TC & & \[
    \begin{aligned}
    & 14 \\
    & 14
    \end{aligned}
    \] & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay \(\overline{M R}\) to \(Q_{n}\) ('160) & & 28 & ns \\
    \hline
    \end{tabular}

    \section*{Functional Description}

    The 'LS160 and 'LS162 count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The '161 and '163 count modulo-16 binary sequence. From state \(15(\mathrm{HHHH})\) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the \(Q\) outputs (except due to Master Reset of the 'LS160) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('LS160), synchronous reset ('LS162), parallel load, count-up and hold. Five control inputs-Master Reset (MR, 'LS160), Synchronous Reset ( \(\overline{\mathrm{SR}}\), 'LS162), Parallel Enable ( \(\overline{\mathrm{PE}}\) ), Count Enable Parallel (CEP) and Count Enable Trickle (CET)-determine the mode of operation, as shown in the

    Mode Select Table. A LOW signal on \(\overline{M R}\) overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on \(\overline{\text { SR }}\) overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on \(\overline{\mathrm{PE}}\) overrides counting and allows information on the Parallel Data \(\left(P_{n}\right)\) inputs to be loaded into the flip-flops on the next rising edge of CP. With \(\overline{\mathrm{PE}}\) and \(\overline{\mathrm{MR}}\) ('LS160) or SR ('LS162) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.
    The 'LS160A and 'LS162A use D-type edge-triggered flipflops and changing the \(\overline{S R}, \overline{P E}, \operatorname{CEP}\) and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP , are observed.

    \section*{Functional Description (Continued)}

    The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in its maximum count state ( 9 for the decade counters, 15 for the binary counters). To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways.
    These two schemes are shown in the 9310 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the decade counters of the 'LS160, 'LS162, the TC output is fully decoded and can only be HIGH in state 9.
    LOGIC EQUATIONS:
    Count Enable \(=\mathrm{CEP} \cdot \mathrm{CET} \cdot \mathrm{PE}\)
    Mode Select Table
    \begin{tabular}{|l|c|c|c|l|}
    \hline\(* \overline{S R}\) & \(\overline{\text { PE }}\) & CET & CEP & \begin{tabular}{c} 
    Action on the Rising \\
    Clock Edge (
    \end{tabular} \\
    \hline L & X & X & X & RESET (Clear) \\
    H & L & X & X & LOAD \(\left(P_{n} \rightarrow Q_{n}\right)\) \\
    H & H & H & H & COUNT (Increment) \\
    H & H & L & X & NO CHANGE (Hold) \\
    H & H & X & L & NO CHANGE (Hold) \\
    \hline
    \end{tabular}
    *For the 'LS162
    \(H=\) HIGH Voltage Level
    L = LOW Voltage Level
    \(\mathrm{X}=\) Immaterial
    'LS160, 'LS162
    
    

    \section*{54LS161A/DM54LS161A/DM74LS161A, 54LS163A/DM54LS163A/DM74LS163A \\ Synchronous 4-Bit Binary Counters}

    \section*{General Description}

    These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The LS161A and LS163A are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flipflops clocked simultaneously so that the outputs change coincident with each other when so instructed by the countenable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.
    These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable input. Low-to-high transitions at the load input are perfectly acceptable, regardless of the logic levels on the clock or enable inputs. The clear function for the LS161A is asynchronous; and a low level at the clear input sets all four of the flip-flop outputs low, regardless of the levels of clock, load, or enable inputs. The clear function for the LS163A is synchronous; and a low level at the clear inputs sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs.

    The carry look-ahead circuitry provides for cascading counters for \(n\)-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output.
    Both count-enable inputs ( P and T ) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the \(Q_{A}\) output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs may occur, regardless of the logic level of the clock.
    These counters feature a fully independent clock circuit. Changes made to control inputs (enable P or T or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

    \section*{Features}
    - Synchronously programmable
    - Internal look-ahead for fast counting
    - Carry output for n-bit cascading
    - Synchronous counting
    - Load control line
    - Diode-clamped inputs
    - Typical propagation time, clock to Q output 14 ns
    - Typical clock frequency 32 MHz
    - Typical power dissipation 93 mW
    - Alternate Military/Aerospace device (54LS161, 54LS163) is available. Contact a National Semiconductor Sales Office/Distributor for specificaitons.

    \section*{Connection Diagram}
    

    Order Numbers 54LS161ADMQB, 54LS161AFMQB, 54LS161ALMQB, 54LS163ADMQB, 54LS163AFMQB, 54LS163ALMQB, DM54LS161AJ, DM54LS161AW, DM54LS163AJ, DM54LS163AW, DM74LS161AM, DM74LS161AN, DM74LS163AM or DM74LS163AN See NS Package Number E20A, J16A, M16A, N16E or W16A

    \section*{Absolute Maximum Ratings (Note)}

    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avallablilty and specifications.
    Supply Voltage
    Input Voltage
    7 V
    Operating Free Air Temperature Range

    DM54LS and 54LS
    DM74LS
    Storage Temperature Range
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54LS161A} & \multicolumn{3}{|c|}{DM74LS161A} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.7 & & & 0.8 & V \\
    \hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 4 & & & 8 & mA \\
    \hline \multirow[t]{2}{*}{fCLK} & \multicolumn{2}{|l|}{Clock Frequency (Note 1)} & 0 & & 25 & 0 & & 25 & MHz \\
    \hline & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & & 20 & 0 & & 20 & MHz \\
    \hline \multirow[t]{4}{*}{tw} & \multirow[t]{2}{*}{Pulse Width (Note 1)} & Clock & 20 & 6 & & 20 & 6 & & \multirow[t]{2}{*}{ns} \\
    \hline & & Clear & 20 & 9 & & 20 & 9 & & \\
    \hline & \multirow[t]{2}{*}{Pulse Width (Note 2)} & Clock & 25 & & & 25 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Clear & 25 & & & 25 & & & \\
    \hline \multirow[t]{6}{*}{tsu} & \multirow[t]{3}{*}{Setup Time (Note 1)} & Data & 20 & 8 & & 20 & 8 & & \multirow{3}{*}{ns} \\
    \hline & & Enable P & 25 & 17 & & 25 & 17 & & \\
    \hline & & Load & 25 & 15 & & 25 & 15 & & \\
    \hline & \multirow[t]{3}{*}{Setup Time (Note 2)} & Data & 20 & & & 20 & & & \multirow{3}{*}{ns} \\
    \hline & & Enable P & 30 & & & 30 & & & \\
    \hline & & Load & 30 & & & 30 & & & \\
    \hline \multirow[t]{4}{*}{\({ }_{\text {t }}^{\mathrm{H}}\)} & \multirow[t]{2}{*}{Hold Time (Note 1)} & Data & 0 & -3 & & 0 & -3 & & \multirow[t]{2}{*}{ns} \\
    \hline & & Others & 0 & -3 & & 0 & -3 & & \\
    \hline & \multirow[t]{2}{*}{Hold Time (Note 2)} & Data & 5 & & & 5 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Others & 5 & & & 5 & & & \\
    \hline \multirow[t]{2}{*}{\(t_{\text {REL }}\)} & \multicolumn{2}{|l|}{Clear Release Time (Note 1)} & 20 & & & 20 & & & ns \\
    \hline & \multicolumn{2}{|l|}{Clear Release Time (Note 2)} & 25 & & & 25 & & & ns \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}
    over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{V OH} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\
    & V_{I L}=M a x, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline \multirow[t]{4}{*}{1} & \multirow[t]{4}{*}{Input Current @ Max Input Voltage} & \multirow[t]{4}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=7 V
    \end{aligned}
    \]} & Enable T & & & 0.2 & \multirow{4}{*}{mA} \\
    \hline & & & Clock & & & 0.2 & \\
    \hline & & & Load & & & 0.2 & \\
    \hline & & & Others & & & 0.1 & \\
    \hline \multirow[t]{4}{*}{\(\mathrm{IIH}^{\text {H}}\)} & \multirow[t]{4}{*}{High Level Input Current} & \multirow[t]{4}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=2.7 V
    \end{aligned}
    \]} & Enable T & & & 40 & \multirow{4}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & Clock & & & 40 & \\
    \hline & & & Load & & & 40 & \\
    \hline & & & Others & & & 20 & \\
    \hline \multirow[t]{4}{*}{IIL} & \multirow[t]{4}{*}{Low Level Input Current} & \multirow[t]{4}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=M a x \\
    & V_{1}=0.4 V
    \end{aligned}
    \]} & Enable T & & & -0.8 & \multirow{4}{*}{mA} \\
    \hline & & & Clock & & & -0.8 & \\
    \hline & & & Load & & & -0.8 & \\
    \hline & & & Others & & & -0.4 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=M a x \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & DM54 & \(-20\) & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Max} \\
    & (\text { Note 3) }
    \end{aligned}
    \]} & & 18 & 31 & mA \\
    \hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
    & \text { (Note 4) }
    \end{aligned}
    \]} & & 19 & 32 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: \(\mathrm{I}_{\mathrm{CH}}\) is measured with the load high, then again with the load low, with all other inputs high and all outputs open.
    Note 4: ICCL is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.
    'LS161 Switching Characteristics
    at \(V_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{\begin{tabular}{l}
    From (Input) \\
    To (Output)
    \end{tabular}} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(f_{\text {MAX }}\) & Maximum Clock Frequency & & 25 & & 20 & & MHz \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Ripple Carry & & 24 & & 30 & ns \\
    \hline \({ }^{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Ripple Carry & & 30 & & 38 & ns \\
    \hline \({ }_{\text {tpLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Any Q (Load High) & & 22 & & 27 & ns \\
    \hline \({ }^{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Any Q (Load High) & & 27 & & 38 & ns \\
    \hline
    \end{tabular}
    'LS161 Switching Characteristics
    at \(V_{C C}=5 \mathrm{~V}\) and \(T_{A}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load) (Continued)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(\mathrm{t}_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Any Q (Load Low) & & 24 & & 30 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Any Q (Load Low) & & 29 & & 38 & ns \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & Enable T to Ripple Carry & & 18 & & 27 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Enable T to Ripple Carry & & 15 & & 27 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clear to Any Q & & 35 & & 45 & ns \\
    \hline
    \end{tabular}

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54LS163A} & \multicolumn{3}{|c|}{DM74LS163A} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\text {CC }}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(V_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.7 & & & 0.8 & V \\
    \hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 4 & & & 8 & mA \\
    \hline \multirow[t]{2}{*}{\(\mathrm{f}_{\mathrm{CLK}}\)} & \multicolumn{2}{|l|}{Clock Frequency (Note 1)} & 0 & & 25 & 0 & & 25 & MHz \\
    \hline & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & & 20 & 0 & & 20 & MHz \\
    \hline \multirow[t]{4}{*}{\({ }^{\text {tw }}\)} & \multirow[t]{2}{*}{Pulse Width (Note 1)} & Clock & 20 & 6 & & 20 & 6 & & \multirow[t]{2}{*}{ns} \\
    \hline & & Clear & 20 & 9 & & 20 & 9 & & \\
    \hline & \multirow[t]{2}{*}{Pulse Width (Note 2)} & Clock & 25 & & & 25 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Clear & 25 & & & 25 & & & \\
    \hline \multirow[t]{6}{*}{tsu} & \multirow[t]{3}{*}{Setup Time (Note 1)} & Data & 20 & 8 & & 20 & 8 & & \multirow{3}{*}{ns} \\
    \hline & & Enable P & 25 & 17 & & 25 & 17 & & \\
    \hline & & Load & 25 & 15 & & 25 & 15 & & \\
    \hline & \multirow[t]{3}{*}{Setup Time (Note 2)} & Data & 20 & & & 20 & & & \multirow{3}{*}{ns} \\
    \hline & & Enable P & 30 & & & 30 & & & \\
    \hline & & Load & 30 & & & 30 & & & \\
    \hline \multirow[t]{4}{*}{\(\mathrm{t}_{\mathrm{H}}\)} & \multirow[t]{2}{*}{\begin{tabular}{l}
    Hold Time \\
    (Note 1)
    \end{tabular}} & Data & 0 & -3 & & 0 & -3 & & \multirow[t]{2}{*}{ns} \\
    \hline & & Others & 0 & -3 & & 0 & -3 & & \\
    \hline & \multirow[t]{2}{*}{Hold Time (Note 2)} & Data & 5 & & & 5 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Others & 5 & & & 5 & & & \\
    \hline \multirow[t]{2}{*}{\(t_{\text {REL }}\)} & \multicolumn{2}{|l|}{Clear Release Time (Note 1)} & 20 & & & 20 & & & ns \\
    \hline & \multicolumn{2}{|l|}{Clear Release Time (Note 2)} & 25 & & & 25 & & & ns \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note 1: \(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 2: \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{8}{|l|}{'LS163 Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test} \\
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|r|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Any Q (Load Low) & & 24 & & 30 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Any Q (Load Low) & & 29 & & 38 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Enable T to Ripple Carry & & 18 & & 27 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
    Enable \(T\) to \\
    Ripple Carry
    \end{tabular} & & 15 & & 27 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clear to Any Q (Note 1) & & 35 & & 45 & ns \\
    \hline
    \end{tabular}

    Note 1: The propagation delay clear to output is measured from the clock input transition.
    Logic Diagram

    LS163A
    

    The LS161A is similar, however, the clear buffer is connected directly to the flip flops.

    \section*{Parameter Measurement Information}
    

    TL/F/6397-3
    Note A: The input pulses are supplied by generators having the following characteristics: PRR \(\leq 1 \mathrm{MHz}\), duty cycle \(\leq 50 \%, Z_{\text {OUT }} \approx 50 \Omega, \mathrm{t}_{\mathrm{r}} \leq 10 \mathrm{~ns}, \mathrm{t}_{\mathrm{f}} \leq 10 \mathrm{~ns}\). Vary PRR to measure fmax.
    Note B: Outputs \(Q_{D}\) and carry are tested at \(t_{n+16}\) where \(t_{n}\) is the bit time when all outputs are low.
    Note C: \(\mathrm{V}_{\text {REF }}=1.5 \mathrm{~V}\).
    

    TL/F/6397-4
    Note A: The input pulses are supplied by generators having the following characteristics: PRR \(\leq 1 \mathrm{MHz}\), duty cycle \(\leq 50 \%, \mathrm{Z}_{\mathrm{OUT}} \approx 50 \Omega, \mathrm{t}_{\mathrm{r}} \leq 6 \mathrm{~ns}, \mathrm{t}_{\mathrm{f}} \leq 6 \mathrm{~ns}\). Vary PRR to measure \(\mathrm{f}_{\text {MAX }}\).
    Note B: Enable \(P\) and enable \(T\) setup times are measured at \(t_{n+0}\).
    Note C: \(\mathrm{V}_{\text {REF }}=1.3 \mathrm{~V}\).

    \section*{Timing Diagram}

    LS161A, LS163A Synchronous Binary Counters Typical Clear, Preset, Count and Inhibit Sequences
    

    Sequence:
    (1) Clear outputs to zero
    (2) Preset to binary twelve
    (3) Count to thirteen, fourteen, fifteen, zero, one, and two
    (4) Inhibit

    \section*{54LS164/DM54LS164/DM74LS164 8-Bit Serial In/Parallel Out Shift Registers}

    \section*{General Description}

    These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmis-sion-line effects.

    \section*{Features}
    - Gated (enable/disable) serial inputs
    - Fully buffered clock and serial inputs
    - Asynchronous clear
    - Typical clock frequency 36 MHz
    - Typical power dissipation 80 mW
    - Alternate Military/Aerospace device (54LS164) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

    \section*{Connection Diagram}
    

    TL/F/6398-1
    Order Number 54LS164DMQB, 54LS164FMQB, 54LS164LMQB, DM54LS164J, DM54LS164W, DM74LS164M or DM74LS164N See NS Package Number E20A, J14A, M14A, N14A or W14B

    \section*{Function Table}
    \begin{tabular}{|c|c|cc|cccc|}
    \hline \multicolumn{5}{|c|}{ Inputs } & \multicolumn{5}{c|}{ Outputs } \\
    \hline Clear & Clock & \(\mathbf{A}\) & \(\mathbf{B}\) & \(\mathbf{Q}_{\mathbf{A}}\) & \(\mathbf{Q}_{\mathbf{B}}\) & \(\ldots\) & \(\mathbf{Q}_{\mathbf{H}}\) \\
    \hline L & X & X & X & L & L & \(\ldots\) & L \\
    H & L & X & X & \(\mathrm{Q}_{\mathrm{AO}}\) & \(\mathrm{Q}_{\mathrm{BO}}\) & \(\ldots\) & \(\mathrm{Q}_{\mathrm{HO}}\) \\
    H & \(\uparrow\) & H & H & H & \(\mathrm{Q}_{\mathrm{An}}\) & \(\ldots\) & \(\mathrm{Q}_{\mathrm{Gn}}\) \\
    H & \(\uparrow\) & L & X & L & \(\mathrm{Q}_{\mathrm{An}}\) & \(\ldots\) & \(\mathrm{Q}_{\mathrm{Gn}}\) \\
    H & \(\uparrow\) & X & L & L & \(\mathrm{Q}_{\mathrm{An}}\) & \(\ldots\) & \(\mathrm{Q}_{\mathrm{Gn}}\) \\
    \hline
    \end{tabular}
    \(H=\) High Level (steady state), L = Low Level (steady state)
    \(X=\) Don't Care (any input, including transitions)
    \(\uparrow=\) Transition from low to high level
    \(Q_{A 0}, Q_{B 0}, Q_{H 0}=\) The level of \(Q_{A}, Q_{B}\), or \(Q_{H}\), respectively, before the indicated steady-state input conditions were established.
    \(Q_{A n}, Q_{G n}=\) The level of \(Q_{A}\) or \(Q_{G}\) before the most recent \(\uparrow\) transition of the clock; indicates a one-bit shift.

    \section*{Logic Diagram}
    

    \section*{Absolute Maximum Ratings (Note)}

    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    \begin{tabular}{lr} 
    Supply Voltage & 7 V \\
    Input Voltage & 7 V \\
    Operating Free Air Temperature Range & \\
    \(\quad\) DM54LS and 54LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Input Voltage
    Operating Free Air Temperature Range
    DM54LS and 54LS
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    Storage Temperature Range
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Recommended Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|r|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54LS164} & \multicolumn{3}{|c|}{DM74LS164} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{\text {l }}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & & & -0.4 & mA \\
    \hline \(\mathrm{lOL}^{2}\) & \multicolumn{2}{|l|}{Low Level Output Current} & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 4)} & 0 & & 25 & 0 & & 25 & MHz \\
    \hline \multirow[t]{2}{*}{\(t_{\text {W }}\)} & \multirow[t]{2}{*}{Pulse Width (Note 4)} & Clock & 20 & & & 20 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Clear & 20 & & & 20 & & & \\
    \hline tsu & \multicolumn{2}{|l|}{Data Setup Time (Note 4)} & 17 & & & 17 & & & ns \\
    \hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Data Hold Time (Note 4)} & 5 & & & 5 & & & ns \\
    \hline \(t_{\text {REL }}\) & \multicolumn{2}{|l|}{Clear Release Time (Note 4)} & 30 & & & 30 & & & ns \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \begin{tabular}{l}
    Typ \\
    (Note 1)
    \end{tabular} & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O H}=M a x \\
    & V_{I L}=M a x, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & V \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O L}=\operatorname{Max} \\
    & V_{I L}=M a x, V_{I H}=M i n
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{I}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline 1 LL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & DM54 & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\) (Note 3)} & & 16 & 27 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: ICC is measured with all outputs open, the SERIAL input grounded, the CLOCK input at 2.4 V , and a momentary ground, then 4.5 V , applied to the CLEAR input.
    Note 4: \(T_{A}=25^{\circ} \mathrm{C}\) and \(V_{C C}=5 \mathrm{~V}\).

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 25 & & & & MHz \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Output & & 27 & & 30 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Output & & 32 & & 40 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clear to Output & & 36 & & 45 & ns \\
    \hline
    \end{tabular}

    Timing Diagram
    

    TL/F/6398-3

    \section*{54LS165/DM74LS165 8-Bit Parallel In/Serial Output Shift Registers}

    \section*{General Description}

    This device is an 8 -bit serial shift register which shifts data in the direction of \(Q_{A}\) toward \(Q_{H}\) when clocked. Parallel-in access is made available by eight individual direct data inputs, which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.
    Clocking is accomplished through a 2 -input NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high.

    Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input, regardless of the logic levels on the clock, clock inhibit, or serial inputs.

    \section*{Features}
    - Complementary outputs
    - Direct overriding (data) inputs
    - Gated clock inputs
    - Parallel-to-serial data conversion
    - Typical frequency 35 MHz
    

    \section*{Connection Diagram}
    

    TL/F/6399-1
    Order Number 54LS165DMQB, 54LS165FMQB, DM74LS165WM or DM74LS165N See NS Package Number J16A, M16B, N16E or W16A
    Function Table
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{5}{|c|}{Inputs} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Internal Outputs}} & \multirow[b]{3}{*}{Output \(\mathbf{Q}_{\mathbf{H}}\)} \\
    \hline \multirow[t]{2}{*}{Shift/ Load} & \multirow[t]{2}{*}{Clock Inhibit} & \multirow[t]{2}{*}{Clock} & \multirow[t]{2}{*}{Serial} & Parallel & & & \\
    \hline & & & & A...H & \(\mathbf{Q}_{\mathbf{A}}\) & \(\mathrm{Q}_{\mathrm{B}}\) & \\
    \hline L & X & X & X & a...h & a & b & h \\
    \hline H & L & L & X & X & \(Q_{\text {AO }}\) & \(Q_{B 0}\) & \(Q_{\text {Ho }}\) \\
    \hline H & L & \(\uparrow\) & H & \(x\) & H & \(Q_{A n}\) & \(Q_{G n}\) \\
    \hline H & L & \(\uparrow\) & L & X & L & \(Q_{A n}\) & \(Q_{G n}\) \\
    \hline H & H & X & X & X & \(Q_{A O}\) & \(\mathrm{Q}_{\mathrm{BO}}\) & \(Q_{\text {Ho }}\) \\
    \hline
    \end{tabular}
    \(H=\) High Level (steady state), L = Low Level (steady state)
    \(X=\) Don't Care (any input, including transitions)
    \(\uparrow=\) Transition from low-to-high level
    a... \(h=\) The level of steady-state input at inputs \(A\) through \(H\), respectively.
    \(Q_{A 0}, Q_{B 0}, Q_{H 0}=\) The level of \(Q_{A}, Q_{B}\), or \(Q_{H}\), respectively, before the indicated steady-state input conditions were established.
    \(Q_{A n}, Q_{G n}=\) The level of \(Q_{A}\) or \(Q_{G}\), respectively, before the most recent \(\uparrow\) transition of the clock.

    \section*{Absolute Maximum Ratings (Note)}

    If Military/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for availablity and specifications.
    Supply Voltage
    Input Voltage
    \(7 V\)
    Operating Free Air Temperature Range
    54LS
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    DM74LS
    Storage Temperature Range

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{54LS165} & \multicolumn{3}{|c|}{DM74LS165} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.7 & & & 0.8 & V \\
    \hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 1)} & & & 30 & 0 & & 25 & MHz \\
    \hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & & & & 0 & & 20 & MHz \\
    \hline \multirow[t]{2}{*}{tw} & \multirow[t]{2}{*}{Pulse Width (Note 2)} & Clock & 18 & & & 25 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Load & 15 & & & 15 & & & \\
    \hline \multirow[t]{4}{*}{tsu} & \multirow[t]{4}{*}{Setup Time (Note 6)} & Parallel & 10 & & & 10 & & & \multirow{4}{*}{ns} \\
    \hline & & Serial & 10 & & & 20 & & & \\
    \hline & & Enable & 10 & & & 30 & & & \\
    \hline & & Shift & 10 & & & 45 & & & \\
    \hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Hold Time (Note 6)} & 5 & & & 0 & & & ns \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 3) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOH}_{\mathrm{OH}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & 54LS & 2.5 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\
    & V_{I L}=M a x, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \multicolumn{2}{|l|}{\(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\)} & & 0.25 & 0.4 & \\
    \hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current @ Max Input Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x, V_{1}=7 V(D M 74) \\
    & V_{1}=10 V(54 L S)
    \end{aligned}
    \]} & Shift/Load & & & 0.3 & \multirow[t]{2}{*}{mA} \\
    \hline & & & Others & & & 0.1 & \\
    \hline \multirow[t]{2}{*}{1 IH} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{I}=2.7 V
    \end{aligned}
    \]} & Shift/Load & & & 60 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & Others & & & 20 & \\
    \hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=0.4 V
    \end{aligned}
    \]} & Shift/Load & & & -1.2 & \multirow[t]{2}{*}{mA} \\
    \hline & & & Others & & & -0.4 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
    & \text { (Note 4) }
    \end{aligned}
    \]} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 5)} & & 21 & 36 & mA \\
    \hline
    \end{tabular}

    Note 1: \(C_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\)
    Note 2: \(C_{L}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\)
    Note 3: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 5: With all outputs open, clock inhibit and shift/load at 4.5 V , and a clock pulse applied to the CLOCK input, IcC is measured first with the parallel inputs at 4.5 V , then again grounded.

    Note 6: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{From (Input) To (Output)} & \multicolumn{2}{|c|}{54LS} & \multicolumn{2}{|c|}{DM74LS} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & R_{L}=2 \mathrm{k} \Omega \\
    & C_{L}=50 \mathrm{pF}
    \end{aligned}
    \]} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 25 & & 20 & & MHz \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Load to Any Q & & 30 & & 37 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
    Load to \\
    Any Q
    \end{tabular} & & 30 & & 42 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Any Q & & 30 & & 42 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Any Q & & 30 & & 47 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    H \\
    \text { to } Q_{H}
    \end{gathered}
    \] & & 20 & & 27 & ns \\
    \hline tPHL & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    H \\
    \text { to } Q_{H} \\
    \hline
    \end{gathered}
    \] & & 30 & & 37 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{aligned}
    & \mathrm{H} \\
    & \text { to } \overline{\mathrm{Q}}_{\mathrm{H}}
    \end{aligned}
    \] & & 30 & & 32 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{aligned}
    & \mathrm{H} \\
    & \text { to } \overline{\mathrm{Q}}_{\mathrm{H}}
    \end{aligned}
    \] & & 25 & & 32 & ns \\
    \hline
    \end{tabular}

    \section*{Timing Diagram}
    
    

    \section*{DM74LS166}

    \section*{8-Bit Parallel-In/Serial-Out Shift Registers}

    \section*{General Description}

    These parallel-in or serial-in, serial-out shift registers feature gated clock inputs and an overriding clear input. All inputs are buffered to lower the drive requirements to one normalized load, and input clamping diodes minimize switching transients to simplify system design. The load mode is established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on
    the low-to-high-level edge of the clock pulse through a twoinput NOR gate, permitting one input to be used as a clockenable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running, and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

    \section*{Connection Diagram}
    

    TL/F/6400-1

    \section*{Function Table}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{6}{|c|}{Inputs} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Internal Outputs}} & \multirow{3}{*}{Output \(\mathbf{Q}_{\mathbf{H}}\)} \\
    \hline \multirow[t]{2}{*}{Clear} & \multirow[t]{2}{*}{Shift/ Load} & \multirow[t]{2}{*}{Clock Inhibit} & \multirow[t]{2}{*}{Clock} & \multirow[t]{2}{*}{Serial} & Parallel & & & \\
    \hline & & & & & A...H & \(\mathbf{Q}_{\mathbf{A}}\) & \(\mathrm{Q}_{\mathrm{B}}\) & \\
    \hline L & X & X & X & X & X & L & L & L \\
    \hline H & X & L & L & X & X & \(Q_{\text {A0 }}\) & \(Q_{B 0}\) & Q \({ }_{\text {Ho }}\) \\
    \hline H & L & L & \(\uparrow\) & X & a...h & a & b & h \\
    \hline H & H & L & \(\uparrow\) & H & X & H & \(Q_{\text {An }}\) & \(Q_{G n}\) \\
    \hline H & H & L & \(\uparrow\) & L & X & L & \(Q_{A n}\) & \(Q_{G n}\) \\
    \hline H & X & H & \(\uparrow\) & X & X & \(Q_{A 0}\) & \(\mathrm{Q}_{\mathrm{BO}}\) & \(\mathrm{Q}_{\mathrm{HO}}\) \\
    \hline
    \end{tabular}

    \footnotetext{
    \(H=\) High Level (steady state), L = Low Level (steady state)
    \(X=\) Don't Care (any input, including transitions)
    \(\uparrow=\) Transition from low to high level
    a ... \(h=\) The level of steady-state input at inputs \(A\) through \(H\), respectively
    \(Q_{A 0}, Q_{B 0}, Q_{H 0}=\) The level of \(Q_{A}, Q_{B}, Q_{H}\), respectively, before the indicated steady-state input conditions were established \(Q_{A n}, Q_{G n}=\) The level of \(Q_{A}, Q_{G}\), respectively, before the most recent \(\uparrow\) transition of the clock
    }
    \begin{tabular}{|c|c|}
    \hline \multicolumn{2}{|l|}{Absolute Maximum Ratings (Note)} \\
    \hline If Military/Aerospace specified please contact the National & ces are requil conductor \\
    \hline Supply Voltage & \\
    \hline Input Voltage & \\
    \hline Operating Free Air Temperature Rang DMM4LS & \(0^{\circ} \mathrm{C}\) to + \\
    \hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \\
    \hline
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM74LS166} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & \\
    \hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{\text {l }}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 8 & mA \\
    \hline \multirow[t]{2}{*}{\(\mathrm{f}_{\text {CLK }}\)} & \multicolumn{2}{|l|}{Clock Frequency (Note 1)} & 0 & & 25 & MHz \\
    \hline & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & & 20 & MHz \\
    \hline \multirow[t]{2}{*}{tw} & \multirow[t]{2}{*}{Pulse Width (Note 6)} & Clock & 20 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Clear & 20 & & & \\
    \hline \multirow[t]{2}{*}{tsu} & \multirow[t]{2}{*}{Setup Time (Note 6)} & Mode & 30 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Data & 20 & & & \\
    \hline \(t_{H}\) & \multicolumn{2}{|l|}{Hold Time (Note 6)} & 0 & & & ns \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & Typ (Note 3) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\) & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \] & 2.7 & 3.4 & & V \\
    \hline \multirow[t]{2}{*}{VOL} & \multirow[t]{2}{*}{Low Level Output Voltage} & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \] & & 0.35 & 0.5 & \multirow[t]{2}{*}{V} \\
    \hline & & \(\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}\) & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\) & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \(1 / 1\) & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -0.4 & mA \\
    \hline los & Short Circuit Output Current & \[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 4) } \\
    & \hline
    \end{aligned}
    \] & -20 & & -100 & mA \\
    \hline ICC & Supply Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 5) & & 22 & 38 & mA \\
    \hline
    \end{tabular}

    Note 1: \(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 2: \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 3: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 5: With all outputs open, 4.5 V applied to the serial input, all other inputs except the CLOCK grounded, ICc is measured after a momentary ground, then 4.5 V is applied to the CLOCK.
    Note 6: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 25 & & 20 & & MHz \\
    \hline \({ }_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output & Clock to Output & 8 & 35 & & 38 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Output & 8 & 35 & & 41 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clear to Output & 6 & 30 & & 36 & ns \\
    \hline
    \end{tabular}

    \section*{Parameter Measurement Information}
    

    Note A: The clock pulse has the following characteristics: \(t_{\text {W(clock) }} \geq 20 \mathrm{~ns}\) and PRR \(=1 \mathrm{MHz}\). The clear pulse has the following characteristics: tw(clear) \(\geq 20 \mathrm{~ns}\) and \(t_{\text {HOLD }}=0 \mathrm{~ns}\). When testing fmAx, vary the clock PRR.
    Note B: A clear pulse is applied prior to each test.
    Note C: Propagation delay times ( \(t_{p L H}\) and \(t_{P H L}\) ) are measured at \(t_{n+1}\). Proper shifting of data is verified at \(t_{n+8}\) with a functional test.
    Note \(\mathrm{D}: \mathrm{t}_{\mathrm{n}}=\) bit time before clocking transition
    \(t_{n+1}=\) bit time after one clocking transition
    \(t_{n+8}=\) bit time after eight clocking transitions
    Note E: \(\mathrm{V}_{\text {REF }}=1.3 \mathrm{~V}\).

    Logic Diagram
    

    Timing Diagram
    

    \section*{54LS168 Synchronous Bi-Directional BCD Decade Counter}

    \section*{General Description}

    The 54LS168 is a fully synchronous 4-state up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/D input to control the direction of counting. It counts in the BCD (8421) sequence and all state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

    \section*{Connection Diagram}

    \section*{Logic Symbol}
    

    TL/F/10207-1
    

    54LS168FMQB or 54LS168LMQB
    See NS Package Number
    E20A, J16A or W16A
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
    \hline\(\overline{\mathrm{CEP}}\) & Count Enable Parallel Input (Active LOW) \\
    \(\overline{\mathrm{CET}}\) & Count Enable Trickle Input (Active LOW) \\
    CP & Clock Pulse Input (Active Rising Edge) \\
    \(\mathrm{PO}-\mathrm{P3}\) & Parallel Data Inputs \\
    \(\overline{\mathrm{PE}}\) & Parallel Enable Input (Active LOW) \\
    \(\mathrm{U} / \overline{\mathrm{D}}\) & Up-Down Count Control Input \\
    \(\mathrm{QO}-\mathrm{Q3}\) & Flip-Flop Outputs \\
    \(\overline{\mathrm{TC}}\) & Terminal Count Output (Active LOW) \\
    \hline
    \end{tabular}
    ```

    Absolute Maximum Ratings (Note)
    If Milltary/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for availability and specifications.

    | Supply Voltage | 7 V |
    | :--- | ---: |
    | Input Voltage | 5.5 V |
    | Operating Free Air Temperature Range |  |
    | $\quad 54 \mathrm{LS}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
    | Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

    ```

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS168} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & V \\
    \hline IOH & High Level Output Current & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & t_{s}(H) \\
    & t_{s}(L)
    \end{aligned}
    \] & Setup Time HIGH or LOW \(P_{n}, \overline{C E P}\) or \(\overline{\text { CET }}\) to CP & \[
    \begin{aligned}
    & 15 \\
    & 15 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L) \\
    & \hline
    \end{aligned}
    \] & Hold Time HIGH or LOW \(P_{n}, \overline{\text { CEP }}\) or \(\overline{\text { CET }}\) to CP & \[
    \begin{aligned}
    & 5 \\
    & 5
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{S}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW \(\overline{\text { PE to CP }}\) & \[
    \begin{array}{r}
    20 \\
    20 \\
    \hline
    \end{array}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L)
    \end{aligned}
    \] & Hold Time HIGH or LOW \(\overline{\text { PE to CP }}\) & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{s}(H) \\
    & t_{s}(L)
    \end{aligned}
    \] & Setup Time HIGH or LOW U/D to CP & \[
    \begin{array}{r}
    25 \\
    25 \\
    \hline
    \end{array}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L)
    \end{aligned}
    \] & Hold Time HIGH or LOW \(U / \bar{D}\) to \(C P\) & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{w}(H) \\
    & t_{w}(L)
    \end{aligned}
    \] & CP Pulse Width HIGH or LOW & \[
    \begin{array}{r}
    20 \\
    20 \\
    \hline
    \end{array}
    \] & & & ns \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline VOH & High Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 2.5 & & & V \\
    \hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min}, I_{\mathrm{OL}}=\operatorname{Max}, \\
    & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 0.4 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\) Max, \(V_{1}=10.0 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \multirow[t]{2}{*}{\({ }_{1 /}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\(V_{C C}=\operatorname{Max}, V_{1}=2.7 \mathrm{~V}\)} & Inputs & & & 20 & \multirow{2}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & CET & & & 40 & \\
    \hline \multirow[t]{3}{*}{ILL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\)} & Data & -0.5 & & -400 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & CP, PE, U/D, \(\overline{\mathrm{CEP}}\) & -30 & & -400 & \\
    \hline & & & \(\overline{\text { CET }}\) & -60 & & -800 & \\
    \hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 2)} & -20 & & -100 & mA \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 3)} & & & 34 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: Icc is measured with all outputs open and all inputs grounded.

    \section*{Switching Characteristics}
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for test waveforms and output load)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{2}{|c|}{54LS168} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \\
    \hline & & Min & Max & \\
    \hline \(\mathrm{f}_{\text {Max }}\) & Maximum Clock Frequency & 25 & & MHz \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(t_{\text {PHL }}\)
    \end{tabular} & Propagation Delay \(C P\) to \(Q_{n}\) & & \[
    \begin{array}{r}
    20 \\
    20 \\
    \hline
    \end{array}
    \] & ns \\
    \hline \[
    t_{\text {PLH }}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & Propagation Delay CP to TC & & \[
    \begin{aligned}
    & 30 \\
    & 30 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    tpHL
    \end{tabular} & Propagation Delay \(\overline{\mathrm{CET}}\) to \(\overline{\mathrm{TC}}\) & & \[
    \begin{array}{r}
    15 \\
    20 \\
    \hline
    \end{array}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}}
    \end{aligned}
    \] & Propagation Delay \(U / \bar{D}\) to \(\overline{T C}\) & & \[
    \begin{aligned}
    & 25 \\
    & 25 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}

    \section*{Functional Description}

    The 'LS168 uses edge-triggered D-type flip-flops and has no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When PE is LOW, the data on the PO-P3 inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both CEP and \(\overline{C E T}\) must be LOW and \(\overline{\text { PE }}\) must be HIGH. The U/ \(\overline{\mathrm{D}}\) input then determines the direction of counting. The Terminal Count ( \(\overline{\mathrm{TC}}\) ) output is normally HIGH and goes LOW, provided that CET is LOW, when a counter reaches zero in the COUNT DOWN mode or reaches 9 in the COUNT UP mode. The \(\overline{T C}\) output state is not a function of the Count Enable Parallel ( \(\overline{\mathrm{CEP}}\) ) input level. The \(\overline{\mathrm{TC}}\) output of the 'LS168 decade counter can also be LOW in the illegal states 11,13 and 15 , which can occur when power is turned on or via parallel loading. If an illegal state occurs, the 'LS168 will return to the legitimate sequence within two counts. Since the \(\overline{T C}\) signal is derived by decoding the flipflop states, there exists the possibility of decoding spikes on \(\overline{T C}\). For this reason the use of \(\overline{T C}\) as a clock signal is not recommended (see logic equation below).
    1. Count Enable \(=\overline{\mathrm{CEP}} \cdot \overline{\mathrm{CET}} \cdot \overline{\mathrm{PE}}\)
    2. Up: \(\overline{T C}=Q 0 \bullet Q 3 \cdot(U / \bar{D}) \cdot \overline{C E T}\)
    3. Down: \(\overline{T C}=Q 0 \cdot Q 1 \bullet Q 2 \cdot Q 3 \bullet(U / \bar{D}) \cdot \overline{C E T}\)
    'LS168 Mode Select Table
    \begin{tabular}{|c|c|c|c|l|}
    \hline\(\overline{\text { PE }}\) & \(\overline{\text { CEP }}\) & \(\overline{\text { CET }}\) & U/D & Action on Rising Clock Edge \\
    \hline L & X & X & X & Load \(\left(P_{n} \rightarrow Q_{n}\right)\) \\
    H & L & L & H & Count Up (increment) \\
    H & L & L & L & Count Down (Decrement) \\
    H & H & X & X & No Change (Hold) \\
    H & X & H & X & No Change (Hold) \\
    \hline
    \end{tabular}

    H \(=\) HIGH Voltage Level
    L = LOW Voltage Level
    \(X=\) Immaterial

    \section*{State Diagram}
    

    TL/F/10207-3

    \section*{Logic Diagram}
    

    TL/F/10207-4

    \section*{54LS169/DM54LS169A/DM74LS169A Synchronous 4-Bit Up/Down Binary Counter}

    \section*{General Description}

    This synchronous presettable counter features an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs all change at the same time when so instructed by the countenable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising edge of the clock waveform.
    This counter is fully programmable; that is, the outputs may each be preset either high or low. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse. The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count-enable inputs ( \(\overline{\mathrm{P}}\) and \(\overline{\mathrm{T}}\) ) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input T is fed forward to enable the carry outputs. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the \(Q_{A}\) output when
    counting up, and approximately equal to the low portion of the \(Q_{A}\) output when counting down. This low-level overflow carry pulse can be used to enable successively cascaded stages. Transitions at the enable \(\overline{\mathrm{P}}\) or \(\overline{\mathrm{T}}\) inputs are allowed regardless of the level of the clock input. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.
    This counter features a fully independent clock circuit. Changes at control inputs (enable \(\overline{\mathrm{P}}\), enable \(\overline{\mathrm{T}}\), load, up/ down), which modify the operating mode, have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

    \section*{Features}
    - Fully synchronous operation for counting and programming.
    - Internal look-ahead for fast counting.
    - Carry output for n-bit cascading.
    - Fully independent clock circuit
    - Alternate Military/Aerospace device (54LS169) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

    \section*{Connection Diagram}
    

    \section*{Absolute Maximum Ratings (Note)}

    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    \begin{tabular}{ll} 
    Supply Voltage & 7 V \\
    Input Voltage & 7 V
    \end{tabular}

    Input Voltage
    Operating Free Air Temperature Range
    DM54LS and 54LS
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    DM74LS
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    Storage Temperature Range
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54LS169A} & \multicolumn{3}{|c|}{DM74LS169A} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline VCC & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{lOH}^{2}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & & & -0.4 & mA \\
    \hline loL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 4 & & & 8 & mA \\
    \hline \multirow[t]{2}{*}{\({ }_{\text {f CLK }}\)} & \multicolumn{2}{|l|}{Clock Frequency (Note 1)} & 0 & & 25 & 0 & & 25 & MHz \\
    \hline & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & & 20 & 0 & & 20 & MHz \\
    \hline tw & \multicolumn{2}{|l|}{Clock Pulse Width (Note 3)} & 25 & & & 25 & & & ns \\
    \hline \multirow[t]{4}{*}{tsu} & \multirow[t]{4}{*}{Setup Time (Note 3)} & Data & 20 & & & 20 & & & \multirow{4}{*}{ns} \\
    \hline & & Enable \(\bar{T}\) or \(\overline{\mathrm{P}}\) & 20 & & & 20 & & & \\
    \hline & & Load & 25 & & & 25 & & & \\
    \hline & & U/D & 30 & & & 30 & & & \\
    \hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Hold Time (Note 3)} & 0 & & & 0 & & & ns \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note 1: \(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 2: \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 3: \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 4) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{VOL} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current @ Max Input Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=7 V
    \end{aligned}
    \]} & Enable \(\bar{T}\) & & & 0.2 & \multirow[t]{2}{*}{mA} \\
    \hline & & & Others & & & 0.1 & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{I}_{\mathrm{H}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=2.7 V
    \end{aligned}
    \]} & Enable \(\bar{T}\) & & & 40 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & Others & & & 20 & \\
    \hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=0.4 V
    \end{aligned}
    \]} & Enable T & & & -0.8 & \multirow[t]{2}{*}{mA} \\
    \hline & & & Others & & & -0.4 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
    & (\text { Note } 5)
    \end{aligned}
    \]} & DM54 & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline Icc & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}\) (Note 6)} & & 20 & 34 & mA \\
    \hline
    \end{tabular}

    Note 4: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 6: ICC is measured after a momentary 4.5 V , then ground, is applied to the CLOCK with all other inputs grounded and all the outputs open.
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[b]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 25 & & 20 & & MHz \\
    \hline \({ }_{\text {tple }}\) & Propagation Delay Time Low to High Level Output & Clock to Ripple Carry & & 35 & & 39 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Ripple Carry & & 35 & & 44 & ns \\
    \hline \({ }_{\text {tple }}\) & Propagation Delay Time Low to High Level Output & Clock to Any Q & & 20 & & 24 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Any Q & & 23 & & 32 & ns \\
    \hline \({ }_{\text {tpLH }}\) & Propagation Delay Time Low to High Level Output & Enable \(\bar{T}\) to Ripple Carry & & 18 & & 24 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Enable \(\bar{T}\) to Ripple Carry & & 18 & & 28 & ns \\
    \hline \(\mathrm{t}_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Up/Down to Ripple Carry (Note 1) & & 25 & & 30 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Up/Down to Ripple Carry (Note 1) & & 29 & & 38 & ns \\
    \hline
    \end{tabular}

    Note 1: The propagation delay from UP/DOWN to RIPPLE CARRY must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum, the ripple carry output transition will be in phase. If the count is maximum, the ripple carry output will be out of phase.
    

    TL/F/6401-2

    Timing Diagram
    LS169A Binary Counters
    Typical Load, Count, and Inhibit Sequences
    

    TL/F/6401-3

    National Semiconductor

    \section*{54LS170/DM74LS170}
    \(4 \times 4\) Register File with Open-Collector Outputs

    \section*{General Description}

    The 'LS170 contains 16 high speed, low power, transparent D-type latches arranged as four words of four bits each, to function as a \(4 \times 4\) register file. Separate read and write inputs, both address and enable, allow simultaneous read and write operation. Open-collector outputs make it possible to connect up to 128 outputs in a wired-AND configuration to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length. The '670 provides a similar function to this device but it features TRI-STATE \({ }^{\text {© }}\) outputs.

    \section*{Features}
    - Simultaneous read/write operation
    - Expandable to 512 words of n-bits
    - Typical access time of 20 ns
    - Low leakage open-collector outputs for expansion

    \section*{Connection Diagram}
    

    Order Number 54LS170DMQB, 54LS170FMQB, DM74LS170WM or DM74LS170N
    See NS Package Number J16A, M16B, N16E or W16A

    \section*{Logic Symbol}
    

    TL/F/9820-2
    \[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Pin} 16 \\
    & \mathrm{GND}=\operatorname{Pin} 8
    \end{aligned}
    \]
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{c|}{ Description } \\
    \hline D1-D4 & Data Inputs \\
    WAO-WA1 & Write Address Inputs \\
    \(\overline{W E}\) & Write Enable Input (Active LOW) \\
    RAO, RA1 & Read Address Inputs \\
    \(\overline{\text { RE }}\) & Read Enable Input (Active LOW) \\
    O1-O4 & Data Outputs \\
    \hline
    \end{tabular}

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    \begin{tabular}{lr}
    54 LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74 & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS170} & \multicolumn{3}{|c|}{DM74LS170} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{\text {l }}\) & High Level Output Current & & & 20 & & & 20 & \(\mu \mathrm{A}\) \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \(\mathrm{t}_{\text {s }}\) & Setup Time HIGH or LOW Dn to Rising \(\overline{W E}\) & 10 & & & 10 & & & ns \\
    \hline \(t_{h}\) & Hold Time HIGH or LOW Dn to Rising \(\overline{\text { WE }}\) & 5.0 & & & 5.0 & & & ns \\
    \hline \(\mathrm{t}_{\text {s }}\) & Setup Time HIGH or LOW WAn to Falling WE & 10 & & & 10 & & & ns \\
    \hline \(t_{n}\) & Hold Time HIGH or LOW WAn to Rising \(\overline{W E}\) & 5.0 & & & 5.0 & & & ns \\
    \hline \(t_{w}(\mathrm{~L})\) & \(\overline{\text { WE }}\) or \(\overline{\text { RE }}\) Pulse Width LOW & 25 & & & 25 & & & ns \\
    \hline
    \end{tabular}

    \section*{Electrical Characteristics}

    Over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Uints \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min}, I_{\mathrm{OH}}=\operatorname{Max}, \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & 54LS & 2.0 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O L}=M a x, \\
    & V_{I H}=M i n
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current @ Max Input Voltage} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=10 \mathrm{~V}\)} & Dns, RAO, WAO & & & 0.1 & \multirow[t]{2}{*}{mA} \\
    \hline & & & \(\overline{\text { WE, }} \overline{\mathrm{RE}}\) & & & 0.2 & \\
    \hline \multirow[t]{2}{*}{\({ }_{1 H}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & Inputs & & & 20 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & \(\overline{\mathrm{RE}}, \overline{\mathrm{WE}}\) & & & 40 & \\
    \hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}\)} & \(\overline{\mathrm{RE}}, \overline{\mathrm{WE}}\) & -0.06 & & -0.8 & \multirow{3}{*}{mA} \\
    \hline & & & RA1, WA1 & -0.05 & & -0.4 & \\
    \hline & & & DATA, RAO, WAO & -0.03 & & -0.4 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Max}, \mathrm{Dn}, \overline{\mathrm{WE}}, \\
    & \overline{\mathrm{RE}}=4.5 \mathrm{~V}, \mathrm{WAn}, \mathrm{RAn}=\mathrm{GND}
    \end{aligned}
    \]} & & & 40 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    Switching Characteristics
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\), (See Section 1 for waveforms and load configurations)
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Conditions} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k}, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Max & \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    tpHL
    \end{tabular} & Propagation Delay* RAO or RA1 to On & & & \[
    \begin{aligned}
    & 35 \\
    & 35 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(\mathrm{t}_{\mathrm{PHL}}\)
    \end{tabular} & Propagation Delay \(\overline{R E}\) to On & & & \[
    \begin{aligned}
    & 30 \\
    & 30
    \end{aligned}
    \] & ns \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(t_{\text {PHL }}\)
    \end{tabular} & Propagation Delay \(\overline{W E}\) to On & & & \[
    \begin{aligned}
    & 35 \\
    & 35 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    tpHL
    \end{tabular} & Propagation Delay Dn to On & & & \[
    \begin{aligned}
    & 35 \\
    & 35
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}
    *Measured at least 25 ns after entry of new data at selected location.

    \section*{Switching Waveforms}
    

    TL/F/9820-4
    FIGURE a

    Write Function Table
    \begin{tabular}{|c|cc|l|}
    \hline \multicolumn{3}{|c|}{ Write Inputs } & \multirow{2}{*}{ D Inputs to } \\
    \hline WE & WA1 & WAO & \\
    \hline L & L & L & Word 0 \\
    L & L & H & Word 1 \\
    L & H & L & Word 2 \\
    L & H & H & Word 3 \\
    H & X & X & None (Hold) \\
    \hline
    \end{tabular}
    \(H=H I G H\) Voltage Level
    \(\mathrm{L}=\) LOW Voltage Level

    Read Function Table
    \begin{tabular}{|c|cc|l|}
    \hline \multicolumn{3}{|c|}{ Read Inputs } & \multirow{2}{*}{ Outputs from } \\
    \cline { 1 - 3 }\(\overline{\text { RE }}\) & RA1 & RA0 & \\
    \hline L & L & L & Word 0 \\
    L & L & H & Word 1 \\
    L & H & L & Word 2 \\
    L & H & H & Word 3 \\
    H & X & X & None (High Z) \\
    \hline
    \end{tabular}
    \(X=\) Immaterial
    

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    \section*{54LS173/DM74LS173A} TRI-STATE \({ }^{\circledR}\) 4-Bit D-Type Register

    \section*{General Description}

    This four-bit register contains D-type flip-flops with totempole TRI-STATE® outputs, capable of driving highly capacitive or low-impedance loads. The high-impedance state and increased high-logic-level drive provide these flip-flops with the capability of driving the bus lines in a bus-organized system without need for interface or pull-up components.
    Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flipflops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the truth table.

    To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

    \section*{Features}
    - TRI-STATE outputs interface directly with system bus
    - Gated output control lines for enabling or disabling the outputs
    - Fully independent clock eliminates restrictions for operating in one of two modes:
    Parallel load
    Do nothing (hold)
    - For application as bus buffer registers

    \section*{Connection Diagram}
    

    OUTPUT CONTROL OUTPUTS
    TL/F/6403-1
    Order Number 54LS173DMQB, 54LS173FMQB, 54LS173LMQB, DM74LS173AM or DM74LS173AN See NS Package Number E20A, J16A, M16A, N16E or W16A

    \section*{Function Table}
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multicolumn{5}{|c|}{Inputs} & \multirow{3}{*}{Output Q} \\
    \hline \multirow[t]{2}{*}{Clear} & \multirow[t]{2}{*}{Clock} & \multicolumn{2}{|c|}{\begin{tabular}{l}
    Data \\
    Enable
    \end{tabular}} & \multirow[b]{2}{*}{Data D} & \\
    \hline & & G1 & G2 & & \\
    \hline H & X & X & X & X & L \\
    \hline L & L & X & X & X & \(Q_{0}\) \\
    \hline L & \(\uparrow\) & H & X & X & \(Q_{0}\) \\
    \hline L & \(\uparrow\) & X & H & X & \(Q_{0}\) \\
    \hline L & \(\uparrow\) & L & L & L & L \\
    \hline L & \(\uparrow\) & L & L & H & H \\
    \hline
    \end{tabular}

    When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

    H = High Level (Steady State)
    L = Low Level (Steady State)
    \(\uparrow=\) Low-to-High Level Transition
    \(X=\) Don't Care (Any Input Including Transitions)
    \(\mathrm{Q}_{0}=\) The Level of Q Before the Indicated Steady State Input Conditions Were Established.

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the Natlonal Semiconductor Sales Office/Distributors for avallability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    54LS
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) DM74LS
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    Storage Temperature Range
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    Recommended Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{54LS173} & \multicolumn{3}{|c|}{DM74LS173A} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{2}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -1 & & & -2.6 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 12 & & & 24 & mA \\
    \hline \multirow[t]{2}{*}{\(f_{\text {fle }}\)} & \multicolumn{2}{|l|}{Clock Frequency (Note 1)} & 30 & & & 0 & & 30 & MHz \\
    \hline & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & & & & 0 & & 20 & MHz \\
    \hline \multirow[t]{2}{*}{\({ }^{\text {tw }}\)} & \multirow[t]{2}{*}{Pulse Width (Note 3)} & Clock & 20 & & & 17 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Clear & 17 & & & 17 & & & \\
    \hline \multirow[t]{2}{*}{tsu} & \multirow[t]{2}{*}{Setup Time (Note 3)} & Enable & 17 & & & 23 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Data & 15 & & & 15 & & & \\
    \hline \multirow[t]{2}{*}{\({ }_{\text {t }}\)} & \multirow[t]{2}{*}{Hold Time (Note 3)} & Enable & 0 & & & 0 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Data & 5 & & & 0 & & & \\
    \hline \(t_{\text {REL }}\) & \multicolumn{2}{|l|}{Clear Release Time} & 10 & & & 10 & & & ns \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note 1: \(\mathrm{C}_{\mathrm{L}}=45 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=667 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 2: \(C_{L}=150 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=667 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 3: \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 5) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\) Min, \(\mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & 2.4 & & & V \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O L}=\operatorname{Max} \\
    & V_{I L}=M a x, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline 11 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, V_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline lozh & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Max}, V_{\mathrm{O}}=2.7 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline Iozl & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=0.4 \mathrm{~V} \\
    & V_{\mathrm{IH}}=\operatorname{Min}, V_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & -20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
    & \text { (Note 6) }
    \end{aligned}
    \]} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline lCC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}\) ( Note 7)} & & 17 & 30 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{From (Input) To (Output)} & \multicolumn{2}{|c|}{54LS} & \multicolumn{2}{|c|}{DM74LS} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\[
    \begin{gathered}
    C_{L}=150 \mathrm{pF} \\
    R_{L}=667 \Omega
    \end{gathered}
    \]} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 30 & & 20 & & ns \\
    \hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Output & & 28 & & 34 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Output & & 28 & & 40 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clear to Output & & 30 & & 40 & ns \\
    \hline \(t_{\text {PZH }}\) & Output Enable Time to High Level Output & Output Control (M or N) to Any Q & & 23 & & 34 & ns \\
    \hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level Output & Output Control ( M or N ) to Any Q & & 28 & & 45 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time from High Level Output (Note 8) & Output Control ( M or N ) to Any Q & & 17 & & 25 & ns \\
    \hline tplz & Output Disable Time from Low Level Output (Note 8) & Output Control ( M or N ) to Any Q & & 23 & & 25 & ns \\
    \hline
    \end{tabular}

    Note 4: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 6: \(\mathrm{I}_{\mathrm{Cc}}\) is measured with all outputs open: Clear grounded after a momentary \(4.5 \mathrm{~V} ; \mathrm{N}, \mathrm{G} 1, \mathrm{G} 2\) and all data inputs grounded: and the CLOCK and M input at 4.5V.

    Note 7: \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\).
    

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    \section*{54LS174/DM54LS174/DM74LS174, 54LS175/DM54LS175/DM74LS175 \\ Hex/Quad D Flip-Flops with Clear}

    \section*{General Description}

    These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) versions feature complementary outputs from each flip-flop.
    Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

    \section*{Features}

    LS174 contains six flip-flops with single-rail outputs
    - LS175 contains four flip-flops with double-rail outputs
    - Buffered clock and direct clear inputs
    - Individual data input to each flip-flop
    - Applications include:

    Buffer/storage registers
    Shift registers
    Pattern generators
    . Typical clock frequency 40 MHz
    - Typical power dissipation per flip-flop 14 mW
    - Alternate Military/Aerospace device (54LS174, 54LS175) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

    \section*{Connection Diagrams}
    

    Order Number 54LS174DMQB, 54LS174FMQB,
    54LS174LMQB, DM54LS174J,
    DM54LS174W, DM74LS174M or DM74LS174N
    See NS Package Number E20A, J16A, M16A, N16E or W16A

    \section*{Dual-In-Line Package}
    

    Order Number 54LS175DMQB, 54LS175FMQB, 54LS175LMQB, DM54LS175J
    DM54LS175W, DM74LS175M or DM74LS175N See NS Package Number E20A, J16A, M16A, N16E or W16A
    \(\mathrm{H}=\) High Level (steady state)
    L = Low Level (steady state)
    X = Don't Care
    \(\uparrow=\) Transition from low to high level
    \(Q_{0}=\) The level of \(Q\) before the indicated steady-state input conditions were established.
    \(\dagger=\) LS175 only

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    7V
    Operating Free Air Temperature Range
    DM54LS and 54LS
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    Storage Temperature Range

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54LS174} & \multicolumn{3}{|c|}{DM74LS174} & \multirow{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{\text {l }}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 4 & & & 8 & mA \\
    \hline fCLK & \multicolumn{2}{|l|}{Clock Frequency (Note 1)} & 0 & & 30 & 0 & & 30 & MHz \\
    \hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & & 25 & 0 & & 25 & MHz \\
    \hline \multirow[t]{2}{*}{tw} & \multirow[t]{2}{*}{Pulse Width (Note 6)} & Clock & 20 & & & 20 & & & ns \\
    \hline & & Clear & 20 & & & 20 & & & \\
    \hline tsu & \multicolumn{2}{|l|}{Data Setup Time (Note 6)} & 20 & & & 20 & & & ns \\
    \hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Data Hold Time (Note 6)} & 0 & & & 0 & & & ns \\
    \hline \(t_{\text {REL }}\) & \multicolumn{2}{|l|}{Clear Release Time (Note 6)} & 25 & & & 25 & & & ns \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    \section*{'LS174 Electrical Characteristics}
    over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 3) } \\
    \hline
    \end{gathered}
    \] & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{VOH} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[b]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline 1 & Input Current@Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{I}=0.4 V
    \end{aligned}
    \]} & Clock & & & -0.4 & \multirow{3}{*}{mA} \\
    \hline & & & Clear & & & -0.4 & \\
    \hline & & & Data & & & -0.36 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & (\text { Note 4) }
    \end{aligned}
    \]} & DM54 & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 5)} & & 16 & 26 & mA \\
    \hline
    \end{tabular}

    Note 1: \(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 2: \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 3: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 5: With all outputs open and 4.5 V applied to all data and clear inputs, \(\mathrm{I}_{\mathrm{Cc}}\) is measured after a momentary ground, then 4.5 V applied to the clock.
    Note 6: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

    \section*{'LS174 Switching Characteristics}
    at \(V_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|c|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 30 & & 25 & & MHz \\
    \hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Output & & 30 & & 32 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Output & & 30 & & 36 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clear to Output & & 35 & & 42 & ns \\
    \hline
    \end{tabular}

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54LS175} & \multicolumn{3}{|c|}{DM74LS175} & \multirow{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\text {CC }}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.7 & & & 0.8 & V \\
    \hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 1)} & 0 & & 30 & 0 & & 30 & MHz \\
    \hline \({ }_{\text {f CLK }}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & & 25 & 0 & & 25 & MHz \\
    \hline \multirow[t]{2}{*}{tw} & \multirow[t]{2}{*}{Pulse Width (Note 3)} & Clock & 20 & & & 20 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Clear & 20 & & & 20 & & & \\
    \hline tsu & \multicolumn{2}{|l|}{Data Setup Time (Note 3)} & 20 & & & 20 & & & ns \\
    \hline \(t_{H}\) & \multicolumn{2}{|l|}{Data Hold Time (Note 3)} & 0 & & & 0 & & & ns \\
    \hline \(t_{\text {REL }}\) & \multicolumn{2}{|l|}{Clear Release Time (Note 3)} & 25 & & & 25 & & & ns \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note 1: \(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 2: \(C_{L}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{C C}=5 \mathrm{~V}\).
    Note 3: \(T_{A}=25^{\circ} \mathrm{C}\) and \(V_{C C}=5 \mathrm{~V}\).
    'LS175 Electrical Characteristics
    over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\text { Min }
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{lOL}=4 \mathrm{~mA}\), & DM74 & & 0.25 & 0.4 & \\
    \hline 1 & Input Current@Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Max} \\
    & V_{1}=0.4 V
    \end{aligned}
    \]} & Clock & & & -0.4 & \multirow{3}{*}{mA} \\
    \hline & & & Clear & & & -0.4 & \\
    \hline & & & Data & & & -0.36 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Max} \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & DM54 & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline Icc & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 3)} & & 11 & 18 & mA \\
    \hline
    \end{tabular}

    \section*{'LS175 Switching Characteristics}
    at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|r|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 30 & & 25 & & MHz \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Q or \(\bar{Q}\) & & 30 & & 32 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Q or \(\bar{Q}\) & & 30 & & 36 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clear to \(\bar{Q}\) & & 25 & & 29 & ns \\
    \hline tpHL \(^{\text {d }}\) & Propagation Delay Time High to Low Level Output & Clear to Q & & 35 & & 42 & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: With all outputs open and 4.5 V applied to all data and clear inputs, ICC is measured after a momentary ground, then 4.5 V applied to the clock input.

    \section*{Logic Diagrams}

    LS174
    

    TL/F/6404-3
    

    TL/F/6404-4

    National Semiconductor

    \section*{54LS181/DM74LS181 4-Bit Arithmetic Logic Unit}

    \section*{General Description}

    The 'LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations.

    \section*{Features}
    - Provides 16 arithmetic operations: add, subtract, compare, double, plus twelve other arithmetic operations
    - Provides all 16 logic operations of two variables: exclu-sive-OR, compare, AND, NAND, OR, NOR, plus ten other logic operations
    - Full lookahead for high speed arithmetic operation on long words

    \section*{Connection Diagram}
    

    TL/F/9821-1
    Order Number 54LS181DMQB, 54LS181FMQB or DM74LS181N
    See NS Package Number J24A, N24A or W24C
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{c|}{ Description } \\
    \hline\(\overline{\mathrm{A}} 0-\overline{\mathrm{A}} 3\) & Operand Inputs (Active LOW) \\
    \(\overline{\mathrm{B}} 0-\overline{\mathrm{B}} 3\) & Operand Inputs (Active LOW) \\
    \(\mathrm{S} 0-\mathrm{S} 3\) & Function Select Inputs \\
    M & Mode Control Input \\
    \(\mathrm{C}_{n}\) & Carry Input \\
    \(\overline{\mathrm{F}} 0-\overline{\mathrm{F}} 3\) & Function Outputs (Active LOW) \\
    \(\mathrm{A}=\mathrm{B}\) & Comparator Output \\
    \(\overline{\mathrm{G}}\) & Carry Generate Output (Active LOW) \\
    \(\overline{\mathrm{P}}\) & Carry Propagate Output (Active LOW) \\
    \(\mathrm{C}_{\mathrm{n}+4}\) & Carry Output \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|}
    \hline \multicolumn{2}{|l|}{Absolute Maximum Ratings (Note)} \\
    \hline \multicolumn{2}{|l|}{please contact the National Semiconductor Sales Office/Distributors for availability and specifications.} \\
    \hline Supply Voltage & 7 V \\
    \hline Input Voltage & \\
    \hline Operating Free Air Temperature Range & \\
    \hline 54LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    \hline DN & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    \hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note: The "Absolute Maximum Ratings", are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS181} & \multicolumn{3}{|c|}{DM74LS181} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline IOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\text { Max, } \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & 54LS & 2.5 & & \multirow[t]{2}{*}{} & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & & & \\
    \hline \multirow[t]{3}{*}{VOL} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\operatorname{Max}, \\
    & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \(V_{C C}=M a x, V_{1}=10 \mathrm{~V}\) & \begin{tabular}{l}
    \(M\) input \(\bar{A}_{n}, \bar{B}_{n}\) \\
    \(S_{n}\) \\
    \(\mathrm{C}_{\mathrm{n}}\)
    \end{tabular} & & & \[
    \begin{aligned}
    & 0.1 \\
    & 0.3 \\
    & 0.4 \\
    & 0.5
    \end{aligned}
    \] & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \(V_{C C}=M a x, V_{l}=2.7 \mathrm{~V}\) & \begin{tabular}{l}
    \(\bar{A}_{n}, \bar{B}_{n}\) \(\mathrm{S}_{\mathrm{n}}\) \\
    \(\mathrm{C}_{\mathrm{n}}\)
    \end{tabular} & & & \[
    \begin{gathered}
    20 \\
    60 \\
    80 \\
    100
    \end{gathered}
    \] & \(\mu \mathrm{A}\) \\
    \hline ILL & Low Level Input Current & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & \begin{tabular}{l}
    \(\bar{A}_{n}, \bar{B}_{n}\) \(\mathrm{S}_{\mathrm{n}}\) \\
    \(\mathrm{C}_{\mathrm{n}}\)
    \end{tabular} & & & \[
    \begin{aligned}
    & -0.4 \\
    & -1.2 \\
    & -1.6 \\
    & -2.0
    \end{aligned}
    \] & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline \multirow[t]{2}{*}{Icc} & \multirow[t]{2}{*}{Supply Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x, \bar{B}_{n}, C_{n}=G N D \\
    & S_{n}, M, \bar{A}_{n}=4.5 V
    \end{aligned}
    \]} & 54LS & & & 35 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & & & 37 & \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multicolumn{6}{|l|}{\begin{tabular}{l}
    Switching Characteristics \\
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
    \end{tabular}} \\
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{Conditions} & \multicolumn{2}{|r|}{\multirow[t]{2}{*}{\[
    \begin{gathered}
    \text { 54LS/DM74LS } \\
    C_{L}=15 \mathrm{pF} \\
    \hline
    \end{gathered}
    \]}} & \multirow{3}{*}{Units} \\
    \hline & & & & & \\
    \hline & & & Min & Max & \\
    \hline \[
    \begin{aligned}
    & \text { tPLH } \\
    & t_{\text {PHL }} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay
    \[
    C_{n} \text { to } C_{n+4}
    \] & \(\mathrm{M}=\mathrm{GND}\) & & \[
    \begin{aligned}
    & 27 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & t_{\text {PLH }} \\
    & t_{\text {PHL }} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(C_{n}\) to \(\bar{F}\) & \(\mathrm{M}=\mathrm{GND}\) & & \[
    \begin{aligned}
    & 26 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    t_{\text {PLH }}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & Propagation Delay \(\overline{\mathrm{A}}\) or \(\overline{\mathrm{B}}\) to \(\overline{\mathrm{G}}\) (Sum) & \[
    \begin{aligned}
    & \mathrm{M}, \mathrm{~S}_{1}, \mathrm{~S}_{2}=\mathrm{GND} ; \\
    & \mathrm{S}_{1}, \mathrm{~S}_{3}=4.5 \mathrm{~V}
    \end{aligned}
    \] & & \[
    \begin{array}{r}
    29 \\
    23 \\
    \hline
    \end{array}
    \] & ns \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(t_{\text {PHL }}\)
    \end{tabular} & Propagation Delay \(\overline{\mathrm{A}}\) or \(\overline{\mathrm{B}}\) to \(\overline{\mathrm{G}}\) (Diff) & \[
    \begin{aligned}
    & \mathrm{M}, \mathrm{~S}_{0}, \mathrm{~S}_{3}=\mathrm{GND} ; \\
    & \mathrm{S}_{1}, \mathrm{~S}_{2}=4.5 \mathrm{~V}
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 32 \\
    & 26 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\bar{A}\) or \(\bar{B}\) to \(\bar{P}\) (Sum) & \[
    \begin{aligned}
    & M, S_{1}, S_{2}=G N D ; \\
    & S_{0}, S_{3}=4.5 \mathrm{~V}
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 30 \\
    & 30 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\overline{\mathrm{A}}\) or \(\overline{\mathrm{B}}\) to \(\overline{\mathrm{P}}\) (Diff) & \[
    \begin{aligned}
    & \mathrm{M}, \mathrm{~S}_{0}, \mathrm{~S}_{3}=\mathrm{GND} ; \\
    & \mathrm{S}_{1}, \mathrm{~S}_{2}=4.5 \mathrm{~V}
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 30 \\
    & 33 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\bar{A}_{i}\) or \(\bar{B}_{i}\) to \(\bar{F}_{i}\) (Sum) & \[
    \begin{aligned}
    & \mathrm{M}, \mathrm{~S}_{1}, \mathrm{~S}_{2}=\mathrm{GND} ; \\
    & \mathrm{S}_{0}, \mathrm{~S}_{3}=4.5 \mathrm{~V}
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 32 \\
    & 25 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\overline{\mathrm{A}}_{i}\) or \(\overline{\mathrm{B}}_{\mathrm{i}}\) to \(\overline{\mathrm{F}}_{\mathrm{i}}\) (Diff) & \[
    \begin{aligned}
    & \mathrm{M}, \mathrm{~S}_{0}, \mathrm{~S}_{3}=\mathrm{GND} ; \\
    & \mathrm{S}_{1}, \mathrm{~S}_{2}=4.5 \mathrm{~V}
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 32 \\
    & 33 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\bar{A}\) or \(\bar{B}\) to \(\bar{F}\) (Logic) & \(\mathrm{M}=4.5 \mathrm{~V}\) & & \[
    \begin{aligned}
    & 33 \\
    & 29 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\bar{A}\) or \(\bar{B}\) to \(C_{n+4}\) (Sum) & \[
    \begin{aligned}
    & \mathrm{M}, \mathrm{~S}_{1}, \mathrm{~S}_{2}=\mathrm{GND} ; \\
    & \mathrm{S}_{0}, \mathrm{~S}_{3}=4.5 \mathrm{~V}
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 38 \\
    & 38
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \text { tpLH } \\
    & t_{\text {pHL }} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\bar{A}\) or \(\bar{B}\) to \(C_{n+4}\) (Diff) & \[
    \begin{aligned}
    & \mathrm{M}, \mathrm{~S}_{0}, \mathrm{~S}_{3}=\mathrm{GND} ; \\
    & \mathrm{S}_{1}, \mathrm{~S}_{2}=4.5 \mathrm{~V}
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 41 \\
    & 41
    \end{aligned}
    \] & ns \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(t_{\text {PHL }}\)
    \end{tabular} & Propagation Delay \(\bar{A}\) or \(\bar{B}\) to \(A=B\) & \[
    \begin{aligned}
    & M, S_{0}, S_{3}=G N D ; \\
    & S_{1}, S_{2}=4.5 \mathrm{~V} ; \\
    & R_{L}=2 \mathrm{k} \Omega \text { to } 5.0 \mathrm{~V}
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 50 \\
    & 62
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}

    Sum Mode Test Table I Function Inputs \(\mathrm{s} 0=\mathrm{s} 3=4.5 \mathrm{~V}, \mathrm{~s} 1=\mathrm{s} 2=\mathrm{M}=\mathrm{ov}\)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{\begin{tabular}{l}
    Input \\
    Under \\
    Test
    \end{tabular}} & \multicolumn{2}{|c|}{Other Input Same Bit} & \multicolumn{2}{|c|}{Other Data Inputs} & \multirow[t]{2}{*}{\begin{tabular}{l}
    Output \\
    Under \\
    Test
    \end{tabular}} \\
    \hline & & Apply 4.5V & Apply GND & Apply
    \[
    4.5 \mathrm{~V}
    \] & Apply GND & \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & \(\bar{A}_{i}\) & \(\bar{B}_{i}\) & None & Remaining \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}\) & \(C_{n}\) & \(\bar{F}_{i}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & \(\bar{B}_{i}\) & \(\bar{A}_{i}\) & None & Remaining \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}\) & \(\mathrm{C}_{n}\) & \(\bar{F}_{i}\) \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(\mathrm{t}_{\mathrm{PHL}}\)
    \end{tabular} & \(\bar{A}\) & \(\bar{B}\) & None & None & Remaining \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}}\) & \(\overline{\mathrm{P}}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & \(\bar{B}\) & \(\bar{A}\) & None & None & \begin{tabular}{l}
    Remaining \\
    \(\bar{A}\) and \(\bar{B}, C_{n}\)
    \end{tabular} & \(\overline{\mathrm{P}}\) \\
    \hline \[
    t_{\text {PLH }}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & \(\bar{A}\) & None & \(\bar{B}\) & \[
    \begin{gathered}
    \text { Remaining } \\
    \bar{B}
    \end{gathered}
    \] & \[
    \begin{aligned}
    & \text { Remaining } \\
    & \overline{\mathrm{A}}, \mathrm{C}_{\mathrm{n}} \\
    & \hline
    \end{aligned}
    \] & \(\overline{\mathrm{G}}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}}
    \end{aligned}
    \] & \(\bar{B}\) & None & \(\bar{A}\) & \[
    \begin{gathered}
    \text { Remaining } \\
    \bar{B} \\
    \hline
    \end{gathered}
    \] & \[
    \begin{aligned}
    & \text { Remaining } \\
    & \overline{\mathrm{A}}, \mathrm{C}_{\mathrm{n}}
    \end{aligned}
    \] & \(\overline{\mathrm{G}}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & \(\bar{A}\) & None & \(\bar{B}\) & \[
    \begin{gathered}
    \text { Remaining } \\
    \bar{B} \\
    \hline
    \end{gathered}
    \] & \[
    \begin{aligned}
    & \text { Remaining } \\
    & \overline{\mathrm{A}}, \mathrm{C}_{\mathrm{n}}
    \end{aligned}
    \] & \(C_{n+4}\) \\
    \hline \[
    \begin{aligned}
    & t_{\text {PLH }} \\
    & t_{\text {PHL }} \\
    & \hline
    \end{aligned}
    \] & \(\bar{B}\) & None & \(\bar{A}\) & \[
    \begin{gathered}
    \text { Remaining } \\
    \bar{B} \\
    \hline
    \end{gathered}
    \] & \[
    \begin{aligned}
    & \text { Remaining } \\
    & \overline{\mathrm{A}}, \mathrm{C}_{\mathrm{n}}
    \end{aligned}
    \] & \(C_{n+4}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & \(C_{n}\) & None & None & \[
    \begin{aligned}
    & \mathrm{All} \\
    & \overline{\mathrm{~A}}
    \end{aligned}
    \] & \[
    \begin{aligned}
    & \text { All } \\
    & \bar{B}
    \end{aligned}
    \] & \[
    \begin{gathered}
    \text { Any } \bar{F} \\
    \text { or } C_{n+4} \\
    \hline
    \end{gathered}
    \] \\
    \hline
    \end{tabular}

    \section*{Diff Mode Test Table II}

    Function Inputs \(\mathrm{s} 1=\mathrm{s} 2=4.5 \mathrm{~V}, \mathrm{so}=\mathrm{S3}=\mathrm{M}=0 \mathrm{~V}\)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Input Under Test} & \multicolumn{2}{|c|}{Other Input Same Bit} & \multicolumn{2}{|c|}{Other Data Inputs} & \multirow[t]{2}{*}{Output Under Test} \\
    \hline & & \[
    \begin{gathered}
    \text { Apply } \\
    4.5 \mathrm{~V}
    \end{gathered}
    \] & Apply GND & \[
    \begin{aligned}
    & \text { Apply } \\
    & 4.5 \mathrm{~V}
    \end{aligned}
    \] & Apply GND & \\
    \hline \[
    \begin{aligned}
    & t_{\text {PLH }} \\
    & t_{\text {PHLL }} \\
    & \hline
    \end{aligned}
    \] & \(\overline{\text { A }}\) & None & \(\overline{\text { B }}\) & \[
    \begin{gathered}
    \text { Remaining } \\
    \bar{A} \\
    \hline
    \end{gathered}
    \] & \[
    \begin{gathered}
    \text { Remaining } \\
    \overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}} \\
    \hline
    \end{gathered}
    \] & \(\bar{F}_{i}\) \\
    \hline \[
    \begin{aligned}
    & t_{\text {PLH }} \\
    & t_{\text {PHLL }}
    \end{aligned}
    \] & \(\bar{B}\) & \(\overline{\text { A }}\) & None & \[
    \operatorname{Remaining~}_{\bar{A}}
    \] & \[
    \begin{gathered}
    \text { Remaining } \\
    \overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}}
    \end{gathered}
    \] & \(\bar{F}_{i}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHLL}} \\
    & \hline
    \end{aligned}
    \] & \(\overline{\text { A }}\) & None & \(\overline{\text { B }}\) & None & \begin{tabular}{l}
    Remaining \\
    \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}}\)
    \end{tabular} & \(\overline{\text { P }}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLLH}} \\
    & \mathrm{t}_{\mathrm{PHLL}} \\
    & \hline
    \end{aligned}
    \] & \(\bar{B}\) & \(\bar{A}\) & None & None & \begin{tabular}{l}
    Remaining \\
    \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}}\)
    \end{tabular} & \(\overline{\text { F }}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHLL}} \\
    & \hline
    \end{aligned}
    \] & \(\bar{A}\) & \(\overline{\text { B }}\) & None & None & \begin{tabular}{l}
    Remaining \\
    \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}}\)
    \end{tabular} & \(\overline{\mathrm{G}}\) \\
    \hline \[
    \begin{aligned}
    & t_{\text {PLH }} \\
    & t_{\text {PHL }}
    \end{aligned}
    \] & \(\bar{B}\) & None & \(\bar{A}\) & None & \begin{tabular}{l}
    Remaining \\
    \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}}\)
    \end{tabular} & \(\overline{\mathrm{G}}\) \\
    \hline \[
    \begin{aligned}
    & \text { tpLH } \\
    & t_{\text {tPHL }} \\
    & \hline
    \end{aligned}
    \] & \(\bar{A}\) & None & \(\overline{\text { B }}\) & \[
    \begin{gathered}
    \text { Remaining } \\
    \overline{\mathrm{A}} \\
    \hline
    \end{gathered}
    \] & \[
    \begin{gathered}
    \text { Remaining } \\
    \overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}} \\
    \hline
    \end{gathered}
    \] & \(A=B\) \\
    \hline \[
    \begin{aligned}
    & \text { tpLH } \\
    & t_{\text {PHL }} \\
    & \hline
    \end{aligned}
    \] & \(\bar{B}\) & \(\overline{\text { A }}\) & None & \[
    \begin{gathered}
    \text { Remaining } \\
    \overline{\mathrm{A}} \\
    \hline
    \end{gathered}
    \] & \[
    \begin{gathered}
    \text { Remaining } \\
    \overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}} \\
    \hline
    \end{gathered}
    \] & \(A=B\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHLL}} \\
    & \hline
    \end{aligned}
    \] & \(\bar{A}\) & \(\overline{\text { B }}\) & None & None & Remaining \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}}\) & \(c_{n+4}\) \\
    \hline \[
    \begin{aligned}
    & \text { tpLH } \\
    & \text { tpHL } \\
    & \hline
    \end{aligned}
    \] & \(\overline{\text { B }}\) & None & \(\overline{\text { A }}\) & None & \begin{tabular}{l}
    Remaining \\
    \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}}\)
    \end{tabular} & \(\mathrm{C}_{\mathrm{n}+4}\) \\
    \hline \[
    \begin{aligned}
    & \text { tpLH } \\
    & t_{\text {tPHL }} \\
    & \hline
    \end{aligned}
    \] & \(\mathrm{C}_{n}\) & None & None & All \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}\) & None & \(c_{n+4}\) \\
    \hline
    \end{tabular}

    Logic Mode Test Table III Function Inputs \(\mathrm{s} 1=\mathrm{S} 2=\mathrm{M}=4.5 \mathrm{~V}, \mathrm{~s} 0=\mathrm{s} 3=\mathrm{ov}\)

    \section*{Functional Description}

    The 'LS181 is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S0-S3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations
    When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the \(\mathrm{C}_{\mathrm{n}+4}\) output, or for carry lookahead between packages using the signals \(\bar{P}\) (Carry Propagate) and \(\bar{G}\) (Carry Generate). In the ADD mode, \(\bar{P}\) indicates that \(\bar{F}\) is 15 or more, while \(\bar{G}\) indicates that \(\bar{F}\) is 16 or more. In the SUBTRACT mode, \(\bar{P}\) indicates that \(\bar{F}\) is zero or less, while \(\bar{G}\) indicates that \(\bar{F}\) is less than zero. \(\overline{\mathrm{P}}\) and \(\overline{\mathrm{G}}\) are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output ( \(\mathrm{C}_{n+4}\) ) signal to the Carry input \(\left(C_{n}\right)\) of the next unit. For high speed operation the device is used in conjunction with the 9342 or \(93 S 42\) carry lookahead circuit. One carry lookahead pack-
    age is required for each group of four 'LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.
    The \(A=B\) output from the device goes HIGH when all four \(\bar{F}\) outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The \(\mathrm{A}=\mathrm{B}\) output is open-collector and can be wired-AND with other \(\mathrm{A}=\mathrm{B}\) outputs to give a comparison for more than four bits. The \(A=B\) signal can also be used with the \(C_{n+4}\) signal to indicate \(A>B\) and \(A<B\).
    The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus \(B\) minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

    Function Table
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{4}{|c|}{Mode Select Inputs} & \multicolumn{2}{|r|}{Active LOW Operands \& \(\mathrm{F}_{\mathrm{n}}\) Outputs} & \multicolumn{2}{|r|}{Active HIGH Operands \& F \({ }_{n}\) Outputs} \\
    \hline S3 & S2 & S1 & S0 & \[
    \begin{gathered}
    \text { Logic } \\
    (M=H)
    \end{gathered}
    \] & Arithmetic**
    \[
    (M=L)\left(C_{n}=L\right)
    \] & Logic
    \[
    (M=H)
    \] & \[
    \begin{gathered}
    \text { Arithmetic** } \\
    (M=L)\left(C_{n}=H\right)
    \end{gathered}
    \] \\
    \hline L & L & L & L & \(\bar{A}\) & A minus 1 & \(\bar{A}\) & A \\
    \hline L & L & L & H & \(\overline{A B}\) & \(A B\) minus 1 & \(\overline{A+B}\) & \(A+B\) \\
    \hline L & L & H & L & \(\overline{A+B}\) & \(A \bar{B}\) minus 1 & \(\bar{A} B\) & \(A+\bar{B}\) \\
    \hline L & L & H & H & Logic 1 & minus 1 & Logic 0 & minus 1 \\
    \hline L & H & L & L & \(\overline{A+B}\) & A plus ( \(A+\bar{B}\) ) & \(\overline{A B}\) & A plus \(\bar{A} \bar{B}\) \\
    \hline L & H & L & H & \(\bar{B}\) & \(A B\) plus \((A+\bar{B})\) & \(\overline{\text { B }}\) & \((A+B)\) plus \(A \bar{B}\) \\
    \hline L & H & H & L & \(\overline{A \oplus B}\) & \(A\) minus \(B\) minus 1 & \(A \oplus B\) & A minus \(B\) minus 1 \\
    \hline L & H & H & H & \(A+\bar{B}\) & \(A+\bar{B}\) & \(A \bar{B}\) & \(A B\) minus 1 \\
    \hline H & L & L & L & \(\bar{A} B\) & A plus ( \(A+B\) ) & \(\bar{A}+B\) & A plus AB \\
    \hline H & L & L & H & \(A \oplus B\) & A plus B & \(\overline{A \oplus B}\) & A plus B \\
    \hline H & L & H & L & B & \(A \bar{B}\) plus \((A+B)\) & B & \((A+\bar{B})\) plus \(A B\) \\
    \hline H & L & H & H & \(A+B\) & \(A+B\) & AB & \(A B\) minus 1 \\
    \hline H & H & L & L & Logic 0 & A plus \(\mathrm{A}^{*}\) & Logic 1 & A plus \(\mathrm{A}^{*}\) \\
    \hline H & H & L & H & \(A \bar{B}\) & \(A B\) plus \(A\) & \(A+\bar{B}\) & \((A+B)\) plus \(A\) \\
    \hline H & H & H & L & \(A B\) & \(A \bar{B}\) minus \(A\) & \(A+B\) & \((A+\bar{B})\) plus \(A\) \\
    \hline H & H & H & H & A & A & A & A minus 1 \\
    \hline
    \end{tabular}

    \footnotetext{
    *Each bit is shifted to the next move significant position.
    **Arithmetic operations expressed in 2 s complement notation.
    }
    

    Active Low Operands
    

    TL/F/9821-4
    

    \section*{DM54LS190/DM74LS190, DM54LS191/DM74LS191 Synchronous 4-Bit Up/Down Counters with Mode Control}

    \section*{General Description}

    These circuits are synchronous, reversible, up/down counters. The LS191 is a 4-bit binary counter and the LS190 is a BCD counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

    The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/ up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.
    These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as moduloN dividers by simply modifying the count length with the preset inputs.
    The clock, down/up, and load inputs are buffered to lower the drive requirement; which significantly reduces the number of clock drivers, etc., required for long parallel words.

    Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

    \section*{Features}
    - Counts 8-4-2-1 BCD or binary
    - Single down/up count control line
    - Count enable control input
    - Ripple clock output for cascading
    - Asynchronously presettable with load control
    - Parallel outputs
    - Cascadable for n-bit applications
    - Average propagation delay 20 ns
    - Typical clock frequency 25 MHz
    - Typical power dissipation 100 mW

    \section*{Connection Diagram}
    

    TL/F/6405-1
    Order Number DM54LS190J, DM54LS191J, DM54LS190W, DM54LS191W, DM74LS190M, DM74LS191M, DM74LS190N, or DM74LS191N

    See NS Package Number
    J16A, M16A, N16A or W16A
    ```

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range

    ```
    DM54LS
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    Storage Temperature Range
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54LS190, LS191} & \multicolumn{3}{|c|}{DM74LS190, LS191} & \multirow{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.7 & & & 0.8 & V \\
    \hline \({ }^{\mathrm{OH}}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 4 & & & 8 & mA \\
    \hline \({ }^{\text {f CLK }}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 4)} & 0 & & 20 & 0 & & 20 & MHz \\
    \hline \multirow[t]{2}{*}{tw} & \multirow[t]{2}{*}{Pulse Width (Note 4)} & Clock & 25 & & & 25 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Load & 35 & & & 35 & & & \\
    \hline \(\mathrm{t}_{\text {Su }}\) & \multicolumn{2}{|l|}{Data Setup Time (Note 4)} & 20 & & & 20 & & & ns \\
    \hline \(t_{H}\) & \multicolumn{2}{|l|}{Data Hold Time (Note 4)} & 0 & & & 0 & & & ns \\
    \hline ten & \multicolumn{2}{|l|}{Enable Time to Clock (Note 4)} & 30 & & & 30 & & & ns \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    \section*{'LS190 and 'LS191 Electrical Characteristics}
    over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \\
    \hline & & & DM74 & 2.7 & 3.4 & & V \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    V_{C C} & =\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    V_{\mathrm{IL}} & =\mathrm{Max}, \mathrm{~V}_{\mathrm{H}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current @ Max Input Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=7 V
    \end{aligned}
    \]} & Enable & & & 0.3 & \multirow[t]{2}{*}{mA} \\
    \hline & & & Others & & & 0.1 & \\
    \hline \multirow[t]{2}{*}{\({ }_{1 H}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=2.7 V
    \end{aligned}
    \]} & Enable & & & 60 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & Others & & & 20 & \\
    \hline \multirow[t]{2}{*}{ILL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=0.4 V
    \end{aligned}
    \]} & Enable & & & -1.08 & \multirow[t]{2}{*}{mA} \\
    \hline & & & Others & & & -0.4 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & DM54 & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 3)} & & 20 & 35 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: ICC is measured with all inputs grounded and all outputs open.
    Note 4: \(T_{A}=25^{\circ} \mathrm{C}\) and \(V_{C C}=5 \mathrm{~V}\).
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{8}{|l|}{\begin{tabular}{l}
    'LS190 and 'LS191 Switching Characteristics \\
    at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \end{tabular}} \\
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \({ }_{\text {f max }}\) & Maximum Clock Frequency & & 20 & & 20 & & MHz \\
    \hline tplH & Propagation Delay Time Low to High Level Output & Load to Any Q & & 33 & & 43 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Load to Any Q & & 50 & & 59 & ns \\
    \hline tple & Propagation Delay Time Low to High Level Output & Data to Any Q & & 22 & & 26 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to Any Q & & 50 & & 62 & ns \\
    \hline tple & Propagation Delay Time Low to High Level Output & Clock to Ripple Clock & & 20 & & 24 & ns \\
    \hline tpHL & Propagation Delay Time High to Low Level Output & Clock to Ripple Clock & & 24 & & 33 & ns \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & Clock to Any Q & & 24 & & 29 & ns \\
    \hline tpHL & Propagation Delay Time High to Low Level Output & Clock to Any Q & & 36 & & 45 & ns \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & \begin{tabular}{l}
    Clock to \\
    Max/Min
    \end{tabular} & & 42 & & 47 & ns \\
    \hline tphL & Propagation Delay Time High to Low Level Output & Clock to Max/Min & & 52 & & 65 & ns \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & Up/Down to Ripple Clock & & 45 & & 50 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Up/Down to Ripple Clock & & 45 & & 54 & ns \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & Down/Up to Max/Min & & 33 & & 36 & ns \\
    \hline \(\mathrm{t}_{\text {P }}\) & Propagation Delay Time High to Low Level Output & Down/Up to Max/Min & & 33 & & 42 & ns \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & Enable to Ripple Clock & & 33 & & 36 & ns \\
    \hline tpHL & Propagation Delay Time High to Low Level Output & Enable to Ripple Clock & & 33 & & 42 & ns \\
    \hline
    \end{tabular}
    

    Logic Diagrams (Continued)
    

    \section*{Timing Diagrams}

    LS190 Decade Counters Typlcal Load, Count, and Inhlbit Sequences
    

    LS191 Binary Counters
    Typical Load, Count, and Inhibit Sequences
    

    National Semiconductor

    \section*{54LS192/DM74LS192 Up/Down Decade Counter with Separate Up/Down Clocks}

    \section*{General Description}

    The 'LS192 is an up/down BCD decade (8421) counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-toHIGH transitions on the clock inputs.

    \section*{Connection Diagram}
    

    TL/F/10178-1
    Order Number 54LS192DMQB, 54LS192FMQB,
    54LS192LMQB, DM74LS192M or DM74LS192N
    See NS Package Number E20A, J16A, M16A, N16E or W16A
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{c|}{ Description } \\
    \hline \(\mathrm{CP}_{\mathrm{U}}\) & \begin{tabular}{l} 
    Count Up Clock Input \\
    (Active Rising Edge) \\
    Count Down Clock Input \\
    (Active Rising Edge)
    \end{tabular} \\
    \(\mathrm{CP}_{\mathrm{D}}\) & \begin{tabular}{l} 
    Asynchronous Master Reset Input \\
    (Active HIGH) \\
    Asynchronous Parallel Load Input \\
    MR \\
    \(\overline{\mathrm{PL}}\) \\
    \(\mathrm{PO}-\mathrm{PB}\) \\
    \(\mathrm{QO}-\mathrm{Q3}\)
    \end{tabular} \\
    \(\mathrm{TC}_{\mathrm{D}}\) & \begin{tabular}{l} 
    Parallel Data Inputs \\
    Flip-Flop Outputs
    \end{tabular} \\
    \(\overline{\mathrm{TC}}_{\mathrm{U}}\) & \begin{tabular}{l} 
    Terminal Count Down (Borrow) \\
    Output (Active LOW) \\
    Terminal Count Up (Carry) \\
    Output (Active LOW)
    \end{tabular} \\
    \hline
    \end{tabular}

    Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stage without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load (피) and the Master Reset (MR) inputs asynchronously override the clocks.

    \section*{Logic Symbol}
    

    TL/F/10178-2
    \(V_{\mathrm{CC}}=\operatorname{Pin} 16\)
    \(\mathrm{GND}=\operatorname{Pin} 8\)

    Mode Select Table
    \begin{tabular}{|c|c|c|c|c|}
    \hline MR & \(\overline{\text { PL }}\) & \(\mathrm{CP}_{\mathbf{u}}\) & CPD & Mode \\
    \hline H & X & X & X & Reset (Asyn.) \\
    \hline L & L & X & X & Preset (Asyn.) \\
    \hline L & H & H & H & No Change \\
    \hline L & H & \(\checkmark\) & H & Count Up \\
    \hline L & H & H & 5 & Count Down \\
    \hline
    \end{tabular}
    \(H=H I G H\) Voltage Level
    \(\mathrm{L}=\) LOW Voltage Level
    \(X=\) Immaterial

    Absolute Maximum Ratings (Note)
    If Millitary/Aerospace specifled devices are required, please contact the National Semiconductor Sales Office/Distributors for availablity and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    \begin{tabular}{lr} 
    54LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS192} & \multicolumn{3}{|c|}{DM74LS192} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Voltage & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & t_{s}(H) \\
    & t_{s}(L) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW Pn to \(\overline{\mathrm{P}}\) & \[
    \begin{aligned}
    & 20 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 20 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(\mathrm{~L})
    \end{aligned}
    \] & Hold Time HIGH or LOW Pn to \(\overline{\mathrm{P}}\) & \[
    \begin{array}{r}
    3 \\
    3 \\
    \hline
    \end{array}
    \] & & & \[
    \begin{aligned}
    & 3 \\
    & 3 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \(t_{w}(L)\) & CP Pulse Width LOW & 17 & & & 17 & & & ns \\
    \hline \(t_{w}(L)\) & \(\overline{\text { PL Pulse Width LOW }}\) & 20 & & & 20 & & & ns \\
    \hline \(t_{w}(\mathrm{H})\) & MR Pulse Width HIGH & 15 & & & 15 & & & ns \\
    \hline \(\mathrm{t}_{\text {rec }}\) & Recovery Time, MR to CP & 3 & & & 3 & & & ns \\
    \hline \(\mathrm{t}_{\text {rec }}\) & Recovery Time, \(\overline{\text { PL }}\) to CP & 10 & & & 10 & & & ns \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & 54LS & 2.5 & & & V \\
    \hline & & & DM74 & 2.7 & & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\text { Min, } I_{O L}=\text { Max }, \\
    & V_{I H}=\text { Min }
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & & 0.5 & \\
    \hline & & \(\mathrm{lOL}=4 \mathrm{~mA}\) & DM74 & & & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=10 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, V_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \(1 / 2\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline Icc & Supply Current & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{MR}, \overline{\mathrm{PL}}=\mathrm{GND} \\
    & \text { Other Inputs }=4.5 \mathrm{~V}
    \end{aligned}
    \]} & & & 31 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{Switching Characterisitcs}
    \(\mathrm{V}_{\mathrm{CC}}=+0.5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\[
    \begin{gathered}
    R_{\mathrm{L}}=2 \mathrm{k} \\
    \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}
    \end{gathered}
    \]} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \(\mathrm{f}_{\text {max }}\) & Maximum Count Frequency & 30 & & MHz \\
    \hline \(t_{\text {PLH }}\)
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & Propagation Delay \(C P u\) or \(C P_{D}\) to \(Q_{n}\) & & \[
    \begin{aligned}
    & 31 \\
    & 28
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\mathrm{CP}_{\mathrm{U}}\) to \(\overline{T C}_{U}\) & & \[
    \begin{aligned}
    & 16 \\
    & 21
    \end{aligned}
    \] & ns \\
    \hline \[
    t_{\text {PLH }}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & Propagation Delay \(\mathrm{CP}_{\mathrm{D}}\) to \(\overline{\mathrm{TC}}_{\mathrm{D}}\) & & \[
    \begin{aligned}
    & 16 \\
    & 24
    \end{aligned}
    \] & \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay
    \[
    P_{n} \text { to } Q_{n}
    \] & & \[
    \begin{aligned}
    & 20 \\
    & 30 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \begin{tabular}{l}
    tpLH \\
    \({ }^{\text {tpHL }}\)
    \end{tabular} & Propagation Delay \(\overline{\text { PL }}\) to \(Q_{n}\) & & \[
    \begin{aligned}
    & 32 \\
    & 30
    \end{aligned}
    \] & ns \\
    \hline tPHL & Propagation Delay, MR to \(\mathrm{Q}_{\mathrm{n}}\) & & 25 & \\
    \hline
    \end{tabular}

    \section*{Functional Description}

    The '192 is an asynchronously presettable decade and 4-bit binary synchronous up/down (reversible) counter. The operating modes of the '192 decade counter and the '193 binary counter are identical, with the only difference being the count sequences as noted in the State Diagram. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up, and count down operations.

    Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.
    The Terminal Count Up ( \(\overline{T C}_{U}\) ) and Terminal Count Down ( \(\overline{T C}_{D}\) ) outputs are normally HIGH. When a circuit has reached the maximum count state ( 9 for the '192, 15 for the '193), the next HIGH-to-LOW transition of the Count Up Clock will cause \(\overline{T C}_{U}\) to go LOW. \(\overline{T C}_{U}\) will stay LOW until CPu goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the \(\overline{T C}_{D}\) output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the TC outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.
    \[
    \begin{gathered}
    \overline{\mathrm{TC}}_{\mathrm{U}}=\mathrm{Q} 0 \bullet \mathrm{Q} 3 \bullet \overline{\mathrm{CP}} \mathrm{U} \\
    \overline{\mathrm{TC}}_{\mathrm{D}}=\overline{\mathrm{Q}} 0 \bullet \overline{\mathrm{Q}} 1 \bullet \overline{\mathrm{Q}} 2 \bullet \overline{\mathrm{Q} 3} \cdot \overline{\mathrm{CP}}_{\mathrm{D}}
    \end{gathered}
    \]

    Each circuit has an asynchronous parallel load capability permitting the counter to be reset. When the Parallel Load ( \(\overline{\mathrm{PL}}\) ) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs (P0-P3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

    \section*{State Diagram}
    

    TL/F/10178-4

    Logic Diagram

    \section*{54LS193/DM54LS193/DM74LS193 Synchronous 4-Bit Up/Down Binary Counters with Dual Clock}

    \section*{General Description}

    This circuit is a synchronous up/down 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.
    The outputs of the four master-slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is held high.
    The counter is fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is low. The output will change independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.
    A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

    These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up and down counting functions. The borrow output produces a pulse equal in width to the count down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count down and count up inputs respectively of the succeeding counter.

    \section*{Features}
    - Fully independent clear input
    - Synchronous operation
    - Cascading circuitry provided internally
    - Individual preset each flip-flop
    - Alternate Military/Aerospace device (54LS193) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.
    

    TL/F/6406-1
    Order Number 54LS193DMQB, 54LS193FMQB, 54LS193LMQB,
    DM54LS193J, DM54LS193W, DM74LS193M or DM74LS193N
    See NS Package Number E20A, J16A, M16A, N16E or W16A
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{9}{|l|}{Absolute Maximum Ratings (Note)} \\
    \hline \multicolumn{3}{|l|}{If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.} & \multicolumn{6}{|l|}{Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The} \\
    \hline \multicolumn{2}{|l|}{Supply Voltage} & VV & \multicolumn{6}{|l|}{\multirow[t]{2}{*}{parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define}} \\
    \hline \multicolumn{2}{|l|}{Input Voltage} & 7 V & & & & & & \\
    \hline \multicolumn{2}{|l|}{Operating Free Air Temperature Range DM54LS and 54LS} & \(125^{\circ} \mathrm{C}\)
    \(+70^{\circ} \mathrm{C}\) & \multicolumn{6}{|l|}{the conditions for actual device operation.} \\
    \hline \multicolumn{2}{|l|}{Storage Temperature Range \(\quad-65^{\circ} \mathrm{C}\)} & \(150^{\circ} \mathrm{C}\) & & & & & & \\
    \hline \multicolumn{9}{|l|}{Recommended Operating Conditions} \\
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54LS193} & \multicolumn{3}{|c|}{DM74LS193} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \({ }_{\mathrm{OH}}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \multirow[t]{2}{*}{\({ }_{\text {f CLK }}\)} & Clock Frequency (Note 1) & 0 & & 25 & 0 & & 25 & MHz \\
    \hline & Clock Frequency (Note 2) & 0 & & 20 & 0 & & 20 & MHz \\
    \hline tw & Pulse Width of Any Input (Note 6) & 20 & & & 20 & & & ns \\
    \hline tsu & Data Setup Time (Note 6) & 20 & & & 20 & & & ns \\
    \hline \(t_{H}\) & Data Hold Time (Note 6) & 0 & & & 0 & & & ns \\
    \hline \(t_{\text {REL }}\) & Release Time (Note 6) & 40 & & & 40 & & & ns \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    

    Note 1: \(C_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{I}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 2: \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{I}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 3: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 5: Icc is measured with all outputs open, CLEAR and LOAD inputs grounded, and all other inputs at 4.5V.
    Note 6: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 25 & & 20 & & MHz \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Count Up to Carry & & 26 & & 30 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Count Up to Carry & & 24 & & 36 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Count Down to Borrow & & 24 & & 29 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Count Down to Borrow & & 24 & & 32 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Either Count to Any Q & & 38 & & 45 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \text { Either Count } \\
    \text { to Any Q } \\
    \hline
    \end{gathered}
    \] & & 47 & & 54 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Load to Any Q & & 40 & & 41 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Load to Any Q & & 40 & & 47 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clear to
    Any Q & & 35 & & 44 & ns \\
    \hline
    \end{tabular}
    

    \section*{Timing Diagrams}

    Typical Clear, Load, and Count Sequences
    

    TL/F/6406-3
    Note A: Clear overrides load, data, and count inputs.
    Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

    \section*{54LS194A/DM74LS194A 4-Bit Bidirectional Universal Shift Register}

    \section*{General Description}

    This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register; they feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

    Parallel (broadside) load
    Shift right (in the direction \(Q_{A}\) toward \(Q_{D}\) )
    Shift left (in the direction \(Q_{D}\) toward \(Q_{A}\) )
    Inhibit clock (do nothing)
    Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, SO and \(S 1\), high. The data is loaded into the associated flipflops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.
    Shift right is accomplished synchronously with the rising edge of the clock pulse when SO is high and S 1 is low.

    Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.
    Clocking of the flip-flop is inhibited when both mode control inputs are low.

    \section*{Features}
    - Parallel inputs and outputs
    - Four operating modes:

    Synchronous parallel load
    Right shift
    Left shift
    Do nothing
    - Positive edge-triggered clocking
    - Direct overriding clear

    \section*{Connection Diagram}

    Dual-In-Line Package
    OUTPUTS
    

    TL/F/6407-1
    Order Number 54LS194ADMQB, 54LS194AFMQB, 54LS194ALMQB, DM74LS194AM or DM74LS194AN See NS Package Number E20A, J16A, M16A, N16E or W16A

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    54LS
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    DM74LS
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    Storage Temperature Range
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{54LS194A} & \multicolumn{3}{|c|}{DM74LS194A} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\text {CC }}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.7 & & & 0.8 & V \\
    \hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 4 & & & 8 & mA \\
    \hline \({ }^{\text {f CLK }}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 1)} & 30 & & 0 & 0 & & 25 & MHz \\
    \hline & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 22 & & & 0 & & 20 & \\
    \hline \multirow[t]{2}{*}{tw} & \multirow[t]{2}{*}{Pulse Width (Note 3)} & Clock & 17 & & & 20 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Clear & 12 & & & 20 & & & \\
    \hline \multirow[t]{2}{*}{tsu} & \multirow[t]{2}{*}{Setup Time (Note 3)} & Mode & 25 & & & 30 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Data & 16 & & & 20 & & & \\
    \hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Hold Time (Note 3)} & 0 & & & 0 & & & ns \\
    \hline \(t_{\text {REL }}\) & \multicolumn{2}{|l|}{Clear Release Time (Note 3)} & 18 & & & 25 & & & ns \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note 1: \(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 2: \(C_{L}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 3: \(T_{A}=25^{\circ} \mathrm{C}\) and \(V_{C C}=5 \mathrm{~V}\).
    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 4) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{V OH} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & 2.5 & & & V \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{VOL} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \\
    \hline & & & DM74 & & 0.35 & 0.5 & V \\
    \hline & & \multicolumn{2}{|l|}{\(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\)} & & & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 5) }
    \end{aligned}
    \]} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 6)} & & 15 & 23 & mA \\
    \hline
    \end{tabular}

    Note 4: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 6: With all outputs open, inputs A through D grounded, and 4.5 V applied to \(\mathrm{SO}, \mathrm{S} 1, \mathrm{CLEAR}\), and the serial inputs, ICc is tested with momentary ground, then 4.5 V applied to CLOCK.

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{2}{|c|}{54LS} & \multicolumn{2}{|c|}{DM74LS} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & C_{L}=50 \mathrm{pF} \\
    & R_{\mathrm{L}}=2 \mathrm{k} \Omega
    \end{aligned}
    \]} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 30 & & 20 & & MHz \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Any Q & & 21 & & 26 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Any Q & & 24 & & 35 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Output & \begin{tabular}{l}
    Clear to \\
    Any Q
    \end{tabular} & & 26 & & 38 & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: With all outputs open, inputs A through D grounded, and 4.5 V applied to SO, S1, CLEAR, and the serial inputs, Icc is tested with momentary ground, then 4.5 V applied to CLOCK.

    \section*{Logic Diagram}
    

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    \section*{Function Table}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{10}{|c|}{Inputs} & \multicolumn{4}{|c|}{Outputs} \\
    \hline \multirow[t]{2}{*}{Clear} & \multicolumn{2}{|r|}{Mode} & \multirow[t]{2}{*}{Clock} & \multicolumn{2}{|c|}{Serial} & \multicolumn{4}{|c|}{Parallel} & \multirow[b]{2}{*}{\(\mathbf{Q}_{\mathbf{A}}\)} & \multirow[t]{2}{*}{\(\mathbf{Q}_{\mathbf{B}}\)} & \multirow[t]{2}{*}{\(Q_{C}\)} & \multirow[t]{2}{*}{\(Q_{D}\)} \\
    \hline & S1 & SO & & Left & Right & A & B & C & D & & & & \\
    \hline L & X & X & X & X & X & X & X & X & X & L & L & L & L \\
    \hline H & X & X & L & X & \(x\) & X & X & X & X & \(Q_{A 0}\) & \(Q_{B 0}\) & Qco & Q \({ }_{\text {DO }}\) \\
    \hline H & H & H & \(\uparrow\) & X & X & a & b & c & d & a & b & c & d \\
    \hline H & L & H & \(\uparrow\) & X & H & X & X & X & X & H & \(Q_{\text {An }}\) & \(Q_{B n}\) & \(Q_{C n}\) \\
    \hline H & L & H & \(\uparrow\) & X & L & X & X & X & X & L & \(Q_{A n}\) & \(Q_{B n}\) & \(Q_{C n}\) \\
    \hline H & H & L & \(\uparrow\) & H & X & X & X & X & X & \(\mathrm{Q}_{\mathrm{Bn}}\) & \(Q_{C n}\) & \(Q_{D n}\) & H \\
    \hline H & H & L & \(\uparrow\) & L & X & X & X & \(X\) & X & \(\mathrm{Q}_{\mathrm{Bn}}\) & \(Q_{\text {cn }}\) & \(Q_{\text {Dn }}\) & L \\
    \hline H & L & L & X & X & X & X & X & X & X & \(\mathrm{Q}_{\text {AO }}\) & \(\mathrm{Q}_{\mathrm{BO}}\) & \(Q_{\text {co }}\) & \(Q_{\text {DO }}\) \\
    \hline
    \end{tabular}

    \footnotetext{
    \(H=\) High Level (steady state), \(L=\) Low Level (steady state), \(X=\) Don't Care (any input, including transitions)
    \(\uparrow=\) Transition from low to high level
    \(a, b, c, d=\) The level of steady state input at inputs \(A, B, C\) or \(D\), respectively.
    \(Q_{A 0}, Q_{B 0}, Q_{C 0}, Q_{D 0}=\) The level of \(Q_{A}, Q_{B}, Q_{C}\), or \(Q_{D}\), respectively, before the indicated steady state input conditions were established.
    \(Q_{A n}, Q_{B n}, Q_{C n}, Q_{D n}=\) The level of \(Q_{A}, Q_{B}, Q_{C}\), respectively, before the most-recent \(\uparrow\) transition of the clock.
    }

    Timing Diagram
    Typical Clear, Load, Right-Shift, Left-Shift, Inhibit, and Clear Sequences
    

    \section*{54LS195A/DM74LS195A}

    \section*{4-Bit Parallel Access Shift Register}

    \section*{General Description}

    This 4-bit register features parallel inputs, parallel outputs, \(\mathrm{J}-\overline{\mathrm{K}}\) serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:
    Parallel (broadside) load
    Shift (in the direction \(Q_{A}\) toward \(Q_{D}\) )
    Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.
    Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the \(J-\bar{K}\) inputs. These inputs permit the first stage to perform as a \(J-\bar{K}, D\), or T-type flip-flop as shown in the truth table.

    \section*{Features}
    - Synchronous parallel load
    - Positive-edge-triggered clocking
    - Parallel inputs and outputs from each flip-flop
    - Direct overriding clear

    ■ J and \(\overline{\mathrm{K}}\) inputs to first stage
    - Complementary outputs from last stage
    - For use in high-performance: accumulators/processors serial-to-parallel, parallel-to-serial converters
    - Typical clock frequency 39 MHz
    - Typical power dissipation 70 mW

    \section*{Connection Diagram}
    

    Absolute Maximum Ratings (Note)

    If Milltary/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avallability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    \begin{tabular}{lr} 
    54LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    \end{tabular}

    Storage Temperature Range \(\quad-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{54LS195A} & \multicolumn{3}{|c|}{DM74LS195A} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{1 \mathrm{H}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.7 & & & 0.8 & V \\
    \hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 4 & & & 8 & mA \\
    \hline \multirow[t]{2}{*}{\({ }_{\text {f CLK }}\)} & \multicolumn{2}{|l|}{Clock Frequency (Note 1)} & 30 & & 0 & 0 & & 30 & MHz \\
    \hline & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 30 & & 0 & 0 & & 25 & MHz \\
    \hline \multirow[t]{2}{*}{tw} & \multirow[t]{2}{*}{Pulse Width (Note 3)} & Clock & 16 & & & 16 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Clear & 14 & & & 12 & & & \\
    \hline \multirow[t]{2}{*}{tsu} & \multirow[t]{2}{*}{Setup Time (Note 3)} & Shift/Load & 25 & & & 25 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Data & 15 & & & 15 & & & \\
    \hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Hold Time (Note 3)} & 0 & & & 0 & & & \multirow[t]{2}{*}{ns} \\
    \hline \multirow[t]{2}{*}{\(t_{\text {tel }}\)} & \multicolumn{2}{|l|}{Shift/Load Release Time (Note 3)} & 10 & & & 10 & & & \\
    \hline & \multicolumn{2}{|l|}{Clear Release Time (Note 3)} & 25 & & & 25 & & & ns \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note 1: \(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 2: \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 3: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{C C}=5 \mathrm{~V}\).
    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 4) } \\
    \hline
    \end{gathered}
    \] & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\
    & V_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & 2.5 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74LS & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\
    & V_{I L}=\operatorname{Max}, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74LS & & 0.35 & 0.5 & \\
    \hline & & \multicolumn{2}{|l|}{\(\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\)} & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\) Max, \(\mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Max} \\
    & (\text { Note } 5)
    \end{aligned}
    \]} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74LS & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\) Max, (Note 6)} & & 14 & 21 & mA \\
    \hline
    \end{tabular}

    Note 4: All typicals are at \(\mathrm{V}_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 6: With all inputs open, SHIFT/LOAD grounded, and 4.5 V applied to the \(\mathrm{J}, \overline{\mathrm{K}}\), and data inputs, ICc is measured by applying a momentary ground, then 4.5 V to the CLEAR and then applying a momentary ground then 4.5 V to the CLOCK.

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{From (Input) To (Output)} & \multicolumn{2}{|c|}{54LS} & \multicolumn{2}{|c|}{DM74LS} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|r|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \\
    & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}
    \end{aligned}
    \]} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 30 & & 25 & & MHz \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Any Q & & 21 & & 26 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
    Clock to \\
    Any Q
    \end{tabular} & & 24 & & 35 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
    Clear to \\
    Any Q
    \end{tabular} & & 26 & & 38 & ns \\
    \hline
    \end{tabular}

    \section*{Function Table}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{9}{|c|}{Inputs} & \multicolumn{5}{|c|}{Outputs} \\
    \hline \multirow[t]{2}{*}{Clear} & \multirow[t]{2}{*}{\begin{tabular}{l}
    Shift/ \\
    Load
    \end{tabular}} & \multirow[t]{2}{*}{Clock} & \multicolumn{2}{|c|}{Serial} & \multicolumn{4}{|c|}{Parallel} & \multirow[t]{2}{*}{\(Q_{\text {A }}\)} & \multirow[t]{2}{*}{\(Q_{B}\)} & \multirow[t]{2}{*}{\(\mathrm{Q}_{\mathrm{C}}\)} & \multirow[t]{2}{*}{\(Q_{\text {d }}\)} & \multirow[t]{2}{*}{\(\overline{\mathbf{Q}}_{\mathrm{D}}\)} \\
    \hline & & & \(J\) & \(\overline{\mathbf{K}}\) & A & B & c & D & & & & & \\
    \hline L & X & X & X & X & X & X & X & X & L & L & L & L & H \\
    \hline H & L & \(\uparrow\) & X & X & a & b & c & d & a & b & c & d & ¢ \\
    \hline H & H & L & X & X & x & x & x & x & \(\mathrm{Q}_{\text {A0 }}\) & \(\mathrm{Q}_{\text {B0 }}\) & Q \({ }_{\text {co }}\) & \(Q_{\text {D }}\) & \(\overline{\mathrm{Q}}_{\mathrm{D} 0}\) \\
    \hline H & H & \(\uparrow\) & L & H & X & X & X & x & \(\mathrm{Q}_{\text {A0 }}\) & \(\mathrm{Q}_{\text {A }}\) & \(Q_{B n}\) & \(Q_{\text {cn }}\) & \(\overline{\mathrm{Q}}_{\mathrm{C}}\) \\
    \hline H & H & \(\uparrow\) & L & L & X & X & X & X & L & \(\mathrm{Q}_{\text {An }}\) & \(\mathrm{Q}_{\mathrm{Bn}}\) & \(\mathrm{Q}_{\mathrm{C}}\) & \(\overline{\mathrm{Q}}_{\mathrm{C}}\) \\
    \hline H & H & \(\uparrow\) & H & H & x & x & x & \(\times\) & H & \(Q_{\text {An }}\) & \(Q_{\text {Bn }}\) & \(Q_{\text {c }}\) & \(\overline{\mathrm{Q}}_{\mathrm{Cn}}\) \\
    \hline H & H & \(\uparrow\) & H & L & X & X & X & x & \(\bar{Q}_{\text {An }}\) & \(\mathrm{Q}_{\text {An }}\) & \(\mathrm{Q}_{\mathrm{Bn}}\) & \(\mathrm{Q}_{\mathrm{C}}\) & \(\bar{Q}_{\text {cn }}\) \\
    \hline
    \end{tabular}
    \(H=\) High Level (steady state), \(L=\) Low Level (steady state), \(X=\) Don't Care (any input, including transitions)
    \(\uparrow=\) Transition from low to high level
    \(a, b, c, d=\) The level of steady state input at \(A, B, C\), or \(D\), respectively.
    \(Q_{A O}, Q_{B 0}, Q_{C 0}, Q_{D O}=\) The level of \(Q_{A}, Q_{B}, Q_{C}\), or \(Q_{D}\), respectively, before the indicated steady state input conditions were established.
    \(Q_{A n}, Q_{B n}, Q_{C n}=\) The level of \(Q_{A}, Q_{B}, Q_{C}\), respectively, before the most recent transition of the clock.

    \section*{Logic Diagram}
    

    Timing Diagram
    

    \section*{DM74LS196}

    Presettable Decade Counter

    \section*{General Description}

    The 'LS196 decade ripple counter is partitioned into divide-by-two and divide-by-five sections which can be combined to count either in BCD (8421) sequence or in a bi-quinary mode producing a \(50 \%\) duty cycle output. Both circuit types have a Master Reset ( \(\overline{\mathrm{MR}}\) ) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input ( \(\overline{\mathrm{PL}}\) ) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (Pn) into the flip-flops. This preset feature makes the circuits usable as programmable counters. The circuits can also be used as 4-bit latches, loading data from the Parallel Data inputs when \(\overline{\mathrm{PL}}\) is LOW and storing the data when \(\overline{\mathrm{PL}}\) is HIGH. In the counting modes, state changes are initiated by the falling edge of the clock.

    \section*{Features}
    - High counting rates-typically 60 MHz
    - Choice of counting modes-BCD, bi-quinary, binary
    - Asynchronous preset and master reset

    \section*{Connection Diagram}
    

    TL/F/10179-1
    Order Number DM74LS196M or DM74LS196N See NS Package Number M14A or N14A

    \section*{Logic Symbol}
    

    TL/F/10179-2
    \(V_{C C}=\operatorname{Pin} 14\)
    GND \(=\operatorname{Pin} 7\)
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{c|}{ Description } \\
    \hline\(\overline{\mathrm{CP}} \mathbf{1}\) & \begin{tabular}{l}
    \(\div 2\) Section Clock Input \\
    (Active Falling Edge) \\
    \(\div 5\) Section Clock Input \\
    (Active Falling Edge)
    \end{tabular} \\
    \(\overline{\mathrm{CP} 1}\) & \begin{tabular}{l} 
    Asynchronous Master Reset Input \\
    (Active LOW)
    \end{tabular} \\
    \(\overline{\mathrm{MR}}\) & \begin{tabular}{l} 
    Parallel Data Inputs \\
    Asynchronous Parallel Load Input \\
    (Active LOW)
    \end{tabular} \\
    \(\overline{\mathrm{PL}} \mathrm{PB}\) & Flip-Flop Outputs \\
    \(\mathrm{QO}-\mathrm{Q3}\) & \\
    \hline
    \end{tabular}

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage 7V
    Operating Free Air Temperature Range DM74LS
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    Storage Temperature Range

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM74LS196} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(V_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -0.4 & mA \\
    \hline \(\mathrm{lOL}^{\text {l }}\) & Low Level Output Current & & & 8 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & t_{s}(H) \\
    & t_{s}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW Pn to \(\overline{\mathrm{PL}}\) & \[
    \begin{gathered}
    8 \\
    12
    \end{gathered}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L)
    \end{aligned}
    \] & Hold Time HIGH or LOW Pn to \(\overline{P L}\) & \[
    \begin{aligned}
    & 0 \\
    & 6 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \(t_{w}(H)\) & \(\overline{\text { CPO Pulse Width HIGH }}\) & 12 & & & ns \\
    \hline \(t_{w}(H)\) & \(\overline{\text { CP1 Pulse Width HIGH }}\) & 24 & & & ns \\
    \hline \(t_{w}(\mathrm{~L})\) & PL Pulse Width LOW & 18 & & & ns \\
    \hline \(t_{w}(L)\) & \(\overline{M R}\) Pulse Width LOW & 12 & & & ns \\
    \hline \(t_{\text {rec }}\) & Recovery Time \(\overline{\text { PL }}\) to \(\overline{\mathrm{CP}}\) n & 16 & & & ns \\
    \hline \(t_{\text {rec }}\) & Recovery Time \(\overline{\mathrm{MR}}\) to \(\overline{\mathrm{CP}} \mathrm{n}\) & 18 & & & ns \\
    \hline
    \end{tabular}

    Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) } \\
    \hline
    \end{gathered}
    \] & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\) & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{OH}}=\mathrm{Max}, \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}\) & 2.7 & 3.4 & & V \\
    \hline \multirow[t]{2}{*}{V OL} & \multirow[t]{2}{*}{Low Level Output Voltage} & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\mathrm{Max}, \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}\) & & 0.35 & 0.5 & \multirow[t]{2}{*}{V} \\
    \hline & & \(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & & 0.25 & 0.4 & \\
    \hline 11 & Input Current @ Max Input Voltage & \(V_{C C}=M a x, V_{1}=10 \mathrm{~V}\) & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}, \overline{\mathrm{CP}} 1\) & & & 40 & \(\mu \mathrm{A}\) \\
    \hline 1 l & Low Level Input Current & \(\mathrm{V}_{C C}=\) Max, \(\mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -0.4 & mA \\
    \hline los & Short Circuit Output Current & \(V_{C C}=\operatorname{Max}\) (Note 2) & -20 & & -100 & mA \\
    \hline ICC & Supply Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\text {IN }}=\mathrm{GND}\) & & & 20 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, T_{A}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    Switching Characteristics
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\[
    \begin{gathered}
    R_{L}=2 k \\
    C_{L}=15 \mathrm{pF} \\
    \hline
    \end{gathered}
    \]} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \(f_{\text {max }}\) & Maximum Count Frequency at \(\overline{\mathrm{CP}}\) & 45 & & MHz \\
    \hline \(f_{\text {max }}\) & Maximum Count Frequency at \(\overline{\mathrm{CP}} 1\) & 22.5 & & MHz \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(t_{\text {PHL }}\)
    \end{tabular} & Propagation Delay \(\overline{\mathrm{CP}} 0\) to QO & & \[
    \begin{aligned}
    & 15 \\
    & 15 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & t_{\text {PLH }} \\
    & t_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\overline{\mathrm{CP}} 1\) to Q1 & & \[
    \begin{aligned}
    & 15 \\
    & 15 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(t_{\text {PHL }}\)
    \end{tabular} & Propagation Delay \(\overline{\mathrm{CP}} 1\) to Q2 & & \[
    \begin{aligned}
    & 34 \\
    & 34 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(\mathrm{t}_{\mathrm{PHL}}\)
    \end{tabular} & Propagation Delay CP1 to Q3 & & \[
    \begin{aligned}
    & 15 \\
    & 21
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay Pn to Qn & & \[
    \begin{aligned}
    & 25 \\
    & 35 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay PL to Qn & & \[
    \begin{aligned}
    & 31 \\
    & 37 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \(\mathrm{t}_{\mathrm{PHL}}\) & Propagation Delay \(\overline{\text { MR }}\) to Qn & & 42 & ns \\
    \hline
    \end{tabular}

    \section*{Functional Description}

    The '196 and '197 are asynchronous presettable decade and binary ripple counters. The '196 decade counter is partitioned into divide-by-two and divide-by-five sections while the '197 is partitioned into divide-by-two and divide-by-eight sections, with all sections having a separate Clock input. In the counting modes, state changes are initiated by the HIGH-to-LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously because of the internal ripple delays. When using external logic to decode the Q outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The \(\overline{\mathrm{CP}} 0\) input serves the Q0 flip-flop in both circuit types while the \(\overline{\mathrm{CP}} 1\) input serves the divide-by-five or divide-by-eight section. The Q0 output is designed and specified to drive the rated fan-out plus the \(\overline{\mathrm{CP}} 1\) input. With the input frequency connected to \(\overline{\mathrm{CP}} 0\) and with Q 0 driving \(\overline{\mathrm{CP}} 1\), the '197 forms a straight forward modulo-16 counter, with Q0 the least significant output and Q3 the most significant output.

    The '196 decade counter can be connected up to operate in two different count sequences. With the input frequency connected to \(\overline{\mathrm{CP}} 0\) and with Q 0 driving \(\overline{\mathrm{CP}} 1\), the circuit counts in the BCD (8421) sequence. With the input frequency connected to \(\overline{\mathrm{CP}} 1\) and Q 3 driving \(\overline{\mathrm{CP}} 0, \mathrm{Q} 0\) becomes the low frequency output and has a \(50 \%\) duty cycle waveform. Note that the maximum counting rate is reduced in the latter (bi-quinary) configuration because of the interstage gating delay within the divide-by-five section.
    The '196 and '197 have an asynchronous active LOW Master Reset input ( \(\overline{\mathrm{MR}}\) ) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input ( \(\overline{\mathrm{PL}}\) ) overrides the clock inputs and loads the data from Parallel Data (PO-P3) inputs into the flip-flops. While PL is LOW, the counters act as transparent latches and any change in the Pn inputs will be reflected in the outputs. In order for the intended parallel data to be entered and stored, the recommended setup and hold times with respect to the rising edge of \(\overline{P L}\) should be observed.
    

    TL/F/10179-4
    

    TL/F/10179-5

    Mode Select Table
    \begin{tabular}{|c|c|c|l|}
    \hline \multicolumn{3}{|c|}{ Inputs } & \multirow{2}{*}{ Response } \\
    \cline { 1 - 2 }\(\overline{\mathbf{M R}}\) & \(\overline{\mathbf{P L}}\) & \(\overline{\mathbf{C P}}\) & \\
    \hline \(\mathbf{L}\) & \(X\) & \(X\) & Qn forced LOW \\
    \(H\) & L & X & Pn \(\rightarrow\) Qn \\
    \(H\) & \(H\) & & Count Up \\
    \hline
    \end{tabular}

    H = HIGH Voltage Level
    L = LOW Voltage Level
    X = Immaterial

    \section*{DM74LS197 Presettable Binary Counters}

    \section*{General Description}

    The 'LS197 ripple counter contains divide-by-two and di-vide-by-eight sections which can be combined to form a modulo-16 binary counter. State changes are initiated by the falling edge of the clock. The 'LS197 has a Master Reset ( \(\overline{\mathrm{MR}}\) ) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input ( \(\overline{\mathrm{PL}})\) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs ( \(\mathrm{P}_{\mathrm{n}}\) ) into the flipflops. This preset feature makes the circuit usable as a programmable counter. The circuit can also be used as a 4-bit
    latch, loading data from the Parallel Data inputs when \(\overline{\mathrm{PL}}\) is LOW and storing the data when \(\overline{\mathrm{PL}}\) is HIGH. For detail specifications and functional description, please refer to the 'LS196 data sheet.

    \section*{Features}
    - High counting rates-Typically 70 MHz
    - Asynchronous preset
    - Asynchronous master reset

    \section*{Connection Diagram}

    \section*{Dual-In-Line Package}
    

    TL/F/10180-1
    Order Number DM74LS197M or DM74LS197N
    See NS Package Number M14A or N14A
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{c|}{ Description } \\
    \hline\(\overline{\mathrm{CP}} 0\) & \begin{tabular}{l}
    \(\div 2\) Section Clock Input \\
    (Active Falling Edge) \\
    \(\div 8\) Section Clock Input \\
    (Active Falling Edge)
    \end{tabular} \\
    \(\overline{\mathrm{CP} 1}\) & \begin{tabular}{l} 
    Asynchronous Master Reset Input \\
    \\
    (Active LOW)
    \end{tabular} \\
    \(\overline{\mathrm{MR}}\) & Parallel Data Inputs \\
    \(\mathrm{P0}-\mathrm{P} 3\) & Asynchronous Parallel Load Input \\
    \(\overline{\mathrm{PL}}\) & (Active LOW) \\
    QO & \(\div 2\) Section Output* \\
    \(\mathrm{Q} 1-\mathrm{Q} 3\) & \(\div 8\) Section Outputs \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|l|}
    \hline \multicolumn{3}{|c|}{ Inputs } & \multirow{2}{*}{ Response } \\
    \cline { 1 - 2 }\(\overline{\mathbf{M R}}\) & \(\overline{\mathbf{P L}}\) & \(\overline{\mathbf{C P}}\) & \\
    \hline L & X & X & Qn Forced LOW \\
    \(H\) & L & X & Pn \(\rightarrow\) Qn \\
    \(H\) & \(H\) & Z & Count Up \\
    \hline
    \end{tabular}
    \(H=H I G H\) Voltage Level
    L = LOW Voltage Level
    \(X=\) Immaterial
    *Q0 output is guaranteed to drive the full rated fan-out plus the \(\overline{\mathrm{CP}} 1\) input.
    \begin{tabular}{|c|c|}
    \hline \multicolumn{2}{|l|}{Absolute Maximum Ratings (Note)} \\
    \hline If Military/Aerospace specified dev please contact the National Sem Office/Distributors for availability and & ices are required, iconductor Sales d specifications. \\
    \hline Supply Voltage & 7 V \\
    \hline Input Voltage & 7V \\
    \hline Operating Free Air Temperature Range DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    \hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    Recommended Operating Conditions
    \begin{tabular}{l|l|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multirow{2}{|c|}{ Parameter } & \multicolumn{3}{c|}{ 74LS197 } & \multirow{2}{*}{ Units } \\
    \cline { 3 - 4 } & & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Voltage & & & -0.4 & mA \\
    \hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 8 & mA \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \(V_{C C}=\) Min, \(l_{l}=-18 \mathrm{~mA}\) & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \] & 2.7 & 3.4 & & V \\
    \hline \multirow[t]{2}{*}{VOL} & \multirow[t]{2}{*}{Low Level Output Voltage} & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \] & & 0.35 & 0.5 & \multirow[t]{2}{*}{V} \\
    \hline & & \(\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=10 \mathrm{~V}\) & & & 0.1 & mA \\
    \hline 1 H & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\) & & & 20 & \(\mu \mathrm{A}\) \\
    \hline I/L & Low Level Input Current & \(V_{C C}=\) Max, \(V_{1}=0.4 \mathrm{~V}\) & & & -0.4 & mA \\
    \hline los & Short Circuit Output Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 2) & -20 & & -100 & mA \\
    \hline Icc & Supply Current & \(V_{C C}=\operatorname{Max}\) & & & 27 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multicolumn{5}{|l|}{\begin{tabular}{l}
    Switching Characteristics \\
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Loads)
    \end{tabular}} \\
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\[
    \begin{aligned}
    & \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \\
    & \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}
    \end{aligned}
    \]} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Max CLK Frequency & 55 & & MHz \\
    \hline \({ }^{\text {tpLH }}\) \(t_{\text {PHL }}\) & Propagation Delay \(\overline{\mathrm{CPO}}\) to QO & & \[
    \begin{aligned}
    & 15 \\
    & 15
    \end{aligned}
    \] & ns \\
    \hline \begin{tabular}{l}
    \(t_{\text {pLH }}\) \\
    \(t_{\text {PHL }}\)
    \end{tabular} & Propagation Delay \(\overline{\mathrm{CP}} 1\) to Q2 & & \[
    \begin{aligned}
    & 34 \\
    & 34
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay P2 to Q2 & & \[
    \begin{aligned}
    & 27 \\
    & 44 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}}
    \end{aligned}
    \] & Propagation Delay PL to Q2 & & \[
    \begin{aligned}
    & 39 \\
    & 45
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathbf{t}_{\mathrm{PLH}} \\
    & \mathbf{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\overline{\mathrm{CP}} 1\) to Q1 & & \[
    \begin{aligned}
    & 15 \\
    & 17 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \begin{tabular}{l}
    \(t_{\text {pLH }}\) \\
    \(t_{\text {PHL }}\)
    \end{tabular} & Propagation Delay \(\overline{\mathrm{CP}} 1\) to Q3 & & \[
    \begin{aligned}
    & 55 \\
    & 63 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay \(\overline{\text { MR }}\) to Q3 & & 42 & ns \\
    \hline \multicolumn{5}{|l|}{Logic Diagram} \\
    \hline
    \end{tabular}
    
    \(\mathrm{V}_{\mathrm{CC}}=\operatorname{Pin} 14\)
    GND \(=\operatorname{Pin} 7\)

    16 State Diagram
    

    \section*{DM74LS221 Dual Non-Retriggerable One-Shot with Clear and Complementary Outputs}

    \section*{General Description}

    The DM74LS221 is a dual monostable multivibrator with Schmitt-trigger input. Each device has three inputs permitting the choice of either leading-edge or trailing-edge triggering. Pin (A) is an active-low trigger transition input and pin \((B)\) is an active-high transition Schmitt-trigger input that allows jitter free triggering for inputs with transition rates as slow as 1 volt/second. This provides the input with excellent noise immunity. Additionally an internal latching circuit at the input stage also provides a high immunity to \(\mathrm{V}_{\mathrm{CC}}\) noise. The clear (CLR) input can terminate the output pulse at a predetermined time independent of the timing components. This (CLR) input also serves as a trigger input when it is pulsed with a low level pulse transition (ㄴ). To obtain the best and trouble free operation from this device please read operating rules as well as the NSC one-shot application notes carefully and observe recommendations.

    \section*{Features}
    - A dual, highly stable one-shot
    - Compensated for \(V_{C C}\) and temperature variations

    \section*{Connection Diagram}
    

    Order Number DM74LS221M or DM74LS221N See NS Package Number M16A or N16A
    - Pin-out identical to 'LS123 (Note 1)
    - Output pulse width range from 30 ns to 70 seconds
    - Hysteresis provided at (B) input for added noise immunity
    - Direct reset terminates output pulse
    - Triggerable from CLEAR input
    - DTL, TTL compatible
    - Input clamp diodes

    Note 1: The pin-out is identical to 'LS123 but, functionally it is not; refer to Operating Rules \#10 in this datasheet.

    \section*{Functional Description}

    The basic output pulse width is determined by selection of an external resistor ( \(\mathrm{R}_{\mathrm{X}}\) ) and capacitor ( \(\mathrm{C}_{\mathrm{X}}\) ). Once triggered, the basic pulse width is independent of further input transitions and is a function of the timing components, or it may be reduced or terminated by use of the active low CLEAR input. Stable output pulse width ranging from 30 ns to 70 seconds is readily obtainable.

    \section*{Function Table}
    \begin{tabular}{|c|c|c|cc|}
    \hline \multicolumn{3}{|c|}{ Inputs } & \multicolumn{3}{c|}{ Outputs } \\
    \hline CLEAR & A & B & Q & \(\overline{\mathbf{Q}}\) \\
    \hline L & X & X & L & \(H\) \\
    X & \(H\) & \(X\) & \(L\) & \(H\) \\
    X & X & L & L & \(H\) \\
    H & L & \(\uparrow\) & \(\Omega\) & \(U\) \\
    \(H\) & \(\downarrow\) & \(H\) & \(\Omega\) & \(工\) \\
    \(* \uparrow\) & \(L\) & \(H\) & \(\Omega\) & \(U\) \\
    \hline
    \end{tabular}
    \(H=\) High Logic Level
    L = Low Logic Level
    X = Can Be Either Low or High
    \(\uparrow=\) Positive Going Transition
    \(\uparrow=\) Negative Going Transition
    \(\Omega=\) A Positive Pulse
    \(\tau=A\) Negative Pulse
    *This mode of triggering requires first the \(B\) input be set from a low to high level while the CLEAR input is maintained at logic low level. Then with the B input at logic high level, the CLEAR input whose positive transition from low to high will trigger an output pulse.
    

    \footnotetext{
    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    \(\begin{array}{lr}\text { Supply Voltage } & 7 \mathrm{~V} \\ \text { Input Voltage } & 7 \mathrm{~V} \\ \text { Operating Free Air Temperature Range } & \\ \text { DM74LS } & 0^{\circ} \mathrm{C} \text { to }+70^{\circ} \mathrm{C} \\ \text { Storage Temperature Range } & -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C}\end{array}\)
    }

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM74LS221} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\text {CC }}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{T}+}\) & \multicolumn{2}{|l|}{Positive-Going Input Threshold Voltage at the A Input ( \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}\) )} & & 1 & 2 & V \\
    \hline \(\mathrm{V}_{\mathrm{T}-}\) & \multicolumn{2}{|l|}{Negative-Going Input Threshold Voltage at the A Input ( \(V_{\mathrm{CC}}=\mathrm{Min}\) )} & 0.8 & 1 & & V \\
    \hline \(\mathrm{V}_{\mathrm{T}+}\) & \multicolumn{2}{|l|}{Positive-Going Input Threshold Voltage at the B Input ( \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}\) )} & & 1 & 2 & V \\
    \hline \(\mathrm{V}_{\mathrm{T}-}\) & \multicolumn{2}{|l|}{Negative-Going Input Threshold Voltage at the B Input ( \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}\) )} & 0.8 & 0.9 & & V \\
    \hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & mA \\
    \hline OL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 8 & mA \\
    \hline \multirow[t]{2}{*}{tw} & \multirow[t]{2}{*}{Pulse Width (Note 1)} & Data & 40 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Clear & 40 & & & \\
    \hline \(t_{\text {REL }}\) & \multicolumn{2}{|l|}{Clear Release Time (Note 1)} & 15 & & & ns \\
    \hline \[
    \frac{\mathrm{dV}}{\mathrm{dt}}
    \] & \multicolumn{2}{|l|}{Rate of Rise or Fall of Schmitt Input (B) (Note 1)} & & & 1 & \(\frac{\mathrm{V}}{\mathrm{s}}\) \\
    \hline \(\frac{d V}{d t}\) & \multicolumn{2}{|l|}{Rate of Rise or Fall of Logic Input (A) (Note 1)} & & & 1 & \(\frac{\mathrm{V}}{\mu \mathrm{s}}\) \\
    \hline \(\mathrm{R}_{\text {EXT }}\) & \multicolumn{2}{|l|}{External Timing Resistor (Note 1)} & 1.4 & & 100 & \(\mathrm{k} \Omega\) \\
    \hline \(\mathrm{C}_{\text {EXT }}\) & \multicolumn{2}{|l|}{External Timing Capacitance (Note 1)} & 0 & & 1000 & \(\mu \mathrm{F}\) \\
    \hline \multirow[t]{2}{*}{DC} & \multirow[t]{2}{*}{Duty Cycle (Note 1)} & \(\mathrm{R}_{\mathrm{T}}=2 \mathrm{k} \Omega\) & & & 50 & \multirow[t]{2}{*}{\%} \\
    \hline & & \(\mathrm{R}_{\mathrm{T}}=\mathrm{R}_{\text {EXT }}\) (Max) & & & 60 & \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note 1: \(T_{A}=25^{\circ} \mathrm{C}\) and \(V_{C C}=5 \mathrm{~V}\).
    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\text {CC }}=\mathrm{Min}, \mathrm{l}_{\mathrm{l}}=-18 \mathrm{~mA}\) & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\text {OH }}\) & High Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \\
    & \hline
    \end{aligned}
    \] & 2.7 & 3.4 & & v \\
    \hline \multirow[t]{2}{*}{VoL} & \multirow[t]{2}{*}{Low Level Output Voltage} & \[
    \begin{aligned}
    & V_{\mathrm{CC}}=\text { Min, } \mathrm{IOL}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \] & & 0.35 & 0.5 & \multirow[t]{2}{*}{V} \\
    \hline & & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{loL}=4 \mathrm{~mA}\) & & & 0.4 & \\
    \hline 1 & Input Current © Max Input Voltage & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}\) & & & 0.1 & mA \\
    \hline
    \end{tabular}

    \section*{Electrical Characteristics}
    over recommended operating free air temperature range (unless otherwise noted) (Continued)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \({ }_{1 / \mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\) Max, \(V_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=0.4 V
    \end{aligned}
    \]} & A1, A2 & & & -0.4 & \multirow{3}{*}{mA} \\
    \hline & & & B & & & -0.8 & \\
    \hline & & & Clear & & & -0.8 & \\
    \hline los & Short Circuit Output Current & \[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \] & & -20 & & -100 & mA \\
    \hline \multirow[t]{2}{*}{ICC} & \multirow[t]{2}{*}{Supply Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{\text {CC }}=\) Max} & Quiescent & & 4.7 & 11 & \multirow[t]{2}{*}{mA} \\
    \hline & & & Triggered & & 19 & 27 & \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Switching Characteristics at \(\mathrm{V}_{C C}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & From (Input) To (Output) & Conditions & Min & Max & Units \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & A1, A2 to \(Q\) & \multirow[t]{6}{*}{\[
    \begin{gathered}
    \mathrm{C}_{E X T}=80 \mathrm{pF} \\
    \mathrm{R}_{\mathrm{EXT}}=2 \mathrm{k} \Omega \\
    \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\
    \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega
    \end{gathered}
    \]} & & 70 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    B \\
    \text { to } Q
    \end{gathered}
    \] & & & 55 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \mathrm{A} 1, \mathrm{~A} 2 \\
    \text { to } \mathrm{Q}
    \end{gathered}
    \] & & & 80 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \mathrm{B} \\
    \text { to } \overline{\mathrm{Q}}
    \end{gathered}
    \] & & & 65 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clear to \(\bar{Q}\) & & & 65 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{aligned}
    & \text { Clear } \\
    & \text { to } Q
    \end{aligned}
    \] & & & 55 & ns \\
    \hline tw(out) & \begin{tabular}{l}
    Output Pulse \\
    Width Using Zero \\
    Timing Capacitance
    \end{tabular} & \[
    \begin{aligned}
    & A 1, A 2 \\
    & \text { to } Q, \bar{Q}
    \end{aligned}
    \] & \[
    \begin{gathered}
    C_{E X T}=0 \\
    R_{E X T}=2 \mathrm{k} \Omega \\
    R_{\mathrm{L}}=2 \mathrm{k} \Omega \\
    \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\
    \hline
    \end{gathered}
    \] & 20 & 70 & ns \\
    \hline \multirow[t]{3}{*}{tw(out)} & \multirow[t]{3}{*}{\begin{tabular}{l}
    Output Pulse \\
    Width Using External \\
    Timing Resistor
    \end{tabular}} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & A 1, A 2 \\
    & \text { to } Q, \bar{Q}
    \end{aligned}
    \]} & \[
    \begin{gathered}
    \mathrm{C}_{\mathrm{EXT}}=100 \mathrm{pF} \\
    \mathrm{R}_{\mathrm{EXT}}=10 \mathrm{k} \Omega \\
    \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \\
    \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\
    \hline
    \end{gathered}
    \] & 600 & 750 & ns \\
    \hline & & & \[
    \begin{gathered}
    \mathrm{C}_{\mathrm{EXT}}=1 \mu \mathrm{~F} \\
    \mathrm{R}_{\mathrm{EXT}}=10 \mathrm{k} \Omega \\
    \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \\
    \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\
    \hline
    \end{gathered}
    \] & 6 & 7.5 & ms \\
    \hline & & & \[
    \begin{gathered}
    \mathrm{C}_{\mathrm{EXT}}=80 \mathrm{pF} \\
    \mathrm{R}_{\mathrm{EXT}}=2 \mathrm{k} \Omega \\
    \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \\
    \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}
    \end{gathered}
    \] & 70 & 150 & ns \\
    \hline
    \end{tabular}

    \section*{Operating Rules}
    1. An external resistor \(\left(R_{X}\right)\) and an external capacitor ( \(C_{x}\) ) are required for proper operation. The value of \(\mathrm{C}_{X}\) may vary from 0 to approximately \(1000 \mu \mathrm{~F}\). For small time constants high-grade mica, glass, polypropylene, polycarbonate, or polystyrene material capacitor may be used. For large time constants use tantalum or special aluminum capacitors. If timing capacitor has leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
    2. When an electrolytic capacitor is used for \(C_{x}\) a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current. This switching diode is not needed for the 'LS221 one-shot and should not be used.
    3. For \(C_{X} \gg 1000 \mathrm{pF}\), the output pulse width ( \(\mathrm{T}_{\mathrm{W}}\) ) is defined as follows:
    \(T_{W}=K R_{X} C_{X}\)
    where [ \(R_{X}\) is in \(k \Omega\) ]
    \[
    \begin{aligned}
    & {\left[C_{X} \text { is in } p F\right]} \\
    & {\left[T_{W} \text { is in } n s\right]} \\
    & \mathrm{K} \approx \mathrm{Ln} 2=0.70
    \end{aligned}
    \]
    4. The multiplicative factor \(K\) is plotted as a function of \(C_{X}\) below for design considerations:
    

    FIGURE 1
    5. For \(C_{X}<1000 \mathrm{pF}\) see Figure 2 for \(\mathrm{T}_{W}\) vs \(\mathrm{C}_{X}\) family curves with \(\mathrm{RXX}_{\mathrm{X}}\) as a parameter:
    

    TL/F/6409-4
    6. To obtain variable pulse widths by remote trimming, the following circuit is recommended:
     TL/F/6409-5
    Note: "R Remote " should be as close to the one-shot as possible.
    FIGURE 3
    7. Output pulse width versus \(V_{C C}\) and temperatures: Figure 4 depicts the relationship between pulse width variation versus \(\mathrm{V}_{\mathrm{Cc}}\). Figure 5 depicts pulse width variation versus temperatures.
    
    8. Duty cycle is defined as \(T_{W} / T \times 100\) in percentage, if it goes above \(50 \%\) the output pulse width will become shorter. If the duty cycle varies between low and high values, this causes output pulse width to vary, or jitter (a function of the REXT only). To reduce jitter, \(\mathrm{R}_{\text {EXT }}\) should be as large as possible, for example, with \(\mathrm{R}_{\text {EXT }}=100 \mathrm{k}\) jitter is not appreciable until the duty cycle approaches 90\%.

    FIGURE 2

    \section*{Operating Rules (Continued)}
    9. Under any operating condition \(\mathrm{C}_{\mathrm{X}}\) and \(\mathrm{R}_{\mathrm{X}}\) must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I-R and Ldi/dt voltage developed along their connecting paths. If the lead length from \(\mathrm{C}_{X}\) to pins (6) and (7) or pins (14) and (15) is greater than 3 cm , for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of \(C_{X}\) in each cycle of its operation so that the output pulse width will be accurate.
    10. Although the 'LS221's pin-out is identical to the 'LS123 it should be remembered that they are not functionally identical. The 'LS123 is a retriggerable device such that the output is dependent upon the input transitions when
    its output " \(Q\) " is at the "High" state. Furthermore, it is recommended for the 'LS123 to externally ground the \(\mathrm{C}_{\mathrm{EXt}}\) pin for improved system performance. However, this pin on the 'LS221 is not an internal connection to the device ground. Hence, if substitution of an 'LS221 onto an 'LS123 design layout where the CEXT pin is wired to the ground, the device will not function.
    11. \(\mathrm{V}_{\mathrm{CC}}\) and ground wiring should conform to good high-frequency standards and practices so that switching transients on the \(V_{C C}\) and ground return leads do not cause interaction between one-shots. A \(0.01 \mu \mathrm{~F}\) to \(0.10 \mu \mathrm{~F}\) bypass capacitor (disk ceramic or monolithic type) from \(V_{C C}\) to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the \(\mathrm{V}_{\mathrm{CC}}\)-pin as space permits.
    For further detailed device characteristics and output performance, please refer to the NSC one-shot application note AN-366.

    \section*{54LS240/DM54LS240/DM74LS240, 54LS241/DM54LS241/DM74LS241 Octal TRI-STATE \({ }^{\circledR}\) Buffers/Line Drivers/Line Receivers}

    \section*{General Description}

    These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE buffers/ drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs and can be used to drive terminated lines down to \(133 \Omega\).

    \section*{Features}
    - TRI-STATE outputs drive bus lines directly
    - PNP inputs reduce DC loading on bus lines
    - Hysteresis at data inputs improves noise margins
    - Typical lol (sink current)
    \[
    \begin{array}{ll}
    54 \mathrm{LS} & 12 \mathrm{~mA} \\
    74 \mathrm{LS} & 24 \mathrm{~mA}
    \end{array}
    \]
    - Typical \(\mathrm{l}_{\mathrm{OH}}\) (source current)
    \begin{tabular}{ll} 
    54LS & -12 mA \\
    74 LS & -15 mA
    \end{tabular}
    - Typical propagation delay times

    Inverting 10.5 ns Noninverting 12 ns
    - Typical enable/disable time 18 ns
    - Typical power dissipation (enabled) Inverting \(\quad 130 \mathrm{~mW}\) Noninverting 135 mW
    - Alternate Military/Aerospace devices (54LS240/ 54LS241) are available. Contact a National Semiconductor Sales Office/Distributor for specifications.

    \section*{Connection Diagrams}
    

    Order Number 54LS240DMQB, 54LS240FMQB, 54LS240LMQB, DM54LS240J, DM74LS240WM or DM74LS240N See NS Package Number E20A, J20A, M20B, N20A or W20A
    

    \section*{Function Tables}

    \section*{LS240}
    \begin{tabular}{|c|c|c|}
    \hline \multicolumn{2}{|c|}{ Inputs } & Output \\
    \hline\(\overline{\mathbf{G}}\) & \(\mathbf{A}\) & \(\mathbf{Y}\) \\
    \hline L & L & H \\
    L & H & L \\
    H & \(X\) & Z \\
    \hline
    \end{tabular}

    LS241
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multicolumn{4}{|c|}{ Inputs } & \multicolumn{3}{c|}{ Outputs } \\
    \hline G & \(\bar{G}\) & 1A & 2A & 1Y & 2Y \\
    \hline X & L & L & X & L & \\
    X & L & H & X & H & \\
    X & H & X & X & Z & \\
    H & X & X & L & & L \\
    H & X & X & H & & H \\
    L & X & X & X & & Z \\
    \hline
    \end{tabular}
    \(\mathrm{L}=\) Low Logic Level
    \(H=\) High Logic Level
    \(X=\) Either Low or High Logic Level
    \(Z=\) High Impedance
    

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{3}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline HYS & Hysteresis ( \(\mathrm{V}_{\mathrm{T}+}-\mathrm{V}_{\mathrm{T}-}\) ) Data Inputs Only & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}\)} & 0.2 & 0.4 & & V \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{3}{*}{High Level Output Voltage} & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{I}_{\mathrm{OH}}=-1 \mathrm{~mA}
    \end{aligned}
    \]} & DM74 & 2.7 & & & \\
    \hline & & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, V_{I H}=M i n \\
    & V_{I L}=M a x, I_{O H}=-3 \mathrm{~mA}
    \end{aligned}
    \]} & DM54/DM74 & 2.4 & 3.4 & & V \\
    \hline & & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min} \\
    & \mathrm{V}_{\mathrm{IL}}=0.5 \mathrm{~V}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}
    \end{aligned}
    \]} & DM54/DM74 & 2 & & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & \mathrm{IOL}_{\mathrm{OL}}=12 \mathrm{~mA} \\
    & \mathrm{l}_{\mathrm{OL}}=\mathrm{Max}
    \end{aligned}
    \]} & DM74 & & & 0.4 & \\
    \hline & & & & DM54 & & & 0.4 & v \\
    \hline & & & & DM74 & & & 0.5 & \\
    \hline lozh & Off-State Output Current, High Level Voltage Applied & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=M a x \\
    & \mathrm{~V}_{\mathrm{IL}}=M a x \\
    & \mathrm{~V}_{\mathrm{IH}}=\text { Min }
    \end{aligned}
    \]} & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{O}}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline lozl & Off-State Output Current, Low Level Voltage Applied & & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}\)} & & & -20 & \(\mu \mathrm{A}\) \\
    \hline 1 & Input Current at Maximum Input Voltage & \multicolumn{3}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M a x, V_{1}=7 V(D M 74) \\
    & V_{1}=10 V(D M 54)
    \end{aligned}
    \]} & & & 0.1 & mA \\
    \hline IIH & High Level Input Current & \multicolumn{3}{|l|}{\(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{3}{|l|}{\(V_{C C}=\operatorname{Max}, V_{1}=0.4 \mathrm{~V}\)} & & & -0.2 & mA \\
    \hline los & Short Circuit Output Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}\) (Note 2)} & -40 & & -225 & mA \\
    \hline \multirow[t]{5}{*}{ICC} & \multirow[t]{5}{*}{Supply Current} & \multirow[t]{5}{*}{\(V_{C C}=M a x\), Outputs Open} & Outputs High & LS240, LS241 & & 13 & 23 & \\
    \hline & & & \multirow[t]{2}{*}{Outputs Low} & LS240 & & 26 & 44 & \\
    \hline & & & & LS241 & & 27 & 46 & mA \\
    \hline & & & \multirow[t]{2}{*}{Outputs Disabled} & LS240 & & 29 & 50 & \\
    \hline & & & & LS241 & & 32 & 54 & \\
    \hline
    \end{tabular}

    \footnotetext{
    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    }

    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{2}{|l|}{\multirow{3}{*}{Conditions}} & DM54LS & DM74LS & \multirow{3}{*}{Units} \\
    \hline & & & & DM54LS & DM74LS & \\
    \hline & & & & Max & Max & \\
    \hline \multirow[t]{2}{*}{\(t_{\text {PLH }}\)} & \multirow[t]{2}{*}{Propagation Delay Time Low to High Level Output} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & C_{L}=45 \mathrm{pF} \\
    & R_{L}=667 \Omega
    \end{aligned}
    \]} & LS240 & 18 & 14 & \multirow[t]{2}{*}{ns} \\
    \hline & & & LS241 & 18 & 18 & \\
    \hline \multirow[t]{2}{*}{\(t_{\text {PHL }}\)} & \multirow[t]{2}{*}{Propagation Delay Time High to Low Level Output} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & C_{L}=45 \mathrm{pF} \\
    & R_{L}=667 \Omega
    \end{aligned}
    \]} & LS240 & 18 & 18 & \multirow[t]{2}{*}{ns} \\
    \hline & & & LS241 & 18 & 18 & \\
    \hline \multirow[t]{2}{*}{\(t_{\text {PZL }}\)} & \multirow[t]{2}{*}{Output Enable Time to Low Level} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{C}_{\mathrm{L}}=45 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=667 \Omega
    \end{aligned}
    \]} & LS240 & 30 & 30 & \multirow[t]{2}{*}{ns} \\
    \hline & & & LS241 & 30 & 30 & \\
    \hline \multirow[t]{2}{*}{\(t_{\text {PZH }}\)} & \multirow[t]{2}{*}{Output Enable Time to High Level} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & C_{L}=45 \mathrm{pF} \\
    & R_{L}=667 \Omega
    \end{aligned}
    \]} & LS240 & 23 & 23 & \multirow[t]{2}{*}{ns} \\
    \hline & & & LS241 & 23 & 23 & \\
    \hline \multirow[t]{2}{*}{tplZ} & \multirow[t]{2}{*}{Output Disable Time from Low Level} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & C_{L}=5 \mathrm{pF} \\
    & R_{L}=667 \Omega
    \end{aligned}
    \]} & LS240 & 25 & 25 & \multirow[t]{2}{*}{ns} \\
    \hline & & & LS241 & 25 & 25 & \\
    \hline \multirow[t]{2}{*}{\(t_{\text {PHZ }}\)} & \multirow[t]{2}{*}{Output Disable Time from High Level} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & C_{L}=5 \mathrm{pF} \\
    & R_{L}=667 \Omega
    \end{aligned}
    \]} & LS240 & 18 & 18 & \multirow[t]{2}{*}{ns} \\
    \hline & & & LS241 & 18 & 18 & \\
    \hline \multirow[t]{2}{*}{\(t_{\text {PLH }}\)} & \multirow[t]{2}{*}{Propagation Delay Time Low to High Level Output} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & C_{L}=150 \mathrm{pF} \\
    & R_{L}=667 \Omega
    \end{aligned}
    \]} & LS240 & & 18 & \multirow[t]{2}{*}{ns} \\
    \hline & & & LS241 & & 21 & \\
    \hline \multirow[t]{2}{*}{\(t_{\text {PHL }}\)} & \multirow[t]{2}{*}{Propagation Delay Time High to Low Level Output} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & C_{L}=150 \mathrm{pF} \\
    & R_{L}=667 \Omega
    \end{aligned}
    \]} & LS240 & & 22 & \multirow[t]{2}{*}{ns} \\
    \hline & & & LS241 & & 22 & \\
    \hline \multirow[t]{2}{*}{tpzL} & \multirow[t]{2}{*}{Output Enable Time to Low Level} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & C_{L}=150 \mathrm{pF} \\
    & R_{L}=667 \Omega
    \end{aligned}
    \]} & LS240 & & 33 & \multirow[t]{2}{*}{ns} \\
    \hline & & & LS241 & & 33 & \\
    \hline \multirow[t]{2}{*}{\(t_{\text {PZ }}\)} & \multirow[t]{2}{*}{Output Enable Time to High Level} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & C_{\mathrm{L}}=150 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=667 \Omega
    \end{aligned}
    \]} & LS240 & & 26 & \multirow[t]{2}{*}{ns} \\
    \hline & & & LS241 & & 26 & \\
    \hline
    \end{tabular}

    Note: 54LS Output load is \(C_{L}=50 \mathrm{pF}\) for \(\mathrm{t}_{\mathrm{PLH}}, \mathrm{t}_{\mathrm{PHL}}, \mathrm{t}_{\mathrm{PZL}}\) and \(\mathrm{t}_{\mathrm{PZH}}\).

    \section*{DM74LS243 Quadruple Bus Transceiver}

    \section*{General Description}

    This four data line transceiver is designed for asynchronous two-way communications between data buses. It can be used to drive terminated lines down to \(133 \Omega\).

    \section*{Features}
    - Two-way asynchronous communication between data buses
    - PNP inputs reduce DC loading on bus line
    - Hysteresis at data inputs improves noise margin

    \section*{Connection Diagram}

    \section*{Dual-In-Line Package}
    

    Order Number DM74LS243WM or DM74LS243N See NS Package Number M14B or N14A

    \section*{Function Table}
    \begin{tabular}{|cc|cc|}
    \hline \multicolumn{2}{|c|}{\begin{tabular}{c} 
    Control \\
    Inputs
    \end{tabular}} & \multicolumn{2}{c|}{\begin{tabular}{c} 
    Data Port \\
    Status
    \end{tabular}} \\
    \hline GAB & GBA & A & B \\
    \hline H & H & O & I \\
    L & H & \({ }^{*}\) & \(*\) \\
    H & L & \multicolumn{2}{|c|}{ ISOLATED } \\
    L & L & I & O \\
    \hline
    \end{tabular}
    *Possibly destructive oscillation may occur if the transceivers are enabled in both directions at once.

    I = Input, O = Output.
    \(H=\) High Logic Level, L = Low Logic Level.

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Any G
    A or B
    5.5 V

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    Operating Free Air Temperature Range

    DM74LS
    Storage Temperature Range
    \[
    \begin{array}{r}
    0^{\circ} \mathrm{C} \text { to }+70^{\circ} \mathrm{C} \\
    -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C}
    \end{array}
    \]
    \begin{tabular}{c|c|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multirow{2}{*}{ Parameter } & \multicolumn{2}{|c|}{ DM74LS243 } & \multirow{2}{*}{ Units } \\
    \cline { 3 - 4 } & & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -15 & mA \\
    \hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 24 & mA \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{3}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline HYS & Hysteresis ( \(\mathrm{V}_{\mathrm{T}+}-\mathrm{V}_{\mathrm{T}-}\) ) (Data Inputs Only) & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}\)} & 0.2 & 0.4 & & V \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{3}{*}{High Level Output Voltage} & \multicolumn{3}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M i n, V_{I H}=M i n \\
    & V_{I L}=M a x, I_{O H}=-1 \mathrm{~mA}
    \end{aligned}
    \]} & 2.7 & & & \\
    \hline & & \multicolumn{3}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, V_{I H}=\operatorname{Min} \\
    & V_{I L}=M a x, I_{O H}=-3 \mathrm{~mA}
    \end{aligned}
    \]} & 2.4 & 3.4 & & V \\
    \hline & & \multicolumn{3}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.5 \mathrm{~V}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}
    \end{aligned}
    \]} & 2 & & & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M i n \\
    & V_{\mathrm{IL}}=M a x \\
    & V_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & \multicolumn{2}{|l|}{\(\mathrm{lOL}=12 \mathrm{~mA}\)} & & & 0.4 & \\
    \hline & & & \multicolumn{2}{|l|}{\(\mathrm{IOL}_{\mathrm{O}}=\mathrm{Max}\)} & & & 0.5 & V \\
    \hline lozh & Off-State Output Current, High Level Voltage Applied & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=M a x \\
    & V_{\mathrm{IL}}=M a x \\
    & V_{\mathrm{IH}}=M i n
    \end{aligned}
    \]} & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{O}}=2.7 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
    \hline lozl & Off-State Output Current, Low Level Voltage Applied & & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}\)} & & & -200 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current at Maximum Input Voltage} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & \(\mathrm{V}_{1}=5.5 \mathrm{~V}\) & A or B & & & 0.1 & mA \\
    \hline & & & \(\mathrm{V}_{1}=7 \mathrm{~V}\) & Any G & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {I }}\) & High Level Input Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{3}{|l|}{\(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.2 & mA \\
    \hline los & Short Circuit Output Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\operatorname{Max}\) (Note 2)} & -40 & & -225 & mA \\
    \hline \multirow[t]{3}{*}{Icc} & \multirow[t]{3}{*}{Supply Current} & \multirow[t]{3}{*}{\begin{tabular}{l}
    \[
    V_{C C}=M a x
    \] \\
    Outputs Open
    \end{tabular}} & \multicolumn{2}{|l|}{Outputs High} & & 22 & 38 & \\
    \hline & & & \multicolumn{2}{|l|}{Outputs Low} & & 29 & 50 & mA \\
    \hline & & & \multicolumn{2}{|l|}{Outputs Disabled} & & 32 & 54 & \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & Max & Units \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{aligned}
    & C_{\mathrm{L}}=45 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=667 \Omega
    \end{aligned}
    \] & & 18 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{aligned}
    & C_{\mathrm{L}}=45 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=667 \Omega
    \end{aligned}
    \] & & 18 & ns \\
    \hline \(\mathrm{t}_{\text {PZL }}\) & Output Enable Time to Low Level & \[
    \begin{aligned}
    & C_{\mathrm{L}}=45 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=667 \Omega \\
    & \hline
    \end{aligned}
    \] & & 30 & ns \\
    \hline \(t_{\text {PZH }}\) & Output Enable Time to High Level & \[
    \begin{aligned}
    & C_{\mathrm{L}}=45 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=667 \Omega \\
    & \hline
    \end{aligned}
    \] & & 23 & ns \\
    \hline tpLZ & Output Disable Time from Low Level & \[
    \begin{aligned}
    & C_{\mathrm{L}}=5 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=667 \Omega \\
    & \hline
    \end{aligned}
    \] & & 25 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time from High Level & \[
    \begin{aligned}
    & \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=667 \Omega
    \end{aligned}
    \] & & 18 & ns \\
    \hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{aligned}
    & C_{L}=150 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=667 \Omega
    \end{aligned}
    \] & & 21 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{aligned}
    & \mathrm{C}_{\mathrm{L}}=150 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=667 \Omega
    \end{aligned}
    \] & & 22 & ns \\
    \hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level & \[
    \begin{aligned}
    & C_{L}=150 \mathrm{pF} \\
    & R_{\mathrm{L}}=667 \Omega \\
    & \hline
    \end{aligned}
    \] & & 33 & ns \\
    \hline \(\mathrm{t}_{\text {PZH }}\) & Output Enable Time to High Level & \[
    \begin{aligned}
    & C_{L}=150 \mathrm{pF} \\
    & R_{L}=667 \Omega
    \end{aligned}
    \] & & 26 & ns \\
    \hline
    \end{tabular}

    \section*{54LS244/DM74LS244 Octal TRI-STATE \({ }^{\circledR}\) Buffers/Line Drivers/Line Receivers}

    \section*{General Description}

    These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE buffers/ drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs and can be used to drive terminated lines down to \(133 \Omega\).

    \section*{Features}
    - TRI-STATE outputs drive bus lines directly
    - PNP inputs reduce DC loading on bus lines
    - Hysteresis at data inputs improves noise margins
    - Typical lol (sink current) 54LS 12 mA 74LS \(\quad 24 \mathrm{~mA}\)
    - Typical \(\mathrm{I}_{\mathrm{OH}}\) (source current)
    \[
    \begin{array}{ll}
    \text { 54LS } & -12 \mathrm{~mA} \\
    \text { 74LS } & -15 \mathrm{~mA}
    \end{array}
    \]
    - Typical propagation delay times Inverting 10.5 ns Noninverting 12 ns
    - Typical enable/disable time 18 ns
    - Typical power dissipation (enabled)

    Inverting 130 mW
    Noninverting 135 mW

    \section*{Connection Diagram}

    Dual-In-Line Package
    

    TL/F/8442-1
    Order Number 54LS244DMQB, 54LS244FMQB, 54LS244LMQB,
    DM74LS244WM or DM74LS244N
    See NS Package Number E20A, J20A, M20B, N20A or W20A

    \section*{Function Table}
    \begin{tabular}{|c|c|c|}
    \hline \multicolumn{2}{|c|}{ Inputs } & Output \\
    \hline \(\mathbf{G}\) & \(\mathbf{A}\) & \(\mathbf{Y}\) \\
    \hline L & L & L \\
    L & H & H \\
    H & X & Z \\
    \hline
    \end{tabular}

    \footnotetext{
    \(L=\) Low Logic Level
    \(H=\) High Logic Level
    \(X=\) Either Low or High Logic Level
    Z = High Impedance
    }
    \begin{tabular}{|c|c|}
    \hline \multicolumn{2}{|l|}{olute Maximum Ratings (Note)} \\
    \hline \multicolumn{2}{|l|}{\multirow[t]{2}{*}{please contact the National Semiconductor Sales Office/Distributors for availability and specifications.}} \\
    \hline & \\
    \hline Supply Voltage & \\
    \hline Input Voltage & \\
    \hline Operating Free A & \\
    \hline & -5 \\
    \hline DM & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ}\) \\
    \hline torage Temperature Range & \({ }^{\circ} \mathrm{C}\) to \\
    \hline
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS244} & \multicolumn{3}{|c|}{DM74LS244} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \({ }^{\mathrm{IOH}}\) & High Level Output Current & & & -12 & & & -15 & mA \\
    \hline 1 OL & Low Level Output Current & & & 12 & & & 24 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{3}{|c|}{Conditions} & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline HYS & Hysteresis ( \(\mathrm{V}_{\mathrm{T}+}-\mathrm{V}_{\mathrm{T}_{-}}\)) Data Inputs Only & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}\)} & 0.2 & 0.4 & & V \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{3}{*}{High Level Output Voltage} & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{I}_{\mathrm{OH}}=-1 \mathrm{~mA}
    \end{aligned}
    \]} & DM74 & 2.7 & & & \\
    \hline & & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M i n, V_{I H}=M i n \\
    & V_{I L}=M a x, I_{O H}=-3 \mathrm{~mA}
    \end{aligned}
    \]} & 54LS/DM74 & 2.4 & 3.4 & & V \\
    \hline & & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min} \\
    & \mathrm{V}_{\mathrm{IL}}=0.5 \mathrm{~V}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}
    \end{aligned}
    \]} & 54LS/DM74 & 2 & & & \\
    \hline \multirow[t]{2}{*}{VOL} & \multirow[t]{2}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min} \\
    & V_{\mathrm{IL}}=M a x \\
    & V_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & \(\mathrm{lOL}^{\prime}=12 \mathrm{~mA}\) & 54LS/DM74 & & & 0.4 & \multirow[b]{2}{*}{V} \\
    \hline & & & \(\mathrm{lOL}_{\text {O }}=\mathrm{Max}\) & DM74 & & & 0.5 & \\
    \hline Iozh & Off-State Output Current, High Level Voltage Applied & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Max} \\
    & V_{\mathrm{IL}}=\operatorname{Max} \\
    & V_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & \multicolumn{2}{|l|}{\(V_{O}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline IozL & Off-State Output Current, Low Level Voltage Applied & & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}\)} & & & -20 & \(\mu \mathrm{A}\) \\
    \hline 1 & Input Current at Maximum Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{1}=7 V(D M 74) \\
    & V_{1}=10 V(54 L S)
    \end{aligned}
    \]} & & & 0.1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) & \multicolumn{2}{|l|}{\(\mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \(\mathrm{I}_{\text {IL }}\) & Low Level Input Current & \(\mathrm{V}_{\text {CC }}=\mathrm{Max}\) & \multicolumn{2}{|l|}{\(\mathrm{V}_{1}=0.4 \mathrm{~V}\)} & -0.5 & & -200 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{\(V_{C C}=\operatorname{Max}(\) Note 2)}} & 54LS & -50 & & -225 & mA \\
    \hline & & & & DM74 & -40 & & & \\
    \hline \multirow[t]{3}{*}{Icc} & \multirow[t]{3}{*}{Supply Current} & \multirow[t]{3}{*}{\begin{tabular}{l}
    \[
    V_{C C}=M a x,
    \] \\
    Outputs Open
    \end{tabular}} & \multicolumn{2}{|l|}{Outputs High} & & 13 & 23 & \\
    \hline & & & \multicolumn{2}{|l|}{Outputs Low} & & 27 & 46 & mA \\
    \hline & & & \multicolumn{2}{|l|}{Outputs Disabled} & & 32 & 54 & \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & 54LS Max & DM74LS Max & Units \\
    \hline \({ }^{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{aligned}
    & \mathrm{C}_{\mathrm{L}}=45 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=667 \Omega
    \end{aligned}
    \] & 18 & 18 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{aligned}
    & \mathrm{C}_{\mathrm{L}}=45 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=667 \Omega \\
    & \hline
    \end{aligned}
    \] & 18 & 18 & ns \\
    \hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level & \[
    \begin{aligned}
    & C_{L}=45 \mathrm{pF} \\
    & R_{\mathrm{L}}=667 \Omega
    \end{aligned}
    \] & 30 & 30 & ns \\
    \hline \({ }^{\text {tPZH }}\) & Output Enable Time to High Level & \[
    \begin{aligned}
    & C_{L}=45 \mathrm{pF} \\
    & R_{\mathrm{L}}=667 \Omega \\
    & \hline
    \end{aligned}
    \] & 23 & 23 & ns \\
    \hline \(t_{\text {PLZ }}\) & Output Disable Time from Low Level & \[
    \begin{aligned}
    & \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=667 \Omega
    \end{aligned}
    \] & 25 & 25 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time from High Level & \[
    \begin{aligned}
    & \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=667 \Omega \\
    & \hline
    \end{aligned}
    \] & 18 & 18 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{aligned}
    & C_{L}=150 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=667 \Omega \\
    & \hline
    \end{aligned}
    \] & & 21 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{aligned}
    & C_{L}=150 \mathrm{pF} \\
    & R_{\mathrm{L}}=667 \Omega \\
    & \hline
    \end{aligned}
    \] & & 22 & ns \\
    \hline tPZL & Output Enable Time to Low Level & \[
    \begin{aligned}
    & C_{L}=150 \mathrm{pF} \\
    & R_{\mathrm{L}}=667 \Omega \\
    & \hline
    \end{aligned}
    \] & & 33 & ns \\
    \hline \({ }_{\text {tPZH }}\) & Output Enable Time to High Level & \[
    \begin{aligned}
    & C_{L}=150 \mathrm{pF} \\
    & R_{\mathrm{L}}=667 \Omega \\
    & \hline
    \end{aligned}
    \] & & 26 & ns \\
    \hline
    \end{tabular}

    Note: 54LS Output Load is \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\) for \(\mathrm{t}_{\mathrm{PLH}}, \mathrm{t}_{\mathrm{PHL}}, \mathrm{t}_{\mathrm{PZL}}\) and \(\mathrm{t}_{\mathrm{PZH}}\).

    \section*{54LS245／DM54LS245／DM74LS245 TRI－STATE \({ }^{\circledR}\) Octal Bus Transceiver}

    \section*{General Description}

    These octal bus transceivers are designed for asynchro－ nous two－way communication between data buses．The control function implementation minimizes external timing requirements．
    The device allows data transmission from the \(A\) bus to the \(B\) bus or from the \(B\) bus to the \(A\) bus depending upon the logic level at the direction control（DIR）input．The enable input （ \(\overline{\mathrm{G}}\) ）can be used to disable the device so that the buses are effectively isolated．

    \section*{Features}
    －Bi－Directional bus transceiver in a high－density 20－pin package
    © TRI－STATE outputs drive bus lines directly
    m PNP inputs reduce DC loading on bus lines
    m Hysteresis at bus inputs improve noise margins
    －Typical propagation delay times，port－to－port 8 ns
    （1）Typical enable／disable times 17 ns
    －IOL（sink current）
    \[
    \begin{array}{ll}
    54 \mathrm{LS} & 12 \mathrm{~mA} \\
    74 \mathrm{LS} & 24 \mathrm{~mA}
    \end{array}
    \]
    － \(\mathrm{I}_{\mathrm{OH}}\)（source current）
    \[
    \begin{array}{ll}
    54 \mathrm{LS} & -12 \mathrm{~mA} \\
    74 \mathrm{LS} & -15 \mathrm{~mA}
    \end{array}
    \]

    ⿴囗十丌 Alternate Military／Aerospace device（54LS245）is avail－ able．Contact a National Semiconductor Sales Office／ Distributor for specifications．

    \section*{Connection Diagram}

    \section*{Dual－In－Line Package}
    

    Order Number 54LS245DMQB，54LS245FMQB，54LS245LMQB， DM54LS245J，DM54LS245W，DM74LS245WM or DM74LS245N See NS Package Number E20A，J20A，M20B，N20A or W20A

    TL／F／6413－1

    \section*{Function Table}
    \begin{tabular}{|cc|c|}
    \hline \begin{tabular}{c} 
    Enable \\
    \(\overline{\mathbf{G}}\)
    \end{tabular} & \begin{tabular}{c} 
    Direction \\
    Control \\
    DIR
    \end{tabular} & Operation \\
    \hline L & L & B data to \(A\) bus \\
    L & H & A data to \(B\) bus \\
    H & X & Isolation \\
    \hline
    \end{tabular}

    \footnotetext{
    \(H=\) High Level，\(L=\) Low Level，\(X=1\) rrinvart
    }
    \begin{tabular}{lr} 
    Absolute Maximum Ratings (Note) \\
    If Military/Aerospace specified devices are required, \\
    please contact the National Semiconductor Sales \\
    Office/Distributors for availability and specifications. \\
    Supply Voltage \\
    Input Voltage & 7 V \\
    DIR or \(\overline{\mathrm{G}}\) & 7 V \\
    A or B & 5.5 V \\
    Operating Free Air Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM55LS and 54LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    DMM4LS \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54LS245} & \multicolumn{3}{|c|}{DM74LS245} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -12 & & & -15 & mA \\
    \hline \(\mathrm{lOL}^{\text {l }}\) & Low Level Output Current & & & 12 & & & 24 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{3}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{3}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline HYS & Hysteresis ( \(\mathrm{V}_{\mathrm{T}+}-\mathrm{V}_{\mathrm{T}-\text { ) }}\) & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}\)} & 0.2 & 0.4 & & V \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{3}{*}{High Level Output Voltage} & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{I}_{\mathrm{OH}}=-1 \mathrm{~mA}
    \end{aligned}
    \]} & DM74 & 2.7 & & & \\
    \hline & & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Min} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{I}_{\mathrm{OH}}=-3 \mathrm{~mA}
    \end{aligned}
    \]} & DM54/DM74 & 2.4 & 3.4 & & V \\
    \hline & & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \\
    & \mathrm{V}_{\mathrm{IL}}=0.5 \mathrm{~V}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}
    \end{aligned}
    \]} & DM54/DM74 & 2 & & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Min} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & \(\mathrm{l}_{\mathrm{OL}}=12 \mathrm{~mA}\) & DM74 & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & \multirow[t]{2}{*}{\(\mathrm{I}_{\mathrm{OL}}=\mathrm{Max}\)} & DM54 & & & 0.4 & \\
    \hline & & & & DM74 & & & 0.5 & \\
    \hline Iozh & Off-State Output Current, High Level Voltage Applied & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{\mathrm{IL}}=M a x \\
    & V_{\mathrm{IH}}=M i n
    \end{aligned}
    \]} & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{O}}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline Iozl & Off-State Output Current, Low Level Voltage Applied & & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}\)} & & & -200 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current at Maximum Input Voltage} & \multirow[t]{2}{*}{\(\mathrm{V}_{C C}=\) Max} & A or B & \(\mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 0.1 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DIR or \(\overline{\mathrm{G}}\) & \(\mathrm{V}_{1}=7 \mathrm{~V}\) & & & 0.1 & \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{3}{|l|}{\(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline  & Low Level Input Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.2 & mA \\
    \hline los & Short Circuit Output Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 2)} & -40 & & -225 & mA \\
    \hline \multirow[t]{3}{*}{ICC} & \multirow[t]{3}{*}{Supply Current} & \multicolumn{2}{|l|}{Outputs High} & \multirow[t]{3}{*}{\(\mathrm{V}_{C C}=\mathrm{Max}\)} & & 48 & 70 & \\
    \hline & & \multicolumn{2}{|l|}{Outputs Low} & & & 62 & 90 & mA \\
    \hline & & \multicolumn{2}{|l|}{Outputs at Hi-Z} & & & 64 & 95 & \\
    \hline
    \end{tabular}

    \footnotetext{
    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, not to exceed one second duration
    }
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{Conditions} & \multicolumn{2}{|r|}{\multirow[t]{2}{*}{\[
    \begin{gathered}
    \hline \text { DM54/74 } \\
    \hline \text { LS245 } \\
    \hline
    \end{gathered}
    \]}} & \multirow{3}{*}{Units} \\
    \hline & & & & & \\
    \hline & & & Min & Max & \\
    \hline \(\mathrm{t}_{\text {PLH }}\) & Propagation Delay Time, Low-to-High-Level Output & \multirow{4}{*}{\[
    \begin{aligned}
    & C_{L}=45 \mathrm{pF} \\
    & R_{\mathrm{L}}=667 \Omega
    \end{aligned}
    \]} & & 12 & ns \\
    \hline \(\mathrm{t}_{\mathrm{PHL}}\) & Propagation Delay Time, High-to-Low-Level Output & & & 12 & ns \\
    \hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level & & & 40 & ns \\
    \hline \(\mathrm{t}_{\text {PZH }}\) & Output Enable Time to High Level & & & 40 & ns \\
    \hline tplz & Output Disable Time from Low Level & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & C_{L}=5 \mathrm{pF} \\
    & R_{L}=667 \Omega
    \end{aligned}
    \]} & & 25 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time from High Level & & & 25 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time, Low-to-High-Level Output & \multirow{4}{*}{\[
    \begin{aligned}
    & C_{L}=150 \mathrm{pF} \\
    & R_{\mathrm{L}}=667 \Omega
    \end{aligned}
    \]} & & 16 & ns \\
    \hline \(\mathrm{t}_{\mathrm{PHL}}\) & Propagation Delay Time, High-to-Low-Level Output & & & 17 & ns \\
    \hline \(\mathrm{t}_{\text {PZL }}\) & Output Enable Time to Low Level & & & 45 & ns \\
    \hline \(t_{\text {PZH }}\) & Output Enable Time to High Level & & & 45 & ns \\
    \hline
    \end{tabular} National Semiconductor

    \section*{54LS247/DM74LS247}

    BCD to 7-Segment Decoder/Driver with Open-Collector Outputs

    \section*{General Description}

    The 'LS247 has active LOW open-collector outputs guaranteed to sink 12 mA (Military) or 24 mA (Commercial). It has the same electrial characteristics and pin connections as the 'LS47. The only difference is that the 'LS247 will ight the top bar (segment a) for numeral 6 and the bottom bar (segment d) for number 9 . For detailed description and specifications please refer to the 'LS47 data sheet.

    \section*{Connection Diagram}
    

    \section*{Logic Symbol}
    

    TL/F/9822-2
    \(V_{C C}=\operatorname{Pin} 16\)
    \(G N D=P i n 8\)

    TL/F/9822-1
    Order Number 54LS247DMQB, 54LS247FMQB,

    \section*{DM74LS247M or DM74LS247N}

    See NS Package Number J16A, M16A, N16E or W16A
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{c|}{ Description } \\
    \hline \(\mathrm{AO}-\mathrm{AB}\) & BCD Inputs \\
    \(\overline{\mathrm{RBI}}\) & Ripple Blanking Input (Active LOW) \\
    \(\overline{\mathrm{LT}}\) & Lamp Test Input (Active LOW) \\
    \(\overline{\mathrm{BI}} / \overline{\mathrm{RBO}}\) & Blanking Input (Avtive LOW) or \\
    & Ripple Blanking Output (Active LOW) \\
    \(\overline{\mathrm{a}}-\overline{\mathrm{g}}\) & Segment Outputs (Active LOW) \\
    \hline
    \end{tabular}

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avallability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    \begin{tabular}{lr} 
    54LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Storage Temperature Range
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS247} & \multicolumn{3}{|c|}{DM74LS247} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{lOH}^{\text {l }}\) & High Level Output Current & & & -50 & & & -50 & \(\mu \mathrm{a}\) \\
    \hline \(\mathrm{lOL}^{\text {l }}\) & Low Level Output Current & & & 12 & & & 24 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M i n, l_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & 54LS & 2.4 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74LS & 2.4 & 3.4 & & \\
    \hline Ioff & Output High Current Segement Outputs & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{M}}=15 \mathrm{~V}\)} & & & 250 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & 54LS & & & 0.5 & \multirow{3}{*}{V} \\
    \hline & & & DM74LS & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{IOL}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74LS & & 0.25 & 0.5 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=10 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{ILL} & \multirow[t]{2}{*}{Low Level Input Current} & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline & & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{l}}=0.4 \mathrm{~V} \\
    & \overline{\mathrm{BI} / / \overline{\mathrm{RBO}} \text { Input }}
    \end{aligned}
    \]} & & & -1.2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & 54LS & -0.3 & & -2.0 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74LS & -0.3 & & -2.0 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & & 13 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    Switching Characteristics \(\mathrm{V}_{\mathrm{CC}}=+5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{2}{|r|}{\(R_{L}=2 \mathrm{k} \Omega(54 \mathrm{LS}=665 \Omega)\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \\
    \hline & & Min & Max & \\
    \hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & & 100 & ns \\
    \hline \({ }^{\text {PPLH }}\) & Propagation Delay Time High to Low Level Output & & 100 & ns \\
    \hline
    \end{tabular}

    \section*{54LS248/DM74LS248 BCD to 7-Segment Decoder (with 2 k \(\Omega\) Pull-Up Resistors)}

    \section*{General Description}

    The 'LS248 has active HIGH outputs with internal \(2 \mathrm{k} \Omega\) pullup resistors. It has the same electrical characteristics and pin connections as the 'LS48. The only difference is that the 'LS248 will light the top bar (segment a) for numeral 6 and the bottom bar (segment d) for numeral 9. For detailed description and specifications please refer to the 'LS48 data sheet.

    \section*{Connection Diagram}
    

    TL/F/10181-1
    Order Number 54LS248DMQB, 54LS248FMQB, DM74LS248M or DM74LS248N
    See NS Package Number J16A, M16A, N16E or W16A

    \section*{Logic Symbol}
    

    TL/F/10181-2
    \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Pin} 16 \\
    & \mathrm{GND}=\operatorname{Pin} 8
    \end{aligned}
    \]
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
    \hline AO-A3 & BCD Inputs \\
    \(\overline{\mathrm{RBI}}\) & Ripple Blanking Input (Active LOW) \\
    \(\overline{\mathrm{LT}}\) & Lamp Test Input (Active LOW) \\
    \(\overline{\mathrm{BI} / \mathrm{RBO}}\) & Blanking Input (Active LOW) or \\
    & Ripple Blanking Output (Active LOW) \\
    \(\mathrm{a-g}\) & Segment Outputs (Active HIGH) \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|}
    \hline \multicolumn{2}{|l|}{Absolute Maximum Ratings (Note)} \\
    \hline \multicolumn{2}{|l|}{If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.} \\
    \hline Supply Voltage & \\
    \hline Input Voltage & \\
    \hline Operating Free Air Temperature Range & \\
    \hline 54LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    \hline DM & \(0^{\circ} \mathrm{C}\) \\
    \hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ}\) \\
    \hline
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS248} & \multicolumn{3}{|c|}{DM74LS248} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{1 \mathrm{LL}}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \({ }^{\mathrm{lOH}}\) & High Level Output Voltage & & & -0.1 & & & -0.1 & mA \\
    \hline lOL & Low Level Output Current & & & 2 & & & 6 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & 54LS & 2.4 & & & V \\
    \hline & & & DM74 & 2.4 & & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\text {OL }}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & & 0.5 & \\
    \hline & & \(\mathrm{I}_{\mathrm{OL}}=3.2 \mathrm{~mA}\) & DM74 & & & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=10 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline ILL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & 54LS & -0.3 & & -2.0 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -0.3 & & -2.0 & \\
    \hline Icc & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}\)} & & & 38 & mA \\
    \hline loff & Output High Current & \multicolumn{2}{|l|}{Segment Inputs, \(\mathrm{V}_{\mathrm{O}}=0.85 \mathrm{~V}\)} & -1.3 & & & \(\mu \mathrm{A}\) \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{Switching Characteristics}
    \(V_{C C}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
    \begin{tabular}{c|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multirow{2}{*}{ Parameter } & \multicolumn{2}{|c|}{\(\mathbf{R}_{\mathrm{L}}=\mathbf{2 k}, \mathrm{C}_{\mathrm{L}}=\mathbf{1 5} \mathrm{pF}\)} & \multirow{2}{*}{ Units } \\
    \cline { 3 - 4 } & & \(\mathbf{M i n}\) & \(\mathbf{M a x}\) & \multirow{2}{*}{ns} \\
    \hline \(\mathrm{t}_{\mathrm{PLH}}\) & \begin{tabular}{l} 
    Propagation Delay Time \\
    Low to High Level Output
    \end{tabular} & & 100 & ns \\
    \hline \(\mathrm{t}_{\mathrm{PHL}}\) & \begin{tabular}{l} 
    Propagation Delay Time \\
    High to Low Level Output
    \end{tabular} & & 100 & \multirow{2}{*}{} \\
    \hline
    \end{tabular}

    \section*{54LS249/DM74LS249}

    BCD to 7-Segment Decoder (with Open-Collector Outputs)

    \section*{General Description}

    The 'LS249 has active HIGH open-collector outputs and incorporates the Lamp Test and BI/RBO inputs. Additionally, the 'LS249 will light the top bar (segment a) for numeral 6 and the bottom bar (segment d) for numeral 9.

    \section*{Connection Diagram}

    Dual-In-Line Package
    

    \section*{Logic Symbol}
    

    TL/F/10213-2
    \[
    \mathrm{V}_{\mathrm{CC}}=\operatorname{Pin} 16
    \]

    GND \(=\operatorname{Pin} 8\)

    Order Number 54LS249DMBQ, 54LS249FMBQ or DM74LS249N
    See NS Package Number J16A, N16E or W16A
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{c|}{ Description } \\
    \hline \(\mathrm{A}_{0}-\mathrm{A}_{3}\) & BCD Inputs \\
    \(\overline{\mathrm{BI}}\) & Blanking Input (Active LOW) \\
    \(\overline{\mathrm{LT}}\) & Lamp Test Input (Active LOW) \\
    \(\overline{\mathrm{BI} / \mathrm{RBO}}\) & \begin{tabular}{l} 
    Blanking Input (Active LOW) or \\
    \\
    \(\mathrm{a}-\mathrm{g}\)
    \end{tabular} \\
    & Ripple Blanking Output (Active LOW) \\
    Segment Outputs (Active HIGH) \\
    \hline
    \end{tabular}

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range

    54LS
    DM74LS
    Storage Temperature Range
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS249} & \multicolumn{3}{|c|}{DM74LS249} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{lOH}^{\text {l }}\) & High Level Output Current & & & \(-0.25\) & & & -0.25 & mA \\
    \hline \(\mathrm{IOL}^{\text {l }}\) & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & 54LS & 2.4 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{l}=10 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}\)} & Inputs & -0.03 & & -0.4 & \multirow[t]{2}{*}{mA} \\
    \hline & & & \(\mathrm{BI} / \overline{\mathrm{RBO}}\) & -0.09 & & -1.2 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 2)} & 54LS & -0.3 & & -2.0 & \multirow{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline \(\mathrm{I}_{\mathrm{CC}}\) & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{IN}}=4.5 \mathrm{~V}\)} & & & 15 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    at \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{2}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \\
    \hline & & Min & Max & \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    tpHL
    \end{tabular} & Propagation Delay Time \(A_{n}\) to a-g (54LS \(R_{L}=2 \mathrm{k} \Omega\) ) & & \[
    \begin{aligned}
    & 100 \\
    & 100 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \begin{tabular}{l}
    tplH \\
    tpHL
    \end{tabular} & Propagation Delay Time \(\overline{\mathrm{BI}}\) to \(\mathrm{a}-\mathrm{g}\left(54 \mathrm{LS} \mathrm{R}_{\mathrm{L}}=6 \mathrm{k} \Omega\right)\) & & \[
    \begin{aligned}
    & 100 \\
    & 100
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}

    Numerical Designations-Resultant Displays
    

    \section*{Truth Table}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Decimal or Function} & \multicolumn{6}{|c|}{Inputs} & \multicolumn{7}{|c|}{Outputs} & \multirow{2}{*}{Note} \\
    \hline & \(\overline{\mathbf{L T}}\) & \(\mathrm{A}_{3}\) & \(\mathrm{A}_{2}\) & \(A_{1}\) & \(\mathrm{A}_{0}\) & BI/RBO & a & b & c & d & e & f & g & \\
    \hline 0 & H & L & L & L & L & H & H & H & H & H & H & H & L & 1 \\
    \hline 1 & H & \(L\) & L & L & H & H & L & H & H & L & L & L & L & 1 \\
    \hline 2 & H & L & L & H & L & H & H & H & L & H & H & L & H & \\
    \hline 3 & H & L & L & H & H & H & H & H & H & H & L & L & H & \\
    \hline 4 & H & L & H & L & L & H & L & H & H & L & L & H & H & \\
    \hline 5 & H & L & H & L & H & H & H & L & H & H & L & H & H & \\
    \hline 6 & H & L & H & H & L & H & L & L & H & H & H & H & H & \\
    \hline 7 & H & L & H & H & H & H & H & H & H & L & L & L & L & \\
    \hline 8 & H & H & L & L & L & H & H & H & H & H & H & H & H & \\
    \hline 9 & H & H & L & L & H & H & H & H & H & L & L & H & H & \\
    \hline 10 & H & H & L & H & L & H & L & L & L & H & H & L & H & \\
    \hline 11 & H & H & L & H & H & H & L & L & H & H & L & L & H & \\
    \hline 12 & H & H & H & L & L & H & L & H & L & L & L & H & H & \\
    \hline 13 & H & H & H & L & H & H & H & L & L & H & L & H & H & \\
    \hline 14 & H & H & H & H & L & H & L & L & L & H & H & H & H & \\
    \hline 15 & H & H & H & H & H & H & L & L & L & L & L & L & L & \\
    \hline BI & X & X & X & X & X & L & L & L & L & L & L & L & L & 2 \\
    \hline LT & L & X & X & X & X & H & H & H & H & H & H & H & H & 3 \\
    \hline
    \end{tabular}

    Note 1: \(\overline{\mathrm{BI} / \mathrm{RBO}}\) is wired-AND logic serving as blanking input ( \(\overline{\mathrm{BI}})\) and/or ripple-blanking output ( \(\overline{\mathrm{RBO}}\) ). The blanking out ( \(\overline{\mathrm{BI}}\) ) must be open or held at a HIGH level when output functions 0 through 15 are desired. \(X=\) input may be HIGH or LOW.
    Note 2: When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level, regardless of the state of any other input condition.
    Note 3: When the blanking input/ripple-blanking output ( \(\overline{\mathrm{BI} / \mathrm{RBO}}\) ) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a HIGH level.

    \section*{Logic Diagram}
    

    \section*{DM54LS251/DM74LS251 \\ TRI-STATE \({ }^{\circledR}\) Data Selectors/Multiplexers}

    \section*{General Description}

    These data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources, and feature a strobe-controlled TRI-STATE output. The strobe must be at a low logic level to enable these devices. The TRI-STATE outputs permit direct connection to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totempole outputs.
    To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

    \section*{Features}
    - TRI-STATE version of LS151
    - Interface directly with system bus
    - Perform parallel-to-serial conversion
    - Permit multiplexing from N -lines to one line
    - Complementary outputs provide true and inverted data
    - Maximum number of common outputs

    54LS 49
    74LS 129
    - Typical propagation delay time ( D to Y )

    54LS 17 ns
    74LS 17 ns
    - Typical power dissipation

    54LS 35 mW
    74LS 35 mW

    \section*{Connection Diagram}
    

    TL/F/6415-1
    Order Number DM54LS251J, DM54LS251W, DM74LS251M or DM74LS251N
    See NS Package Number J16A, M16A, N16E or W16A

    \section*{Function Table}
    \begin{tabular}{|ccc|c|cc|}
    \hline \multicolumn{4}{c|}{ Inputs } & \multicolumn{2}{c|}{ Outputs } \\
    \cline { 1 - 3 } & Select & Strobe & Y & W \\
    \cline { 1 - 3 } C & B & A & S & & \\
    \hline X & X & X & H & Z & Z \\
    L & L & L & L & D0 & \(\overline{\text { DO }}\) \\
    L & L & H & L & D1 & \(\overline{\text { D1 }}\) \\
    L & H & L & L & D2 & \(\overline{\text { D2 }}\) \\
    L & H & H & L & D3 & \(\overline{\text { D3 }}\) \\
    H & L & L & L & D4 & \(\overline{\text { D4 }}\) \\
    H & L & H & L & D5 & \(\overline{\text { D5 }}\) \\
    H & H & L & L & D6 & \(\overline{\text { D6 }}\) \\
    H & H & H & L & D7 & \(\overline{\text { D7 }}\) \\
    \hline
    \end{tabular}

    H = High Logic Level, L = Low Logic Level,
    \(X=\) Don't Care, \(Z=\) High Impedance (Off)
    D0, D1 . . D7 = The level of the respective \(D\) input

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage 7V
    Operating Free Air Temperature Range
    \begin{tabular}{lr} 
    DM54LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54LS251} & \multicolumn{3}{|c|}{DM74LS251} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -1 & & & -2.6 & mA \\
    \hline lOL & Low Level Output Current & & & 12 & & & 24 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{VOH} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\
    & V_{I L}=\operatorname{Max}, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.4 & 3.4 & & \multirow[b]{2}{*}{V} \\
    \hline & & & DM74 & 2.4 & 3.1 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{l} \mathrm{OL}=12 \mathrm{~mA}\) & DM74 & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \(\mathrm{I}_{\text {IL }}\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline lozH & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{\mathrm{O}}=2.7 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, V_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline lozl & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=0.4 V \\
    & V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
    \end{aligned}
    \]} & & & -20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -20 & & -100 & \multirow[b]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline \(\mathrm{lCC1}\) & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\) (Note 3)} & & 6.1 & 10 & mA \\
    \hline ICC2 & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}\) (Note 4)} & & 7.1 & 12 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: \(\mathrm{I}_{\mathrm{C}} 1\) is measured with the outputs open, STROBE grounded, and all other inputs at 4.5 V .
    Note 4: \(\mathrm{l}_{\mathrm{CC}}\) is measured with the outputs open and all inputs at 4.5 V .

    Switching Characteristics
    at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{From (Input) to (Output)} & \multicolumn{4}{|c|}{\(R_{L}=667 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=45 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=150 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    \text { A, B, C } \\
    \text { (4 Levels) to } Y \\
    \hline
    \end{gathered}
    \] & & 45 & & 53 & ns \\
    \hline tPHL & Propagation Delay Time High to Low Level Output & A, B, C (4 Levels) to \(Y\) & & 45 & & 53 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & A, B, C (3 Levels) to W & & 33 & & 38 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \text { A, B, C } \\
    \text { (3 Levels) to W }
    \end{gathered}
    \] & & 33 & & 42 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    \mathrm{D} \\
    \text { to } \mathrm{Y}
    \end{gathered}
    \] & & 28 & & 35 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \mathrm{D} \\
    \text { to } \mathrm{Y}
    \end{gathered}
    \] & & 28 & & 38 & ns \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    D \\
    \text { to } \mathrm{W}
    \end{gathered}
    \] & & 15 & & 25 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    D \\
    \text { to } \mathrm{W}
    \end{gathered}
    \] & & 15 & & 25 & ns \\
    \hline \(t_{\text {PZH }}\) & Output Enable Time to High Level Output & Strobe to \(Y\) & & 45 & & 60 & ns \\
    \hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level Output & Strobe to Y & & 40 & & 51 & ns \\
    \hline \({ }^{\text {tPHZ }}\) & Output Disable Time from High Level Output (Note 1) & Strobe to \(Y\) & & 45 & & & ns \\
    \hline \(t_{\text {PLZ }}\) & Output Disable Time from Low Level Output (Note 1) & Strobe to Y & & 25 & & & ns \\
    \hline \(t_{\text {PRH }}\) & Output Enable Time to High Level Output & Strobe to W & & 27 & & 40 & ns \\
    \hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level Output & Strobe to W & & 40 & & 47 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time from High Level Output (Note 1) & Strobe to W & & 55 & & & ns \\
    \hline \(t_{\text {PLZ }}\) & Output Disable Time from Low Level Output (Note 1) & Strobe to W & & 25 & & & ns \\
    \hline
    \end{tabular}

    Note 1: \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\)

    \section*{Logic Diagram}
    

    TL/F/6415-2

    \section*{54LS253/DM54LS253/DM74LS253 TRI-STATE \({ }^{\otimes}\) Data Selectors/Multiplexers}

    \section*{General Description}

    Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.
    The TRI-STATE outputs can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level.

    \section*{Features}
    - TRI-STATE version of LS153 with same pinout
    - Schottky-diode-clamped transistors
    - Permit multiplexing from N -lines to one line
    - Performs parallel-to-serial conversion

    ■ Strobe/output control
    - High fanout totem-pole outputs
    - Typical propagation delay Data to output 12 ns Select to output 21 ns
    - Typical power dissipation 35 mW
    - Alternate Military/Aerospace device (54LS253) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

    Function Table
    \begin{tabular}{|cc|cccc|c|c|}
    \hline \begin{tabular}{c} 
    Select \\
    Inputs
    \end{tabular} & & \multicolumn{3}{|c|}{ Data Inputs } & & \begin{tabular}{c} 
    Output \\
    Control
    \end{tabular} & Output \\
    \hline B & A & C0 & C1 & C2 & C3 & G & Y \\
    \hline X & X & X & X & X & X & H & Z \\
    L & L & L & X & X & X & L & L \\
    L & L & H & X & X & X & L & H \\
    L & H & X & L & X & X & L & L \\
    L & H & X & H & X & X & L & H \\
    H & L & X & X & L & X & L & L \\
    H & L & X & X & H & X & L & H \\
    H & H & X & X & X & L & L & L \\
    H & H & X & X & X & H & L & H \\
    \hline
    \end{tabular}

    Address Inputs A and B are common to both sections. \(H=\) High Level, \(L=\) Low Level, \(X=\) Don't Care, \(Z=\) High Impedance (off).

    Connection Diagram
    

    Order Number 54LS253DMQB, 54LS253FMQB, 54LS253LMQB, DM54LS253J, DM54LS253W, DM74LS253M or DM74LS253N
    See NS Package Number E20A, J16A, M16A, N16E or W16A

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avallablility and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    DM54LS and 54LS
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    DM74LS
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    Storage Temperature Range
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54LS253} & \multicolumn{3}{|c|}{DM74LS253} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -1 & & & -2.6 & mA \\
    \hline lOL & Low Level Output Current & & & 12 & & & 24 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \begin{tabular}{l}
    Typ \\
    (Note 1)
    \end{tabular} & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & DM54 & 2.4 & 3.4 & & V \\
    \hline & & & DM74 & 2.4 & 3.1 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & DM54 & & & 0.4 & \\
    \hline & & & DM74 & & & 0.5 & V \\
    \hline & & \(\mathrm{l}_{\mathrm{OL}}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(I_{1 H}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, V_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \(1 / \mathrm{L}\) & Low Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline lozH & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=2.7 V \\
    & V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
    \end{aligned}
    \]} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline lozl & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=0.4 \\
    & V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
    \end{aligned}
    \]} & & & -20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=M a x
    \] \\
    (Note 2)
    \end{tabular}} & DM54 & -20 & & -100 & \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline \(\mathrm{I}_{\mathrm{CC} 1}\) & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 3)} & & 7 & 12 & mA \\
    \hline ICC2 & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 4)} & & 8.5 & 14 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: \(\mathrm{I}_{\mathrm{C} 1}\) is measured with all outputs open, and all the inputs grounded.
    Note 4: \(\mathrm{I}_{\mathrm{CC}}\) is measured with the outputs open, OUTPUT CONTROL at 4.5 V and all other inputs grounded.
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(R_{L}=667 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=45 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=150 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & Data to \(Y\) & & 25 & & 35 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to \(Y\) & & 20 & & 30 & ns \\
    \hline \({ }^{\text {PPLH }}\) & Propagation Delay Time Low to High Level Output & Select to \(Y\) & & 45 & & 54 & ns \\
    \hline \({ }^{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Select to \(Y\) & & 32 & & 44 & ns \\
    \hline \({ }_{\text {tpzH }}\) & Output Enable Time to High Level Output & Output Control to \(Y\) & & 18 & & 32 & ns \\
    \hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level Output & Output Control to Y & & 23 & & 35 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time from High Level Output (Note 1) & Output Control to \(Y\) & & 41 & & & ns \\
    \hline tpLz & Output Disable Time from Low Level Output (Note 1) & Output Control to \(Y\) & & 27 & & & ns \\
    \hline
    \end{tabular}

    Note 1: \(C_{L}=5 \mathrm{pF}\).

    \section*{Logic Diagram}
    

    National Semiconductor

    \section*{54LS256/DM74LS256 Dual 4-Bit Addressable Latch}

    \section*{General Description}

    The 'LS256 is a dual 4-bit addressable latch with common control inputs; these include two Address inputs (A0, A1), an active LOW enable input ( \(\bar{E}\) ) and an active LOW Clear input ( \(\overline{\mathrm{CL}}\) ). Each latch has a Data input (D) and four outputs (Q0-Q3).
    When the Enable ( \(\overline{\mathrm{E}}\) ) is HIGH and the Clear input ( \(\overline{\mathrm{CL}}\) ) is LOW, all outputs (QO-Q3) are LOW. Dual 4-channel demultiplexing occurs when the \(\overline{C L}\) and \(\bar{E}\) are both LOW. When \(\overline{\mathrm{CL}}\) is HIGH and \(\overline{\mathrm{E}}\) is LOW, the selected output (Q0-Q3), determined by the Address inputs, follows D. When the E goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ( \(\bar{E}=\) LOW, \(\overline{C L}=\) HIGH), changing more than one bit of the Address (AO, A1)
    could impose a transient wrong address. Therefore, this should be done only while in the memory mode ( \(\overline{\mathrm{E}}=\overline{\mathrm{CL}}=\) HIGH).

    \section*{Features}
    - Serial-to-parallel capability
    - Output from each storage bit available
    - Random (addressable) data entry
    - Easily expandable
    - Active low common clear

    \section*{Connection Diagram}

    Dual-In-Line Package
    

    TL/F/9823-1
    Order Number 54LS256DMQB,
    54LS256FMQB or DM74LS256N
    See NS Package Number J16A, N16E or W16A

    Logic Symbol
    
    \(V_{C C}=\operatorname{Pin} 16\)
    GND \(=\operatorname{Pin} 8\)
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
    \hline\(A 0, A 1\) & Common Address Inputs \\
    \(\mathrm{D}_{\mathrm{a}}, \mathrm{D}_{\mathrm{b}}\) & Data Inputs \\
    \(\overline{\mathrm{E}}\) & Common Enable Input (Active LOW) \\
    \(\overline{\mathrm{CL}}\) & Conditional Clear Input (Active LOW) \\
    \(\mathrm{QO}_{\mathrm{a}}-\mathrm{Q}_{3} \mathrm{a}\) & Side \(A\) Latch Outputs \\
    \(\mathrm{QO} \mathrm{D}_{\mathrm{b}}-\mathrm{Q}_{3} \mathrm{~b}\) & Side B Latch Outputs \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{4}{|c|}{Inputs} & \multicolumn{4}{|c|}{Outputs} & \multirow[t]{2}{*}{Mode} \\
    \hline \(\overline{\mathbf{C L}}\) & \(\bar{E}\) & A0 & A1 & Q0 & Q1 & Q2 & Q3 & \\
    \hline L & H & X & X & L & L & L & L & Clear \\
    \hline L & L & L & L & D & L & L & L & Demultiplex \\
    \hline L & L & H & L & L & D & L & L & \\
    \hline L & L & L & H & L & L & D & L & \\
    \hline L & L & H & H & L & L & L & D & \\
    \hline H & H & X & X & \(Q_{t-1}\) & \(Q_{t-1}\) & \(Q_{t-1}\) & \(\mathrm{Q}_{\mathrm{t}-1}\) & Memory \\
    \hline H & L & L & L & D & \(Q_{t-1}\) & \(Q_{t-1}\) & \(Q_{t-1}\) & Addressable \\
    \hline H & L & H & L & \(Q_{t-1}\) & D & \(\mathrm{Q}_{\mathrm{t}-1}\) & \(\mathrm{Q}_{\mathrm{t}-1}\) & Latch \\
    \hline H & L & L & H & \(Q_{t-1}\) & \(Q_{t-1}\) & D & \(Q_{t-1}\) & \\
    \hline H & L & H & H & \(\mathrm{Q}_{\mathrm{t}-1}\) & \(Q_{t-1}\) & \(Q_{t-1}\) & D & \\
    \hline
    \end{tabular}

    \footnotetext{
    \(t-1=\) Bit time before address change or rising edge of \(E\)
    \(H=\) HIGH Voltage Level
    L = LOW Voltage Level
    \(X=\) Immaterial
    }

    Mode Selection
    \begin{tabular}{|c|c|l|}
    \hline\(\overline{\mathbf{E}}\) & \(\overline{\mathbf{C L}}\) & \multicolumn{1}{|c|}{ Mode } \\
    \hline L & H & Addressable Latch \\
    H & H & Memory \\
    L & L & Active HIGH 4-Channel Demultiplexers \\
    H & L & Clear \\
    \hline
    \end{tabular}

    \section*{Logic Diagram}
    

    TL/F/9823-3
    ```

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for avallability and specifications.
    Supply Voltage
    7 V
    Input Voltage
    $7 V$
    Operating Free Air Temperature Range
    54LS
    DM74LS
    Storage Temperature Range
    $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
    $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$
    $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

    ```

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS256} & \multicolumn{3}{|c|}{DM74LS256} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{lOH}^{2}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \(\mathrm{t}_{\mathrm{s}}(\mathrm{H})\) & Setup Time HIGH, \(D_{n}\) to \(\bar{E}\) & 20 & & & 20 & & & ns \\
    \hline \(t_{n}(H)\) & Hold Time HIGH, \(\mathrm{D}_{\mathrm{n}}\) to \(\overline{\mathrm{E}}\) & 0 & & & 0 & & & ns \\
    \hline \(t_{s}(L)\) & Setup Time LOW, \(\mathrm{D}_{\mathrm{n}}\) to \(\bar{E}\) & 15 & & & 15 & & & ns \\
    \hline \(t_{n}(L)\) & Hold Time LOW, \(\mathrm{D}_{\mathrm{n}}\) to \(\bar{E}\) & 0 & & & 0 & & & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L})
    \end{aligned}
    \] & Setup Time HIGH or LOW, \(A_{n}\) to \(\bar{E}\) & 0 & & & 0 & & & ns \\
    \hline \(t_{w}(L)\) & E Pulse Width LOW & 17 & & & 17 & & & ns \\
    \hline
    \end{tabular}

    \section*{Electrical Characteristics}

    Over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \begin{tabular}{l}
    Typ \\
    (Note 1)
    \end{tabular} & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M \ln , I_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O H}=M a x \\
    & V_{I L}=M a x
    \end{aligned}
    \]} & 54LS & 2.5 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{V \({ }_{\text {OL }}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\
    & V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline \multirow[t]{2}{*}{11} & \multirow[t]{2}{*}{Input Current @ Max Input Voltage} & \multirow[t]{2}{*}{\(V_{C C}=M a x, V_{1}=10 \mathrm{~V}\)} & Inputs & & & 0.1 & \multirow[t]{2}{*}{mA} \\
    \hline & & & E & & & 0.2 & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{IIH}^{\text {H}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\)} & Inputs & & & 20 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & \(\bar{E}\) & & & 40 & \\
    \hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=0.4 \mathrm{~V}\)} & Inputs & & & -0.4 & \multirow[t]{2}{*}{mA} \\
    \hline & & & \(\bar{E}\) & & & -0.8 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline Icc & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & & 25 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    \begin{tabular}{|c|c|c|c|}
    \hline \multicolumn{4}{|l|}{Switching Characteristics
    \(\mathrm{V}_{C C}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configuratio} \\
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \[
    \begin{aligned}
    & R_{\mathrm{L}}=2 \mathrm{k} \Omega \\
    & \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}
    \end{aligned}
    \] & \multirow[t]{2}{*}{Units} \\
    \hline & & Max & \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\bar{E}\) to \(Q_{n}\) & \[
    \begin{aligned}
    & 27 \\
    & 24 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay
    \[
    D_{n} \text { to } Q_{n}
    \] & \[
    \begin{array}{r}
    30 \\
    20 \\
    \hline
    \end{array}
    \] & ns \\
    \hline  & Propagation Delay
    \[
    A_{n} \text { to } Q_{n}
    \] & \[
    \begin{aligned}
    & 30 \\
    & 29
    \end{aligned}
    \] & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay \(\overline{C L}\) to \(Q_{n}\) & 18 & ns \\
    \hline
    \end{tabular}

    \section*{54LS257A/DM54LS257B/DM74LS257B, 54LS258A/DM54LS258B/DM74LS258B TRI-STATE \({ }^{\circledR}\) Quad 2-Data Selectors/Multiplexers}

    \section*{General Description}

    These Schottky-clamped high-performance multiplexers feature TRI-STATE outputs that can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output enable circuitry is designed such that the output disable times are shorter than the output enable times.
    This TRI-STATE output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

    \section*{Features}
    - TRI-STATE versions LS157 and LS158 with same pinouts
    - Schottky-clamped for significant improvement in A-C performance
    - Provides bus interface from multiple sources in highperformance systems
    - Average propagation delay from data input 12 ns
    - Typical power dissipation

    LS257B 50 mW
    LS258B 35 mW
    - Alternate military/aerospace devices (54LS257A/ 54LS258A) are available. Contact a National Semiconductor Sales Office/Distributor for specifications.

    \section*{Connection Diagrams}
    

    TL/F/6417-1
    Order Number 54LS257ADMQB, 54LS257AFMQB, 54LS257ALMQB, DM54LS257BJ, DM54LS257BW, DM74LS257BM or DM74LS257BN
    See NS Package Number E20A, J16A, M16A, N16E or W16A
    

    TL/F/6417-2 Order Number 54LS258ADMQB, 54LS258AFMQB, 54LS258ALMQB, DM54LS258BJ, DM54LS258BW, DM74LS258BM or DM74LS258BN
    See NS Package Number E20A, J16A, M16A, N16E or W16A

    \section*{Function Table}
    \begin{tabular}{|c|c|cc|c|c|}
    \hline \multicolumn{4}{|c|}{ Inputs } & \multicolumn{3}{c|}{ Output Y } \\
    \hline \begin{tabular}{c} 
    Output \\
    Control
    \end{tabular} & Select & A & B & LS257 & LS258 \\
    \hline H & X & X & X & Z & Z \\
    L & L & L & X & L & H \\
    L & L & H & X & H & L \\
    L & H & X & L & L & H \\
    L & H & X & H & H & L \\
    \hline
    \end{tabular}

    \footnotetext{
    \(H=\) High Level, L = Low Level, X = Don't Care,
    \(Z=\) High Impedance (off)
    }
    ```

    Absolute Maximum Ratings (Note)

    ```

    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    7V
    Operating Free Air Temperature Range
    DM54LS and 54LS
    DM74LS
    Storage Temperature Range
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[b]{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54LS257B} & \multicolumn{3}{|c|}{DM74LS257B} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{\text {l }}\) & High Level Output Current & & & -1 & & & -2.6 & mA \\
    \hline lOL & Low Level Output Current & & & 12 & & & 24 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    \section*{'LS257B Electrical Characteristics}
    over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O H}=\operatorname{Max} \\
    & V_{I L}=M a x, V_{I H}=M i n
    \end{aligned}
    \]} & DM54 & 2.4 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.4 & 3.1 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\
    & V_{I L}=\operatorname{Max}, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{I}_{\mathrm{OL}}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current @ Max Input Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x, \\
    & V_{1}=7 V
    \end{aligned}
    \]} & Select & & & 0.2 & \multirow[t]{2}{*}{mA} \\
    \hline & & & Other & & & 0.1 & \\
    \hline \multirow[t]{2}{*}{\({ }_{1 /}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x, \\
    & V_{1}=2.7 V
    \end{aligned}
    \]} & Select & & & 40 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & Other & & & 20 & \\
    \hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x, \\
    & V_{1}=0.4 V
    \end{aligned}
    \]} & Select & & & \(-0.8\) & \multirow[t]{2}{*}{mA} \\
    \hline & & & Other & & & -0.4 & \\
    \hline lozh & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=2.7 \mathrm{~V} \\
    & V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
    \end{aligned}
    \]} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline lozl & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=0.4 V \\
    & V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
    \end{aligned}
    \]} & & & -20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline \({ }^{\text {ICCH }}\) & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 3)} & & 5.9 & 10 & mA \\
    \hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}(\) Note 3)} & & 9.2 & 16 & mA \\
    \hline ICCZ & Supply Current with Outputs Disabled & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}(\) Note 3)} & & 12 & 19 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: ICC is measured with all outputs open and all possible inputs grounded, while achieving the stated output conditions.
    'LS257B Switching Characteristics
    at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(R_{L}=667 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=45 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(C_{L}=150 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \({ }^{\text {tpLH }}\) & Propagation Delay Time Low to High Level Output & Data to Output & & 18 & & 27 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
    Data to \\
    Output
    \end{tabular} & & 18 & & 27 & ns \\
    \hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & Select to Output & & 28 & & 35 & ns \\
    \hline tphL & Propagation Delay Time High to Low Level Output & Select to Output & & 35 & & 42 & ns \\
    \hline \(t_{\text {PZH }}\) & Output Enable Time to High Level Output & Output Control to \(Y\) & & 15 & & 27 & ns \\
    \hline \(\mathrm{t}_{\text {PZL }}\) & Output Enable Time to Low Level Output & Output Control to \(Y\) & & 28 & & 38 & ns \\
    \hline \(\mathrm{t}_{\text {PHZ }}\) & Output Disable Time from High Level Output (Note 1) & Output Control to \(Y\) & & 26 & & & ns \\
    \hline \(t_{\text {PLZ }}\) & Output Disable Time from Low Level Output (Note 1) & Output Control to \(Y\) & & 25 & & & ns \\
    \hline
    \end{tabular}

    Note 1: \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\).

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54LS258B} & \multicolumn{3}{|c|}{DM74LS258B} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{1 H}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \({ }^{\mathrm{OH}}\) & High Level Output Current & & & -1 & & & -2.6 & mA \\
    \hline \(\mathrm{lOL}^{2}\) & Low Level Output Current & & & 12 & & & 24 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    \section*{'LS258B Electrical Characteristics}
    over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\
    & V_{I L}=\operatorname{Max}, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.4 & 3.4 & & V \\
    \hline & & & DM74 & 2.4 & 3.1 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{l}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{I}_{\mathrm{OL}}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current @ Max Input Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x, \\
    & V_{1}=7 V
    \end{aligned}
    \]} & Select & & & 0.2 & \multirow[t]{2}{*}{mA} \\
    \hline & & & Other & & & 0.1 & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{I}_{\mathrm{H}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x, \\
    & V_{1}=2.7 V
    \end{aligned}
    \]} & Select & & & 40 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & Other & & & 20 & \\
    \hline
    \end{tabular}

    \section*{'LS258B Electrical Characteristics}
    over recommended operating free air temperature range (unless otherwise noted) (Continued)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x, \\
    & V_{1}=0.4 V
    \end{aligned}
    \]} & Select & & & -0.8 & \multirow[t]{2}{*}{mA} \\
    \hline & & & Other & & & -0.4 & \\
    \hline \(\mathrm{l}^{\text {OZH }}\) & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{O}}=2.7 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline Iozl & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & -20 & \(\mu \mathrm{A}\) \\
    \hline los & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=\operatorname{Max}
    \] \\
    (Note 2)
    \end{tabular}} & DM54 & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline \(\mathrm{I}_{\mathrm{CCH}}\) & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}(\) Note 3)} & & 4.1 & 7 & mA \\
    \hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}(\) Note 3)} & & 9 & 14 & mA \\
    \hline ICCZ & Supply Current with Outputs Disabled & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}(\) Note 3)} & & 12 & 19 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: ICC is measured with all outputs open and all possible inputs grounded, while achieving the stated output conditions.

    \section*{'LS258B Switching Characteristics}
    at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=667 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(C_{L}=45 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=150 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Data to Output & & 18 & & 27 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to Output & & 18 & & 27 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Select to Output & & 28 & & 35 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Select to Output & & 35 & & 42 & ns \\
    \hline tPZH & Output Enable Time to High Level Output & Output Control to \(Y\) & & 15 & & 27 & ns \\
    \hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level Output & Output Control to \(Y\) & & 28 & & 38 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time from High Level Output (Note 4) & Output Control to \(Y\) & & 26 & & & ns \\
    \hline \(t_{\text {PLZ }}\) & Output Disable Time from Low Level Output (Note 4) & Output Control to \(Y\) & & 25 & & & ns \\
    \hline
    \end{tabular}

    Note 4: \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\).
    

    LS258B
    

    TL/F/6417-4

    \section*{54LS259/DM74LS259 8-Bit Addressable Latches}

    \section*{General Description}

    These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.
    Four distinct modes of operation are selectable by controlling the clear and enable inputs as enumerated in the function table. In the addressable-latch mode, data at the datain terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

    \section*{Features}
    - 8-Bit parallel-out storage register performs serial-to-parallel conversion with storage
    - Asynchronous parallel clear
    - Active high decoder
    - Enable/disable input simplifies expansion
    - Direct replacement for Fairchild 9334
    - Expandable for N -bit applications
    - Four distinct functional modes
    - Typical propagation delay times:

    Enable-to-output 18 ns
    Data-to-output 16 ns
    Address-to-output 21 ns
    Clear-to-output 17 ns
    - Fan-out
    lol (sink current) 54LS259 4 mA 74LS259 8 mA \(\mathrm{IOH}^{(\text {source current) }}-0.4 \mathrm{~mA}\)
    - Typical ICC 22 mA

    \section*{Connection Diagram}
    

    Order Number 54LS259DMQB, 54LS259FMQB, 54LS259LMQB, DM74LS259WM or DM74LS259N See NS Package Number E20A, J16A, M16B, N16E or W16A

    \section*{Function Table}
    \begin{tabular}{|cc|c|c|l|}
    \hline \multicolumn{2}{|c|}{ Inputs } & \begin{tabular}{c} 
    Output of \\
    Addressed \\
    Latch
    \end{tabular} & \begin{tabular}{c} 
    Each \\
    Other \\
    Output
    \end{tabular} & \multicolumn{1}{|c|}{ Function } \\
    \hline H & E & L & D & Q \(_{i 0}\) \\
    H & H & Q \(_{i 0}\) & Q \(_{i 0}\) & Addressable Latch \\
    L & L & D & L & 8-Line Demultiplexer \\
    L & H & L & L & Clear \\
    \hline
    \end{tabular}

    Latch Selection Table
    \begin{tabular}{|ccc|c|}
    \hline \multicolumn{3}{c|}{ Select Inputs } & \multirow{2}{c|}{\begin{tabular}{c} 
    Latch \\
    Addressed
    \end{tabular}} \\
    \hline C & B & A & 0 \\
    L & L & L & 1 \\
    L & L & H & 2 \\
    L & H & H & 3 \\
    H & L & L & 4 \\
    H & L & H & 5 \\
    H & H & L & 6 \\
    H & H & H & 7 \\
    \hline
    \end{tabular}

    \footnotetext{
    \(H=\) High Level, \(L=\) Low Level
    \(D=\) the Level of the Data Input
    \(Q_{i 0}=\) the Level of \(Q_{i}(i=0,1, \ldots 7\), as Appropriate) before the Indicated Steady-State Input Conditions Were Established.
    }
    

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{54LS259} & \multicolumn{3}{|c|}{DM74LS259} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\text {CC }}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{l}_{\mathrm{OH}}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 4 & & & 8 & mA \\
    \hline \multirow[t]{2}{*}{\(t^{W}\)} & \multirow[t]{2}{*}{Pulse Width (Note 7)} & Enable & 17 & & & 15 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Clear & 17 & & & 15 & & & \\
    \hline \multirow[t]{2}{*}{tsu} & \multirow[t]{2}{*}{\begin{tabular}{l}
    Setup Time \\
    (Notes 1, 2, 3 \& 7)
    \end{tabular}} & Data & \(20 \uparrow\) & & & \(15 \uparrow\) & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Select & 15 \(\downarrow\) & & & 15 \(\downarrow\) & & & \\
    \hline \multirow[t]{2}{*}{\({ }_{\text {t }}^{\mathrm{H}}\)} & \multirow[t]{2}{*}{Hold Time (Notes 1, 2 \& 7)} & Data & \(5 \uparrow\) & & & \(0 \uparrow\) & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Select & \(0 \uparrow\) & & & \(0 \uparrow\) & & & \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 4) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & 54LS & 2.5 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{IOL}^{2}=4 \mathrm{~mA}\), & DM74 & & 0.25 & 0.4 & \\
    \hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current @ Max Input Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    V_{C C}=M a x, & V_{1}
    \end{aligned}=7 \mathrm{~V}, V_{1}=10 \mathrm{~V} .
    \]} & DM74 & & & \multirow[t]{2}{*}{0.1} & \multirow[t]{2}{*}{mA} \\
    \hline & & & 54LS & & & & \\
    \hline \({ }_{1} \mathrm{H}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{IIL} & Low Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & \multirow[t]{2}{*}{mA} \\
    \hline & Enable & \multicolumn{2}{|l|}{\(V_{C C}=5.0, V_{1}=0.4 \mathrm{~V}\)} & & & -0.8 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 5) }
    \end{aligned}
    \]} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}\) (Note 6)} & & 22 & 36 & mA \\
    \hline
    \end{tabular}

    Note 1: The symbols ( \(\downarrow, \uparrow\) ) indicate the edge of the clock pulse used for reference: \(\uparrow\) for rising edge, \(\downarrow\) for falling edge.
    Note 2: Setup and hold times are with reference to the enable input.
    Note 3: The select-to-enable setup time is the time betore the High-to-Low enable transition that the select must be stable so that the correct latch is selected and the others not affected.
    Note 4: All typlcals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 6: Icc is measured with all inputs at 4.5 V , and all outputs open.
    Note 7: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{\begin{tabular}{l}
    From (Input) \\
    To (Output)
    \end{tabular}} & \multicolumn{2}{|r|}{\multirow[t]{2}{*}{54 LS
    \(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)}} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{\[
    \begin{gathered}
    \text { DM74LS } \\
    \hline C_{L}=50 \mathrm{pF} \\
    R_{\mathrm{L}}=2 \mathrm{k} \Omega
    \end{gathered}
    \]}} & \multirow{3}{*}{Units} \\
    \hline & & & & & & & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Enable to Output & & 27 & & 38 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Enable to Output & & 24 & & 32 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Data to Output & & 30 & & 35 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Data to Output & & 20 & & 30 & ns \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & Select to Output & & 30 & & 41 & ns \\
    \hline \({ }_{\text {t }}^{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Select to Output & & 29 & & 38 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clear to Output & & 18 & & 36 & ns \\
    \hline
    \end{tabular}

    \section*{54LS260/DM74LS260 Dual 5-Input NOR Gate}

    \section*{General Description}

    This device contains two individual five input gates, each of which perform the logic NOR function.

    \section*{Connection Diagram}
    

    TL/F/9824-1
    Order Number 54LS260DMQB, 54LS260FMQB,
    54LS260LMQB, DM74LS260M or DM74LS260N See NS Package Number E20A, J14A, M14A, N14A or W14B

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    \begin{tabular}{lr}
    54 LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS260} & \multicolumn{3}{|c|}{DM74LS260} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{l}_{\mathrm{OH}}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
    \begin{aligned}
    & \text { Typ } \\
    & \text { (Note 1) }
    \end{aligned}
    \] & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & 54LS & 2.5 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & & 0.5 & \\
    \hline & & \(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=10 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & 54LS & & & -0.40 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & & & -0.36 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=\operatorname{Max}
    \] \\
    (Note 2)
    \end{tabular}} & 54LS & \(-20\) & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{IN}}=\mathrm{GND}\)} & & & 4.0 & mA \\
    \hline \(\mathrm{I}_{\mathrm{CCL}}\) & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\[
    V_{C C}=M a x, V_{I N}=\text { Open }
    \]} & & & 5.5 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Switching Characteristics
    \(\mathrm{V}_{\mathrm{CC}}=+5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Ouput Load)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \({ }_{\text {PPLH }}\) & Propagation Delay Time Low to High Level Output & & 10 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & & 12 & ns \\
    \hline
    \end{tabular}

    \section*{54LS266/DM74LS266 \\ Quad 2-Input Exclusive-NOR Gate with Open-Collector Outputs}

    \section*{General Description}

    This device contains four independent gates each of which performs the logic exclusive-OR function. Outputs are open collector.

    \section*{Connection Diagram}

    \section*{Dual-In-Line Package}
    

    TL/F/10182-1
    Order Number 54LS266DMQB, 54LS266FMQB, DM74LS266M or DM74LS266N See NS Package Number J14A, M14A, N14A or W14B

    Truth Table
    \begin{tabular}{|c|c|c|}
    \hline \multicolumn{2}{|c|}{ Inputs } & Outputs \\
    \hline A & B & Z \\
    \hline L & L & H \\
    L & H & L \\
    H & L & L \\
    H & H & H \\
    \hline
    \end{tabular}

    \footnotetext{
    \(H=H I G H\) Voltage Level
    L = LOW Voltage Level
    }

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    \begin{tabular}{lr} 
    54LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    Recommended Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS266} & \multicolumn{3}{|c|}{DM74LS266} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \({ }_{\mathrm{OH}}\) & High Level Output Current & & & -0.1 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & 54LS & 2.5 & & & V \\
    \hline & & & DM74 & 2.7 & & & \\
    \hline \multirow[t]{3}{*}{VOL} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{OL}}=\text { Max, } \\
    & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & & 0.5 & \\
    \hline & & \(\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=10 \mathrm{~V}\)} & & & 0.2 & mA \\
    \hline 1 IH & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 40 & \(\mu \mathrm{A}\) \\
    \hline \(1 / 2\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & \(-0.8\) & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=\operatorname{Max}
    \] \\
    (Note 2)
    \end{tabular}} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & \(-100\) & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & & 13 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\[
    \begin{aligned}
    & \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \\
    & \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}
    \end{aligned}
    \]} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \({ }_{\text {PLLH }}\) & Propagation Delay Time Low to High Level Output & & 23 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & & 23 & ns \\
    \hline
    \end{tabular}

    \footnotetext{
    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    }

    \section*{54LS273/DM74LS273 8-Bit Register with Clear}

    \section*{General Description}

    The 'LS273 is a high speed 8 -bit register, consisting of eight D-type flip-flops with a common Clock and an asynchronous active LOW Master Reset. This device is supplied in a \(20-\) pin package featuring 0.3 inch row spacing.

    \section*{Features}
    - Edge-triggered
    - 8-bit high speed register
    - Parallel in and out
    - Common clock and master reset

    Connection Diagram

    TL/F/9825-1
    Order Number 54LS273DMQB, 54LS273FMQB, 54LS273LMQB, DM74LS273M or DM74LS273N See NS Package Number E20A, J20A, M20B, N20A or W20A
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
    \hline CP & Clock Pulse Input (Active Rising Edge) \\
    \(\mathrm{DO}-\mathrm{D7}\) & Data Inputs \\
    \(\overline{M R}\) & \begin{tabular}{l} 
    Asynchronous Master Reset Input \\
    (Active LOW) \\
    Q0-Q7 \\
    Flip-Flop Outputs \\
    \hline
    \end{tabular} \\
    \hline
    \end{tabular}

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specifled devices are required, please contact the National Semiconductor Sales Office/Distributors for avallability and specifications.
    \begin{tabular}{lr} 
    Supply Voltage & 7 V \\
    Input Voltage & 7 V \\
    Operating Free Air Temperature Range & \\
    54 LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS273} & \multicolumn{3}{|c|}{DM74LS273} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW
    \[
    D_{n} \text { to } C P
    \] & \[
    \begin{aligned}
    & 15 \\
    & 15 \\
    & \hline
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 15 \\
    & 15 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Hold Time HIGH or LOW \(D_{n}\) to CP & \[
    \begin{aligned}
    & 5 \\
    & 5
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 5 \\
    & 5
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{w}(H) \\
    & t_{w}(L)
    \end{aligned}
    \] & CP Pulse Width HIGH or LOW & \[
    \begin{aligned}
    & 20 \\
    & 20
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 20 \\
    & 20
    \end{aligned}
    \] & & & ns \\
    \hline \(t_{w}(L)\) & \(\overline{M R}\) Pulse Width LOW & 20 & & & 20 & & & ns \\
    \hline \(t_{\text {rec }}\) & Recovery Time \(\overline{\mathrm{MR}}\) to CP & 15 & & & 15 & & & ns \\
    \hline
    \end{tabular}

    \section*{Electrical Characteristics}

    Over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \begin{tabular}{l}
    Typ \\
    (Note 1)
    \end{tabular} & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & 54LS & 2.5 & & & V \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\text {OL }}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O L}=\text { Max, } \\
    & V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=10 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline 1 IH & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & & 27 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{Switching Characteristics}
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{4}{*}{Symbol} & \multirow{4}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow{4}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{54LS}} & \multicolumn{2}{|c|}{DM74LS} & \\
    \hline & & & & \multicolumn{2}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(f_{\text {max }}\) & Maximum Clock Frequency & 30 & & 30 & & MHz \\
    \hline \[
    t_{P L H}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & Propagation Delay CP to \(Q_{n}\) & & \[
    \begin{aligned}
    & 32 \\
    & 32
    \end{aligned}
    \] & & \[
    \begin{array}{r}
    24 \\
    24 \\
    \hline
    \end{array}
    \] & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay \(\overline{M R}\) to \(Q_{n}\) & & 32 & & 27 & ns \\
    \hline
    \end{tabular}

    \section*{Functional Description}

    The 'LS273 is an 8-bit parallel register with a common Clock and common Master Reset. When the \(\overline{\text { MR }}\) input is LOW, the Q outputs are LOW, independent of the other inputs. Information meeting the setup and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-toHIGH transition of the clock input.

    \section*{Truth Table}
    \begin{tabular}{|c|c|c|c|}
    \hline \multicolumn{3}{|c|}{Inputs} & Outputs \(\mathbf{Q}_{\boldsymbol{n}}\) \\
    \hline L & X & X & L \\
    \hline H & \(\checkmark\) & H & H \\
    \hline H & \(\checkmark\) & L & L \\
    \hline
    \end{tabular}
    \[
    \begin{aligned}
    & H=\text { HIGH Voltage Level } \\
    & L=\text { LOW Voltage Level } \\
    & X=\text { Immaterial }
    \end{aligned}
    \]

    \section*{Logic Symbol}
    

    TL/F/9825-2
    \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Pin} 20 \\
    & \mathrm{GND}=\operatorname{Pin} 10
    \end{aligned}
    \]

    \section*{Logic Diagram}
    

    \section*{54LS279/DM54LS279/DM74LS279 \\ Quad \(\overline{\mathrm{S}}-\overline{\mathrm{R}}\) Latches}

    \section*{General Description}

    The 'LS279 consists of four individual and independent SetReset Latches with active low inputs. Two of the four latches have an additonal \(\overline{\mathrm{S}}\) input ANDed with the primary \(\overline{\mathrm{S}}\) input. A low on any \(\bar{S}\) input while the \(\overline{\mathrm{R}}\) input is high will be stored in the latch and appear on the corresponding \(Q\) output as a high. A low on the \(\overline{\mathrm{R}}\) input while the \(\overline{\mathrm{S}}\) input is high will clear the Q output to a low. Simultaneous transistion of the \(\overline{\mathrm{R}}\) and \(\overline{\mathrm{S}}\) inputs from low to high will cause the \(Q\) output
    to be indeterminate. Both inputs are voltage level triggered and are not affected by transition time of the input data.

    \section*{Features}
    - Alternate military/aerospace device (54LS279) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

    \section*{Connection Diagram}
    

    TL/F/6420-1
    Order Number 54LS279DMQB, 54LS279FMQB, 54LS279LMQB, DM54LS279J, DM74LS279M or DM74LS279N
    See NS Package Number E20A, J16A, M16A, N16E or W16A

    \section*{Function Table}
    \begin{tabular}{|c|c|c|}
    \hline \multicolumn{2}{|c|}{ Inputs } & Output \\
    \hline\(\overline{\mathbf{S}}(1)\) & \(\overline{\mathbf{R}}\) & \(\mathbf{Q}\) \\
    \hline L & L & \(\mathrm{H}^{*}\) \\
    L & H & H \\
    H & L & L \\
    \(H\) & \(H\) & \(\mathrm{Q}_{0}\) \\
    \hline
    \end{tabular}
    \(H=\) High Level
    \(\mathrm{L}=\) Low Level
    \(Q_{0}=\) The Level of \(\mathbf{Q}\) before the indicated input conditions were established.
    *This output level is pseudo stable; that is, it may not persist when the \(\overline{\mathrm{S}}\) and \(\overline{\mathrm{R}}\) inputs return to their inactive (high) level.
    Note 1: For latches with double \(\overline{\mathrm{S}}\) inputs:
    \(\mathrm{H}=\) both \(\overline{\mathrm{S}}\) inputs high
    \(\mathrm{L}=\) one or both \(\overline{\mathrm{S}}\) inputs low

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54LS279} & \multicolumn{3}{|c|}{DM74LS279} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{VOH} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.5 & & V \\
    \hline & & & DM74 & 2.7 & 3.5 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\
    & V_{I L}=\operatorname{Max}, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{IOL}^{\text {a }}\) 4 mA, & DM74 & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=0.4 V\)} & & & -0.4 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\) (Note 3)} & & 3.8 & 7 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: \(I_{C C}\) is measured with all \(\overline{\mathrm{A}}\) inputs grounded, all \(\overline{\mathrm{S}}\) inputs at 4.5 V and all outputs open.

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{\begin{tabular}{l}
    From (Input) \\
    To (Output)
    \end{tabular}} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    \bar{S} \text { to } \\
    \mathrm{Q}
    \end{gathered}
    \] & & 22 & & 25 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \(\overline{\mathrm{S}}\) to
    Q & & 15 & & 23 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \(\overline{\mathrm{R}}\) to Q & & 27 & & 33 & ns \\
    \hline
    \end{tabular}

    \section*{54LS283/DM54LS283/DM74LS283 \\ 4-Bit Binary Adders with Fast Carry}

    \section*{General Description}

    These full adders perform the addition of two 4-bit binary numbers. The sum ( \(\Sigma\) ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial lookahead performance at the economy and reduced package count of a ripple-carry implementation.

    The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

    \section*{Features}
    - Full-carry look-ahead across the four bits
    - Systems achieve partial look-ahead performance with the economy of ripple carry
    - Typical add times

    Two 8-bit words 25 ns
    Two 16-bit words 45 ns
    - Typical power dissipation per 4-bit adder 95 mW
    - Alternate Military/Aerospace device (54LS283) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

    \section*{Connection Diagram}

    \section*{Dual-In-Line Package}
    

    TL/F/6421-1
    Order Number 54LS283DMQB, 54LS283FMQB, 54LS283LMQB, DM54LS283J, DM54LS283W, DM74LS283M or DM74LS283N See NS Package Number E20A, J16A, M16A, N16E or W16A
    

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54LS283} & \multicolumn{3}{|c|}{DM74LS283} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current @ Max Input Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{\mathrm{I}}=7 \mathrm{~V}
    \end{aligned}
    \]} & A, B & & & 0.2 & \multirow[t]{2}{*}{mA} \\
    \hline & & & CO & & & 0.1 & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{I}_{\mathrm{H}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=2.7 V
    \end{aligned}
    \]} & A, B & & & 40 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & CO & & & 20 & \\
    \hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{I}=0.4 V
    \end{aligned}
    \]} & A, B & & & -0.8 & \multirow[t]{2}{*}{mA} \\
    \hline & & & CO & & & -0.4 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & DM54 & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC1 & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\operatorname{Max}\) (Note 3)} & & 19 & 34 & mA \\
    \hline ICC2 & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\) (Note 4)} & & 22 & 39 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: \(\mathrm{I}_{\mathrm{CC} 1}\) is measured with all outputs open, all B inputs low and all other inputs at 4.5 V , or all inputs at 4.5 V .
    Note 4: ICC2 is measured with all outputs open and all inputs grounded.

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \({ }_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    \text { C0 to } \\
    \Sigma 1, \Sigma 2 \\
    \hline
    \end{gathered}
    \] & & 24 & & 28 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \text { C0 to } \\
    \Sigma 1, \Sigma 2 \\
    \hline
    \end{gathered}
    \] & & 24 & & 30 & ns \\
    \hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    \mathrm{CO} \text { to } \\
    \Sigma 3
    \end{gathered}
    \] & & 24 & & 28 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \text { CO to } \\
    \Sigma 3 \\
    \hline
    \end{gathered}
    \] & & 24 & & 30 & ns \\
    \hline \({ }_{\text {tpLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    \mathrm{CO} \text { to } \\
    \Sigma 4 \\
    \hline
    \end{gathered}
    \] & & 24 & & 28 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \hline \mathrm{CO} \text { to } \\
    \mathrm{\Sigma 4} \\
    \hline
    \end{gathered}
    \] & & 24 & & 30 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \(\mathrm{A}_{\mathrm{i}}\) or \(\mathrm{B}_{\mathrm{i}}\) to \(\Sigma_{i}\) & & 24 & & 28 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \(\mathrm{A}_{\mathrm{i}}\) or \(\mathrm{B}_{\mathrm{i}}\) to \(\Sigma_{i}\) & & 24 & & 30 & ns \\
    \hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    \mathrm{C} 0 \text { to } \\
    \mathrm{C} 4 \\
    \hline
    \end{gathered}
    \] & & 17 & & 24 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \mathrm{C} 0 \text { to } \\
    \mathrm{C} 4 \\
    \hline
    \end{gathered}
    \] & & 17 & & 25 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \(\mathrm{A}_{\mathrm{i}}\) or \(\mathrm{B}_{\mathrm{i}}\) to C 4 & & 17 & & 24 & ns \\
    \hline tPHL & Propagation Delay Time High to Low Level Output & \(\mathrm{A}_{\mathrm{i}}\) or \(\mathrm{B}_{\mathrm{i}}\) to C 4 & & 17 & & 26 & ns \\
    \hline
    \end{tabular}

    Function Table
    (

    TL/F/6421-3
    \(H=\) High Level, \(L=\) Low Level
    Note: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs \(\Sigma 1\) and \(\Sigma 2\) and the value of the internal carry C2. The values at \(\mathrm{C} 2, \mathrm{~A} 3, \mathrm{~B} 3, \mathrm{~A} 4\), and B4 are then used to determine outputs \(\Sigma 3, \Sigma 4\), and \(\mathrm{C4}\).

    \section*{Logic Diagram}
    

    TL/F/6421-2

    \section*{DM74LS290 4-Bit Decade Counter}

    \section*{General Description}

    The 'LS290 counter is electrically and functionally identical to the 'LS90. Only the arrangement of the terminals has been changed for the 'LS290.
    Each of these monolithic counters contains four masterslave flip-flops and additional gating to provide a divide-bytwo counter and a three-stage binary counter for which the count cycle length is divide-by-five.
    This counter has a gated zero reset and gated set-to-nine inputs for use in BCD nine's complement applications.
    To use the maximum count length (decade) of this counter, the \(B\) input is connected to the \(Q_{A}\) output. The input count pulses are applied to input A and the outputs are as de-
    scribed in the appropriate function table. A symmetrical di-vide-by-ten count can be obtained from the 'LS290 counter by connecting the \(Q_{D}\) output to the \(A\) input and applying the input count to the \(B\) input which gives a divide-by-ten square wave at output \(Q_{A}\).

    \section*{Features}
    - GND and \(V_{C C}\) on Corner Pins (Pins 7 and 14 respectively)
    ■ Typical power dissipation 45 mW
    - Count frequency 42 MHz

    \section*{Connection Diagram}
    

    TL/F/6422-1
    Order Number DM74LS290M or DM74LS290N See NS Package Number M14A or N14A
    

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM74LS290} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & \\
    \hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{\text {l }}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 8 & mA \\
    \hline \multirow[t]{2}{*}{\(\mathrm{f}_{\mathrm{CLK}}\)} & \multirow[t]{2}{*}{Clock Freq. (Note 1)} & \(A\) to \(Q_{A}\) & 0 & & 32 & \multirow[t]{2}{*}{MHz} \\
    \hline & & \(B\) to \(Q_{B}\) & 0 & & 16 & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{f}_{\mathrm{CLK}}\)} & \multirow[t]{2}{*}{Clock Freq. (Note 2)} & A to \(Q_{A}\) & 0 & & 20 & \multirow[t]{2}{*}{MHz} \\
    \hline & & \(B\) to \(Q_{B}\) & 0 & & 10 & \\
    \hline \multirow[t]{3}{*}{tw} & \multirow[t]{3}{*}{Pulse Width (Note 6)} & A & 15 & & & \multirow{3}{*}{ns} \\
    \hline & & B & 30 & & & \\
    \hline & & Reset & 15 & & & \\
    \hline \(t_{\text {REL }}\) & \multicolumn{2}{|l|}{Reset Release Time (Note 6)} & 25 & & & ns \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 3) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \] & & 2.7 & 3.4 & & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\text {OL }}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \[
    \begin{aligned}
    & V_{C C}=M i n, I_{O L}=M a x \\
    & V_{\mathrm{IL}}=\operatorname{Max}, V_{I H}=M i n
    \end{aligned}
    \] & & & 0.35 & 0.5 & \multirow[t]{2}{*}{V} \\
    \hline & & \(\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & & & 0.25 & 0.4 & \\
    \hline \multirow[t]{3}{*}{1} & \multirow[t]{3}{*}{Input Current @ Max Input Voltage} & \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}\)} & Reset & & & 0.1 & \multirow{3}{*}{mA} \\
    \hline & & & A & & & 0.2 & \\
    \hline & & & B & & & 0.4 & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{IIH}_{\mathrm{H}}\)} & \multirow[t]{3}{*}{High Level Input Current} & \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & Reset & & & 20 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & A & & & 40 & \\
    \hline & & & B & & & 80 & \\
    \hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=0.4 V
    \end{aligned}
    \]} & Reset & & & -0.4 & \multirow{3}{*}{mA} \\
    \hline & & & A & & & -2.4 & \\
    \hline & & & B & & & -3.2 & \\
    \hline los & Short Circuit Output Current & \[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 4) }
    \end{aligned}
    \] & & -20 & & -100 & mA \\
    \hline Icc & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\) (Note 5)} & & 9 & 15 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[b]{3}{*}{\begin{tabular}{l}
    From (Input) \\
    To (Output)
    \end{tabular}} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \multirow[t]{2}{*}{\(f_{\text {MAX }}\)} & \multirow[t]{2}{*}{Maximum Clock Frequency} & \(A\) to \(Q_{A}\) & 32 & & 20 & & \multirow[t]{2}{*}{MHz} \\
    \hline & & \(B\) to \(Q_{B}\) & 16 & & 10 & & \\
    \hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & \(A\) to \(Q_{A}\) & & 16 & & 23 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & \(A\) to \(Q_{A}\) & & 18 & & 30 & ns \\
    \hline \({ }_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output & \(A\) to \(Q_{D}\) & & 48 & & 60 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{aligned}
    & \text { A to } \\
    & Q_{D}
    \end{aligned}
    \] & & 50 & & 68 & ns \\
    \hline \({ }_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{aligned}
    & \text { B to } \\
    & Q_{B}
    \end{aligned}
    \] & & 16 & & 23 & ns \\
    \hline tpHL & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \mathrm{B} \text { to } \\
    \mathrm{Q}_{\mathrm{B}}
    \end{gathered}
    \] & & 21 & & 35 & ns \\
    \hline \(\mathrm{t}_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{aligned}
    & \text { B to } \\
    & Q_{C} \\
    & \hline
    \end{aligned}
    \] & & 32 & & 48 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{aligned}
    & \mathrm{B} \text { to } \\
    & \mathrm{Q}_{\mathrm{C}}
    \end{aligned}
    \] & & 35 & & 53 & ns \\
    \hline \({ }_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output & \(B\) to \(Q_{D}\) & & 32 & & 48 & ns \\
    \hline tpHL & Propagation Delay Time High to Low Level Output & \[
    \begin{aligned}
    & B \text { to } \\
    & Q_{D} \\
    & \hline
    \end{aligned}
    \] & & 35 & & 53 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & SET-9 to
    \[
    Q_{A}, Q_{D}
    \] & & 30 & & 38 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & SET-9 to
    \[
    \mathrm{Q}_{\mathrm{B}}, \mathrm{Q}_{\mathrm{C}}
    \] & & 40 & & 53 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & SET-0 to Any Q & & 40 & & 53 & ns \\
    \hline
    \end{tabular}

    Note 1: \(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 2: \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 3: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 5: Icc is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5 V and all other inputs grounded.
    Note 6: \(T_{A}=25^{\circ} \mathrm{C}\) and \(V_{C C} 5 V\).

    Function Tables
    BCD Count Sequence
    (See Note A)
    \begin{tabular}{|c|cccc|}
    \hline \multirow{2}{*}{ Count } & \multicolumn{4}{|c|}{ Output } \\
    \cline { 2 - 5 } & Q \(_{\text {D }}\) & Q \(_{\text {C }}\) & Q \(_{\text {B }}\) & \(\mathbf{Q}_{\mathbf{A}}\) \\
    \hline 0 & \(L\) & \(L\) & \(L\) & \(L\) \\
    1 & \(L\) & \(L\) & \(L\) & \(H\) \\
    2 & \(L\) & \(L\) & \(H\) & \(L\) \\
    3 & \(L\) & \(L\) & \(H\) & \(H\) \\
    4 & \(L\) & \(H\) & \(L\) & \(L\) \\
    5 & \(L\) & \(H\) & \(L\) & \(H\) \\
    6 & \(L\) & \(H\) & \(H\) & \(L\) \\
    7 & \(L\) & \(H\) & \(H\) & \(H\) \\
    8 & \(H\) & \(L\) & \(L\) & \(L\) \\
    9 & \(H\) & \(L\) & \(L\) & \(H\) \\
    \hline
    \end{tabular}

    Note \(A\) : Output \(Q_{A}\) is connected to input \(B\) for BCD count
    \(H=\) High Logic Level
    L = Low Logic Level
    \(X=\) Either Low or High Logic Level

    Bi-Quinary (5-2)
    (See Note B)
    \begin{tabular}{|c|cccc|}
    \hline \multirow{2}{*}{ Count } & \multicolumn{4}{|c|}{ Output } \\
    \cline { 2 - 5 } & \(\mathbf{Q}_{\mathbf{A}}\) & \(\mathbf{Q}_{\mathbf{B}}\) & \(\mathbf{Q}_{\mathbf{C}}\) & \(\mathbf{Q}_{\mathbf{D}}\) \\
    \hline 0 & L & L & L & L \\
    1 & L & L & L & H \\
    2 & L & L & H & L \\
    3 & L & L & H & H \\
    4 & L & H & L & L \\
    5 & H & L & L & L \\
    6 & H & L & L & H \\
    7 & H & L & H & L \\
    8 & H & L & H & H \\
    9 & H & H & L & L \\
    \hline
    \end{tabular}

    Note B: Output \(Q_{D}\) is connected to input \(A\) for biquinary count.

    \section*{Logic Diagram}
    

    Reset/Count Truth Table
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{4}{|c|}{Reset Inputs} & \multicolumn{4}{|c|}{Outputs} \\
    \hline R0(1) & RO(2) & R9(1) & R9(2) & \(\mathbf{Q}_{\mathbf{D}}\) & \(Q_{c}\) & \(\mathbf{Q}_{B}\) & \(Q_{\text {A }}\) \\
    \hline H & H & L & X & L & L & L & L \\
    \hline H & H & X & L & L & L & L & L \\
    \hline X & X & H & H & H & L & L & H \\
    \hline X & L & X & L & & COU & NT & \\
    \hline L & X & L & X & & COU & NT & \\
    \hline L & X & X & L & & COU & NT & \\
    \hline X & L & L & X & & COU & NT & \\
    \hline
    \end{tabular}

    \section*{DM74LS293 4-Bit Binary Counter}

    \section*{General Description}

    The 'LS293 counter is electrically and functionally identical to the 'LS93. Only the arrangement of the terminals has been changed for the 'LS293.
    Each of these monolithic counters contains four masterslave flip-flops and additional gating to provide a divide-bytwo counter and a three-stage binary counter for which the count cycle length is divide-by-eight.
    All of these counters have a gated zero reset.

    To use the maximum count length (four-bit binary) of these counters, the \(B\) input is connected to the \(Q_{A}\) output. The input count pulses are applied to input \(A\) and the outputs are as described in the appropriate function table.

    \section*{Features}
    - GND and \(V_{C C}\) on Corner Pins (Pins 7 and 14 respectively)
    - Typical power dissipation 45 mW
    - Count frequency 42 MHz

    \section*{Connection Diagram}
    
    

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM74LS293} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & \\
    \hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{\text {l }}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 8 & mA \\
    \hline \multirow[t]{2}{*}{fCLK} & \multirow[t]{2}{*}{Clock Frequency (Note 1)} & \(A\) to \(Q_{A}\) & 0 & & 32 & \multirow[t]{2}{*}{MHz} \\
    \hline & & \(B\) to \(Q_{B}\) & 0 & & 16 & \\
    \hline \multirow[t]{2}{*}{\({ }_{\text {f CLK }}\)} & \multirow[t]{2}{*}{Clock Frequency (Note 2)} & \(A\) to \(Q_{A}\) & 0 & & 20 & \multirow[t]{2}{*}{MHz} \\
    \hline & & \(B\) to \(Q_{B}\) & 0 & & 10 & \\
    \hline \multirow[t]{3}{*}{tw} & \multirow[t]{3}{*}{Pulse Width (Note 6)} & A & 15 & & & \multirow{3}{*}{ns} \\
    \hline & & B & 30 & & & \\
    \hline & & Reset & 15 & & & \\
    \hline \(t_{\text {REL }}\) & \multicolumn{2}{|l|}{Reset Release Time (Note 6)} & 25 & & & ns \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 3) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 2.7 & 3.4 & & V \\
    \hline \multirow[t]{2}{*}{V \({ }_{\text {OL }}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & & 0.35 & 0.5 & V \\
    \hline & & \multicolumn{2}{|l|}{\(\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\)} & & 0.25 & 0.4 & \\
    \hline \multirow[t]{3}{*}{1} & \multirow[t]{3}{*}{Input Current @ Max Input Voltage} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{I}=7 V
    \end{aligned}
    \]} & Reset & & & 0.1 & \multirow{3}{*}{mA} \\
    \hline & & & A & & & 0.2 & \\
    \hline & & & B & & & 0.2 & \\
    \hline \multirow[t]{3}{*}{\({ }_{1 / H}\)} & \multirow[t]{3}{*}{High Level Input Current} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=2.7 V
    \end{aligned}
    \]} & Reset & & & 20 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & A & & & 40 & \\
    \hline & & & B & & & 40 & \\
    \hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=0.4 V
    \end{aligned}
    \]} & Reset & & & -0.4 & \multirow{3}{*}{mA} \\
    \hline & & & A & & & -2.4 & \\
    \hline & & & B & & & -1.6 & \\
    \hline los & Short Circuit Output Current & \[
    \begin{aligned}
    & V_{C C}=\text { Max } \\
    & \text { (Note 4) }
    \end{aligned}
    \] & & -20 & & -100 & mA \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\) Max (Note 5)} & & 9 & 15 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{\begin{tabular}{l}
    From (Input) \\
    To (Output)
    \end{tabular}} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \multirow[t]{2}{*}{\(t_{\text {max }}\)} & \multirow[t]{2}{*}{Maximum Clock Frequency} & \(A\) to \(Q_{A}\) & 32 & & 20 & & \multirow[t]{2}{*}{MHz} \\
    \hline & & \(B\) to \(Q_{B}\) & 16 & & 10 & & \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & A to \(Q_{A}\) & & 16 & & 23 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & A to \(Q_{A}\) & & 18 & & 30 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \(A\) to \(Q_{D}\) & & 70 & & 87 & ns \\
    \hline tPHL & Propagation Delay Time High to Low Level Output & A to \(Q_{D}\) & & 70 & & 93 & ns \\
    \hline \(\mathrm{tplH}^{\text {L }}\) & Propagation Delay Time Low to High Level Output & \(B\) to \(Q_{B}\) & & 16 & & 23 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \(B\) to \(Q_{B}\) & & 21 & & 35 & ns \\
    \hline \(\mathrm{tpLH}^{\text {l }}\) & Propagation Delay Time Low to High Level Output & \(B\) to \(Q_{C}\) & & 32 & & 48 & ns \\
    \hline tpHL & Propagation Delay Time High to Low Level Output & \(B\) to \(Q_{C}\) & & 35 & & 53 & ns \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & \(B\) to \(Q_{D}\) & & 51 & & 71 & ns \\
    \hline tPHL & Propagation Delay Time High to Low Level Output & \(B\) to \(Q_{D}\) & & 51 & & 71 & ns \\
    \hline tpHL & Propagation Delay Time High to Low Level Output & SET-0 to Any Q & & 40 & & 53 & ns \\
    \hline
    \end{tabular}

    Note 1: \(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 2: \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 3: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 5: ICC is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5 V and all other inputs grounded.
    Note 6: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

    Function Tables
    Count Sequence (See Note C)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Count} & \multicolumn{4}{|c|}{Outputs} \\
    \hline & \(Q_{D}\) & \(Q_{C}\) & \(Q_{B}\) & \(Q_{\text {A }}\) \\
    \hline 0 & L & L & L & L \\
    \hline 1 & L & L & L & H \\
    \hline 2 & L & L & H & L \\
    \hline 3 & L & L & H & H \\
    \hline 4 & L & H & L & L \\
    \hline 5 & L & H & L & H \\
    \hline 6 & L & H & H & L \\
    \hline 7 & L & H & H & H \\
    \hline 8 & H & L & L & L \\
    \hline 9 & H & L & L & H \\
    \hline 10 & H & L & H & L \\
    \hline 11 & H & L & H & H \\
    \hline 12 & H & H & L & L \\
    \hline 13 & H & H & L & H \\
    \hline 14 & H & H & H & L \\
    \hline 15 & H & H & H & H \\
    \hline
    \end{tabular}

    Reset/Count Truth Table
    \begin{tabular}{|cc|cccc|}
    \hline \multicolumn{2}{|c|}{ Reset Inputs } & \multicolumn{4}{|c|}{ Outputs } \\
    \hline RO(1) & RO(2) & \(\mathbf{Q}_{\mathbf{D}}\) & \(\mathbf{Q}_{\mathbf{C}}\) & \(\mathbf{Q}_{\mathbf{B}}\) & \(\mathbf{Q}_{\mathbf{A}}\) \\
    \hline H & H & L & L & L & L \\
    L & X & & COUNT & \\
    X & L & & COUNT & \\
    \hline
    \end{tabular}
    \(H=\) High Level, \(L=\) Low Level, \(X=\) Don't Care.

    Note C: Output \(Q_{A}\) is connected to input \(B\).

    \section*{Logic Diagram}
    

    National
    Semiconductor

    \section*{54LS295A/DM74LS295A 4-Bit Shift Register with TRI-STATE \({ }^{\circledR}\) Outputs}

    \section*{General Description}

    The 'LS295A is a 4-bit shift register with serial and parallel synchronous operating modes, and independent TRISTATE output buffers. The Parallel Enable input (PE) controls the shift-right or parallel load operation. All data transfers and shifting occur synchronous with the HIGH-to-LOW clock transition.

    The TRI-STATE output buffers are controlled by an active HIGH Output Enable input (OE). Disabling the output buffers does not affect the shifting or loading of input data, but it does inhibit serial expansion. The device is fabricated with the Schottky barrier diode process for high speed.

    \section*{Features}
    - Fully synchronous serial or parallel data transfers
    - Negative edge-triggered clock input
    - Parallel enable mode control input
    - TRI-STATE bussable output buffers

    \section*{Connection Diagram}

    Dual-In-Line Package
    

    TL/F/10183-1
    Order Number 54LS295ADMQB, 54LS295AFMQB, DM74LS295AM or DM74LS295AN
    See NS Package Number J14A, M14A, N14A or W14B

    Logic Symbol
    

    TL/F/10183-2
    \(V_{C C}=\operatorname{Pin} 14\)
    GND \(=\operatorname{Pin} 7\)
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
    \hline PE & Parallel Enable Input (Active HIGH) \\
    DS & Serial Data Input \\
    PO-P3 & Parallel Data Inputs \\
    OE & TRI-STATE Output Enable Input (Active HIGH) \\
    \(\overline{C P}\) & Clock Pulse Input (Active Falling Edge) \\
    OO-O3 & TRI-STATE Outputs \\
    \hline
    \end{tabular}

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avallability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    ```

    54LS
    DM74LS
    Storage Temperature Range

    ```

    Recommended Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS295A} & \multicolumn{3}{|c|}{DM74LS295A} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Current & & & -1.0 & & & -2.6 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & t_{s}(H) \\
    & t_{s}(L)
    \end{aligned}
    \] & Setup Time HIGH or LOW
    \[
    D_{S}, P_{n} \text { to } \overline{C P}
    \] & \[
    \begin{aligned}
    & 20 \\
    & 20
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 20 \\
    & 20
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L) \\
    & \hline
    \end{aligned}
    \] & Hold Time HIGH or LOW
    \[
    D_{S}, P_{n} \text { to } \overline{C P}
    \] & \[
    \begin{aligned}
    & 10 \\
    & 10 \\
    & \hline
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 10 \\
    & 10
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L})
    \end{aligned}
    \] & Setup Time HIGH or LOW PE to \(\overline{C P}\) & \[
    \begin{aligned}
    & 20 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 20 \\
    & 20
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L)
    \end{aligned}
    \] & Hold Time HIGH or LOW PE to \(\overline{\mathrm{CP}}\) & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & ns \\
    \hline \(\mathrm{t}_{\mathrm{w}}(\mathrm{L})\) & \(\overline{\text { CP Pulse Width LOW }}\) & 20 & & & 20 & & & ns \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & 54LS & 2.4 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.4 & & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & & 0.5 & \\
    \hline & & \(\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & & 0.4 & \\
    \hline 11 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=10 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \({ }_{1 / 4}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\) Max, \(V_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline ILL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline \multirow[t]{2}{*}{ICCH} & Supply Current Outputs ON & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M a x, P_{n}=G N D \\
    & P E, D S, O E=4.5 V, \overline{C P}=乙
    \end{aligned}
    \]} & & & 23 & mA \\
    \hline & Outputs OFF & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M a x, P E, D S=4.5 V \\
    & P_{n}, O E, \overline{C P}=G N D
    \end{aligned}
    \]} & & & 25 & mA \\
    \hline
    \end{tabular}

    Electrical Characteristics (Continued)
    over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{l|l|l|c|c|c|c}
    \hline Symbol & \multicolumn{1}{|c|}{ Parameter } & \multicolumn{1}{|c|}{ Conditions } & \multicolumn{1}{c|}{\begin{tabular}{c} 
    Typ \\
    (Note 1)
    \end{tabular}} & Max & Units \\
    \hline IOZH & \begin{tabular}{l} 
    Off-State Output Current \\
    with High Level Output \\
    Voltage Applied
    \end{tabular} & \begin{tabular}{l}
    \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{O}}=2.7 \mathrm{~V}\) \\
    \(\mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}\)
    \end{tabular} & & 20 & \(\mu \mathrm{~A}\) \\
    \hline IOZL & \begin{tabular}{l} 
    Off-State Output Current \\
    with Low Level Output \\
    Voltage Applied
    \end{tabular} & \begin{tabular}{l}
    \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}\) \\
    \(\mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}\)
    \end{tabular} & & & -20 & \(\mu \mathrm{~A}\) \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{Switching Characteristics}
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 3 for waveforms and load configurations)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{2}{|c|}{54/74LS} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|r|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \\
    \hline & & Min & Max & \\
    \hline \(f_{\text {max }}\) & Maximum Shift Frequency & 30 & & MHz \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(t_{\text {PHL }}\)
    \end{tabular} & Propagation Delay \(\overline{\mathrm{CP}}\) to \(\mathrm{Q}_{\mathrm{n}}\) & & \[
    \begin{aligned}
    & 30 \\
    & 26 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PZH}} \\
    & \mathrm{t}_{\mathrm{PZL}} \\
    & \hline
    \end{aligned}
    \] & Output Enable Time & & \[
    \begin{aligned}
    & 18 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PHZ}} \\
    & \mathrm{t}_{\mathrm{PLZ}}
    \end{aligned}
    \] & Output Disable Time & & \[
    \begin{aligned}
    & 24 \\
    & 20
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}

    \section*{Functional Description}

    This device is a 4-bit shift register with serial and parallel synchronous operating modes. It has a Serial Data ( \(D_{\mathrm{S}}\) ) and four Parallel Data (P0-P3) inputs and four parallel TRISTATE output buffers ( \(\mathrm{O} 0-\mathrm{O} 3\) ). When the Parallel Enable (PE) input is HIGH, data is transferred from the Parallel Data inputs (PO-P3) into the register synchronous with the HIGH-to-LOW transition of the Clock ( \(\overline{\mathrm{CP}}\) ). When the PE is LOW, a HIGH-to-LOW transition on the clock transfers the serial data on the \(\mathrm{D}_{\mathrm{S}}\) input to the register Q0, and shifts data from Q0 to Q1, Q1 to Q2 and Q2 to Q3. The input data and parallel enable are fully edge-triggered and must be stable only one setup time before the HIGH-to-LOW clock transition.

    The TRI-STATE output buffers are controlled by an active HIGH Output Enable input (OE). When the OE is HIGH, the four register outputs appear at the \(\mathrm{O} 0-\mathrm{O} 3\) outputs. When OE is LOW, the outputs are forced to a high impedance OFF state. The TRI-STATE output buffers are completely independent of the register operation, i.e., the input transitions on the OE input do not affect the serial or parallel data transfers of the register. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRISTATE devices whose outputs are tied together are designed so there is no overlap.
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{9}{|c|}{Mode Select Table} \\
    \hline \multirow[t]{2}{*}{Operating Mode} & \multicolumn{4}{|c|}{Inputs} & \multicolumn{4}{|c|}{Outputs} \\
    \hline & PE & \(\overline{\text { CP }}\) & \(\mathrm{D}_{\mathrm{S}}\) & \(\mathrm{P}_{\mathrm{n}}\) & Q0 & Q1 & Q2 & Q3 \\
    \hline Shift Right & \[
    1
    \] & \[
    2
    \] & \[
    \begin{aligned}
    & \mathrm{l} \\
    & \mathrm{~h}
    \end{aligned}
    \] & \[
    \begin{aligned}
    & \mathrm{X} \\
    & \mathrm{X}
    \end{aligned}
    \] & \[
    \begin{aligned}
    & L \\
    & H
    \end{aligned}
    \] & \[
    \begin{aligned}
    & \mathrm{q}_{0} \\
    & \mathrm{q}_{0} \\
    & \hline
    \end{aligned}
    \] & \[
    \begin{aligned}
    & \mathrm{q}_{1} \\
    & \mathrm{q}_{1}
    \end{aligned}
    \] & \[
    \begin{aligned}
    & \mathrm{q}_{2} \\
    & \mathrm{q}_{2} \\
    & \hline
    \end{aligned}
    \] \\
    \hline Parallel Load & h & \(\checkmark\) & X & \(p_{n}\) & p0 & p1 & p2 & p3 \\
    \hline
    \end{tabular}
    *The indicated data appears at the Q outputs when OE is HIGH. When OE is LOW, the indicated data is loaded into the register, but the outputs are all forced to the high impedance OFF state.
    \(\mathrm{p}_{\mathrm{n}}\left(\mathrm{q}_{\mathrm{n}}\right)=\) Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.
    \(1=\) LOW Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.
    \(h=\) HIGH Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.
    \(H=\) HIGH Voltage Level
    \(L=\) LOW Voltage Level
    \(X=\) Immaterial

    \section*{Logic Diagram}
    

    \section*{54LS298/DM74LS298 Quad 2-Port Register Multiplexer with Storage}

    \section*{General Description}

    The 'LS298 is a quad 2-port register. It is the logical equivalent of a quad 2 -input multiplexer followed by a quad 4 -bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register synchronous with the HIGH-to-LOW transition of the Clock input.

    \section*{Features}
    - Select from two data sources
    - Fully edge-triggered operation
    - Typical power dissipation of 65 mW

    \section*{Logic Symbol}
    

    TL/F/9826-2
    \[
    V_{C C}=\operatorname{Pin} 16
    \]
    \[
    \text { GND }=\operatorname{Pin} 8
    \]

    Order Number 54LS298DMQB, 54LS298FMQB,
    DM74LS298M or DM74LS298N
    See NS Package Number J16A, N16E or W16A
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{c|}{ Description } \\
    \hline S & Common Select Inputs \\
    \(\overline{\mathrm{CP}}\) & Clock Pulse Input (Active Falling Edge) \\
    \(10_{a}, 10_{d}\) & Source 0 Data Inputs \\
    \(11_{a}, 11_{d}\) & Source 1 Data Inputs \\
    \(\mathrm{Q}_{\mathrm{a}}, \mathrm{Q}_{\mathrm{d}}\) & Flip-Flip Outputs \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|}
    \hline \multicolumn{2}{|l|}{Absolute Maximum Ratings (Note)} \\
    \hline \multicolumn{2}{|l|}{\multirow[t]{2}{*}{please contact the National Semiconductor Sales Office/Distributors for availability and specifications.}} \\
    \hline & \\
    \hline Supply Voltage & 7 \\
    \hline Input Voltage & 10 V \\
    \hline Operating Free Air Temperature Range & \\
    \hline 54LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    \hline DM74LS & \(0^{\circ} \mathrm{C}\) to \\
    \hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to +15 \\
    \hline
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    Recommended Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS298} & \multicolumn{3}{|c|}{DM74LS298} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\text {c }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{2}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline 1 OL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L})
    \end{aligned}
    \] & Setup Time HIGH or LOW S to \(\overline{\mathrm{CP}}\) & \[
    \begin{aligned}
    & 25 \\
    & 25
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 25 \\
    & 25
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(\mathrm{H}) \\
    & t_{\mathrm{h}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Hold Time HIGH or LOW \(S\) to \(\overline{\mathrm{CP}}\) & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L})
    \end{aligned}
    \] & Setup Time HIGH or LOW \(10_{x}\) or \(11_{x}\) to \(\overline{C P}\) & \[
    \begin{aligned}
    & 15 \\
    & 15
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 15 \\
    & 15
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(\mathrm{~L})
    \end{aligned}
    \] & Hold Time HIGH or LOW \(10 x\) or \(11_{x}\) to \(\overline{C P}\) & \[
    \begin{aligned}
    & 5.0 \\
    & 5.0 \\
    & \hline
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 5.0 \\
    & 5.0 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{w}(H) \\
    & t_{w}(L) \\
    & \hline
    \end{aligned}
    \] & \(\overline{\text { CP Pulse Width HIGH or LOW }}\) & \[
    \begin{aligned}
    & 20 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 20 \\
    & 20
    \end{aligned}
    \] & & & ns \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O H}=M a x \\
    & V_{I L}=M a x
    \end{aligned}
    \]} & 54LS & 2.5 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=10 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\) Max, \(\mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\[
    V_{C C}=\operatorname{Max}, V_{1}=0.4 V
    \]} & & & -0.4 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline Icc & Supply Current & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, 10_{n}, 11_{n}, \\
    & S=\operatorname{GND}, \overline{C P}=
    \end{aligned}
    \]} & & & 21 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{Switching Characteristics}
    at \(\mathrm{V}_{\mathrm{CC}}=+5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for test waveforms and output load)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output \(\overline{C P}\) to \(Q_{n}\) & & 25 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output \(\overline{\mathrm{CP}}\) to \(\mathrm{Q}_{\mathrm{n}}\) & & 25 & ns \\
    \hline
    \end{tabular}

    \section*{Functional Description}

    This device is a high speed quad 2-port register. It selects four bits of data from two sources (ports) under the control of a Common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the Clock input ( \(\overline{\mathrm{CP}}\) ). The 4-bit output register is fully edge-triggered. The Data inputs ( \(I_{\mathrm{nx}}\) ) and Select input ( S ) need be stable only one setup time prior to the HIGH-to-LOW transition of the clock for predictable operation.

    \section*{Truth Table}
    \begin{tabular}{|ccc|c|}
    \hline \multicolumn{3}{c|}{ Inputs } & Output \\
    \hline \(\mathbf{S}\) & \(\mathbf{1 0}\) & \(\mathbf{1 1 _ { \mathbf { x } }}\) & \(\mathbf{Q}_{\mathbf{x}}\) \\
    \hline I & I & X & L \\
    I & h & X & H \\
    h & X & I & L \\
    h & X & h & H \\
    \hline
    \end{tabular}

    I = LOW Voltage Level one setup time prior to the HIGH-to-LOW clock transition.
    \(h=\) HIGH Voltage Level one setup time prior to the HIGH-to-LOW clock transition.
    \(H=\) HIGH Voltage Level
    L = LOW Voltage Level
    \(X=\) Immaterial

    \section*{Logic Diagram}
    

    \section*{54LS299/DM74LS299}

    8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

    \section*{General Description}

    The 'LS299 is an 8-bit universal shift/storage register with TRI-STATE \({ }^{\oplus}\) outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q0 and Q7 to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

    Features
    - Common I/O for reduced pin count
    - Four operation modes: shift left, shift right, load and store
    - Separate shift right serial input and shift left serial input for easy cascading
    - TRI-STATE outputs for bus oriented applications

    \section*{Connection Diagram}
    

    TL/F/9827-1
    Order Number 54LS299DMQB, 54LS299FMQB, 54LS299LMQB, DM74LS299WM or DM74LS299N See NS Package Number E20A, J20A, M20B, N20A or W20A
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
    \hline CP & Clock Pulse Input (Active Rising Edge) \\
    \(\mathrm{D}_{\mathrm{S} 0}\) & Serial Data Input for Right Shift \\
    \(\mathrm{D}_{\mathrm{S7}}\) & Serial Data Input for Left Shift \\
    \(\mathrm{SO}, \mathrm{S} 1\) & Mode Select Inputs \\
    \(\overline{\mathrm{MR}}\) & Asynchronous Master Reset Input \\
    & (Active LOW) \\
    \(\overline{\mathrm{OE} 1, \overline{\mathrm{OE} 2}}\)\begin{tabular}{l} 
    TRI-STATE Output Enable Inputs \\
    (Active LOW) \\
    I/O0-I/O7 \\
    \\
    Q0-Q7
    \end{tabular} \begin{tabular}{l} 
    Parallel Data Inputs or TRI-STATE \\
    Parallel Outputs \\
    Serial Outputs \\
    \hline
    \end{tabular} \\
    \hline
    \end{tabular}
    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    54LS
    DM74LS
    Storage Temperature Range
    St

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS299} & \multicolumn{3}{|c|}{DM74LS299} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \({ }_{\mathrm{OH}}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L})
    \end{aligned}
    \] & Setup Time HIGH or LOW S0 or S1 to CP & \[
    \begin{aligned}
    & 24 \\
    & 24
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 24 \\
    & 24
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(\mathrm{~L})
    \end{aligned}
    \] & Hold Time HIGH or LOW SO or S1 to CP & \[
    \begin{aligned}
    & 5 \\
    & 5
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW \(1 / O_{n}, D_{S 0}, D_{S 7}\) to CP & \[
    \begin{aligned}
    & 15 \\
    & 15 \\
    & \hline
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 10 \\
    & 10 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Hold Time HIGH or LOW \(1 / O_{n}, D_{S 0}, D_{S 7}\) to CP & \[
    \begin{aligned}
    & 5 \\
    & 5
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{w}(H) \\
    & t_{w}(L)
    \end{aligned}
    \] & CP Pulse Width HIGH or LOW & \[
    \begin{aligned}
    & 15 \\
    & 15
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 15 \\
    & 15
    \end{aligned}
    \] & & & ns \\
    \hline \(\mathrm{t}_{\mathrm{w}}(\mathrm{L})\) & \(\overline{M R}\) Pulse Width LOW & 15 & & & 15 & & & ns \\
    \hline \(\mathrm{t}_{\text {rec }}\) & Recovery Time \(\overline{M R}\) to CP & 10 & & & 10 & & & ns \\
    \hline
    \end{tabular}

    \section*{Electrical Characteristics}

    Over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{V OH} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & 54LS & 2.5 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{VOL} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{l}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.55 & \\
    \hline & & \(\mathrm{l} \mathrm{OL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current @ Max Input Voltage} & \multirow[t]{2}{*}{\(V_{C C}=M a x, V_{1}=10 \mathrm{~V}\)} & Inputs & & & 0.1 & mA \\
    \hline & & & Sn & & & 0.2 & mA \\
    \hline \multirow[t]{2}{*}{\({ }_{1} \mathrm{H}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & Sn & & & 40 & \(\mu \mathrm{A}\) \\
    \hline & & & Inputs & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
    \mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{~V}_{1}=0.4 \mathrm{~V}
    \]} & Sn & & & -0.8 & mA \\
    \hline & & & Inputs & & & -0.4 & mA \\
    \hline
    \end{tabular}

    Electrical Characteristics (Continued)
    Over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=M a x
    \] \\
    (Note 2)
    \end{tabular}} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline Icc & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, \overline{O E}=4.5 \mathrm{~V}\)} & & & 60 & mA \\
    \hline lozH & TRI-STATE Output Off Current High & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=V_{\mathrm{CCH}} \\
    & \mathrm{~V}_{\mathrm{OZH}}=2.7 \mathrm{~V}
    \end{aligned}
    \]} & & & 40 & \(\mu \mathrm{A}\) \\
    \hline lozl & TRI-STATE Output Off Current Low & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCH}} \\
    & \mathrm{~V}_{\mathrm{OZL}}=0.4 \mathrm{~V}
    \end{aligned}
    \]} & & & -400 & \(\mu \mathrm{A}\) \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{Switching Characteristics}
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\[
    \begin{aligned}
    & R_{\mathrm{L}}=2 \mathrm{k} \Omega \\
    & \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\
    & \hline
    \end{aligned}
    \]} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \(f_{\text {max }}\) & Maximum Input Frequency & 35 & & MHz \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(t_{\text {PHL }}\)
    \end{tabular} & Propagation Delay CP to Q0 or Q7 & & \[
    \begin{aligned}
    & 26 \\
    & 28 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}}
    \end{aligned}
    \] & Propagation Delay CP to \(1 / O_{n}\) & & \[
    \begin{aligned}
    & 25 \\
    & 35
    \end{aligned}
    \] & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay \(\overline{M R}\) to Q0 or Q7 & & 28 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay \(\overline{M R}\) to \(I / O_{n}\) & & 35 & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PZH}} \\
    & \mathrm{t}_{\mathrm{PLL}} \\
    & \hline
    \end{aligned}
    \] & Output Enable Time & & \[
    \begin{aligned}
    & 18 \\
    & 25 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\text {PHZ }} \\
    & \mathrm{t}_{\mathrm{PLZ}} \\
    & \hline
    \end{aligned}
    \] & Output Disable Time & & \[
    \begin{aligned}
    & 15 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}

    \section*{Logic Symbol}
    

    TL/F/9827-2
    \(V_{C C}=\operatorname{Pin} 20\)
    GND \(=\operatorname{Pin} 10\)

    \section*{Functional Description}

    The 'LS299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by the S 0 and S 1 , as shown in the Mode Select Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. QO and Q7 are also brought out on other pins for expansion in serial shifting of longer words.
    A LOW signal on \(\overline{M R}\) overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP , are observed.

    A HIGH signal on either \(\overline{\mathrm{OE}} 1\) or \(\overline{\mathrm{OE}} 2\) disables the TRISTATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S0 and S1 in preparation for a parallel load operation.

    Mode Select Table
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multicolumn{4}{|c|}{Inputs} & \multirow[t]{2}{*}{Response} \\
    \hline & S1 & So & CP & \\
    \hline L & X & X & X & Asynchronous Reset; Q0-Q7 = LOW \\
    \hline H & H & H & - & Parallel Load; \(\mathrm{I} / \mathrm{O}_{\mathrm{n}} \rightarrow \mathrm{Q}_{\mathrm{n}}\) \\
    \hline H & L & H & - & Shift Right; \(\mathrm{D}_{\text {S } 0} \rightarrow \mathrm{Q} 0, \mathrm{Q} 0 \rightarrow\) Q1, etc. \\
    \hline H & H & L & - & Shift Left; D \({ }_{\text {S7 }} \rightarrow\) Q7, Q7 \(\rightarrow\) Q6, etc. \\
    \hline H & L & L & X & Hold \\
    \hline
    \end{tabular}

    \footnotetext{
    H = HIGH Voltage Level
    L = LOW Voltage Level
    \(X=\) Immaterial
    }
    Logic Diagram
    

    \section*{54LS322/DM74LS322 \\ 8-Bit Serial/Parallel Register with Sign Extend}

    \section*{General Description}

    The 'LS322 is an 8-bit shift register with provision for either serial or parallel loading and with TRI-STATE® parallel outputs plus a bi-state serial output. Parallel data inputs and parallel outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store),
    shift right with serial entry, shift right with sign extend and parallel load. An asynchronous Master Reset (MR) input overrides clocked operation and clears the register. The '322 is specifically designed for operation with the '384 Multiplier and provides the sign extend function required for the '384.

    \section*{Connection Diagram}
    

    \section*{Logic Symbol}
    
    \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Pin} 20 \\
    & \mathrm{GND}=\operatorname{Pin} 10
    \end{aligned}
    \]

    TL/F/9828-1
    Order Number 54LS322DMQB, 54LS322FMQB, DM74LS322WM or DM74LS322N
    See NS Package Number J20A, M20B, N20A or W20A
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
    \hline\(\overline{R E}\) & Register Enable Input (Active LOW) \\
    \(\mathrm{S} / \overline{\mathrm{P}}\) & Serial (HIGH) or Parallel (LOW) \\
    & Mode Control Input \\
    \(\overline{\mathrm{SE}}\) & Sign Extend Input (Active LOW) \\
    S & Serial Data Select Input \\
    \(\mathrm{DO}, \mathrm{D1}\) & Serial Data Inputs \\
    CP & Clock Pulse Input (Active Rising Edge) \\
    \(\overline{\mathrm{MR}}\) & Asynchronous Master Reset Input \\
    & (Active LOW) \\
    \(\overline{\mathrm{OE}}\) & TRI-STATE Output Enable Input \\
    & (Active LOW) \\
    QO & Bi-State Serial Output \\
    \(\mathrm{I} / \mathrm{OO-I/O7}\) & Multiplexed Parallel Inputs or \\
    & TRI-STATE Parallel Outputs \\
    \hline
    \end{tabular}
    \begin{tabular}{lr} 
    Absolute Maximum Ratings (Note) \\
    If Military/Aerospace specified devices are required, \\
    please contact the National Semiconductor Sales \\
    Office/Distributors for availability and specifications. \\
    Supply Voltage & 7 V \\
    Input Voltage & 10 V \\
    Operating Free Air Temperature Range & \\
    54LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS322} & \multicolumn{3}{|c|}{DM74LS322} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline 1 OL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW \(\overline{R E}\) to \(C P\) & \[
    \begin{array}{r}
    24 \\
    24 \\
    \hline
    \end{array}
    \] & & & \[
    \begin{aligned}
    & 24 \\
    & 24
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Hold Time HIGH or LOW \(\overline{R E}\) to CP & \[
    \begin{aligned}
    & 5 \\
    & 5
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(H) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW D0, D1 or \(I / O_{n}\) to CP & \[
    \begin{aligned}
    & 15 \\
    & 15
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 10 \\
    & 10
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L)
    \end{aligned}
    \] & Hold Time HIGH or LOW D0, D1 or I/On to CP & \[
    \begin{array}{r}
    5 \\
    5 \\
    \hline
    \end{array}
    \] & & & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{s}(H) \\
    & t_{s}(L) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW \(\overline{S E}\) to CP & \[
    \begin{aligned}
    & 15 \\
    & 15 \\
    & \hline
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 15 \\
    & 15 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L) \\
    & \hline
    \end{aligned}
    \] & Hold Time HIGH or LOW \(\overline{S E}\) to \(C P\) & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW \(S \bar{P}\) to \(C P\) & \[
    \begin{array}{r}
    24 \\
    24 \\
    \hline
    \end{array}
    \] & & & \[
    \begin{aligned}
    & 24 \\
    & 24
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L})
    \end{aligned}
    \] & Setup Time HIGH or LOW \(S\) to CP & \[
    \begin{aligned}
    & 15 \\
    & 15
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 15 \\
    & 15
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L)
    \end{aligned}
    \] & Hold Time HIGH or LOW \(S\) or \(S \bar{P}\) to \(C P\) & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & ns \\
    \hline \(t_{w}(H)\) & CP Pulse Width HIGH & 15 & & & 15 & & & ns \\
    \hline \(t_{w}(L)\) & \(\overline{\text { MR }}\) Pulse Width LOW & 15 & & & 15 & & & ns \\
    \hline \(\mathrm{trec}^{\text {c }}\) & Recovery Time \(\overline{\mathrm{MR}}\) to CP & 15 & & & 15 & & & ns \\
    \hline
    \end{tabular}

    \section*{Electrical Characteristics}

    Over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{3}{|l|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{3}{|l|}{\(V_{C C}=\operatorname{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{VOH} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & \multicolumn{2}{|l|}{54LS} & 2.5 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & \multicolumn{2}{|l|}{DM74} & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{VoL} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{l}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & & 0.25 & 0.4 & \\
    \hline \multirow[t]{3}{*}{1} & \multirow[t]{3}{*}{Input Current @ Max Input Voltage} & \multicolumn{3}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=10 \mathrm{~V}\)} & & & 0.1 & \multirow{3}{*}{mA} \\
    \hline & & & \multicolumn{2}{|l|}{S Input} & & & 0.2 & \\
    \hline & & & \multicolumn{2}{|l|}{SE Input} & & & 0.3 & \\
    \hline \multirow[t]{3}{*}{IIH} & \multirow[t]{3}{*}{High Level Input Current} & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & \multicolumn{2}{|l|}{S Input} & & & 40 & \\
    \hline & & & \multicolumn{2}{|l|}{SE Input} & & & 60 & \\
    \hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}\)} & & & -0.4 & \multirow{3}{*}{mA} \\
    \hline & & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & \multicolumn{2}{|l|}{S Input} & & & -0.8 & \\
    \hline & & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & \multicolumn{2}{|l|}{SE Input} & & & -1.2 & \\
    \hline \multirow[t]{3}{*}{los} & \multirow[t]{3}{*}{Short Circuit Output Current} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Max} \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & \multirow[t]{2}{*}{54LS} & I/On & -30 & & -130 & \multirow{3}{*}{mA} \\
    \hline & & & & Qn & -20 & & -100 & \\
    \hline & & & \multicolumn{2}{|l|}{DM74} & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{3}{|l|}{\(V_{C C}=M a x\)} & & & 60 & mA \\
    \hline lozh & TRI-STATE Output Off Current HIGH & \multicolumn{3}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCH}} \\
    & \mathrm{~V}_{\mathrm{OZH}}=2.7 \mathrm{~V}
    \end{aligned}
    \]} & & & 40 & \(\mu \mathrm{A}\) \\
    \hline lozl & TRI-STATE Output Off Current LOW & \multicolumn{3}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCH}} \\
    & \mathrm{~V}_{\mathrm{OZL}}=0.4 \mathrm{~V}
    \end{aligned}
    \]} & & & -0.4 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{Switching Characteristics}
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{54LS} & \multicolumn{2}{|c|}{DM74LS} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(f_{\text {max }}\) & Maximum Clock Frequency & 35 & & 35 & & MHz \\
    \hline tpLH
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & Propagation Delay CP to \(/ / O_{n}{ }^{* *}\) & & \[
    \begin{aligned}
    & 25 \\
    & 35 \\
    & \hline
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 25 \\
    & 34 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \begin{tabular}{l}
    tpLH \\
    \(t_{\text {PHL }}\)
    \end{tabular} & Propagation Delay CP to Q0 & & \[
    \begin{array}{r}
    26 \\
    28 \\
    \hline
    \end{array}
    \] & & \[
    \begin{aligned}
    & 26 \\
    & 29 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay \(\overline{\mathrm{MR}}\) to \(\mathrm{I} / \mathrm{O}_{\mathrm{n}}{ }^{* *}\) & & 35 & & 34.1 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay \(\overline{M R}\) to QO & & 28 & & 28 & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PZH}} \\
    & \mathrm{t}_{\mathrm{PZL}}
    \end{aligned}
    \] & Output Enable Time \(\overline{\mathrm{OE}}\) to \(\mathrm{I} / \mathrm{O}_{\mathrm{n}}{ }^{* *}\) & & \[
    \begin{aligned}
    & 18 \\
    & 25
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 21.5 \\
    & 23.9 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}

    \footnotetext{
    \({ }^{* *} \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)
    }

    \section*{Switching Characteristics}
    \(V_{C C}=+5.0 \mathrm{~V}, T_{A}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{54LS} & \multicolumn{2}{|c|}{DM74LS} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PHZ}} \\
    & \mathrm{t}_{\mathrm{PLLZ}} \\
    & \hline
    \end{aligned}
    \] & Output Disable Time \(\overline{\mathrm{OE}}\) to \(/ / \mathrm{O}_{\mathrm{n}}{ }^{*}\) & & \[
    \begin{array}{r}
    15 \\
    20 \\
    \hline
    \end{array}
    \] & & \[
    \begin{aligned}
    & 15 \\
    & 15
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PZH}} \\
    & \mathrm{t}_{\mathrm{PZL}} \\
    & \hline
    \end{aligned}
    \] & Output Enable Time \(S / \overline{\mathrm{P}}\) to \(\mathrm{I} / \mathrm{O}_{\mathrm{n}}{ }^{* *}\) & & \[
    \begin{aligned}
    & 22 \\
    & 30
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 25.2 \\
    & 25.8
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PHZ}} \\
    & \mathrm{t}_{\mathrm{PLZ}} \\
    & \hline
    \end{aligned}
    \] & Output Disable Time \(S \overline{\mathrm{P}}\) to \(\mathrm{I} / \mathrm{O}_{\mathrm{n}}{ }^{*}\) & & \[
    \begin{aligned}
    & 23 \\
    & 23 \\
    & \hline
    \end{aligned}
    \] & & \[
    \begin{array}{r}
    40.2 \\
    26.8 \\
    \hline
    \end{array}
    \] & ns \\
    \hline
    \end{tabular}
    \({ }^{*} \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\)
    \({ }^{* *} \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)

    \section*{Functional Description}

    The LS322 contains eight D-type edge triggered flip-flops and the interstage gating required to perform right shift and the intrastage gating necessary for hold and synchronous parallel load operations. A LOW signal on RE enables shifting or parallel loading, while a HIGH signal enables the hold mode. A HIGH signal on S/ \(\bar{P}\) enables shift right, while a LOW signal disables the TRI-STATE output buffers and enables parallel loading. In the shift right mode a HIGH signal
    on \(\overline{\text { SE }}\) enables serial entry from either D0 or D1, as determined by the S input. A LOW signal on \(\overline{\mathrm{SE}}\) enables shift right but Q7 reloads its contents, thus performing the sign extend function required for the ' 384 Twos Complement Multiplier. A HIGH signal on \(\overline{O E}\) disables the TRI-STATE output buffers, regardless of the other control inputs. In this condition the shifting and loading operations can still be performed.

    \section*{Mode Table}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{17}{|c|}{Mode Table} \\
    \hline \multirow{2}{*}{Mode} & \multicolumn{7}{|c|}{Inputs} & \multicolumn{8}{|c|}{Outputs} & \multirow[b]{2}{*}{Q0} \\
    \hline & \(\overline{\mathrm{MR}}\) & RE & \(\mathbf{S} / \overline{\mathrm{P}}\) & \(\overline{\text { SE }}\) & S & \(\overline{\mathbf{O E}}{ }^{*}\) & CP & 1/07 & 1/06 & 1/05 & 1/04 & 1/03 & 1/02 & 1/01 & 1/00 & \\
    \hline \multirow[t]{2}{*}{Clear} & L & X & X & X & X & L & X & L & L & L & L & L & L & L & L & L \\
    \hline & L & X & X & X & X & H & X & Z & Z & Z & Z & Z & \(z\) & Z & \(z\) & L \\
    \hline \begin{tabular}{l}
    Parallel \\
    Load
    \end{tabular} & H & L & L & X & X & X & \(\checkmark\) & 17 & 16 & 15 & 14 & 13 & 12 & 11 & 10 & 10 \\
    \hline Shift & H & L & H & H & L & L & \(\sim\) & D0 & 07 & 06 & 05 & 04 & O3 & 02 & 01 & 01 \\
    \hline Right & H & L & H & H & H & L & \(\sim\) & D1 & 07 & 06 & 05 & 04 & O3 & O 2 & 01 & 01 \\
    \hline \begin{tabular}{l}
    Sign \\
    Extend
    \end{tabular} & H & L & H & L & X & L & \(\checkmark\) & 07 & 07 & 06 & O5 & 04 & O3 & O2 & 01 & 01 \\
    \hline Hold & H & H & X & X & X & L & \(\checkmark\) & NC & NC & NC & NC & NC & NC & NC & NC & NC \\
    \hline
    \end{tabular}
    *When the \(\overline{\mathrm{OE}}\) input is HIGH , all \(1 / \mathrm{O}_{\mathrm{n}}\) terminals are at the high-impedance state; sequential operation or clearing of the register is not affected.
    Note 1: \(17-10=\) The level of the steady-state input at the respective I/O terminal is loaded into the flip-flop while the flip-flop outputs (except Q0) are isolated from the I/O terminal.
    Note 2: DO, D1 = The level of the steady-state inputs to the serial multiplexer input.
    Note 3: \(07-\mathrm{OO}=\) The level of the respective \(\mathrm{Q}_{\mathrm{n}}\) flip-flop prior to the last Clock LOW-to-HIGH transition.
    NC = No Change \(Z=\) High-Impedance Output State \(H=H I G H\) Voltage Level \(L=\) LOW Voltage Level
    

    \section*{54LS323/DM74LS323 \\ 8-Bit Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins}

    \section*{General Description}

    The 'LS323 is an 8-bit universal shift/storage register with TRI-STATE \({ }^{\circledR}\) outputs. Its function is similar to the 'LS299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate inputs and outputs are provided for flipflops Q0 and Q7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right, and parallel load. All modes are activated on the LOW-to-HIGH transition of the Clock.

    \section*{Features}
    - Common I/O for reduced pin count
    - Four operation modes: shift left, shift right, parallel load and store
    - Separate continuous inputs and outputs from Q0 and Q7 allow easy cascading
    ■ Fully synchronous reset
    - TRI-STATE outputs for bus oriented applications

    \section*{Connection Diagram}
    \begin{tabular}{|c|c|c|}
    \hline \multicolumn{3}{|l|}{Dual-In-Line Package} \\
    \hline S0-1 & 20 & \(-V_{c c}\) \\
    \hline OE1-2 & 19 & -S1 \\
    \hline OE2-3 & 18 & -DS7 \\
    \hline 1/06-4 & 17 & -Q7 \\
    \hline 1/04-5 & 16 & -1/07 \\
    \hline 1/02-6 & 15 & -1/05 \\
    \hline 1/00-7 & 14 & -1/03 \\
    \hline QO-8 & 13 & -1/01 \\
    \hline \(\overline{\mathrm{SR}}-9\) & 12 & CP \\
    \hline GND - 10 & 11 & -DSO \\
    \hline
    \end{tabular}

    TL/F/9829-1
    Order Number 54LS323DMQB, 54LS323FMQB, DM74LS323WM or DM74LS323N See NS Package Number J20A, M20B, N20A or W20A
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{c|}{ Description } \\
    \hline\(C P\) & Clock Pulse Input (Active Rising Edge) \\
    \(D_{S} 0\) & Serial Data Input for Right Shift \\
    \(D_{S} 7\) & Serial Data Input for Left Shift \\
    S0, S1 & Mode Select Inputs \\
    \(\overline{S R}\) & Synchronous Reset Input (Active LOW) \\
    \(\overline{O E} 1, \overline{O E} 2\) & TRI-STATE Output Enable Inputs (Active LOW) \\
    I/O0-I/O7 & \begin{tabular}{l} 
    Parallel Data Inputs or TRI-STATE \\
    Parallel Outputs
    \end{tabular} \\
    Q0, Q7 & Serial Outputs \\
    \hline
    \end{tabular}

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avaliability and specifications.
    \begin{tabular}{lr} 
    Supply Voltage & 7 V \\
    Input Voltage & 10 V \\
    Operating Free Air Temperature Range & \\
    54 LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS323} & \multicolumn{3}{|c|}{DM74LS323} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(V_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline 1 OH & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & t_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L})
    \end{aligned}
    \] & Setup Time HIGH or LOW S0 or S1 to CP & \[
    \begin{aligned}
    & 24 \\
    & 24 \\
    & \hline
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 24 \\
    & 24 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L) \\
    & \hline
    \end{aligned}
    \] & Hold Time HIGH or LOW S0 or S1 to CP & \[
    \begin{aligned}
    & 5 \\
    & 5
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathbf{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L})
    \end{aligned}
    \] & Setup Time HIGH or LOW I/On, \(\mathrm{D}_{\mathrm{S}} 0, \mathrm{D}_{\mathrm{S}} 7\) to CP & \[
    \begin{aligned}
    & 15 \\
    & 15 \\
    & \hline
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 10 \\
    & 10 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L) \\
    & \hline
    \end{aligned}
    \] & Hold Time HIGH or LOW \(1 / \mathrm{O}_{\mathrm{n}}, \mathrm{DS}_{\mathrm{S}} 0, \mathrm{D}_{\mathrm{s}} 7\) to CP & \[
    \begin{aligned}
    & 5 \\
    & 5 \\
    & \hline
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L})
    \end{aligned}
    \] & Setup Time HIGH or LOW \(\overline{\mathrm{SR}}\) to CP & \[
    \begin{array}{r}
    30 \\
    20 \\
    \hline
    \end{array}
    \] & & & \[
    \begin{aligned}
    & 15 \\
    & 15 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{h}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{h}}(\mathrm{~L})
    \end{aligned}
    \] & Hold Time HIGH or LOW \(\overline{\mathrm{SR}}\) to CP & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{w}(H) \\
    & t_{w}(L) \\
    & \hline
    \end{aligned}
    \] & CP Pulse Width HIGH or LOW & \[
    \begin{aligned}
    & 15 \\
    & 15
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 15 \\
    & 15
    \end{aligned}
    \] & & & ns \\
    \hline
    \end{tabular}

    \section*{Electrical Characteristics}

    Over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & \(-1.5\) & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & 54LS & 2.5 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current @ Max Input Voltage} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=10 \mathrm{~V}\)} & & & & 0.1 & mA \\
    \hline & & & \(S_{n}\) Inputs & & & 0.2 & mA \\
    \hline \multirow[t]{2}{*}{\(\mathrm{I}_{\mathrm{IH}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\)} & & & & 20 & \(\mu \mathrm{A}\) \\
    \hline & & & \(S_{n}\) Inputs & & & 40 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & & -0.4 & mA \\
    \hline & & & \(\mathrm{S}_{\mathrm{n}}\) Inputs & & & -0.8 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=M a x \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & & 60 & mA \\
    \hline lozh & TRI-STATE Output Off Current HIGH & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCH}} \\
    & \mathrm{~V}_{\mathrm{OZH}}=2.7 \mathrm{~V}
    \end{aligned}
    \]} & & & 40 & \(\mu \mathrm{A}\) \\
    \hline lozl & TRI-STATE Output Off Current LOW & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCH}} \\
    & \mathrm{~V}_{\mathrm{OZL}}=0.4 \mathrm{~V}
    \end{aligned}
    \]} & & & -400 & \(\mu \mathrm{A}\) \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{Switching Characteristics}
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{2}{|c|}{54LS323} & \multicolumn{2}{|c|}{DM74LS323} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {max }}\) & Maximum Input Frequency & 35 & & 35 & & MHz \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay CP to Q0 or Q7 & & \[
    \begin{aligned}
    & 26 \\
    & 28 \\
    & \hline
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 23 \\
    & 25 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay CP to \(1 / O_{n}\) & & \[
    \begin{aligned}
    & 25 \\
    & 35 \\
    & \hline
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 25 \\
    & 29 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PZH}} \\
    & \mathrm{t}_{\mathrm{PZL}}
    \end{aligned}
    \] & Output Enable Time
    \[
    \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}
    \] & & \[
    \begin{aligned}
    & 18 \\
    & 25
    \end{aligned}
    \] & & \[
    \begin{array}{r}
    18 \\
    23
    \end{array}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PHZ}} \\
    & \mathrm{t}_{\mathrm{PLZ}}
    \end{aligned}
    \] & Output Disable Time \(C_{L}=5 \mathrm{pF}\) & & \[
    \begin{aligned}
    & 15 \\
    & 20
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 15 \\
    & 15
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}

    \section*{Functional Description}

    The 'LS323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S0 and S1 as shown in the Mode Select Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q0 and Q7 are also brought out on other pins for expansion in serial shifting of longer words.
    A LOW signal on \(\overline{\mathrm{SR}}\) overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP , are observed.
    A HIGH signal on either \(\overline{O E} 1\) or \(\overline{\mathrm{OE}} 2\) disables the TRISTATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S0 and S1 in preparation for a parallel load operation.

    Mode Select Table
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multicolumn{4}{|c|}{Inputs} & \multirow{2}{*}{Response} \\
    \hline \(\overline{\text { SR }}\) & S1 & S0 & CP & \\
    \hline L & X & X & - & Synchronous Reset; Q0-Q7 = LOW \\
    \hline H & H & H & \(\checkmark\) & Parallel Load; \(1 / \mathrm{O}_{\mathrm{n}} \rightarrow \mathrm{Q}_{\mathrm{n}}\) \\
    \hline H & L & H & - & Shift Right; DS0 \(\rightarrow\) Q0, Q0 \(\rightarrow\) Q1, etc. \\
    \hline H & H & L & \(\checkmark\) & Shift Left; DS7 \(\rightarrow\) Q7, Q7 \(\rightarrow\) Q6, etc. \\
    \hline H & H & H & X & Hold \\
    \hline
    \end{tabular}

    H = HIGH Voltage Level
    L = LOW Voltage Level
    \(X=\) Immaterial

    \section*{Logic Symbol}
    
    

    \section*{54LS347/DM74LS347 \\ BCD to 7-Segment Decoder/Driver}

    \section*{General Description}

    The 'LS347 is the same as the 'LS47 except that the Output OFF Voltage, \(\mathrm{V}_{\mathrm{OH}}\), is specified as 7.0 V rather than 15 V , with the same \(\mathrm{I}_{\mathrm{OH}}\) limit of \(250 \mu \mathrm{~A}\). For all other information please refer to the 'LS47 data sheet.

    \section*{Connection Diagram}
    

    \section*{Logic Symbol}
    

    GND \(=\operatorname{Pin} 8\)

    Order Number 54LS347DMQB, 54LS347FMQB, DM74LS347M or DM74LS347N
    See NS Package Number J16A, M16A, N16E or W16A
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
    \hline \(\mathrm{AO}-\mathrm{A} 3\) & BCD Inputs \\
    \(\overline{\mathrm{RBI}}\) & Ripple Blanking Input (Active LOW) \\
    \(\overline{\mathrm{LT}}\) & Lamp Test Input (Active LOW) \\
    \(\overline{\mathrm{BI}} / \overline{\mathrm{RBO}}\) & Blanking Input (Active LOW) or \\
    \(\overline{\mathrm{a}}-\overline{\mathrm{g}}\) & Ripple Blanking Output (Active LOW) \\
    & *Segment Outputs (Active LOW) \\
    \hline
    \end{tabular}
    *OC-Open Collector

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specifled devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    \begin{tabular}{lr} 
    Supply Voltage & 7 V \\
    Input Voltage & 7 V \\
    Operating Free Air Temperature Range & \\
    54 LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS347} & \multicolumn{3}{|c|}{DM74LS347} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{2}\) & High Level Output Voltage & & & -50 & & & -50 & \(\mu \mathrm{A}\) \\
    \hline lOL & Low Level Output Current & & & 12 & & & 24 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min}, V_{O H}=\operatorname{Max}, \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & 54LS & 2.5 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}_{\mathrm{OL}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & & 0.5 & \\
    \hline & & \(\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=10 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{ILL} & \multirow[t]{2}{*}{Low Level Input Current} & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}\)} & \(-0.03\) & & -0.4 & mA \\
    \hline & & \multicolumn{2}{|l|}{BI/त्RBO Input} & -0.09 & & -1.2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=\operatorname{Max}
    \] \\
    (Note 2)
    \end{tabular}} & 54LS & -0.3 & & -2.0 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & \(-0.3\) & & -2.0 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}\)} & & & 13 & mA \\
    \hline loff & & \multicolumn{2}{|l|}{Segment Outputs, \(\mathrm{V}_{\mathrm{O}}=7 \mathrm{~V}\)} & & & 250 & \(\mu \mathrm{A}\) \\
    \hline
    \end{tabular}

    Switching Characteristics
    at \(V_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Loading)
    \begin{tabular}{c|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multirow{2}{*}{ Parameter } & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=\mathbf{1 5} \mathbf{p F}\)} & \multirow{2}{*}{ Units } \\
    \cline { 3 - 4 } & & Min & Max & \\
    \hline tPLH & & & 100 & ns \\
    tPHL & Propagation Delay & & 100 & ns \\
    \hline tPLH & \(\mathrm{A}_{\mathrm{n}}\) to \(\overline{\mathrm{a}} \overline{\mathrm{g}}\) & & 100 & ns \\
    tPHL & Propagation Delay & & 100 & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{54LS352/DM74LS352 Dual 4-Line to 1-Line Data Selectors/Multiplexers}

    \section*{General Description}

    Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

    \section*{Features}
    - Inverting version of DM54/74LS153
    - Permits multiplexing from N lines to 1 line

    \section*{Connection Diagram}
    

    TL/F/6425-1
    Order Number 54LS352DMQB, 54LS352FMQB, DM74LS352M or DM74LS352N
    See NS Package Number J16A, M16A, N16E or W16A
    - Performs parallel-to-serial conversion

    ■ Strobe (enable) line provided for cascading ( N lines to \(n\) lines)
    - High fan-out, low-impedance, totem-pole outputs
    - Typical average propagation delay times

    From data 15 ns
    From strobe 19 ns
    From select 22 ns
    - Typical power dissipation 31 mW

    \section*{Function Table}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \begin{tabular}{c} 
    Select \\
    Inputs
    \end{tabular} & \multicolumn{5}{|c|}{ Data Inputs } & Strobe & Output \\
    \hline B & A & C0 & C1 & C2 & C3 & G & Y \\
    \hline X & X & X & X & X & X & H & H \\
    L & L & L & X & X & X & L & H \\
    L & L & H & X & X & X & L & L \\
    L & H & X & L & X & X & L & H \\
    L & H & X & H & X & X & L & L \\
    H & L & X & X & L & X & L & H \\
    H & L & X & X & H & X & L & L \\
    H & H & X & X & X & L & L & H \\
    H & H & X & X & X & H & L & L \\
    \hline
    \end{tabular}

    Select inputs A and B are common to both sections.
    \(H=\) High Level, \(L=\) Low Level, \(X=\) Don't Care

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage \(7 V\)
    Operating Free Air Temperature Range
    \begin{tabular}{lr} 
    54LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Recommended Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS352} & \multicolumn{3}{|c|}{DM74LS352} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 12 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Condlitions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{V OH} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\
    & V_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & 2.5 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{VoL} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, \mathrm{IOL}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \[
    \begin{aligned}
    & \mathrm{I}_{\mathrm{OL}}=4 \mathrm{~mA} \\
    & \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}
    \end{aligned}
    \] & DM74 & & 0.25 & 0.4 & \\
    \hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current @ Max Input Voltage} & \(V_{\text {CC }}=\) Max & 54LS & & & \multirow[t]{2}{*}{0.1} & \multirow[t]{2}{*}{mA} \\
    \hline & & \(\mathrm{V}_{\mathrm{CC}}=\) Max & DM74 & & & & \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \(\mathrm{I}_{\mathrm{LL}}\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=M a x
    \] \\
    (Note 2)
    \end{tabular}} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 3)} & & 6.2 & 10 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: ICC is measured with all outputs open and all other inputs at ground.

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{2}{|c|}{54LS} & \multicolumn{2}{|c|}{DM74LS} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|r|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega
    \end{aligned}
    \]} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline tplH & Propagation Delay Time Low to High Level Output & Data to Y & & 12 & & 24 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to \(Y\) & & 12 & & 35 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Select to Y & & 22 & & 33 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Select to Y & & 38 & & 47 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Strobe to Y & & 15 & & 29 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Strobe to Y & & 20 & & 41 & ns \\
    \hline
    \end{tabular}

    \section*{Logic Diagram}
    

    TL/F/6425-2

    National Semiconductor

    \section*{54LS353/DM74LS353}

    \section*{Dual 4-Input Multiplexer with TRI-STATE \({ }^{\circledR}\) Outputs}

    \section*{General Description}

    The ' 353 is a dual 4 -input multiplexer with TRI-STATE outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output ( \(\overline{\mathrm{OE}}\) ) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all National TTL families.

    \section*{Connection Diagram}

    \section*{Dual-In-Line Package}
    

    TL/F/10185-1
    Order Number 54LS353DMQB, 54LS353FMQB, DM74LS353M or DM74LS353N
    See NS Package Number J16A, M16A, N16E or W16A

    \section*{Features}
    - Inverted version of 'LS253
    - Schottky process for high speed
    - Multifunction capability

    \section*{Logic Symbol}
    

    TL/F/10185-2
    \(V_{C C}=\operatorname{Pin} 16\)
    GND \(=\operatorname{Pin} 8\)
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
    \hline \(10 \mathrm{a}-13 \mathrm{a}\) & Side A Data Inputs \\
    \(10 \mathrm{~b}-\mathrm{I} \mathrm{b} \mathrm{b}\) & Side B Data Inputs \\
    \(\mathrm{SO}, \mathrm{S} 1\) & Common Select Inputs \\
    \(\overline{\mathrm{OE}}_{\mathrm{a}}\) & Side A Output Enable Input (Active Low) \\
    \(\overline{\mathrm{OE}}_{\mathrm{b}}\) & Side B Output Enable Input (Active Low) \\
    \(\overline{\mathrm{Z}}_{\mathrm{a}}, \overline{\mathrm{Z}}_{\mathrm{b}}\) & TRI-STATE Outputs (Inverted) \\
    \hline
    \end{tabular}
    ```

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range

    | 54LS | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
    | :--- | ---: |
    | DM74LS | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
    | Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

    ```

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    Recommended Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS353} & \multicolumn{3}{|c|}{DM74LS353} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{lOH}^{\text {O }}\) & High Level Output Current & & & -1.0 & & & -2.6 & mA \\
    \hline lOL & Low Level Output Current & & & 12 & & & 24 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Condlitions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{l}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & 54LS & 2.5 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & & 0.5 & \\
    \hline & & \(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=10 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline ILL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & 54LS & \(-30\) & & -130 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -30 & & -130 & \\
    \hline ICCL & Supply Current Outputs HIGH & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M a x, \\
    & I n, S n, \overline{O E n}=\mathrm{GND}
    \end{aligned}
    \]} & & & 12 & mA \\
    \hline Iccz & Supply Current Outputs OFF & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \overline{\mathrm{OEn}}=4.5 \mathrm{~V} \\
    & \mathrm{In}, \mathrm{Sn}=\mathrm{GND}
    \end{aligned}
    \]} & & & 14 & mA \\
    \hline lozh & TRI-STATE Output OFF Current HIGH & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCH}} \\
    & \mathrm{~V}_{\mathrm{OZH}}=2.7 \mathrm{~V}
    \end{aligned}
    \]} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline lozz & TRI-STATE Output OFF Current LOW & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCH}} \\
    & \mathrm{~V}_{\mathrm{OZL}}=0.4 \mathrm{~V}
    \end{aligned}
    \]} & & & -20 & \(\mu \mathrm{A}\) \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    Switching Characteristics \(\mathrm{v}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for test waveforms and output loads)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay Sn to \(\overline{\mathrm{Z}} \mathrm{n}\) & & \[
    \begin{aligned}
    & 24 \\
    & 32 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    tpHL
    \end{tabular} & Propagation Delay In to \(\bar{Z} n\) & & \[
    \begin{aligned}
    & 15 \\
    & 15 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PZH}} \\
    & \mathrm{t}_{\mathrm{PZL}}
    \end{aligned}
    \] & Output Enable Time \(\overline{\mathrm{OE}}\) to Zn & & \[
    \begin{aligned}
    & 18 \\
    & 18 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PHZ}} \\
    & \mathrm{t}_{\mathrm{PLZ}}
    \end{aligned}
    \] & Output Disable Time \(\overline{\mathrm{OE}}\) to Zn & & \[
    \begin{aligned}
    & 18 \\
    & 18 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}

    \section*{Functional Description}

    The 'LS353 contains two identical 4-input multiplexers with TRI-STATE outputs. They select two bits from four sources selected by common Select inputs ( \(\mathrm{S} 0, \mathrm{~S} 1\) ). The 4 -input multiplexers have individual Output Enable ( \(\left.\overline{\mathrm{OE}}_{\mathrm{a}}\right), \overline{\mathrm{OE}}_{\mathrm{b}}\) ) inputs which when HIGH, force the outputs to a high impedance (high Z) state. The logic equations for the outputs are shown below:
    \[
    \begin{aligned}
    & \overline{\overline{\mathrm{Z}_{\mathrm{a}}}=\overline{\mathrm{OEa}} \bullet(10 \mathrm{a} \bullet \overline{\mathrm{~S}} 1 \bullet \overline{\mathrm{~S}} 0+11 \mathrm{a} \bullet \overline{\mathrm{~S}} 1 \bullet \mathrm{~S} 0+12 \mathrm{a} \bullet \mathrm{~S} 1 \bullet \overline{\mathrm{~S}} 0+13 \mathrm{a} \bullet \mathrm{~S} 1 \bullet \mathrm{~S} 0)} \\
    & \overline{\overline{\mathrm{Z}}_{\mathrm{b}}=\overline{\mathrm{OE}}{ }_{\mathrm{b}} \bullet(10 \mathrm{~b} \bullet \overline{\mathrm{~S}} 1 \bullet \overline{\mathrm{~S}} 0+11 \mathrm{~b} \bullet \overline{\mathrm{~S}} 1 \bullet \mathrm{~S} 0+12 \mathrm{~b} \bullet \mathrm{~S} 1 \bullet \overline{\mathrm{~S}} 0+13 \mathrm{~b} \bullet \mathrm{~S} 1 \bullet \mathrm{~S} 0)}
    \end{aligned}
    \]

    \section*{Truth Table}

    If the outputs of TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRISTATE devices whose outputs are tied together are designed so that there is no overlap.
    \begin{tabular}{|cc|cccc|c|c|}
    \hline \multicolumn{2}{|c|}{\begin{tabular}{c} 
    Select \\
    Inputs
    \end{tabular}} & \multicolumn{4}{|c|}{ Data Inputs } & \begin{tabular}{c} 
    Output \\
    Enable
    \end{tabular} & Output \\
    \hline S0 & S1 & I0 & I1 & I2 & I3 & OE & Z \\
    \hline X & X & X & X & X & X & H & (Z) \\
    L & L & L & X & X & X & L & H \\
    L & L & H & X & X & X & L & L \\
    H & L & X & L & X & X & L & H \\
    H & L & & X & H & X & X & L \\
    L & H & X & X & L & X & L & L \\
    L & H & X & X & H & X & L & L \\
    H & H & X & X & X & L & L & H \\
    H & H & X & X & X & H & L & L \\
    \hline
    \end{tabular}

    Address inputs S 0 and S 1 are common to both sections.
    H = HIGH Voltage Level
    L = LOW Voltage Level
    \(X=\) Immaterial
    \((Z)=\) High Impedance
    

    \section*{54LS365A/DM54LS365A/DM74LS365A Hex TRI-STATE \({ }^{\circledR}\) Buffers}

    \section*{General Description}

    This device contains six independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility
    that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

    \section*{Features}

    ■ Alternate Military/Aerospace device (54LS365A) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

    \section*{Connection Diagram}

    \section*{Dual-In-Line Package}
    

    Order Number 54LS365ADMQB, 54LS365AFMQB, 54LS365ALMQB, DM54LS365AJ, DM54LS365AW, DM74LS265AM or DM74LS365AN See NS Package Number E20A, J16A, M16A, N16E or W16A

    \section*{Function Table}
    \begin{tabular}{|c|c|c|c|}
    \hline \multicolumn{3}{|c|}{Input} & Output \\
    \hline \(\overline{\mathrm{G}} 1\) & \(\overline{\mathbf{G} 2}\) & A & Y \\
    \hline H & X & X & \(\mathrm{Hi}-\mathrm{Z}\) \\
    \hline X & H & X & \(\mathrm{Hi}-\mathrm{Z}\) \\
    \hline L & L & H & H \\
    \hline L & L & L & L \\
    \hline
    \end{tabular}
    \(H=\) High Logic Level
    L = Low Logic Level
    \(X=\) Either Low or High Logic Level
    \(\mathrm{Hi}-\mathrm{Z}=\) TRI-STATE (Outputs are disabled)

    \section*{Absolute Maximum Ratings (Note)}

    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    DM54LS and 54LS
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    DM74LS
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    Storage Temperature Range
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54LS365A} & \multicolumn{3}{|c|}{DM74LS365A} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -1 & & & -2.6 & mA \\
    \hline \(\mathrm{lOL}^{\text {l }}\) & Low Level Output Current & & & 12 & & & 24 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline V OH & High Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\
    & V_{\mathrm{IL}}=\operatorname{Max}, V_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 2.4 & 3.4 & & V \\
    \hline \multirow[t]{3}{*}{VOL} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\
    & V_{I L}=\operatorname{Max}, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{IOL}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline 1 IH & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{3}{*}{ILL} & \multirow[t]{3}{*}{Low Level Input Current} & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{I}}=0.5 \mathrm{~V} \\
    & \text { (Note 4) }
    \end{aligned}
    \] & A Input & & & -20 & \(\mu \mathrm{A}\) \\
    \hline & & \[
    \begin{aligned}
    & V_{c c}=\text { Max, } V_{1}=0.4 V \\
    & \text { (Note 5) }
    \end{aligned}
    \] & A Input & & & -0.4 & \multirow[t]{2}{*}{mA} \\
    \hline & & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & \(\overline{\mathrm{G}}\) Input & & & -0.4 & \\
    \hline lozh & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=2.4 V \\
    & V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
    \end{aligned}
    \]} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline lozl & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=0.4 V \\
    & V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
    \end{aligned}
    \]} & & & -20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -20 & & \(-100\) & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 3)} & & 14 & 24 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: \(\mathrm{I}_{\mathrm{CC}}\) is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5 V .
    Note 4: Both \(\bar{G}\) inputs are at 2V.
    Note 5: Both \(\overline{\mathrm{G}}\) inputs at 0.4 V .

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(R_{L}=667 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(C_{L}=50 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(C_{L}=150 \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & & 16 & & 25 & ns \\
    \hline tPHL & Propagation Delay Time High to Low Level Output & & 16 & & 25 & ns \\
    \hline \({ }_{\text {tPZH }}\) & Output Enable Time to High Level Output & & 30 & & 40 & ns \\
    \hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level Output & & 30 & & 40 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time from High Level Output (Note 6) & & 20 & & & ns \\
    \hline \(t_{\text {PLZ }}\) & Output Disable Time from Low Level Output (Note 6) & & 20 & & & ns \\
    \hline
    \end{tabular}

    Note 6: \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\).

    \section*{54LS366A/DM74LS366A} Hex TRI-STATE \({ }^{\circledR}\) Inverting Buffers

    \section*{General Description}

    This device contains six independent gates each of which performs an inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output
    transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

    \section*{Connection Diagram}
    

    TL/F/6428-1
    Order Number 54LS366ADMQB, 54LS366AFMQB, 54LS366ALMQB, DM74LS366AM or DM74LS366AN See NS Package Number E20A, J16A, M16A, N16E or W16A

    \section*{Function Table}
    \begin{tabular}{|c|c|c|c|}
    \hline \multicolumn{4}{|c|}{\(\mathbf{Y}=\overline{\mathbf{A}}\)} \\
    \hline \multicolumn{3}{|c|}{Inputs} & Output \\
    \hline G1 & G2 & A & Y \\
    \hline H & X & X & \(\mathrm{Hi}-\mathrm{Z}\) \\
    \hline X & H & X & \(\mathrm{Hi}-\mathrm{Z}\) \\
    \hline L & L & L & H \\
    \hline L & L & H & L \\
    \hline
    \end{tabular}
    \(\mathrm{H}=\) High Logic Level
    \(L=\) Low Logic Level
    \(X=\) Either Low or High Logic Level
    Hi-Z = TRI-STATE (Outputs are disabled)

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

    \section*{Supply Voltage}

    Input Voltage
    7V
    Operating Free Air Temperature Range
    DM54LS
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    Storage Temperature Range

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS366A} & \multicolumn{3}{|c|}{DM74LS366A} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -1 & & & -2.6 & mA \\
    \hline \(\mathrm{lOL}^{\text {l }}\) & Low Level Output Current & & & 12 & & & 24 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 2.4 & 3.4 & & V \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\text {OL }}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\
    & V_{I L}=\operatorname{Max}, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{IOL}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current @ Max Input Voltage} & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}\) & DM74 & & & \multirow[t]{2}{*}{0.1} & \multirow[t]{2}{*}{mA} \\
    \hline & & \(V_{C C}=M a x, V_{1}=10.0 \mathrm{~V}\) & 54LS & & & & \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\) & & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \[
    \begin{aligned}
    & V_{C C}=M a x, V_{1}=0.5 V \\
    & \text { (Note 4) }
    \end{aligned}
    \] & A Input & & & -20 & \(\mu \mathrm{A}\) \\
    \hline & & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{~V}_{1}=0.4 \mathrm{~V} \\
    & \text { (Note 5) }
    \end{aligned}
    \] & A Input & & & -0.4 & \multirow[t]{2}{*}{mA} \\
    \hline & & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & \(\overline{\mathrm{G}}\) Input & & & -0.4 & \\
    \hline lozh & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M a x, V_{O}=2.4 V \\
    & V_{I H}=\operatorname{Min}, V_{I L}=M a x
    \end{aligned}
    \]} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline Iozl & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & -20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & 54LS & -30 & & \(-130\) & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}\) (Note 3)} & & 12 & 21 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: \(\mathrm{I}_{\mathrm{CC}}\) is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5 V .
    Note 4: Both \(\overline{\mathrm{G}}\) inputs are at 2 V .
    Note 5: Both \(\overline{\mathrm{G}}\) inputs at 0.4 V .

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{2}{|c|}{54LS} & \multicolumn{2}{|c|}{DM74LS} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}\)} & \multicolumn{2}{|r|}{\[
    \begin{aligned}
    & C_{\mathrm{L}}=150 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=667 \Omega \\
    & \hline
    \end{aligned}
    \]} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & & 12 & & 25 & ns \\
    \hline tPHL & Propagation Delay Time High to Low Level Output & & 22 & & 25 & ns \\
    \hline \(t_{\text {PZH }}\) & Output Enable Time to High Level Output & & 24 & & 35 & ns \\
    \hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level Output & & 30 & & 40 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time from High Level Output (Note 6) & & 25 & & & ns \\
    \hline \(t_{\text {PLZ }}\) & Output Disable Time from Low Level Output (Note 6) & & 20 & & & ns \\
    \hline
    \end{tabular}

    Note 6: \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\).

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    \section*{54LS367A/DM54LS367A/DM74LS367A Hex TRI-STATE \({ }^{\circledR}\) Buffers}

    \section*{General Description}

    This device contains six independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility
    that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

    \section*{Features}
    - Alternate military/aerospace device (54LS367A) is available. Contact a National Semiconductor sales office/distributor for specifications.

    \section*{Connection Diagram}

    Dual-In-Line Package
    

    TL/F/6429-1
    Order Number 54LS367ADMQB, 54LS367AFMQB, 54LS367ALMQB, DM54LS367AJ, DM54LS367AW, DM74LS367AM or DM74LS367AN See NS Package Number E20A, J16A, M16A, N16E or W16A

    Function Table
    \begin{tabular}{|c|c|c|}
    \multicolumn{3}{c|}{\(\mathbf{Y}=\mathbf{A}\)} \\
    \hline \multicolumn{2}{|c|}{ Inputs } & Output \\
    \hline \(\mathbf{A}\) & \(\overline{\mathbf{G}}\) & \(\mathbf{Y}\) \\
    \hline L & L & L \\
    H & L & H \\
    X & H & \(\mathrm{Hi}-\mathrm{Z}\) \\
    \hline
    \end{tabular}

    H = High Logic Level
    L = Low Logic Level
    \(X=\) Either Low or High Logic Level
    \(\mathrm{Hi}-\mathrm{Z}=\) TRI-STATE (Outputs are disabled)

    \section*{Absolute Maximum Ratings (Note)}

    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage 7V
    Operating Free Air Temperature Range
    DM54LS
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    Storage Temperature Range

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54LS367A} & \multicolumn{3}{|c|}{DM74LS367A} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{\text {l }}\) & High Level Output Current & & & -1 & & & -2.6 & mA \\
    \hline lOL & Low Level Output Current & & & 12 & & & 24 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 2.4 & 3.4 & & V \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\text {OL }}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O L}=M a x \\
    & V_{I L}=M a x, V_{I H}=M i n
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{IOL}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(I_{1 H}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{l}}=0.5 \mathrm{~V} \\
    & \text { (Note 4) }
    \end{aligned}
    \] & A Input & & & -20 & \(\mu \mathrm{A}\) \\
    \hline & & \[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Max}, \mathrm{~V}_{1}=0.4 \mathrm{~V} \\
    & \text { (Note 5) }
    \end{aligned}
    \] & A Input & & & -0.4 & \multirow[t]{2}{*}{mA} \\
    \hline & & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & \(\overline{\mathrm{G}}\) Input & & & -0.4 & \\
    \hline IOZH & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=2.4 V \\
    & V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
    \end{aligned}
    \]} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline IozL & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M a x, V_{O}=0.4 V \\
    & V_{I H}=\operatorname{Min}, V_{I L}=M a x
    \end{aligned}
    \]} & & & -20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -20 & & \(-100\) & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}\) (Note 3)} & & 14 & 24 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: \(\mathrm{ICC}_{\mathrm{C}}\) is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5 V .
    Note 4: Both \(\overline{\mathrm{G}}\) inputs are at 2V.
    Note 5: Both \(\overline{\mathrm{G}}\) inputs at 0.4 V .

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=667 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=150 \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & & 16 & & 25 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & & 16 & & 25 & ns \\
    \hline tpZH & Output Enable Time to High Level Output & & 30 & & 40 & ns \\
    \hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level Output & & 30 & & 40 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time from High Level Output (Note 6) & & 20 & & & ns \\
    \hline \(t_{\text {PLZ }}\) & Output Disable Time from Low Level Output (Note 6) & & 20 & & & ns \\
    \hline
    \end{tabular}

    Note 6: \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\).

    \section*{54LS368A/DM54LS368A/DM74LS368A Hex TRI-STATE® Inverting Buffers}

    \section*{General Description}

    This device contains six independent gates each of which performs an inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two
    outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

    \section*{Features}
    - Alternate Military/Aerospace device (54LS368) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

    \section*{Connection Diagram}

    Dual-In-Line Package
    

    TL/F/6430-1
    Order Number 54LS368ADMQB, 54LS368AFMQB, 54LS368ALMQB, DM54LS368AJ, DM54LS368AW, DM74LS368AM or DM74LS368AN See NS Package Number E20A, J16A, M16A, N16E or W16A
    Function Table
    \begin{tabular}{|c|c|c|}
    \hline \multicolumn{3}{c|}{\(\mathbf{Y}=\overline{\mathbf{A}}\)} \\
    \hline \multicolumn{2}{|c|}{ Inputs } & Output \\
    \hline \(\mathbf{A}\) & \(\overline{\mathbf{G}}\) & \(\mathbf{Y}\) \\
    \hline L & L & H \\
    \(H\) & L & L \\
    X & H & \(\mathrm{Hi}-\mathrm{Z}\) \\
    \hline
    \end{tabular}
    \(H=\) High Logic Level
    L = Low Logic Level
    \(X=\) Either Low or High Logic Level
    \(\mathrm{Hi}-\mathrm{Z}=\) TRI-STATE (Outputs are disabled)

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    \(7 V\)
    Operating Free Air Temperature Range
    ```

    DM54LS and 54LS
    DM74LS
    Storage Temperature Range

    ```
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54LS368A} & \multicolumn{3}{|c|}{DM74LS368A} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -1 & & & -2.6 & mA \\
    \hline lOL & Low Level Output Current & & & 12 & & & 24 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 2.4 & 3.4 & & V \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{I}_{\mathrm{OL}}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{IH}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{1}=0.5 V \\
    & \text { (Note 4) }
    \end{aligned}
    \] & A Input & & & -20 & \(\mu \mathrm{A}\) \\
    \hline & & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{l}}=0.4 \mathrm{~V} \\
    & \text { (Note 5) }
    \end{aligned}
    \] & A Input & & & -0.4 & \multirow[t]{2}{*}{mA} \\
    \hline & & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & \(\overline{\mathrm{G}}\) Input & & & -0.4 & \\
    \hline lozh & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M a x, V_{O}=2.4 V \\
    & V_{I H}=M i n, V_{I L}=M a x
    \end{aligned}
    \]} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline Iozl & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & -20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}\) (Note 3)} & & 12 & 21 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: ICC is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5 V .
    Note 4: Both \(\overline{\mathrm{G}}\) inputs are at 2 V .
    Note 5: Both \(\overline{\mathrm{G}}\) inputs at 0.4 V .

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=667 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(C_{L}=150 \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & & 15 & & 25 & ns \\
    \hline \({ }^{\text {t }}\) PHL & Propagation Delay Time High to Low Level Output & & 18 & & 25 & ns \\
    \hline \(t_{\text {PZH }}\) & Output Enable Time to High Level Output & & 30 & & 35 & ns \\
    \hline tPZL & Output Enable Time to Low Level Output & & 30 & & 40 & ns \\
    \hline \(\mathrm{t}_{\text {PHZ }}\) & Output Disable Time from High Level Output (Note 6) & & 20 & & & ns \\
    \hline \(t_{\text {PLZ }}\) & Output Disable Time from Low Level Output (Note 6) & & 20 & & & ns \\
    \hline
    \end{tabular}

    Note 6: \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\).

    \section*{DM54LS373/DM74LS373, 54LS374/DM54LS374/DM74LS374 TRI-STATE \({ }^{\circledR}\) Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops}

    \section*{General Description}

    These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.
    (Continued)

    \section*{Features}
    © Choice of 8 latches or 8 D-type flip-flops in a single package
    - TRI-STATE bus-driving outputs
    © Full parallel-access for loading
    ■ Buffered control inputs
    - P-N-P inputs reduce D-C loading on data lines

    四 Alternate military/aerospace device (54LS374) is available. Contact a National Semiconductor sales office/ distributor for specifications.

    \section*{Connection Diagrams}
    

    General Description (Continued)
    The eight latches of the DM54/74LS373 are transparent Dtype latches meaning that while the enable \((G)\) is high the \(Q\) outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.
    The eight flip-flops of the DM54/74LS374 are edge-triggered D-type flip flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.
    Function Tables
    DM54/74LS373
    \begin{tabular}{|c|c|c|c|}
    \hline \begin{tabular}{c} 
    Output \\
    Control
    \end{tabular} & \begin{tabular}{c} 
    Enable \\
    G
    \end{tabular} & D & Output \\
    \hline L & H & H & H \\
    L & H & L & L \\
    L & L & X & Q \(_{0}\) \\
    H & X & X & Z \\
    \hline
    \end{tabular}

    A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.
    The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

    DM54/74LS374
    \begin{tabular}{|c|c|c|c|}
    \hline \begin{tabular}{c} 
    Output \\
    Control
    \end{tabular} & Clock & D & Output \\
    \hline L & \(\uparrow\) & H & H \\
    L & \(\uparrow\) & L & L \\
    L & L & X & \(\mathrm{Q}_{0}\) \\
    H & X & X & Z \\
    \hline
    \end{tabular}
    \(H=\) High Level (Steady State), \(L=\) Low Level (Steady State), \(X=\) Don't Care
    \(\uparrow=\) Transition from low-to-high level, \(Z=\) High Impedance State
    \(Q_{0}=\) The level of the output before steady-state input conditions were established.

    Logic Diagrams
    DM54/74LS373
    Transparent Latches
    

    DM54/74LS374
    Positive-Edge-Triggered Flip-Flops
    

    TL/F/6431-4
    Absolute Maximum Ratings (See Note)
    If Military/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Storage Temperature Range
    Operating Free Air Temperature Range
    DM54LS and 54LS
    DM74LS

    Recommended Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54LS373} & \multicolumn{3}{|c|}{DM74LS373} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Votage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{\text {l }}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -1 & & & -2.6 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 12 & & & 24 & mA \\
    \hline \multirow[t]{2}{*}{\(t_{W}\)} & \multirow[t]{2}{*}{Pulse Width (Note 2)} & Enable High & 15 & & & 15 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Enable Low & 15 & & & 15 & & & \\
    \hline tsu & \multicolumn{2}{|l|}{Data Setup Time (Notes 1 \& 2)} & 5 \(\downarrow\) & & & 5 \(\downarrow\) & & & ns \\
    \hline \(t_{H}\) & \multicolumn{2}{|l|}{Data Hold Time (Notes 1 \& 2)} & \(20 \downarrow\) & & & 20 \(\downarrow\) & & & ns \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note 1: The symbol ( \(\downarrow\) ) indicates the falling edge of the clock pulse is used for reference.
    Note 2: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

    \section*{'LS373 Electrical Characteristics}
    over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voitage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{V OH} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min} \\
    & \mathrm{IOH}_{\mathrm{OH}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & DM54 & 2.4 & 3.4 & & \multirow{2}{*}{V} \\
    \hline & & & DM74 & 2.4 & 3.1 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\text {OL }}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min} \\
    & \mathrm{IOL}_{\mathrm{OL}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \[
    \begin{aligned}
    & \mathrm{l}_{\mathrm{OL}}=12 \mathrm{~mA} \\
    & \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min} \\
    & \hline
    \end{aligned}
    \] & DM74 & & & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline 1 IH & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline ILL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline lozh & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Max}, V_{\mathrm{O}}=2.7 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline lozl & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=0.4 V \\
    & V_{\mathrm{IH}}=\operatorname{Min}, V_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & -20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\text { Max } \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -50 & & -225 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -50 & & -225 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\) Max} & & 24 & 40 & mA \\
    \hline
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.
    'LS373 Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\)
    (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{\begin{tabular}{l}
    From \\
    (Input) To (Output)
    \end{tabular}} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=667 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=45 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=150 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    \text { Data } \\
    \text { to } \\
    \mathrm{Q}
    \end{gathered}
    \] & & 18 & & 26 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \text { Data } \\
    \text { to } \\
    \mathrm{Q} \\
    \hline
    \end{gathered}
    \] & & 18 & & 27 & ns \\
    \hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & Enable to Q & & 30 & & 38 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Enable to Q & & 30 & & 36 & ns \\
    \hline \(t_{\text {PZH }}\) & Output Enable Time to High Level Output & Output Control to Any Q & & 28 & & 36 & ns \\
    \hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level Output & Output Control to Any Q & & 36 & & 50 & ns \\
    \hline \(t_{\text {PHZ }}\) & \begin{tabular}{l}
    Output Disable \\
    Time from High Level Output (Note 3)
    \end{tabular} & Output Control to Any Q & & 20 & & & ns \\
    \hline \(t_{\text {PLZ }}\) & \begin{tabular}{l}
    Output Disable \\
    Time from Low Level Output (Note 3)
    \end{tabular} & Output Control to Any Q & & 25 & & & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\).
    Recommended Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54LS374} & \multicolumn{3}{|c|}{DM74LS374} & \multirow{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\mathrm{IL}}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.7 & & & 0.8 & V \\
    \hline \({ }_{\mathrm{OH}}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -1 & & & -2.6 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 12 & & & 24 & mA \\
    \hline \({ }_{\text {f CLK }}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & & 35 & 0 & & 35 & MHz \\
    \hline \({ }_{\text {f CLK }}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 3)} & 0 & & 20 & 0 & & 20 & MHz \\
    \hline \multirow[t]{2}{*}{tw} & \multirow[t]{2}{*}{Pulse Width (Note 4)} & Clock High & 15 & & & 15 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Clock Low & 15 & & & 15 & & & \\
    \hline tsu & \multicolumn{2}{|l|}{Data Setup Time (Notes 1 \& 4)} & \(20 \uparrow\) & & & \(20 \uparrow\) & & & ns \\
    \hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Data Hold Time (Notes 1 \& 4)} & \(1 \uparrow\) & & & \(1 \uparrow\) & & & ns \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note 1: The symbol ( \(\uparrow\) ) indicates the rising edge of the clock pulse is used for reference.
    Note 2: \(\mathrm{C}_{\mathrm{L}}=45 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=667 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 3: \(\mathrm{C}_{\mathrm{L}}=150 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=667 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 4: \(T_{A}=25^{\circ} \mathrm{C}\) and \(V_{C C}=5 \mathrm{~V}\).

    \section*{'LS374 Electrical Characteristics}
    over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Min} \\
    & \mathrm{IOH}_{\mathrm{OH}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.4 & 3.4 & & \\
    \hline & & & DM74 & 2.4 & 3.1 & & V \\
    \hline \multirow[t]{3}{*}{Vol} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M i n \\
    & l_{\mathrm{OL}}=M a x \\
    & V_{\mathrm{IL}}=\operatorname{Max} \\
    & V_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \\
    \hline & & & DM74 & & 0.35 & 0.5 & V \\
    \hline & & \[
    \begin{aligned}
    & \mathrm{I}_{\mathrm{OL}}=12 \mathrm{~mA} \\
    & \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}
    \end{aligned}
    \] & DM74 & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \(1 / 2\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline IOZH & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=2.7 V \\
    & V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
    \end{aligned}
    \]} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline lozl & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=0.4 V \\
    & V_{\mathrm{IH}}=\operatorname{Min}, V_{I L}=\operatorname{Max}
    \end{aligned}
    \]} & & & -20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Max} \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -50 & & -225 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -50 & & -225 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 27 & 45 & mA \\
    \hline
    \end{tabular}
    'LS374 Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\)
    (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(R_{L}=667 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(C_{L}=45 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(C_{L}=150 \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & 35 & & 20 & & MHz \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & & 28 & & 32 & ns \\
    \hline tPHL & Propagation Delay Time High to Low Level Output & & 28 & & 38 & ns \\
    \hline \(t_{\text {PZH }}\) & Output Enable Time to High Level Output & & 28 & & 44 & ns \\
    \hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level Output & & 28 & & 44 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time from High Level Output (Note 3) & & 20 & & & ns \\
    \hline tplz & Output Disable Time from Low Level Output (Note 3) & & 25 & & & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\).

    \section*{54LS375/DM74LS375}

    4-Bit Latch

    \section*{General Description}

    The 'LS375 is a 4-bit D-type latch for use as temporary storage for binary information between processing units and input/output or indicator units. When its Enable ( E ) input is HIGH, a latch is transparent, i.e., the Q output will follow the
    \(D\) input each time it changes. When \(E\) is LOW a latch stores the last valid data present on the \(D\) input preceding the HIGH-to-LOW transition of E. The 'LS375 is functionally identical to the 'LS75 except for the corner power pins.

    \section*{Connection Diagram}
    

    \section*{Logic Symbol}

    TL/F/9830-2
    \(V_{C C}=\operatorname{Pin} 16\)
    GND \(=\operatorname{Pin} 8\)
    TL/F/9830-1
    Order Number 54LS375DMQB, 54LS375FMQB, DM74LS375M or DM74LS375N

    See NS Package Number
    J16A, M16A, N16E or W16A
    \begin{tabular}{|l|l|}
    \hline Pin Name & \multicolumn{1}{c|}{ Description } \\
    \hline D1-D4 & Data Inputs \\
    E1,2 & Latches 1, 2 Enable Inputs \\
    E3,4 & Latches 3, 4 Enable Inputs \\
    Q1-Q4 & Latch Outputs \\
    \(\overline{\text { Q1-Q4 }}\) & Complementary Latch Outputs \\
    \hline
    \end{tabular}
    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for avallability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    \begin{tabular}{lr}
    54 LS & \\
    DM74LS & 10 V \\
    Storage Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}\(\quad-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS375} & \multicolumn{3}{|c|}{DM74LS375} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L})
    \end{aligned}
    \] & Setup Time HIGH or LOW
    \[
    D_{n} \text { to } E_{n}
    \] & 20 & & & 20 & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L)
    \end{aligned}
    \] & Hold Time HIGH or LOW
    \[
    D_{n} \text { to } E_{n}
    \] & 0 & & & 0 & & & ns \\
    \hline \(t_{w}(\mathrm{H})\) & \(\mathrm{E}_{\mathrm{n}}\) Pulse Width HIGH & 20 & & & 15 & & & ns \\
    \hline
    \end{tabular}

    \section*{Electrical Characteristics}

    Over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, l_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min}, I_{O H}=\text { Max, } \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & 54LS & 2.5 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max}, \\
    & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current @ Max Input Voltage} & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=10 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline & & & Enable Input & & & 0.4 & mA \\
    \hline \multirow[t]{2}{*}{\(\mathrm{IIH}^{\text {H }}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline & & & Enable Input & & & 80 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{ILL} & \multirow[t]{2}{*}{Low Level Input Current} & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline & & & Enable Input & & & -1.2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & & 12 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    Switching Characteristics
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{2}{|c|}{54LS/DM74LS} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \\
    \hline & & Min & Max & \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay
    \[
    D_{n} \text { to } Q_{n}
    \] & & \[
    \begin{array}{r}
    27 \\
    23 \\
    \hline
    \end{array}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay
    \[
    D_{n} \text { to } \bar{Q}_{n}
    \] & & \[
    \begin{aligned}
    & 20 \\
    & 15 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(E_{n}\) to \(Q_{n}\) & & \[
    \begin{aligned}
    & 27 \\
    & 25 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(t_{\text {PHL }}\)
    \end{tabular} & Propagation Delay \(E_{n}\) to \(\bar{Q}_{n}\) & & \[
    \begin{aligned}
    & 30 \\
    & 18 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}

    \section*{Truth Table (Each Latch)}
    \begin{tabular}{|c|c|}
    \hline \(\mathbf{t}_{\mathbf{n}}\) & \(\mathbf{t}_{\mathbf{n}+\mathbf{1}}\) \\
    \hline\(D\) & \(Q\) \\
    \hline\(H\) & \(H\) \\
    \(L\) & \(L\) \\
    \hline
    \end{tabular}
    \(t_{n}=\) Bit time before Enable negative going transition.
    \(\mathrm{t}_{\mathrm{n}+1}=\) Bit time after Enable negative going transition.
    \(H=H I G H\) Voltage Level
    L = LOW Voltage Level

    \section*{Logic Diagram (1/4 of diagram shown)}
    

    TL/F/9830-3

    \section*{54LS377/DM74LS377}

    \section*{Octal D Flip-Flop with Common Enable and Clock}

    \section*{General Description}

    The 'LS377 is an 8 -bit register built using advanced low power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common input enable. The device is packaged in the space-saving ( 0.3 inch row spacing) 20-pin package.

    \section*{Features}
    - 8-bit high speed parallel registers
    - Positive edge-triggered D-type flip-flops
    - Fully buffered common clock and enable inputs

    \section*{Connection Diagram}

    Dual-In-Line Package
    

    TL/F/9831-1
    Order Number 54LS377DMQB, 54LS377FMQB,
    54LS377LMQB, DM74LS377WM or DM74LS377N See NS Package Number
    E20A, J20A, M20B, N20A or W20A
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
    \hline \(\bar{E}\) & Enable Input (Active LOW) \\
    D0-D7 & Data Inputs \\
    CP & Clock Pulse Input (Active Rising Edge) \\
    Q0-Q7 & Flip-Flop Outputs \\
    \hline
    \end{tabular}

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range

    54LS
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    Recommended Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS377} & \multicolumn{3}{|c|}{DM74LS377} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \({ }^{1} \mathrm{OH}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & t_{s}(H) \\
    & t_{s}(L) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW
    \[
    D_{n} \text { to CP }
    \] & \[
    \begin{array}{r}
    20 \\
    20 \\
    \hline
    \end{array}
    \] & & & \[
    \begin{aligned}
    & 10 \\
    & 10 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L)
    \end{aligned}
    \] & Hold Time HIGH or LOW \(D_{n}\) to CP & \[
    \begin{aligned}
    & 5.0 \\
    & 5.0
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 5.0 \\
    & 5.0
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{\mathbf{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW \(\bar{E}\) to CP & \[
    \begin{array}{r}
    10 \\
    20 \\
    \hline
    \end{array}
    \] & & & \[
    \begin{aligned}
    & 10 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L)
    \end{aligned}
    \] & Hold Time HIGH or LOW \(\bar{E}\) to CP & \[
    \begin{aligned}
    & 5.0 \\
    & 5.0
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 5.0 \\
    & 5.0 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{w}(H) \\
    & t_{w}(L) \\
    & \hline
    \end{aligned}
    \] & CP Pulse Width HIGH or LOW & \[
    \begin{aligned}
    & 20 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 20 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \begin{tabular}{l}
    Typ \\
    (Note 1)
    \end{tabular} & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M i n, l_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & 54LS & 2.5 & & & V \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\text {OL }}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \\
    \hline & & & DM74 & & 0.35 & 0.5 & V \\
    \hline & & \(\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=10 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(I_{\mathbb{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\)} & & & 20.0 & \(\mu \mathrm{A}\) \\
    \hline 1 IL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & 54LS & -20 & & -100 & mA \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & & 28 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multicolumn{5}{|l|}{\begin{tabular}{l}
    Switching Characteristics \\
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
    \end{tabular}} \\
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \(\mathrm{f}_{\text {max }}\) & Maximum Clock Frequency & 30 & & MHz \\
    \hline \[
    t_{\text {PLH }}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & Propagation Delay CP to \(Q_{n}\) & & \[
    \begin{aligned}
    & 25 \\
    & 25
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}

    \section*{Functional Description}

    The 'LS377 consists of eight edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable input ( \(\overline{\mathrm{E}}\) ) are common to all flip-flops.
    When \(\bar{E}\) is LOW, new data is entered into the register on the next LOW-to-HIGH transition of CP. When \(\bar{E}\) is HIGH, the register will retain the present data independent of the CP.

    \section*{Logic Symbol}

    \section*{Logic Diagram}
    

    \section*{Truth Table}
    \begin{tabular}{|c|c|c|c|}
    \hline \multicolumn{3}{|c|}{ Inputs } & Output \\
    \hline \(\bar{E}\) & CP & \(\mathbf{D}_{\mathbf{n}}\) & \(\mathbf{Q}_{\boldsymbol{n}}\) \\
    \hline\(H\) & \(X\) & X & No Change \\
    L & \(\Gamma\) & H & H \\
    L & - & L & L \\
    \hline
    \end{tabular}
    \(H=\) HIGH Voltage Level
    \(L=\) LOW Voltage Level
    \(X=\) Immaterial
    

    \section*{54LS378/DM74LS378 Parallel D Register with Enable}

    \section*{General Description}

    The 'LS378 is a 6-bit register with a buffered common enable. This device is similar to the 'LS174, but with common Enable rather than common Master Reset.

    \section*{Features}

    ■ 6-bit high speed parallel register
    - Positive edge-triggered D-type inputs
    - Fully buffered common clock and enable inputs
    - Input clamp diodes limit high speed termination effects
    - Full TTL and CMOS compatible

    \section*{Connection Diagram}

    Logic Symbol

    \section*{Dual-In-Line Package}
    

    TL/F/9832-1
    Order Number 54LS378DMQB, 54LS378FMQB, DM74LS378M or DM74LS378N
    See NS Package Number J16A, M16A, N16E or W16A
    

    TL/F/9832-2
    \(V_{C C}=\operatorname{Pin} 16\)
    GND \(=\operatorname{Pin} 8\)
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
    \hline\(\overline{\mathrm{E}}\) & Enable Input (Active LOW) \\
    D0-D5 & Data Inputs \\
    CP & Clock Pulse Input (Active Rising Edge) \\
    Q0-Q5 & Flip-Flop Outputs \\
    \hline
    \end{tabular}

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    \begin{tabular}{lr} 
    54LS & \(-54^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    Recommended Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS378} & \multicolumn{3}{|c|}{DM74LS378} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{H}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \(\mathrm{l}_{\mathrm{OH}}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline loL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \(\mathrm{t}_{\text {s }}(\mathrm{H})\) & Setup Time HIGH, \(D_{n}\) to CP & 20 & & & 20 & & & ns \\
    \hline \(t_{n}(H)\) & Hold Time HIGH, \(\mathrm{D}_{\mathrm{n}}\) to CP & 5.0 & & & 5.0 & & & ns \\
    \hline \(t_{s}(L)\) & Setup Time LOW, \(\mathrm{D}_{\mathrm{n}}\) to CP & 20 & & & 20 & & & ns \\
    \hline \(t_{h}(L)\) & Hold Time LOW, \(\mathrm{D}_{\mathrm{n}}\) to CP & 5.0 & & & 5.0 & & & ns \\
    \hline \(\mathrm{t}_{\mathrm{s}}(\mathrm{H})\) & Setup Time HIGH, \(\overline{\mathrm{E}}\) to CP & 30 & & & 30 & & & ns \\
    \hline \(t_{h}(\mathrm{H})\) & Hold Time HIGH, E to CP & 5.0 & & & 5.0 & & & ns \\
    \hline \(t_{s}(L)\) & Setup Time LOW, Ē to CP & 30 & & & 30 & & & ns \\
    \hline \(t_{n}(L)\) & Hold Time LOW, E to CP & 5.0 & & & 5.0 & & & ns \\
    \hline \(t_{w}(H)\) & CP Pulse Width HIGH & 20 & & & 20 & & & ns \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, l_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & 54LS & 2.5 & & & V \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\text {OL }}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\text { Max }, \\
    & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}\), & DM74 & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=10 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20.0 & \(\mu \mathrm{A}\) \\
    \hline \(1 / 2\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\text { Max } \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max} D_{n} ; \bar{E}=G N D, C P=\Omega\)} & & & 22 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{Switching Characteristics}
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\(2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \(\mathrm{f}_{\text {max }}\) & Maximum Clock Frequency & 30 & & MHz \\
    \hline \[
    t_{\text {PLH }}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & Propagation Delay CP to \(Q_{n}\) & & \[
    \begin{aligned}
    & 27 \\
    & 27
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}

    \section*{Functional Description}

    The 'LS378 consists of eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable \((\bar{E})\) inputs are common to all flip-flops.
    When the \(\bar{E}\) input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the \(\bar{E}\) input is HIGH the register will retain the present data independent of the CP input.

    \section*{Truth Table}
    \begin{tabular}{|c|c|c|c|}
    \hline \multicolumn{3}{|c|}{ Inputs } & Output \\
    \hline \(\bar{E}\) & CP & \(\mathbf{D}_{\mathbf{n}}\) & \(\mathbf{Q}_{\mathbf{n}}\) \\
    \hline\(H\) & \(\Gamma\) & \(X\) & No change \\
    \(L\) & & \(H\) & \(H\) \\
    \(L\) & & \(L\) & \(L\) \\
    \hline
    \end{tabular}

    \footnotetext{
    \(H=\) HIGH Voltage Level
    L = LOW Voltage Level
    \(X=\) Immaterial
    }

    Logic Diagram
    

    \section*{54LS379/DM74LS379 Quad Parallel Register with Enable}

    \section*{General Description}

    The LS379 is a 4-bit register with buffered common Enable. This device is similar to the LS175 but features the common Enable rather than common Master Reset.

    \section*{Features}

    ■ Edge-triggered D-type inputs
    - Buffered positive edge-triggered clock
    - Buffered common enable input
    - True and complement outputs

    \section*{Connection Diagram}
    

    TL/F/10186-1
    Order Number 54LS379DMQB, 54LS379FMQB, 54LS379LMQB, DM74LS379M or DM74LS379N

    See NS Package Number E20A, J16A, M16A, N16E or W16A

    \section*{Logic Symbol}
    

    TL/F/10186-2
    \(V_{C C}=\operatorname{Pin} 16\)
    GND \(=\operatorname{Pin} B\)
    \begin{tabular}{|l|l|}
    \hline \begin{tabular}{c} 
    Pin \\
    Names
    \end{tabular} & \multicolumn{1}{c|}{ Description } \\
    \hline\(\overline{\mathrm{E}}\) & Enable Input (Active LOW) \\
    D0-D3 & Data Inputs \\
    CP & Clock Pulse Input (Active Rising Edge) \\
    Q0-Q3 & Flip-Flop Outputs \\
    \(\bar{Q} 0-\bar{Q} 3\) & Complement Outputs \\
    \hline
    \end{tabular}

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    \begin{tabular}{lr} 
    Supply Voltage & 7 V \\
    Input Voltage & 7 V \\
    Operating Free Air Temperature Range & \\
    54 LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS379} & \multicolumn{3}{|c|}{DM74LS379} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \({ }_{\mathrm{OH}}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & t_{s}(H) \\
    & t_{s}(L) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW Dn to CP & 20 & & & 20 & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L) \\
    & \hline
    \end{aligned}
    \] & Hold Time HIGH or LOW Dn to CP & 5 & & & 5 & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{s}(H) \\
    & t_{s}(L) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW \(\bar{E}\) to CP & 25 & & & 25 & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L) \\
    & \hline
    \end{aligned}
    \] & Hold Time HIGH or LOW \(\bar{E}\) to CP & 5 & & & 5 & & & ns \\
    \hline \(\mathrm{t}_{\mathrm{w}}(\mathrm{L})\) & CP Pulse Width LOW & 17 & & & 17 & & & ns \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & 54LS & 2.5 & & & V \\
    \hline & & & DM74 & 2.7 & & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}} \operatorname{Min}, \mathrm{IOL}_{\mathrm{L}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \\
    \hline & & & DM74 & & & 0.5 & V \\
    \hline & & \(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & & 0.4 & \\
    \hline 11 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=10 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline I/L & Low Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & 54LS & -20 & & -100 & mA \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & & 18 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Note more than one output should be shorted at a time, and the duration should not exceed one second.
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for test waveforms and output load)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \(f_{\text {max }}\) & Maximum Clock Frequency & 30 & & MHz \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(t_{\text {PHL }}\)
    \end{tabular} & Propagation Delay CP to Qn & & \[
    \begin{aligned}
    & 27 \\
    & 27
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}

    \section*{Functional Description}

    The LS379 consists of four edge-triggered D-type flip-flops with individual \(D\) inputs and \(Q\) and \(\bar{Q}\) outputs. The Clock (CP) and Enable ( E ) inputs are common to all flip-flops. When the \(\bar{E}\) input is HIGH, the register will retain the present data independent of the CP input. The Dn and E inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed.

    Truth Table
    \begin{tabular}{|c|c|c|cc|}
    \hline \multicolumn{3}{|c|}{ Inputs } & \multicolumn{2}{c|}{ Outputs } \\
    \hline \multicolumn{2}{|c|}{ CP } & Dn & Qn & Qn \\
    \hline H & - & \(X\) & No & No \\
    L & - & \(H\) & Change & Change \\
    L & - & L & L & H \\
    \hline
    \end{tabular}

    H \(=\) HIGH Voltage Level
    L = LOW Voltage Level
    \(\mathrm{X}=\) Immaterial

    \section*{Logic Diagram}
    

    National Semiconductor

    \section*{DM54LS380/74LS380}

    Multifunction Octal Register

    \section*{General Description}

    The 'LS380 is an 8-bit synchronous register with parallel load, load complement, preset, clear, and hold capacity. Four control inputs ( \(\overline{\mathrm{LD}}, \mathrm{POL}, \overline{\mathrm{CLR}}, \overline{\mathrm{PR}}\) ) provide one of four operations which occur synchronously on the rising edge of the clock (CK). The LS380 combines the features of the LS374, LS377, LS273 and LS534 into a single 300 mil wide package.
    The LOAD operation loads the inputs ( \(D_{7}-D_{0}\) ) into the output register \(\left(Q_{7}-Q_{0}\right)\), when POL is HIGH, or loads the compliment of the inputs when POL is LOW. The CLEAR operation resets the output register to all LOWs. The PRESET operation presets the output register to all HIGHs. The HOLD operation holds the previous value regardless of clock transitions. CLEAR overrides PRESET, PRESET overrides LOAD, and LOAD overrides HOLD.

    The output register \(\left(Q_{7}-Q_{0}\right)\) is enabled when \(\overline{O E}\) is LOW, and disabled ( \(\mathrm{HI}-\mathrm{Z}\) ) when \(\overline{\mathrm{OE}}\) is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

    \section*{Features/Benefits}
    - Octal Register for general purposes interfacing applications
    - 8 bits match byte boundaries
    - Bus-structured pinout
    - 24-pin SKINNYDIP saves space
    - TRI-STATE \({ }^{\circledR}\) outputs
    - Low current PNP inputs reduce loading

    \section*{Connection Diagram}
    

    \section*{Standard Test Load}
    

    TL/L/8339-2

    Function Table
    \begin{tabular}{|l|c|c|c|c|c|c|c|l|}
    \hline\(\overline{\text { OC }}\) & CLK & \(\overline{\text { CLR }}\) & \(\overline{\text { PR }}\) & \(\overline{\text { LD }}\) & POL & D7-D0 & Q7-Q0 & Operation \\
    \hline H & X & X & X & X & X & X & Z & HI-Z \\
    L & \(\uparrow\) & L & X & X & X & X & L & CLEAR \\
    L & \(\uparrow\) & H & L & X & X & X & H & PRESET \\
    L & \(\uparrow\) & H & H & H & X & X & Q & HOLD \\
    L & \(\uparrow\) & H & H & L & H & D & D & LOAD true \\
    L & \(\uparrow\) & H & H & L & L & D & \(\bar{D}\) & LOAD comp \\
    \hline
    \end{tabular}

    \section*{Absolute Maximum Ratings}

    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage \(\mathrm{V}_{\mathrm{CC}}\) \(7 V\)
    Input Voltage
    5.5 V

    Off-State Output Voltage
    5.5 V

    Storage Temperature
    \(-65^{\circ}\) to \(+150^{\circ} \mathrm{C}\)

    \section*{Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|r|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(\mathrm{V}_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Operating Free-Air Temperature} & -55 & & 125* & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \multirow[t]{2}{*}{\(t_{\text {w }}\)} & \multirow[t]{2}{*}{Width of Clock} & High & 40 & & & 40 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Low & 35 & & & 35 & & & \\
    \hline \(\mathrm{t}_{\text {SU }}\) & \multicolumn{2}{|l|}{Set-Up Time} & 60 & & & 50 & & & \multirow[t]{2}{*}{ns} \\
    \hline \(t_{h}\) & \multicolumn{2}{|l|}{Hold Time} & 0 & -15 & & 0 & -15 & & \\
    \hline
    \end{tabular}
    *Case temperature
    Electrical Characteristics Over Operating Conditions
    
    * No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second
    \(\dagger\) All typical values are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V} . \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\)
    Switching Characteristics Over Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multirow[t]{2}{*}{Test Conditions (See Test Load)} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow{2}{*}{Units} \\
    \hline & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \\
    & \mathrm{R}_{1}=200 \Omega
    \end{aligned}
    \]} & 10.5 & & & 12.5 & & & MHz \\
    \hline tpp & Clock to Q & & & 20 & 35 & & 20 & 30 & ns \\
    \hline tpzX & Output Enable Delay & \multirow[t]{2}{*}{\(\mathrm{R}_{2}=390 \Omega\)} & & 35 & 55 & & 35 & 45 & ns \\
    \hline tpxz & Output Disable Delay & & & 35 & 55 & & 35 & 45 & ns \\
    \hline
    \end{tabular}
    

    \section*{DM54LS380A/DM74LS380A Multifunction Octal Register}

    \section*{General Description}

    The 'LS380A is an 8-bit synchronous register with parallel load, load complement, preset, clear and hold capacity. Four control inputs ( \(\overline{\mathrm{LD}}, \mathrm{POL}, \overline{\mathrm{CLR}}, \overline{\mathrm{PR}}\) ) provide one of four operations which occur synchronously on the rising edge of the clock (CK). The 'LS380A combines the features of the 'LS374, 'LS377, 'LS273 and 'LS534 into a single 300 mil wide package.
    The LOAD operation loads the inputs (D7-D0) into the output register (Q7-Q0), when POL is HIGH, or loads the compliment of the inputs when POL is LOW. The CLEAR operation resets the output register to all LOWs. The PRESET operation presets the output register to all HIGHs. The HOLD operation holds the previous value regardless of clock transitions. CLEAR overrides PRESET, PRESET overrides LOAD, and LOAD overrides HOLD.

    The output register (Q7-Q0) is enabled when \(\overline{O E}\) is LOW and disabled ( \(\mathrm{HI}-\mathrm{Z}\) ) when \(\overline{\mathrm{OE}}\) is HIGH. The output drivers will sink 24 mA required for many bus interface standards.

    \section*{Features}
    - Octal Register for general purpose interfacing applications
    ■ 8 bits match byte boundaries
    - Low current PNP inputs reduce loading
    - Bus-structured pinout
    - TRI-STATE \({ }^{\circledR}\) outputs
    - 24-pin SKINNYDIP saves space

    Connection Diagram
    

    TL/L/10229-1
    Order Number DM54LS380AJ, DM74LS380AJ, DM74LS380AN or DM74LS380AV See NS Package Number J24F, N24C or V28A

    \section*{Function Table}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline OC & CLK & \(\overline{\text { CLR }}\) & \(\overline{\mathbf{P R}}\) & \(\overline{\text { LD }}\) & POL & D7-D0 & Q7-Q0 & Operation \\
    \hline H & X & X & \(X\) & X & X & X & Z & HI-Z \\
    \hline L & \(\uparrow\) & L & X & \(x\) & X & X & L & CLEAR \\
    \hline L & \(\uparrow\) & H & L & X & X & X & H & PRESET \\
    \hline L & \(\uparrow\) & H & H & H & X & X & Q & HOLD \\
    \hline L & \(\uparrow\) & H & H & L & H & D & D & LOAD true \\
    \hline L & \(\uparrow\) & H & H & L & L & D & \(\overline{\text { D }}\) & LOAD comp \\
    \hline
    \end{tabular}

    Absolute Maximum Ratings (Note 1)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    \(\begin{array}{lr}\text { VCC Supply Voltage } & 7 \mathrm{~V} \\ \text { Input Voltage } & 5.5 \mathrm{~V} \\ \text { Off-State Output Voltage } & 5.5 \mathrm{~V}\end{array}\)

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{Milltary} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Operating Free-Air Temperature & -55 & 25 & & 0 & 25 & 75 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \(\mathrm{T}_{\mathrm{C}}\) & Operating Case Temperature & & & 125 & & & & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics Series 24A Over Recommended Operating Temperature Range
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{3}{|c|}{Test Conditions} & Min & Typ & Max & Units \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & \multicolumn{3}{|l|}{(Note 2)} & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & \multicolumn{3}{|l|}{(Note 2)} & & & 0.8 & V \\
    \hline \(V_{\text {IC }}\) & Input Clamp Voltage & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{II}=-18 \mathrm{~mA}\)} & & -0.8 & -1.5 & V \\
    \hline \multirow[t]{2}{*}{V OH} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Min} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}
    \end{aligned}
    \]} & \(\mathrm{l}_{\mathrm{OH}}=-2 \mathrm{~mA}\) & MIL & \multirow[b]{2}{*}{2.4} & \multirow[b]{2}{*}{2.9} & & \multirow[b]{2}{*}{V} \\
    \hline & & & \(\mathrm{l}_{\mathrm{OH}}=-3.2 \mathrm{~mA}\) & COM & & & & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Min} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \\
    & \hline
    \end{aligned}
    \]} & \(\mathrm{l}_{\mathrm{OL}}=12 \mathrm{~mA}\) & MIL & & \multirow[b]{2}{*}{0.3} & \multirow[b]{2}{*}{0.5} & \multirow[b]{2}{*}{V} \\
    \hline & & & \(\mathrm{l}_{\mathrm{OL}}=24 \mathrm{~mA}\) & COM & & & & \\
    \hline l OZH & \multirow[t]{2}{*}{Off-State Output Current (Note 3)} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \\
    & \hline
    \end{aligned}
    \]} & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}\)} & & & 100 & \(\mu \mathrm{A}\) \\
    \hline Iozl & & & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}\)} & & & -100 & \(\mu \mathrm{A}\) \\
    \hline 1 & Maximum Input Current & \multicolumn{3}{|l|}{\(V_{C C}=M a x, V_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{IIH}_{\mathrm{H}}\) & High Level Input Current (Note 3) & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 25 & \(\mu \mathrm{A}\) \\
    \hline I/L & Low Level Input Current (Note 3) & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & -0.04 & -0.25 & mA \\
    \hline los & Output Short-Circuit Current & \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}\) (Note 4)} & \(-30\) & -70 & -130 & mA \\
    \hline ICC & Supply Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 135 & 180 & mA \\
    \hline
    \end{tabular}

    Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at
    these values.
    Note 2: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to
    Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at
    these values.
    Note 2: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to
    Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at
    these values.
    Note 2: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
    Note 3: I/O leakage as the worst case of IOZX or IIX, e.g., IIL and IOZL.
    Note 4: During los measurment, only one output at a time should be grounded. Permanent damage otherwise may result.
    \begin{tabular}{lr} 
    Storage Temperature & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) \\
    ESD Tolerance & \(>1000 \mathrm{~V}\)
    \end{tabular}

    Czap \(=100 \mathrm{pF}\)
    Rzap \(=1500 \Omega\)
    Test Method: Human Body Model
    Test Specification: NSC SOP 5-028

    Switching Characteristics Over Recommended Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Parameter}} & \multirow[t]{2}{*}{Test Conditions} & \multicolumn{3}{|c|}{Milltary} & \multicolumn{3}{|c|}{Commerclal} & \multirow[t]{2}{*}{Units} \\
    \hline & & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline ts & \multicolumn{2}{|l|}{Set-Up Time from Input} & & 40 & 20 & & 30 & 20 & & ns \\
    \hline \multirow[t]{2}{*}{tw} & \multirow[t]{2}{*}{Width of Clock} & High & & 20 & 7 & & 15 & 7 & & ns \\
    \hline & & Low & & 35 & 15 & & 25 & 15 & & ns \\
    \hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Hold Time} & & 0 & -15 & & 0 & -15 & & ns \\
    \hline \(\mathrm{T}_{\text {clk }}\) & \multicolumn{2}{|l|}{Clock to Output} & \(C_{L}=50 \mathrm{pF}\) & & 10 & 25 & & 10 & 15 & ns \\
    \hline \(\mathrm{T}_{\mathrm{pzx}}\) & \multicolumn{2}{|l|}{Output Enable Delay} & \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\) & & 19 & 35 & & 19 & 30 & ns \\
    \hline \(\mathrm{T}_{\mathrm{pxz}}\) & \multicolumn{2}{|l|}{Output Disable Delay} & \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\) & & 15 & 35 & & 15 & 30 & ns \\
    \hline \(f_{\text {max }}\) & \multicolumn{2}{|l|}{Maximum Frequency} & & 15.3 & 32 & & 22.2 & 32 & & MHz \\
    \hline
    \end{tabular}

    Test Load
    

    TL/L/10229-2

    Test Waveforms
    

    Note \(A: V_{T}=1.5 \mathrm{~V}\).
    Note B: \(\mathrm{C}_{\mathrm{L}}\) includes probe and jig capacitance.
    Note C : In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

    Schematic of Inputs and Outputs
    

    TL/L/10229-3
    

    TL/L/10229-5
    

    Octal Register
    

    National Semiconductor

    \section*{DM74LS390 Dual 4-Bit Decade Counter}

    \section*{General Description}

    Each of these monolithic circuits contains eight masterslave flip-flops and additional gating to implement two individual four-bit counters in a single package. The 'LS390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to di-vide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The 'LS390 has parallel outputs from each counter stage so that any submultiple of the input count frequency is available for sys-tem-timing signals.

    \section*{Features}
    - Dual version of the popular 'LS90
    - 'LS390 ... individual clocks for A and B flip-flops provide dual \(\div 2\) and \(\div 5\) counters
    - Direct clear for each 4-bit counter
    - Dual 4-bit version can significantly improve system densities by reducing counter package count by \(50 \%\)
    - Typical maximum count frequency . . . 35 MHz

    ■ Buffered outputs reduce possibility of collector commutation

    \section*{Function Tables}
    

    Order Number DM74LS390M or DM74LS390N See NS Package Number M16A or N16E
    \begin{tabular}{c} 
    BCD Count Sequence \\
    (Each Counter) \\
    (See Note A)
    \end{tabular}
    \begin{tabular}{|c|cccc|}
    \hline \multirow{2}{*}{ Count } & \multicolumn{4}{c|}{ Outputs } \\
    \cline { 2 - 5 } & Q \(_{\mathbf{D}}\) & Q \(_{\mathbf{C}}\) & Q \(_{\mathbf{B}}\) & \(\mathbf{Q}_{\mathbf{A}}\) \\
    \hline 0 & L & L & L & L \\
    1 & L & L & L & H \\
    2 & L & L & H & L \\
    3 & L & L & H & H \\
    4 & L & H & L & L \\
    5 & L & H & L & H \\
    6 & L & H & H & L \\
    7 & L & H & H & H \\
    8 & H & L & L & L \\
    9 & H & L & L & H \\
    \hline
    \end{tabular}

    Bl-Quinary (5-2)
    (Each Counter)
    (See Note B)
    \begin{tabular}{|c|cccc|}
    \hline \multirow{2}{*}{ Count } & \multicolumn{4}{|c|}{ Outputs } \\
    \cline { 2 - 5 } & \(\mathbf{Q}_{\mathbf{A}}\) & \(\mathbf{Q}_{\mathbf{D}}\) & \(\mathbf{Q}_{\mathbf{C}}\) & \(\mathbf{Q}_{\mathbf{B}}\) \\
    \hline 0 & L & L & L & L \\
    1 & L & L & L & H \\
    2 & L & L & H & L \\
    3 & L & L & H & H \\
    4 & L & H & L & L \\
    5 & H & L & L & L \\
    6 & H & L & L & H \\
    7 & H & L & H & L \\
    8 & H & L & H & H \\
    9 & H & H & L & L \\
    \hline
    \end{tabular}

    Note \(A\) : Output \(Q_{A}\) is connected to input \(B\) for \(B C D\) count. Note B: Output \(Q_{D}\) is connected to input \(A\) for Bi-quinary count. Note C: H = High Level, L = Low Level.
    

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM74LS390} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & \\
    \hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{2}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 8 & mA \\
    \hline \multirow[t]{2}{*}{fcLK} & \multirow[t]{2}{*}{Clock Frequency (Note 1)} & \(A\) to \(Q_{A}\) & 0 & & 25 & \multirow[t]{2}{*}{MHz} \\
    \hline & & \(B\) to \(Q_{B}\) & 0 & & 20 & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{f}_{\mathrm{CLK}}\)} & \multirow[t]{2}{*}{Clock Frequency (Note 2)} & \(A\) to \(Q_{A}\) & 0 & & 20 & \multirow[t]{2}{*}{MHz} \\
    \hline & & \(B\) to \(Q_{B}\) & 0 & & 15 & \\
    \hline \multirow[t]{3}{*}{tw} & \multirow[t]{3}{*}{Pulse Width (Note 1)} & A & 20 & & & \multirow{3}{*}{ns} \\
    \hline & & B & 25 & & & \\
    \hline & & Clear High & 20 & & & \\
    \hline \(\mathrm{t}_{\text {REL }}\) & \multicolumn{2}{|l|}{Clear Release Time (Notes 3 \& 4)} & 25 \(\downarrow\) & & & ns \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note 1: \(C_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 2: \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 3: The symbol \((\downarrow)\) indicates the falling edge of the clear pulse is used for reference.
    Note 4: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline VOH & High Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 2.7 & 3.4 & & V \\
    \hline \multirow[t]{2}{*}{VOL} & \multirow[t]{2}{*}{Low Level Output Voltage} & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\
    & V_{I L}=M a x, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & & 0.35 & 0.5 & V \\
    \hline & & \multicolumn{2}{|l|}{\(\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\)} & & 0.25 & 0.4 & \\
    \hline \multirow[t]{3}{*}{1} & \multirow[t]{3}{*}{Input Current @ Max Input Voltage} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{1} \\
    & V_{C C}=\operatorname{Max} \\
    & V_{1}=5.5 \mathrm{~V}
    \end{aligned}
    \]} & Clear & & & 0.1 & \\
    \hline & & & A & & & 0.2 & mA \\
    \hline & & & B & & & 0.4 & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{IIH}^{\text {H}}\)} & \multirow[t]{3}{*}{High Level Input Current} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=2.7 V
    \end{aligned}
    \]} & Clear & & & 20 & \\
    \hline & & & A & & & 40 & \(\mu \mathrm{A}\) \\
    \hline & & & B & & & 80 & \\
    \hline
    \end{tabular}

    \section*{Electrical Characteristics}
    over recommended operating free air temperature range (unless otherwise noted) (Continued)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}\)} & Clear & & & -0.4 & \multirow{3}{*}{mA} \\
    \hline & & & A & & & -1.6 & \\
    \hline & & & B & & & -2.4 & \\
    \hline los & Short Circuit Output Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 2) & DM74 & -20 & & -100 & mA \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 3)} & & 15 & 26 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: \(I_{c c}\) is measured with all outputs open, both CLEAR inputs grounded following momentary connection to 4.5 and all other inputs grounded.

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{\begin{tabular}{l}
    From (Input) \\
    To (Output)
    \end{tabular}} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=\mathbf{2 k} \mathbf{~}\),} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \multirow[t]{2}{*}{\(f_{\text {max }}\)} & \multirow[t]{2}{*}{Maximum Clock Frequency} & \(A\) to \(Q_{A}\) & 25 & & 20 & & \multirow[t]{2}{*}{MHz} \\
    \hline & & \(B\) to \(Q_{B}\) & 20 & & 15 & & \\
    \hline tplH & Propagation Delay Time Low to High Level Output & A to \(Q_{A}\) & & 20 & & 24 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & A to \(Q_{A}\) & & 20 & & 30 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & A to \(Q_{C}\) & & 60 & & 81 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & A to \(Q_{C}\) & & 60 & & 81 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \(B\) to \(Q_{B}\) & & 21 & & 27 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \(B\) to \(Q_{B}\) & & 21 & & 33 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \(B\) to \(Q_{C}\) & & 39 & & 51 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \(B\) to \(Q_{C}\) & & 39 & & 54 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \(B\) to \(Q_{D}\) & & 21 & & 27 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \(B\) to \(Q_{D}\) & & 21 & & 33 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
    Clear to \\
    Any Q
    \end{tabular} & & 39 & & 45 & ns \\
    \hline
    \end{tabular}
    

    \section*{DM74LS393 Dual 4-Bit Binary Counter}

    \section*{General Description}

    Each of these monolithic circuits contains eight masterslave flip-flops and additional gating to implement two individual four-bit counters in a single package. The 'LS393 comprises two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The LS393 has parallel outputs from each counter stage so that any submultiple of the input count freqency is available for system-timing signals.

    \section*{Features}
    - Dual version of the popular 'LS93

    ■ 'LS393 dual 4-bit binary counter with individual clocks
    - Direct clear for each 4-bit counter
    - Dual 4-bit versions can significantly improve system densities by reducing counter package count by \(50 \%\)
    - Typical maximum count frequency 35 MHz
    - Buffered outputs reduce possibility of collector commutation

    \section*{Connection Diagram}
    

    Order Number DM74LS393M or DM74LS393N See NS Package Number M14A or N14A

    \section*{Function Table}
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multicolumn{5}{|c|}{Count Sequence (Each Counter)} \\
    \hline Count & \multicolumn{4}{|c|}{Outputs} \\
    \hline & \(Q_{D}\) & \(Q_{C}\) & \(\mathbf{Q}_{B}\) & \(\mathbf{Q}_{\mathbf{A}}\) \\
    \hline 0 & L & L & L & L \\
    \hline 1 & L & L & L & H \\
    \hline 2 & L & L & H & L \\
    \hline 3 & L & L & H & H \\
    \hline 4 & L & H & L & L \\
    \hline 5 & L & H & L & H \\
    \hline 6 & L & H & H & L \\
    \hline 7 & L & H & H & H \\
    \hline 8 & H & L & L & L \\
    \hline 9 & H & L & L & H \\
    \hline 10 & H & L & H & L \\
    \hline 11 & H & L & H & H \\
    \hline 12 & H & H & L & L \\
    \hline 13 & H & H & L & H \\
    \hline 14 & H & H & H & L \\
    \hline 15 & H & H & H & H \\
    \hline
    \end{tabular}
    \(H=\) High Logic Level
    L = Low Logic Level

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Clear
    A
    Operating Free Air Temperature Range
    \begin{tabular}{lr} 
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM74LS393} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & \\
    \hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{\text {l }}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & mA \\
    \hline \(\mathrm{IOL}^{\text {l }}\) & \multicolumn{2}{|l|}{Low Level Output Current} & & & 8 & mA \\
    \hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 1)} & 0 & & 25 & MHz \\
    \hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & & 20 & MHz \\
    \hline \multirow[t]{2}{*}{tw} & \multirow[t]{2}{*}{Pulse Width (Note 7)} & A & 20 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Clear High & 20 & & & \\
    \hline \(\mathrm{t}_{\text {REL }}\) & \multicolumn{2}{|l|}{Clear Release Time (Notes 3 \& 7)} & \(25 \downarrow\) & & & ns \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
    \begin{aligned}
    & \text { Typ } \\
    & \text { (Note 4) }
    \end{aligned}
    \] & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 2.7 & 3.4 & & V \\
    \hline \multirow[t]{2}{*}{VOL} & \multirow[t]{2}{*}{Low Level Output Voltage} & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & & 0.35 & 0.5 & V \\
    \hline & & \multicolumn{2}{|l|}{\(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\)} & & 0.25 & 0.4 & \\
    \hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current @ Max Input Voltage} & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}\) & Clear & & & 0.1 & \multirow[t]{2}{*}{mA} \\
    \hline & & \(V_{C C}=M a x, V_{1}=5.5 \mathrm{~V}\) & A & & & 0.2 & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{IIH}^{\text {H}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & Clear & & & 20 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & A & & & 40 & \\
    \hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{C C}=\operatorname{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}\)} & Clear & & & -0.4 & \multirow[t]{2}{*}{mA} \\
    \hline & & & A & & & -1.6 & \\
    \hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\text { Max } \\
    & \text { (Note 5) } \\
    & \hline
    \end{aligned}
    \]} & -20 & & -100 & mA \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}\) (Note 6)} & & 15 & 26 & mA \\
    \hline
    \end{tabular}

    Note 1: \(C_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 2: \(C_{L}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(V_{C C}=5 \mathrm{~V}\).
    Note 3: The symbol \((\downarrow)\) indicates that the falling edge of the clear pulse is used for reference.
    Note 4: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 6: ICC is measured with all outputs open, both CLEAR inputs grounded following momentary connection to 4.5 V , and all other inputs grounded.
    Note 7: \(T_{A}=25^{\circ} \mathrm{C}\), and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[b]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(f_{\text {MAX }}\) & Maximum Clock Frequency & \(A\) to \(Q_{A}\) & 25 & & 20 & & MHz \\
    \hline \({ }_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output & \(A\) to \(Q_{A}\) & & 20 & & 24 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \(A\) to
    \[
    Q_{A}
    \] & & 20 & & 30 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \(A\) to \(Q_{D}\) & & 60 & & 87 & ns \\
    \hline tpHL & Propagation Delay Time High to Low Level Output & A to \(Q_{D}\) & & 60 & & 87 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clear to Any Q & & 39 & & 45 & ns \\
    \hline
    \end{tabular}

    Logic Diagram
    

    TL/F/6434-2

    \section*{54LS395/DM74LS395}

    \section*{4-Bit Shift Register with TRI-STATE \({ }^{\circledR}\) Outputs}

    \section*{General Description}

    The LS395 is a 4-bit shift register with TRI-STATE outputs and can operate in either a synchronous parallel load or a serial shift-right mode, as determined by the Select input. An asynchronous active LOW Master Reset (MR) input overrides the synchronous operations and clears the register. An active LOW Output Enable ( \(\overline{\mathrm{OE}}\) ) input controls the TRISTATE output buffers, but does not interfere with the other operations. The fourth stage also has a conventional output for linking purposes in multi-stage serial operations.

    \section*{Features}
    - Shift right or parallel 4-bit register
    - TRI-STATE outputs
    - Input clamp diodes limit high speed termination effects
    m Fully CMOS and TTL compatible

    \section*{Connection Diagram}

    Dual-In-Line Package
    

    \section*{Logic Symbol}
    

    TL/F/9833-2
    \(V_{C C}=\operatorname{Pin} 16\)
    GND \(=\operatorname{Pin} 8\)

    Order Number 54LS395DMQB, 54LS395FMQB,
    54LS395LMQB, DM74LS395WM or DM74LS395N
    See NS Package Number
    E20A, J16A, M16B, N16E or W16A
    \(t_{n}, t_{n+1}=\) Time before and after CP HIGH-to-LOW transition
    \(\mathrm{H}=\) HIGH Voltage Level
    L = LOW Voltage Level
    \(X=\) Immaterial
    \begin{tabular}{|c|c|}
    \hline \multicolumn{2}{|l|}{Absolute Maximum Ratings (Note)} \\
    \hline If Military/Aerospace specified dev please contact the National Sem & s are required, onductor Sales \\
    \hline Supply Voltage & 7 V \\
    \hline Input Voltage & 10V \\
    \hline Operating Free Air Temperature Range & \\
    \hline 54LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    \hline DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    \hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to + \\
    \hline
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS395} & \multicolumn{3}{|c|}{DM74LS395} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline \({ }^{\mathrm{OH}}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathbf{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW \(S\), \(D_{S}\) or \(P_{n}\) to CP & \[
    \begin{aligned}
    & 20 \\
    & 20
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 20 \\
    & 20
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L)
    \end{aligned}
    \] & Hold Time HIGH or LOW \(S, D_{S}\) or \(P_{n}\) to \(\overline{C P}\) & \[
    \begin{aligned}
    & 5 \\
    & 5
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 5 \\
    & 5 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \(t_{w}(L)\) & \(\overline{\text { CP Pulse Width LOW }}\) & 18 & & & 18 & & & ns \\
    \hline \(t_{w}(L)\) & \(\overline{M R}\) Pulse Width LOW & 20 & & & 20 & & & ns \\
    \hline
    \end{tabular}

    Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Condlitions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) } \\
    \hline
    \end{gathered}
    \] & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O H}=\operatorname{Max} \\
    & V_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & 54LS & 2.5 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\text {OL }}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}_{\mathrm{OL}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=10 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \(1 / 2\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current with Outputs OFF & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \overline{\mathrm{OE}, \mathrm{D}_{\mathrm{S}}, \mathrm{~S}=4.5 \mathrm{~V}} \\
    & \mathrm{CP}=\neg, \mathrm{P}_{\mathrm{n}}=\mathrm{GND}
    \end{aligned}
    \]} & & & 29 & mA \\
    \hline & Supply Current with Outputs ON & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{D}_{\mathrm{S}}, \mathrm{~S}=4.5 \mathrm{~V} \\
    & \mathrm{OE}, \overline{\mathrm{CP}}, \mathrm{P}_{\mathrm{n}}=\mathrm{GND}
    \end{aligned}
    \]} & & & 25 & mA \\
    \hline lozh & TRI-STATE Output Off Current HIGH & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCH}} \\
    & \mathrm{~V}_{\mathrm{OZH}}=2.7 \mathrm{~V}
    \end{aligned}
    \]} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline lozL & TRI-STATE Output Off Current LOW & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCH}} \\
    & \mathrm{~V}_{\mathrm{OZL}}=0.4 \mathrm{~V}
    \end{aligned}
    \]} & & & -20 & \(\mu \mathrm{A}\) \\
    \hline
    \end{tabular}

    \footnotetext{
    Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, T_{A}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    }

    \section*{Switching Characteristics}
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{2}{|c|}{54LS/DM74LS} & \\
    \hline & & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \\
    \hline & & Min & Max & \\
    \hline \(f_{\text {max }}\) & Maximum Shift Frequency & 30 & & MHz \\
    \hline \(t_{\text {PLH }}\)
    \[
    t_{\mathrm{PHL}}
    \] & Propagation Delay \(\overline{\mathrm{CP}}\) to \(\mathrm{O}_{\mathrm{n}}\) & & \[
    \begin{array}{r}
    35 \\
    25 \\
    \hline
    \end{array}
    \] & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay \(\overline{M R}\) to \(\mathrm{O}_{\mathrm{n}}\) & & 35 & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PZH}} \\
    & \mathrm{t}_{\mathrm{PZL}} \\
    & \hline
    \end{aligned}
    \] & Output Enable Time & & \[
    \begin{array}{r}
    20 \\
    20 \\
    \hline
    \end{array}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PHZ}} \\
    & \mathrm{t}_{\mathrm{PLZ}} \\
    & \hline
    \end{aligned}
    \] & Output Disable Time & & \[
    \begin{array}{r}
    17 \\
    23 \\
    \hline
    \end{array}
    \] & ns \\
    \hline
    \end{tabular}

    \section*{Functional Description}

    The LS395 contains four D-type edge-triggered flip-flops and auxiliary gating to select a D input either from a Parallel \(\left(P_{n}\right)\) input or from the preceding stage. When the Select input is HIGH, the \(P_{n}\) inputs are enabled. A LOW signal in the \(S\) input enables the serial inputs for shift-right operations, as indicated in the Truth Table.
    State changes are initiated by HIGH-to-LOW transitions on the Clock Pulse ( \(\overline{\mathrm{CP}}\) ) input. Signals on the \(\mathrm{P}_{\mathrm{n}}, \mathrm{D}_{\mathrm{S}}\) and S inputs can change when the Clock is in either state, provided that the recommended setup and hold times are ob-
    served. When the S input is LOW, a \(\overline{\mathrm{CP}}\) HIGH-LOW transition transfers data in O 0 to \(\mathrm{O} 1, \mathrm{O} 1\) to O 2 , and O 2 to O 3 . A left-shift is accomplished by connecting the outputs back to the \(P_{n}\) inputs, but offset one place to the left, i.e., O3 to P2, O 2 to P1, and O 1 to P0, with P3 acting as the linking input from another package.
    When the \(\overline{\mathrm{OE}}\) input is HIGH, the output buffers are disabled and the \(\mathrm{O} 0-\mathrm{O} 3\) outputs are in a high impedance condition. The shifting, parallel loading or resetting operations can still be accomplished, however.

    \section*{Logic Diagram}
    

    \section*{54LS447/DM74LS447 BCD to 7-Segment Decoder/Driver}

    \section*{General Description}

    The 'LS447 is the same as the 'LS247 except that the Output OFF Voltage, \(\mathrm{V}_{\mathrm{OH}}\) is specified as 7.0 V rather than 15 V , with the same \(\mathrm{I}_{\mathrm{OH}}\) limit of \(250 \mu \mathrm{~A}\). For all other information please refer to the 'LS247 data sheet.

    \section*{Connection Diagram}
    

    TL/F/10187-1
    Order Number 54LS447FMQB, 54LS447FMQB, DM74LS447M or DM74LS447N See NS Package Number J16A, M16A, N16E or W16A
    Absolute Maximum Ratings (Note)
    If Millitary/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avallability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    \begin{tabular}{lr} 
    54LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The 'Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS447} & \multicolumn{3}{|c|}{DM74LS447} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & , & -50 & & & -50 & \(\mu \mathrm{A}\) \\
    \hline loL & Low Level Output Current & & & 12 & & & 24 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O H}=M a x, \\
    & V_{\mathrm{IL}}=M a x
    \end{aligned}
    \]} & 54LS & 2.4 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.4 & 3.4 & & \\
    \hline loff & High Level Output Current & \multicolumn{2}{|l|}{Segment Outputs, \(\mathrm{V}_{\mathrm{M}}=7.0 \mathrm{~V}\)} & & & 250 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}} \text { Min, } \mathrm{IOL}=\text { Max, } \\
    & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & 0.35 & 0.5 & \\
    \hline & & \(\mathrm{I}_{\mathrm{OL}}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=10 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{IfL} & \multirow[t]{2}{*}{Low Level Input Current} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{~V}_{1}=0.4 \mathrm{~V} \\
    & \mathrm{BI} / \overline{\mathrm{RBO} \text { Inputs }}
    \end{aligned}
    \]}} & -0.03 & & -0.4 & mA \\
    \hline & & & & -0.09 & & -1.2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & 54LS & -0.3 & & -2.0 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -0.3 & & -2.0 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & & 13 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load).
    \begin{tabular}{c|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multirow{2}{*}{ Parameter } & \multicolumn{2}{|c|}{\(\mathbf{R}_{\mathbf{L}}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow{2}{*}{ Units } \\
    \cline { 3 - 4 } & & Min & Max & \\
    \hline \(\mathrm{t}_{\mathrm{LLH}}\) & Propagation Delay & & 100 & \multirow{2}{*}{ns} \\
    \(t_{\text {PHL }}\) & & & 100 & ns \\
    \hline
    \end{tabular}

    Logic Symbol
    
    \(V_{C C}=\operatorname{Pin} 16\)
    GND \(=\operatorname{Pin} 8\)

    State Diagram
    

    \section*{DM54LS450/DM74LS450 16:1 Multiplexer}

    \section*{General Description}

    The 16:1 Mux selects one of sixteen inputs, E0 through E15, specified by four binary select inputs, A, B, C, and D. The true data is output on \(Y\) and the inverted data on W. Propagation delays are the same for both inputs and addresses and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem pole drive standard.

    Features/Benefits
    - 24-pin SKINNYDIP saves space

    ■ Similar to 74150 (Fat DIP)
    ■ Low current PNP inputs reduce loading

    Connection Diagram
    

    Order Number DM54LS450J, DM74LS450J, DM74LS450N or DM74LS450V
    See NS Package Number J24F, N24C or V28A

    \section*{Standard Test Load}
    

    Function Table
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multicolumn{4}{|c|}{\begin{tabular}{l}
    Input \\
    Select
    \end{tabular}} & \multicolumn{2}{|c|}{Output} \\
    \hline D & C & B & A & W & Y \\
    \hline L & L & L & L & EO & E0 \\
    \hline L & L & L & H & E1 & E1 \\
    \hline L & L & H & L & E2 & E2 \\
    \hline L & L & H & H & \(\overline{\text { E }}\) & E3 \\
    \hline L & H & L & L & E4 & E4 \\
    \hline L & H & L & H & E5 & E5 \\
    \hline L & H & H & L & E6 & E6 \\
    \hline L & H & H & H & \(\overline{\mathrm{E7}}\) & E7 \\
    \hline H & L & L & L & E8 & E8 \\
    \hline H & L & L & H & E9 & E9 \\
    \hline H & L & H & L & E10 & E10 \\
    \hline H & L & H & H & E11 & E11 \\
    \hline H & H & L & L & E12 & E12 \\
    \hline H & H & L & H & E13 & E13 \\
    \hline H & H & H & L & E14 & E14 \\
    \hline H & H & H & H & \(\overline{E 15}\) & E15 \\
    \hline
    \end{tabular}

    \section*{Absolute Maximum Ratings}

    If Military/Aerospace specified devices are required,
    Off-State Output Voltage
    5.5 V please contact the National Semiconductor Sales Office/Distributors for avallability and specifications.
    Supply Voltage VCC
    7 V
    Input Voltage

    \section*{Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{T}_{\text {A }}\) & Operating Free-Air Temperature & -55 & & 125* & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}
    *Case temperature

    Electrical Characteristics Over Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|r|}{Test Conditions} & Min & Typ \(\dagger\) & Max & Units \\
    \hline \(\mathrm{V}_{\mathrm{IL}}\) & Low-Level Input Voltage & & & & & 0.8 & V \\
    \hline \(\mathrm{V}_{1 \mathrm{H}}\) & High-Level Input Voltage & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IC }}\) & Input Clamp Voltage & \(\mathrm{V}_{C C}=\mathrm{MIN}\) & \(\mathrm{I}_{1}=-18 \mathrm{~mA}\) & & & -1.5 & V \\
    \hline ILL & Low-Level Input Current & \(V_{C C}=\) MAX & \(V_{1}=0.4 \mathrm{~V}\) & & & -0.25 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High-Level Input Current & \(V_{C C}=\) MAX & \(\mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 25 & \(\mu \mathrm{A}\) \\
    \hline 11 & Maximum Input Current & \(V_{C C}=\) MAX & \(\mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
    \hline VOL & Low-Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \\
    & \hline
    \end{aligned}
    \] & \(\mathrm{loL}=8 \mathrm{~mA}\) & & & 0.5 & V \\
    \hline VOH & High-Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}
    \end{aligned}
    \] & \begin{tabular}{ll} 
    MIL & \(\mathrm{I}_{\mathrm{OH}}=-2 \mathrm{~mA}\) \\
    COM & \(\mathrm{I}_{\mathrm{OH}}=-3.2 \mathrm{~mA}\)
    \end{tabular} & 2.4 & & & V \\
    \hline los & Output Short-Circuit Current* & \(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}\) & \(\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}\) & -30 & & -130 & mA \\
    \hline ICC & Supply Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}\) & & & 60 & 100 & mA \\
    \hline
    \end{tabular}
    *No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
    \(\dagger\) All typical values are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).

    Switching Characteristics Over Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Test Conditions (See Test Load)} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline tPD & Any Input to Y or W & \[
    \begin{aligned}
    & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \\
    & \mathrm{R}_{1}=560 \Omega \\
    & \mathrm{R}_{2}=1.1 \mathrm{k} \Omega \\
    & \hline
    \end{aligned}
    \] & & 25 & 45 & & 25 & 40 & ns \\
    \hline
    \end{tabular}
    

    \section*{General Description}

    The 16:1 Mux selects one of sixteen inputs, E0 through E15, specified by four binary inputs, A, B, C and D. The true data is output on Y and the inverted data on W. Propagation delays are the same for both inputs and addresses and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem pole drive standard.

    \section*{Connection Diagram}
    

    Order Number DM54LS450AJ, DM74LS450AJ, DM74LS450AN or DM74LS450AV

    \section*{See NS Package Number}

    J24F, N24C or V28A

    \section*{Features}
    - 24-pin SKINNYDIP saves space
    - Similar to 74150 (Fat Dip)
    - Low current PNP inputs reduce loading
    - 15 ns typical propagation delay

    Function Table
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multicolumn{4}{|c|}{\begin{tabular}{l}
    Input \\
    Select
    \end{tabular}} & \multicolumn{2}{|c|}{Output} \\
    \hline D & C & B & A & W & Y \\
    \hline L & L & L & L & EO & E0 \\
    \hline L & L & L & H & E1 & E1 \\
    \hline L & L & H & L & E2 & E2 \\
    \hline L & L & H & H & E3 & E3 \\
    \hline L & H & L & L & E4 & E4 \\
    \hline L & H & L & H & E5 & E5 \\
    \hline L & H & H & L & E6 & E6 \\
    \hline L & H & H & H & E7 & E7 \\
    \hline H & L & L & L & E8 & E8 \\
    \hline H & L & L & H & E9 & E9 \\
    \hline H & L & H & L & E10 & E10 \\
    \hline H & L & H & H & E11 & E11 \\
    \hline H & H & L & L & E12 & E12 \\
    \hline H & H & L & H & E13 & E13 \\
    \hline H & H & H & L & E14 & E14 \\
    \hline H & H & H & H & E15 & E15 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|}
    \hline \multicolumn{2}{|l|}{Absolute Maximum Ratings (Note 1)} \\
    \hline If Military/Aerospace please contact the Office/Distributors fo & cified devices are required, onal Semiconductor Sales lability and specifications. \\
    \hline Supply Voltage \(\mathrm{V}_{\mathrm{CC}}\) & -0.5 V to +7 V (Note 2) \\
    \hline Input Voltage & -1.5 V to +5.5 V (Note 2) \\
    \hline Off-State Output Voltage & -1.5 V to +5.5 V (Note 2) \\
    \hline Input Current & -30.0 mA to +5.0 mA (Note 2) \\
    \hline Output Current (loL) & \(+100 \mathrm{~mA}\) \\
    \hline Storage Temperature & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Ambient Temperature with Power Applied
    \(-65^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    Junction Temperature with
    Power Applied
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    ESD Tolerance
    2000V
    \(C_{\text {ZAP }}=100 \mathrm{pF}\)
    \(R_{\text {ZAP }}=1500 \Omega\)
    Test Method: Human Body Model
    Test Specification: NSC SOP-5-028

    \section*{Recommended Operating Conditons}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{T}_{\text {A }}\) & Operating Free-Air Temperature & -55 & & 125 & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics Over Recommended Operating Conditions
    

    Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.
    Note 2: Some device pins may be raised above these limits during programming operations according to the applicable specification.
    Note 3: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
    Note 4: To avoid invalid readings in other parameter tests, it is preferable to conduct the los test last. To minimize internal heating, only one output should be shorted at a time with maximum duration of 1.0 second each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

    Switching Characteristics Over Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multirow{2}{*}{Test Conditions} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow{2}{*}{Units} \\
    \hline & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(\mathrm{T}_{\mathrm{pd}}\) & Input to Output & \(C_{L}=50 \mathrm{pF}\) & & & 35 & & & 30 & ns \\
    \hline
    \end{tabular}

    Test Load
    

    TL/L/10228-2

    Test Waveform
    

    Notes:
    \(V_{T}=1.5 \mathrm{~V}\)
    \(\mathrm{C}_{\mathrm{L}}\) includes probe and jig capacitance.
    In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

    \section*{Schematic of Inputs and Outputs}
    

    TL/L/10228-4
    

    \section*{DM54LS451/DM74LS451 Dual 8:1 Multiplexer}

    \section*{General Description}

    The Dual 8:1 Mux selects one of eight inputs, \(D 0\) through D7, specified by three binary select inputs, \(A, B\), and \(C\). The true data is output on Y when strobed by S . Propagation delays are the same for inputs, addresses and strobes and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem pole drive standard.

    \section*{Features/Benefits}
    - 24-pin SKINNYDIP saves space
    - Twice the density of 74LS151
    - Low current PNP inputs reduce loading

    \section*{Standard Test Load}
    

    TL/L/8337-2

    Connection Diagram

    Top View
    

    Order Number DM54LS451J, DM74LS451J, DM74LS451N or DM74LS451V
    See NS Package Number J24F, N24C or V28A

    Function Table
    \begin{tabular}{|ccc|c|c|}
    \hline \multicolumn{4}{c|}{ Inputs } & Outputs \\
    \hline \multicolumn{3}{|c|}{ Select } & Strobe & Y \\
    \cline { 1 - 3 } C & B & A & S & \\
    \hline X & X & X & H & H \\
    L & L & L & L & D0 \\
    L & L & H & L & D1 \\
    L & H & L & L & D2 \\
    L & H & H & L & D3 \\
    H & L & L & L & D4 \\
    H & L & H & L & D5 \\
    H & H & L & L & D6 \\
    H & H & H & L & D7 \\
    \hline
    \end{tabular}

    \section*{Absolute Maximum Ratings}

    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage VCC
    Input Voltage
    5.5 V

    Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{T}_{\text {A }}\) & Operating Free-Air Temperature & -55 & & 125* & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}
    *Case Temperature
    Electrical Characteristics Over Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|r|}{Test Conditions} & Min & Typ \(\dagger\) & Max & Units \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low-Level Input Voltage & & & & & 0.8 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High-Level Input Voltage & & & 2 & & & V \\
    \hline \(\mathrm{V}_{1 \mathrm{C}}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}\) & \(\mathrm{l}_{1}=-18 \mathrm{~mA}\) & & & -1.5 & V \\
    \hline \(\mathrm{I}_{1 /}\) & Low-Level Input Current & \(V_{C C}=\) MAX & \(\mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -0.25 & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High-Level Input Current & \(V_{C C}=M A X\) & \(\mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 25 & \(\mu \mathrm{A}\) \\
    \hline 1 & Maximum Input Current & \(V_{C C}=\) MAX & \(\mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low-Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}
    \end{aligned}
    \] & \(\mathrm{loL}=8 \mathrm{~mA}\) & & & 0.5 & V \\
    \hline V OH & High-Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}
    \end{aligned}
    \] & \begin{tabular}{ll} 
    MIL & \(\mathrm{I}_{\mathrm{OH}}=2 \mathrm{~mA}\) \\
    \hline COM & \(\mathrm{I}_{\mathrm{OH}}=-3.2 \mathrm{~mA}\)
    \end{tabular} & 2.4 & & & V \\
    \hline los & Output Short-Circuit Current* & \(\mathrm{V}_{C C}=5.0 \mathrm{~V}\) & \(\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}\) & -30 & & \(-130\) & mA \\
    \hline ICC & Supply Current & \(V_{C C}=M A X\) & & & 60 & 100 & mA \\
    \hline
    \end{tabular}
    *No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
    \(\dagger\) All typical values are \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Switching Characteristics Over Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Test Conditions (See Test Load)} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(t_{\text {PD }}\) & Any Input to \(Y\) & \[
    \begin{aligned}
    & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \\
    & \mathrm{R}_{1}=560 \Omega \\
    & \mathrm{R}_{2}=1.1 \Omega \\
    & \hline
    \end{aligned}
    \] & & 25 & 45 & & 25 & 40 & ns \\
    \hline
    \end{tabular}

    Logic Diagram
    

    TL/L/8337-3

    \section*{DM54LS451A/DM74LS451A}

    Dual 8:1 Multiplexer

    \section*{General Description}

    The Dual Mux selects one of eight inputs, D0 through D7, specified by three binary select inputs, A, B and C. The true data is output on Y when strobed by S . Propagation delays are the same for inputs, addresses and strobes and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem pole drive standard.

    \section*{Connection Diagram}

    Order Number DM54LS451AJ, DM74LS451AJ, DM74LS451AN or DM74LS451AV
    See NS Package Number J24F, N24C or V28A
    

    \section*{Features}
    - 24-pin SKINNYDIP saves space
    - Twice the density of 74LS151
    - Low current PNP inputs reduce loading
    - 15 ns typical propagation delay

    \section*{Function Table}
    \begin{tabular}{|ccc|c|c|}
    \hline \multicolumn{4}{c|}{ Inputs } & Outputs \\
    \hline \multicolumn{3}{|c|}{ Select } & Strobe & \multirow{2}{*}{ Y } \\
    \cline { 1 - 3 } C & B & A & S & \\
    \hline X & X & X & H & H \\
    L & L & L & L & D0 \\
    L & L & H & L & D1 \\
    L & H & L & L & D2 \\
    L & H & H & L & D3 \\
    H & L & L & L & D4 \\
    H & L & H & L & D5 \\
    H & H & L & L & D6 \\
    H & H & H & L & D7 \\
    \hline
    \end{tabular}

    \begin{abstract}
    Absolute Maximum Ratings (Note 1) If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage VCC Input Voltage Off-State Output Voltage
    Input Current
    Output Current (loL)
    Storage Temperature
    \[
    \begin{array}{r}
    -0.5 \mathrm{~V} \text { to }+7 \mathrm{~V}(\text { Note } 2) \\
    -1.5 \mathrm{~V} \text { to }+5.5 \mathrm{~V}(\text { Note } 2) \\
    -1.5 \mathrm{~V} \text { to }+5.5 \mathrm{~V}(\text { Note } 2) \\
    -30.0 \mathrm{~mA} \text { to }+5.0 \mathrm{~mA}(\text { Note } 2) \\
    +100 \mathrm{~mA}
    \end{array}
    \]
    \end{abstract}

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{T}_{\text {A }}\) & Operating Free-Air Temperature & -55 & & 125 & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics Over Recommended Operating Conditions
    

    Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.
    Note 2: Some device pins may be raised above these limits during programming operations according to the applicable specification.
    Note 3: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
    Note 4: To avoid invalid readings in other parameter tests, it is preferable to conduct the los test last. To minimize internal heating, only one output should be shorted at a time with maximum duration of 1.0 second each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Test Conditions} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(\mathrm{T}_{\mathrm{pd}}\) & Input to Output & \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\) & & 15 & 30 & & 15 & 25 & ns \\
    \hline
    \end{tabular}

    Test Load
    

    TL/L/10227-2

    \section*{Test Waveform}
    

    Notes:
    \(V_{T}=1.5 \mathrm{~V}\)
    \(C_{L}\) includes probe and jig capacitance.
    In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

    \section*{Schematic of Inputs and Outputs}
    

    TL/L/10227-4

    Logic Diagram
    

    \section*{General Description}

    The quad 4:1 Mux selects one of four inputs, C0 through C3, specified by two binary select inputs, A and B . The true data is output on Y. Propagation delays are the same for inputs and addresses and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem pole drive standard.

    \section*{Connection Diagram}

    Top Vlew
    

    Order Number DM54LS453J,
    DM74LS453J or DM74LS453N
    See NS Package Number J24F or N24C

    \section*{Features/Benefits}
    - 24-pin SKINNYDIP saves space
    - Twice the density of 74LS153

    ■ Low current PNP inputs reduce loading

    \section*{Standard Test Load}
    

    TL/L/8336-2

    Function Table
    \begin{tabular}{|cc|c|}
    \hline \multicolumn{2}{|c|}{ INPUT } \\
    SELECT & \multirow{2}{*}{ OUTPUTS } \\
    B & A & \\
    \hline L & L & C0 \\
    L & \(H\) & C1 \\
    \(H\) & L & C2 \\
    \(H\) & \(H\) & C3 \\
    \hline
    \end{tabular}

    \section*{Absolute Maximum Ratings}

    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avallability and specifications.

    Off-State Output Voltage
    Supply Voltage \(V_{C C}\)
    7V
    Input Voltage
    5.5 V

    \section*{Operating Conditions}
    \begin{tabular}{l|l|c|c|c|c|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multirow{2}{*}{ Parameter } & \multicolumn{3}{|c|}{ Military } & \multicolumn{3}{c|}{ Commercial } & \multirow{2}{*}{ Units } \\
    \cline { 3 - 8 } & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & Operating Free-Air Temperature & -55 & & \(125^{*}\) & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}
    *Case temperature

    Electrical Characteristics Over Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{3}{|c|}{Test Conditions} & Min & Typ \(\dagger\) & Max & Units \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low-Level Input Voltage & & & & & & 0.8 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High-Level Input Voltage & & & & 2 & & & V \\
    \hline \(\mathrm{V}_{10}\) & Input Clamp Voltage & \(\mathrm{V}_{C C}=\mathrm{MIN}\) & \(1{ }_{1}=\) & & & & -1.5 & V \\
    \hline I/L & Low-Level Input Current & \(V_{C C}=\) MAX & \(V_{1}=\) & & & & \(-0.25\) & mA \\
    \hline \(\mathrm{I}_{\mathrm{iH}}\) & High-Level Input Current & \(V_{C C}=\) MAX & \(V_{1}=\) & & & & 25 & \(\mu \mathrm{A}\) \\
    \hline 1 & Maximum Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}\) & \(V_{1}=5.5\) & & & & 1 & mA \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low-Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \\
    & \hline
    \end{aligned}
    \] & & \(\mathrm{lOL}^{\prime}=8 \mathrm{~mA}\) & & & 0.5 & V \\
    \hline VOH & High-Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}
    \end{aligned}
    \] & \[
    \frac{\text { MIL }}{\text { COM }}
    \] & \[
    \begin{aligned}
    & \mathrm{I}_{\mathrm{OH}}=-2 \mathrm{~mA} \\
    & \mathrm{I}_{\mathrm{OH}}=-3.2 \mathrm{~mA}
    \end{aligned}
    \] & 2.4 & & & V \\
    \hline los & Output Short-Circuit Current* & \(\mathrm{V}_{C C}=5.0 \mathrm{~V}\) & & \(\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}\) & -30 & & -130 & mA \\
    \hline ICC & Supply Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}\) & & & & 60 & 100 & mA \\
    \hline
    \end{tabular}
    *No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
    \(\dagger\) All typical values are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\)

    Switching Characteristics Over Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Test Conditions (See Test Load)} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow{2}{*}{Units} \\
    \hline & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline tPD & Any Input to \(Y\) & \[
    \begin{aligned}
    & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \\
    & \mathrm{R}_{1}=560 \Omega \\
    & \mathrm{R}_{2}=1.1 \mathrm{k} \Omega \\
    & \hline
    \end{aligned}
    \] & & 25 & 45 & & 25 & 40 & ns \\
    \hline
    \end{tabular}
    

    \section*{DM54LS453A/DM74LS453A Quad 4:1 Multiplexer}

    \section*{General Description}

    The quad 4:1 Mux selects one of four inputs, C0 through C3, specified by two binary select inputs, A and B. The true data is output on \(Y\). Propagation delays are the same for inputs and addresses and specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem pole drive standard.

    \section*{Features}

    ■ 24-pin SKINNYDIP saves space
    - Twice the density of 74LS153
    - Low current PNP inputs reduce loading
    - 15 ns typical propagation delay

    \section*{Connection Diagram}

    Top View
    

    Order Number DM54LS453AJ, DM74LS453AJ, DM74LS453AN or DM74LS453AV See NS Package Number J24F, N24C or V28A

    \section*{Function Table}
    \begin{tabular}{|cc|c|}
    \hline \multicolumn{2}{|c|}{\begin{tabular}{c} 
    Input \\
    Select
    \end{tabular}} & \multirow{2}{*}{ Outputs } \\
    \cline { 1 - 2 } B & A & \\
    \hline L & L & C0 \\
    L & H & C1 \\
    H & L & C2 \\
    H & H & C3 \\
    \hline
    \end{tabular}

    > Absolute Maximum Ratings (Note 1)
    > If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    > Supply Voltage \(\mathrm{V}_{\mathrm{CC}}\)
    > -0.5 V to +7 V (Note 2)
    > Input Voltage
    > -1.5 V to +5.5 V (Note 2)
    > -1.5 V to +5.5 V (Note 2)
    > Off-State Output Voltage
    > -30.0 mA to +5.0 mA (Note 2)
    > Output Current (loL)
    > Storage Temperature
    > \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{Milltary} & \multicolumn{3}{|c|}{Commercial} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{T}_{\text {A }}\) & Operating Free-Air Temperature & -55 & & 125 & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics Over Recommended Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{3}{|c|}{Test Conditions} & Min & Typ & Max & Units \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage (Note 3) & & & & & & 0.8 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage (Note 3) & & & & 2 & & & V \\
    \hline \(\mathrm{V}_{1 \mathrm{C}}\) & Input Clamp Voltage & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline IIL & Low Level Input Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.25 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 25 & \(\mu \mathrm{A}\) \\
    \hline 11 & Maximum Input Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}\) & \(\mathrm{l} \mathrm{OL}=8 \mathrm{~mA}\) & & & & 0.5 & V \\
    \hline \multirow[t]{2}{*}{V OH} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}\)} & \(\mathrm{IOH}=-2 \mathrm{~mA}\) & MIL & \multirow[t]{2}{*}{2.4} & & & V \\
    \hline & & & \(\mathrm{l}_{\mathrm{OH}}=-3.2 \mathrm{~mA}\) & COM & & & & \\
    \hline los & Output Short-Circuit Current (Note 4) & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\)} & \(-30\) & & -130 & mA \\
    \hline ICC & Supply Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\) Max, Outputs Open} & & 60 & 100 & mA \\
    \hline
    \end{tabular}

    Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.
    Note 2: Some device pins may be raised above these limits during programming operations according to the applicable specification.
    Note 3: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

    Note 4: To avoid invalid readings in other parameter tests, it is preferable to conduct the los test last. To minimize internal heating, only one output should be shorted at a time with maximum duration of 1.0 second each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

    Switching Characteristics Over Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Test Conditions} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(\mathrm{T}_{\mathrm{pd}}\) & Input to Output & \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\) & & 15 & 30 & & 15 & 25 & ns \\
    \hline
    \end{tabular}

    Test Load
    

    Test Waveform
    

    \section*{Notes:}
    \(V_{T}=1.5 \mathrm{~V}\)
    \(\mathrm{C}_{\mathrm{L}}\) includes probe and jig capacitance.
    In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

    \section*{Schematic of Inputs and Outputs}
    

    TL/L/10226-4

    \section*{Logic Diagram}
    

    \section*{DM54LS460/DM74LS460 10-Bit Comparator}

    \section*{General Description}

    The 'LS460 is a 10 -bit comparator with true and complement comparison status outputs. The device compares two 10-bit data strings ( \(A_{g}-A_{0}\) and \(B_{g}-B_{0}\) ) to establish if this data is Equivalent ( \(\mathrm{EQ}=\mathrm{HIGH}\) and \(\mathrm{NE}=\mathrm{LOW}\) ) or Not Equivalent ( \(\mathrm{EQ}=\mathrm{LOW}\) and \(\mathrm{NE}=\mathrm{HIGH}\) ).
    Outputs conform to the usual 8 mA LS totem-pole drive standard.

    \section*{Connection Diagram}
    

    \section*{Features/Benefits}
    - True and complement comparison status outputs
    - 24-pin SKINNYDIP saves space
    - Low current PNP inputs reduce loading
    - Expandable in 10 -bit increments

    \section*{Standard Test Load}
    

    Function Table
    \begin{tabular}{|c|c|c|c|c|}
    \hline A9-A0 & B9-B0 & EQ & NE & Operation \\
    \hline A & A & H & L & \multirow{2}{c|}{ Equivalent \((A=B)\)} \\
    B & B & H & L & Eq \\
    A & B & L & H & Not Equivalent \((A \neq B)\) \\
    \hline
    \end{tabular}

    \section*{Absolute Maximum Ratings}

    If Milltary/Aerospace specifled devices are required, please contact the National Semiconductor Sales Office/Distributors for avallablity and specifications.
    Supply Voltage \(\mathrm{V}_{\mathrm{CC}}\)
    \(\begin{array}{lr}\text { Input Voltage } & 5.5 \mathrm{~V} \\ \text { Off-State Output Voltage } & 5.5 \mathrm{~V} \\ \text { Storage Temperature } & -65^{\circ} \text { to }+150^{\circ} \mathrm{C}\end{array}\)

    \section*{Operating Conditions}
    \begin{tabular}{l|l|c|c|c|c|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multirow{2}{*}{ Parameter } & \multicolumn{3}{|c|}{ Milltary } & \multicolumn{3}{c|}{ Commerclal } & \multirow{2}{*}{ Units } \\
    \cline { 3 - 9 } & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & Operating Free-Air Temperature & -55 & & \(125^{*}\) & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}
    -Case Temperature
    Electrical Characteristics Over Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{3}{|c|}{Test Conditions} & Min & Typ \(\dagger\) & Max & Units \\
    \hline \(V_{\text {IL }}\) & Low-Level Input Voltage & & & & & & 0.8 & V \\
    \hline \(\mathrm{V}_{1 \text { H }}\) & High-Level Input Voltage & & & & 2 & & & V \\
    \hline \(\mathrm{V}_{16}\) & Input Clamp Voltage & \(V_{C C}=\mathrm{MIN}\) & \(1=\) & & & & -1.5 & V \\
    \hline IIL & Low-Level Input Current & \(V_{C C}=M A X\) & \(V_{1}=\) & & & & \(-0.25\) & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High-Level Input Current & \(V_{C C}=M A X\) & \(V_{1}=2\) & & & & 25 & \(\mu \mathrm{A}\) \\
    \hline 11 & Maximum Input Current & \(V_{C C}=\mathrm{MAX}\) & \(V_{1}=5\) & & & & 1 & mA \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low-Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}
    \end{aligned}
    \] & & \(\mathrm{lOL}^{\prime}=8 \mathrm{~mA}\) & & & 0.5 & V \\
    \hline VOH & High-Level Output Voltage & \[
    \begin{aligned}
    & V_{C C}=M I N \\
    & V_{I L}=0.8 \mathrm{~V} \\
    & V_{I H}=2 \mathrm{~V}
    \end{aligned}
    \] & MIL COM & \[
    \begin{aligned}
    & \mathrm{I}_{\mathrm{OH}}=-2 \mathrm{~mA} \\
    & \mathrm{I}_{\mathrm{OH}}=-3.2 \mathrm{~mA}
    \end{aligned}
    \] & 2.4 & & & V \\
    \hline los & Output Short-Circuit Current* & \(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}\) & & \(\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}\) & -30 & & \(-130\) & mA \\
    \hline ICC & Supply Current & \(V_{C C}=M A X\) & & & & 60 & 100 & mA \\
    \hline
    \end{tabular}
    *No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second
    \(\dagger\) All typical values are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\)
    Switching Characteristics Over Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Test Conditions (See Test Load)} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(t_{\text {PD }}\) & Any Input to EQ or NE & \[
    \begin{aligned}
    & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \\
    & \mathrm{R}_{1}=560 \Omega \\
    & \mathrm{R}_{2}=1.1 \mathrm{k} \Omega \\
    & \hline
    \end{aligned}
    \] & & 25 & 45 & & 25 & 40 & ns \\
    \hline
    \end{tabular}
    

    \section*{National Semiconductor}

    \section*{DM54LS460A/DM74LS460A 10-Bit Comparator}

    \section*{General Description}

    The 'LS460A is a 10 -bit comparator with true complement comparison status outputs. The device compares two 10-bit data strings ( \(\mathrm{Ag}-\mathrm{AO}\) and \(\mathrm{Bg}-\mathrm{BO}\) ) to establish if this data is Equivalent ( \(\mathrm{EQ}=\mathrm{HIGH}\) and \(\mathrm{NE}=\mathrm{LOW}\) ) or Not Equivalent ( \(\mathrm{EQ}=\mathrm{LOW}\) and \(\mathrm{NE}=\mathrm{HIGH}\) ).
    Outputs conform to the usual 8 mA LS totem-pole drive standard.

    \section*{Features}
    - True and complement comparison status outputs

    ■ 24-pin SKINNYDIP saves space
    - Low current PNP inputs reduce loading
    - Expandable in 10 -bit increments
    - 15 ns typical propagation delay

    \section*{Connection Diagram}
    

    TL/L/10225-1
    Order Number DM54LS460AJ, DM74LS460AJ, DM74LS460AN or DM74LS460AV See NS Package Number J24F, N24C or V28A

    \section*{Function Table}
    \begin{tabular}{|c|c|c|c|c|}
    \hline A9-A0 & B9-B0 & EQ & NE & Operation \\
    \hline A & A & \(H\) & L & \multirow{2}{c|}{ Equivalent \((A=B)\)} \\
    \(B\) & \(B\) & \(H\) & L & Eq \\
    A & \(B\) & L & \(H\) & Not Equivalent \((A \neq B)\) \\
    \hline
    \end{tabular}
    ```

    Absolute Maximum Ratings (Note 1)
    If Military/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for availability and specifications.
    Supply Voltage (VCC)
    -0.5 to +7 V (Note 2)
    Input Voltage
    -1.5 to +5.5 V (Note 2)
    Off-State Output Voltage
    -1.5 to +5.5 V (Note 2)
    Input Current
    -30.0 mA to +5.0 mA (Note 2)
    Output Current (loL)
    Storage Temperature
    -0.5 to +7 V (Note 2)
    -1.5 to +5.5 V (Note 2)
    -1.5 to +5.5 V (Note 2)
    -30.0 mA to +5.0 mA (Note 2)
    +100 mA
    $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

    ```

    Ambient Temperature with Power Applied
    \(-65^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    Junction Temperature with Power Applied
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    ESD Tolerance
    2000 V
    CZAP \(=100 \mathrm{pF}\)
    RZAP \(=1500 \Omega\)
    Test Method: Human Body Model
    Test Specification: NSC SOP-5-028

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{T}_{\text {A }}\) & Operating Free-Air Temperature & -55 & & 125 & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics Over Recommended Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{3}{|c|}{Test Conditions} & Min & Typ & Max & Units \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage (Note 3) & & & & & & 0.8 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage (Note 3) & & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IC }}\) & Input Clamp Voltage & \multicolumn{3}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{I}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline IIL & Low Level Input Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{VI}=0.4 \mathrm{~V}\)} & & & -0.25 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{VI}=2.4 \mathrm{~V}\)} & & & 25 & \(\mu \mathrm{A}\) \\
    \hline 11 & Maximum Input Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{VI}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \(V_{C C}=\operatorname{Min}\) & \(\mathrm{l}_{\mathrm{OL}}=8 \mathrm{~mA}\) & & & & 0.5 & V \\
    \hline \multirow[t]{2}{*}{V OH} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\(\mathrm{V}_{C C}=\mathrm{Min}\)} & \(\mathrm{IOH}=-2 \mathrm{~mA}\) & MIL & \multirow[t]{2}{*}{2.4} & & & \multirow[t]{2}{*}{V} \\
    \hline & & & \(\mathrm{l}_{\mathrm{OH}}=-3.2 \mathrm{~mA}\) & COM & & & & \\
    \hline los & Output Short-Circuit Current (Note 4) & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\)} & -30 & & -130 & mA \\
    \hline ICC & Supply Current & \multicolumn{3}{|l|}{\(V_{C C}=\) Max, Outputs Open} & & 60 & 100 & mA \\
    \hline
    \end{tabular}

    Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.
    Note 2: Some device pins may be raised above these limits during programming operations according to the applicable specification.
    Note 3: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
    Note 4: To avoid invalid readings in other parameter tests, it is preferable to conduct the los test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 second each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

    Switching Characteristics Over Recommended Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Test Conditions} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(\mathrm{T}_{\mathrm{pd}}\) & Input to Output & \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\) & & & 35 & & & 30 & ns \\
    \hline
    \end{tabular}

    Test Load
    

    Test Waveform

    MIL/COM
    \(\mathrm{R} 1=560\)
    \(R 2=1.1 \mathrm{k}\)

    TL/L/10225-2
    

    TL/L/10225-3

    Notes:
    \(V_{T}=1.5 \mathrm{~V}\)
    \(\mathrm{C}_{\mathrm{L}}\) includes probe and jig capacitance.
    In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

    \section*{Schematic of Inputs and Outputs}
    

    10-Bit Comparator
    

    \section*{DM54LS461/DM74LS461 Octal Counter}

    \section*{General Description}

    The LS461 is an 8 -bit synchronous counter with parallel load, clear, and hold capability. Two function select inputs ( \(I_{0}, I_{1}\) ) provide one of four operations which occur synchronously on the rising edge of the clock (CK).
    The LOAD operation loads the inputs ( \(D_{7}-D_{0}\) ) into the output register \(\left(Q_{7}-Q_{0}\right)\). The CLEAR operation resets the output register to all LOWs. The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE ( \(\overline{\mathrm{Cl}}=\mathrm{LOW}\) ), otherwise the operation is a HOLD. The carry-out \((\overline{\mathrm{CO}})\) is TRUE \((\overline{\mathrm{CO}}=\mathrm{LOW})\) when the output register \(\left(Q_{7}-Q_{0}\right)\) is all HIGHs, otherwise FALSE ( \(\overline{\mathrm{CO}}=\mathrm{HIGH}\) ).
    The output register \(\left(Q_{7}-Q_{0}\right)\) is enabled when \(\overline{O E}\) is LOW, and disabled ( \(\mathrm{HI}-\mathrm{Z}\) ) when \(\overline{\mathrm{OE}}\) is HIGH . The output drivers will sink the 24 mA required for many bus interface standards.

    Two or more LS461 octal counters may be cascaded to provide larger counters. The operation codes were chosen such that when \(I_{1}\) is HIGH, \(I_{0}\) may be used to select between LOAD and INCREMENT as in a program counter (JUMP/INCREMENT).

    \section*{Features/Benefits}

    ■ Octal counter for microprogram-counter, DMA controller and general purpose counting applications
    - 8 bits match byte boundaries
    - Bus-structured pinout
    - 24-pin Skinny Dip saves space
    - TRI-STATE \({ }^{\circledR}\) outputs drive bus lines
    - Low current PNP inputs reduce loading
    - Expandable in 8 -bit increments

    Connection Diagram
    

    Standard Test Load
    

    TL/L/8334-2

    Function Table
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline\(\overline{\mathbf{O E}}\) & \(\mathbf{C K}\) & \(\mathbf{1 1}\) & \(\mathbf{1 0}\) & \(\overline{\mathbf{C I}}\) & D7-D0 & Q7-Q0 & Operation \\
    \hline H & X & X & X & X & X & Z & HI-Z \\
    L & \(\uparrow\) & L & L & X & X & L & CLEAR \\
    L & \(\uparrow\) & L & H & X & X & Q & HOLD \\
    L & \(\uparrow\) & H & L & X & D & D & LOAD \\
    L & \(\uparrow\) & H & H & H & X & Q & HOLD \\
    L & \(\uparrow\) & H & H & L & X & Q plus 1 & INCREMENT \\
    \hline
    \end{tabular}

    \section*{Absolute Maximum Ratings}
    \(\begin{array}{lr}\text { If Military/Aerospace specified devices are required, } \\ \text { please contact the National Semiconductor Sales } \\ \text { Office/Distributors for availability and specifications. } \\ \text { Supply Voltage } V_{\mathrm{CC}} & 7 \mathrm{~V} \\ \text { Input Voltage } & 5.5 \mathrm{~V}\end{array}\)
    Off-State Output Voltage
    5.5 V

    Storage Temperature
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    \section*{Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Operating Free-Air Temperature} & -55 & & 125* & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \multirow[t]{2}{*}{tw} & \multirow[t]{2}{*}{Width of Clock} & Low & 40 & & & 35 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & High & 30 & & & 25 & & & \\
    \hline tsu & \multicolumn{2}{|l|}{Set Up Time} & 60 & & & 50 & & & \multirow[t]{2}{*}{ns} \\
    \hline \(t_{h}\) & \multicolumn{2}{|l|}{Hold Time} & 0 & -15 & & 0 & -15 & & \\
    \hline
    \end{tabular}
    *Case Temperature
    Electrical Characteristics over Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & & Test Conditions & Min & Typ \(\dagger\) & Max & Units \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low-Level Input Voltage & & & & & 0.8 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High-Level Input Voltage & & & 2 & & & V \\
    \hline \(\mathrm{V}_{1 \mathrm{C}}\) & Input Clamp Voltage & \(V_{C C}=\mathrm{MIN}\) & \(I_{1}=-18 \mathrm{~mA}\) & & & -1.5 & V \\
    \hline \(\mathrm{I}_{\text {IL }}\) & Low-Level Input Current & \(\mathrm{V}_{C C}=\mathrm{MAX}\) & \(\mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -0.25 & mA \\
    \hline \(\mathrm{I}_{\mathrm{IH}}\) & High-Level Input Current & \(V_{C C}=\) MAX & \(\mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 25 & \(\mu \mathrm{A}\) \\
    \hline 1 & Maximum Input Current & \(V_{C C}=\) MAX & \(\mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{2}{*}{Low-Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{gathered}
    \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\
    \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}
    \end{gathered}
    \]} & MIL \(\quad \mathrm{lOL}^{\prime}=12 \mathrm{~mA}\) & & & \multirow[t]{2}{*}{0.5} & \multirow[t]{2}{*}{V} \\
    \hline & & & \(\mathrm{COM} \quad \mathrm{IOL}=24 \mathrm{~mA}\) & & & & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High-Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{gathered}
    \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\
    \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}
    \end{gathered}
    \]} & MIL \(\quad \mathrm{I}_{\mathrm{OH}}=-2 \mathrm{~mA}\) & \multirow[t]{2}{*}{2.4} & & & \multirow[t]{2}{*}{V} \\
    \hline & & & \(\mathrm{COM} \quad \mathrm{IOH}=-3.2 \mathrm{~mA}\) & & & & \\
    \hline lozL & \multirow[t]{2}{*}{Off-State Output Current} & \multirow[t]{2}{*}{\[
    \begin{gathered}
    V_{C C}=M A X \\
    V_{I L}=0.8 V \\
    V_{I H}=2 V
    \end{gathered}
    \]} & \(\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}\) & & & -100 & \(\mu \mathrm{A}\) \\
    \hline lozh & & & \(\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}\) & & & 100 & \(\mu \mathrm{A}\) \\
    \hline lOS & Output Short-Circuit Current* & \(\mathrm{V}_{C C}=5.0 \mathrm{~V}\) & \(\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V}\) & -30 & & -130 & mA \\
    \hline ICC & Supply Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}\) & & & 120 & 180 & mA \\
    \hline
    \end{tabular}
    *No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second
    \(\dagger\) All typical values are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Switching Characteristics Over Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Test Conditions (See Test Load)} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & \multirow{6}{*}{\[
    \begin{aligned}
    \mathrm{C}_{\mathrm{L}} & =50 \mathrm{pF} \\
    \mathrm{R}_{1} & =200 \Omega \\
    \mathrm{R}_{2} & =390 \Omega
    \end{aligned}
    \]} & 10.5 & & & 12.5 & & & MHz \\
    \hline \(t_{P D}\) & \(\overline{\mathrm{CBI}}\) to \(\overline{\mathrm{CBO}}\) Delay & & & 35 & 60 & & 35 & 50 & ns \\
    \hline \(t_{\text {PD }}\) & Clock to Q & & & 20 & 35 & & 20 & 30 & ns \\
    \hline \(t_{\text {PD }}\) & Clock to \(\overline{\mathrm{CO}}\) & & & 55 & 95 & & 55 & 80 & ns \\
    \hline \(t_{\text {PZX }}\) & Output Enable Delay & & & 35 & 55 & & 35 & 45 & ns \\
    \hline \(t_{\text {PXZ }}\) & Output Disable Delay & & & 35 & 55 & & 35 & 45 & ns \\
    \hline
    \end{tabular}
    

    \section*{DM54LS461A/DM74LS461A Octal Counter}

    \section*{General Description}

    The LS461A is an 8-bit synchronous counter with parallel load, clear and hold capability. Two function select inputs ( 10,11 ) provide one of four operations which occur synchronously on the rising edge of the (CK).

    The LOAD operation loads the inputs (D7-D0) into the output register (Q7-Q0). The CLEAR operation resets the output register to all LOWs. The HOLD operation holds the previous value regardless of the clock transitions. The IN CREMENT operation adds one to the output register when the carry-in input is TRUE \((\overline{\mathrm{Cl}}=\mathrm{LOW})\), otherwise the operation is a HOLD. The carry-out ( \(\overline{\mathrm{CO}}\) ) is True ( \(\overline{\mathrm{CO}}=\) LOW) when the output register (Q7-Q0) is all HIGHs, otherwise FALSE ( \(\overline{\mathrm{CO}}=\mathrm{HIGH}\) ).
    The output register (Q7-Q0) is enabled when \(\overline{\mathrm{OE}}\) is LOW, and disabled ( \(\mathrm{HI}-\mathrm{Z}\) ) when OE is HIGH. The output drivers will sink 24 mA required for many bus interface standards.
    Two or more LS461A octal counters may be cascaded to provide larger counters. The operation codes were chosen such that when I1 is HIGH IO may be used to select between LOAD and INCREMENT as in a program counter (JUMP/INCREMENT).

    \section*{Features}
    - Octal counter for microprogram-counter, DMA controller for general purpose counting applications
    - 8 bits match byte boundaries
    - Low current PNP inputs reduce loading
    - Bus-structured pinout
    - TRI-STATE \({ }^{\circledR}\) outputs drive bus lines
    - 24-pin SKINNYDIP saves space
    ■ Expadable in 8 -bit increments

    \section*{Connection Diagram}
    

    TL/L/10224-1
    Order Number DM54LS461AJ, DM74LS461AJ, DM74LS461AN or DM74LS461AV See NS Package Number J24F, N24C or V28A

    \section*{Function Table}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline\(\overline{\mathbf{O E}}\) & \(\mathbf{C K}\) & \(\mathbf{1 1}\) & \(\mathbf{1 0}\) & \(\overline{\mathbf{C I}}\) & D7-D0 & Q7-Q0 & Operation \\
    \hline H & X & X & X & X & X & Z & HI-Z \\
    L & \(\uparrow\) & L & L & X & X & L & CLEAR \\
    L & \(\uparrow\) & L & H & X & X & Q & HOLD \\
    L & \(\uparrow\) & H & L & X & D & D & LOAD \\
    L & \(\uparrow\) & H & H & H & X & Q & HOLD \\
    L & \(\uparrow\) & H & H & L & X & QPlus 1 & INCREMENT \\
    \hline
    \end{tabular}

    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    \(\begin{array}{lr}V_{C C} \text { Supply Voltage } & 7 \mathrm{~V} \\ \text { Input Voltage } & 5.5 \mathrm{~V} \\ \text { Off-State Output Voltage } & 5.5 \mathrm{~V}\end{array}\)

    Storage Temperature
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    ESD Tolerance
    \(>1000 \mathrm{~V}\)

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{T}_{\text {A }}\) & Operating Free-Air Temperature & -55 & 25 & & 0 & 25 & 75 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \(\mathrm{T}_{\mathrm{C}}\) & Operating Case Temperature & & & 125 & & & & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics Series 24A Over Recommended Operating Temperature Range
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{3}{|c|}{Test Conditions} & Min & Typ & Max & Units \\
    \hline \(\mathrm{V}_{1 \mathrm{H}}\) & High Level Input Voltage & \multicolumn{3}{|l|}{(Note 2)} & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & \multicolumn{3}{|l|}{(Note 2)} & & & 0.8 & V \\
    \hline \(V_{\text {IC }}\) & Input Clamp Voltage & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{II}=-18 \mathrm{~mA}\)} & & \(-0.8\) & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Min} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \\
    & \hline
    \end{aligned}
    \]} & \(\mathrm{IOH}=-2 \mathrm{~mA}\) & MIL & \multirow[b]{2}{*}{2.4} & \multirow[b]{2}{*}{2.9} & & \multirow[b]{2}{*}{V} \\
    \hline & & & \(\mathrm{lOH}=-3.2 \mathrm{~mA}\) & COM & & & & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}
    \end{aligned}
    \]} & \(\mathrm{lOL}=12 \mathrm{~mA}\) & MIL & & \multirow[b]{2}{*}{0.3} & \multirow[b]{2}{*}{0.5} & \multirow[b]{2}{*}{V} \\
    \hline & & & \(\mathrm{loL}=24 \mathrm{~mA}\) & COM & & & & \\
    \hline lozh & \multirow[t]{2}{*}{Off-State Output Current (Note 3)} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{I L}=0.8 \mathrm{~V} \\
    & V_{I H}=2 \mathrm{~V} \\
    & \hline
    \end{aligned}
    \]} & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}\)} & & & 100 & \(\mu \mathrm{A}\) \\
    \hline lozl & & & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}\)} & & & -100 & \(\mu \mathrm{A}\) \\
    \hline 1 & Maximum Input Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current (Note 3) & \multicolumn{3}{|l|}{\(V_{C C}=M a x, V_{1}=2.4 \mathrm{~V}\)} & & & 25 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current (Note 3) & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & -0.04 & -0.25 & mA \\
    \hline los & Output Short-Circuit Current & \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) & \multicolumn{2}{|l|}{\[
    \mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}(\text { Note } 4)
    \]} & -30 & -70 & -130 & mA \\
    \hline ICC & Supply Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 135 & 180 & mA \\
    \hline
    \end{tabular}

    Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.
    Note 2: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
    Note 3: I/O leakage as the worst case of IOZX or IIX, e.g., IIL and IOZL.
    Note 4: During los measurement, only one output at a time should be grounded. Permanent damage otherwise may result.
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|}
    \hline & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multirow[t]{2}{*}{Test Conditions} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline ts & \multicolumn{2}{|l|}{Set-Up Time from Input} & & 40 & 20 & & 30 & 20 & & ns \\
    \hline \multirow[t]{2}{*}{\({ }^{\text {tw }}\)} & \multirow[t]{2}{*}{Width of Clock} & High & & 20 & 7 & & 15 & 7 & & ns \\
    \hline & & Low & & 35 & 15 & & 25 & 15 & & ns \\
    \hline \(T_{\text {pd }}\) & \multicolumn{2}{|l|}{\(\overline{\mathrm{CBI}}\) to CBO Delay} & \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\) & & 23 & 35 & & 23 & 30 & ns \\
    \hline \(\mathrm{T}_{\text {clk }}\) & \multicolumn{2}{|l|}{Clock to Output} & \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\) & & 10 & 25 & & 10 & 15 & ns \\
    \hline \(\mathrm{T}_{\mathrm{pzx}}\) & \multicolumn{2}{|l|}{Output Enable Delay} & \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\) & & 19 & 35 & & 19 & 30 & ns \\
    \hline \(\mathrm{T}_{\mathrm{pzx}}\) & \multicolumn{2}{|l|}{Output Disable Delay} & \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\) & & 15 & 35 & & 15 & 30 & ns \\
    \hline \(t_{H}\) & \multicolumn{2}{|l|}{Hold Time} & & 0 & -15 & & 0 & -15 & & ns \\
    \hline \(\mathrm{f}_{\text {max }}\) & \multicolumn{2}{|l|}{Maximum Frequency} & & 15.3 & 32 & & 22.2 & 32 & & MHz \\
    \hline
    \end{tabular}

    Test Load
    

    Test Waveforms
    

    Note \(A: V_{T}=1.5 \mathrm{~V}\).
    Note \(B: C_{L}\) includes probe and jig capacitance.
    Note C: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

    Schematic of Inputs and Outputs
    

    TL/L/10224-3
    

    TL/L/10224-6
    

    TL/L/10224-7
    

    \section*{DM74LS465/DM74LS466/DM74LS467/DM74LS468 TRI-STATE \({ }^{\circledR}\) Octal Buffers}

    \section*{General Description}

    These devices provide eight, two-input buffers in each package. All employ the newest low-power-Schottky TTL technology. One of the two inputs to each buffer is used as a control line to gate the output into the high-impedance state, while the other input passes the data through the buffer. The 'LS465 and 'LS467 present true data at the outputs, while the 'LS466 and 'LS468 are inverting. On the 'LS465 and 'LS466 versions, all eight TRI-STATE enable lines are common, with access through a 2 -input NOR gate. On the 'LS467 and 'LS468 versions, four buffers are enabled from one common line, and the other four buffers are enabled from another common line. In all cases the outputs are placed in the TRI-STATE condition by applying a high logic level to the enable pins. These devices represent octal, low power-Schottky versions of the very popular DM54/74365, 366, 367, and 368 (DM8095, 96, 97, and 98) TRI-STATE hex buffers.

    \section*{Features}
    - Octal versions of popular DM74365, 366, 367, and 368 (DM8095, 96, 97 and 98)
    - Typical power dissipation

    DM74LS465, 46780 mW
    DM74LS466, 46865 mW
    - Typical propagation delay

    DM74LS465, 46715 ns
    DM74LS466, 46810 ns
    - Low power-Schottky, TRI-STATE technology

    \section*{Connection Diagrams}

    Dual-In-Line Packages
    
    Absolute Maximum Ratings (Note)
    If Millitary/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    \begin{tabular}{lr} 
    DM74LS & 7 V \\
    Storage Temperature Range & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}\(\quad-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. the parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{l|l|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multirow{2}{*}{ Parameter } & \multicolumn{2}{|c|}{ DM74LS465, 466, 467, 468 } & \multirow{2}{*}{ Units } \\
    \cline { 3 - 4 } & & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -5.2 & mA \\
    \hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 24 & mA \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    \section*{'LS465 and 'LS467 Electrical Characteristics}
    over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{3}{|c|}{Conditions} & Min & \begin{tabular}{l}
    Typ \\
    (Note 1)
    \end{tabular} & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{3}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & 2.7 & & & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \multicolumn{3}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline & & \multicolumn{3}{|l|}{\(\mathrm{l}_{\mathrm{OL}}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\)} & & & 0.4 & \\
    \hline 1 & Input Current @Max Input Voltage & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{3}{|l|}{\(V_{C C}=\) Max, \(V_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}\)} & \(\mathrm{V}_{1}=0.5 \mathrm{~V}\) & A (Note 3) & & & -20 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & \multirow[t]{2}{*}{\(\mathrm{V}_{1}=0.4 \mathrm{~V}\)} & A (Note 4) & & & -50 & \\
    \hline & & & & \(\overline{\mathrm{G}}\) & & & -50 & \\
    \hline lozh & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{3}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline IozL & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{3}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=0.4 V \\
    & V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
    \end{aligned}
    \]} & & & -20 & \(\mu \mathrm{A}\) \\
    \hline los & Short Circuit Output Current & \multicolumn{3}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\text { Max } \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & -20 & & -100 & mA \\
    \hline ICC & Supply Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 3)} & & 16 & 26 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: Both \(\overline{\mathrm{G}}\) inputs are at 2 V .
    Note 4: Both \(\overline{\mathrm{G}}\) inputs are at 0.4 V .
    'LS465 and 'LS467 Switching Characteristics
    at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=667 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=150 \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & & 16 & & 25 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & & 28 & & 40 & ns \\
    \hline tpzH & Output Enable Time to High Level Output & & 25 & & 30 & ns \\
    \hline \(\mathrm{t}_{\text {PZL }}\) & Output Enable Time to Low Level Output & & 30 & & 42 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time from High Level Output (Note 1) & & 20 & & & ns \\
    \hline \(t_{\text {PLZ }}\) & Output Disable Time from Low Level Output (Note 1) & & 27 & & & ns \\
    \hline
    \end{tabular}

    \section*{Note 1: \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\).}

    \section*{'LS466 and 'LS468 Electrical Characteristics}
    over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{3}{|c|}{Conditions} & Min & Typ (Note 2) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{3}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{I}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM74 & 2.7 & & & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \multicolumn{3}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline & & \multicolumn{3}{|l|}{\(\mathrm{IOL}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\)} & & & 0.4 & \\
    \hline 1 & Input Current @Max Input Voltage & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline 1 IH & High Level Input Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{3}{*}{ILL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\(V_{C C}=\) Max} & \(\mathrm{V}_{1}=0.5 \mathrm{~V}\) & A (Note 4) & & & -20 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & \multirow[t]{2}{*}{\(\mathrm{V}_{1}=0.4 \mathrm{~V}\)} & A (Note 5) & & & -50 & \\
    \hline & & & & \(\overline{\mathrm{G}}\) & & & -50 & \\
    \hline lozh & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{3}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=2.4 V \\
    & V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
    \end{aligned}
    \]} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline lozl & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{3}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & -20 & \(\mu \mathrm{A}\) \\
    \hline los & Short Circuit Output Current & \multicolumn{3}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\text { Max } \\
    & \text { (Note 3) }
    \end{aligned}
    \]} & -20 & & -100 & mA \\
    \hline Icc & Supply Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 5)} & & 13 & 21 & mA \\
    \hline
    \end{tabular}

    Note 2: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 4: Both \(\overline{\mathrm{G}}\) inputs are at 2 V .
    Note 5: Both \(\overline{\mathrm{G}}\) inputs are at 0.4 V .
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multicolumn{7}{|l|}{\begin{tabular}{l}
    'LS466 and 'LS468 Switching Characteristics \\
    at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \end{tabular}} \\
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=667 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=150 \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & & 10 & & 16 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & & 17 & & 30 & ns \\
    \hline \(t_{\text {PZ }}\) & Output Enable Time to High Level Output & & 15 & & 30 & ns \\
    \hline \(\mathrm{t}_{\text {PZL }}\) & Output Enable Time to Low Level Output & & 35 & & 45 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time from High Level Output (Note 1) & & 20 & & & ns \\
    \hline tplz & Output Disable Time from Low Level Output (Note 1) & & 27 & & & ns \\
    \hline
    \end{tabular}

    \section*{Note 1: \(C_{L}=5 \mathrm{pF}\).}

    \section*{Function Tables}

    LS465
    \begin{tabular}{|c|c|c|c|}
    \hline \multicolumn{3}{|c|}{Inputs} & \multirow[t]{2}{*}{Output Y} \\
    \hline G1 & \(\overline{\mathbf{G} 2}\) & A & \\
    \hline H & X & X & \(\mathrm{Hi}-\mathrm{Z}\) \\
    \hline X & H & X & \(\mathrm{Hi}-\mathrm{Z}\) \\
    \hline L & L & H & H \\
    \hline L & L & L & L \\
    \hline
    \end{tabular}

    LS467
    \begin{tabular}{|cc|c|}
    \hline \multicolumn{2}{|c|}{ Inputs } & \multirow{2}{c|}{ Output } \\
    \cline { 1 - 2 } \(\mathbf{~} \mathbf{G}\) & \(\mathbf{A}\) & \(\mathbf{Y}\) \\
    \hline H & X & Hi-Z \\
    L & \(H\) & H \\
    L & L & L \\
    \hline
    \end{tabular}

    \footnotetext{
    \(H\) = High Logic Level
    L = Low Logic Level
    \(X=\) Either High or Low Logic Level
    \(\mathrm{Hi}-\mathrm{Z}=\) High Impedance (Off) State
    }

    LS466
    \begin{tabular}{|c|c|c|c|}
    \hline \multicolumn{3}{|c|}{Inputs} & \multirow[t]{2}{*}{Output Y} \\
    \hline G1 & \(\overline{\mathrm{G}} 2\) & A & \\
    \hline H & X & X & Hi-Z \\
    \hline X & H & X & \(\mathrm{Hi}-\mathrm{Z}\) \\
    \hline L & L & H & L \\
    \hline L & L & L & H \\
    \hline
    \end{tabular}

    LS468
    \begin{tabular}{|cc|c|}
    \hline \multicolumn{2}{|c|}{ Inputs } & \multirow{2}{c|}{ Output } \\
    \cline { 1 - 2 } \(\mathbf{~} \mathbf{G}\) & \(\mathbf{A}\) & \(\mathbf{Y}\) \\
    \hline H & X & \(\mathrm{Hi}-\mathrm{Z}\) \\
    L & H & L \\
    L & L & H \\
    \hline
    \end{tabular}

    \section*{DM54LS469/DM74LS469 8-Bit Up/Down Counter}

    \section*{General Description}

    The 'LS469 is an 8-bit synchronous up/down counter with parallel load and hold capability. Three function-select inputs ( \(\overline{\mathrm{LD}}, \overline{\mathrm{UD}}, \overline{\mathrm{CBI}}\) ) provide one of four operations which occur synchronously on the rising edge of the clock (CK).
    The LOAD operation loads the inputs ( \(D_{7}-D_{0}\) ) into the output register \(\left(Q_{7}-Q_{0}\right)\). The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE ( \(\overline{\mathrm{CBI}}=\mathrm{LOW}\) ), otherwise the operation is a HOLD. The carry-out \((\overline{\mathrm{CBO}})\) is TRUE \((\overline{\mathrm{CBO}}=\mathrm{LOW})\) when the output register \(\left(Q_{7}-Q_{0}\right)\) is all HIGHs, otherwise FALSE \((\overline{\mathrm{CBO}}=\mathrm{HIGH})\). The DECREMENT operation subtracts one from the output register when the borrow-in input is TRUE ( \(\overline{C B I}=\mathrm{LOW}\) ), otherwise the operation is a HOLD. The bor-row-out \((\overline{\mathrm{CBO}})\) is TRUE \((\overline{\mathrm{CBO}}=\mathrm{LOW})\) when the output register \(\left(Q_{7}-Q_{0}\right)\) is all LOWs, otherwise FALSE \((\overline{\mathrm{CBO}}=\mathrm{HIGH})\).

    The output register \(\left(Q_{7}-Q_{0}\right)\) is enabled when \(\overline{O E}\) is LOW, and disabled (HI-Z) when OE is HIGH. The output drivers will sink the 24 mA required for many bus-interface standards. Two or more 'LS469 octal up/down counters may be cascaded to provide larger counters.

    \section*{Features/Benefits}

    ■ 8-bit up/down counter for microprogram-counter, DMA controller and general-purpose counting applications
    - 8 bits matches byte boundaries
    - Bus-structured pinout
    - 24-pin SKINNYDIP saves space
    - TRI-STATE \({ }^{\circledR}\) outputs drive bus lines
    - Low current PNP inputs reduce loading
    - Expandable in 8 -bit increments

    \section*{Connection Diagram}
    

    TL/L/8333-1

    Order Number DM54LS469J, DM74LS469J or DM74LS469N
    See NS Package Number J24F or N24C

    \section*{Standard Test Load}
    

    \section*{Function Table}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \(\overline{O E}\) & CK & \(\overline{\text { LD }}\) & UD & CBI & D7-D0 & Q7-Q0 & Operation \\
    \hline H & X & X & X & X & X & Z & H-Z \\
    \hline L & \(\uparrow\) & L & X & X & D & D & LOAD \\
    \hline L & \(\uparrow\) & H & L & H & X & Q & HOLD \\
    \hline L & \(\uparrow\) & H & L & L & X & Q plus 1 & INCREMENT \\
    \hline L & \(\uparrow\) & H & H & H & \(x\) & Q & HOLD \\
    \hline L & \(\uparrow\) & H & H & L & X & Q minus 1 & DECREMENT \\
    \hline
    \end{tabular}

    \section*{Absolute Maximum Ratings}

    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage \(\mathrm{V}_{\mathrm{CC}}\)
    \(7 V\)
    Input Voltage
    5.5 V

    \section*{Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Operating Free-Air Temperature} & -55 & & 125* & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \multirow[b]{2}{*}{tw} & \multirow[t]{2}{*}{Width of Clock} & Low & 40 & & & 35 & 10 & & \multirow{2}{*}{ns} \\
    \hline & & High & 30 & & & 25 & & & \\
    \hline tsu & \multicolumn{2}{|l|}{Set Up Time} & 60 & & & 50 & & & \multirow[t]{2}{*}{ns} \\
    \hline \(t_{\text {h }}\) & \multicolumn{2}{|l|}{Hold Time} & 0 & -15 & & 0 & -15 & & \\
    \hline
    \end{tabular}
    *Case Temperature

    \section*{Electrical Characteristics Over Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & & Test Conditions & Min & Typ \(\dagger\) & Max & Units \\
    \hline \(V_{\text {IL }}\) & Low-Level Input Voltage & & & & & 0.8 & V \\
    \hline \(\mathrm{V}_{1 \text { H }}\) & High-Level Input Voltage & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IC }}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}\) & \(I_{1}=-18 \mathrm{~mA}\) & & & -1.5 & V \\
    \hline \(\mathrm{I}_{\text {IL }}\) & Low-Level Input Current & \(V_{C C}=\mathrm{MAX}\) & \(\mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -0.25 & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High-Level Input Current & \(V_{C C}=\) MAX & \(\mathrm{V}_{1}=2.4 \mathrm{~V}\) & & & 25 & \(\mu \mathrm{A}\) \\
    \hline 1 & Maximum Input Current & \(V_{C C}=\mathrm{MAX}\) & \(\mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low-Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}
    \end{aligned}
    \] & \begin{tabular}{ll} 
    MIL & \(\mathrm{I}_{\mathrm{OL}}=12 \mathrm{~mA}\) \\
    \hline COM & \(\mathrm{I}_{\mathrm{OL}}=24 \mathrm{~mA}\) \\
    \hline
    \end{tabular} & & & 0.5 & V \\
    \hline V OH & High-Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}
    \end{aligned}
    \] & \begin{tabular}{ll} 
    MIL & \(\mathrm{I}_{\mathrm{OH}}=-2 \mathrm{~mA}\) \\
    \hline COM & \(\mathrm{I}_{\mathrm{OH}}=-3.2 \mathrm{~mA}\) \\
    \hline
    \end{tabular} & 2.4 & & & V \\
    \hline Iozl & Off-State Output Current & \[
    \begin{aligned}
    & V_{C C}=\mathrm{MAX} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V}
    \end{aligned}
    \] & \(\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}\) & & & -100 & \(\mu \mathrm{A}\) \\
    \hline IOZH & & \[
    \mathrm{V}_{\mathrm{IH}}=2 \mathrm{~V}
    \] & \(\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}\) & & & 100 & \(\mu \mathrm{A}\) \\
    \hline los & Output Short-Circuit Current* & \(\mathrm{V}_{C C}=5.0 \mathrm{~V}\) & \(\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}\) & -30 & & -130 & mA \\
    \hline \(\mathrm{I}_{\mathrm{CC}}\) & Supply Current & \(V_{C C}=\mathrm{MAX}\) & & & 120 & 180 & mA \\
    \hline
    \end{tabular}
    *No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second
    \(\dagger\) All typical values are \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).

    \section*{Switching Characteristics Over Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Test Conditions (See Test Load/Waveforms)} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & \multirow{6}{*}{\[
    \begin{aligned}
    & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \\
    & \mathrm{R}_{1}=200 \Omega \\
    & \mathrm{R}_{2}=390 \Omega
    \end{aligned}
    \]} & 10.5 & & & 12.5 & & & MHz \\
    \hline \(t_{\text {PD }}\) & \(\overline{\mathrm{CBI}}\) to \(\overline{\mathrm{CBO}}\) Delay & & & 35 & 60 & & 35 & 50 & ns \\
    \hline \(t_{\text {PD }}\) & Clock to Q & & & 20 & 35 & & 20 & 30 & ns \\
    \hline \(t_{\text {PD }}\) & Clock to CBO & & & 55 & 95 & & 55 & 80 & ns \\
    \hline tpzx & Output Enable Delay & & & 20 & 45 & & 20 & 35 & ns \\
    \hline tpxz & Output Disable Delay & & & 20 & 45 & & 20 & 35 & ns \\
    \hline
    \end{tabular}

    LS469
    

    \section*{7 National \\ Semiconductor}

    \section*{DM54LS469A/DM74LS469A 8-Bit Up/Down Counter}

    \section*{General Description}

    The 'LS469A is an 8-bit synchronous up/down counter with parallel load and hold capability. Three function-select inputs ( \(\overline{\mathrm{LD}}, \overline{\mathrm{UD}}, \overline{\mathrm{CBI}}\) ) provide one of four operations which occur synchronously on the rising edge of the clock (CK).
    The LOAD operation loads the inputs (D7-D0) into the output register (Q7-Q0). The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE \((\overline{\mathrm{CBI}}=\mathrm{LOW})\), otherwise the operation is a HOLD. The carry-out ( \(\overline{\mathrm{CBO} \text { ) }) \text { is True (CBO }=\text { LOW) when }}\) the output register (Q7-Q0) is all HIGHs, otherwise FALSE \((\overline{C B O}=H I G H)\). The DECREMENT operation subtracts one from the output register when the borrow-in input is TRUE \((\overline{\mathrm{CBI}}=\mathrm{LOW})\), otherwise the operation is a HOLD. The bor-row-out \((\overline{\mathrm{CBO}})\) is true \((\overline{\mathrm{CBO}}=\mathrm{LOW})\) when the output register \((\mathrm{Q7}-\mathrm{QO})\) is all LOWs, otherwise FALSE \((\overline{\mathrm{CBO}}=\mathrm{HIGH})\).

    The output register (Q7-Q0) is enabled when \(\overline{O E}\) is LOW, and disabled ( \(\mathrm{HI}-\mathrm{Z}\) ) when \(\overline{\mathrm{OE}}\) is HIGH . The output drivers will sink the 24 mA required for many bus-interface standards. Two or more 'LS469A octal up/down counters may be cascaded to provide larger counters.

    \section*{Features}

    Octal Register for general purpose interfacing applications
    - 8 bits match byte boundaries
    - Low current PNP inputs reduce loading
    - Bus-structured pinout
    - TRI-STATE \({ }^{\circledR}\) outputs
    - 24-pin SKINNYDIP saves space

    \section*{Connection Diagram}
    

    TL/L/10223-1
    Order Number DM54LS469AJ, DM74LS469AJ, DM74LS469AN or DM74LS469AV See NS Package Number J24F, N24C or V28A
    Function Table
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline\(\overline{\mathbf{O E}}\) & \(\mathbf{C K}\) & \(\overline{\mathbf{L D}}\) & \(\overline{\mathbf{U D}}\) & \(\overline{\mathbf{C B I}}\) & \(\mathbf{D 7}\)-D0 & Q7-Q0 & Operation \\
    \hline H & X & X & X & X & X & Z & HI-Z \\
    L & \(\uparrow\) & L & X & X & D & D & LOAD \\
    L & \(\uparrow\) & H & L & H & X & Q & HOLD \\
    L & \(\uparrow\) & H & L & L & X & QPlus 1 & INCREMENT \\
    L & \(\uparrow\) & H & H & H & X & Q & HOLD \\
    L & \(\uparrow\) & H & H & L & X & Q Minus 1 & DECREMENT \\
    \hline
    \end{tabular}
    \begin{tabular}{lrl} 
    If Military/Aerospace specified devices are required, & ESD Tolerance \\
    please contact the National Semiconductor Sales & Czap \(=100 \mathrm{pF}\) \\
    Office/Distributors for availability and specifications. & Rzap \(=150 \Omega\) \\
    Supply Voltage \(\left(V_{\mathrm{CC}}\right)\) & 7 V & Test Method: Human Body Model \\
    Input Voltage & 5.5 V & Test Specification: NSC SOP 5-028 \\
    Off-State Output Voltage & 5.5 V & \\
    Storage Temperature & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) &
    \end{tabular}

    \section*{Recommended Operating Conditions}
    \begin{tabular}{l|l|c|c|c|c|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multirow{2}{*}{ Parameter } & \multicolumn{3}{|c|}{ Military } & \multicolumn{3}{c|}{ Commercial } & \multirow{2}{*}{ Units } \\
    \cline { 3 - 7 } & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & Operating Free-Air Temperature & -55 & 25 & & 0 & 25 & 75 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \(\mathrm{T}_{\mathrm{C}}\) & Operating Case Temperature & & & 125 & & & & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics Series 24A Over Recommended Operating Temperature Range
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{3}{|c|}{Test Conditions} & Min & Typ & Max & Units \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & \multicolumn{3}{|l|}{(Note 2)} & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & \multicolumn{3}{|l|}{(Note 2)} & & & 0.8 & V \\
    \hline \(V_{\text {IC }}\) & Input Clamp Voltage & \multicolumn{3}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{II}=-18 \mathrm{~mA}\)} & & -0.8 & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{VOH}^{\text {O}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M i n \\
    & V_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & V_{\mathrm{IH}}=2 \mathrm{~V}
    \end{aligned}
    \]} & \(\mathrm{l}_{\mathrm{OH}}=-2 \mathrm{~mA}\) & MIL & \multirow[b]{2}{*}{2.4} & \multirow[b]{2}{*}{2.9} & & \multirow[b]{2}{*}{V} \\
    \hline & & & \(\mathrm{IOH}=-3.2 \mathrm{~mA}\) & COM & & & & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \\
    & \hline
    \end{aligned}
    \]} & \(\mathrm{IOL}^{\prime}=12 \mathrm{~mA}\) & MIL & & \multirow[b]{2}{*}{0.3} & \multirow[b]{2}{*}{0.5} & \multirow[b]{2}{*}{V} \\
    \hline & & & \(\mathrm{IOL}^{\prime}=24 \mathrm{~mA}\) & COM & & & & \\
    \hline lozH & \multirow[t]{2}{*}{Off-State Output Current (Note 3)} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}
    \end{aligned}
    \]} & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}\)} & & & 100 & \(\mu \mathrm{A}\) \\
    \hline lozl & & & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}\)} & & & -100 & \(\mu \mathrm{A}\) \\
    \hline 1 & Maximum Input Current & \multicolumn{3}{|l|}{\(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{IIH}_{\mathrm{H}}\) & High Level Input Current (Note 3) & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 25 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current (Note 3) & \multicolumn{3}{|l|}{\(V_{C C}=M a x, V_{1}=0.4 \mathrm{~V}\)} & & -0.04 & -0.25 & mA \\
    \hline los & Output Short-Circuit Current & \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}\) (Note 4)} & -30 & -70 & -130 & mA \\
    \hline ICC & Supply Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}\)} & & 135 & 180 & mA \\
    \hline
    \end{tabular}

    Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device maybe operated at these values.

    Note 2: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
    Note 3: I/O leakage as the worst case of IOZX or IIX, e.g., IIL and IOZL.
    Note 4: During los measurement, only one output at a time should be grounded. Permanent damage otherwise may result.

    Switching Characteristics Over Recommended Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multirow[t]{2}{*}{Test Conditions} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline ts & \multicolumn{2}{|l|}{Set-Up Time from Input} & & 40 & 20 & & 30 & 20 & & ns \\
    \hline \multirow[t]{2}{*}{\({ }^{\text {tw }}\)} & \multirow[t]{2}{*}{Width of Clock} & High & & 20 & 7 & & 15 & 7 & & ns \\
    \hline & & Low & & 35 & 15 & & 25 & 15 & & ns \\
    \hline \(\mathrm{t}_{\mathrm{pd}}\) & \multicolumn{2}{|l|}{\(\overline{\mathrm{CBI}}\) to \(\overline{\mathrm{CBO}}\) Delay} & \(C_{L}=50 \mathrm{pF}\) & & 23 & 35 & & 23 & 30 & ns \\
    \hline \(\mathrm{t}_{\mathrm{clk}}\) & \multicolumn{2}{|l|}{Clock to Output} & \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\) & & 10 & 25 & & 10 & 15 & ns \\
    \hline \(\mathrm{t}_{\mathrm{pzx}}\) & \multicolumn{2}{|l|}{Output Enable Delay} & \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\) & & 19 & 35 & & 19 & 30 & ns \\
    \hline \(\mathrm{t}_{\mathrm{pzx}}\) & \multicolumn{2}{|l|}{Output Disable Delay} & \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\) & & 15 & 35 & & 15 & 30 & ns \\
    \hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Hold Time} & & 0 & -15 & & 0 & -15 & & ns \\
    \hline \(\mathrm{f}_{\text {max }}\) & \multicolumn{2}{|l|}{Maximum Frequency} & & 15.3 & 32 & & 22.2 & 32 & & MHz \\
    \hline
    \end{tabular}

    \section*{Test Load}
    

    TL/L/10223-2

    \section*{Test Waveforms}
    

    Note \(\mathrm{A}: \mathrm{VT}=1.5 \mathrm{~V}\).
    Note \(B: C_{L}\) includes probe and jig capacitance.
    Note C: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

    \section*{Schematic of Inputs and Outputs}
    

    TL/L/10223-3
    

    TL/L/10223-6

    Enable and Disable
    

    TL/L/10223-7
    

    \section*{54LS490/DM74LS490 Dual Decade Counter}

    \section*{General Description}

    The 'LS490 contains a pair of high speed 4-stage ripple counters. Each half of the 'LS490 has individual Clock, Master Reset and Master Set (Preset 9) inputs. Each section counts in the 8421 BCD code.

    \section*{Features}
    - Dual version of 54LS/74LS90
    - Individual asynchronous clear and preset to 9 for each counter
    - Count frequency-typically 65 MHz
    - Input clamp diodes limit high speed termination effects
    - TTL and CMOS compatible

    \section*{Connection Diagram}

    TL/F/10188-1
    Order Number 54LS490DMQB, 54LS490FMQB, DM54LS490M or DM54LS490N See NS Package Number J16A, M16A, N16E or W16A
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
    \hline MS & Master Set (Set to 9) Input (Active HIGH) \\
    MR & Master Reset Input (Active HIGH) \\
    \(\overline{C P}\) & Clock Pulse Input (Active Falling Edge) \\
    Q0-Q3 & Counter Outputs \\
    \hline
    \end{tabular}

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avallablity and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    \begin{tabular}{lr}
    54 LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS490} & \multicolumn{3}{|c|}{DM74LS490} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Veltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \(t_{w}(L)\) & \(\overline{\text { CP Pulse Width LOW }}\) & 12.5 & & & 12.5 & & & ns \\
    \hline \(t_{w}(\mathrm{H})\) & MR, MS Pulse Width HIGH & 20 & & & 20 & & & ns \\
    \hline \(t_{\text {rec }}\) & Recovery Time, MR or MS to \(\overline{\mathrm{CP}}\) & 15 & & & 15 & & & ns \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O H}=M a x, \\
    & V_{I L}=M a x
    \end{aligned}
    \]} & 54LS & 2.5 & & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & & & \\
    \hline \multirow[t]{3}{*}{VOL} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}_{\mathrm{OL}}=\operatorname{Max}, \\
    & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & & 0.5 & \\
    \hline & & \(\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & & 0.4 & \\
    \hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current @ Max Input Voltage} & \multirow[t]{2}{*}{\(V_{C C}=M a x, V_{1}=10 \mathrm{~V}\)} & Inputs & & & 100 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & \(\overline{\mathrm{CP}}\) & & & 200 & \\
    \hline \multirow[t]{2}{*}{1 H} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & Inputs & & & 20 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & \(\overline{\mathrm{CP}}\) & & & 40 & \\
    \hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & Inputs & -0.03 & & -0.4 & \multirow[t]{2}{*}{mA} \\
    \hline & & & \(\overline{C P}\) & -0.18 & & -2.4 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=M a x
    \] \\
    (Note 2)
    \end{tabular}} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\)} & & & 26 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multicolumn{5}{|l|}{\begin{tabular}{l}
    Switching Characteristics \\
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for test waveforms and output load)
    \end{tabular}} \\
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \(\mathrm{f}_{\text {max }}\) & Maximum Clock Frequency & 40 & & MHz \\
    \hline \begin{tabular}{l}
    tpLH \\
    tpHL
    \end{tabular} & Propagation Delay \(\overline{\mathrm{CP}}\) to Q0 & & \[
    \begin{aligned}
    & 15 \\
    & 15 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\overline{\mathrm{CP}}\) to Q1 or Q3 & & \[
    \begin{aligned}
    & 30 \\
    & 30 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\overline{\mathrm{CP}}\) to Q2 & & \[
    \begin{aligned}
    & 45 \\
    & 45 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay MS to Qn & & \[
    \begin{aligned}
    & 35 \\
    & 35 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \(t_{\text {teHL }}\) & Propagation Delay MR to Qn & & 39 & ns \\
    \hline
    \end{tabular}

    Logic Diagram (one-hali shown)
    

    TL/F/10188-4

    Logic Symbol
    

    TL/F/10188-2
    \(V_{C C}=\operatorname{Pin} 16\)
    GND \(=\operatorname{Pin} 8\)

    \section*{DM54LS491/74LS491 10-Bit Counter}

    \section*{General Description}

    The ten-bit counter can count up, count down, set, and load 2 LSB's, 2 MSB's and 6 middle bits high or low as a group. All operations are synchronous with the clock. SET overrides LOAD, COUNT and HOLD. LOAD overrides COUNT. COUNT is conditional on \(\mathrm{C}_{\mathbb{N}}\), otherwise it holds.
    All outputs are enabled when \(\overline{\mathrm{OE}}\) is low, otherwise HIGH-Z. The 24 mA IOL outputs are suitable for driving RAM/PROM address lines in video graphics systems.

    \section*{Connection Diagram}
    

    TL/L/8332-1
    Order Number DM54LS491J, DM74LS491J or DM74LS491N See NS Package Number J24F or N24C

    \section*{Features/Benefits}
    - CRT vertical and horizontal timing generation
    - Bus-structured pinout
    - 24-pin SKINNYDIP saves space
    - TRI-STATE \({ }^{\circledR}\) Outputs drive bus lines
    - Low current PNP inputs reduce loading

    \section*{Standard Test Load}
    

    \section*{Function Table}
    \begin{tabular}{|l|c|c|c|c|c|c|c|c|l|}
    \hline OE & CK & SET & LD & CNT & Clin \(_{\text {IN }}\) & UP & D9-D0 & Q9-Q0 & Operation \\
    \hline H & X & X & X & X & X & X & X & Z & Hi-Z \\
    L & \(\uparrow\) & H & X & X & X & X & X & H & Set all HIGH \\
    L & \(\uparrow\) & L & L & X & X & X & D & D & LOAD D \\
    L & \(\uparrow\) & L & H & H & X & X & X & Q & HOLD \\
    L & \(\uparrow\) & L & H & L & H & X & X & Q & HOLD \\
    L & \(\uparrow\) & L & H & L & L & L & X & Q plus 1 & Count UP \\
    L & \(\uparrow\) & L & H & L & L & H & X & Q minus 1 & Count DN \\
    \hline
    \end{tabular}

    If Military/Aerospace specified devices are required,
    please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage VCC
    7 V
    Input Voltage
    5.5 V

    Off-State Output Voltage
    5.5 V

    Storage Temperature
    \(-65^{\circ}\) to \(+150^{\circ} \mathrm{C}\)

    \section*{Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Operating Free-Air Temperature} & -55 & & 125* & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \multirow{2}{*}{\(t_{w}\)} & \multirow{2}{*}{Width of Clock} & High & 40 & & & 40 & & & \multirow{2}{*}{ns} \\
    \hline & & Low & 35 & & & 35 & & & \\
    \hline tsu & \multicolumn{2}{|l|}{Set-Up Time} & 60 & & & 50 & & & \multirow[t]{2}{*}{ns} \\
    \hline \(t_{\text {h }}\) & \multicolumn{2}{|l|}{Hold Time} & 0 & -15 & & 0 & -15 & & \\
    \hline
    \end{tabular}
    * Case temperature

    \section*{Electrical Characteristics Over Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{3}{|c|}{Test Conditions} & Min & Typ \(\dagger\) & Max & Units \\
    \hline VIL & Low-Level Input Voltage & & & & & & 0.8 & V \\
    \hline \(\mathrm{V}_{1 \mathrm{H}}\) & High-Level Input Voltage & & & & 2 & & & V \\
    \hline \(\mathrm{V}_{1 \mathrm{C}}\) & Input Clamp Voltage & \(\mathrm{V}_{C C}=\mathrm{MIN}\) & \(1=\) & & & & -1.5 & V \\
    \hline 1 lL & Low-Level Input Current & \(V_{C C}=\) MAX & \(V_{1}=\) & & & & -0.25 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High-Level Input Current & \(V_{C C}=\mathrm{MAX}\) & \(V_{1}=\) & & & & 25 & \(\mu \mathrm{A}\) \\
    \hline 11 & Maximum Input Current & \(V_{C C}=M A X\) & \(V_{1}=5\) & & & & 1 & mA \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low-Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}
    \end{aligned}
    \] & \begin{tabular}{l}
    MIL \\
    COM
    \end{tabular} & \[
    \begin{aligned}
    & \mathrm{l}_{\mathrm{OL}}=12 \mathrm{~mA} \\
    & \mathrm{I}_{\mathrm{OL}}=24 \mathrm{~mA}
    \end{aligned}
    \] & & & 0.5 & V \\
    \hline VOH & High-Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}
    \end{aligned}
    \] & \begin{tabular}{l}
    MIL \\
    COM
    \end{tabular} & \(\mathrm{IOH}=-2 \mathrm{~mA}\)
    \(\mathrm{I}_{\mathrm{OH}}=3.2 \mathrm{~mA}\) & 2.4 & & & V \\
    \hline lozl & Off-State Output Current & \[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{MAX} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V}
    \end{aligned}
    \] & & \(\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}\) & & & -100 & \(\mu \mathrm{A}\) \\
    \hline IOZH & & \(\mathrm{V}_{1 \mathrm{H}}=2 \mathrm{~V}\) & & \(\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}\) & & & 100 & \(\mu \mathrm{A}\) \\
    \hline los & Output Short-Circuit Current* & \(V_{C C}=5.0 \mathrm{~V}\) & & \(\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}\) & -30 & & \(-130\) & mA \\
    \hline \(\mathrm{I}_{\mathrm{CC}}\) & Supply Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}\) & & & & 120 & 180 & mA \\
    \hline
    \end{tabular}
    * No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
    \(\dagger\) All typical values are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\)

    \section*{Switching Characteristics Over Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multirow[t]{2}{*}{Test Conditions (See Test Load)} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow{2}{*}{Units} \\
    \hline & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & \multirow{4}{*}{\[
    \begin{aligned}
    & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \\
    & \mathrm{R}_{1}=200 \Omega \\
    & \mathrm{R}_{2}=390 \Omega
    \end{aligned}
    \]} & 10.5 & & & 12.5 & & & MHz \\
    \hline \(t_{\text {PD }}\) & Clock to Q & & & 20 & 35 & & 20 & 30 & ns \\
    \hline \(t_{\text {PZX }}\) & Output Enable Delay & & & 35 & 55 & & 35 & 45 & ns \\
    \hline tpxz & Output Disable Delay & & & 35 & 55 & & 35 & 45 & ns \\
    \hline
    \end{tabular}
    

    \section*{General Description}

    The ten-bit counter can count up, count down, set, and load 2 LSB's, 2 MSB's and 6 middle bits high or low as a group. All operations are synchronous with the clock. SET overrides LOAD, COUNT and HOLD. LOAD overrides COUNT. COUNT is conditional on \(\mathrm{C}_{\mathbb{N}}\), otherwise it holds.
    All outputs are enabled when OE is low, otherwise HIGH-Z. The 24 mA IOL outputs are suitable for driving RAM/PROM address lines in video graphics systems.

    \section*{Features}
    - CRT vertical and horizontal timing generation
    - Bus-structured pinout
    - Low current PNP inputs reduce loading
    - TRI-STATE \({ }^{@}\) outputs
    - 24-pin SKINNYDIP saves space

    \section*{Connection Diagram}
    

    TL/L/10222-1
    Order Number DM54LS491AJ, DM74LS491AJ, DM74LS491AN or DM74LS491AV See NS Package Number J24F, N24C or V28A

    \section*{Function Table}
    \begin{tabular}{|l|c|c|c|c|c|c|c|c|l|}
    \hline\(\overline{\mathbf{O E}}\) & CK & SET & LD & \(\overline{\text { CNT }}\) & CIN \(_{\text {IN }}\) & \(\overline{\text { UP }}\) & D9-D0 & Q9-Q0 & Operation \\
    \hline H & X & X & X & X & X & X & X & Z & Hi-Z \\
    L & \(\uparrow\) & H & X & X & X & X & X & H & Set all HIGH \\
    L & \(\uparrow\) & L & L & X & X & X & D & D & LOAD D \\
    L & \(\uparrow\) & L & H & H & X & X & X & Q & HOLD \\
    L & \(\uparrow\) & L & H & L & H & X & X & Q & HOLD \\
    L & \(\uparrow\) & L & H & L & L & L & X & QPlus 1 & Count Up \\
    L & \(\uparrow\) & L & H & L & L & H & X & Q Minus 1 & Count Down \\
    \hline
    \end{tabular}
    \begin{tabular}{lr} 
    Absolute Maximum Ratings (Note 1) \\
    If Military/Aerospace specified devices are required, \\
    please contact the National & Semiconductor Sales \\
    Office/Distributors for availability and specifications. \\
    Supply Voltage, V VCC & 7 V \\
    Input Voltage & 5.5 V \\
    Off-State Output Voltage & \(5 . \mathrm{V}^{2}\) \\
    Storage Temperature & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    ESD Tolerance
    \(>1000 \mathrm{~V}\)
    Czap \(=100 \mathrm{pF}\)
    Rzap \(=1500 \Omega\)
    Test Method: Human Body Model
    Test Specification: NSC SOP 5-028

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Operating Free-Air Temperature & -55 & 25 & & 0 & 25 & 75 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \(\mathrm{T}_{\mathrm{C}}\) & Operating Case Temperature & & & 125 & & & & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics Series 24A Over Recommended Operating Temperature Range
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|r|}{Conditions} & Min & Typ & Max & Units \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & \multicolumn{2}{|l|}{(Note 2)} & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & \multicolumn{2}{|l|}{(Note 2)} & & & 0.8 & V \\
    \hline \(V_{\text {IC }}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{II}=-18 \mathrm{~mA}\)} & & -0.8 & -1.5 & V \\
    \hline \multirow[t]{2}{*}{V OH} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Min} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}
    \end{aligned}
    \]} & \(\mathrm{I}_{\mathrm{OH}}=-2 \mathrm{~mA} \quad\) MIL & \multirow[b]{2}{*}{2.4} & \multirow[b]{2}{*}{2.9} & & \multirow[b]{2}{*}{V} \\
    \hline & & & \(\mathrm{IOH}=-3.2 \mathrm{~mA} \quad \mathrm{COM}\) & & & & \\
    \hline \multirow[t]{2}{*}{VOL} & \multirow[t]{2}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\mathrm{Min} \\
    & V_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}
    \end{aligned}
    \]} & \(\mathrm{IOL}=12 \mathrm{~mA} \quad \mathrm{MIL}\) & & \multirow[b]{2}{*}{0.3} & \multirow[b]{2}{*}{0.5} & \multirow[b]{2}{*}{V} \\
    \hline & & & \(\mathrm{IOL}=24 \mathrm{~mA} \quad \mathrm{COM}\) & & & & \\
    \hline lozh & \multirow[t]{2}{*}{Off-State Output Current (Note 3)} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{I L}=0.8 \mathrm{~V} \\
    & V_{I H}=2 \mathrm{~V} \\
    & \hline
    \end{aligned}
    \]} & \(\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}\) & & & 100 & \(\mu \mathrm{A}\) \\
    \hline Iozl & & & \(\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}\) & & & -100 & \(\mu \mathrm{A}\) \\
    \hline 1 & Maximum Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \({ }_{1 / \mathrm{H}}\) & High Level Input Current (Note 3) & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.4 \mathrm{~V}\)} & & & 25 & \(\mu \mathrm{A}\) \\
    \hline I/L & Low Level Input Current (Note 3) & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=0.4 V\)} & & -0.04 & -0.25 & mA \\
    \hline los & Outut Short-Circuit Current & \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) & \(\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}\) (Note 4) & -30 & \(-70\) & \(-130\) & mA \\
    \hline ICC & Supply Current & \(V_{C C}=\) Max & & & 135 & 180 & mA \\
    \hline
    \end{tabular}

    Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.
    Note 2: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

    Note 3: I/O leakage as the worst case of IOZX or IIX, e.g., IIL and IOZL.
    Note 4: During los measurement, only one output at a time should be grounded. Permanent damage otherwise may result.

    Switching Characteristics Over Recommended Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow{2}{*}{Parameter}} & \multirow{2}{*}{Test Condition} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow{2}{*}{Units} \\
    \hline & & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(\mathrm{ts}_{5}\) & \multicolumn{2}{|l|}{Setup Time from Input} & & 40 & 20 & & 30 & 20 & & ns \\
    \hline \multirow[t]{2}{*}{tw} & \multirow[t]{2}{*}{Width of Clock} & High & & 20 & 7 & & 15 & 7 & & ns \\
    \hline & & Low & & 35 & 15 & & 25 & 15 & & ns \\
    \hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Hold Time} & & 0 & -15 & & 0 & -15 & & ns \\
    \hline tCLK & \multicolumn{2}{|l|}{Clock to Output} & \(C_{L}=50 \mathrm{pF}\) & & 10 & 25 & & 10 & 15 & ns \\
    \hline tpzx & \multicolumn{2}{|l|}{Output Enable Delay} & \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\) & & 19 & 35 & & 19 & 30 & ns \\
    \hline tpxz & \multicolumn{2}{|l|}{Output Disable Delay} & \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\) & & 15 & 35 & & 15 & 30 & ns \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & \multicolumn{2}{|l|}{Maximum Frequency} & & 15.3 & 32 & & 22.2 & 32 & & MHz \\
    \hline
    \end{tabular}

    Test Load
    

    \section*{Test Waveforms}
    

    Note \(A: V_{T}=1.5 \mathrm{~V}\).
    Note \(\mathrm{B}: \mathrm{C}_{\mathrm{L}}\) includes probe and jig capacitance.
    Note B: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

    Schematic of Inputs and Outputs
    

    TL/L/10222-3
    

    TL/L/10222-5
    Enable and Disable
    
    

    \section*{DM54LS498/DM74LS498 Octal Shift Register}

    \section*{General Description}

    The LS498 is an 8-bit synchronous shift register with parallel load and hold capability. Two function select inputs \(\left(l_{0}, l_{1}\right)\) provide one of four operations which occur synchronously on the rising edge of the clock (CK).
    The LOAD operation loads the input ( \(D_{7}-D_{0}\) ) into the output register \(\left(\mathrm{Q}_{7}-\mathrm{Q}_{0}\right)\). The HOLD operation holds the previous value regardless of clock transitions. The SHIFT LEFT operation shifts the output register, \(Q\), one bit to the left; \(Q_{0}\) is replaced by LIRO. RILO outputs \(Q_{7}\).
    The SHIFT RIGHT operation shifts the output register, \(Q\), one bit to the right; \(Q_{7}\) is replaced by RILO. LIRO outputs \(Q_{0}\).
    The output register \(\left(Q_{7}-Q_{0}\right)\)-is enabled when \(\overline{O E}\) is LOW, and disabled ( \(\mathrm{HI}-\mathrm{Z}\) ) when \(\overline{\mathrm{OE}}\) is HIGH . The output drivers will sink the 24 mA required for many bus interface standards.

    Two or more LS498 octal shift registers may be cascaded to provide larger shift registers as shown in the application section.

    \section*{Features/Benefits}
    - Octal shift register for serial to parallel and parallel to serial applications
    - 8 bits match byte boundaries
    - Bus-structured pinout
    - 24-pin SKINNYDIP saves space
    - TRI-STATE \({ }^{\circledR}\) outputs drive bus lines
    - Low current PNP inputs reduce loading
    - Expandable in 8 -bit increments

    \section*{Connection Diagram}
    

    TL/L/8331-1
    Order Number DM54LS498J, DM74LS498J or DM74LS498N
    See NS Package Number J24F or N24C

    \section*{Standard Test Load}
    

    Function Table
    \begin{tabular}{|c|c|c|c|c|c|l|}
    \hline\(\overline{\mathbf{O E}}\) & \(\mathbf{C K}\) & \(\mathbf{I}_{\mathbf{1}}\) & \(\mathbf{I}_{\mathbf{0}}\) & \(\mathbf{D}_{\mathbf{7}}-\mathbf{D}_{\mathbf{0}}\) & \(\mathbf{Q}_{\mathbf{7}}-\mathbf{Q}_{\mathbf{0}}\) & \multicolumn{1}{|c|}{ Operation } \\
    \hline\(H\) & \(X\) & \(X\) & \(X\) & \(X\) & \(Z\) & HI-Z \\
    L & \(\uparrow\) & L & L & \(X\) & L & HOLD \\
    L & \(\uparrow\) & L & \(H\) & \(X\) & SR(Q) & SHIFT RIGHT \\
    L & \(\uparrow\) & \(H\) & \(L\) & \(X\) & SL(Q) & SHIFT LEFT \\
    L & \(\uparrow\) & \(H\) & \(H\) & \(D\) & \(D\) & LOAD \\
    \hline
    \end{tabular}
    Supply Voltage \(V_{C C}\)
    7V
    Input Voltage
    5.5 V

    \section*{Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Operating Free-Air Temperature} & -55 & & 125* & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \multirow[b]{2}{*}{\(t_{\text {w }}\)} & \multirow[t]{2}{*}{Width of Clock} & Low & 40 & & & 35 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & High & 30 & & & 25 & & & \\
    \hline \(\mathrm{t}_{\mathrm{su}}\) & \multicolumn{2}{|l|}{Set-Up Time} & 60 & & & 50 & & & \multirow[t]{2}{*}{ns} \\
    \hline \(t_{h}\) & \multicolumn{2}{|l|}{Hold Time} & 0 & -15 & & 0 & -15 & & \\
    \hline
    \end{tabular}
    * Case temperature

    Electrical Characteristics Over Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{3}{|c|}{Test Conditions} & Min & Typ \(\dagger\) & Max & Units \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low-Level Input Voltage & & & & & & 0.8 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High-Level Input Voltage & & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IC }}\) & Input Clamp Voltage & \(\mathrm{V}_{C C}=\mathrm{MIN}\) & \(l_{1}=-\) & & & & -1.5 & V \\
    \hline \(1 / 2\) & Low-Level Input Current & \(V_{C C}=M A X\) & \(V_{1}=0\). & & & & -0.25 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High-Level Input Current & \(V_{C C}=\mathrm{MAX}\) & \(\mathrm{V}_{1}=2\). & & & & 25 & \(\mu \mathrm{A}\) \\
    \hline 1 & Maximum Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}\) & \(V_{1}=5\). & & & & 1 & mA \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{2}{*}{Low-Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}
    \end{aligned}
    \]} & & \(\mathrm{IOL}^{\prime}=12 \mathrm{~mA}\) & & & 0.5 & V \\
    \hline & & & COM & \(\mathrm{I}_{\mathrm{OL}}=24 \mathrm{~mA}\) & & & & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{VOH}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High-Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{HH}}=2 \mathrm{~V}
    \end{aligned}
    \]} & MIL & \(\mathrm{lOH}^{\text {O }}=-2 \mathrm{~mA}\) & \multirow[t]{2}{*}{2.4} & & & V \\
    \hline & & & COM & \(\mathrm{IOH}=-3.2 \mathrm{~mA}\) & & & & \\
    \hline lozl & \multirow{2}{*}{Off-State Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\mathrm{MAX} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{HH}}=2 \mathrm{~V}
    \end{aligned}
    \]} & & \(\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}\) & & & -100 & \(\mu \mathrm{A}\) \\
    \hline l OH & & & & \(\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}\) & & & 100 & \(\mu \mathrm{A}\) \\
    \hline los & Output Short-Circuit Current* & \multicolumn{2}{|l|}{\(V_{C C}=5.0 \mathrm{~V}\)} & \(\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}\) & -30 & & -130 & mA \\
    \hline ICC & Supply Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}\)} & & 120 & 180 & mA \\
    \hline
    \end{tabular}
    *No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
    \(\dagger\) All typical values are at \(V_{C C}=5 \mathrm{~V}, T_{A}=25^{\circ} \mathrm{C}\)
    Switching Characteristics Over Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Test Conditions (See Test Load)} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & \multirow{6}{*}{\[
    \begin{aligned}
    & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \\
    & \mathrm{R}_{1}=200 \Omega \\
    & \mathrm{R}_{2}=390 \Omega
    \end{aligned}
    \]} & 10.5 & & & 12.5 & & & MHz \\
    \hline \(t_{\text {PD }}\) & 10, 11 to LIRO, RILO & & & 35 & 60 & & 35 & 50 & ns \\
    \hline \(t_{\text {PD }}\) & Clock to Q & & & 20 & 35 & & 20 & 30 & ns \\
    \hline \(t_{\text {PD }}\) & Clock to LIRO, RILO & & & 55 & 95 & & 55 & 80 & ns \\
    \hline tPZX & Output Enable Delay & & & 35 & 55 & & 35 & 45 & ns \\
    \hline tpxz & Output Disable Delay & & & 35 & 55 & & 35 & 45 & ns \\
    \hline
    \end{tabular}

    Octal Shift Register
    

    TL/L/8331-3

    \section*{DM54LS498A/DM74LS498A Octal Shift Register}

    \section*{General Description}

    The LS498A is an 8-bit synchronous shift register with parallel load and hold capability. Two function-select inputs ( \(l_{0}\), \(\mathrm{I}_{1}\) ) provide one of four operations which occur synchronously on the rising edge of the clock (CK).
    The LOAD operation loads the inputs (D7-D0) into the output register (Q7-Q0). The HOLD operation holds the previous value regardless of clock transitions. The SHIFT LEFT operation shifts the output register \(Q\), one bit to the left; Q0 is replaced by LIRO. LIRO outputs Q0.
    The output register (Q7-Q0)-is enabled when \(\overline{O E}\) is LOW, and disabled ( \(\mathrm{HI}-\mathrm{Z}\) ) when \(\overline{\mathrm{OE}}\) is HIGH . The output drivers will sink the 24 mA required for many bus interface standards.

    Two or more LS498 octal shift registers may be cascaded to provide larger shift registers as shown in the application.

    \section*{Features}
    - Octal shift register for serial to parallel and parallel to serial applications
    - 8 bits match byte boundaries
    - Low current PNP inputs reduce loading
    - Bus-structured pinout
    - TRI-STATE \({ }^{\oplus}\) outputs
    - 24-pin SKINNYDIP saves space
    - Expandable in 8 -bit increments

    \section*{Connection Diagram}
    

    TL/L/10221-1

    \section*{Order Number DM54LS498AJ, DM74LS498AJ, DM74LS498AN or DM74LS498AV}

    See NS Package Number J24F, N24C or V28A

    \section*{Function Table}
    \begin{tabular}{|c|c|c|c|c|c|l|}
    \hline\(\overline{\mathbf{O E}}\) & \(\mathbf{C K}\) & \(\mathbf{1 1}\) & 10 & D7-D0 & Q7-Q0 & \multicolumn{1}{|c|}{ Operation } \\
    \hline H & \(X\) & \(X\) & \(X\) & \(X\) & \(Z\) & HI-Z \\
    L & \(\uparrow\) & L & L & X & L & HOLD \\
    L & \(\uparrow\) & L & H & X & SR(Q) & SHIFTRIGHT \\
    L & \(\uparrow\) & \(H\) & L & X & SL(Q) & SHIFT LEFT \\
    L & \(\uparrow\) & \(H\) & \(H\) & D & D & LOAD \\
    \hline
    \end{tabular}

    Absolute Maximum Ratings (Note 1)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    \(\begin{array}{lr}\text { Supply Voltage VCC } & 7 \mathrm{~V} \\ \text { Input Voltage } & 5.5 \mathrm{~V} \\ \text { Off-State Output Voltage } & 5.5 \mathrm{~V}\end{array}\)
    \begin{tabular}{lr} 
    Storage Temperature & \(-65^{\circ}\) to \(+150^{\circ} \mathrm{C}\) \\
    ESD Tolerance & \(>1000 \mathrm{~V}\) \\
    Czap \(=100 \mathrm{pF}\) & \\
    Rzap \(=1500 \Omega\) & \\
    Test Method: Human Body Model & \\
    Test Specification: NSC SOP 5-028 &
    \end{tabular}

    Test Specification: NSC SOP 5-028

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(\mathrm{V}_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{T}_{\text {A }}\) & Operating Free-Air Temperature & -55 & 25 & & 0 & 25 & 75 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \(\mathrm{T}_{\mathrm{C}}\) & Operating Case Temperature & & & 125 & & & & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics Series 24A Over Recommended Operating Temperature Range
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|r|}{Test Conditions} & Min & Typ & Max & Units \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & \multicolumn{2}{|l|}{(Note 2)} & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & \multicolumn{2}{|l|}{(Note 2)} & & & 0.8 & V \\
    \hline \(V_{\text {IC }}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & -0.8 & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Min} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \\
    & \hline
    \end{aligned}
    \]} & \(\mathrm{IOH}^{\prime}=-2 \mathrm{~mA} \quad\) MIL & \multirow[b]{2}{*}{2.4} & \multirow[b]{2}{*}{2.9} & & \multirow[b]{2}{*}{V} \\
    \hline & & & \(\mathrm{IOH}^{\prime}=-3.2 \mathrm{~mA} \mathrm{COM}\) & & & & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Min} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \\
    & \hline
    \end{aligned}
    \]} & \(\mathrm{l}_{\mathrm{OL}}=12 \mathrm{~mA} \quad \mathrm{MIL}\) & & \multirow[b]{2}{*}{0.3} & \multirow[b]{2}{*}{0.5} & \multirow[b]{2}{*}{V} \\
    \hline & & & \(\mathrm{IOL}^{\prime}=24 \mathrm{~mA} \quad \mathrm{COM}\) & & & & \\
    \hline lozh & \multirow[t]{2}{*}{Off-State Output Current (Note 3)} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max} \\
    & V_{I L}=0.8 \mathrm{~V} \\
    & V_{I H}=2 \mathrm{~V} \\
    & \hline
    \end{aligned}
    \]} & \(\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}\) & & & 100 & \(\mu \mathrm{A}\) \\
    \hline lozl & & & \(\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}\) & & & -100 & \(\mu \mathrm{A}\) \\
    \hline 11 & Maximum Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current (Note 3) & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.4 \mathrm{~V}\)} & & & 25 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current (Note 3) & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}\)} & & -0.04 & -0.25 & mA \\
    \hline los & Output Short-Circuit Current & \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) & \(\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}\) (Note 4) & -30 & -70 & \(-130\) & mA \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x\)} & & 135 & 180 & mA \\
    \hline
    \end{tabular}

    Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.
    Note 2: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
    Note 3: I/O leakage as the worst case of IOZX or IIX, e.g., IIL and IOZL.
    Note 4: During los measurement, only one output at a time should be grounded. Permanent damage otherwise may result.

    Switching Characteristics Over Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Parameter}} & \multirow[t]{2}{*}{Test Conditions} & \multicolumn{3}{|c|}{Military} & \multicolumn{3}{|c|}{Commercial} & \multirow[t]{2}{*}{Units} \\
    \hline & & & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(\mathrm{T}_{S}\) & \multicolumn{2}{|l|}{Setup Time from Input} & & 40 & 20 & & 30 & 20 & & ns \\
    \hline \multirow[t]{2}{*}{\(\mathrm{T}_{W}\)} & \multirow[t]{2}{*}{Width of Clock} & High & & 20 & 7 & & 15 & 7 & & ns \\
    \hline & & Low & & 35 & 15 & & 25 & 15 & & ns \\
    \hline \(\mathrm{T}_{\mathrm{PD}}\) & \multicolumn{2}{|l|}{10, I1 to LIRO, RILO} & \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\) & & 23 & 35 & & 23 & 30 & ns \\
    \hline TCLK & \multicolumn{2}{|l|}{Clock to Output} & \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\) & & 10 & 25 & & 10 & 15 & ns \\
    \hline TPZX & \multicolumn{2}{|l|}{Output Enable Delay} & \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\) & & 19 & 35 & & 19 & 30 & ns \\
    \hline \(T_{P X}\) & \multicolumn{2}{|l|}{Output Disable Delay} & \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\) & & 15 & 35 & & 15 & 30 & ns \\
    \hline \(\mathrm{T}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Hold Time} & & 0 & -15 & & 0 & -15 & & ns \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & \multicolumn{2}{|l|}{Maximum Frequency} & & 15.3 & 32 & & 22.2 & 32 & & MHz \\
    \hline
    \end{tabular}

    \section*{Test Load}
    

    Test Waveforms
    

    Note \(A: V_{T}=1.5 \mathrm{~V}\).
    Note \(B: C_{L}\) includes probe and jig capacitance.
    Note C: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

    Schematic of Inputs and Outputs
    

    TL/L/10221-3

    Pulse Width
    

    TL/L/10221-6

    Enable and Disable
    

    TL/L/10221-7
    

    \section*{54LS502/DM74LS502}

    \section*{8-Bit Successive Approximation Register}

    \section*{General Description}

    The LS502 is an 8-bit register with the interstage logic necessary to perform serial-to-parallel conversion and provide an active LOW Conversion Complete ( \(\overline{\mathrm{CC}}\) ) signal coincident with storage of the eighth bit. An active LOW Start ( \(\overline{\mathrm{S}}\) ) input performs synchronous initialization which forces Q7 LOW and all other outputs HIGH. Subsequent clocks shift this Q7 LOW signal downstream which simultaneously backfills the register such that the first serial data ( \(D\) input) bit is stored in Q7, the second bit in Q6, the third in Q5, etc. The serial input data is also synchronized by an auxiliary flip-flop and brought out on \(Q_{D}\).

    Designed primarily for use in the successive approximation technique for analog-to-digital conversion, the LS502 can also be used as a serial-to-parallel converter ring counter and as the storage and control element in recursive digital routines.

    \section*{Features}
    - Low power Schottky version of 2502
    - Storage and control for successive approximation A to D conversion
    - Performs serial-to-parallel conversion

    \section*{Connection Diagram}
    

    TL/F/10189-1
    Order Number 54LS502DMQB, 54LS502FMQB, DM74LS502WM or DM74LS502N
    See NS Package Number J16A, M16B, N16E or W16A

    \section*{Logic Symbol}
    
    \(V_{C C}=\operatorname{Pin} 16\)
    GND \(=\operatorname{Pin} 8\)
    \begin{tabular}{|l|l|}
    \hline \begin{tabular}{c} 
    Pin \\
    Names
    \end{tabular} & \multicolumn{1}{c|}{ Description } \\
    \hline D & Serial Data Input \\
    \(\bar{S}\) & Start Input (Active LOW) \\
    CP & Clock Pulse Input (Active Rising Edge) \\
    \(\mathrm{Q}_{\mathrm{D}}\) & Synchronized Serial Data Output \\
    \(\overline{\mathrm{CC}}\) & Conversion Complete Output (Active LOW) \\
    \(\mathrm{Q} 0-\mathrm{Q7}\) & Parallel Register Outputs \\
    \(\overline{\mathrm{Q} 7}\) & Complement of Q7 Output \\
    \hline
    \end{tabular}

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avallabllity and specifications.
    \begin{tabular}{lr} 
    Supply Voltage & 7 V \\
    Input Voltage & 7 V \\
    Operating Free Air Temperature Range & \\
    54 LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS502} & \multicolumn{3}{|c|}{DM74LS502} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW \(\bar{S}\) to CP & \[
    \begin{array}{r}
    5 \\
    5 \\
    \hline
    \end{array}
    \] & & & \[
    \begin{array}{r}
    5 \\
    5
    \end{array}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Hold Time HIGH or LOW \(\overline{\mathrm{S}}\) to CP & \[
    \begin{aligned}
    & 5 \\
    & 5
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 5 \\
    & 5
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L})
    \end{aligned}
    \] & Setup Time HIGH or LOW D to CP & \[
    \begin{array}{r}
    5 \\
    5 \\
    \hline
    \end{array}
    \] & & & \[
    \begin{aligned}
    & 5 \\
    & 5
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Hold Time HIGH or LOW D to CP & \[
    \begin{aligned}
    & 5 \\
    & 5
    \end{aligned}
    \] & & & \[
    \begin{array}{r}
    5 \\
    5 \\
    \hline
    \end{array}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{w}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{w}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & CP Pulse Width HIGH or LOW & \[
    \begin{aligned}
    & 20 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 20 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & 54LS & 2.5 & & & V \\
    \hline & & & DM74 & 2.7 & & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\text {OL }}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}} \operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \\
    \hline & & & DM74 & & & 0.5 & V \\
    \hline & & \(\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=10 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline I/L & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -1.2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & 54LS & -20 & & -100 & mA \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x\)} & & & 65 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Note more than one output should be shorted at a time, and the duration should not exceed one second.

    Switching Characteristics \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for test waveforms and output loads)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \(f_{\text {max }}\) & Maximum Clock Frequency & 25 & & MHz \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(C P\) to \(Q_{n}\) or \(\overline{C C}\) & & \[
    \begin{aligned}
    & 35 \\
    & 25
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}

    \section*{Functional Description}

    The register stages are composed of transparent RS latches arranged in master/slave pairs. The master and slave latches are enabled separately by non-overlapping complementary signals \(\phi 1\) and \(\phi 2\) derived internally from the CP input. Master latches are enabled when CP is LOW and slave latches are enabled when CP is HIGH. Information is transferred from master to slave, and thus to the outputs, by the LOW-to-HIGH transition of CP.
    Initializing the register requires a LOW signal on \(\overline{\mathrm{S}}\) while exercising CP. With \(\overline{\mathrm{S}}\) and CP LOW, all master latches are SET (Q side HIGH). A LOW-to-HIGH CP transition, with \(\overline{\mathrm{S}}\) remaining LOW, then forces the slave latches to the condition wherein Q7 is LOW and all other register outputs, including \(\overline{\mathrm{CC}}\), are HIGH. This condition will prevail as long as \(\overline{\mathrm{S}}\) remains LOW, regardless of subsequent CP rising edge. To start the conversion process, \(\overline{\mathrm{S}}\) must return to the HIGH state. On the next CP rising edge, the information stored in the serial data input latch is transferred to \(Q_{D}\) and \(Q 7\), while Q6 is forced to the LOW state. On the rising edge of the next seven clocks, this LOW signal is shifted downstream, one bit at a time, while the serial data enters the register position one bit behind this LOW signal, as shown in the Truth Table. Note that after a serial data bit appears at a particular output, that register position undergoes no further changes. After the shifted LOW signal reaches \(\overline{\mathrm{CC}}\), the register is locked up and no further changes can occur until the register is initialized for the next conversion process.
    Figure a shows a simplified hook-up of a LS502, a D/A converter and a comparator arranged to convert an analog input voltage into an 8 -bit binary number by the successive approximation technique. Figure \(b\) is an idealized graph showing the various values that the D/A converter output voltage can assume in the course of the conversion. The vertical axis is calibrated in fractions of the full-scale output capability of the D/A converter and the horizontal axis represents the successive states of the Truth Table. At time t1, Q7 is LOW and Q6-Q0 are HIGH, causing the D/A output to be one-half of full scale. If the analog input voltage is greater than this voltage the comparator output (hence the D input of the LS502) will be LOW, and at times t2 the D/A output will rise to three-fourths of full scale because Q7 will remain LOW and contribute \(50 \%\) while Q6 is forced LOW and contributes another \(25 \%\). On the other hand, if the ana\(\log\) input voltage is less than one-half of full scale, the comparator output will be HIGH and Q7 will go HIGH at t2. Q6 will still be forced LOW at t2, and the D/A output will decrease to \(25 \%\) of full scale. Thus with each successive clock, the D/A output will change by smaller increments. When the conversion is completed at \(t 9\), the binary number represented by the register outputs will be the numerator of the fraction \(n / 256\), representing the analog input voltage as a fraction of the full scale output D/A converter.
    

    TL/F/10189-4
    FIGURE \(a\).
    

    TL/F/10189-5
    FIGURE b.

    Truth Table
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[b]{2}{*}{\[
    \begin{gathered}
    \text { Time } \\
    t_{\mathrm{n}} \\
    \hline
    \end{gathered}
    \]} & \multicolumn{2}{|r|}{Inputs} & \multicolumn{10}{|c|}{Outputs} \\
    \hline & D & \(\overline{\mathbf{S}}\) & \(Q_{D}\) & Q7 & Q6 & Q5 & Q4 & Q3 & Q2 & Q1 & Q0 & \(\overline{\mathbf{C C}}\) \\
    \hline 0 & X & L & X & X & X & X & X & X & X & X & X & X \\
    \hline 1 & D7 & H & X & L & H & H & H & H & H & H & H & H \\
    \hline 2 & D6 & H & D7 & D7 & L & H & H & H & H & H & H & H \\
    \hline 3 & D6 & H & D6 & D7 & D6 & L & H & H & H & H & H & H \\
    \hline 4 & D4 & H & D5 & D7 & D6 & D5 & L & H & H & H & H & H \\
    \hline 5 & D3 & H & D4 & D7 & D6 & D5 & D4 & L & H & H & H & H \\
    \hline 6 & D2 & H & D3 & D7 & D6 & D5 & D4 & D3 & L & H & H & H \\
    \hline 7 & D1 & H & D2 & D7 & D6 & D5 & D4 & D3 & D2 & L & H & H \\
    \hline 8 & D0 & H & D1 & D7 & D6 & D5 & D4 & D3 & D2 & D1 & L & H \\
    \hline 9 & X & H & D0 & D7 & D6 & D5 & D4 & D3 & D2 & D1 & DO & L \\
    \hline 10 & X & H & X & D7 & D6 & D5 & D4 & D3 & D2 & D1 & D0 & L \\
    \hline
    \end{tabular}

    H = HIGH Voltage Level
    \(L=\) LOW Voltage Level
    \(X=\) Immaterial
    Logic Diagram
    

    Note: Cell logic is repeated for register stages Q5 to Q1.

    \section*{54LS503/DM74LS503}

    \section*{8-Bit Successive Approximation Register (with Expansion Control)}

    \section*{General Description}

    The 'LS503 register is basically the same as the 'LS502 except that it has an active LOW Enable ( \(\bar{E}\) ) input that is used in cascading two or more packages for longer word lengths. A HIGH signal on \(\bar{E}\), after a START operation, forces Q7 HIGH and prevents the device from accepting serial data. With the \(\bar{E}\) input of an 'LS503 connected to the \(\overline{\mathrm{CC}}\) output of a preceding (more significant) device, the 'LS503 will be inhibited until the preceding device is filled, causing its \(\overline{C C}\) output to go LOW. This LOW signal then enables the 'LS503 to accept the serial data on subsequent clocks. For a description of the starting, shifting and conversion operations, please see the 'LS502 data sheet.

    \section*{Features}

    ■ Performs serial-to-parallel conversion
    - Expansion control for longer words
    - Storage and control for successive approximation A to D conversion
    ■ Low power Schottky version of 2503

    \section*{Connection Diagram}

    \section*{Dual-In-Line Package}
    

    \section*{Logic Symbol}
    

    TL/F/10190-2
    \(V_{C C}=\operatorname{Pin} 16\)
    GND \(=\operatorname{Pin} 8\)

    TL/F/10190-1
    Order Number 54LS503DMQB, 54LS503FMQB, D74LS503WM or DM74LS503N
    See NS Package Number J16A, M16B, N16E or W16A
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
    \hline D & Serial Data Input \\
    \(\bar{S}\) & Start Input (Active LOW) \\
    CP & Clock Pulse Input (Active Rising Edge) \\
    \(\overline{\mathrm{E}}\) & Conversion Enable Input (Active LOW) \\
    \(\overline{\mathrm{CC}}\) & Conversion Complete Output (Active LOW) \\
    Q0-Q7 & Parallel Register Outputs \\
    \(\overline{\mathrm{Q} 7}\) & Complement of Q7 Output \\
    \hline
    \end{tabular}

    \section*{Absolute Maximum Ratings (Note)}

    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range

    54LS
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    DM74LS
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    Storage Temperature Range

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{54LS503} & \multicolumn{3}{|c|}{DM74LS503} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Voltage & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & t_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW \(\bar{S}\) to CP & \[
    \begin{aligned}
    & 5 \\
    & 5
    \end{aligned}
    \] & & & \[
    \begin{array}{r}
    5 \\
    5 \\
    \hline
    \end{array}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L) \\
    & \hline
    \end{aligned}
    \] & Hold Time HIGH or LOW \(\bar{S}\) to CP & \[
    \begin{aligned}
    & 5 \\
    & 5
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 5 \\
    & 5 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW \(\overline{\mathrm{S}}\) to CP & \[
    \begin{aligned}
    & 5 \\
    & 5
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 5 \\
    & 5
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{th}_{\mathrm{h}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{h}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Hold Time HIGH or LOW D to CP & \[
    \begin{aligned}
    & 5 \\
    & 5
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 5 \\
    & 5
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{w}(H) \\
    & t_{w}(L) \\
    & \hline
    \end{aligned}
    \] & CP Pulse Width HIGH or LOW & \[
    \begin{aligned}
    & 20 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & & & \[
    \begin{aligned}
    & 20 \\
    & 20
    \end{aligned}
    \] & & & ns \\
    \hline
    \end{tabular}

    Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\text { Max, } \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & 54LS & 2.5 & & & v \\
    \hline & & & DM74 & 2.7 & & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 54LS & & & 0.4 & \multirow{3}{*}{V} \\
    \hline & & & DM74 & & & 0.5 & \\
    \hline & & \(\mathrm{IOL}^{\text {a }}\) 4 mA, & DM74 & & & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=10 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}\)} & & & -0.8 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Max} \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & 54LS & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & & 65 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    Switching Characteristics
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \(f_{\text {max }}\) & Maximum Count Frequency & 25 & & MHz \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay CP to Qn or \(\overline{\mathrm{CC}}\) & & \[
    \begin{array}{r}
    35 \\
    25 \\
    \hline
    \end{array}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay E to Q7 & & \[
    \begin{aligned}
    & 20 \\
    & 24 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}

    \section*{Logic Diagram}
    

    Note: Cell logic is repeated for register stages Q5 to Q1.

    Connection for Longer Word Lengths
    

    TL/F/10190-4

    \section*{DM74LS533}

    \section*{Octal Transparent Latch with TRI-STATE \({ }^{\circledR}\) Outputs}

    \section*{General Description}

    The 'LS533 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ( \(\overline{(\mathrm{OE})}\) is LOW. When \(\overline{\mathrm{OE}}\) is HIGH the bus output is in the high impedance state. The 'LS533 is the same as the 'LS373, except that the outputs are inverted. For detailed
    specifications please see the 'LS373 data sheet, but note that the propagation delays from data to output are 5.0 ns longer for the 'LS533 than for the 'LS373.

    \section*{Features}
    - Eight latches in a single package
    - TRI-STATE outputs for bus interfacing

    \section*{Connection Diagram}

    Dual-In-Line Package
    

    \section*{Logic Symbol}
    

    TL/F/9811-2
    \(\mathrm{V}_{\mathrm{CC}}=\operatorname{Pin} 20\)
    GND \(=\operatorname{Pin} 10\)

    TL/F/9811-1
    Order Number DM74LS533WM or DM74LS533N
    See NS Package Number M20B or N20A
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
    \hline D0, D7 & Data Inputs \\
    LE & Latch Enable Input (Active HIGH) \\
    \(\overline{\mathrm{OE}}\) & Output Enable Input (Active LOW) \\
    \(\overline{\mathrm{O} 0-\overline{\mathrm{O}} 7}\) & Complementary TRI-STATE Outputs \\
    \hline
    \end{tabular}
    \begin{tabular}{lr} 
    Absolute Maximum Ratings (Note) \\
    If Military/Aerospace specified devices are required, \\
    please contact the National Semiconductor Sales \\
    Office/Distributors for availability and specifications. \\
    Supply Voltage & 7 V \\
    Input Voltage & 7 V \\
    Operating Free Air Temperature Range \\
    DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{l|l|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multirow{2}{|c|}{ Parameter } & \multicolumn{2}{|c|}{ DM74LS533 } & \multirow{2}{*}{ Units } \\
    \cline { 3 - 5 } & & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -0.4 & mA \\
    \hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 24 & mA \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    \section*{Electrical Characteristics}

    Over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{l}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\text { Max, } \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \] & DM74 & 2.7 & 3.4 & & V \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\text { Max }, \\
    & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \] & DM74 & & 0.35 & 0.5 & V \\
    \hline & & \(\mathrm{l}_{\mathrm{OL}}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=10 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{IH}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline los & Short Circuit Output Current & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
    & \text { (Note 2) } \\
    & \hline
    \end{aligned}
    \] & DM74 & -20 & & -100 & mA \\
    \hline ICCZ & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & & 46 & mA \\
    \hline lozl & TRI-STATE Output Off Current LOW & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCH}} \\
    & \mathrm{~V}_{\mathrm{OZL}}=0.4 \mathrm{~V}
    \end{aligned}
    \]} & & & -20.0 & \(\mu \mathrm{A}\) \\
    \hline lozh & TRI-STATE Output Off Current HIGH & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCH}} \\
    & \mathrm{~V}_{\mathrm{OZH}}=2.7 \mathrm{~V}
    \end{aligned}
    \]} & & & 20.0 & \(\mu \mathrm{A}\) \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{Switching Characteristics}
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\[
    \begin{aligned}
    & C_{\mathrm{L}}=15 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \\
    & \hline
    \end{aligned}
    \]} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{~T}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay Data to \(\bar{Q}_{x}\) & & \[
    \begin{aligned}
    & 32 \\
    & 23 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay LE to \(\bar{Q}_{x}\) & & \[
    \begin{aligned}
    & 36 \\
    & 25 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PZL}} \\
    & \mathrm{t}_{\mathrm{PZH}} \\
    & \hline
    \end{aligned}
    \] & Output Enable Time \(\overline{O E}\) to \(\bar{Q}_{x}\) & & \[
    \begin{gathered}
    22 \\
    2 \\
    \hline
    \end{gathered}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \text { tpHZ } \\
    & \mathrm{t}_{\mathrm{PLZ}} \\
    & \hline
    \end{aligned}
    \] & Output Enable Time \(\overline{O E}\) to \(\bar{Q}_{x}\) & & \[
    \begin{array}{r}
    34 \\
    27 \\
    \hline
    \end{array}
    \] & ns \\
    \hline
    \end{tabular}

    \section*{DM74LS534}

    Octal D-Type Flip-Flop (With TRI-STATE \({ }^{\circledR}\) Outputs)

    \section*{General Description}

    The 'LS534 is a high speed, low power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRISTATE outputs for bus oriented applications. A buffered Clock (CP) and Output Enable ( \(\overline{\mathrm{OE}}\) ) is common to all flipflops. The 'LS534 is the same as the 'LS374 except that the outputs are inverted.

    \section*{Connection Diagram}
    

    \section*{Logic Symbol}
    

    TL/F/9812-2
    \[
    V_{C C}=\operatorname{Pin} 20
    \]
    \[
    \text { GND }=\operatorname{Pin} 10
    \]

    TL/F/9812-1
    Order Number DM74LS534WM or DM74LS534N
    See NS Package Number M20B or N20A
    \begin{tabular}{|l|l|}
    \hline Pin Name & \multicolumn{1}{|c|}{ Description } \\
    \hline\(D 0-D 7\) & Data Inputs \\
    \(\overline{C P}\) & Clock Pulse Input (Active Rising Edge) \\
    \(\overline{\mathrm{OE}}\) & TRI-STATE Output Enable Input (Active LOW) \\
    \(\overline{\mathrm{O}} 0-\overline{\mathrm{O}} 7\) & Complementary TRI-STATE Outputs \\
    \hline
    \end{tabular}

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range

    \section*{DM74LS}

    Storage Temperature Range
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM74LS534} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Current & & & -2.6 & mA \\
    \hline lOL & Low Level Output Current & & & 24 & mA \\
    \hline TA & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW
    \[
    D_{n} \text { to } \overline{C P}
    \] & \[
    \begin{aligned}
    & 20 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L) \\
    & \hline
    \end{aligned}
    \] & Hold Time HIGH or LOW
    \[
    D_{n} \text { to } \overline{C P}
    \] & \[
    \begin{aligned}
    & 0 \\
    & 0 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{w}(H) \\
    & t_{w}(L) \\
    & \hline
    \end{aligned}
    \] & CP Pulse Width HIGH or LOW & \[
    \begin{aligned}
    & 15 \\
    & 15 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\) & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\
    & V_{\mathrm{IL}}=\operatorname{Max} \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \] & 2.4 & 3.3 & & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \\
    & \hline
    \end{aligned}
    \] & & 0.35 & 0.5 & \multirow[t]{2}{*}{V} \\
    \hline & & \(\mathrm{I}_{\mathrm{OL}}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=7 \mathrm{~V}\) & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\) & & & 20 & \(\mu \mathrm{A}\) \\
    \hline I/L & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\) & & & -20 & \(\mu \mathrm{A}\) \\
    \hline l OZH & Off-State Output Current with High Level Output Voltage Applied & \[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=2.4 V \\
    & V_{I H}=\operatorname{Min}, V_{I L}=M a x
    \end{aligned}
    \] & & & 20 & \(\mu \mathrm{A}\) \\
    \hline lozl & Off-State Output Current with Low Level Output Voltage Applied & \[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{\mathrm{O}}=0.4 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \] & & & -20 & \(\mu \mathrm{A}\) \\
    \hline los & Short Circuit Output Current & \[
    \begin{aligned}
    & V_{C C}=\text { Max } \\
    & (\text { Note 2) }
    \end{aligned}
    \] & -20 & & -100 & mA \\
    \hline ICC & Supply Current & \(\mathrm{V}_{C C}=\mathrm{Max}\) (Note 3) & & 45 & & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: ICC is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5 V .

    \section*{Switching Characteristics}
    \(V_{C C}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for test waveforms and output loads)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|l|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=45 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \(f_{\text {max }}\) & Maximum Clock Frequency & 35 & & MHz \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(t_{\text {PHL }}\)
    \end{tabular} & Propagation Delay CP to \(Q_{n}\) & & \[
    \begin{aligned}
    & 28 \\
    & 28 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PZH}} \\
    & \mathrm{t}_{\mathrm{PZL}} \\
    & \hline
    \end{aligned}
    \] & Output Enable Time & & \[
    \begin{array}{r}
    28 \\
    28 \\
    \hline
    \end{array}
    \] & ns \\
    \hline \[
    t_{P H Z}
    \]
    \[
    t_{p L z}
    \] & Output Disable Time & & \[
    \begin{aligned}
    & 20 \\
    & 25
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}

    \section*{Functional Description}

    The '534 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual \(D\) inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transistion. With the Output Enable ( \(\overline{\mathrm{OE}}\) ) LOW, the contents of the eight flip-flops are available at the outputs. When the \(\overline{O E}\) is HIGH, the outputs go to the high impedance state. Operation of the \(\overline{\mathrm{OE}}\) input does not affect the state of the flip-flops.

    \section*{Truth Table}
    \begin{tabular}{|c|c|c|c|}
    \hline \multicolumn{2}{|c|}{ Inputs } & \multicolumn{2}{c|}{ Outputs } \\
    \hline\(D_{\boldsymbol{n}}\) & \(\mathbf{C P}\) & \(\mathbf{O E}\) & \(\mathbf{O}_{\boldsymbol{n}}\) \\
    \hline\(H\) & \(\Gamma\) & L & L \\
    L & \(\Gamma\) & L & H \\
    \(X\) & \(X\) & \(H\) & \(Z\) \\
    \hline
    \end{tabular}
    \(H=\) HIGH Voltage Level
    \(\mathrm{L}=\) LOW Voltage Level
    \(X=\) Immaterial
    z = High Impedance

    \section*{Logic Diagram}
    

    TL/F/9812-3

    \section*{DM74LS540 \\ Octal Buffer/Line Driver with TRI-STATE \({ }^{\circledR}\) Outputs}

    \section*{General Description}

    The DM74LS540 is similar in function to the 'LS240, except that the inputs and outputs are on opposite sides of the package (see Connection Diagram). This pinout arrangement makes this device especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

    Features
    - Hysteresis at inputs to improve noise margin
    - PNP inputs reduce loading
    - TRI-STATE outputs drive bus lines
    - Inputs and outputs opposite side of package, allowing easier interface to microprocessors
    - Fully TTL and CMOS compatible

    \section*{Connection Diagram}

    Dual-In-Line Package
    

    TL/F/9813-1
    Order Number DM74LS540WM or DM74LS540N
    See NS Package Number M20B or N20A
    \begin{tabular}{|l|l|}
    \hline Pin Name & \multicolumn{1}{|c|}{ Description } \\
    \hline\(\overline{\text { E1, E2 }}\) & Output Enable (Active Low) \\
    \(10-7\) & Data Inputs \\
    \(00-7\) & Data Outputs \\
    \hline
    \end{tabular}

    \section*{Truth Table}
    \begin{tabular}{|c|c|c|c|}
    \hline \multicolumn{3}{|c|}{ Inputs } & \multirow{2}{*}{ Outputs } \\
    \hline E1 & E2 & D & \\
    \hline L & L & H & L \\
    H & X & X & Z \\
    X & H & X & Z \\
    L & L & L & H \\
    \hline
    \end{tabular}

    \footnotetext{
    \(H=\) HIGH Voltage Level
    \(\mathrm{L}=\) LOW Voltage Level
    X \(=\) Immaterial
    Z = High Impedance
    }
    ```

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for availability and specifications.
    Supply Vóltage 7V
    Input Voltage 7V
    Operating Free Air Temperature
    DM74LS
    $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$
    Storage Temperature Range
    $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

    ```

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{l|l|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multirow{2}{|c|}{ Parameter } & \multicolumn{2}{|c|}{ DM74LS540 } & \multirow{2}{*}{ Units } \\
    \cline { 3 - 4 } & & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -3 & mA \\
    \hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 24 & mA \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    \section*{Electrical Characteristics}

    Over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & Typ (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\) & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \] & 2.7 & 3.4 & & V \\
    \hline \multirow[t]{2}{*}{V \({ }_{\text {OL }}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\text { Max, } \\
    & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \] & & 0.35 & 0.5 & \multirow[t]{2}{*}{V} \\
    \hline & & \(\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=10 \mathrm{~V}\) & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}_{\text {H }}\) & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\) & & & 20 & \(\mu \mathrm{A}\) \\
    \hline I/L & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -0.2 & mA \\
    \hline los & Short Circuit Output Current & \begin{tabular}{l}
    \[
    V_{C C}=M a x
    \] \\
    (Note 3)
    \end{tabular} & -50 & & -225 & mA \\
    \hline ICC & Supply Current & \(V_{C C}=\) Max & & & 50 & mA \\
    \hline lozH & TRI-STATE Output Off Current High & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCH}}, \mathrm{V}_{\mathrm{OZH}}=2.7 \mathrm{~V}\) & & & 20 & \(\mu \mathrm{A}\) \\
    \hline lozl & TRI-STATE Output Off Current Low & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCH}}, \mathrm{V}_{\mathrm{OZL}}=0.4 \mathrm{~V}\) & & & -20 & \(\mu \mathrm{A}\) \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at at time, and the duration should not exceed one second.

    \section*{Switching Characteristics}
    at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 or Test Waveforms and Output Loading)
    \begin{tabular}{l|l|l|l|c|c}
    \hline Symbol & Parameter & Conditions & Min & Max & Units \\
    \hline\(t_{P L H}\) & Propagation Delay & \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\) & & 14 & ns \\
    \(\mathrm{t}_{\mathrm{PHL}}\) & Data to Output & & 18 & ns \\
    \hline \(\mathrm{t}_{\mathrm{PZH}}\) & Output Enable Time & \(\mathrm{R}_{\mathrm{L}}=667 \Omega, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\) & & 23 & \multirow{2}{*}{ns} \\
    \(\mathrm{t}_{\mathrm{PZL}}\) & & & 30 & \\
    \hline \(\mathrm{t}_{\mathrm{PLZ}}\) & Output Disable Time & \(\mathrm{R}_{\mathrm{L}}=667 \Omega, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\) & & 25 & n \\
    \(\mathrm{t}_{\mathrm{PHZ}}\) & & & 18 & ns \\
    \hline
    \end{tabular}
    \({ }^{*} D C\) limits apply over operating temperature range; \(A C\) limits apply at \(T_{A}=+25^{\circ}\) and \(V_{C C}=+5.0 \mathrm{~V}\).

    \section*{DM74LS563}

    \section*{Octal D-Type Latch with TRI-STATE \({ }^{\circledR}\) Outputs}

    \section*{General Description}

    The 'LS563 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ( \(\overline{\mathrm{OE}})\) inputs.
    This device is functionally indentical to the 'LS573, but has inverted outputs.

    \section*{Connection Diagram}
    

    \section*{Logic Symbol}
    

    TL/F/10214-2
    \[
    \begin{aligned}
    & V_{C C}=\operatorname{Pin} 20 \\
    & \mathrm{GND}=\operatorname{Pin} 10
    \end{aligned}
    \]

    TL/F/10214-1
    Order Number DM74LS563WM or DM74LS563N
    See NS Package Number M20B or N20A
    \begin{tabular}{|l|l|}
    \hline \multicolumn{1}{|c|}{\begin{tabular}{c} 
    Pin \\
    Names
    \end{tabular}} & \multicolumn{1}{|c|}{ Description } \\
    \hline D0-D7 & Data Inputs \\
    LE & Latch Enable Input (Active HIGH) \\
    \(\overline{\text { OE }}\) & TRI-STATE Output Enable Input (Active LOW) \\
    \(\bar{O} 0-\bar{O} 7\) & TRI-STATE Latch Outputs \\
    \hline
    \end{tabular}
    

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM74LS563} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -2.6 & mA \\
    \hline lOL & Low Level Output Current & & & 24 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW Dn to LE & \[
    \begin{aligned}
    & 0 \\
    & 0 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L)
    \end{aligned}
    \] & Hold Time HIGH or LOW Dn to LE & \[
    \begin{aligned}
    & 10 \\
    & 10 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{w}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{w}}(\mathrm{~L})
    \end{aligned}
    \] & LE Pulse Width HIGH or LOW & \[
    \begin{aligned}
    & 15 \\
    & 15
    \end{aligned}
    \] & & & ns \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & \begin{tabular}{l}
    Typ \\
    (Note 1)
    \end{tabular} & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\) & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \] & 2.4 & 3.3 & & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\text { Max } \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \] & & 0.35 & 0.5 & \multirow[t]{2}{*}{V} \\
    \hline & & \(\mathrm{l}_{\mathrm{OL}}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & & 0.25 & 0.4 & \\
    \hline 11 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}\) & & & 0.1 & mA \\
    \hline \(\mathrm{I}_{1}\) & High Level Input Current & \(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\) & & & 20 & \(\mu \mathrm{A}\) \\
    \hline ILL & Low Level Input Current & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\) & & & -20 & \(\mu \mathrm{A}\) \\
    \hline IOZH & Off-State Output Current with High Level Output Voltage Applied & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \] & & & 20 & \(\mu \mathrm{A}\) \\
    \hline lozl & Off-State Output Current with Low Level Output Voltage Applied & \[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=0.4 V \\
    & V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
    \end{aligned}
    \] & & & -20 & \(\mu \mathrm{A}\) \\
    \hline los & Short Circuit Output Current & \[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \] & -20 & & -100 & mA \\
    \hline ICC & Supply Current & \(V_{C C}=\operatorname{Max}\) (Note 3) & & & 40 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3 : \(\mathrm{I}_{\mathrm{CC}}\) is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5 V .

    \section*{Switching Characteristics}
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for test waveforms and output loading)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\[
    \begin{aligned}
    & R_{\mathrm{L}}=2 \mathrm{k} \Omega \\
    & \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\
    & \hline
    \end{aligned}
    \]} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    tpHL
    \end{tabular} & Propagation Delay Dn to On & & \[
    \begin{aligned}
    & 23 \\
    & 25 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(\mathrm{t}_{\mathrm{PHL}}\)
    \end{tabular} & Propagation Delay LE to On & & \[
    \begin{aligned}
    & 35 \\
    & 35
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PZH}} \\
    & \mathrm{t}_{\mathrm{PZL}}
    \end{aligned}
    \] & Output Enable Time & & \[
    \begin{aligned}
    & 28 \\
    & 36 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \text { tpHZ } \\
    & \text { tpLZ }^{2}
    \end{aligned}
    \] & Output Disable Time & & \[
    \begin{aligned}
    & 20 \\
    & 25 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}

    \section*{Functional Description}

    The 'LS563 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the \(D\) in-
    puts a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ( \(\overline{\mathrm{OE}})\) input. When \(\overline{O E}\) is LOW, the buffers are in the bi-state mode. When \(\overline{O E}\) is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

    \section*{Logic Diagram}
    

    \section*{DM74LS564}

    Octal D-Type Flip-Flop (with TRI-STATE® Outputs)

    \section*{General Description}

    The 'LS564 is a high speed low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ( \(\overline{\mathrm{OE}})\). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition
    This device is functionally identical to the 'LS574, but has inverted outputs. For complete discussions of operations, truth tables, AC and DC electrical specifications, refer to the 'LS374 data sheet.

    \section*{Features}

    ■ Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
    ■ Useful as input or output port for microprocessors
    - Functionally identical to 'LS574
    - Input clamp diodes limit high speed termination effects
    - Fully TTL and CMOS compatible

    \section*{Connection Diagram}

    \section*{Logic Symbol}
    

    TL/F/10191-2
    \(V_{C C}=\operatorname{Pin} 20\)
    GND \(=\operatorname{Pin} 10\)

    TL/F/10191-1
    Order Number DM74LS564WM or DM74LS564N
    See NS Package Number M20B or N20A
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
    \hline DO-D7 & Data Inputs \\
    CP & Clock Pulse Input (Active Rising Edge) \\
    \(\overline{\mathrm{OE}}\) & TRI-STATE® Output Enable Input \\
    & (Active LOW) \\
    \(\overline{\mathrm{O} 0-\bar{O} 7}\) & TRI-STATE Outputs \\
    \hline
    \end{tabular}
    

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{l|l|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multirow{2}{|c|}{ Parameter } & \multicolumn{2}{|c|}{ DM74LS564 } & \multirow{2}{*}{ Units } \\
    \cline { 3 - 5 } & & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -2.6 & mA \\
    \hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 24 & mA \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & Typ (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \(V_{C C}=\operatorname{Min}, \_{1}=-18 \mathrm{~mA}\) & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\text { Max, } \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \] & 2.7 & 3.4 & & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \] & & 0.35 & 0.5 & V \\
    \hline & & \(\mathrm{IOL}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \(V_{C C}=M a x, V_{1}=10 \mathrm{~V}\) & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\) & & & 20 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -0.4 & mA \\
    \hline los & Short Circuit Output Current & \[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Max} \\
    & (\text { Note 2) }
    \end{aligned}
    \] & -30 & & -130 & mA \\
    \hline lcc & Supply Current & \(V_{C C}=M a x\) & & & 60 & mA \\
    \hline lozh & TRI-STATE Output OFF Current HIGH & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCH}}, \mathrm{V}_{\mathrm{OZH}}=2.7 \mathrm{~V}\) & & & 20 & \(\mu \mathrm{A}\) \\
    \hline lozl & TRI-STATE Output OFF Current LOW & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCH}}, \mathrm{V}_{\mathrm{OZL}}=0.4 \mathrm{~V}\) & & & -20 & \(\mu \mathrm{A}\) \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{Switching Characteristics}
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for test waveforms and output load)
    \begin{tabular}{|c|c|c|c|c|}
    \hline Symbol & Parameter & Min & Max & Units \\
    \hline \[
    \begin{aligned}
    & t_{\mathrm{PLH}} \\
    & t_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay CP to \(\overline{\text { On }}\) & & \[
    \begin{array}{r}
    28 \\
    28 \\
    \hline
    \end{array}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PZH}} \\
    & \mathrm{t}_{\mathrm{PZL}} \\
    & \hline
    \end{aligned}
    \] & Enable Time \(\overline{\mathrm{OE}}\) to \(\overline{\mathrm{O}} \mathrm{n}\) & & \[
    \begin{array}{r}
    28 \\
    28 \\
    \hline
    \end{array}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PHZ}} \\
    & \mathrm{t}_{\mathrm{PLZ}} \\
    & \hline
    \end{aligned}
    \] & Enable Time \(\overline{O E}\) to \(\bar{O} n\) & & \[
    \begin{aligned}
    & 20 \\
    & 25 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \(\mathrm{t}_{\text {s }}\) & Setup Time Dn to CP & 5 & & ns \\
    \hline \(t_{n}\) & Hold Time Dn to CP & 5 & & ns \\
    \hline \[
    \begin{aligned}
    & t_{w}(H) \\
    & t_{w}(L)
    \end{aligned}
    \] & Pulse Width (HIGH/LOW) CP & \[
    \begin{aligned}
    & 20 \\
    & 10 \\
    & \hline
    \end{aligned}
    \] & & ns \\
    \hline
    \end{tabular}

    \section*{DM74LS573}

    \section*{Octal D-Type Latch (with TRI-STATE \({ }^{\circledR}\) Outputs)}

    \section*{General Description}

    The 'LS573 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ( \(\overline{\mathrm{OE}}\) ) inputs.
    This device is functionally identical to the 'LS373, but has different pinouts. For truth tables, discussion of operations and AC and DC specifications, please refer to the 'LS373 data sheet.

    \section*{Features}
    - Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
    - Useful as input or output port for microprocessors
    - Functionally identical to 'LS373
    - Input clamp diodes limit high speed termination effects
    - Fully TTL and CMOS compatible

    \section*{Connection Diagram}
    

    \section*{Logic Symbol}
    

    TL/F/9814-2
    \[
    V_{C C}=\operatorname{Pin} 20
    \]

    GND \(=\operatorname{Pin} 10\)

    TL/F/9814-1
    Order Number DM74LS573WM or DM74LS573N
    See NS Package Number M20B or N20A
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{|c|}{ Description } \\
    \hline DO-D7 & Data Inputs \\
    LE & Latch Enable Input (Active HIGH) \\
    \(\overline{O E}\) & \begin{tabular}{l} 
    TRI-STATE Output Enable Input (Active LOW) \\
    OO-O7 \\
    TRI-STATE Latch Outputs
    \end{tabular} \\
    \hline
    \end{tabular}

    \section*{Absolute Maximum Ratings (Note)}

    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    DM74LS
    Storage Temperature Range
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    Recommended Operating Conditions
    \begin{tabular}{l|l|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multirow{2}{|c|}{ Parameter } & \multicolumn{2}{c|}{ DM74LS } & \multirow{2}{*}{ Units } \\
    \cline { 3 - 5 } & & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Input Current & & & -2.6 & mA \\
    \hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 24 & mA \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    \section*{Electrical Characteristics}

    Over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \(V_{C C}=\operatorname{Min}, \mathrm{l}_{\mathrm{J}}=-18 \mathrm{~mA}\) & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \] & 2.7 & 3.4 & & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}=\text { Max, } \\
    & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \] & & 0.35 & 0.5 & \multirow[t]{2}{*}{V} \\
    \hline & & \(\mathrm{IOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=10 \mathrm{~V}\) & & & 1 & mA \\
    \hline \({ }_{1 / H}\) & High Level Input Current & \(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\) & & & 20 & \(\mu \mathrm{A}\) \\
    \hline I/L & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -0.4 & mA \\
    \hline los & Short Circuit Output Current & \[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \] & -30 & & \(-130\) & mA \\
    \hline ICC & Supply Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) & & & 50 & mA \\
    \hline lozh & TRI-STATE Output off Current High & \[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCH}} \\
    & \mathrm{~V}_{\mathrm{OZH}}=2.7 \mathrm{~V}
    \end{aligned}
    \] & & & 20 & \(\mu \mathrm{A}\) \\
    \hline lozl & TRI-STATE Output off Current Low & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCH}} \\
    & \mathrm{~V}_{\mathrm{OZL}}=0.4 \mathrm{~V}
    \end{aligned}
    \] & & & -20 & \(\mu \mathrm{A}\) \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    at \(V_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (see Section 1 for Test Waveforms and output loading)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\[
    \begin{aligned}
    & R_{L}=2 \mathrm{k} \Omega, \\
    & \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}
    \end{aligned}
    \]} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay Data to Q & & \[
    \begin{aligned}
    & 27 \\
    & 18 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay LE to Q & & \[
    \begin{aligned}
    & 36 \\
    & 25 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PZH}} \\
    & \mathrm{t}_{\mathrm{PZL}} \\
    & \hline
    \end{aligned}
    \] & TRI-STATE Enable Time \(\overline{\mathrm{OE}}\) to Q & & \[
    \begin{aligned}
    & 20 \\
    & 25 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PHZ}} \\
    & \mathrm{t}_{\mathrm{PLZ}} \\
    & \hline
    \end{aligned}
    \] & TRI-STATE Enable Time \(\overline{\mathrm{OE}}\) to Q & & \[
    \begin{aligned}
    & 20 \\
    & 25
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & \begin{tabular}{l}
    Setup Time (High/Low) \\
    Data to LE
    \end{tabular} & \[
    \begin{aligned}
    & 3 \\
    & 7
    \end{aligned}
    \] & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L) \\
    & \hline
    \end{aligned}
    \] & Hold Time (High/Low) Data to LE & \[
    \begin{aligned}
    & 3 \\
    & 7
    \end{aligned}
    \] & & ns \\
    \hline \(t_{w}(\mathrm{H})\) & Pulse Width (High) Data to LE & 15 & & ns \\
    \hline
    \end{tabular}

    \section*{DM74LS574}

    \section*{Octal D-Type Flip-Flop (with TRI-STATE \({ }^{\circledR}\) Outputs)}

    \section*{General Description}

    The 'LS574 is a high speed low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ( \(\overline{\mathrm{OE}}\) ). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

    This device is functionally identical to the 'LS374 except for the pinouts.

    \section*{Connection Diagram}

    \section*{Dual-In-Line Package}
    

    TL/F/9815-1
    Order Number DM74LS574WM or DM74LS574N
    See NS Package Number M20B or N20A

    \section*{Logic Symbol}
    

    TL/F/9815-2
    \(V_{C C}=\operatorname{Pin} 20\)
    GND \(=\operatorname{Pin} 10\)
    \begin{tabular}{|c|c|}
    \hline \multicolumn{2}{|l|}{Absolute Maximum Ratings (Note)} \\
    \hline If Military/Aerospace specified dev please contact the National Sem Office/Distributors for availability and & ices are required, iconductor Sales d specifications. \\
    \hline Supply Voltage & 7 V \\
    \hline Input Voltage & 7V \\
    \hline Operating Free Air Temperature Range DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    \hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    Recommended Operating Conditions \(\mathrm{v}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\)
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM74LS574} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{C C}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -2.6 & mA \\
    \hline lOL & Low Level Output Current & & & 24 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW Dn to CP & \[
    \begin{array}{r}
    20 \\
    20 \\
    \hline
    \end{array}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L) \\
    & \hline
    \end{aligned}
    \] & Hold Time HIGH or LOW Dn to CP & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{w}(H) \\
    & t_{w}(L)
    \end{aligned}
    \] & CP Pulse Width HIGH or LOW & \[
    \begin{aligned}
    & 15 \\
    & 15
    \end{aligned}
    \] & & & ns \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \(V_{C C}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\) & & & -1.5 & V \\
    \hline VOH & High Level Output Voltage & \[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \] & 2.4 & 3.3 & & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\text {OL }}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \[
    \begin{aligned}
    & V_{\mathrm{CC}}=M i n, \mathrm{I}_{\mathrm{OL}}=M a x, \\
    & \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \] & & 0.35 & 0.5 & \multirow[t]{2}{*}{V} \\
    \hline & & \(\mathrm{IOL}=12 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=7 \mathrm{~V}\) & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\) & & & 20 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \(\mathrm{V}_{\text {CC }}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\) & & & -20 & \(\mu \mathrm{A}\) \\
    \hline lozh & Off-State Output Current with High Level Output Voltage Applied & \[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=2.4 V \\
    & V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
    \end{aligned}
    \] & & & 20 & \(\mu \mathrm{A}\) \\
    \hline lozl & Off-State Output Current with Low Level Output Voltage Applied & \[
    \begin{aligned}
    & V_{C C}=M a x, V_{O}=0.4 V \\
    & V_{I H}=M i n, V_{I L}=M a x
    \end{aligned}
    \] & & & -20 & \(\mu \mathrm{A}\) \\
    \hline
    \end{tabular}

    \section*{Electrical Characteristics}
    over recommended operating free air temperature range (unless otherwise noted) (Continued)
    \begin{tabular}{l|l|l|c|c|c|c}
    \hline Symbol & \multicolumn{1}{|c|}{ Parameter } & Conditions & Min & \begin{tabular}{c} 
    Typ \\
    (Note 1)
    \end{tabular} & Max & Units \\
    \hline IOS & \begin{tabular}{l} 
    Short Circuit (Note 2) \\
    Output Current
    \end{tabular} & \(\mathrm{V}_{\mathrm{CC}}=\operatorname{Max}\) & -20 & & -100 & mA \\
    \hline ICC & Supply Current & \(\mathrm{V}_{\mathrm{CC}}=\operatorname{Max}\) (Note 3) & & & 45 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: \(I_{C C}\) is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5 V .
    Note 4: Both \(\bar{G}\) inputs are at 2 V
    Note 5: Both \(\overline{\mathrm{G}}\) inputs at 0.4 V

    \section*{Switching Characteristics}
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for test waveforms and output load)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\[
    \begin{aligned}
    & \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \\
    & \mathrm{C}_{\mathrm{L}}=45 \mathrm{pF}
    \end{aligned}
    \]} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \(f_{\text {max }}\) & Maximum Clock Frequency & 35 & & MHz \\
    \hline \[
    t_{\text {PLH }}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & Propagation Delay CP to On & & \[
    \begin{aligned}
    & 28 \\
    & 28 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PZH}} \\
    & \mathrm{t}_{\mathrm{P} Z \mathrm{~L}} \\
    & \hline
    \end{aligned}
    \] & Output Enable Time & & \[
    \begin{aligned}
    & 28 \\
    & 28 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\text {PHZ }} \\
    & \mathrm{t}_{\mathrm{PLLZ}} \\
    & \hline
    \end{aligned}
    \] & Output Disable Time & & \[
    \begin{array}{r}
    20 \\
    25 \\
    \hline
    \end{array}
    \] & ns \\
    \hline
    \end{tabular}

    \section*{Functional Description}

    The LS574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Outputs Enable are common to all flip-flops. The eight flip-flops will store the state of their individual \(D\) inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (OE) LOW, the contents of the eight flipflops are available at the outputs. When the \(\overline{\mathrm{OE}}\) is HIGH, the outputs go to the high impedence state. Operation of the \(\overline{\mathrm{OE}}\) input does not affect the state of the flip-flops.

    Truth Table
    \begin{tabular}{|c|c|c|c|}
    \hline \multicolumn{2}{|c|}{ Inputs } & \multicolumn{2}{c|}{ Outputs } \\
    \hline \multicolumn{2}{|c|}{ Dn } & CP & OE \\
    \hline H & \(\Gamma\) & L & H \\
    L & \(\Gamma\) & L & L \\
    X & X & H & Z \\
    \hline
    \end{tabular}
    \(H=H I G H\) Voltage Level
    L = LOW Voltage Level
    \(X=\) Immaterial
    \(\mathbf{Z}=\) High Impedance

    \section*{Logic Diagram}
    

    TL/F/9815-3

    \section*{DM74LS645 Octal Bus Transceivers}

    \section*{General Description}

    These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the \(A\) bus to the \(B\) bus or from the \(B\) bus to the \(A\) bus depending upon the level at the direction control (DIR) input. The enable input ( \(\overline{\mathrm{G}}\) ) can be used to disable the device so that the buses are effectively isolated.

    \section*{Features}
    - Bi-directional bus transceivers in high-density 20 -pin packages
    - Hysteresis at bus inputs improves noise margins
    - TRI-STATE® outputs

    \section*{Connection Diagram}

    \section*{Dual-In-Line Package}
    

    Function Table
    \begin{tabular}{|c|c|c|}
    \hline \multicolumn{2}{|c|}{\begin{tabular}{c} 
    Control \\
    Inputs
    \end{tabular}} & \multirow{2}{*}{ 'LS645 } \\
    \cline { 1 - 2 }\(\overline{\mathbf{G}}\) & DIR & \\
    \hline L & L & B data to A bus \\
    L & H & A data to \(B\) bus \\
    H & X & Isolation \\
    \hline
    \end{tabular}

    \footnotetext{
    H = High Level
    \(\mathrm{L}=\) Low Leve
    X = Irrelevant
    }
    ```

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for availability and specifications.

    ```

    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    DM74LS
    Storage Temperature Range
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \(-55^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{c|c|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multicolumn{2}{|c|}{ Parameter } & \multicolumn{2}{|c|}{ DM74LS645 } & \multirow{2}{*}{ Units } \\
    \cline { 3 - 4 } & & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage (Note 1) & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.6 & V \\
    \hline \(\mathrm{IOH}_{\mathrm{OH}}\) & High Level Output Current & & & -15 & mA \\
    \hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 24 & mA \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & \begin{tabular}{l} 
    Free Air Operating \\
    Temperature
    \end{tabular} & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{3}{|c|}{\[
    \begin{aligned}
    & \text { Conditions } \\
    & \text { (Note 2) } \\
    & \hline
    \end{aligned}
    \]} & Min & Typ
    (Note 3) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \(\mathrm{H}_{Y S}\) & Hysteresis ( \(\mathrm{V}_{\mathrm{T}+}-\mathrm{V}_{-}\)) A or B Input & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}\)} & 0.2 & 0.4 & & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M i n, V_{I H}=2 V \\
    & V_{I L}=M a x
    \end{aligned}
    \]}} & \(\mathrm{IOH}=-3 \mathrm{~mA}\) & 2.4 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & & \(\mathrm{l}_{\mathrm{OH}}=\mathrm{Max}\) & 2 & & & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\text {OL }}\)} & \multirow[t]{2}{*}{Low Level Output Voitage} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, V_{\mathbb{I H}}=2 V \\
    & V_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]}} & \(\mathrm{l}_{\mathrm{OL}}=12 \mathrm{~mA}\) & & 0.25 & 0.4 & \multirow[t]{2}{*}{V} \\
    \hline & & & & \(\mathrm{I}_{\mathrm{OL}}=24 \mathrm{~mA}\) & & 0.35 & 0.5 & \\
    \hline lozH & Off-State Output Current, High Level Voltage Applied & \multicolumn{3}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M a x, G \text { at } 2 V, \\
    & V_{O}=2.7 V
    \end{aligned}
    \]} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline lozl & Off-State Output Current, Low Level Voltage Applied & \multicolumn{3}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M a x, G \text { at } 2 V \\
    & V_{O}=0.4 V
    \end{aligned}
    \]} & & & -400 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{1} & \multirow[t]{2}{*}{Input Current at Maximum Input Voltage} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & A or B & \(\mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 0.1 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DIR or G & \(\mathrm{V}_{1}=7 \mathrm{~V}\) & & & 0.1 & \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}, \mathrm{V}_{\text {IH }}=2.7\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline \(\mathrm{I}_{\text {IL }}\) & Low Level Input Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{IL}}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline los & Short Circuit Output Current (Note 4) & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & -40 & & -225 & mA \\
    \hline \multirow[t]{3}{*}{\(\mathrm{I}_{\mathrm{CC}}\)} & \multirow[t]{3}{*}{Total Supply Current} & \multicolumn{2}{|l|}{Outputs High} & \multirow[t]{3}{*}{\begin{tabular}{l}
    \[
    V_{C C}=M a x
    \] \\
    Outputs Open
    \end{tabular}} & & 48 & 70 & \\
    \hline & & \multicolumn{2}{|l|}{Outputs Low} & & & 62 & 90 & mA \\
    \hline & & \multicolumn{2}{|l|}{Outputs at \(\mathrm{Hi}-\mathrm{Z}\)} & & & 64 & 95 & \\
    \hline
    \end{tabular}

    Note 1: Voltage values are with respect to the network ground terminal.
    Note 2: For conditions shown as Min or Max, use the appropriate value specified under Recommended Operating Conditions.
    Note 3: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(R_{L}=667 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=45 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \(A\) to \(B\) & & 15 & & & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \(A\) to \(B\) & & 15 & & & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \(B\) to \(A\) & & 15 & & & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \(B\) to \(A\) & & 15 & & & ns \\
    \hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level & \[
    \begin{gathered}
    \overline{\mathrm{G}} \\
    \text { to } \mathrm{A}
    \end{gathered}
    \] & & 40 & & & ns \\
    \hline \(t_{\text {PZH }}\) & Output Enable Time to High Level & \[
    \begin{gathered}
    \overline{\mathrm{G}} \\
    \text { to } \mathrm{A}
    \end{gathered}
    \] & & 40 & & & ns \\
    \hline \(\mathrm{t}_{\text {PZL }}\) & Output Enable Time to Low Level & \[
    \begin{gathered}
    \overline{\mathrm{G}} \\
    \text { to } \mathrm{B}
    \end{gathered}
    \] & & 40 & & & ns \\
    \hline \(t_{\text {PZH }}\) & Output Enable Time to High Level & \[
    \begin{gathered}
    \overline{\mathrm{G}} \\
    \text { to } \mathrm{B}
    \end{gathered}
    \] & & 40 & & & ns \\
    \hline tplz & Output Disable Time to Low Level & \[
    \begin{gathered}
    \overline{\mathrm{G}} \\
    \text { to } \mathrm{A}
    \end{gathered}
    \] & & & & 25 & ns \\
    \hline tphz \(^{\text {P }}\) & Output Disable Time to High Level & \[
    \begin{gathered}
    \overline{\mathrm{G}} \\
    \text { to } \mathrm{A}
    \end{gathered}
    \] & & & & 25 & ns \\
    \hline \(t_{\text {PLZ }}\) & Output Disable Time to Low Level & \[
    \begin{gathered}
    \overline{\mathrm{G}} \\
    \text { to } \mathrm{B}
    \end{gathered}
    \] & & & & 25 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time to High Level & \[
    \begin{gathered}
    \overline{\mathrm{G}} \\
    \text { to } \mathrm{B}
    \end{gathered}
    \] & & & & 25 & ns \\
    \hline
    \end{tabular}

    \section*{54LS670/DM54LS670/DM74LS670 TRI-STATE \({ }^{\text {® }} 4\)-by-4 Register Files}

    \section*{General Description}

    These register files are organized as 4 words of 4 bits each, and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits writing into one location, and reading from another word location, simultaneously.
    Four data inputs are available to supply the word to be stored. Location of the word is determined by the write select inputs \(A\) and \(B\), in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the \(D\) input is transferred to the latch output. When the write-enable input, GW, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, \(\mathrm{G}_{\mathrm{R}}\), is high, the data outputs are inhibited and go into the high impedance state.
    The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.
    This arrangement-data entry addressing separate from data read addressing and individual sense line - eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time ( 27 ns typical)
    and the read time (24 ns typical). The register file has a nonvolatile readout in that data is not lost when addressed.
    All inputs (except read enable and write enable) are buffered to lower the drive requirements to one normal Series 54LS/74LS load, and input clamping diodes minimize switching transients to simplify system design. High speed, double ended AND-OR-INVERT gates are employed for the read-address function and have high sink current, TRISTATE outputs. Up to 128 of these outputs may be wireAND connected for increasing the capacity up to 512 words. Any number of these registers may be paralleled to provide \(n\)-bit word length.

    \section*{Features}
    - Alternate Military/Aerospace device (54LS670) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.
    - For use as:

    \section*{Scratch pad memory}

    Buffer storage between processors Bit storage in fast multiplication designs
    - Separate read/write addressing permits simultaneous reading and writing
    - Organized as 4 words of 4 bits
    - Expandable to 512 words of n-bits
    - TRI-STATE versions of DM54LS170/DM74LS170
    - Fast access times 20 ns typ

    \section*{Connection Diagram}
    

    TL/F/6436-1
    Order Number 54LS670DMQB, 54LS670FMQB, 54LS670LMQB, DM54LS670J, DM54LS670W, DM74LS670M or DM74LS670N See NS Package Number E20A, J16A, M16A, N16A or W16A

    \section*{Function Tables}

    WRITE TABLE (SEE NOTES A, B, AND C)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multicolumn{3}{|r|}{Write Inputs} & \multicolumn{4}{|c|}{Word} \\
    \hline \(\mathrm{W}_{\mathrm{B}}\) & \(\mathrm{W}_{\text {A }}\) & Gw & 0 & 1 & 2 & 3 \\
    \hline L & L & L & \(Q=D\) & \(Q_{0}\) & \(Q_{0}\) & \(Q_{0}\) \\
    \hline L & H & L & \(Q_{0}\) & \(Q=D\) & \(Q_{0}\) & \(Q_{0}\) \\
    \hline H & L & L & \(Q_{0}\) & \(Q_{0}\) & \(Q=D\) & \(Q_{0}\) \\
    \hline H & H & L & \(Q_{0}\) & \(Q_{0}\) & \(\mathrm{Q}_{0}\) & \(Q=D\) \\
    \hline X & X & H & \(Q_{0}\) & \(Q_{0}\) & \(Q_{0}\) & \(Q_{0}\) \\
    \hline
    \end{tabular}

    READ TABLE (SEE NOTES A AND D)
    \begin{tabular}{|ccc|cccc|}
    \hline \multicolumn{3}{|c|}{ Read Inputs } & \multicolumn{4}{c|}{ Outputs } \\
    \hline \(\mathbf{R}_{\mathbf{B}}\) & \(\mathbf{R}_{\mathbf{A}}\) & \(\mathbf{G}_{\mathbf{R}}\) & \(\mathbf{Q 1}\) & Q2 & Q3 & Q4 \\
    \hline L & L & L & WOB1 & WOB2 & WOB3 & WOB4 \\
    L & H & L & W1B1 & W1B2 & W1B3 & W1B4 \\
    H & L & L & W2B1 & W2B2 & W2B3 & W2B4 \\
    H & H & L & W3B1 & W3B2 & W3B3 & W3B4 \\
    X & X & H & Z & Z & Z & Z \\
    \hline
    \end{tabular}

    Note A: \(H=\) High Level, \(L=\) Low Level, \(X=\) Don't Care, \(Z=\) High Impedance (Off).
    Note B: \((Q=D)=\) The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
    Note C: \(Q_{0}=\) The level of \(Q\) before the indicated input conditions were established.
    Note D: WOB1 \(=\) The first bit of word 0 , etc.

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avallability and specifications.
    Supply Voltage
    Input Voltage
    7V
    Operating Free Air Temperature Range

    DM54LS and 54LS
    DM74LS
    Storage Temperature Range
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54LS670} & \multicolumn{3}{|c|}{DM74LS670} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\text {CC }}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.7 & & & 0.8 & V \\
    \hline \({ }^{\mathrm{OH}}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -1 & & & -2.6 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 12 & & & 24 & mA \\
    \hline \(t_{W}\) & \multicolumn{2}{|l|}{Write Enable Pulse Width (Note 3)} & 25 & & & 25 & & & ns \\
    \hline \multirow[t]{2}{*}{tsu} & \multirow[t]{2}{*}{\begin{tabular}{l}
    Setup Time \\
    (Notes 1 \& 3)
    \end{tabular}} & Data & 10 & & & 10 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & \(W_{A}, W_{B}\) & 15 & & & 15 & & & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{t}_{\mathrm{H}}\)} & \multirow[t]{2}{*}{Hold Time (Notes \(1 \& 3\) )} & Data & 15 & & & 15 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & \(W_{A}, W_{B}\) & 5 & & & 5 & & & \\
    \hline t LATCH & \multicolumn{2}{|l|}{Latch Time for New Data (Notes 2 \& 3)} & 25 & & & 25 & & & ns \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{\begin{tabular}{l}
    Free Air Operating \\
    Temperature
    \end{tabular}} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note 1: Times are with respect to the Write-Enable input. Write-Select time will protect the data written into the previous address. If protection of data in the previous address, \(t_{\text {SETUP }}\left(W_{A}, W_{B}\right)\) can be ignored. As any address selection sustained for the final 30 ns of the Write-Enable pulse and during \(t_{H}\left(W_{A}, W_{B}\right)\) will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.
    Note 2: Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data.
    Note 3: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{C C}=5 \mathrm{~V}\).
    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 2.4 & 3.4 & & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & DM54 & & 0.25 & 0.4 & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & & 0.34 & 0.5 & \\
    \hline \multirow[t]{3}{*}{1} & \multirow[t]{3}{*}{Input Current @ Max Input Voltage} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=7 V
    \end{aligned}
    \]} & D, R or W & & & 0.1 & \multirow{3}{*}{mA} \\
    \hline & & & \(\mathrm{G}_{\mathrm{w}}\) & & & 0.2 & \\
    \hline & & & \(\mathrm{G}_{\mathrm{R}}\) & & & 0.3 & \\
    \hline \multirow[t]{3}{*}{\({ }_{1 / H}\)} & \multirow[t]{3}{*}{High Level Input Current} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=2.7 V
    \end{aligned}
    \]} & D, R or W & & & 20 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & \(\mathrm{G}_{\mathrm{w}}\) & & & 40 & \\
    \hline & & & \(\mathrm{G}_{\mathrm{R}}\) & & & 60 & \\
    \hline
    \end{tabular}

    Electrical Characteristics
    over recommended operating free air temperature (unless otherwise noted) (Continued)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
    (Note 1) & Max & Units \\
    \hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=0.4 V
    \end{aligned}
    \]} & D, R, or W & & & -0.4 & \multirow{3}{*}{mA} \\
    \hline & & & \(\mathrm{G}_{\mathrm{w}}\) & & & -0.8 & \\
    \hline & & & \(\mathrm{G}_{\mathrm{R}}\) & & & -1.2 & \\
    \hline lozH & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=2.7 V \\
    & V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
    \end{aligned}
    \]} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline IozL & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & -20 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Max} \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 3)} & & 30 & 50 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[b]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=667 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=45 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=150 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    \text { Read Select } \\
    \text { to } \mathrm{Q} \\
    \hline
    \end{gathered}
    \] & & 40 & & 50 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \text { Read Select } \\
    \text { to } Q
    \end{gathered}
    \] & & 45 & & 55 & ns \\
    \hline tply & Propagation Delay Time Low to High Level Output & \[
    \begin{aligned}
    & \text { Write Enable } \\
    & \text { to Q }
    \end{aligned}
    \] & & 45 & & 55 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Write Enable to \(Q\) & & 50 & & 60 & ns \\
    \hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & \begin{tabular}{l}
    Data \\
    to Q
    \end{tabular} & & 45 & & 55 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to Q & & 40 & & 50 & ns \\
    \hline \(t_{\text {PZH }}\) & Output Enable Time to High Level Output & Read Enable to Any Q & & 35 & & 45 & ns \\
    \hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level Output & Read Enable to Any Q & & 40 & & 50 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time from High Level Output (Note 4) & Read Enable to Any Q & & 50 & & & ns \\
    \hline tpLZ & Output Disable Time from Low Level Output (Note 4) & Read Enable to Any Q & & 35 & & & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: ICC is measured with 4.5 V applied to all DATA inputs and both ENABLE inputs, all ADDRESS inputs are grounded and all outputs are open.
    Note 4: \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\).
    

    TL/F/6436-2

    \section*{DM74LS952 \\ Dual Rank 8-Bit TRI-STATE \({ }^{\circledR}\) Shift Registers}

    \section*{General Description}

    These circuits are TRI-STATE, edge-triggered, 8 -bit I/O registers in parallel with 8 -bit serial shift registers which are capable of operating in any of the following modes: parallel load from I/O pins to register " \(A\) ", parallel transfer down from register " \(A\) " to serial shift register " \(B\) ", parallel transfer up from shift register " \(B\) " to register " \(A\) ", serial shift of register " \(B\) ", synchronously clear. Since the registers are edgetriggered by the positive transition of the clock, the control lines which determine the mode or operation are completely independent of the logic level applied to the clock. Designed for bus-oriented systems, these circuits have their TRI-STATE inputs and outputs on the same pins.

    \section*{Features}
    - Registers are edge-triggered by the positive transition of the clock
    - All inputs are PNP transistors
    - Input disable dominates over output disable
    - Output high impedance state does not impede any other mode of operation
    - 8-bit I/O pins are TRI-STATE buffers
    - Typical shift frequency is 36 MHz
    - Typical power dissipation is 305 mW
    - All control inputs are active when in an " \(L\) " logic state
    - Devices can be cascaded into N -bit word

    \section*{Connection Diagram}

    Dual-In-Line Package
    

    TL/F/6437-1

    Pin Description
    DIS \({ }_{\mathrm{O}}\)-Output disable
    IS-Serial input
    DIS \({ }_{\text {--Input disable }}\)
    DIS TU-Transfer up disable \(^{\text {un }}\)
    DIS TD-Transfer down disable
    DIS \({ }_{\mathrm{S}}\)-Shift disable
    \(\mathrm{O}_{\mathrm{S}}\)-Serial output
    CLK-Clock
    GND-Ground
    I/O 1 . . . I/O 8-8-bit I/O pins
    \(V_{C C}\)-Supply Voltage
    \begin{tabular}{|c|c|}
    \hline \multicolumn{2}{|l|}{Absolute Maximum Ratings (Note)} \\
    \hline \multicolumn{2}{|l|}{If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.} \\
    \hline Supply Voltage & \\
    \hline Input Voltage & \\
    \hline Operating Free Air Temperature Range DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    \hline Storage Temperature Range - & \(-65^{\circ} \mathrm{C}\) to +150 \\
    \hline ead Temperature (Soldering, 10 seconds) & \\
    \hline
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM74LS952} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Typ & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{1 \mathrm{H}}\) & High-Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low-Level Input Voltage & & & 0.8 & V \\
    \hline IOH & High-Level Output Current & & & -5.2 & mA \\
    \hline lOL & Low-Level Output Current & & & 16 & mA \\
    \hline \(\mathrm{f}_{\text {CLOCK }}\) & Clock Frequency (Note 5) & 0 & & 25 & MHz \\
    \hline \multirow[t]{2}{*}{Clock Pulse} & High Pulse Width (Note 5) & 25 & 17 & & ns \\
    \hline & Low Pulse Width (Note 5) & 15 & 7 & & ns \\
    \hline \(\mathrm{t}_{\text {SET-UP }}\) & Data Set-Up Time (Note 5) & 10 & & & ns \\
    \hline \(\mathrm{thOLD}^{\text {d }}\) & Data Hold Time (Note 5) & 0 & & & ns \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Conditions (1)}} & \multicolumn{3}{|c|}{DM74LS952} & \multirow[t]{2}{*}{Units} \\
    \hline & & & & Min & Typ (2) & Max & \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High-Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}, \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{V}_{\mathrm{IL}} \mathrm{Max}
    \end{aligned}
    \] & \(\mathrm{l}_{\mathrm{OH}}=-5.2 \mathrm{~mA}\) & 2.4 & & & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\text {OL }}\)} & \multirow[t]{2}{*}{Low-Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IH}}=2 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{V}_{\mathrm{IL}} \operatorname{Max}
    \end{aligned}
    \]} & \(\mathrm{I}_{\mathrm{OL}}=8 \mathrm{~mA}\) & & 0.25 & 0.4 & \multirow[t]{2}{*}{V} \\
    \hline & & & \(\mathrm{lOL}=16 \mathrm{~mA}\) & & 0.35 & 0.5 & \\
    \hline 1 & Input Current at Maximum Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{I}_{1}\) & High-Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\) Max, \(V_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low-Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -50 & \(\mu \mathrm{A}\) \\
    \hline los & Short-Circuit Output Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}(3)\)} & -20 & & -100 & mA \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max~(4)~}\)} & & 61 & 99 & mA \\
    \hline \multirow[t]{2}{*}{IOFF} & \multirow[t]{2}{*}{TRI-STATE I/O Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{IH}}=2 \mathrm{~V}\)} & \(\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}\) & & & 20 & \(\mu \mathrm{A}\) \\
    \hline & & & \(\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}\) & & & -20 & \(\mu \mathrm{A}\) \\
    \hline
    \end{tabular}

    Note 1: For conditions shown as min or max, use the appropriate value specified under recommended operating conditions.
    Note 2: All typical values are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 3: Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
    Note 4: \(\mathrm{I}_{\mathrm{CC}}\) is measured with serial output open, the clock and shift disable input at 2.4 V . All other control inputs and I/O pins grounded.
    Note 5: \(T_{A}=25^{\circ} \mathrm{C}\) and \(V_{C C}=5 \mathrm{~V}\).

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}^{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & Max & Units \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & \multirow{7}{*}{\(C_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega\)} & 25 & & MHz \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time, Low-to-High-Level from Clock to Any Outputs & & 7 & 33 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time, High-to-Low Level from Clock to Any Output & & 10 & 48 & ns \\
    \hline \(t_{\text {ENABLE }}\) & Enable Time from Any Control Inputs & & 5 & 24 & ns \\
    \hline \(t_{\text {DISABLE }}\) & Disable Time from Any Control Inputs & & 6 & 27 & ns \\
    \hline \({ }_{\text {tPZH }}\) & Output Enable Time to High Level & & 5 & 23 & ns \\
    \hline \(\mathrm{t}_{\text {PZL }}\) & Output Enable to Low Level & & 4 & 18 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time from High Level & \multirow[t]{2}{*}{\(C_{L}=5 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega\)} & 5 & 23 & ns \\
    \hline \(t_{\text {PLZ }}\) & Output Disable Time from Low Level & & 6 & 27 & ns \\
    \hline
    \end{tabular}

    \section*{Logic Diagram}
    

    \section*{Function Table}

    Table I
    

    X \(\equiv\) Don't Care
    \(\mathrm{Hi}-\mathrm{Z} /\) Output/Input/ \(\equiv\) High impedance state/output state/input state
    \(\mathrm{a} 1 . . \mathrm{a} / \mathrm{b} 1 \ldots \mathrm{~b} 8 \equiv\) The content of the upper register " A "/the lower serial shift register " B " before the most recent \(\uparrow\) transition of the clock
    \(I_{1} \ldots I_{8} \equiv\) The level of steady state inputs of the I/O pins
    \(D O R \equiv\) "Data ORing function" ORing data from both \(I / O\) pins and register " \(B\) ", i.e., \(l_{1}+b 1, l_{2}+b 2, l_{3}+b 3 \ldots l_{8}+b 8\)
    \(d \equiv\) Data of the serial input

    Timing Diagram
    

    TL/F/6437-3

    AC Test Circuit and Switching Time Waveforms
    

    All diodes are 1N916 or 1N3064. \(\mathrm{C}_{\mathrm{L}}\) includes probe and jig capacitance.

    TL/F/6437-4
    

    TL/F/6437-5
    All input pulses are supplied by generators having \(\mathrm{t}_{\mathrm{f}} \leq 15 \mathrm{~ns}, \mathrm{t}_{\mathrm{f}} \leq 6 \mathrm{~ns}, \mathrm{PRR} \leq 1 \mathrm{MHz}, \mathrm{Z}_{\mathrm{OUT}} \approx 50 \Omega\).

    \section*{Cascading Packages}
    

    \section*{DM74LS962}

    Dual Rank 8-Bit TRI-STATE \({ }^{\circledR}\) Shift Registers

    \section*{General Description}

    These circuits are TRI-STATE, edge-triggered, 8-bit I/O registers in parallel with 8 -bit serial shift registers which are capable of operating in any of the following modes: parallel load from I/O pins to register " \(A\) ", parallel transfer down from register " \(A\) " to serial shift register " \(B\) ", parallel transfer up from shift register " \(B\) " to register " \(A\) ", serial shift of register " \(B\) ", or exchange data between register " \(A\) " and shift register " B ". Since the registers are edge-triggered by the positive transition of the clock, the control lines which determine the mode or operation are completely independent of the logic level applied to the clock. Designed for bus-oriented systems, these circuits have their TRI-STATE inputs and outputs on the same pins.

    \section*{Features}
    - Registers are edge-triggered by the positive transition of the clock
    - All inputs are PNP transistors
    - Input disable dominates over output disable
    - Output high impedance state does not impede any other mode of operation
    - 8-bit I/O pins are TRI-STATE buffers
    - Typical shift frequency is 36 MHz
    - Typical power dissipation is 305 mW
    - All control inputs are active when in an "L" logic state
    - Devices can be cascaded into N -bit word

    \section*{Connection Diagram}

    Pin Description
    DIS \({ }_{\mathrm{O}}\)-Output disable
    Is-Serial input
    DIS
    DISTU-Transfer up disable
    DIS TD-Transfer down disable
    DIS \(S_{S}\)-Shift disable
    \(\mathrm{O}_{\mathrm{S}}-\) Serial output
    CLK-Clock
    GND-Ground
    1/O 1 . . . I/O 8-8-bit I/O pins
    \(\mathrm{V}_{\mathrm{CC}}-\) Supply Voltage
    ```

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    DM74LS
    Storage Temperature Range $\quad-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
    Lead Temperature (Soldering, 10 seconds) $300^{\circ} \mathrm{C}$

    ```

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM74LS962} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Typ & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High-Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low-Level Input Voltage & & & 0.8 & V \\
    \hline IOH & High-Level Output Current & & & -5.2 & mA \\
    \hline lOL & Low-Level Output Current & & & 16 & mA \\
    \hline \(\mathrm{f}_{\mathrm{CLOCK}}\) & Clock Frequency (Note 5) & 0 & & 25 & MHz \\
    \hline \multirow[t]{2}{*}{Clock Pulse} & High Pulse Width (Note 5) & 25 & 17 & & ns \\
    \hline & Low Pulse Width (Note 5) & 15 & 7 & & ns \\
    \hline \(\mathrm{t}_{\text {SET-UP }}\) & Data Set-Up Time (Note 5) & 10 & & & ns \\
    \hline \(\mathrm{t}_{\mathrm{HOLD}}\) & Data Hold Time (Note 5) & 0 & & & ns \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions (1)} & Min & Typ (2) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{V OH} & \multirow[t]{2}{*}{High-Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, V_{I H}=2 V \\
    & V_{I L}=V_{I L} \operatorname{Max}
    \end{aligned}
    \]} & \(\mathrm{IOH}^{\prime}=-2.6 \mathrm{~mA}\) & & & & V \\
    \hline & & & \(\mathrm{IOH}^{\text {O }}=-5.2 \mathrm{~mA}\) & 2.4 & & & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\text {OL }}\)} & \multirow[t]{2}{*}{Low-Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IH}}=2 \mathrm{~V}, \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{V}_{\mathrm{IL}} \operatorname{Max}
    \end{aligned}
    \]} & \(\mathrm{l}_{\mathrm{OL}}=8 \mathrm{~mA}\) & & 0.25 & 0.4 & \multirow[t]{2}{*}{V} \\
    \hline & & & \(\mathrm{lOL}=16 \mathrm{~mA}\) & & 0.35 & 0.5 & \\
    \hline 1 & Input Current at Maximum Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High-Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline ILL & Low-Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -50 & \(\mu \mathrm{A}\) \\
    \hline los & Short-Circuit Output Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\operatorname{Max}(3)\)} & -20 & & -100 & mA \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}(4)\)} & & 61 & 99 & mA \\
    \hline \multirow[t]{2}{*}{loff} & \multirow[t]{2}{*}{TRI-STATE I/O Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{IH}}=2 \mathrm{~V}\)} & \(\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}\) & & & 20 & \(\mu \mathrm{A}\) \\
    \hline & & & \(\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}\) & & & -20 & \(\mu \mathrm{A}\) \\
    \hline
    \end{tabular}

    Note 1: For conditions shown as min or max, use the appropriate value specified under recommended operating conditions.
    Note 2: All typical values are at \(V_{C C}=5 \mathrm{~V}, T_{A}=25^{\circ} \mathrm{C}\).
    Note 3: Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
    Note 4: ICC is measured with serial output open, the clock and shift disable input at 2.4 V . All other control inputs and I/O pins grounded.
    Note 5: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multicolumn{6}{|l|}{Switching Characteristics \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)} \\
    \hline Symbol & Parameter & Condilions & Min & Max & Units \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & \multirow{7}{*}{\(C_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega\)} & 25 & & MHz \\
    \hline \(t_{\text {PLL }}\) & Propagation Delay Time, Low-to-High-Level from Clock to Any Outputs & & 7 & 33 & ns \\
    \hline \({ }_{\text {tpHL }}\) & Propagation Delay Time, High-to-Low Level from Clock to Any Outputs & & 10 & 48 & ns \\
    \hline tenable & Enable Time from Any Control Inputs & & 5 & 24 & ns \\
    \hline \(\mathrm{t}_{\text {DISABLE }}\) & Disable Time from Any Control Inputs & & 6 & 27 & ns \\
    \hline \(\mathrm{tzH}^{\text {H }}\) & Output Enable Time to High Level & & 5 & 23 & ns \\
    \hline \(\mathrm{t}_{\mathrm{ZL}}\) & Output Enable to Low Level & & 4 & 18 & ns \\
    \hline \(\mathrm{t}_{\mathrm{Hz}}\) & Output Disable Time from High Level & \multirow[t]{2}{*}{\(C_{L}=5 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega\)} & 5 & 23 & ns \\
    \hline tLz & Output Disable Time from Low Level & & 6 & 27 & ns \\
    \hline
    \end{tabular}

    \section*{Logic Diagram}
    

    Function Table
    Table I
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
    \hline & \multirow{2}{*}{DISo} & \multirow[t]{2}{*}{DIS,} & \multirow[t]{2}{*}{DIS \({ }_{\text {TU }}\)} & \multirow[t]{2}{*}{\(\mathrm{DIS}_{\text {TD }}\)} & \multirow[t]{2}{*}{DISs} & \multirow[t]{2}{*}{CLK} & \multirow[t]{2}{*}{Is} & \multirow[t]{2}{*}{8-Bit I/O Pins} & \multicolumn{8}{|c|}{Content of Upper Reg. "A"} & \multicolumn{8}{|l|}{Content of Lower Serial Shift Reg. "B"} & \multirow[t]{2}{*}{Os} & \multirow[t]{2}{*}{Comments} \\
    \hline & & & & & & & & & A1 & A2 & A3 & A4 & A5 & A6 & A7 & A8 & B1 & B2 & B3 & B4 & B5 & B6 & B7 & B8 & & \\
    \hline & H & H & H & H & H & X & x & Hi-Z & a1 & a2 & a3 & a4 & a5 & a6 & a7 & a8 & b1 & b2 & b3 & b4 & b5 & b6 & b7 & b8 & b8 & \multirow[t]{3}{*}{\begin{tabular}{l}
    Stable state \\
    Entering data from I/O to reg. " A "
    \end{tabular}} \\
    \hline & L & H & H & H & H & X & x & Output & a1 & a2 & a3 & a4 & a5 & a6 & a7 & a8 & b1 & b2 & b3 & b4 & b5 & b6 & b7 & b8 & b8 & \\
    \hline & X & L & H & H & H & \(\uparrow\) & x & Input & \(\mathrm{l}_{1}\) & \(\mathrm{I}_{2}\) & \(\mathrm{I}_{3}\) & \(\mathrm{I}_{4}\) & \(\mathrm{I}_{5}\) & \(\mathrm{I}_{6}\) & 17 & \(\mathrm{I}_{8}\) & b1 & b2 & b3 & b4 & b5 & b6 & b7 & b8 & b8 & \\
    \hline & H & H & L & H & H & \(\uparrow\) & x & Hi-Z & b1 & b2 & b3 & b4 & b5 & b6 & b7 & b8 & b1 & b2 & b3 & b4 & b5 & b6 & b7 & b8 & b8 & \multirow[b]{3}{*}{\begin{tabular}{l}
    Transfer data up from reg. " \(B\) " to reg. " \(A\) " \\
    Reg. " \(A\) " will OR data from \(1 / O\) to reg. " \(B\) "
    \end{tabular}} \\
    \hline & L & H & L & H & H & \(\uparrow\) & X & Output & b1 & b2 & b3 & b4 & b5 & b6 & b7 & b8 & b1 & b2 & b3 & b4 & b5 & b6 & b7 & b8 & b8 & \\
    \hline & X & L & L & H & H & \(\uparrow\) & X & Input & & & \(\leftarrow\) & DO & R & \(\rightarrow\) & \(\rightarrow\) & & b1 & b2 & b3 & b4 & b5 & b6 & b7 & b8 & b8 & \\
    \hline & H & H & H & L & X & \(\uparrow\) & x & Hi-Z & a1 & a2 & a3 & a4 & a5 & a6 & a7 & a8 & a1 & a2 & a3 & a4 & a5 & a6 & a7 & a8 & a8 & \multirow[b]{3}{*}{\begin{tabular}{l}
    Transfer data down from reg. " \(A\) " to reg. " \(B\) " \\
    Entering data and transfer down
    \end{tabular}} \\
    \hline & L & H & H & L & X & \(\uparrow\) & x & Output & a1 & a2 & a3 & a4 & a5 & a6 & a7 & a8 & a1 & a2 & a3 & a4 & a5 & a6 & a7 & a8 & a8 & \\
    \hline & X & L & H & L & x & \(\uparrow\) & x & Input & \(\mathrm{l}_{1}\) & \(\mathrm{I}_{2}\) & \(\mathrm{I}_{3}\) & \(\mathrm{I}_{4}\) & \(\mathrm{I}_{5}\) & \(\mathrm{I}_{6}\) & 17 & \(\mathrm{I}_{8}\) & a1 & a2 & a3 & a4 & a5 & a6 & a7 & a8 & a8 & \\
    \hline & H & H & L & L & x & \(\uparrow\) & x & Hi-Z & b1 & b2 & b3 & b4 & b5 & b6 & b7 & b8 & a1 & a2 & a3 & a4 & a5 & a6 & a7 & a8 & a8 & (1) Exchange data between registers \\
    \hline & L & H & L & L & x & \(\uparrow\) & X & Output & b1 & b2 & b3 & b4 & b5 & b6 & b7 & b8 & 21 & a2 & a3 & a4 & a5 & a6 & a7 & a8 & 28 & (2) Beside data exchanging, reg. " A " \\
    \hline & X & L & L & L & X & \(\uparrow\) & X & Input & & & \(\leftarrow\) & - DO & R \(\rightarrow\) & \(\rightarrow\) & \(\rightarrow\) & & a1 & a2 & a3 & a4 & a5 & a6 & a7 & a8 & a8 & (3) will "OR" data from I/O and reg. "B" \\
    \hline & H & H & H & H & L & \(\uparrow\) & d & Hi-Z & a1 & a2 & a3 & a4 & a5 & a6 & a7 & a8 & d & b1 & b2 & b3 & b4 & b5 & b6 & b7 & b7 & \multirow[t]{3}{*}{\begin{tabular}{l}
    Serial shifting in the lower reg. " B " \\
    Entering data and serial shifting
    \end{tabular}} \\
    \hline & L & H & H & H & L & \(\uparrow\) & d & Output & a1 & a2 & a3 & a4 & a5 & a6 & a7 & a8 & d & b1 & b2 & b3 & b4 & b5 & b6 & b7 & b7 & \\
    \hline & X & L & H & H & L & \(\uparrow\) & d & Input & \(\mathrm{I}_{1}\) & \(\mathrm{I}_{2}\) & \(\mathrm{I}_{3}\) & \(\mathrm{I}_{4}\) & \(\mathrm{I}_{5}\) & \(\mathrm{I}_{6}\) & 17 & \(\mathrm{I}_{8}\) & d & b1 & b2 & b3 & b4 & b5 & b6 & b7 & b7 & \\
    \hline & H & H & L & H & L & \(\uparrow\) & d & Hi-Z & b1 & b2 & b3 & b4 & b5 & b6 & b7 & b8 & d & b1 & b2 & b3 & b4 & b5 & b6 & b7 & b7 & \multirow[b]{3}{*}{Transfer up and serial shifting DOR function and serial shifting} \\
    \hline & L & H & L & H & L & \(\uparrow\) & d & Output & b1 & b2 & b3 & b4 & b5 & b6 & b7 & b8 & d & b1 & b2 & b3 & b4 & b5 & b6 & b7 & b7 & \\
    \hline & x & L & L & H & L & \(\uparrow\) & d & Input & \multicolumn{8}{|c|}{\(\leftarrow \leftarrow \leftarrow\) DOR \(\rightarrow \rightarrow \rightarrow\)} & d & b1 & b2 & b3 & b4 & b5 & b6 & b7 & b7 & \\
    \hline
    \end{tabular}

    X \(\equiv\) Don't Care
    Hi-Z/Output/Input/ 三 High impedance state/output state/input state
    \(\mathrm{a} 1 \ldots \mathrm{a} / \mathrm{b} 1 \ldots \mathrm{~b} \equiv \equiv\) The content of the upper register " A "/the lower serial shift register " \(B\) " before the most recent \(\uparrow\) transition of the clock
    \(l_{1} \ldots l_{8} \equiv\) The level of steady state inputs of the I/O pins
    \(D O R \equiv\) "Data ORing function" ORing data from both \(1 / O\) pins and register " \(B\) ", i.e., \(l_{1}+b 1, l_{2}+b 2, l_{3}+b 3 \ldots l_{8}+b 8\)
    \(d \equiv\) Data of the serial input

    \section*{Timing Diagram}
    

    AC Test Circuit and Switching Time Waveforms
    

    All diodes are 1N916 or 1N3064.
    \(C_{L}\) includes probe and jig capacitance.

    TL/F/6438-4
    

    TL/F/6438-5
    All input pulses are supplied by generators having \(\mathrm{t}_{\mathrm{f}} \leq 15 \mathrm{~ns}, \mathrm{t}_{\mathrm{f}} \leq 6 \mathrm{~ns}, \mathrm{PRR} \leq 1 \mathrm{MHz}, \mathrm{Z}_{\mathrm{OUT}} \approx 50 \Omega\).

    \section*{Cascading Packages}

    \section*{Cascading Packages for N -Bit Word}
    

    TL/F/6438-6

    National
    Semiconductor
    96LS02/DM96LS02
    Dual Retriggerable Resettable Monostable Multivibrator

    \section*{General Description}

    The 96LS02 is a dual retriggerable and resettable monostable multivibrator. The one-shot provides exceptionally wide delay range, pulse width stability, predictable accuracy and immunity to noise. The pulse width is set by an external resistor and capacitor. Resistor values up to \(1.0 \mathrm{M} \Omega\) reduce required capacitor values. Hysteresis is provided on both trigger inputs of the 96LS02 for increased noise immunity.

    \section*{Features}
    - Required timing capacitance reduced by factors of 10 to 100 over conventional designs
    ■ Broad timing resistor range- \(1.0 \mathrm{k} \Omega\) to \(2.0 \mathrm{M} \Omega\)
    ■ Output Pulse Width is variable over a 2000:1 range by resistor control
    - Propagation delay of 35 ns
    - 0.3V hysteresis on trigger inputs
    - Output pulse width independent of duty cycle
    - 35 ns to \(\infty\) output pulse width range

    \section*{Connection Diagram}
    

    TL/F/9816-1
    Order Number 96LS02DMQB, 96LS02FMQB, DM96LS02M or DM96LS02N
    See NS Package Number J16A, M16A, N16E or W16A
    \begin{tabular}{|l|l|}
    \hline Pin Names & \multicolumn{1}{c|}{ Description } \\
    \hline\(\overline{1} 0\) & Trigger Input (Active Falling Edge) \\
    \(\overline{1} 0\) & Schmitt Trigger Input (Active Falling Edge) \\
    11 & Schmitt Trigger Input (Active Rising Edge) \\
    \(\bar{C}_{D}\) & Direct Clear Input (Active LOW) \\
    Q & True Pulse Output \\
    \(\bar{Q}\) & Complementary Pulse Output \\
    \hline
    \end{tabular}

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    96LS Military
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    Storage Temperature Range

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{96LS02 (MIL)} & \multicolumn{3}{|c|}{DM96LS02 (COM)} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
    \hline lOL & Low Level Output Current & & & 4 & & & 8 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    \section*{Electrical Characteristics}

    Over recommended operating free air temperature range (unless otherwised noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & MIL & 2.5 & & & V \\
    \hline & & & COM & 2.7 & 3.4 & & \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\text { Min, } \mathrm{I}_{\mathrm{OL}}=\text { Max }, \\
    & \mathrm{V}_{\mathrm{IH}}=\text { Min }
    \end{aligned}
    \]} & MIL & & & 0.4 & \\
    \hline & & & COM & & 0.35 & 0.5 & V \\
    \hline & & \(\mathrm{lOL}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & COM & & 0.25 & 0.4 & \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=10 \mathrm{~V}\)} & & & 0.1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
    \hline I/L & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Max} \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & MIL & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & COM & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & & 36 & mA \\
    \hline \(\mathrm{V}_{\mathrm{T}+}\) & Positive-Going Threshold Voltage, \(\mathrm{I} 0, \mathrm{II}\) & & & & & 2.0 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{T}-}\)} & \multirow[t]{2}{*}{Negative-Going Threshold Voltage, īo, I1} & & MIL & 0.7 & & & V \\
    \hline & & & COM & 0.8 & & & \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multicolumn{7}{|l|}{\begin{tabular}{l}
    Switching Characteristics \\
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
    \end{tabular}} \\
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{2}{|c|}{96LS (MIL)} & \multicolumn{2}{|l|}{DM96LS (COM)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \({ }_{\text {tpLH }}\) & Propagation Delay \(\overline{10}\) to Q & & 45 & & 55 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay \(\overline{10}\) to \(\bar{Q}\) & & 33 & & 50 & ns \\
    \hline tplu & \[
    \begin{aligned}
    & \text { Propagation Delay } \\
    & 11 \text { to } Q
    \end{aligned}
    \] & & 45 & & 60 & ns \\
    \hline tPHL & Propagation Delay 11 to \(\bar{Q}\) & & 33 & & 55 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay \(\overline{\mathrm{C}}_{\mathrm{D}}\) to Q & & 25 & & 30 & ns \\
    \hline tplH & Propagation Delay \(\overline{\mathrm{C}}_{\mathrm{D}}\) to \(\bar{Q}\) & & 30 & & 35 & ns \\
    \hline \(\mathrm{tw}_{\text {w }}(\mathrm{L})\) & \(\overline{10}\) Pulse Width LOW & 15 & & 15 & & ns \\
    \hline \(\mathrm{tw}_{\text {w }}(\mathrm{H})\) & 11 Pulse With HIGH & 30 & & 30 & & ns \\
    \hline \(\mathrm{tw}_{\text {w }}(\mathrm{L})\) & \(\bar{C}_{D}\) Pulse Width LOW & 22 & & 22 & & ns \\
    \hline \(\mathrm{tw}_{\text {w }}(\mathrm{H})\) & Minimum Q Pulse Width HIGH & 20 & 70 & 25 & 55 & ns \\
    \hline \(t_{w}\) & Q Pulse Witdh & 4.25 & 5.0 & 4.1 & 4.5 & \(\mu \mathrm{s}\) \\
    \hline RX & Timing Resistor Range* & & & 1 & 1000 & k \(\Omega\) \\
    \hline t & Change in Q Pulse Width over Temperature & & & & 1.0 & \% \\
    \hline t & Change in Q Pulse Width over \(\mathrm{V}_{\mathrm{CC}}\) Range & & & & 0.8
    1.5 & \% \\
    \hline \multicolumn{3}{|l|}{\begin{tabular}{l}
    Functional Description \\
    The 96LS02 dual retriggerable resettable monostable multivibrator has two DC coupled trigger inputs per function, one active LOW ( \(\overline{1} 0)\) and one active HIGH (11). The It input and io input of the 96LS02 utilize an internal Schmitt trigger with hysteresis of 0.3 V to provide increased noise immunity. The use of active HIGH and LOW inputs allows either rising or falling edge triggering and optional non-retriggerable operation. The inputs are DC coupled making triggering independent of input transition times. When input conditions for triggering are met, the Q output goes HIGH and the external capacitor is rapidly discharged and then allowed to recharge. An input trigger which occurs during the timing cycle will retrigger the circuit and result in Q remaining HIGH. The output pulse may be terminated ( \(Q\) to the LOW state) at any time by setting the Direct Clear input LOW. Retriggering may be inhibited by tying the \(\overline{\mathrm{Q}}\) output to \(\overline{\mathrm{O}} \mathrm{O}\) or the Q output to 11 . Differential sensing techniques are used to obtain excellent stability over temperature and power supply variations and a feedback Darlington capacitor discharge circuit minimizes pulse width variation from unit to unit. Schottky TTL output stages provide high switching speeds and output compatibility with all TTL logic families.
    \end{tabular}} & \begin{tabular}{l}
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    outpu \\
    F is d \\
    \(R x\) is \\
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    outpu \\
    be d \\
    obtain \\
    g circ \\
    N2 (4) \\
    N1 (15)
    \end{tabular} & \begin{tabular}{l}
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    \(\mathrm{k} \Omega\) to \\
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    14) and \\
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    \end{tabular} & \begin{tabular}{l}
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    directly ected to 1(15) the tim \(x \geq 1\) \\
    x ns or \\
    \(10 \mathrm{k} \Omega\) width \\
    by remo
    \(\qquad\)
    \end{tabular} & \begin{tabular}{l}
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    \(C_{x} \geq\) \\
    \(\Omega \Omega, C_{x}\) is \\
    1000 pF X or RX \\
    ming, the \\
    \(5 \mathrm{k} \Omega\) \\
    /F/9816-4
    \end{tabular} \\
    \hline
    \end{tabular}
    *Applies only over commercial \(\mathrm{V}_{\mathrm{CC}}\) and \(\mathrm{T}_{\mathrm{A}}\) range for 96 S 02 .

    \section*{Functional Description}

    The 96LS02 dual retriggerable resettable monostable multivibrator has two DC coupled trigger inputs per function, one active LOW (10) and one active HIGH (11). The It input and h in of 0 L有 falling acde tion. The inputs are DC coupled making triggering independent of input transition times. When input conditions for trigare met, the Q output goes HIGH and the external charge An input trigger which occurs during the timing cycle will retrigger the circuit and result in Q remaining HIGH. The output pulse may be terminated ( \(Q\) to the LOW state) at any time by setting the Direct Clear input LOW. Retriggering may be inhibited by tying the \(\bar{Q}\) output to \(\overline{1} 0\) or the \(Q\) output to 11 . Differential sensing techniques are used to obtain excellent slability over temperature and power supply variations and a ark Darlington capacitor discharge circuit minimizes stages provide high switching speeds and output compatibility with all TTL logic families.

    \section*{Operation Notes}

    \section*{timing}
    1. An external resistor ( \(\mathrm{R}_{\mathrm{X}}\) ) and an external capacitor ( \(\mathrm{C}_{\mathrm{X}}\) ) are required as shown in the Logic Diagram. The value of SO2)
    2. The val if her the pasificant leakage relative the pulse width obtained.
    3. Polarized capacitors may be used directly. The ( + ) terminal of a polarized capacitor is connected to pin 1 (15), the -) terminal to pin 2(14) and Rx. Pin 1(15) will remain posi2(14) during the timing cycle. 1000 pF is determined as follows:
    \[
    t_{w}=0.43 R_{X} C_{X}
    \]

    Where \(R_{X}\) is in \(k \Omega, C_{X}\) is in \(p F\), \(t\) is in ns or \(R_{X}\) is in \(k \Omega, C_{X}\) is 5. The output pulse width for \(\mathrm{R}_{\mathrm{X}}<10 \mathrm{k} \Omega\) or \(\mathrm{C}_{\mathrm{X}}<1000 \mathrm{pF}\) should be determined from pulse width versus \(C_{X}\) or \(R_{X}\) graphs.
    6. To obtain variable pulse width by remote trimming, the following circuit is recommended:
    

    TL/F/9816-4

    \section*{Operation Notes (Continued)}
    7. Under any operating condition, \(\mathrm{C}_{X}\) and \(\mathrm{R}_{X}\) (Min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
    8. \(\mathrm{V}_{\mathrm{CC}}\) and ground wiring should conform to good high frequency standards so that switching transients on \(V_{C C}\) and ground leads do not cause interaction between one shots. Use of a \(0.01 \mu \mathrm{~F}\) to \(0.1 \mu \mathrm{~F}\) bypass capacitor between \(\mathrm{V}_{\mathrm{CC}}\) and ground located near the circuit is recommended.

    \section*{TRIGGERING}
    1. The minimum negative pulse width into \(\overline{0} 0\) is 8.0 ns ; the minimum positive pulse width into 11 is 12 ns .
    

    TL/F/9816-5

    Triggering Truth Table
    \begin{tabular}{|ccc|l|}
    \hline \multicolumn{4}{c|}{\begin{tabular}{c} 
    Pin No's. \\
    4(12)
    \end{tabular}} \\
    \(\mathbf{5 ( 1 1 )}\) & 3(13) & Operation \\
    \hline\(H \rightarrow L\) & \(L\) & \(H\) & Trigger \\
    \(H\) & \(L \rightarrow H\) & \(H\) & Trigger \\
    \(X\) & \(X\) & \(L\) & Reset \\
    \hline
    \end{tabular}

    \footnotetext{
    \(H=H I G H\) Voltage Level \(\geq V_{\mathbb{I}}\)
    \(\mathrm{L}=\) LOW Voltage Level \(\leq \mathrm{V}_{\mathrm{IL}}\)
    \(X=\) Immaterial (either H or L )
    \(H \rightarrow L=\) HIGH to LOW Voltage Level Transition
    \(\mathrm{L} \rightarrow \mathrm{H}=\) LOW to HIGH Voltage Level Transition
    }
    2. Input signals to the 96LS02 exhibiting slow or noisy transitions can use either trigger as both are Schmitt triggers.
    3. When non-retriggerable operation is required, i.e., when input triggers are to be ignored during quasi-stable state, input latching is used to inhibit retriggering.
    4. An overriding active LOW level direct clear is provided on each multivibrator. By applying a LOW to the clear, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW. A LOW-to-HIGH transition on \(\overline{\mathrm{C}}_{\mathrm{D}}\) will not trigger the 96LS02. If the \(\overline{\mathrm{C}}_{\mathrm{D}}\) input goes HIGH coincident with a trigger transition, the circuit will respond to the trigger.
    

    \section*{Logic Symbol}
    

    TL/F/9816-2

    \section*{Logic Diagram}

    \section*{96LS02}
    

    TL./F/9816-3

    \section*{Typical Performance Characteristics}
    
    

    FIGURE A

    Section 3
    Schottky

    \section*{Section 3-Schottky}
    Schottky-Commercial Products
    DM74S00 Quad 2-Input NAND Gate ..... 3-3
    DM74S02 Quad 2-Input NOR Gate ..... 3-5
    DM74S03 Quad 2-Input NAND Gate with Open-Collector Outputs ..... 3-7
    DM74S04 Hex Inverter ..... 3-9
    DM74S05 Hex Inverter with Open-Collector Outputs ..... 3-11
    DM74S08 Quad 2-Input AND Gate ..... 3-13
    DM74S09 Quad 2-Input AND Gate with Open-Collector Outputs ..... 3-15
    DM74S10 Triple 3-Input NAND Gate ..... 3-17
    DM74S11 Triple 3-Input AND Gate ..... 3-19
    DM74S20 Dual 4-Input NAND Gate ..... 3-21
    DM74S30 8-Input NAND Gate ..... 3-23
    DM74S32 Quad 2-Input OR Gate ..... 3-25
    DM74S40 Dual 4-Input NAND Buffer ..... 3-27
    DM74S51 Dual 2-Wide 2-Input AND-OR-INVERT Gate ..... 3-29
    DM74S64 4-Wide AND-OR-INVERT Gate ..... 3-31
    DM74S74 Dual Positive-Edge-Triggered D Flip-Flop with Preset, Clear, and Complementary Outputs ..... 3-33
    DM74S86 Quad 2-Input EXCLUSIVE-OR Gate ..... 3-36
    DM74S109 Dual Positive-Edge-Triggered J-K Flip-Flop with Preset, Clear, and Complementary Outputs ..... 3-38
    DM74S112 Dual Negative-Edge-Triggered J-K Flip-Flop with Preset, Clear, and Complementary Outputs ..... 3-41
    DM74S113 Dual Negative-Edge-Triggered J-K Flip-Flop with Preset and Complementary Outputs ..... 3-44
    DM74S132 Quad 2-Input Schmitt Trigger NAND Gate ..... 3-47
    DM74S133 13-Input NAND Gate ..... 3-50
    DM74S138 3-to-8 Line Decoder/Demultiplexer ..... 3-52
    DM74S139 Dual 2-to-4 Line Decoder/Demultiplexer ..... 3-52
    DM74S140 Dual 4-Input NAND \(50 \Omega\) Line Driver ..... 3-56
    DM74S151 1-of-8 Line Data Selector/Multiplexer with Complementary Outputs ..... 3-59
    DM74S153 Dual 1-of-4 Line Data Selector/Multiplexer ..... 3-63
    DM74S157 Quad 2-to-1 Line Data Selector/Multiplexer ..... 3-66
    DM74S158 Quad 2-to-1 Line Inverting Data Selector/Multiplexer ..... 3-66
    DM74S161 Synchronous 4-Bit Binary Counter with Asynchronous Clear ..... 3-71
    DM74S163 Synchronous 4-Bit Binary Counter with Synchronous Clear ..... 3-71
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    DM74S182 Look-Ahead Carry Generator ..... 3-90
    DM74S194 4-Bit Bidirectional Universal Shift Register ..... 3-94
    DM74S195 4-Bit Parallel Access Shift Register ..... 3-98
    DM74S240 Octal TRI-STATE Inverting Buffer/Line Driver/Line Receiver ..... 3-102
    DM74S241 Octal TRI-STATE Buffer/Line Driver/Line Receiver ..... 3-102
    DM74S244 Octal TRI-STATE Buffer/Line Driver/Line Receiver ..... 3-102
    DM74S251 TRI-STATE 1-of-8 Line Data Selector/Multiplexer with Complementary Outputs ..... 3-105
    DM74S253 Dual TRI-STATE 1-of-4 Line Data Selector/Multiplexer ..... 3-109
    Section 3-Schottky (Continued)
    Schottky-Commercial Products (Continued)
    DM74S257 Quad TRI-STATE 2-to-1 Line Data Selector/Multiplexer ..... 3-112
    DM74S258 Quad TRI-STATE 2-to-1 Line Inverting Data Selector/Multiplexer ..... 3-112
    DM74S280 9-Bit Parity Generator/Checker ..... 3-117
    DM74S283 4-Bit Binary Adder with Fast Carry ..... 3-121
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    DM74S373 Octal TRI-STATE Transparent D Latch ..... 3-130
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    DM96S02 Dual Retriggerable Resettable Monostable Multivibrator (One-Shot) ..... 3-165
    Schottky—Mil/Aero Products
    DM54S00 Quad 2-Input NAND Gate ..... 3-3
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    DM54S04 Hex Inverter ..... 3-9
    DM54S08 Quad 2-Input AND Gate ..... 3-13
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    DM54S74 Dual Positive-Edge-Triggered D Flip-Flop with Preset, Clear, and Complementary Outputs ..... 3-33
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    DM54S112 Dual Negative-Edge-Triggered J-K Flip-Flop with Preset, Clear, and Complementary Outputs ..... 3-41
    DM54S113 Dual Negative-Edge-Triggered J-K Flip-Flop with Preset and Complementary Outputs ..... 3-44
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    DM54S138 3-to-8 Line Decoder/Demultiplexer ..... 3-52
    DM54S139 Dual 2-to-4 Line Decoder/Demultiplexer ..... 3-52
    DM54S140 Dual 4-Input NAND \(50 \Omega\) Line Driver ..... 3-56
    DM54S151 1-of-8 Line Data Selector/Multiplexer with Complementary Outputs ..... 3-59
    DM54S153 Dual 1-of-4 Line Data Selector/Multiplexer ..... 3-63
    DM54S157 Quad 2-to-1 Line Data Selector/Multiplexer ..... 3-66
    DM54S158 Quad 2-to-1 Line Inverting Data Selector/Multiplexer ..... 3-66
    DM54S161 Synchronous 4-Bit Binary Counter with Asynchronous Clear ..... 3-71
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    DM54S174 Hex D Flip-Flop with Clear ..... 3-77
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    DM54S181 Arithmetic Logic Unit/Function Generator ..... 3-81
    DM54S182 Look-Ahead Carry Generator ..... 3-90
    DM54S194 4-Bit Bidirectional Universal Shift Register ..... 3-94
    DM54S195 4-Bit Parallel Access Shift Register ..... 3-98
    DM54S240 Octal TRI-STATE Inverting Buffer/Line Driver/Line Receiver ..... 3-102
    DM54S241 Octal TRI-STATE Buffer/Line Driver/Line Receiver ..... 3-102
    Section 3-Schottky (Continued)
    Schottky-Mil/Aero Products (Continued)
    DM54S244 Octal TRI-STATE Buffer/Line Driver/Line Receiver ..... 3-102
    DM54S251 TRI-STATE 1-of-8 Line Data Selector/Multiplexer with Complementary Outputs ..... 3-105
    DM54S253 Dual TRI-STATE 1-of-4 Line Data Selector/Multiplexer ..... 3-109
    DM54S257 Quad TRI-STATE 2-to-1 Line Data Selector/Multiplexer ..... 3-112
    DM54S258 Quad TRI-STATE 2-to-1 Line Inverting Data Selector/Multiplexer ..... 3-112
    DM54S280 9-Bit Parity Generator/Checker ..... 3-117
    DM54S283 4-Bit Binary Adder with Fast Carry ..... 3-121
    DM54S373 Octal TRI-STATE Transparent D Latch ..... 3-130
    DM54S374 Octal TRI-STATE Positive-Edge-Triggered D Flip-Flop ..... 3-130

    \section*{DM54S00/DM74S00 Quad 2-Input NAND Gates}

    \section*{General Description}

    This device contains four independent gates each of which performs the logic NAND function.

    \section*{Connection Diagram}
    

    Order Number DM54S00J, DM54S00W, DM74S00M or DM74S00N See NS Package Number J14A, M14A, N14A or W14B

    Function Table
    \begin{tabular}{|c|c|c|}
    \multicolumn{3}{c|}{\(\mathbf{Y}=\overline{\mathbf{A B}}\)} \\
    \hline \multicolumn{2}{|c|}{ Inputs } & Output \\
    \hline \(\mathbf{A}\) & \(\mathbf{B}\) & \(\mathbf{Y}\) \\
    \hline L & L & \(H\) \\
    L & \(H\) & \(H\) \\
    \(H\) & L & \(H\) \\
    \(H\) & \(H\) & L \\
    \hline
    \end{tabular}
    \(H=\) High Logic Level
    \(L=\) Low Logic Level

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    5.5 V

    Operating Free Air Temperature Range
    DM54S
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    DM74S \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    Storage Temperature Range

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S00} & \multicolumn{3}{|c|}{DM74S00} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{\text {l }}\) & High Level Output Current & & & -1 & & & -1 & mA \\
    \hline \(\mathrm{IOL}^{\text {l }}\) & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M i n, l_{1}=-18 \mathrm{~mA}\)} & & & \(-1.2\) & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O H}=M a x \\
    & V_{\mathrm{IL}}=M a x
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline \(\mathrm{I}_{\mathrm{LL}}\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=\operatorname{Max}
    \] \\
    (Note 2)
    \end{tabular}} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\) Max} & & 10 & 16 & mA \\
    \hline \({ }^{\text {ICCL }}\) & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 20 & 36 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PL }}\) & Propagation Delay Time Low to High Level Output & 2 & 4.5 & 2 & 7 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & 2 & 5 & 2 & 8 & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time and the duration should not exceed one second.

    DM54S02/DM74S02 Quad 2-Input NOR Gates

    \section*{General Description}

    This device contains four independent gates each of which performs the logic NOR function.

    \section*{Connection Diagram}
    

    Function Table
    \begin{tabular}{|c|c|c|}
    \multicolumn{3}{c|}{\(\mathbf{Y}=\overline{\mathbf{A}+\mathbf{B}}\)} \\
    \hline \multicolumn{2}{|c|}{ Inputs } & Output \\
    \hline \(\mathbf{A}\) & \(\mathbf{B}\) & \(\mathbf{Y}\) \\
    \hline L & L & H \\
    L & \(H\) & L \\
    H & L & L \\
    H & \(H\) & L \\
    \hline
    \end{tabular}
    \(H=\) High Logic Level
    L = Low Logic Level
    \begin{tabular}{lr} 
    Absolute Maximum Ratings (Note) \\
    Af Military/Aerospace specified devices are required, \\
    please contact the National Semiconductor Sales \\
    Office/Distributors for availability and specifications. \\
    Supply Voltage & 7 V \\
    Input Voltage & 5.5 V \\
    Operating Free Air Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM54S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    DM74S & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S02} & \multicolumn{3}{|c|}{DM74S02} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{\text {l }}\) & High Level Output Current & & & -1 & & & -1 & mA \\
    \hline lOL & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M i n, l_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\
    & V_{I L}=\operatorname{Max}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\)} & & 17 & 29 & mA \\
    \hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}\)} & & 26 & 45 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & 1.5 & 5.5 & 2 & 7.5 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & 1.5 & 5.5 & 2 & 7.5 & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{DM74S03 Quad 2-Input NAND Gates with Open-Collector Outputs}

    \section*{General Description}

    This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

    Pull-Up Resistor Equations
    \(R_{M A X}=\frac{V_{\mathrm{CC}}(\mathrm{Min})-\mathrm{V}_{\mathrm{OH}}}{\mathrm{N}_{1}\left(\mathrm{IOH}_{\mathrm{OH}}\right)+\mathrm{N}_{2}\left(\mathrm{I}_{\mathrm{I}}\right)}\)
    \(R_{\text {MIN }}=\frac{V_{C C}(\text { Max })-V_{\mathrm{OL}}}{l_{\mathrm{OL}}-\mathrm{N}_{3}\left(\mathrm{IIL}^{\prime}\right)}\)
    Where: \(\mathrm{N}_{1}\left(\mathrm{I}_{\mathrm{OH}}\right)=\) total maximum output high current for all outputs tied to pull-up resistor
    \(\mathrm{N}_{2}\left(\mathrm{I}_{\mathrm{H}}\right)=\) total maximum input high current for all inputs tied to pull-up resistor
    \(N_{3}\left(l_{I L}\right)=\) total maximum input low current for all inputs tied to pull-up resistor

    \section*{Connection Diagram}
    

    \section*{Function Table}
    \(\mathbf{Y}=\overline{\mathbf{A B}}\)
    \begin{tabular}{|c|c|c|}
    \hline \multicolumn{2}{|c|}{ Inputs } & Output \\
    \hline A & \(\mathbf{B}\) & \(\mathbf{Y}\) \\
    \hline L & L & \(H\) \\
    L & \(H\) & \(H\) \\
    \(H\) & L & \(H\) \\
    \(H\) & \(H\) & L \\
    \hline
    \end{tabular}

    \footnotetext{
    \(H=\) High Logic Level
    L = Low Logic Level
    }
    \begin{tabular}{lr} 
    Supply Voltage & 7 V \\
    Input Voltage & 5.5 V \\
    Output Voltage & 7 V \\
    Operating Free Air Temperature Range & \\
    DM74S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{l|l|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multirow{2}{|c|}{ Parameter } & \multicolumn{2}{c|}{ DM74S03 } & \multirow{2}{*}{ Units } \\
    \cline { 3 - 4 } & & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline \(\mathrm{~V}_{\mathrm{OH}}\) & High Level Output Voltage & & & 5.5 & V \\
    \hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 20 & mA \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\) & & & -1.2 & V \\
    \hline \(I_{\text {CEX }}\) & High Level Output Current & \[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, V_{O}=5.5 \mathrm{~V} \\
    & V_{I L}=\operatorname{Max}
    \end{aligned}
    \] & & & 250 & \(\mu \mathrm{A}\) \\
    \hline VOL & Low Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \] & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{C C}=\) Max, \(\mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\) & & & 50 & \(\mu \mathrm{A}\) \\
    \hline ILL & Low Level Input Current & \(V_{C C}=\) Max, \(V_{1}=0.5 \mathrm{~V}\) & & & -2 & mA \\
    \hline ICCH & Supply Current with Outputs High & \(V_{C C}=\operatorname{Max}\) & & 6.0 & 13.2 & mA \\
    \hline \(\mathrm{I}_{\text {CCL }}\) & Supply Current with Outputs Low & \(V_{C C}=\operatorname{Max}\) & & 20 & 36 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=\mathbf{2 8 0} \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & 2 & 7.5 & 3 & 11 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & 2 & 7 & 3 & 11 & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).

    \section*{National Semiconductor \\ DM54S04/DM74S04 Hex Inverting Gates}

    \section*{General Description}

    This device contains six independent gates each of which performs the logic INVERT function.

    \section*{Connection Diagram}
    

    Order Number DM54S04J, DM54S04W, DM74S04M or DM74S04N See NS Package Number J14A, M14A, N14A or W14B

    \section*{Function Table}
    \begin{tabular}{|c|c|}
    \multicolumn{2}{c|}{\(\mathbf{Y}=\overline{\mathbf{A}}\)} \\
    \hline Input & Output \\
    \hline \(\mathbf{A}\) & \(\mathbf{Y}\) \\
    \hline L & H \\
    \(H\) & L \\
    \hline
    \end{tabular}
    \(\mathrm{H}=\) High Logic Level
    \(\mathrm{L}=\) Low Logic Level

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S04} & \multicolumn{3}{|c|}{DM74S04} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -1 & & & -1 & mA \\
    \hline \(\mathrm{lOL}^{\text {l }}\) & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O L}=M a x \\
    & V_{I H}=M i n
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\[
    V_{C C}=\operatorname{Max}, V_{1}=0.5 \mathrm{~V}
    \]} & & & -2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\text { Max } \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 15 & 24 & mA \\
    \hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(V_{C C}=M a x\)} & & 30 & 54 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & 2 & 4.5 & 2 & 7 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & 2 & 5 & 2 & 8 & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{DM74S05 Hex Inverters with Open-Collector Outputs}

    \section*{General Description}

    This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

    Pull-Up Resistor Equations
    \(R_{\text {MAX }}=\frac{V_{\mathrm{CC}}(\mathrm{Min})-\mathrm{V}_{\mathrm{OH}}}{\mathrm{N}_{1}\left(\mathrm{I}_{\mathrm{OH}}\right)+\mathrm{N}_{2}\left(I_{\mathrm{IH}}\right)}\)
    \(R_{\text {MIN }}=\frac{V_{C C}(M a x)-V_{O L}}{I_{O L}-N_{3}\left(I_{L L}\right)}\)
    Where: \(\mathrm{N}_{1}\left(\mathrm{l}_{\mathrm{OH}}\right)=\) total maximum output high current for all outputs tied to pull-up resistor
    \(\mathrm{N}_{2}\left(\mathrm{I}_{\mathrm{H}}\right)=\) total maximum input high current for all inputs tied to pull-up resistor
    \(N_{3}\left(I_{I L}\right)=\) total maximum input low current for all inputs tied to pull-up resistor

    \section*{Connection Diagram}
    

    \section*{Function Table}
    \begin{tabular}{|c|c|}
    \hline Input & Output \\
    \hline \(\mathbf{A}\) & \(\mathbf{Y}\) \\
    \hline L & \(H\) \\
    \(H\) & L \\
    \hline
    \end{tabular}

    \footnotetext{
    \(H=\) High Logic Level
    }

    L = Low Logic Level

    Absolute Maximum Ratings (Note)
    \begin{tabular}{lr} 
    Supply Voltage & 7 V \\
    Input Voltage & 5.5 V \\
    Output Voltage & 7 V \\
    Operating Free Air Temperature & \\
    Range & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{l|l|c|c|c|c}
    \hline Symbol & Parameter & Min & Nom & Max & Units \\
    \hline\(V_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline \(\mathrm{~V}_{\mathrm{OH}}\) & High Level Output Voltage & & & 5.5 & V \\
    \hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 20 & mA \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & Typ & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\) & & & -1.2 & V \\
    \hline ICEX & High Level Output Current & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{O}}=5.5 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \] & & & 250 & \(\mu \mathrm{A}\) \\
    \hline VOL & Low Level Output Voltage & \[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \] & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
    \hline \(\mathrm{IIH}_{\mathrm{H}}\) & High Level Input Current & \(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\) & & & 50 & \(\mu \mathrm{A}\) \\
    \hline \(\mathrm{I}_{\text {L }}\) & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\) & & & -2 & mA \\
    \hline ICCH & Supply Current with Outputs High & \(V_{C C}=\operatorname{Max}\) & & 9 & 19.8 & mA \\
    \hline ICCL & Supply Current with Outputs Low & \(\mathrm{V}_{C C}=\mathrm{Max}\) & & 30 & 54 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & 2 & 7.5 & 3 & 11 & ns \\
    \hline \({ }^{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & 2 & 7 & 3 & 11 & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).

    \section*{DM54S08/DM74S08 Quad 2-Input AND Gates}

    \section*{General Description}

    This device contains four independent gates each of which performs the logic AND function.

    \section*{Connection Diagram}
    

    Order Number DM54S08J, DM54S08W or DM74S08N See NS Package Number J14A, N14A or W14B

    \section*{Function Table}
    \begin{tabular}{|c|c|c|}
    \hline \multicolumn{3}{|c|}{ Inputs } \\
    \hline\(A\) & \(B\) & Output \\
    \hline\(L\) & \(L\) & \(L\) \\
    \(L\) & \(H\) & \(L\) \\
    \(H\) & \(L\) & \(L\) \\
    \(H\) & \(H\) & \(H\) \\
    \hline
    \end{tabular}

    \footnotetext{
    \(H=\) High Logic Level
    \(L=\) Low Logic Level
    }
    \begin{tabular}{lr} 
    Absolute Maximum Ratings (Note) \\
    If Military/Aerospace specified devices are required, \\
    please contact the National Semiconductor Sales \\
    Office/Distributors for availability and specifications. \\
    Supply Voltage & 7 V \\
    Input Voltage & 5.5 V \\
    Operating Free Air Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM54S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    DM74S & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S08} & \multicolumn{3}{|c|}{DM74S08} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline \(\mathrm{lOH}^{\text {O }}\) & High Level Output Current & & & -1 & & & -1 & mA \\
    \hline lOL & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, l_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O L}=M a x \\
    & V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \({ }_{1 / H}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline \(1 / 2\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\text { Max } \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -40 & & \(-100\) & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & \(-100\) & \\
    \hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 18 & 32 & mA \\
    \hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & 32 & 57 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & 2.5 & 7 & 3 & 9 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & 2.5 & 7.5 & 3 & 11 & ns \\
    \hline
    \end{tabular}

    \footnotetext{
    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    }

    \section*{DM74S09 Quad 2-Input AND Gates with Open-Collector Outputs}

    \section*{General Description}

    This device contains four independent gates each of which performs the logic AND function. The open-collector outputs require an external pull-up resistor for proper logical operation.

    \section*{Pull-Up Resistor Equations}
    \(R_{\text {MAX }}=\frac{V_{\mathrm{CC}}(\mathrm{Min})-\mathrm{V}_{\mathrm{OH}}}{\mathrm{N}_{1}\left(\mathrm{IOH}_{\mathrm{OH}}\right)+\mathrm{N}_{2}\left(\mathrm{I}_{\mathrm{IH}}\right)}\)
    \(R_{\text {MIN }}=\frac{V_{C C}(\text { Max })-V_{\mathrm{OL}}}{I_{\mathrm{OL}}-N_{3}\left(l_{\mathrm{IL}}\right)}\)
    Where: \(\mathrm{N}_{1}\left(\mathrm{l}_{\mathrm{OH}}\right)=\) total maximum output high current for all outputs tied to pull-up resistor
    \(\mathrm{N}_{2}\left(\mathrm{I}_{\mathrm{H}}\right)=\) total maximum input high current for all inputs tied to pull-up resistor
    \(\mathrm{N}_{3}\left(l_{I L}\right)=\) total maximum input low current for all inputs tied to pull-up resistor

    \section*{Connection Diagram}

    \section*{Dual-In-Line Package}
    

    \section*{Function Table}
    \begin{tabular}{|c|c|c|}
    \multicolumn{3}{c|}{\(\mathbf{Y}=\mathbf{A B}\)} \\
    \begin{tabular}{|c|c|c|}
    \hline \multicolumn{2}{|c|}{ Inputs } & Output \\
    \hline \(\mathbf{A}\) & \(\mathbf{B}\) & \(\mathbf{Y}\) \\
    \hline\(L\) & \(L\) & L \\
    L & \(H\) & L \\
    \(H\) & \(L\) & L \\
    \(H\) & \(H\) & \(H\) \\
    \hline
    \end{tabular}
    \end{tabular}
    \(H=\) High Logic Level
    L = Low Logic Level
    \begin{tabular}{|c|c|}
    \hline Supply Voltage & te) \\
    \hline Input Voltage & 5.5 V \\
    \hline Output Voltage & 7 V \\
    \hline Operating Free Air Temperature Range DM74S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ}\) \\
    \hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    Recommended Operating Conditions
    \begin{tabular}{l|l|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multirow{2}{|c|}{ Parameter } & \multicolumn{2}{|c|}{ DM74S09 } & \multirow{2}{*}{ Units } \\
    \cline { 3 - 4 } & & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline \(\mathrm{~V}_{\mathrm{OH}}\) & High Level Output Voltage & & & 5.5 & V \\
    \hline \(\mathrm{l}_{\mathrm{OL}}\) & Low Level Output Current & & & 20 & mA \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & \begin{tabular}{l}
    Typ \\
    (Note 1)
    \end{tabular} & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\) & & & -1.2 & V \\
    \hline ICEX & High Level Output Current & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{O}}=5.5 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \] & & & 250 & \(\mu \mathrm{A}\) \\
    \hline VOL & Low Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \] & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\) & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL. & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\) & & & -2 & mA \\
    \hline ICCH & Supply Current with Outputs High & \(\mathrm{V}_{\mathrm{CC}}=\) Max & & 18 & 32 & mA \\
    \hline ICCL & Supply Current with Outputs Low & \(V_{C C}=\) Max & & 32 & 57 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(R_{L}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & 3 & 10 & 4 & 18 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & 3 & 10 & 4 & 18 & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).

    \section*{DM54S10/DM74S10 Triple 3-Input NAND Gates}

    \section*{General Description}

    This device contains three independent gates each of which performs the logic NAND function.

    \section*{Connection Diagram}
    

    Function Table
    \[
    \mathbf{Y}=\overline{\mathbf{A B C}}
    \]
    \begin{tabular}{|c|c|c|c|}
    \hline \multicolumn{3}{|c|}{ Inputs } & Output \\
    \hline A & B & C & Y \\
    \hline X & X & L & H \\
    X & L & X & H \\
    L & X & X & H \\
    H & H & H & L \\
    \hline
    \end{tabular}
    \(H=\) High Logic Level
    L = Low Logic Level
    X = Either Low or High Logic Level
    \(\begin{array}{lr}\text { Absolute Maximum Ratings (Note) } \\ \text { If Military/Aerospace specified devices are required, } \\ \text { please contact the National Semiconductor Sales } \\ \text { Office/Distributors for availability and specifications. } \\ \text { Supply Voltage } & 7 \mathrm{~V} \\ \text { Input Voltage } & 5.5 \mathrm{~V} \\ \text { Operating Free Air Temperature Range } & \\ \text { DM54S } & -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\ \text { DM74S } & 0^{\circ} \mathrm{C} \text { to }+70^{\circ} \mathrm{C} \\ \text { Storage Temperature Range } & -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C}\end{array}\)
    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S10} & \multicolumn{3}{|c|}{DM74S10} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -1 & & & -1 & mA \\
    \hline lOL & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Min}, I_{1}=-18 \mathrm{~mA}\)} & & & \(-1.2\) & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}_{\mathrm{OL}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=M a x
    \] \\
    (Note 2)
    \end{tabular}} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline \(\mathrm{I}_{\mathrm{CCH}}\) & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 7.5 & 12 & mA \\
    \hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}\)} & & 15 & 27 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & 2 & 4.5 & 2 & 7 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & 2 & 5 & 2 & 8 & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{National Semiconductor \\ DM54S11/DM74S11 Triple 3-Input AND Gates}

    \section*{General Description}

    This device contains three independent gates each of which performs the logic AND function.

    \section*{Connection Diagram}
    

    TL/F/6447-1
    Order Number DM54S11J, DM54S11W or DM74S11N See NS Package Number J14A, N14A or W14B
    Function Table
    \begin{tabular}{c}
    \multicolumn{4}{c|}{ Y ABC } \\
    \begin{tabular}{|c|c|c|c|}
    \hline \multicolumn{3}{|c|}{ Inputs } & Output \\
    \hline A & B & C & Y \\
    \hline\(X\) & \(X\) & \(L\) & \(L\) \\
    \(X\) & \(L\) & \(X\) & \(L\) \\
    \(L\) & \(X\) & \(X\) & \(L\) \\
    \(H\) & \(H\) & \(H\) & \(H\) \\
    \hline
    \end{tabular}
    \end{tabular}
    \(H=\) High L.ogic Level
    L = Low Logic Level
    \(X=\) Either Low or High Logic Level
    \begin{tabular}{l} 
    Absolute Maximum Ratings (Note) \\
    If Military/Aerospace speclified devices are required, \\
    please contact the National Semilonductor Sales \\
    Office/Distributors for avallability and specifications. \\
    Supply Voltage \\
    Input Voltage \\
    Operating Free Air Temperature Range \\
    DM54S \\
    DM74S \\
    Storage Temperature Range \\
    SM \\
    \hline
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S11} & \multicolumn{3}{|c|}{DM74S11} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{\text {l }}\) & High Level Output Current & & & -1 & & & -1 & mA \\
    \hline \(\mathrm{lOL}^{\text {l }}\) & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\text { Max } \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(V_{C C}=M a x\)} & & 13.5 & 24 & mA \\
    \hline \({ }^{\text {ICCL }}\) & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & 24 & 42 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & 2.5 & 7 & 3 & 9 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & 2.5 & 7.5 & 3 & 11 & ns \\
    \hline
    \end{tabular}

    \footnotetext{
    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    }

    \section*{General Description}

    This device contains two independent gates each of which performs the logic NAND function.

    \section*{Connection Diagram}
    

    Function Table
    \(\mathbf{Y}=\overline{\mathrm{ABCD}}\)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multicolumn{4}{|c|}{ Inputs } & Output \\
    \hline A & B & C & D & Y \\
    \hline X & X & X & L & H \\
    X & X & L & X & H \\
    X & L & X & X & H \\
    L & X & X & X & H \\
    H & H & H & H & L \\
    \hline
    \end{tabular}
    \(H=\) High Logic Level
    \(L=\) Low Logic Level
    X = Either Low or High Logic Level
    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    \begin{tabular}{lr} 
    DM54S & \\
    DM74S & \\
    Storage Temperature Range & \(55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    Sto \\
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}\(\quad-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{l|l|c|c|c|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multicolumn{2}{|c|}{ Parameter } & \multicolumn{3}{|c|}{ DM54S20 } & \multicolumn{3}{c|}{ DM74S20 } \\
    \cline { 3 - 9 } & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -1 & & & -1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\) Min, \(\mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{V OH} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline ILL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=M a x
    \] \\
    (Note 2)
    \end{tabular}} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & \(-100\) & \\
    \hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 5 & 8 & mA \\
    \hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & 10 & 18 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (see Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & 2 & 4.5 & 2 & 7 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & 2 & 5 & 2 & 8 & ns \\
    \hline
    \end{tabular}

    \footnotetext{
    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    }

    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{DM54S30/DM74S30 8-Input NAND Gate}

    \section*{General Description}

    This device contains a single gate which performs the logic NAND function.

    \section*{Connection Diagram}
    

    Order Number DM54S30J, DM54S30W or DM74S30N See NS Package Number J14A, N14A or W14B

    \section*{Function Table}
    \begin{tabular}{|c|c|}
    \hline \multicolumn{1}{c}{\(=\overline{\text { ABCDEFGH }}\)} \\
    \hline Inputs & Output \\
    \hline A thru H & \(\mathbf{Y}\) \\
    \hline All Inputs H & L \\
    One or More \\
    Input L
    \end{tabular}\(\quad \mathrm{H}\),
    \(H=\) High Logic Level
    \(L=\) Low Logic Level

    \footnotetext{
    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    \begin{tabular}{cr} 
    DM54S & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}
    }

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S30} & \multicolumn{3}{|c|}{DM74S30} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -1 & & & -1 & mA \\
    \hline lOL & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{\mathrm{l}}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{V OH} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O H}=M a x \\
    & V_{I L}=M a x
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline \(1 / 2\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=M a x
    \] \\
    (Note 2)
    \end{tabular}} & DM54 & -40 & & \(-100\) & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & \(-100\) & \\
    \hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & 3 & 5 & mA \\
    \hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\operatorname{Max}\)} & & 5.5 & 10 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline tplH & Propagation Delay Time Low to High Level Output & 2 & 6 & 2 & 8 & ns \\
    \hline \({ }_{\text {tpHL }}\) & Propagation Delay Time High to Low Level Output & 2 & 7 & 3 & 10 & ns \\
    \hline
    \end{tabular}

    \footnotetext{
    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    }

    \section*{General Description}

    This device contains four independent gates each of which performs the logic OR function.

    \section*{Connection Diagram}
    

    Order Number DM54S32J, DM54S32W or DM74S32N
    See NS Package Number J14A, N14A or W14B
    Function Table
    \begin{tabular}{|c|c|c|}
    \multicolumn{3}{c|}{\(\mathbf{Y}=\mathbf{A}+\mathbf{B}\)} \\
    \hline \multicolumn{2}{|c|}{ Inputs } & Output \\
    \hline \(\mathbf{A}\) & \(\mathbf{B}\) & \(\mathbf{Y}\) \\
    \hline L & L & L \\
    L & \(H\) & \(H\) \\
    \(H\) & L & \(H\) \\
    \(H\) & \(H\) & \(H\) \\
    \hline
    \end{tabular}
    \(H=\) High Logic Level
    L = Low Logic Level

    \section*{Absolute Maximum Ratings (Note)}

    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    5.5V

    Operating Free Air Temperature Range
    DM54S
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    Storage Temperature Range
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S32} & \multicolumn{3}{|c|}{DM74S32} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -1 & & & -1 & mA \\
    \hline lOL & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \begin{tabular}{l}
    Typ \\
    (Note 1)
    \end{tabular} & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{VOH} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O L}=M a x \\
    & V_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline 1 IL & Low Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 18 & 32 & mA \\
    \hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(V_{C C}=M a x\)} & & 38 & 68 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(C_{L}=50 \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \({ }_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output & 2 & 7 & 2 & 9 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & 2 & 7 & 2 & 9 & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{DM54S40/DM74S40 Dual 4-Input NAND Buffers}

    \section*{General Description}

    This device contains two independent gates each of which performs the logic NAND function.

    \section*{Connection Diagram}
    

    Order Number DM54S40J, DM54S40W or DM74S40N See NS Package Number J14A, N14A or W16B

    Function Table
    \begin{tabular}{|c|c|c|c|c|}
    \multicolumn{5}{|c|}{ Y \(=\overline{\text { ABCD }}\)} \\
    \hline \multicolumn{4}{|c|}{ Inputs } & Output \\
    \hline A & B & C & D & Y \\
    \hline X & X & X & L & H \\
    X & X & L & X & H \\
    X & L & X & X & H \\
    L & X & X & X & H \\
    H & H & H & H & L \\
    \hline
    \end{tabular}

    \footnotetext{
    \(H=\) High Logic Level
    L = Low Logic Level
    X = Either Low or High Logic Level
    }
    \begin{tabular}{lr} 
    Absolute Maximum Ratings (Note) \\
    If military/Aerospace specified devices are required, \\
    please contact the National Semiconductor Sales \\
    Office/Distributors for availability and specifications. \\
    Supply Voltage & 7 V \\
    Input Voltage & 5.5 V \\
    Operating Free Air Temperature Range & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM54S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    DM74S & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S40} & \multicolumn{3}{|c|}{DM74S40} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline \(\mathrm{lOH}^{\text {l }}\) & High Level Output Current & & & -3 & & & -3 & mA \\
    \hline lOL & Low Level Output Current & & & 60 & & & 60 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \begin{tabular}{l}
    Typ \\
    (Note 1)
    \end{tabular} & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOH}_{\mathrm{O}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{lOL}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, V_{1}=2.7 \mathrm{~V}\)} & & & 100 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\)} & & & -4 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=M a x
    \] \\
    (Note 2)
    \end{tabular}} & DM54 & -50 & & -225 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -50 & & -225 & \\
    \hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & 10 & 18 & mA \\
    \hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(V_{C C}=\) Max} & & 25 & 44 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=93 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=150 \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & 2 & 6.5 & 3 & 9 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & 2 & 6.5 & 3 & 9 & ns \\
    \hline
    \end{tabular}

    \footnotetext{
    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    }

    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{DM74S51 Dual 2-Wide 2-Input AND-OR-INVERT Gates}

    \section*{General Description}

    This device contains two independent combinations of gates each of which performs the logic AND-OR-INVERT function.

    \section*{Connection Diagram}
    

    \section*{Function Table}
    \[
    \mathbf{Y}=\overline{\mathbf{A B}+\mathbf{C D}}
    \]
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multicolumn{4}{|c|}{ Inputs } & Output \\
    \hline A & B & C & D & Y \\
    \hline H & H & X & X & L \\
    X & X & H & H & L \\
    \hline \multicolumn{4}{|c|}{ All other } \\
    combinations
    \end{tabular}\(\quad\) H

    \footnotetext{
    \(H=\) High Logic Level
    L = Low Logic Level
    X = Either Low or High Logic Leve
    }

    Absolute Maximum Ratings (Note)
    \begin{tabular}{lr} 
    Supply Voltage & 7 V \\
    Input Voltage & 5.5 V \\
    Operating Free Air Temperature Range & \\
    DM 74 S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{l|l|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multirow{2}{|c|}{ Parameter } & \multicolumn{2}{c|}{ DM74S51 } & \multirow{2}{*}{ Units } \\
    \cline { 3 - 5 } & & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 20 & mA \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Min}, I_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \] & DM74 & 2.7 & 3.4 & & V \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(I_{1 H}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\) (Note 2)} & -40 & & -100 & mA \\
    \hline \({ }^{\text {ICCH }}\) & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 8.2 & 17.8 & mA \\
    \hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & 14 & 22 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(R_{L}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(C_{L}=50 \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \({ }_{\text {tpLH }}\) & Propagation Delay Time Low to High Level Output & 2 & 5.5 & 3 & 8 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & 2 & 5.5 & 3 & 8 & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{DM54S64/DM74S64 4-Wide AND-OR-INVERT Gates}

    \section*{General Description}

    This device contains a combination of gates which performs the logic AND-OR-INVERT function.

    \section*{Connection Diagram}

    \section*{Dual-In-Line Package}
    

    TL/F/6455-1
    Order Number DM54S64J, DM54S64W or DM74S64N See NS Package Number J14A, N14A or W14B

    Function Table
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{11}{|c|}{Inputs} & Output \\
    \hline A & B & C & D & E & F & G & H & 1 & J & K & Y \\
    \hline H & H & H & H & X & X & X & X & X & X & X & L \\
    \hline X & X & X & X & H & H & X & X & X & X & X & L \\
    \hline X & X & X & X & X & X & H & H & H & X & X & L \\
    \hline X & X & X & X & X & X & X & X & X & H & H & L \\
    \hline \multicolumn{11}{|c|}{All other combinations} & H \\
    \hline
    \end{tabular}

    \footnotetext{
    \(H=\) High Logic Leve
    L = Low Logic Level
    \(X=\) Either Low or High Logic Level
    }

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S64} & \multicolumn{3}{|c|}{DM74S64} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -1 & & & -1 & mA \\
    \hline lOL & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=M i n, I_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=M a x
    \] \\
    (Note 2)
    \end{tabular}} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}\)} & & 7 & 12.5 & mA \\
    \hline \({ }^{\text {c CCL }}\) & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}\)} & & 8.5 & 16 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & 2 & 5.5 & 3 & 8 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & 2 & 5.5 & 3 & 8 & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{DM54S74/DM74S74}

    \title{
    Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear, and Complementary Outputs
    }

    \section*{General Description}

    This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the \(D\) input may
    be changed while the clock is low or high without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

    \section*{Connection Diagram}

    Dual-In-Line Package
    

    TL/F/6457-1
    Order Number DM54S74J, DM54S74W, DM74S74M or DM74S74N See NS Package Number J14A, M14A, N14A or W14B

    \section*{Function Table}
    \begin{tabular}{|l|c|c|c|c|c|}
    \hline \multicolumn{5}{|c|}{ Inputs } & \multicolumn{2}{c|}{ Outputs } \\
    \hline PR & CLR & CLK & D & Q & \(\overline{\mathbf{Q}}\) \\
    \hline L & H & X & X & H & L \\
    H & L & X & X & L & H \\
    L & L & X & X & \(H^{*}\) & \(H^{*}\) \\
    H & H & \(\uparrow\) & H & H & L \\
    H & H & \(\uparrow\) & L & L & H \\
    H & H & L & X & Q \(_{0}\) & \(\bar{Q}_{0}\) \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|}
    \hline \multicolumn{2}{|l|}{Absolute Maximum Ratings (Note)} \\
    \hline \multicolumn{2}{|l|}{please contact the National Semiconductor Sales Office/Distributors for avallability and specifications.} \\
    \hline Supply Voltage & 7 V \\
    \hline Input Voltage & 5.5 V \\
    \hline Operating Free Air Temperature Range & \\
    \hline DM54S & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    \hline DM74S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    \hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    Recommended Operating Conditions (See Section 1 for Test Waveiorms and Output Loaid)
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54S74} & \multicolumn{3}{|c|}{DM74S74} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
    \hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -1 & & & -1 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & 110 & 75 & 0 & 110 & 75 & MHz \\
    \hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 3)} & 0 & 95 & 65 & 0 & 95 & 65 & MHz \\
    \hline \multirow[t]{4}{*}{\(t_{W}\)} & \multirow[t]{4}{*}{Pulse Width (Note 2)} & Clock High & 6 & & & 6 & & & \multirow{4}{*}{ns} \\
    \hline & & Clock Low & 7.3 & & & 7.3 & & & \\
    \hline & & Clear Low & 7 & & & 7 & & & \\
    \hline & & Preset Low & 7 & & & 7 & & & \\
    \hline \multirow[t]{4}{*}{tw} & \multirow[t]{4}{*}{Pulse Width (Note 3)} & Clock High & 8 & & & 8 & & & \multirow{4}{*}{ns} \\
    \hline & & Clock Low & 9 & & & 9 & & & \\
    \hline & & Clear Low & 9 & & & 9 & & & \\
    \hline & & Preset Low & 9 & & & 9 & & & \\
    \hline tsu & \multicolumn{2}{|l|}{Setup Time (Notes 1 \& 2)} & \(3 \uparrow\) & & & \(3 \uparrow\) & & & ns \\
    \hline tsu & \multicolumn{2}{|l|}{Setup Time (Notes 1 \& 3)} & \(3 \uparrow\) & & & \(3 \uparrow\) & & & ns \\
    \hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Input Hold Time (Notes 1 \& 2)} & \(2 \uparrow\) & & & \(2 \uparrow\) & & & ns \\
    \hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Input Hold Time (Notes 1 \& 3)} & \(2 \uparrow\) & & & \(2 \uparrow\) & & & ns \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note 1: The symbol ( \(\uparrow\) ) indicates the rising edge at the clock pulse is used for reference.
    Note 2: \(C_{L}=15 \mathrm{pF}, R_{L}=280 \Omega, T_{A}=25^{\circ} \mathrm{C}\) and \(V_{C C}=5 \mathrm{~V}\).
    Note 3: \(C_{L}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega, \mathrm{~T}_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{C C}=5 \mathrm{~V}\).

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \multirow[t]{4}{*}{\({ }_{\mathrm{I} H}\)} & \multirow[t]{4}{*}{High Level Input Current} & \multirow[t]{4}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=2.7 V
    \end{aligned}
    \]} & D & & & 50 & \multirow{4}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & Clear & & & 150 & \\
    \hline & & & Preset & & & 100 & \\
    \hline & & & Clock & & & 100 & \\
    \hline \multirow[t]{4}{*}{IIL} & \multirow[t]{4}{*}{Low Level Input Current} & \multirow[t]{4}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{I}=0.5 \mathrm{~V} \\
    & \text { (Note 4) }
    \end{aligned}
    \]} & D & & & -2 & \multirow{4}{*}{mA} \\
    \hline & & & Clear & & & -6 & \\
    \hline & & & Preset & & & -4 & \\
    \hline & & & Clock & & & -4 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICC & Supply Current & \(\mathrm{V}_{\text {CC }}=\) Max, (Note 3) & & & 30 & 50 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: With all outputs open, \(I_{\text {CC }}\) is measured with the \(Q\) and \(\bar{Q}\) outputs high in turn. At the time of measurement, the clock is grounded.
    Note 4: Clear is tested with preset high and preset is tested with clear high.
    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{\begin{tabular}{l}
    From (Input) \\
    To (Output)
    \end{tabular}} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 75 & & 65 & & MHz \\
    \hline tp'.H & Propagation Delay Time Low to High Level Output & Preset to Q & & 6 & & 9 & ns \\
    \hline \({ }_{\text {tpLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{aligned}
    & \text { Clear } \\
    & \text { to } \bar{Q}
    \end{aligned}
    \] & & 6 & & 9 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output (Clock High) & Preset to \(\bar{Q}\) & & 13.5 & & 17 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output (Clock Low) & Preset to \(\bar{Q}\) & & 8 & & 14 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output (Clock High) & \[
    \begin{gathered}
    \hline \text { Clear } \\
    \text { to } \\
    Q \\
    \hline
    \end{gathered}
    \] & & 13.5 & & 16 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output (Clock Low) & \[
    \begin{gathered}
    \text { Clear } \\
    \text { to } \\
    Q \\
    \hline
    \end{gathered}
    \] & & 8 & & 13 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to
    \[
    \mathrm{Q} \text { or } \bar{Q}
    \] & & 9 & & 12 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Q or \(\bar{Q}\) & & 9 & & 14 & ns \\
    \hline
    \end{tabular}

    \section*{DM54S86/DM74S86 Quad 2-Input Exclusive-OR Gates}

    \section*{General Description}

    This device contains four independent gates each of which performs the logic Exclusive-OR function.

    \section*{Connection Diagram}
    

    Order Number DM54S86J, DM54S86W or DM74S86N See NS Package Number J14A, N14A or W14B

    \section*{Function Table}
    \begin{tabular}{|c|c|c|}
    \hline \multicolumn{2}{|c|}{Inputs} & Output \\
    \hline A & B & Y \\
    \hline L & L & L \\
    \hline L & H & H \\
    \hline H & L & H \\
    \hline H & H & L \\
    \hline
    \end{tabular}
    \(H=\) High Logic Level
    \(L=\) Low Logic Level
    ```

    Absolute Maximum Ratings
    (Note)

    ```

    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    7 V
    Input Voltage
    Operating Free Air Temperature Range
    \begin{tabular}{lr} 
    DM54S & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S86} & \multicolumn{3}{|c|}{DM74S86} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -1 & & & -1 & mA \\
    \hline loL & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline TA & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & (\text { Note } 3)
    \end{aligned}
    \]} & & 35 & 50 & mA \\
    \hline \(\mathrm{I}_{\text {CCL }}\) & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\text { Max } \\
    & (\text { Note 4) }
    \end{aligned}
    \]} & & 50 & 75 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: I CCH is measured with all outputs open, one input of each gate at 4.5 V , and the other inputs grounded.
    Note 4: \(\mathrm{I}_{\mathrm{CCL}}\) is measured with all outputs open and all inputs grounded.
    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) to (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \multirow[t]{2}{*}{\(A\) or B to \(Y\)} & & 10.5 & & 14 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & & & 10 & & 13 & ns \\
    \hline
    \end{tabular}

    \section*{General Description}

    This device consists of two high speed, completely independent transition clocked \(\sqrt{\mathrm{K}}\) flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The \(\sqrt{K}\) design allows operation as a \(D\) flip-flop (refer to 'S74 data sheet) by connecting the \(J\) and \(\bar{K}\) inputs together.

    \section*{Connection Diagram}

    \section*{Dual-In-Line Package}
    

    Order Number DM74S109N
    See NS Package Number N16E

    \section*{Truth Table}
    \begin{tabular}{|cc|c|}
    \hline \multicolumn{2}{|c|}{ Inputs } & \multicolumn{2}{c|}{ Outputs } \\
    \hline \multicolumn{2}{|c|}{\(@ \mathbf{t}_{\mathbf{n}}\)} & \multicolumn{2}{c|}{\(@ \mathbf{t}_{\mathbf{n}}+\mathbf{1}\)} \\
    \hline J & K & \(\mathbf{Q}\) \\
    \hline L & H & \multicolumn{2}{c|}{ No Change } \\
    L & L & L \\
    H & H & H \\
    H & L & \multicolumn{2}{c|}{ Toggles } \\
    \hline
    \end{tabular}

    Asynchronous Inputs:
    LOW input to \(\bar{S}_{D}\) sets \(Q\) to HIGH level LOW input to \(\overline{\mathrm{C}}_{\mathrm{D}}\) sets Q to LOW level Clear and Set are independent of clock Simultaneous LOW on \(\overline{\mathrm{C}}_{\mathrm{D}}\) and \(\overline{\mathrm{S}}_{\mathrm{D}}\) makes both Q and \(\overline{\mathrm{Q}} \mathrm{HIGH}\)
    \(t_{n}=\) Bit time before clock pulse
    \(t_{\mathrm{n}+1}=\) Bit time after clock pulse
    H = HIGH Voltage Level
    \(L=\) LOW Voltage Level
    Logic Symbol
    

    TL/F/9802-2
    \begin{tabular}{lr} 
    Absolute Maximum Ratings (Note) \\
    If Military/Aerospace specified devices are required, \\
    please contact the National Semiconductor Sales \\
    Office/Distributors for availability and specifications. \\
    Supply Voltage & 7 V \\
    Input Voltage & 5.5 V \\
    Operating Free Air Temperature Range \\
    DM74S & \\
    Storage Temperature Range & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM74S109} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{\text {l }}\) & High Level Output Current & & & -1 & mA \\
    \hline lOL & Low Level Output Current & & & 20 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Setup Time
    \[
    J_{n} \text { or } \bar{K}_{n} \text { to } C P_{n}
    \] & \[
    \begin{aligned}
    & 6.0 \\
    & 6.0 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L)
    \end{aligned}
    \] & Hold Time \(J_{n}\) or \(\bar{K}_{n}\) to \(C P_{n}\) & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{w}(H) \\
    & t_{w}(L)
    \end{aligned}
    \] & \(\mathrm{CP}_{\mathrm{n}}\) Pulse Width & \[
    \begin{aligned}
    & 7.0 \\
    & 6.5 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \(t_{w}(L)\) & \(\overline{\mathrm{C}}_{\text {Dn }}\) or \(\bar{S}_{\text {Dn }}\) Pulse Width LOW & 6.0 & & & ns \\
    \hline
    \end{tabular}

    \section*{Electrical Characteristics}

    Over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & \begin{tabular}{l}
    Typ \\
    (Note 1)
    \end{tabular} & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\) & & & -1.2 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \] & 2.7 & 3.4 & & V \\
    \hline Vol & Low Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \] & & 0.35 & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\) & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\) & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\) & & & -2.0 & mA \\
    \hline los & Short Circuit Output Current & \[
    \begin{aligned}
    & V_{\mathrm{CC}}=\text { Max } \\
    & \text { (Note 2) }
    \end{aligned}
    \] & -40 & & -100 & mA \\
    \hline Icc & Supply Current & \[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{CP}}=0 \mathrm{~V}
    \end{aligned}
    \] & & & 52 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    Switching Characteristics
    \(V_{C C}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\[
    \begin{aligned}
    & C_{L}=15 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=280 \Omega
    \end{aligned}
    \]} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \(\mathrm{f}_{\max }\) & Maximum Clock Frequency & 75 & & MHz \\
    \hline \[
    t_{\text {PLH }}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & Propagation Delay \(C P_{n}\) to \(Q_{n}\) or \(\bar{Q}_{n}\) & & \[
    \begin{aligned}
    & 9.0 \\
    & 11 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(\mathrm{t}_{\mathrm{PHL}}\)
    \end{tabular} & Propagation Delay \(\bar{C}_{D n}\) or \(\bar{S}_{D n}\) to \(Q_{n}\) or \(\bar{Q}_{n}\) & & \[
    \begin{aligned}
    & 6.0 \\
    & 11
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Logic Diagram (one hall shown)
    

    \title{
    DM54S112/DM74S112 Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset, Clear, and Complementary Outputs
    }

    \section*{General Description}

    This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. Data on the J and K
    inputs can be changed while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

    \section*{Connection Diagram}

    Dual-In-Line Package
    

    TL/F/6459-1
    Order Number DM54S112J or DM74S112N See NS Package Number J16A or N16E

    Function Table
    \begin{tabular}{|c|c|c|c|c|cc|}
    \hline \multicolumn{6}{|c|}{ Inputs } & \multicolumn{2}{c|}{ Outputs } \\
    \hline PR & CLR & CLK & J & K & Q & \(\overline{\mathbf{Q}}\) \\
    \hline L & \(H\) & X & X & X & \(H\) & L \\
    \(H\) & L & X & X & X & L & \(H\) \\
    L & L & X & X & X & \(H^{*}\) & \(H^{*}\) \\
    \(H\) & \(H\) & \(\downarrow\) & L & L & \(Q_{0}\) & \(\bar{Q}_{0}\) \\
    \(H\) & \(H\) & \(\downarrow\) & \(H\) & L & \(H\) & L \\
    \(H\) & \(H\) & \(\downarrow\) & L & \(H\) & L & \(H\) \\
    \(H\) & \(H\) & \(\downarrow\) & \(H\) & \(H\) & \multicolumn{2}{|c|}{ Toggle } \\
    \(H\) & \(H\) & \(H\) & \(X\) & \(X\) & \(Q_{0}\) & \(\bar{Q}_{0}\) \\
    \hline
    \end{tabular}

    \footnotetext{
    \(\mathrm{H}=\) High Logic Level
    }
    \(X=\) Either Low or High Logic Level
    \(\mathrm{L}=\) Low Logic Level
    \(\downarrow=\) Negative going edge of pulse.
    \(Q_{0}=\) The output logic level of \(Q\) before the indicated input conditions were established.
    * = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to its inactive (high) level.
    Toggle \(=\) Each output changes to the complement of its previous level on each falling edge of the clock pulse.
    \begin{tabular}{lr} 
    Absolute Maximum Ratings (Note) \\
    If Milltary/Aerospace specified devices are required, \\
    please contact the National Semiconductor Sales \\
    Office/Distributors for avallability and specifications. \\
    Supply Voltage & 7 V \\
    Input Voltage & 5.5 V \\
    Operating Free Air Temperature Range & \\
    DM54S & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54S112} & \multicolumn{3}{|c|}{DM74S112} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{\text {CC }}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
    \hline \(\mathrm{lOH}^{2}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -1 & & & -1 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 20 & & & 20 & mA \\
    \hline \({ }_{\text {f CLK }}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & 125 & 80 & 0 & 125 & 80 & MHz \\
    \hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 3)} & 0 & 80 & 60 & 0 & 80 & 60 & MHz \\
    \hline \multirow[t]{4}{*}{tw} & \multirow[t]{4}{*}{Pulse Width (Note 2)} & Clock High & 6 & & & 6 & & & \multirow{4}{*}{ns} \\
    \hline & & Clock Low & 6.5 & & & 6.5 & & & \\
    \hline & & Clear Low & 8 & & & 8 & & & \\
    \hline & & Preset Low & 8 & & & 8 & & & \\
    \hline \multirow[t]{4}{*}{tw} & \multirow[t]{4}{*}{Pulse Width (Note 3)} & Clock High & 8 & & & 8 & & & \multirow{4}{*}{ns} \\
    \hline & & Clock Low & 8 & & & 8 & & & \\
    \hline & & Clear Low & 10 & & & 10 & & & \\
    \hline & & Preset Low & 10 & & & 10 & & & \\
    \hline tsu & \multicolumn{2}{|l|}{Setup Time (Notes 1 \& 4)} & \(7 \downarrow\) & & & \(7 \downarrow\) & & & ns \\
    \hline \(t_{H}\) & \multicolumn{2}{|l|}{Input Hold Time (Notes 1 \& 4)} & 0 \(\downarrow\) & & & 0 \(\downarrow\) & & & ns \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note 1: The symbol \((\downarrow)\) indicates the falling edge at the clock pulse is used for reference.
    Note 2: \(C_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 3: \(C_{L}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega, \mathrm{~T}_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{C C}=5 \mathrm{~V}\).
    Note 4: \(T_{A}=25^{\circ} \mathrm{C}\) and \(V_{C C}=5 \mathrm{~V}\).

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, l_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\
    & V_{I L}=M a x, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \multirow[t]{4}{*}{\({ }_{1 / \mathrm{H}}\)} & \multirow[t]{4}{*}{High Level Input Current} & \multirow[t]{4}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=2.7 V
    \end{aligned}
    \]} & J, K & & & 50 & \multirow{4}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & Clear & & & 100 & \\
    \hline & & & Preset & & & 100 & \\
    \hline & & & Clock & & & 100 & \\
    \hline \multirow[t]{4}{*}{IIL} & \multirow[t]{4}{*}{Low Level Input Current} & \multirow[t]{4}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=0.5 \mathrm{~V} \\
    & (\text { Note } 4)
    \end{aligned}
    \]} & J, K & & & -1.6 & \multirow{4}{*}{mA} \\
    \hline & & & Clear & & & -7 & \\
    \hline & & & Preset & & & -7 & \\
    \hline & & & Clock & & & -4 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 3)} & & 30 & 50 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: With all outputs open, ICC is measured with the \(Q\) and \(\overline{\mathrm{Q}}\) outputs high in turn. At the time of measurement, the clock input is grounded.
    Note 4: Clear is tested with preset high and preset is tested with clear high.
    Switching CharacteristicS at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 80 & & 60 & & MHz \\
    \hline \({ }_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output & Preset to Q & & 7 & & 9 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Preset to \(\bar{Q}\) & & 7 & & 12 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{aligned}
    & \text { Clear } \\
    & \text { to } \bar{Q}
    \end{aligned}
    \] & & 7 & & 9 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{aligned}
    & \text { Clear } \\
    & \text { to } \mathrm{Q}
    \end{aligned}
    \] & & 7 & & 12 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Q or \(\overline{\mathrm{Q}}\) & & 7 & & 9 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Q or \(\bar{Q}\) & & 7 & & 12 & ns \\
    \hline
    \end{tabular}

    \section*{DM54S113/DM74S113 Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset and Complementary Outputs}

    \section*{General Description}

    This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the
    negative going edge of the clock pulse. Data on the J and K inputs may be changed while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset input will set the outputs regardless of the logic levels of the other inputs.

    \section*{Connection Diagram}

    \section*{Dual-In-Line Package}
    

    \section*{Function Table}
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multicolumn{4}{|c|}{Inputs} & \multicolumn{2}{|c|}{Outputs} \\
    \hline PR & CLK & J & K & Q & \(\overline{\mathbf{Q}}\) \\
    \hline L & X & X & X & H & L \\
    \hline H & \(\downarrow\) & L & L & \(Q_{0}\) & \(\bar{Q}_{0}\) \\
    \hline H & \(\downarrow\) & H & L & H & L \\
    \hline H & \(\downarrow\) & L & H & L & H \\
    \hline H & \(\downarrow\) & H & H & & \\
    \hline H & H & X & X & \(Q_{0}\) & \(\bar{Q}_{0}\) \\
    \hline
    \end{tabular}
    \(H=\) High Logic Level
    \(X=\) Either Low or High Logic Level
    \(\mathrm{L}=\) Low Logic Level
    \(\downarrow=\) Negative going edge of pulse.
    \(Q_{0}=\) The output logic level of \(Q\) before the indicated input conditions were established.
    Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.
    \begin{tabular}{|c|c|c|}
    \hline \multicolumn{3}{|l|}{Absolute Maximum Ratings (Note)} \\
    \hline If Military/Aerospace specified devi please contact the National Sem Office/Distributors for availability and & ces are required, iconductor Sales d specifications. & Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The \\
    \hline Supply Voltage & 7 V & parametric values defined in the "Electrical Characteristics" \\
    \hline input Voltage & 5.5 V & table are not guaranteed at the absolute maximum ratings. \\
    \hline Operating Free Air Temperature Range & & the conditions for actual device operation. \\
    \hline \begin{tabular}{l}
    DM54S \\
    DM74S
    \end{tabular} & \[
    \begin{array}{r}
    -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\
    0^{\circ} \mathrm{C} \text { to }+70^{\circ} \mathrm{C}
    \end{array}
    \] & \\
    \hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) & \\
    \hline
    \end{tabular}

    Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54S113} & \multicolumn{3}{|c|}{DM74S113} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
    \hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -1 & & & -1 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & 125 & 80 & 0 & 125 & 80 & MHz \\
    \hline \(\mathrm{f}_{\text {CLK }}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 3)} & 0 & 80 & 60 & 0 & 80 & 60 & MHz \\
    \hline \multirow[t]{3}{*}{tw} & \multirow[t]{3}{*}{Pulse Width (Note 2)} & Clock High & 6 & & & 6 & & & \multirow{3}{*}{ns} \\
    \hline & & Clock Low & 6.5 & & & 6.5 & & & \\
    \hline & & Preset Low & 8 & & & 8 & & & \\
    \hline \multirow[t]{3}{*}{\({ }^{\text {tw }}\)} & \multirow[t]{3}{*}{Pulse Width (Note 3)} & Clock High & 8 & & & 8 & & & \multirow{3}{*}{\(n \mathrm{~s}\)} \\
    \hline & & Clock Low & 8 & & & 8 & & & \\
    \hline & & Preset Low & 10 & & & 10 & & & \\
    \hline tsu & \multicolumn{2}{|l|}{Setup Time (Notes 1 \& 4)} & \(7 \downarrow\) & & & 7 \(\downarrow\) & & & ns \\
    \hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Input Hold Time (Notes 1 \& 4)} & 0 \(\downarrow\) & & & 0】 & & & ns \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note 1: The symbol \((\downarrow)\) indicates the falling edge at the clock pulse is used for reference.
    Note 2: \(C_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega, \mathrm{~T}_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{C C}=5 \mathrm{~V}\).
    Note 3: \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 4: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=5.5 \mathrm{~V}\)} & & - & 1 & mA \\
    \hline \multirow[t]{3}{*}{IIH} & \multirow[t]{3}{*}{High Level Input Current} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=2.7 V
    \end{aligned}
    \]} & J, K & & & 50 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & Preset & & & 100 & \\
    \hline & & & Clock & & & 100 & \\
    \hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=0.5 V
    \end{aligned}
    \]} & J, K & & & -1.6 & \multirow{3}{*}{mA} \\
    \hline & & & Preset & & & -7 & \\
    \hline & & & Clock & & & -4 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=M a x
    \] \\
    (Note 2)
    \end{tabular}} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max},(\) Note 3)} & & 30 & 50 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: With all outputs open, ICC is measured with the \(Q\) and \(\bar{Q}\) outputs high in turn. At the time of measurement, the clock input is grounded.
    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|r|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 80 & & 60 & & MHz \\
    \hline \({ }_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output & Preset to Q & & 7 & & 9 & ns \\
    \hline tPHL & Propagation Delay Time High to Low Level Output & Preset to \(\bar{Q}\) & & 7 & & 12 & ns \\
    \hline tplH & Propagation Delay Time Low to High Level Output & Clock to Q or \(\bar{Q}\) & & 7 & & 9 & ns \\
    \hline tpHL & Propagation Delay Time High to Low Level Output & Clock to Q or \(\bar{Q}\) & & 7 & & 12 & ns \\
    \hline
    \end{tabular}

    \section*{Quad 2-Input Schmitt Trigger NAND Gate}

    \section*{General Description}

    This device contains four independent gates that perform the logic NAND function. Each gate has two inputs that are Schmitt Triggers.

    \section*{Connection Diagram}
    

    TL/F/9803-1
    Order Number DM74S132N
    See NS Package Number N14A
    \begin{tabular}{l} 
    Absolute Maximum Ratings (Note) \\
    If Military/Aerospace specified devices are required, \\
    please contact the National Semiconductor Sales \\
    Office/Distributors for availability and specifications. \\
    Supply Voltage \\
    Input Voltage \\
    Operating Free Air Temperature Range \\
    DM74S \\
    Storage Temperature Range \\
    \hline
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for acutal device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM74S132} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -1 & mA \\
    \hline loL & Low Level Output Current & & & 20 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \(\mathrm{V}_{\mathrm{T}+}\) & Positive-Going Threshold Voltage & 1.6 & & 1.9 & V \\
    \hline \(\mathrm{V}_{\mathrm{T}-}\) & Negative-Going Threshold Voltage & 1.1 & & 1.4 & V \\
    \hline \(\mathrm{V}_{\mathrm{T}+}-\mathrm{V}_{\mathrm{T}-}\) & Hysteresis Voltage & 0.2 & & & V \\
    \hline \(\mathrm{I}_{\mathrm{T}+}\) & Input Current at PositiveGoing Threshold & -0.9** & & & mA \\
    \hline \(\mathrm{I}_{\mathrm{T} \text { - }}\) & Input Current at NegativeGoing Threshold & -1.1** & & & mA \\
    \hline
    \end{tabular}
    *DC limits apply over operating temperature range; \(A C\) limits apply at \(T_{A}=+25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}\). \(\quad\) **Typical Value.
    Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) } \\
    \hline
    \end{gathered}
    \] & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\) & & & -1.2 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \] & 2.7 & 3.4 & & V \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
    \begin{aligned}
    & V_{C C}=\text { Min, } I_{O L}=M a x \\
    & V_{I H}=M i n
    \end{aligned}
    \] & & 0.35 & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\) & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \(\mathrm{V}_{C C}=\operatorname{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\) & & & -2.0 & mA \\
    \hline los & Short Circuit Output Current & \[
    \begin{aligned}
    & V_{\mathrm{CC}}=M a x \\
    & \text { (Note 2) } \\
    & \hline
    \end{aligned}
    \] & -40 & & -100 & mA \\
    \hline ICCH & Supply Current with Outputs High & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) & & & 44 & mA \\
    \hline \({ }^{\text {ICCL }}\) & Supply Current with Outputs Low & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) & & & 68 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    Switching Characteristics \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{2}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \\
    \hline & & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & & 10.5 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & & 13 & ns \\
    \hline
    \end{tabular}

    \section*{DM54S133/DM74S133 13-Input NAND Gate}

    \section*{General Description}

    This device contains a single gate which performs the logic NAND function.

    \section*{Connection Diagram}
    

    \section*{Function Table}
    \(\mathbf{Y}=\overline{\text { ABCDEFGHIJKLM }}\)
    \begin{tabular}{|c|c|}
    \hline Inputs & Output \\
    \hline A thru M & \(\mathbf{Y}\) \\
    \hline All Inputs H & L \\
    One or More & H \\
    Input L & \\
    \hline
    \end{tabular}
    \(\mathrm{H}=\) High Logic Level
    L = Low Logic Level
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{9}{|l|}{Absolute Maximum Ratings (Note)} \\
    \hline \multicolumn{3}{|l|}{If Military/Aerospace specified devices are required please contact the National Semiconductor Sale Office/Distributors for avallability and specifications.} & \multicolumn{6}{|l|}{Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The} \\
    \hline \multicolumn{2}{|l|}{Supply Voltage} & 7 & \multicolumn{6}{|l|}{\multirow[t]{2}{*}{parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define}} \\
    \hline \multicolumn{2}{|l|}{Input Voltage} & 5.5 V & & & & & & \\
    \hline \multicolumn{2}{|l|}{Operating Free Air Temperature Range DM54S} & \[
    \begin{aligned}
    & -125^{\circ} \\
    & +70^{\circ}
    \end{aligned}
    \] & \multicolumn{6}{|l|}{the conditions for actual device operation.} \\
    \hline \multicolumn{2}{|l|}{Storage Temperature Range} & \(150^{\circ} \mathrm{C}\) & & & & & & \\
    \hline \multicolumn{9}{|l|}{Recommended Operating Conditions} \\
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S133} & \multicolumn{3}{|c|}{DM74S133} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{1 \mathrm{H}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline lOH & High Level Output Current & & & -1 & & & -1 & mA \\
    \hline \(\mathrm{IOL}^{\text {l }}\) & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \begin{tabular}{l}
    Typ \\
    (Note 1)
    \end{tabular} & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
    & V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & 3 & 5 & mA \\
    \hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & 5.5 & 10 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(R_{L}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & 2 & 6 & 2 & 8 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & 2 & 7 & 3 & 10 & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{DM54S138/DM74S138, DM54S139/DM74S139 Decoders/Demultiplexers}

    \section*{General Description}

    These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.
    The S138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24 -line decoder can be implemented with no external inverters, and a 32 -line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.
    The S139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.
    All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

    \section*{Features}

    ■ Designed specifically for high speed:
    Memory decoders
    Data transmission systems
    - S138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
    - S139 contains two fully independent 2-to-4-line decoders/demultiplexers
    - Schottky clamped for high performance
    - Typical propagation delay time (3 levels of logic)

    S138 8 ns S139 7.5 ns
    - Typical power dissipation

    S138 245 mW
    S139 300 mW

    \section*{Connection Diagrams}
    

    TL/F/6466-1
    \begin{tabular}{l} 
    Absolute Maximum Ratings (Note) \\
    If Military/Aerospace specified devices are required, \\
    please contact the National Semiconductor Sales \\
    Office/Distributors for availability and specifications. \\
    Supply Voltage \\
    Input Voltage \\
    Operating Free Air Temperature Range \\
    DM54S \\
    DM74S \\
    Storage Temperature Range \\
    \hline
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    Recommended Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S138,S139} & \multicolumn{3}{|c|}{DM74S138,S139} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -1 & & & -1 & mA \\
    \hline \(\mathrm{lOL}_{\mathrm{OL}}\) & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline ILL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=\operatorname{Max}
    \] \\
    (Note 2)
    \end{tabular}} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICC & Supply Current (S138) & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}\) (Note 3)} & & 49 & 74 & mA \\
    \hline ICC & Supply Current (S139) & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\operatorname{Max}\) (Note 3)} & & 60 & 90 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: ICC is measured with all outputs enabled and open.

    \section*{'S138 Switching Characteristics}
    at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{\begin{tabular}{l}
    From \\
    (Input) to (Output)
    \end{tabular}} & \multirow{3}{*}{Levels of Delay} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & & \multicolumn{2}{|l|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Select to Output & 2 & & 7 & & 9 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Select to Output & 2 & & 10.5 & & 14 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Select to Output & 3 & & 12 & & 14 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Select to Output & 3 & & 12 & & 15 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Enable to Output & 2 & & 8 & & 10 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Enable to Output & 2 & & 11 & & 14 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Enable to Output & 3 & & 11 & & 13 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Enable to Output & 3 & & 11 & & 14 & ns \\
    \hline
    \end{tabular}

    \section*{'S139 Switching Characteristics}
    at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) to (Output)} & \multirow{3}{*}{Levels of Delay} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Select to Output & 2 & & 7.5 & & 10 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Select to Output & 2 & & 10 & & 13 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Select to Output & 3 & & 12 & & 13 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Select to Output & 3 & & 12 & & 15 & ns \\
    \hline tply & Propagation Delay Time Low to High Level Output & Enable to Output & 2 & & 8 & & 10 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Enable to Output & 2 & & 10 & & 13 & ns \\
    \hline
    \end{tabular}

    \section*{Function Tables}

    S138
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{5}{|c|}{Inputs} & \multicolumn{8}{|c|}{\multirow[t]{2}{*}{Outputs}} \\
    \hline \multicolumn{2}{|l|}{Enable} & \multicolumn{3}{|r|}{Select} & & & & & & & & \\
    \hline G1 & G2* & C & B & A & Y0 & Y1 & Y2 & Y3 & Y4 & Y5 & Y6 & Y7 \\
    \hline X & H & X & \(X\) & X & H & H & H & H & H & H & H & H \\
    \hline L & X & X & X & X & H & H & H & H & H & H & H & H \\
    \hline H & L & L & L & L & L & H & H & H & H & H & H & H \\
    \hline H & L & L & L & H & H & L & H & H & H & H & H & H \\
    \hline H & L & L & H & L & H & H & L & H & H & H & H & H \\
    \hline H & L & L & H & H & H & H & H & L & H & H & H & H \\
    \hline H & L & H & L & L & H & H & H & H & L & H & H & H \\
    \hline H & \(L\) & H & L & H & H & H & H & H & H & L & H & H \\
    \hline H & L & H & H & L & H & H & H & H & H & H & L & H \\
    \hline H & L & H & H & H & H & H & H & H & H & H & H & L \\
    \hline
    \end{tabular}
    * \(\mathrm{G} 2=\mathrm{G} 2 \mathrm{~A}+\mathrm{G} 2 \mathrm{~B}\)
    \(H=\) high level, \(L=\) low level, \(X=\) don't care (either low or high logic level)

    \section*{Logic Diagrams}
    

    \section*{DM54S140/DM74S140 \\ Dual 4-Input NAND \(50 \Omega\) Line Driver}

    \section*{General Description}

    This device contains two independent line driver gates each of which performs the logic NAND function.

    \section*{Connection Diagram}
    

    TL/F/6467-1
    Order Number DM54S140J or DM74S140N See NS Package Number J14A or N14A

    Function Table
    \[
    \mathbf{Y}=\overline{\mathbf{A B C D}}
    \]
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multicolumn{5}{|c|}{ Inputs } \\
    \hline A & B & C & D & Y \\
    \hline X & X & X & L & H \\
    X & X & L & X & H \\
    X & L & X & X & H \\
    L & X & X & X & H \\
    H & H & H & H & L \\
    \hline
    \end{tabular}

    H = High Logic Level
    L = Low Logic Level
    \(X=\) Either Low or High Logic Level

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    \begin{tabular}{lr} 
    Supply Voltage & 7 V \\
    Input Voltage & 5.5 V \\
    Operating Free Air Temperature Range & \\
    DM54S & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S140} & \multicolumn{3}{|c|}{DM74S140} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -3 & & & -3 & mA \\
    \hline lOL & Low Level Output Current & & & 60 & & & 60 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{3}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, V_{\mathrm{IL}}=\operatorname{Max} \\
    & \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{3}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline & & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{IL}}=0.5 \mathrm{~V}, \mathrm{R}_{\mathrm{O}}=50 \Omega\) to GND} & 2.0 & & & \\
    \hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\)} & & & 100 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}_{1} \mathrm{~V}_{1}=0.5 \mathrm{~V}\)} & & & -4 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & (\text { Note } 2)
    \end{aligned}
    \]} & DM54 & \(-50\) & & -225 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -50 & & -225 & \\
    \hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & 10 & 18 & mA \\
    \hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\)} & & 25 & 44 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=93 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=150 \mathrm{pF}\)} & \\
    \hline & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & 2 & 6.5 & 3 & 9 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & 2 & 6.5 & 3 & 9 & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{DM54S151/DM74S151 1-of-8 Data Selector/Multiplexer with Complementary Outputs}

    \section*{General Description}

    These data selectors/multiplexers contain full on-chip decoding to select the desired data source. The 'S151 selects one-of-eight data sources. The 'S151 has a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the \(W\) output high and the \(Y\) output low.
    The 'S151 features complementary W and Y outputs.

    \section*{Features}

    ■ Select one-of-eight data lines
    - Performs parallel-to-serial conversion
    - Permits multiplexing from N lines to one line
    - Also for use as Boolean function generator

    ■ Typical average propagation delay time, data input to W output 4.5 ns
    - Typical power dissipation 225 mW

    \section*{Connection Diagram}
    

    TL/F/6468-1
    Order Number DM54S151J, DM54S151W or DM74S151N See NS Package Number J16A, N16E or W16A

    \section*{Function Table}
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multicolumn{4}{|c|}{Inputs} & \multicolumn{2}{|c|}{Outputs} \\
    \hline \multicolumn{3}{|c|}{Select} & \multirow[t]{2}{*}{Strobe S} & \multirow{2}{*}{Y} & \multirow{2}{*}{W} \\
    \hline C & B & A & & & \\
    \hline X & X & X & H & L & H \\
    \hline L & L & L & L & DO & \(\overline{\text { DO }}\) \\
    \hline L & L & H & L & D1 & \(\overline{\mathrm{D} 1}\) \\
    \hline L & H & L & L & D2 & \(\overline{\mathrm{D} 2}\) \\
    \hline L & H & H & L & D3 & \(\overline{\mathrm{D} 3}\) \\
    \hline H & L & L & L & D4 & \(\overline{\text { D4 }}\) \\
    \hline H & L & H & L & D5 & \(\overline{\mathrm{D} 5}\) \\
    \hline H & H & L & L & D6 & \(\overline{\text { D6 }}\) \\
    \hline H & H & H & L & D7 & \(\overline{\text { D7 }}\) \\
    \hline
    \end{tabular}

    \footnotetext{
    \(H=\) high level, \(L=\) low level, \(X=\) don't care
    D0, D1 . . D7 = the level of the respective D input
    }

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    DM54S
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    Storage Temperature Range

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S151} & \multicolumn{3}{|c|}{DM74S151} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -1 & & & -1 & mA \\
    \hline loL & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Condlitions & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\) & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, I_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & 2.5 & 3.4 & & \\
    \hline & & & 2.7 & 3.4 & & \\
    \hline VOL & Low Level Output Voltage & \[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\
    & V_{I H}=M i n, V_{I L}=\operatorname{Max}
    \end{aligned}
    \] & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \(V_{C C}=\) Max, \(V_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
    \hline 1 H & High Level Input Current & \(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\) & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\) & & & -2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\text { Max } \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & \(-40\) & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & -40 & & -100 & \\
    \hline ICC & Supply Current & \(\mathrm{V}_{C C}=\operatorname{Max}(\) Note 3) & & 45 & 70 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: \(I_{C C}\) is measured with the strobe and data select inputs at 4.5 V , all other inputs and outputs open.

    Switching Characteristics at \(\mathrm{V}_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & \begin{tabular}{l}
    Select to \(Y\) \\
    (4 Levels)
    \end{tabular} & & 18 & & 21 & ns \\
    \hline tPHL & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
    Select to \(Y\) \\
    (4 Levels)
    \end{tabular} & & 18 & & 21 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Select to W (3 Levels) & & 15 & & 18 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
    Select to W \\
    (3 Levels)
    \end{tabular} & & 13.5 & & 17 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Strobe to \(Y\) & & 16.5 & & 19 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Strobe to \(Y\) & & 18 & & 21 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \begin{tabular}{l}
    Strobe \\
    to W
    \end{tabular} & & 13 & & 16 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
    Strobe \\
    to W
    \end{tabular} & & 12 & & 16 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{aligned}
    & \text { D0 thru D7 } \\
    & \text { to } Y
    \end{aligned}
    \] & & 12 & & 15 & ns \\
    \hline tPHL & Propagation Delay Time High to Low Level Output & \[
    \begin{aligned}
    & \text { D0 thru D7 } \\
    & \text { to } Y
    \end{aligned}
    \] & & 12 & & 15 & ns \\
    \hline tple & Propagation Delay Time Low to High Level Output & \[
    \begin{aligned}
    & \text { D0 thru D7 } \\
    & \text { to W }
    \end{aligned}
    \] & & 7 & & 9 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{aligned}
    & \text { D0 thru D7 } \\
    & \text { to W }
    \end{aligned}
    \] & & 7 & & 10 & ns \\
    \hline
    \end{tabular}
    

    TL/F/6468-2

    \section*{DM54S153/DM74S153 Dual 1 of 4 Line Data} Selectors/Multiplexers

    \section*{General Description}

    Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

    \section*{Features}
    - Permits multiplexing from \(N\) lines to 1 line
    - Performs parallel-to-serial conversion

    ■ Strobe (enable) line provided for cascading ( N lines to \(n\) lines)
    - High fan-out, low-impedance, totem-pole outputs
    - Typical average propagation delay times

    From data 6 ns
    From strobe 9.5 ns
    From select 12 ns
    - Typical power dissipation 225 mW

    \section*{Logic and Connection Diagrams}
    

    \section*{Function Table}

    TL/F/6469-1
    
    \begin{tabular}{|c|c|}
    \hline \multicolumn{2}{|l|}{Absolute Maximum Ratings (Note)} \\
    \hline If Military/Aerospace specified dev please contact the National Sem Office/Distributors for availability an & ces are required, conductor Sales specifications. \\
    \hline Supply Voltage & 7 V \\
    \hline Input Voltage & 5.5 V \\
    \hline Operating Free Air Temperature Range & \\
    \hline DM54S & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    \hline DM74S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    \hline Storage Temperture Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S153} & \multicolumn{3}{|c|}{DM74S153} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(V_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -1 & & & -1 & mA \\
    \hline loL & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, \mathrm{IOL}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, \mathrm{V}_{\mathrm{I}}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, V_{1}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=M a x
    \] \\
    (Note 2)
    \end{tabular}} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}(\) Note 3)} & & 45 & 70 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: ICC is measured with all outputs open and all inputs grounded.

    Switching Characteristics at \(\mathrm{V}_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{\begin{tabular}{l}
    From (Input) \\
    To (Output)
    \end{tabular}} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|r|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & Data to \(Y\) & & 9 & & 12 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to \(Y\) & & 9 & & 12 & ns \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & Select to \(Y\) & & 18 & & 20 & ns \\
    \hline tphL & Propagation Delay Time High to Low Level Output & Select to \(Y\) & & 18 & & 21 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagtion Delay Time Low to High Level Output & Strobe to \(Y\) & & 15 & & 18 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Strobe to \(Y\) & & 13.5 & & 17 & ns \\
    \hline
    \end{tabular}

    \section*{DM54S157/DM74S157, DM54S158/DM74S158 Quad 1 of 2 Line Data Selectors/Multiplexers}

    \section*{General Description}

    These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The S157 presents true data whereas the S158 presents inverted data to minimize propagation delay time.

    \section*{Applications}
    - Expand any data input point
    - Multiplex dual data buses
    - Generate four functions of two variables (one variable is common)
    - Source programmable counters

    Connection Diagrams (Dual-In-Line Packages)

    See NS Package Number J16A, N16E or W16A
    

    TL/F/6470-1
    Order Number DM54S157J, DM54S157W or DM74S157N

    \section*{Features}
    - Buffered inputs and outputs
    - Typical propagation time S157 5 ns S158 4 ns
    - Typical power dissipation

    S157 250 mW S158 195 mW
    

    TL/F/6470-2
    Order Number DM54S158J, DM54S158W or DM74S158N See NS Package Number J16A, N16E or W16A

    Function Table
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multicolumn{4}{|c|}{ Inputs } & \multicolumn{2}{c|}{ Output Y } \\
    \hline Strobe & Select & A & B & S157 & S158 \\
    \hline H & X & X & X & L & H \\
    L & L & L & X & L & H \\
    L & L & H & X & H & L \\
    L & H & X & L & L & H \\
    L & H & X & H & H & L \\
    \hline
    \end{tabular}

    H = High Level, L = Low Level, X = Don't Care

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    5.5 V

    Operating Free Air Temperature Range
    \begin{tabular}{lr} 
    DM54S & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended' Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S157} & \multicolumn{3}{|c|}{DM74S157} & \multirow{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline VIL & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -1 & & & -1 & mA \\
    \hline loL & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    \section*{'S157 Electrical Characteristics}
    over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \begin{tabular}{l}
    Typ \\
    (Note 1)
    \end{tabular} & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min} \\
    & \mathrm{l}_{\mathrm{OH}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \\
    \hline & & & DM74 & 2.7 & 3.4 & & V \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \multirow[t]{2}{*}{\(\mathrm{IIH}^{\text {H}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{I}=2.7 V
    \end{aligned}
    \]} & S or G & & & 100 & \multirow{2}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & A or B & & & 50 & \\
    \hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max} \\
    & V_{1}=0.5 V
    \end{aligned}
    \]} & S or G & & & -4 & \multirow[t]{2}{*}{mA} \\
    \hline & & & A or B & & & -2 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -40 & & -100 & \multirow{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 3) }
    \end{aligned}
    \]} & & 50 & 78 & mA \\
    \hline
    \end{tabular}

    \footnotetext{
    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: \(\mathrm{I}_{\mathrm{CC}}\) is measured 4.5 V applied to all inputs and all outputs open.
    }
    'S157 Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\)
    (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{\begin{tabular}{l}
    From \\
    (Input) To (Output)
    \end{tabular}} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    \text { Data } \\
    \text { to } \\
    Y \\
    \hline
    \end{gathered}
    \] & & 7.5 & & 10 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \text { Data } \\
    \text { to } \\
    Y \\
    \hline
    \end{gathered}
    \] & & 6.5 & & 10 & ns \\
    \hline \(t_{\text {PLH }}\) & \begin{tabular}{l}
    Propagation Delay \\
    Time Low to High \\
    Level Output
    \end{tabular} & Strobe to Y & & 12.5 & & 15 & ns \\
    \hline \(t_{\text {PHL }}\) & \begin{tabular}{l}
    Propagation Delay \\
    Time High to Low \\
    Level Output
    \end{tabular} & Strobe to Y & & 12 & & 15 & ns \\
    \hline \(t_{\text {PLH }}\) & \begin{tabular}{l}
    Propagation Delay \\
    Time Low to High \\
    Level Output
    \end{tabular} & Select to Y & & 15 & & 17 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Select to Y & & 15 & & 17 & ns \\
    \hline
    \end{tabular}

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S158} & \multicolumn{3}{|c|}{DM74S158} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -1 & & & -1 & mA \\
    \hline lol & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    \section*{'S158 Electrical Characteristics}
    over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min} \\
    & l_{\mathrm{OH}}=\operatorname{Max} \\
    & V_{\mathrm{IL}}=\operatorname{Max} \\
    & V_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \\
    \hline & & & DM74 & 2.7 & 3.4 & & V \\
    \hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \multirow[t]{2}{*}{\(\mathrm{IIH}^{\text {H }}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{I}=2.7 V
    \end{aligned}
    \]} & S or G & & & 100 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & A or B & & & 50 & \\
    \hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=0.5 V
    \end{aligned}
    \]} & S or G & & & -4 & \multirow[t]{2}{*}{mA} \\
    \hline & & & A or B & & & -2 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Max} \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & DM54 & \(-40\) & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICC1 & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\operatorname{Max}\) (Note 3)} & & 39 & 61 & mA \\
    \hline ICC2 & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 4)} & & & 81 & mA \\
    \hline
    \end{tabular}
    'S158 Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\)
    (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{\begin{tabular}{l}
    From \\
    (Input) To (Output)
    \end{tabular}} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|c|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & \begin{tabular}{l}
    Propagation Delay \\
    Time Low to High \\
    Level Output
    \end{tabular} & Data to Y & & 6 & & 9 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to Y & & 6 & & 9 & ns \\
    \hline \(t_{\text {PLH }}\) & \begin{tabular}{l}
    Propagation Delay \\
    Time Low to High Level Output
    \end{tabular} & Strobe to Y & & 11.5 & & 12 & ns \\
    \hline \(t_{\text {PHL }}\) & \begin{tabular}{l}
    Propagation Delay \\
    Time High to Low \\
    Level Output
    \end{tabular} & Strobe to Y & & 12 & & 14 & ns \\
    \hline \(t_{\text {PLH }}\) & \begin{tabular}{l}
    Propagation Delay \\
    Time Low to High \\
    Level Output
    \end{tabular} & Select to Y & & 12 & & 15 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & \begin{tabular}{l}
    Propagation Delay \\
    Time High to Low Level Output
    \end{tabular} & Select to Y & & 12 & & 15 & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: \(\mathrm{I}_{\mathrm{CC} 1}\) is measured with all outputs open and all inputs at 4.5 V .
    Note 4: ICC2 is measured with B, G, and S inputs grounded, A inputs at 4.5 V , and all outputs open.
    

    S158
    

    TL/F/6470-4

    National Semiconductor

    \section*{DM54S161/DM74S161, DM54S163/DM74S163 Synchronous 4-Bit Binary Counters}

    \section*{General Description}

    These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. They are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.
    These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input.

    The carry look-ahead circuitry provides for cascading counters for \(n\)-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both countenable inputs ( \(P\) and \(T\) ) must be high to count, and input \(T\) is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the \(Q_{A}\) output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages.

    \section*{Features}
    - Synchronously programmable
    - Internal look-ahead for fast counting
    - Carry output for \(n\)-bit cascading
    - Synchronous counting
    - Load control line
    - Diode-clamped inputs

    \section*{Connection Diagram}
    

    TL/F/6471-1
    Order Number DM54S161J, DM54S163J, DM54S161W, DM74S161N, or DM74S163N
    See NS Package Number J16A, N16E or W16A

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    5.5 V

    Operating Free Air Temperature Range
    \begin{tabular}{lr} 
    DM54S & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    Recommended Operating Conditions See Section 1 for Test Waveforms and Output Load
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54S161/163} & \multicolumn{3}{|c|}{DM74S161/163} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\mathrm{IL}}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
    \hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -1 & & & -1 & mA \\
    \hline l OL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 20 & & & 20 & mA \\
    \hline \multirow[t]{2}{*}{fCLK} & \multicolumn{2}{|l|}{Clock Frequency (Note 1)} & 0 & & 40 & 0 & & 40 & \multirow[t]{2}{*}{MHz} \\
    \hline & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & & 35 & 0 & & 35 & \\
    \hline \multirow[t]{4}{*}{\(t_{w}\)} & \multirow[t]{2}{*}{Pulse Width (Note 1)} & Clock & 10 & & & 10 & & & \multirow{4}{*}{ns} \\
    \hline & & Clear (Note 4) & 10 & & & 10 & & & \\
    \hline & \multirow[t]{2}{*}{Pulse Width (Note 2)} & Clock & 12 & & & 12 & & & \\
    \hline & & Clear (Note 4) & 12 & & & 12 & & & \\
    \hline \multirow[t]{8}{*}{\({ }^{\text {tsu }}\)} & \multirow[t]{4}{*}{Setup Time (Note 1)} & Data & 4 & & & 4 & & & \multirow{8}{*}{ns} \\
    \hline & & Enable P or T & 12 & & & 12 & & & \\
    \hline & & Load & 14 & & & 14 & & & \\
    \hline & & Clear (Note 3) & 14 & & & 14 & & & \\
    \hline & \multirow[t]{4}{*}{Setup Time (Note 2)} & Data & 5 & & & 5 & & & \\
    \hline & & Enable P or T & 14 & & & 14 & & & \\
    \hline & & Load & 16 & & & 16 & & & \\
    \hline & & Clear (Note 3) & 16 & & & 16 & & & \\
    \hline \multirow[t]{4}{*}{\({ }_{\text {th }}\)} & \multirow[t]{2}{*}{Hold Time (Note 1)} & Data & 3 & & & 3 & & & \multirow{4}{*}{ns} \\
    \hline & & Others & 0 & & & 0 & & & \\
    \hline & \multirow[t]{2}{*}{Hold Time (Note 2)} & Data & 5 & & & 5 & & & \\
    \hline & & Others & 2 & & & 2 & & & \\
    \hline \multirow[t]{2}{*}{\(t_{\text {REL }}\)} & \multicolumn{2}{|l|}{Load or Clear Release Time (Note 1)} & 12 & & & 12 & & & \multirow[t]{2}{*}{ns} \\
    \hline & \multicolumn{2}{|l|}{Load or Clear Release Time (Note 2)} & 14 & & & 14 & & & \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note 1: \(C_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 2: \(C_{L}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 3: Applies only to the ' S 163 which has synchronous clear inputs.
    Note 4: Applies only to the 'S161 which has asynchronous clear inputs.

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min} \\
    & I_{O H}=M a x \\
    & V_{I L}=M a x \\
    & V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[b]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \multirow[t]{2}{*}{\(\mathrm{IIH}^{\text {H}}\)} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=2.7 V
    \end{aligned}
    \]} & CLK, Data & & & 50 & \multirow[b]{2}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & Others & -10 & & -200 & \\
    \hline \multirow[t]{2}{*}{ILL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Max} \\
    & V_{1}=0.5 \mathrm{~V}
    \end{aligned}
    \]} & Enable T & & & -4 & \multirow[b]{2}{*}{mA} \\
    \hline & & & Others & & & -2 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x\)} & & 95 & 160 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 40 & & 35 & & MHz \\
    \hline tpLH & Propagation Delay Time Low to High Level Output & Clock to Ripple Carry & & 25 & & 25 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Ripple Carry & & 25 & & 28 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Any Q & & 15 & & 15 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Any Q & & 15 & & 18 & ns \\
    \hline \(\mathrm{t}_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Enable T to Ripple Carry & & 15 & & 18 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & Enable T to Ripple Carry & & 15 & & 18 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output (Note 3) & Clear to Any Q & & 20 & & 24 & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: Propagation delay for clearing is measured from clear input for the 'S161 and from the clock input transition for the 'S163.

    Logic Diagram
    

    \section*{Timing Diagram}

    S161, S163 Synchronous Binary Counters Typical Clear, Preset, Count and Inhibit Sequences
    

    \section*{Parameter Measurement Information}
    

    TL/F/6471-4
    Note \(A\) : The input pulses are supplied by generators having the following characteristics: PRR \(\leq 1 \mathrm{MHz}\), duty cycle \(\leq 50 \%, Z_{\text {OUT }} \approx 50 \Omega\). For \(\mathrm{S} 161 / 163\), \(t_{f} \leq 2.5 \mathrm{~ns}, \mathrm{t}_{\mathrm{f}} \leq 2.5 \mathrm{~ns}\). Vary PRR to measure \(\mathrm{f}_{\text {MAX }}\).
    Note B: Outputs \(Q_{D}\) and carry are tested at \(t_{n}+16\) for \(\mathrm{S} 161, \mathrm{~S} 163\) where \(\mathrm{t}_{\mathrm{n}}\) is the bit time when all outputs are low.
    Note C: VREF \(=1.5 \mathrm{~V}\).
    Switching Time Waveforms
    

    TL/F/6471-5
    Note A: The input pulses are supplied by generators having the following characteristics: PRR \(\leq 1 \mathrm{MHz}\), duty cycle \(\leq 50 \%, \mathrm{Z}_{\mathrm{OUT}} \approx 50 \Omega\). \(\mathrm{t}_{\mathrm{r}} \leq 2.5 \mathrm{~ns}, \mathrm{t}_{\mathrm{f}} \leq 2.5 \mathrm{~ns}\). Vary PRR to measure \(f_{\text {MAX }}\).
    Note B: Enable \(P\) and enable \(T\) setup times are measured at \(t_{n}+0\).
    Note \(C\) : \(V_{\text {REF }}=1.5 \mathrm{~V}\).

    \section*{DM54S174/DM74S174, DM54S175/DM74S175 Hex/Quad D Flip-Flops with Clear}

    \section*{General Description}

    These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) versions feature complementary outputs from each flip-flop.
    Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

    \section*{Features}
    - S174 contain six flip-flops with single-rail outputs.
    - S175 contain four flip-flops with double-rail outputs.
    - Buffered clock and direct clear inputs
    - Individual data input to each flip-flop
    - Applications include:

    Buffer/storage registers Shift registers Pattern generators
    ■ Typical clock frequency 110 MHz
    - Typical power dissipation per flip-flop 75 mW

    \section*{Connection Diagrams}
    

    Function Table (Each Fipp-Flop)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multicolumn{3}{|c|}{ Inputs } & \multicolumn{2}{c|}{ Outputs } \\
    \hline Clear & Clock & D & Q & \(\overline{\mathbf{Q}} \dagger\) \\
    \hline L & X & X & L & H \\
    H & \(\uparrow\) & \(H\) & \(H\) & L \\
    H & \(\uparrow\) & L & L & H \\
    H & L & X & \(Q_{0}\) & \(\bar{Q}_{0}\) \\
    \hline
    \end{tabular}

    \footnotetext{
    \(H=\) High Level (steady state)
    \(L=\) Low Level (steady state)
    X = Don't Care
    \(\uparrow=\) Transition from low to high level
    \(Q_{0}=\) The level of \(Q\) before the indicated steady-state input conditions were established
    \(t=\) S175 only
    }

    Absolute Maximum Ratings (Note)

    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for avallability and specifications.
    Supply Voltage
    Input Voltage
    5.5 V

    Operating Free Air Temperature Range
    DM54S
    DM74S
    Storage Temperature Range

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    Recommended Operating Conditions See Section 1 for Test Waveforms and Output Load
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54S174} & \multicolumn{3}{|c|}{DM74S175} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{2}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -1 & & & -1 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 20 & & & 20 & mA \\
    \hline \({ }_{\text {f CLK }}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 1)} & 0 & 110 & 75 & 0 & 110 & 75 & MHz \\
    \hline \({ }_{\text {f CLK }}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & 90 & 65 & 0 & 90 & 65 & MHz \\
    \hline \multirow[t]{4}{*}{\(t_{w}\)} & \multirow[t]{2}{*}{Pulse Width (Note 1)} & Clock & 7 & & & 7 & & & \multirow{4}{*}{ns} \\
    \hline & & Clear & 10 & & & 10 & & & \\
    \hline & \multirow[t]{2}{*}{Pulse Width (Note 2)} & Clock & 9 & & & 9 & & & \\
    \hline & & Clear & 12 & & & 12 & & & \\
    \hline \multirow[t]{2}{*}{tsu} & \multicolumn{2}{|l|}{Data Setup Time (Note 1)} & 5 & & & 5 & & & \multirow[b]{2}{*}{ns} \\
    \hline & \multicolumn{2}{|l|}{Data Setup Time (Note 2)} & 7 & & & 7 & & & \\
    \hline \multirow[t]{2}{*}{\({ }_{\text {t }}^{\mathrm{H}}\)} & \multicolumn{2}{|l|}{Data Hold Time (Note 1)} & 3 & & & 3 & & & \multirow[b]{2}{*}{ns} \\
    \hline & \multicolumn{2}{|l|}{Data Hold Time (Note 2)} & 5 & & & 5 & & & \\
    \hline \multirow[t]{2}{*}{\(t_{\text {REL }}\)} & \multicolumn{2}{|l|}{Clear Release Time (Note 1)} & 5 & & & 5 & & & \multirow[b]{2}{*}{ns} \\
    \hline & \multicolumn{2}{|l|}{Clear Release Time (Note 2)} & 7 & & & 7 & & & \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note 1: \(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 2: \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[b]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\) Max, \(\mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \({ }_{1 / H}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, V_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}, \mathrm{V}_{\mathrm{I}}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max} \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline Icc & Supply Current (S174) & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\text { Max } \\
    & \text { (Note 3) }
    \end{aligned}
    \]} & & 90 & 144 & mA \\
    \hline ICC & Supply Current (S175) & \multicolumn{2}{|l|}{\begin{tabular}{l}
    \[
    V_{C C}=M a x
    \] \\
    (Note 3)
    \end{tabular}} & & 60 & 96 & mA \\
    \hline
    \end{tabular}

    Switching Characteristics at \(V_{C C}=5 V_{\text {and }} T_{A}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|r|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 75 & & 65 & & MHz \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Output & & 12 & & 15 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Output & & 17 & & 21 & ns \\
    \hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output (S175 Only) & Clear to \(\bar{Q}\) & & 15 & & 18 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{aligned}
    & \text { Clear } \\
    & \text { to } \mathrm{Q}
    \end{aligned}
    \] & & 22 & & 23 & ns \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: With all outputs open and 4.5 V applied to all DATA and CLEAR inputs, ICC is measured after a momentary ground, then 4.5 V applied to the CLOCK input.

    Logic Diagrams
    

    TL/F/6472-3

    \section*{DM54S181/DM74S181 Arithmetic Logic Unit/Function Generators}

    \section*{General Description}

    These arithmetic logic units (ALU)/function generators perform 16 binary arithmetic operations on two 4-bit words, as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is available in these devices for fast, simultaneous carry generation by means of two cascade-outputs ( P and G ) for the four bits in the package. When used in conjunction with the DM54S182/DM74S182 full carry look-ahead circuits, highspeed arithmetic operations can be performed. The typical addition times shown below illustrate how little time is required for addition of longer words, when full carry lookahead is employed. The method of cascading 182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the DM54S182/DM74S182.
    (Continued)

    Features
    - Arithmetic operating modes:

    Addition
    Subtraction
    Shift operand A one position
    Magnitude comparison
    Plus twelve other arithmetic operations
    - Logic function modes:

    EXCLUSIVE-OR
    Comparator
    AND, NAND, OR, NOR
    Plus ten other logic operations
    ■ Full look-ahead for high-speed operations on long words

    \section*{Connection Diagram}
    

    Order Number DM54S181J or DM74S181N See NS Package Number J24A or N24A

    \section*{Pin Designations}
    \begin{tabular}{|c|c|c|}
    \hline Designation & Pin Nos. & Functlon \\
    \hline A3, A2, A1, A0 & \(19,21,23,2\) & Word A Inputs \\
    \hline B3, B2, B1, B0 & \(18,20,22,1\) & Word B Inputs \\
    \hline S3, S2, S1, S0 & \(3,4,5,6\) & \begin{tabular}{c} 
    Function-Select \\
    Inputs
    \end{tabular} \\
    \hline C \(_{n}\) & 7 & Inv. Carry Input \\
    \hline M & 8 & \begin{tabular}{c} 
    Mode Control \\
    Input
    \end{tabular} \\
    \hline F3, F2, F1, F0 & \(13,11,10,9\) & Function Outputs \\
    \hline A \(=\) B & 14 & Comparator Output \\
    \hline P & 15 & \begin{tabular}{c} 
    Carry Propagate \\
    Output
    \end{tabular} \\
    \hline C \(_{n}+4\) & 16 & Inv. Carry Output \\
    \hline G & 17 & \begin{tabular}{c} 
    Carry Generate \\
    Output
    \end{tabular} \\
    \hline VCC & 24 & Supply Voltage \\
    \hline GND & 12 & Ground \\
    \hline
    \end{tabular}

    \section*{General Description (Continuad)}

    If high speed is not important, a ripple-carry input \(\left(C_{n}\right)\) and a ripple-carry output ( \(C_{n}+4\) ) are available. However, the rip-ple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.
    These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below. Subtraction is accomplished by 1 's complement addition, where the 1 's complement of the subtrahend is generated internally. The resultant output is \(A-B-1\), which requires an end-around or forced carry to provide A-B.
    The S181 can also be utilized as a comparator. The \(\mathrm{A}=\mathrm{B}\) output is internally decoded from the function outputs (FO, F1, F2, F3) so that when two words of equal magnitude are applied at the \(A\) and \(B\) inputs, it will assume a high level to indicate equality \((A=B)\). The \(A L U\) should be in the subtract mode with \(C_{n}=H\) when performing this comparison. The \(A\) \(=\mathrm{B}\) output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output \(\left(C_{n}+4\right)\) can also be used to supply
    relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.
    These circuits have been designed to not only incorporate all of the designer's requriements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusiveOR, NAND, AND, NOR, and OR functions.

    \section*{ALU SIGNAL DESIGNATIONS}

    The DM54S181/DM74S181 can be used with the signal designations of either Figure 1 or Figure 2.
    The logic functions and arithmetic operations obtained with signal designations as in Figure 1 are given in Table I; those obtained with the signal designations of Figure 2 are given in Table II.
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow{2}{*}{\begin{tabular}{c} 
    Number \\
    of \\
    Bits
    \end{tabular}} & \begin{tabular}{c} 
    Typical \\
    Addition Times
    \end{tabular} & \multicolumn{2}{|c|}{ Package Count } & \multirow{2}{*}{\begin{tabular}{c} 
    Carry Method \\
    Between \\
    ALU's
    \end{tabular}} \\
    \cline { 3 - 4 } & \begin{tabular}{c} 
    Arithmetic/ \\
    Logic Units
    \end{tabular} & \begin{tabular}{c} 
    Look Ahead \\
    Carry Generators
    \end{tabular} & \begin{tabular}{c} 
    None \\
    1 to 4 \\
    5 to 8
    \end{tabular} & 20 ns \\
    9 to 16 & 30 ns & 1 & 0 & Ripple \\
    17 to 64 & 50 ns & 3 or 4 & 0 & 1
    \end{tabular}
    \begin{tabular}{c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c}
    \hline Pin Number & \(\mathbf{2}\) & \(\mathbf{1}\) & \(\mathbf{2 3}\) & \(\mathbf{2 2}\) & \(\mathbf{2 1}\) & \(\mathbf{2 0}\) & \(\mathbf{1 9}\) & \(\mathbf{1 8}\) & \(\mathbf{9}\) & \(\mathbf{1 0}\) & \(\mathbf{1 1}\) & \(\mathbf{1 3}\) & \(\mathbf{7}\) & \(\mathbf{1 6}\) & \(\mathbf{1 5}\) & \(\mathbf{1 7}\) \\
    \hline Active-High Data (Table I) & A 0 & B 0 & A 1 & B 1 & A 2 & B 2 & A 3 & B 3 & F 0 & F 1 & F 2 & F 3 & \(\overline{\mathrm{C}}_{n}\) & \(\overline{\mathrm{C}}_{n}+4\) & X & Y \\
    \hline Active-Low Data (Table II) & \(\overline{\mathrm{A}} 0\) & \(\overline{\mathrm{~B}} 0\) & \(\overline{\mathrm{~A}} 1\) & \(\overline{\mathrm{~B}} 1\) & \(\overline{\mathrm{~A}} 2\) & \(\overline{\mathrm{~B}} 2\) & \(\overline{\mathrm{~A}} 3\) & \(\overline{\mathrm{~B}} 3\) & \(\overline{\mathrm{~F}} 0\) & \(\overline{\mathrm{~F}} 1\) & \(\overline{\mathrm{~F}} 2\) & \(\overline{\mathrm{~F}} 3\) & \(\mathrm{C}_{n}\) & \(\mathrm{C}_{n}+4\) & \(\overline{\mathrm{P}}\) & \(\overline{\mathrm{G}}\) \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|}
    \hline \begin{tabular}{c} 
    Input \\
    \(\mathrm{C}_{\boldsymbol{n}}\)
    \end{tabular} & \begin{tabular}{c} 
    Output \\
    \(\mathrm{C}_{\boldsymbol{n}}+\mathbf{4}\)
    \end{tabular} & \begin{tabular}{c} 
    Active-High Data \\
    (Figure 1)
    \end{tabular} & \begin{tabular}{c} 
    Active-Low Data \\
    (Figure 2)
    \end{tabular} \\
    \hline\(H\) & \(H\) & \(A \leq B\) & \(A \leq B\) \\
    \(H\) & L & \(\mathrm{A} \leq \mathrm{B}\) & \(\mathrm{A} \leq \mathrm{B}\) \\
    L & \(H\) & \(\mathrm{~A} \leq \mathrm{B}\) & \(\mathrm{A} \leq \mathrm{B}\) \\
    L & L & \(\mathrm{A} \leq \mathrm{B}\) & \(\mathrm{A} \leq \mathrm{B}\) \\
    \hline
    \end{tabular}

    General Description (Continued)
    

    FIGURE 1

    TABLE I
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multicolumn{4}{|c|}{\multirow{2}{*}{Selection}} & \multicolumn{3}{|c|}{Active High Data} \\
    \hline & & & & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    \mathbf{M}=\mathbf{H}
    \] \\
    Logic Functions
    \end{tabular}} & \multicolumn{2}{|c|}{M \(=\) L; Arithmetic Operations} \\
    \hline S3 & S2 & S1 & S0 & & \(\mathrm{C}_{\mathrm{n}}=\mathrm{H}\) ( no carry) & \(C_{n}=L\) (with carry) \\
    \hline L & L & L & L & \(F=\bar{A}\) & \(F=A\) & \(F=A\) Plus 1 \\
    \hline L & L & L & H & \(F=\overline{A+B}\) & \(F=A+B\) & \(F=(A+B)\) Plus 1 \\
    \hline L & L & H & L & \(F=\overline{\mathrm{AB}}\) & \(F=A+\bar{B}\) & \(F=(A+\bar{B})\) Plus 1 \\
    \hline L & L & H & H & \(\mathrm{F}=0\) & \(\mathrm{F}=\) Minus 1 (2's Compl) & \(F=\) Zero \\
    \hline L & H & L & L & \(F=\overline{A B}\) & \(F=A\) Plus \(A \bar{B}\) & \(F=A\) Plus \(A \bar{B}\) Plus 1 \\
    \hline L & H & L & H & \(\mathrm{F}=\overline{\mathrm{B}}\) & \(F=(A+B)\) Plus \(A \bar{B}\) & \(F=(A+B)\) Plus \(A \bar{B}\) Plus 1 \\
    \hline L & H & H & L & \(F=A \oplus B\) & \(F=A\) Minus \(B\) Minus 1 & \(F=A\) Minus \(B\) \\
    \hline L & H & H & H & \(F=A \bar{B}\) & \(F=A \bar{B}\) Minus 1 & \(F=A \bar{B}\) \\
    \hline H & L & L & L & \(F=\bar{A}+B\) & \(F=A\) Plus \(A B\) & \(F=A\) Plus AB Plus 1 \\
    \hline H & L & L & H & \(F=\overline{A \oplus B}\) & \(F=A\) Plus B & \(F=A\) Plus \(B\) Plus 1 \\
    \hline H & L & H & L & \(F=B\) & \(F=(A+\bar{B})\) Plus \(A B\) & \(F=(A+\bar{B})\) Plus \(A B\) Plus 1 \\
    \hline H & L & H & H & \(F=A B\) & \(F=A B\) Minus 1 & \(F=A B\) \\
    \hline H & H & L & L & \(\mathrm{F}=1\) & \(\mathrm{F}=\mathrm{A}\) Plus \(\mathrm{A}^{*}\) & \(\mathrm{F}=\mathrm{A}\) Plus A Plus 1 \\
    \hline H & H & L & H & \(F=A+\bar{B}\) & \(F=(A+B)\) Plus \(A\) & \(F=(A+B)\) Plus A Plus 1 \\
    \hline H & H & H & L & \(F=A+B\) & \(F=(A+\bar{B})\) Plus \(A\) & \(F=(A+\bar{B})\) Plus A Plus 1 \\
    \hline H & H & H & H & \(F=A\) & \(F=A\) Minus 1 & \(F=A\) \\
    \hline
    \end{tabular}
    *Each bit is shifted to the next more significant position.
    

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    FIGURE 2

    TABLE II
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multicolumn{4}{|c|}{\multirow{2}{*}{Selection}} & \multicolumn{3}{|c|}{Active Low Data} \\
    \hline & & & & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    M=H
    \] \\
    Logic Functions
    \end{tabular}} & \multicolumn{2}{|r|}{\(\mathbf{M}=\mathrm{L}\); Arithmetic Operations} \\
    \hline S3 & S2 & S1 & SO & & \(\mathrm{C}_{\mathrm{n}}=\mathrm{L}\) ( no carry) & \(\mathrm{C}_{\mathrm{n}}=\mathrm{H}\) (with carry) \\
    \hline L & L & L & L & \(F=\bar{A}\) & \(F=A\) Minus 1 & \(F=A\) \\
    \hline L & L & L & H & \(F=\overline{A B}\) & \(F=A B\) Minus 1 & \(F=A B\) \\
    \hline L & L & H & L & \(F=\bar{A}+B\) & \(F=A \bar{B}\) Minus 1 & \(F=A \bar{B}\) \\
    \hline L & L & H & H & \(\mathrm{F}=1\) & \(\mathrm{F}=\) Minus 1 (2's Compl) & \(F=\) Zero \\
    \hline L & H & L & L & \(F=\overline{A+B}\) & \(\mathrm{F}=\mathrm{A}\) Plus \((\mathrm{A}+\overline{\mathrm{B}})\) & \(F=A\) Plus ( \(\mathrm{A}+\overline{\mathrm{B}}\) ) Plus 1 \\
    \hline L & H & L & H & \(F=\bar{B}\) & \(F=A B\) Plus ( \(A+B\) ) & \(F=A B\) Plus \((A+\bar{B})\) Plus 1 \\
    \hline L & H & H & L & \(F=\overline{A \oplus B}\) & \(F=A\) Minus \(B\) Minus 1 & \(F=A\) Minus \(B\) \\
    \hline L & H & H & H & \(F=A+\bar{B}\) & \(F=A+\bar{B}\) & \(F=(A+\bar{B})\) Plus 1 \\
    \hline H & L & L & L & \(F=\bar{A} B\) & \(F=A\) Plus \((A+B)\) & \(F=A\) Plus ( \(A+B\) ) Plus 1 \\
    \hline H & L & L & H & \(F=A \oplus B\) & \(F=A\) Plus \(B\) & \(F=A\) Plus B Plus 1 \\
    \hline H & L & H & L & \(F=B\) & \(F=A \bar{B}\) Plus \((A+B)\) & \(F=A \bar{B}\) Plus \((A+B)\) Plus 1 \\
    \hline H & L & H & H & \(F=A+B\) & \(F=A+B\) & \(F=(A+B)\) Plus 1 \\
    \hline H & H & L & L & \(F=0\) & \(F=\) A Plus \({ }^{*}\) & \(\mathrm{F}=\mathrm{A}\) Plus A Plus 1 \\
    \hline H & H & L & H & \(F=A+A \bar{B}\) & \(F=A B\) Plus \(A\) & \(F=A B\) Plus A Plus 1 \\
    \hline H & H & H & L & \(F=A B\) & \(F=A \bar{B}\) Plus \(A\) & \(F=A \bar{B}\) Plus \(A\) Plus 1 \\
    \hline H & H & H & H & \(F=A\) & \(F=A\) & \(\mathrm{F}=\mathrm{A}\) Plus 1 \\
    \hline
    \end{tabular}
    *Each bit is shifted to the next more significant position.

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    \begin{tabular}{lr} 
    Supply Voltage & 7 V \\
    Input Voltage & 5.5 V \\
    Output Voltage (A = B Output) & 5.5 V \\
    Operating Free Air Temperature Range & \\
    DM54S & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S181} & \multicolumn{3}{|c|}{DM74S181} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage ( \(\mathrm{A}=\mathrm{B}\) Output) & & & 5.5 & & & 5.5 & V \\
    \hline IOH & High Level Output Current (All Except A = B) & & & -1 & & & -1 & mA \\
    \hline \(\mathrm{l}_{\mathrm{OL}}\) & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \(l_{\text {CEX }}\) & High Level Output Current ( \(\mathrm{A}=\mathrm{B}\) Output) & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{O}}=5.5 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & & & 250 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage (All Except A = B)} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O H}=\operatorname{Max} \\
    & V_{I L}=M a x, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline V \({ }_{\text {OL }}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\
    & V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 11 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \multirow[t]{4}{*}{\(\mathrm{IIH}^{\text {H}}\)} & \multirow[t]{4}{*}{High Level Input Current} & \multirow[t]{4}{*}{\[
    \begin{aligned}
    & V_{C c}=M a x \\
    & V_{1}=2.7 V
    \end{aligned}
    \]} & Mode & & & 50 & \multirow{4}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & A or B & & & 150 & \\
    \hline & & & S & & & 200 & \\
    \hline & & & Carry & & & 250 & \\
    \hline \multirow[t]{4}{*}{IIL} & \multirow[t]{4}{*}{Low Level Input Current} & \multirow[t]{4}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=0.5 V
    \end{aligned}
    \]} & Mode & & & -2 & \multirow{4}{*}{mA} \\
    \hline & & & A or B & & & -6 & \\
    \hline & & & S & & & -8 & \\
    \hline & & & Carry & & & -10 & \\
    \hline los & Short Circuit Output Current (Any Output Except A = B) & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}(\) Note 2)} & -40 & & -100 & mA \\
    \hline lCC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 3)} & & 120 & 220 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: \(\mathrm{I}_{\mathrm{CC}}\) is measured for the following conditions: A. SO through \(\mathrm{S} 3, \mathrm{M}\), and A inputs at 4.5 V , all other inputs grounded and all outputs open. B. SO through S 3 and M inputs at 4.5 V , all other inputs grounded and all outputs open.

    Switching Characteristics \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{Conditions} & \multirow{3}{*}{From (Input)} & \multirow{3}{*}{To (Output)} & \multicolumn{4}{|c|}{\[
    \begin{gathered}
    \text { DM54/74 } \\
    \text { S181 }
    \end{gathered}
    \]} & \multirow{3}{*}{Units} \\
    \hline & & & & & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & R_{\mathrm{L}}=280 \Omega, \\
    & \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}
    \end{aligned}
    \]} & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathbf{R}_{\mathrm{L}}=280 \Omega, \\
    & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}
    \end{aligned}
    \]} & \\
    \hline & & & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time, Low-to-High Level Output & & \multirow[t]{2}{*}{\(C_{n}\)} & \multirow[t]{2}{*}{\(C_{n}+4\)} & & 10.5 & & 14 & \multirow[t]{2}{*}{ns} \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 10.5 & & 14 & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & M=0 V, S 0= \\
    & S 3=4.5 V \\
    & S 1=S 2=0 V \\
    & (\overline{S U M} \text { mode })
    \end{aligned}
    \]} & \multirow[t]{2}{*}{Any A or B} & \multirow[t]{2}{*}{\(\mathrm{C}_{\mathrm{n}}+4\)} & & 18.5 & & 22 & \multirow[t]{2}{*}{ns} \\
    \hline \(\mathrm{t}_{\mathrm{PHL}}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 18.5 & & 22 & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{\[
    \begin{array}{|l|}
    \hline M=O V, S O= \\
    S 3=O V \\
    S 1=S 2=4.5 \mathrm{~V} \\
    (\overline{\text { DIFF }} \text { mode })
    \end{array}
    \]} & \multirow[t]{2}{*}{Any A or B} & \multirow[t]{2}{*}{\(\mathrm{C}_{\mathrm{n}}+4\)} & & 23 & & 27 & \multirow[t]{2}{*}{ns} \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 23 & & 27 & \\
    \hline \({ }_{\text {tPLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & M=0 V \\
    & \text { (SUM or } \\
    & \text { DIFF mode) }
    \end{aligned}
    \]} & \multirow[t]{2}{*}{\(\mathrm{C}_{\mathrm{n}}\)} & \multirow[t]{2}{*}{Any F} & & 12 & & 14 & \multirow[t]{2}{*}{ns} \\
    \hline \({ }_{\text {t }}\) HLL & Propagation Delay Time, High-to-Low Level Output & & & & & 12 & & 14 & \\
    \hline \({ }_{\text {tplH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & M=0 V, S 0= \\
    & S 3=4.5 V \\
    & S 1=S 2=0 V \\
    & (\overline{S U M} \text { mode })
    \end{aligned}
    \]} & \multirow[t]{2}{*}{Any A or B} & \multirow[t]{2}{*}{G} & & 12 & & 15 & \multirow[t]{2}{*}{ns} \\
    \hline tphL & Propagation Delay Time, High-to-Low Level Output & & & & & 12 & & 15 & \\
    \hline \({ }_{\text {tPLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \hline M=O V, S 0= \\
    & S 3=O V \\
    & S 1=S 2=4.5 V \\
    & \text { (DIFF mode })
    \end{aligned}
    \]} & \multirow[t]{2}{*}{Any A or B} & \multirow[t]{2}{*}{G} & & 15 & & 19 & \multirow[t]{2}{*}{ns} \\
    \hline \({ }^{\text {tpHL }}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 15 & & 20 & \\
    \hline \(t_{\text {tpLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & M=0 V, S 0= \\
    & S 3=4.5 V \\
    & S 1=S 2=0 V \\
    & (\overline{S U M} \text { mode })
    \end{aligned}
    \]} & \multirow[t]{2}{*}{Any A or B} & \multirow[t]{2}{*}{P} & & 12 & & 15 & \multirow[t]{2}{*}{ns} \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 12 & & 15 & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & M=O V, S 0= \\
    & S 3=O V \\
    & S 1=S 2=4.5 \mathrm{~V} \\
    & \text { (DIFF mode) }
    \end{aligned}
    \]} & \multirow[t]{2}{*}{Any A or B} & \multirow[t]{2}{*}{P} & & 15 & & 19 & \multirow[t]{2}{*}{ns} \\
    \hline \({ }^{\text {tpHL }}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 15 & & 20 & \\
    \hline \({ }_{\text {tpLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & M=0 \mathrm{~V}, \mathrm{SO}= \\
    & \mathrm{S} 3=4.5 \mathrm{~V} \\
    & \mathrm{~S} 1=\mathrm{S} 2=0 \mathrm{~V} \\
    & (\mathrm{SUM} \text { mode })
    \end{aligned}
    \]} & \multirow[t]{2}{*}{\(A_{i}\) or \(B_{i}\)} & \multirow[t]{2}{*}{\(\mathrm{F}_{\mathrm{i}}\)} & & 16.5 & & 20 & \multirow[t]{2}{*}{ns} \\
    \hline \({ }_{\text {tpHL }}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 16.5 & & 20 & \\
    \hline \({ }_{\text {tpLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & M=O V, S 0= \\
    & S 3=O V \\
    & S 1=S 2=4.5 \mathrm{~V} \\
    & \hline(\overline{D I F F} \text { mode })
    \end{aligned}
    \]} & \multirow[t]{2}{*}{\(A_{i}\) or \(B_{i}\)} & \multirow[t]{2}{*}{\(\mathrm{F}_{\mathrm{i}}\)} & & 20 & & 24 & \multirow[t]{2}{*}{ns} \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 22 & & 24 & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & M=4.5 \mathrm{~V} \\
    & \text { (logic mode) }
    \end{aligned}
    \]} & \multirow[t]{2}{*}{\(\mathrm{A}_{i}\) or \(\mathrm{B}_{\mathrm{i}}\)} & \multirow[t]{2}{*}{\(\mathrm{F}_{\mathrm{i}}\)} & & 20 & & 24 & \multirow[t]{2}{*}{ns} \\
    \hline \(\mathrm{t}_{\mathrm{PHL}}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 22 & & 24 & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time, Low-to-High Level Output & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & M=O V, S 0= \\
    & S 3=O V \\
    & S 1=S 2=4.5 \mathrm{~V} \\
    & \text { (DIFF mode) }
    \end{aligned}
    \]} & \multirow[t]{2}{*}{Any A or B} & \multirow[t]{2}{*}{\(A=B\)} & & 23 & & 26 & \multirow[t]{2}{*}{ns} \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time, High-to-Low Level Output & & & & & 30 & & 33 & \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{8}{|l|}{Parameter Measurement Information} \\
    \hline \multicolumn{8}{|c|}{\begin{tabular}{l}
    Logic Mode Test Table \\
    Function Inputs: S1 \(=\mathbf{S 2}=\mathrm{M}=\mathbf{4 . 5 V}, \mathrm{SO}=\mathrm{S} 3=\mathbf{O V}\)
    \end{tabular}} \\
    \hline \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{\begin{tabular}{l}
    Input \\
    Under \\
    Test
    \end{tabular}} & \multicolumn{2}{|c|}{Other Input Same Bit} & \multicolumn{2}{|r|}{Other Data Inputs} & \multirow[t]{2}{*}{\begin{tabular}{l}
    Output \\
    Under \\
    Test
    \end{tabular}} & \multirow[t]{2}{*}{Output Waveform} \\
    \hline & & \[
    \begin{gathered}
    \text { Apply } \\
    4.5 \mathrm{~V}
    \end{gathered}
    \] & Apply GND & Apply 4.5V & Apply GND & & \\
    \hline \[
    \frac{t_{\mathrm{PLH}}}{\mathrm{t}_{\mathrm{PHL}}}
    \] & \(A_{i}\) & \(\mathrm{B}_{i}\) & None & None & Remaining A and \(\mathrm{B}, \mathrm{C}_{\mathrm{n}}\) & \(\mathrm{F}_{\mathrm{i}}\) & Out-of-Phase \\
    \hline \(t_{\text {PLH }}\) & \multirow[t]{2}{*}{\(\mathrm{B}_{i}\)} & \multirow[t]{2}{*}{\(A_{i}\)} & \multirow[t]{2}{*}{None} & \multirow[t]{2}{*}{None} & \multirow[t]{2}{*}{\begin{tabular}{l}
    Remaining \\
    \(A\) and \(B, C_{n}\)
    \end{tabular}} & \multirow[t]{2}{*}{\(\mathrm{F}_{\mathrm{i}}\)} & \multirow[t]{2}{*}{Out-of-Phase} \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & & & & & & & \\
    \hline
    \end{tabular}

    SUM Mode Test Table
    Function Inputs: \(\mathrm{SO}=\mathbf{S 3}=\mathbf{4 . 5 V}, \mathrm{S} 1=\mathrm{S} 2=\mathrm{M}=\mathbf{O V}\)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Input Under Test} & \multicolumn{2}{|r|}{Other Input Same Bit} & \multicolumn{2}{|l|}{Other Data Inputs} & \multirow[t]{2}{*}{Output Under Test} & \multirow[t]{2}{*}{Output Waveform} \\
    \hline & & Apply
    \[
    4.5 \mathrm{~V}
    \] & Apply GND & Apply
    \[
    4.5 \mathrm{~V}
    \] & Apply GND & & \\
    \hline \[
    \frac{t_{\mathrm{PLH}}}{t_{\mathrm{PHLL}}}
    \] & \(\mathrm{A}_{\mathrm{i}}\) & \(B_{i}\) & None & Remaining \(A\) and \(B\) & \(C_{n}\) & \(\mathrm{F}_{\mathrm{i}}\) & In-Phase \\
    \hline \[
    \frac{t_{\text {PLH }}}{t_{\text {PHL }}}
    \] & \(\mathrm{B}_{\mathrm{i}}\) & \(\mathrm{A}_{\mathrm{i}}\) & None & Remaining \(A\) and \(B\) & \(\mathrm{C}_{\mathrm{n}}\) & \(\mathrm{F}_{\mathrm{i}}\) & In-Phase \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & \(\mathrm{A}_{\mathrm{i}}\) & \(\mathrm{B}_{\mathrm{i}}\) & None & None & \begin{tabular}{l}
    Remaining \\
    \(A\) and \(B, C_{n}\)
    \end{tabular} & P & In-Phase \\
    \hline \[
    \frac{t_{\text {PLH }}}{t_{\text {PHL }}}
    \] & \(B_{i}\) & \(A_{i}\) & None & None & \begin{tabular}{l}
    Remaining \\
    \(A\) and \(B, C_{n}\)
    \end{tabular} & P & In-Phase \\
    \hline \({ }_{\text {tPLH }}\) & \(A_{i}\) & None & \(\mathrm{B}_{\mathrm{i}}\) & Remaining B & Remaining \(A, C_{n}\) & G & In-Phase \\
    \hline \[
    \frac{t_{\mathrm{PLH}}}{\mathrm{t}_{\mathrm{PHL}}}
    \] & \(\mathrm{B}_{\mathrm{i}}\) & None & \(A_{i}\) & Remaining B & Remaining \(A, C_{n}\) & G & In-Phase \\
    \hline \[
    \frac{t_{\text {PLH }}}{t_{\text {PHL }}}
    \] & \(C_{n}\) & None & None & \[
    \begin{gathered}
    \text { All } \\
    \text { A }
    \end{gathered}
    \] & \[
    \begin{gathered}
    \text { All } \\
    \text { B }
    \end{gathered}
    \] & \[
    \begin{gathered}
    \text { Any } F \\
    \text { or } C_{n}+4
    \end{gathered}
    \] & In-Phase \\
    \hline \[
    \frac{t_{\text {PLH }}}{t_{\text {PHL }}}
    \] & \(\mathrm{A}_{i}\) & None & \(\mathrm{B}_{\mathrm{i}}\) & Remaining B & Remaining A, \(C_{n}\) & \(C_{n}+4\) & Out-of-Phase \\
    \hline \(\mathrm{t}_{\text {tPL }}\) & \(\mathrm{B}_{\mathrm{i}}\) & None & \(A_{i}\) & Remaining B & Remaining \(A, C_{n}\) & \(C_{n}+4\) & Out-of-Phase \\
    \hline
    \end{tabular}

    Parameter Measurement Information (Continued)
    \(\overline{\text { DIFF }}\) Mode Test Table
    Function Inputs: \(\mathrm{S} 1=\mathrm{S} 2=4.5 \mathrm{~V}, \mathrm{SO}=\mathrm{S} 3=\mathrm{M}=\mathbf{O V}\)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{\begin{tabular}{l}
    Input \\
    Under Test
    \end{tabular}} & \multicolumn{2}{|l|}{Other Input Same Bit} & \multicolumn{2}{|l|}{Other Data Inputs} & \multirow[t]{2}{*}{\begin{tabular}{l}
    Output \\
    Under \\
    Test
    \end{tabular}} & \multirow[t]{2}{*}{Output Waveform} \\
    \hline & & Apply 4.5V & Apply GND & Apply 4.5V & Apply GND & & \\
    \hline \[
    \frac{t_{\text {PLH }}}{t_{\text {PHL }}}
    \] & \(A_{i}\) & None & \(\mathrm{Bi}_{i}\) & Remaining A & Remaining \(B, C_{n}\) & \(\mathrm{F}_{\mathrm{i}}\) & In-Phase \\
    \hline \(t_{\text {tPLH }}\) & \(\mathrm{B}_{\mathrm{i}}\) & \(A_{i}\) & None & \[
    \begin{gathered}
    \text { Remaining }
    \end{gathered}
    \] & Remaining \(B, C_{n}\) & \(\mathrm{F}_{\mathrm{i}}\) & Out-of-Phase \\
    \hline \(t_{\text {PLH }}\) & \multirow[t]{2}{*}{\(A_{i}\)} & \multirow[t]{2}{*}{None} & \multirow[t]{2}{*}{\(\mathrm{B}_{\mathrm{i}}\)} & \multirow[t]{2}{*}{None} & \multirow[t]{2}{*}{\begin{tabular}{l}
    Remaining \\
    A and \(\mathrm{B}, \mathrm{C}_{\mathrm{n}}\)
    \end{tabular}} & \multirow[t]{2}{*}{P} & \multirow[t]{2}{*}{In-Phase} \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & & & & & & & \\
    \hline tplH & \multirow[t]{2}{*}{\(B_{i}\)} & \multirow[t]{2}{*}{\(A_{i}\)} & \multirow[t]{2}{*}{None} & \multirow[t]{2}{*}{None} & \multirow[t]{2}{*}{Remaining A and \(\mathrm{B}, \mathrm{C}_{\mathrm{n}}\)} & \multirow[t]{2}{*}{P} & \multirow[t]{2}{*}{Out-of-Phase} \\
    \hline tPHL & & & & & & & \\
    \hline tpLH & \multirow[t]{2}{*}{\(A_{i}\)} & \multirow[t]{2}{*}{\(\mathrm{B}_{\mathrm{i}}\)} & \multirow[t]{2}{*}{None} & \multirow[t]{2}{*}{None} & \multirow[t]{2}{*}{Remaining \(A\) and \(B, C_{n}\)} & \multirow[t]{2}{*}{G} & \multirow[t]{2}{*}{In-Phase} \\
    \hline \(t_{\text {PHL }}\) & & & & & & & \\
    \hline tpLH & \multirow[t]{2}{*}{\(\mathrm{B}_{\mathrm{i}}\)} & \multirow[t]{2}{*}{None} & \multirow[t]{2}{*}{\(\mathrm{A}_{\mathrm{i}}\)} & \multirow[t]{2}{*}{None} & \multirow[t]{2}{*}{\begin{tabular}{l}
    Remaining \\
    A and \(\mathrm{B}, \mathrm{C}_{\mathrm{n}}\)
    \end{tabular}} & \multirow[t]{2}{*}{G} & \multirow[t]{2}{*}{Out-of-Phase} \\
    \hline tpHL & & & & & & & \\
    \hline \(t_{\text {PLH }}\) & \multirow[t]{2}{*}{\(A_{i}\)} & \multirow[t]{2}{*}{None} & \multirow[t]{2}{*}{\(\mathrm{B}_{\mathrm{i}}\)} & \multirow[t]{2}{*}{Remaining
    A} & \multirow[t]{2}{*}{Remaining \(B, C_{n}\)} & \multirow[t]{2}{*}{\(A=B\)} & \multirow[t]{2}{*}{In-Phase} \\
    \hline \(t_{\text {PHL }}\) & & & & & & & \\
    \hline \(t_{\text {PLH }}\) & \multirow[t]{2}{*}{\(\mathrm{B}_{\mathrm{i}}\)} & \multirow[t]{2}{*}{\(A_{i}\)} & \multirow[t]{2}{*}{None} & \multirow[t]{2}{*}{Remaining
    A} & \multirow[t]{2}{*}{Remaining \(B, C_{n}\)} & \multirow[t]{2}{*}{\(A=B\)} & \multirow[t]{2}{*}{Out-of-Phase} \\
    \hline \(t_{\text {PHL }}\) & & & & & & & \\
    \hline tpLH & \multirow[t]{2}{*}{\(\mathrm{C}_{\mathrm{n}}\)} & \multirow[t]{2}{*}{None} & \multirow[t]{2}{*}{None} & \multirow[t]{2}{*}{All \(A\) and \(B\)} & \multirow[t]{2}{*}{None} & \multirow[t]{2}{*}{\[
    \begin{gathered}
    \mathrm{C}_{\mathrm{n}}+4 \\
    \text { or any } \mathrm{F}
    \end{gathered}
    \]} & \multirow[t]{2}{*}{In-Phase} \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & & & & & & & \\
    \hline \(t_{\text {PLH }}\) & \multirow[t]{2}{*}{\(A_{i}\)} & \multirow[t]{2}{*}{\(\mathrm{B}_{\mathrm{i}}\)} & \multirow[t]{2}{*}{None} & \multirow[t]{2}{*}{None} & \multirow[t]{2}{*}{Remaining \(A, B, C_{n}\)} & \multirow[t]{2}{*}{\(C_{n}+4\)} & \multirow[t]{2}{*}{Out-of-Phase} \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & & & & & & & \\
    \hline \(t_{\text {PLH }}\) & \multirow[t]{2}{*}{\(\mathrm{B}_{\mathrm{i}}\)} & \multirow[t]{2}{*}{None} & \multirow[t]{2}{*}{\(\mathrm{A}_{\mathrm{i}}\)} & \multirow[t]{2}{*}{None} & \multirow[t]{2}{*}{Remaining
    \[
    A, B, C_{n}
    \]} & \multirow[t]{2}{*}{\(\mathrm{C}_{\mathrm{n}}+4\)} & \multirow[t]{2}{*}{In-Phase} \\
    \hline tPHL & & & & & & & \\
    \hline
    \end{tabular}
    

    TL/F/6473-4

    \section*{DM54S182/DM74S182 Look-Ahead Carry Generators}

    \section*{General Description}

    These circuits are high-speed, look-ahead carry generators, capable of anticipating a carry across four binary adders or groups of adders. They are cascadable to perform full lookahead across \(n\)-bit adders. Carry, generate-carry, and prop-agate-carry functions are provided as shown in the pin designation table.
    When used in conjunction with the 181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each S182 generates the lookahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to \(n\)-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.
    Carry input and output of the ALU's are in their true form, and the carry propagate ( \(P\) ) and carry generate \((G)\) are in negated form; therefore, the carry functions (inputs, outputs,
    generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Positive logic equations for the S182 are:
    \[
    \begin{aligned}
    & C_{n}+x=\bar{G} 0+\bar{P} 0 C_{n} \\
    & C_{n}+y=\bar{G} 1+\bar{P} 1 \bar{G} 0+\bar{P} 1 \bar{P} 0 C_{n} \\
    & C_{n}+z=\bar{G} 2+\bar{P} 2 \bar{G} 1+\bar{P} 2 \bar{P} 1 \bar{G} 0+\bar{P} 2 \bar{P} 1 \bar{P} 0 C_{n} \\
    & \bar{G}=\bar{G} 3(\bar{P} 3+\bar{G} 2)(\bar{P} 3+\bar{P} 2+\bar{G} 1) \\
    & \quad(\bar{P} 3+\bar{P} 2+\bar{P} 1+\bar{G} 0) \\
    & \quad \bar{P}=\bar{P} 3 \bar{P} 2 \bar{P} 1 \bar{P} 0
    \end{aligned}
    \]

    \section*{Features}
    - Typical propagation delay time 7 ns
    - Typical power dissipation 260 mW

    \section*{Connection Diagram}
    

    TL/F/6474-1
    Order Number DM54S182J or DM74S182N See NS Package Number J16A or N16E

    \section*{Pin Designations}
    \begin{tabular}{|c|c|c|}
    \hline Designation & Pin Nos. & Function \\
    \hline G0, G1, G2, G3 & \(3,1,14,5\) & \begin{tabular}{c} 
    Active Low \\
    Carry Generate Inputs
    \end{tabular} \\
    \hline P0, P1, P2, P3 & \(4,2,15,6\) & \begin{tabular}{c} 
    Active Low \\
    Carry Propagate Inputs
    \end{tabular} \\
    \hline\(C_{n}\) & 13 & Carry Input \\
    \hline \begin{tabular}{c}
    \(C_{n}+x, C_{n}+y\) \\
    \(C_{n}+z\)
    \end{tabular} & \(12,11,9\) & Carry Outputs \\
    \hline G & 10 & \begin{tabular}{c} 
    Active Low \\
    Carry Generate Output
    \end{tabular} \\
    \hline\(P\) & 7 & \begin{tabular}{c} 
    Active Low \\
    Carry Propagate Output
    \end{tabular} \\
    \hline VCC & 16 & Supply Voltage \\
    \hline GND & 8 & Ground \\
    \hline
    \end{tabular}
    

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S182} & \multicolumn{3}{|c|}{DM74S182} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline \({ }^{\mathrm{IOH}}\) & High Level Output Current & & & -1 & & & -1 & mA \\
    \hline lOL & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
    \begin{aligned}
    & \text { Typ } \\
    & \text { (Note 1) }
    \end{aligned}
    \] & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O L}=M a x \\
    & V_{I H}=M i n, V_{I L}=M a x
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \multirow[t]{6}{*}{\(\mathrm{IIH}^{\text {H}}\)} & \multirow[t]{6}{*}{High Level Input Current} & \multirow[t]{6}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=M a x \\
    & V_{1}=2.7 \mathrm{~V}
    \end{aligned}
    \]} & P0, P1 or G3 & & & 200 & \multirow{6}{*}{\(\mu A\)} \\
    \hline & & & P3 & & & 100 & \\
    \hline & & & P2 & & & 150 & \\
    \hline & & & \(\mathrm{C}_{\mathrm{n}}\) & & & 50 & \\
    \hline & & & G0, G2 & & & 350 & \\
    \hline & & & G1 & & & 400 & \\
    \hline \multirow[t]{6}{*}{IIL} & \multirow[t]{6}{*}{Low Level Input Current} & \multirow[t]{6}{*}{\[
    \begin{aligned}
    & V_{c C}=M a x \\
    & V_{1}=0.5 \mathrm{~V}
    \end{aligned}
    \]} & P0, P1 or G3 & & & -8 & \multirow{6}{*}{mA} \\
    \hline & & & P3 & & & -4 & \\
    \hline & & & P2 & & & -6 & \\
    \hline & & & \(\mathrm{C}_{\mathrm{n}}\) & & & -2 & \\
    \hline & & & G0, G2 & & & -14 & \\
    \hline & & & G1 & & & -16 & \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline \multirow[t]{2}{*}{ICCH} & \multirow[t]{2}{*}{Supply Current with Outputs High} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Max} \\
    & \text { (Note 3) }
    \end{aligned}
    \]} & DM54 & & 39 & 55 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & & 39 & 55 & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{I}_{\mathrm{CCL}}\)} & \multirow[t]{2}{*}{Supply Currents with Outputs Low} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Max} \\
    & \text { (Note 4) }
    \end{aligned}
    \]} & DM54 & & 69 & 99 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & & 69 & 109 & \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: ICCH is measured with all outputs open, inputs P3 and G3 at 4.5V , and all other inputs grounded.
    Note 4: ICCL is measured with all outputs open, inputs G0, G1, and G2 at 4.5 V , and all other inputs grounded.

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathbf{R}_{\mathbf{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|r|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Min & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    \mathrm{GN} \text { or } \mathrm{PN} \\
    \text { to } \mathrm{C}_{\mathrm{n}}+\mathrm{x}, \mathrm{y}, \mathrm{z}
    \end{gathered}
    \] & & 7 & & 10 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \mathrm{GN} \text { or } \mathrm{PN} \\
    \text { to } \mathrm{C}_{\mathrm{n}}+\mathrm{x}, \mathrm{y}, \mathrm{z}
    \end{gathered}
    \] & & 7 & & 11 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    \mathrm{GN} \text { or } \mathrm{PN} \\
    \text { to } \mathrm{G}
    \end{gathered}
    \] & & 7.5 & & 11 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \mathrm{GN} \text { or } \mathrm{PN} \\
    \text { to } \mathrm{G}
    \end{gathered}
    \] & & 10.5 & & 14 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{aligned}
    & \mathrm{PN} \\
    & \text { to } \mathrm{P}
    \end{aligned}
    \] & & 6.5 & & 10 & ns \\
    \hline tPHL & Propagation Delay Time High to Low Level Output & \[
    \begin{array}{r}
    \mathrm{PN} \\
    \text { to } \mathrm{P}
    \end{array}
    \] & & 10 & & 14 & ns \\
    \hline tple & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    C_{n} \text { to } \\
    \text { to } C_{n}+x, y, z \\
    \hline
    \end{gathered}
    \] & & 10 & & 13 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    C_{n} \text { to } \\
    \text { to } C_{n}+x, y, z \\
    \hline
    \end{gathered}
    \] & & 10.5 & & 14 & ns \\
    \hline
    \end{tabular}
    

    TL/F/6474-2

    \section*{Typical Application}

    \section*{64-Bit ALU, Full-Carry Look Ahead in Three Levels}
    

    TL/F/6474-3
    \(A\) and \(B\) inputs, and \(F\) outputs of 181 are not shown.

    \section*{DM54S194/DM74S194}

    \section*{4-Bit Bidirectional Universal Shift Registers}

    \section*{General Description}

    These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register; they feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-modecontrol inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:
    Parallel (broadside) load
    Shift right (in the direction \(Q_{A}\) toward \(Q_{D}\) )
    Shift left (in the direction \(Q_{D}\) toward \(Q_{A}\) )
    Inhibit clock (do nothing)
    Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flipflops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

    Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.
    Clocking of the flip-flop is inhibited when both mode control inputs are low.

    \section*{Features}
    - Parallel inputs and outputs
    - Four operating modes: Synchronous parallel load Right shift Left shift Do nothing
    - Positive edge-triggered clocking

    ■ Direct overriding clear
    - Typical clock frequency 105 MHz
    - Typical power dissipation 425 mW

    \section*{Connection Diagram}
    

    TL/F/6475-1

    Order Number DM54S194J or DM74S194N See NS Package Number J16A or N16E

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    5.5 V

    Operating Free Air Temperature Range
    DM54S
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    Storage Temperature Range

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|r|}{\multirow{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54S194} & \multicolumn{3}{|c|}{DM74S194} & \multirow{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
    \hline \({ }_{\mathrm{OH}}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -1 & & & -1 & mA \\
    \hline lol & \multicolumn{2}{|l|}{Low Level Output Current} & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 1)} & 0 & 105 & 70 & 0 & 105 & 70 & MHz \\
    \hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & 90 & 60 & 0 & 90 & 60 & MHz \\
    \hline \multirow[t]{2}{*}{tw} & \multirow[t]{2}{*}{Pulse Width (Note 3)} & Clock & 7 & & & 7 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Clear & 12 & & & 12 & & & \\
    \hline \multirow[t]{2}{*}{\({ }^{\text {t }}\) U} & \multirow[t]{2}{*}{Setup Time (Note 3)} & Mode & 11 & & & 11 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Data & 5 & & & 5 & & & \\
    \hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Hold Time (Note 3)} & 3 & & & 3 & & & ns \\
    \hline \(t_{\text {REL }}\) & \multicolumn{2}{|l|}{Clear Release Time (Note 3)} & 9 & & & 9 & & & ns \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note 1: \(C_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 2: \(C_{L}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{C C}=5 \mathrm{~V}\).
    Note 3: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \begin{tabular}{l}
    Typ \\
    (Note 4)
    \end{tabular} & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\
    & V_{I L}=M a x, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=M a x
    \] \\
    (Note 5)
    \end{tabular}} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 6)} & & 85 & 135 & mA \\
    \hline
    \end{tabular}

    Note 4: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 6: With all outputs open, inputs A through D grounded, and 4.5 V applied to \(\mathrm{SO}, \mathrm{S} 1, \mathrm{CLEAR}\), and the SERIAL inputs, \(\mathrm{I}_{\mathrm{CC}}\) is tested with a momentary ground, then 4.5 V applied to CLOCK.

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 70 & & 60 & & MHz \\
    \hline \({ }_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{aligned}
    & \text { Clock } \\
    & \text { to Q } \\
    & \hline
    \end{aligned}
    \] & & 12 & & 15 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \text { Clock } \\
    \text { to } \mathrm{Q} \\
    \hline
    \end{gathered}
    \] & & 16.5 & & 20 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
    Clear \\
    to Q
    \end{tabular} & & 18.5 & & 23 & ns \\
    \hline
    \end{tabular}

    Function Table
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{10}{|c|}{Inputs} & \multicolumn{4}{|c|}{Outputs} \\
    \hline \multirow[t]{2}{*}{Clear} & \multicolumn{2}{|c|}{Mode} & \multirow[t]{2}{*}{Clock} & \multicolumn{2}{|c|}{Serial} & \multicolumn{4}{|c|}{Parallel} & \multirow[t]{2}{*}{\(a_{A}\)} & \multirow[t]{2}{*}{\(Q_{B}\)} & \multirow[t]{2}{*}{\(Q_{C}\)} & \multirow[t]{2}{*}{\(Q_{\text {D }}\)} \\
    \hline & S1 & so & & Left & Right & A & B & c & D & & & & \\
    \hline L & X & X & X & X & X & X & X & X & X & L & L & L & L \\
    \hline H & X & X & L & X & X & X & X & x & x & \(Q_{A 0}\) & \(Q_{B 0}\) & \(Q_{\text {co }}\) & \(Q_{\text {D }}\) \\
    \hline H & H & H & \(\uparrow\) & x & X & a & b & c & d & a & b & c & d \\
    \hline H & L & H & \(\uparrow\) & x & H & x & X & x & x & H & \(Q_{\text {An }}\) & \(\mathrm{Q}_{\mathrm{Bn}}\) & \(Q_{\text {cn }}\) \\
    \hline H & L & H & \(\uparrow\) & X & x & X & \(x\) & x & x & L & \(Q_{\text {An }}\) & \(Q_{B n}\) & \(Q_{\text {cn }}\) \\
    \hline H & H & L & \(\uparrow\) & H & x & X & \(x\) & X & x & \(\mathrm{Q}_{\mathrm{Bn}}\) & \(Q_{C n}\) & \(Q_{\text {Dn }}\) & H \\
    \hline H & H & L & \(\uparrow\) & L & X & X & x & x & \(x\) & \(\mathrm{Q}_{\mathrm{Bn}}\) & \(Q_{\text {cn }}\) & \(Q_{\text {D }}\) & L \\
    \hline H & L & L & X & x & X & X & X & x & X & \(Q_{A 0}\) & \(\mathrm{Q}_{\mathrm{B} 0}\) & \(Q_{\mathrm{c} 0}\) & \(Q_{D 0}\) \\
    \hline
    \end{tabular}
    \(H=\) High Level (steady state). \(L=\) Low Level (steady state). \(X=\) Don't Care (any input, including transitions).
    \(\uparrow=\) Transition from low to high level.
    \(a, b, c, d=\) The level of steady state input at inputs \(A, B, C\), or \(D\), respectively.
    \(Q_{A 0}, Q_{B 0}, Q_{C 0}, Q_{D 0}=\) The level of \(Q_{A}, Q_{B}, Q_{C}\), or \(Q_{D}\), respectively, before the indicated steady state input conditions were established.
    \(Q_{A n}, Q_{\mathrm{Bn}}, Q_{\mathrm{Cn}}, Q_{D n}=\) The level of \(Q_{A}, Q_{B}, Q_{C}\) respectively, before the most recent \(\uparrow\) transition of the clock.
    Logic Diagram
    

    TL/F/6475-2

    \section*{Timing Diagram}

    Typical Clear, Load, Right-Shift, Left-Shift, Inhibit, and Clear Sequences
    

    \section*{DM54S195/DM74S195 4-Bit Parallel Access Shift Registers}

    \section*{General Description}

    These 4-bit registers feature parallel inputs, parallel outputs, \(J-\bar{K}\) serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

    Parallel (broadside) load
    Shift (in the direction \(Q_{A}\) toward \(Q_{D}\) )
    Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.
    Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the \(J-\bar{K}\) inputs. These inputs permit the first stage to perform as a \(J-\bar{K}, D\), or \(T\)-type flip-flop as shown in the truth table.

    The high-performance S195, with a 105 MHz typical shift frequency, is particularly attractive for very high-speed data processing systems. In most cases existing systems can be upgraded merely by using this Schottky-clamped shift register.

    \section*{Features}

    ■ Synchronous parallel load
    - Positive-edge-triggered clocking
    - Parallel inputs and outputs from each flip-flop
    - Direct overriding clear
    - \(J\) and \(\bar{K}\) inputs to first stage
    - Complementary outputs from last stage
    - For use in high-performance: accumulators/processors serial-to-parallel, parallel-to-serial converters
    - Typical clock frequency 105 MHz
    - Typical power dissipation 350 mW

    \section*{Connection Diagram}
    
    ```

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for avallability and specifications.
    Supply Voltage
    7V
    Input Voltage
    5.5V
    Operating Free Air Temperature Range

    | DM54S | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
    | :--- | ---: |
    | DM74S | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
    | Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

    ```

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54S195} & \multicolumn{3}{|c|}{DM74S195} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{C C}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
    \hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -1 & & & -1 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 1)} & 0 & 105 & 70 & 0 & 105 & 70 & MHz \\
    \hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & 90 & 60 & 0 & 90 & 60 & MHz \\
    \hline \multirow[t]{2}{*}{\(t_{W}\)} & \multirow[t]{2}{*}{Pulse Width (Note 3)} & Clock & 7 & & & 7 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Clear & 12 & & & 12 & & & \\
    \hline \multirow[t]{2}{*}{\({ }^{\text {tsu }}\)} & \multirow[t]{2}{*}{Setup Time (Note 3)} & Shift/Load & 11 & & & 11 & & & \multirow[t]{2}{*}{ns} \\
    \hline & & Data & 5 & & & 5 & & & \\
    \hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Data Hold Time (Note 3)} & 3 & & & 3 & & & ns \\
    \hline \multirow[t]{2}{*}{\(\mathrm{t}_{\text {REL }}\)} & \multicolumn{2}{|l|}{Shift/Load Release Time (Note 3)} & 6 & & & 6 & & & s \\
    \hline & \multicolumn{2}{|l|}{Clear Release Time (Note 3)} & 9 & & & 9 & & & \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note 1: \(C_{L}=15 \mathrm{pF}, R_{L}=280 \Omega, T_{A}=25^{\circ} \mathrm{C}\) and \(V_{C C}=5 \mathrm{~V}\).
    Note 2: \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 3: \(T_{A}=25^{\circ} \mathrm{C}\) and \(V_{C C}=5 \mathrm{~V}\).
    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 4) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O H}=\operatorname{Max} \\
    & V_{\mathrm{IL}}=\operatorname{Max}, V_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 5) }
    \end{aligned}
    \]} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}\) (Note 6)} & & 70 & 109 & mA \\
    \hline
    \end{tabular}

    Note 4: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 6: With all inputs open, SHIFT/LOAD grounded, and 4.5 V applied to the \(\mathrm{J}, \mathrm{K}\), and data inputs, I CC is measured by applying a momentary ground, then 4.5 V to the CLEAR and then applying a momentary ground then 4.5 V to the CLOCK.

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & 70 & & 60 & & MHz \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Any Q & & 12 & & 15 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Any Q & & 16.5 & & 20 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clear to Any Q & & 18.5 & & 23 & ns \\
    \hline
    \end{tabular}

    Function Table
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{9}{|c|}{Inputs} & \multicolumn{5}{|c|}{Outputs} \\
    \hline \multirow[t]{2}{*}{Clear} & \multirow[t]{2}{*}{\begin{tabular}{l}
    Shift/ \\
    Load
    \end{tabular}} & \multirow[t]{2}{*}{Clock} & \multicolumn{2}{|c|}{Serial} & \multicolumn{4}{|c|}{Parallel} & \multirow[t]{2}{*}{\(Q_{A}\)} & \multirow{2}{*}{\(Q_{B}\)} & \multirow{2}{*}{\(Q_{C}\)} & \multirow[t]{2}{*}{\(Q_{D}\)} & \multirow[t]{2}{*}{\(\overline{\mathbf{Q}}_{\mathbf{D}}\)} \\
    \hline & & & J & \(\overline{\mathbf{K}}\) & A & B & C & D & & & & & \\
    \hline L & X & X & X & X & X & X & X & X & L & L & L & L & H \\
    \hline H & L & \(\uparrow\) & X & X & a & b & c & d & a & b & c & d & \(\bar{d}\) \\
    \hline H & H & L & X & X & X & X & X & X & \(Q_{\text {A }}\) & \(Q_{B 0}\) & \(Q_{C 0}\) & \(Q_{\text {DO }}\) & \(\overline{\mathrm{Q}}_{\mathrm{DO}}\) \\
    \hline H & H & \(\uparrow\) & L & H & X & X & X & X & \(Q_{A 0}\) & \(Q_{\text {A0 }}\) & \(Q_{B n}\) & \(Q_{C n}\) & \(\bar{Q}_{C n}\) \\
    \hline H & H & \(\uparrow\) & L & L & X & X & X & X & L & \(Q_{A n}\) & \(Q_{B n}\) & \(Q_{C n}\) & \(\bar{Q}_{C n}\) \\
    \hline H & H & \(\uparrow\) & H & H & X & X & X & X & H & \(Q_{A n}\) & \(Q_{B n}\) & \(Q_{C n}\) & \(\bar{Q}_{\mathrm{C}}\) \\
    \hline H & H & \(\uparrow\) & H & L & X & X & X & X & \(\bar{Q}_{\text {An }}\) & \(Q_{\text {An }}\) & \(Q_{B n}\) & \(Q_{C n}\) & \(\bar{Q}_{C n}\) \\
    \hline
    \end{tabular}
    \(H=\) High Level (steady state), \(L=\) Low Level (steady state), \(X=\) Don't Care (any input, including transitions)
    \(\uparrow=\) Transition from low to high level
    \(a, b, c, d=\) The level of steady state input at \(A, B, C\), or \(D\), respectively.
    \(Q_{A O}, Q_{B 0}, Q_{C 0}, Q_{D O}=\) The level of \(Q_{A}, Q_{B}, Q_{C}\), or \(Q_{D}\), respectively, before the indicated steady state input conditions were established.
    \(Q_{A n}, Q_{B n}, Q_{C n}=\) The level of \(Q_{A}, Q_{B}, Q_{C}\), respectively, before the most recent transition of the clock.

    \section*{Logic Diagram}
    

    Timing Diagram
    

    TL/F/6476-3

    \section*{DM54S240/DM74S240, DM54S241/DM74S241, DM54S244/DM74S244 Octal TRI-STATE \({ }^{\circledR}\) Buffers/Line Drivers/Line Receivers}

    \section*{General Description}

    These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE buffers/ drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs, and can be used to drive terminated lines down to \(133 \Omega\).

    \section*{Features}
    - TRI-STATE outputs drive bus lines directly
    - PNP inputs reduce DC loading on bus lines
    - Hysteresis at data inputs improves noise margins
    - Typical lol (sink current) 54 S 48 mA 74S 64 mA
    - Typical \(\mathrm{I}_{\mathrm{OH}}\) (source current)

    54S - 12 mA
    74S - 15 mA
    - Typical propagation delay times Inverting 4.5 ns Noninverting 6 ns
    - Typical enable/disable times 9 ns
    - Typical power dissipation (enabled) Inverting 450 mW Noninverting 538 mW

    \section*{Connection Diagrams}

    Dual-In-Line Package
    

    TL/F/6478-1
    Order Number DM54S240J, DM74S240WM or DM74S240N See NS Package Number J20A, M20B or N20A

    Dual-In-Line Package
    

    TL/F/6478-2
    Order Number DM54S241J
    or DM74S241N
    See NS Package Number J20A or N20A

    Dual-In-Line Package
    

    Order Number DM54S244J, DM74S244WM or DM74S244N

    See NS Package Number J20A, M20B or N20A

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    \begin{tabular}{lr} 
    Supply Voltage & 7 V \\
    Input Voltage & 5.5 V \\
    Operating Free Air Temperature Range & \\
    DM54S & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S} & \multicolumn{3}{|c|}{DM74S} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Typ & Max & Min & Typ & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.5 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline lOH & High Level Output Current & & & -12 & & & -15 & mA \\
    \hline lOL & Low Level Output Current & & & 48 & & & 64 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{3}{|c|}{Conditions} & Min & \begin{tabular}{l}
    Typ \\
    (Note 1)
    \end{tabular} & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \(\mathrm{H}_{\mathrm{ys}}\) & Hysteresis ( \(\mathrm{V}_{\mathrm{T}+}-\mathrm{V}_{\mathrm{T}-}\) ) (Data Inputs Only) & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}\)} & 0.2 & 0.4 & & V \\
    \hline \multirow[t]{3}{*}{V OH} & \multirow[t]{3}{*}{High Level Output Voltage} & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=4.75 \mathrm{~V}, \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V}, \mathrm{I}_{\mathrm{OH}}=-1 \mathrm{~mA}
    \end{aligned}
    \]} & DM74 & 2.7 & & & \\
    \hline & & \multicolumn{3}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V}, \mathrm{I}_{\mathrm{OH}}=-3 \mathrm{~mA}
    \end{aligned}
    \]} & 2.4 & 3.4 & & V \\
    \hline & & \multicolumn{3}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.5 \mathrm{~V}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}
    \end{aligned}
    \]} & 2 & & & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{2}{*}{Low Level Output Voltage} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min} \quad \mathrm{I}_{\mathrm{OL}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V}, \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}
    \end{aligned}
    \]}} & DM54 & & & 0.55 & \\
    \hline & & & & DM74 & & & 0.55 & \\
    \hline IozH & Off-State Output Current, High Level Voltage Applied & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=M a x \\
    & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}
    \end{aligned}
    \]} & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline Iozl & Off-State Output Current, Low Level Voltage Applied & & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{O}}=0.5 \mathrm{~V}\)} & & & -50 & \(\mu \mathrm{A}\) \\
    \hline 1 & Input Current at Maximum Input Voltage & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \quad \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{3}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \quad \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\(V_{C C}=M a x\)} & \multirow[t]{2}{*}{\(\mathrm{V}_{1}=0.5 \mathrm{~V}\)} & Any A & & & -400 & \(\mu \mathrm{A}\) \\
    \hline & & & & Any G & & & -2 & mA \\
    \hline
    \end{tabular}

    \section*{Electrical Characteristics}
    over recommended operating free-air temperature range (unless otherwise noted) (Continued)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 2)} & -50 & & -225 & mA \\
    \hline \multirow[t]{12}{*}{Icc} & \multirow[t]{12}{*}{Supply Current} & \multirow[t]{4}{*}{Outputs High} & DM54S240 & & 80 & 123 & \multirow{12}{*}{mA} \\
    \hline & & & DM74S240 & & 80 & 135 & \\
    \hline & & & DM54S241, 244 & & 95 & 147 & \\
    \hline & & & DM74S241, 244 & & 95 & 160 & \\
    \hline & & \multirow[t]{4}{*}{Outputs Low} & DM54S240 & & 100 & 145 & \\
    \hline & & & DM74S240 & & 100 & 150 & \\
    \hline & & & DM54S241, 244 & & 120 & 170 & \\
    \hline & & & DM74S241, 244 & & 120 & 180 & \\
    \hline & & \multirow[t]{4}{*}{\begin{tabular}{l}
    Outputs \\
    Disabled
    \end{tabular}} & DM54S240 & & 100 & 145 & \\
    \hline & & & DM74S240 & & 100 & 150 & \\
    \hline & & & DM54S241, 244 & & 120 & 170 & \\
    \hline & & & DM74S241, 244 & & 120 & 180 & \\
    \hline
    \end{tabular}

    Note 1: All typical values are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time and duration should not exceed one second.
    Switching Characteristics \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow[t]{3}{*}{\begin{tabular}{l}
    Symbol \\
    \(t_{\text {PLH }}\)
    \end{tabular}} & \multirow[t]{3}{*}{\begin{tabular}{c} 
    Parameter \\
    \hline Propagation Delay Time \\
    Low to High Level Output
    \end{tabular}} & \multicolumn{2}{|r|}{Conditions} & \multirow[t]{2}{*}{\[
    \begin{gathered}
    \text { Min } \\
    \hline 2
    \end{gathered}
    \]} & \multirow[t]{2}{*}{\[
    \begin{gathered}
    \hline \text { Max } \\
    \hline 7 \\
    \hline
    \end{gathered}
    \]} & \multirow[t]{3}{*}{\begin{tabular}{l}
    Units \\
    ns
    \end{tabular}} \\
    \hline & & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{C}_{\mathrm{L}}=45 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=90 \Omega
    \end{aligned}
    \]} & DM54/74S240 & & & \\
    \hline & & & DM54/74S241, 244 & 2 & 9 & \\
    \hline \multirow[t]{2}{*}{tPHL} & \multirow[t]{2}{*}{Propagation Delay Time High to Low Level Output} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & C_{\mathrm{L}}=45 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=90 \Omega
    \end{aligned}
    \]} & DM54/74S240 & 2 & 7 & ns \\
    \hline & & & DM54/74S241, 244 & 2 & 9 & \\
    \hline \multirow[t]{2}{*}{\({ }_{\text {tPZL }}\)} & \multirow[t]{2}{*}{Output Enable Time to Low Level} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{C}_{\mathrm{L}}=45 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=90 \Omega
    \end{aligned}
    \]} & DM54/74S240 & 3 & 15 & ns \\
    \hline & & & DM54/74S241, 244 & 3 & 15 & \\
    \hline \multirow[t]{2}{*}{\(t_{\text {PZH }}\)} & \multirow[t]{2}{*}{Output Enable Time to High Level} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & C_{L}=45 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=90 \Omega
    \end{aligned}
    \]} & DM54/74S240 & 2 & 10 & ns \\
    \hline & & & DM54/74S241, 244 & 3 & 12 & \\
    \hline \multirow[t]{2}{*}{\({ }_{\text {t }}\) LZ} & \multirow[t]{2}{*}{Output Disable Time from Low Level} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & C_{\mathrm{L}}=5 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=90 \Omega
    \end{aligned}
    \]} & DM54/74S240 & 4 & 15 & ns \\
    \hline & & & DM54/74S241, 244 & 2 & 15 & \\
    \hline \multirow[t]{2}{*}{\(\mathrm{t}_{\text {PHZ }}\)} & \multirow[t]{2}{*}{Output Disable Time from High Level} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & C_{L}=5 \mathrm{pF} \\
    & R_{\mathrm{L}}=90 \Omega
    \end{aligned}
    \]} & DM54/74S240 & 2 & 9 & ns \\
    \hline & & & DM54/74S241, 244 & 2 & 9 & \\
    \hline \multirow[t]{2}{*}{\(t_{\text {PLH }}\)} & \multirow[t]{2}{*}{Propagation Delay Time Low to High Level Output} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & C_{\mathrm{L}}=150 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=90 \Omega
    \end{aligned}
    \]} & DM54/74S240 & 3 & 10 & ns \\
    \hline & & & DM54/74S241, 244 & 4 & 12 & \\
    \hline \multirow[t]{2}{*}{\({ }^{\text {tpHL }}\)} & \multirow[t]{2}{*}{Propagation Delay Time High to Low Level Output} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & C_{\mathrm{L}}=150 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=90 \Omega
    \end{aligned}
    \]} & DM54/74S240 & 3 & 10 & ns \\
    \hline & & & DM54/74S241, 244 & 4 & 12 & \\
    \hline \multirow[t]{2}{*}{\(t_{\text {PZL }}\)} & \multirow[t]{2}{*}{Output Enable Time to Low Level} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & C_{\mathrm{L}}=150 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=90 \Omega
    \end{aligned}
    \]} & DM54/74S240 & 6 & 21 & ns \\
    \hline & & & DM54/74S241, 244 & 6 & 21 & \\
    \hline \multirow[t]{2}{*}{tPZH} & \multirow[t]{2}{*}{Output Enable Time to High Level} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & C_{L}=150 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=90 \Omega
    \end{aligned}
    \]} & DM54/74S240 & 4 & 12 & ns \\
    \hline & & & DM54/74S241, 244 & 4 & 15 & \\
    \hline
    \end{tabular}

    \section*{DM54S251/DM74S251 TRI-STATE® 1 of 8 Line Data Selector/Multiplexer}

    \section*{General Description}

    These data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources, and feature a strobe-controlled TRI-STATE output. The strobe must be at a low logic level to enable these devices. The TRI-STATE outputs permit direct connection to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totempole outputs.
    To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

    \section*{Connection Diagram}

    TL/F/6480-1
    Order Number DM54S251J or DM74S251N See NS Package Number J16A or N16E
    
    \(-1\)

    \section*{Features}
    - TRI-STATE version of S151
    - Interface directly with system bus
    - Perform parallel-to-serial conversion
    - Permit multiplexing from N -lines to one line
    - Complementary outputs provide true and inverted data
    - Max no. of common outputs

    54S 39
    74S 129
    - Typical propagation delay time ( D to Y ) 8 ns
    - Typical power dissipation 275 mW

    Function Table
    \begin{tabular}{|ccc|c|cc|}
    \hline \multicolumn{4}{c|}{ Inputs } & \multicolumn{2}{c|}{ Outputs } \\
    \hline \multicolumn{3}{|c|}{ Select } & Strobe & Y & W \\
    \cline { 1 - 3 } C & B & A & S & & \\
    \hline X & X & X & H & Z & Z \\
    L & L & L & L & D0 & \(\overline{\text { D0 }}\) \\
    L & L & H & L & D1 & \(\overline{\text { D1 }}\) \\
    L & H & L & L & D2 & \(\overline{\text { D2 }}\) \\
    L & H & H & L & D3 & \(\overline{\text { D3 }}\) \\
    H & L & L & L & D4 & \(\overline{\text { D4 }}\) \\
    H & L & H & L & D5 & \(\overline{\text { D5 }}\) \\
    H & H & L & L & D6 & \(\overline{D 6}\) \\
    H & H & H & L & D7 & \(\overline{\text { D7 }}\) \\
    \hline
    \end{tabular}
    \(H=\) High Logic Level, L = Low Logic Level
    X = Don't Care, \(\mathbf{Z}=\) High Impedance (Off)
    D0, D1 \(\ldots\) D7 = The Level of the respective \(D\) input
    \begin{tabular}{lr} 
    Absolute Maximum Ratings (Note) \\
    If Military/Aerospace specified devices are required, \\
    please contact the National Semiconductor Sales \\
    Office/Distributors for availability and specifications. \\
    Supply Voltage & 7 V \\
    Input Voltage & 5.5 V \\
    Operating Free Air Temperature Range & \\
    DM54S & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S251} & \multicolumn{3}{|c|}{DM74S251} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{\text {l }}\) & High Level Output Current & & & -2 & & & -6.5 & mA \\
    \hline \(\mathrm{lOL}^{\text {l }}\) & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
    \begin{aligned}
    & \text { Typ } \\
    & \text { (Note 1) }
    \end{aligned}
    \] & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.4 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.4 & 3.2 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O L}=M a x \\
    & V_{\mathrm{IH}}=\operatorname{Min}, V_{\mathrm{IL}}=M a x
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline 1 IH & High Level Input & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline ILL & Low Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline lozH & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Max}, V_{\mathrm{O}}=2.4 \\
    & V_{\mathrm{IH}}=\operatorname{Min}, V_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline lozl & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M a x, V_{O}=0.5 \\
    & V_{I H}=M i n, V_{I L}=M a x
    \end{aligned}
    \]} & & & -50 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=M a x
    \] \\
    (Note 2)
    \end{tabular}} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 3)} & & 55 & 85 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: \(\mathrm{ICC}_{\mathrm{CC}}\) is measured with the outputs open and all inputs at 4.5 V .
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{8}{|l|}{Switching Characteristics at \(\mathrm{V}_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)} \\
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    \text { A, B, or C } \\
    (4 \text { Levels }) \text { to } Y
    \end{gathered}
    \] & & 18 & & 21 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \text { A, B, or C } \\
    (4 \text { Levels) to } Y
    \end{gathered}
    \] & & 19.5 & & 23 & ns \\
    \hline \({ }^{\text {tpLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    \text { A, B, or C } \\
    \text { (3 Levels) to W } \\
    \hline
    \end{gathered}
    \] & & 15 & & 18 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \text { A, B, or C } \\
    \text { (3 Levels) to W }
    \end{gathered}
    \] & & 13.5 & & 17 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \(D\) to Y & & 12 & & 15 & ns \\
    \hline \({ }^{\text {tpHL }}\) & Propagation Delay Time High to Low Level Output & D to Y & & 12 & & 15 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & D to W & & 7 & & 10 & ns \\
    \hline \({ }_{\text {tPHL }}\) & Propagation Delay Time High to Low Level Output & D to W & & 7 & & 10 & ns \\
    \hline \(t_{\text {PZH }}\) & Output Enable Time to High Level Output & Strobe to \(Y\) & & & & 19.5 & ns \\
    \hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level Output & Strobe to \(Y\) & & & & 21 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time to High Level Output (Note 1) & Strobe to \(Y\) & & 8.5 & & & ns \\
    \hline \(t_{\text {PLZ }}\) & Output Disable Time to Low Level Output (Note 1) & Strobe to \(Y\) & & 14 & & & ns \\
    \hline tPZH & Output Enable Time to High Level Output & Strobe to W & & & & 19.5 & ns \\
    \hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level Output & Strobe to W & & & & 21 & ns \\
    \hline \(t_{\text {PHZ }}\) & \begin{tabular}{l}
    Output Disable Time \\
    to High Level Output (Note 1)
    \end{tabular} & Strobe to W & & 8.5 & & & ns \\
    \hline \(t_{\text {PLZ }}\) & \begin{tabular}{l}
    Output Disable Time \\
    to Low Level Output (Note 1)
    \end{tabular} & Strobe to W & & 14 & & & ns \\
    \hline
    \end{tabular}

    Note 1: \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\).

    \section*{Logic Diagram}
    

    \section*{DM54S253/DM74S253}

    Dual TRI-STATE \({ }^{\circledR} 1\) of 4 Line Data Selectors/Multiplexers

    \section*{General Description}

    Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.
    The TRI-STATE outputs can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enable output will drive the bus line to a high or low logic level.

    \section*{Features}
    - TRI-STATE version of S153 with same pin-out

    ■ Schottky-diode-clamped transistors
    - Permits multiplexing from \(N\) lines to 1 line
    - Performs parallel-T-serial conversion
    - Strobe/output control
    - High fan-out totem-pole outputs
    - Typical propagation delay

    From data to output 6 ns
    From select to output 12 ns
    - Typical power dissipation 275 mW

    \section*{Connection Diagram}

    Dual-In-Line Package
    

    TL/F/6481-1
    Order Number DM54S253J, DM54S253W or DM74S253N NS Package Number J16A, N16E or W16A

    \section*{Function Table}
    \begin{tabular}{|cc|cccc|c|c|}
    \hline \begin{tabular}{c} 
    Select \\
    Inputs
    \end{tabular} & \multicolumn{4}{|c|}{ Data Inputs } & \begin{tabular}{c} 
    Output \\
    Control
    \end{tabular} & Output \\
    \hline B & A & C0 & C1 & C2 & C3 & G & Y \\
    \hline X & X & X & X & X & X & H & Z \\
    L & L & L & X & X & X & L & L \\
    L & L & H & X & X & X & L & H \\
    L & H & X & L & X & X & L & L \\
    L & H & X & H & X & X & L & H \\
    H & L & X & X & L & X & L & L \\
    H & L & X & X & H & X & L & H \\
    H & H & X & X & X & L & L & L \\
    H & H & X & X & X & H & L & H \\
    \hline
    \end{tabular}

    Address inputs \(A\) and \(B\) are common to both sections. \(H=\) High Level, \(L=\) Low Level, \(X=\) Don't Care, \(Z=\) High Impedance

    \section*{Absolute Maximum Ratings (Note)}

    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    5.5 V

    Operating Free Air Temperature Range
    \begin{tabular}{lr} 
    DM54S & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S253} & \multicolumn{3}{|c|}{DM74S253} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -2 & & & -6.5 & mA \\
    \hline lOL & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Condlitions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{VOH} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.4 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.4 & 3.2 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, \mathrm{IOL}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{IH}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline ILL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline IozH & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline Iozl & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{\mathrm{O}}=0.5 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & -50 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & (\text { Note 2) }
    \end{aligned}
    \]} & DM54 & -40 & & \(-100\) & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline Icc & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}\) (Note 3)} & & 55 & 70 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: \(\mathrm{ICC}_{\mathrm{CC}}\) is measured with all outputs open.
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & & pF & & pF & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Data to \(Y\) & & 9 & & 12 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to \(Y\) & & 9 & & 12 & ns \\
    \hline \({ }_{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & Select to \(Y\) & & 18 & & 21 & ns \\
    \hline tPHL & Propagation Delay Time High to Low Level Output & Select to \(Y\) & & 18 & & 21 & ns \\
    \hline \(t_{\text {PZH }}\) & Output Enable Time to High Level Output & Output Control to \(Y\) & & 16.5 & & 19.5 & ns \\
    \hline \(t_{P Z L}\) & Output Enable Time to Low Level Output & Output Control to \(Y\) & & 18 & & 21 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time to High Level Output (Note 1) & Output Control to Y & & 9.5 & & & ns \\
    \hline \(t_{\text {PLZ }}\) & Output Disable Time to Low Level Output (Note 1) & Output Control to \(Y\) & & 15 & & & ns \\
    \hline
    \end{tabular}

    Note 1: \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\).

    \section*{Logic Diagram}
    

    \section*{DM54S257/DM74S257, DM54S258/DM74S258 TRI-STATE \({ }^{\circledR}\) Quad 1 of 2 Data Selectors/Multiplexers}

    \section*{General Description}

    These Schottky-clamped high-performance multiplexers feature TRI-STATE outputs that can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output enable circuitry is designed such that the output disable times are shorter than the output enable times.
    This TRI-STATE output feature means that n -bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

    \section*{Features}
    - TRI-STATE versions S157, S158, with same pin-outs
    - Schottky-clamped for significant improvement in A-C performance
    - Provides bus interface from multiple sources in highperformance systems
    - Average propagation delay from data input

    S257 4.8 ns
    S258 4 ns
    - Typical power dissipation

    S257 320 mW
    S258 280 mW

    \section*{Connection Diagrams}
    

    Dual-In-Line Package
    

    TL/F/6482-1
    TL/F/6482-2
    Order Number DM54S257J, DM54S258J, DM54S257W, DM74S257N or DM74S258N See NS Package Number J16A, N16E or W16A

    \section*{Function Table}
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multicolumn{4}{|c|}{ Inputs } & \multicolumn{3}{c|}{ Output Y } \\
    \hline \begin{tabular}{c} 
    Output \\
    Control
    \end{tabular} & Select & A & B & S257 & S258 \\
    \hline H & X & X & X & Z & Z \\
    L & L & L & X & L & H \\
    L & L & H & X & H & L \\
    L & H & X & L & L & H \\
    L & H & X & H & H & L \\
    \hline
    \end{tabular}

    \footnotetext{
    H = High Level, L = Low Level, X = Don't Care
    Z = High Impedance (off)
    }

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    \begin{tabular}{lr} 
    Supply Voltage & 7 V \\
    Input Voltage & 5.5 V \\
    Operating Free Air Temperature Range & \\
    DM54S & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S257} & \multicolumn{3}{|c|}{DM74S257} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline lOH & High Level Output Current & & & -2 & & & -6.5 & mA \\
    \hline IOL & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    \section*{'S257 Electrical Characteristics}
    over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.4 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.4 & 3.2 & & \\
    \hline VOL & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O L}=M a x \\
    & V_{I H}=M i n, V_{I L}=M a x
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\) Max, \(\mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \multirow[t]{2}{*}{\(\mathrm{I}_{\mathrm{H}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=2.7 V
    \end{aligned}
    \]} & Select & & & 100 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & Other & & & 50 & \\
    \hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{I}}=0.5 \mathrm{~V}
    \end{aligned}
    \]} & Select & & & -4 & \multirow[t]{2}{*}{mA} \\
    \hline & & & Other & & & -2 & \\
    \hline lozh & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M a x, V_{O}=2.4 V \\
    & V_{I H}=M i n, V_{I L}=M a x
    \end{aligned}
    \]} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline lozl & \begin{tabular}{l}
    Off-State Output Current with \\
    Low Level Output \\
    Voltage Applied
    \end{tabular} & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=0.5 \mathrm{~V} \\
    & V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
    \end{aligned}
    \]} & & & -50 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=M a x
    \] \\
    (Note 2)
    \end{tabular}} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}\) (Note 3)} & & 44 & 68 & mA \\
    \hline ICCL & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 3)} & & 60 & 93 & mA \\
    \hline Iccz & Supply Current with Outputs Disabled & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}\) (Note 3)} & & 64 & 99 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: ICC is measured with all outputs open and all possible inputs grounded, while achieving the stated output conditions.
    at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(R_{L}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Data to Output & & 7.5 & & 11 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to Output & & 6.5 & & 10 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Select to Output & & 15 & & 16 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Select to Output & & 15 & & 16 & ns \\
    \hline tpzH & Output Enable Time to High Level Output & Output Control to \(Y\) & & 19.5 & & 23 & ns \\
    \hline tpzL & Output Enable Time to Low Level Output & Output Control to \(Y\) & & 21 & & 24 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time to High Level Output (Note 1) & Output Control to \(Y\) & & 8.5 & & & ns \\
    \hline tplz & \begin{tabular}{l}
    Output Disable Time \\
    to Low Level Output (Note 1)
    \end{tabular} & Output Control to \(Y\) & & 14 & & & ns \\
    \hline
    \end{tabular}

    Note 1: \(C_{L}=5 \mathrm{pF}\).
    Recommended Operating Conditions
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S258} & \multicolumn{3}{|c|}{DM74S258} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline \({ }^{\mathrm{OH}}\) & High Level Output Current & & & -2 & & & -6.5 & mA \\
    \hline lOL & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    \section*{'S258 Electrical Characteristics}
    over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{VOH} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\
    & V_{I L}=\operatorname{Max}, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.4 & 3.4 & & \multirow[t]{2}{*}{V} \\
    \hline & & & DM74 & 2.4 & 3.2 & & \\
    \hline V \({ }_{\text {OL }}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, \mathrm{IOL}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \multirow[t]{2}{*}{\(\mathrm{I}_{\mathrm{IH}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, \\
    & V_{1}=2.7 V
    \end{aligned}
    \]} & Select & & & 100 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & Other & & & 50 & \\
    \hline \multirow[t]{2}{*}{IIL} & \multirow[t]{2}{*}{Low Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max} \\
    & V_{I}=0.5 V
    \end{aligned}
    \]} & Select & & & -4 & \multirow[t]{2}{*}{mA} \\
    \hline & & & Other & & & -2 & \\
    \hline
    \end{tabular}

    \section*{'S258 Electrical Characteristics}
    over recommended operating free air temperature (unless otherwise noted) (Continued)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline IOZH & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline lozl & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{O}}=0.5 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & -50 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\mathrm{Max} \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline \(\mathrm{I}^{\mathrm{CCH}}\) & Supply Current with Outputs High & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\text { Max } \\
    & (\text { Note 3) }
    \end{aligned}
    \]} & & 36 & 56 & mA \\
    \hline \({ }^{\text {CCCL }}\) & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\begin{tabular}{l}
    \[
    V_{C C}=\operatorname{Max}
    \] \\
    (Note 3)
    \end{tabular}} & & 52 & 81 & mA \\
    \hline ICCZ & Supply Current with Outputs Disabled & \multicolumn{2}{|l|}{\begin{tabular}{l}
    \[
    V_{C C}=M a x
    \] \\
    (Note 3)
    \end{tabular}} & & 56 & 87 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: ICC is measured with all outputs open and all possible inputs grounded, while achieving the stated output conditions.
    'S258 Switching Characteristics
    at \(V_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[t]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Data to Output & & 6 & & 9 & ns \\
    \hline tpHL & Propagation Delay Time High to Low Level Output & Data to Output & & 6 & & 9 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Select to Output & & 12 & & 15 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Select to Output & & 12 & & 15 & ns \\
    \hline \({ }_{\text {tPZH }}\) & Output Enable Time to High Level Output & Output Control to \(Y\) & & 19.5 & & 23 & ns \\
    \hline \(t_{P Z L}\) & Output Enable Time to Low Level Output & Output Control to \(Y\) & & 21 & & 24 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time to High Level Output (Note 1) & Output Control to Y & & 8.5 & & & ns \\
    \hline \(t_{\text {PLZ }}\) & \begin{tabular}{l}
    Output Disable Time \\
    to Low Level Output (Note 1)
    \end{tabular} & Output Control to \(Y\) & & 14 & & & ns \\
    \hline
    \end{tabular}

    Note 1: \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\).
    

    TL/F/6482-3
    

    TL/F/6482-4

    \section*{DM54S280/DM74S280 9-Bit Parity Generators/Checkers}

    \section*{General Description}

    These universal, nine-bit parity generators/checkers utilize Schottky-clamped TTL high-performance circuitry, and feature odd/even outputs to facilitate operation of either odd or even parity applications. The word-length capability is easily expanded by cascading.
    The S280 can be used to upgrade the performance of most systems utilizing the DM74180 parity generator/checker. Although the S280 is implemented without expander inputs, the corresponding function is provided by the availability of all input at pin 4, and no internal connection at pin 3. This permits the S280 to be substituted for the 180 in existing designs to produce an identical function, even if S280's are mixed with existing 180's.

    Input buffers are provided so that each input represents only one normal 74 S load, and full fan-out to 10 normal Series 74S loads is available from each of the outputs at low logic levels. A fan-out to 20 normal Series 74S loads is provided at high logic levels, to facilitate connection of unused inputs to used inputs.

    \section*{Features}
    - Generates either odd or even parity for nine data lines
    - Cascadable for N -bits
    - Can be used to upgrade existing systems using MSI parity circuits
    - Typical data-to-output delay-14 ns

    \section*{Connection Diagram}
    

    TL/F/6483-1
    Order Number DM54S280J, DM54S280W, DM74S280M or DM74S280N See NS Package Number J14A, M14A, N14A or W14B

    Function Table
    \begin{tabular}{|c|cc|}
    \hline \multirow{2}{*}{\begin{tabular}{c} 
    Number of Inputs (A \\
    Thru I) that are High
    \end{tabular}} & \multicolumn{2}{|c|}{ Outputs } \\
    \hline & इ Even \(\Sigma\) Odd \\
    \hline \(0,2,4,6,8\) & H & L \\
    \(1,3,5,7,9\) & L & H \\
    \hline
    \end{tabular}
    \begin{tabular}{lr} 
    Absolute Maximum Ratings (Note) \\
    If Military/Aerospace specified devices are required, \\
    please contact the National Semiconductor Sales \\
    Office/Distributors for availability and specifications. \\
    Supply Voltage & 7 V \\
    Input Voltage & 5.5 V \\
    Operating Free Air Temperature Range & \\
    DM54S & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
    DM74S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S280} & \multicolumn{3}{|c|}{DM74S280} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline IOH & High Level Output Current & & & -1 & & & -1 & mA \\
    \hline lOL & Low Level Output Current & & & 20 & & & 20 & mA \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O H}=\operatorname{Max} \\
    & V_{I L}=M a x, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & 2.7 & 3.4 & & V \\
    \hline VOL & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M a x, V_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline ILL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
    \[
    V_{C C}=\operatorname{Max}
    \] \\
    (Note 2)
    \end{tabular}} & DM54 & \(-40\) & & -100 & \multirow{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(V_{\text {CC }}\) Max (Note 3)} & & 67 & 105 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: \(I_{C C}\) is measured with all inputs grounded and all outputs open.

    Switching Characteristics at \(\mathrm{V}_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{From (Input) To (Output)} & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & R_{\mathrm{L}}=280 \Omega \\
    & \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}
    \end{aligned}
    \]} & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & R_{\mathrm{L}}=280 \Omega \\
    & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}
    \end{aligned}
    \]} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Data to \(\Sigma\) Even & & 21 & & 24 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
    Data to \\
    \(\Sigma\) Even
    \end{tabular} & & 18 & & 21 & ns \\
    \hline \({ }_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output & Data to \(\Sigma\) Odd & & 21 & & 24 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Data to \(\Sigma\) Odd & & 18 & & 21 & ns \\
    \hline
    \end{tabular}

    \section*{Logic Diagram}
    

    TL/F/6483-2

    Three S280's can be used to implement a 25 -line parity generator/checker. This arrangement will provide parity in typically 25 ns . (See Figure 1.)
    As an alternative, the outputs of two or three parity generators/checkers can be decoded with a 2-input (S86) or
    

    TL/F/6483-3
    FIGURE 1. 25-Line Parity/Generator Checker

    3-input (S135) exclusive-OR gate for 18 or 27 -line parity applications.
    Longer word lengths can be implemented by cascading S280's. As shown in Figure 2, parity can be generated for word lengths up to 81 bits in typically 25 ns .
    

    TL/F/6483-4
    FIGURE 2. 81-Line Parity/Generator Checker

    \section*{DM54S283/DM74S283 4-Bit Binary Adders with Fast Carry}

    \section*{General Description}

    These full adders perform the addition of two 4-bit binary numbers. The sum ( \(\Sigma\) ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial lookahead performance at the economy and reduced package count of a ripple-carry implementation.
    The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

    \section*{Features}
    - Full-carry look-ahead across the four bits
    - Systems achieve partial look-ahead performance with the economy of ripple carry
    - Typical add times

    Two 8-bit words 15 ns
    Two 16 -bit words 30 ns
    - Typical power dissipation 510 mW

    \section*{Connection Diagram}
    
    

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54S283} & \multicolumn{3}{|c|}{DM74S283} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(V_{C C}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & & & 0.8 & V \\
    \hline \multirow[t]{2}{*}{l OH} & High Level Output Current (Output C4) & & & -0.5 & & & -0.5 & \multirow[b]{2}{*}{mA} \\
    \hline & High Level Output Current (Other Outputs) & & & -1 & & & -1 & \\
    \hline \multirow[t]{2}{*}{lol} & Low Level Output Current (Output C4) & & & 10 & & & 10 & \multirow[b]{2}{*}{mA} \\
    \hline & Low Level Output Current (Other Outputs) & & & 20 & & & 20 & \\
    \hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min} \\
    & \mathrm{IOH}_{\mathrm{OH}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & DM54 & 2.5 & 3.4 & & \multirow[b]{2}{*}{V} \\
    \hline & & & DM74 & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O L}=M a x \\
    & V_{I H}=M i n, V_{I L}=M a x
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline \(\mathrm{L}_{\mathrm{L}}\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.5 \mathrm{~V}\)} & & & -2 & mA \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\text { Max } \\
    & \text { (Note 2) }
    \end{aligned}
    \]} & C4 Output & -20 & & -100 & \multirow[b]{2}{*}{mA} \\
    \hline & & & Other Outputs & -40 & & -100 & \\
    \hline \(\mathrm{ICC1}\) & Supply Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}\) (Note 3)} & & 80 & 120 & mA \\
    \hline ICC2 & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\operatorname{Max}\) (Note 4)} & & 95 & 160 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Note 3: \(\mathrm{I}_{\mathrm{CC} 1}\) is measured with all outputs open, all B inputs low and all other inputs at 4.5 V .
    Note 4: \(\mathrm{I}_{\mathrm{CC} 2}\) is measured with all outputs open and all inputs at 4.5 V .
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{8}{|l|}{Switching Characteristics at \(\mathrm{V}_{C C}=5 \mathrm{~V}\) and \(\mathrm{T}_{A}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)} \\
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[b]{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \({ }^{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    \mathrm{CO} \text { to } \\
    \Sigma 1 \text { or } \Sigma 2 \\
    \hline
    \end{gathered}
    \] & & 18 & & 20 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \mathrm{CO} \text { to } \\
    \Sigma 1 \text { or } \Sigma 2 \\
    \hline
    \end{gathered}
    \] & & 18 & & 20 & ns \\
    \hline \({ }^{\text {tpLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    \mathrm{CO} \text { to } \\
    \Sigma 3 \\
    \hline
    \end{gathered}
    \] & & 18 & & 20 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \mathrm{CO} \text { to } \\
    \Sigma 3 \\
    \hline
    \end{gathered}
    \] & & 18 & & 20 & ns \\
    \hline \({ }^{\text {tPLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    \mathrm{CO} \text { to } \\
    \Sigma 4 \\
    \hline
    \end{gathered}
    \] & & 18 & & 20 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \mathrm{CO} \text { to } \\
    \Sigma 4 \\
    \hline
    \end{gathered}
    \] & & 18 & & 20 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{aligned}
    & A_{i}, B_{i} \\
    & \text { to } S_{i}
    \end{aligned}
    \] & & 18 & & 20 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{aligned}
    & A_{i}, B_{i} \\
    & \text { to } S_{i} \\
    & \hline
    \end{aligned}
    \] & & 18 & & 20 & ns \\
    \hline tPLH & Propagation Delay Time Low to High Level Output (Note 1) & \[
    \begin{gathered}
    \mathrm{CO} \text { to } \\
    \Sigma 4 \\
    \hline
    \end{gathered}
    \] & & 11 & & 15 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output (Note 1) & \[
    \begin{gathered}
    \mathrm{CO} \text { to } \\
    \Sigma 4 \\
    \hline
    \end{gathered}
    \] & & 11 & & 15 & ns \\
    \hline \(t_{\text {tplH }}\) & Propagation Delay Time Low to High Level Output (Note 1) & \[
    \begin{aligned}
    & A_{i}, B_{i} \\
    & \text { to } C 4
    \end{aligned}
    \] & & 12 & & 16 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output (Note 1) & \[
    \begin{aligned}
    & \mathrm{A}_{\mathrm{i}}, \mathrm{~B}_{\mathrm{i}} \\
    & \text { to } \mathrm{C} 4 \\
    & \hline
    \end{aligned}
    \] & & 12 & & 16 & ns \\
    \hline
    \end{tabular}

    Note 1: \(\mathrm{R}_{\mathrm{L}}=560 \Omega\).
    Function Table
    (2)
    \(H=\) High Level, \(L=\) Low Level
    Note: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs \(\Sigma 1\) and \(\Sigma 2\) and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs \(\Sigma 3, \Sigma 4\), and C 4 .

    Logic Diagram
    

    TL/F/6484-2

    \section*{DM74S299}

    \section*{TRI-STATE \({ }^{\circledR}\) 8-Bit Universal Shift/Storage Registers}

    \section*{Description}

    This Schottky TTL eight-bit universal register features multiplexed inputs/outputs to achieve full eight bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.
    Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the TRI-STATE outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

    \section*{Features}

    ■ Multiplexed inputs/outputs provide improved bit density
    - Four modes of operation: Hold (Store) Shift Left Shift Right Load Data
    - TRI-STATE outputs drive bus lines directly
    - Can be cascaded for N -bit word lengths
    - Operates with outputs enabled or at high Z
    - Guaranteed shift (clock) frequency 50 MHz

    ■ Typical power dissipation 700 mW

    \section*{Connection Diagram}
    

    Order Number DM74S299N See NS Package Number N20A

    \section*{Absolute Maximum Ratings (Note)}

    \section*{If Military/Aerospace specifled devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.}

    Supply Voltage
    Input Voltage
    5.5 V

    Operating Free Air Temperature Range
    DM74S
    Storage Temperature Range
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|l|}{\multirow{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM74S299} & \multirow{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & \\
    \hline \(V_{\text {CC }}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{IOH}^{\text {l }}\)} & \multicolumn{2}{|l|}{High Level Output Current ( \(\mathrm{Q}_{\mathrm{A}}\) thru \(\mathrm{Q}_{H}\) )} & & & -6.5 & mA \\
    \hline & \multicolumn{2}{|l|}{High Level Output Current ( \(\mathrm{Q}_{\mathrm{A}^{\prime}}, \mathrm{Q}_{\mathrm{H}^{\prime}}\) )} & & & -0.5 & \\
    \hline \multirow[t]{2}{*}{loL} & \multicolumn{2}{|l|}{Low Level Output Current ( \(Q_{A}\) thru \(Q_{H}\) )} & & & 20 & mA \\
    \hline & \multicolumn{2}{|l|}{High Level Output Current ( \(Q_{A^{\prime}}, \mathrm{Q}_{H^{\prime}}\) )} & & & 6 & \\
    \hline fCLK & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & 70 & 50 & MHz \\
    \hline \(\mathrm{f}_{\text {CLK }}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 3)} & 0 & 60 & 40 & MHz \\
    \hline \multirow[t]{3}{*}{tw} & \multirow[t]{3}{*}{Pulse Width (Note 5)} & Clock High & 10 & & & \multirow{3}{*}{ns} \\
    \hline & & Clock Low & 10 & & & \\
    \hline & & Clear Low & 10 & & & \\
    \hline \multirow[t]{3}{*}{tsu} & \multirow[t]{3}{*}{Setup Time (Notes 4 \& 5)} & Select & \(15 \uparrow\) & & & \\
    \hline & & Data High & \(7 \uparrow\) & & & ns \\
    \hline & & Data Low & \(5 \uparrow\) & & & \\
    \hline \({ }_{\text {th }}\) & \multicolumn{2}{|l|}{Hold Time (Notes 4 \& 5)} & \(5 \uparrow\) & & & ns \\
    \hline \(t_{\text {REL }}\) & \multicolumn{2}{|l|}{Clear Release Time (Note 5)} & \(10 \uparrow\) & & & ns \\
    \hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note 1: The symbol ( \(\uparrow\) ) indicates the rising edge of the clock pulse is used for reference.
    Note 2: \(C_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 3: \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 4: Data includes the two serial inputs and the eight input/output data lines.
    Note 5: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOH}_{\mathrm{O}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \]} & \(Q_{A}\) thru \(Q_{H}\) & 2.4 & 3.2 & & \multirow[t]{2}{*}{V} \\
    \hline & & & \(Q_{A^{\prime}}, Q_{H^{\prime}}\) & 2.7 & 3.4 & & \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \multirow[t]{2}{*}{\(\mathrm{I}_{\mathrm{H}}\)} & \multirow[t]{2}{*}{High Level Input Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=2.7 V
    \end{aligned}
    \]} & \[
    \begin{aligned}
    & \text { A thru } \mathrm{H} \text {, } \\
    & \text { So, S1 } \\
    & \hline
    \end{aligned}
    \] & & & 100 & \(\mu \mathrm{A}\) \\
    \hline & & & Any Other & & & 50 & \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    over recommended operating free air temperature range (unless otherwise noted) (Continued)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \multirow[t]{3}{*}{IL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
    & \mathrm{~V}_{1}=0.5 \mathrm{~V}
    \end{aligned}
    \]} & Clock, Clear & & & -2 & \multirow{3}{*}{mA} \\
    \hline & & & S0, S1 & & & -0.5 & \\
    \hline & & & Other & & & -0.25 & \\
    \hline Iozh & Off-State Output Current with High Level Output Voltage Applied \(\left(\mathrm{Q}_{\mathrm{A}}\right.\) thru \(\left.\mathrm{Q}_{\mathrm{H}}\right)\) & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M a x, V_{O}=2.4 V \\
    & V_{I H}=M i n, V_{I L}=\operatorname{Max}
    \end{aligned}
    \]} & & & 100 & \(\mu \mathrm{A}\) \\
    \hline IozL & Off-State Output Current with Low Level Output Voltage Applied ( \(Q_{A}\) thru \(Q_{H}\) ) & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=0.5 \mathrm{~V} \\
    & V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
    \end{aligned}
    \]} & & & -250 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{los} & Short Circuit Output Current ( \(Q_{A}\) thru \(Q_{H}\) ) & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}\) (Note 2)} & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & Short Circuit Output Current ( \(\mathrm{Q}_{\mathrm{A}^{\prime}}, \mathrm{Q}_{\mathrm{H}^{\prime}}\) ) & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {CC }}=\mathrm{Max}\) (Note 2)} & -20 & & -100 & \\
    \hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 140 & 225 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{From (Input) To (Output)} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\) (Note 2)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & (Note 3) & 50 & & 40 & & MHz \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output (Note 2) & \[
    \begin{aligned}
    & \text { Clock to } \\
    & Q_{A^{\prime}} \text { or } \mathrm{Q}_{H^{\prime}}
    \end{aligned}
    \] & & 20 & & 22 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output (Note 2) & \[
    \begin{gathered}
    \text { Clock to } \\
    \mathrm{Q}_{\mathrm{A}^{\prime}} \text { or } \mathrm{Q}_{\mathrm{H}^{\prime}}
    \end{gathered}
    \] & & 20 & & 23 & ns \\
    \hline tPLH & Propagation Delay Time Low to High Level Output & \[
    \begin{gathered}
    \text { Clock to } \\
    Q_{A} \text { thru } Q_{H} \\
    \hline
    \end{gathered}
    \] & & & & 21 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \text { Clock to } \\
    Q_{A} \text { thru } Q_{H} \\
    \hline
    \end{gathered}
    \] & & & & 21 & ns \\
    \hline tPHL & Propagation Delay Time High to Low Level Output (Note 2) & \[
    \begin{gathered}
    \text { Clear to } \\
    \mathrm{Q}_{\mathrm{A}^{\prime}} \text { or } \mathrm{Q}_{\mathrm{H}^{\prime}} \\
    \hline
    \end{gathered}
    \] & & 21 & & 24 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \[
    \begin{gathered}
    \text { Clear to } \\
    \mathrm{Q}_{\mathrm{A}} \text { thru } \mathrm{Q}_{\mathrm{H}}
    \end{gathered}
    \] & & & & 24 & ns \\
    \hline \(t_{\text {PZH }}\) & Output Enable Time to High Level Output & \(\overline{\mathrm{G}} 1, \overline{\mathrm{G}} 2\) to \(Q_{A}\) thru \(Q_{H}\) & & & & 18 & ns \\
    \hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level Output & \[
    \begin{aligned}
    & \overline{\mathrm{G}} 1, \overline{\mathrm{G}} 2 \text { to } \\
    & \mathrm{Q}_{\mathrm{A}} \text { thru } \mathrm{Q}_{\mathrm{H}}
    \end{aligned}
    \] & & & & 18 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time to High Level Output (Note 1) & \[
    \begin{aligned}
    & \overline{\mathrm{G}} 1, \overline{\mathrm{G} 2 \text { to }} \\
    & \mathrm{Q}_{\mathrm{A}} \text { thru } \mathrm{Q}_{\mathrm{H}}
    \end{aligned}
    \] & & 12 & & & ns \\
    \hline \(t_{\text {PLZ }}\) & \begin{tabular}{l}
    Output Disable Time \\
    to Low Level Output (Note 1)
    \end{tabular} & \(\overline{\mathrm{G}} 1, \overline{\mathrm{G}} 2\) to \(Q_{A}\) thru \(Q_{H}\) & & 12 & & & ns \\
    \hline
    \end{tabular}

    Note 1: \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\).
    Note 2: \(R_{L}=1 \mathrm{~K} \Omega\) for delays measured to \(Q_{A^{\prime}}\) and \(Q_{H^{\prime}}\).
    Note 3: For testing \(f_{\text {MAX }}\) all outputs are loaded simultaneously.

    \section*{Function Table}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Mode} & \multicolumn{6}{|c|}{Inputs} & \multicolumn{8}{|c|}{Inputs/Outputs} & Outputs \\
    \hline & \multirow[t]{2}{*}{Clear} & \multicolumn{2}{|l|}{Function Select} & Output Control & \multirow[t]{2}{*}{Clock} & \multirow[t]{2}{*}{\[
    \left|\begin{array}{cc}
    \text { Serial } \\
    \text { SL SR }
    \end{array}\right|
    \]} & \multirow[t]{2}{*}{\(A / Q_{A}\)} & \multirow[t]{2}{*}{\(B / Q_{B}\)} & \multirow[t]{2}{*}{C/Qc} & \multirow[t]{2}{*}{D/Q \(\mathbf{D}\)} & \multirow[t]{2}{*}{\(E / Q_{E}\)} & \multirow[t]{2}{*}{\(F / Q_{F}\)} & \multirow[t]{2}{*}{\(\mathbf{G} / \mathbf{Q}_{\mathbf{G}}\)} & \multirow[t]{2}{*}{\(H / Q_{H}\)} & \multirow[t]{2}{*}{\(\mathbf{Q}_{\mathbf{A}^{\prime}} \mathbf{Q}_{\mathbf{H}^{\prime}}\)} \\
    \hline & & S1 & So & \(\overline{\mathbf{G} 1+} \mathbf{G} \mathbf{2} \dagger\) & & & & & & & & & & & \\
    \hline Clear & \[
    \begin{aligned}
    & L \\
    & L
    \end{aligned}
    \] & \[
    x
    \] & \[
    \begin{aligned}
    & L \\
    & X
    \end{aligned}
    \] & \[
    \begin{array}{ll}
    L & L \\
    L & L
    \end{array}
    \] & \[
    \begin{aligned}
    & x \\
    & x
    \end{aligned}
    \] & \[
    \begin{array}{ll}
    x & x \\
    x & x
    \end{array}
    \] & \[
    \begin{aligned}
    & L \\
    & L
    \end{aligned}
    \] & \[
    \begin{aligned}
    & L \\
    & L
    \end{aligned}
    \] & \[
    \begin{aligned}
    & L \\
    & L
    \end{aligned}
    \] & \[
    \begin{aligned}
    & \mathrm{L} \\
    & \mathrm{~L}
    \end{aligned}
    \] & \[
    \begin{aligned}
    & L \\
    & L
    \end{aligned}
    \] & \[
    \begin{aligned}
    & L \\
    & L
    \end{aligned}
    \] & \[
    \begin{aligned}
    & L \\
    & L
    \end{aligned}
    \] & \[
    \begin{aligned}
    & L \\
    & L
    \end{aligned}
    \] & \[
    \begin{array}{ll}
    \mathrm{L} & \mathrm{~L} \\
    \mathrm{~L} & \mathrm{~L}
    \end{array}
    \] \\
    \hline Hold & \[
    \begin{aligned}
    & \mathrm{H} \\
    & \mathrm{H}
    \end{aligned}
    \] & \[
    \begin{aligned}
    & \mathrm{L} \\
    & \mathrm{X}
    \end{aligned}
    \] & \[
    \begin{aligned}
    & \mathrm{L} \\
    & \mathrm{X}
    \end{aligned}
    \] & \[
    \begin{array}{ll}
    L & L \\
    L & L
    \end{array}
    \] & \[
    \begin{aligned}
    & X \\
    & L
    \end{aligned}
    \] & \[
    \begin{array}{ll}
    x & x \\
    x & x
    \end{array}
    \] & \[
    \begin{aligned}
    & Q_{A O} \\
    & Q_{A O}
    \end{aligned}
    \] & \[
    \begin{aligned}
    & Q_{B 0} \\
    & Q_{B 0}
    \end{aligned}
    \] & \[
    \begin{aligned}
    & Q_{\mathrm{CO}} \\
    & Q_{\mathrm{CO}}
    \end{aligned}
    \] & \[
    \begin{aligned}
    & Q_{D 0} \\
    & Q_{D 0}
    \end{aligned}
    \] & \[
    \begin{aligned}
    & Q_{E 0} \\
    & Q_{E 0}
    \end{aligned}
    \] & \[
    \begin{aligned}
    & Q_{F 0} \\
    & Q_{F 0}
    \end{aligned}
    \] & \[
    \begin{aligned}
    & \mathrm{Q}_{\mathrm{GO}} \\
    & \mathrm{Q}_{\mathrm{GO}}
    \end{aligned}
    \] & \[
    \begin{aligned}
    & Q_{H O} \\
    & Q_{H O}
    \end{aligned}
    \] & \[
    \begin{array}{ll}
    Q_{A O} & Q_{H O} \\
    Q_{A O} & Q_{H O} \\
    \hline
    \end{array}
    \] \\
    \hline Shift Right & \[
    \begin{aligned}
    & \mathrm{H} \\
    & \mathrm{H}
    \end{aligned}
    \] & \[
    \begin{aligned}
    & L \\
    & L
    \end{aligned}
    \] & \[
    \begin{aligned}
    & \mathrm{H} \\
    & \mathrm{H}
    \end{aligned}
    \] & \[
    \begin{array}{ll}
    L & L \\
    L & L
    \end{array}
    \] & \[
    \uparrow
    \] & \[
    \begin{array}{ll}
    X & H \\
    X & L
    \end{array}
    \] & \[
    \begin{aligned}
    & H \\
    & L
    \end{aligned}
    \] & \[
    \begin{aligned}
    & Q_{A n} \\
    & Q_{A n}
    \end{aligned}
    \] & \(Q_{B n}\) \(Q_{B n}\) & \begin{tabular}{l}
    \(Q_{C n}\) \\
    \(Q_{C n}\)
    \end{tabular} & \(Q_{D n}\) \(Q_{D n}\) & \[
    \begin{aligned}
    & Q_{\mathrm{En}} \\
    & Q_{\mathrm{En}}
    \end{aligned}
    \] & \[
    \begin{aligned}
    & Q_{F n} \\
    & Q_{\text {Fn }}
    \end{aligned}
    \] & \[
    \begin{aligned}
    & \mathrm{Q}_{\mathrm{Gn}} \\
    & \mathrm{Q}_{\mathrm{Gn}}
    \end{aligned}
    \] & \(\begin{array}{ll}H & Q_{G n} \\ L & Q_{G n}\end{array}\) \\
    \hline Shift Left & \[
    \begin{aligned}
    & \mathrm{H} \\
    & \mathrm{H}
    \end{aligned}
    \] & \[
    \begin{aligned}
    & \mathrm{H} \\
    & \mathrm{H} \\
    & \hline
    \end{aligned}
    \] & \[
    \begin{aligned}
    & L \\
    & L
    \end{aligned}
    \] & \[
    \begin{array}{ll}
    L & L \\
    L & L
    \end{array}
    \] & \[
    \uparrow
    \] & \[
    \begin{array}{ll}
    H & X \\
    L & X
    \end{array}
    \] & \[
    \begin{aligned}
    & \mathrm{Q}_{\mathrm{Bn}} \\
    & \mathrm{Q}_{\mathrm{Bn}} \\
    & \hline
    \end{aligned}
    \] & \begin{tabular}{l}
    \(Q_{C n}\) \\
    \(Q_{C n}\)
    \end{tabular} & \begin{tabular}{l}
    \(Q_{D n}\) \\
    \(Q_{D n}\)
    \end{tabular} & \[
    \begin{aligned}
    & Q_{E \in n} \\
    & Q_{\mathrm{En}} \\
    & \hline
    \end{aligned}
    \] & \[
    \begin{aligned}
    & Q_{F n} \\
    & Q_{F n}
    \end{aligned}
    \] & \begin{tabular}{l}
    \(Q_{G n}\) \\
    \(Q_{G n}\)
    \end{tabular} & \[
    \begin{aligned}
    & \mathrm{Q}_{\mathrm{Hn}} \\
    & \mathrm{Q}_{\mathrm{Hn}} \\
    & \hline
    \end{aligned}
    \] & \[
    \begin{aligned}
    & H \\
    & L
    \end{aligned}
    \] & \[
    \begin{array}{ll}
    Q_{B n} & H \\
    Q_{B n} & L
    \end{array}
    \] \\
    \hline Load & H & H & H & \(\mathrm{X} \times\) & \(\uparrow\) & \(\mathrm{X} \times\) & a & b & c & d & e & \(f\) & g & h & a h \\
    \hline
    \end{tabular}
    tWhen one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected
    a...h \(=\) the level of the steady-state input at inputs \(A\) through \(H\), respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.
    \(Q_{A O} \ldots Q_{H O}=\) The output logic level of \(Q_{X}\) before the indicated input conditions were established.
    \(H=\) high level, \(L=\) low logic level, \(X=\) either low or high logic level
    \(Q_{A n} \ldots Q_{H n}=\) The output logic level before the active transition ( \(\uparrow\) ) of the clock input.
    

    \section*{DM54S373/DM74S373, DM54S374/DM74S374 TRI-STATE \({ }^{\circledR}\) Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops}

    \section*{General Description}

    These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.
    The eight latches of the DM54/74S373 are transparent D -type latches meaning that while the enable \((\mathrm{G})\) is high the \(Q\) outputs will follow the data ( \(D\) ) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.
    The eight flip-flops of the DM54/74S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the \(D\) inputs.

    Schmitt-trigger buffered inputs at the enable/clock lines simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

    \section*{Features}
    - Choice of 8 latches or 8 D-type flip-flops in a single package
    - TRI-STATE bus-driving outputs
    - Full parallel-access for loading
    - Buffered control inputs
    - P-N-P input reduce D-C loading on data lines

    \section*{Connection Diagrams}

    \section*{Dual-In-Line Package}
    

    Order Number DM54S373J, DM74S373WM or DM74S373N
    See NS Package Number J20A, M20B or N20A

    \section*{Dual-In-Line Package}
    

    Order Number DM54S374J, DM74S374WM or DM74S374N See NS Package Number J20A, M20B or N20A

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    7 V
    Input Voltage 5.5 V
    Operating Free Air Temperature Range
    DM54S
    \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
    DM74S
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)

    Storage Temperature Range \(\quad-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Function Tables}
    \begin{tabular}{c|cc|c|c|c|c|c|c|}
    \multicolumn{4}{c}{\begin{tabular}{c} 
    DM54/74S373 \\
    \multicolumn{4}{c|}{ Truth Table }
    \end{tabular}} & \multicolumn{4}{c|}{\begin{tabular}{c} 
    DM54/74S374 \\
    Truth Table
    \end{tabular}} \\
    \hline \begin{tabular}{c} 
    Output \\
    Control
    \end{tabular} & \begin{tabular}{c} 
    Enable \\
    G
    \end{tabular} & D & Output \\
    \hline L & H & H & H \\
    L & H & L & L \\
    L & L & X & \(\mathrm{Q}_{0}\) \\
    H & X & X & Z \\
    \hline
    \end{tabular}
    \(H=\) High Level (Steady State), \(L=\) Low Level (Steady State), \(X=\) Don't Care
    \(\uparrow=\) Transition from low-to-high level, \(Z=\) High Impedance State
    \(Q_{0}=\) The level of the output before steady-state input conditions were established.

    \section*{Logic Diagrams}
    

    DM54/74S374
    Positive-Edge-Triggered Flip-Flops
    
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54S373} & \multicolumn{3}{|c|}{DM74S373} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\text {CC }}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
    \hline \(\mathrm{V}_{\mathrm{IL}}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
    \hline \({ }^{\mathrm{OH}}\) & \multicolumn{2}{|l|}{High Level Output Current} & & & -2 & & & -6.5 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 20 & & & 20 & mA \\
    \hline \multirow[t]{2}{*}{\({ }^{\text {tw }}\)} & \multirow[t]{2}{*}{Pulse Width (Note 2)} & Enable High & 6 & & & 6 & & & ns \\
    \hline & & Enable Low & 7.3 & & & 7.3 & & & \\
    \hline tsu & \multicolumn{2}{|l|}{Data Setup Time (Notes 1 and 3)} & O \(\downarrow\) & & & 0 \(\downarrow\) & & & ns \\
    \hline \(t_{H}\) & \multicolumn{2}{|l|}{Data Hold Time (Notes 1 and 3)} & 10 \(\downarrow\) & & & \(10 \downarrow\) & & & ns \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Note 1: The symbol \((\downarrow)\) indicates the falling edge of the clock pulse is used for reference.
    Note 2: \(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    Note 3: \(T_{A}=25^{\circ} \mathrm{C}\) and \(V_{C C}=5 \mathrm{~V}\).
    'S373 Electrical Characteristics overrecommended operating free a ar temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|r|}{Conditions} & Min & Typ (Note 4) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \multirow[t]{2}{*}{V OH} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Min} \\
    & I_{O H}=M a x \\
    & V_{I L}=M a x \\
    & V_{I H}=M i n
    \end{aligned}
    \]} & DM54 & 2.4 & 3.4 & & \\
    \hline & & & DM74 & 2.4 & 3.2 & & V \\
    \hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\)} & & & -250 & \(\mu \mathrm{A}\) \\
    \hline lozh & \begin{tabular}{l}
    Off-State Output \\
    Current with High \\
    Level Output \\
    Voltage Applied
    \end{tabular} & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Max}, V_{\mathrm{O}}=2.4 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, V_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline lozL & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Max}, \mathrm{V}_{\mathrm{O}}=0.5 \mathrm{~V} \\
    & \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}, \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & -50 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & (\text { Note 5) }
    \end{aligned}
    \]} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline \multirow[t]{2}{*}{Icc} & \multirow[t]{2}{*}{Supply Current} & \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & Outputs High or Low & & 105 & 160 & \multirow{2}{*}{mA} \\
    \hline & & & Outputs Disabled & & & 190 & \\
    \hline
    \end{tabular}

    Note 4: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{10}{|l|}{\begin{tabular}{l}
    'S373 Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}^{\text {and }} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) \\
    (See Section 1 for Test Waveforms and Output Load)
    \end{tabular}} \\
    \hline \multirow{3}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow{3}{*}{Parameter}} & \multicolumn{2}{|l|}{\multirow{3}{*}{\begin{tabular}{l}
    From (Input) \\
    To (Output)
    \end{tabular}}} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & & & \(\mathrm{C}_{\mathrm{L}}=\) & & \(\mathrm{C}_{\mathrm{L}}=\) & & \\
    \hline & & & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & \multicolumn{2}{|l|}{Propagation Delay Time Low to High Level Output} & \multicolumn{2}{|l|}{\begin{tabular}{l}
    Data to \\
    Any Q
    \end{tabular}} & & 12 & & 14 & ns \\
    \hline \(t_{\text {PHL }}\) & \multicolumn{2}{|l|}{Propagation Delay Time High to Low Level Output} & \multicolumn{2}{|l|}{Data to Any Q} & & 12 & & 16 & ns \\
    \hline \(t_{\text {PLH }}\) & \multicolumn{2}{|l|}{Propagation Delay Time Low to High Level Output} & \multicolumn{2}{|l|}{Enable to Any Q} & & 14 & & 14 & ns \\
    \hline \(t_{\text {PHL }}\) & \multicolumn{2}{|l|}{Propagation Delay Time High to Low Level Output} & \multicolumn{2}{|l|}{Enable to Any Q} & & 18 & & 21 & ns \\
    \hline \(t_{\text {PZH }}\) & \multicolumn{2}{|l|}{Enable Time to High Level Output} & \multicolumn{2}{|l|}{Output Control to Any Q} & & 15 & & 17 & ns \\
    \hline \(t_{\text {PZL }}\) & \multicolumn{2}{|l|}{Output Enable Time to Low Level Output} & \multicolumn{2}{|l|}{Output Control to Any Q} & & 18 & & 23 & ns \\
    \hline \(\mathrm{t}_{\text {PHZ }}\) & \multicolumn{2}{|l|}{Output Disable Time to High Level Output (Note 1)} & \multicolumn{2}{|l|}{Output Control to Any Q} & & 9 & & & ns \\
    \hline tpLZ & \multicolumn{2}{|l|}{Output Disable Time to Low Level Output (Note 1)} & \multicolumn{2}{|l|}{Output Control to Any Q} & & 12 & & & ns \\
    \hline \multicolumn{10}{|l|}{\multirow[t]{2}{*}{\begin{tabular}{l}
    Note 1: \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\) \\
    'S374 Recommended Operating Conditions \\
    (See Section 1 for Test Waveforms and Output Load)
    \end{tabular}}} \\
    \hline & & & & & & & & & \\
    \hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54S374} & \multicolumn{3}{|c|}{DM74S374} & \multirow{2}{*}{Units} \\
    \hline & & & Min & Nom & Max & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{1 \mathrm{H}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.8 & & & 0.8 & V \\
    \hline lOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -2 & & & -6.5 & mA \\
    \hline lOL & \multicolumn{2}{|l|}{Low Level Output Current} & & & 20 & & & 20 & mA \\
    \hline fCLK & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & 100 & 75 & 0 & 100 & 75 & MHz \\
    \hline fCLK & \multicolumn{2}{|l|}{Clock Frequency (Note 3)} & 0 & 100 & 75 & 0 & 100 & 75 & MHz \\
    \hline \multirow[t]{4}{*}{tw} & \multirow[t]{2}{*}{Pulse Width (Note 2)} & Clock
    High & 6 & & & 6 & & & \multirow{4}{*}{ns} \\
    \hline & & \begin{tabular}{l}
    Clock \\
    Low
    \end{tabular} & 7.3 & & & 7.3 & & & \\
    \hline & \multirow[t]{2}{*}{Pulse Width (Note 3)} & \begin{tabular}{l}
    Clock \\
    High
    \end{tabular} & 15 & & & 15 & & & \\
    \hline & & \begin{tabular}{l}
    Clock \\
    Low
    \end{tabular} & 15 & & & 15 & & & \\
    \hline tsu & \multicolumn{2}{|l|}{Data Setup Time (Notes 1 and 4)} & \(5 \uparrow\) & & & \(5 \uparrow\) & & & ns \\
    \hline \(t_{H}\) & \multicolumn{2}{|l|}{Data Hold Time (Notes 1 and 4)} & \(2 \uparrow\) & & & \(2 \uparrow\) & & & ns \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \multicolumn{3}{|l|}{\begin{tabular}{l}
    Note 1: The symbol ( \(\uparrow\) ) indicates the rising edge of the clock \\
    Note 2: \(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\). \\
    Note 3: \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\). \\
    Note 4: \(T_{A}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
    \end{tabular}} & \multicolumn{2}{|l|}{pulse is used for reference.} & & & & & \\
    \hline
    \end{tabular}

    \section*{'S374 Electrical Characteristics}
    over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|r|}{Conditions} & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) } \\
    \hline
    \end{gathered}
    \] & Max & Units \\
    \hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min} \\
    & \mathrm{IOH}_{\mathrm{OH}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \]} & DM54 & 2.4 & 3.4 & & \\
    \hline & & & DM74 & 2.4 & 3.2 & & v \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O L}=M a x \\
    & V_{I H}=M i n, V_{I L}=M a x
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \({ }_{\mathrm{H}}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.5 \mathrm{~V}\)} & & & -250 & \(\mu \mathrm{A}\) \\
    \hline lozh & Off-State Output Current with High Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=2.4 V \\
    & V_{\mathrm{IH}}=\operatorname{Min}, V_{\mathrm{IL}}=\operatorname{Max}
    \end{aligned}
    \]} & & & 50 & \(\mu \mathrm{A}\) \\
    \hline lozl & Off-State Output Current with Low Level Output Voltage Applied & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=\operatorname{Max}, V_{O}=0.5 \mathrm{~V} \\
    & V_{I H}=\operatorname{Min}, V_{I L}=\operatorname{Max}
    \end{aligned}
    \]} & & & -50 & \(\mu \mathrm{A}\) \\
    \hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & (\text { Note } 2)
    \end{aligned}
    \]} & DM54 & -40 & & -100 & \multirow[t]{2}{*}{mA} \\
    \hline & & & DM74 & -40 & & -100 & \\
    \hline \multirow[t]{3}{*}{ICC} & \multirow[t]{3}{*}{Supply Current} & \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & Outputs High & & & 110 & \multirow{3}{*}{mA} \\
    \hline & & & Outputs Low & & 90 & 140 & \\
    \hline & & & Outputs Disabled & & & 160 & \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    'S374 Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\)
    (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{\begin{tabular}{l}
    From (Input) \\
    To (Output)
    \end{tabular}} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|l|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(\mathrm{f}_{\text {MAX }}\) & Maximum Clock Frequency & & & 75 & & 75 & MHz \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Clock to Any Q & & 15 & & 15 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & Clock to Any Q & & 17 & & 20 & ns \\
    \hline \(t_{\text {tPZ }}\) & Output Enable Time to High Level Output & Output Control to Any Q & & 15 & & 17 & ns \\
    \hline \(t_{\text {PZL }}\) & Output Enable Time to Low Level Output & Output Control to Any Q & & 18 & & 23 & ns \\
    \hline \(t_{\text {PHZ }}\) & Output Disable Time from High Level Output (Note 1) & Output Control to Any Q & & 9 & & & ns \\
    \hline tplz & Output Disable Time from Low Level Output (Note 1) & Output Control to Any Q & & 12 & & & ns \\
    \hline
    \end{tabular}

    Note 1: \(\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}\)

    \section*{DM74S381 Arithmetic Logic Unit/Function Generator}

    \section*{General Description}

    The 'S381 is a Schottky TTL arithmetic logic unit (ALU)/ function generator that performs eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. These operations are selected by the three functionselect lines (S0, S1, S2). A full carry look-ahead circuit is provided for fast, simultaneous carry generation by means of two cascade outputs ( \(\overline{\mathrm{P}}\) and \(\overline{\mathrm{G}}\) ) for the four bits in the package. The method of cascading 54S182/74S182 lookahead carry generators with these ALU's to provide multilevel full carry look-ahead is illustated under typical applications data for the 'S182. The typical addition times shown illustrate the short delay time required for addition of longer words when full look-ahead is employed. The exclusive-OR, AND, or OR function of two Boolean variables is provided without the use of external circuitry. Also, the outputs can be either cleared (low) or preset (high) as desired.

    \section*{Connection Diagram}

    \section*{Pin Designations}
    \begin{tabular}{|c|c|c|}
    \hline Designation & Pin Nos. & Function \\
    \hline A3, A2, A1, A0 & \(17,19,1,3\) & Word A Inputs \\
    \hline B3, B2, B1, B0 & \(16,18,2,4\) & Word B Inputs \\
    \hline S2, S1, S0 & \(7,6,5\) & \begin{tabular}{c} 
    Function-Select \\
    Inputs
    \end{tabular} \\
    \hline C \(_{\mathrm{n}}\) & 15 & \begin{tabular}{c} 
    Carry Input for \\
    Addition, Inverted \\
    Carry Input for \\
    Subtraction
    \end{tabular} \\
    \hline F3, F2, F1, F0 & \(12,11,9,8\) & Function Outputs \\
    \hline\(\overline{\text { P }}\) & 14 & \begin{tabular}{c} 
    Inverted Carry \\
    Propagate Output
    \end{tabular} \\
    \hline \(\bar{G}\) & 13 & \begin{tabular}{c} 
    Inverted Carry \\
    Generated Output
    \end{tabular} \\
    \hline VCC & 20 & Supply Voltage \\
    \hline GND & 10 & Ground \\
    \hline
    \end{tabular}

    \section*{Features}
    - A fully parallel 4 -Bit ALU in 20-pin package for 0.300 inch row spacing
    - Ideally suited for high-density economical processors
    - Parallel inputs and outputs and full look-ahead provide system flexibility
    - Arithmetic and logic operations selected specifically to simplify system implementation:

    A minus B
    \(B\) minus \(A\)
    A plus B
    and five other functions
    - Schottky-clamped for high performance

    16-bit add time ... 26 ns typ using look-ahead 32-bit add time . . . 34 ns typ using look-ahead
    

    Function Table
    \begin{tabular}{|c|c|c|c|}
    \hline \multicolumn{3}{|c|}{ Selection } & \multirow{2}{*}{\begin{tabular}{c} 
    Arithmetic/Logic \\
    Operation
    \end{tabular}} \\
    \hline S2 & S1 & S0 & CLEAR \\
    \hline L & L & L & B MINUS A \\
    L & L & H & A MINUS B \\
    L & H & L & A PLUS B \\
    H & H & H & A \(\oplus\) B \\
    H & L & L & A + B \\
    H & H & H & AB \\
    H & H & H & PRESET \\
    \hline
    \end{tabular} See NS Package Number N20A
    \(H=\) high level, \(L=\) low level
    \begin{tabular}{lr} 
    Supply Voltage & 7 V \\
    Input Voltage & 5.5 V \\
    Operating Free Air Temperature Range & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{l|l|c|c|c|c}
    \hline Symbol & Parameter & Min & Nom & Max & Units \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 20 & mA \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(V_{C C}=M i n, l_{1}=-18 \mathrm{~mA}\)} & & & -1.2 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & V_{C C}=M i n, I_{O H}=\text { Max }, \\
    & V_{I L}=M a x, V_{I H}=\operatorname{Min}
    \end{aligned}
    \]} & 2.7 & 3.4 & & V \\
    \hline \(\mathrm{V}_{\text {OL }}\) & Low Level Output Voltage & \multicolumn{2}{|l|}{\[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{OL}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\mathrm{Min}, \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \]} & & & 0.5 & V \\
    \hline 11 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=5.5 \mathrm{~V}\)} & & & 1 & mA \\
    \hline \multirow[t]{3}{*}{\({ }_{1 / H}\)} & \multirow[t]{3}{*}{High Level Input Current} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{I}=2.7 V
    \end{aligned}
    \]} & Any S & & & 50 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
    \hline & & & Cn & & & 250 & \\
    \hline & & & Any Other & & & 200 & \\
    \hline \multirow[t]{3}{*}{IIL} & \multirow[t]{3}{*}{Low Level Input Current} & \multirow[t]{3}{*}{\[
    \begin{aligned}
    & V_{C C}=M a x \\
    & V_{1}=0.5 V
    \end{aligned}
    \]} & Any S & & & -2 & \multirow{3}{*}{mA} \\
    \hline & & & Cn & & & -8 & \\
    \hline & & & Any Other & & & -6 & \\
    \hline los & Short Circuit Output Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 2)} & -40 & & -100 & mA \\
    \hline lcc & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 105 & 160 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow[b]{3}{*}{\begin{tabular}{l}
    From (Input) \\
    To (Output)
    \end{tabular}} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=280 \Omega\)} & \multirow{3}{*}{Units} \\
    \hline & & & \multicolumn{2}{|l|}{\(C_{L}=15 \mathrm{pF}\)} & \multicolumn{2}{|r|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
    \hline & & & Min & Max & Min & Max & \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & Cn to Any F & & 17 & & 19 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
    Cn to \\
    Any F
    \end{tabular} & & 17 & & 19 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
    \begin{aligned}
    & A \text { or } B \\
    & \text { to } \bar{G}
    \end{aligned}
    \] & & 20 & & 23 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \(A\) or \(B\) to \(\bar{G}\) & & 20 & & 23 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \(A\) or \(B\)
    \[
    \text { to } \bar{P}
    \] & & 18 & & 21 & ns \\
    \hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \(A\) or \(B\) to \(\bar{P}\) & & 18 & & 21 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \(\mathrm{A}_{\mathrm{i}}\) or \(\mathrm{B}_{\mathrm{i}}\) to \(\mathrm{F}_{\mathrm{i}}\) & & 27 & & 30 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \(\mathrm{A}_{\mathrm{i}}\) or \(\mathrm{B}_{\mathrm{i}}\) to \(\mathrm{F}_{\mathrm{i}}\) & & 25 & & 27 & ns \\
    \hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \begin{tabular}{l}
    \(S\) to \\
    Any
    \end{tabular} & & 30 & & 33 & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \begin{tabular}{l}
    \(S\) to \\
    Any
    \end{tabular} & & 30 & & 33 & ns \\
    \hline
    \end{tabular}
    

    DM93S00

    \section*{4-Bit Universal Shift Register}

    \section*{General Description}

    This device is 4-bit universal shift register. As a high speed multifunctional sequential logic block, it is useful in a wide variety of register and counter applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallelserial, and parallel-parallel data register transfers.

    \section*{Connection Diagram}
    

    \section*{Logic Symbol}
    

    TL/F/10164-2
    \[
    V_{C C}=\operatorname{Pin} 16
    \]
    \(\mathrm{GND}=\operatorname{Pin} 8\)

    TL/F/10164-1
    Order Number DM93S00N See NS Package Number N16E

    \section*{Truth Table}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Operating Mode} & \multicolumn{7}{|c|}{Inputs ( \(\overline{\mathrm{MR}}=\mathrm{H}\) )} & \multicolumn{5}{|c|}{Outputs @ tn+1} \\
    \hline & \(\overline{\mathbf{P E}}\) & J & \(\overline{\mathbf{K}}\) & PO & P1 & P2 & P3 & Q0 & Q1 & Q2 & Q3 & Q3 \\
    \hline \multirow[t]{4}{*}{Shift Mode} & H & L & L & X & X & X & \(x\) & L & Q0 & Q1 & Q2 & \(\overline{\mathrm{Q}} 2\) \\
    \hline & H & L & H & X & X & X & \(x\) & Q0 & Q0 & Q1 & Q2 & Q2 \\
    \hline & H & H & L & X & \(x\) & X & \(x\) & Q0 & Q0 & Q1 & Q2 & Q2 \\
    \hline & H & H & H & X & X & X & X & H & Q0 & Q1 & Q2 & Q2 \\
    \hline Parallel & L & X & X & L & L & L & L & L & L & L & L & H \\
    \hline Entry Mode & L & X & X & H & H & H & H & H & H & H & H & L \\
    \hline
    \end{tabular}
    *tn \(+1=\) State after next LOW-to-HIGH clock transition.
    H = HIGH Voltage Level
    \(\mathrm{L}=\) LOW Voltage Level
    \(X=\) Immaterial
    \begin{tabular}{lr} 
    Absolute Maximum Ratings \\
    Supply Voltage & 7 V \\
    Input Voltage & 5.5 V \\
    Operating Free Air Temperature Range & \\
    DM93S & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
    Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
    \end{tabular}

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM93S00} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline \(\mathrm{IOH}^{2}\) & High Level Output Current & & & -1 & mA \\
    \hline lOL & Low Level Output Current & & & 20 & mA \\
    \hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{s}}(\mathrm{H}) \\
    & \mathrm{t}_{\mathrm{s}}(\mathrm{~L}) \\
    & \hline
    \end{aligned}
    \] & Setup Time HIGH or LOW, \(J, \bar{K}\) and PO-P3 to CP & \[
    \begin{aligned}
    & 6.0 \\
    & 6.0 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L) \\
    & \hline
    \end{aligned}
    \] & Hold Time HIGH or LOW, \(J, \bar{K}\) and P0-P3 to CP & \[
    \begin{aligned}
    & 0 \\
    & 0 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{s}(H) \\
    & t_{s}(L)
    \end{aligned}
    \] & Setup Time HIGH or LOW, \(\overline{\mathrm{PE}}\) to CP & \[
    \begin{aligned}
    & 8.0 \\
    & 8.0 \\
    & \hline
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{h}(H) \\
    & t_{h}(L)
    \end{aligned}
    \] & Hold Time HIGH or LOW, \(\overline{P E}\) to CP & \[
    \begin{aligned}
    & 0 \\
    & 0
    \end{aligned}
    \] & & & ns \\
    \hline \[
    \begin{aligned}
    & t_{w}(H) \\
    & t_{w}(L) \\
    & \hline
    \end{aligned}
    \] & CP Pulse Width HIGH or LOW & \[
    \begin{aligned}
    & 7.0 \\
    & 7.0
    \end{aligned}
    \] & & & ns \\
    \hline \(t_{w}(L)\) & \(\overline{M R}\) Pulse Width LOW & 12 & & & ns \\
    \hline \(\mathrm{trec}^{\text {c }}\) & Recovery Time \(\overline{\mathrm{MR}}\) to CP & 5.0 & & & ns \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & Typ
    (Note 1) & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \(V_{C C}=M i n, l_{1}=-18 \mathrm{~mA}\) & & & -1.2 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \] & 2.7 & 3.4 & & V \\
    \hline VOL & Low Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \] & & 0.35 & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\) & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\) & & & -2.0 & mA \\
    \hline los & Short Circuit Output Current & \[
    \begin{aligned}
    & V_{C C}=\text { Max } \\
    & \text { (Note 2) }
    \end{aligned}
    \] & 20 & & 80 & mA \\
    \hline ICC & Supply Current & \(\mathrm{V}_{C C}=\) Max & & & 120 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\[
    \begin{aligned}
    & R_{\mathrm{L}}=280 \Omega \\
    & \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}
    \end{aligned}
    \]} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \(\mathrm{f}_{\text {max }}\) & Maximum Shift Frequency & 70 & & MHz \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay CP to Qn & & \[
    \begin{gathered}
    8.5 \\
    12 \\
    \hline
    \end{gathered}
    \] & ns \\
    \hline \(\mathrm{t}_{\text {PHL }}\) & Propagation Delay \(\overline{M R}\) to Qn & & 23 & ns \\
    \hline
    \end{tabular}

    \section*{Functional Description}

    The Logic Diagrams and Truth Table indicate the functional characteristics of the DM93S00 4-bit shift register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers.
    The DM93S00 has two primary modes of operation, shift right ( \(\mathrm{Q} 0 \rightarrow \mathrm{Q} 1\) ) and parallel load, which are controlled by the state of the Parallel Enable ( \(\overline{\mathrm{PE}}\) ) input. When the PE input is HIGH, serial data enters the first flip-flop Q0 via the \(J\) and \(\bar{K}\) inputs and is shifted one bit in the direction Q0 \(\rightarrow\) Q1 \(\rightarrow\) Q2 \(\rightarrow\) Q3 following each LOW-to-HIGH clock transition. The \(\sqrt{\bar{K}}\) inputs provide the flexibility of the JK type input for special applications, and the simple

    D-type input for general applications by tying the two pins together. When the \(\overline{P E}\) input is LOW, the DM93S00 appears as four common clocked D flip-flops. The data on the parallel inputs P0-P3 is transferred to the respective Q0-Q3 outputs following the LOW-to-HIGH clock transition. Shift left operation (Q3 \(\rightarrow\) Q2) can be achieved by tying the Qn outputs to the \(\mathrm{Pn}-1\) inputs and holding the PE input LOW. All serial and parallel data transfers are synchronous, occuring after each LOW-to-HIGH clock transition. Since the DM93S00 utilizes edge triggering, there is no restriction on the activity of the \(\mathrm{J}, \overline{\mathrm{K}}, \mathrm{Pn}\) and \(\overline{\mathrm{PE}}\) inputs for logic opera-tion-except for the setup and release time requirements. A LOW on the asynchronous Master Reset (MR) input sets all Q outputs LOW, independent of any other input condition.

    \section*{Logic Diagram}
    

    \section*{DM93S41}

    \section*{4-Bit Arithmetic Logic Unit}

    \section*{General Description}

    The DM93S41 4-bit arithmetic logic units can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations; the Add and Subtract modes are the most important. The DM93S41 is a pin replacement for the 54/74181.

    \section*{Connection Diagram}
    

    TL/F/9805-1
    Order Number DM93S41N See NS Package Number N24A

    \section*{Logic Symbols}

    \section*{Active Low Operands}
    

    TL/F/9805-2
    \begin{tabular}{|l|l|}
    \hline \multicolumn{1}{|c|}{ Pin Name } & \multicolumn{1}{c|}{ Description } \\
    \hline \(\bar{A} 0-\bar{A} 3, \bar{B} 0-\bar{B} 3\) & Operand Inputs (Active LOW) \\
    SO-S3 & Function Select Inputs \\
    \(M\) & Mode Control Input \\
    Cu & Carry Input \\
    \(\overline{\mathrm{F}} 0-\overline{\mathrm{F}} 3\) & Function Outputs (Active LOW) \\
    \(\mathrm{A}=\mathrm{B}\) & Comparator Output \\
    \(\bar{G}\) & Carry Generate Output (Active LOW) \\
    \(\bar{P}\) & Carry Propagate Output (Active LOW) \\
    \(\mathrm{C}_{\mathrm{n}}+4\) & Carry Output \\
    \hline
    \end{tabular}

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    5.5 V

    Operating Free Air Temperature Range DM93S
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    Storage Temperature Range

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{c|c|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multicolumn{2}{|c|}{ Parameter } & \multicolumn{2}{|c|}{ DM93S41 } & \multirow{2}{*}{ Units } \\
    \cline { 3 - 4 } & & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 20 & mA \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & \begin{tabular}{l}
    Typ \\
    (Note 1)
    \end{tabular} & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{1}=-18 \mathrm{~mA}\) & & & -1.2 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \] & 2.7 & 3.4 & & V \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
    \end{aligned}
    \] & & 0.35 & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\) & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\) & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\) & & & -1.6 & mA \\
    \hline los & Short Circuit Output Current & \[
    \begin{aligned}
    & V_{C C}=M a x \\
    & \text { (Note 2) }
    \end{aligned}
    \] & -40 & & -100 & mA \\
    \hline \({ }^{\text {I CCL }}\) & Supply Current & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
    & \mathrm{M}, \mathrm{SO}-\mathrm{S3}=4.5 \mathrm{~V} \\
    & \text { All Other Inputs }=0 \mathrm{~V}
    \end{aligned}
    \] & & & 150 & mA \\
    \hline ICCH & Supply Current & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
    & \mathrm{C}_{\mathrm{n}}, \overline{\mathrm{~B}} 0-\overline{\mathrm{B}} 3=\mathrm{GND} \\
    & \text { All Other Inputs }=4.5 \mathrm{~V}
    \end{aligned}
    \] & & & 140 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    Switching Characteristics
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Conditions} & \multicolumn{2}{|c|}{\[
    \begin{aligned}
    & C L=15 \mathrm{pF} \\
    & \mathrm{R}_{\mathrm{L}}=280 \Omega \\
    & \hline
    \end{aligned}
    \]} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Max & \\
    \hline \[
    t_{\text {PLH }}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & Propagation Delay
    \[
    C_{n} \text { to } C_{n+4}
    \] & \(\mathrm{M}=\) Gnd & & \[
    \begin{aligned}
    & 12 \\
    & 12 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    t_{\text {PLH }}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & Propagation Delay \(\mathrm{C}_{\mathrm{n}}\) to \(\overline{\mathrm{F}}\) & \(\mathrm{M}=\) Gnd & & \[
    \begin{aligned}
    & 12 \\
    & 12 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\bar{A}_{n}\) or \(\bar{B}_{n}\) to \(\bar{G}\) & \[
    \begin{aligned}
    & \mathrm{M}, \mathrm{~S} 1, \mathrm{~S} 2=\mathrm{Gnd} \\
    & \mathrm{SO}, \mathrm{~S} 3=4.5 \mathrm{~V} \\
    & \hline
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 14 \\
    & 14
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\bar{A}_{n}\) or \(\bar{B}_{n}\) to \(\bar{G}\) & \[
    \begin{aligned}
    & M, S 0, S 3=\text { Gnd } \\
    & S 1, S 2=4.5 \mathrm{~V}
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 15 \\
    & 15
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\bar{A}_{n}\) or \(\bar{B}_{n}\) to \(\bar{P}\) & \[
    \begin{aligned}
    & \mathrm{M}, \mathrm{~S} 1, \mathrm{~S} 2=\mathrm{Gnd} \\
    & \mathrm{~S} 0, \mathrm{~S} 3=4.5 \mathrm{~V}
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 14 \\
    & 14
    \end{aligned}
    \] & ns \\
    \hline \[
    t_{\text {PLH }}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & Propagation Delay \(\bar{A}_{n}\) or \(\bar{B}_{n}\) to \(\bar{P}\) & \[
    \begin{aligned}
    & M, S 0, S 3=\text { Gnd } \\
    & S 1, S 2=4.5 \mathrm{~V}
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 15 \\
    & 15 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{pHL}}
    \end{aligned}
    \] & Propagation Delay \(\overline{\mathrm{A}}_{i}\) or \(\overline{\mathrm{B}}_{\mathrm{i}}\) to \(\overline{\mathrm{F}}_{\mathrm{i}}\) & \[
    \begin{aligned}
    & M, S 1, S 3=\text { Gnd } \\
    & S 0, S 3=4.5 \mathrm{~V}
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 20 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\bar{A}_{i}\) or \(\bar{B}_{i}\) to \(\bar{F}_{i}\) & \[
    \begin{aligned}
    & M, S 0, S 3=\text { Gnd } \\
    & S 1, S 2=4.5 \mathrm{~V}
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 21 \\
    & 21 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(\mathrm{t}_{\mathrm{PHL}}\)
    \end{tabular} & Propagation Delay \(\overline{\mathrm{A}}_{i}\) or \(\overline{\mathrm{B}}_{\mathrm{i}}\) to \(\bar{F}_{i}+1\) & \[
    \begin{aligned}
    & M, S 1, S 2=G n d \\
    & S O, S 3=4.5 V
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 24 \\
    & 24
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\overline{\mathrm{A}}_{\mathrm{i}}\) or \(\overline{\mathrm{B}}_{\mathrm{i}}\) to \(\overline{\mathrm{F}}_{\mathrm{i}}+1\) & \[
    \begin{aligned}
    & \mathrm{M}, \mathrm{SO}, \mathrm{~S} 3=\mathrm{Gnd} \\
    & \mathrm{~S} 1, \mathrm{~S} 2=4.5 \mathrm{~V}
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 25 \\
    & 25 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{pLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\bar{A}_{n}\) or \(\bar{B}_{n}\) to \(\bar{F}\) & \(\mathrm{M}=4.5 \mathrm{~V}\) & & \[
    \begin{aligned}
    & 20 \\
    & 20 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\bar{A}_{n}\) or \(\bar{B}_{n}\) to \(C_{n+1}\) & \[
    \begin{aligned}
    & M, S 1, S 2=\text { Gnd } \\
    & S 0, S 3=4.5 V
    \end{aligned}
    \] & & \[
    \begin{array}{r}
    18.5 \\
    18.5 \\
    \hline
    \end{array}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay \(\bar{A}_{n}\) or \(\bar{B}_{n}\) to \(C_{n+1}\) & \[
    \begin{aligned}
    & M, S 0, S 3=\text { Gnd } \\
    & S 1, S 2=4.5 V
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 23 \\
    & 23
    \end{aligned}
    \] & ns \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \({ }^{\text {tpHL }}\)
    \end{tabular} & Propagation Delay \(\bar{A}_{n}\) or \(\bar{B}_{n}\) to \(A=B\) & \[
    \begin{aligned}
    & M, S 0, S 3=\text { Gnd } \\
    & S 1, S 2=4.5 \mathrm{~V} \\
    & R_{L}=400 \Omega \text { to } 5.0 \mathrm{~V}
    \end{aligned}
    \] & & \[
    \begin{aligned}
    & 23 \\
    & 23
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}

    \section*{Functional Description}

    The DM93S41 is a 4 -bit high speed parallel arithmetic logic unit (ALU). Controlled by the four Function Select inputs (S0-S3) and the Mode Control input (M), it can perform all the 16 possible operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table below lists these operations.
    When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the \(\mathrm{C}_{n+4}\) output, or for carry lookahead between packages using the signals \(\overline{\mathrm{P}}\) (Carry Propagate) and \(\overline{\mathrm{G}}\) (Carry Generate). \(\overline{\mathrm{P}}\) and \(\overline{\mathrm{G}}\) are not affected by carry in. When speed requirements are not stringent, the DM93S41 can be used in a simple ripple carry mode by connecting the Carry output ( \(\mathrm{C}_{\mathrm{n}}+4\) ) signal to the Carry input \(\left(\mathrm{C}_{n}\right)\) of the next unit. For super high speed operation the Schottky DM93S41 should be used in conjunction with the ' 42 carry lookahead circuit.

    The \(A=B\) output from the DM93S41 goes HIGH when all four \(\bar{F}_{n}\) outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The \(A=B\) output is open-collector and can be wired-AND with the other \(A=B\) outputs to give a comparison for more than four bits. The \(A=B\) signal can also be used with the \(C_{n+4}\) signal to indicate \(A>B\) and \(A<B\).
    The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus select code LHHL generates A minus \(B\) minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.
    As indicated the ' 41 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.
    
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multicolumn{7}{|c|}{SUM MODE TEST TABLE I. Function Inputs: \(\mathrm{SO}=\mathrm{S} 3=4.5 \mathrm{~V}, \mathrm{~S} 1=\mathrm{S} 2=\mathrm{M}=0 \mathrm{~V}\)} \\
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{\begin{tabular}{l}
    Input \\
    Under \\
    Test
    \end{tabular}} & \multicolumn{2}{|c|}{Other Input Same Bit} & \multicolumn{2}{|c|}{Other Data Input} & \multirow[t]{2}{*}{Output Under Test} \\
    \hline & & Apply
    \[
    4.5 \mathrm{~V}
    \] & Apply GND & Apply
    \[
    4.5 \mathrm{~V}
    \] & Apply GND & \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & \(\bar{A}_{i}\) & \(\bar{B}_{i}\) & None & Remaining \(\bar{A}\) to \(\bar{B}\) & \(C_{n}\) & \(\overline{F_{i}}\) \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(\mathrm{t}_{\mathrm{PHL}}\)
    \end{tabular} & \(\bar{B}_{i}\) & \(\bar{A}_{i}\) & None & Remaining \(\bar{A}\) to \(\bar{B}\) & \(C_{n}\) & \(\bar{F}_{i}\) \\
    \hline \begin{tabular}{l}
    \(\mathrm{t}_{\mathrm{PLH}}\) \\
    \(t_{\text {PHL }}\)
    \end{tabular} & \(\bar{A}_{i}\) & \(\bar{B}_{i}\) & None & \(\mathrm{C}_{n}\) & Remaining \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}\) & \(\bar{F}_{i}+1\) \\
    \hline \begin{tabular}{l}
    \(t_{\text {pLH }}\) \\
    tpHL
    \end{tabular} & \(\bar{B}_{i}\) & \(\bar{A}_{i}\) & None & \(\mathrm{C}_{\mathrm{n}}\) & Remaining \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}\) & \(\bar{F}_{i}+1\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & \(\bar{A}\) & \(\bar{B}\) & None & None & Remaining \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}}\) & \(\overline{\mathrm{P}}\) \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(t_{\text {PHL }}\)
    \end{tabular} & \(\bar{B}\) & \(\bar{A}\) & None & None & \begin{tabular}{l}
    Remaining \\
    \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}}\)
    \end{tabular} & \(\overline{\mathrm{P}}\) \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    tpHL
    \end{tabular} & \(\overline{\mathrm{A}}\) & None & \(\overline{\text { B }}\) & \[
    \begin{gathered}
    \text { Remaining } \\
    \bar{B} \\
    \hline
    \end{gathered}
    \] & \[
    \begin{aligned}
    & \text { Remaining } \\
    & \overline{\mathrm{A}}, \mathrm{C}_{\mathrm{n}} \\
    & \hline
    \end{aligned}
    \] & \(\overline{\mathrm{G}}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & \(\bar{B}\) & None & \(\bar{A}\) & \[
    \begin{gathered}
    \text { Remaining } \\
    \overline{\mathrm{B}} \\
    \hline
    \end{gathered}
    \] & \[
    \begin{aligned}
    & \text { Remaining } \\
    & \overline{\mathrm{A}}, \mathrm{C}_{\mathrm{n}} \\
    & \hline
    \end{aligned}
    \] & \(\overline{\mathrm{G}}\) \\
    \hline \(t_{\text {PLH }}\)
    \(t_{\text {PHL }}\) & \(\bar{A}\) & None & \(\bar{B}\) & \[
    \begin{aligned}
    & \text { Remaining } \\
    & \bar{B}
    \end{aligned}
    \] & \[
    \begin{aligned}
    & \text { Remaining } \\
    & \overline{\mathrm{A}}, \mathrm{C}_{\mathrm{n}} \\
    & \hline
    \end{aligned}
    \] & \(C_{n+4}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & \(\bar{B}\) & None & \(\bar{A}\) & \[
    \begin{gathered}
    \text { Remaining } \\
    \bar{B}
    \end{gathered}
    \] & Remaining \(\overline{\mathrm{A}}, \mathrm{C}_{\mathrm{n}}\) & \(C_{n+4}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & \(C_{n}\) & None & None & \[
    \begin{aligned}
    & \mathrm{All} \\
    & \overline{\mathrm{~A}}
    \end{aligned}
    \] & \[
    \begin{aligned}
    & \text { All } \\
    & \overline{\mathrm{B}}
    \end{aligned}
    \] & \[
    \begin{gathered}
    \text { Any } \bar{F} \\
    \text { or } C_{n}+4 \\
    \hline
    \end{gathered}
    \] \\
    \hline
    \end{tabular}

    DIFF MODE TEST TABLE II. Function Inputs: \(\mathrm{S} 1=\mathrm{S} 2=4.5 \mathrm{~V}, \mathrm{SO}=\mathrm{S} 3=\mathrm{M}=0 \mathrm{~V}\)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{\begin{tabular}{l}
    Input \\
    Under \\
    Test
    \end{tabular}} & \multicolumn{2}{|c|}{Other Input Same Bit} & \multicolumn{2}{|c|}{Other Data Inputs} & \multirow[t]{2}{*}{\begin{tabular}{l}
    Output \\
    Under \\
    Test
    \end{tabular}} \\
    \hline & & Apply
    \[
    4.5 \mathrm{~V}
    \] & Apply GND & Apply 4.5V & Apply GND & \\
    \hline \(t_{\text {PLH }}\)
    \[
    t_{\mathrm{PHL}}
    \] & \(\overline{\mathrm{A}}\) & None & \(\bar{B}\) & \[
    \begin{gathered}
    \text { Remaining } \\
    \overline{\mathrm{A}} \\
    \hline
    \end{gathered}
    \] & \[
    \begin{gathered}
    \text { Remaining } \\
    \overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}} \\
    \hline
    \end{gathered}
    \] & \(\bar{F}_{i}\) \\
    \hline \[
    t_{\text {PLH }}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & \(\bar{B}\) & \(\bar{A}\) & None & \[
    \begin{gathered}
    \text { Remaining } \\
    \bar{A} \\
    \hline
    \end{gathered}
    \] & \[
    \begin{gathered}
    \text { Remaining } \\
    \bar{B}, C_{n} \\
    \hline
    \end{gathered}
    \] & \(\bar{F}_{i}\) \\
    \hline \begin{tabular}{l}
    tpLH \\
    \(t_{\text {PHL }}\)
    \end{tabular} & \(\bar{A}_{i}\) & None & \(\overline{B_{i}}\) & Remaining \(\bar{B}, C_{n}\) & \[
    \begin{gathered}
    \text { Remaining } \\
    \bar{A} \\
    \hline
    \end{gathered}
    \] & \(\bar{F}_{i}+1\) \\
    \hline \begin{tabular}{l}
    tplH \\
    \(t_{\text {PHL }}\)
    \end{tabular} & \(\bar{B}_{i}\) & \(\bar{A}_{i}\) & None & \[
    \begin{aligned}
    & \text { Remaining } \\
    & \overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}} \\
    & \hline
    \end{aligned}
    \] & \[
    \begin{gathered}
    \text { Remaining } \\
    \bar{A} \\
    \hline
    \end{gathered}
    \] & \(\bar{F}_{i}+1\) \\
    \hline \begin{tabular}{l}
    tpLH \\
    \(t_{\text {PHL }}\)
    \end{tabular} & \(\bar{A}\) & None & \(\bar{B}\) & None & \begin{tabular}{l}
    Remaining \\
    \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}}\)
    \end{tabular} & \(\overline{\text { P }}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & \(\bar{B}\) & \(\bar{A}\) & None & None & Remaining \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}}\) & \(\overline{\mathrm{P}}\) \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & \(\bar{A}\) & \(\bar{B}\) & None & None & Remaining \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}}\) & \(\overline{\mathrm{G}}\) \\
    \hline
    \end{tabular}

    DIFF MODE TEST TABLE II. Function Inputs: \(S 1=S 2=4.5 \mathrm{~V}, \mathrm{SO}=\mathrm{S} 3=\mathrm{M}=0 \mathrm{~V}\) (Continued)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{\begin{tabular}{l}
    Input \\
    Under Test
    \end{tabular}} & \multicolumn{2}{|c|}{Other Input Same Bit} & \multicolumn{2}{|c|}{Other Data Inputs} & \multirow[t]{2}{*}{Output Under Test} \\
    \hline & & \[
    \begin{gathered}
    \text { Apply } \\
    \text { 4.5V }
    \end{gathered}
    \] & Apply GND & \[
    \begin{gathered}
    \text { Apply } \\
    4.5 \mathrm{~V}
    \end{gathered}
    \] & Apply GND & \\
    \hline \[
    \begin{aligned}
    & \text { tpLH } \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & \(\bar{B}\) & None & \(\bar{A}\) & None & Remaining \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}}\) & \(\overline{\mathbf{G}}\) \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(\mathrm{t}_{\mathrm{PHL}}\)
    \end{tabular} & \(\bar{A}\) & None & \(\overline{\text { B }}\) & \[
    \begin{gathered}
    \text { Remaining } \\
    \bar{A}
    \end{gathered}
    \] & Remaining \(\bar{B}, C_{n}\) & \(A=B\) \\
    \hline \[
    t_{p L H}
    \]
    \[
    t_{\mathrm{PHL}}
    \] & \(\bar{B}\) & \(\bar{A}\) & None & \[
    \begin{gathered}
    \text { Remaining } \\
    \overline{\mathrm{A}} \\
    \hline
    \end{gathered}
    \] & Remaining \(\bar{B}, C_{n}\) & \(A=B\) \\
    \hline \[
    \mathrm{t}_{\mathrm{pLH}}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & \(\bar{A}\) & \(\bar{B}\) & None & None & Remaining \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}}\) & \(\mathrm{C}_{\mathrm{n}}+4\) \\
    \hline \[
    t_{\text {PLH }}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & \(\bar{B}\) & None & \(\bar{A}\) & None & Remaining \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}}\) & \(\mathrm{C}_{\mathrm{n}}+4\) \\
    \hline \[
    t_{\text {PLH }}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & \(C_{n}\) & None & None & All \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}\) & None & \(\mathrm{C}_{\mathrm{n}}+4\) \\
    \hline
    \end{tabular}

    LOGIC MODE TEST TABLE III. Function Inputs: \(\mathrm{S} 1=\mathrm{S} 2=\mathrm{M}=4.5 \mathrm{~V}, \mathrm{~S} 0=\mathrm{S} 3=0 \mathrm{~V}\)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline \multirow{2}{*}{Symbol} & \multirow[t]{2}{*}{\begin{tabular}{l}
    Input \\
    Under \\
    Test
    \end{tabular}} & \multicolumn{2}{|c|}{Other Input Same Bit} & \multicolumn{2}{|r|}{Other Data Inputs} & \multirow[t]{2}{*}{Output Under Test} \\
    \hline & & Apply
    \[
    4.5 \mathrm{~V}
    \] & Apply GND & Apply
    \[
    4.5 \mathrm{~V}
    \] & Apply GND & \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}}
    \end{aligned}
    \] & \(\bar{A}\) & \(\bar{B}\) & None & None & Remaining \(\bar{A}\) and \(\bar{B}, C_{n}\) & Any \(\overline{\mathrm{F}}\) \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(\mathrm{t}_{\mathrm{PHL}}\)
    \end{tabular} & \(\bar{B}\) & \(\bar{A}\) & None & None & Remaining \(\overline{\mathrm{A}}\) and \(\overline{\mathrm{B}}, \mathrm{C}_{\mathrm{n}}\) & Any \(\bar{F}\) \\
    \hline
    \end{tabular}

    \section*{DM93S43}

    \section*{4-Bit by 2-Bit Twos Complement Multiplier}

    \section*{General Description}

    The DM93S43 is a high-speed twos complement multiplier. The device is a 4 -bit by 2 -bit building block that can be connected in an iterative array to perform multiplication of
    two binary numbers of variable lengths. The device can generate the twos complement product, without correction, of two binary numbers presented in twos complement notation.

    \section*{Connection Diagram}

    Dual-In-Line Package
    

    \section*{Logic Symbol}
    

    TL/F/9806-2
    \[
    V_{C C}=P \text { in } 24
    \]
    \[
    \text { GND }=\operatorname{Pin} 12
    \]

    Order Number DM93S43N
    See NS Package Number N24A
    \begin{tabular}{|l|l|}
    \hline \multicolumn{1}{|c|}{ Pin Name } & \multicolumn{1}{c|}{ Description } \\
    \hline \(\mathrm{X}-1, \mathrm{X} 3, \mathrm{X} 4\), & Multiplicand Inputs \\
    \(\mathrm{X0}, \mathrm{X} 1, \mathrm{X} 2\) & \\
    \(\mathrm{Y}, \mathrm{Y}-1, \mathrm{Y} 1\) & Multiplier Inputs \\
    \(\mathrm{C}_{n}\) & Carry Input \\
    \(\mathrm{KO}-\mathrm{K} 3\) & Constant Inputs \\
    \(\overline{\mathrm{P}}\) & Polarity Control Input (Active \\
    & Low for High Operands) \\
    S0-S5 & Product Outputs \\
    \(\mathrm{C}_{\mathrm{n}+4}\) & Carry Output \\
    \hline
    \end{tabular}

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    7V
    Input Voltage
    5.5 V

    Operating Free Air Temperature Range
    DM93S
    \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
    Storage Temperature Range \(\quad-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{l|l|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multirow{2}{|c|}{ Parameter } & \multicolumn{2}{|c|}{ DM93S43 } & \multirow{2}{*}{ Units } \\
    \cline { 3 - 5 } & & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 20 & mA \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{1}=-18 \mathrm{~mA}\) & & & -1.2 & V \\
    \hline \(\mathrm{V}_{\mathrm{OH}}\) & High Level Output Voltage & \[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O H}=\operatorname{Max} \\
    & V_{I L}=M a x
    \end{aligned}
    \] & 2.7 & 3.4 & & V \\
    \hline VOL & Low Level Output Voltage & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{IOL}=\mathrm{Max} \\
    & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
    \end{aligned}
    \] & & 0.35 & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{C C}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H}}\) & High Level Input Current & \(\mathrm{V}_{C C}=\operatorname{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\) & & & 40 & \(\mu \mathrm{A}\) \\
    \hline \(1 / 2\) & Low Level Input Current & \(V_{C C}=M a x, V_{1}=0.5 \mathrm{~V}\) & & & -1.6 & mA \\
    \hline los & Short Circuit Output Current & \(V_{C C}=\operatorname{Max}\) (Note 2) & -40 & & -100 & mA \\
    \hline ICC & Supply Current & \(V_{C C}=\operatorname{Max}\) & & & 149 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{Switching Characteristics}
    \(V_{C C}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\(C_{L}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \[
    t_{\text {PLH }}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & Propagation Delay
    \[
    C_{n} \text { to } C_{n}+4
    \] & & \[
    \begin{aligned}
    & 9.0 \\
    & 9.0^{1} . \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay
    \[
    \mathrm{C}_{\mathrm{n}} \text { to } \mathrm{S}_{0}-\mathrm{S}_{3}
    \] & & \[
    \begin{aligned}
    & 13 \\
    & 11
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}}
    \end{aligned}
    \] & Propagation Delay
    \[
    C_{n} \text { to } S_{4}, S_{5}
    \] & & \[
    \begin{aligned}
    & 16 \\
    & 15 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}
    \(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations) (Continued)
    \begin{tabular}{|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{2}{|c|}{\(C_{L}=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
    \hline & & Min & Max & \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay kn to \(\mathrm{C}_{\mathrm{n}}+4\) & & \[
    \begin{aligned}
    & 12 \\
    & 13
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}}
    \end{aligned}
    \] & Propagation Delay kn to S0 - S3 & & \[
    \begin{aligned}
    & 14 \\
    & 12 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    t_{\text {PLH }}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & Propagation Delay kn to S4, S5 & & \[
    \begin{array}{r}
    19 \\
    17 \\
    \hline
    \end{array}
    \] & ns \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    \(t_{\text {PHL }}\)
    \end{tabular} & Propagation Delay xn to \(\mathrm{C}_{\mathrm{n}}+4\) & & \[
    \begin{aligned}
    & 15 \\
    & 24 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay xn to S0 - S3 & & \[
    \begin{array}{r}
    25 \\
    25 \\
    \hline
    \end{array}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathbf{t}_{\mathrm{PLH}} \\
    & \mathbf{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay xn to \(\mathrm{S} 4, \mathrm{~S} 5\) & & \[
    \begin{aligned}
    & 30 \\
    & 21 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    t_{P L H}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & Propagation Delay yn to \(\mathrm{C}_{\mathrm{n}}+4\) & & \[
    \begin{aligned}
    & 25 \\
    & 27 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    \begin{aligned}
    & \mathrm{t}_{\mathrm{PLH}} \\
    & \mathrm{t}_{\mathrm{PHL}} \\
    & \hline
    \end{aligned}
    \] & Propagation Delay yn to S0 - S3 & & \[
    \begin{aligned}
    & 28 \\
    & 27 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \begin{tabular}{l}
    \(t_{\text {PLH }}\) \\
    tphL
    \end{tabular} & Propagation Delay yn to S4, S5 & & \[
    \begin{aligned}
    & 32 \\
    & 30 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}
    ment multiplication of an X -bit number by a Y -bit number. This application requires \(X \bullet Y \div 4 \bullet 2\) packages and the resulting product has \(X+Y\) bits. At the beginning of the array, a constant can be presented at the K inputs that will be added to the least significant part of the product. The packages can be connected in parallel, triangular or split-array scheme depending on the speed requirement. The ' 41 ALU can be used with these multipliers in the split-array scheme to obtain high speed multiplication.

    \section*{Functional Description}

    The DM93S43 is a super fast hardware multiplier employing Schottky technology and twos complement arithmetic. It multiplies a multiplicand of four bits by a multiplier of two bits
    and forms a basic iterative logic cell. It can also multiply in multiplies a multiplicand of four bits by a multiplier of two bits
    and forms a basic iterative logic cell. It can also multiply in active HIGH (positive logic) or active LOW (negative logic)
    representations by reinterpreting the active levels of the inactive HIGH (positive logic) or active LOW (negative logic)
    representations by reinterpreting the active levels of the inputs, outputs and the Polarity Control \((\bar{P})\). The binary number with 1 as the most significant bit is treated as a negative number represented in twos complement form. These DM93S43 iterative logic cells can be connected to imple-

    TABLE I. Switching Test Conditions
    \begin{tabular}{|c|c|c|}
    \hline Input & Outputs & Inputs at OV (Remaining Inputs at 4.5 V) \\
    \hline \(\mathrm{C}_{\mathrm{n}}\) & \(\mathrm{C}_{\mathrm{n}}+4, \mathrm{SO}-\mathrm{S} 3, \mathrm{~S} 4, \mathrm{~S} 5\) & \(\bar{P}, y-1, y 1\) All \(x\) \\
    \hline \[
    \begin{aligned}
    & \text { k0 } \\
    & \text { k1 } \\
    & \text { k2 } \\
    & \text { k3 } \\
    & \text { k3 }
    \end{aligned}
    \] & \[
    \begin{aligned}
    & C_{n}+4, S 0-S 3, S 4, S 5 \\
    & C_{n}+4, S 1-S 3, S 4, S 5 \\
    & C_{n}+4, S 2, S 3, S 4, S 5 \\
    & S 3 \\
    & \text { S4, S5 }
    \end{aligned}
    \] & \begin{tabular}{l}
    \(\overline{\mathrm{P}}, \mathrm{y}-1, \mathrm{y} 1\) All x \\
    \(\overline{\mathrm{P}}, \mathrm{y}-1, \mathrm{y} 1\) All x \\
    \(\bar{P}, y-1, y 1\) All \(x\) \\
    \(\bar{P}, y-1, y 1\) All \(x\) \\
    \(\bar{P}, y-1, y 1\) All \(x, C_{n}\)
    \end{tabular} \\
    \hline \[
    \begin{aligned}
    & x-1 \\
    & x 0 \\
    & x 1 \\
    & x 2 \\
    & x 3, x 4 \\
    & x 3, x 4 \\
    & x 3, x 4
    \end{aligned}
    \] & \[
    \begin{aligned}
    & C_{n}+4, S 0-S 3, S 4, S 5 \\
    & C_{n}+4, S 0-S 3, S 4, S 5 \\
    & C_{n}+4, S 1-S 3, S 4, S 5 \\
    & C_{n}+4, S 2, S 3, S 4, S 5 \\
    & S 3 \\
    & \text { S4,S5 } \\
    & \text { S4,S5 }
    \end{aligned}
    \] & \[
    \begin{aligned}
    & \bar{P}, y-1, \text { All } k \\
    & \bar{P}, y-1, y 1, \text { All } k \\
    & \bar{P}, y-1, y 1, \text { All } k \\
    & \bar{P}, y-1, y 1, \text { All } k \\
    & \bar{P}, y-1, y 1, \text { All } k \\
    & \bar{P}, y-1, y 1, \text { All k, C }
    \end{aligned}
    \] \\
    \hline \[
    \begin{aligned}
    & y-1 \\
    & y 0 \\
    & y 1 \\
    & \hline
    \end{aligned}
    \] & \[
    \begin{aligned}
    & C_{n}+4, S 0-S 3, S 4, S 5 \\
    & C_{n}+4, S 0-S 3, S 4, S 5 \\
    & C_{n}+4, S 0-S 3, S 4, S 5 \\
    & \hline
    \end{aligned}
    \] & \(\bar{P}, x 1, x 2, x 3, x 4\), All \(k\) \(\bar{P}, x 1, x 2, x 3, x 4\), All \(k\) \(x 0, x 1, x 2, x 3, x 4\), All k \\
    \hline
    \end{tabular}

    \section*{Logic Diagram}
    

    \section*{DM93S46}

    High-Speed 6-Bit Identity Comparator

    \section*{General Description}

    The DM93S46 is a very high speed 6-bit identity comparator. The device compares two words of up to six bits and indicates identity in less than 12 ns . It is easily expandable to any word length by using either serial or parallel expansion techniques. When the Enable input ( E ) is LOW, it forces the output LOW.

    \section*{Connection Diagram}

    Dual-In-Line Package
    

    Order Number DM93S46N See NS Package Number N16E

    \section*{Logic Symbol}
    \(V_{C C}=\operatorname{Pin} 16\)
    \(G N D=\operatorname{Pin} 18\)
    

    TL/F/9807-1
    \begin{tabular}{|l|l|}
    \hline Pin Name & \multicolumn{1}{c|}{ Description } \\
    \hline\(A 0-A 5\) & Word A Inputs \\
    B0-B5 & Word B Inputs \\
    E & Enable Input (Active High) \\
    \(\mathrm{A}=\mathrm{B}\) & A Equal to B Output \\
    \hline
    \end{tabular}
    ```

    Absolute Maximum Ratings (Note)
    If Military/Aerospace specified devices are required,
    please contact the National Semiconductor Sales
    Office/Distributors for avallability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature Range
    DM93S
    $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$
    Storage Temperature Range
    $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

    ```

    Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

    \section*{Recommended Operating Conditions}
    \begin{tabular}{c|c|c|c|c|c}
    \hline \multirow{2}{*}{ Symbol } & \multirow{2}{*}{ Parameter } & \multicolumn{2}{|c|}{ DM93S46 } & \multirow{2}{*}{ Units } \\
    \cline { 3 - 4 } & & Min & Nom & Max & \\
    \hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
    \hline \(\mathrm{~V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & V \\
    \hline \(\mathrm{~V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.8 & V \\
    \hline \(\mathrm{I}_{\mathrm{OH}}\) & High Level Output Current & & & -1 & mA \\
    \hline \(\mathrm{I}_{\mathrm{OL}}\) & Low Level Output Current & & & 20 & mA \\
    \hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
    \hline
    \end{tabular}

    Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline Symbol & Parameter & Conditions & Min & \[
    \begin{gathered}
    \text { Typ } \\
    \text { (Note 1) }
    \end{gathered}
    \] & Max & Units \\
    \hline \(V_{1}\) & Input Clamp Voltage & \(V_{C C}=M i n, l_{1}=-18 \mathrm{~mA}\) & & & -1.2 & V \\
    \hline VOH & High Level Output Voltage & \[
    \begin{aligned}
    & V_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
    & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
    \end{aligned}
    \] & 2.7 & 3.4 & & V \\
    \hline \(\mathrm{V}_{\mathrm{OL}}\) & Low Level Output Voltage & \[
    \begin{aligned}
    & V_{C C}=\operatorname{Min}, I_{O L}=\operatorname{Max} \\
    & V_{I H}=\operatorname{Min}
    \end{aligned}
    \] & & 0.35 & 0.5 & V \\
    \hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=5.5 \mathrm{~V}\) & & & 1 & mA \\
    \hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\) & & & 50 & \(\mu \mathrm{A}\) \\
    \hline IIL & Low Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.5 \mathrm{~V}\) & & & -20 & mA \\
    \hline los & Short Circuit Output Current & \[
    \begin{aligned}
    & \mathrm{V}_{\mathrm{CC}}=\text { Max } \\
    & \text { (Note 2) }
    \end{aligned}
    \] & -40 & & -100 & mA \\
    \hline ICC & Supply Current & \(\mathrm{V}_{\text {CC }}=\) Max & & & 70 & mA \\
    \hline
    \end{tabular}

    Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
    Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

    \section*{Switching Characteristics}
    \(V_{C C}=+5.0 \mathrm{~V}, T_{A}=+25^{\circ} \mathrm{C}\) (See Section 1 for waveforms and load configurations)
    \begin{tabular}{|c|c|c|c|c|c|}
    \hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Conditions} & \multicolumn{2}{|c|}{\(C L=15 \mathrm{pF}\)} & \multirow[t]{2}{*}{Units} \\
    \hline & & & Min & Max & \\
    \hline \[
    t_{\text {PLH }}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & Propagation Delay \(A_{n}\) or \(B_{n}\) to \(A=B\) & \begin{tabular}{l}
    \[
    E=4.5 \mathrm{~V}, \text { Other Inputs }=4.5 \mathrm{~V}
    \] \\
    Test Each Input Individually
    \end{tabular} & \[
    \begin{aligned}
    & 3.0 \\
    & 3.0 \\
    & \hline
    \end{aligned}
    \] & \[
    \begin{aligned}
    & 17 \\
    & 17 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline \[
    t_{\text {PLH }}
    \]
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & Propagation Delay \(A_{n}\) or \(B_{n}\) to \(A=B\) & \(E=4.5 \mathrm{~V}\), Other Inputs \(=\) Gnd, Test Each Input Individually & \[
    \begin{aligned}
    & 3.0 \\
    & 3.0 \\
    & \hline
    \end{aligned}
    \] & \[
    \begin{aligned}
    & 14 \\
    & 15 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline tpLH
    \[
    \mathrm{t}_{\mathrm{PHL}}
    \] & Propagation Delay \(E\) to \(A=B\) & \(A_{n}=B_{n}\) & \[
    \begin{aligned}
    & 2.0 \\
    & 2.0
    \end{aligned}
    \] & \[
    \begin{aligned}
    & 10 \\
    & 10 \\
    & \hline
    \end{aligned}
    \] & ns \\
    \hline
    \end{tabular}

    \section*{Functional Description}

    The DM93S46 is a very high speed 6-bit identity comparator. The \(A=B\) output is HIGH when the Enable ( \(E\) ) is HIGH and the two 6-bit words are equal. Equality is determined by Exclusive-NOR circuits which individually compare the equivalent bits from each word. When any two of the equivalent bits from each word have different logic levels, the A \(=B\) output is LOW.
    \[
    \begin{aligned}
    (A=B)= & (A \overline{0} \oplus B 0) \cdot(A \overline{A 1 \oplus B 1}) \cdot(A \bar{A} \oplus \overline{B 2}) \bullet \\
    & (\overline{A 3 \oplus B 3}) \cdot(\overline{A 4 \oplus B 4}) \bullet(\overline{A 5 \oplus B 5}) \bullet E
    \end{aligned}
    \]

    An active HIGH Enable (E) provides a means of fast ripple expansion. By connecting the \(A=B\) output of the first stage of the comparator to the enable of the next stage, the comparator can be expanded in 6-bit increments at an addtional 4.5 ns per stage. An even faster expansion technique is achieved by connecting the \(\mathrm{A}=\mathrm{B}\) outputs to a Schottky NAND gate. This method compares two words of up to 78 bits each in 15 ns (typical) using the '133 13-input Schottky NAND gate.

    \section*{Truth Table}
    \begin{tabular}{|c|c|c|}
    \hline \multicolumn{2}{|c|}{ Inputs } & Output \\
    \hline\(E\) & \(A_{\mathbf{n}}, B_{\mathbf{n}}\) & \(\mathbf{A}=\mathbf{B}\) \\
    \hline\(L\) & \(A_{n}=B_{n}\) & \(L\) \\
    \(L\) & \(A_{n} \neq B_{n}\) & \(L\) \\
    \(H\) & \(A_{n} \neq B_{n}\) & \(L\) \\
    \(H\) & \(A_{n}=B_{n}\) & \(H\) \\
    \hline
    \end{tabular}
    \(H=H I G H\) Voltage Level
    \(L=\) LOW Voltage Level

    \section*{Logic Diagram}
    

    \section*{Ripple Expansion}
    

    Note: This simple method of expansion adds 4.5 ns for each additional ' 46 used.
    

    TL/F/9807-4
    Note: This method of expansion adds one gate delay ( \(\cong 3 \mathrm{~ns}\) ) to the ' 46 , independent of the word length that is compared.

    \section*{DM93S47}

    High Speed 6-Bit Identity Comparator

    \section*{General Description}

    The DM93S47 is a very high speed 6-bit identity comparator. The device features an open-collector output for wiredOR expansion and active LOW enable. The DM93S47 is fabricated with the Schottky barrier diode process for high speed, and is completely compatible with all TTL families.

    This device is recommended for applications where wiredOR expansion is desired and the speed of an active pull-up is not required. The DM93S47 is a pin-for-pin replacement for the DM7160/8160.

    \section*{Connection Diagram}
     See NS Package Number N16E

    \section*{Logic Symbol}
    

    \section*{Truth Table}
    \begin{tabular}{|c|c|c|}
    \hline \multicolumn{2}{|c|}{ Inputs } & Output \\
    \hline \(\bar{E}\) & \(A_{n}, B_{n}\) & \(\mathbf{A}=\mathbf{B}\) \\
    \hline\(L\) & \(A_{n}=B_{n}\) & \(H\) \\
    \(L\) & \(A_{n} \neq B_{n}\) & \(L\) \\
    \(H\) & \(A_{n} \neq B_{n}\) & \(H\) \\
    \(H\) & \(A_{n}=B_{n}\) & \(H\) \\
    \hline
    \end{tabular}

    \footnotetext{
    \(H=H I G H\) Voltage Level
    L = LOW Voltage Level
    }

    \section*{Absolute Maximum Ratings (Note)}

    If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
    Supply Voltage
    Input Voltage
    Operating Free Air Temperature
    Range (DM93S)
    Storage Temperature Range
    5.5 V
    5.5V
    \circ```

