

Specifying A/D and D/A Converters

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The specification or selection of analog-to-digital (A/D) or digital-to-analog (D/A) converters can be a chancey thing unless the specifications are understood by the person making the selection. Of course, you know you want an accurate converter of specific resolution; but how do you ensure that you get what you want? For example, 12 switches, 12 arbitrarily valued resistors, and a reference will produce a 12-bit DAC exhibiting 12 quantum steps of output voltage. In all probability, the user wants something better than the expected performance of such a DAC. Specifying a 12-bit DAC or an ADC must be made with a full understanding of accuracy, linearity, differential linearity, monotonicity, scale, gain, offset, and hysteresis errors.

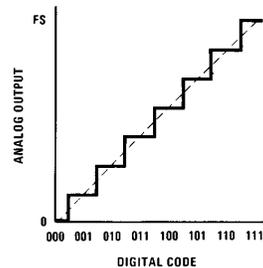
This note explains the meanings of and the relationships between the various specifications encountered in A/D and D/A converter descriptions. It is intended that the meanings be presented in the simplest and clearest practical terms. Included are transfer curves showing the several types of errors discussed. Timing and control signals and several binary codes are described as they relate to A/D and D/A converters.

MEANING OF PERFORMANCE SPECS

Resolution describes the smallest standard incremental change in output voltage of a DAC or the amount of input voltage change required to increment the output of an ADC between one code change and the next adjacent code change. A converter with n switches can resolve 1 part in 2^n . The least significant increment is then 2^{-n} , or one least significant bit (LSB). In contrast, the most significant bit (MSB) carries a weight of 2^{-1} . Resolution applies to DACs and ADCs, and may be expressed in percent of full scale or in binary bits. For example, an ADC with 12-bit resolution could resolve 1 part in 2^{12} (1 part in 4096) or 0.0244% of full scale. A converter with 10V full scale could resolve a 2.44mV input change. Likewise, a 12-bit DAC would exhibit an output voltage change of 0.0244% of full scale when the binary input code is incremented one binary bit (1 LSB). Resolution is a design parameter rather than a performance specification; it says nothing about accuracy or linearity.

Accuracy is sometimes considered to be a non-specific term when applied to D/A or A/D converters. A linearity spec is generally considered as more descriptive. An accuracy specification describes the worst case deviation of the DAC output voltage from a straight line drawn between zero and full scale; it includes all errors. A 12-bit DAC could not have a conversion accuracy better than $\pm 1/2$ LSB or ± 1 part in $2^{12} + 1$ ($\pm 0.0122\%$ of full scale) due to finite resolution. This would be the case in *Figure 1* if there were no errors. Actually, $\pm 0.0122\%$ FS represents a deviation from 100% accuracy; therefore accuracy should be specified as 99.9878%. However, convention would dictate 0.0122% as being an accuracy spec rather than an inaccuracy (tolerance or error) spec.

Accuracy as applied to an ADC would describe the difference between the actual input voltage and the full-scale weighted equivalent of the binary output code; included are quantizing and all other errors. If a 12-bit ADC is stated to be ± 1 LSB accurate, this is equivalent to $\pm 0.0245\%$ or twice the minimum possible quantizing error of 0.0122%. An accuracy spec describes the maximum sum of all errors including quantizing error, but is rarely provided on data sheets as the several errors are listed separately.



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FIGURE 1. Linear DAC Transfer Curve Showing Minimum Resolution Error and Best Possible Accuracy

Quantizing Error is the maximum deviation from a straight line transfer function of a perfect ADC. As, by its very nature, an ADC quantizes the analog input into a finite number of output codes, only an infinite resolution ADC would exhibit zero quantizing error. A perfect ADC, suitably offset $\frac{1}{2}$ LSB at zero scale as shown in *Figure 2*, exhibits only $\pm\frac{1}{2}$ LSB maximum output error. If not offset, the error will be $\frac{-1}{+0}$ LSB as shown in *Figure 3*. For example, a perfect 12-bit ADC will show a $\pm\frac{1}{2}$ LSB error of $\pm 0.0122\%$ while the quantizing error of an 8-bit ADC is $\pm\frac{1}{2}$ part in 2^8 or $\pm 0.195\%$ of full scale. Quantizing error is not strictly applicable to a DAC; the equivalent effect is more properly a resolution error.

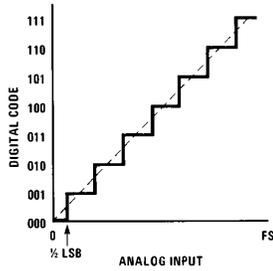


FIGURE 2. ADC Transfer Curve, $\frac{1}{2}$ LSB Offset at Zero

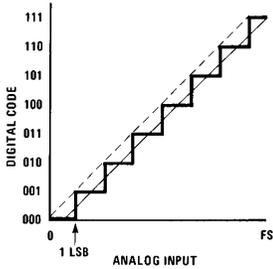


FIGURE 3. ADC Transfer Curve, No Offset

Scale Error (full scale error) is the departure from design output voltage of a DAC for a given input code, usually full-scale code. (See *Figure 4*.) In an ADC it is the departure of actual input voltage from design input voltage for a full-scale output code. Scale errors can be caused by errors in reference voltage, ladder resistor values, or amplifier gain, *et. al.* (See **Temperature Coefficient**.) Scale errors may be corrected by adjusting output amplifier gain or reference voltage. If the transfer curve resembles that of *Figure 7*, a scale adjustment at $\frac{3}{4}$ scale could improve the overall \pm accuracy compared to an adjustment at full scale.

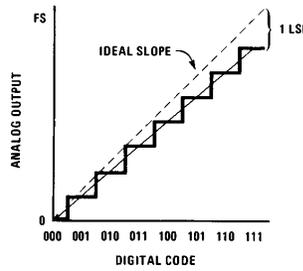


FIGURE 4. Linear, 1 LSB Scale Error

Gain Error is essentially the same as scale error for an ADC. In the case of a DAC with current and voltage mode outputs, the current output could be to scale while the voltage output could exhibit a gain error. The amplifier feedback resistors would be trimmed to correct the gain error.

Offset Error (zero error) is the output voltage of a DAC with zero code input, or it is the required mean value of input voltage of an ADC to set zero code out. (See *Figure 5*.) Offset error is usually caused by amplifier or comparator input offset voltage or current; it can usually be trimmed to zero with an offset zero adjust potentiometer external to the DAC or ADC. Offset error may be expressed in % FS or in fractional LSB.

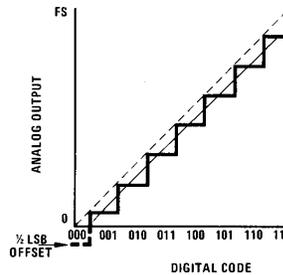


FIGURE 5. DAC Transfer Curve, $\frac{1}{2}$ LSB Offset at Zero

Hysteresis Error in an ADC causes the voltage at which a code transition occurs to be dependent upon the direction from which the transition is approached. This is usually caused by hysteresis in the comparator inside an ADC. Excessive hysteresis may be reduced by design; however, some slight hysteresis is inevitable and may be objectionable in converters if hysteresis approaches $\frac{1}{2}$ LSB.

Linearity, or, more accurately, non-linearity specifications describe the departure from a linear transfer curve for either an ADC or a DAC. Linearity error does not include quantizing, zero, or scale errors. Thus, a specification of $\pm\frac{1}{2}$ LSB

linearity implies error in addition to the inherent $\pm 1/2$ LSB quantizing or resolution error. In reference to *Figure 2*, showing no errors other than quantizing error, a linearity error allows for one or more of the steps being greater or less than the ideal shown.

Figure 6 shows a 3-bit DAC transfer curve with no more than $\pm 1/2$ LSB non-linearity, yet one step shown is of zero amplitude. This is within the specification, as the maximum deviation from the ideal straight line is ± 1 LSB ($1/2$ LSB resolution error plus $1/2$ LSB non-linearity). With any linearity error, there is a differential non-linearity (see below). A $\pm 1/2$ LSB linearity spec guarantees monotonicity (see below) and $\leq \pm 1$ LSB differential non-linearity (see below). In the example of *Figure 6*, the code transition from 100 to 101 is the worst possible non-linearity, being the transition from 1 LSB high at code 100 to 1 LSB low at 110. Any fractional non-linearity beyond $\pm 1/2$ LSB will allow for a non-monotonic transfer curve. *Figure 7* shows a typical non-linear curve; non-linearity is $1 1/4$ LSB yet the curve is smooth and monotonic.

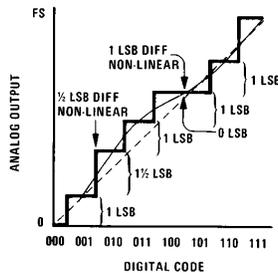


FIGURE 6. $\pm 1/2$ LSB Non-Linearity (Implies 1 LSB Possible Error), 1 LSB Differential Non-Linearity (Implies Monotonicity)

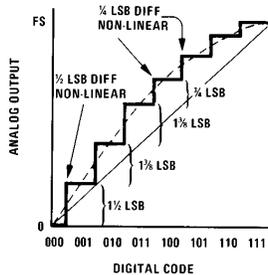


FIGURE 7. $1 1/4$ LSB Non-Linear, $1/2$ LSB Differential Non-Linearity

Linearity specs refer to either ADCs or to DACs, and do not include quantizing, gain, offset, or scale errors. Linearity errors are of prime importance along with differential linearity in either ADC or DAC specs, as all other errors (except quantizing, and temperature and long-term drifts) may be adjusted to zero. Linearity errors may be expressed in % FS or fractional LSB.

Differential Non-Linearity indicates the difference between actual analog voltage change and the ideal (1 LSB) voltage change at any code change of a DAC. For example, a DAC with a 1.5 LSB step at a code change would be said to exhibit $1/2$ LSB differential non-linearity (see *Figures 6* and *7*). Differential non-linearity may be expressed in fractional bits or in % FS.

Differential linearity specs are just as important as linearity specs because the apparent quality of a converter curve can be significantly affected by differential non-linearity even though the linearity spec is good. *Figure 6* shows a curve with a $\pm 1/2$ LSB linearity and ± 1 LSB differential non-linearity while *Figure 7* shows a curve with $+ 1 1/4$ LSB linearity and $\pm 1/2$ LSB differential non-linearity. In many user applications, the curve of *Figure 7* would be preferred over that of *Figure 6* because the curve is smoother. The differential non-linearity spec describes the smoothness of a curve; therefore it is of great importance to the user. A gross example of differential non-linearity is shown in *Figure 8* where the linearity spec is ± 1 LSB and the differential linearity spec is ± 2 LSB. The effect is to allow a transfer curve with grossly degraded resolution; the normal 8-step curve is reduced to 3 steps in *Figure 8*. Similarly, a 16-step curve (4-bit converter) with only 2 LSB differential non-linearity could be reduced to 6 steps (a 2.6-bit converter?). The real message is, "Beware of the specs." Do not ignore or omit differential linearity characteristics on a converter unless the linearity spec is tight enough to guarantee the desired differential linearity. As this characteristic is impractical to measure on a production basis, it is rarely, if ever, specified, and linearity is the primary specified parameter. Differential non-linearity can always be as much as twice the non-linearity, but no more.

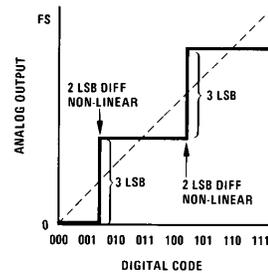


FIGURE 8. ± 1 LSB Linear, ± 2 LSB Differential Non-Linear

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Monotonicity. A monotonic curve has no change in sign of the slope; thus all incremental elements of a monotonically increasing curve will have positive or zero, but never negative slope. The converse is true for decreasing curves. The transfer curve of a monotonic DAC will contain steps of only positive or zero height, and no negative steps. Thus a smooth line connecting all output voltage points will contain no peaks or dips. The transfer function of a monotonic ADC will provide no decreasing output code for increasing input voltage.

Figure 9 shows a non-monotonic DAC transfer curve. For the curve to be non-monotonic, the linearity error must exceed $\pm 1/2$ LSB no matter by how little. The greater the linearity error, the more significant the negative step might be. A non-monotonic curve may not be a special disadvantage in some systems; however, it is a disaster in closed-loop servo systems of any type (including a DAC-controlled ADC). A $\pm 1/2$ LSB maximum linearity spec on an n-bit converter guarantees monotonicity to n bits. A converter exhibiting more than $\pm 1/2$ LSB non-linearity may be monotonic, but is not necessarily monotonic. For example, a 12-bit DAC with $\pm 1/2$ bit linearity to 10 bits (not $\pm 1/2$ LSB) will be monotonic at 10 bits but may or may not be monotonic at 12 bits unless tested and guaranteed to be 12-bit monotonic.

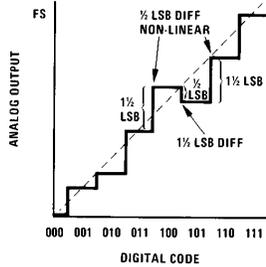


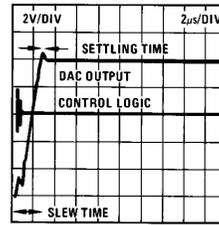
FIGURE 9. Non-Monotonic
(Must be $> \pm 1/2$ LSB Non-Linear)

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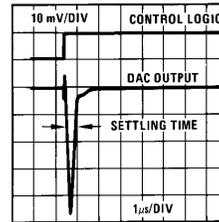
Settling Time is the elapsed time after a code transition for DAC output to reach final value within specified limits, usually $\pm 1/2$ LSB. (See also **Conversion Rate** below.) Settling time is often listed along with a slew rate specification; if so, it may not include slew time. If no slew rate spec is included, the settling time spec must be expected to include slew time. Settling time is usually summed with slew time to obtain total elapsed time for the output to settle to final value. Figure 10 delineates that part of the total elapsed time which is considered to be slew and that part which is settling time. It is apparent from this figure that the total time is greater for a major than for a minor code change due to amplifier slew limitations, but settling time may also be different depending upon amplifier overload recovery characteristics.

Slew Rate is an inherent limitation of the output amplifier in a DAC which limits the rate of change of output voltage after code transitions. Slew rate is usually anywhere from 0.2 to several hundred volts/ μ s. Delay in reaching final value of DAC output voltage is the sum of slew time and settling time as shown in Figure 10.

Overshoot and Glitches occur whenever a code transition occurs in a DAC. There are two causes. The current output of a DAC contains switching glitches due to possible asynchronous switching of the bit currents (expected to be worst at half-scale transition when all bits are switched). These



(a) Full-Scale Step



(b) 1 LSB Step

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FIGURE 10. DAC Slew and Settling Time

glitches are normally of extremely short duration but could be of $1/2$ scale amplitude. The current switching glitches are generally somewhat attenuated at the voltage output of the DAC because the output amplifier is unable to slew at a very high rate; they are, however, partially coupled around the amplifier via the amplifier feedback network and seen at the output. The output amplifier introduces overshoot and some non-critically damped ringing which may be minimized but not entirely eliminated except at the expense of slew rate and settling time.

Temperature Coefficient of the various components of a DAC or ADC can produce or increase any of the several errors as the operating temperature varies. Zero scale offset error can change due to the TC of the amplifier and comparator input offset voltages and currents. Scale error can occur due to shifts in the reference, changes in ladder resistance or non-compensating RC product shifts in dual-slope ADCs, changes in beta or reference current in current switches, changes in amplifier bias current, or drift in amplifier gain-set resistors. Linearity and monotonicity of the DAC can be affected by differential temperature drifts of the ladder resistors and switches. Overshoot, settling time, and slew rate can be affected by temperature due to internal change in amplifier gain and bandwidth. In short, every specification except resolution and quantizing error can be affected by temperature changes.

Long-Term Drift, due mainly to resistor and semiconductor aging can affect all those characteristics which temperature change can affect. Characteristics most commonly affected are linearity, monotonicity, scale, and offset. Scale change due to reference aging is usually the most important change.

Supply Rejection relates to the ability of a DAC or ADC to maintain scale, offset, TC, slew rate, and linearity when the supply voltage is varied. The reference must, of course, remain constant unless considering a multiplying DAC. Most affected are current sources (affecting linearity and scale) and amplifiers or comparators (affecting offset and slew rate). Supply rejection is usually specified only as a % FS change at or near full scale at 25°C.

Conversion Rate is the speed at which an ADC or DAC can make repetitive data conversions. It is affected by propagation delay in counting circuits, ladder switches and comparators; ladder RC and amplifier settling times; amplifier and comparator slew rates; and integrating time of dual-slope converters. Conversion rate is specified as a number of conversions per second, or conversion time is specified as a number of microseconds to complete one conversion (including the effects of settling time). Sometimes, conversion rate is specified for less than full resolution, thus showing a misleading (high) rate.

Clock Rate is the minimum or maximum pulse rate at which ADC counters may be driven. There is a fixed relationship between the minimum conversion rate and the clock rate depending upon the converter accuracy and type. All factors which affect conversion rate of an ADC limit the clock rate.

Input Impedance of an ADC describes the load placed on the analog source.

Output Drive Capability describes the digital load driving capability of an ADC or the analog load driving capacity of a DAC; it is usually given as a current level or a voltage output into a given load.

CODES

Several types of DAC input or ADC output codes are in common use. Each has its advantages depending upon the system interfacing the converter. Most codes are binary in form; each is described and compared below.

Natural Binary (or simply Binary) is the usual 2^n code with 2, 4, 8, 16, . . . , 2^n progression. An input or output high or "1" is considered a signal, whereas a "0" is considered an absence of signal. This is a positive true binary signal. Zero scale is then all "zeros" while full scale is all "ones."

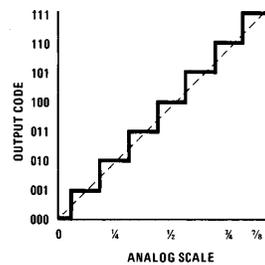
Complementary Binary (or Inverted Binary) is the negative true binary system. It is identical to the binary code except that all binary bits are inverted. Thus, zero scale is all "ones" while full scale is all "zeros."

Binary Coded Decimal (BCD) is the representation of decimal numbers in binary form. It is useful in ADC systems intended to drive decimal displays. Its advantage over decimal is that only 4 lines are needed to represent 10 digits. The disadvantage of coding DACs or ADCs in BCD is that a full 4 bits could represent 16 digits while only 10 are represented in BCD. The full-scale resolution of a BCD coded system is less than that of a binary coded system. For

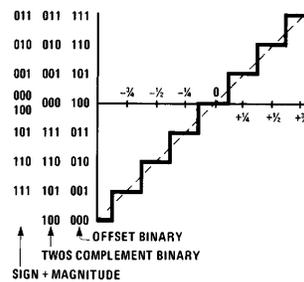
example, a 12-bit BCD system has a resolution of only 1 part in 1000 compared to 1 part in 4096 for a binary system. This represents a loss in resolution of over 4:1.

Offset Binary is a natural binary code except that it is offset (usually $\frac{1}{2}$ scale) in order to represent negative and positive values. Maximum negative scale is represented to be all "zeros" while maximum positive scale is represented as all "ones." Zero scale (actually center scale) is then represented as a leading "one" and all remaining "zeros." The comparison with binary is shown in Figure 11.

Two's Complement Binary is an alternate and more widely used code to represent negative values. With this code, zero and positive values are represented as in natural binary while all negative values are represented in a twos complement form. That is, the twos complement of a number represents a negative value so that interface to a computer or microprocessor is simplified. The twos complement is formed by complementing each bit and then adding a 1; any overflow is neglected. The decimal number -8 is represented in twos complement as follows: start with binary code of decimal 8 (off scale for \pm representation in 4 bits so not a valid code in the \pm scale of 4 bits) which is 1000; complement it to 0111; add 0001 to get 1000. The comparison with offset binary is shown in Figure 11. Note that the offset binary representation of the \pm scale differs from the twos complement representation only in that the MSB is complemented. The conversion from offset binary to twos complement only requires that the MSB be inverted.



(a) Zero to + Full-Scale



(b) \pm Full-Scale

FIGURE 11. ADC Codes

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Sign Plus Magnitude coding contains polarity information in the MSB (MSB = 1 indicates a negative sign); all other bits represent magnitude only. This code is compared to offset binary and twos complement in *Figure 11*. Note that one code is used up in providing a double code for zero. Sign plus magnitude code is used in certain instrument and audio systems; its advantage is that only one bit need be changed for small scale changes in the vicinity of zero, and plus and minus scales are symmetrical. A DVM might be an example of its use.

CONTROL

Each ADC must accept and/or provide digital control signals telling it and/or the external system what to do and when to do it. Control signals should be compatible with one or more types of logic in common use. Control signal timing must be such that the converter or connected system will accept the signals. Common control signals are listed below.

Start Conversion (SC) is a digital signal to an ADC which initiates a single conversion cycle. Typically, an SC signal must be present at the fall (or rise) of the clock waveform to initiate the cycle. A DAC needs no SC signal; however, such could be provided to gate digital inputs to a DAC.

End of Conversion (EOC) is a digital signal from an ADC which informs the external system that the digital output

data is valid. Typically, an EOC output can be connected to an SC input to cause the ADC to operate in continuous conversion mode. In non-continuous conversion systems, the SC signal is a command from the system to the ADC. A DAC does not supply an EOC signal.

Clock signals are required or must be generated within an ADC to control counting or successive approximation registers. The clock controls the conversion speed within the limitations of the ADC. DACs do not require clock signals.

CONCLUSION

Once the user has a working knowledge of DAC or ADC characteristics and specifications, he should be able to select a converter to suit a specific system need. The likelihood of overspecification, and therefore an unnecessarily high cost, is likewise reduced. The user will also be aware that specific parameters, test conditions, test circuits, and even definitions may vary from manufacturer to manufacturer. For practical production reasons, parameters may not be tested in the same manner for all converter types, even those supplied by the same manufacturer. Using information in this note, the user should, however, be able to sort out and understand those specifications (from any manufacturer) pertinent to his needs.

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