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High-Performance Internal Product Portfolio Overview

Issue 4
Fourth Quarter, 1993

MOTOROLA

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PREFACE

Welcome to the High-Performance MPU Marketing Group in Austin.

This document has been prepared as a quarterly guide to the broad range of 16- and 32-bit microprocessors available from Motorola. It is intended to be a handy reference guide to Motorola's MPU portfolio that complements the other sources of technical product information.

Our High Performance product family is still growing rapidly. The 68000 family continues to win new customers with increasing levels of integration, low-power operation, and high-performance networking solutions that improve price/performance thus enabling our customers to develop new market segments. The large base of installed software and development environments available for the family make the 68000 Family the processor of choice for the embedded control world.

Because of the increasing complexity and range of our products, the tools we provide to the field need to be appropriate and user friendly. Thus, we have tried to produce this document in a similar format to other offerings from High-Performance MPU division, but we appreciate your comments both on the style and content. A short questionnaire is included at the end of this document for this purpose.

If you have any questions, please do not hesitate to call either your local High-Performance PME or the factory Technical Marketing Group.

Table of Contents

M68000 FAMILY STRATEGY

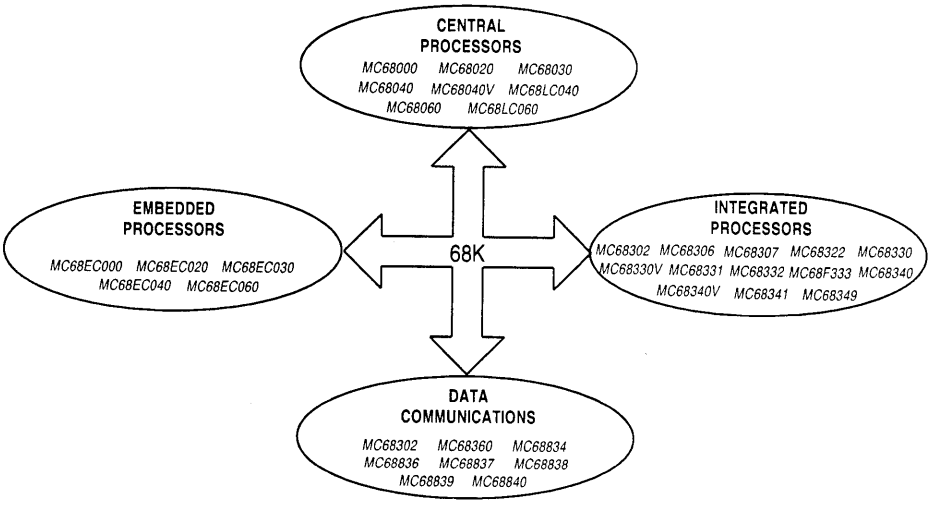
The M68000 family is already the industry standard in computing and embedded control applications.

Markets:

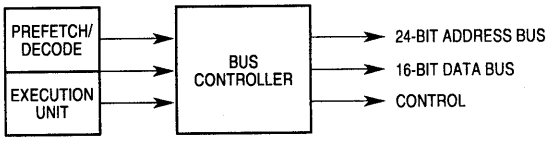
- Low-to Mid-Range Computing
- Laptop and Hand-Held Computing
- Telecommunications (digital switches, SDH platforms, PABX)
- Office Automation (printers, faxes, servers, X-terminals)
- Network Controllers
- Consumer Products

The M68000 family provides industry-standard architecture in an extremely cost- effective package/solution. Solutions are available from less than $3 to more than 40 MIPS with an excellent migration path.

M68000 FAMILY ROADMAP



MC68000/MC68HC000



Features:

- 24-Bit Address Bus, 16-Bit Data Bus
- 16 32-Bit Registers
- 7 Interrupt Levels
- 2.7 MIPS Performance at 16 MHz

Target Markets/Applications:

The 68000 processor is the foundation of the 68000 Family and is based on the full 32-bit family architecture. It is an ideal choice for performance upgrades from existing 8-bit applications. Applications range from high-end printers and modems to dumb and intelligent terminals. The low-power 68HC000 is an ideal device for applications where the processing power of the 68000 is required but power consumption is an issue.

Also see MC68306 and 68307.

Competitive Advantages:

Intel 8085: Similar performance but limited migration path to higher performance Microprocessors

Literature:

Title	Order Number
MC68000 Technical Summary	MC68000/D
M68000 User's Manual	M68000UM/AD Rev 8
M68000 Programmer's Reference Manual	M68000PM/AD
68000 Family Fact Sheet	BR1115/D

Support Tools:

M68EC000IDP—Integrated Development Platform: hardware/software evaluation module

Third party support listed in *The 68K Source* 1993 Edition BR729/D.

Support Chips:

MC68440/450—DMA Controllers

MC68901—Multifunction Peripheral

MC68230—Parallel Interface Timer

MC68681—DUART

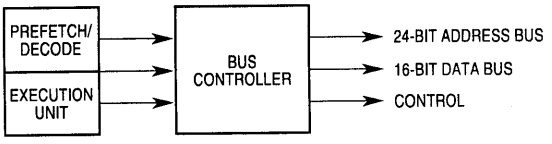
MC68HC05I8—MCU

Package/Speed Options:

Device	Package	Speed	Order Quantity
MC68000	64-lead L *	8, 10, 12	MPQ = 6
	64-lead P	8, 10, 12, 12F*	MPQ = 6
	68-lead R, RC*	8, 10, 12	MPQ = 21
	68-lead FN	8, 10, 12, 12F	MPQ = 19
SPAK000FN	68-lead FN	8, 10, 12, 12F*	SOQ = 2
SPAK000RC	68-lead RC	8, 10, 12	SOQ = 2
MC68HC000	64-lead P	8, 10, 12, 16	MPQ = 6
	68-lead R, RC*	8, 10, 12, 16	MPQ = 21
	68-lead FN	8, 10, 12, 16	MPQ = 19
	68-lead FC	8, 10, 12, 16	MPQ = 78
SPAKHC000FN	68-lead FN	8, 10, 12, 16	SOQ = 2
SPAKHC000FC	68-lead FC	8, 10, 12, 16	SOQ = 2
SPAKHC000P	64-lead P	8, 10, 12, 16	SOQ = 2
SPAKHC000RC	68-lead RC	8, 10, 12, 16	SOQ = 2

NOTE: L = Ceramic DIP
P = Plastic DIP
R = Pin Grid Array
RC = Pin Grid Array, Gold Lead Finish
FN = Plastic Leaded Chip Carrier (PLCC)
MPQ = Minimum Package Quantity
* Not recommended for new designs

MC68EC000



Features:

- 24-Bit Address Bus, 16-Bit Data Bus
- 16 32-Bit Registers
- Interrupt Levels
- 2.7 MIPS Performance at 16.67 MHz

Target Markets/Applications:

The 68EC000 represents the most inexpensive entry point to any 32-bit architecture. Upward migration to higher performance processors is possible because of software compatibility of the architecture. CMOS process ensures low power consumption. Target applications are PABX low level, line cards, GSM fax, modems, industrial control, instrumentation, etc.

Also see MC68306 and 68307.

Competitive Advantages:

Z80: Low cost but limited performance upgrade potential

8086/88: Requires external support chips to avoid technical limitations

Literature:

Title	Order Number
MC68EC000 Technical Summary	MC68EC000/D
M68000 User's Manual	M68000UM/AD Rev 8
M68000 Programmer's Reference Manual	M68000PM/AD
68EC0x0 Family Fact Brochure	BR1109/D

Support Tools:

M68EC000IDP—Integrated Development Platform: hardware/software evaluation module

Third party support listed in *The 68K Source* 1993 Edition BR729/D.

Support Chips:

MC68440/450—DMA Controllers

MC68901—Multifunction Peripheral

MC68230—Parallel Interface Timer

MC68681—DUART

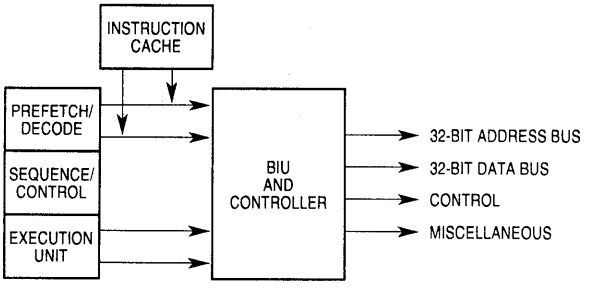
MC68HC05I8—MCU

Package/Speed Options:

Device	Package	Speed	Order Quantity
MC68EC000	68-lead FN	8, 10, 12, 16	MPQ = 19
	64-lead FU	8, 10, 12, 16	MPQ = 84
SPAKEC000	68-lead FN	8, 10, 12, 16	SOQ = 2
	64-lead FU	8, 10, 12, 16	SOQ = 2

NOTE: FN = Plastic Leaded Chip Carrier (PLCC)
FU = Plastic Quad Flat Pack
MPQ = Minimum Package Quantity

MC68020



Features:

- 32-Bit Address Bus, 32-Bit Data Bus
- 256-Byte Instruction Cache
- Coprocessor Interface
- 9.8 MIPS/0.25MFLOPS Performance at 33 MHz

Target Markets/Applications:

The 68020 is the first microprocessor to use a full 32-bit internal and external architecture and offers a vast increase in performance over 8- and 16-bit processors. The dynamic bus feature improves system flexibility, which allows use of 8- or 16-bit peripherals. The MC68EC020 should also be considered unless there is a clear need for a 32-bit address bus.

Literature:

Title	Order Number
MC68020 Technical Summary (Rev 4)	MC68020/D
M68020 User's Manual	M68020UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD

Support Tools:

M68EC020IDP—Integrated Development Platform: hardware/software evaluation module

Third party support listed in *The 68K Source* 1993 Edition BR729/D.

Support Chips:

MC68882—Enhanced Floating-Point Coprocessor

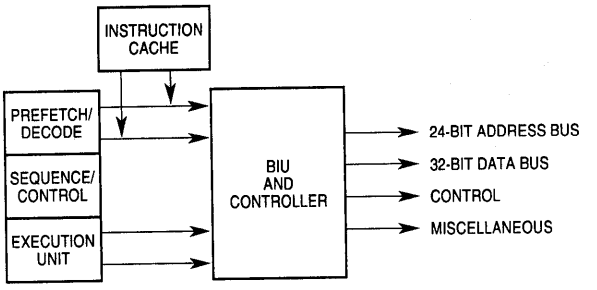
Package/Speed Options:

Device	Package	Speed	Rev	Order Quantity
MC68020	144-lead RC, RP	16, 20, 25, 33*	E	MPQ = 1
	132-lead FE** FC	16, 20, 25, 33	E	MPQ = 36
SPAK020	132-lead FE, FC	16, 20, 25, 33	E	SOQ = 2

NOTE: RC = Pin Grid Array, Gold Lead Finish
RP = Plastic Pin Grid Array
FE = Ceramic Quad Flat Pack (CQFP)
FC = Plastic Quad Flat Pack (PQFP)
MPQ = Minimum Package Quantity

*Available in RC package only
** Not recommended for new designs.

MC68EC020



Features:

- 24-Bit Address Bus, 32-Bit Data Bus
- 256-Byte Instruction Cache
- Coprocessor Interface
- 7.4 MIPS Performance at 25 MHz

Target Markets/Applications:

The strategy behind the 68EC020 is to upgrade current 68000 and 68HC000 users to a higher performance product with minimum increase in device or system cost. Key applications are PABX low level, GSM basestations, network controllers, printers, dumb terminals, robotics, VME boards, instrumentation, etc. The MC68EC020 has a 24-bit address bus and does not support extended temperature.

Competitive Advantages:

960SA: Similar price range, but overall system cost increased due to extra logic

960SB: On-chip floating point unit. Can be attacked with higher performance 68EC020/68882 combination at aggressive price

Literature:

Title	Order Number
MC68EC020 Technical Summary	MC68EC020/D
M68020 User's Manual	M68020UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD
68EC0x0 Family Fact Brochure	BR1109/D

Support Tools:

M68EC020IDP—Integrated Development Platform: hardware/software evaluation module.

Third party support listed in *The 68K Source* 1993 Edition BR729/D.

Support Chips:

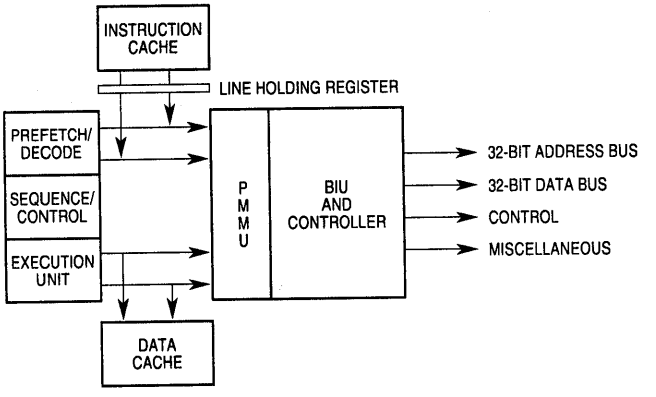
MC68882—Floating-Point Coprocessors

MC68307—Slave Mode.

Package/Speed Options:

Device	Package	Speed	Rev	Order Quantity
MC68EC020	100-lead FG	16, 25		MPQ = 66
	100-lead RP	16, 25		MPQ = 1
SPAKEC020	100-lead FG	16, 25		SOQ = 2

NOTE: FG = Plastic QFP EIAJ Standard
RP = Plastic Pin Grid Array
MPQ = Minimum Package Quantity



Features:

- 32-Bit Address Bus, 32-Bit Data Bus
- 256-Byte On-Chip Instruction Cache
- 256-Byte On-Chip Data Cache
- 17.9 MIPS at 50 MHz
- Burst Memory Interface
- Internal Harvard Architecture
- Dynamic Bus Sizing
- On-Chip Memory Management

Target Markets/Applications:

The 68030 is well suited for all applications requiring moderate performance and low cost (via dynamic bus sizing, burst memory interface, etc.). Memory management support provides protection for users and tasks allowing controlled execution of programs. Target markets are high-speed LAN controllers (Ethernet, FDDI, X.25, etc.), I/O processors, laser printers, X-terminals, mid-range PCs, low-end workstations, servers, etc.

Principle markets include low-end to mid-range personal computers as well as embedded applications that require the protection features of a memory management unit.

Competitive Advantages:

Intel 386: Comparable 030 performance

Weaknesses: Has awkward register set and memory management

Intel 960KA: Comparable 68030 performance at approximately the same price range

Weaknesses: Multiplexed address and data buses. No data cache. Performance very susceptible to wait states. Interrupt latency poor—**Intel quote *typically* 1 ms at 33 MHz.**

Literature:

Title	Order Number
MC68030 Technical Summary	MC68030/D
MC68030 User's Manual	MC68030UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD
68000 Family Fact Brochure	BR1115/D

Support Tools:

M68EC030IDP—Integrated Development Platform: hardware/software evaluation module

Third party support listed in *The 68K Source* 1993 Edition BR729/D.

Support Chips:

MC68882—Floating-Point Coprocessor

MC88915/MC88916—Clock Driver

Crystals—Champion, Kyocera, ACT

FSRAMS—MCM6206C, MCM6226A

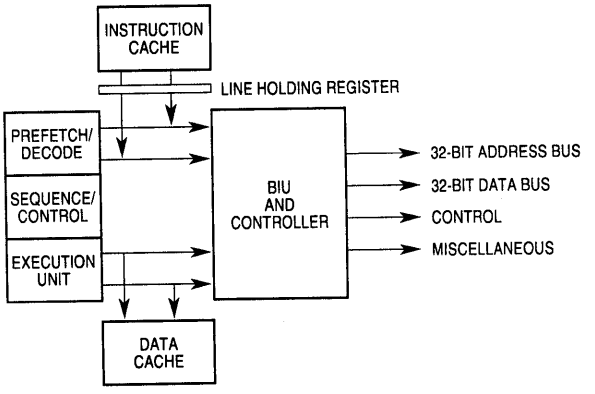
MC68307—Slave Mode

Package/Speed Options:

Device	Package	Speed	Rev	Order Quantity
MC68030	128-lead RC	16, 20, 25, 33, 40, 50	B	MPQ = 1
	124-lead RP	16, 20, 25, 33	B	MPQ = 1
	132-lead FE	16, 20, 25, 33	B	MPQ = 36
SPAK030	132-lead FE	16, 20, 25, 33	B	SOQ = 2

NOTE: RC = Pin Grid Array, Gold Lead Finish
RP = Plastic Pin Grid Array
FE = Ceramic Quad Flat Pack (CQFP)
MPQ = Minimum Package Quantity
SOQ = Sample Order Quantity

MC68EC030



Features:

- 32-Bit Address Bus, 32-Bit Data Bus
- 256-Byte On-Chip Instruction Cache
- 256-Byte On-Chip Data Cache
- 14.3 MIPS at 40 MHz
- Burst Memory Interface
- Internal Harvard Architecture
- Bus Sizing

Target Markets/Applications:

The 68EC030 is well suited for all mid-range embedded control applications that require moderate performance, low cost and the option of surface-mount packaging. Target markets are high-speed LAN controllers (Ethernet, FDDI, X.25, etc.), I/O processors, laser printers, X-terminals, etc.

Competitive Advantages:

Intel 960KA: Around 68EC030 performance at roughly same price

Weaknesses: Multiplexed address and data buses. No data cache. Performance very susceptible to wait states. Interrupt latency poor—Intel quote *typically* 1 ms at 33 MHz.

AMD29000: Performance lies between 68EC030 and 68EC040 levels

Weaknesses: Lower performance with DRAMs in burst-mode and much more susceptible to wait states. Large register sets— not well suited to multitasking.

Literature:

Title	Order Number
MC68EC030 Technical Summary	MC68EC030/D
MC68EC030 User's Manual	MC68EC030UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD
68000 Family Brochure	BR1115/D

Support Tools:

M68EC030IDP—Integrated Development Platform: hardware/software evaluation module

Third party support listed in *The 68K Source* 1993 Edition BR729/D.

Support Chips:

MC68882—Floating-Point Coprocessor

MC68307—Slave Mode

MC88915/MC88916—Clock Driver

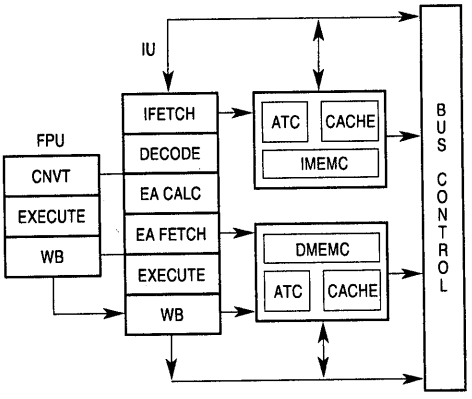
FSRAMS—MCM6206C, MCM6226A

Crystals—Champion, Kyocera, ACT

Package/Speed Options:

Device	Package	Speed	Rev	Order Quantity
MC68EC030	124-lead RP	25, 40	B	MPQ = 1
	132-lead FE	25, 40	B	MPQ = 36
SPAKEC030	132-lead FE	25, 40	B	SOQ = 2

NOTE: R = Plastic Pin Grid Array
FE = Ceramic Quad Flat Pack (CQFP)
MPQ = Minimum Package Quantity
SOQ = Sample Order Quantity



Features:

- 32-Bit Address Bus, 32-Bit Data Bus
- 4-Kbyte On-Chip Instruction Cache
- 4-Kbyte On-Chip Data Cache
- On-Chip Floating-Point Support
- 43.8 MIPS at 40 MHz
- 5.3 MFLOPS at 40 MHz
- Burst Memory Interface
- On-Chip Memory Management

Target Markets/Applications:

The 68040 is well suited for all applications that require high-integer and floating-point performance while still retaining compatibility with the 68K architecture. Target markets include servers, X-terminals, graphics low-end workstations, high-performance PCs, etc.

Competitive Advantages:

Intel 486: Dominates PC-DOS market

Weaknesses: 25–MHz 68040 outperforms 50–MHz 486 in both Ingram Labs and *PC Week* benchmarks. Numerous clones confuse functional and performance issues.

IDT 3051/52: Aggressive pricing, high performance, surface mount

Weaknesses: Multiplexed bus requires external components. RISC machine intolerant of wait states. Limited range of development tools compared to 68K.

AMD29030/35: Aggressive pricing, 4K/8K instruction cache

Weaknesses: No data cache. Very high bus usage. No support for multiprocessor system.

Literature:

Title	Order Number
MC68040 Technical Summary	MC68040/D
M68040 User's Manual	M68040UM/AD Rev 1
M68000 Programmer's Reference Manual	M68000PM/AD
68000 Family Fact Brochure	BR1115/D

Support Tools:

M68EC040IDP—Integrated Development Platform: hardware/software evaluation module

Third party support listed in *The 68K Source* 1993 Edition BR729/D.

Support Chips:

MC68150—Dynamic Bus Sizer

MC68307—Slave Mode

MC88915/MC88916—Clock Driver

Crystals—Champion, Kyocera, ACT

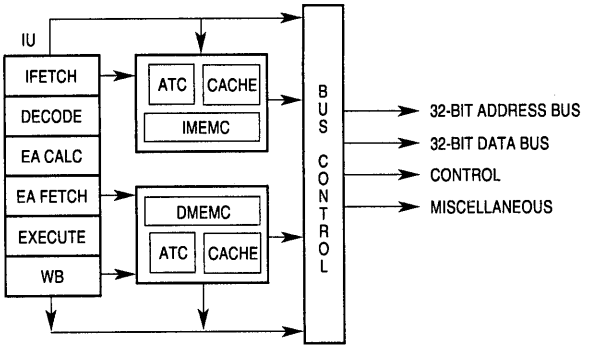
FSRAMS—MCM62940 Burst Mode SRAM

Package/Speed Options:

Device	Package	Speed	Rev	Order Quantity
XC68040	179-lead RC	25, 33,40	M	MPQ = 1

NOTE: RC = Pin Grid Array, Gold Lead Finish
MPQ = Minimum Package Quantity

MC68040V



Features:

- Low Voltage (3.3v), Low Power (1.5 watts @ 33 MHZ)
- Low Power Mode for Full Power-Down Capatbility (660uW)
- Full Static Design
- Dual Input/Output Voltag Compatibility (3.3Volt & 5Volt TTL)
- Identical Code to the MC68040 plus LPSTOP Command for Power Down
- Non-Mulitplexed 32-Bit Address Bus, 32-Bit Data Bus
- 4K-Byte On-Chip Instruction Cache
- 4K-Byte On-Chip Data Cache
- 26.1 MIPS Integer Performance at 25 MHz
- Burst Memory Interface
- On-Chip Memory Management Unit

Target Markets/Applications:

The principle target for the MC68040V is for all high-performance, power-sensitive, general computing and embedded processing applications.

Competitive Advantages:

Intel 960CA/F: Marketed as a RISC high-end solution

Weakness: High Power Consumption and Less Performance. RISC machine intolerant of wait states, requires Expensive high speed SRAM. Poor IDT 3051/52, 3081/3082: Aggressive pricing, high performance, surface mount

Weaknesses: Multiplexed bus requires external components. RISC machine intolerant of wait states, requires Expensive high speed SRAM. High Power Consumption

AMD29030/35: Aggressive pricing, 4K/8K instruction cache

Weaknesses: No data cache. Very high bus usage. No support for multiprocessor system. RISC machine intolerant of wait states, requires Expensive high speed SRAM. High Power Consumption.

Literature:

Title	Order Number
MC68040 VTProduct Brief	MC68040V/D
M68040 User's Manual	M68040UM/AD Rev 1.
M68000 Programmer's Reference Manual	M68000PM/AD
The 68K Source	BR729/D
BR1407/D	3.3 Volt Logic and Interface Circuits

Support Tools:

M68EC040IDP—Integrated Development Platform: hardware/software evaluation module

Support Chips:

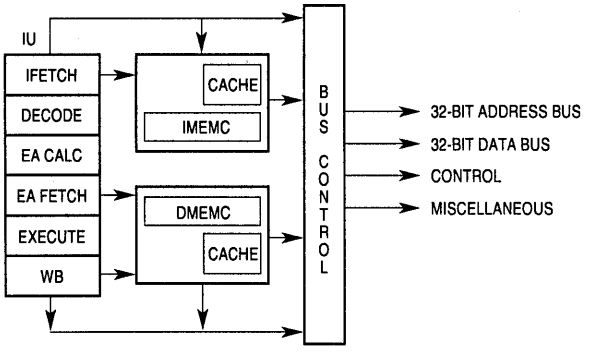
- MC68150—Dynamic Bus Sizer
- MC88915/MC88916/MC8892—Clock Driver
- Crystals—Champion, Kyocera, ACT
- National NM27C6841 Burst EPROM
- FSRAMS—MCM62940A Burst Mode SRAM

Package/Speed Options:

Device	Package	Speed	Rev	Order Quantity
MC68040V	179 lead RC	25, 33	N/A	MPQ = 1
	189 lead FE	25, 33	N/A	MPQ = 21
SPAK040V	189 lead FE	25, 33	N/A	SOQ = 1

NOTE: RC = Pin Grid Array, Gold Lead Finish
FE = Ceramic Quad Flat Pack
MPQ = Minimum Package Quantity

MC68EC040



Features:

- 32-Bit Address Bus, 32-Bit Data Bus
- 4-Kbyte On-Chip Instruction Cache
- 4-Kbyte On-Chip Data Cache
- 27.4 MIPS at 25 MHz
- Burst Memory Interface

Target Markets/Applications:

The 68EC040 is suited for high-end embedded control applications that require high performance and low cost. Target markets include high-speed LAN controllers (Ethernet, FDDI, X.25, etc.), I/O processors, laser printers, X-terminals, routers, bridges, etc.

Competitive Advantages:

Intel 960CA/F: Marketed as a RISC high-end solution

Weaknesses: Lower performance than the EC040

IDT 3051/52: Aggressive pricing, high performance, surface mount

Weaknesses: Multiplexed bus requires external components. RISC machine intolerant of wait states. Limited development tools support compared to 68K.

AMD29030/35: Aggressive pricing, 4K/8K instruction cache

Weaknesses: No data cache. Very high bus usage. No support for multiprocessor system.

Literature:

Title	Order Number
MC68EC040 Technical Summary	MC68EC040/D
M68040 User's Manual	M68040UM/AD Rev 1
M68000 Programmer's Reference Manual	M68000PM/AD
68EC0x0 Family Brochure	BR1109/D

Support Tools:

M68EC040IDP—Integrated Development Platform: hardware/software evaluation module

Third party support listed in *The 68K Source* 1993 Edition BR729/D.

Support Chips:

68150—Dynamic Bus Sizer

MC68307—Slave Mode

MC68360—Integrated Communication Controller

MC68915/MC88916—Clock Driver

Crystals—Champion, Kyocera, ACT

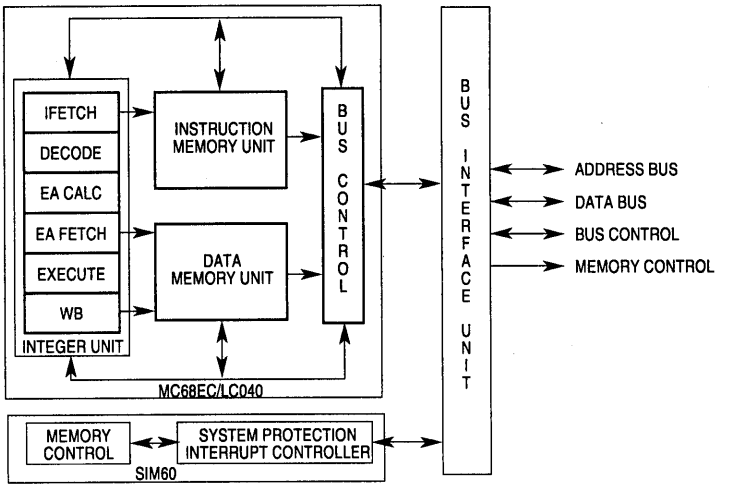
FSRAMS—MCM62940 Burst Mode SRAM

Package/Speed Options:

Device	Package	Speed	Rev	Order Quantity
XC68EC040	179-lead RC	20, 25, 33, 40	B	MPQ = 1
XC68EC040	184-lead FE	20, 25, 33	B	MPQ = 21
SPAKEC040	184-lead FE	20, 25, 33	B	SOQ = 2

NOTE: RC = Pin Grid Array, Gold Lead Finish
MPQ = Minimum Package Quantity

MC68IP040 Integrated Processor



Features:

- Glueless Interface to Memory & Peripherals
- Non-Mulitplexed 32-Bit Address and Data Bus
- 4K-Byte Physical Instruction Cache
- 4K-Byte Physical Data Cache
- 27 MIPS Integer Performance at 25 MHz
- Code Compatible with 68000 Family

Target Markets/Applications:

The IP040 high level of integration results in significant reduction in component count, power consumption, board space, and cost while yielding higher system reliability and shorter design time. The principle market for the MC68IP040 is for all high-performance, space-sensitive, general computing, embedded and controlling applications that require DRAM and Peripheral support.

Competitive Advantages:

Intel 960CA/F: Marketed as a RISC high-end solution

Weakness: High Power Consumption and Less Performance. RISC machine intolerant of wait states, requires Expensive high speed SRAM. Poor Support Tool s.

IDT 3051/52, 3081/3082: Aggressive pricing, high performance, surface mount

Weaknesses: Multiplexed bus requires external components. RISC machine intolerant of wait states, requires Expensive high speed SRAM. AMD29030/35: Aggressive pricing, 4K/8K instruction cache

Weakness: High Power Consumption and Less Performance. RISC machine intolerant of wait states, requires Expensive high speed SRAM. Poor Support Tool s.

IDT 3051/52, 3081/3082: Aggressive pricing, high performance, surface mount

Weaknesses: Multiplexed bus requires external components. RISC machine intolerant of wait states, requires Expensive high speed SRAM. AMD29030/35: Aggressive pricing, 4K/8K instruction cache

Weaknesses: No data cache. Very high bus usage. No support for multiprocessor system. RISC machine intolerant of wait states, requires Expensive high speed SRAM. High Power Consumption.

Literature:

Title	Order Number
MC68IP40 Product Brief	IP040/D

Support Tools:

M68EC040IDP—Integrated Development Platform: hardware/software evaluation module

Support Chips:

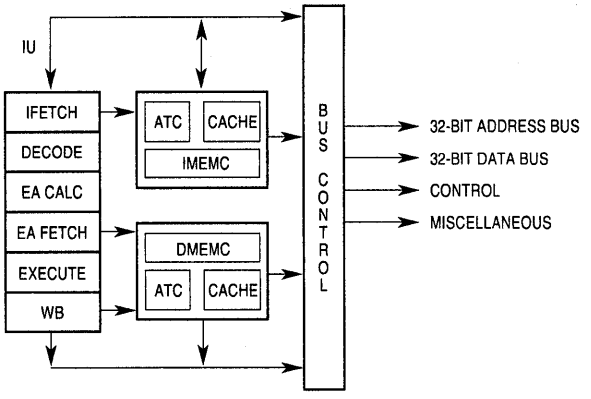
- MC68150—Dynamic Bus Sizer
- MC88915/MC88916/MC88920—Clock Driver
- Crystals—Champion, Kyocera, ACT
- National NM27C6841Burst EPROM
- FSRAMS—MCM62940 Burst Mode SRAM

Package/Speed Options:

Device	Package	Speed	Rev	Order Quantity
SPAKIP040	184-lead FE	25	N/A	SOQ = 1

NOTE: FE = Ceramic Quad Flat Pack
SOQ = Sample Quantity
Samples available second half of 1994

MC68LC040



Features:

- 32-Bit Address Bus, 32-Bit Data Bus
- 4K-Byte On-Chip Instruction Cache
- 4K-Byte On-Chip Data Cache
- 27.4 MIPS at 25 MHz
- Burst Memory Interface
- On-Chip Memory Management

Target Markets/Applications:

The principle target for the MC68LC040 is low-end PCs that do not require the floating-point features of the 68040. The 68LC040 is well suited for all high-end embedded control applications that require high performance, low cost and memory management.

Competitive Advantages:

Intel 486SX: Lowest cost 486 entry point

Weaknesses: No acceptance outside of DOS compatible marketplace.

IDT 3051/52: Aggressive pricing, high performance, surface mount

Weaknesses: Multiplexed bus requires external components. RISC machine intolerant of wait states. Limited development tool support compared to 68K.

AMD29030/35: Aggressive pricing, 4K/8K instruction cache

Weaknesses: No data cache. Very high bus usage. No support for multiprocessor system.

Literature:

Title	Order Number
MC68LC040 Technical Summary	MC68LC040/D
M68040 User's Manual	M68040UM/AD Rev 1
M68000 Programmer's Reference Manual	M68000PM/AD
68000 Family Brochure	BR1115/D

Support Tools:

M68EC040IDP—Integrated Development Platform: hardware/software evaluation module

Third party support listed in *The 68K Source* 1993 Edition BR729/D.

Support Chips:

68150—Dynamic Bus Sizer

MC68307—Slave Mode

MC68360—Integrated Communication Controller

MC88915MC88916—Clock Driver

Crystals—Champion, Kyocera, ACT

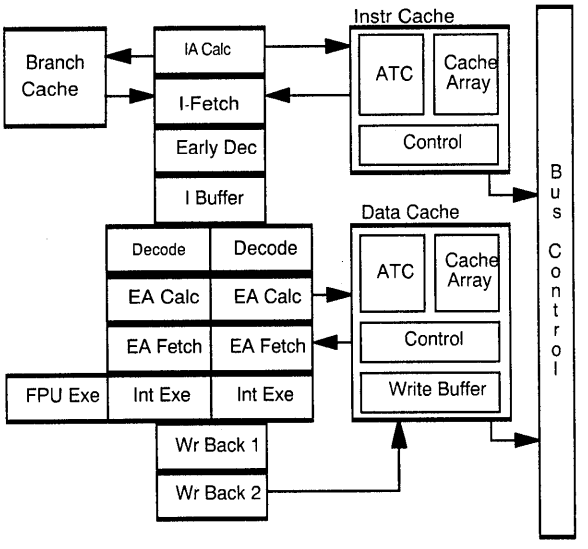
FSRAMS—MCM62940 Burst Mode SRAM

Package/Speed Options:

Device	Package	Speed	Rev	Order Quantity
XC68LC040	179-lead RC	20, 25, 33	B	MPQ = 1
	184-lead FE	20, 25, 33	B	MPQ = 21
SPAKLC040	184-lead FE	20, 25, 33	B	SOQ = 2

NOTE: RC = Pin Grid Array, Gold Lead Finish
MPQ = Minimum Package Quantity

MC68060 (Samples available 1H94)



Features:

- Greater than 50 Integer SPECmarks at 50MHz
- Dual issue execution pipeline
- 32-Bit Address Bus, 32-Bit Data Bus
- 8-Kbyte On-Chip Instruction Cache
- 8-Kbyte On-Chip Data Cache
- 256 Entry Branch Cache
- On-Chip Floating-Point Support
- On-Chip Memory Management
- Burst Memory Interface
- Designed for low power
- 3.3 Volt Operation

Target Markets/Applications:

The 68060 is well suited for all applications that require very high integer and floating-point performance while still retaining compatibility with the 68K architecture.

Competitive Advantages:

Intel Pentium: Dominates PC-DOS market

Weaknesses: Requires 64 bit bus. Very high power dissipation.

68060: Superior integer performance with low cost memory system.

Literature:

Title	Order Number
MC68060 Product Brief	MC68060/D
M68060 User's Manual	1Q94
MC68060 Design Specification	Available from Marketing under NDA

Support Tools:

M68060IDP—Integrated Development Platform: hardware/software evaluation module planned for 1Q94.

Support Chips:

MC68150—Dynamic Bus Sizer

MC88926—Clock Driver

Crystals—Champion, Kyocera, ACT

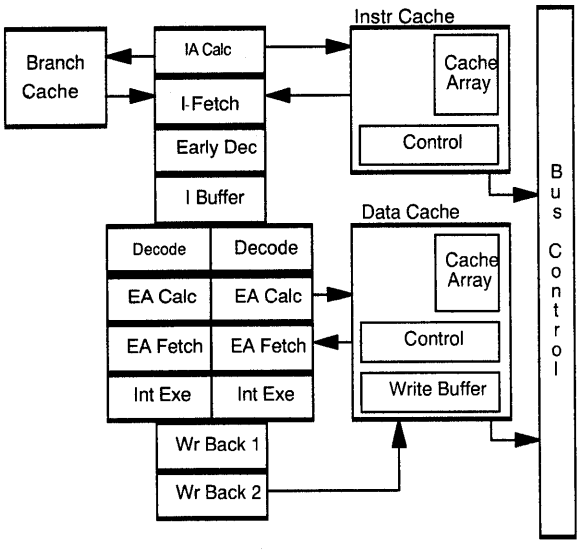
FSRAMS—MCM62940 Burst Mode SRAM

Package/Speed Options:

Device	Package	Speed	Rev	Order Quantity
PC68060	223-lead RC	50, 66	-	1
PC68060	208-lead FE	50, 66	-	2

NOTE: RC = Pin Grid Array, Gold Lead Finish
FE = Ceramic Quad Flat Pack

MC68EC060 (Samples available 1H94)



Features:

- Greater than 50 Integer SPECmarks at 50MHz
- Dual issue execution pipeline
- 32-Bit Address Bus, 32-Bit Data Bus
- 8-Kbyte On-Chip Instruction Cache
- 8-Kbyte On-Chip Data Cache
- 256 Entry Branch Cache
- Burst Memory Interface
- Designed for low power
- 3.3 Volt Operation

Target Markets/Applications:

The 68EC060 is suited for high-end embedded control applications that require high performance low cost. Target markets include high-speed LAN controllers (Ethernet, FDDI, X.25, etc.), I/O processors, laser printers, X-terminals, routers, bridges, etc.

Competitive Advantages:

Intel Pentium: Dominates PC-DOS market

Weaknesses: Requires 64 bit bus. Very high power dissipation.

68060: Superior integer performance with low cost memory system.

Literature:

Title	Order Number
MC68060 Product Brief	MC68060/D
M68060 User's Manual	1Q94
MC68060 Design Specification	Available from Marketing under NDA

Support Tools:

M68060IDP—Integrated Development Platform: hardware/software evaluation module planned for 1Q94.

Support Chips:

MC68150—Dynamic Bus Sizer

MC88926—Clock Driver

Crystals—Champion, Kyocera, ACT

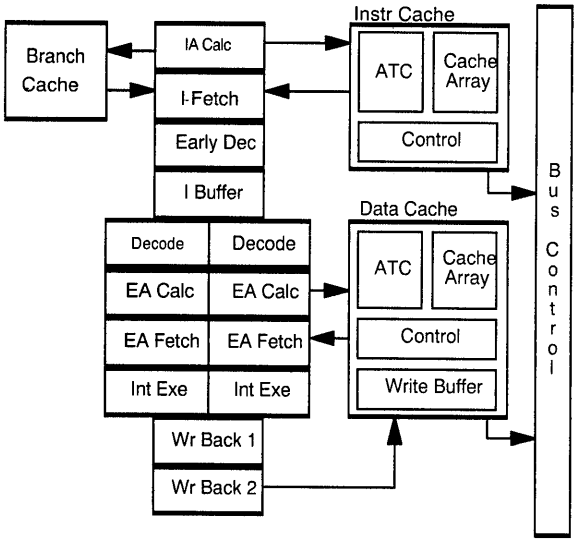
FSRAMS—MCM62940 Burst Mode SRAM

Package/Speed Options:

Device	Package	Speed	Rev	Order Quantity
PC68EC060	223-lead RC	40, 50, 66	-	1
PC68EC060	208-lead FE	40, 50, 66	-	2

NOTE: RC = Pin Grid Array, Gold Lead Finish
FE = Ceramic Quad Flat Pack

MC68LC060 (Samples available 1H94)



Features:

- Greater than 50 Integer SPECmarks at 50MHz
- Dual issue execution pipeline
- 32-Bit Address Bus, 32-Bit Data Bus
- 8-Kbyte On-Chip Instruction Cache
- 8-Kbyte On-Chip Data Cache
- 256 Entry Branch Cache
- Burst Memory Interface
- On-Chip Memory Management
- Designed for low power
- 3.3 Volt Operation

Target Markets/Applications:

The 68LC060 is well suited for all high-end embedded control applications that require high performance, low cost, and the function of memory management.

Competitive Advantages:

Intel Pentium: Dominates PC-DOS market

Weaknesses: Requires 64 bit bus. Very high power dissipation.

68060: Superior integer performance with low cost memory system.

Literature:

Title	Order Number
MC68060 Product Brief	MC68060/D
M68060 User's Manual	1Q94
MC68060 Design Specification	Available from Marketing under NDA

Support Tools:

M68060IDP—Integrated Development Platform: hardware/software evaluation module planned for 1Q94.

Support Chips:

MC68150—Dynamic Bus Sizer

MC88926—Clock Driver

Crystals—Champion, Kyocera, ACT

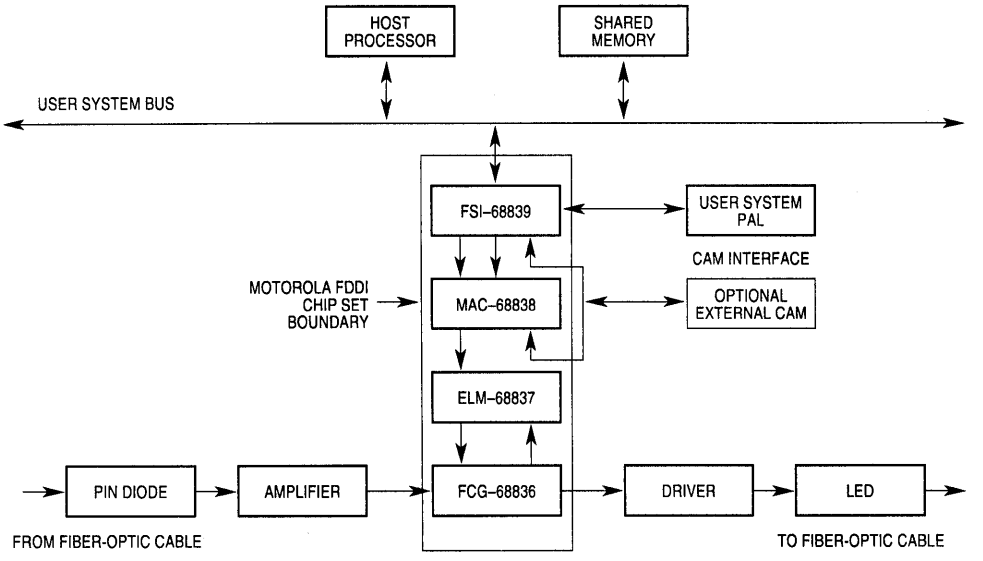
FSRAMS—MCM62940 Burst Mode SRAM

Package/Speed Options:

Device	Package	Speed	Rev	Order Quantity
PC68LC060	223-lead RC	50, 66	-	1
PC68LC060	208-lead FE	50, 66	-	2

NOTE: RC = Pin Grid Array, Gold Lead Finish
FE = Ceramic Quad Flat Pack

First-Generation FDDI Chip Set



Features:

- MC68836 FDDI Clock Generator (FCG)
- MC68837 Elasticity Buffer and Link Manager (ELM)
- MC68838 Media Access Controller (MAC)
- MC68839 FDDI System Interface (FSI)

Target Markets/Applications:

The fiber distributed data interface (FDDI) chip set fully implements the 100 Mbits/sec networking standard set up by the American National Standards Institute (ANSI). The chip set offers a high-performance, flexible, low-cost solution for applications such as FDDI adapter cards, bridges, and concentrators where large data-transfer rates are required.

Competitive Advantages:

AMD: Inferior performance, awkward to use, and shedding resources due to 386/486 opportunities.

National Semiconductor: Inferior performance and requires many external components.

Literature:

Title	Order Number
FDDI Chip Set Technical Summary	M68800/D
FDDI Chip Set Brochure	BR1104/D
FCG User's Manual	MC68836UM/AD
ELM User's Manual	MC68837UM/AD
MAC User's Manual	MC68838UM/AD
FSI User's Manual (Planned)	MC68839UM/AD (Call Factory)

Support Tools:

M68FDDISMT—Station Management Software (SMT) available in DOS and TAR format

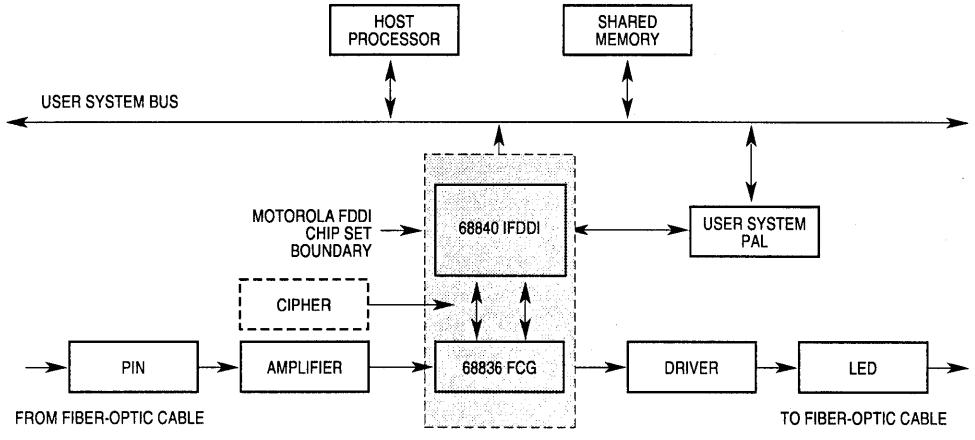
Third party support listed in *The 68K Source* 1993 Edition BR729/D.

Package/Speed Options:

Device	Package	Rev	Order Quantity
XC68836	52-lead FN		MPQ = 1
MC68837	120-lead KB	B	MPQ = 1
MC68837	120-lead FC	B	MPQ = 24
SPAK837	120-lead FC	B	SOQ = 2
MC68838	120-lead KB	C	MPQ = 1
MC68838	120-lead FC	C	MPQ = 24
SPAK838	120-lead FC	C	SOQ = 2
XC68839	184-lead RC	C	MPQ = 1
XC68839	184-lead FE	C	MPQ = 12
SPAK839	184-lead FE	C	SOQ = 2

NOTE:
FN = Plastic Leaded Chip Carrier (PLCC)
RC = Pin Grid Array, Gold Lead Finish, Metal Lid
FC = Plastic Quad Flat Pack
FE = Ceramic Quad Flat Pack
KB = Ceramic PGA, Ceramic Lid
MPQ = Minimum Package Quantity
SOQ = Sample Order Quantity

Next-Generation FDDI Chip Set



Features:

- MC68836 FDDI Clock Generator (FCG)
- MC68840 Integrated Fiber Distributed Data Interface (IFDDI)
- MC68834 Stream Cipher ChipMedia Access Controller (MAC)

Target Markets/Applications:

Motorola's next generation FDDI chip set fully implements the 100 Mbits/sec networking standard set up by the American National Standards Institute (ANSI). The chip set offers a highly integrated, high-performance, flexible, low-cost solution for applications such as adapter cards, motherboards, bridges, and concentrators where large data transfer rates are required. Twisted pair wire can also be supported with the addition of the 68834 stream cipher chip. The 68834 implements the scrambling algorithm adopted by ANSI.

Competitive Advantages:

AMD: Inferior performance, awkward to use, and shedding resources due to 386/486 opportunities. No integration of first-generation components.

National Semiconductor: Inferior performance and requires many external components, and less flexible.

Literature:

Title	Order Number
FCG User's Manual	MC68836UM/AD
IFDDI User's Manual	MC68840UM/AD
Cipher Chip User's Manual (Planned)	MC68834UM/AD

Support Tools:

M68FDDISMT—Station Management Software (SMT) available in DOS and TAR format

Third party support listed in *The 68K Source* 1993 Edition BR729/D.

Package/Speed Options:

Device	Package	Rev	Order Quantity
XC68836	52-lead FN		MPQ = 1
XC68840	184-lead RC, FE		MPQ = 1, 12
SPAK840	184-lead FE		SOQ = 2
XC68834	44-lead PB		MPQ = 96
SPAK834	44-lead PB		SOQ = 2

NOTE:
FN = Plastic Leaded Chip Carrier (PLCC)
RC = Pin Grid Array, Gold Lead Finish, Metal Lid
FC = Plastic Quad Flat Pack
FE = Ceramic Quad Flat Pack
KB = Ceramic PGA, Ceramic Lid
MPQ = Minimum Package Quantity
SOQ = Sample Order Quantity
PB = 10mm x 10mm Plastic Quad Flat Pack

M68300 FAMILY STRATEGY

The M68300 Family consist of highly integrated processors aimed at the embedded computing and control market. The core processor is either the 68000 (MC68302, MC68306, MC68307) the CPU32 (MC68330, MC68340, MC68341), or the CPU32+ (MC68349, MC68360), which is a derivative of the MC68020.

The M68300 family is the dominant 32-bit architecture in the area of integrated processors. This is achieved via the ongoing matching of Motorola capabilities to customer needs with particular focus in the following markets:

CONSUMER—CD-I, information terminals, global positioning (navigation aids) and personal computing.

COMMUNICATIONS—Network control and portable applications such as phones.

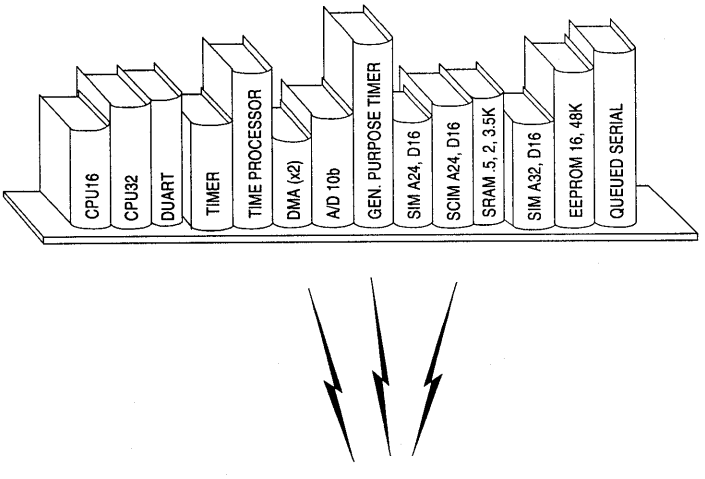
OFFICE EQUIPMENT—Copiers, network interfaces, portable computers and personal information computers.

AUTOMOTIVE—Engine and transmission management and navigation systems.

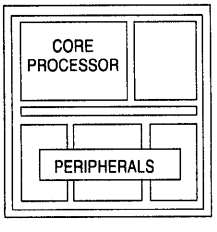
PORTABLE INSTRUMENTS—Measuring, monitoring, medical, inventory control and computers.

Much of the M68300 Family is based around the intermodule bus (IMB), which allows the device to be assembled from a library of peripheral modules as shown in the following illustration.

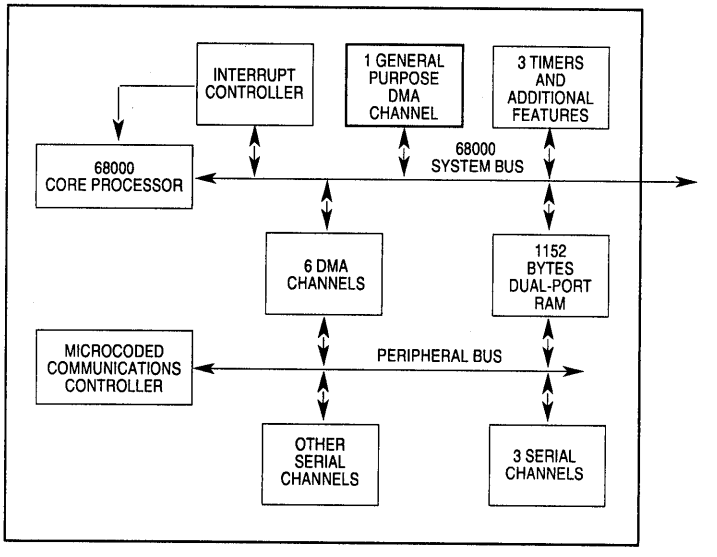
PERIPHERAL LIBRARY



68300



MC68302



Features:

- 68000 Core CPU (16 or 20 MHz)
- Independent DMA Controller
- 1152 Bytes of Dual-Port Static RAM
- 4 Chip Selects (CS)
- System Integration: 3 Timers Including a Watchdog, Independent DMA Controller, 1152 Bytes of Dual-Port Static RAM, 4 Chip Selects (CS), Interrupt Controller, Parallel Input/Output (I/O) Ports, On-Chip Clock Generator with Output Signal
- Communications Processor: RISC-Based Communications Controller, 3 Serial Communications Channels each supporting HDLC/SDLC, UART, BISYNC, DDCMP, and Transparent Modes, 6 Serial DMAs for the 3 SCC's, SCP for Synchronous Communications, Flexible Physical Interface Including IDL, NMSI, GCI, and PCM, Two Serial Management Controllers to Support IDL & GCI Auxiliary Channels.

Target Markets/Applications:

- Modems
- Computer I/O Subsystems
- Routers and Bridges
- Switching Networks
- ISDN
- Industrial Control

Literature:

Title	Order Number
MC68302 User's Manual (Rev 2)	MC68302UM/AD
MC68302 Technical Summary (Rev 2)	MC68302/D
MC68302 Development Tools Technical Summary	BR469/D

Support Tools:

M68302ADS—Application Development System

M68302ADI—Host Interface Card

M68302ICERC—PGA Target Cable

Third party support listed in *The 68K Source* 1993 Edition BR729/D.

Support Chips:

MC68195 LocalTalk Adapter for the MC68302—The MC68195 interfaces the MC68302 to AppleTalk. Order as MC68195FN.

Package/Speed Options:

Commercial Temperatures (0–70°C)

Device	Package	Speed	Temp Range (°C)	Order Quantity
MC68302RC	132-lead PGA	16, 20 MHz	0 to 70	MPQ = 1
MC68302FC	132-lead PQFP	16, 20 MHz	0 to 70	MPQ = 36
MC68302FE	132-lead CQFP	16, 20 MHz	0 to 70	MPQ = 36
SPAK302FE	132-lead CQFP	16, 20 MHz	0 to 70	SOQ = 2
SPAK302FC	132-lead PQFP	16, 20 MHz	0 to 70	SOQ = 2
MC68302PV	144-lead TQFP	16 MHz	0 to 70	MPQ = 60
SPAK302PV	144-lead TQFP	16 MHz	0 to 70	SOQ = 2

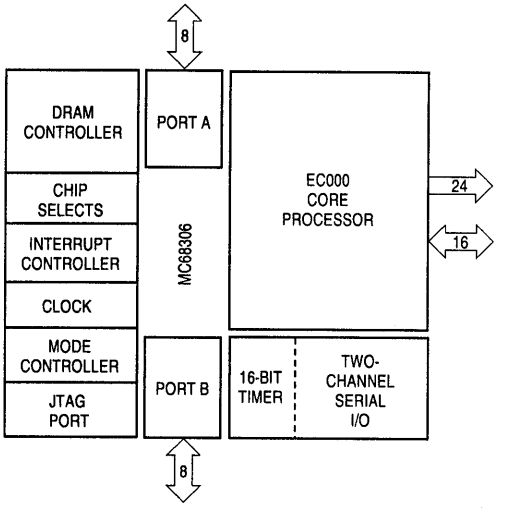
Industrial Temperatures (-40–85°C)

Device	Package	Speed	Temp Range (°C)	Order Quantity
MC68302CRC	132-lead PGA	16 MHz	–40 to 85	MPQ = 140
MC68302CFC*	132-lead PQFP	16 MHz	–40 to 85	MPQ = 144
MC68302CFE	132-lead CQFP	16, 20 MHz	–40 to 85	MPQ = 144

NOTE: RC = Pin Grid Array, Gold Lead Finish, Metal Lid
FC = Plastic Quad Flat Pack
FE = Ceramic Quad Flat Pack
CFC = Plastic Quad Flat Pack (evaluating)
PV = Thin Quad Flat Pack (evaluating 144-pin)
MPQ = Minimum Package Quantity
SOQ = Sample Order Quantity

*Available 1st Quarter 1994

MC68306



Features:

- EC000 Core CPU
- 68681 Two-Channel Serial
- DRAM Controller
- 16 Parallel I/O
- 2.5 MIPS Performance at 16 MHz

Target Markets/Applications:

The 68306 is currently the only integrated device with a DRAM controller priced at less than $10. As such, it holds broad appeal to designers of 68000-based systems. The integrated features, particularly the DRAM controller, simplify system design and speed time-to-market.

Competitive Advantages:

Intel 80186: Slightly lower price, similar processor performance

Weaknesses: Mulitplexed address and data buses. No DRAM controller. Segmented architecture.

Toshiba 68301, 68303: Similar price, similar processor performance

Weaknesses: No DRAM controller

Literature:

Title	Order Number
MC68306 Product Brief	MC68306/D
MC68306 User's Manual	MC68306UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD
68300 Family Brochure (Rev 1)	BR1114/D

Support Tools:

Third party support listed in *The 68K Source* 1993 Edition BR729/D.

Support Chips:

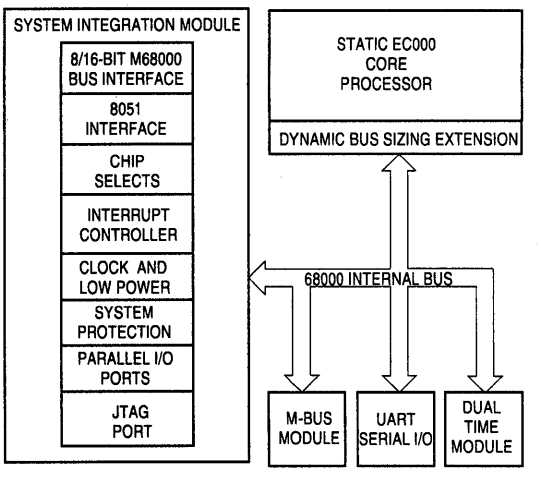
None needed

Package/Speed Options:

Device	Package	Speed	Order Quantity
XC68306	132-lead FC	16	MPQ = 36
SPAK306	132-lead FC	16	SOQ = 2

NOTE: FC = Plastic Quad Flat Pack
MPQ = Minimum Purchase Quantity
SOQ = Sample Order Quantity

MC68307/MC68307V



Features:

- Static EC000 Core CPU
- 8051 Interface
- M-Bus (I2C) Interface
- 68681 Type UART
- 8 Chip Selects
- Interrupt Controller
- 24 Programmable I/O
- Watch Dog Timer
- JTAG Testability
- 2.7 MIPS Performance at 16 MHz

Target Markets/Applications:

The 68307 holds a broad appeal to designers of 68000 systems. Some applications include system upgrades, computer I/O subsystems, portable phones, DECT, GSM basestations, and POS terminals.

Competitive Advantages:

Intel 80186: Slightly lower price, similar processor performance

Weaknesses: One less serial channel, no DMA

Toshiba 68301, 68303: Similar price, similar processor performance

Weaknesses: One less serial channel, no DMA

Literature:

Title	Order Number
MC68307 Product Brief	MC68307/D
MC68307 User's Manual	MC68307UM/AD (2Q94)
M68000 Programmer's Reference Manual	M68000PM/AD

Support Tools:

Software support provided through various third-party vendors of 68000 software tools.

Third party support listed in *The 68K Source* 1993 Edition BR729/D.

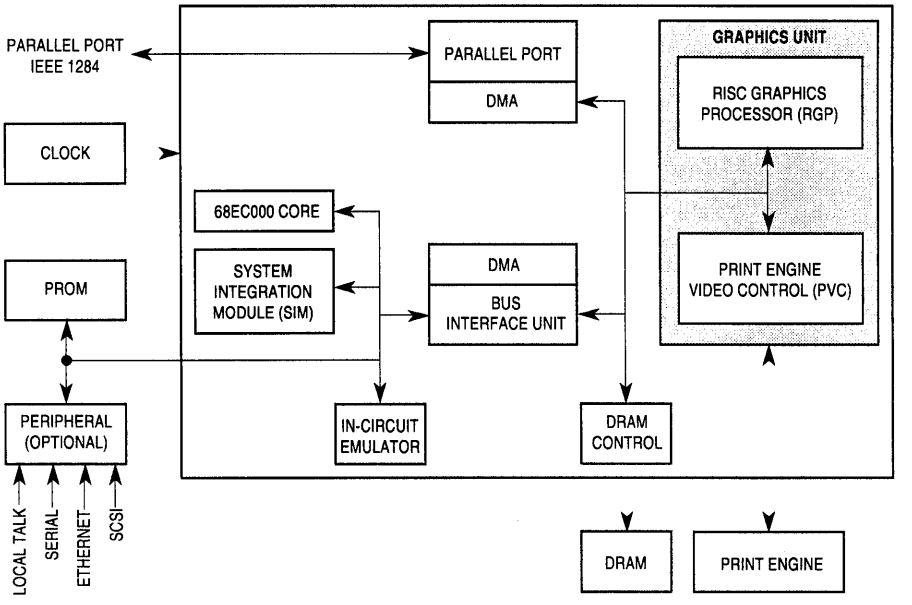
Support Chips:

None needed

Package/Speed Options:

Device	Package	Speed	Order Quantity
PC68307	100-lead FG	8*, 16	MPQ = ?

NOTE: FG = Plastic QFP EIAJ Standard
MPQ = Minimum Purchase Quantity
SOQ = Sample Order Quantity
* Available in 3.3V only.



Features:

- EC000 Core CPU
- Graphic Unit
- DRAM System Integration
- General Purpose DMA Unit
- System Integration Module
- Parallel Communication Port (IEEE 1284)
- Low Power
- Dual Bus
- Static Design
- 16 and 20 MHz

Target Markets/Applications:

The 68322 is suited for the low and mid-range printer market. The 68322 supports laser printers directly and ink jets and fax machines. Other applications may include graphic applications, and applications where the on-board system integration module (chip selects, auto termination, etc.) DMA and DRAM support

Competitive Advantages:

Literature:

Title	Order Number
MC68322Product Brief	MC68322/D
MC68322 User's Manual	MC68322UM/AD (2Q94)
M68000 Programmer's Reference Manual	M68000PM/AD

Support Tools:

Software support provided through various third-party vendors of 68000 software tools.

Third party support listed in *The 68K Source* 1993 Edition BR729/D.

Support Chips:

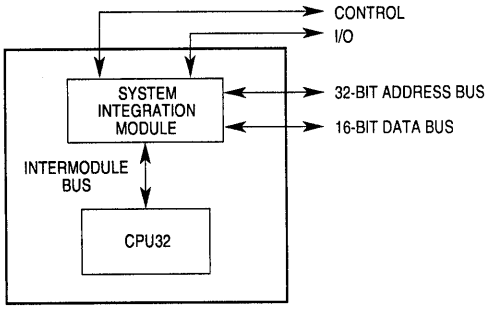
None needed

Package/Speed Options:

Device	Package	Speed	Order Quantity
XC68322	160-lead FT	16, 20 MHz	MPQ = 24

NOTE: FT = Plastic Quad Flat Pack
MPQ = Minimum Purchase Quantity
SOQ = Sample Order Quantity

MC68330/MC68330V



Features:

- CPU32 Processor
- System Integration Module (SIM40)
- 3 V Operation Available (68330V)
- 8.3 MIPS Performance at 25 MHz

Target Markets/Applications:

Applications requiring 68020 performance from a 16-bit memory system; minimal glue logic (SIM40 contains most of it); static design/low power modes—e.g., low power consumption; 5.0 V and 3.3 V parts; and 68000 upgrade solution for applications requiring performance of CPU32 with no on-chip peripherals.

The ability to operate at 3.3 V makes the 68330V an ideal solution for portable applications.

Literature:

Title	Order Number
MC68330 Technical Summary	MC68330/D
MC68330 User's Manual	MC68330UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD

Support Tools:

M68340EVS—Low-Cost Evaluation System

Third party support listed in *The 68K Source* 1993 Edition BR729/D.

Various hardware and software support available from third parties.

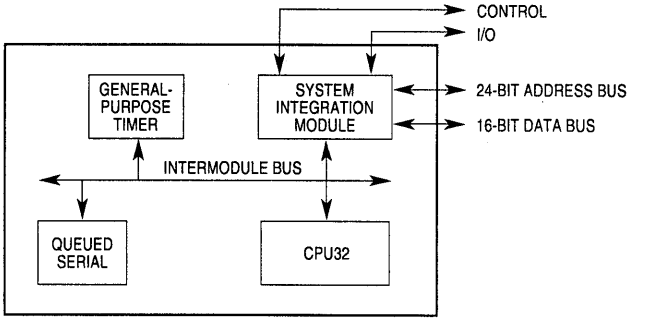
Package/Speed Options:

Device	Package	Speed (MHZ)	Order Quantity
XC68330	132-lead FC	8*, 16*, 25*	MPQ = 36
SPAK330	132-lead FC	16, 25	SOQ = 2

NOTE: FC = Plastic Quad Flat Pack
FG = 128-lead 14 x 20mm Quad Flat Pack
MPQ = Minimum Package Quantity
SOQ = Sample Order Quantity

*Available in 3.3 V

MC68331



Features:

- CPU32 Processor
- System Integration Module (SIM)
- General-Purpose Timer (GPT)
- SCI and Queued SPI (QSM)

Target Markets/Applications:

General purpose embedded control—e.g.:

- Communications—mobile phones
- Office Equipment—mobile equipment
- Industrial Control—peripheral control

Literature:

Title	Order Number
MC68331 User's Manual	MC68331UM/AD
MC68331 Technical Summary	MC68331TS/D
32-bit Central Processing Unit (CPU32) Ref. Manual	CPU32RM/AD
Queued Serial Module (QSM) Reference Manual	QSMRM/AD
General-Purpose Timer (GPT) Reference Manual	GPTRM/AD
System Integration Module (SIM) Reference Manual	SIMRM/AD

Support Tools:

M68331EVS—Low-Cost Evaluation System (contact AMCU marketing for more details)

Third party support listed in *The 68K Source* 1993 Edition BR729/D.

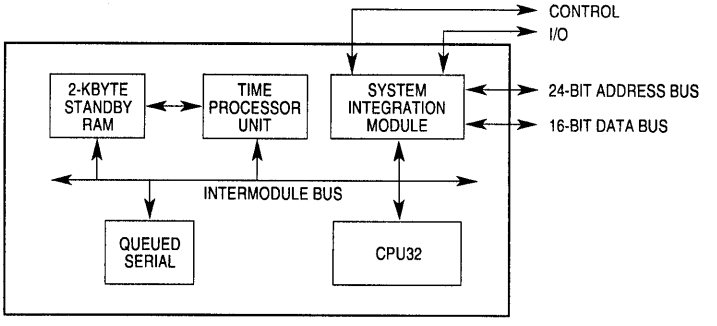
Package/Speed Options:

Device	Package	Speed (MHz)	Order Quantity
MC68331	132-lead CFC, CFD	16	*
	144-lead CFM, CFV	16	*

NOTE: FC = Plastic Quad Flat Pack
FD = Plastic Quad Flat Pack with molded carrier ring
FM = Molded Carrier Ring
FV = 20X20 mm Quad Flat Pack

*Contact AMCU marketing for more details.

MC68332



Features:

- CPU32 Core
- System Integration Module (SIM)
- Programmable Time Processor Unit (TPU)
- SCI and Queued SPI (QSM)
- 2-Kbyte Standby Ram with TPU Emulation (TPU RAM)

Target Markets/Applications:

Any advanced real-time control application—e.g.:

- Powertrain—engine management and gearbox
- Office Equipment—I/O and motor control in plotter, printer, copier, fax, etc.
- Industrial Control—DC and AC motor control

The ability to operate at 3.3 V makes the 68330V an ideal solution for portable applications.

Competitive Advantages:

The MC68332 has the most advanced timer unit on the market today.

Literature:

Title	Order Number
MC68332 User's Manual	MC68332UM/AD
MC68332 Technical Summary	BR756/D
32-bit Central Processing Unit (CPU32) Ref. Manual	CPU32RM/AD
Time Processor Unit (TPU) Reference Manual	TPURM/AD
Queued Serial Module (QSM) Reference Manual	QSMRM/AD
System Integration Module (SIM) Reference Manual	SIMRM/AD

Support Tools:

M68332EVS—Low-Cost Evaluation System

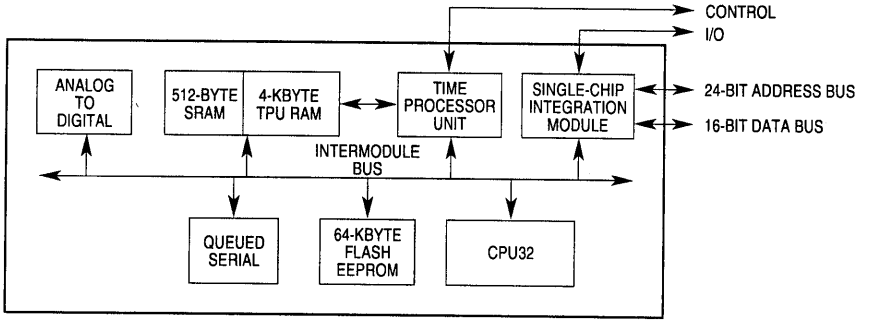
Third party support listed in *The 68K Source* 1993 Edition BR729/D.

Package/Speed Options:

Device	Package	Speed (MHz)	Order Quantity
MC68332	132-lead FC/FD	16	MPQ = 32
	144-lead FM, FV	16	MPQ = 32

NOTE: FC = Plastic Quad Flat Pack in extended temperature (–40 to +85°C)
FD = Plastic Quad Flat Pack with molded carrier ring in extended temperature (–40 to +85°C)
FM = Molded Carrier Ring
FV = 20X20 mm Quad Flat Pack
MPQ = Minimum Package Quantity

MC68F333



Features:

- CPU32 Processor
- Single Chip Integration Module (SCIM)
- 8/10-Bit Analog-to-Digital Converter (ADC)
- Programmable Time Processor Unit (TPU)
- SCI and Queued SPI (QSM)
- 512 Bytes of Standby RAM (SRAM)
- 3.5-Kbyte Standby Ram with TPU Emulation (TPU RAM)
- 64-Kbyte Flash EEPROM

Target Markets/Applications:

- Engine Management (powertrain)
- Motor Control

Competitive Advantages:

First microcontroller to integrate flash EEPROM on-chip.

Literature:

Title	Order Number
MC68F333 Product Preview	MC68F333/D
MC68F333 Technical Summary	MC68F333TS/D
32-bit Central Processing Unit (CPU32) Ref. Manual	CPU32RM/AD
Timer Processor Unit (TPU) Manual	TPURM/AD
Queued Serial Module (QSM) Reference Manual	QSMRM/AD
Analog-to-Digital Converter (ADC) Reference Manual	ADCRM/AD

Support Tools:

Low-cost evaluation board will be available (contact AMCU marketing for more details).

Hardware and software development tools are available from third parties.

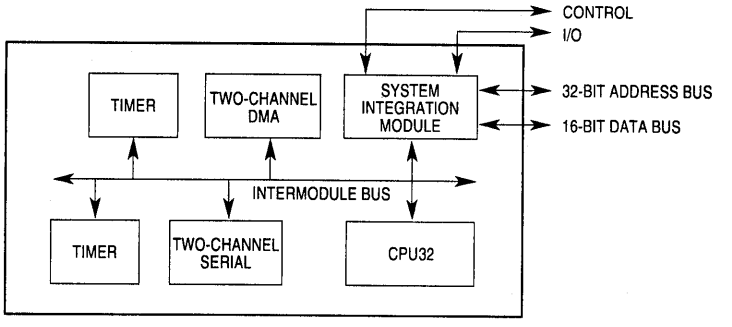
Package/Speed Options:

Device	Package	Speed	Order Quantity
68F333	160-lead FC	16	*

NOTE: FC = Plastic Quad Flat Pack

*Contact AMCU marketing for more details.

MC68340/MC68340V



Features:

- CPU32 Processor
- System Integration Module (SIM40)
- Two-Channel DMA Controller
- Two-Channel Serial UART
- Two Timer Modules
- 3 V Operation Available (68340V)
- 8.3 MIPS Performance at 25 MHz

Target Markets/Applications:

High-Speed Data Movement—terminals, disk controllers, printers, copiers, CD-I, audio-video processing and global positioning systems (navigation aids).

Mobile/Portable Applications—pen-based computers, portable computers, portable phones, and medical instruments.

The ability to operate at 3.3 V makes the 68340V ideal for portable applications.

Literature:

Title	Order Number
MC68340 User's Manual	MC68340UM/AD Rev. 1
MC68340 Product Brief	MC68340/D

Support Tools:

M68340EVS—Low-Cost Evaluation System.

Third party support listed in *The 68K Source* 1993 Edition BR729/D.

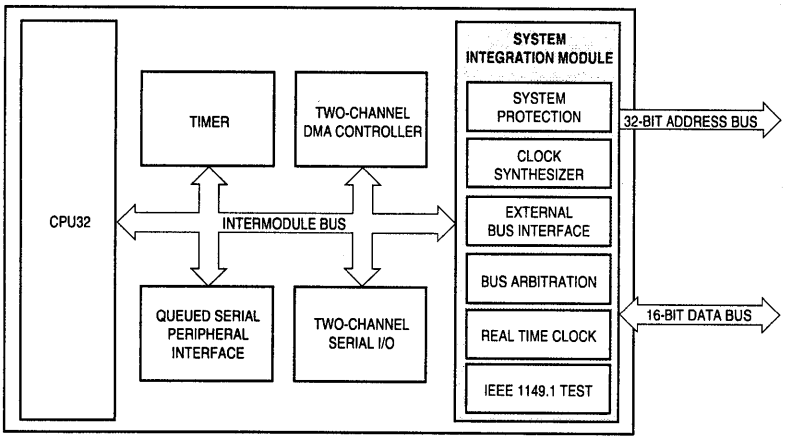
Various hardware and software support available from third parties.

Package/Speed Options:

Device	Package	Speed*	Rev	Order Quantity
MC68340	144-lead FE	8, 16, 25	B	MPQ = 24
MC68340	145-lead RP, PV	8, 16, 25	B	MPQ = 1
SPAK340	144-lead FE	8, 16	B	SOQ = 2

NOTE: FE = Ceramic Quad Flat Pack
RP = Plastic Pin Grid Array
MPQ = Minimum Package Quantity
SOQ = Sample Order Quantity
Low-profile TQFP expected mid '93
Extended-temperature 16-MHz parts available (CFE/CRP); 25 MHz (CFE25B/CRP25B)
"V" Suffix for 3.3 V V_{CC}
"B" Suffix for Rev. K Silicon (not MC)

*Available in 3.3 V V_{CC}.



Features:

- High Performance CPU32 Core Processor
- High-Speed Dual DMA Controllers for Low-Latency Transfers
- Counter/Timer
- Dual Serial Communication Ports
- Queued Serial Peripheral Interface (QSPI)
- System Integration Module for Flexible and Cost-Effective System Interface
- Power Management
- 0–16 or 25 MHz Operation
- 160-Pin Plastic Quad Flat Pack (QFP)

Target Markets/Applications:

High-Speed Data Movement—terminals, disk controllers, printers, copiers, consumer video games, CD-I, audio-video processing, and global positioning systems (navigation aids).

Mobile/Portable Applications—pen-based and hand-held computers, portable computers, portable phones, and medical instruments.

The ability to operate at 3.3 V means that the 68341V is ideally suited for portable applications.

Central Processor for CD-I Players—full Motion video CD-I systems make the best use of the MC68341 high performance.

Literature:

Title	Order Number
M68300 Integrated Processor Family	BR1114/D
MC68341 User's Manual	MC68341UM/AD

Support Tools:

Various hardware and software support available from third parties.

Third party support listed in *The 68K Source* 1993 Edition BR729/D.

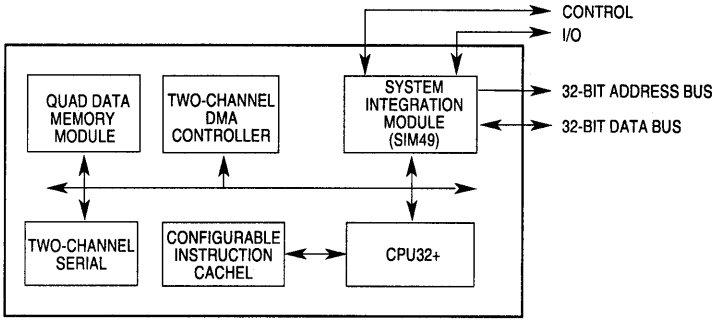
Ordering Information:

Device	Package	Speed*	Rev	Order Quantity
XC68341	160-lead FT	16, 25	0	MPQ = 24
SPAK341	160-lead FT	16, 25	0	SOQ = 2

NOTE: FT = Plastic Quad Flat Pack
MPQ = Minimum Purchase Quantity
SOQ = Sample Order Quantity
"V" = Suffix for 3.3 V V_{CC}

* Available in 3.3V VCC.

MC68349/MC68349V "DRAGON I™ "



Features:

- CPU32+ Processor
- Configurable Instruction Cache
- Quad Data Memory Module
- Two-Channel DMA Controller
- Two-Channel Serial UART
- System Integration Module (SIM49)
- 3.3 V (68349V) or 5 V (68349) Operation

Target Markets/Applications:

- Personal Intelligent Communicators (PICs)
- Personal Digital Assistants (PDAs)
- I/O Processors for High-Performance Systems
- Real-Time Control Engines

The ability to operate at 3.3 V means that the 68349V is ideally suited for portable applications.

Literature:

Title	Order Number
*M68349 User's Manual**	MC68349UM/AD
*MC68349 Product Brief**	MC68349/D

*Available Third Quarter 93.

Support Tools:

Various hardware and software support available from third parties.

Third party support listed in *The 68K Source* 1993 Edition BR729/D.

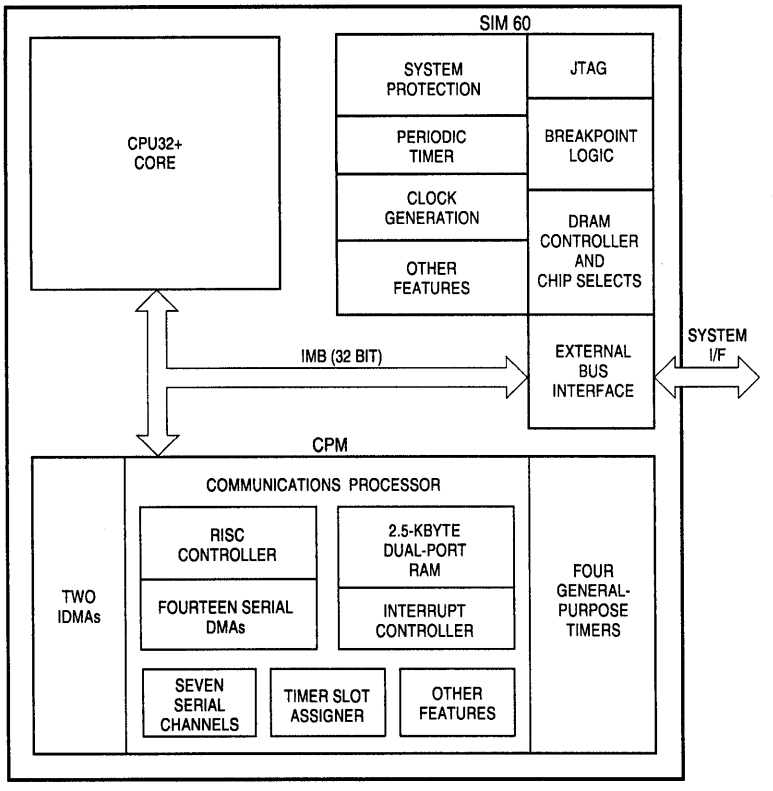
Ordering Information:

Device	Package	Speed*	Order Quantity
XC68349	160-lead FT	8, 16, 25	MPQ = 24
SPAK349	160-lead FT	8, 16, 25	SOQ = 2

NOTE: FT = Plastic Quad Flat Pack
MPQ = Minimum Purchase Quantity
SOQ = Sample Order Quantity
"V" = Suffix for 3.3 V V_{CC}

* Available in 3.3 V VCC.

MC68360 "QUICC"



Features:

- CPU32+ Processor
- Slave Mode To Disable CPU32+ — Glueless Interface to 68040/EC040
- Memory Controller (Eight Banks)
- System Integration Module (SIM60)
- Communications Processor Module (CPM)
- Four SCCs
- Time-Slot Assigner

Target Markets/Applications:

- Bridges
- Routers
- T1 Line Card Controllers
- PABX's
- Cellular Base Stations
- Industrial Control Networking
- 040 Peripheral Chip

Industry's first 32-bit controller to integrate a CPU with WAN and Ethernet LAN capability on a single chip.

Literature:

Title	Order Number
MC68360 Product Brief	MC68360/D
M68360User's Manual	MC68360UM/AD
MC68000 Family Programmer's Reference Manual	MC68000PM/AD
The 68K Source	BR729/D

Support Tools:

M68360QUADS—QUICC Application Development Board

M68360ADI-PC—IBM PC Interface Card

M68360ADI-SUN4—Sun 4 Interface Card

Third party support listed in *The 68K Source* 1993 Edition BR729/D.

Ordering Information:

Device	Package	Speed	Order Quantity
XC68360EM25	240–lead Quad Flat Pack (EM Suffix)	25	MPQ = 24
XC68EN360EM25	240–lead Quad Flat Pack with Ethernet	25	MPQ = 24
XC68360RC25	241–lead Pin Grid Array	25	MPQ = 1
XC68EN360RC25	241–lead Pin Grid Array with Ethernet	25	MPQ = 1
SPAK360	24old EM	25	SOQ = 2
SPAKEN360	24old EM	25	SOQ = 2

NOTE: EM = Quad Flat Pack
RC = Pin Grid Array

COMPETITION

AMD

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
2903X	68EC030/040	• RISC core • SMT capability • 4-Kbyte on-chip instruction cache	• Very poor DRAM performance • No on-chip data cache • Not price aggressive • 29035 only in 16 MHz
29005/050	LC040	• RISC core • 17–32 MIPS at 40 MHz • Floating-point support	• MIPS rating < 040 at same clock frequency • Poor DRAM performance
29200	68340	• Performance (RISC vs. CSIC)	• Not price competitive • Little integration • No low power mode
	EC020	• Integrated device for laser printers	• Only 16 MHz available • 25-MHz EC020 has higher performance-to-cost ratio • Not general purpose
FDDI	FDDI	• Established Ethernet customer base • Provide excellent support and documentation • Sponsors of the European Advanced Networking & Test Center (EANTC)	• Poor integration strategy • Needs more external circuitry • Design team broken up to focus on 386/486
286	EC020	• Intel architecture	• Non-32-bit register set, dedicated registers • Segmented addressing range • Only a 16-bit data bus • Not CMOS
	CPU32	• Intel architecture • Comparable performance with CPU32	• No integration • Higher system cost
386	EC030/030	• 32-bit architecture • Intel architecture • CMOS implementation	• Compatibility/performance issues with '286 • Lower performance architecture • No on-chip caches, no burst mode

Hitachi

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
HC000	HC000	• Very price aggressive	• Not Hitachi proprietary architecture • No second-source support network
H8/500	68331/332	• A/D on-chip • Good timer performance • Small package	• Poorer CPU performance • Lower serial channel performance • Does not have flexibility of TPU

IDT

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
3051/2	EC040	• R3000 core • Price aggressive	• Poor DRAM performance • Multiplexed bus • Inferior development tools
3040	EC030	• Price	• Poor DRAM performance • Multiplexed bus • Inferior development tools

INTEL

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
960SA/B	68340 (25 MHz)	• Faster speeds available	• Lack of integration • Poorer price/performance ratio • No low-voltage parts available
	EC020	• Floating-point support on 'SB • Limited burst mode	• Multiplexed bus • Needs expensive memory for performance • RISC instruction set inefficient on memory usage
960KA/B	EC030	• RISC core (although only microcoded!)	• Poor performance in DRAM • Poor development tools • Not x86 code compatible • Not price aggressive • Multiplexed bus • No data cache
196	EC000		• EC000 is VERY price aggressive • No '196 upgrade path while EC000 is 68K entry point • Poor architecture • 8-bit bus
	68331/332/334	• A/D on-chip • Cost-effective 16-bit MCU	• No integration • Poor performance
186	EC000	• Good software base • Cost aggressive	• Not 32-bit architecture • Nonorthogonal architecture • No good migration path with integration
	68340	• 8 more chip selects • On-board memory refresh • Runs DOS	• Poorer CPU performance (0.5 x CPU32) • Lower addressing range • No JTAG support • Poorer DMA performance • No communications (serial) support
	68302		• No communications support
	68306	• 2 DMA channels	• Lower addressing range • No DRAM controller • No JTAG • No serial support
286	EC020/020	• Intel architecture	• Non-32-bit register set, dedicated registers • Segmented addressing range • Only a 16-bit data bus • Not CMOS

INTEL (continued)

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
286	CPU32	• Intel architecture • Comparable performance with CPU32	• No integration • Higher system cost
386SX	EC030	• 16-bit bus gives smaller package	• Performance limited by 16-bit bus • Compatibility/performance issues with '286 • Lower performance architecture • No on-chip caches, no burst mode
386DX	EC030	• 32-bit architecture • Intel architecture • CMOS implementation	• Compatibility/performance issues with '286 • Lower performance architecture • No on-chip caches, no burst mode
486SX	EC030/EC040 LC040	• Entry point to '486 architecture • SMT option	• Part of confused marketing strategy vs 487SX • Architecture not as powerful as '040 • Unified cache—bottleneck
486DX	68040	• PC base	• Lower performance than '040 at same clock (50-MHz '486 = 33-MHz '040) • Unified cache—bottleneck • No copy back cache—poor multiprocessor
8051	EC000	• Cheap and cheerful	
	68330	• Price	• Poorer price/performance ratio

LSI Logic

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
LR33020	EC040	• Targeted at X-terminals • Cut-down R3000 core	• Poor DRAM performance • Not general purpose • Inferior development tools
33000	EC030	• Cut-down R3000 core • Integrated peripherals • SMT packaging	• Poorer DRAM performance • Not cost effective • Inferior development tools

National Semiconductor

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
FDDI	FDDI CHIP SET	• Basic MAC (BMAC) DP83261 very strong • Very price aggressive at strategic customers • Excellent documentation and support • Integration strategy firm	• Currently 5-chip solution • Critical layout required • No PCM state machine • BSI requires high-performance processor • No second source on MAC/PHY chips • No SMT software

National Semiconductor (continued)

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
HPC16400	68302	• Very price aggressive	• Lower performance core • Limited communications support (HDLC + UART) • Limited addressing range
NS32FX16	68331/332	• On-board DSP • Small package	• Only small installed software base • No configurable timing capabilities
	68302	• On-board DSP • Price aggressive	• Limited protocol support

NEC

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
V25/25+ V35/V35+	68302/340	• Very price aggressive • Single-chip versions available • Runs DOS	• Limited communications capability • Lower addressing range • Lower performance
78kVII	68331/332/333/340	• Very price aggressive	• Only half '302 performance • No timers/flash/microcode capability • No low power capabilities • Limited installed software base

Siemens

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
80C166	68331/332	• Interrupt handler	• Low installed S/W base • Not a widely accepted architecture • No user-configurable timers

SGS-Thomson

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
ST10F166	68F333	• Interrupt handler	• Half as much flash EEPROM • Third of RAM size available • No silicon yet

Toshiba

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
HC000	HC000	• Very price aggressive	• Not Toshiba proprietary architecture • No second-source support network
	68330	• Very price aggressive	• Lower performance • No integration

Toshiba (continued)

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
68301	68302	• Price aggressive • Built-in Centronics	• No DMA • Only 3 dedicated UARTS—no multiple communications • No SCP port or microcode capability
	68306	• Built-in Centronics • 1 more serial channel	• No DRAM controller • Smaller address space
	68340	• Built-in Centronics	• No DMA • Lower CPU Performance • No low power mode
68303	68340	• 1 superior timer • Dedicated motor control • DRAM controller	• Only 3 DMA channels • Lower CPU performance
	68306	• Timer • Dedicated motor control • DMA	• Smaller address space • Less robust DRAM controller

PRODUCT ROUTING

Device & Pkg.	Fab. Site	Probe	Assembly Site	Final Test Site
68000RC,L,P	MOS5	OHT	KLM	OHT
68000FN	MOS5	OHT	KLM/ANAM	OHT
68EC000FN	MOS8	OHT	KLM	OHT
68EC000FU	MOS8	OHT	SHC	SHC
68HC000RC,FN,FC	MOS8/TSC	OHT	KLM	OHT
68HC000P/LC	MOS8	OHT	KLM	OHT
68HC001RC,FN	MOS8	OHT	KLM	OHT
68HC001FC	MOS8	OHT	KLM	OHT
68008P	MOS5	OHT	ANAM	ANAM
68008L	MOS5	OHT	KLM	OHT
68008FN	MOS5	OHT	ANAM	OHT
68010RC,L,P,FN	MOS5	OHT	KLM	OHT
68020RC	MOS8/TSC	OHT/TSC	ATX/KLM	OHT
68020RL,FE	MOS8/TSC	OHT/TSC	KLM	OHT/KLM
68020RP	MOS8/TSC	OHT/TSC	CITIZEN	OHT
68020FC	MOS8/TSC	OHT/TSC	ATX/KLM	OHT/KLM
68EC020RP	MOS8	OHT/TSC	CITIZEN	OHT
68EC020FG	MOS8	OHT/TSC	ANAM	ANAM
68185FN,RC,FN	MOS3	CHNDLR	CHNDLR	CHNDLR
68030RC	MOS8/TSC	OHT/TSC	ATX/KLM	OHT
68030FE	MOS8/TSC	OHT/TSC	ATX/KLM	OHT
68030RP	MOS8/TSC	OHT/TSC	ATX/KLM	OHT
68EC030RP	MOS8/TSC	OHT/TSC	ATX/KLM	OHT
68040RC	MOS8	OHT	ATX	OHT
68230P	MOS5	MOS5	ANAM	ANAM
68230FN,LC	MOS5	MOS5	KLM	OHT
68302RC,FE,FC	MOS8	OHT	KLM	OHT
68306FC	MOS8	OHT	KLM	OHT
68307FG	MOS8	OHT	KLM	OHT
68322FT	MOS8	OHT	KLM	OHT
68330FC	MOS8	OHT	KLM	OHT
68331FC	MOS8	OHT	ATX	OHT
68332FC	MOS8	OHT	ATX	OHT
68340RP	MOS8	OHT	CITIZEN	OHT
68340FE	MOS8	OHT	KLM	OHT
68450RC,L,P	MOS5	MOS5	KLM	OHT
68440RC,L,P,FN	MOS5	MOS5	KLM	OHT
68605RC	MOS8	OHT	KLM	OHT

Device & Pkg.	Fab. Site	Probe	Assembly Site	Final Test Site
68605FN	MOS8	OHT	ANAM	OHT
68606RC	MOS8	OHT	KLM	OHT
68606FN	MOS8	OHT	ANAM	OHT
68661PA,PB,PC	MOS3	MOS5	KLM	KLM
68681P,L	MOS5	MOS5	KLM	KLM
68681FN	MOS5	MOS5	KLM	OHT
2681P,L	MOS5	MOS5	KLM	KLM
2681FN	MOS5	MOS5	KLM	OHT
68824RC	MOS8	OHT	KLM	OHT
68824FN	MOS8	OHT	ANAM	OHT
68851RC	MOS8	OHT	KLM	OHT
68881RC,FN	MOS8	OHT	KLM	OHT
68882RC,FN	MOS8	OHT	KLM	OHT
68901LC,FN	MOS3	OHT	OHT	OHT
68901P	MOS3	OHT	ANAM	ANAM
68836FN	BIP3	BIP3	ATX	OHT
68837KB	MOS6	CHD	CHD	CHD
68837FC	MOS6	CHD	CHD	CHD
68838KB	MOS6	CHD	CHD	CHD
68838FC	MOS6	CHD	CHD	CHD
68839RC	MOS8	OHT	ATX	OHT
68839FE	MOS8	OHT	KLM	OHT
68840RC	MOS8	OHT	ATX	OHT
68840FE	MOS8	OHT	KLM	OHT
68834PB	MOS8	OHT	SWINE	OHT

PACKAGE DESCRIPTION	SITE DESCRIPTION
EM = PLASTIC QUAD FLAT PACK (PQFP)	OHT = OAK HILL, TEXAS
FC = PLASTIC QUAD FLAT PACK (PQFP)	ATX = AUSTIN, TEXAS
FE = CERAMIC QUAD FLAT PACK (CQFP)	KLM = KUALA LUMPUR, MALAYSIA
FG = PLASTIC QUAD FLAT PACK (PQFP)	ANAM = KOREA
FN = PLASTIC LEADED CHIP CARRIER (PLCC)	CITIZEN = CITIZEN
FT = PLASTIC QUAD FLAT PACK (PQFP)	CHNDLR = CHANDLER, ARIZONA
FU = PLASTIC QUAD FLAT PACK (PQFP)	EKB = EAST KILBRIDE, SCOTLAND
L/LC = CERAMIC DIP	MESA = MESA, ARIZONA
P = PLASTIC DUAL-IN-LINE PIN (PDIP)	AIZU = AIZU, JAPAN
RC = CERAMIC PIN GRID ARRAY (PGA)	TSC = TOHOKU, JAPAN
RP = LOW-COST PLASTIC PGA	

FAB. SITE DESCRIPTION			
MOS1	EKB	4 INCH	>1.2 MICRON
MOS2	ATX	4 INCH	LOGIC PRODUCT
MOS3	ATX	4 INCH	>1.2 MICRON
MOS5	MESA	5 INCH	>1.2 MICRON
MOS6	MESA	6 INCH	ASIC PRODUCT
MOS7	AIZU	4 INCH	>1.5 MICRON
MOS8	ATX	5 INCH	0.8–1.5 MICRON
MOS9	EKB	6 INCH	0.8–1.5 MICRON
TOHOKU	TSC	6 INCH	0.8–1.5 MICRON
MOS11	OHT	8 INCH	<0.8 MICRON

THIRD-PARTY SUPPORT

Please refer to BR729/D, *The 68K Source* for third-party support and contacts.

—NOTES—

QUESTIONNAIRE

In order to support your needs, we would appreciate your completing and returning this questionnaire. Please fax to HIPPO, High-Performance Marketing, Austin, Texas (512) 891-2943. Thank you for your cooperation.

1. Are you a: FAE ☐ FSE ☐ FSA ☐ PME ☐
   OTHER ☐ _____

2. Do you see a need for a summarized version of high-performance information like this high-performance update?
   Yes ☐ No ☐

3. If no, why not? _____

4. How will you use a document like HIPPO? I Won't ☐ Office Reference ☐
   Carry with Me ☐

5. What would be your preferred format for receiving this guide?
   A5, time system & punched (like this issue) ☐ A5, bound and not hole punched ☐
   A4, not hole punched ☐ Time manager format ☐
   Other ☐ _____

6. How do you rate the content of this guide?
   From 10 (perfect for my job) to 0 (of no use or interest) _____

7. How often do you believe this guide should be updated?
   Every 12 months ☐ Every 6 months ☐
   Every 3 months ☐ More often ☐

8. Should the distribution list be expanded?
   Yes ☐ No ☐ To whom? _____

9. If updated regularly, is this guide, likely to improve your first customer response on high-performance questions?
   Yes ☐ No ☐

10. Please complete the following (optional): Name _____
    Waccvm user I.D. _____ Location _____

11. Please add any comments: _____

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BR1133/D

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