FC3560 Read Channel Tile Array

GENERAL DESCRIPTION

The FC3560 is an application focused tile array targeted specifically for mass storage applications. This Tile Array can implement all of the functions required in a high performance read channel.

The array consists of optimized circuit blocks for the following functions: a pulse detector, servo demodulator, data separator, frequency synthesizer, write pre-compensation, two crystal oscillators, bandgap reference, as well as 800 gates of uncommitted logic. The logic can be used to implement an encoder/decoder function, address mark generation/detection, or M & N dividers.

Typical performance of circuit blocks integrated on the FC3560 Tile Array is shown in the Tile Array summary below.

Although very specialized, the FC3560 maintains a high degree of flexibility. All of the components are uncommitted until connected with two layers of metal at the final step of the production process. The performance or function of the individual circuit functions can be modified or the architecture chosen to achieve an optimum read channel system.

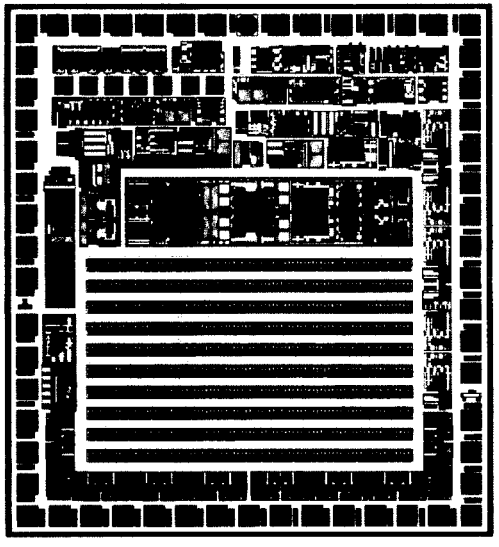
The FC3560 is fabricated using our advanced BiCMOS technology. This 4GHz, 1.5µ process combines the advantages of high speed bipolar with dense CMOS.

FEATURES

- Application Focused Tile Array
- Optimized for Mass Storage Read Channel Functions
- Flexibility at the Functional Block and Component Level
- Advanced 4 GHz, 1.5µ BiCMOS process

ARRAY SUMMARY

Pulse Detector	±0.5ns Pulse Pairing
Servo Demodulator	4 Channels
Data Separator	36 Mbits/s
Frequency Synthesizer	VCO and Charge Pump
Write Pre-Compensation	2 to 20ns
CrystalOscillators (2)	36 MHz
Bandgap Reference	For Servo Reference
Uncommitted Logic Gates	800
Bond Pads	58
Die Size (mils)	134 x 142



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