

# 12-Bit Rail-to-Rail Micropower DAC with Clear Input

September 1996

## FEATURES

- **SO-8 Package**
- 12-Bit Resolution
- **Buffered True Rail-to-Rail Voltage Output**
- **Asynchronous Clear Input**
- Built-In Reference
- Schmitt Trigger On Input Allows Direct Optocoupler Interface
- Power-On Reset Clears DAC to 0V
- 3-Wire Cascadable Serial Interface
- **Maximum DNL Error: 0.5LSB**
- Low Cost

## APPLICATIONS

- Digital Calibration
- Industrial Process Control
- Automatic Test Equipment
- Cellular Telephones

## DESCRIPTION

The LTC<sup>®</sup>1456 is a complete single supply, rail-to-rail voltage output, 12-bit digital-to-analog converter (DAC) in an SO-8 package. It includes an output buffer amplifier and an easy-to-use 3-wire cascadable serial interface. The LTC1456 includes a CLR pin that asynchronously clears the DAC to zero scale.

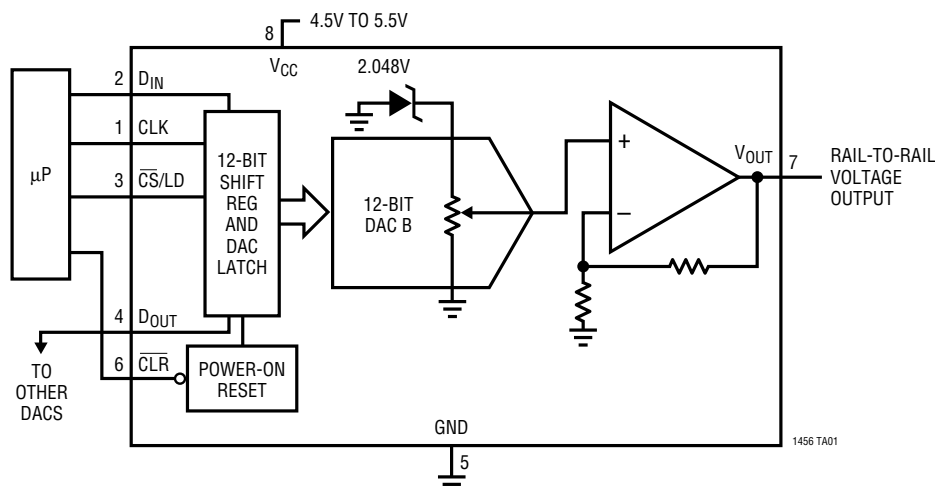
The LTC1456 has an internal 2.048V reference and a full-scale output of 4.095V. It operates on a 4.5V to 5.5V supply, dissipating 2.2mW.

The low power supply current and the space saving SO-8 package make the LTC1456 ideal for battery-powered applications.

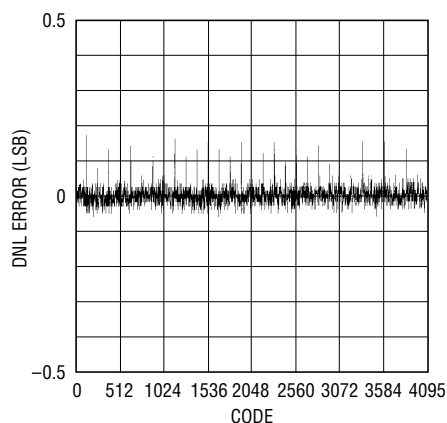
LT, LTC and LT are registered trademarks of Linear Technology Corporation.

## TYPICAL APPLICATION

Functional Block Diagram: 12-Bit Rail-to-Rail DAC with Clear Input



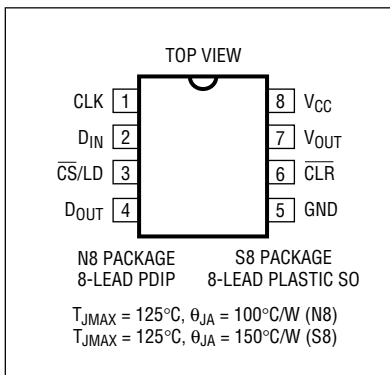
Differential Nonlinearity  
vs Input Code



## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$ to GND .....	–0.5V to 7.5V
Logic Inputs to GND .....	–0.5V to 7.5V
$V_{OUT}$ .....	–0.5V to $V_{CC} + 0.5V$
Maximum Junction Temperature .....	–65°C to 125°C
Operating Temperature Range	
LTC1456C .....	0°C to 70°C
LTC1456I .....	–40°C to 85°C
Storage Temperature Range .....	–65°C to 150°C
Lead Temperature (Soldering, 10 sec) .....	300°C

## PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
	LTC1456CN8 LTC1456IN8 LTC1456CS8 LTC1456IS8
	S8 PART MARKING
	1456 1456I

Consult factory for Military grade parts.

## ELECTRICAL CHARACTERISTICS

 $V_{CC} = 4.5V$  to  $5.5V$ ,  $V_{OUT}$  unloaded,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DAC</b>						
	Resolution		●	12		Bits
DNL	Differential Nonlinearity	Guaranteed Monotonic (Note 1)	●		±0.5	LSB
INL	Integral Nonlinearity	$T_A = 25^\circ C$ (Note 1)	●		±3.5 ±4	LSB LSB
$V_{OS}$	Offset Error	$T_A = 25^\circ C$	●		±12 ±18	mV mV
$V_{OS}TC$	Offset Error Temperature Coefficient			±15		μV/°C
$V_{FS}$	Full-Scale Voltage	$T_A = 25^\circ C$	●	4.065 4.045	4.095 4.145	V V
$V_{FS}TC$	Full-Scale Voltage Temperature Coefficient			±24		ppm/°C

## Power Supply

$V_{CC}$	Positive Supply Voltage	For Specified Performance	●	4.5	5.5	V
$I_{CC}$	Supply Current	(Note 4)	●	430	650	μA

## Op Amp DC Performance

	Short-Circuit Current Low	$V_{OUT}$ Shorted to GND	●		120	mA
	Short-Circuit Current High	$V_{OUT}$ Shorted to $V_{CC}$	●		120	mA
	Output Impedance to GND	Input Code = 0	●	40	120	Ω

## AC Performance

	Voltage Output Slew Rate	(Note 2)	●	0.5	1.0	V/μs
	Voltage Output Settling Time	(Notes 2, 3) to ±0.5LSB			14	μs
	Digital Feedthrough				0.3	nV•s

## ELECTRICAL CHARACTERISTICS

$V_{CC} = 4.5V$  to  $5.5V$ ,  $V_{OUT}$  unloaded,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>Digital I/O</b>							
$V_{IH}$	Digital Input High Voltage		●	2.4			V
$V_{IL}$	Digital Input Low Voltage		●			0.8	V
$V_{OH}$	Digital Output High Voltage	$I_{OUT} = -1mA$ , $D_{OUT}$ Only	●	$V_{CC} - 1.0$			V
$V_{OL}$	Digital Output Low Voltage	$I_{OUT} = 1mA$ , $D_{OUT}$ Only	●			0.4	V
$I_{LEAK}$	Digital Input Leakage	$V_{CC} = 5V$ , $V_{IN} = GND$ to $V_{CC}$	●			$\pm 10$	$\mu A$
$C_{IN}$	Digital Input Capacitance	Guaranteed by Design. Not Subject to Test.	●			10	pF
<b>Switching</b>							
$t_1$	$D_{IN}$ Valid to CLK Setup		●	40			ns
$t_2$	$D_{IN}$ Valid to CLK Hold		●	0			ns
$t_3$	CLK High Time		●	40			ns
$t_4$	CLK Low Time		●	40			ns
$t_5$	$\overline{CS}/LD$ Pulse Width		●	50			ns
$t_6$	LSB CLK to $\overline{CS}/LD$		●	40			ns
$t_7$	$\overline{CS}/LD$ Low to CLK		●	20			ns
$t_8$	$D_{OUT}$ Output Delay	$C_{LOAD} = 15pF$ , $V_{CC} = 5V$	●			150	ns
$t_9$	CLK Low to $\overline{CS}/LD$ Low		●	20			ns
$t_{10}$	$\overline{CLR}$ Pulse Width		●	*	100		ns

The ● denotes specifications which apply over the full operating temperature range.

**Note 1:** Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to code 4095 (full scale).

**Note 2:** Load is  $5k\Omega$  in parallel with  $100pF$ .

**Note 3:** DAC switched between all 1s and the code corresponding to  $V_{OS}$  for the part.

**Note 4:** Digital inputs at  $0V$  or  $V_{CC}$ .

\*Final spec limits will be established for this parameter.

## PIN FUNCTIONS

**CLK (Pin 1):** The Serial Interface Clock. Internal Schmitt trigger on this input allows direct optocoupler interface.

**D<sub>IN</sub> (Pin 2):** The Serial Interface Data. Data on the D<sub>IN</sub> pin is latched into the shift register on the rising edge of the serial clock.

**$\overline{\text{CS/LD}}$  (Pin 3):** The Serial Interface Enable and Load Control. When  $\overline{\text{CS/LD}}$  is low the CLK signal is enabled, so the data can be clocked in. When  $\overline{\text{CS/LD}}$  is pulled high, data is loaded from the shift register into the DAC register, updating the DAC output and the CLK is disabled internally.

**D<sub>OUT</sub> (Pin 4):** The Output of the Shift Register which Becomes Valid on the Rising Edge of the Serial Clock.

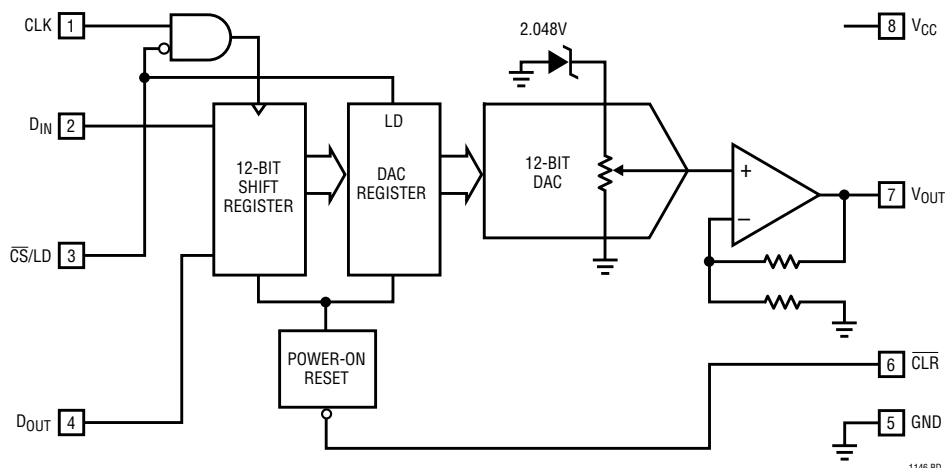
**GND (Pin 5):** Ground.

**$\overline{\text{CLR}}$  (Pin 6):** The Clear Input. When pulled low, this pin asynchronously clears the internal shift and DAC registers to zero scale. Should be tied high for normal operation.

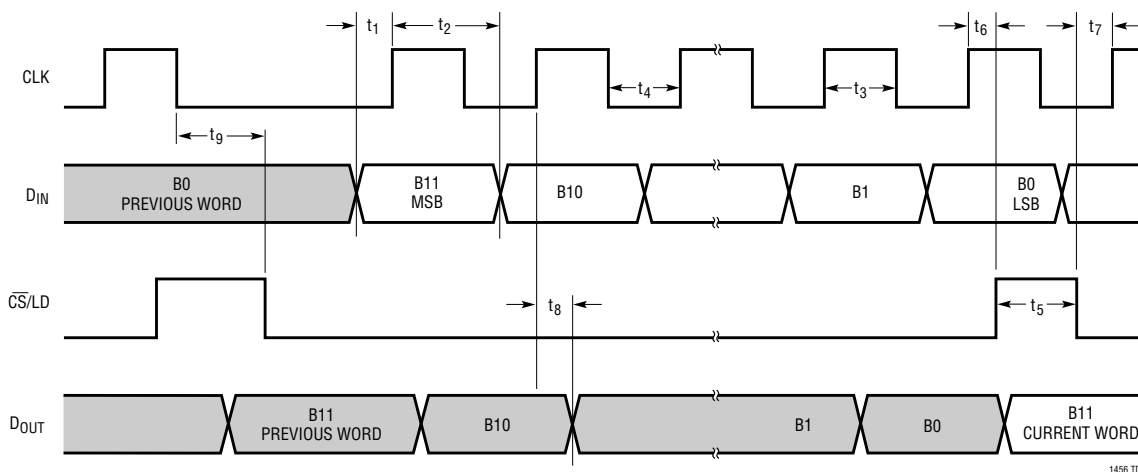
**V<sub>OUT</sub> (Pin 7):** The Buffered DAC Output.

**V<sub>CC</sub> (Pin 8):** The Positive Supply Input.  $4.5\text{V} \leq V_{\text{CC}} \leq 5.5\text{V}$ . Requires a bypass capacitor to ground.

## BLOCK DIAGRAM



## TIMING DIAGRAM



## DEFINITIONS

**Resolution (n):** Resolution is defined as the number of digital input bits, n. It defines the number of DAC output states ( $2^n$ ) that divide the full-scale range. The resolution does not imply linearity.

**Full-Scale Voltage ( $V_{FS}$ ):** This is the output of the DAC when all bits are set to 1.

**Voltage Offset Error ( $V_{OS}$ ):** The theoretical voltage at the output when the DAC is loaded with all zeros. The output amplifier can have a true negative offset, but because the part is operated from a single supply, the output cannot go below zero. If the offset is negative, the output will remain near 0V resulting in the transfer curve shown in Figure 1.

The offset of the part is measured at the code that corresponds to the maximum offset specification:

$$V_{OS} = V_{OUT} - [(Code \times V_{FS}) / (2^n - 1)]$$

**Least Significant Bit (LSB):** One LSB is the ideal voltage difference between two successive codes.

$$LSB = (V_{FS} - V_{OS}) / (2^n - 1) = (V_{FS} - V_{OS}) / 4095$$

$$LSB = 4.095 / 4095 = 1\text{mV}$$

**Integral Nonlinearity (INL):** End-point INL is the maximum deviation from a straight line passing through the end-points of the DAC transfer curve. Because the part operates from a single supply and the output cannot go below zero, the linearity is measured between full scale and the code corresponding to the maximum offset specification. The INL error at a given input code is calculated as follows:

$$INL = [V_{OUT} - V_{OS} - (V_{FS} - V_{OS})(code/4095)] / LSB$$

$V_{OUT}$  = The output voltage of the DAC measured at the given input code

**Differential Nonlinearity (DNL):** DNL is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$DNL = (\Delta V_{OUT} - LSB) / LSB$$

$\Delta V_{OUT}$  = The measured voltage difference between two adjacent codes

**Digital Feedthrough:** The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in (nV)(sec).

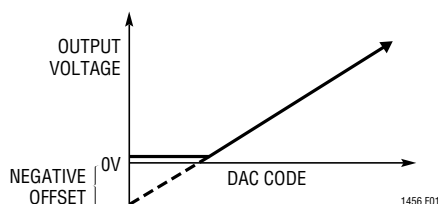


Figure 1. Effect of Negative Offset

## OPERATION

### Serial Interface

The data on the  $D_{IN}$  input is loaded into the shift register on the rising edge of the clock. The MSB is loaded first. The DAC register loads the data from the shift register when  $\overline{CS/LD}$  is pulled high. The CLK is disabled internally when  $\overline{CS/LD}$  is high. Note: CLK must be low before  $\overline{CS/LD}$  is pulled low to avoid an extra internal clock pulse.

When  $\overline{CLR}$  is pulled low it asynchronously resets the shift and DAC registers to all zeros.

The buffered output of the 12-bit shift register is available on the  $D_{OUT}$  pin which swings from GND to  $V_{CC}$ .

Multiple LTC1456s may be daisy-chained together by connecting the  $D_{OUT}$  pin to the  $D_{IN}$  pin of the next chip,

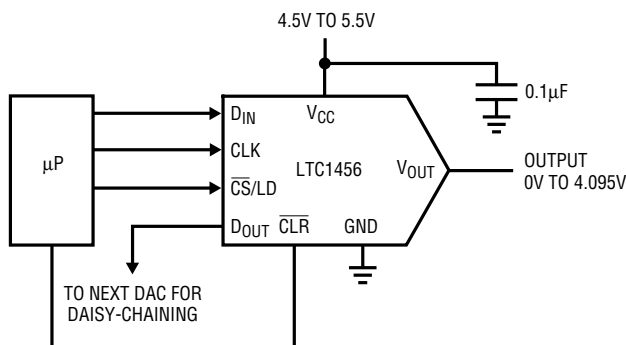
while the CLK and  $\overline{CS/LD}$  signals remain common to all chips in the daisy chain. The serial data is clocked to all of the chips, then the  $\overline{CS/LD}$  signal is pulled high to update all of them simultaneously.

### Voltage Output

The LTC1456's rail-to-rail buffered output can source or sink 5mA over the entire operating temperature range while pulling to within 300mV of the positive supply voltage or ground. The output swings to within a few millivolts of either supply rail when unloaded and has an equivalent output resistance of 40 $\Omega$  when driving a load to the rails. The output can drive 1000pF without going into oscillation.

## TYPICAL APPLICATION

12-Bit 5V Single Supply Voltage Output DAC

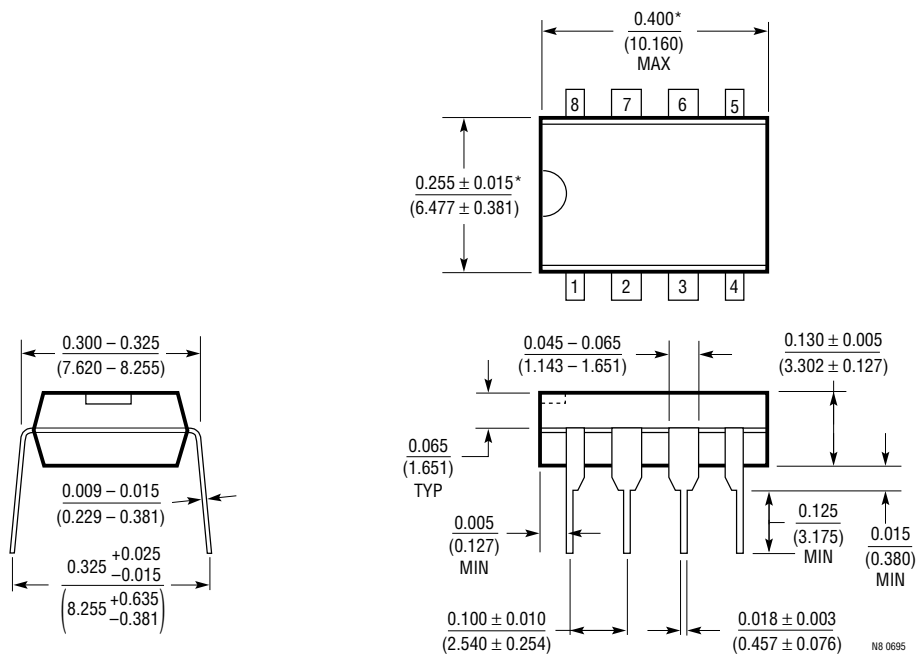


1456 TA03

# PACKAGE DESCRIPTION

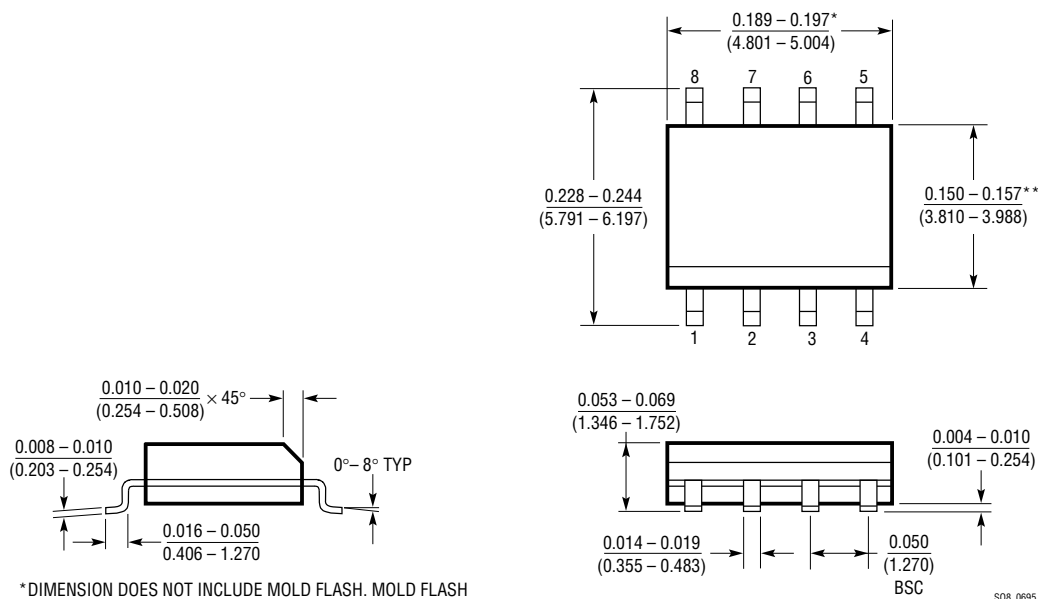
Dimensions in inches (millimeters) unless otherwise noted.

## N8 Package 8-Lead PDIP (Narrow 0.300) (LTC DWG # 05-08-1510)



\*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

## S8 Package 8-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)



\*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH  
SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

\*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD  
FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1257	Single 12-Bit $V_{OUT}$ DAC, Full Scale: 2.048V, $V_{CC}$ : 4.75V to 15.75V, Reference Can Be Overdriven Up to 12V, i.e., $FS_{MAX} = 12V$	5V to 15V Single Supply, Complete $V_{OUT}$ DAC in SO-8 Package
LTC1446/LTC1446L	Dual 12-Bit $V_{OUT}$ DACs in SO-8 Package	LTC1446: $V_{CC} = 4.5V$ to 5.5V, $V_{OUT} = 0V$ to 4.095V LTC1446L: $V_{CC} = 2.7V$ to 5.5V, $V_{OUT} = 0V$ to 2.5V
LTC1450/LTC1450L	Single 12-Bit $V_{OUT}$ DACs with Parallel Interface	LTC1450: $V_{CC} = 4.5V$ to 5.5V, $V_{OUT} = 0V$ to 4.095V LTC1450L: $V_{CC} = 2.7V$ to 5.5V, $V_{OUT} = 0V$ to 2.5V
LTC1451	Single Rail-to-Rail 12-Bit DAC, Full Scale: 4.095V, $V_{CC}$ : 4.5V to 5.5V, Internal 2.048V Reference Brought Out to Pin	Low Power, Complete $V_{OUT}$ DAC in SO-8 Package
LTC1452	Single Rail-to-Rail 12-Bit $V_{OUT}$ Multiplying DAC, $V_{CC}$ : 2.7V to 5.5V	Low Power, Multiplying $V_{OUT}$ DAC with Rail-to-Rail Buffer Amplifier in SO-8 Package
LTC1453	Single Rail-to-Rail 12-Bit $V_{OUT}$ DAC, Full Scale: 2.5V, $V_{CC}$ : 2.7V to 5.5V	3V, Low Power, Complete $V_{OUT}$ DAC in SO-8 Package
LTC1454/LTC1454L	Dual 12-Bit $V_{OUT}$ DACs in SO-16 Package with Added Functionality	LTC1454: $V_{CC} = 4.5V$ to 5.5V, $V_{OUT} = 0V$ to 4.095V LTC1454L: $V_{CC} = 2.7V$ to 5.5V, $V_{OUT} = 0V$ to 2.5V
LTC1458/LTC1458L	Quad 12 Bit Rail-to-Rail Output DACs with Added Functionality	LTC1458: $V_{CC} = 4.5V$ to 5.5V, $V_{OUT} = 0V$ to 4.095V LTC1458L: $V_{CC} = 2.7V$ to 5.5V, $V_{OUT} = 0V$ to 2.5V