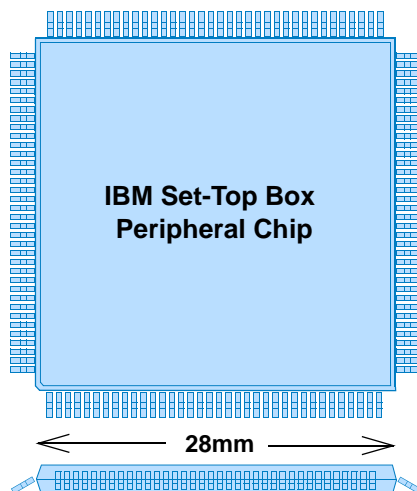


Set-Top Box Peripheral Chip

Highlights

- Seven peripheral units on a single chip:
 - 24-line GPIO controller
 - Serial communications controller (SCC) with two UARTs
 - Three-channel PWM interface
 - Two-port smart card interface
 - Industry standard I²C serial interface
 - SCP serial interface with receive, transmit, and clock functions
 - IEEE 1284 bi-directional parallel interface
- Direct DMA channel connection between PowerPC[®] 403xx and STBP serial ports, parallel port, and smart card interface
- Simple interconnect to any PowerPC 403xx embedded controller



Product Description

With the Set-Top Box Peripheral Chip (STBP), IBM solidifies its presence as a premier vendor of set-top box silicon technology. This single-chip design provides designers with an efficient way to connect and maintain optimum throughput to the high bandwidth peripherals required in set-top box applications.

The STBP functions as a memory-mapped I/O peripheral device, providing a simple interface to the system bus and DMA channels of PowerPC 403GA[®], 403GB[®], 403GC[®] and 403GCX[®] controllers. The STBP chip also provides seven other peripherals:

GPIO Controller —

The GPIO controller contains 24 pins for use as inputs, outputs, or bi-directional. Inputs can be programmed to interrupt.

Serial Ports —

Two UARTs, each supporting baud rates ranging from 1200 baud to 843K baud and each having independent access to DMA channels.

PWM Serial Interface —

A three-channel pulse width modulation interface, supporting IR remote control and IR blaster.

Smart Card Interface —

A two-port ISO/IEC 7816-3 compatible smart card interface, with hardware error checking and eight-bit memory-mapped registers.

I²C Interface —

The I²C interface features bi-directional SCL and SDA lines to support:

- Multiple bus masters
- Mixing of “fast” and “slow” devices on the same bus
- 100 and 400 KHz operation
- 8-bit data transfers
- 7- and 10-bit address decode/generation
- Master and slave transmitters and receivers

SCP Interface —

An inter-chip digital link that performs data exchanges via full-duplex, synchronous, character-oriented channel, and serial communications. Clock rates from 31.25 KHz to 1 MHz are supported.

1284 Interface —

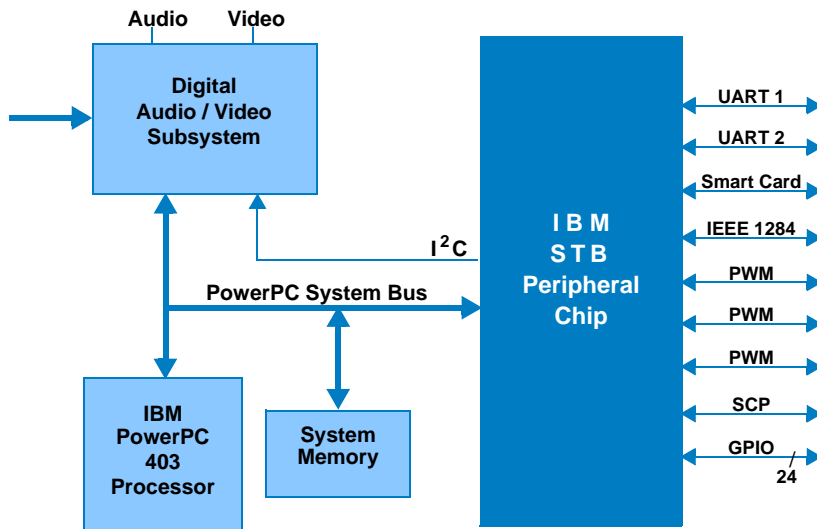
An IEEE standard 1284 parallel interface with the following features:

- Compatibility mode - used as an asynchronous, byte-wide forward channel.
- Nibble mode - used as an asynchronous reverse channel, under processor control.
- Byte mode - used as an asynchronous, byte-wide reverse channel, and used with compatible mode to implement a bi-directional channel.
- ECP mode - used as an asynchronous, byte-wide, bi-directional channel.



Set-Top Box Peripheral Chip Specifications

Technology	0.5µm CMOS
Maximum Case Temp. Range	
Operating	0°C to 120°C
Storage	0°C to 150°C
Power Supply	3.3V ± 150mV (nominal) Supports TTL compatible I/Os and is 5V tolerant on I/Os
Power Dissipation (typical)	0.25W (estimated)
Packaging	144-pin plastic quad flat pack



Set-Top Box Peripheral Chip Interfaces

IBM Microelectronics' commitment to the set-top box market is being recognized by a growing number of designers. You too are invited to employ our technology, tools, and technical support to develop leading-edge, cost-competitive STB solutions.

For more information about this and other IBM set-top box products, contact your nearest IBM Microelectronics office, and visit our web site at:

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