

## PowerPC 401B2, 401C2, and 401D2 Embedded Controller Cores

### Highlights

#### 401 CPU

- Compatible with PowerPC User Instruction Set Architecture
- 138K Dhrystones/Sec @ 75MHz
- 3.2 mm<sup>2</sup>, in 0.35µm CMOS process, (0.27µm L<sub>eff</sub>), three levels of metal
- 32-bit x 32 general purpose registers
- Hardware multiply and divide

#### Cache Controllers

- Fill-first, data forwarding
- Non-blocking flush operations
- Separate I and D controllers

#### Virtual Mode MMU

- Variable page sizes (1 KB-16 MB)
- 64-entry fully-associative TLB

#### I/O Interfaces

- Processor Local Bus (PLB)
- Auxiliary Process Unit (APU)
- On-Chip Memory (OCM)
- Device Control Register (DCR)
- Interrupts
- JTAG

#### Timers

- Support for external timer clock
- 64-bit time-base
- Programmable interval timer
- Fixed interval timer
- Watchdog timer

#### Trace FIFO

- Real-time non-invasive trace
- Exclusive traceback capability

### TheCore Solution

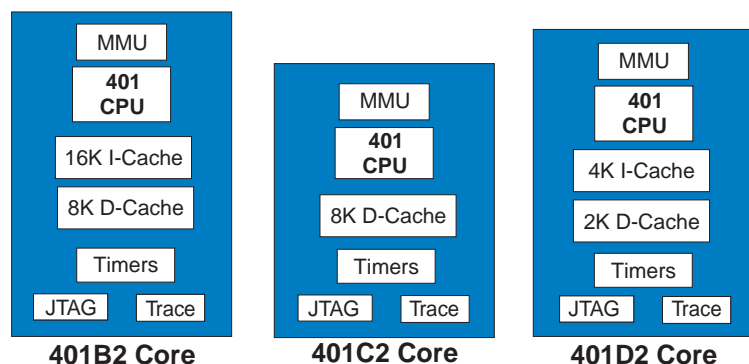
The PowerPC 401B2\*, 401C2\*, and 401D2\* Embedded Controller Cores are 32-bit RISC cores for use in custom logic applications. These embedded cores integrate a PowerPC 401 CPU, as well as separate instruction and data caches, a JTAG port, Trace FIFO, multiple timers, and a memory management (MMU). These cores are available as hard macros in the IBM ASIC library, and can be integrated with peripheral and application-specific macro cores to develop system-on-a-chip (SOC) solutions. The three cores are optimized for low-cost, low-power consumer electronics, communications, and imaging applications.

The PowerPC 401 CPU is compatible with the scalable and flexible PowerPC instruction set architecture, so code written for a PowerPC 401 is compatible with any other PowerPC Embedded Processor. The PowerPC 401 CPU takes advantage of the same high-performance architectural features as other IBM PowerPC 4xx, 6xx, and 7xx processors. At the same time, the 401 CPU implements a simple 3-stage pipeline (fetch, decode, execute) in order to minimize silicon area, thus optimizing SOC designs for low cost.

For optimal performance and cost-control, the PowerPC 401x2 cores integrate and tightly couple features to the 401 CPU. The cache controllers, for example, use sophisticated design techniques typically found in high-performance devices. The MMU implementation is optimal for low cost embedded applications, due to its small size and flexibility. JTAG and Trace FIFO ports enable robust debug capabilities, even in complex SOC designs.

Additionally, these cores are members of the PowerPC 400Series\*, which is supported by the PowerPC Embedded Tools\* Program. In this program, IBM and over 75 select third-party vendors offer a full range of embedded system development tools. Available tools include compilers, debuggers, real-time operating systems and logic analyzers.

Simulation platforms offering a variety of full-function VSS and VHDL simulation models are available for use in product development.





<b>Specifications</b>	<b>401B2</b>	<b>401C2</b>	<b>401D2</b>
<b>Maximum Speed</b>	75 MHz	75 MHz	75 MHz
<b>Technology</b>	0.35µm CMOS (0.27µm L <sub>eff</sub> )	0.35µm CMOS (0.27µm L <sub>eff</sub> )	0.35µm CMOS (0.27µm L <sub>eff</sub> )
<b>I-Cache</b>	16K	0K	4K
<b>D-Cache</b>	8K	8K	2K
<b>MMU</b>	Y	Y	Y
<b>Timers</b>	Y	Y	Y
<b>JTAG</b>	Y	Y	Y
<b>Trace FIFO</b>	Y	Y	Y

### 401xx Core Integration

Through IBM's Core + ASIC System Architecture, the PowerPC 401B2, 401C2, and 401D2 cores easily integrate on-chip with other reusable peripheral and application-specific cores. High speed, high bandwidth peripherals, such as the embedded controller cores, directly attach to the Processor Local Bus (PLB). Less performance-critical cores attach to

the On-Chip Peripheral Bus (OPB). Toolkits are available to assist designing ASICs to the OPB/PLB standard.

For more information on IBM Microelectronics core offerings, view the ever expanding core library on the WWW at <http://www.chips.ibm.com/products/asics/> or contact your local IBM Microelectronics sales office.

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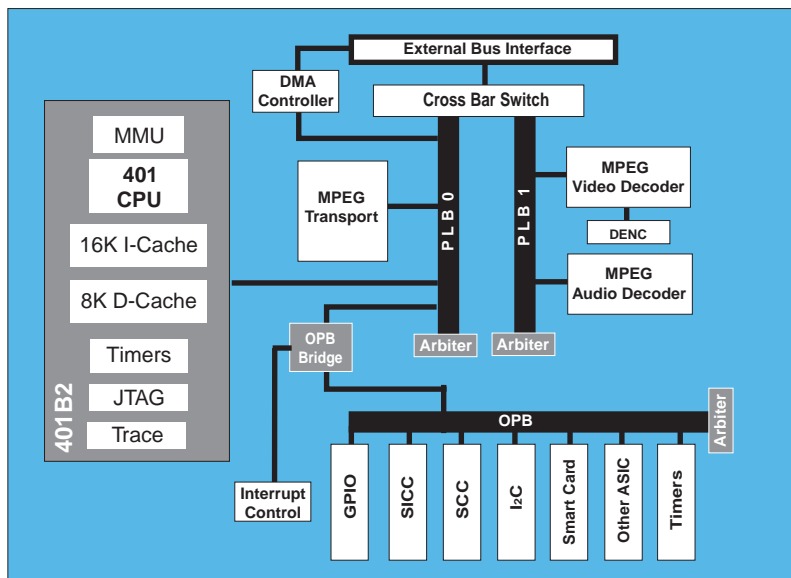
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Example 401x2 Core-Based Digital Video Application