

High Performance, Low Power Consumption

PowerPC 750 RISC Microprocessor

Highlights

Power Management Unit

- Static low-power design
- Dynamic power management
- Integrated Thermal Management Assist Unit

Level 2 (L2) Cache Interface

- Internal L2 cache controller and 4K-entry tags
- Supports 256K, 512K, and 1Mbyte 2-way set associative L2 cache
- Copy-back or write-through data cache
- 64 byte (256K/512K) and 128 byte (1M byte) sectored line size
- Support different speed SRAMs
- Parity on interface

Instruction Fetching & Branch Unit

- 4 instructions fetched per clock
- 64-entry BTIC
- 512-entry BHT

Dispatch Unit

- Dispatches 2 instructions per cycle
- 4-stage pipeline: Fetch, Dispatch, Execute, and Complete

Load/Store Unit

- One cycle cache access
- Executes cache and TLB instructions
- Alignment and number denormalization
- Hit under reload instruction

Fixed-Point Execution Unit

- One cycle add, subtract, shift, or rotate
- Hardware multiply and divide
- Thirty-two, 32-bit General Purpose Registers

Floating-Point Execution Unit

- Optimized for single-precision multiply/add
- IEEE-754 standard single-and double-precision floating point arithmetic
- Thirty-two, 64-bit Floating Point Registers

System Unit

- Executes condition register logical, special register transfer, and other system instructions
- Executes integer add/compare instructions

Memory Management Unit

- 52-bit virtual and 32-bit real addressing
- 8 Block Address Translation registers
- 128-entry, 2-way data and instruction TLB
- Fast-trap mechanism for software reload TLB
- Support Big/Little-endian addressing

Cache Unit

- 32K, 32 byte line, 8-way set associative instruction cache
- 32K, 32 byte line, 8-way set associative data cache
- 3-state coherency (MEI)
- Physically tagged and addressed
- Copy-back or write-through data cache
- Hardware support for data coherency

Bus Interface Unit

- General purpose interface for a wide range of system configurations
- 32-bit address and 64-bit data bus
- Powerful diagnostic and test interface through the Common On-Chip Processor (COP) and IEEE 1149.1 (JTAG) interface
- Parity checking on bus
- Fast reset due to Level Sensitive Scan Design (LSSD)

Product Description

The PowerPC 750™ microprocessor is a 32 bit implementation of the PowerPC™ family of Reduced Instruction Set Computer (RISC) microprocessors. The PowerPC 750 microprocessor is especially suitable for the notebook, mobile and power conscious desktop computing segments. It delivers the impressive performance of desktop system productivity applications at the extremely low typical power consumption of 5.7 watts at 266MHz.

The combination of PowerPCArchitecture™ and state-of-the-art CMOS manufacturing process technology enable the PowerPC 750 microprocessor to feature a 2.6 volt core logic design as well as delivering 3.3 volts for I/O support.

- Higher clock frequencies delivering higher levels of performance
- Dedicated L2 bus independent of the system bus

- A performance enhancing feature supporting misaligned little endian accesses for certain operating system environments



© International Business Machines Corporation 1996
Printed in the United States of America
7-97

All Rights Reserved

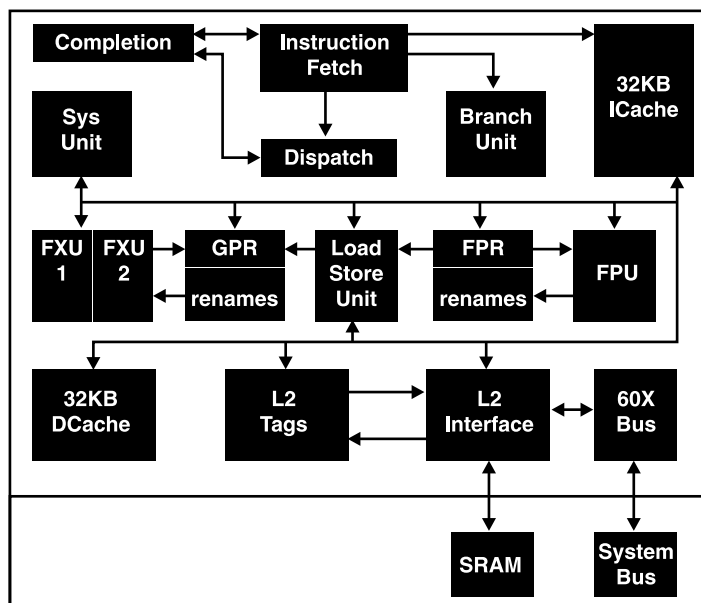
™ Indicates a trademark or registered trademark of the International Business Machines Corporation.

® All other products and company names are trademarks or registered trademarks of their respective holders.

The information contained in this document is subject to change without notice. The products described in this document are NOT intended for use in implantation or other life support applications where malfunction may result in injury or death to persons. The information contained in this document does not affect or change IBM's product specifications or warranties. Nothing in this document shall operate as an express or implied license or indemnity under the intellectual property rights of IBM or third parties. All the information contained in this document was obtained in specific environments, and is presented as an illustration. The results obtained in other operating environments may vary.

THE INFORMATION CONTAINED IN THIS DOCUMENT IS PROVIDED ON AN "AS IS" BASIS. In no event will IBM be liable for any damages arising directly or indirectly from any use of the information contained in this document.

Specifications	PID 8t
Technology	0.25µm / 0.18 Leff - CMOS technology, five levels of metal
Die Size	756 mm x 8.79 mm (67 mm²)
Number of Transistors	6.35 million
Performance (est)	106 SPECint95, 78 SPECfp95 @ 225/64, 1M L2 cache 11.0 SPECint95, 8.1 SPECfp95 @ 233/66, 1M L2 cache 11.8 SPECint95, 8.7 SPECfp95 @ 250/71, 1M L2 cache 12.4 SPECint95, 8.4 SPECfp95 @ 266/66, 1M L2 cache
CPU bus Ratio	3X, 3.5X, 4X, 4.5X, 5X, 5.5X, 6X, 6.5X, 7X, 7.5X, 8X
L1 Cache size	32k Instruction 32k Data
L2 Cache Size	Supports 256K, 512K or 1M byte
Signal I/Os	267
Power Supply	2.6V ± 100mV core 3.3V ± 5% I/O
Power Dissipation Typ./Max. (est)	5.0/70W @ 233MHz 5.7/79W @ 266MHz
Temperature Range	0°C to 105°C
Packaging	Ball Grid Array (360 pins)



IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY
12533-6531
(800) POWERPC

The IBM home page can be found at:
<http://www.ibm.com>

The IBM Microelectronics Division home page
can be found at:
<http://www.chips.ibm.com>

This product's URL is:
<http://www.chips.ibm.com/products/ppc>