

PowerPC 60x Memory Controller and PCI Bridge

Highlights

General

- Extensive programmability
- Flexible and programmable error handling
- Dual split bus structure (CPU-PCI)
- Chipset options configured in register set
- Two low-cost plastic quad flat packs

CPU

- PowerPC 601, 603 and 604 families
- Up to two 66MHz CPUs on CPU bus
- Address pipelining
- Data path latches to enhance bandwidth
- Supports all clock modes
- Bi-Endian operation
- Fully compatible with 60x MCP# TEA# / INT# error reporting signals
- Supports No-DRTRY# / Fast-L2 mode

PCI

- PCI 2.0/2.1 compliant, 33MHz, 3.3V/5V
- Memory mapping of 60x address space into PCI transactions
- Memory accesses snooped to L1 & L2

- Supports ISA bus bridges
- PCI resource locking
- Supports type 0 and type 1 configuration cycles

DRAM

- ECC or parity DRAM error checking
- Page mode or EDO DRAM
- Up to 1G DRAM with 168-pin DIMMs
- Up to 1G DRAM with 72-pin SIMMs
- Up to eight (8) memory banks
- Extensive programmability and flexibility
- On-board refresh timer/counter

L2 Cache Controller

- Look aside, direct mapped, write through
- 256K, 512K or 1M SRAM support
- Sync or async SRAM and tagRAM
- Can be disabled if external L2 is used

ROM

- Up to 2M of ROM
- Flash ROM read, write, and lock-out
- 8 to 64-bit conversion on reads
- Single-beat and burst reads

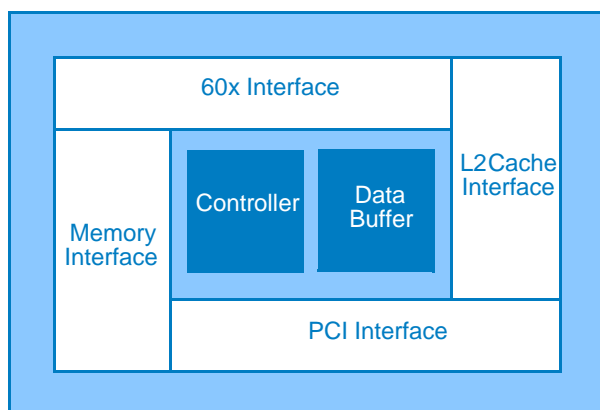
IBM27-82660 Description

IBM Microelectronics offers many opportunities for system designers. The IBM27-82660 PowerPC 60x Memory Controller and PCI Bridge is no exception — especially if you want the opportunity to realize higher performance and efficiency from your PowerPC 60x driven system.

This PowerPC 60x Memory Controller and PCI Bridge is an integrated multi-function chipset, logically residing like a hub connecting the 60x bus, PCI bus, and memory. The controller chip provides a memory-control interface for the 60x processor and the PCI bus. This programmable and flexible memory controller manages all aspects of system DRAM, SRAM and ROM. It supports two CPUs, and provides L2 Cache control. Other support includes error checking, handling and reporting, and onboard refresh generation.

The buffer chip provides a 72-bit wide (64 data and eight error-checking bits) data path between the 6xx processor and system memory. A 32-bit data path is provided to the PCI bus. This buffer chip eliminates the need for an additional 72 bits of external data buffer. It also enhances system performance by providing limited concurrency between the PCI bus and the 60x bus.

Through the highly-tuned integration of these two chips, the IBM PowerPC 60x Memory Controller and PCI Bridge provides support for a variety of system configurations.





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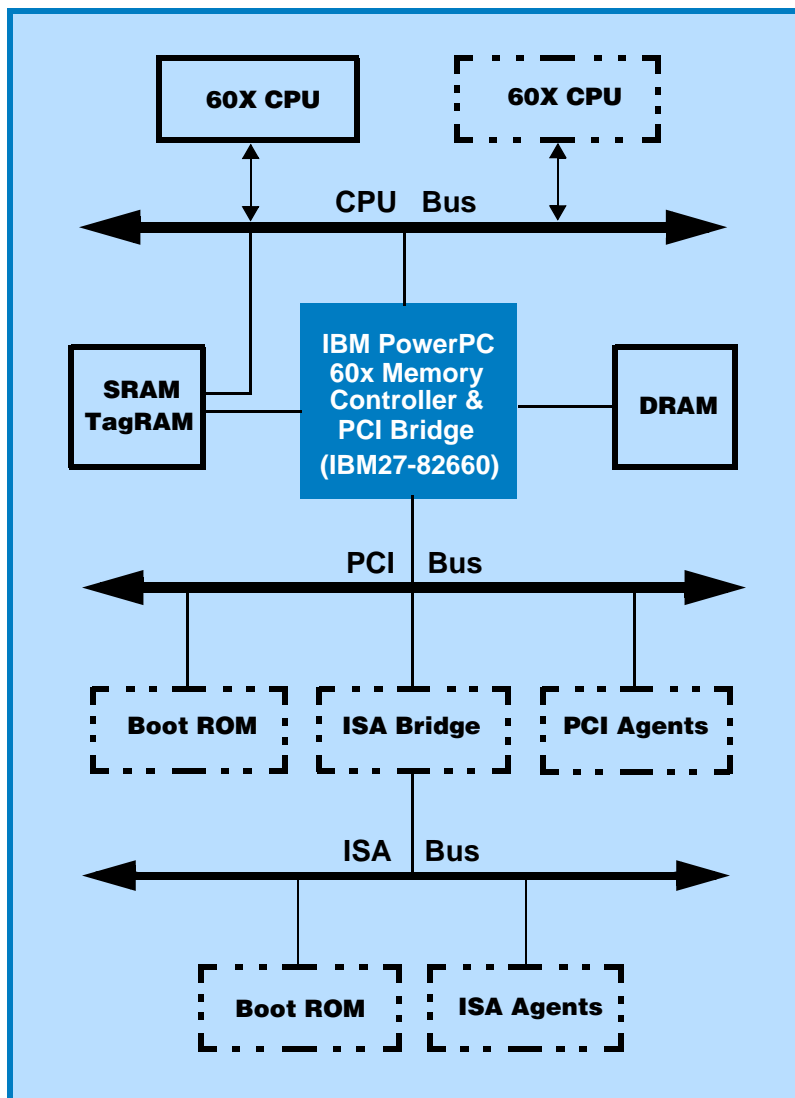
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Pipelined Minimum

Cycle Times	Read	Write
70ns Page DRAM	-4-4-4-4	-3-3-4-4
60ns EDO DRAM	-5-3-3-3	-3-3-3-3
Sync 9ns SRAM	3111 -2111 -2111	Snarf
Async 15ns SRAM	3222 -3222 -3222	Snarf
PCI to Memory (Typ)	81111111 71111111 ... 711	
PCI to Memory (Typ)		51113111 31113111 ... 311



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