

### High Level Schematic

## Description

The PowerPC 603e\* multi-chip module (MCM) contains the PowerPC 603e microprocessor, a PLL clock driver chip, the IBM27-82660 chipset, and L2 cache chips. A block diagram is shown on page one.

The MCM repackages the microprocessor, clocking, L2 cache and cache control, memory control, and PCI bridge functions of the IBM PowerPC 603/604 Reference Design into a single, small MCM package.

The IBM27-82660 Bridge chipset interfaces the CPU to the DRAM memory off the MCM, and provides L2 cache control for the tag RAM and 512k of L2 memory located on the MCM. The 660 Bridge chipset also interfaces the CPU to the PCI bus, which comes off the MCM.

The compact size of the MCM makes it well suited for data processing applications where size is a factor.

## Purpose

The PowerPC 603e MCM is targeted at data processing, portable, or high-end embedded control applications where size and performance are factors. The MCM also enables quick time-to-market and lower total system cost advantages by packaging the most demanding portion of a system for the user on a single package.

## Interface

The MCM connects to a motherboard through 831 solder columns on the bottom side of the MCM. The solder columns are located as shown under Bottom Surface Layout on page 5. The 831 pins are divided functionally as follows:

- Signal (449)
- Daisy chain (40)
- Ground (128)
- 3.3V (127)
- 5.0V (9)
- Unused/Reserved (78)

## Configuration

Clock speeds are set by the user by tying selected module I/O signals high or low. The MCM is intended for use such that the processor operates at 100 MHz internally with a 66 MHz local bus.

The module is populated with a Motorola MPC970 PLL Clock Driver to provide system and PCI clocks to the other chips on the MCM and PCI clocks to PCI devices on the user's motherboard. The user must provide either a reference TTL or oscillator input to the MCM. All clocks come off the module and return such that the user can match clock lengths based on the distance of the user's PCI devices from the MCM.

## Test/Debug

Most nets on the MCM go to module I/O. Though there are 449 signals coming off the MCM, not all must be wired by the user. The PCI and system memory interface, along with other control signals must be wired on the motherboard. But the other nets on the MCM, like the 60X bus data, address and control signals, are made available to the user to facilitate testing and debug of the MCM and system if desired. These test signals do not need to be wired for operation of the MCM in a system environment.

The RISCWATCH signals of the PowerPC 603e are wired directly to module I/O. The user is expected to wire these signals to a RISCWATCH connector on the motherboard.

## Availability

Sample MCMs will be available 2Q96.

## Schematic

A 23 page schematic is available hardcopy. Sockets are available for modules with or without columns for test and burn-in.

The schematic can be sent softcopy through e-mail in PostScript format.

A netlist or a list of the I/O of the MCM is available in softcopy.

## Bill of Materials

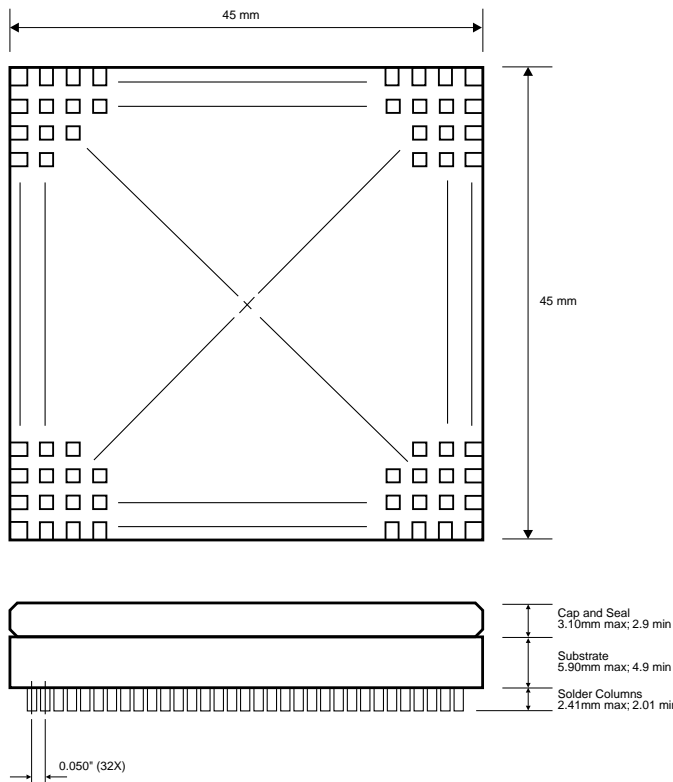
- PowerPC 603e microprocessor
- Motorola MPC970 clock driver chip
- IBM 041814 64kx18 SRAM - 9 ns (4X)
- IBM 27-82664 Controller - version 1.2
- IBM 27-82663 Buffer - version 2.0
- Integrated Device Technology IDT71216 Tag RAM
- Texas Instruments SN74LVT16245 Transceiver
- Custom resistor chip
- Capacitors

## Reference

The MCM is based on the PowerPC 603/604 Reference Design. The PowerPC 603/604 Reference Design Technical Specification is the key reference document for users of the MCM. Other documents include:

- PowerPC 603e RISC Microprocessor Hardware Specification
- PowerPC 603e RISC Microprocessor Technical Summary
- PowerPC 603/604 RISC Microprocessor Hardware Specification
- The IBM27-82660 PowerPC to PCI Bridge User's Manual
- Motorola MPC970 Data Sheet
- Integrated Device Technology IDT71216 Data Sheet
- IBM IBM041814 Data Sheet

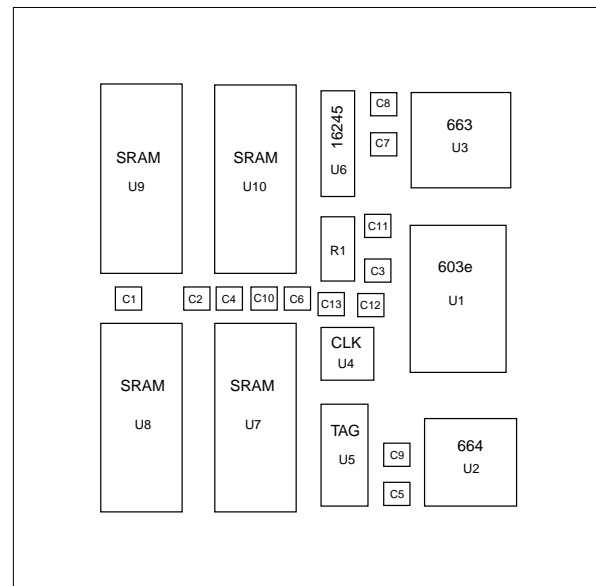
## Physical Characteristics



### Notes:

- Not to scale
- All dimensions nominal. Contact IBM for product drawings
- Sufficient airflow should be provided across the heat sink
- Heat sink is to be provided by user

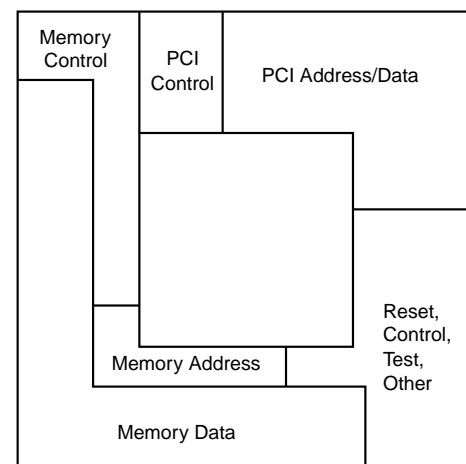
## Top Surface Layout



### Notes:

- Not to scale
- Refer to schematic for reference designators (Ux)
- Chips are in bare-die form, flip-chip joined to ceramic substrate. They are not visible under the cap

## Module I/O Signal Locations



### Notes:

- X-ray view, though th MCM top
- Shows approximate grouping of signals
- Center region contains 60X bus signals and others that do not need to be wired for system operation
- Daisy chain nets not shown



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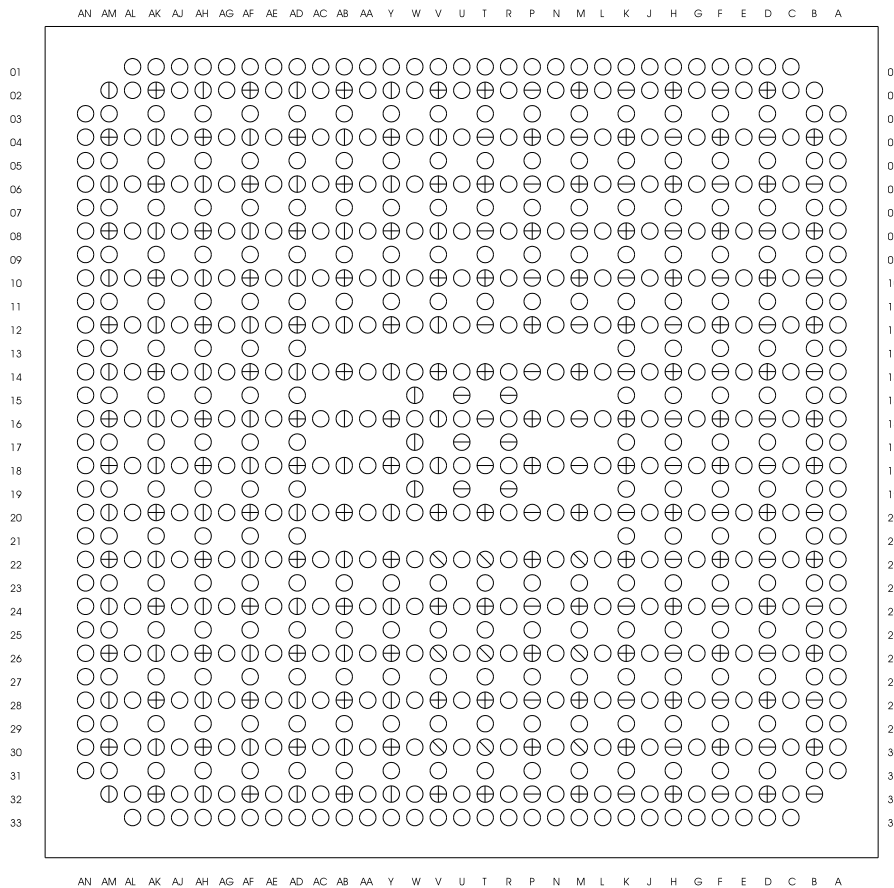
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## Bottom Surface Layout

(X-ray view, though the MCM from the top)



○ SIGNAL    ⊕ ⊖ 3.3 V    ⊖ 5.0 V    ⊕ GROUND