

# PowerPC 603 Embedded Processor

## 66 MHz

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### Highlights

#### **Power Management Unit**

- Power Management Unit
- Static low-power design
- Dynamic power management
- Processor:bus clock ratio of half integer increments up to 6:1

#### **Instruction Fetching & Branch Unit**

- 6-instruction prefetch queue
- Static branch prediction

#### **Dispatch Unit**

- Dispatches 2 instructions per cycle
- 4-stage pipeline: Fetch, Dispatch, Execute, and Complete

#### **Load/Store Unit**

- One cycle cache access
- Executes cache and TLB instructions
- Alignment and number denormalization
- Hit under reload instruction

#### **Fixed-Point Execution Unit**

- One cycle add, subtract, shift, or rotate
- Hardware multiply and divide
- Thirty-two, 32-bit General Purpose Registers

#### **Floating-Point Execution Unit**

- Optimized for single-precision multiply/add
- IEEE-754 standard single-and double-precision floating point arithmetic
- Thirty-two, 64-bit Floating Point Registers

#### **System Unit**

- Executes condition register logical, special register transfer, and other system instructions
- Executes integer add/compare instructions

#### **Memory Management Unit**

- 52-bit virtual and 32-bit real addressing
- 8 Block Address Translation registers
- 64-entry, 2-way data and instruction TLB
- Fast-trap mechanism for software reload TLB

#### **Cache Unit**

- 8K, 32 byte line, 4-way set associative instruction cache
- 8K, 32 byte line, 4-way set associative data cache
- 3-state coherency (MEI)
- Physically tagged and addressed
- Copy-back data cache
- Hardware support for data coherency

#### **Bus Interface Unit**

- Bus Interface Unit
- General purpose interface for a wide range of system configurations
- 32-bit address and selectable 64- or 32-bit data bus
- Powerful diagnostic and test interface through the Common On-Chip
- Processor (COP) and IEEE 114 9.1 (JTAG) interface
- Parity checking on bus
- Fast reset due to Level Sensitive Scan Design (LSSD)

### Product Description

The PowerPC 603<sup>tm</sup> microprocessor is a 32 bit implementation of the PowerPC<sup>tm</sup> family of Reduced Instruction Set Computer (RISC) microprocessors.

The PowerPC 603 is especially suitable for networking and network computing applications. The combination of PowerPC Architecture<sup>tm</sup> and state-of-the-art CMOS manufacturing process technology enable the 603 to feature a 3.3 volt core logic design as well as delivering 3.3 volts for I/O support. Enhancements to this generation of the PowerPC 603 microprocessor family include:

- Higher clock frequencies delivering higher levels of performance
- Additional bus divider ratios making it easier to design in
- A new performance enhancing feature supporting misaligned little endian accesses for certain operating system environments



## PowerPC 603 Specifications (66 MHz)

<b>Technology</b>	0.5µm CMOS technology, four levels of metal
<b>Frequency</b>	66 MHz
<b>Performance</b>	62 SPECint92, 54 SPECfp92 @ 66 MHz
<b>CPU Bus Ratio</b>	1X, 2X
<b>Cache Size</b>	8K Instruction, 8K Data
<b>Signal I/Os</b>	165
<b>Power Supply</b>	3.3V ± 5% I/O, Core
<b>Power Dissipation (typ.)</b>	2.2W @ 66.67 MHz
<b>Number of Transistors</b>	~ 1.6 million
<b>Max Case Temp. Range</b>	0°C to 105°C
<b>Packaging</b>	240 C4FP
<b>Die Size</b>	7.4 mm x 11.5 mm (85 mm <sup>2</sup> )
<b>Part Numbers</b>	IBM25EMPPC603FE-066 (uncapped) IBM25EMPPCC603FE-066 (capped)

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