

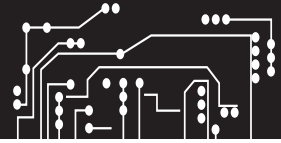


PowerPC 403GB

32-Bit RISC

Embedded Controller

**Data
Sheet**



Features

- PowerPC™ RISC CPU and instruction set architecture
- Glueless interfaces to DRAM, SRAM, ROM, and peripherals, including byte and half-word devices
- Separate instruction cache and write-back data cache, both two-way set-associative
- Minimized interrupt latency
- Individually programmable on-chip controllers for:
 - Two DMA channels
 - DRAM, SRAM, and ROM banks
 - Peripherals
 - External interrupts
- Flexible interface to external bus masters
- Hardware multiplier and divider for faster integer arithmetic
- Thirty-two 32-bit general purpose registers

Applications

- Set-top boxes
- Consumer electronics and video games
- Telecommunications and networking
- Office automation (printers, copiers, fax machines)

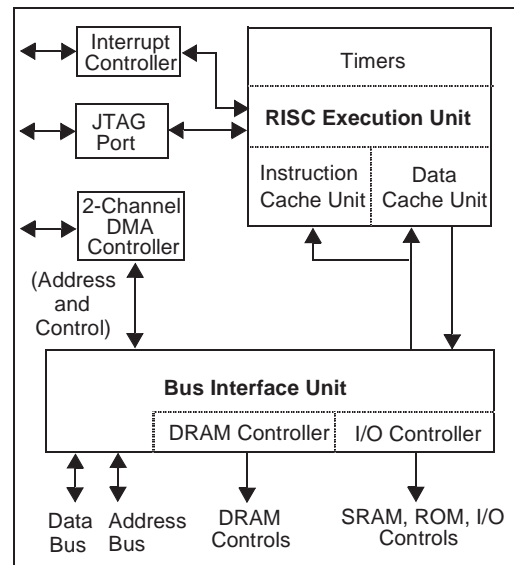
Specifications

- 28MHz operation
- Interfaces to both 3V and 5V technologies
- Low-power 3.3V operation with built-in power management and stand-by mode
- Low-cost 128 lead TQFP package
- 0.5 μm triple-level-metal CMOS

Overview

The PowerPC 403GB 32-bit RISC embedded controller offers high performance and functional integration with low power consumption. The 403GB RISC CPU executes at sustained speeds approaching one cycle per instruction. On-chip caches and integrated DRAM and SRAM control functions reduce chip count and design complexity in systems, while improving system throughput.

External I/O devices or SRAM/DRAM memory banks can be directly attached to the 403GB bus interface unit (BIU). Interfaces for up to six memory banks and I/O devices, including a maximum of two DRAM banks, can be configured individually, allowing the BIU to manage devices or memory banks with differing control, timing, or bus width requirements.



The 403GB RISC controller consists of a pipelined RISC processor core and several peripheral interface units: BIU, DMA controller, asynchronous interrupt controller, and JTAG debug port.

The RISC processor core includes the internal 2KB instruction cache and 1KB data cache, reducing overhead for data transfers to or from external memory. The instruction queue logic manages branch prediction, folding of branch and condition register logical instructions, and instruction prefetching to minimize pipeline stalls.

RISC CPU

The RISC core comprises three tightly coupled functional units: the execution unit (EXU), the data cache unit (DCU), and the instruction cache unit (ICU). Each cache unit consists of a data array, tag array, and control logic for cache management and addressing. The execution unit consists of general purpose registers (GPR), special purpose registers (SPR), ALU, multiplier, divider, barrel shifter, and the control logic required to manage data flow and instruction execution within the EXU.

The EXU handles instruction decoding and execution, queue management, branch prediction, and branch folding. The instruction cache unit passes instructions to the queue in the EXU or, in the event of a cache miss, requests a fetch from external memory through the bus interface unit.

General Purpose Registers

Data transfers to and from the EXU are handled through the bank of 32 GPRs, each 32 bits wide. Load and store instructions move data operands between the GPRs and the data cache unit, except in the cases of noncacheable data or cache misses. In such cases the DCU passes the address for the data read or write to the BIU. When noncacheable operands are being transferred, data can pass directly between the EXU and the BIU, which interfaces to the external memory being accessed.

Special Purpose Registers

Special purpose registers are used to control debug facilities, timers, interrupts, the protection mechanism, memory cacheability, and other

architected processor resources. SPRs are accessed using move to/from special purpose register (mtspr/mfspr) instructions, which move operands between GPRs and SPRs.

Supervisory programs can write the appropriate SPRs to configure the operating and interface modes of the execution unit. The condition register (CR) and machine state register (MSR) are written by internal control logic with program execution status and machine state, respectively. Status of external interrupts is maintained in the external interrupt status register (EXISR). Fixed-point arithmetic exception status is available from the exception register (XER).

Device Control Registers

Device control registers (DCR) are used to manage I/O interfaces, DMA channels, SRAM and DRAM memory configurations and timing, and status/address information regarding bus errors. DCRs are accessed using move to/from device control register (mtdcr/mfdcr) instructions, which move operands between GPRs and DCRs.

Instruction Set

Table 1 summarizes the 403GB instruction set by categories of operations. Most instructions execute in a single cycle, with the exceptions of load/store multiple, load/store string, multiply, and divide instructions.

Bus Interface Unit

The bus interface unit integrates the functional controls for data transfers and address operations other than those which the DMA controller handles. DMA transfers use the address logic in the BIU to output the memory addresses being accessed.

Control functions for direct-connect I/O devices and for DRAM, SRAM, or ROM banks are provided by the BIU. Burst access for SRAM, ROM, and page-mode DRAM devices is supported for cache fill and flush operations.

The BIU controls the transfer of data between the external bus and the instruction cache, the data cache, or registers internal to the processor core. The BIU also arbitrates among external bus master and DMA transfers, the internal buses to the

cache units and the register banks.

Memory Addressing Regions

The 403GB can address an effective range of 3.192 GB (128 MB DRAM; 64 MB SRAM, ROM or other I/O; and 3GB reserved). SRAM banks can be up to 16MB and DRAM banks for internally multiplexed access can be up to 64MB. Cacheability with respect to the instruction or data cache is programmed via the instruction and data cache control registers, respectively.

Within the DRAM and SRAM/ROM regions, a total of six banks of devices are supported. Each bank can be configured for 8-, 16-, or 32-bit devices.

For individual DRAM banks, the number of wait states, bank size, $\overline{\text{RAS}}$ -to- $\overline{\text{CAS}}$ timing, use of an external address multiplexer (for external bus masters), and refresh rate are user-programmable. For each SRAM/ROM bank, the bank size, bank location, number of wait states, and timings of chip selects, byte enables, and output enables are all user-programmable.

Instruction Cache Unit

The instruction cache unit (ICU) is a two-way set-associative 2KB cache memory unit with enhancements to support branch prediction and folding. The ICU is organized as 64 sets of 2

lines, each line containing 16 bytes. A separate bypass path is available to handle cache-inhibited instructions and to improve performance during line fill operations.

The cache can send two cached instructions per cycle to the execution unit, allowing instructions to be folded out of the queue without interrupting normal instruction flow. When a branch instruction is folded and executed in parallel with another instruction, the ICU provides two more instructions to replace both of the instructions just executed so that bandwidth is balanced between the ICU and the execution unit.

Data Cache Unit

The data cache unit is provided to minimize the access time of frequently used data items in main store. The 1KB cache is organized as a two-way set associative cache. There are 32 sets of 2 lines, each line containing 16 bytes of data. The cache features byte-writeability to improve the performance of byte and halfword store operations.

Cache operations are performed using a write-back strategy. A write-back cache only updates locations in main storage that corresponds to changed locations in the cache. Data is flushed from the cache to main storage whenever changed data needs to be removed from the

Table 1. 403GB Instructions by Category

Category	Base Instructions
Data Movement	load, store
Arithmetic / Logical	add, subtract, negate, multiply, divide, and, or, xor, nand, nor, xnor, sign extension, count leading zeros
Comparison	compare, compare logical, compare immediate
Branch	branch, branch conditional
Condition	condition register logical
Rotate/Shift	rotate, rotate and mask, shift left, shift right
Cache Control	invalidate, touch, zero, flush, store
Interrupt Control	write to external interrupt enable bit, move to/from machine state register, return from interrupt, return from critical interrupt
Processor Management	system call, synchronize, move to/from device control registers, move to/from special purpose registers

cache to make room for other data.

The data cache may be disabled for a 128MB memory region via control bits in the data cache control register. A separate bypass path is available to handle cache-inhibited data operations and to improve performance during line fill operations.

Cache flushing and filling are triggered by load, store, and cache control instructions executed by the processor. Cache blocks are loaded starting at the requested fullword, continuing to the end of the block and then wrapping around to fill the remaining fullwords at the beginning of the block.

DMA Controller

The two-channel DMA controller manages block data transfers in buffered, fly-by and memory-to-memory transfer modes with options for burst-mode operation. In fly-by and buffered modes, the DMA controller supports transactions between memory and peripheral devices.

Each DMA channel provides a control register, a source address register, a destination address register, a transfer count register, and a chained count register. Peripheral set-up cycles, wait cycles, and hold cycles can be programmed into each DMA channel control register. Each channel supports chaining operations. The DMA status register holds the status of both channels.

Exception Handling

Table 2 summarizes the 403GB exception priorities, types, and classes. Exceptions are generated by interrupts from internal and external peripherals, instructions, the internal timer facility, debug events or error conditions. Six external interrupt signals are provided on the 403GB: one critical and five general-purpose, all individually maskable.

All exceptions fall into three basic classes: asynchronous imprecise exceptions, synchronous precise exceptions, and asynchronous precise exceptions. Asynchronous exceptions are caused by events external to processor execution, while synchronous exceptions are caused by instructions.

Except for a system reset or machine check, all

403GB exceptions are handled precisely. Precise handling implies that the address of the excepting instruction (synchronous exceptions other than system call) or the address of the next sequential instruction (asynchronous exceptions and system call) is passed to the exception handling routine. Precise handling also implies that all instructions prior to the excepting instruction have completed execution and have written back their results.

Asynchronous imprecise exceptions include system resets and machine checks. Synchronous precise exceptions include most debug exceptions, program exceptions, protection violations, system calls, and alignment error exceptions. Asynchronous precise exceptions include the critical interrupt exception, external interrupts, and internal timer facility exceptions and some debug events.

Only one exception is handled at a time. If multiple exceptions occur simultaneously, they are handled in priority order.

The 403GB processes exceptions as reset, critical, or noncritical. Four exceptions are defined as critical: machine check exceptions, debug exceptions, exceptions caused by an active level on the critical interrupt pin, and the first time-out from the watchdog timer.

When a noncritical exception is taken, special purpose register Save/Restore 0 (SRR0) is loaded with the address of the excepting instruction (synchronous exceptions other than system call) or the next sequential instruction to be processed (asynchronous exceptions and system call). If the 403GB is executing a multicycle instruction (load/store multiple, load/store string, multiply or divide), the instruction is terminated and its address stored in SRR0. Save/Restore Register 1 (SRR1) is loaded with the contents of the machine state register. The MSR is then updated to reflect the new context of the machine. The new MSR contents take effect beginning with the first instruction of the exception handling routine.

At the end of the exception handling routine, execution of a return from interrupt (rfi) instruction forces the contents of SRR0 and SRR1 to be

loaded into the program counter and the MSR, respectively. Execution then begins at the address in the program counter.

The four critical exceptions are processed in a similar manner. When a critical exception is taken, SRR2 and SRR3 hold the next sequential address to be processed when returning from the exception and the contents of the machine state register, respectively. After the critical exception handling routine, return from critical interrupt (rfci) forces the contents of SRR2 and SRR3 to be loaded into the program counter and the MSR, respectively.

Timers

The 403GB contains four timer functions: a time base, a programmable interval timer (PIT), a fixed interval timer (FIT), and a watchdog timer. The time base is a 56-bit counter incremented at the timer clock rate. The timer clock is driven by an internal signal equal to the processor clock rate. No interrupts are generated when the time base rolls over.

The programmable interval timer is a 32-bit register that is decremented at the same rate as the time base is incremented. The user preloads the PIT register with a value to create the desired delay. When the register is decremented to zeros, the timer stops decrementing, a bit is set in the timer status register (TSR), and a PIT interrupt is generated. Optionally, the PIT can be pro-

grammed to reload automatically the last value written to the PIT register, after which the PIT begins decrementing again. The timer control register (TCR) contains the interrupt enable for the PIT interrupt.

The fixed interval timer generates periodic interrupts based on selected bits in the time base. Users may select one of four intervals for the timer period by setting the correct bits in the TCR. When the selected bit in the time base changes from 0 to 1, a bit is set in the TSR and a FIT interrupt is generated. The FIT interrupt enable is contained in the TCR.

The watchdog timer generates a periodic interrupt based on selected bits in the time base. Users may select one of four time periods for the interval and the type of reset generated if the watchdog timer expires twice without an intervening clear from software. If enabled, the watchdog timer generates a system reset unless an exception handler updates the watchdog timer status bit before the timer has completed two of the selected timer intervals.

JTAG Port

The JTAG port has been enhanced to allow it to be used as a debug port. Through the JTAG test access port, debug software on a workstation can single-step the processor and interrogate internal processor state to facilitate software

Table 2. 403GB Exception Priorities, Types and Classes

Priority	Exception Type	Exception Class
1	System Reset	Asynchronous imprecise
2	Machine Check	Asynchronous imprecise
3	Debug	Synchronous precise (except UDE and EXC)
4	Critical Interrupt	Asynchronous precise
5	WatchdogTimer Time-out	Asynchronous precise
6	Program Exception, Protection Violation, and System Calls	Synchronous precise
7	Alignment Exceptions	Synchronous precise
8	External Interrupts	Asynchronous precise
9	Fixed Interval Timer	Asynchronous precise
10	Programmable Interval Timer	Asynchronous precise

IBM PowerPC 403GB

debugging. The standard JTAG boundary-scan register allows testing of circuitry external to the chip, primarily the board interconnect. Alternatively, the JTAG bypass register can be selected when no other test data register needs to be accessed during a board-level test operation.

P/N Code

Table 3. PPC403GB Part Number

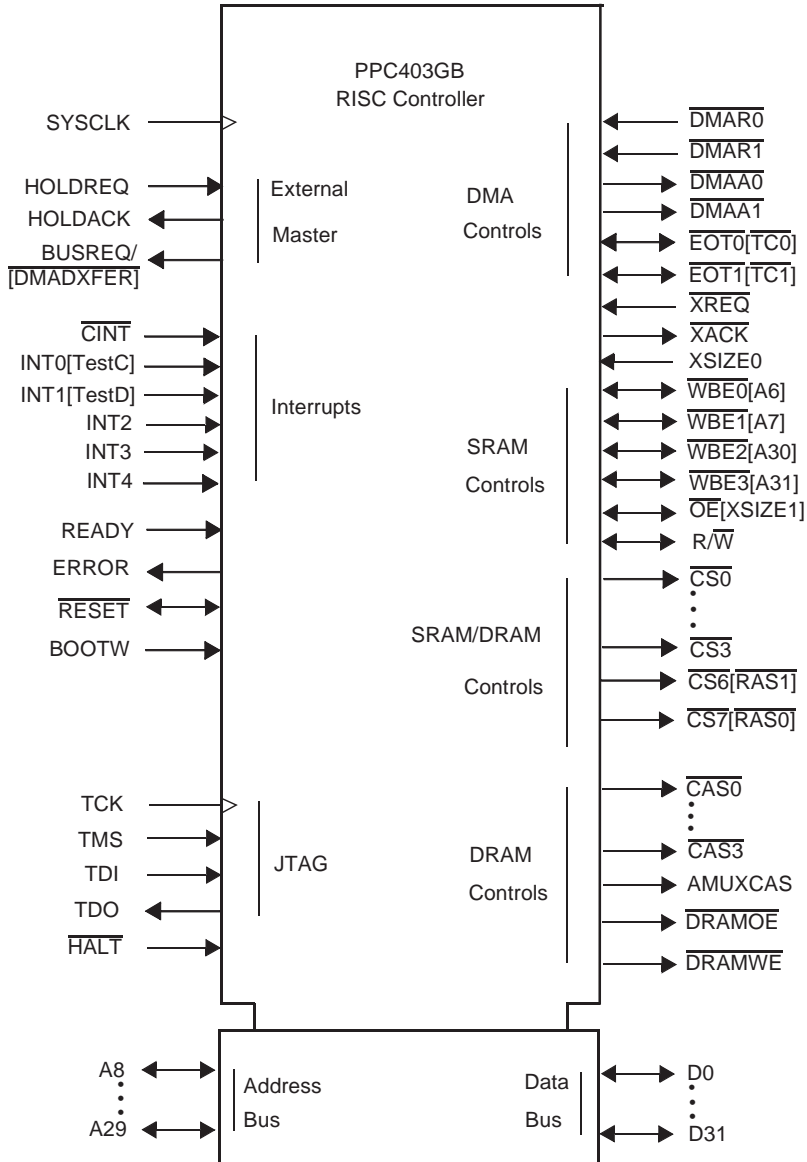
MHz	Part Number
28	PPC403GB-KA28C-1

Notes:

- 1. The dash number indicates the speed version.
- 2. The characters in the dash number indicate package type (K), revision level (A), commercial version (C).

Logic Symbol

Signals in brackets are multiplexed..



Pin Functional Descriptions

Active-low signals are shown with overbars: $\overline{\text{DMAR0}}$. Multiplexed signals are alphabetized under the first (unmultiplexed) signal names on the same pins. The logic symbol on the preceding page shows all 403GB signals arranged by functional groups.

Table 4. 403GB Signal Descriptions

Signal Name	Pin	I/O Type	Function
A8	79	I/O	Address Bus Bit 8. When the 403GB is bus master, this is an address output from the 403GB. When the 403GB is not bus master, this is an address input from the external bus master, to determine bank register usage.
A9	80	I/O	Address Bus Bit 9. See description of A8
A10	81	I/O	Address Bus Bit 10. See description of A8
A11	82	I/O	Address Bus Bit 11. See description of A8
A12	83	O	Address Bus Bit 12. When the 403GB is bus master, this is an address output from the 403GB.
A13	86	O	Address Bus Bit 13. See description of A12.
A14	87	O	Address Bus Bit 14. See description of A12.
A15	88	O	Address Bus Bit 15. See description of A12.
A16	89	O	Address Bus Bit 16. See description of A12.
A17	90	O	Address Bus Bit 17. See description of A12.
A18	92	O	Address Bus Bit 18. See description of A12.
A19	93	O	Address Bus Bit 19. See description of A12.
A20	94	O	Address Bus Bit 20. See description of A12.
A21	95	O	Address Bus Bit 21. See description of A12.
A22	96	I/O	Address Bus Bit 22. When the 403GB is bus master, this is an address output from the 403GB. When the 403GB is not bus master, this is an address input from the external bus master, to determine page crossings.
A23	97	I/O	Address Bus Bit 23. See description of A8

Table 4. 403GB Signal Descriptions (Continued)

Signal Name	Pin	I/O Type	Function
A24	98	I/O	Address Bus Bit 24. See description of A8
A25	99	I/O	Address Bus Bit 25. See description of A8
A26	101	I/O	Address Bus Bit 26. See description of A8
A27	102	I/O	Address Bus Bit 27. See description of A8
A28	103	I/O	Address Bus Bit 28. See description of A8
A29	104	I/O	Address Bus Bit 29. See description of A8
AMuxCAS	127	O	DRAM External Address Multiplexer Select. AMuxCAS controls the select logic on an external multiplexer. If AMuxCAS is low, the multiplexer should select the row address for the DRAM and when AMuxCAS is 1, the multiplexer should select the column address.
BootW	23	I	Boot-up ROM Width Select. BootW is sampled before and after the RESET pin is active to determine the width of the boot-up ROM. If this pin is tied to logic 0 when sampled on reset, an 8-bit boot width is assumed. If BootW is tied to 1, a 32-bit boot width is assumed. For 16-bit boot widths, this pin should be tied to the RESET pin.
BusReq/ DMADXFER	123	O	Bus Request. While HoldAck is active, BusReq is active when the 403GB has a bus operation pending and needs to regain control of the bus. DMA Data Transfer. When HoldAck is not active, DMADXFER indicates a valid data transfer cycle. For DMA use, DMADXFER controls burst-mode fly-by DMA transfers between memory and peripherals. DMADXFER is not meaningful unless a DMA Acknowledge signal (DMAA0:DMAA1) is active. For transfer rates slower than one transfer per cycle, DMADXFER is active for one cycle when one transfer is complete and the next one starts. For transfer rates of one transfer per cycle, DMADXFER remains active throughout the transfer.
CAS0	116	O	DRAM Column Address Select 0. CAS0 is used with byte 0 of all DRAM banks.
CAS1	117	O	DRAM Column Address Select 1. CAS1 is used with byte 1 of all DRAM banks.
CAS2	118	O	DRAM Column Address Select 2. CAS2 is used with byte 2 of all DRAM banks.

Table 4. 403GB Signal Descriptions (Continued)

Signal Name	Pin	I/O Type	Function
$\overline{\text{CAS3}}$	119	O	DRAM Column Address Select 3. $\overline{\text{CAS3}}$ is used with byte 3 of all DRAM banks.
$\overline{\text{CINT}}$	34	I	Critical Interrupt. To initiate a critical interrupt, the user must maintain a logic 0 on the $\overline{\text{CINT}}$ pin for a minimum of one SysClk clock cycle followed by a logic 1 on the $\overline{\text{CINT}}$ pin for at least one SysClk cycle.
$\overline{\text{CS0}}$	8	O	SRAM Chip Select 0. Bank register 0 controls an SRAM bank, $\overline{\text{CS0}}$ is the chip select for that bank.
$\overline{\text{CS1}}$	5	O	SRAM Chip Select 1. Same function as $\overline{\text{CS0}}$ but controls bank 1.
$\overline{\text{CS2}}$	4	O	SRAM Chip Select 2. Same function as $\overline{\text{CS0}}$ but controls bank 2.
$\overline{\text{CS3}}$	3	O	SRAM Chip Select 3. Same function as $\overline{\text{CS0}}$ but controls bank 3.
$\overline{\text{CS6/RAS1}}$	2	O	Chip Select 6/ DRAM Row Address Select 1. When bank register 6 is configured to control an SRAM bank, $\overline{\text{CS6/RAS1}}$ functions as a chip select. When bank register 6 is configured to control a DRAM bank, $\overline{\text{CS6/RAS1}}$ is the row address select for that bank.
$\overline{\text{CS7/RAS0}}$	128	O	Chip Select 7/ DRAM Row Address Select 0. Same function as $\overline{\text{CS6/RAS1}}$ but controls bank 7.
D0	36	I/O	Data bus bit 0 (Most significant bit)
D1	37	I/O	Data bus bit 1
D2	39	I/O	Data bus bit 2
D3	40	I/O	Data bus bit 3
D4	41	I/O	Data bus bit 4
D5	43	I/O	Data bus bit 5
D6	44	I/O	Data bus bit 6
D7	45	I/O	Data bus bit 7
D8	46	I/O	Data bus bit 8
D9	47	I/O	Data bus bit 9
D10	48	I/O	Data bus bit 10

Table 4. 403GB Signal Descriptions (Continued)

Signal Name	Pin	I/O Type	Function
D11	49	I/O	Data bus bit 11
D12	50	I/O	Data bus bit 12
D13	53	I/O	Data bus bit 13
D14	54	I/O	Data bus bit 14
D15	57	I/O	Data bus bit 15
D16	58	I/O	Data bus bit 16
D17	59	I/O	Data bus bit 17
D18	60	I/O	Data bus bit 18
D19	61	I/O	Data bus bit 19
D20	62	I/O	Data bus bit 20
D21	63	I/O	Data bus bit 21
D22	64	I/O	Data bus bit 22
D23	67	I/O	Data bus bit 23
D24	68	I/O	Data bus bit 24
D25	69	I/O	Data bus bit 25
D26	70	I/O	Data bus bit 26
D27	71	I/O	Data bus bit 27
D28	72	I/O	Data bus bit 28
D29	73	I/O	Data bus bit 29
D30	74	I/O	Data bus bit 30
D31	75	I/O	Data bus bit 31
$\overline{\text{DMAA0}}$	9	O	DMA Channel 0 Acknowledge. $\overline{\text{DMAA0}}$ has an active level when a transaction is taking place between the 403GB and a peripheral.
$\overline{\text{DMAA1}}$	10	O	DMA Channel 1 Acknowledge. See description of $\overline{\text{DMAA0}}$

Table 4. 403GB Signal Descriptions (Continued)

Signal Name	Pin	I/O Type	Function
$\overline{\text{DMAR0}}$	15	I	DMA Channel 0 Request. When the 403GB is the bus master, external devices request a DMA transfer on channel 0 by putting a logic 0 on $\overline{\text{DMAR0}}$. When the 403GB HoldAck output is active and the 403GB is not the bus master, active requests on $\overline{\text{DMAR0}}$ are ignored until the 403GB becomes the bus master.
$\overline{\text{DMAR1}}$	16	I	DMA Channel 1 Request. See description of $\overline{\text{DMAR0}}$
$\overline{\text{DRAMOE}}$	125	O	DRAM Output Enable. $\overline{\text{DRAMOE}}$ has an active level when either the 403GB or an external bus master is reading from a DRAM bank. This signal enables the selected DRAM bank to drive the data bus.
$\overline{\text{DRAMWE}}$	126	O	DRAM Write Enable. $\overline{\text{DRAMWE}}$ has an active level when either the 403GB or an external bus master is writing to a DRAM bank.
$\overline{\text{EOT0/TC0}}$	112	I/O	End of Transfer 0 / Terminal Count 0. The function of the $\overline{\text{EOT0/TC0}}$ is controlled via the $\overline{\text{EOT/TC}}$ bit in the DMA Channel 0 Control Register. When $\overline{\text{EOT0/TC0}}$ is configured as an End of Transfer pin, external users may stop a DMA transfer by placing a logic 0 on this input pin. When configured as a Terminal Count pin, the 403GB signals the completion of a DMA transfer by placing a logic 0 on this pin.
$\overline{\text{EOT1/TC1}}$	113	I/O	End of Transfer1 / Terminal Count 1. See description of $\overline{\text{EOT0/TC0}}$
Error	124	O	System Error. Error goes to a logic 1 whenever a machine check error is detected in the 403GB. The Error pin then remains a logic 1 until the machine check error is cleared in the Exception Syndrome Register and/or Bus Error Syndrome Register.
GND	1		Ground. All ground pins must be used.
	6		Ground. All ground pins must be used.
	20		Ground. All ground pins must be used.
	38		Ground. All ground pins must be used.
	51		Ground. All ground pins must be used.
	55		Ground. All ground pins must be used.
	66		Ground. All ground pins must be used.

Table 4. 403GB Signal Descriptions (Continued)

Signal Name	Pin	I/O Type	Function
GND	76		Ground. All ground pins must be used.
	84		Ground. All ground pins must be used.
	100		Ground. All ground pins must be used.
	115		Ground. All ground pins must be used.
	120		Ground. All ground pins must be used.
$\overline{\text{Halt}}$	22	I	Halt from external debugger, active low.
HoldAck	122	O	Hold Acknowledge. HoldAck outputs a logic 1 when the 403GB relinquishes its external buses to an external bus master. The external bus master uses the HoldReq pin to request use of the 403GB buses.
HoldReq	25	I	Hold Request. External bus masters can request the 403GB bus by placing a logic1 on this pin. When the 403GB HoldAck pin is logic 1, the 403GB has relinquished its address, data and control buses to the external master. The external bus master relinquishes the buses to the 403GB by deasserting HoldReq. The 403GB then deasserts HoldAck during the following cycle.
INT0/TestC	29	I	Interrupt 0. While $\overline{\text{Reset}}$ is not active, INT0 is an interrupt input to the 403GB and users may program the pin to be either edge-triggered or level triggered and may also program the polarity to be active high or active low. The IOCR contains the bits necessary to program the trigger type and polarity. TestC. Reserved for manufacturing test during the reset interval. While $\overline{\text{Reset}}$ is active, this signal should be tied low for normal operation.
INT1/TestD	30	I	Interrupt 1 / TestD. See description of INT0/TestC.
INT2	31	I	Interrupt 2. INT2 is an interrupt input to the 403GB and users may program the pin to be either edge-triggered or level triggered and may also program the polarity to be active high or active low. The IOCR contains the bits necessary to program the trigger type and polarity.
INT3	32	I	Interrupt 3. See description of INT2
INT4	33	I	Interrupt 4. See description of INT2

Table 4. 403GB Signal Descriptions (Continued)

Signal Name	Pin	I/O Type	Function
IVR	35		Interface voltage reference. When connected to 3.3V supply, allows the device to interface to an exclusively 3V system. When connected to 5V supply, allows the device to interface to 5V or mixed 3V/5V system. If any input or output connects to 5V system, this pin must be connected to 5V supply.
\overline{OE} / XSize1	110	O/I	Output Enable / External Master Transfer Size 1. When the 403GB is bus master, \overline{OE} enables the selected SRAMs to drive the data bus. The timing parameters of \overline{OE} relative to the chip select, \overline{CS} , are programmable via bits in the 403GB bank registers. When the 403GB is not bus master, \overline{OE} / XSize1 is used as one of two external transfer size input bits, XSize0:1.
Ready	24	I	Ready. Ready is used to insert externally generated (device-paced) wait states into bus transactions. The Ready pin is enabled via the Ready Enable bit in 403GB bank registers.
\overline{Reset}	78	I/O	Reset. A logic 0 input placed on this pin for eight SysClk cycles causes the 403GB to begin a system reset. When a system reset is internally invoked, the \overline{Reset} pin becomes a logic 0 output for three SysClk cycles, and the system must maintain \overline{Reset} active for a total of eight cycles minimum.
R/\overline{W}	111	I/O	Read / Write. When the 403GB is bus master, R/\overline{W} is an output which is high when data is read from memory and low when data is written to memory. R/\overline{W} is driven with the same timings as the address bus. When the 403GB is not bus master, R/\overline{W} is an input from the external bus master which indicates the direction of data transfer.
SysClk	26	I	SysClk is the processor system clock input. SysClk supports a 50/50 duty cycle clock input at the rated chip frequency.
TCK	18	I	JTAG Test Clock Input. TCK is the clock source for the 403GB test access port (TAP). The maximum clock rate into the TCK pin is one half of the processor SysClk clock rate.
TDI	13	I	Test Data In. The TDI is used to input serial data into the TAP. When the TAP enables the use of the TDI pin, the TDI pin is sampled on the rising edge of TCK and this data is input to the selected TAP shift register.
TDO	12	O	Test Data Output. TDO is used to transmit data from the 403GB TAP. Data from the selected TAP shift register is shifted out on TDO.
TestA	27	I	Reserved for manufacturing test. Tied low for normal operation.

Table 4. 403GB Signal Descriptions (Continued)

Signal Name	Pin	I/O Type	Function
TestB	28	I	Reserved for manufacturing test. Tied high for normal operation.
TMS	21	I	Test Mode Select. The TMS pin is sampled by the TAP on the rising edge of TCK. The TAP state machine uses the TMS pin to determine the mode in which the TAP operates.
V _{DD}	7		Power. All power pins must be connected to 3.3V supply.
	19		Power. All power pins must be connected to 3.3V supply.
	42		Power. All power pins must be connected to 3.3V supply.
	52		Power. All power pins must be connected to 3.3V supply.
	56		Power. All power pins must be connected to 3.3V supply.
	65		Power. All power pins must be connected to 3.3V supply.
	77		Power. All power pins must be connected to 3.3V supply.
	85		Power. All power pins must be connected to 3.3V supply.
	91		Power. All power pins must be connected to 3.3V supply.
	105		Power. All power pins must be connected to 3.3V supply.
	114		Power. All power pins must be connected to 3.3V supply.
	121		Power. All power pins must be connected to 3.3V supply.
$\overline{\text{WBE0}} / \text{A6}$	106	O/I	Write Byte Enable 0 / Address Bus Bit 6. When the 403GB is bus master, the write byte enable outputs, $\overline{\text{WBE0:3}}$, select the active byte(s) in a memory write access. For 8-bit memory regions, $\overline{\text{WBE2}}$ and $\overline{\text{WBE3}}$ become address bits 30 and 31 and $\overline{\text{WBE0}}$ is the write-enable line. For 16-bit memory regions, $\overline{\text{WBE2:WBE3}}$ are address bits A30:A31 and $\overline{\text{WBE0}}$ and $\overline{\text{WBE1}}$ are the high byte and low write enables, respectively. For 32-bit memory regions, $\overline{\text{WBE0:3}}$ are write byte enables for bytes 0-3 on the data bus, respectively. When the 403GB is not bus master, $\overline{\text{WBE0:1}}$ are used as the A6:7 inputs (for bank register selection) and $\overline{\text{WBE2:3}}$ are used as the A30:31 inputs (for byte selection and page crossing detection).
$\overline{\text{WBE1}} / \text{A7}$	107	O/I	Write Byte Enable 1 / Address Bus Bit 7. See description of $\overline{\text{WBE0}} / \text{A6}$ above.

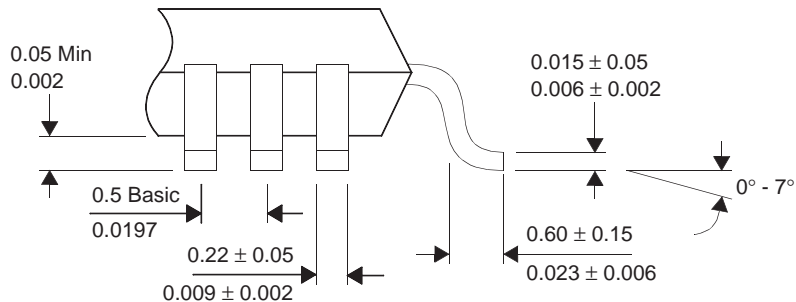
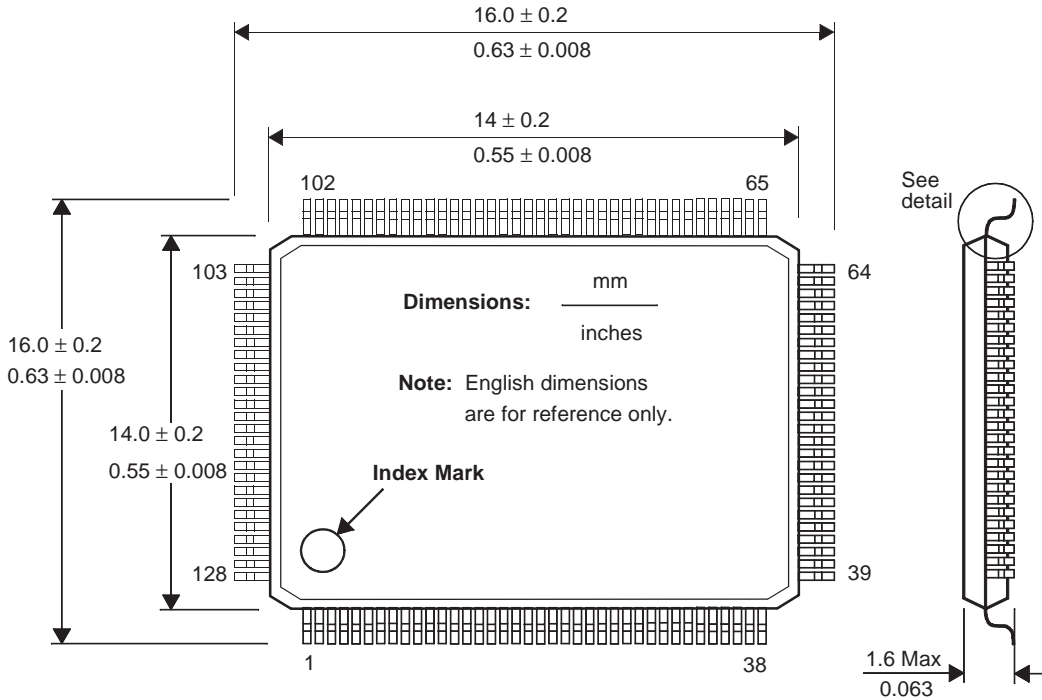
Table 4. 403GB Signal Descriptions (Continued)

Signal Name	Pin	I/O Type	Function
$\overline{\text{WBE2}}$ / A30	108	O/I	Write Byte Enable 2 / Address Bus Bit 30. See description of $\overline{\text{WBE0}}$ / A6 above
$\overline{\text{WBE3}}$ / A31	109	O/I	Write Byte Enable 3 / Address Bus Bit 31. See description of $\overline{\text{WBE0}}$ / A6 above
XACK	11	O	When the 403GB HoldAck output is active and the 403GB is not bus master, $\overline{\text{XACK}}$ is an output from the 403GB which has an active level when data is valid during an external bus master transaction.
XREQ	17	I	When the 403GB is not the bus master, the external bus master places a logic 0 on $\overline{\text{XREQ}}$ when the 403GB HoldAck is active and external bus master wishes to initiate a transfer to the DRAM controlled by the 403GB DRAM controller.
XSize0	14	I	External Master Transfer Size 0. When the 403GB is not bus master, XSize0 is used as one of two external transfer size input bits, XSize0:1.

Table 5. Signals Ordered by Pin Number

Pin	Signal Names	Pin	Signal Names	Pin	Signal Names	Pin	Signal Names
1	GND	33	INT4	65	V _{DD}	97	A23
2	$\overline{\text{CS6/RAS1}}$	34	$\overline{\text{CINT}}$	66	GND	98	A24
3	$\overline{\text{CS3}}$	35	IVR	67	D23	99	A25
4	$\overline{\text{CS2}}$	36	D0	68	D24	100	GND
5	$\overline{\text{CS1}}$	37	D1	69	D25	101	A26
6	GND	38	GND	70	D26	102	A27
7	V _{DD}	39	D2	71	D27	103	A28
8	$\overline{\text{CS0}}$	40	D3	72	D28	104	A29
9	$\overline{\text{DMAA0}}$	41	D4	73	D29	105	V _{DD}
10	$\overline{\text{DMAA1}}$	42	V _{DD}	74	D30	106	$\overline{\text{WBE0}} / \text{A6}$
11	XACK	43	D5	75	D31	107	$\overline{\text{WBE1}} / \text{A7}$
12	TDO	44	D6	76	GND	108	$\overline{\text{WBE2}} / \text{A30}$
13	TDI	45	D7	77	V _{DD}	109	$\overline{\text{WBE3}} / \text{A31}$
14	XSize0	46	D8	78	$\overline{\text{Reset}}$	110	$\overline{\text{OE}} / \text{XSize1}$
15	$\overline{\text{DMAR0}}$	47	D9	79	A8	111	R/ $\overline{\text{W}}$
16	$\overline{\text{DMAR1}}$	48	D10	80	A9	112	$\overline{\text{EOT0/TC0}}$
17	XREQ	49	D11	81	A10	113	$\overline{\text{EOT1/TC1}}$
18	TCK	50	D12	82	A11	114	V _{DD}
19	V _{DD}	51	GND	83	A12	115	GND
20	GND	52	V _{DD}	84	GND	116	$\overline{\text{CAS0}}$
21	TMS	53	D13	85	V _{DD}	117	$\overline{\text{CAS1}}$
22	$\overline{\text{Halt}}$	54	D14	86	A13	118	$\overline{\text{CAS2}}$
23	BootW	55	GND	87	A14	119	$\overline{\text{CAS3}}$
24	Ready	56	V _{DD}	88	A15	120	GND
25	HoldReq	57	D15	89	A16	121	V _{DD}
26	SysClk	58	D16	90	A17	122	HoldAck
27	TestA	59	D17	91	V _{DD}	123	BusReq/ $\overline{\text{DMADXFER}}$
28	TestB	60	D18	92	A18	124	Error
29	INT0/TestC	61	D19	93	A19	125	$\overline{\text{DRAMOE}}$
30	INT1/TestD	62	D20	94	A20	126	$\overline{\text{DRAMWE}}$
31	INT2	63	D21	95	A21	127	AMuxCAS
32	INT3	64	D22	96	A22	128	$\overline{\text{CS7/RAS0}}$

TQFP Mechanical Drawing (Top View)



Package Thermal Specifications

The 403GB is designed to operate within the case temperature range from 0°C to 120°C. Thermal resistance values for the 128 TQFP are shown in Table 6:

Table 6. Thermal Resistance (°C/Watt)

Parameter	Airflow-ft/min (m/sec)		
	0 (0)	100 (0.51)	200 (1.02)
θ_{JC} Junction to case	2	2	2
θ_{CA} Case to ambient (without heatsink)	37	29	28

Notes:

1. Case temperature T_{mC} is measured at top center of case surface with device soldered to circuit board.
2. $T_{mA} = T_{mC} - P \times \theta_{CA}$, where T_{mA} is ambient temperature.
3. $T_{mCMax} = T_{mJMax} - P \times \theta_{JC}$, where T_{mJMax} is maximum junction temperature and P is power consumption.
4. The above assumes that the chip is mounted on a card with at least one signal and two power planes.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

The absolute maximum ratings in Table 7 below are stress ratings only. Operation at or beyond these maximum ratings may cause permanent damage to the device.

Table 7. 403GB Maximum Ratings

Parameter	Maximum Rating
Supply voltage with respect to GND	-0.5V to +3.8V
Voltage on other pins with respect to GND	-0.5V to +5.5V
Case temperature under bias	0°C to +120°C
Storage temperature	-65°C to +150°C

Operating Conditions

The 403GB can interface to either 3V or 5V technologies. The range for supply voltages is specified for five-percent margins relative to a nominal 3.3V power supply.

Device operation beyond the conditions specified in Table 8 is not recommended. Extended operation beyond the recommended conditions may affect device reliability:

Table 8. Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage	3.14	3.47	V
F_C	Clock frequency	0	28	MHz
T_{mC}	Case temperature under bias	-40	85	°C

Power Considerations

Power dissipation is determined by operating frequency, temperature, and supply voltage, as well as external source/sink current requirements. Typical power dissipation is 0.21 W at 28 MHz, $T_{mC} = 55^\circ\text{C}$, and $V_{CC} = 3.3\text{ V}$, with an average 10pF capacitive load.

Estimated supply current as a function of frequency is shown in the figure, "Supply Current vs Operating Frequency," on page 28. Derating curves are provided in the section, "Output Derating for Capacitance and Voltage," on page 25.

Recommended Connections

Power and ground pins should all be connected to separate power and ground planes in the circuit board to which the 403GB is mounted. Unused input pins must be tied inactive, either high or low.

The interface voltage reference (IVR) pin should be connected to 3.3V supply if all signal pins connecting to the 403GB pins operate at 3V levels. If any signal pin connecting to the 403GB operates with 5V levels, the IVR pin should be connected to 5V supply.

DC Specifications

Table 9. 403GB DC Characteristics

Symbol	Parameter	Min	Max	Units
V_{IL}	Input low voltage (except for SysClk)	GND - 0.1	0.8	V
V_{ILC}	Input low voltage for SysClk	GND - 0.1	0.8	V
V_{IH}	Input high voltage (except for SysClk) ¹	2.0	$V_{IVR} + 0.1$	V
V_{IHC}	Input high voltage for SysClk ¹	2.0	$V_{IVR} + 0.1$	V
V_{OL}	Output low voltage		0.4	V
V_{OH}	Output high voltage	2.4	V_{DD}	V
I_{OH}	Output high current		2	mA
I_{OL}	Output low current		4	mA
I_{LI}	Input leakage current		50	μ A
I_{LO}	Output leakage current		10	μ A
I_{CC}	Supply current ($I_{CC \text{ Max}}$ at F_C of 28MHz) ²		210	mA

Notes:

1. V_{IVR} is the interface voltage reference to which the IVR pin is tied to select either a 3.3V or 5V interface. For additional information, see "Recommended Connections," on page 19.
2. The 403GB drives its outputs to the level of V_{DD} and, when not driving, the 403GB outputs can be pulled up to 5V by other devices in a system if the 403GB IVR pin has been tied to 5V properly.
3. $I_{CC \text{ Max}}$ is measured at $T_{mC} = 85^\circ\text{C}$, worst-case recommended operating conditions for frequency and voltage as specified in Table 8 on page 19, and a capacitive load of 50 pF.

Table 10. 403GB I/O Capacitance

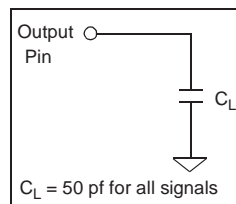
Symbol	Parameter	Min	Max	Units
C_{IN}	Input capacitance (except for SysClk)		5	pF
C_{INC}	Input capacitance for SysClk		25	pF
C_{OUT}	Output capacitance ¹		7	pF
$C_{I/O}$	I/O pin capacitance		8	pF

Note:

1. C_{Out} is specified as the load capacitance of a floating output in high impedance.

AC Specifications

Clock timing and switching characteristics are specified in accordance with recommended operating conditions in Table 8. AC specifications are tested at $V_{DD} = 3.14\text{V}$ and $T_J = 85^\circ\text{C}$ with the 50pF test load shown in the figure at right. Derating of outputs for capacitive loading is shown in the figure "Output Derating for Capacitance and Voltage," on page 25.



SysClk Timing

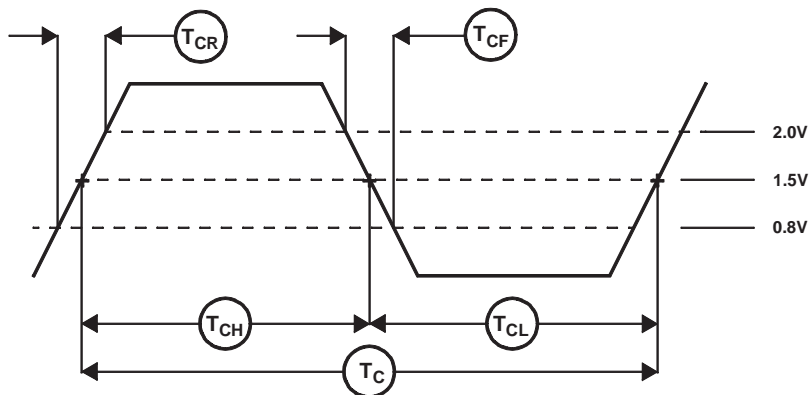


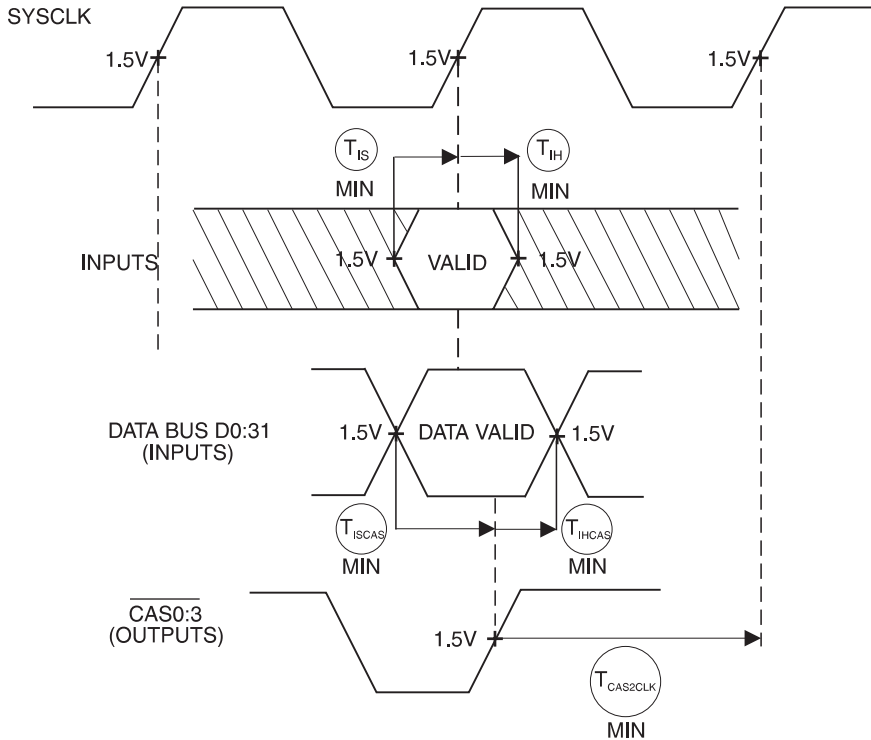
Table 11. 403GB System Clock Timing

Symbol	Parameter	Min	Max	Units
F_C	SysClk clock input frequency		28	MHz
T_C	SysClk clock period	36		ns
T_{CS}	Clock edge stability ¹		0.2	ns
T_{CH}	Clock input high time	16		ns
T_{CL}	Clock input low time	16		ns
T_{CR}	Clock input rise time ²	0.5	2.5	ns
T_{CF}	Clock input fall time ²	0.5	2.5	ns

Notes:

1. Cycle-to-cycle jitter allowed between any two edges.
2. Rise and fall times measured between 0.8V and 2.0V.

Input Setup and Hold Waveform



Notes:

1. The 403GB may be programmed to latch data from the data bus either on the rise of SysClk or the rise of $\overline{\text{CAS}}$. When the 403GB is programmed to latch data on $\overline{\text{CAS}}$, bit 26 of the I/O control register (IOCR) is set to 1.
2. $T_{\text{CAS2CLK}} \geq 15.5$ ns. The capacitive load on the $\overline{\text{CAS}}$ outputs must not delay the $\overline{\text{CAS}}$ low-to-high transition such that the period from the $\overline{\text{CAS}}$ rising edge to the next SysClk rising edge becomes less than 15.5 ns. The maximum value of $\overline{\text{CAS}}$ capacitive loading can be determined by using the output time for $\overline{\text{CAS}}$ from Table 16 on page 25, and applying the appropriate derating factor for your application. See the figure, "Output Derating for Capacitance and Voltage," on page 25.

Table 12. 403GB Synchronous Input Timings

Symbol	Parameter	Min	Max	Units
T_{IS}	Input setup time			
T_{IS1}	A6:11,A22:31	4		
T_{IS2}	D0:31 (to SysClk)	5		
T_{ISCAS}	D0:31 (to $\overline{\text{CAS}}$)	2		
T_{IS3}	HoldReq	4		ns
T_{IS4}	$\overline{\text{R}}/\overline{\text{W}}$	3		
T_{IS5}	Ready	6		
T_{IS6}	$\overline{\text{XReq}}$	5		
T_{IS7}	XSize0:1	5		

Table 12. 403GB Synchronous Input Timings

Symbol	Parameter	Min	Max	Units
T_{IH}	Input hold time			
T_{IH1}	A6:11,A22:31	2		
T_{IH2}	D0:31 (after SysClk)	2		
T_{IHCAS}	D0:31 (after \overline{CAS})	3		
T_{IH3}	HoldReq	2		ns
T_{IH4}	R/ \overline{W}	2		
T_{IH5}	Ready	2		
T_{IH6}	\overline{XReq}	2		
T_{IH7}	XSize0:1	2		
T_R, T_F	Input rise, fall time	0.5	2.5	ns

Note:

1. Data bus setup and hold times for DRAM \overline{CAS} mode are measured relative to \overline{CAS} deactivation.

Table 13. 403GB Asynchronous Input Timings

Symbol	Parameter	Min	Max	Units
T_{IS}	Input setup time			
T_{IS8}	\overline{CINT}	5		
T_{IS9}	$\overline{DMAR0:1}$	3		
T_{IS10}	$\overline{EOT0:1}$	3		ns
T_{IS11}	\overline{HALT}	3		
T_{IS12}	INT0:4	6		
T_{IS13}	\overline{Reset}	8		
T_{IH}	Input hold time			
T_{IH8}	\overline{CINT}	T_C		
T_{IH9}	$\overline{DMAR0:1}$	T_C		
T_{IH10}	$\overline{EOT0:1}$	T_C		ns
T_{IH11}	\overline{HALT}	T_C		
T_{IH12}	INT0:4	T_C		
T_{IH13}	\overline{Reset}	Note 1, 2		

Notes:

1. During a system-initiated reset, \overline{Reset} must be taken low for a minimum of eight SysClk cycles.
2. The BootW input has a maximum rise time requirement of 10 ns when it is tied to \overline{Reset} .
3. Input hold times are measured at 3.47V and $T_J = 10^\circ\text{C}$.

Output Delay and Float Timing Waveform

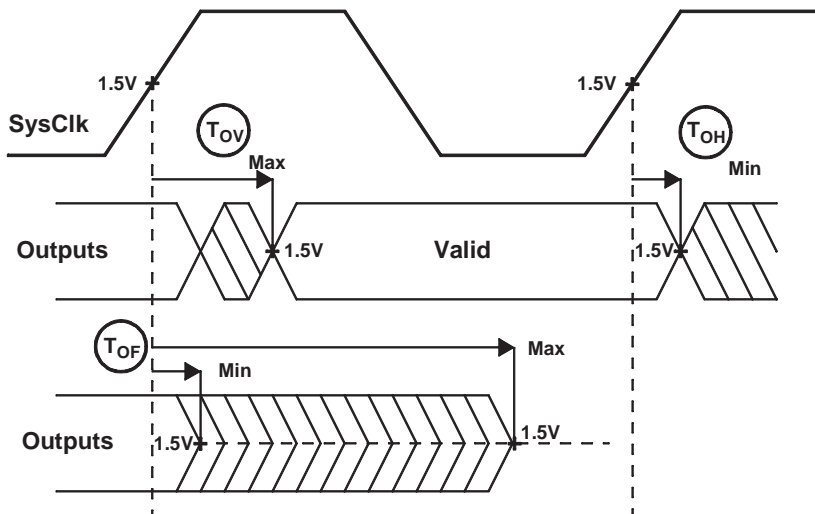


Table 14. 403GB Synchronous Output Timings

Symbol	Parameter		T_{OHMin}	T_{OVMax}	Units
T_{OH}, T_{OV}	Output hold, output valid time				
T_{OH1}, T_{OV1}	A8:31		4	15	ns
T_{OH2}, T_{OV2}	AMuxCAS		3	11	
T_{OH3}, T_{OV3}	BusReq		3	12	
T_{OH4}, T_{OV4}	CAS0:3		4	13	
T_{OH5}, T_{OV5}	$\overline{CS0:3,6:7}$		2	13	
T_{OH6}, T_{OV6}	D0:31		4	16	
T_{OH7}, T_{OV7}	$\overline{DMAA0:1}$		3	11	
T_{OH8}, T_{OV8}	$\overline{DMADXFER}$		3	13	
T_{OH9}, T_{OV9}	\overline{DRAMOE}		3	11	
T_{OH10}, T_{OV10}	\overline{DRAMWE}		2	10	
T_{OH11}, T_{OV11}	Error		4	14	
T_{OH12}, T_{OV12}	HoldAck		3	12	
T_{OH13}, T_{OV13}	\overline{OE}		3	11	
T_{OH14}, T_{OV14}	$\overline{RAS0:1}$		3	12	
T_{OH15}, T_{OV15}	$\overline{RAS0:3}$ (Early)		12	21	
T_{OH16}, T_{OV16}	\overline{Reset}		3	14	
T_{OH17}, T_{OV17}	$\overline{R/W}$		3	11	
T_{OH18}, T_{OV18}	$\overline{TC0:1}$		3	13	
T_{OH19}, T_{OV19}	$\overline{WBEO:3}$		3	12	
T_{OH20}, T_{OV20}	\overline{XAck}		3	13	

Table 14. 403GB Synchronous Output Timings

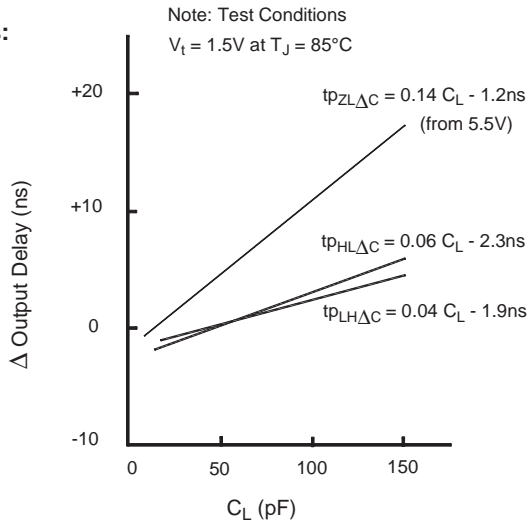
Symbol	Parameter		T_{OHMin}	T_{OVMax}	Units
T_{OF}	Output float time		Min	Max	
	T_{OF1}	A8:31	2	10	
	T_{OF2}	CS0:3,6:7	3	12	
	T_{OF3}	D0:31	3	11	ns
	T_{OF4}	\overline{OE}	3	12	
	T_{OF5}	\overline{Reset}	2	8	
	T_{OF6}	R/ \overline{W}	3	12	
	T_{OF7}	$\overline{WBE0:3}$	3	12	
T_{CAS}	Available \overline{CAS} access time		Min	Max	
	2-1-1-1 access mode (Note)		$0.5T_C - 2.5$		ns
	3-2-2-2 access mode (Note)		$1.5T_C - 2.5$		

Notes:

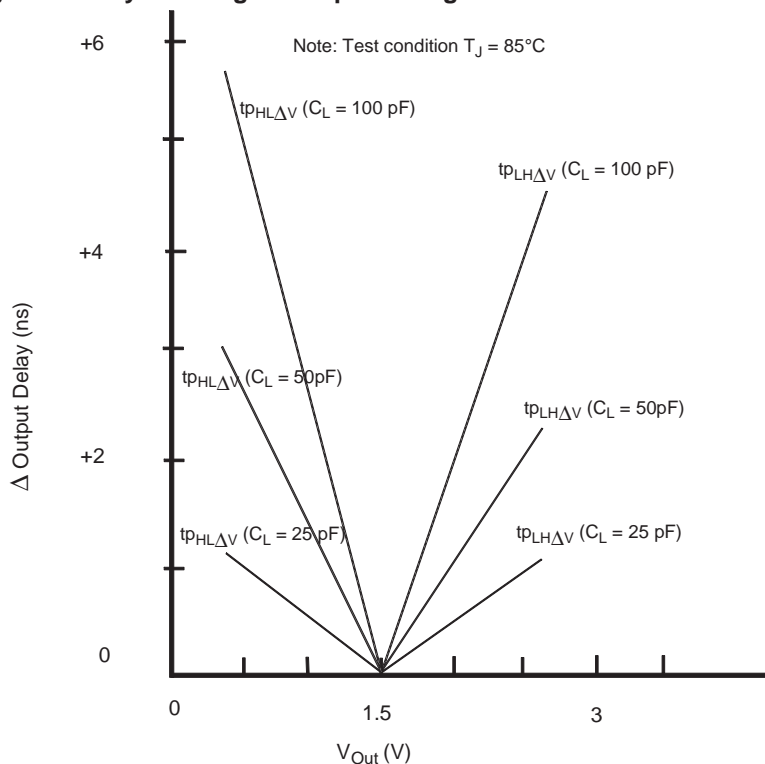
- For normal \overline{RAS} and \overline{CAS} timing, T_{OH} is relative to the rising edge of SysClk and T_{OV} is relative to the falling edge of SysClk. In early \overline{RAS} mode, T_{OV} is relative to the rising edge of SysClk. \overline{CAS} access time assumes a SysClk 50% duty cycle.
- In early \overline{RAS} mode, the \overline{RAS} output delay varies with the 403GB operating frequency. Use the following equation to determine the worst-case output delay for this signal: $T_{OVMax} = 12 \text{ ns} + T_c/4$; T_{OHMin} remains unchanged. Valid for T_c greater than 30 ns and less than 80 ns.
- When initiating a system reset, the 403GB pulls the \overline{Reset} output low for 2048 cycles minimum and then samples to determine when \overline{Reset} has gone low. Three cycles after \overline{Reset} has been sampled as low, the 403GB stops driving the \overline{Reset} output. At this time the system must hold \overline{Reset} low for five more cycles.
- Output times are measured with a standard 50 pF capacitive load, unless otherwise noted. Output hold times are measured at 3.47V and $T_J = 10^\circ\text{C}$.

Output Derating for Capacitance and Voltage**Output Propagation Delay Derating****Derating Equations for Output Delays:**

- $\Delta t_{pLH}(C_L, V) = t_{pLH\Delta C} + t_{pLH\Delta V}$
- $\Delta t_{pHL}(C_L, V) = t_{pHL\Delta C} + t_{pHL\Delta V}$
- $\Delta t_{pZL5V}(C_L, V) = t_{pZL\Delta C} + t_{pHL\Delta V}$



Output Propagation Delay Derating vs Output Voltage Level

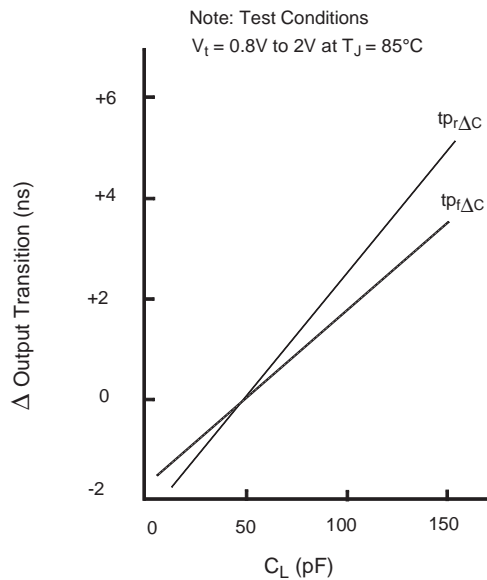


Output Rise and Fall Time Derating

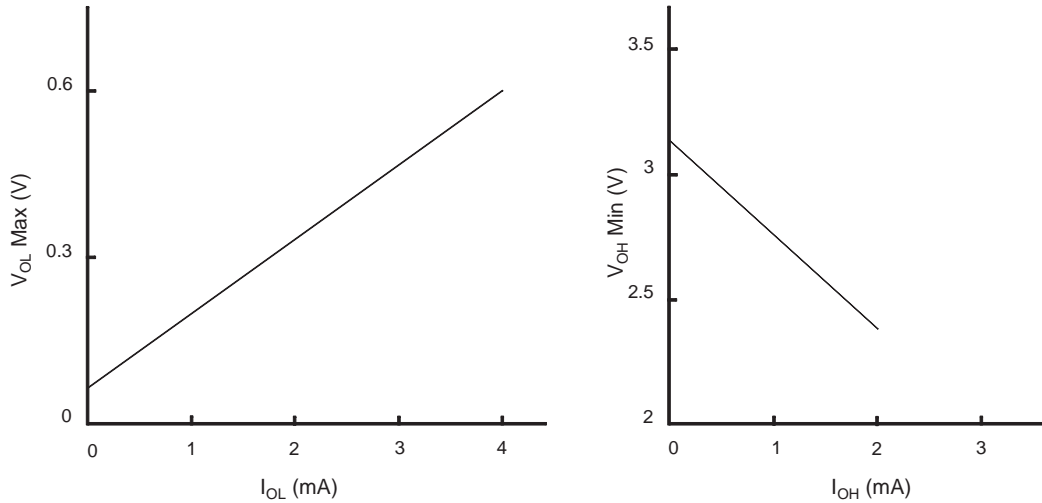
Derating Equations for Output Rise and Fall Times:

4. $t_R(C_L) = 2\text{ns} + t_{p_r\Delta C}$
5. $t_F(C_L) = 2.5\text{ns} + t_{p_f\Delta C}$

Output Transition Time Derating

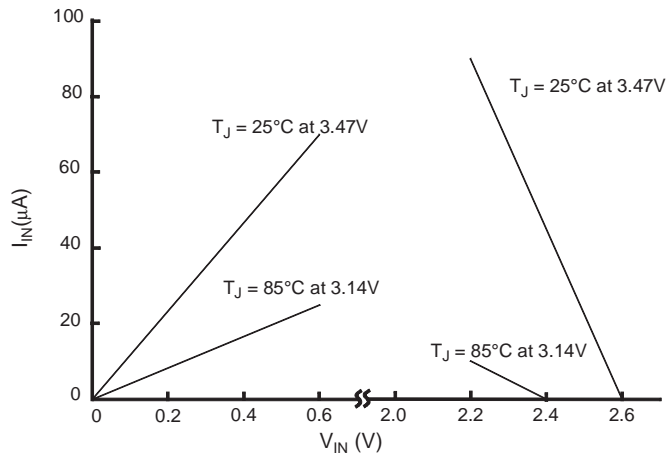


Output Voltage vs Output Current



Note: Test conditions 3.14V at $T_J = 85^\circ\text{C}$

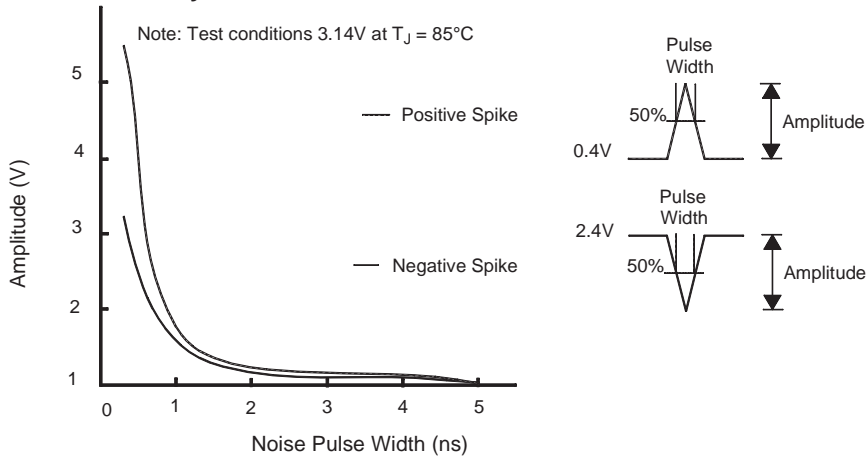
Receiver Input Voltage vs DC Input Current



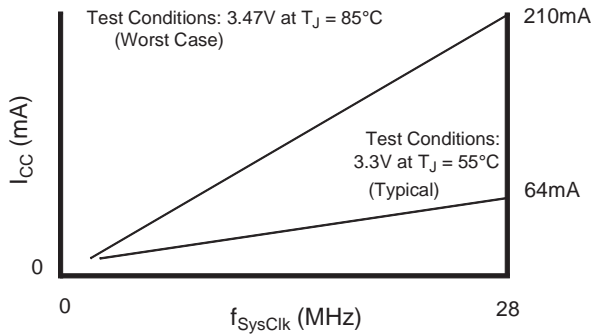
Note:

1. Applies to receivers for asynchronous inputs on pins 15-18, 21-25, 29-34, and 78, and synchronous inputs on pins 17 and 25.

Receiver Noise Sensitivity



Supply Current vs Operating Frequency



Reset and HoldAck

The following table summarizes the states of signals on output pins when $\overline{\text{Reset}}$ or HoldAck is active.

Table 15. Signal States During Reset or Hold Acknowledge

Signal Names	State When $\overline{\text{Reset}}$ Active	State When HoldAck Active
A8:29	Floating	Floating (set to input mode)
AMuxCAS	Inactive (low)	Operable (see note 1)
BusReq	Inactive (low)	Operable (see note 1)
$\overline{\text{CAS0:3}}$	Inactive (high)	Operable (see note 1)
$\overline{\text{CS0:3}}$	Floating	Floating
$\overline{\text{CS6:7/RAS1:0}}$	Floating	$\overline{\text{CS}}$ floating, $\overline{\text{RAS}}$ operable (see note 1)
D0:31	Floating	Floating (external master drives bus)
$\overline{\text{DMAA0:1}}$	Inactive (high)	Inactive (high)
$\overline{\text{XAck}}$	Inactive (high)	Operable (see note 1)
$\overline{\text{DRAMOE}}$	Inactive (high)	Operable (see note 1)
$\overline{\text{DRAMWE}}$	Inactive (high)	Operable (see note 1)
Error	Inactive (low)	Operable (see note 1)
HoldAck	Inactive (low)	Active
$\overline{\text{OE}}$	Floating	Floating (input for XSize1)
$\overline{\text{Reset}}$	Floating unless initiating system reset	Floating unless initiating system reset
$\text{R}/\overline{\text{W}}$	Floating	Floating (set to input)
$\overline{\text{TC0:1}}$	Floating (set to input)	Inactive (high)
TDO	Inactive (high)	Operable (see note 1)
$\overline{\text{WBE0:3}}$	Floating	Operable (inputs for A6:7, A30:31)

Note:

- Signal may be active while HoldAck is asserted, depending on the operation being performed by the 403GB.

BUS WAVEFORMS

The waveforms in this section represent external bus operations, including SRAM and DRAM accesses, DMA transfers, and external master operations.

Write Byte Enable Encoding

The 403GB provides four write byte enable signals ($\overline{\text{WBE0:3}}$) to support 8-, 16-, and 32-bit devices, as shown in Table 16. For an eight-bit memory region, $\overline{\text{WBE2:3}}$ are encoded as A30:31 and $\overline{\text{WBE0}}$ is the byte-enable line. For a 16-bit region, $\overline{\text{WBE0}}$ is the high-byte enable, $\overline{\text{WBE1}}$ is the low-byte enable and $\overline{\text{WBE2:3}}$ are encoded as A30:31. For a 32-bit region, address bits 8:29 select the word address and $\overline{\text{WBE0:3}}$ select data bytes 0:3, respectively.

Table 16. Write Byte Enable Encoding

8-Bit Bus Width	Transfer Size	Address	$\overline{\text{WBE0}} = \overline{\text{WE}}$	$\overline{\text{WBE1}} = 1$	$\overline{\text{WBE2}} = \text{A30}$	$\overline{\text{WBE3}} = \text{A31}$
	Byte	0	0	1	0	0
	Byte	1	0	1	0	1
	Byte	2	0	1	1	0
	Byte	3	0	1	1	1
16-Bit Bus Width	Transfer Size	Address	$\overline{\text{WBE0}} = \overline{\text{BHE}}$	$\overline{\text{WBE1}} = \overline{\text{BLE}}$	$\overline{\text{WBE2}} = \text{A30}$	$\overline{\text{WBE3}} = \text{A31}$
	Half-word	0	0	0	0	0
	Half-word	2	0	0	1	0
	Byte	0	0	1	0	0
	Byte	1	1	0	0	1
	Byte	2	0	1	1	0
	Byte	3	1	0	1	1
32-Bit Bus Width	Transfer Size	Address	$\overline{\text{WBE0}}$	$\overline{\text{WBE1}}$	$\overline{\text{WBE2}}$	$\overline{\text{WBE3}}$
	Word	0	0	0	0	0
	Half-word	0	0	0	1	1
	Half-word	2	1	1	0	0
	Byte	0	0	1	1	1
	Byte	1	1	0	1	1
	Byte	2	1	1	0	1
	Byte	3	1	1	1	0

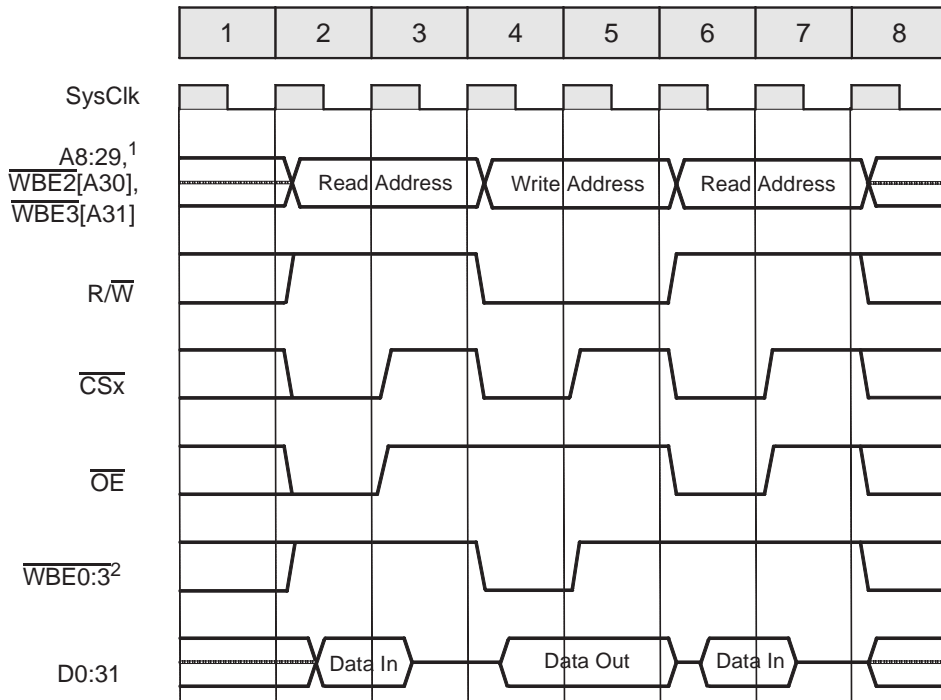
Address Bus Multiplexing

To support memories and I/O devices with differing configurations and bus widths, the 403GB provides an internally multiplexed address bus controlled by the BIU. Table 17 shows the multiplexed address outputs referenced by waveforms later in this section.

Table 17. Multiplexed Address Outputs

Address Pins	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29
Addr Bits Out in $\overline{\text{RAS}}$ Cycle	a6	a7	a8	a9	a10	a11	a12	a13	a12	a13	a14	a15	a16	a17	a18	a19	a20	a21	a22
Addr Bits Out in $\overline{\text{CAS}}$ Cycle	xx	a6	a7	a8	a9	a10	a11	a12	a21	a22	a23	a24	a25	a26	a27	a28	a29	a30	a31

SRAM Read-Write-Read with Zero Wait and One Hold



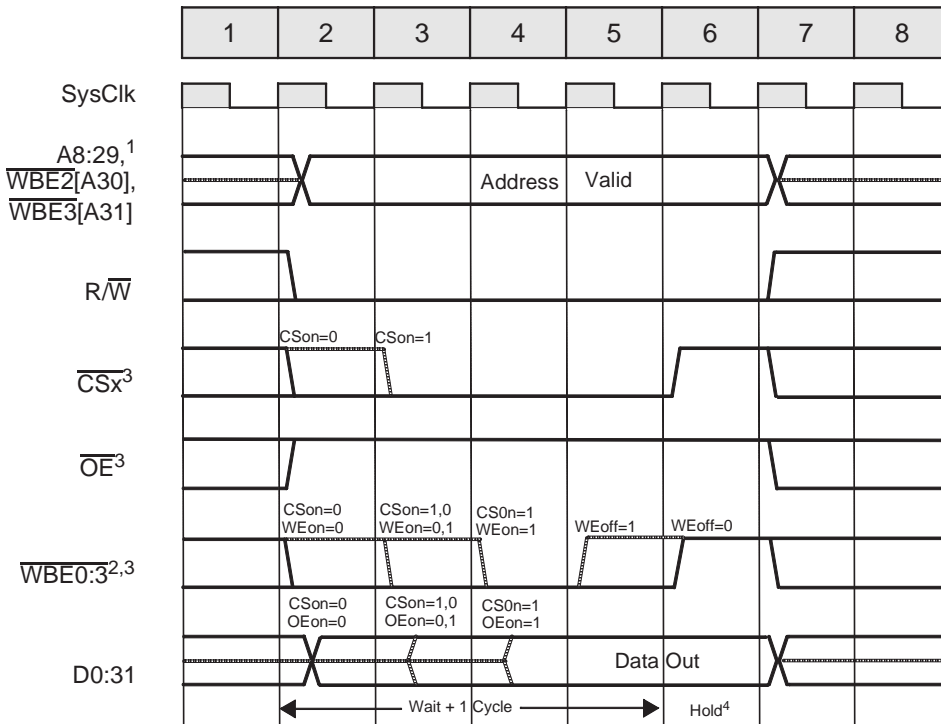
Bank Register Bit Settings

SLF	Burst Mode	Bus Width	Ready Enable	Wait States	CSon	OEon	WEon	WEoff	Hold
Bit 13	Bit 14	Bits 15:16	Bit 17	Bits 18:23	Bit 24	Bit 25	Bit 26	Bit 27	Bits 28:30
0 or 1	0	xx	0	00 0000	0	0	0	0	001

Notes:

1. WBE2:3 are address bits 30:31 if the bus width is programmed as byte or halfword.
2. See Table 18 on page 30 for WBE signal definitions based on bus width.

SRAM, ROM, or I/O Write Request with Wait and Hold



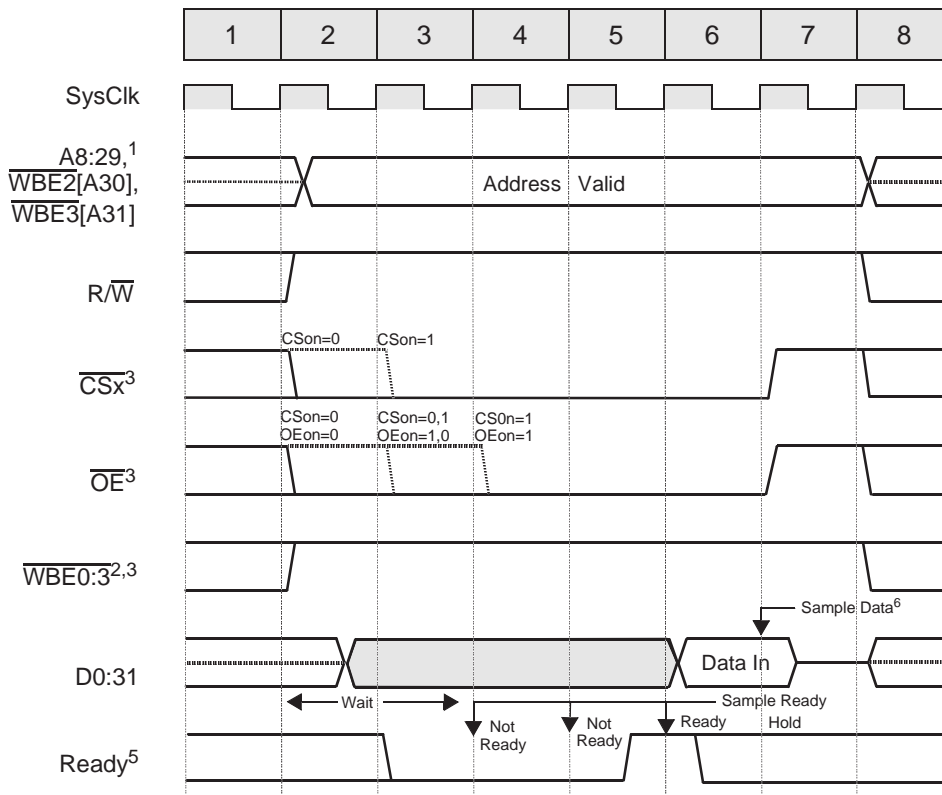
Bank Register Bit Settings

SLF	Burst Mode	Bus Width	Ready Enable	Wait States	CSon	OEon	WEon	WEoff	Hold
Bit 13	Bit 14	Bits 15:16	Bit 17	Bits 18:23	Bit 24	Bit 25	Bit 26	Bit 27	Bits 28:30
0 or 1	0	xx	0	00 0011	0 or 1	0 or 1	0 or 1	0 or 1	001

Notes:

1. WBE2:3 are address bits 30:31 if the bus width is programmed as byte or halfword.
2. See Table 18 for WBE signal definitions based on bus width.
3. 403GBWait must be programmed to a value $\geq (\text{CSon} + \text{WEon} + \text{WEoff})$ and $\geq (\text{CSon} + \text{OEon} + \text{WEoff})$. If $\text{Wait} > (\text{CSon} + \text{WEon})$ and $> (\text{CSon} + \text{OEon})$, then all signals retain the values shown in cycle 4 until the Wait time expires.
4. If Hold is programmed > 001 , all signals retain the values shown in cycle 6 until the Hold timer expires.

SRAM, ROM, or I/O Read Request, Wait Extended with Ready



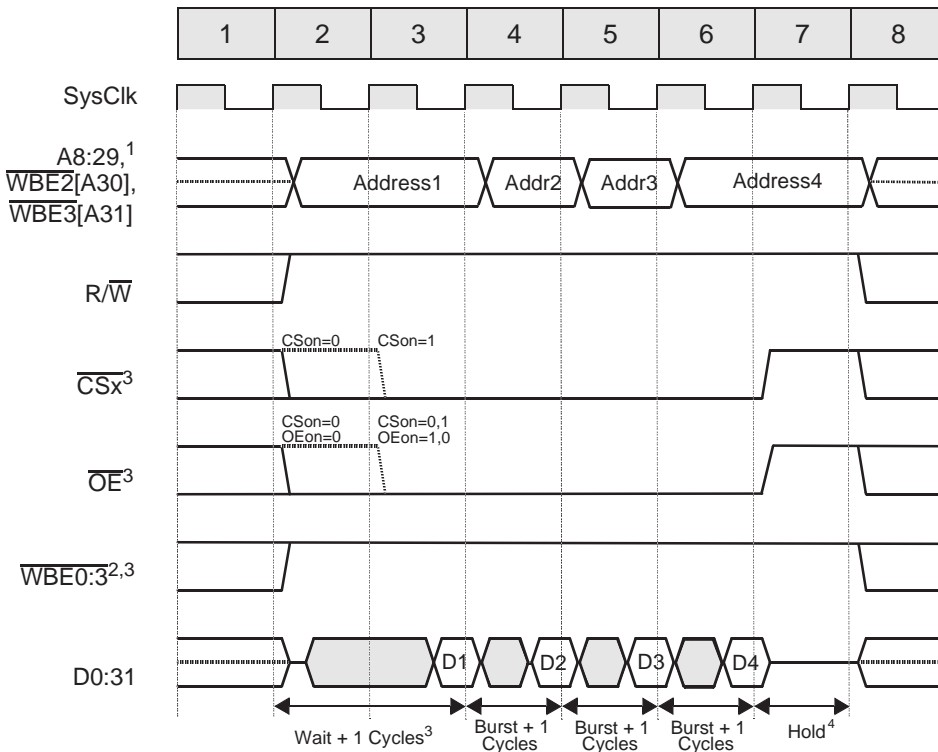
Bank Register Bit Settings

SLF	Burst Mode	Bus Width	Ready Enable	Wait States	CSon	OEon	WEon	WEoff	Hold
Bit 13	Bit 14	Bits 15:16	Bit 17	Bits 18:23	Bit 24	Bit 25	Bit 26	Bit 27	Bits 28:30
0 or 1	0	xx	1	00 0010	0 or 1	0 or 1	0 or 1	x	001

Notes:

1. WBE2:3 are address bits 30:31 if the bus width is programmed as byte or halfword.
2. See Table 18 on page 30 for WBE signal definitions based on bus width.
3. Wait must be programmed to a value \geq (CSon + OEon). If Wait > (CSon + OEon), then all signals will retain the values shown in cycle 4 until the Wait timer expires.
4. If Hold is programmed > 001, all 403GB output signals retain the values shown in cycle 7 until the Hold timer expires.
5. If Wait = 00 0000, the Ready input is ignored and single-cycle transfers occur. If Wait = 00 0001, Ready is sampled starting in cycle 2. If Wait > 00 0001, Ready is sampled starting after the Wait cycles have expired.
6. Data is captured 1 cycle after Ready is sampled active.

SRAM, ROM or I/O Burst Read with Wait and Hold



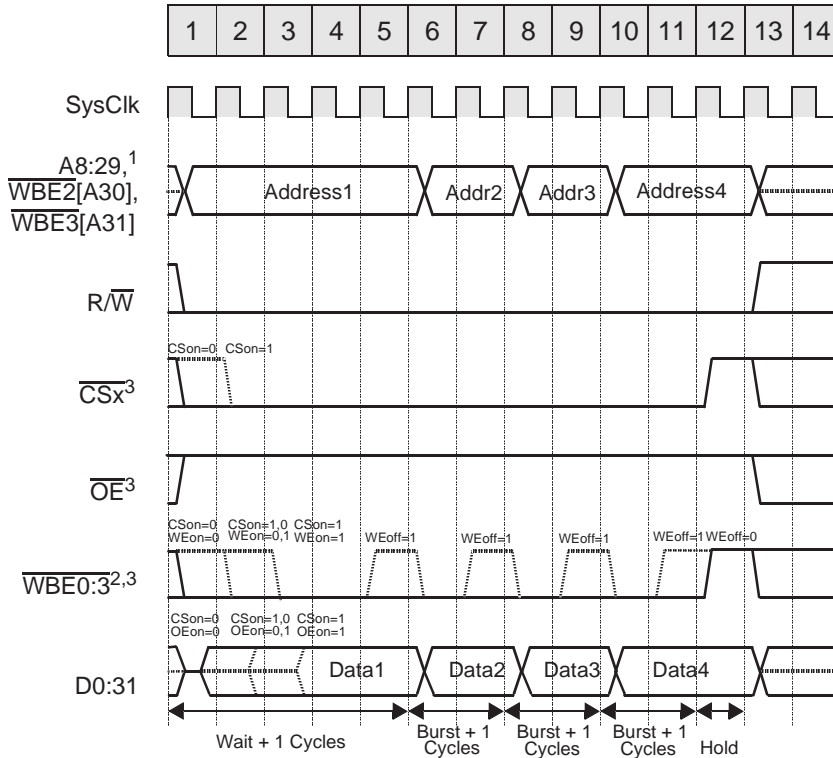
Bank Register Bit Settings

SLF	Burst Mode	Bus Width	Ready Enable	Wait States	Burst Wait	CSon	OEon	WEon	WEoff	Hold
Bit 13	Bit 14	Bits 15:16	Bit 17	Bits 18:21	Bits 22:23	Bit 24	Bit 25	Bit 26	Bit 27	Bits 28:30
0 or 1	1	xx	0	0001	00	0 or 1	0 or 1	x	x	001

Notes:

1. WBE2:3 are address bits 30:31 if the bus width is programmed as byte or halfword.
2. See Table 18 on page 30 for WBE signal definitions based on bus width.
3. Wait must be programmed to a value \geq (CSon + OEon). If Wait > (CSon + OEon), then all signals will retain the values shown in cycle 3 until the Wait timer expires.
4. If Hold is programmed > 001, all 403GB output signals retain the values shown in cycle 7 until the Hold timer expires.

SRAM, ROM or I/O Burst Write with Wait, Burst Wait, and Hold



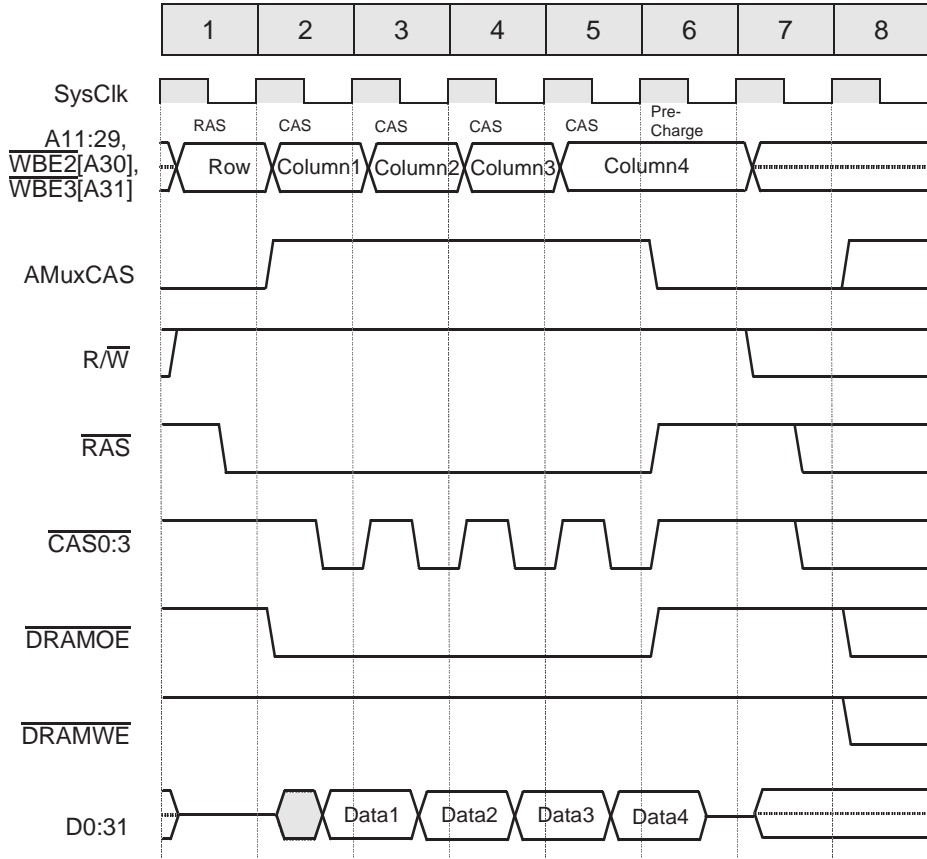
Bank Register Bit Settings

SLF	Burst Mode	Bus Width	Ready Enable	Wait States	Burst Wait	CSon	OEon	WEon	WEoff	Hold
Bit 13	Bit 14	Bits 15:16	Bit 17	Bits 18:21	Bits 22:23	Bit 24	Bit 25	Bit 26	Bit 27	Bits 28:30
0 or 1	1	xx	0	0100	01	0 or 1	0 or 1	0 or 1	0 or 1	001

Notes:

1. WBE2:3 are address bits 30:31 if the bus width is programmed as byte or halfword.
2. See Table 18 on page 30 for WBE signal definitions based on bus width.
3. Wait must be programmed to a value $\geq (\text{CSon} + \text{WEon} + \text{WEoff})$ and $\geq (\text{CSon} + \text{OEon} + \text{WEoff})$. If Wait $> (\text{CSon} + \text{WEon})$ and $> (\text{CSon} + \text{OEon})$, then all signals retain the values shown in cycle 3 until the Wait timer expires.
4. If Hold is programmed > 001 , all 403GB output signals retain the values shown in cycle 12 until the Hold timer expires.

DRAM 2-1-1-1 Page Mode Read

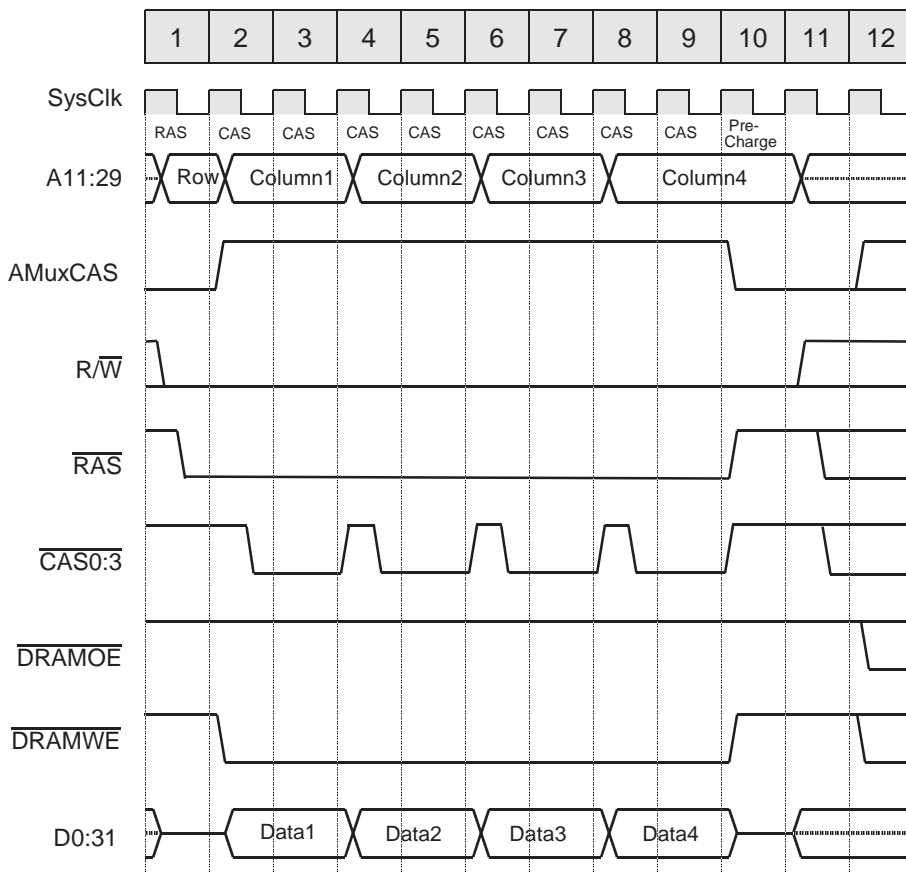


Bank Register Bit Settings

SLF	ERM	Bus Width	Ext Mux	RAS-to-CAS	Refresh Mode	Page Mode	First Access	Burst Access	Prechg Cycles	Refresh RAS	Refresh Rate
Bit 13	Bit 14	Bits 15:16	Bit 17	Bit 18	Bit 19	Bit 20	Bits 21:22	Bits 23:24	Bit 25	Bit 26	Bits 27:30
0 or 1	0	xx	x	0	0	1	00	00	0	x	xxxx

Notes:

1. For burst access, the address represented by Columns 1:4 does not necessarily indicate that they are in incremental address order. Typically, burst access is target word first.
2. If internal mux mode is used, address bits A11:29 represent address bits described in Table 17 on page 30.
3. During internal mux mode access, A8:10 retain their unmultiplexed values.
4. If external mux mode is used, A11:29 are unaffected and do not change between $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ cycles.
5. If bus width is programmed as byte or half-word, $\overline{\text{WBE2:3}}$ represent address bits A30:31 regardless of mux mode.
6. $\overline{\text{WBE0:1}}$ are always ones during DRAM transfers.

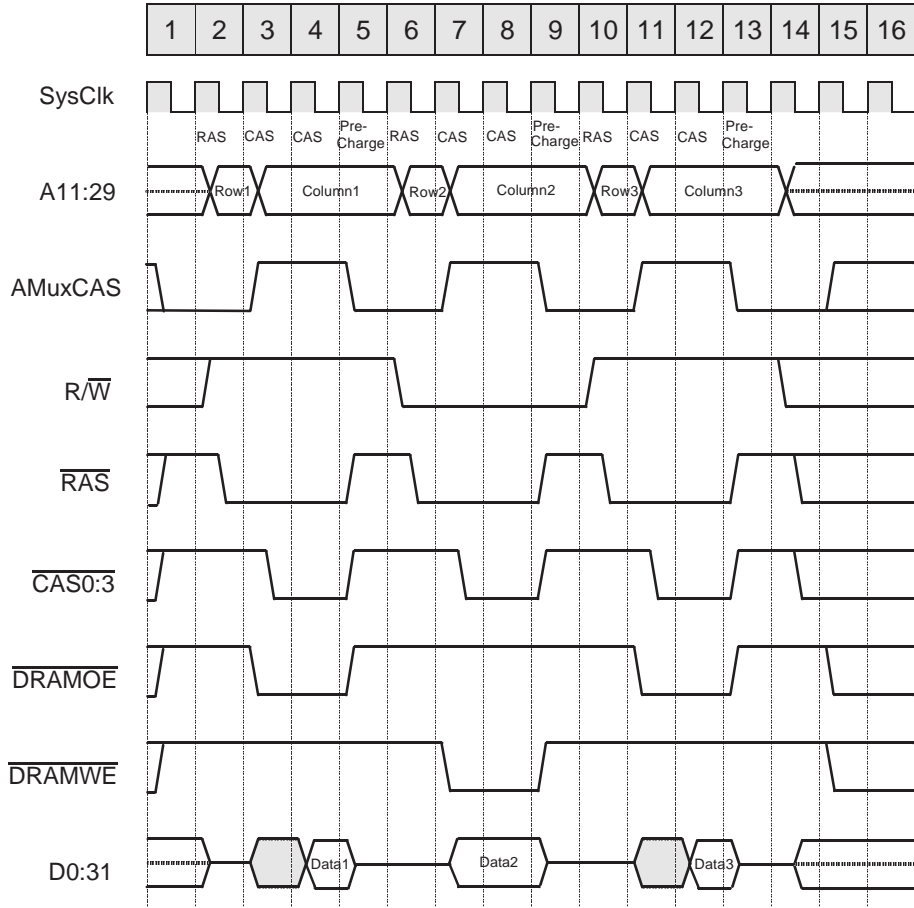
DRAM 3-2-2-2 Page Mode Write**Bank Register Bit Settings**

SLF	ERM	Bus Width	Ext Mux	RAS-to-CAS	Refresh Mode	Page Mode	First Access	Burst Access	Prechg Cycles	Refresh RAS	Refresh Rate
Bit 13	Bit 14	Bits 15:16	Bit 17	Bit 18	Bit 19	Bit 20	Bits 21:22	Bits 23:24	Bit 25	Bit 26	Bits 27:30
0 or 1	0	xx	x	0	0	1	01	01	0	x	xxxx

Notes:

1. For burst access, the addresses represented by Columns 1:4 do not necessarily indicate that they are in incremental address order. Typically, burst access is target word first.
2. If internal mux mode is used, address bits A11:29 represent address bits described in Table 17 on page 30.
3. During internal mux mode access, A8:10 retain their unmultiplexed values.
4. If external mux mode is used, A11:29 are unaffected and do not change between $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ cycles.
5. If bus width is programmed as byte or half-word, $\overline{\text{WBE2:3}}$ represent address bits A30:31 regardless of mux mode.
6. $\overline{\text{WBE0:1}}$ are always ones during DRAM transfers.

DRAM Read-Write-Read, One Wait



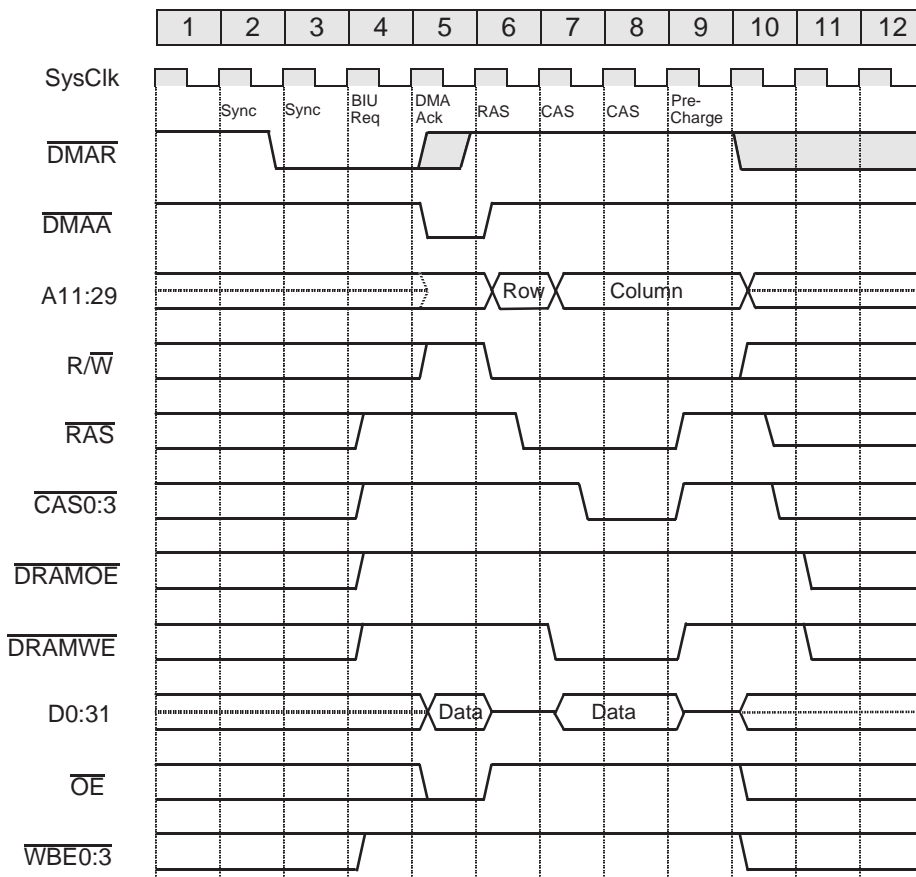
Bank Register Bit Settings

SLF	ERM	Bus Width	Ext Mux	RAS-to-CAS	Refresh Mode	Page Mode	First Access	Burst Access	Prechg Cycles	Refresh RAS	Refresh Rate
Bit 13	Bit 14	Bits 15:16	Bit 17	Bit 18	Bit 19	Bit 20	Bits 21:22	Bits 23:24	Bit 25	Bit 26	Bits 27:30
0 or 1	0	xx	x	0	0	0	01	xx	0	x	xxxx

Notes:

1. If internal mux mode is used, address bits A11:29 represent address bits described in Table 17 on page 30.
2. During internal mux mode access, A8:10 retain their unmultiplexed values.
3. If external mux mode is used, A11:29 are unaffected and do not change between $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ cycles.
4. If bus width is programmed as byte or half-word, $\overline{\text{WBE2:3}}$ represent address bits A30:31 regardless of mux mode.
5. $\overline{\text{WBE0:1}}$ are always ones during DRAM transfers.

DMA Buffered Single Transfer from Peripheral to 3-Cycle DRAM



Bank Register Bit Settings

SLF	ERM	Bus Width	Ext Mux	RAS-to-CAS	Refresh Mode	Page Mode	First Access	Burst Access	Prechg Cycles	Refresh RAS	Refresh Rate
Bit 13	Bit 14	Bits 15:16	Bit 17	Bit 18	Bit 19	Bit 20	Bits 21:22	Bits 23:24	Bit 25	Bit 26	Bits 27:30
0 or 1	0	10	0	0	0	0	01	xx	0	x	xxxx

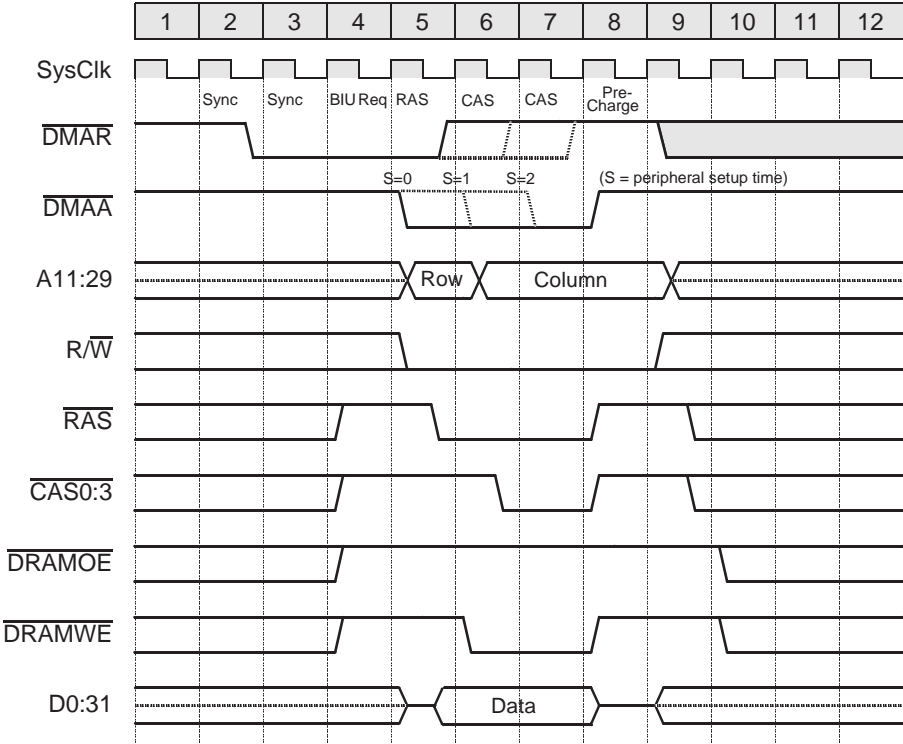
DMA Control Register Bit Settings

Transfer Direction	Transfer Width	Transfer Mode	Peripheral Setup	Peripheral Wait	Peripheral Hold
Bit 2	Bits 4:5	Bits 9:10	Bits 11:12	Bits 13:18	Bits 19:21
1	10	00	00	00 0000	000

Notes:

1. DMAR must be inactive in cycle 9 to guarantee a single transfer.
2. Peripheral data bus width must match DRAM bus width.
3. This waveform assumes that the internal address mux is used.
4. CAS0 is used for byte accesses, CAS0:1 for halfwords, and CAS0:3 for fullwords.

DMA Fly-By Single Transfer, Write to 3-Cycle DRAM



Bank Register Bit Settings

SLF	ERM	Bus Width	Ext Mux	RAS-to-CAS	Refresh Mode	Page Mode	First Access	Burst Access	Prechg Cycles	Refresh RAS	Refresh Rate
Bit 13	Bit 14	Bits 15:16	Bit 17	Bit 18	Bit 19	Bit 20	Bits 21:22	Bits 23:24	Bit 25	Bit 26	Bits 27:30
0 or 1	0	10	0	0	0	0	01	xx	0	x	xxxx

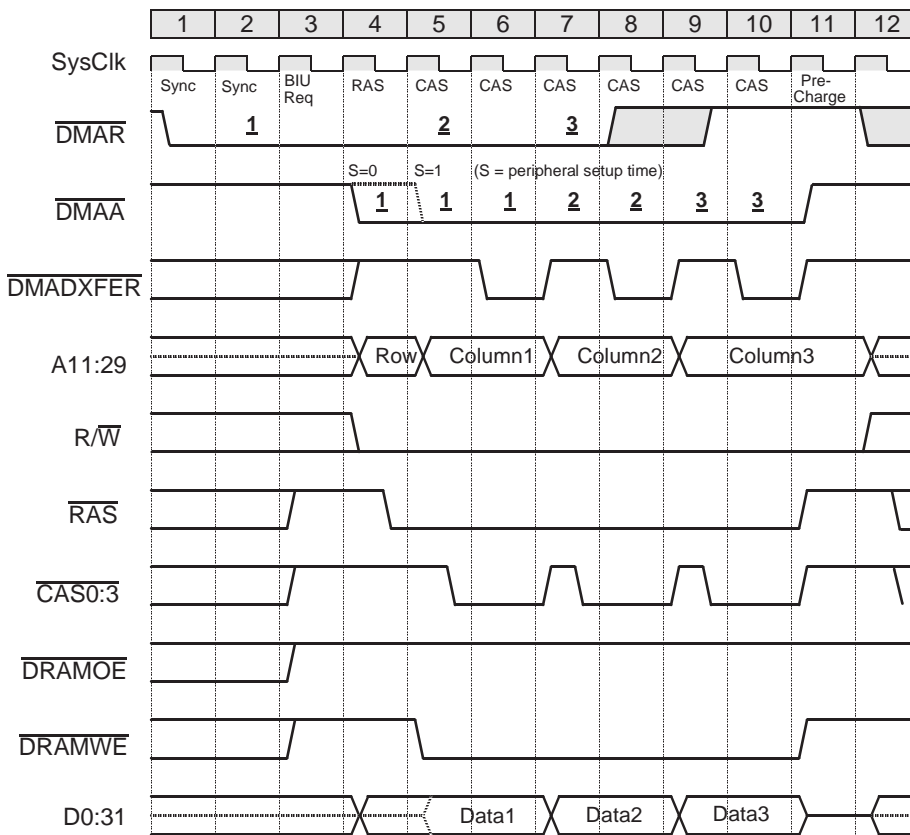
DMA Control Register Bit Settings

Transfer Direction	Transfer Width	Transfer Mode	Peripheral Setup	Peripheral Wait	Peripheral Hold
Bit 2	Bits 4:5	Bits 9:10	Bits 11:12	Bits 13:18	Bits 19-21
1	10	01	Note 3	xx xxxx	xxx

Notes:

1. $\overline{\text{DMAR}}$ must be inactive in cycle 7 (last $\overline{\text{DMAA}}$ cycle) to guarantee a single transfer.
2. Peripheral data bus width must match DRAM bus width.
3. See diagram for settings.
4. This waveform assumes that the internal address mux is used.
5. $\overline{\text{CAS0}}$ is used for byte accesses, $\overline{\text{CAS0:1}}$ for halfwords, and $\overline{\text{CAS0:3}}$ for fullwords.

DMA Fly-By Continuous Burst to 3-Cycle DRAM



Bank Register Bit Settings

SLF	ERM	Bus Width	Ext Mux	RAS-to-CAS	Refresh Mode	Page Mode	First Access	Burst Access	Prechg Cycles	Refresh RAS	Refresh Rate
Bit 13	Bit 14	Bits 15:16	Bit 17	Bit 18	Bit 19	Bit 20	Bits 21:22	Bits 23:24	Bit 25	Bit 26	Bits 27:30
0 or 1	0	10	0	0	0	1	01	01	0	x	xxxx

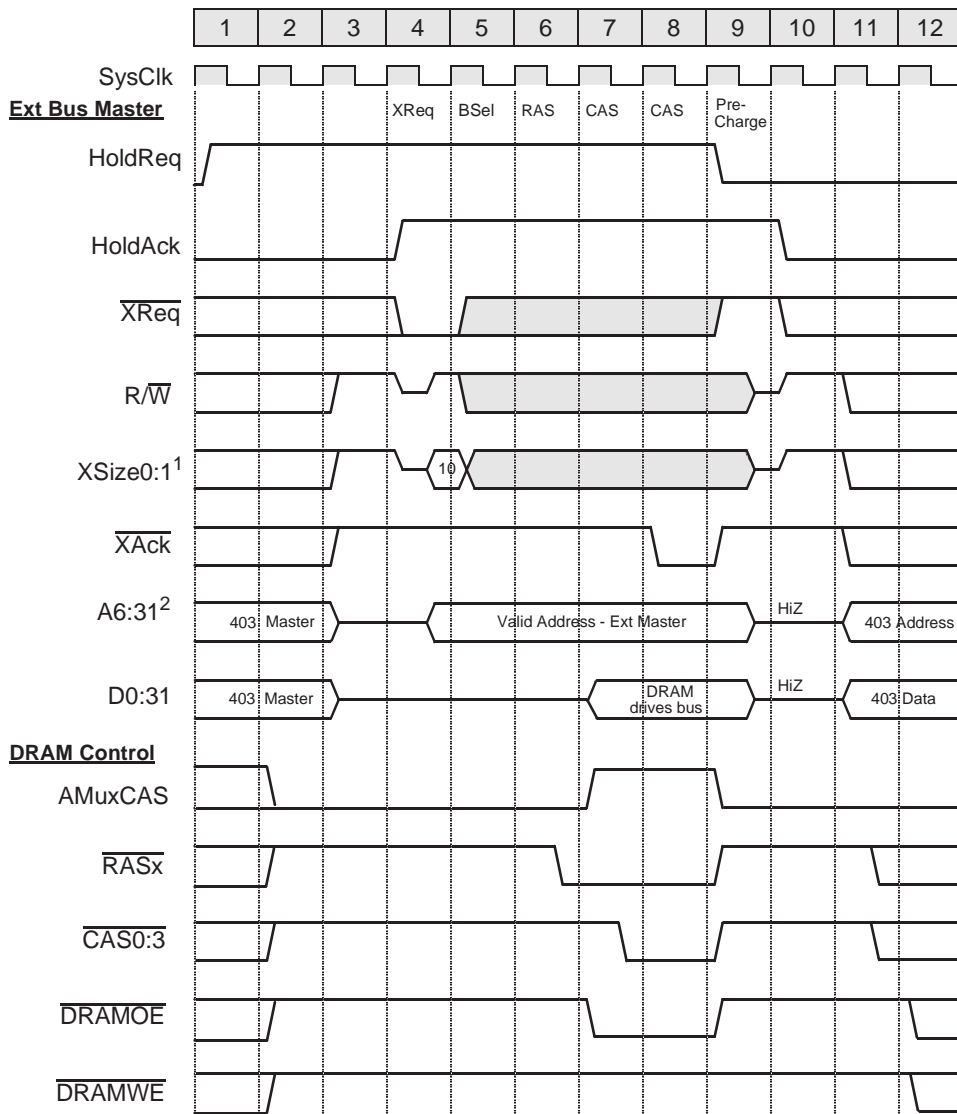
DMA Control Register Bit Settings

Transfer Direction	Transfer Width	Transfer Mode	Peripheral Setup	Peripheral Wait	Peripheral Hold	Burst Mode
Bit 2	Bits 4:5	Bits 9:10	Bits 11:12	Bits 13:18	Bits 19:21	Bit 25
1	10	01	Note 3	xx xxxx	xxx	1

Notes:

1. **DMAR** must be inactive at the end of cycle 9 (last **DMAA** cycle) to guarantee three transfers.
2. Peripheral data bus width must match DRAM bus width.
3. See diagram for settings.
4. This waveform assumes that the internal address mux is used.
5. **CAS0** is used for byte accesses, **CAS0:1** for halfwords, and **CAS0:3** for fullwords.
6. Numbers (1,2,3,...) in the **DMAR** signal represent when **DMAR** is sampled and accepted. Numbers (1,2,3,...) in the **DMAA** signal represent the transfers associated with the accepted **DMAR**.

External Master Nonburst DRAM Read with HoldReq/HoldAck



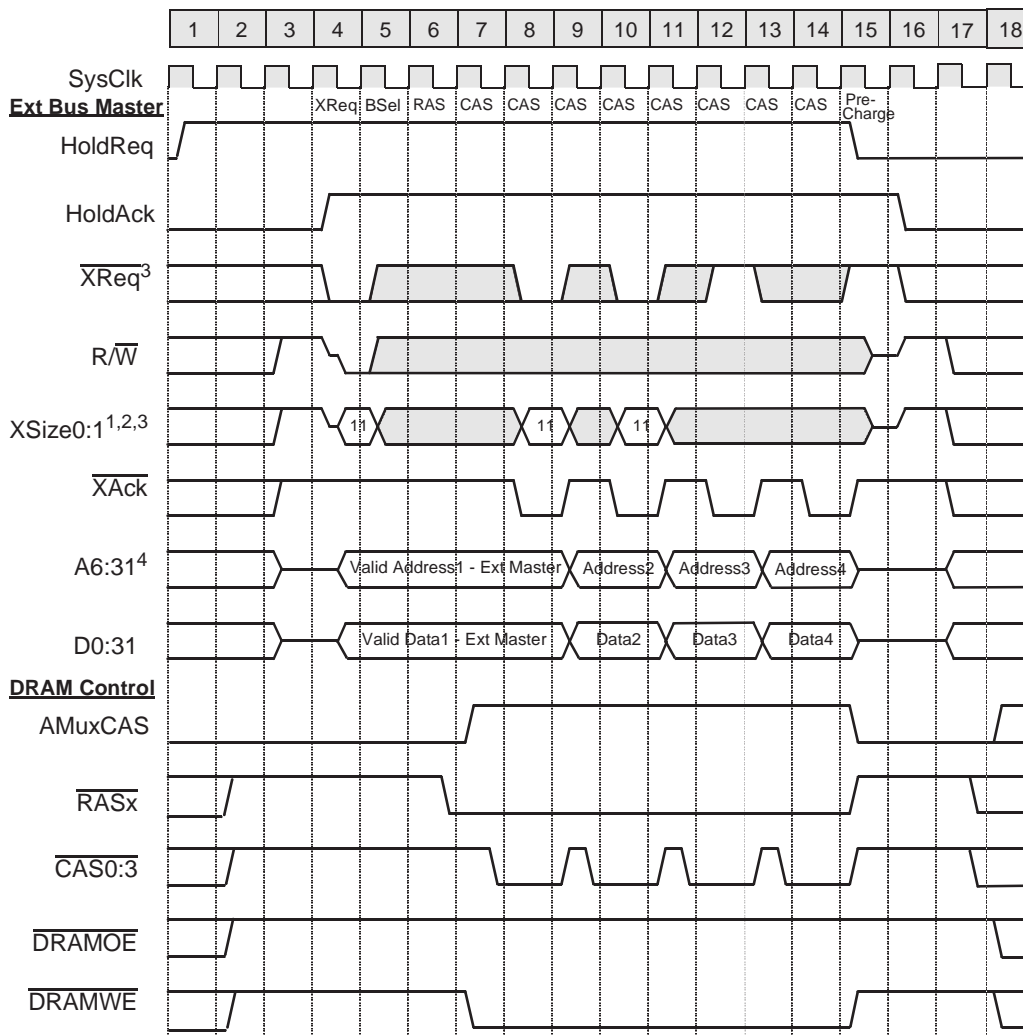
Bank Register Bit Settings

SLF	ERM	Bus Width	Ext Mux	RAS-to-CAS	Refresh Mode	Page Mode	First Access	Burst Access	Prechg Cycles	Refresh RAS	Refresh Rate
Bit 13	Bit 14	Bits 15:16	Bit 17	Bit 18	Bit 19	Bit 20	Bits 21:22	Bits 23:24	Bit 25	Bit 26	Bits 27:30
0 or 1	0	10	1	0	0	0	01	xx	0	x	xxxx

Notes:

- XSize1 is multiplexed with \overline{OE}
- A6, A7, A30, and A31 are multiplexed with $\overline{WBE0}$, $\overline{WBE1}$, $\overline{WBE2}$, and $\overline{WBE3}$, respectively. External master drives A6:7 into the 403GB.

External Master DRAM Burst Write, 3-2-2-2 Page Mode



Bank Register Bit Settings

SLF	ERM	Bus Width	Ext Mux	RAS-to-CAS	Refresh Mode	Page Mode	First Access	Burst Access	Prechg Cycles	Refresh RAS	Refresh Rate
Bit 13	Bit 14	Bits 15:16	Bit 17	Bit 18	Bit 19	Bit 20	Bits 21:22	Bits 23:24	Bit 25	Bit 26	Bits 27:30
0 or 1	0	10	1	0	0	1	01	01	0	x	xxxx

Notes:

- XSize1 is multiplexed with \overline{OE} .
- XSize0:1 = 11 indicates a burst transfer at the width of the DRAM device.
- The burst is terminated in cycle 12 by deasserting the \overline{XReq} input signal. A burst may also be terminated by deasserting either XSize0 or XSize1.
- A6, A7, A30, and A31 are multiplexed with $\overline{WBE0}$, $\overline{WBE1}$, $\overline{WBE2}$, and $\overline{WBE3}$, respectively. External master drives A6:7 in the 403GB.



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