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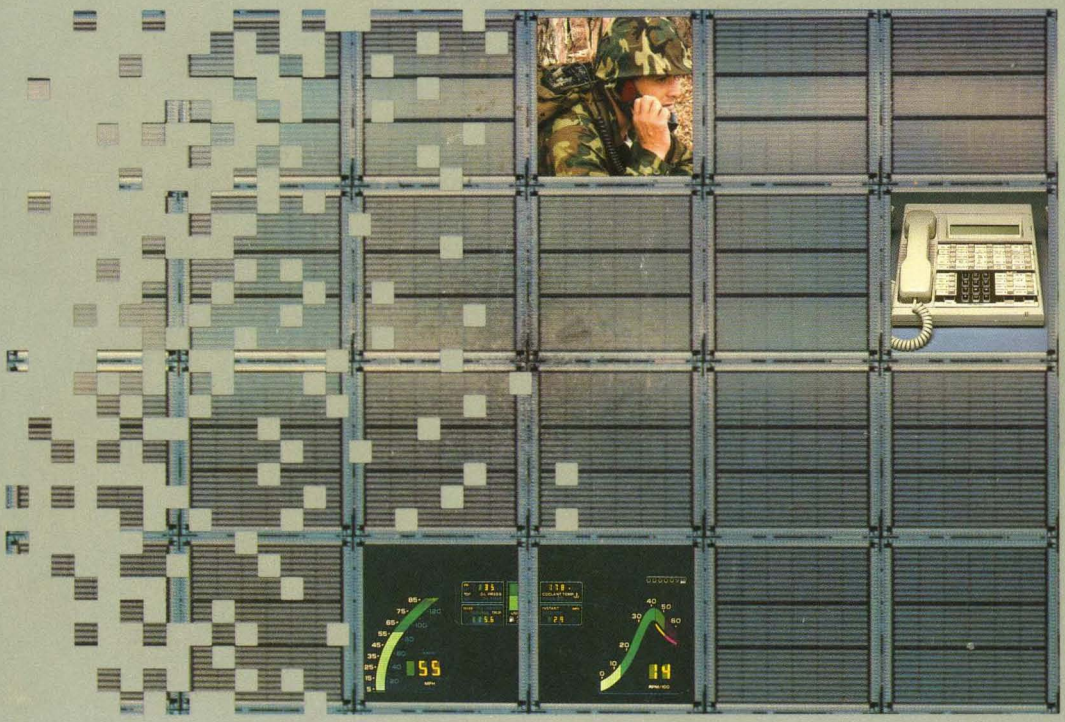
SOLID STATE PRODUCTS

1984 CMOS DATABOOK



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CMOS DATABOOK
1984

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Volume No. 2
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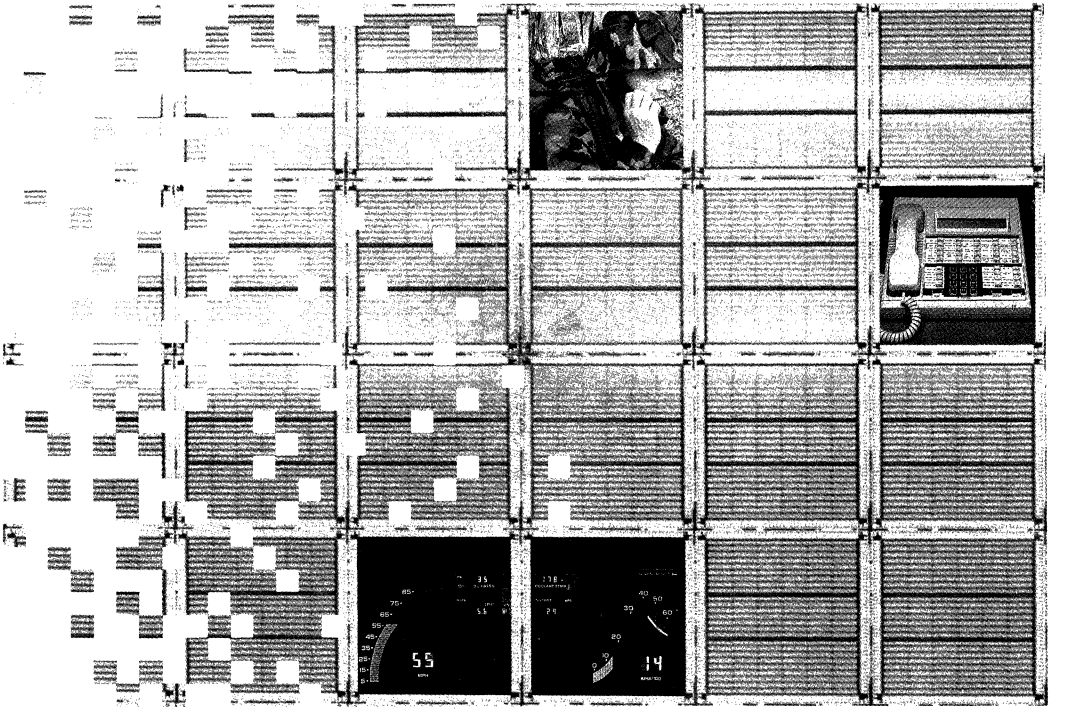

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Printed in U.S.A.

PRODUCT SELECTION GUIDE

Gate Arrays

Device	Number of Gates	Total Pads	I/O Pads	Packaging Options			
				DIP	LCC	Pin Grid Array	Flat Pack
H2084	2K	84	80	24 — 64	68 — 84	68, 84	—
H4120	4K	120	116	28 — 64	68, 84, 100	84, 120	—
H6152	6K	152	148	—	120	156	—
H8180	8K	180	172	—	—	180	180

CMOS EEPROMs

Device	Size	Organization	Access Time (Typ.)	Voltage	Erase/Write Byte Time	Endurance (Typ.)	Data Retention	CS Function To Enable EEPROM	No. Of Pins
H3104	4096	512 x 8	500 ns	4 — 6V	1 ms	10^4 cycles	10 yrs. @ 125°C	No	24
H3108	8192	1024 x 8	500 ns	4 — 6V	1 ms	10^4 cycles	10 yrs. @ 125°C	Yes	24
H3300	256	32 x 8	550 ns	5V	1 ms	10^4 cycles	10 yrs. @ 125°C	No	18
HB3108	8192	1024 x 8	700 ns	4 — 6V	1 ms	10^4 cycles	10 yrs. @ 125°C	Yes	24

Nonvolatile RAM

Device	Size	Organization	Access Time (Typ.)	Voltage	N.V. Store Operation	Recall Operation	Endurance (Typ.)	Data Retention	No. of Pins
H3500	256	64 x 4	300 ns	5V	10 ms	1 µs	10^4 cycles	10 yrs. @ 125°C	18

CMOS LCD Drivers

Device	Type of Drive	Input	Output	Buffer Size	Supply Voltage	Cascadable	No. of Pins
H0437	Direct Segment	4 Bit BCD	28 Segments (4 x 7)	28 Bits	3 — 10V	Yes	40
H7211-1	Direct Segment	4 Bit Multiplexed	Hexidecimal 28 Segments (4 x 7)	28 Bits	3 — 6V	Yes	40
H7211-2	Direct Segment	4 Bit Multiplexed	Code B 28 Segments (4 x 7)	28 Bits	3 — 6V	Yes	40
H7211-3	Direct Segment	4 Digit Select Microprocessor Interface	Hexidecimal 28 Segments (4 x 7)	28 Bits	3 — 6V	Yes	40
H7211-4	Direct Segment	4 Digit Select Microprocessor Interface	Code B 28 Segments (4 x 7)	28 Bits	3 — 6V	Yes	40
H0438A	Direct Segment	1 Bit Serial	32 Segments	32 Bits	3 — 10V	Yes	40
H0439	Direct Segment	1 Bit Serial	32 Segments	32 Bits	4.5 — 10V	Yes	40
H0488	Multiplexed	4 Bit Parallel	16 Rows x 16 Columns	32 Bits	3 — 8V	Yes	40
H0538A	Multiplexed	Serial	8 Rows x 26 Columns	34 Bits	3 — 10V	Yes	40
H0539A	Multiplexed	Serial	34 Columns	34 Bits	3 — 10V	Yes	40
H0540	Multiplexed	Serial	32 Rows or 32 Columns	31 Bits	3 — 12V	Yes	40
H0541	Multiplexed	4 Bit Parallel	8 Rows x 23 Columns	32 Bits	3 — 12V	Yes	40
H0542	Multiplexed	4 Bit Parallel	32 Columns	32 Bits	3 — 12V	Yes	40
H0548	Multiplexed	Serial	16 Rows x 16 Columns	200 Bits	3 — 12V	Yes	40
H0607A	Multiplexed	Serial	4 Rows x 30 Columns	34 Bits	3 — 12V	Yes	40
H0515	Multiplexed/ Auto-Refresh	Serial	8 Rows x 25 Columns	32 Bits	5 — 10V	Yes	40
H0550	Multiplexed/ Auto-Refresh	8 Bit Parallel/ASCII	8 Rows x 12 Columns	32 Char	3 — 10V	Yes	40
H0551	Multiplexed/ Auto-Refresh	Serial	34 Columns	34 Bits	3 — 10V	Yes	40
HM0438A	Direct Segment	1 Bit Serial	32 Segments	32 Bits	3 — 10V	Yes	40

PRODUCT SELECTION GUIDE

CMOS ROMs

Device	Size	Organization	Access Time (Typ.)		Temperature Range		Supply Voltage		Ouput	No. of Pins
			5V	10V	Ceramic	Plastic	Low Voltage	High Voltage		
H1831	4096	512 x 8	850 ns	400 ns	−55 to +125°C	−40 to +85°C	4 — 6.5V	4 — 10.5V	3-state	24
H1832	4096	512 x 8	850 ns	400 ns	−55 to +125°C	−40 to + 85°C	4 — 6.5V	4 — 10.5V	3-state	24
H1833	8192	1024 x 8	650 ns	350 ns	−55 to +125°C	−40 to +85°C	4 — 6.5V	4 — 10.5V	3-state	24
H1834	8192	1024 x 8	575 ns	350 ns	−55 to +125°C	−40 to +85°C	4 — 6.5V	4 — 10.5V	3-state	24
H1835	16384	2048 x 8	900 ns	—	−55 to +125°C	−40 to +85°C	4 — 6.5V	—	3-state	24
H23C16	16834	2048 x 8	900 ns	—	−55 to +125°C	−40 to +85°C	4 — 6.5V	—	3-state	24
H1837	32768	4096 x 8	750 ns	—	−55 to +125°C	−40 to +85°C	4 — 6.5V	—	3-state	24
H23C32	32768	4096 x 8	750 ns	—	−55 to +125°C	−40 to +85°C	4 — 6.5V	—	3-state	24
H23C64	65536	8192 x 8	300 ns	—	−55 to +125°C	−40 to +85°C	4 — 6.5V	—	3-state	24
H23C65	65536	8192 x 8	300 ns	—	−55 to +125°C	−40 to +85°C	4 — 6.5V	—	3-state	28
HM1831	4096	512 x 8	850 ns	400 ns	−55 to +125°C	—	4 — 6.5V	4 — 10.5V	3-state	24
HM1833	8197	1024 x 8	650 ns	350 ns	−55 to +125°C	—	4 — 6.5V	4 — 10.5V	3-state	24

CMOS RAMs

Device	Size	Organization	Access Time (Typ.)		Temperature Range		Supply Voltage		Ouput	No. of Pins
			5V	10V	Ceramic	Plastic	Low Voltage	High Voltage		
H1822	1024	256 x 4	250 ns	—	−55 to +125°C	−40 to +85°C	4 — 6.5 V	—	3-state	22
H1823	1024	128 x 8	250 ns	—	−55 to +125°C	−40 to +85°C	4 — 6.5V	—	3-state	24
H1824	256	32 x 8	400 ns	200 ns	−55 to +125°C	−40 to +85°C	4 — 6.5V	4 — 10.5V	3-state	18

1800 Microprocessor Family

Device	Description	Temperature Range		Voltage Range		No. of Pins
		Ceramic	Plastic	Low Voltage	High Voltage	
H1802A	CPU — 8 Bit Parallel with 3.2 MHz clock @ 5V.	−55 to +125°C	−40 to +85°C	4 — 6.5V	4 — 10.5V	40
H1802B	CPU — 8 Bit Parallel with 5 MHz clock @ 5V.	−55 to +125°C	−40 to +85°C	4 — 6.5V	—	40
H1822	RAM — 256 x 4 (1024) with a typ. access time of 250 ns @ 5V.	−55 to +125°C	−40 to +85°C	4 — 6.5V	—	22
H1823	RAM — 128 x 8 (1024) with a typ. access time of 250 ns @ 5V.	−55 to +125°C	−40 to +85°C	4 — 6.5V	—	24
H1824	RAM — 32 x 8 (256) with a typ. access time of 400 ns @ 5V/200 ns @ 10V.	−55 to +125°C	−40 to +85°C	4 — 6.5V	4 — 10.5V	18
H1831	ROM — 512 x 8 (4096) with a typ. access time of 850 ns @ 5V/400 ns @ 10V.	−55 to +125°C	−40 to +85°C	4 — 6.5V	4 — 10.5V	24
H1832	ROM — 512 x 8 (4096) with a typ. access time of 850 ns @ 5V/400 ns @ 10V.	−55 to +125°C	—	4 — 6.5V	4 — 10.5V	24
H1833	ROM — 1024 x 8 (8192) with a typ. access time of 575 ns @ 5V/350 ns @ 10V.	−55 to +125°C	−40 to +85°C	4 — 6.5V	4 — 10.5V	24
H1834	ROM — 1024 x 8 (8192) with a typ. access time of 575 ns @ 5V/350 ns @ 10V.	−55 to +125°C	—	4 — 6.5V	4 — 10.5V	24
H1835	ROM — 2048 x 8 (16384) with a typ. access time of 900 ns @ 5V/500 ns @ 10V.	−55 to +125°C	−40 to +85°C	4 — 6.5V	—	24
H1837	ROM — 4096 x 8 (32768) with a typ. access time of 750 ns @ 5V/450 ns @ 10V.	−55 to +125°C	−40 to +85°C	4 — 6.5V	—	24
H1852	INPUT/OUTPUT PORT — 8 Bit Parallel with mode programmable 3-state data bus.	−55 to +125°C	−40 to +85°C	4 — 6.5V	4 — 10.5V	24
H1853	N-BIT DECODER — 1 of 8 Decoder for I/O Expansion.	−55 to +125°C	−40 to +85°C	4 — 6.5V	4 — 10.5V	16
H1854A	UART — Full duplex organization with serial/parallel inputs/outputs.	−55 to +125°C	−40 to +85°C	4 — 6.5V	4 — 10.5V	40
H1855	MULTIPLY/DIVIDE — 8 x 8 Multiply of 16 ÷ 8 Divide with bi-directional 3-state data bus.	−55 to +125°C	−40 to +85°C	4 — 6.5V	4 — 10.5V	28
H1856/57	BUFFER/SEPARATOR — 4 Bit with bi-directional 3-state data bus.	−55 to +125°C	−40 to +85°C	4 — 6.5V	4 — 10.5V	16
H1858/59	LATCH/DECODER — 4 Bit Memory Address to select 1K RAMS.	−55 to +125°C	−40 to +85°C	4 — 6.5V	4 — 10.5V	16
HM1831	ROM — 128 x 8 (1024) processed to Mil. Std. 883B.	−55 to +125°C	—	4 — 6.5V	4 — 10.5V	24
HM1833	ROM — 1024 x 8 (8192) processed to Mil. Std. 883B.	−55 to +125°C	—	4 — 6.5V	4 — 10.5V	24

MICROPROCESSOR/PERIPHERALS

HUGHES P/N	AMI	FAIRCHILD	GENERAL INSTRUMENTS	HARRIS	INTEL	INTERSIL	MOSTEK	MOTOROLA	NATIONAL	RCA	WESTERN DIGITAL
H1802A/B 8 Bit CPU										CDP 1802A/B	
H1852 8 Bit I/O Port		MK 386K			8212				INSB212	CDP 1852	
H1853 N-Bit Decoder										CDP 1853	
H1854A UART			AY-3- 1013	HD6402		IM6402				CDP 1854A	TR 1602A
H1855 Multiply/Divide										CDP 1855	
H1856 Bus Separator Buffer										CDP 1856	
H1857 Bus Separator Buffer										CDP 1857	
H1858 Latch/Decoder										CDP 1858	
H1859 Latch/Decoder										CDP 1859	

NONVOLATILE MEMORIES/CMOS MEMORIES

HUGHES P/N	AMI	FAIRCHILD	HARRIS	HITACHI	INTEL	INTERSIL	MOSTEK	MOTOROLA	NATIONAL	OKI	RCA	SIGNETICS	SSS	SUPERTEX	SYNERTEK	TEXAS INSTRUMENTS	TOSHIBA	XICOR
H1822C 256 x 4 RAM	S5101	F47218C	HM 6551	HM435101		IM 6551		MC5101	MM2101 74C920	MSM573	CDP 1822C	2101	SLM 5101		SY2101	2101	TC 5501	
H1823C 128 x 4 RAM								MC6810A	6551 6552									
H1824 32 x 8 RAM											CDP 1824							
H1831/32 512 x 8 ROM					2704		MK2500P MK2600		87SL9S/6 5204C 5232/33	MSM575	CDP 1831/32					SNXXS474 SNXXS475		
H1833/34 1024 x 8 ROM					8708			MCM65308			CDP 1833/34							
H1835 2048 x 8 ROM					2716 2316						CDP 1835							
H1837 4096 x 8 ROM											CDP 1837							
H23C16 2048 x 8 ROM					2716 2316	IM 6316				5316				CM 1600				
H23C32 4096 x 8 ROM																		
H23C64 8192 x 8 ROM																		
H3104 512 x 8 E^2PROM																		
H3108 1024 x 8 E^2PROM																		
H3300 32 x 8 E^2PROM																		
H3500 64 x 4 NOV RAM																		X2210

LCD DRIVERS

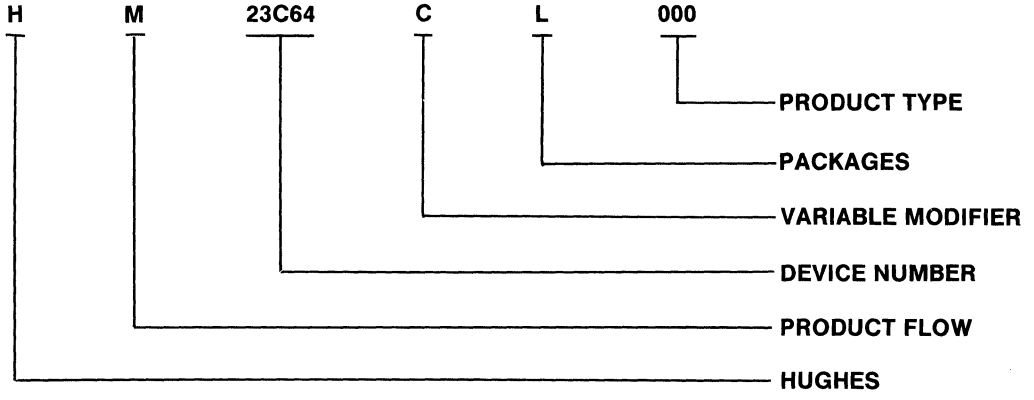
HUGHES P/N	AMI	DATEL	INTERSIL	NATIONAL	SILICONIX
H0437 4 DIGIT DRIVER					
H7211-1 4 Digit Driver		DD7211	7211IPL		
H7211-2 4 Digit Driver		DD7211A	7211AIPL		DF412
H7211-3 4 Digit Driver			7211MIPL		
H7211-4 4 Digit Driver			7211AMIPL		
H0438A Serial Input Driver	S4521			58438	
H0488 Parallel Input Driver					
H0538A/0539A Serial Input Drivers					
H0540 Serial Input Driver					
H0541/0542 Parallel Input Drivers					
H0548 Serial Input Driver					
H0515 Auto Refresh Driver					
H0550/0551 Intelligent Controller					
H0607A Serial Input Driver					

STATUS NOTICES

Preliminary Information: indicates guidance values for evaluation purposes. Some electrical parameters are subject to change.
Advance Information: indicates design objectives. Some functional characteristics are subject to change.

NOMENCLATURE

Hughes is in the process of re-defining our nomenclature. For more detailed information, contact Hughes or Hughes' representatives.



Example
HM 23C64-C-L-000 = Hughes Military 23C64, 4-6.5 voltage range, in a leadless chip carrier package, standard device.

Product Type
- 000 = Standard Product
- XYZ = Custom Product*

Variable Modifier*
One character modifier for speed, power, processing, etc.

Packages
- L = Leadless Chip Carrier
- D = Ceramic Dip
- H = Devices in Chip Form
- P = Plastic Dip
- Y = Cerdip

Product Flow
- C = Commercial
- I = Industrial
- B = Hi Reliability
- M = Military
- S = Special*

*For detailed information, contact Hughes' Customer Service.

HCMOS Configurable Gate Arrays

DESCRIPTION

Hughes' Quad Logic® Array family of Configurable Gate Arrays utilize an oxide-isolated, double metal HCMOS process. The devices range in complexity from 2,000 to 8,000 gates.

The basic Quad Logic cell is a four gate equivalent, consisting of 10 n-channel and 10 p-channel transistors arranged as two back-to-back 2-input and 3-input gate equivalents(see figure below). This architecture, combined with double layer metal interconnections, minimizes the number of gates necessary to implement macro functions and ensures efficient interconnection and routing.

The Quad Logic Array family is fully supported by Hughes Design Automation software tools which include an extensive macro function library, logic capture, simulation and verification tools, testability analysis and fault modeling. Hughes' proprietary Gate Array Layout Automation system (GALA) allows for automatic placement of macros and routing of the interconnection patterns. The HCMOS process provides switching speeds exceeding that of Schottky/TTL while providing low power consumption, high noise immunity, and ease of design.

The Quad Logic Array family is available in a variety of ceramic and plastic DIPs, leadless chip carriers and pin grid arrays. See page 5 for more details.

FEATURES

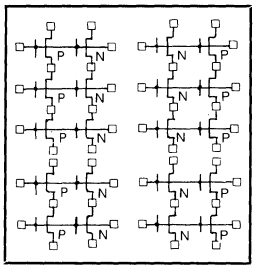
- High Performance 3μ HCMOS Silicon Gate Technology
- TTL and CMOS I/O Compatibility
- Output Buffer Options Provide Drive Currents of up to 16 mA
- Standard Process is MIL. STD. 883
- Up to 172 I/O Buffers Available
- P Channel and N Channel Sizes for Symmetrical Switching ($W_p = 2W_n$)
- Extensive Macro Library Available
- Two Levels of Metal Interconnection
- Propagation Delays of 1.4 Nanoseconds and Data Rates up to 35 MHz

Quad Logic Array Family

DEVICE	H2088	H4120	H6152	H8180
Number of Gates	2K	4K	6K	8K
Total Pads	88	120	152	180
I/O Pads	84	116	148	172
PACKAGING OPTIONS				
DIP	24-64	28-64	—	—
LCC	68,84	68,84,100	120	—
Pin Grid Array	68,84	84,120	156	180
Flat Pack	—	80	—	180*

* In development

Quad Cell Schematic



ABSOLUTE MAXIMUM RATINGS

(Referenced to Ground)

DC Supply-Voltage Range (V_{DD}) ..... − 0.3 to + 7.5 Volts
Input Voltage (V_I) ..... − 0.3 Volts to (V_{DD} + 0.3) Volts
DC Input Current (I_I) ..... ± 10 mA
Storage Temperature Range (T_{STG})
Ceramic ..... − 65 to + 150°C
Plastic ..... − 40 to + 125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Operating Ambient Temperature Range (T_A)
Military ..... − 55 to + 125°C
Industrial ..... − 40 to + 85°C
Commercial ..... 0 to + 70°C
DC Supply Voltage (V_{DD}) ..... + 3 to + 6 Volts

D.C. CHARACTERISTICS, Specified at V_{DD} = 5V ± 10% (referenced to Ground), T_A = − 55 to + 125°C.

SYMBOL	PARAMETERS	CONDITIONS	Min.	Typ.	Max.	UNITS
V_{IL}	Low Level Input Voltage TTL Inputs	—	—	—	0.8	V
	CMOS Inputs	—	—	—	1.5	
V_{IH}	High level Input Voltage TTL Inputs	—	2.2	1.7	—	V
	CMOS Inputs	—	3.5	2.5	—	
I_{IN}	Input Current CMOS, TTL Inputs	$V_{IN} = V_{DD}$	− 10	1	10	µA
	Inputs with pull-down resistors	$V_{IN} = V_{DD}$	—	150	800	
	CMOS Inputs	V_{IN} = 0.4V	− 10	1	10	
	TTL Inputs & Inputs with Pull-Up Resistors	V_{IN} = 0.4V	−800	− 150	—	
V_{OH}	High Level Output Voltage Type T1	I_{OH} = 1.6 mA	2.4	4.5	—	V
	Type T2	I_{OH} = 3.2 mA	2.4	4.5	—	
	Type T3	I_{OH} = 4.8 mA	2.4	4.5	—	
V_{OL}	Low Level Output Range Type T1	I_{OL} = 2.0 mA	—	0.2	0.4	V
	Type T2	I_{OL} = 4.0 mA	—	0.2	0.4	
	Type T3	I_{OL} = 8.0 mA	—	0.2	0.4	
I_{OZ}	Three-State Output Leakage Current	V_{OH} = +V or GND	− 10	1	10	µA
I_{OS}	Output Short Circuit Current Type T3	+V = 5V, V_O = +V + V = 5V, V_O = OV	25 − 7	— —	90 − 28	mA
I_{DD}	Quiescent Supply Current	V_{IN} = +V or GND	Design Dependent			
C_{IN}	Input Capacitance	Any Output (design dependent/typical)	—	5	—	pF
C_{OUT}	Output Capacitance	Any Input (design dependent/typical)	—	8	—	pF

A.C. CHARACTERISTICS (Typical Values), Supply Voltage (+V) = 5V, T_A = + 25°C

MACRO TYPE	SYMBOL	Δt_{PD} 1 Gate Load ns	Δt_{PD} per Gate Load ns Gate	Δt_{PD} mm Metal ns/mm	Δt_{PD} ns t_R/t_F ns/ns
1X Inverter	t_{PHL} t_{PLH}	.74 .82	.27 .36	.23 .30	.08 .14
2X Inverter	t_{PHL} t_{PLH}	.60 .63	.13 .17	.12 .14	.06 .11
4X Inverter	t_{PHL} t_{PLH}	.53 .56	.06 .08	.06 .08	.05 .09
NAND, 2- Input	t_{PHL} t_{PLH}	1.42 1.11	.40 .30	.38 .31	.07 .15
NAND, 3- Input	t_{PHL} t_{PLH}	2.43 1.41	.57 .31	.57 .29	.04 .17
NOR, 2- Input	t_{PHL} t_{PLH}	.80 1.53	.23 .61	.20 .60	.08 .17
NOR, 3- Input	t_{PHL} t_{PLH}	1.15 3.4	.26 .92	.25 .90	.13 .09
D Flip/Flop	t_{PHL} t_{PLH} t_S t_H	2.60 2.30 2.83 —	.32 .40 — —	.36 .40 — —	0.19 0.15 — —
Input Buffer, R1	t_{PHL} t_{PLH}	3.13 4.95	.39 1.38	.45 1.25	0.15 0.17

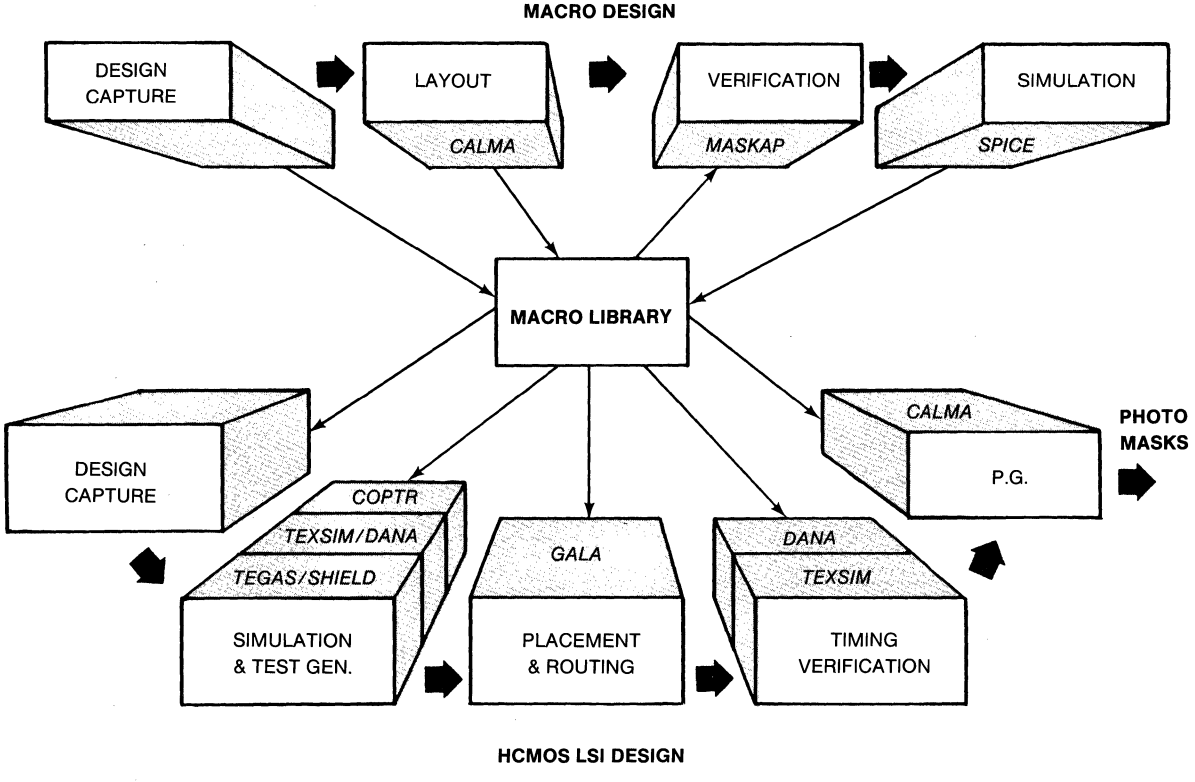
A.C. CHARACTERISTICS, cont.

OUTPUT LOADING	SYMBOL	15pF	50pF	100pF	150pF	UNITS
Output, T1	t_{PHL} t_{PLH}	5.96 3.66	13.83 8.95	25.03 16.5	36.2 24.5	ns
Output, T2	t_{PHL} t_{PLH}	5.55 3.08	9.66 5.75	15.30 9.53	21.0 13.30	ns
Output, T3	t_{PHL} t_{PLH}	6.12 3.25	9.10 5.08	13 7.6	16.8 10.13	ns

DESIGN AUTOMATION

The heart of Quad Logic Array implementation is the well-documented macro library. The figure below depicts the parallel paths for LSI and macro developments.

Each developmental step is supported by the software indicated and the designer may choose to enter the development cycle at any step as long as the data bases are compatible. New macros are continuously being added to the library and are available for general use after verification and simulation.



POWER DISSIPATION ESTIMATES

The most important elements of power dissipation in HCMOS circuits are the charging and discharging of circuit capacitances and output loading. Power dissipation due to leakage currents and switching overlap currents are normally negligible over the standard logic operating conditions.

The capacitive switching power is equivalent to $P = fCV^2$; where P = power dissipation, f = switching frequency, C = capacitance being switched, and V = the voltage change across the capacitance. The following guide can be used for initial estimation of power dissipation of the Quad Logic Array family.

1. Equivalent gate dissipation P_G = 0.016 mW/MHz
   (2-input NAND with fanout = 2 and 2 mm of interconnect)

2.

Output Type	Dissipation mW/MHz/pf
T1	0.026
T2	0.0265
T3	0.027

Example for Power Dissipation Estimation

1. Internal logic dissipation:

   a) No. of equivalent gates utilized 6,500
   b) Percent switching each cycle 15%
   c) No. of gates switching each cycle 975
   d) Power per gate/MHz 0.016 mW/MHz
   Total internal logic dissipation = 15.6 mW/MHz

2. Output power dissipation:

   a) No. of T3 outputs utilized 72
   b) Output load capacitance (avg) 50 pF
   c) No. of outputs switching (avg) 18
   d) Power per output of MHz 1.35 mW/MHz
   Total output power dissipation = 24.3 mW/MHz

3. Total power per MHz (1 + 2) = 39.9 mW/MHz
   @ 10 MHz Power = 399 mW

Use the above estimation technique during initial design. More accurate power dissipation estimates can be made with actual interconnect capacitances as determined from routing data and from nodal switching as determined during logic simulation.

PROPAGATION DELAY ESTIMATION

The tabulation of typical AC Characteristics provides a method of estimating the propagation delays through the logic circuitry by summing the effects of gate fanout, interconnect loading and input rise and fall times for each node of interest.

The macro library data sheets provide curves and data for worse case (V_{DD} = 4.5V, T_A = + 125°C); best case (V_{DD} = 5.5V, T_A = − 55°C) and nominal case (V_{DD} = 5V, T_A = + 25°C) conditions. To estimate delays at other conditions, the following multipliers may be used to account for temperature and supply voltage variations.

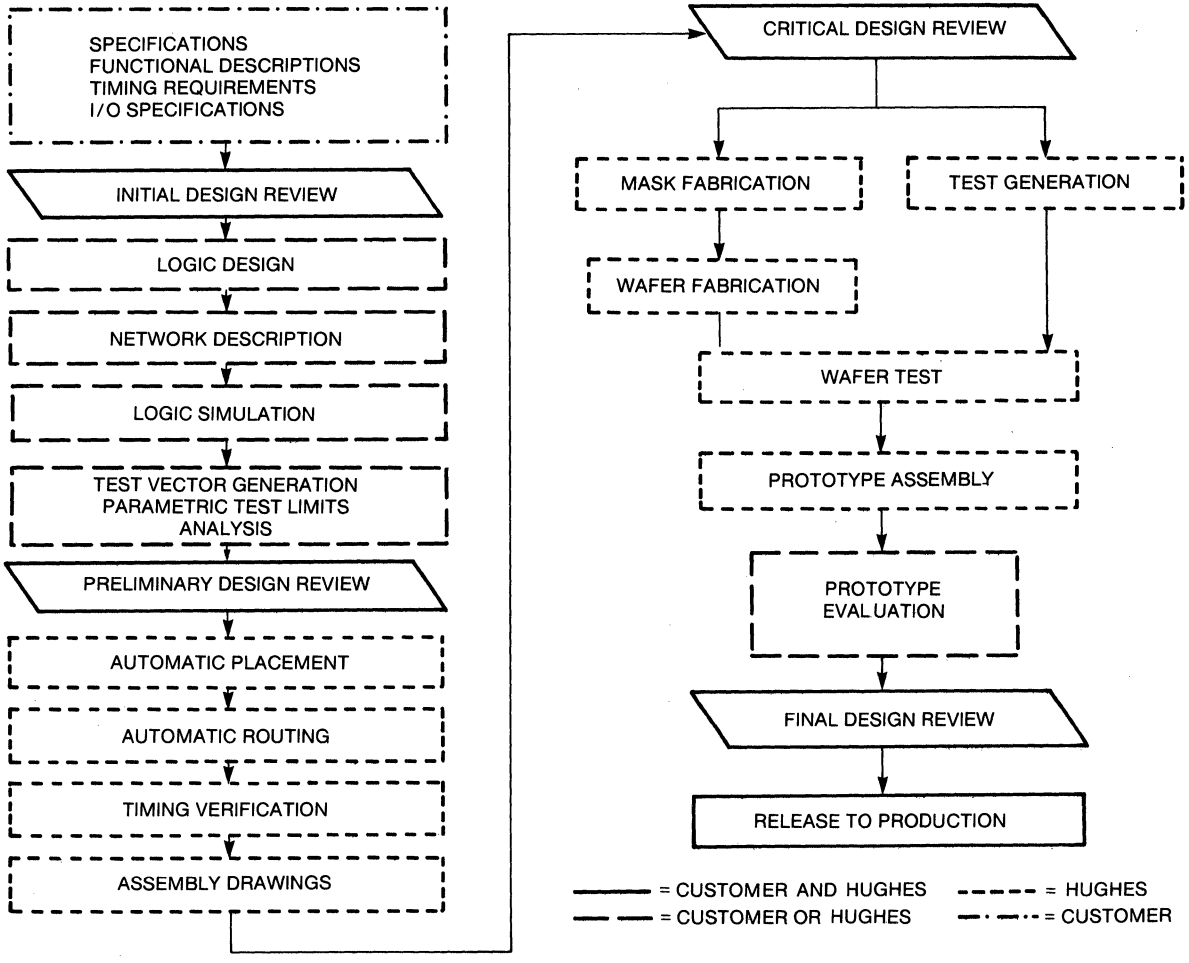
Temperature	− 55°C	− 30°C	0°C	+ 25°C	+ 85°C	+ 125°C
Multiplier	0.76	0.83	0.93	1.0	1.18	1.3

Voltages	+ 3.0V	+ 4.0V	+ 4.5V	+ 4.75V	+ 5.0V	+ 5.25V	+ 5.5V	+ 6.0V	+ 7.0V
Multiplier	1.7	1.3	1.15	1.07	1.0	0.93	0.89	0.78	0.70

The above consideration for gate loading, gate input rise and fall times, temperature variations and supply voltage variations are all determined for nominal production conditions. Estimating "worse case" and "best case" delays should include a 40% factor for lot-to-lot manufacturing variations.

DEVELOPMENT CYCLE

Hughes offers several levels of design interface. Your engineers may do the entire design or Hughes' engineers can do the design work. The chart below details the levels of interface.



PACKAGING

The standard packages listed below are available for the Quad Logic Array family of High Performance Gate Arrays. The primary package used for each type is further highlighted. Pin grid array packages are preferred for prototype evaluation. Package types other than those listed may be available upon request.

DEVICE	DIP TYPES 0.100" CENTER	LCC TYPES 0.050" CENTERS	PIN GRID ARRAY 0.100" CENTERS	FLAT PACKS
H2088	24 to 64	68, 84	68, 84	—
H4120	28 to 64	68, 84, 100, 120	84, 120	80 (0.050" centers)
H6152	—	—	156	—
H8180	—	—	180	180* (0.035" centers)

* In Development

512 x 8
CMOS EEPROM

DESCRIPTION

Hughes' 3104 is a CMOS Electrically Erasable and Programmable Read Only Memory (EEPROM) organized 512 x 8. It is ideal for applications where large amounts of data must occasionally be altered and then stored during power down conditions such as program storage, data tables or data collection.

Data modification is accomplished by first raising the power voltage, V_{DD} to + V_{PP} and selecting the device with CS high (+5V). Then, erasing or writing is controlled with T^2L level signals to the appropriate control inputs $\overline{OE}$ (Erase) and $\overline{CE}$ (Write).

All read operations are performed with V_{DD} at 5 volts. With CS at a high level, the falling edge of the Chip Enable signal ($\overline{CE}$) latches a valid address input and initiates the accessing of data. The information is enabled on the bus when Output Enable ($\overline{OE}$) is a low level.

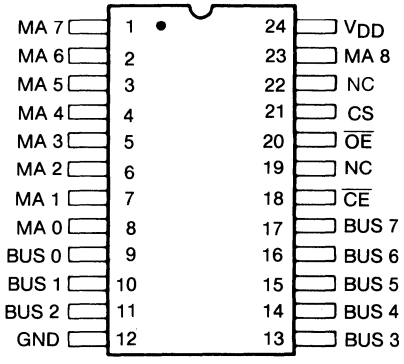
The Chip Select (CS) input for this device is functional in all modes, allowing for chip selection in the Read, Erase, or Write modes independent of $\overline{OE}$ and $\overline{CE}$ inputs.

The 3104 is available in a 24 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carriers, (L suffix).

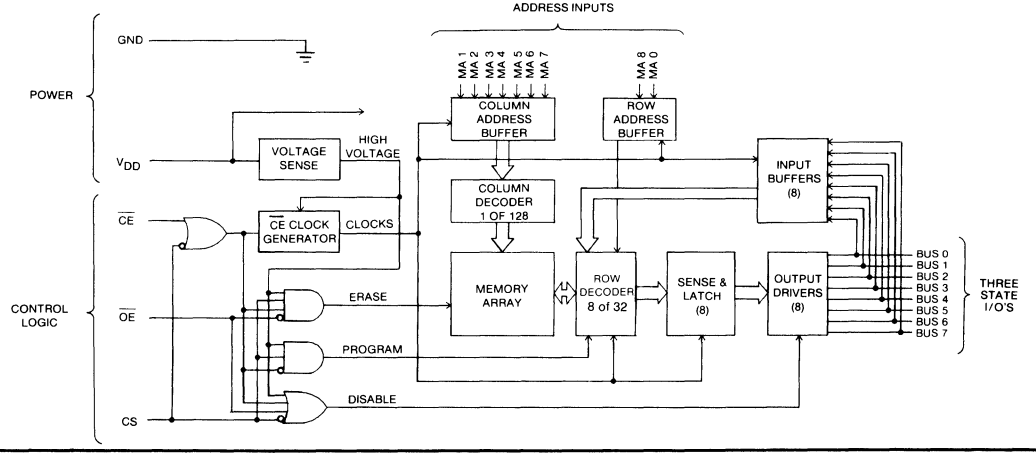
FEATURES

- 512 x 8 CMOS EEPROM
- TTL Level Erase/Byte Write Controls
- 1 ms Erase/Write times
- 10,000 Erase/Write cycles
- 10 year Data Retention
- 3-Line Control Architecture
- 10 µW Typical Quiescent Power Dissipation
- JEDEC Approved 24 pin DIP

PIN CONFIGURATION



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage Range ..... −0.3 to + 18 Volts
(All Voltages referenced to GND terminal)
Input Voltage Range ..... −0.3 to V_{DD} + 0.3 Volts
Storage Temperature Range ..... −65 to + 150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		Read Mode	Write or Erase Mode
V_{DD} Supply Voltage		5 ± 1 Volts	16 ± 1 Volts
Temperature Range	HC3104	0°C to + 70°C	0°C to + 70°C
	HI 3104	−40°C to + 85°C	−40°C to + 85°C

DC OPERATING CHARACTERISTICS

Read: V_{DD} = 6V Unless Otherwise Specified

			HC3104		HI 3104			
		+25°C	0°C to +70°C		-40°C to +85°C			TEST A
SYMBOL	PARAMETER	TYPICAL[1]	MIN.	MAX.	MIN.	MAX.	UNITS	CONDITIONS
I_{CC1}	Standby Current	2	—	100	—	100	µA	V_{IN} = 0 or V_{DD}
I_{CC1A}	Active Current[1]	2	—	100	—	100	µA	$\overline{CE}$ = $\overline{OE}$ = 0
V_{OL}	Output Low Voltage	0.25	—	0.45	—	0.45	V	V_{DD} = 4.75V, I_O = 2.1mA
V_{OH}	Output High Voltage	4.5	2.4	—	2.4	—	V	V_{DD} = 4.75V, I_O = −400µA
V_{IL}	Input Low Voltage	—	—	0.6	—	0.6	V	V_{DD} = 4.75V
V_{IH}	Input High Voltage	—	2.4	—	2.4	—	V	V_{DD} = 5.25V
I_{LI}	Input Leakage Current[1]	± 0.1	—	± 1	—	± 1	µA	V_{IN} = 0 or V_{DD}
I_{LO}	Output Leakage Current[1]	± 0.3	—	± 1	—	± 1	µA	V_O = 0 or V_{DD}

Erase or Write: V_{DD} = 17V Unless Otherwise Specified

			HC3104		HI 3104			
		25°C	0°C to + 70°C		−40°C to +85°C			TEST
SYMBOL	PARAMETER	TYPICAL[1]	MIN.	MAX.	MIN.	MAX.	UNITS	CONDITIONS
I_{CC2}	Prog. Current	3	—	5	—	5	mA	V_{IN} = 0 or V_{DD}
I_{CC2A}	Prog. Current	25	—	30	—	30	mA	V_{IN} = 5V
V_{IL}	Input Low Voltage	—	—	0.6	—	0.6	V	—
V_{IH}	Input High Voltage	—	3.8	—	3.8	—	V	—
I_{LI}	Input Leakage Current[1]	± 0.1	—	± 1	—	± 1	µA	V_{IN} = 0 or V_{DD}
I_{LO}	Output Leakage Current[1]	± 0.3	—	± 1	—	± 1	µA	V_O = 0 or V_{DD}

AC OPERATING CHARACTERISTICS
Read: V_{DD} = 5V Unless Otherwise Specified

			HC3104		HI 3104			
		25°C	0°C to +70°C		−40 to +85°C		UNITS	TEST CONDITIONS
SYMBOL	PARAMETER	TYPICAL[1]	MIN.	MAX.	MIN.	MAX.		
t_{ASU}	Address Set Up Time	0	75	—	75	—	ns	$CS = V_H$
t_{AH}	Address Hold Time	100	200	—	200	—	ns	$CS = V_H$
t_{ACE}	Access Time from $\overline{CE}$	500	—	800	—	825	ns	$CS = V_H$, $\overline{OE} = V_L$
$t_{\overline{OE}}$	Output Enable Time	250	—	375	—	400	ns	$CS = V_H$, $\overline{CE} = V_L$
t_{ACS}	Access Time from CS	550	—	800	—	825	ns	$\overline{CE} = V_L$, $\overline{OE} = V_L$
t_{DF}	$\overline{OE}$ to High Impedence	350	—	450	—	475	ns	$\overline{CE} = V_L$, $CS = V_H$
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$, or CS which ever occurs first	0	0	—	0	—	ns	—
t_{CEH}	$\overline{CE}$ High Time	0.5	1.4	—	1.4	—	µs	—
I_{CC3}	Dynamic Current	1.0	—	1.2	—	1.2	mA	f = 100KHz

READ TEST CONDITIONS

Output Load: C_L = 50pF
Input Levels: V_H = 2.4 Volts, V_L = 0.45 Volts
Timing Measurement Reference Levels: Input = Output = 50%
Input Rise and Fall Times: $t_r = t_f$ = 10ns

Erase and Write, V_{DD} = 16V Unless Otherwise Specified

			HC3104		HI 3104			
		25°C	0°C to +70°C		−40 to +85°C		UNITS	TEST CONDITIONS
SYMBOL	PARAMETER	TYPICAL[1]	MIN.	MAX.	MIN.	MAX.		
t_{VPS}	Program Set Up Time[1]	—	5	—	5	—	µs	—
t_{EP}	Erase Pulse Width[2]	1	1	10	1	10	ms	$CS = V_H$, $\overline{CE} = V_H$
t_{WP}	Write Pulse Width[2]	1	1	10	1	10	ms	$CS = V_H$, $\overline{OE} = V_H$
t_{DS}	Data Set Up Time[1]	200	260	—	260	—	ns	$CS = V_H$, $\overline{OE} = V_H$
t_{DH}	Data Hold Time[1]	200	260	—	260	—	ns	$CS = V_H$, $\overline{OE} = V_H$
t_{ASP}	Address Set Up Time[1]	200	260	—	260	—	ns	$CS = V_H$
t_{AHP}	Address Hold Time[1]	200	260	—	260	—	ns	$CS = V_H$

PROGRAMMING TEST CONDITIONS

Input Levels: V_H = 3.8 Volts, V_L = 0.6 Volts
Timing Measurement Reference Levels: Input = Output = 50%
Input Rise and Fall Times: $t_r = t_f$ = 10ns

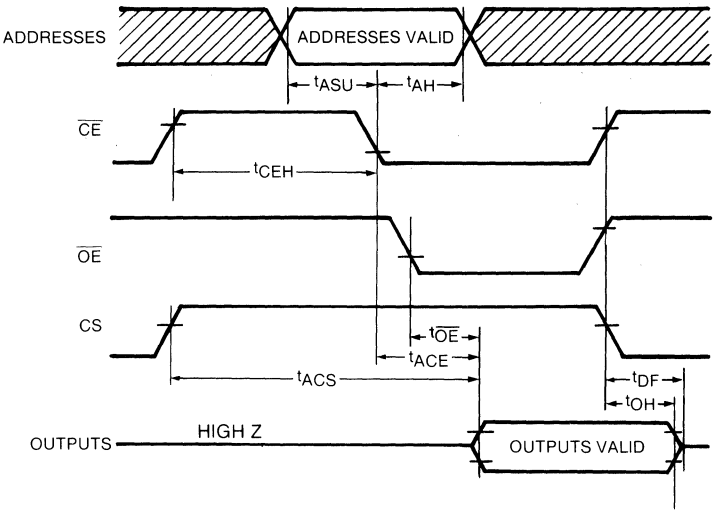
NONVOLATILE CHARACTERISTICS

			HC3104		HI 3104			
		25°C	0°C to +70°C		-40 to + 85°C		UNITS	TEST CONDITIONS
SYMBOL	PARAMETER	TYPICAL[1]	MIN.	MAX.	MIN.	MAX.		
E	Endurance[1,3]	100,000	10,000	—	10,000	—	Cycles/Byte	V_{DD} = 16V $t_{EP} = t_{WP}$ = 1 ms
T_R	Retention [1,4]	—	10	—	10	—	Years	V_{DD} = 0 to 5V

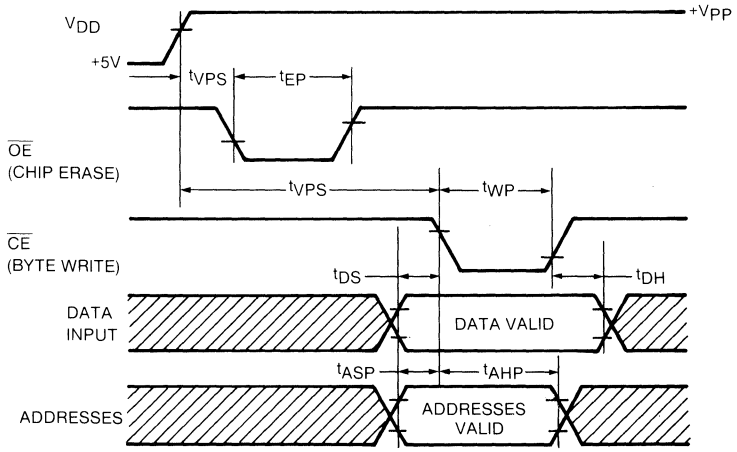
NOTES:
1. This parameter is only sampled and is not 100% tested.
2. Erase and Write time is a function of $+V_{PP}$. See characteristic curve.
3. Endurance is the maximum number of erase/write cycles per byte.
4. Retention is the amount of time the data is retained in the memory without power being supplied.

TIMING WAVEFORMS

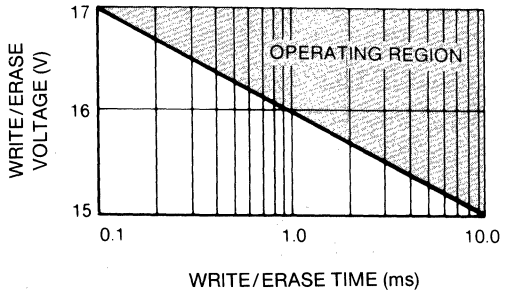
Read



Chip Erase/Byte Write (CS = V_H)



PROGRAM CHARACTERISTICS VS. SUPPLY VOLTAGE



OPERATING MODES

The 3104 has three modes of operation: Read, Block Erase and Byte Write, all enabled when the chip is selected (CS = high). In the Read Mode the 3104 functions as a normal CMOS ROM. When the power input (V_{DD}) is raised to + V_{PP}, the Erase or Program Mode is enabled. In the Erase Mode, all bytes are reset to a logic low (GND). In the Program Mode, bits of the addressed byte may be set to a logic high. An Erase Operation is required before re-writing over previously Programmed data. Detailed procedures for each mode follow:

READ MODE: The circuit reads addresses on the falling edge of $\overline{CE}$ and latches the accessed data until $\overline{CE}$ goes high again. The latched data will appear at the outputs whenever $\overline{CE}$ is low, CS is high, and $\overline{OE}$ is low. A read is initiated with CS going high if $\overline{CE}$ is already low.

ERASE MODE: A Block Erase (all 0's in memory) is accomplished by setting $\overline{CE}$ and $\overline{OE}$ high, raising the positive supply to + V_{PP} and then pulsing $\overline{OE}$ low. When the circuit internally senses the + V_{PP} voltage, it floats the outputs, preventing + V_{PP} level signals from appearing on the data I/O bus. Erasure can also be controlled by CS if $\overline{OE}$ is already low.

WRITE MODE: A write consists of programming 1's into bits that contain a 0. A byte is programmed by setting $\overline{CE}$ and $\overline{OE}$ high, raising the positive supply to + V_{PP}, and pulsing $\overline{CE}$ low. The address lines must have valid data when CE falls and the data to be programmed must be valid on the data I/O lines while $\overline{CE}$ is low. A write operation can follow an Erase while holding + V_{DD} at + V_{PP}, and several or all the bytes can be programmed with + V_{DD} held at + V_{PP}. A write can also be controlled by CS if $\overline{CE}$ is already low.

State	$\overline{CE}$	CS	$\overline{OE}$	V_{DD}	I/O Bus
Standby (unselected)[5]	X	0	X	X	Floating
Standby (unselected)[5]	1	1	1	X	Floating
Standby (selected)	1	1	0	+5	Floating
Read	0	1	0	+5	Floating
Read	0	1	0	+5	Data Out
Erase	1	1	0	+V_{PP}	Floating
Program	0	1	1	+V_{PP}	Data Input
Prohibited State	0	1	0	+V_{PP}	Data Input

NOTE 5: Recommended modes for V_{DD} transition to and from + V_{PP}. V_{DD} should not fall below input levels during transition.

PIN DESCRIPTIONS

MA 0-MA 8: Address inputs which select one of 512 bytes of memory for either Read or Program. The addresses need to be valid only during the falling edge of $\overline{CE}$.

I/O 0-I/O 7: Bidirectional three-state data lines that are Data outputs during Read operation and Data inputs during Program operation.

GND: Negative supply terminal and V = 0 reference.

V_{DD}: Positive supply terminal. It is raised to + V_{PP} for Erase and Program operations.

CS: Chip Select. A Logic Low disables all control inputs in all modes.

$\overline{OE}$: Output Enable. A Logic High disables the Data Output Drivers in normal operation. If V_{DD} = + V_{PP}, a Logic Low causes a block erase. This input is active only when CS operates high.

$\overline{CE}$: Chip Enable. This input causes the circuit to read the addresses at its falling edge for both Read and Program operations. For the Read operation, accessed data is latched and valid as long as $\overline{CE}$ is held at Logic Low. If V_{DD} = + V_{PP}, a Logic Low causes a byte program operation. This input is active only when CS is high.

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Printed in U.S.A. 2/84
Supersedes Previous Data

1024 x 8
CMOS EEPROM

DESCRIPTION

Hughes' H3108 is a CMOS Electrically Erasable and Programmable Read Only Memory (EEPROM) organized 1024 x 8. It is ideal for applications where large amounts of data must occasionally be altered and then stored during power down conditions such as program storage, data tables or data collection.

Data modification is accomplished by first raising the power voltage, V_{DD} to + V_{PP} and selecting the device with CS high (+5V). Then, erasing or writing is controlled with T^2L level signals to the appropriate control inputs $\overline{OE}$ (Erase) and $\overline{CE}$ (Write).

All read operations are performed with V_{DD} at 5 volts. With CS at a high level, the falling edge of the Chip Enable signal ($\overline{CE}$) latches a valid address input and initiates the accessing of data. The information is enabled on the bus when Output Enable ($\overline{OE}$) is a low level.

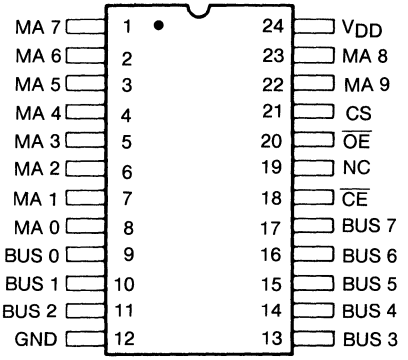
The Chip Select (CS) input for this device is functional in all modes, allowing for chip selection in the Read, Erase, or Write modes independent of $\overline{OE}$ and $\overline{CE}$ inputs.

Hughes' H3108 is available in a 24 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request. Information on Hughes' HB3108, 1K x 8 Military EEPROM is available upon request.

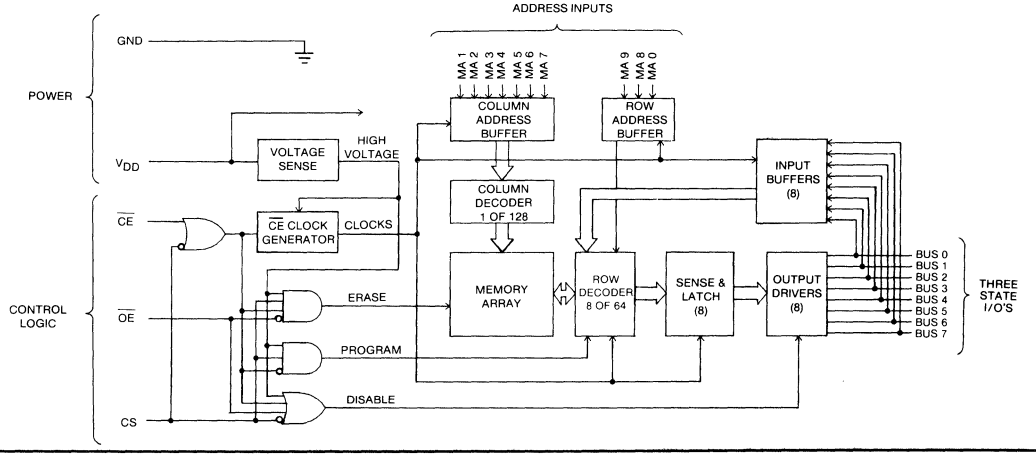
FEATURES

- 1K x 8 CMOS EEPROM
- TTL Level Erase/Byte Write Controls
- 1 ms Erase/Write times
- 10,000 Erase/Write cycles
- 10 year Data Retention
- 3-Line Control Architecture
- 10 µW Typical Quiescent Power Dissipation
- JEDEC Approved 24 pin DIP

PIN CONFIGURATION



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage Range ..... −0.3 to + 18 Volts
(All Voltages referenced to GND terminal)
Input Voltage Range ..... −0.3 to V_{DD} + 0.3 Volts
Storage Temperature Range ..... −65 to + 150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		Read Mode	Write or Erase Mode
V_{DD} Supply Voltage		5 ± 1 Volts	16 ± 1 Volts
Temperature Range	HC3108	0°C to + 70°C	0°C to + 70°C
	HI 3108	−40°C to + 85°C	−40°C to + 85°C

DC OPERATING CHARACTERISTICS

Read: V_{DD} = 6V Unless Otherwise Specified

			HC3108		HI 3108			
		+25°C	0°C to +70°C		-40°C to +85°C			
SYMBOL	PARAMETER	TYPICAL[1]	MIN.	MAX.	MIN.	MAX.	UNITS	TEST A CONDITIONS
I_{CC1}	Standby Current	2	—	100	—	100	µA	V_{IN} = 0 or V_{DD}
I_{CC1A}	Active Current[1]	2	—	100	—	100	µA	$\overline{CE}$ = $\overline{OE}$ = 0
V_{OL}	Output Low Voltage	0.25	—	0.45	—	0.45	V	V_{DD} = 4.75V, I_O = 2.1mA
V_{OH}	Output High Voltage	4.5	2.4	—	2.4	—	V	V_{DD} = 4.75V, I_O = −400µA
V_{IL}	Input Low Voltage	—	—	0.6	—	0.6	V	V_{DD} = 4.75V
V_{IH}	Input High Voltage	—	2.4	—	2.4	—	V	V_{DD} = 5.25V
I_{LI}	Input Leakage Current[1]	± 0.1	—	± 1	—	± 1	µA	V_{IN} = 0 or V_{DD}
I_{LO}	Output Leakage Current[1]	± 0.3	—	± 1	—	± 1	µA	V_O = 0 or V_{DD}

Erase or Write: V_{DD} = 17V Unless Otherwise Specified

			HC3108		HI 3108			
		25°C	0°C to + 70°C		−40°C to +85°C			
SYMBOL	PARAMETER	TYPICAL[1]	MIN.	MAX.	MIN.	MAX.	UNITS	TEST CONDITIONS
I_{CC2}	Prog. Current	3	—	5	—	5	mA	V_{IN} = 0 or V_{DD}
I_{CC2A}	Prog. Current	25	—	30	—	30	mA	V_{IN} = 5V
V_{IL}	Input Low Voltage	—	—	0.6	—	0.6	V	—
V_{IH}	Input High Voltage	—	3.8	—	3.8	—	V	—
I_{LI}	Input Leakage Current[1]	± 0.1	—	± 1	—	± 1	µA	V_{IN} = 0 or V_{DD}
I_{LO}	Output Leakage Current[1]	± 0.3	—	± 1	—	± 1	µA	V_O = 0 or V_{DD}

AC OPERATING CHARACTERISTICS
Read: V_{DD} = 5V Unless Otherwise Specified

			HC3108		HI 3108			
		25°C	0°C to +70°C		−40 to +85°C			TEST
SYMBOL	PARAMETER	TYPICAL[1]	MIN.	MAX.	MIN.	MAX.	UNITS	CONDITIONS
t_{ASU}	Address Set Up Time	0	75	—	75	—	ns	CS = V_H
t_{AH}	Address Hold Time	100	200	—	200	—	ns	CS = V_H
t_{ACE}	Access Time from $\overline{CE}$	500	—	800	—	825	ns	CS = V_H, $\overline{OE}$ = V_L
$t_{\overline{OE}}$	Output Enable Time	250	—	375	—	400	ns	CS = V_H, $\overline{CE}$ = V_L
t_{ACS}	Access Time from CS	550	—	800	—	825	ns	$\overline{CE}$ = V_L, $\overline{OE}$ = V_L
t_{DF}	$\overline{OE}$ to High Impedence	350	—	450	—	475	ns	$\overline{CE}$ = V_L, CS = V_H
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$, or CS which ever occurs first	0	0	—	0	—	ns	—
t_{CEH}	$\overline{CE}$ High Time	0.5	1.4	—	1.4	—	µs	—
I_{CC3}	Dynamic Current	1.0	—	1.2	—	1.2	mA	f = 100KHz

READ TEST CONDITIONS

Output Load: C_L = 50pF
Input Levels: V_H = 2.4 Volts, V_L = 0.45 Volts

Timing Measurement Reference Levels: Input = Output = 50%
Input Rise and Fall Times: $t_r = t_f$ = 10ns

Erase and Write, V_{DD} = 16V Unless Otherwise Specified

			HC3108		HI 3108			
		25°C	0°C to +70°C		−40 to +85°C			TEST
SYMBOL	PARAMETER	TYPICAL[1]	MIN.	MAX.	MIN.	MAX.	UNITS	CONDITIONS
t_{VPS}	Program Set Up Time[1]	—	5	—	5	—	µs	—
t_{EP}	Erase Pulse Width[2]	1	1	10	1	10	ms	CS = V_H, $\overline{CE}$ = V_H
t_{WP}	Write Pulse Width[2]	1	1	10	1	10	ms	CS = V_H, $\overline{OE}$ = V_H
t_{DS}	Data Set Up Time[1]	200	260	—	260	—	ns	CS = V_H, $\overline{OE}$ = V_H
t_{DH}	Data Hold Time[1]	200	260	—	260	—	ns	CS = V_H, $\overline{OE}$ = V_H
t_{ASP}	Address Set Up Time[1]	200	260	—	260	—	ns	CS = V_H
t_{AHP}	Address Hold Time[1]	200	260	—	260	—	ns	CS = V_H

PROGRAMMING TEST CONDITIONS

Input Levels: V_H = 3.8 Volts, V_L = 0.6 Volts

Timing Measurement Reference Levels: Input = Output = 50%
Input Rise and Fall Times: $t_r = t_f$ = 10ns

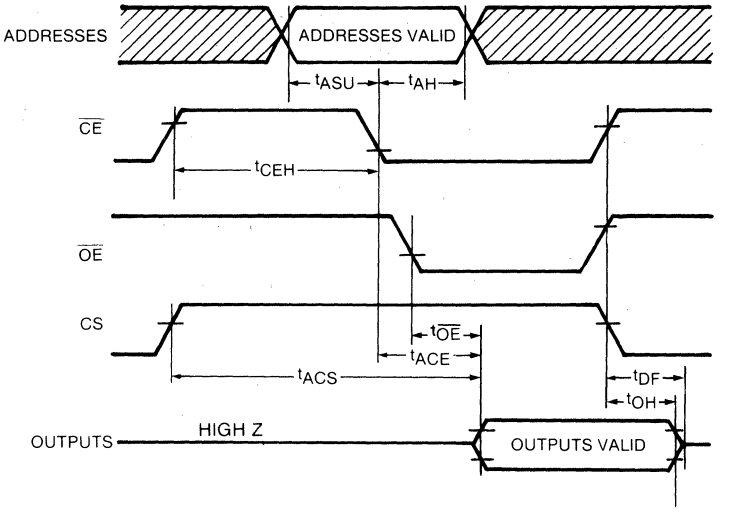
NONVOLATILE CHARACTERISTICS

			HC3108		HI 3108			
		25°C	0°C to +70°C		-40 to + 85°C			TEST
SYMBOL	PARAMETER	TYPICAL[1]	MIN.	MAX.	MIN.	MAX.	UNITS	CONDITIONS
E	Endurance[1,3]	100,000	10,000	—	10,000	—	Cycles/Byte	V_{DD} = 16V t_{EP} = t_{WP} = 1 ms
T_R	Retention [1,4]	—	10	—	10	—	Years	V_{DD} = 0 to 5V

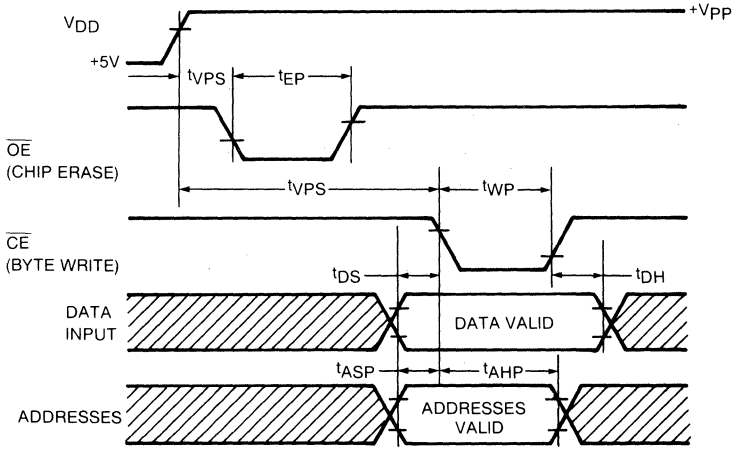
NOTES:
1. This parameter is only sampled and is not 100% tested.
2. Erase and Write time is a function of +V_{PP}. See characteristic curve.
3. Endurance is the maximum number of erase/write cycles per byte.
4. Retention is the amount of time the data is retained in the memory without power being supplied.

TIMING WAVEFORMS

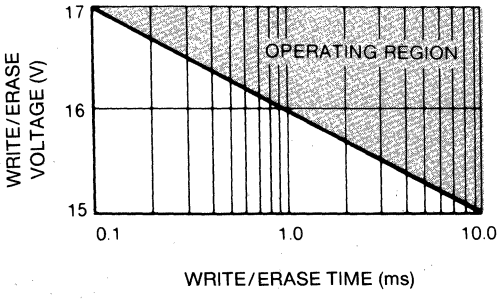
Read



Chip Erase/Byte Write (CS = V_H)



PROGRAM CHARACTERISTICS VS. SUPPLY VOLTAGE



OPERATING MODES

The 3108 has three modes of operation: Read, Block Erase and Byte Write, all enabled when the chip is selected (CS = high). In the Read Mode the 3108 functions as a normal CMOS ROM. When the power input (V_{DD}) is raised to + V_{PP}, the Erase or Program Mode is enabled. In the Erase Mode, all bytes are reset to a logic low (GND). In the Write Mode, bits of the addressed byte may be set to a logic high. An Erase Operation is required before re-writing over previously Programmed data. Detailed procedures for each mode follow:

READ MODE: The circuit reads addresses on the falling edge of $\overline{CE}$ and latches the accessed data until $\overline{CE}$ goes high again. The latched data will appear at the outputs whenever $\overline{CE}$ is low, CS is high, and $\overline{OE}$ is low. A read is initiated with CS going high if $\overline{CE}$ is already low.

ERASE MODE: A Block Erase (all 0's in memory) is accomplished by setting $\overline{CE}$ and $\overline{OE}$ high, raising the positive supply to + V_{PP} and then pulsing $\overline{OE}$ low. When the circuit internally senses the + V_{PP} voltage, it floats the outputs, preventing + V_{PP} level signals from appearing on the data I/O bus. Erasure can also be controlled by CS if $\overline{OE}$ is already low.

WRITE MODE: A Write consists of programming 1's into bits that contain a 0. A byte is written by setting $\overline{CE}$ and $\overline{OE}$ high, raising the positive supply to + V_{PP}, and pulsing $\overline{CE}$ low. The address lines must have valid data when $\overline{CE}$ falls and the data to be programmed must be valid on the data I/O lines while $\overline{CE}$ is low. A Write operation can follow an Erase while holding + V_{DD} at + V_{PP}, and several or all the bytes can be programmed with + V_{DD} held at + V_{PP}. A write can also be controlled by CS if $\overline{CE}$ is already low.

SUMMARY OF OPERATING MODES

State	$\overline{CE}$	CS	$\overline{OE}$	V_{DD}	I/O Bus
Standby (unselected)[5]	X	0	X	X	Floating
Standby (unselected)[5]	1	1	1	X	Floating
Standby (selected)	1	1	0	+5	Floating
Read	0	1	1	+5	Floating
Read	0	1	0	+5	Data Output
Erase	1	1	0	+V_{PP}	Floating
Program	0	1	1	+V_{PP}	Data Input
Prohibited State	0	1	0	+V_{PP}	Data Input

NOTE 5: Recommended modes for V_{DD} transition to and from + V_{PP}. V_{DD} should not fall below input levels during transition.

PIN DESCRIPTIONS

MA 0-MA 9: Address inputs which select one of 1024 bytes of memory for either Read or Program. The addresses need to be valid only during the falling edge of $\overline{CE}$.

BUS 0-BUS 7: Bidirectional three-state data lines that are Data outputs during Read operation and Data inputs during Program operation.

GND: Negative supply terminal and V = 0 reference.

V_{DD}: Positive supply terminal. It is raised to + V_{PP} for Erase and Program operations.

CS: Chip Select. A Logic Low disables all control inputs in all modes.

$\overline{OE}$: Output Enable. A Logic High disables the Data Output Drivers in normal operation. If V_{DD} = + V_{PP}, a Logic Low causes a block erase. This input is active only when CS operates high.

$\overline{CE}$: Chip Enable. This input causes the circuit to read the addresses at its falling edge for both Read and Program operations. For the Read operation, accessed data is latched and valid as long as $\overline{CE}$ is held at Logic Low. If V_{DD} = + V_{PP}, a Logic Low causes a byte program operation. This input is active only when CS is high.

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Printed in U.S.A. 2/84
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256 BIT CMOS EEPROM

DESCRIPTION

Hughes' 3300 is a CMOS Electrically Erasable Programmable ROM (EEPROM), organized as 32 x 8. Read and Write operations are performed with a single 5V power supply using simple TTL level control signals.

Writing data into nonvolatile storage is performed in a similar manner to the write control of a static RAM. A short logic low pulse to the $\overline{WE}$ pin (Write Enable) initiates the byte write operation which is completed with on-chip timing (a separate erase operation is not required). Addresses and data are internally latched to free the system bus for other tasks during the write period.

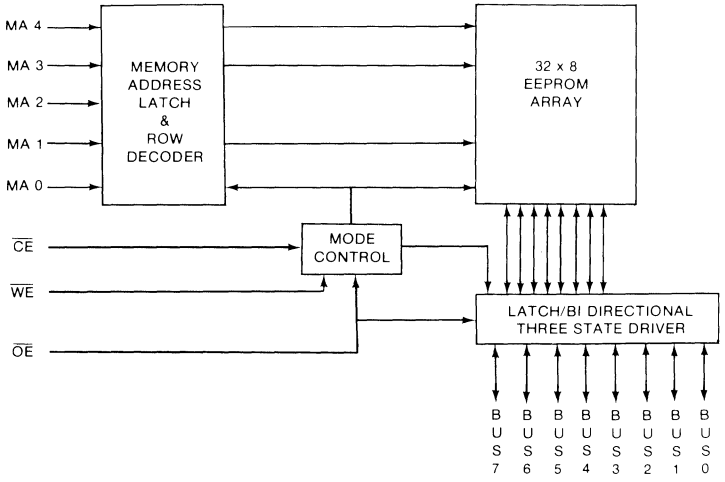
A Read operation is performed by presenting the byte address and enabling the chip with $\overline{CE}$ (Chip Enable) low. The device uses a two-line control architecture, $\overline{CE}$ and $\overline{OE}$ (Output Enable), to eliminate bus contention in a system environment.

The 3300 is available in an 18 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

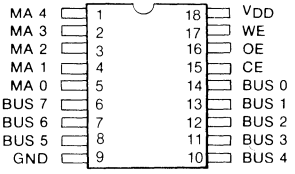
FEATURES

- Byte wide organization (32 x 8)
- Single 5V power supply (Read and Write)
- Very low power dissipation (CMOS)
- Byte programmable (no erase required)
- On chip timing for byte write
- On chip Address & Data latches
- Simple and efficient 3-line control ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$)
- Fast access time: 450ns typical
- Fast Write time: 1 ms typical

BLOCK DIAGRAM



PIN CONFIGURATION



64 x 4 CMOS Nonvolatile RAM

DESCRIPTION

Hughes' 3500 is a CMOS Nonvolatile RAM organized as 64 x 4. The device consists of a conventional static CMOS RAM paralleled by a background Nonvolatile EEPROM array. This combination is useful for applications where the fast data access time and unlimited reprogramming capabilities of RAMs and the nonvolatile data storage of EEPROMs is required; for example, reconfigurable systems or fault protection (without battery back up).

Four modes of operation are provided: Read, Write, Store and Recall. Both Read and Write options are performed as in standard RAMs. A read is initiated by taking Chip Select ($\overline{CS}$) low or by a change of address while $\overline{CS}$ is low. A Write is initiated with $\overline{CS}$ low and pulsing the Write Enable ($\overline{WE}$) low.

Nonvolatile operations: A $\overline{Store}$ pulse transfers all of the data in the RAM cells, in parallel, to the background nonvolatile array. The $\overline{Recall}$ pulse restores this data from the nonvolatile array to the RAM cells.

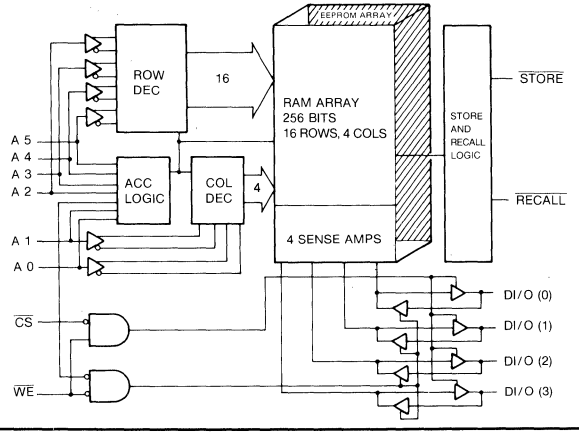
All operations are performed at 5V supply voltage with TTL level data, address and control inputs.

The 3500 is available in an 18 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), or leadless chip carrier (L suffix).

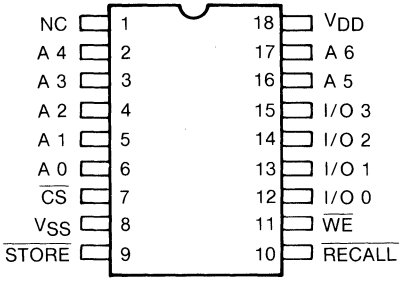
FEATURES

- Nonvolatile Data Storage
- 64 x 4 Bit Organization
- Single 5V operation in all modes
- Fast access/Cycle time
  Access time — 300ns typical (from $\overline{CS}$)
  Cycle time — 500ns typical
- Standard pinout — 18 pin package
- Nonvolatile store operation — 10ms
- Recall operation — 1 µs
- Wide temperature range
  -55°C to + 125°C — Ceramic Package
  -40°C to + 85°C — Plastic Package
- Very Low Current
  Operational — 2ma typical
  Standby — 100 µa typical

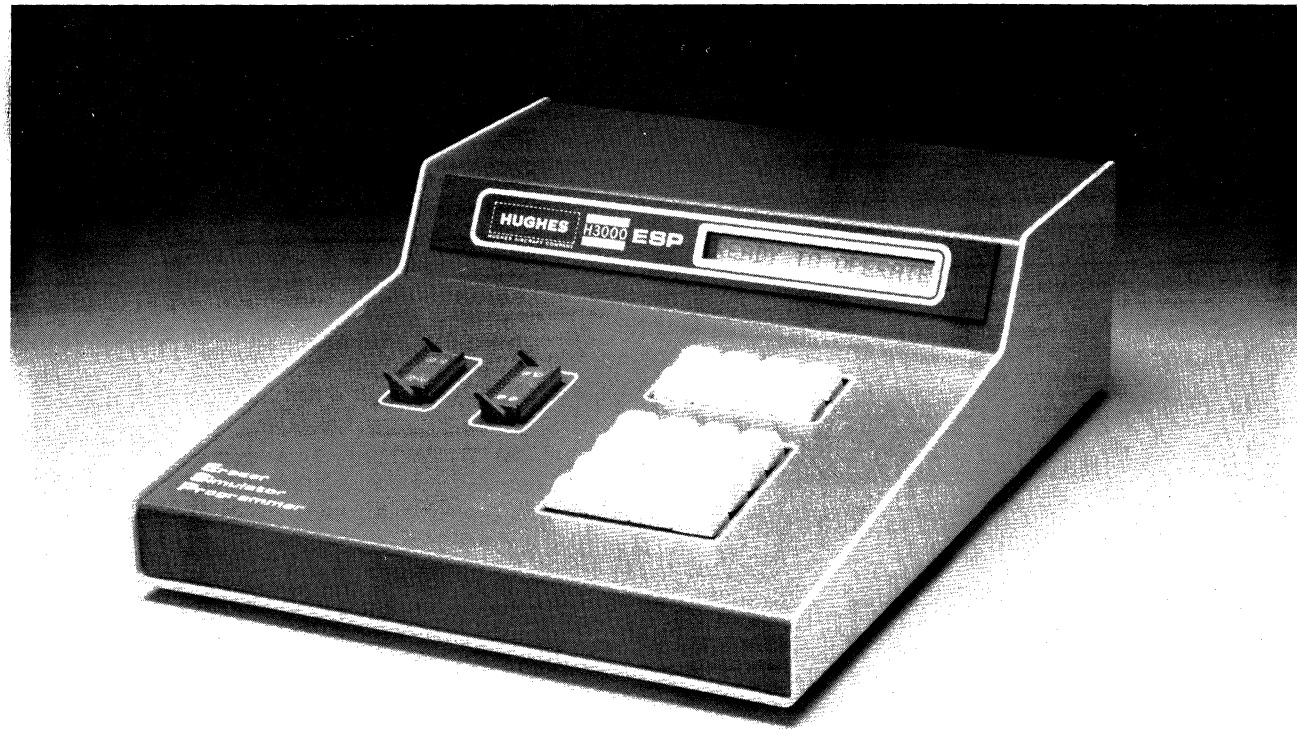
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



ERASER SIMULATOR PROGRAMMER



Hughes H3000 Eraser, Simulator, Programmer

Hughes offers a complete low power unit to evaluate the capabilities of Hughes EEPROM family. The H3000 provides the necessary modes to erase, program, read, copy, simulate, modify, and compare Hughes H 3004, 3008, 3108, 3704, 3708, and the future Hughes Nonvolatile Memories, as well as members of the industry standard 2700* family.

HUGHES FEATURES

Automatic Self Test

To insure proper operation, the unit runs an automatic self-check as power is activated and then displays the results.

Easy to Operate

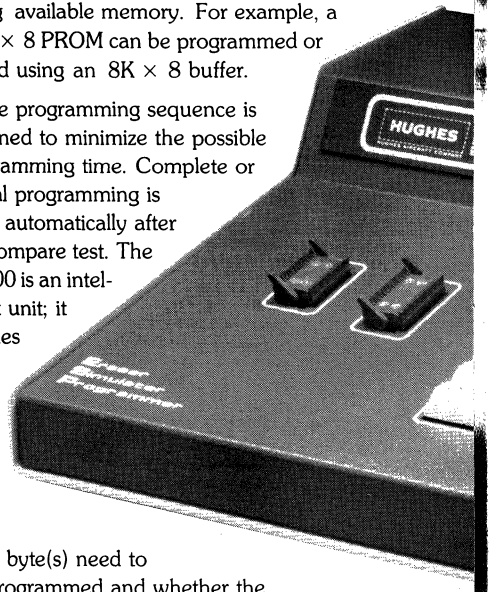
The H3000 unit leads the operator (without the aid of the manual) through each mode of operation by requesting information via prompter messages on the 16 character display and the eight function keys.

Software Controlled Selection

The H3000, a microprocessor controlled unit, requires no personality boards, hardware changes or switch settings for selection of PROM types or data transfer port characteristics. The last selected parameters remain in the memory until they are altered or the power is turned off.

Smart and Adaptive Programming

The H3000 has an 8K × 8 static RAM buffer. The starti address for the buffer is software selectable in 4K range Programming and editing are possible on any PROM by using available memory. For example, a 16K × 8 PROM can be programmed or edited using an 8K × 8 buffer.

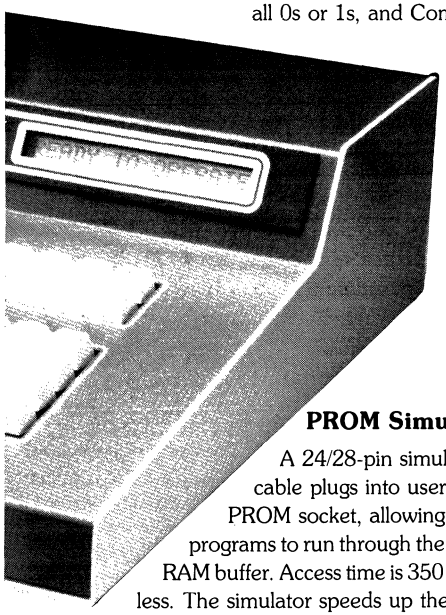


The programming sequence is designed to minimize the possible programming time. Complete or partial programming is done automatically after the compare test. The H3000 is an intelligent unit; it decides what byte(s) need to be programmed and whether the programming can be done without erasure. Also, while programming (on selected PROMs), the H3000 pulses a word for 10ms at a time and tests the word after each pul Once the unit adequately retains the information, it is ov programmed one more time. The unit rejects the PRO more than five pulses are required to program. This sm and adaptive programming sequence saves significant ti in programming any EPROM. The erase function can b enabled to activate automatically in the case of EEPRO when the programming is not possible without erasure. T compare operation is performed at the end of each programming cycle for verification.

*2700 series requires uv-erasure

werful Editor

Edit mode allows very fast scrolling back and forth ugh the entire work space. In addition to the Examine Replace commands, the editor supports many text ing commands such as Move block, Find byte(s), Write all 0s or 1s, and Compare.



PROM Simulator

A 24/28-pin simulator cable plugs into user's PROM socket, allowing his programs to run through the H3000 RAM buffer. Access time is 350 nsec or less. The simulator speeds up the elopment cycle by avoiding the need to erase and ·ogram PROMs.

rial and Parallel I/O

t data transfer in both directions is allowed through an 232C and a parallel port. Start and end addresses the block can be user specified.
1 the serial transfer, baud rate, parity bits/character, etc. keyboard selectable.

ers Application

ers can employ the programmer to support their own lication programs and additional PROMs via a special nmand to the H1802 microprocessor in the unit's fer.

The H3000 can provide a number of useful functions such as an aid in program development and check-out, a functional tester for incoming inspection, a remote programming unit, a field service tool, a production programmer, and many more.

The unique capabilities of the H3000 are established by using Hughes CMOS devices including the 1800 Microprocessor Family, the 8K EEPROM for program storage and an Intelligent LCD Controller/ Driver chip set (H 0550/0551). These latter units allow a very simple interface between the microprocessor and the display.

Product Demonstration and Evaluation

The H3000 also offers a number of programs to demonstrate capabilities of Hughes EEPROM devices, Intelligent LCD Controller/Driver (H 0550/0551) and 1800 Microprocessor Family.

Operators can use resident subroutines to create new programs and apply the capabilities of the H3000 for their needs. ASCII data can be entered or read in the H3000 without having a ASCII keyboard.

Interactive Diagnostics

A series of interactive programs help the user to diagnose a fault in the H3000 if it is suspected that the unit is not functioning properly.

H3000 ESP Specifications

Functions	• PROM selection • Read data into buffer • Send data from buffer • Inspect, change, find data byte(s), move block, scroll • Compare, verify • Clear buffer to zeros or ones • Erase EEPROM • Program PROM partially or fully • Simulate PROM • Special modes to evaluate Hughes EEPROMs, LCD Drivers, and 1802 Microprocessor
PROM Types	• Hughes H 3004, 3008, 3108, 3704, 3708 and future nonvolatile memories; Intel 2704, 2708, 2758, 2716, 2732, 2732A, 2764, 27128 or equivalent; National 27C16, 27C32 or equivalent, Texas Instruments 2532 or equivalent
PROM Sockets	• A 24 pin and a 28 pin (zero insertion force sockets)
Display	• 16 character, dot matrix LCD
RAM Buffer	• 8 K × 8 static RAM
Keyboard	• 16 hexadecimal keys, 8 function keys
Data Transfer (To/From H3000	• Serial — RS232C, parallel — with ready resume handshake Start address and end address of the block can be specified Baud rate 110, 300, 600, 1200, 2400, 4800, 9600 Parity — odd, even, none Bits/character — 7, 8 Stop bits — 1, 2 Delay
Power Requirement	• 100/115/230 VAC, 50/60 Hz
Size (H × W × L)	• 4.5″ × 12″ × 15″
Weight	• 10 lbs.

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Four Digit LCD Driver

DESCRIPTION

Hughes' 0437 is a CMOS/LSI circuit that drives a 4-digit LCD display from multiplexed BCD information. The inputs are four positive true strobe (digit select) signals and four BCD data lines. Such signals are generated by several LSI counting circuits including the Hughes' 4010 and 6010. The input levels are compatible with T²L and NMOS as well as CMOS.

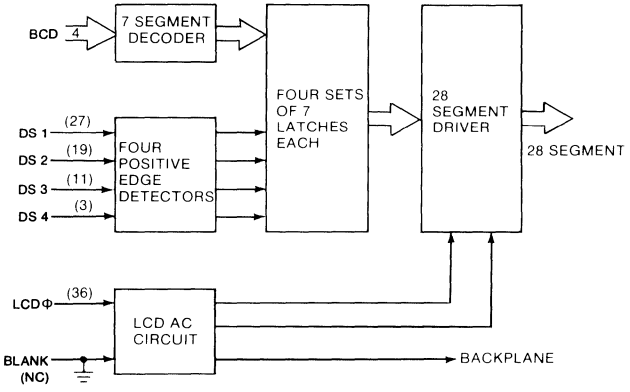
The outputs are four sets of seven segment drive lines with AC waveform and a backplane signal. Input data is loaded into latches upon the positive edge of the appropriate strobe signal. The hexidecimal codes of 0 through 9 give the usual seven segment characters, 15 causes a blank, and 10 through 14 form the letters A, C, d, E, and F. The LCDΦ pin controls an internal oscillator that determines the LCD drive frequency. A capacitor must be attached at this point. The LCDΦ pin can be over driven by an external signal or the backplane signal of another 0437, allowing the use of a display of over four characters. The backplane signal is, thus, the same polarity as the impressed LCDΦ signal.

The 0437 is available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

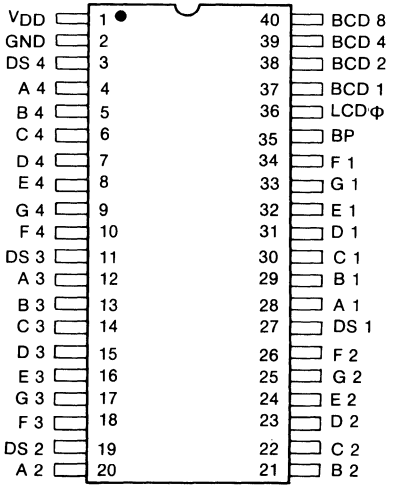
FEATURES

- Drives a 4-digit LCD display
- CMOS construction for:
  - Wide supply voltage range
  - Low power operation
  - High noise immunity
  - Wide temperature range
- CMOS, NMOS, and T²L compatible inputs
- Cascadable for larger displays
- On chip oscillator

BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

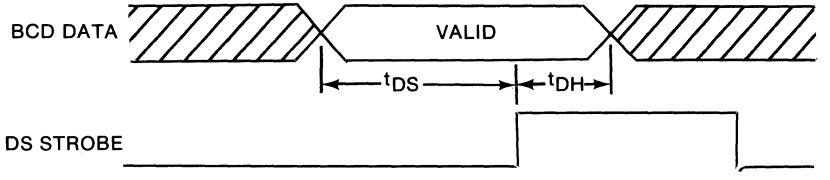
V_{DD} ..... −.3 to + 17V
Inputs..... $+V_{DD}$ −17 to + V_{DD} + .3V
LCDΦ Input ..... −.3 to + V_{DD} + .3V
Power Dissipation 250mW
Operating Temperature
Ceramic Package..... −55 to + 125°C
Plastic Package..... −40 to + 85°C
Storage Temperature..... −65 to + 125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

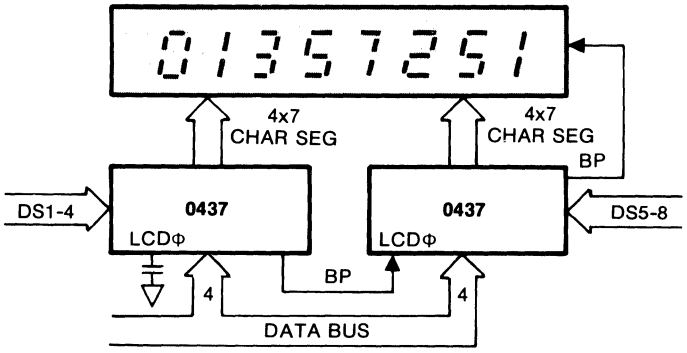
ELECTRICAL CHARACTERISTICS at T_A = +25°C and V_{DD} = ±5 unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		3	10	V
Supply Current	I_{DD1} I_{DD2}	LCDΦ Osc at <15 KHz LCDΦ Driven		65 10	μA μA
Input High Level	V_{IH}		$.5V_{DD}$	V_{DD}	V
Input Low Level	V_{IL}		$+V_{DD}-15$	$.2V_{DD}$	V
Input Current	I_L			5	uA
Input Capacitance	C_I			5	pf
Segment Output Impedance	R_{ON}	I_L = 10μA		50	KΩ
Backplane Output Impedance	R_{ON}			3	KΩ
Strobe Rate	f	25% Duty Cycle	DC	500	KHz
BCD Set-up Time	t_{DS}	BCD Data change to Strobe rising edge	0		nsec
BCD Hold Time	t_{DH}	Strobe rising edge to BCD Change	300		nsec
DS Rise Time	t_R			100	nsec
LCDΦ Input High Level	V_{IN}		$.8V_{DD}$		V
LCDΦ Input Low Level	V_{IL}			$.2V_{DD}$	V
LCDΦ Input Impedance	R_{IN}	Typical	2		MΩ

TIMING DIAGRAMS



TYPICAL SYSTEM INTERCONNECT
(CASCADED TO DRIVE 8 CHARACTERS)



OPERATING NOTES

1. The latches load on the rising edge of Digit Strobe (DS) signals.
2. To cascade units, either connect the Backplane of one chip to LCDΦ of another chip (thus one capacitor provides frequency control for all chips) or connect LCDΦ of all chips to a common driving signal. If the former is chosen, don't tie all backplanes together (just use one of them) and drive LCDΦ with a Backplane output that doesn't go to the actual backplane. This reduces the DC component of driving signals.
3. The supply voltage of the 0437 is equal to half the peak driving voltage of the LCD. If the 0437 supply voltage is less than the swing of the input logic signals, the positive supply leads of the logic circuitry and the 0437 should be tied in common, but not the ground (or negative) supply leads. Be careful that the input level specifications are met.
4. The LCDΦ pin can be used in two modes, driven or oscillating. If the LCDΦ is driven, the backplane will repeat its frequency. If the LCDΦ pin is allowed to oscillate, its frequency is inversely proportional to capacitance and the LCD driving waveforms have a frequency 2^8 slower that the oscillator itself. The relationship is shown graphically.

OPERATING NOTES, cont.

5. Each DS signal loads latches that control 7 outputs, but the assignment of which character in the display corresponds to which DS is arbitrary. The circuit does not have a requirement that certain characters in the display must come from certain output pins.
6. All LCD Output signals are square wave of amplitude equal to the supply voltage. Compared to the backplane signal, on segments are out of phase and off segments are in phase.

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Printed in U.S.A. 8/83
Supersedes Previous Data

Four Digit LCD Decoder/Drivers

DESCRIPTION

Hughes' 7211 devices are configured to drive conventional 4 digit, 7 segment LCD displays. They feature on-chip oscillator, divider chain, backplane driver, and 28 segment drivers. These devices simplify the task of implementing a cost effective alphanumeric 7 segment display for microprocessor systems since they latch data and perform character encoding.

Two input configurations are available. One provides four data bit inputs and four digit select inputs. This configuration (7211-1, 7211-2) is suitable for interfacing with multiplexed BCD or binary output devices such as counters. The microprocessor oriented interface (7211-3, 7211-4) devices provide data input latches and digit select code latches under control of chip select inputs.

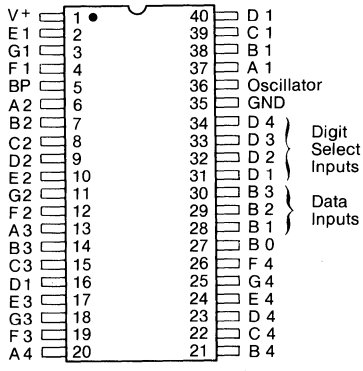
Two different decoder configurations are available. One configuration (7211-1, 7211-3) will decode four bit binary input into a seven segment alphanumeric hexadecimal output. The other (7211-2, 7211-4) versions will provide the output code 0-9, dash, E, H, L, P, blank. Either device will correctly decode BCD to seven segment decimal outputs.

The 7211-1/7211-2/7211-3/7211-4 are available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

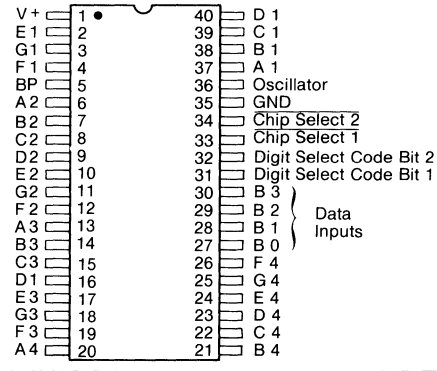
FEATURES

- CMOS Circuitry
  - Wide supply voltage range
  - Low power operation
  - High noise immunity
  - Wide temperature range
- Four digit non-multiplexed 7 segment LCD display outputs with backplane driver
- Complete onboard RC oscillator to generate backplane frequency
- Backplane input/output allows simple synchronization of slave-device segment outputs to a master backplane signal
- 7211-1, 7211-2 provide separate digit select inputs to accept multiplexed BCD input
- 7211-3, 7211-4 provide data and digit select code input latches controlled by chip select inputs to provide direct microprocessor interface.
- 7211-1, 7211-3: decode binary to hexadecimal
- 7211-2, 7211-4: decode binary to code B (0-9, dash, E, H, L, P, blank)

7211-1, 7211-2 PIN CONFIGURATION



7211-3, 7211-4 PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Dissipation[1] ..... 0.5 W at 70°C
Supply Voltage ..... 6.5 Volts
Input Voltage[2] ..... V^+ + 0.3 Volts, Ground − 0.3 Volts
(Any Terminal)
Operating Temperature Range... − 20°C to + 85°C
Storage Temperature Range .... − 55°C to + 125°C
Lead Temperature ..... 300°C
(Soldering 10 sec.)

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

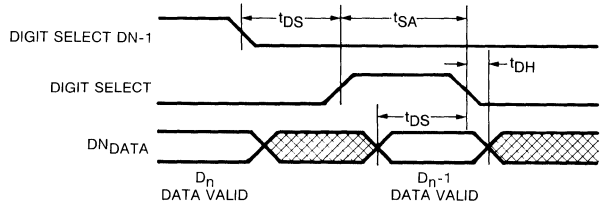
NOTE 1: This limit refers to that of the package and will not be realized during normal operation.

NOTE 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than Ground may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the 7211 devices be turned on first.

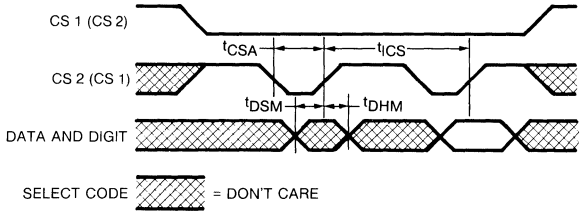
ELECTRICAL CHARACTERISTICS at T_A = Full temperature range. All parameters measured with V + = 5V.

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
Operating Supply Voltage Range	V_{SUPP}		3	5	6	V
Operating Current	I_{OP}	Test circuit, Display blank		10	50	µA
Oscillator Input Current	I_{OSCI}	Pin 36		± 2	± 10	
Segment Rise/Fall Time	t_{RFS}	C_L = 200 pF		0.5		µs
Backplane Rise/Fall Time	t_{RFB}	C_L = 5000 pF		1.5		
Oscillator Frequency	f_{OSC}	Pin 36 Floating		16		KHz
Backplane Frequency	f_{BP}	Pin 36 Floating		125		Hz
Logical "1" input voltage	V_{IH}		3			V
Logical "0" input voltage	V_{IL}				1	
Input Leakage current	I_{ILK}	Pins 27-34		± .01	± 1	µA
Input capacitance	C_{IN}	Pins 27-34		5		pF
BP/Brightness input leakage	I_{BPLK}	Measured at Pin 5 with Pin 36 at GND		± .01	± 1	µA
BP/Brightness input capacitance	C_{BPI}	All Devices		200		pF
AC CHARACTERISTICS - MULTIPLEXED INPUT CONFIGURATION						
Digit Select Active Pulse Width	t_{SA}	Refer to Timing Diagrams	1			µs
Data Setup Time	t_{DS}		500			ns
Data Hold Time	t_{DH}		200			
Inter-Digit Select Time	t_{IDS}		2			µs
AC CHARACTERISTICS - MICROPROCESSOR INTERFACE						
Chip Select Active Pulse Width	t_{CSA}	Other chip select either held active, or both driven together	200			ns
Data Setup Time	t_{DS}		100			
Data Hold Time	t_{DH}		10	0		
Inter-Chip Select Time	t_{ICS}		2			µs

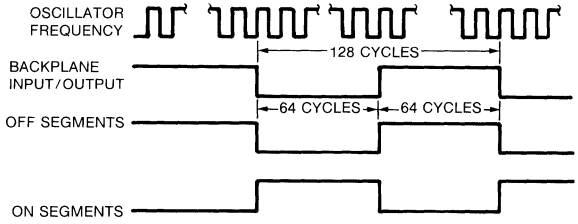
(a) Multiplexed Input Timing



(b) Microprocessor Interface Input Timing



DIGITAL WAVEFORMS



FUNCTIONAL DESCRIPTION

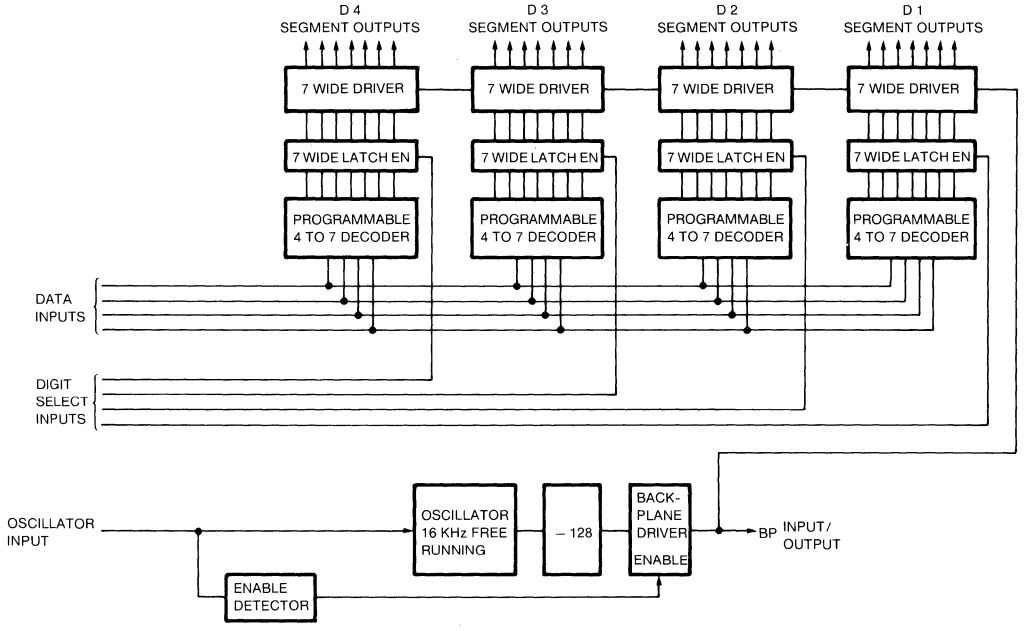
The LCD devices in the 7211-1, 7211-2, 7211-3, 7211-4 family provide outputs suitable for driving conventional four digit by seven segment LCD displays. They include 28 individual segment drivers, a backplane driver, and a self-contained oscillator and divider chain to generate backplane frequency.

The segment and backplane drivers consist of a CMOS inverter, with the n- and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any dc component which could arise from different rise and fall times, and ensures maximum display life.

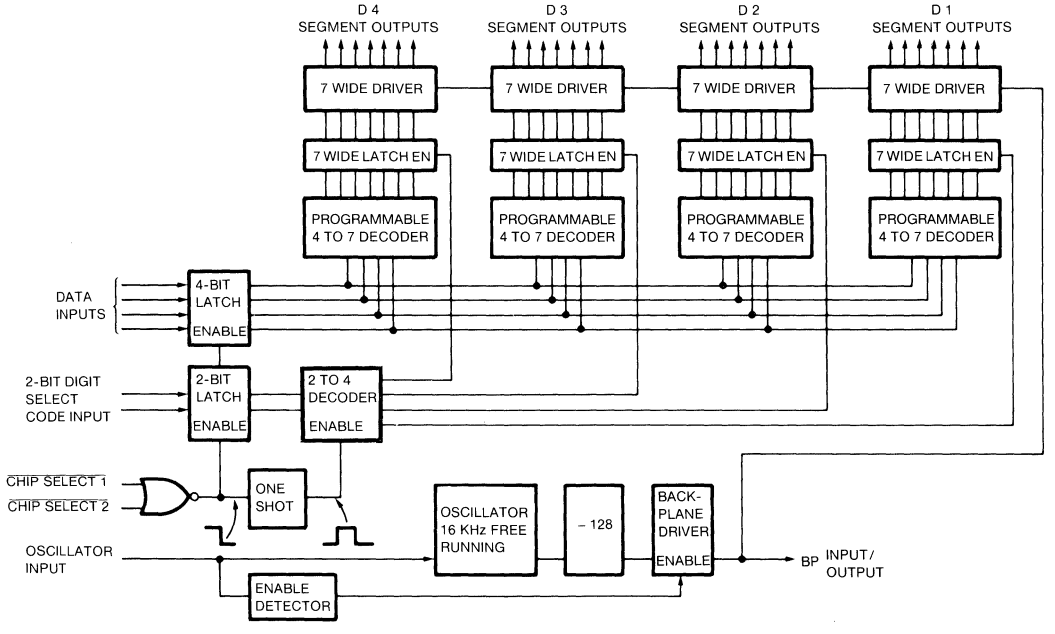
The backplane output devices can be disabled by connecting the oscillator input (pin 36) to the negative supply. This allows the 28 segment outputs to be synchronized directly to a signal input at the BP terminal (pin 5). In this manner, several slave devices may be cascaded to the backplane output of one master device or the backplane may be derived from an external source. This allows the use of displays with more than 4 digits and a single backplane. The limitation on how many devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits, and the effect of that load on the backplane rise and fall times. The backplane driver devices of one device should handle the backplane to a display of 16 one-half-inch characters without the rise and fall times exceeding 5 µs. (i.e. 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the 7211 devices be slaved to it. This external signal should be capable of driving very large capacitive loads with short (1-2 µs) rise and fall times. The maximum frequency for a backplane signal should be about 125Hz although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

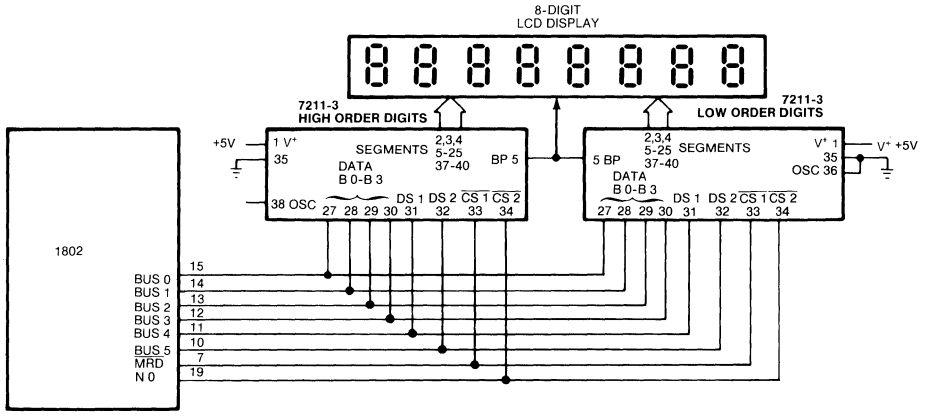
FUNCTIONAL DIAGRAMS

7211-1, 7211-2

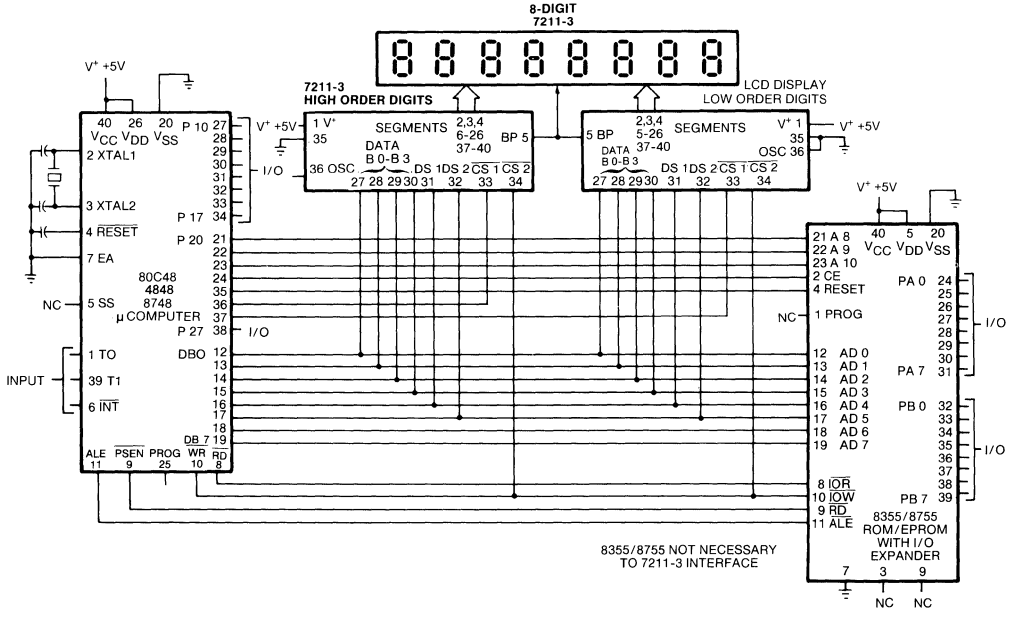


7211-3, 7211-4





(d) 80C48/8048/8748 Microcomputer Interface



The onboard oscillator is designed to free run at approximately 16KHz at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 125Hz with oscillator free-running. The oscillator frequency may be reduced by connecting an external capacitor to the oscillator terminal (pin 36). The oscillator may also be overdriven if desired, although care must be taken to ensure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a d.c. component to the display). This can be done by driving the oscillator input between the positive supply and a level out of the range where the backplane disable is sensed, about one fifth of the supply voltage above the negative supply. Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about 1 microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

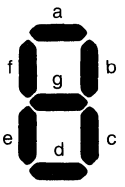
INPUT CONFIGURATION AND OUTPUT CODES

Part Number	Input Configuration	Output Code
7211-1P	Multiplexed 4-bit	Hexadecimal
7211-2P	Multiplexed 4-bit	Code B
7211-3P	Microprocessor Interface	Hexadecimal
7211-4P	Microprocessor Interface	Code B

OUTPUT CODES

BINARY					
B 3	B 2	B 1	B 0	HEXADECIMAL	CODE B
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(BLANK)

SEGMENT ASSIGNMENT



A1, A2, A3, A4 — Outputs directly connected to the "a" segments of LCD
B1, B2, B3, B4 — Outputs directly connected to the "b" segments of LCD
C1, C2, C3, C4 — Outputs directly connected to the "c" segments of LCD
D1, D2, D3, D4 — Outputs directly connected to the "d" segments of LCD
E1, E2, E3, E4 — Outputs directly connected to the "e" segments of LCD
F1, F2, F3, F4 — Outputs directly connected to the "f" segments of LCD
G1, G2, G3, G4 — Outputs directly connected to the "g" segments of LCD

B0, B1, B2, B2 — Data input bits select appropriate output code B0 is the least significant bit
D1, D2, D3, D4 — Digit selects bits (7211-1, 7211-2) D1 is the least significant bit
DS1, DS2 — Two bit digit select code (7211-3, 7211-4) DS 1 is the least significant bit

DS 2	DS 1	
0	0	selects D 4
0	1	selects D 3
1	0	selects D 2
1	1	selects D 1

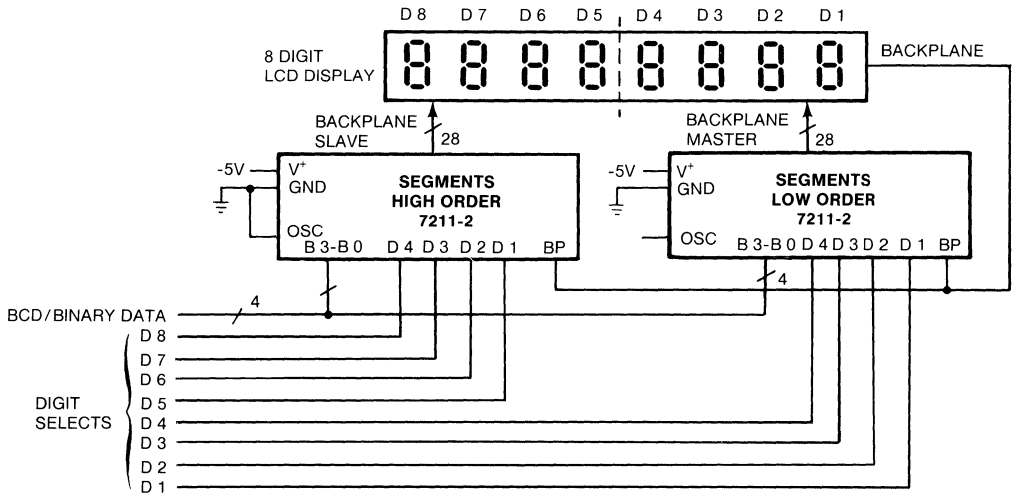
$\overline{CS\,1}$, $\overline{CS\,2}$ — Chip select signals (7211-3, 7211-4): when both $\overline{CS\,1}$, $\overline{CS\,2}$ are low, the data at the Data Inputs (B 0-B 4) and Digit Select Inputs (D 1-D 4) are written into the input latches. On the rising edge of either chip select, the data is decoded and written into the output latches.

OSC — Oscillator input can be floating or tied to external capacitor. When grounded, disables BP output devices, allowing segments to be synched to an external signal input at the BP terminal.

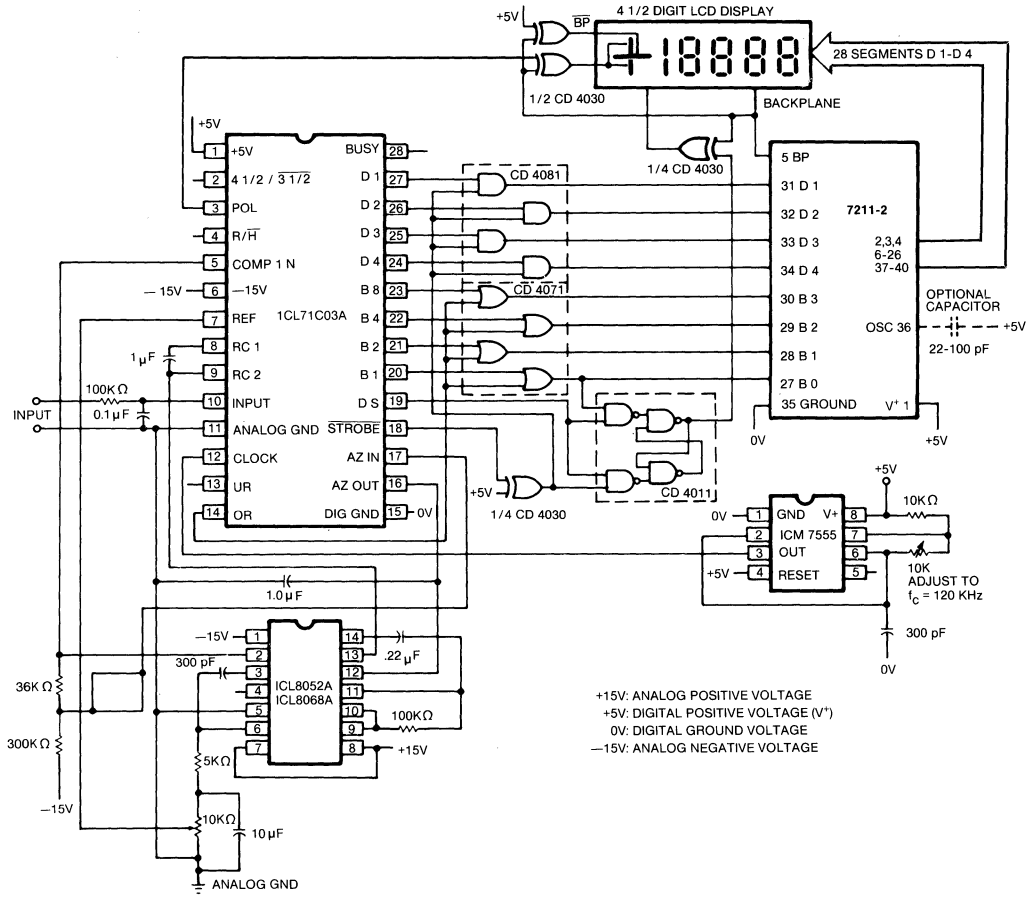
BP — See OSC pin above.

APPLICATIONS:

(a) Cascading and Synchronization:



(b) 4 1/2 Digit LCD DPM With Digit Blanking on Overrange



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Printed in U.S.A. 7/83
Supersedes Previous Data

Serial Input LCD Driver

DESCRIPTION

The 0438A is a CMOS/LSI circuit which drives an LCD display, usually under microprocessor control. The part acts as a smart peripheral, driving up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms.

The 0438A can drive any standard or custom parallel drive LCD display whether it be field effect or dynamic scattering, 7, 9, 14 or 16 segment characters, decimals, leading + or −, or special symbols. Several 0438A's can be cascaded. The AC frequency of the LCD waveforms can be supplied by the user or can be generated by attaching a capacitor to the LCDΦ input, which controls the frequency of an internal oscillator.

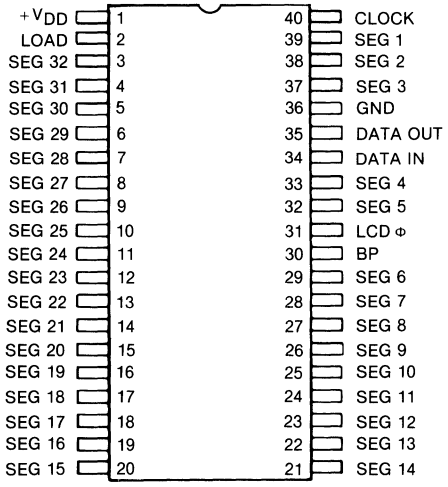
The 0438A can also be used as a column driver in a multiplexed LCD display. In this application, timing and refresh must be supplied externally.

The 0438A is available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available on request.

FEATURES

- Drives up to 32 LCD segments of arbitrary configuration
- CMOS construction for:
  - Wide supply voltage range
  - Low power operation
  - High noise immunity
  - Wide temperature range
- CMOS, NMOS, and T^2L compatible inputs
- Cascadable
- On chip oscillator
- Requires only 3 control lines

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

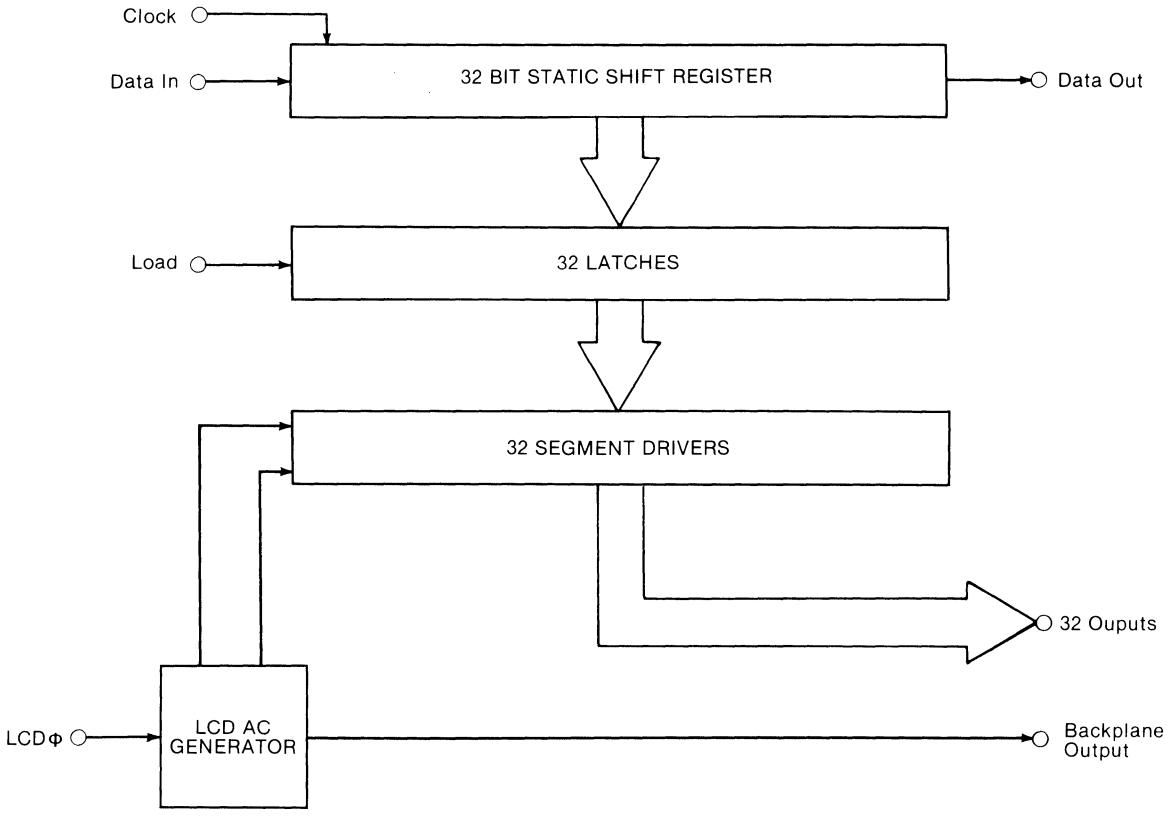
V_{DD} ..... −.3 to + 15V
Inputs (Clk, Data In, Load)..... $+V_{DD}$ − 15 to + V_{DD} + .3V
LCDΦ Input ..... −.3 to + V_{DD} + .3V
Power Dissipation ..... 250 mW
Operating Temperature
Plastic Package ..... −40 to + 85°C
Ceramic Package ..... −55 to +125°C
Storage Temperature ..... −65 to + 150°C

NOTE: Operating the device above the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

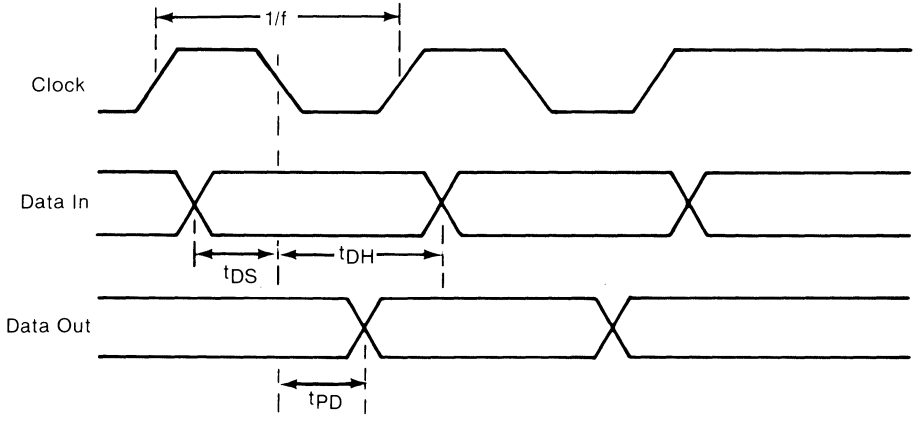
ELECTRICAL CHARACTERISTICS at T_A = +25°C and V_{DD} = 5V unless otherwise noted

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		3	10	V
Supply Current	I_{DD1}	LCD Φ Osc < 15 KHz		60	µA
Quiescent Current	I_Q	V_{DD} = 10V		10	µA
Input High Level (Clock, Data, Load)	V_{IH}		.5V_{DD}	V_{DD}	V
Input Low Level (Clock, Data, Load)	V_{IL}		V_{DD}−15	.2V_{DD}	V
Input Current (Clock, Data, Load)	I_L			5	µA
Input Capacitance (Clock, Data, Load)	C_I			5	pf
Segment Output Impedance	R_{ON}	I_L = 10µA		40	KΩ
Backplane Output Impedance	R_{ON}			3	KΩ
Data-Out Output Impedance	R_{ON}			3	KΩ
Clock Rate	f	50% Duty Cycle, V_{DD} = 10	DC	1.5	MHz
Data Set-up Time	t_{DS}	Data change to Clk falling edge, V_{DD} = 10	150		nsec
Data Hold Time	t_{DH}	V_{DD} = 10	50		nsec
Load Pulse Width	t_{PW}	V_{DD} = 10	175		nsec
Data Out Prop. Delay	t_{PD}	C_L = 55pf, V_{DD} = 10		500	nsec
LCD Φ Input High Level	V_{IN}		.9V_{DD}		V
LCD Φ Input Low Level	V_{IL}			.1V_{DD}	V
LCD Φ Input Current Level	I_L	Driven		10	µA

BLOCK DIAGRAM



TIMING DIAGRAM



OPERATING NOTES

1. The shift register loads, shifts, and outputs on the falling edge of Clock.

2. A logic 1 on Data In causes a segment to be visible.

3. A logic 1 on Load causes a parallel load of the data in the shift register into latches that control the segment drivers.

4. If LCD Φ is driven, it is in phase with the Backplane Output.

5. To cascade units, either connect Backplane of one circuit to LCD Φ of all other circuits (thus one capacitor provides frequency control for all circuits) or connect LCD Φ of all circuits to a common driving signal. If the former is chosen, tie just one Backplane to the LCD and use a different Backplane output to drive the LCD Φ inputs. Either the data can be loaded to all circuits in parallel or Data Out can be connected to Data In to form a long serial shift register.

6. The supply voltage of the 0438A is equal to half the peak driving voltage of the LCD. If the 0438A supply voltage is less than the swing of the controlling logic signals, the positive supply leads of the logic circuitry and the 0438A should be tied in common, not the ground (or negative) supply leads. Be careful that input level specifications are met.

7. The LCD Φ pin can be used in two modes, driven or oscillating. If LCD Φ is driven, the circuit will sense this condition and pass the LCD Φ input to the Backplane output. If the LCD Φ pin is allowed to oscillate, its frequency is inversely proportional to capacitance and the LCD driving waveforms have a frequency 2^8 slower than the oscillator itself. This relationship is shown in Figure 1. The frequency is nearly independent of supply voltage. If LCD Φ is oscillating, it is important to keep coupling capacitance to backplane and segments as low as possible. Similarly, it is recommended that the load capacitance on LCD Φ be as large as is practical.

8. There are two obvious signal races to be avoided in this circuit, (1) changing Data In when Clock is falling, and (2) changing load when Clock is falling.

9. The number of a segment corresponds to how many clock pulses have occurred since its data was present at the input. For example, the data on Seg 19 was input 19 clock pulses earlier.

10. It is acceptable to tie the load line high. In this case the latches are transparent. Also, remote control would only require two signal lines, Clock and Data In.

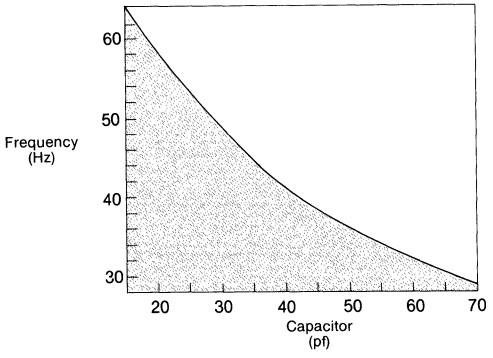


FIGURE 1

HUGHES SOLID STATE PRODUCTS
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Printed in U.S.A.
Rev. N/C ; 5/83
Supersedes Previous Data

Parallel Input Dot Matrix LCD Driver

DESCRIPTION

Hughes' 0488 is a CMOS/LSI circuit that drives a rectangular matrix LCD displays under microcomputer control. The display itself may be a standard x-y array or a custom array that geometrically is not regular at all. Applications include games, bar graphs, and various custom patterns. The 0488 is organized as 16 rows and 16 columns. It will drive an LCD display of up to 16 x 16 directly and can be cascaded for larger displays.

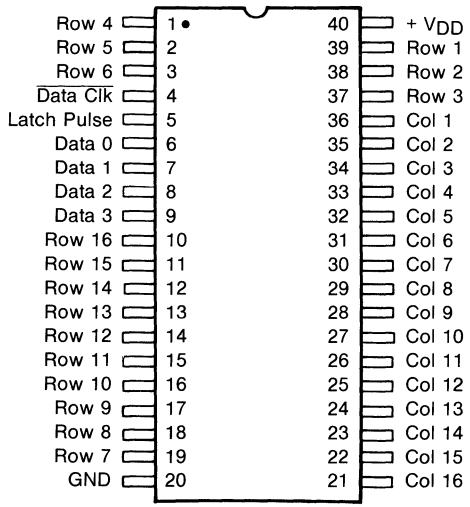
Data is input 4 bit parallel to minimize the time required to load in data. This circuit drives (using a multiplexed scheme) the display with proper voltage level waveforms, but does not handle refresh, character encoding, or AC generation. This results in lower parts cost and greater design flexibility, but puts more burden on the microcomputer.

The 0488 is available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

FEATURES

- Direct drive of matrix LCDs
- Cascadable for large displays
- On chip precision voltage divider
- CMOS construction for:
  - Wide supply voltage range
  - Low power operation
  - High noise immunity
  - Wide temperature range
- CMOS, NMOS, and PMOS compatible inputs
- Architecture allows arbitrary display patterns
- 4 bit parallel input

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

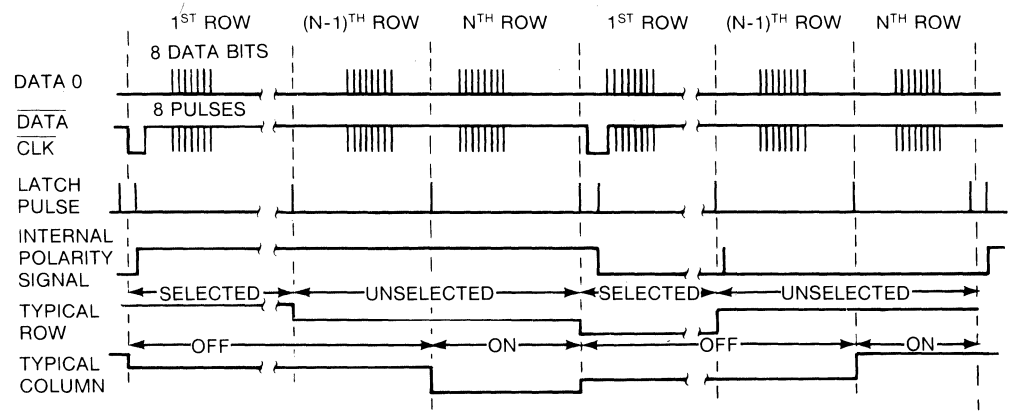
V_{DD} ..... — .3 to + 17 Volts
Inputs ..... + V_{DD} — 17 to + V_{DD} + .3 Volts
Power Dissipation ..... 250 mW
Operating Temperature
Ceramic Package ..... — 55 to + 125°C
Plastic Package ..... — 40 to + 85°C
Storage Temperature ..... — 65 to + 125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

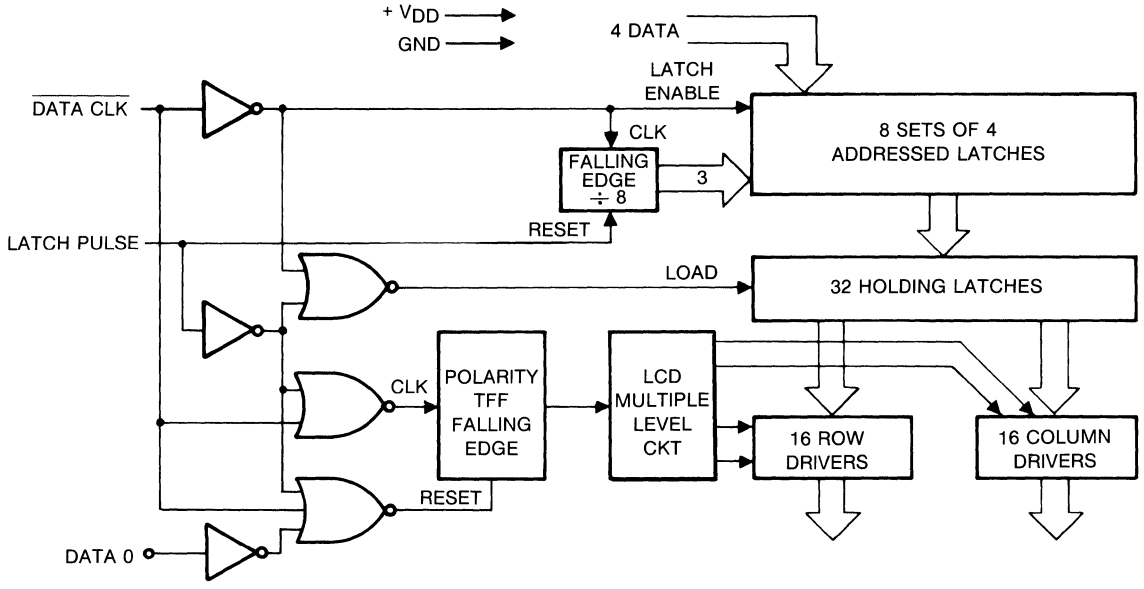
ELECTRICAL CHARACTERISTICS at T_A = + 25°C and V_{DD} = 5V unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		3	8	V
Supply Current	I_{DD}			1.5	mA
Input High Level	V_{IH}		V_{DD}—.5	V_{DD}	V
Input Low Level	V_{IL}		—12	V_{DD}—2	V
Input Leakage	I_L			5	µA
Input Capacitance	C_I			5	pf
Output High Selected	V_{OH}		V_{DD}—.05	V_{DD}	V
Output Low Selected	V_{OL}		0	.05	V
Output High Unselected	$V_{2/3}$		2/3 V_{DD}—.05	2/3 V_{DD} + .05	V
Output Low Unselected	$V_{1/3}$		1/3 V_{DD} —.05	1/3 V_{DD} + .05	V
Row and Column Output Impedence	R_{ON}	I_L = 10µA		15	KΩ
Data in Setup Time	t_{DS}	Data Change to clock fall		500	nsec
Data in Hold Time	t_{DH}	Clock Fall to data change		250	nsec
Latch Pulse Width	t_{PW}			500	nsec

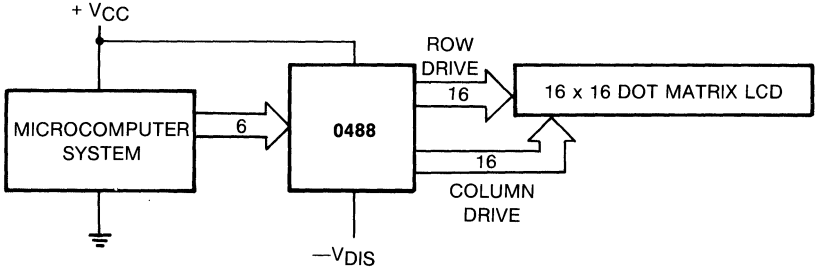
TYPICAL WAVEFORMS



BLOCK DIAGRAM



TYPICAL SYSTEM BLOCK DIAGRAM USING 0488



OPERATING NOTES

1. The addressed latches load when $\overline{\text{Data Clk}}$ is low.
2. A logic 1 on Data In selects a row or causes a segment to be visible.
3. A parallel transfer of data from the addressed latches to the holding latches occurs whenever Latch Pulse is high and $\overline{\text{Data Clk}}$ is high.
4. Output drive polarity is inverted upon the falling edge of Latch Pulse if $\overline{\text{Data Clk}}$ is low.
5. Latch Pulse, when high, resets the ÷ 8 latch address counter.
6. When they are selected Row and Column waveforms are full swing and out of phase with each other. Unselected rows swing from 1/3 to 2/3 of supply out of phase with a selected row waveform. Unselected columns operate analogously.
7. The intended mode of operation is as follows: (see timing diagram)
   A. The Polarity signal (internal to circuit) has a frequency slightly above the flicker rate. 30Hz to 50Hz is adequate.
   B. The Polarity signal should be a square wave of precisely 50% duty cycle to keep DC off the display.
   C. The latch pulse is exactly periodic with a frequency of Polarity frequency x 2 x number of backplanes utilized, plus 2 extra pulses per Polarity period. These extra pulses are associated with a change of Polarity. The state of $\overline{\text{Data Clk}}$ must change from high to low between these first and second closely spaced pulses.
   D. Each time increment contains 8 rising edges of $\overline{\text{Data Clk}}$.
8. To synchronize two circuits driving a large display, set Latch Pulse and Data 0 high with $\overline{\text{Data Clk}}$ low, drop Data 0, then begin normal timing. This initializes the Polarity FF.
9. If supply voltage is altered to optimize LCD contrast or for temperature compensation, it is best to tie all positive supply terminals in common and vary the negative supply. This prevents inadvertently forward biasing diodes.
10. Input order of 0488:

Clk Pulse	1	2	3	4	5	6	7	8
Data 0	R 1	R 5	R 9	R 13	C 1	C 5	C 9	C 13
Data 1	R 2	R 6	R 10	R 14	C 2	C 6	C 10	C 14
Data 2	R 3	R 7	R 11	R 15	C 3	C 7	C 11	C 15
Data 3	R 4	R 8	R 12	R 16	C 4	C 8	C 12	C 16

11. The RMS drive voltages supplied by this IC to an N backplane LCD are as follows:

$$V_{OFF} = V_{DD}/3 \qquad V_{ON} = \frac{V_{DD}}{3}\sqrt{\frac{N+8}{N}}$$

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Printed in U.S.A. 6/83
Supersedes Previous Data

Serial Input Dot Matrix LCD Driver

DESCRIPTION

Hughes' 0538A and 0539A are a set of CMOS/LSI circuits that drive a dot matrix LCD display under microcomputer control. The intended display is a 5 x 7 or 5 x 8 alphanumeric dot matrix with nearly any number of characters. Other matrix displays, such as games and custom arrays, could also be driven by this set of circuits.

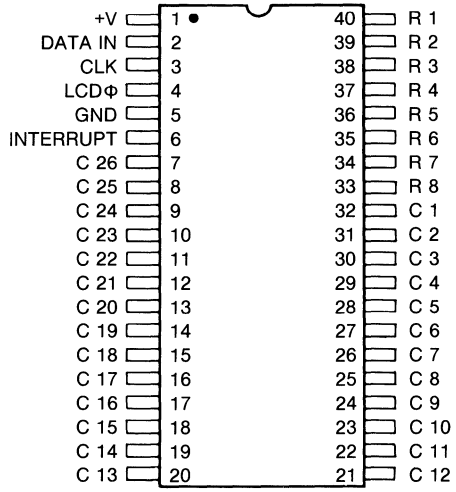
The 0538A is organized as 8 rows x 26 columns, and thus can handle up to five characters by itself. The 0539A is organized as 0 rows x 34 columns and is used in addition to the 0538A when more than 26 columns are required. Data is serially input to maximize the number of output pins and minimize the number of control pins. This circuit set drives (using a multiplexed scheme) the display with proper voltage level AC waveforms, but does not handle refresh or character encoding. This results in lower parts cost and greater design flexibility, but puts more burden on the microcomputer.

The 0538A and 0539A are available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

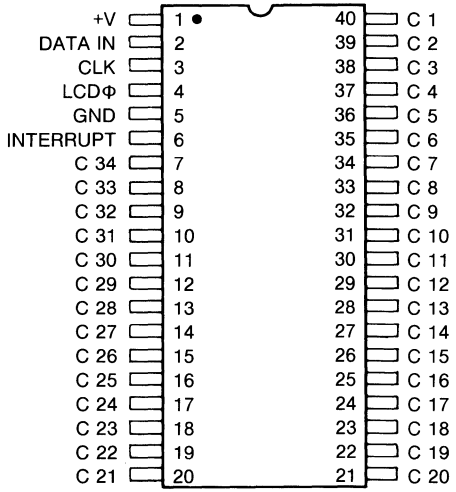
FEATURES

- Direct drive of matrix LCDs
- Cascadable for larger displays
- On chip oscillator
- CMOS construction for:
  - Wide supply voltage range
  - Low power operation
  - High noise immunity
  - Wide temperature range
- CMOS, NMOS, and T^2L compatible inputs
- Requires only 3 control lines
- Flexible organization allows arbitrary display patterns
- Interrupt output to request data from microcomputer

0538A PIN CONFIGURATION



0539A PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

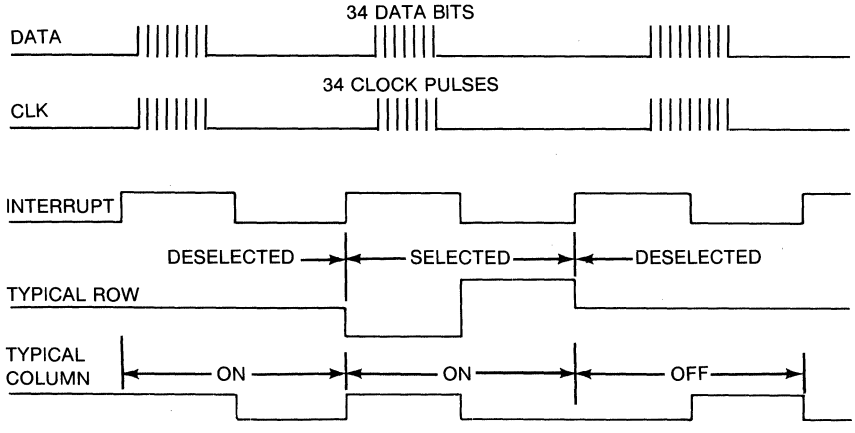
V_{DD} ..... — .3 to + 15 volts
Inputs ..... + V_{DD} — 17 to + V_{DD} + .3 volts
Power Dissipation ..... 250 mW
Operating Temperature
Ceramic Package ..... — 55 to + 125°C
Plastic Package ..... — 40 to + 85°C
Storage Temperature ..... — 65 to + 125°C

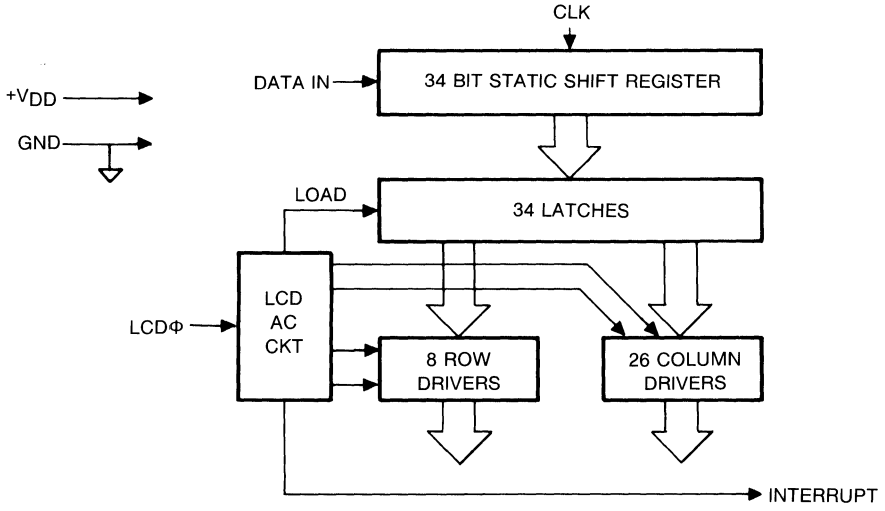
Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS at T_A = +25° and V_{DD} = 5V unless otherwise noted.

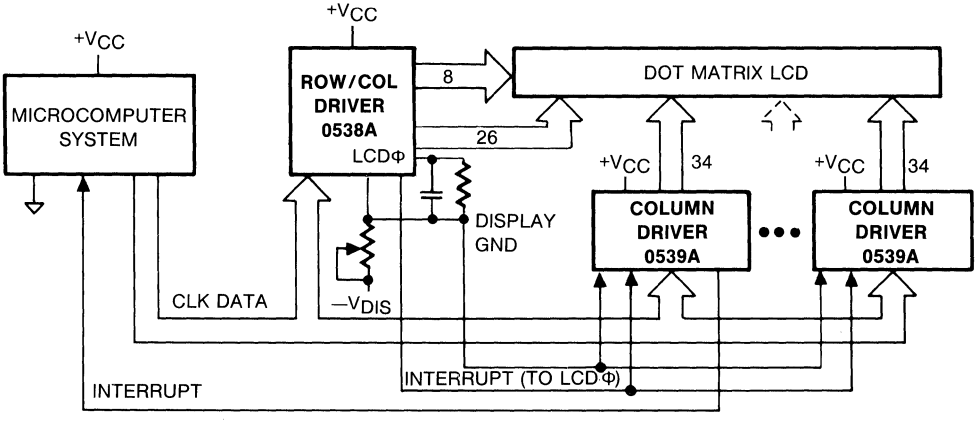
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		3	10	V
Supply Current	I_{DD}			750	µA
Input High Level	V_{IH}		.8 V_{DD}	V_{DD}	V
Input Low Level	V_{IL}		V_{DD}—15	.5V_{DD}	V
Input Leakage	I_L			5	µA
Input Capacitance	C_I			5	pf
Row and Column Output Impedance	R_{ON}	I_L = 10 µA		40	KΩ
Interrupt Output Impedence	R_{ON}	I_L = 100 µA		3	KΩ
Clock Rate	f		DC	1.5	MHz
Data in Setup Time	t_{DS}	Data change to clock fall	300		nsec.
Data in Hold Time	t_{DH}	Clock fall to data change	100		nsec.
LCDΦ to Interrupt Output Delay	t_D		600		nsec.
LCDΦ High Level	V_{IH}		.9V_{DD}	V_{DD}	V
LCDΦ Low Level	V_{IL}		0	.1V_{DD}	V
LCDΦ Input Impedance	R_{IN}		1	3	MΩ
DC Offset Voltage, Any Display Element	V_{OFF}			15	mV
Row Output High	V_{OH}	Typical	V_{DD}		V
Row Output Low	V_{OL}	Typical	0		V
Row Output Unselected	V_{OM}	Typical	.5V_{DD}		V
Column Output High	V_{OH}	Typical	.68V_{DD}		V
Column Output Low	V_{OL}	Typical	.32V_{DD}		V

TYPICAL WAVEFORMS

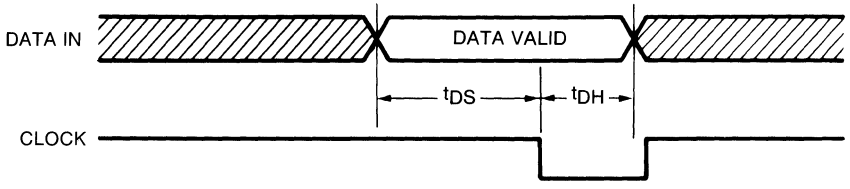




TYPICAL SYSTEM BLOCK DIAGRAM



TIMING DIAGRAM



OPERATING NOTES

1. The Shift register loads and shifts on the falling edge of clock.
2. A logic 1 on Data In causes a segment to be visible.
3. A parallel transfer of data from the shift register to the latches occurs upon the rising edge of Interrupt Output.
4. Row waveforms are out of phase with Interrupt Output if selected and at midpoint voltage otherwise. Levels are V_{DD}, 0, and $V_{DD}/2$.
5. Column waveforms are in phase with Interrupt Output if selected and out of phase if not selected. Levels are .32 V_{DD} and .68 V_{DD}.
6. The intended mode of operation is as follows:
   a. Interrupt Output frequency is the minimum no flicker frequency (> 30Hz) times the number of backplanes utilized.
   b. Interrupt Output is exactly 50% duty cycle (to keep DC off the display) and is synchronized with loading the data from shift register to latches.
   c. In between each Interrupt Output rising edge, serial data is loaded for the next row to await the next Interrupt Output rising edge, which causes parallel transfer from shift register to display latches.
   d. The Interrupt Output goes to the microcomputer and is treated as a refresh request, or else the microcomputer drives the LCDΦ input with 50% duty cycle.
   e. Backplanes are addressed sequentially and individually.
7. The LCDΦ pin can be used in two modes. If LCDΦ is driven, the Interrupt Output will follow it. LCDΦ will also oscillate if a resistor and capacitor are connected in parallel to ground. The resistor value should be at least 1MΩ. The approximate relationship is $f_{out} = \frac{1}{RC}$, which appears at Interrupt Output.
8. To cascade and synchronize several circuits, either connect Interrupt Output of one circuit to LCDΦ of all other circuits (thus one oscillator provides frequency control for all circuits) or connect LCDΦ of all circuits to a common driving signal. Then connect all clock lines together to the clock signal and connect each Data In to a different line of the data bus, allowing a parallel loading of all circuits' serial data. It is also possible to tie all data lines together and drive each clock individually like a chip select.
9. There are two obvious signal races to be avoided.
   a. Changing data when clock is falling, and
   b. Allowing Interrupt Output rising edge to be very close to clock falling edge.
10. If supply voltage is altered to optimize LCD contrast or for temperature compensation, it is best to tie all positive supply terminals in common and vary the negative supply. This prevents inadvertently forward biasing diodes.
11. Output locations correspond to a clockwise advancing shift register, thus R 1 is the last data loaded and C 30 is the first data loaded.
12. The RMS voltages this circuit delivers to individual LCD pixels depends on V_{DD} and the number of backplanes (N) used according to the following equations:

$$V_{OFF} = V_{DD}\sqrt{\frac{.0324\,N + .07}{N}}$$

$$V_{ON} = V_{DD}\sqrt{\frac{.0324\,N + .43}{N}}$$

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Printed in U.S.A. 6/83
Supersedes Previous Data

Serial Input Dot Matrix LCD Driver

DESCRIPTION

Hughes' 0540 is a CMOS/LSI circuit that drives rectangular matrix LCD displays under microcomputer control. The display itself may be a standard x-y array or a custom array that geometrically is not regular at all. Applications include games, bar graphs, and various custom patterns.

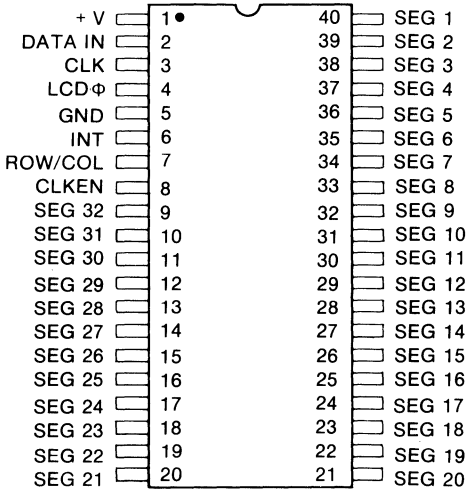
The 0540 can be externally programmed as either 32 rows or 32 columns, under control of the Row/Col pin. Thus, two 0540s with opposite selections can drive a 32 x 32 display. Data is serially input to maximize the number of output pins and minimize the number of control pins. This circuit set could be referred to as a dumb driver because it drives (using a multiplexed scheme) the display with proper voltage level AC waveforms, but does not handle refresh or character encoding. This results in lower parts cost and greater design flexibility, but puts more burden on the microcomputer.

The 0540 is available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

FEATURES

- Direct drive of matrix LCDs
- Cascadable for larger displays
- On chip oscillator
- CMOS construction for:
  - Wide supply voltage range
  - Low power operation
  - High noise immunity
  - Wide temperature range
- CMOS, NMOS, and T^2L compatible inputs
- Requires only 3 control lines
- Flexible organization allows arbitrary display patterns
- Interrupt Output to request data from microcomputer

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

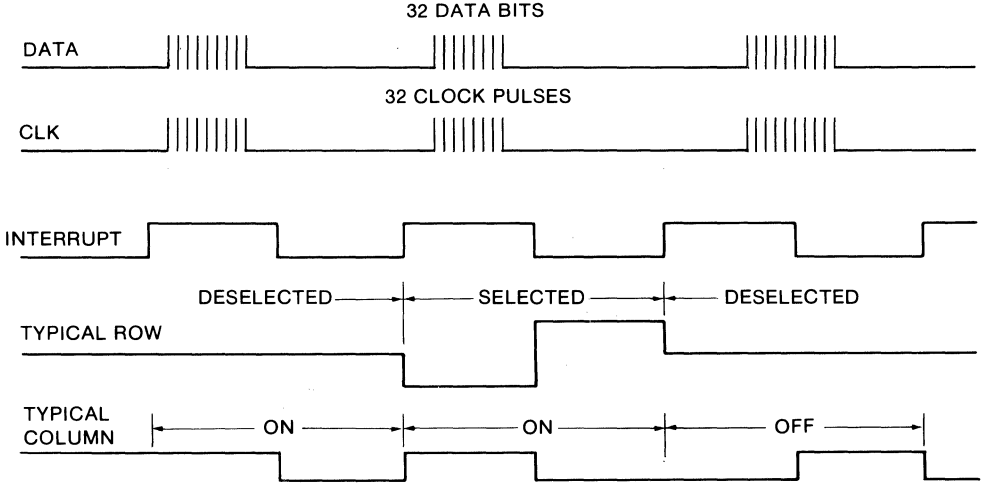
V_{DD} ..... −.3 to +15 volts
Inputs ..... $+V_{DD}$ −17 to $+V_{DD}$ + .3 volts
Power Dissipation ..... 250 mW
Operating Temperature
  Ceramic Package ..... −55 to +125°C
  Plastic Package ..... −40 to +85°C
Storage Temperature ..... −65 to +125°C

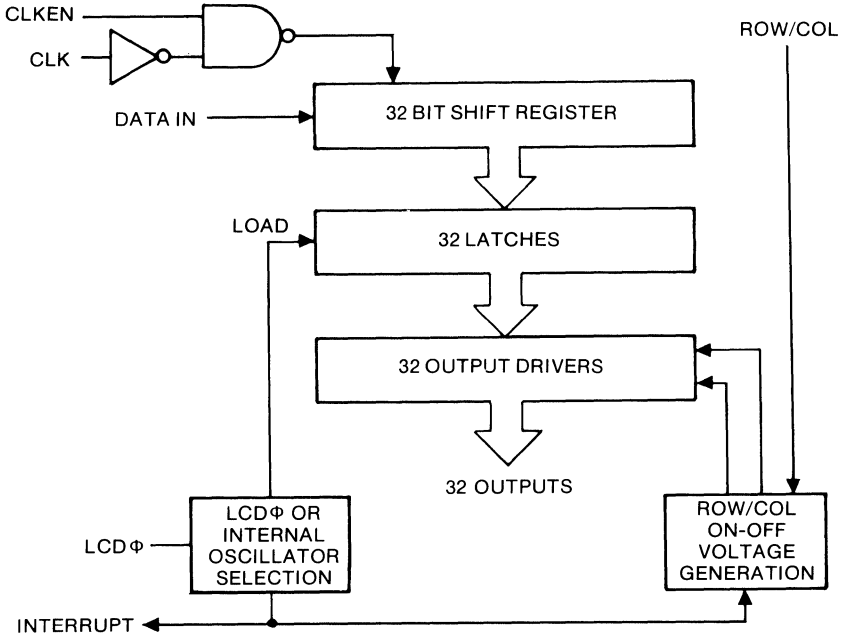
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS at T_A = +25° C and V_{DD} = 5V unless otherwise noted.

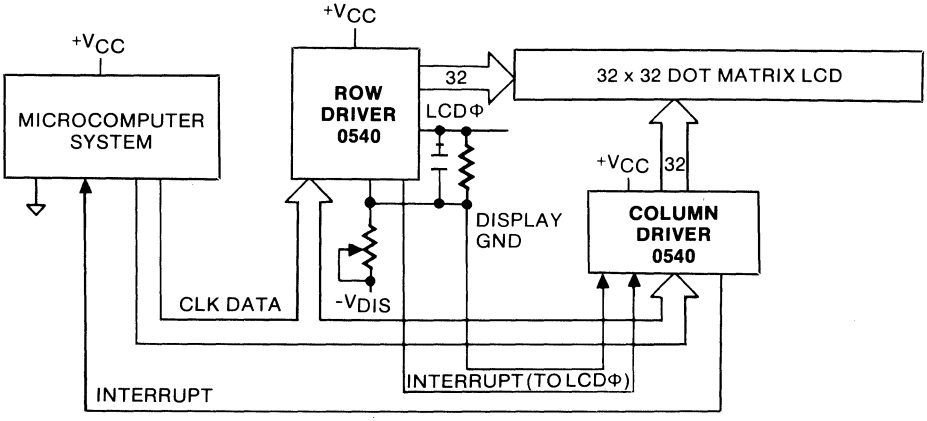
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		3	12	V
Supply Current	I_{DD}			750	µA
Input High Level	V_{IH}		.75V_{DD}	V_{DD}	V
Input Low Level	V_{IL}		V_{DD}−15	.25V_{DD}	V
Input Leakage	I_L			5	µA
Input Capacitance	C_I			5	pf
Row Output High	V_{OH}		V_{DD}−.05	V_{DD}	V
Row Output Low	V_{OL}		0	.05	V
Row Output Unselected	V_{OM}		.5V_{DD}−.05	.5V_{DD}+.05	V
Column Output High	V_{OH}		.68V_{DD}−.05	.68V_{DD}+.05	V
Column Output Low	V_{OL}		.32V_{DD}−.05	.32V_{DD}+.05	V
Row and Column Output Impedance	R_{ON}	I_L = 10µA		40	KΩ
Interrupt Output Impedance	R_{ON}	I_L = 100µA		3	KΩ
Clock Rate	f		DC	1.5	MHz
Data in Setup Time	t_{DS}	Data change to clock fall	300		nsec.
Data in Hold Time	t_{DH}	Clock fall to data change	100		nsec.
LCDΦ High Level	V_{IH}		.9V_{DD}	V_{DD}	V
LCDΦ Low Level	V_{IL}		0	.1V_{DD}	V
LCDΦ Input Impedance	R_{IN}		1	3	MΩ

TYPICAL WAVEFORMS





TYPICAL SYSTEM BLOCK DIAGRAM



OPERATING NOTES

1. The Shift register loads and shifts on the falling edge of the clock.
2. A logic 1 on Data In causes a segment to be visible.
3. A parallel transfer of data from the shift register to the latches occurs upon the rising edge of Interrupt Output.
4. Row waveforms are out of phase with the Interrupt Output if selected and at midpoint voltage otherwise. Levels are V_{DD}, 0, and $V_{DD}/2$. Selection of the 0540 as a row driver is accomplished by V_{CC} on pin 7.
5. Column waveforms are in phase with the Interrupt Output selected and out of phase if not selected. Levels are .32 V_{DD} and .68 V_{DD}. Selection of the 0540 as a column driver is accomplished by V_{SS} on pin 7.
6. The intended mode of operation is as follows:
   a. Interrput Output frequency is the minimum no flicker frequency (> 30Hz) times the number of backplanes utilized.
   b. Interrupt Output is exactly 50% duty cycle (to keep DC off the display) and is synchronized with loading the data from the shift register to latches.
   c. In between each Interrupt Output rising edge, serial data is loaded for the next row to await the next Interrupt Output rising edge, which causes parallel transfer from shift register to display latches.
   d. The Interrupt Output goes to the microcomputer and is treated as a refresh request, or else the microcomputer drives the LCDΦ input with 50% duty cycle.
   e. Backplanes are addressed sequentially and individually.
7. The LCDΦ pin can be used in two modes. If LCDΦ is driven, the Interrput Output will follow it. LCDΦ will also oscillate if a resistor and capacitor are connected in parallel to ground. The resistor value should be at least 1 MΩ. The approximate relationship is $f_{out} = \frac{1}{RC}$, which appears at Interrput Output.
8. To cascade and synchronize several circuits, either connect Interrupt Output of one circuit to LCDΦ of all other circuits (thus one oscillator provides the frequency control for all circuits) or connect LCDΦ of all circuits to a common driving signal. Then connect all clock lines together to the clock signal and connect each Data In to a different line of the data bus, allowing a parallel loading of all the circuits' serial data. It is also possible to tie all data lines together and drive each clock individually like a chip select. Another alternative is to use the clock enable to allow reading data into specific circuits.
9. There are two obvious signal races to be avoided:
   a. Changing data when the Clock is falling, and
   b. Allowing Interrupt Output rising edge to be very close to clock falling edge.
10. If supply voltage is altered to optimize LCD contrast or for temperature compensation, it is best to tie all positive supply terminals in common and vary the negative supply. This prevents inadvertently forward biasing diodes.
11. Output locations correspond to a clockwise advancing shift register, thus Seg 1 is the last data loaded and Seg 32 is the first data loaded.
12. If the N backplanes are utilized, this IC drives the LCD with the following RMS voltages:

$$V_{OFF} = V_{DD}\sqrt{\frac{.0324\,N + .07}{N}}$$

$$V_{ON} = V_{DD}\sqrt{\frac{.0324\,N + .43}{N}}$$

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Printed in U.S.A. 6/83
Supersedes Previous Data

Parallel Input Dot Matrix LCD Driver

DESCRIPTION

Hughes' 0541 and 0542 are a set of CMOS/LSI circuits which drive a dot matrix LCD display under microcomputer control. The intended display is a 5 x 7 or 5 x 8 alphanumeric dot matrix with nearly any number of characters. Other matrix displays, such as games and custom arrays, could also be driven by this set of circuits.

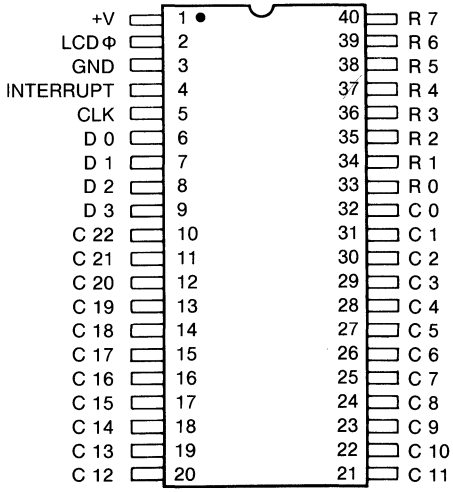
The 0541 is organized as 8 rows x 23 columns, and thus can handle up to four characters by itself. The 0542 is organized as 0 rows x 32 columns and is used in addition to the 0541 when more than 23 columns are required. Data is input 4 bit parallel to minimize the time required to load in data. This circuit drives (using a multiplexed scheme) the display with proper voltage level AC waveforms, but does not handle refresh or character encoding. This results in lower parts cost and greater design flexibility, but puts more burden on the microcomputer.

The 0541 and 0542 are available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

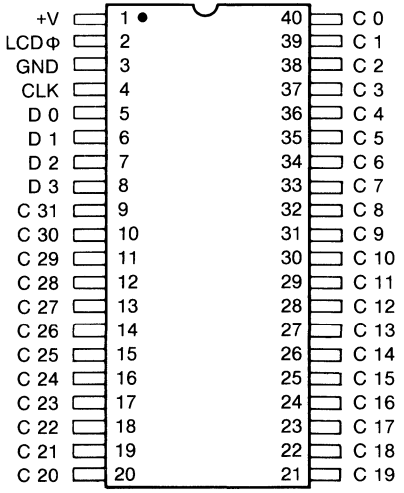
FEATURES

- Direct drive of matrix LCDs
- Cascadable for larger displays
- On chip oscillator
- CMOS construction for:
  - Wide supply voltage range
  - Low power operation
  - High noise immunity
  - Wide temperature range
- CMOS, NMOS, and PMOS compatible inputs
- Flexible organization allows arbitrary display patterns
- Interrupt Output to request data from microcomputer

0541 PIN CONFIGURATION



0542 PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

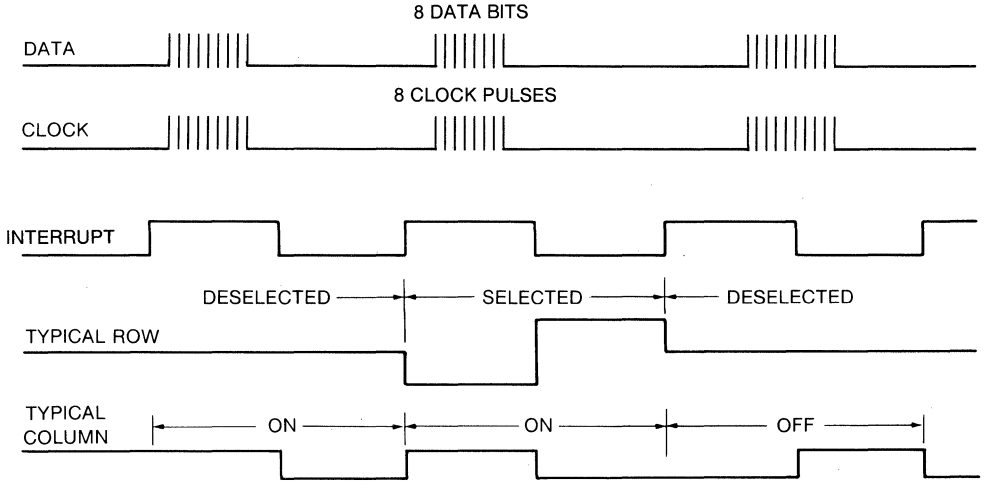
V_{DD} ..... — .3 to + 17 volts
Inputs ..... + V_{DD} — 17 to + V_{DD} + .3 volts
Power Dissipation ..... 250 mW
Operating Temperature
Ceramic Package ..... — 55 to + 125°C
Plastic Package ..... — 40 to + 85°C
Storage Temperature ..... — 65 to + 125°C

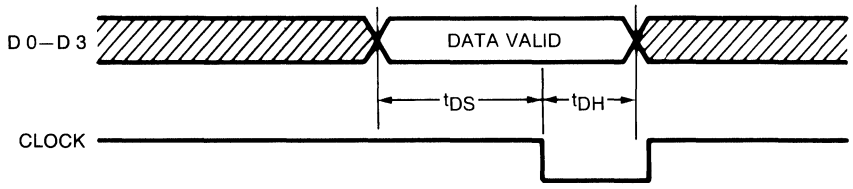
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS at T_A = + 25°C and V_{DD} = 5V unless otherwise noted.

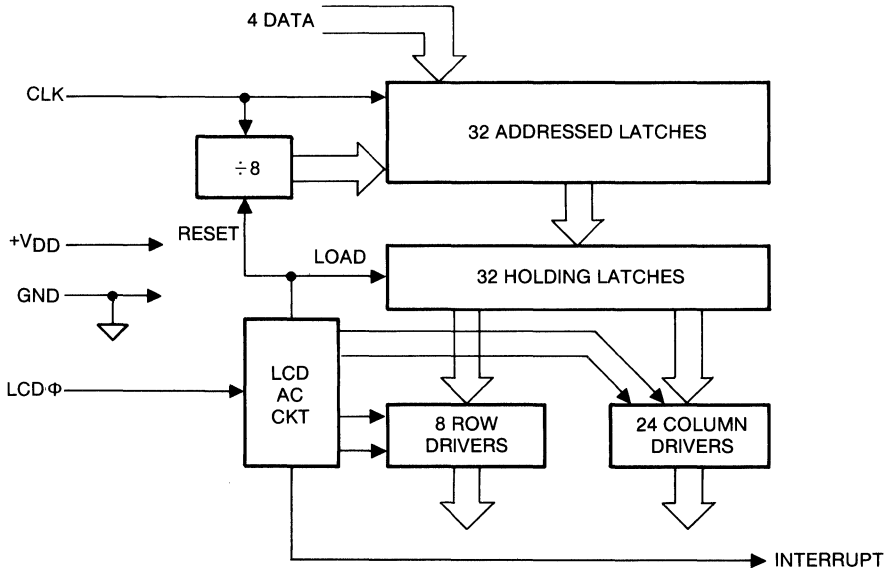
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		3	12	V
Supply Current	I_{DD}			600	µA
Input High Level	V_{IH}		.75V_{DD}	V_{DD}	V
Input Low Level	V_{IL}		V_{DD}—15	.25V_{DD}	V
Input Leakage	I_L			5	µA
Input Capacitance	C_I			5	pf
Row Output High	V_{OH}		V_{DD}—.05	V_{DD}	V
Row Output Low	V_{OL}		0	.05	V
Row Output Unselected	V_{OM}		.5V_{DD}—.05	.5V_{DD}+.05	V
Column Output High	V_{OH}		.68V_{DD}—.05	.68V_{DD}+.05	V
Column Output Low	V_{OL}		.32V_{DD}—.05	.32V_{DD}+.05	V
Row and Column Output Impedance	R_{ON}	I_L = 10µA		30	KΩ
Interrupt Output Impedence	R_{ON}	I_L = 100µA		1	KΩ
Clock Rate	f		DC	1.0	MHz
Data in Setup Time	t_{DS}	Data change to clock fall	300		nsec.
Data in Hold Time	t_{DH}	Clock fall to data change	150		nsec.
LCDΦ to Interrupt Output Delay	t_D		300		nsec.
LCDΦ High Level	V_{IH}		.9V_{DD}	V_{DD}	V
LCDΦ Low Level	V_{IL}		0	.1V_{DD}	V
LCDΦ Input Impendence	R_{IN}		1	3	MΩ

TYPICAL WAVEFORMS

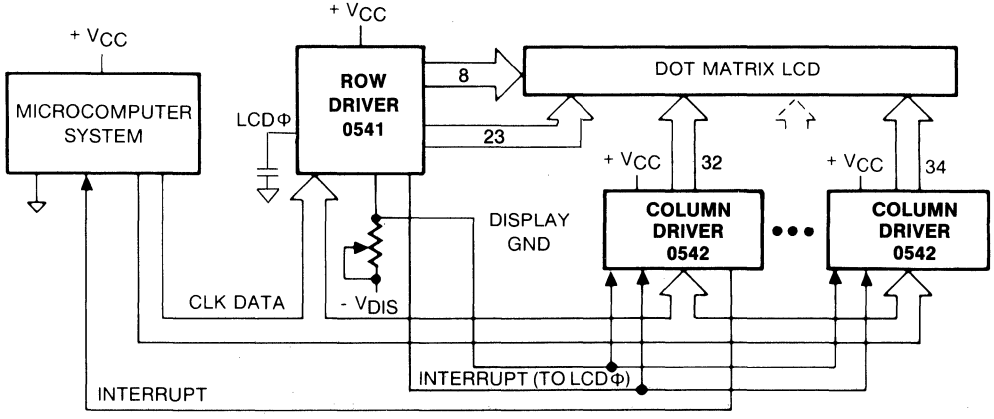




BLOCK DIAGRAM



TYPICAL SYSTEM BLOCK DIAGRAM



OPERATING NOTES

1. The addressed latches load when clock is high.
2. A logic 1 on Data In selects a row or causes a segment to be visible.
3. A parallel transfer of data from the addressed latches register to the holding latches occurs upon the rising edge of Interrupt Output. Also, the ÷8 counter is reset.
4. Row waveforms are out of phase with Interrupt Output if selected and at midpoint voltage otherwise. Levels are V_{DD}, 0, and $V_{DD}/2$.
5. Column waveforms are in phase with Interrupt Output if selected and are out of phase if not selected. Levels are .32 V_{DD} and .68 V_{DD}.
6. The intended mode of operation is as follows:
   a. Interrupt Output frequency is the minimum no flicker frequency (≈30Hz) times the number of backplanes utilized.
   b. Interrupt Output is exactly 50% duty cycle (to keep DC off the display) and is synchronized with loading the data from addressed latches to holding latches.
   c. In between each Interrupt Output rising edge, 4 bit parallel data is clocked in with 8 clock pulses for the next time slot to await the next Interrupt Output rising edge, which causes the parallel transfer.
   d. The Interrupt Output goes to the microcomputer and is treated as a refresh request, or else the microcomputer drives the LCDΦ input.
   e. Backplanes are addressed sequentially and individually.
7. The LCDΦ pin can be used in two modes, driven or oscillating. If LCDΦ is driven, the Interrupt Output will follow it. If the LCDΦ pin is allowed to oscillate, its frequency is inversely proportional to capacitance and the Interrupt Output waveform has a frequency half that of the oscillator itself. The approximate relationship is f_{out} (KHz) = 380/ c (pf). The frequency is nearly independent of supply voltage.
8. To cascade units, either connect Interrupt Output of one circuit to LCDΦ of all other circuits (thus one capacitor provides frequency control for all circuits) or connect LCDΦ of all circuits to a common driving signal. Then tie all corresponding data inputs together and clock each circuit individually when its data is on the bus. In the case of two driver circuits and an 8 bit microcomputer, the clocks could be common and each Data In tied to a different line of the data bus.
9. There are two obvious signal races to be avoided:
   a. Changing data when clock is falling, and
   b. Allowing Interrupt Output rising edge to be very close to clock falling edge.
10. If supply voltage is altered to optimize LCD contrast or for temperature compensation, it is best to tie all positive supply terminals in common and vary the negative supply. This prevents inadvertently forward biasing diodes.
11. Input order of 0541.

Clk Pulse	1	2	3	4	5	6	7	8
Data 0	R 0	R 4	C 0	C 4	C 8	C 12	C 16	C 20
Data 0	R 1	R 5	C 1	C 5	C 9	C 13	C 17	C 21
Data 2	R 2	R 6	C 2	C 6	C 10	C 14	C 18	C 22
Data 3	R 3	R 7	C 3	C 7	C 11	C 15	C 19	

12. Input order of 0542 is similar, but starts at C0 (Pulse 1, Data 0) and ends at C 31 (Pulse 8, Data 3).

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Printed in U.S.A. 6/83
Supersedes Previous Data

HUGHES AIRCRAFT COMPANY

Serial Input Dot Matrix LCD Driver

DESCRIPTION

Hughes' 0548 is a CMOS/LSI circuit which drives rectangular matrix LCD displays under microcomputer control. The display itself may be a standard x-y array or a custom array that geometrically is not regular at all. Applications include games, bar graphs, and various custom patterns.

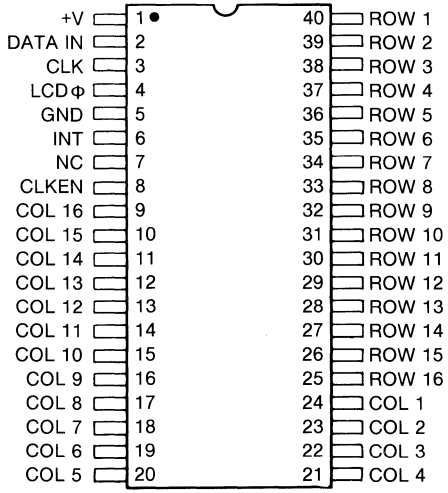
The 0548 is organized as 16 rows and 16 columns. It will drive an LCD display of up to 16 x 16 directly and can be cascaded for larger displays with additional 0548's or other Hughes LCD drivers. Data is input serially to maximize the number of output pins and minimize the number of control pins. This circuit drives (using a multiplexed scheme) the display with proper voltage level AC waveforms, but does not handle refresh or character encoding. This results in lower parts cost and greater design flexibility, but puts more burden on the microcomputer. The 0548 can be used with an 0539 to drive a display that has up to 16 rows and an arbitrary number of columns.

The 0548 is available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

FEATURES

- Direct drive of matrix LCDs
- Cascadable for larger displays
- On chip oscillator
- CMOS construction for:
  - Wide supply voltage range
  - Low power operation
  - High noise immunity
  - Wide temperature range
- CMOS, NMOS, and T^2L compatible inputs
- Requires only 3 control lines
- Flexible organization allows arbitrary display patterns
- Interrupt Output to request data from microcomputer

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

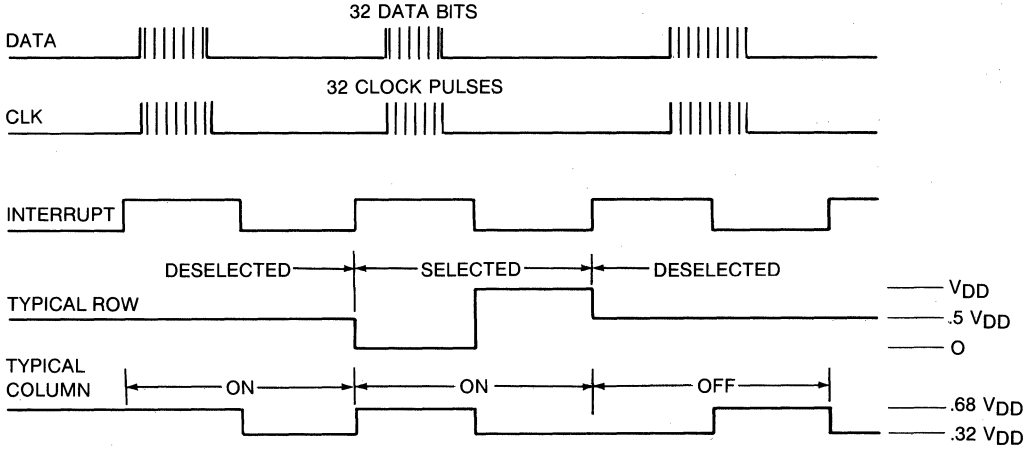
V_{DD} ..... — .3 to + 17 volts
Inputs ..... + V_{DD} — 17 to + V_{DD} + .3 volts
Power Dissipation ..... 250 mW
Operating Temperature
Ceramic Package .... — 55 to + 125°C
Plastic Package ..... — 40 to + 85°C
Storage Temperature ..... — 65 to + 125°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

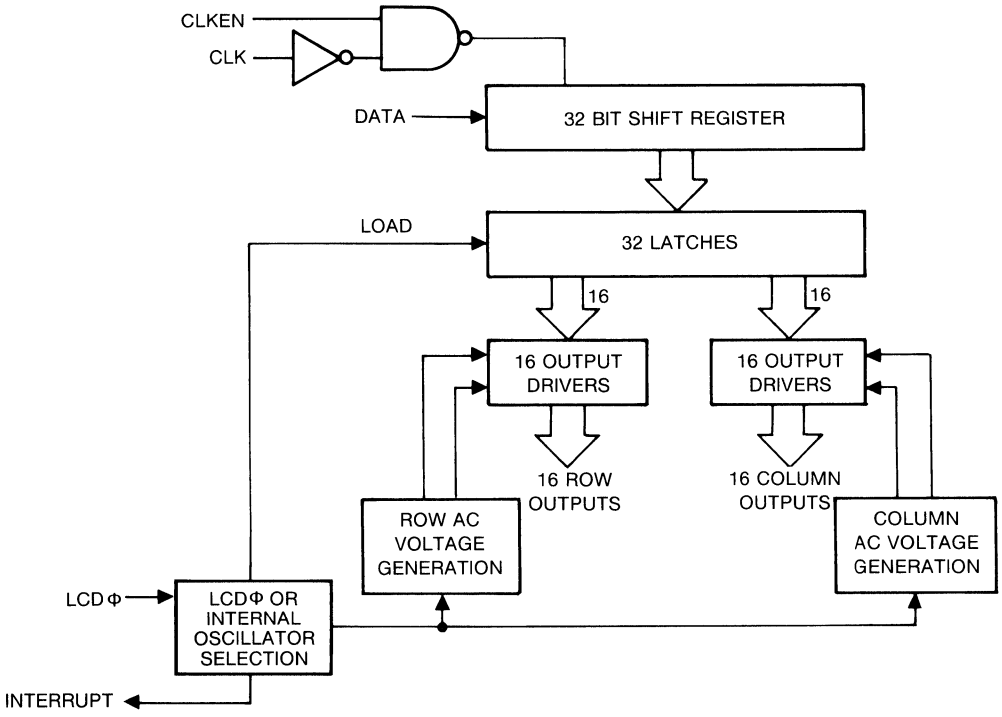
ELECTRICAL CHARACTERISTICS at T_A = + 25°C and V_{DD} = 5V unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		3	12	V
Supply Current	I_{DD}			750	μA
Input High Level	V_{IH}		.75V_{DD}	V_{DD}	V
Input Low Level	V_{IL}		V_{DD}—15	.25V_{DD}	V
Input Leakage	I_L			5	μA
Input Capacitance	C_I			5	pf
Row Output High	V_{OH}		V_{DD}—.05	V_{DD}	V
Row Output Low	V_{OL}		0	.05	V
Row Output Unselected	V_{OM}		.5V_{DD}—.05	.5V_{DD}+.05	V
Column Output High	V_{OH}		.68V_{DD}—.05	.68V_{DD}+.05	V
Column Output Low	V_{OL}		.32V_{DD}—.05	.32V_{DD}+.05	V
Row and Column Output Impedance	R_{ON}	I_L = 10 μA		40	KΩ
Interrupt Output Impedence	R_{ON}	I_L = 100 μA		1.5	KΩ
Clock Rate	f		DC	1.5	MHz
Data in Setup Time	t_{DS}	Data change to clock fall	300		nsec.
Data in Hold Time	t_{DH}	Clock fall to data change	100		nsec.
LCDΦ High Level	V_{IH}		.9V_{DD}	V_{DD}	V
LCDΦ Low Level	V_{IL}		0	.1V_{DD}	V
LCDΦ Input Impedance	R_{IN}		1	3	MΩ

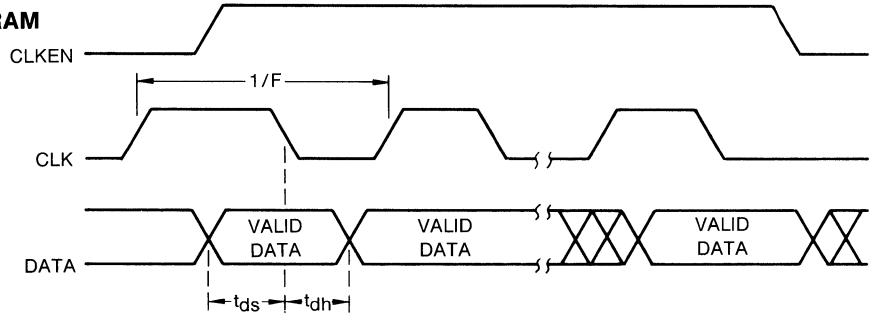
TYPICAL WAVEFORMS



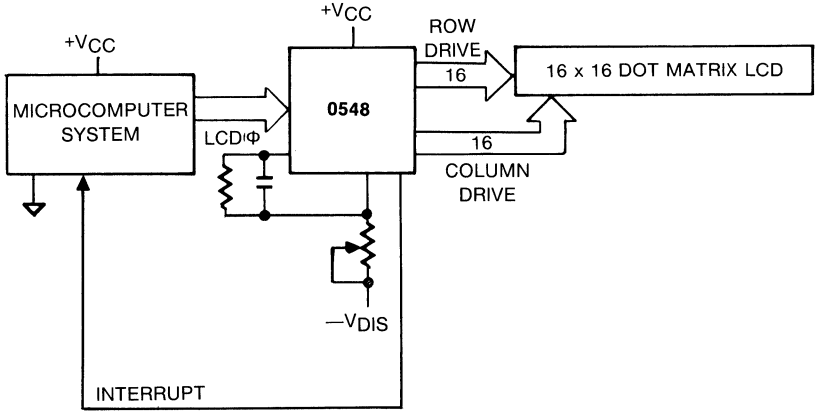
BLOCK DIAGRAM



TIMING DIAGRAM



TYPICAL SYSTEM BLOCK DIAGRAM



OPERATING NOTES

1. The Shift register loads and shifts on the falling edge of clock.
2. A logic 1 on Data In causes a segment to be visible.
3. A parallel transfer of data from the shift register to the latches occurs upon the rising edge of Interrupt Output.
4. Row waveforms are out of phase with Interrupt Output if selected and at mid-point voltage otherwise. Levels are V_{DD}, 0, and $V_{DD}/2$.
5. Column waveforms are in phase with Interrupt Output if selected and out of phase if not selected. Levels are .32 V_{DD} and .68 V_{DD}.
6. The intended mode of operation is as follows:
   a. Interrupt Output frequency is the minimum no flicker frequency (> 30Hz) times the number of backplanes utilized.
   b. Interrupt Output is exactly 50% duty cycle (to keep DC off the display) and is synchronized with loading the data from shift register to latches.
   c. In between each Interrupt Output rising edge, serial data is loaded for the next row to await the next Interrupt Output rising edge, which causes parallel transfer from shift register to display latches.
   d. The Interrupt Output goes to the microcomputer and is treated as a refresh request, or the microcomputer drives the LCDΦ input with 50% duty cycle.
   e. Backplanes are addressed sequentially and individually.
7. The LCDΦ pin can be used in two modes. If LCDΦ is driven, the Interrupt Output will follow it. LCDΦ will also oscillate if a resistor and capacitor are connected in parallel to ground. The resistor value should be at least 1MΩ. The approximate relationship is $f_{out} = \frac{1}{RC}$, which appears at Interrupt Output.
8. To cascade and synchronize several circuits, either connect Interrupt Output of one circuit to LCDΦ of all other circuits (thus one oscillator provides frequency control for all circuits) or connect LCDΦ of all circuits to a common driving signal. Then connect all clock lines together to the clock signal and connect each Data In to a different line of the data bus, allowing a parallel loading of all circuits' serial data. It is also possible to tie all data lines together and drive each clock individually like a chip select. Another alternative is to use the clock enable to allow reading data into specific circuits.
9. There are two obvious signal races to be avoided.
   a. Changing data when clock is falling, and
   b. Allowing Interrupt Output rising edge to be very close to clock falling edge.
10. If supply voltage is altered to optimize LCD contrast or for temperature compensation, it is best to tie all positive supply terminals in common and vary the negative supply. This prevents inadvertently forward biasing diodes.
11. Output locations correspond to a clockwise advancing shift register, thus Row 1 is the last data loaded and Col 16 is the first data loaded.
12. The RMS voltages this circuit delivers to individual LCD pixels depends on V_{DD} and the number of backplanes (N) used according to the following equations:

$$V_{RMS\ OFF} = V_{DD}\sqrt{\frac{.0324\ N + .07}{N}}$$

$$V_{RMS\ ON} = V_{DD}\sqrt{\frac{.0324\ N + .43}{N}}$$

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Printed in U.S.A. 6/83
Supersedes Previous Data

Serial Input Dot Matrix LCD Driver

DESCRIPTION

Hughes' 0607A is a CMOS/LSI circuit that drives a matrix LCD display under microcomputer control. The intended display is a 4 x 4 (16 segment) alphanumeric matrix or a 4 x 2 or 3 x 3 numeric matrix, each with nearly any number of characters. Other matrix displays, such as games and custom arrays, could also be driven by this circuit.

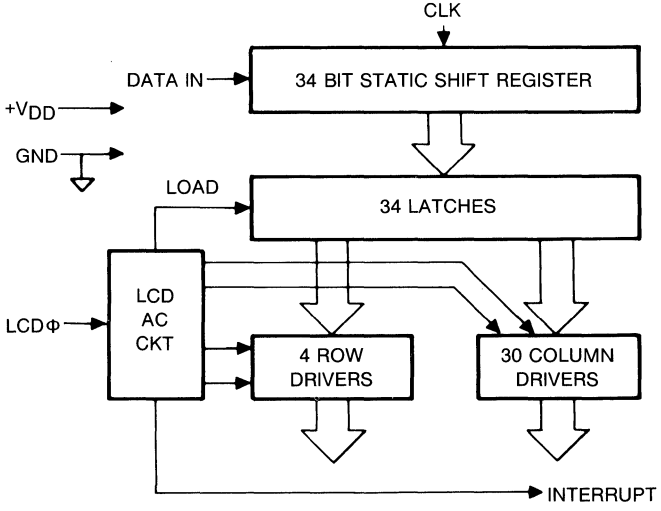
The 0607A is organized as 4 rows x 30 columns, and thus can handle 7 alphanumeric or 15 numeric characters by itself. The 0539A, organized as 0 rows x 34 columns may be used in addition to the 0607A when more than 30 columns are required. Data is serially input to maximize the number of output pins and minimize the number of control pins. This circuit drives (using a multiplexed scheme) the display with proper voltage level AC waveforms, but does not handle refresh or character encoding. This results in lower parts costs and greater design flexibility, but puts more burden on the microcomputer.

The 0607A is available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

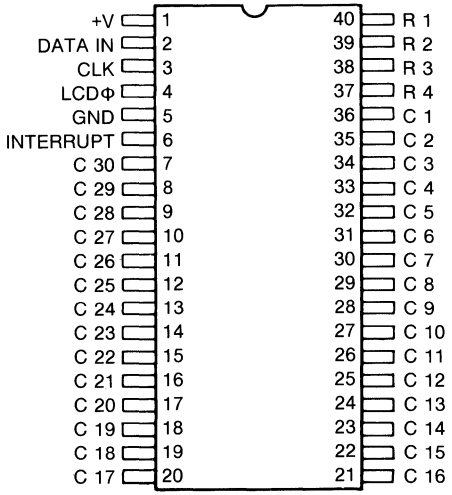
FEATURES

- Direct drive of matrix LCDs
- Cascadable for larger displays
- On chip oscillator
- CMOS construction for:
  - Wide supply voltage range
  - Low power operation
  - High noise immunity
  - Wide temperature range
- CMOS, NMOS, and T^2L compatible inputs
- Requires only 3 control lines
- Flexible organization allows arbitrary display patterns
- Interrupt Output to request data from microcomputer

BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

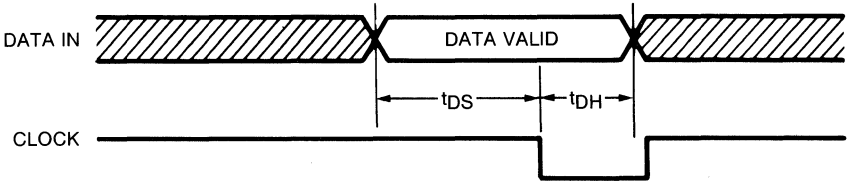
V_{DD} ..... — .3 to + 15 volts
Inputs ..... + V_{DD} — 17 to + V_{DD} + .3 volts
Power Dissipation ..... 250 mW
Storage Temperature ..... — 65 to + 125°C
Operating Temperature
Ceramic Package .... — 55 to + 125°C
Plastic Package ..... — 40 to + 85°C

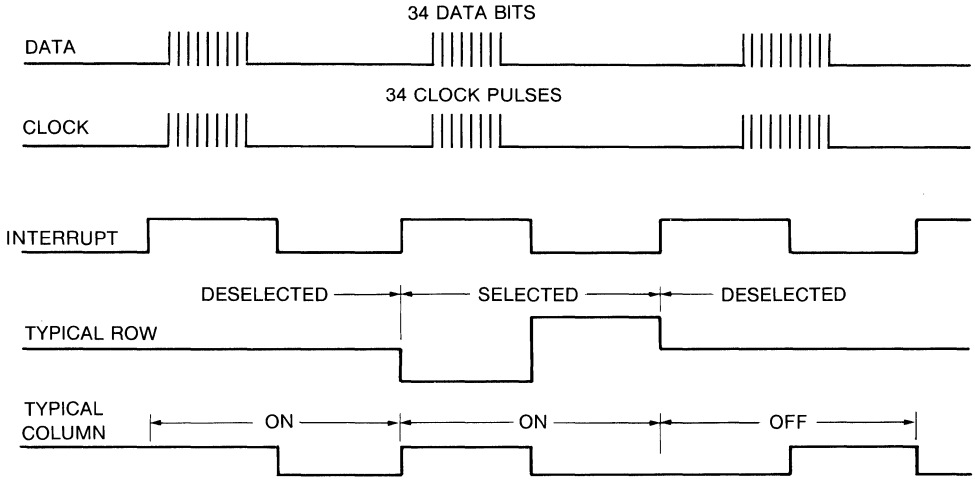
Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS at T_A = + 25°C and V_{DD} = 5V unless otherwise noted.

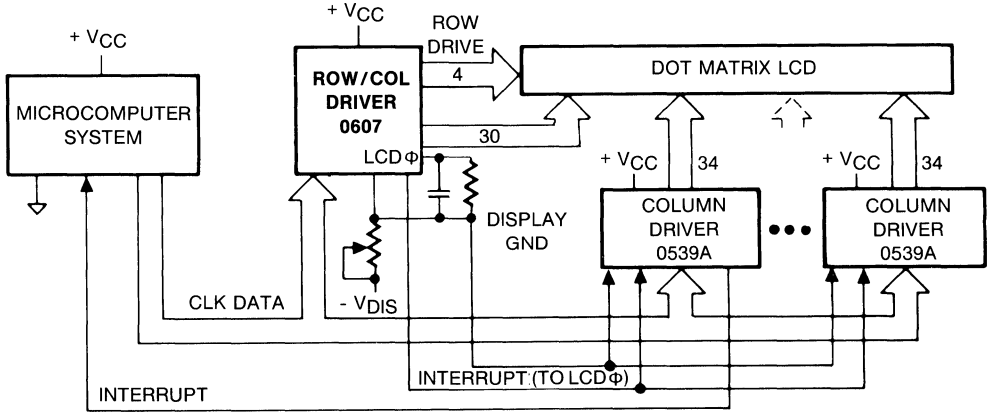
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		3	12	V
Supply Current	I_{DD}			750	μA
Input High Level	V_{IH}		.8 V_{DD}	V_{DD}	V
Input Low Level	V_{IL}		V_{DD}−15	.5V_{DD}	V
Input Leakage	I_L			5	μA
Input Capacitance	C_I			5	pf
Row and Column Output Impedance	R_{ON}	I_L = 10 μA		40	KΩ
Interrupt Output Impedence	R_{ON}	I_L = 100 μA		3	KΩ
Clock Rate	f		DC	1.5	MHz
Data in Setup Time	t_{DS}	Data change to clock fall	300		nsec.
Data in Hold Time	t_{DH}	Clock fall to data change	100		nsec.
LCDΦ to Interrupt Output Delay	t_D			600	nsec.
LCDΦ High Level	V_{IH}		.9V_{DD}	V_{DD}	V
LCDΦ Low Level	V_{IL}		0	.1V_{DD}	V
LCDΦ Input Impedance	R_{IN}		1	3	MΩ
DC Offset Voltage, Any Display Element	V_{OFF}			50	mV
Row Output High	V_{OH}	Typical	V_{DD}		V
Row Output Low	V_{OL}	Typical	0		V
Row Output Unselected	V_{OM}	Typical	.5V_{DD}		V
Column Output High	V_{OH}	Typical	.68V_{DD}		V
Column Output Low	V_{OL}	Typical	.32V_{DD}		V

TIMING DIAGRAM





TYPICAL SYSTEM BLOCK DIAGRAM



OPERATING NOTES

1. The Shift register loads and shifts on the falling edge of clock.
2. A logic 1 on Data In causes a segment to be visible.
3. A parallel transfer of data from the shift register to the latches occurs upon the rising edge of Interrupt Output.
4. Row waveforms are out of phase with Interrupt Output if selected and at midpoint voltage otherwise. Levels are V_{DD}, 0, and $V_{DD}/2$.
5. Column waveforms are in phase with Interrupt Output if selected and out of phase if not selected. Levels are .32 V_{DD} and .68 V_{DD}.
6. The intended mode of operation is as follows:
   a. Interrupt Output frequency is the minimum no flicker frequency (>30Hz) times the number of backplanes utilized.
   b. Interrupt Output is exactly 50% duty cycle (to keep DC off the display) and is synchronized with loading the data from shift register to latches.
   c. In between each Interrupt Output rising edge, serial data is loaded for the next row to await the next Interrupt Output rising edge, which causes parallel transfer from shift register to display latches.
   d. The Interrupt Output goes to the microcomputer and is treated as a refresh request, or else the microcomputer drives the LCDΦ input with 50% duty cycle.
   e. Backplanes are addressed sequentially and individually.
7. The LCDΦ pin can be used in two modes. If LCDΦ is driven, the Interrupt Output will follow it. LCDΦ will also oscillate if a resistor and capacitor are connected in parallel to ground.

   The resistor value should be at least 1MΩ. The approximate relationship is $f_{out} = \frac{1}{RC}$, which appears at Interrupt Output.
8. To cascade and synchronize several circuits, either connect Interrupt Output of one circuit to LCDΦ of all other circuits (thus one oscillator provides frequency control for all circuits) or connect LCDΦ of all circuits to a common driving signal. Then connect all clock lines together to the clock signal and connect each Data In to a different line of the data bus, allowing a parallel loading of all circuits' serial data. It is also possible to tie all data lines together and drive each clock individually like a chip select.
9. There are two obvious signal races to be avoided.
   a. Changing data when clock is falling, and
   b. Allowing Interrupt Output rising edge to be very close to clock falling edge.
10. If supply voltage is altered to optimize LCD contrast or for temperature compensation, it is best to tie all positive supply terminals in common and vary the negative supply. This prevents inadvertently forward biasing diodes.
11. Output locations correspond to a clockwise advancing shift register, thus R 1 is the last data loaded and C 30 is the first data loaded.
12. The RMS voltages this circuit delivers to individual LCD pixels depends on V_{DD} and the number of backplanes (N) used according to the following equations:

$$V_{RMS\ OFF} = V_{DD}\sqrt{\frac{.0324\ N + .07}{N}}$$

$$V_{RMS\ ON} = V_{DD}\sqrt{\frac{.0324\ N + .43}{N}}$$

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HUGHES AIRCRAFT COMPANY

Auto-Refresh CMOS LCD Driver

DESCRIPTION

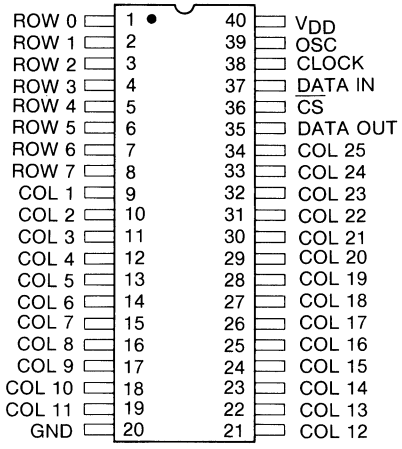
Hughes' 0515 is a CMOS driver for multiplexed Liquid Crystal Displays. Each unit is capable of driving an LCD matrix of up to 8 rows x 25 columns. This display could be a graphic array, custom array, or 5 characters in a 5 x 7 format. Multiple units may be cascaded for displays with more rows and/or more columns. The input is in a serial format (data is loaded in one row at a time) and requires the user to specify the on/off state of each pixel. Therefore, the user has great flexibility in displaying the shapes and figures he needs. The 0515 provides all the multi-level AC waveforms necessary for the LCD driver, automatically refreshes the display, and interfaces directly with most microprocessors and microcomputers.

The 0515 operates over a 5-10 voltage range. The 0515 is available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

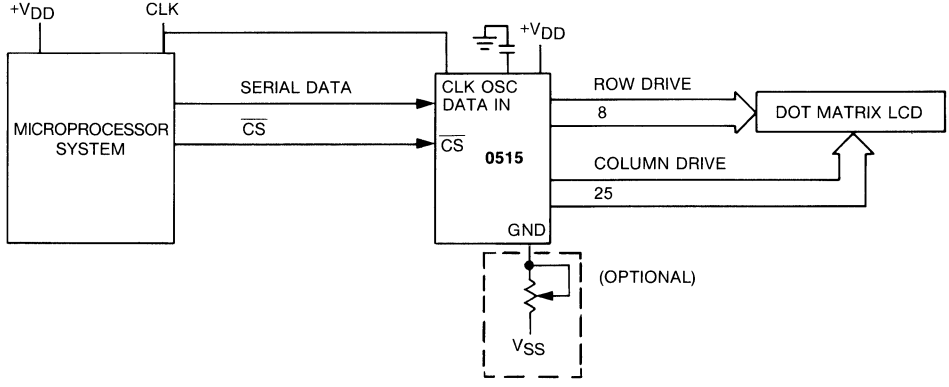
FEATURES

- CMOS circuitry
  - Low power dissipation
  - Wide temperature range
  - Wide supply range
- Microprocessor compatible
- CMOS and NMOS compatible
- Drives an 8 x 25 multiplexed LCD
- Automatic display refresh
- On-Chip oscillator
- Power down/blank display mode
- Number of backplanes is software programmable

PIN CONFIGURATION



TYPICAL SYSTEM INTERCONNECT



ABSOLUTE MAXIMUM RATINGS

V_{DD} Supply ..... −.03 to + 12 Volts
Input to Voltages ..... V_{DD} −12 to V_{DD} + .3
Operating Temperature
Plastic Package ..... − 40 to + 85°C
Ceramic Package ..... − 55 to + 125°C
Storage Temperature ..... − 65 to + 125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

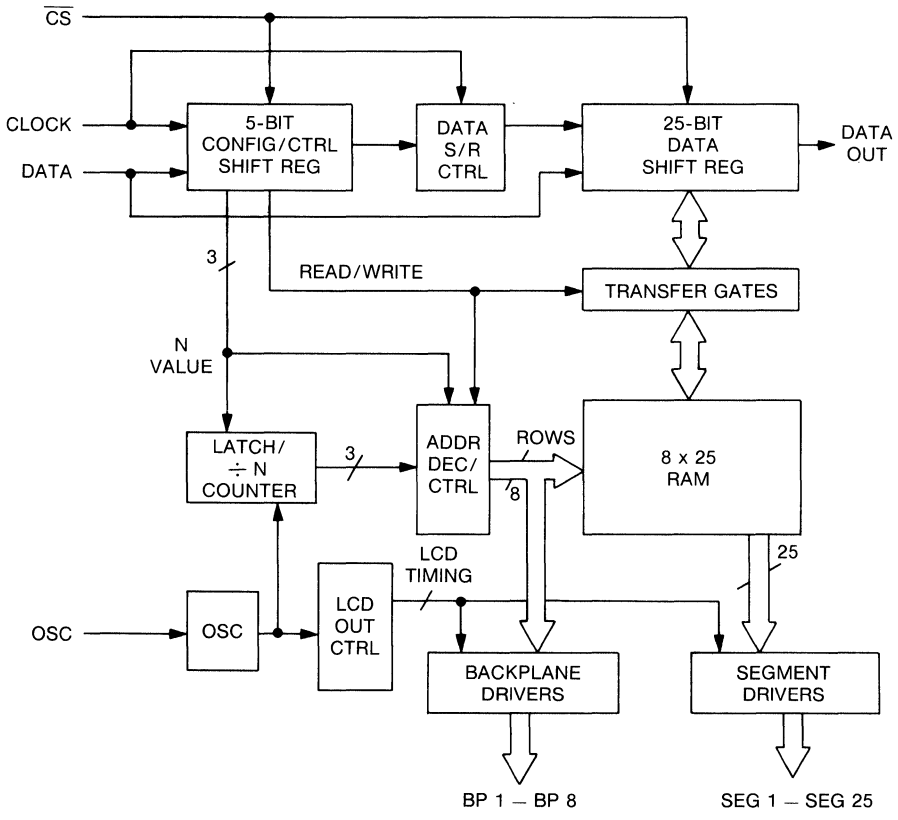
STATIC ELECTRICAL CHARACTERISTICS at T_A = + 25°C, V_{DD} = + 5V, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}		5		10	V
Supply Current	I_{DD}	V_{DD} = 5			900	µA
Input High Level	V_{IH}	entire V_{DD} range	.75 V_{DD}		V_{DD}	V
Input Low Level	V_{IL}		V_{DD}−12		.25V_{DD}	V
Input Leakage	I_L				5	µA
Input Capacitance	C_I				5	pf
Row Output High (Sel)	V_{OH}			V_{DD}		V
Row Output Low (Sel)	V_{OL}			0		V
Row Output High (Unsel)	V_{OUH}			.75 V_{DD}		V
Row Output Low (Unsel)[1]	V_{OUL}			.25 V_{DD}		V
Column Output High	V_{OH}			V_{DD}		V
Column Output Low	V_{OL}			0		V
Column Output (Unsel)	V_{OM}			.5 V_{DD}		V
Data Output High Level	V_{OH}	40 µA	2.4			V
Data Output Low Level	V_{OL}	I_L = 1.6µA			.4	V
Row Output Impedance	R_{OUTR}	I_L = 10µA			10	KΩ
Column Output Impedance	R_{OUTC}	I_L = 10µA			40	KΩ
Offset Voltage	V_{OFF}				50	mV

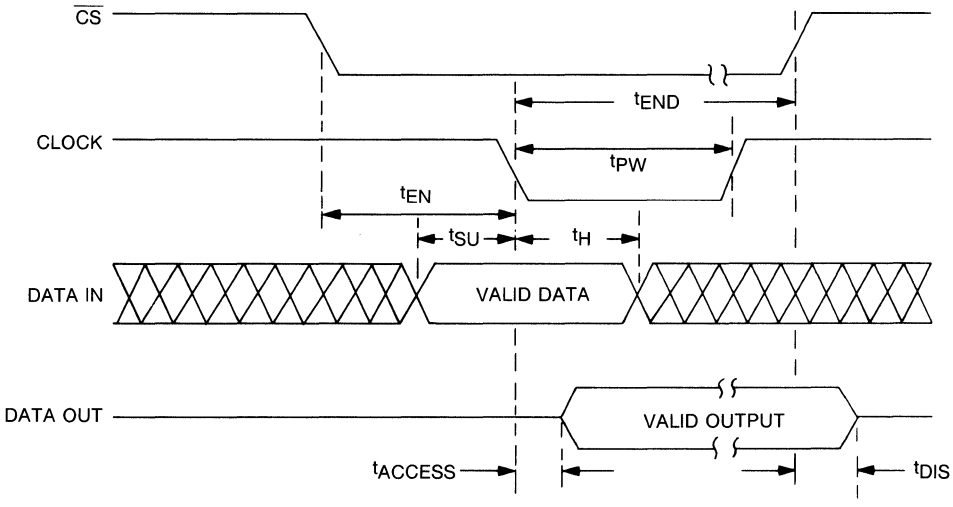
NOTE 1: See Output Waveforms

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = +25°C; V_{DD} = +5V unless otherwise specified.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Select enable time, chip select falling edge to clock falling edge	t_{EN}	500		nsec
Data Setup time, data valid prior to clock falling edge	t_{SU}	100		nsec
Data hold time, data valid after clock falling edge	t_H	10		nsec
Output Prop delay, clock-falling edge to data output valid	t_{ACCESS}		200	nsec
Disable time, chip select rising edge to data output hi-impedance	t_{DIS}		200	nsec
Deselect time delay from clock falling edge to chip select rising edge	t_{END}	250		nsec



TIMING DIAGRAM



SELECT AND MODE CONTROL

There are four modes of operation in the 0515:

1. Write buffer mode
2. Read buffer mode
3. Initialization mode — blank display
4. Initialization mode — visible display

A serial data string is presented to the Data In terminal for any operation. The data format is shown below:

FIRST ← SERIAL DATA BITS TO THE DATA IN TERMINAL → LAST																														
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Row Control (8 rows)			Mode con-trol		Column Select (25 columns)																									

ROW CONTROL

Data bits 1, 2, and 3 represent the address of the row to be selected or the total number of rows to be selected minus 1 depending on the mode controls. The row control information is in binary and controls 8 rows from 0 through 7. Data bit 1 is the MSB and data bit 3 is the LSB.

MODE CONTROL

Data bits 4 and 5 represent the operational mode to be selected. Each mode is described separately in the Operational Mode Section.

Data bit 4	5	
0	0	Write into RAM storage buffer
0	1	Read from RAM storage buffer
1	0	Initialization with blank display
1	1	Initialization with visible display

COLUMN SELECT

Data bits 6 through 30 represent the 25 individual column bits in the addressed row (bits 1-3) while in the write mode. Data bit 6 corresponds to column 1, data bit 7 corresponds to column 2 . . . , data bit 30 corresponds to column 25.

OPERATIONAL MODES

1. Initialization Mode:

There are two modes available for initialization of the 0515. The main purpose for initialization is to define the total number of rows to be used in the display, and to make the display visible or blank.

a. Initialization with Blank Display (Bit 4 = 1, Bit 5 = 0)

When this mode is selected, the display is blanked out and the total number of rows are selected via data bits 1, 2, and 3. Column information may or may not be provided. If the column information is provided via data bits 6 through 30, this mode also acts as a write into RAM storage mode writing a row of data into the RAM at the row selected by data bits 1, 2 and 3. (i.e., the last row of the display).

b. Initialization with Visible Display (Bit 4 = 1, Bit 5 = 1)

In this mode, the first three data bits represent (N-1) where N is the total number of rows used in the display. Also it enables the display information to become visible. This mode can be terminated after five data bits, otherwise, it will read the column information of the row that is selected via the data-out line on successive clock inputs (i.e., the last row of the display).

2. Write Mode (Bit 4 = 0, Bit 5 = 0)

This mode is used to write or update the data into the 8 x 25 RAM storage. Row address is provided by row control data bits 1, 2, and 3, while 25 bit data for each column is provided via data bit 6 through bit 30. The display can be made visible or blank depending upon the initialization mode previously selected.

3. Read mode (Bit 4 = 0, Bit 5 = 1)

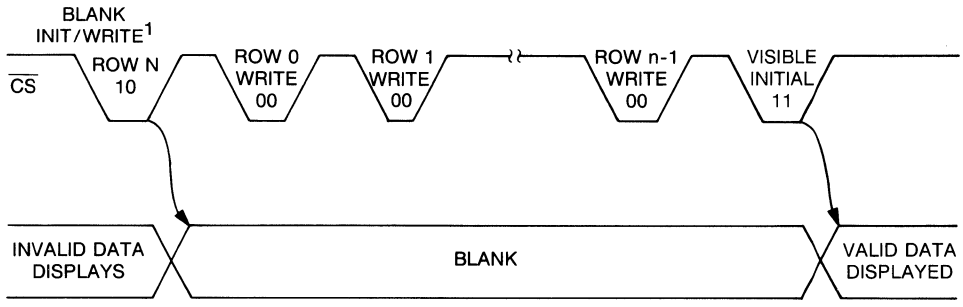
This mode is used to read the data from the 8 x 25 RAM storage and sequentially display it on the Data Out terminal. Row address is provided by row control data bits 1, 2 & 3.

For each row address, column data is shifted serially on Data Out terminal from column 25 to column 1 on each successive clock.

4. Typical Mode Sequence

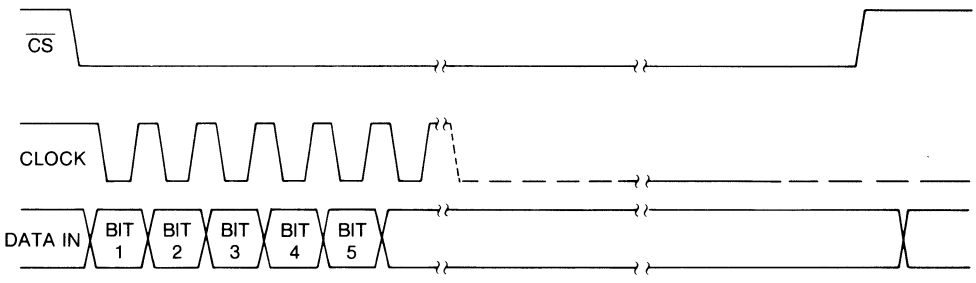
With power on, the display shows random data on the display. The initialization with blank display mode can be selected and the first write can be made on the last row during the same cycle by providing column data on bit 6 through bit 30. Additional write modes will be selected to write into all the rows in the same manner. Once the final row is written, an initialization mode with visible display must be selected.

TYPICAL MODE SEQUENCE & TIMING



NOTE 1: SEE EXPANDED TIMING BELOW

EXPANDED INITIALIZATION/WRITE WITH BLANK DISPLAY (30 BITS)



SYNCHRONIZATION AND CASCADING

To cascade a number of 0515 s, which share rows, all units must be synchronized. This can be done by driving each Osc pin of the 0515 with the same external signal and initializing all units at the same time.

In Figure A, the 0515 is used to drive 8 rows x 25N columns. Rows from one unit are tied to the display and rows on the other units are not used. The chip select signal also controls all the 0515s at the same time on Data In pins. The different data (column data) is presented by the data bus to control different columns. In the initialization mode all 0515s must be presented the same data on Data In pins by software. Alternatively, a common data line and individual chip selects could be used.

Theoretically any number of 0515s can be cascaded together as shown. In reality, it depends on the characteristics of the display and the application. In a similar manner, one can utilize a number of 0515s to drive 16 rows x m column displays. For each 8 x 25 block, one 0515 is required as shown in Figure B.

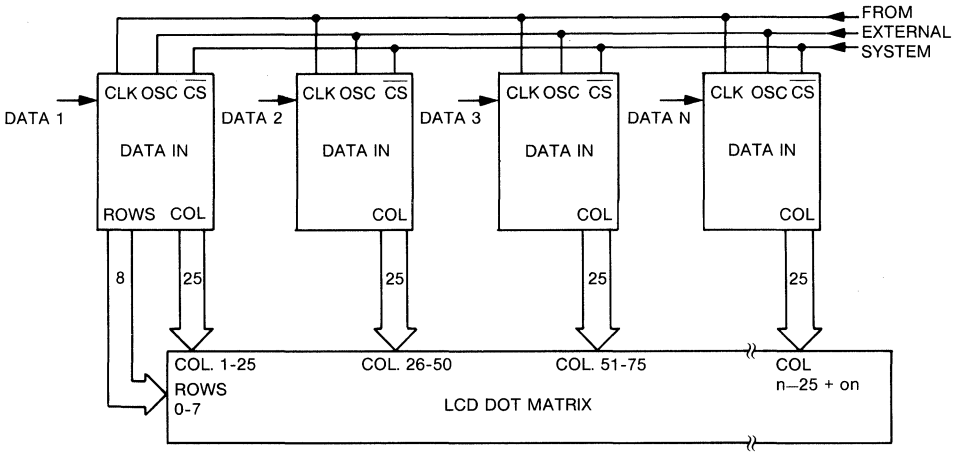


Figure A

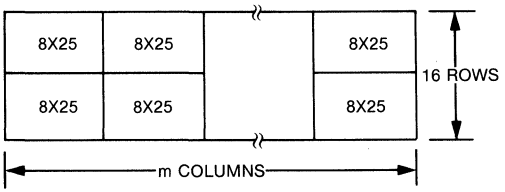


Figure B

SIGNAL DESCRIPTION

Row 0 — Row 7; Pin 1 — Pin 8 (Outputs): These eight outputs can be connnected directly to the row pins (backplanes) of the display.

Col 1 — Col 25; Pin 9 — Pin 19, Pin 21 — Pin 34 (Outputs): These twenty five outputs can be connected directly to the column pins of the display.

GND; Pin 20: Ground for display and display driver.

V_{DD}; Pin 40: Most positive supply for the display and display driver.

Data Out; Pin 35 (Output): The Data Output pin produces data serially from the RAM buffer during the read buffer mode.

$\overline{CS}$; Pin 36 (Input): The chip select input enables all operating modes of 0515 when $\overline{CS}$ is low.

Data In; Pin 37: The data input pin is used for loading the RAM buffer data serially from an external system. Positive logic is used and a logic 1 makes a pixel visible.

Clock; Pin 38 (Input): Negative going edge on this pin clocks the data in or out, depending on the mode.

OSC; Pin 39 (Input): The timing for refresh waveforms for the LCD is determined by a capacitor connected to this pin. An external signal should be used to synchronize the oscillators while cascaded.

OSCILLATOR FREQUENCY

To determine the proper frequency of operation, one must consider:

1) the external frequency is divided by two on-board.
2) number of backplanes selected (rows), and
3) 30 Hz minimum no-flicker frequency.

The f is derived as:

$$f = \frac{1}{2 \times N \times 30}$$

The external capacitor which will produce f is:

$$f = \frac{1}{50K \times C}$$

where the value of C is in microfarads

Example: 8 backplanes, $\frac{1}{2 \times 8 \times 30} = \frac{1}{50K \times C}$, yields C = .01 microfarads

LCD DRIVER NOTES

1. RMS Drive Voltages: The On and Off RMS drive voltages supplied to each pixel by the 0515 depend on the number of backplanes, N, as follows:

$$V_{RMS}\ ON = \frac{V_{DD}}{4}\sqrt{\frac{N+15}{N}}$$

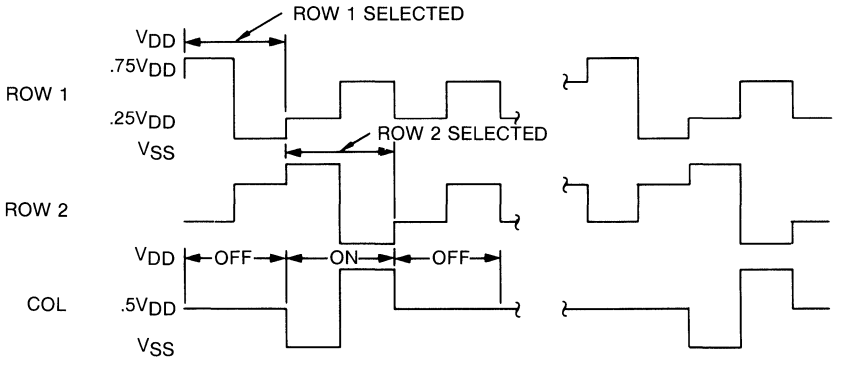
$$V_{RMS}\ OFF = \frac{V_{DD}}{4}\sqrt{\frac{N+3}{N}}$$

The 0515 generates on-chip all required voltages to drive a multiplexed LCD with the V/4 drive scheme. The V/4 scheme requires the following voltages to be derived (when V_{DD} is the supply voltage):

V_{DD}
.75 V_{DD}
.5 V_{DD}
.25 V_{DD}
0

Note if the display requires a swing more negative than system ground, the V_{DD} is tied in common with system V_{DD} and the GND is taken sufficiently lower than system GND to provide the required swing. (The user must ensure that the 0515's V_{IL} spec is not violated and that V_{OL}'s can be read by the system.) Waveforms for the V/4 display drive scheme are shown below:

TYPICAL OUTPUT WAVEFORMS



2. Temperature Compensation: The 0515 can be used with displays requiring temperature compensation. The technique is to select a PTC (Positive Temp Compensation) thermistor with a temperature response which complements that of the display. The thermistor is inserted between the 0515's V_{SS} and the negative reference source.

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Printed in U.S.A. 7/83
Supersedes Previous Data

Intelligent LCD Dot Matrix Controller/Driver

DESCRIPTION

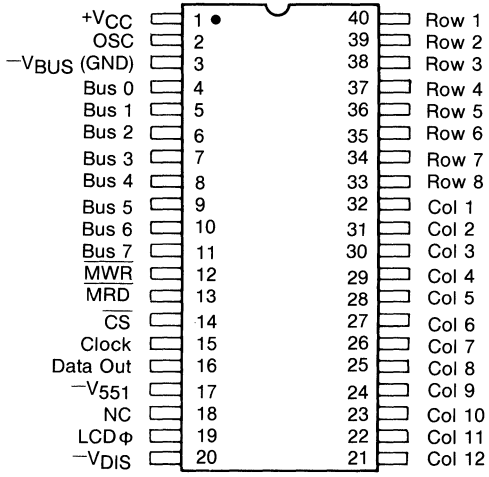
Hughes' 0550 and 0551 Chip Set will drive a 5 x 7 or 5 x 8 liquid crystal dot matrix of up to 32 characters. Control of the display is handled through an 8 bit bidirectional I/O port. The chip set handles character decode, display manipulation, cursor control, and all display drive functions including refresh and generation of multiple-level AC waveforms.

The 0550/0551 is available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

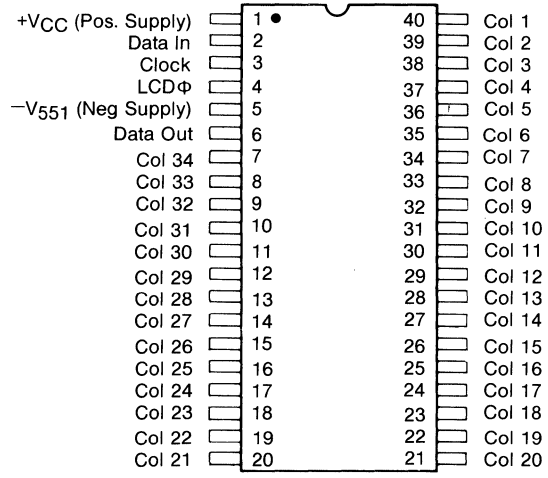
FEATURES

- CMOS circuitry
  - Low power dissipation
  - Wide supply variation
  - High noise immunity
- Microcomputer compatible
- ASCII input format
- Display of 64 different characters
- Control of up to a 32 character display
- Generation of all drive waveforms
- Automatic refresh
- Cursor control
- Display manipulation instructions to accomplish:
  - Shift
  - Rotate
  - Blank
  - Blink
  - Fast load
  - Power down
- Instructions to control output of:
  - Characters
  - Cursor position
  - Display control flags
  - Busy status

0550 PIN CONFIGURATION



0551 PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, ($+V_{DD}$) ..... — 3V to + 13 Volts
Input Voltage, (V_I) ..... V_{DD} — 15 to V_{DD} + .3 Volts
Operating Temperature, (T_{OP})
Plastic Package ..... — 40 to + 85°C
Ceramic Package ..... — 55 to + 125°C
Storage Temperature, (T_{STO}) .. — 50 to + 125°C

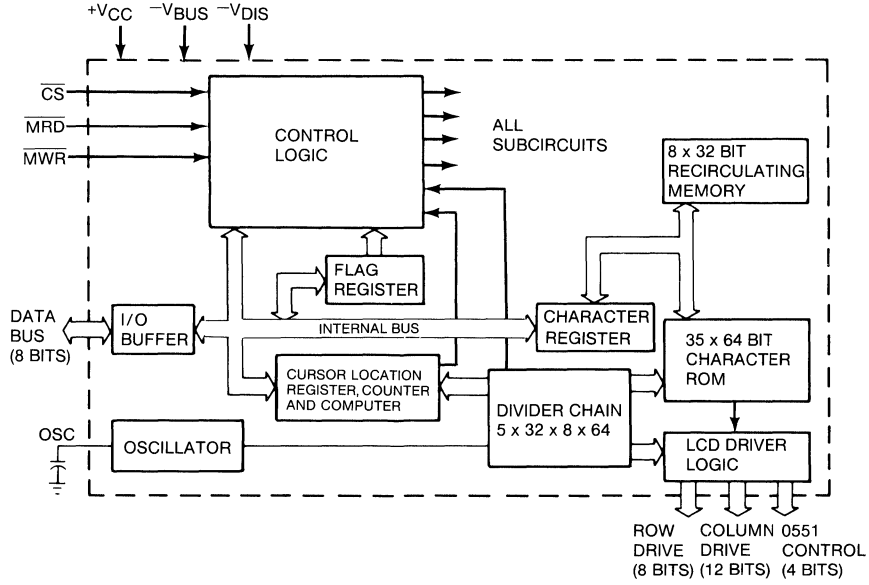
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS at T_A = + 25°C unless otherwise specified ($-V_{BUS}$ pin is considered GND) $V_{DD} = V_{CC} + V_{DIS}$.

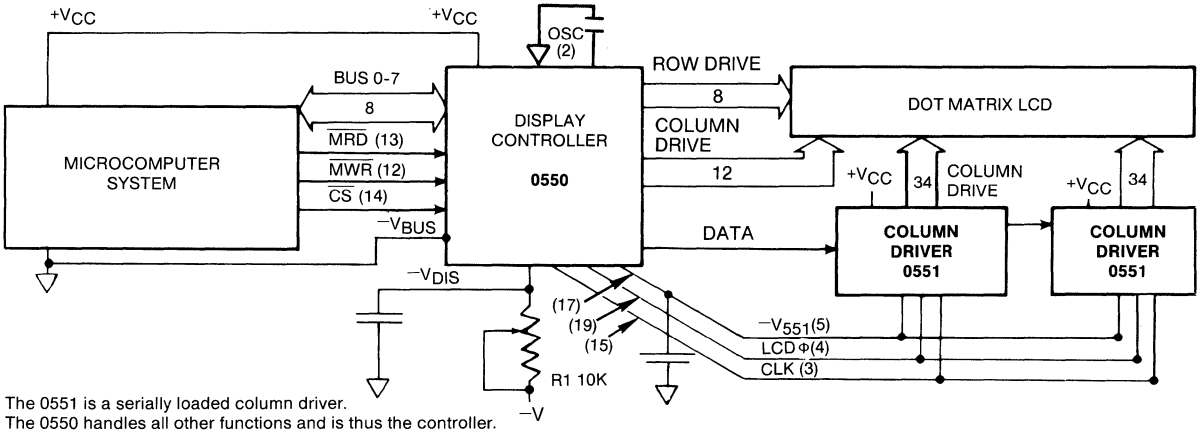
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNITS
Environmental Power Supply Voltage	$+V_{DD}$		5	10	V
Power Supply Current (0550 and 0551)	I_{DD}	Operating at 5V		750	µA
Quiescent Current (0550 and 0551)	I_Q	5V, Power Down Mode Inputs at Either Supply[1]		20	µA
Inputs - 550	V_{IH}	V_{DD} = 3 to 10V	.8V_{DD}	V_{DD}	V
High Level (0550 Inputs 8 Data Bus $\overline{CS}$ $\overline{MRD}$ $\overline{MWR}$)	V_{IL}	8 Data Bus	0	.5V_{DD}	V
Low Level	V_{IL}	$\overline{CS}$, $\overline{MRD}$, $\overline{MWR}$	V_{CC}−15	.5V_{DD}	V
Leakage	I_L	V_{IN} = 0, V_{DD} = 10		5	µA
Capacitance	C_{IN}			5	pf
Inputs - 551					
High Level (0551 Inputs Data In LCDΦ Clock)	V_{IH}		.8V_{DD}	V_{DD}	V
Low Level	V_{IL}		V_{DD}−15	.5V_{DD}	V
Leakage	I_L	V_{IN} = 0, V_{DD} = 10		5	µA
Capacitance	C_{IN}			5	pf
Outputs					
High Level (Signals to 0551 LCDΦ Data Out Clock)	V_{OH}		V_{CC}−.05	V_{CC}	V
Low Level	V_{OL}		$-V_{DIS}$	$-V_{DIS}$+.05	V
Impedance	R_{ON}	5V, I = 100 µA		3	KΩ
Column Drive Impedance	R_{OUT}	5V		40	KΩ
Row Drive Impedance	R_{OUT}	5V		10	KΩ
Bus Drive High	V_{IH}	5V, I = 1.6 mA source	4		V
Bus Drive Low	V_{IL}	5V, I = 1.6 mA sink		.4	V
Timing (See Note 2) Data Set-up Time	t_{DS}	Data valid to $\overline{MWR}$ fall	20		nsec
Data Hold Time	t_{DH}	$\overline{MWR}$ pulse to data change	75		nsec
$\overline{MWR}$ Pulse Width High	t_{PWH}		600		nsec
$\overline{MWR}$ Pulse Width Low	t_{PWL}		600		nsec
$\overline{MRD}$ Delay	t_{PD}	$\overline{MRD}$ fall to data valid	600		nsec
$\overline{MRD}$ Pulse Width High	t_{PWH}		600		nsec
$\overline{MRD}$ Pulse Width Low	t_{PWL}		600		nsec

NOTE 1 — Oscillator high if driven
NOTE 2 — $\overline{MWR}$ and $\overline{MRD}$ negative pulses assumed to be coincident with or narrower than $\overline{CS}$ negative pulse

FUNCTIONAL BLOCK DIAGRAM

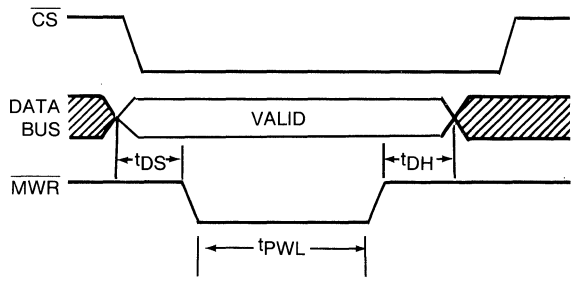


SYSTEM BLOCK DIAGRAM

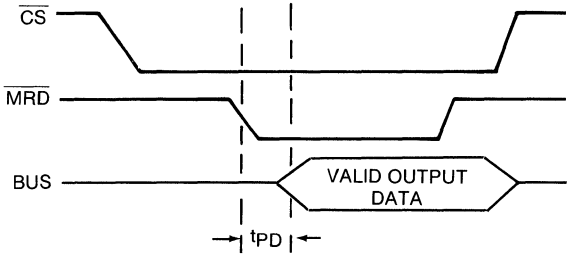


The 0551 is a serially loaded column driver.
The 0550 handles all other functions and is thus the controller.
(See Operating Notes, page 8, Variable Resistor (item 2) and Power Supply (item 4).

INPUT TIMING — 0550



OUTPUT TIMING — 0550



INSTRUCTION SET

Table 1

Description	OP Code 76543210 (see note 1)	HEX Code	BUS (see note 1)	Input or Output	Immed. Exec.	Creates Short Busy	Creates Long Busy	Not During PD	Not During Busy
Load Character	001XXXXX to 010XXXXX	20 to 5F		I	—	—	√	√	√
Load Cursor Location	000XXXXX	00 to 1F		I	√	—	—	—	√ (see note 2)
Set Display Control Flag	011XXXXY	60 to 71		I	√	—	—	—	—
Blink Cursor	0110 0000 - off 0110 0010 - on	60 61	0						
Blink Display	0110 0011 - off 0110 0011 - on	62 63	1						
Auto/Inc Dec	0110 0100 - off 0110 0101 - on	64 65	2						
Up/Down	0110 0110 - off 0110 0111 - on	66 67	3						
Blank Display	0110 1000 - off 0110 1001 - on	68 69	4						
Visible Cursor	0110 1010 - off 0110 1011 - on	70 71	5						
Cursor Type	0110 1100 - off 0110 1101 - on	72 73	6						
Busy	Output Only	—	7						
Rapid Load	0110 1110 - off 0110 1111 - on	76 77	—						
Power Down	0111 0000 - off 0111 0001 - on	—	—						
Get Character	10000100	84		O	√	—	—	√ (see note 3)	√ (see note 3)
Get Cursor Location	10000010	82		O	√	—	—	—	—
Get Display Control Flags	10000001	81		O	√	—	—	—	—
Inc/Dec Cursor	1000100X	88 89		I	√	—	—	—	√ (see note 2)
Shift Right	10001111	8F		I	—	—	√	√	√
Shift Left	10001101	8D		I	—	—	√	√	√
Rotate Right	10001110	8E		I	—	√	—	√	√
Rotate Left	10001100	8C		I	—	√	—	√	√
Clear	10001010	8A		I	—	—	√	√	√
Reset Busy (Abort)	10001011	8B		I	√	—	—	—	—

NOTE: 1. Associated Bus Line for display control flags. Status appears on Bus Line on $\overline{MRD}$ input following a get control flags instruction.
2. Only if busy is due to Load Character.
3. See Instruction Set for special precautions.

X = Variable Data Y = Flag State
Short Busy is 5 to 10 periods of master oscillator, or 125 μsec. at 82 KHz.
Long Busy is up to 160 periods of master oscillator, or 2 msec. at 82 KHz.
Input Instructions are accomplished when $\overline{MWR}$ and $\overline{CS}$ are held low.
Output Instructions are accomplished when $\overline{MRD}$ and $\overline{CS}$ are held low.
(An output instruction must have been previously written.)

DISPLAY DRIVE LSI REQUIREMENTS

Number of Characters	8	16	20	32
Number of 0550 Required	1	1	1	1
Number of 0551 Required	1	2	3	5

Load Character
This instruction loads a specific character into a previously specified location. The instruction code is 0XXXXXXX where the 7 bit ASCII data must be the 64 character subset corresponding to hex addresses 20 through 5F. This instruction creates a long busy and cannot be performed during an existing busy condition or a power down. During the busy time, the ASCII data is loaded into a memory location which corresponds to the display position held in the cursor location register.

Load Cursor Location
This instruction sets the cursor location. The instruction code is 000XXXXX where XXXXX can be any binary number 0 through 31. The cursor location serves as a pointer to one of the 32 display positions. Zero corresponds to the 1st location and 31 corresponds to the 32nd location. The left most position is the 0 location and displays of less than 32 characters use positions 0, 1, 2.... N.

Set Display Control Flag
This instruction sets or resets the individual flags which control the display and enable special instructions. The instruction code is 011XXXXY, where the XXXX is a binary number 0 through 8 which corresponds to one of the 9 flag registers, and the Y is the flag state. Table II gives the flag, the flag address, and the I/O bus on which the flag contents appear after the get display control flag instruction.

Get Character
This instruction enables an output command ($\overline{MRD}$ = 0) to fetch the ASCII code for the character pointed to by the cursor location register. After a load cursor location instruction, a time of 160 oscillator periods must be allowed before the Get Character instruction will output correct data. Bus 7 contains the Busy status.

Get Cursor Location
This instruction enables a subsequent output command ($\overline{MRD}$ = 0) to fetch the cursor location. Bus 0-4 contain the cursor location, Bus 5-6 float, and Bus 7 contains the Busy status.

Get Display Control Flags
This instruction enables an output command ($\overline{MRD}$ = 0) to fetch the status of the display control flag registers. See the Instruction Set Table on page 4 for details of the positioning of the flags on the bus.
Note: Any "Get" command need be given only once. Being stored on the chip, it may be used until a different "Get" instruction is needed.

Inc/Dec Cursor
The instruction code is 1000100X, where X = 1 will cause an immediate advancement of the cursor one position to the right, and X = 0 will cause an immediate advancement of one position to the left.

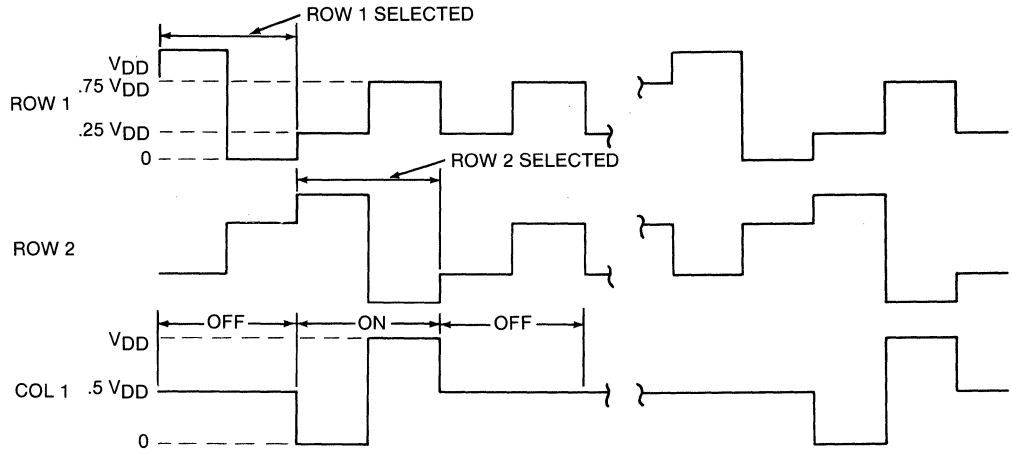
Shift
The shift right (left) instruction advances every character right (left) by one position and loads a blank into the first (last) position.

Rotate
The rotate right (left) instruction advances every character right (left) by one position and moves the last (first) character to the first (last) position.

Clear
This instruction loads a blank into every display location.

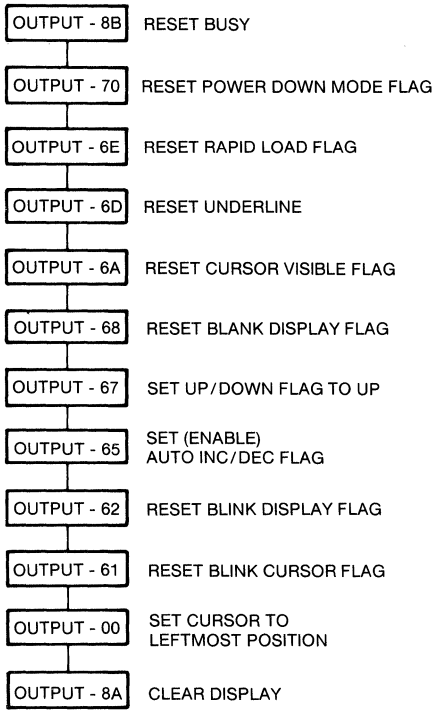
Reset Busy
This instruction aborts any instruction execution which has caused a busy signal, resets the busy flag, and allows the immediate loading of any instruction. Of course the aborted instruction may or may not have been completed.

TYPICAL OUTPUT WAVEFORMS

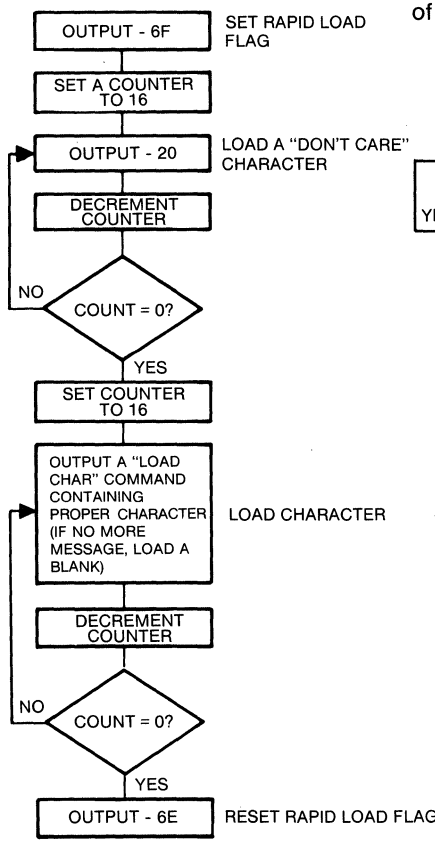


SAMPLE PROGRAMS

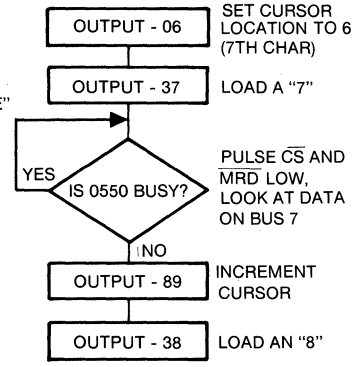
Initialize - This sequence, performed after system power up, will initialize everything, blank the cursor and set it at the left most position, and be ready for character loading from left to right.



Rapid Load Display - This sequence will display a 16 character message using the rapid load feature. Assume initialization was done as in example.



Character Load Display - Suppose the display shows the message SUM = 354.2 (left justified) and it is desired that this be changed to SUM = 357.8. Assume the initialization of the example.



Blink Cursor
A "1" in this flag register causes the cursor (the position pointed to by the cursor location register) to blink at approximately 1 Hz. The cursor visible flag must be set. The blinking is an on/off flashing for the underline cursor or an alternation between the character and solid fill (all 35 dots) for the full character cursor.

Blink Display
A "1" causes the entire display to flash on and off at approximately 1 Hz.

Auto Inc/Dec.
A "1" in this flag register causes the cursor location register to automatically be changed by one every time a character is read from or written to the character register. (See Up/Down flag.)

Up/Down
A "1" ("0") in this flag register works in conjunction with the Auto Inc/Dec flag to cause automatic incrementing (decrementing) of the cursor location register when a character is written to or read from the 0550.

Blank Display
A "1" in this flag register blanks the display, but leaves the display memory intact.

Visible Cursor
A "1" in this flag register causes the cursor (the position stored in the cursor location register) to be visible. The cursor cannot be blinked by the Cursor Blink flag unless it is made visible.

Cursor Type
A "1" in this register selects an underline on row 8 for the cursor, and a "0" selects a filled character, all 35 dots visible.

Power Down
A "1" in this flag register stops the oscillator and opens a switch in the resistor divider used in the multiple voltage generator circuit, so all LCD drive signals rise to the positive supply. To ensure ultra low power, the inputs should be near the power rails, and, if driven, OSC should be held high. During this condition memory is not lost, but the circuit will not respond properly to some instructions. See Table 1.

Busy
The busy state means the circuit is processing a previous instruction and cannot be given certain other instructions (see Table 1 for details). Busy status will appear on Bus 7 during all output instructions, (hex. code 81, 82, and 84).

Rapid Load
A "1" in this flag register stops the oscillator and resets the circuit. Each character load instruction loads a character starting with the 31st location until the mode is terminated. Rapid load can be initiated at any time and creates a busy signal. The Rapid Load instruction needs 32 loads to function properly. No other instructions should be given during a rapid load sequence. Rapid loading does not change the cursor location.

OPERATING NOTES

1. Oscillator

The on-chip oscillator is controlled by an external capacitor. The frequency must be high enough (at least 50KHz) to ensure a flicker free display. The recommended frequency is 82KHz for 64Hz update rate and 1Hz blink rate. The typical capacitor value is 50pf when using a 1mΩ resistor.

2. The Variable Resistor

The variable resistor indicated in the system block diagram may not be necessary, but could assist in display drive optimization and is also meant to imply possible temperature compensation. The resistor may need capacitor bypass.

3. Input Signals

The 0550 will interface with signals that come from circuits with different power supply magnitudes, either higher or lower. The constraints are (1) no signal should go more positive than the positive supply (therefore positive common is recommended) and (2) input levels must be satisfied. Input swings which are more negative than supply are allowed and input levels are biased toward the positive supply. Note that input levels are referenced to $V_{DD} = (V_{CC} - (-V_{DIS}))$.

4. Power Supply Voltages

Two negative voltages are supplied to this chip. The microcomputer ground ($-V_{BUS}$) is used for the low output level on the I/O bus. The negative display supply ($-V_{DIS}$) is chosen to give proper levels to the LCD. $-V_{DIS}$ must be equal to or lower than $-V_{BUS}$.

5. Initialization

This circuit doesn't power up in a particular state. The recommended power up sequence is a reset busy instruction (not necessary if a long busy time period is allowed to pass), setting of all display control flags, and a clear instruction.

6. Cascading Chips

If a display of over 32 characters is being driven and row lines are shared, two 0550's can be synchronized by giving them a fast load instruction simultaneously, and driving their oscillator pins with a common signal. The row drivers of one 0550 need not be used.

7. RMS Drive Voltages

The RMS voltages supplied to the LCD by the 0550 and 0551 Chip Set are as follows:

V_{DD} = voltage across chip, $(V_{CC}+V_{DIS})$

V_{RMS} on = .424 V_{DD}

V_{RMS} off = .293 V_{DD}

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Printed in U.S.A. 1/84, Rev A
Supersedes Previous Data

Intelligent Dot Matrix LCD Controller/Driver Kit

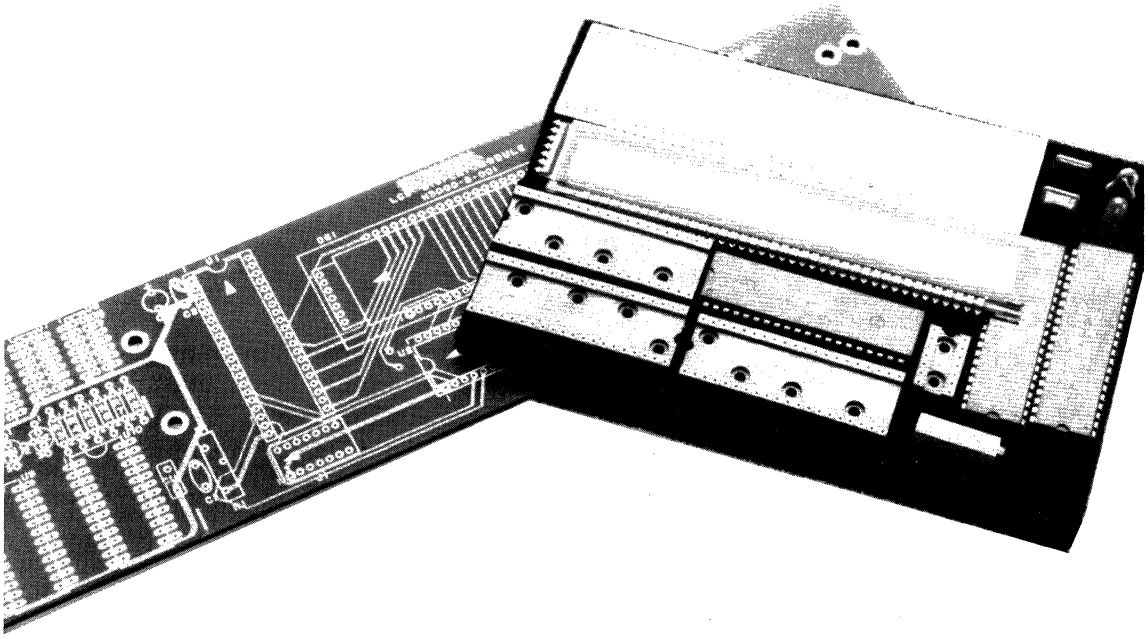
DESCRIPTION

Hughes' Intelligent Controller Evaluation Kit allows ease of design by providing a p.c. board with a complete interface circuit between 16 character dot matrix Liquid Crystal Display and the Hughes' 0550/0551 Intelligent LCD Controller/Driver.

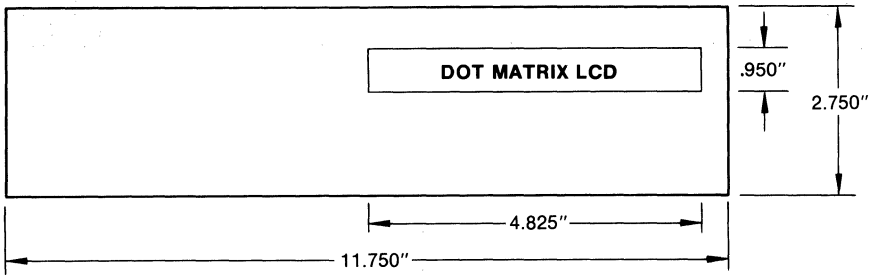
The p.c. board provides extra space (wire wrap) for users interface. Control of the display is handled through an 8 bit bi-directional I/O port. Completed circuit handles character decode, display manipulation, cursor control and all drive functions including refresh and generation of multi-level AC waveforms.

FEATURES

- Low power CMOS circuitry with power down mode
- Microprocessor compatible parallel interface
- 5 x 7 dot matrix; 16 character display
- ASCII input format
- Generation of all drive waveforms
- Cursor control
- Display manipulation, Instruction to accomplish shift, rotate, blank, blink, fast load, and power down
- Instructions to control output of characters, cursor position, display control flags, and busy status, etc.
- 11¾" x 2¾" p.c. board with users circuit space
- Low cost



P.C. BOARD OUTLINE DRAWING



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Printed in U.S.A. 6/83
Supersedes Previous Data

256 x 4 Static RAM — 1822C

DESCRIPTION

Hughes' 1822C is a static CMOS Random Access Memory organized as 256 words of 4 bits. The 1822C has separate data inputs and outputs and operates over a 4-6.5 voltage supply, (V_{DD}).

Two chip selects ($\overline{CS\ 1}$ and CS 2) are provided to simplify expansion within a memory system. The Output Disable (OD) signal controls the output data disabling and is useful in Wire — OR connections and Common Input/Output systems.

The address is decoded on the chip to access a four bit data word. When the chip is selected ($\overline{CS\ 1}$ = low and CS 2 = high) and the Output Disable signal is low (V_{SS}), the accessed data appears on the data output lines (DO 0-DO 3) and remains until OD goes high or the device is deselected ($\overline{CS\ 1}$ = high or CS 2 = low). After valid data appears, the address inputs may be changed immediately to select another data word.

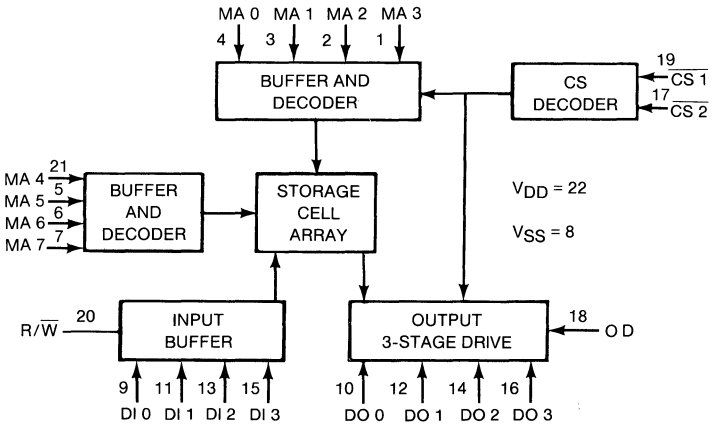
To write information, a valid address and data word is presented to the 1822C with the memory write enabled (R/$\overline{W}$ = low), and the chip selected. When using a common input/output data bus, the Output Disable signal must be high.

The 1822C is available in a 22 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix), or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

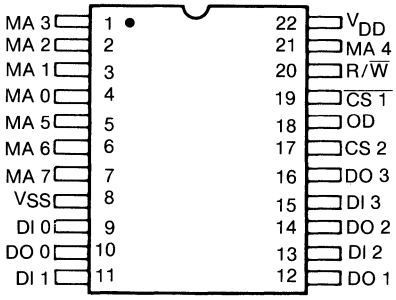
FEATURES

- Static CMOS Circuitry
- Interfaces Directly to 1802A Microprocessor
- Fast Access Time
  250ns at V_{DD} = 5V
- Low Quiescent and Operating Power
- No Precharge or Clock Required
- Industry Standard Pinout

FUNCTONAL DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T_A)
- Ceramic Package ..... − 55 to + 125°C
- Plastic Package ..... − 40 to + 85°C

DC Supply-Voltage Range (V_{DD})
(All Voltage values referenced to V_{SS} terminal)
- 1822C ..... − 0.5 to + 7 Volts

Storage Temperature Range (Tstg) ..... − 65 to + 150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full Package Temperature Range

CHARACTERISTICS	CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS Min.	LIMITS Typ.[1]	LIMITS Max.	UNITS
DC Operating Voltage Range	—	—	—	4	—	6.5	V
Input Voltage Range	—	—	—	V_{SS}	—	V_{DD}	V
STATIC ELECTRICAL CHARACTERISTICS at T_A = − 40 to + 125°C, V_{DD} ± 5%							
Quiescent Device Current, I_{DD}	—	0, 5	5	—	20	500	µA
Output Voltage: Low-level, V_{OL}	—	0, 5	5	—	0	0.1	V
High-Level, V_{OH}	—	0, 5	5	4.9	5	—	V
Input Low Voltage, V_{IL}	0.5, 4.5	—	5	—	—	1.5	V
Input High Voltage, V_{IH}	0.5, 4.5	—	5	3.5	—	—	V
Output Low (Sink) Current, I_{OL}	0.4	0, 5	5	1.6	2.6	—	mA
Output High (Source) Current, I_{OH}	4.6	0, 5	5	−1	−1.5	—	mA
Input Current, I_{IN}	—	0, 5	5	—	—	±5	µA
3-State Output Leakage Current, I_{OUT}	0, 5	0, 5	5	—	—	±5	µA
Operating Current[2], I_{DD1}	—	0, 5	5	—	4	8	mA
Input Capacitance, C_{IN}	—	0, 5	—	—	5	7.5	pF
Output Capacitance, C_{OUT}				—	5	7.5	pF
DATA RETENTION CHARACTERISTICS at T_A = − 55 to + 125°C; See Timing Diagram							

CHARACTERISTICS	CONDITIONS V_{DR} (V)	CONDITIONS V_{DD} (V)	LIMITS Min.	LIMITS Typ.[1]	LIMITS Max.	UNITS
Minimum Data Retention Voltage, V_{DR}	—	—	—	1.5	2	V
Data Retention Quiescent Current, I_{DD}	2	—	—	30	100	µA
Chip Select to Data Retention Time, C_{DR}	—	5	600	—	—	ns
Recovery to Normal Operation Time, t_{RC}	—	5	600	—	—	ns

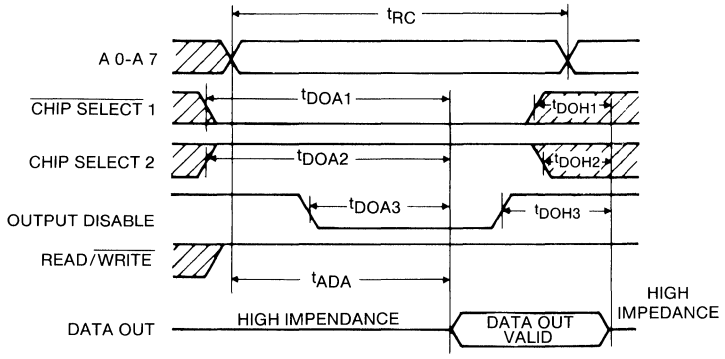
NOTES: 1. Typical Values are for T_A = + 25°C and nominal V_{DD}.
2. Outputs are open circuited; cycle time = 1 µs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = − 55°C to + 125°C, V_{DD} + 5%, t_r, t_f = 20ns. See Timing Diagram

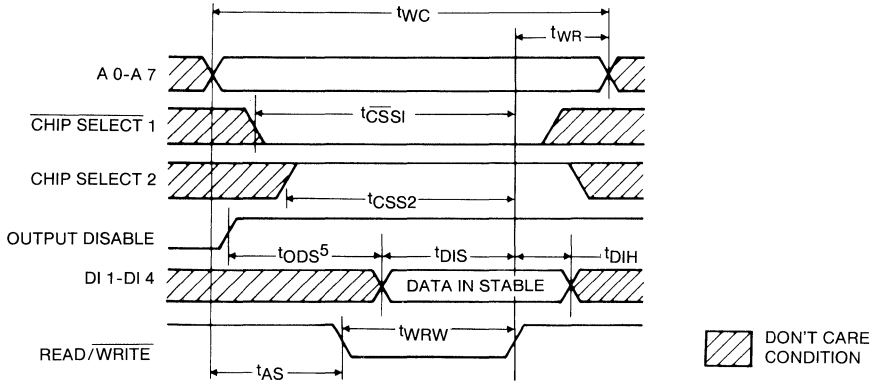
CHARACTERISTICS	V_{DD} (V)	1822C Min.[3]	1822C Typ.[4]	1822C Max.	UNITS
Read Cycle Times					
Read Cycle, t_{RC}	5	450	300	—	ns
Access from Address, t_{ADA}	5	—	250	450	ns
Output Valid from Chip-Select 1, t_{DOA1}	5	—	100	450	ns
Output Valid from Chip-Select 2, t_{DOA2}	5	—	100	450	ns
Output Active from Output Disable, t_{DOA3}	5	—	75	200	ns
Output Hold from Chip-Select 1, t_{DOH1}	5	20	—	—	ns
Output Hold from Chip-Select 2, t_{DOH2}	5	20	—	—	ns
Output Hold from Output Disable, t_{DOH3}	5	20	—	—	ns
Write Cycle Times					
Write Cycle, t_{WC}	5	500	300	—	ns
Address Set-up, t_{AS}	5	200	—	—	ns
Write Recovery, t_{WR}	5	50	—	—	ns
Write, Width, t_{WRW}	5	250	70	—	ns
Data input set-up, t_{DIS}	5	250	70	—	ns
Data input Hold, t_{DIH}	5	100	70	—	ns
Chip Select 1 Set-up, t_{CSS1}	5	250	100	—	ns
Chip-Select 2 Set-up t_{CSS2}	5	250	100	—	ns
Output Disable Set-up t_{ODS}	5	200	—	—	ns

NOTES: 3. Time required by a limit is to allow for the indicated function.
4. Typical values are for T_A = + 25°C and nominal V_{DD}.

Read cycle waveforms and timing diagram.

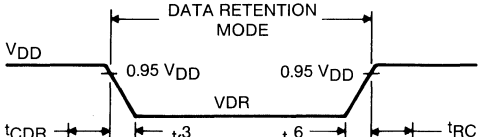


Write cycle waveforms and timing diagram.



NOTE 5: t_{ODS} is required for common I/O operation only; for separate I/O operations, Output Disable is Don't Care.

Low V_{DD} data retention waveforms and timing diagram.



NOTE 6: t_r, t_f >1 µS

SIGNAL DESCRIPTION

MA 0-MA 7: The eight input address lines select one of 256 four bit words. They are statically decoded on the chip to access the memory array.

DI 0-DI 3: These four data inputs are read into the memory when the chip is selected and the Memory Write control (R/$\overline{W}$ = low) is asserted.

DO 0-DO 3: These four data outputs reflect the accessed data when the chip is selected and the Output Disable control is inactive (OD = low).

$\overline{CS\ 1}$, CS 2: These two input chip select signals enable the RAM when $\overline{CS\ 1}$ is low and CS 2 is high.

OD, R/$\overline{W}$: These two input controls determine the mode of memory operation. Output Disable signal (OD) is inactive when performing a Read operation and enables the Data Output (DO 0-DO 3) three-state drivers. The Memory Write signal (R/$\overline{W}$) is activated to perform a Write operation. A detailed control table follows:

OPERATIONAL MODES

Mode	Inputs				Output
	$\overline{\text{Chip Select 1}}$ $\overline{\text{CS 1}}$	Chip Select 2 CS 2	Output Disable OD	$\overline{\text{Read Write}}$ R/$\overline{W}$	
Read	0	1	0	1	Read
Write	0	1	0	0	Data Input
Write	0	1	1	0	High Impedance
Standby	1	X	X	X	High Impedance
Standby	X	0	X	X	High Impedance
Output Disable	X	X	1	X	High Impedance

Logic 1 = High; Logic 0 = Low; X = Don't Care

NOTES: 1. When using an 1802A CPU controlled system, $\overline{MWR}$ is connected to R/$\overline{W}$ and $\overline{MRD}$ is connected to OD.
2. For T^2L interfacing an external pull-up is recommended at each input.

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Printed in U.S.A. 10/83
Supersedes Previous Data

128 x 8 Static RAM — 1823C

DESCRIPTION

Hughes' 1823C is a static CMOS Random Access Memory organized as 128 words of 8 bits. The 1823 has 8 common data input and output terminals and operates over a 4-6.5 voltage supply, (V_{DD}).

Five chip selects (CS 1, $\overline{CS\ 2}$, $\overline{CS\ 3}$, CS 4 and $\overline{CS\ 5}$) are provided to simplify expansion within a memory system. The Memory Read ($\overline{MRD}$) signal controls the output data enabling and is useful in direct connection to a processor bidirectional data bus.

The address is decoded on the chip to access an 8 bit data word. When the chip is selected ($\overline{CS\ 2}$, $\overline{CS\ 3}$ and $\overline{CS\ 5}$ = low and CS 1 and CS 4 = high) and the $\overline{MRD}$ signal is low (V_{SS}) the accessed data appears on the data output lines (DO 0-DO 7). They remain valid until $\overline{MRD}$ goes high or the device is de-selected. After valid data appears, the address inputs may be changed immediately to select another data word.

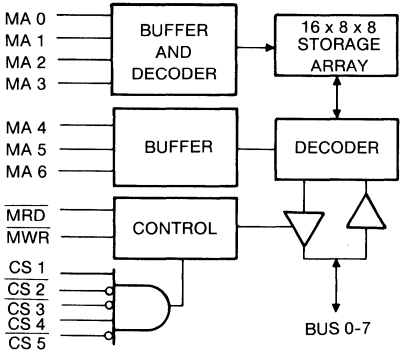
To write information a valid address and data word is presented to the 1823C with the Memory Write enabled ($\overline{MWR}$ = low), and the chip selected. During a write operation, the $\overline{MRD}$ signal must be high.

The 1823C is available in a 24 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

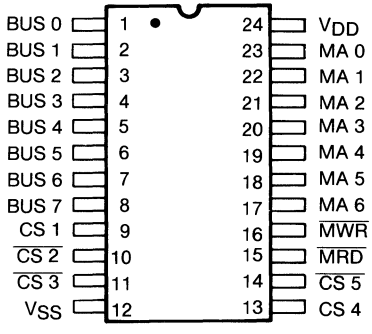
FEATURES

- Static CMOS Circuitry
- Byte wide organization
- Interfaces directly to 1802A and most microprocessors.
- Fast access time 250ns at V_{DD} = 5V
- Low quiescent and operating power
- No precharge or clock required
- Industry standard pinout

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T_A)
- Ceramic Package ..... − 55 to + 125°C
- Plastic Package ..... − 40 to + 85°C

DC SUPPLY—Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- 1823C ..... − 0.5 to + 7 Volts

Storage Temperature Range (T_{stg}) .... − 65 to + 150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full Package Temperature Range

CHARACTERISTICS	CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS Min.	LIMITS Typ.[1]	LIMITS Max.	UNITS
DC Operating Voltage Range	—	—	—	4	—	6.5	V
Input Voltage Range	—	—	—	V_{SS}	—	V_{DD}	V
STATIC ELECTRICAL CHARACTERISTICS at T_A = − 55 to + 125°C, V_{DD} ± 5%							
Quiescent Device Current, I_{DD}	—	0, 5	5	—	20	500	µA
Output Voltage: Low-Level, V_{OL}	—	0, 5	5	—	0	0.1	V
High-Level, V_{OH}	—	0, 5	5	4.9	5	—	
Input Low Voltage, V_{IL}	0.5, 4.5	—	5	—	—	1.5	V
Input High Voltage, V_{IH}	0.5, 4.5	—	5	3.5	—	—	
Output Low (Sink) Current, I_{OL}	0.4	0, 5	5	2.0	4.0	—	mA
Output High (Source) Current, I_{OH}	4.6	0, 5	5	− 1.0	− 2.0	—	
Input Current, I_{IN}	—	0, 5	5	—	—	± 5	µA
3-State Output Leakage Current, I_{OUT}	0, 5	0, 5	5	—	—	± 5	
Operating Current, I_{DD1}[2]	—	0, 5	5	—	4	8	mA
Input Capacitance, C_{IN}	—	0, 5	—	—	5	7.5	pF
Output Capacitance, C_{OUT}				—	5	7.5	

DATA RETENTION CHARACTERISTICS at T_A = − 55 to + 125°C; See Timing Diagram

CHARACTERISTICS	CONDITIONS V_{DR} (V)	CONDITIONS V_{DD} (V)	LIMITS Min.	LIMITS Typ.[1]	LIMITS Max.	UNITS
Min. Data Retention Voltage, V_{DR}	—	—	—	1.5	2	V
Data Retention Quiescent Current, I_{DD}	2	—	—	30	50	µA
Chip Select to Data Retention Time, C_{DR}	—	5	600	—	—	ns
Recovery to Normal Operation Time, t_{RC}	—	5	600	—	—	

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = − 55°C to + 125°C, V_{DD} ± 5%, t_r, t_f = 20ns. See Timing Diagram.

CHARACTERISTICS	V_{DD} (V)	LIMITS Min.[3]	LIMITS Typ.[1]	LIMITS Max.	UNITS
Read Cycle Times (See Figure 1)					
Read Cycle, t_{RC}	5	450	300	—	ns
Access from Address; t_{ADA}	5	—	250	450	ns
Output Valid from Chip Select, t_{DOA1}	5	—	100	450	ns
Output Valid from Chip-Select, t_{DOA2}	5	—	100	450	ns
Output Active from Memory Read, t_{AM}	5	—	75	200	ns
Data Hold from Chip-Select, t_{DOH1}	5	100	50	100	ns
Data Hold from Chip-Select, t_{DOH2}	5	100	50	100	ns
Data Hold from $\overline{MRD}$, t_{DOH3}	5	100	50	100	ns
Write Cycle Times (See Figure 2)					
Write Cycle, t_{WC}	5	500	300	—	ns
Address Set-up, t_{AS}	5	200	—	—	ns
Write Recovery, t_{WR}	5	75	—	—	ns
Write Width, t_{WRW}	5	250	70	—	ns
Data Input Set-up, t_{DIS}	5	250	70	—	ns
Data Input Hold, t_{DIH}	5	100	70	—	ns
Chip Select Set-up, t_{CSS1}	5	250	100	—	ns
Chip-Select Set-up t_{CSS2}	5	250	100	—	ns

NOTE: 1. Typical values are for T_A = + 25°C and nominal V_{DD}.
2. Outputs open circuited; cycle time = 1 µs
3. Time required by a limit is to allow for the indicated function.

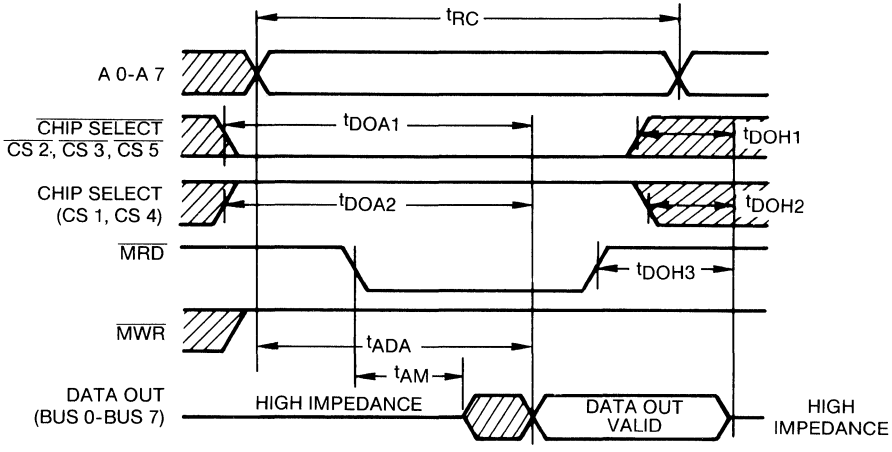


Figure 1 — Read cycle waveforms and timing diagram.

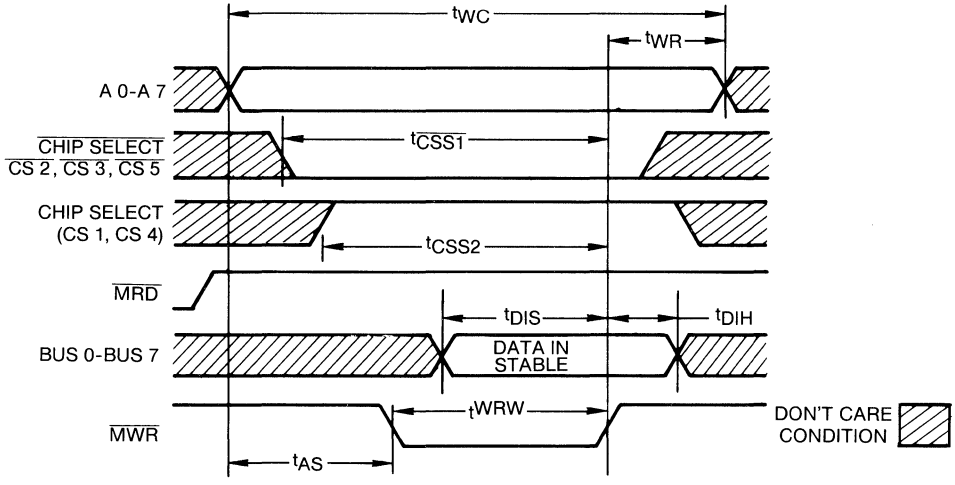
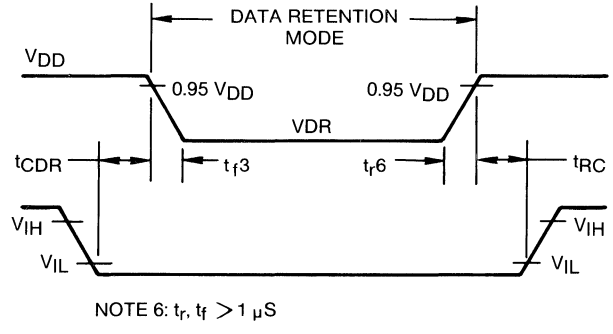


Figure 2 — Write cycle waveforms and timing diagram.



NOTE 6: t_r, t_f $>1\ \mu S$

Figure 3 — Low V_{DD} data retention waveforms and timing diagram.

SIGNAL DESCRIPTION

MA 0-MA 6: The seven input address lines select one of 128 eight bit words. They are statically decoded on the chip to access the memory array.

BUS 0-BUS 7: These eight data lines are read into the memory when the chip is selected and the Memory Write control is active (MWR = low). They become data outputs and carry the accessed data when the chip is selected and the Memory Read Control is active ($\overline{MRD}$ = low).

CS 1, $\overline{CS\ 2}$, $\overline{CS\ 3}$, CS 4, $\overline{CS\ 5}$: These five input chip select signals enable the RAM when $\overline{CS\ 2}$, $\overline{CS\ 3}$, and $\overline{CS\ 5}$ are low and CS 1 and CS 4 are high.

$\overline{MRD}$, $\overline{MWR}$: These two input controls determine the mode of memory operation. The memory read signal ($\overline{MRD}$) is active when performing a Read operation and enables the Data Output (BUS 0-BUS-7) three-state drivers. The Memory Write signal ($\overline{MWR}$) is activated to perform a Write operation. A detailed control table follows:

OPERATIONAL MODES

FUNCTION	$\overline{MRD}$	$\overline{MWR}$	CS 1	$\overline{CS\ 2}$	$\overline{CS\ 3}$	CS 4	$\overline{CS\ 5}$	BUS TERMINAL STATE
Read	0	X	1	0	0	1	0	Storage State of Addressed Word
Write	1	0	1	0	0	1	0	Input High-Impedance
Stand-by	1	1	1	0	0	1	0	High-Impedance
Not Selected	X	X	0	X	X	X	X	High-Impedance
	X	X	X	1	X	X	X	
	X	X	X	X	1	X	X	
	X	X	X	X	X	0	X	
	X	X	X	X	X	X	1	

Logic 1 = High Logic 0 = Low X = Don't Care

NOTE: For T^2L interfacing an external pull-up is recommended at each point.

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Printed in U.S.A. 10/83
Supersedes Previous Data

32 x 8 Static RAM — 1824

DESCRIPTION

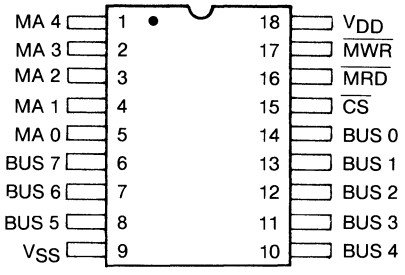
Hughes' 1824 is a static CMOS Random Access Memory organized as 32 registers of 8 bits, and contains a common bi-directional three state data bus enabled by the Memory Read ($\overline{MRD}$) signal. Data is written into the RAM when the chip is selected ($\overline{CS}$ = 0) and the Memory Write ($\overline{MWR}$) signal is asserted. Data is accessed by decoding the address lines and is transmitted onto the data bus when $\overline{CS}$ and $\overline{MRD}$ are enabled. The 1824 is fully decoded and does not require a precharge or clocking signal. This RAM may be used to provide a data stack or buffer storage for small systems.

The 1824 operates over a 4-10.5 voltage supply while the 1824C operates over a 4-6.5 voltage supply. The 1824 is available in an 18 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carriers (L suffix). Devices in chip form (H suffix) are available upon request.

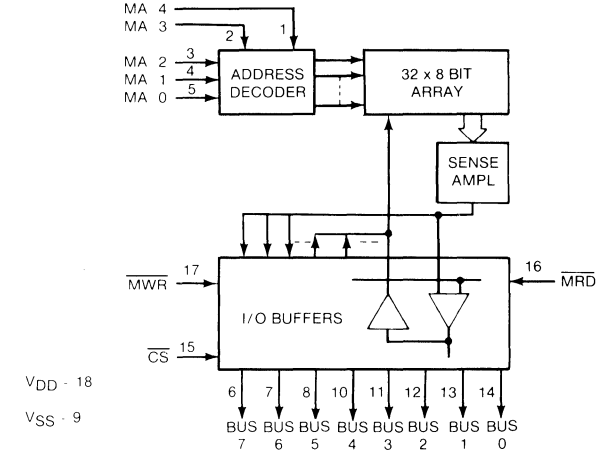
FEATURES

- Static Silicon Gate CMOS Circuitry
- Interfaces Directly to 1802A Microprocessor without Additional Components
- Access Time
  400ns typical at V_{DD} = 5V
  200ns typical at V_{DD} = 10V
- Single Voltage Supply
- Low Quiescent and Operating Power
- No Precharge or Clock Required

PIN CONFIGURATION



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T_A)
- Ceramic Package ..... − 55 to + 125°C
- Plastic Package ..... − 40 to + 85°C

DC Supply — Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- 1824 ..... − 0.5 to + 13 Volts
- 1824C ..... − 0.5 to + 7 Volts

Storage Temperature Range (T_{stg}) .... − 65 to + 150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full Package Temperature Range Unless Otherwise Specified

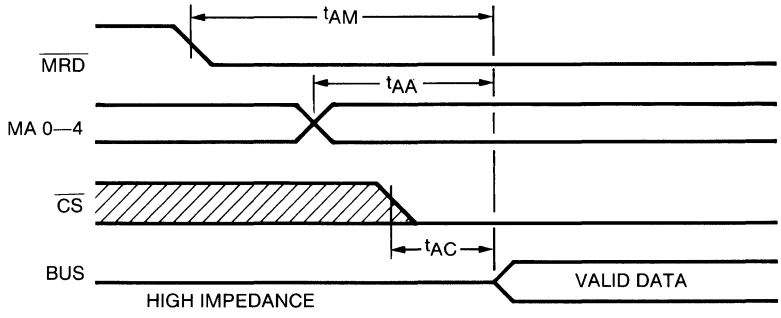
CHARACTERISTICS	CONDITIONS V_{DD} (V)	LIMITS 1824 Min.	1824 Max.	1824C Min.	1824C Max.	UNITS
Supply Voltage Range	—	4	10.5	4	6.5	V
Recommended Input Voltage Range	—	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Input Signal Rise and Fall Time, t_r, t_f,	5	—	5	—	5	µS
	10	—	2	—	—	

CHARACTERISTICS	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS 1824 Min.	1824 Typ.[1]	1824 Max.	1824C Min.	1824C Typ.[1]	1824C Max.	UNITS
STATIC ELECTRICAL CHARACTERISTICS at T_A = − 40 to + 85°C, V_{DD} ± 5%										
Quiescent Device Current, I_L	—	—	5	—	50	100	—	250	500	µA
	—	—	10	—	250	500	—	—	—	
Output Voltage	0.5	—	5	—	0	0.05	—	0	0.05	
Low Level, V_{OL}	0, 10	—	10	—	0	0.05	—	—	—	V
High Level, V_{OH}	0, 5	—	5	4.95	5	—	4.95	5	—	
	0, 10	—	10	9.95	10	—	—	—	—	
Input Voltage	—	0.5, 4.5	5	—	—	1.5	—	—	1.5	
Low Level, V_{IL}	—	1.9	10	—	—	3	—	—	—	V
High Level, V_{IH}	—	0.5, 4.5	5	3.5	—	—	3.5	—	—	
	—	1.9	10	7	—	—	—	—	—	
Output Drive Current	0, 5	0.4	5	1.8	2.2	—	1.8	2.2	—	
N-Channel (Sink) I_{DN}	0, 10	0.5	10	3.6	4.5	—	—	—	—	mA
P-Channel (Source), I_{DP}	0, 5	4.6	5	− 0.9	− 1.1	—	− 0.9	− 1.1	—	
	0, 10	9.5	10	− 1.8	− 2.2	—	—	—	—	
Input Leakage, I_{IL}, I_{IH}	Any Input	—	5, 10	—	± 0.1	± 1	—	± 0.1	± 1	µA
3-State Output Leakage	0, 5	0, 5	5	—	± 0.2	± 2	—	± 0.2	± 2	µA
Current I_{OUT}	0, 10	0, 10	10	—	± 0.2	± 2	—	—	—	
DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = − 40 to + 85°C, V_{DD} ± 5%; t_r, t_f = 10ns, C_L = 50 pF, R_L = 200KΩ										
Read Operation										
Access Time From Address Change, t_{AA}	—	—	5	—	400	710	—	400	710	ns
		—	10	—	200	320	—	—	—	
Access Time From Chip Select, t_{AC}[2]	—	—	5	—	300	710	—	300	710	ns
		—	10	—	150	320	—	—	—	
Output Active From $\overline{MRD}$, t_{AM}[2]	—	—	5	—	300	710	—	300	710	ns
		—	10	—	150	320	—	—	—	
Write Operation										
Write Pulse Width, t_{WW}	—	—	5	390	200	—	390	200	—	ns
		—	10	180	150	—	—	—	—	
Data Setup Time, t_{DS}	—	—	5	390	100	—	390	100	—	ns
		—	10	180	50	—	—	—	—	
Data Hold Time, t_{DH}	—	—	5	70	40	—	70	40	—	ns
		—	10	35	20	—	—	—	—	
Chip Select Setup Time, t_{CS}	—	—	5	425	210	—	425	210	—	ns
		—	10	215	110	—	—	—	—	
Address Setup Time, t_{AS}	—	—	5	640	500	—	640	500	—	ns
		—	10	390	300	—	—	—	—	
Address Hold Time, t_{AH}	—	—	5	—	100	—	—	100	—	ns
		—	10	—	50	—	—	—	—	
Power Dissipation, P_D (Chip Selected)	—	—	5	—	10	—	—	10	—	mW
		—	10	—	40	—	—	—	—	

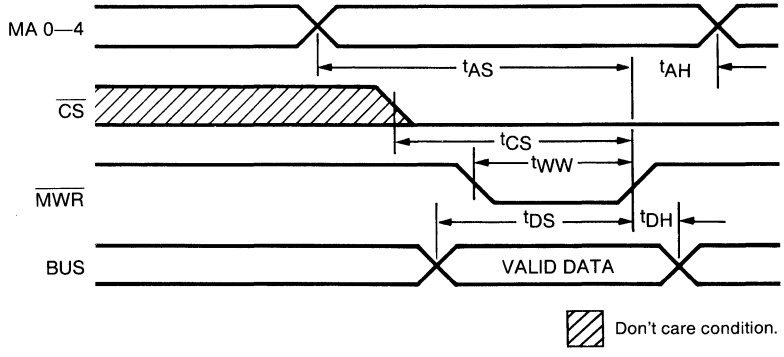
NOTE: 1. Typical values are for T_A = + 25°C and nominal V_{DD}

2. t_{AC} and t_{AM} are given as minimum times for valid data outputs. Longer times will initiate an earlier but invalid input.

Read Operation



Write Operation



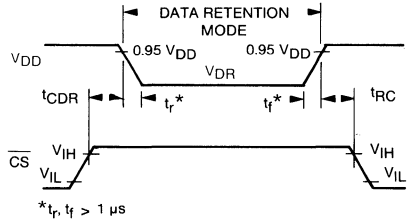
The dynamic characteristic table and the above timing diagrams represent maximum performance capability of the 1824. When used in direct system interface with the 1802A microprocessor, the timing relation will be determined by the clock frequency and timing signal generation of the microprocessor. In the latter case the following general timing conditions hold.

$t_{WW} = 2t_C$ $t_{AH} = 1.0t_C$ $t_{AS} = 4.5t_C$
$t_{DH} = 1.0t_C$ Data transfers from 1802A to Memory
$t_{DS} = 5.5t_C$

$\overline{MRD}$ occurs one clock period (t_C) earlier than address bus MA 0-MA 7
t_C = 1/1802A clock frequency

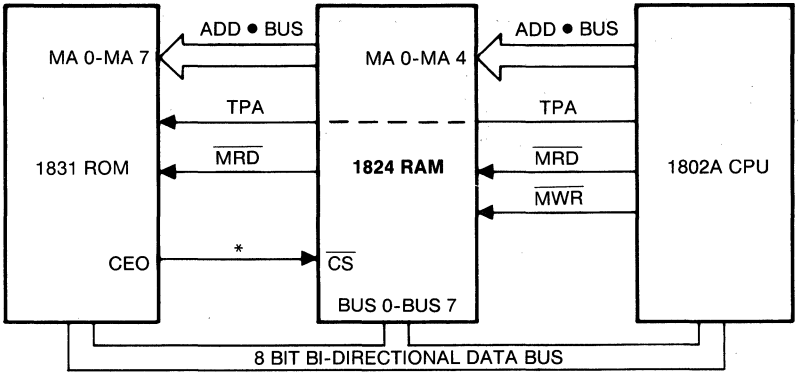
DATA RETENTION CHARACTERISTICS at T_A = – 40 to + 85°C

CHARACTERISTICS	CONDITIONS	V_{DD} (V)	1824		1824C		UNITS
			Min.	Max.	Min.	Max.	
Data Retention Voltage, V_{DR}	—	—	2.5	—	2.5	—	V
Data Retention Quiescent Current, I_{DD}	V_{DR} = 2.5V	—	—	50	—	250	µA
Chip Deselect to Data Retention Time, t_{CDR}	V_{DR} = 2.5V	5 10	600 300	— —	600 —	— —	ns
Recovery to Normal Operation Time, t_{RC}	V_{DR} = 2.5V	5 10	600 300	— —	600 —	— —	



Low V_{DD} data retention waveforms and timing diagram.

SYSTEM INTERCONNECT



*Chip select may be derived through (1) address decode, (2) CEO signal from ROM, or (3) always enabled (GND) per system requirements.

For a microprocessor system requiring a minimal amount of writable storage, the 1824 can be used as an adequate scratch pad memory and as stack storage for a wide range of control applications. No additional interface elements are required.

SIGNAL DESCRIPTION

MA 0-MA 4: These five input address lines select one of 32 eight bit words. They are statically decoded on the chip to directly access the register array.

BUS 0-BUS 7: These eight bi-directional three state data lines form a data bus common with the 1802A microprocessor. Data is written into the RAM or read from the RAM through these lines.

$\overline{\text{MRD}}$, $\overline{\text{MWR}}$, $\overline{\text{CS}}$: These three control signals determine chip selection bi-directional data control and operation of the chip when activated as follows:

$\overline{\text{MRD}}$ = Memory Read
$\overline{\text{MWR}}$ = Memory Write
$\overline{\text{CS}}$ = Chip Select (allows memory expansion)

FUNCTION	$\overline{\text{CS}}$	$\overline{\text{MRD}}$	$\overline{\text{MWR}}$	DATA LINES
Read	0	0	X	Output Mode
Write	0	1	0	Input Mode
Not Selected	1	X	X	High Impedance Mode
Standby	0	1	1	High Impedance Mode

Logic 1 = High Logic 0 = Low X = Don't Care
NOTE: $\overline{\text{MRD}}$ overrides $\overline{\text{MWR}}$

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HUGHES AIRCRAFT COMPANY

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Printed in U.S.A. 12/83
Supersedes Previous Data

512 x 8 Static ROM – 1831
1024 x 8 Static ROM – 1833

DESCRIPTION

Hughes' 1831 and 1833 are static CMOS Mask Programmable Read Only Memories. The 1831 and 1833 respond to a 16-bit address time multiplexed on the 8 address lines (MA 0-MA 7).

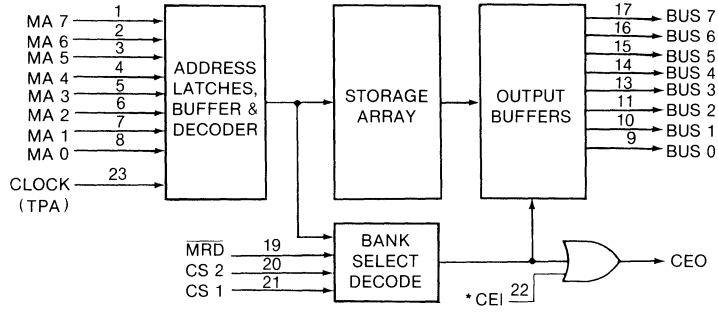
The eight most significant address lines are latched on chip by the clock input. This address may be decoded by a mask option to allow the 1831 to operate in any 512 word area, and the 1833 in any 1024 word area within the 65,536 byte memory space. In addition, three chip select signals may be decoded for simplified system interfacing. The Chip Enable Output (CEO) is activiated when the chip is selected and can be used as a disable control for the small RAM memory systems. Data is accessed from the memory by decoding the Address inputs and enabled on the data bus by the two Chip Selects (CS2 and CS1), the Memory Read ($\overline{MRD}$) and the upper address decode. The CEI signal may be used as an additional control of the ROM selected output signal, CEO, on the 1833.

The 1831 and 1833 operate over a 4-10.5 voltage range while the 1831C and 1833C operate over a 4-6.5 voltage range. The ROMs are available in a 24 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

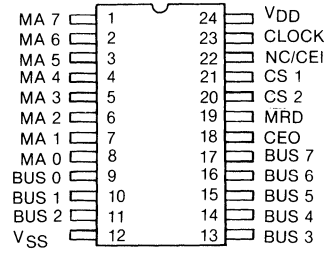
FEATURES

- Static Silicon Gate CMOS Circuitry
- Interfaces Directly with 1802A Microprocessor without Additional Components
- Access Time
  850ns Typical at V_{DD} = 5V
  350ns Typical at V_{DD} = 10V
- Single Voltage Supply
- Low Quiescent and Operating Power
- Static – No Clocks Required
- Chip Select and Address Location Within 64K Memory Space, Mask Programmable

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T_A)
- Ceramic Package . . . . . −55 to +125°C
- Plastic Package . . . . . −40 to + 85°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- 1831/1833 . . . . . −0.5 to +13V
- 1831C/1833C . . . . . −0.5 to + 7V

Storage Temperature Range (T_{stg}) . . −65 to +150°C

NOTE: Operating the device above the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full Package Temperature Range Unless Otherwise Specified.

CHARACTERISTICS	CONDITIONS	LIMITS								UNITS
	V_{DD} (V)	1831		1831C		1833		1833C		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Supply Voltage Range (At T_A = Full Package Temperature Range)	–	4	10.5	4	6.5	0	10.5	4	6.5	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Clock Pulse Width (TPA), t_{PAW}	5	200	–	200	–	200	–	200	–	ns
	10	70	–	–	–	70	–	–	–	
Address Setup Time, t_{AS}	5	50	–	50	–	75	–	75	–	ns
	10	25	–	–	–	40	–	–	–	
Address Hold Time, t_{AH}	5	150	–	150	–	100	–	100	–	ns
	10	75	–	–	–	50	–	–	–	

ELECTRICAL CHARACTERISTICS at T_A = −40 to + 85°C, V_{DD} = ± 5% except as noted

CHARACTERISTICS	CONDITIONS		1831			1831C			1833			1833C			UNITS
	V_O (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
STATIC															
Quiescent Device Current, I_L	–	5	–	0.01	50	–	0.02	200	–	0.01	50	–	0.02	200	µA
	–	10	–	1	200	–	–	–	–	1	200	–	–	–	
Output Drive Current,	0.4	5	0.55	–	–	0.55	–	–	0.8	–	–	0.8	–	–	mA
N-Channel (Sink), I_{DN}	0.5	10	1.3	–	–	–	–	–	1.8	–	–	–	–	–	
P-Channel (Source), I_{DP}	4.6	5	−0.35	–	–	−0.35	–	–	−0.8	–	–	−0.8	–	–	
	9.5	10	−0.65	–	–	–	–	–	−1.8	–	–	–	–	–	
Output Voltage	–	5	–	0	0.05	–	0	0.05	–	0	0.05	–	0	0.05	V
Low Level, V_{OL}	–	10	–	0	0.05	–	–	–	–	0	0.05	–	–	–	
Output Voltage	–	5	4.95	5	–	4.95	5	–	4.95	5	–	4.95	5	–	V
High Level, V_{OH}	–	10	9.95	10	–	–	–	–	9.95	10	–	–	–	–	
Input Leakage Current,	–	5	–	–	±1	–	–	±1	–	–	±1	–	–	±1	µA
I_{IL}, I_{IH}	–	10	–	–	±1	–	–	–	–	–	±1	–	–	–	
3-State Output Leakage	0,5	5	–	–	±1	–	–	±1	–	–	±1	–	–	±1	µA
Current, I_{OUT}	0,10	10	–	–	±1	–	–	–	–	–	±1	–	–	–	

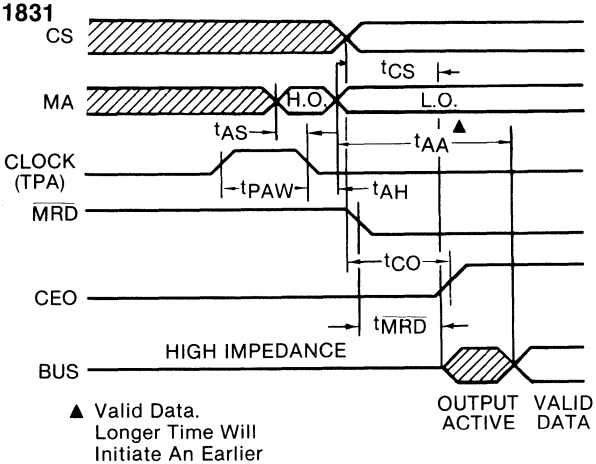
* Typical values are for T_A = 25°C and nominal V_{DD}

CHARACTERISTICS	CONDITIONS		1831			1831C			1833			1833C			UNITS
	V_O (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
DYNAMIC: t_r, t_f = 10ns, C_L = 50pF, R_L = 200 KΩ															
Access Time From Address	–	5	–	850	1000	–	850	1000	–	650	775	–	650	775	
Change, t_{AA}	–	10	–	350	400	–	–	–	–	350	425	–	–	–	ns
Access Time From Chip	–	5	–	700	800	–	700	800	–	500	625	–	500	625	
Select, t_{ACS}	–	10	–	250	300	–	–	–	–	275	310	–	–	–	ns
CEO From Address	–	5	–	500	600	–	500	600	–	120	170	–	120	170	
Change, t_{CA}	–	10	–	200	250	–	–	–	–	70	100	–	–	–	ns
Bus Contention Delay,	–	5	–	200	350	–	200	350	–	220	270	–	220	270	
t_D	–	10	–	100	150	–	–	–	–	130	150	–	–	–	ns
Daisy Chain Delay,	–	5	–	–	–	–	–	–	–	200	250	–	200	250	
t_{IO}	–	10	–	–	–	–	–	–	–	100	150	–	–	–	ns
Read Delay,	–	5	–	300	500	–	300	500	–	400	500	–	400	500	
$t_{\overline{MRD}}$	–	10	–	100	150	–	–	–	–	200	275	–	–	–	ns
Chip Select Delay,	–	5	–	600	750	–	600	750	–	250	320	–	250	320	
t_{CS}	–	10	–	200	300	–	–	–	–	125	180	–	–	–	ns
Chip Enable Output Delay	–	5	–	400	500	–	400	500	–	200	250	–	200	250	
Time From CS, t_{CO}	–	10	–	200	250	–	–	–	–	100	150	–	–	–	ns
Power Dissipation, P_D	–	5	–	15	–	–	15	–	–	30	–	–	30	–	
Cycle time = 2.5μs	–	10	–	60	–	–	–	–	–	120	–	–	–	–	mW

* Typical values are for T_A = 25°C and nominal V_{DD}

TIMING DIAGRAMS

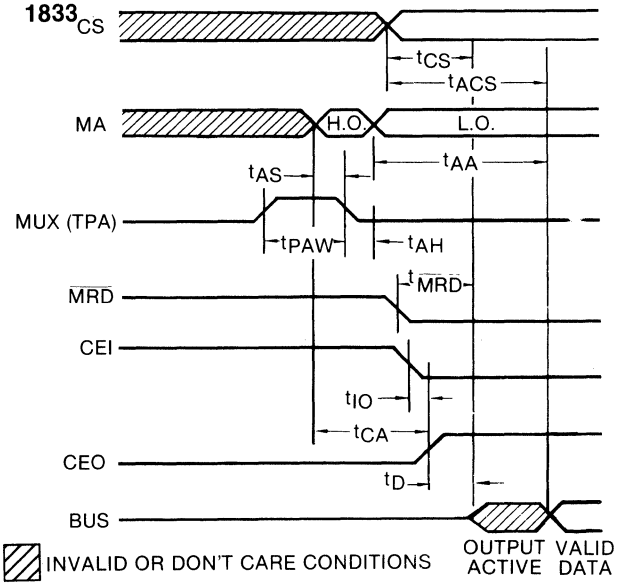
1831



▲ Valid Data. Longer Time Will Initiate An Earlier But Invalid Output

H.O. = High Order Address
L.O. = Low Order Address

1833



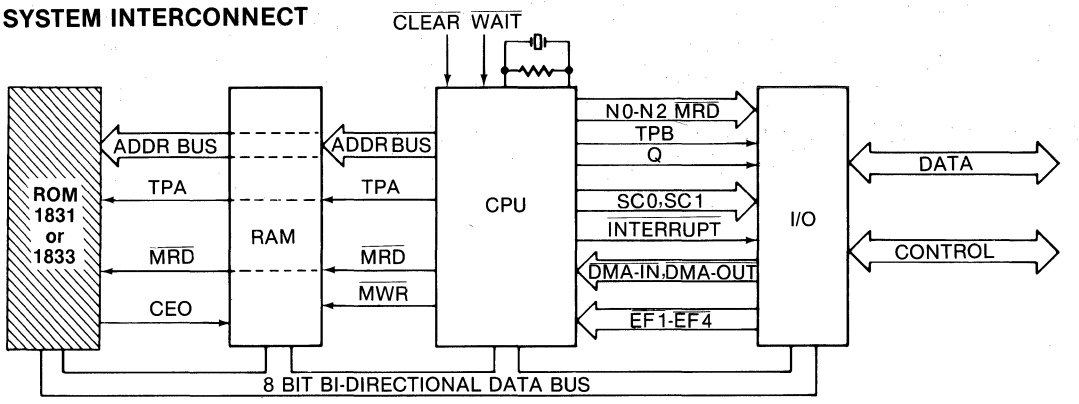
INVALID OR DON'T CARE CONDITIONS

The dynamic characteristic table and the above timing diagrams represent maximum performance capability of the 1831/1833. When used in direct system interface with the 1802A microprocessor, the timing relation will be determined by the clock frequency and timing signal generation of the microprocessor. In the latter case the following general timing conditions hold: $t_{AH} = 0.5t_C$

$t_{PAW} = 1.0t_C$

$\overline{MRD}$ occurs one clock period (t_C) earlier than address bus MA0 – MA7.
t_C = 1/1802A clock frequency.

SYSTEM INTERCONNECT



SIGNAL DESCRIPTION

MA0 – MA7: High order byte of a 16-bit memory address appears on the memory address lines (MA0–MA7) first. Those bits required by the memory system are strobed into internal address latches by Clock (TPA) input. The low order byte of 16-bit address appears on the address lines after the termination of TPA.

BUS0 – BUS7: These eight bi-directional three state data lines form a common bus with the 1802A microprocessor.

CLOCK (TPA): A timing signal from 1802A microprocessor (trailing edge of TPA) is used to latch the high order byte of the 16-bit memory address. The polarity of TPA is user mask programmable.

CS1, CS2, $\overline{\text{MRD}}$: Chip Select and Memory Read (output enable) signals. The polarity of the chip select signals are user mask programmable.

CEO, CEI: Chip Enable Output signal (CEO) is high when either the chip is selected or CEI is high (1833 only). CEO and CEI can be connected in daisy chain operation between several ROMs to control selection of RAM chips in a microprocessor system without additional components. The polarity of CEI is user mask programmable in the 1833.

ORDERING INFORMATION

Contact Hughes for prices and other information relating to ROMs. ROM order forms and instructions concerning means of data conveyance are available from Hughes Solid State Products or Hughes' Representatives.

HUGHES SOLID STATE PRODUCTS
HUGHES AIRCRAFT COMPANY

500 Superior Avenue
Newport Beach, CA 92663
Telephone (714) 759-2942 TWX: 910-596-1374

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Hughes International Service Co.
Schmaedel Str. 22, 8000 Munich, Germany
Telephone: 49-89-834. 7088 Telex: 5213856 HSPD

Printed in U.S.A.
Rev. N/C; 5/83*
Supersedes Previous Data

1800 CMOS Microprocessor Family
Static ROM

512x8 Static ROM – 1832
1024x8 Static ROM – 1834

DESCRIPTION

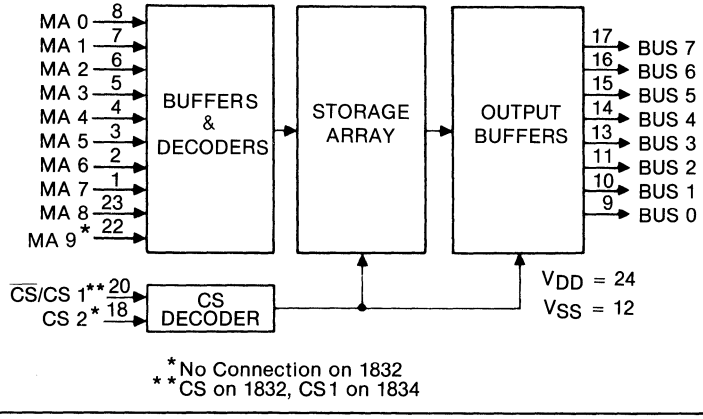
Hughes' 1832 and 1834 are static CMOS Mask Programmable Read Only Memories. When an address is presented on lines MA 0-MA 8 (1832) or MA 0-MA 9 (1834) the decoded word location is accessed and presented to the output sense amplifiers. This 8-bit word is enabled onto the lines by the CS signal in the 1832, or the CS 1 and CS 2 signals in the 1834, which can be used for memory expansion. The 1832 is a pin-for-pin compatible replacement for the 2704/8704 PROMs while the 1834 is a pin-for-pin compatible replacement for the 2708 PROM or 2308 ROM.

The 1832 and 1834 operate over a 4-10.5 voltage range while the 1832C and 1834C operate over a 4-6.5 voltage range. The ROMs are available in a 24 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

FEATURES

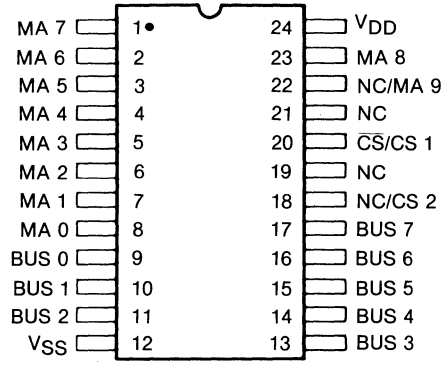
- Static Silicon Gate CMOS Circuitry
- Compatible with 1802A microprocessor at maximum speed
- Access Time – 1832
  - 850ns Typical at V_{DD} = 5V
  - 400ns Typical at V_{DD} = 10V
- Access Time – 1834
  - 575ns Typical at V_{DD} = 5V
  - 350ns Typical at V_{DD} = 10V
- Single Voltage Supply
- Low Quiescent and Operating Power
- Static – No Clocks Required
- Functional Replacement for Industry Standard 2704 (512 x 8) PROM or 2708 (1024 x 8) PROM

FUNCTIONAL DIAGRAM



*No Connection on 1832
**CS on 1832, CS1 on 1834

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T_A)
- Ceramic Package ..... −55 to +125°C
- Plastic Package ..... −40 to + 85°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- 1832/1834 ..... −0.5 to +13V
- 1832C/1834C ..... −0.5 to + 7V

Storage Temperature Range (T_{stg}) .... −65 to +150°C

NOTE: Operating the device above the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full package temperature range unless otherwise specified

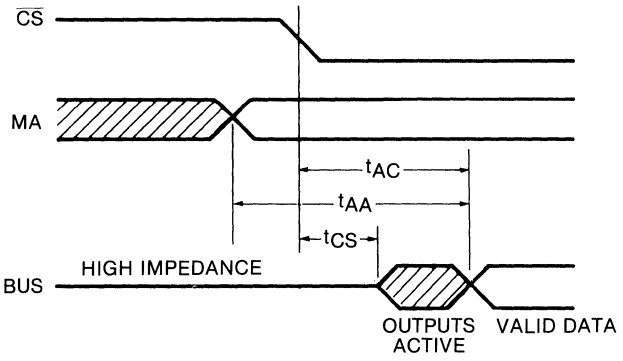
CHARACTERISTICS	CONDITIONS V_{DD} (V)	LIMITS 1832 Min.	1832 Max.	1832C Min.	1832C Max.	1834 Min.	1834 Max.	1834C Min.	1834C Max.	UNITS
STATIC										
Supply Voltage Range (At T_A = Full Package Temperature Range)	–	4	10.5	4	6.5	4	10.5	4	6.5	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} = ±5% except as noted

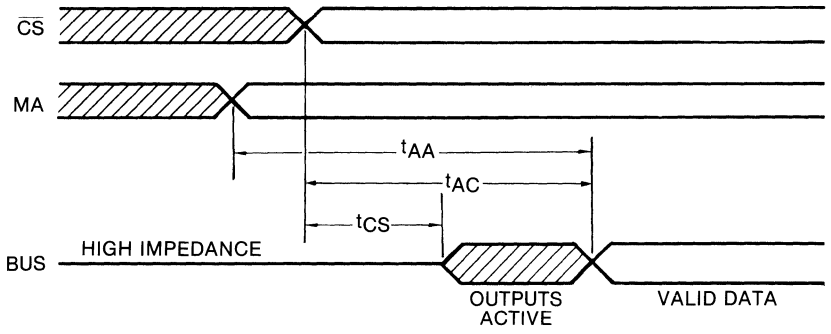
CHARACTERISTICS	CONDITIONS V_O (V)	V_{DD} (V)	1832 Min.	1832 Typ.*	1832 Max.	1832C Min.	1832C Typ.*	1832C Max.	1834 Min.	1834 Typ.*	1834 Max.	1834C Min.	1834C Typ.*	1834C Max.	UNITS
STATIC															
Quiescent Device Current, I_L	–	5	–	0.01	50	–	0.02	200	–	0.01	50	–	0.02	200	µA
	–	10	–	1	200	–	–	–	–	1	200	–	–	–	
Output Drive Current	0.4	5	0.55	–	–	0.55	–	–	0.8	–	–	0.8	–	–	mA
N-Channel (Sink), I_{DN}	0.5	10	1.30	–	–	–	–	–	1.8	–	–	–	–	–	
P-Channel (Source), I_{DP}	4.6	5	−0.35	–	–	−0.35	–	–	−0.8	–	–	−0.8	–	–	
	9.5	10	−0.65	–	–	–	–	–	−1.8	–	–	–	–	–	
Output Voltage	–	5	–	0	0.05	–	0	0.05	–	0	0.05	–	0	0.05	V
Low Level, V_{OL}	–	10	–	0	0.05	–	–	–	–	0	0.05	–	–	–	
Output Voltage	–	5	4.95	5	–	4.95	5	–	4.95	5	–	4.95	5	–	V
High Level, V_{OH}	–	10	9.95	10	–	–	–	–	9.95	10	–	–	–	–	
Input Leakage Current	–	5	–	–	±1	–	–	±1	–	–	±1	–	–	±1	µA
I_{IL}, I_{IH}	–	10	–	–	±1	–	–	–	–	–	±1	–	–	–	
3 State Ouput Leakage	0,5	5	–	–	±1	–	–	±1	–	–	±1	–	–	±1	µA
Current, I_{OUT}	0,10	10	–	–	±1	–	–	–	–	–	±1	–	–	–	
DYNAMIC: t_r, t_f = 10ns, C_L = 50pF, R_L = 200 KΩ															
Access Time From Address	–	5	–	850	1000	–	850	1000	–	575	750	–	575	750	ns
Change, t_{AA}	–	10	–	400	500	–	–	–	–	350	425	–	–	–	
Access Time From Chip	–	5	–	400	550	–	400	550	–	600	700	–	600	700	ns
Select, t_{AC}	–	10	–	200	250	–	–	–	–	325	410	–	–	–	
Chip Select Delay, t_{CS}	–	5	–	200	250	–	200	250	–	480	580	–	480	580	ns
	–	10	–	100	130	–	–	–	–	250	340	–	–	–	
Power Dissipation, P_D	–	5	–	15	–	–	15	–	–	30	–	–	30	–	mW
Cycle Time = 2.5 µs	–	10	–	60	–	–	–	–	–	120	–	–	–	–	

* Typical values are for T_A = 25°C and nominal V_{DD}

1832



1834

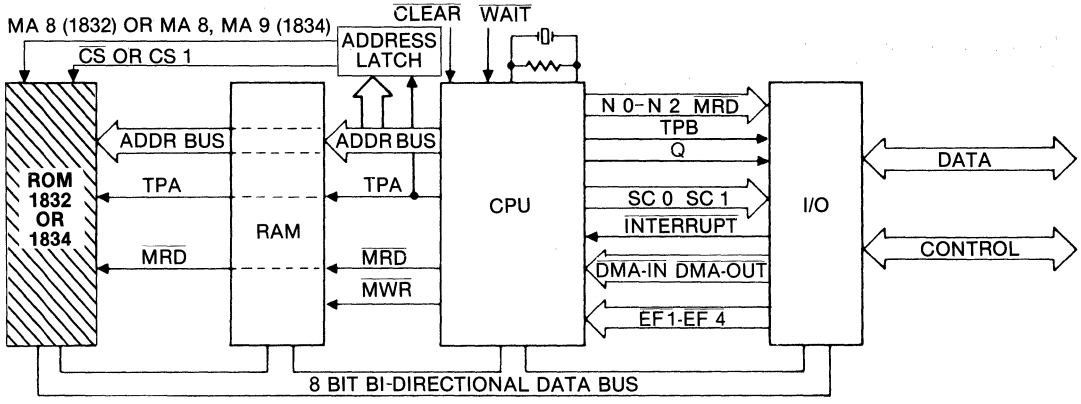


▨ INVALID OR DON'T CARE CONDITIONS

FUNCTIONAL OPERATION

These ROMs are completely static (no clocks are required). Decode of the input address selects a word from the storage array. The chip select signal enables the selected word to appear on the output bus line.

SYSTEM INTERCONNECT



SIGNAL DESCRIPTION

MA0-MA9: These address lines, MA0-MA8 (1832) or MA0-MA9 (1834), select a decoded word.

BUS0-BUS7: These eight bi-directional three-state data lines form a common bus with the 1802A microprocessor.

$\overline{CS}$, CS1, CS2: These chip select signals are provided for memory expansion. Outputs are enabled when $\overline{CS}$ = 0 in the 1832, while the polarity of CS1 and CS2 are user mask programmable in the 1834.

ORDERING INFORMATION

Contact Hughes for prices and other information relating to the ROMs. ROM order forms and instructions concerning means of data conveyance are available from Hughes Solid State Products or Hughes' representative.

HUGHES SOLID STATE PRODUCTS
HUGHES AIRCRAFT COMPANY

500 Superior Avenue
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Telephone: 49-89-834. 7088 Telex: 5213856 HSPD

Printed in U.S.A.
Rev. N/C 6/83
Supersedes Previous Data

2048 x 8 Static ROM—1835

DESCRIPTION

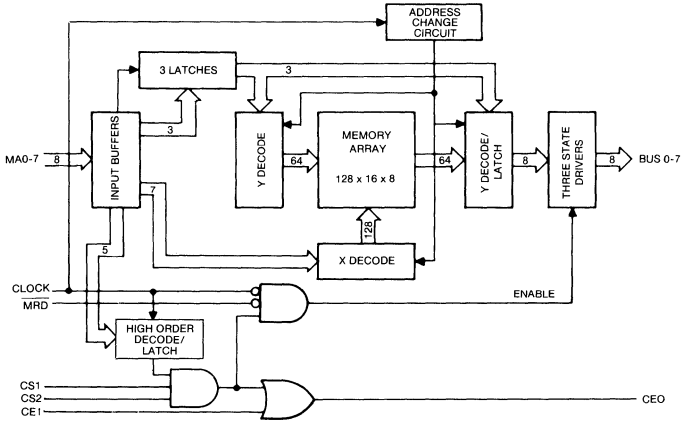
Hughes' 1835 is a static CMOS Mask Programmable Read Only memory. The 1835 responds to a 16 bit address time multiplexed on the eight address lines (MA 0-MA 7). The eight most significant address lines are latched on chip by the Clock input's negative transition. This address may be decoded by mask option to allow the 1835 to operate in any 2048 byte area within the 65,636 byte memory space. In addition, three chip select signals may be decoded for simplified system interfacing. The Chip Enable Output (CEO) is activated when the chip is selected and can be used as a disable control for small memory systems. The CEI signal may be used as an additional control of the ROM selected output signal, CEO. Data is accessed from memory by decoding the Address inputs and enabled on the data bus by the two Chip Selects (CS 2 and CS 1), the Memory Read (MRD) and the upper address decode. The polarity of the CS 2 and CS 1 signals are mask programmable.

The 1835 operates over a 4-10.5 voltage range while the 1835C operates over a 4-6.5 voltage range. The ROMs are available in a 24 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

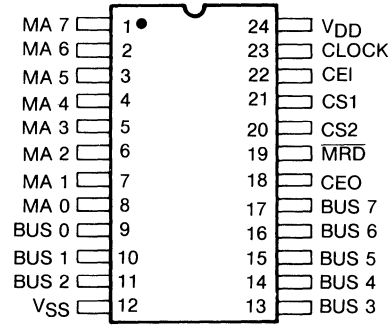
FEATURES

- Static CMOS Circuitry
- Interfaces Directly with 1802A Microprocessor without Additional Components
- Access Time
  900ns Typical at V_{DD} = 5V
  500ns Typical at V_{DD} = 10V
- Single Voltage
- Low Quiescent and Operating Power
- No Clocks Required
- Chip Select and Address Location within 64K Memory Space, Optionally Programmable

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T_A)
- Ceramic Package ..... − 55 to + 125°C
- Plastic Package ..... − 40 to + 85°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- 1835 ..... − 0.5 to + 11 Volts
- 1835C ..... − 0.5 to + 7 Volts

Storage Temperature Range (T_{stg}) ..... − 65 to + 150°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full Package Temperature Range Unless Otherwise Specified

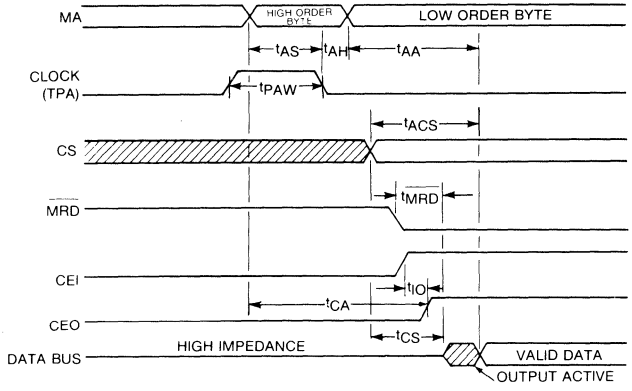
CHARACTERISTICS	CONDITIONS	LIMITS						UNITS
		1835			1835C			
	V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage Range (At T_A = full Package Temperature Range	—	4	—	10.5	4	—	6.5	V
Recommended Input Voltage Range	—	V_{SS}	—	V_{DD}	V_{SS}	—	V_{DD}	V
Clock Pulse Width (TPA), t_{PAW}	5	300	—	—	300	—	—	ns
	10	150	—	—	—	—	—	
Address Setup Time, t_{AS}	5	300	—	—	300	—	—	ns
	10	150	—	—	—	—	—	
Address Hold Time, t_{AH}	5	0	—	—	0	—	—	ns
	10	0	—	—	—	—	—	

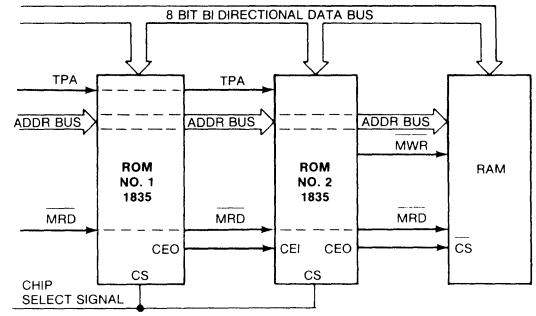
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = ± 5% except as noted.

CHARACTERISTICS	CONDITIONS		LIMITS						UNITS
			1835			1835C			
	V_O (V)	V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
STATIC									
Quiescent Device Current, IQ	—	5	—	1	100	—	1	100	µA
	—	10	—	10	400	—	—	400	
Input Voltage Low Level, V_{IL}	—	5	—	—	1.25	—	—	1.25	V
	—	10	—	—	2.5	—	—	—	
Input Voltage High Level, V_{IH}	—	5	3.75	—	—	3.75	—	—	V
	—	10	7.5	—	—	—	—	—	
Output (Sink) Current, I_{OL}	0.4	5	2	—	—	1.6	—	—	mA
	0.4	10	4	—	—	—	—	—	
Output (Source) Current, I_{OH}	4.5	5	2	—	—	1.6	—	—	mA
	9.5	10	4	—	—	—	—	—	
Input Leakage Current, I_{IL}, I_{IH}	0	5	—	± 1	± 5	—	± 1	5	µA
	0	10	—	± 1	± 10	—	—	—	
3 State Output Leakage Current, I_{OUT}	0, 5	5	—	± 1	± 1	—	± 1	± 10	µA
	0, 10	10	—	± 1	± 2	—	—	—	

CHARACTERISTICS	CONDITIONS		LIMITS						UNITS
			1835			1835C			
	V_O (V)	V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
DYNAMIC: t_r, t_f = 10 ns, C_L = 50 pF									
Power Supply Current, I_{DD} (Chip Selected 400 KHz)	—	5	—	3	—	—	3.5	—	mA
	—	10	—	10	—	—	—	—	
CEO from Address Change, t_{CA}	—	5	—	—	325	—	—	325	ns
	—	10	—	—	200	—	—	—	
Daisy Chain Delay, t_{IO}	—	5	—	—	150	—	—	150	ns
	—	10	—	—	100	—	—	—	
Read Delay, $t_{\overline{MRD}}$	—	5	—	—	200	—	—	200	ns
	—	10	—	—	100	—	—	—	
Chip Select Delay, t_{CS}	—	5	—	—	250	—	—	250	ns
	—	10	—	—	125	—	—	—	
Access Time from Chip Select, t_{ACS}	—	5	—	—	325	—	—	325	ns
	—	10	—	—	175	—	—	—	
Access Time From Address Change, t_{AA}	—	5	—	900	1300	—	900	1300	ns
	—	10	—	500	800	—	—	—	

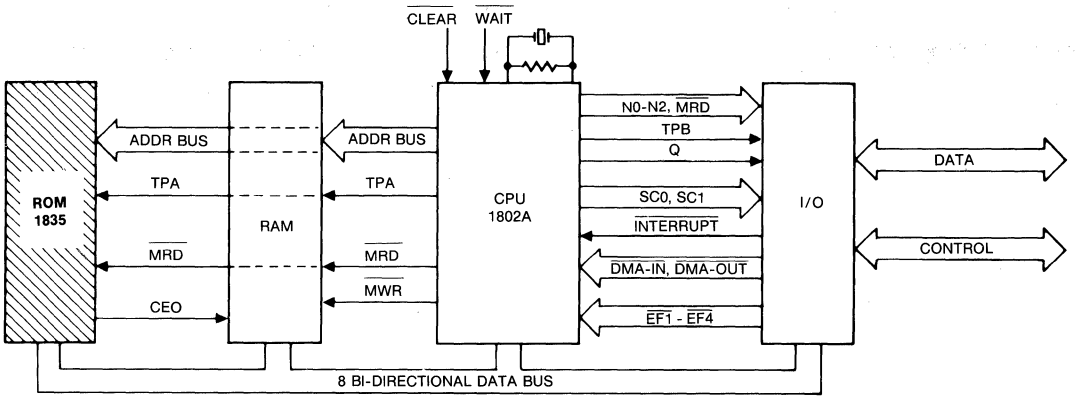
TIMING DIAGRAM





"Daisy Chaining" with CEI inputs and CEO outputs is used to avoid memory conflicts between ROM and RAM in a user system. In the above configuration, if ROM #1 was masked-programmed for memory locations 0000-$3FF_{16}$ and ROM #2 masked-programmed for memory locations 0400-$07FF_{16}$ for addresses from 0000-$07FF_{16}$ the RAM would be disabled and the ROM enabled. For locations above $07FF_{16}$ the ROM s would be disabled and RAM enabled.

SYSTEM INTERCONNECT



SIGNAL DESCRIPTION

MA 0-MA 7 — Under 1802A control the high order byte of a 16-bit memory address appears on the memory address lines, MA 0—MA 7, first. Three bits required by the ROM Address Decodes are strobed into internal address latches by Clock (TPA) input. The low order byte of 16 bit address appears on the address lines after the termination of TPA.

BUS 0-BUS 7: These eight bi-directional three state data lines form a common bus with the 1802A microprocessor.

CLK (TPA): A timing signal from 1802A microprocessor (trailing edge of TPA) is used to latch the high order byte of the 16 bit memory address.

CS 1, CS 2, $\overline{\text{MRD}}$: Chip select and memory read (output enable) signals. The polarity of the CS 1 and CS 2 signals are user mask programmable.

CEO, CEI: Chip Enable Output (CEO) signal is high when either the chip is selected or CEI is high. CEO and CEI can be connected in daisy chain operation between several ROMs to control selection of RAM chips in a microprocessor system without additional components.

ORDERING INFORMATION

Contact Hughes for price and other information relating to ROMs. ROM order forms and instructions concerning means of data conveyance are available from Hughes Solid State Products or Hughes' representatives.

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HUGHES AIRCRAFT COMPANY

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Printed in U.S.A. 6/83
Supersedes Previous Data

4096 x 8 Static ROM – 1837

DESCRIPTION

Hughes' 1837 is a static CMOS Mask Programmable Read Only Memory organized as 4096 x 8. No clocks are required. The 1837 responds to a 16 bit address time multiplexed on the eight address lines (MA 0 — MA 7).

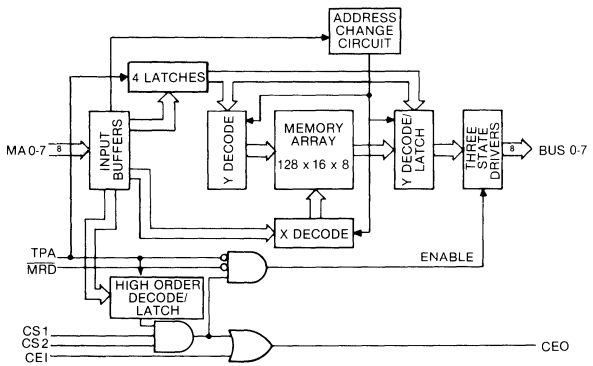
The most significant address lines are latched on chip by the Clock input's negative transition. This address may be decoded by mask option to allow the 1837 to operate in any 4096 byte area within the 65,636 byte memory space. In addition, three chip select signals may be decoded for simplified system interfacing. The Chip Enable Output (CEO) is activated when the chip is selected and can be used as a disable control for small memory systems. The CEI signal may be used as an additional control of the ROM selected output signal, CEO. Data is accessed from memory by decoding the Address inputs and enabled on the data bus by the two Chip Selects (CS 2 and CS 1), the Memory Read ($\overline{MRD}$) and the upper address decode.

The 1837 operates over a 4 – 10.5 voltage range while the 1837C operates over a 4 – 6.5 voltage range. The ROMs are available in a 24 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

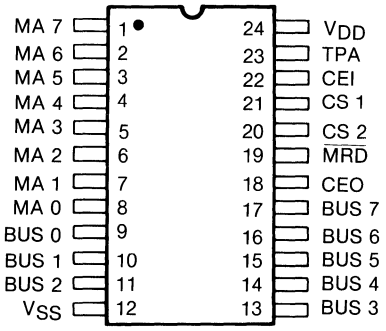
FEATURES

- Static CMOS Circuitry
- Interfaces Directly with 1802A Microprocessor without Additional Components
- Access Time
  750ns Typical at V_{DD} = 5V
  450ns Typical at V_{DD} = 10V
- Single Voltage Supply
- Low Quiescent and Operating Power
- No Clocks Required
- Chip Select and Address Location within 64K Memory Space, Optionally Programmable

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T_A)
- Ceramic Package ..... −55 to +125°C
- Plastic Package ..... −40 to + 85°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- 1837 ..... −0.5 to +13V
- 1837C ..... −0.5 to + 7V

Storage Temperature Range (T_{Stg}) .... −65 to +150°C

NOTE: Operating the device above the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full Package Temperature Range Unless Otherwise Specified

CHARACTERISTICS	CONDITIONS	LIMITS						UNITS
		1837			1837C			
	V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage Range (At T_A = Full Package Temperature Range	–	4	–	10.5	4	–	6.5	V
Recommended Input Voltage Range	–	V_{SS}	–	V_{DD}	V_{SS}	–	V_{DD}	V
Clock Pulse Width (TPA), t_{PAW}	5	300	–	–	300	–	–	ns
	10	150	–	–	–	–	–	
Address Setup Time, t_{AS}	5	300	–	–	300	–	–	ns
	10	150	–	–	–	–	–	
Address Hold Time, t_{AH}	5	0	–	–	0	–	–	ns
	10	0	–	–	–	–	–	

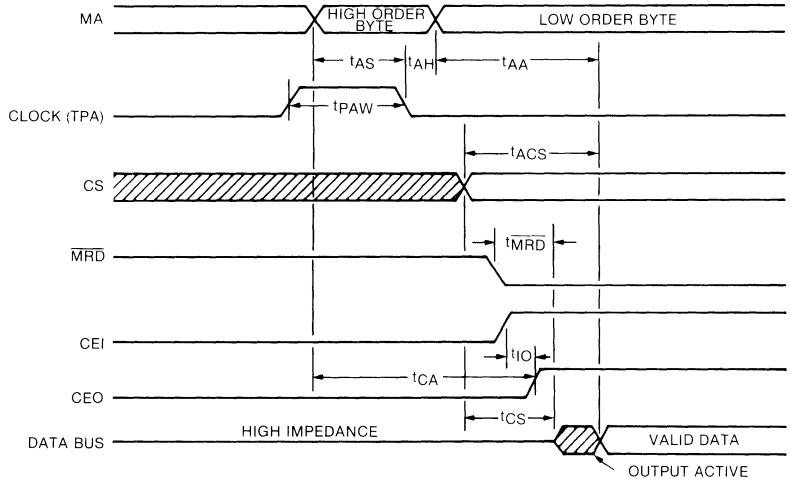
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = ±5% except as noted.

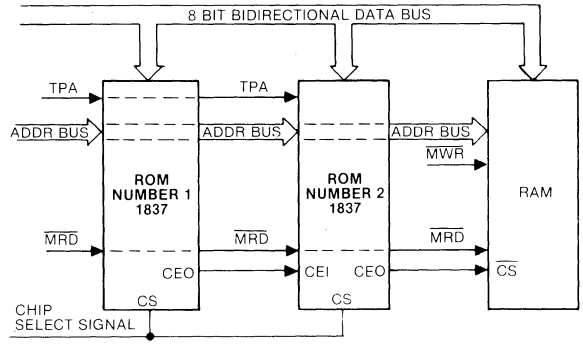
CHARACTERISTICS	CONDITIONS		LIMITS						UNITS
			1837			1837C			
	V_O (V)	V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
STATIC									
Quiescent Device Current, I_Q	–	5	–	1	50	–	1	50	µA
	–	10	–	1	100	–	–	–	
Input Voltage Low Level, V_{IL}	–	5	–	–	1.25	–	–	1.25	V
	–	10	–	–	3	–	–	–	
Input Voltage High Level, V_{IH}	–	5	3.75	–	–	3.75	–	–	V
	–	10	7	–	–	–	–	–	
Output (Sink) Current, I_{OL}	0.4	5	2.2	–	–	2.2	–	–	mA
	0.4	10	4.4	–	–	–	–	–	
Output (Source) Current, I_{OH}	4.5	5	−1.6	–	–	−1.6	–	–	mA
	9.5	10	−3.2	–	–	–	–	–	
Input Leakage Current I_{IL}, I_{IH}	0 0	5 10	– –	±1 ±1	±2 ±12	– –	±1 –	±2 –	µA
3 State Output Leakage Current, I_{OUT}	0,5 0,10	5 10	– –	±1 ±1	±12 ±2	– –	±1 –	±12 –	µA

ELECTRICAL CHARACTERISTICS, Cont.

CHARACTERISTICS	CONDITIONS		LIMITS						UNITS
			1837			1837C			
	V_O (V)	V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
DYNAMIC: t_r, t_f = 10 ns, C_L = 50pF									
Power Supply Current, I_{DD} (Chip Selected 400 KHz)	–	5	–	4	–	–	4	–	mA
	–	10	–	10	–	–	–	–	
CEO from Address Change, t_{CA}	–	5	–	–	325	–	–	325	ns
	–	10	–	–	200	–	–	–	
Daisy Chain Delay, t_{IO}	–	5	–	–	150	–	–	150	ns
	–	10	–	–	100	–	–	–	
Read Delay, $t_{\overline{MRD}}$	–	5	–	–	200	–	–	200	ns
	–	10	–	–	100	–	–	–	
Chip Select Delay, t_{CS}	–	5	–	–	250	–	–	250	ns
	–	10	–	–	125	–	–	–	
Access Time from Chip Select, t_{ACS}	–	5	–	–	325	–	–	325	ns
	–	10	–	–	175	–	–	–	
Access Time from Address Change, t_{AA}	–	5	–	750	1000	–	750	1000	ns
	–	10	–	450	600	–	–	–	

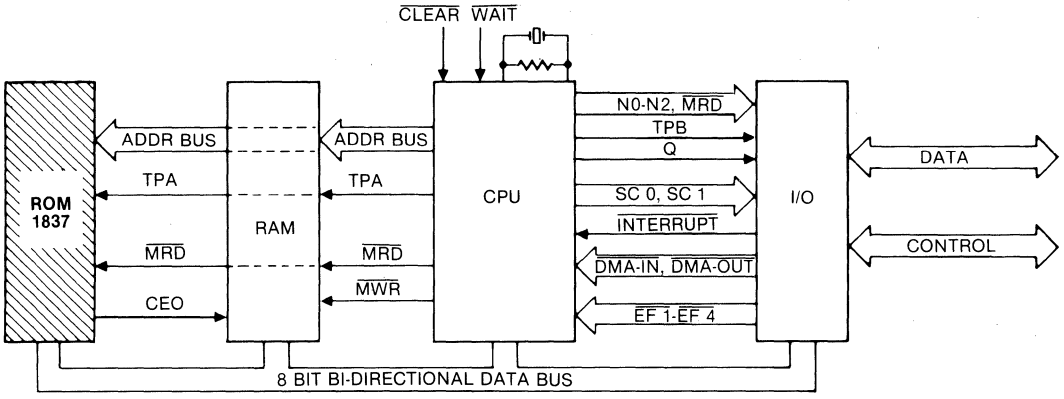
TIMING DIAGRAM





"Daisy Chaining" with CEI inputs and CEO outputs is used to avoid memory conflicts between the ROM and RAM in the user's system. In the above configuration, if ROM Number 1 was masked programmed for memory locations 0000-OFFF$_{16}$; and the ROM Number 2 masked programmed for memory locations 1000-1FFF$_{16}$; for addresses from 0000-1FFF$_{16}$, the RAM would be disabled and the ROM enabled. For locations above 1FFF$_{16}$ the ROMs would be ROM disabled and the RAM enabled.

SYSTEM INTERCONNECT



SIGNAL DESCRIPTION

MA 0 — MA 7: Under 1802A control, the high order byte of a 16 bit memory address appears first on the memory address lines (MA 0—MA 7). Three bits required by the ROM Address Decodes are strobed into the internal address latches by the Clock (TPA) input. The low order byte of the 16 bit address appears on the address lines after the termination of TPA.

BUS 0 — BUS 7: These eight bi-directional three state data lines form a common bus with the 1802A microprocessor.

CLOCK (TPA): A timing signal from the 1802A microprocessor (trailing edge of TPA) is used to latch the high order byte of the 16 bit memory address.

CS 1, CS 2, $\overline{\text{MRD}}$: The Chip Select and Memory Read (output enable) signals. The polarity of the CS 1 and CS 2 signals are user mask programmable.

CEO, CEI: Chip Enable Output (CEO) signal is high when either the chip is selected or CEI is high. CEO and CEI can be connected in a daisy chain operation between several ROMs to control the selection of RAM chips in a microprocessor system without additional components.

ORDERING INFORMATION

Contact Hughes for price and other information relating to ROMs. ROM order forms and instructions concerning means of data conveyance are available from Hughes Solid State Products or a Hughes' Representative.

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Telephone: 49-89-834. 7088 Telex: 5213856 HSPD

Printed in U.S.A.
Rev. N/C 6/83
Supersedes Previous Data

2048 x 8
CMOS Static ROM

2048 x 8 Static ROM – 23C16C

DESCRIPTION

Hughes' 23C16C is a CMOS Mask Programmable Read Only Memory organized as 2048 x 8. The ROM circuit is static and updates its outputs when any address changes. Two chip selects are included which are programmed for polarity with the same mask that programs the data pattern.

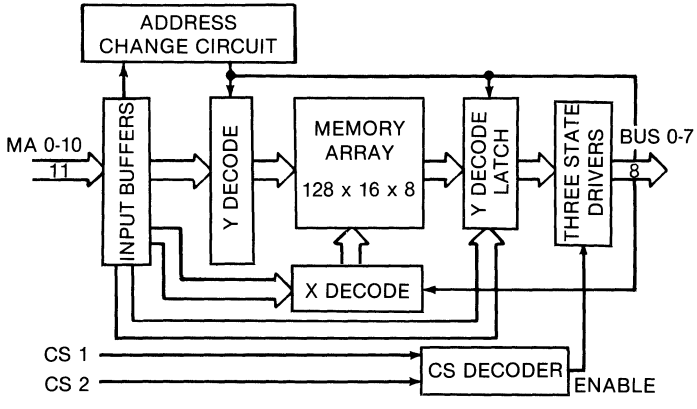
When the chip is selected, the address present on lines MA 0-MA 10 accesses data which is presented to the output sense amplifiers. The eight-bit output word is enabled onto the data lines by the chip select signals, which can be used for memory expansion. The 23C16C is a pin compatible replacement for the 2716 PROM.

The 23C16C operates over a 4-6.5 voltage range. The ROM is supplied in a 24 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

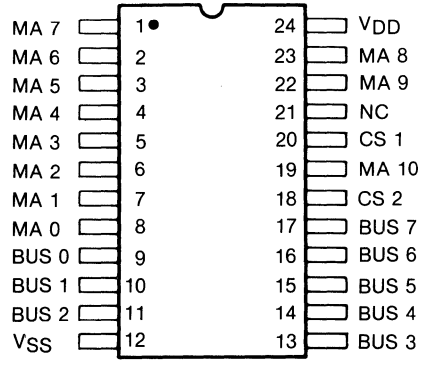
FEATURES

- Static CMOS Circuitry
- No Clocks are Required
- Compatible with 1802A Microprocessor at Maximum Speed
- Access Time
  900ns Typical at V_{DD} = 5V
- Single Voltage Supply
- Low Quiescent and Operating Power
- Functional Replacement for Industry Standard Type 2716 (2048 x 8) PROM

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Storage Temperature Range (T_{stg}) . . . . . −65 to +150°C

Operating Temperature Range (T_A)

Ceramic Package . . . . . −55 to +125°C

Plastic Package . . . . . −40 to +85°C

DC Supply-Voltage Range (V_{DD})

(All voltage values referenced to V_{SS} terminal)

23C16C . . . . . −0.5 to +7V

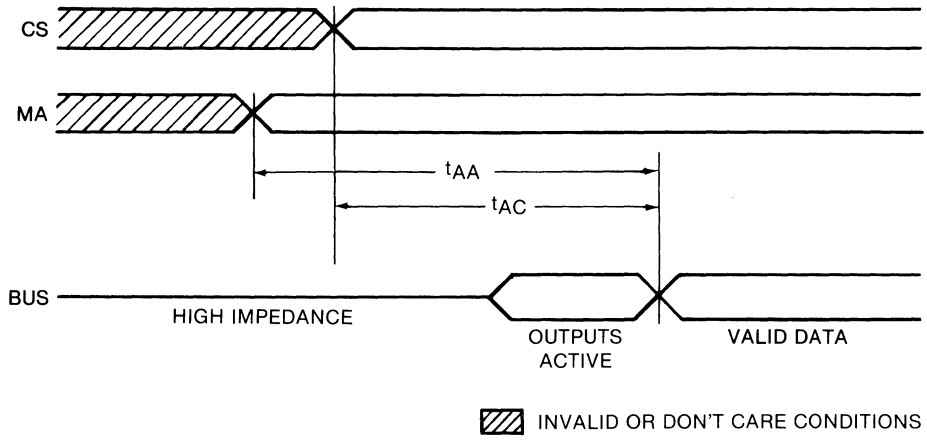
NOTE: Operating the device above the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full Package Range Unless Otherwise Specified

CHARACTERISTICS	CONDITIONS		LIMITS			UNITS
	V_O (V)	V_{DD} (V)	Min.	Typ.	Max.	
Supply Voltage Range (At T_A = Full Package Temperature Range)	–	–	4	–	6.5	V
Recommended Input Voltage Range	–	–	V_{SS}	–	V_{DD}	V

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = ±5% except as noted.

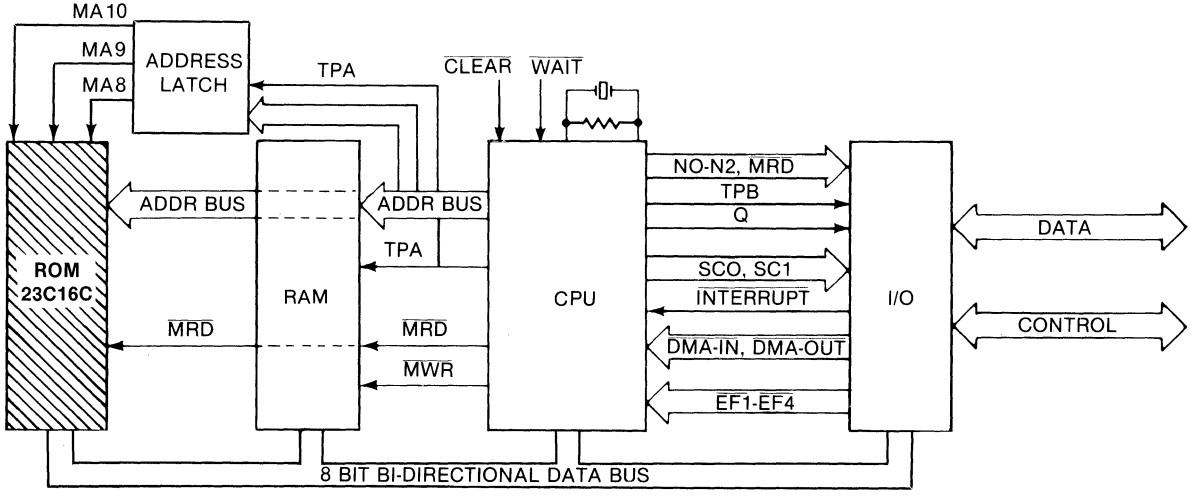
CHARACTERISTICS	CONDITIONS		LIMITS			UNITS
	V_O (V)	V_{DD} (V)	Min.	Typ.	Max.	
STATIC						
Quiescent Device Current, I_L	–	5	–	–	50	µA
Supply Current, I_{DD} (400KHz Addresses)	–	5	–	–	5.75	mA
Output Drive Current, N-Channel (Sink), I_{DN}	0.5	5	2	–	–	mA
P-Channel (Source), I_{DP}	4.5	5	2	–	–	mA
Output Voltage Low Level, V_{OL}	–	5	–	0	0.05	V
Output Voltage High Level, V_{OH}	–	5	4.95	5	–	V
Input Low Voltage V_{IL}	0.5,4.5	5	–	–	1.25	V
Input High Voltage, V_{IH}	0.5,4.5	5	3.75	–	–	V
Input Leakage Current I_{IL}, I_{IH}	0	5	–	±1	±1	µA
3 State Output Leakage Current, I_{OUT}	0.5	5	–	±1	±2	µA
DYNAMIC: t_r, t_f = 10 ns, C_L = 50pF; R_L = 200K Ω						
Access Time From Address Change, t_{AA}	–	5	–	900	1200	ns
Access Time From Chip Select, t_{AC}	–	5	–	330	425	ns



FUNCTIONAL OPERATION

This ROM is completely static (no clocks required). Decode of the input address selects a word from the storage array. The chip select signal enables the selected word to appear on the output bus line. Address rise and fall times should be less than 500 nsec.

SYSTEM INTERCONNECT



SIGNAL DESCRIPTION

MA0 – MA10: These address lines select a byte location. MA10 is the high order address bit.

BUS0 – BUS7: These eight three-state data lines form a common bus with the microprocessor.

CS1, CS2: These chip select signals are provided for memory expansion. Outputs are enabled when CS 1 and CS 2 are active. Polarity of CS 1 and CS 2 are user mask programmable.

ORDERING INFORMATION

Contact Hughes for price and other information relating to ROMs. ROM order forms and instructions concerning means of data conveyance are available from Hughes Solid State Products or Hughes' representatives.

HUGHES SOLID STATE PRODUCTS
HUGHES AIRCRAFT COMPANY

500 Superior Avenue
Newport Beach, CA 92663
Telephone (714) 759-2942 TWX: 910-596-1374

In Europe: Hughes Solid State Products
Hughes International Service Co.
Schmaedel Str. 22, 8000 Munich, Germany
Telephone: 49-89-834. 7088 Telex: 5213856 HSPD

Printed in U.S.A.
Rev. A; 5/83
Supersedes Previous Data

4096 x 8 CMOS Static ROM

4096 x 8 Static ROM – 23C32C

DESCRIPTION

Hughes' 23C32C is a CMOS Mask Programmable Read Only Memory, organized as 4096 x 8. The ROM circuit is static and updates its outputs when any address changes. Two chip selects are included which are programmed for polarity with the same mask that programs the data pattern.

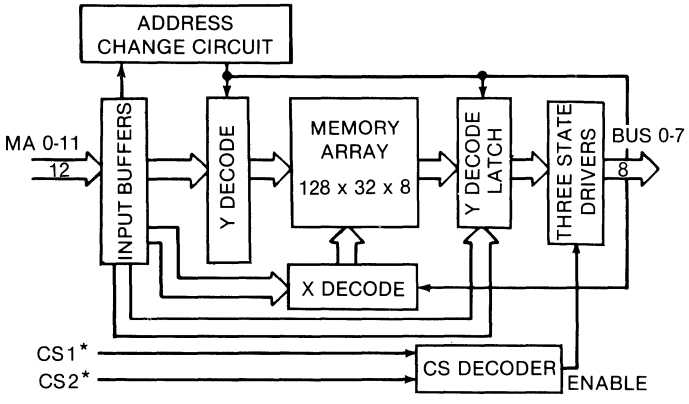
When the chip is selected (CS 1 and CS 2 are activated) the address present on lines MA 0 – MA 11 accesses data which is presented to the output sense amplifiers. The 3-bit output word is enabled onto the data lines by the chip select signals, which can be used for memory expansion. The 23C32C is a pin compatible replacement for the 2732 PROM.

The 23C32C operates over a 4-6.5 voltage range. The ROM is available in a 24 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

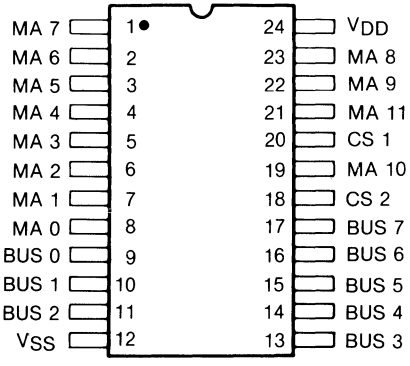
FEATURES

- Static CMOS Circuitry
- Functional Replacement for Industry Standard Type 2732 (4096 x 8) PROM
- Compatible with 1802A Microprocessor at Maximum Speed
- Access Time
  750ns Typical at V_{DD} = 5V
- Single Voltage Supply
- Low Quiescent and Operating Power
- Very Low Standby Power Mode – Less than 10μa, controlled by CS 1

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



* ACTIVE STATE IS MASK PROGRAMMABLE

ABSOLUTE MAXIMUM RATINGS

Storage Temperature Range (T_{stg}) . . . . −65 to +150°C

Operating Temperature Range (T_A)

Ceramic Package . . . . . −55 to +125°C

Plastic Package . . . . . −40 to + 85°C

DC Supply-Voltage Range (V_{DD})

(All voltage values referenced to V_{SS} terminal)

23C32C . . . . . −0.5 to + 7V

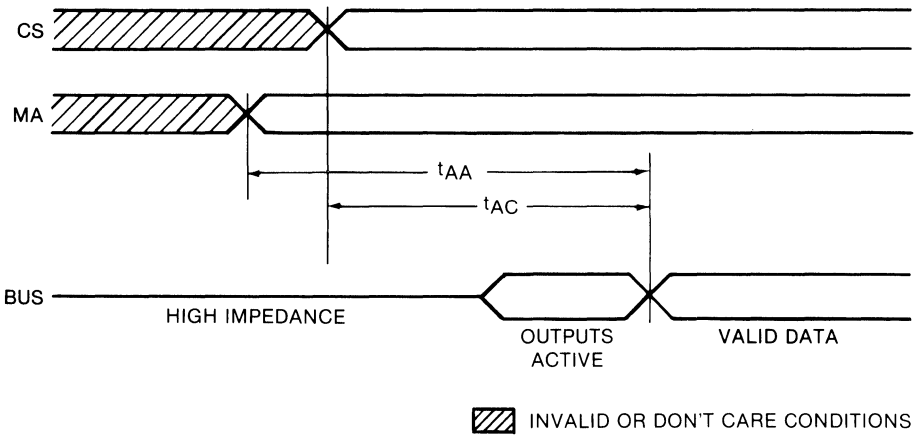
NOTE: Operating the device above the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full Package Range Unless Otherwise Specified

CHARACTERISTICS	CONDITIONS		LIMITS			UNITS
	V_O (V)	V_{DD} (V)	Min.	Typ.	Max.	
Supply Voltage Range (At T_A = Full Package Temperature Range)	–	–	4	–	6.5	V
Recommended Input Voltage Range	–	–	V_{SS}	–	V_{DD}	V

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = ±5% except as noted.

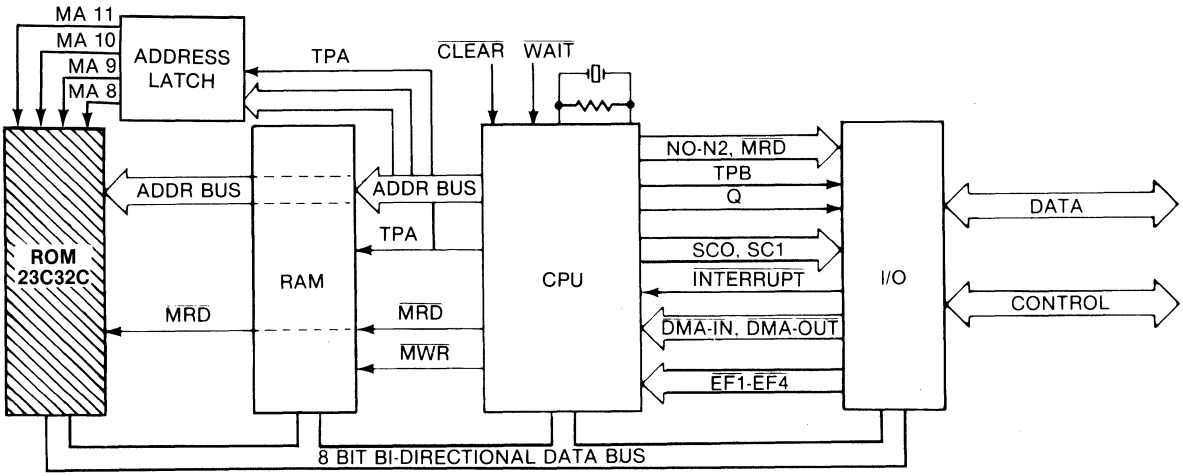
CHARACTERISTICS	CONDITIONS		LIMITS			UNITS
	V_O (V)	V_{DD} (V)	Min.	Typ.	Max.	
STATIC						
Quiescent Device Current, I_L	–	5	–	1	100	µA
Supply Current, I_{DD} (400KHz Addresses)	–	5	–	–	4	mA
Output Drive Current: N-Channel (Sink), I_{DN}	0.5	5	2.2	–	–	mA
P-Channel (Source), I_{DP}	4.5	5	2	–	–	mA
Output Voltage Low Level, V_{OL}	–	5	–	0	0.05	V
Output Voltage High Level, V_{OH}	–	5	4.95	5	–	V
Input Low Voltage V_{IL}	0.5, 4.5	5	–	–	1.25	V
Input High Voltage, V_{IH}	0.5, 4.5	5	3.75	–	–	V
Input Leakage Current, I_{IL}, I_{IH}	0	5	–	±1	±2	µA
3 State Ouput Leakage Current, I_{OUT}	0, 5	5	–	±1	±2	µA
DYNAMIC: t_r, t_f = 10 ns, C_L = 50pF; R_L = 200K Ω						
Access Time From Address Change, t_{AA}	–	5	–	750	1000	ns
Access Time From Chip Select, t_{AC}	–	5	–	330	425	ns



FUNCTIONAL OPERATION

This ROM is completely static (no clocks required). Decode of the input address selects a word from the storage array. The chip select signal enables the selected word to appear on the output bus line. Address rise and fall times should be less than 500nsec.

TYPICAL SYSTEM INTERCONNECT



SIGNAL DESCRIPTION

MA0 – MA11: These address lines select a byte location. MA 11 is the high order address bit.

BUS0 – BUS7: These eight three-state data lines form a common bus with the microprocessor.

CS1, CS2: These chip select signals are provided for memory expansion. Outputs are enabled when CS 1 and CS 2 are active. Polarity of CS 1 and CS 2 are user mask programmable.

ORDERING INFORMATION

Contact Hughes for price and other information relating to ROMs. ROM order forms and instructions concerning means of data conveyance are available from Hughes Solid State Products or Hughes' representatives.

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Telephone: 49-89-834, 7088 Telex: 5213856 HSPD

Printed in U.S.A.
Rev. A; 5/83
Supersedes Previous Data

8192 x 8 Static ROM — HCMP 23C64C

DESCRIPTION

Hughes' 23C64C is a CMOS Mask Programmable Read Only Memory organized 8192 x 8. The ROM circuit is static and updates its outputs when any address changes. One chip select is included which is programmed for polarity with the same mask that programs the data pattern.

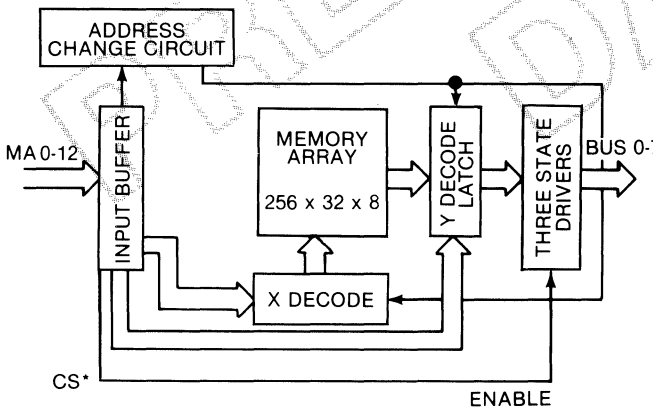
When the chip is selected (CS is activated) the address present on lines MA 0 – MA 12 accesses data which is presented to the output sense amplifiers. The 8-bit output word is enabled onto the data lines by the chip select signal which can be used for memory expansion.

The 23C64C operates over a 4-6.5 voltage range. The ROMs are available in a 24 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

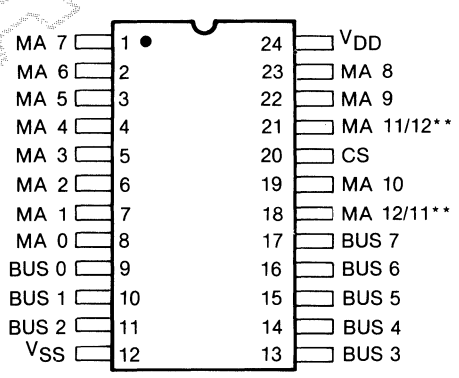
FEATURES

- Static CMOS Circuitry
- Access Time
  300ns Typical at V_{DD} = 5V
- Compatible with Most Microprocessors at Maximum Speed
- Single Voltage Supply
- Low Quiescent and Operating Power
  Standby — 5μA typical
  Operating — 3mA typical

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



*ACTIVE STATE IS MASK PROGRAMMABLE
**ADDRESS PLACEMENT IS USER SELECTABLE (MA 12 AND MA 11 ONLY).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature Range (T_{stg}) . . . . . −65 to +150°C
Operating Temperature Range (T_A)
Ceramic Package . . . . . −55 to +125°C
Plastic Package . . . . . −40 to +85°C
DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
23C64C . . . . . 0.5 to +7V

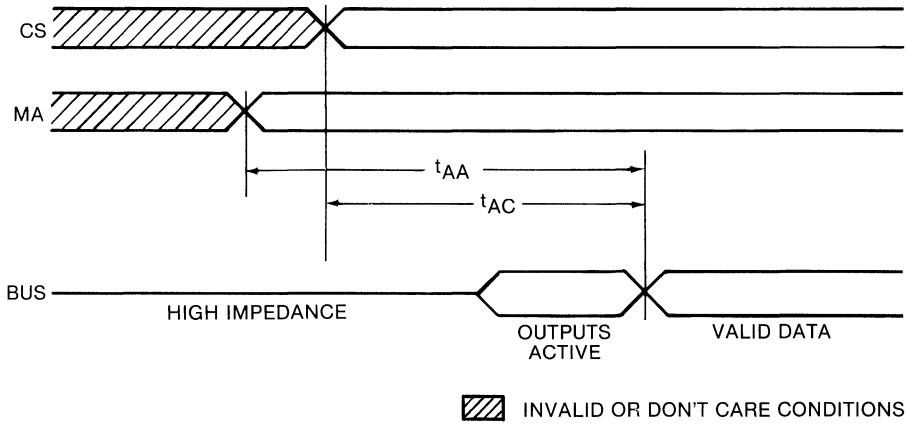
NOTE: Operating the device above the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full Package Range Unless Otherwise Specified

CHARACTERISTICS	CONDITIONS		LIMITS			UNITS
	V_O (V)	V_{DD} (V)	Min.	Typ.	Max.	
Supply Voltage Range (At T_A = Full Package Temperature Range)	–	–	4	–	6.5	V
Recommended Input Voltage Range	–	–	V_{SS}	–	V_{DD}	V

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = ±5% except as noted.

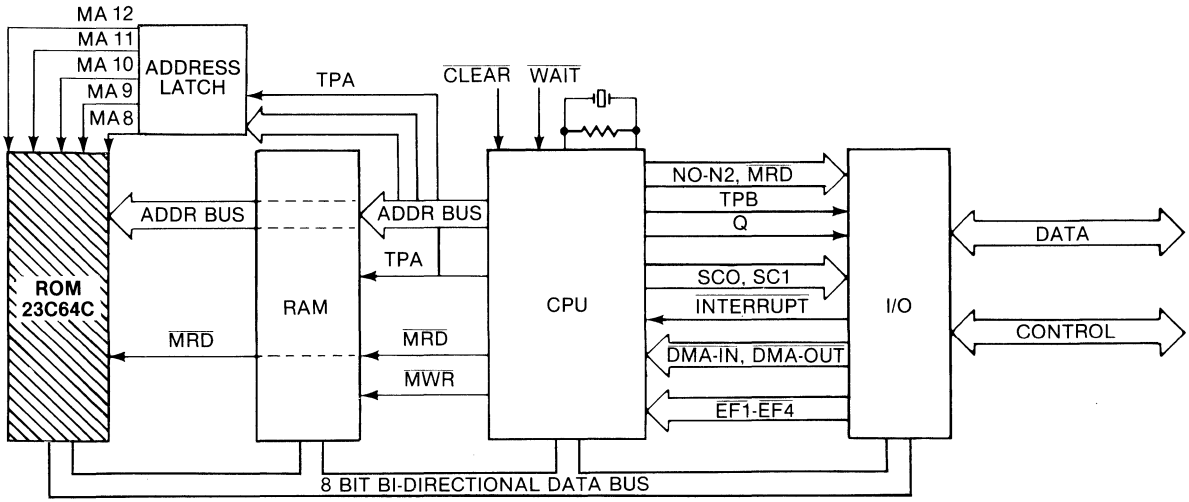
CHARACTERISTICS	CONDITIONS		LIMITS			UNITS
	V_O (V)	V_{DD} (V)	Min.	Typ.	Max.	
STATIC						
Quiescent Device Current, I_L (Chip not selected)	–	5	–	5	50	μA
Supply Current, I_{DD} (400KHz Addresses)	–	5	–	3	5	mA
Output Drive Current; N-Channel (Sink), I_{DN}	0.5	5	2.2	–	–	mA
P-Channel (Source), I_{DP}	4.5	5	2.2	–	–	mA
Output Voltage Low Level, V_{OL}	–	5	–	0	0.05	V
Output Voltage High Level, V_{OH}	–	5	4.95	5	–	V
Input Low Voltage V_{IL}	0.5,4.5	5	–	–	1.25	V
Input High Voltage V_{IH}	0.5,4.5	5	3.75	–	–	V
Input Leakage Current I_{IL}, I_{IH}	0	5	–	±1	±2	μA
3 State Output Leakage Current I_{OUT}	0,5	5	–	±1	±2	μA
DYNAMIC: t_r, t_f = 10 ns, C_L = 50pF; R_L = 200KΩ						
Access Time From Address Change t_{AA}	–	5	–	300	325	ns
Access Time From Chip Select t_{AC}	–	5	–	100	125	ns



FUNCTIONAL OPERATION

This ROM is completely static (no clocks required). Decode of the input address selects a word from the storage array. The chip select signal enables the selected word to appear on the output bus line. Address rise and fall times should be less than 500 nsec.

TYPICAL SYSTEM INTERCONNECT



SIGNAL DESCRIPTION

MA 0 – MA 12: These address lines select a byte location. MA12 is the high order address bit.

BUS 0 – BUS 7: These eight three-state data lines form a common bus with the microprocessor.

CS: This chip select signal is provided for memory expansion. Outputs are enabled when CS is active. Polarity of CS is user mask programmable.

ORDERING INFORMATION

Contact Hughes for prices and other information relating to ROMs. ROM order forms and instructions concerning means of data conveyance are available from Hughes Solid State Products or Hughes' Representatives.

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HUGHES AIRCRAFT COMPANY

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Schmaedel Str. 22, 8000 Munich, Germany
Telephone: 49-89-834, 7088 Telex: 5213856 HSPD

Printed in U.S.A.
Rev. N/C 3/84
Supersedes Previous Data

CMOS Static ROM 8192 x 8

8192 x 8 Static ROM — 23C65

DESCRIPTION

Hughes' 23C65 is a CMOS Mask Programmable Read Only Memory organized 8192 x 8. The ROM circuit is static and updates its outputs when any address changes. One Chip Enable (CE) and one Output Enable (OE) are included and are programmed for polarity with the same mask that programs the data pattern.

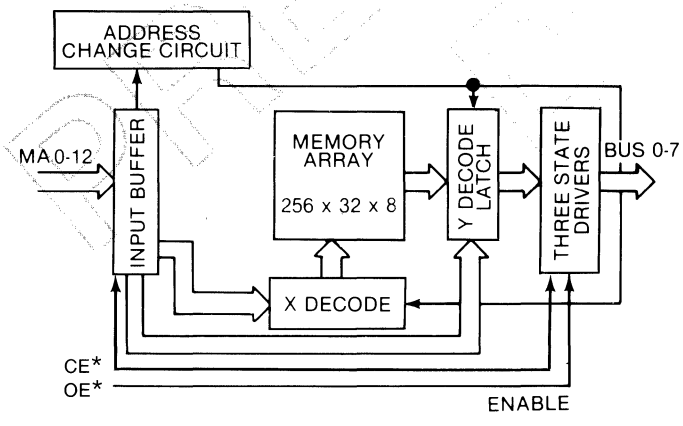
When the chip is selected (CE is activated) the address present on lines MA 0—MA 12 accesses data which is presented to the output sense amplifiers. The 8-bit output word is enabled onto the data lines by the Output Enable signal (OE) which can be used for bus control.

Hughes' 23C65 operates over a 4-6.5 voltage range. The ROMs are available in a 28 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

FEATURES

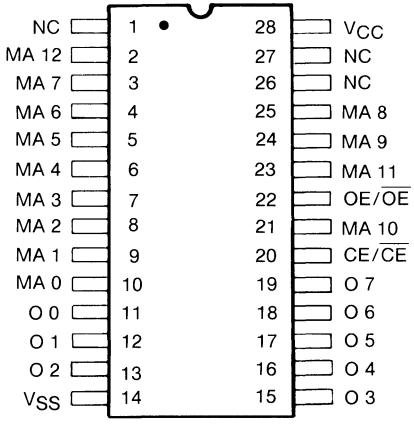
- Static CMOS Circuitry
- Access Time From Address Change 300 ns Typical at V_{DD} = 5V
- Compatible with Most Microprocessors at Maximum Speed
- Standard Jedec Pinouts
- Single Voltage Supply
- Low Quiescent and Operating Power
  Standby — 5 µA typical (CE Disabled)
  Operating — 3mA typical

FUNCTIONAL DIAGRAM



*ACTIVE STATE IS MASK PROGRAMMABLE

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T_A)
- Ceramic Package ..... −55 to + 125°C
- Plastic Package ..... −40 to + 85°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- 23C65C ..... 0.5 to + 7 Volts

Storage Temperature Range (T_{stg}) ..... −65 to + 150°C

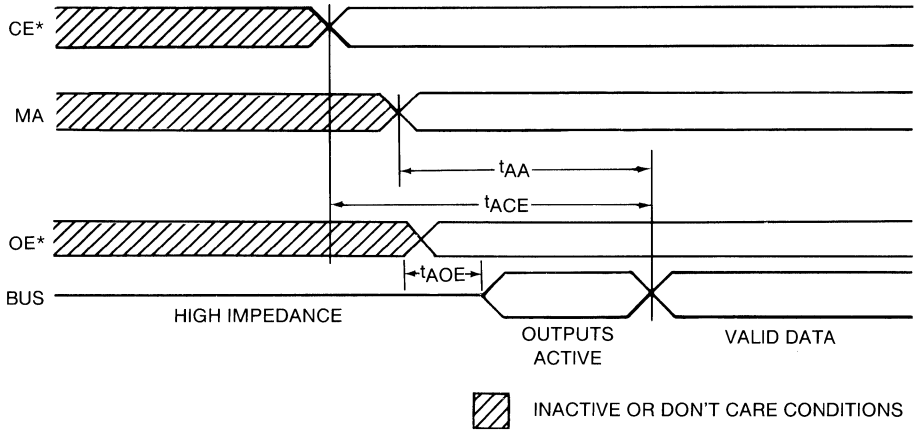
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full Package Range Unless Otherwise Specified

CHARACTERISTICS	CONDITIONS		LIMITS			UNITS
	V_O (V)	V_{DD} (V)	Min.	Typ.	Max.	
Supply Voltage Range (At T_A = Full Package Temperature Range)	—	—	4	—	6.5	V
Recommended Input Voltage Range	—	—	V_{SS}	—	V_{DD}	V

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = ± 5% except as noted.

CHARACTERISTICS	CONDITIONS		LIMITS			UNITS
	V_O (V)	V_{DD} (V)	Min.	Typ.	Max.	
STATIC						
Quiescent Device Current, I_L (Chip not selected)	—	5	—	5	50	µA
Supply Current, I_{DD} (400KHz Addresses)	—	5	—	3	5	mA
Output Drive Current; N-Channel (Sink), I_{DN}	0.5	5	2.2	—	—	mA
P-Channel (Source), I_{DP}	4.5	5	2.2	—	—	mA
Output Voltage Low Level, V_{OL}	—	5	—	0	0.05	V
Output Voltage High Level, V_{OH}	—	5	4.95	5	—	V
Input Low Voltage V_{IL}	0.5, 4.5	5	—	—	1.25	V
Input High Voltage V_{IH}	0.5, 4.5	5	3.75	—	—	V
Input Leakage Current I_{IL}, I_{IH}	0	5	—	± 1	± 2	µA
3 State Output Leakage Current I_{OUT}	0, 5	5	—	± 1	± 2	µA
DYNAMIC: t_r, t_f = 10 ns, C_L = 50pF; R_L = 200KΩ						
Access Time From Address Change t_{AA}	—	5	—	300	450	ns
Access Time From Chip Enable t_{ACE}	—	5	—	350	500	ns
Access Time From Output Enable t_{AOE}	—	5	—	100	125	ns

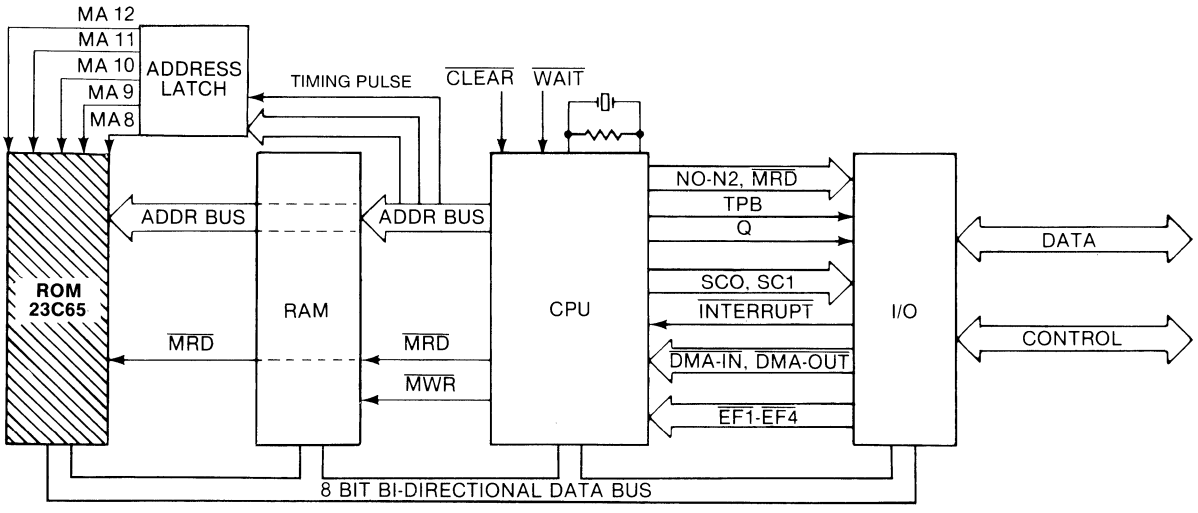


*Active state is mask programmable.

FUNCTIONAL OPERATION

This ROM is completely static (no clocks required). Decode of the input address selects a word from the storage array. The chip select signal enables the selected word to appear on the output bus line. Address rise and fall times should be less than 500 nsec.

TYPICAL SYSTEM INTERCONNECT



SIGNAL DESCRIPTION

MA 0—MA 12: These address lines select a byte location. MA 12 is the high order address bit.

BUS 0—BUS 7: These eight three-state data lines form a common bus with the microprocessor.

CE: This Chip Enable signal is provided for memory selection. All memory functions are enabled when CE is active. Polarity of CE is mask programmable.

OE: This Output Enable signal is provided for bus control. Outputs are enabled when the chip is selected and OE is active. Polarity of OE is mask programmable.

ORDERING INFORMATION:

Contact Hughes for prices and other information relating to ROMs. ROM order forms and instructions concerning means of data conveyance are available from Hughes Solid State Products or Hughes' Representatives.

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Schmaedel Str. 22, 8000 Munich, Germany
Telephone 49-89-834. 7088 Telex: 5213856 HSPD

Printed in U.S.A. 3/84
Supersedes Previous Data

1800 CMOS Microprocessor Family
Central Processing Unit

DESCRIPTION

Hughes' 1802A is an 8 bit register-oriented Central Processing Unit (CPU) designed for use as a general-purpose computing or control element in a wide range of stored program systems or products. The 1802A has a common bi-directional bus shared between all internal data, control, status and array registers. Accessing of memory is accomplished by time multiplexing a 16 bit address representing 65,536 locations into two sequentially transmitted bytes (8 bits). The presence of the most significant address bits is signified by the TPA clock. The 16x16 array of registers may be selected by the P,X, and N register designators to represent a program counter, data pointer and general pointer register respectively. Switching of programs may be readily accomplished by manipulating the register designators.

It has a flexible I/O interface including separate control signals (N0-N2) and memory access signals allowing direct memory data transfer with peripherals under CPU program control (through I/O instructions) or under peripheral control ($\overline{\text{DMA-IN}}$ and $\overline{\text{DMA-OUT}}$ signals). In addition to nonprogrammed Interrupt response, the CPU can monitor 4 flag inputs ($\overline{\text{EF1}}$-$\overline{\text{EF4}}$) from peripherals and set an output (Q) to the peripheral under program control. This may be used for serial data transfer or general control signals. State Codes (SC0-SC1) are available to monitor the CPU internal states.

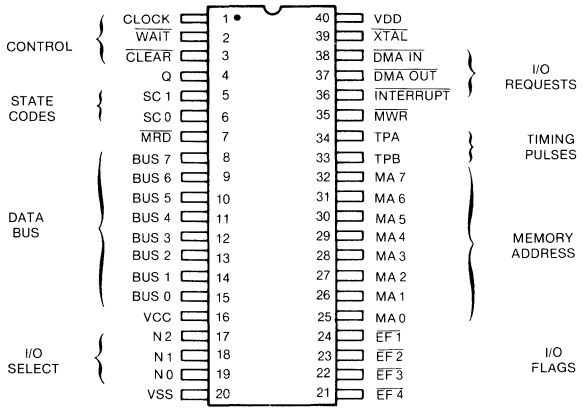
The 1802A operates over a 4-10.5 voltage range while the 1802AC has a recommended 4-6.5 volts. The CPUs are available in a 40 lead dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

Hughes' 1802BC (operating with 5 MHz Clock at 5V) is available for designs requiring higher system speed.

FEATURES

- Instruction Cycle Time 2.5-3.75 µs at 6.4 MHz
- 8 Bit Parallel Data Organization
- Memory Addressing to 65,536 Bytes
- On Chip Direct Memory Access
- 16x16 General Purpose Register Matrix
- Four Flag Inputs and One Programmable Output
- Direct Memory to Peripheral Transfer on I/O Instructions
- T^2L, NMOS and CMOS Compatible
- Optional On Chip Xtal Controlled Oscillator
- Low Power Single Voltage Supply
- 91 Instructions
- Schmitt Triggered $\overline{\text{Clear}}$

PIN CONFIGURATION



ARCHITECTURAL ORGANIZATION

N,X,P Registers – These three registers provide a 4 bit binary number which designates (selects) one of the registers in the register array to provide an address to memory. In addition, the N register holds device selection codes for input/output operations, and acts as a buffer for the lower 4 bits of the op-code.

Q-Flip Flop – This internal flip flop can be set or reset by instruction and can be sensed by conditional branch instructions. Q can also be used as a microprocessor output control.

Register Array – These 16 registers of 16 bit word size can be used to provide three separate functions: as program counters, as data pointers or as a scratch pad buffer. Each array register designated by N, X, or P provides a 16 bit memory address latched by the A register and multiplexed 8 bits at a time onto the memory address lines.

- **Program Counter** – Any register may be used as the main program counter or as a subroutine program counter. This is determined by the user by setting the P register (4 bits) to point to any of the 16 array registers. When interrupts are serviced R(1) is used as the interrupt service routine program counter.

- **Data Pointers** – Any array register may be selected by the N and X registers to provide the address of a data word location in memory. The N register selects an array register to provide addresses for several Load D from memory and Store D (accumulator) to memory instructions. The X register can also select array registers to provide addresses of memory data used in ALU operations and Input/Output operations, and additional Load from Memory and Store to Memory instructions with the D register.

- **Data Register** – The N register also selects an array register location to act as a scratch pad buffer for data exchange with the D register. Data is transferred by a set of four instructions which select the high order byte R(N).1, or the low order byte R(N).0. Additionally an array register may be incremented or decremented for usage as loop counters.

INTERFACE MODES –

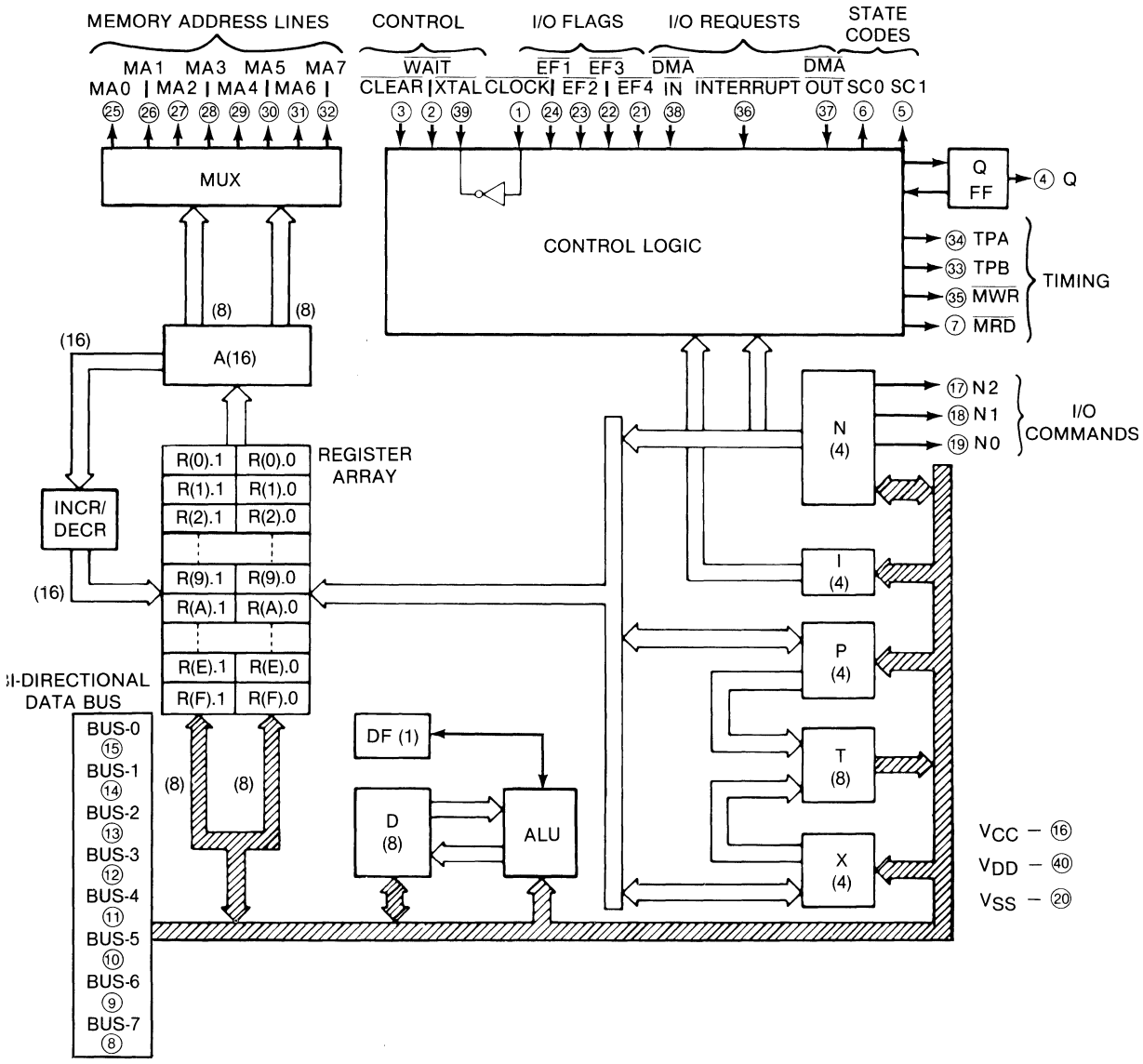
There are three modes of peripheral data transfer in the 1802A. These are programmed I/O, Interrupt Servicing, and Direct Memory Access.

- **Programmed I/O** – The 1802A provides a direct memory to peripheral device interface. The N0-N2 lines select a peripheral device while the memory address lines access a memory location. On Input instructions the peripheral data is read into the D register and memory simultaneously. On Output instructions the memory data is sent directly to the peripheral device. The $\overline{EF}$ flags and Q output can be used as additional programmable controls or as a serial data transfer path.

- **Interrupt Servicing** – Upon the completion of an instruction, a non-masked (enabled) interrupt request will be acknowledged by the 1802A. This results in the saving of the present X and P register values in the T register, resetting the Interrupt Enable flip flop, and setting of X to point to Register 2 and P to Register 1. At the end of an Interrupt routine, a Return instruction restores old values of X and P and allows reactivation of the Interrupt Enable flip flop.

- **Direct Memory Access** – The DMA mode is entered at the end of the execute machine cycle in the currently held instruction. This is a special extension of programmed input/output. When a DMA-In or DMA-Out request is activated, array register R(0) provides the location in memory for data transfer. On each byte transfer R(0) is incremented. The DMA mode can also be used to initially load memory after Reset and eliminates the requirement for specialized "bootstrap" load programs.

FUNCTIONAL DIAGRAM



1802A REGISTER SUMMARY

REG.	NO. OF BITS	DESCRIPTION
D	8	DATA REGISTER (ACCUMULATOR)
DF	1	DATA FLAG (ALU CARRY/BORROW)
R	16	1 OF 16 SCRATCHPAD REGISTER
P	4	DESIGNATES WHICH REGISTER IS PROGRAM COUNTER
X	4	DESIGNATES WHICH REGISTER IS DATA OR STACK POINTER
N	4	HOLDS LOW ORDER INSTRUCTION DIGIT/DESIGNATES DATA PTR
I	4	HOLDS HIGH ORDER (OP CODE) INSTRUCTION DIGIT
T	8	HOLDS OLD X, P VALUES AFTER INTERRUPT (X IS HIGH BYTE)
IE	1	INTERRUPT ENABLE FLIP FLOP
Q	1	OUTPUT FLIP FLOP

ABSOLUTE MAXIMUM RATINGS

DC SUPPLY-VOLTAGE RANGE (V_{CC}, V_{DD})
(All voltage values referenced to V_{SS} terminal)
$V_{CC} \leq V_{DD}$:
1802A ..... −0.5 to + 11V
1802AC/1802BC ..... −0.5 to + 7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} + 0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ± 10mA
OPERATING TEMPERATURE RANGE (T_A) CERAMIC PACKAGE .. −55 to + 125°C
PLASTIC PACKAGE ... −40 to + 85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... −65 to + 150°C

NOTE: Operating the device above the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STATIC ELECTRICAL CHARACTERISTICS AT T_A = −40 to +85°C, except as noted.

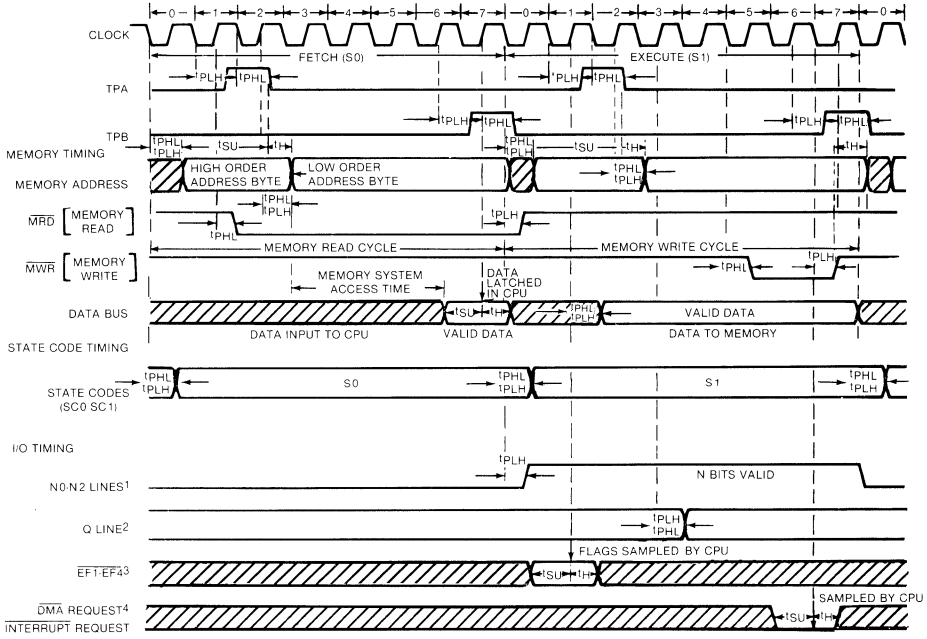
CHARACTERISTICS	CONDITIONS V_O (V)	V_{IN} (V)	V_{CC} V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) 1802A Min.	1802A Typ.*	1802A Max.	1802AC Min.	1802AC Typ.*	1802AC Max.	1802BC Min.	1802BC Typ.*	1802BC Max.	UNITS
Quiescent Device Current, I_L Max.	–	–	5	–	0.01	100	–	0.02	400	–	0.02	400	µA
	–	–	10	–	1	400	–	–	–	–	–	–	
Output Low Drive (Sink) Current, I_{OL} Min (Except $\overline{Xtal}$)	0.4	0,5	5	1.2	2.5	–	1.2	2.5	–	1.2	2.5	–	mA
	0.5	0,10	10	24	4.4	–	–	–	–	–	–	–	
$\overline{Xtal}$ Output I_{OL} Min.	0.4	5	5	200	360	–	200	360	–	200	360	–	µA
Output High Drive (Source Current) I_{OH} Min. (Except $\overline{Xtal}$)	4.6	0,5	5	-0.40	-0.80	–	-0.40	-0.80	–	-0.40	-0.80	–	mA
	9.5	0,10	10	-0.60	-1.2	–	–	–	–	–	–	–	
$\overline{Xtal}$ Output I_{OH} Min.	4.6	0	5	-100	-260	–	-100	-260	–	-100	-260	–	µA
Output Voltage Low Level V_{OL} Max.	–	0,5	5	–	0	0.1	–	0	0.1	–	0	0.1	V
	–	0,10	10	–	0	0.1	–	–	–	–	–	–	
Output Voltage High Level, V_{OH} Min.	–	0,5	5	4.9	5	–	4.9	5	–	4.9	5	–	
	–	0,10	10	9.9	10	–	–	–		–	–		
Input Low Voltage V_{IL} Max.	0.5, 4.5	–	5	–	–	1.5	–	–	1.5	–	–	1.5	V
	0.5, 4.5	–	5, 10	–	–	1	–	–	1	–	–	1	
	1.9	–	10	–	–	3	–	–	–	–	–	–	
Input High Voltage V_{IH} Min.	0.5, 4.5	–	5	3.5	–	–	3.5	–	–	3.5	–	–	
	0.5, 4.5	–	5, 10	4	–	–	4	–	–	4	–	–	
	1.9	–	10	7	–	–	–	–	–	–	–	–	
Clear Input Voltage V_H	–	–	5	0.4	0.5	–	0.4	0.5	–	0.4	0.5	–	V
	–	–	5, 10	0.3	0.4	–	–	–	–	–	–	–	
	–	–	10	1.5	2	–	–	–	–	–	–	–	
Input Leakage Current, I_{IN} Max.	Any Input	0,5	5	–	$\pm 10^{-4}$	±1	–	$\pm 10^{-4}$	±1	–	$\pm 10^{-4}$	±1	µA
		0,10	10	–	$\pm 10^{-4}$	±1	–	–	–	–	–	–	
3-State Output Leakage Current, I_{OUT} Max.	0.5	0,5	5	–	$\pm 10^{-4}$	±1	–	$\pm 10^{-4}$	±1	–	$\pm 10^{-4}$	±1	µA
	0,10	0, 10	10	–	$\pm 10^{-4}$	±1	–	–	–	–	–	–	
Minimum Data Retention Voltage, V_{DR}	$V_{DD} = V_{DR}$			–	2	2.4	–	2	2.4	–	2	2.4	V
Data Retention Current, I_{DR}	V_{DD} = 2.4V			–	0.1	1	–	0.5	5	–	0.5	5	µA
Effective Input Capacitance, C_{IN} Any Input	–			–	5	7.5	–	5	7.5	–	5	7.5	pF
Effective 3-State Terminal Capacitance Data Bus	–			–	10	15	–	10	15	–	10	15	pF

*Typical Values are for T_A = 25° C and Nominal V_{DD}

RECOMMENDED OPERATION CONDITIONS at T_A = −40° to +85°C Unless Otherwise Specified

CHARACTERISTICS	CONDITIONS		LIMITS			UNITS
	V_{CC}[1] (V)	V_{DD} (V)	H1802A	H1802AC	H1802BC	
Supply-Voltage Range	–	–	4 to 10.5	4 to 6.5	4 to 6.5	V
Input Voltage Range	–	–	V_{SS} to V_{DD}	V_{SS} to V_{DD}	V_{SS} to V_{DD}	V
Maximum Clock Input Rise or Fall Time, t_r or t_f	4-10.5	4-10.5	1	1	1	µs
Minimum Instruction Time[2] (See Fig. 6)	5	5	5	5	3.2	µs
	5	10	4	–	–	
	10	10	2.5	–	–	
Maximum DMA Transfer Rate	5	5	400	400	625	KBytes/sec
	5	10	500	–	–	
	10	10	800	–	–	
Maximum Clock Input Frequency, f_{CL}[3]	5	5	DC - 3.2	DC - 3.2	DC - 5.0	MHz
	5	10	DC - 4	–	–	
	10	10	DC - 6.4	–	–	

NOTES:
1. $V_{CC} \leqslant V_{DD}$; for 1802AC $V_{DD} = V_{CC} = 5$ volts.
2. Equals 2 machine cycles — one Fetch and one Execute operation for all instructions except Long Branch and Long Skip, which require 3 machine cycles — one Fetch and two Execute operations.
3. Load Capacitance (C_L) = 50 pF.



NOTES:
This timing diagram is used to show signal relationship only. All measurements are referenced to 50% point of the wave forms. Shaded areas indicate "Don't Care" on Inputs or Undefined State on Outputs. Sample or setting action at clock is designated by an arrow.

1. The N0-N2 bits are valid during the S1 cycle of Input or Output instructions only (61-67 and 69-6F)
2. The Q line is set or reset during the S1 cycle of the SEQ or REQ instructions
3. The flag inputs ($\overline{EF1}$-$\overline{EF4}$) are sampled during an S1 cycle
4. The DMA and Interrupt inputs are sampled during cycles S1, S2 or S3. The priority on concurrent signal inputs are (i) DMA-In (ii) DMA-Out and (iii) Interrupt.

Figure – 1 General Timing Diagram

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85°C$, $V_{DD} \pm 5\%$, except as noted.

CHARACTERISTICS	V_{CC} (V)	V_{DD} (V)	LIMITS Min.	LIMITS Typ.*	LIMITS Max.	UNITS
Propagation Delay Time, t_{PLH}, t_{PHL} Clock to TPA, TPB	5	5	–	200	350	ns
	5	10	–	150	250	
	10	10	–	100	150	
Clock-to-Memory High Address Byte	5	5	–	575	850	ns
	5	10	–	350	600	
	10	10	–	240	400	
Clock-to-Memory Low Address Byte	5	5	–	220	350	ns
	5	10	–	150	250	
	10	10	–	100	150	
Clock to $\overline{MRD}$, t_{PLH}, t_{PHL}	5	5	–	220	350	ns
	5	10	–	150	250	
	10	10	–	100	150	
Clock to $\overline{MWR}$, t_{PLH}, t_{PHL}	5	5	–	190	300	ns
	5	10	–	150	250	
	10	10	–	75	150	
Clock (CPU Data to Bus)	5	5	–	310	450	ns
	5	10	–	250	350	
	10	10	–	150	200	
Clock to State Code	5	5	–	290	450	ns
	5	10	–	250	350	
	10	10	–	130	250	
Clock to Q	5	5	–	250	400	ns
	5	10	–	150	250	
	10	10	–	115	175	
Clock to N (0-2), t_{PLH}, t_{PHL}	5	5	–	280	550	ns
	5	10	–	200	350	
	10	10	–	130	250	

TIMING SPECIFICATIONS as a function of T ($T = 1/f_{Clock}$) at $T_A = -40$ to $+85°C$

CHARACTERISTICS	V_{CC} (V)	V_{DD} (V)	LIMITS Min.	LIMITS Typ.*	UNITS
High Order Memory Address Byte Setup to TPA ↓ Time t_{SU}	5	5	2T-550	2T-300	ns
	5	10	2T-350	2T-200	
	10	10	2T-250	2T-130	
1802B	5	5	2T-350**	2T-50	
High Order Memory Address Byte Hold after TPA Time t_H	5	5	T/2-25	T/2-15	ns
	5	10	T/2-35	T/2-25	
	10	10	T/2-10	T/2+0	
Low Order Memory Address Byte Hold after WR Time t_H	5	5	T-30	T+0	ns
	5	10	T-20	T+0	
	10	10	T-10	T+0	
CPU Data to Bus Hold after WR Time t_H	5	5	T-200	T-150	ns
	5	10	T-150	T-100	
	10	10	T-100	T-50	
Required Memory Access Time Address to Data t_{ACC}	5	5	5T-350	5T-220	ns
	5	10	5T-250	5T-150	
	10	10	5T-150	5T-100	

*Typical values are for $T_A = 25°C$ and nominal V_{DD}

**Minimum value for 1802B t_{SU} is measured at $+25°C$.
2T-350 ns insures 50 ns set-up at F = 5 MHz.

DYNAMIC ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTICS	V_{CC} (V)	V_{DD} (V)	LIMITS Min.[1]	LIMITS Typ.[2]	LIMITS Max.	UNITS
Minimum Set Up and Hold Times, t_{SU}, t_H Data Input Set Up	5	5	0	−20	–	ns
	5	10	0	−15	–	
	10	10	0	−10	–	
Data Input Hold	5	5	200	150	–	ns
	5	10	125	100	–	
	10	10	100	75	–	
$\overline{DMA}$ Set Up	5	5	30	0	–	ns
	5	10	20	0	–	
	10	10	10	0	–	
$\overline{DMA}$ Hold	5	5	250	150	–	ns
	5	10	200	100	–	
	10	10	125	75	–	
Interrupt Set Up	5	5	0	−75	–	ns
	5	10	0	−50	–	
	10	10	0	−25	–	
Interrupt Hold	5	5	160	100	–	ns
	5	10	100	75	–	
	10	10	80	50	–	
$\overline{Wait}$ Set Up	5	5	0	−15	–	ns
	5	10	0	−25	–	
	10	10	0	− 5	–	
$\overline{EF1\text{-}4}$ Set Up	5	5	0	−50	–	ns
	5	10	0	−30	–	
	10	10	0	−20	–	
$\overline{EF1\text{-}4}$ Hold	5	5	200	100	–	ns
	5	10	150	75	–	
	10	10	100	50	–	
Minimum Pulse Width, $\overline{Clear}$ Pulse Width, t_{WL}	5	5	300	100	–	ns
	5	10	200	75	–	
	10	10	150	50	–	
$\overline{Clock}$ Pulse Width, t_{WL}	5	5	175	100	–	ns
	5	10	125	75	–	
	10	10	75	50	–	
Typical Total Power Dissipation Idle "00" at M (0000), C_L = 50 pF f=2.0 MHz	5	5	–	7.5	–	mW
f=4.0 MHz	10	10	–	70	–	

NOTE:
1. Typical values are for T_A = 25°C and nominal V_{DD}
2. Minimum characteristics are the values above which all devices function, i.e., data hold at 5 volts requires 200 msec. minimum to function over the temperature range but only 150 msec. at + 25°C.

INSTRUCTION SUMMARY

In all registers bits are numbered from least significant bit (LSB) to most significant bit (MSB) starting with 0.

R(W) Indicates an array register designated by the W register where W = N,X, or P. Example if X = 3, array reg. R(3) addresses memory data.

R(W).0 Low order byte contents of R(W)

R(W).1 High order byte contents of R(W)

NO Least significant bit of N register

M(R(W)) Contents of Memory addressed by selected array register
Operation Notation: M(R(N))→D; R(N)+1
This is interpreted as the memory byte addressed by the array register R(N) is loaded into the D reg., and the contents of R(N) are incremented by 1.

OP. CODE	MNEM-ONIC	NO. OF BYTES	MACH. CYCLES	INSTRUCTION	DESCRIPTION OF OPERATION
REGISTER OPERATIONS					
1N	INC	1	2	INCREMENT REGISTER N	R(N)+1. The register selected by the hex digit in N is incremented by 1.
2N	DEC	1	2	DECREMENT REGISTER N	R(N)−1. The register selected by the hex digit in N is decremented by 1.
60	IRX	1	2	INCREMENT REGISTER X	R(X)+1. The register selected by the hex digit in X is incremented by 1.
8N	GLO	1	2	GET LOW REGISTER N	R(N).0→D. The low order byte of the register selected by N replaces the byte in the D register.
AN	PLO	1	2	PUT LOW REGISTER N	D→R(N).0. The byte contained in the D register replaces the low order byte of the register selected by N. D is not changed.
9N	GHI	1	2	GET HIGH REGISTER N	R(N).1→D. The high order byte of the register selected by N replaces the byte in the D register.
BN	PHI	1	2	PUT HIGH REGISTER N	D→R(N).1. The byte contained in the D register replaces the high order byte of the register selected by N. D is unchanged.
MEMORY REFERENCE OPERATIONS					
ON	LDN	1	2	LOAD VIA N	M(R(N))→D; N≠0. The memory byte addressed by the contents of the reg. selected by N, R(N), replaces the byte in the D reg. Memory is unchanged.
4N	LDA	1	2	LOAD VIA N AND ADVANCE	M(R(N))→D; R(N)+1. The memory byte addressed by R(N) replaces the byte in the D reg. The memory address, R(N), is incremented. Memory is unchanged.
FO	LDX	1	2	LOAD VIA X	M(R(X))→D. The memory byte addressed by the contents of the reg. selected by X, R(X), replaces the byte in the D reg. Memory is unchanged.
72	LDXA	1	2	LOAD VIA X AND ADVANCE	M(R(X))→D; R(X)+1. The memory byte addressed by R(X) replaces the byte in the D reg. The memory address, R(X), is incremented. Memory is unchanged.
F8 ⟨B2⟩	LDI	2	2	LOAD IMMEDIATE	M(R(P))→D; R(P)+1. The memory byte following the F8 instruction replaces the byte in the D reg. The program counter R(P) is incremented to point to the next instruction.
5N	STR	1	2	STORE VIA N	D→M (R(N)). The byte in the D reg. replaces the memory byte addressed by the contents of the reg. selected by X, R(X). D is unchanged.
73	STXD	1	2	STORE VIA X AND DECREMENT	D→M(R(X)); R(X)−1. The byte in the D reg. replaces the memory byte addressed by R(X). The memory address, R(X), is decremented. D is unchanged.
LOGIC OPERATIONS					
F1	OR	1	2	OR MEMORY WITH D	M(R(X)) OR D→D. The 8 bit contents of the D reg. are logically ORed with the contents of the memory byte addressed by R(X).
F9 ⟨B2⟩	ORI	2	2	OR IMMEDIATE WITH D	M(R(P)) OR D→D; R(P)+1. The 8 bit contents of the D reg. are logically ORed with the memory byte following the F9 instruction. R(P) is incremented to point to the next instruction.
F3	XOR	1	2	EXCLUSIVE OR	M(R(X)) XOR D→D. The 8 bit contents of the D reg. are logically XORed with the memory byte addressed by R(X).
FB ⟨B2⟩	XRI	2	2	EXCLUSIVE OR IMMEDIATE	M(R(P)) XOR D→D; R(P)+1. The 8 bit contents of the D reg. are logically XORed with the memory byte following the F8 instruction. R(P) is incremented to point to the next instruction.
F2	AND	1	2	AND MEMORY WITH D	M(R(X)) AND D→D. The 8 bit contents of the D reg. are logically ANDed with the memory byte addressed by R(X).
FA ⟨B2⟩	ANI	2	2	AND IMMEDIATE WITH D	M(R(P)) AND D→D; R(P)+1. The 8 bit contents of the D reg. are logically ANDed with the memory byte following the FA instruction. R(P) is incremented to point to the next instruction.

⟨B2⟩ = 2nd byte of instruction.

The DF flip flop can only be altered by arithmetic and shift operations.
After an add instruction, DF=1 denotes a carry has occurred.
After a subtraction instruction, DF=0 denotes a borrow. D is in Two's compliment form.

The syntax – "(NOT DF)" denotes the subtraction of the borrow.

INSTRUCTION SUMMARY (Continued)

OP. CODE	MNEM–ONIC	NO. OF BYTES	MACH. CYCLES	INSTRUCTION	DESCRIPTION OF OPERATION
F6	SHR	1	2	SHIFT D RIGHT	SHIFT D RIGHT; LSB(D)→DF, 0→MSB(D). The 8 bits in D reg. are shifted one bit position to the right. The original LSB of D reg. is placed in DF. A "0" is placed in the MSB of D.
76	SHRC RSHR	1	2	SHIFT D RIGHT WITH CARRY RING SHIFT RIGHT	SHIFT D RIGHT; LSB(D)→DF, DF→MSB(D). The 8 bits in D are shifted one bit position to the right. The original LSB of D is placed in DF. The original content of DF is placed in MSB of D.
FE	SHL	1	2	SHIFT D LEFT	SHIFT D LEFT; MSB(D)→DF, 0→LSB(D). The 8 bits in D are shifted one bit position to the left. The original MSB of D is placed in DF, A "0" is placed in the LSB of D.
7E	SHLC RSHL	1	2	SHIFT D LEFT WITH CARRY RING SHIFT LEFT	SHIFT D LEFT; MSB(D)→DF, DF→LSB(D). The 8 bits in D are shifted one bit position to the left. The original MSB of D is placed in DF. The original content of DF is placed in LSB of D.
ARITHMETIC OPERATION					
F4	ADD	1	2	ADD MEMORY WITH D	M(R(X))+D→DF,D. The memory byte addressed by R(X) is added to the contents of the D reg. DF receives any carry generated from the addition.
FC ⟨B2⟩	ADI	2	2	ADD IMMEDIATE WITH D	M(R(P))+D→DF,D. R(P)+1. The memory byte following the FC instruction is added to the D reg. DF receives any carry. R(P) is incremented to point to the next instruction.
74	ADC	1	2	ADD MEM. WITH CARRY	M(R(X))+D+DF→DF,D. The memory byte addressed by R(X) plus the content of DF are added to the D reg. DF receives any carry generated from the addition.
7C ⟨B2⟩	ADCI	2	2	ADD IMMED. WITH CARRY	M(R(P))+D+DF→DF,D; R(P)+1. The memory byte following the 7C instruction plus DF are added to the D reg. DF receives any carry. (R(P) points to the next instruction.
F7	SM	1	2	SUBTRACT MEM FROM D (2's Compliment)	D–M (R(X))→DF,D. The memory byte addressed by R(X) is subtracted from the D reg. Any resulting carry is stored in DF (DF=0 indicates a borrow).
FF ⟨B2⟩	SMI	2	2	SUBTRACT MEM. IMMED. FROM D (2's Compliment)	D–M (R(P))→DF,D; R(P)+1. The memory byte following the FF instruction is subtracted from the D reg. Any carry is stored in DF. R(P) points to the next instruction.
77	SMB	1	2	SUBTRACT MEMORY WITH BORROW (1's Compliment +DF)	D–M (R(X))–(NOT DF)→DF,D. The memory byte addressed by R(X) plus the borrow indicator, $\overline{DF}$, is subtracted from the D reg. Any resulting carry is stored in DF.
7F ⟨B2⟩	SMBI	2	2	SUB. MEM. IMMED. WITH BORROW (1's Compliment +DF)	D–M(R(P))–NOT DF)→DF,D; R(P)+1. The memory byte following the 7F instruction plus $\overline{DF}$ is subtracted from the D reg. Any carry is stored in DF. R(P) points to next instruction.
F5	SD	1	2	SUBTRACT D FROM MEMORY (2's Compliment)	M(R(X))–D→DF,D. The 8 bit contents of the D reg. are subtracted from the memory byte addressed by R(X). DF receives any carry. Memory is unchanged.
FD ⟨B2⟩	SDI	2	2	SUB D FROM IMMEDIATE (2's Compliment)	M(R(P))–D→DF,D; R(P)+1. The contents of the D reg. are subtracted from the memory byte following the FD instruction. DF receives any carry. R(P) points to the next instruction.
75	SDB	1	2	SUB D WITH BORROW (1's Compliment +DF)	M(R(X))–D–(NOT DF)→DF,D. The contents of the D reg. plus $\overline{DF}$ are subtracted from the memory byte addressed by R(X). DF receives any carry. Memory is unchanged.
7D ⟨B2⟩	SDBI	2	2	SUB D WITH BORROW, IMMED. (1's Compliment +DF)	M(R(P))–D–(NOT DF)→DF,D; R(P)+1. The D reg. plus $\overline{DF}$ are subtracted from the memory byte following the 7D instruction. DF receives any carry (R(P) points to the next instruction.
BRANCH OPERATIONS					
30 ⟨B2⟩	BR	2	2	UNCONDITIONAL BRANCH	M(R(P))→R(P)-0. The byte following the 30 instruction always replaces the low order byte of the program counter R(P).
38	NBR	1	2	NO SHORT BRANCH	R(P)+1. The byte following the 38 instruction is always skipped. This instruction may also be considered a SHORT SKIP.
32 ⟨B2⟩	BZ	2	2	SHORT BRANCH IF D=0	IF D=0, M(R(P))→R(P)-0; ELSE R(P)+1. If each bit of the D reg. is "0" the byte following the 32 instruction replaces the low order byte of the program counter R(P). If D≠0, R(P) is incremented to point to the following instr.
3A ⟨B2⟩	BNZ	2	2	SHORT BRANCH IF D≠0	IF D≠0, M(R(P)) – R(P)-0; ELSE R(P) + 1. If any bit of the D reg. is "1" the immediate byte replaces the low order byte of R(P). If D=0, R(P) points to the following instruction. All short branches below are similar in operation.
33 ⟨B2⟩	BDF	2	2	SHORT BRANCH IF DF=1	IF DF=1, M(R(P))→R(P)-0; ELSE R(P)+1. This instruction may also be called a short branch if pos or zero (BPZ) or short branch if greater or equal (BGE).
3B ⟨B2⟩	BNF	2	2	SHORT BRANCH IF DF=0	IF DF=0, M(R(P))→R(P)-0; ELSE R(P)+1. This instruction may also be called a short branch if minus (BM) or short branch if less (BL).
31 ⟨B2⟩	BQ	2	2	SHORT BRANCH IF Q=1	IF Q=1, M(R(P))→R(P)-0; ELSE R(P)+1.
39 ⟨B2⟩	BNQ	2	2	SHORT BRANCH IF Q=0	IF Q=0, M(R(P))→R(P)-0; ELSE R(P)+1.
34 ⟨B2⟩	B1	2	2	SHORT BRANCH IF EF1=1	IF EF1=1, M(R(P))→R(P)-0; ELSE R(P)+1.
3C ⟨B2⟩	BNI	2	2	SHORT BRANCH IF EF1=0	IF EF1=0, M(R(P))→R(P)-0; ELSE R(P)+1.
35 ⟨B2⟩	B2	2	2	SHORT BRANCH IF EF2=1	IF EF2=1, M(R(P))→R(P)-0; ELSE R(P)+1.

Instruction is associated with more than one mnemonics.
⟨B2⟩ = 2nd byte of instruction.

All instructions require two machine cycles except Long Branches and Long Skips which take three machine cycles. Each machine cycle = 8 external clocks, i.e. @ 6.4 MHz, cycle = 1.25μs.

EF = 1, if $\overline{EF}$ input = 0 (GND).

INSTRUCTION SUMMARY (Continued)

OP. CODE	MNEMONIC	NO. OF BYTES	MACH. CYCLES	INSTRUCTION	DESCRIPTION OF OPERATION
3D ⟨B2⟩[1]	BN2	2	2	SHORT BRANCH IF EF2 = 0	IF EF2 = 0, M(R(P)) → R(P)-0; Else R(P) + 1.
36 ⟨B2⟩[1]	B3,	2	2	SHORT BRANCH IF EF3 = 1	IF EF3 = 1, M(R(P)) → R(P)-0; Else R(P) + 1.
3E ⟨B2⟩[1]	BN3,	2	2	SHORT BRANCH IF EF3 = 0	IF EF3 = 0, M(R(P)) → R(P)-0; ELSE R(P) + 1.
37 ⟨B2⟩[1]	B4,	2	2	SHORT BRANCH IF EF4 = 1	IF EF4 = 1, M(R(P)) → R(P)-0; Else R(P) + 1.
3F ⟨B2⟩[1]	BN4,	2	2	SHORT BRANCH IF EF4 = 0	IF EF4 = 0, M(R(P)) → R(P)-0; Else R(P) + 1.
CO ⟨B2⟩[1]	LBR ⟨B3⟩	3	3	UNCONDITIONAL LONG BRANCH	M(R(P)) → R(P)-1, M(R(P + 1)) → R(P)-0. The two bytes following the CO instruction always replace the high and low order bytes of the program counter R(P)
C8[2]	NLBR	1	3	NO LONG BRANCH	R(P) + 2. The next two bytes after the C8 instruction are always skipped. This instruction may also be considered a Long Skip.
C2 ⟨B2⟩[1]	LBZ ⟨B3⟩	3	3	LONG BRANCH IF D = 0	IF D = 0, M(R(P)) → R(P)-1, M(R(P + 1)) → R(P)-0; Else R(P) + 2. If all bits of the D reg. are "0", the two bytes following the C2 instruction replace the contents of the program counter, R(P). If not R(P) points to the next instruction. All long branches below are similar in operation.
CA ⟨B2⟩[1]	LBNZ ⟨B3⟩	3	3	LONG BRANCH IF D ≠ 0	If D not 0, M(R(P)) → R(P)-1, M(R(P + 1)) → R(P)-0. Else R(P) + 2.
C3 ⟨B2⟩[1]	LBDF ⟨B3⟩	3	3	LONG BRANCH IF DF = 1	IF DF = 1, M(R(P)) → R(P)-1, M(R(P + 1)) → R(P)-0; Else R(P) + 2.
CB ⟨B2⟩[1]	LBNF ⟨B3⟩	3	3	LONG BRANCH IF DF = 0	IF DF = 0, M(R(P)) → R(P)-1, M(R(P + 1)) → R(P)-0; Else R(P) + 2.
C1 ⟨B2⟩[1]	LBQ ⟨B3⟩	3	3	LONG BRANCH IF Q = 1	IF Q = 1, M(R(P)) → R(P)-1, M(R(P + 1)) → R(P)-0; Else R(P) + 2.
C9 ⟨B2⟩[1]	LBNQ ⟨B3⟩	3	3	LONG BRANCH IF Q = 0	I Q = 0, M(R(P)) → R(P)-1, M(R(P + 1)) → R(P)-0; Else R(P) + 2.
38[2]	SKP	1	2	SHORT SKIP	R(P) + 1. Always skips the following byte. Also called No Short Branch (NBR).
C8[2]	LSKP	1	3	LONG SKIP	R(P) + 2. Always skips the following two bytes. Also called No Long Branch (NLBR).
CE	LSZ	1	3	LONG SKIP IF D = 0	IF D = 0, R(P) + 2; Else Continue. If all bits of D are "0", the next two bytes following the CE instruction are skipped. If not, they are accessed as the next instruction.
C6	LSNZ	1	3	LONG SKIP IF D ≠ 0	IF D NOT 0, R(P) + 2; Else Continue.
CF	LSDF	1	3	LONG SKIP IF DF = 1	IF DF = 1, R(P) + 2; Else Continue.
C7	LSNF	1	3	LONG SKIP IF DF = 0	IF DF = 0, R(P) + 2; Else Continue.
CD	LSQ	1	3	LONG SKIP IF Q = 1	IF Q = 1, R(P) + 2; Else Continue.
C5	LSNQ	1	3	LONG SKIP IF Q = 0	IF Q = 0, R(P) + 2; Else Continue.
CC	LSIE	1	3	LONG SKIP IF IE = 1	IF IE = 1, R(P) + 2; Else Continue. 1E is interrupt enable.
CONTROL OPERATIONS					
00	IDL	1	2	IDLE (WAIT)	M(R(0)) → Bus. The processor repeats execute (S1) cycles until an I/O request ($\overline{INTERRUPT}$, DMA-IN, or DMA-OUT) is asserted.
C4	NOP	1	3	NO OPERATION	The processor performs no change of status during this instruction.
DN	SEP	1	2	SET P	N → P. The low order hex digit of the instruction is placed in the P register and designates which register is to serve as program counter, R(P).
EN	SEX	1	2	SET X	N → X. The low order hex digit of the instruction is placed in the X register.
7B	SEQ	1	2	SET Q	1 → Q. Sets the Q flip flop to logic high.
7A	REQ	1	2	RESET Q	0 → Q. Resets the Q flip flop to a logic low.
78	SAV	1	2	SAVE	T → M(R(X)). The T reg. containing previous X and P information is stored in the memory location addressed by R(X).
79	MARK	1	2	PUSH X, P TO STACK	(X,P) → T; (X,P) → M(R(2)), Then P → X; R(2) − 1. The current contents of X and P are stored in temporary reg. T and memory addressed by R(2). New P is set equal to X and R(2) is decremented.
70	RET	1	2	RETURN	M(R(X)) → (X,P), R(X) + 1; 1 → IE. The memory byte addressed by R(X) replaces X and P contents. The memory address, R(X), is incremented and IE is enabled. M(R(X)) → (X,P), R(X) + 1; 0 → IE. Same operation as RET except IE is disabled. Both RET and DIS are used primarily in returns from interrupt processing.
71	DIS	1	2	DISABLE	
INPUT/OUTPUT OPERATIONS					
6N	OUT	1	2	OUTPUT	M(R(X)) → Bus; R(X) + 1. N = 1 − 7. When N is 1 through 7, the memory byte addressed by R(X) is accessed and placed on the memory bus. The three low order bits of N are also placed on the N2 − N0 signal lines memory address. R(X) is incremented.
6N	INP	1	2	INPUT	Bus → M(R(X)); Bus → D. N = 9 − F. When N is 9 through F a byte is input to the D reg. and the memory location addressed by R(X). The low order 3 bits of N are placed on the N2 − N0 signal line. R(X) is not modified.

NOTE:
1. Instruction associated with more than one mnemonic.
2. ⟨B2⟩ = 2nd byte of instruction. ⟨B3⟩ = 3rd byte of instruction.

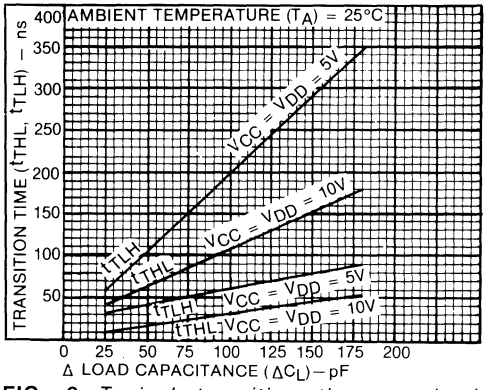


FIG. 2 *Typical transition time vs. load capacitance.*

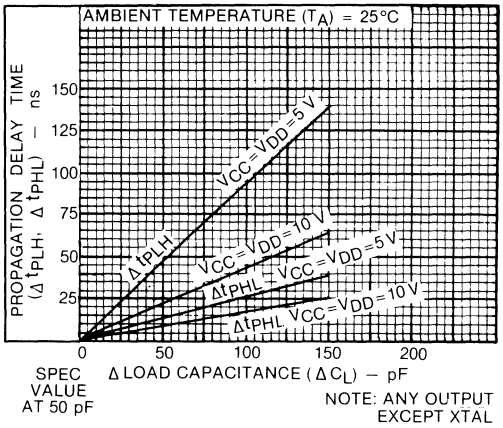


FIG. 3 *Typical change in propagation delay as a function of a change in load capacitance.*

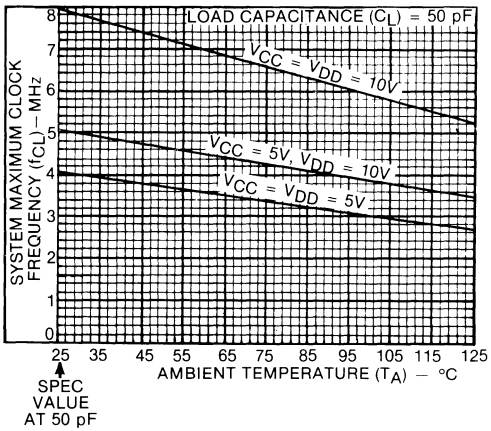
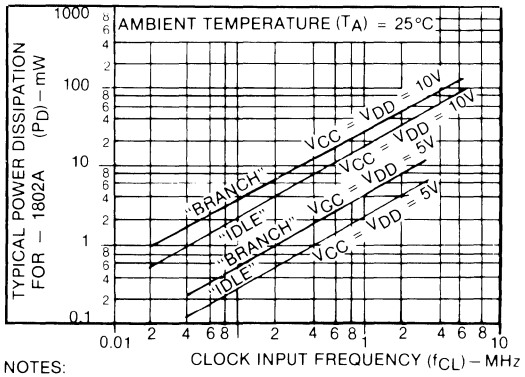


FIG. 4 *Typical maximum clock frequency as a function of temperature.*



NOTES:
IDLE = "00" AT M(0000)
BRANCH = "3707" AT M (8107)
C_L = 50 pF

FIG. 5 *Typical power dissipation as a function of clock frequency for Branch instruction and Idle instruction for 1802A.*

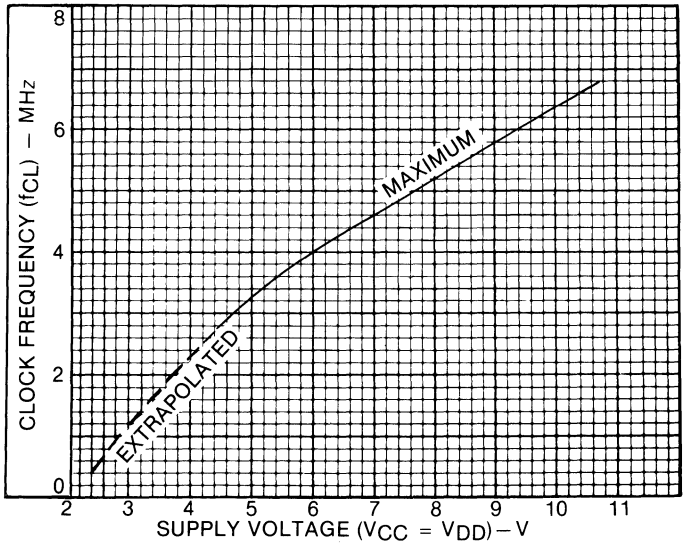


FIG. 6 *Clock frequency is a function of supply voltage.*

TABLE 1 –
CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES

STATE	I	N	MNEMONIC	INSTRUCTION	OPERATION	DATA BUS	MEMORY ADDRESS	MRD	NOTES
S1	RESET				JAM: I,N,Q,X,P=0 IE=1	0	R(0) UNDEFINED	1	A
	FIRST CYCLE AFTER RESET NOT PROGRAMMER ACCESSIBLE				INITIALIZE	0	R(0) UNDEFINED	1	B
S0		FETCH			M(R(P))→I,N R(P)+1	M(R(P))	R(P)	0	C
S1 (Execute)	0	0	IDL	IDLE	[Load=0 (Program Idle)]	M(R(0))	R(0)	0	D
					[Load=1 (Load Mode)]	M(R(0))	PREVIOUS ADDRESS	0	E
		N = 0	LDN	LOAD [D VIA N]	M(R(N))→D	M(R(N))	R(N)	0	
	1	N	INC	INCREMENT	R(N)+1	FLOAT	R(N)	1	
	2	N	DEC	DECREMENT	R(N)−1	FLOAT	R(N)	1	
	3	N	–	SHORT BRANCH	(BRANCH NOT TAKEN)	M(R(P))	R(P)	0	
					(BRANCH TAKEN)	M(R(P))	R(P)	0	
	4	N	LDA	LOAD ADVANCE	M(R(N))→D R(N)+1	M(R(N))	R(N)	0	
	5	N	STR	STORE VIA N	D→M(R(N))	D	R(N)	1	
	6	0	IRX	INC REG X	R(X)+1	M(R(X))	R(X)	0	
		N=1–7	OUT N	OUTPUT	M(R(X))→BUS R(X)+1	M(R(X))	R(X)	0	
		N=9–F	INP N	INPUT	BUS→M(R(X)), D	I/O DEVICE	R(X)	1	
	7	0	RET	RETURN	M((R)(X))→(X,P) R(X)+1; 1→IE	M(R(X))	R(X)	0	
		1	DIS	DISABLE	M(R(X))→(X,P) R(X)+1;0→IE	M(R(X))	R(X)	0	
		2	LDXA	LOAD VIA X AND ADVANCE	M(R(X))→D P(X)−1	M(R(X))	R(X)	0	
		3	STXD	STORE VIA X AND DECREMENT	D− M(R(X)) R(X)−1	D	R(X)	1	
		4,5,7	–		ALU OPERATION	M(R(X))	R(X)	0	
		6	–		ALU OPERATION	FLOAT	R(X)	1	
		8	SAV	SAVE	T→M(R(X))	T	R(X)	1	
		9	MARK	MARK	(X,P)→T,M(R(2)) P→X;R(2)−1	T	R(2)	1	
		A	REQ	RESET Q	Q=0	FLOAT	(R(P)	1	
		B	SEQ	SET Q	Q=1	FLOAT	R(P)	1	
		C,D,F			ALU OPERATION IMMEDIATE	M(R(P))	R(P)	0	
		E			ALU OPERATION	FLOAT	R(X)	1	
	8	N	GLO	GET LOW	R(N) .0→D	R(N) .0	R(N)	1	
	9	N	GHI	GET HIGH	R(N) .1→D	R(N) .1	R(N)	1	
	A	N	PLO	PUT LOW	D→R(N) .0	D	R(N)	1	
	B	N	PHI	PUT HIGH	D→R(N) .1	D	R(N)	1	
	C	0,1,2 3,8,9 A,B		LONG BRANCH	(BRANCH NOT TAKEN)	M(R(P))	R(P)	0	
					(BRANCH TAKEN)	M(R(P))	R(P)	0	
		5,6,7 C,D,E F		LONG SKIP	(SKIP NOT TAKEN)	M(R(P))	R(P)	0	
					(SKIP TAKEN)	M(R(P))	R(P)	0	
		4	NOP	NO OPERATION	NO OPERATION	M(R(P))	R(P)	0	
	D	N	SEP	SET P	N→P	N N	R(N)	1	
	E	N	SEX	SET X	N→X	N N	R(N)	1	
	F	0	LDX	LOAD VIA X	M(R(X))→D	M(R(X))	R(X)	0	
		1,2,3 4,5,7			ALU OPERATION	M(R(X))	R(X)	0	
		6	SHR	SHIFT RIGHT	SHIFT D RIGHT LSB(D)→DF 0→MSB(D)	FLOAT	R(X)	1	
		8	LDI	LOAD IMMEDIATE	M(R(P))→D R(P)+1	M(R(P))	R(P)	0	
		9,A,B, C,D,F,			ALU OPERATION IMMEDIATE	M(R(P))	R(P)	0	
		E	SHL	SHIFT LEFT	ALU OPERATION	FLOAT	R(P)	1	
S2	IN REQUEST			DMA IN	BUS→M(R(0)) R(0)+1	I/O DEVICE	R(0)	1	F
	OUT REQUEST			DMA OUT	M(R(0))− BUS R(0)+1	M(R(0))	R(0)	0	F
S3	INTERRUPT				X,P→T,0→IE 2→X, 1→P	FLOAT	R(N)	1	

NOTES:

A. IE=1; TPA, TPB suppressed, state=S1
B. BUS=0 for entire cycle
C. Next state always S1
D. Wait for DMA or Interrupt
E. Suppress TPA, wait for DMA
F. In Request has priority over Out Request

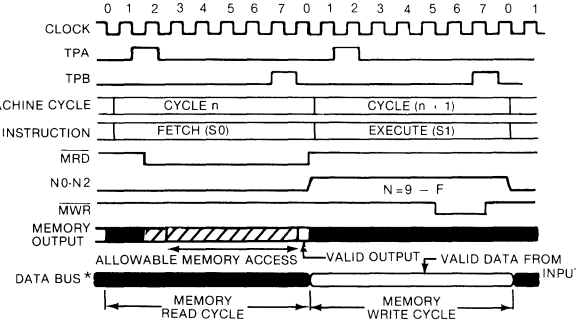


FIG. 7 *Memory — In cycle*

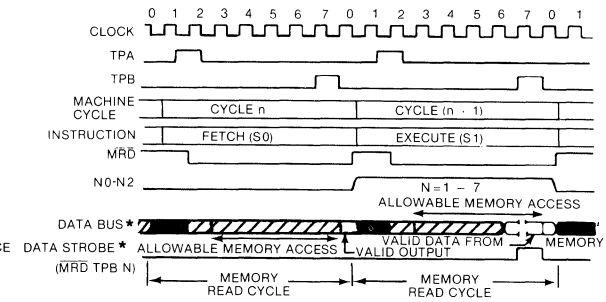


FIG. 8 *Memory — Out cycle*

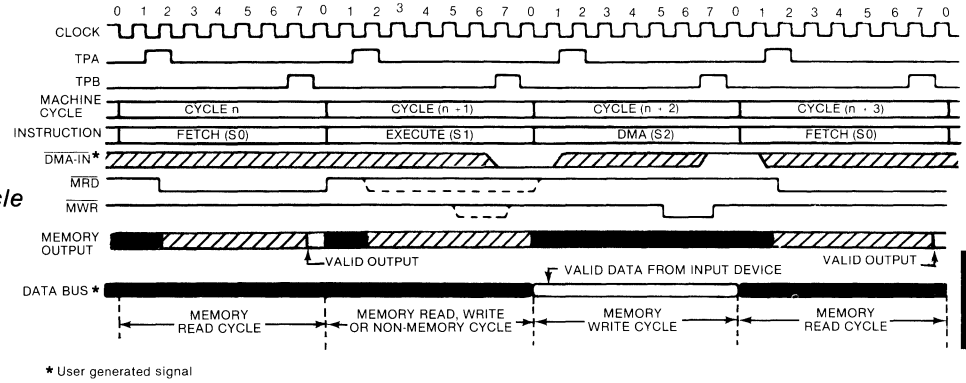


FIG. 9 *DMA — In cycle*

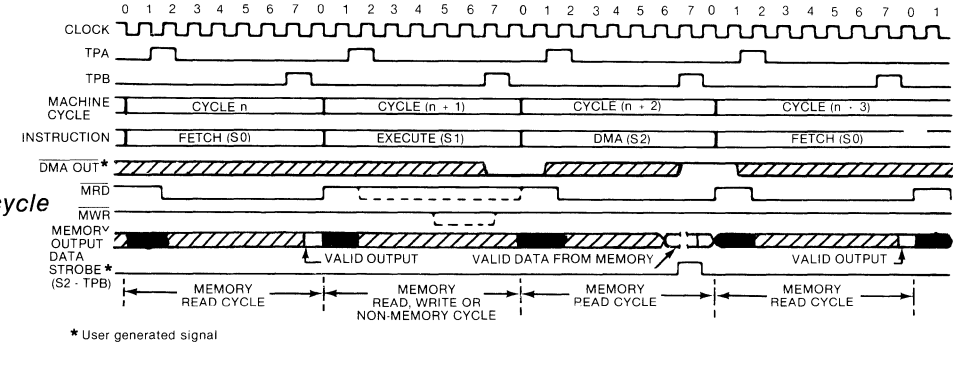


FIG. 10 *DMA — Out cycle*

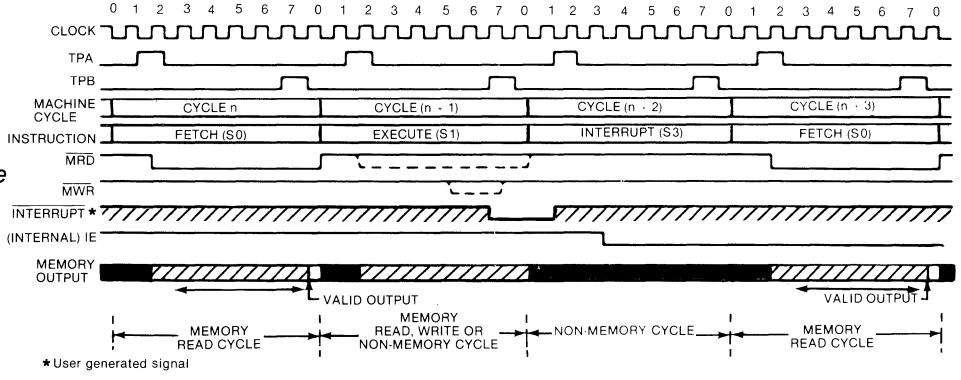
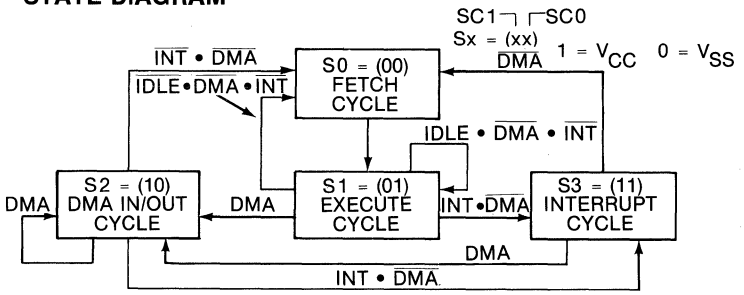


FIG. 11 *Interrupt cycle*

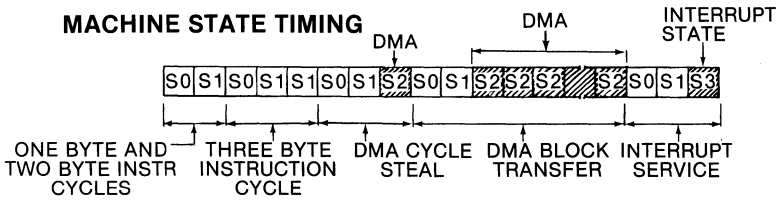
STATE DIAGRAM



The 1802A state transitions when in the run mode are shown to the left. Each machine cycle requires 8 clock pulses except the initialization cycle, after reset, which requires nine clock pulses.

The execution of an instruction requires either two or three machine cycles, an S0 cycle followed by a single S1 cycle, or two S1 cycles. S2 is the response to a DMA request and S3 is the interrupt response. Table 1 shows the conditions on the Data Bus and memory address line during all machine states.

MACHINE STATE TIMING



INTERFACE DESCRIPTION

CLOCK,XTAL: The clock reference to the microprocessor may be supplied by an externally generated single phase clock to the Clock input or by an on-chip oscillator by using a crystal in parallel with a resistor (10 MΩtypical) tied between the Clock and XTAL inputs. Frequency trimming capacitors may be required at terminals 1 and 39.

WAIT, CLEAR: These input control lines provide four internal CPU modes:

Clear	Wait	Mode
L	L	Load
L	H	Reset
H	L	Pause
H	H	Run

The functions of the modes are defined as follows:

Load: holds the CPU in the Idle execution state and allows a peripheral device to load memory without need for a "bootstrap" loader. It modifies the Idle condition so that the DMA-IN operation does not force execution of the next instruction.

Reset: resets registers I, N and Q and places 0's (VSS) on the data bus, IE is set and the S1 state is forced. TPA and TPB are suppressed while Reset condition is held. The first machine cycle after termination of reset initializes the CPU by resetting registers X, P, and R(0). The next cycle is an S0, S1, or an S2 but never an S3 (interrupt). By using a 71 instruction followed by 00 at memory locations 0000 and 0001, respectively, IE may be reset to preclude interrupts until the user is ready for them. Power up Reset can be realized by connecting an RC network directory to the Clear input, since it has a Schmitt triggered input.

Pause: stops the internal CPU timing generator on the first negative (high-to-low) transition of the input clock. The oscillator continues to operate but all subsequent clock transitions are ignored internally while in this mode.

Run: If initiated from the Pause mode the CPU resumes operation on the first negative transition of the input clock. When initiated from the Reset operation the first machine cycle following Reset is always the initialization cycle, followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

Q, EF1-EF4: The Q output is set or reset under program control. The EF1-EF4 user generated inputs are tested under program control. These signals may be used for serial transmission or external control and status. The input flags are sampled at the beginning of every S1 cycle. Q is set or reset between the trailing edge of TPA and leading edge of TPB.

INTERFACE DESCRIPTION (Continued)

SC0, SC1: These state code outputs indicate internal CPU modes of operation:

SC1	SC0	STATE TYPE
L	L	S0 – Fetch Instruction Cycle
L	H	S1 – Execute Instruction Cycle
H	L	S2 – DMA Input or Output Cycle
H	H	S3 – Interrupt Response Cycle

$\overline{MWR}$: The negative write pulse output indicates address lines are stable during a memory write cycle.

BUS 0 – BUS 7: These 8 bi-directional three-state lines are used to transfer data between the memory, the microprocessor, and I/O devices.

V_{CC}, V_{SS}, V_{DD}: These power supply input pins allow several options since the internal voltage supply V_{DD} is isolated from the I/O interface supply V_{CC}. The processor may operate at maximum speed, governed by V_{DD}, while interfacing T^2L through V_{CC}. V_{CC} must be less than or equal to V_{DD}. All outputs swing from V_{SS} to V_{CC}.

N2, N1, N0: These three lines can directly select seven input ports and seven output ports under I/O instruction control. They are all low during non I/O operations. Input ports are selected when $\overline{MRD}$ is high and output ports are selected when $\overline{MRD}$ is low.

MA0 – MA7: These 8 output lines contain the memory address. The high order 8 bits are present during the TPA timing pulse. The low order bits appear after termination of the TPA pulse.

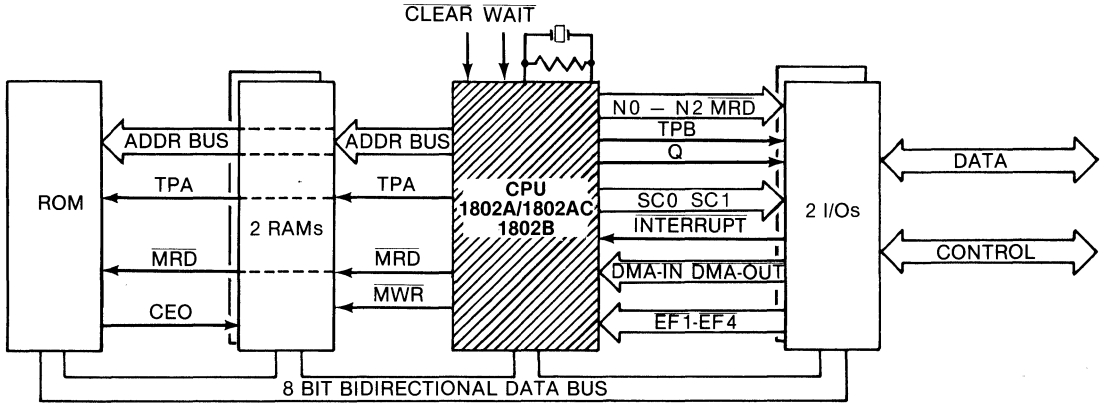
TPA, TPB: These positive timing pulse outputs are available once each machine cycle to control I/O interfaces. TPA is suppressed in idle when the CPU is in the load mode.

$\overline{MRD}$: The negative pulse output indicates a memory read cycle and may be used to control the three-state outputs of memories and to control I/O to memory interfacing during an I/O instruction.

- $\overline{MRD}$ = V_{CC} indicates data transfer from I/O to CPU and Memory.
- $\overline{MRD}$ = V_{SS} indicates data from Memory to I/O.

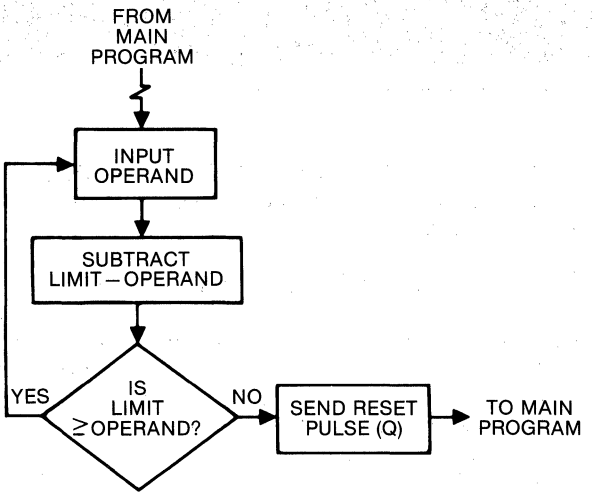
$\overline{INTERRUPT}$, $\overline{DMA\text{-}IN}$, $\overline{DMA\text{-}OUT}$: These three mode request inputs are sampled during the execution cycle of each instruction. In concurrent requests the following priority is set up: (1) DMA-In (2) DMA-Out (3) Interrupt. In DMA modes, array register R (0) points to a memory area and is incremented during each data transfer. In the Interrupt mode, the X and P indicators are stored in temporary register T, the X and P indicators are set to hex 1 and 2 respectively and the Interrupt Enable flip flop is reset.

SYSTEM BLOCK DIAGRAM



APPLICATION PROGRAM

Compare changing input for Limits, and then Reset.



ASSEMBLY LANGUAGE

MACHINE LANGUAGE

				ADDRESS	CODE
LOOP:	INP	OPER	•• INPUT OPERAND TO D	010F	6C
	SDI	# LIMIT	•• SUBTRACT LIMIT – OPERAND	0110	FD
				0111	10
	BDF	LOOP	•• BRANCH TO LOOP IF	0112	33
			NO BORROW (LIMIT ≥ OPERAND)	0113	0F
	SEQ		•• SET Q	0114	7B
	NOP		•• DELAY 3 MACHINE CYCLES	0115	C4
	REQ		•• RESET Q	0116	7A
	• •				
	• •				

INPUT CHANNEL = 4, LIMIT = 10_{16}

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Printed in U.S.A.
Rev. N/C 4/83
Supersedes Previous Data

1800 CMOS Microprocessor Family
Input/Output Port

DESCRIPTION

Hughes' 1852 is an 8 bit mode programmable CMOS Input or Output Port. The device acts as a buffer between the 1802A data bus and the peripheral data bus. It can also be used as an 8 bit address latch for multiplexed address buses.

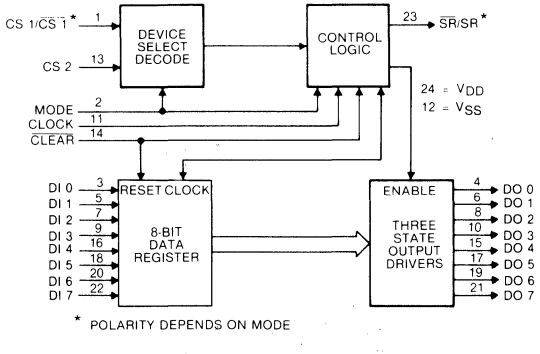
The Mode control signal programs the 1852 as an input port mode (mode = 0) or an output port (mode = 1). As an input port, data (DI 0-DI 7) is strobed from the peripheral into the 8 bit buffer register by a logic high on the Clock signal input; the negative clock transition sets the service request flip flop low ($\overline{SR}$ = 0) and latches data. When the CS 1 and CS 2 signals are enabled, the data (DO 0-DO 7) is read onto the microprocessor bus. The signal $\overline{SR}$ is then reset ($\overline{SR}$ = 1) on the negative transition CS 1 • CS 2. As an output port, data (DI 0-DI 7) is strobed into the buffer register by the microprocessor when $\overline{CS 1}$, CS 2, and the Clock input are activated. The Service Request is set on the negative transition of $\overline{CS 1}$ • CS 2, and will remain until the following negative transition of the clock. The Output driver is always enabled when the output mode is chosen. A $\overline{Clear}$ control allows asynchronous resetting of the port's register (DO 0-DO 7) and service request flip flop.

The 1852 operates over a 4—10.5 voltage range while the 1852C operates over a 4—6.5 voltage range. The 1852 is available in a 24 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

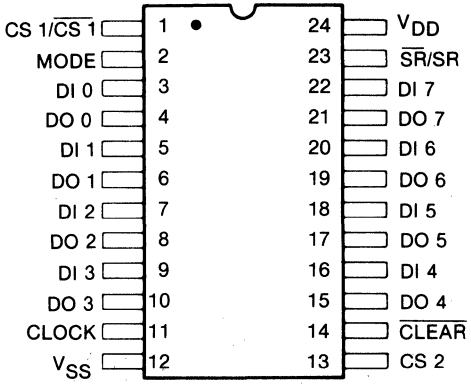
FEATURES

- Static Silicon Gate CMOS Circuitry
- Interfaces Directly with 1802A Microprocessor without Additional Components.
- Parallel 8 Bit Data Register and Buffer
- Stored Service Request
- Asynchronous Register Clear
- Single Voltage Supply
- Low Quiescent and Operating Power

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T_A)
- Ceramic Package ..... −55 to +125°C
- Plastic Package ..... −40 to + 85°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- 1852 ..... −0.5 to +13 Volts
- 1852C ..... −0.5 to +7 Volts

Storage Temperature Range (T_{stg}) .... −65 to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full Package Temperature Range.

CHARACTERISTICS	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	1852 Min.	1852 Typ.*	1852 Max.	1852C Min.	1852C Typ.*	1852C Max.	
Supply-Voltage Range (At T_A = Full Package Temperature Range)	–	–	–	4	–	10.5	4	–	6.5	V
Recommended Input Voltage Range	–	–	–	V_{SS}	–	V_{DD}	V_{SS}	–	V_{DD}	V
Static Electrical Characteristics at T_A = − 40 to + 85°C, V_{DD} = ± 5%										
Quiescent Device Current, I_{DD}	–	0,5	5	–	–	10	–	–	50	µA
	–	0,10	10	–	–	100	–	–	–	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	1.6	3.2	–	1.6	3.2	–	mA
	0.5	0,10	10	3	6	–	–	–	–	
Output High Drive (Source) Current, I_{OH}	4.6	0,5	5	−1.15	−2.3	–	−1.15	−2.3	–	mA
	9.5	0,10	10	−3	−6	–	–	–	–	
Output Voltage Low Level, V_{OL}[1]	–	0,5	5	–	0	0.1	–	0	0.1	V
	–	0,10	10	–	0	0.1	–	–	–	
Output Voltage High Level, V_{OH}	–	0,5	5	4.9	5	–	4.9	5	–	
	–	0,10	10	9.9	10	–	–	–	–	
Input Low Voltage, V_{IL}	0.5,4.5	–	5	–	–	1.5	–	–	1.5	V
	0.5,9.5	–	10	–	–	3	–	–	–	
Input High Voltage, V_{IH}	0.5,4.5	–	5	3.5	–	–	3.5	–	–	
	0.5,9.5	–	10	7	–	–	–	–	–	
Input Current, I_{IN}	–	0,5	5	–	–	±1	–	–	±1	µA
	–	0,10	10	–	–	±2	–	–	–	
3-State Output Leakage Current, I_{OUT}	0,5	0,5	5	–	–	±1	–	–	±1	
	0,10	0,10	10	–	–	±2	–	–	–	
Operating Current, I_{DD1}[2]	–	0,5	5	–	130	200	–	150	200	µA
	–	0,10	10	–	400	600	–	–	–	
Input Capacitance C_{IN}	–	–	–	–	5	7.5	–	5	7.5	pF
Output Capacitance, C_{OUT}	–	–	–	–	5	7.5	–	–	–	
DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = − 40 to +85°C, V_{DD} = ±5%, t_r, t_f = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, and 1 TTL Loan. LIMITS AT V_{DD} = + 10V APPLY TO THE 1852 ONLY.										
Required Select Pulse Width, t_{SW}	–	–	5	–	180	360	–	180	360	ns
	–	–	10	–	90	180	–	–	–	
Required Write Pulse Width, t_{WW}	–	–	5	–	130	260	–	130	260	
	–	–	10	–	65	130	–	–	–	
Required Clear Pulse Width, t_{CLR}	–	–	5	–	80	160	–	80	160	
	–	–	10	–	40	80	–	–	–	
Required Data Setup Time, t_{DS}	–	–	5	–	−10	0	–	−10	0	
	–	–	10	–	−5	0	–	–	–	
Required Data Hold Time, t_{DH}	–	–	5	–	75	150	–	75	150	
	–	–	10	–	35	75	–	–	–	

*Typical Values are for T_A =+25°C and nominal V_{DD}

NOTE 1: I_{OL} = I_{OH} = 1 µA

NOTE 2: Operating current is measured at 2MHz in an 1802 system with open outputs and a program of alternating 1 and 0 data pattern.

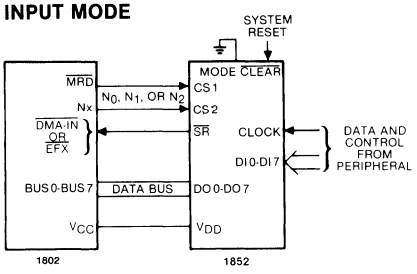
CHARACTERISTICS	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS 1852 Min.	1852 Typ.*	1852 Max.	1852C Min.	1852C Typ.*	1852C Max.	UNITS
Propogation Delay Times, t_{PLH}, t_{PHL}										
Service Request: Clear to SR, t_{RSR}	–	–	5	–	170	340	–	170	340	ns
	–	–	10	–	85	170	–	–	–	
Clock to SR, t_{CSR}	–	–	5	–	120	240	–	120	240	
	–	–	10	–	60	120	–	–	–	
Select to SR, t_{SSR}	–	–	5	–	120	240	–	120	240	
	–	–	10	–	60	120	–	–	–	
Input Mode: Data Output Hold Time[1], t_{DOH}	–	–	5	30	185	370	30	185	370	ns
	–	–	10	15	100	200	–	–	–	
Select to Data Output[1], t_{SDO}	–	–	5	30	185	370	30	185	370	
	–	–	10	15	100	200	–	–	–	
Output Mode: Clear to Data Output, t_{RDO}	–	–	5	–	140	280	–	140	280	ns
	–	–	10	–	70	140	–	–	–	
Write to Data Output, t_{WDO}	–	–	5	–	220	440	–	220	440	
	–	–	10	–	110	220	–	–	–	
Data Input to Data Output, t_{DDO}	–	–	5	–	100	200	–	100	200	
	–	–	10	–	50	100	–	–	–	

* Typical Values are for T_A = + 25°C and nominal V_{DD}

NOTE 1: Minimum value is measured from CS 2; maximum value is measured from CS 1.

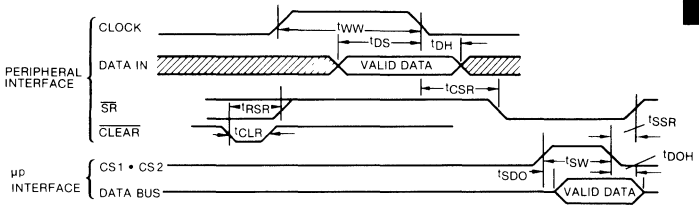
SYSTEM INTERCONNECT

INPUT MODE



INPUT MODE

CS1•CS2 is the overlap of CS1 = 1 and CS2 = 1



MODE = V_{SS} MODE 0 (INPUT)

CLOCK	CS1•CS2	$\overline{CLEAR}$	DATA OUTPUT
X	0	X	HIGH IMPEDANCE
0	1	0	0
0	1	1	DATA LATCH
1	1	X	DATA INPUT

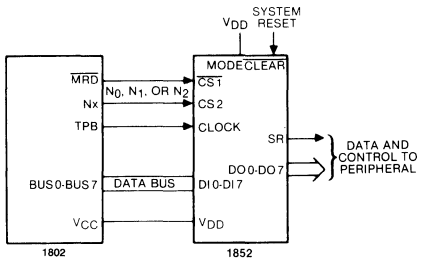
$\overline{SR}$=0 CLOCK↓ ($\overline{CLEAR}$ = 1, CS1•CS2 = 0)
$\overline{SR}$=1 (CS1•CS2)↑ OR ($\overline{CLEAR}$)↓

MODE = V_{DD} MODE 1 (OUTPUT)

CLOCK	$\overline{CS1}$•CS2	$\overline{CLEAR}$	DATA OUTPUT
0	X	0	0
0	X	1	DATA LATCH
X	0	1	DATA LATCH
1	1	X	DATA INPUT

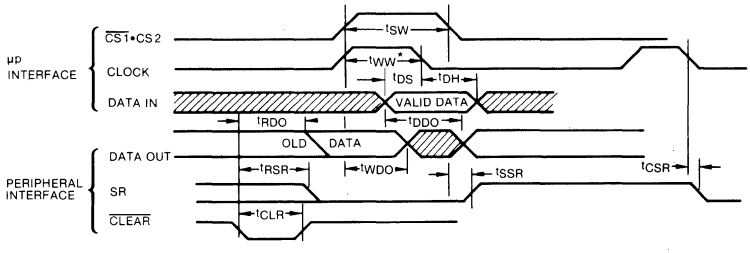
SR=1 $\overline{CS1}$•CS2↑ ($\overline{CLEAR}$ = 1)
SR=0 CLOCK↓ ($\overline{CLEAR}$ = 1, $\overline{CS1}$•CS2 = 0) OR ($\overline{CLEAR}$)↓

OUTPUT MODE



OUTPUT MODE

$\overline{CS1}$•CS2 is the overlap of $\overline{CS1}$ = 0 and CS2 = 1

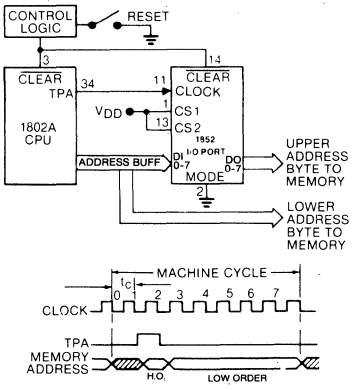


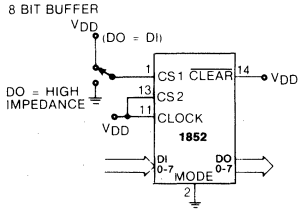
*Write is the overlap of $\overline{CS1}$•CS2 and Clock

APPLICATION EXAMPLES

Address Latch

1852 can be used as an address latch to latch the upper byte of the 1802A microprocessor memory address in each machine cycle. The figure below shows the I/O port connected for this application together with its associated timing diagram.





This figure shows 1852 connected as a non-inverting, three state, 8 bit buffer, with MODE = 0, CLOCK = 1 and CS 2 = 1, CS 1 can be used as a tri-state control. When CS 1 = 0, the output is a high impedance, but when CS 1 = 1 data output equals data input. If a high impedance state is not required, the CS 1 input can be tied high (CS 1 = 1).

SIGNAL DESCRIPTION

DI0-DI1: These 8 input lines are strobed into an internal buffer by a high level on the Clock input line and latched by the negative transition of the Clock input.

DO0-DO7: These 8 output lines reflect the information from the internal buffer when the three state drivers are enabled by CS1 • CS2 in the input mode or, at all times, in the output mode.

MODE: This control input sets the 1852 in the input mode with a V_{SS} applied or in the output mode with V_{DD} applied.

$\overline{\text{CLEAR}}$: This asynchronous reset control clears the buffer register and resets the SR flip flop.

CLOCK: Input Mode: This input strobes data into the buffer when it is activated (high) and sets the SR flip flop (SR = 0) while latching data on its negative transition.

Output Mode: This input along with the chip selects ($\overline{CS1}$ • CS2 • Clock = 1) trobes data into the buffer. The service request ($\overline{SR}$) is set high on the termination of $\overline{CS1}$ • CS2 = 1 and reset low on the next negative transition of the clock.

CS1/$\overline{\text{CS1}}$, CS2: These chip select controls enable device selection.

SR/$\overline{\text{SR}}$: This output signal is used as a service request transfer control between the microprocessor and peripheral buses.

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Printed in U.S.A. 9/83
Supersedes Previous Data

1800 CMOS Microprocessor Family
N-Bit 1 of 8 Decoder

DESCRIPTION

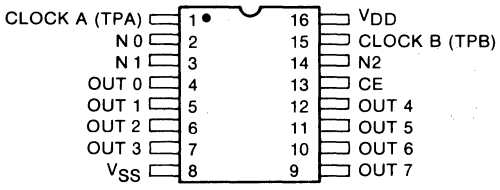
Hughes' 1853 allows decoding of the 1802A microprocessor generated I/O lines (N0-N2) to provide direct control for up to seven input and seven output devices. The TPA and TPB clock inputs provide control signal output timing while the Chip Enable (CE) input allows multi-level I/O expansion for decoding. The 1853 can also be used as a general 1 of 8 decoder for memory system applications.

The 1853 operates over a 4-10.5 voltage range while the 1853C operates over a 4-6.5 voltage range. The 1853 is available in a 16 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

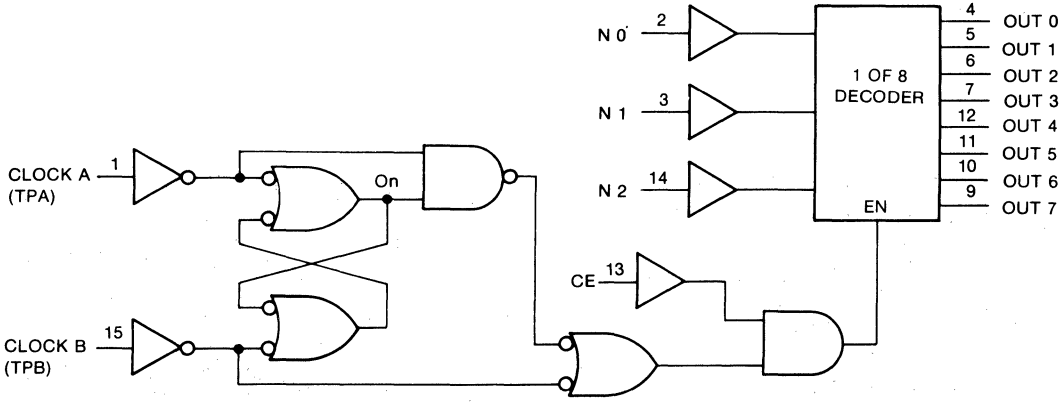
FEATURES

- Static Silicon Gate CMOS Circuitry
- Interfaces Directly with 1802A Microprocessor without Additional Components
- Provides Control for up to 7 Input and 7 Output Devices
- Low Power Dissipation
- Easy Expansion for Multi-Level I/O Systems through Chip Enable.
- Buffered Inputs and Outputs
- Strobed Outputs for Spike-Free Decoding

PIN CONFIGURATION



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T_A)
- Ceramic Package ..... −55 to + 125°C
- Plastic Package ..... −40 to + 85°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- 1853 ..... −0.5 to + 13 Volts
- 1853C ..... −0.5 to + 7 Volts

Storage Temperature Range (T_{stg}) ..... −65 to + 150°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at TA = Full Package Temperature Range

CHARACTERISTICS	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	1853			1853C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Supply-Voltage Range	—	—	—	4	—	10.5	4	—	6.5	V
Recommended Input Voltage Range	—	—	—	VSS	—	VDD	VSS	—	VDD	V
Static Electrical Characteristics at T_A = −40° to +85°C Unless Otherwise Specified										
Quiescent Device Current, I_L	—	—	5	—	1	10	—	5	50	µA
	—	—	10	—	10	100	—	—	—	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	1.6	3.2	—	1.6	3.2	—	mA
	0.5	0,10	10	2.6	5.2	—	—	—	—	
Ouput High Drive (Source Current), I_{OH}	4.6	0,5	5	-1.15	-2.3	—	-1.15	-2.3	—	mA
	9.5	0,10	10	-2.6	-5.2	—	—	—	—	
Output Voltage Low-Level, V_{OL}[1]	—	0,5	5	—	0	0.1	—	0	0.1	V
	—	0,10	10	—	0	0.1	—	—	—	
Output Voltage High Level, V_{OH}	—	0,5	5	4.95	5	—	4.95	5	—	
	—	0,10	10	9.95	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	V
	1,9	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	
	1,9	—	10	7	—	—	—	—	—	
Input Leakage Current, I_{IN}	Any Input	0,5	5	—	—	±1	—	—	±1	µA
		0,10	10	—	—	±1	—	—	—	
3-State Ouput Leakage Current, I_{OUT}	0,5	0,5	5	—	—	±1	—	—	±1	µA
	0,10	0,10	10	—	—	±1	—	—	—	
Operating Current I_{DD1}[2]	0,5	0,5	5	—	50	100	—	50	100	µA
	0,10	0,10	10	—	150	300	—	—	—	
Input Capacitance, C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT}	—	—	—	—	10	15	—	10	15	pF

*Typical values are for T_A = +25°C and nominal voltage.

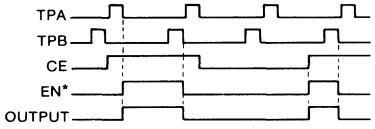
NOTE 1: $I_{OL} = I_{OH}$ = 1 uA

NOTE 2: Operating current measured in a 1802A system at 2MHz with outputs floating.

CHARACTERISTICS	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	1853			1853C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Dynamic Electrical Characteristics at T_A =−40 to +85° C, tr, tf = 20 ns CL = 100 pF V_{DD} ±5%, V_{IH} = 0.7 V_{DD}, VIL =0.3 V_{DD}										
Propogation Delay Time:	—	—	5	—	175	275	—	175	275	ns
CE to Output, t_{EOH}, t_{EOL}	—	—	10	—	90	150	—	—	—	
N to Outputs, t_{NOH}, t_{NOL}	—	—	5	—	225	350	—	225	350	ns
	—	—	10	—	120	200	—	—	—	
Clock A to Output, t_{AO}	—	—	5	—	200	300	—	200	300	ns
	—	—	10	—	100	150	—	—	—	
Clock B to Output, t_{BO}	—	—	5	—	175	275	—	175	275	ns
	—	—	10	—	90	150	—	—	—	
Minimum Pulse Widths:	—	—	5	—	50	75	—	50	75	ns
Clock A, t_{CACA}	—	—	10	—	25	50	—	—	—	
Clock B, t_{CBCB} C8	—	—	5	—	50	75	—	50	75	
	—	—	10	—	25	50	—	—	—	

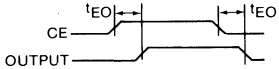
*Typical values are for TA = 25°C and nominal voltage.

TIMING DIAGRAMS

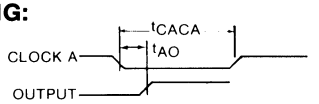


*OUTPUT ENABLED WHEN EN = HIGH
INTERNAL SIGNAL SHOWN FOR REFERENCE ONLY

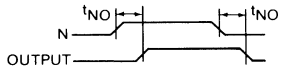
PROPOGATION DELAY TIMING:



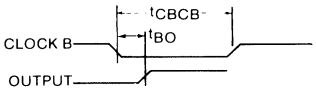
a)CE TO OUTPUT (0-7) DELAY TIME



c) CLOCK A TO OUPUT (0-7) DELAY TIME



b) N LINES TO OUTPUT (0-7) DELAY TIME



d) CLOCK B TO OUTPUT (0-7) DELAY TIME

APPLICATIONS EXAMPLES

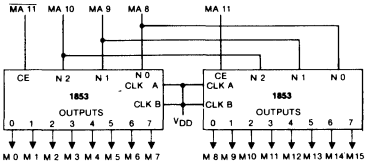
The Figure shows two 1853 used to decode 4K address into 16 groups of 256 address each.

MA 8 represents the 8th binary address bit. (i.e. 2^8 = 256)
M 0 will address 0-255
M 1 will address 256-511
M 15 will address 3840-4095

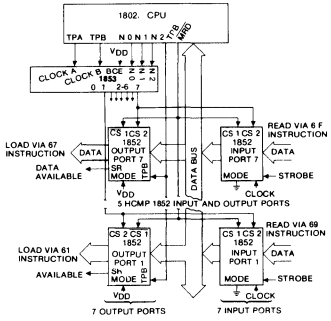
In the 1802A microprocessor systems, when more than three I/O ports are required, the N lines can be decoded to specify up to 7 different input and 7 different output channels as shown.

By executing Input instruction 69 (N lines = 001) for instance, the port 1 input register is enabled to the bus since MRD is high during the memory write cycle. The 1853 decode line 1 will also be active high during an output instruction, 61 (N lines = 001) but MRD is low during the memory read cycle disabling the memory read cycle disabling the port 1 input register from the bus. At TPB, the valid byte from memory is strobed into the port 1 output register.

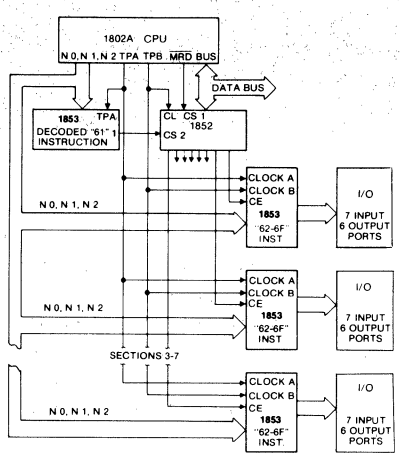
ADDRESS DECODER:



ONE LEVEL I/O SYSTEMS:



TWO LEVEL I/O SYSTEMS



In the 1802A microprocessor systems, when more than 7 input or 7 output ports are required, a two level I/O system can be designed as shown in the figure.

A 61 (N lines = 001) output instruction is first executed to place an 8-bit device selection code in the I/O device-select register, 1852. Subsequent execution of one of the 6 remaining output instructions (62-67) selects one of 48 output ports, or subsequent execution of one of the 7 input instructions (69-6F) selects one of the 56 input ports.

With additional decoding the total number of input and output ports can be further expanded.

SIGNAL DESCRIPTION

Clock A, Clock B: The selected outputs stay true from the trailing edge of the Clock A (TPA) input to the trailing edge of Clock B (TPB) input, if the chip is enabled. The transition of both the clock inputs at the trailing edge should be the high-to-low.

CE: The Chip Enable input enables the chip when high. All outputs will be low when CE = 0.

N 0, N 1, N 2: These three inputs select one of eight decoded outputs when the chip is enabled. N 0 is the least significant input, N 2 is the most significant input.

Output 0 - Output 7: One output can be selected at a time. The truth table is shown below.

TRUTH TABLE

CE	CLK A	CLK B	EN
1	0	0	Qn-1*
1	0	1	1
1	1	0	0
1	1	1	1
0	X	X	0

1 = High Level
0 = Low Level
X = Don't Care
*Qn-1 = Enable remains in previous state.

N 2	N 1	N 0	EN	0	1	2	3	4	5	6	7
0	0	0	1	1	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	1	0	0
1	1	0	1	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1
X	X	X	0	0	0	0	0	0	0	0	0

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Supersedes Previous Data

1800 CMOS Microprocessor Family
Receiver/Transmitter Universal Asynchronous

DESCRIPTION

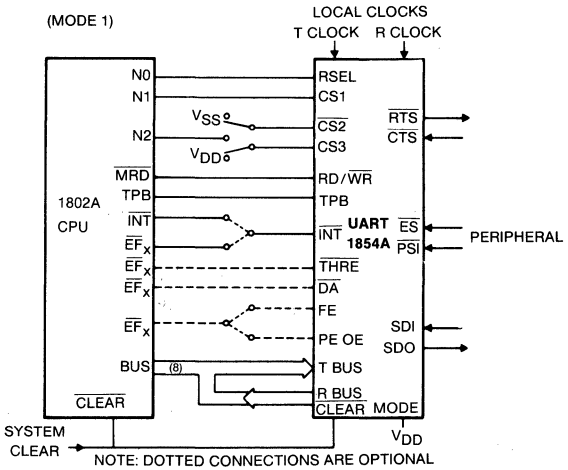
Hughes' 1854A is a CMOS Universal Asynchronous Receiver/Transmitter (UART). It is designed to provide formatting and controls to interface serial and parallel data busses, such as a telephone modem to an 1802 microprocessor bus. The 1854A is capable of full duplex operation allowing simultaneous conversion from serial to parallel (receiver section) and parallel to serial (transmitter section). A local receiver clock (R Clock) and transmitter clock (T Clock) operates at 16 times the serial data rate to provide references for receiver sampling and transmitter timing. The mode control allows the UART to be used as a functional replacement for industry standard UARTs (such as the TR1602) in mode 0 while utilizing a single supply voltage; in mode 1 the UART can be selected as a bus oriented device for direct interfacing with the 1802 microprocessor as shown below.

The 1854A operates over a 4-10.5 voltage range while the 1854C operates over a 4-6.5 voltage range. The UART is available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix), or leadless chip carrier (L suffix). Devices in chip form (H suffix) are also available upon request.

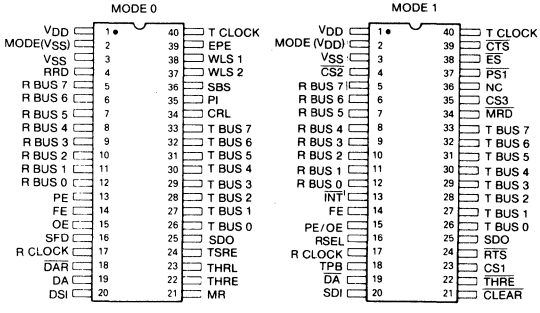
FEATURES

- Static Silicon Gate CMOS Circuitry
- Two Operating Modes
  - Mode 0 — Functionally Compatible with Industry Standard UARTs such as TR1602A
  - Mode 1 — Directly Interfaces with 1802 Microprocessor without Additional Components
- Full or Half Duplex Operation
- Baud Rate — DC to 250K at V_{DD} = 5V
  DC to 500K at V_{DD} = 10V
- Selectable Word Length, 5, 6, 7 or 8 Bits
- Programmable Parity and Stop Bits (1, 1½, 2)
- Parity, Framing and Overrun Error Detection
- Single Voltage Supply
- Low Quiescent and Operating Power

SYSTEM INTERCONNECT



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T_A)
- Ceramic Package ..... −55 to + 125°C
- Plastic Package ..... −40 to + 85°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- 1854A ..... −0.5 to + 11 Volts
- 1854AC ..... −0.5 to + 7 Volts

Storage Temperature Range (T_{stg}) ..... −65 to + 150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

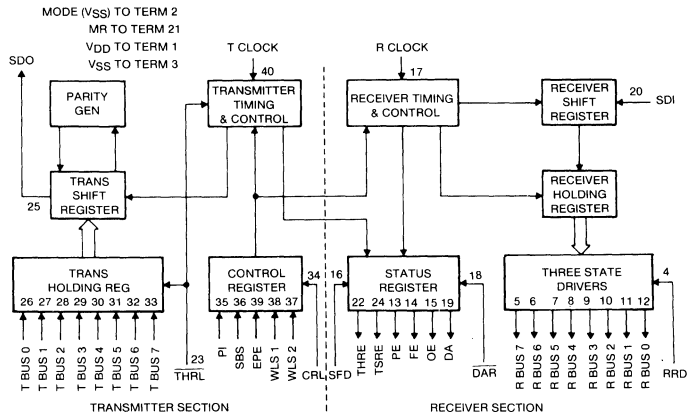
OPERATING CONDITIONS at T_A = Full Temperature Range

CHARACTERISTICS	V_{DD} (V)	TYPICAL VALUES 1854A	TYPICAL VALUES 1854AC	UNITS
Supply Voltage Range (At T_A = Full Package Temperature Range)	—	4 to 10.5	4 to 6.5	V
Recommended Input Voltage Range	—	V_{SS} to V_{DD}	V_{SS} to V_{DD}	V
Clock Input Frequency, f_{CL}	5	DC − 4	DC − 4	MHz
(16 times bit rate)	10	DC − 8	—	
Minimum Clock Pulse Width,	5	125	125	ns
t_{WL}, t_{WH}	10	100	—	
Minimum Master Reset,	5	500	500	ns
$\overline{\text{Clear}}$ Pulse Width	10	250	—	

STATIC ELECTRICAL CHARACTERISTICS at T_A = − 40 to + 85°C, Unless Otherwise Specified

CHARACTERISTICS		CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS 1854A Min.	LIMITS 1854A Typ.[1]	LIMITS 1854A Max.	LIMITS 1854AC Min.	LIMITS 1854AC Typ.[1]	LIMITS 1854AC Max.	UNITS
Quiescent Device Current	I_{DD}	—	0, 5	5	—	0.01	50	—	0.02	200	µA
		—	0, 10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	0.55	1.1	—	0.55	1.1	—	mA
		0.5	0, 10	10	1.3	2.6	—	—	—	—	
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	−0.55	−1.1	—	−0.55	−1.1	—	mA
		9.5	0, 10	10	−1.3	−2.6	—	—	—	—	
Output Voltage Low-Level	V_{OL}[2]	—	0, 5	5	—	0	0.1	—	0	0.1	V
		—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High-Level	V_{OH}	—	0, 5	5	4.9	5	—	4.9	5	—	V
		—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage	V_{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	V
		0.5, 9.5	—	10	—	—	3	—	—	—	
Input High Voltage	V_{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	V
		0.5, 9.5	—	10	7	—	—	—	—	—	
Input Current	I_{IN}	—	0, 5	5	—	$\pm 10^{-4}$	±1	—	$\pm 10^{-4}$	±1	µA
		—	0, 10	10	—	$\pm 10^{-4}$	±2	—	—	—	
Three State Output Leakage	I_{OUT}	0, 5	0, 5	5	—	$\pm 10^{-4}$	±1	—	$\pm 10^{-4}$	±1	µA
Current		0, 10	0, 10	10	—	$\pm 10^{-4}$	±2	—	—	—	
Operating Current	I_{DD1}[3]	—	0, 5	5	—	1.5	—	—	1.5	—	mA
		—	0, 10	10	—	10	—	—	—	—	
Input Capacitance	C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	—	10	15	—	10	15	

NOTE 1: Typical values are for T_A = +25°C
NOTE 2: I_{OL} = I_{OH} = 1 µA.
NOTE 3: Operating current is measured at 200 kHz for V_{DD} = 5 Volts and 400 kHz for V_{DD} = 10 Volts in an 1802 system, with open outputs.



DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = — 40 to + 85°C, V_{DD} ± 5%, t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF, See Fig. 1.

CHARACTERISTICS		V_{DD} (V)	LIMITS 1854A Typ.[1]	LIMITS 1854A Max.[2]	LIMITS 1854AC Typ.[1]	LIMITS 1854AC Max.[2]	UNITS
Standard Timing — MODE 0							
Minimum Pulse Width:	t_{CRL}	5	100	150	100	150	ns
		10	50	75	—	—	
Minimum Setup Time: Control Word to CRL	t_{CWC}	5	200	300	200	300	ns
		10	100	150	—	—	
Minimum Hold Time: Control Word after CRL	t_{CCW}	5	100	150	100	150	ns
		10	50	75	—	—	
Propagation Delay Time: SFD High to SOD	t_{SFDH}	5	200	300	200	300	ns
		10	100	150	—	—	
SFD Low to SOD	t_{SFDL}	5	75	120	75	120	ns
		10	40	60	—	—	
RRD High to Receiver Register High Impedence	t_{RRDH}	5	200	300	200	300	ns
		10	100	150	—	—	
RRD Low to Receiver Register Active	t_{RRDL}	5	100	150	100	150	ns
		10	50	75	—	—	

NOTE 1: Typical values are for T_A = + 25°C and nominal voltages.
NOTE 2: Maximum limits of minimum characteristics are the values above which all devices function.

TABLE 1. DYNAMIC ELECTRICAL CHARACTERISTICS

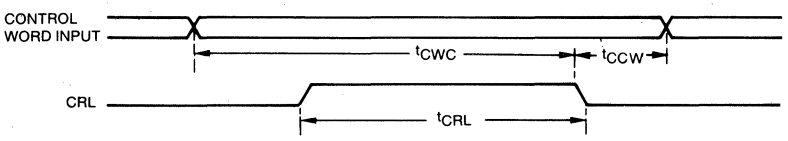
MODE 0 OPERATION (MODE INPUT = V_{SS})

A. Initialization and Controls

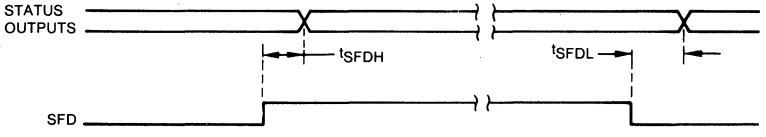
The Master Reset (MR) is pulsed to initialize the UART; for example, after power turn on. It resets (zeroes) the Control, Status and Receiver Holding Registers and sets the Serial Data Output (SDO) signal to a logic high. After release of the Master Reset (return to a logic low), the internal timing is generated from the Transmitter Clock (T Clock) and Receiver Clock (R Clock) inputs which are divided internally by sixteen to provide the serial data bit rate. When the receiver data input rate and the transmitter data output rate are the same, as in two-way communications over the same channel, the T Clock and R Clock inputs may be connected together.

To set the operational mode of the UART the control inputs: Parity Inhibit (PI), Even Parity Enable (EPE), Stop Bit Select (SBS), and Word Length Selects (WLS1 and WLS2) are strobed into the UART by the Control Register Load (CRL) input signal activation (logic high). The control bits may be dynamically changed or may be hard wired to the required voltage level (V_{SS}) or V_{DD}) with CRL hard wired to V_{DD}. The 1854A is then ready for transmitter and/or receiver operation.

CONTROL INPUT WORD TIMING



STATUS OUTPUT TIMING



RECEIVER REGISTER DISCONNECT TIMING

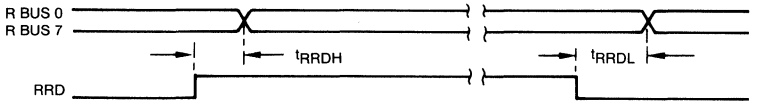


FIGURE 1. STANDARD MODE 0 TIMING DIAGRAM

B. Word Format

A diagram of the serial data word format is shown in Fig. 2. The data, 5-8 bits, is transmitted with the least significant bit (LSB) sent first. The parity bit, if enabled, is sent after the most significant data bit. The parity may be either odd or even as chosen by the Control Word. The data is enclosed by a Start bit (logic low) identifying start of character transmission and either 1, 1½, or 2 bit wide Stop bit(s) which identifies the end of character transmission and separates successive data words. The width of each data bit is normally 16 input clock widths of 16/f where f is the clock frequency.

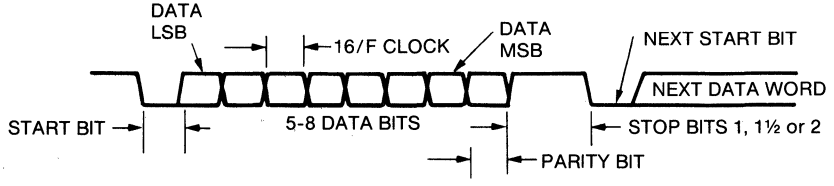


FIGURE 2. SERIAL DATA WORD FORMAT

C. Transmitter Operation

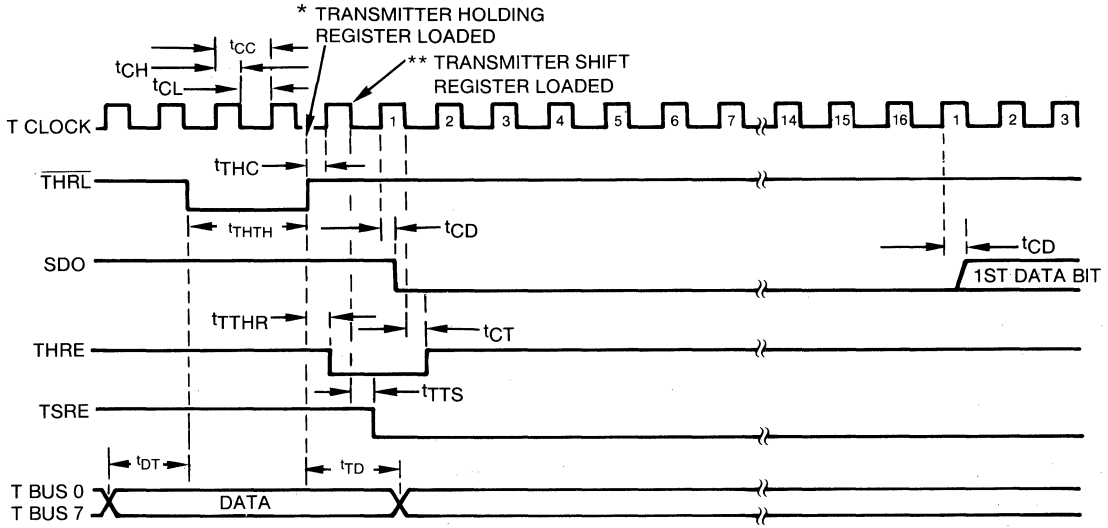
The transmitter timing diagram showing the start of data transmission are seen in Figure 3. At the beginning of a transmitting sequence the Transmitter Holding Register is empty (status signal THRE is high). A character is transferred from the transmitter bus to the Transmitter Holding Register by applying a low pulse to the Transmitter Holding Register Load ($\overline{\text{THRL}}$) input. This causes the THRE status to go to a low state. If the Transmitter Shift Register is empty (Status signal TSRE is High) and the input clock is low, the next high-to-low transition of the clock loads the contents of the Transmitter Holding Register into the Transmitter Shift Register, preceded by a start (low) bit. Serial data tranmission begins one-half clock period later with a start bit, followed by 5-8 data bits, the parity bit (if programmed) and stop bit(s). The THRE status signal returns high one-half clock period later on the high-to-low transition of the input clock. When THRE goes high it signals that another character can be loaded into the Transmitter Holding Register for subsequent transmission immediately following the last stop bit of the previous character. This process is repeated until all characters are transmitted. When transmission is complete both THRE and the Transmitter Shift Register Empty (TSRE) status signals will be high.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = — 40 to + 85°C, V_{DD} ± 5%, t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF, See Fig. 3.

CHARACTERISTICS		V_{DD} (V)	LIMITS 1854A Typ.[1]	LIMITS 1854A Max.[2]	LIMITS 1854AC Typ.[1]	LIMITS 1854AC Max.[2]	UNITS
Transmitter Timing — MODE 0							
Minimum Clock Period	t_{CC}	5 10	250 125	310 155	250 —	310 —	ns
Minimum Pulse Width: Clock Low Level	t_{CL}	5 10	100 75	125 100	100 —	125 —	ns
Clock High Level	t_{CH}	5 10	100 75	125 100	100 —	125 —	ns
$\overline{THRL}$	t_{THTH}	5 10	100 50	150 75	100 —	150 —	ns
Minimum Setup Time: $\overline{THRL}$ to Clock	t_{THC}	5 10	175 90	275 150	175 —	275 —	ns
Data to $\overline{THRL}$	t_{DT}	5 10	−100 −50	−75 −35	−100 —	−75 —	ns
Minimum Hold Time: Data after $\overline{THRL}$	t_{TD}	5 10	75 40	125 60	75 —	125 —	ns
Propagation Delay Time: Clock to Data Start Bit	t_{CD}	5 10	300 150	450 225	300 —	450 —	ns
Clock to THRE	t_{CT}	5 10	200 100	300 150	200 —	300 —	ns
$\overline{THRL}$ to THRE	t_{TTHR}	5 10	200 100	300 150	200 —	300 —	ns
Clock to TSRE	t_{TTS}	5 10	200 100	300 150	200 —	300 —	ns

NOTE 1: Typical values are for T_A = + 25°C and nominal voltages.
NOTE 2: Maximum limits of minimum characteristics are the values above which all devices function.

TABLE 2. TRANSMITTER TIMING MODE 0



* THE HOLDING REGISTER IS LOADED ON THE TRAILING EDGE OF $\overline{THRL}$

** THE TRANSMITTER SHIFT REGISTER, IF EMPTY, IS LOADED ON THE FIRST HIGH-TO-LOW TRANSITION OF THE CLOCK WHICH OCCURS AT LEAST 1/2 CLOCK PERIOD + t_{THC} AFTER THE TRAILING EDGE OF $\overline{THRL}$, AND TRANSMISSION OF A START BIT OCCURS 1/2 CLOCK PERIOD + t_{CD} LATER

FIGURE 3. MODE 0 TRANSMITTER TIMING DIAGRAM

D. Receiver Operation

The receive operation begins when a Start bit (logic low) is detected at the Serial Data In (SDI) input. When a high-to-low transition is detected on the SDI line a divide by 16 internal counter is enabled, driven by the R Clock input, and a valid Start bit is verified by checking for a low level input 7½ receiver clock periods later. This prevents false triggering on noise inputs. When a valid Start bit is verified, the sampling occurs every subsequent 16 clock pulses to shift in data bits, parity bit (if programmed) and stop bit(s) into the Receiver Shift Register. If programmed, the parity bit is checked and the Parity Error (PE) status updated. The receipt of a valid Stop bit is also verified and Framing Error (FE) status updated. On count 7½ of the first Stop bit the received data is transferred to the Receiver Holding Register. If the word length is less than 8 bits, zeroes (low voltage level) are loaded into the unused most significant bits. If the Data Available (DA) flag has not been reset by the time the Receiver Holding Register is updated with new data, the Overrun Error (OE) flag is activated to a high level. One half clock after the data transfer the Parity Error (PE) and Framing Error (FE) signals become valid for the character in the Receiver Holding Register. The DA signal is also raised at this time. The three-state output drivers for the status and error flags (DA, OE, PE and FE) are enabled when Status Flag Disconnect (SFD) is pulsed or hard wired to a low voltage state. When Receiver Register Disconnect (RRD) goes low, the receiver bus three-state output drivers are enabled and data is available on the Receiver Bus (R BUS 0 — R BUS 7) output lines. The DA flag is reset by a negative pulse on the Data Available Reset ($\overline{DAR}$) input.

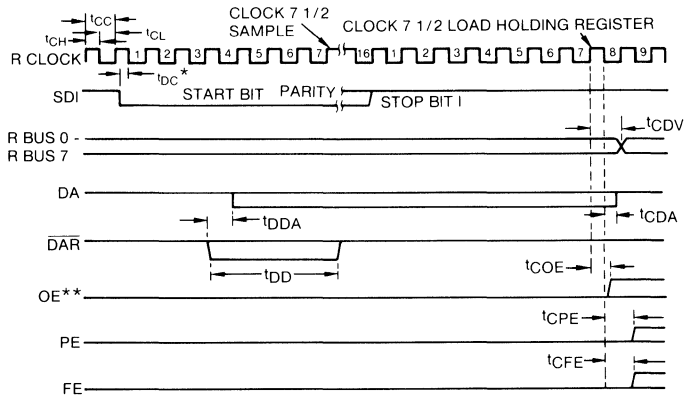
The preceding sequence of operations is repeated for each serial character received. The receiver timing diagram is shown in Figure 4.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ±5%, t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF. See Fig. 4.

CHARACTERISTICS		V_{DD} (V)	LIMITS 1854A Typ.[1]	LIMITS 1854A Max.[2]	LIMITS 1854AC Typ.[1]	LIMITS 1854AC Max.[2]	UNITS
Receiver Timing — MODE 0							
Minimum Clock Period	t_{CC}	5 10	250 125	310 155	250 —	310 —	ns
Minimum Pulse Width: Clock Low Level	t_{CL}	5 10	100 75	125 100	100 —	125 —	ns
Clock High Level	t_{CH}	5 10	100 75	125 100	100 —	125 —	ns
$\overline{\text{Data Available Reset}}$	t_{DD}	5 10	50 25	75 40	50 —	75 —	ns
Minimum Setup Time: Data Start Bit to Clock	t_{DC}	5 10	100 50	150 75	100 —	150 —	ns
Propagation Delay Time: $\overline{\text{Data Available Reset}}$ to Data Available	t_{DDA}	5 10	150 75	225 125	150 —	225 —	ns
Clock to Data Valid	t_{CDV}	5 10	225 110	325 175	225 —	325 —	ns
Clock to Data Available	t_{CDA}	5 10	225 110	325 175	225 —	325 —	ns
Clock to Overrun Error	t_{COE}	5 10	210 100	300 150	210 —	300 —	ns
Clock to Parity Error	t_{CPE}	5 10	240 120	375 175	240 —	375 —	ns
Clock to Framing Error	t_{CFE}	5 10	200 100	300 150	200 —	300 —	ns

NOTE 1: Typical values are for T_A = + 25°C and nominal voltages.
NOTE 2: Maximum limits of minimum characteristics are the values above which all devices function.

TABLE 3



* IF A START BIT OCCURS AT A TIME LESS THAN t_{DC} BEFORE A HIGH-TO-LOW TRANSITION OF THE CLOCK, THE START BIT MAY NOT BE RECOGNIZED UNTIL THE NEXT HIGH-TO-LOW TRANSITION OF THE CLOCK. THE START BIT MAY BE COMPLETELY ASYNCHRONOUS WITH THE CLOCK.

** IF A PENDING DA HAS NOT BEEN CLEARED BY A READ OF THE RECEIVER HOLDING REGISTER BY THE TIME A NEW WORD IS LOADED INTO THE RECEIVER HOLDING REGISTER, THE OE SIGNAL WILL COME TRUE.

FIGURE 4. MODE 0 RECEIVER TIMING DIAGRAM

SIGNAL DESCRIPTION (Standard Mode 0)

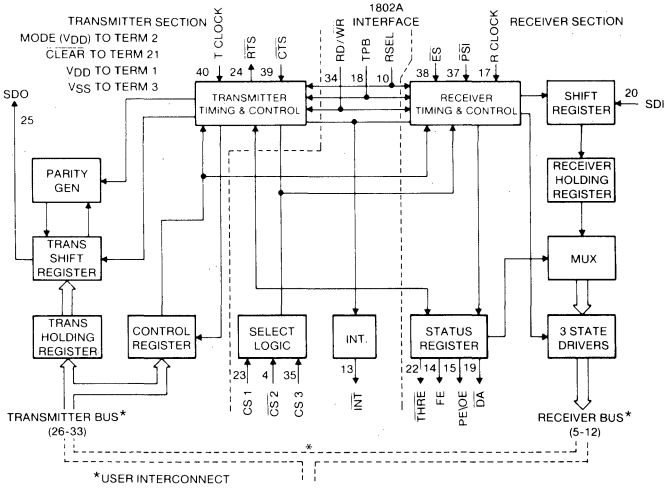
Terminal No.	Signal	Function
1	V_{DD}	Positive supply
2	Mode Select (Mode)	A low level voltage at this input selects Standard Mode 0 Operation.
3	V_{SS}	Ground
4	Receiver Register Disconnect (RRD)	A high-level voltage applied to this input disconnects the Receiver Holding Register from the Receiver Bus.
5-12	Receiver Bus (R BUS 0 — R BUS 7)	Receiver parallel data outputs. R BUS 7 is the most significant bit.
13	Parity Error (PE)	A high-level voltage at this output indicates that the received parity does not compare to that programmed by the Even Parity Enable (EPE) control. This output is updated each time a character is transferred to the Receiver Holding Register. PE lines from a number of arrays can be bused together since an output disconnect capability is provided by the Status Flag Disconnect (SFD) line.
14	Framing Error (FE)	A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) or MSB of data (if parity is not programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register. FE lines from a number of arrays can be bused together since an output disconnect capability is provided by the Status Flag Disconnect (SFD) line.
15	Overrun Error (OE)	A high-level voltage at this output indicates that the Data Available (DA) flag was not reset before the next character was transferred to the Receiver Holding Register and the previous data was presumably lost. OE lines from a number of arrays can be bused together since an output disconnect capability is provided by the Status Flag Disconnect (SFD) line.
16	Status Flag Disconnect (SFD)	A high-level voltage applied to this input disables the 3-state output drivers for PE, FE, OE, DA, and THRE, allowing these status outputs to be bus connected.
17	Receiver Clock (R Clock)	Clock input with a frequency 16 times the desired receiver bit shift rate.
18	$\overline{\text{Data Available}}$ $\overline{\text{Reset}}$ ($\overline{\text{DAR}}$)	A low-level voltage applied to this input resets the DA flip-flop.
19	Data Available (DA)	A high-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.

20	Serial Data Input (SDI)	Serial data received at this input enters the receiver shift register at a point determined by the character length. A high-level voltage must be present when data is not being received (IDLE STATE)
21	Master Reset (MR)	A high-level voltage at this input resets the Receiver Holding Register, Control Register, and Status Register, and sets the serial data output high.
22	Transmitter Holding Register Empty (THRE)	A high-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.
23	Transmitter Holding Register Load ($\overline{\text{THRL}}$)	A low-level voltage applied to this input enters the character on the data bus into the Transmitter Holding Register. Data is latched on the trailing edge of this signal.
24	Transmitter Shift Register Empty (TSRE)	A high-level voltage at this output indicates that the Transmitter Shift Register has completed serial transmission of a full character including stop bit(s). It remains at this level until the start of transmission of the next character.
25	Serial Data Output (SDO)	The contents of the Transmitter Shift Register (start bit, data bits, parity bit, and stop bit(s) are serially shifted out on this output. When no character is being transmitted, a high-level idle state is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.
26-33	Transmitter Bus (T BUS 0 — T BUS 7)	Transmitter parallel data inputs. T BUS 7 is the most significant bit.
34	Control Register Load (CRL)	A high-level voltage at this input loads the Control Register with the control bits (PI, EPE, SBS, WLS1, WLS2). This line may be strobed or hardwired to a high-level input voltage.
35	Parity Inhibit (PI)	A high-level voltage at this input inhibits the parity generation and verification circuits and will clamp the PE output low. If parity is inhibited the stop bits(s) will immediately follow the last data bit on transmission.
36	Stop Bit Select (SBS)	This input selects the number of stop bits to be transmitted after the parity bit. A high-level selects two stop bits, a low-level selects one stop bit. Selection of two stop bits (logic high) with five data bits programmed (WLS2 = low. WLS1 = low) selects 1.5 stop bits.
37	Word Length Select 2 (WLS2)	These two inputs select the character length (exclusive of parity) as follows:
38	Word Length Select 1 (WLS1)	

WLS2	WLS1	Word Length
Low	Low	5 Bits
Low	High	6 Bits
High	Low	7 Bits
High	High	8 Bits

39	Even Parity Enable (EPE)	A high-level voltage at this input selects even parity to be generated by the transmitter and checked by the receiver. A low-level input selects odd parity.
40	Transmitter Clock (T Clock)	Clock input with a frequency 16 times the desired transmitter shift rate.

FUNCTIONAL DIAGRAM (1802 Compatible — Mode 1)



MODE 1 OPERATION (MODE INPUT = V_{DD})

A. Initialization and Controls

In the microprocessor compatible mode the 1854A is configured to receive commands and transmitter data, and to send status and receiver data via the microprocessor data bus. The register selected to be connected to the transmitter bus or receiver bus is determined by the Read/$\overline{\text{Write}}$ (RD/$\overline{\text{WR}}$) and Register Select (RSEL) inputs as follows:

RSEL	RD/$\overline{\text{WR}}$	Function
Low	Low	Load Transmitter Holding Register from Transmitter Bus
Low	High	Read Receiver Holding Register from Receiver Bus
High	Low	Load Control Register from Transmitter Bus
High	High	Read Status Register from Receiver Bus

TABLE 4. REGISTER SELECTION

In mode 1 the 1854A is compatible with an 8 bit bidirectional bus system. The Receiver and Transmitter buses can be connected together externally to directly interface with the microprocessor bus. The I/O control signals generated by the 1802 can be connected directly to the 1854A as shown on the front page.

To initiate the UART operation the $\overline{\text{Clear}}$ input is pulsed which resets the Control, Status and Receiver Holding Registers and sets the Serial Data Out (SDO) to a logic high. The Control Register is then loaded from the Transmitter bus to determine the operating configuration for the UART. Data is transferred over the transmitter bus to the Control Register during the TPB lock output from the 1802 when the UART is selected (CS 1•$\overline{\text{CS 2}}$•CS 3 = 1) and the control Register is designated (RSEL) = high, RD/$\overline{\text{WR}}$ = low). The status register of the 1854A can be read onto the Receiver bus (R BUS 0 — R BUS 7) to determine the UART status. Some of these bits are also available at separate terminals as indicated in the mode 1 block diagram.

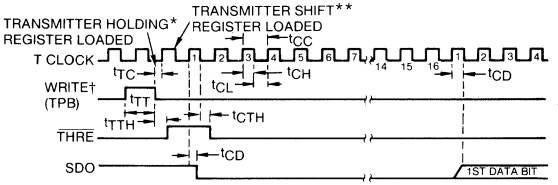
B. Transmitter Operation

Before transmitting, the Transmit Request (TR) bit in the Control Register must be set. This is done by executing the operation to load the Control Register with the TR bit set (bit 7) in the byte transmitted over the bus. When bit 7 is high it inhibits changing of the other control bits. Therefore, two loads are required: one to format the UART, the second to set TR. When TR has been set a $\overline{\text{Transmitter Holding Register Empty}}$ ($\overline{\text{THRE}}$) interrupt will occur, signaling the microprocessor (normally through the $\overline{\text{INTR}}$ or $\overline{\text{EF}}$ lines) that the Transmitter Holding Register is empty and may be loaded with data. Setting TR also sets a low level on the $\overline{\text{Request To Send}}$ ($\overline{\text{RTS}}$) output to peripherals (such as a modem).

The Transmitter Holding Register is loaded from the bus by TPB during execution of an Output instruction from the microprocessor. The 1854A UART is selected by (CS 1•$\overline{\text{CS 2}}$•CS 3 = 1). The Transmitter Holding Register is selected by RSEL = low and RD/$\overline{\text{WR}}$ = low. When the $\overline{\text{Clear To Send}}$ ($\overline{\text{CTS}}$) input signal is low the Transmitter Shift Register is loaded with the contents of the Transmitter Holding Register and data transmission will begin. If $\overline{\text{CTS}}$ is low the Transmitter Shift Register will be loaded on the first high-to-low edge of the clock which occurs at least 1/2 clock period after the TPB trailing edge. Transmission of the start bit occurs 1/2 clock period later (see Fig. 5). Parity (if programmed) and stop bit(s) are transmitted following the last data bit. If the word length selected is less than 8 bits, the most significant unused bits in the transmitter shift register will not be transmitted.

One transmitter clock period after the Transmitter Shift Register is loaded the THRE signal goes to a low and the interrupt is asserted ($\overline{INT}$ goes low). The next character to be transmitted can then be loaded into the Transmitter Holding Register and its Start bit will immediately follow the last Stop bit of the previous character. This cycle is repeated until the last character is transmitted, at which time a final THRE•TSRE interrupt will occur. This interrupt signals the microprocessor that the TR control bit can be turned off by reloading the original control byte with the TR bit = 0. This also terminates the $\overline{\text{Request To Send}}$ ($\overline{RTS}$) signal.

The Serial Data Out (SDO) line can be held low by setting the Break bit (bit 6) in the Control Register to a high. SDO is held low until the Break bit is reset.



* The Holding Register is Loaded On the Trailing Edge of TPS.

** The Transmitter Shift Register is Loaded On the First High-to-Low Transition of the Clock Which Occurs at Least 1/2 Clock Period + t_{TC} After the Trailing Edge of TPS, and Transmission of a Start Bit Occurs 1/2 Clock Period + t_{CD} Later.

† Write is the Overlap of TPS, CS 1 and $\overline{CS\ 3}$ = 1 and CS 3, RD/$\overline{WR}$ = 0.

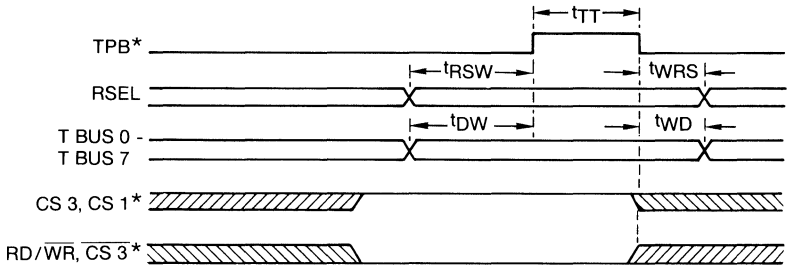
FIGURE 5. TRANSMITTER TIMING DIAGRAM — MODE 1

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = — 40 to + 85°C, V_{DD} ± 5%, t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF, See Figs. 5 and 6.

CHARACTERISTICS		V_{DD} (V)	LIMITS 1854A Typ.[1]	1854A Max.[2]	1854AC Typ.[1]	1854AC Max.[2]	UNITS
Transmitter Timing — MODE 1							
Minimum Clock Period	t_{CC}	5 10	250 125	310 155	250 —	310 —	ns
Minimum Pulse Width: Clock Low Level	t_{CL}	5 10	100 75	125 100	100 —	125 —	ns
Clock High Level	t_{CH}	5 10	100 75	125 100	100 —	125 —	ns
TPB	t_{TT}	5 10	100 50	150 75	100 —	150 —	ns
Minimum Setup Time: TPB to Clock	t_{TC}	5 10	175 90	225 150	175 —	225 —	ns
Propagation Delay Time: Clock to Data Start Bit	t_{CD}	5 10	300 150	450 225	300 —	450 —	ns
TPB to $\overline{THRE}$	t_{TTH}	5 10	200 100	300 150	200 —	300 —	ns
Clock to $\overline{THRE}$	t_{CTH}	5 10	200 100	300 150	200 —	300 —	ns
CPU Interface — WRITE Timing — MODE 1							
Minimum Pulse Width: TPB	t_{TT}	5 10	100 50	150 75	100 —	150 —	ns
Minimum Setup Time: RSEL to Write	t_{RSW}	5 10	50 25	75 40	50 —	75 —	ns
Data to Write	t_{DW}	5 10	—100 —50	—75 —35	—100 —	—75 —	ns
Minimum Hold Time: RSEL after Write	t_{WRS}	5 10	50 25	75 40	50 —	75 —	ns
Data after Write	t_{WD}	5 10	75 40	125 60	75 —	125 —	ns

NOTE 1: Typical values are for T_A = + 25°C and nominal voltages.

NOTE 2: Maximum limits of minimum characteristics are the values above which all devices function.

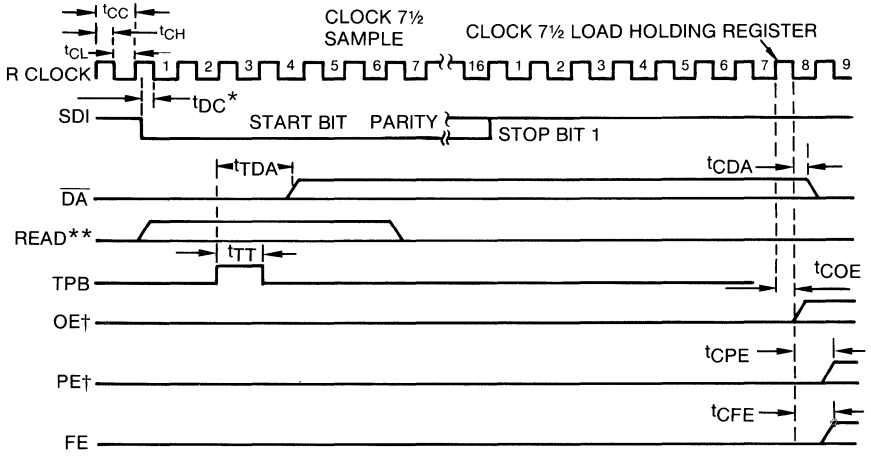


* WRITE IS THE OVERLAP OF TPB, CS 1, CS 3 = 1 AND $\overline{CS\ 2}$, RD/$\overline{WR}$ = 0.

FIGURE 6. MODE 1 CPU INTERFACE (WRITE) TIMING DIAGRAM

C. Receiver Operation

The receive operation begins when a start bit is detected at the Serial Data In (SDI) input. After detection of the first high-to-low transition on the SDI line, a valid START bit is verified by checking for a low level input 7½ receiver clock periods later. After verification of a valid Start bit, the following data bits, parity bit (if programmed) and Stop bit(s) are shifted into the Receiver Shift Register by being sampled every sixteen clocks (at clock pulse 7½). On count 7½ of the first Stop bit the data in the Receiver Register is loaded into the Receiver Holding Register. If the word length is less than 8 bits, zeros (low level outputs) are loaded into the unused left-most (significant) bits. If $\overline{\text{Data Available}}$ ($\overline{DA}$) has not been reset by the time the Receiver Holding Register is loaded, the Overrun Error (OE) status bit is set. One half clock period later the Parity Error (PE) and Framing Error (FE) status bits become valid for the character in the Receiver Holding Register. Also, at this time, the $\overline{\text{Data Available}}$ ($\overline{DA}$) and $\overline{\text{Interrupt}}$ ($\overline{INT}$) outputs go low, signaling to the microprocessor that a received character is available to be read. The microprocessor responds by executing an Input instruction. The UART's 3-state bus drivers are enabled when the UART is selected (CS 1•$\overline{CS\ 2}$•CS 3 = 1) and RD/$\overline{WR}$ is high. Data is read when RSEL = low and status is read when RSEL = high. When reading data, TPB latches the data in the microprocessor and resets the $\overline{\text{Data Available}}$ ($\overline{DA}$) signal in the UART. This sequence is repeated for each serial character which is received from the peripheral.



* IF A START BIT OCCURS AT A TIME LESS THAN t_{DC} BEFORE A HIGH-TO-LOW TRANSITION OF THE CLOCK, THE START BIT MAY NOT BE RECONGIZED UNTIL THE NEXT HIGH-TO-LOW TRANSITION OF THE CLOCK. THE START BIT MAY BE COMPLETELY ASYNCHRONOUS WITH THE CLOCK.

** READ IS THE OVERLAP OF CS 1, CS 3, RD/$\overline{WR}$ = 1 and $\overline{CS\ 2}$ = 0.
IF A PENDING DA HAS NOT BEEN CLEARED BY A READ OF THE RECEIVER HOLDING REGISTER BY THE TIME A NEW WORD IS LOADED INTO THE RECEIVER HOLDING REGISTER, THE OE SIGNAL WILL COME TRUE.

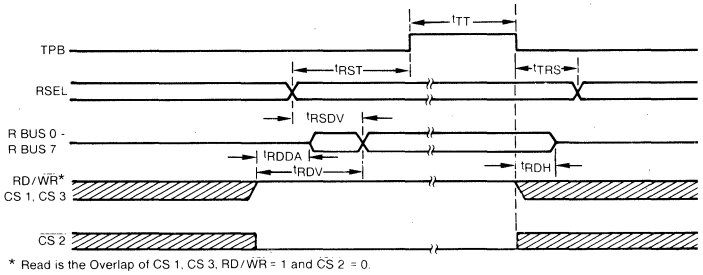
† OE AND PE SHARE TERMINAL 15 AND ARE ALSO AVAILABLE AS TWO SEPARATE BITS IN THE STATUS REGISTER.

FIGURE 7. MODE 1 RECEIVER TIMING DIAGRAM

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = — 40 to + 85°C, V_{DD} ± 5%, t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF, See Figs. 7 and 8.

CHARACTERISTICS		V_{DD} (V)	LIMITS 1854A Min.	1854A Typ.[1]	1854A Max.[2]	1854AC Min.	1854AC Typ.[1]	1854AC Max.[2]	UNITS
Receiver Timing — MODE 1									
Minimum Clock Period	t_{CC}	5	—	250	310	—	250	310	ns
		10	—	125	155	—	—	—	
Minimum Pulse Width: Clock Low Level	t_{CL}	5	—	100	125	—	100	125	ns
		10	—	75	100	—	—	—	
Clock High Level	t_{CH}	5	—	100	125	—	100	125	ns
		10	—	75	100	—	—	—	
TPB	t_{TT}	5	—	100	150	—	100	150	ns
		10	—	50	75	—	—	—	
Minimum Setup Time: Data Start Bit to Clock	t_{DC}	5	—	100	150	—	100	150	ns
		10	—	50	75	—	—	—	
Propagation Delay Time: TPB to $\overline{\text{DATA AVAILABLE}}$	t_{TDA}	5	—	220	325	—	220	325	ns
		10	—	110	175	—	—	—	
Clock to $\overline{\text{DATA AVAILABLE}}$	t_{CDA}	5	—	220	325	—	220	325	ns
		10	—	110	175	—	—	—	
Clock to Overrun Error	t_{COE}	5	—	210	300	—	210	300	ns
		10	—	105	150	—	—	—	
Clock to Parity Error	t_{CPE}	5	—	240	375	—	240	375	ns
		10	—	120	175	—	—	—	
Clock to Framing Error	t_{CFE}	5	—	200	300	—	200	300	ns
		10	—	100	150	—	—	—	
CPU Interface — READ Timing — MODE 1									
Minimum Pulse Width: TPB	t_{TT}	5	—	100	150	—	100	150	ns
		10	—	50	75	—	—	—	
Minimum Setup Time: RSEL to TPB	t_{RST}	5	—	50	75	—	50	75	ns
		10	—	25	40	—	—	—	
Minimum Hold Time: RSEL after TPB	t_{TRS}	5	—	50	75	—	50	75	ns
		10	—	25	40	—	—	—	
Read to Data Access Time	t_{RDDA}	5	—	200	300	—	200	300	ns
		10	—	100	150	—	—	—	
Read to Data Valid Time	t_{RDV}	5	—	200	300	—	200	300	ns
		10	—	100	150	—	—	—	
RSEL to Data Valid Time	t_{RSDV}	5	—	150	225	—	150	225	ns
		10	—	75	125	—	—	—	
Hold Time: Data after Read	t_{RDM}	5	50	150	—	50	150	—	ns
		10	25	75	—	—	—	—	

NOTE 1: Typical values are for T_A = + 25°C and nominal voltages.
NOTE 2: Maximum limits of minimum characteristics are the values above which all devices function.



* Read is the Overlap of CS 1, CS 3, RD/$\overline{WR}$ = 1 and $\overline{CS}$ 2 = 0.

FIGURE 8. MODE 1 CPU INTERFACE (READ) TIMING DIAGRAM

Control Register Bit Assignment

Bit	7	6	5	4	3	2	1	0
Signal	TR	BREAK	IE	WLS2	WLS1	SBS	EPE	PI

Bit	Signal	Function
0	Parity Inhibit (PI)	When set high parity generation and verification are inhibited and the PE Status bit is held low. If parity is inhibited the stop bit(s) will immediately follow the last data bit on transmission, and EPE is ignored.
1	Even Parity Enable (EPE)	When set high, even parity is generated by the transmitter and checked by the receiver. When low, odd parity is selected.
2	Stop Bit Select (SBS)	See table below.
3	Word Length Select 1 (WLS1)	See table below.
4	Word Length Select 2 (WLS2)	See table below.

Bit 4 WLS2	Bit 3 WLS1	Bit 2 SB S	Function
0	0	0	5 data bits, 1 stop bit
0	0	1	5 data bits, 1.5 stop bits
0	1	0	6 data bits, 1 stop bit
0	1	1	6 data bits, 2 stop bits
1	0	0	7 data bits, 1 stop bit
1	0	1	7 data bits, 2 stop bits
1	1	0	8 data bits, 1 stop bit
1	1	1	8 data bits, 2 stop bits

5	Interrupt Enable (IE)	When set high $\overline{\text{THRE}}$, DA, THRE•TSRE, $\overline{\text{CTS}}$, and PSI interrupts are enabled (see interrupt Conditions, Table 5
6	Transmit Break (Break)	Holds SDO in a spacing (low) condition when set. Once the break bit in the control register has been set high, SDO will stay low until the break bit is reset low or one of the following occurs — Clear goes low; $\overline{\text{CTS}}$ goes high; or a word is transmitted. The transmitted word will not be valid since there can be no start bit if SDO is already low. SDO can be set high without intermediate transitions by transmitting a word consisting of zeros.
7	Transmit Request (TR)	When set high, RTS is set low and data transfer through the transmitter is initiated by the initial THRE interrupt. (When loading the Control Register from the bus, this bit inhibits changing of other control flip-flops.)

D. Peripheral Interface

In addition to serial data in and out, four signals are provided for communication with a peripheral. The Request To Send ($\overline{\text{RTS}}$) output signal alerts the peripheral to get ready to receive data. The Clear To Send (CTS) input signal is the response, signalling that the peripheral is ready. The External Status ($\overline{\text{ES}}$) input latches a peripheral status level, and the Peripheral Status Interrupt ($\overline{\text{PSI}}$) input senses a status change edge (high-to-low) and also generates an interrupt. For example, the modem Data Carrier Detect line could be connected to the $\overline{\text{PSI}}$ input on the UART in order to signal the microprocessor that transmission failed because of loss of the carrier on the communications line. The $\overline{\text{PSI}}$ and $\overline{\text{ES}}$ bits are stored in the Status Register (see below).

Status Register Bit Assignment

Bit	7	6	5	4	3	2	1	0
Signal	THRE	TSRE	PSI	ES	FE	PE	OE	DA
Also Available at Terminal	22*	—	—	—	14	15	15	19*

*Polarity reversed at output terminal.

Bit	Signal	Function
0	Data Available (DA)	When set high, this bit indicates that an entire character has been received and transferred to the Receiver Holding Register. This signal is also available at Term. 19 but with its polarity reversed.
1	Overrun Error (OE)	When set high, this bit indicates that the Data Available bit was not reset before the next character was transferred to the Receiver Holding Register (i.e., the original data was lost). This signal OR'ed with PE is output at Term. 15.
2	Parity Error (PE)	When set high, this bit indicates that the received parity bit does not compare to that programmed by the Even Parity Enable (EPE) control. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal OR'ed with OE is output at Term. 15.
3	Framing Error (FE)	When set high, this bit indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal is also available at Term. 14.
4	External Status (ES)	This bit is set high a low-level input at Term. 38 ($\overline{ES}$).
5	Peripheral Status Interrupt (PSI)	This bit is set high by a high-to-low voltage transition at Term. 37 ($\overline{PSI}$). The Interrupt output (Term. 13) is also asserted ($\overline{INT}$ = low) when this bit is set.
6	Transmitter Shift Register Empty (TSRE)	When set high, this bit indicates that the Transmitter Shift Register has completed serial transmission of a full character including stop bit(s). It remains set until the start of transmission of the next character.
7	Transmitter Holding Register Empty (THRE)	When set high, this bit indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character. Setting this bit also resets the $\overline{THRE}$ output (Term. 22) low and causes an Interrupt ($\overline{INT}$ = low), if TR is high.

INTERRUPT CONDITIONS

SET* ($\overline{INT}$ = LOW)	RESET ($\overline{INT}$ = HIGH)	
CAUSE	**CONDITION**	**TIME**
DA (Receipt of data)	Read of data	TPB leading edge
THRE▲ (Ability to reload)	Read of status or write of character	TPB leading edge
THRE•TSRE (Transmitter done)	Read of status or write of character	TPB leading edge
$\overline{PSI}$ (Negative edge)	Read of status	TPB trailing edge
$\overline{CTS}$ (Positive edge when $\overline{THRE \cdot TSRE}$)	Read of status	TPB leading edge

* Interrupts will occur only after the IE bit in the Control Register has been set
▲THRE will cause an interrupt only after the TR bit in the Control Register has been set.

TABLE 5. INTERRUPT CONDITIONS

SIGNAL DESCRIPTION (1802 Compatible — Mode 1)

Terminal No.	Signal	Function
1	V_{DD}	Positive supply
2	Mode Select (Mode)	A high-level voltage at this input selects the 1802 Mode of operation.
3	V_{SS}	Ground
4	$\overline{\text{Chip Select 2}}$ ($\overline{CS\ 2}$)	A low-level voltage at this input together with CS 1 and CS 3 selects the 1854A UART.
5-12	Receiver Bus (R BUS 0 — R BUS 7)	Receiver parallel data outputs (may be externally connected to corresponding transmitter bus terminals).
13	$\overline{\text{Interrupt}}$ ($\overline{INT}$)	A low-level voltage at this output indicates the presence of one or more of the interrupt conditions listed in Table 5.

14	Framing Error (FE)	A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register.
15	Parity Error or Overrun Error (PE/OE)	A high-level voltage at this output indicates that either the PE or OE bit in the Status Register has been set (see Status Register Bit Assignment).
16	Register Select (RSEL)	This input is used to choose either the Control/Status Registers (high input) or the transmitter/receiver data registers (low intput) according to the truth table 1.
17	Receiver Clock (R Clock)	Clock input with a frequency 16 times the desired receiver shift rate.
18	TPB	A positive input pulse used as a data load or reset strobe.
19	Data Available ($\overline{DA}$)	A low-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.
20	Serial Data In (SDI)	Serial data received on this input line enters the Receiver Shift Register at a point determined by the character length. A high-level input voltage must be present when data is not being received.
21	$\overline{\text{Clear}}$ ($\overline{\text{Clear}}$)	A low-level voltage at this input resets the interrupt flip-flop, Receiver Holding Register, Control Register, and Status Register, and sets Serial Data Out (SDO) high.
22	Transmitter Holding Register Empty ($\overline{THRE}$)	A low-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.
23	Chip Select 1 (CS 1)	A high-level voltage at this input together with $\overline{CS\ 2}$ and CS 3 selects the UART.
24	Request To Send ($\overline{RTS}$)	This output signal tells the peripheral to get ready to receive data. Clear To Send ($\overline{CTS}$) is the response from the peripheral. $\overline{RTS}$ is set to a low-level voltage when data is latched in the Transmitter Holding Register or TR is set high, and is reset high when both the Transmitter Holding Register and Transmitter Shift Register are empty and TR is low.
25	Serial Data Outupt (SDO)	The contents of the Transmitter Shift Register (start bit, data bits, parity bit, and stop bit(s)) are serially shifted out on this output. When no character is being transmitted, a high level is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.
26-33	Transmitter Bus (T BUS 0 — T BUS 7)	Transmitter parallel data inputs. These may be externally connected to corresponding Receiver bus terminals.
34	Read/Write (RD/$\overline{WR}$)	A low-level voltage at this input gates data from the transmitter bus to the Transmitter Holding Register or the Control Register as chosen by register select. A high-level voltage gates data from the Receiver Holding Register or the Status Register, as chosen by register select, to the receiver bus.
35	Chip Select 3 (CS 3)	A high-level voltage at this input with CS 1 and $\overline{CS\ 2}$ selects the UART.
36	No Connection	
37	Peripheral Status Interrupt ($\overline{PSI}$)	A high-to-low transition on this input line sets a bit in the Status Register and causes an Interrupt ($\overline{INT}$ = low).
38	External Status ($\overline{ES}$)	A low-level voltage at this input sets a bit in the Status Register.
39	Clear To Send ($\overline{CTS}$)	When this input from peripheral is high, transfer of a character to the Transmitter Shift Register and shifting of serial data out is inhibited.
40	Transmitter Clock (T Clock)	Clock input with a frequency 16 times the desired transmitter shift rate.

1800 CMOS Microprocessor Family
Multiply/Divide Unit

DESCRIPTION

Hughes' 1855 is an 8 bit mode programmable multiply/divide unit which can be used to greatly increase the capabilities of 8 bit microprocessors. The 1855 interfaces directly to the 1802 microprocessor via the N-lines and can easily be configured to fit in either the memory or I/O space of generalized 8 bit microprocessors. The 1855 performs multiply and divide operations on unsigned, binary operators. It saves considerable memory space and execution time over the same functions as performed by coded multiply and divide software subroutines.

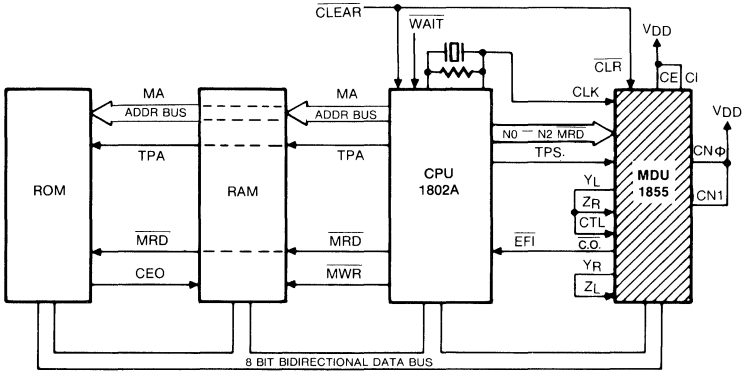
Add and shift right operations and subtract and shift left operations are used for multiply and divide functions respectively. The 1855 is cascadable up to 4 units for 32 x 32 bit multiply or 64 ÷ 32 bit divide functions.

The 1855 operates over a 4-10.5 voltage range while the 1855C operates over a 4-6.5 voltage range. The 1855 is available in a 28 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form are available upon request.

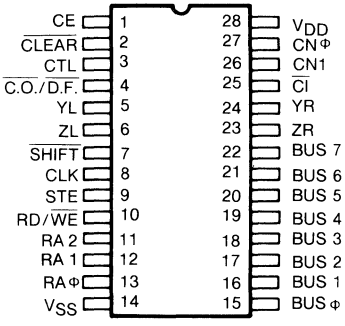
FEATURES

- Static silicon gate CMOS circuitry
- Interfaces directly to 1802A microprocessor without additional components.
- Easy interface to general 8 bit microprocessors.
- Low power dissipation
- Single non-critical voltage supply
- Cascadable up to 4 units for 32 bit by 32 bit multiply or 64 ÷ 32 bit divide
- 8 bit by 8 bit multiply of 16 ÷ 8 bit divide in 5 μs at 5V or 2.5 μs at 10V typical
- Significantly increased throughput of μp used for arithmetic calculations.

SYSTEM INTERCONNECT
Typical 1800 System with 1855



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

DC Supply-Voltage Range, (V_{CC}, V_{DD})
(All Voltage Values referenced to V_{SS} Terminal)
$V_{CC} \leq V_{DD}$:
1855 ..... −0.5 to + 13 Volts
1855C ..... −0.5 to + 7 Volts
Input Voltage Range, all inputs ..... −0.5 to V_{DD} + 0.5 Volts
DC Input Current, any one input ..... ± 10mA
Operating-Temperature Range (T_A)
Plastic Package ..... −40 to + 85°C
Ceramic Package ..... −55 to + 125°C
Storage Temperature Range (T_{stg}) .... −65 to + 150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full Package Range

CHARACTERISTICS	LIMITS				UNITS
	1855		1855C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = − 40 to + 85°.

CHARACTERISTICS	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	1855			1855C			
				Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max	
Quiescent Device	−	0, 5	5	−	0.01	50	−	0.02	200	µA
Current, I_{DD}	−	0, 10	10	−	1	200	−	−	−	
Output Low (Sink)	0.4	0, 5	5	1.6	3.2	−	1.6	3.2	−	mA
Current, I_{OL}	0.5	0, 10	10	2.6	5.2	−	−	−	−	
Output High (Source)	4.6	0, 5	5	1.15	2.3	−	1.15	2.3	−	
Current, I_{OH}	9.5	0, 10	10	2.6	5.2	−	−	−	−	
Output Voltage	−	0, 5	5	−	0	0.1	−	0	0.1	V
Low-Level, V_{OL}[2]	−	0, 10	10	−	0	0.1	−	−	−	
Output Voltage	−	0, 5	5	4.9	5	−	4.9	5	−	
High-level, V_{OH}[2]	−	0, 10	10	9.9	10	−	−	−	−	
Input Low	0.5, 4.5	−	5	−	−	1.5	−	−	1.5	
Voltage, V_{IL}	0.5, 9.5	−	10	−	−	3	−	−	−	
Input High	0.5, 4.5	−	5	−	3.5	−	3.5	−	−	
Voltage, V_{IH}	0.5, 9.5	−	10	−	7	−	−	−	−	
Input Current,	−	0, 5	5	−	$\pm 10^{-4}$	± 1	−	$\pm 10^{-4}$	± 1	µA
I_{IN}	−	0, 10	10	−	$\pm 10^{-4}$	± 1	−	−	−	
3-State Output Leakage	0, 5	0, 5	5	−	−	± 15	−	−	± 15	
Current, I_{OUT}	0, 10	0, 10	10	−	−	± 15	−	−	−	
Operating Current,	−	0, 5	5	−	2	5	−	2	5	mA
I_{DD}[3]	−	0, 10	10	−	4	10	−	−	−	
Input Capacitance, C_{IN}	−	−	−	−	5	7.5	−	5	7.5	pF
Output Capacitance, C_{OUT}	−	−	−	−	10	15	−	−	15	

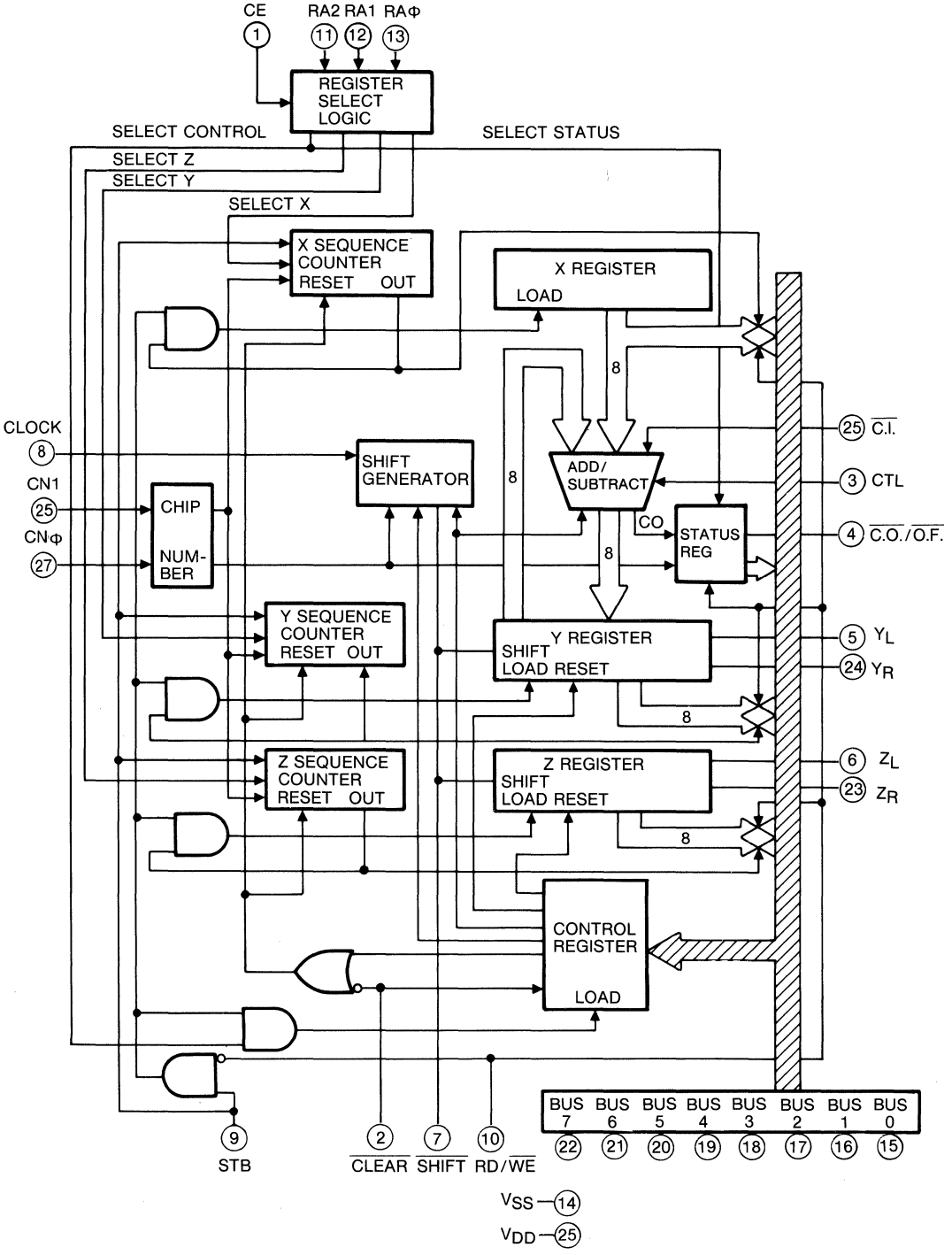
Notes: 1. Typical values are to T_A = + 25°C and nominal voltage.
2. I_{OL} = 1 µA.
3. Operating current measured in a 1802A at 2 MHz with outputs floating.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ± 5% t_r, t_f = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF (See Timing Diagram)

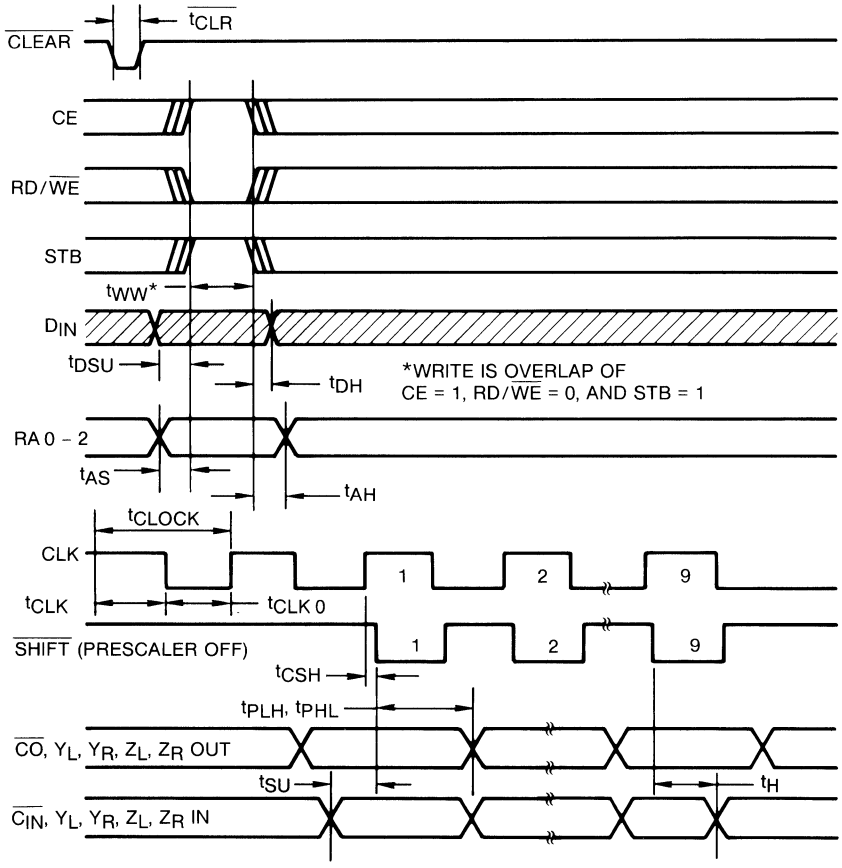
CHARACTERISTICS[1]	SYMBOL	V_{DD} (V)	LIMITS 1855 Min.	1855 Typ.[2]	1855 Max.	1855C Min.	1855C Typ.[2]	1855C Max.	UNITS
WRITE CYCLE									
Minimum Clear Pulse Width	$t_{\overline{CLR}}$	5	–	50	75	–	50	75	ns
		10	–	25	40	–	–	–	
Minimum Write Pulse Width	t_{WW}	5	–	150	225	–	150	225	
		10	–	75	115	–	–	–	
Minimum Data-In Setup	t_{DSU}	5	–	−75	0	–	−75	0	
		10	–	−40	0	–	–	–	
Minimum Data-In Hold	t_{DH}	5	–	50	75	–	50	75	
		10	–	25	40	–	–	–	
Minimum Address to Write Setup	t_{ASU}	5	–	50	75	–	50	75	
		10	–	25	40	–	–	–	
Minimum Address after Write Hold	t_{AH}	5	–	50	75	–	50	75	
		10	–	25	40	–	–	–	
READ CYCLE									
CE to Data Out Active	t_{CDO}	5	–	200	300	–	200	300	ns
		10	–	100	150	–	–	–	
CE to Data Access	t_{CA}	5	–	300	450	–	300	450	
		10	–	150	225	–	–	–	
Address to Data Access	t_{AA}	5	–	300	450	–	300	450	
		10	–	150	225	–	–	–	
Data Out Hold After CE	t_{DOH}	5	50	150	225	50	150	225	
		10	25	75	115	–	–	–	
Data Out Hold After Read	t_{DOH}	5	50	150	225	50	150	225	
		10	25	75	115	–	–	–	
Read to Data Out Active	t_{RDO}	5	–	200	300	–	200	300	
		10	–	100	150	–	–	–	
Read to Data Access	t_{RA}	5	–	200	300	–	200	300	
		10	–	100	150	–	–	–	
Strobe to Data Access	t_{SA}	5	50	200	300	50	200	300	
		10	25	100	150	–	–	–	
Minimum Strobe Width	t_{SW}	5	–	150	225	–	150	225	
		10	–	75	115	–	–	–	
OPERATION TIMING									
Maximum Clock Frequency[3]	t_{CF}	5	3	4	–	3	4	–	MHz
		10	6	8	–	–	–	–	
Maximum Shift Frequency (1 Device)[4]	t_{SF}	5	1.5	2	–	1.5	2	–	
		10	3	4	–	–	–	–	
Minimum Clock Width	t_{CLK0} t_{CLK1}	5	–	100	150	–	100	150	ns
		10	–	50	75	–	–	–	
Minimum Clock Period	t_{CLK}	5	–	250	333	–	250	333	ns
		10	–	125	167	–	–	–	
Clock to Shift Prop. Delay	t_{CSH}	5	–	200	300	–	200	300	
		10	–	100	150	–	–	–	
Minimum C.I. to Shift Setup	t_{SU}	5	–	50	67	–	50	67	
		10	–	25	33	–	–	–	
C.O. from Shift Prog. Delay	t_{PLH} t_{PHL}	5	–	450	600	–	450	600	
		10	–	225	300	–	–	–	
Minimum C.I. from Shift Hold	t_H	5	–	50	75	–	50	75	
		10	–	25	40	–	–	–	
Minimum Register Input Setup	t_{SU}	5	–	−20	10	–	−20	10	
		10	–	−10	10	–	–	–	
Register after Shift Prop. Delay	t_{PLH} t_{PHL}	5	–	400	600	–	400	600	
		10	–	200	300	–	–	–	
Minimum Register after Shift Hold	t_H	5	–	50	100	–	50	100	
		10	–	25	50	–	–	–	
C.O. from C.I. Prop. Delay	t_{PLH} t_{PHL}	5	–	100	150	–	100	150	
		10	–	50	75	–	–	–	
Register from C.I. Prop. Delay	t_{PLH} t_{PHL}	5	–	80	120	–	80	120	
		10	–	40	60	–	–	–	

Notes:
1. Maximum limits of minimum characteristics are the values above which all devices function.
2. Typical values are for T_A = +25°C and nominal voltages.
3. Clock frequency and pulse width are given for systems using the internal clock option of the 1855. Clock frequency equals shift frequency for systems not using the internal clock option.
4. Shift period for cascading of devices is increased by an amount equal to the C.O. to C.I. Prop. Delay for each device added.

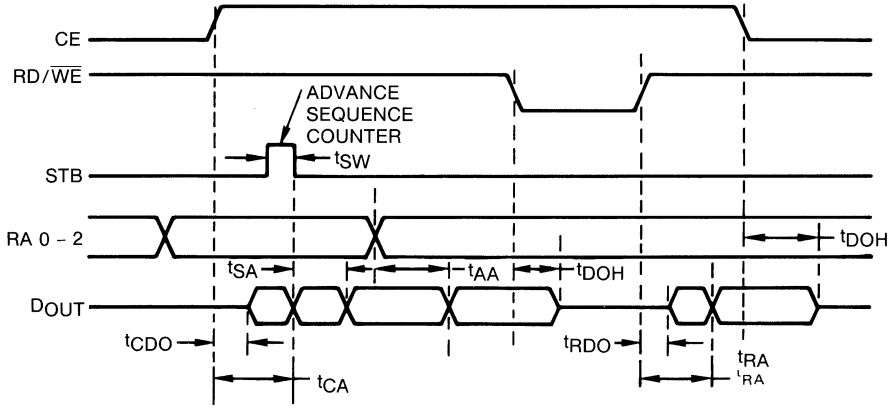
FUNCTIONAL DIAGRAM



Write Timing And Operation Timing



Read Timing



CONTROL TRUTH TABLE

INPUTS*						
CE	RA 2 (N 2)	RA 1 (N 1)	RA 0 (N 0)	RD/WE (MRD)	STB (TPB)	RESPONSE
0	X	X	X	X	X	NO ACTION (BUS FLOATS)
X	0	X	X	X	X	NO ACTION (BUS FLOATS)
1	1	0	0	1	X	X TO BUS } INCREMENT SEQUENCE
1	1	0	1	1	X	Z TO BUS } COUNTER WHEN
1	1	1	0	1	X	Y TO BUS } STB AND RD = 1
1	1	1	1	1	X	STATUS TO BUS
1	1	0	0	0	1	LOAD X FROM BUS } INCREMENT
1	1	0	1	0	1	LOAD Z FROM BUS } SEQUENCE
1	1	1	0	0	1	LOAD Y FROM BUS } COUNTER
1	1	1	1	0	1	LOAD CONTROL REGISTER
1	1	X	X	0	0	NO ACTION (BUS FLOATS)

*( ) = 1800 system signals. 1 = High Level, 0 = Low Level, X = High Level or Low Level

REGISTER BIT ASSIGNMENT CONTROL/REGISTER BIT ASSIGNMENT

BITS							
7	6	5	4	3	2	1	0
SHIFT RATE SELECT	RESET CONT. SEQUENCE COUNTER	NUMBER OF MDU		RESET CONT. Y REG.	RESET CONT. Z REG.	OPERATION	
0 = Clock frequency 1 = Select option*	1 = Reset sequence counters	00 = Four 1855's 01 = Three 1855's 10 = Two 1855's 11 = One 1855		1 = Reset Y register	1 = Reset Z register	00 = No Operation (except reset controls) 01 = Multiply 10 = Divide 11 = Invalid State	

*Select shift rate option:
One 1855 = shift rate = clock frequency ÷ 2
Two 1855's = shift rate = clock frequency ÷ 4
Three or four 1855's = shift rate = clock frequency ÷ 8

STATUS REGISTER BIT ASSIGNMENT

BIT	7	6	5	4	3	2	1	0
Output	0	0	0	0	0	0	0	O.F.

O.F. = 1 if overflow (only valid after a divide has been done).

FUNCTIONAL DESCRIPTION

The 1855 performs an 8N-bit by 8N-bit multiply with a 16N-bit results and 16N bit by 8N-bit divide yielding an 8N-bit result plus an 8 bit remainder. The N represents the number of cascaded 1855s from 1 through 4. All operations require 8N + 1 shift pulses.

The 1855 contains X, Y and Z registers for loading the operands and saving the results, the control register for initializing the multiply or divide operation, and a status register for storing an overflow flag. There are two register address lines (RA 0-RA 1) provided to select the appropriate register for loading or reading. The RD/$\overline{WE}$ and STB lines are used in conjunction with the RA lines to determine the exact MDU response (see Control Truth Table).

When multiple MDUs are cascaded, the loading of each register is done sequentially. The first selection of any register loads the most significant 1855, the second loads the next significant and so on. Registers are also read out sequentially. This is accomplished by internal counters on each 1855 which are decremented by STB during each register selection. When the counter matches the chip number (CN 1, CN 0 lines), the device is selected. These counters must be cleared with a clear pulse on pin 2 or with bit 6 in the control word (See Control Register Bit Assignment Table) in order to start each sequence of accesses with the most significant device.

The 1855 has a built-in clock prescaler which can be selected via bit 7 on the control register. The prescaler may be necessary in cascaded systems operating at high frequencies or in systems where a suitable exact frequency is not available. This need is to provide for propagation delay of the carry output signal. Without the prescaler select, the shift frequency is equal to the clock input frequency. With the prescaler selected, the rate depends on the number of MDUs as defined by bits 4 and 5 of the control word. For one MDU, the clock frequency is divided by two; the two MDUs the clock frequency is divided by four and for three or four MDUs the clock frequency is divided by eight.

OPERATION

A. Initialization and Controls:

The 1855 must be cleared by a low signal input on pin 2 during power on. This prevents bus contention problems at YL, YR and ZL, and ZR terminals. It also resets the sequence counters and shift pulse generator.

Prior to loading any other registers, the control register must be loaded to specify the number of 1855s being cascaded. Once the number of devices has been specified and sequence counters cleared with a clear pulse or bit 6 of the control word, the X, Y and Z registers can be loaded as defined in the control truth table. Registers can be loaded in any sequence. Successive loads to a given register will always proceed sequentially from the most significant byte to the least significant byte as described previously. Resetting the sequence counters selects the most significant MDU. In a four MDU system, loading all MDUs results in the sequence counter pointing to the first MDU again while in all other configurations it must be reset prior to each series or register reads or writes.

OPERATION, cont.

B. Multiply Operation:

(X) x (Z) + (Y) ⇒ (Y) (Z); (X) unchanged

The two numbers to be multiplied are loaded in the X and Z registers. The result will be in the Y and Z register with Y being the more significant half and Z the less significant half. The X register will be unchanged after the operation is completed.

The original contents of Y register are added to the product of X and Z. Bit 3 of the control word will reset register Y to zero if desired.

C. Divide Operation:

$\frac{(Y)\ (Z)}{(X)}$ ⇒ (Z) = quotient, (Y) = remainder; $\overline{C.O.}/\overline{O.F.}$ in status byte.

The divisor is loaded into the X register. The dividend is loaded in the Y and Z registers with the more significant half in the Y register and less significant half in the Z register. The X register will be unaltered by the operation. The quotient will be in the Z register while the remainder will be in the Y register. An overflow will be indicated by the $\overline{C.O.}/\overline{O.F.}$ of the most significant MDU and can also be determined by reading the status byte.

The overflow indicator will be set at the start of the divide operation if the resultant will exceed the size of the Z register (8N-bits).

The Z register can be reset using bit 2 of the control word and another divide can be performed in order to further divide the remainder.

Programming Examples:

Connection to an 1802A Microprocessor in direct I/O mode (N lines connected to R inputs).

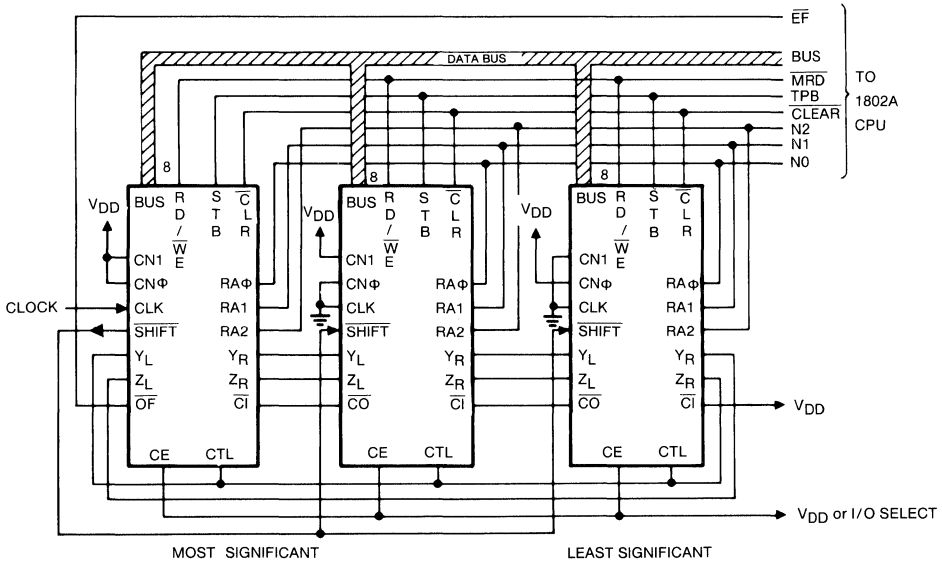
$F\Phi E1_{16}$ X $2D3C_{16}$ Multiply

LDI #ΦΦ PLO R2 LDI #1Φ PHI R2	$R_2 = 1\Phi\Phi\Phi$
OUT 7, #60	Load control word with 2 MDUs and reset/sequence counters.
OUT 4, #FΦ OUT 4, #E1	Load MSB of X reg. Load LSB of X reg. (X) = FΦE1
OUT 5, #2D OUT 5, #3C	Load MSB of Z reg. Load LSB of Z reg. (Z) = 2D3C
OUT 7, #69	Load control word with 2 MDUs, reset y reg and seq counters and do multiply operation
SEX R2	
INP 6; IRX INP 6; IRX INP 5; IRX INP 5; IRX	MSB of results from Y reg. to Location 1ΦΦΦ and 1ΦΦ1 LSB of result from Z reg. to Location 1ΦΦ2 and 1ΦΦ3

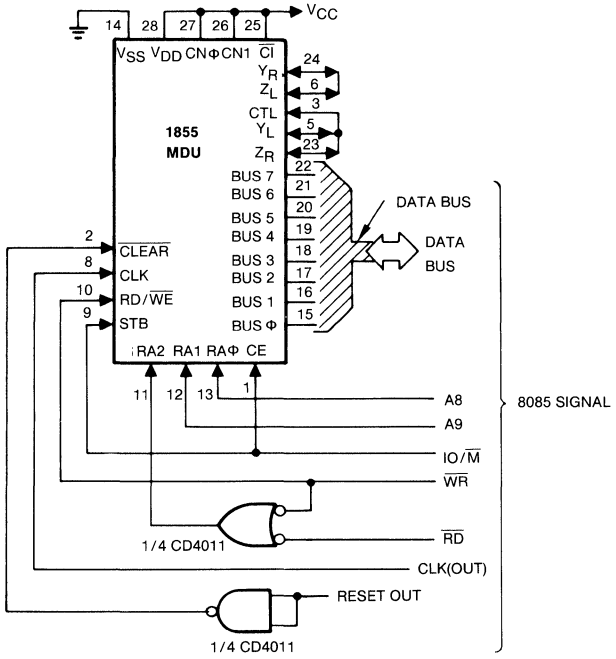
Divide $\frac{B4A59685_{16}}{4F3\Phi_{16}}$

LDI #ΦΦ PLO R2 LDI #2Φ PHI R2	$R_2 = 2\Phi\Phi\Phi$
OUT 7, #60	load control word
OUT 6, #B4 OUT 6, #A5	= Y register (Y) = BYA5
OUT 5, #96 OUT 5, #85	= Z register (Z) = 9685
OUT 4, #4F OUT 4, #30	= X register (X) = 4F3Φ
OUT 7, #6A	Load control word for divide function
SEX R2	
INP 5; IRX	Quotient for z register to mem.
INP 5; IRX	2ΦΦΦ, 2ΦΦ3
INP 6: IRX	Remainder from y register to mem.
INP 6: IRX	2ΦΦ2, 2ΦΦ3

(A) Cascading 3 MDUs in 1802A system with MDU being accessed as an I/O port.



(B) Interfacing the 1855 to 8085 microprocessor as an I/O device.



SIGNAL DESCRIPTION

CE — CHIP ENABLE (Input):

A high on this pin enables the 1855 MDU to respond to the select lines. All cascaded MDUs must be enabled together. CE also controls the three state $\overline{C.O.}/\overline{O.F.}$ output of the most significant MDU.

$\overline{Clear}$ (Input):

The 1855 MDU(s) must be cleared upon power on with a low on this pin. The clear signal resets the sequence counters, the shift pulse generator, and bits 0 and 1 of the control register.

CTL-Control (Input):

This is an input pin. All CTL pins must be wired together and to the Y_L of the most significant 1855 MDU and the Z_R of the least significant 1855 MDU. This signal is used to indicate whether the registers are to be operated on or only shifted.

$\overline{C.O.}/\overline{O.F.}$ — $\overline{Carry\ Out}/\overline{Over\ Flow}$ (Output):

The three state 1855 Carry Out signal is connected to CI (Carry-In) of the next more significant 1855 MDU, except on the most significant MDU. On that MDU it is an overflow indicator and is enabled when a chip enable is true. A low on this pin indicates that an overflow has occurred. The overflow signal is latched each time the control register is loaded, but is only meaningful after a divide command.

Y_L, Y_R — Y-Left, Y-Right:

These are three state bi-directional pins for data transfer between the Y registers of cascaded 1855 MDUs. The Y_R pin in an output and Y_L is an input during a multiply and the reverse is true at all other times. The Y_L pin must be connected to the Y_R pin of the next more significant MDU. An exception is the Y_L pin of the most significant MDU must be connected to the Z_R pin of the least significant MDU and the CTL pins of all MDU's. Also the Y_R pin of the least significant MDU is tied to the Z_L pin of the most significant MDU.

Z_L, Z_R — Z-Left, Z-Right:

These are three state bi-directional pins for data transfers between the Z registers of cascaded MDUs. The Z_R pin is an output and Z_L is an input during a multiply and the reverse is true at all other times. the Z_L pin must be tied to the Y_R pin of the next most significant MDU. An exception is the Z_L pin of the most significant MDU must be connected to the Y_R pin of the lest significant MDU. Also, the Z_R pin of the least significant MDU is tied to the Y_L of the most significant MDU.

$\overline{Shift}$ — $\overline{Shift\ Clock}$:

This is a three state bi-directional pin. It is an output on the most significant MDU and an input on all other MDUs. It provides the MDU system's timing pulses. All $\overline{Shift}$ pins must be connected together for cascaded operation. A maximum of the 8N + 1 shifts are required for an operation where N equals the number of MDU devices cascaded.

Clk — Clock (Input):

This pin should be grounded on all but the most significant MDU. There is an optional reduction of clock frequency available on this pin, if so desired, controlled by bit 7 of the control byte.

Stb — Strobe (Input):

When RD/$\overline{WE}$, low data, is latched from bus lines on the falling edge of this signal, it may be asynchronous to the clock. Strobe also increments the selected register's sequence counter during reads and writes. TPB would be used in 1802A systems.

RD/$\overline{WE}$ — Read/$\overline{Write\ Enable}$ (Input):

This signal defines whether the selected register is to be read from or written to. In the 1802A systems use $\overline{MRD}$ if MDUs are addressed as I/O devices; $\overline{MWR}$ is used if MDUs are addressed as memory devices.

RAΦ, RA 1, RA 2 — Register Address (Input):
These input signals define which register is to be read from or written to. It can be seen in the Control Truth Table that RA 2 can be used as a chip enable. It is identical to the CE pin, except only CE controls the tristate $\overline{C.O.}$ / $\overline{O.F.}$ on the most significant MDU. In the 1802A systems use N lines if MDUs are used as I/O devices; use address lines or function of address lines if MDUs are used as memory devices.

V_{SS} — Ground:
Power supply line.

BUS 0 — BUS 7 — Bus Lines:
Three state bidirectional bus for direct interface with 1802A series and other 8-bit microprocessors.

Z_R — Z-Right:
See signal Z_L

Y_R — Y-Right:
See signal Y_L

$\overline{CI}$-$\overline{Carry\text{-}In}$ (Input):
This is an input for the carry from the next less significant MDU. On the least significant MDU, it must be high (V_{DD}) on all others and connected to the $\overline{CO}$ pin of the next less significant MDU.

CNΦ, CN 1 — Chip Number (Input):
These two input pins are wired high or low to indicate the MDU position in the cascaded chain. Both are high for the most significant MDU regardless of how many 1855 MDUs are used. Then CN 1 = high and CN 0 = low for the next MDU and so forth.

V_{DD} — V+:
Power supply line.

1800 CMOS Microprocessor Family
4-Bit Bus Buffers/Separators

DESCRIPTION

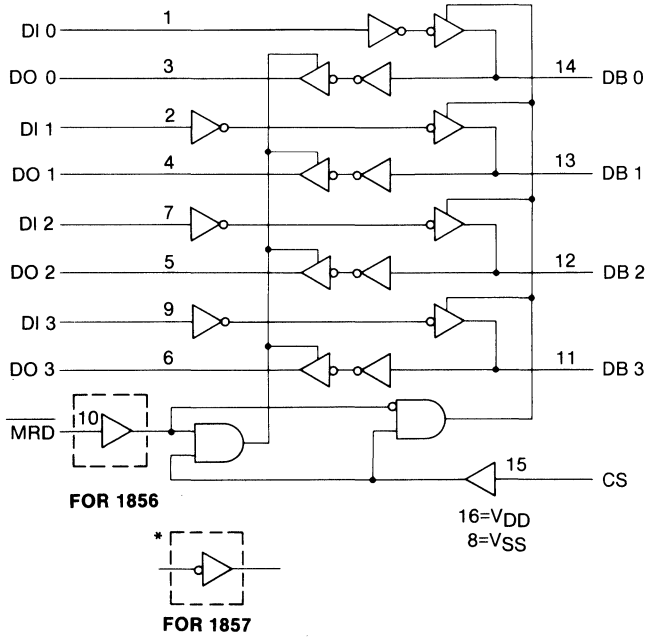
Hughes' 1856 and 1857 are 4-bit bus buffer/separators to allow data to be split from a single bi-directional bus into separate input and output busses. The 1857 is intended for peripheral or I/O bus control while the 1856 is intended for memory bus control. The difference between the two devices is in the polarity of the input buffer for the Memory Read ($\overline{MRD}$) signal. This signal is inverted in the 1857, and enables the $\overline{MRD}$ signal to set the input mode in the 1856 or to set the output mode in the 1857. When $\overline{MRD} = V_{DD}$ the output mode is set in the 1856 and the input mode is set in the 1857.

The 1856 and 1857 operate over a 4-10.5 voltage range while the 1856C and 1857C operate over a 4-6.5 voltage range. The 1856 and 1857 are available in a 16 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

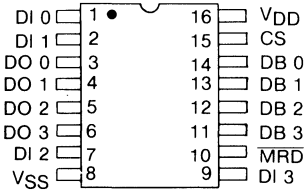
FEATURES

- Static Silicon Gate CMOS Circuitry
- Compatible with 1802A Microprocessor
- Provides easy connection of Memory or I/O Devices to 1802A Microprocessor Bus
- Provides Non-inverted Bi-directional Buffered Data Transfer
- Chip Select for Simple System Expansion
- Low Quiescent and Operating Power

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T_A)
- Ceramic Package ..... −55 to + 125°C
- Plastic Package ..... −40 to + 85°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- 1856/1857 ..... −0.5 to + 11 Volts
- 1856C/1857C ..... −0.5 to + 7 Volts

Storage Temperature Range (T_{stg}) ..... −65 to + 150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full Package Temperature Range

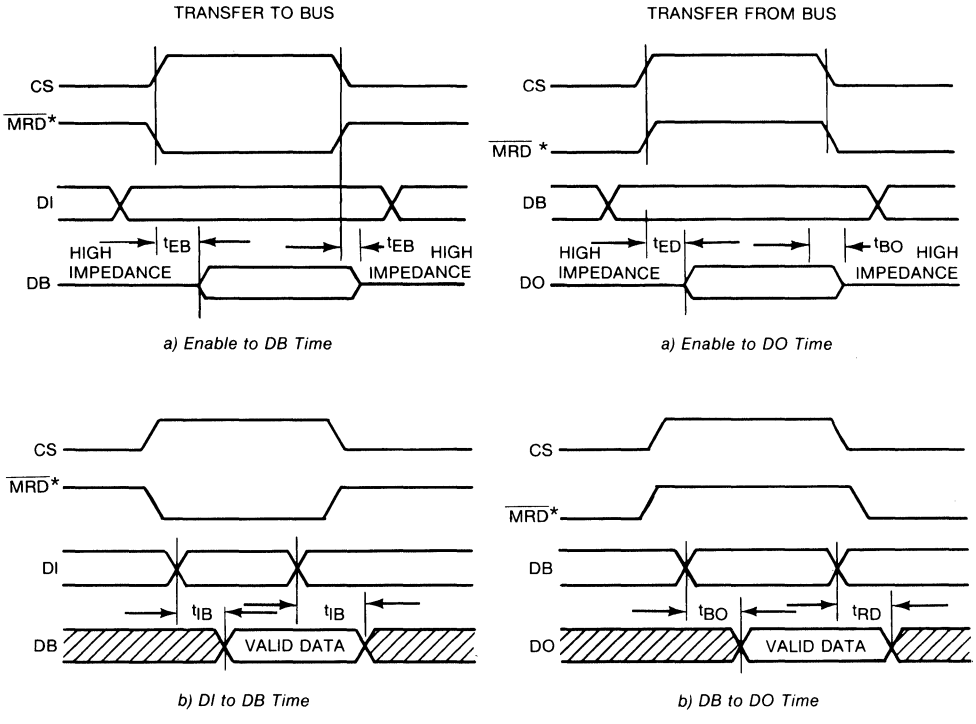
CHARACTERISTICS	CONDITIONS V_{DD} (V)	LIMITS 1856 1857 Min.	LIMITS 1856 1857 Max.	LIMITS 1856C 1856C Min.	LIMITS 1856C 1856C Max.	UNITS
Supply Voltage Range	—	4	10.5	4	6.5	V
Recommended Input Voltage Range	—	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

ELECTRICAL CHARACTERISTICS at T_A = − 40 to + 85°C Unless Otherwise Specified.

CHARACTERISTICS	CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS 1856 1857 Min.	LIMITS 1856 1857 Typ.*	LIMITS 1856 1857 Max.	LIMITS 1856C 1857C Min.	LIMITS 1856C 1857C Typ.*	LIMITS 1856C 1857C Max.	UNITS
Static Electrical Characteristics at T_A = −40°C to +85°C Unless Otherwise Specified										
Quiescent Device Current, I_L	—	—	5	—	1	10	—	5	50	µA
	—	—	10	—	10	100	—	—	—	
Output Low Drive (Sink) Current, I_{OL}	0.4	0, 5	5	1.6	3.2	—	1.6	3.2	—	mA
	0.5	0, 10	10	2.6	5.2	—	—	—	—	
Output High Drive (Source) Current I_{OH}	4.6	0, 5	5	−1.15	−2.3	—	−1.15	−2.3	—	mA
	9.5	0, 10	10	−2.6	−5.2	—	—	—	—	
Output Voltage Low Level V_{OL}[1]	—	0, 5	5	—	0	0.1	—	0	0.1	V
	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High Level, V_{OH}	—	0, 5	5	4.95	5	—	4.95	5	—	
	—	0, 10	10	9.95	10	—	—	—	—	
Input Low Voltage V_{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	V
	0.5, 9.5	—	10	—	—	3	—	—	—	
Input High Voltage V_{IH}	0.5, 9.5	—	5	3.5	—	—	3.5	—	—	
	0.5, 9.5	—	10	7	—	—	—	—	—	
Input Leakage Current, I_{IN}	Any Input	0, 5	5	—	—	±1	—	—	±1	µA
		0, 10	10	—	—	±1	—	—	—	
Operating Current I_{DD}[2]	0, 5	0, 5	5	—	50	100	—	50	100	µA
	0, 10	0, 10	10	—	150	300	—	—	—	
Input Capacitance, C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT}	—	—	—	—	10	15	—	10	15	pF
Dynamic Electrical Charactistics at T_A = −40 to + 85°C, t_r, t_f = 20 ns C_L = 100pF V_{DD} ±5%, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}										
Propogation Delay Time:	—	—	5	—	150	225	—	150	225	ns
$\overline{MRD}$ or CS to DO, t_{ED}	—	—	10	—	75	125	—	—	—	
$\overline{MRD}$ or CS to DB,	—	—	5	—	150	225	—	150	225	ns
t_{EB}	—	—	10	—	75	125	—	—	—	
DI to DB,	—	—	5	—	100	150	—	100	—	ns
t_{IB}	—	—	10	—	50	75	—	—	—	
DB to DO,	—	—	5	—	100	150	—	100	150	ns
t_{DB}	—	—	10	—	50	75	—	—	—	

*Typical values are for T_A = +25°C and nominal voltage.

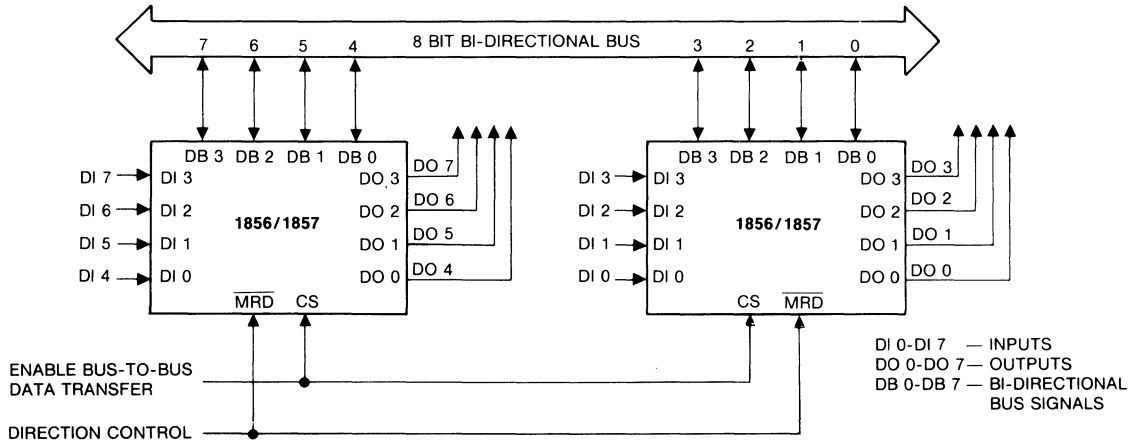
NOTE 1: I_{OL} = I_{OH} = 1 µA.
NOTE 2: Operating current measured in a 1802A at 2MHz with outputs floating.



NOTE: ALL TIMES MEASURED FROM 50% POINT TO 50% POINT OF SIGNAL
*POLARITIES ARE REVERSED FOR 1857

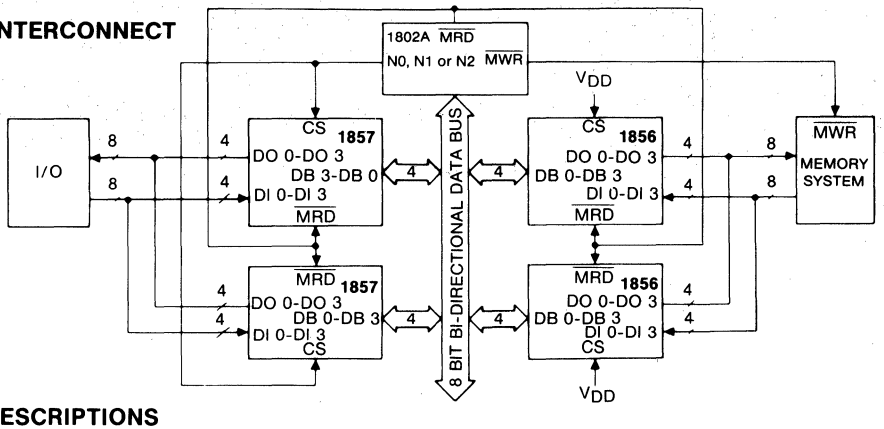
INVALID OR DON'T CARE CONDITION

APPLICATION



The Figure shows how two 1856 or two 1857 can be used as bus buffers or separators between an 8 Bit Bi-directional Data bus and memories or between an 8 Bit Bi-directional Data bus and I/O devices. The chip select input signal enables the bus separator three-state output drivers. The direction of data flow, when enabled, is controlled by the state of the $\overline{MRD}$ input signal.

SYSTEM INTERCONNECT



SIGNAL DESCRIPTIONS

DB 0-DB 3: These four bi-directional signals can be used as data outputs or receiver inputs depending on the logic polarity of the $\overline{MRD}$ input signal. Data is non-inverted.

DI 0-DI 3: The four data inputs. They are enabled onto the corresponding DB lines when Chip Select (CS) and the Memory Read ($\overline{MRD}$) signals are activated.

DO 0-DO 3: The four receiver outputs reflect the data on the DB lines when the Chip Select and Memory Read signals are activated.

CS: The Chip Select signal along with $\overline{MRD}$ controls the activation of the 1856 and 1857 as indicated in the table below. CS is active when it is a logic high (V_{DD}).

$\overline{MRD}$: The Memory Read signal controls the direction of data flow when Chip Select is enabled. In the 1856, when $\overline{MRD}$ = 0, it enables the three state bus drivers (DB 0-DB 3), and outputs data from the driver inputs (DI 0-DI 3) to the data bus. When $\overline{MRD}$ = 1, it disables the three-state bus drivers and enables the three-state data output drivers (DO 0-DO 3), transferring data from the data bus to the data outputs.

In the 1857, when $\overline{MRD}$ = 1 it enables the three-state bus drivers (DB 0-DB 3) and transfers data from the driver inputs (DI 0-DI 3) onto the data bus. When $\overline{MRD}$ = 0, it disables the three-state bus drivers (DB 0-DB 3) and enables the three-state data output drivers (DO 0-DB 3), transferring data bus to the data outputs.

1856 FUNCTION TABLE
For Memory Data Bus Separator Operation

CS	$\overline{MRD}$	DATA BUS OUT DB 0-DB 3	DATA OUT DO 0-DO 3
O	X	HIGH IMPEDANCE	HIGH IMPEDANCE
1	0	DATA IN	HIGH IMPEDANCE
1	1	HIGH IMPEDANCE	DATA BUS

1857 FUNCTION TABLE
For I/O Bus Separator Operation

CS	$\overline{MRD}$	DATA BUS OUT DB 0-DB 3	DATA OUT DO 0-DO 3
O	X	HIGH IMPEDANCE	HIGH IMPEDANCE
1	0	HIGH IMPEDANCE	DATA BUS
1	1	DATA IN	HIGH IMPEDANCE

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Printed in U.S.A. 9/83
Supersedes Previous Data

1800 CMOS Microprocessor Family
4-Bit Memory Latch/Decoder

DESCRIPTION

Hughes' 1858 and 1859 are 4-bit memory address latch/decoders which control 4K bytes of memory. The 1858 provides chip select outputs to control up to 32 H1822 (organized 256 x 4) RAMs. The 1859 provides chip select outputs to control RAMs organized 1024 x 1. The Enable input allows expansion of memory systems beyond 4K bytes of memory. The chip select outputs are a function of the memory address bits connected to the MA 0-MA 3 lines.

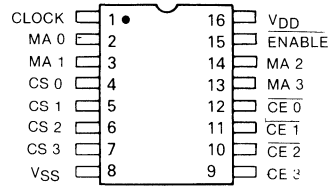
The 1858 and 1859 operate over a 4-10.5 voltage range while the 1858C and 1859C operate over a 4-6.5 voltage range. The 1858 and 1859 are available in a 16 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix), or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

FEATURES

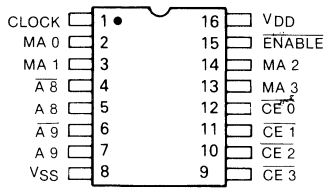
- Static Silicon Gate CMOS Circuitry
- Interfaces Directly with 1802A Microprocessor
- Chip Enable pin allows easy expansion above 4K Bytes of Memory
- Low Quiescent and Operating Power
- Allows direct control of 4K bytes of memory
- 1858 is designed for 256 x 4 Memory Configuration
- 1859 is designed for 1024 x 1 Memory Configuration

PIN CONFIGURATION

1858

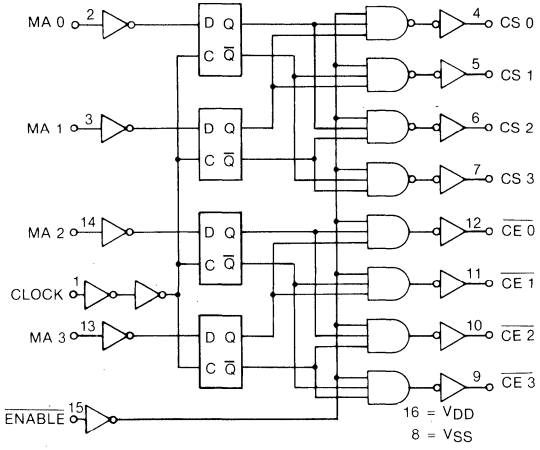


1859

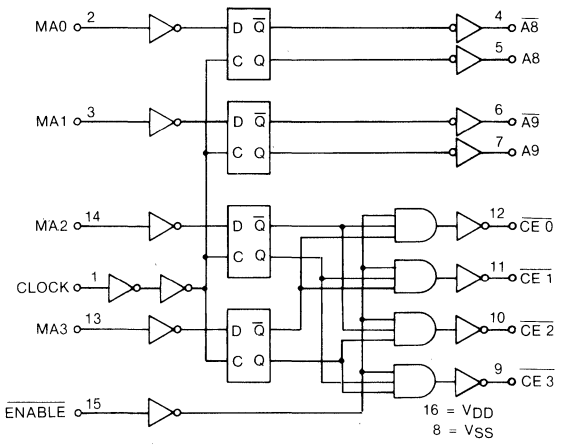


FUNCTIONAL DIAGRAM

1858



1859



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T_A)
- Ceramic Package . . . . . −55 to + 125°C
- Plastic Package . . . . . −40 to + 85°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- 1858/1859 . . . . . −0.5 to + 13V
- 1858C/1859C . . . . . −0.5 to + 7V

Storage Temperature Range (T_{stg}) . . . . . −65 to + 150°C

NOTE: Operating the device above the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full Package Temperature Range

CHARACTERISTICS	CONDITIONS			LIMITS						UNITS
				1858 1859			1858C 1859C			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Supply Voltage Range	–	–	–	4	–	10.5	4	–	6.5	V
Recommended Input Voltage Range	–	–	–	V_{SS}	–	V_{DD}	V_{SS}	–	V_{DD}	V
Minimum Clock Pulse Width, t_W[1]	–	–	5	–	50	75	–	50	75	ns
	–	–	10	–	25	40	–	–	–	
Minimum Data Setup Time, t_{DS}[1]	–	–	5	–	25	40	–	25	40	ns
	–	–	10	–	10	25	–	–	–	
Minimum Data Hold Time, T_{DH}[1]	–	–	5	–	0	25	–	0	25	ns
	–	–	10	–	0	10	–	–	–	
Static Electrical Characteristics at T_A = −40°C to + 85°C Unless Otherwise Specified										
Quiescent Device Current, I_L	–	0, 5	5	–	0.1	10	–	5	50	µA
	–	0, 10	10	–	1	100	–	–	–	
Output Low Drive (Sink) Current, I_{OL}	0.4	0, 5	5	1.6	3.2	–	1.6	3.2	–	mA
	0.5	0, 10	10	2.6	5.2	–	–	–	–	
Output High Drive (Source) Current, I_{OH}	4.6	0, 5	5	−1.15	−2.3	–	−1.15	−2.3	–	mA
	9.5	0, 10	10	−2.6	−5.2	–	–	–	–	
Output Voltage Low Level, V_{OL}[2]	–	0, 5	5	–	0	0.1	–	0	0.1	V
	–	0, 10	10	–	0	0.1	–	–	–	
Output Voltage High Level, V_{OH}	–	0, 5	5	4.9	5	–	4.9	5	–	
	–	0, 10	10	9.9	10	–	–	–	–	
Input Low Voltage, V_{IL}	0.5, 4.5	–	5	–	–	1.5	–	–	1.5	V
	0.5, 9.5	–	10	–	–	3	–	–	–	
Input High Voltage, V_{IH}	0.5, 9.5	–	5	3.5	–	–	3.5	–	–	
	0.5, 9.5	–	10	7	–	–	–	–	–	
Input Leakage Current, I_{IN}	Any Input	0, 5	5	–	10^{-4}	±1	–	10^{-4}	±1	µA
		0, 10	10	–	10^{-4}	±2	–	–	–	
Operating Current, I_{DD}[3]	–	0, 5	5	–	50	100	–	50	100	µA
	–	0, 10	10	–	150	300	–	–	–	
Input Capacitance, C_{IN}	–	–	–	–	5	7.5	–	5	7.5	pF
Output Capacitance, C_{OUT}	–	–	–	–	10	15	–	–	–	–

*Typical values are for T_A = 25°C and nominal voltage

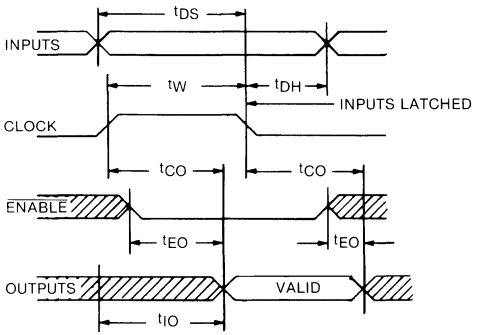
Note 1: Maximum limits of minimum characteristics are the values above which all devices function.
Note 2: I_{OL} = I_{OH} = 1µA.
Note 3: Measured in an 1802 system at 2 MHz with open outputs.

OPERATING CONDITIONS, cont.

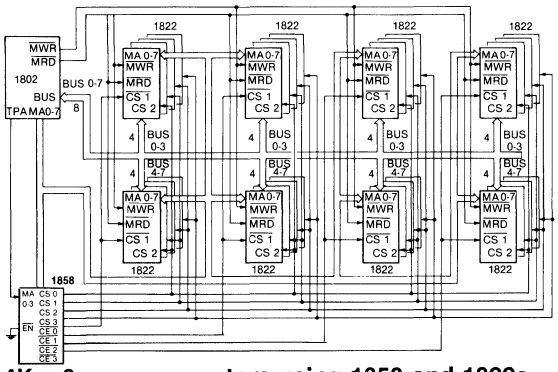
CHARACTERISTICS	CONDITIONS			LIMITS						UNITS
				1858 1859			1858C 1859C			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Dynamic Electrical Characteristics at T_A = −40 to + 85°C, t_r, t_f = 20 ns, C_L = 100pF, V_{DD} ± 5%, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}										
Propogation Delay Times: Clock (Low-to-High) to Any Output, t_{CO}		$\overline{\text{Enable}}$ = 0	5	–	150	225	–	150	225	ns
			10	–	75	125	–	–	–	
$\overline{\text{Enable}}$ to Any Output, t_{EO}		Clock = 1	5	–	125	200	–	125	200	ns
			10	–	65	100	–	–	–	
Memory Address to All Outputs, t_{IO}		Clock = 1 $\overline{\text{Enable}}$ = 0	5	–	150	225	–	150	225	ns
			10	–	75	125	–	–	–	
Propogation Delay Times: Clock (Low-to-high) to A8, A9, $\overline{A8}$, or $\overline{A9}$, t_{CO}			5	–	125	200	–	125	200	ns
			10	–	65	100	–	–	–	
Clock (Low-to-High) to $\overline{CE0}$, $\overline{CE1}$, $\overline{CE2}$, or $\overline{CE3}$, t_{CO}		$\overline{\text{Enable}}$ = 0	5	–	175	275	–	175	275	ns
			10	–	90	140	–	–	–	
Enable to $\overline{CE0}$, $\overline{CE1}$, $\overline{CE2}$, or $\overline{CE3}$, t_{EO}			5	–	125	200	–	125	200	ns
			10	–	65	100	–	–	–	
MA0, MA1 to A8, A9, $\overline{A8}$, or $\overline{A9}$, t_{IO}			5	–	100	150	–	100	150	ns
			10	–	50	75	–	–	–	
MA2, MA3 to $\overline{CE0}$, $\overline{CE1}$, $\overline{CE2}$, or $\overline{CE3}$, t_{IO}		Clock = 1 $\overline{\text{Enable}}$ = 0	5	–	150	225	–	150	225	ns
			10	–	75	125	–	–	–	

*Typical values are for T_A = 25°C and nominal voltage

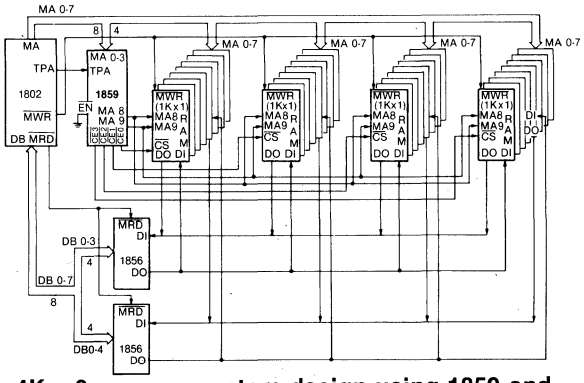
TIMING DIAGRAMS



APPLICATIONS



4K x 8 memory system using 1858 and 1822s



4K x 8 memory system design using 1859 and 1K x 1 RAMs

SIGNAL DESCRIPTION

MA 0 – MA 3: 4 Bit Address inputs. MA 0 is the least significant input address bit and MA 3 is the most significant input address bit.

CLOCK: The MA 0 – MA 3 address bits are latched at the high to low transition of Clock input (TPA) in the 1858 and the 1859.

The 1858 and the 1859 can also be used in general purpose memory system application with a non-multiplexed address bus by connecting the Clock input to V_{DD}.

$\overline{\text{ENABLE}}$: In the 1858, when $\overline{\text{Enable}}$ = V_{DD}, the CS outputs = V_{SS} and the $\overline{CE}$ outputs = V_{DD}. When $\overline{\text{Enable}}$ = V_{SS}, the outputs are enabled and correspond to the binary decode of the inputs. The $\overline{\text{Enable}}$ input can be used for memory system expansion.

In the 1859, when $\overline{\text{Enable}}$ = V_{DD}, the $\overline{CE}$ outputs = V_{DD}; when $\overline{\text{Enable}}$ = V_{SS}, $\overline{CE}$ outputs are enabled and correspond to the binary decode of the MA 3 and MA 2 inputs. Enable does not affect the latching or state of outputs A 8, $\overline{A\ 8}$, A 9, or $\overline{A\ 9}$.

A 8, $\overline{\text{A 8}}$, A 9, $\overline{\text{A 9}}$: These outputs represent the non-inverted and inverted state of the latched address inputs, MA0 and MA1, in the 1859.

$\overline{\text{CE 0}}$ – $\overline{\text{CE 3}}$, CS 0 – CS 3: Decoded outputs. The decoding is shown in the truth tables below.

TRUTH TABLES

1858 DECODE TRUTH TABLE

$\overline{\text{ENABLE}}$	DATA INPUTS		CS0	CS1	CS2	CS3	$\overline{CE0}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$
	MA1	MA0								
0	0	0	1	0	0	0	NOT AFFECTED BY MA1, MA0			
0	0	1	0	1	0	0				
0	1	0	0	0	1	0				
0	1	1	0	0	0	1				
	MA3	MA2								
0	0	0	NOT AFFECTED BY MA3, MA2				0	1	1	1
0	0	1					1	0	1	1
0	1	0					1	1	0	1
0	1	1					1	1	1	0
1	X	X	0	0	0	0	1	1	1	1

X = MA0, MA1, MA2, MA3 DON'T CARE

1859 DECODE TRUTH TABLE

$\overline{\text{ENABLE}}$	DATA INPUTS		A8	A9	$\overline{A8}$	$\overline{A9}$	$\overline{CE0}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$
	MA1	MA0								
0	0	0	0	0	1	1	NOT AFFECTED BY MA1, MA0			
0	0	1	0	1	1	0				
0	1	0	1	0	0	1				
0	1	1	1	1	0	0				
	MA3	MA2								
0	0	0	NOT AFFECTED BY MA3, MA2				0	1	1	1
0	0	1					1	0	1	1
0	1	0					1	1	0	1
0	1	1					1	1	1	0
1	X	X	NOT AFFECTED BY ENABLE				1	1	1	1

X = MA0, MA1, MA2, MA3 DON'T CARE

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Printed in U.S.A.
Rev. N/C 6/83
Supersedes Previous Data

Datasheets are available from Hughes Representatives or Hughes Solid State Products.

HCTR 0107P	Counter/Latch/Decoder/Driver
HCTR 0200P	Decade Counter/Latch/Decoder/Driver
HCTR 0320AP	Frequency Synthesizer
HCTR 4010P	4 Decade Up/Down Counter
HCTR 6010	4½ Decade Counter
HDGP 1000	General Purpose PMOS Fet
HDIG 1030	Insulated Gate PMOS Fet
HLSS 0533Y	Single Chip, Heart Rate Monitor

For technical information on Hughes Quad Logic® Arrays, see pages 13-17.

FEATURES

- Standard Process is MIL. STD. 883B
- High Performance 3μ HCMOS Silicon Gate Technology
- TTL and CMOS I/O Compatability
- Output Buffer Options Provide Drive Currents of up to 16 mA
- Up to 172 I/O Buffers Available
- P Channel and N Channel Sizes for Symmetrical Switching ($W_p = 2W_n$)
- Extensive Macro Library Available
- Two Levels of Metal Interconnection
- Propagation Delays of 1.4 Nanoseconds and Data Rates up to 35 MHz

Military CMOS EEPROM 1024X8

DESCRIPTION

Hughes' HB 3108 is a 1K x 8 (8192 bits) CMOS Electrically Erasable Programmable Read Only Memory (E^2PROM), tested in accordance with Military Standard 883B requirements. As such, it is intended for military or other applications which require superior performance and reliability over the wide temperature range of -55°C to +125°C.

Thorough testing screens ensure a high reliability device, allowing for over 10,000 erase/write cycles and greater than 10 years data retention and unlimited read cycles. The chip erase time and byte write times of 1 ms combine for a fast entire chip program time of about 1 sec. Both chip erase and byte write are controlled with TTL level pulses when V_{DD} is elevated to +16 Volts. A 3-line control architecture providing Chip Select (CS), Chip Enable ($\overline{CE}$), and Output Enable ($\overline{OE}$) allows for maximum flexibility in system implementation. The Hughes' CMOS process provides the advantages of low power to the EEPROM user with a typical quiescent current of 2 μa.

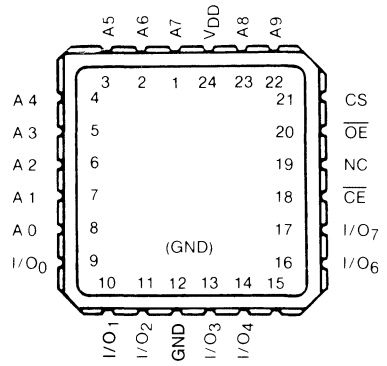
The HB 3108 is available in a 24 lead hermetic dual-in-line ceramic package (D suffix) or leadless chip carrier (L suffix).

FEATURES

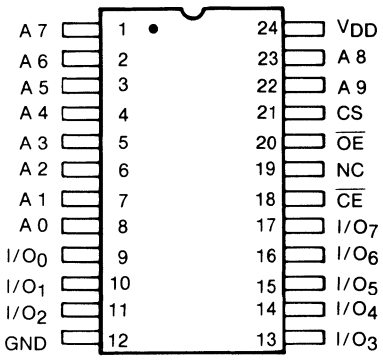
- 1K x 8 CMOS EEPROM
- TTL Level Erase/Byte Write Controls
- 1 ms Erase/Write Times
- 10,000 Erase/Write Cycles
- 10 year Data Retention
- 3-Line Control Architecture
- 10 μW Typical Quiescent Power Dissipation
- JEDEC Approved 24 pin DIP and LCC Pinouts

PIN CONFIGURATION

Leadless Chip Carrier



Ceramic Dip



ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage Range ..... −0.3 to + 18 Volts
(All Voltages referenced to GND terminal)
Input Voltage Range ..... −0.3 to V_{DD} + 0.3 Volts
Operating Temperature Range
Ceramic Package ..... −55 to + 125°C
Storage Temperature Range ..... −65 to + 150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	Read Mode	Write or Erase Mode
V_{DD} Supply Voltage	5 ± 1 Volts	16 ± 1 Volts
Temperature Range	−55°C to + 125°C	−55°C to + 125°C

DC OPERATING CHARACTERISTICS

Read: V_{DD} = 6V Unless Otherwise Specified

SYMBOL	PARAMETER	T_A = −55°C		T_A = +25°C		T_A = +125°C		UNITS	TEST CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
I_{CC1}	Standby Current	—	100	—	100	—	200	µA	V_{IN} = 0 or V_{DD}
I_{CC1A}	Active Current[1]	—	100	—	100	—	200	µA	$\overline{CE}$ = $\overline{OE}$ = 0
V_{OL}	Output Low Voltage	—	0.45	—	0.45	—	0.45	V	V_{DD} = 4.75V, I_O = 2.1mA
V_{OH}	Output High Voltage	2.4	—	2.4	—	2.4	—	V	V_{DD} = 4.75V, I_O = −400µA
V_{IL}	Input Low Voltage	—	0.6	—	0.6	—	0.6	V	V_{DD} = 4.75V
V_{IH}	Input High Voltage	2.4	—	2.4	—	2.4	—	V	V_{DD} = 5.25V
I_{LI}	Input Leakage Current[1]	—	±1	—	±1	—	±1	µA	V_{IN} = 0 or V_{DD}
I_{LO}	Output Leakage Current[1]	—	±1	—	±1	—	±1	µA	V_O = 0 or V_{DD}

Erase or Write: V_{DD} = 17V Unless Otherwise Specified

SYMBOL	PARAMETER	T_A = −55°C		T_A = +25°C		T_A = +125°C		UNITS	TEST CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
I_{CC2}	Prog. Current	—	3	—	3	—	5	mA	V_{IN} = 0 or V_{DD}
I_{CC2A}	Prog. Current	—	25	—	25	—	30	mA	V_{IN} = 5V
V_{IL}	Input Low Voltage	—	0.6	—	0.6	—	0.6	V	—
V_{IH}	Input High Voltage	3.8	—	3.8	—	3.8	—	V	—
I_{LI}	Input Leakage Current[1]	—	±1	—	±1	—	±1	µA	V_{IN} = 0 or V_{DD}
I_{LO}	Output Leakage Current[1]	—	±1	—	±1	—	±1	µA	V_O = 0 or V_{DD}

AC OPERATING CHARACTERISTICS

Read: V_{DD} = 5V Unless Otherwise Specified

SYMBOL	PARAMETER	T_A = −55°C		T_A = +25°C		T_A = +125°C		UNITS	TEST CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{ASU}	Address Set Up Time	75	—	75	—	75	—	ns	CS = V_H
t_{AH}	Address Hold Time	130	—	150	—	200	—	ns	CS = V_H
t_{ACE}	Access Time from $\overline{CE}$	—	550	—	700	—	925	ns	CS = V_H, $\overline{OE}$ = V_L
$t_{\overline{OE}}$	Output Enable Time	—	275	—	325	—	475	ns	CS = V_H, $\overline{CE}$ = V_L
t_{ACS}	Access Time from CS	—	550	—	700	—	925	ns	$\overline{CE}$ = V_L, $\overline{OE}$ = V_L
t_{DF}	$\overline{OE}$ to High Impedence	—	340	—	400	—	520	ns	$\overline{CE}$ = V_L, CS = V_H
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$, or CS which ever occurs first	0	—	0	—	0	—	ns	—
t_{CEH}	$\overline{CE}$ High Time	0.9	—	1.1	—	1.4	—	µs	—
I_{CC3}	Dynamic Current	—	1.0	—	1.0	—	1.2	mA	f = 100KHz

READ TEST CONDITIONS

Output Load: C_L = 50pF
Input Levels: V_H = 2.4 Volts, V_L = 0.45 Volts
Timing Measurement Reference Levels: Input = Output = 50%
Input Rise and Fall Times: $t_r = t_f$ = 10ns

Erase and Write, V_{DD} = 16V Unless Otherwise Specified

SYMBOL	PARAMETER	T_A = −55°C		T_A = +25°C		T_A = +125°C		UNITS	TEST CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{VPS}	Program Set Up Time[1]	5	—	5	—	5	—	µs	—
t_{EP}	Erase Pulse Width[2]	1	10	1	10	1	10	ms	CS = V_H, $\overline{CE}$ = V_H
t_{WP}	Write Pulse Width[2]	1	10	1	10	1	10	ms	CS = V_H, $\overline{OE}$ = V_H
t_{DS}	Data Set Up Time[1]	170	—	200	—	260	—	ns	CS = V_H, $\overline{OE}$ = V_H
t_{DH}	Data Hold Time[1]	170	—	200	—	260	—	ns	CS = V_H, $\overline{OE}$ = V_H
t_{ASP}	Address Set Up Time[1]	170	—	200	—	260	—	ns	CS = V_H
t_{AHP}	Address Hold Time[1]	170	—	200	—	260	—	ns	CS = V_H

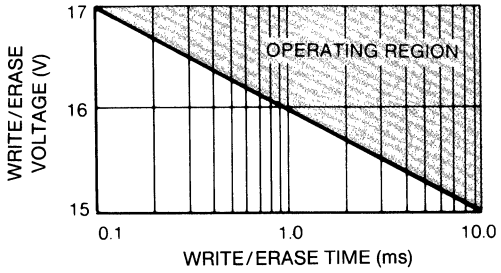
PROGRAMMING TEST CONDITIONS

Input Levels: V_H = 3.8 Volts, V_L = 0.6 Volts
Timing Measurement Reference Levels: Input = Output = 50%
Input Rise and Fall Times: $t_r = t_f$ = 10ns

NONVOLATILE CHARACTERISTICS

SYMBOL	PARAMETER	25°C	0°C to +70°C		-40 to + 85°C		UNITS	TEST CONDITIONS
		TYPICAL[1]	MIN.	MAX.	MIN.	MAX.		
E	Endurance[1,3]	100,000	10,000	—	10,000	—	Cycles/Byte	V_{DD} = 16V $t_{EP} = t_{WP}$ = 1 ms
T_R	Retention [1,4]	—	10	—	10	—	Years	V_{DD} = 0

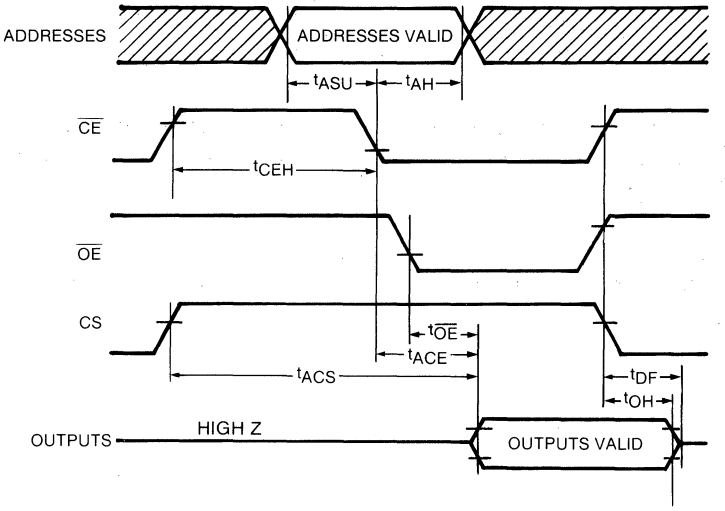
PROGRAM CHARACTERISTICS VS. SUPPLY VOLTAGE



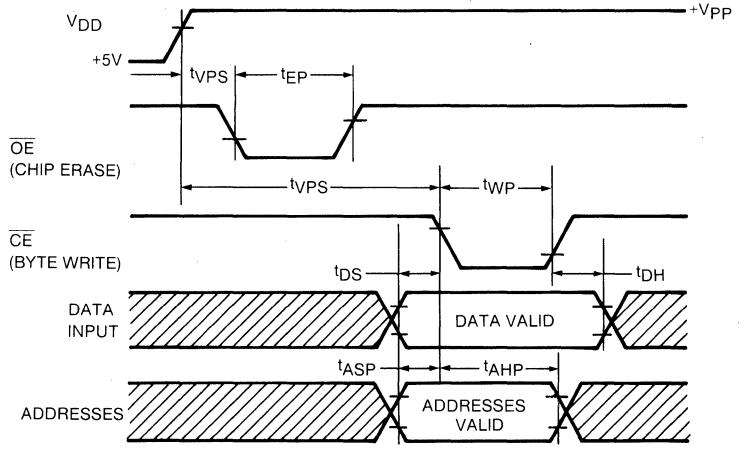
NOTES:
1. This parameter is only sampled and is not 100% tested.
2. Erase and Write time is a function of +Vpp. See characteristic curve.
3. Endurance is the maximum number of erase/write cycles per byte.
4. Retention is the amount of time the data is retained in the memory without power being supplied.

TIMING WAVEFORMS

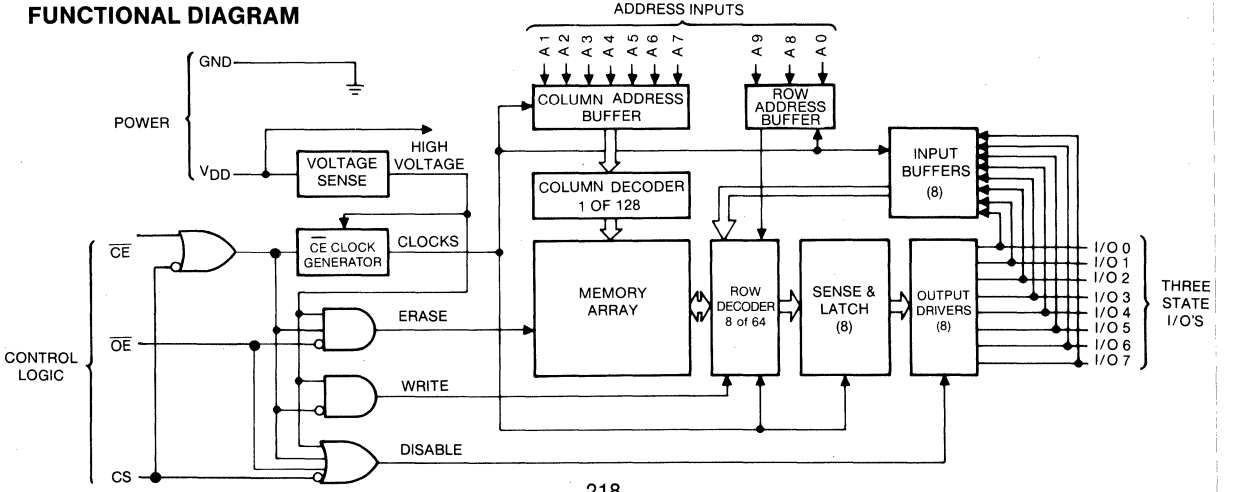
Read



Chip Erase/Byte Write (CS = V_H)



FUNCTIONAL DIAGRAM



HUGHES MILITARY PROGRAM

HB 3108

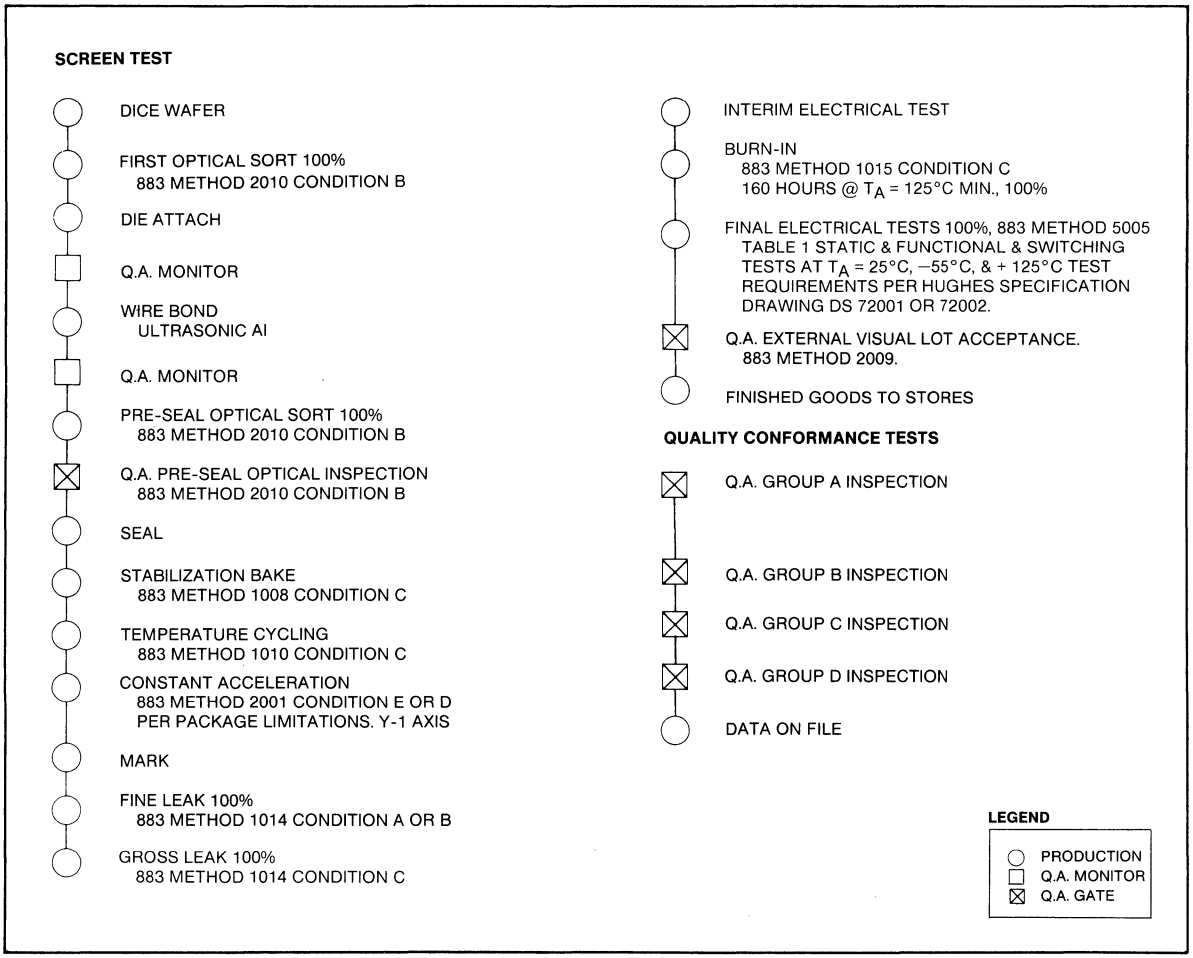
The Hughes' Military Program was developed to provide Mil. Std. 883B processing of memory products. This includes screening to Class B of Method 5004 and quality conformance to Method 5005.

Mil. Std. 883B, Method 5004, Class B, defines the procedures for total lot screening of the HB 3108 over the full temperature range defined as: −55°C to + 125°C.

Mil. Std. 883B, Method 5005, Class B, defines the quality conformance inspections and tests required to ensure that each lot consistently meets specified quality and reliability levels. Method 5005 consists of Group A (electrical tests), Group B (package integrity tests), Group C (life tests), and Group D (package integrity tests) lot inspection procedures.

The Hughes' HB 3108 product flow is illustrated below. Details of the Class B screening tests and quality conformance testing for the HB 3108 are found in Hughes Specification Control Documents.

HB 3108 PRODUCT FLOW SCREEN TESTS



OPERATING MODES

The HB 3108 has three modes of operation: Read, Block Erase and Byte Write, all enabled when the chip is selected (CS = high). In the Read Mode the HB 3108 functions as a normal CMOS ROM. When the power input (V_{DD}) is raised to + V_{PP} the Erase or Write Mode is enabled. In the Erase Mode, all bytes are reset to a logic low (GND). In the Write Mode, bits of the addressed byte may be programmed to a logic high. An Erase Operation is required before re-writing over previously Programmed data. Detailed procedures for each mode follow:

READ MODE: The circuit reads addresses on the falling edge of $\overline{CE}$ and latches the accessed data until $\overline{CE}$ goes high again. The latched data will appear at the outputs whenever $\overline{CE}$ is low, CS is high, and $\overline{OE}$ is low. A read is initiated with CS going high if $\overline{CE}$ is already low.

ERASE MODE: A Block Erase (all 0's in memory) is accomplished by setting $\overline{CE}$ and $\overline{OE}$ high, raising the positive supply to + V_{PP} and then pulsing $\overline{OE}$ low. When the circuit internally senses the +V_{PP} voltage, it floats the outputs preventing +V_{PP} level signals from appearing on the data I/O bus. Erasure can also be controlled by CS if $\overline{OE}$ is already low.

WRITE MODE: A Write consists of programming 1's into bits that contain a 0. A byte is written by setting $\overline{CE}$ and $\overline{OE}$ high, raising the positive supply to +V_{PP}, and pulsing $\overline{CE}$ low. The address lines must have valid data when $\overline{CE}$ falls and the data to be programmed must be valid on the data I/O lines while $\overline{CE}$ is low. A Write operation can follow an Erase while holding +V_{DD} at +V_{PP}, and several or all the bytes can be programmed with +V_{DD} held at +V_{PP}. A Write can also be controlled by CS if $\overline{CE}$ is already low.

SUMMARY OF OPERATING MODES

State	$\overline{CE}$	CS	$\overline{OE}$	V_{DD}	I/O Bus
Standby (unselected)[5]	X	0	X	X	Floating
Standby (selected)[5]	1	1	1	X	Floating
Standby (selected)	1	1	0	+5	Floating
Read	0	1	1	+5	Floating
Read	0	1	0	+5	Data Output
Erase	1	1	0	+V_{PP}	Floating
Program	0	1	1	+V_{PP}	Data Input
Prohibited State	0	1	0	+V_{PP}	Data Input

NOTE 5 — Recommended modes for V_{DD} transition to and from +V_{PP}. V_{DD} should not fall below input levels during transition.

PIN DESCRIPTIONS

A 0—A 9: Address inputs which select one of 1024 bytes of memory for either Read or Program. The addresses need to be valid only during the falling edge of $\overline{CE}$.

I/O_0—I/O_7: Bidirectional three-state data lines that are Data outputs during a Read operation and Data inputs during a Write operation.

GND: Negative supply terminal and V = 0 reference.

V_{DD}: Positive supply terminal. It is raised to +V_{PP} for Erase and Write operations.

CS: Chip Select. A Logic Low disables all control inputs in all modes.

$\overline{OE}$: Output Enable. A Logic High disables the Data Output Drivers in normal operation. If V_{DD} = +V_{PP}, a Logic Low causes a block erase. This input is active only when CS is high.

$\overline{CE}$: Chip Enable. This input causes the circuit to read the addresses at its falling edge for both Read and Write operations. For the Read operation, accessed data is latched and valid as long as $\overline{CE}$ is held at a Logic Low. If V_{DD} = +V_{PP}, a Logic Low causes a byte Write operation. This input is active only when CS is high.

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Printed in U.S.A. 2/84
Supersedes Previous Data

Serial Input LCD Driver

DESCRIPTION

The 0438A is a CMOS/LSI circuit which acts as a smart peripheral that drives up to 32 segment LCD displays, usually under microprocessor control. The device is processed to MIL STD 883B Class B to meet military/aerospace environments. Requiring only three control lines due to its serial input construction, the device latches the data to be displayed and relieves the microprocessor of the task of generating the required waveforms.

The 0438A can drive any standard or custom parallel drive LCD display whether it be field effect or dynamic scattering, 7, 9, 14 or 16 segment characters, decimals, leading + or −, or special symbols. Several 0438A's can be cascaded. The AC frequency of the LCD waveforms can be supplied by the user or can be generated by attaching a capacitor to the LCDΦ input, which controls the frequency of an internal oscillator.

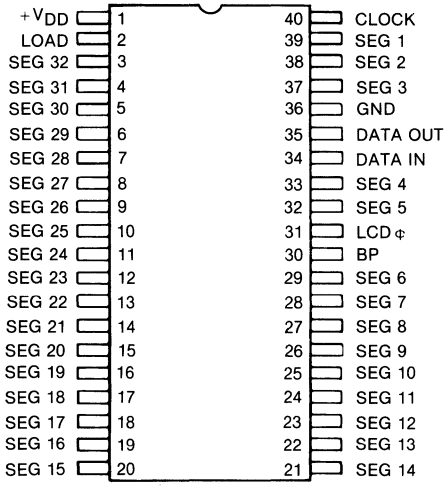
The 0438A can also be used as a column driver in a multiplexed LCD display. In this application timing and refresh must be supplied externally.

The 0438A is available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available to Class B optical criteria upon request.

FEATURES

- Military Standard 883B, Class B Qualified
- Drives up to 32 LCD segments of arbitrary configuration
- CMOS construction for:
  - Wide supply voltage range
  - Low power operation
  - High noise immunity
  - Wide temperature range
- CMOS, NMOS, and T^2L compatible inputs
- Cascadable
- On chip oscillator
- Requires only 3 control lines

PIN CONFIGURATION



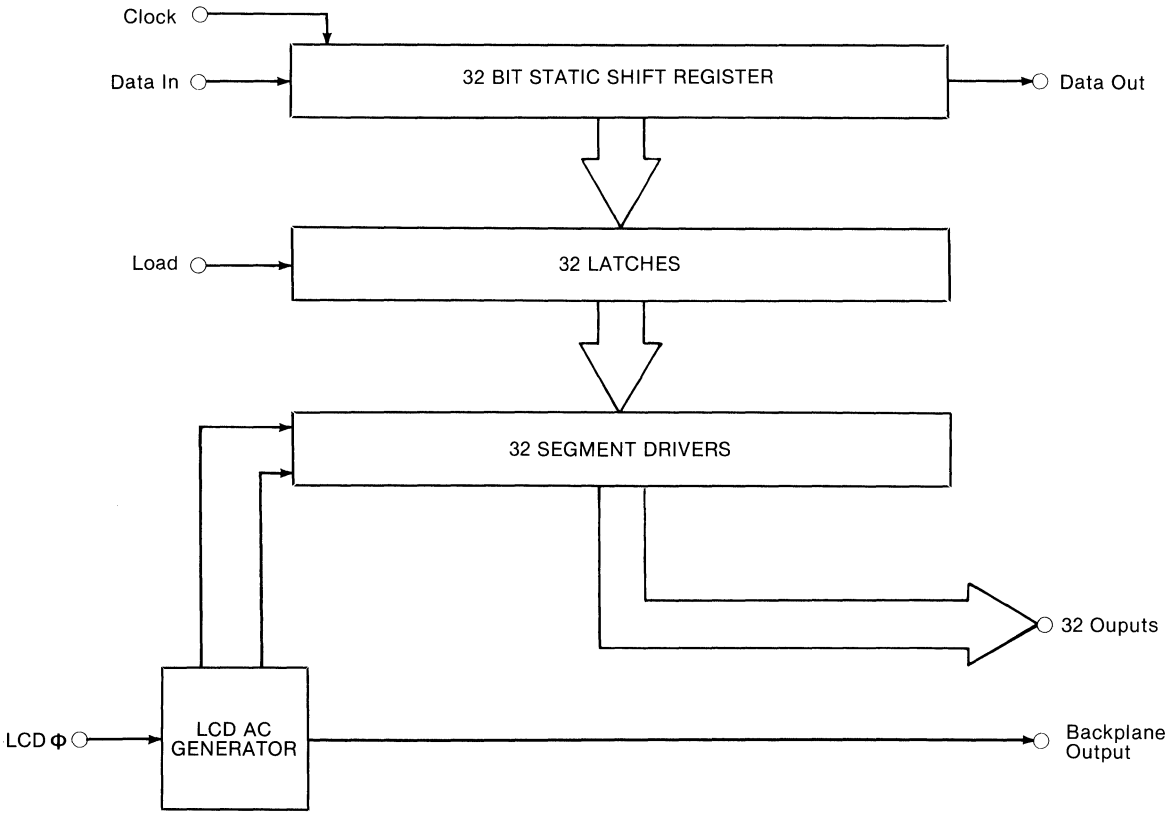
ABSOLUTE MAXIMUM RATINGS

V_{DD} ..... −.3 to + 15V
Inputs (Clk, Data In, Load) ..... $+V_{DD}$ − 15 to + V_{DD} + .3V
LCDΦ Input ..... −.3 to + V_{DD} + .3V
Power Dissipation ..... 250 mW
Operating Temperature
Ceramic Package ..... −55 to +125°C
Storage Temperature ..... −65 to + 150°C

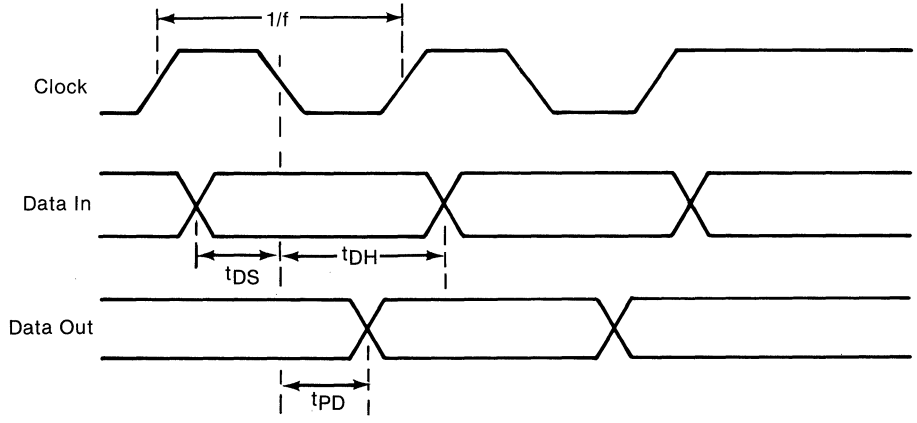
NOTE: Operating the device above the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS at T_A = −55 to + 125°C and V_{DD} = 5V unless otherwise noted

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		3	10	V
Supply Current	I_{DD1}	LCDΦ Osc < 15 KHz 5V		200	μA
		LCDΦ Osc < 15 KHz 15V		1.2	mA
Quiescent Current	I_Q	V_{DD} = 5V		40	μA
		V_{DD} = 15V		200	μA
Input High Level (Clock, Data, Load)	V_{IH}		$.5V_{DD}$	V_{DD}	V
Input Low Level (Clock, Data, Load)	V_{IL}		$V_{DD}-15$	$.2V_{DD}$	V
Input Current (Clock, Data, Load)	I_L	V_{DD} = 10V		10	μA
Input Capacitance (Clock, Data, Load)	C_I			5	pf
Segment Output Impedance	R_{ON}	I_L = 10μA		60	KΩ
Backplane Output Impedance	R_{ON}			4	KΩ
Data-Out Output Impedance	R_{ON}			4	KΩ
Clock Rate	f	50% Duty Cycle, V_{DD} = 10	DC	1.0	MHz
Data Set-up Time	t_{DS}	Data change to Clk falling edge, V_{DD} = 10	210		nsec
Data Hold Time	t_{DH}	V_{DD} = 10	70		nsec
Load Pulse Width	t_{PW}	V_{DD} = 10	245		nsec
Data Out Prop. Delay	t_{PD}	C_L = 55pf, V_{DD} = 10		700	nsec
LCDΦ Input High Level	V_{IN}		$.9V_{DD}$		V
LCDΦ Input Low Level	V_{IL}			$.1V_{DD}$	V
LCDΦ Input Current Level	I_L	Driven, V_{DD} = 10V		20	μA



TIMING DIAGRAM



OPERATING NOTES

1. The shift register loads, shifts, and outputs on the falling edge of Clock.

2. A logic 1 on Data In causes a segment to be visible.

3. A logic 1 on Load causes a parallel load of the data in the shift register into latches that control the segment drivers.

4. If LCD Φ is driven, it is in phase with the Backplane Output.

5. To cascade units, either connect Backplane of one circuit to LCD Φ of all other circuits (thus one capacitor provides frequency control for all circuits) or connect LCD Φ of all circuits to a common driving signal. If the former is chosen, tie just one Backplane to the LCD and use a different Backplane output to drive the LCD Φ inputs. Either the data can be loaded to all circuits in parallel or Data Out can be connected to Data In to form a long serial shift register.

6. The supply voltage of the 0438A is equal to half the peak driving voltage of the LCD. If the 0438A supply voltage is less than the swing of the controlling logic signals, the positive supply leads of the logic circuitry and the 0438A should be tied in common, not the ground (or negative) supply leads. Be careful that input level specifications are met.

7. The LCD Φ pin can be used in two modes, driven or oscillating. If LCD Φ is driven, the circuit will sense this condition and pass the LCD Φ input to the Backplane output. If the LCD Φ pin is allowed to oscillate, its frequency is inversely proportional to capacitance and the LCD driving waveforms have a frequency 2^8 slower than the oscillator itself. This relationship is shown in Figure 1. The frequency is nearly independent of supply voltage. If LCD Φ is oscillating, it is important to keep coupling capacitance to backplane and segments as low as possible. Similarly, it is recommended that the load capacitance on LCD Φ be as large as is practical.

8. There are two obvious signal races to be avoided in this circuit, (1) changing Data In when Clock is falling, and (2) changing load when Clock is falling.

9. The number of a segment corresponds to how many clock pulses have occurred since its data was present at the input. For example, the data on Seg 19 was input 19 clock pulses earlier.

10. It is acceptable to tie the load line high. In this case the latches are transparent. Also, remote control would only require two signal lines, Clock and Data In.

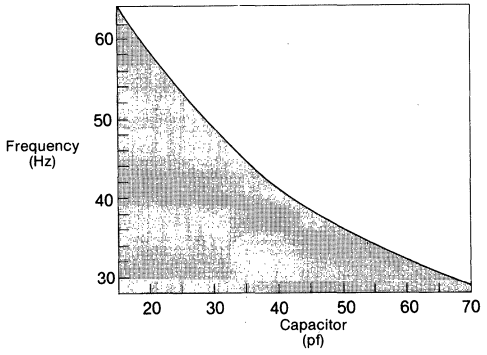


FIGURE 1

HUGHES SOLID STATE PRODUCTS
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11/83 Rev. N/C
Printed in U.S.A.
Supersedes Previous Data

1800 CMOS Microprocessor Products
Static ROM

512 x 8 Static ROM – 1831
1024 x 8 Static ROM – 1833

DESCRIPTION

Hughes' 1831 and 1833 are Static CMOS Mask Programmable Read Only Memories processed to MIL STD 883B, Class B to meet military/aerospace environments.

The 1831 and 1833 respond to a 16 bit address time multiplexed on the eight address (MA 0-MA 7). The eight most significant address lines are latched on the chip by the clock input. This address may be decoded by a mask option to allow the 1831 to operate in any 512 word area, and the 1833 in any 1024 word area within the 65,536 byte memory space.

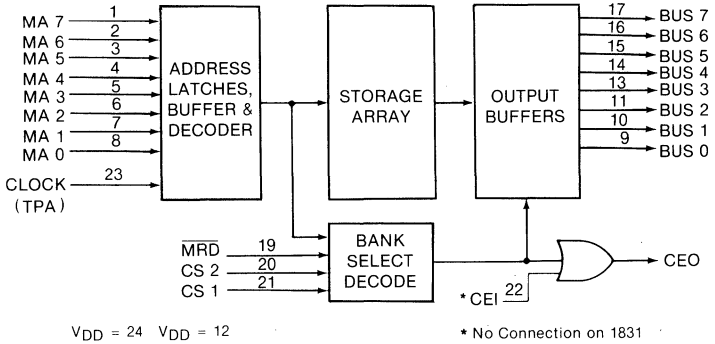
In addition, three chip select signals may be decoded for simplified system interfacing. The Chip Enable Output (CEO) is activated when the chip is selected and can be used as a disable control for small RAM memory systems. Data is accessed from the memory by decoding the Address inputs and enabled on the data bus by the two Chip Selects (CS 2 and CS 1), the Memory Read ($\overline{MRD}$) and the upper address decode. The CEI signal may be used as an additional control of the ROM selected output signal, CEO, on the 1833.

The 1831 and 1833 operate over a 4-10.5 voltage range while the 1831C and 1833C operate over a 4-6.5 voltage range. The ROMs are available in a 24 lead hermetic dual-in-line ceramic package (D suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request to Class B optical criteria.

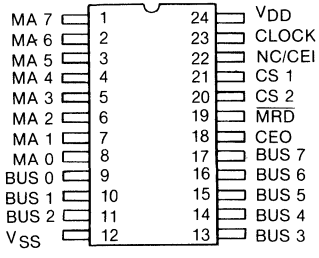
FEATURES

- MIL STD 883B, Class B Qualified
- Static Silicon Gate CMOS Circuitry
- Interfaces Directly with 1802A Microprocessor without Additional Components
- Access Time
  850ns Typical at V_{DD} = 5V
  350ns Typical at V_{DD} = 10V
- Single Voltage Supply
- Low Quiescent and Operating Power
- Static – No Clocks Required
- Chip Select and Address Location Within 64K Memory Space, Mask Programmable

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T_A)
Ceramic Package ..... −55 to +125°C
DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
1831/1833 ..... −0.5 to +13V
1831C/1833C ..... −0.5 to + 7V
Storage Temperature Range (T_{stg}) .... −65 to +150°C

NOTE: Operating the device above the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full Package Temperature Range Unless Otherwise Specified.

CHARACTERISTICS	CONDITIONS V_{DD} (V)	LIMITS 1831 Min.	1831 Max.	1831C Min.	1831C Max.	LIMITS 1833 Min.	1833 Max.	1833C Min.	1833C Max.	UNITS
Supply Voltage Range (At T_A = Full Package Temperature Range)	–	4	10.5	4	6.5	4	10.5	4	6.5	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Clock Pulse Width (TPA), t_{PAW}	5	200	–	200	–	200	–	200	–	ns
	10	70	–	–	–	70	–	–	–	
Address Setup Time, t_{AS}	5	100	–	100	–	100	–	100	–	ns
	10	50	–	–	–	50	–	–	–	
Address Hold Time, t_{AH}	5	150	–	150	–	120	–	120	–	ns
	10	75	–	–	–	60	–	–	–	

ELECTRICAL CHARACTERISTICS at T_A = −55 to + 125°C

CHARACTERISTICS	CONDITIONS V_O (V)	V_{DD} (V)	1831 Min.	1831 Typ.*	1831 Max.	1831C Min.	1831C Typ.*	1831C Max.	1833 Min.	1833 Typ.*	1833 Max.	1833C Min.	1833C Typ.*	1833C Max.	UNITS
STATIC															
Quiescent Device Current, I_L	–	5	–	0.01	100	–	0.02	400	–	0.01	100	–	0.02	400	µA
	–	10	–	1	400	–	–	–	–	1	400	–	–	–	
Output Drive Current,	0.4	5	0.4	0.6	–	0.4	0.6	–	0.8	–	–	0.8	–	–	
N-Channel (Sink), I_{DN}	0.5	10	0.8	1.2	–	–	–	–	1.8	–	–	–	–	–	mA
P-Channel (Source), I_{DP}	4.6	5	−0.4	0.6	–	0.4	0.6	–	−0.8	–	–	−0.8	–	–	
	9.5	10	−0.8	1.2	–	–	–	–	−1.8	–	–	–	–	–	
Output Voltage	–	5	–	0	0.05	–	0	0.05	–	0	0.05	–	0	0.05	V
Low Level, V_{OL}	–	10	–	0	0.05	–	–	–	–	0	0.05	–	–	–	
Output Voltage	–	5	4.95	5	–	4.95	5	–	4.95	5	–	4.95	5	–	V
High Level, V_{OH}	–	10	9.95	10	–	–	–	–	9.95	10	–	–	–	–	
Input Leakage Current,	–	5	–	–	±1	–	–	±1	–	–	±1	–	–	±1	
I_{IL}, I_{IH}	–	10	–	–	±1	–	–	–	–	–	±1	–	–	–	µA
3-State Output Leakage	0,5	5	–	–	±1	–	–	±1	–	–	±1	–	–	±1	
Current, I_{OUT}	0,10	10	–	–	±1	–	–	–	–	–	±1	–	–	–	µA

* Typical values are for T_A = 25°C and nominal V_{DD}

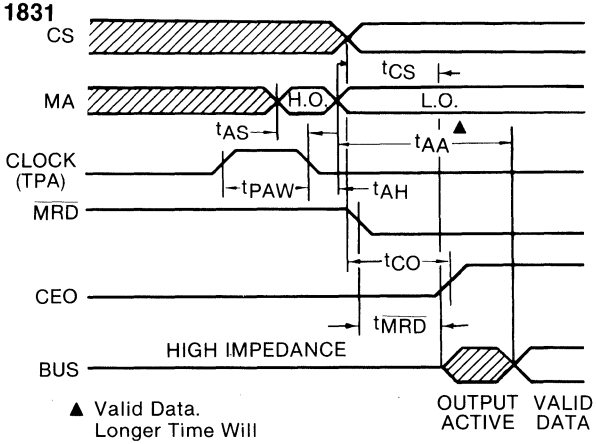
ELECTRICAL CHARACTERISTICS, Cont.

CHARACTERISTICS	CONDITIONS V_O (V)	CONDITIONS V_{DD} (V)	1831 Min.	1831 Typ.*	1831 Max.	1831C Min.	1831C Typ.*	1831C Max.	1833 Min.	1833 Typ.*	1833 Max.	1833C Min.	1833C Typ.*	1833C Max.	UNITS
DYNAMIC: t_r, t_f = 10ns, C_L = 50pF, R_L = 200 KΩ															
Access Time From Address	–	5	–	850	1100	–	850	1100	–	650	1000	–	650	1000	
Change, t_{AA}	–	10	–	400	600	–	–	–	–	350	500	–	–	–	ns
Access Time From Chip	–	5	–	700	1000	–	700	800	–	500	900	–	500	900	
Select, t_{ACS}	–	10	–	250	500	–	–	–	–	275	400	–	–	–	ns
CEO From Address	–	5	–	500	600	–	500	600	–	120	240	–	120	240	
Change, t_{CA}	–	10	–	200	250	–	–	–	–	70	140	–	–	–	ns
Bus Contention Delay,	–	5	–	200	350	–	200	350	–	220	300	–	220	300	
t_D	–	10	–	100	150	–	–	–	–	130	250	–	–	–	ns
Daisy Chain Delay,	–	5	–	–	–	–	–	–	–	200	360	–	200	300	
t_{IO}	–	10	–	–	–	–	–	–	–	100	150	–	–	–	ns
Read Delay,	–	5	–	300	800	–	300	700	–	400	700	–	400	700	
$t_{\overline{MRD}}$	–	10	–	100	400	–	–	–	–	200	350	–	–	–	ns
Chip Select Delay,	–	5	–	600	800	–	600	800	–	250	450	–	250	450	
t_{CS}	–	10	–	200	400	–	–	–	–	125	250	–	–	–	ns
Chip Enable Output Delay	–	5	–	450	500	–	400	500	–	200	325	–	200	325	
Time From CS, t_{CO}	–	10	–	200	250	–	–	–	–	100	170	–	–	–	ns
Power Dissipation, P_D	–	5	–	15	–	–	15	–	–	30	–	–	30	–	
Cycle time = 2.5μs	–	10	–	60	–	–	–	–	–	120	–	–	–	–	mW

*Typical values are for T_A = 25°C and nominal V_{DD}

TIMING DIAGRAMS

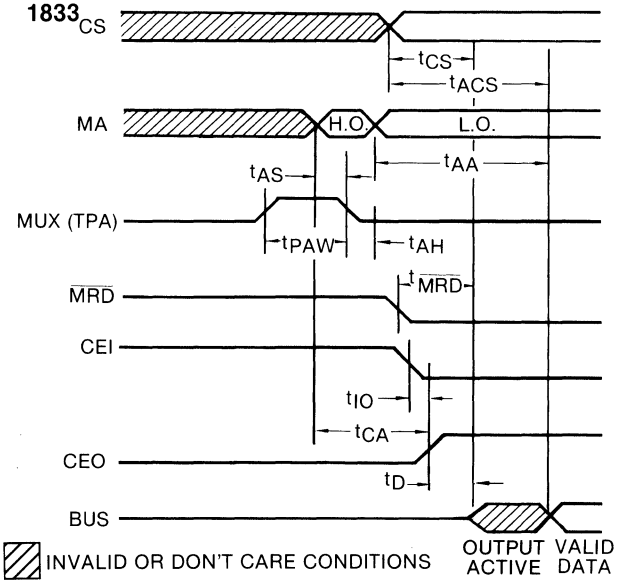
1831



▲ Valid Data. Longer Time Will Initiate An Earlier But Invalid Output

H.O. = High Order Address
L.O. = Low Order Address

1833



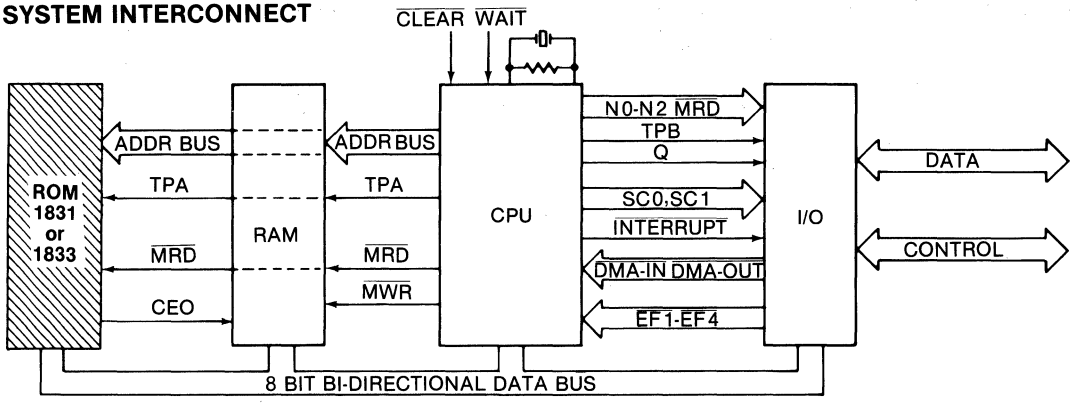
INVALID OR DON'T CARE CONDITIONS

The dynamic characteristic table and the above timing diagrams represent maximum performance capability of the 1831/1833. When used in direct system interface with the 1802A microprocessor, the timing relation will be determined by the clock frequency and timing signal generation of the microprocessor. In the latter case the following general timing conditions hold: $t_{AH} = 0.5\ t_C$

$t_{PAW} = 1.0 t_C$

$\overline{MRD}$ occurs one clock period (t_C) earlier than address bus MA0 – MA7.
t_C = 1/1802A clock frequency.

SYSTEM INTERCONNECT



SIGNAL DESCRIPTION

MA0 – MA7: High order byte of a 16-bit memory address appears on the memory address lines, (MA0–MA7), first. Those bits required by the memory system are strobed into internal address latches by Clock (TPA) input. The low order byte of 16-bit address appears on the address lines after the termination of TPA.

BUS0 – BUS7: These eight bi-directional three state data lines form a common bus with the 1802A microprocessor.

CLOCK (TPA): A timing signal from 1802A microprocessor (trailing edge of TPA) is used to latch the high order byte of the 16-bit memory address. The polarity of TPA is user mask programmable.

CS1, CS2, $\overline{\text{MRD}}$: Chip Select and Memory Read (output enable) signals. The polarity of the chip select signals are user mask programmable.

CEO, CEI: Chip enable output signal (CEO) is high when either the chip is selected or CEI is high (1833 only). CEO and CEI can be connected in daisy chain operation between several ROMs to control selection of RAM chips in a microprocessor system without additional components. The polarity of CEI is user mask programmable in the 1833.

ORDERING INFORMATION

Contact Hughes for price and other information relating to ROMs. ROM order forms and instructions concerning means of data conveyance are available from Hughes Solid State Products or Hughes' representatives.

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HUGHES AIRCRAFT COMPANY

500 Superior Avenue
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Telephone (714) 759-2942 TWX: 910-596-1374

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Printed in U.S.A.
Rev. N/C 5/83
Supersedes Previous Data

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Hughes can add another dimension to your product by adding nonvolatile memory to your custom circuit!

Hughes is equipped to handle your custom and semi-custom requirements from specification definition through:

- Design
- Mask Fabrication
- Wafer Fabrication
- Assembly
- Test
- Delivery of volume production

Hughes' CMOS processes include our high performance 3μ HCMOS (1 nsec gate delay) and metal gate processes, which are selectively used for logic, nonvolatile memory and analog functions.

Hughes' Standard Cell technology can be used for fast turnaround of prototypes. Our design automation system allows for merging linear and digital logic functions on a Standard Cell device.

Microcircuit Packaging

Hughes is a producer of high volume multi-chip assemblies, utilizing state of the art technology to achieve high packaging densities for hi-rel applications at competitive prices.

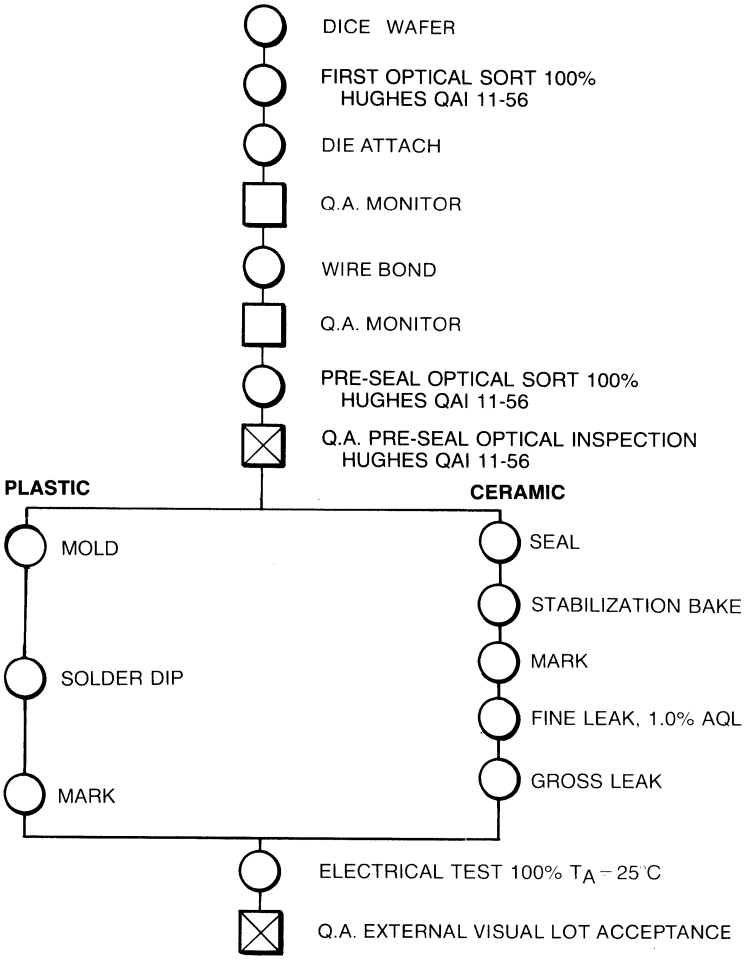
SILICON FOUNDRY

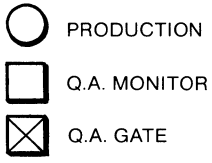
Hughes' full service foundry accepts customer owned tooling (COT) for our 3μ HCMOS silicon gate, 5μ CMOS metal gate, and 7μ PMOS metal gate processes. Custom designs should be supplied in the form of Calma GDS-II database tapes or masks for a minimum run of 25 wafers. We provide wafers, die or packaged devices, processed for military, industrial or commercial applications.

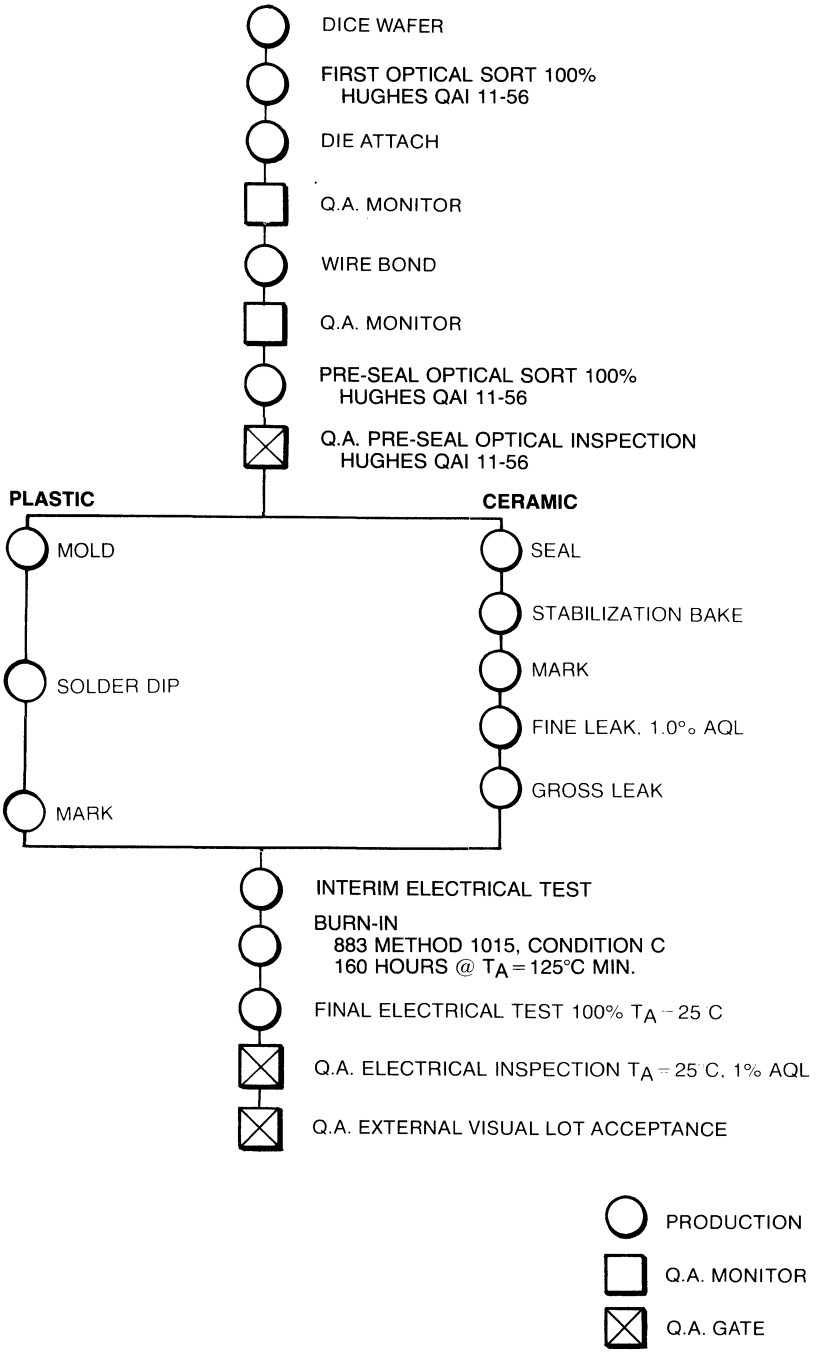
Hughes provides simulation in SPICE to worst case parameters. Our post-wafer processing includes wafer probing, packaging and packaged device testing. We maintain our processes by using sophisticated process control monitors.

Process Specifications — Design Parameters

ELECTRICAL PARAMETERS @ 25°C	N Channel Typ.	P Channel Typ.
V_T @ 1μa, volts	.6 to 1.2	−.6 to −1.2
Field Inv @ 1μa, volts		
Poly Silicon	10	−8
Metal I	15	−15
BV_{DSS} volts	10	−10
Body Effect	1.2	0.69
KP	20 to 30	10 to 14
PROCESS PARAMETERS		
Oxide Thickness, μm		
Gate (Std Gate)	0.070	0.070
Field (Poly-Sub)	0.75	0.75
Field (Poly-Met)	0.60	0.60
Met-Metal II	1.00	1.00
Capacitance		
COX, pF/sq. mil	.32	.32
CJO, pF/sq. mil	.15	.10
Poly Silicon		
Sheet Res, ohms/sq.	25	35
Diffusion		
Well Res., kohms/sq.	1.0 to 2.5	—
Diff. Res., ohms/sq.	20 to 35	30 to 50
Metal		
Met Thick, μm	.60	.60
Metal II Thick, μm	1.00	1.00
Max. Current Density = 5. 0E5 amp/sq. cm		


DICE WAFER
FIRST OPTICAL SORT 100%
HUGHES QAI 11-56
DIE ATTACH
Q.A. MONITOR
WIRE BOND
Q.A. MONITOR
PRE-SEAL OPTICAL SORT 100%
HUGHES QAI 11-56
Q.A. PRE-SEAL OPTICAL INSPECTION
HUGHES QAI 11-56
PLASTIC
CERAMIC
MOLD
SOLDER DIP
MARK
SEAL
STABILIZATION BAKE
MARK
FINE LEAK, 1.0% AQL
GROSS LEAK
ELECTRICAL TEST 100% $T_A = 25°C$
Q.A. EXTERNAL VISUAL LOT ACCEPTANCE


PRODUCTION
Q.A. MONITOR
Q.A. GATE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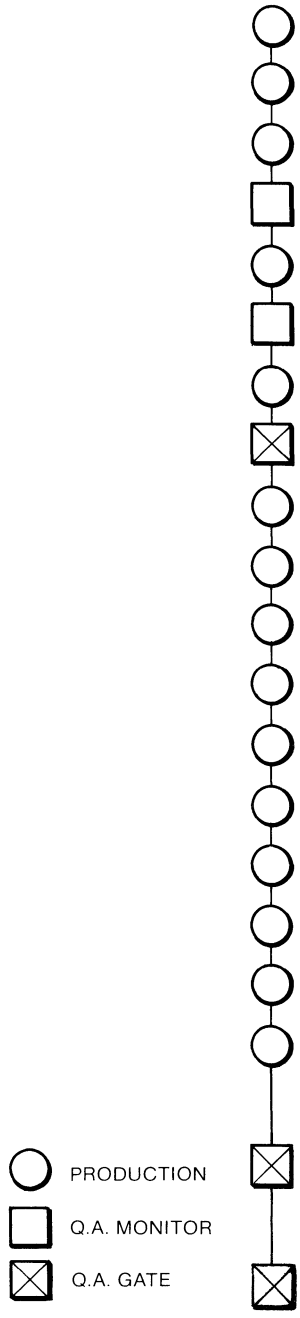
SEAL
STABILIZATION BAKE
MARK
FINE LEAK, 1.0% AQL
GROSS LEAK
INTERIM ELECTRICAL TEST
BURN-IN
883 METHOD 1015, CONDITION C
160 HOURS @ T_A = 125°C MIN.
FINAL ELECTRICAL TEST 100% T_A = 25 C
Q.A. ELECTRICAL INSPECTION T_A = 25 C, 1% AQL
Q.A. EXTERNAL VISUAL LOT ACCEPTANCE
PRODUCTION
Q.A. MONITOR
Q.A. GATE



DICE WAFER

FIRST OPTICAL SORT 100%
883 METHOD 2010 CONDITION B

DIE ATTACH

Q.A. MONITOR

WIRE BOND
ULTRASONIC Al 10% REBOND

Q.A. MONITOR

PRE-SEAL OPTICAL SORT 100%
883 METHOD 2010 CONDITION B

Q.A. PRE-SEAL OPTICAL INSPECTION
883 METHOD 2010 CONDITION B

SEAL

STABILIZATION BAKE
883 METHOD 1008 CONDITION C MIN.

TEMPERATURE CYCLING
883 METHOD 1010 CONDITION C

CONSTANT ACCELERATION
883 METHOD 2001 CONDITION E OR D
PER PACKAGE LIMITATIONS, Y-1 AXIS

MARK

FINE LEAK 100%
883 METHOD 1014 CONDITION A OR B

GROSS LEAK 100%
883 METHOD 1014 CONDITION C

INTERIM ELECTRICAL TEST

BURN-IN
883 METHOD 1015 CONDITION C
160 HOURS @ $T_A = 125°C$ MIN.

FINAL ELECTRICAL TESTS 100%
883 METHOD 5005, TABLE 1
STATIC & FUNCTIONAL TESTS @ $T_A = 25°C$ AND 125°C
SWITCHING TESTS @ $T_A = 25°C$
TEST REQ. PER HUGHES DATA SHEET OR CUST. SPEC.

Q.A. ELECTRICAL INSPECTION; GROUP A TESTS PER
883 METHOD 5005, TABLE 1
STATIC & FUNCTIONAL TESTS @ $T_A = 25°C$ AND 125°C
SWITCHING TESTS @ $T_A = 25°C$

Q.A. EXTERNAL VISUAL LOT ACCEPTANCE
883 METHOD 2009, 2.5% AQL

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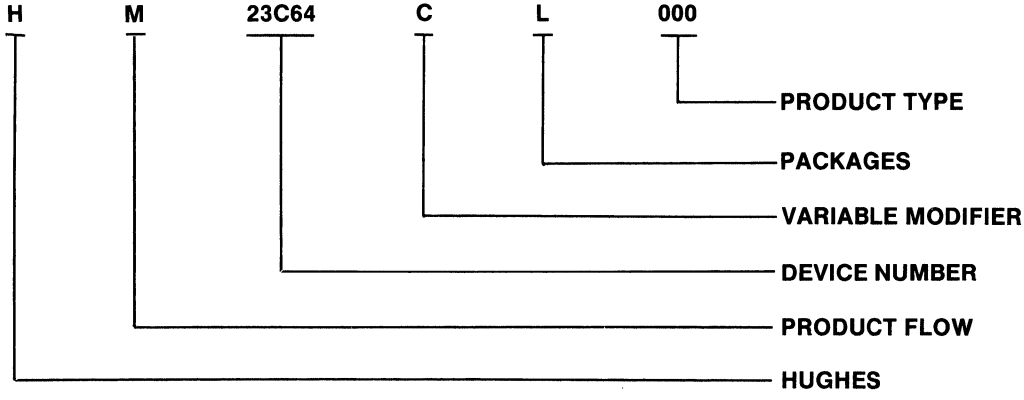
STATUS NOTICES

Preliminary Information: indicates guidance values for evaluation purposes. Some electrical parameters are subject to change.

Advance Information: indicates design objectives. Some functional characteristics are subject to change.

NOMENCLATURE

Hughes is in the process of re-defining our nomenclature. For more detailed information, contact Hughes or Hughes' representatives.



Example

HM 23C64-C-L-000 = Hughes Military 23C64, 4-6.5 voltage range, in a leadless chip carrier package, standard device.

Product Type
- 000 = Standard Product
- XYZ = Custom Product*

Variable Modifier*
- One character modifier for speed, power, processing, etc.

Packages
- L = Leadless Chip Carrier
- D = Ceramic Dip
- H = Devices in Chip Form
- P = Plastic Dip
- Y = Cerdip

Product Flow
- C = Commercial
- I = Industrial
- B = Hi Reliability
- M = Military
- S = Special*

*For detailed information, contact Hughes' Customer Service.

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