

# MB1517A ASSP

## 2.0 GHz High-Speed Tuning PLL Frequency Synthesizer

The Fujitsu MB1517A is a serial input phase-locked loop (PLL) frequency synthesizer with a pulse-swallow function. MB1517A achieves the low noise performance as well as the high-speed lock-up which is required for digital mobile communications. The MB1517A can operate from a single +3 V supply. Fujitsu's advanced technology achieves an  $I_{CC}$  of 12 mA (typical) as well as 100  $\mu$ A (typical) at power down mode.

### FEATURES

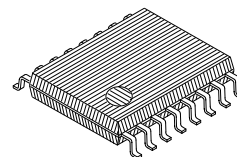
- High operating frequency :  $f_{IN} = 2.0$  GHz ( $P_{IN} = -10$  dBm)
- Pulse-swallow function : High-speed two-modulus prescaler with selectable 64/65 and 128/129 divide ratios
- Low supply current :  $I_{CC} = 12$  mA typ. at 3 V
- Power saving function :  $I_{PS} = 100$   $\mu$ A typ.
- Serial input, 18-bit programmable divider consisting of:  
Binary 7-bit swallow counter : 0 to 127  
Binary 11-bit programmable counter : 5 to 2,047
- Serial input 17-bit programmable reference divider consisting of:  
Binary 14-bit programmable reference counter: 6 to 16,383  
1-bit switch counter sets prescaler divide ratio  
1-bit power saving function control  
1-bit LD/font switch
- On-chip high performance charge pump circuit and phase comparator, achieving high-speed lock-up and low phase noise
- Two types of phase comparator outputs selectable  
On-chip charge pump output  
Output for an external charge pump
- Wide operating temperature range:  $-40$  to  $+85^{\circ}\text{C}$
- Plastic 16-pin SSOP (shrink small outline) package

### ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameters	Symbol	Rating	Unit	Remark
Supply voltage	$V_{CC}$	$-0.5$ to $+5.0$	V	
	$V_P$	$V_{CC}$ to $5.5$	V	
Output voltage	$V_O$	$-0.5$ to $V_{CC} + 0.5$	V	
Open drain voltage	$V_{OOP}$	$-0.5$ to $6.0$	V	$\Phi P$ , LD/fout
Output current	$I_O$	$\pm 10$	mA	
Storage temperature	Tstg	$-55$ to $+125$	$^{\circ}\text{C}$	

**NOTE:** Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Plastic SSOP, 16 pin



(FPT-16P-M05)

### PIN ASSIGNMENT

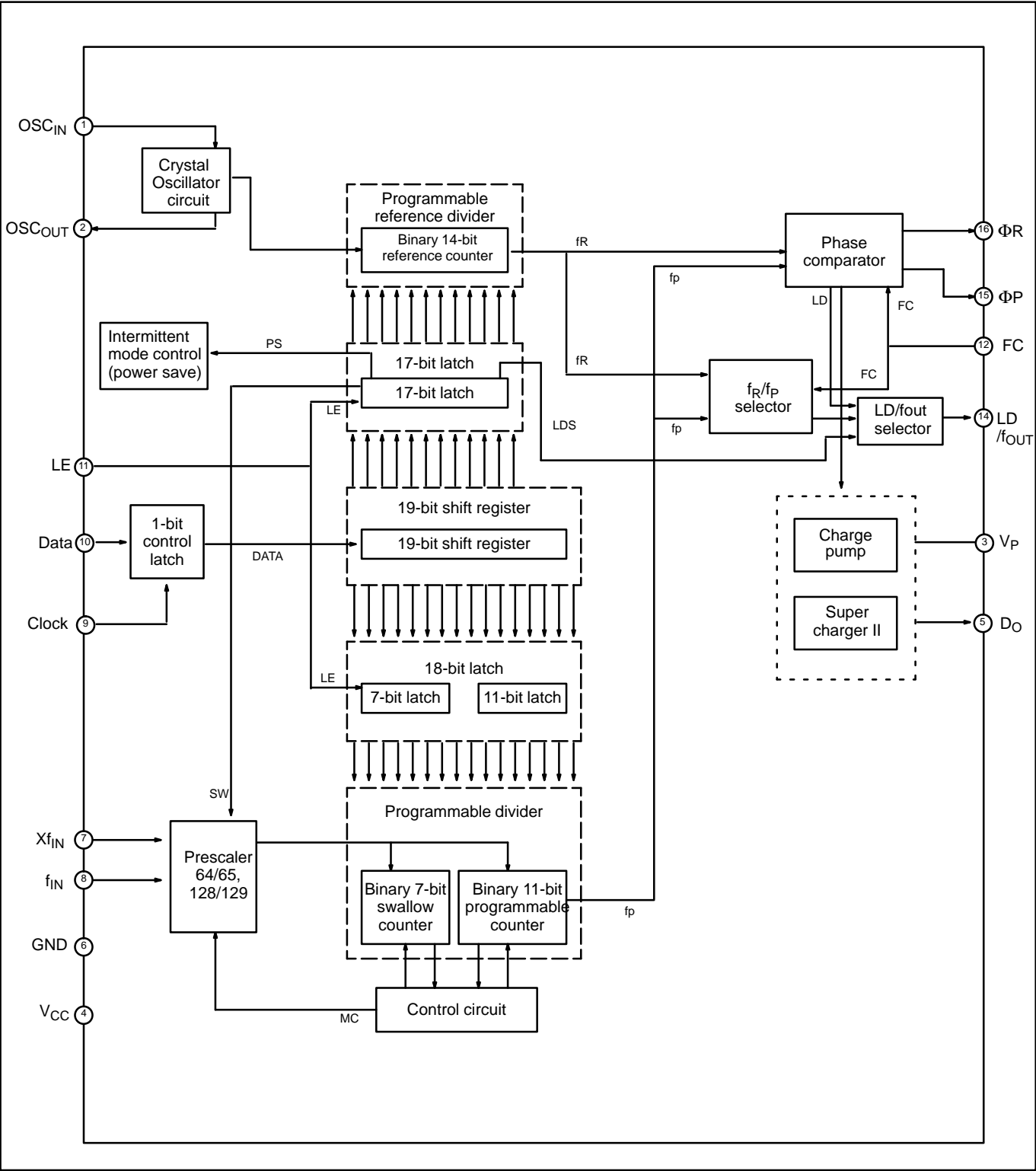
(TOP VIEW)

OSC <sub>IN</sub>	1	16	$\Phi R$
OSC <sub>OUT</sub>	2	15	$\Phi P$
$V_P$	3	14	LD/f <sub>OUT</sub>
$V_{CC}$	4	13	NC
$D_O$	5	12	FC
GND	6	11	LE
$Xf_{IN}$	7	10	Data
$f_{IN}$	8	9	Clock

(FPT-16P-M05)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



## PIN DESCRIPTION

Pin No.	Pin name	I/O	Description
1	OSC <sub>IN</sub>	I	Programmable reference divider input Oscillator input Connection for external crystal or TCXO.
2	OSC <sub>OUT</sub>	O	Oscillator output Connection for external crystal.
3	V <sub>P</sub>	–	Power supply input for the internal charge pump
4	V <sub>CC</sub>	–	Power supply
5	D <sub>O</sub>	O	Charge pump output Phase characteristics of the charge pump can be reversed by FC input.
6	GND	–	Ground
7	Xfin	I	Complementary input of the prescaler Xfin pin should be grounded via a capacitor.
8	f <sub>IN</sub>	I	Prescaler input Connection with an external VCO should be done AC coupled.
9	Clock	I	Clock input for 19-bit shift register Data is shifted into the shift register on the rising edge of the clock.
10	Data	I	Serial data input using binary code The last bit of the data is a control bit. When the control bit is high, data is transmitted to the 17-bit latch. When it is low, data is transmitted to the 18-bit latch.
11	LE	I	Load enable signal input When LE is high, the data of the shift register are transferred to a latch, according to the control bit in the serial data.
12	FC	I	Phase switch input for phase comparator When FC is low, the characteristics of the charge pump and phase comparator are reversed The FC input signal is also used to control the f <sub>OUT</sub> pin (test pin) output (f <sub>R</sub> or f <sub>P</sub> ).
13	NC	–	No connection
14	LD/f <sub>OUT</sub>	O	Lock detector output / Phase comparator monitoring output This is a N-ch open drain output. Either of the outputs is selected by LDS bit of the serial data. a) Lock detector output : at lock state .... LD = "H" at unlock stae .. LD = "L" b) Monitoring output : Phase comparator input signals (f <sub>P</sub> , f <sub>R</sub> ) can be monitored.
15	ΦP	O	Phase comparator output for an external charge pump Phase of the output is reversed according to FC input. ΦP pin is a N-ch open drain output.
16	ΦR	O	Phase comparator output for an external charge pump Phase of the output is reversed depending on FC input.

# FUNCTION DESCRIPTIONS

## Pulse swallow function

The divide ratio can be calculated using the following equation:

$$f_{VCO} = [(P \times N) + A] \times f_{OSC} \div R \quad (A < N)$$
  
 $f_{VCO}$  : Output frequency of external voltage controlled oscillator (VCO)  
 $N$  : Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)  
 $A$  : Preset divide ratio of binary 7-bit swallow counter ( $0 \leq A \leq 127$ )  
 $f_{OSC}$  : Output frequency of the reference frequency oscillator  
 $R$  : Preset divide ratio of binary 14-bit programmable reference counter (6 to 16,383)  
 $P$  : Preset divide ratio of modules prescaler (64 or 128)

## Serial data input

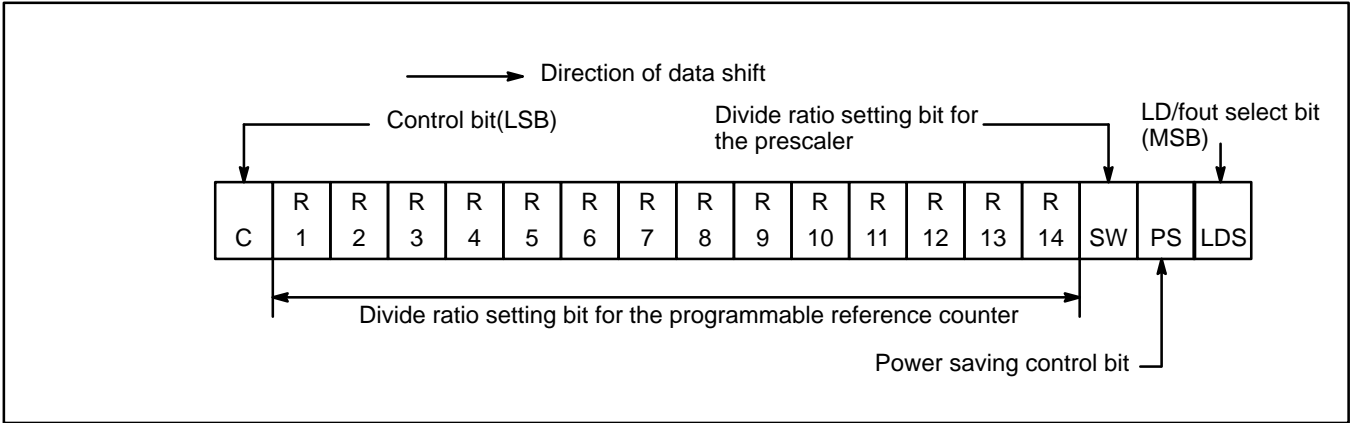
Serial data is processed using the Data, Clock, and LE pins. Serial data controls the 17-bit programmable reference divider and 18-bit programmable divider separately.

Binary serial data is entered via the Data pin.

One bit of data is shifted into the internal shift register on the rising edge of the clock. When the load enable pin is high, stored data is latched according to the control data as follows:

Control data	Destination of serial data
H	17 bit latch
L	18 bit latch

- (a) Programmable reference divider ratio  
The programmable reference divider consists of a 18-bit shift register, a 17-bit latch and a 14-bit reference counter. The serial 18-bit data format is shown below:



- 14-bit programmable reference counter divide ratio

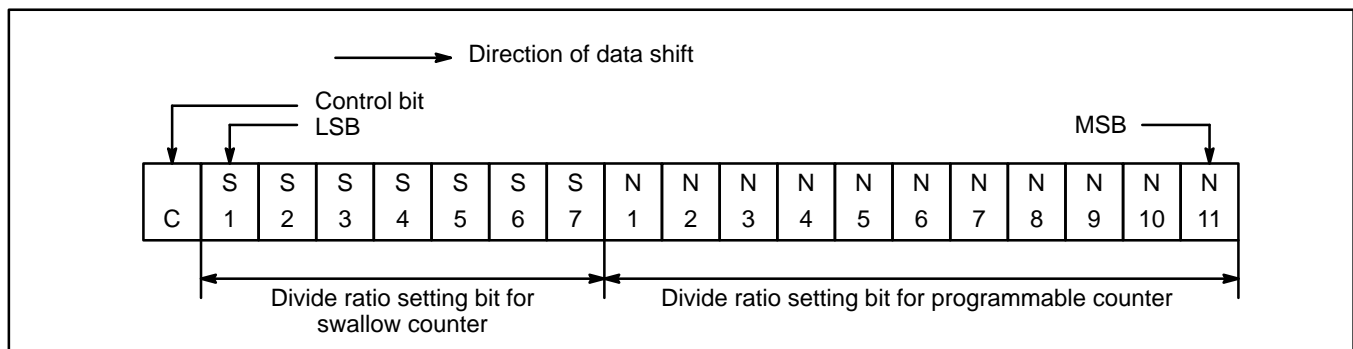
Divide ratio R	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 6 to 16,383)

- Notes:**
- Divide ratios less than 6 are prohibited.
  - SW : This bit selects the divide ratio of the prescaler.  
Low: 128 or 129  
High: 64 or 65
  - R1 to R14: These bits select the divide ratio of the programmable reference counter (6 to 16,383).
  - C: Control bit: Set high.
  - PS: This bit controls power saving mode.  
High : Nomal operation  
Low : Power saving mode
  - LDS: This bit controls LD/fout output signal  
High : fout signal ( $f_R$  or  $f_P$ ) is selected and output via LD/fout pin.  
Low : Lock detect signal is selected and output via LD/fout pin.
  - Start data input with MSB first .

(b) Programmable divider divide ratio

The programmable divider consists of a 19-bit shift register, a 18-bit latch, a 7-bit swallow counter, and a 11-bit programmable counter. The serial 19-bit data format is shown below:



MB1517A

- 7-bit swallow counter divide ratio

Divide ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

(Divide ratio = 0 to 127)

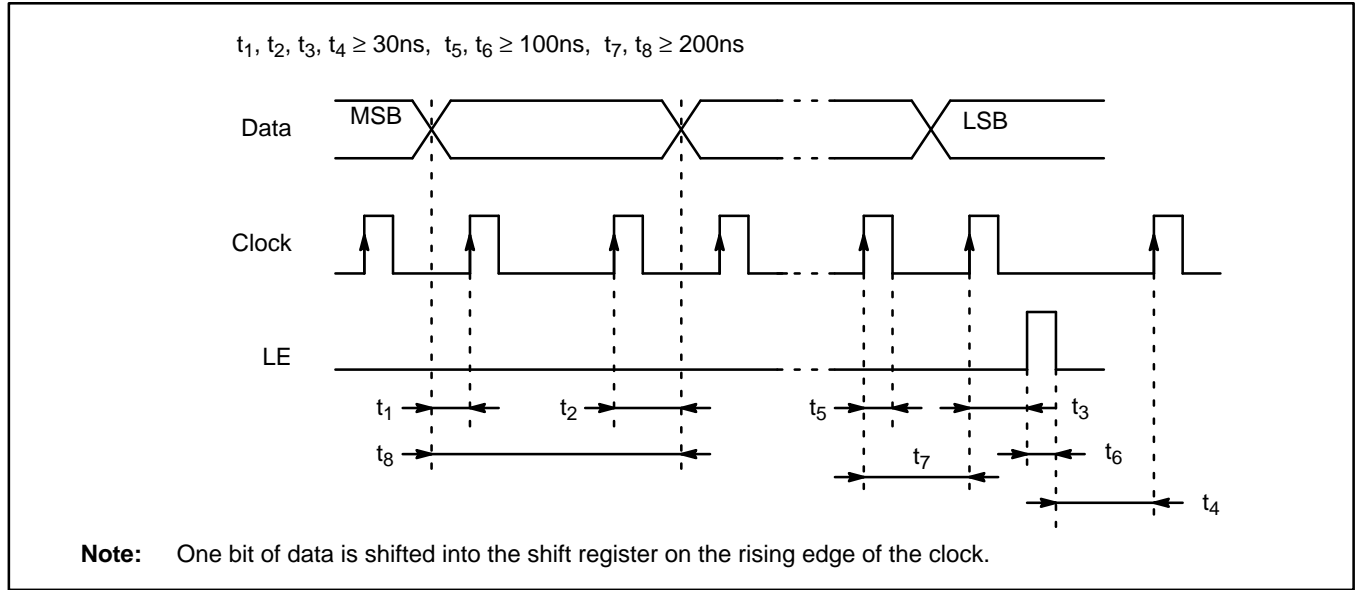
- 11-bit programmable counter divide ratio

Divide ratio N	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 5 to 2,047)

- Notes:**
1. Divide ratios less than 5 are prohibited for the 11-bit programmable counter.
  2. S1 to S7: These bits select the divide ratio of the swallow counter (0 to 127).
  3. N1 to N11: These bits select the divide ratio of the programmable counter (5 to 2,047).
  4. C: Control bit: (Set low)
  5. Start data input with MSB first.

Serial data input timing



### Power saving mode (Intermittent operation control circuit)

Setting PS bit to Low, MB1517A enters into power saving mode resultatly current sonsumption can be limited to 100 $\mu$ A (typ.). Setting PS bit to High, power saving mode is released so that the device works normally.

In addition, the intermittent operation control circuit is included which helps smooth start up from power saving mode. The power consumption can be reduced by the intermittent operation that powering down or waking up parts of the PLL circuitry. If a PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency ( $f_R$ ) and comparison frequency ( $f_P$ ) and may in the worst case take longer time for lock up of the loop. To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up, thus keeping the loop locked.

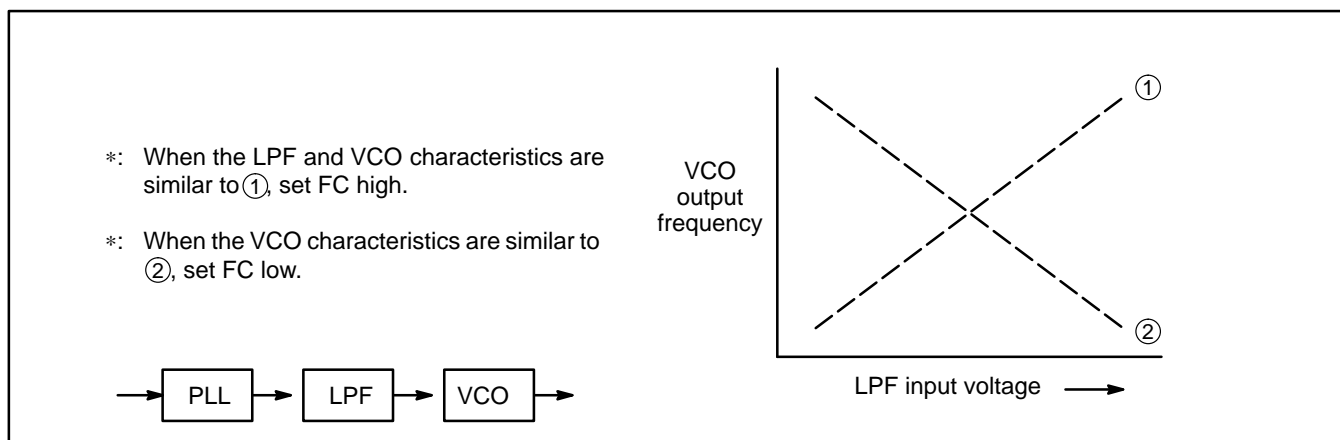
### Relation between the FC input and phase characteristics

The FC pin changes the phase characteristics of the phase comparator. Both the internal charge pump output level ( $D_O$ ) and the phase comparator output ( $\Phi_R$ ,  $\Phi_P$ ) are reversed depending on the FC pin input level. Also, the monitor pin ( $f_{OUT}$ ) output is controlled by the FC pin. The relationship between the FC input level and each of  $D_O$ ,  $\Phi_R$ , and  $\Phi_P$  is shown below:

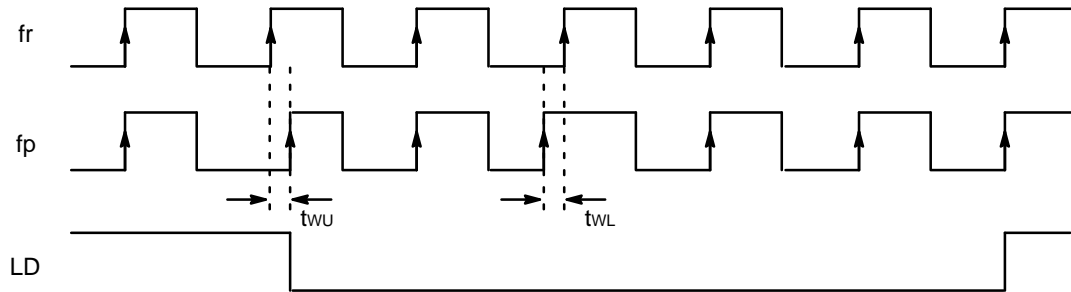
	FC = High				FC = Low			
	$D_O$	$\Phi_R$	$\Phi_P$	$f_{OUT}$	$D_O$	$\Phi_R$	$\Phi_P$	$f_{OUT}$
$f_R > f_P$	H	L	L	( $f_R$ )	L	H	Z(*1)	( $f_P$ )
$f_R < f_P$	L	H	Z(*1)	( $f_R$ )	H	L	L	( $f_P$ )
$f_R = f_P$	Z(*1)	L	Z(*1)	( $f_R$ )	Z(*1)	L	Z(*1)	( $f_P$ )

\*1: High impedance

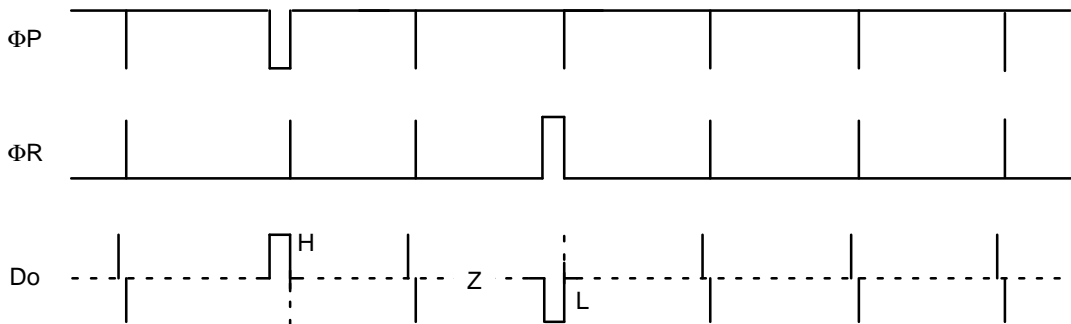
When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.



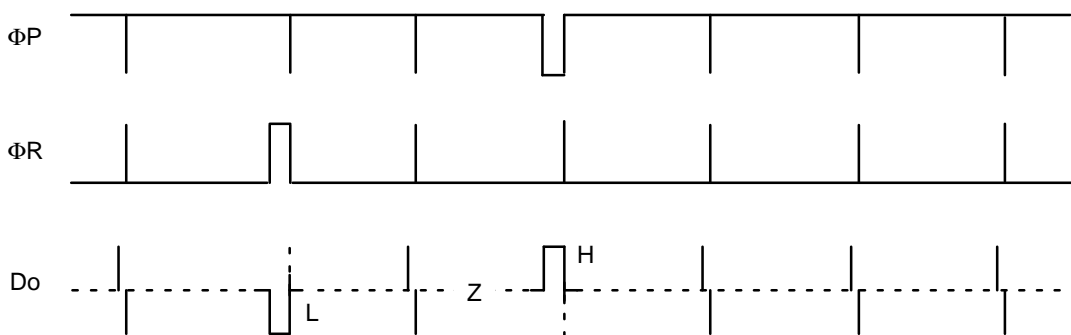
## Phase comparator output waveforms



[ FC = "H" ]



[ FC = "L" ]



- Notes:**
1. Phase difference detection range:  $-2\pi$  to  $+2\pi$
  2. LD output becomes low when phase error is  $t_{wu}$  or more. LD output becomes high when phase error is  $t_{wl}$  or less and continues to be so for three cycles or more.
  3.  $t_{wu}$  and  $t_{wl}$  depend on OSCin input frequency.  
 $t_{wu} \geq 8/f_{osc}$  (e. g.  $t_{wu} \geq 625\text{ns}$ ,  $f_{osc} = 12.8\text{ MHz}$ )  
 $t_{wl} \leq 16/f_{osc}$  (e. g.  $t_{wl} \leq 1250\text{ns}$ ,  $f_{osc} = 12.8\text{ MHz}$ )



## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Supply voltage	$V_{CC}$	2.7	3.0	3.6	V	
	$V_p$	$V_{CC}$	–	5.0	V	
Input voltage	$V_I$	GND	–	$V_{CC}$	V	
Operating temperature	$T_a$	–40	–	+85	°C	

**Notes:** To protect against damage by electrostatic discharge, note the following handling precautions:

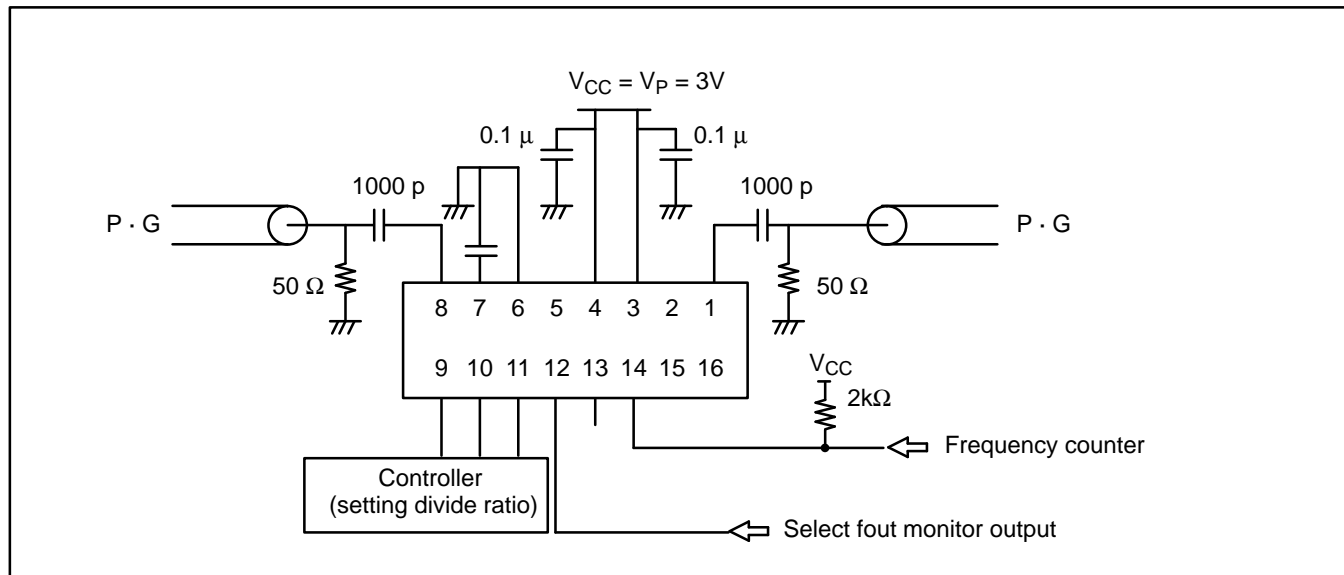
- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device.

# ELECTRICAL CHARACTERISTICS

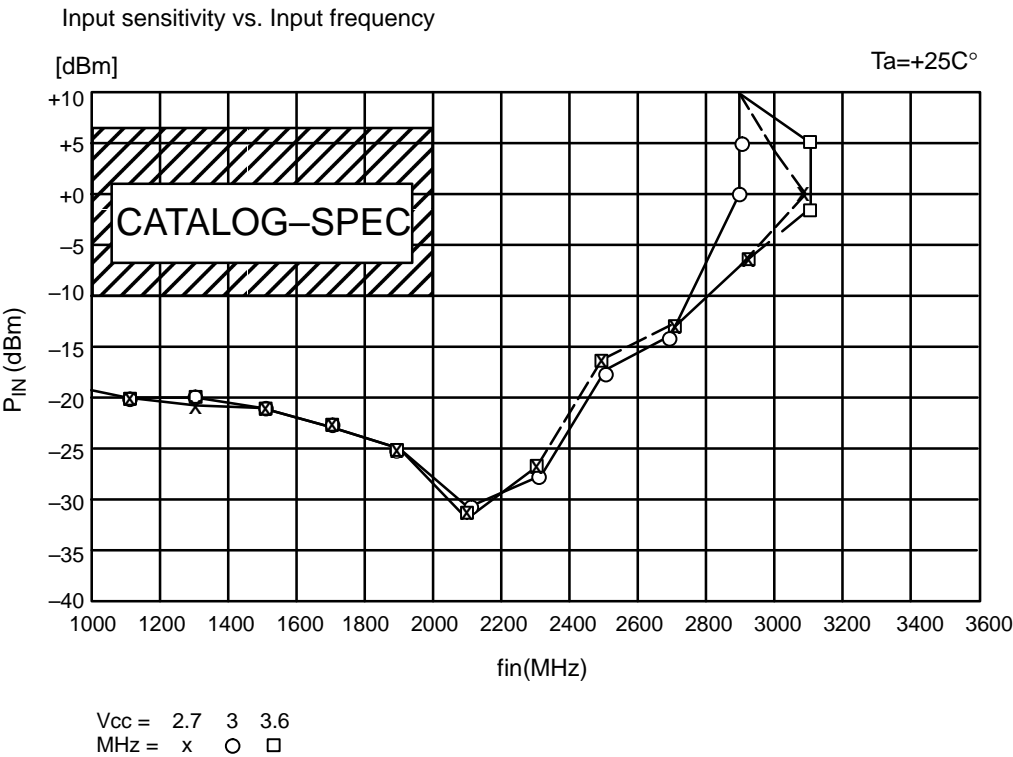
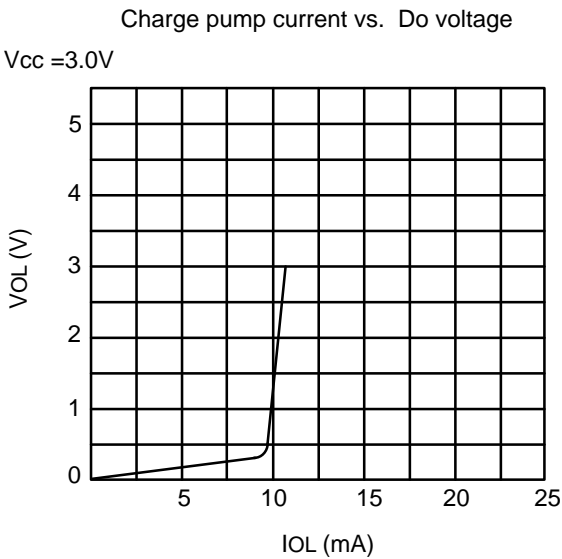
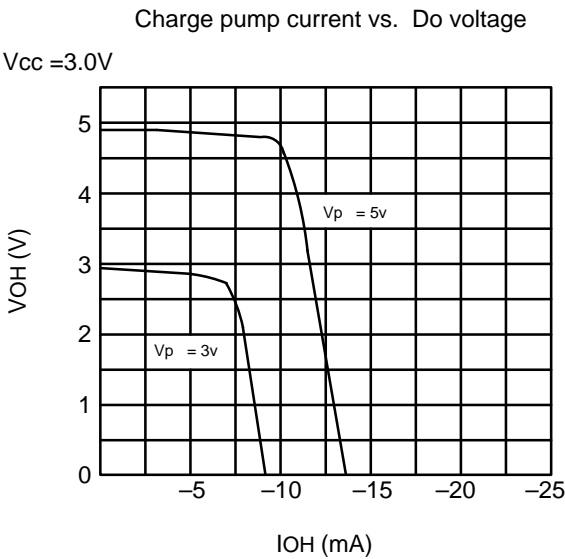
(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit	Condition
			Min	Typ	Max		
Supply current		$I_{CC}$	–	12	–	mA	With $f_{IN} = 2.0$ GHz, $OSC_{IN} = 12$ MHz, $V_{CC} = 3.0$ V. In locked state.
Stand by current		$I_{PS}$	–	100	–	$\mu A$	PS bit = "L"
Operating frequency	$f_{IN}$	$f_{IN}$	1000	–	2000	MHz	AC coupling. The minimum operating frequency is measured with a 1000pF capacitor connected.
	$OSC_{IN}$	$f_{OSC}$	–	12	23	MHz	
Input sensitivity	$f_{IN}$	$P_{f IN}$	–10	–	6	dBm	50 $\Omega$ System
	$OSC_{IN}$	$V_{OSC}$	0.5	–	–	Vp-p	
High-level input voltage	Except $f_{IN}$ and $OSC_{IN}$	$V_{IH}$	$V_{CC} \times 0.7$	–	–	V	
Low-level input voltage		$V_{IL}$	–	–	$V_{CC} \times 0.3$	V	
High-level input current	Data, Clock, LE, FC	$I_{IH}$	–	–	1.0	$\mu A$	
Low-level input current		$I_{IL}$	–1.0	–	–	$\mu A$	
Input current	$OSC_{IN}$	$I_{OSC}$	–100		+100	$\mu A$	
High-level output voltage	Except $D_O$ and $OSC_{OUT}$	$V_{OH}$	2.1	–	–	V	$V_{CC} = 3$ V, $I_{OH} = -1.0$ mA
Low-level output voltage		$V_{OL}$	–	–	0.4	V	$V_{CC} = 3$ V, $I_{OL} = 1.0$ mA
High-impedance Cut off current	$D_O$ , LD/fout, $\Phi P$	$I_{OFF}$	–	–	1.1	$\mu A$	$V_{CC} = 3.6$ V, $V_P = 5.0$ V $V_{OOP} = GND$ to 6.0 V
Output current	Except $D_O$ and $OSC_{OUT}$	$I_{OH}$	–1.0	–	–	mA	$V_{CC} = 3$ V
		$I_{OL}$	–	–	1.0	mA	$V_{CC} = 3$ V

## TEST CIRCUIT (for Measuring Input Sensitivity fin/OSCin)

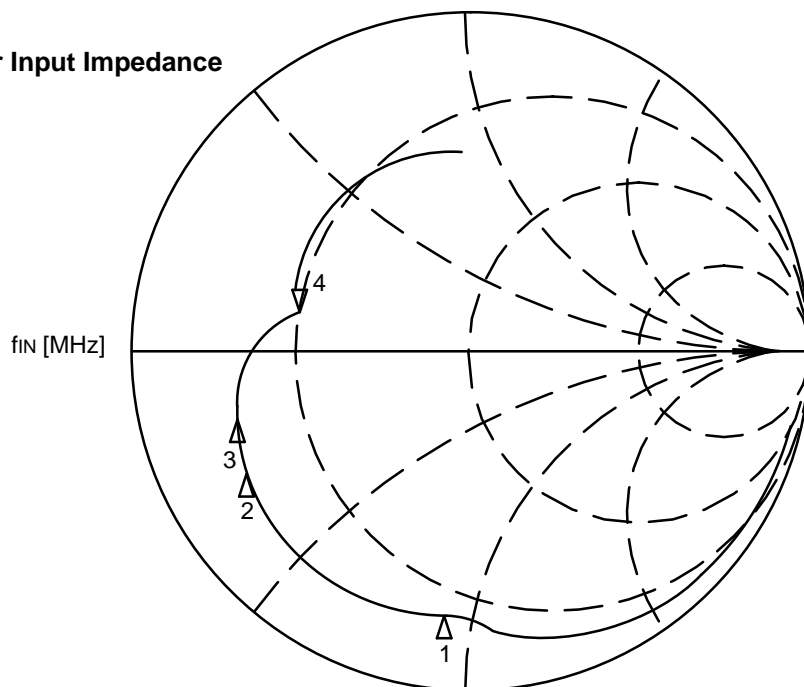


TYPICAL CHARACTERISTIC CURVES



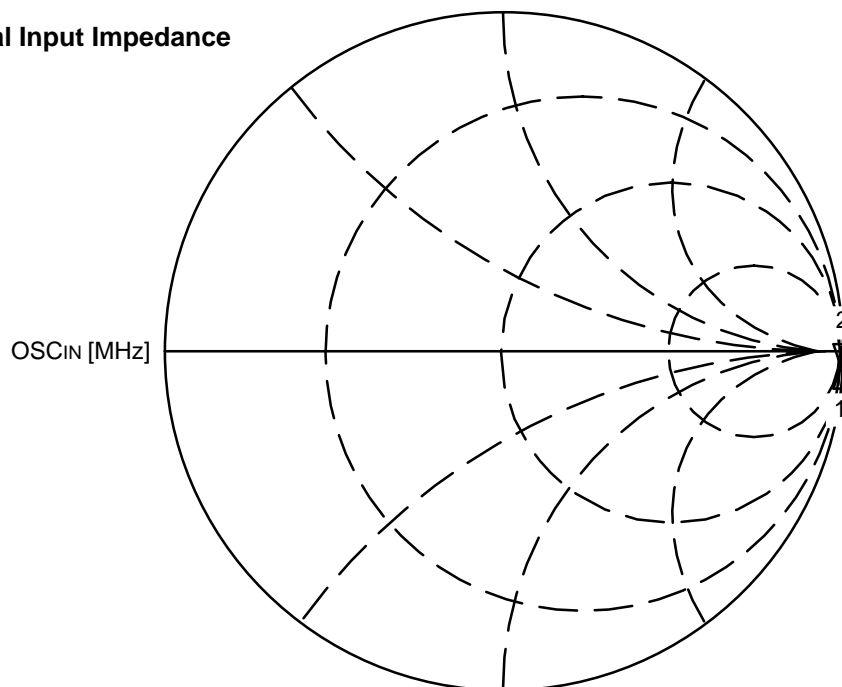
# TYPICAL CHARACTERISTIC CURVES (Continued)

## Prescaler Input Impedance



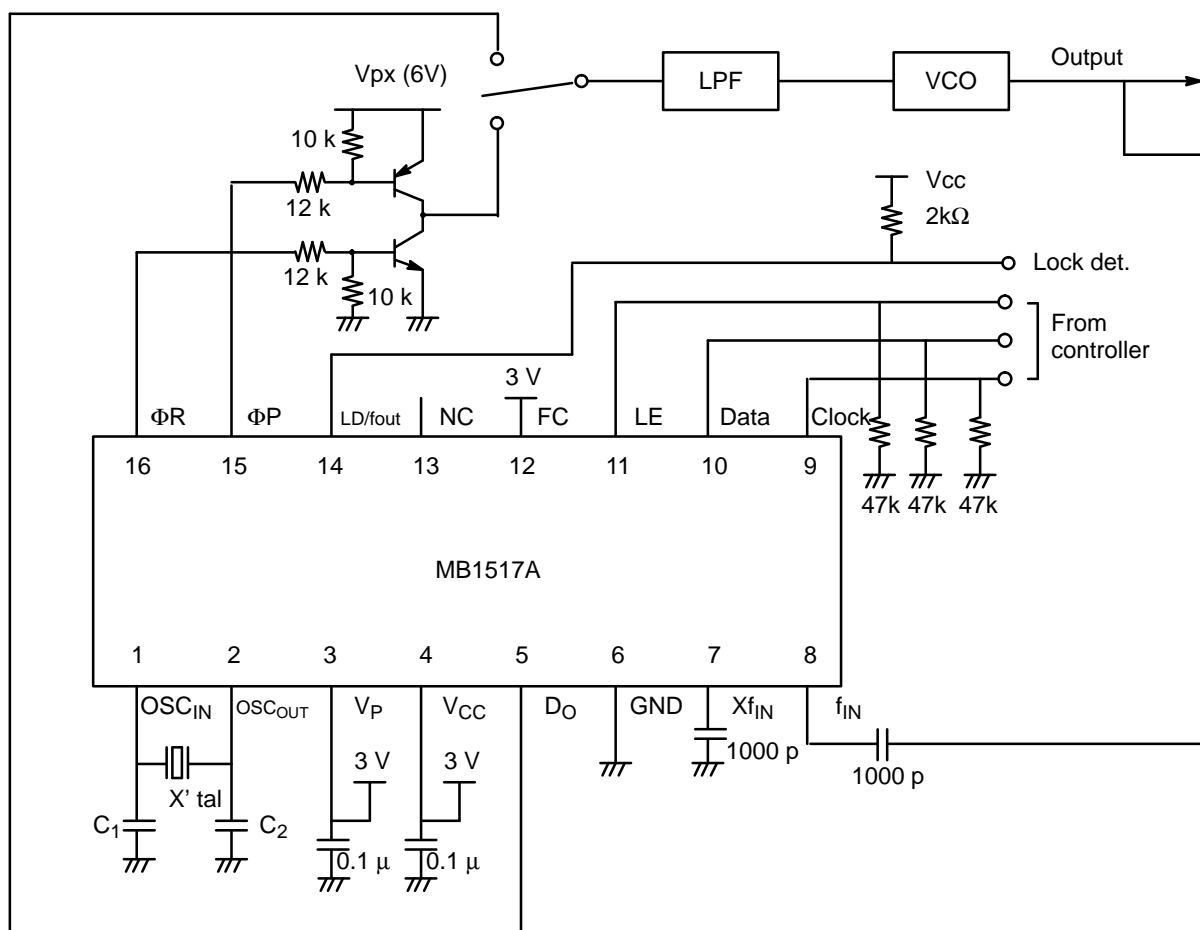
- |    |                  |
|----|------------------|
| 1: | 11.115 $\Omega$  |
|    | -45.209 $\Omega$ |
|    | 1 GHz            |
| 2: | 8.3428 $\Omega$  |
|    | -12.503 $\Omega$ |
|    | 1.5 GHz          |
| 3: | 9.2764 $\Omega$  |
|    | -7.1001 $\Omega$ |
|    | 1.6 GHz          |
| 4: | 17.173 $\Omega$  |
|    | 5.8379 $\Omega$  |
|    | 2 GHz            |

## Crystal Input Impedance



- |    |                  |
|----|------------------|
| 1: | 2.1155 $\Omega$  |
|    | -4.4665 $\Omega$ |
|    | 10 MHz           |
| 2: | 426.63 $\Omega$  |
|    | -2.201 $k\Omega$ |
|    | 25 MHz           |

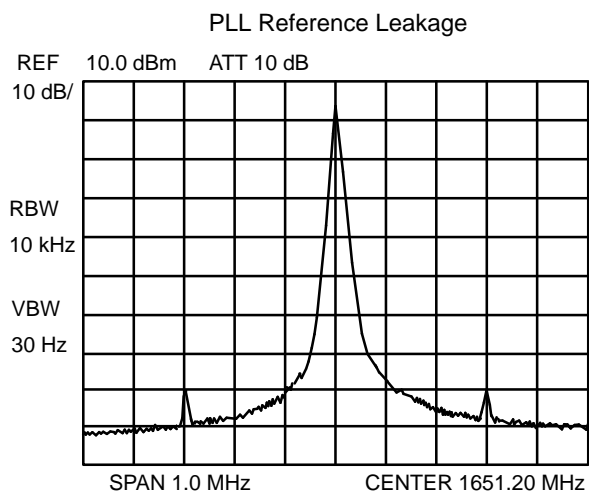
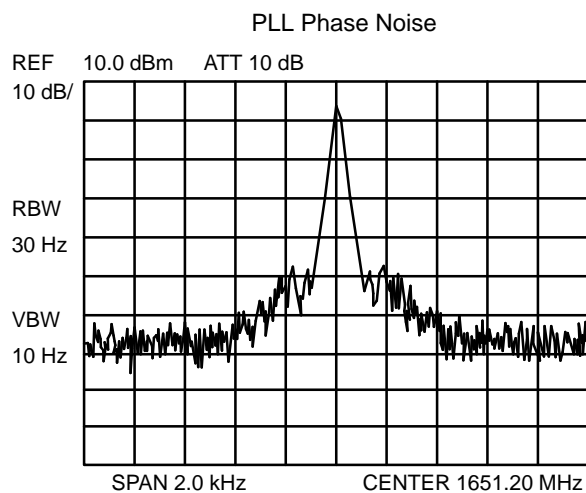
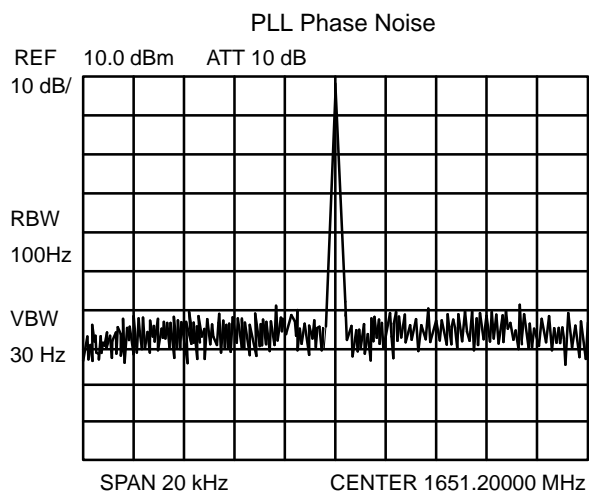
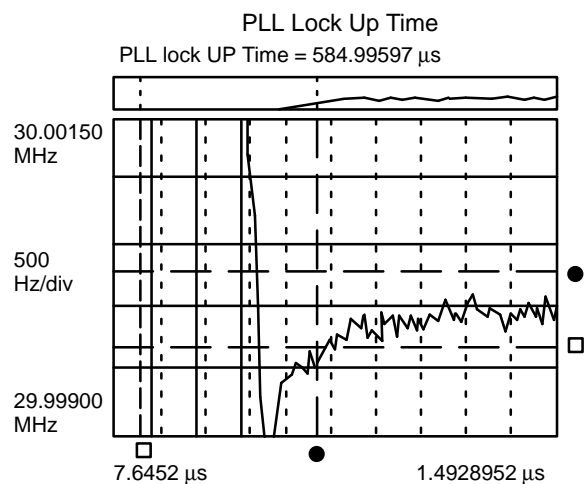
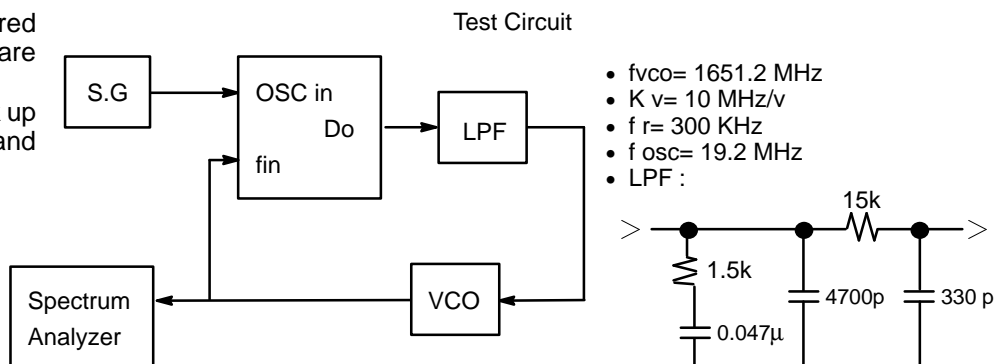
## TYPICAL APPLICATION EXAMPLE



$V_{PX}$  : Maximum 6 V  
 $C_1, C_2$  : Depend on the crystal oscillator  
 $\Phi P, LD/fout$  : N-ch open drain output  
 $\Phi R$  : C-MOS output

## REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below. Each plot shows lock up time, phase noise, and reference leakage.



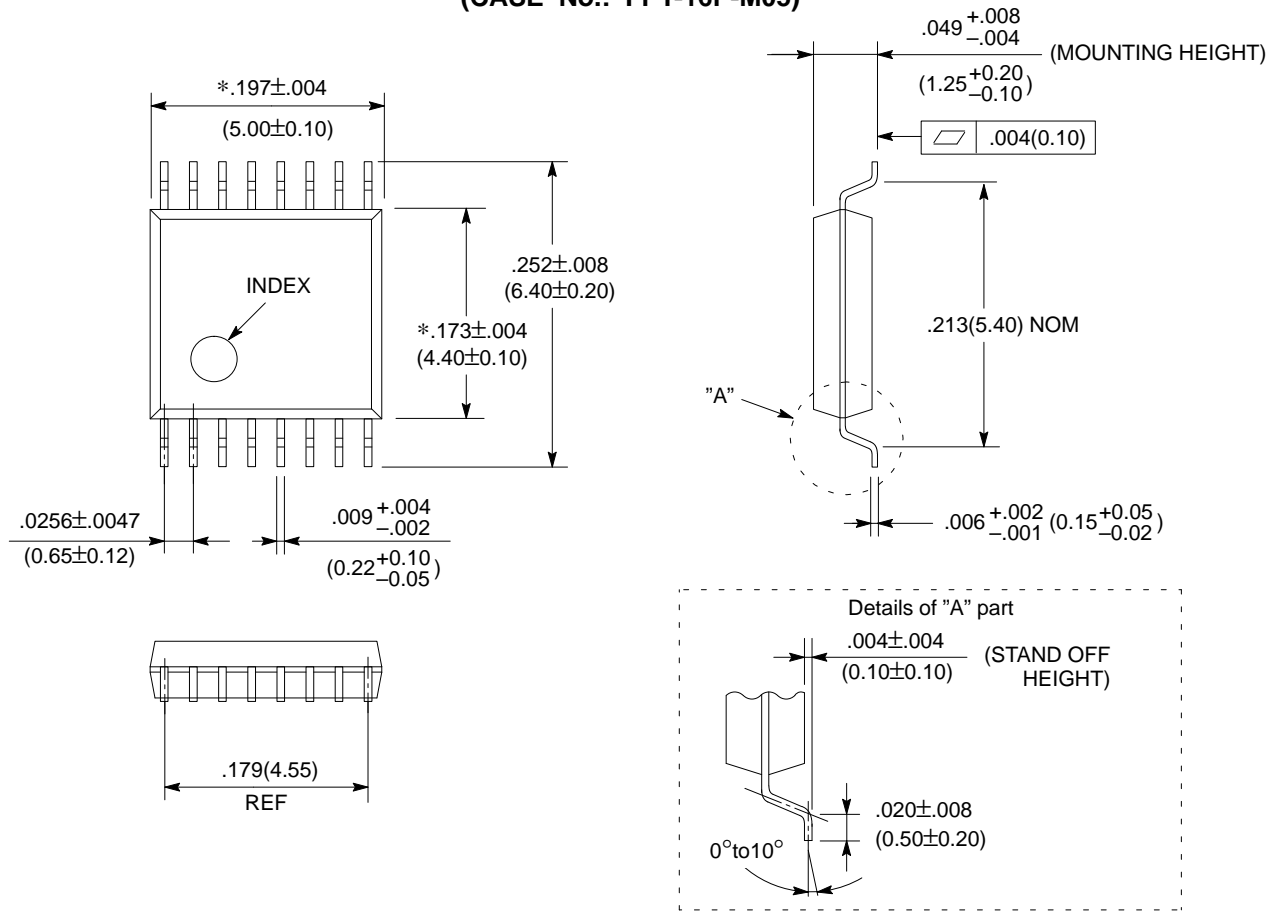
## ORDERING INFORMATION

Part number	Package	Remarks
MB1517APFV1	Plastic · SSOP, 16-pin (FPT-16P-M05)	



# PACKAGE DIMENSION

## 16-LEAD PLASTIC FLAT PACKAGE (CASE No.: FPT-16P-M05)



\*:This dimension does not include resin protrusion.

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Dimensions in  
inches (millimeters)

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