

LINEAR IC CMOS

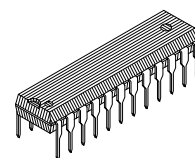
8 BIT 4-CHANNEL D/A CONVERTER

MB86022

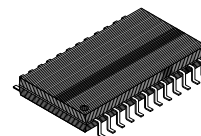
CMOS 8-BIT 4-CHANNEL D/A CONVERTER

The Fujitsu MB86022 is a 8-bit 4-channel Digital to Analog Converter which is fabricated with Fujitsu CMOS Technology. The data latch and output buffer circuitry are provided on each channel which can operate independently selected by 2bit data.

- Resolution : 8-Bits (4-channels)
- Conversion Rate : 200k sps
- Digital Input Voltage : TTL Level
- Power Supply Voltage : +5V
- Low Power Dissipation : 14mW typ. at +5V
- Each channel operates independently
- On-chip Data Initialization & Power Down Function
- Reference voltage mode selection: On-chip or External generation
- Easy to take interface with micro processor (Parallel Data Input)



**PLASTIC PACKAGE
DIP-24P-M03**



**PLASTIC PACKAGE
FPT-24P-M02**

PIN ASSIGNMENT (TOP VIEW)

D0	<input type="checkbox"/>	1	24	<input type="checkbox"/>	RESET
D1	<input type="checkbox"/>	2	23	<input type="checkbox"/>	PD
D2	<input type="checkbox"/>	3	22	<input type="checkbox"/>	V _{DD}
D3	<input type="checkbox"/>	4	21	<input type="checkbox"/>	VR2
D4	<input type="checkbox"/>	5	20	<input type="checkbox"/>	VR1
D5	<input type="checkbox"/>	6	19	<input type="checkbox"/>	AO0
D6	<input type="checkbox"/>	7	18	<input type="checkbox"/>	AO1
D7	<input type="checkbox"/>	8	17	<input type="checkbox"/>	AO2
C0	<input type="checkbox"/>	9	16	<input type="checkbox"/>	AO3
C1	<input type="checkbox"/>	10	15	<input type="checkbox"/>	N.C.
WR	<input type="checkbox"/>	11	14	<input type="checkbox"/>	AG
CE	<input type="checkbox"/>	12	13	<input type="checkbox"/>	DG

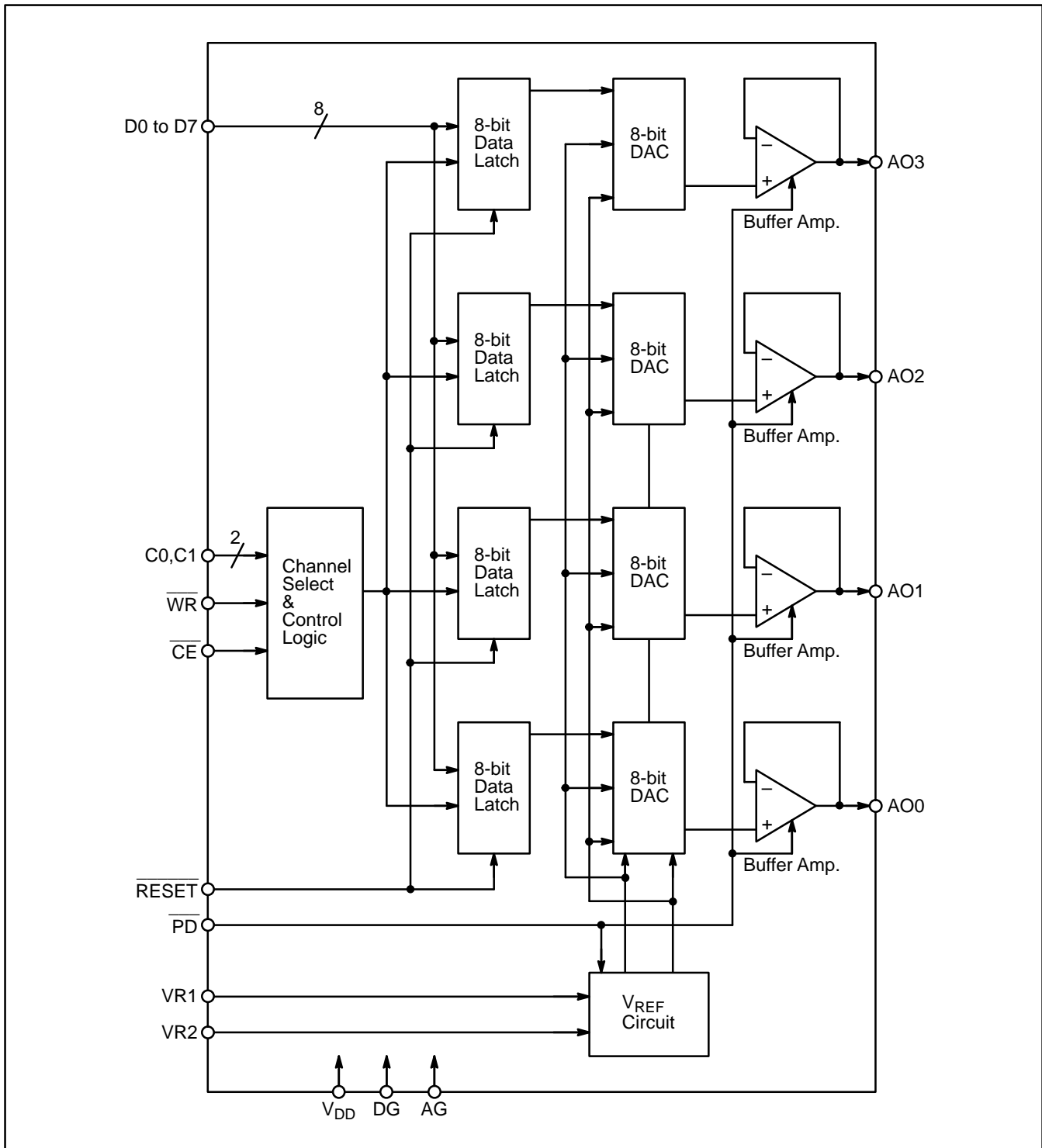
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Pin Name	Rating			Unit
			Min	Typ	Max	
Power supply voltage	V_{DD}	V_{DD}	GND-0.3	–	7	V
Digital input voltage	V_{DI}	All digital input pins	GND-0.3	–	$V_{DD}+0.3$	V
Analog input voltage	V_1, V_2	VR1, VR2	GND-0.3	–	$V_{DD}+0.3$	V
Analog output voltage	V_{AO}	AO0, AO1, AO2, AO3	GND-0.3	–	$V_{DD}+0.3$	V
Analog output current	I_{AO}	AO0, AO1, AO2, AO3	-10	–	10	mA
Storage temperature	Tstg		-40	–	125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



PIN DESCRIPTION

System	Pin Number	Symbol	Descriptions															
Power Supply	22	V _{DD}	Power Supply Voltage 5V															
	13	DG	GND for Digital System															
	14	AG	GND for Analog System															
Digital Input	23	$\overline{\text{PD}}$	Power down control signal pin. The circuit is set power down when this pin goes to “L”. This pin is pulled up by high resistance. TTL interface.															
	24	$\overline{\text{RESET}}$	Reset input signal pin. The data at all channels is initialized when this pin goes to “L”. At this time, the D/A output is set at D(A)=128. This pin is pulled up by high resistance. TTL interface.															
	12	$\overline{\text{CE}}$	Chip enable signal pin. The data can be written when this pin goes to “L”. This pin is pulled up by high resistance. TTL interface.															
	11	$\overline{\text{WR}}$	Data write pin. The data from D0 to D7 is written when the rising edge (L → H) of this pin. TTL interface.															
	9	C0	Channel selection signal pin. Channels are selected by following table. TTL interface. <table><tr><th>C1</th><th>C0</th><th>Channel</th></tr><tr><td>L</td><td>L</td><td>0</td></tr><tr><td>L</td><td>H</td><td>1</td></tr><tr><td>H</td><td>L</td><td>2</td></tr><tr><td>H</td><td>H</td><td>3</td></tr></table>	C1	C0	Channel	L	L	0	L	H	1	H	L	2	H	H	3
	C1	C0		Channel														
	L	L	0															
	L	H	1															
	H	L	2															
	H	H	3															
	10	C1																
	1	D0	Data input signal pin. The digital data is read by the channel which is selected by C0 and C1 pins when the rising edge of $\overline{\text{WR}}$ (L → H), and analog output is shown correspond to that digital code. D0 is LSB and D7 is MSB. Code is set at 10000000 when reset. TTL interface.															
	2	D1																
	3	D2																
	4	D3																
5	D4																	
6	D5																	
7	D6																	
8	D7																	
Analog Input	20	VR ₁	Reference voltage (H level) input pin. V _{DD} is given by internal reference voltage circuitry to this pin when internal reference voltage mode. In this case, the capacitor between this pin and AG pin is required to limit noise generation. In case of external reference voltage mode, the reference voltage should be given from this pin.															
	21	VR ₂	Middle point of reference voltage input pin. Reference voltage (H level) input pin. $\frac{1}{2}$ V _{DD} is given by internal reference voltage circuitry to this pin when internal reference voltage mode. In this case, the capacitor between this pin and AG pin is required to limit noise generation. In case of external reference voltage mode, the reference voltage should be given from this pin.															

(Continued)

System	Pin Number	Symbol	Descriptions
Analog Output	16	AO3	Analog output pin of channel 3. This pin is set to high-impedance state at Power Down.
	17	AO2	Analog output pin of channel 2. This pin is set to high-impedance state at Power Down.
	18	AO1	Analog output pin of channel 1. This pin is set to high-impedance state at Power Down.
	19	AO0	Analog output pin of channel 0. This pin is set to high-impedance state at Power Down.
–	15	N.C.	No connection pin

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin Name	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{DD}	V_{DD}	4.75	5.0	5.25	V
Digital input voltage	V_{DI}	All digital input pins	0	–	V_{DD}	V
Analog input voltage	V_1	VR1	1.2	3.75	3.8	V
	V_2	VR2	$\frac{V_1+1.2}{2}$	2.5	$\frac{V_1+3.8}{2}$	V
Analog output load resistance	R_{AL}	AO0, AO1, AO2, AO3	20	–	–	k Ω
Analog output load capacitance	C_{AL}		–	–	50	pF
Operating temperature	T_a		–20	–	70	°C

ELECTRICAL CHARACTERISTICS

(V_{DD}=4.75V to 5.25V, Ta=−20°C to 70°C)

Parameter		Symbol	Pin Name	Conditions	Value			Unit
					Min	Typ	Max	
Power supply current		I _{DD1}	V _{DD}	No load	—	2.8	5.5	mA
		I _{DD2}						
Digital input	"L" Voltage	V _{IL}	All digital input pins	PD="H"	0	—	0.8	V
	"H" Voltage	V _{IH}		PD="L"	2.2	—	V _{DD}	V
	"L" Current	I _{IL}	D0 to D7, $\overline{\text{WR}}$	V _{DI} =GND	−10	—	10	μA
	"H" Current	I _{IH}		V _{DI} =V _{DD}	−10	—	10	μA
Pull up current		I _{PLU}	$\overline{\text{PD}}$, $\overline{\text{CE}}$, $\overline{\text{RESET}}$	V _{DI} =GND	−100	−50	−25	μA
$\overline{\text{WR}}$ "H" Width		t _{WHWR}	$\overline{\text{WR}}$	Ref. to timing chart	200	—	—	ns
$\overline{\text{WR}}$ "L" Width		t _{WLWR}	$\overline{\text{WR}}$	Ref. to timing chart	200	—	—	ns
Digital input "L" width		t _{WLRP}	$\overline{\text{RESET}}$, $\overline{\text{PD}}$	Ref. to timing chart	500	—	—	ns
DATA Set up time 1		t _{SD1}	D0 to D7, $\overline{\text{WR}}$	Ref. to timing chart	100	—	—	ns
DATA Set up time 2		t _{SD2}	C0, C1, $\overline{\text{WR}}$	Ref. to timing chart	100	—	—	ns
$\overline{\text{CE}}$ Set up time		t _{SCE}	$\overline{\text{CE}}$, $\overline{\text{WR}}$	Ref. to timing chart	0	—	—	ns
DATA Hold time 1		t _{HD1}	D0 to D7, $\overline{\text{WR}}$	Ref. to timing chart	50	—	—	ns
DATA Hold time 2		t _{HD2}	C0, C1, $\overline{\text{WR}}$	Ref. to timing chart	50	—	—	ns
$\overline{\text{CE}}$ Hold time		t _{HCE}	$\overline{\text{CE}}$, $\overline{\text{WR}}$	Ref. to timing chart	0	—	—	ns

(Continued)

(V_{DD}=4.75V to 5.25V, Ta=–20°C to 70°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit
				Min	Typ	Max	
Rising time 1	t _{r1}	WR	Ref. to timing chart	0	–	50	ns
Falling time 1	t _{f1}	WR	Ref. to timing chart	0	–	50	ns
Rising time 2	t _{r2}	D0 to D7, C0, C1, $\overline{\text{CE}}$, RESET, PD	Ref. to timing chart	0	–	50	ns
Falling time 2	t _{f2}	D0 to D7, C0, C1, $\overline{\text{CE}}$, RESET, PD	Ref. to timing chart	0	–	50	ns
Resolution	Res	AO0, AO1, AO2, AO3		–	8	–	bits
Analog output Min. voltage	V _{AOL1}		Input code D(A)= 0 No external VR input VR1=open VR2=open	(Typ.) –0.1	$\frac{V_{DD}}{4}$	(Typ.) +0.1	V
	V _{AOL2}		External VR input VR1=V ₁ VR2=V ₂	(Typ.) –0.1	2xV ₂ –V ₁	(Typ.) +0.1	V
Analog output Max. voltage	V _{AOH1}		Input code D(A)= 255 No external VR input VR1=open VR2=open	(Typ.) –0.1	$\frac{383}{512} \times V_{DD}$	(Typ.) +0.1	V
	V _{AOH2}		External VR input VR1=V ₁ VR2=V ₂	(Typ.) –0.1	$V_1 - \frac{V_1 - V_2}{128}$	(Typ.) +0.1	V
Analog input resistance	R _I	VR ₁ , VR ₂		30	50	200	kΩ
Linearity error	LE	AO0, AO1, AO2, AO3	No external VR input VR1=open VR2=open	–1.5	–	1.5	LSB
Differential linearity error	D _{LE}			–1	–	1	LSB
Setting time	t _S		Full scale change (Ref. to timing chart)	–	–	5	μs

FUNCTION DESCRIPTION

TRUTH TABLE


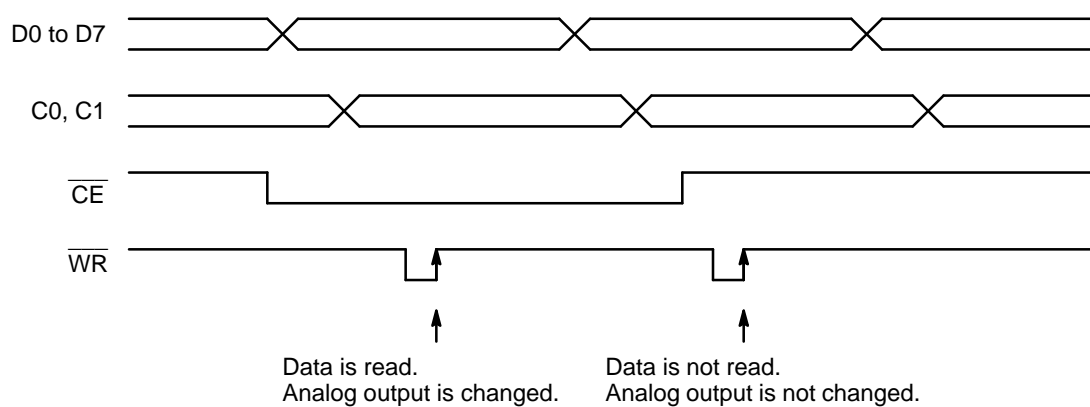
$\overline{\text{PD}}$	$\overline{\text{RESET}}$	$\overline{\text{CE}}$	$\overline{\text{WR}}$	C0, C1	D0 to D7	Function
0	x	x	x	—	—	Power down
1	0	x	x	—	—	Initialization
1	1	1	x	—	No data input	No analog output change
1	1	0		Channel selectiion	Data input	Analog output change

Fig. 1 – DATA SET TIMING DIAGRAM



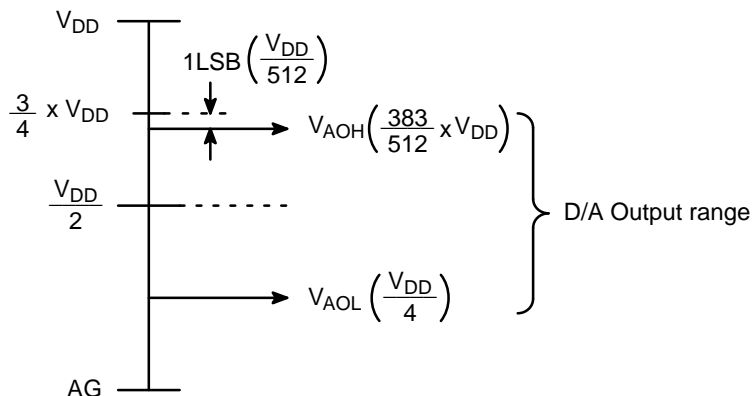
SETTING OF ANALOG OUTPUT VOLTAGE

Data									Analog Output Voltage		
D(A)	D7	D6	D5	D4	D3	D2	D1	D0	VR1=Open VR2=Open (No external VR input)	VR1=V ₁ VR2=Open (External VR1 input)	VR1=V ₁ VR2=V ₂ (External VR input)
255	1	1	1	1	1	1	1	1	$\frac{383}{512} \times V_{DD}$	$\frac{2xV_1-V_{DD}}{256} \times 127 + \frac{V_{DD}}{2}$	$\frac{V_1-V_2}{128} \times 127 + V_2$
254	1	1	1	1	1	1	1	0	$\frac{382}{512} \times V_{DD}$	$\frac{2xV_1-V_{DD}}{256} \times 126 + \frac{V_{DD}}{2}$	$\frac{V_1-V_2}{128} \times 126 + V_2$
253	1	1	1	1	1	1	0	1	$\frac{381}{512} \times V_{DD}$	$\frac{2xV_1-V_{DD}}{256} \times 125 + \frac{V_{DD}}{2}$	$\frac{V_1-V_2}{128} \times 125 + V_2$
⋮	⋮								$\frac{V_{DD}}{512} \times (D(A)-128) + \frac{V_{DD}}{2}$	$\frac{2xV_1-V_{DD}}{256} \times (D(A)-128) + \frac{V_{DD}}{2}$	$\frac{V_1-V_2}{128} \times (D(A)-128) + V_2$
129	1	0	0	0	0	0	0	1	$\frac{257}{512} \times V_{DD}$	$\frac{2xV_1-V_{DD}}{256} + \frac{V_{DD}}{2}$	$\frac{V_1-V_2}{128} + V_2$
128	1	0	0	0	0	0	0	0	$\frac{V_{DD}}{2}$	$\frac{V_{DD}}{2}$	V_2
127	0	1	1	1	1	1	1	1	$\frac{255}{512} \times V_{DD}$	$\frac{2xV_1-V_{DD}}{256} \times (-1) + \frac{V_{DD}}{2}$	$\frac{V_1-V_2}{128} \times (-1) + V_2$
126	0	1	1	1	1	1	1	0	$\frac{254}{512} \times V_{DD}$	$\frac{2xV_1-V_{DD}}{256} \times (-2) + \frac{V_{DD}}{2}$	$\frac{V_1-V_2}{128} \times (-2) + V_2$
⋮	⋮								⋮	⋮	⋮
2	0	0	0	0	0	0	1	0	$\frac{130}{512} \times V_{DD}$	$\frac{2xV_1-V_{DD}}{256} \times (-126) + \frac{V_{DD}}{2}$	$\frac{V_1-V_2}{128} \times (-126) + V_2$
1	0	0	0	0	0	0	0	1	$\frac{129}{512} \times V_{DD}$	$\frac{2xV_1-V_{DD}}{256} \times (-127) + \frac{V_{DD}}{2}$	$\frac{V_1-V_2}{128} \times (-127) + V_2$
0	0	0	0	0	0	0	0	0	$\frac{V_{DD}}{4}$	$V_{DD}-V_1$	$-(V_1-V_2) + V_2$
1LSB									$\frac{V_{DD}}{512}$	$\frac{2xV_1-V_{DD}}{256}$	$\frac{V_1-V_2}{128}$

* Code is set at "10000000" when reset mode.

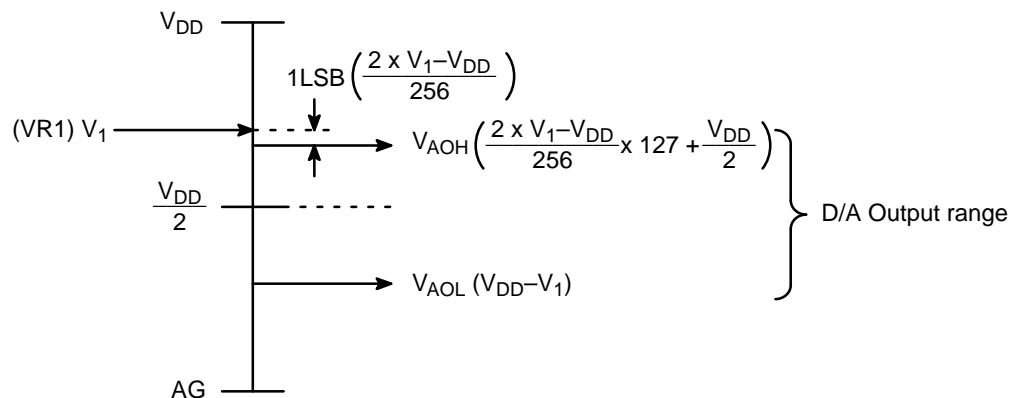
ANALOG OUTPUT VOLTAGE RANGE

Fig. 2 – ON-CHIP REFERENCE VOLTAGE MODE (NO EXTERNAL VR INPUT)



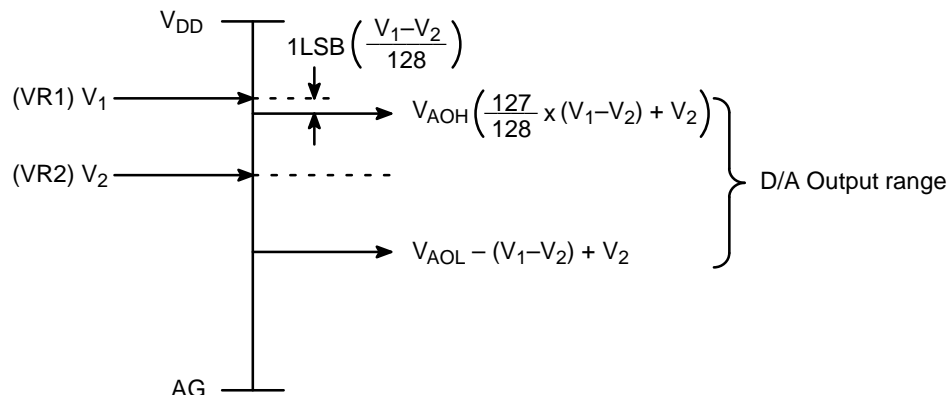
(VR1=V₁, VR2=1/2xV_{DD})

Fig. 3 – EXTERNAL REFERENCE VOLTAGE MODE



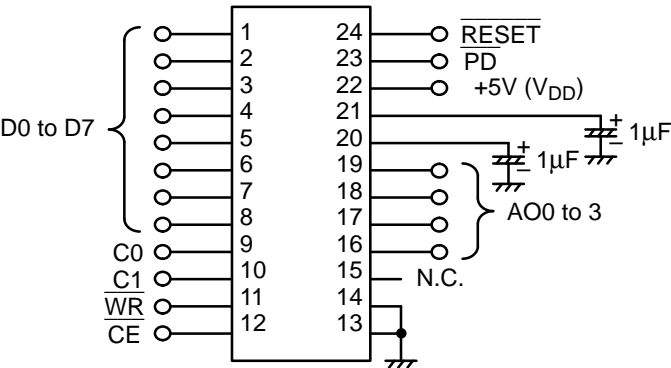
(VR1=V₁, VR2=V₂)

Fig. 4 – EXTERNAL REFERENCE VOLTAGE MODE



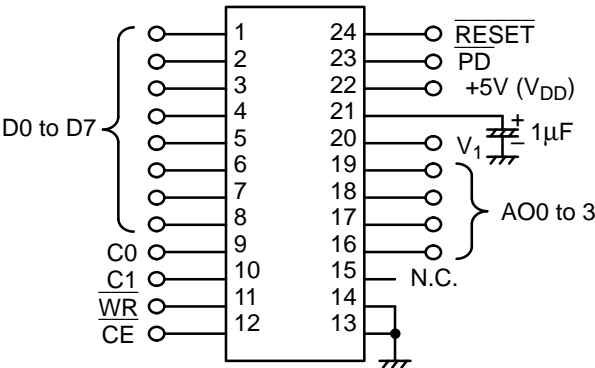
TYPICAL APPLICATION CIRCUIT FOR EACH MODE

Fig. 5 – ON-CHIP REFERENCE VOLTAGE MODE



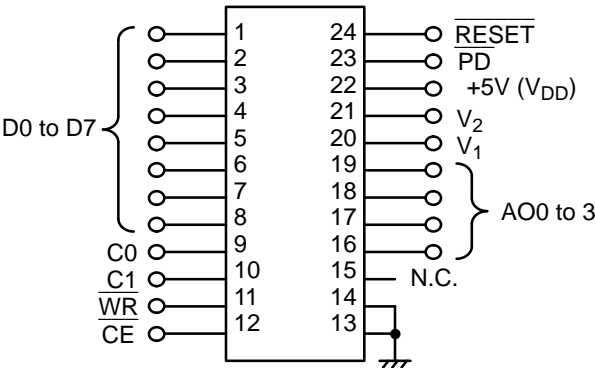
(VR1=V₁, VR2=1/2xV_{DD})

Fig. 6 – EXTERNAL REFERENCE VOLTAGE MODE

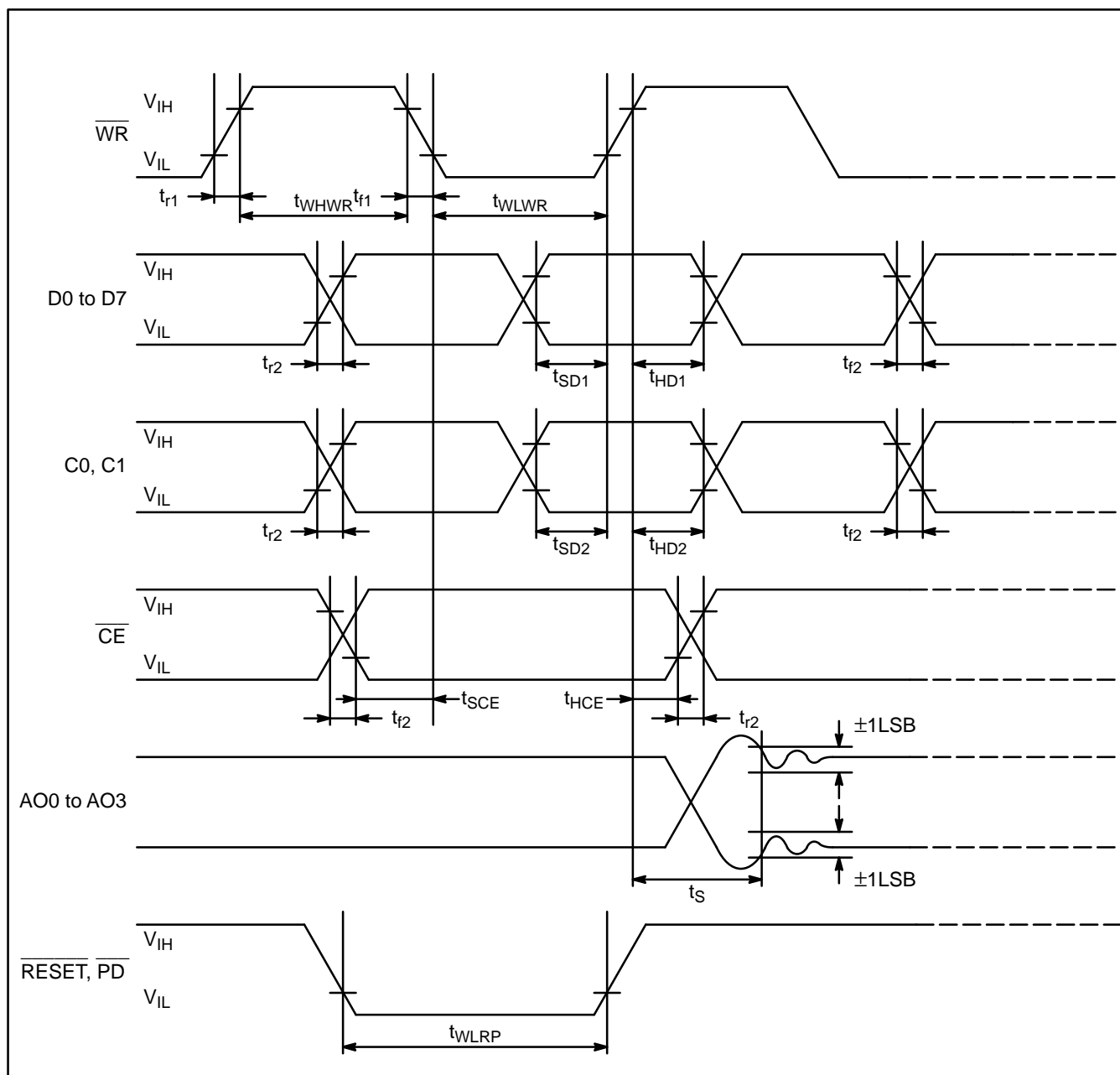


(VR1=V₁, VR2=V₂)

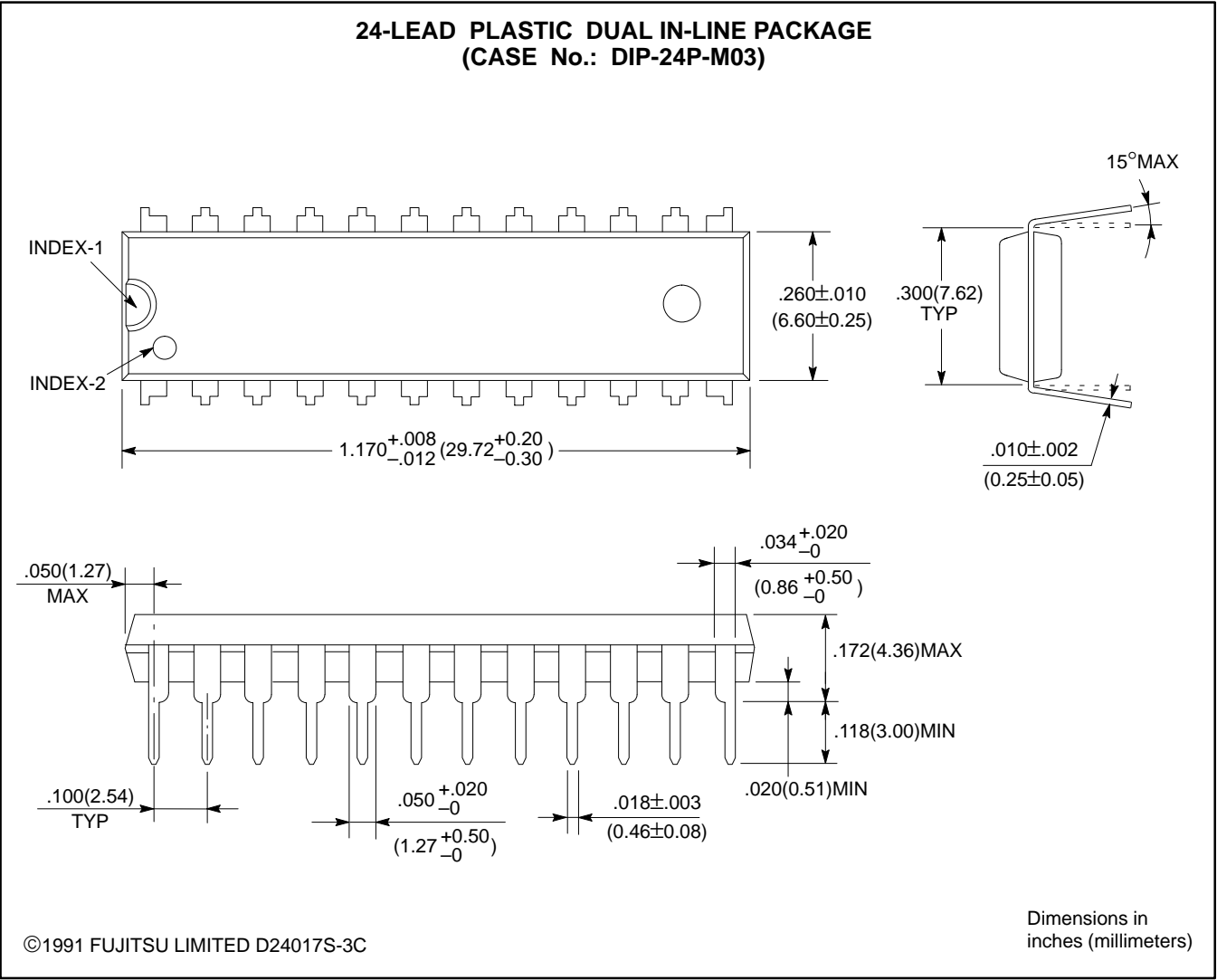
Fig. 7 – EXTERNAL REFERENCE VOLTAGE MODE



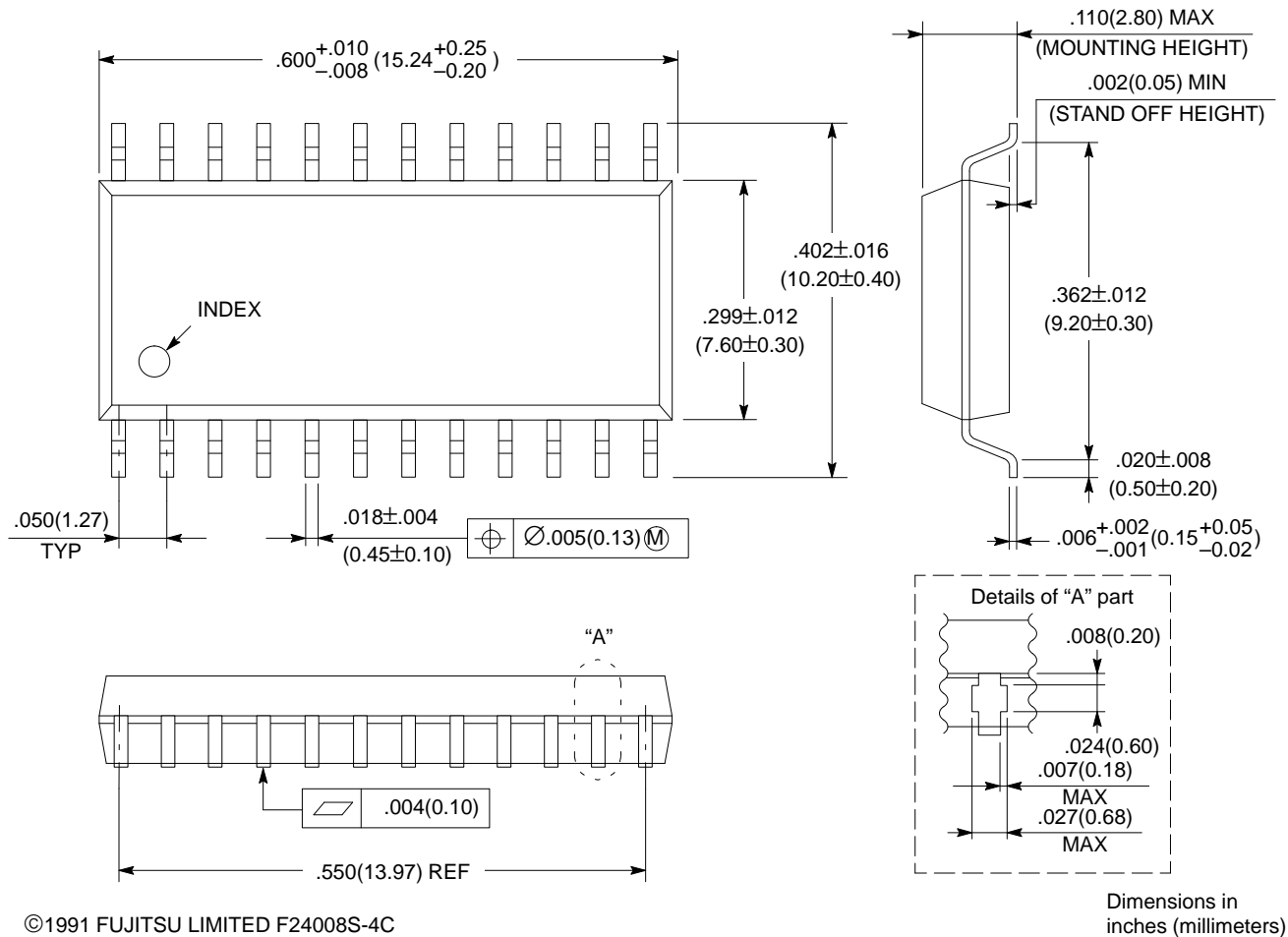
TIMING DIAGRAM



PACKAGE DIMENSIONS



**24-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-24P-M02)**



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