

8K x 8 Static RAM

Features

- **High speed**
— 20 ns
- **CMOS for optimum speed/power**
- **Low active power**
— 743 mW
- **Low standby Power**
— 220 mW
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with \overline{CE}_1 , CE_2 and \overline{OE} features**
- **Automatic power-down when deselected**

Functional Description

The CY7C185A is a high-performance CMOS static RAM organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}_1), an active HIGH chip enable (CE_2), an active LOW output enable (\overline{OE}), and three-state drivers. The device has an automatic power-down feature (\overline{CE}_1), reducing the power consumption by over 70% when deselected. The CY7C185A is in the standard 300-mil-wide DIP package and leadless chip carrier.

Writing to the device is accomplished when the chip enable one (\overline{CE}_1) and write enable (\overline{WE}) inputs are both LOW, and the chip enable two (CE_2) input is HIGH.

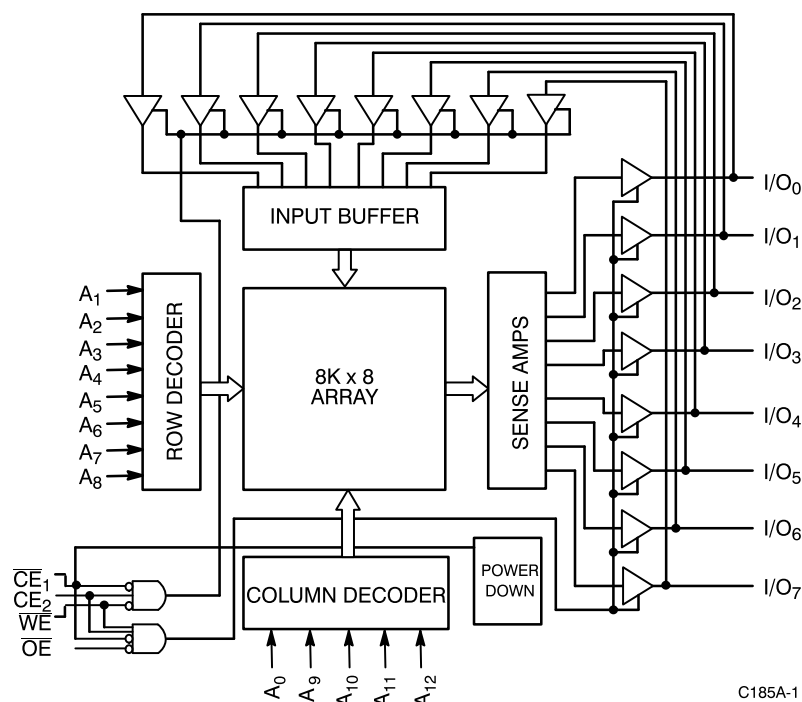
Data on the eight I/O pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{12}).

Reading the device is accomplished by taking chip enable one (\overline{CE}_1) and output enable (\overline{OE}) LOW, while taking write enable (\overline{WE}) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the I/O pins.

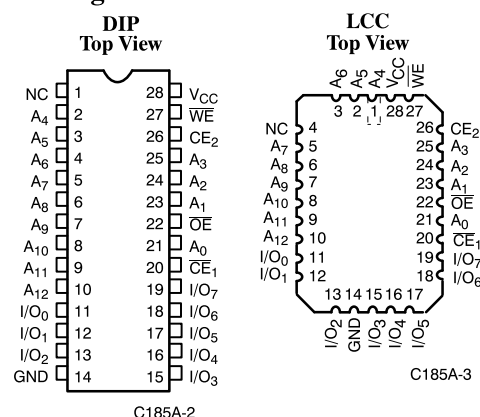
The I/O pins remain in a high-impedance state when chip enable one (\overline{CE}_1) or output enable (\overline{OE}) is HIGH, or write enable (\overline{WE}) or chip enable two (CE_2) is LOW.

A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configurations



Selection Guide^[1]

		7C185A-15	7C185A-20	7C185A-25	7C185A-35	7C185A-45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Military	170	135	125	125	125
Maximum Standby Current (mA)	Military	40/20	40/20	40/20	30/20	30/20

Shaded area contains advanced information.

Note:

1. For commercial specifications, see the CY7C185 datasheet.



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Ambient Temperature with

Power Applied -55°C to $+125^{\circ}\text{C}$

Supply Voltage to Ground Potential

(Pin 28 to Pin 14) -0.5V to $+7.0\text{V}$

DC Voltage Applied to Outputs

in High Z State^[2] -0.5V to $+7.0\text{V}$

DC Input Voltage^[2] -0.5V to $+7.0\text{V}$

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage $>2001\text{V}$
(per MIL-STD-883, Method 3015)

Latch-Up Current $>200\text{ mA}$

Operating Range

Range	Ambient Temperature	V _{CC}
Military ^[3]	-55°C to $+125^{\circ}\text{C}$	$5\text{V} \pm 10\%$

Electrical Characteristics Over the Operating Range^[4]

Parameter	Description	Test Conditions	7C185A-15		7C185A-20		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[2]		-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	$\text{GND} \leq V_I \leq V_{CC}$	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	$\text{GND} \leq V_I \leq V_{CC}$, Output Disabled	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[5]	V _{CC} = Max., V _{OUT} = GND		-350		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max. I _{OUT} = 0 mA		170		135	mA
I _{SB1}	Automatic $\overline{\text{CE}}_1$ Power-Down Current	Max. V _{CC} , $\overline{\text{CE}}_1 \geq V_{IH}$, Min. Duty Cycle = 100%		40		40	mA
I _{SB2}	Automatic $\overline{\text{CE}}_1$ Power-Down Current	Max. V _{CC} , $\overline{\text{CE}}_1 \geq V_{CC} - 0.3\text{V}$ V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≥ 0.3V		20		20	mA

Shaded area contains advanced information.

Notes:

- V_{IL} (min.) = -3.0V for pulse durations less than 30 ns.
- T_A is the “instant on” case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range^[4] (continued)

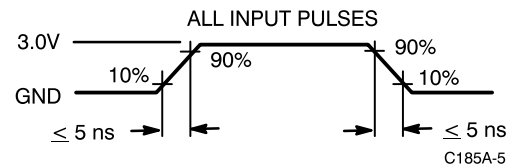
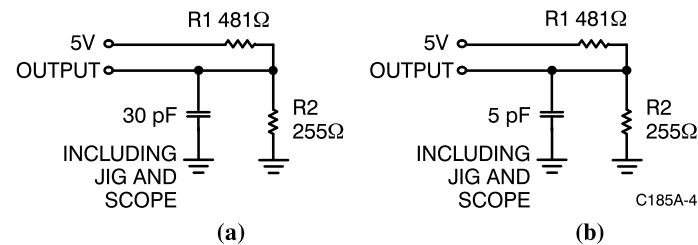
Parameter	Description	Test Conditions	7C185A-25		7C185A-35, 45		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[2]		-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[5]	V _{CC} = Max., V _{OUT} = GND		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		125		125	mA
I _{SB1}	Automatic \overline{CE}_1 Power-Down Current	Max. V _{CC} , $\overline{CE}_1 \geq V_{IH}$, Min. Duty Cycle = 100%		40		30	mA
I _{SB2}	Automatic \overline{CE}_1 Power-Down Current	Max. V _{CC} $\overline{CE}_1 \geq V_{CC} - 0.3V$ V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≥ 0.3V		20		20	mA

Capacitance^[6]

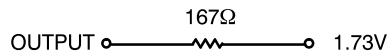
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Note:

6. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms


Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range^[3, 7]

Parameter	Description	7C185A–15		7C185A–20		7C185A–25		7C185A–35		7C185A–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	15		20		25		35		45		ns
t _{AA}	Address to Data Valid		15		20		25		35		45	ns
t _{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t _{ACE1}	\overline{CE}_1 LOW to Data Valid		15		20		25		35		45	ns
t _{ACE2}	CE ₂ HIGH to Data Valid		15		20		25		35		30	ns
t _{DOE}	\overline{OE} LOW to Data Valid		7		10		12		15		20	ns
t _{LZOE}	\overline{OE} LOW to Low Z	0		3		3		3		3		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[8]		8		8		10		12		15	ns
t _{LZCE1}	\overline{CE}_1 LOW to Low Z ^[9]	3		5		5		5		5		ns
t _{LZCE2}	CE ₂ HIGH to Low Z	3		3		3		3		3		ns
t _{HZCE}	\overline{CE}_1 HIGH to High Z ^[8, 9] CE ₂ LOW to High Z		8		8		10		15		15	ns
t _{PU}	\overline{CE}_1 LOW to Power-Up	0		0		0		0		0		ns
t _{PD}	\overline{CE}_1 HIGH to Power-Down		15		20		20		20		25	ns
WRITE CYCLE ^[10]												
t _{WC}	Write Cycle Time	15		20		20		25		40		ns
t _{SCE1}	\overline{CE}_1 LOW to Write End	10		15		20		25		30		ns
t _{SCE2}	CE ₂ HIGH to Write End	10		15		20		25		30		ns
t _{AW}	Address Set-Up to Write End	10		15		20		25		30		ns
t _{HA}	Address Hold from Write End	0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t _{PWE}	\overline{WE} Pulse Width	10		15		15		20		20		ns
t _{SD}	Data Set-Up to Write End	7		10		10		15		15		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		ns
t _{LZWE}	\overline{WE} HIGH to Low Z	3		3		5		5		5		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[8]		7		7		7		10		15	ns

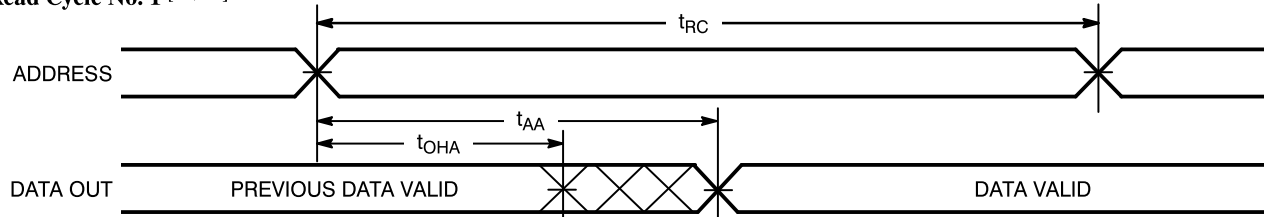
Shaded area contains advanced information.

Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
- Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$. CE₂ = V_{IH}.

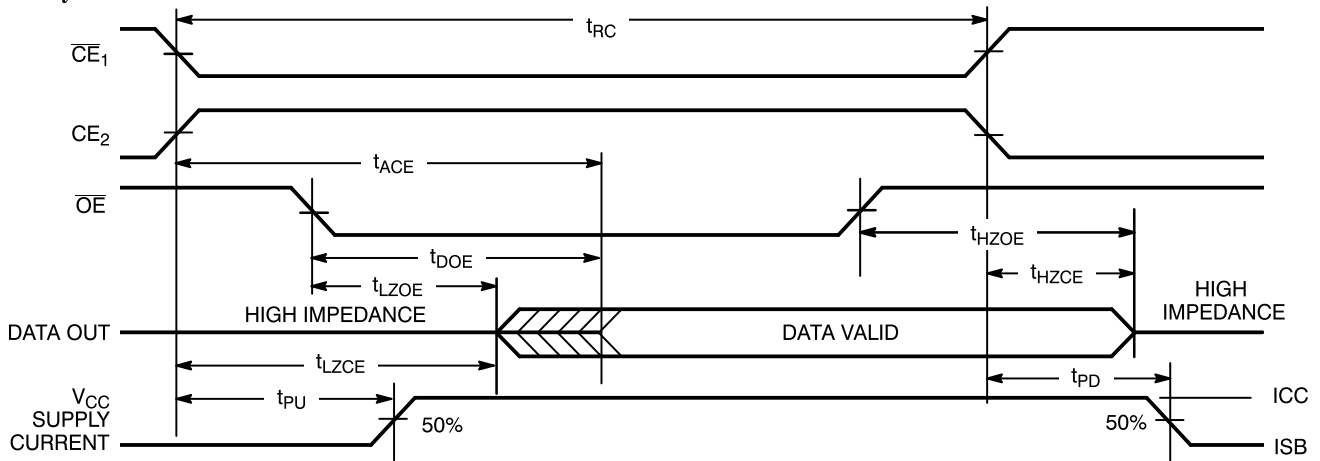
Switching Waveforms

Read Cycle No. 1 [10, 11]



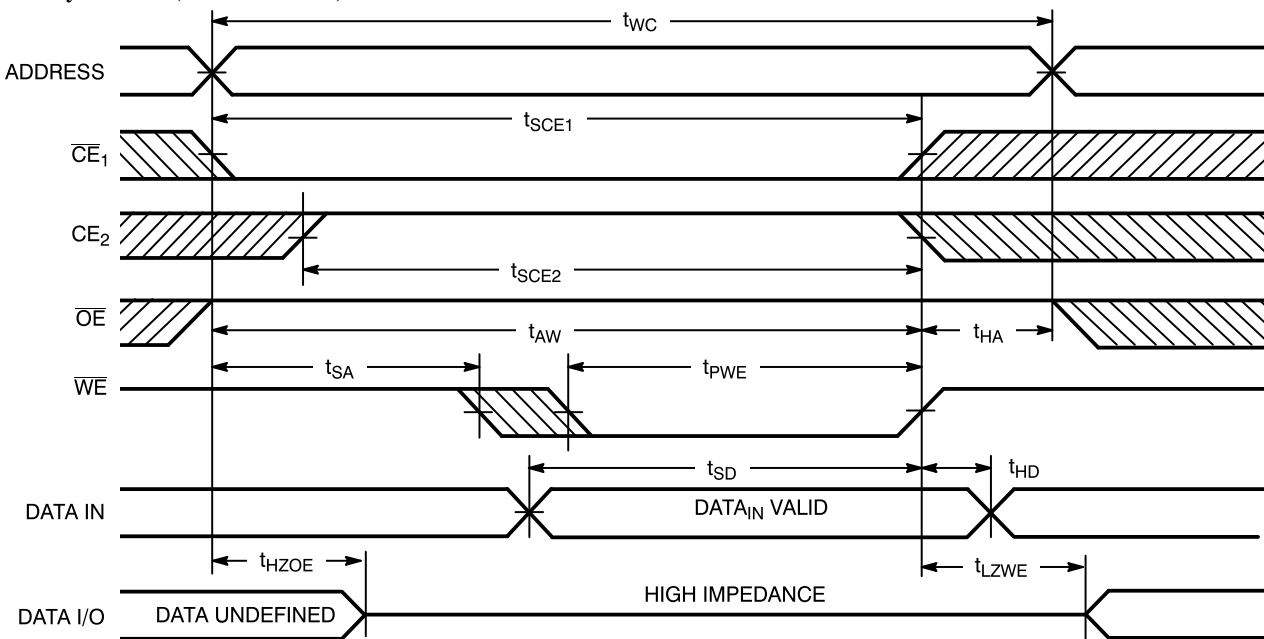
C185A-6

Read Cycle No. 2 [11, 12]



C185A-7

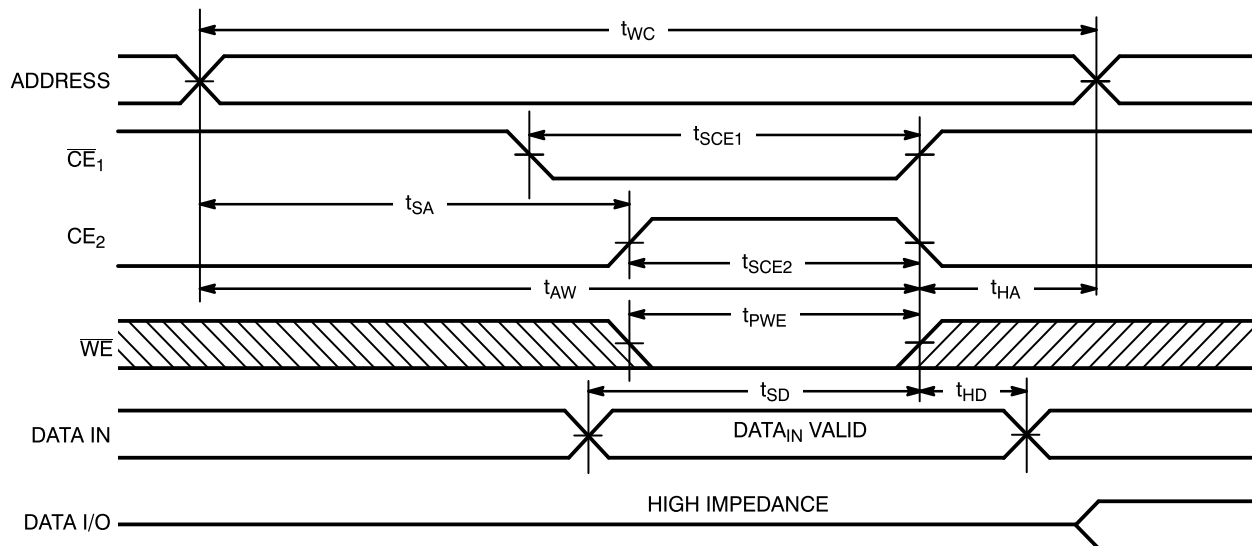
Write Cycle No. 1 (\overline{WE} Controlled) [13, 14]



C185A-8

Notes:

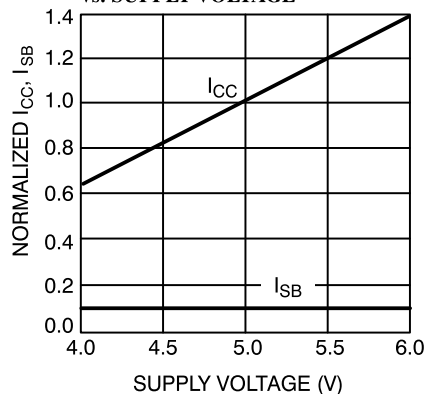
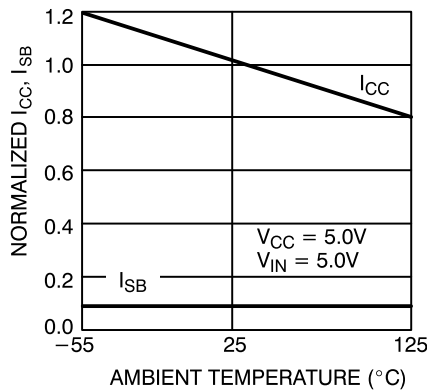
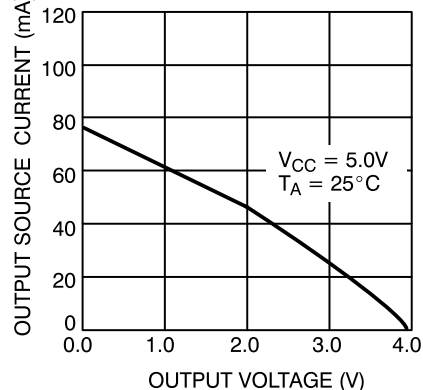
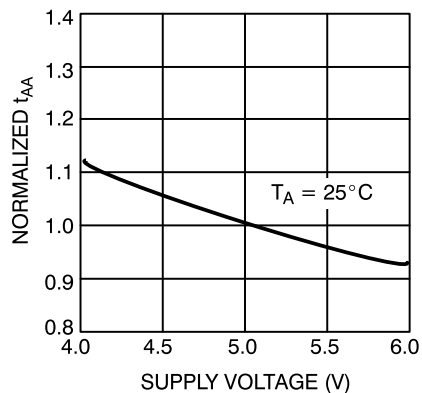
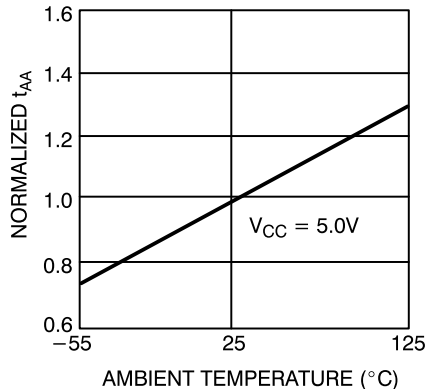
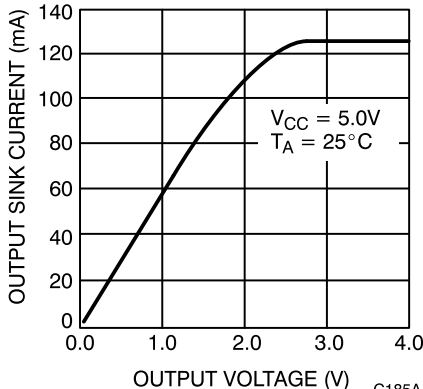
11. Address valid prior to or coincident with \overline{CE} transition LOW.
12. \overline{WE} is HIGH for read cycle.
13. The internal write time of the memory is defined by the overlap of \overline{CE}_1 LOW, \overline{CE}_2 HIGH, and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
14. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

Switching Waveforms (continued)
Write Cycle No. 2 (\overline{CE} Controlled) [13, 14, 15]


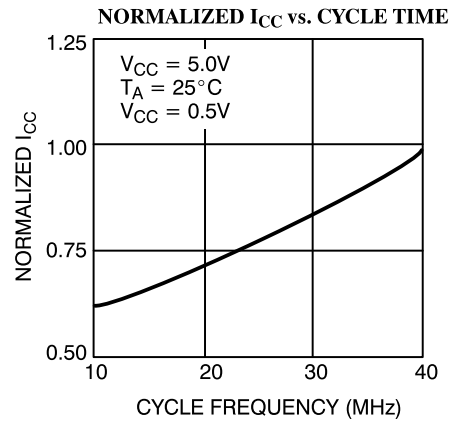
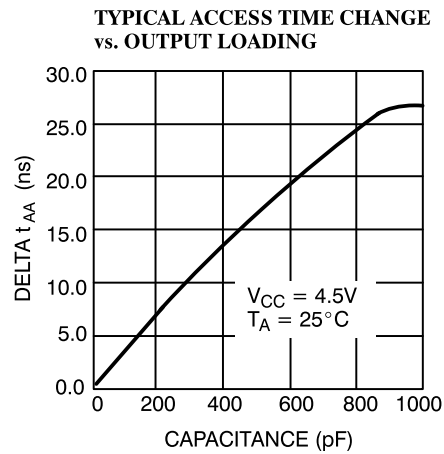
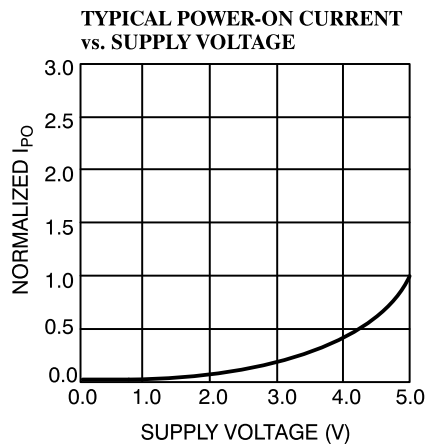
C185A-9

Note:

15. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE

OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE


C185A-10

Typical DC and AC Characteristics (continued)


C185A-11

Truth Table

\overline{CE}_1	CE_2	\overline{WE}	\overline{OE}	Input/Output	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

Address Designators

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C185A-15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C185A-20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A-20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C185A-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A-25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C185A-35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A-35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C185A-45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A-45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains advanced information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL} Max.	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{OS}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3

Switching Characteristics

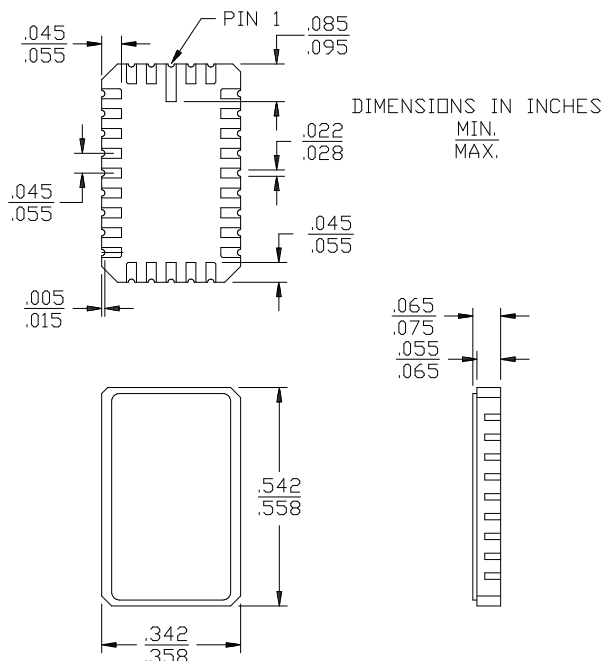
Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE1}	7, 8, 9, 10, 11
t _{ACE2}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE1}	7, 8, 9, 10, 11
t _{SCE2}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

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Package Diagrams

28-Pin Rectangular Leadless Chip Carrier L54

MIL-STD-1835 C-11A



28-Lead (300-Mil) CerDIP D22

MIL-STD-1835 D-15 Config. A

