



256K x 4 Static RAM

Features

- **High speed**
— $t_{AA} = 10$ ns
- **CMOS for optimum speed/power**
- **Center power/ground pinout**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C1014 is a high-performance CMOS static RAM organized as 262,144

words by 4 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}), and three-state drivers. The device has an automatic power-down feature that significantly reduces power consumption when deselected.

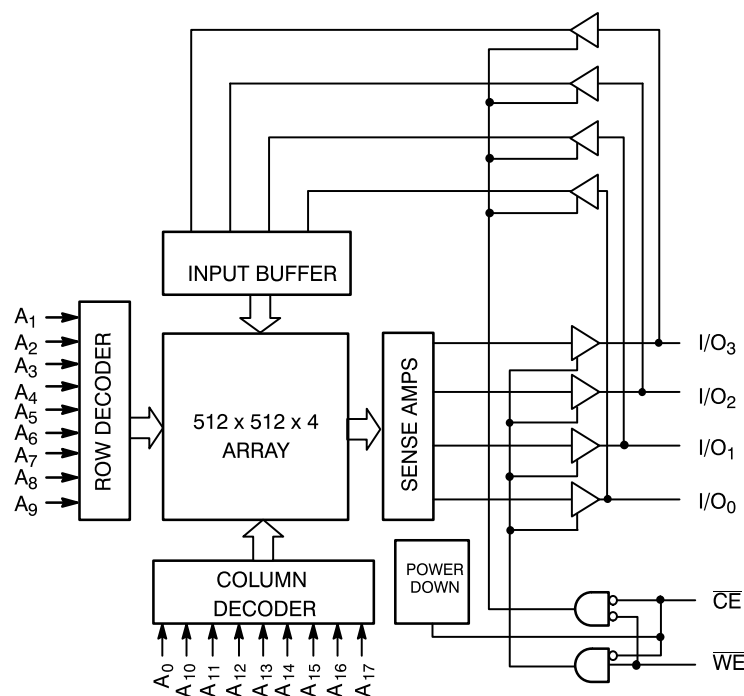
Writing to the device is accomplished by taking chip enable (\overline{CE}) and write enable (\overline{WE}) inputs LOW. Data on the four I/O pins (I/O_0 through I/O_3) is then written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking chip enable (\overline{CE}) LOW while forcing write enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the four I/O pins.

The four input/output pins (I/O_0 through I/O_3) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), or during a write operation (\overline{CE} and \overline{WE} LOW).

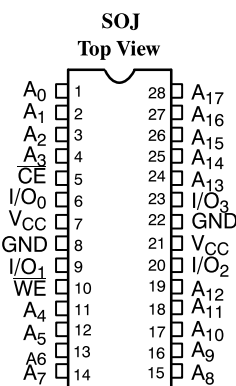
The CY7C1014 is available in standard 400-mil-wide SOJs.

Logic Block Diagram



C1014-1

Pin Configuration



C1014-2

Selection Guide

		7C1014-10	7C1014-12	7C1014-15
Maximum Access Time (ns)		10	12	15
Maximum Operating Current (mA)	Commercial	175	165	155
	Military		175	165
Maximum Standby Current (mA)	Commercial	55	50	40
	Military		50	40

Document #: 38-00454